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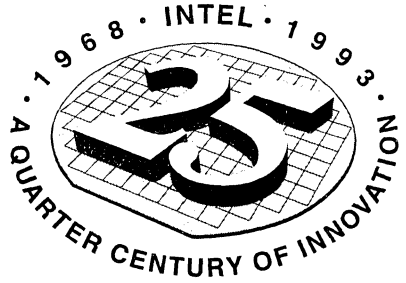

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MCS®-48 Single Component System

1

THE SINGLE COMPONENT MCS®-48 SYSTEM

1.0 INTRODUCTION

Sections 2 through 5 describe in detail the functional characteristics of the 8748H and 8749H EPROM, 8048AH/8049AH/8050AH ROM, and 8035AHL/8039AHL/8040-AHL CPU only single component microcomputers. Unless otherwise noted, details within these sections apply to all versions. This chapter is limited to those functions useful in single-chip implementations of the MCS®-48. The Chapter on the Expanded MCS®-48 System discusses functions which allow expansion of program memory, data memory, and input output capability.

2.0 ARCHITECTURE

The following sections break the MCS-48 Family into functional blocks and describe each in detail. The following description will use the 8048AH as the representative product for the family. See Figure 1.

2.1 Arithmetic Section

The arithmetic section of the processor contains the basic data manipulation functions of the 8048AH and can be divided into the following blocks:

- Arithmetic Logic Unit (ALU)
- Accumulator
- Carry Flag
- Instruction Decoder

In a typical operation data stored in the accumulator is combined in the ALU with data from another source on the internal bus (such as a register or I/o port) and the result is stored in the accumulator or another register.

The following is more detailed description of the function of each block.

INSTRUCTION DECODER

The operation code (op code) portion of each program instruction is stored in the Instruction Decoder and converted to outputs which control the function of each of the blocks of the Arithmetic Section. These lines control the source of data and the destination register as well as the function performed in the ALU.

ARITHMETIC LOGIC UNIT

The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under control of the Instruction Decoder. The ALU can perform the following functions:

- Add With or Without Carry
- AND, OR, Exclusive OR
- Increment/Decrement
- Bit Complement
- Rotate Left, Right
- Swap Nibbles
- BCD Decimal Adjust

If the operation performed by the ALU results in a value represented by more than 8 bits (overflow of most significant bit), a Carry Flag is set in the Program Status Word.

ACCUMULATOR

The accumulator is the single most important data register in the processor, being one of the sources of input to the ALU and often the destination of the result of operations performed in the ALU. Data to and from I/O ports and memory also normally passes through the accumulator.

2.2 Program Memory

Resident program memory consists of 1024, 2048, or 4096 words eight bits wide which are addressed by the program counter. In the 8748H and the 8749H this memory is user programmable and erasable EPROM; in the 8048AH/8049AH/8050AH the memory is ROM which is mask programmable at the factory. The 8035AHL/8039AHL/8040AHL has no internal program memory and is used with external memory devices. Program code is completely interchangeable among the various versions. To access the upper 2K of program memory in the 8050AH, and other MCS-48 devices, a select memory bank and a JUMP or CALL instruction must be executed to cross the 2K boundary.

There are three locations in Program Memory of special importance as shown in Figure 2.

LOCATION 0
Activating the Reset line of the processor causes the first instruction to be fetched from location 0.

LOCATION 3
Activating the Interrupt input line of the processor (if interrupt is enabled) causes a jump to subroutine at location 3.

LOCATION 7
A timer/counter interrupt resulting from timer counter overflow (if enabled) causes a jump to subroutine at location 7.

Therefore, the first instruction to be executed after initialization is stored in location 0, the first word of an external interrupt service subroutine is stored in location 3, and the first word of a timer/counter service routines

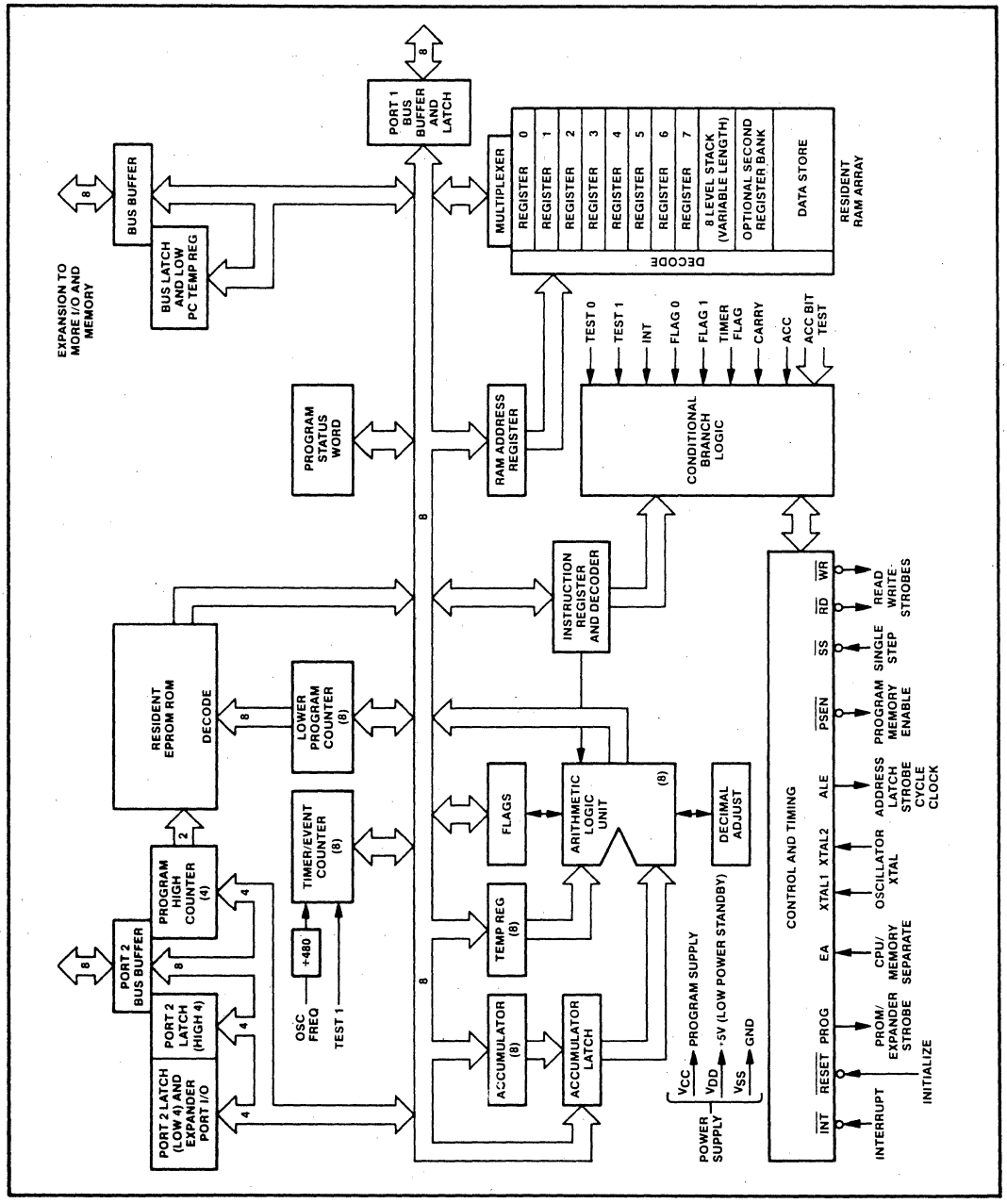


Figure 1. 8748H/8048H/8749AH/8050AH Block Diagram

is stored in location 7. Program memory can be used to store constants as well as program instructions. Instructions such as MOVP and MOVP3 allow easy access to data "lookup" tables.

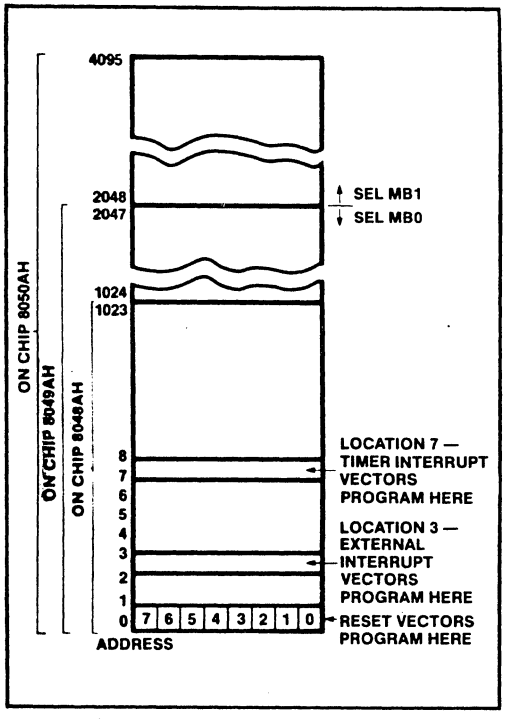


Figure 2. Program Memory Map

2.3 Data Memory

Resident data memory is organized as 64, 128, or 256 by 8-bits wide in the 8048AH, 8049AH and 8050AH. All locations are indirectly addressable through either of two RAM Pointer Registers which reside at address 0 and 1 of the register array. In addition, as shown in Figure 3, the first 8 locations (0–7) of the array are designated as working registers and are directly addressable by several instructions. Since these registers are more easily addressed, they are usually used to store frequently accessed intermediate results. The DJNZ instruction makes very efficient use of the working registers as program loop counters by allowing the programmer to decrement and test the register in a single instruction.

By executing a Register Bank Switch instruction (SEL RB) RAM locations 24–31 are designated as the working registers in place of locations 0–7 and are then directly addressable. This second bank of working registers may be used as an extension of the first bank or reserved for use during interrupt service subroutines allowing the registers of Bank 0 used in the main program to be instantly "saved" by a Bank Switch. Note that if this second bank is not used, locations 24–31 are still addressable as general purpose RAM. Since the two RAM pointer Registers R0 and R1 are a part of the working register array, bank switching effectively creates two more pointer registers (R0/and R1/) which can be used with R0 and R1 to easily access up to four separate working areas in RAM at one time. RAM locations (8–23) also serve a dual role in that they contain the program counter stack as explained in Section 2.6. These locations are addressed by the Stack Pointer during subroutine calls as well as by RAM Pointer Registers R0 and R1. If the level of subroutine nesting is less than 8, all stack registers are not required and can be used as general purpose RAM locations. Each level of subroutine nesting not used provides the user with two additional RAM locations.

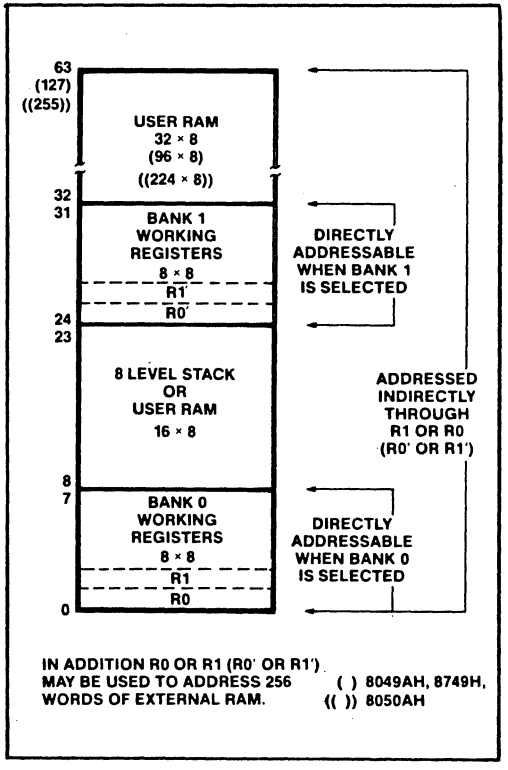


Figure 3. Data Memory Map

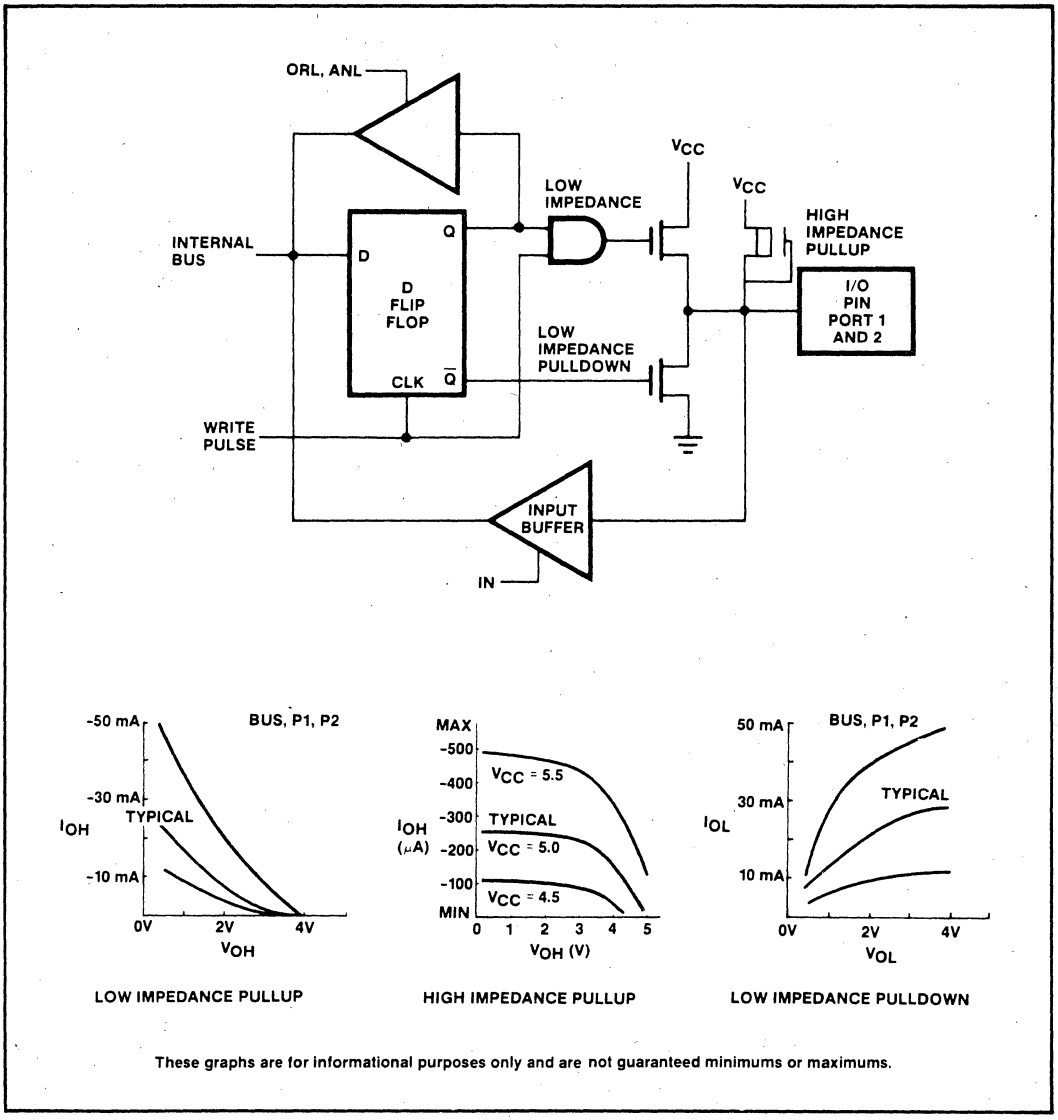


Figure 4. "Quasi-bidirectional" Port Structure

2.4 Input/Output

The 8048AH has 27 lines which can be used for input or output functions. These lines are grouped as 3 ports of 8 lines each which serve as either inputs, outputs or bidirectional ports and 3 "test" inputs which can alter program sequences when tested by conditional jump instructions.

PORTS 1 AND 2

Ports 1 and 2 are each 8 bits wide and have identical characteristics. Data written to these ports is statically latched and remains unchanged until rewritten. As input ports these lines are non-latching, i.e., inputs must be present until read by an input instruction. Inputs are fully TTL compatible and outputs will drive one standard TTL load.

The lines of ports 1 and 2 are called quasi-bidirectional because of a special output circuit structure which allows each line to serve as an input, and output, or both even though outputs are statically latched. Figure 4 shows the circuit configuration in detail. Each line is continuously pulled up to V_{CC} through a resistive device of relatively high impedance.

This pullup is sufficient to provide the source current for a TTL high level yet can be pulled low by a standard TTL gate thus allowing the same pin to be used for both input and output. To provide fast switching times in a "0" to "1" transition a relatively low impedance device is switched in momentarily ($\approx$ 1/5 of a machine cycle) whenever a "1" is written to the line. When a "0" is written to the line a low impedance device overcomes the light pullup and provides TTL current sinking capability. Since the pulldown transistor is a low impedance device a "1" must first be written to any line which is to be used as an input. Reset initializes all lines to the high impedance "1" state.

It is important to note that the ORL and the ANL are read/write operations. When executed, the μC "reads" the port, modifies the data according to the instruction, then "writes" the data back to the port. The "writing" (essentially an OUTL instruction) enables the low impedance pull-up momentarily again even if the data was unchanged from a "1." This specifically applies to configurations that have inputs and outputs mixed together on the same port. See also section 8 in the Expanded MCS-48 System chapter.

BUS

Bus is also an 8-bit port which is a true bidirectional port with associated input and output strobes. If the bidirectional feature is not needed, Bus can serve as either a statically latched output port or non-latching input port. Input and output lines on this port cannot be mixed however.

As a static port, data is written and latched using the OUTL instruction and inputted using the INS instruction. The INS and OUTL instructions generate pulses on the corresponding $\overline{RD}$ and $\overline{WR}$ output strobe lines; however, in the static port mode they are generally not used. As a bidirectional port the MOVX instructions are used to read and write the port. A write to the port generates a pulse on the $\overline{WR}$ output line and output data is valid at the trailing edge of $\overline{WR}$. A read of the port generates a pulse on the $\overline{RD}$ output line and input data must be valid at the trailing edge of $\overline{RD}$. When not being written or read, the BUS lines are in a high impedance state. See also sections 7 and 8 in the Expanded MCS-48 System chapter.

2.5 Test and INT Inputs

Three pins serve as inputs and are testable with the conditional jump instruction. These are T0, T1, and $\overline{INT}$. These pins allow inputs to cause program branches without the necessity to load an input port into the accumulator. The T0, T1, and $\overline{INT}$ pins have other possible functions as well. See the pin description in Section 3.

2.6 Program Counter and Stack

The Program Counter is an independent counter while the Program Counter Stack is implemented suing pairs of registers in the Data Memory Array. Only 10, 11, or 12 bits of the Program Counter are used to address the 1024, 2048, or 4096 words of on-board program memory of the 8048AH, 8049AH, or 8050AH, while the most significant bits can be used for external Program Memory fetches. See Figure 5. The Program Counter is initialized to zero by activating the Reset line.

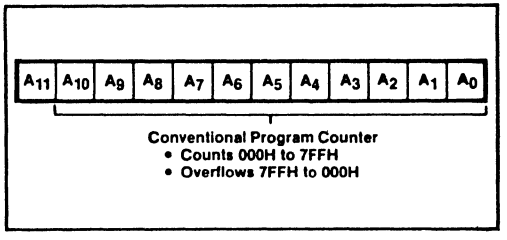


Figure 5. Program Counter

An interrupt or CALL to a subroutine causes the contents of the program counter to be stored in one of the 8 register pairs of the Program Counter Stack as shown in Figure 6. The pair to be used is determined by a 3-bit Stack Pointer which is part of the Program Status Word (PSW).

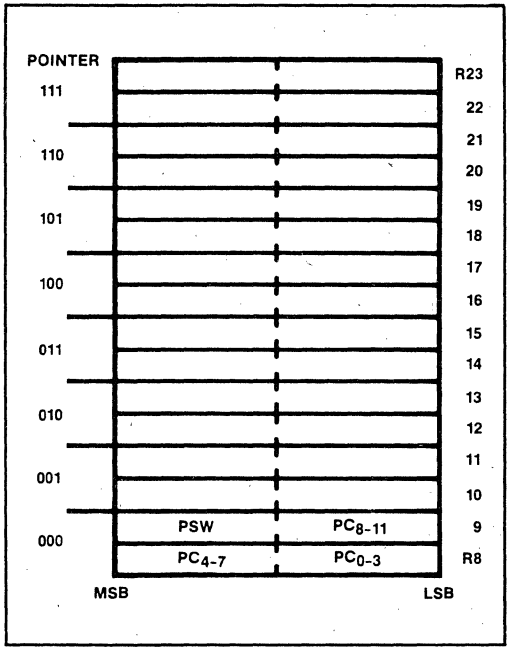


Figure 6. Program Counter Stack

Data RAM locations 8-23 are available as stack registers and are used to store the Program Counter and 4 bits of PSW as shown in Figure 6. The Stack Pointer when initialized to 000 points to RAM locations 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to locations 8 and 9 of the RAM array. The stack pointer is then incremented by one to point to locations 10 and 11 in anticipation of another CALL. Nesting of subroutines wihtin subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The end of a subroutine, which is signalled by a return instruction (RET or RETR), causes the Stack Pointer to be decremented and the contents of the resulting register pair to be transferred to the Program Counter.

2.7 Program Status Word

An 8-bit status word which can be loaded to and from the accumulator exists called the Program Status Word (PSW). Figure 7 shows the information available in the word. The Program Status Word is actually a collection of flip-flops throughout the machine which can be read or written as a whole. The ability to write to PSW allows for easy restoration of machine status after a power down sequence.

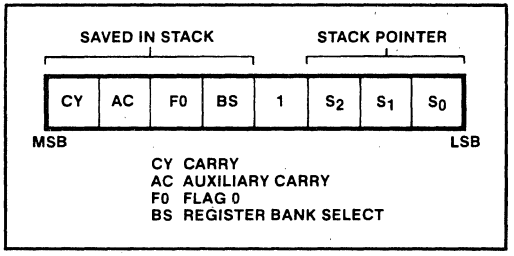


Figure 7. Program Status Word (PSW)

The upper four bits of PSW are stored in the Program Counter Stack with every call to subroutine or interrupt vector and are optionally restored upon return with the RETR instruction. The RET return instruction does not update PSW.

The PSW bit definitions are as follows:

Bits 0–2: Stack Pointer bits (S_0, S_1, S_2)

Bit 3: Not used ("1" level when read)

Bit 4: Working Register Bank Switch Bit (BS)
0 = Bank 0
1 = Bank 1

Bit 5: Flag 0 bit (F0) user controlled flag which can be complemented or cleared, and tested with the conditional jump instruction JF0.

Bit 6: Auxiliary Carry (AC) carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A.

Bit 7: Carry (CY) carry flag which indicates that the previous operation has resulted in overflow of the accumulator.

2.8 Conditional Branch Logic

The conditional branch logic within the processsor enables several conditions internal and external to the processor to be tested by the users program. By using the conditional jump instruction the conditions that are listed in Table 1 can effect a change in the sequence of the program execution.

Table 1

Device Testable	Jump Conditions (Jump On)	
		not all
Accumulator	All zeros	zeros
Accumulator Bit	—	1
Carry Flag	0	1
User Flags (F0, F1)	—	1
Timer Overflow Flag	—	1
Test Inputs (T0, T1)	0	1
Interrupt Input ($\overline{INT}$)	0	—

2.9 Interrupt

An interrupt sequence is initiated by applying a low "0" level input to the INT pin. Interrupt is level triggered and active low to allow "WIRE ORing" of several interrupt sources at the input pin. Figure 8 shows the interrupt logic of the 8048AH. The Interrupt line is sampled every instruction cycle and when detected causes a "call to subroutine" at location 3 in program memory as soon as all cycles of the current instruction are complete. On 2-cycle instructions the interrupt line is sampled on the 2nd cycle only. $\overline{INT}$ must be held low for at least 3 machine cycles to ensure proper interrupt operations. As in any CALL to subroutine, the Program Counter and Program Status word are saved in the stack. For a description of this operation see the previous section, Program Counter and Stack. Program Memory location 3 usually contains an unconditional jump to an interrupt service subroutine elsewhere in program memory. The end of an interrupt service subroutine is signalled by the execution of a Return and Restore Status instruction RETR. The interrupt system is single level in that once an interrupt is detected all further interrupt requests are ignored until execution of an RETR reenables the interrupt input logic. This occurs at the beginning of the second cycle of the RETR instruction. This sequence holds true also for an internal interrupt generated by timer overflow. If an internal timer/counter generated interrupt and an external interrupt are detected at the same time, the external source will be recognized. See the following Timer/Counter section for a description of timer interrupt. If needed, a second external interrupt can be created by enabling the timer/counter interrupt, loading FFH in the Counter (ones less than terminal count), and enabling the event counter mode. A "1" to "0" transition on the T1 input will then cause an interrupt vector to location 7.

INTERRUPT TIMING

The interrupt input may be enabled or disabled under Program Control using the EN I and DIS I instructions. Interrupts are disabled by Reset and remain so until enabled by the users program. An interrupt request must be removed before the RETR instruction is executed upon return from the service routine otherwise the processor will re-enter the service routine immediately. Many peripheral devices prevent this situation by resetting their interrupt request line whenever the processor accesses (Reads or Writes) the peripherals data buffer register. If the interrupting device does not require access by the processor, one output line of the 8048AH may be designated as an "interrupt acknowledge" which is activated by the service subroutine to reset the interrupt request. The $\overline{INT}$ pin may also be tested using the conditional jump instruction JNI. This instruction may be used to detect the presence of a pending interrupt before interrupts are enabled. If interrupt is left disabled, $\overline{INT}$ may be used as another test input like T0 and T1.

2.10 Timer/Counter

The 8048AH contains a counter to aid the user in counting external events and generating accurate time delays without placing a burden on the processor for these functions. In both modes the counter operation is the same, the only difference being the source of the input to the counter. The timer/event counter is shown in Figure 9.

COUNTER

The 8-bit binary counter is presettable and readable with two MOV instructions which transfer the contents of the accumulator to the counter and vice versa. The counter content may be affected by Reset and should be initialized by software. The counter is stopped by a Reset or STOP TCNT instruction and remains stopped until started as a timer by a START T instruction or as an event counter by a START CNT instruction. Once started the counter will increment to this maximum count (FF) and overflow to zero continuing its count until stopped by a STOP TCNT instruction or Reset.

The increment from maximum count to zero (overflow) results in the setting of an overflow flag flip-flop and in the generation of an interrupt request. The state of the overflow flag is testable with the conditional jump instruction JTF. The flag is reset by executing a JTF or by Reset. The interrupt request is stored in a latch and then ORed with the external interrupt input INT. The timer interrupt may be enabled or disabled independently of external interrupt by the EN TCNTI and DIS TCNTI instructions. If enabled, the counter overflow will cause a subroutine call to location 7 where the timer or counter service routine may be stored.

If timer and external interrupts occur simultaneously, the external source will be recognized and the Call will be to

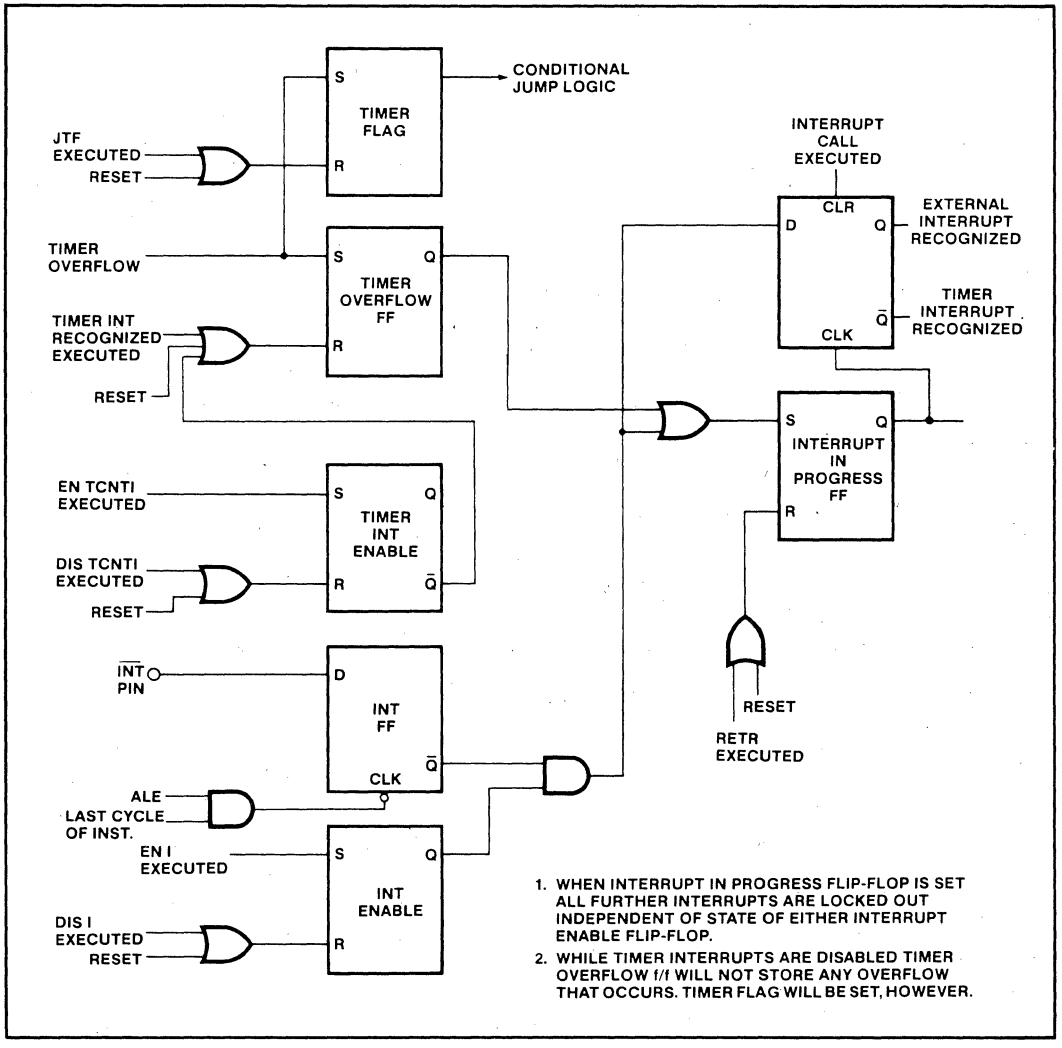


Figure 8. Interrupt Logic

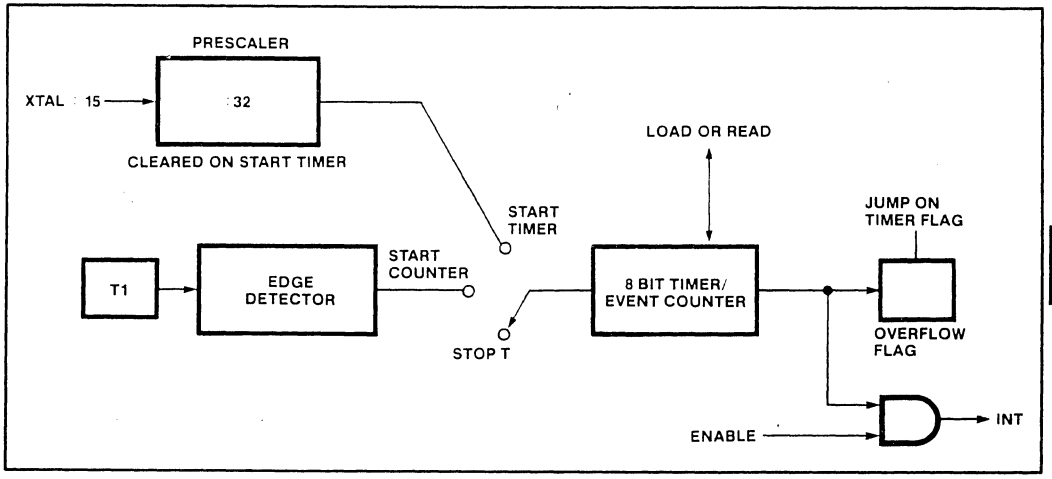


Figure 9. Timer/Event Counter

location 3. Since the timer interrupt is latched it will remain pending until the external device is serviced and immediately be recognized upon return from the service routine. The pending timer interrupt is reset by the Call to location 7 or may be removed by executing a DIS TCNT1 instruction.

AS AN EVENT COUNTER

Execution of a START CNT instruction connects the T1 input pin to the counter input and enables the counter. The T1 input is sampled at the beginning of state 3 or in later MCS-48 devices in state time 4. Subsequent high to low transitions on T1 will cause the counter to increment. T1 must be held low for at least 1 machine cycle to insure it won't be missed. The maximum rate at which the counter may be incremented is once per three instruction cycles (every 5.7 μsec when using an 8 MHz crystal) — there is no minimum frequency. T1 input must remain high for at least 1/5 machine cycle after each transition.

AS A TIMER

Eexcution of a START T instruction connects an internal clock to the counter input and enables the counter. The internal clock is derived bypassing the basic machine cycle clock through a ÷32 prescaler. The prescaler is reset during the START T instruction. The resulting clock increments the counter every 32 machine cycles. Various delays from 1 to 256 counts can be obtained by presetting the counter and detecting overflow. Times longer than 256 counts may be achieved by accumulating multiple overflows in a register under software control. For time resolution less than 1 count an external clock can be applied to the T1 input and the counter operated in the event counter mode. ALE divided by 3 or more can serve as this external clock. Very small delays or "fine tuning" of larger delays can be easily accomplished by software delay loops.

Often a serial link is desirable in an MCS-48 family member. Table 2 lists the timer counts and cycles needed for a specific baud rate given a crystal frequency.

2.11 Clock and Timing Circuits

Timing generation for the 8048AH is completely selfcontained with the exeception of a frequency reference which can be XTAL, ceramic resonator, or external clock source. The Clock and Timing circuitry can be divided into the following functional blocks.

OSCILLATOR

The on-board oscillator is a high gain parallel resonant circuit with a frequency range of 1 to 11 MHz. The X1 external pin is the input to the amplifier stage while X2 is the output. A crystal or ceramic resonator connected between X1 and X2 provides the feedback and phase shift required for oscillation. If an accurate frequency reference is not required, ceramic resonator may be used in place of the crystal.

For accurate clocking, a crystal should be used. An externally generated clock may also be applied to X1–X2 as the frequency source. See the data sheet for more information.

Table 2. Baud Rate Generation

	Frequency (MHz)	T_{cy}	T0 Prr(1/5 T_{cy})	Timer Prescaler (32 T_{cy})
	4	3.75μs	750ns	120μs
	6	2.50μs	500ns	80μs
	8	1.88μs	375ns	60.2μs
	11	1.36μs	275ns	43.5μs
Baud Rate	4 MHz Timer Counts + Instr. Cycles	6 MHz Timer Counts + Instr. Cycles	8 MHz Timer Counts + Instr. Cycles	11 MHz Timer Counts + Instr. Cycles
110	75 + 24 Cycles .01% Error	113 + 20 Cycles .01% Error	151 + 3 Cycles .01% Error	208 + 28 Cycles .01% Error
300	27 + 24 Cycles .1% Error	41 + 21 Cycles .03% Error	55 + 13 Cycles .01% Error	76 + 18 Cycles .04% Error
1200	6 + 30 Cycles .1% Error	10 + 13 Cycles .1% Error	12 + 27 Cycles .06% Error	19 + 4 Cycles .12% Error
1800	4 + 20 Cycles .1% Error	6 + 30 Cycles .1% Error	9 + 7 Cycles .17% Error	12 + 24 Cycles .12% Error
2400	3 + 15 Cycles .1% Error	5 + 6 Cycles .4% Error	6 + 24 Cycles .29% Error	9 + 18 Cycles .12% Error
4800	1 + 23 Cycles 1.0% Error	2 + 19 Cycles .4% Error	3 + 14 Cycles .74% Error	4 + 25 Cycles .12% Error

STATE COUNTER

The output of the oscillator is divided by 3 in the State Counter to create a clock which defines the state times of the machine (CLK). CLK can be made available on the external pin T0 by executing an ENTO CLK instruction. The output of CLK on T0 is disabled by Reset of the processor.

CYCLE COUNTER

CLK is then divided by 5 in the Cycle Counter to provide a clock which defines a machine cycle consisting of 5 machine states as shown in Figure 10. Figure 11 shows the different internal operations as divided into the machine states. This clock is called Address Latch Enable (ALE) because of its function in MCS-48 systems with external memory. It is provided continuously on the ALE output pin.

2.12 Reset

The reset input provides a means for initialization for the processor. This Schmitt-trigger input has an internal pull-up device which in combination with an external 1 μ fd capacitor provides an internal reset pulse of sufficient length to guarantee all circuitry is reset, as shown in Figure 12. If the reset pulse is generated externally the RESET pin must be held low for at least 10 milliseconds after the power supply is within tolerance. Only 5 machine cycles (6.8 μs @ 11 MHz) are required if power is already on and the oscillator has stabilized. ALE and PSEN (if EA = 1) are active while in Reset.

Reset performs the following functions:

1) Sets program counter to zero.
2) Sets stack pointer to zero.
3) Selects register bank 0.
4) Selects memory bank 0.
5) Sets BUS to high impedance state (except when EA = 5V).
6) Sets Ports 1 and 2 to input mode.
7) Disables interrupts (timer and external).
8) Stops timer.
9) Clears timer flag.
10) Clears F0 and F1.
11) Disables clock output from T0.

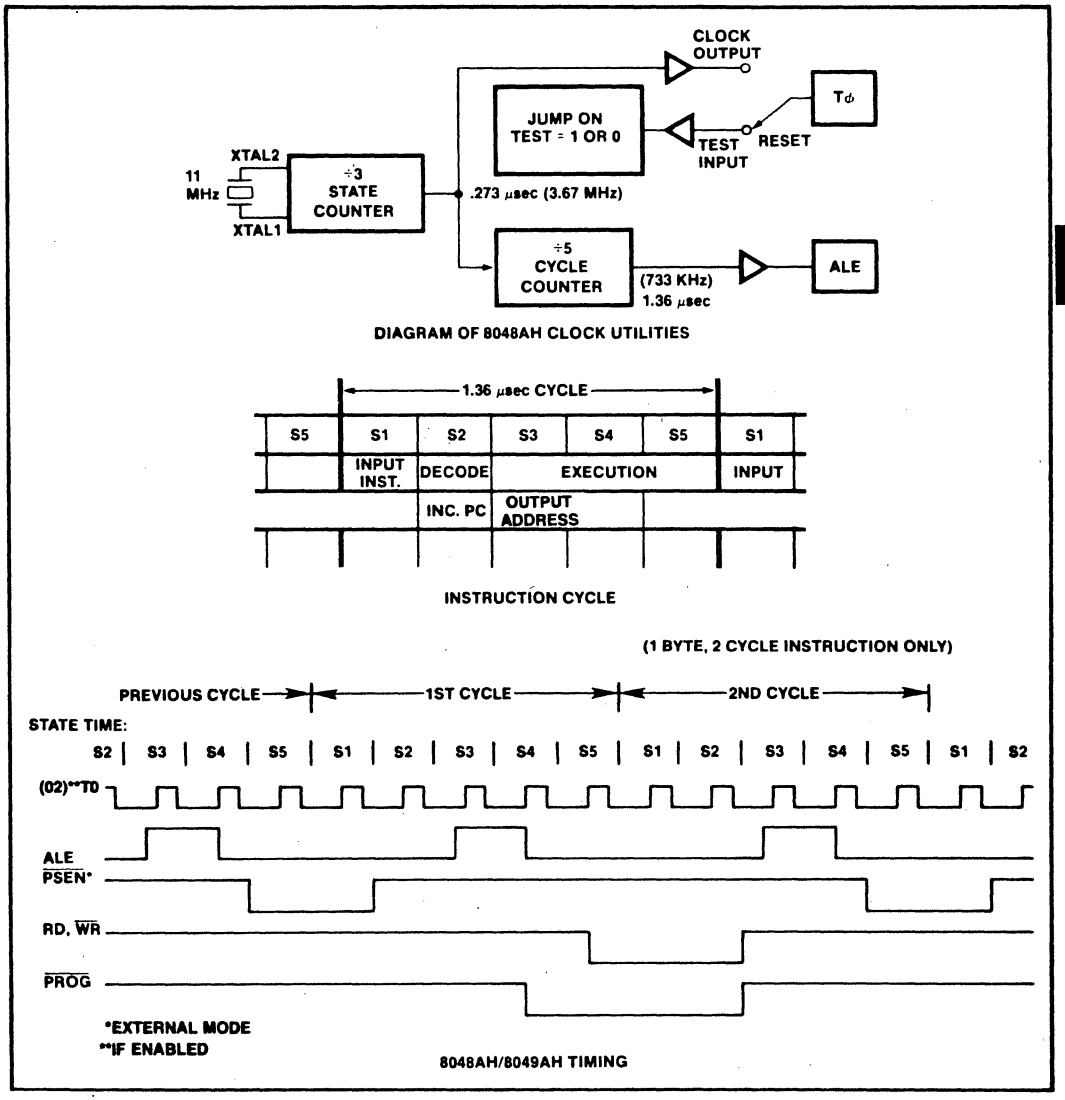


Figure 10. MCS®-48 Timing Generation and Cycle Timing

2.13 Single-Step

This feature, as pictured in Figure 13, provides the user with a debug capability in that the processor can be stepped through the program one instruction at a time. While stopped, the address of the next instruction to be fetched is available concurrently on BUS and the lower half of Port 2. The user can therefore follow the program through each of the instruction steps. A timing diagram, showing the interaction between output ALE and input $\overline{SS}$, is shown. The BUS buffer contents are lost during single step; however, a latch may be added to reestablish the lost I/O capability if needed. Data is valid at the leading edge of ALE.

	CYCLE 1					CYCLE 2				
INSTRUCTION	S1	S2	S3	S4	S5	S1	S2	S3	S4	S5
IN A,P	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	*INCREMENT TIMER	—	—	READ PORT	—	* —	—
OUTL P,A	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	*INCREMENT TIMER	OUTPUT TO PORT	—	—	—	* —	—
ANL P, = DATA	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	*INCREMENT TIMER	READ PORT	FETCH IMMEDIATE DATA	—	INCREMENT PROGRAM COUNTER	*OUTPUT TO PORT	—
ORL P, = DATA	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	*INCREMENT TIMER	READ PORT	FETCH IMMEDIATE DATA	—	INCREMENT PROGRAM COUNTER	*OUTPUT TO PORT	—
INS A, BUS	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	INCREMENT TIMER	—	—	READ PORT	—	* —	—
OUTL BUS, A	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	INCREMENT TIMER	OUTPUT TO PORT	—	—	—	* —	—
ANL BUS, = DATA	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	*INCREMENT TIMER	READ PORT	FETCH IMMEDIATE DATA	—	INCREMENT PROGRAM COUNTER	*OUTPUT TO PORT	—
ORL BUS, = DATA	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	*INCREMENT TIMER	READ PORT	FETCH IMMEDIATE DATA	—	INCREMENT PROGRAM COUNTER	*OUTPUT TO PORT	—
MOVX @ R,A	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	OUTPUT RAM ADDRESS	INCREMENT TIMER	OUTPUT DATA TO RAM	—	—	—	* —	—
MOVX A,@R	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	OUTPUT RAM ADDRESS	INCREMENT TIMER	—	—	READ DATA	—	* —	—
MOVD A,P_i	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	OUTPUT OPCODE/ADDRESS	INCREMENT TIMER	—	—	READ P2 LOWER	—	* —	—
MOVD P_i,A	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	OUTPUT OPCODE/ADDRESS	INCREMENT TIMER	OUTPUT DATA TO P2 LOWER	—	—	—	* —	—
ANLD P,A	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	OUTPUT OPCODE/ADDRESS	INCREMENT TIMER	OUTPUT DATA	—	—	—	* —	—
ORLD P,A	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	OUTPUT OPCODE/ADDRESS	INCREMENT TIMER	OUTPUT DATA	—	—	—	* —	—
J(CONDITIONAL)	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	SAMPLE CONDITION	*INCREMENT SAMPLE	—	FETCH IMMEDIATE DATA	—	UPDATE PROGRAM COUNTER	* —	—
STRT T STRT CNT	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	* —	START COUNTER					
STOP TCNT	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	* —	STOP COUNTER					
ENI	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	* ENABLE INTERRUPT	—					
DIS I	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER	—	* DISABLE INTERRUPT	—					
ENTO CLK	FETCH INSTRUCTION	INCREMENT PROGRAM COUNTER		* ENABLE CLOCK	—					

*VALID INSTRUCTION ADDRESSES ARE OUTPUT AT THIS TIME IF EXTERNAL PROGRAM MEMORY IS BEING ACCESSED.

(1) IN LATER MCS-48 DEVICES T1 IS SAMPLED IN S4.

Figure 11. 8048AH/8049AH Instruction Timing Diagram

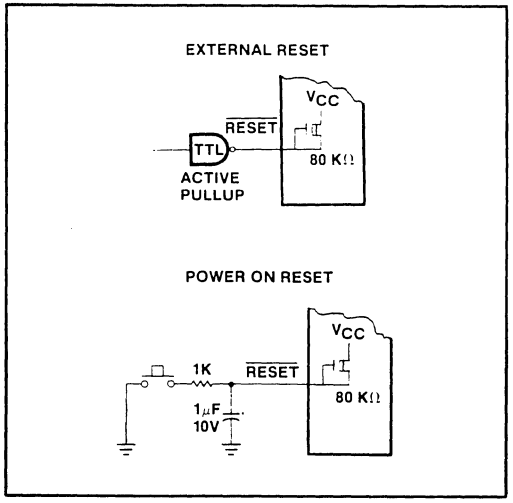


Figure 12.

TIMING

The 8048AH operates in a single-step mode as follows:

1) The processor is requested to stop by applying a low level on $\overline{SS}$.
2) The processor responds by stopping during the address fetch portion of the next instruction. If a double cycle instruction is in progress when the single step command is received, both cycles will be completed before stopping.
3) The processor acknowledges it has entered the stopped state by raising ALE high. In this state (which can be maintained indefinitely) the address of the next instruction to be fetched is present on BUS and the lower half of port 2.
4) $\overline{SS}$ is then raised high to bring the processor out of the stopped mode allowing it to fetch the next instruction. The exit from stop is indicated by the processor bringing ALE low.
5) To stop the processor at the next instruction $\overline{SS}$ must be brought low again soon after ALE goes low. If $\overline{SS}$ is left high the processor remains in a "Run" mode.

A diagram for implementing the single-step function of the 8748H is shown in Figure 13. D-type flip-flop with preset and clear is used to generate $\overline{SS}$. In the run mode SS is held high by keeping the flip-flop preset (preset has precedence over the clear input). To enter single step, preset is removed allowing ALE to bring $\overline{SS}$ low via the clear input. ALE should be buffered since the clear input of an SN7474 is the equivalent of 3 TTL loads. The processor is now in the stopped state. The next instruction is initiated by clocking a "1" into the flip-flop. This "1" will not appear on $\overline{SS}$ unless ALE is high removing clear from the flip-flop. In response to $\overline{SS}$ going high the processor begins an instruction fetch which brings ALE low resetting $\overline{SS}$ through the clear input and causing the processor to again enter the stopped state.

2.14 Power Down Mode (8048AH, 8049AH, 8050AH, 8039AHL, 8035AHL, 8040AHL)

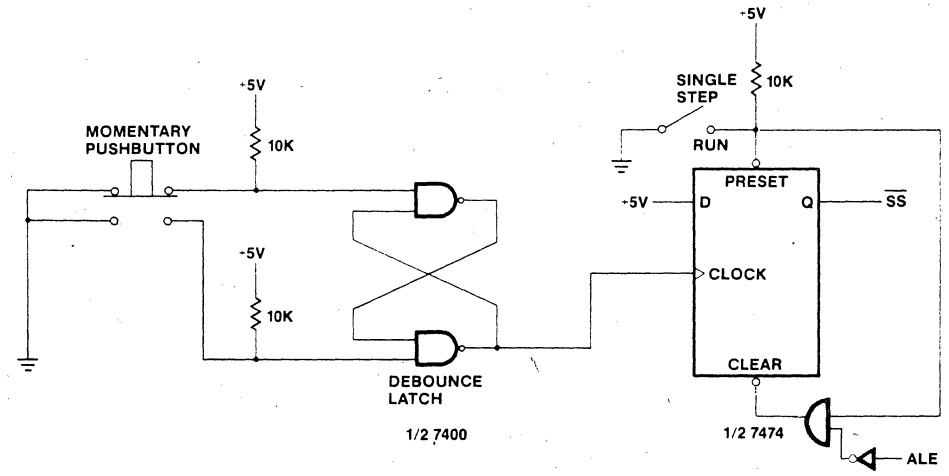
Extra circuitry has been added to the 8048AH/8049AH/8050AH ROM version to allow power to be removed from all but the data RAM array for low power standby operation. In the power down mode the contents of data RAM can be maintained while drawing typically 10% to 15% of normal operating power requirements.

V_{CC} serves as the 5V supply pin for the bulk of circuitry while the V_{DD} pin supplies only the RAM array. In normal operation both pins are a 5V while in standby, V_{CC} is at ground and V_{DD} is maintained at its standby value. Applying Reset to the processor through the $\overline{RESET}$ pin inhibits any access to the RAM by the processor and guarantees that RAM cannot be inadvertently altered as power is removed from V_{CC}.

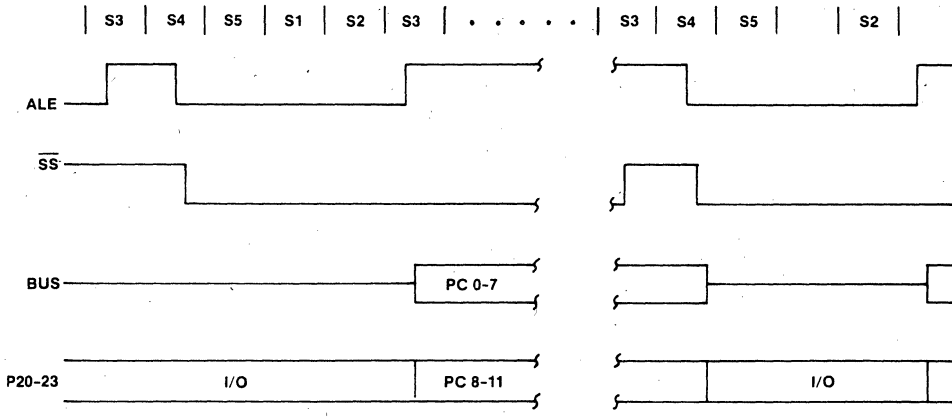
A typical power down sequence (Figure 14) occurs as follows:

1) Imminent power supply failure is detected by user defined circuitry. Signal must be early enough to allow 8048AH to save all necessary data before V_{CC} falls below normal operating limits.
2) Power fail signal is used to interrupt processor and vector it to a power fail service routine.
3) Power fail routine saves all important data and machine status in the internal data RAM array. Routine may also initiate transfer of backup supply to the V_{DD} pin and indicate to external circuitry that power fail routine is complete.
4) Reset is applied to guarantee data will not be altered as the power supply falls out of limits. Reset must be held low until V_{CC} is at ground level.

Recovery from the Power Down mode can occur as any other power-on sequence with an external capacitor on the Reset input providing the necessary delay. See the previous section on Reset.



SINGLE STEP CIRCUIT



SINGLE STEP TIMING

Figure 13. Single Step Operation

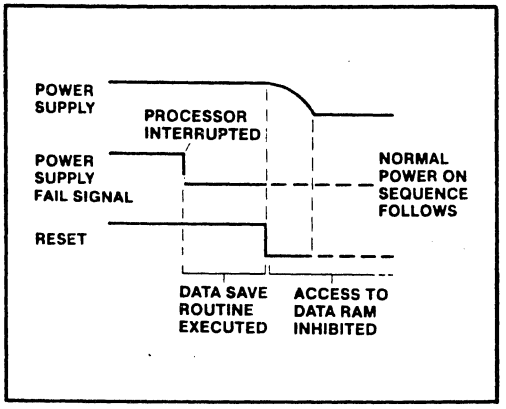


Figure 14. Power Down Sequence

2.15 External Access Mode

Normally the first 1K (8048AH), 2K (8049AH), or 4K (8050AH) words of program memory are automatically fetched from internal ROM or EPROM. The EA input pin however allows the user to effectively disable internal program memory by forcing all program memory fetches to reference external memory. The following chapter explains how access to external program memory is accomplished.

The External Access mode is very useful in system test and debug because it allows the user to disable his internal applications program and substitute an external program of his choice — a diagnostic routine for instance. In addition, the date sheet shows how internal program memory can be read externally, independent of the processor. A "1" level on EA initiates the external accesss mode. For proper operation, Reset should be applied while the EA input is changed.

2.16 Sync Mode

The 8048AH, 8049AH, 8050AH has incorporated a new SYNC mode. The Sync mode is provided to ease the design of multiple controller circuits by allowing the designer to force the device into known phase and state time. The SYNC mode may also be utilized by automatic test equipment (ATE) for quick, easy, and efficient synchronizing between the tester and the DUT (device under test).

SYNC mode is enabled when SS' pin is raised to high voltage level of +12 volts. To begin synchronization, T0 is raised to 5 volts at least four clocks cycles after SS'. T0 must be high for at least four X1 clock cycles to fully reset the prescaler and time state generators. T0 may then be brought down with the rising edge of X1. Two clock cycles later, with the rising edge of X1, the device enters into Time State 1, Phase 1, SS' is then brought down to 5 volts 4 clocks later after T0. RESET' is allowed to go high 5 tCY (75 clocks) later for normal execution of code. See Figure 15.

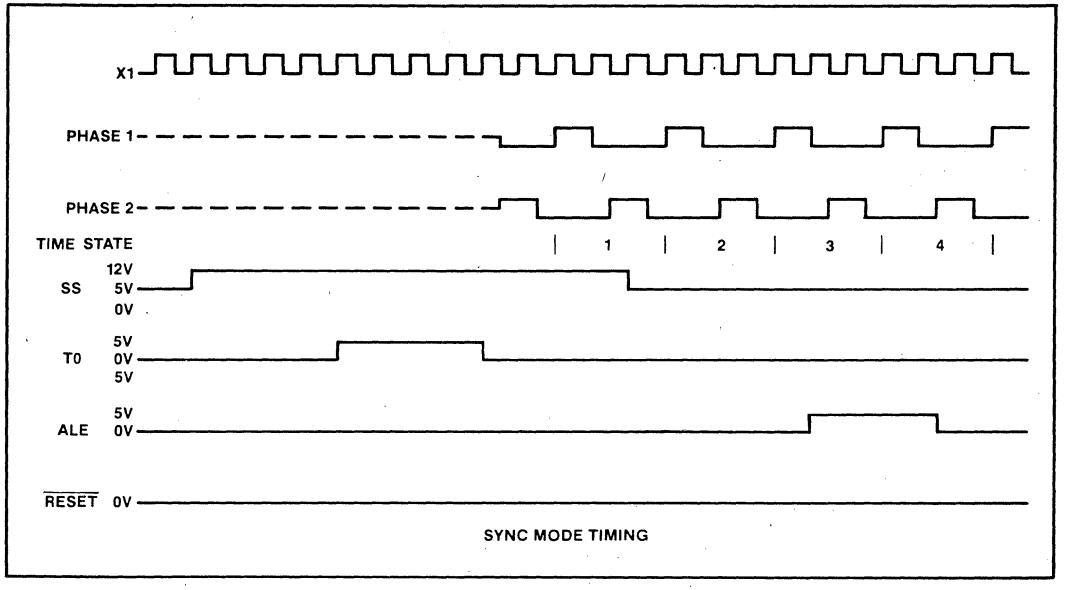


Figure 15. Sync Mode Timing

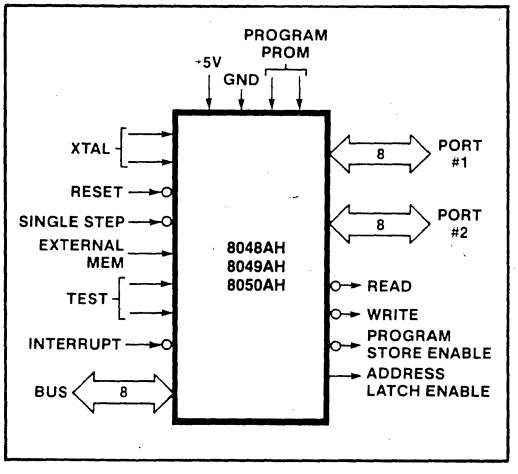


Figure 16. 8048AH and 8049AH Logic Symbol

3.0 PIN DESCRIPTION

The MCS-48 processors are packaged in 40 pin Dual In-Line Packages (DIP's). Table 3 is a summary of the functions of each pin. Figure 16 is the logic symbol for the 8048AH product family. Where it exists, the second paragraph describes each pin's function in an expanded MCS-48 system. Unless otherwise specified, each input is TTL compatible and each output will drive one standard TTL load.

Table 3. Pin Description

Designation	Pin Number*	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; 21V during program for the 8748H/8749H; +5V during operation for both ROM and EPROM. Low power standby pin in 8048AH and 8049AH/8050AH ROM versions.
V_{CC}	40	Main power supply; +5V during operation and during 8748H and 8749H programming.
PROG	25	Program pulse; +18V input pin during 8748H, 8749H programming. Output strobe for 8243 I/O expander.
P10-P17 (Port 1)	27-34	8-bit quasi-bidirectional port. (Internal Pullup ≈ 50KΩ)
P20-P27 (Port 2)	21-24 35-38	8-bit quasi-bidirectional port. (Internal Pullup ≈ 50KΩ) P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
D0-D7 (BUS)	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENTO CLK instruction. T0 is also used during programming and sync mode.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the event counter input using the STRT CNT instruction. (See Section 2.10).
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. (Active low) Interrupt must remain low for at least 3 machine cycles to ensure proper operation.
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. (Active low) Used as a Read Strobe to External Data Memory.
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during EPROM programming and verification. (Active low) (Internal pullup ≈ 80K Ω)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low) Used as write strobe to external data memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

Table 3. Pin Description (Continued)

Designation	Pin Number*	Function
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low) (Internal pullup ≈ 300KΩ) +12V for sync modes (See 2.16).
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high) +12V for 8048AH 8049AH 8050AH program verification and +18V for 8748H 8749H program verification (Internal pullup ≈ 10MΩ on 8048AH 8049AH 8035AHL 8039AHL 8050AH 8040AHL)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source.
XTAL2	3	Other side of crystal external source input.

*Unless otherwise stated, inputs do not have internal pullup resistors. 8048AH, 8748H, 8049AH, 8050AH, 8040AHL

4.0 PROGRAMMING, VERIFYING AND ERASING EPROM

The internal Program Memory of the 8748H and the 8749H may be erased and reprogrammed by the user as explained in the following sections. See also the 8748H and 8749H data sheets.

4.1 Programming/Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. This programming algorithm applies to both the 8748H and 8749H. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a descsription of their functions:

Pin	Function
XTAL 1	Clock Input (3 to 4 MHz)
Reset	Initialization and Address Latching
Test 0	Selection of Program (0V) or Verify (5V) Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output During Verify
P20-1	Address Input for 8748H
P20-2	Address Input for 8749H
V_{DD}	Programming Power Supply
PROG	Program Pulse Input
P10–P11	Tied to ground (8749H only)

8748H AND 8749H ERASURE CHARACTERISTICS

The erasure characteristics of the 8748H and 8749H are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000A range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8748H and 8749H in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8748H or 8749H is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the 8748H window to prevent unintentional erasure.

When erased, bits of the 8748H and 8749H Program Memory are in the logic "0" state.

The recommended erasure procedure for the 8748H and 8749H is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8748H and 8749H should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter in their tubes and this filter should be removed before erasure.

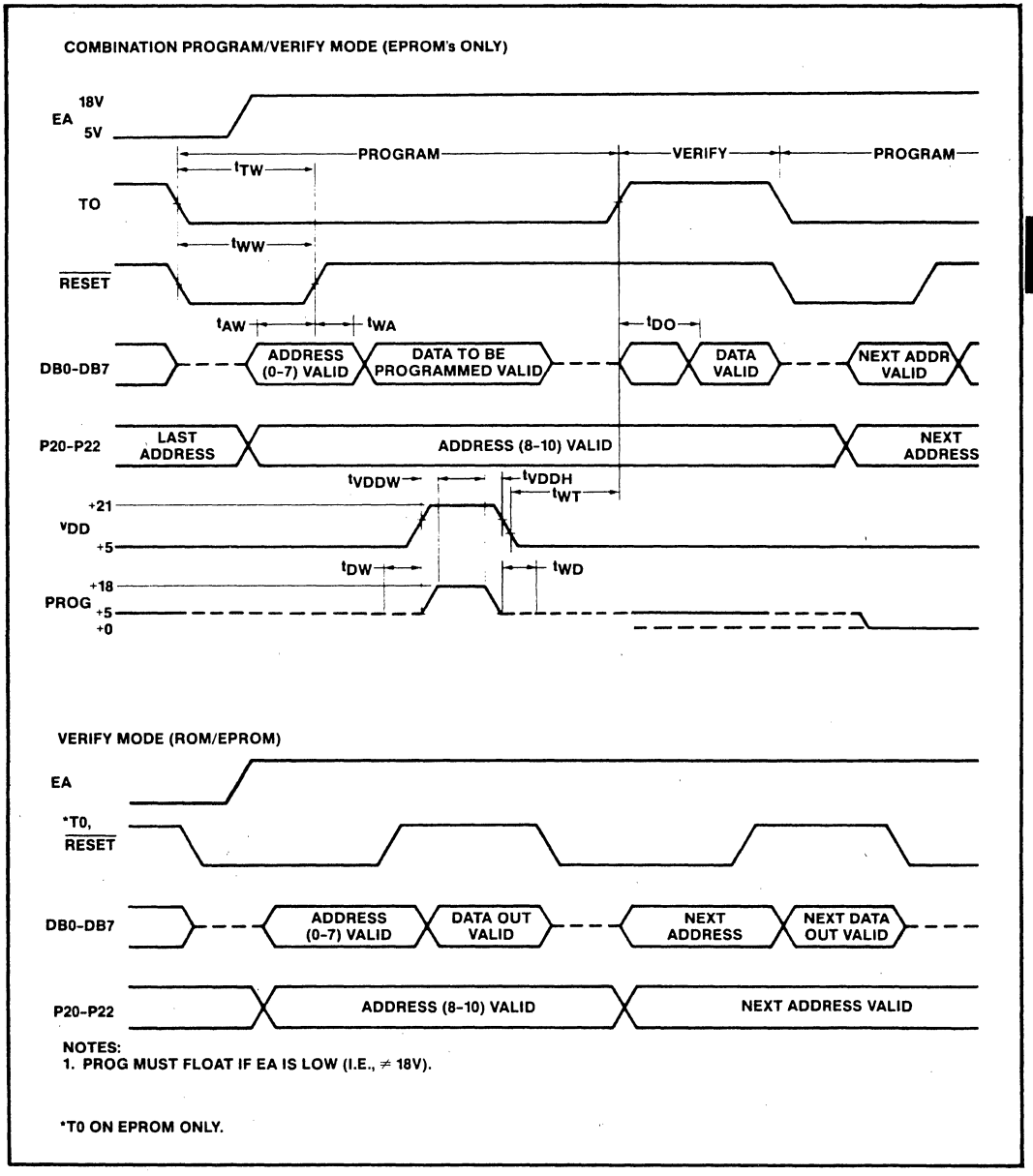


Figure 17. Program/Verify Sequence for 8749H/8748H

MCS®-48 Expanded System

2

EXPANDED MCS®-48 SYSTEM

1.0 INTRODUCTION

If the capabilities resident on the single-chip 8048AH/8748H/8035AHL/8049AH/8749H/8039AHL are not sufficient for your system requirements, special on-board circuitry allows the addition of a wide variety of external memory, I/O, or special peripherals you may require. The processors can be directly and simply expanded in the following areas:

- Program Memory to 4K words
- Data Memory to 320 words (384 words with 8049AH)
- I/O by unlimited amount
- Special Functions using 8080/8085AH peripherals

By using bank switching techniques, maximum capability is essentially unlimited. Bank switching is discussed later in the chapter. Expansion is accomplished in two ways:

1) Expander I/O — A special I/O Expander circuit, the 8243, provides for the addition of four 4-bit Input/Output ports with the sacrifice of only the lower half (4-bits) of port 2 for inter-device communication. Multiple 8243's may be added to this 4-bit bus by generating the required "chip select" lines.
2) Standard 8085 Bus — One port of the 8048AH/8049AH is like the 8-bit bidirectional data bus of the 8085 microcomputer system allowing interface to the numerous standard memories and peripherals of the MCS®-80/85 microcomputer family.

MCS-48 systems can be configured using either or both of these expansion features to optimize system capabilities to the application.

Both expander devices and standard memories and peripherals can be added in virtually any number and combination required.

2.0 EXPANSION OF PROGRAM MEMORY

Program Memory is expanded beyond the resident 1K or 2K words by using the 8085 BUS feature of the MCS®-48. All program memory fetches from the addresses less than 1024 on the 8048AH and less than 2048 on the 8049AH occur internally with no external signals being generated (except ALE which is always present). At address 1024 on the 8048AH, the processor automatically initiates external program memory fetches.

2.1 Instruction Fetch Cycle (External)

As shown in Figure 1, for all instruction fetches from addresses of 1024 (2048) or greater, the following will occur:

1) The contents of the 12-bit program counter will be output on BUS and the lower half of port 2.
2) Address Latch Enable (ALE) will indicate the time at which address is valid. The trailing edge of ALE is used to latch the address externally.
3) Program Store Enable ($\overline{PSEN}$) indicates that an external instruction fetch is in progress and serves to enable the external memory device.
4) BUS reverts to input (floating) mode and the processor accepts its 8-bit contents as an instruction word.

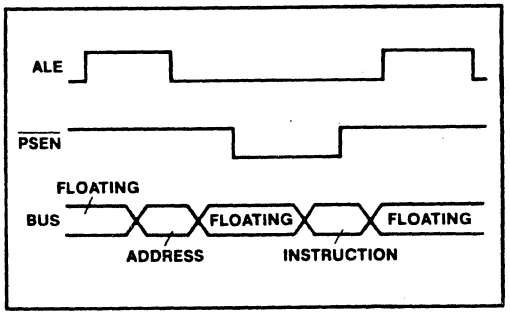


Figure 1. Instruction Fetch from External Program Memory

All instruction fetches, including internal addresses, can be forced to be external by activating the EA pin of the 8048AH/8049AH/8050AH. The 8035AHL/8039AHL/8040AHL processors without program memory always operate in the external program memory mode (EA = 5V).

2.2 Extended Program Memory Addressing (Beyond 2K)

For programs of 2K words or less, the 8048AH/8049AH addresses program memory in the conventional manner. Addresses beyond 2047 can be reached by executing a program memory bank switch instruction (SEL MB0, SEL MB1) followed by a branch instruction (JMP or CALL). The bank switch feature extends the range of branch instructions beyond their normal 2K range and at the same time prevents the user from inadvertently crossing the 2K boundary.

PROGRAM MEMORY BANK SWITCH

The switching of 2K program memory banks is accomplished by directly setting or resetting the most significant bit of the program counter (bit 11); see Figure 2. Bit 11 is not altered by normal incrementing of the program counter but is loaded with the contents of a special flip-flop each time a JMP or CALL instruction is executed. This special flip-flop is set by executing an SEL MB1

instruction and reset by SEL MB0. Therefore, the SEL MB instruction may be executed at any time prior to the actual bank switch which occurs during the next branch instruction encountered. Since all twelve bits of the program counter, including bit 11, are stored in the stack, when a Call is executed, the user may jump to subroutines across the 2K boundary and the proper bank will be restored upon return. However, the bank switch flip-flop will not be altered on return.

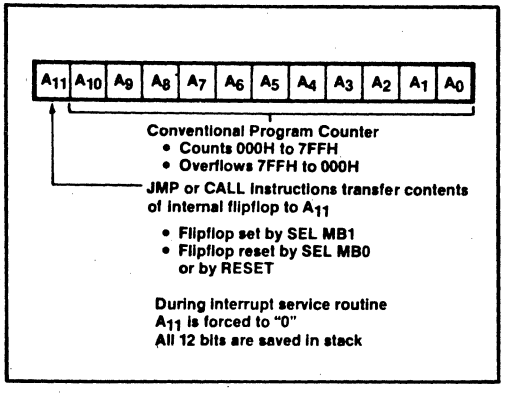


Figure 2. Program Counter

INTERRUPT ROUTINES

Interrupts always vector the program counter to location 3 or 7 in the first 2K bank, and bit 11 of the program counter is held at "0" during the interrupt service routine. The end of the service routine is signalled by the execution of an RETR instruction. Interrupt service routines should therefore be contained entirely in the lower 2K words of program memory. The execution of a SEL MB0 or SEL MB1 instruction within an interrupt routine is not recommended since it will not alter PC11 while in the routine, but will change the internal flip-flop.

2.3 Restoring I/O Port Information

Although the lower half of Port 2 is used to output the four most significant bits of address during an external program memory fetch, the I/O information is still outputed during certain portions of each machine cycle. I/O information is always present on Port 2's lower 4 bits at the rising edge of ALE and can be sampled or latched at this time.

2.4 Expansion Examples

Shown in Figure 3 is the addition of 2K words of program memory using an 2716A 2K x 8 ROM to give a total of 3K words of program memory. In this case no chip select decoding is required and $\overline{PSEN}$ enables the memory directly through the chip select input. If the system requires only 2K of program memory, the same configuration can be used with an 8035AHL substituted for the 8048AH. The 8049AH would provide 4K of program memory with the same configuration.

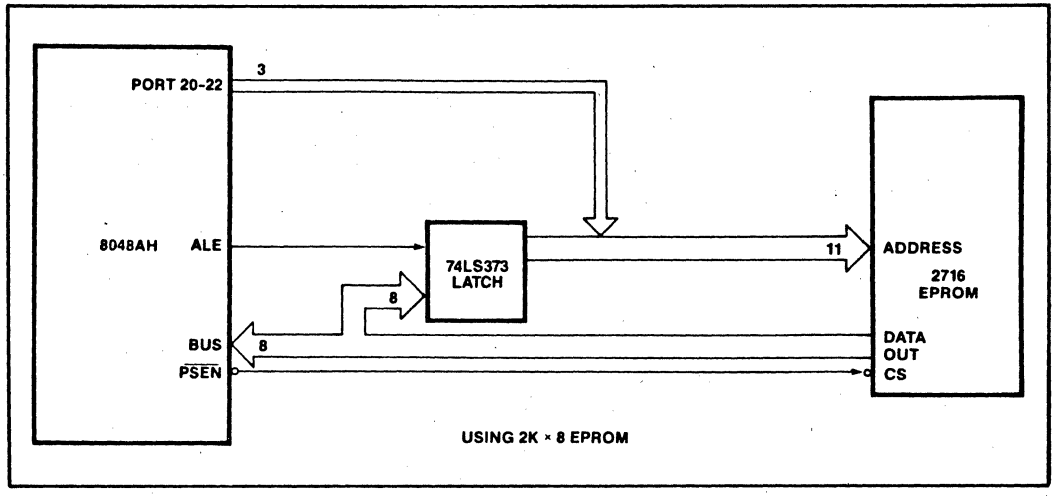


Figure 3. Expanding MCS®-48 Program Memory Using Standard Memory Products

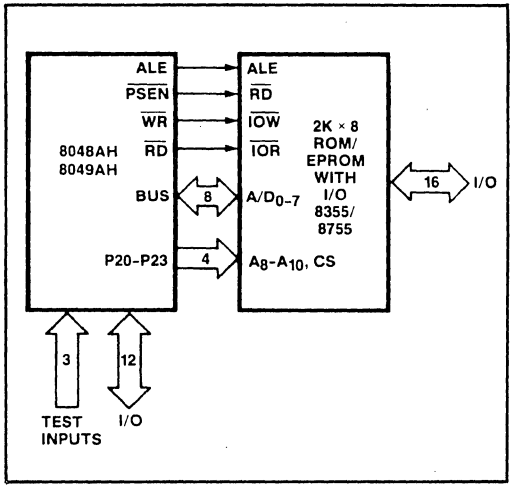


Figure 4. External Program Memory Interface

Figure 4 shows how the 8755/8355 EPROM/ROM with I/O interfaces directly to the 8048AH without the need for an address latch. The 8755/8355 contains an internal 8-bit address latch eliminating the need for an 8212 latch. In addition to a 2K x 8 program memory, the 8755/8355 also contains 16 I/O lines addressable as two 8-bit ports. These ports are addressed as external RAM; therefore the $\overline{RD}$ and $\overline{WR}$ outputs of the 8048AH are required. See the following section on data memory expansion for more detail. The subsequent section on I/O expansion explains the operation of the 16 I/O lines.

3.0 EXPANSION OF DATA MEMORY

Data Memory is expanded beyond the resident 64 words by using the 8085AH type bus feature of the MCS®-48.

2

3.1 Read/Write Cycle

All address and data is transferred over the 8 lines of BUS. As shown in Figure 5, a read or write cycle occurs as follows:

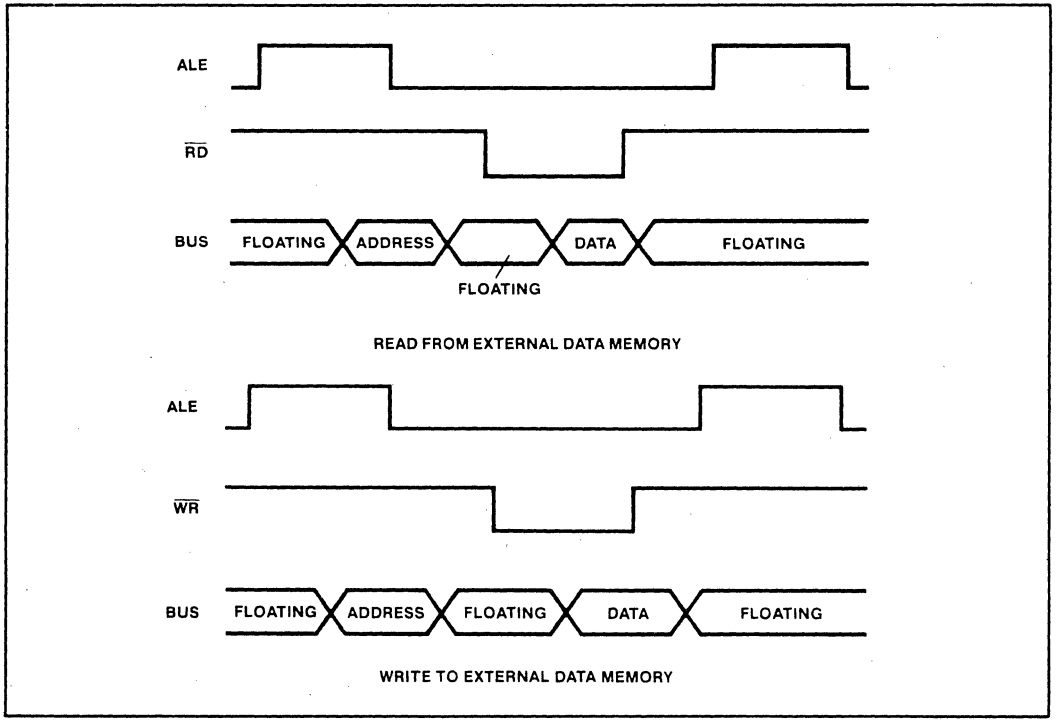


Figure 5. External Data Memory Timings

1) The contents of register R0 or R1 is outputed on BUS.
2) Address Latch Enable (ALE) indicates addresss is valid. The trailing edge of ALE is used to latch the address externally.
3) A read ($\overline{RD}$) or write ($\overline{WR}$) pulse on the corresponding output pins of the 8048AH indicates the type of data memory access in progress. Output data is valid at the trailing edge of $\overline{WR}$ and input data must be valid at the trailing edge of $\overline{RD}$.
4) Dat (8 bits) is transferred in or out over BUS.

3.2 Addressing External Data Memory

External Data Memory is accessed with its own two-cycle move instructions. MOVXA, @R and MOVX@R, A, which transfer 8 bits of data between the accumulator and the external memory location addressed by the contents of one of the RAM Pointer Registers R0 and R1. This allows 256 locations to be addressed in addition to the resident locations. Additional pages may be added by "bank switching" with extra output lines of the 8048AH.

3.3 Examples of Data Memory Expansion

Figure 6 shows how the 8048-AH can be expanded using the 8155 memory and I/O expanding device. Since the 8155 has an internal 8-bit address latch, it can interface directly to the 8048AH without the use of an external latch. The 8155 provides an additional 256 words of static data memory and also includes 22 I/O lines and a 14-bit timer. See the following section on I/O expansion and the 8155 data sheet for more details on these additional features.

4.0 EXPANSION OF INPUT/OUTPUT

There are four possible modes of I/O expansion with the 8048AH: one using a special low-cost expander, the 8243; another using standard MCS-80/85 I/O devices; and a third using the combination memory I/O expander devices the 8155, 8355, and 8755. It is also possible to expand using standard TTL devices.

4.1 I/O Expander Device

The most efficient means of I/O expansion for small systems is the 8243 I/O Expander Device which requires only 4 port lines (lower half of Port 2) for communication with the 8048AH. The 8243 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports #4–7 (see Figure 13-7). The following operations may be performed on these ports:

- Transfer Accumulator to Port
- Transfer Port to Accumulator
- AND Accumulator to Port
- OR Accumulator to Port

A 4-bit transfer from a port to the lower half of the Accumulator sets the most significant four bits to zero. All communication between the 8048AH and the 8243 occurs over Port 2 lower (P20–P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles: The first containing the "op code" and port address, and the second containing the actual 4 bits of data.

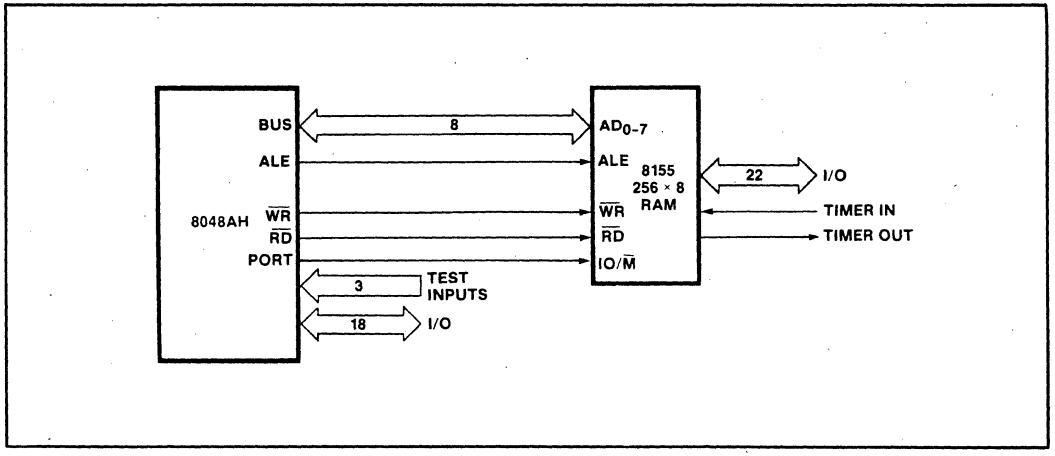


Figure 6. 8048AH Interface to 256 x 8 Standard Memories

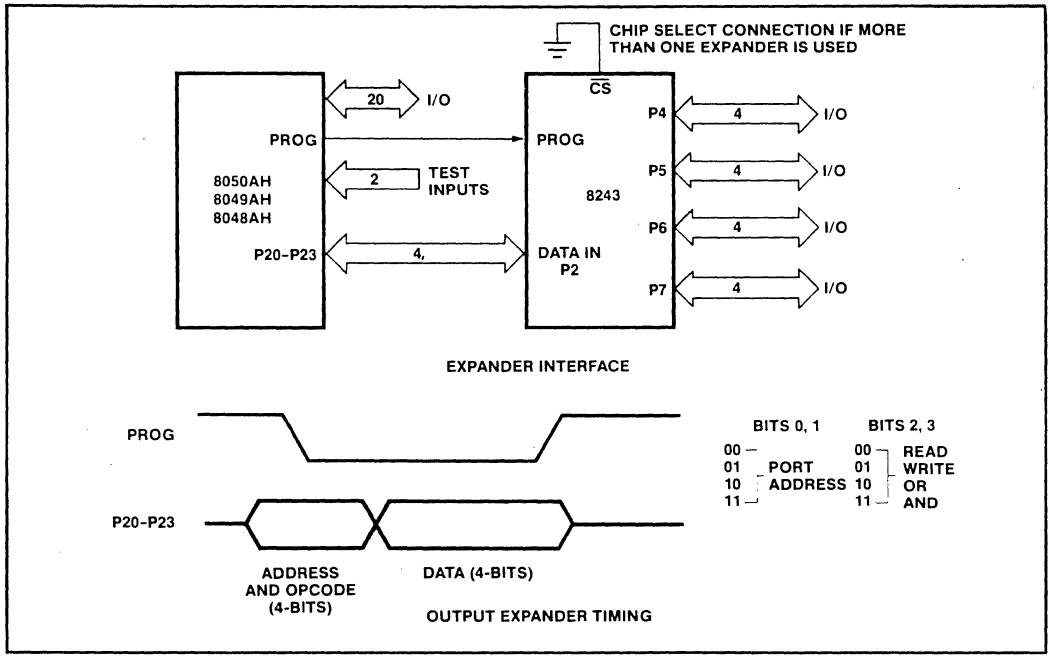


Figure 7. 8243 Expander I/O Interface

Nibble 1

3	2	1	0
I	I	A	A

Instruction Code

Port Address

Nibble 2

3	2	1	0
d	d	d	d

data

II	AA
00 Read	00 — Port #4
01 Write	01 — Port #5
10 OR	10 — Port #6
11 AND	11 — Port #7

A high to low transition of the PROG line indicates that address is present, while allow to high transition indicates the presence of data. Additional 8243's may be added to the four-bit bus and chip selected using additional output lines from the 8048AH/8748H.

I/O PORT CHARACTERISTICS

Each of the four 4-bit ports of the 8243 can serve as either input or output and can provide high drive capability in both the high and low state.

4.2 I/O Expansion with Standard Peripherals

Standard MCS-80/85 type I/O devices may be added to the MCS®-48 using the same bus and timing used for Data Memory expansion. Figure 8 shows an example of how an 8048AH can be connected to an MCS-85 peripheral. I/O devices reside on the Data Memory bus and in the data memory address space and are accessed with the same MOVX instructions. (See the previous section on data memory expansion for a description of timing.) The following are a few of the Standard MCS-80 devices which are very useful in MCS®-48 systems:

- 8214 Priority Interrupt Encoder
- 8251 Serial Communications Interface
- 8255 General Purpose Programmable I/O
- 8279 Keyboard/Display Interface
- 8254 Interval Timer

4.3 Combination Memory and I/O Expanders

As mentioned in the sections on program and data memory expansion, the 8355/8755 and 8155 expanders also contain I/O capability.

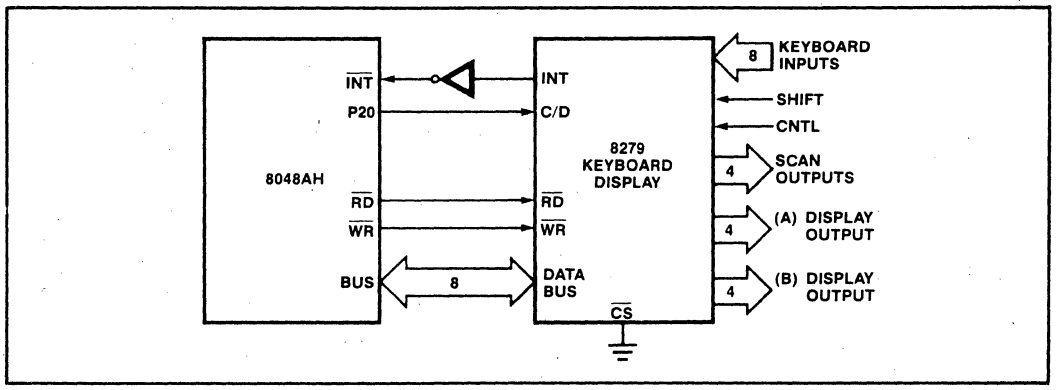


Figure 8. Keyboard/Display Interface

8355/8755: These two parts of ROM and EPROM equivalents and therefore contain the same I/O structure. I/O consists of two 8-bit ports which normally reside in the external data memory address space and are accessed with MOVX instructions. Associated with each port is an 8-bit Data Direction Register which defines each bit in the port as either an input or an output. The data direction registers are directly addressable, thereby allowing the user to define under software control each individual bit of the ports as either input or output. All outputs are statically latched and double buffered. Inputs are not latched.

8155/8156: I/O on the 8155/8156 is configured as two 8-bit programmable I/O ports and one 6-bit programmable port. These three registers and a Control/Status register are accessible as external data memory with the MOVX instructions. The contents of the control register determines the mode of the three ports. The ports can be programmed as input or output with or without associated handshake communication lines. In the handshake mode, lines of the six-bit port become input and output strobes for the two 8-bit ports. Also included in the 8155 is a 14-bit programmable timer. The clock input to the timer and the timer overflow output are available on external pins. The timer can be programmed to stop on terminal count or to continuously reload itself. A square wave or pulse output on terminal count can also be specified.

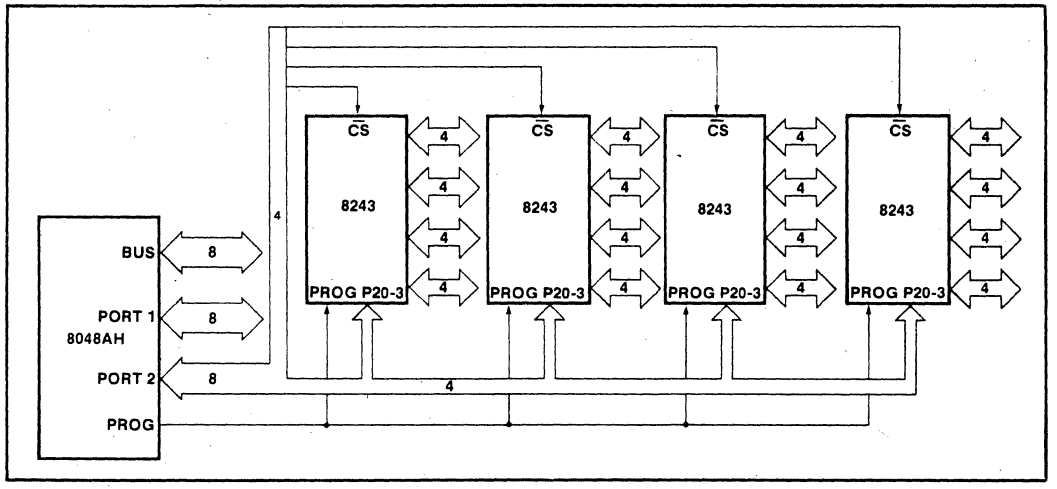


Figure 9. Low Cost I/O Expansion

I/O EXPANSION EXAMPLES

Figure 9 shows the expansion of I/O using multiple 8243's. The only difference from a single 8243 system is the addition of chip selects provided by additional 8048AH output lines. Two output liens and a decoder could also be used to address the four chips. Large numbers of 8243's would require a chip select decoder chip such as the 8205 to save I/O pins.

Figure 10 shows the 8048AH interface to a standard MCS®-80 peripheral; in this case, the 8255 Programmable Peripheral Interface, a 40-pin part which provides three 8-bit programmable I/O ports. The 8255 bus interface is typical of programmable MCS®-80 peripherals with an 8-bit bidirectional data bus, a RD and WR input for Read/Write control, a CS (chip select) input used to enable the Read/Write control logic and the address inputs used to select various internal registers.

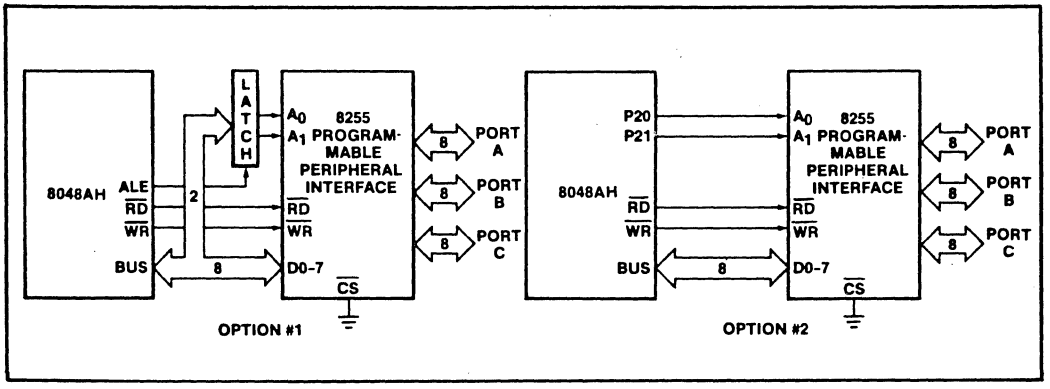


Figure 10. Interface to MCS®-80 Peripherals

Interconnection to the 8048AH is very straightforward with BUS, $\overline{RD}$, and $\overline{WR}$ connecting directly to the corresponding pins on the 8255. The only design consideration is the way in which the internal registers of the 8255 are to be addressed. If the registers are to be addressed as external data memory using the MOVX instructions, the appropriate number of address bits (in this case, 2) must be latched on BUS using ALE as described in the section on external data memories. If only a single device is connected to BUS, the 8255 may be continuously selected by grounding $\overline{CS}$. If multiple 8255's are used, additional address bits can be latched and used as chip selects.

A second addressing method eliminates external latches and chip select decoders by using output port lines as address and chip select lines directly. This method, of course, requires the setting of an output port with address information prior to executing a MOVX instruction.

5.0 MULTI-CHIP MCS®-48 SYSTEMS

Figure 11 shows the addition of two memory expanders to the 8048AH, one 8355/8755 ROM and one 8156 RAM. The main consideration in designing such a system is the addressing of the various memories and I/O ports. Note that in this configuration address lines A_{10} and A_{11} have been ORed to chip select the 8355. This ensures that the chip is active for all external program memory fetches in the 1K to 3K range and is disabled for all other addresses. This gating has been added to allow the I/O port of the 8355 to be used. If the chip was left selected all the time, there would be conflict between these ports and the RAM and I/O of the 8156. The NOR gate could be eliminated and A_{11} connected directly to the CE (instead of $\overline{CE}$) input of the 8355; however, this would create a 1K word "hole" in the program memory by causing the 8355 to be active in the 2K and 4K range instead of the normal 1K to 3K range.

In this system the various locations are addressed as follows:

- Data RAM — Addresses 0 to 255 when Port 2 Bit 0 has been previously set = 1 and Bit 1 set = 0
- RAM I/O — Addresses 0 to 3 when Port 2 Bit 0 = 1 and Bit 1 = 1
- ROM I/O — Addresses 0 to 3 when Port 2 Bit 2 or Bit 3 = 1

See the memory map in Figure 12.

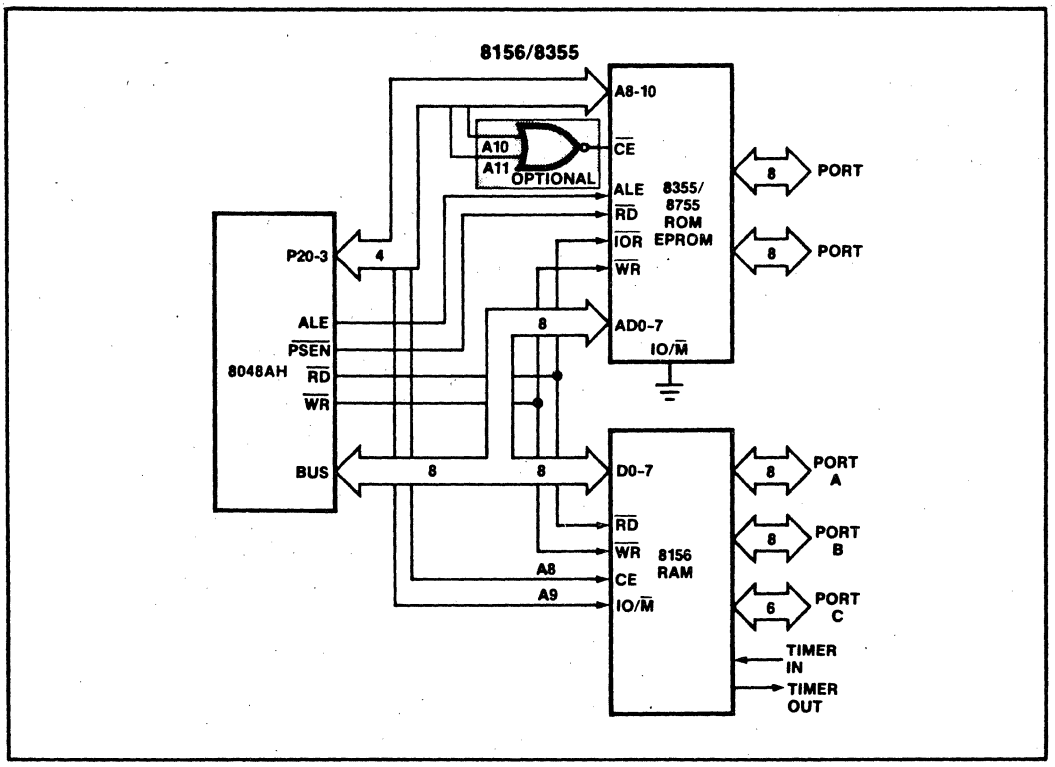


Figure 11. The Three-Component MCS®-48 System

6.0 MEMORY BANK SWITCHING

Certain systems may require more than the 4K words of program memory which are directly addressable by the program counter or more than the 256 data memory and I/O locations directly addressable by the pointer registers R0 and R1. These systems can be achieved using "bank switching" techniques. Bank switching is merely the selection of various blocks of "banks" of memory using dedicated output port lines from the processor. In the case of the 8048AH, program memory is selected in blocks of 4K words at a time, while data memory and I/O are enabled 256 words at a time.

The most important consideration in implementing two or more banks is the software required to cross the bank boundaries. Each crossing of the boundary requires that the processor first write a control bit to an output port before accessing memory or I/O in the new bank. If program memory is being switched, programs should be organized to keep boundary crossings to a minimum.

Jumping to subroutines across the boundary should be avoided when possible since the programmer must keep track of which bank to return to after completion of the subroutine. If these subroutines are to be nested and accessed from either bank, a software "stack" should be implemented to save the bank switch bit just as if it were another bit of the program counter.

From a hardware standpoint bank switching is very straightforward and involves only the connection of an I/O line or lines as bank enable signals. These enables are ANDed with normal memory and I/O chip select signals to activate the proper bank.

7.0 CONTROL SIGNAL SUMMARY

Table 1 summarizes the instructions which activate the various control outputs of the MCS®-48 processors. During all other instructions these outputs are driven to the active state.

Table 1. MCS®-48 Control Signals

Control Signal	When Active
$\overline{RD}$	During MOVX, A, @R or INS Bus
$\overline{WR}$	During MOVX @R, A or OUTL Bus
ALE	Every Machine Cycle
$\overline{PSEN}$	During Fetch of external program memory (instruction or immediate data)
PROG	During MOVD, A,P ANLD P,A MOVD P,A ORLD P,A

8.0 PORT CHARACTERISTICS

8.1 BUS Port Operations

The BUS port can operate in three different modes: as a latched I/O port, as a bidirectional bus port, or as a program memory address output when external memory is used. The BUS port lines are either active high, active low, or high impedance (floating).

The latched mode (INS, OUTL) is intended for use in the single-chip configuration where BUS is not begin used as an expander port. OUTL and MOVX instructions can be mixed if necessary. However, a previously latched output will be destroyed by executing a MOVX instruction and BUS will be left in the high impedance state. INS does not put the BUS in a high impedance state. Therefore, the use of MOVX after OUTL to put the BUS in a high impedance state is necessary before an INS instruction intended to read an external word (as opposed to the previously latched value).

OUTL should never be used in a system with external program memory, since latching BUS can cause the next instruction, if external, to be fetched improperly.

8.2 Port 2 Operations

The lower half of Port 2 can be used in three different ways: as a quasi-bidirectional static port, as an 8243 expander port, and to adddress external program memory.

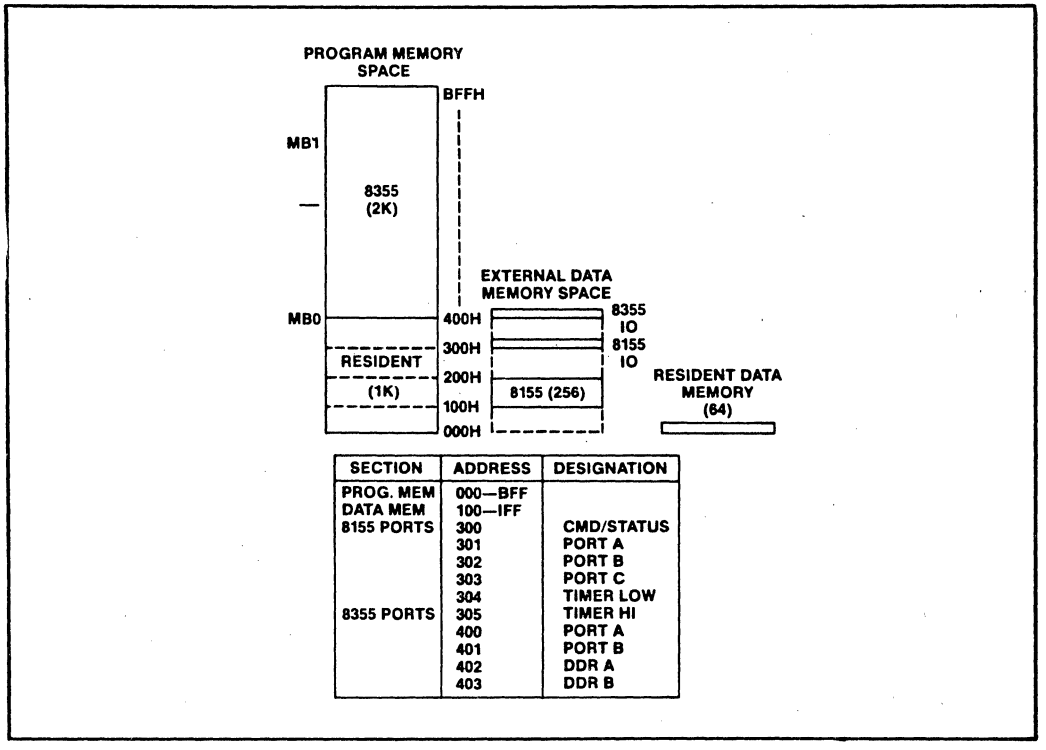


Figure 12. Memory Map for Three-Component MCS®-48 Family

In all cases outputs are driven low by an active device and driven high momentarily by a low impedance device and held high by a high impedance device to VCC.

The port may contain latched I/O data prior to its use in another mode without affecting operation of either. If lower Port 2 (P20-3) is used to output address for an external program memory fetch, the I/O information previously latched will be automatically removed temporarily while address is present, then retored when the fetch is complete. However, if lower Port 2 is used to communicate with an 8243, previously latched I/O information will be removed and not restored. After an input from the 8243, P20-3 will be left in the input mode (floating). After an output to the 8243, P20-3 will contain the value written, ANDed, or ORed to the 8243 port.

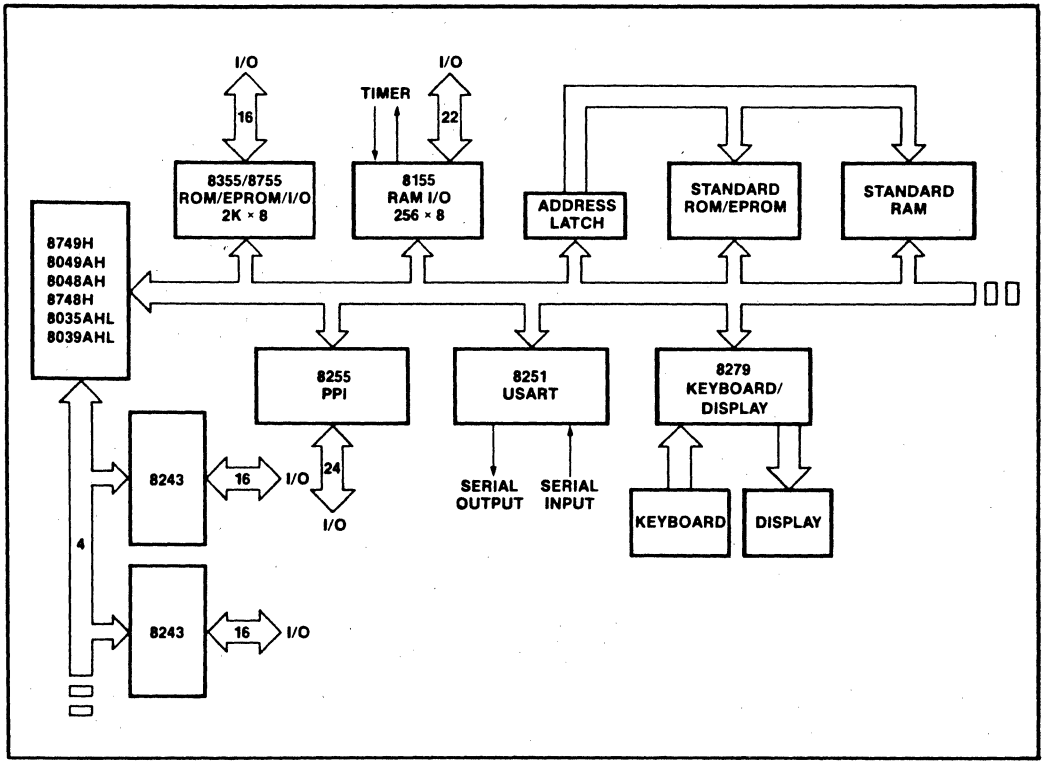


Figure 13. MCS®-48 Expansion Capability

MCS®-48 Instruction Set 3

MCS®-48 INSTRUCTION SET

1.0 INTRODUCTION

The MCS®-48 instruction set is extensive for a machine of its size and has been tailored to be straightforward and very efficient in its use of program memory. All instructions are either one or two bytes in length and over 80% are only one byte long. Also, all instructions execute in either one or two cycles and over 50% of all instructions execute in a single cycle. Double cycle instructions include all immediate instructions, and all I/O instructions.

The MCS-48 microcomputers have been designed to handle arithmetic operations efficiently in both binary and BCD as well as handle the single-bit operations required in control applications. Special instructions have also been included to simplify loop counters, table look-up routines, and N-way branch routines.

1.1 Data Transfers

As can be seen in Figure 1 the 8-bit accumulator is the central point for all data transfers within the 8048. Data can be transferred between the 8 registers of each working register bank and the accumulator directly, i.e., the source or destination register is specified by the instruction. The remaining locations of the internal RAM array are referred to as Data Memory and are addressed indirectly via an address stored in either R0 or R1 of the active register bank. R0 and R1 are also used to indirecly address external data memory when it is present. Transfers to and from internal RAM require one cycle, while transfers to external RAM require two. Constants stored in Program Memory can be loaded directly to the accumulator and to the 8 working registers. Data can also be transferred directly between the accumulator and the on-

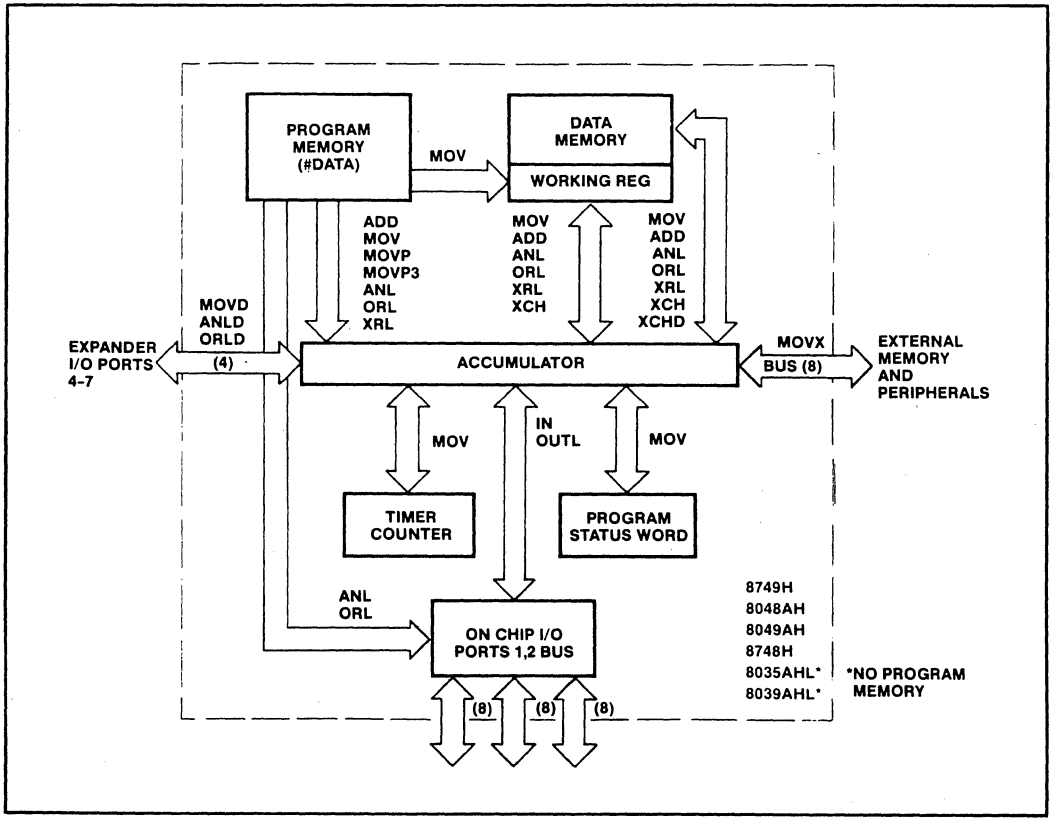


Figure 1. Data Transfer Instructions

board timer counter or the accumulator and the Program Status word (PSW). Writing to the PSW alters machine status accordingly and provides a means of restoring status after an interrupt or of altering the stack pointer if necessary.

1.2 Accumulator Operations

Immediate data, data memory, or the working registers can be added with or without carry to the accumulator. These sources can also be ANDed, ORed, or Exclusive ORed to the accumulator. Data may be moved to or from the accumulator and working registers or data memory. The two values can also be exchanged in a single operation.

In addition, the lower 4 bits of the accumulator can be exchanged with the lower 4-bits of any of the internal RAM locations. This instruction, along with an instruction which swaps the upper and lower 4-bit halves of the accumulator, provides for easy handling of 4-bit quantities, including BCD numbers. To facilitate BCD arithmetic, a Decimal Adjust instruction is included. This instruction is used to correct the result of the binary addition of two 2-digit BCD numbers. Performing a decimal adjust on the result in the accumulator produces the required BCD result.

Finally, the accumulator can be incremented, decremented, cleared, or complemented and can be rotated left or right 1 bit at a time with or without carry.

Although there is no subtract instruction in the 8048AH, this operation can be easily implemented with three single-byte single-cycle instructions.

A value may be subtracted from the accumulator with the result in the accumulator by:

- Complementing the accumulator
- Adding the value to the accumulator
- Complementing the accumulator

1.3 Register Operations

The working registers can be accessed via the accumulator as explained above, or can be loaded immediate with constants from program memory. In addition, they can be incremented or decremented or used as loop counters using the decrement and jump, if not zero instruction, as explained under branch instructions.

All Data Memory including working registers can be accessed with indirect instructions via R0 and R1 and can be incremented.

1.4 Flags

There are four user-accessible flags in the 8048AH: Carry, Auxiliary Carry, F0 and F1. Carry indicates overflow of the accumulator, and Auxiliary Carry is used to indiate overflow between BCD digits and is used during decimal-adjust operation. Both Carry and Auxiliary Carry are accessible as part of the program status word and are stored on the stack during subroutines. F0 and F1 are undedicated general-purpose flags to be used as the programmer desires. Both flags can be cleared or complemented and tested by conditional jump instructions. F0 is also accessible via the Program Status word and is stored on the stack with the carry flags.

1.5 Branch Instructions

The unconditional jump instruction is two bytes and allows jumps anywhere in the first 2K words of program memory. Jumps to the second 2K of memory (4K words are directly addressable) are made first by executing a select memory bank instruction, then executing the jump instruction. The 2K boundary can only be crossed via a jump or subroutine call instruction, i.e., the bank switch does not occur until a jump is executed. Once a memory bank has been selected all subsequent jumps will be to the selected bank until another select memory bank instruction is executed. A subroutine in the opposite bank can be accessed by a select memory bank instruction followed by a call instruction. Upon completion of the subroutine, execution will automatically return to the original bank; however, unless the original bank is reselected, the next jump instruction encountered will again transfer execution to the opposite bank.

Conditional jumps can test the following inputs and machine status:

- T0 Input Pin
- T1 Input Pin
- $\overline{\text{INT}}$ Input Pin
- Accumulator Zero
- Any bit of Accumulator
- Carry Flag
- F0 Flag
- F1 Flag

Conditional jumps allow a branch to any address within the current page (256 words) of execution. The conditions tested are the instantaneous values at the time the conditional jump is executed. For instance, the jump on accumulator zero instruction tests the accumulator itself, not an intermediate zero flag.

The decrement register and jump if not zero instruction combines a decrement and a branch instruction to create an instruction very useful in implementing a loop counter. This instruction can designate any one of the 8 working registers as a counter and can effect a branch to any address within the current page of execution.

A single-byte indirect jump instruction allows the program to be vectored to any one of several different locations based on the contents of the accumulator. The contents of the accumulator points to a location in program memory which contains the jump address. The 8-bit jump address refers to the current page of execution. This instruction could be used, for instance, to vector to any one of several routines based on an ASCII character which has been loaded in the accumulator. In this way ASCII key inputs can be used to initiate various routines.

1.6 Subroutines

Subroutines are entered by executing a call instruction. Calls can be made like unconditional jumps to any address in a 2K word bank, and jumps across the 2K boundary are executed in the same manner. Two separate return instructions determine whether or not status (upper 4-bits of PSW) is restored upon return from the subroutine.

The return and restore status instruction also signals the end of an interrupt service routine if one has been in progress.

1.7 Timer Instructions

The 8-bit on board timer/counter can be loaded or read via the accumulator while the counter is stopped or while counting. The counter can be started as a timer with an internal clock source or an event counter or timer with an external clock applied to the T1 input pin. The instruction executed determines which clock source is used. A single instruction stops the counter whether it is operating with an internal or an external clock source. In addition, two instructions allow the timer interrupt to be enabled or disabled.

1.8 Control Instructions

Two instructions allow the external interrupt source to be enabled or disabled. Interrupts are initially disabled and are automatically disabled while an interrupt service routines is in progress and re-enabled afterward.

There are four memory bank select instructions, two to designate the active working register bank and two to control program memory banks. The operation of the program memory bank switch is explained in Section 2.2 in the Expanded MCS-48 System chapter.

The working register bank switch instructions allow the programmer to immediately substitute a second 8-register working register bank for the one in use. This effectively provides 16 working registers or it can be used as a means of quickly saving the contents of the registers in response to an interrupt. The user has the option to switch or not to switch banks on interrupt. However, if the banks are switched, the original bank will be automatically restored upon execution of a return and restore status instruction at the end of the interrupt service routine.

A special instruction enables an internal clock, which is the XTAL frequency divided by three to be output on pin T0. This clock can be used as a general-purpose clock in the user's system. This instruction should be used only to initialize the system since the clock output can be disabled only by application of system reset.

1.9 Input/Output Instructions

Ports 1 and 2 are 8-bit static I/O ports which can be loaded to and from the accumulator. Outputs are statically latched but inputs are not latched and must be read while inputs are present. In addition, immediate data from program memory can be ANDed or ORed directly to Port 1 and Port 2 with the result remaining on the port. This allows "masks" stored in program memory to selectively set or reset individual bits of the I/O ports. Ports 1 and 2 are configured to allow input on a given pin by first writing a "1" out to the pin.

An 8-bit port called BUS can also be accessed via the accumulator and can have statically latched outputs as well. It too can have immediate data ANDed or ORed directly to its outputs, however, unlike ports 1 and 2, all eight lines of BUS must be treated as either input or output at any one time. In addition to being a static port, BUS can be used as a true synchronous bi-directional port using the Move External instructions used to access external data memory. When these instructions are executed, a corresponding $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ pulse is generated and data is valid only at that time. When data is not being transferred, BUS is in a high impedance state. Note that the OUTL, ANL, and the ORL instructions for the BUS are for use with internal program memory only.

The basic three on-board I/O ports can be expanded via a 4-bit expander bus using half of port 2. I/O expander devices on this bus consist of four 4-bit ports which are addressed as ports 4 through 7. These ports have their own AND and OR instructions like the on-board ports as well as move instructions to transfer data in or out. The expander AND and OR instructions, however, combine the contents of accumulator with the selected port rather than immediate data as is done with the on-board ports.

I/O devices can also be added externally using the BUS port as the expansion bus. In this case the I/O ports become "memory mapped", i.e., they are addressed in the same way as external data memory and exist in the external data memory address space addressed by pointer register R0 or R1.

2.0 INSTRUCTION SET DESCRIPTION

The following pages describe the MCS®-48 instruction set in detail. The instruction set is first summarized with instructions grouped functionally. This summary page is followed by a detailed description listed alphabetically by mnemonic opcode.

The alphabetical listing includes the following information.

- Mnemonic
- Machine Code
- Verbal Description
- Symbolic Description
- Assembly Language Example

The machine code is represented with the most significant bit (7) to the left and two byte instructions are represented with the first byte on the left. The assembly language examples are formulated as follows:

Arbitrary

Label: Mnemonic, Operand;

Descriptive Comment

8048AH/8748H/8049AH/8050AH/8749H
Instruction Set Summary

Mnemonic	Description	Bytes	Cycle
Accumulator			
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive Or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL, A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Input/Output			
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
*INS A, BUS	Input BUS to A	1	2
*OUTL BUS, A	Output A to BUS	1	2
*ANL BUS, # data	And immediate to BUS	2	2
*ORL BUS, # data	Or immediate to BUS	2	2
MOVD A, P	Input Expander port to A	1	2
MOVD P, A	Output A to Expander port	1	2
ANLD P, A	And A to Expander port	1	2
ORLD P, A	Or A to Expander port	1	2

Mnemonic	Description	Bytes	Cycles
Registers			
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1
Branch			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and jump	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag = 1	2	2
JNI addr	Jump on INT = 0	2	2
JBb addr	Jump on Accumulator Bit	2	2
Subroutine			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
Flags			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear Flag 1	1	1
CPL F1	Complement Flag 1	1	1
Data Moves			
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, # data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1

*For use with internal memory only.

8048AH/8748H/8049AH/8050AH/8749H
Instruction Set Summary (Con't)

Mnemonic	Description	Bytes	Cycle
Data Moves (Cont'd)			
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from Page 3	1	2
Timer/Counter			
MOV A, T	Read Timer/Counter	1	1
MOV T, A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/Counter Interrupt	1	1
DIS TCNTI	Disable Timer/Counter Interrupt	1	1

Mnemonic	Description	Bytes	Cycle
Control			
EN I	Enable external Interrupt	1	1
DIS I	Disable external Interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1
NOP	No Operation	1	1

MCS®-48 INSTRUCTION SET
Symbols and Abbreviations Used

A	Accumulator
AC	Auxiliary Carry
addr	12-Bit Program Memory Address
Bb	Bit Designator (b = 0-7)
BS	Bank Switch
BUS	BUS Port
C	Carry
CLK	Clock
CNT	Event Counter
CRR	Conversion Result Register
D	Mnemonic for 4-Bit Digit (Nibble)
data	8-Bit Number or Expression
DBF	Memory Bank Flip-Flop
F0, F1	Flag 0, Flag 1
I	Interrupt
P	Mnemonic for "in-page" Operation
PC	Program Counter
Pp	Port Designator (p = 1, 2 or 4-7)
PSW	Program Status Word
Ri	Data memory Pointer (i = 0, or 1)
Rr	Register Designator (r = 0-7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Test 0, Test 1
X	Mnemonic for External RAM
#	Immediate Data Prefix
@	Indirect Address Prefix
$	Current Value of Program Counter
(X)	Contents of X
((X))	Contents of Location Addressed by X
←	Is Replaced by

ADD A,R_r Add Register Contents to Accumulator

Encoding: | 0 1 1 0 | 1 r r r | 68H-6FH

Description: The contents of register 'r' are added to the accumulator. Carry is affected.

Operation: (A) ← (A) + (Rr) r = 0-7

Example:
```
ADDREG: ADD A,R6      ;ADD REG 6 CONTENTS
                      ;TO ACC
```

ADD A,@R_i Add Data Memory Contents to Accumulator

Encoding; | 0 1 1 0 | 0 0 0 i | 60H-61H

Description: The contents of the resident data memory location addressed by register 'i' bits 0–5** are added to the accumulator. Carry is affected.

Operation: (A) ← (A) + ((Ri)) i = 0-1

Example:
```
ADDM:  MOV R0, #01FH   ;MOVE '1F' HEX TO REG 0
       ADD A, @R0      ;ADD VALUE OF LOCATION
                       ;31 TO ACC
```

ADD A,#data Add Immediate Data to Accumulator

Encoding: | 0 0 0 0 | 0 0 1 1 | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | 03H

Description: This is a 2-cycle instruction. The specified data is added to the accumulator. Carry is affected.

Operation: (A) ← (A) + data

Example:
```
ADDID: ADD A,#ADDER:   ;ADD VALUE OF SYMBOL
                       ;ADDER' TO ACC
```

ADDC A,R_r Add Carry and Register Contents to Accumulator

Encoding: | 0 1 1 1 | 1 r r r | 78H-7FH

Description: The content of the carry bit is added to accumulator location 0 and the carry bit cleared. The contents of register 'r' are then added to the accumulator. Carry is affected.

Operation: (A) ← (A) + (Rr) + (C) r = 0-7

Example:
```
ADDRGC: ADDC A,R4      ;ADD CARRY AND REG 4
                       ;CONTENTS TO ACC
```

** 0–5 in 8048AH/8748H
0–6 in 8049AH/8749H
0–7 in 8050AH

ADDC A,@R_i Add Carry and Data Memory Contents to Accumulator

Encoding: | 0 1 1 1 | 0 0 0 i | 70H-71H

Description: The content of the carry bit is added to accumulator location 0 and the carry bit cleared. Then the contents of the resident data memory location addressed by register 'i' bits 0–5** are added to the accumulator. Carry is affected.

Operation: (A) ← (A) + ((Ri)) + (C) i = 0-1

Example:
```
ADDMC: MOV R1,#40      ;MOVE '40' DEC TO REG 1
       ADDC A,@R1      ;ADD CARRY AND LOCATION 40
                       ;CONTENTS TO ACC
```

ADDC A,@data Add Carry and Immediate Data to Accumulator

Encoding: | 0 0 0 1 | 0 0 1 1 | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | 13H

Description: This is a 2-cycle instruction. The content of the carry bit is added to accumulator location 0 and the carry bit cleared. Then the specified data is added to the accumulator. Carry is affected.

Operation: (A) ← (A) + data + (C)

Example:
```
ADDC A,#225            ;ADD CARRY AND '225' DEC
                       ;TO ACC
```

ANL A,R_r Logical AND Accumulator with Register Mask

Encoding: | 0 1 0 1 | 1 r r r | 58H-5FH

Description: Data in the accumulator is logically ANDed with the mask contained in working register 'r'.

Operation: (A) ← (A) AND (Rr) r = 0-7

Example:
```
ANDREG: ANL A,R3       ;'AND' ACC CONTENTS WITH MASK
                       ;IN REG 3
```

ANL A,@R_i Logical AND Accumulator with memory Mask

Encoding: | 0 1 0 1 | 0 0 0 i | 50H-51H

Description: Data in the accumulator is logically ANDed with the mask contained in the data memory location referenced by register 'i' bits 0-5**.

Operation: (A) ← (A) AND ((Ri)) i = 0-1

Example:
```
ANDDM: MOV R0,#03FH    ;MOVE '3F' HEX TO REG 0
       ANL A, @R0      ;'AND' ACC CONTENTS WITH
                       ;MASK IN LOCATION 63
```

** 0–5 in 8048AH/8748H
0–6 in 8049AH/8749H
0–7 in 8050AH

ANL A,#data Logical AND Accumulator with Immediate Mask

Encoding: | 0 1 0 1 | 0 0 1 1 | | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | 53H

Description: This is a 2-cycle instruction. Data in the accumulator is logically ANDed with an immediately-specified mask.

Operation: (A) ← (A) AND data

Examples:
```
ANDID: ANL A,#0AFH      ;'AND' ACC CONTENTS
                        ;WITH MASK 10101111
       ANL A,#3 + X/Y   ;'AND' ACC CONTENTS
                        ;WITH VALUE OF EXP
                        ;'3 + XY/Y'
```

ANL BUS,#data* Logical AND BUS with Immediate Mask

Encoding: | 1 0 0 1 | 1 0 0 0 | | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | 98H

Description: This is a 2-cycle instruction. Data on the BUS port is logically ANDed with an immediately-specified mask. This instruction assumes prior specification of an 'OUTL BUS, A' instruction.

Operation: (BUS) ← (BUS) AND data

Example:
```
ANDBUS: ANL BUS,#MASK   ;'AND' BUS CONTENTS
                        ;WITH MASK EQUAL VALUE
                        ;OF SYMBOL 'MASK'
```

ANL Pp,#data Logical AND Port 1-2 with Immediate Mask

Encoding: | 1 0 0 1 | 1 0 p p | | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | 99H-9AH

Description: This is a 2-cycle instruction. Data on port 'p' is logically ANDed with an immediately-specified mask.

Operation: (Pp) ← (Pp) AND DATA p = 1-2

Example:
```
ANDP2: ANL P2,#0F0H     ;'AND' PORT 2 CONTENTS
                        ;WITH MASK 'F0' HEX
                        ;(CLEAR P20-23)
```

* For use with internal program memory ONLY.

ANLD Pp,A Logical AND Port 4-7 with Accumulator Mask

Encoding: | 1 0 0 1 | 1 1 p p | 9CH-9FH

Description: This is a 2-cycle instruction. Data on port 'p' is logically ANDed with the digit mask contained in accumulator bits 0-3.

Operation: (Pp) ← (Pp) AND (A0-3) p = 4-7

Note: The mapping of port 'p' to opcode bits 0-1 is as follows:

1 0	Port
0 0	4
0 1	5
1 0	6
1 1	7

Example:
```
ANDP4: ANLD P4,A        ;'AND' PORT 4 CONTENTS
                        ;WITH ACC BITS 0-3
```

CALL address Subroutine Call

Encoding: | a_{10} a_9 a_8 1 | 0 1 0 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

Page	Hex Op Code
0	14
1	34
2	54
3	74
4	94
5	B4
6	D4
7	F4

Description: This is a 2-cycle instruction. The program counter and PSW bits 4-7 are saved in the stack. The stack pointer (PSW bits 0-2) is updated. Program control is then passed to the location specified by 'address'. PC bit 11 is determined by the most recent SEL MB instruction.

A CALL cannot begin in locations 2046-2047 or 4094-4095. Execution continues at the instruction following the CALL upon return from the subroutine.

Operation: $((SP)) \leftarrow (PC), (PSW_{4-7})$
$(SP) \leftarrow (SP) + 1$
$(PC_{8-10}) \leftarrow (addr_{8-10})$
$(PC_{0-7}) \leftarrow (addr_{0-7})$
$(PC_{11}) \leftarrow DBF$

Example: Add three groups of two numbers. Put subtotals in locations 50, 51 and total in location 52.

```
          MOV R0,#50        ;MOVE '50' DEC TO ADDRESS
                            ;REG 0
BEGADD:   MOV A,R1          ;MOVE CONTENTS OF REG 1
                            ;TO ACC
          ADD A,R2          ;ADD REG 2 TO ACC
          CALL SUBTOT       ;CALL SUBROUTINE 'SUBTOT'
          ADDC A R3         ;ADD REG 3 TO ACC
          ADDC A,R4         ;ADD REG 4 TO ACC
          CALL SUBTOT       ;CALL SUBROUTINE 'SUBTOT'
          ADDC A,R5         ;ADD REG 5 TO ACC
          ADDC A,R6         ;ADD REG 6 TO ACC
          CALL SUBTOT       ;CALL SUBROUTINE 'SUBTOT'
SUBTOT:   MOV @R0,A         ;MOVE CONTENTS OF ACC TO
                            ;LOCATION ADDRESSED BY
                            ;REG 0
          INC R0            ;INCREMENT REG 0
          RET               ;RETURN TO MAIN PROGRAM
```

CLR A Clear Accumulator

Encoding: | 0 0 1 0 | 0 1 1 1 | 27H

Description: The contents of the accumulator are cleared to zero.

Operation: A ← 0

CLR C Clear Carry Bit

Encoding: | 1 0 0 1 | 0 1 1 1 | 97H

Description: During normal program execution, the carry bit can be set to one by the ADD, ADDC, RLC, CPL C, RRC, and DAA insructions. This instruction resets the carry bit to zero.

Operation: C ← 0

CLR F1 Clear Flag 1

Encoding: | 1 0 1 0 | 0 1 0 1 | A5H

Description: Flag 1 is cleared to zero.

Operation: (F1) ← 0

CLR F0 Clear Flag 0

Encoding: | 1 0 0 0 | 0 1 0 1 | 85H

Description: Flag 0 is cleared to zero.

Operation: (F0) ← 0

CPL A Complement Accumulator

Encoding: | 0 0 1 1 | 0 1 1 1 | 37H

Description: The contents of the accumulator are complemented. This is strictly a one's complement. Each one is changed to zero and vice-versa.

Operation: (A) ← NOT (A)

Example: Assume accumulator contains 01101010.

```
CPLA: CPL A          ;ACC CONTENTS ARE COMPLE-
                     ;MENTED TO 10010101
```

CPL C Complement Carry Bit

Encoding: | 1 0 1 0 | 0 1 1 1 | A7H

Description: The setting of the carry bit is complemented; one is changed to zero, and zero is changed to one.

Operation: (C) ← NOT (C)

Example: Set C to one; current setting is unknown.

```
CTO1: CLR C          ;C IS CLEARED TO ZERO
      CPL C          ;C IS SET TO ONE
```

CPL F0 Complement Flag 0

Encoding: | 1 0 0 1 | 0 1 0 1 | 95H

Description: The setting of flag 0 is complemented; one is changed to zero, and zero is changed to one.

Operation: F0 ← NOT (F0)

CPL F1 Complement Flag 1

Encoding: | 1 0 1 1 | 0 1 0 1 | B5H

Description: The setting of flag 1 is complemented; one is changed to zero, and zero is changed to one.

Operation: (F1) ← NOT (F1)

DA A Decimal Adjust Accumulator

Encoding: | 0 1 0 1 | 0 1 1 1 | 57H

Description: The 8-bit accumulator value is adjusted to form two 4-bit Binary Coded Decimal (BCD) digits following the binary addition of BCD numbers. The carry bit C is affected. If the contents of bits 0–3 are greater than nine, or if AC is one, the accumulator is incremented by six.

The four high-order bits are then checked. If bits 4–7 exceed nine, or if C is one, these bits are increased by six. If an overflow occurs, C is set to one.

Example: Assume accumulator contains 10011011.

```
DA A                          ;ACC Adjusted to 00000001
                              ;WITH C SET

C AC 7     4 3     0
0  0 1 0 0 1 1 0 1 1
     0 0 0 0 0 1 1 0          ADD SIX TO BITS 0-7
0  1 1 0 1 0 0 0 0 1
     0 1 1 0                  ADD SIX TO BITS 4-7
1  0 0 0 0 0 0 0 0 1          OVERFLOW TO C
```

DEC A Decrement Accumulator

Encoding: | 0 0 0 0 | 0 1 1 1 | 07H

Description: The contents of the accumulator are decremented by one. The carry flag is not affected.

Operation: (A) ← (A) -1

Example: Decrement contents of external data memory location 63.

```
MOV R0,#3FH                   ;MOVE '3F' HEX TO REG 0
MOVX A, @R0                   ;MOVE CONTENTS OF
                              ;LOCATION 63 TO ACC
DEC A                         ;DECREMENT ACC
MOVX @R0,A                    ;MOVE CONTENTS OF ACC TO
                              ;LOCATION 63 IN EXPANDED
                              ;MEMORY
```

DEC Rr Decrement Register

Encoding: | 1 1 0 0 | 1 r r r | C8H-CFH

Description: The contents of working register 'r' are decremented by one.

Operation: (Rr) ← (Rr) -1 r = 0-7

Example:

```
DECR1: DEC R1                 ;DECREMENT CONTENTS OF REG 1
```

DIS I External Interrupt

Encoding: | 0 0 0 1 | 0 1 0 1 | 15H

Description: External interrupts are disabled. A low signal on the interrupt input pin has no effect.

DIS TCNTI Disable Timer/Counter Interrupt

Encoding: | 0 0 1 1 | 0 1 0 1 | 35H

Description: Timer/counter interrupts are disabled. Any pending timer interrupt request is cleared. The interrupt sequence is not initiated by an overflow, but the timer flag is set and time accumulation continues.

DJNZ R_r, address Decrement Register and Test

Encoding: | 1 1 1 0 | 1 r r r | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | E8H-EFH

Description: This is a 2-cycle instruction. Register 'r' is decremented, then tested for zero. If the register contains all zeros, program control falls through to the next instruction. If the register contents are not zero, control jumps to the specified 'address'.

The address in this case must evaluate to 8-bits, that is, the jump must be to a location within the current 256-location page.

Example: (Rr) ← (Rr) -1 r = 0-7
If Rr not 0
(PC_{0-7}) ← addr
Note: A 12-bit address specification does not cause an error if the DJNZ instruction and the jump target are on the same page. If the DJNZ instruction begins in location 255 of a page, it must jump to a target address on the following page.

Example: Increment values in data memory locations 50-54.

```
        MOV R0,#50          ;MOVE '50' DEC TO ADDRESS
                            ;REG 0
        MOV R3,#5           ;MOVE '5' DEC TO COUNTER
                            ;REG 3
INCRT:  INC @R0             ;INCREMENT CONTENTS OF
                            ;LOCATION ADDRESSED BY
                            ;REG 0
        INC R0              ;INCREMENT ADDRESS IN REG 0
        DJNZ R3, INCRT      ;DECREMENT REG 3 — JUMP TO
                            ;'INCRT' IF REG 3 NONZERO
        NEXT —              ;'NEXT' ROUTINE EXECUTED
                            ;IF R3 IS ZERO
```

EN I Enable External Interrupt

Encoding: | 0 0 0 0 | 0 1 0 1 | 05H

Description: External interrupts are enabled. A low signal on the interrupt input pin initiates the interrupt sequence.

EN TCNTI Enable Timer/Counter Interrupt

Encoding: | 0 0 1 0 | 0 1 0 1 | 25H

Description: Timer/counter interrupts are enabled. An overflow of the timer/counter initiates the interrupt sequence.

ENT0 CLK Enable Clock Output

Encoding: | 0 1 1 1 | 0 1 0 1 | 75H

Description: The test 0 pin is enabled to act as the clock output. This function is disabled by a system reset.

Example:
```
EMTST0: ENT0 CLK          ;ENABLE T0 AS CLOCK OUTPUT
```

IN A,Pp Input Port or Data to Accumulator

Encoding: | 0 0 0 0 | 1 0 p p | 09H-0AH

Description: This is a 2-cycle instruction. Data present on port 'p' is transferred (read) to the accumulator.

Operation: (A) ← (Pp) p = 1-2

```
INP12: IN A,P1        ;INPUT PORT 1 CONTENTS TO ACC
       MOV R6,A       ;MOVE ACC CONTENTS TO REG 6
       IN A,P2        ;INPUT PORT 2 CONTENTS TO ACC
       MOV R7,A       ;MOVE ACC CONTENTS TO REG 7
```

INC A Increment Accumulator

Encoding: | 0 0 0 1 | 0 1 1 1 | 17H

Description: The contents of the accumulator are incremented by one. Carry is not affected.

Operation: (A) ← (A) +1

Example: Increment contents of location 100 in external data memory.

```
INCA:  MOV R0,#100      ;MOVE '100' DEC TO ADDRESS REG 0
       MOVX A,@R0       ;MOVE CONTENTS OF LOCATION
                        ;100 TO ACC
       INC A            ;INCREMENT A
       MOVX @R0,A       ;MOVE ACC CONTENTS TO
                        ;LOCATION 101
```

INC R_r Increment Register

Encoding: | 0 0 0 1 | 1 r r r | 18H-1FH

Description: The contents of working register 'r' are incremented by one.

Operation: (Rr) ← (Rr) + 1 r = 0-7

Example:
```
INCR0: INC R0           ;INCREMENT CONTENTS OF REG 0
```

INC @R_i Increment Data Memory Location

Encoding: | 0 0 0 1 | 0 0 0 i | 10H-11H

Description: The contents of the resident data memory location addressed by register 'i' bits 0–5** are incremented by one.

Operation: ((Ri)) ← ((Ri)) + 1 i = 0-1

Example:
```
INCDM: MOV R1,#03FH     ;MOVE ONES TO REG 1
       INC @R1          ;INCREMENT LOCATION 63
```

INS A,BUS* Strobed Input of BUS Data to Accumulator

Encoding: | 0 0 0 0 | 1 0 0 0 | 08H

Description: This is a 2-cycle instruction. Data present on the BUS port is transferred (read) to the accumulator when the RD pulse is dropped. (Refer to section on programming memory expansion for details.)

Operation: (A) ← (BUS)

Example:
```
INPBUS: INS A,BUS       ;INPUT BUS CONTENTS TO ACC
```

* For use with internal program memory ONLY.

** 0–5 in 8048AH/8748H
0–6 in 8049AH/8749H
0–7 in 8050AH

JBb address Jump If Accumulator Bit Is Set

Encoding: | b_2 b_1 b_0 1 | 0 0 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

Accumulator Bit	Hex Op Code
0	12
1	32
2	52
3	72
4	92
5	B2
6	D2
7	F2

Description: This is a 2-cycle instruction. Control passes to the specified address if accumulator bit 'b' is set to one.

Operation:

	b = 0-7
$(PC_{0-7}) \leftarrow$ addr	If Bb = 1
(PC) = (PC) + 2	If Bb = 0

Example:

```
JB4IS1: JB4 NEXT    ;JUMP TO 'NEXT' ROUTINE
                    ;IF ACC BIT 4 = 1
```

JC address Jump If Carry Is Set

Encoding: | 1 1 1 1 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | F6H

Description: This is a 2-cycle instruction. Control passes to the specified address if the carry bit is set to one.

Operation:

$(PC_{0-7}) \leftarrow$ addr	If C = 1
(PC) = (PC) + 2	If C = 0

Example:

```
JC1: JC OVFLOW      ;JUMP TO 'OVFLOW' ROUTINE
                    ;IF C = 1
```

JF0 address Jump If Flag 0 Is Set

Encoding: | 1 0 1 1 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | B6H

Description: This is a 2-cycle instruction. Control passes to the specified address if flag 0 is set to one.

Operation:

$(PC_{0-7}) \leftarrow$ addr	If F0 = 1
(PC) =(PC) + 2	If F0 = 0

Example:

```
JF0IS1: JF0 TOTAL   ;JUMP TO 'TOTAL' ROUTINE IF F0 = 1
```

JF1 address Jump If Flag 1 Is Set

Encoding: | 0 1 1 1 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | 76H

Description: This is a 2-cycle instruction. Control passes to the specified address if flag 1 is set to one.

Operation: $(PC_{0-7}) \leftarrow$ addr — If F1 = 1
(PC) = (PC + 2) — If F1 = 0

Example:
```
JF1IS1: JF1 FILBUF      ;JUMP TO 'FILBUF'
                        ;ROUTINE IF F1 = 1
```

JMP address Direct Jump within 2K Block

Encoding: | a_{10} a_9 a_8 0 | 0 1 0 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

Page	Hex Op Code
0	04
1	24
2	44
3	64
4	84
5	A4
6	C4
7	E4

Description: This is a 2-cycle instruction. Bits 0-10 of the program counter are replaced with the directly-specified address. The setting of PC bit 11 is determined by the most recent SELECT MB instruction.

Operation: $(PC_{8-10}) \leftarrow$ addr 8-10
$(PC_{0-7}) \leftarrow$ addr 0-7
$(PC_{11}) \leftarrow$ DBF

Example:
```
JMP SUBTOT              ;JUMP TO SUBROUTINE 'SUBTOT'
JMP $-6                 ;JUMP TO INSTRUCTION SIX
                        ;LOCATIONS BEFORE CURRENT
                        ;LOCATION
JMP 2FH                 ;JUMP TO ADDRESS '2F' HEX
```

JMPP @A Indirect Jump within Page

Encoding: | 1 0 1 1 | 0 0 1 1 | B3H

Description: This is a 2-cycle insruction. The contents of the program memory location pointed to by the accumulator are substituted for the 'page' portion of the program counter (PC bits 0-7).

Operation: $(PC_{0-7}) \leftarrow ((A))$

Example: Assume accumulator contains 0FH.

```
JMPPAG: JMPP @A          ;JUMP TO ADDRESS STORED IN
                         ;LOCATION 15 IN CURRENT PAGE
```

JNC address Jump If Carry Is Not Set

Encoding:

1 1 1 0	0 1 1 0	a_7 a_6 a_5 a_4	a_3 a_2 a_1 a_0	E6H

Description: This is a 2-cycle instruction. Control passes to the specified address if the carry bit is not set, that is, equals zero.

Operation:

```
(PC0-7) ← addr          If C = 0
(PC) = (PC) + 2         If C = 1
```

Example:

```
JC0: JNC NOVFLO          ;JUMP TO 'NOVFLO' ROUTINE
                         ;IF C = 0
```

JNI address Jump If Interrupt Input Is Low

Encoding:

1 0 0 0	0 1 1 0	a_7 a_6 a_5 a_4	a_3 a_2 a_1 a_0	86H

Description: This is a 2-cycle instruction. Control passes to the specified address if the interrupt input signal is low (= 0), that is, an external interrupt has been signaled. (This signal initiates an interrupt service sequence if the external interrupt is enabled.)

Operation:

```
(PC0-7) ← addr          If I = 0
(PC) = (PC) + 2         If I = 1
```

Example:

```
LOC 3: JNI EXTINT        ;JUMP TO 'EXTINT' ROUTINE
                         ;IF I = 0
```

JNT0 address Jump If Test 0 is Low

Encoding:

0 0 1 0	0 1 1 0	a_7 a_6 a_5 a_4	a_3 a_2 a_1 a_0	26H

Description: This is a 2-cycle instruction. Control passes to the specified address, if the test 0 signal is low.

Operation:

```
(PC0-7) ← addr          If T0 = 0
(PC) = (PC) + 2         If T0 = 1
```

Example:

```
JT0LOW: JNT0 60          ;JUMP TO LOCATION 60 DEC
                         ;IF T0 = 0
```

JNT1 address Jump If Test 1 Is Low

Encoding: | 0 1 0 0 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | 46H

Description: This is a 2-cycle instruction. Control passes to the specified address, if the test 1 signal is low.

Operation: $(PC_{0-7}) \leftarrow$ addr — If T1 = 0
(PC) = (PC) + 2 — If T1 = 1

JNZ Address Jump If Accumulator Is Not Zero

Encoding: | 1 0 0 1 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | 96H

Description: This is a 2-cycle instruction. Control passes to the specified address if the accumulator contents are nonzero at the time this instruction is executed.

Operation: $(PC_{0-7}) \leftarrow$ addr — If A $\neq$ 0
(PC) = (PC) + 2 — If A = 0

Example:
```
JACCN0: JNZ 0ABH      ;JUMP TO LOCATION 'AB' HEX
                      ;IF ACC VALUE IS NONZERO
```

JTF address Jump If Timer Flag Is Set

Encoding: | 0 0 0 1 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | 16H

Description: This is a 2-cycle instruction. Control passes to the specified address if the timer flag is set to one, that is, the timer/counter register has overflowed. Testing the timer flag resets it to zero. (This overflow initiates an interrupt service sequence if the timer-overflow interrupt is enabled.)

Operation: $(PC_{0-7}) \leftarrow$ addr — If TF = 1
(PC) = (PC) + 2 — If TF = 0

Example:
```
JTF1: JTF TIMER       ;JUMP TO 'TIMER' ROUTINE
                      ;IF TF = 1
```

JT0 address Jump If Test 0 Is High

Encoding: | 0 0 1 1 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | 36H

Description: This is a 2-cycle instruction. Control passes to the specified address if the test 0 signal is high (= 1).

Operation: $(PC_{0-7}) \leftarrow$ addr — If T0 = 1
(PC) = (PC) + 2 — If T0 = 0

Example:
```
JT0HI: JT0 53         ;JUMP TO LOCATION 53 DEC
                      ;IF T0 = 1
```

JT1 address Jump If Test 1 Is High

Encoding: | 0 1 0 1 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | 56H

Description: This is a 2-cycle instruction. Control passes to the specified address if the test 1 signal is high (= 1).

Operation: $(PC_{0-7}) \leftarrow$ addr — If T1 = 1
(PC) = (PC) + 2 — If T1 = 0

Example:
```
JT1HI: JT1 COUNT        ;JUMP TO 'COUNT' ROUTINE
                        ;IF T1 = 1
```

JZ address Jump If Accumulator Is Zero

Encoding: | 1 1 0 0 | 0 1 1 0 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | C6H

Description: This is a 2-cycle instruction. Control passes to the specified address if the accumulator contains all zeros at the time this instruction is executed.

Operation: $(PC_{0-7}) \leftarrow$ addr — If A = 0
(PC) = (PC) + 2 — If A $\neq$ 1

Example:
```
JACCO: JZ 0A3H          ;JUMP TO LOCATION 'A3' HEX
                        ;IF ACC VALUE IS ZERO
```

MOV A,#data Move Immediate Data to Accumulator

Encoding: | 0 0 1 0 | 0 0 1 1 | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 | 23H

Description: This is a 2-cycle instruction. The 8-bit value specified by 'data' is loaded in the accumulator.

Operation: (A) $\leftarrow$ data

Example:
```
MOV A,#0A3H             ;MOVE 'A3' HEX TO ACC
```

MOV A,PSW Move PSW Contents to Accumulator

Encoding: | 1 1 0 0 | 0 1 1 1 | C7H

Description: The contents of the program status word are moved to the accumulator.

Operation: (A) $\leftarrow$ (PSW)

Example: Jump to 'RB1SET' routine if PSW bank switch, bit 4, is set.
```
BSCHK:  MOV A,PSW       ;MOVE PSW CONTENTS TO ACC
        JB4 RB1SET      ;JUMP TO 'RB1SET' IF ACC BIT 4 = 1
```

MOV A,R_r Move Register Contents to Accumulator

Encoding: | 1 1 1 1 | 1 r r r | F8H-FFH

Description: 8-bits of data are removed from working register 'r' into the accumulator.

Operation: (A) ← (Rr) r = 0-7

Example:
```
MAR: MOV A,R3          ;MOVE CONTENTS OF REG 3 TO ACC
```

MOV A,@R_i Move Data Memory Contents to Accumulator

Encoding | 1 1 1 1 | 0 0 0 i | F0H-F1H

Description: The contents of the resident data memory location addressed by bits 0–5** of register 'i' are moved to the accumulator. Register 'i' contents are unaffected.

Operation: (A) ← ((Ri)) i = 0-1

Example: Assume R1 contains 00110110.
```
MADM: MOV A,@R1        ;MOVE CONTENTS OF DATA MEM
                       ;LOCATION 54 TO ACC
```

MOV A,T Move Timer/Counter Contents to Accumulator

Encoding: | 0 1 0 0 | 0 0 1 0 | 42H

Description: The contents of the timer/event-counter register are moved to the accumulator.

Operation: (A) ← (T)

Example: Jump to "EXIT" routine when timer reaches '64', that is, when bit 6 set—assuming initialization 64,
```
TIMCHK: MOV A,T        ;MOVE TIMER CONTENTS TO ACC
        JB6 EXIT       ;JUMP TO 'EXIT' IF ACC BIT 6 = 1
```

MOV PSW,A Move Accumulator Contents to PSW

Encoding: | 1 1 0 1 | 0 1 1 1 | D7H

Description: The contents of the accumulator are moved into the progam status word. All condition bits and the stack pointer are affected by this move.

Operation: (PSW) ← (A)

Example: Move up stack pointer by two memory locations, that is, increment the pointer by one.
```
INCPTR: MOV A,PSW      ;MOVE PSW CONTENTS TO ACC
        INC A          ;INCREMENT ACC BY ONE
        MOV PSW,A      ;MOVE ACC CONTENTS TO PSW
```

** 0–5 in 8048AH/8748H
0–6 in 8049AH/8749H
0–7 in 8050AH

MOV R_r,A Move Accumulator Contents to Register

Encoding: | 1 0 1 0 | 1 r r r | A8H-AFH

Description: The contents of the accumulator are moved to register 'r'.

Operation: (Rr) ← (A) r = 0-7

Example:
```
MRA:  MOV R0,A        ;MOVE CONTENTS OF ACC TO REG 0
```

MOV R_r,#data Move Immediate Data to Register

Encoding: | 1 0 1 1 | 1 r_2 r_1 r_0 | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | B8H-BFH

Description: This is a 2-cycle instruction. The 8-bit value specified by 'data' is moved to register 'r'.

Operation: (Rr) ← data r = 0-7

Examples:
```
MIR4:  MOV R4,#HEXTEN      ;THE VALUE OF THE SYMBOL
                           ;'HEXTEN' IS MOVED INTO REG 4
MIR 5: MOV R5,#PI*(R*R)    ;THE VALUE OF THE EXPRESSION
                           ;'PI*(R*R)' IS MOVED INTO REG 5
MIR 6: MOV R6, #0ADH       ;'AD' HEX IS MOVED INTO REG 6
```

MOV @ R_i,A Move Accumulator Contents to Data Memory

Encoding: | 1 0 1 0 | 0 0 0 i | A0H-A1H

Description: The contents of the accumulator are moved to the resident data memory location whose address is specified by bits 0-5** of register 'i'. Register 'i' contents are unaffected.

Operation: ((Ri)) ← (A) i = 0-1

Example: Assume R0 contains 00000111.
```
MDMA:  MOV @R0,A           ;MOVE CONTENTS OF ACC TO
                           ;LOCATION 7 (REG 7)
```

MOV @ R_i,#data Move Immediate Data to Data memory

Encoding: | 1 0 1 1 | 0 0 0 i | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | B0H-B1H

Description: This is a 2-cycle instruction. The 8-bit value specified by 'data' is moved to the resident data memory location addressed by register 'i', bits 0-5**.

Operation: ((Ri)) ← data i = 0-1

Examples: Move the hexadecimal value AC3F to locations 62-63.
```
MIDM:  MOV R0,#62          ;MOVE '62' DEC TO ADDR REG 0
       MOV @R0,#0ACH       ;MOVE 'AC' HEX TO LOCATION 62
       INC R0              ;INCREMENT REG 0 to '63'
       MOV @R0,#3FH        ;MOVE '3F' HEX TO LOCATION 63
```

** 0-5 in 8048AH/8748H
0-6 in 8049AH/8749H
0-7 in 8050AH

MOV T,A Move Accumulator Contents to Timer/Counter

Encoding: | 0 1 1 0 | 0 0 1 0 | 62H

Description: The contents of the accumulator are moved to the timer/event-counter register.

Operation: (T) ← (A)

Example: Initialize and start event counter.

```
INITEC: CLR A          ;CLEAR ACC TO ZEROS
        MOV T,A        ;MOVE ZEROS TO EVENT COUNTER
        START CNT      ;START COUNTER
```

MOVD A,Pp Move Port 4-7 Data to Accumulator

Encoding: | 0 0 0 0 | 1 1 p p | 0CH-0FH

Description: This is a 2-cycle instruction. Data on 8243 port 'p' is moved (read) to accumulator bits 0-3. Accumulator bits 4-7 are zeroed.

Operation: (0-3) ← (Pp) p = 4-7
(4-7) ← 0

Note: Bits 0-7 of the opcode are used to represent ports 4-7. If you are coding in binary rather than assembly language, the mapping is as follows:

Bits 1 0	Port
0 0	4
0 1	5
1 0	6
1 1	7

Example:

```
INPPT5: MOVD A,P5      ;MOVE PORT 5 DATA TO ACC
                       ;BITS 0-3, ZERO ACC BITS 4-7
```

MOVD Pp,A Move Accumulator Data to Port 4-7

Encoding: | 0 0 1 1 | 1 1 p p | 3CH-3FH

Description: This is a 2-cycle instruction. Data in accumulator bits 0-3 is moved (written) to 8243 port 'p'. Accumulator bits 4-7 are unaffected. (See NOTE above regarding port mapping.)

Operation: (Pp) ← (A_{0-3}) P = 4-7

Example: Move data in accumulator to ports 4 and 5.

```
OUTP45: MOVD P4,A      ;MOVE ACC BITS 0-3 TO PORT 4
        SWAP A         ;EXCHANGE ACC BITS 0-3 and 4-7
        MOVD P5,A      ;MOVE ACC BITS 0-3 TO PORT 5
```

MOVP A,@A Move Current Page Data to Accumulator

Encoding: | 1 0 1 0 | 0 0 1 1 | A3H

Description: The contents of the program memory location addressed by the accumulator are moved to the accumulator. Only bits 0-7 of the program counter are affected, limiting the program memory reference to the current page. The program counter is restored *following* this operation.

Operation: $(PC_{0-7}) \leftarrow (A)$
$(A) \leftarrow ((PC))$
Note: This is a 1-byte, 2-cycle instruction. If it appears in location 255 of a program memory page, @A addresses a location in the *following* page.

Example:
```
MOV128: MOV A,#128      ;MOVE '128' DEC TO ACC
        MOVP A,@A       ;CONTENTS OF 129th LOCATION IN
                        ;CURRENT PAGE ARE MOVED TO ACC
```

MOVP3 A,@A Move Page 3 Data to Accumulator

Encoding: | 1 1 1 0 | 0 0 1 1 | E3H

Description: This is a 2-cycle instruction. The contents of the program memory location (within page 3) addressed by the accumulator are moved to the accumulator. The program counter is restored following this operation.

Operation: $(PC_{0-7}) \leftarrow (A)$
$(PC_{8-11}) \leftarrow 0011$
$(A) \leftarrow ((PC))$

Example: Look up ASCII equivalent of hexadecimal code in table contained at the beginning of page 3. Note that ASCII characters are designated by a 7-bit code; the eighth bit is always reset.

```
TABSCH: MOV A,#0B8H     ;MOVE 'B8' HEX TO ACC (10111000)
        ANL A,#7FH      ;LOGICAL AND ACC TO MASK BIT
                        ;7 (00111000)
        MOVP3 A,@A      ;MOVE CONTENTS OF LOCATION '38'
                        ;HEX IN PAGE 3 TO ACC (ASCII '8')
```

Access contents of location in page 3 labelled TAB1.
Assume current program location is not in page 3.

```
TABSCH: MOV A,#LOW TAB 1 ;ISOLATE BITS 0-7 OF LABEL
                         ;ADDRESS VALUE
        MOVP3 A,@A       ;MOVE CONTENTS OF PAGE 3
                         ;LOCATION LABELED 'TAB1' TO ACC
```

MOVX A,@R_i Move External-Data-Memory Contents to Accumulator

Encoding: | 1 0 0 0 | 0 0 0 i | 80H-81H

Description: This is a 2-cycle instruction. The contents of the external data memory location addressed by register 'i' are moved to the accumulator. Register 'i' contents are unaffected. A read pulse is generated.

Operation: (A) ← ((Ri)) i = 0-1

Example: Assume R1 contains 01110110.

```
MAXDM:  MOVX A,@R1      ;MOVE CONTENTS OF LOCATION
                        ;118 TO ACC
```

MOVX @R_i,A Move Accumulator Contents to External Data Memory

Encoding: | 1 0 0 1 | 0 0 0 i | 90H-91H

Description: This is a 2-cycle instruction. The contents of the accumulator are moved to the external data memory location addressed by register 'i'. Register 'i' contents are unaffected. A write pulse is generated.

Operation: ((Ri)) ← A i = 0-1

Example: Assume R0 contains 11000111.

```
MXDMA:  MOVX @R0,A      ;MOVE CONTENTS OF ACC TO
                        ;LOCATION 199 IN EXPANDED
                        ;DATA MEMORY
```

NOP The NOP Instruction

Encoding: | 0 0 0 0 | 0 0 0 0 | 00H

Description: No operation is performed. Execution continues with the following instruction.

ORL A,R_r Logical OR Accumulator With Register Mask

Encoding: | 0 1 0 0 | 1 r r r | 48H-4FH

Description: Data in the accumulator is logically ORed with the mask contained in working register 'r'.

Operation: (A) ← (A) OR (Rr) r = 0-7

Example:

```
ORREG:  ORL A,R4        ;'OR' ACC CONTENTS WITH
                        ;MASK IN REG 4
```

ORL A,@R_i Logical OR Accumulator With Memory Mask

Encoding: | 0 1 0 0 | 0 0 0 i | 40H-41H

Description: Data in the accumulator is logically ORed with the mask contained in the resident data memory location referenced by register "i", bits 0–5**.

Operation: (A) ← (A) OR ((Ri)) i = 0-1

Example:
```
ORDM: MOV R0,#3FH     ;MOVE '3F' HEX TO REG 0
      ORL A,@R0       ;'OR' AC CONTENTS WITH MASK
                      ;IN LOCATION 63
```

ORL A,#data Logical OR Accumulator With Immediate Mask

Encoding: | 0 1 0 0 | 0 0 1 1 | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | 43H

Description: This is a 2-cycle instruction. Data in the accumulator is logically ORed with an immediately-specified mask.

Operation: (A) ← (A) OR data

Example:
```
ORID: ORL A,#'X'      ;'OR' ACC CONTENTS WITH MASK
                      ;01011000 (ASCII VALUE OF 'X')
```

ORL BUS,#data* Logical OR BUS With Immediate Mask

Encoding: | 1 0 0 0 | 1 0 0 0 | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | 88H

Description: This is a 2-cycle instruction. Data on the BUS port is logically ORed with an immediately-specified mask. This instruction assumes prior specification on an 'OUTL BUS,A' instruction.

Operation: (BUS) ← (BUS) OR data

Example:
```
ORBUS: ORL BUS,#HEXMSK  :'OR' BUS CONTENTS WITH MASK
                        ;EQUAL VALUE OF SYMBOL 'HEXMSK'
```

ORL Pp, #data Logical OR Port 1 or 2 With Immediate Mask

Encoding: | 1 0 0 0 | 1 0 p p | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | 89H-8AH

Description: This is a 2-cycle instruction. Data on port 'p' is logically ORed with an immediately-specified mask.

Operation: (Pp) ← (Pp) OR data p = 1-2

Example:
```
ORP1: ORL P1, #0FFH   ;'OR' PORT 1 CONTENTS WITH MASK
                      ;'FF' HEX (SET PORT 1 TO ALL ONES)
```

* For use with internal program memory ONLY.
** 0–5 in 8048AH/8748H
0–6 in 8049AH/8749H
0–7 in 8050AH

ORLD Pp,A Logical OR Port 4-7 With Accumulator Mask

Encoding: | 1 0 0 0 | 1 1 p p | 8CH-8FH

Description: This is a 2-cycle instruction. Data on port 'p' is logically ORed with the digit mask contained in accumulator bits 0-3.

Operation: (Pp) ← (Pp) OR (A_{0-3}) p = 4-7

Example:
```
ORP7: ORLD P7,A      ;'OR' PORT 7 CONTENTS WITH ACC
                     ;BITS 0-3
```

OUTL BUS,A* Output Accumulator Data to BUS

Encoding: | 0 0 0 0 | 0 0 1 0 | 02H

Description: This is a 2-cycle instruction. Data residing in the accumulator is transferred (written) to the BUS port and latched. The latched data remains valid until altered by another OUTL instruction. Any other instruction requiring use of the BUS port (except INS) destroys the contents of the BUS latch. This includes expanded memory operations (such as the MOVX instruction). Logical operations on BUS data (AND, OR) assume the OUTL BUS,A instruction has been issued previously.

Operation: (BUS) ← (A)

Example:
```
OUTLBP: OUTL BUS, A      ;OUTPUT ACC CONTENTS TO BUS
```

OUTL Pp,A Output Accumulator Data to Port 1 or 2

Encoding: | 0 0 1 1 | 1 0 p p | 39H-3AH

Description: This is a 2-cycle instruction. Data residing in the accumulator is transferred (written) to port 'p' and latched.

Operation: (Pp) ← (A) p = 1-2

Example:
```
OUTLP: MOV A,R7      ;MOVE REG 7 CONTENTS TO ACC
       OUTL P2,A     ;OUTPUT ACC CONTENTS TO PORT 2
       MOV A, R6     ;MOV REG 6 CONTENTS TO ACC
       OUTL P1,A     ;OUTPUT ACC CONTENTS TO PORT 1
```

* For use with internal program memory ONLY.

RET Return Without PSW Restore

Encoding: | 1 0 0 0 | 0 0 1 1 | 83H

Description: This is a 2-cycle instruction. The stack pointer (PSW bits 0-2) is decremented. The program counter is then restored from the stack. PSW bits 4-7 are not restored.

Operation: (SP) ← (SP)-1
(PC) ← ((SP))

RETR Return with PSW Restore

Encoding: | 1 0 0 1 | 0 0 1 1 | 93H

Description: This is a 2-cycle instruction. The stack pointer is decremented. The program counter and bits 4-7 of the PSW are then restored from the stack. Note that RETR should be used to return from an interrupt, but should not be used within the interrupt service routine as it signals the end of an interrupt routine by resetting the Interrupt in Progress flip-flop.

Operation: (SP) ← (SP)-1
(PC) ← ((SP))
(PSW 4-7) ← ((SP))

RL A Rotate Left without Carry

Encoding: | 1 1 1 0 | 0 1 1 1 | E7H

Description: The contents of the accumulator are rotated left one bit. Bit 7 is rotated into the bit 0 position.

Operation: (An + 1) ← (An)
(A0) ← (A7) n = 0-6

Example: Assume accumulator contains 10110001.

```
RLNC: RL A          ;NEW ACC CONTENTS ARE 01100011
```

RLC A Rotate Left through Carry

Encoding: | 1 1 1 1 | 0 1 1 1 | F7H

Description: The contents of the accumulator are rotated left one bit. Bit 7 replaces the carry bit; the carry bit is rotatd into the bit 0 position.

Operation: (An + 1) ← (An)
n = 0-6
(A0) ← (C)
(C) ← (A7)

Example: Assume accumulator contains a 'signed' number; isolate sign without changing value.

```
RLTC: CLR C         ;CLEAR CARRY TO ZERO
      RLC A         ;ROTATE ACC LEFT, SIGN
                    ;BIT (7) IS PLACED IN CARRY
      RR A          ;ROTATE ACC RIGHT — VALUE
                    ;(BITS 0-6) IS RESTORED,
                    ;CARRY UNCHANGED, BIT 7
                    ;IS ZERO
```

RR A Rotate Right without Carry

Encoding: | 0 1 1 1 | 0 1 1 1 | 77H

Description: The contents of the accumulator are rotated right one bit. Bit 0 is rotated into the bit 7 position.

Operation: (An) ← (An + 1) n = 0-6
(A7) ← (A0)

Example: Assume accumulator contains 10110001.

```
RRNC: RR A          ;NEW ACC CONTENTS ARE 11011000
```

RRC A Rotate Right through Carry

Encoding: | 0 1 1 0 | 0 1 1 1 | 67H

Description: The contents of the accumulator are rotated right one bit. Bit 0 replaces the carry bit; the carry bit is rotated into the bit 7 position.

Operation: (An) ← (An + 1) n = 0-6
(A7) ← (C)
(C) ← (A_0)

Example: Assume carry is not set and accumulator contains 10110001.

```
RRTC: RRC A          ;CARRY IS SET AND ACC
                     ;CONTAINS 01011000
```

SEL MB0 Select Memory Bank 0

Encoding: | 1 1 1 0 | 0 1 0 1 | E5H

Description: PC bit 11 is set to zero on next JMP or CALL instruction. All references to program memory addresses fall within the range 0-2047.

Operation: (DBF) ← 0

Example: Assume program counter contains 834 Hex.

```
SEL MB0              ;SELECT MEMORY BANK 0
JMP $+20             ;JUMP TO LOCATION 58 HEX
```

SEL MB1 Select Memory Bank 1

Encoding: | 1 1 1 1 | 0 1 0 1 | F5H

Description: PC bit 11 is set to one on next JMP or CALL instruction. All references to program memory addresses fall within the range 2048-4095.

Operation: (DBF) ← 1

SEL RB0 Select Register Bank 0

Encoding: | 1 1 0 0 | 0 1 0 1 | C5H

Description: PSW bit 4 is set to zero. References to working registers 0-7 address data memory locations 0-7. This is the recommended setting for normal program execution.

Operation: (BS) ← 0

SEL RB1 Select Register Bank 1

Encoding: | 1 1 0 1 | 0 1 0 1 | D5H

Description: PSW bit 4 is set to one. References to working registers 0-7 address data memory locations 24-31. This is the recommended setting for interrupt service routines, since locations 0-7 are left intact. The setting of PSW bit 4 in effect at the time of an interrupt is restored by the RETR instruction when the interrupt service routine is completed.

Operation: (BS) ← 1

Example: Assume an external interrupt has occurred, control has passed to program memory location 3, and PSW bit 4 was zero before the interrupt.

Operation:

```
LOC3:  JNI INIT          ;JUMP TO ROUTINE 'INIT' IF
                         ;INTERRUPT INPUT IS ZERO
INIT:  MOV R7,A          ;MOVE ACC CONTENTS TO
                         ;LOCATION 7
       SEL RB1           ;SELECT REG BANK 1
       MOV R7,#0FAH      ;MOVE 'FA' HEX TO LOCATION 31
       .
       .
       .
       SEL RB0           ;SELECT REG BANK 0
       MOV A,R7          ;RESTORE ACC FROM LOCATION 7
       RETR              ;RETURN — RESTORE PC AND PSW
```

STOP TCNT Stop Timer/Event-Counter

Encoding: | 0 1 1 0 | 0 1 0 1 | 65H

Description: This instruction is used to stop both time accumulation and event counting.

Example: Disable interrupt, but jump to interrupt routine after eight overflows and stop timer. Count overflows in register 7.

```
START: DIS TCNTI          ;DISABLE TIMER INTERRUPT
       CLR A              ;CLEAR ACC TO ZEROS
       MOV T,A            ;MOVE ZEROS TO TIMER
       MOV R7,A           ;MOVE ZEROS TO REG 7
       STRT T             ;START TIMER
MAIN:  JTF COUNT          ;JUMP TO ROUTINE 'COUNT'
                          ;IF TF = 1 AND CLEAR TIMER FLAG
       JMP MAIN           ;CLOSE LOOP
COUNT: INC R7             ;INCREMENT REG 7
       MOV A,R7           ;MOVE REG 7 CONTENTS TO ACC
       JB3 INT            ;JUMP TO ROUTINE 'INT' IF ACC
                          ;BIT 3 IS SET (REG 7 = 8)
       JMP MAIN           ;OTHERWISE RETURN TO ROUTINE
                          ;MAIN
       .
       .
       .
INT:   STOP TCNT          ;STOP TIMER
       JMP 7H             ;JUMP TO LOCATION 7 (TIMER)
                          ;INTERRUPT ROUTINE
```

STRT CNT Start Event Conter

Encoding: | 0 1 0 0 | 0 1 0 1 | 45H

Description: The test 1 (T1) pin is enabled as the event-counter input and the counter is started. The event-counter register is incremented with each high-to-low transition on the T1 pin.

Example: Initialize and start event counter. Assume overflow is desired with first T1 input.

```
STARTC: EN TCNTI          ;ENABLE COUNTER INTERRUPT
        MOV A,#0FFH       ;MOVE 'FF'HEX (ONES) TO ACC
        MOV T,A           ;MOVES ONES TO COUNTER
        STRT CNT          ;ENABLE T1 AS COUNTER
                          ;INPUT AND START
```

STRT T Start Timer

Encoding: | 0 1 0 1 | 0 1 0 1 | 55H

Description: Timer accumulation is initiated in the timer register. The register is incremented every 32 instruction cycles. The prescaler which counts the 32 cycles is cleared but the timer register is not.

Example: Initialize and start timer.

```
STARTT: CLR A          ;CLEAR ACC TO ZEROS
        MOV T,A        ;MOVE ZEROS TO TIMER
        EN TCNTI       ;ENABLE TIMER INTERRUPT
        STRT T         ;START TIMER
```

SWAP A Swap Nibbles within Accumulator

Encoding: | 0 1 0 0 | 0 1 1 1 | 47H

Description: Bits 0-3 of the accumulator are swapped with bits 4-7 of the accumulator.

Operation: $(A_{4-7}) \rightleftarrows (A_{0-3})$

Example: Pack bits 0-3 of locations 50-51 into location 50.

```
PCKDIG: MOV R0, #50     ;MOVE '50' DEC TO REG 0
        MOV R1, #51     ;MOVE '51' DEC TO REG 1
        XCHD A,@R0      ;EXCHANGE BITS 0-3 OF ACC
                        ;AND LOCATION 50
        SWAP A          ;SWAP BITS 0-3 AND 4-7 OF ACC
        XCHD A,@R1      ;EXCHANGE BITS 0-3 OF ACC AND
                        ;LOCATION 51
        MOV @R0,A       ;MOVE CONTENTS OF ACC TO
                        ;LOCATION 50
```

XCH A,R_r Exchange Accumulator-Register Contents

Encoding: | 0 0 1 0 | 1 r r r | 28H-2FH

Description: The contents of the accumulator and the contents of working register 'r' are exchanged.

Operation: $(A) \rightleftarrows (Rr)$ r = 0-7

Example: Move PSW contents to Reg 7 without losing accumulator contents.

```
XCHAR7: XCH A,R7        ;EXCHANGE CONTENTS OF REG 7
                        ;AND ACC
        MOV A, PSW      ;MOVE PSW CONTENTS TO ACC
        XCH A,R7        ;EXCHANGE CONTENTS OF REG 7
                        'AND ACC AGAIN
```

XCH A,@R_i Exchange Accumulator and Data Memory Contents

Encoding: | 0 0 1 0 | 0 0 0 i | 20H-21H

Description: The contents of the accumulator and the contents of the resident data memory location addressed by bits 0-5** of register 'i' are exchanged. Register 'i' contents are unaffected.

Operation: (A) ⇆ ((Ri)) i = 0-1

Example: Decrement contents of location 52.

```
DEC52: MOV R0,#52      ;MOVE '52' DEC TO ADDRESS REG 0
       XCH A,@R0       ;EXCHANGE CONTENTS OF ACC
                       ;AND LOCATION 52
       DEC A           ;DECREMENT ACC CONTENTS
       XCH A,@R0       ;EXCHANGE CONTENTS OF ACC
                       ;AND LOCATION 52 AGAIN
```

XCHD A,@R_i Exchange Accumulator and Data Memory 4-Bit Data

Encoding: | 0 0 1 1 | 0 0 0 i | 30H-31H

Description: This instruction exchanges bits 0-3 of the accumulator with bits 0-3 of the data memory location addressed by bits 0-5** of register 'i'. Bits 4-7 of the accumulator, bits 4-7 of the data memory location, and the contents of register 'i' are unaffected.

Operation: (A_{0-3}) ⇆ ((Ri0-3)) i = 0-1

Example: Assume program counter contents have been stacked in locations 22-23.

```
XCHNIB: MOV R0,#23     ;MOVE '23' DEC TO REG 0
        CLR A          ;CLEAR ACC TO ZEROS
        XCHD A,@R0     ;EXCHANGE BITS 0-3 OF ACC AND
                       ;LOCATION 23 (BTS 8-11 OF PC ARE
                       ;ZEROED, ADDRESS REFERS
                       :TO PAGE 0)
```

XRL A,R_r Logical XOR Accumulator With Register Mask

Encoding: | 1 1 0 1 | 1 r r r | D8H-DFH

Description: Data in the accumulator is EXCLUSIVE ORed with the mask contained in working register 'r'.

Operation: (A) ← (A) XOR (Rr) r = 0-7

Example:

```
XORREG: XRL A,R5        ;'XOR' ACC CONTENTS WITH
                        ;MASK IN REG 5
```

** 0-5 in 8048AH/8748H
0-6 in 8049AH/8749H
0-7 in 8050AH

XRL A,@R_i Logical XOR Accumulator With Memory Mask

Encoding: | 1 1 0 1 | 0 0 0 i | D0H-D1H

Description: Data in the accumulator is EXCLUSIVE ORed with the mask contained in the data memory location addressed by register 'i', bits 0–5.**

Operation: (A) ← (A) XOR ((Ri)) i = 0-1

Example:
```
XORDM: MOV R1,#20H      ;MOVE '20' HEX TO REG 1
       XRL A,@R1        ;'XOR' ACC CONTENTS WITH MASK
                        ;IN LOCATION 32
```

XRL A,#data Logical XOR Accumulator With Immediate Mask

Encoding: | 1 1 0 1 | 0 0 1 1 | | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 | D3H

Description: This is a 2-cycle instruction. Data in the accumulator is EXCLUSIVE ORed with an immediately-specified mask.

Operation: (A) ← (A) XOR data

Example:
```
XORID: XOR A,#HEXTEN    ;XOR CONTENTS OF ACC WITH MASK
                        ;EQUAL VALUE OF SYMBOL 'HEXTEN'
```

** 0–5 in 8048AH/8748H
0–6 in 8049AH/8749H
0–7 in 8050AH

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MCS®-48 Data Sheets

4

8243
MCS®-48 INPUT/OUTPUT EXPANDER

■ 0°C TO 70°C Operation

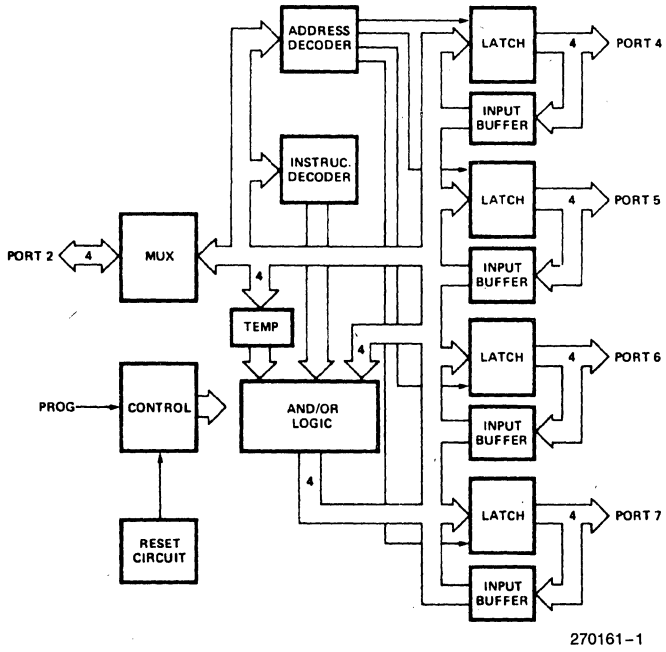

Figure 1. 8243 Block Diagram

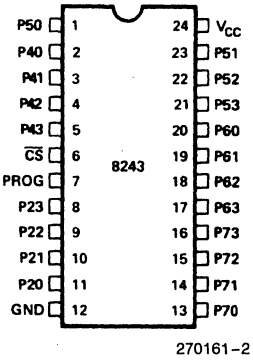

Figure 2. 8243 Pin Configuration

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November 1990
Order Number: 270161-001

Table 1. Pin Description

Symbol	Pin No.	Function
PROG	7	Clock Input. A high to low transition on PROG signifies that address and control are available on P20–P23, and a low to high transition signifies that data is available on P20–P23.
$\overline{CS}$	6	Chip Select Input. A high on CS inhibits any change of output or internal status.
P20–P23	11–8	Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition, P2 contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.
GND	12	0V supply.
P40–P43	2–5	Four (4) bit bi-directional I/O ports.
P50–P53 P60–P63 P70–P73	1, 23–21 20–17 13–16	May be programmed to be input (during read), low impedance latched output (after write), or a tri-state (after read). Data on pins P20–P23 may be directly written, ANDed or ORed with previous data.
V_{CC}	24	+5V supply.

FUNCTIONAL DESCRIPTION

General Operation

The 8243 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as Ports 4–7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the 8048 and the 8243 occurs over Port 2 (P20–P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles:

The first containing the "op code" and port address and the second containing the actual 4-bits of data. A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional 8243's may be added to the 4-bit bus and chip selected using additional output lines from the 8048/8748/8035.

Power On Initialization

Initial application of power to the device forces input/output Ports 4, 5, 6, and 7 to the tri-state and Port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes the device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

Write Modes

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data, AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input Port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on Port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input Port 2

on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while Port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 8243 output. A read of any port will leave that port in a high impedance state.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin
with Respect to Ground.....−0.5V to +7V
Power Dissipation .....1 Watt

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

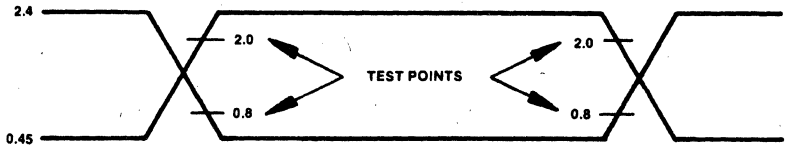
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage Ports 4–7			0.45	V	I_{OL} = 4.5 mA*
V_{OL2}	Output Low Voltage Port 7			1	V	I_{OL} = 20 mA
V_{OH1}	Output High Voltage Ports 4–7	2.4			V	I_{OH} = 240 μA
I_{IL1}	Input Leakage Ports 4–7	−10		20	μA	V_{in} = V_{CC} to 0V
I_{IL2}	Input Leakage Port 2, CS, PROG	−10		10	μA	V_{in} = V_{CC} to 0V
V_{OL3}	Output Low Voltage Port 2			0.45	V	I_{OL} = 0.6 mA
I_{CC}	V_{CC} Supply Current		10	20	mA	(Note 1)
V_{OH2}	Output Voltage Port 2	2.4				I_{OH} = 100 μA
I_{OL}	Sum of All I_{OL} From 16 Outputs			72	mA	4.5 mA Each Pin

*Refer to Figure 3 for additional sink current capability.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min	Max	Units	Test Conditions
t_A	Code Valid before PROG	50		ns	80 pF Load
t_B	Code Valid after PROG	60		ns	20 pF Load
t_C	Data Valid before PROG	200		ns	80 pF Load
t_D	Data Valid after PROG	20		ns	20 pF Load
t_H	Floating after PROG	0	150	ns	20 pF Load
t_K	PROG Negative Pulse Width	700		ns	
t_{CS}	CS Valid before/after PROG	50		ns	
t_{PO}	Ports 4–7 Valid after PROG		700	ns	100 pF Load
t_{LP1}	Ports 4–7 Valid before/after PROG	100		ns	
t_{ACC}	Port 2 Valid after PROG		650	ns	80 pF Load

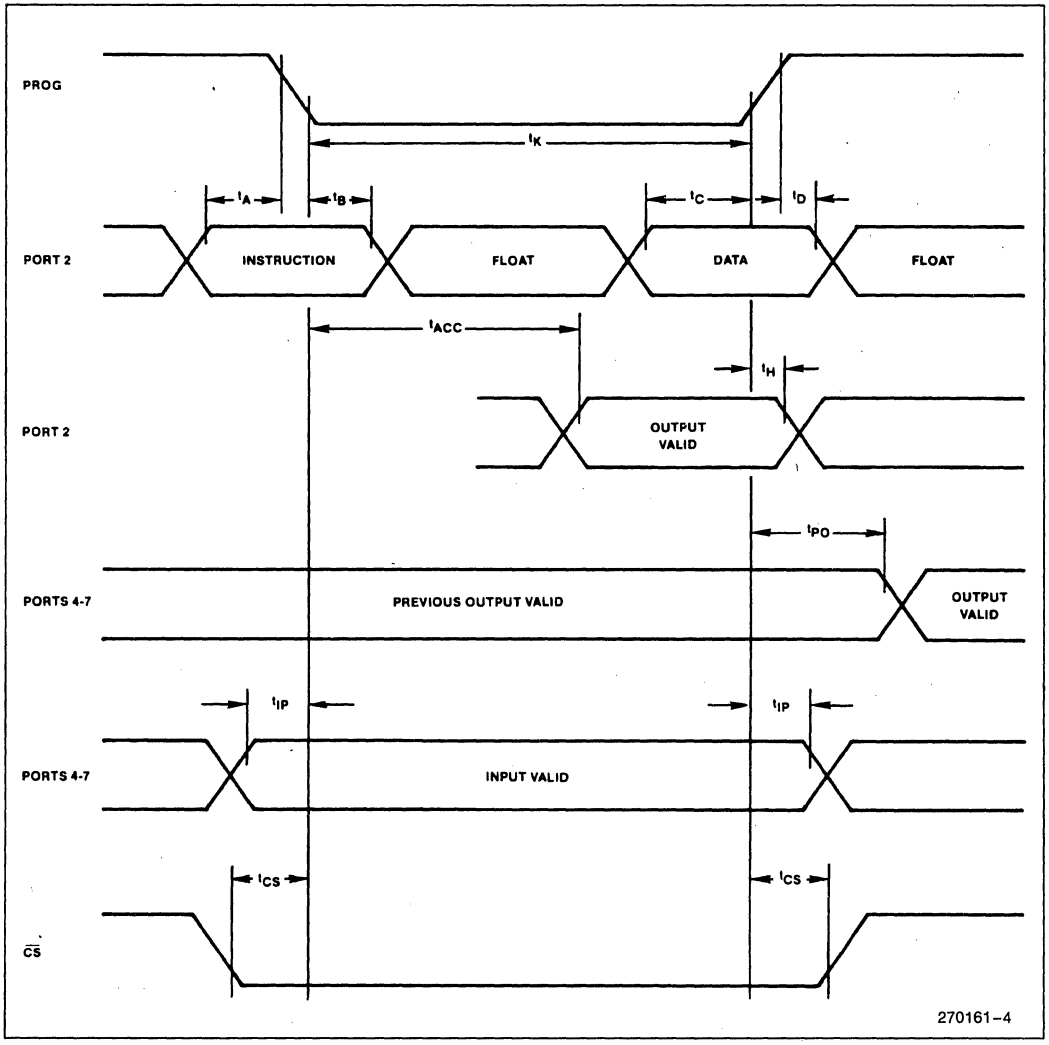
NOTE:
1. I_{CC} (−40°C to 85°C EXPRESS options) 15 mA typical/25 mA maximum.



270161-3

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Output timing measurements are made at 2.0V for Logic "1" and 0.8V for a Logic "0".

WAVEFORMS


PROG
t_K
t_A
t_B
t_C
t_D
PORT 2
INSTRUCTION
FLOAT
DATA
FLOAT
t_{ACC}
t_H
PORT 2
OUTPUT VALID
t_{PO}
PORTS 4-7
PREVIOUS OUTPUT VALID
OUTPUT VALID
t_{IP}
t_{IP}
PORTS 4-7
INPUT VALID
t_{CS}
t_{CS}
$\overline{CS}$
270161-4

4

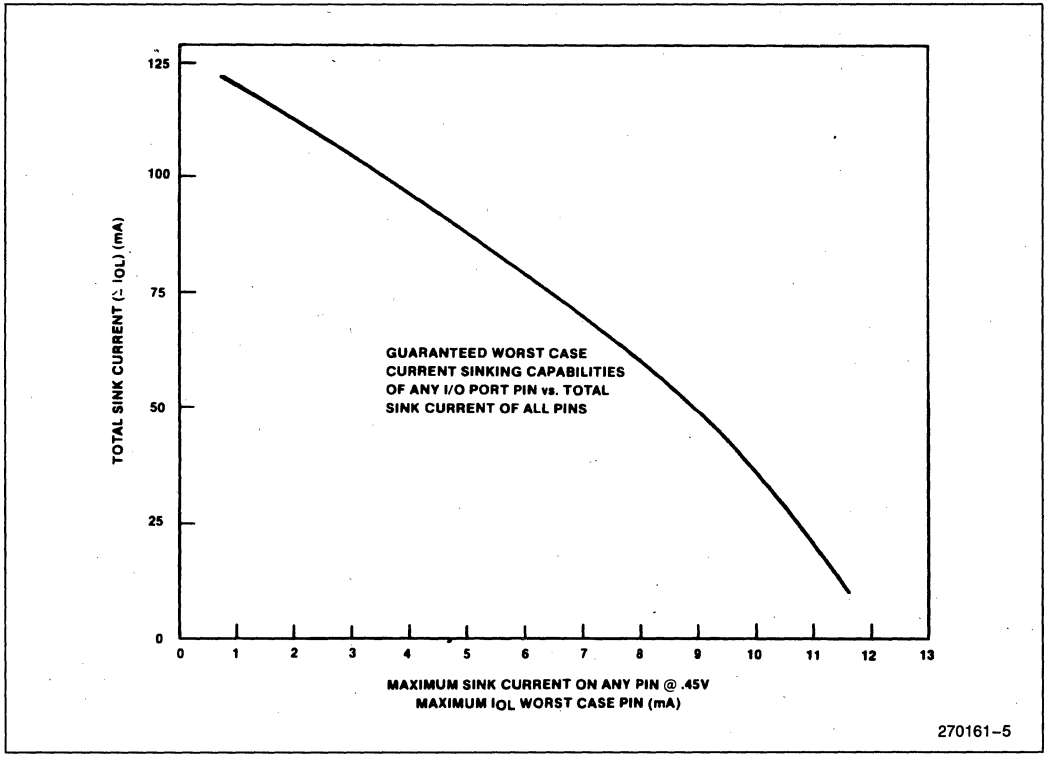


Figure 3. 8243 Current Sink Capability

Sink Capability

The 8243 can sink 5 mA @ 0.45V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 9 mA @ 0.45V (if any lines are to sink 9 mA the total I_{OL} must not exceed 45 mA or five 9 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

$I_{OL} = 5 \times 1.6\ mA = 8\ mA$

$\epsilon I_{OL} = 60$ mA from curve

pins $= 60\ mA \div 8\ mA/pin = 7.5 = 7$

In this case, 7 lines can sink 8 mA for a total of 56 mA. This leaves 4 mA sink current capability which can be divided in any way among the remaining 8 I/O lines of the 8243.

NOTE:

A10 to 50 KΩ pullup resistor to +5V should be added to 8243 outputs when driving to 5V CMOS directly.

Example: This example shows how the use of the 20 mA sink capability of Port 7 affects the sinking capability of the other I/O lines.

An 8243 will drive the following loads simultaneously.

2 loads—20 mA @ 1V (Port 7 only)

8 loads—4 mA @ 0.45V

6 loads—3.2 mA @ 0.45V

Is this within the specified limits?

$\epsilon I_{OL} = (2 \times 20) + (8 \times 4) + (6 \times 3.2) = 91.2$ mA.

From the curve: for $I_{OL} = 4$ mA, $\epsilon I_{OL} \cong 93$ mA. Since 91.2 mA < 93 mA the loads are within specified limits.

Although the 20 mA @ 1V loads are used in calculating ϵI_{OL}, it is the largest current required @ 0.45V which determines the maximum allowable ϵI_{OL}.

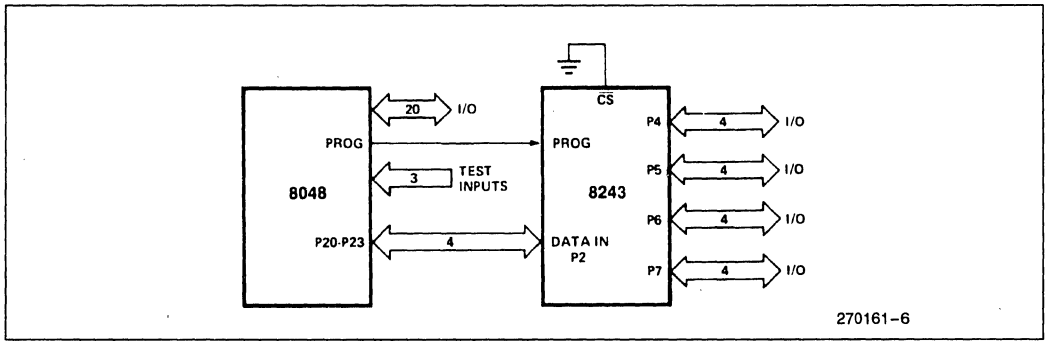


Figure 4. Expander Interface

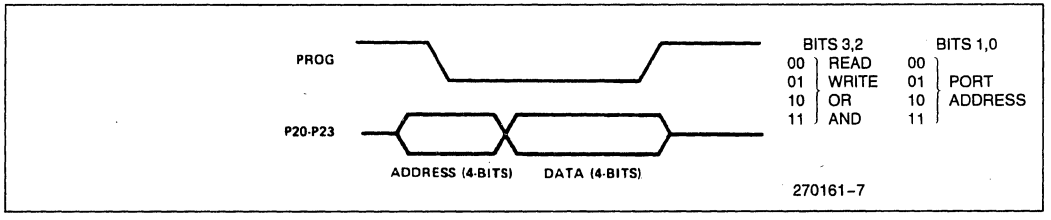


Figure 5. Output Expander Timing

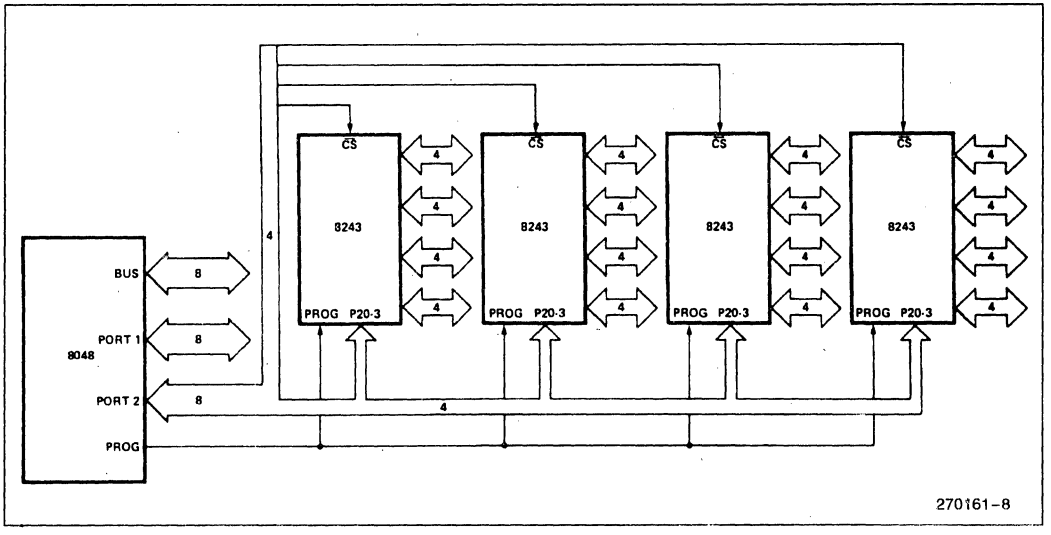


Figure 6. Using Multiple 8243's

P8748H/P8749H
8048AH/8035AHL/8049AH/8039AHL/8050AH/8040AHL
HMOS SINGLE-COMPONENT 8-BIT MICROCONTROLLER

- **High Performance HMOS II**
- **Interval Time/Event Counter**
- **Two Single Level Interrupts**
- **Single 5-Volt Supply**
- **Over 96 Instructions; 90% Single Byte**
- **Programmable ROMs Using 21V**
- **Easily Expandable Memory and I/O**
- **Up to 1.36 μs Instruction Cycle All Instructions 1 or 2 Cycles**

The Intel MCS®-48 family are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

The family contains 27 I/O lines, an 8-bit timer/counter, and on-board oscillator/clock circuits. For systems that require extra capability, the family can be expanded using MCS®-80/MCS®-85 peripherals.

These microcontrollers are available in both masked ROM and ROMless versions as well as a new version, The Programmable ROM. The Programmable ROM provides the user with the capability of a masked ROM while providing the flexibility of a device that can be programmed at the time of requirement and to the desired data. Programmable ROM's allow the user to lower inventory levels while at the same time decreasing delay times and code risks.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting of mostly single byte instructions and no instructions over 2 bytes in length.

Device	Internal	Memory	RAM STANDBY
8050AH	4K x 8 ROM	256 x 8 RAM	yes
8049AH	2K x 8 ROM	128 x 8 RAM	yes
8048AH	1K x 8 ROM	64 x 8 RAM	yes
8040AHL	None	256 x 8 RAM	yes
8039AHL	None	128 x 8 RAM	yes
8035AHL	None	64 x 8 RAM	yes
P8749H	2K x 8 Programmable ROM	128 x 8 RAM	no
P8748H	1K x 8 Programmable ROM	64 x 8 RAM	no

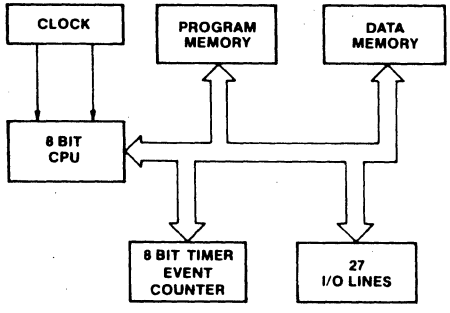


Figure 1. Block Diagram

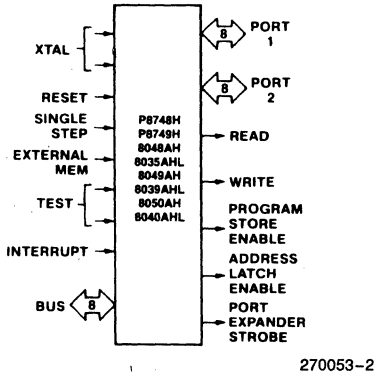


Figure 2. Logic Symbol

August 1989
Order Number: 270053-003

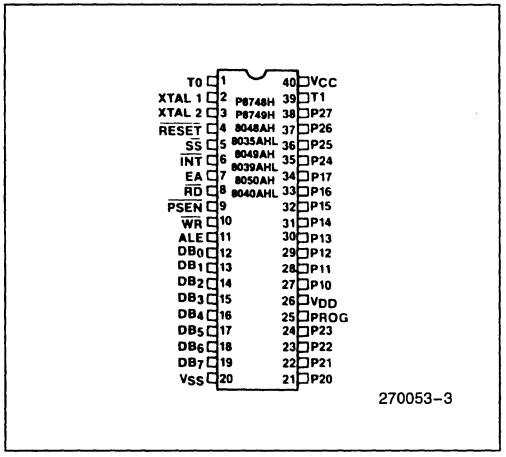


Figure 3. Pin Configuration

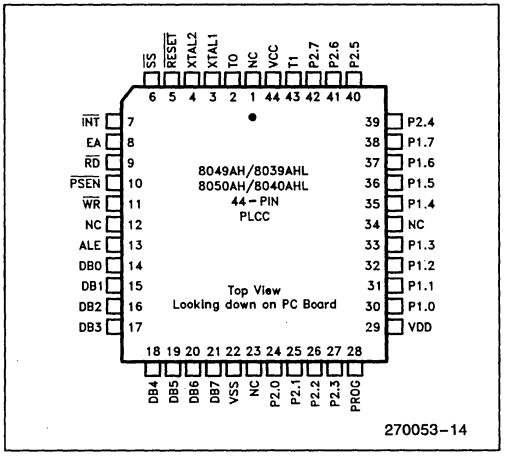


Figure 4. Pad Configuration

Table 1. Pin Description

Symbol	Pin No.	Function	Device
V_{SS}	20	Circuit GND potential.	All
V_{DD}	26	+5V during normal operation.	All
		Low power standby pin.	8048AH 8035AHL 8049AH 8039AHL 8050AH 8040AHL
		Programming power supply (+21V).	P8748H P8749H
V_{CC}	40	Main power supply; +5V during operation and programming.	All
PROG	25	Output strobe for 8243 I/O expander.	All
		Program pulse (+18V) input pin During Programming.	P8748H P8749H
P10–P17 Port 1	27–34	8-bit quasi-bidirectional port.	All
P20–P23 P24–P27 Port 2	21–24 35–38	8-bit quasi-bidirectional port. P20–P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.	All
DB0–DB7 BUS	12–19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.	All
T0	1	Input pin testable using the conditional transfer instruction JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.	All
		Used during programming.	P8748H P8749H

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Table 1. Pin Description (Continued)

Symbol	Pin No.	Function	Device
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.	All
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) interrupt must remain low for at least 3 machine cycles for proper operation.	All
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)	All
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})	All
		Used during power down.	8048AH 8035AHL 8049AH 8039AHL 8050AH 8040AHL
		Used during programming.	P8748H P8749H
		Used during ROM verification.	8048AH P8748H 8049AH P8749H 8050AH
$\overline{WR}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.	All
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.	All
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)	All
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction.	All
		(Active low) Used in sync mode.	8048AH 8035AHL 8049AH 8039AHL 8050AH 8040AHL
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug. (Active high)	All
		Used during (18V) programming.	P8748H P8749H
		Used during ROM verification (12V).	8048AH 8049AH 8050AH
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})	All
XTAL2	3	Other side of crystal input.	All

Table 2. Instruction Set

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, #data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, #data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A, @R	Or data memory to A	1	1
ORL A, #data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL A, #data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, #data	And immediate to port	2	2
ORL P, #data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, #data	And immediate to BUS	2	2
ORL BUS, #data	Or immediate to BUS	2	2
MOVD A, P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JNI addr	Jump on $\overline{INT}$ = 0	2	2
JBb addr	Jump on accumulator bit	2	2

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Table 2. Instruction Set (Continued)

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, #data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and data memory	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/counter interrupt	1	1
DIS TCNTI	Disable timer/counter interrupt	1	1

Control

Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on any Pin with Respect to Ground . . . . . −0.5V to +7V
Power Dissipation 1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions	Device
		Min	Typ	Max			
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, X1, X2)	−0.5		0.8	V		All
V_{IL1}	Input Low Voltage ($\overline{RESET}$, X1, X2)	−0.5		0.6	V		All
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.0		V_{CC}	V		All
V_{IH1}	Input High Voltage (X1, X2, $\overline{RESET}$)	3.8		V_{CC}	V		All
V_{OL}	Output Low Voltage (BUS)			0.45	V	I_{OL} = 2.0 mA	All
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			0.45	V	I_{OL} = 1.8 mA	All
V_{OL2}	Output Low Voltage (PROG)			0.45	V	I_{OL} = 1.0 mA	All
V_{OL3}	Output Low Voltage (All Other Outputs)			0.45	V	I_{OL} = 1.6 mA	All
V_{OH}	Output High Voltage (BUS)	2.4			V	I_{OH} = −400 μA	All
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH} = −100 μA	All
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = −40 μA	All

4

D.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$ (Continued)

Symbol	Parameter	Limits			Unit	Test Conditions	Device
		Min	Typ	Max			
I_{L1}	Leakage Current (T1, $\overline{INT}$)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$	All
I_{LI1}	Input Leakage Current (P10–P17, P20–P27, EA, $\overline{SS}$)			−500	μA	$V_{SS} + 0.45 \le V_{IN} \le V_{CC}$	All
I_{LI2}	Input Leakage Current $\overline{RESET}$	−10		−300	μA	$V_{SS} \le V_{IN} \le 3.8$	All
I_{LO}	Leakage Current (BUS, T0) (High Impedance State)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$	All
I_{DD}	V_{DD} Supply Current (RAM Standby)		3	5	mA		8048AH 8035AHL
			4	7	mA		8049AH 8039AHL
			5	10	mA		8050AH 8040AHL
$I_{DD} + I_{CC}$	Total Supply Current*		30	65	mA		8048AH 8035AHL
			35	70	mA		8049AH 8039AHL
			40	80	mA		8050AH 8040AHL
			30	100	mA		P8748H
			50	110	mA		P8749H
V_{DD}	RAM Standby Voltage	2.2		5.5	V	Standby Mode Reset $\le V_{IL1}$	8048AH 8035AH
		2.2		5.5	V		8049AH 8039AH
		2.2		5.5	V		8050AH 8040AHL

*$I_{CC} + I_{DD}$ are measured with all outputs in their high impedance state; $\overline{RESET}$ low; 11 MHz crystal applied; $\overline{INT}$, $\overline{SS}$, and EA floating.

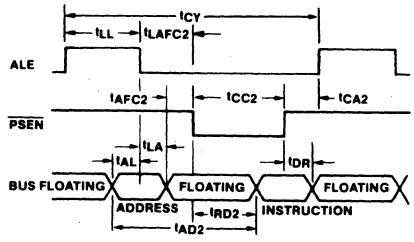
A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	f (t) (Note 3)	11 MHz		Unit	Conditions (Note 1)
			Min	Max		
t	Clock Period	1/xtal freq	90.9	1000	ns	(Note 3)
t_{LL}	ALE Pulse Width	3.5t−170	150		ns	
t_{AL}	Addr Setup to ALE	2t−110	70		ns	(Note 2)
t_{LA}	Addr Hold from ALE	t−40	50		ns	
t_{CC1}	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	7.5t−200	480		ns	
t_{CC2}	Control Pulse Width ($\overline{PSEN}$)	6t−200	350		ns	
t_{DW}	Data Setup before $\overline{WR}$	6.5t−200	390		ns	
t_{WD}	Data Hold after $\overline{WR}$	t−50	40		ns	
t_{DR}	Data Hold ($\overline{RD}$, $\overline{PSEN}$)	1.5t−30	0	110	ns	
t_{RD1}	$\overline{RD}$ to Data in	6t−170		375	ns	
t_{RD2}	$\overline{PSEN}$ to Data in	4.5t−170		240	ns	
t_{AW}	Addr Setup to $\overline{WR}$	5t−150	300		ns	
t_{AD1}	Addr Setup to Data ($\overline{RD}$)	10.5t−220		730	ns	
t_{AD2}	Addr Setup to Data ($\overline{PSEN}$)	7.5t−200		460	ns	
t_{AFC1}	Addr Float to $\overline{RD}$, $\overline{WR}$	2t−40	140		ns	(Note 2)
t_{AFC2}	Addr Float to $\overline{PSEN}$	0.5t−40	10		ns	(Note 2)
t_{LAFC1}	ALE to Control ($\overline{RD}$, $\overline{WR}$)	3t−75	200		ns	
t_{LAFC2}	ALE to Control ($\overline{PSEN}$)	1.5t−75	60		ns	
t_{CA1}	Control to ALE ($\overline{RD}$, $\overline{WR}$, PROG)	t−65	25		ns	
t_{CA2}	Control to ALE ($\overline{PSEN}$)	4t−70	290		ns	
t_{CP}	Port Control Setup to PROG	1.5t−80	50		ns	
t_{PC}	Port Control Hold to PROG	4t−260	100		ns	
t_{PR}	PROG to P2 Input Valid	8.5t−120		650	ns	
t_{PF}	Input Data Hold from PROG	1.5t	0	140	ns	
t_{DP}	Output Data Setup	6t−290	250		ns	
t_{PD}	Output Data Hold	1.5t−90	40		ns	
t_{PP}	PROG Pulse Width	10.5t−250	700		ns	
t_{PL}	Port 2 I/O Setup to ALE	4t−200	160		ns	
t_{LP}	Port 2 I/O Hold to ALE	0.5t−30	15		ns	
t_{PV}	Port Output from ALE	4.5t+100		5.0	ns	
t_{0PRR}	T0 Rep Rate	3t	270		ns	
t_{CY}	Cycle Time	15t	1.36	15.0	μs	

NOTES:
1. Control outputs: $C_L = 80$ pF. BUS Outputs: $C_L = 150$ pF.
2. BUS High Impedance Load 20 pF
3. f(t) assumes 50% duty cycle on X1, X2. Max clock period is for a 1 MHz crystal input.

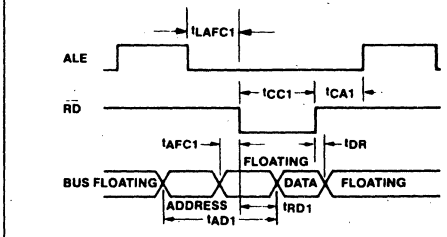
WAVEFORMS

INSTRUCTION FETCH FROM PROGRAM MEMORY



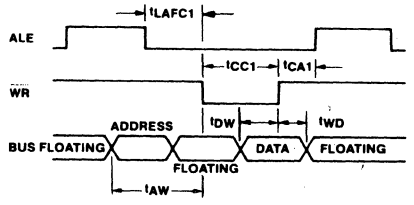
270053-4

READ FROM EXTERNAL DATA MEMORY



270053-5

WRITE TO EXTERNAL DATA MEMORY



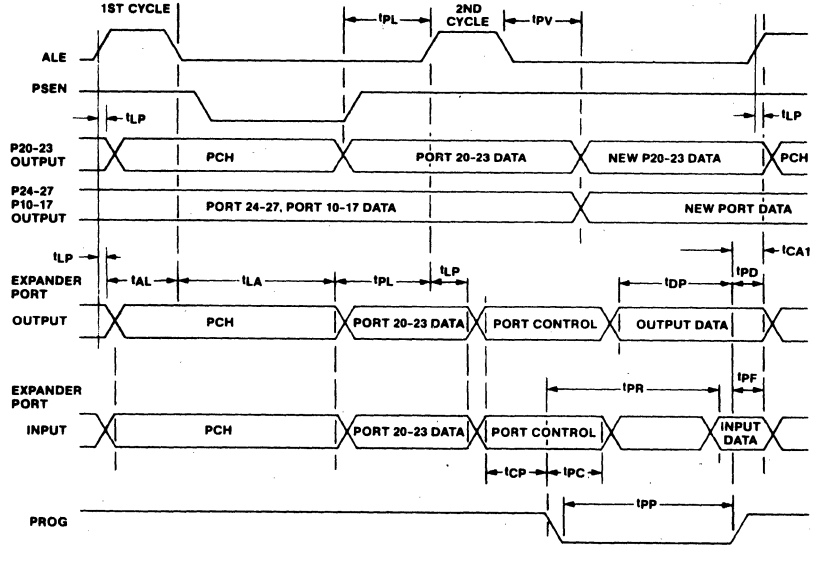
270053-6

INPUT AND OUTPUT FOR A.C. TESTS

270053-7

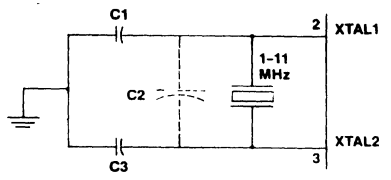
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Output timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PORT 1/PORT 2 TIMING



270053-8

CRYSTAL OSCILLATOR MODE

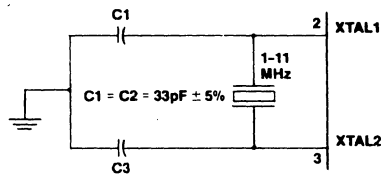


270053-9

C1 = 5 pF ±½ pF + (STRAY < 5 pF)
C2 = (CRYSTAL + STAY) < 8 pF
C3 = 20 pF ±1 pF + (STRAY < 5 pF)

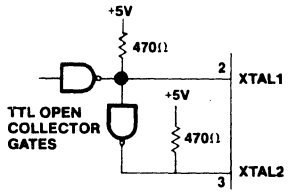
Crystal series resistance should be less than 30Ω at 11 MHz; less than 75Ω at 6 MHz; less than 180Ω at 3.6 MHz.

CERAMIC RESONATOR MODE



270053-10

DRIVING FROM EXTERNAL SOURCE



270053-11

For XTAL1 and XTAL2 define "high" as voltages above 1.6V and "low" as voltages below 1.6V. The duty cycle requirements for externally driving XTAL1 and XTAL2 using the circuits shown above are as follows: XTAL1 must be high 35–65% of the period and XTAL2 must be high 35–65% of the period. Rise and fall times must be faster than 20 ns.

4

PROGRAMMING AND VERIFYING THE P8749H/48H PROGRAMMABLE ROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL1	Clock Input (3 to 4.0 MHz)
XTAL2	
$\overline{\text{RESET}}$	Initialization and Address Latching
T0	Selection of Program or Verifying Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input
	Data Output During Verify
P20–P22	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING:

An attempt to program a missocketed P8749H/48H will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. V_{DD} = 5V, Clock applied or internal oscillator operating, $\overline{\text{RESET}}$ = 0V, T0 = 5V, EA = 5V, BUS and PROG floating. P10 and P11 must be tied to ground.
2. Insert P8749H/48H in programming socket
3. T0 = 0V (select program mode)
4. EA = 18V (activate program mode)
5. Address applied to BUS and P20–22
6. $\overline{\text{RESET}}$ = 5V (latch address)
7. Data applied to BUS
8. V_{DD} = 21V (programming power)
9. PROG = V_{CC} or float followed by one 50 ms pulse to 18V
10. V_{DD} = 5V
11. T0 = 5V (verify mode)
12. Read and verify data on BUS
13. T0 = 0V
14. $\overline{\text{RESET}}$ = 0V and repeat from step 5
15. Programmer should be at conditions of step 1 when P8749H/48H is removed from socket.

NOTE:
Once programmed the P8749H/48H cannot be erased.

A.C. TIMING SPECIFICATION FOR PROGRAMMING P8748H/P8749H ONLY

T_A = 25°C ±5°C; V_{CC} = 5V ±5%; V_{DD} = 21 ±0.5V

Symbol	Parameter	Min	Max	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{RESET}$	$4t_{CY}$			
t_{WA}	Address Hold Time After $\overline{RESET}$	$4t_{CY}$			
t_{DW}	Data in Setup Time to PROG	$4t_{CY}$			
t_{WD}	Data in Hold Time After PROG	$4t_{CY}$			
t_{PH}	$\overline{RESET}$ Hold Time to Verify	$4t_{CY}$			
t_{VDDW}	V_{DD} Hold Time Before PROG	0	1.0	ms	
t_{VDDH}	V_{DD} Hold Time After PROG	0	1.0	ms	
t_{PW}	Program Pulse Width	50	60	ms	
t_{TW}	T0 Setup Time for Program Mode	$4t_{CY}$			
t_{WT}	T0 Hold Time After Program Mode	$4t_{CY}$			
t_{DO}	T0 to Data Out Delay		$4t_{CY}$		
t_{WW}	$\overline{RESET}$ Pulse Width to Latch Address	$4t_{CY}$			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	100	μs	
t_{CY}	CPU Operation Cycle Time	3.75	5	μs	
t_{RE}	$\overline{RESET}$ Setup Time before EA	$4t_{CY}$			

NOTE:
If Test 0 is high, t_{DO} can be triggered by $\overline{RESET}$.

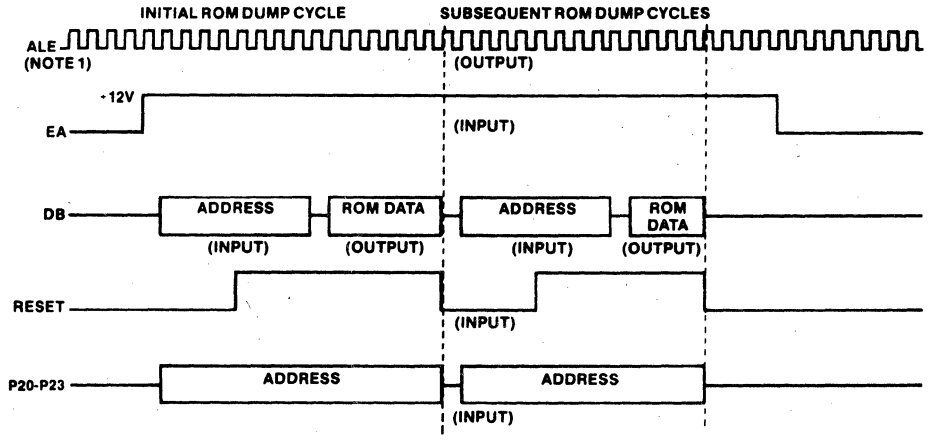
4

D.C. CHARACTERISTICS FOR PROGRAMMING P8748H/P8749H ONLY

T_A = 25°C ±5°C; V_{CC} = 5V ±5%; V_{DD} = 21 ±0.5V

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DDH}	V_{DD} Program Voltage High Level	20.5	21.5	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	17.5	18.5	V	
V_{PL}	PROG Voltage Low Level	4.0	V_{CC}	V	
V_{EAH}	EA Program or Verify Voltage High Level	17.5	18.5	V	
I_{DD}	V_{DD} High Voltage Supply Current		20.0	mA	
I_{PROG}	PROG High Voltage Supply Current		1.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

SUGGESTED ROM VERIFICATION ALGORITHM FOR ROM DEVICE ONLY



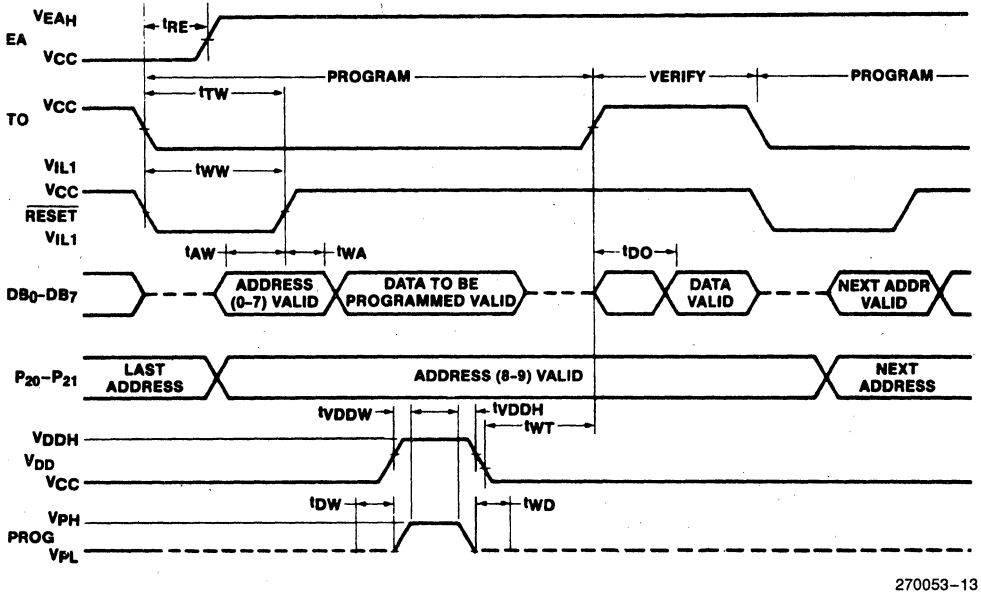
270053-12

	48H	49H	50H
A10	0	ADDR	ADDR
A11	0	0	ADDR

$V_{CC} = V_{DD} = +5V$
$V_{SS} = 0V$

NOTE:
ALE is function of X1, X2 inputs.

COMBINATION PROGRAM/VERIFY MODE (PROGRAMMABLE ROMS ONLY)



270053-13

D8748H/D8749H
HMOS-E SINGLE-COMPONENT 8-BIT MICROCONTROLLER

- **High Performance HMOS-E**
- **Interval Timer/Event Counter**
- **Two Single Level Interrupts**
- **Single 5-Volt Supply**
- **Over 96 Instructions; 90% Single Byte**
- **Compatible with 8080/8085 Peripherals**
- **Easily Expandable Memory and I/O**
- **Up to 1.35 μs Instruction Cycle; All Instructions 1 or 2 Cycles**

The Intel D8749H/D8748H are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS-E process.

The family contains 27 I/O lines, an 8-bit timer/counter, on-chip RAM and on-board oscillator/clock circuits. For systems that require extra capability, the family can be expanded using MCS®-80/MCS®-85 peripherals.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

Device	Internal Memory	
D8749H	2K x 8 EPROM	128 x 8 RAM
D8748H	1K x 8 EPROM	64 x 8 RAM

4

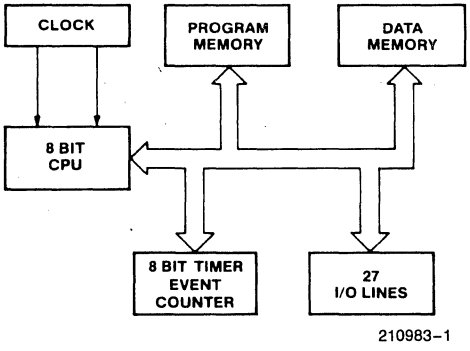


Figure 1. Block Diagram

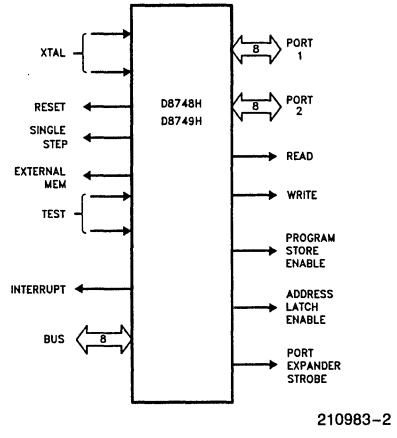
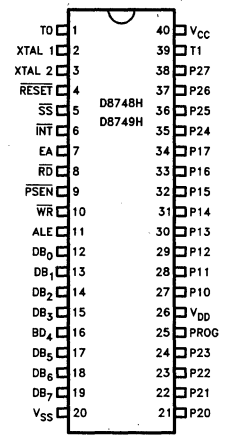


Figure 2. Logic Symbol

September 1992
Order Number: 210983-004



210983-3

Figure 3. Pin Configuration

Table 1. Pin Description (40-Pin DIP)

Symbol	Pin No.	Function
V_{SS}	20	Circuit GND potential.
V_{DD}	26	+5V during normal operation.
		Programming power supply (+21V).
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Output strobe for 8243 I/O expander.
		Program pulse (+18V) input pin during programming.
P10–P17 Port 1	27–34	8-bit quasi-bidirectional port.
P20–P23 P24–P27 Port 2	21–24 35–38	8-bit quasi-bidirectional port. P20–P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0–DB7 BUS	12–19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CKL instruction.
		Used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) interrupt must remain low for at least 3 machine cycles for proper operation.
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)

Table 1. Pin Description (40-Pin DIP) (Continued)

Symbol	Pin No.	Function
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
		Used during programming.
$\overline{WR}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low.)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction.
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug. (Active high.)
		Used during (18V) programming.
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH}.)
XTAL2	3	Other side of crystal input.

Table 2. Instruction Set

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A, R	Add register to A	1	1
ADD A,@R	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, #data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, #data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A, @R	Or data memory to A	1	1
ORL A, #data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL A, #data	Exclusive or immediate to A	2	2

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR (Continued)			
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
INPUT/OUTPUT			
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, #data	And immediate to port	2	2
ORL P, #data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, #data	And immediate to BUS	2	2
ORL BUS, #data	Or immediate to BUS	2	2
MOVD A, P	Input expander port to A	1	2

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Table 2. Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles
INPUT/OUTPUT (Continued)			
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2
REGISTERS			
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1
BRANCH			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JNI addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
FLAGS			
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1
DATA MOVES			
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	2

Mnemonic	Description	Bytes	Cycles
DATA MOVES (Continued)			
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, #data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from page 3	1	2
TIMER/COUNTER			
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/ counter interrupt	1	1
DIS TCNTI	Disable timer/ counter interrupt	1	1
CONTROL			
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1
NOP	No operation	1	1

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1.0 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = V_{DD} = 5V ±10%; V_{SS} = 0V

Symbol	Parameter	Limits			Unit	Test Conditions	Device
		Min	Typ	Max			
V_{IL}	Input Low Voltage (All Except RESET, X1, X2)	−0.5		0.8	V		All
V_{IL1}	Input Low Voltage ($\overline{RESET}$, X1, X2)	−0.5		0.6	V		All
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$	2.0		V_{CC}	V		All
V_{IH1}	Input High Voltage (X1, X2, $\overline{RESET}$)	3.8		V_{CC}	V		All
V_{OL}	Output Low Voltage (BUS)			0.45	V	I_{OL} = 2.0 mA	All
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			0.45	V	I_{OL} = 1.8 mA	All
V_{OL2}	Output Low Voltage (PROG)			0.45	V	I_{OL} = 1.0 mA	All
V_{OL3}	Output Low Voltage (All Other Outputs)			0.45	V	I_{OL} = 1.6 mA	All
V_{OH}	Output High Voltage (BUS)	2.4			V	I_{OH} = −400 μA	All
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH} = −100 μA	All
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = −40 μA	All
I_{L1}	Leakage Current (T1, $\overline{INT}$)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$	All
I_{LI1}	Input Leakage Current (P10–P17, P20–P27, EA, $\overline{SS}$)			−500	μA	V_{SS} + 0.45 ≤ $V_{IN} \le V_{CC}$	All
I_{LI2}	Input Leakage Current $\overline{RESET}$	−10		−300	μA	$V_{SS} \le V_{IN} \le 3.8V$	All
I_{L0}	Leakage Current (BUS, T0) (High Impedance State)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$	All
I_{DD} + I_{CC}	Total Supply Current*		80	100	mA		8748H
			95	110	mA		8749H

NOTE:
*I_{CC} + I_{DD} is measured with all outputs disconnected; $\overline{SS}$, $\overline{RESET}$, and $\overline{INT}$ equal to V_{CC}; EA equal to V_{SS}.

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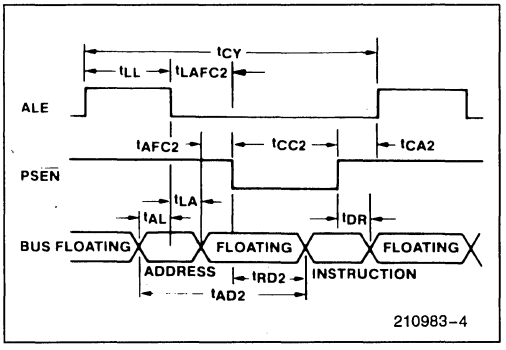
AC CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	f(t) (Note 3)	11 MHz		Unit	Conditions (Note 1)
			Min	Max		
t	Clock Period	1/xtal freq	90.9	1000	ns	(Note 3)
t_{LL}	ALE Pulse Width	3.5t − 170	150		ns	
t_{AL}	Addr Setup to ALE	2t − 110	70		ns	(Note 2)
t_{LA}	Addr Hold from ALE	t − 40	50		ns	
t_{CC1}	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	7.5t − 200	480		ns	
t_{CC2}	Control Pulse Width ($\overline{PSEN}$)	6t − 200	350		ns	
t_{DW}	Data Setup before $\overline{WR}$	6.5t − 200	390		ns	
t_{WD}	Data Hold after $\overline{WR}$	t − 50	40		ns	
t_{DR}	Data Hold ($\overline{RD}$, $\overline{PSEN}$)	1.5t − 30	0	110	ns	
t_{RD1}	$\overline{RD}$ to Data In	6t − 170		375	ns	
t_{RD2}	$\overline{PSEN}$ to Data In	4.5t − 170		240	ns	
t_{AW}	Addr Setup to $\overline{WR}$	5t − 150	300		ns	
t_{AD1}	Addr Setup to Data ($\overline{RD}$)	10.5t − 220		730	ns	
t_{AD2}	Addr Setup to Data ($\overline{PSEN}$)	7.5t − 200		460	ns	
t_{AFC1}	Addr Float to $\overline{RD}$, $\overline{WR}$	2t − 40	140		ns	(Note 2)
t_{AFC2}	Addr Float to $\overline{PSEN}$	0.5t − 40	10		ns	(Note 2)
t_{LAFC1}	ALE to Control ($\overline{RD}$, $\overline{WR}$)	3t − 75	200		ns	
t_{LAFC2}	ALE to Control ($\overline{PSEN}$)	1.5t − 75	60		ns	
t_{CA1}	Control to ALE ($\overline{RD}$, $\overline{WR}$, PROG)	t − 65	25		ns	
t_{CA2}	Control to ALE ($\overline{PSEN}$)	4t − 70	290		ns	
t_{CP}	Port Control Setup to PROG	1.5t − 80	50		ns	
t_{PC}	Port Control Hold to PROG	4t − 260	100		ns	
t_{PR}	PROG to P2 Input Valid	8.5t − 120		650	ns	
t_{PF}	Input Data Hold from PROG	1.5t	0	140	ns	
t_{DP}	Output Data Setup	6t − 290	250		ns	
t_{PD}	Output Data Hold	1.5t − 90	40		ns	
t_{PP}	PROG Pulse Width	10.5t − 250	700		ns	
t_{PL}	Port 2 I/O Setup to ALE	4t − 200	160		ns	
t_{LP}	Port 2 I/O Hold to ALE	0.5t − 30	15		ns	
t_{PV}	Port Output from ALE	4.5t + 100		510	ns	
t_{0PRR}	T0 Rep Rate	3t	270		ns	
t_{CY}	Cycle Time	15t	1.36	15.0	μs	

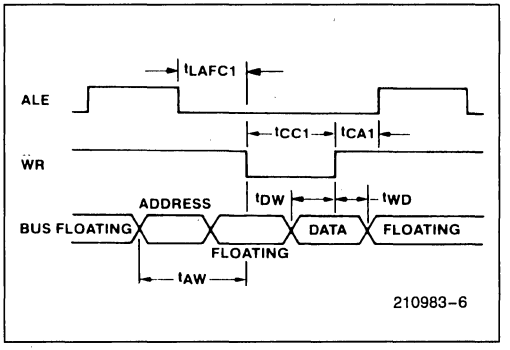
NOTES:
1. Control outputs CL = 80 pF; BUS outputs CL = 150 pF.
2. BUS High Impedance Load 20 pF.
3. f(t) assumes 50% duty cycle on X1, X2. Max clock period is for a 1 MHz crystal input.

WAVEFORMS

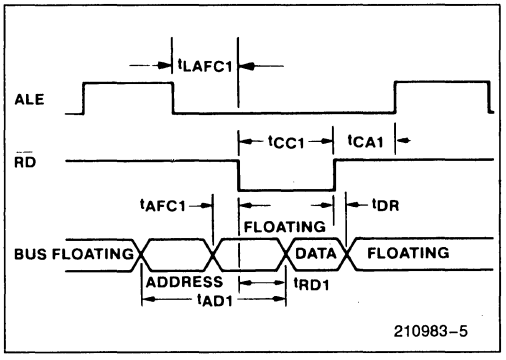
INSTRUCTION FETCH FROM PROGRAM MEMORY



WRITE TO EXTERNAL DATA MEMORY



READ FROM EXTERNAL DATA MEMORY

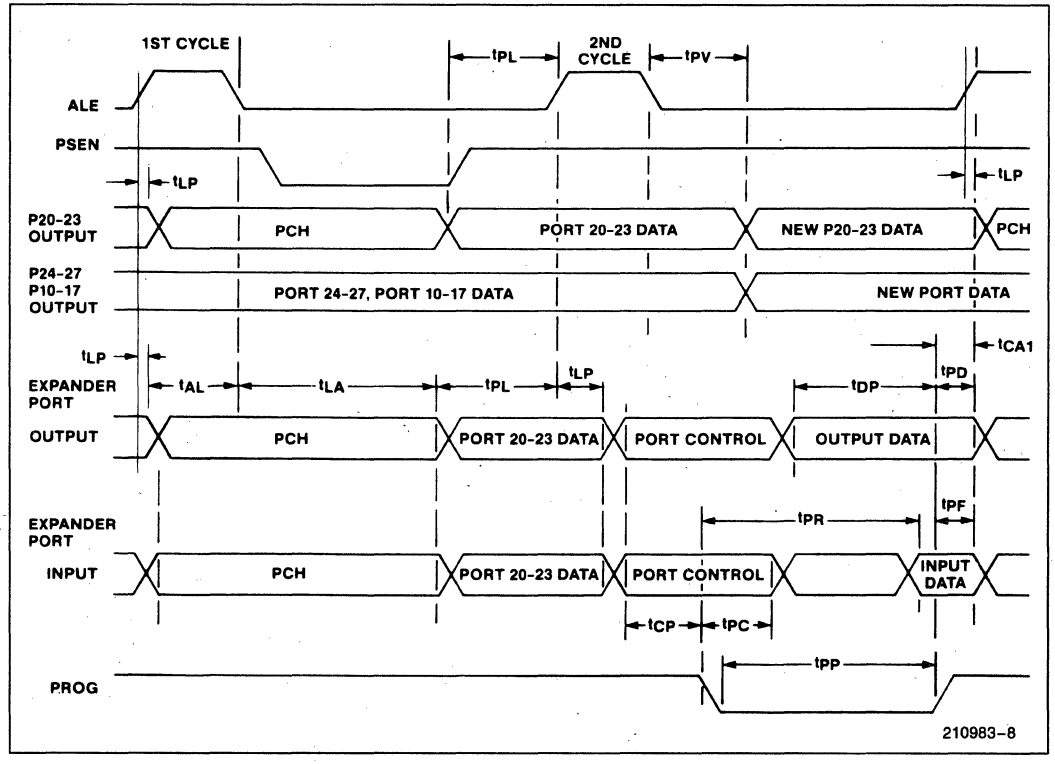


INPUT AND OUTPUT FOR AC TESTS

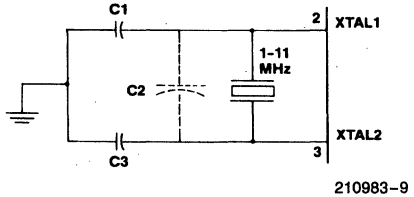
AC testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Output timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

4

PORT 1/PORT 2 TIMING



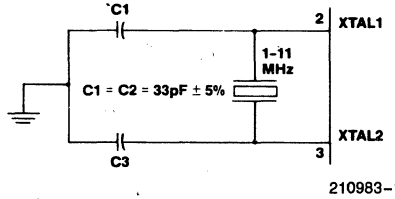
CRYSTAL OSCILLATOR MODE



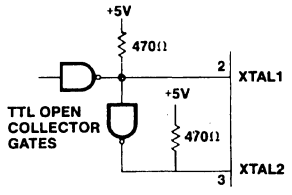
C1 = 5 pF ±½ pF + (STRAY < 5 pF)
C2 = (CRYSTAL + STRAY) < 8 pF
C3 = 20 pF ±1 pF (STRAY < 5 pF)

Crystal series resistance should be less than 30Ω at 11 MHz; less than 75Ω at 6 MHz; less than 180Ω at 3.6 MHz.

CERAMIC RESONATOR MODE



DRIVING FROM EXTERNAL SOURCE



210983-11

For XTAL1 and XTAL2 define "high" as voltages above 1.6V and "low" as voltages below 1.6V. The duty cycle requirements for externally driving XTAL1 and XTAL2 using the circuit shown above are as follows: XTAL1 must be high 35–65% of the period and XTAL2 must be high 36–65% of the period. Rise and fall times must be faster than 20 ns.

PROGRAMMING, VERIFYING AND ERASING THE 8749H (8748H) EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (3 to 4.0 MHz)
XTAL 2	
RESET	Initialization and Address Latching
TEST 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input
	Data Output During Verify
P20–P22	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING

An attempt to program a missocketed 8749H (8748H) will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1) V_{DD} = 5V, Clock applied or internal oscillator operating. RESET = 0V, TEST 0 = 5V, EA = 5V, BUS and PROG floating. P10 and P11 must be tied to ground.
2) Insert 8749H (8748H) in programming socket.
3) TEST 0 = 0V (select program mode)
4) EA = 18V (activate program mode)
5) Address applied to BUS and P20–22
6) RESET = 5V (latch address)
7) Data applied to BUS
8) V_{DD} = 21V (programming power)
9) PROG = V_{CC} or float followed by one 50 ms pulse to 18V
10) V_{DD} = 5V
11) TEST 0 = 5V (verify mode)
12) Read and verify data on BUS
13) TEST 0 = 0V
14) RESET = 0V and repeat from step 5
15) Programmer should be at conditions of step 1 when 8749H (8748H) is removed from socket.

4

AC TIMING SPECIFICATION FOR PROGRAMMING 8748H/8749H

T_A = 25°C ±5°C; V_{CC} = 5V ±5%; V_{DD} = 21V ±0.5V

Symbol	Parameter	Min	Max	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{RESET}$ ↑	$4t_{CY}$			
t_{WA}	Address Hold Time after $\overline{RESET}$ ↑	$4t_{CY}$			
t_{DW}	Data in Setup Time to PROG ↑	$4t_{CY}$			
t_{WD}	Data in Hold Time after PROG ↓	$4t_{CY}$			
t_{PH}	$\overline{RESET}$ Hold Time to Verify	$4t_{CY}$			
t_{VDDW}	V_{DD} Hold Time before PROG ↑	0	1.0	ms	
t_{VDDH}	V_{DD} Hold Time after PROG ↓	0	1.0	ms	
t_{PW}	Program Pulse Width	50	60	ms	
t_{TW}	TEST 0 Setup Time for Program Mode	$4t_{CY}$			
t_{WT}	TEST 0 Hold Time after Program Mode	$4t_{CY}$			
t_{DO}	TEST 0 to Data Out Delay		$4t_{CY}$		
t_{WW}	$\overline{RESET}$ Pulse Width to Latch Address	$4t_{CY}$			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	100	μs	
t_{CY}	CPU Operation Cycle Time	3.75	5	μs	
t_{RE}	$\overline{RESET}$ Setup Time before EA ↑	$4t_{CY}$			

NOTE:
If TEST 0 is high, t_{DO} can be triggered by $\overline{RESET}$ ↑.

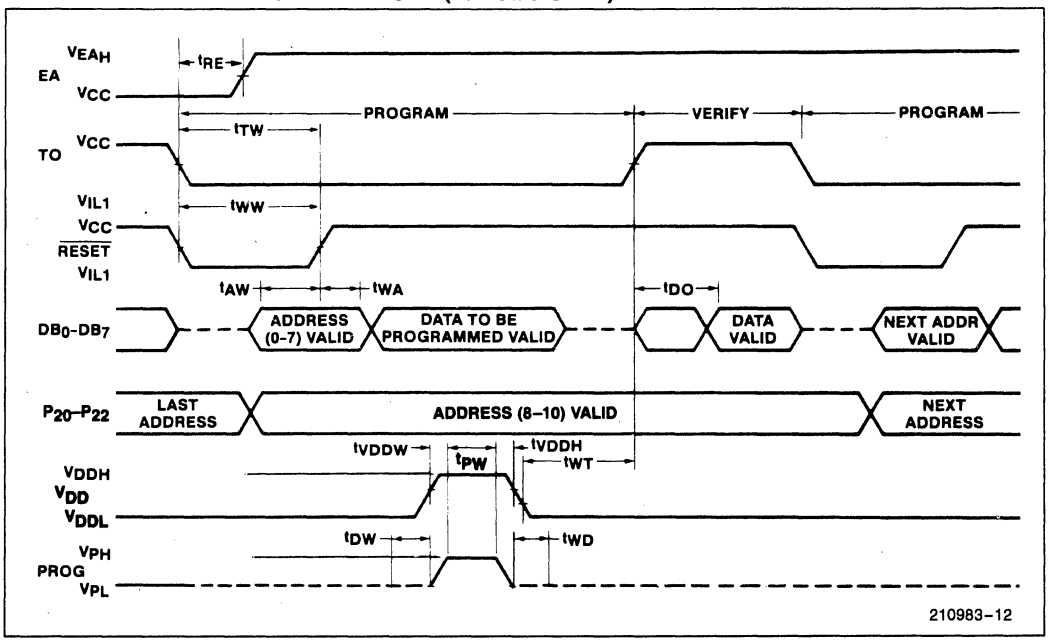
DC SPECIFICATION FOR PROGRAMMING 8748H/8749H

T_A = 25°C ±5°C; V_{CC} = 5V ±5%; V_{DD} = 21V ±0.5V

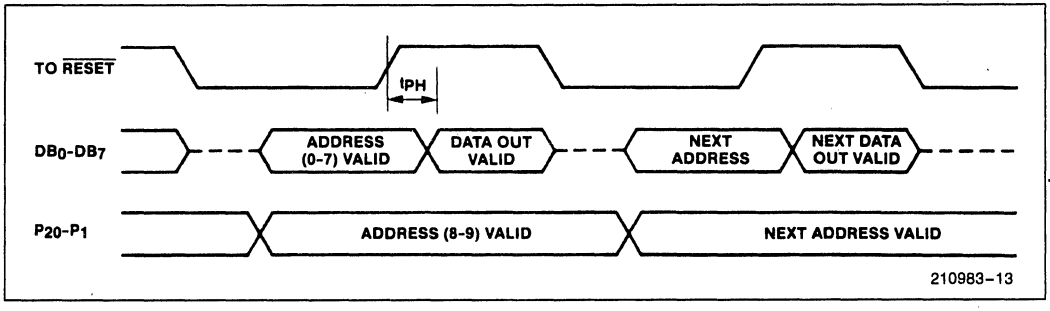
Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DDH}	V_{DD} Program Voltage High Level	20.5	21.5	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	17.5	18.5	V	
V_{PL}	PROG Voltage Low Level	4.0	V_{CC}	V	
V_{EAH}	EA Program or Verify Voltage High Level	17.5	18.5	V	
I_{DD}	V_{DD} High Voltage Supply Current		20.0	mA	
I_{PROG}	PROG High Voltage Supply Current		1.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

WAVEFORMS

COMBINATION PROGRAM/VERIFY MODE (EPROMs ONLY)



VERIFY MODE



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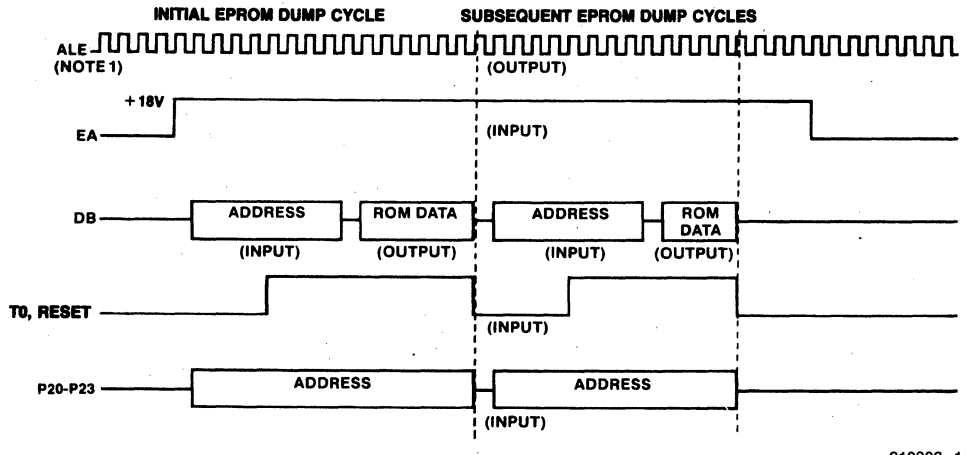
SUGGESTED EPROM VERIFICATION ALGORITHM FOR HMOS-E DEVICE ONLY



210983-14

	48H	49H
A10	0	ADDR
A11	0	0

$V_{CC} = V_{DD} = +5V$
$V_{SS} = 0V$

NOTE:
ALE is function of X1, X2 inputs.

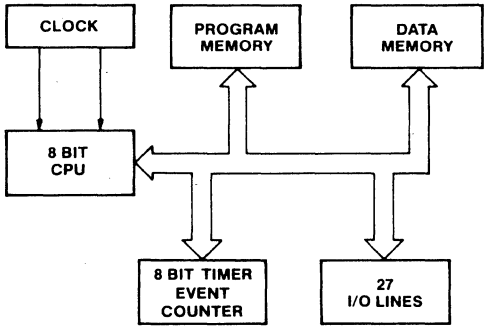
P8049KB
HMOS SINGLE-COMPONENT 8-BIT MICROCONTROLLER

- **Four 10 mA LED Drivers**
- **Interval Time/Event Counter**
- **Two Single Level Interrupts**
- **Single 5V Supply**
- **Over 96 Instructions**
- **Easily Expandable Memory and I/O**
- **1 to 8 MHz Operation**
- **1.87 μs Instruction Cycle**
- **1 or 2 Cycle Instructions**
- **2K x 8 ROM**
- **128 x 8 RAM**

The Intel 8049KB is a totally self-sufficient, 8-bit parallel computer fabricated on a single silicon chip using Intel's advanced N-channel silicon gate HMOS process. This microcontroller is available in the masked ROM version and runs at a maximum XTAL frequency of 8 MHz.

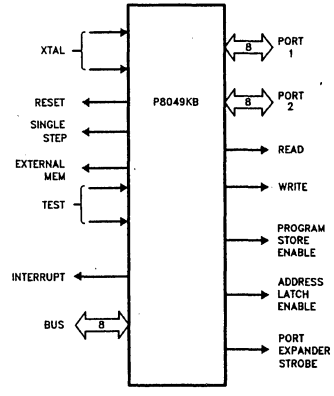
This microcomputer is designed to be an efficient controller as well as arithmetic processor. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting of mostly single byte instructions and no instruction over 2 bytes in length.

4



270790-1

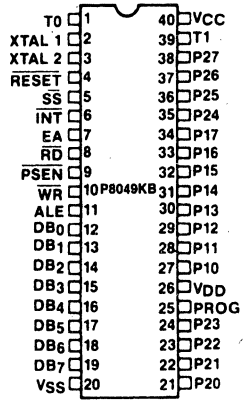
Figure 1. Block Diagram



270790-2

Figure 2. Logic Symbol

February 1990
Order Number: 270790-002



270790-12

Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Function
V_{SS}	20	Circuit GND potential.
V_{DD}	26	+5V during normal operation.
		Low power standby pin.
		Programming power supply (+21V).
V_{CC}	40	Main power supply; +5V during operation and programming.
P10–P17 Port 1	27–34	8-bit quasi-bidirectional port.
P20–P23 P24–P27 Port 2	21–24 35–38	8-bit quasi-bidirectional port. P20–P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0–DB7 BUS	12–19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instruction JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
		Used during programming.

Table 1. Pin Description (Continued)

Symbol	Pin No.	Function
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) interrupt must remain low for at least 3 machine cycles for proper operation.
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
		Used during power down.
		Used during programming.
		Used during ROM verification.
$\overline{WR}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction.
		(Active low) Used in sync mode.
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug. (Active high)
		Used during (18V) programming.
		Used during ROM verification (12V).
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

Table 2. Instruction Set

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, #data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, #data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A, @R	Or data memory to A	1	1
ORL A, #data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL A, #data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, #data	And immediate to port	2	2
ORL P, #data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, #data	And immediate to BUS	2	2
ORL BUS, #data	Or immediate to BUS	2	2
MOVD A, P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JNI addr	Jump on $\overline{INT}$ = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Table 2. Instruction Set (Continued)

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	Clear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, #data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and data memory	1	1
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNTI	Enable timer/counter interrupt	1	1
DIS TCNTI	Disable timer/counter interrupt	1	1

Control

Mnemonic	Description	Bytes	Cycles
EN I	Enable external interrupt	1	1
DIS I	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

4

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on any Pin with Respect to Ground.....−0.5V to +7V
Power Dissipation.....1.5W

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = V_{DD} = 5V ±10%; V_{SS} = 0V

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, X1, X2)	−0.5		0.8	V	
V_{IL1}	Input Low Voltage ($\overline{RESET}$, X1, X2)	−0.5		0.6	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage (X1, X2, $\overline{RESET}$)	3.8		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS)			0.45	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			0.45	V	I_{OL} = 1.8 mA
V_{OL2}	Output Low Voltage (PROG)			0.45	V	I_{OL} = 1.0 mA
V_{OL3}	Output Low Voltage (All Other Outputs)			0.45	V	I_{OL} = 1.6 mA
V_{OL4}	Output Low Voltage (Any Four Port Outputs)			0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (BUS)	2.4			V	I_{OH} = −400 μA
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH} = −100 μA
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = −40 μA

D.C. CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = V_{DD} = 5V ±10%; V_{SS} = 0V (Continued)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
I_{L1}	Leakage Current (T1, $\overline{INT}$)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{LI1}	Input Leakage Current (P10–P17, P20–P27, EA, $\overline{SS}$)			−500	μA	$V_{SS} + 0.45 \le V_{IN} \le V_{CC}$
I_{LI2}	Input Leakage Current $\overline{RESET}$	−10		−300	μA	$V_{SS} \le V_{IN} \le 3.8$
I_{LO}	Leakage Current (BUS, T0) (High Impedance State)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{DD}	V_{DD} Supply Current (RAM Standby)		3	5	mA	
			4	7	mA	
			5	10	mA	
$I_{DD} + I_{CC}$	Total Supply Current*		30	65	mA	
			35	70	mA	
			40	80	mA	
			30	100	mA	
			50	110	mA	
V_{DD}	RAM Standby Voltage	2.2		5.5	V	Standby Mode Reset ≤ V_{IL1}
		2.2		5.5	V	
		2.2		5.5	V	

*$I_{CC} + I_{DD}$ are measured with all outputs in their high impedance state; $\overline{RESET}$ low; 8 MHz crystal applied; $\overline{INT}$, $\overline{SS}$, and EA floating.

†Any four Port Outputs can be loaded to a 10 mA maximum. Excessive heating and dissipation will result if more than four outputs are loaded to 10 mA.

4

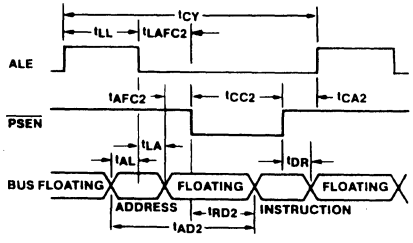
A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	f (t) (Note 3)	8 MHz		Unit	Conditions (Note 1)
			Min	Max		
t	Clock Period	1/xtal freq	125	1000	ns	(Note 3)
t_{LL}	ALE Pulse Width	3.5t−170	268		ns	
t_{AL}	Addr Setup to ALE	2t−110	140		ns	(Note 2)
t_{LA}	Addr Hold from ALE	t−40	85		ns	
t_{CC1}	Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	7.5t−200	675		ns	
t_{CC2}	Control Pulse Width ($\overline{PSEN}$)	6t−200	550		ns	
t_{DW}	Data Setup before $\overline{WR}$	6.5t−200	613		ns	
t_{WD}	Data Hold after $\overline{WR}$	t−50	75		ns	
t_{DR}	Data Hold ($\overline{RD}$, $\overline{PSEN}$)	1.5t−30	0	158	ns	
t_{RD1}	$\overline{RD}$ to Data in	6t−170		580	ns	
t_{RD2}	$\overline{PSEN}$ to Data in	4.5t−170		393	ns	
t_{AW}	Addr Setup to $\overline{WR}$	5t−150	475		ns	
t_{AD1}	Addr Setup to Data ($\overline{RD}$)	10.5t−220		1093	ns	
t_{AD2}	Addr Setup to Data ($\overline{PSEN}$)	7.5t−200		738	ns	
t_{AFC1}	Addr Float to $\overline{RD}$, $\overline{WR}$	2t−40	210		ns	(Note 2)
t_{AFC2}	Addr Float to $\overline{PSEN}$	0.5t−40	23		ns	(Note 2)
t_{LAFC1}	ALE to Control ($\overline{RD}$, $\overline{WR}$)	3t−75	300		ns	
t_{LAFC2}	ALE to Control ($\overline{PSEN}$)	1.5t−75	113		ns	
t_{CA1}	Control to ALE ($\overline{RD}$, $\overline{WR}$, PROG)	t−65	60		ns	
t_{CA2}	Control to ALE ($\overline{PSEN}$)	4t−70	430		ns	
t_{CP}	Port Control Setup to PROG	1.5t−80	108		ns	
t_{PC}	Port Control Hold to PROG	4t−260	240		ns	
t_{PR}	PROG to P2 Input Valid	8.5t−120		943	ns	
t_{PF}	Input Data Hold from PROG	1.5t	0	188	ns	
t_{DP}	Output Data Setup	6t−290	460		ns	
t_{PD}	Output Data Hold	1.5t−90	98		ns	
t_{PP}	PROG Pulse Width	10.5t−250	1063		ns	
t_{PL}	Port 2 I/O Setup to ALE	4t−200	300		ns	
t_{LP}	Port 2 I/O Hold to ALE	0.5t−30	33		ns	
t_{PV}	Port Output from ALE	4.5t+100		663	ns	
t_{0PRR}	T0 Rep Rate	3t	375		ns	
t_{CY}	Cycle Time	15t	1.87	28	μs	

NOTES:
1. Control outputs: $C_L = 80$ pF. BUS Outputs: $C_L = 150$ pF.
2. BUS High Impedance Load 20 pF
3. f(t) assumes 50% duty cycle on X1, X2. Max clock period is for a 1 MHz crystal input.

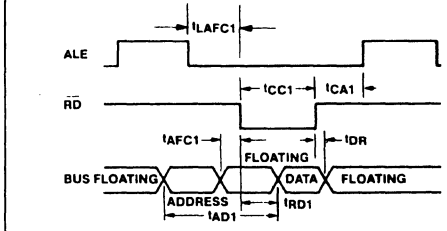
WAVEFORMS

INSTRUCTION FETCH FROM PROGRAM MEMORY



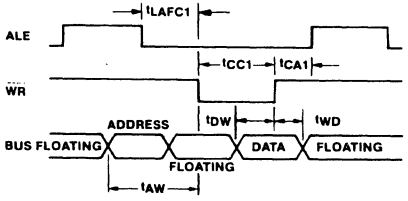
270790-3

READ FROM EXTERNAL DATA MEMORY



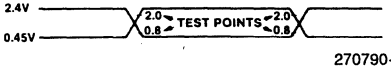
270790-4

WRITE TO EXTERNAL DATA MEMORY



270790-5

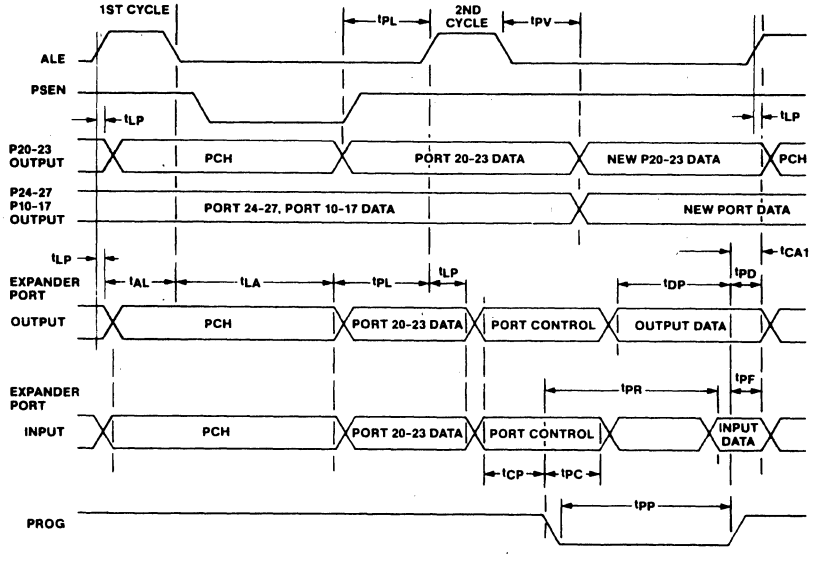
INPUT AND OUTPUT FOR A.C. TESTS



270790-6

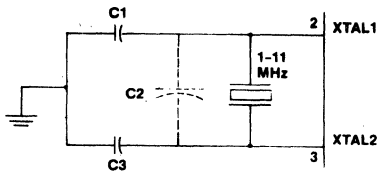
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Output timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

PORT 1/PORT 2 TIMING



270790-7

CRYSTAL OSCILLATOR MODE

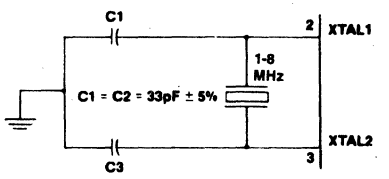


270790-8

C1 = 5 pF ±½ pF + (STRAY < 5 pF)
C2 = (CRYSTAL + STAY) < 8 pF
C3 = 20 pF ±1 pF + (STRAY < 5 pF)

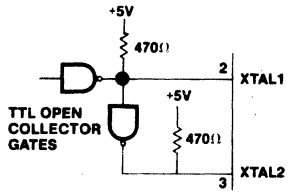
Crystal series resistance should be less than 50Ω at 8 MHz; less than 75Ω at 6 MHz; less than 180Ω at 3.6 MHz.

CERAMIC RESONATOR MODE



270790-9

DRIVING FROM EXTERNAL SOURCE



270790-10

For XTAL1 and XTAL2 define "high" as voltages above 1.6V and "low" as voltages below 1.6V. The duty cycle requirements for externally driving XTAL1 and XTAL2 using the circuits shown above are as follows: XTAL1 must be high 35-65% of the period and XTAL2 must be high 35-65% of the period. Rise and fall times must be faster than 20 ns.

VERIFYING THE 8049KB ROM

Programming Verification

The following is a list of the pins used for verification and a description of their functions:

Pin	Function
XTAL1	Clock Input (3 to 4.0 MHz)
XTAL2	
$\overline{\text{RESET}}$	Initialization and Address Latching
T0	Selection of Program or Verifying Mode
EA	Activation Verify Modes
BUS	Address and Data Output During Verify
P20–P22	Address Input

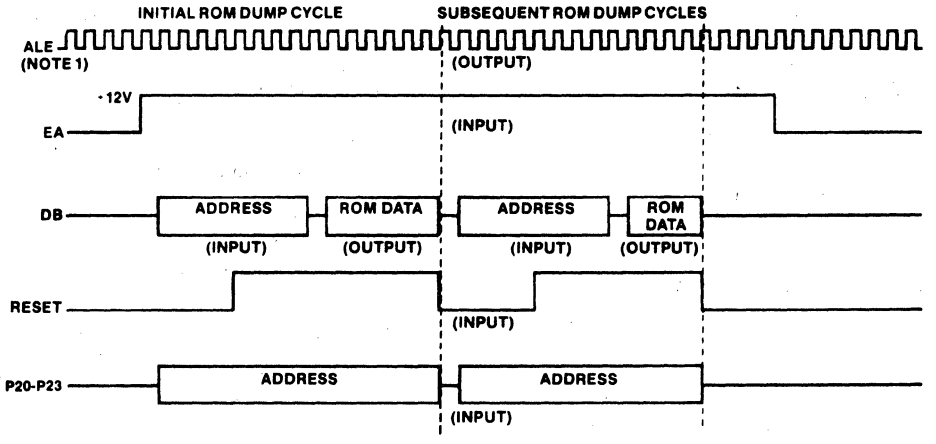
WARNING:

An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Verify sequence is:

1. V_{DD} = 5V, Clock applied or internal oscillator operating, $\overline{\text{RESET}}$ = 0V, EA = 5V, BUS floating.
2. Insert 8049KB in verify socket
3. EA = 12V (activate verify mode)
4. Address applied to BUS and P20–23
5. $\overline{\text{RESET}}$ = 5V (latch address)
6. Read and verify Data on BUS
7. $\overline{\text{RESET}}$ = 0V and repeat from step 4
8. Verify socket should be at conditions of step 1 for removal from socket.

SUGGESTED ROM VERIFICATION ALGORITHM FOR ROM DEVICE ONLY



270790-11

	48H	49H	50H
A10	0	ADDR	ADDR
A11	0	0	ADDR

$V_{CC} = V_{DD} = +5V$
$V_{SS} = 0V$

NOTE:
ALE is function of X1, X2 inputs.

MCS®-48
EXPRESS

- **0°C to 70°C Operation**
- **−40°C to +85°C Operation**
- **168 Hr. Burn-In**
- **8048AH/8035AHL**
- **8049AH/8039AHL**
- **8050AH/8040AHL**
- **8748H**
- **8243**
- **8749H**

The new Intel EXPRESS family of single-component 8-bit microcomputers offers enhanced processing options to the familiar 8048AH/8035AHL, 8748H, 8049AH/8039AHL, 8749H, 8050AH/8040AHL Intel components. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards, but fall short of military conditions.

The EXPRESS options include the commercial standard and −40°C to +85°C operation with or without 168 ±8 hours of dynamic burn-in at 125°C per MIL-STD-883, method 1015. Figure 1 summarizes the option marking designators and package selections.

For a complete description of 8048AH/8035AHL, 8748H, 8049AH/8309AHL, 8749H, 8040AHL and 8050AH features and operating characteristics, refer to the respective standard commercial grade data sheet. This document highlights only the electrical specifications which differ from the respective commercial part.

Temp Range °C	0–70	−40–+85	0–70	−40–+85
Burn In	0 Hrs	0 Hrs	168 Hrs	168 Hrs
	P8048AH	TP8048AH	QP8048AH	LP8048AH
	D8048AH	TD8048AH	QD8048AH	LD8048AH
	D8748H	TD8748H	QD8748H	LD8748H
	P8035AHL	TP8035AHL	QP8035AHL	LP8035AHL
	D8035AHL	TD8035AHL	QD8035AHL	LD8035AHL
	P8049AH	TP8049AH	QP8049AH	LP8049AH
	D8049AH	TD8049AH	QD8049AH	LD8049AH
	D8749H	TD8749AH	QD8749H	LD8749AH
	P8039AHL	TP8039AHL	QP8039AHL	LP8039AHL
	D8039AHL	TD8039AHL	QD8039AHL	LD8039AHL
	P8050AH	TP8050AH	QP8050AH	LP8050AH
	D8050AH	TD8050AH	QD8050AH	LD8050AH
	P8040AHL	TP8040AHL	QP8040AHL	LP8040AHL
	D8040AHL	TD8040AHL	QD8040AHL	LD8040AHL
	P8243	TP8243	QP8243	—
	D8243	TD8243	QD8243	LD8243

* Commercial Grade
P Plastic Package
D Cerdip Package

September 1987
Order Number: 270225-002

*Extended Temperature Electrical Specification Deviations**

TP8048AH/TP8035AHL/LP8048AH/LP8035AHL
TD8048AH/TD8035AHL/LD8048AH/LD8035AHL

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.2		V_{CC}	V	
I_{DD}	V_{DD} Supply Current		4	8	mA	
$I_{DD} + I_{CC}$	Total Supply Current		40	80	mA	

TP8049AH/TP8039AHL/LP8049AH/LP8039AHL
TD8049AH/TD8039AHL/LD8049AH/LD8039AHL

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.2		V_{CC}	V	
I_{DD}	V_{DD} Supply Current		5	10	mA	
$I_{DD} + I_{CC}$	Total Supply Current		50	100	mA	

TP8050AH/TP8040AHL/LP8050AHL/LP8040AHL
TD8050AH/TD8040AHL/LD8050AH/LD8040AHL

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.2		V_{CC}	V	
I_{DD}	V_{DD} Supply Current		10	20	mA	
$I_{DD} + I_{CC}$	Total Supply Current		75	120	mA	

*Extended Temperature Electrical Specification Deviations**

TD8748H/LD8748H

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.2		V_{CC}	V	
$I_{DD} + I_{CC}$	Total Supply Current		50	130	mA	

TD8749H/LD8749H

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.2		V_{CC}	V	
$I_{DD} + I_{CC}$	Total Supply Current		75	150	mA	

TP8743/TD8243/LD8243

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
I_{CC}	V_{CC} Supply Current		15	25	mA	

*Refer to individual commercial grade data sheet for complete operating characteristics.

MCS®-51 Architectural Overview

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intel®

September 1989

MCS®-51 Family of Microcontrollers Architectural Overview

5

Order Number: 270251-004

MCS®-51 FAMILY OF MICROCONTROLLERS ARCHITECTURAL OVERVIEW

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INTRODUCTION

The 8051 is the original member of the MCS®-51 family, and is the core for all MCS-51 devices. The features of the 8051 core are:

- 8-bit CPU optimized for control applications
- Extensive Boolean processing (single-bit logic) capabilities
- 64K Program Memory address space
- 64K Data Memory address space
- 4K bytes of on-chip Program Memory
- 128 bytes of on-chip Data RAM
- 32 bidirectional and individually addressable I/O lines
- Two 16-bit timer/counters
- Full duplex UART
- 6-source/5-vector interrupt structure with two priority levels
- On-chip clock oscillator

The basic architectural structure of this 8051 core is shown in Figure 1.

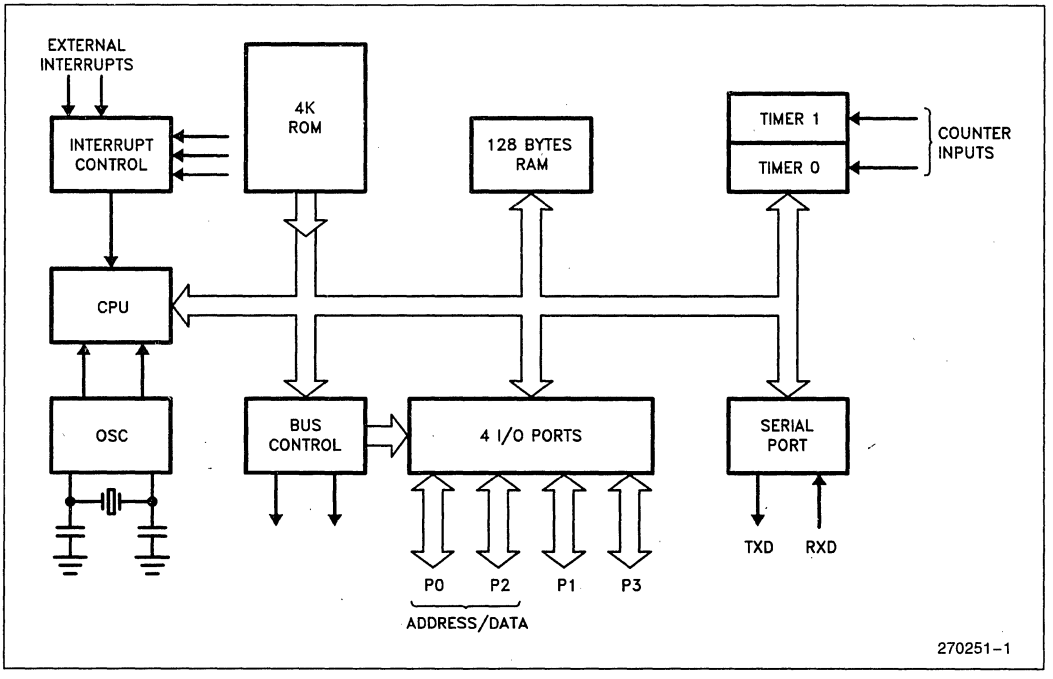

Figure 1. Block Diagram of the 8051 Core

Each device on the MCS-51 family consists of all the core features plus some additional features. A feature comparison of all the MCS-51 devices is shown in Table 1.

Table 1. The MCS®-51 Family of Microcontrollers

Device	ROMless Version	EPROM Version	ROM Bytes	RAM Bytes	8-Bit I/O Ports	16-Bit Timer/ Counters	Programmable Counter Array (PCA)	UART	Serial Expansion Port (SEP)	Global Serial Channel (GSC)	DMA Channels	A/D Channels	Interrupt Sources/ Vectors	Power Down and Idle Modes
8051	8031	—	4K	128	4	2		✓					6/5	
8051AH	8031AH	8751H 8751BH	4K	128	4	2		✓					6/5	
8052AH	8032AH	8752BH	8K	256	4	3		✓					8/6	
80C51BH	80C31BH	87C51	4K	128	4	2		✓					6/5	✓
80C52	80C32	—	8K	256	4	3		✓					8/6	✓
83C51FA	80C51FA	87C51FA	8K	256	4	3	✓	✓					14/7	✓
83C51FB	80C51FA	87C51FB	16K	256	4	3	✓	✓					14/7	✓
83C152JA	80C152JA	—	8K	256	5	2		✓		✓	2		19/11	✓
—	80C152JB	—	—	256	7	2		✓		✓	2		19/11	✓
83C152JC	80C152JC	—	8K	256	5	2		✓		✓	2		19/11	✓
—	80C152JD	—	—	256	7	2		✓		✓	2		19/11	✓
83C452	80C452	87C452P	8K	256	5	2		✓					9/8	✓

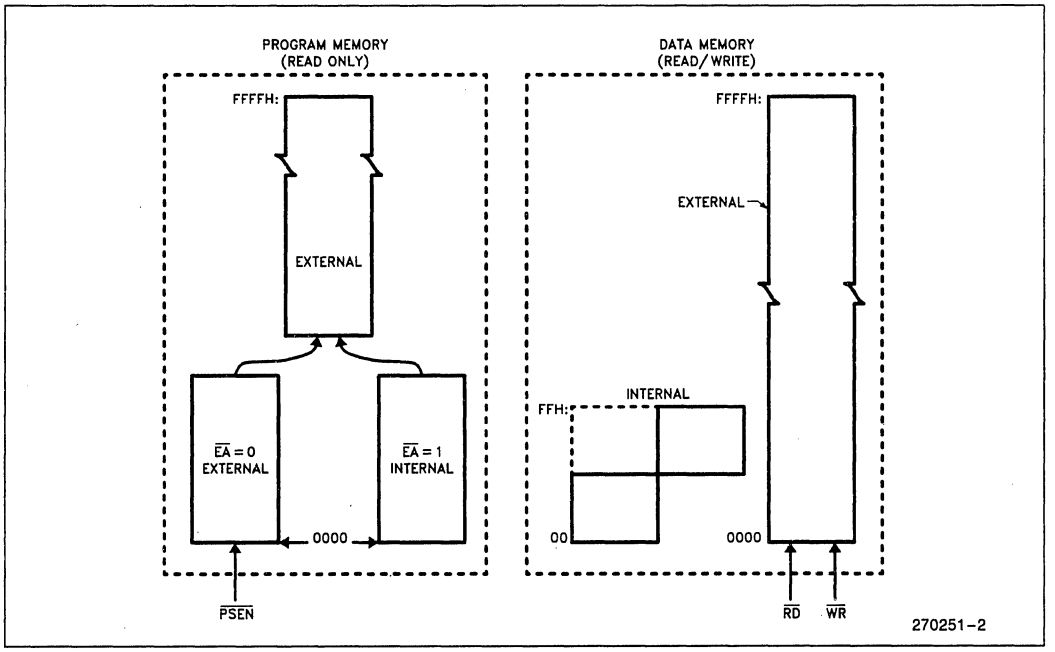

Figure 2. MCS®-51 Memory Structure

CHMOS Devices

Functionally, the CHMOS devices (designated with "C" in the middle of the device name) are all fully compatible with the 8051, but being CMOS, draw less current than an HMOS counterpart. To further exploit the power savings available in CMOS circuitry, two reduced power modes are added:

- Software-invoked Idle Mode, during which the CPU is turned off while the RAM and other on-chip peripherals continue operating. In this mode, current draw is reduced to about 15% of the current drawn when the device is fully active.
- Software-invoked Power Down Mode, during which all on-chip activities are suspended. The on-chip RAM continues to hold its data. In this mode the device typically draws less than 10 μA.

Although the 80C51BH is functionally compatible with its HMOS counterpart, specific differences between the two types of devices must be considered in the design of an application circuit if one wishes to ensure complete interchangeability between the HMOS and CHMOS devices. These considerations are discussed in the Application Note AP-252, "Designing with the 80C51BH".

For more information on the individual devices and features listed in Table 1, refer to the Hardware Descriptions and Data Sheets of the specific device.

MEMORY ORGANIZATION IN MCS®-51 DEVICES

5

Logical Separation of Program and Data Memory

All MCS-51 devices have separate address spaces for Program and Data Memory, as shown in Figure 2. The logical separation of Program and Data Memory allows the Data Memory to be accessed by 8-bit addresses, which can be more quickly stored and manipulated by an 8-bit CPU. Nevertheless, 16-bit Data Memory addresses can also be generated through the DPTR register.

Program Memory can only be read, not written to. There can be up to 64K bytes of Program Memory. In the ROM and EPROM versions of these devices the lowest 4K, 8K or 16K bytes of Program Memory are provided on-chip. Refer to Table 1 for the amount of on-chip ROM (or EPROM) on each device. In the ROMless versions all Program Memory is external. The read strobe for external Program Memory is the signal $\overline{\text{PSEN}}$ (Program Store Enable).

Data Memory occupies a separate address space from Program Memory. Up to 64K bytes of external RAM can be addressed in the external Data Memory space. The CPU generates read and write signals, $\overline{RD}$ and $\overline{WR}$, as needed during external Data Memory accesses.

External Program Memory and external Data Memory may be combined if desired by applying the $\overline{RD}$ and $\overline{PSEN}$ signals to the inputs of an AND gate and using the output of the gate as the read strobe to the external Program/Data memory.

Program Memory

Figure 3 shows a map of the lower part of the Program Memory. After reset, the CPU begins execution from location 0000H.

As shown in Figure 3, each interrupt is assigned a fixed location in Program Memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine must begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

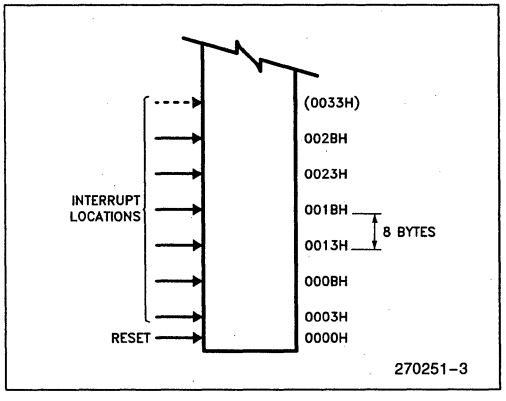

Figure 3. MCS®-51 Program Memory

The interrupt service locations are spaced at 8-byte intervals: 0003H for External Interrupt 0, 000BH for Timer 0, 0013H for External Interrupt 1, 001BH for Timer 1, etc. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

The lowest 4K (or 8K or 16K) bytes of Program Memory can be either in the on-chip ROM or in an external ROM. This selection is made by strapping the $\overline{EA}$ (External Access) pin to either V_{CC} or V_{SS}.

In the 4K byte ROM devices, if the $\overline{EA}$ pin is strapped to V_{CC}, then program fetches to addresses 0000H through 0FFFH are directed to the internal ROM. Program fetches to addresses 1000H through FFFFH are directed to external ROM.

In the 8K byte ROM devices, $\overline{EA} = V_{CC}$ selects addresses 0000H through 1FFFH to be internal, and addresses 2000H through FFFFH to be external.

In the 16K byte ROM devices, $\overline{EA} = V_{CC}$ selects addresses 0000H through 3FFFH to be internal, and addresses 4000H through FFFFH to be external.

If the $\overline{EA}$ pin is strapped to V_{SS}, then all program fetches are directed to external ROM. The ROMless parts must have this pin externally strapped to V_{SS} to enable them to execute properly.

The read strobe to external ROM, $\overline{PSEN}$, is used for all external program fetches. $\overline{PSEN}$ is not activated for internal program fetches.

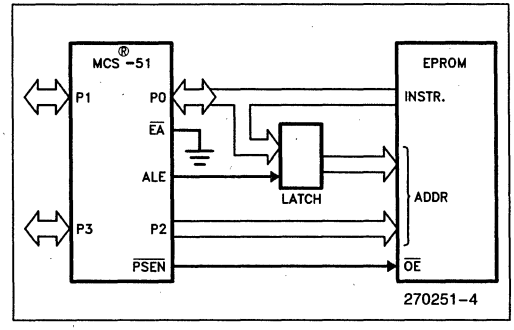

Figure 4. Executing from External Program Memory

The hardware configuration for external program execution is shown in Figure 4. Note that 16 I/O lines (Ports 0 and 2) are dedicated to bus functions during external Program Memory fetches. Port 0 (P0 in Figure 4) serves as a multiplexed address/data bus. It emits the low byte of the Program Counter (PCL) as an address, and then goes into a float state awaiting the arrival of the code byte from the Program Memory. During the time that the low byte of the Program Counter is valid on P0, the signal ALE (Address Latch Enable) clocks this byte into an address latch. Meanwhile, Port 2 (P2 in Figure 4) emits the high byte of the Program Counter (PCH). Then $\overline{PSEN}$ strobes the EPROM and the code byte is read into the microcontroller.

Program Memory addresses are always 16 bits wide, even though the actual amount of Program Memory used may be less than 64K bytes. External program execution sacrifices two of the 8-bit ports, P0 and P2, to the function of addressing the Program Memory.

Data Memory

The right half of Figure 2 shows the internal and external Data Memory spaces available to the MCS-51 user.

Figure 5 shows a hardware configuration for accessing up to 2K bytes of external RAM. The CPU in this case is executing from internal ROM. Port 0 serves as a multiplexed address/data bus to the RAM, and 3 lines of Port 2 are being used to page the RAM. The CPU generates $\overline{RD}$ and $\overline{WR}$ signals as needed during external RAM accesses.

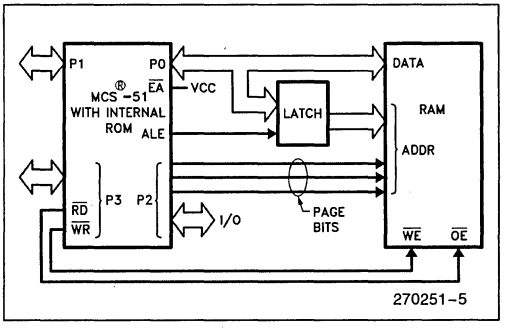

Figure 5. Accessing External Data Memory. If the Program Memory is Internal, the Other Bits of P2 are Available as I/O.

There can be up to 64K bytes of external Data Memory. External Data Memory addresses can be either 1 or 2 bytes wide. One-byte addresses are often used in conjunction with one or more other I/O lines to page the RAM, as shown in Figure 5. Two-byte addresses can also be used, in which case the high address byte is emitted at Port 2.

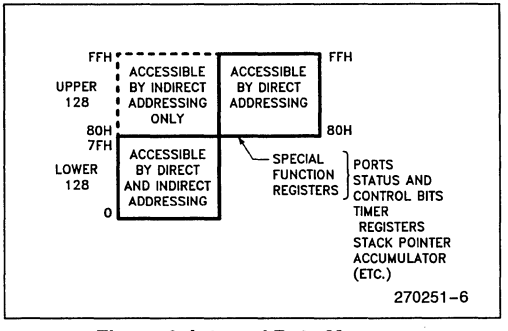

Figure 6. Internal Data Memory

Internal Data Memory is mapped in Figure 6. The memory space is shown divided into three blocks, which are generally referred to as the Lower 128, the Upper 128, and SFR space.

Internal Data Memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes, using a simple trick. Direct addresses higher than 7FH access one memory space, and indirect addresses higher than 7FH access a different memory space. Thus Figure 6 shows the Upper 128 and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

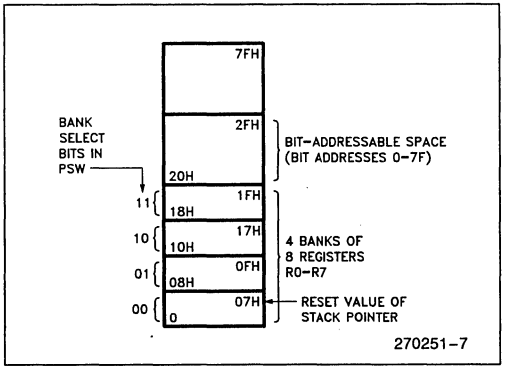

Figure 7. The Lower 128 Bytes of Internal RAM

The Lower 128 bytes of RAM are present in all MCS-51 devices as mapped in Figure 7. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

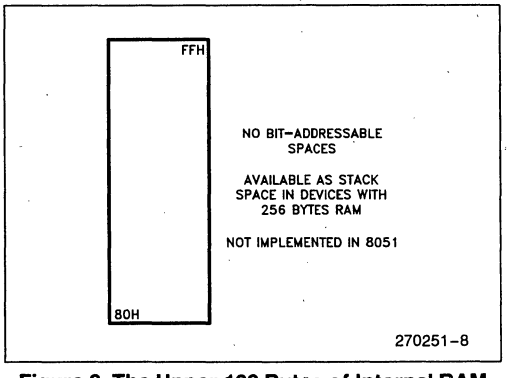

Figure 8. The Upper 128 Bytes of Internal RAM

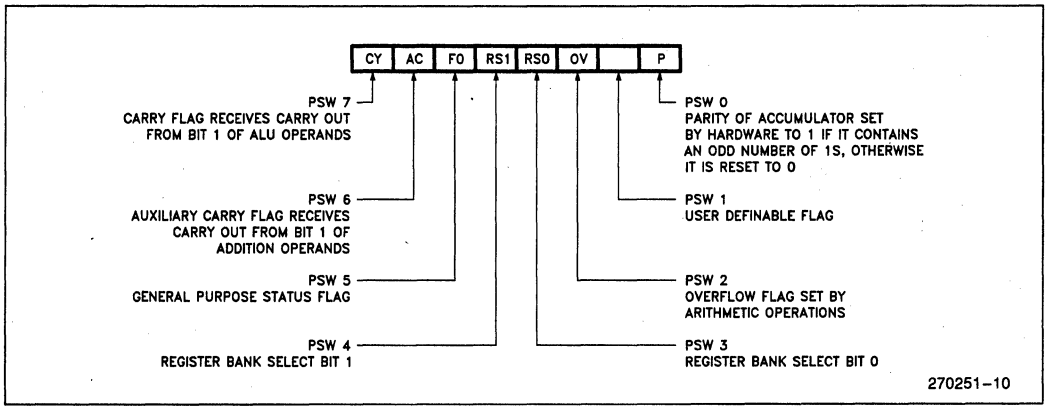

Figure 10. PSW (Program Status Word) Register in MCS®-51 Devices

The next 16 bytes above the register banks form a block of bit-addressable memory space. The MCS-51 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the Lower 128 can be accessed by either direct or indirect addressing. The Upper 128 (Figure 8) can only be accessed by indirect addressing. The Upper 128 bytes of RAM are not implemented in the 8051, but are in the devices with 256 bytes of RAM. (See Table 1).

Figure 9 gives a brief look at the Special Function Register (SFR) space. SFRs include the Port latches, timers, peripheral controls, etc. These registers can only be accessed by direct addressing. In general, all MCS-51 microcontrollers have the same SFRs as the 8051, and at the same addresses in SFR space. However, enhancements to the 8051 have additional SFRs that are not present in the 8051, nor perhaps in other proliferations of the family.

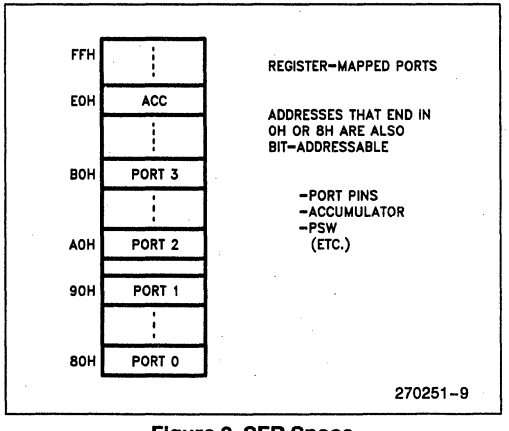

Figure 9. SFR Space

Sixteen addresses in SFR space are both byte- and bit-addressable. The bit-addressable SFRs are those whose address ends in 000B. The bit addresses in this area are 80H through FFH.

THE MCS®-51 INSTRUCTION SET

All members of the MCS-51 family execute the same instruction set. The MCS-51 instruction set is optimized for 8-bit control applications. It provides a variety of fast addressing modes for accessing the internal RAM to facilitate byte operations on small data structures. The instruction set provides extensive support for one-bit variables as a separate data type, allowing direct bit manipulation in control and logic systems that require Boolean processing.

An overview of the MCS-51 instruction set is presented below, with a brief description of how certain instructions might be used. References to "the assembler" in this discussion are to Intel's MCS-51 Macro Assembler, ASM51. More detailed information on the instruction set can be found in the MCS-51 Macro Assembler User's Guide (Order No. 9800937 for ISIS Systems, Order No. 122752 for DOS Systems).

Program Status Word

The Program Status Word (PSW) contains several status bits that reflect the current state of the CPU. The PSW, shown in Figure 10, resides in SFR space. It contains the Carry bit, the Auxiliary Carry (for BCD operations), the two register bank select bits, the Overflow flag, a Parity bit, and two user-definable status flags.

The Carry bit, other than serving the functions of a Carry bit in arithmetic operations, also serves as the "Accumulator" for a number of Boolean operations.

The bits RS0 and RS1 are used to select one of the four register banks shown in Figure 7. A number of instructions refer to these RAM locations as R0 through R7. The selection of which of the four banks is being referred to is made on the basis of the bits RS0 and RS1 at execution time.

The Parity bit reflects the number of 1s in the Accumulator: P = 1 if the Accumulator contains an odd number of 1s, and P = 0 if the Accumulator contains an even number of 1s. Thus the number of 1s in the Accumulator plus P is always even.

Two bits in the PSW are uncommitted and may be used as general purpose status flags.

Addressing Modes

The addressing modes in the MCS-51 instruction set are as follows:

DIRECT ADDRESSING

In direct addressing the operand is specified by an 8-bit address field in the instruction. Only internal Data RAM and SFRs can be directly addressed.

INDIRECT ADDRESSING

In indirect addressing the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed.

The address register for 8-bit addresses can be R0 or R1 of the selected register bank, or the Stack Pointer. The address register for 16-bit addresses can only be the 16-bit "data pointer" register, DPTR.

REGISTER INSTRUCTIONS

The register banks, containing registers R0 through R7, can be accessed by certain instructions which carry a 3-bit register specification within the opcode of the instruction. Instructions that access the registers this way are code efficient, since this mode eliminates an address byte. When the instruction is executed, one of the eight registers in the selected bank is accessed. One of four banks is selected at execution time by the two bank select bits in the PSW.

REGISTER-SPECIFIC INSTRUCTIONS

Some instructions are specific to a certain register. For example, some instructions always operate on the Accumulator, or Data Pointer, etc., so no address byte is needed to point to it. The opcode itself does that. Instructions that refer to the Accumlator as A assemble as accumulator-specific opcodes.

IMMEDIATE CONSTANTS

The value of a constant can follow the opcode in Program Memory. For example,

```
MOV A, #100
```

loads the Accumulator with the decimal number 100. The same number could be specified in hex digits as 64H.

INDEXED ADDRESSING

Only Program Memory can be accessed with indexed addressing, and it can only be read. This addressing mode is intended for reading look-up tables in Program Memory. A 16-bit base register (either DPTR or the Program Counter) points to the base of the table, and the Accumulator is set up with the table entry number. The address of the table entry in Program Memory is formed by adding the Accumulator data to the base pointer.

Another type of indexed addressing is used in the "case jump" instruction. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the Accumulator data.

Arithmetic Instructions

The menu of arithmetic instructions is listed in Table 2. The table indicates the addressing modes that can be used with each instruction to access the <byte> operand. For example, the ADD A,<byte> instruction can be written as:

```
ADD     A,7FH       (direct addressing)
ADD     A,@R0       (indirect addressing)
ADD     A,R7        (register addressing)
ADD     A,#127      (immediate constant)
```

The execution times listed in Table 2 assume a 12 MHz clock frequency. All of the arithmetic instructions execute in 1 μs except the INC DPTR instruction, which takes 2 μs, and the Multiply and Divide instructions, which take 4 μs.

Note that any byte in the internal Data Memory space can be incremented or decremented without going through the Accumulator.

One of the INC instructions operates on the 16-bit Data Pointer. The Data Pointer is used to generate 16-bit addresses for external memory, so being able to increment it in one 16-bit operation is a useful feature.

The MUL AB instruction multiplies the Accumulator by the data in the B register and puts the 16-bit product into the concatenated B and Accumulator registers.

Table 2. A List of the MCS®-51 Arithmetic Instructions

Mnemonic	Operation	Addressing Modes				Execution Time (μs)
		Dir	Ind	Reg	Imm	
ADD A,<byte>	A = A + <byte>	X	X	X	X	1
ADDC A,<byte>	A = A + <byte> + C	X	X	X	X	1
SUBB A,<byte>	A = A − <byte> − C	X	X	X	X	1
INC A	A = A + 1	Accumulator only				1
INC <byte>	<byte> = <byte> + 1	X	X	X		1
INC DPTR	DPTR = DPTR + 1	Data Pointer only				2
DEC A	A = A − 1	Accumulator only				1
DEC <byte>	<byte> = <byte> − 1	X	X	X		1
MUL AB	B:A = B x A	ACC and B only				4
DIV AB	A = Int [A/B] B = Mod [A/B]	ACC and B only				4
DA A	Decimal Adjust	Accumulator only				1

The DIV AB instruction divides the Accumulator by the data in the B register and leaves the 8-bit quotient in the Accumulator, and the 8-bit remainder in the B register.

Oddly enough, DIV AB finds less use in arithmetic "divide" routines than in radix conversions and programmable shift operations. An example of the use of DIV AB in a radix conversion will be given later. In shift operations, dividing a number by 2^n shifts its n bits to the right. Using DIV AB to perform the division completes the shift in 4 μs and leaves the B register holding the bits that were shifted out.

The DA A instruction is for BCD arithmetic operations. In BCD arithmetic, ADD and ADDC instructions should always be followed by a DA A operation, to ensure that the result is also in BCD. Note that DA A will not convert a binary number to BCD. The DA A operation produces a meaningful result only as the second step in the addition of two BCD bytes.

Table 3. A List of the MCS®-51 Logical Instructions

Mnemonic	Operation	Addressing Modes				Execution Time (μs)
		Dir	Ind	Reg	Imm	
ANL A,<byte>	A = A .AND. <byte>	X	X	X	X	1
ANL <byte>,A	<byte> = <byte> .AND. A	X				1
ANL <byte>,#data	<byte> = <byte> .AND. #data	X				2
ORL A,<byte>	A = A .OR. <byte>	X	X	X	X	1
ORL <byte>,A	<byte> = <byte> .OR. A	X				1
ORL <byte>,#data	<byte> = <byte> .OR. #data	X				2
XRL A,<byte>	A = A .XOR. <byte>	X	X	X	X	1
XRL <byte>,A	<byte> = <byte> .XOR. A	X				1
XRL <byte>,#data	<byte> = <byte> .XOR. #data	X				2
CRL A	A = 00H	Accumulator only				1
CPL A	A = .NOT. A	Accumulator only				1
RL A	Rotate ACC Left 1 bit	Accumulator only				1
RLC A	Rotate Left through Carry	Accumulator only				1
RR A	Rotate ACC Right 1 bit	Accumulator only				1
RRC A	Rotate Right through Carry	Accumulator only				1
SWAP A	Swap Nibbles in A	Accumulator only				1

Logical Instructions

Table 3 shows the list of MCS-51 logical instructions. The instructions that perform Boolean operations (AND, OR, Exclusive OR, NOT) on bytes perform the operation on a bit-by-bit basis. That is, if the Accumulator contains 00110101B and <byte> contains 01010011B, then

```
ANL     A,<byte>
```

will leave the Accumulator holding 00010001B.

The addressing modes that can be used to access the <byte> operand are listed in Table 3. Thus, the ANL A,<byte> instruction may take any of the forms

```
ANL     A,7FH       (direct addressing)
ANL     A,@R1       (indirect addressing)
ANL     A,R6        (register addressing)
ANL     A,#53H      (immediate constant)
```

All of the logical instructions that are Accumulator-specific execute in 1μs (using a 12 MHz clock). The others take 2 μs.

Note that Boolean operations can be performed on any byte in the lower 128 internal Data Memory space or the SFR space using direct addressing, without having to use the Accumulator. The XRL <byte>, #data instruction, for example, offers a quick and easy way to invert port bits, as in

```
XRL     P1,#0FFH
```

If the operation is in response to an interrupt, not using the Accumulator saves the time and effort to stack it in the service routine.

The Rotate instructions (RL A, RLC A, etc.) shift the Accumulator 1 bit to the left or right. For a left rotation, the MSB rolls into the LSB position. For a right rotation, the LSB rolls into the MSB position.

The SWAP A instruction interchanges the high and low nibbles within the Accumulator. This is a useful operation in BCD manipulations. For example, if the Accumulator contains a binary number which is known to be less than 100, it can be quickly converted to BCD by the following code:

```
MOV     B,#10
DIV     AB
SWAP    A
ADD     A,B
```

Dividing the number by 10 leaves the tens digit in the low nibble of the Accumulator, and the ones digit in the B register. The SWAP and ADD instructions move the tens digit to the high nibble of the Accumulator, and the ones digit to the low nibble.

Data Transfers

INTERNAL RAM

Table 4 shows the menu of instructions that are available for moving data around within the internal memory spaces, and the addressing modes that can be used with each one. With a 12 MHz clock, all of these instructions execute in either 1 or 2 μs.

The MOV <dest>, <src> instruction allows data to be transferred between any two internal RAM or SFR locations without going through the Accumulator. Remember the Upper 128 byes of data RAM can be accessed only by indirect addressing, and SFR space only by direct addressing.

Note that in all MCS-51 devices, the stack resides in on-chip RAM, and grows upwards. The PUSH instruction first increments the Stack Pointer (SP), then copies the byte into the stack. PUSH and POP use only direct addressing to identify the byte being saved or restored,

Table 4. A List of the MCS®-51 Data Transfer Instructions that Access Internal Data Memory Space

Mnemonic	Operation	Addressing Modes				Execution Time (μs)
		Dir	Ind	Reg	Imm	
MOV A,<src>	A = <src>	X	X	X	X	1
MOV <dest>,A	<dest> = A	X	X	X		1
MOV <dest>, <src>	<dest> = <src>	X	X	X	X	2
MOV DPTR,#data16	DPTR = 16-bit immediate constant.				X	2
PUSH <src>	INC SP : MOV "@SP",<src>	X				2
POP <dest>	MOV <dest>, "@SP" : DEC SP	X				2
XCH A,<byte>	ACC and <byte> exchange data	X	X	X		1
XCHD A,@Ri	ACC and @Ri exchange low nibbles		X			1

but the stack itself is accessed by indirect addressing using the SP register. This means the stack can go into the Upper 128, if they are implemented, but not into SFR space.

In devices that do not implement the Upper 128, if the SP points to the Upper 128, PUSHed bytes are lost, and POPped bytes are indeterminate.

The Data Transfer instructions include a 16-bit MOV that can be used to initialize the Data Pointer (DPTR) for look-up tables in Program Memory, or for 16-bit external Data Memory accesses.

The XCH A, <byte> instruction causes the Accumulator and addressed byte to exchange data. The XCHD A,@Ri instruction is similar, but only the low nibbles are involved in the exchange.

To see how XCH and XCHD can be used to facilitate data manipulations, consider first the problem of shifting an 8-digit BCD number two digits to the right. Figure 11 shows how this can be done using direct MOVs, and for comparison how it can be done using XCH instructions. To aid in understanding how the code works, the contents of the registers that are holding the BCD number and the content of the Accumulator are shown alongside each instruction to indicate their status after the instruction has been executed.

		2A	2B	2C	2D	2E	ACC
MOV	A,2EH	00	12	34	56	78	78
MOV	2EH,2DH	00	12	34	56	56	78
MOV	2DH,2CH	00	12	34	34	56	78
MOV	2CH,2BH	00	12	12	34	56	78
MOV	2BH,#0	00	00	12	34	56	78

(a) Using direct MOVs: 14 bytes, 9 μs

		2A	2B	2C	2D	2E	ACC
CLR	A	00	12	34	56	78	00
XCH	A,2BH	00	00	34	56	78	12
XCH	A,2CH	00	00	12	56	78	34
XCH	A,2DH	00	00	12	34	78	56
XCH	A,2EH	00	00	12	34	56	78

(b) Using XCHs: 9 bytes, 5 μs

Figure 11. Shifting a BCD Number Two Digits to the Right

After the routine has been executed, the Accumulator contains the two digits that were shifted out on the right. Doing the routine with direct MOVs uses 14 code bytes and 9 μs of execution time (assuming a 12 MHz clock). The same operation with XCHs uses less code and executes almost twice as fast.

To right-shift by an odd number of digits, a one-digit shift must be executed. Figure 12 shows a sample of code that will right-shift a BCD number one digit, using the XCHD instruction. Again, the contents of the registers holding the number and of the Accumulator are shown alongside each instruction.

			2A	2B	2C	2D	2E	ACC
	MOV	R1,#2EH	00	12	34	56	78	XX
	MOV	R0,#2DH	00	12	34	56	78	XX
	loop for R1 = 2EH:							
LOOP:	MOV	A,@R1	00	12	34	56	78	78
	XCHD	A,@R0	00	12	34	58	78	76
	SWAP	A	00	12	34	58	78	67
	MOV	@R1,A	00	12	34	58	67	67
	DEC	R1	00	12	34	58	67	67
	DEC	R0	00	12	34	58	67	67
	CJNE	R1,#2AH,LOOP						
	loop for R1 = 2DH:		00	12	38	45	67	45
	loop for R1 = 2CH:		00	18	23	45	67	23
	loop for R1 = 2BH:		08	01	23	45	67	01
	CLR	A	08	01	23	45	67	00
	XCH	A,2AH	00	01	23	45	67	08

Figure 12. Shifting a BCD Number One Digit to the Right

First, pointers R1 and R0 are set up to point to the two bytes containing the last four BCD digits. Then a loop is executed which leaves the last byte, location 2EH, holding the last two digits of the shifted number. The pointers are decremented, and the loop is repeated for location 2DH. The CJNE instruction (Compare and Jump if Not Equal) is a loop control that will be described later.

The loop is executed from LOOP to CJNE for R1 = 2EH, 2DH, 2CH and 2BH. At that point the digit that was originally shifted out on the right has propagated to location 2AH. Since that location should be left with 0s, the lost digit is moved to the Accumulator.

EXTERNAL RAM

Table 5 shows a list of the Data Transfer instructions that access external Data Memory. Only indirect addressing can be used. The choice is whether to use a one-byte address, @Ri, where Ri can be either R0 or R1 of the selected register bank, or a two-byte address, @DPTR. The disadvantage to using 16-bit addresses if only a few K bytes of external RAM are involved is that 16-bit addresses use all 8 bits of Port 2 as address bus. On the other hand, 8-bit addresses allow one to address a few K bytes of RAM, as shown in Figure 5, without having to sacrifice all of Port 2.

All of these instructions execute in 2 μs, with a 12 MHz clock.

Table 5. A List of the MCS®-51 Data Transfer Instructions that Access External Data Memory Space

Address Width	Mnemonic	Operation	Execution Time (μs)
8 bits	MOVX A,@Ri	Read external RAM @Ri	2
8 bits	MOVX @Ri,A	Write external RAM @Ri	2
16 bits	MOVX A,@DPTR	Read external RAM @DPTR	2
16 bits	MOVX @DPTR,A	Write external RAM @DPTR	2

Note that in all external Data RAM accesses, the Accumulator is always either the destination or source of the data.

The read and write strobes to external RAM are activated only during the execution of a MOVX instruction. Normally these signals are inactive, and in fact if they're not going to be used at all, their pins are available as extra I/O lines. More about that later.

LOOKUP TABLES

Table 6 shows the two instructions that are available for reading lookup tables in Program Memory. Since these instructions access only Program Memory, the lookup tables can only be read, not updated. The mnemonic is MOVC for "move constant".

If the table access is to external Program Memory, then the read strobe is $\overline{PSEN}$.

Table 6. The MCS®-51 Lookup Table Read Instructions

Mnemonic	Operation	Execution Time (μs)
MOVC A,@A+DPTR	Read Pgm Memory at (A+DPTR)	2
MOVC A,@A+PC	Read Pgm Memory at (A+PC)	2

The first MOVC instruction in Table 6 can accommodate a table of up to 256 entries, numbered 0 through 255. The number of the desired entry is loaded into the Accumulator, and the Data Pointer is set up to point to beginning of the table. Then

```
MOVC    A,@A+DPTR
```

copies the desired table entry into the Accumulator.

The other MOVC instruction works the same way, except the Program Counter (PC) is used as the table base, and the table is accessed through a subroutine. First the number of the desired entry is loaded into the Accumulator, and the subroutine is called:

```
        MOV     A,ENTRY_NUMBER
        CALL    TABLE
```

The subroutine "TABLE" would look like this:

```
TABLE:  MOVC    A,@A+PC
        RET
```

The table itself immediately follows the RET (return) instruction in Program Memory. This type of table can have up to 255 entries, numbered 1 through 255. Number 0 can not be used, because at the time the MOVC instruction is executed, the PC contains the address of the RET instruction. An entry numbered 0 would be the RET opcode itself.

Boolean Instructions

MCS-51 devices contain a complete Boolean (single-bit) processor. The internal RAM contains 128 addressable bits, and the SFR space can support up to 128 other addressable bits. All of the port lines are bit-addressable, and each one can be treated as a separate single-bit port. The instructions that access these bits are not just conditional branches, but a complete menu of move, set, clear, complement, OR, and AND instructions. These kinds of bit operations are not easily obtained in other architectures with any amount of byte-oriented software.

Table 7. A List of the MCS®-51 Boolean Instructions

Mnemonic		Operation	Execution Time (μs)
ANL	C,bit	C = C .AND. bit	2
ANL	C,/bit	C = C .AND. .NOT. bit	2
ORL	C,bit	C = C .OR. bit	2
ORL	C,/bit	C = C .OR. .NOT. bit	2
MOV	C,bit	C = bit	1
MOV	bit,C	bit = C	2
CLR	C	C = 0	1
CLR	bit	bit = 0	1
SETB	C	C = 1	1
SETB	bit	bit = 1	1
CPL	C	C = .NOT. C	1
CPL	bit	bit = .NOT. bit	1
JC	rel	Jump if C = 1	2
JNC	rel	Jump if C = 0	2
JB	bit,rel	Jump if bit = 1	2
JNB	bit,rel	Jump if bit = 0	2
JBC	bit,rel	Jump if bit = 1; CLR bit	2

The instruction set for the Boolean processor is shown in Table 7. All bit accesses are by direct addressing. Bit addresses 00H through 7FH are in the Lower 128, and bit addresses 80H through FFH are in SFR space.

Note how easily an internal flag can be moved to a port pin:

```
MOV   C,FLAG
MOV   P1.0,C
```

In this example, FLAG is the name of any addressable bit in the Lower 128 or SFR space. An I/O line (the LSB of Port 1, in this case) is set or cleared depending on whether the flag bit is 1 or 0.

The Carry bit in the PSW is used as the single-bit Accumulator of the Boolean processor. Bit instructions that refer to the Carry bit as C assemble as Carry-specific instructions (CLR C, etc). The Carry bit also has a direct address, since it resides in the PSW register, which is bit-addressable.

Note that the Boolean instruction set includes ANL and ORL operations, but not the XRL (Exclusive OR) operation. An XRL operation is simple to implement in software. Suppose, for example, it is required to form the Exclusive OR of two bits:

C = bit1 .XRL. bit2

The software to do that could be as follows:

```
      MOV   C,bit1
      JNB   bit2,OVER
      CPL   C
OVER: (continue)
```

First, bit1 is moved to the Carry. If bit2 = 0, then C now contains the correct result. That is, bit1 .XRL. bit2 = bit1 if bit2 = 0. On the other hand, if bit2 = 1 C now contains the complement of the correct result. It need only be inverted (CPL C) to complete the operation.

This code uses the JNB instruction, one of a series of bit-test instructions which execute a jump if the addressed bit is set (JC, JB, JBC) or if the addressed bit is not set (JNC, JNB). In the above case, bit2 is being tested, and if bit2 = 0 the CPL C instruction is jumped over.

JBC executes the jump if the addressed bit is set, and also clears the bit. Thus a flag can be tested and cleared in one operation.

All the PSW bits are directly addressable, so the Parity bit, or the general purpose flags, for example, are also available to the bit-test instructions.

RELATIVE OFFSET

The destination address for these jumps is specified to the assembler by a label or by an actual address in Program Memory. However, the destination address assembles to a **relative** offset byte. This is a signed (two's complement) offset byte which is added to the PC in two's complement arithmetic if the jump is executed.

The range of the jump is therefore −128 to +127 Program Memory bytes relative to the first byte following the instruction.

Jump Instructions

Table 8 shows the list of unconditional jumps.

Table 8. Unconditional Jumps in MCS®-51 Devices

Mnemonic	Operation	Execution Time (μs)
JMP addr	Jump to addr	2
JMP @A+DPTR	Jump to A+DPTR	2
CALL addr	Call subroutine at addr	2
RET	Return from subroutine	2
RETI	Return from interrupt	2
NOP	No operation	1

The Table lists a single "JMP addr" instruction, but in fact there are three—SJMP, LJMP and AJMP—which differ in the format of the destination address. JMP is a generic mnemonic which can be used if the programmer does not care which way the jump is encoded.

The SJMP instruction encodes the destination address as a relative offset, as described above. The instruction is 2 bytes long, consisting of the opcode and the relative offset byte. The jump distance is limited to a range of −128 to +127 bytes relative to the instruction following the SJMP.

The LJMP instruction encodes the destination address as a 16-bit constant. The instruction is 3 bytes long, consisting of the opcode and two address bytes. The destination address can be anywhere in the 64K Program Memory space.

The AJMP instruction encodes the destination address as an 11-bit constant. The instruction is 2 bytes long, consisting of the opcode, which itself contains 3 of the 11 address bits, followed by another byte containing the low 8 bits of the destination address. When the instruction is executed, these 11 bits are simply substituted for the low 11 bits in the PC. The high 5 bits stay the same. Hence the destination has to be within the same 2K block as the instruction following the AJMP.

In all cases the programmer specifies the destination address to the assembler in the same way: as a label or as a 16-bit constant. The assembler will put the destination address into the correct format for the given instruction. If the format required by the instruction will not support the distance to the specified destination address, a "Destination out of range" message is written into the List file.

The JMP @A+DPTR instruction supports case jumps. The destination address is computed at execution time as the sum of the 16-bit DPTR register and the Accumulator. Typically, DPTR is set up with the address of a jump table, and the Accumulator is given an index to the table. In a 5-way branch, for example, an integer 0 through 4 is loaded into the Accumulator. The code to be executed might be as follows:

```
MOV   DPTR,#JUMP_TABLE
MOV   A,INDEX_NUMBER
RL    A
JMP   @A+DPTR
```

The RL A instruction converts the index number (0 through 4) to an even number on the range 0 through 8, because each entry in the jump table is 2 bytes long:

```
JUMP_TABLE:
      AJMP    CASE_0
      AJMP    CASE_1
      AJMP    CASE_2
      AJMP    CASE_3
      AJMP    CASE_4
```

Table 8 shows a single "CALL addr" instruction, but there are two of them—LCALL and ACALL—which differ in the format in which the subroutine address is given to the CPU. CALL is a generic mnemonic which can be used if the programmer does not care which way the address is encoded.

The LCALL instruction uses the 16-bit address format, and the subroutine can be anywhere in the 64K Program Memory space. The ACALL instruction uses the 11-bit format, and the subroutine must be in the same 2K block as the instruction following the ACALL.

In any case the programmer specifies the subroutine address to the assembler in the same way: as a label or as a 16-bit constant. The assembler will put the address into the correct format for the given instructions.

Subroutines should end with a RET instruction, which returns execution to the instruction following the CALL.

RETI is used to return from an interrupt service routine. The only difference between RET and RETI is that RETI tells the interrupt control system that the interrupt in progress is done. If there is no interrupt in progress at the time RETI is executed, then the RETI is functionally identical to RET.

Table 9 shows the list of conditional jumps available to the MCS-51 user. All of these jumps specify the destination address by the relative offset method, and so are limited to a jump distance of −128 to +127 bytes from the instruction following the conditional jump instruction. Important to note, however, the user specifies to the assembler the actual destination address the same way as the other jumps: as a label or a 16-bit constant.

Table 9. Conditional Jumps in MCS®-51 Devices

Mnemonic	Operation	Addressing Modes				Execution Time (μs)
		Dir	Ind	Reg	Imm	
JZ rel	Jump if A = 0	Accumulator only				2
JNZ rel	Jump if A ≠ 0	Accumulator only				2
DJNZ <byte>,rel	Decrement and jump if not zero	X		X		2
CJNE A,<byte>,rel	Jump if A ≠ <byte>	X			X	2
CJNE <byte>,#data,rel	Jump if <byte> ≠ #data		X	X		2

There is no Zero bit in the PSW. The JZ and JNZ instructions test the Accumulator data for that condition.

The DJNZ instruction (Decrement and Jump if Not Zero) is for loop control. To execute a loop N times, load a counter byte with N and terminate the loop with a DJNZ to the beginning of the loop, as shown below for N = 10:

```
        MOV     COUNTER,#10
LOOP:   (begin loop)
          *
          *
          *
        (end loop)
        DJNZ    COUNTER,LOOP
        (continue)
```

The CJNE instruction (Compare and Jump if Not Equal) can also be used for loop control as in Figure 12. Two bytes are specified in the operand field of the instruction. The jump is executed only if the two bytes are not equal. In the example of Figure 12, the two bytes were the data in R1 and the constant 2AH. The initial data in R1 was 2EH. Every time the loop was executed, R1 was decremented, and the looping was to continue until the R1 data reached 2AH.

Another application of this instruction is in "greater than, less than" comparisons. The two bytes in the operand field are taken as unsigned integers. If the first is less than the second, then the Carry bit is set (1). If the first is greater than or equal to the second, then the Carry bit is cleared.

CPU TIMING

All MCS-51 microcontrollers have an on-chip oscillator which can be used if desired as the clock source for the CPU. To use the on-chip oscillator, connect a crystal or ceramic resonator between the XTAL1 and XTAL2 pins of the microcontroller, and capacitors to ground as shown in Figure 13.

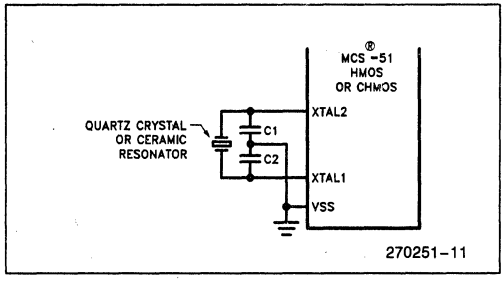

Figure 13. Using the On-Chip Oscillator

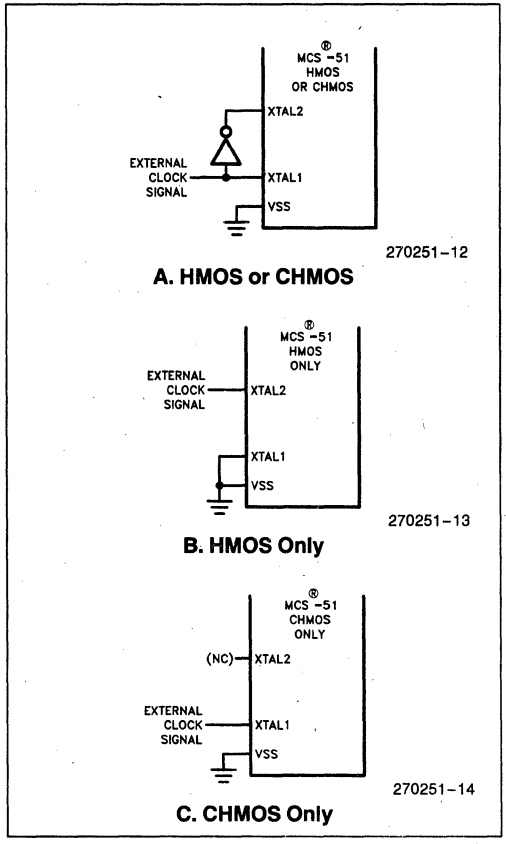

Figure 14. Using an External Clock

Examples of how to drive the clock with an external oscillator are shown in Figure 14. Note that in the HMOS devices (8051, etc.) the signal at the XTAL2 pin actually drives the internal clock generator. In the CHMOS devices (80C51BH, etc.) the signal at the XTAL1 pin drives the internal clock generator. If only one pin is going to be driven with the external oscillator signal, make sure it is the right pin.

The internal clock generator defines the sequence of states that make up the MCS-51 machine cycle.

Machine Cycles

A machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency is 12 MHz.

Each state is divided into a Phase 1 half and a Phase 2 half. Figure 15 shows the fetch/execute sequences in

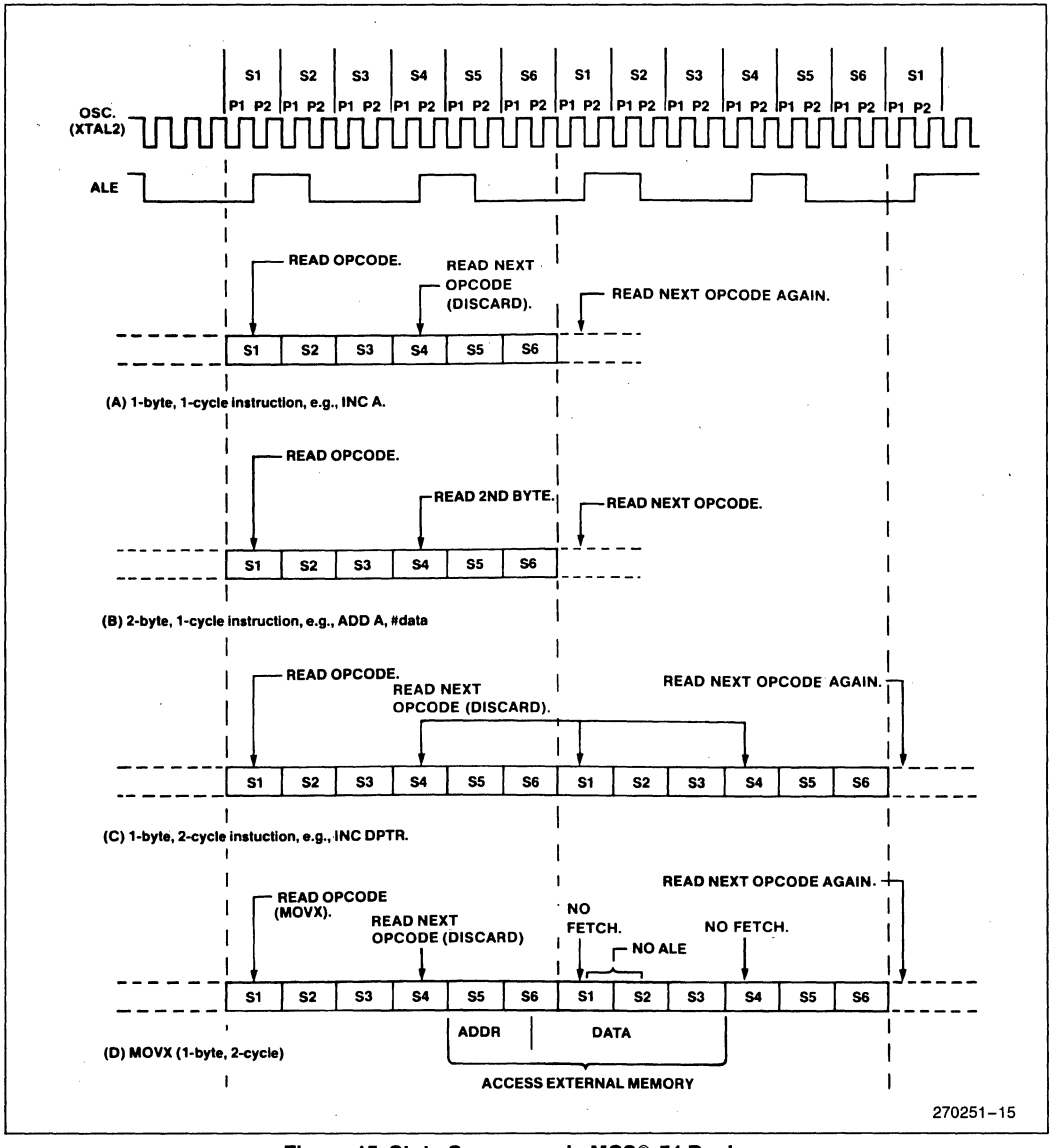

Figure 15. State Sequences in MCS®-51 Devices

states and phases for various kinds of instructions. Normally two program fetches are generated during each machine cycle, even if the instruction being executed doesn't require it. If the instruction being executed doesn't need more code bytes, the CPU simply ignores the extra fetch, and the Program Counter is not incremented.

Execution of a one-cycle instruction (Figure 15A and B) begins during State 1 of the machine cycle, when the opcode is latched into the Instruction Register. A second fetch occurs during S4 of the same machine cycle. Execution is complete at the end of State 6 of this machine cycle.

The MOVX instructions take two machine cycles to execute. No program fetch is generated during the second cycle of a MOVX instruction. This is the only time program fetches are skipped. The fetch/execute sequence for MOVX instructions is shown in Figure 15(D).

The fetch/execute sequences are the same whether the Program Memory is internal or external to the chip. Execution times do not depend on whether the Program Memory is internal or external.

Figure 16 shows the signals and timing involved in program fetches when the Program Memory is external. If Program Memory is external, then the Program Memory read strobe $\overline{PSEN}$ is normally activated twice per machine cycle, as shown in Figure 16(A).

If an access to external Data Memory occurs, as shown in Figure 16(B), two $\overline{PSEN}$s are skipped, because the address and data bus are being used for the Data Memory access.

Note that a Data Memory bus cycle takes twice as much time as a Program Memory bus cycle. Figure 16 shows the relative timing of the addresses being emitted at Ports 0 and 2, and of ALE and $\overline{PSEN}$. ALE is used to latch the low address byte from P0 into the address latch.

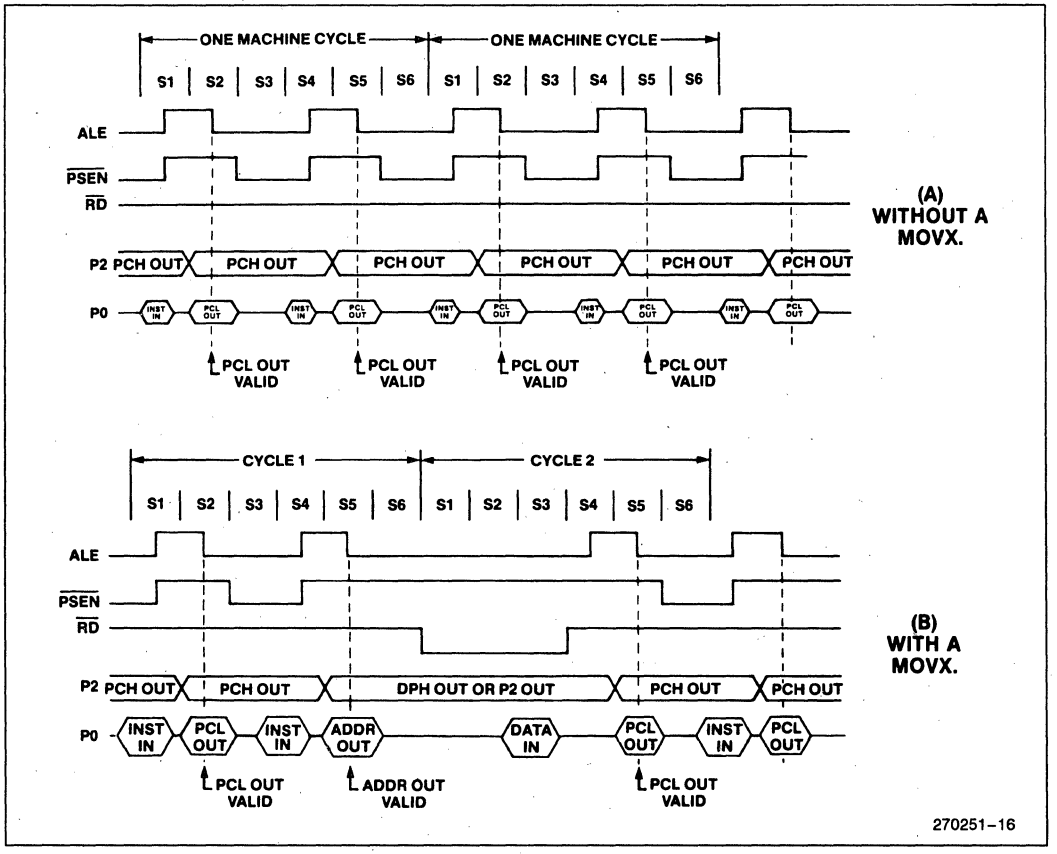

Figure 16. Bus Cycles in MCS®-51 Devices Executing from External Program Memory

When the CPU is executing from internal Program Memory, $\overline{PSEN}$ is not activated, and program addresses are not emitted. However, ALE continues to be activated twice per machine cycle and so is available as a clock output signal. Note, however, that one ALE is skipped during the execution of the MOVX instruction.

Interrupt Structure

The 8051 core provides 5 interrupt sources: 2 external interrupts, 2 timer interrupts, and the serial port interrupt. What follows is an overview of the interrupt structure for the 8051. Other MCS-51 devices have additional interrupt sources and vectors as shown in Table 1. Refer to the appropriate chapters on other devices for further information on their interrupts.

INTERRUPT ENABLES

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the SFR named IE (Interrupt Enable). This register also contains a global disable bit, which can be cleared to disable all interrupts at once. Figure 17 shows the IE register for the 8051.

(MSB)							(LSB)
EA	—	—	ES	ET1	EX1	ET0	EX0

Enable bit = 1 enables the interrupt.
Enable bit = 0 disables it.

Symbol	Position	Function
EA	IE.7	disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	reserved*
—	IE.5	reserved*
ES	IE.4	Serial Port Interrupt enable bit.
ET1	IE.3	Timer 1 Overflow Interrupt enable bit.
EX1	IE.2	External Interrupt 1 enable bit.
ET0	IE.1	Timer 0 Overflow Interrupt enable bit.
EX0	IE.0	External Interrupt 0 enable bit.

*These reserved bits are used in other MCS-51 devices.

Figure 17. IE (Interrupt Enable) Register in the 8051

INTERRUPT PRIORITIES

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in the SFR named IP (Interrupt Priority). Figure 18 shows the IP register in the 8051.

A low-priority interrrupt can be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Figure 19 shows, for the 8051, how the IE and IP registers and the polling sequence work to determine which if any interrupt will be serviced.

(MSB)							(LSB)
—	—	—	PS	PT1	PX1	PT0	PX0

Priority bit = 1 assigns high priority.
Priority bit = 0 assigns low priority.

Symbol	Position	Function
—	IP.7	reserved*
—	IP.6	reserved*
—	IP.5	reserved*
PS	IP.4	Serial Port interrupt priority bit.
PT1	IP.3	Timer 1 interrupt priority bit.
PX1	IP.2	External Interrupt 1 priority bit.
PT0	IP.1	Timer 0 interrupt priority bit.
PX0	IP.0	External Interrupt 0 priority bit.

*These reserved bits are used in other MCS-51 devices.

Figure 18. IP (Interrupt Priority) Register in the 8051

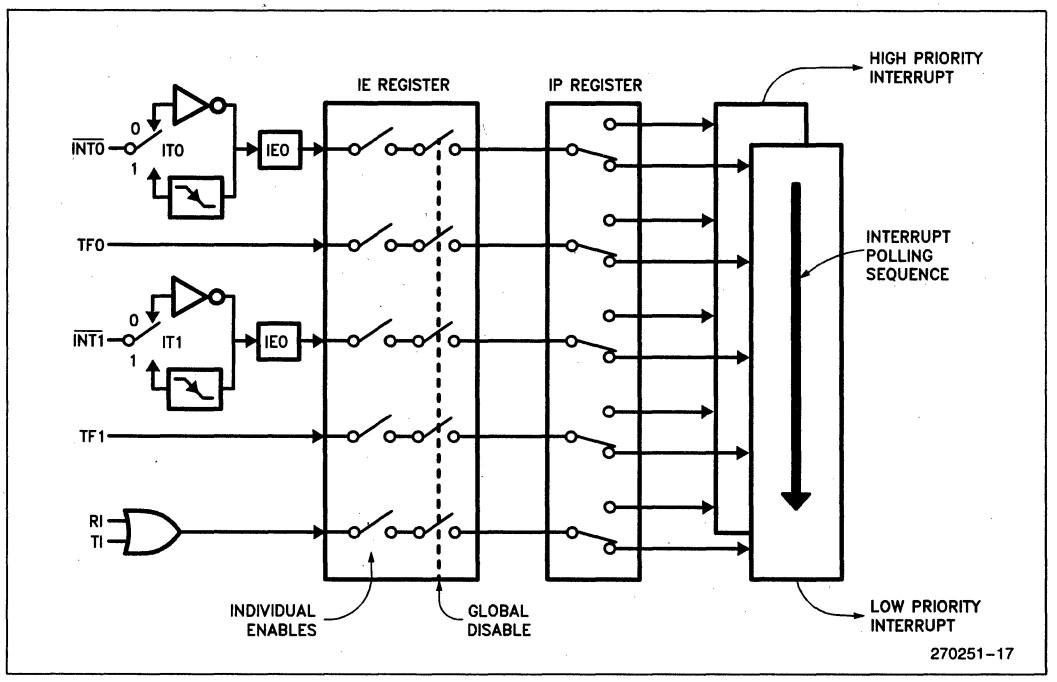

Figure 19. 8051 Interrupt Control System

In operation, all the interrupt flags are latched into the interrupt control system during State 5 of every machine cycle. The samples are polled during the following machine cycle. If the flag for an enabled interrupt is found to be set (1), the interrupt system generates an LCALL to the appropriate location in Program Memory, unless some other condition blocks the interrupt. Several conditions can block an interrupt, among them that an interrupt of equal or higher priority level is already in progress.

The hardware-generated LCALL causes the contents of the Program Counter to be pushed onto the stack, and reloads the PC with the beginning address of the service routine. As previously noted (Figure 3), the service routine for each interrupt begins at a fixed location.

Only the Program Counter is automatically pushed onto the stack, not the PSW or any other register. Having only the PC be automatically saved allows the programmer to decide how much time to spend saving which other registers. This enhances the interrupt response time, albeit at the expense of increasing the programmer's burden of responsibility. As a result, many interrupt functions that are typical in control applications—toggling a port pin, for example, or reloading a timer, or unloading a serial buffer—can often be completed in less time than it takes other architectures to commence them.

SIMULATING A THIRD PRIORITY LEVEL IN SOFTWARE

Some applications require more than the two priority levels that are provided by on-chip hardware in MCS-51 devices. In these cases, relatively simple software can be written to produce the same effect as a third priority level.

First, interrupts that are to have higher priority than 1 are assigned to priority 1 in the IP (Interrupt Priority) register. The service routines for priority 1 interrupts that are supposed to be interruptible by "priority 2" interrupts are written to include the following code:

```
        PUSH    IE
        MOV     IE,#MASK
        CALL    LABEL
          *******
(execute service routine)
          *******
        POP     IE
        RET
LABEL:  RETI
```

As soon as any priority 1 interrupt is acknowledged, the IE (Interrupt Enable) register is re-defined so as to disable all but "priority 2" interrupts. Then, a CALL to LABEL executes the RETI instruction, which clears the priority 1 interrupt-in-progress flip-flop. At this point any priority 1 interrupt that is enabled can be serviced, but only "priority 2" interrupts are enabled.

POPping IE restores the original enable byte. Then a normal RET (rather than another RETI) is used to terminate the service routine. The additional software adds 10 μs (at 12 MHz) to priority 1 interrupts.

ADDITIONAL REFERENCES

The following application notes are found in the *Embedded Control Applications* handbook. (Order Number: 270648)

1. AP-69 "An Introduction to the Intel MCS®-51 Single-Chip Microcomputer Family"
2. AP-70 "Using the Intel MCS®-51 Boolean Processing Capabilities"

MCS®-51 Programmer's Guide and Instruction Set

6

intel®

July 1989

MCS®-51 Programmer's Guide and Instruction Set

6

Order Number: 270249-003

MCS®-51 PROGRAMMER'S GUIDE AND INSTRUCTION SET

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The information presented in this chapter is collected from the MCS®-51 Architectural Overview and the Hardware Description of the 8051, 8052 and 80C51 chapters of this book. The material has been selected and rearranged to form a quick and convenient reference for the programmers of the MCS-51. This guide pertains specifically to the 8051, 8052 and 80C51.

MEMORY ORGANIZATION

PROGRAM MEMORY

The 8051 has separate address spaces for Program Memory and Data Memory. The Program Memory can be up to 64K bytes long. The lower 4K (8K for the 8052) may reside on-chip.

Figure 1 shows a map of the 8051 program memory, and Figure 2 shows a map of the 8052 program memory.

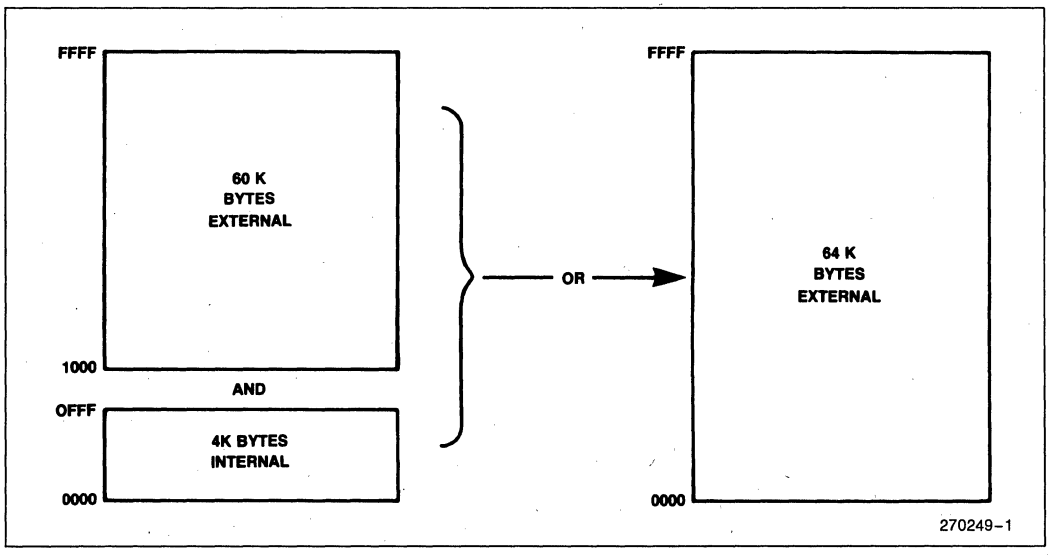


Figure 1. The 8051 Program Memory

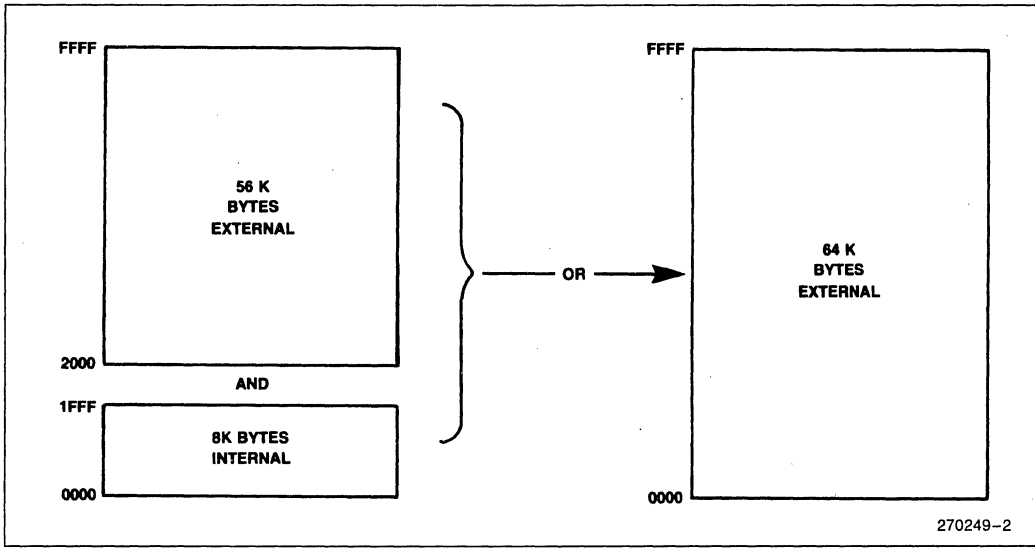


Figure 2. The 8052 Program Memory

Data Memory:

The 8051 can address up to 64K bytes of Data Memory external to the chip. The "MOVX" instruction is used to access the external data memory. (Refer to the MCS-51 Instruction Set, in this chapter, for detailed description of instructions).

The 8051 has 128 bytes of on-chip RAM (256 bytes in the 8052) plus a number of Special Function Registers (SFRs). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr) or by indirect addressing (MOV @Ri). Figure 3 shows the 8051 and the 8052 Data Memory organization.

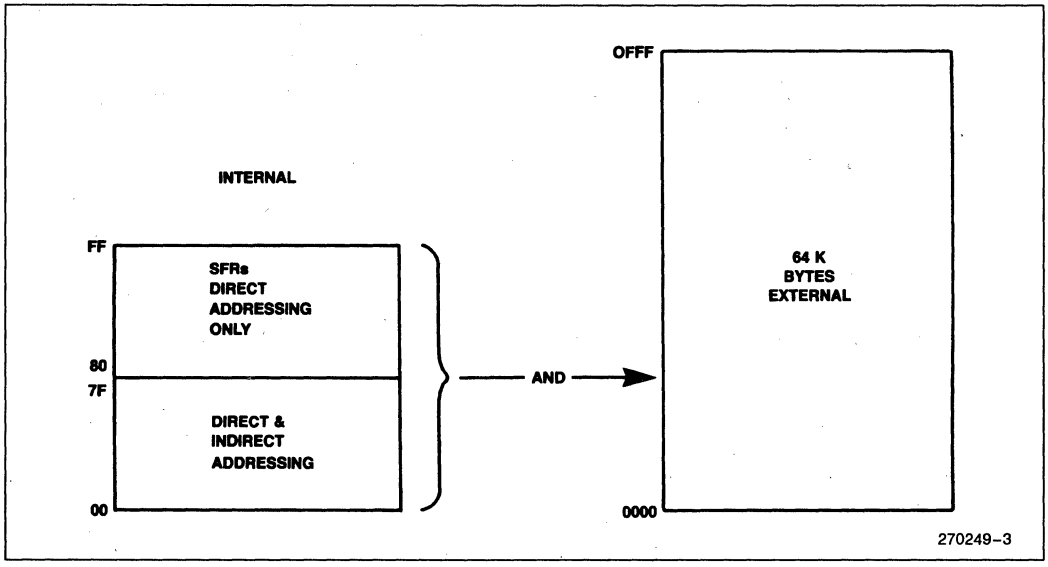


Figure 3a. The 8051 Data Memory

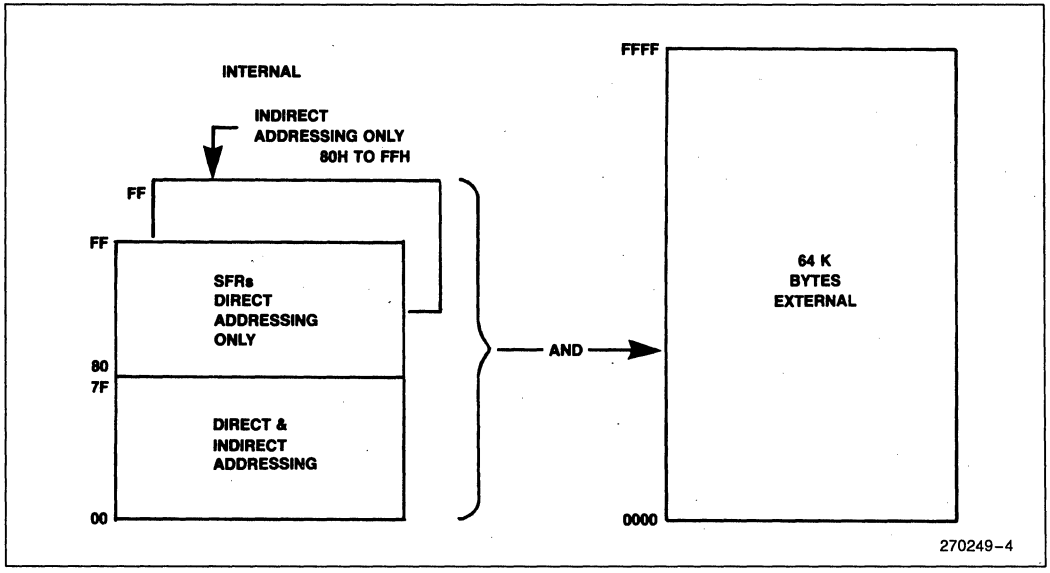


Figure 3b. The 8052 Data Memory

INDIRECT ADDRESS AREA:

Note that in Figure 3b the SFRs and the indirect address RAM have the same addresses (80H–0FFH). Nevertheless, they are two separate areas and are accessed in two different ways.

For example the instruction

```
MOV    80H,#0AAH
```

writes 0AAH to Port 0 which is one of the SFRs and the instruction

```
MOV    R0,#80H

MOV    @R0,#0BBH
```

writes 0BBH in location 80H of the data RAM. Thus, after execution of both of the above instructions Port 0 will contain 0AAH and location 80 of the RAM will contain 0BBH.

Note that the stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space in those devices which implement 256 bytes of internal RAM.

DIRECT AND INDIRECT ADDRESS AREA:

The 128 bytes of RAM which can be accessed by both direct and indirect addressing can be divided into 3 segments as listed below and shown in Figure 4.

1. Register Banks 0-3: Locations 0 through 1FH (32 bytes). ASM-51 and the device after reset default to register bank 0. To use the other register banks the user must select them in the software (refer to the MCS-51 Micro Assembler User's Guide). Each register bank contains 8 one-byte registers, 0 through 7.

Reset initializes the Stack Pointer to location 07H and it is incremented once to start from location 08H which is the first register (RO) of the second register bank. Thus, in order to use more than one register bank, the SP should be intialized to a different location of the RAM where it is not used for data storage (ie, higher part of the RAM).

2. Bit Addressable Area: 16 bytes have been assigned for this segment, 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH).

The bits can be referred to in two ways both of which are acceptable by the ASM-51. One way is to refer to their addresses, ie. 0 to 7FH. The other way is with reference to bytes 20H to 2FH. Thus, bits 0–7 can also be referred to as bits 20.0–20.7, and bits 8-FH are the same as 21.0–21.7 and so on.

Each of the 16 bytes in this segment can also be addressed as a byte.

3. Scratch Pad Area: Bytes 30H through 7FH are available to the user as data RAM. However, if the stack pointer has been initialized to this area, enough number of bytes should be left aside to prevent SP data destruction.

Figure 4 shows the different segments of the on-chip RAM.

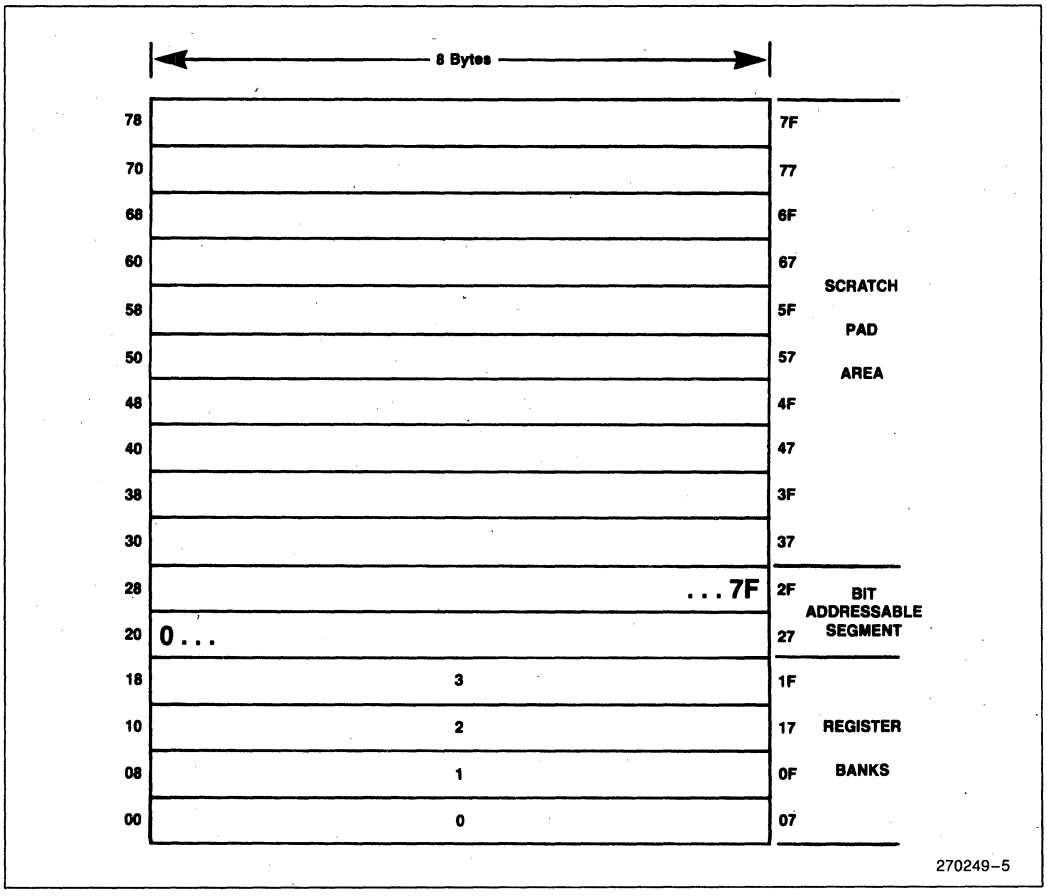


Figure 4. 128 Bytes of RAM Direct and Indirect Addressable

SPECIAL FUNCTION REGISTERS:

Table 1 contains a list of all the SFRs and their addresses.

Comparing Table 1 and Figure 5 shows that all of the SFRs that are byte and bit addressable are located on the first column of the diagram in Figure 5.

Table 1

Symbol	Name	Address
*ACC	Accumulator	0E0H
*B	B Register	0F0H
*PSW	Program Status Word	0D0H
SP	Stack Pointer	81H
DPTR	Data Pointer 2 Bytes	
DPL	Low Byte	82H
DPH	High Byte	83H
*P0	Port 0	80H
*P1	Port 1	90H
*P2	Port 2	0A0H
*P3	Port 3	0B0H
*IP	Interrupt Priority Control	0B8H
*IE	Interrupt Enable Control	0A8H
TMOD	Timer/Counter Mode Control	89H
*TCON	Timer/Counter Control	88H
*+T2CON	Timer/Counter 2 Control	0C8H
TH0	Timer/Counter 0 High Byte	8CH
TL0	Timer/Counter 0 Low Byte	8AH
TH1	Timer/Counter 1 High Byte	8DH
TL1	Timer/Counter 1 Low Byte	8BH
+TH2	Timer/Counter 2 High Byte	0CDH
+TL2	Timer/Counter 2 Low Byte	0CCH
+RCAP2H	T/C 2 Capture Reg. High Byte	0CBH
+RCAP2L	T/C 2 Capture Reg. Low Byte	0CAH
*SCON	Serial Control	98H
SBUF	Serial Data Buffer	99H
PCON	Power Control	87H

* = Bit addressable
\+ = 8052 only

WHAT DO THE SFRs CONTAIN JUST AFTER POWER-ON OR A RESET?

Table 2 lists the contents of each SFR after power-on or a hardware reset.

Table 2. Contents of the SFRs after reset

Register	Value in Binary
*ACC	00000000
*B	00000000
*PSW	00000000
SP	00000111
DPTR	
DPH	00000000
DPL	00000000
*P0	11111111
*P1	11111111
*P2	11111111
*P3	11111111
*IP	8051 XXX00000, 8052 XX000000
*IE	8051 0XX00000, 8052 0X000000
TMOD	00000000
*TCON	00000000
*+T2CON	00000000
TH0	00000000
TL0	00000000
TH1	00000000
TL1	00000000
+TH2	00000000
+TL2	00000000
+RCAP2H	00000000
+RCAP2L	00000000
*SCON	00000000
SBUF	Indeterminate
PCON	HMOS 0XXXXXXX CHMOS 0XXX0000

X = Undefined
* = Bit Addressable
+ = 8052 only

SFR MEMORY MAP

8 Bytes

F8								FF
F0	B							F7
E8								EF
E0	ACC							E7
D8								DF
D0	PSW							D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2		CF
C0								C7
B8	IP							BF
B0	P3							B7
A8	IE							AF
A0	P2							A7
98	SCON	SBUF						9F
90	P1							97
88	TCON	TMOD	TL0	TL1	TH0	TH1		8F
80	P0	SP	DPL	DPH				PCON 87

↑
Bit
Addressable

Figure 5

Those SFRs that have their bits assigned for various functions are listed in this section. A brief description of each bit is provided for quick reference. For more detailed information refer to the Architecture Chapter of this book.

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	—	P

CY PSW.7 Carry Flag.

AC PSW.6 Auxiliary Carry Flag.

F0 PSW.5 Flag 0 available to the user for general purpose.

RS1 PSW.4 Register Bank selector bit 1 (SEE NOTE 1).

RS0 PSW.3 Register Bank selector bit 0 (SEE NOTE 1).

OV PSW.2 Overflow Flag.

— PSW.1 User definable flag.

P PSW.0 Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator.

NOTE:
1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	Register Bank	Address
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

PCON: POWER CONTROL REGISTER. NOT BIT ADDRESSABLE.

SMOD	—	—	—	GF1	GF0	PD	IDL

SMOD Double baud rate bit. If Timer 1 is used to generate baud rate and SMOD = 1, the baud rate is doubled when the Serial Port is used in modes 1, 2, or 3.

— Not implemented, reserved for future use.*

— Not implemented, reserved for future use.*

— Not implemented, reserved for future use.*

GF1 General purpose flag bit.

GF0 General purpose flag bit.

PD Power Down bit. Setting this bit activates Power Down operation in the 80C51BH. (Available only in CHMOS).

IDL Idle Mode bit. Setting this bit activates Idle Mode operation in the 80C51BH. (Available only in CHMOS).

If 1s are written to PD and IDL at the same time, PD takes precedence.

*User software should not write 1s to reserved bits. These bits may be used in future MCS-51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

INTERRUPTS:

In order to use any of the interrupts in the MCS-51, the following three steps must be taken.

1. Set the EA (enable all) bit in the IE register to 1.
2. Set the corresponding individual interrupt enable bit in the IE register to 1.
3. Begin the interrupt service routine at the corresponding Vector Address of that interrupt. See Table below.

Interrupt Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI & TI	0023H
TF2 & EXF2	002BH

In addition, for external interrupts, pins $\overline{INT0}$ and $\overline{INT1}$ (P3.2 and P3.3) must be set to 1, and depending on whether the interrupt is to be level or transition activated, bits IT0 or IT1 in the TCON register may need to be set to 1.

ITx = 0 level activated

ITx = 1 transition activated

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	—	ET2	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Not implemented, reserved for future use.*
ET2	IE.5	Enable or disable the Timer 2 overflow or capture interrupt (8052 only).
ES	IE.4	Enable or disable the serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt.
EX1	IE.2	Enable or disable External Interrupt 1.
ET0	IE.1	Enable or disable the Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External Interrupt 0.

*User software should not write 1s to reserved bits. These bits may be used in future MCS-51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

ASSIGNING HIGHER PRIORITY TO ONE OR MORE INTERRUPTS:

In order to assign higher priority to an interrupt the corresponding bit in the IP register must be set to 1.

Remember that while an interrupt service is in progress, it cannot be interrupted by a lower or same level interrupt.

PRIORITY WITHIN LEVEL:

Priority within level is only to resolve simultaneous requests of the same priority level.

From high to low, interrupt sources are listed below:

IE0
TF0
IE1
TF1
RI or TI
TF2 or EXF2

IP: INTERRUPT PRIORITY REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is 1 the corresponding interrupt has a higher priority.

—	—	PT2	PS	PT1	PX1	PT0	PX0

— IP. 7 Not implemented, reserved for future use.*
— IP. 6 Not implemented, reserved for future use.*
PT2 IP. 5 Defines the Timer 2 interrupt priority level (8052 only).
PS IP. 4 Defines the Serial Port interrupt priority level.
PT1 IP. 3 Defines the Timer 1 interrupt priority level.
PX1 IP. 2 Defines External Interrupt 1 priority level.
PT0 IP. 1 Defines the Timer 0 interrupt priority level.
PX0 IP. 0 Defines the External Interrupt 0 priority level.

*User software should not write 1s to reserved bits. These bits may be used in future MCS-51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

TCON: TIMER/COUNTER CONTROL REGISTER. BIT ADDRESSABLE.

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1 TCON. 7 Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine.

TR1 TCON. 6 Timer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF.

TF0 TCON. 5 Timer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as processor vectors to the service routine.

TR0 TCON. 4 Timer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF.

IE1 TCON. 3 External Interrupt 1 edge flag. Set by hardware when External Interrupt edge is detected. Cleared by hardware when interrupt is processed.

IT1 TCON. 2 Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.

IE0 TCON. 1 External Interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by hardware when interrupt is processed.

IT0 TCON. 0 Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.

TMOD: TIMER/COUNTER MODE CONTROL REGISTER. NOT BIT ADDRESSABLE.

GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TIMER 1				TIMER 0			

GATE When TRx (in TCON) is set and GATE = 1, TIMER/COUNTERx will run only while INTx pin is high (hardware control). When GATE = 0, TIMER/COUNTERx will run only while TRx = 1 (software control).

C/$\overline{T}$ Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).

M1 Mode selector bit. (NOTE 1)

M0 Mode selector bit. (NOTE 1)

NOTE 1:

M1	M0		Operating Mode
0	0	0	13-bit Timer (MCS-48 compatible)
0	1	1	16-bit Timer/Counter
1	0	2	8-bit Auto-Reload Timer/Counter
1	1	3	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits, TH0 is an 8-bit Timer and is controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/Counter 1 stopped.

TIMER SET-UP

Tables 3 through 6 give some values for TMOD which can be used to set up Timer 0 in different modes.

It is assumed that only one timer is being used at a time. If it is desired to run Timers 0 and 1 simultaneously, in any mode, the value in TMOD for Timer 0 must be ORed with the value shown for Timer 1 (Tables 5 and 6).

For example, if it is desired to run Timer 0 in mode 1 GATE (external control), and Timer 1 in mode 2 COUNTER, then the value that must be loaded into TMOD is 69H (09H from Table 3 ORed with 60H from Table 6).

Moreover, it is assumed that the user, at this point, is not ready to turn the timers on and will do that at a different point in the program by setting bit TRx (in TCON) to 1.

TIMER/COUNTER 0

As a Timer:

Table 3

MODE	TIMER 0 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13-bit Timer	00H	08H
1	16-bit Timer	01H	09H
2	8-bit Auto-Reload	02H	0AH
3	two 8-bit Timers	03H	0BH

As a Counter:

Table 4

MODE	COUNTER 0 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13-bit Timer	04H	0CH
1	16-bit Timer	05H	0DH
2	8-bit Auto-Reload	06H	0EH
3	one 8-bit Counter	07H	0FH

NOTES:
1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on $\overline{INT0}$ (P3.2) when TR0 = 1 (hardware control).

TIMER/COUNTER 1

As a Timer:

Table 5

MODE	TIMER 1 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13-bit Timer	00H	80H
1	16-bit Timer	10H	90H
2	8-bit Auto-Reload	20H	A0H
3	does not run	30H	B0H

As a Counter:

Table 6

MODE	COUNTER 1 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13-bit Timer	40H	C0H
1	16-bit Timer	50H	D0H
2	8-bit Auto-Reload	60H	E0H
3	not available	—	—

NOTES:
1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on $\overline{INT1}$ (P3.3) when TR1 = 1 (hardware control).

T2CON: TIMER/COUNTER 2 CONTROL REGISTER. BIT ADDRESSABLE

8052 Only

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

TF2 T2CON. 7 Timer 2 overflow flag set by hardware and cleared by software. TF2 cannot be set when either RCLK = 1 or CLK = 1

EXF2 T2CON. 6 Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX, and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.

RCLK T2CON. 5 Receive clock flag. When set, causes the Serial Port to use Timer 2 overflow pulses for its receive clock in modes 1 & 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

TLCK T2CON. 4 Transmit clock flag. When set, causes the Serial Port to use Timer 2 overflow pulses for its transmit clock in modes 1 & 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.

EXEN2 T2CON. 3 Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of negative transition on T2EX if Timer 2 is not being used to clock the Serial Port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.

TR2 T2CON. 2 Software START/STOP control for Timer 2. A logic 1 starts the Timer.

C/$\overline{T2}$ T2CON. 1 Timer or Counter select.

0 = Internal Timer. 1 = External Event Counter (falling edge triggered).

CP/$\overline{RL2}$ T2CON. 0 Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, Auto-Reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the Timer is forced to Auto-Reload on Timer 2 overflow.

TIMER/COUNTER 2 SET-UP

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the Timer on.

As a Timer:

Table 7

MODE	T2CON	
	INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
BAUD rate generator receive & transmit same baud rate	34H	36H
receive only	24H	26H
transmit only	14H	16H

As a Counter:

Table 8

MODE	TMOD	
	INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
16-bit Auto-Reload	02H	0AH
16-bit Capture	03H	0BH

NOTES:
1. Capture/Reload occurs only on Timer/Counter overflow.
2. Capture/Reload occurs on Timer/Counter overflow and a 1 to 0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generating mode.

SCON: SERIAL PORT CONTROL REGISTER. BIT ADDRESSABLE.

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SM0 SCON. 7 Serial Port mode specifier. (NOTE 1).

SM1 SCON. 6 Serial Port mode specifier. (NOTE 1).

SM2 SCON. 5 Enables the multiprocessor communication feature in modes 2 & 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0. (See Table 9).

REN SCON. 4 Set/Cleared by software to Enable/Disable reception.

TB8 SCON. 3 The 9th bit that will be transmitted in modes 2 & 3. Set/Cleared by software.

RB8 SCON. 2 In modes 2 & 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.

TI SCON. 1 Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software.

RI SCON. 0 Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes (except see SM2). Must be cleared by software.

NOTE 1:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	SHIFT REGISTER	Fosc./12
0	1	1	8-Bit UART	Variable
1	0	2	9-Bit UART	Fosc./64 OR Fosc./32
1	1	3	9-Bit UART	Variable

SERIAL PORT SET-UP:

Table 9

MODE	SCON	SM2 VARIATION
0 1 2 3	10H 50H 90H D0H	Single Processor Environment (SM2 = 0)
0 1 2 3	NA 70H B0H F0H	Multiprocessor Environment (SM2 = 1)

GENERATING BAUD RATES

Serial Port in Mode 0:

Mode 0 has a fixed baud rate which is 1/12 of the oscillator frequency. To run the serial port in this mode none of the Timer/Counters need to be set up. Only the SCON register needs to be defined.

$$\text{Baud Rate} = \frac{\text{Osc Freq}}{12}$$

Serial Port in Mode 1:

Mode 1 has a variable baud rate. The baud rate can be generated by either Timer 1 or Timer 2 (8052 only).

USING TIMER/COUNTER 1 TO GENERATE BAUD RATES:

For this purpose, Timer 1 is used in mode 2 (Auto-Reload). Refer to Timer Setup section of this chapter.

$$\text{Baud Rate} = \frac{\text{K x Oscillator Freq.}}{32 \times 12 \times [256 - (\text{TH1})]}$$

If SMOD = 0, then K = 1.
If SMOD = 1, then K = 2. (SMOD is the PCON register).

Most of the time the user knows the baud rate and needs to know the reload value for TH1.
Therefore, the equation to calculate TH1 can be written as:

$$\text{TH1} = 256 - \frac{\text{K x Osc Freq.}}{384 \times \text{baud rate}}$$

TH1 must be an integer value. Rounding off TH1 to the nearest integer may not produce the desired baud rate. In this case, the user may have to choose another crystal frequency.

Since the PCON register is not bit addressable, one way to set the bit is logical ORing the PCON register. (ie, ORL PCON,#80H). The address of PCON is 87H.

USING TIMER/COUNTER 2 TO GENERATE BAUD RATES:

For this purpose, Timer 2 must be used in the baud rate generating mode. Refer to Timer 2 Setup Table in this chapter. If Timer 2 is being clocked through pin T2 (P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

And if it is being clocked internally the baud rate is:

$$\text{Baud Rate} = \frac{\text{Osc Freq}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

To obtain the reload value for RCAP2H and RCAP2L the above equation can be rewritten as:

$$\text{RCAP2H, RCAP2L} = 65536 - \frac{\text{Osc Freq}}{32 \times \text{Baud Rate}}$$

SERIAL PORT IN MODE 2:

The baud rate is fixed in this mode and is $1/32$ or $1/64$ of the oscillator frequency depending on the value of the SMOD bit in the PCON register.

In this mode none of the Timers are used and the clock comes from the internal phase 2 clock.

SMOD = 1, Baud Rate = $1/32$ Osc Freq.

SMOD = 0, Baud Rate = $1/64$ Osc Freq.

To set the SMOD bit: ORL PCON,#80H. The address of PCON is 87H.

SERIAL PORT IN MODE 3:

The baud rate in mode 3 is variable and sets up exactly the same as in mode 1.

MCS®-51 INSTRUCTION SET

Table 10. 8051 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings(1)

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	O		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	O	X		ANL C,/bit	X		
DIV	O	X		ORL C,bit	X		
DA	X			ORL C,bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

(1)Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Note on instruction set and addressing modes:

Rn — Register R7–R0 of the currently selected Register Bank.

direct — 8-bit internal data location's address. This could be an Internal Data RAM location (0–127) or a SFR [i.e., I/O port, control register, status register, etc. (128–255)].

@Ri — 8-bit internal data RAM location (0–255) addressed indirectly through register R1 or R0.

#data — 8-bit constant included in instruction.

#data 16 — 16-bit constant included in instruction.

addr 16 — 16-bit destination address. Used by LCALL & LJMP. A branch can be anywhere within the 64K-byte Program Memory address space.

addr 11 — 11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.

rel — Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to +127 bytes relative to first byte of the following instruction.

bit — Direct Addressed bit in Internal Data RAM or Special Function Register.

Mnemonic		Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	12
ADD	A,direct	Add direct byte to Accumulator	2	12
ADD	A,@Ri	Add indirect RAM to Accumulator	1	12
ADD	A,#data	Add immediate data to Accumulator	2	12
ADDC	A,Rn	Add register to Accumulator with Carry	1	12
ADDC	A,direct	Add direct byte to Accumulator with Carry	2	12
ADDC	A,@Ri	Add indirect RAM to Accumulator with Carry	1	12
ADDC	A,#data	Add immediate data to Acc with Carry	2	12
SUBB	A,Rn	Subtract Register from Acc with borrow	1	12
SUBB	A,direct	Subtract direct byte from Acc with borrow	2	12
SUBB	A,@Ri	Subtract indirect RAM from ACC with borrow	1	12
SUBB	A,#data	Subtract immediate data from Acc with borrow	2	12
INC	A	Increment Accumulator	1	12
INC	Rn	Increment register	1	12
INC	direct	Increment direct byte	2	12
INC	@Ri	Increment direct RAM	1	12
DEC	A	Decrement Accumulator	1	12
DEC	Rn	Decrement Register	1	12
DEC	direct	Decrement direct byte	2	12
DEC	@Ri	Decrement indirect RAM	1	12

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
ARITHMETIC OPERATIONS (Continued)				
INC	DPTR	Increment Data Pointer	1	24
MUL	AB	Multiply A & B	1	48
DIV	AB	Divide A by B	1	48
DA	A	Decimal Adjust Accumulator	1	12
LOGICAL OPERATIONS				
ANL	A,Rn	AND Register to Accumulator	1	12
ANL	A,direct	AND direct byte to Accumulator	2	12
ANL	A,@Ri	AND indirect RAM to Accumulator	1	12
ANL	A,#data	AND immediate data to Accumulator	2	12
ANL	direct,A	AND Accumulator to direct byte	2	12
ANL	direct,#data	AND immediate data to direct byte	3	24
ORL	A,Rn	OR register to Accumulator	1	12
ORL	A,direct	OR direct byte to Accumulator	2	12
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12
ORL	A,#data	OR immediate data to Accumulator	2	12
ORL	direct,A	OR Accumulator to direct byte	2	12
ORL	direct,#data	OR immediate data to direct byte	3	24
XRL	A,Rn	Exclusive-OR register to Accumulator	1	12
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR	A	Clear Accumulator	1	12
CPL	A	Complement Accumulator	1	12

Mnemonic		Description	Byte	Oscillator Period
LOGICAL OPERATIONS (Continued)				
RL	A	Rotate Accumulator Left	1	12
RLC	A	Rotate Accumulator Left through the Carry	1	12
RR	A	Rotate Accumulator Right	1	12
RRC	A	Rotate Accumulator Right through the Carry	1	12
SWAP	A	Swap nibbles within the Accumulator	1	12
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	12
MOV	A,direct	Move direct byte to Accumulator	2	12
MOV	A,@Ri	Move indirect RAM to Accumulator	1	12
MOV	A,#data	Move immediate data to Accumulator	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	Rn,#data	Move immediate data to register	2	12
MOV	direct,A	Move Accumulator to direct byte	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct byte	2	24
MOV	direct,#data	Move immediate data to direct byte	3	24
MOV	@Ri,A	Move Accumulator to indirect RAM	1	12

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
DATA TRANSFER (Continued)				
MOV	@Ri,direct	Move direct byte to indirect RAM	2	24
MOV	@Ri,#data	Move immediate data to indirect RAM	2	12
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	24
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to Acc	1	24
MOVC	A,@A+PC	Move Code byte relative to PC to Acc	1	24
MOVX	A,@Ri	Move External RAM (8-bit addr) to Acc	1	24
MOVX	A,@DPTR	Move External RAM (16-bit addr) to Acc	1	24
MOVX	@Ri,A	Move Acc to External RAM (8-bit addr)	1	24
MOVX	@DPTR,A	Move Acc to External RAM (16-bit addr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accumulator	1	12
XCH	A,direct	Exchange direct byte with Accumulator	2	12
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD	A,@Ri	Exchange low-order Digit indirect RAM with Acc	1	12

Mnemonic		Description	Byte	Oscillator Period
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear Carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set Carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement Carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to CARRY	2	24
ANL	C,/bit	AND complement of direct bit to Carry	2	24
ORL	C,bit	OR direct bit to Carry	2	24
ORL	C,/bit	OR complement of direct bit to Carry	2	24
MOV	C,bit	Move direct bit to Carry	2	12
MOV	bit,C	Move Carry to direct bit	2	24
JC	rel	Jump if Carry is set	2	24
JNC	rel	Jump if Carry not set	2	24
JB	bit,rel	Jump if direct Bit is set	3	24
JNB	bit,rel	Jump if direct Bit is Not set	3	24
JBC	bit,rel	Jump if direct Bit is set & clear bit	3	24
PROGRAM BRANCHING				
ACALL	addr11	Absolute Subroutine Call	2	24
LCALL	addr16	Long Subroutine Call	3	24
RET		Return from Subroutine	1	24
RETI		Return from interrupt	1	24
AJMP	addr11	Absolute Jump	2	24
LJMP	addr16	Long Jump	3	24
SJMP	rel	Short Jump (relative addr)	2	24

Table 10. 8051 Instruction Set Summary (Continued)

Mnemonic		Description	Byte	Oscillator Period
PROGRAM BRANCHING (Continued)				
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is Zero	2	24
JNZ	rel	Jump if Accumulator is Not Zero	2	24
CJNE	A,direct,rel	Compare direct byte to Acc and Jump if Not Equal	3	24
CJNE	A,#data,rel	Compare immediate to Acc and Jump if Not Equal	3	24
CJNE	Rn,#data,rel	Compare immediate to register and Jump if Not Equal	3	24
CJNE	@Ri,#data,rel	Compare immediate to indirect and Jump if Not Equal	3	24
DJNZ	Rn,rel	Decrement register and Jump if Not Zero	2	24
DJNZ	direct,rel	Decrement direct byte and Jump if Not Zero	3	24
NOP		No Operation	1	12

Table 11. Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	code addr
02	3	LJMP	code addr
03	1	RR	A
04	1	INC	A
05	2	INC	data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	bit addr, code addr
11	2	ACALL	code addr
12	3	LCALL	code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	bit addr, code addr
21	2	AJMP	code addr
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,data addr
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	bit addr, code addr
31	2	ACALL	code addr
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,data addr
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	code addr
41	2	AJMP	code addr
42	2	ORL	data addr,A
43	3	ORL	data addr,#data
44	2	ORL	A,#data
45	2	ORL	A,data addr
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	code addr
51	2	ACALL	code addr
52	2	ANL	data addr,A
53	3	ANL	data addr,#data
54	2	ANL	A,#data
55	2	ANL	A,data addr
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	code addr
61	2	AJMP	code addr
62	2	XRL	data addr,A
63	3	XRL	data addr,#data
64	2	XRL	A,#data
65	2	XRL	A,data addr

Table 11. Instruction Opcodes in Hexadecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	ORL	C,bit addr
73	1	JMP	@A+DPTR
74	2	MOV	A,#data
75	3	MOV	data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data
7F	2	MOV	R7,#data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	data addr, data addr
86	2	MOV	data addr,@R0
87	2	MOV	data addr,@R1
88	2	MOV	data addr,R0
89	2	MOV	data addr,R1
8A	2	MOV	data addr,R2
8B	2	MOV	data addr,R3
8C	2	MOV	data addr,R4
8D	2	MOV	data addr,R5
8E	2	MOV	data addr,R6
8F	2	MOV	data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	code addr
92	2	MOV	bit addr,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/bit addr
A1	2	AJMP	code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,/bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Table 11. Instruction Opcodes in Hexadecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

INSTRUCTION DEFINITIONS

ACALL addr11

Function: Absolute Call

Description: ACALL unconditionally calls a subroutine located at the indicated address. The instruction increments the PC twice to obtain the address of the following instruction, then pushes the 16-bit result onto the stack (low-order byte first) and increments the Stack Pointer twice. The destination address is obtained by successively concatenating the five high-order bits of the incremented PC, opcode bits 7-5, and the second byte of the instruction. The subroutine called must therefore start within the same 2K block of the program memory as the first byte of the instruction following ACALL. No flags are affected.

Example: Initially SP equals 07H. The label "SUBRTN" is at program memory location 0345 H. After executing the instruction,

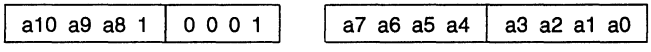
ACALL SUBRTN

at location 0123H, SP will contain 09H, internal RAM locations 08H and 09H will contain 25H and 01H, respectively, and the PC will contain 0345H.

Bytes: 2

Cycles: 2

Encoding:



Operation: ACALL
(PC) ← (PC) + 2
(SP) ← (SP) + 1
((SP)) ← (PC_{7-0})
(SP) ← (SP) + 1
((SP)) ← (PC_{15-8})
(PC_{10-0}) ← page address

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ADD A,<src-byte>

Function: Add

Description: ADD adds the byte variable indicated to the Accumulator, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occured.

OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands, or a positive sum from two negative operands.

Four source operand addressing modes are allowed: register, direct, register-indirect, or immediate.

Example: The Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B). The instruction,

ADD A,R0

will leave 6DH (01101101B) in the Accumulator with the AC flag cleared and both the carry flag and OV set to 1.

ADD A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 1 0	1 r r r

Operation: ADD
(A) ← (A) + (Rn)

ADD A,direct

Bytes: 2

Cycles: 1

Encoding:

0 0 1 0	0 1 0 1	direct address

Operation: ADD
(A) ← (A) + (direct)

ADD A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 1 0	0 1 1 i

Operation: ADD
(A) ← (A) + ((Ri))

ADD A,#data

Bytes: 2

Cycles: 1

Encoding:

0 0 1 0	0 1 0 0	immediate data

Operation: ADD
(A) ← (A) + #data

ADDC A,<src-byte>

Function: Add with Carry

Description: ADDC simultaneously adds the byte variable indicated, the carry flag and the Accumulator contents, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occured.

OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not out of bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands or a positive sum from two negative operands.

Four source operand addressing modes are allowed: register, direct, register-indirect, or immediate.

Example: The Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B) with the carry flag set. The instruction,

ADDC A,R0

will leave 6EH (01101110B) in the Accumulator with AC cleared and both the Carry flag and OV set to 1.

ADDC A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 1 1	1 r r r

Operation: ADDC
(A) ← (A) + (C) + (R_n)

ADDC A,direct

Bytes: 2

Cycles: 1

Encoding:

0 0 1 1	0 1 0 1	direct address

Operation: ADDC
(A) ← (A) + (C) + (direct)

ADDC A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 1 1	0 1 1 i

Operation: ADDC
(A) ← (A) + (C) + ((R_i))

ADDC A,#data

Bytes: 2

Cycles: 1

Encoding:

0 0 1 1	0 1 0 0	immediate data

Operation: ADDC
(A) ← (A) + (C) + #data

AJMP addr11

Function: Absolute Jump

Description: AJMP transfers program execution to the indicated address, which is formed at run-time by concatenating the high-order five bits of the PC (*after* incrementing the PC twice), opcode bits 7-5, and the second byte of the instruction. The destination must therefore be within the same 2K block of program memory as the first byte of the instruction following AJMP.

Example: The label "JMPADR" is at program memory location 0123H. The instruction,

```
AJMP   JMPADR
```

is at location 0345H and will load the PC with 0123H.

Bytes: 2

Cycles: 2

Encoding:

a10 a9 a8 0	0 0 0 1	a7 a6 a5 a4	a3 a2 a1 a0

Operation: AJMP
(PC) ← (PC) + 2
($PC_{10\text{-}0}$) ← page address

ANL <dest-byte>,<src-byte>

Function: Logical-AND for byte variables

Description: ANL performs the bitwise logical-AND operation between the variables indicated and stores the results in the destination variable. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: If the Accumulator holds 0C3H (11000011B) and register 0 holds 55H (01010101B) then the instruction,

```
ANL   A,R0
```

will leave 41H (01000001B) in the Accumulator.

When the destination is a directly addressed byte, this instruction will clear combinations of bits in any RAM location or hardware register. The mask byte determining the pattern of bits to be cleared would either be a constant contained in the instruction or a value computed in the Accumulator at run-time. The instruction,

```
ANL   P1,#01110011B
```

will clear bits 7, 3, and 2 of output port 1.

ANL A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 1 0 1	1 r r r

Operation: ANL
(A) ← (A) ∧ (Rn)

ANL A,direct

Bytes: 2

Cycles: 1

Encoding:

0 1 0 1	0 1 0 1	direct address

Operation: ANL

(A) ← (A) ∧ (direct)

ANL A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 1 0 1	0 1 1 i

Operation: ANL

(A) ← (A) ∧ ((Ri))

ANL A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 0 1	0 1 0 0	immediate data

Operation: ANL
(A) ← (A) ∧ #data

ANL direct,A

Bytes: 2

Cycles: 1

Encoding:

0 1 0 1	0 0 1 0	direct address

Operation: ANL
(direct) ← (direct) ∧ (A)

ANL direct,#data

Bytes: 3

Cycles: 2

Encoding:

0 1 0 1	0 0 1 1	direct address	immediate data

Operation: ANL
(direct) ← (direct) ∧ #data

ANL C,<src-bit>

Function: Logical-AND for bit variables

Description: If the Boolean value of the source bit is a logical 0 then clear the carry flag; otherwise leave the carry flag in its current state. A slash ("/") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, *but the source bit itself is not affected.* No other flags are affected.

Only direct addressing is allowed for the source operand.

Example: Set the carry flag if, and only if, P1.0 = 1, ACC. 7 = 1, and OV = 0:

```
MOV  C,P1.0     ;LOAD CARRY WITH INPUT PIN STATE
ANL  C,ACC.7    ;AND CARRY WITH ACCUM. BIT 7
ANL  C,/OV      ;AND WITH INVERSE OF OVERFLOW FLAG
```

ANL C,bit

Bytes: 2

Cycles: 2

Encoding:

1 0 0 0	0 0 1 0	bit address

Operation: ANL
(C) ← (C) ∧ (bit)

ANL C,/bit

Bytes: 2

Cycles: 2

Encoding:

1 0 1 1	0 0 0 0	bit address

Operation: ANL
(C) ← (C) ∧ ¬ (bit)

CJNE <dest-byte>,<src-byte>, rel

Function: Compare and Jump if Not Equal.

Description: CJNE compares the magnitudes of the first two operands, and branches if their values are not equal. The branch destination is computed by adding the signed relative-displacement in the last instruction byte to the PC, after incrementing the PC to the start of the next instruction. The carry flag is set if the unsigned integer value of <dest-byte> is less than the unsigned integer value of <src-byte>; otherwise, the carry is cleared. Neither operand is affected.

The first two operands allow four addressing mode combinations: the Accumulator may be compared with any directly addressed byte or immediate data, and any indirect RAM location or working register can be compared with an immediate constant.

Example: The Accumulator contains 34H. Register 7 contains 56H. The first instruction in the sequence,

```
                CJNE    R7,#60H, NOT_EQ
;               ...     .....           ; R7 = 60H.
NOT_EQ:         JC      REQ_LOW         ; IF R7 < 60H.
;               ...     .....           ; R7 > 60H.
```

sets the carry flag and branches to the instruction at label NOT_EQ. By testing the carry flag, this instruction determines whether R7 is greater or less than 60H.

If the data being presented to Port 1 is also 34H, then the instruction,

```
WAIT:  CJNE  A,P1,WAIT
```

clears the carry flag and continues with the next instruction in sequence, since the Accumulator does equal the data read from P1. (If some other value was being input on P1, the program will loop at this point until the P1 data changes to 34H.)

CJNE A,direct,rel

Bytes: 3

Cycles: 2

Encoding:

1 0 1 1	0 1 0 1	direct address	rel. address

Operation:

```
(PC) ← (PC) + 3
IF (A) <> (direct)
THEN
        (PC) ← (PC) + relative offset

IF (A) < (direct)
THEN
        (C) ← 1
ELSE
        (C) ← 0
```

CJNE A,#data,rel

Bytes: 3

Cycles: 2

Encoding:

1 0 1 1	0 1 0 0	immediate data	rel. address

Operation:

```
(PC) ← (PC) + 3
IF (A) <> data
THEN
        (PC) ← (PC) + relative offset

IF (A) < data
THEN
        (C) ← 1
ELSE
        (C) ← 0
```

CJNE Rn,#data,rel

Bytes: 3

Cycles: 2

Encoding:

1 0 1 1	1 r r r	immediate data	rel. address

Operation:

```
(PC) ← (PC) + 3
IF (Rn) <> data
THEN
        (PC) ← (PC) + relative offset

IF (Rn) < data
THEN
        (C) ← 1
ELSE
        (C) ← 0
```

CJNE @Ri,#data,rel

Bytes: 3

Cycles: 2

Encoding:

1 0 1 1	0 1 1 i	immediate data	rel. address

Operation:

```
(PC) ← (PC) + 3
IF ((Ri)) <> data
THEN
        (PC) ← (PC) + relative offset

IF ((Ri)) < data
THEN
        (C) ← 1
ELSE
        (C) ← 0
```

CLR A

Function: Clear Accumulator

Description: The Accumulator is cleared (all bits set on zero). No flags are affected.

Example: The Accumulator contains 5CH (01011100B). The instruction,

```
CLR  A
```

will leave the Accumulator set to 00H (00000000B).

Bytes: 1

Cycles: 1

Encoding:

1 1 1 0	0 1 0 0

Operation:
```
CLR
(A) ← 0
```

CLR bit

Function: Clear bit

Description: The indicated bit is cleared (reset to zero). No other flags are affected. CLR can operate on the carry flag or any directly addressable bit.

Example: Port 1 has previously been written with 5DH (01011101B). The instruction,

```
CLR  P1.2
```

will leave the port set to 59H (01011001B).

CLR C

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	0 0 1 1

Operation:
```
CLR
(C) ← 0
```

CLR bit

Bytes: 2

Cycles: 1

Encoding:

1 1 0 0	0 0 1 0	bit address

Operation:
```
CLR
(bit) ← 0
```

CPL A

Function: Complement Accumulator

Description: Each bit of the Accumulator is logically complemented (one's complement). Bits which previously contained a one are changed to a zero and vice-versa. No flags are affected.

Example: The Accumulator contains 5CH (01011100B). The instruction,

```
CPL   A
```

will leave the Accumulator set to 0A3H (10100011B).

Bytes: 1

Cycles: 1

Encoding:

1 1 1 1	0 1 0 0

Operation:

```
CPL
(A) ← ¬(A)
```

CPL bit

Function: Complement bit

Description: The bit variable specified is complemented. A bit which had been a one is changed to zero and vice-versa. No other flags are affected. CLR can operate on the carry or any directly addressable bit.

Note: When this instruction is used to modify an output pin, the value used as the original data will be read from the output data latch, *not* the input pin.

Example: Port 1 has previously been written with 5BH (01011101B). The instruction sequence,

```
CPL   P1.1

CPL   P1.2
```

will leave the port set to 5BH (01011011B).

CPL C

Bytes: 1

Cycles: 1

Encoding:

1 0 1 1	0 0 1 1

Operation:

```
CPL
(C) ← ¬(C)
```

CPL bit

Bytes: 2

Cycles: 1

Encoding:

1 0 1 1	0 0 1 0	bit address

Operation: CPL
(bit) ← ¬ (bit)

DA A

Function: Decimal-adjust Accumulator for Addition

Description: DA A adjusts the eight-bit value in the Accumulator resulting from the earlier addition of two variables (each in packed-BCD format), producing two four-bit digits. Any ADD or ADDC instruction may have been used to perform the addition.

If Accumulator bits 3-0 are greater than nine (xxxx1010-xxxx1111), or if the AC flag is one, six is added to the Accumulator producing the proper BCD digit in the low-order nibble. This internal addition would set the carry flag if a carry-out of the low-order four-bit field propagated through all high-order bits, but it would not clear the carry flag otherwise.

If the carry flag is now set, or if the four high-order bits now exceed nine (1010xxxx-111xxxx), these high-order bits are incremented by six, producing the proper BCD digit in the high-order nibble. Again, this would set the carry flag if there was a carry-out of the high-order bits, but wouldn't clear the carry. The carry flag thus indicates if the sum of the original two BCD variables is greater than 100, allowing multiple precision decimal addition. OV is not affected.

All of this occurs during the one instruction cycle. Essentially, this instruction performs the decimal conversion by adding 00H, 06H, 60H, or 66H to the Accumulator, depending on initial Accumulator and PSW conditions.

Note: DA A *cannot* simply convert a hexadecimal number in the Accumulator to BCD notation, nor does DA A apply to decimal subtraction.

Example: The Accumulator holds the value 56H (01010110B) representing the packed BCD digits of the decimal number 56. Register 3 contains the value 67H (01100111B) representing the packed BCD digits of the decimal number 67. The carry flag is set. The instruction sequence.

```
ADDC  A,R3
DA    A
```

will first perform a standard twos-complement binary addition, resulting in the value 0BEH (10111110) in the Accumulator. The carry and auxiliary carry flags will be cleared.

The Decimal Adjust instruction will then alter the Accumulator to the value 24H (00100100B), indicating the packed BCD digits of the decimal number 24, the low-order two digits of the decimal sum of 56, 67, and the carry-in. The carry flag will be set by the Decimal Adjust instruction, indicating that a decimal overflow occurred. The true sum 56, 67, and 1 is 124.

BCD variables can be incremented or decremented by adding 01H or 99H. If the Accumulator initially holds 30H (representing the digits of 30 decimal), then the instruction sequence,

```
ADD   A,#99H

DA    A
```

will leave the carry set and 29H in the Accumulator, since 30 + 99 = 129. The low-order byte of the sum can be interpreted to mean 30 − 1 = 29.

Bytes: 1

Cycles: 1

Encoding:

1 1 0 1	0 1 0 0

Operation:

```
DA
-contents of Accumulator are BCD
IF    [[(A3-0) > 9] ∨ [(AC) = 1]]
      THEN(A3-0) ← (A3-0) + 6
           AND

IF    [[(A7-4) > 9] ∨ [(C) = 1]]
      THEN (A7-4) ← (A7-4) + 6
```

DEC byte

Function: Decrement

Description: The variable indicated is decremented by 1. An original value of 00H will underflow to 0FFH. No flags are affected. Four operand addressing modes are allowed: accumulator, register, direct, or register-indirect.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: Register 0 contains 7FH (01111111B). Internal RAM locations 7EH and 7FH contain 00H and 40H, respectively. The instruction sequence,

```
DEC  @R0
DEC  R0
DEC  @R0
```

will leave register 0 set to 7EH and internal RAM locations 7EH and 7FH set to 0FFH and 3FH.

DEC A

Bytes: 1

Cycles: 1

Encoding:

0 0 0 1	0 1 0 0

Operation: DEC
(A) ← (A) − 1

DEC Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 0 1	1 r r r

Operation: DEC
(Rn) ← (Rn) − 1

DEC direct

Bytes: 2

Cycles: 1

Encoding:

0 0 0 1	0 1 0 1	direct address

Operation: DEC
(direct) ← (direct) − 1

DEC @Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 0 1	0 1 1 i

Operation: DEC
((Ri)) ← ((Ri)) − 1

DIV AB

Function: Divide

Description: DIV AB divides the unsigned eight-bit integer in the Accumulator by the unsigned eight-bit integer in register B. The Accumulator receives the integer part of the quotient; register B receives the integer remainder. The carry and OV flags will be cleared.

Exception: if B had originally contained 00H, the values returned in the Accumulator and B-register will be undefined and the overflow flag will be set. The carry flag is cleared in any case.

Example: The Accumulator contains 251 (0FBH or 11111011B) and B contains 18 (12H or 00010010B). The instruction,

DIV AB

will leave 13 in the Accumulator (0DH or 00001101B) and the value 17 (11H or 00010001B) in B, since 251 = (13 X 18) + 17. Carry and OV will both be cleared.

Bytes: 1

Cycles: 4

Encoding:

1 0 0 0	0 1 0 0

Operation: DIV
$(A)_{15\text{-}8}$ ← (A)/(B)
$(B)_{7\text{-}0}$

DJNZ <byte>,<rel-addr>

Function: Decrement and Jump if Not Zero

Description: DJNZ decrements the location indicated by 1, and branches to the address indicated by the second operand if the resulting value is not zero. An original value of 00H will underflow to 0FFH. No flags are affected. The branch destination would be computed by adding the signed relative-displacement value in the last instruction byte to the PC, after incrementing the PC to the first byte of the following instruction.

The location decremented may be a register or directly addressed byte.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: Internal RAM locations 40H, 50H, and 60H contain the values 01H, 70H, and 15H, respectively. The instruction sequence,

```
DJNZ  40H,LABEL_1
DJNZ  50H,LABEL_2
DJNZ  60H,LABEL_3
```

will cause a jump to the instruction at label LABEL_2 with the values 00H, 6FH, and 15H in the three RAM locations. The first jump was *not* taken because the result was zero.

This instruction provides a simple way of executing a program loop a given number of times, or for adding a moderate time delay (from 2 to 512 machine cycles) with a single instruction. The instruction sequence,

```
        MOV     R2,#8
TOGGLE: CPL     P1.7
        DJNZ    R2,TOGGLE
```

will toggle P1.7 eight times, causing four output pulses to appear at bit 7 of output Port 1. Each pulse will last three machine cycles; two for DJNZ and one to alter the pin.

DJNZ Rn,rel

Bytes: 2

Cycles: 2

Encoding:

1 1 0 1	1 r r r	rel. address

Operation:

```
DJNZ
(PC) ← (PC) + 2
(Rn) ← (Rn) − 1
IF  (Rn) > 0 or (Rn) < 0
    THEN
        (PC) ← (PC) + rel
```

DJNZ direct,rel

Bytes: 3

Cycles: 2

Encoding:

1 1 0 1	0 1 0 1	direct address	rel. address

Operation:

```
DJNZ
(PC) ← (PC) + 2
(direct) ← (direct) − 1
IF (direct) > 0 or (direct) < 0
   THEN
        (PC) ← (PC) + rel
```

INC <byte>

Function: Increment

Description: INC increments the indicated variable by 1. An original value of 0FFH will overflow to 00H. No flags are affected. Three addressing modes are allowed: register, direct, or register-indirect.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: Register 0 contains 7EH (01111110B). Internal RAM locations 7EH and 7FH contain 0FFH and 40H, respectively. The instruction sequence,

```
INC  @R0
INC  R0
INC  @R0
```

will leave register 0 set to 7FH and internal RAM locations 7EH and 7FH holding (respectively) 00H and 41H.

INC A

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	0 1 0 0

Operation:

```
INC
(A) ← (A) + 1
```

INC Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	1 r r r

Operation: INC
(Rn) ← (Rn) + 1

INC direct

Bytes: 2

Cycles: 1

Encoding:

0 0 0 0	0 1 0 1	direct address

Operation: INC
(direct) ← (direct) + 1

INC @Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	0 1 1 i

Operation: INC
((Ri)) ← ((Ri)) + 1

INC DPTR

Function: Increment Data Pointer

Description: Increment the 16-bit data pointer by 1. A 16-bit increment (modulo 2^{16}) is performed; an overflow of the low-order byte of the data pointer (DPL) from 0FFH to 00H will increment the high-order byte (DPH). No flags are affected.

This is the only 16-bit register which can be incremented.

Example: Registers DPH and DPL contain 12H and 0FEH, respectively. The instruction sequence,

```
INC  DPTR
INC  DPTR
INC  DPTR
```

will change DPH and DPL to 13H and 01H.

Bytes: 1

Cycles: 2

Encoding:

1 0 1 0	0 0 1 1

Operation: INC
(DPTR) ← (DPTR) + 1

JB bit,rel

Function: Jump if Bit set

Description: If the indicated bit is a one, jump to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. *The bit tested is not modified.* No flags are affected.

Example: The data present at input port 1 is 11001010B. The Accumulator holds 56 (01010110B). The instruction sequence,

```
JB   P1.2,LABEL1

JB   ACC.2,LABEL2
```

will cause program execution to branch to the instruction at label LABEL2.

Bytes: 3

Cycles: 2

Encoding:

0 0 1 0	0 0 0 0	bit address	rel. address

Operation:

```
JB
(PC) ← (PC) + 3
IF  (bit) = 1
    THEN
            (PC) ← (PC) + rel
```

JBC bit,rel

Function: Jump if Bit is set and Clear bit

Description: If the indicated bit is one, branch to the address indicated; otherwise proceed with the next instruction. *The bit will not be cleared if it is already a zero.* The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. No flags are affected.

Note: When this instruction is used to test an output pin, the value used as the original data will be read from the output data latch, *not* the input pin.

Example: The Accumulator holds 56H (01010110B). The instruction sequence,

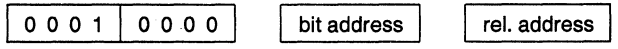
```
JBC  ACC.3,LABEL1
JBC  ACC.2,LABEL2
```

will cause program execution to continue at the instruction identified by the label LABEL2, with the Accumulator modified to 52H (01010010B).

Bytes: 3

Cycles: 2

Encoding:



Operation:

```
JBC
(PC) ← (PC) + 3
IF  (bit) = 1
    THEN
            (bit) ← 0
            (PC) ← (PC) + rel
```

JC rel

Function: Jump if Carry is set

Description: If the carry flag is set, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. No flags are affected.

Example: The carry flag is cleared. The instruction sequence,

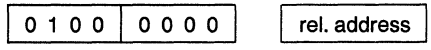
```
JC    LABEL1
CPL   C
JC    LABEL 2
```

will set the carry and cause program execution to continue at the instruction identified by the label LABEL2.

Bytes: 2

Cycles: 2

Encoding:



Operation:

```
JC
(PC) ← (PC) + 2
IF  (C) = 1
    THEN
            (PC) ← (PC) + rel
```

JMP @A+DPTR

Function: Jump indirect

Description: Add the eight-bit unsigned contents of the Accumulator with the sixteen-bit data pointer, and load the resulting sum to the program counter. This will be the address for subsequent instruction fetches. Sixteen-bit addition is performed (modulo 2^{16}): a carry-out from the low-order eight bits propagates through the higher-order bits. Neither the Accumulator nor the Data Pointer is altered. No flags are affected.

Example: An even number from 0 to 6 is in the Accumulator. The following sequence of instructions will branch to one of four AJMP instructions in a jump table starting at JMP_TBL:

```
        MOV     DPTR,#JMP_TBL
        JMP     @A+DPTR
JMP_TBL: AJMP   LABEL0
        AJMP    LABEL1
        AJMP    LABEL2
        AJMP    LABEL3
```

If the Accumulator equals 04H when starting this sequence, execution will jump to label LABEL2. Remember that AJMP is a two-byte instruction, so the jump instructions start at every other address.

Bytes: 1

Cycles: 2

Encoding:

0 1 1 1	0 0 1 1

Operation: JMP
(PC) ← (A) + (DPTR)

6

JNB bit,rel

Function: Jump if Bit Not set

Description: If the indicated bit is a zero, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. *The bit tested is not modified.* No flags are affected.

Example: The data present at input port 1 is 11001010B. The Accumulator holds 56H (01010110B). The instruction sequence,

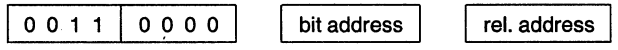
```
JNB  P1.3,LABEL1
JNB  ACC.3,LABEL2
```

will cause program execution to continue at the instruction at label LABEL2.

Bytes: 3

Cycles: 2

Encoding:



Operation:

```
JNB
(PC) ← (PC) + 3
IF  (bit) = 0
    THEN (PC) ← (PC) + rel.
```

JNC rel

Function: Jump if Carry not set

Description: If the carry flag is a zero, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice to point to the next instruction. The carry flag is not modified.

Example: The carry flag is set. The instruction sequence,

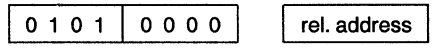
```
JNC  LABEL1
CPL  C
JNC  LABEL2
```

will clear the carry and cause program execution to continue at the instruction identified by the label LABEL2.

Bytes: 2

Cycles: 2

Encoding:



Operation:

```
JNC
(PC) ← (PC) + 2
IF  (C) = 0
    THEN  (PC) ← (PC) + rel
```

JNZ rel

Function: Jump if Accumulator Not Zero

Description: If any bit of the Accumulator is a one, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

Example: The Accumulator originally holds 00H. The instruction sequence,

```
JNZ  LABEL1
INC  A
JNZ  LABEL2
```

will set the Accumulator to 01H and continue at label LABEL2.

Bytes: 2

Cycles: 2

Encoding:

0 1 1 1	0 0 0 0	rel. address

Operation:

```
JNZ
(PC) ← (PC) + 2
IF   (A) ≠ 0
     THEN  (PC) ← (PC) + rel
```

JZ rel

Function: Jump if Accumulator Zero

Description: If all bits of the Accumulator are zero, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

Example: The Accumulator originally contains 01H. The instruction sequence,

```
JZ   LABEL1
DEC  A
JZ   LABEL2
```

will change the Accumulator to 00H and cause program execution to continue at the instruction identified by the label LABEL2.

Bytes: 2

Cycles: 2

Encoding:

0 1 1 0	0 0 0 0	rel. address

Operation:

```
JZ
(PC) ← (PC) + 2
IF   (A) = 0
     THEN  (PC) ← (PC) + rel
```

LCALL addr16

Function: Long call

Description: LCALL calls a subroutine located at the indicated address. The instruction adds three to the program counter to generate the address of the next instruction and then pushes the 16-bit result onto the stack (low byte first), incrementing the Stack Pointer by two. The high-order and low-order bytes of the PC are then loaded, respectively, with the second and third bytes of the LCALL instruction. Program execution continues with the instruction at this address. The subroutine may therefore begin anywhere in the full 64K-byte program memory address space. No flags are affected.

Example: Initially the Stack Pointer equals 07H. The label "SUBRTN" is assigned to program memory location 1234H. After executing the instruction,

```
LCALL   SUBRTN
```

at location 0123H, the Stack Pointer will contain 09H, internal RAM locations 08H and 09H will contain 26H and 01H, and the PC will contain 1234H.

Bytes: 3

Cycles: 2

Encoding:

0 0 0 1	0 0 1 0	addr15-addr8	addr7-addr0

Operation:

LCALL
(PC) ← (PC) + 3
(SP) ← (SP) + 1
((SP)) ← (PC_{7-0})
(SP) ← (SP) + 1
((SP)) ← (PC_{15-8})
(PC) ← $addr_{15-0}$

LJMP addr16

Function: Long Jump

Description: LJMP causes an unconditional branch to the indicated address, by loading the high-order and low-order bytes of the PC (respectively) with the second and third instruction bytes. The destination may therefore be anywhere in the full 64K program memory address space. No flags are affected.

Example: The label "JMPADR" is assigned to the instruction at program memory location 1234H. The instruction,

```
LJMP   JMPADR
```

at location 0123H will load the program counter with 1234H.

Bytes: 3

Cycles: 2

Encoding:

0 0 0 0	0 0 1 0	addr15-addr8	addr7-addr0

Operation:

LJMP
(PC) ← $addr_{15-0}$

MOV <dest-byte>,<src-byte>

Function: Move byte variable

Description: The byte variable indicated by the second operand is copied into the location specified by the first operand. The source byte is not affected. No other register or flag is affected.

This is by far the most flexible operation. Fifteen combinations of source and destination addressing modes are allowed.

Example: Internal RAM location 30H holds 40H. The value of RAM location 40H is 10H. The data present at input port 1 is 11001010B (0CAH).

```
MOV   R0,#30H   ;R0 <= 30H
MOV   A,@R0     ;A <= 40H
MOV   R1,A      ;R1 <= 40H
MOV   B,@R1     ;B <= 10H
MOV   @R1,P1    ;RAM (40H) <= 0CAH
MOV   P2,P1     ;P2 #0CAH
```

leaves the value 30H in register 0, 40H in both the Accumulator and register 1, 10H in register B, and 0CAH (11001010B) both in RAM location 40H and output on port 2.

MOV A,Rn

Bytes: 1

Cycles: 1

Encoding:

1 1 1 0	1 r r r

Operation: MOV
(A) ← (Rn)

*MOV A,direct

Bytes: 2

Cycles: 1

Encoding:

1 1 1 0	0 1 0 1	direct address

Operation: MOV
(A) ← (direct)

MOV A,ACC is not a valid instruction.

MOV A,@Ri

Bytes: 1

Cycles: 1

Encoding:

1 1 1 0	0 1 1 i

Operation: MOV
(A) ← ((Ri))

MOV A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 1	0 1 0 0	immediate data

Operation: MOV
(A) ← #data

MOV Rn,A

Bytes: 1

Cycles: 1

Encoding:

1 1 1 1	1 r r r

Operation: MOV
(Rn) ← (A)

MOV Rn,direct

Bytes: 2

Cycles: 2

Encoding:

1 0 1 0	1 r r r	direct addr.

Operation: MOV
(Rn) ← (direct)

MOV Rn,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 1	1 r r r	immediate data

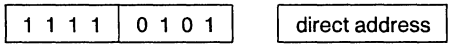
Operation: MOV
(Rn) ← #data

MOV direct,A

Bytes: 2

Cycles: 1

Encoding:



Operation: MOV
(direct) ← (A)

MOV direct,Rn

Bytes: 2

Cycles: 2

Encoding:

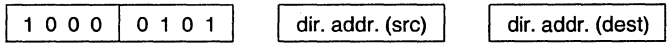
Operation: MOV
(direct) ← (Rn)

MOV direct,direct

Bytes: 3

Cycles: 2

Encoding:



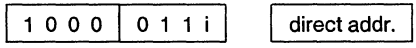
Operation: MOV
(direct) ← (direct)

MOV direct,@Ri

Bytes: 2

Cycles: 2

Encoding:



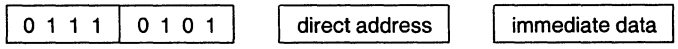
Operation: MOV
(direct) ← ((Ri))

MOV direct,#data

Bytes: 3

Cycles: 2

Encoding:



Operation: MOV
(direct) ← #data

MOV @RI,A

Bytes: 1

Cycles: 1

Encoding:

1 1 1 1	0 1 1 i

Operation: MOV
((Ri)) ← (A)

MOV @Ri,direct

Bytes: 2

Cycles: 2

Encoding:

1 0 1 0	0 1 1 i	direct addr.

Operation: MOV
((Ri)) ← (direct)

MOV @Ri,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 1	0 1 1 i	immediate data

Operation: MOV
((RI)) ← #data

MOV <dest-bit>,<src-bit>

Function: Move bit data

Description: The Boolean variable indicated by the second operand is copied into the location specified by the first operand. One of the operands must be the carry flag; the other may be any directly addressable bit. No other register or flag is affected.

Example: The carry flag is originally set. The data present at input Port 3 is 11000101B. The data previously written to output Port 1 is 35H (00110101B).

```
MOV  P1.3,C
MOV  C,P3.3
MOV  P1.2,C
```

will leave the carry cleared and change Port 1 to 39H (00111001B).

MOV C,bit

Bytes: 2

Cycles: 1

Encoding:

1 0 1 0	0 0 1 0	bit address

Operation: MOV
(C) ← (bit)

MOV bit,C

Bytes: 2

Cycles: 2

Encoding:

1 0 0 1	0 0 1 0	bit address

Operation: MOV
(bit) ← (C)

MOV DPTR,#data16

Function: Load Data Pointer with a 16-bit constant

Description: The Data Pointer is loaded with the 16-bit constant indicated. The 16-bit constant is loaded into the second and third bytes of the instruction. The second byte (DPH) is the high-order byte, while the third byte (DPL) holds the low-order byte. No flags are affected.

This is the only instruction which moves 16 bits of data at once.

Example: The instruction,

MOV DPTR,#1234H

will load the value 1234H into the Data Pointer: DPH will hold 12H and DPL will hold 34H.

Bytes: 3

Cycles: 2

Encoding:

1 0 0 1	0 0 0 0	immed. data15-8	immed. data7-0

Operation: MOV
(DPTR) ← #data$_{15\text{-}0}$
DPH □ DPL ← #data$_{15\text{-}8}$ □ #data$_{7\text{-}0}$

MOVC A,@A+<base-reg>

Function: Move Code byte

Description: The MOVC instructions load the Accumulator with a code byte, or constant from program memory. The address of the byte fetched is the sum of the original unsigned eight-bit Accumulator contents and the contents of a sixteen-bit base register, which may be either the Data Pointer or the PC. In the latter case, the PC is incremented to the address of the following instruction before being added with the Accumulator; otherwise the base register is not altered. Sixteen-bit addition is performed so a carry-out from the low-order eight bits may propagate through higher-order bits. No flags are affected.

Example: A value between 0 and 3 is in the Accumulator. The following instructions will translate the value in the Accumulator to one of four values defined by the DB (define byte) directive.

```
REL_PC: INC   A
        MOVC  A,@A+PC
        RET
        DB    66H
        DB    77H
        DB    88H
        DB    99H
```

If the subroutine is called with the Accumulator equal to 01H, it will return with 77H in the Accumulator. The INC A before the MOVC instruction is needed to "get around" the RET instruction above the table. If several bytes of code separated the MOVC from the table, the corresponding number would be added to the Accumulator instead.

MOVC A,@A+DPTR

Bytes: 1

Cycles: 2

Encoding:

1 0 0 1	0 0 1 1

Operation: MOVC
(A) ← ((A) + (DPTR))

MOVC A,@A + PC

Bytes: 1

Cycles: 2

Encoding:

1 0 0 0	0 0 1 1

Operation: MOVC
(PC) ← (PC) + 1
(A) ← ((A) + (PC))

MOVX <dest-byte>,<src-byte>

Function: Move External

Description: The MOVX instructions transfer data between the Accumulator and a byte of external data memory, hence the "X" appended to MOV. There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type, the contents of R0 or R1 in the current register bank provide an eight-bit address multiplexed with data on P0. Eight bits are sufficient for external I/O expansion decoding or for a relatively small RAM array. For somewhat larger arrays, any output port pins can be used to output higher-order address bits. These pins would be controlled by an output instruction preceding the MOVX.

In the second type of MOVX instruction, the Data Pointer generates a sixteen-bit address. P2 outputs the high-order eight address bits (the contents of DPH) while P0 multiplexes the low-order eight bits (DPL) with data. The P2 Special Function Register retains its previous contents while the P2 output buffers are emitting the contents of DPH. This form is faster and more efficient when accessing very large data arrays (up to 64K bytes), since no additional instructions are needed to set up the output ports.

It is possible in some situations to mix the two MOVX types. A large RAM array with its high-order address lines driven by P2 can be addressed via the Data Pointer, or with code to output high-order address bits to P2 followed by a MOVX instruction using R0 or R1.

Example: An external 256 byte RAM using multiplexed address/data lines (e.g., an Intel 8155 RAM/I/O/Timer) is connected to the 8051 Port 0. Port 3 provides control lines for the external RAM. Ports 1 and 2 are used for normal I/O. Registers 0 and 1 contain 12H and 34H. Location 34H of the external RAM holds the value 56H. The instruction sequence,

```
MOVX  A,@R1

MOVX  @R0,A
```

copies the value 56H into both the Accumulator and external RAM location 12H.

MOVX A,@Ri

Bytes: 1

Cycles: 2

Encoding:

1 1 1 0	0 0 1 i

Operation: MOVX
(A) ← ((Ri))

MOVX A,@DPTR

Bytes: 1

Cycles: 2

Encoding:

1 1 1 0	0 0 0 0

Operation: MOVX
(A) ← ((DPTR))

MOVX @Ri,A

Bytes: 1

Cycles: 2

Encoding:

1 1 1 1	0 0 1 i

Operation: MOVX
((Ri)) ← (A)

MOVX @DPTR,A

Bytes: 1

Cycles: 2

Encoding:

1 1 1 1	0 0 0 0

Operation: MOVX
(DPTR) ← (A)

MUL AB

Function: Multiply

Description: MUL AB multiplies the unsigned eight-bit integers in the Accumulator and register B. The low-order byte of the sixteen-bit product is left in the Accumulator, and the high-order byte in B. If the product is greater than 255 (0FFH) the overflow flag is set; otherwise it is cleared. The carry flag is always cleared.

Example: Originally the Accumulator holds the value 80 (50H). Register B holds the value 160 (0A0H). The instruction,

```
MUL   AB
```

will give the product 12,800 (3200H), so B is changed to 32H (00110010B) and the Accumulator is cleared. The overflow flag is set, carry is cleared.

Bytes: 1

Cycles: 4

Encoding:

1 0 1 0	0 1 0 0

Operation:
MUL
$(A)_{7\text{-}0} \leftarrow (A) \times (B)$
$(B)_{15\text{-}8}$

NOP

Function: No Operation

Description: Execution continues at the following instruction. Other than the PC, no registers or flags are affected.

Example: It is desired to produce a low-going output pulse on bit 7 of Port 2 lasting exactly 5 cycles. A simple SETB/CLR sequence would generate a one-cycle pulse, so four additional cycles must be inserted. This may be done (assuming no interrupts are enabled) with the instruction sequence,

```
CLR     P2.7
NOP
NOP
NOP
NOP
SETB    P2.7
```

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	0 0 0 0

Operation:
NOP
$(PC) \leftarrow (PC) + 1$

ORL <dest-byte> <src-byte>

Function: Logical-OR for byte variables

Description: ORL performs the bitwise logical-OR operation between the indicated variables, storing the results in the destination byte. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: If the Accumulator holds 0C3H (11000011B) and R0 holds 55H (01010101B) then the instruction,

```
ORL  A,R0
```

will leave the Accumulator holding the value 0D7H (11010111B).

When the destination is a directly addressed byte, the instruction can set combinations of bits in any RAM location or hardware register. The pattern of bits to be set is determined by a mask byte, which may be either a constant data value in the instruction or a variable computed in the Accumulator at run-time. The instruction,

```
ORL  P1,#00110010B
```

will set bits 5, 4, and 1 of output Port 1.

ORL A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 1 0 0	1 r r r

Operation: ORL
(A) ← (A) ∨ (Rn)

ORL A,direct

Bytes: 2

Cycles: 1

Encoding:

0 1 0 0	0 1 0 1	direct address

Operation: ORL
(A) ← (A) ∨ (direct)

ORL A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 1 0 0	0 1 1 i

Operation: ORL
(A) ← (A) ∨ ((Ri))

ORL A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 0 0	0 1 0 0	immediate data

Operation: ORL
(A) ← (A) ∨ #data

ORL direct,A

Bytes: 2

Cycles: 1

Encoding:

0 1 0 0	0 0 1 0	direct address

Operation: ORL
(direct) ← (direct) ∨ (A)

ORL direct,#data

Bytes: 3

Cycles: 2

Encoding:

0 1 0 0	0 0 1 1	direct addr.	immediate data

Operation: ORL
(direct) ← (direct) ∨ #data

ORL C,<src-bit>

Function: Logical-OR for bit variables

Description: Set the carry flag if the Boolean value is a logical 1; leave the carry in its current state otherwise . A slash ("/") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, but the source bit itself is not affected. No other flags are affected.

Example: Set the carry flag if and only if P1.0 = 1, ACC. 7 = 1, or OV = 0:

```
MOV  C,P1.0     ;LOAD CARRY WITH INPUT PIN P10
ORL  C,ACC.7    ;OR CARRY WITH THE ACC. BIT 7
ORL  C,/OV      ;OR CARRY WITH THE INVERSE OF OV.
```

ORL C,bit

Bytes: 2

Cycles: 2

Encoding:

0 1 1 1	0 0 1 0	bit address

Operation: ORL
(C) ← (C) ∨ (bit)

ORL C,/bit

Bytes: 2

Cycles: 2

Encoding:

1 0 1 0	0 0 0 0	bit address

Operation: ORL
(C) ← (C) ∨ ($\overline{\text{bit}}$)

POP direct

Function: Pop from stack.

Description: The contents of the internal RAM location addressed by the Stack Pointer is read, and the Stack Pointer is decremented by one. The value read is then transferred to the directly addressed byte indicated. No flags are affected.

Example: The Stack Pointer originally contains the value 32H, and internal RAM locations 30H through 32H contain the values 20H, 23H, and 01H, respectively. The instruction sequence,

```
POP   DPH
POP   DPL
```

will leave the Stack Pointer equal to the value 30H and the Data Pointer set to 0123H. At this point the instruction,

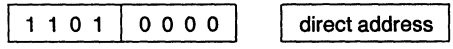
```
POP   SP
```

will leave the Stack Pointer set to 20H. Note that in this special case the Stack Pointer was decremented to 2FH before being loaded with the value popped (20H).

Bytes: 2

Cycles: 2

Encoding:



Operation:
POP
(direct) ← ((SP))
(SP) ← (SP) − 1

PUSH direct

Function: Push onto stack

Description: The Stack Pointer is incremented by one. The contents of the indicated variable is then copied into the internal RAM location addressed by the Stack Pointer. Otherwise no flags are affected.

Example: On entering an interrupt routine the Stack Pointer contains 09H. The Data Pointer holds the value 0123H. The instruction sequence,

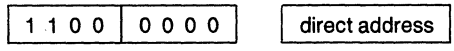
```
PUSH   DPL
PUSH   DPH
```

will leave the Stack Pointer set to 0BH and store 23H and 01H in internal RAM locations 0AH and 0BH, respectively.

Bytes: 2

Cycles: 2

Encoding:



Operation:
PUSH
(SP) ← (SP) + 1
((SP)) ← (direct)

RET

Function: Return from subroutine

Description: RET pops the high- and low-order bytes of the PC successively from the stack, decrementing the Stack Pointer by two. Program execution continues at the resulting address, generally the instruction immediately following an ACALL or LCALL. No flags are affected.

Example: The Stack Pointer originally contains the value 0BH. Internal RAM locations 0AH and 0BH contain the values 23H and 01H, respectively. The instruction,

RET

will leave the Stack Pointer equal to the value 09H. Program execution will continue at location 0123H.

Bytes: 1

Cycles: 2

Encoding:

0 0 1 0	0 0 1 0

Operation: RET
$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

RETI

Function: Return from interrupt

Description: RETI pops the high- and low-order bytes of the PC successively from the stack, and restores the interrupt logic to accept additional interrupts at the same priority level as the one just processed. The Stack Pointer is left decremented by two. No other registers are affected; the PSW is *not* automatically restored to its pre-interrupt status. Program execution continues at the resulting address, which is generally the instruction immediately after the point at which the interrupt request was detected. If a lower- or same-level interrupt had been pending when the RETI instruction is executed, that one instruction will be executed before the pending interrupt is processed.

Example: The Stack Pointer originally contains the value 0BH. An interrupt was detected during the instruction ending at location 0122H. Internal RAM locations 0AH and 0BH contain the values 23H and 01H, respectively. The instruction,

RETI

will leave the Stack Pointer equal to 09H and return program execution to location 0123H.

Bytes: 1

Cycles: 2

Encoding:

0 0 1 1	0 0 1 0

Operation: RETI
$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

RL A

Function: Rotate Accumulator Left

Description: The eight bits in the Accumulator are rotated one bit to the left. Bit 7 is rotated into the bit 0 position. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction,

```
RL   A
```

leaves the Accumulator holding the value 8BH (10001011B) with the carry unaffected.

Bytes: 1

Cycles: 1

Encoding:

0 0 1 0	0 0 1 1

Operation:
RL
$(A_n + 1) \leftarrow (An) \quad n = 0 - 6$
$(A0) \leftarrow (A7)$

RLC A

Function: Rotate Accumulator Left through the Carry flag

Description: The eight bits in the Accumulator and the carry flag are together rotated one bit to the left. Bit 7 moves into the carry flag; the original state of the carry flag moves into the bit 0 position. No other flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B), and the carry is zero. The instruction,

```
RLC   A
```

leaves the Accumulator holding the value 8BH (10001010B) with the carry set.

Bytes: 1

Cycles: 1

Encoding:

0 0 1 1	0 0 1 1

Operation:
RLC
$(An + 1) \leftarrow (An) \quad n = 0 - 6$
$(A0) \leftarrow (C)$
$(C) \leftarrow (A7)$

RR A

Function: Rotate Accumulator Right

Description: The eight bits in the Accumulator are rotated one bit to the right. Bit 0 is rotated into the bit 7 position. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction,

RR A

leaves the Accumulator holding the value 0E2H (11100010B) with the carry unaffected.

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	0 0 1 1

Operation: RR
$(An) \leftarrow (A_n + 1) \quad n = 0 - 6$
$(A7) \leftarrow (A0)$

RRC A

Function: Rotate Accumulator Right through Carry flag

Description: The eight bits in the Accumulator and the carry flag are together rotated one bit to the right. Bit 0 moves into the carry flag; the original value of the carry flag moves into the bit 7 position. No other flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B), the carry is zero. The instruction,

RRC A

leaves the Accumulator holding the value 62 (01100010B) with the carry set.

Bytes: 1

Cycles: 1

Encoding:

0 0 0 1	0 0 1 1

Operation: RRC
$(An) \leftarrow (An + 1) \quad n = 0 - 6$
$(A7) \leftarrow (C)$
$(C) \leftarrow (A0)$

SETB <bit>

Function: Set Bit

Description: SETB sets the indicated bit to one. SETB can operate on the carry flag or any directly addressable bit. No other flags are affected.

Example: The carry flag is cleared. Output Port 1 has been written with the value 34H (00110100B). The instructions,

SETB C

SETB P1.0

will leave the carry flag set to 1 and change the data output on Port 1 to 35H (00110101B).

SETB C

Bytes: 1

Cycles: 1

Encoding:

1 1 0 1	0 0 1 1

Operation: SETB
(C) ← 1

SETB bit

Bytes: 2

Cycles: 1

Encoding:

1 1 0 1	0 0 1 0	bit address

Operation: SETB
(bit) ← 1

SJMP rel

Function: Short Jump

Description: Program control branches unconditionally to the address indicated. The branch destination is computed by adding the signed displacement in the second instruction byte to the PC, after incrementing the PC twice. Therefore, the range of destinations allowed is from 128 bytes preceding this instruction to 127 bytes following it.

Example: The label "RELADR" is assigned to an instruction at program memory location 0123H. The instruction,

SJMP RELADR

will assemble into location 0100H. After the instruction is executed, the PC will contain the value 0123H.

(*Note:* Under the above conditions the instruction following SJMP will be at 102H. Therefore, the displacement byte of the instruction will be the relative offset (0123H-0102H) = 21H. Put another way, an SJMP with a displacement of 0FEH would be a one-instruction infinite loop.)

Bytes: 2

Cycles: 2

Encoding:

1 0 0 0	0 0 0 0	rel. address

Operation: SJMP
(PC) ← (PC) + 2
(PC) ← (PC) + rel

SUBB A,<src-byte>

Function: Subtract with borrow

Description: SUBB subtracts the indicated variable and the carry flag together from the Accumulator, leaving the result in the Accumulator. SUBB sets the carry (borrow) flag if a borrow is needed for bit 7, and clears C otherwise. (If C was set *before* executing a SUBB instruction, this indicates that a borrow was needed for the previous step in a multiple precision subtraction, so the carry is subtracted from the Accumulator along with the source operand.) AC is set if a borrow is needed for bit 3, and cleared otherwise. OV is set if a borrow is needed into bit 6, but not into bit 7, or into bit 7, but not bit 6.

When subtracting signed integers OV indicates a negative number produced when a negative value is subtracted from a positive value, or a positive result when a positive number is subtracted from a negative number.

The source operand allows four addressing modes: register, direct, register-indirect, or immediate.

Example: The Accumulator holds 0C9H (11001001B), register 2 holds 54H (01010100B), and the carry flag is set. The instruction,

SUBB A,R2

will leave the value 74H (01110100B) in the accumulator, with the carry flag and AC cleared but OV set.

Notice that 0C9H minus 54H is 75H. The difference between this and the above result is due to the carry (borrow) flag being set before the operation. If the state of the carry is not known before starting a single or multiple-precision subtraction, it should be explicitly cleared by a CLR C instruction.

SUBB A,Rn

Bytes: 1

Cycles: 1

Encoding:

1 0 0 1	1 r r r

Operation: SUBB

(A) ← (A) − (C) − (Rn)

SUBB A,direct

Bytes: 2

Cycles: 1

Encoding:

1 0 0 1	0 1 0 1	direct address

Operation: SUBB
(A) ← (A) − (C) − (direct)

SUBB A,@Ri

Bytes: 1

Cycles: 1

Encoding:

1 0 0 1	0 1 1 i

Operation: SUBB
(A) ← (A) − (C) − ((Ri))

SUBB A,#data

Bytes: 2

Cycles: 1

Encoding:

1 0 0 1	0 1 0 0	immediate data

Operation: SUBB
(A) ← (A) − (C) − #data

SWAP A

Function: Swap nibbles within the Accumulator

Description: SWAP A interchanges the low- and high-order nibbles (four-bit fields) of the Accumulator (bits 3-0 and bits 7-4). The operation can also be thought of as a four-bit rotate instruction. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction,

SWAP A

leaves the Accumulator holding the value 5CH (01011100B).

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	0 1 0 0

Operation: SWAP
$(A_{3-0}) \rightleftarrows (A_{7-4})$

XCH A,<byte>

Function: Exchange Accumulator with byte variable

Description: XCH loads the Accumulator with the contents of the indicated variable, at the same time writing the original Accumulator contents to the indicated variable. The source/destination operand can use register, direct, or register-indirect addressing.

Example: R0 contains the address 20H. The Accumulator holds the value 3FH (00111111B). Internal RAM location 20H holds the value 75H (01110101B). The instruction,

```
XCH   A,@R0
```

will leave RAM location 20H holding the values 3FH (00111111B) and 75H (01110101B) in the accumulator.

XCH A,Rn

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	1 r r r

Operation:
XCH
(A) $\rightleftarrows$ (Rn)

XCH A,direct

Bytes: 2

Cycles: 1

Encoding:

1 1 0 0	0 1 0 1	direct address

Operation:
XCH
(A) $\rightleftarrows$ (direct)

XCH A,@Ri

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	0 1 1 i

Operation:
XCH
(A) $\rightleftarrows$ ((Ri))

XCHD A,@Ri

Function: Exchange Digit

Description: XCHD exchanges the low-order nibble of the Accumulator (bits 3-0), generally representing a hexadecimal or BCD digit, with that of the internal RAM location indirectly addressed by the specified register. The high-order nibbles (bits 7-4) of each register are not affected. No flags are affected.

Example: R0 contains the address 20H. The Accumulator holds the value 36H (00110110B). Internal RAM location 20H holds the value 75H (01110101B). The instruction,

XCHD A,@R0

will leave RAM location 20H holding the value 76H (01110110B) and 35H (00110101B) in the Accumulator.

Bytes: 1

Cycles: 1

Encoding:

1 1 0 1	0 1 1 i

Operation: XCHD
$(A_{3\text{-}0}) \rightleftarrows ((Ri_{3\text{-}0}))$

XRL <dest-byte>,<src-byte>

Function: Logical Exclusive-OR for byte variables

Description: XRL performs the bitwise logical Exclusive-OR operation between the indicated variables, storing the results in the destination. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

(*Note:* When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.)

Example: If the Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B) then the instruction,

XRL A,R0

will leave the Accumulator holding the value 69H (01101001B).

When the destination is a directly addressed byte, this instruction can complement combinations of bits in any RAM location or hardware register. The pattern of bits to be complemented is then determined by a mask byte, either a constant contained in the instruction or a variable computed in the Accumulator at run-time. The instruction,

XRL P1,#00110001B

will complement bits 5, 4, and 0 of output Port 1.

XRL A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 1 1 0	1 r r r

Operation: XRL
(A) ← (A) ∀ (Rn)

XRL A,direct

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 1 0 1	direct address

Operation: XRL
(A) ← (A) ∀ (direct)

XRL A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 1 1 0	0 1 1 i

Operation: XRL
(A) ← (A) ∀ ((Ri))

XRL A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 1 0 0	immediate data

Operation: XRL
(A) ← (A) ∀ #data

XRL direct,A

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 0 1 0	direct address

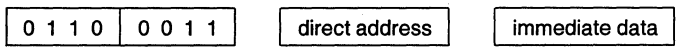
Operation: XRL
(direct) ← (direct) ∀ (A)

XRL direct, #data

Bytes: 3

Cycles: 2

Encoding:



Operation: XRL
(direct) ← (direct) ∀ #data

MCS®-51 Hardware Descriptions and Data Sheets

7

intel®

October 1991

8051, 8052 and 80C51 Hardware Description

7

Order Number: 270252-005

8051, 8052 and 80C51 Hardware Description

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8051, 8052 AND 80C51 HARDWARE DESCRIPTION

INTRODUCTION

This chapter presents a comprehensive description of the on-chip hardware features of the MCS®-51 microcontrollers. Included in this description are

- The port drivers and how they function both as ports and, for Ports 0 and 2, in bus operations
- The Timer/Counters
- The Serial Interface
- The Interrupt System
- Reset
- The Reduced Power Modes in the CHMOS devices
- The EPROM versions of the 8051AH, 8052AH and 80C51BH

The devices under consideration are listed in Table 1. As it becomes unwieldy to be constantly referring to each of these devices by their individual names, we will adopt a convention of referring to them generically as 8051s and 8052s, unless a specific member of the group is being referred to, in which case it will be specifically named. The "8051s" include the 8051AH, 80C51BH, and their ROMless and EPROM versions. The "8052s" are the 8052AH, 8032AH and 8752BH.

Figure 1 shows a functional block diagram of the 8051s and 8052s.

Table 1. The MCS-51 Family of Microcontrollers

Device Name	ROMless Version	EPROM Version	ROM Bytes	RAM Bytes	16-bit Timers	Ckt Type
8051AH	8031AH	8751H, 8751BH	4K	128	2	HMOS
8052AH	8032AH	8752BH	8K	256	3	HMOS
80C51BH	80C31BH	87C51	4K	128	2	CHMOS

Special Function Registers

A map of the on-chip memory area called SFR (Special Function Register) space is shown in Figure 2. SFRs marked by parentheses are resident in the 8052s but not in the 8051s.

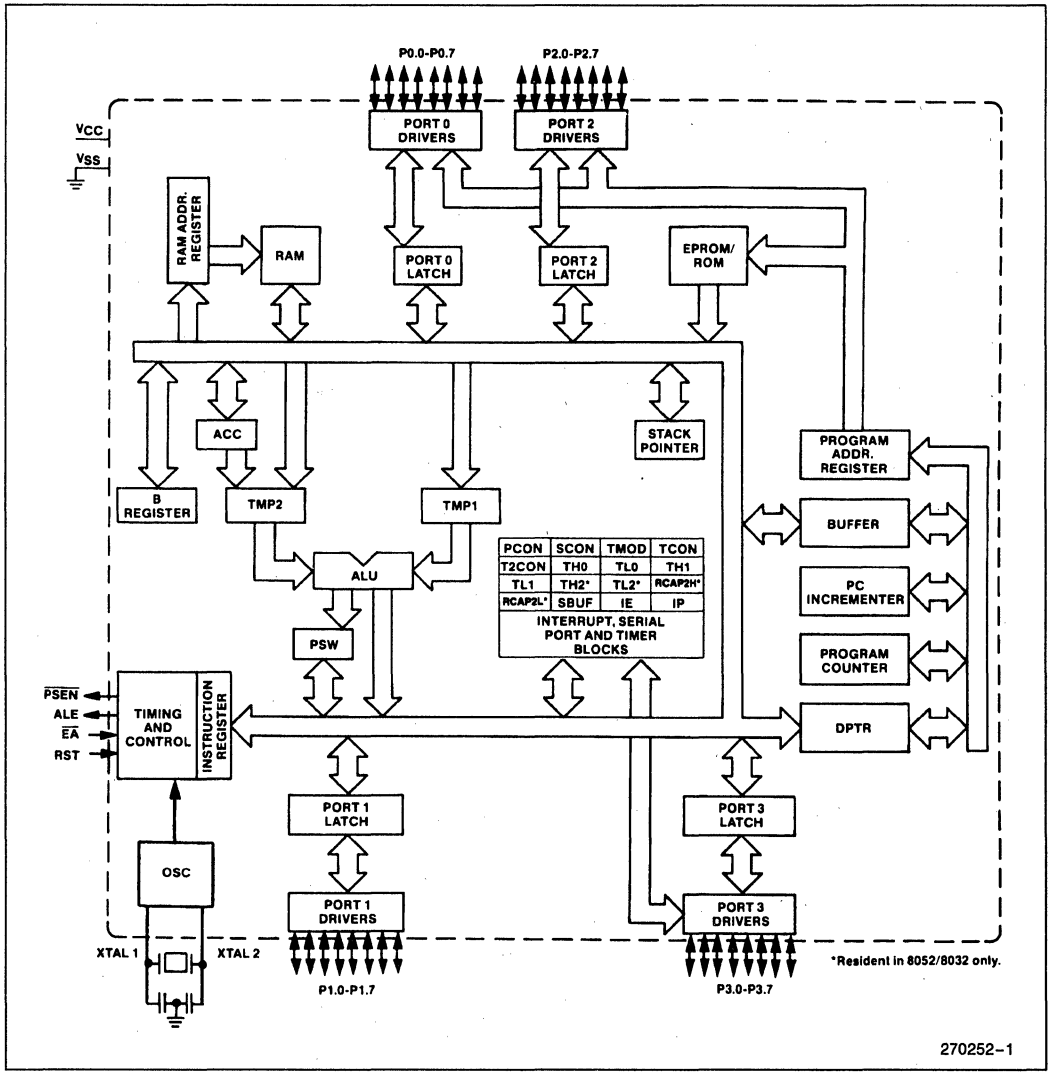


Figure 1. MCS-51 Architectural Block Diagram

	8 Bytes								
F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8									DF
D0	PSW								D7
C8	(T2CON)		(RCAP2L)	(RCAP2H)	(TL2)	(TH2)			CF
C0									C7
B8	IP								BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1								97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

Figure 2. SFR Map. (. . .) Indicates Resident in 8052s, not in 8051s

Note that not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have no effect.

User software should not write 1s to these unimplemented locations, since they may be used in future MCS-51 products to invoke new features. In that case the reset or inactive values of the new bits will always be 0, and their active values will be 1.

The functions of the SFRs are outlined below.

ACCUMULATOR

ACC is the Accumulator register. The mnemonics for Accumulator-Specific instructions, however, refer to the Accumulator simply as A.

B REGISTER

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

PROGRAM STATUS WORD

The PSW register contains program status information as detailed in Figure 3.

STACK POINTER

The Stack Pointer Register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

DATA POINTER

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

PORTS 0 TO 3

P0, P1, P2 and P3 are the SFR latches of Ports 0, 1, 2 and 3, respectively.

SERIAL DATA BUFFER

The Serial Data Buffer is actually two separate registers, a transmit buffer and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer where it is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

TIMER REGISTERS

Register pairs (TH0, TL0), (TH1, TL1), and (TH2, TL2) are the 16-bit Counting registers for Timer/Counters 0, 1, and 2, respectively.

CAPTURE REGISTERS

The register pair (RCAP2H, RCAP2L) are the Capture registers for the Timer 2 "Capture Mode." In this mode, in response to a transition at the 8052's T2EX pin, TH2 and TL2 are copied into RCAP2H and RCAP2L. Timer 2 also has a 16-bit auto-reload mode, and RCAP2H and RCAP2L hold the reload value for this mode. More about Timer 2's features in a later section.

CONTROL REGISTERS

Special Function Registers IP, IE, TMOD, TCON, T2CON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port. They are described in later sections.

(MSB)							(LSB)
CY	AC	F0	RS1	RS0	OV	—	P

Symbol	Position	Name and Significance
CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary Carry flag. (For BCD operations.)
F0	PSW.5	Flag 0 (Available to the user for general purposes.)
RS1	PSW.4	Register bank select control bits 1 &
RS0	PSW.3	0. Set/cleared by software to determine working register bank (see Note).
OV	PSW.2	Overflow flag.
—	PSW.1	User definable flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/ even number of "one" bits in the Accumulator, i.e., even parity.

NOTE:
The contents of (RS1, RS0) enable the working register banks as follows:

(0.0)—Bank 0 (00H–07H)
(0.1)—Bank 1 (08H–0FH)
(1.0)—Bank 2 (10H–17H)
(1.1)—Bank 3 (18H–1FH)

Figure 3. PSW: Program Status Word Register

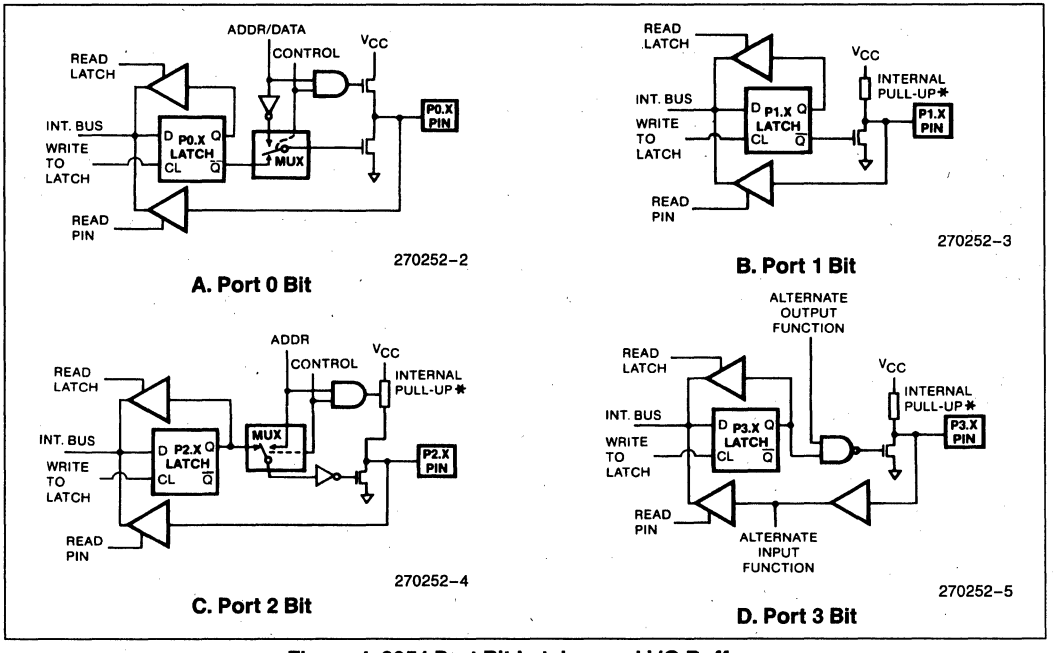


Figure 4. 8051 Port Bit Latches and I/O Buffers
*See Figure 5 for details of the internal pullup.

PORT STRUCTURES AND OPERATION

All four ports in the 8051 are bidirectional. Each consists of a latch (Special Function Registers P0 through P3), an output driver, and an input buffer.

The output drivers of Ports 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise the Port 2 pins continue to emit the P2 SFR content.

All the Port 3 pins, and (in the 8052) two Port 1 pins are multifunctional. They are not only port pins, but also serve the functions of various special features as listed on the following page.

Port Pin	Alternate Function
*P1.0	T2 (Timer/Counter 2 external input)
*P1.1	T2EX (Timer/Counter 2 Capture/Reload trigger)
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt)
P3.3	$\overline{INT1}$ (external interrupt)
P3.4	T0 (Timer/Counter 0 external input)
P3.5	T1 (Timer/Counter 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	$\overline{RD}$ (external Data Memory read strobe)

*P1.0 and P1.1 serve these alternate functions only on the 8052.

The alternate functions can only be activated if the corresponding bit latch in the port SFR contains a 1. Otherwise the port pin is stuck at 0.

I/O Configurations

Figure 4 shows a functional diagram of a typical bit latch and I/O buffer in each of the four ports. The bit latch (one bit in the port's SFR) is represented as a Type D flip-flop, which will clock in a value from the internal bus in response to a "write to latch" signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a "read latch" signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a "read pin" signal from the CPU. Some instructions that read a port activate the "read latch" signal, and others activate the "read pin" signal. More about that later.

As shown in Figure 4, the output drivers of Ports 0 and 2 are switchable to an internal ADDR and ADDR/DATA bus by an internal CONTROL signal for use in external memory accesses. During external memory accesses, the P2 SFR remains unchanged, but the P0 SFR gets 1s written to it.

Also shown in Figure 4, is that if a P3 bit latch contains a 1, then the output level is controlled by the signal labeled "alternate output function." The actual P3.X pin level is always available to the pin's alternate input function, if any.

Ports 1, 2, and 3 have internal pullups. Port 0 has open drain outputs. Each I/O line can be independently used as an input or an output. (Ports 0 and 2 may not be used as general purpose I/O when being used as the ADDR/DATA BUS). To be used as an input, the port bit latch must contain a 1, which turns off the output driver FET. Then, for Ports 1, 2, and 3, the pin is pulled high by the internal pullup, but can be pulled low by an external source.

Port 0 differs in not having internal pullups. The pullup FET in the P0 output driver (see Figure 4) is used only when the Port is emitting 1s during external memory accesses. Otherwise the pullup FET is off. Consequently P0 lines that are being used as output port lines are open drain. Writing a 1 to the bit latch leaves both output FETs off, so the pin floats. In that condition it can be used a high-impedance input.

Because Ports 1, 2, and 3 have fixed internal pullups they are sometimes called "quasi-bidirectional" ports. When configured as inputs they pull high and will source current (IIL, in the data sheets) when externally pulled low. Port 0, on the other hand, is considered "true" bidirectional, because when configured as an input it floats.

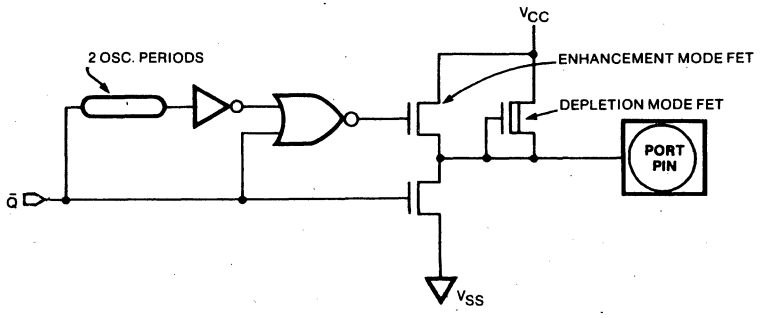
All the port latches in the 8051 have 1s written to them by the reset function. If a 0 is subsequently written to a port latch, it can be reconfigured as an input by writing a 1 to it.

Writing to a Port

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during S6P2 of the final cycle of the instruction. However, port latches are in fact sampled by their output buffers only during Phase 1 of any clock period. (During Phase 2 the output buffer holds the value it saw during the previous Phase 1). Consequently, the new value in the port latch won't actually appear at the output pin until the next Phase 1, which will be at S1P1 of the next machine cycle. See Figure 39 in the Internal Timing section.

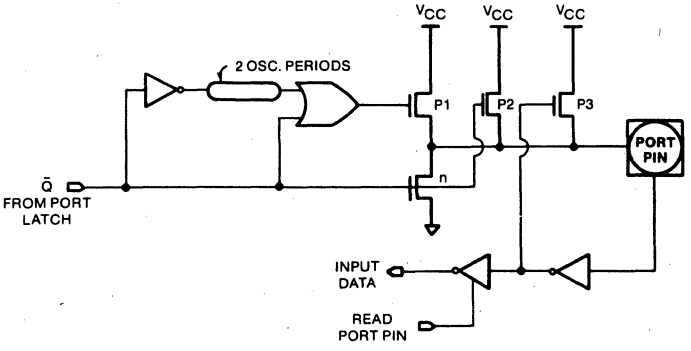
If the change requires a 0-to-1 transition in Port 1, 2, or 3, an additional pullup is turned on during S1P1 and S1P2 of the cycle in which the transition occurs. This is done to increase the transition speed. The extra pullup can source about 100 times the current that the normal pullup can. It should be noted that the internal pullups are field-effect transistors, not linear resistors. The pullup arrangements are shown in Figure 5.

In HMOS versions of the 8051, the fixed part of the pullup is a depletion-mode transistor with the gate wired to the source. This transistor will allow the pin to source about 0.25 mA when shorted to ground. In parallel with the fixed pullup is an enhancement-mode transistor, which is activated during S1 whenever the port bit does a 0-to-1 transition. During this interval, if the port pin is shorted to ground, this extra transistor will allow the pin to source an additional 30 mA.



270252-6

A. HMOS Configuration. The enhancement mode transistor is turned on for 2 osc. periods after $\overline{Q}$ makes a 0-to-1 transition.



270252-7

B. CHMOS Configuration. pFET 1 is turned on for 2 osc. periods after $\overline{Q}$ makes a 0-to-1 transition. During this time, pFET 1 also turns on pFET 3 through the inverter to form a latch which holds the 1. pFET 2 is also on.

Figure 5. Ports 1 And 3 HMOS And CHMOS Internal Pullup Configurations. Port 2 is Similar Except That It Holds The Strong Pullup On While Emitting 1s That Are Address Bits. (See Text, "Accessing External Memory".)

In the CHMOS versions, the pullup consists of three pFETs. It should be noted that an n-channel FET (nFET) is turned on when a logical 1 is applied to its gate, and is turned off when a logical 0 is applied to its gate. A p-channel FET (pFET) is the opposite: it is on when its gate sees a 0, and off when its gate sees a 1.

pFET1 in Figure 5 is the transistor that is turned on for 2 oscillator periods after a 0-to-1 transition in the port latch. While it's on, it turns on pFET3 (a weak pull-up), through the inverter. This inverter and pFET form a latch which hold the 1.

Note that if the pin is emitting a 1, a negative glitch on the pin from some external source can turn off pFET3, causing the pin to go into a float state. pFET2 is a very weak pullup which is on whenever the nFET is off, in traditional CMOS style. It's only about $1/10$ the strength of pFET3. Its function is to restore a 1 to the pin in the event the pin *had* a 1 and lost it to a glitch.

Port Loading and Interfacing

The output buffers of Ports 1, 2, and 3 can each drive 4 LS TTL inputs. These ports on HMOS versions can be driven in a normal manner by any TTL or NMOS circuit. Both HMOS and CHMOS pins can be driven by open-collector and open-drain outputs, but note that 0-to-1 transitions will not be fast. In the HMOS device, if the pin is driven by an open-collector output, a 0-to-1 transition will have to be driven by the relatively weak depletion mode FET in Figure 5(A). In the CHMOS device, an input 0 turns off pullup pFET3, leaving only the very weak pullup pFET2 to drive the transition.

In external bus mode, Port 0 output buffers can each drive 8 LS TTL inputs. As port pins, they require external pullups to drive any inputs.

Read-Modify-Write Feature

Some instructions that read a port read the latch and others read the pin. Which ones do which? The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called "read-modify-write" instructions. The instructions listed below are read-modify-write instructions. When the destination operand is a port, or a port bit, these instructions read the latch rather than the pin:

ANL	(logical AND, e.g., ANL P1, A)
ORL	(logical OR, e.g., ORL P2, A)
XRL	(logical EX-OR, e.g., XRL P3, A)
JBC	(jump if bit = 1 and clear bit, e.g., JBC P1.1, LABEL)
CPL	(complement bit, e.g., CPL P3.0)
INC	(increment, e.g., INC P2)
DEC	(decrement, e.g., DEC P2)
DJNZ	(decrement and jump if not zero, e.g., DJNZ P3, LABEL)
MOV, PX.Y, C	(move carry bit to bit Y of Port X)
CLR PX.Y	(clear bit Y of Port X)
SETB PX.Y	(set bit Y of Port X)

It is not obvious that the last three instructions in this list are read-modify-write instructions, but they are. They read the port byte, all 8 bits, modify the addressed bit, then write the new byte back to the latch.

The reason that read-modify-write instructions are directed to the latch rather than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. When a 1 is written to the bit, the transistor is turned on. If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1.

ACCESSING EXTERNAL MEMORY

Accesses to external memory are of two types: accesses to external Program Memory and accesses to external Data Memory. Accesses to external Program Memory use signal $\overline{PSEN}$ (program store enable) as the read strobe. Accesses to external Data Memory use $\overline{RD}$ or $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory. Refer to Figures 36 through 38 in the Internal Timing section.

Fetches from external Program Memory always use a 16-bit address. Accesses to external Data Memory can use either a 16-bit address (MOVX @DPTR) or an 8-bit address (MOVX @Ri).

Whenever a 16-bit address is used, the high byte of the address comes out on Port 2, where it is held for the duration of the read or write cycle. Note that the Port 2 drivers use the strong pullups during the entire time that they are emitting address bits that are 1s. This is during the execution of a MOVX @DPTR instruction. During this time the Port 2 latch (the Special Function Register) does not have to contain 1s, and the contents of the Port 2 SFR are not modified. If the external memory cycle is not immediately followed by another external memory cycle, the undisturbed contents of the Port 2 SFR will reappear in the next cycle.

If an 8-bit address is being used (MOVX @Ri), the contents of the Port 2 SFR remain at the Port 2 pins throughout the external memory cycle. This will facilitate paging.

In any case, the low byte of the address is time-multiplexed with the data byte on Port 0. The ADDR/DATA signal drives both FETs in the Port 0 output buffers. Thus, in this application the Port 0 pins are not open-drain outputs, and do not require external pullups. Signal ALE (Address Latch Enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is deactivated.

During any access to external memory, the CPU writes 0FFH to the Port 0 latch (the Special Function Register), thus obliterating whatever information the Port 0 SFR may have been holding. If the user writes to Port 0 during an external memory fetch, the incoming code byte is corrupted. Therefore, do not write to Port 0 if external program memory is used.

External Program Memory is accessed under two conditions:

1) Whenever signal $\overline{EA}$ is active; or
2) Whenever the program counter (PC) contains a number that is larger than 0FFFH (1FFFH for the 8052).

This requires that the ROMless versions have $\overline{EA}$ wired low to enable the lower 4K (8K for the 8032) program bytes to be fetched from external memory.

When the CPU is executing out of external Program Memory, all 8 bits of Port 2 are dedicated to an output function and may not be used for general purpose I/O. During external program fetches they output the high byte of the PC. During this time the Port 2 drivers use the strong pullups to emit PC bits that are 1s.

TIMER/COUNTERS

The 8051 has two 16-bit Timer/Counter registers: Timer 0 and Timer 1. The 8052 has these two plus one

more: Timer 2. All three can be configured to operate either as timers or event counters.

In the "Timer" function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is $1/12$ of the oscillator frequency.

In the "Counter" function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0, T1 or (in the 8052) T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is $1/24$ of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

In addition to the "Timer" or "Counter" selection, Timer 0 and Timer 1 have four operating modes from which to select. Timer 2, in the 8052, has three modes of operation: "Capture," "Auto-Reload" and "baud rate generator."

Timer 0 and Timer 1

These Timer/Counters are present in both the 8051 and the 8052. The "Timer" or "Counter" function is selected by control bits C/$\overline{T}$ in the Special Function Register TMOD (Figure 6). These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timer/Counters. Mode 3 is different. The four operating modes are described in the following text.

MODE 0

Either Timer in Mode 0 is an 8-bit Counter with a divide-by-32 prescaler. This 13-bit timer is MCS-48 compatible. Figure 7 shows the Mode 0 operation as it applies to Timer 1.

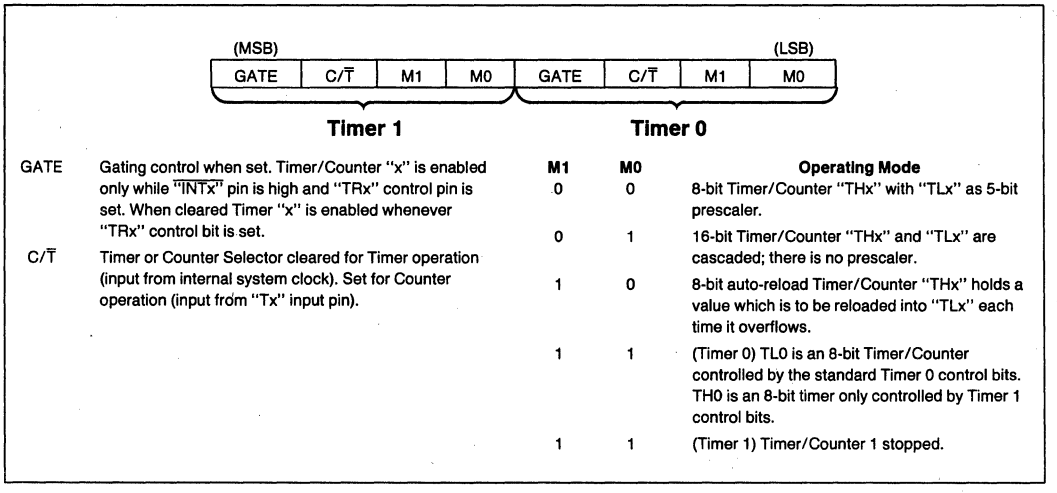
In this mode, the Timer register is configured as a 13-Bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or $\overline{INT1}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements.) TR1 is a control bit in the Special Function Register TCON (Figure 8). GATE is in TMOD.

The 13-Bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1. Substitute TR0, TF0 and $\overline{INT0}$ for the corresponding Timer 1 signals in Figure 7. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

MODE 1

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.



GATE	Gating control when set. Timer/Counter "x" is enabled only while "INTx" pin is high and "TRx" control pin is set. When cleared Timer "x" is enabled whenever "TRx" control bit is set.
C/$\overline{T}$	Timer or Counter Selector cleared for Timer operation (input from internal system clock). Set for Counter operation (input from "Tx" input pin).

M1	M0	Operating Mode
0	0	8-bit Timer/Counter "THx" with "TLx" as 5-bit prescaler.
0	1	16-bit Timer/Counter "THx" and "TLx" are cascaded; there is no prescaler.
1	0	8-bit auto-reload Timer/Counter "THx" holds a value which is to be reloaded into "TLx" each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter 1 stopped.

Figure 6. TMOD: Timer/Counter Mode Control Register

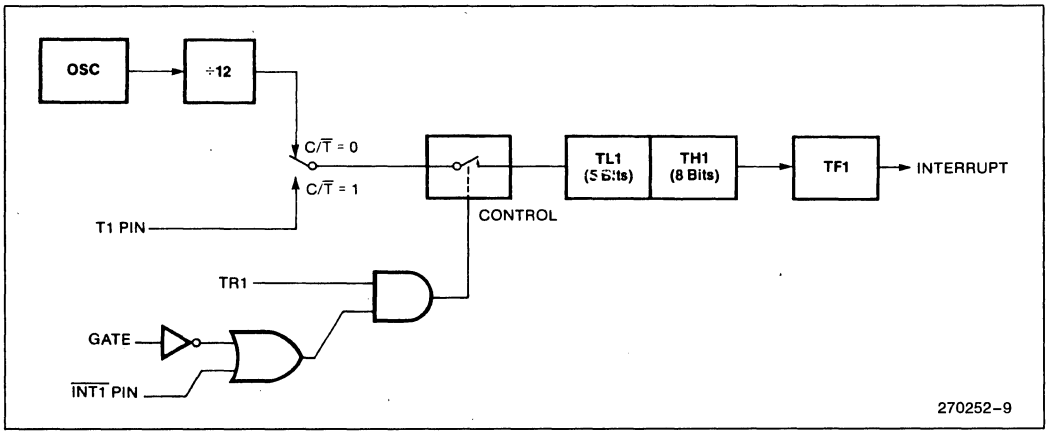


Figure 7. Timer/Counter 1 Mode 0: 13-Bit Counter

(MSB)							(LSB)
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Symbol	Position	Name and Significance
TF1	TCON.7	Timer 1 overflow Flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR1	TCON.6	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter on/off.
TF0	TCON.5	Timer 0 overflow Flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR0	TCON.4	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter on/off.
IE1	TCON.3	Interrupt 1 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT1	TCON.2	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
IE0	TCON.1	Interrupt 0 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT0	TCON.0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

Figure 8.TCON: Timer/Counter Control Register

MODE 2

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 9. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload leaves TH1 unchanged.

Mode 2 operation is the same for Timer/Counter 0.

MODE 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 10. TL0 uses the Timer 0 control bits: C/$\overline{T}$, GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the "Timer 1" interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, an 8051 can look like it has three Timer/Counters, and an 8052, like it has four. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

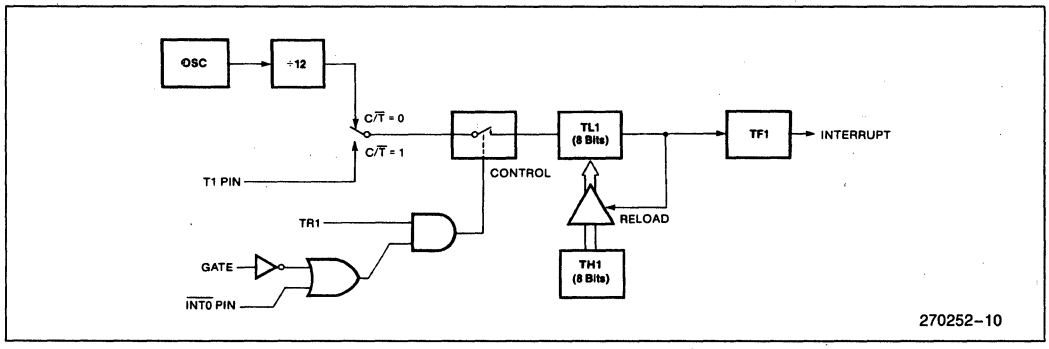


Figure 9. Timer/Counter 1 Mode 2: 8-Bit Auto-Reload

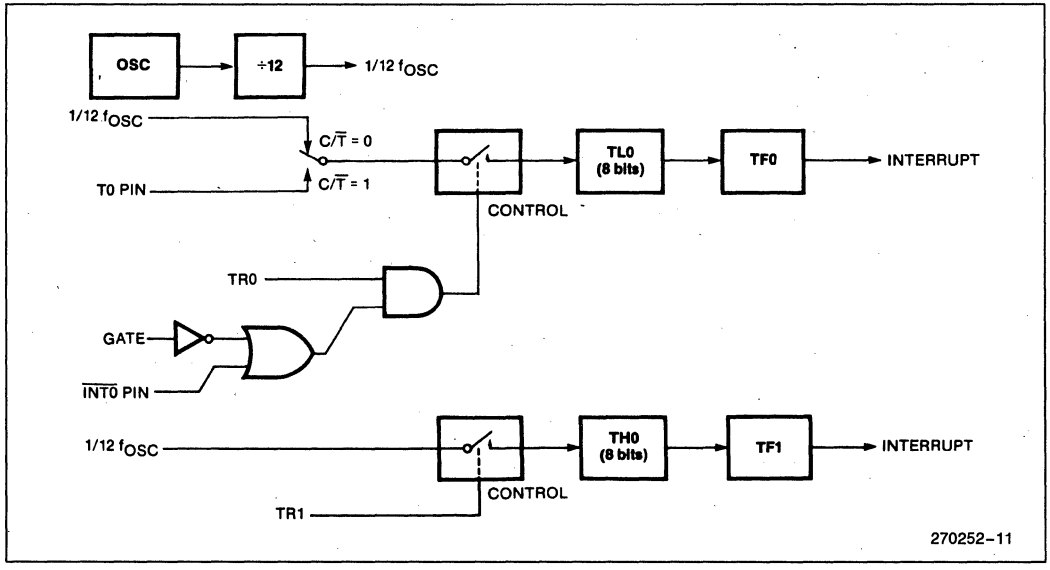


Figure 10. Timer/Counter 0 Mode 3: Two 8-Bit Counters

Timer 2

Timer 2 is a 16-bit Timer/Counter which is present only in the 8052. Like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/$\overline{T2}$ in the Special Function Register T2CON (Figure 11). It has three operating modes: "capture," "auto-load" and "baud rate generator," which are selected by bits in T2CON as shown in Table 2.

Table 2. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	Mode
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(off)

(MSB) (LSB)

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Figure 11. T2CON: Timer/Counter 2 Control Register

In the Capture Mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. (RCAP2L and RCAP2H are new Special Function Registers in the 8052.) In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt.

The Capture Mode is illustrated in Figure 12.

In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2.

The auto-reload mode is illustrated in Figure 13.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1. It will be described in conjunction with the serial port.

SERIAL INTERFACE

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

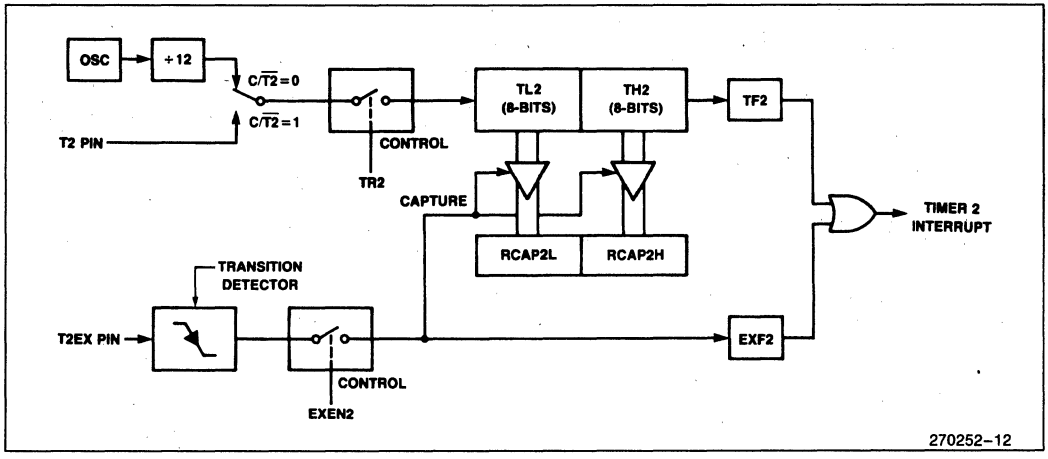


Figure 12. Timer 2 in Capture Mode

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Functon Register SCON, while the stop bit is ignored. The baud rate is programmable to either $1/32$ or $1/64$ the oscillator frequency.

Mode 3: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except the baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

Serial Port Control Register

The serial port control and status register is the Special Function Register SCON, shown in Figure 14. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

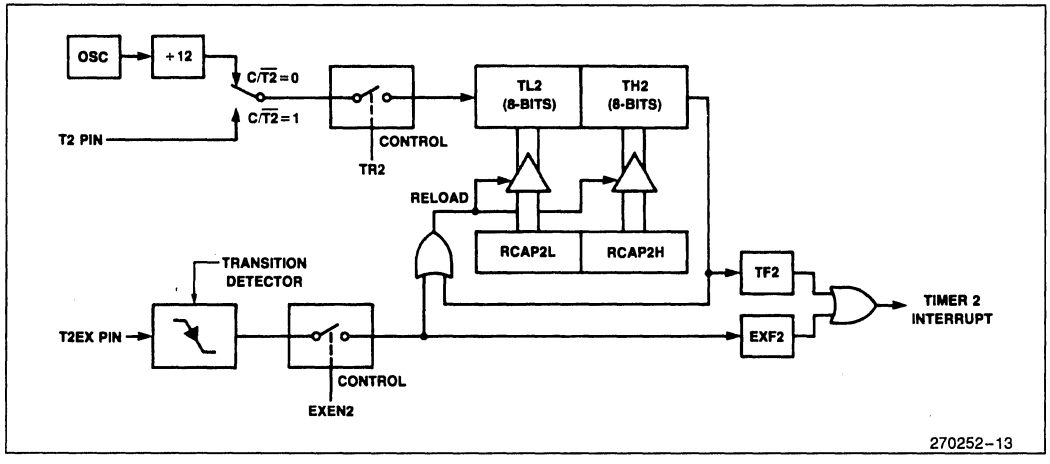


Figure 13. Timer 2 in Auto-Reload Mode

(MSB)							(LSB)
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	shift register	$f_{osc.}/12$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{osc.}/64$ or $f_{osc.}/32$
1	1	3	9-bit UART	variable

- SM2 enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.
- REN enables serial reception. Set by software to enable reception. Clear by software to disable reception.
- TB8 is the 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
- RB8 in Modes 2 and 3, is the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
- TI is transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
- RI is receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Figure 14. SCON: Serial Port Control Register

Baud Rates

The baud rate in Mode 0 is fixed:

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), the baud rate $1/64$ the oscillator frequency. If SMOD = 1, the baud rate is $1/32$ the oscillator frequency.

$$\text{Mode 2 Baud Rate} = \frac{2^{\text{SMOD}}}{64} \times (\text{Oscillator Frequency})$$

In the 8051, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate. In the 8052, these baud rates can be determined by Timer 1, or by Timer 2, or by both (one for transmit and the other for receive).

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$\text{Modes 1, 3 Baud Rate} = \frac{2^{SMOD}}{32} \times \text{(Timer 1 Overflow Rate)}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case, the baud rate is given by the formula

$$\text{Modes 1, 3 Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{\text{Oscillator Frequency}}{12x\,[256 - (TH1)]}$$

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload.

Figure 15 lists various commonly used baud rates and how they can be obtained from Timer 1.

Baud Rate	fosc	SMOD	Timer 1		
			C/$\overline{T}$	Mode	Reload Value
Mode 0 Max: 1 MHZ	12 MHZ	X	X	X	X
Mode 2 Max: 375K	12 MHZ	1	X	X	X
Modes 1, 3: 62.5K	12 MHZ	1	0	2	FFH
19.2K	11.059 MHZ	1	0	2	FDH
9.6K	11.059 MHZ	0	0	2	FDH
4.8K	11.059 MHZ	0	0	2	FAH
2.4K	11.059 MHZ	0	0	2	F4H
1.2K	11.059 MHZ	0	0	2	E8H
137.5	11.986 MHZ	0	0	2	1DH
110	6 MHZ	0	0	2	72H
110	12 MHZ	0	0	1	FEEBH

Figure 15. Timer 1 Generated Commonly Used Baud Rates

Using Timer 2 to Generate Baud Rates

In the 8052, Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Figure 11). Note then the baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 16.

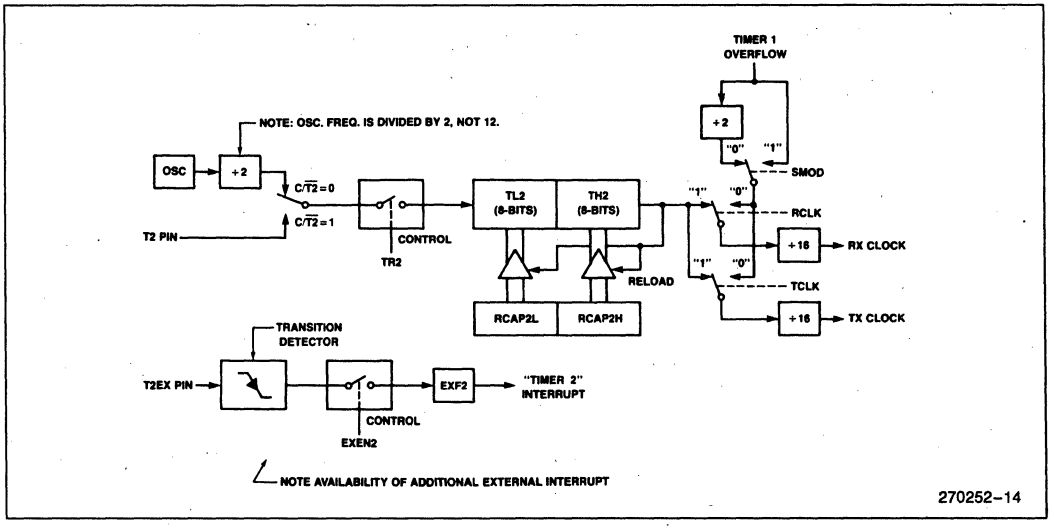


Figure 16. Timer 2 in Baud Rate Generator Mode

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

Now, the baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either "timer" or "counter" operation. In the most typical applications, it is configured for "timer" operation (C/T2 = 0). "Timer" operation is a little different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer it would increment every machine cycle (thus at $1/12$ the oscillator frequency). As a baud rate generator, however, it increments every state time (thus at $1/2$ the oscillator frequency). In that case the baud rate is given by the formula

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32\text{x}\,[65536 - (\text{RCAP2H, RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 16. This Figure is valid only if RCLK + TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the Timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP registers may be read, but shouldn't be written to, because a write might overlap a reload and cause write and/or reload errors. Turn the Timer off (clear TR2) before accessing the Timer 2 or RCAP registers, in this case.

More About Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at $1/12$ the oscillator frequency.

Figure 17 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between "write to SBUF," and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0, and also enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1 and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift register are shifted to the right one position.

As data bits shift out to the right, zeroes come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX Control block to do one last shift and then deactivate SEND and set TI. Both of these actions occur at S1P1 of the 10th machine cycle after "write to SBUF."

Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared and RI is set.

More About Mode 1

Ten bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the 8051 the baud rate is determined by the Timer 1 overflow rate. In the 8052 it is determined either by the Timer 1 overflow rate, or the Timer 2 overflow rate, or both (one for transmit and the other for receive).

Figure 18 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

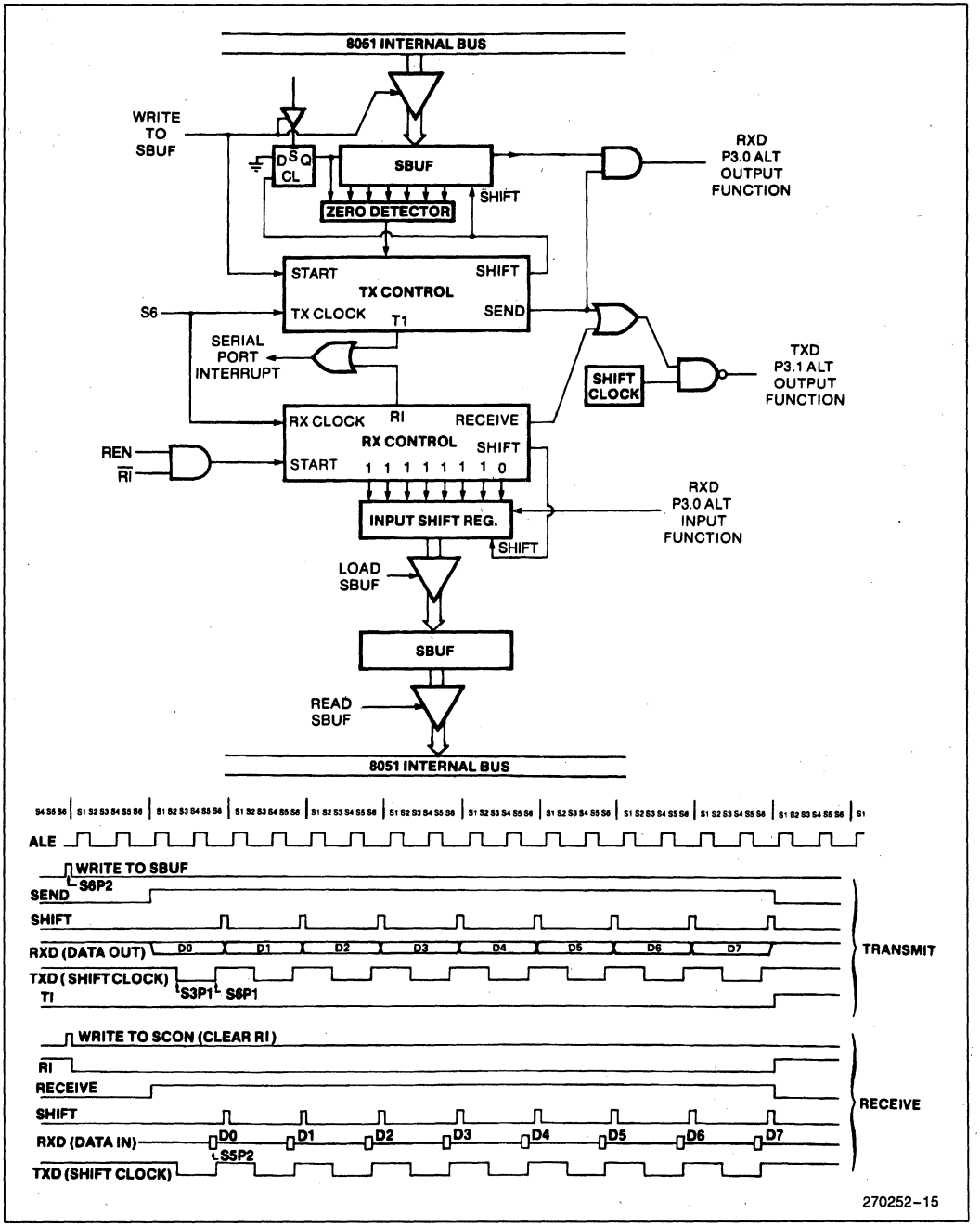


Figure 17. Serial Port Mode 0

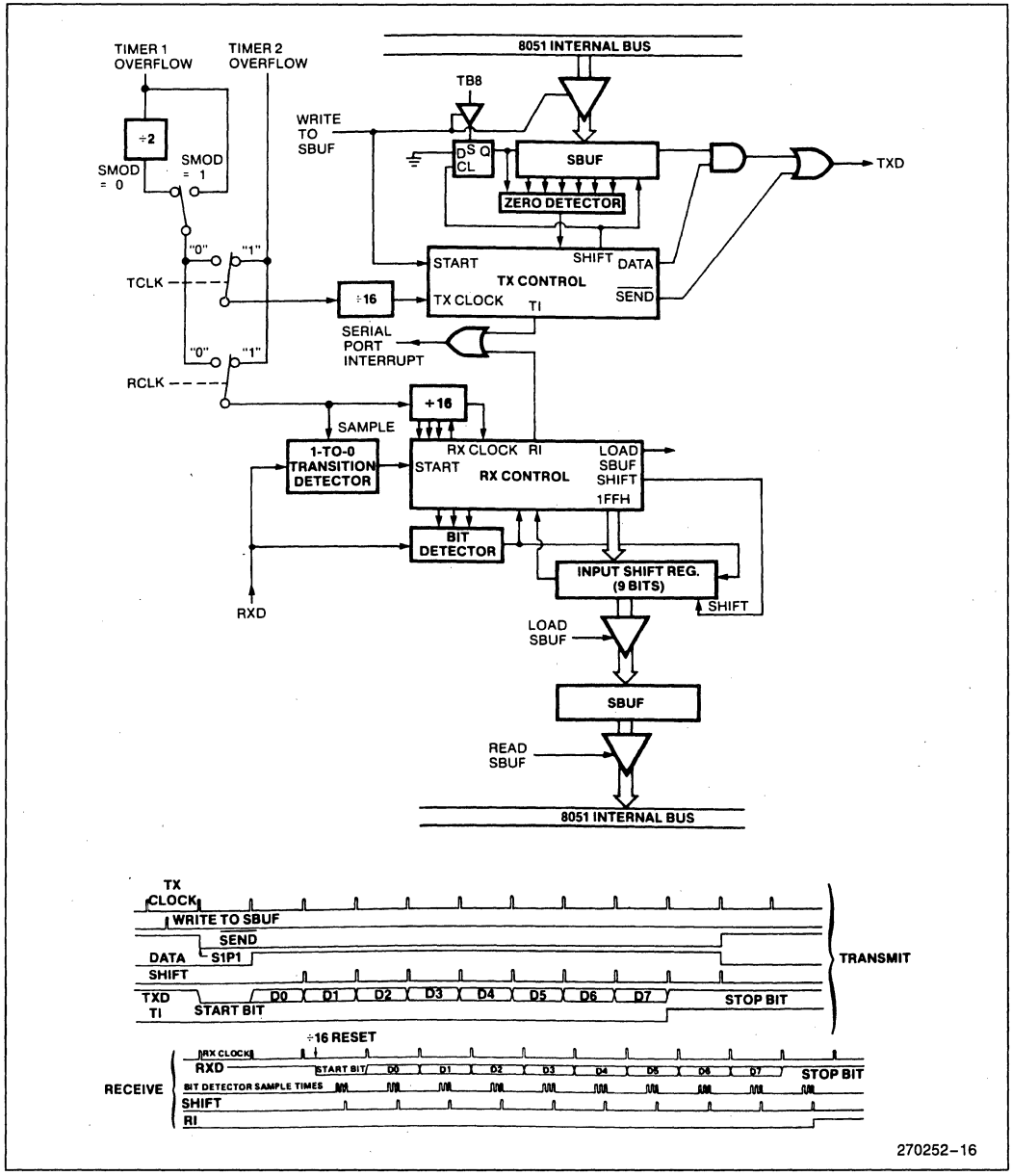


Figure 18. Serial Port Mode 1. TCLK, RCLK and Timer 2 are Present in the 8052/8032 Only.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal).

The transmission begins with activation of $\overline{\text{SEND}}$, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeroes are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift and then deactivate $\overline{\text{SEND}}$ and set TI. This occurs at the 10th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register, (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1) RI = 0, and
2) Either SM2 = 0, or the received stop bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RXD.

More About Modes 2 and 3

Eleven bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either $1/32$ or $1/64$ the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from either Timer 1 or 2 depending on the state of TCLK and RCLK.

Figures 19 and 20 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeroes are clocked in. Thus, as data bits shift out to the right, zeroes are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

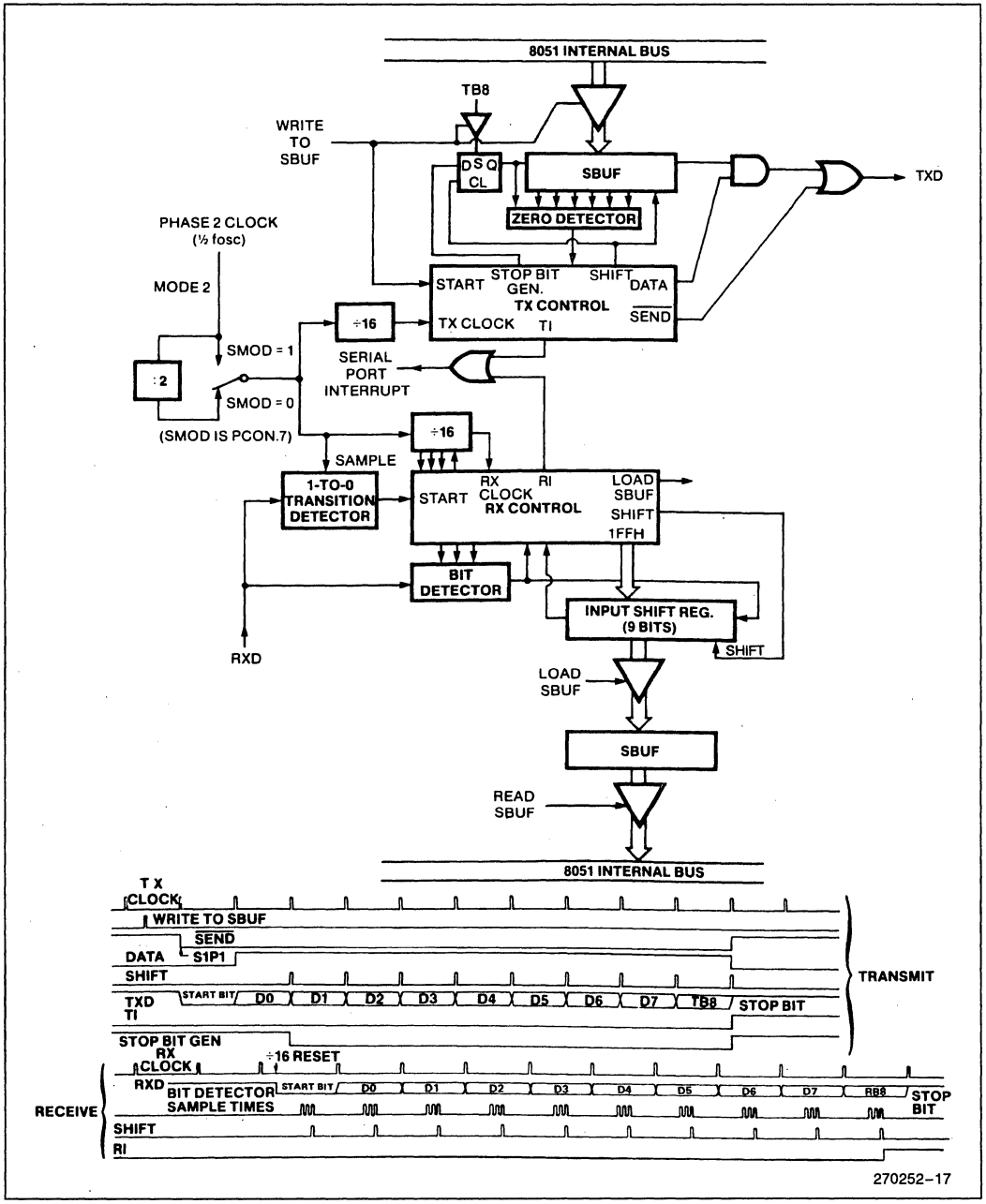


Figure 19. Serial Port Mode 2

7

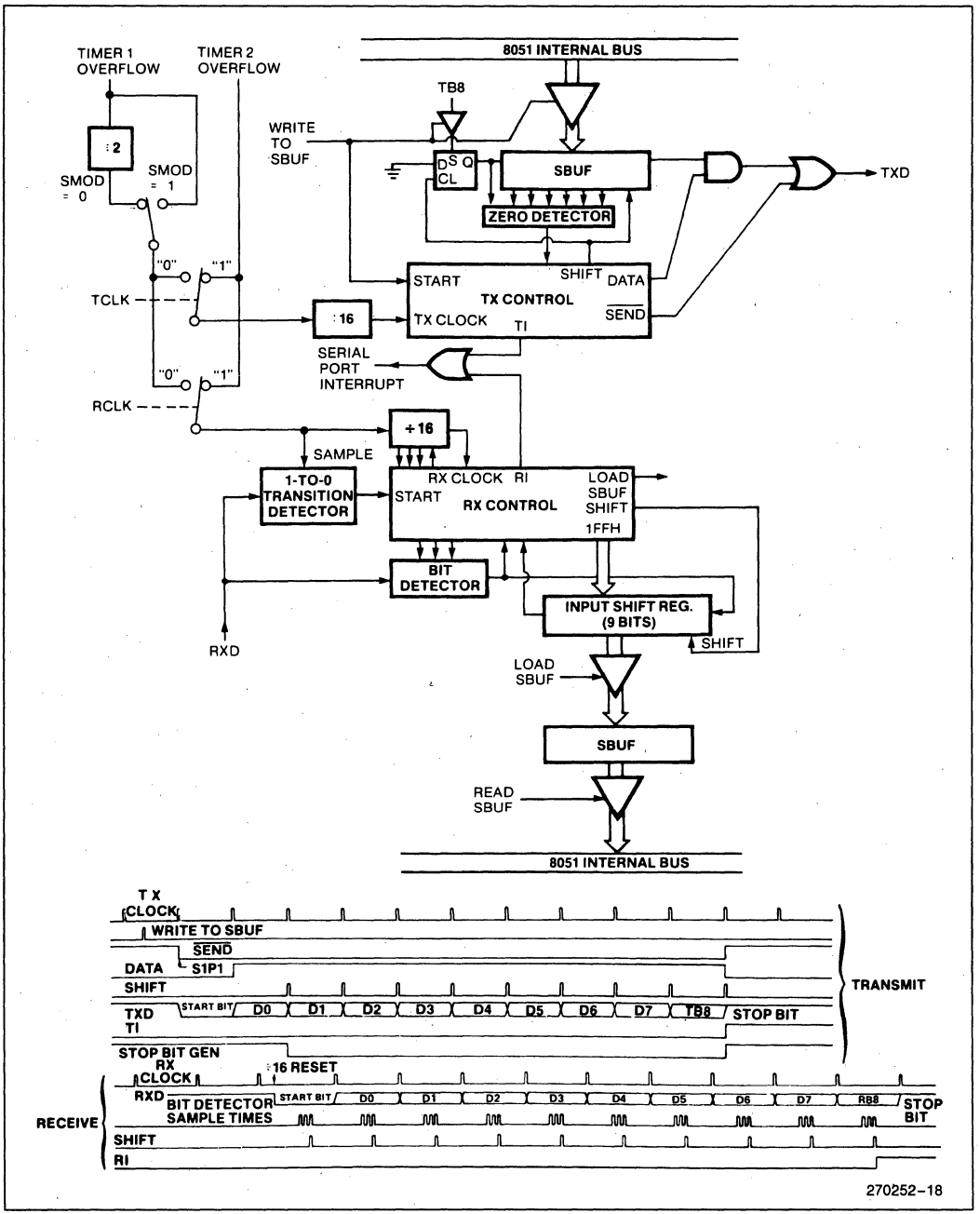


Figure 20. Serial Port Mode 3. TCLK, RCLK, and Timer 2 are Present in the 8052/8032 Only.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

1) RI = 0, and
2) Either SM2 = 0 or the received 9th data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RXD input.

Note that the value of the received stop bit is irrelevant to SBUF, RB8, or RI.

INTERRUPTS

The 8051 provides 5 interrupt sources. The 8052 provides 6. These are shown in Figure 21.

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. When an external interrupt is generated, the flag that generated it is cleared by the hardware when the service routine is vectored to only if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source is what controls the request flag, rather than the on-chip hardware.

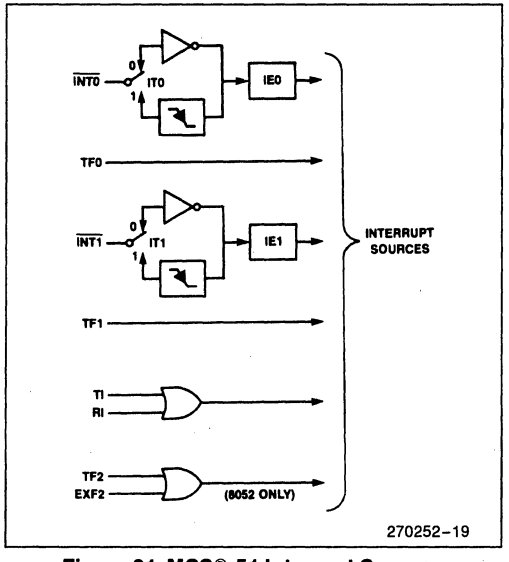


Figure 21. MCS®-51 Interrupt Sources

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers (except see Timer 0 in Mode 3). When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

The Serial Port Interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine will normally have to determine whether it was RI or TI that generated the interrupt, and the bit will have to be cleared in software.

In the 8052, the Timer 2 Interrupt is generated by the logical OR of TF2 and EXF2. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and the bit will have to be cleared in software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be canceled in software.

(MSB) (LSB)

EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

Symbol	Position	Function
EA	IE.7	disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, since they may be used in future MCS-51 products.

Figure 22. IE: Interrupt Enable Register

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE (Figure 22). IE contains also a global disable bit, EA, which disables all interrupts at once.

Note in Figure 22 that bit position IE.6 is unimplemented. In the 8051s, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future MCS-51 products.

Priority Level Structure

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in Special Function Register IP (Figure 23). A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

(MSB) (LSB)

—	—	PT2	PS	PT1	PX1	PT0	PX0

Priority bit = 1 assigns high priority.
Priority bit = 0 assigns low priority.

Symbol	Position	Function
—	IP.7	reserved
—	IP.6	reserved
PT2	IP.5	Timer 2 interrupt priority bit.
PS	IP.4	Serial Port interrupt priority bit.
PT1	IP.3	Timer 1 interrupt priority bit.
PX1	IP.2	External interrupt 1 priority bit.
PT0	IP.1	Timer 0 interrupt priority bit.
PX0	IP.0	External interrupt 0 priority bit.

User software should never write 1s to unimplemented bits, since they may be used in future MCS-51 products.

Figure 23. IP: Interrupt Priority Register

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the **same** priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence, as follows:

	Source	Priority Within Level
1.	IE0	(highest)
2.	TF0	
3.	IE1	
4.	TF1	
5.	RI + TI	
6.	TF2 + EXF2	(lowest)

Note that the "priority within level" structure is only used to resolve *simultaneous requests of the same priority level.*

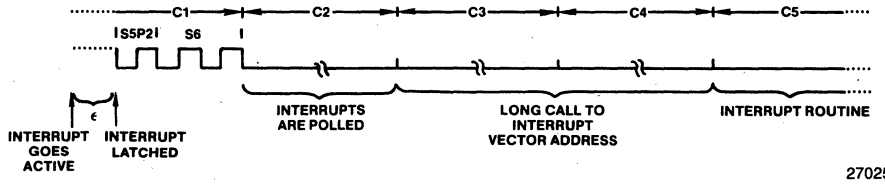
The IP register contains a number of unimplemented bits. IP.7 and IP.6 are vacant in the 8052s, and in the 8051s these and IP.5 are vacant. User software should not write 1s to these bit positions, since they may be used in future MCS-51 products.

How Interrupts Are Handled

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. The 8052's Timer 2 interrupt cycle is different, as described in the Response Time Section. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress.
2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3. The instruction in progress is RETI or any write to the IE or IP registers.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be



This is the fastest possible response when C2 is the final cycle of an instruction other than RETI or an access to IE or IP.

Figure 24. Interrupt Response Timing Diagram

completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any access to IE or IP, then at least *one more* instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note then that if an interrupt flag is active but not being responded to for one of the above conditions, and is not *still* active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The polling cycle/LCALL sequence is illustrated in Figure 24.

Note that if an interrupt of higher priority level goes active prior to S5P2 of the machine cycle labeled C3 in Figure 24, then in accordance with the above rules it will be vectored to during C5 and C6, without any instruction of the lower priority routine having been executed.

Thus the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. In some cases it also clears the flag that generated the interrupt, and in other cases it doesn't. It never clears the Serial Port or Timer 2 flags. This has to be done in the user's software. It clears an external interrupt flag (IE0 or IE1) only if it was transition-activated. The hardware-generated LCALL pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as shown below.

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress.

External Interrupts

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{\text{INTx}}$ pin. If ITx = 1, external interrupt x is edge-triggered. In this mode if successive samples of the $\overline{\text{INTx}}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

Response Time

The $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ levels are inverted and latched into the interrupt flags IE0 and IE1 at S5P2 of every machine cycle. Similarly, the Timer 2 flag EXF2 and the Serial Port flags RI and TI are set at S5P2. The values are not actually polled by the circuitry until the next machine cycle.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag TF2 is set at S2P2 and is polled in the same cycle in which the timer overflows.

If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes two cycles. Thus, a minimum of three complete machine cycles elapse between activation of an external interrupt request and the beginning of execution of the first instruction of the service routine. Figure 24 shows interrupt response timings.

A longer response time would result if the request is blocked by one of the 3 previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than 3 cycles, since the longest instructions (MUL and DIV) are only 4

cycles long, and if the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one more cycle to complete the instruction in progress, plus 4 cycles to complete the next instruction if the instruction is MUL or DIV).

Thus, in a single-interrupt system, the response time is always more than 3 cycles and less than 9 cycles.

SINGLE-STEP OPERATION

The 8051 interrupt structure allows single-step execution with very little software overhead. As previously noted, an interrupt request will not be responded to while an interrupt of equal priority level is still in progress, nor will it be responded to after RETI until at least one other instruction has been executed. Thus, once an interrupt routine has been entered, it cannot be re-entered until at least one instruction of the interrupted program is executed. One way to use this feature for single-stop operation is to program one of the external interrupts (say, $\overline{INT0}$) to be level-activated. The service routine for the interrupt will terminate with the following code:

```
JNB   P3.2,$  ;Wait Here Till INT0 Goes High
JB    P3.2,$  ;Now Wait Here Till it Goes Low
RETI          :Go Back and Execute One Instruction
```

Now if the $\overline{INT0}$ pin, which is also the P3.2 pin, is held normally low, the CPU will go right into the External Interrupt 0 routine and stay there until $\overline{INT0}$ is pulsed (from low to high to low). Then it will execute RETI, go back to the task program, execute one instruction, and immediately re-enter the External Interrupt 0 routine to await the next pulsing of P3.2. One step of the task program is executed each time P3.2 is pulsed.

RESET

The reset input is the RST pin, which is the input to a Schmitt Trigger.

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), *while the oscillator is running.* The CPU responds by generating an internal reset, with the timing shown in Figure 25.

The external reset signal is asynchronous to the internal clock. The RST pin is sampled during State 5 Phase 2 of every machine cycle. The port pins will maintain their current activities for 19 oscillator periods after a logic 1 has been sampled at the RST pin; that is, for 19 to 31 oscillator periods after the external reset signal has been applied to the RST pin.

While the RST pin is high, ALE and PSEN are weakly pulled high. After RST is pulled low, it will take 1 to 2 machine cycles for ALE and PSEN to start clocking. For this reason, other devices can not be synchronized to the internal timings of the 8051.

Driving the ALE and $\overline{PSEN}$ pins to 0 while reset is active could cause the device to go into an indeterminate state.

The internal reset algorithm writes 0s to all the SFRs except the port latches, the Stack Pointer, and SBUF. The port latches are initialized to FFH, the Stack Pointer to 07H, and SBUF is indeterminate. Table 3 lists the SFRs and their reset values.

The internal RAM is not affected by reset. On power up the RAM content is indeterminate.

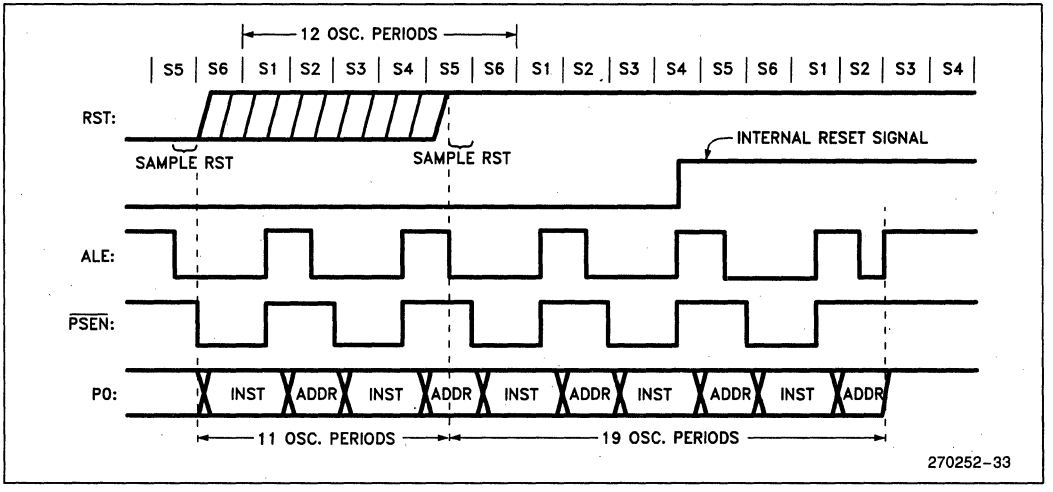


Figure 25. Reset Timing

Table 3. Reset Values of the SFRs

SFR Name	Reset Value
PC	0000H
ACC	00H
B	00H
PSW	00H
SP	07H
DPTR	0000H
P0–P3	FFH
IP (8051)	XXX00000B
IP (8052)	XX000000B
IE (8051)	0XX00000B
IE (8052)	0X000000B
TMOD	00H
TCON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
TH2 (8052)	00H
TL2 (8052)	00H
RCAP2H (8052)	00H
RCAP2L (8052)	00H
SCON	00H
SBUF	Indeterminate
PCON (HMOS)	0XXXXXXXB
PCON (CHMOS)	0XXX0000B

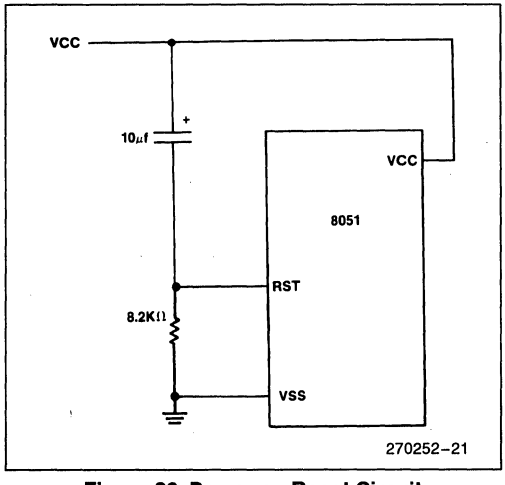


Figure 26. Power on Reset Circuit

POWER-ON RESET

For HMOS devices when V_{CC} is turned on an automatic reset can be obtained by connecting the RST pin to V_{CC} through a 10 μF capacitor and to V_{SS} through an 8.2 KΩ resistor (Figure 26). The CHMOS devices do not require this resistor although its presence does no harm. In fact, for CHMOS devices the external resistor can be removed because they have an internal pulldown on the RST pin. The capacitor value could then be reduced to 1 μF.

When power is turned on, the circuit holds the RST pin high for an amount of time that depends on the capacitor value and the rate at which it charges. To ensure a valid reset the RST pin must be held high long enough to allow the oscillator to start up plus two machine cycles.

On power up, V_{CC} should rise within approximately ten milliseconds. The oscillator start-up time will depend on the oscillator frequency. For a 10 MHz crystal, the start-up time is typically 1 ms. For a 1 MHz crystal, the start-up time is typically 10 ms.

With the given circuit, reducing V_{CC} quickly to 0 causes the RST pin voltage to momentarily fall below 0V. However, this voltage is internally limited and will not harm the device.

NOTE:
The port pins will be in a random state until the oscillator has started and the internal reset algorithm has written 1s to them.

Powering up the device without a valid reset could cause the CPU to start executing instructions from an indeterminate location. This is because the SFRs, specifically the Program Counter, may not get properly initialized.

7

POWER-SAVING MODES OF OPERATION

For applications where power consumption is critical the CHMOS version provides power reduced modes of operation as a standard feature. The power down mode in HMOS devices is no longer a standard feature and is being phased out.

CHMOS Power Reduction Modes

CHMOS versions have two power-reducing modes, Idle and Power Down. The input through which back-up power is supplied during these operations is VCC. Figure 27 shows the internal circuitry which implements these features. In the Idle mode (IDL = 1), the oscillator continues to run and the Interrupt, Serial Port, and Timer blocks continue to be clocked, but the

clock signal is gated off to the CPU. In Power Down (PD = 1), the oscillator is frozen. The Idle and Power Down modes are activated by setting bits in Special Function Register PCON. The address of this register is 87H. Figure 28 details its contents.

In the HMOS devices the PCON register only contains SMOD. The other four bits are implemented only in the CHMOS devices. User software should never write 1s to unimplemented bits, since they may be used in future MCS-51 products.

IDLE MODE

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the Interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and $\overline{PSEN}$ hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into Idle.

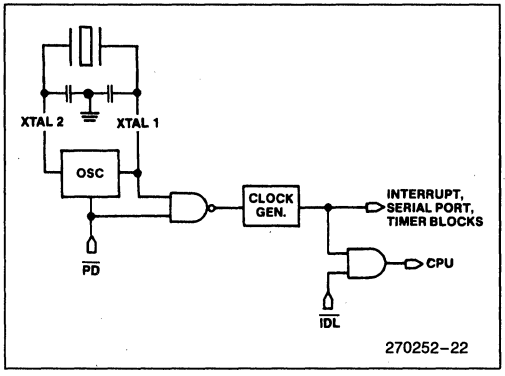


Figure 27. Idle and Power Down Hardware

(MSB)							(LSB)
SMOD	-	-	-	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1 and Timer 1 is used to generate baud rate, and the Serial Port is used in modes 1, 2, or 3.
—	PCON.6	(Reserved)
—	PCON.5	(Reserved)
—	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XXX0000).
In the HMOS devices the PCON register only contains SMOD. The other four bits are implemented only in the CHMOS devices. User software should never write 1s to unimplemented bits, since they may be used in future MCS-51 products.

Figure 28. PCON: Power Control Register

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

The signal at the RST pin clears the IDL bit directly and asynchronously. At this time the CPU resumes program execution from where it left off; that is, at the instruction following the one that invoked the Idle Mode. As shown in Figure 25, two or three machine cycles of program execution may take place before the internal reset algorithm takes control. On-chip hardware inhibits access to the internal RAM during this time, but access to the port pins is not inhibited. To eliminate the possibility of unexpected outputs at the port pins, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external Data RAM.

POWER DOWN MODE

An instruction that sets PCON.1 causes that to be the last instruction executed before going into the Power Down mode. In the Power Down mode, the on-chip oscillator is stopped. With the clock frozen, all func-

Table 4. EPROM Versions of the 8051 and 8052

Device Name	EPROM Version	EPROM Bytes	Ckt Type	VPP	Time Required to Program Entire Array
8051AH	8751H/8751BH	4K	HMOS	21.0V/12.75V	4 minutes
80C51BH	87C51	4K	CHMOS	12.75V	13 seconds
8052AH	8752BH	8K	HMOS	12.75V	26 seconds

tions are stopped, but the on-chip RAM and Special Function Registers are held. The port pins output the values held by their respective SFRs. ALE and $\overline{PSEN}$ output lows.

The only exit from Power Down for the 80C51 is a hardware reset. Reset redefines all the SFRs, but does not change the on-chip RAM.

In the Power Down mode of operation, VCC can be reduced to as low as 2V. Care must be taken, however, to ensure that VCC is not reduced before the Power Down mode is invoked, and that VCC is restored to its normal operating level, before the Power Down mode is terminated. The reset that terminates Power Down also frees the oscillator. The reset should not be activated before VCC is restored to its normal operating level, and must be held active long enough to allow the oscillator to restart and stabilize (normally less than 10 msec).

EPROM VERSIONS

The EPROM versions of these devices are listed in Table 4. The 8751H programs at VPP = 21V using one 50 msec $\overline{PROG}$ pulse per byte programmed. This results in a total programming time (4K bytes) of approximately 4 minutes.

The 8751BH, 8752BH and 87C51 use the faster "Quick-Pulse" programming™ algorithm. These devices program at $\overline{VPP}$ = 12.75V using a series of twenty-five 100 μs $\overline{PROG}$ pulses per byte programmed. This results in a total programming time of approximately 26 seconds for the 8752BH (8 Kbytes) and 13 seconds for the 87C51 (4 Kbytes).

Detailed procedures for programming and verifying each device are given in the data sheets.

Exposure to Light

It is good practice to cover the EPROM window with an opaque label when the device is in operation. This is not so much to protect the EPROM array from inadvertent erasure, but to protect the RAM and other on-chip logic. Allowing light to impinge on the silicon die while the device is operating can cause logical malfunction.

Program Memory Locks

In some microcontroller applications it is desirable that the Program Memory be secure from software piracy. Intel has responded to this need by implementing a Program Memory locking scheme in some of the MCS-51 devices. While it is impossible for anyone to guarantee absolute security against all levels of technological sophistication, the Program Memory locks in the MCS-51 devices will present a substantial barrier against illegal readout of protected software.

One Lock Bit Scheme on 8751H

The 8751H contains a lock bit which, once programmed, denies electrical access by any external means to the on-chip Program Memory. The effect of this lock bit is that while it is programmed the internal Program Memory can not be read out, the device can not be further programmed, and it *can not execute external Program Memory.* Erasing the EPROM array deactivates the lock bit and restores the device's full functionality. It can then be re-programmed.

The procedure for programming the lock bit is detailed in the 8751H data sheet.

Two Program Memory Lock Schemes

The 8751BH, 8752BH and 87C51 contain two Program Memory locking schemes: Encrypted Verify and Lock Bits.

Encryption Array: Within the EPROM is an array of encryption bytes that are initially unprogrammed (all 1's). The user can program the array to encrypt the code bytes during EPROM verification. The verification procedure sequentially XNORs each code byte with one of the key bytes. When the last key byte in the array is reached, the verify routine starts over with the first byte of the array for the next code byte. If the key bytes are unprogrammed, the XNOR process leaves the code byte unchanged. With the key bytes programmed, the code bytes are encrypted and can be read correctly only if the key bytes are known in their proper order. Table 6 lists the number of encryption bytes available on the various products.

When using the encryption array, one important factor should be considered. If a code byte has the value

0FFH, verifying the byte will produce the encryption byte value. If a large block of code is left unprogrammed, a verification routine will display the encryption array contents. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits: Also included in the Program Lock scheme are Lock Bits which can be enabled to provide varying degrees of protection. Table 5 lists the Lock Bits and their corresponding effect on the microcontroller. Refer to Table 6 for the Lock Bits available on the various products.

Erasing the EPROM also erases the Encryption Array and the Lock Bits, returning the part to full functionality.

Table 5. Program Lock Bits and their Features

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. (Code verify will still be encrypted by the encryption array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

P-Programmed
U-Unprogrammed

Any other combination of the Lock Bits is not defined.

Table 6. Program Protection

Device	Lock Bits	Encrypt Array
8751BH	LB1, LB2	32 Bytes
8752BH	LB1, LB2	32 Bytes
87C51	LB1, LB2, LB3	64 Bytes

When Lock Bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ROM PROTECTION

The 8051AHP and 80C51BHP are ROM Protected versions of the 8051AH and 80C51BH, respectively. To incorporate this Protection Feature, program verification has been disabled and external memory accesses have been limited to 4K. Refer to the data sheets on these parts for more information.

ONCE™ Mode

The ONCE ("on-circuit emulation") mode facilitates testing and debugging of systems using the device without the device having to be removed from the circuit. The ONCE mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored after a normal reset is applied.

THE ON-CHIP OSCILLATORS

HMOS Versions

The on-chip oscillator circuitry for the HMOS (HMOS-I and HMOS-II) members of the MCS-51 family is a single stage linear inverter (Figure 29), intended for use as a crystal-controlled, positive reactance oscillator (Figure 30). In this application the crystal is operated in its fundamental response mode as an inductive reactance in parallel resonance with capacitance external to the crystal.

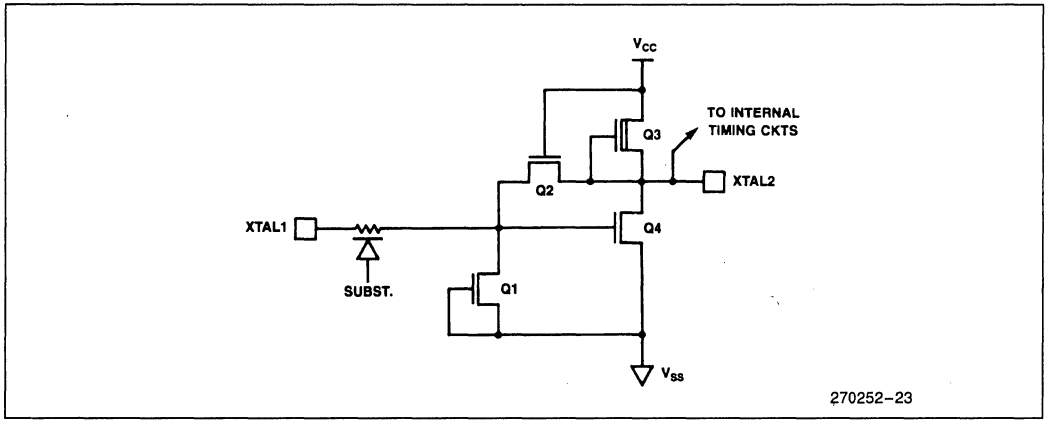


Figure 29. On-Chip Oscillator Circuitry in the HMOS Versions of the MCS®-51 Family

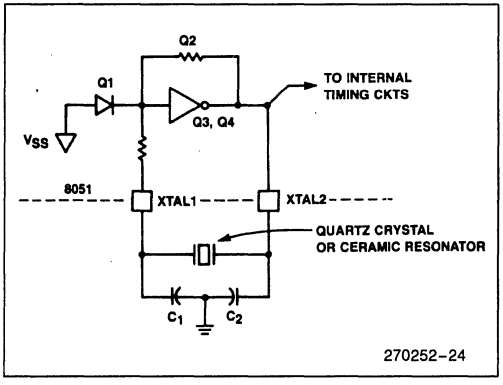


Figure 30. Using the HMOS On-Chip Oscillator

The crystal specifications and capacitance values (C1 and C2 in Figure 30) are not critical. 30 pF can be used in these positions at any frequency with good quality crystals. A ceramic resonator can be used in place of the crystal in cost-sensitive applications. When a ceramic resonator is used, C1 and C2 are normally selected to be of somewhat higher values, typically, 47 pF. The manufacturer of the ceramic resonator should be consulted for recommendations on the values of these capacitors.

In general, crystals used with these devices typically have the following specifications:

ESR (Equivalent Series Resistance)	see Figure 31
C_O (Shunt Capacitance)	7.0 pF max.
C_L (Load Capacitance)	30 pF ±3 pF
Drive Level	1 mW

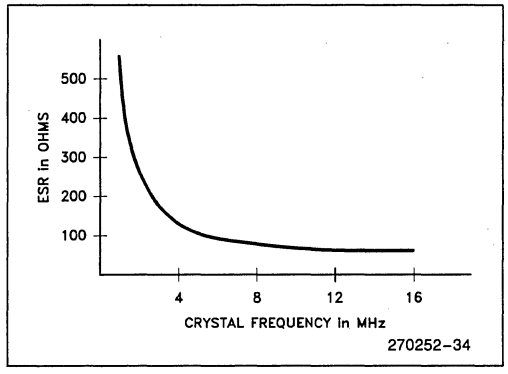


Figure 31. ESR vs Frequency

Frequency, tolerance and temperature range are determined by the system requirements.

A more in-depth discussion of crystal specifications, ceramic resonators, and the selection of values for C1 and C2 can be found in Application Note AP-155, "Oscillators for Microcontrollers," which is included in the *Embedded Applications Handbook*.

To drive the HMOS parts with an external clock source, apply the external clock signal to XTAL2, and ground XTAL1, as shown in Figure 32. A pullup resistor may be used (to increase noise margin), but is optional if VOH of the driving gate exceeds the VIH MIN specification of XTAL2.

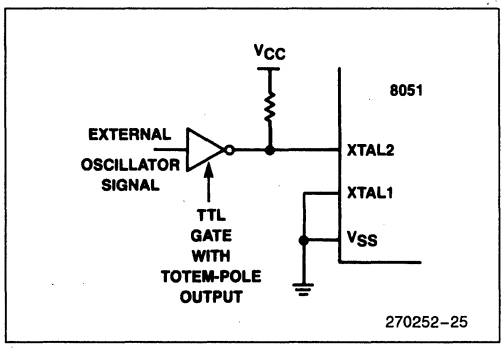


Figure 32. Driving the HMOS MCS®-51 Parts with an External Clock Source

CHMOS Versions

The on-chip oscillator circuitry for the 80C51BH, shown in Figure 33, consists of a single stage linear inverter intended for use as a crystal-controlled, positive reactance oscillator in the same manner as the HMOS parts. However, there are some important differences.

One difference is that the 80C51BH is able to turn off its oscillator under software control (by writing a 1 to the PD bit in PCON). Another difference is that in the 80C51BH the internal clocking circuitry is driven by the signal at XTAL1, whereas in the HMOS versions it is by the signal at XTAL2.

The feedback resistor R_f in Figure 33 consists of paralleled n- and p- channel FETs controlled by the PD bit, such that R_f is opened when PD = 1. The diodes D1 and D2, which act as clamps to VCC and VSS, are parasitic to the R_f FETs.

The oscillator can be used with the same external components as the HMOS versions, as shown in Figure 34. Typically, C1 = C2 = 30 pF when the feedback element is a quartz crystal, and C1 = C2 = 47 pF when a ceramic resonator is used.

To drive the CHMOS parts with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 float, as shown in Figure 35.

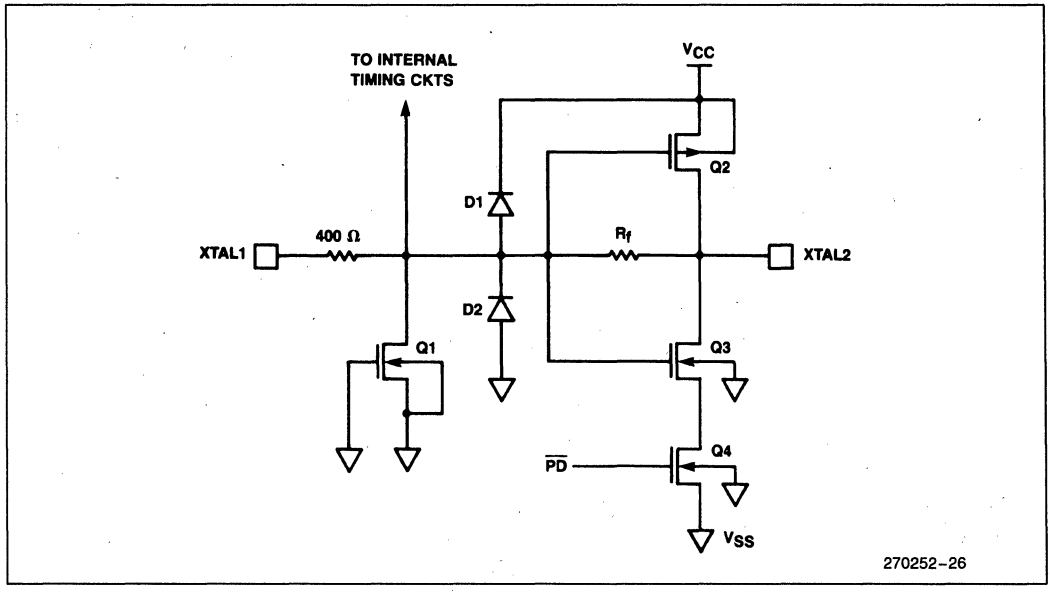


Figure 33. On-Chip Oscillator Circuitry in the CHMOS Versions of the MCS®-51 Family

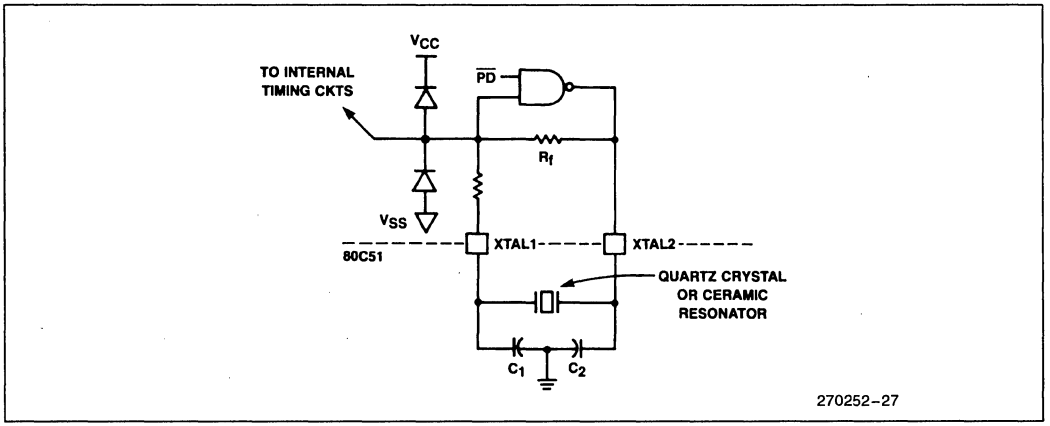


Figure 34. Using the CHMOS On-Chip Oscillator

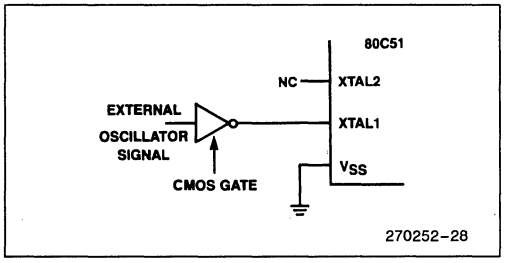


Figure 35. Driving the CHMOS MCS®-51 Parts with an External Clock Source

The reason for this change from the way the HMOS part is driven can be seen by comparing Figures 29 and 33. In the HMOS devices the internal timing circuits are driven by the signal at XTAL2. In the CHMOS devices the internal timing circuits are driven by the signal at XTAL1.

INTERNAL TIMING

Figures 36 through 39 show when the various strobe and port signals are clocked internally. The figures do not show rise and fall times of the signals, nor do they show propagation delays between the XTAL signal and events at other pins.

Rise and fall times are dependent on the external loading that each pin must drive. They are often taken to be something in the neighborhood of 10 nsec, measured between 0.8V and 2.0V.

Propagation delays are different for different pins. For a given pin they vary with pin loading, temperature, VCC, and manufacturing lot. If the XTAL waveform is taken as the timing reference, prop delays may vary from 25 to 125 nsec.

The AC Timings section of the data sheets do not reference any timing to the XTAL waveform. Rather, they relate the critical edges of control and input signals to each other. The timings published in the data sheets include the effects of propagation delays under the specified test conditions.

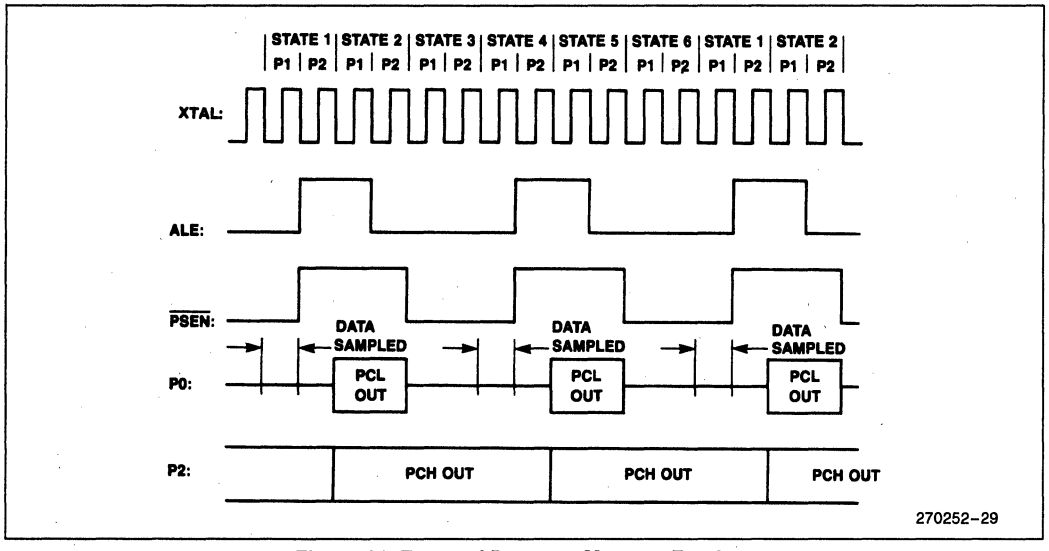


Figure 36. External Program Memory Fetches

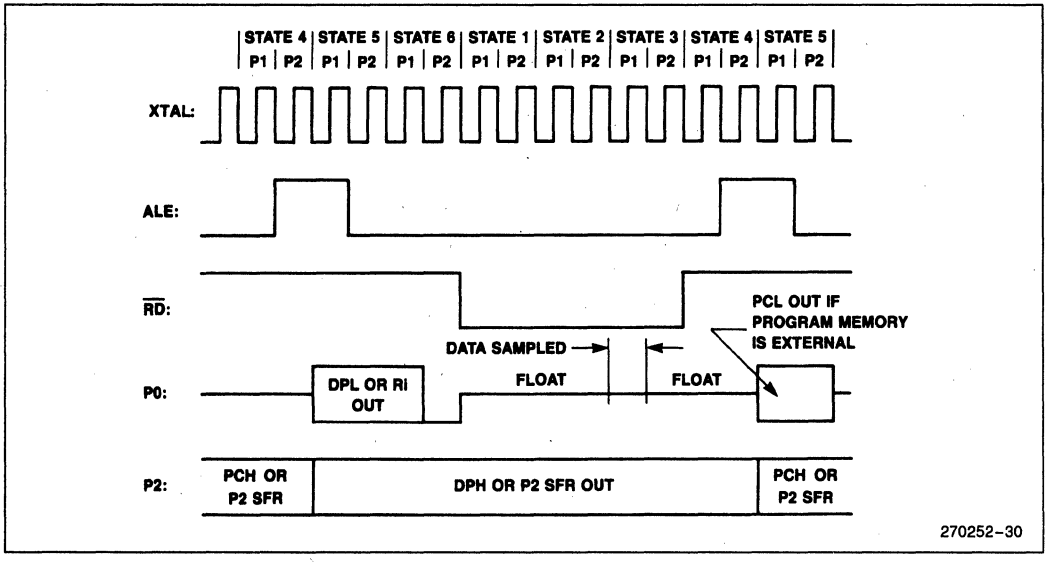


Figure 37. External Data Memory Read Cycle

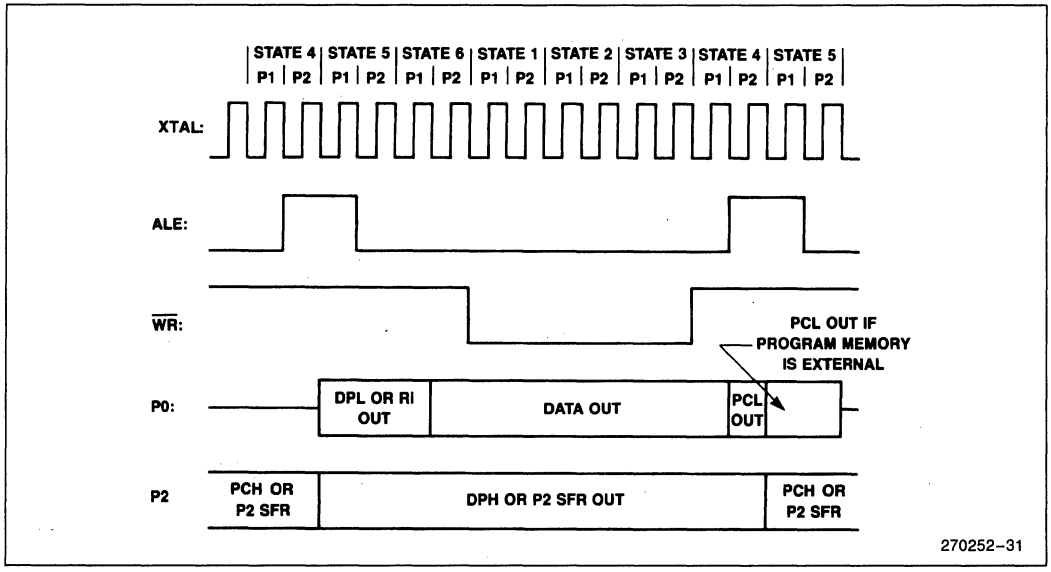


Figure 38. External Data Memory Write Cycle

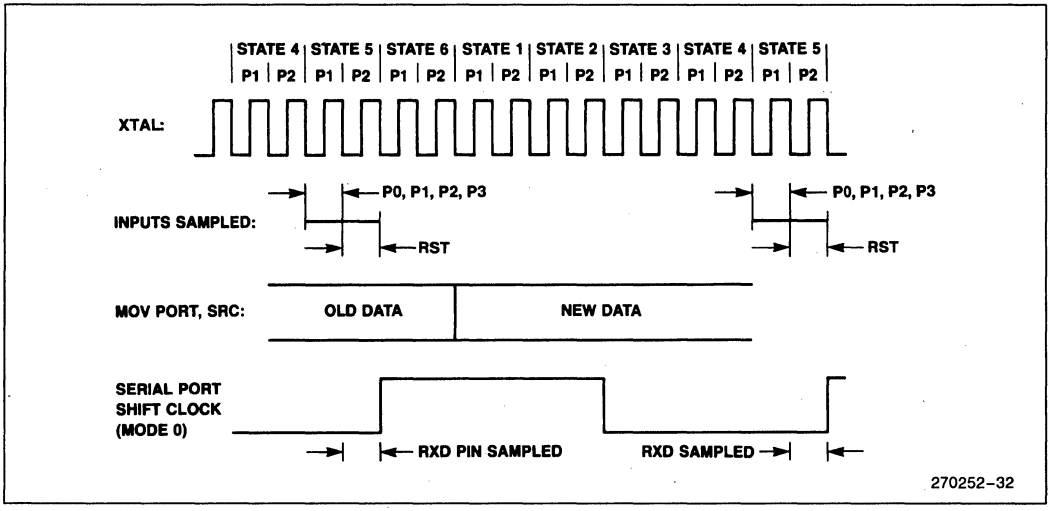


Figure 39. Port Operation

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ADDITIONAL REFERENCES

The following application notes and articles are found in the *Embedded Applications* handbook. (Order Number: 270648)

1. AP-125 "Designing Microcontroller Systems for Electrically Noisy Environments".
2. AP-155 "Oscillators for Microcontrollers".
3. AP-252 "Designing with the 80C51BH".
4. AR-517 "Using the 8051 Microcontroller with Resonant Transducers".

8XC52/54/58 HARDWARE DESCRIPTION

INTRODUCTION

The 8XC52/54/58 is a highly integrated 8-bit microcontroller based on the MCS®-51 architecture. The key features are an enhanced serial port for multi-processor communications and an up/down timer/counter. As this product is CHMOS, it has two software selectable reduced power modes: Idle Mode and Power Down Mode. Being a member of the MCS-51 family, the 8XC52/54/58 is optimized for control applications.

This document presents a comprehensive description of the on-chip hardware features of the 8XC52/54/58 as they differ from the 80C51BH. It begins by describing how the I/O functions are different and then discusses each of the peripherals as follows:

- 256 Bytes On-Chip RAM
- Special Function Registers (SFR)
- Timer 2
  - — Capture Timer/Counter
  - — Up/Down Timer/Counter
  - — Baud Rate Generator
- Full-Duplex Programmable Serial Interface with
  - — Framing Error Detection
  - — Automatic Address Recognition
- 6 Interrupt Sources
- Enhanced Power Down Mode
- Power Off Flag
- ONCE Mode

The 8XC52/54/58 uses the standard 8051 instruction set and is pin-for-pin compatible with the existing MCS-51 family of products. Table 1 summarizes the product names and memory differences of the various 8XC52/54/58 products currently available. Throughout this document, the products will generally be referred to as the 8XC5X.

Table 1. 8XC52/54/58 Microcontrollers

ROM Device	EPROM Version	ROMless Version	ROM/EPROM Bytes	RAM Bytes
80C52	87C52	80C32	8K	256
80C54	87C54	80C32	16K	256
80C58	87C58	80C32	32K	256

For a description of the features that are the same as the 80C51, the reader should refer to the MCS-51 Architectural Overview, MCS-51 Programmers Guide/ Instruction Set, and the Hardware Description of the 80C51 in the Embedded Microcontrollers and Processors Handbook (Order #270645).

PIN DESCRIPTION

The 8XC5X pin-out is the same as the 80C51. The only difference is the alternate function of pins P1.0 and P1.1. P1.0 is the external clock input for Timer 2. P1.1 is the Reload/Capture/Direction Control for Timer 2.

DATA MEMORY

The 8XC5X implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. That means they have the same addresses, but they are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of RAM or the SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example,

MOV 0A0H, #data (Direct Addressing)

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the upper 128 bytes of RAM. For example,

MOV @R0, #data (Indirect Addressing)

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H). Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

SPECIAL FUNCTION REGISTERS

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 2.

Note that not all of the addresses are occupied. Unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future MCS-51 products to invoke new features. In that case the reset or inactive values of the new bits will always be 0.

Table 2. 8XC5X SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP X0000000	SADEN 00000000							0BFH
0B0H	P3 11111111							IPH X0000000	0B7H
0A8H	IE 00000000	SADDR 00000000							0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00000000	87H

Timer Registers—Control and status bits are contained in registers T2CON and T2MOD for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Serial Port Registers—Registers SADDR and SADEN are used to define the Given and the Broadcast addresses for the Automatic Address Recognition feature.

Interrupt Registers—The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the 6 interrupt sources in the IP register. The IPH register allows four priorities.

TIMER 2

Timer 2 is a 16-bit Timer/Counter which can operate either as a timer or an event counter. This is selectable by bit C/$\overline{T2}$ in the SFR T2CON (Table 3). It has three

operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON as shown in Table 4.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is $1/12$ of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is $1/24$ of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Table 3. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CP/$\overline{T2}$	CP/$\overline{RL2}$
7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

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Table 4. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-Bit Auto-Reload
0	1	1	16-Bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

CAPTURE MODE

In the capture mode there are two options selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

AUTO-RELOAD (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by a bit named DCEN (Down Counter Enable) located in the SFR T2MOD (see Table 5). Upon reset the DCEN bit is set to 0 so that Timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode there are two options selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

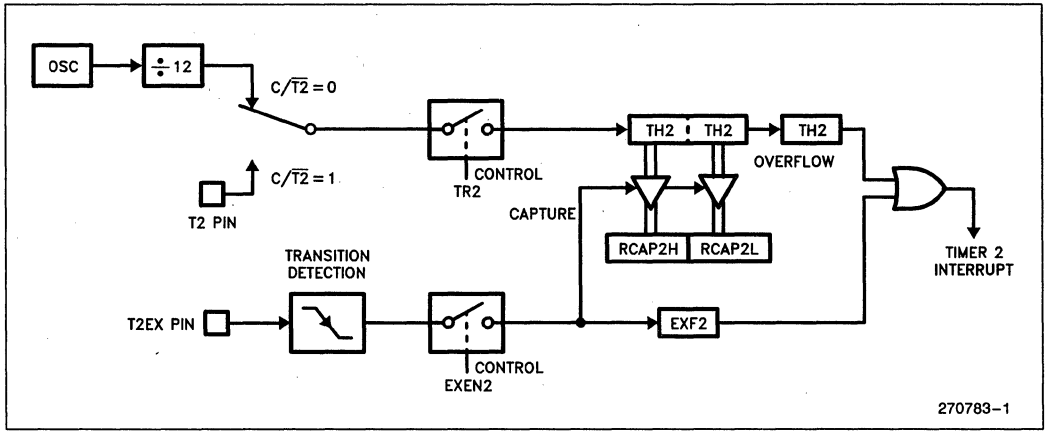

Figure 1. Timer 2 in Capture Mode

Table 5. T2MOD—Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

—	—	—	—	—	—	T20E	DCEN
7	6	5	4	3	2	1	0

Bit

Symbol	Function
—	Not implemented, reserved for future use.
T20E	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

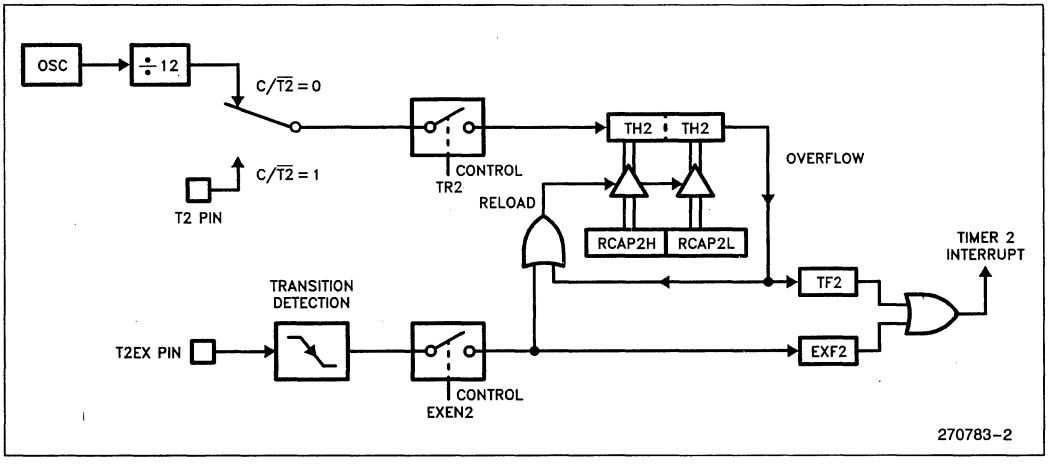

Figure 2. Timer 2 Auto Reload Mode (DCEN = 0)

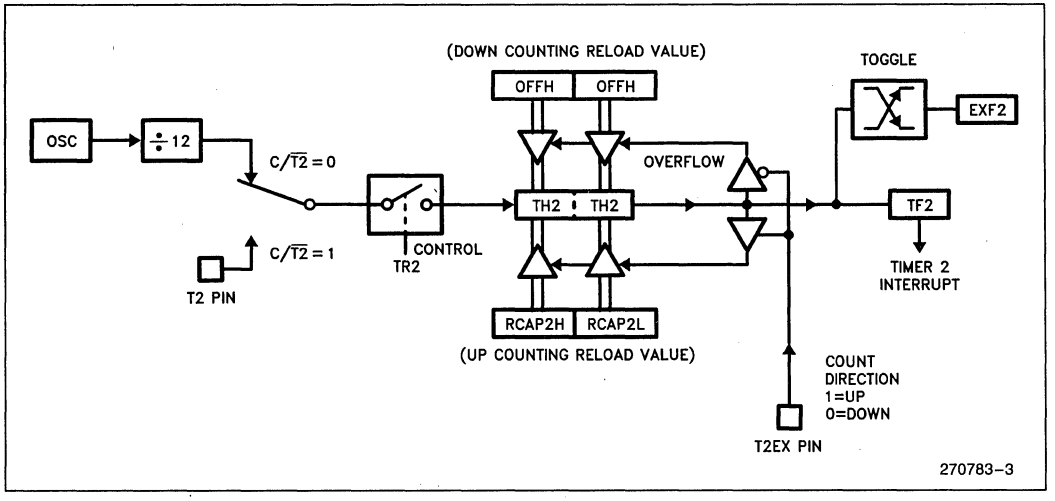

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

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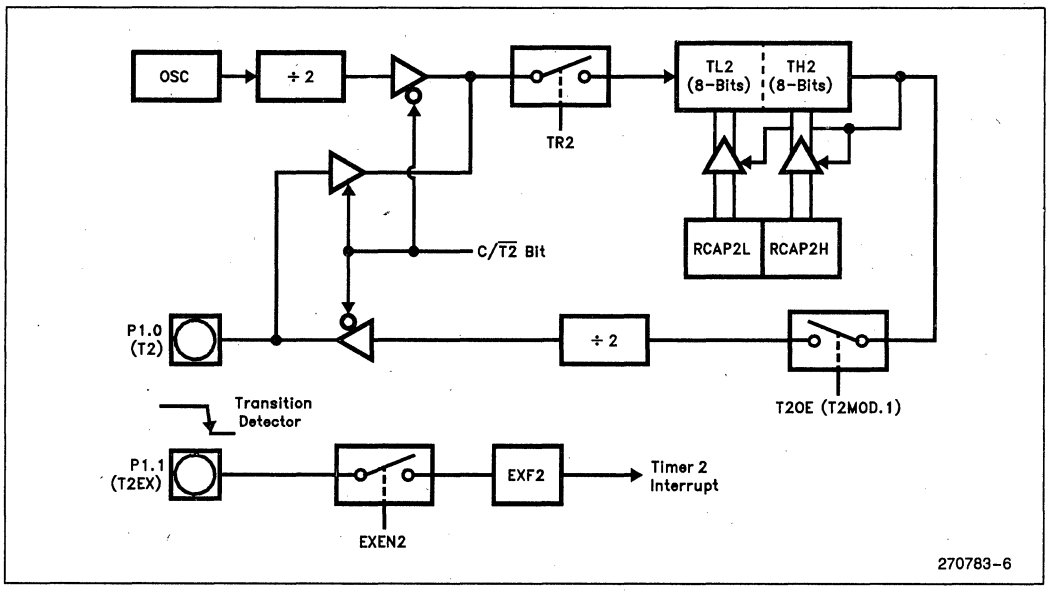


Figure 4. Timer 2 in Clock-Out Mode

Setting the DCEN bit enables Timer 2 to count up or down as shown in Figure 3. In this mode the T2EX pin controls the direction of count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. Now the timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows. This bit can be used as a 17th bit of resolution if desired. In this operating mode, EXF2 does not flag an interrupt.

BAUD RATE GENERATOR

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 3). Note that the baud rates for transmit and receive can be different. This is accomplished by using Timer 2 for the receiver or transmitter and using Timer 1 for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 5.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either "timer" or "counter" operation. In most applications, it is configured for "timer" operation ($C/\overline{T2} = 0$). The "timer" operation is different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer, it increments every machine cycle (thus at $1/12$ the oscillator frequency). As a baud rate generator, however, it increments every state time (thus at $1/2$ the oscillator frequency). The baud rate formula is given below:

$$\text{Modes 1 and 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 5. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the Timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read, but shouldn't be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

PROGRAMMABLE CLOCK OUT

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed (1) to input the external clock for Timer/Counter 2 or (2) to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, TCAP2L) as shown in this equation:

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies can not be determined independently from one another since they both use RCAP2H and RCAP2L.

UART

The UART in the 8XC5X operates identically to the UART in the 80C51 except for the following enhancements. For a complete understanding of the 8XC5X UART please refer to the description in the 80C51 Hardware Description chapter in the Embedded Microcontrollers and Processors Handbook.

Framing Error Detection—Framing Error Detection allows the serial port to check for valid stop bits in modes 1, 2 or 3. A missing stop bit can be caused, for example, by noise on the serial lines, or transmission by two CPUs simultaneously.

If a stop bit is missing a Framing Error bit (FE) is set. The FE bit can be checked in software after each reception to detect communication errors. Once set, the FE bit must be cleared in software. A valid stop bit will not clear FE.

The FE bit is located in SCON and shares the same bit address as SM0. Control bit SMOD0 in the PCON register (location PCON.6) determines whether the SM0 or FE bit is accessed. If SMOD0 = 0, then accesses to SCON.7 are to SM0. If SMOD0 = 1, then accesses to SCON.7 are to FE.

Automatic Address Recognition—Automatic Address Recognition reduces the CPU time required to service the serial port. Since the CPU is only interrupted when it receives its own address, the software overhead to compare addresses is eliminated. With this feature enabled in one of the 9-bit modes, the Receive Interrupt (RI) flag will only get set when the received byte corresponds to either a Given or Broadcast address.

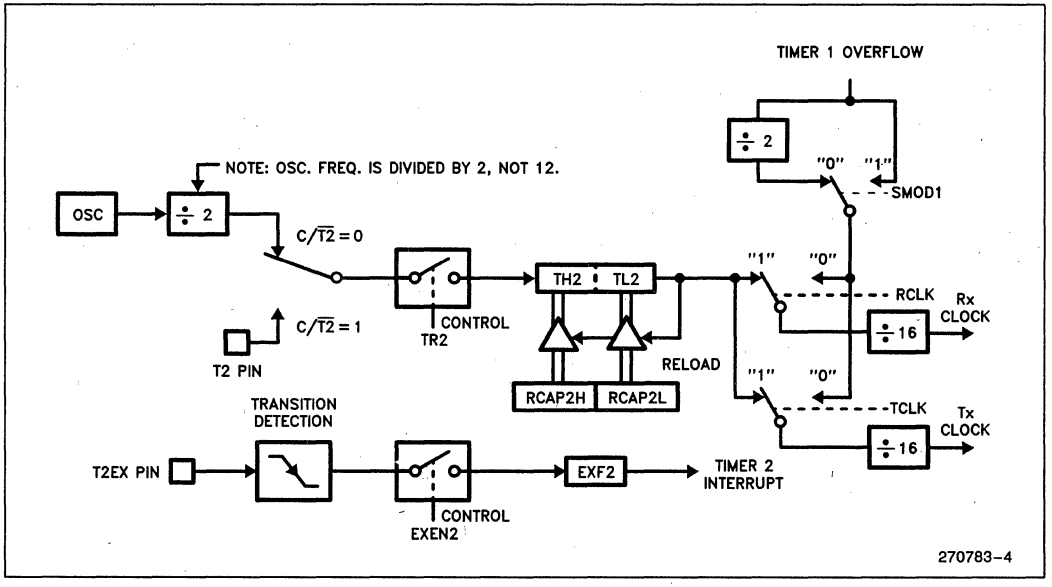


Figure 5. Timer 2 In Baud Rate Generator Mode

A way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. Remember, an address byte has its 9th bit set to 1, whereas a data byte has its 9th bit set to 0. All the slave processors should have their SM2 bits set to 1 so they will only be interrupted by an address byte. The Automatic Address Recognition feature allows only the addressed slave to be interrupted. In this mode, the address comparison occurs in hardware, not software. (On the 80C51 serial port, an address byte interrupts all slaves for an address comparison).

The addressed slave then clears its SM2 bit and prepares to receive the data bytes that will be coming. The other slaves are unaffected by these data bytes as they are still waiting to receive an address byte.

The feature works the same way in the 8-bit mode (Mode 1) as in the 9-bit modes, except that the stop bit takes the place of the 9th data bit. If SM2 is set, the RI flag is set only if the received byte matches the Given or Broadcast Address and is terminated by a valid stop bit. Setting the SM2 bit has no effect on Mode 0.

The master can selectively communicate with groups of slaves by using the Given Address. Addressing all slaves at once is possible with the Broadcast Address. These addresses are defined for each slave by two Special Function Registers: SADDR and SADEN.

A slave's individual address is specified in SADDR. SADEN is a mask byte that defines don't-care bits to form the Given Address. These don't-cares allow flexibility in the user-defined protocol to address one or more slaves at a time. The following is an example of how the user could define Given Addresses to selectively address different slaves.

Slave 1:

SADDR	=	1111 0001
SADEN	=	1111 1010
GIVEN	=	1111 0X0X

Slave 2:

SADDR	=	1111 0011
SADEN	=	1111 1001
GIVEN	=	1111 0XX1

The SADEN bits are selected such that each slave can be addressed separately. Notice that bit 0 (LSB) is a don't-care for Slave 1's Given Address, but bit 0 = 1 for Slave 2. Thus, to selectively communicate with just Slave 1 the master must send an address with bit 0 = 0 (e.g., 1111 0000).

Similarly, bit 1 = 0 for Slave 1, but is a don't-care for Slave 2. Now to communicate with just Slave 2 an address with bit 1 = 1 must be used (e.g., 1111 0111).

Finally, for a master to communicate with both slaves at once the address must have bit 0 = 1 and bit 1 = 0. Notice, however, that bit 2 is a don't-care for both slaves. This allows two different addresses to select both slaves (1111 0001 or 1111 0101). If a third slave was added that required its bit 2 = 0, then the latter address could be used to communicate with Slave 1 and 2 but not Slave 3.

The master can also communicate with all slaves at once with the Broadcast Address. It is formed from the logical OR of the SADDR and SADEN registers with zeroes defined as don't-cares. The don't-cares also allow flexibility in defining the Broadcast Address, but in most applications a Broadcast Address will be 0FFH.

SADDR and SADEN are located at address 0A9H and 0B9H, respectively. On reset, the SADDR and SADEN registers are initialized to 00H which defines the Given and Broadcast Addresses as XXXX XXXX (all don't-cares). This assures the 8XC5X serial port to be backwards compatible with other MCS®-51 products which do not implement automatic address recognition.

INTERRUPTS

The 8XC5X has a total of 6 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1 and 2) and the serial port interrupt. These interrupts are all shown in Figure 6.

Timer 2 Interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2 is set at S2P2 and is polled in the same cycle in which the timer overflows.

Interrupt Priority Structure

A second Interrupt Priority register (IPH) has been added, increasing the number of priority levels to four. Table 6 shows this second register. The added register becomes the MSB of the priority select bits and the existing IP register acts as the LSB. This scheme maintains compatibility with the rest of the MCS-51 family. Table 7 shows the bit values and priority levels associated with each combination.

Table 6. IPH: Interrupt Priority High Register

IPH Address = 0B7H — Reset Value = X000 0000

—	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit 7	6	5	4	3	2	1	0

Symbol	Function
—	Not Implemented, reserved for future use.
PPCH	PCA interrupt priority high bit.
PT2H	Timer 2 interrupt priority high bit.
PSH	Serial Port interrupt priority high bit.
PT1H	Timer 1 interrupt priority high bit.
PX1H	External interrupt 1 priority high bit.
PT0H	Timer 0 interrupt priority high bit.
PX0H	External interrupt priority high bit.

Table 7. Priority Level Bit Values

Priority Bits		Interrupt Priority Level
IPH.x	IP.x	
0	0	Level 0 (Lowest)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (Highest)

POWER DOWN MODE

The 8XC5X can exit Power Down with either a hardware reset or external interrupt. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs (except PD in PCON) and the on-chip RAM to retain their values.

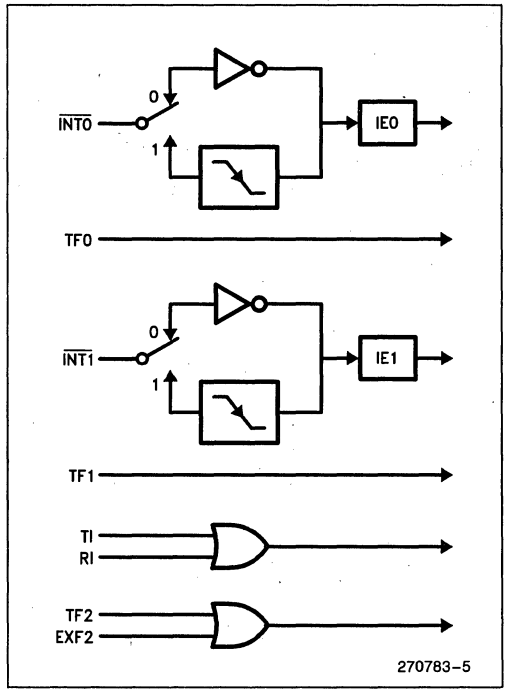


Figure 6. Interrupt Sources

To properly terminate Power Down the reset or external interrupt should not be applied before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 msec).

With an external interrupt, $\overline{INT0}$ or $\overline{INT1}$ must be enabled and configured as level-sensitive before entering Power Down. Holding the pin low restarts the oscillator and bringing the pin back high completes the exit. After the RETI instruction is executed in the interrupt service routine, the next instruction will be the one following the instruction that put the device in Power Down.

POWER OFF FLAG

The Power Off Flag (POF) located at PCON.4 is set by hardware when V_{CC} rises from 0 to approximately 5V. POF can also be set or cleared by software. This allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is one that is coincident with V_{CC} being turned on to the device after it was turned off. A warm start reset occurs while V_{CC} is still applied to the device and could be generated, for example, by an exit from Power Down.

Immediately after reset, the user's software can check the status of the POF bit. POF = 1 would indicate a cold start. The software then clears POF and commences its tasks. POF = 0 immediately after reset would indicate a warm start.

V_{CC} must remain above 3V for POF to retain a 0.

Program Memory Lock

In some microcontroller applications it is desirable that the Program Memory be secure from software piracy. The 8XC5X has varying degrees of program protection depending on the device. Table 8 outlines the lock schemes available for each device.

Encryption Array: Within the EPROM/ROM is an array of encryption bytes that are initially unprogrammed (all 1's). For EPROM devices, the user can program the encryption array to encrypt the program code bytes during EPROM verification. For ROM devices, the user submits the encryption array to be programmed by the factory. If an encryption array is submitted, LB1 will also be programmed by the factory. The encryption array is not available without the Lock Bit. Program code verification is performed as usual except that each code byte comes out exclusive-NOR'ed (XNOR) with one of the key bytes. Therefore, to read the ROM/EPROM code, the user has to know the encryption key bytes in their proper sequence.

Unprogrammed bytes have the value 0FFH. If the Encryption Array is left unprogrammed, all the key bytes have the value 0FFH. Since any code byte XNOR'ed

with 0FFH leaves the byte unchanged, leaving the Encryption Array unprogrammed in effect bypasses the encryption feature.

Program Lock Bits: Also included in the Program Lock scheme are Lock Bits which can be enabled to provide varying degrees of protection. Table 9 lists the Lock Bits and their corresponding influence on the microcontroller. Refer to Table 8 for the Lock Bits available on the various products. The user is responsible for programming the Lock Bits on EPROM devices. On ROM devices, LB1 is automatically set by the factory when the encryption array is submitted. The Lock Bit is not available without the encryption array on ROM devices.

Erasing the EPROM also erases the Encryption Array and the Lock Bits, returning the part to full functionality.

Table 8. Program Protection

Device	Lock Bits	Encrypt Array
80C52	LB1	64 Bytes
80C54	LB1	64 Bytes
80C58	LB1	64 Bytes
87C52	LB1, LB2, LB3	64 Bytes
87C54	LB1, LB2, LB3	64 Bytes
87C58	LB1, LB2, LB3	64 Bytes

ONCE MODE

The ON-Circuit Emulation (ONCE) mode facilitates testing and debugging of systems using the 8XC5X without having to remove the device from the circuit. The ONCE mode is invoked by either:

1. Pulling ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Holding ALE low as RESET is deactivated.

While the device is in ONCE mode, the Port 0 pins go into a float state, and the other port pins, ALE, and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit.

Normal operation is restored after a valid reset is applied.

ADDITIONAL REFERENCES

The following application notes provide supplemental information to this document and can be found in the *Embedded Applications* handbook (Order No. 270648).

1. AP-125 "Designing Microcontroller Systems for Electrically Noisy Environments"
2. AP-155 "Oscillators for Microcontrollers"
3. AP-252 "Designing with the 80C51BH"
4. AP-410 "Enhanced Serial Port on the 83C51FA"

Table 9. Lock Bits

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. (Code verify will still be encrypted by the encryption array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

P = Programmed
U = Unprogrammed
Any other combination of Lock Bits is not defined.

intel®

MCS®-51
8-BIT CONTROL-ORIENTED MICROCONTROLLERS
8031AH/8051AH
8032AH/8052AH
8751H/8751H-8

- **High Performance HMOS Process**
- **Internal Timers/Event Counters**
- **2-Level Interrupt Priority Structure**
- **32 I/O Lines (Four 8-Bit Ports)**
- **64K Program Memory Space**
- **Security Feature Protects EPROM Parts Against Software Piracy**
- **Boolean Processor**
- **Bit-Addressable RAM**
- **Programmable Full Duplex Serial Channel**
- **111 Instructions (64 Single-Cycle)**
- **64K Data Memory Space**

The MCS®-51 products are optimized for control applications. Byte-processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide instructions. Extensive on-chip support is provided for one-bit variables as a separate data type, allowing direct bit manipulation and testing in control and logic systems that require Boolean processing.

The 8751H is an EPROM version of the 8051AH. It has 4 Kbytes of electrically programmable ROM which can be erased with ultraviolet light. It is fully compatible with the 8051AH but incorporates one additional feature: a Program Memory Security bit that can be used to protect the EPROM against unauthorized readout. The 8751H-8 is identical to the 8751H but only operates up to 8 MHz.

The 8052AH is an enhanced version of the 8051AH. It is backwards compatible with the 8051AH and is fabricated with HMOS II technology. The 8052AH enhancements are listed in the table below. Also refer to this table for the ROM, ROMless and EPROM versions of each product.

Device	Internal Memory		Timers/ Event Counters	Interrupts
	Program	Data		
8052AH	8K x 8 ROM	256 x 8 RAM	3 x 16-Bit	6
8051AH	4K x 8 ROM	128 x 8 RAM	2 x 16-Bit	5
8032AH	none	256 x 8 RAM	3 x 16-Bit	6
8031AH	none	128 x 8 RAM	2 x 16-Bit	5
8751H	4K x 8 EPROM	128 x 8 RAM	2 x 16-Bit	5
8751H-8	4K x 8 EPROM	128 x 8 RAM	2 x 16-Bit	5

August 1992
Order Number: 270048-007

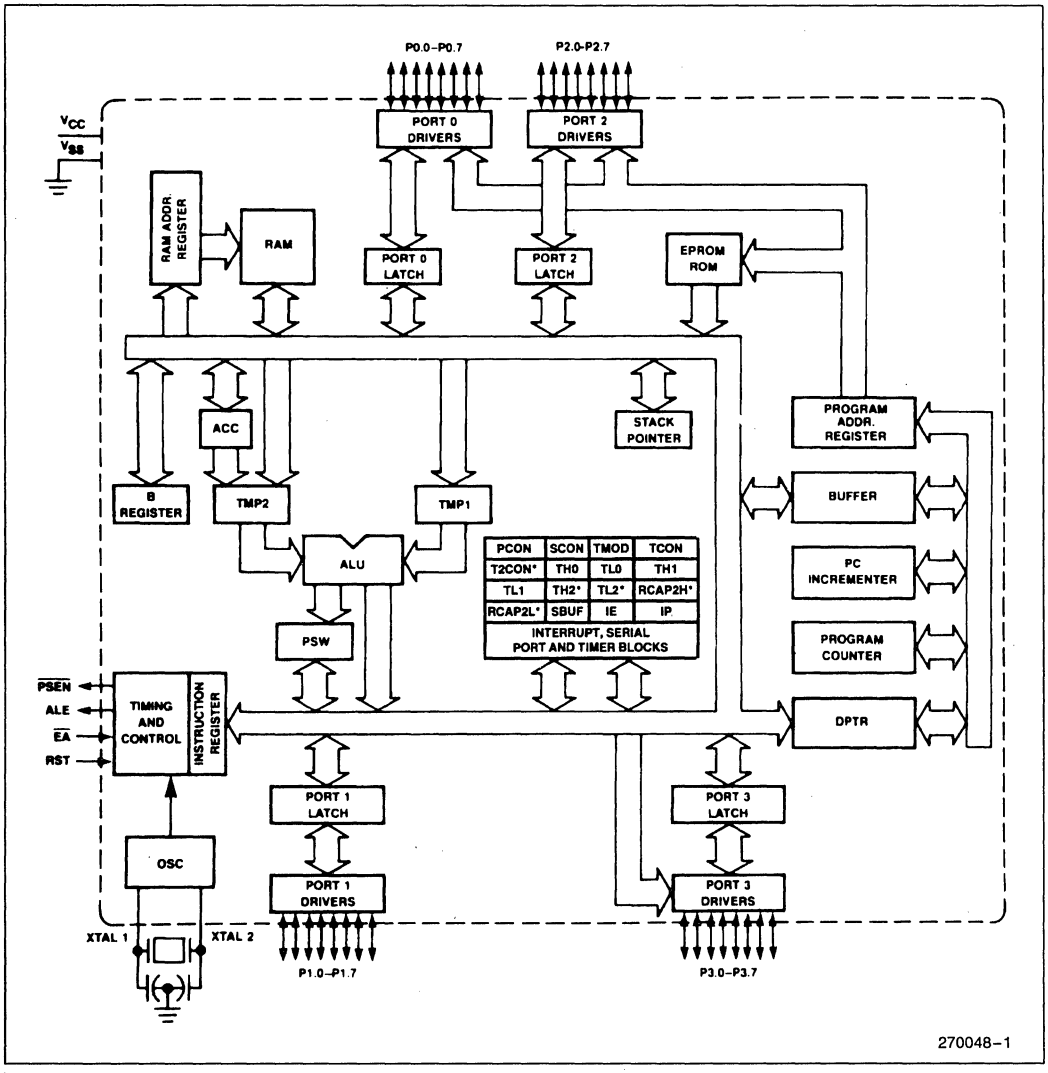


Figure 1. MCS®-51 Block Diagram

PROCESS INFORMATION

The 8031AH/8051AH and 8032AH/8052AH devices are manufactured on P414.1, an HMOS II process. The 8751H/8751H-8 devices are manufactured on P421.X, an HMOS-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8051AH/ 8031AH	P D N	40-Pin Plastic DIP 40-Pin CERDIP 44-Pin PLCC	45°C/W 45°C/W 46°C/W	16°C/W 15°C/W 16°C/W
8052AH/ 8032AH	P D N	40-Pin Plastic DIP 40-Pin CERDIP 44-Pin PLCC	45°C/W 45°C/W 46°C/W	16°C/W 15°C/W 16°C/W
8751H/ 8751H-8	D	40-Pin CERDIP	45°C/W	15°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

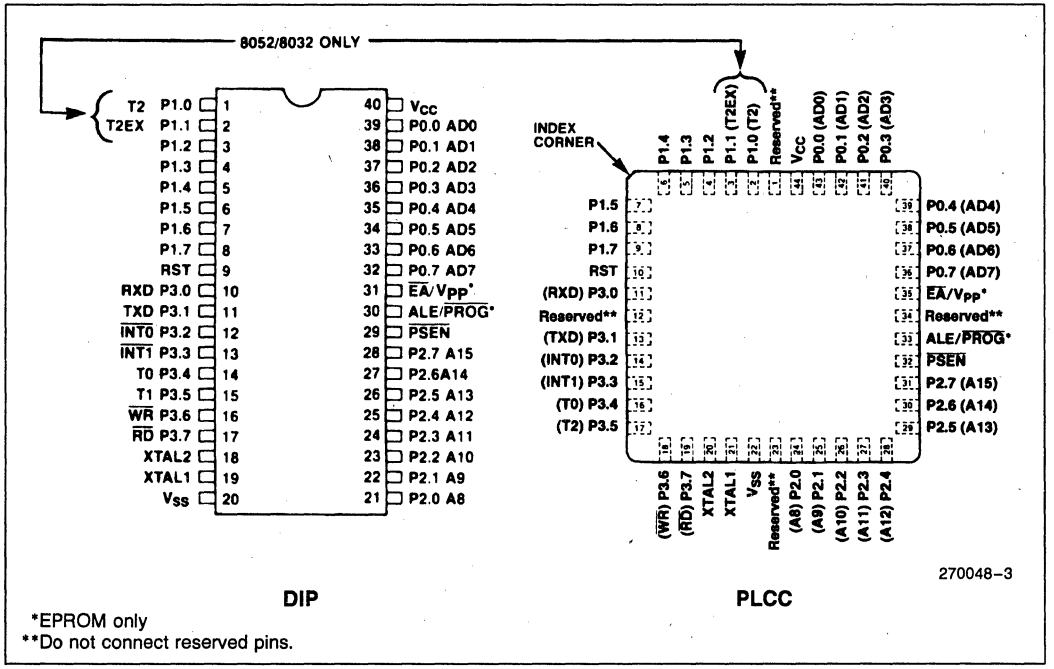


Figure 2. MCS®-51 Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs.

Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during programming of the EPROM parts, and outputs the code bytes during program verification of the ROM and EPROM parts. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during programming of the EPROM parts and during program verification of the ROM and EPROM parts.

In the 8032AH and 8052AH, Port 1 pins P1.0 and P1.1 also serve the T2 and T2EX functions, respectively.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during programming of the EPROM parts and during program verification of the ROM and EPROM parts.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL} on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternative Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during programming of the EPROM parts.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the device is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable $\overline{EA}$ must be strapped to V_{SS} in order to enable any MCS-51 device to fetch code from external Program memory locations starting at 0000H up to FFFFH. $\overline{EA}$ must be strapped to V_{CC} for internal program execution.

Note, however, that if the Security Bit in the EPROM devices is programmed, the device will not fetch code from any location in external Program Memory.

This pin also receives the 21V programming supply voltage (VPP) during programming of the EPROM parts.

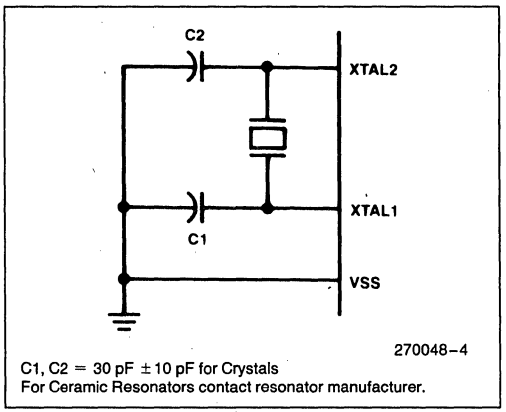


Figure 3. Oscillator Connections

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

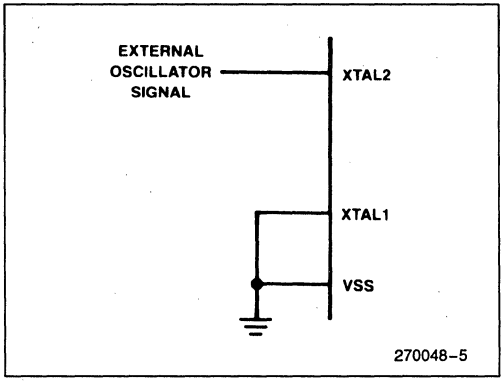


Figure 4. External Drive Configuration

DESIGN CONSIDERATIONS

If an 8751BH or 8752BH may replace an 8751H in a future design, the user should carefully compare both data sheets for DC or AC Characteristic differences. Note that the V_{IH} and I_{IH} specifications for the $\overline{EA}$ pin differ significantly between the devices.

Exposure to light when the EPROM device is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window when the die is exposed to ambient light.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on $\overline{EA}$/V_{PP} Pin to V_{SS} ... −0.5V to +21.5V
Voltage on Any Other Pin to V_{SS} .... −0.5V to +7V
Power Dissipation..... 1.5W

NOTICE: This is a production data sheet. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions: T_A (Under Bias) = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V

DC CHARACTERISTICS (Over Operating Conditions)

Symbol	Parameter		Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$ Pin of 8751H & 8751H-8)		−0.5	0.8	V	
V_{IL1}	Input Low Voltage to $\overline{EA}$ Pin of 8751H & 8751H-8		0	0.7	V	
V_{IH}	Input High Voltage (Except XTAL2, RST)		2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage to XTAL2, RST		2.5	V_{CC} + 0.5	V	XTAL1 = V_{SS}
V_{OL}	Output Low Voltage (Ports 1, 2, 3)*			0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)*					
		8751H, 8751H-8		0.60 0.45	V V	I_{OL} = 3.2 mA I_{OL} = 2.4 mA
		All Others		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)		2.4		V	I_{OH} = −80 µA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)		2.4		V	I_{OH} = −400 µA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, RST) 8032AH, 8052AH All Others			−800 −500	µA µA	V_{IN} = 0.45V V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current to $\overline{EA}$ Pin of 8751H & 8751H-8 Only			−15	mA	V_{IN} = 0.45V
I_{IL2}	Logical 0 Input Current (XTAL2)			−3.2	mA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0) 8751H & 8751H-8 All Others			±100 ±10	µA µA	$0.45 \le V_{IN} \le V_{CC}$ $0.45 \le V_{IN} \le V_{CC}$
I_{IH}	Logical 1 Input Current to $\overline{EA}$ Pin of 8751H & 8751H-8			500	µA	V_{IN} = 2.4V
I_{IH1}	Input Current to RST to Activate Reset			500	µA	$V_{IN} < (V_{CC} - 1.5V)$
I_{CC}	Power Supply Current: 8031AH/8051AH 8032AH/8052AH 8751H/8751H-8			 125 175 250	 mA mA mA	 All Outputs Disconnected; $\overline{EA}$ = V_{CC}
C_{IO}	Pin Capacitance			10	pF	Test freq = 1 MHz

***NOTE:**
Capacitive loading on Ports 0 and 2 may cause noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

AC CHARACTERISTICS Over Operating Conditions;
Load Capacitance for Port 0, ALE, and PSEN = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12.0	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold after ALE Low	48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instr In 8751H All Others		 183 233		 4TCLCL−150 4TCLCL−100	 ns ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL−25		ns
TPLPH	$\overline{PSEN}$ Pulse Width 8751H All Others	 190 215		 3TCLCL−60 3TCLCL−35		 ns ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In 8751H All Others		 100 125		 3TCLCL−150 3TCLCL−125	 ns ns
TPXIX	Input Instr Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float after $\overline{PSEN}$		63		TCLCL−20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	75		TCLCL−8		ns
TAVIV	Address to Valid Instr In 8751H All Others		 267 302		 5TCLCL−150 5TCLCL−115	 ns ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition 8751H All Others	 13 23		 TCLCL−70 TCLCL−60		 ns ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		20		20	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High 8751H All Others	 33 43	 133 123	 TCLCL−50 TCLCL−40	 TCLCL+50 TCLCL+40	 ns ns

NOTE:
*This table does not include the 8751-8 AC characteristics (see next page).

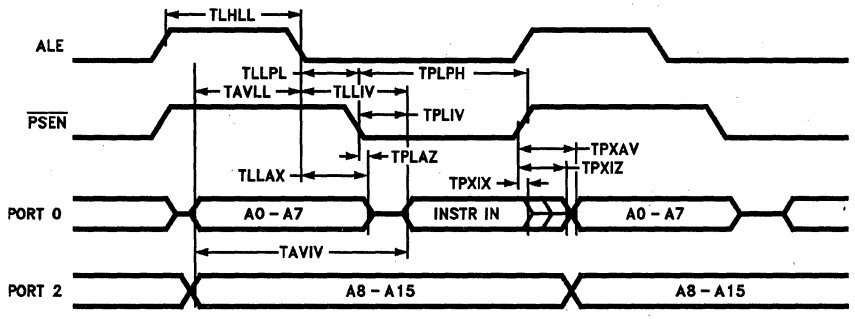
This Table is only for the 8751H-8

AC CHARACTERISTICS

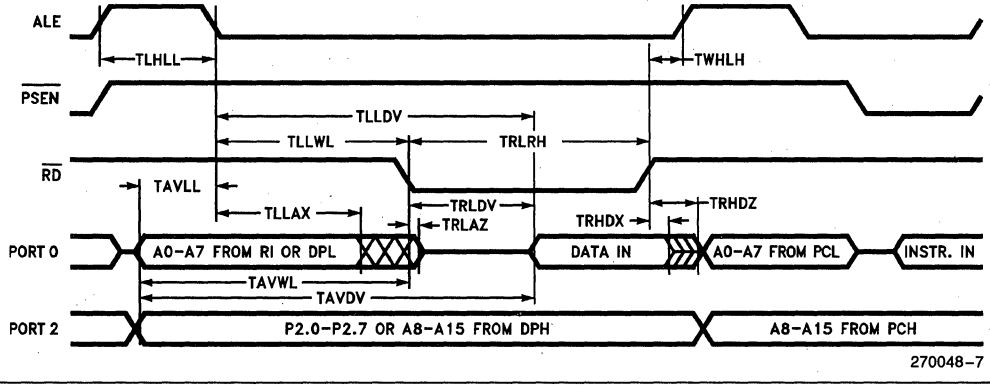
Over Operating Conditions;
Load Capacitance for Port 0, ALE, and PSEN = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

Symbol	Parameter	8 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	8.0	MHz
TLHLL	ALE Pulse Width	210		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	85		TCLCL−40		ns
TLLAX	Address Hold after ALE Low	90		TCLCL−35		ns
TLLIV	ALE Low to Valid Instr In		350		4TCLCL−150	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	100		TCLCL−25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	315		3TCLCL−60		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		225		3TCLCL−150	ns
TPXIX	Input Instr Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float after $\overline{PSEN}$		105		TCLCL−20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	117		TCLCL−8		ns
TAVIV	Address to Valid Instr In		475		5TCLCL−150	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	650		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	650		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		460		5TCLCL−165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		180		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		850		8TCLCL−150	ns
TAVDV	Address to Valid Data In		960		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	325	425	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	370		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	55		TCLCL−70		ns
TQVWH	Data Valid to $\overline{WR}$ High	725		7TCLCL−150		ns
TWHQX	Data Hold after $\overline{WR}$	75		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		20		20	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	75	175	TCLCL−50	TCLCL+50	ns

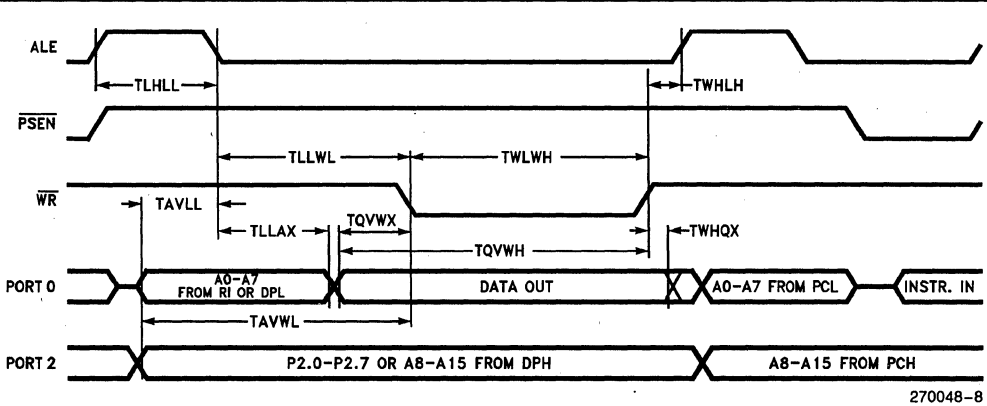
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

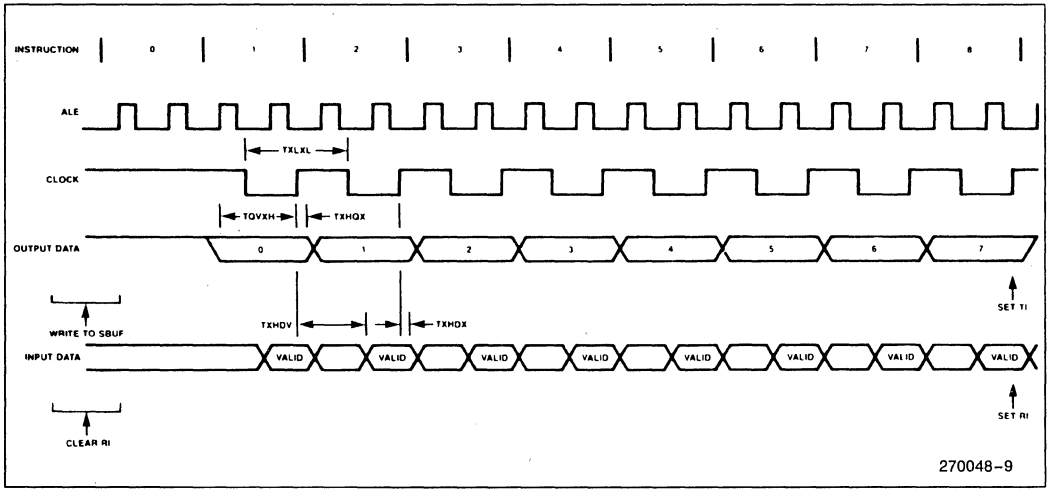


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

SHIFT REGISTER TIMING WAVEFORMS

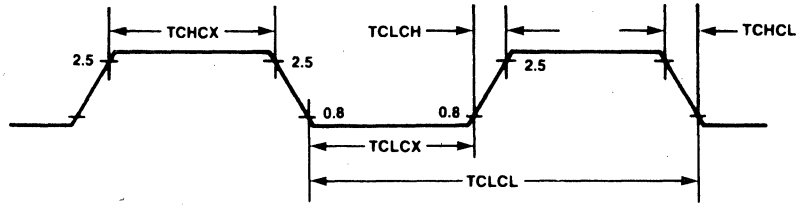


7

EXTERNAL CLOCK DRIVE

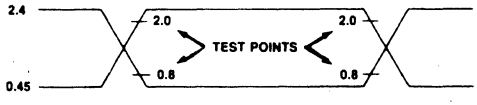
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency (except 8751H-8) 8751H-8	3.5 3.5	12 8	MHz MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



270048-10

AC TESTING INPUT, OUTPUT WAVEFORM



270048-11

AC Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

EPROM CHARACTERISTICS

Table 3. EPROM Programming Modes

Mode	RST	PSEN	ALE	EA	P2.7	P2.6	P2.5	P2.4
Program	1	0	0*	VPP	1	0	X	X
Inhibit	1	0	1	X	1	0	X	X
Verify	1	0	1	1	0	0	X	X
Security Set	1	0	0*	VPP	1	1	X	X

NOTE:
"1" = logic high for that pin
"0" = logic low for that pin
"X" = "don't care"
"VPP" = +21V ±0.5V
*ALE is pulsed low for 50 ms.

Programming the EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0–P2.3 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 pins, and RST, PSEN, and EA should be held at the "Program" levels indicated in Table 3. ALE is **pulsed** low for 50 ms to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally EA is held at a logic high until just before ALE is to be pulsed. Then EA is raised to +21V, ALE is pulsed, and then EA is returned to a logic high. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

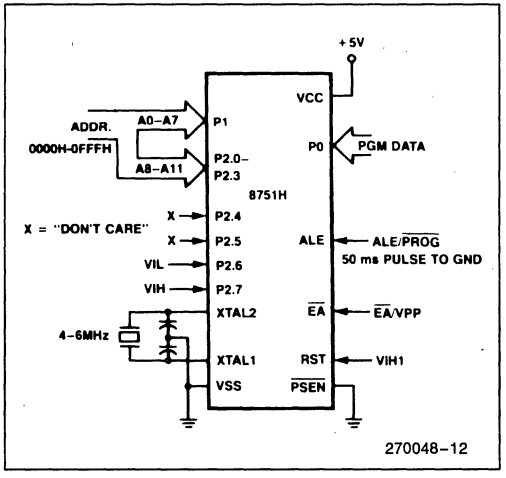


Figure 5. Programming Configuration

Note that the EA/VPP pin must not be allowed to go above the maximum specified VPP level of 21.5V for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The VPP source should be well regulated and free of glitches.

Program Verification

If the Security Bit has not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0–P2.3. The other pins should be held at the "Verify" levels indicated in Table 3. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation.

The setup, which is shown in Figure 6, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active-low read strobe.

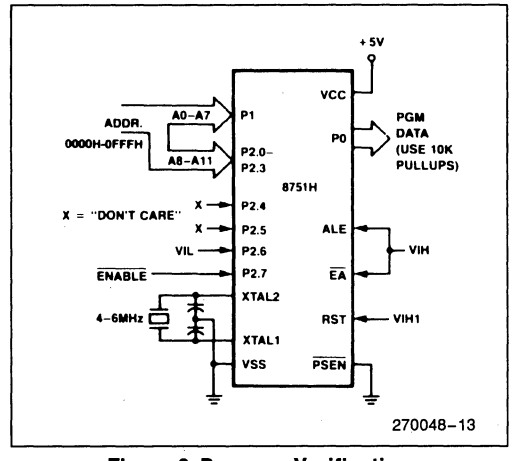


Figure 6. Program Verification

EPROM Security

The security feature consists of a "locking" bit which when programmed denies electrical access by any external means to the on-chip Program Memory. The bit is programmed as shown in Figure 7. The setup and procedure are the same as for normal EPROM programming, except that P2.6 is held at a logic high. Port 0, Port 1 and pins P2.0–P2.3 may be in any state. The other pins should be held at the "Security" levels indicated in Table 3.

Once the Security Bit has been programmed, it can be cleared only by full erasure of the Program Memory. While it is programmed, the internal Program Memory can not be read out, the device can not be further programmed, and it **can not execute out of external program memory**. Erasing the EPROM, thus clearing the Security Bit, restores the device's full functionality. It can then be reprogrammed.

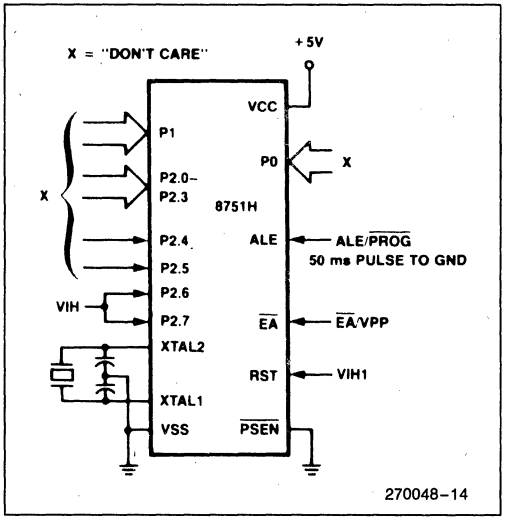


Figure 7. Programming the Security Bit

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

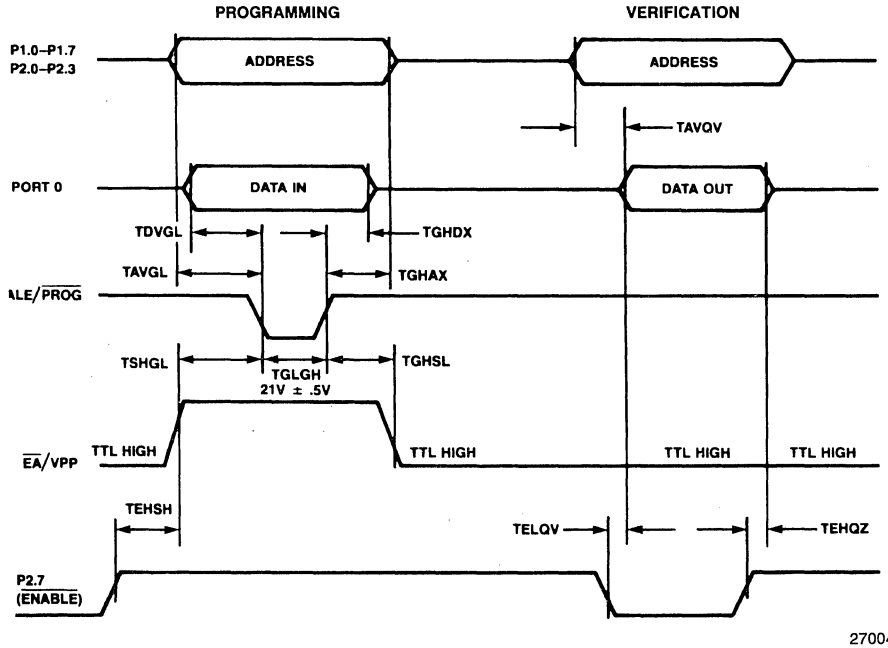
Erasure leaves the array in an all 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_A = 21°C to 27°C; VCC = 5V ±10%; VSS = 0V

Symbol	Parameter	Min	Max	Units
VPP	Programming Supply Voltage	20.5	21.5	V
IPP	Programming Supply Current		30	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{\text{PROG}}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{\text{PROG}}$	48TCLCL		
TDVGL	Data Setup to $\overline{\text{PROG}}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{\text{PROG}}$	48TCLCL		
TEHSH	P2.7 ($\overline{\text{ENABLE}}$) High to VPP	48TCLCL		
TSHGL	VPP Setup to $\overline{\text{PROG}}$ Low	10		μs
TGHSL	VPP Hold after $\overline{\text{PROG}}$	10		μs
TGLGH	$\overline{\text{PROG}}$ Width	45	55	ms
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{\text{ENABLE}}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float after $\overline{\text{ENABLE}}$	0	48TCLCL	

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



For programming conditions see Figure 5.

For verification conditions see Figure 6.

DATA SHEET REVISION HISTORY

This data sheet (270048-007) is valid for 8051AH/8031AH and 8052AH/8032AH devices with an "A" at the end of the topside tracking number. It is also valid for 8751H/8751H-8 devices without an "A" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (270048-007) and the previous version (270048-006):

1. Data sheet title was changed from:
   MCS-51 8-Bit Control-Oriented Microcomputers 8031AH/8051AH 8032AH/8052AH 8751H/8751H-8
   to:
   MCS-51 8-Bit Control-Oriented Microcontrollers 8031AH/8051AH 8032AH/8052AH 8751H/8751H-8
2. The Operating Temperature Range has been changed to: 0°C to +70°C.

The following differences exist between the -006 and the -005 version of this data sheet.

1. 8051/8031 device offering deleted.
2. θ_{ja} and θ_{jc} specifications added to the "Packages" table.
3. Capacitor values for ceramic resonators deleted from Figure 3.

The following are the key differences between the -005 and the -004 version of this data sheet.

1. Data sheet status changed from "Preliminary" to "Production".
2. LCC package offering deleted.
3. Maximum Ratings Warning and Data Sheet Revision History revised.

The following are the key differences between the -004 and the -003 version of this data sheet:

1. Introduction was expanded to include product descriptions.
2. Package table was added.
3. Design Considerations added.
4. Test Conditions for I_{IL1} and I_{IH} specifications added to the DC Characteristics.
5. Data Sheet Revision History added.

8051AHP
MCS®-51 FAMILY
8-BIT CONTROL-ORIENTED MICROCONTROLLER WITH PROTECTED ROM

- **High Performance HMOS Process**
- **Internal Timers/Event Counters**
- **2-Level Interrupt Priority Structure**
- **32 I/O Lines (Four 8-Bit Ports)**
- **4K Program Memory Space**
- **Protection Feature Protects ROM Parts Against Software Piracy**
- **Boolean Processor**
- **Bit-Addressable RAM**
- **Programmable Full Duplex Serial Channel**
- **111 Instructions (64 Single-Cycle)**
- **4K Data Memory Space***
  *Expandable to 64K
- **Available in 40 Pin Plastic and CERDIP Packages**
  (See Packaging Outlines and Dimensions Order #231369)

The MCS®-51 products are optimized for control applications. Byte-processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide instructions. Extensive on-chip support is provided for one-bit variables as a separate data type, allowing direct bit manipulation and testing in control and logic systems that require Boolean processing.

MCS-51 HMOS Family Device	Internal Memory		Timers/ Event Counters	Interrupts
	Program	Data		
8051AH	4K x 8 ROM	128 x 8 RAM	2 x 16-Bit	5
8051AHP	4K x 8 ROM	128 x 8 RAM	2 x 16-Bit	5

The 8051AHP is identical to the 8051AH with the exception of the Protection Feature. To incorporate this Protection Feature, program verification has been disabled and external memory accesses have been limited to 4K.

7

October 1990
Order Number: 270279-004

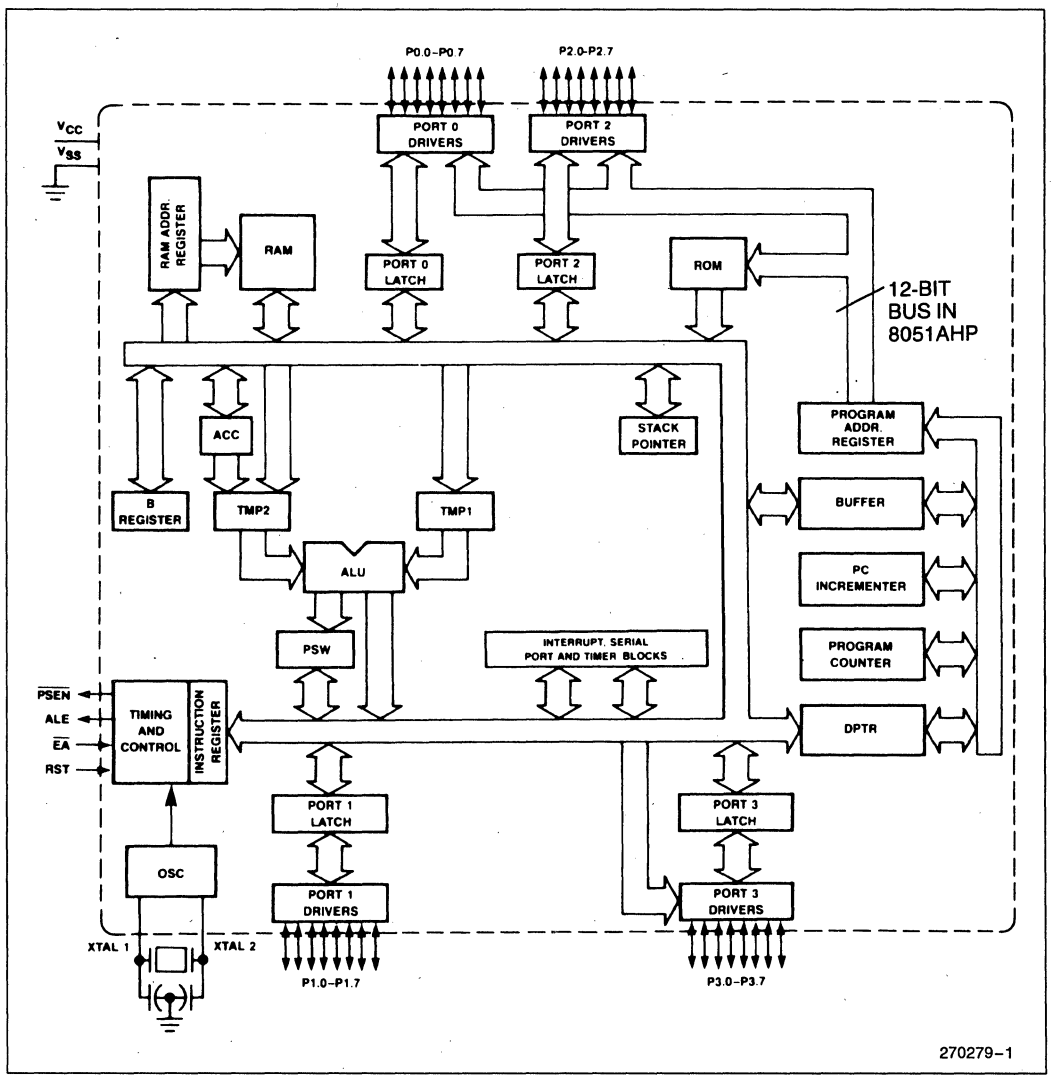
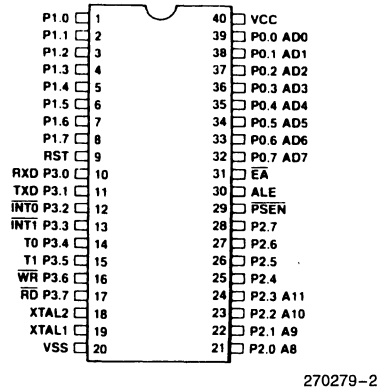


Figure 1. MCS®-51 Block Diagram

PACKAGES

Part	Prefix	Package Type
8051AHP	P	40-Pin Plastic DIP
	D	40-Pin CERDIP



Pin (PDIP, CERDIP)

Figure 2. MCS®-51 Connections

PIN DESCRIPTIONS

V_{CC}

Supply voltage.

V_{SS}

Circuit ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs.

Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s and can source and sink 8 LS TTL inputs.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. Bits P2.4 through P2.7 are forced to 0, effectively limiting external Data and Code space to 4K each in the 8051AHP during external accesses*. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL} on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternative Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

*Protection feature

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{\text{PSEN}}$

Program Store Enable is the read strobe to external Program Memory.

When the device is executing code from external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external Data Memory.

$\overline{\text{EA}}$

External Access enable $\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions. $\overline{\text{EA}}$ must be strapped to V_{SS} in order to enable any MCS-51 device to fetch code from external Program memory locations starting at 0000H up to FFFFH.

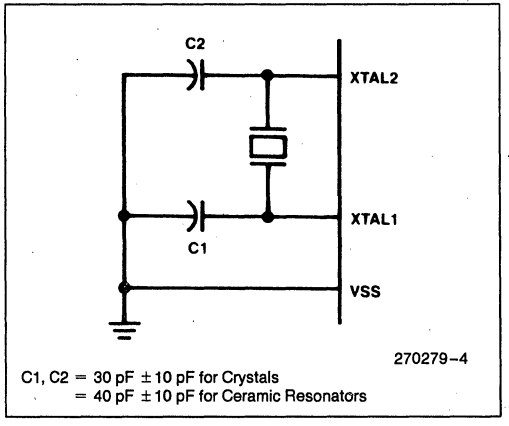


Figure 3. Oscillator Connections

XTAL1

Input to the inverting oscillator amplifier.

XTAL2

Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

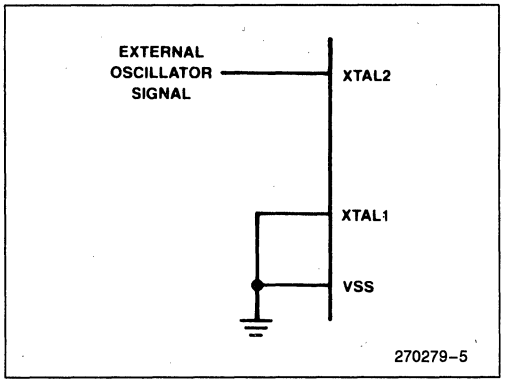


Figure 4. External Drive Configuration

DESIGN CONSIDERATION

The 8051AHP cannot access external Program or Data memory above 4K. This means that the following instructions that use the Data Pointer only read/write data at address locations below 0FFFH:

```
MOVX A, @DPTR
MOVX @DPTR, A
```

When the Data Pointer contains an address above the 4K limit, those locations will not be accessed.

To access Data Memory above 4K, the MOVX, @Ri, A or MOVX A, @Ri instructions must be used.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} . . . −0.5V to +21.5V
Voltage on Any Other Pin to V_{SS} . . . . −0.5V to +7V
Power Dissipation 1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions: T_A (Under Bias) = 0°C to +70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V

D.C. CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (Except XTAL2, RST)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage to XTAL2, RST	2.5	V_{CC} + 0.5	V	XTAL1 = V_{SS}
V_{OL}	Output Low Voltage (Ports 1, 2, 3)*		0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)*		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	2.4		V	I_{OH} = −80 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4		V	I_{OH} = −400 μA
I_{IL}	Logical 0 Input Current		−500	μA	V_{IN} = 0.45V
I_{IL2}	Logical 0 Input Current (XTAL2)		−3.2	mA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0)		±10	μA	0.45 ≤ V_{IN} ≤ V_{CC}
I_{IH}	Input Current to RST to Activate Reset		500	μA	V_{IN} < (V_{CC} − 1.5V)
I_{CC}	Power Supply Current		125	mA	All Outputs Disconnected; $\overline{EA}$ = VCC
CIO	Pin Capacitance		10	pF	Test freq = 1 MHz

***NOTE:**
Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

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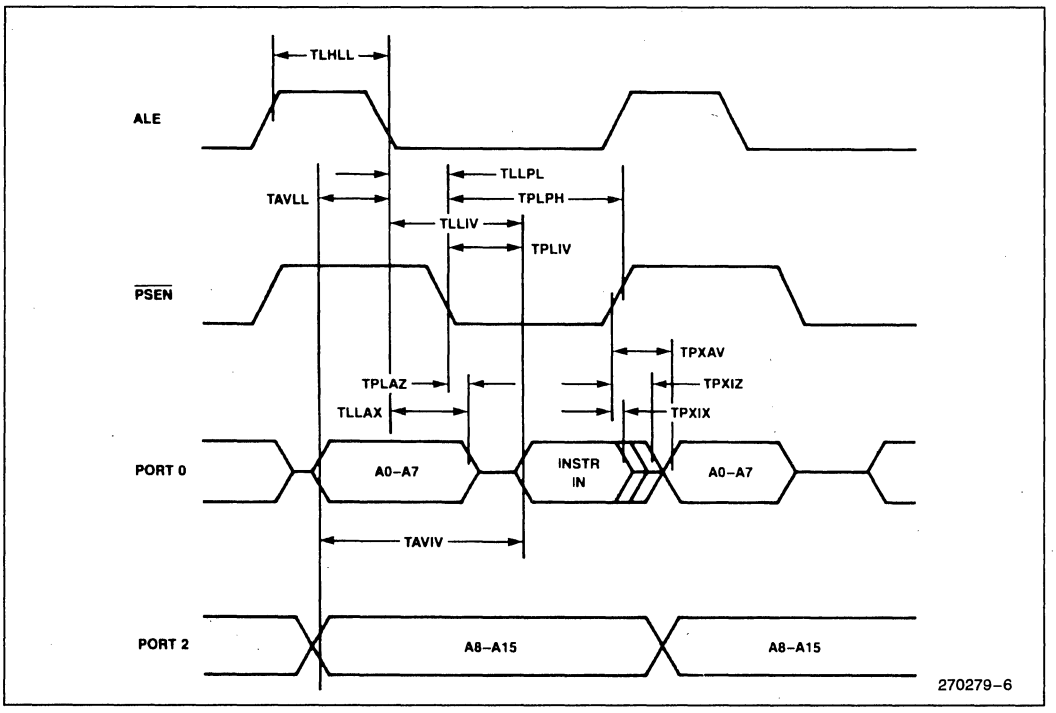
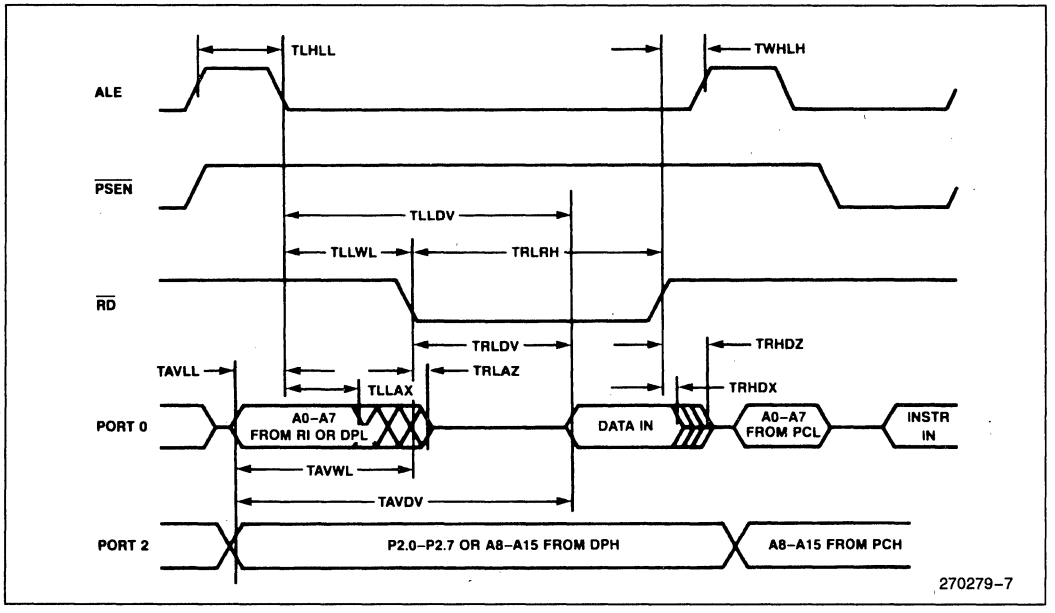
A.C. CHARACTERISTICS Under Operating Conditions;
Load Capacitance for Port 0, ALE, and PSEN = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12.0	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold after ALE Low	48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instr In		233		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL−25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		3TCLCL−35		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		125		3TCLCL−125	ns
TPXIX	Input Instr Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float after $\overline{PSEN}$		63		TCLCL−20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	75		TCLCL−8		ns
TAVIV	Address to Valid Instr In		302		5TCLCL−115	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	23		TCLCL−60		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		20		20	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



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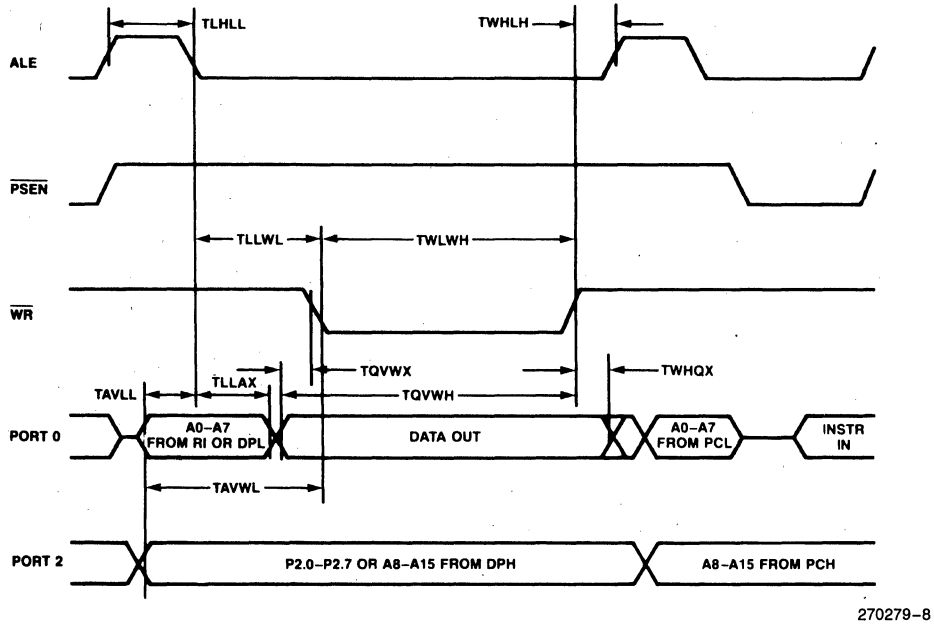
EXTERNAL DATA MEMORY WRITE CYCLE

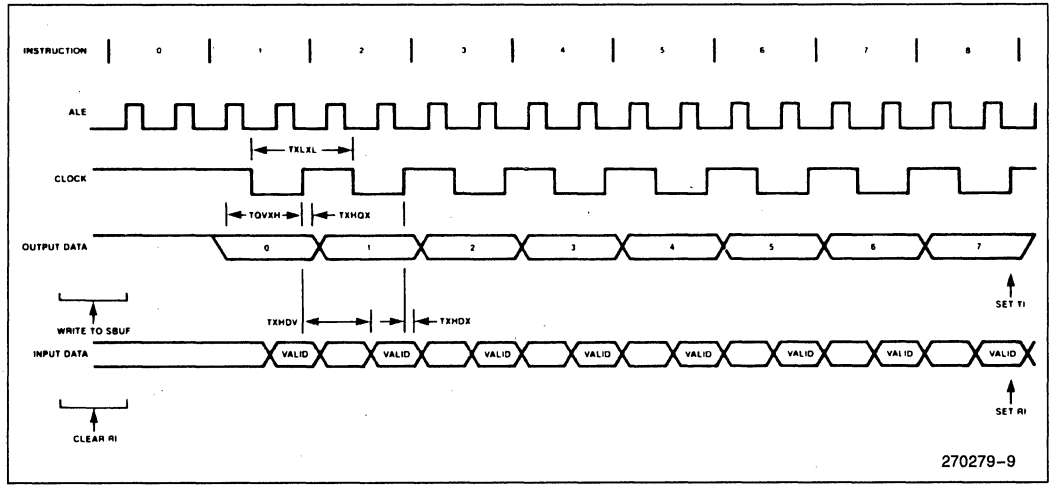


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

SHIFT REGISTER TIMING WAVEFORMS



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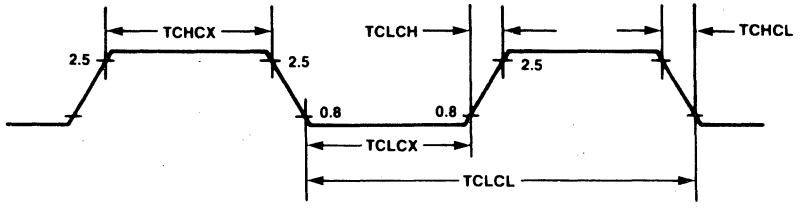
EXTERNAL CLOCK DRIVE

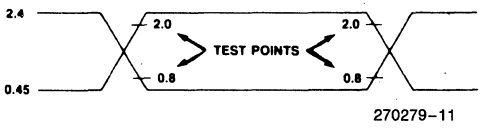
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



270279-10

A.C. TESTING INPUT, OUTPUT WAVEFORM



270279-11

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

Program Verification

The program verification test mode has been eliminated on the 8051AHP. It is not possible to verify the ROM contents using this mode, the way EPROM programmers typically do. Also, the ROM contents cannot be verified by a program executing out of external program memory due to the restricted addressing on the 8051AHP.

DATA SHEET REVISION HISTORY

The following are the key differences between this and the -003 version of the 8051AHP data sheet:

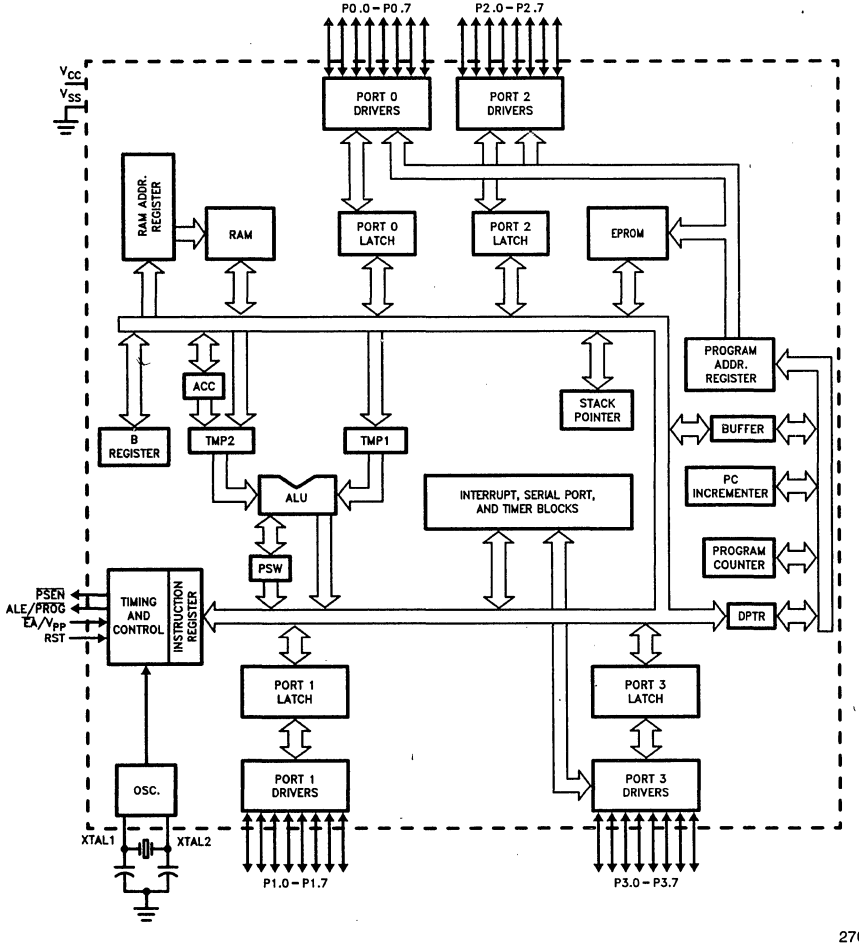
1. Data sheet status changed from "Preliminary" to "Production".
2. Revised Maximum Ratings Warning and Data Sheet Status Notice.

The following are the key differences between this and the -002 version of 8051AHP data sheet:

1. Package Table was added.
2. Added clearer explanation to DESIGN CONSIDERATION.
3. Data Sheet Revision History was added.

8751BH
SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 4 KBYTES OF EPROM PROGRAM MEMORY

- Program Memory Lock
- 128 Bytes Data Ram
- Quick Pulse Programming Algorithm
- 12.75 Volt Programming Voltage
- Boolean Processor
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 5 Interrupt Sources
- Programmable Serial Channel
- 64K External Program Memory Space
- 64K External Data Memory Space



270248–1

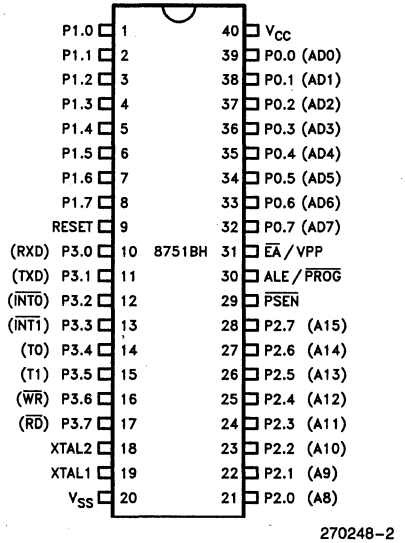
Figure 1. 8751BH Block Diagram

7

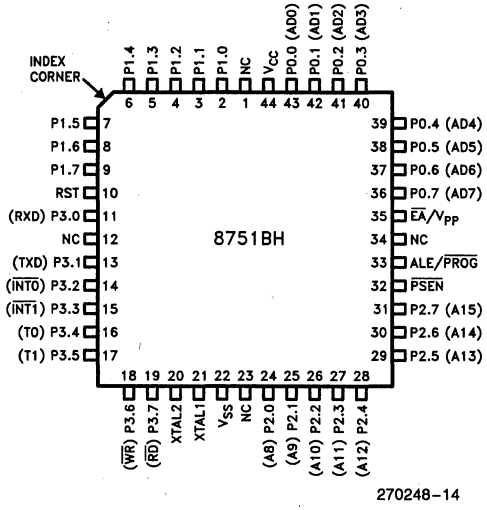
September 1992
Order Number: 270248-005

PACKAGES

Part	Prefix	Package Type
8751BH	P N	40-Pin Plastic DIP 44-Pin PLCC



Pin (DIP)



Pad (PLCC)

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s, and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS®-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during EPROM programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$: Program Store Enable is the Read strobe to External Program Memory.

When the 8751BH is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Applications Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

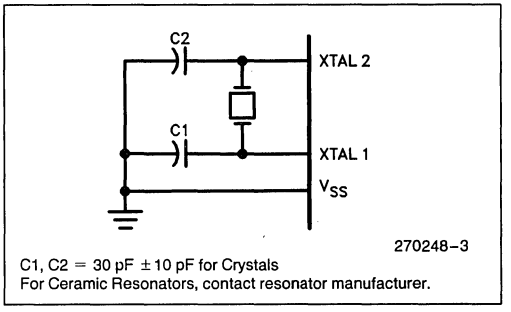


Figure 3. Oscillator Connections

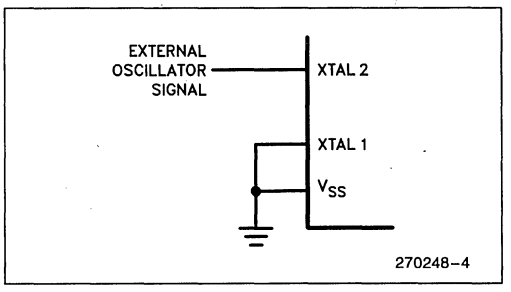


Figure 4. External Clock Drive Configuration

DESIGN CONSIDERATIONS

If an 8751BH is replacing an 8751H in an existing design, the user should carefully compare both data sheets for DC or AC Characteristic differences. Note that the V_{IH} and I_{IH} specifications for the EA pin differ significantly between the 8751H and 8751BH.

7

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} . . . −0.5V to +13.0V
Voltage on Any Other Pin to V_{SS} . . . . −0.5V to +7V
Maximum I_{OL} Per I/O Pin . . . . . 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Operating Conditions: T_A (Under Bias) = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V

DC CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	V_{SS}	0.7	V	
V_{IH}	Input High Voltage (Except XTAL2, RST, $\overline{EA}$)	2.0	V_{CC}+0.5	V	
V_{IH1}	Input High Voltage XTAL2, RST	2.5	V_{CC}+0.5	V	XTAL1 = VSS
V_{IH2}	Input High Voltage to $\overline{EA}$	4.5	5.5	V	
V_{OL}	Output Low Voltage (Note 3) (Ports 1, 2 and 3)		0.45	V	I_{OL} = 1.6 mA (Note 1)
V_{OL1}	Output Low Voltage (Note 3) (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)		0.45	V	I_{OL} = 3.2 mA (Notes 1, 2)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE/$\overline{PROG}$ and $\overline{PSEN}$)	2.4		V	I_{OH} = −80 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4		V	I_{OH} = −400 μA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3 and RST)		−1	mA	V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current ($\overline{EA}$)		−10	mA	V_{IN} = VSS
I_{IL2}	Logical 0 Input Current (XTAL2)		−3.2	mA	V_{IN} = 0.45 V XTAL1 = V_{SS}
I_{LI}	Input Leakage Current (Port 0)		±10	μA	0.45 < V_{IN} < V_{CC}
I_{IH}	Logical 1 Input Current ($\overline{EA}$)		1	mA	4.5V < V_{IN} < 5.5V
I_{IH1}	Input Current to RST to Activate Reset		500	μA	V_{IN} < (V_{CC} − 1.5V)
I_{CC}	Power Supply Current		175	mA	All Outputs Disconnected
C_{IO}	Pin Capacitance		10	pF	Test Freq = 1MHz

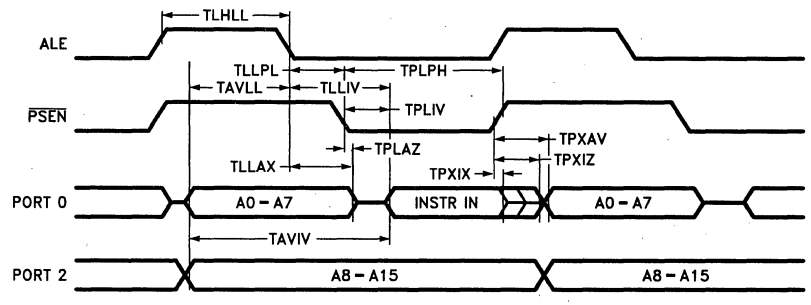
NOTES:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE/$\overline{PROG}$ and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE/$\overline{PROG}$ pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. ALE/$\overline{PROG}$ refers to a pin on the 8751BH. ALE refers to a timing signal that is output on the ALE/$\overline{PROG}$ pin.
3. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port -
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

AC CHARACTERISTICS (Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

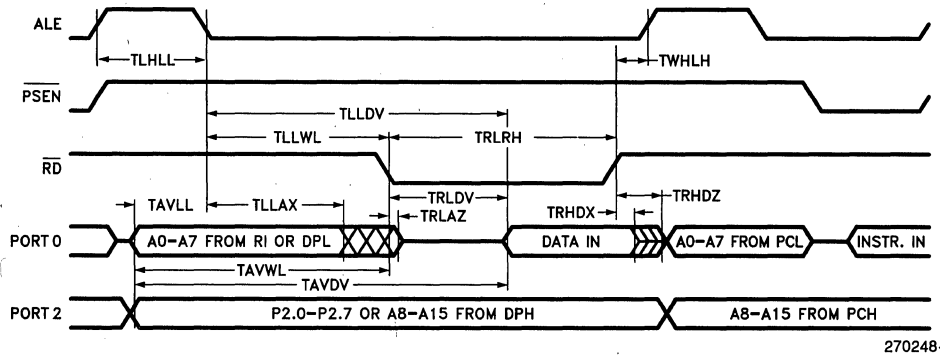
Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12.0	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instruction In		233		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL−25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		3TCLCL−35		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		125		3TCLCL−125	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		63		TCLCL−20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	75		TCLCL−8		ns
TAVIV	Address to Valid Instruction In		302		5TCLCL−115	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	23		TCLCL−60		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TWHQX	Data Held After $\overline{WR}$	33		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



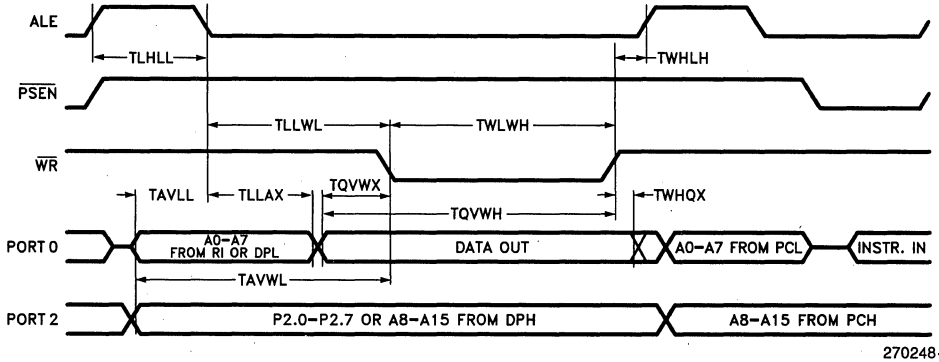
270248-5

EXTERNAL DATA MEMORY READ CYCLE



270248-6

EXTERNAL DATA MEMORY WRITE CYCLE



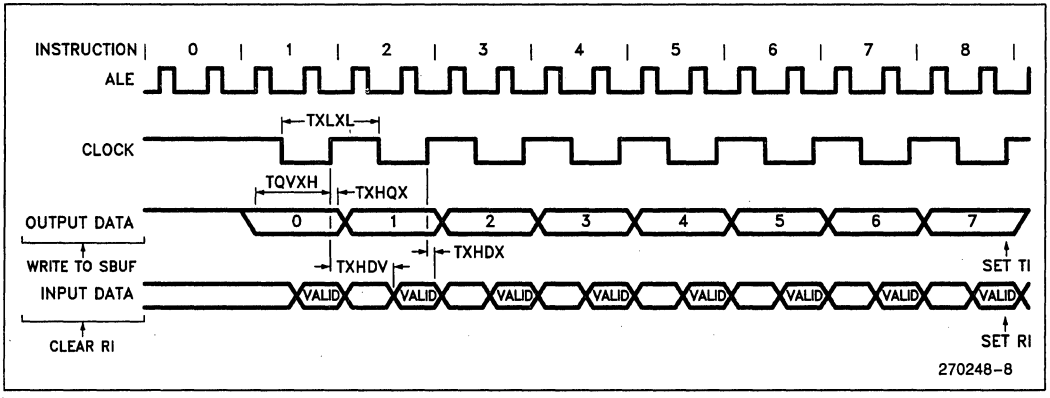
270248-7

SERIAL PORT TIMING — SHIFT REGISTER MODE

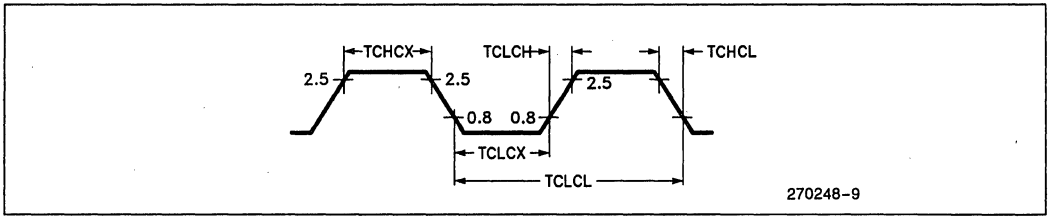
TEST CONDITIONS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V; Load Capacitance = 80 pF)

Symbol	Parameter	12MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



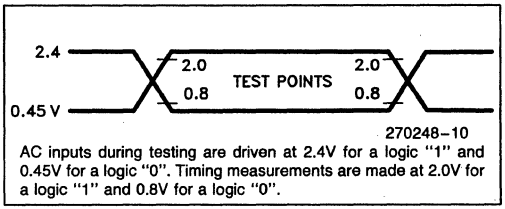
EXTERNAL CLOCK DRIVE WAVEFORMS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

AC TESTING INPUT/OUTPUT WAVEFORMS



AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

EPROM CHARACTERISTICS

Programming the EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.3 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, and RST, $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 1. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally $\overline{EA}/V_{PP}$ is held at a logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches.

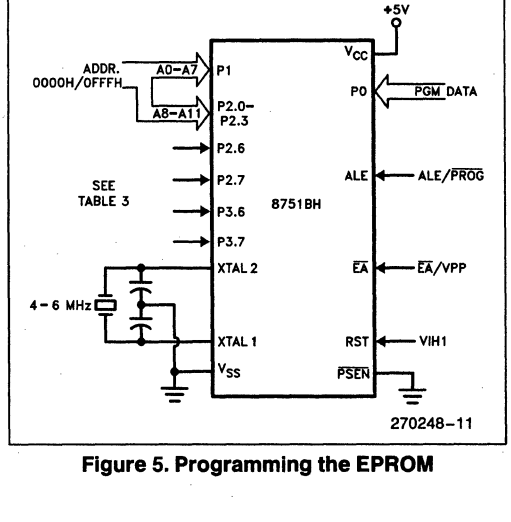


Figure 5. Programming the EPROM

Table 1. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/VPP	P2.7	P2.6	P3.6	P3.7
Program Code Data	1	0	0*	VPP	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Program Encryption Table Use Addresses 0-1FH	1	0	0*	VPP	1	0	0	1
Program Lock x=1	1	0	0*	VPP	1	1	1	1
Bits (LBx) x=2	1	0	0*	VPP	1	1	0	0
Read Signature	1	0	1	1	0	0	0	0

NOTES:
"1" = Valid high for that pin
"0" = Valid low for that pin
"VPP" = +12.75V ±0.25V
* ALE/PROG is pulsed low for 100 μs for programming. (Quick-Pulse Programming)

QUICK-PULSE PROGRAMMING ALGORITHM

The 8751BH can be programmed using the Quick-Pulse Programming Algorithm for microcontrollers. The features of the new programming method are a lower VPP (12.75 volts as compared to 21 volts) and a shorter programming pulse. It is possible to program the entire 4 Kbytes of EPROM memory in less than 13 seconds with this algorithm

To program the part using the new algorithm, VPP must be 12.75 ±0.25 Volts. ALE/PROG is pulsed low for 100 μseconds, 25 times. Then, the byte just programmed may be verified. After programming, the entire array should be verified. The Program Lock features are programmed using the same method, but with the setup as shown in Table 1. The only difference in programming Lock features is that the Lock features cannot be directly verified. Instead, verification of programming is by observing that their features are enabled.

PROGRAM VERIFICATION

If the Lock Bits have not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0 - P2.3. The other pins should be held at the "Verify" levels indicated in Table 1. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation. (If the Encryption Array in the EPROM has been programmed, the data present at Port 0 will be Code Data XNOR Encryption Data. The user must know the Encryption Array contents to manually "unencrypt" the data during verify.)

The setup, which is shown in Figure 6, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active low read strobe.

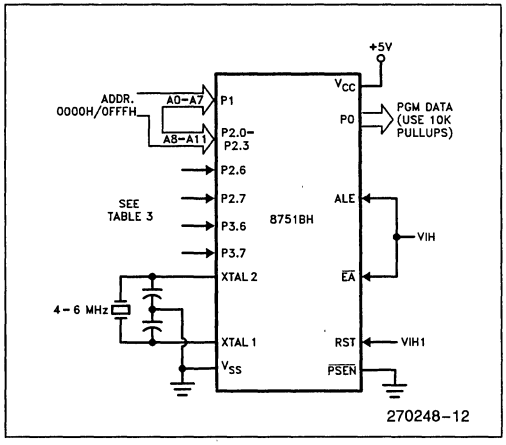


Figure 6. Verifying the EPROM

PROGRAM MEMORY LOCK

The two-level Program Lock system consists of 2 Lock bits and a 32-byte Encryption Array which are used to protect the program memory against software piracy.

Encryption Array

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte. The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form.

It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

Lock Bits

Also included in the EPROM Program Lock scheme are two Lock Bits which function as shown in Table 2.

Table 2. Lock Bits and their Features

Lock Bits		Logic Enabled
LB1	LB2	
U	U	Minimum Program Lock features enabled. (Code Verify will still be encrypted by the Encryption Array)
P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled
P	P	Same as above, but Verify is also disabled
U	P	Reserved for Future Definition

P = Programmed
U = Unprogrammed

To ensure proper functionality of the chip, the internally latched value of the $\overline{EA}$ pin must agree with its external state.

ERASURE CHARACTERISTICS

This device is in a plastic package without a window and, therefore, cannot be erased.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. the values returned are:

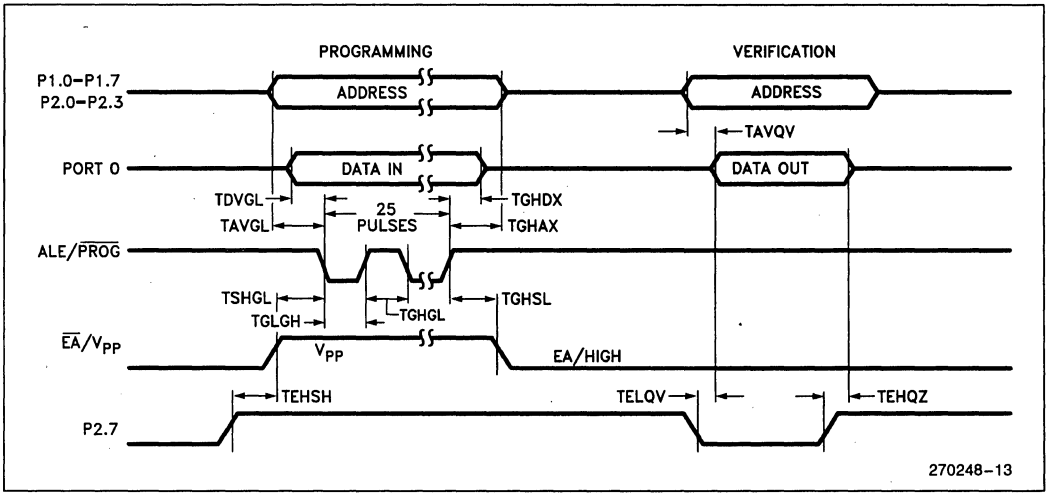
(030H) = 89H indicates manufactured by Intel
(031H) = 51H indicates 8751BH

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C, V_{CC} = 5.0V ±10%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
IPP	Programming Supply Current		50	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold After $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold After $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µsec
TGHSL	V_{PP} Hold After $\overline{PROG}$	10		µsec
TGLGH	$\overline{PROG}$ Width	90	110	µsec
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float After $\overline{ENABLE}$	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µsec

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



DATA SHEET REVISION HISTORY

The following is the key difference between this and the -004 version of the 8751BH data sheet:

Data sheet title was changed from:
8751BH Single-Chip 8-Bit Microcomputer with 4K Bytes of EPROM Program Memory

to:
8751BH Single-Chip 8-Bit Microcontroller with 4 Kbytes of EPROM Program Memory

The following are the key differences between the -004 and the -003 version of the 8751BH data sheet:

1. Data sheet status changed from "Preliminary" to "Production".
2. Revised Maximum Ratings Warning and data sheet status notice.

The following are the key differences between the -003 and the -002 version of the 8751BH data sheet:

1. Status went from ADVANCE INFORMATION to PRELIMINARY.
2. Package Table was added.
3. PLCC pin connections shown.
4. Design Considerations section replaced with reference to previous designs using the 8751H.
5. Note 3 on maximum current specification was added to DC Characteristics.
6. Table 1 updated to show Read Signature Mode.
7. ERASING THE EPROM paragraph deleted.
8. ERASURE CHARACTERISTICS section changed to indicate plastic packages only.
9. Signature Bytes added.
10. Data Sheet Revision History was added.

8751BH

EXPRESS

■ **Extended Temperature Range** ■ **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program is an extended temperature range with or without burn-in.

With the commercial standard temperature range operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic, for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS T_A = −40°C to +85°C; V_{CC} = 5V ±10%; V_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input High Voltage (Except XTAL2, RST, $\overline{EA}$)	2.1	V_{CC} + 0.5	V	

7

January 1989
Order Number: 270708-001

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	plastic	commercial	no
N	PLCC	commercial	no
TP	plastic	extended	no
TN	PLCC	extended	no
LP	plastic	extended	yes

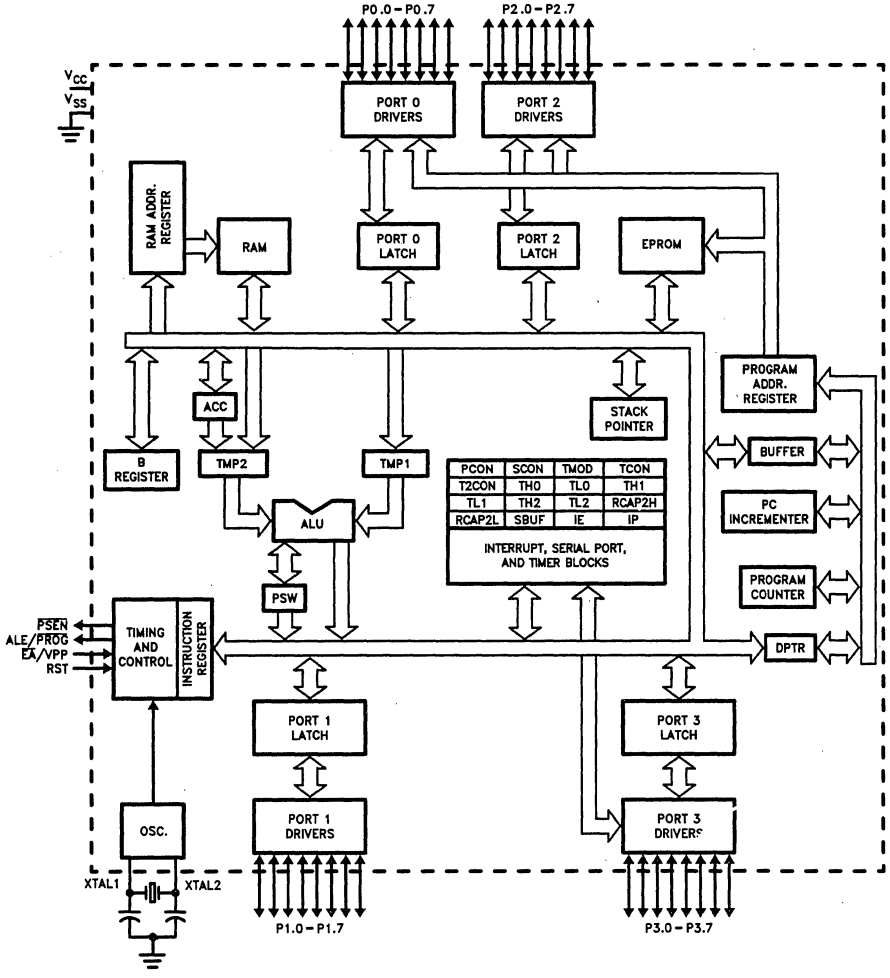
Please note:

- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-in is dynamic, for a minimum time of 160 hours at 125°C, V_{CC} = 5.5V ±0.25V, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples: N8751BH indicates 8751BH in a PLCC package and specified for commercial temperature range, without burn-in. LP8751BH indicates 8751BH in a plastic package and specified for extended temperature range with burn-in.

8752BH
SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 8 KBYTES OF EPROM PROGRAM MEMORY

- 2-Bit Program Memory Lock
- 256 Bytes Data Ram
- Quick Pulse Programming Algorithm
- 12.75 Volt Programming Voltage
- Boolean Processor
- 32 Programmable I/O Lines
- Three 16-Bit Timer/Counters
- 6 Interrupt Sources
- Programmable Serial Channel
- Separate Transmit/Receive Baud Rate Capability
- 64K External Program Memory Space
- 64K External Data Memory Space



270429-1

Figure 1. Block Diagram

7

September 1992
Order Number: 270429-004

PACKAGES

Part	Prefix	Package Type
8752BH	P	40-Pin Plastic DIP
	D	40-Pin CERDIP
	N	44-Pin PLCC

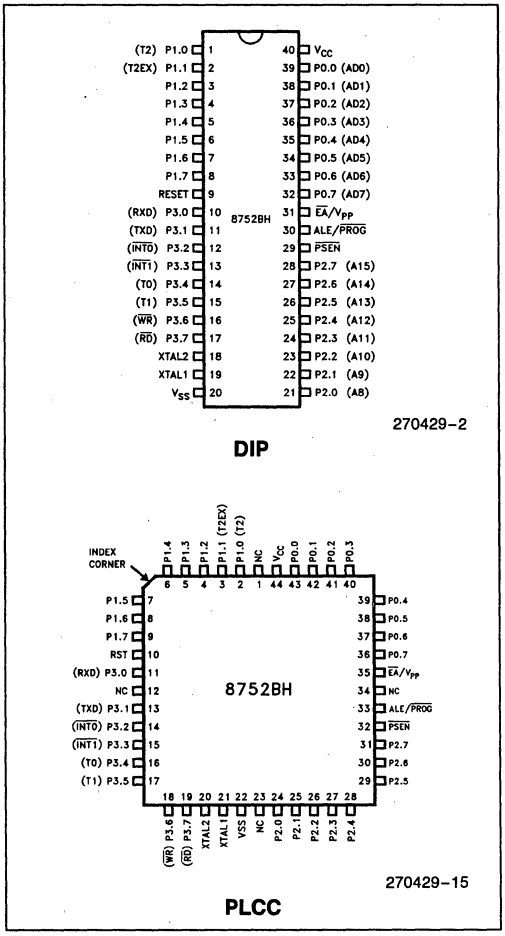


Figure 2. Pin Connections

PIN DESCRIPTION

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s, and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

In addition, P1.0 and P1.1 serve the functions of the following special features of the MCS®-51 Family:

Port Pin	Alternate Function
P1.0	T2 (Timer/Counter 2 External Input)
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger)

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS®-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during EPROM programming on the 8752BH.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

PSEN: Program Store Enable is the Read strobe to External Program Memory.

When the device is executing code from external Program Memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to External Data Memory.

EA/V_{PP}: External Access enable. EA must be strapped to V_{SS} in order to enable the device to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits are programmed, EA will be internally latched on reset.

EA should be strapped to V_{CC} for internal program executions.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.

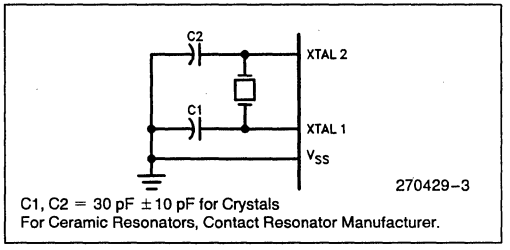
XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Applications Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, Contact Resonator Manufacturer.

Figure 3. Oscillator Connections

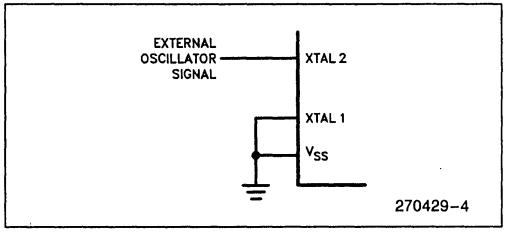


Figure 4. External Clock Drive Configuration

DESIGN CONSIDERATIONS

Exposure to light when the 8752BH is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window of the 8752BH when the die is exposed to ambient light.

Due to a timing problem in the Timer/Counter 2 interrupt circuitry, the device may vector to location 03H (External Interrupt 0 vector address). It happens when a low priority interrupt has been in progress for either 1 or 2 machine cycles and Timer/Counter 2 generates a priority 1 interrupt. Therefore, Timer/Counter 2 should only be assigned priority level 0.

If an 8752BH is replacing an 8751H in an existing design, the user should carefully compare both data sheets for DC or AC characteristic differences. Note that the V_{IH} and I_{IH} specifications for the EA pin differ significantly between the 8751H and 8752BH.

7

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} ...−0.5V to +13.0V
Voltage on Any Other Pin to V_{SS} ....−0.5V to +7V
Maximum I_{OL} Per I/O Pin .....15 mA
Power Dissipation.....1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions: T_A (under Bias) = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V

DC CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	V_{SS}	0.7	V	
V_{IH}	Input High Voltage (Except XTAL2, RST, $\overline{EA}$)	2.0	V_{CC}+0.5	V	
V_{IH1}	Input High Voltage XTAL2, RST	2.5	V_{CC}+0.5	V	XTAL1 = V_{SS}
V_{IH2}	Input High Voltage to $\overline{EA}$	4.5	5.5	V	
V_{OL}	Output Low Voltage (Note 3) (Ports 1, 2 and 3)		0.45	V	I_{OL} = 1.6 mA (Note 1)
V_{OL1}	Output Low Voltage (Note 3) (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)		0.45	V	I_{OL} = 3.2 mA (Note 1, 2)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE/$\overline{PROG}$ and $\overline{PSEN}$)	2.4		V	I_{OH} = −80 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4		V	I_{OH} = −400 μA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3 and RST)		−500	μA	V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current ($\overline{EA}$)	−10	500	mA μA	V_{IN} = V_{SS}
I_{IL2}	Logical 0 Input Current (XTAL2)		−3.2	mA	V_{IN} = 0.45V XTAL1 = V_{SS}
I_{LI}	Input Leakage Current (Port 0)		±10	μA	0.45 < V_{IN} < V_{CC}
I_{IH}	Logical 1 Input Current ($\overline{EA}$)		1	mA	4.5V < V_{IN} < 5.5V
I_{IH1}	Input Current to RST to activate Reset		500	μA	V_{IN} < (V_{CC} − 1.5V)
I_{CC}	Power Supply Current		175	mA	All Outputs Disconnected
C_{IO}	Pin Capacitance		10	pF	Test freq = 1 MHz

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE/$\overline{PROG}$ and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE/$\overline{PROG}$ pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. ALE/$\overline{PROG}$ refers to a pin on the device. ALE refers to a timing signal that is output on the ALE/$\overline{PROG}$ pin.
3. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port-
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A:Address
C:Clock
D:Input Data
H:Logic level HIGH
I:Instruction (program memory contents)
L:Logic level LOW, or ALE
P:$\overline{\text{PSEN}}$
Q:Output data
R:$\overline{\text{RD}}$ signal
T:Time
V:Valid
W:$\overline{\text{WR}}$ signal
X:No longer a valid logic level
Z:Float

For example,

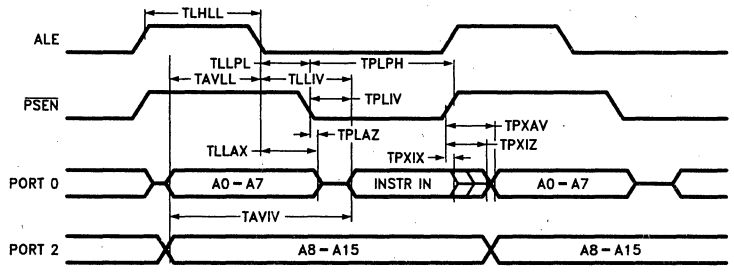
TAVLL = Time from Address Valid to ALE Low.
TLLPL = Time from ALE Low to PSEN Low.

AC CHARACTERISTICS (Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

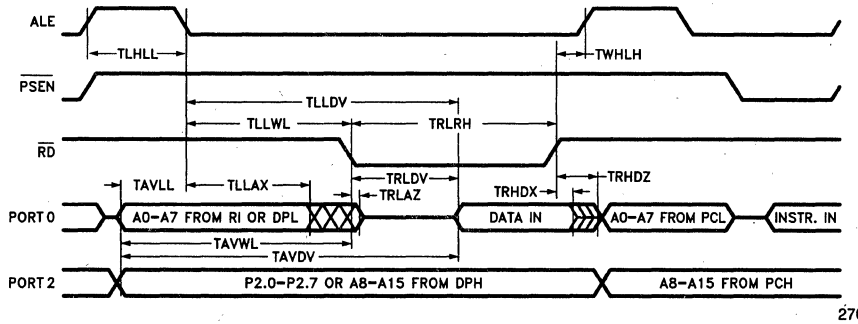
Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12.0	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instruction In		233		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	58		TCLCL−25		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	215		3TCLCL−35		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In		125		3TCLCL−125	ns
TPXIX	Input Instr Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{\text{PSEN}}$		63		TCLCL−20	ns
TPXAV	$\overline{\text{PSEN}}$ to Address Valid	75		TCLCL−8		ns
TAVIV	Address to Valid Instruction In		302		5TCLCL−115	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		20		20	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{\text{WR}}$ Transition	23		TCLCL−60		ns
TQVWH	Data Valid to $\overline{\text{WR}}$ High	433		7TCLCL−150		ns
TWHQX	Data Held After $\overline{\text{WR}}$	33		TCLCL−50		ns
TRLAZ	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



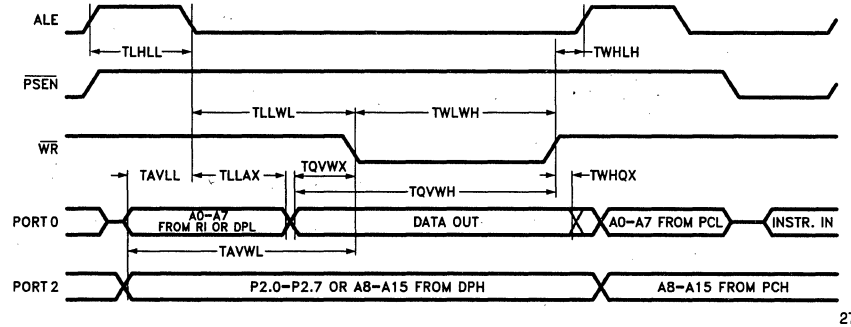
270429-5

EXTERNAL DATA MEMORY READ CYCLE



270429-6

EXTERNAL DATA MEMORY WRITE CYCLE



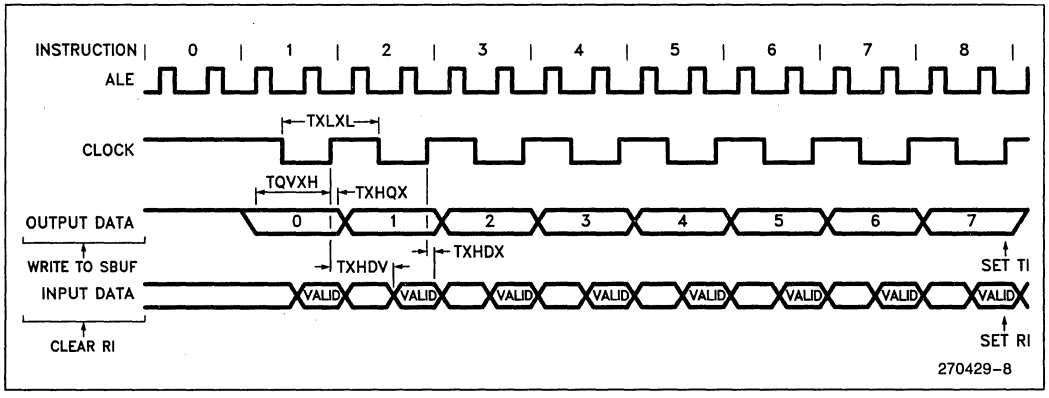
270429-7

SERIAL PORT TIMING—SHIFT REGISTER MODE

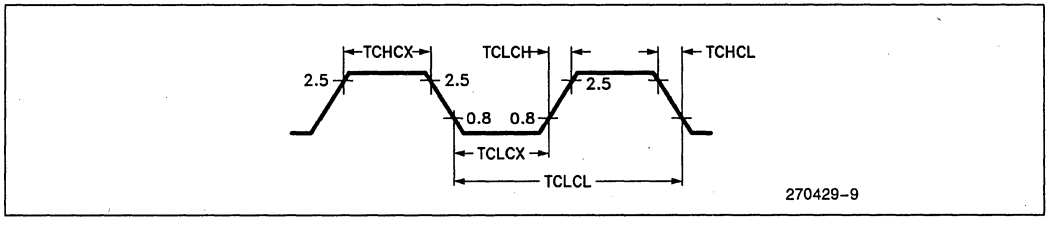
TEST CONDITIONS T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



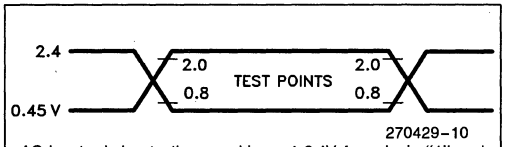
EXTERNAL CLOCK DRIVE WAVEFORMS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

AC TESTING INPUT/OUTPUT WAVEFORMS



270429-10

AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

EPROM CHARACTERISTICS

Table 1 shows the logic levels for programming the Program Memory, the Encryption Table, and the Lock Bits and for reading the signature bytes.

Programming the EPROM

To be programmed, the 8752BH must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.4 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, and RST, $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 1. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally $\overline{EA}/V_{PP}$ is held at a logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches.

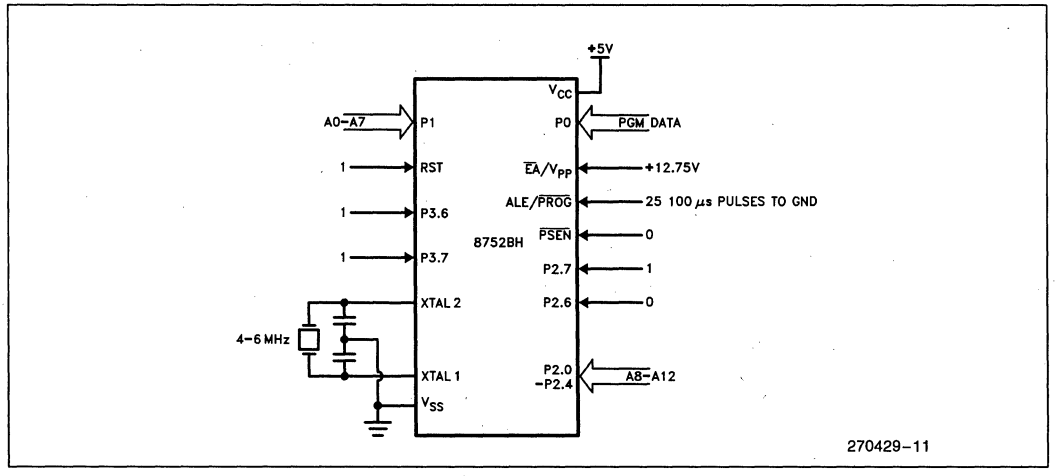


Figure 5. Programming the EPROM

Table 1. EPROM Programming Modes

MODE	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.6	P3.7
Program Code Data	1	0	0*	V_{PP}	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Program Encryption Table Use Addresses 0-1FH	1	0	0*	V_{PP}	1	0	0	1
Program Lock x=1	1	0	0*	V_{PP}	1	1	1	1
Bits (LBx) x=2	1	0	0*	V_{PP}	1	1	0	0
Read Signature	1	0	1	1	0	0	0	0

NOTES:
"1" = Valid high for that pin
"0" = Valid low for that pin
"V_{PP}" = +12.75V ±0.25V
*ALE/$\overline{PROG}$ is pulsed low for 100 uS for programming. (Quick-Pulse Programming)

QUICK-PULSE PROGRAMMING ALGORITHM

The 8752BH can be programmed using the Quick-Pulse Programming Algorithm for microcontrollers. The features of the new programming method are a lower V_{PP} (12.75 volts as compared to 21 volts) and a shorter programming pulse. It is possible to program the entire 8 Kbytes of EPROM memory in less than 25 seconds with this algorithm!

To program the part using the new algorithm, V_{PP} must be 12.75 ±0.25 Volts. ALE/$\overline{PROG}$ is pulsed low for 100 μseconds, 25 times as shown in Figure 6. Then, the byte just programmed may be verified. After programming, the entire array should be verified. The Program Lock features are programmed using the same method, but with the setup as shown in Table 1. The only difference in programming Lock features is that the Lock features cannot be directly verified. Instead, verification of programming is by observing that their features are enabled.

PROGRAM VERIFICATION

If the Lock Bits have not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0 - P2.4. The other pins should be held at the "Verify" levels indicated in Table 1. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation. (If the Encryption Array in the EPROM has been programmed, the data present at Port 0 will be Code Data XNOR Encryption Data. The user must know the Encryption Array contents to manually "unencrypt" the data during verify.)

The setup, which is shown in Figure 7, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active low read strobe.

7

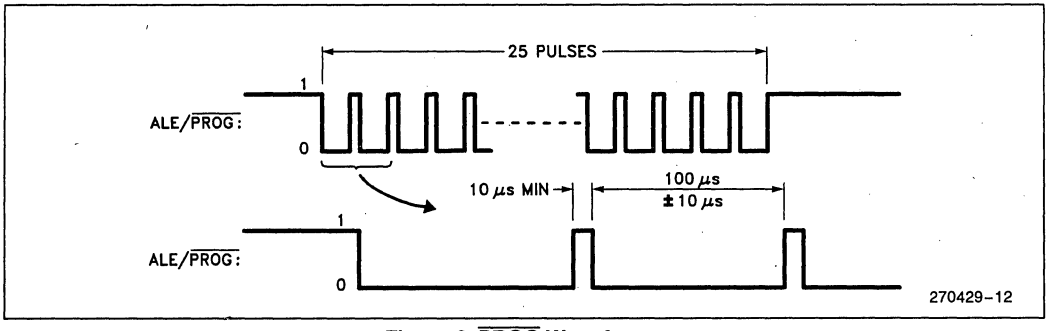


Figure 6. $\overline{PROG}$ Waveforms

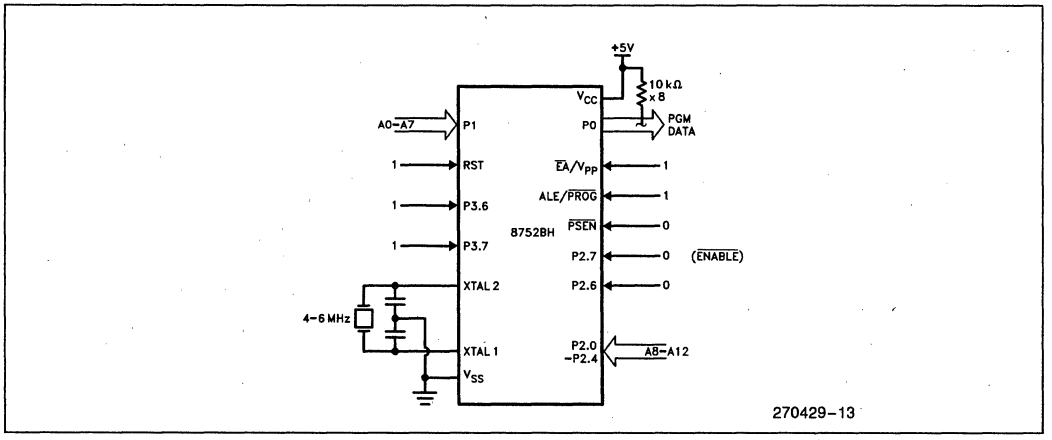


Figure 7. Verifying the EPROM

PROGRAM MEMORY LOCK

The two-level Program Lock system consists of 2 Lock bits and a 32-byte Encryption Array which are used to protect the program memory against software piracy.

ENCRYPTION ARRAY

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte. The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form.

It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

LOCK BITS

Also included in the EPROM Program Lock scheme are two Lock Bits which function as shown in Table 2.

Erasing the EPROM also erases the Encryption Array and the Lock Bits, returning the part to full unlocked functionality.

To ensure proper functionality of the chip, the internally latched value of the $\overline{EA}$ pin must agree with its external state.

Table 2. Lock Bits and their Features

Lock Bits		Logic Enabled
LB1	LB2	
U	U	Minimum Program Lock features enabled. (Code Verify will still be encrypted by the Encryption Array)
P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled
P	P	Same as above, but Verify is also disabled
U	P	Reserved for Future Definition

P = Programmed
U = Unprogrammed

READING THE SIGNATURE BYTES

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values returned are:

(030H) = 89H indicates manufactured by Intel
(031H) = 52H indicates 8752BH

ERASURE CHARACTERISTICS

Erasure of the EPROM begins to occur when the 8752BH is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at lease 15 W-sec/cm. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

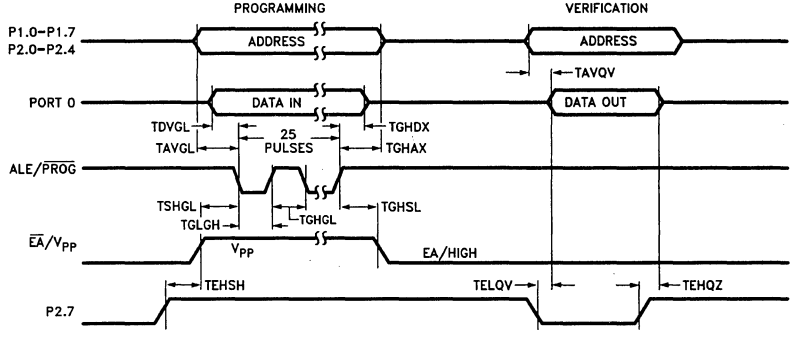
Erasure leaves the array in an all 1s state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C, V_{CC} = 5.0V ±10%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		50	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold After $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold After $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
TGHSL	V_{PP} Hold After $\overline{PROG}$	10		μs
TGLGH	$\overline{PROG}$ Width	90	110	μs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float After $\overline{ENABLE}$	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		μs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



270429-14

DATA SHEET REVISION HISTORY

The following is the key difference between this and the -003 version of the 8752BH data sheet:

Data sheet title was changed from:
8752BH Single-Chip 8-Bit Microcomputer with 8K Bytes of EPROM Program Memory

to:
8752BH Single-Chip 8-Bit Microcontroller with 8 Kbytes of EPROM Program Memory.

The following are the key differences between the -003 and the -002 version of the 8752BH data sheet.

1. Data sheet status changed from "Preliminary" to "Production".
2. Deleted LCC Package offering.
3. Revised Maximum Ratings warning and data sheet status notice.

The following are the key differences between the -002 and the -001 version of the 8752BH data sheet.

1. PLCC pin connection diagram was added.
2. Package table was added.
3. Timer/Counter 2 Design Consideration was added.
4. Design Consideration was added referring to previous designs using the 8751H.
5. Note 3 was added to DC Characteristics to explain the maximum current specification.
6. Signature Byte was corrected.
7. Data Sheet Revision History was added.

8752BH

EXPRESS

■ **Extended Temperature Range** ■ **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in, and an extended temperature range with or without burn-in.

With the commercial standard temperature range operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic, for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS T_A = −40°C to +85°C; V_{CC} = 5V ±10%; V_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input High Voltage (Except XTAL2, RST, $\overline{EA}$)	2.1	V_{CC} + 0.5	V	

7

January 1989
Order Number: 270650-002

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	plastic	commercial	no
D	cerdip	commercial	no
N	PLCC	commercial	no
R	LCC	commercial	no
TD	cerdip	extended	no
QP	plastic	commercial	yes
LD	cerdip	extended	yes

Please note:

- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-in is dynamic, for a minimum time of 160 hours at 125°C, V_{CC} = 5.5V ±0.25V, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples: N8752BH indicates 8752BH in a PLCC package and specified for commercial temperature range, without burn-in. LD8752BH indicates 8752BH in a cerdip package and specified for extended temperature range with burn-in.

DATA SHEET REVISION SUMMARY

The following are the key differences between this and the -001 version of the 8752BH Express data sheet:

1. V_{IH} parameter changed to read "(Except XTAL2, RST, $\overline{EA}$)".
2. QD option removed.
3. Data Sheet Revision Summary added.

80C31BH/80C51BH

EXPRESS

- **Extended Temperature Range**
- **Burn-In**
- **3.5 to 12 MHz V_{CC} = 5V ±20%**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here. This data sheet is valid in conjunction with the commercial 80C51BH/80C31BH data sheet, 270064-008.

September 1990
Order Number: 270218-003

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 20\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
V_{IL}	Input Low Voltage (Except EA)	-0.5	$0.2V_{CC} - 0.15$	V	
V_{IL1}	EA	$-0.5V$	$0.2V_{CC} - 0.35$	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	$0.2V_{CC} + 1$	$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage to XTAL1, RST	$0.7V_{CC} + 0.1$	$V_{CC} + 0.5$	V	
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)		-75	μA	$V_{in} = 0.45V$
I_{TL}	Logical 1 to 0 transition Current (Ports 1, 2, 3)		-750	μA	$V_{in} = 2.0V$

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD	Cerdip	Extended	No
TN	PLCC	Extended	No
QP	Plastic	Commercial	Yes
QD	Cerdip	Commercial	Yes
QN	PLCC	Commercial	Yes
LP	Plastic	Extended	Yes
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

NOTE:
- Commercial temperature range is 0°C to 70°C. Extended temperature range is $-40°C$ to $+85°C$.
- Burn-in is dynamic for a minimum time of 160 hours at 125°C, $V_{CC} = 6.9V \pm 0.25V$, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples:

P80C31BH indicates 80C31BH in a plastic package and specified for commercial temperature range, without burn-in.
LD80C51BH indicates 80C51BH in a cerdip package and specified for extended temperature range with burn-in.

DATA SHEET REVISION HISTORY

The following are the key differences between this and the -002 version of the 80C31BH/80C51BH express data sheet:

1. Data sheet status changed from "Preliminary" to "Production".
2. Added this revision history.

80C51BHP
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH PROTECTED ROM

80C51BHP—3.5–12 MHz, V_{CC} = 5V ± 20%
80C51BHP-1—3.5–16 MHz, V_{CC} = 5V ± 20%
80C51BHP-2—0.5–12 MHz, V_{CC} = 5V ± 20%

- **Power Control Modes**
- **128 x 8-Bit RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **4K Program Memory Space**
- **Protection Feature Protects ROM Parts Against Software Piracy**
- **High Performance CHMOS Process**
- **Boolean Processor**
- **5 Interrupt Sources**
- **Programmable Serial Port**
- **4K Data Memory Space (Expandable to 64K)**
- **ONCE (On-Circuit Emulation) Mode**

The MCS®-51 family of CHMOS products is fabricated on Intel's CHMOS III process and is functionally compatible with the standard 8051 HMOS and EPROM products. CHMOS III is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. This combination expands the effectiveness of the powerful 8051 architecture and instruction set.

Like the 8051 HMOS versions, the 80C51BHP has the following features: 4 Kbytes of ROM; 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry. In addition, the 80C51BHP has two software selectable modes of reduced activity for further power reduction—Idle and Power Down.

The Idle mode freezes the CPU while allowing the RAM, timer/counters serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The 80C51BHP is identical to the 80C51BH with the exception of the Protection Feature. To incorporate this Protection Feature, program verification has been disabled and external memory accesses have been limited to 4K.

September 1992
Order Number: 270603-004

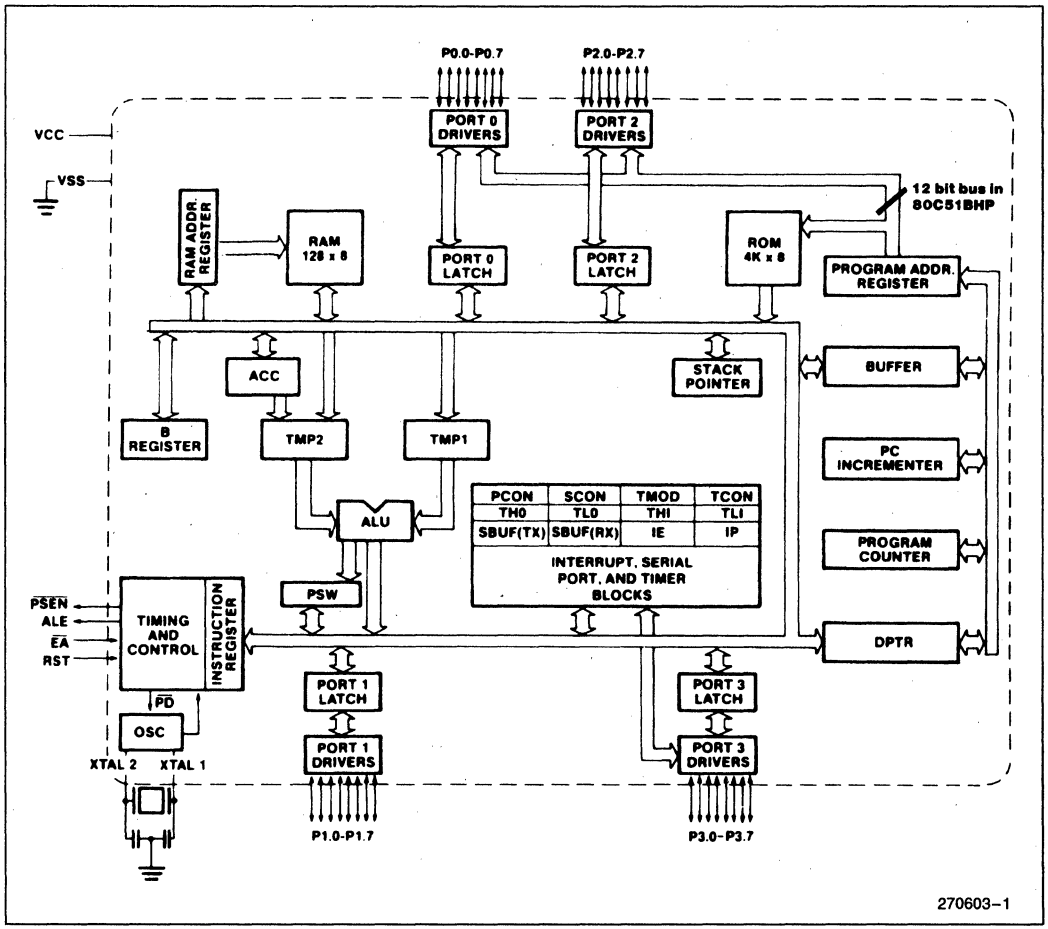


Figure 1. Block Diagram

IDLE MODE

In the Idle mode, the CPU puts itself to sleep while all the on chip peripherals stay active. The instruction that invokes the Idle mode is the last instruction executed in the normal operating mode before Idle mode is activated. The content of the on-chip RAM and all the Special Function Registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor the same as a power on reset.

POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

The only exit from Power Down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

The control bits for the reduced power modes are in the Special Function Register PCON.

NOTE:
For more detailed information on these reduced power modes refer to Application Note AP-252, "Designing with the 80C51BH".

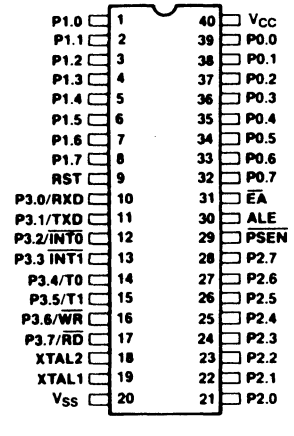
ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 80C51BHP without removing the device from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

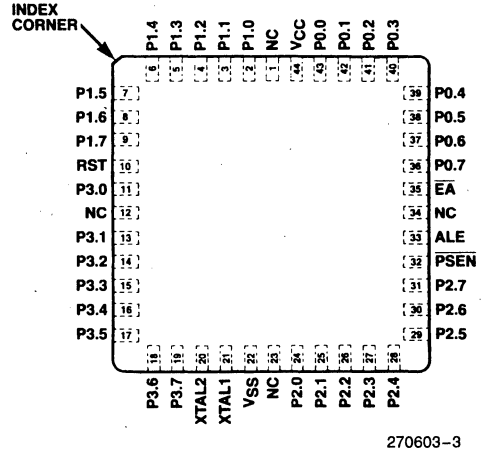
Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data



270603-2

Pin (PDIP)



270603-3

Pad (PLCC)

Figure 2. Connection Diagrams

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 80C51BHP is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

PACKAGES

Part	Prefix	Package Type
80C51BHP	P N	40-Pin Plastic DIP 44-Pin PLCC

PIN DESCRIPTIONS

V_{CC}

Supply voltage during normal, Idle, and Power Down operations.

V_{SS}

Circuit ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. In the 80C51BHP, Bits 2.4 through 2.7 are forced to 0, effectively limiting external data and code space to 4K each during external accesses (see Design Considerations). During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits Power-On reset using only an external capacitor to V_{CC}.

ALE

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$

Program Store Enable is the read strobe to external Program Memory.

When the device is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.

$\overline{EA}$

External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations starting at 0000H up to FFFFH. If $\overline{EA}$ is strapped to V_{CC} the device executes from internal Program Memory unless the program counter contains an address greater than 0FFFH.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock generator circuits.

XTAL2

Output from the inverting oscillator amplifier.

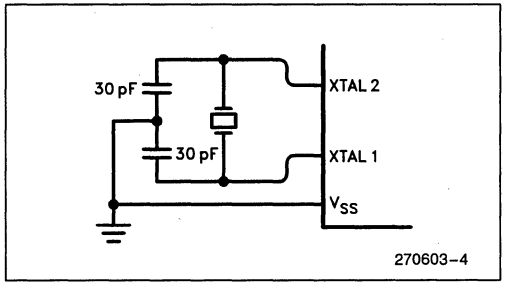


Figure 3. Crystal Oscillator

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillator for Microcontrollers".

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

Design Considerations

- The 80C51BHP cannot access external Program or Data memory above 4K. This means that the following instructions that use the Data Pointer only read/write data at address locations below 0FFFH:

  MOVX A, @DPTR
  MOVX @DPTR, A

  When the Data Pointer contains an address above the 4K limit, those locations will not be accessed. To access Data Memory above 4K, the MOVX @Ri, A or MOVX A, @Ri instructions must be used.
- Before entering the Power Down mode the contents of the Carry Bit and B.7 must be equal.
- When the Idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

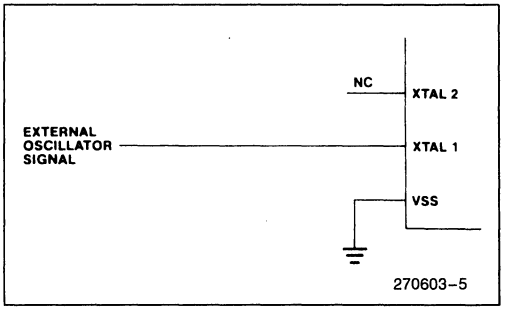


Figure 4. External Drive Configuration

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on any
Pin to V_{SS} .....−0.5V to V_{CC} +0.5V
Voltage on V_{CC} to V_{SS} .....−0.5V to 6.5V
Maximum I_{OL} per I/O Pin .....15 mA
Power Dissipation.....1.0W*

*This value is based on the maximum allowable die temperature and the thermal resistance of the package.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions: T_A (Under Bias) = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V

DC CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Min	Typ(3)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$)	−0.5		0.2 V_{CC} −0.1	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$)	−0.5		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (6) (Ports 1, 2, 3)			0.45	V	I_{OL} = 1.6 mA (1)
V_{OL1}	Output Low Voltage (6) (Port 0, ALE, $\overline{PSEN}$)			0.45	V	I_{OL} = 3.2 mA (1)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	2.4			V	I_{OH} = −60 μA V_{CC} = 5V ±10%
		0.75 V_{CC}			V	I_{OH} = −25 μA
		0.9 V_{CC}			V	I_{OH} = −10 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I_{OH} = −800 μA V_{CC} = 5V ±10%
		0.75 V_{CC}			V	I_{OH} = −300 μA
		0.9 V_{CC}			V	I_{OH} = −80 μA (2)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)			−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)			−650	μA	V_{IN} = 2V
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)			±10	μA	0.45 < V_{IN} < V_{CC}
RRST	Reset Pulldown Resistor	50		150	KΩ	
CIO	Pin Capacitance			10	pF	Test Freq = 1 MHz, T_A = 25°C
I_{CC}	Power Supply Current:					
	Active Mode, 12 MHz (4)		11	20	mA	
	Idle Mode, 12 MHz (4)		1.7	5	mA	(5)
	Power Down Mode		5	50	μA	

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OLS} of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.
3. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temperature, 5V.
4. ICCMAX at other frequencies is given by
   Active Mode: ICCMAX = 1.47 × FREQ + 2.35
   Idle Mode: ICCMAX = 0.33 × FREQ + 1.05
where FREQ is the external oscillator frequency in MHz. ICCMAX is given in mA. See Figure 5.
5. See Figures 6 through 9 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per Port Pin:	10 mA
Maximum I_{OL} per 8-Bit Port —	
Port 0:	26 mA
Ports 1, 2 and 3:	15 mA
Maximum Total I_{OL} for all output pins:	71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

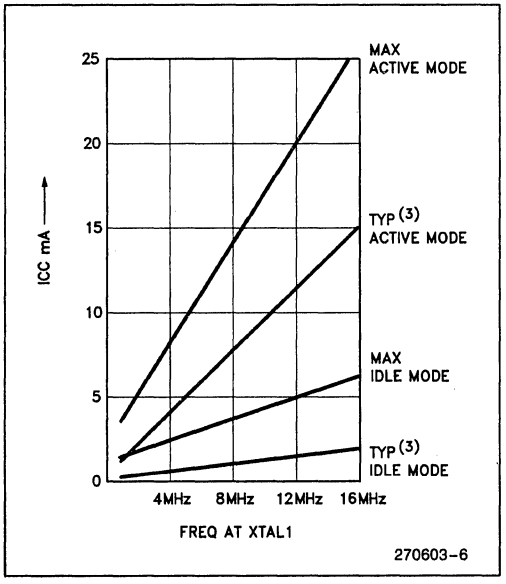


Figure 5. I_{CC} vs. Frequency
Valid only within frequency specifications of the device under test.

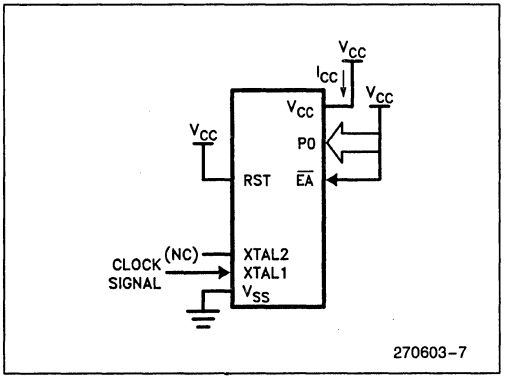


Figure 6. I_{CC} Test Condition, Active Mode
All other pins are disconnected.

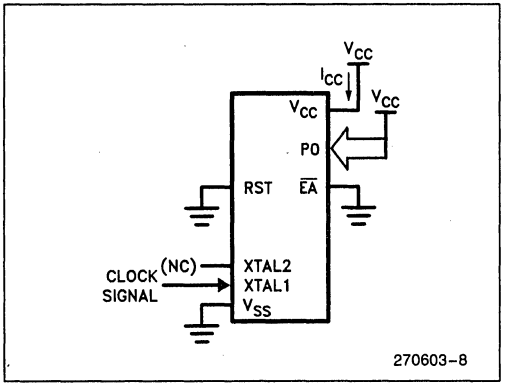


Figure 7. I_{CC} Test Condition, Idle Mode
All other pins are disconnected.

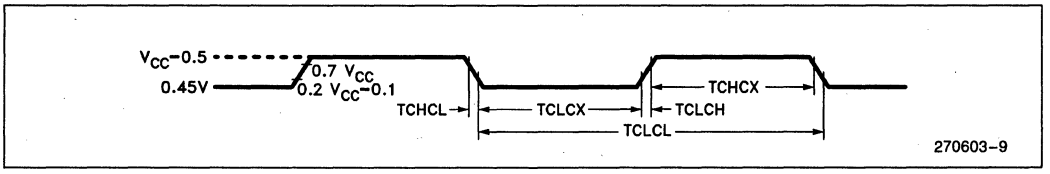


Figure 8. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

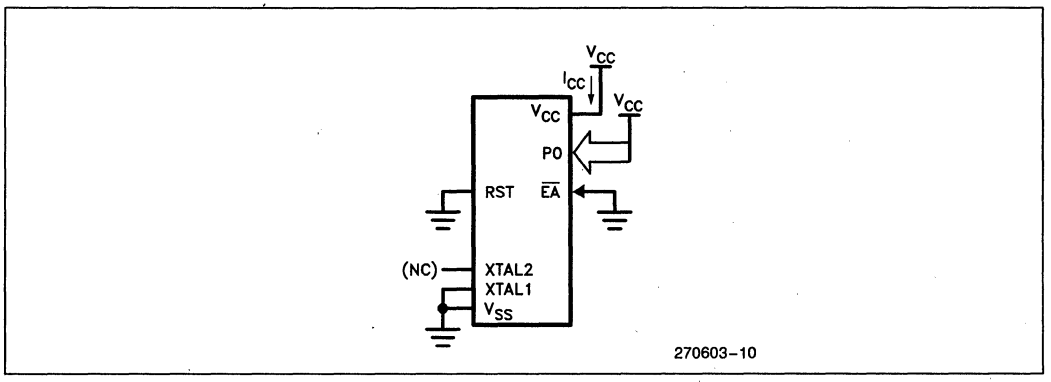


Figure 9. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected. V_{CC} = 2V to 6V

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address.
C: Clock.
D: Input data.
H: Logic level HIGH.
I: Instruction (program memory contents).
L: Logic level LOW, or ALE.
P: $\overline{\text{PSEN}}$.
Q: Output data.
R: $\overline{\text{RD}}$ signal.
T: Time.
V: Valid.
W: $\overline{\text{WR}}$ signal.
X: No longer a valid logic level.
Z: Float.

EXAMPLE:

TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{\text{PSEN}}$ Low.

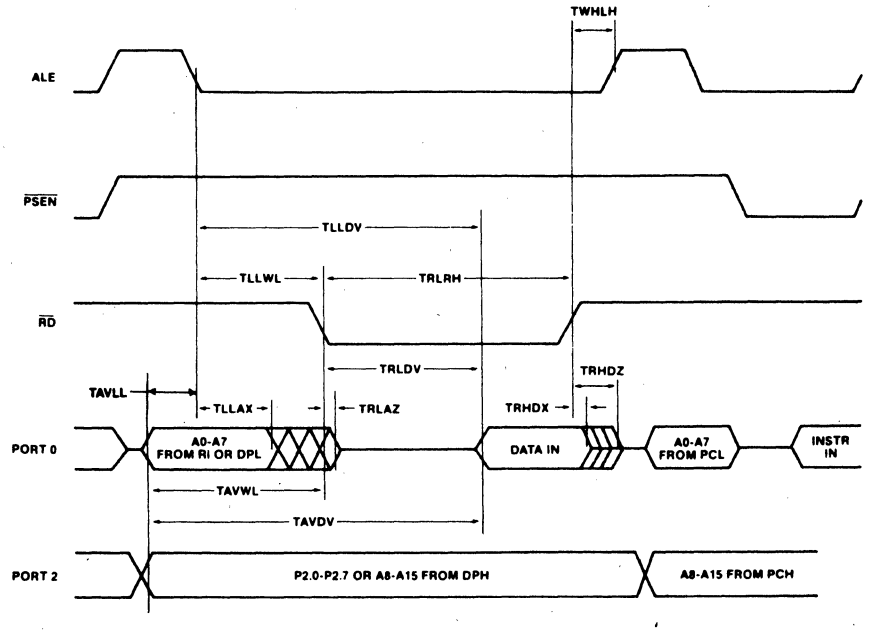
AC CHARACTERISTICS

(Under Operating Conditions: Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 80C51BH/80C31BH 80C51BH-1/80C31BH-1 80C51BH-2/80C31BH-2			 3.5 3.5 0.5	 12 16 12	MHz
TLHLL	ALE Pulse Width	127		2TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	28		TCLCL − 55		ns
TLLAX	Address Hold After ALE Low	48		TCLCL − 35		ns
TLLIV	ALE Low to Valid Instr In		234		4TCLCL − 100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	43		TCLCL − 40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL − 45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		145		3TCLCL − 105	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		59		TCLCL − 25	ns
TAVIV	Address to Valid Instr In		312		5TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL − 165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL − 70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL − 150	ns
TAVDV	Address to Valid Data In		585		9TCLCL − 165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL − 50	3TCLCL + 50	ns
TAVWL	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL − 130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	23		TCLCL − 60		ns
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL − 50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL − 40	TCLCL + 40	ns

EXTERNAL DATA MEMORY READ CYCLE



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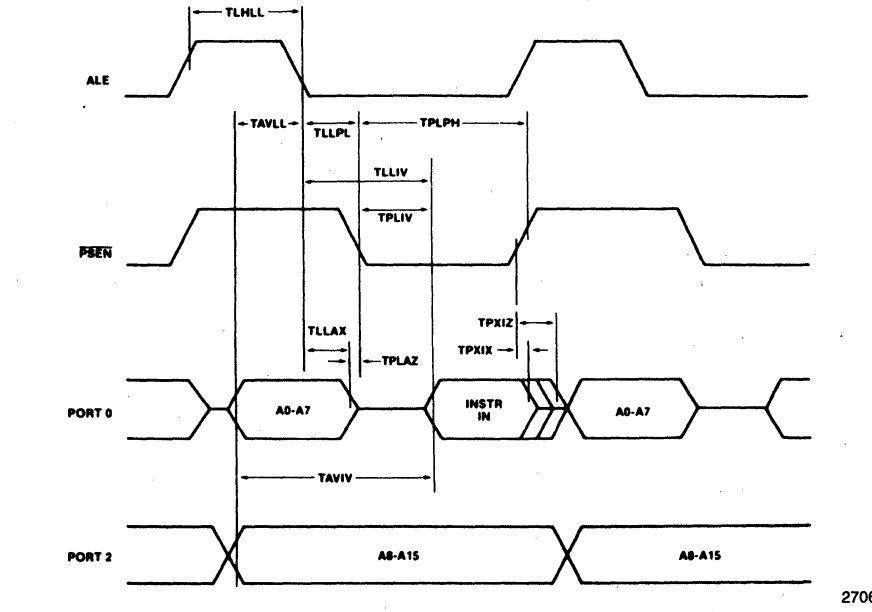
EXTERNAL PROGRAM MEMORY READ CYCLE



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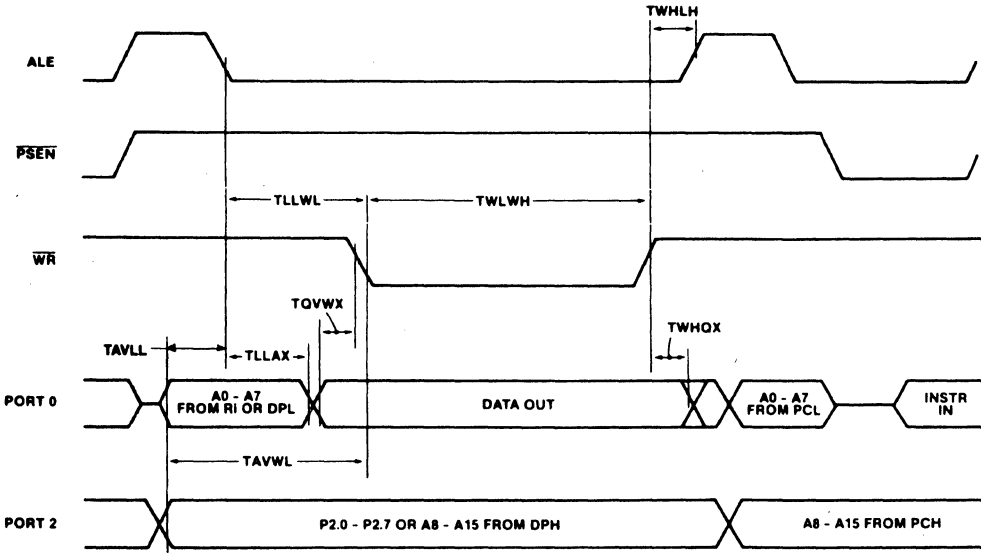
EXTERNAL DATA MEMORY WRITE CYCLE



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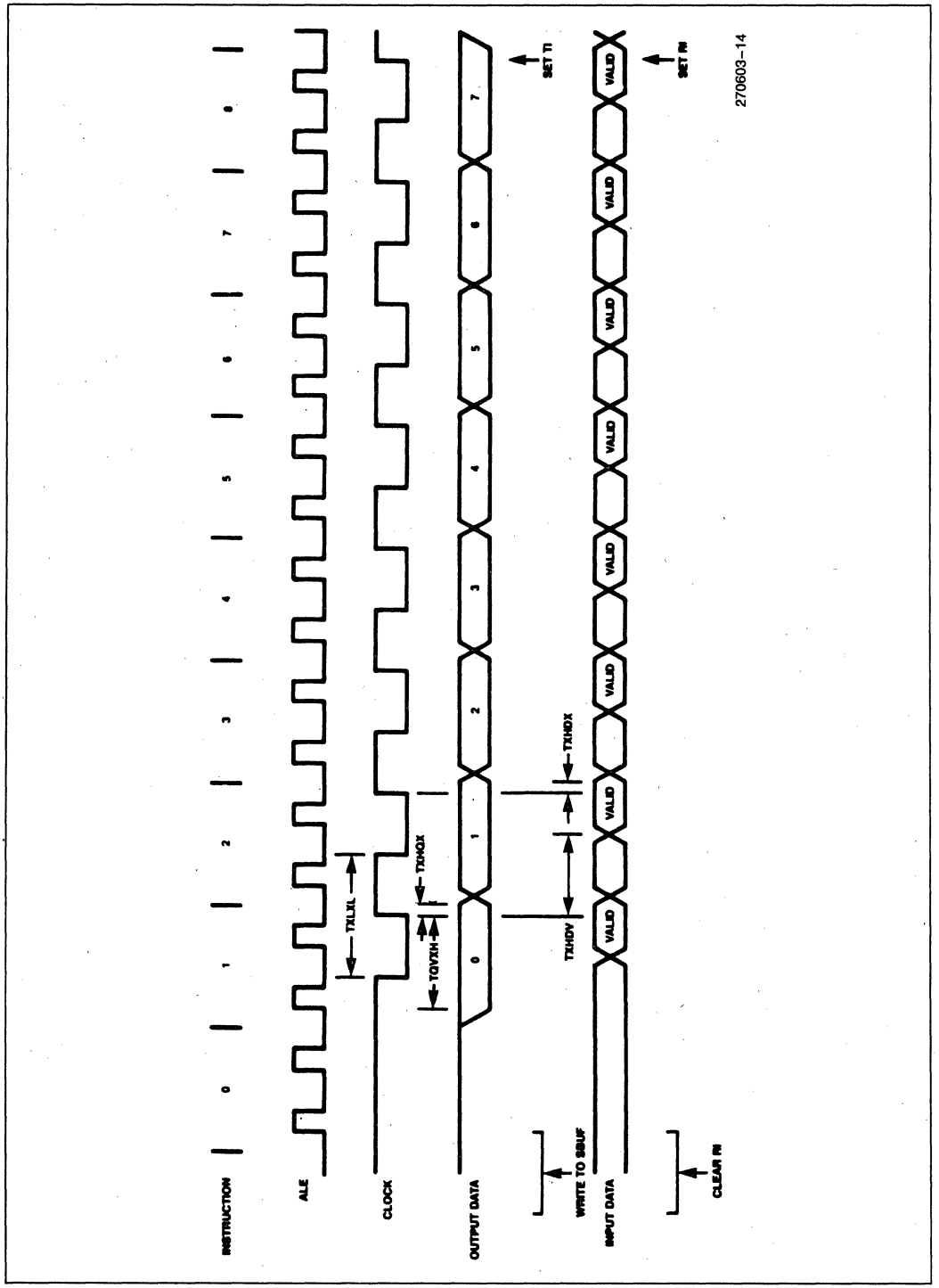


Shift Register Mode Timing Waveforms

EXTERNAL CLOCK DRIVE

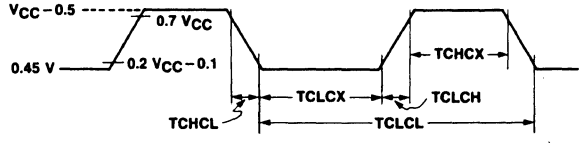
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 80C51BHP 80C51BHP-1 80C51BHP-2	 3.5 3.5 0.5	 12 16 12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

SERIAL TIMING—SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to 70°C; V_{CC} = 5V ±20%; V_{SS} = 0V; Load Capacitance = 80 pF

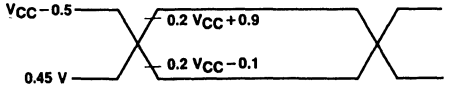
Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL − 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL − 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL − 133	ns

EXTERNAL CLOCK DRIVE WAVEFORM



270603-15

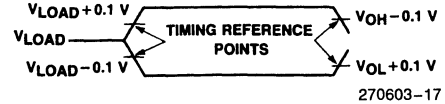
AC TESTING INPUT, OUTPUT WAVEFORMS



270603-16

AC Inputs during testing are driven at V_{CC} − 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at V_{IH} min. for a logic "1" and V_{IL} max. for a logic "0".

FLOAT WAVEFORMS



270603-17

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

7

DATA SHEET REVISION HISTORY

The following is the key difference between this and the -003 version of the 80C51BHP data sheet:

Data sheet title was changed from:
80C51BHP CHMOS Single-Chip 8-Bit Microcomputer with Protected ROM

to:
80C51BHP CHMOS Single-Chip 8-Bit Microcontroller with Protected ROM

The following are the key differences between the -003 and the -002 version of the 80C51BHP data sheet:

1. Data sheet status changed from "Preliminary" to "Production".
2. Revised Maximum Ratings Warning and Data Sheet Status Notice.
3. ONCE Mode feature added.

The following are the key differences between the -002 and the -001 version of the 80C51BHP data sheet:

1. Package Table was added.
2. Note 6 on Maximum Current Specifications was added to DC Characteristics.
3. Data Sheet Revision History was added.

87C51/80C51BH/80C31BH
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 4 KBYTES INTERNAL PROGRAM MEMORY

87C51/80C51BH/80C31BH—3.5 to 12 MHz, V_{CC} = 5V ±20%
87C51-1/80C51BH-1/80C31BH-1—3.5 to 16 MHz, V_{CC} = 5V ±20%
87C51-2/80C51BH-2/80C31BH-2—0.5 to 12 MHz, V_{CC} = 5V ±20%
87C51-L—3.5 MHz to 8 MHz, V_{CC} = 3.3V ±0.3V

- High Performance CHMOS EPROM
- Low Voltage Operation (-L Only)
- Improved Quick-Pulse Programming Algorithm
- 3-Level Program Memory Lock
- Boolean Processor
- 128-Byte Data RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 5 Interrupt Sources
- Programmable Serial Port
- TTL- and CMOS-Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- Idle and Power Down Modes
- ONCE Mode Facilitates System Testing
- Power Control Modes

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 4 Kbytes of the program memory can reside on-chip (except 80C31BH). In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 128 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C51 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. The Intel 80C51BH/80C31BH is fabricated on CHMOS III technology. Being a member of the MCS®-51 family, the 87C51/80C51BH/80C31BH uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products.

Applications that require low voltage can use the 87C51-L. The 87C51-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz.

The extremely low operating power, along with the two reduced power modes, Idle and Power Down, make this part very suitable for low power applications. The Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

For the remainder of this document, the 87C51, 80C51BH, and 80C31BH will be referred to as the 87C51/BH, unless information applies to a specific device.

October 1992
Order Number: 270147-008

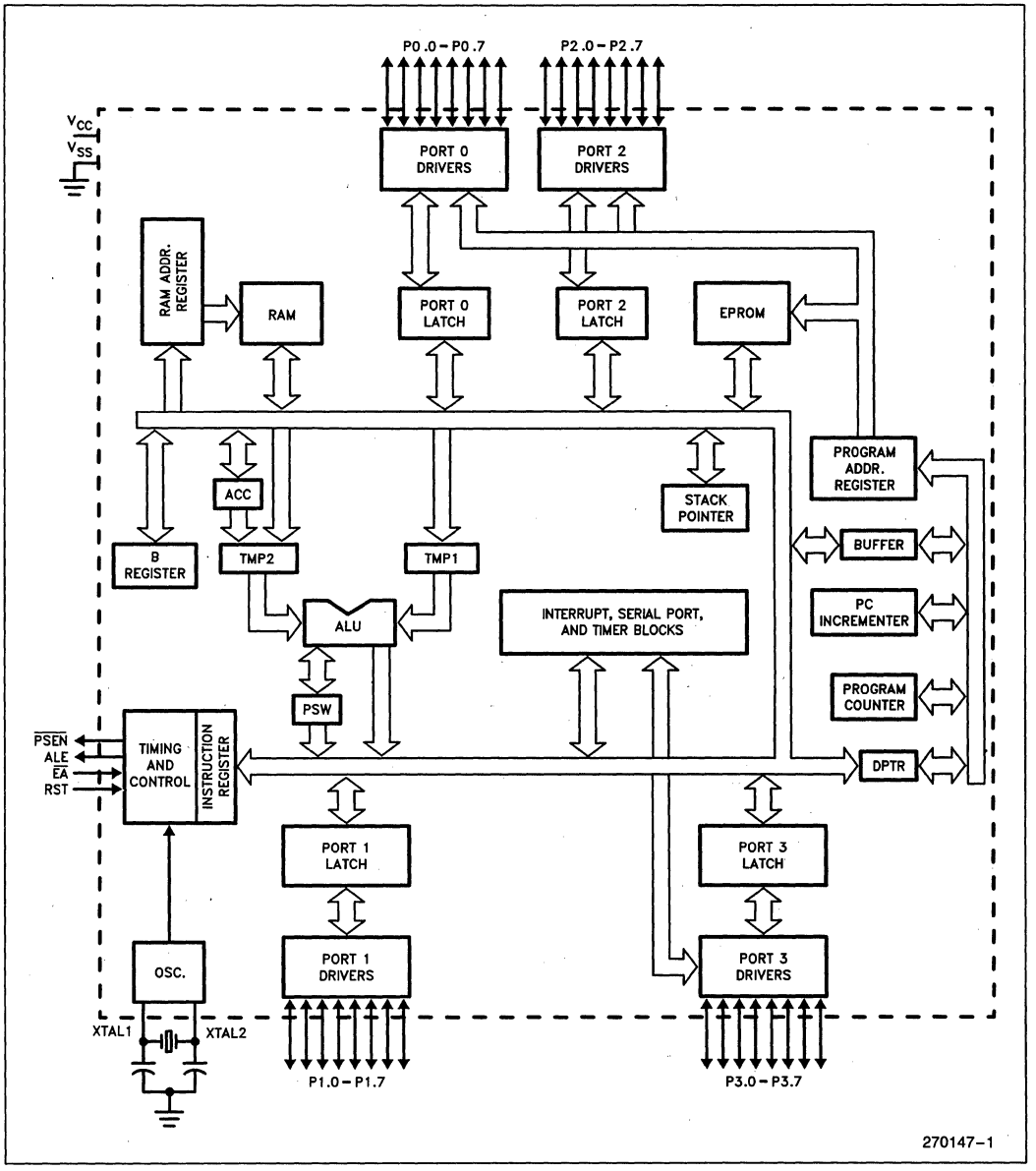


Figure 1. 87C51/BH Block Diagram

PROCESS INFORMATION

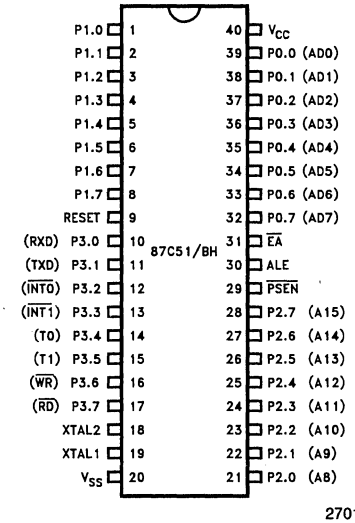
The 87C51 is manufactured on P629.0, a CHMOS III-E process. The 80C51BH/80C31BH are manufactured on P645, a CHMOS III process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
87C51	P	40-Pin Plastic DIP (OTP)	45°C/W	16°C/W
	D	40-Pin CERDIP (EPROM)	45°C/W	15°C/W
	N	44-Pin PLCC (OTP)	46°C/W	16°C/W
	S	44-Pin QFP (OTP)	98°C/W	24°C/W

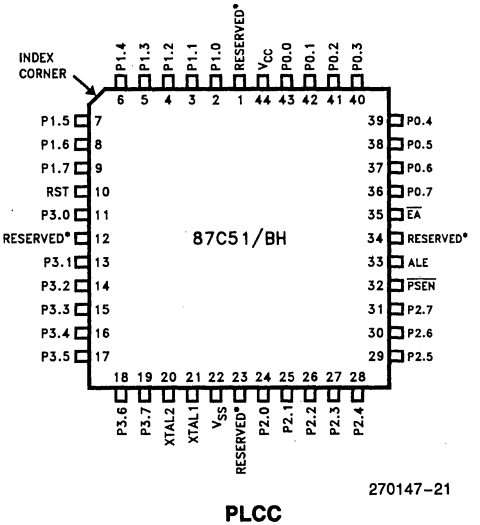
Part	Prefix	Package Type	θ_{ja}	θ_{jc}
80C51BH/ 80C31BH	P	40-Pin Plastic DIP	75°C/W	23°C/W
	D	40-Pin CERDIP	36°C/W	13°C/W
	N	44-Pin PLCC	46°C/W	16°C/W
	S	44-Pin QFP	98°C/W	24°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



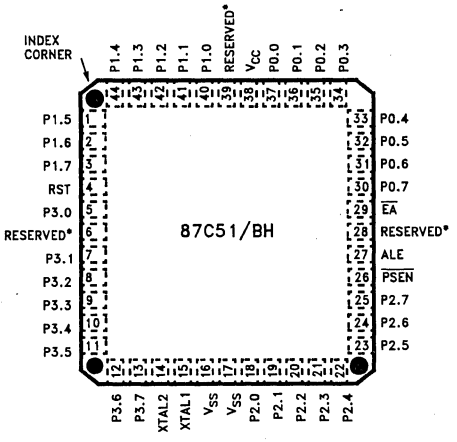
270147-2

DIP



270147-21

PLCC



270147-22

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTION

V_{CC}: Supply voltage during normal, Idle and Power Down operations.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1's.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's.

During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives some control signals and the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Pin	Name	Alternate Function
P3.0	RXD	Serial input line
P3.1	TXD	Serial output line
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 external input
P3.5	T1	Timer 1 external input
P3.6	$\overline{WR}$	External Data Memory Write strobe
P3.7	$\overline{RD}$	External Data Memory Read strobe

Port 3 also receives some control signals for EPROM programming and program verification.

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not (87C51 only). An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE/$\overline{PROG}$: Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$: Program Store Enable is the Read strobe to External Program Memory. When the 87C51/BH is executing from Internal Program Memory, $\overline{PSEN}$ is inactive (high). When the device is executing code from External Program Memory, $\overline{PSEN}$ is activated

twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the 87C51/BH to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits is programmed, the logic level at $\overline{EA}$ is internally latched during reset.

$\overline{EA}$ must be strapped to V_{CC} for internal program execution.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

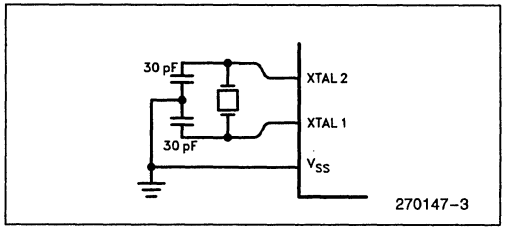


Figure 3. Using the On-Chip Oscillator

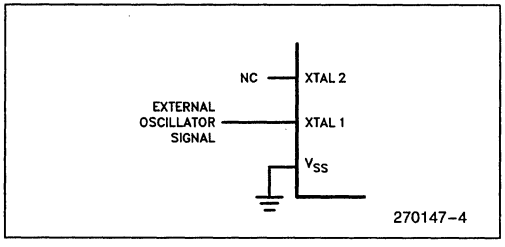


Figure 4. External Clock Drive

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the Special Functions Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when Idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

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Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

The only exit from Power Down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

DESIGN CONSIDERATIONS

- The 87C51-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz. Operating beyond these specifications could cause improper device functionality. (To program the 87C51-L, follow the same procedure as the 87C51.)
- Exposure to light when the device is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window when the die is exposed to ambient light.
- The 87C51 has some additional features that are not available on the 80C51BH/80C31BH. The features are: asynchronous port reset, 4 interrupt priority levels, power off flag, ALE disable, serial port automatic address recognition, serial port framing error detection, 64-byte encryption array, and 3 program lock bits. These features cannot be used with the 80C51BH/80C31BH.

ONCE MODE

The ONCE ("On-Circuit Emulation") mode facilitates testing and debugging of systems using the 87C51/BH without the 87C51/BH having to be removed from the circuit. The ONCE mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 87C51BH is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
Maximum I_{OL} per I/O Pin ..... 15 mA
Power Dissipation..... 1.5W
(Based on package heat transfer limitations, not device power consumption).

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

OPERATING CONDITIONS

T_A (under Bias) = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V (87C51-L, V_{CC} = 3.3V ±0.3V)

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage(6) (Ports 1, 2, 3)			0.3	V	I_{OL} = 100 μA(2)
				0.45	V	I_{OL} = 1.6 mA(2)
				1.0	V	I_{OL} = 3.5 mA(2)
V_{OL1}	Output Low Voltage(6) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA(2)
				0.45	V	I_{OL} = 3.2 mA (2)
				1.0	V	I_{OL} = 7.0 mA(2)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$) 87C51	V_{CC} − 0.3			V	I_{OH} = −10 μA(3)
		V_{CC} − 0.7			V	I_{OH} = −30 μA(3)
		V_{CC} − 1.5			V	I_{OH} = −60 μA(3)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$) 80C51BH/31BH	0.9 V_{CC}			V	I_{OH} = −10 μA(3) V_{CC} = 5V ±10%
		0.75 V_{CC}			V	I_{OH} = −25 μA
		2.4			V	I_{OH} = −60 μA(3)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) 87C51	V_{CC} − 0.3			V	I_{OH} = −200 μA(3)
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA(3)
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA(3)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) 80C51BH/31BH	0.9 V_{CC}			V	I_{OH} = −80 μA V_{CC} = 5V ±10%
		0.75 V_{CC}			V	I_{OH} = −300 μA
		2.4			V	I_{OH} = −800 μA

7

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)			−50	μA	V_{IN} = 2V (87C51) V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			−650	μA	V_{IN} = 2V
RRST	RST Pulldown Resistor	50		300	KΩ	
C_{IO}	Pin Capacitance		10		pF	@ 1 MHz, 25°C
I_{CC}	Power Supply Current Active Mode 87C51-L at 8 MHz All Others at 12 MHz(4) Idle Mode @ 12 MHz(4) Power Down Mode		 11.5 1.7 5	 12 20 5 50	 mA mA mA μA	(Note 5)

NOTES:
1. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temp, 5V.
2. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. I_{CC}MAX at other frequencies is given by:

$$\text{Active Mode: } I_{CC}MAX = 0.94 \times FREQ + 13.71$$

$$\text{Idle Mode: } I_{CC}MAX = 0.14 \times FREQ + 2.31$$

where FREQ is the external oscillator frequency in MHz. I_{CC}MAX is given in mA. See Figure 5.
5. See Figures 6 through 9 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port—
Port 0: 26 mA
Ports 1, 2, and 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
Pins are not guaranteed to sink greater than the listed test conditions.

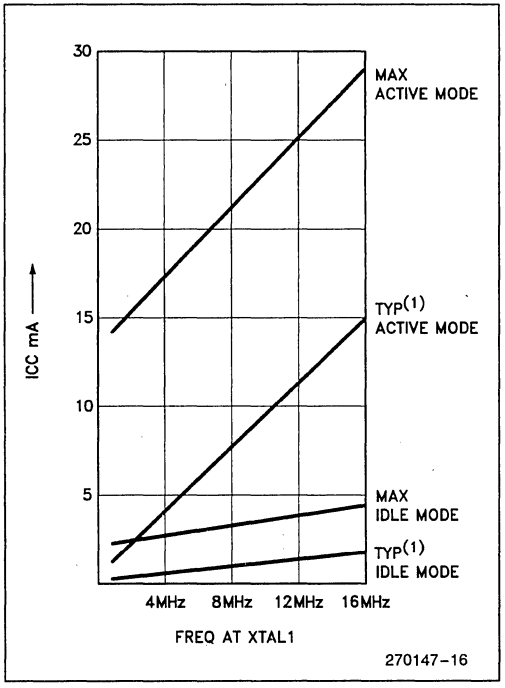


Figure 5. I_{CC} vs. FREQ. Valid only within frequency specifications of the device under test.

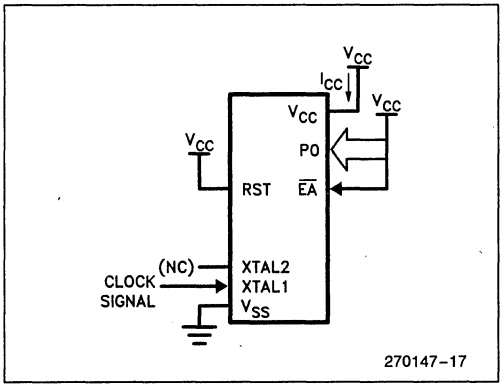


Figure 6. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

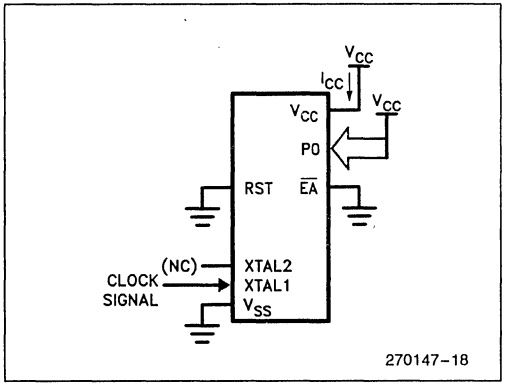


Figure 7. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

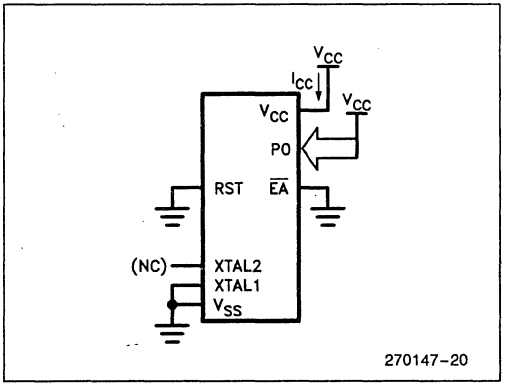


Figure 9. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected. V_{CC} = 2V to 5.5V.

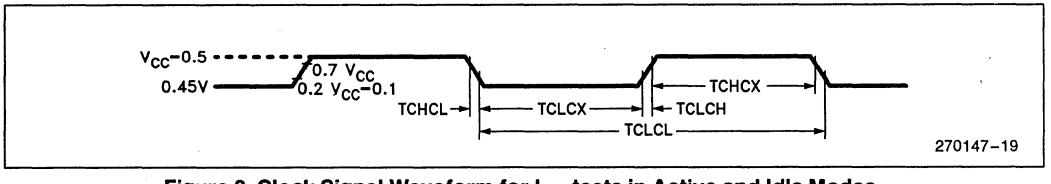


Figure 8. Clock Signal Waveform for I_{CC} tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A:Address.
C:Clock.
D:Input data.
H:Logic level HIGH.
I:Instruction (program memory contents).
L:Logic level LOW, or ALE.
P:$\overline{PSEN}$.
Q:Output data.
R:$\overline{RD}$ signal.
T:Time.
V:Valid.
W:$\overline{WR}$ signal.
X:No longer a valid logic level.
Z:Float.

For example,

TAVLL = Time from Address Valid to ALE Low.
TLLPL = Time from ALE Low to PSEN Low.

AC CHARACTERISTICS: (Over Operating Conditions; Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

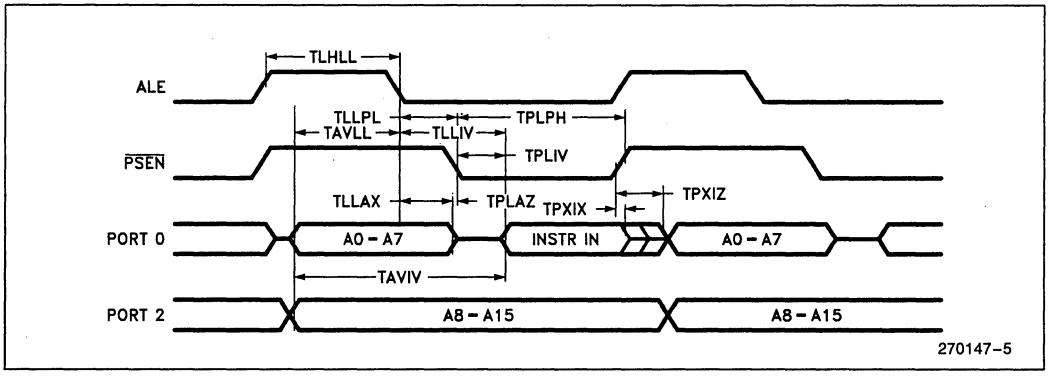
EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 87C51/BH 87C51-1/BH-1 87C51-2/BH-2			 3.5 3.5 0.5	 12 16 12	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low 87C51 80C51BH/C31BH	 43 28		 TCLCL−40 TCLCL−55		 ns ns
TLLAX	Address Hold After ALE Low 87C51 80C51BH/C31BH	 53 48		 TCLCL−30 TCLCL−35		 ns ns
TLLIV	ALE Low to Valid Instr In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low 87C51 80C51BH/C31BH	 53 43		 TCLCL−30 TCLCL−40		 ns ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		145		3TCLCL−105	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instr In		312		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns

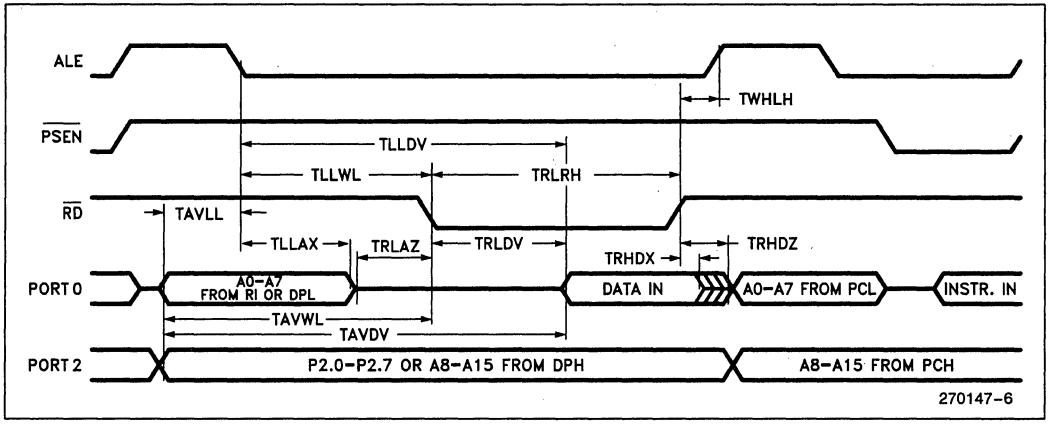
EXTERNAL MEMORY CHARACTERISTICS (Continued)

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TRHDZ	Data Float After $\overline{RD}$					
	87C51		107		2TCLCL−60	ns
	80C51BH/C31BH		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition					
	87C51	33		TCLCL−50		ns
	80C51BH/C31BH	23		TCLCL−60		ns
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

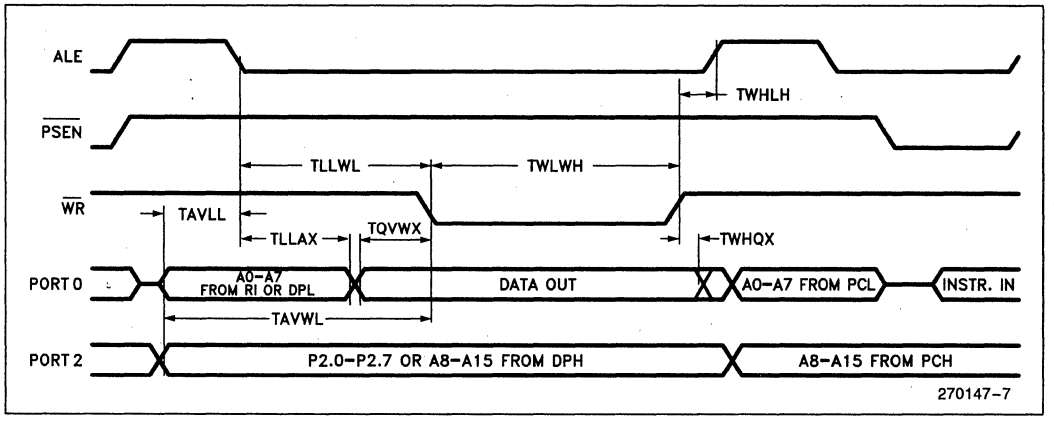
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



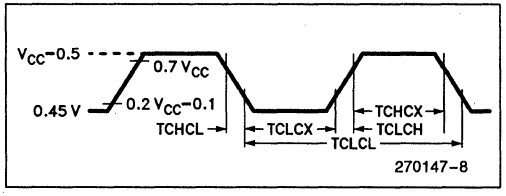
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency			
	87C51/BH	3.5	12	MHz
	87C51-1/BH-1	3.5	16	
	87C51-2/BH-2	0.5	12	
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

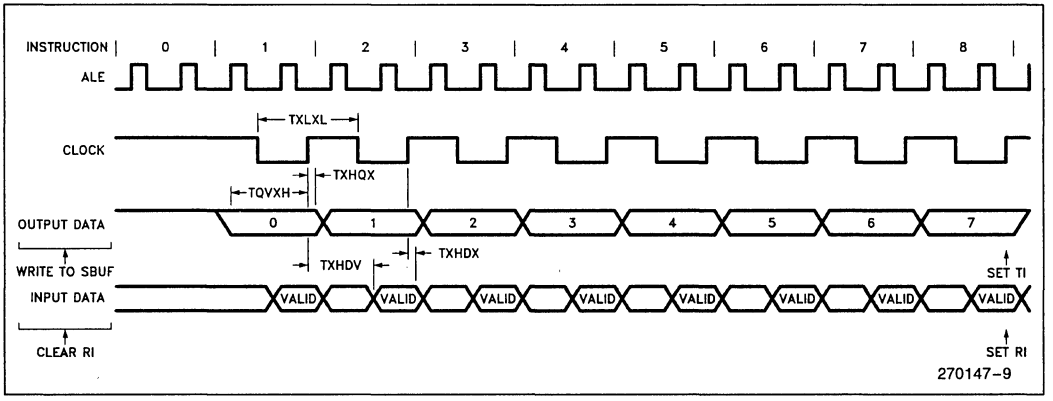
EXTERNAL CLOCK DRIVE WAVEFORM



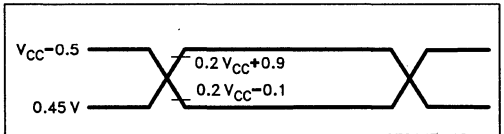
SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS

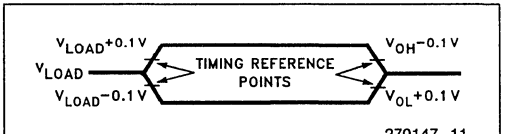


AC TESTING INPUT, OUTPUT WAVEFORMS



AC inputs during testing are driven at V_{CC} – 0.5 for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ±20 mA. (-L, I_{OL}/I_{OH} = ±10 mA)

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:

- Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.
- Programming specifications for the 87C51-L are the same as the standard 87C51.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4 respectively for A0–A14.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.6, P3.7.

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$.

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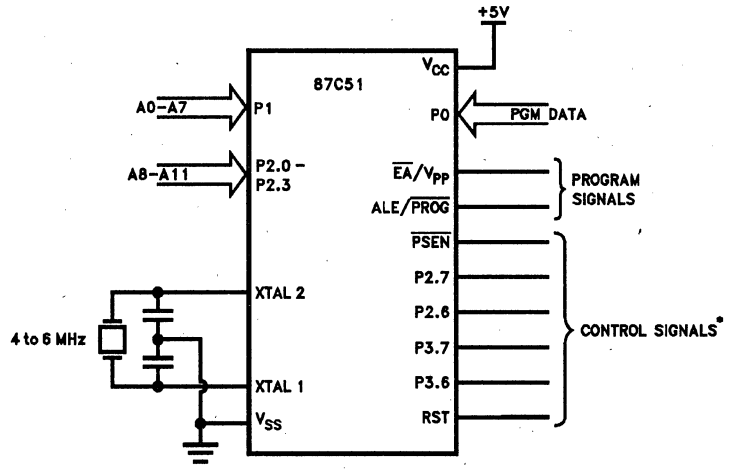
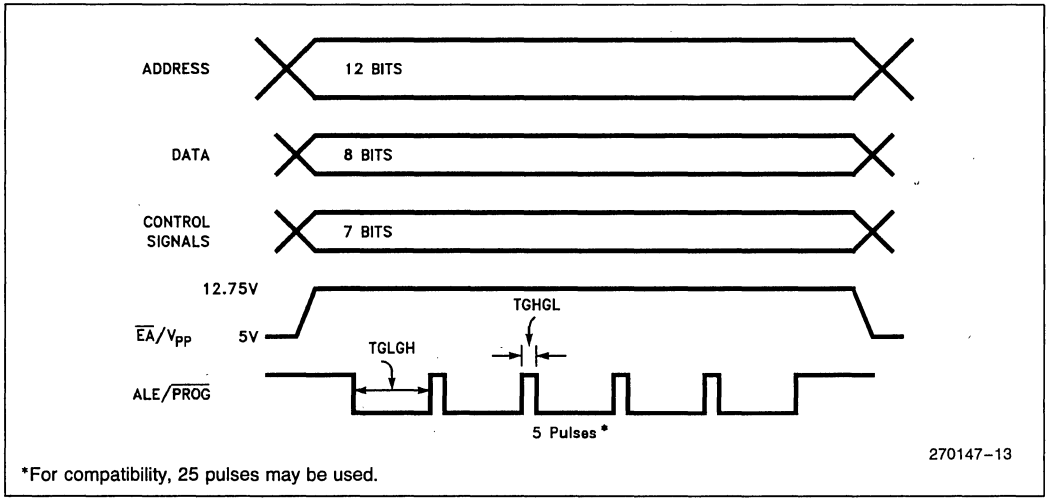
Table 2. EPROM Programming Modes

Mode		RST	PSEN	ALE/PROG	EA/VPP	P2.6	P2.7	P3.6	P3.7
Program Code Data		H	L	⎍	12.75V	L	H	H	H
Verify Code Data		H	L	H	H	L	L	H	H
Program Encryption Array Address 0–3F		H	L	⎍	12.75V	L	H	L	H
Program Lock Bits	Bit 1	H	L	⎍	12.75V	H	H	H	H
	Bit 2	H	L	⎍	12.75V	H	H	L	L
	Bit 3	H	L	⎍	12.75V	H	L	H	L
Read Signature Byte		H	L	H	H	L	L	L	L



*See Table 2 for proper input on these pins

Figure 10. Programming the EPROM



*For compatibility, 25 pulses may be used.

Figure 11. Programming Waveforms

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times* for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

Program Verify

Verification may be done after programming either one byte or a block of bytes. In either case a complete verify of the array will ensure reliable programming of the 87C51.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

EPROM Lock System

The 87C51 program lock system, when programmed, protects the onboard program against software piracy.

The 87C51 has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 3.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 2 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

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Program Lock Bits

The 87C51 has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 87C51 has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents
	87C51
30H	89H
31H	58H
60H	51H

Erasure Characteristics (Windowed Devices Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1's state.

Table 3. Program Lock Bits and the Features

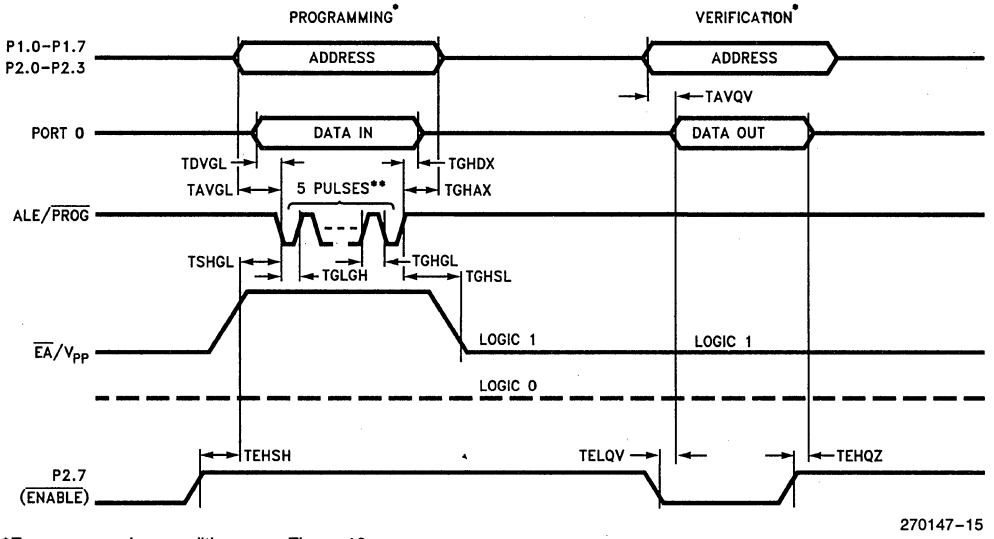
Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. (Code verify will still be encrypted by the encryption array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS:

(T_A = 21°C to 27°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold After $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold After $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold After $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float After $\overline{ENABLE}$	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*For programming conditions see Figure 10.
**5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

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DATA SHEET REVISION HISTORY

This data sheet (271047-008) is valid for devices with an "A" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (271047-008) and the previous version (271047-007):

1. The 80C51BH/80C31BH CHMOS Single-Chip 8-Bit Microcomputer data sheet (270064-008) has been combined with the 87C51 CHMOS Single-Chip 8-Bit Microcontroller with 4 Kbytes of EPROM Program Memory data sheet (271047-001) to create this new data sheet.
2. 80C51BH/80C31BH specs have been added to the Package Table, DC Characteristics Table and AC Characteristics Table.
3. Added 3.3V device to data sheet.
4. EPROM Programming Information has been added.
5. The Operating Temperature Range has been changed to: 0°C to +70°C.

The following are the key differences between the -007 and the -006 versions of the 87C51 data sheet.

1. Pins labeled "NC" and "V_{SS1}" changed to "Reserved" in Figure 2.
2. θ_{ja} and θ_{jc} specifications added to "Packages" table.
3. V_{SS1} pin description deleted.
4. Capacitor values for ceramic resonators deleted from Figure 3.
5. Second paragraph added to "Encrypted Verify" under "Program Memory Lock" section.
6. All pin numbers and the P3.3 control line deleted from Figure 10.

The following differences exist between the -006 and the -005 versions of the 87C51 data sheet:

1. Technology changed from CHMOS II-E to CHMOS III-E.
2. QFP package offering added.
3. Asynchronous Reset added.
4. ALE disable added.
5. Program Memory Lock feature changes:
   - — Third lock bit added
   - — Encryption array enhanced to 64 bytes
6. Data sheet status notice and Absolute Maximum Ratings warning revised.
7. DC Characteristics changes:
   - — Additional V_{OL} entries added (0.3V @ I_{OL} = 100 μA, 1.0V @ I_{OL} = 3.5 mA).
   - — Additional V_{OL1} entries added (0.3V @ I_{OL} = 200 μA, 1.0V @ I_{OL} = 7.0 mA).
   - — V_{OH} entries changed from 2.4V @ I_{OH} = −60 μA, 0.75 V_{CC} @ I_{OH} = −25 μA, and 0.9 V_{CC} @ I_{OH} = −10 μA to the current values.
   - — V_{OH1} entries changed from 2.4V @ I_{OH} = −800 μA, 0.75 V_{CC} @ I_{OH} = −300 μA, and 0.9 V_{CC} @ I_{OH} = −80 μA to the current values.
   - — RRST changed from 50 KΩ min and 300 KΩ max to the current values.
   - — C_{IO} changed from 10 pF max to 10 pF typical
8. Note 2 reworded (ALE noise pulses).
9. Note 4 deleted (transition current sourcing).

DATA SHEET REVISION HISTORY (Continued)

10. AC Timings improved for:
    TAVLL changed from TCLCL−55 to TCLCL−40
    TLLAX changed from TCLCL−35 to TCLCL−30
    TLLPL changed from TCLCL−40 to TCLCL−30
    TRHDZ changed from 2 TCLCL−70 to 2 TCLCL−60
    TQVWX changed from TCLCL−60 to TCLCL−50
11. EPROM programming control line (P3.3) added to Figure 10.
12. Programming Algorithm paragraph reworded to describe programming changes.
13. Figure 11 changed to show 5 programming pulses rather than 25.
14. Figure 12 deleted (Program Verification).
15. Program Verification paragraph reworded.
16. Third signature byte added; location and definition included.
17. Program/Verify Algorithms paragraph deleted.
18. I_{PP} programming spec changed from 50 mA to 75 mA.

The following are the key differences between -005 and the -004 versions of the 87C51 data sheet:

1. Package table was added.
2. Note 7 on maximum current specifications added to DC Characteristics.
3. Data Sheet Revision Summary was added.

87C51

EXPRESS

- **Extended Temperature Range**
- **Burn-In**
- **3.5 MHz to 12 MHz V_{CC} = 5V ±10%**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.

September 1988
Order Number: 270430-002

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
V_{IL}	Input Low Voltage (Except EA)	−0.5	$0.2V_{CC} - 0.15$	V	
V_{IL1}	EA	0	$0.2V_{CC} - 0.35$	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	$0.2V_{CC} + 1$	$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage to XTAL1, RST	$0.7V_{CC} + 0.1$	$V_{CC} + 0.5$	V	
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)		−75	μA	$V_{IN} = 0.45V$
I_{TL}	Logical 1 to 0 transition Current (Ports 1, 2, 3)		−750	μA	$V_{IN} = 2.0V$
I_{CC}	Power Supply Current Active Mode Idle Mode Power Down Mode		 35 6 50	 mA mA μA	(Note 1)

NOTE:
1. V_{CC} = 4.5V–5.5V, Frequency Range = 3.5 MHz–12 MHz.

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Table 1. Prefix Identification

Prefix	Package Type	Temperature Range(2)	Burn-In(3)
P	Plastic	Commercial	No
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD	Cerdip	Extended	No
TN	PLCC	Extended	No
QP	Plastic	Commercial	Yes
QD	Cerdip	Commercial	Yes
QN	PLCC	Commercial	Yes
LP	Plastic	Extended	Yes
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

NOTES:
2. Commercial temperature range is 0°C to +70°C. Extended temperature range is −40°C to +85°C.
3. Burn-in is dynamic for a minimum time of 160 hours at +125°C, V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples:

P87C51 indicates 87C51 in a plastic package and specified for commercial temperature range, without burn-in.
LD87C51 indicates 87C51 in a cerdip package and specified for extended temperature range with burn-in.

87C51-20/-3
COMMERCIAL/EXPRESS
20 MHz CHMOS MICROCONTROLLER

87C51-20—3.5 to 20 MHz, V_{CC} = 5V ±20%
87C51-3—24 MHz Internal Operation, V_{CC} = 5V ±20%

- **High Performance CHMOS EPROM**
- **24 MHz Internal Operation (-3 only)**
- **Improved Quick-Pulse Programming Algorithm**
- **3-Level Program Memory Lock**
- **Boolean Processor**
- **128-Byte Data RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **5 Interrupt Sources**
- **Programmable Serial Channel**
- **TTL- and CMOS-Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **IDLE and POWER DOWN Modes**
- **ONCE Mode Facilitates System Testing**

The 87C51-20 is the EPROM version of the 80C51BH. It is fabricated on Intel's CHMOS III-E process. It contains 4 Kbytes of on-chip Program memory that can be electrically programmed, and can be erased by exposure to ultraviolet light.

The 87C51-20 EPROM array uses an improved Quick-Pulse programming algorithm, by which the entire 4 Kbyte array can be programmed in less than 3 seconds.

The 87C51-3 has the same 3.5 MHz to 20 MHz frequency range as the 87C51-20 when operating out of external program/data memory. When running out of internal program/data memory, the 87C51-3 can operate up to 24 MHz.

The extremely low operating power, along with the two reduced power modes, Idle and Power Down, make this part very suitable for low power applications. The Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

Throughout this document 87C51-20 will refer to both the 87C51-20 and the 87C51-3.

September 1992
Order Number: 272082-002

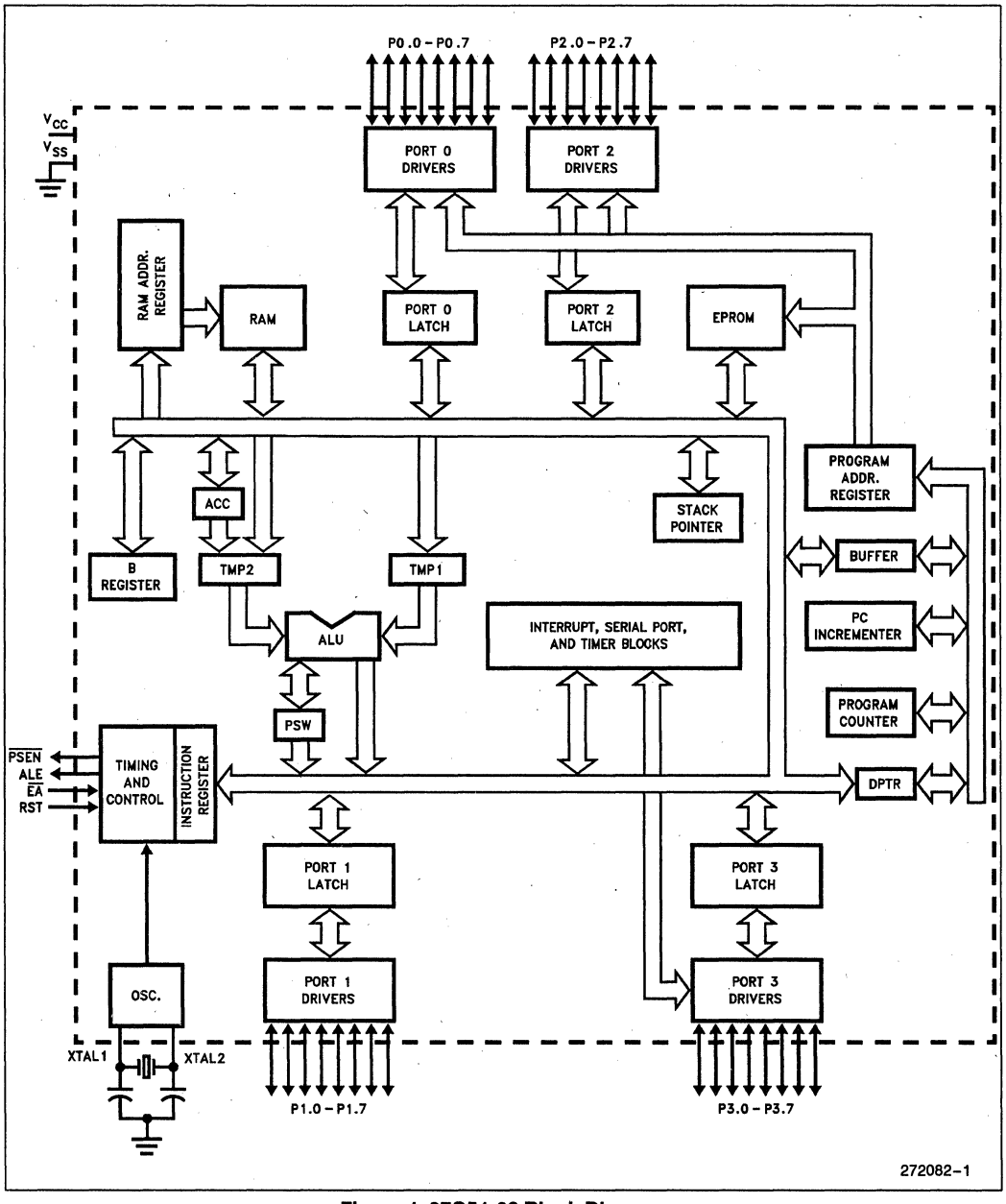


Figure 1. 87C51-20 Block Diagram

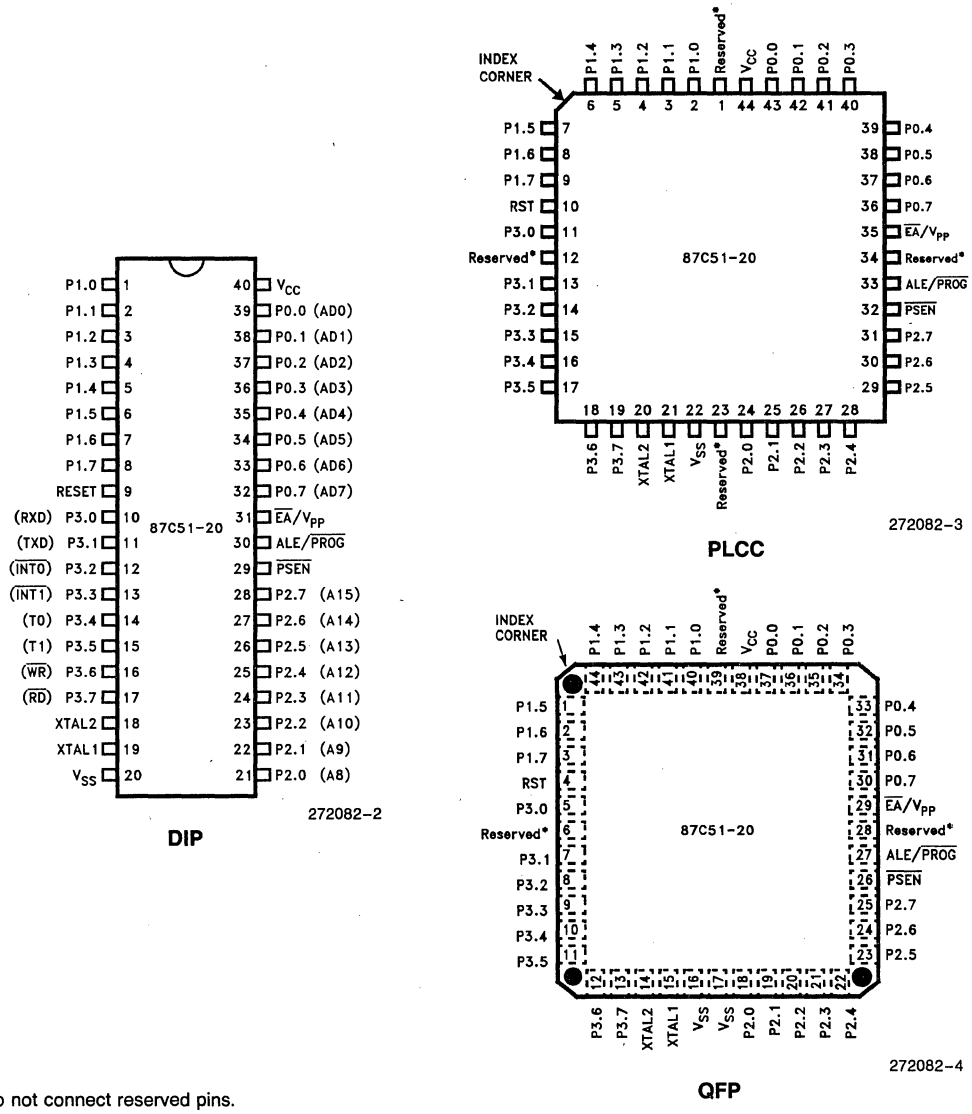
PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.

PACKAGES

Part	Prefix	Package Type	θ_{JA}	θ_{JC}
87C51-20	P	40-Pin Plastic DIP (OTP)	45°C/W	16°C/W
	D	40-Pin CERDIP (EPROM)	45°C/W	15°C/W
	N	44-Pin PLCC (OTP)	46°C/W	16°C/W
	S	44-Pin QFP (OTP)	98°C/W	24°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Circuit ground.
Port 0	8-bit, open drain, bidirectional I/O port. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during verification. When used as an I/O port, pullups to V_{CC} may be needed.
Port 1	8-bit bidirectional I/O port. All of the port 1 pins are shared with other functions in the 87C51-20. Port 1 is also used as the low-order address byte input during EPROM programming.
Port 2	8-bit bidirectional I/O port. Port 2 also emits the high-order address byte during accesses to 16-bit external memory locations. Some of the Port 2 pins are also used as address bits for EPROM programming.
Port 3	8-bit bidirectional I/O port. All of the port 3 pins are shared with other functions in the 87C51-20. Two of the pins are used as control lines ($\overline{RD}$, $\overline{WR}$) for accessing external RAM.
RESET	Reset input to the chip. A high Input for a minimum of two machine cycles with the oscillator running resets the device. The port pins will be reset when a voltage above V_{IH} is applied whether the oscillator is running or not. RST has an internal pulldown.
ALE/$\overline{PROG}$	Address Latch Enable. Provides a signal to demultiplex the address from the address/data bus. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode. This pin is also the program pulse input during EPROM programming.
$\overline{PSEN}$	Program Store Enable. Acts as read strobe for external program memory fetches.
$\overline{EA}/V_{PP}$	External Access Enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external program memory locations 0000H to 0FFFFH. $\overline{EA}$ should be strapped to V_{CC} for internal program executions. If any of the lock bits are programmed, $\overline{EA}$ will be internally latched on reset. This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	Input to the inverting oscillator amplifier.
XTAL2	Output from the inverting oscillator amplifier.

DESIGN CONSIDERATION

When running out of internal program/data memory, the 87C51-3 can be operated using a 24 MHz clock. If the 87C51-3 is running out of external program/data memory, the operating frequency must be between 3.5 MHz to 20 MHz. The 87C51-3 will not function properly at 24 MHz when running out of external program/data memory.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −45°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on $\overline{EA}$/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
Maximum I_{OL} per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(Based on package heat transfer limitations, not device power consumption).

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Express	 0 −40	 +70 +85	 °C °C
V_{CC}	Supply Voltage	4.0	6.0	V
F_{OSC}	Oscillator Frequency	3.5	20	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$) Commercial Express	 −0.5 −0.5		 0.2 V_{CC} − 0.1 0.2 V_{CC} − 0.15	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$) Commercial Express	 0 0		 0.2 V_{CC} − 0.3 0.2 V_{CC} − 0.35	V	
V_{IH}	Input High Voltage (Except XTAL1, RST) Commercial Express	 0.2 V_{CC} + 0.9 0.2 V_{CC} + 1.0		 V_{CC} + 0.5 V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST) Commercial Express	 0.7 V_{CC} 0.7 V_{CC} + 0.1		 V_{CC} + 0.5 V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage(5) (Ports 1, 2, 3)			0.3	V	I_{OL} = 100 μA(2)
				0.45	V	I_{OL} = 1.6 mA(2)
				1.0	V	I_{OL} = 3.5 mA(5)
V_{OL1}	Output Low Voltage(5) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA(2)
				0.45	V	I_{OL} = 3.2 mA (2)
				1.0	V	I_{OL} = 7.0 mA(2)
V_{OH}	Output High Voltage (Ports 1, 2, 3)	V_{CC} − 0.3			V	I_{OH} = −10 μA(3)
		V_{CC} − 0.7			V	I_{OH} = −30 μA(3)
		V_{CC} − 1.5			V	I_{OH} = −60 μA(3)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −200 μA(3)
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA(3)
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA(3)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3) Commercial Express			 −50 −75	μA	V_{IN} = 2.0V

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DC CHARACTERISTICS (Over Operating Conditions) (Continued)

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

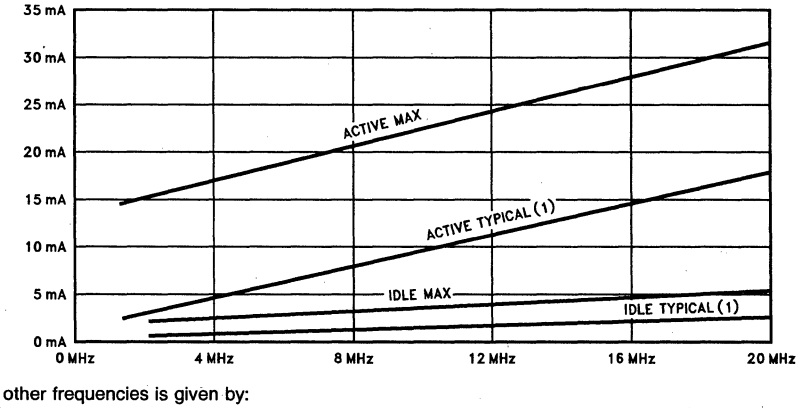
Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{LI}	Input Leakage Current (Port 0)			±10	μA	$0 < V_{IN} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3) Commercial Express			 −650 −750	 μA	 V_{IN} = 2.0V
RRST	RST Pulldown Resistor	50		300	KΩ	
C_{IO}	Pin Capacitance		10		pF	@ 1 MHz, 25°C
I_{CC}	Power Supply Current Active Mode Commercial Express Idle Mode Commercial Express Power Down Mode		 18 2.5 3.0	 32.5 45.5 5 7.5 50	 mA mA mA mA μA	(Note 4)

NOTES:

1. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temp, 5V.
2. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. See Figures 6 through 9 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = 0.94 x FREQ + 13.71
Idle Mode
I_{CC} Max = 0.14 x FREQ + 2.31
Where Osc Freq is in MHz, I_{CC} is in mA

Figure 3. I_{CC} vs Frequency

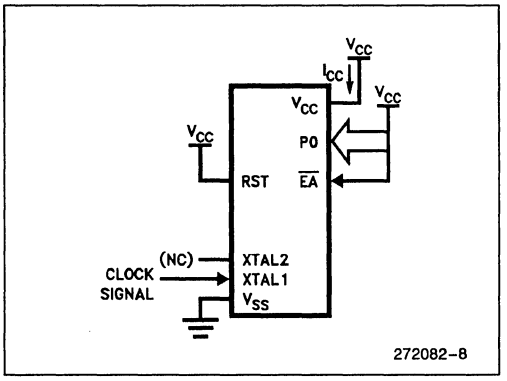


Figure 4. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

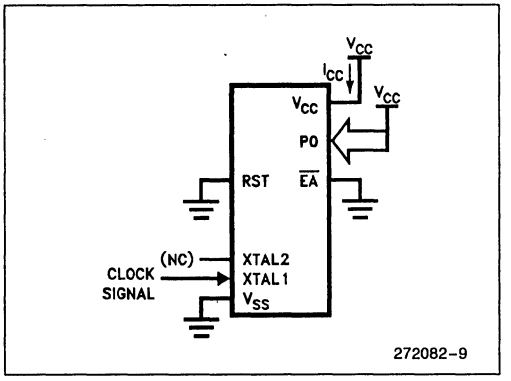


Figure 5. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

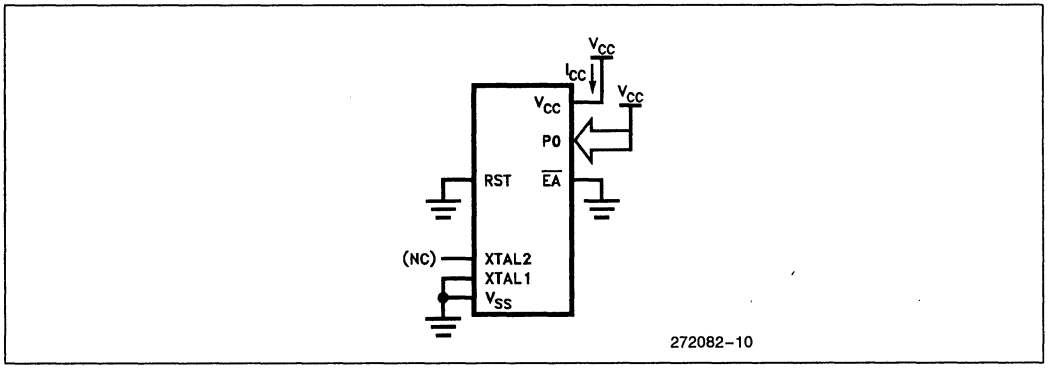


Figure 6. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected. V_{CC} = 2V to 5.5V.

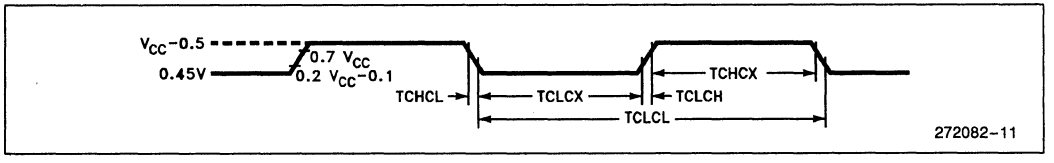


Figure 7. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

7

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

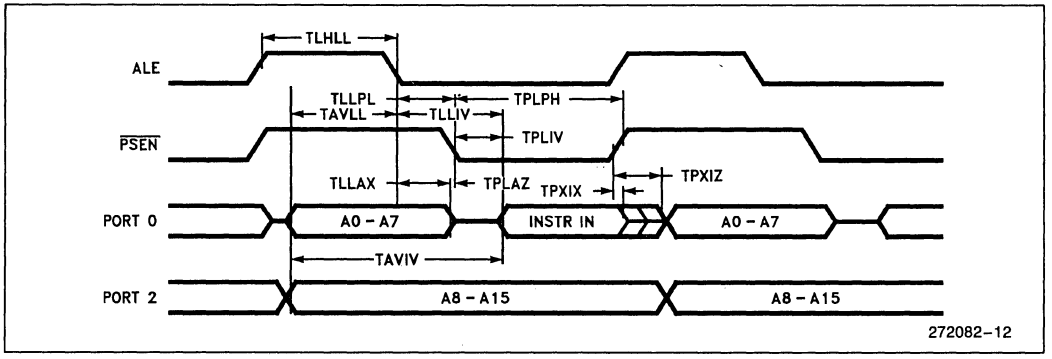
TAVLL = Time from Address Valid to ALE Low.
TLLPL = Time from ALE Low to PSEN Low.

AC CHARACTERISTICS (Over Operating Conditions; Load Capacitance for Port 0, ALE and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

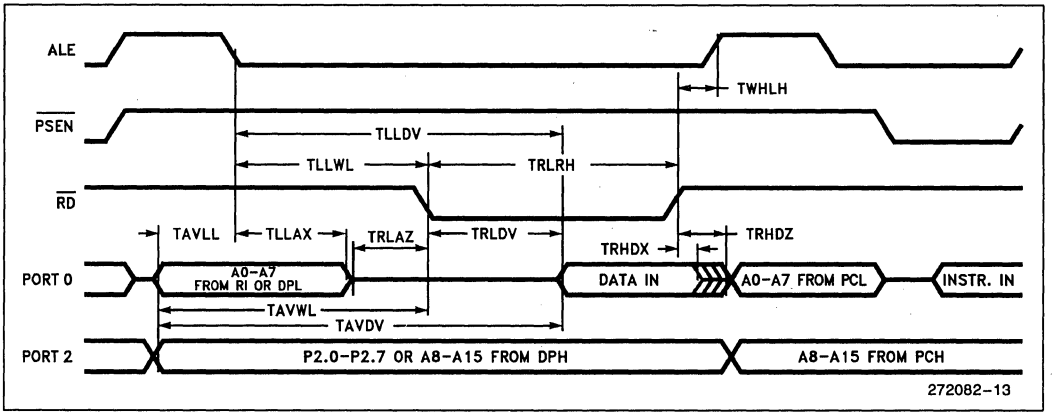
EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	20	MHz
TLHLL	ALE Pulse Width	60		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	10		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	20		TCLCL−30		ns
TLLIV	ALE Low to Valid Instr In		125		4TCLCL−75	ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	20		TCLCL−30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	105		3TCLCL−45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instr In		60		3TCLCL−90	ns
TPXIX	Input Instr Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{\text{PSEN}}$		30		TCLCL−20	ns
TAVIV	Address to Valid Instr In		145		5TCLCL−105	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	200		6TCLCL−100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	200		6TCLCL−100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		155		5TCLCL−95	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		40		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		310		8TCLCL−90	ns
TAVDV	Address to Valid Data In		360		9TCLCL−90	ns
TLLWL	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	100	200	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	110		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{\text{WR}}$ Transition	15		TCLCL−35		ns
TWHQX	Data Hold After $\overline{\text{WR}}$	10		TCLCL−40		ns
TQVWH	Data Valid to $\overline{\text{WR}}$ High	280		7TCLCL−70		ns
TRLAZ	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	10	90	TCLCL−40	TCLCL+40	ns

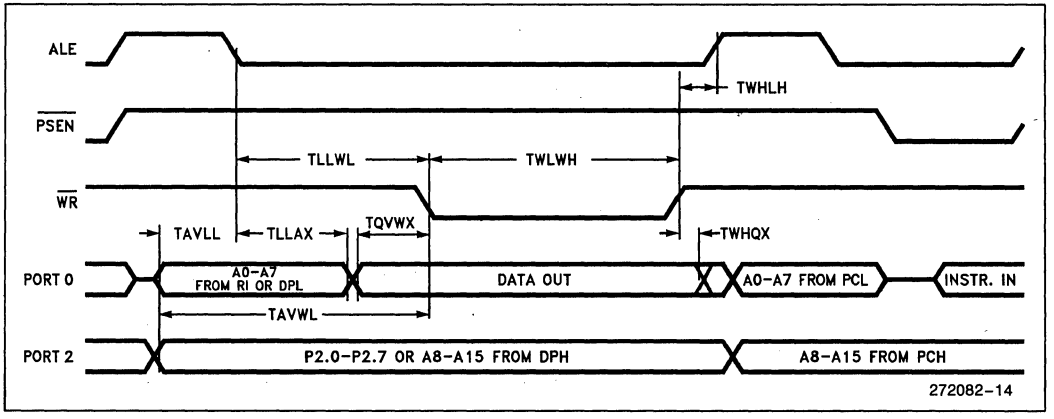
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE



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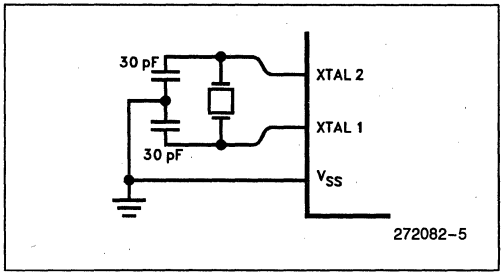


Figure 8. Using the On-Chip Oscillator

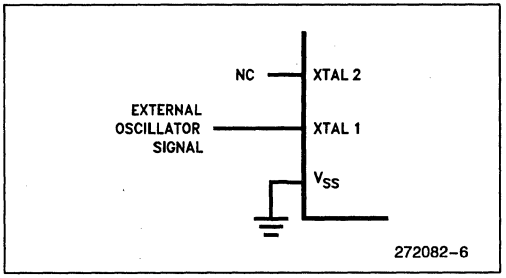
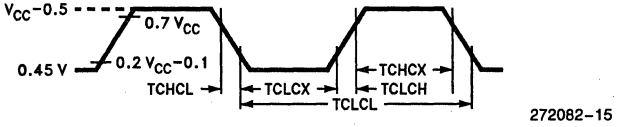


Figure 9. External Clock Drive

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

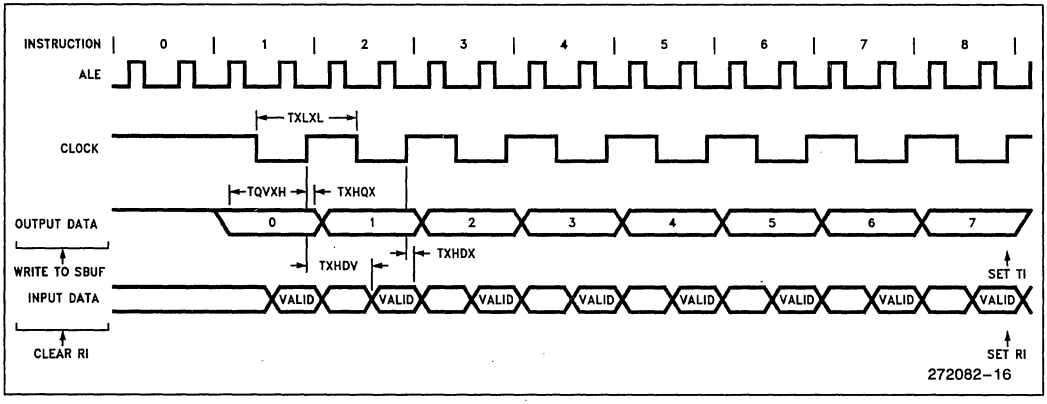
EXTERNAL CLOCK DRIVE WAVEFORM



SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	600		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	367		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL−50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		367		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



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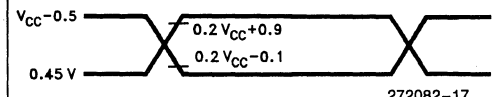
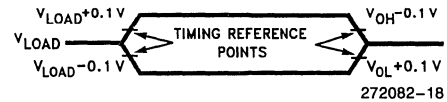
AC TESTING INPUT, OUTPUT WAVEFORMS



272082-17

AC inputs during testing are driven at V_{CC} − 0.5 for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



272082-18

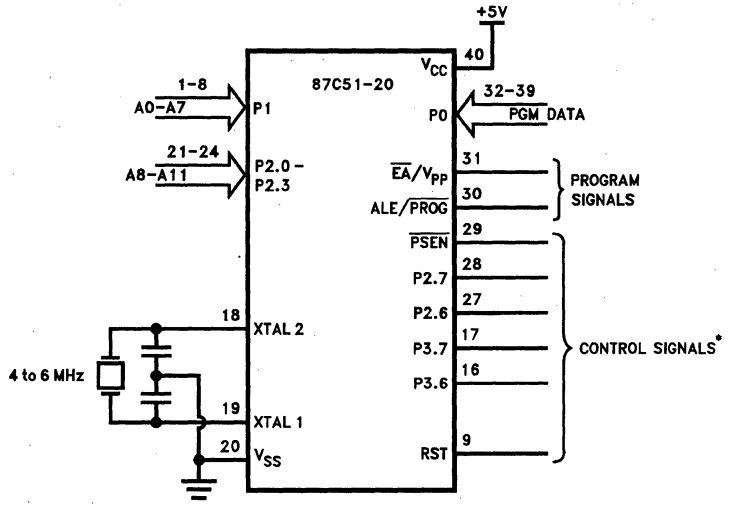
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

PROGRAMMING THE EPROM

Table 1. EPROM Programming Modes

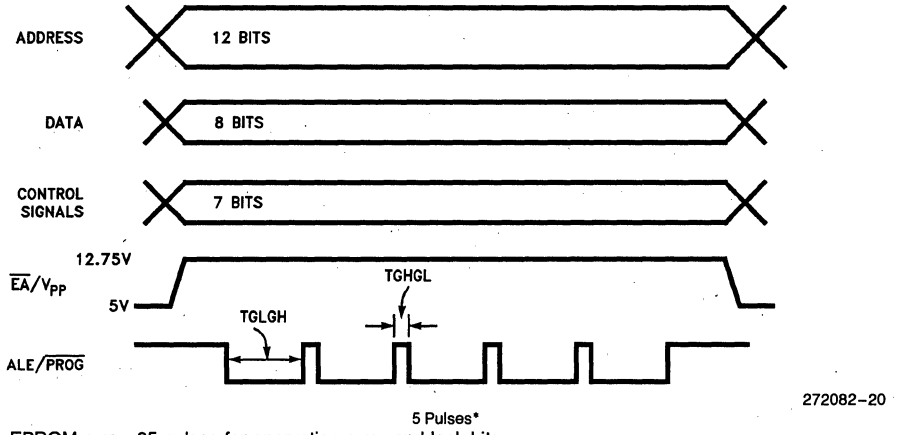
Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Program Code Data		H	L	⎍	12.75V	L	H	H	H
Verify Code Data		H	L	H	H	L	L	H	H
Program Encryption Array Address 0–3F		H	L	⎍	12.75V	L	H	L	H
Program Lock Bits	Bit 1	H	L	⎍	12.75V	H	H	H	H
	Bit 2	H	L	⎍	12.75V	H	H	L	L
	Bit 3	H	L	⎍	12.75V	H	L	H	L
Read Signature Byte		H	L	H	H	L	L	L	L

7



*See Table 1 for proper input on these pins

Figure 10. EPROM Programming Configuration



*5 Pulses for EPROM array, 25 pulses for encryption array and lock bits.
For compatibility, 25 pulses may be used to program the EPROM array.

Figure 11. Programming Waveforms

Signature Bytes

Location	Contents	Description
30H	89H	Indicates Intel Device
31H	58H	Indicates FX-Core Product
60H	51H	Indicates 87C51 Device

Erasure Characteristics (Windowed Devices Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

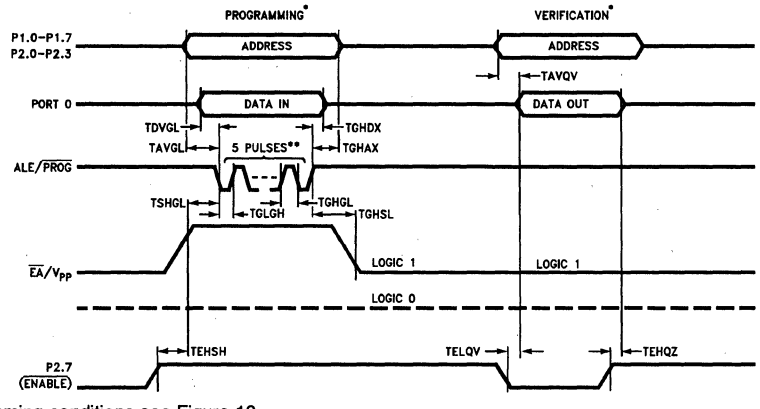
Erasure leaves the array in an all 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold After $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold After $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
TGHSL	V_{PP} Hold After $\overline{PROG}$	10		μs
TGLGH	$\overline{PROG}$ Width	90	110	μs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float After $\overline{ENABLE}$	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		μs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*For programming conditions see Figure 10.
**5 pulses for EPROM array, 25 pulses for encryption table and lock bits. For compatibility, 25 pulses may be used to program the EPROM array.

DATA SHEET REVISION HISTORY

This data sheet (272082-002) is valid for devices with an "A" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (272082-002) and the previous version (272082-001):

1. Added 87C51-3 to 20 MHz data sheet.
2. References to second functions of Port 1 pins have been removed.
3. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	120	125
	4TCLCL−80	4TCLCL−75
TPLIV	3TCLCL−95	3TCLCL−90
TQVWX	TCLCL−50	TCLCL−35
TWHQX	0	10
	TCLCL−50	TCLCL−40

TQVWH has been added.

The following differences exist between version -001 of this data sheet (272082-001) and the 87C51 (270147-006) data sheet.

1. All explanatory wording duplicated in the device user's guide was deleted.
2. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	4TCLCL−100	4TCLCL−80
TPLIV	3TCLCL−105	3TCLCL−95
TPXIZ	TCLCL−25	TCLCL−20
TRLDV	5TCLCL−165	5TCLCL−95
TLLDV	8TCLCL−150	8TCLCL−90
TAVDV	9TCLCL−165	9TCLCL−90
TAVWL	4TCLCL−130	4TCLCL−90
TQVWX	TCLCL−50	TCLCL−35

3. TXHQX in the Serial Port Timing Table changed from (2TCLCL−117) to (2TCLCL− 50).

8XC51SL/LOW VOLTAGE 8XC51SL KEYBOARD CONTROLLER

80C51SL — CPU with RAM and I/O; V_{CC} = 5V ±10%

81C51SL — 16K ROM Preprogrammed with SystemSoft Keyboard Controller and Scanner Firmware. V_{CC} = 5V ±10%.

83C51SL — 16K Factory Programmed ROM. V_{CC} = 5V ±10%.

87C51SL — 16K OTP ROM. V_{CC} = 5V ±10%.

Low Voltage 80C51SL— CPU with RAM and I/O; V_{CC} = 3.3V ±0.3V

Low Voltage 81C51SL— 16K ROM Preprogrammed with SystemSoft Keyboard Controller and Scanner Firmware. V_{CC} = 3.3V ±0.3V.

Low Voltage 83C51SL— 16K Factory Programmed ROM. V_{CC} = 3.3V ±0.3V.

Low Voltage 87C51SL— 16K OTP ROM. V_{CC} = 3.3V ±0.3V.

- **Proliferation of 8051 Architecture**
- **Complete 8042 Keyboard Control Functionality**
- **8042 Style Host Interface**
- **Optional Hardware Speedup of GATEA20 and RCL**
- **Local 16 x 8 Keyboard Switch Matrix Support**
- **Two Industry Standard Serial Keyboard Interfaces; Supported via Four High Drive Outputs**
- **5 LED Drivers**
- **Low Power CHMOS Technology**
- **4-Channel, 8-Bit A/D**
- **Interface for up to 32 Kbytes of External Memory**
- **Slew Rate Controlled I/O Buffers Used to Minimize Noise**
- **256 Bytes Data RAM**
- **Three Multifunction I/O Ports**
- **10 Interrupt Sources with 6 User-Definable External Interrupts**
- **2 MHz–16 MHz Clock Frequency**
- **100-Pin PQFP (8XC51SL)**
  100-Pin SQFP (Low Voltage 8XC51SL)

The 8XC51SL, based on Intel's industry-standard MCS®-51 microcontroller family, is designed for keyboard control in laptop and notebook PCs. The highly integrated keyboard controller incorporates an 8042-style UPI host interface with expanded memory, keyboard scan, and power management. The 8XC51SL supports both serial and scanned keyboard interfaces and is available in pre-programmed versions to reduce time to market. The Low Voltage 8XC51SL is the 3.3V version optimized for even further power savings. Throughout the remainder of this document, both devices will generally be referred to as 51SL.

The 8XC51SL is a pin-for-pin compatible replacement for the 8XC51SL-BG. It does, however have some additional functionality. Those additional functions are as follows:

1. 16K OTP ROM: The 8XC51SL-BG had only 8K of ROM.
2. New Register Set: The 8XC51SL adds a second set of host interface registers available for use in supporting power management. This required an additional address line (A1) for decoding. To accommodate this, one V_{CC} pin was removed. However, in order to maintain compatibility with the -BG version, an enable bit for this new register set was added in configuration register 0. This allows the 8XC51SL to be drop in compatible to existing 8XC51SL-BG designs; no software modifications required.
3. Interrupt Enable: The 10 available interrupts on the 8XC51SL-BG were split into two groups of five, each with its own global enable. The 8XC51SL combines those two groups into a single group with one global enable for all 10 interrupts.

For the complete data sheet on this product, refer to the 1993 Mobile Computer Products handbook.

October 1992
Order Number: 272271-001

87C52/80C52/80C32
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 8 KBYTES INTERNAL PROGRAM MEMORY

87C52/80C52/80C32—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C52-1/80C52-1/80C32-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%
87C52-L—3.5 MHz to 8 MHz, V_{CC} = 3.3V ±0.3V

- High Performance CHMOS EPROM/ ROM/CPU
- Low Voltage Operation (-L Only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Up/Down Timer/Counter
- Three Level Program Lock System
- 8K On-Chip EPROM/ROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 6 Interrupt Sources
- Programmable Serial Channel with:
  - Framing Error Detection
  - Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode
- Four-Level Interrupt Priority

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside on-chip, (except 80C32). The device can also address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C52/80C52/80C32 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 87C52/80C52/80C32 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 87C52/80C52/80C32 is an enhanced version of the 87C51/80C51BH/80C31BH. It's added features make it an even more powerful microcontroller for applications that require clock output, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

Applications that require low voltage operation can use the 87C52-L. The 87C52-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz.

Throughout this document 8XC52 will refer to the 87C52, 80C52 and 80C32.

October 1992
Order Number: 270757-003

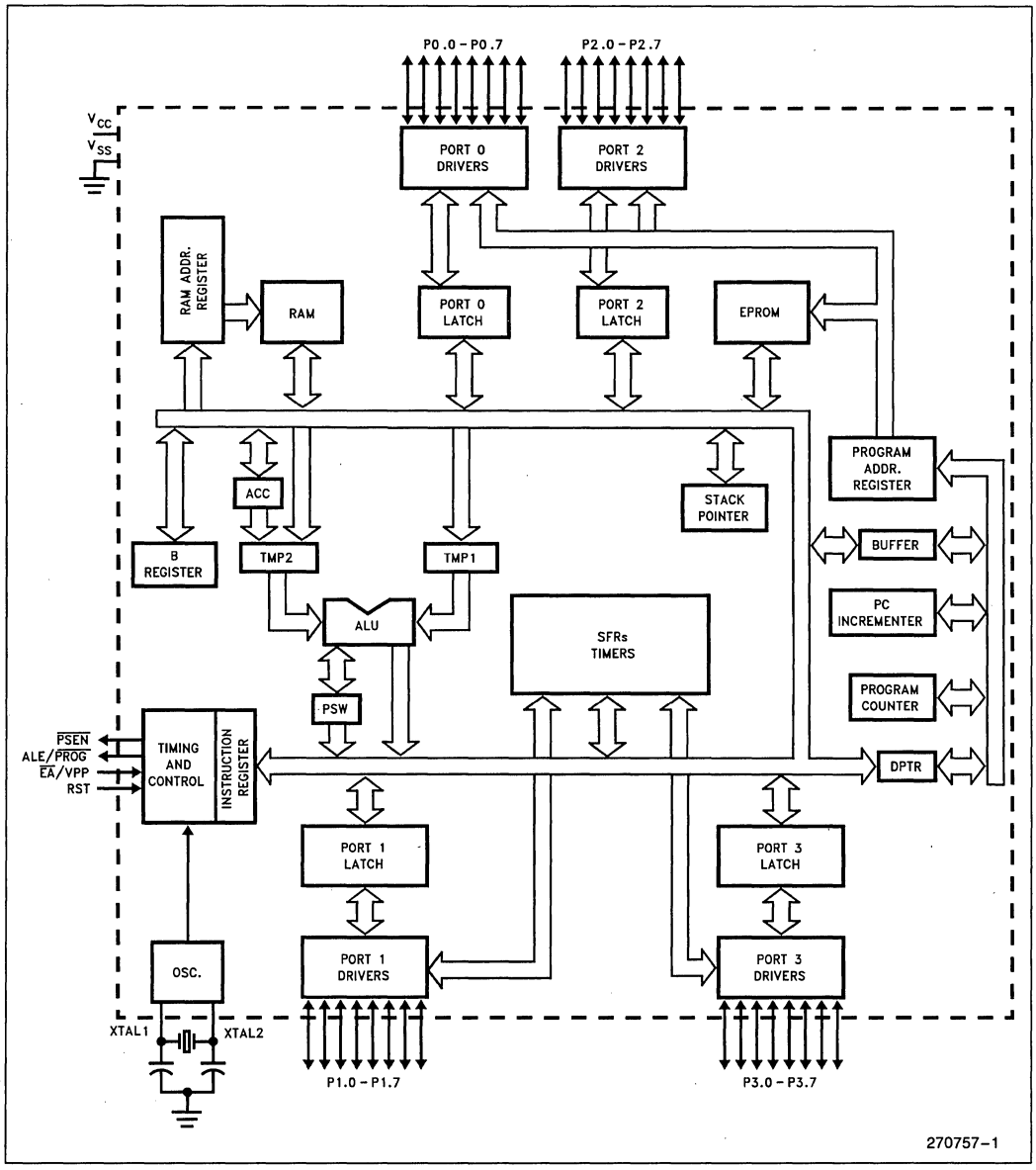


Figure 1. 8XC52 Block Diagram

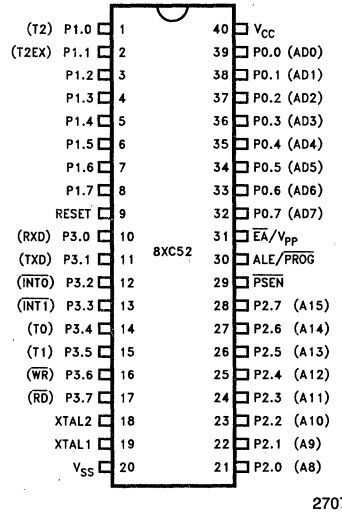
PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

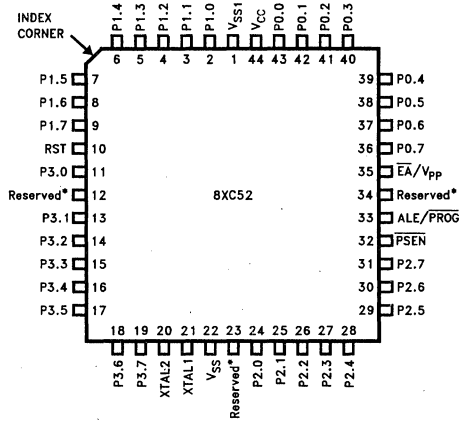
Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC52	P	40-Pin Plastic DIP (OTP)	45°C/W	16°C/W
87C52	D	40-Pin CERDIP (EPROM)	45°C/W	15°C/W
8XC52	N	44-Pin PLCC (OTP)	46°C/W	16°C/W
8XC52	S	44-Pin QFP (OTP)	87°C/W	18°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



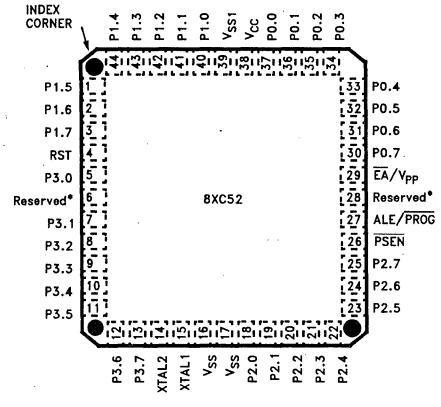
270757-2

DIP



270757-3

PLCC



270757-4

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22).

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC52:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IHI} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C52.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC52 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

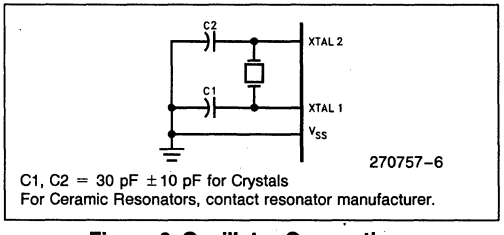


Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

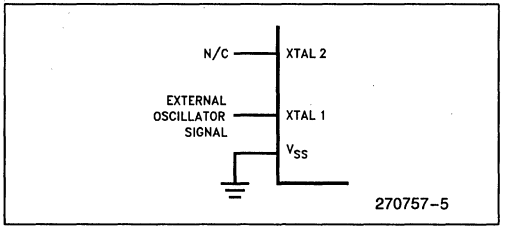


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC52 either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

DESIGN CONSIDERATION

- The 87C52-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz. Operating beyond these specifications could cause improper device functionality. (To program the 87C52-L, follow the same procedure as the 87C52.)
- The window on the 87C52 must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC52 without the 8XC52 having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC52 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

7

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions:

T_A (under bias) = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V (87C52-L, V_{CC} = 3.3V ±0.3V)

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to both 5V and 3.3V devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$)	V_{CC}−0.3			V	I_{OH} = −10 μA
		V_{CC}−0.7			V	I_{OH} = −30 μA
		V_{CC}−1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC}−0.3			V	I_{OH} = −200 μA
		V_{CC}−0.7			V	I_{OH} = −3.2 mA
		V_{CC}−1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)			±10	μA	V_{IN} = V_{IL} or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)			−650	μA	V_{IN} = 2V

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

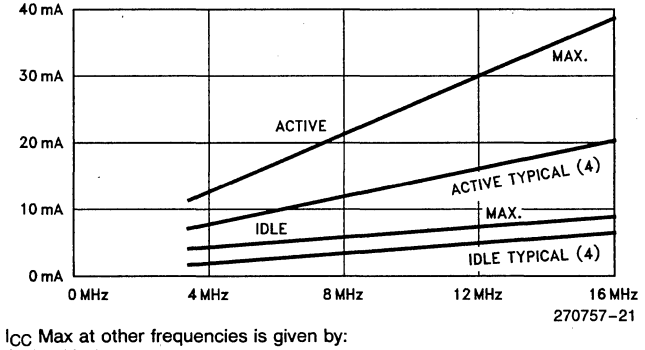
All parameter values apply to both 5V and 3.3V devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
RRST	RST Pulldown Resistor	50		300	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current:					(Note 3)
	Active Mode					
	87C52-L at 8 MHz			12	mA	
	All Others at 12 MHz (Figure 5)		15	30	mA	
	Idle Mode at 12 MHz (Figure 5)		5	7.5	mA	
	Power Down Mode		5	75	μA	

NOTES:

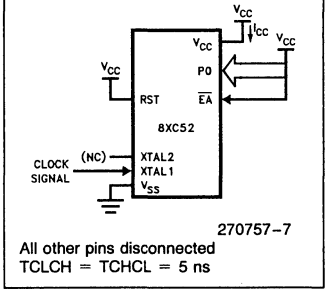
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = 2.2 × Freq + 3.1
Idle Mode
I_{CC} Max = 0.49 × Freq + 1.6
Where Freq is in MHz, I_{CC} Max is given in mA.

Figure 5. I_{CC} vs Frequency



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode

7

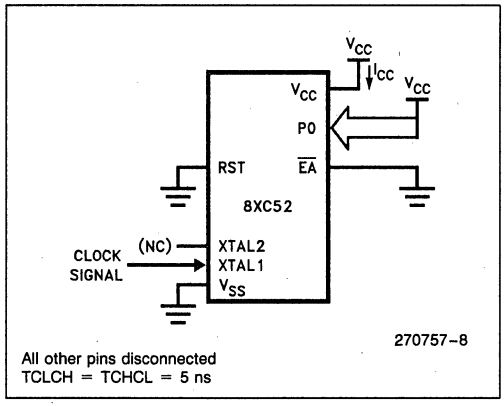


Figure 7. I_{CC} Test Condition Idle Mode

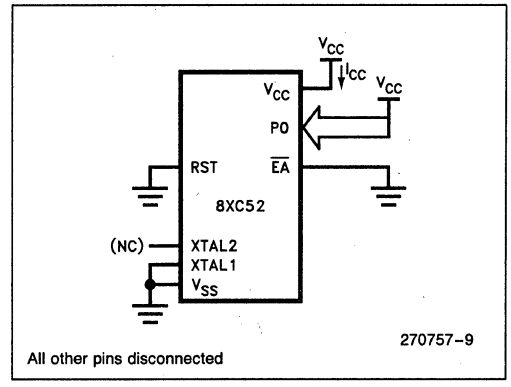


Figure 8. I_{CC} Test Condition, Power Down Mode
V_{CC} = 2.0V to 6.0V

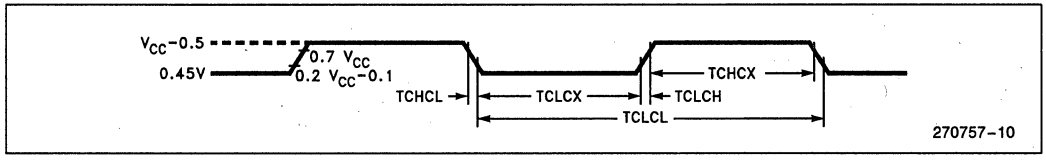


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

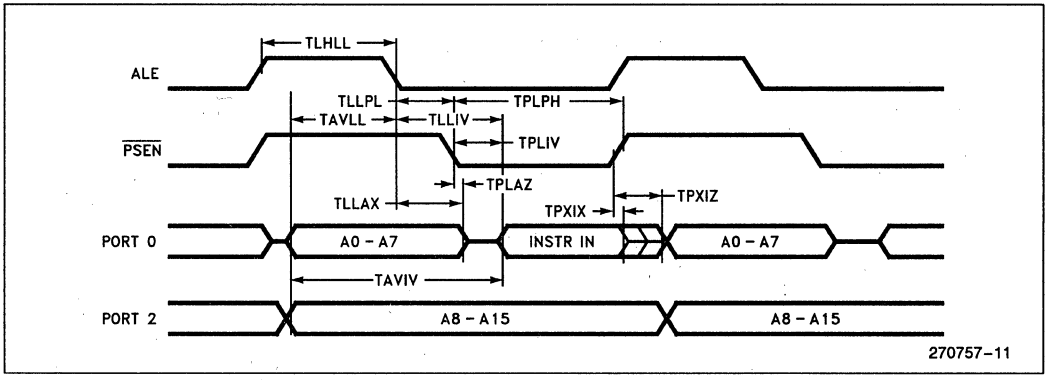
AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

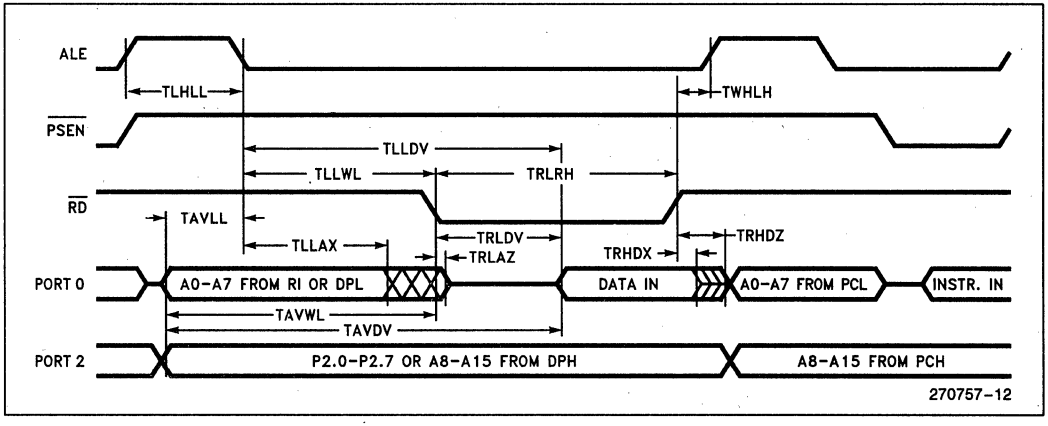
Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	53		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	53		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		3TCLCL−105	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		312		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid before $\overline{WR}$	33		TCLCL−50		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL−50		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

7

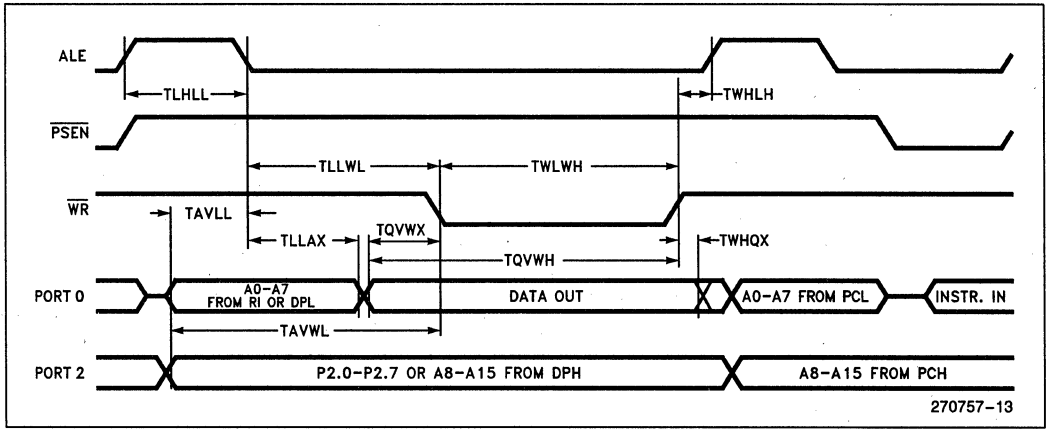
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

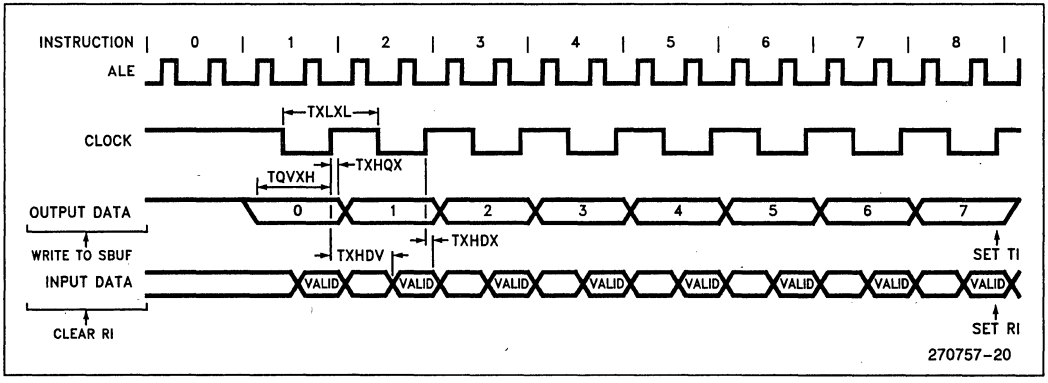


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

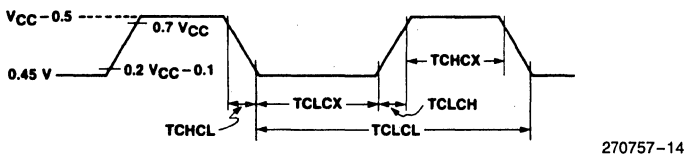
SHIFT REGISTER MODE TIMING WAVEFORMS



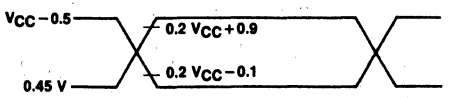
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XC52 8XC52-1	 3.5 3.5	 12 16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



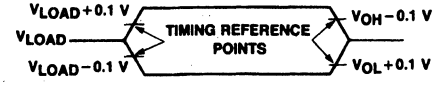
AC TESTING INPUT, OUTPUT WAVEFORMS



270757-15

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



270757-16

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA (-L, $I_{OL}/I_{OH} = \pm 10$ mA).

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTES:

- Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.
- Programming specifications for the 87C52-L are the same as the standard 87C52.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5 respectively for A0–A13.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

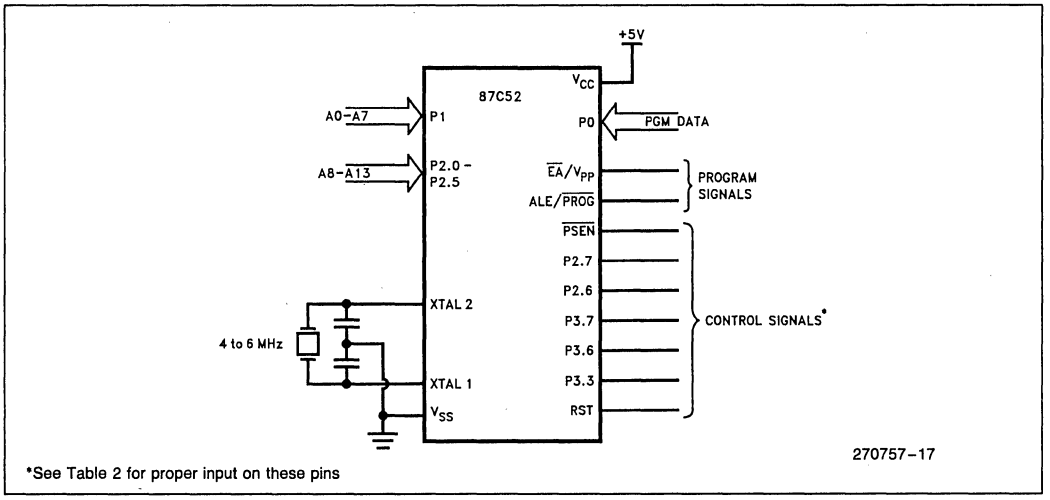


Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C52 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C52.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

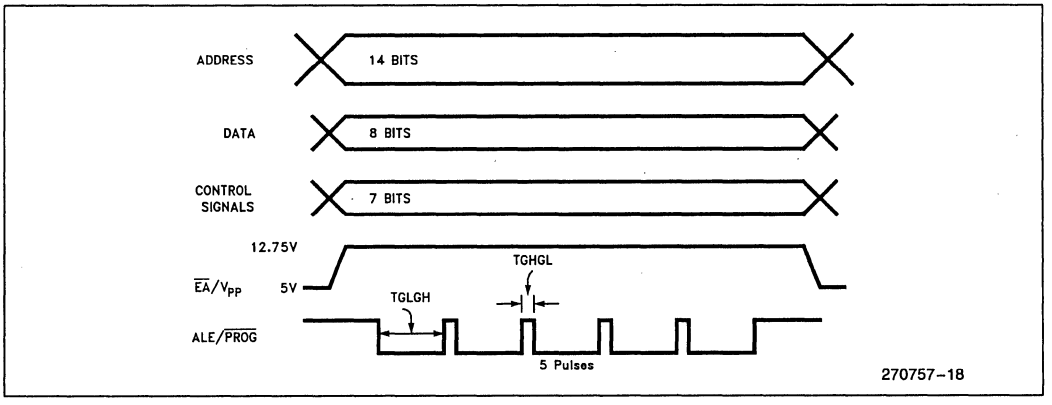


Figure 11. Programming Signal's Waveforms

Reading the Signature Bytes

The 87C52/80C52 each has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Content	
	87C52	80C52
30H	89H	89H
31H	58H	58H/53H
60H	52H	52H/12H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

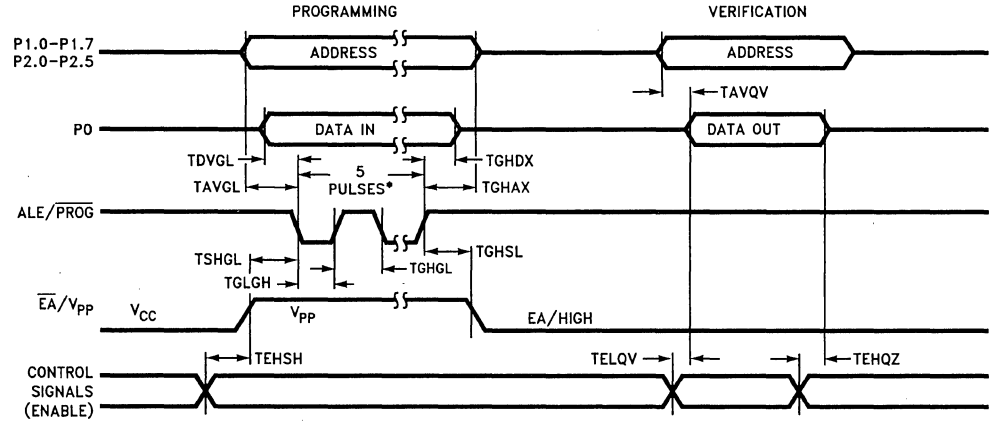
Erasure leaves all the EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		μs
TGLGH	$\overline{PROG}$ Width	90	110	μs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		μs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



270757-19

*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

DATA SHEET REVISION HISTORY

The following differences exist between this data sheet (270757-003) and the previous version (270757-002):

1. Data sheet title was changed from:
   80C52/80C32 CHMOS Single-Chip 8-Bit Microcomputer.
   to:
   87C52/80C52/80C32 CHMOS Single-Chip 8-Bit Microcontroller with 8 Kbytes Internal Program Memory.
2. Added 3.3V device to data sheet.
3. Revision History added to data sheet.

7

87C52/80C52/80C32

EXPRESS

87C52/80C52/80C32—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C52-1/80C52-1/80C32-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%

- **Extended Temperature Range**
- **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here. This data sheet is valid in conjunction with the commercial 87C52/80C52/80C32 data sheet 270757-003.

September 1992
Order Number: 270868-002

Electrical Deviations from Commercial Specifications for Extended Temperature Range

DC and AC parameters not included here are the same as in the commercial temperature range data sheets.

DC CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)		−75	μA	$V_{IN} = 0.45V$
I_{LI}	Input Leakage Current (Port 0 and $\overline{EA}$)		±15	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		−750	μA	$V_{IN} = 2.0V$
I_{CC}	Power Supply Currrent				(Note 1)
	Active Mode		35	mA	
	Idle Mode		7.5	mA	
	Power Down Mode		150	μA	

NOTE:
1. V_{CC} = 4.5V–5.5V, Frequency Range =3.5 MHz–12 MHz.

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
D*	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD*	Cerdip	Extended	No
TN	PLCC	Extended	No
LP	Plastic	Extended	Yes
LD*	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

*Available for 87C52 only.

NOTE:
- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-in is dynamic for a minimum time of 168 hours at 125°C, V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples:

P80C52 indicates 80C52 in a plastic package and specified for commercial temperature range, without burn-in.
LD80C52 indicates 80C52 in a cerdip package and specified for extended temperature range with burn-in.

87C52-20/80C52-20/80C32-20 COMMERCIAL/EXPRESS 20 MHz MICROCONTROLLER

87C52-20/80C52-20/80C32-20—3.5 MHz to 20 MHz, V_{CC} = 5V ±20%
87C52-3/80C52-3—24 MHz Internal Operation, V_{CC} = 5V ±20%

- High Performance CHMOS EPROM
- 24 MHz Internal Execution (-3 only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Up/Down Timer/Counter
- Three Level Program Lock System
- 8K On-Chip EPROM/ROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 6 Interrupt Sources
- Programmable Serial Channel with:
  - Framing Error Detection
  - Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode
- Four-Level Interrupt Priority

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside on-chip (except 80C32). The device can also address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C52-20/80C52-20/80C32-20 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 87C52-20/80C52-20/80C32-20 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 87C52-20/80C52-20/80C32-20 is an enhanced version of the 87C51/80C51BH/80C31BH. Its added features make it an even more powerful microcontroller for applications that require clock output, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

The 87C52-3/80C52-3 has the same 3.5 to 20 MHz frequency range as the 87C52-20/80C52-20 when operating out of external program/data memory. When running out of internal program/data memory, the 87C52-3/80C52-3 can operate up to 24 MHz.

Throughout this document, 8XC52-20 will refer to the 87C52-20, 80C52-20, 80C32-20, 87C52-3 and 80C52-3.

October 1992
Order Number: 272272-001

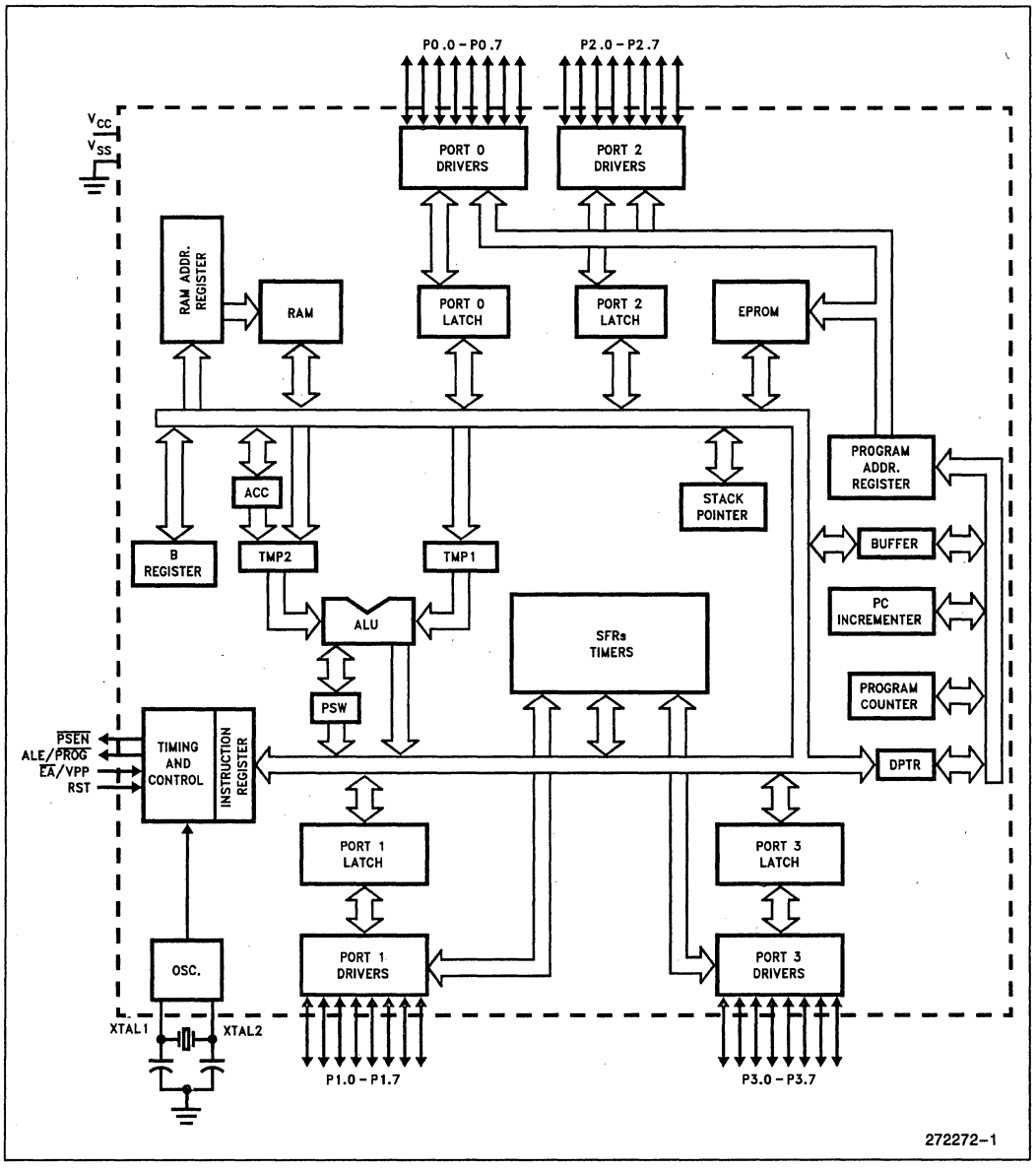
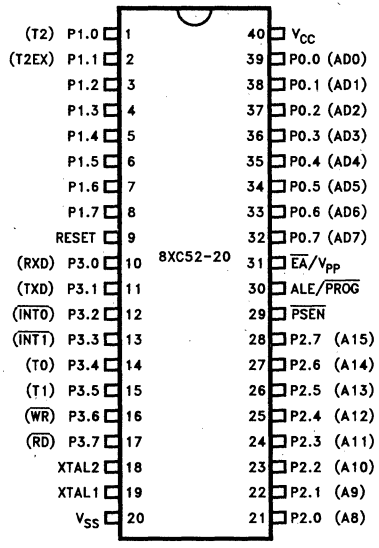


Figure 1. 8XC52-20 Block Diagram

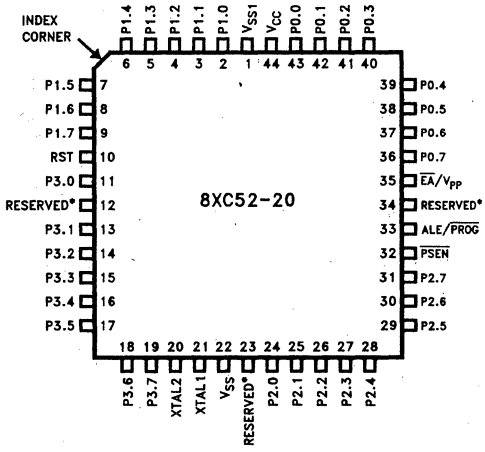
PACKAGES

Part	Prefix	Package Type	θ_{JA}	θ_{JC}
8XC52-20	P	40-Pin Plastic DIP	45°C/W	16°C/W
87C52-20	D	40-Pin CERDIP	45°C/W	15°C/W
8XC52-20	N	44-Pin PLCC	46°C/W	16°C/W
8XC52-20	S	44-Pin QFP	87°C/W	18°C/W



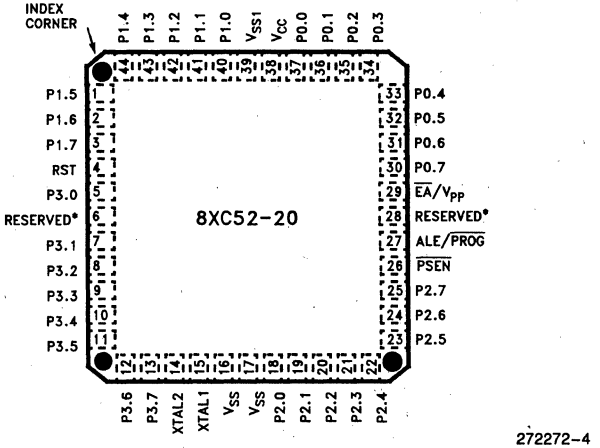
272272-2

DIP



272272-3

PLCC



272272-4

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22).

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC52-20:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IHI} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C52-20.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC52-20 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

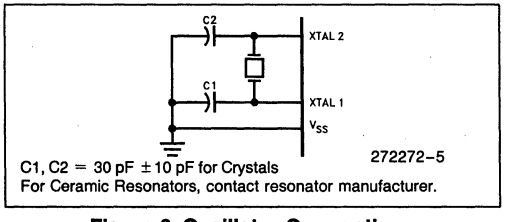


Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

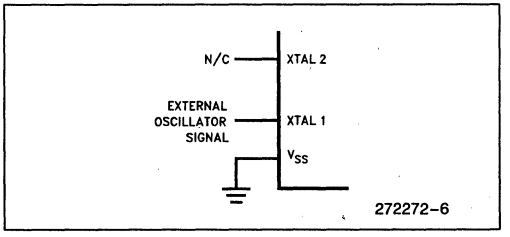


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC52-20 either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

TIMER 2 PROGRAMMABLE CLOCK OUT

The 8XC52-20 has a new Timer 2 feature. A 50% duty cycle clock can be programmed to come out on P1.0. The output frequency ranges from 61 Hz to 4 MHz depending on the oscillator frequency and the reload value of the Timer 2 capture registers (RCAP2H, RCAP2L) as shown in the equation below:

$$\text{*Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared, and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) starts and stops the timer.

For a complete description of all Timer 2 functions, please reference the 8XC52/54/58 Hardware Description of the 8-Bit Embedded Controllers Handbook.

***NOTE:**
Even though the equation permits a maximum clock-out frequency of 5 MHz using a 20 MHz oscillator, the maximum device output frequency is 4 MHz. When using a 20 MHz oscillator, RCAP2L must be limited to a maximum value of FEH.

DESIGN CONSIDERATION

- When running out of internal program/data memory, the 87C52-3/80C52-3 can be operated using a 24 MHz clock. If the 87C52-3/80C52-3 is running out of external program/data memory, the operating frequency must be between 3.5 to 20 MHz. The 87C52-3/80C52-3 will not function properly at 24 MHz when running out of external program/data memory.
- The window on the 87C52-20 must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC52-20 without the 8XC52-20 having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{\text{PSEN}}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{\text{PSEN}}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC52-20 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation..... 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency	3.5	20	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$)	V_{CC}−0.3			V	I_{OH} = −10 μA
		V_{CC}−0.7			V	I_{OH} = −30 μA
		V_{CC}−1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC}−0.3			V	I_{OH} = −200 μA
		V_{CC}−0.7			V	I_{OH} = −3.2 mA
		V_{CC}−1.5			V	I_{OH} = −7.0 mA

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

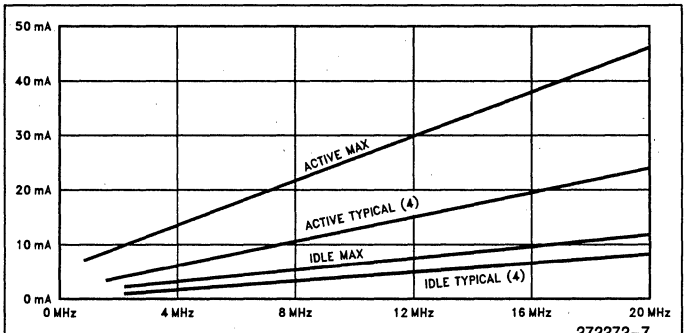
Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3) Commercial Express			 −50 −75	 μA	 V_{IN} = 2.0V
I_{LI}	Input Leakage Current (Port 0) Commercial Express			 ±10 ±15	 μA	 V_{IN} = V_{IL} or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3) Commercial Express			 −650 −750	 μA	 V_{IN} = 2.0V
RRST	RST Pulldown Resistor	50		300	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Active Mode Commercial Express Idle Mode (Figure 5) Power Down Mode		 24 8 5	 47.1 55 11.4 75	 mA mA mA μA	 (Note 3)

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

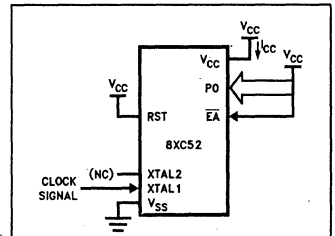
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

7



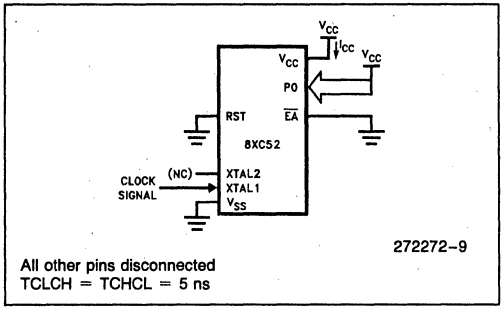
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = 2.2 X FREQ + 3.14
Idle Mode
I_{CC} Max = 0.49 X FREQ + 1.6
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 5. I_{CC} vs Frequency



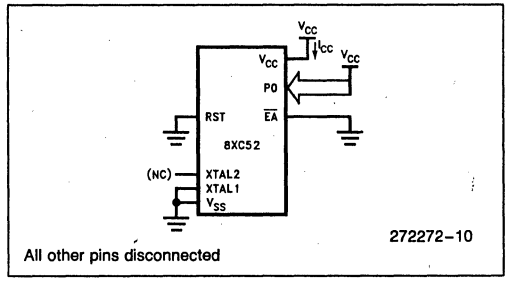
All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition Idle Mode



All other pins disconnected

Figure 8. I_{CC} Test Condition, Power Down Mode V_{CC} = 2.0V to 6.0V

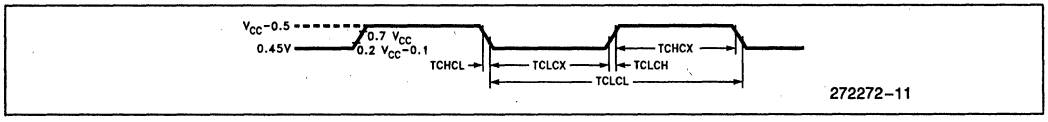


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

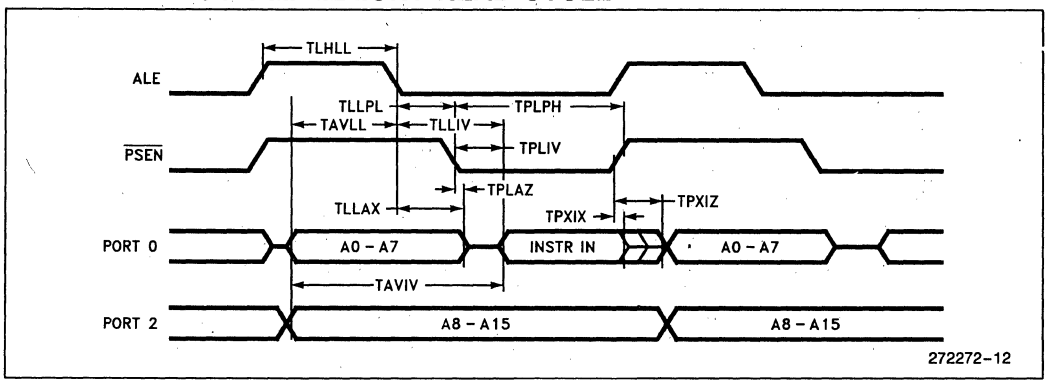
AC CHARACTERISTICS (Over Operating Conditions) Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

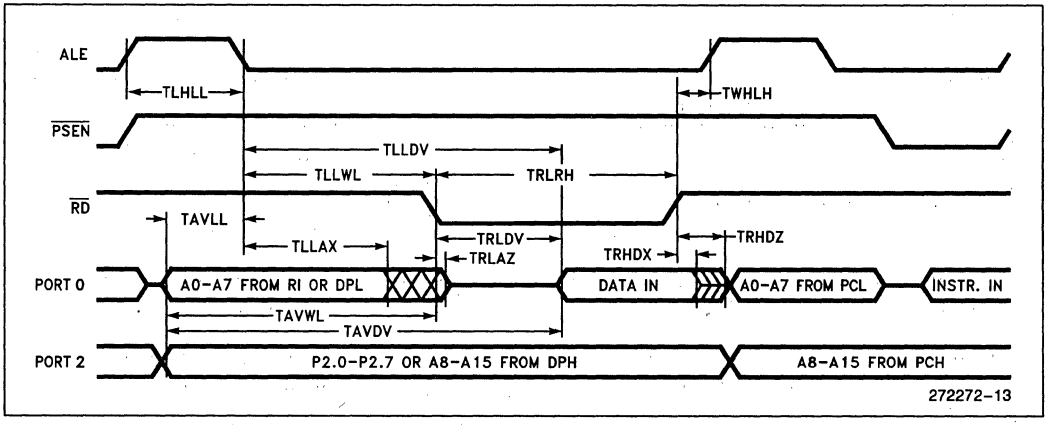
Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	20	MHz
TLHLL	ALE Pulse Width	60		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	10		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	20		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		125		4TCLCL−75	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	20		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	105		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		60		3TCLCL−90	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		30		TCLCL−20	ns
TAVIV	Address to Valid Instruction In		145		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	200		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	200		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		155		5TCLCL−95	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		40		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		310		8TCLCL−90	ns
TAVDV	Address to Valid Data In		360		9TCLCL−90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	100	200	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	110		4TCLCL−90		ns
TQVWX	Data Valid before $\overline{WR}$	15		TCLCL−35		ns
TWHQX	Data Hold after $\overline{WR}$	10		TCLCL−40		ns
TQVWH	Data Valid to $\overline{WR}$ High	280		7TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	10	90	TCLCL−40	TCLCL+40	ns

7

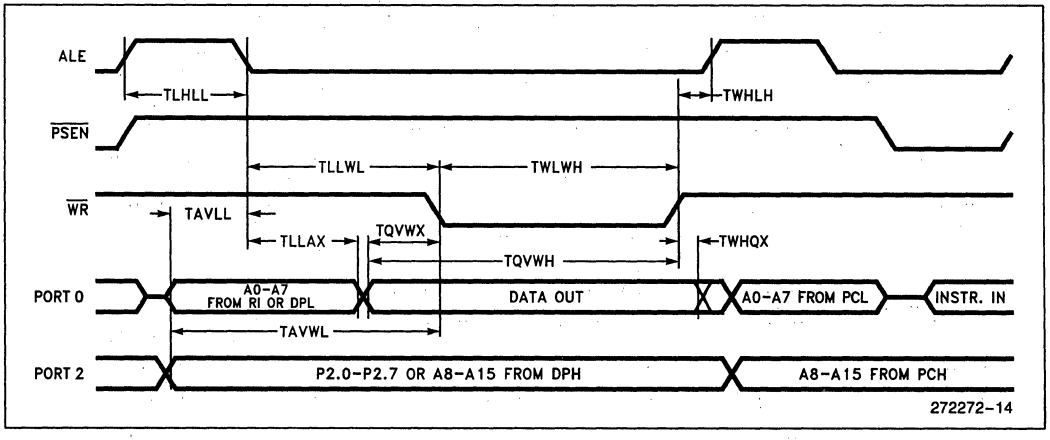
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

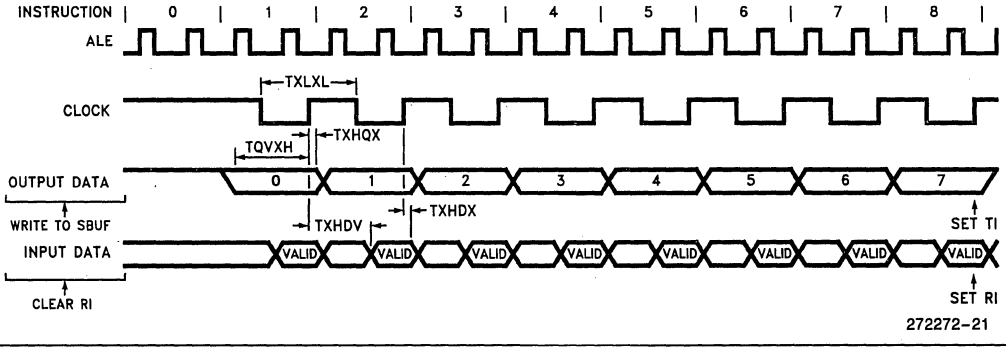


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	600		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	367		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		367		10TCLCL−133	ns

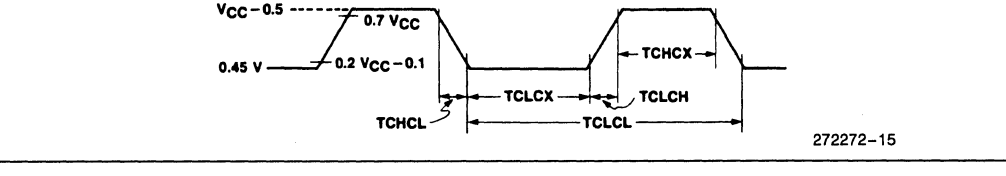
SHIFT REGISTER MODE TIMING WAVEFORMS



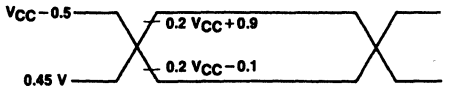
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



AC TESTING INPUT, OUTPUT WAVEFORMS



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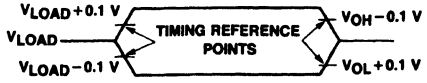
AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



272272-17

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5 respectively for A0–A13.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

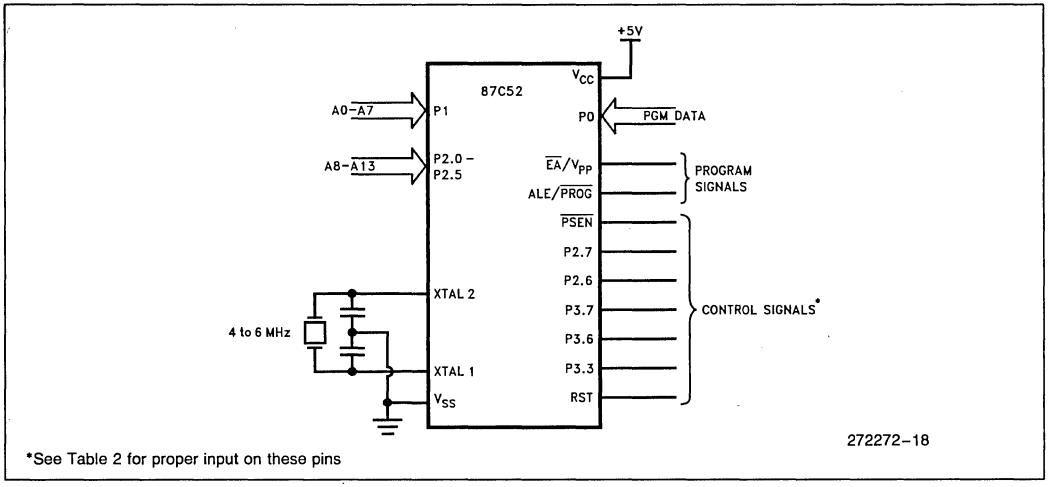


Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C52-20 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C52-20.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

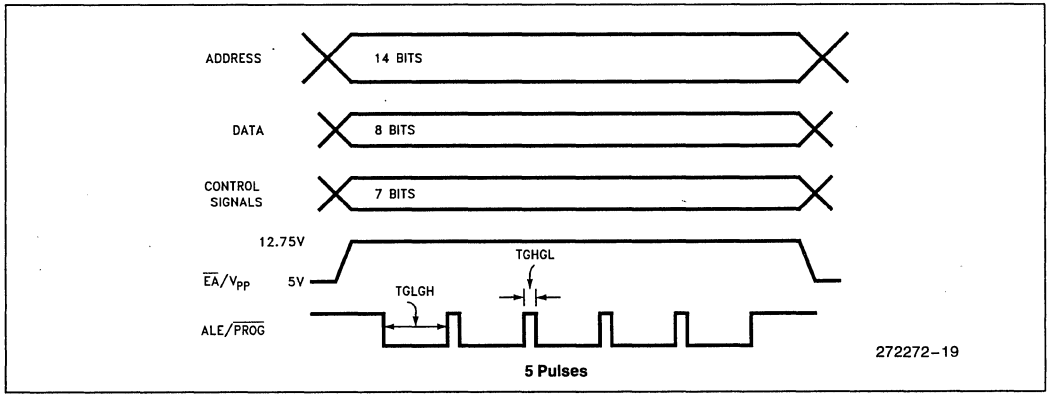


Figure 11. Programming Signal's Waveforms

Reading the Signature Bytes

The 87C52-20/80C52-20 each has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Content	
	87C52-20	80C52-20
30H	89H	89H
31H	58H	58H/53H
60H	52H	52H/12H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

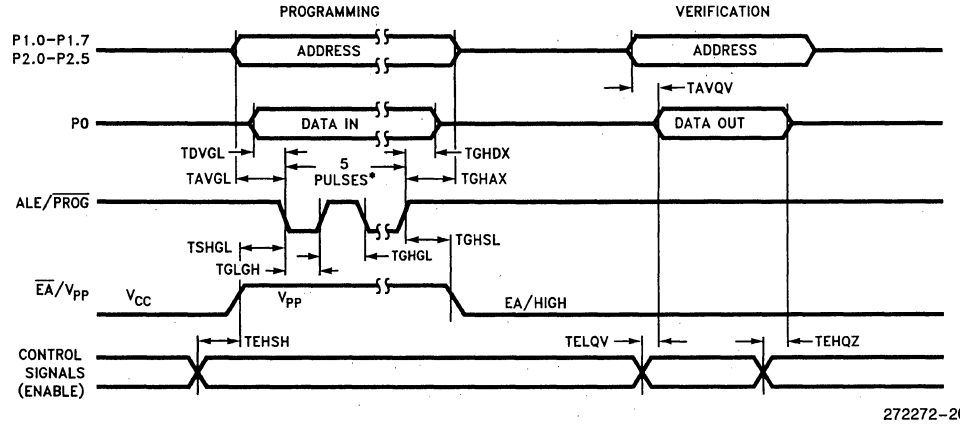
Erasure leaves all the EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		μs
TGLGH	$\overline{PROG}$ Width	90	110	μs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		μs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



NOTE:
*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits

DATA SHEET REVISION HISTORY

This is Rev. 1 of the 87C52-20/80C52-20/80C32-20 data sheet.

7

intel®

87C54/80C54
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 16 KBYTES INTERNAL PROGRAM MEMORY

87C54/80C54—3.5 MHz to 12 MHz, V_{CC} = 5V ± 20%
87C54-1/80C54-1—3.5 MHz to 16 MHz, V_{CC} = 5V ± 20%
87C54-L/80C54-L—3.5 MHz to 8 MHz, V_{CC} = 3.3V ± 0.3V

- High Performance CHMOS EPROM
- Low Voltage Operation (-L only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Up/Down Timer/Counter
- Three Level Program Lock System
- 16K On-Chip EPROM/ROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 6 Interrupt Sources
- Programmable Serial Channel with:
  — Framing Error Detection
  — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode
- Four-Level Interrupt Priority

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 16 Kbytes of the program memory can reside in the on-chip EPROM. The device can also address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C54/80C54 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 87C54/80C54 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 87C54/80C54 is an enhanced version of the 87C51/80C51BH. It's added features make it an even more powerful microcontroller for applications that require clock output, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

Applications that require low voltage can use the 87C54-L/80C54-L. The 8XC54-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz.

Throughout this document 8XC54 will refer to both the 87C54 and the 80C54.

October 1992
Order Number: 270816-004

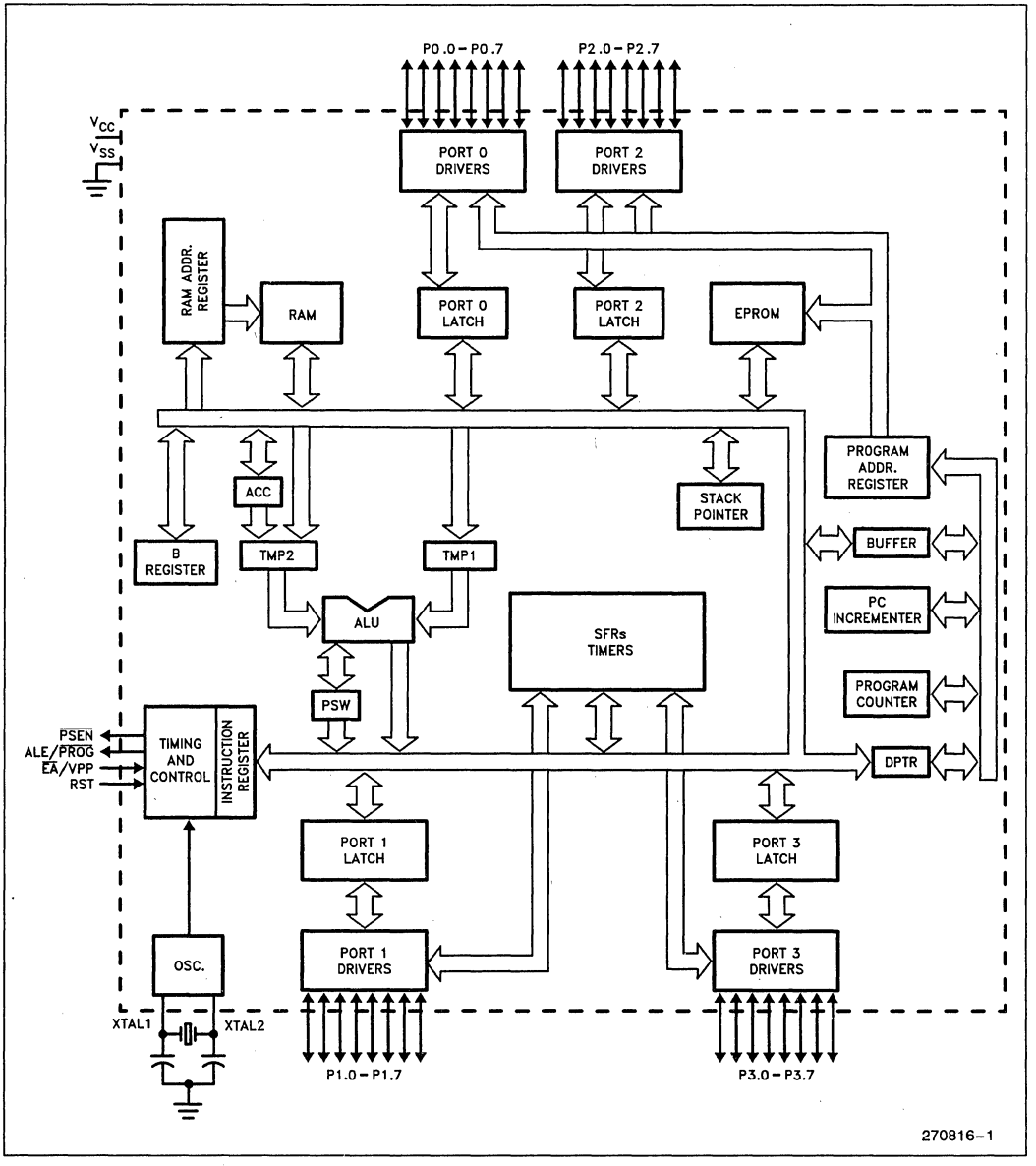


Figure 1. 8XC54 Block Diagram

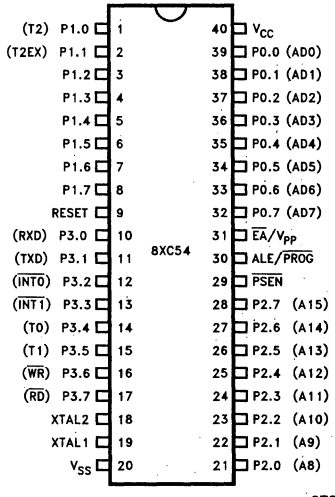
PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

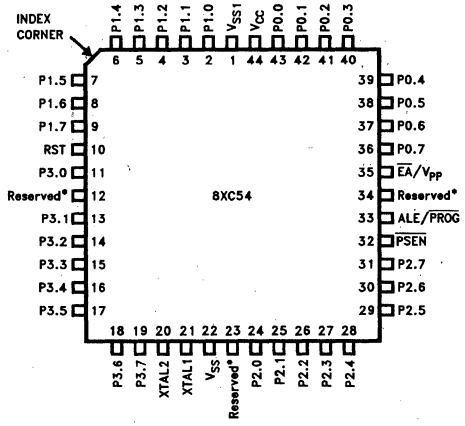
Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC54	P	40-Pin Plastic DIP (OTP)	45°C/W	16°C/W
87C54	D	40-Pin CERDIP (EPROM)	45°C/W	15°C/W
8XC54	N	44-Pin PLCC (OTP)	46°C/W	16°C/W
8XC54	S	44-Pin QFP (OTP)	96°C/W	24°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



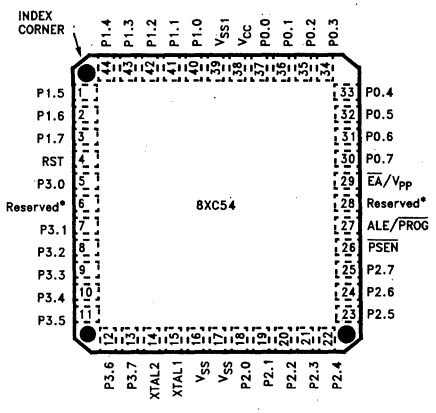
270816-2

DIP



270816-3

PLCC



270816-21

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22).

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC54:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IHI} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C54.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC54 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

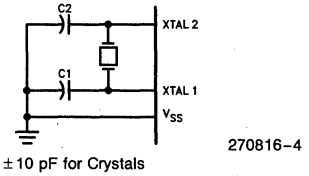
This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

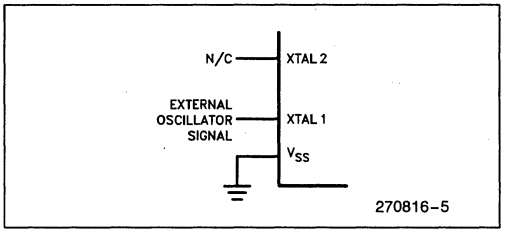


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC54 either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

DESIGN CONSIDERATION

- The 8XC54-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz. Operating beyond these specifications could cause improper device functionality. (To program the 87C54-L, follow the same procedure as the 87C54.)
- The window on the 87C54 must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC54 without the 8XC54 having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC54 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation..... 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions", may affect device reliability.*

Operating Conditions:

T_A (under bias) = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V (8XC54-L, V_{CC} = 3.3V ±0.3V)

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to both 5V and 3.3V devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$)	V_{CC}−0.3			V	I_{OH} = −10 μA
		V_{CC}−0.7			V	I_{OH} = −30 μA
		V_{CC}−1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC}−0.3			V	I_{OH} = −200 μA
		V_{CC}−0.7			V	I_{OH} = −3.2 mA
		V_{CC}−1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)			−650	μA	V_{IN} = 2V

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

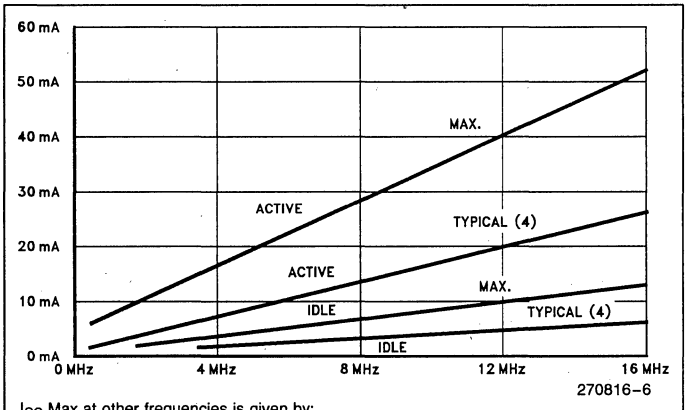
All parameter values apply to both 5V and 3.3V devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current:					(Note 3)
	Active Mode					
	8XC54-L at 8 MHz			12	mA	
	all others at 12 MHz (Figure 5)		20	40	mA	
	Idle Mode at 12 MHz (Figure 5)		5	10	mA	
	Power Down Mode		15	100	μA	

NOTES:

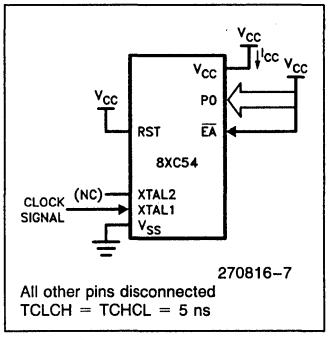
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 5. I_{CC} vs Frequency



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode

7

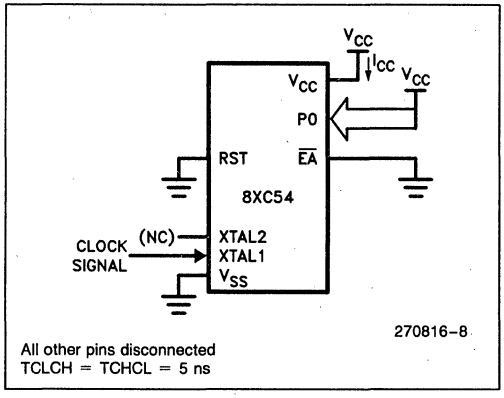


Figure 7. I_{CC} Test Condition Idle Mode

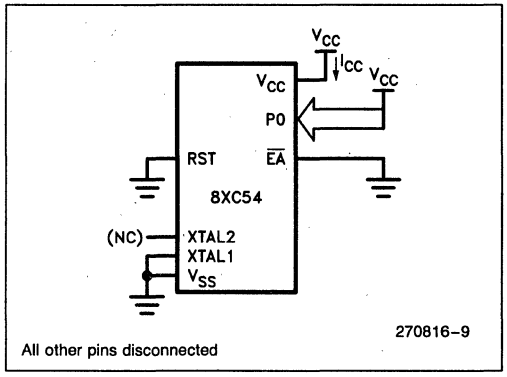


Figure 8. I_{CC} Test Condition, Power Down Mode V_{CC} = 2.0V to 6.0V

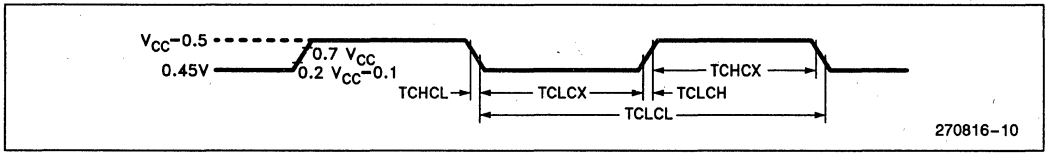


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

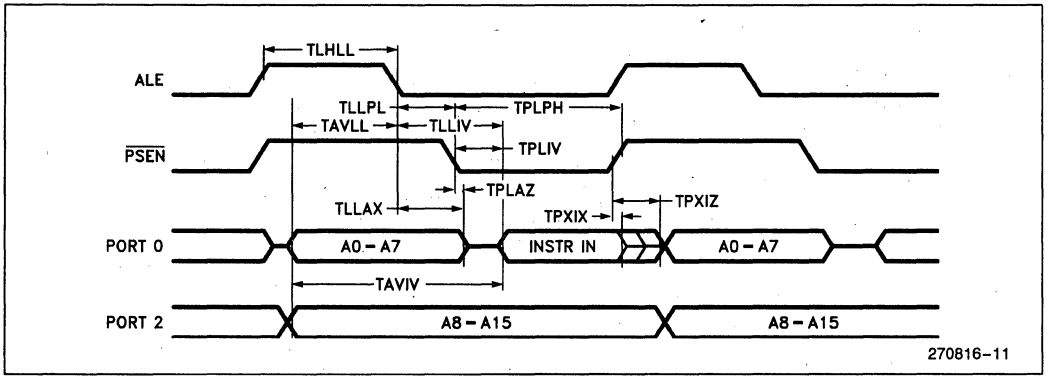
AC CHARACTERISTICS (Over Operating Conditions.) Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and $\overline{\text{PSEN}}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

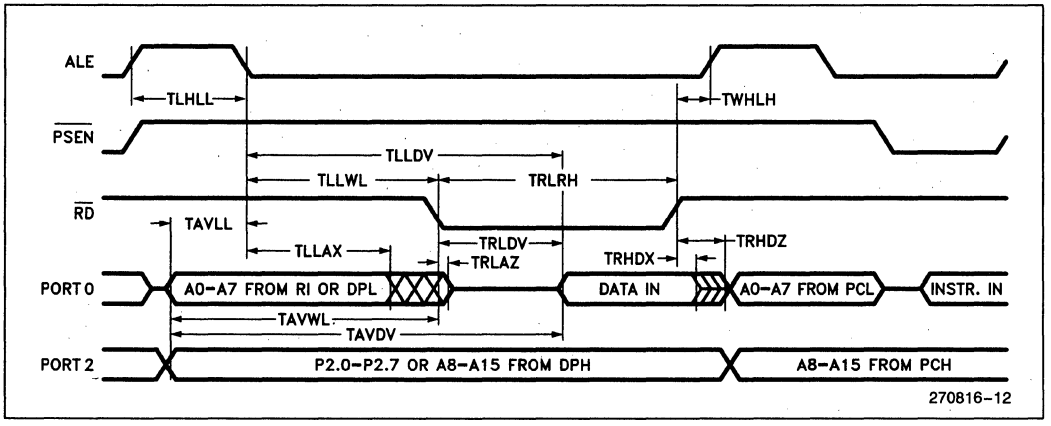
Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	53		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	53		TCLCL−30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		3TCLCL−105	ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{\text{PSEN}}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		312		5TCLCL−105	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		107		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{\text{WR}}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid before $\overline{\text{WR}}$	33		TCLCL−50		ns
TWHQX	Data Hold after $\overline{\text{WR}}$	33		TCLCL−50		ns
TQVWH	Data Valid to $\overline{\text{WR}}$ High	433		7TCLCL−150		ns
TRLAZ	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

7

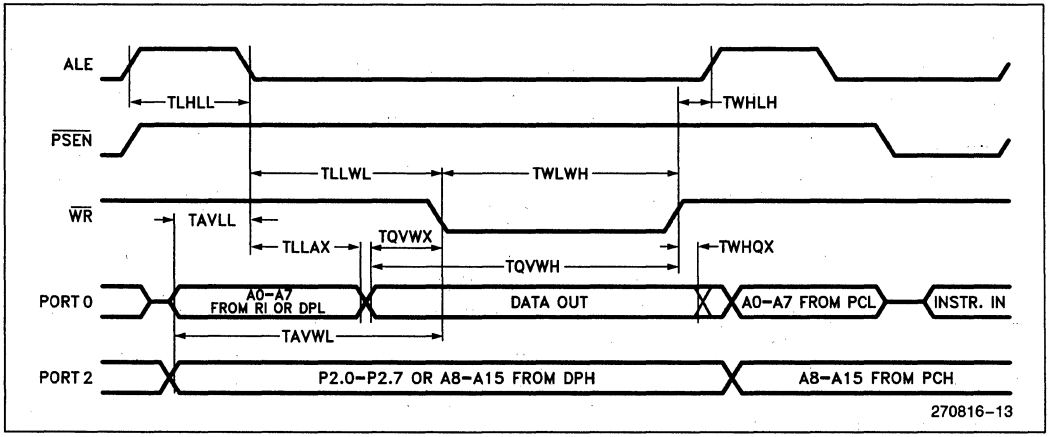
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

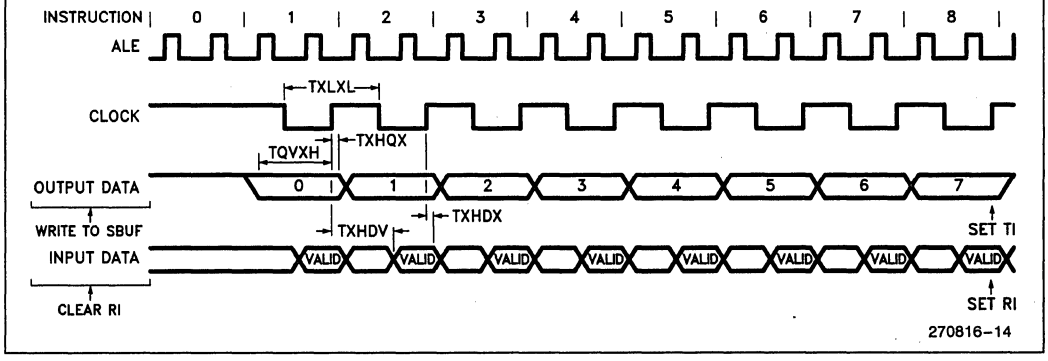


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

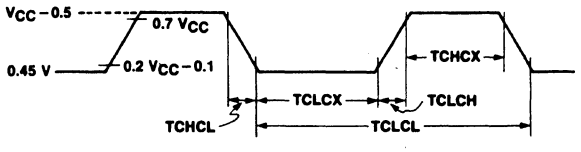
SHIFT REGISTER MODE TIMING WAVEFORMS



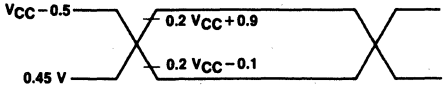
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XC54 8XC54-1	 3.5 3.5	 12 16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



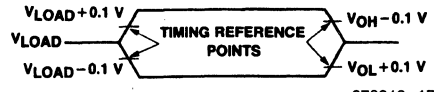
AC TESTING INPUT, OUTPUT WAVEFORMS



270816-16

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



270816-17

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA. (-L, $I_{OL}/I_{OH} = \pm 10$ mA)

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5 respectively for A0–A13.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

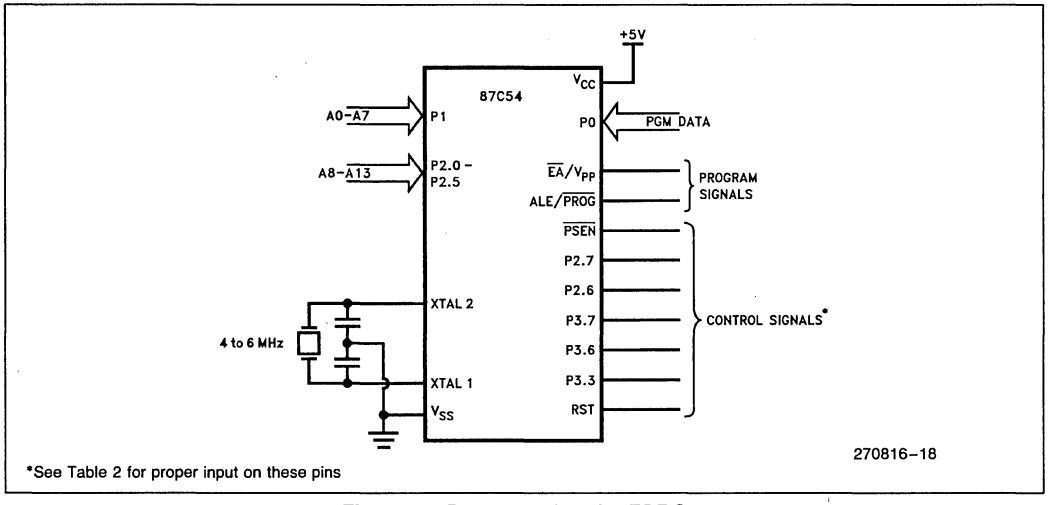


Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C54 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C54.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

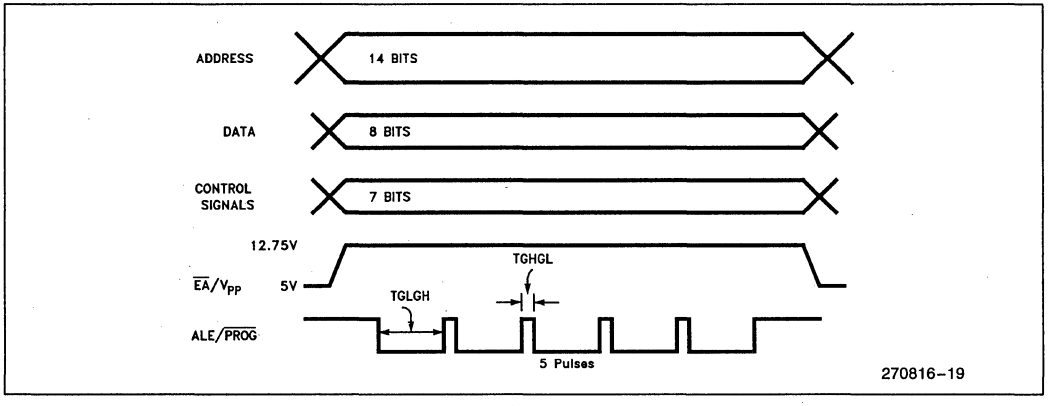


Figure 11. Programming Signal's Waveforms

Reading the Signature Bytes

The 87C54/80C54 each has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Content	
	87C54	80C54
30H	89H	89H
31H	58H	58H
60H	54H	54H/14H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

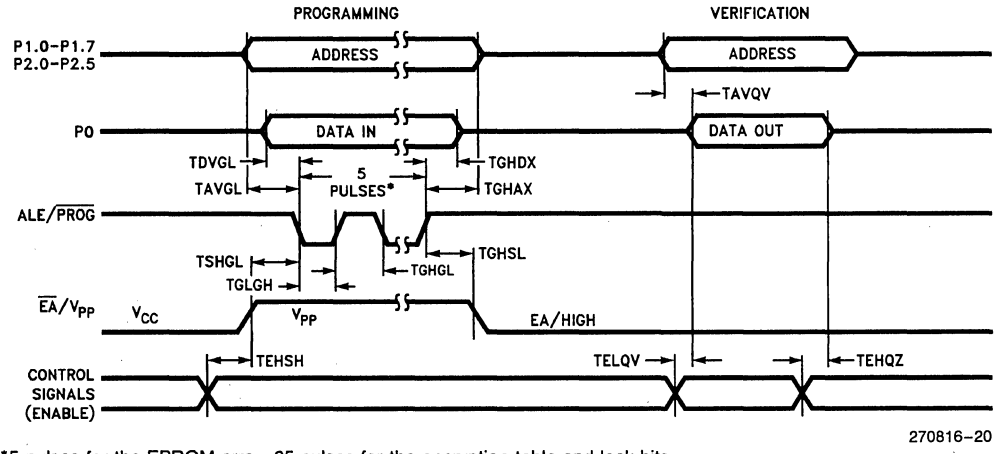
Erasure leaves all the EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		μs
TGLGH	$\overline{PROG}$ Width	90	110	μs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		μs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

DATA SHEET REVISION HISTORY

The following differences exist between this data sheet (270816-004) and the previous version (270816-003):

1. Added 3.3V device to data sheet.
2. Data sheet status changed from "Preliminary" to "Production".
3. References to second functions of Port 1.2 thru Port 1.7 pins have been removed.
4. The Operating Temperature Range has been changed to: 0°C to +70°C.

The following differences exist between the -003 and -002 versions of this data sheet:

1. QFP package type added.
2. "NC" pin labels changed to "Reserved" in Figure 2.
3. θ_{ja} and θ_{jc} information added to Packages table.
4. Capacitor value for ceramic resonators deleted in Figure 3.
5. Pin numbers deleted from Figure 10.
6. Second paragraph under "Encryption Array" section added.
7. All references to Program Lock Bit and Encryption Array deleted from "Program Verification" section. This information is available in the hardware description.

The following differences exist between the -002 and the -001 versions of the 87C54/80C54 data sheet:

1. Changed data sheet status from "Advanced" to "Preliminary".
2. Added "Four-Level Interrupt Priority" feature bullet.
3. Revised RST pin description.
4. Changed Figure 3 to read "= 40 pF ±10 pF for Ceramic Resonators".
5. Added V_{IL1} specification to DC Characteristics table.
6. Changed test conditions under I_{LI} from 0V to 0.45V for V_{IN} minimum.
7. Revised Absolute Maximum Ratings warning and data sheet status notice.
8. Reworded DC Characteristics Note 1.
9. Changed 1/TCLCL Minimum specification from 0.5 MHz to 3.5 MHz.
10. Deleted -2 reference in "External Clock Drive" table.
11. Revised "ROM and EPROM Lock System" section.

7

87C54/80C54

EXPRESS

87C54/80C54—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C54-1/80C54-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%

- **Extended Temperature Range**
- **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here. This data sheet is valid in conjunction with the commercial 87C54/80C54 data sheet, 270816-002.

October 1990
Order Number: 270901-001

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 20\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		−750	μA	$V_{IN} = 2V$

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
D*	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD*	Cerdip	Extended	No
TN	PLCC	Extended	No
LP	Plastic	Extended	Yes
LD*	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

*Available for 87C54 only.

NOTE:
- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-in is dynamic for a minimum time of 168 hours at 125°C, $V_{CC} = 6.9V \pm 0.25V$, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples:

P80C54 indicates 80C54 in a plastic package and specified for commercial temperature range, without burn-in.
LD80C54 indicates 80C54 in a cerdip package and specified for extended temperature range with burn-in.

7

DATA SHEET REVISION SUMMARY

This is Rev. 1 of the 80C54/87C54 Express data sheet.

intel®

87C54-20/-3
80C54-20/-3
COMMERCIAL/EXPRESS 20 MHz MICROCONTROLLER

87C54-20/80C54-20—3.5 MHz to 20 MHz, V_{CC} = 5V ±20%
87C54-3/80C54-3—24 MHz Internal Operation, V_{CC} = 5V ±20%

- High Performance CHMOS EPROM
- 24 MHz Internal Operation (-3 only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Up/Down Timer/Counter
- Three Level Program Lock System
- 16K On-Chip EPROM/ROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 6 Interrupt Sources
- Programmable Serial Channel with:
  — Framing Error Detection
  — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode
- Four-Level Interrupt Priority

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 16 Kbytes of the program memory can reside in the on-chip EPROM. The device can also address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 8XC54-20/-3 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 8XC54-20/-3 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 8XC54-20/-3 is an enhanced version of the 87C51/80C51BH. Its added features make it an even more powerful microcontroller for applications that require clock output, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

The 87C54-3/80C54-3 has the same 3.5 MHz to 20 MHz frequency range as the 87C54-20/80C54-20 when operating out of external program/data memory. When running out of internal program/data memory, the 87C54-3/80C54-3 can operate up to 24 MHz.

Throughout this document 8XC54-20 will refer to the 87C54-20, 80C54-20, 87C54-3 and the 80C54-3.

October 1992
Order Number: 270941-003

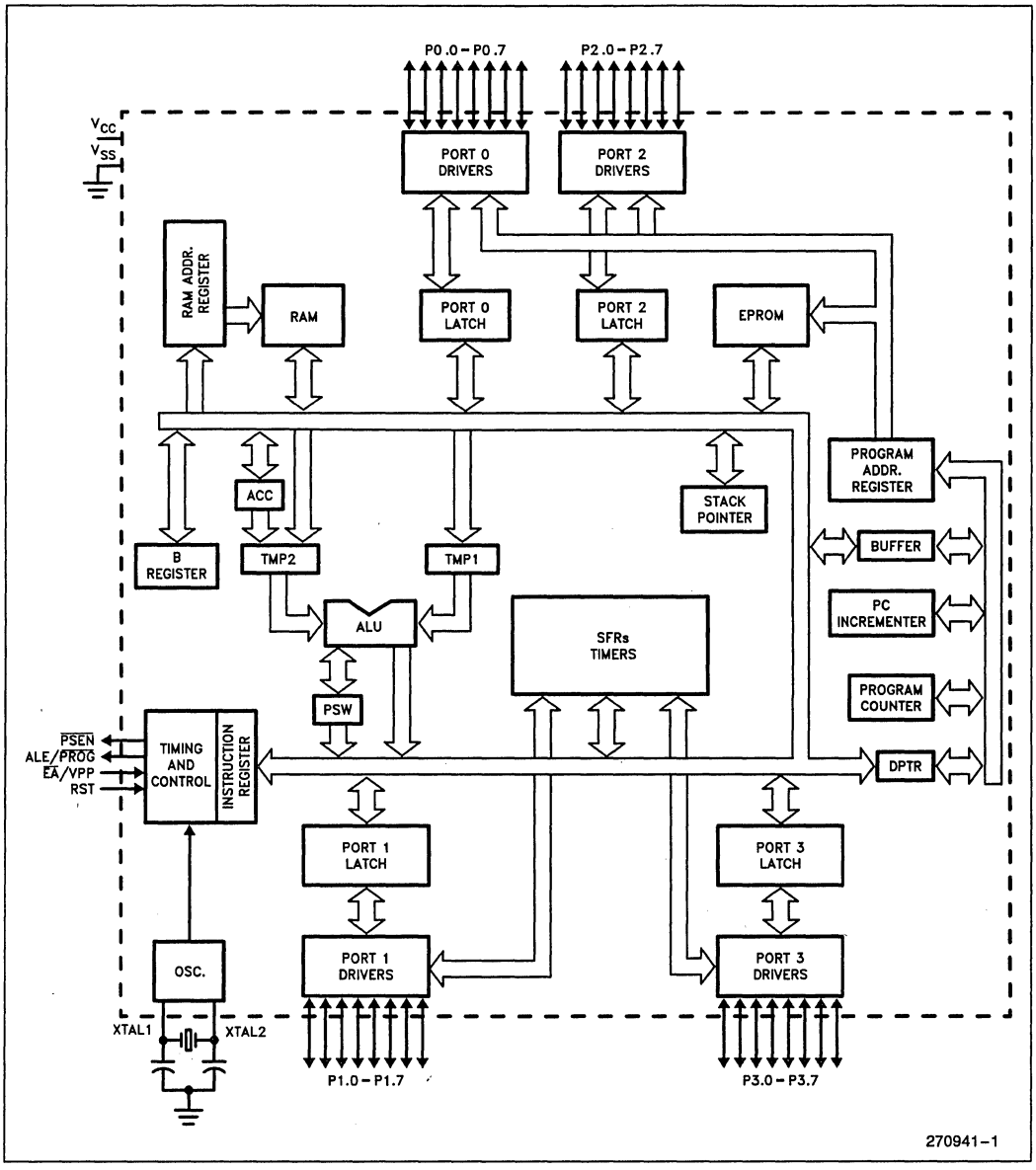


Figure 1. 8XC54-20 Block Diagram

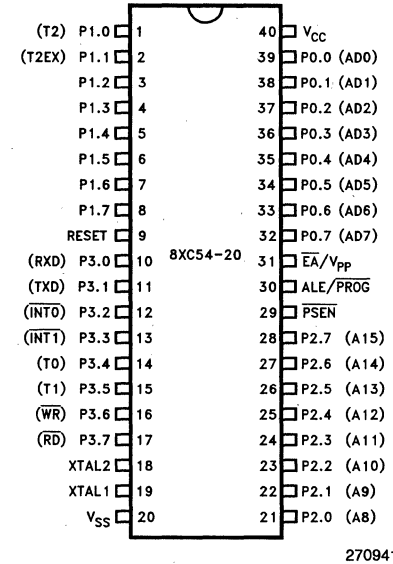
PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.

PACKAGES

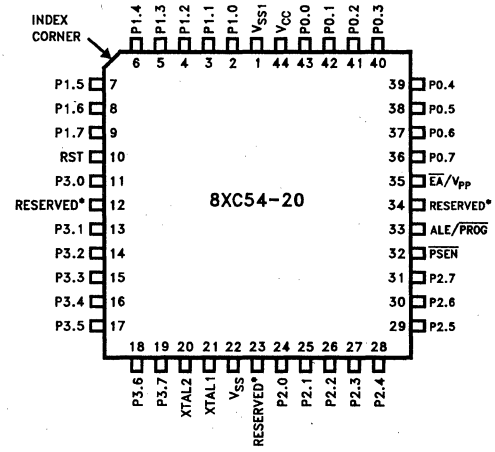
Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC54-20	P	40-Pin Plastic DIP	45°C/W	16°C/W
87C54-20	D	40-Pin CERDIP	45°C/W	15°C/W
8XC54-20	N	44-Pin PLCC	46°C/W	16°C/W
8XC54-20	S	44-Pin QFP	96°C/W	24°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



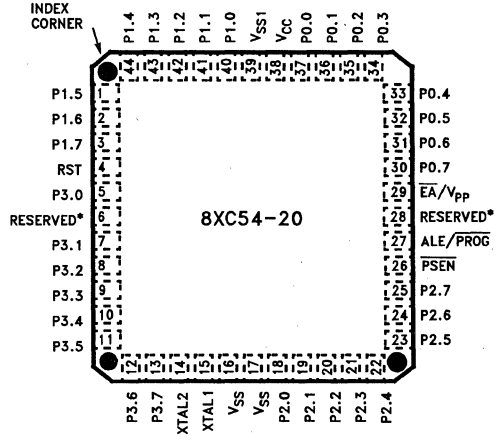
270941-2

DIP



270941-3

PLCC



270941-4

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22).

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC54-20:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IHI} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C54-20.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC54-20 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

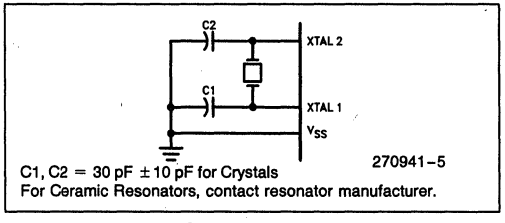


Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

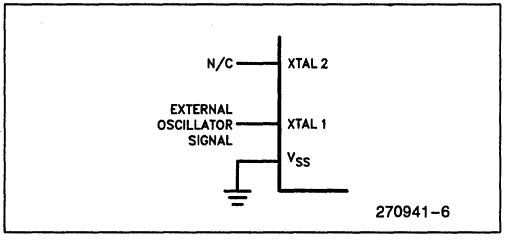


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC54-20 either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

TIMER 2 PROGRAMMABLE CLOCK OUT

The 8XC54-20 has a new Timer 2 feature. A 50% duty cycle clock can be programmed to come out on P1.0. The output frequency ranges from 61 Hz to 4 MHz depending on the oscillator frequency and the reload value of the Timer 2 capture registers (RCAP2H, RCAP2L) as shown in the equation below:

$$\text{*Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared, and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) starts and stops the timer.

For a complete description of all Timer 2 functions, please reference the 8XC52/54/58 Hardware Description of the 8-Bit Embedded Controllers Handbook.

***NOTE:**
Even though the equation permits a maximum clock-out frequency of 5 MHz using a 20 MHz oscillator, the maximum device output frequency is 4 MHz. When using a 20 MHz oscillator, RCAP2L must be limited to a maximum value of FEH.

DESIGN CONSIDERATION

- When running out of internal program/data memory, the 87C54-3/80C54-3 can be operated using a 24 MHz clock. If the 87C54-3/80C54-3 is running out of external program/data memory, the operating frequency must be between 3.5 MHz to 20 MHz. The 87C54-3/80C54-3 will not function properly at 24 MHz when running out of external program/data memory.
- The window on the 87C54-20 must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC54-20 without the 8XC54-20 having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{\text{PSEN}}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{\text{PSEN}}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC54-20 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency	3.5	20	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA
		V_{CC} − 0.7			V	I_{OH} = −30 μA
		V_{CC} − 1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC} − 0.3			V	I_{OH} = −200 μA
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	V_{IN} = 0.45V

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

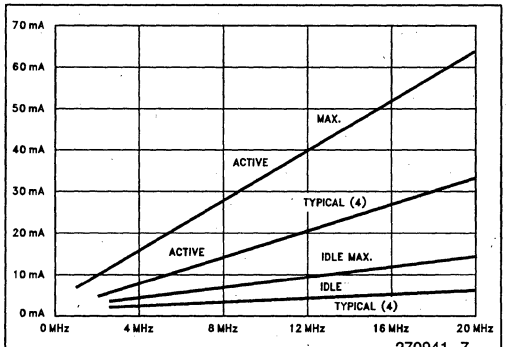
Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
I_{LI}	Input Leakage Current (Port 0)			±10	μA	$0.45 < V_{IN} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3) Commercial Express			 −650 −750	 μA μA	 V_{IN} = 2V
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Running at 12 MHz (Figure 5) Idle Mode at 12 MHz (Figure 5) Power Down Mode		 20 5 15	 40 10 100	 mA mA μA	(Note 3)

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   - Maximum I_{OL} per port pin: 10 mA
   - Maximum I_{OL} per 8-bit port—
     - Port 0: 26 mA
     - Ports 1, 2 and 3: 15 mA
   - Maximum total I_{OL} for all output pins: 71 mA

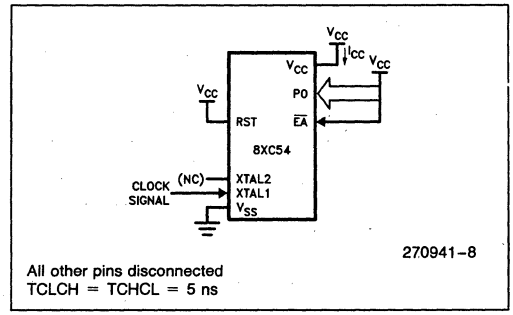
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

7



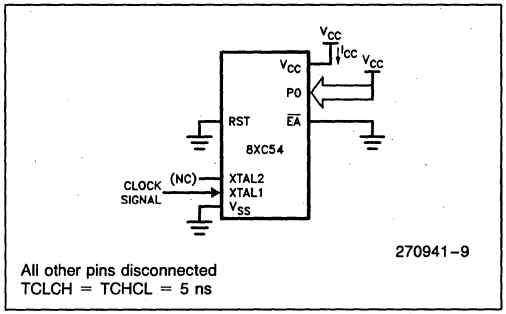
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 5. I_{CC} vs Frequency



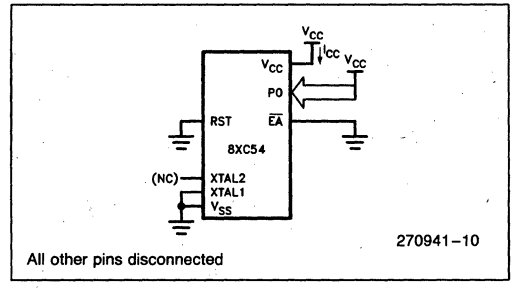
All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition Idle Mode



All other pins disconnected

Figure 8. I_{CC} Test Condition, Power Down Mode
V_{CC} = 2.0V to 6.0V

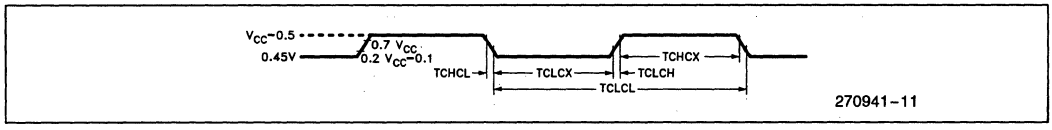


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

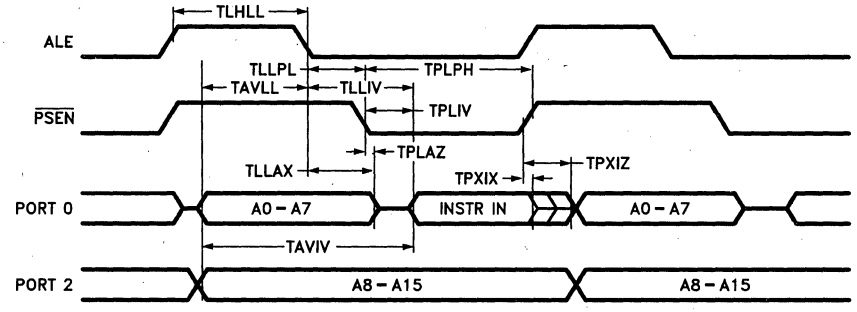
AC CHARACTERISTICS (Over Operating Conditions) Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	20	MHz
TLHLL	ALE Pulse Width	60		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	10		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	20		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		125		4TCLCL−75	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	20		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	105		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		60		3TCLCL−90	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		30		TCLCL−20	ns
TAVIV	Address to Valid Instruction In		145		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	200		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	200		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		155		5TCLCL−95	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		40		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		310		8TCLCL−90	ns
TAVDV	Address to Valid Data In		360		9TCLCL−90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	100	200	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	110		4TCLCL−90		ns
TQVWX	Data Valid before $\overline{WR}$	15		TCLCL−35		ns
TWHQX	Data Hold after $\overline{WR}$	10		TCLCL−40		ns
TQVWH	Data Valid to $\overline{WR}$ High	280		7TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	10	90	TCLCL−40	TCLCL+40	ns

7

EXTERNAL PROGRAM MEMORY READ CYCLE



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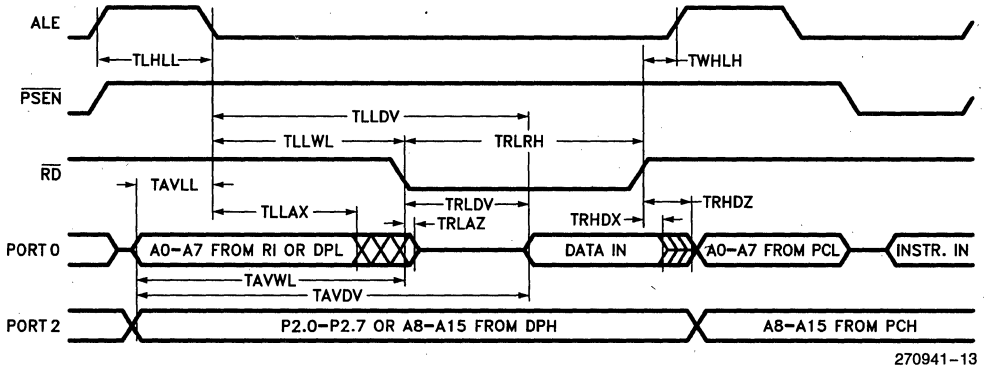
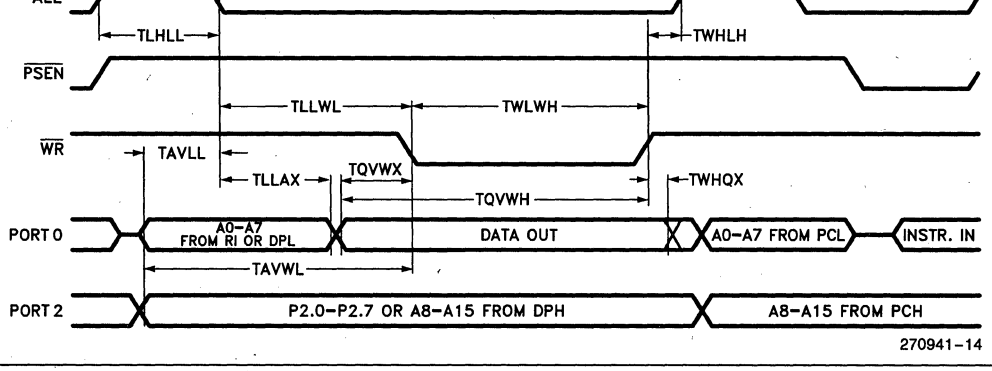
EXTERNAL DATA MEMORY READ CYCLE



270941-13

EXTERNAL DATA MEMORY WRITE CYCLE



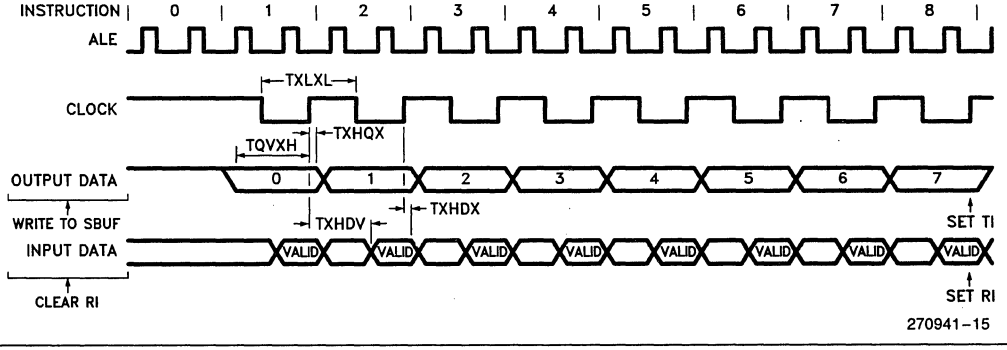
270941-14

SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	600		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	367		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		367		10TCLCL−133	ns

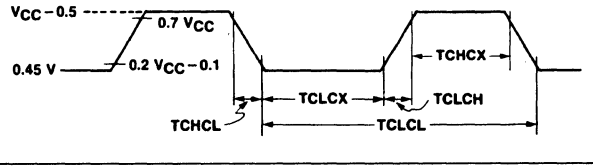
SHIFT REGISTER MODE TIMING WAVEFORMS



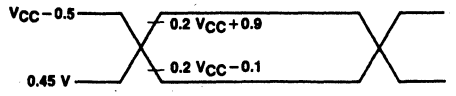
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



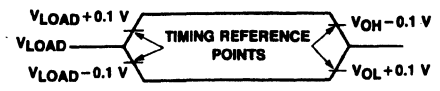
AC TESTING INPUT, OUTPUT WAVEFORMS



270941-17

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



270941-18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5 respectively for A0–A13.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

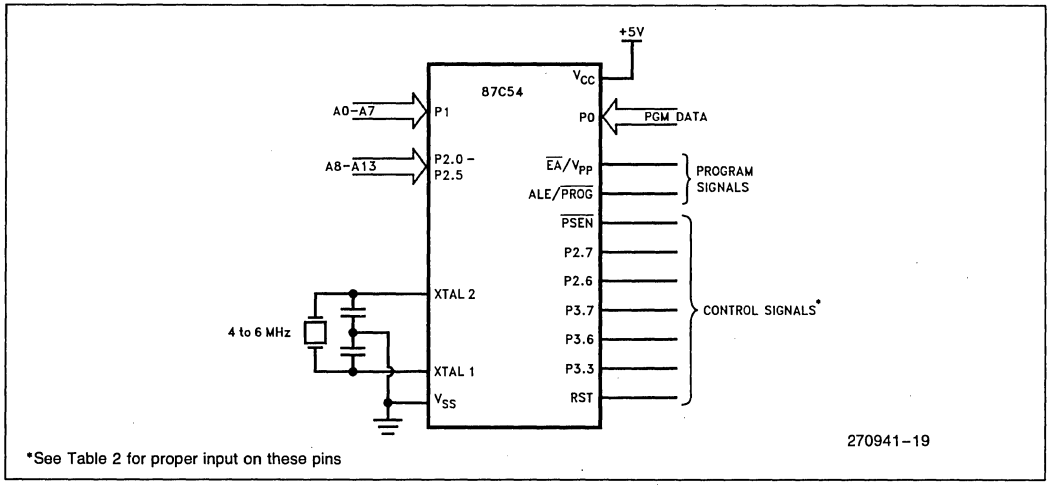


Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C54-20 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C54-20.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

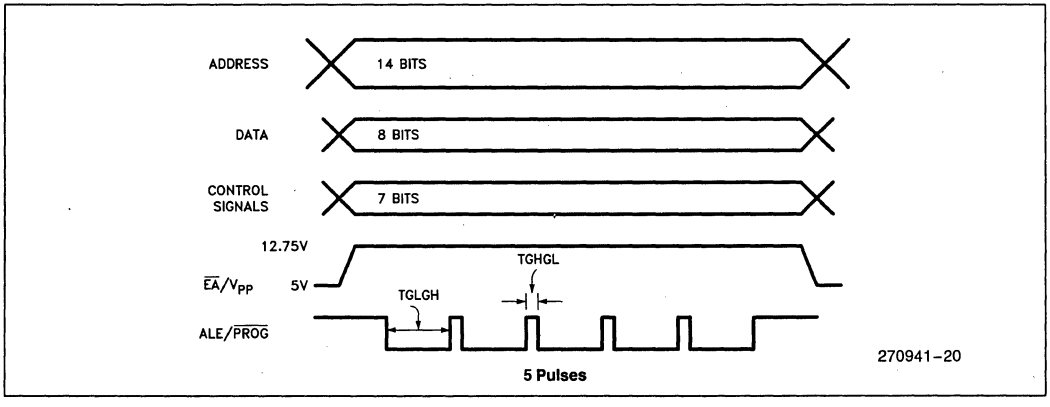


Figure 11. Programming Signal's Waveforms

Reading the Signature Bytes

The 87C54-20/80C54-20 each has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Content	
	87C54-20	80C54-20
30H	89H	89H
31H	58H	58H
60H	54H	54H/14H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

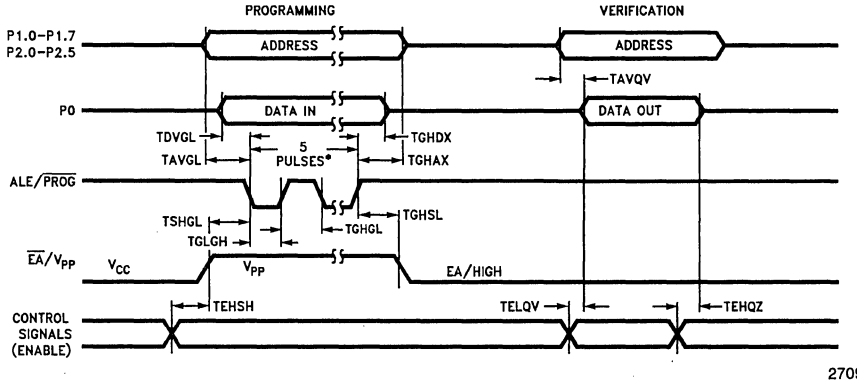
Erasure leaves all the EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		μs
TGLGH	$\overline{PROG}$ Width	90	110	μs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		μs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



270941-21

NOTE:
*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits

DATA SHEET REVISION HISTORY

The following differences exist between this data sheet (270941-003) and the previous version (270941-002):

1. Added 87C54-3/80C54-3 to 20 MHz data sheet.
2. Added EXPRESS version of 8XC54-20/-3 to 20 MHz data sheet.
3. References to second functions of Port 1.2 thru Port 1.7 pins have been removed.
4. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	120 4TCLCL-80	125 4TCLCL-75
TPLIV	3TCLCL-95	3TCLCL-90
TWHQX	0 TCLCL-50	10 TCLCL-40
TQVWH	200 7TCLCL-150	280 7TCLCL-70

The following differences exist between the -002 and -001 versions of this data sheet:

1. "NC" pin labels changed to "Reserved" in Figure 2.
2. θ_{ja} and θ_{jc} information added to Packages table.
3. Capacitor value for ceramic resonators deleted in Figure 3.
4. Serial Port Timings under "20 MHz Oscillator" corrected to agree with the variable oscillator equations for TXLXL, TQVXH and TXHDV.
5. Pin numbers deleted from Figure 10.
6. Second paragraph under "Encryption Array" section added
7. All references to Program Lock Bit and Encryption Array deleted from "Program Verification" section. This information is available in the hardware description.

intel®

87C58/80C58
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 KBYTES INTERNAL PROGRAM MEMORY

87C58/80C58—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C58-1/80C58-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%
87C58-L/80C58-L—3.5 MHz to 8 MHz, V_{CC} = 3.3V ±.3V

- High Performance CHMOS EPROM
- Low Voltage Operation (-L only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Up/Down Timer/Counter
- Three Level Program Lock System
- 32K On-Chip EPROM/ROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 6 Interrupt Sources
- Four Level Interrupt Priority Structure
- Programmable Serial Channel with:
  — Framing Error Detection
  — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 32 Kbytes of the program memory can reside in the on-chip EPROM. The device can also address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C58/80C58 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 87C58/80C58 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 87C58/80C58 is an enhanced version of the 87C51/80C51BH. It's added features make it an even more powerful microcontroller for applications that require clock output, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

Applications that require low voltage can use the 87C58-L/80C58-L. The 8XC58-L will operate at 3.3V ±.3V at a frequency range of 3.5 MHz to 8 MHz.

Throughout this document 8XC58 will refer to both the 87C58 and the 80C58.

October 1992
Order Number: 270900-003

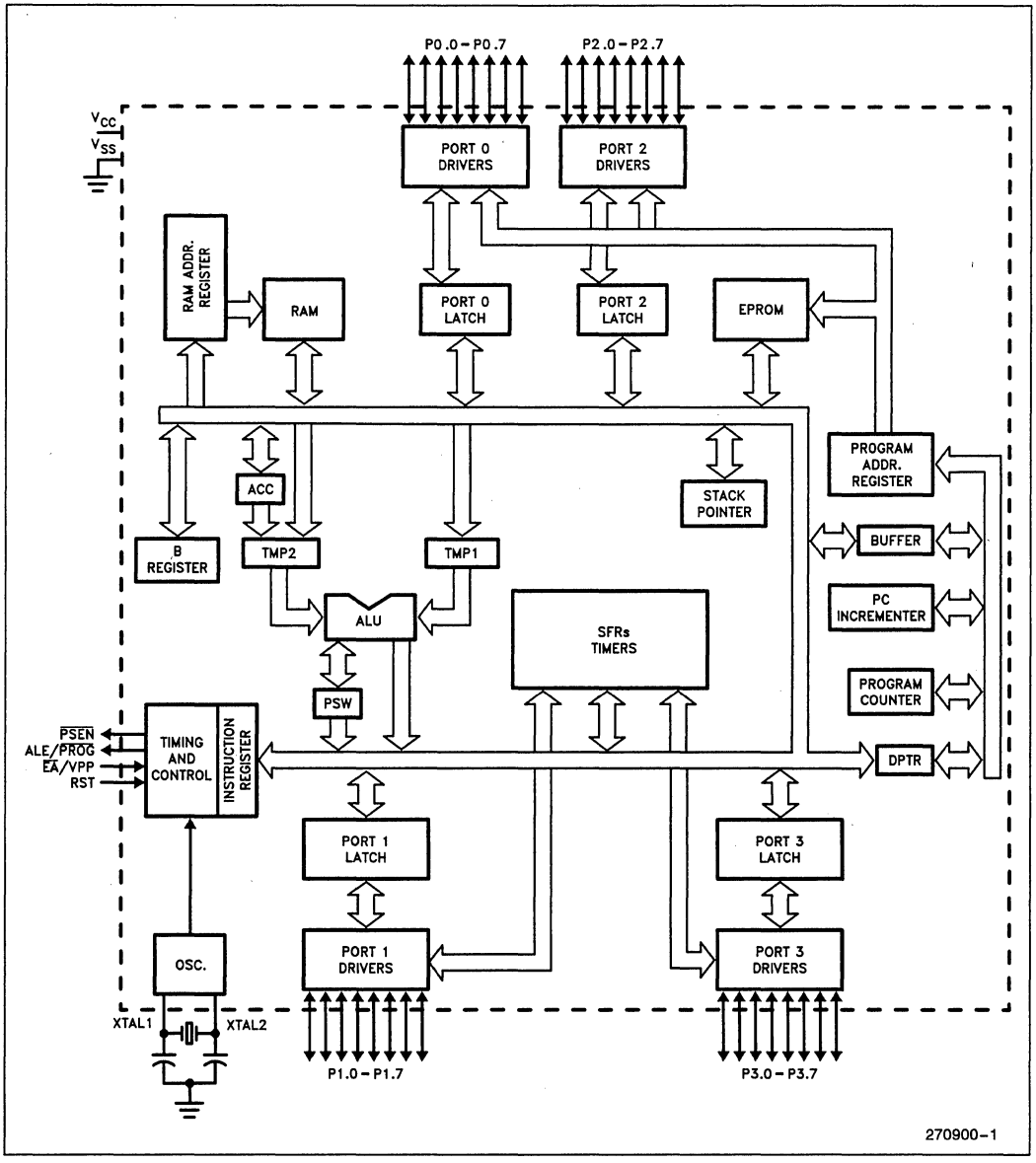


Figure 1. 8XC58 Block Diagram

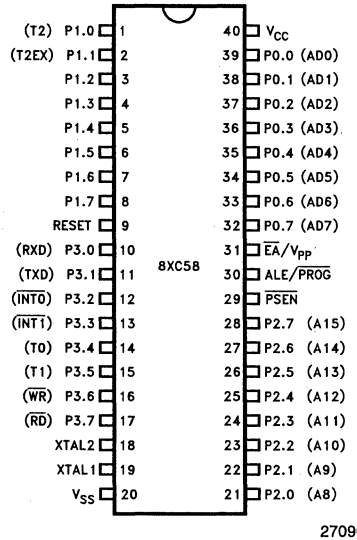
PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

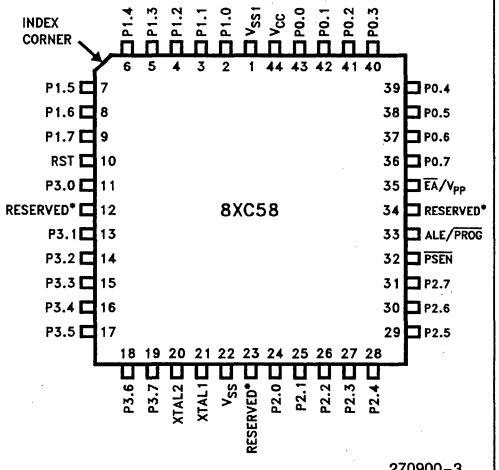
Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC58	P	40-Pin Plastic DIP (OTP)	45°C/W	16°C/W
87C58	D	40-Pin CERDIP (EPROM)	45°C/W	15°C/W
8XC58	N	44-Pin PLCC (OTP)	46°C/W	16°C/W
8XC58	S	44-Pin QFP (OTP)	90°C/W	22°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



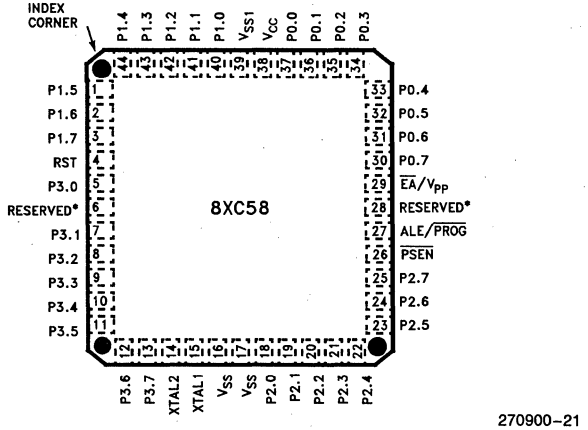
270900-2

DIP



270900-3

PLCC



270900-21

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22).

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC58:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C58.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC58 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

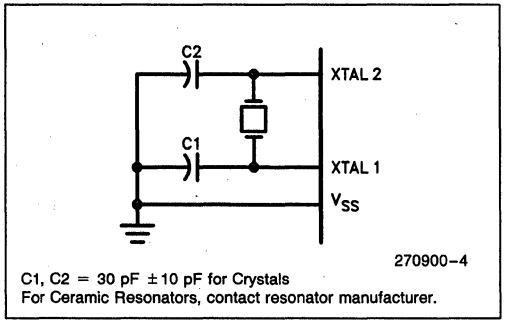


Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

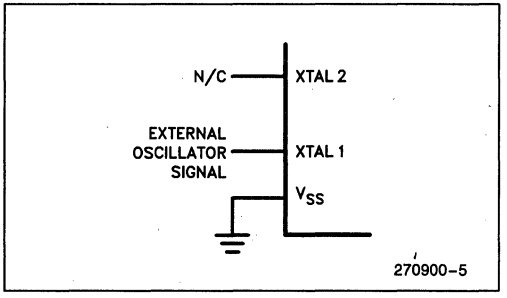


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC58 either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- The 8XC58-L will operate at 3.3V ±.3V at a frequency range of 3.5 MHz to 8 MHz. Operating beyond these specifications could cause improper device functionality. (To program the 87C58-L, follow the same procedure as the 87C58.)
- The window on the 87C58 must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC58 without the 8XC58 having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC58 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions T_A (Under Bias) = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V
(8XC58-L, V_{CC} = 3.3V ±.3V)

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to both 5V and 3.3V devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA
		V_{CC} − 0.7			V	I_{OH} = −30 μA
		V_{CC} − 1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC} − 0.3			V	I_{OH} = −200 μA
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)			−650	μA	V_{IN} = 2V

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

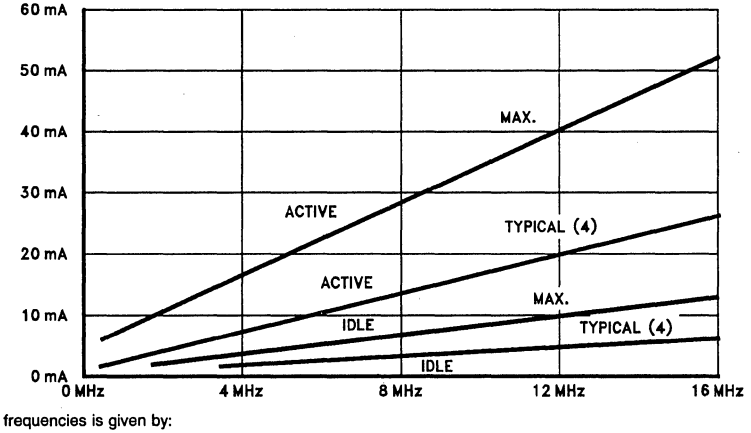
All parameter values apply to both 5V and 3.3V devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current:					(Note 3)
	Active Mode					
	8XC58-L at 8 MHz			12	mA	
	All others at 12 MHz (Figure 5)		20	40	mA	
	Idle Mode at 12 MHz (Figure 5)		5	10	mA	
	Power Down Mode		15	100	μA	

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with Schmitt triggers or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 5. I_{CC} vs Frequency

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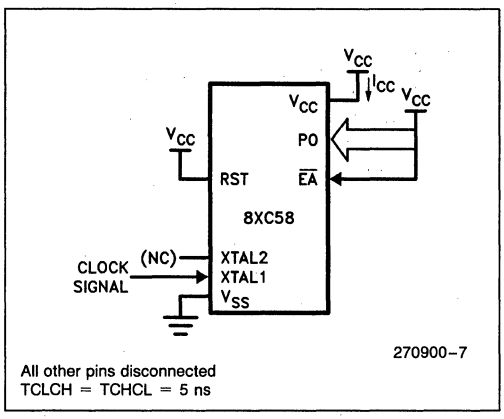

Figure 6. I_{CC} Test Condition, Active Mode

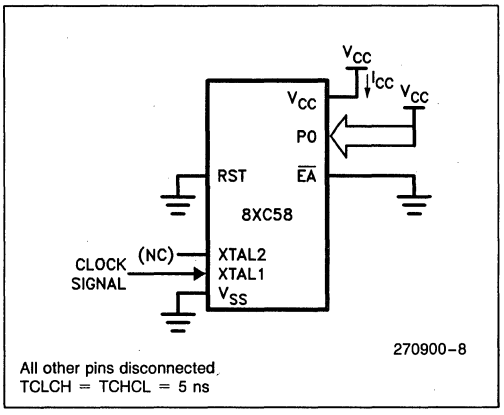

Figure 7. I_{CC} Test Condition Idle Mode

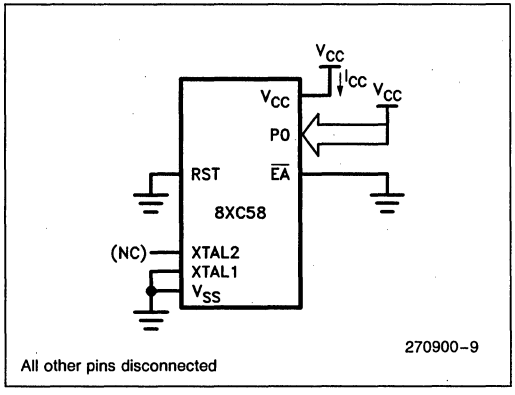

Figure 8. I_{CC} Test Condition, Power Down Mode
V_{CC} = 2.0V to 6.0V

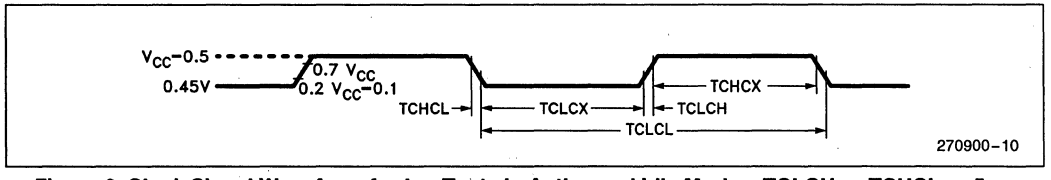

Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and $\overline{\text{PSEN}}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	53		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	53		TCLCL−30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		3TCLCL−105	ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{\text{PSEN}}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		312		5TCLCL−105	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		107		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{\text{WR}}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid before $\overline{\text{WR}}$	33		TCLCL−50		ns
TWHQX	Data Hold after $\overline{\text{WR}}$	33		TCLCL−50		ns
TQVWH	Data Valid to $\overline{\text{WR}}$ High	433		7TCLCL−150		ns
TRLAZ	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

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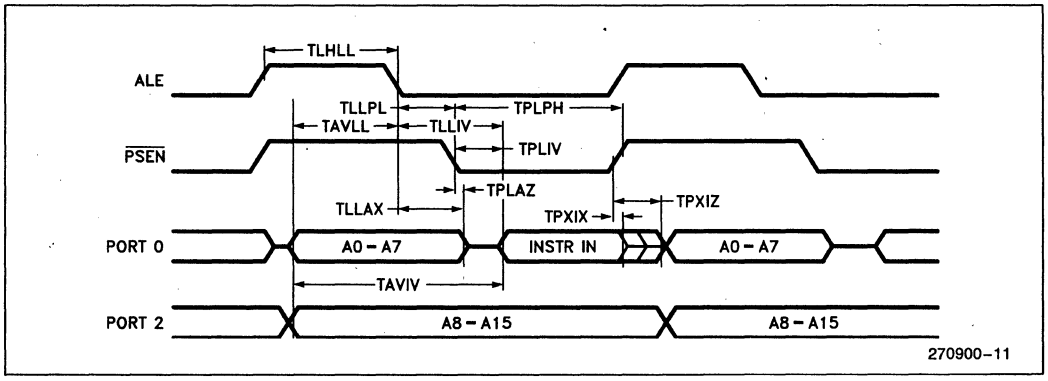
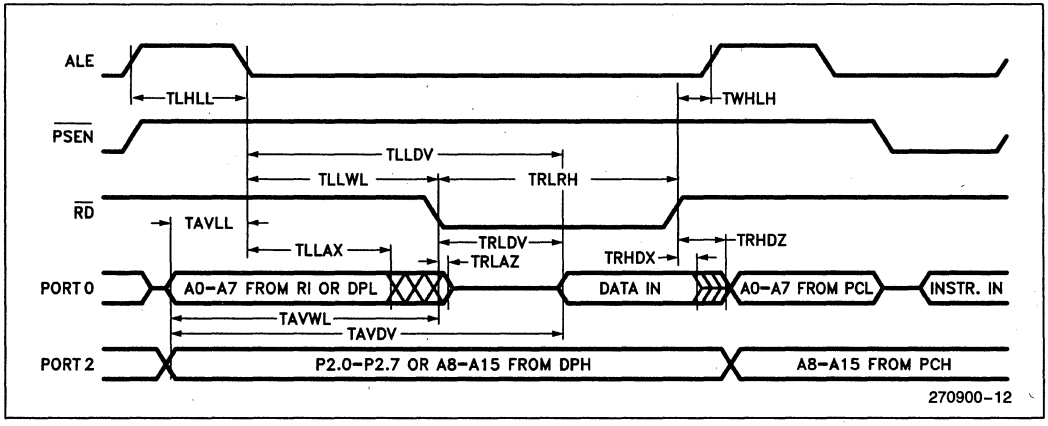
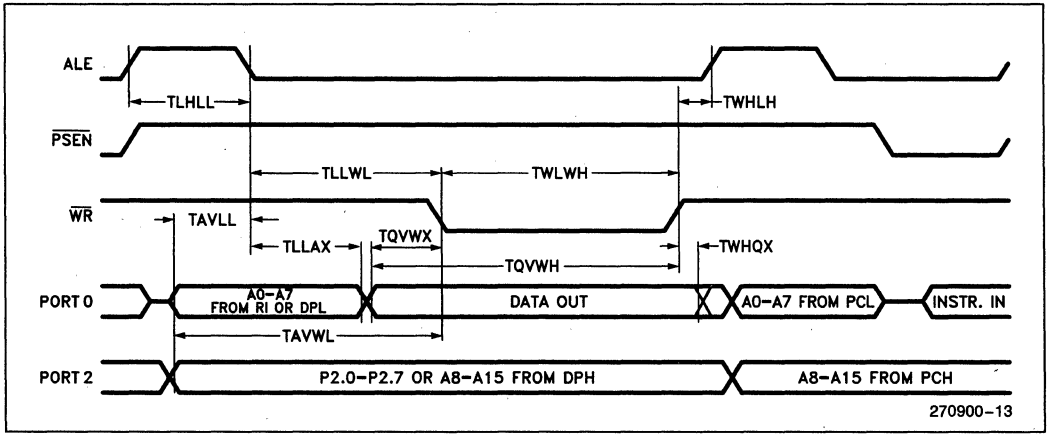
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

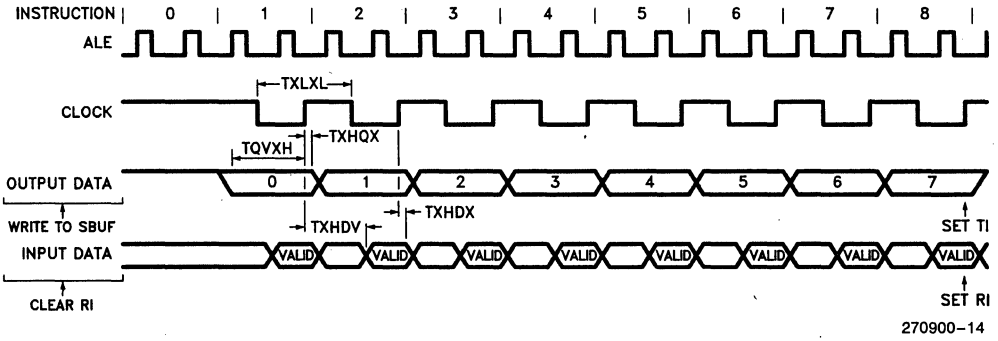


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



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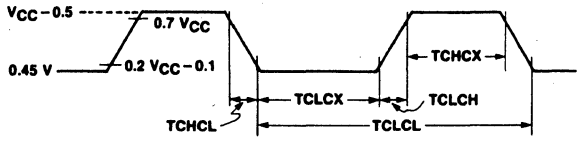
EXTERNAL CLOCK DRIVE

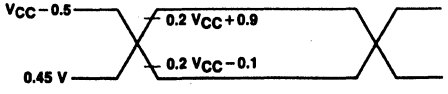
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XC58 8XC58-1	 3.5 3.5	 12 16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



270900-15

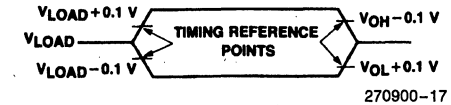
AC TESTING INPUT, OUTPUT WAVEFORMS



270900-16

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



270900-17

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA (-L, $I_{OL}/I_{OH} = \pm 10$ mA).

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4 respectively for A0–A14.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	PSEN	ALE/PROG	EA/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C58 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C58.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

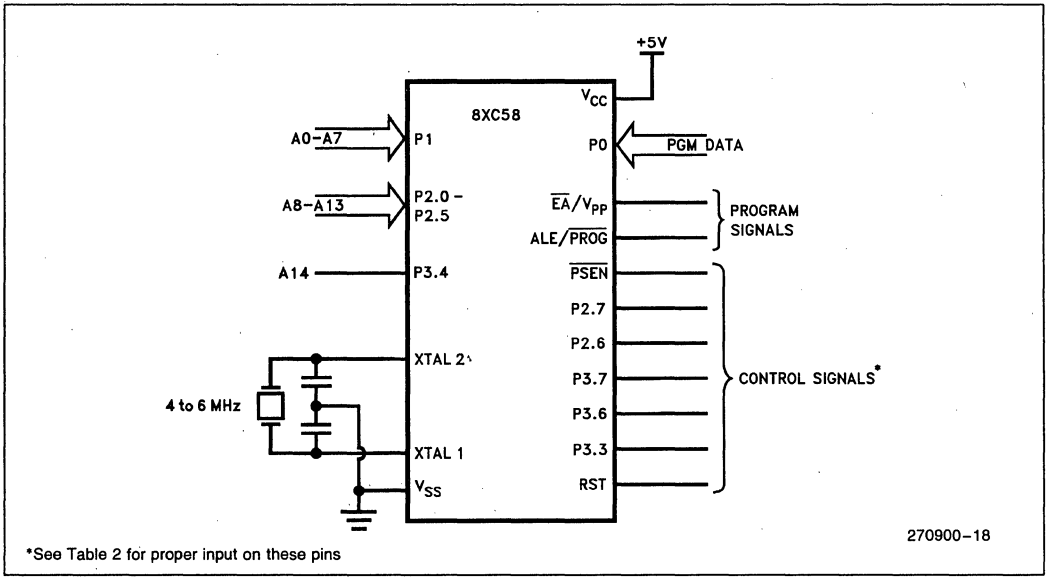


Figure 10. Programming the EPROM

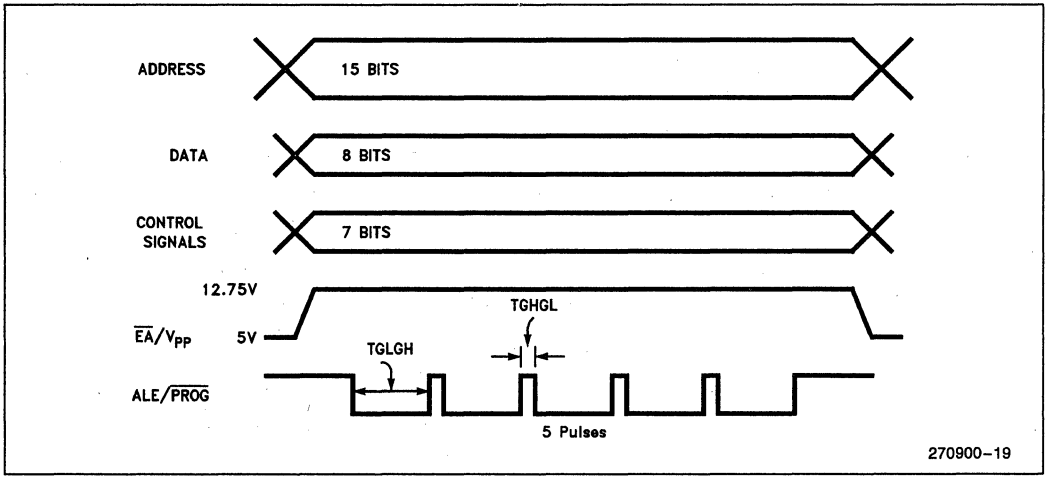


Figure 11. Programming Signal's Waveforms

Reading the Signature Bytes

The 87C58/80C58 each has 3 signature bytes in locations 30H, 31H and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Content	
	87C58	80C58
30H	89H	89H
31H	58H	58H
60H	58H	58H/18H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

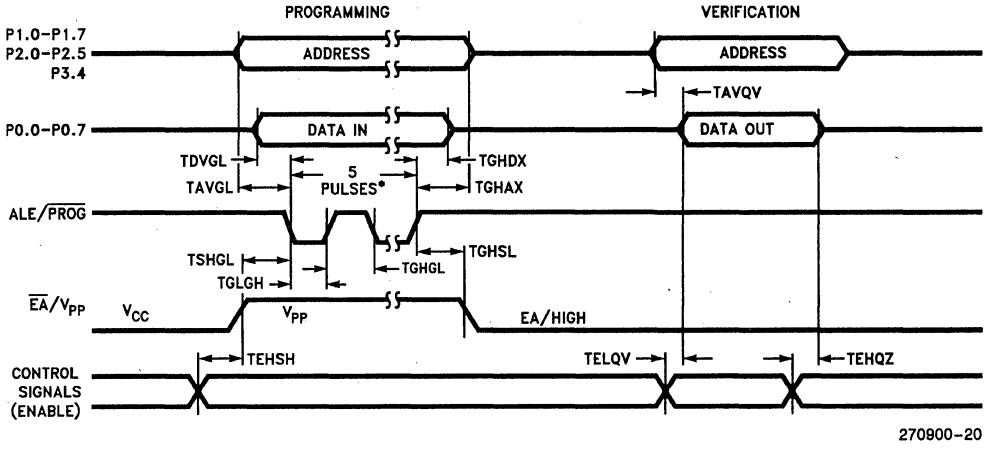
Erasure leaves all the EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



270900-20

NOTE:
*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

7

REVISION HISTORY

The following differences exist between this data sheet (270900-003) and the previous version (270900-002):

1. Added 3.3V device to data sheet.
2. Data sheet status changed from "Preliminary" to "Production".
3. The Operating Temperature Range has been changed to:
   0°C to +70°C.

The following differences exist between the -002 and -001 versions of this data sheet:

1. Data sheet status changed from "Advanced" to "Preliminary".
2. QFP package type added.
3. "NC" pin labels changed to "Reserved" in Figure 2.
4. θ_{ja} and θ_{jc} information added to Packages table.
5. Capacitor value for ceramic resonators deleted in Figure 3.
6. Pin numbers deleted from Figure 10.
7. Second paragraph under "Encryption Array" section added.
8. All references to Program Lock Bit and Encryption Array deleted from "Program Verification" section. This information is available in the hardware description.

87C58/80C58

EXPRESS

87C58/80C58—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C58-1/80C58-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%

- **Extended Temperature Range**
- **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.

This data sheet is valid in conjunction with the commercial 87C58/80C58 data sheet, 270900-001.

September 1990
Order Number: 270902-001

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 20\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		−750	μA	$V_{IN} = 2V$

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
D*	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD*	Cerdip	Extended	No
TN	PLCC	Extended	No
LP	Plastic	Extended	Yes
LD*	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

NOTE:
- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-in is dynamic for a minimum time of 168 hours at 125°C, $V_{CC} = 6.9V \pm 0.25V$, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

EXAMPLES:
P80C58 indicates 80C58 in a plastic package and specified for commercial temperature range, without burn-in.
LD80C58 indicates 80C58 in a cerdip package and specified for extended temperature range with burn-in.

*Available in EPROM version only.

DATA SHEET REVISION SUMMARY

This is the -001 version of the 87C58/80C58 Express data sheet.

87C58-20/-3
80C58-20/-3
COMMERCIAL/EXPRESS 20 MHz MICROCONTROLLER

87C58-20/80C58-20—3.5 MHz–20 MHz V_{CC} = 5V ±20%
87C58-3/80C58-3—24 MHz Internal Operation, V_{CC} = 5V ±20%

- High Performance CHMOS EPRO
- 24 MHz Internal Operation (-3 only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Up/Down Timer/Counter
- Three Level Program Lock System
- 32K On-Chip EPROM/ROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 6 Interrupt Sources
- Programmable Serial Channel with:
  — Framing Error Detection
  — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode
- Four-Level Interrupt Priority

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 32 Kbytes of the program memory can reside in the on-chip EPROM. The device can also address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 8XC58-20/-3 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 8XC58-20/-3 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 8XC58-20/-3 is an enhanced version of the 87C51/80C51BH. Its added features make it an even more powerful microcontroller for applications that require clock output and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

The 87C58-3/80C58-3 has the same 3.5 MHz to 20 MHz frequency range as the 87C58-20/80C58-20 when operating out of external program/data memory. When running out of internal program/data memory, the 87C58-3/80C58-3 can operate up to 24 MHz.

Throughout this document 8XC58-20 will refer to the 87C58-20, 80C58-20, 87C58-3 and the 80C58-3.

October 1992
Order Number: 272029-002

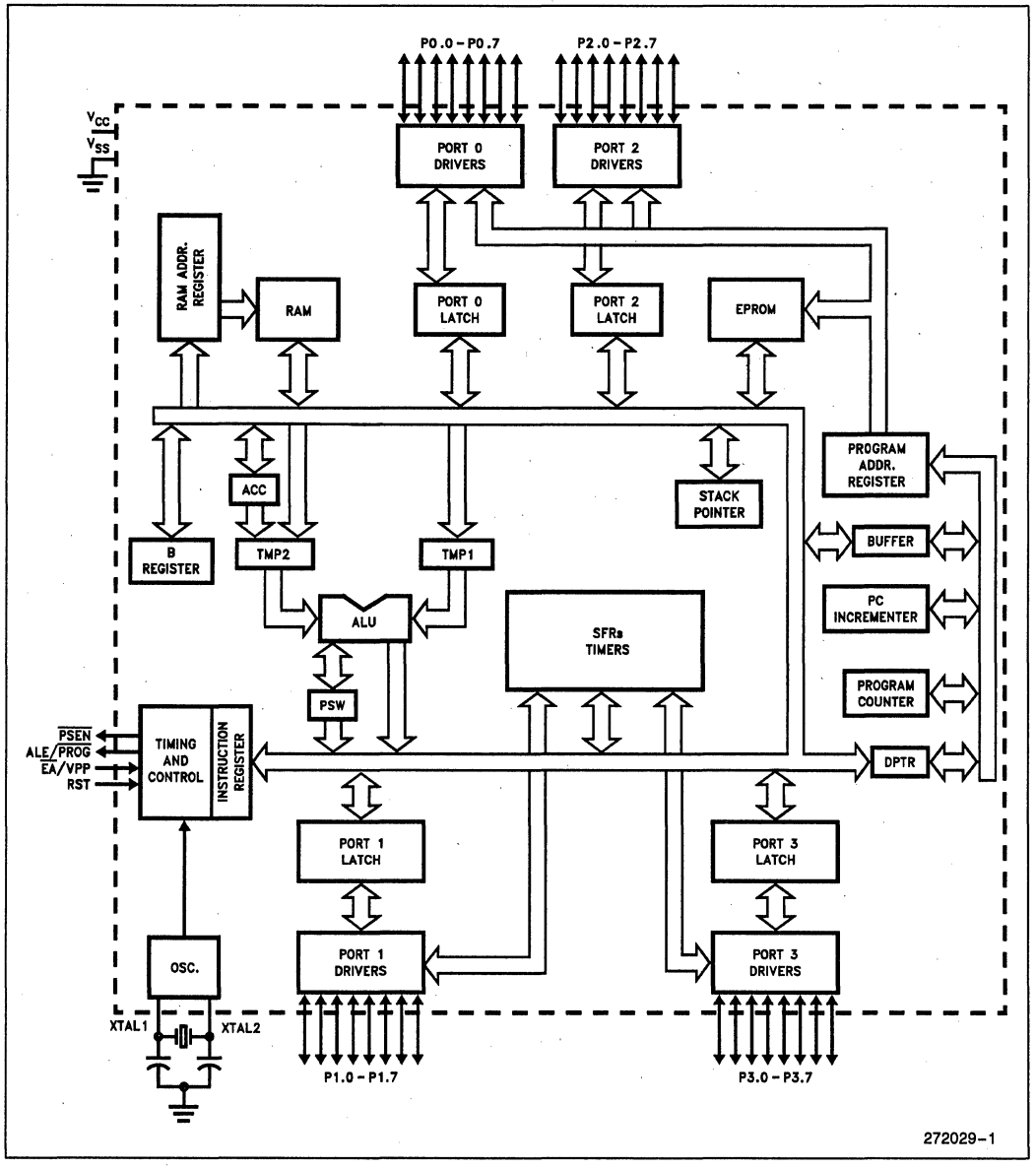


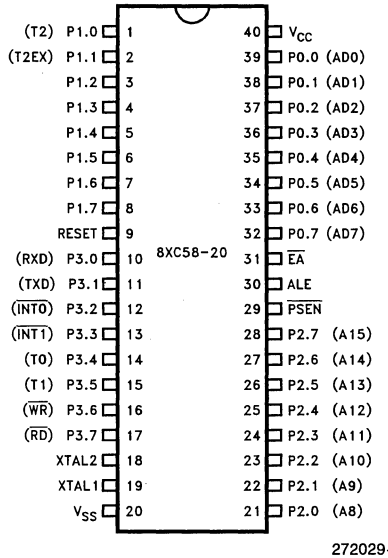
Figure 1. 8XC58-20 Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.

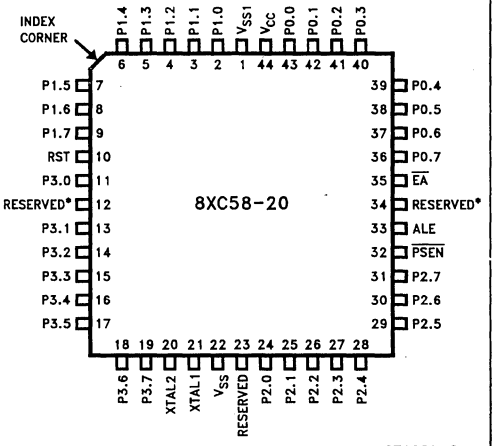
PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC58-20	P	40-Pin Plastic DIP	45°C/W	16°C/W
87C58-20	D	40-Pin CERDIP	45°C/W	15°C/W
8XC58-20	N	44-Pin PLCC	46°C/W	16°C/W
8XC58-20	S	44-Pin QFP	90°C/W	22°C/W



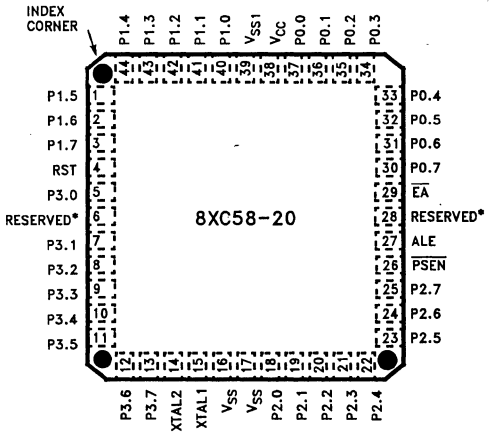
272029-2

DIP



272029-3

PLCC



272029-4

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin. Connect V_{SS} and V_{SS1} with the lowest impedance path possible.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC58-20:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a voltage above V_{IHI} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C58-20.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX instruction. Otherwise, the pin is weakly pulled high.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC58-20 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

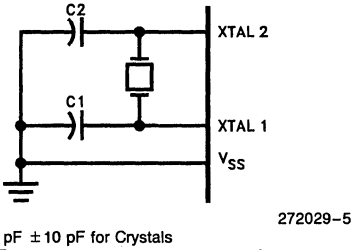
This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators contact resonator manufacturer.

Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but the minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

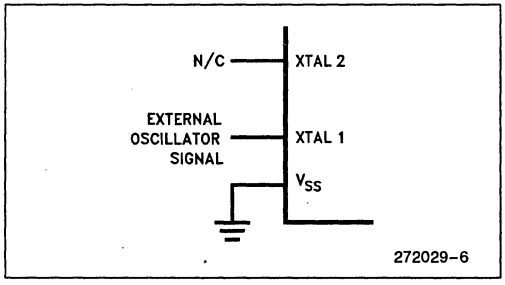


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC58-20 either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level. The external interrupt or reset signal must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

TIMER 2 PROGRAMMABLE CLOCK OUT

The 8XC58-20 has a new Timer 2 feature. A 50% duty cycle clock can be programmed to come out on P1.0. The output frequency ranges from 61 Hz to 4 MHz depending on the oscillator frequency and the reload value of the Timer 2 capture registers (RCAP2H, RCAP2L) as shown in the equation below:

$$\text{*Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared, and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) starts and stops the timer.

For a complete description of all Timer 2 functions, please reference the 8XC52/54/58 Hardware Description of the 8-Bit Embedded Controllers Handbook.

***NOTE:**
Even though the equation permits a maximum clock-out frequency of 5 MHz using a 20 MHz oscillator, the maximum device output frequency is 4 MHz. When using a 20 MHz oscillator, RCAP2L must be limited to a maximum value of FEH.

DESIGN CONSIDERATION

- When running out of internal program/data memory, the 87C58-3/80C58-3 can be operated using a 24 MHz clock. If the 87C58-3/80C58-3 is running out of external program/data memory, the operating frequency must be between 3.5 MHz to 20 MHz. The 87C58-3/80C58-3 will not function properly at 24 MHz when running out of external program/data memory.
- The window on the 87C58-20 must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC54-20 without the 8XC58-20 having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{\text{PSEN}}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{\text{PSEN}}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC58-20 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins During Idle and Power Down

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Express	 0 −40	 +70 +85	 °C °C
V_{CC}	Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency	3.5	20	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage(5) (Ports 1, 2, and 3)			0.3	V	I_{OL} = 100 μA(1)
				0.45	V	I_{OL} = 1.6 mA(1)
				1.0	V	I_{OL} = 3.5 mA(1)
V_{OL1}	Output Low Voltage(5) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA(1)
				0.45	V	I_{OL} = 3.2 mA(1)
				1.0	V	I_{OL} = 7.0 mA(1)
V_{OH}	Output High Voltage (Ports 1, 2, and 3, ALE, $\overline{PSEN}$)	V_{CC}−0.3			V	I_{OH} = −10 μA
		V_{CC}−0.7			V	I_{OH} = −30 μA
		V_{CC}−1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC}−0.3			V	I_{OH} = −200 μA
		V_{CC}−0.7			V	I_{OH} = −3.2 mA
		V_{CC}−1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}

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DC CHARACTERISTICS (Over Operating Conditions) (Continued)

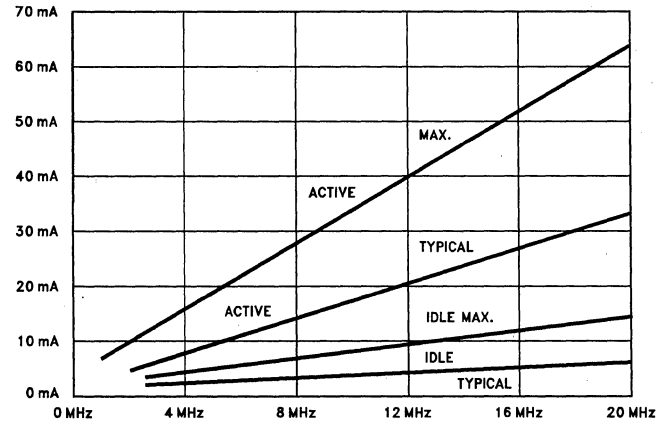
All parameters values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(4)	Max	Unit	Test Conditions
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3) Commercial Express			 −650 −750	 μA μA	 V_{IN} = 2V
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Running at 12 MHz (Figure 5) Idle Mode at 12 MHz (Figure 5) Power Down Mode		 20 5 15	 40 10 100	 mA mA μA	(Note 3)

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 5. I_{CC} vs Frequency

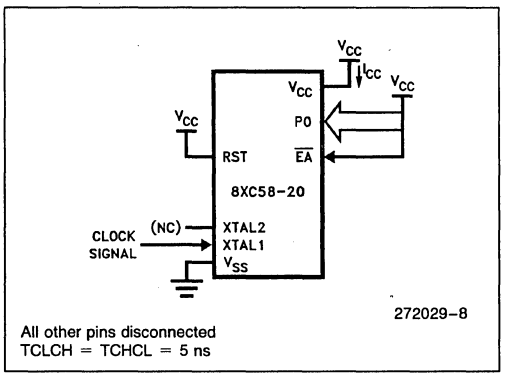


Figure 6. I_{CC} Test Condition, Active Mode

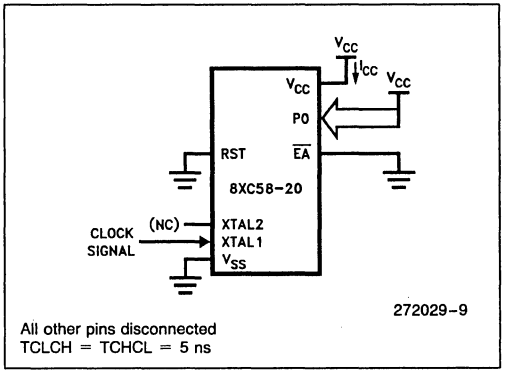


Figure 7. I_{CC} Test Condition Idle Mode

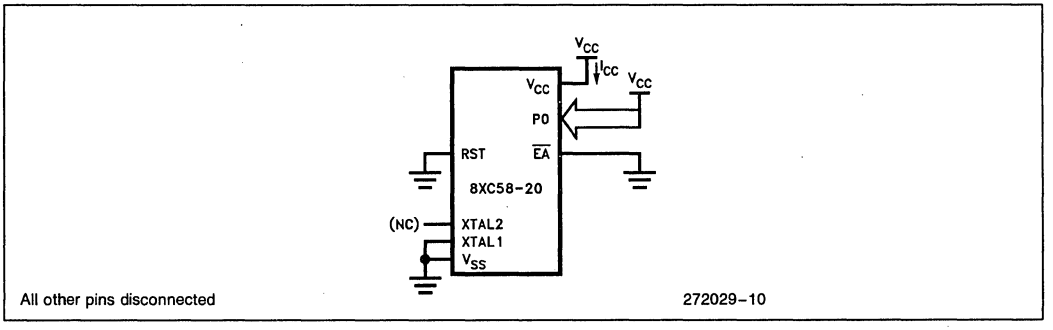


Figure 8. I_{CC} Test Condition, Power Down Mode
V_{CC} = 2.0V to 6.0V

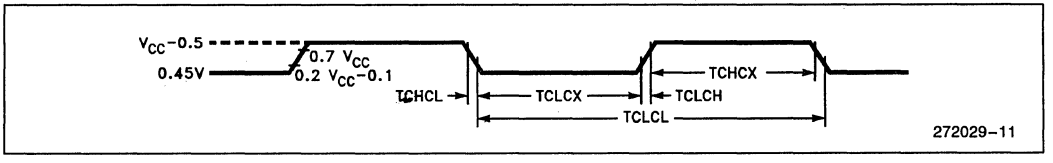


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
TCLCH = TCHCL = 5 ns

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

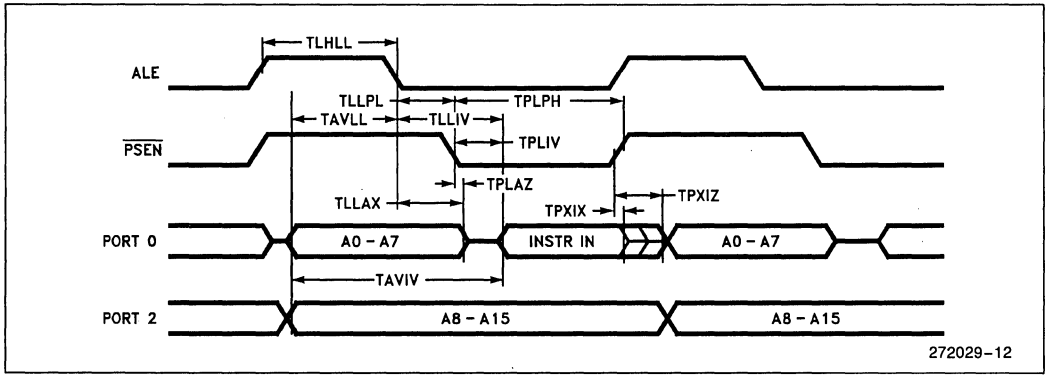
TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

AC CHARACTERISTICS (Over Operating Conditions.) Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

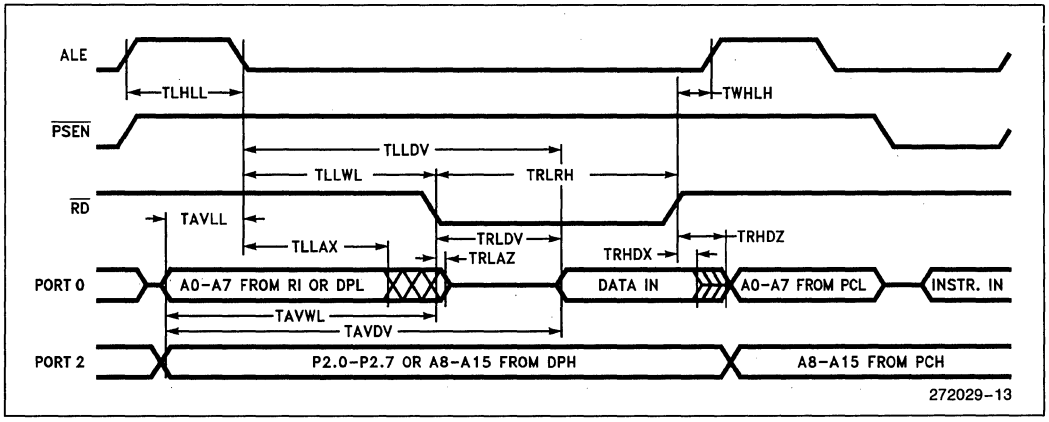
EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	20	MHz
TLHLL	ALE Pulse Width	60		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	10		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	20		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		125		4TCLCL−75	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	20		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	105		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		60		3TCLCL−90	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		30		TCLCL−20	ns
TAVIV	Address to Valid Instruction In		145		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	200		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	200		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		155		5TCLCL−95	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		40		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		310		8TCLCL−90	ns
TAVDV	Address to Valid Data In		360		9TCLCL−90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	100	200	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	110		4TCLCL−90		ns
TQVWX	Data Valid before $\overline{WR}$	15		TCLCL−35		ns
TWHQX	Data Hold after $\overline{WR}$	10		TCLCL−40		ns
TQVWH	Data Valid to $\overline{WR}$ High	280		7TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	10	90	TCLCL−40	TCLCL+40	ns

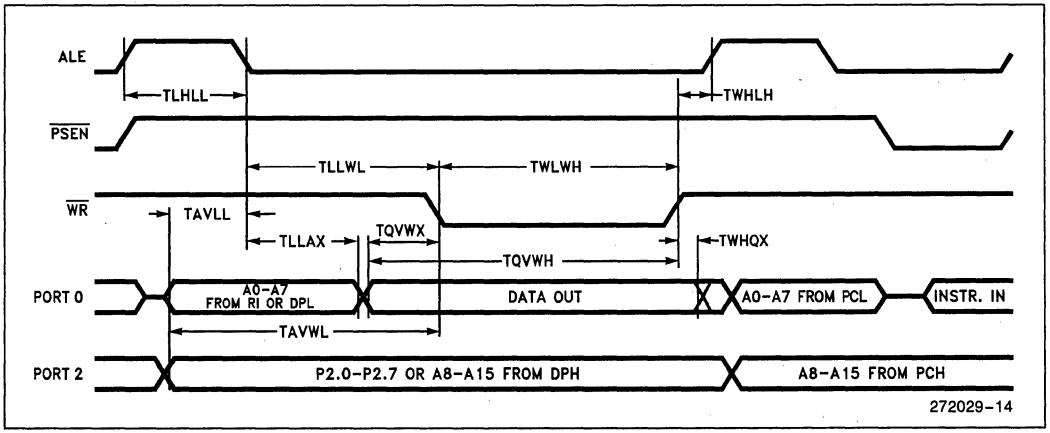
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE



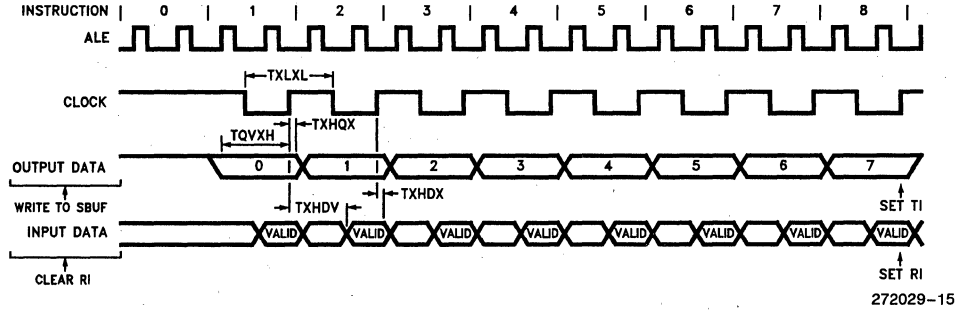
7

SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions T_A = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V; Load Capacitance = 80 pF

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	600		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	367		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		367		10TCLCL−133	ns

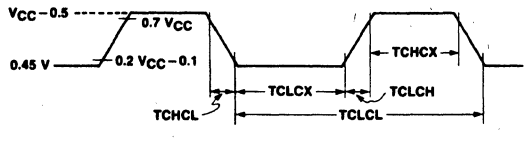
SHIFT REGISTER MODE TIMING WAVEFORMS



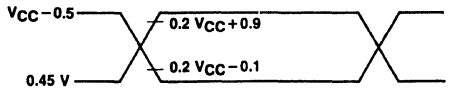
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



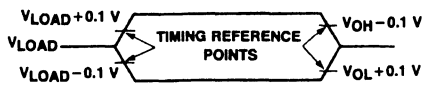
AC TESTING INPUT, OUTPUT WAVEFORMS



272029-17

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



272029-18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4 respectively for A0–A14.

DATA LINES: P0.0–P0.7 for D0–D7.

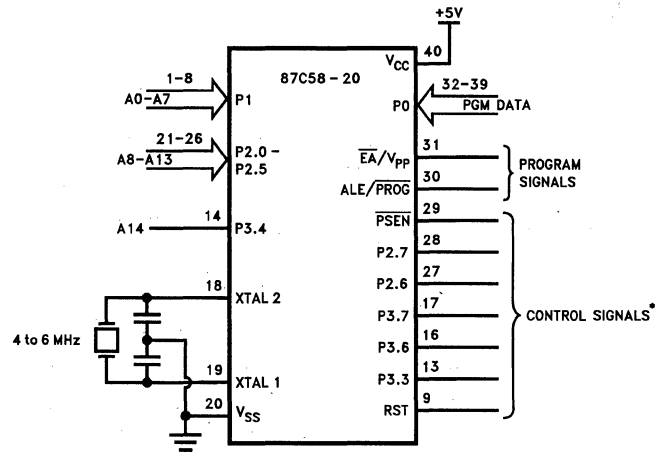
CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

7



*See Table 2 for proper input on these pins

Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C58-20 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes that is programmed. A complete verify of the array will ensure reliable programming of the 87C58-20.

The lock bits cannot be directly verified. They are verified by observing that their features are enabled. Refer to the EPROM Program Lock section in this data sheet.

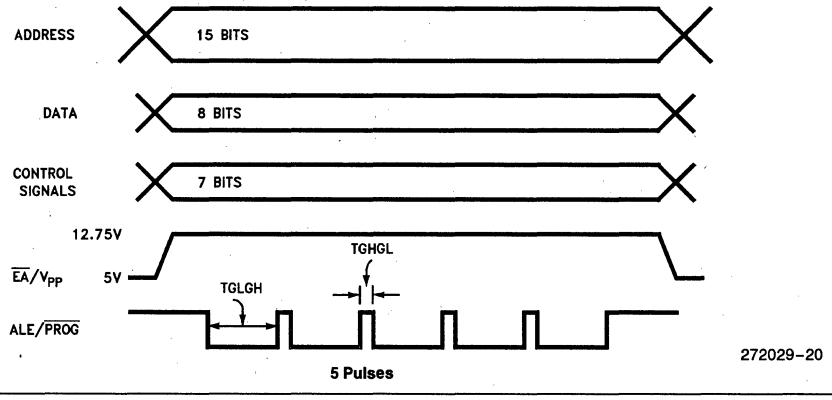


Figure 11. Programming Signal's Waveforms

ROM and EPROM Lock System

The 87C58-20 and the 80C58-20 program lock systems, when programmed, protect the onboard program against software piracy.

The 80C58-20 has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 3. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C58-20 has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user programmable. See Table 3.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in it's original, unmodified form. For programming the Encryption Array, refer to Table 2 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value of 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C58-20 has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 8XC58-20 has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Content	
	87C58-20	80C58-20
30H	89H	89H
31H	58H	58H
60H	58H	58H/18H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

Table 3. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

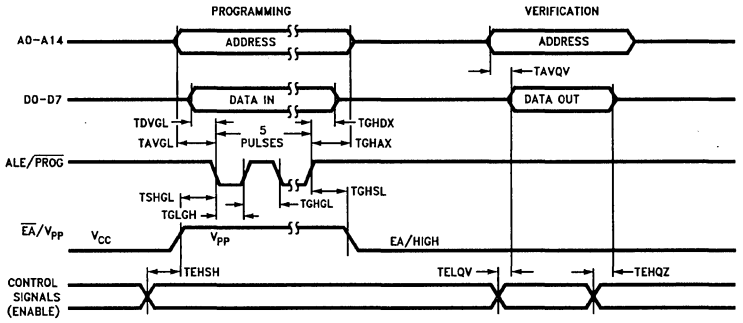
Any other combination of the lock bits is not defined.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



272029-21

DATA SHEET REVISION SUMMARY

The following differences exist between this data sheet (272029-002) and the previous version (272029-001):

1. Added 87C58-3/80C58-3 to 20 MHz data sheet.
2. Added EXPRESS version of 8XC58-20/-3 to 20 MHz data sheet.
3. θ_{ja} and θ_{jc} information added to Packages table.
4. References to second functions of Port 1.2 thru Port 1.7 pins have been removed.
5. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	120	125
	4TCLCL − 80	4TCLCL − 75
TPLIV	3TCLCL − 95	3TCLCL − 90
TWHQX	0	10
	TCLCL − 50	TCLCL − 40
TQVWH	200	280
	7TCLCL − 150	7TCLCL − 70

The following differences exist between version -001 of the 87C58-20/80C58-20 data sheet and the 87C58/80C58 (270900-001) data sheet:

1. QFP package added.
2. Timer 2 Programmable Clock Out paragraph added.
3. 20 MHz extension added to Figure 5.
4. 12 MHz Oscillator timings changed to 20 MHz Oscillator timings in External Program Memory Characteristics and Serial Port Timing tables.
5. Variable Oscillator equations in External Program Memory Characteristics Table changed as follows:

	From	To
TLLIV	4TCLCL − 100	4TCLCL − 80
TPLIV	3TCLCL − 105	3TCLCL − 95
TPXIZ	TCLCL − 25	TCLCL − 20
TRLDV	5TCLCL − 165	5TCLCL − 95
TLLDV	8TCLCL − 150	8TCLCL − 90
TAVDV	9TCLCL − 165	9TCLCL − 90
TAVWL	4TCLCL − 130	4TCLCL − 90
TQVWX	TCLCL − 50	TCLCL − 35

6. TXHQX in the Serial Port Timing Table changed from (2TCLCL − 117) to (2TCLCL − 50).
7. RRST Specification in DC Characteristics table changed from 40 KΩ min, 225 KΩ max to 50 KΩ min, 300 KΩ max.

8XC51FX Hardware Description and Data Sheets

8

intel®

September 1991

8XC51FX
Hardware Description

8

Order Number: 270653-004

HARDWARE DESCRIPTION OF THE 8XC51FX

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1.0 INTRODUCTION

The 8XC51FX is a highly integrated 8-bit microcontroller based on the MCS-51 architecture. As a member of the MCS-51 family, the 8XC51FX is optimized for control applications. Its key feature is the programmable counter array (PCA) which is capable of measuring and generating pulse information on five I/O pins. Also included are an enhanced serial port for multi-processor communications, an up/down timer/counter, and a program lock scheme for the on-chip program memory. Since the 8XC51FX products are CHMOS, they have two software selectable reduced power modes: Idle Mode and Power Down Mode.

The 8XC51FX uses the standard 8051 instruction set and is pin-for-pin compatible with the existing MCS-51 family of products.

This document presents a comprehensive description of the on-chip hardware features of the 8XC51FX. It begins with a discussion of the on-chip memory and then discusses each of the peripherals listed below.

Please note that 8XC51FX does not include the 80C51FA and 83C51FA. Therefore, these devices do not have some of the features found on the 8XC51FX. These features are: programmable clock out, four level interrupt priority structure, enhanced program lock scheme and asynchronous port reset.

- Four 8-Bit Bidirectional Parallel Ports
- Three 16-Bit Timer/Counters with
  - One Up/Down Timer/Counter
  - Clock Out
- Programmable Counter Array with
  - Compare/Capture
  - Software Timer
  - High Speed Output
  - Pulse Width Modulator
  - Watchdog Timer
- Full-Duplex Programmable Serial Port with
  - Framing Error Detection
  - Automatic Address Recognition
- Interrupt Structure with
  - Seven Interrupt Sources
  - Four Priority Levels
- Power-Saving Modes
  - Idle Mode
  - Power Down Mode

Table 1 summarizes the product names and memory differences of the various 8XC51FX products currently available. Throughout this document, the products will generally be referred to as the C51FX.

Table 1. C51FX Family of Microcontrollers

ROM Device	EPROM Version	ROMless Version	ROM/ EPROM Bytes	RAM Bytes
83C51FA	87C51FA	80C51FA	8K	256
83C51FB	87C51FB	80C51FA	16K	256
83C51FC	87C51FC	80C51FA	32K	256

2.0 MEMORY ORGANIZATION

All MCS-51 devices have a separate address space for Program and Data Memory. Up to 64 Kbytes each of external Program and Data Memory can be addressed.

2.1 Program Memory

If the $\overline{EA}$ pin is connected to V_{SS}, all program fetches are directed to external memory. On the 83C51FA (or 87C51FA), if the $\overline{EA}$ pin is connected to V_{CC}, then program fetches to addresses 0000H through 1FFFH are directed to internal ROM and fetches to addresses 2000H through FFFFH are to external memory.

On the 83C51FB (or 87C51FB) if $\overline{EA}$ is connected to VCC, program fetches to addresses 0000H through 3FFFH are directed to internal ROM, and fetches to addresses 4000H through FFFFH are to external memory.

On the 83C51FC (or 87C51FC) if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 7FFFH are directed to internal ROM or EPROM and fetches to addresses 8000H through FFFFH are to external memory.

2.2 Data Memory

The C51FX implements 256 bytes of on-chip data RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. That means they have the same addresses, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example:

MOV 0A0H, #data

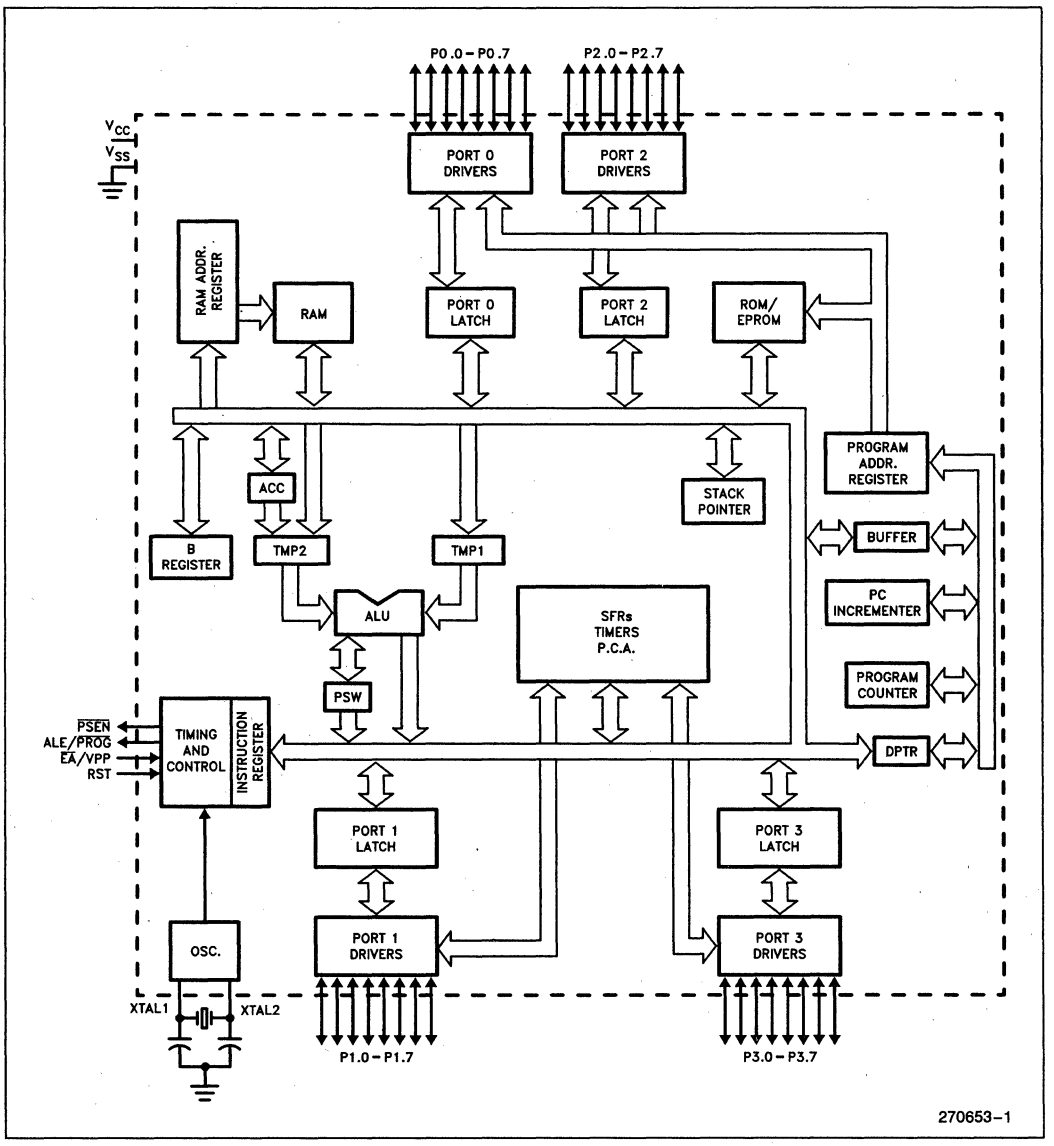


Figure 1. 8XC51FX Functional Block Diagram

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the upper 128 bytes of data RAM. For example:

MOV @R0, #data

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H). Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

3.0 SPECIAL FUNCTION REGISTERS

A map of the on-chip memory area called the SFR (Special Function Register) space is shown in Table 2.

Note that not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have no effect.

User software should not write 1s to these unimplemented locations, since they may be used in future MCS-51 products to invoke new features. In that case the reset or inactive values of the new bits will always be 0, and their active values will be 1.

The functions of the SFRs are outlined below. More information on the use of specific SFRs for each peripheral is included in the description of that peripheral.

Accumulator: ACC is the Accumulator register. The mnemonics for Accumulator-Specific instructions, however, refer to the Accumulator simply as A.

Table 2. SFR Mapping and Reset Values

F8		CH 00000000	CCAP0H XXXXXXXX	CCAP1H XXXXXXXX	CCAP2H XXXXXXXX	CCAP3H XXXXXXXX	CCAP4H XXXXXXXX		FF
F0	* B 00000000								F7
E8		CL 00000000	CCAP0L XXXXXXXX	CCAP1L XXXXXXXX	CCAP2L XXXXXXXX	CCAP3L XXXXXXXX	CCAP4L XXXXXXXX		EF
E0	* ACC 00000000								E7
D8	CCON 00X00000	CMOD 00XXX000	CCAPM0 X0000000	CCAPM1 X0000000	CCAPM2 X0000000	CCAPM3 X0000000	CCAPM4 X0000000		DF
D0	* PSW 00000000								D7
C8	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0									C7
B8	* IP X0000000	SADEN 00000000							BF
B0	* P3 11111111							IPH X0000000	B7
A8	* IE 00000000	SADDR 00000000							AF
A0	* P2 11111111								A7
98	* SCON 00000000	* SBUF XXXXXXXX							9F
90	* P1 11111111								97
88	* TCON 00000000	* TMOD 00000000	* TL0 00000000	* TL1 00000000	* TH0 00000000	* TH1 00000000			8F
80	* P0 11111111	* SP 00000111	* DPL 00000000	* DPH 00000000				* PCON ** 00XX0000	87

* = Found in the 8051 core (See 8051 Hardware Description for explanations of these SFRs).
** = See description of PCON SFR. Bit PCON.4 is not affected by reset.
X = Undefined.

Table 3. PSW: Program Status Word Register

PSW Address = 0D0H Reset Value = 0000 0000B

Bit Addressable

	CY	AC	F0	RS1	RS0	OV	—	P
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CY	Carry flag.
AC	Auxiliary Carry flag. (For BCD Operations)
F0	Flag 0. (Available to the user for general purposes).
RS1	Register bank select bit 1.
RS0	Register bank select bit 0.

RS1	RS0	Working Register Bank and Address	
0	0	Bank 0	(00H–07H)
0	1	Bank 1	(08H–0FH)
1	0	Bank 2	(10H–17H)
1	1	Bank 3	(18H–1FH)

OV	Overflow flag.
—	User definable flag.
P	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the Accumulator, i.e., even parity.

B Register: The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer: The Stack Pointer Register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. The stack may reside anywhere in on-chip RAM. On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Data Pointer: The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

Program Status Word: The PSW register contains program status information as detailed in Table 3.

Ports 0 to 3 Registers: P0, P1, P2, and P3 are the SFR latches of Port 0, Port 1, Port 2, and Port 3 respectively.

Timer Registers: Register pairs (TH0, TL0), (TH1, TL1), and (TH2, TL2) are the 16-bit count registers for Timer/Counters 0, 1, and 2 respectively. Control and status bits are contained in registers TCON and TMOD for Timers 0 and 1 and in registers T2CON and T2MOD for Timer 2. The register pair (RCAP2H, RCAP2L) are the capture/reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Programmable Counter Array (PCA) Registers: The 16-bit PCA timer/counter consists of registers CH and CL. Registers CCON and CMOD contain the control and status bits for the PCA. The CCAPMn (n = 0, 1, 2, 3, or 4) registers control the mode for each of the five PCA modules. The register pairs (CCAPnH, CCAPnL) are the 16-bit compare/capture registers for each PCA module.

Serial Port Registers: The Serial Data Buffer, SBUF, is actually two separate registers: a transmit buffer and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer where it is held for serial transmission. (Moving a byte to SBUF initiates the transmission). When data is moved from SBUF, it comes from the receive buffer. Register SCON contains the control and status bits for the Serial Port. Registers SADDR and SADEN are used to define the Given and the Broadcast addresses for the Automatic Address Recognition feature.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the 7 interrupts in the IP register.

Power Control Register: PCON controls the Power Reduction Modes. Idle and Power Down Modes.

4.0 PORT STRUCTURES AND OPERATION

All four ports in the C51FX are bidirectional. Each consists of a latch (Special Function Registers P0 through P3), an output driver, and an input buffer.

The output drivers of Ports 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise the Port 2 pins continue to emit the P2 SFR content.

All the Port 1 and Port 3 pins are multifunctional. They are not only port pins, but also serve the functions of various special features as listed in Table 4.

The alternate functions can only be activated if the corresponding bit latch in the port SFR contains a 1. Otherwise the port pin is stuck at 0.

4.1 I/O Configurations

Figure 2 shows a functional diagram of a typical bit latch and I/O buffer in each of the four ports. The bit latch (one bit in the port's SFR) is represented as a Type D flip-flop, which clocks in a value from the internal bus in response to a "write to latch" signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a "read latch" signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a "read pin" signal from the CPU. Some instructions that read a port activate the "read latch" signal, and others activate the "read pin" signal. See the Read-Modify-Write Feature section.

As shown in Figure 2, the output drivers of Ports 0 and 2 are switchable to an internal ADDRESS and ADDRESS/DATA bus by an internal CONTROL signal for use in external memory accesses. During external memory accesses, the P2 SFR remains unchanged, but the P0 SFR gets 1s written to it.

Table 4. Alternate Port Functions

Port Pin	Alternate Function
P0.0/AD0–P0.7/AD7	Multiplexed Byte of Address/Data for External Memory
P1.0/T2	Timer 2 External Clock Input/Clock-Out
P1.1/T2EX	Timer 2 Reload/Capture/Direction Control
P1.2/ECI	PCA External Clock Input
P1.3/CEX0	PCA Module 0 Capture Input, Compare/PWM Output
P1.4/CEX1	PCA Module 1 Capture Input, Compare/PWM Output
P1.5/CEX2	PCA Module 2 Capture Input, Compare/PWM Output
P1.6/CEX3	PCA Module 3 Capture Input, Compare/PWM Output
P1.7/CEX4	PCA Module 4 Capture Input, Compare/PWM Output
P2.0/A8–P2.7/A15	High Byte of Address for External Memory
P3.0/RXD	Serial Port Input
P3.1/TXD	Serial Port Output
P3.2/$\overline{\text{INT0}}$	External Interrupt 0
P3.3/$\overline{\text{INT}}$	External Interrupt 1
P3.4/T0	Timer 0 External Clock Input
P3.5/T1	Timer 1 External Clock Input
P3.6/$\overline{\text{WR}}$	Write Strobe for External Memory
P3.7/$\overline{\text{RD}}$	Read Strobe for External Memory

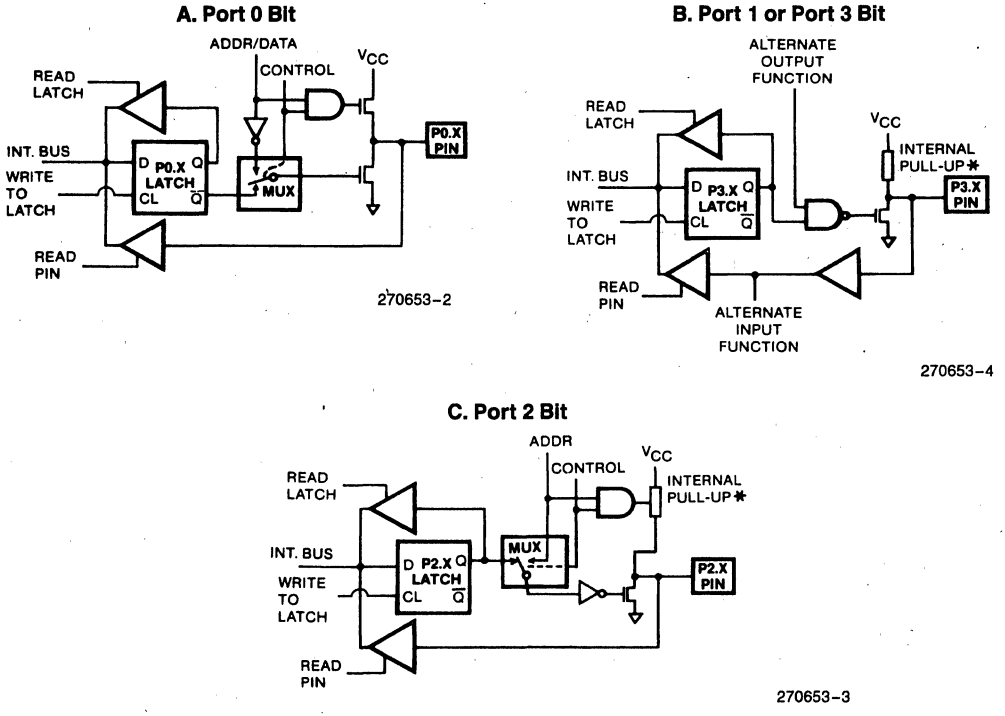


Figure 2. C51FX Port Bit Latches and I/O Buffers

Also shown in Figure 2 is that if a P1 or P3 latch contains a 1, then the output level is controlled by the signal labeled "alternate output function." The actual pin level is always available to the pin's alternate input function, if any.

Ports 1, 2, and 3 have internal pullups. Port 0 has open drain outputs. Each I/O line can be independently used as an input or an output (Ports 0 and 2 may not be used as general purpose I/O when being used as the ADDRESS/DATA BUS). To be used as an input, the port bit latch must contain a 1, which turns off the output driver FET. On Ports 1, 2, and 3, the pin is pulled high by the internal pullup, but can be pulled low by an external source.

Port 0 differs from the other ports in not having internal pullups. The pullup FET in the P0 output driver (see Figure 2) is used only when the Port is emitting 1s during external memory accesses. Otherwise the pullup FET is off. Consequently P0 lines that are being used as output port lines are open drain. Writing a 1 to the bit latch leaves both output FETs off, which floats the pin and allows it to be used as a high-impedance input. Because Ports 1 through 3 have fixed internal pullups they are sometimes call "quasi-bidirectional" ports. When configured as inputs they pull high and will source current (IIL in the data sheets) when externally pulled low. Port 0, on the other hand, is considered "true" bidirectional, because it floats when configured as an input.

All the port latches have 1s written to them by the reset function. If a 0 is subsequently written to a port latch, it can be reconfigured as an input by writing a 1 to it.

4.2 Writing to a Port

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during State 6 Phase 2 of the final cycle of the instruction. However, port latches are in fact sampled by their output buffers only during Phase 1 of any clock period. (During Phase 2 the output buffer holds the value it saw during the previous Phase 1). Consequently, the new value in the port latch won't actually appear at the output pin until the next Phase 1, which will be at S1P1 of the next machine cycle. Refer to Figure 3. For more information on internal timings refer to the CPU Timing section.

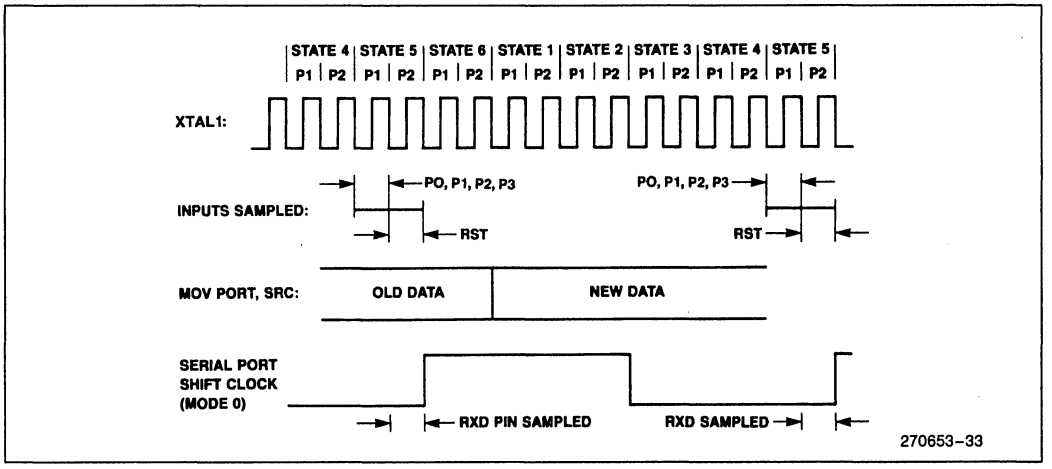


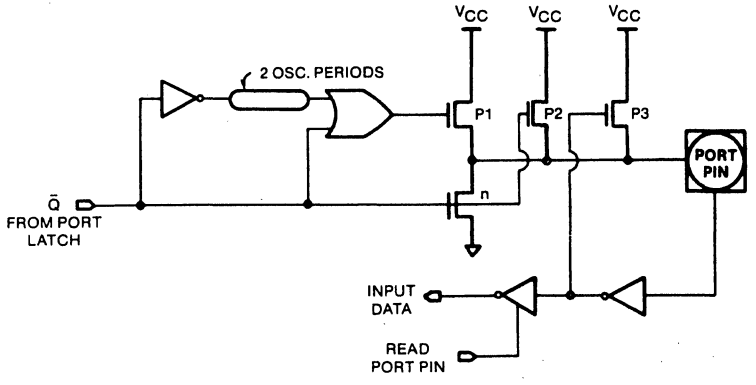
Figure 3. Port Operation

If the change requires a 0-to-1 transition in Ports 1, 2, and 3, an additional pullup is turned on during S1P1 and S1P2 of the cycle in which the transition occurs. This is done to increase the transition speed. The extra pullup can source about 100 times the current that the normal pullup can. The internal pullups are field-effect transistors, not linear resistors. The pull-up arrangements are shown in Figure 4.

The pullup consists of three pFETs. Note that an n-channel FET (nFET) is turned on when a logical 1 is applied to its gate, and is turned off when a logical 0 is applied to its gate. A p-channel FET (pFET) is the opposite: it is on when its gate sees a 0, and off when its gate sees a 1.

pFET 1 in is the transistor that is turned on for 2 oscillator periods after a 0-to-1 transition in the port latch. A 1 at the port pin turns on pFET3 (a weak pull-up), through the invertor. This invertor and pFET form a latch which hold the 1.

If the pin is emitting a 1, a negative glitch on the pin from some external source can turn off pFET3, causing the pin to go into a float state. pFET2 is a very weak pullup which is on whenever the nFET is off, in traditional CMOS style. It's only about $1/10$ the strength of pFET3. Its function is to restore a 1 to the pin in the event the pin had a 1 and lost it to a glitch.



CHMOS Configuration. pFET 1 is turned on for 2 osc. periods after $\overline{Q}$ makes a 0-to-1 transition. During this time, pFET 1 also turns on pFET 3 through the inverter to form a latch which holds the 1. pFET 2 is also on. Port 2 is similar except that it holds the strong pullup on while emitting 1s that are address bits. (See text, "Accessing External Memory".)

Figure 4. Ports 1 and 3 Internal Pullup Configurations

4.3 Port Loading and Interfacing

The output buffers of Ports 1, 2, and 3 can each sink 1.6 mA at 0.45 V. These port pins can be driven by open-collector and open-drain outputs although 0-to-1 transitions will not be fast since there is little current pulling the pin up. An input 0 turns off pullup pFET3, leaving only the very weak pullup pFET2 to drive the transition.

In external bus mode, Port 0 output buffers can each sink 3.2 mA at 0.45 V. However, as port pins they require external pullups to be able to drive any inputs.

See the latest revision of the data sheet for design-in information.

4.4 Read-Modify-Write Feature

Some instructions that read a port read the latch and others read the pin. Which ones do which? The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called "read-modify-write" instructions. Listed below are the read-modify-write instructions. When the destination operand is a port, or a port bit, these instructions read the latch rather than the pin:

ANL	(logical AND, e.g., ANL P1, A)
ORL	(logical OR, e.g., ORL P2, A)
XRL	(logical EX-OR, e.g., XRL P3, A)
JBC	(jump if bit = 1 and clear bit, e.g., JBC P1.1, LABEL)
CPL	(complement bit, e.g., CPL P3.0)
INC	(increment, e.g., INC P2)
DEC	(decrement, e.g., DEC P2)
DJNZ	(decrement and jump if not zero, e.g., DJNZ P3, LABEL)
MOV, PX.Y, C	(move carry bit to bit Y of Port X)
CLR PX.Y	(clear bit Y of Port X)
SETB PX.Y	(set bit Y of Port X)

It is not obvious that the last three instructions in this list are read-modify-write instructions, but they are. They read the port byte, all 8 bits, modify the addressed bit, then write the new byte back to the latch.

The reason that read-modify-write instructions are directed to the latch rather than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. When a 1 is written to the bit, the transistor is turned on. If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1.

4.5 Accessing External Memory

Accesses to external memory are of two types: accesses to external Program Memory and accesses to external Data Memory. Accesses to external Program Memory use signal $\overline{PSEN}$ (program store enable) as the read strobe. Accesses to external Data Memory use $\overline{RD}$ or $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory. Refer to Figures 5 through 7.

Fetches from external Program Memory always use a 16-bit address. Accesses to external Data Memory can use either a 16-bit address (MOVX @ DPTR) or an 8-bit address (MOVX @ Ri).

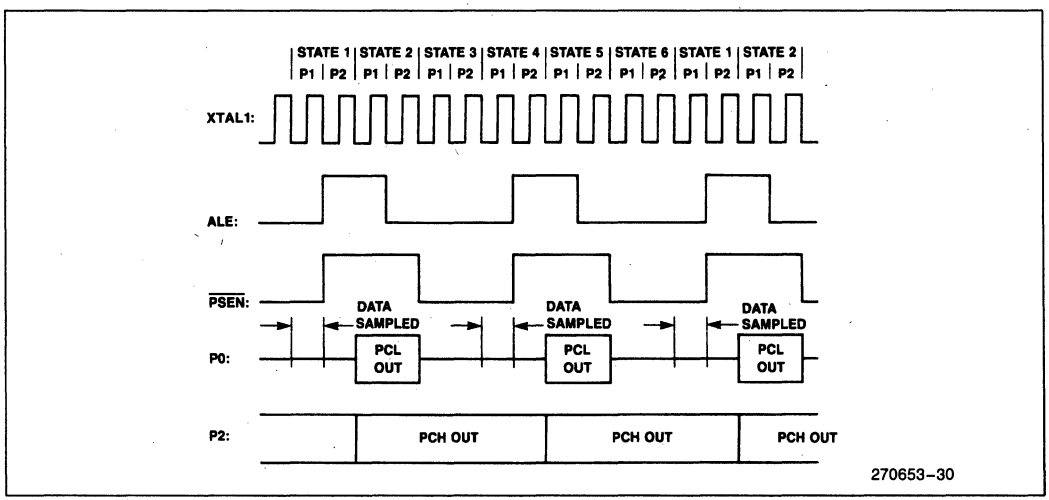


Figure 5. External Program Memory Fetches

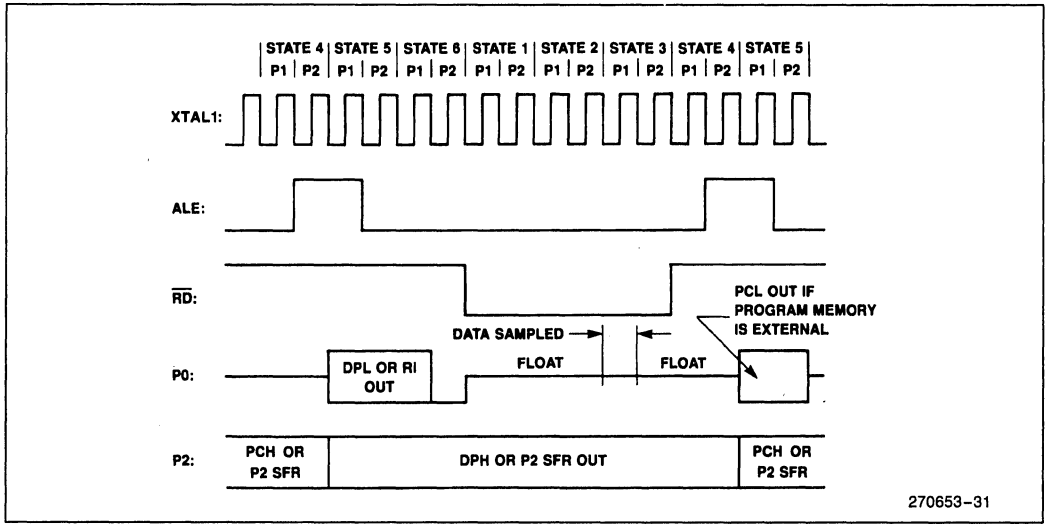


Figure 6. External Data Memory Read Cycle

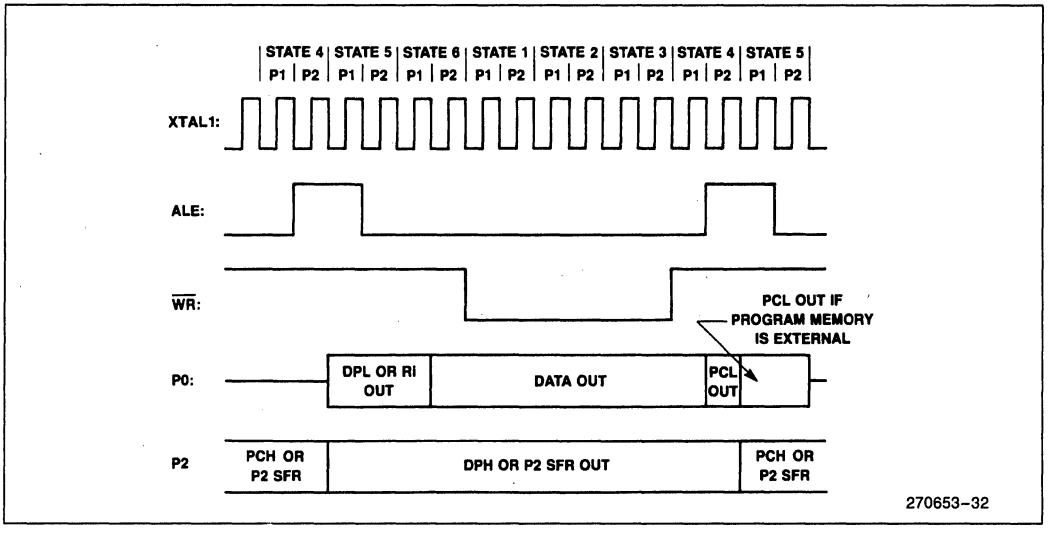


Figure 7. External Data Memory Write Cycle

8

Whenever a 16-bit address is used, the high byte of the address comes out on Port 2, where it is held for the duration of the read or write cycle. The Port 2 drivers use the strong pullups during the entire time that they are emitting address bits that are 1s. This occurs when the MOVX @ DPTR instruction is executed. During this time the Port 2 latch (the Special Function Register) does not have to contain 1s, and the contents of the Port 2 SFR are not modified. If the external memory cycle is not immediately followed by another external memory cycle, the undisturbed contents of the Port 2 SFR will reappear in the next cycle.

If an 8-bit address is being used (MOVX @ Ri), the contents of the Port 2 SFR remain at the Port 2 pins throughout the external memory cycle. In this case, Port 2 pins can be used to page the external data memory.

In either case, the low byte of the address is time-multiplexed with the data byte on Port 0. The ADDRESS/DATA signal drives both FETs in the Port 0 output buffers. Thus, in external bus mode the Port 0 pins are not open-drain outputs and do not require external pullups. The ALE (Address Latch Enable) signal should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe ($\overline{RD}$) is deactivated.

During any access to external memory, the CPU writes 0FFH to the Port 0 latch (the Special Function Register), thus obliterating the information in the Port 0 SFR. Also, a MOV P0 instruction must not take place during external memory accesses. If the user writes to Port 0 during an external memory fetch, the incoming code byte is corrupted. Therefore, do not write to Port 0 if external program memory is used.

External Program Memory is accessed under two conditions:

1. Whenever signal $\overline{EA}$ is active, or
2. Whenever the program counter (PC) contains an address greater than 1FFFH (8K) for the 8XC51FA or 3FFFH (16K) for the 8XC51FB, or 7FFFH (32K) for the 87C51FC.

This requires that the ROMless versions have $\overline{EA}$ wired to V_{SS} enable the lower 8K, 16K, or 32K program bytes to be fetched from external memory.

When the CPU is executing out of external Program Memory, all 8 bits of Port 2 are dedicated to an output function and may not be used for general purpose I/O. During external program fetches they output the high byte of the PC with the Port 2 drivers using the strong pullups to emit bits that are 1s.

5.0 TIMERS/COUNTERS

The C51FX has three 16-bit Timer/Counters: Timer 0, Timer 1, and Timer 2. Each consists of two 8-bit registers, THx and TLx, (x = 0, 1, and 2). All three can be configured to operate either as timers or event counters.

In the Timer function, the TLx register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin—T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is $1/24$ of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

In addition to the Timer or Counter selection, Timer 0 and Timer 1 have four operating modes from which to select: Modes 0 – 3. Timer 2 has three modes of operation: Capture, Auto-Reload, and Baud Rate Generator.

5.1 Timer 0 and Timer 1

The Timer or Counter function is selected by control bits C/$\overline{T}$ in the Special Function Register TMOD (Table 5). These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timer/Counters. Mode 3 operation is different for the two timers.

MODE 0

Either Timer 0 or Timer 1 in Mode 0 is an 8-bit Counter with a divide-by-32 prescaler. Figure 8 shows the Mode 0 operation for either timer.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFx. The counted input is enabled to the Timer when TRx = 1 and either GATE = 0 or $\overline{INTx}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTx}$, to facilitate pulse width measurements). TRx and TFx are

control bits in SFR TCON (Table 6). The GATE bit is in TMOD. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

The 13-bit register consists of all 8 bits of THx and the lower 5 bits of TLx. The upper 3 bits of TLx are indeterminate and should be ignored. Setting the run flag (TRx) does not clear these registers.

MODE 1

Mode 1 is the same as Mode 0, except that the Timer register uses all 16 bits. Refer to Figure 9. In this mode, THx and TLx are cascaded; there is no prescaler.

MODE 2

Mode 2 configures the Timer register as an 8-bit Counter (TLx) with automatic reload, as shown in Figure 10. Overflow from TLx not only sets TFx, but also reloads TLx with the contents of THx, which is preset by software. The reload leaves THx unchanged.

Table 5. TMOD: Timer/Counter Mode Control Register

TMOD Address = 89H Reset Value = 0000 0000B

Not Bit Addressable

	TIMER 1				TIMER 0			
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
GATE	Gating control when set. Timer/Counter 0 or 1 is enabled only while $\overline{INT0}$ or $\overline{INT1}$ pin is high and TR0 or TR1 control pin is set. When cleared, Timer 0 or 1 is enabled whenever TR0 or TR1 control bit is set.
C/$\overline{T}$	Timer or Counter Selector. Clear for Timer operation (input from internal system clock). Set for Counter operation (input from T0 or T1 input pin).

M1	M0	Operating Mode
0	0	8-bit Timer/Counter. THx with TLx as 5-bit prescaler.
0	1	16-bit Timer/Counter. THx and TLx are cascaded; there is no prescaler.
1	0	8-bit auto-reload Timer/Counter. THx holds a value which is to be reloaded into TLx each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter stopped.

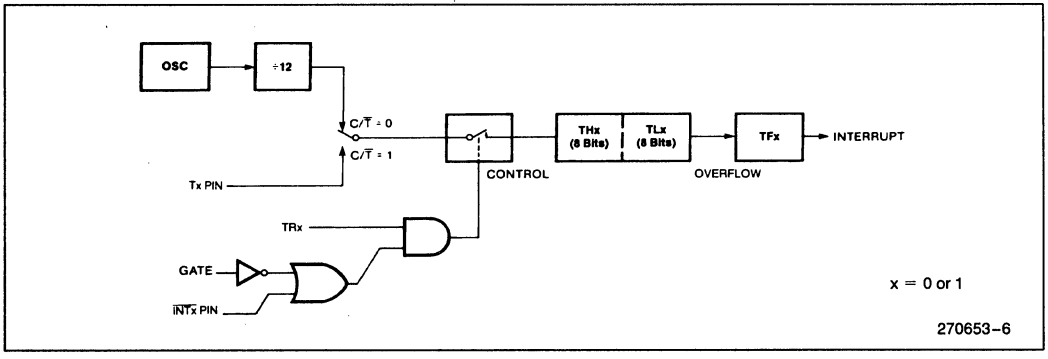


Figure 8. Timer/Counter 0 or 1 in Mode 0: 13-Bit Counter

Table 6. TCON: Timer/Counter Control Register

TCON Address = 88H Reset Value = 0000 0000B

Bit Addressable

	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF1	Timer 1 overflow Flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter 1 on/off.
TF0	Timer 0 overflow Flag. Set by hardware on Timer/Counter 0 overflow. Cleared by hardware when processor vectors to interrupt routine.
TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter 0 on/off.
IE1	Interrupt 1 flag. Set by hardware when external interrupt 1 edge is detected (transmitted or level-activated). Cleared when interrupt processed only if transition-activated.
IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt 1.
IE0	Interrupt 0 flag. Set by hardware when external interrupt 0 edge is detected (transmitted or level-activated). Cleared when interrupt processed only if transition-activated.
IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt 0.

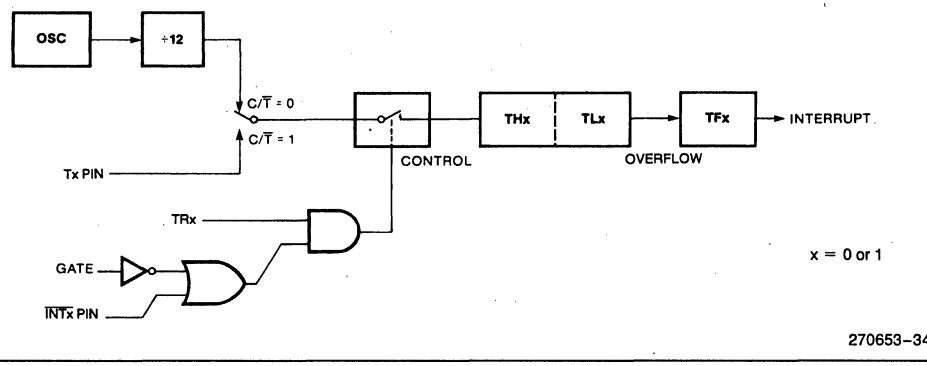


Figure 9. Timer/Counter 0 or 1 in Mode 1: 16-Bit Counter

MODE 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 11. TL0 uses the Timer 0 control bits: C/$\overline{T}$, GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus TH0 now controls the Timer 1 interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

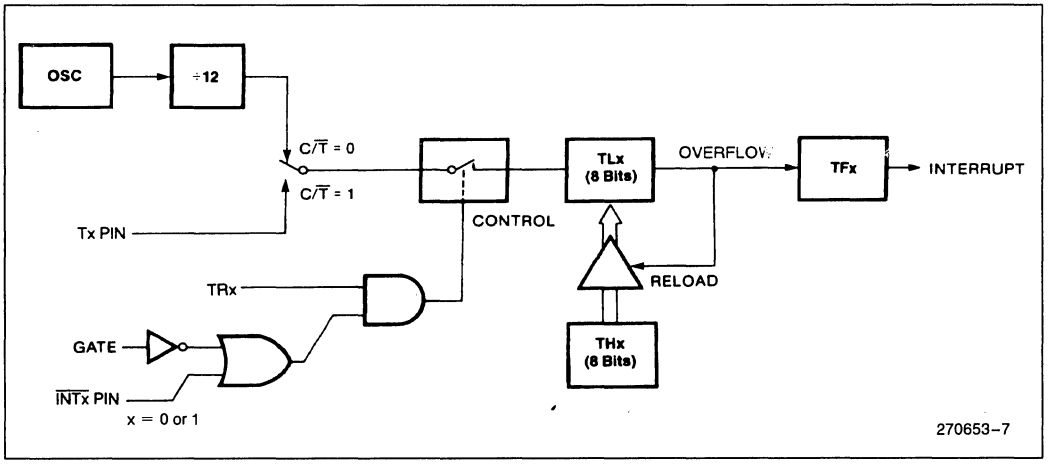


Figure 10. Timer/Counter 1 Mode 2: 8-Bit Auto-Reload

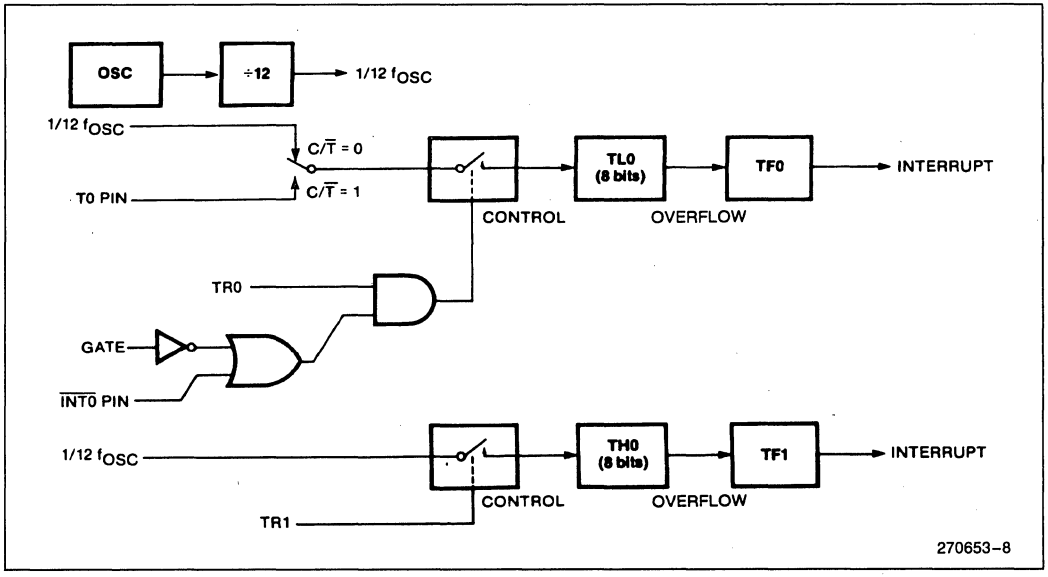


Figure 11. Timer/Counter 0 Mode 3: Two 8-Bit Counters

5.2 Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate either as a timer or as an event counter. This is selected by bit C/$\overline{T2}$ in the Special Function Register T2CON (Table 8). It has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON as shown in Table 7.

Table 7. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	T2*OE	TR2	Mode
0	0	0	1	16-Bit Auto-Reload
0	1	0	1	16-Bit Capture
1	X	X	1	Baud_Rate Generator
X	0	1	1	Clock-Out on P1.0
X	X	X	0	Timer Off

Table 8. T2CON: Timer/Counter 2 Control Register

T2CON Address = 0C8H Reset Value = 0000 0000B

Bit Addressable

	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12 or OSC/2 in baud rate generator mode). 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

CAPTURE MODE

In the capture mode there are two options selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 still does the above, but with the added feature that a 1-to-0 tran-

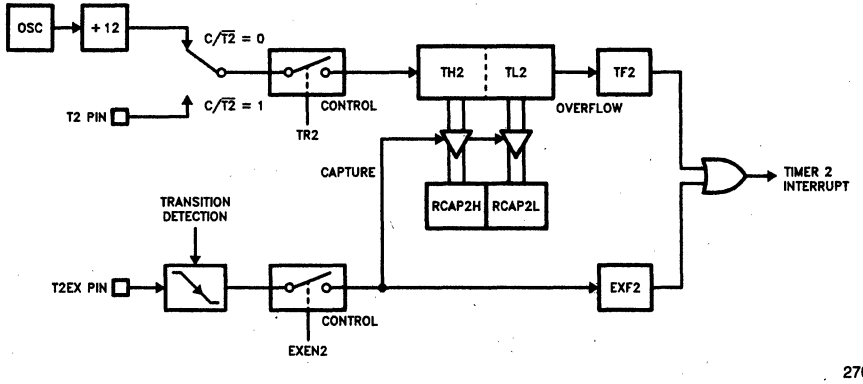


Figure 12. Timer 2 in Capture Mode

sition at external input T2EX causes the current value in the Timer 2 registers, TH2 and TL2, to be captured into registers RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 12.

AUTO-RELOAD MODE (UP OR DOWN COUNTER)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by a bit named DCEN (Down Counter Enable) located in the SFR T2MOD (see Table 9). Upon reset the DCEN bit is set to 0 so that Timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 13 shows Timer 2 automatically counting up when DCEN = 0. In this mode there are two options selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Either the TF2 or EXF2 bit can generate the Timer 2 interrupt if it is enabled.

Table 9. T2MOD: Timer 2 Mode Control Register

T2MOD Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

—	—	—	—	—	—	T2OE	DCEN
Bit 7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.*
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

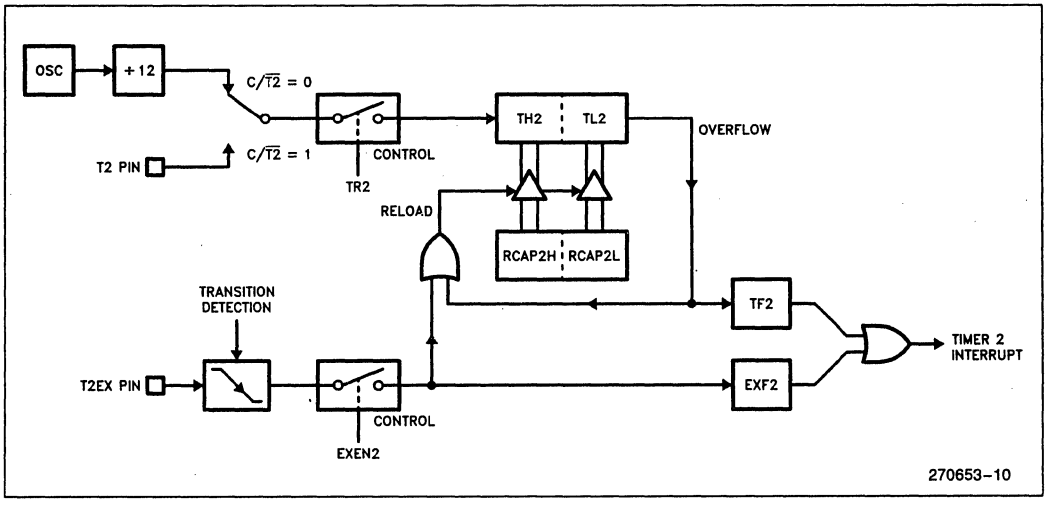


Figure 13. Timer 2 Auto Reload Mode (DCEN = 0)

Setting the DCEN bit enables Timer 2 to count up or down as shown in Figure 14. In this mode the T2EX pin controls the direction of count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit which can then generate an interrupt if it is enabled. This overflow also causes a the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. Now the timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows. This bit can be used as a 17th bit of resolution if desired. In this operating mode, EXF2 does not generate an interrupt.

BAUD RATE GENERATOR MODE

The baud rate generator mode is selected by setting the RCLK and/or TCLK bits in T2CON. Timer 2 in this mode will be described in conjunction with the serial port.

PROGRAMMABLE CLOCK OUT

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed (1) to input the external clock for Timer/Counter 2 or (2) to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer (see Table 6 for operating modes).

The Clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\text{Clock-out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and Clock-out frequencies cannot be determined independently of one another since they both use the values in RCAP2H and RCAP2L.

6.0 PROGRAMMABLE COUNTER ARRAY

The Programmable Counter Array (PCA) consists of a 16-bit timer/counter and five 16-bit compare/capture modules as shown in Figure 15a. The PCA timer/counter serves as a common time base for the five modules and is the only timer which can service the PCA. Its clock input can be programmed to count any one of the following signals:

- oscillator frequency ÷ 12
- oscillator frequency ÷ 4
- Timer 0 overflow
- external input on ECI (P1.2).

Each compare/capture module can be programmed in any one of the following modes:

- rising and/or falling edge capture
- software timer
- high speed output
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer.

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector (more about this in the PCA Interrupt section).

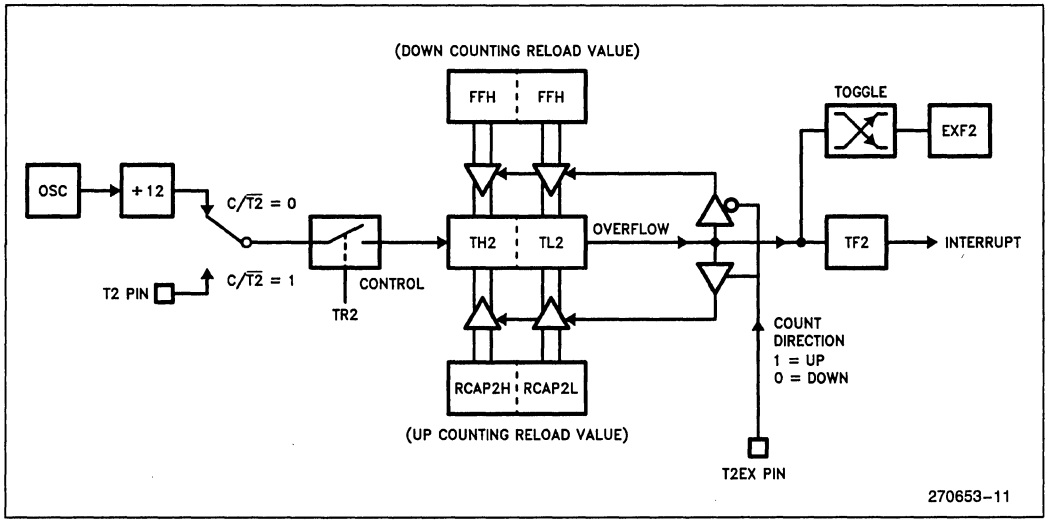


Figure 14. Timer 2 Auto Reload Mode (DCEN = 1)

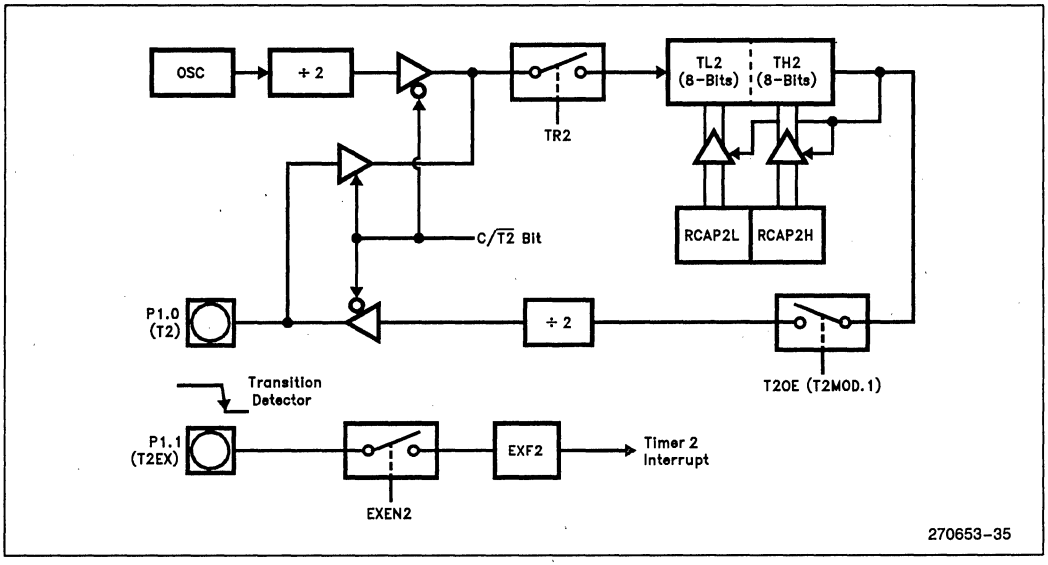


Figure 15. Timer 2 in Clock-Out Mode

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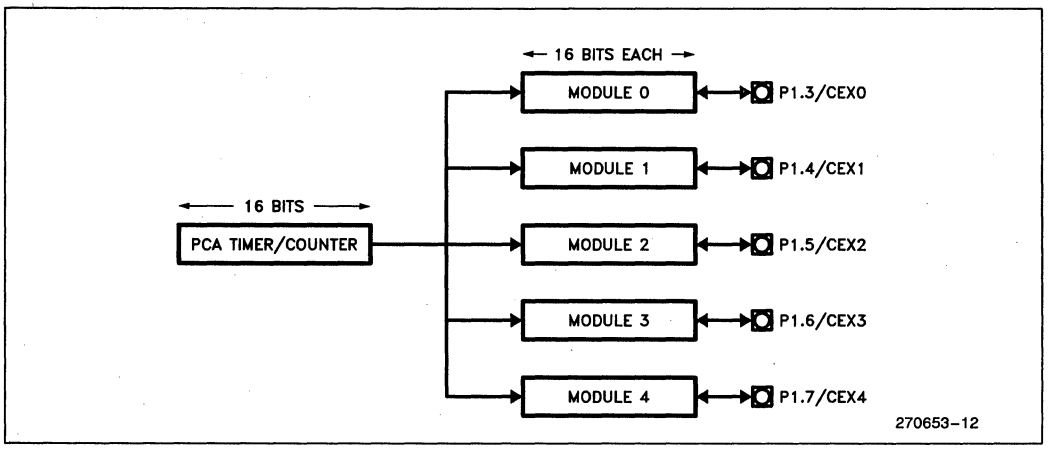


Figure 15a. Programmable Counter Array

The PCA timer/counter and compare/capture modules share Port 1 pins for external I/O. These pins are listed below. If the port pin is not used for the PCA, it can still be used for standard I/O.

PCA Component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

6.1 PCA 16-Bit Timer/Counter

The PCA has a free-running 16-bit timer/counter consisting of registers CH and CL (the high and low bytes of the count value). These two registers can be read or written to at any time. Figure 16 shows a block diagram of this timer. The clock input can be selected from the following four modes:

- Oscillator frequency ÷ 12
  The CL register is incremented at S5P2 of every machine cycle. With a 16 MHz crystal, the timer increments every 750 nanoseconds.
- Oscillator frequency ÷ 4
  The CL register is incremented at S1P2, S3P2 and S5P2 of every machine cycle. With a 16 MHz crystal, the timer increments every 250 nanoseconds.
- Timer 0 overflows
  The CL register is incremented at S5P2 of the machine cycle when Timer 0 overflows. This mode allows a programmable input frequency to the PCA.
- External input
  The CL register is incremented at the first one of S1P2, S3P2 and S5P2 after a 1-to-0 transition is detected on the ECI pin (P1.2). P1.2 is sampled at S1P2, S3P2 and S5P2 of every machine cycle. The maximum input frequency in this mode is oscillator frequency ÷ 8.

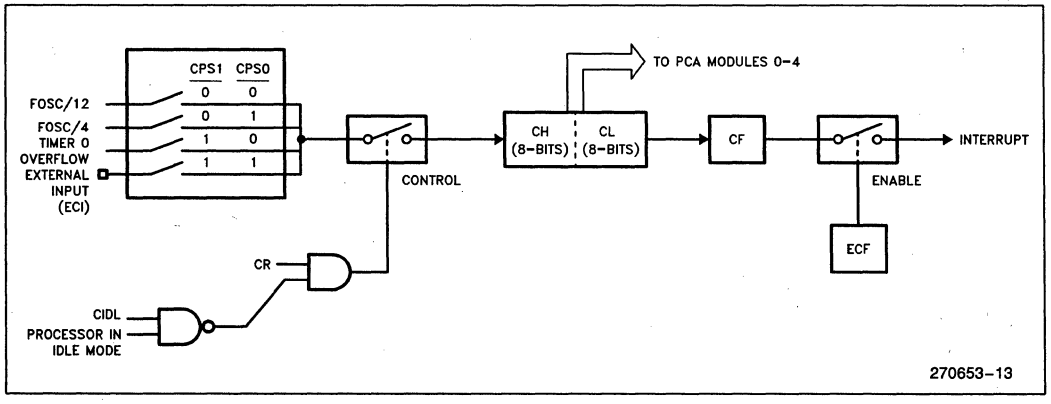


Figure 16. PCA Timer/Counter

CH is incremented after two oscillator periods when CL overflows.

The mode register CMOD contains the Count Pulse Select bits (CPS1 and CPS0) to specify the clock input. CMOD is shown in Table 10. This register also contains the ECF bit which enables the PCA counter overflow to generate the PCA interrupt. In addition, the user has the option of turning off the PCA timer during Idle Mode by setting the Counter Idle bit (CIDL). The Watchdog Timer Enable bit (WDTE) will be discussed in a later section.

The CCON register, shown in Table 11, contains two more bits which are associated with the PCA timer/counter. The CF bit gets set by hardware when the counter overflows, and the CR bit is set or cleared to turn the counter on or off. The other five bits in this register are the event flags for the compare/capture modules and will be discussed in the next section.

Table 10. CMOD: PCA Counter Mode Register

CMOD Address = 0D9H Reset Value = 00XX X000B

Not Bit Addressable

	CIDL	WDTE	—	—	—	CPS1	CPS0	ECF
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.
—	Not implemented, reserved for future use.*
CPS1	PCA Count Pulse Select bit 1.
CPS0	PCA Count Pulse Select bit 0.

CPS1	CPS0	Selected PCA Input**
0	0	Internal clock, Fosc ÷ 12
0	1	Internal clock, Fosc ÷ 4
1	0	Timer 0 overflow
1	1	External clock at ECI/P1.2 pin (max. rate = Fosc ÷ 8)

ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
**Fosc = oscillator frequency

Table 11. CCON: PCA Counter Control Register

CCON Address = 0D8H Reset Value = 00X0 0000B

Bit Addressable

	CF	CR	—	CCF4	CCF3	CCF2	CCF1	CCF0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
—	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

***NOTE:**
User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

6.2 Capture/Compare Modules

Each of the five compare/capture modules has six possible functions it can perform:

- 16-bit Capture, positive-edge triggered
- 16-bit Capture, negative-edge triggered
- 16-bit Capture, both positive and negative-edge triggered
- 16-bit Software Timer
- 16-bit High Speed Output
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer. The modules can be programmed in any combination of the different modes.

Each module has a mode register called CCAPMn (n = 0, 1, 2, 3, or 4) to select which function it will perform. The CCAPMn register is shown in Table 12. Note the ECCFn bit which enables the PCA interrupt when a module's event flag is set. The event flags (CCFn) are located in the CCON register and get set when a capture event, software timer, or high speed output event occurs for a given module.

Table 13 shows the combinations of bits in the CCAPMn register that are valid and have a defined function. Invalid combinations will produce undefined results.

Each module also has a pair of 8-bit compare/capture registers (CCAPnH and CCAPnL) associated with it. These registers store the time when a capture event occurred or when a compare event should occur. For the PWM mode, the high byte regiser CCAPnH controls the duty cycle of the waveform.

The next five sections describe each of the compare/capture modes in detail.

Table 12. CCAPMn: PCA Modules Compare/Capture Registers

CCAPMn Address (n = 0–4): CCAPM0 0DAH, CCAPM1 0DBH, CCAPM2 0DCH, CCAPM3 0DDH, CCAPM4 0DEH — Reset Value = X000 0000B

Not Bit Addressable

	—	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Bit	7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use*.
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Table 13. PCA Module Modes (CCAPMn Register)

—	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module Function
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a postive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative-edge trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	x	0	x	Watchdog Timer

X = Don't Care

6.3 16-Bit Capture Mode

Both positive and negative transitions can trigger a capture with the PCA. This gives the PCA the flexibility to measure periods, pulse widths, duty cycles, and phase differences on up to five separate inputs. Setting the CAPPn and/or CAPNn in the CCAPMn mode register select the input trigger—positive and/or negative transition—for module n. Refer to Figure 17.

The external input pins CEX0 through CEX4 are sampled for a transition. When a valid transition is detected (positive and/or negative edge), hardware loads the 16-bit value of the PCA timer (CH, CL) into the module's capture registers (CCAPnH, CCAPnL). The resulting value in the capture registers reflects the PCA timer value at the time a transition was detected on the CEXn pin.

Upon a capture, the module's event flag (CCFn) in CCON is set, and an interrupt is flagged if the ECCFn bit in the mode register CCAPMn is set. The PCA interrupt will then be generated if it is enabled. Since the hardware does not clear an event flag when the interrupt is vectored to, the flag must be cleared in software. In the interrupt service routine, the 16-bit capture value must be saved in RAM before the next capture event occurs. A subsequent capture on the same CEXn pin will write over the first capture value in CCAPnH and CCAPnL.

6.4 16-Bit Software Timer Mode

In the compare mode, the 16-bit value of the PCA timer is compared with a 16-bit value pre-loaded in the module's compare registers (CCAPnH, CCAPnL). The comparison occurs three times per machine cycle in order to recognize the fastest possible clock input (i.e. ¼ x oscillator frequency). Setting the ECOMn bit in the mode register CCAPMn enables the comparator function as shown in Figure 18.

For the Software Timer mode, the MATn bit also needs to be set. When a match occurs between the PCA timer and the compare registers, a match signal is generated and the module's event flag (CCFn) is set. An interrupt is then flagged if the ECCFn bit is set. The PCA interrupt is generated only if it has been properly enabled. Software must clear the event flag before the next interrupt will be flagged.

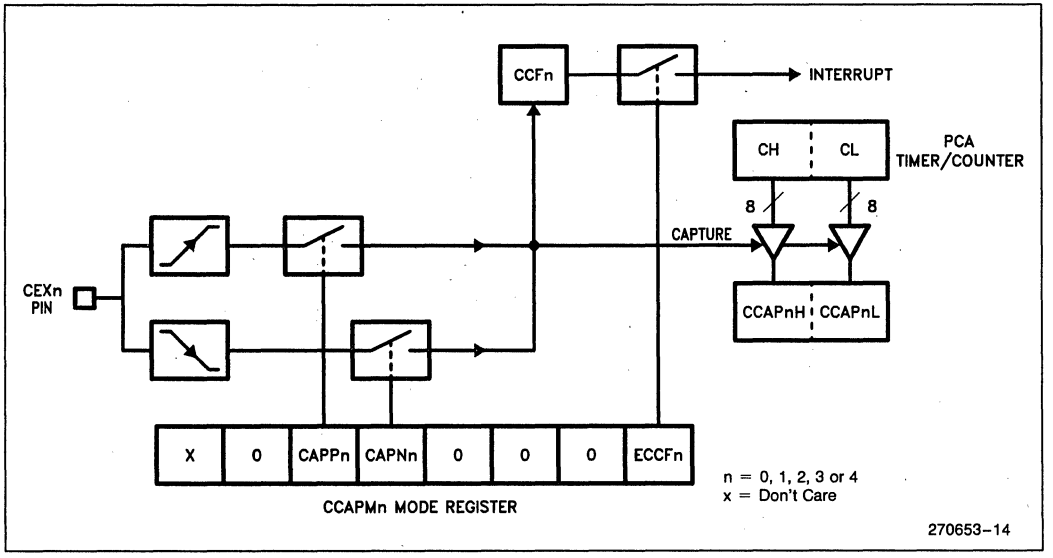


Figure 17. PCA 16-Bit Capture Mode

During the interrupt routine, a new 16-bit compare value can be written to the compare registers (CCAPnH and CCAPnL). *Notice, however, that a write to CCAPnL clears the ECOMn bit which temporarily disables the comparator function while these registers are being updated so an invalid match does not occur.* A write to CCAPnH sets the ECOMn bit and re-enables the comparator. For this reason, user software should write to CCAPnL first, then CCAPnH.

6.5 High Speed Output Mode

The High Speed Output (HSO) mode toggles a CEXn pin when a match occurs between the PCA timer and a pre-loaded value in a module's compare registers. For this mode, the TOGn bit needs to be set in addition to the ECOMn and MATn bits as seen in Figure 18. By setting or clearing the pin in software, the user can select whether the CEXn pin will change from a logical 0 to a logical 1 or vice versa. The user also has the option of flagging an interrupt when a match event occurs by setting the ECCFn bit.

The HSO mode is more accurate than toggling port pins in software because the toggle occurs *before* branching to an interrupt. That is, interrupt latency will not effect the accuracy of the output. If the user does not change the compare registers in an interrupt routine, the next toggle will occur when the PCA timer rolls over and matches the last compare value.

6.6 Watchdog Timer Mode

A Watchdog Timer is a circuit that automatically invokes a reset unless the system being watched sends regular hold-off signals to the Watchdog. These circuits are used in applications that are subject to electrical noise, power glitches, electrostatic discharges, etc., or where high reliability is required.

The Watchdog Timer function is only available on PCA module 4. In this mode, every time the count in the PCA timer matches the value stored in module 4's compare registers, an internal reset is generated. (See Figure 19.) The bit that selects this mode is WDTE in the CMOD register. Module 4 must be set up in either compare mode as a Software Timer or High Speed Output.

When the PCA Watchdog Timer times out, it resets the chip just like a hardware reset, except that it does not drive the reset pin high.

To hold off the reset, the user has three options:

(1) periodically change the compare value so it will never match the PCA timer,

(2) periodically change the PCA timer value so it will never match the compare value,

(3) disable the Watchdog by clearing the WDTE bit before a match occurs and then later re-enable it.

The first two options are more reliable because the Watchdog Timer is never disabled as in option #3. The second option is not recommended if other PCA modules are being used since this timer is the time base for all five modules. Thus, in most applications the first solution is the best option.

If a Watchdog Timer is not needed, module 4 can still be used in other modes.

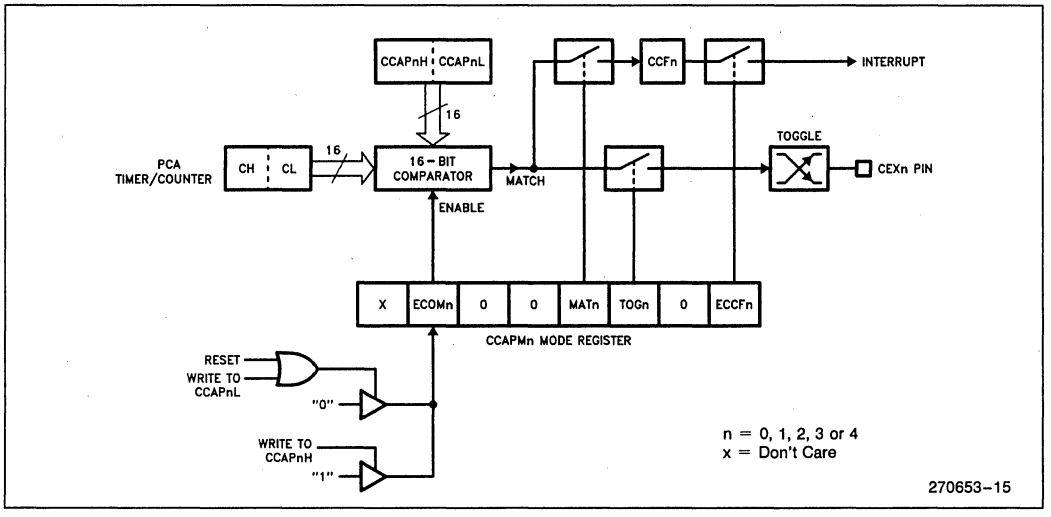


Figure 18. PCA 16-Bit Comparator Mode: Software Timer and High Speed Output

6.7 Pulse Width Modulator Mode

Any or all of the five PCA modules can be programmed to be a Pulse Width Modulator. The PWM output can be used to convert digital data to an analog signal by simple external circuitry. The frequency of the PWM depends on the clock sources for the PCA timer. With a 16 MHz crystal the maximum frequency of the PWM waveform is 15.6 KHz.

The PCA generates 8-bit PWMs by comparing the low byte of the PCA timer (CL) with the low byte of the module's compare registers (CCAPnL). Refer to Figure 20. When CL < CCAPnL the output is low. When CL ≥ CCAPnL the output is high. The value in CCAPnL controls the duty cycle of the waveform. To change the value in CCAPnL without output glitches, the user must write to the high byte register (CCAPnH). This value is then shifted by hardware into CCAPnL when CL rolls over from 0FFH to 00H which corresponds to the next period of the output.

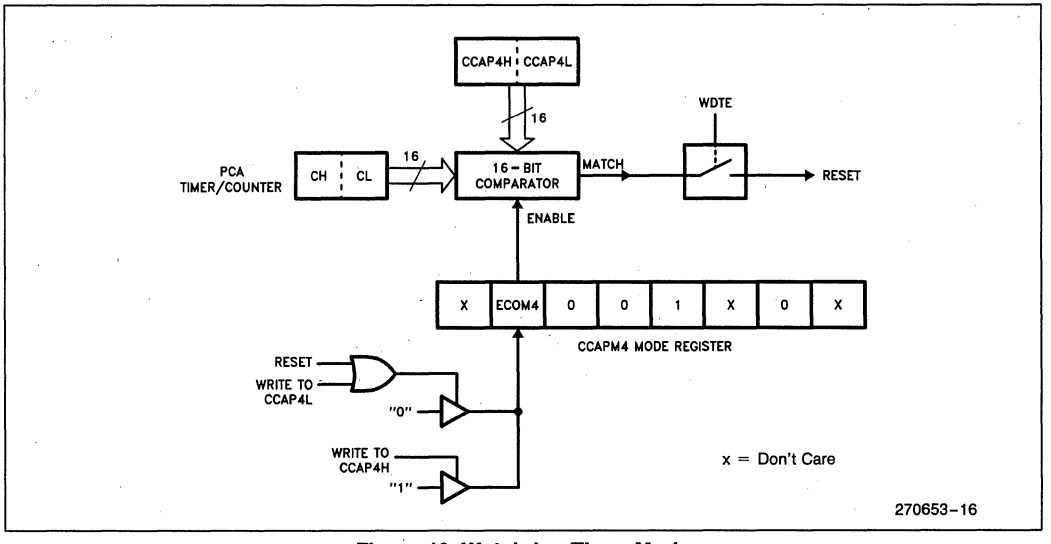


Figure 19. Watchdog Timer Mode

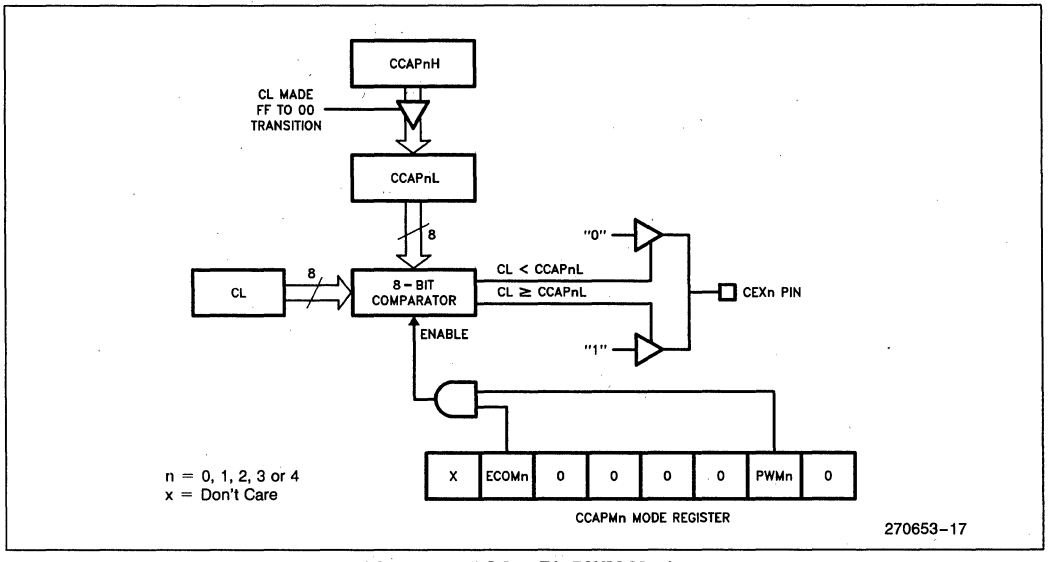


Figure 20. PCA 8-Bit PWM Mode

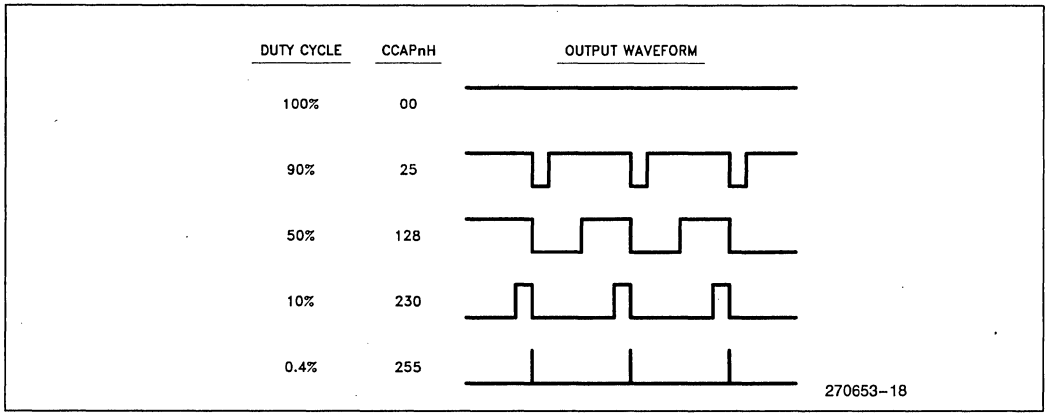


Figure 21. CCAPnH Varies Duty Cycle

CCAPnH can contain any integer from 0 to 255 to vary the duty cycle from a 100% to 0.4% (see Figure 21).

7.0 SERIAL INTERFACE

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Actually, SBUF is two separate registers, a transmit buffer and a receive buffer. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port control and status register is the Special Function Register SCON, shown in Table 14. This register contains the mode selection bits (SM0 and SM1); the SM2 bit for the multiprocessor modes (see Multiprocessor Communications section); the Receive Enable bit (REN); the 9th data bit for transmit and receive (TB8 and RB8); and the serial port interrupt bits (TI and RI).

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Refer to Figure 22. On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in SCON, while the stop bit is ignored. (The validity of the stop bit can be checked with Framing Error Detection.) The baud rate is programmable to either $1/32$ or $1/64$ the oscillator frequency.

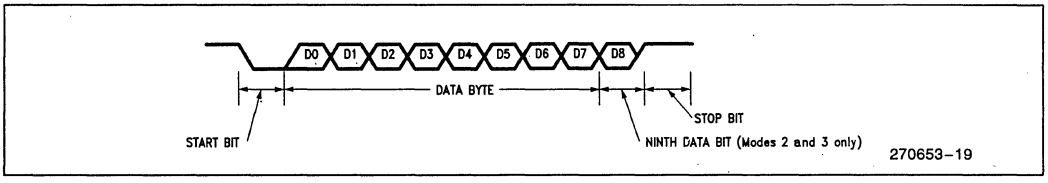


Figure 22. Data Frame: Modes 1, 2 and 3

Mode 3: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except the baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1. For more detailed information on each serial port mode, refer to the "Hardware Description of the 8051, 8052, and 80C51."

7.1 Framing Error Detection

Framing Error Detection allows the serial port to check for valid stop bits in modes 1, 2, or 3. A missing stop bit can be caused, for example, by noise on the serial lines, or transmission by two CPUs simultaneously.

If a stop bit is missing, a Framing Error bit FE is set. The FE bit can be checked in software after each reception to detect communication errors. Once set, the FE bit must be cleared in software. A valid stop bit will not clear FE.

The FE bit is located in SCON and shares the same bit address as SM0. Control bit SMOD0 in the PCON register (location PCON.6) determines whether the SM0 or FE bit is accessed. If SMOD0 = 0, then accesses to SCON.7 are to SM0. If SMOD0 = 1, then accesses to SCON.7 are to FE.

7.2 Multiprocessor Communications

Modes 2 and 3 provide a 9-bit mode to facilitate multiprocessor comunication. The 9th bit allows the controller to distinguish between address and data bytes. The 9th bit is set to 1 for address bytes and set to 0 for data bytes. When receiving, the 9th bit goes into RB8 in SCON. When transmitting, TB8 is set or cleared in software.

The serial port can be programmed such that when the stop bit is received the serial port interrupt will be activated only if the received byte is an address byte (RB8 = 1). This feature is enabled by setting the SM2 bit in SCON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. Remember, an address byte has its 9th bit set to 1, whereas a data byte has its 9th bit set to 0. All the slave processors should have their SM2 bits set to 1 so they will only be interrupted by an address byte. In fact, the C51FX has an Automatic Address Recognition feature which allows only the addressed slave to be interrupted. That is, the address comparison occurs in hardware, not software. (On the 8051 serial port, an address byte interrupts all slaves for an address comparison.)

The addressed slave's software then clears its SM2 bit and prepares to receive the data bytes that will be coming. The other slaves are unaffected by these data bytes. They are still waiting to be addressed since their SM2 bits are all set.

7.3 Automatic Address Recognition

Automatic Address Recognition reduces the CPU time required to service the serial port. Since the CPU is only interrupted when it receives its own address, the software overhead to compare addresses is eliminated. With this feature enabled in one of the 9-bit modes, the Receive Interrupt (RI) flag will only get set when the received byte corresponds to either a Given or Broadcast address.

The feature works the same way in the 8-bit mode (Mode 1) as in the 9-bit modes, except that the stop bit takes the place of the 9th data bit. If SM2 is set, the RI flag is set only if the received byte matches the Given or Broadcast Address and is terminated by a valid stop bit. Setting the SM2 bit has no effect in Mode 0.

The master can selectively communicate with groups of slaves by using the Given Address. Addressing all slaves at once is possible with the Broadcast Address. These addresses are defined for each slave by two Special Function Registers: SADDR and SADEN.

A slave's individual address is specified in SADDR. SADEN is a mask byte that defines don't-cares to form the Given Address. These don't-cares allow flexibility in the user-defined protocol to address one or more slaves at a time. The following is an example of how the user could define Given Addresses to selectively address different slaves.

Slave 1:

SADDR	=	1111	0001
SADEN	=	1111	1010
GIVEN	=	1111	0X0X

Slave 2:

SADDR	=	1111	0011
SADEN	=	1111	1001
GIVEN	=	1111	0XX1

Table 14. SCON: Serial Port Control Register

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
7	6	5	4	3	2	1	0

Bit: (SMOD0 = 0/1)*

Symbol	Function
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0* bit must be set to enable access to the FE bit.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	$F_{OSC}/12$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$F_{OSC}/64$ or $F_{OSC}/32$
1	1	3	9-bit UART	variable

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTE:
*SMOD0 is located at PCON6.
**F_{OSC} = oscillator frequency

The SADEN byte are selected such that each slave can be addressed separately. Notice that bit 1 (LSB) is a don't-care for Slave 1's Given Address, but bit 1 = 1 for Slave 2. Thus, to selectively communicate with just Slave 1 the master must send an address with bit 1 = 0 (e.g. 1111 0000).

Similarly, bit 2 = 0 for Slave 1, but is a don't-care for Slave 2. Now to communicate with just Slave 2 an address with bit 2 = 1 must be used (e.g. 1111 0111).

Finally, for a master to communicate with both slaves at once the address must have bit 1 = 1 and bit 2 = 0. Notice, however, that bit 3 is a don't-care for both slaves. This allows two different addresses to select both slaves (1111 0001 or 1111 0101). If a third slave was added that required its bit 3 = 0, then the latter address could be used to communicate with Slave 1 and 2 but not Slave 3.

The master can also communicate with all slaves at once with the Broadcast Address. It is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-cares. The don't-cares also allow

flexibility in defining the Broadcast Address, but in most applications a Broadcast Address will be 0FFH.

SADDR and SADEN are located at address A9H and B9H, respectively. On reset, the SADDR and SADEN registers are initialized to 00H which defines the Given and Broadcast Addresses as XXXX XXXX (all don't-cares). This assures the C51FX serial port to be backwards compatibility with other MCS®-51 products which do not implement Automatic Addressing.

7.4 Baud Rates

The baud rate in Mode 0 is fixed:

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

The baud rate in Mode 2 depends on the value of bit SMOD1 in Special Function Register PCON. If SMOD1 = 0 (which is the value on reset), the baud rate is $1/64$ the oscillator frequency. If SMOD1 = 1, the baud rate is $1/32$ the oscillator frequency.

$$\text{Mode 2 Baud Rate} = 2^{\text{SMOD1}} \times \frac{\text{Oscillator Frequency}}{64}$$

The baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate, or by Timer 2 overflow rate, or by both (one for transmit and the other for receive).

7.5 Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD1 as follows:

$$\text{Modes 1 and 3 Baud Rate} = 2^{\text{SMOD1}} \times \frac{\text{Timer 1 Overflow Rate}}{32}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In most applications, it is configured for "timer" operation in the auto-reload mode (high nibble of TMOD = 0010B). In this case, the baud rate is given by the formula:

$$\text{Modes 1 and 3 Baud Rate} = \frac{2^{\text{SMOD1}} \times \text{Oscillator Frequency}}{32 \times 12 \times [256 - (\text{TH1})]}$$

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload.

Table 15 lists various commonly used baud rates and how they can be obtained from Timer 1.

7.6 Using Timer 2 to Generate Baud Rates

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 7). Note that the baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 23.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

Table 15. Timer 1 Generated Commonly Used Baud Rates

Baud Rate	f_{OSC}	SMOD	Timer 1		
			C/$\overline{T}$	Mode	Reload Value
Mode 0 Max: 1 MHz	12 MHz	X	X	X	X
Mode 2 Max: 375K	12 MHz	1	X	X	X
Modes 1, 3: 62.5K	12 MHz	1	0	2	FFH
19.2K	11.059 MHz	1	0	2	FDH
9.6K	11.059 MHz	0	0	2	FDH
4.8K	11.059 MHz	0	0	2	FAH
2.4K	11.059 MHz	0	0	2	F4H
1.2K	11.059 MHz	0	0	2	E8H
137.5	11.986 MHz	0	0	2	1DH
110	6 MHz	0	0	2	72H
110	12 MHz	0	0	1	FEEBH

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either "timer" or "counter" operation. In most applications, it is configured for "timer" operation ($C/\overline{T2} = 0$). The "Timer" operation is different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer, it increments every machine cycle (1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (½ the oscillator frequency). The baud rate formula is given below:

$$\text{Modes 1 and 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 23. This figure is valid only if RCLK and/or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the Timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read, but shouldn't be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 16 lists commonly used baud rates and how they can be obtained from Timer 2.

Table 16. Timer 2 Generated Commonly Used Baud Rates

Baud Rate	Osc Freq	Timer 2	
		RCAP2H	RCAP2L
375K	12 MHz	FF	FF
9.6K	12 MHz	FF	D9
4.8K	12 MHz	FF	B2
2.4K	12 MHz	FF	64
1.2K	12 MHz	FE	C8
300	12 MHz	FB	1E
110	12 MHz	F2	AF
300	6 MHz	FD	8F
110	6 MHz	F9	57

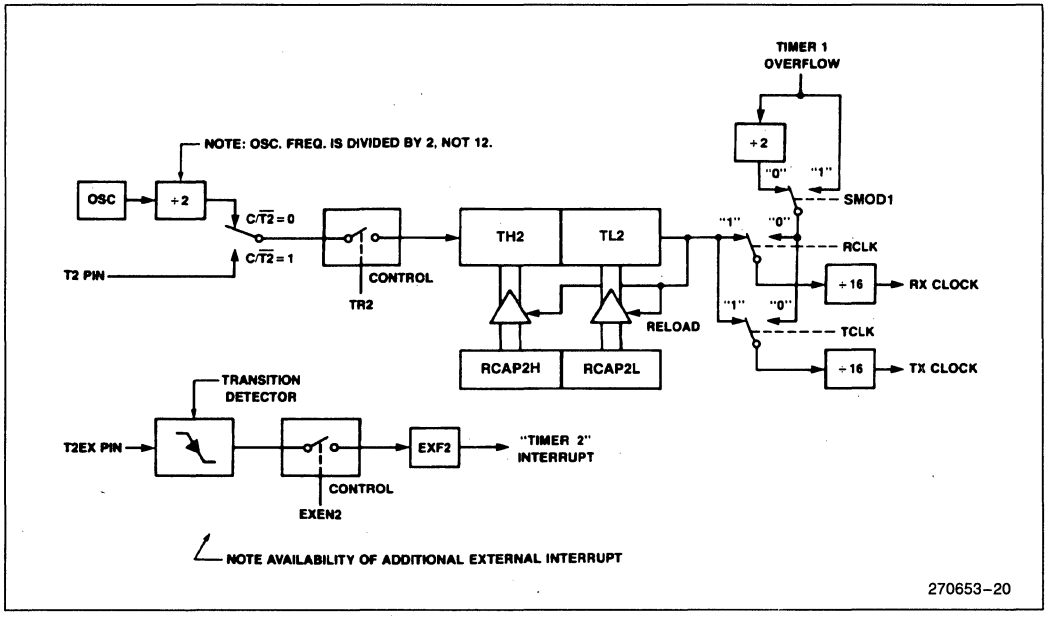


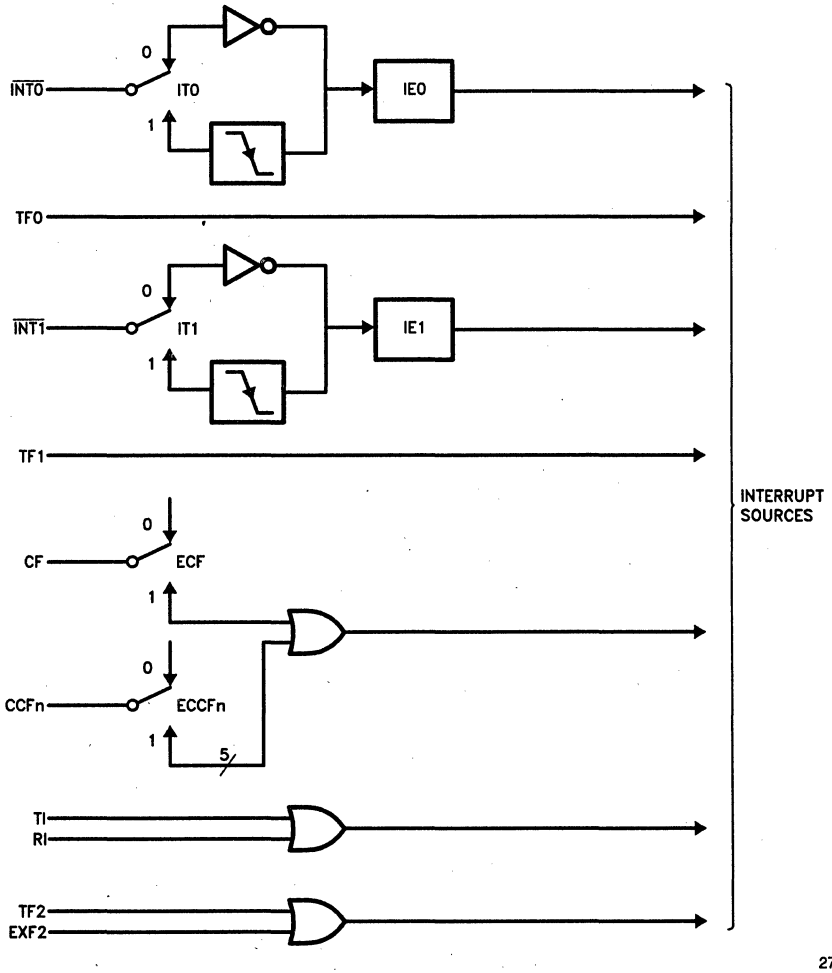
Figure 23. Timer 2 in Baud Rate Generator Mode

8.0 INTERRUPTS

The C51FX has a total of 7 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), the PCA interrupt, and the serial port interrupt. These interrupts are all shown in Figure 24.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled in software.

Each of these interrupts will be briefly described followed by a discussion of the interrupt enable bits and the interrupt priority levels.



(See exceptions when Timer 2 is used as baud rate generator or an up/down counter.)

Figure 24. Interrupt Sources

8.1 External Interrupts

External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{INTx}$ pin. If ITx = 1, external interrupt x is negative edge-triggered. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. These flags are cleared by hardware when the service routine is vectored to only if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source is what controls the request flag, rather than the on-chip hardware.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one cycle, and then hold it low for at least one cycle to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called.

If external interrupt $\overline{INT0}$ or $\overline{INT1}$ is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

8.2 Timer Interrupts

Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1 in register TCON, which are set by a rollover in their respective Timer/Counter registers (except see Timer 0 in Mode 3). When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

Timer 2 Interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and the bit will have to be cleared in software.

8.3 PCA Interrupt

The PCA interrupt is generated by the logical OR of CF, CCF0, CCF1, CCF2, CCF3, and CCF4 in register CCON. None of these flags is cleared by hardware when the service routine is vectored to. Normally the service routine will have to determine which bit flagged the interrupt and clear that bit in software. The PCA interrupt is enabled by bit EC in the Interrupt Enable register (see Table 16). In addition, the CF flag and each of the CCFn flags must also be enabled by bits ECF and ECCFn in registers CMOD and CCAPMn respectively, in order for that flag to be able to cause an interrupt.

8.4 Serial Port Interrupt

The serial port interrupt is generated by the logical OR of bits RI and TI in register SCON. Neither of these flags is cleared by hardware when the service routine is vectored to. The service routine will normally have to determine whether it was RI or TI that generated the interrupt, and the bit will have to be cleared in software.

8.5 Interrupt Enable

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable (IE) register. (See Table 17.) Note that IE also contains a global disable bit, EA. If EA is set (1), the interrupts are individually enabled or disabled by their corresponding bits in IE. If EA is clear (0), all interrupts are disabled.

8.6 Priority Level Structure

Each interrupt source can also be individually programmed to one of two priority levels, by setting or clearing a bit in the Interrupt Priority (IP) register shown in Table 18. A low-priority interrupt can itself be interrupted by a higher priority interrupt, but not by another low-priority interrupt. A high priority interrupt cannot be interrupted by any other interrupt source.

Table 17. IE: Interrupt Enable Register

IE Address = 0A8H Reset Value = 0000 0000B

Bit Addressable

	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

Symbol	Function
EA	Global disable bit. If EA = 0, all Interrupts are disabled. If EA = 1, each Interrupt can be individually enabled or disabled by setting or clearing its enable bit.
EC	PCA interrupt enable bit.
ET2	Timer 2 interrupt enable bit.
ES	Serial Port interrupt enable bit.
ET1	Timer 1 interrupt enable bit.
EX1	External interrupt 1 enable bit.
ET0	Timer 0 interrupt enable bit.
EX0	External interrupt 0 enable bit.

Table 18. IP: Interrupt Priority Registers

IP **Address = 0B8H** **Reset Value = X000 0000B**

Bit Addressable

	—	PPC	PT2	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

Priority Bit = 1 assigns high priority
Priority Bit = 0 assigns low priority

Symbol	Function
—	Not implemented, reserved for future use.*
PPC	PCA interrupt priority bit.
PT2	Timer 2 interrupt priority bit.
PS	Serial Port interrupt priority bit.
PT1	Timer 1 interrupt priority bit.
PX1	External interrupt 1 priority bit.
PT0	Timer 0 interrupt priority bit.
PX0	External interrupt 0 priority bit.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the **same** priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence shown in Table 19.

Note that the "priority within level" structure is only used to resolve *simultaneous requests of the same priority level.*

Table 19. Interrupt Priority within Level Polling Sequence

1 (Highest)	$\overline{INT0}$
2	Timer 0
3	$\overline{INT1}$
4	Timer 1
5	PCA
6	Serial Port
7 (Lowest)	Timer 2

8XC51FX Interrupt Priority Structure

In the 8XC51FX, a second Interrupt Priority register (IPH) has been added, increasing the number of priority levels to four. Table 20 shows this second register. The added register becomes the MSB of the priority select bits and the existing IP register acts as the LSB. This scheme maintains compatibility with the rest of the MCS-51 family. Table 21 shows the bit values and priority levels associated with each combination.

Table 21. Priority Level Bit Values

Priority Bits		Interrupt Priority Level
IPH.x	IP.x	
0	0	Level 0 (Lowest)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (Highest)

How Interrupts are Handled

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. The Timer 2 interrupt cycle is slightly different, as described in the Response Time section. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress.
2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3. The instruction in progress is RETI or any write to the IE or IP registers.

Table 20. IPH: Interrupt Priority High Register

IPH **Address = 0B7H** **Reset Value = X000 0000**

Not Bit Addressable

	—	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.
PPCH	PCA interrupt priority high bit.
PT2H	Timer 2 interrupt priority high bit.
PSH	Serial Port interrupt priority high bit.
PT1H	Timer 1 interrupt priority high bit.
PX1H	External interrupt 1 priority high bit.
PT0H	Timer 0 interrupt priority high bit.
PX0H	External interrupt priority high bit.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any write to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. If the interrupt flag for a *level-sensitive* external interrupt is active but not being responded to for one of the above conditions and is not *still* active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The polling cycle/LCALL sequence is illustrated in Figure 25.

Note that if an interrupt of a higher priority level goes active prior to S5P2 of the machine cycle labeled C3 in Figure 25, then in accordance with the above rules it will be vectored to during C5 and C6, without any instruction of the lower priority routine having been executed.

Thus the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. The hardware-generated LCALL pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as shown in Table 22.

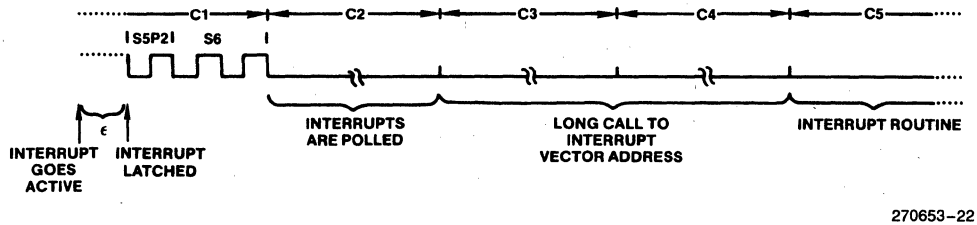
Table 22. Interrupt Vector Address

Interrupt Source	Interrupt Request Bits	Cleared by Hardware	Vector Address
$\overline{\text{INT0}}$	IE0	No (level) Yes (trans.)	0003H
TIMER 0	TF0	Yes	000BH
$\overline{\text{INT1}}$	IE1	No (level) Yes (trans.)	0013H
TIMER 1	TF1	Yes	001BH
SERIAL PORT	RI, TI	No	0023H
TIMER 2	TF2, EXF2	No	002BH
PCA	CF, CCFn (n = 0-4)	No	0033H

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking interrupt was still in progress.

Note that the starting addresses of consecutive interrupt service routines are only 8 bytes apart. That means if consecutive interrupts are being used (IE0 and TF0, for example, or TF0 and IE1), and if the first interrupt routine is more than 7 bytes long, then that routine will have to execute a jump to some other memory location where the service routine can be completed without overlapping the starting address of the next interrupt routine.



This is the fastest possible response when C2 is the final cycle of an instruction other than RETI or write IE or IP.

Figure 25. Interrupt Response Timing Diagram

8.7 Response Time

The $\overline{INT0}$ and $\overline{INT1}$ levels are inverted and latched into the Interrupt Flags IE0 and IE1 at S5P2 of every machine cycle. Similarly, the Timer 2 flag EXF2 and the Serial Port flags RI and TI are set at S5P2. The values are not actually polled by the circuitry until the next machine cycle.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag TF2 is set at S2P2 and is polled in the same cycle in which the timer overflows.

If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes two cycles. Thus, a minimum of three complete machine cycles elapses between activation of an external interrupt request and the beginning of execution of the service routine's first instruction. Figure 25 shows interrupt response timing.

A longer response time would result if the request is blocked by one of the 3 previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than 3 cycles, since the longest instructions (MUL and DIV) are only 4 cycles long, and if the instruction in progress is RETI or write to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one or more cycle to complete the instruction in progress, plus 4 cycles to complete the next instruction if the instruction is MUL or DIV).

Thus, in a single-interrupt system, the response time is always more than 3 cycles and less than 9 cycles.

9.0 RESET

The reset input is the RST pin, which has a Schmitt Trigger input. A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) *while the oscillator is running*. The CPU responds by generating an internal reset, with the timing shown in Figure 26.

The external reset signal is asynchronous to the internal clock. The RST pin is sampled during State 5 Phase 2 of every machine cycle. ALE and PSEN will maintain their current activities for 19 oscillator periods after a logic 1 has been sampled at the RST pin; that is, for 19 to 31 oscillator periods after the external reset signal has been applied to the RST pin. The port pins are driven to their reset state as soon as a valid high is detected on the RST pin, regardless of whether the clock is running.

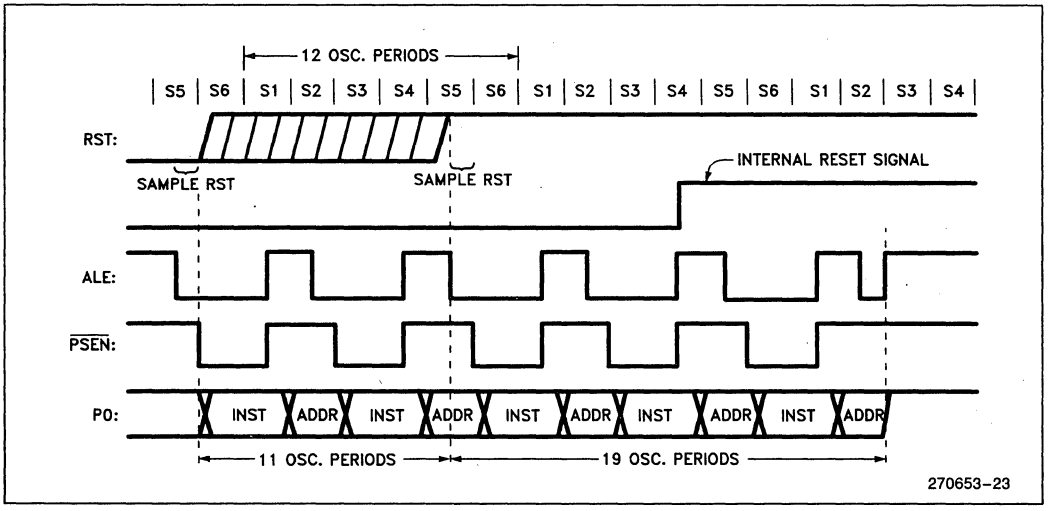


Figure 26. Reset Timing

While the RST pin is high, the port pins, ALE and $\overline{PSEN}$ are weakly pulled high. After RST is pulled low, it will take 1 to 2 machine cycles for ALE and $\overline{PSEN}$ to start clocking. For this reason, other devices can not be synchronized to the internal timings of the 8XC51FX.

Driving the ALE and $\overline{PSEN}$ pins to 0 while reset is active could cause the device to go into an indeterminate state.

The internal reset algorithm redefines all the SFRs. Table 1 lists the SFRs and their reset values. The internal RAM is not affected by reset. On power up the RAM content is indeterminate.

9.1 Power-On Reset

For CHMOS devices, when VCC is turned on, an automatic reset can be obtained by connecting the RST pin to VCC through a 1 μF capacitor (Figure 27). The CHMOS devices do not require an external resistor like the HMOS devices because they have an internal pulldown on the RST pin.

When power is turned on, the circuit holds the RST pin high for an amount of time that depends on the capacitor value and the rate at which it charges. To ensure a valid reset the RST pin must be held high long enough to allow the oscillator to start up plus two machine cycles.

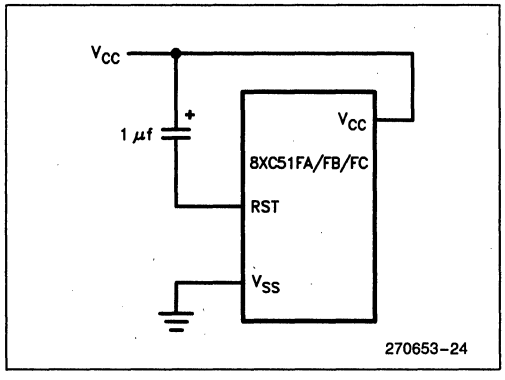


Figure 27. Power on Reset Circuitry

On power up, V_{CC} should rise within approximately ten milliseconds. The oscillator start-up time will depend on the oscillator frequency. For a 10 MHz crystal, the start-up time is typically 1 msec. For a 1 MHz crystal, the start-up time is typically 10 msec.

With the given circuit, reducing V_{CC} quickly to 0 causes the RST pin voltage to momentarily fall below 0V. However, this voltage is internally limited and will not harm the device.

Note that the port pins will be in a random state until the oscillator has started and the internal reset algorithm has written Is to them.

Powering up the device without a valid reset could cause the CPU to start executing instructions from an indeterminate location. This is because the SFRs, specifically the Program Counter, may not get properly initialized.

10.0 POWER-SAVING MODES OF OPERATION

For applications where power consumption is critical, the C51FX provides two power reducing modes of operation: Idle and Power Down. The input through which backup power is supplied during these operations is V_{CC}. Figure 28 shows the internal circuitry which implements these features. In the Idle mode (IDL = 1), the oscillator continues to run and the Interrupt, Serial Port, PCA, and Timer blocks continue to be clocked, but the clock signal is gated off to the CPU. In Power Down (PD = 1), the oscillator is frozen. The Idle and Power Down modes are activated by setting bits in Special Function Register PCON (Table 23).

10.1 Idle Mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the Interrupt, Timer, and Serial Port functions. The PCA can be programmed either to pause or continue operating during Idle (refer to the PCA section for more details). The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and $\overline{PSEN}$ hold at logic high levels.

There are two ways to terminate the Idle Mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into Idle.

The flag bits (GF0 and GF1) can be used to give an indication if an interrupt occurred during normal operation or during Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

The signal at the RST pin clears the IDL bit directly and asynchronously. At this time the CPU resumes program execution from where it left off; that is, at the instruction following the one that invoked the Idle Mode. As shown in Figure 26, two or three machine cycles of program execution may take place before the

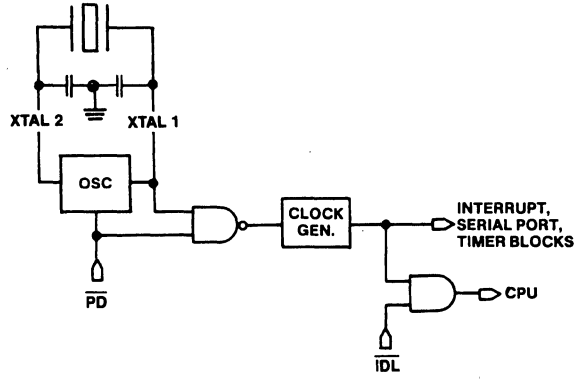


Figure 28. Idle and Power Down Hardware

Table 23. PCON: Power Control Register

PCON Address = 87H Reset Value = 00XX 0000B

Not Bit Addressable

	SMOD1	SMOD0	—	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud rate bit. When set to a 1 and Timer 1 is used to generate baud rates, and the Serial Port is used in modes 1, 2, or 3.
SMOD0	When set, Read/Write accesses to SCON.7 are to the FE bit. When clear, Read/Write accesses to SCON.7 are to the SM0 bit.
—	Not implemented, reserved for future use.*
POF	Power Off Flag. Set by hardware on the rising edge of V_{CC}. Set or cleared by software. This flag allows detection of a power failure caused reset. V_{CC} must remain above 3V to retain this bit.
GF1	General-purpose flag bit.
GF0	General-purpose flag bit.
PD	Power Down bit. Setting this bit activates Power Down operation.
IDL	Idle mode bit. Setting this bit activates idle modes operation. If 1s are written to PD and IDL at the same time, PD takes precedence.

NOTE:
*User software should not write 1s to unimplemented bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate

internal reset algorithm takes control. On-chip hardware inhibits access to the internal RAM during this time, but access to the port pins is not inhibited. To eliminate the possibility of unexpected outputs at the port pins, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external Data RAM.

10.2 Power Down Mode

An instruction that sets PCON.1 causes that to be the last instruction executed before going into the Power Down mode. In this mode the on-chip oscillator is stopped. With the clock frozen, all functions are stopped, but the on-chip RAM and Special Function Registers are held. The port pins output the values held by their respective SFRs, and ALE and $\overline{PSEN}$ output lows. In Power Down V_{CC} can be reduced to as low as 2V. Care must be taken, however, to ensure that V_{CC} is not reduced before Power Down is invoked.

The C51FX can exit Power Down with either a hardware reset or external interrupt. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 msec).

With an external interrupt, $\overline{INT0}$ or $\overline{INT1}$ must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator and bringing the pin back high completes the exit. After the RETI instruction is executed in the interrupt service routine, the next instruction will be the one following the instruction that put the device in Power Down.

10.3 Power Off Flag

The Power Off Flag (POF) located at PCON.4, is set by hardware when V_{CC} rises from 0 to 5 Volts. POF can also be set or cleared by software. This allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is one that is coincident with V_{CC} being turned on to the device after it was turned off. A warm start reset occurs while V_{CC} is still applied to the device and could be generated, for example, by a Watchdog Timer or an exit from Power Down.

Immediately after reset, the user's software can check the status of the POF bit. POF = 1 would indicate a cold start. The software then clears POF and commences its tasks. POF = 0 immediately after reset would indicate a warm start.

V_{CC} must remain above 3 volts for POF to retain a 0.

11.0 EPROM VERSIONS

The 8XC51FX uses the Improved "Quick-Pulse" programming™ algorithm. These devices program at V_{PP} = 12.75V (and V_{CC} = 5.0V) using a series of five 100 μs $\overline{PROG}$ pulses per byte programmed. This results in a total programming time of approximately 5 seconds for the 87C51FA's 8 Kbytes, 10 seconds for the 87C51FB's 16 Kbytes, and 20 seconds for the 87C51FC's 32 Kbytes.

Exposure to Light: The EPROM window must be covered with an opaque label when the device is in operation. This is not so much to protect the EPROM array from inadvertent erasure, but to protect the RAM and other on-chip logic. Allowing light to impinge on the silicon die while the device is operating can cause logical malfunction.

12.0 PROGRAM MEMORY LOCK

In some microcontroller applications, it is desirable that the Program Memory be secure from software piracy. The C51FX has varying degrees of program protection depending on the device. Table 24 outlines the lock schemes available for each device.

Encryption Array: Within the EPROM/ROM is an array of encryption bytes that are initially unprogrammed (all 1's). For EPROM devices, the user can program the encryption array to encrypt the program code bytes during EPROM verification. For ROM devices, the user submits the encryption array to be programmed by the factory. If an encryption array is submitted, LB1 will also be programmed by the factory. The encryption array is not available without the Lock Bit. Program code verification is performed as usual, except that each code byte comes out exclusive-NOR'ed (XNOR) with

one of the key bytes. Therefore, to read the ROM/EPROM code, the user has to know the encryption key bytes in their proper sequence.

Unprogrammed bytes have the value 0FFH. If the Encryption Array is left unprogrammed, all the key bytes have the value 0FFH. Since any code byte XNOR'ed with 0FFH leaves the byte unchanged, leaving the Encryption Array unprogrammed in effect bypasses the encryption feature.

When using the encryption array feature, one important factor should be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the encryption array contents. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits: Also included in the Program Lock scheme are Lock Bits which can be enabled to provide varying degrees of protection. Table 25 lists the Lock Bits and their corresponding influence on the microcontroller. Refer to Table 24 for the Lock Bits available on the various products. The user is responsible for programming the Lock Bits on EPROM devices. On ROM devices, LB1 is automatically set by the factory when the encryption array is submitted. The Lock Bit is not available without the encryption array on ROM devices.

Erasing the EPROM also erases the Encryption Array and the Lock Bits, returning the part to full functionality.

Table 24. C51FX Program Protection

Device	Lock Bits	Encrypt Array
83C51FA	None	None
83C51FB	LB1	64 Bytes
83C51FC	LB1	64 Bytes
87C51FA	LB1, LB2, LB3	64 Bytes
87C51FB	LB1, LB2, LB3	64 Bytes
87C51FC	LB1, LB2, LB3	64 Bytes

13.0 ONCE™ MODE

The ONCE (ON-Circuit Emulation) mode facilitates testing and debugging of systems using the C51FX without having to remove the device from the circuit. The ONCE mode is invoked by:

1. Pulling ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Holding ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins go into a float state, and the other port pins, ALE, and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit.

Normal operation is restored after a valid reset is applied.

Table 25. Lock Bits

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. (Code verify will still be encrypted by the encryption array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

P = Programmed
U = Unprogrammed
Any other combination of the Lock Bits is not defined.

14.0 ON-CHIP OSCILLATOR

The on-chip oscillator for the CHMOS devices, shown in Figure 29, consists of a single stage linear inverter intended for use as a crystal-controlled, positive reactance oscillator. In this application the crystal is operating in its fundamental response mode as an inductive reactance in parallel resonance with capacitance external to the crystal (Figure 30).

The oscillator on the CHMOS devices can be turned off under software control by setting the PD bit in the PCON register. The feedback resistor R_f in Figure 29 consists of paralleled n- and p-channel FETs controlled by the PD bit, such that R_f is opened when PD = 1. The diodes D1 and D2, which act as clamps to V_{CC} and V_{SS}, are parasitic to the R_f FETs.

The crystal specifications and capacitance values (C1 and C2 in Figure 30) are not critical. 30 pF can be used in these positions at any frequency with good quality crystals. In general, crystals used with these devices typically have the following specifications:

ESR (Equivalent Series Resistance)	see Figure 32
C_O (shunt capacitance)	7.0 pF maximum
C_L (load capacitance)	30 pF ±3 pF
Drive Level	1 MW

Frequency, tolerance, and temperature range are determined by the system requirements.

A ceramic resonator can be used in place of the crystal in cost-sensitive applications. When a ceramic resonator is used, C1 and C2 are normally selected as higher values, typically 47 pF. The manufacturer of the ceramic resonator should be consulted for recommendations on the values of these capacitors.

A more in-depth discussion of crystal specifications, ceramic resonators, and the selection of values for C1 and C2 can be found in Application Note AP-155, "Oscillators for Microcontrollers" in the Embedded Applications handbook.

To drive the CHMOS parts with an external clock source, apply the external clock signal to XTAL1 and leave XTAL2 floating as shown in Figure 31. This is an important difference from the HMOS parts. With HMOS, the external clock source is applied to XTAL2, and XTAL1 is grounded.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

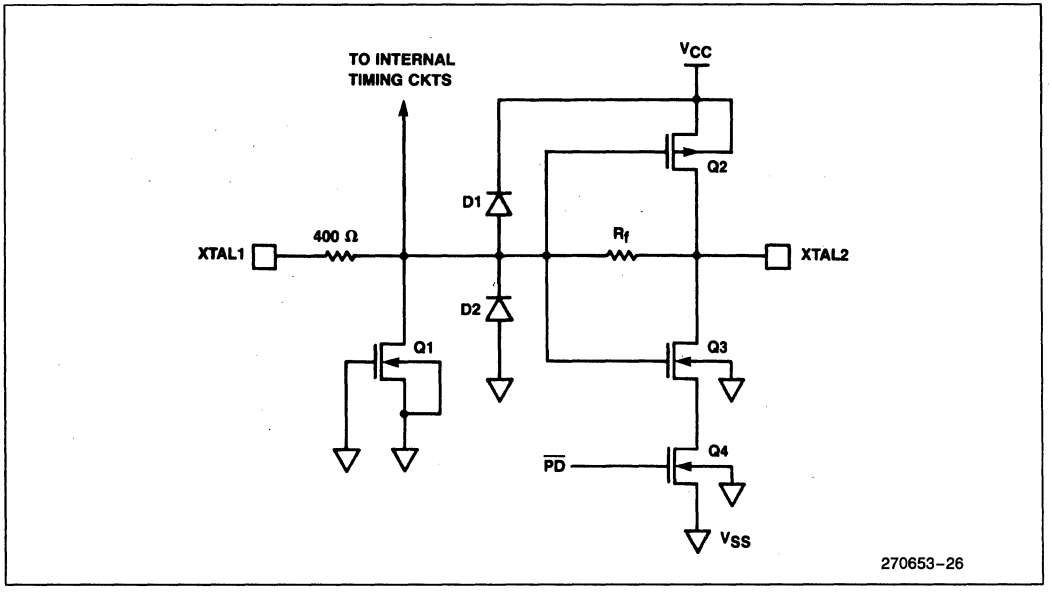


Figure 29. On-Chip Oscillator Circuitry

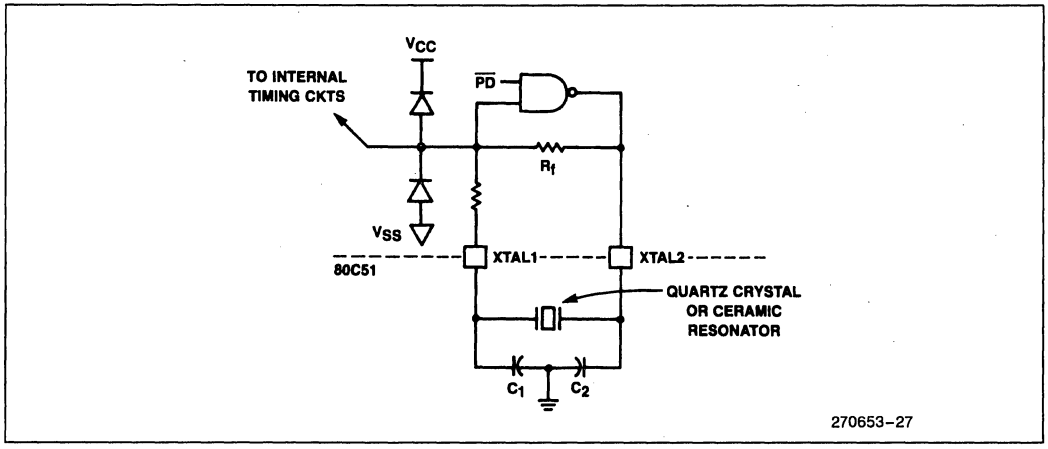


Figure 30. Using the CHMOS On-Chip Oscillator

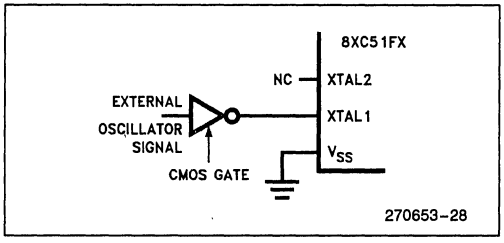


Figure 31. Driving the CHMOS Parts with an External Clock Source

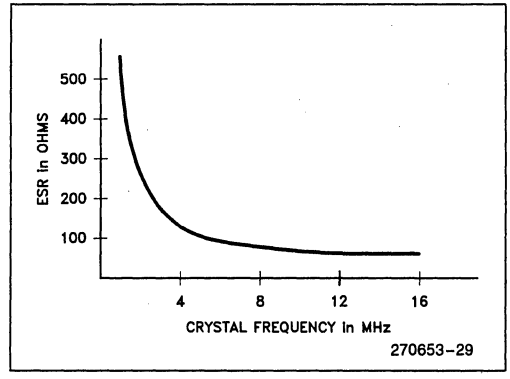


Figure 32. ESR vs Frequency

15.0 CPU TIMING

The internal clock generator defines the sequence of states that make up a machine cycle. A machine cycle consists of 6 states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus a machine cycle takes 12 oscillator periods or 1 microsecond if the oscillator frequency is 12 MHz. Each state is then divided into a Phase 1 and Phase 2 half.

Rise and fall times are dependent on the external loading that each pin must drive. They are approximately 10 nsec, measured between 0.8V and 2.0V.

Propagation delays are different for different pins. For a given pin they vary with pin loading, temperature, V_{CC}, and manufacturing lot. If the XTAL1 waveform is taken as the timing reference, propagation delays may vary from 25 to 125 nsec.

The AC Timings section of the data sheets do not reference any timing to the XTAL1 waveform. Rather, they relate the critical edges of control and input signals to each other. The timings published in the data sheets include the effects of propagation delays under the specified test condition.

ADDITIONAL REFERENCES

The following application notes provide supplemental information to this document and can be found in the *Embedded Applications* handbook.

1. AP-125 "Designing Microcontroller Systems for Electrically Noisy Environments"
2. AP-155 "Oscillators for Microcontrollers"
3. AP-252 "Designing with the 80C51BH"
4. AP-410 "Enhanced Serial Port on the 83C51FA"
5. AP-415 "83C51FA/FB PCA Cookbook"
6. AB-41 "Software Serial Port Implemented with the PCA"
7. AP-425 "Small DC Motor Control"
8. The appropriate data sheet.

83C51FA/80C51FA

EXPRESS

83C51FA/80C51FA—3.5 MHz to 12 MHz, V_{CC} = 5V ±10%
83C51FA-1/80C51FA-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±10%
83C51FA-2/80C51FA-2—0.5 MHz to 12 MHz, V_{CC} = 5V ±10%

- **Extended Temperature Range**
- **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.

August 1988
Order Number: 270620-001

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)		−75	μA	$V_{in} = 0.45V$
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$V_{CC} - 1.5$		V	$I_{OH} = -6.0$ mA

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD	Cerdip	Extended	No
TN	PLCC	Extended	No
LP	Plastic	Extended	Yes
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

NOTE:
- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-in is dynamic for a minimum time of 168 hours at 125°C, $V_{CC} = 6.9V \pm 0.25V$, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples:

P83C51FA indicates 83C51FA in a plastic package and specified for commercial temperature range, without burn-in.
LD80C51FA indicates 80C51FA in a cerdip package and specified for extended temperature range with burn-in.

8

intel®

87C51FA/83C51FA/80C51FA
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 8 KBYTES INTERNAL PROGRAM MEMORY

87C51FA/83C51FA/80C51FA—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C51FA-1/83C51FA-1/80C51FA-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%
83C51FA-2/80C51FA-2—0.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C51FA-L—3.5 MHz to 8 MHz, V_{CC} = 3.3V ±0.3V

- High Performance CHMOS EPROM
- Low Voltage Operation (-L only)
- Power Control Modes
- Three 16-Bit Timer/Counters
- Programmable Counter Array with:
  - —High Speed Output,
  - —Compare/Capture,
  - —Pulse Width Modulator,
  - —Watchdog Timer Capabilities
- Up/Down Timer/Counter
- Three Level Program Lock System
- 8K On-Chip Program Memory
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 7 Interrupt Sources
- Programmable Serial Channel with:
  - —Framing Error Detection
  - —Automatic Address Recognition
- TTL Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside on-chip (except 80C51FA). In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C51FA is a single-chip control oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. The Intel 83C51FA/80C51FA is fabricated on CHMOS III technology. Being a member of the MCS®-51 family, the 87C51FA/83C51FA/80C51FA uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 products. The 87C51FA/83C51FA/80C51FA is an enhanced version of the 87C52/80C52/80C32. Its added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multiprocessor communications.

Applications that require low voltage operation can use the 87C51FA-L. The 87C51FA-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz.

For the remainder of this document, the 87C51FA, 83C51FA, 80C51FA will be referred to as the 8XC51FA, unless information applies to a specific device.

October 1992
Order Number: 270258-007

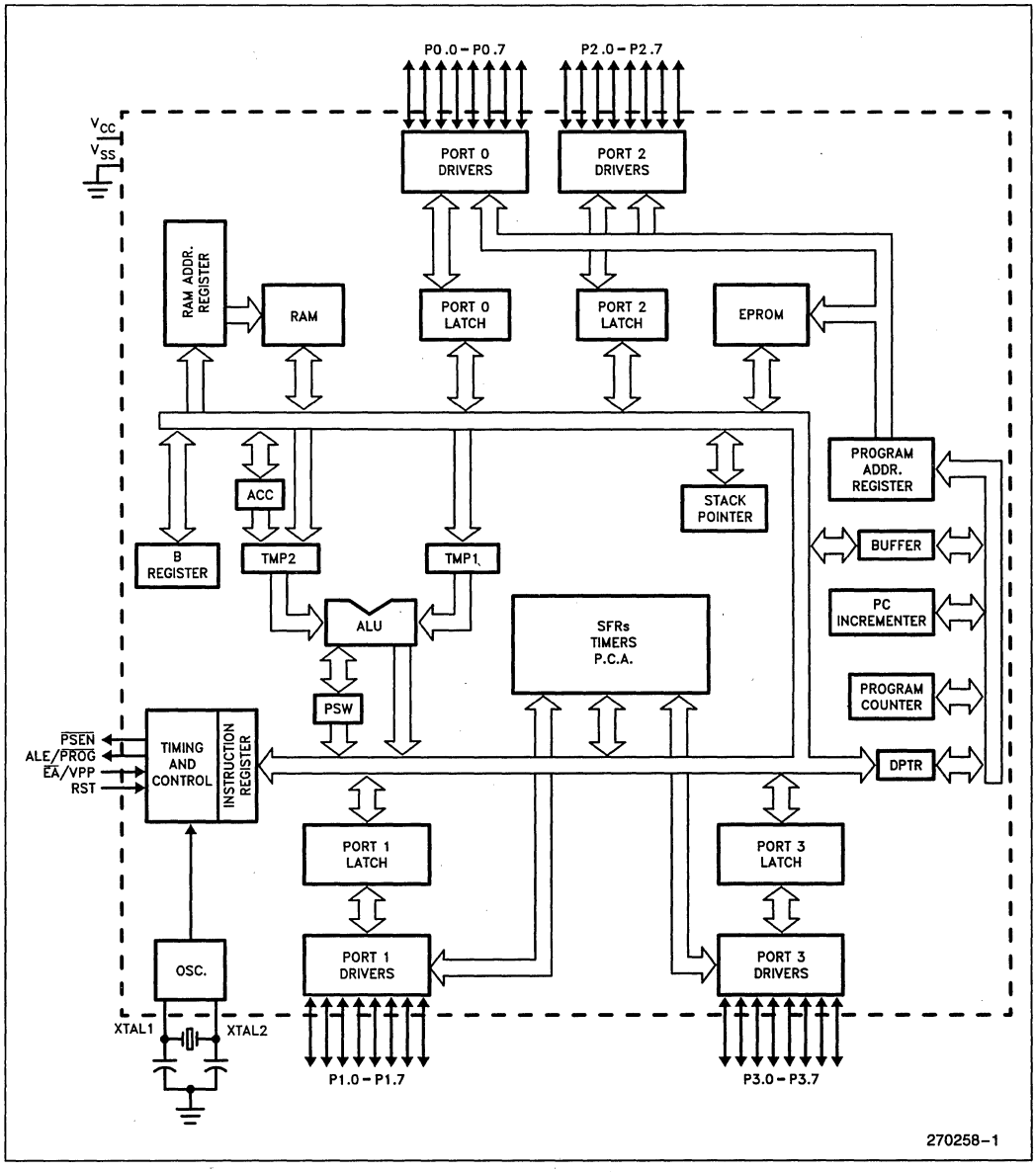


Figure 1. 8XC51FA Block Diagram

PROCESS INFORMATION

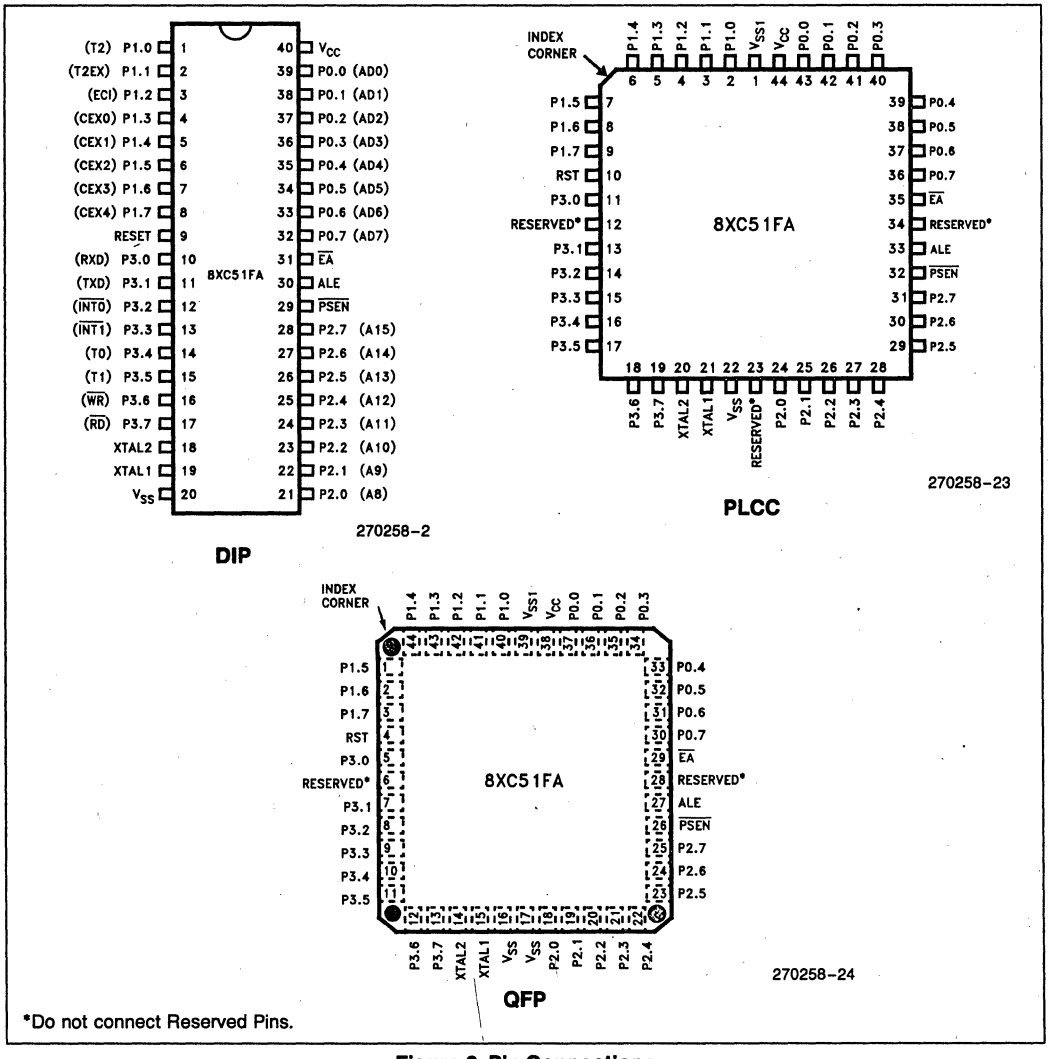
The 87C51FA is manufactured on P629.0, a CHMOS III-E process. The 83C51FA/80C51FA are manufactured on P645, a CHMOS III process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
87C51FA	P	40-Pin Plastic DIP (OTP)	45°C/W	16°C/W
	D	40-Pin CERDIP (EPROM)	45°C/W	15°C/W
	N	44-Pin PLCC (OTP)	46°C/W	16°C/W
	S	44-Pin QFP (OTP)	97°C/W	24°C/W

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
83C51FA/ 80C51FA	P	40-Pin Plastic DIP	45°C/W	16°C/W
	D	40-Pin CERDIP	36°C/W	13°C/W
	N	44-Pin PLCC	46°C/W	16°C/W
	S	44-Pin QFP	97°C/W	24°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



*Do not connect Reserved Pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (only on PLCC and QFP of 87C51FA). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitution for the V_{SS} pin.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC51FA:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not (87C51FA only). An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51FA.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51FA is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

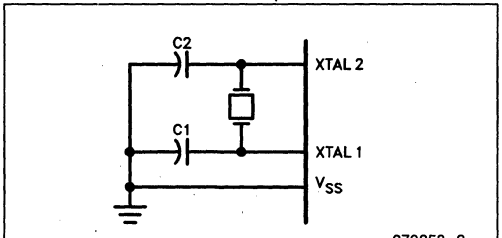
XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 3. Oscillator Connections

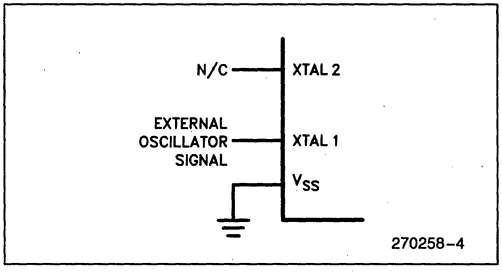


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power

Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51FA either hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- The 87C51FA-L will operate at 3.3V ±0.3V with a frequency range of 3.5 MHz to 8 MHz. Operating beyond these specifications could cause improper device functionality. (To program the 87C51FA-L, follow the same procedure as the 87C51FA).
- Ambient light is known to affect the internal RAM contents during operation. If the 87C51FA application requires the part to be run under ambient lighting, an opaque label should be placed over the window to exclude light.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- The 87C51FA has some additional features that are not available on the 83C51FA/80C51FA. The features are: Timer 2 clockout, 4 interrupt priority levels, asynchronous port reset, 64-byte encryption array, and 3 program lock bits. These features cannot be used with the 83C51FA/80C51FA.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC51FA without the 8XC51FA having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51FA is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

T_A (Under Bias) = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V
(87C51FA-L, V_{CC} = 3.3V ±0.3V)

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typical (Note 4)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Note 5) (Ports 1, 2 and 3)			0.3 0.45 1.0	V	I_{OL} = 100μA I_{OL} = 1.6 mA (Note 1) I_{OL} = 3.5 mA
V_{OL1}	Output Low Voltage (Note 5) (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)			0.3 0.45 1.0	V	I_{OL} = 200 μA I_{OL} = 3.2 mA (Note 1) I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Ports 1, 2 and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −10 μA I_{OH} = −30 μA (Note 2) I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA (Note 2) I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)			±10	μA	V_{IN} = V_{IL} or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)			−650	μA	V_{IN} = 2V

DC CHARACTERISTICS (Over Operating Conditions)

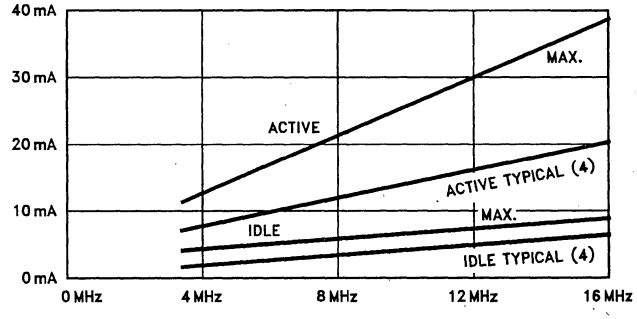
All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typical (Note 4)	Max	Units	Test Conditions
RRST	RST Pulldown Resistor					
	87C51FA	50		300	KΩ	
	83C51FA/80C51FA	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1MHz, 25°C
I_{CC}	Power Supply Current:					(Note 3)
	Active Mode					
	87C51FA-L at 8 MHz			12	mA	
	All Others at 12 MHz (Figure 5)		20	40	mA	
	Idle Mode at 12 MHz (Figure 5)		5	7.5	mA	
	Power Down Mode		5	75	μA	

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitance loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for power down is 2V.
4. Typicals are based on limited number of samples, and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port -
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} MAX = 2.2 × FREQ + 3.1
Idle Mode
I_{CC} MAX = 0.49 × FREQ + 1.6
Where FREQ is in MHz, I_{CC}MAX is given in mA.

Figure 5. I_{CC} vs Frequency

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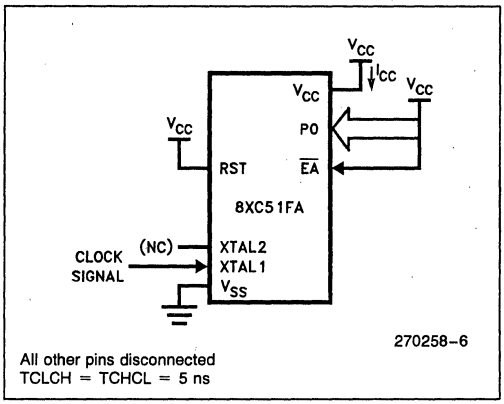


Figure 6. I_{CC} Test Condition, Active Mode

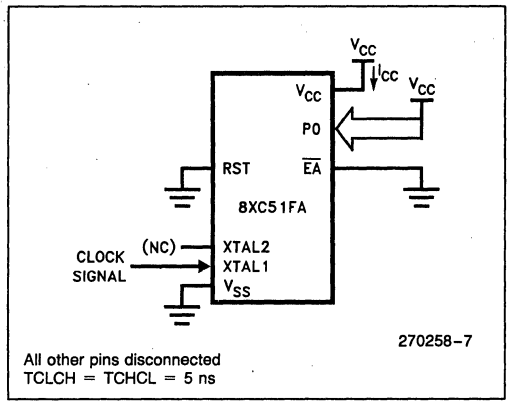


Figure 7. I_{CC} Test Condition Idle Mode

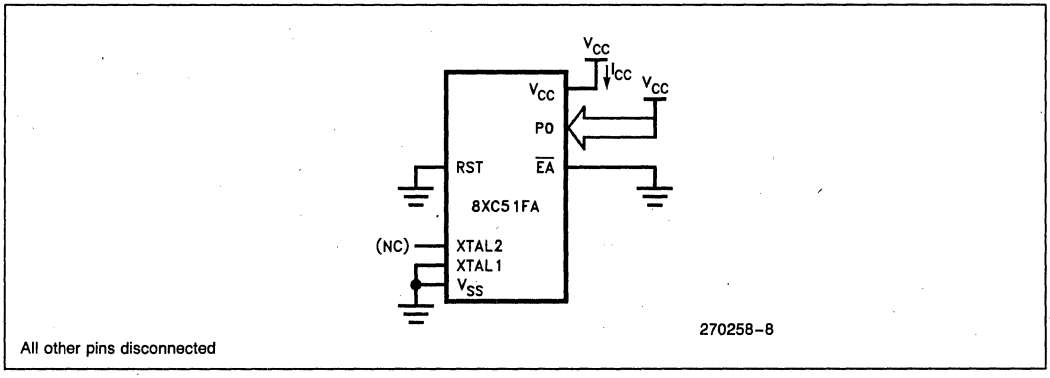


Figure 8. I_{CC} Test Condition, Power Down Mode.
V_{CC} = 2.0V to 5.5V.

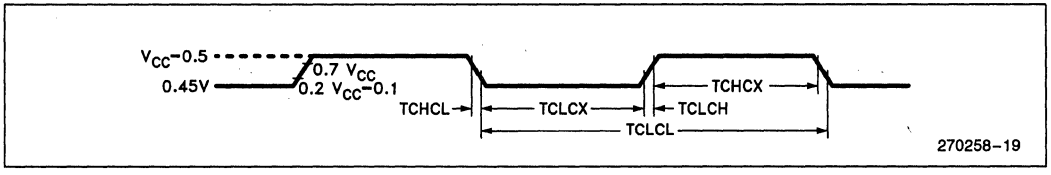


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to PSEN Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$\frac{1}{\text{TCLCL}}$	Oscillator Frequency 8XC51FA 8XC51FA-1 8XC51FA-2			 3.5 3.5 0.5	 12 16 12	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	53		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	53		TCLCL−30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		3TCLCL−105	ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{\text{PSEN}}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		312		5TCLCL−105	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		107		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns

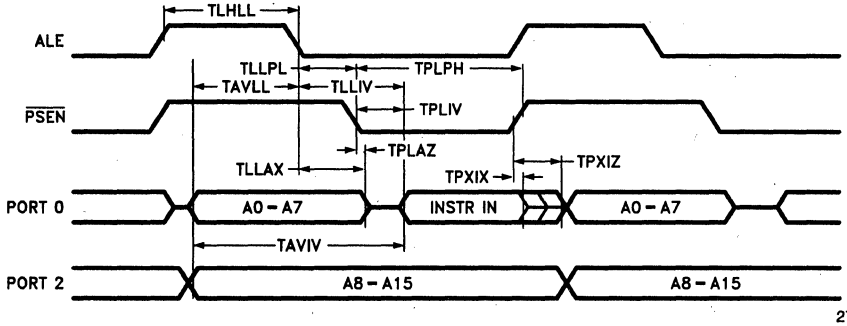
8

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF) (Continued)

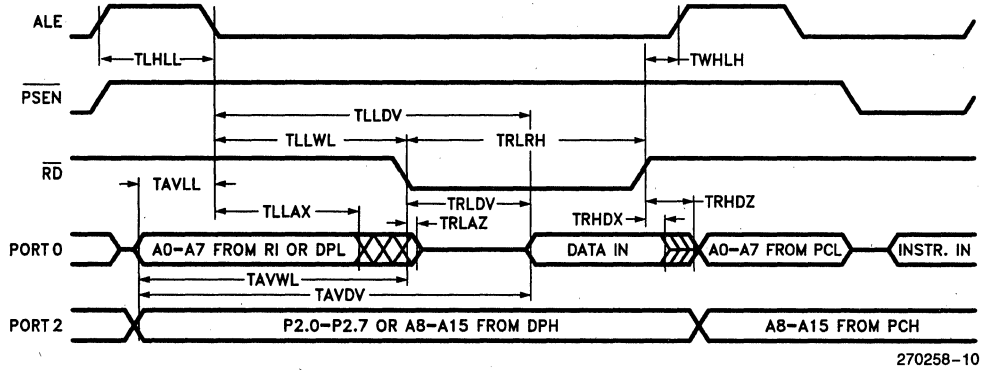
EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL−50		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL−50		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

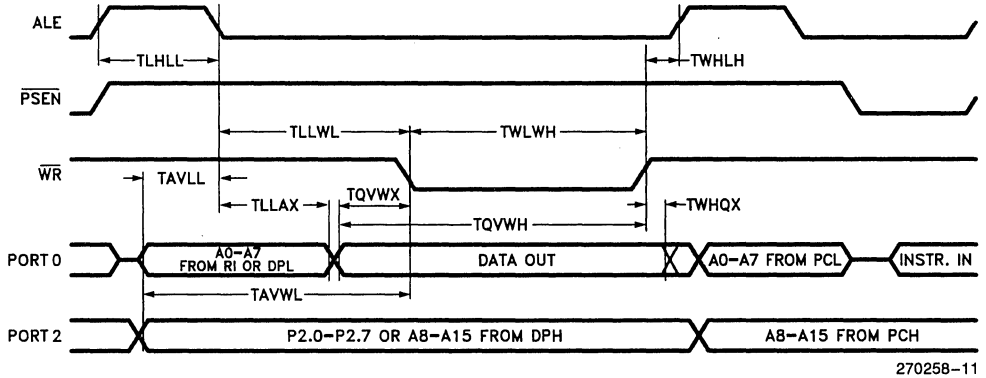
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

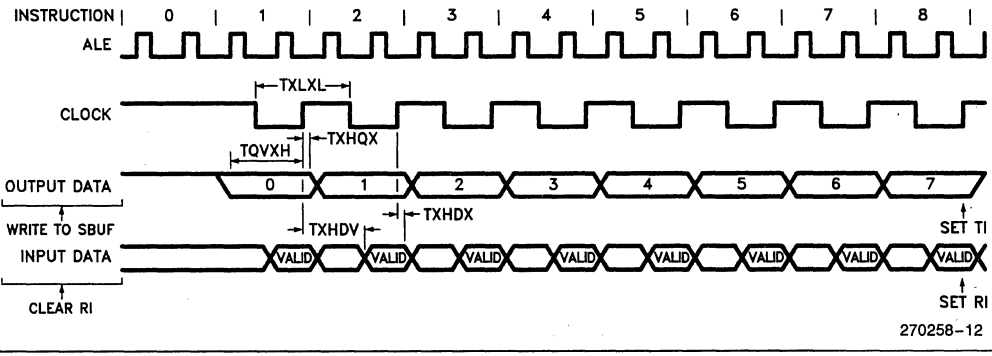


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



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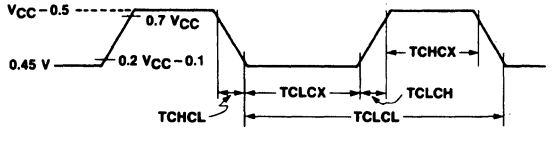
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XC51FA 8XC51FA-1 8XC51FA-2	 3.5 3.5 0.5	 12 16 12	 MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



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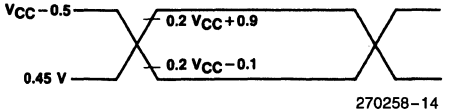
AC TESTING INPUT, OUTPUT WAVEFORMS



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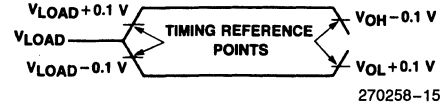
AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{OL} max for a Logic "0".

FLOAT WAVEFORMS



270258-15

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA (-L, $I_{OL}/I_{OH} = \pm 10$ mA).

PROGRAMMING THE EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal EPROM locations.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.4 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, RST $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 2. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 10.

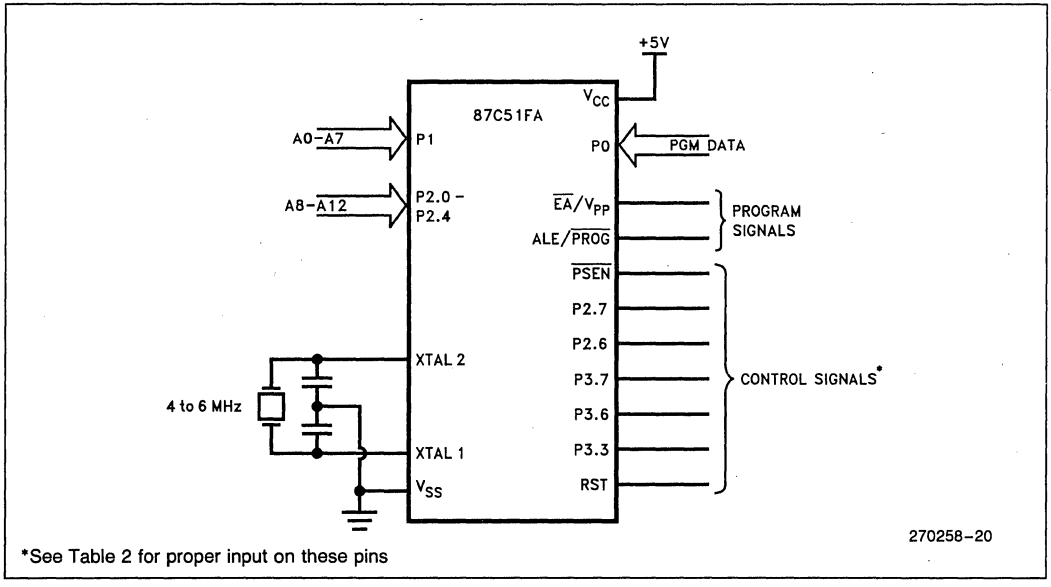
Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

NOTE:

- $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches.
- Programming specifications for the 87C51FA-L are the same as the standard 87C51FA.

Table 2. EPROM Programming Modes

Mode		RST	PSEN	ALE/PROG	EA/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



*See Table 2 for proper input on these pins

Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51FA the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse, ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C51FA.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

8

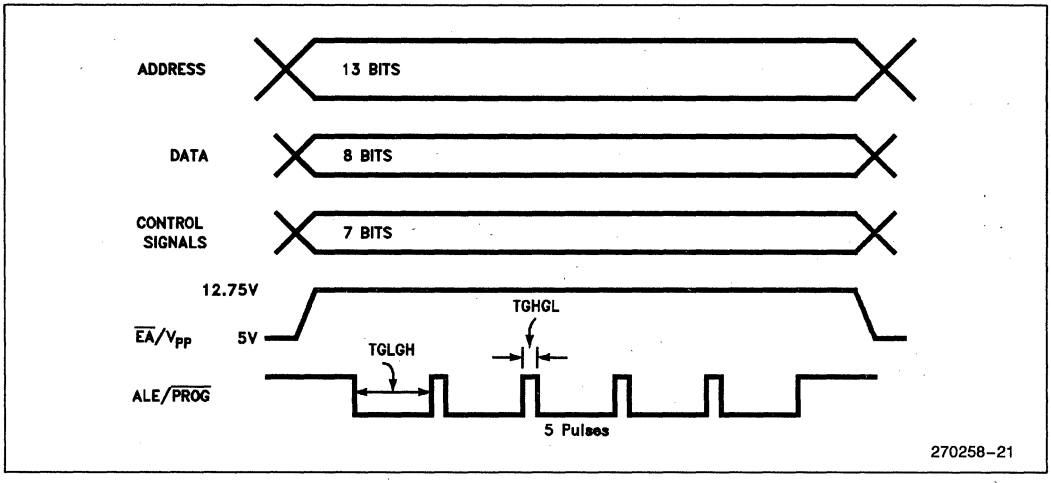


Figure 11. Programming Signals Waveforms

EPROM Lock System

The 87C51FA program lock system, when programmed, protects the onboard program against software piracy.

The 87C51FA has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 3. The 83C51FA does not have protection features.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 2 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Table 3. Program Lock Bits and the Features

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

Program Lock Bits

The 87C51FA has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 87C51FA has 3 signature bytes in locations 30H, 31H, and 60H. The 83C51FA has 2 signature bytes in locations 30H and 31H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents	
	87C51FA	83C51FA
30H	89H	89H
31H	58H	53H
60H	FAH	

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

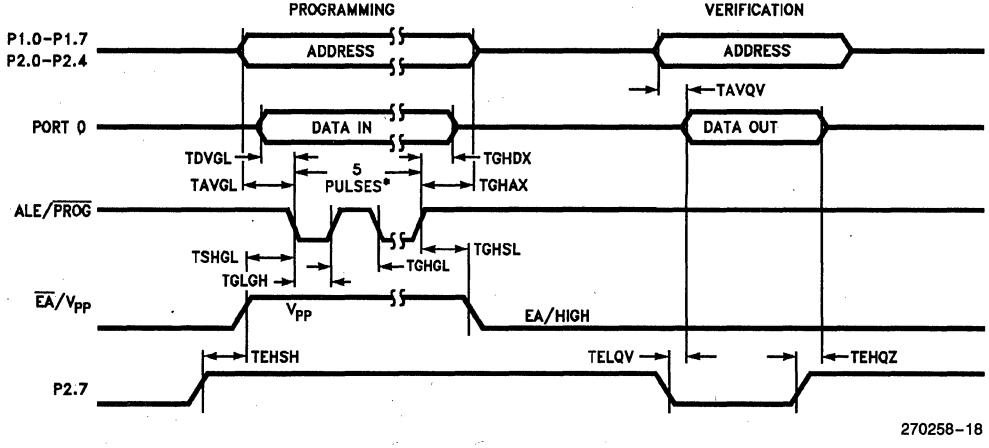
Erasure leaves the all EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 (ENABLE) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



270258-18

NOTE:
*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

DATA SHEET REVISION HISTORY

This data sheet (270258-007) is valid for devices with an "A" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (270258-007) and the previous version (270258-006):

1. The 83C51FA/80C51FA CHMOS Single-Chip 8-Bit Microcontroller data sheet (270538-004) has been combined with the 87C51FA CHMOS Single-Chip 8-Bit Microcontroller with 8 Kbytes User Programmable EPROM data sheet (270258-006) to create this new data sheet.
2. 83C51FA/80C51FA specs have been added to the Package Table and DC Characteristics Table.
3. Added 3.3V device to data sheet.
4. EPROM Programming Information has been added.
5. The Operating Temperature Range has been changed to: 0°C to +70°C.

The following differences exist between the -006 and the -005 versions of the 87C51FA data sheet.

1. "NC" pin labels changed to "Reserved" in Figure 2.
2. θ_{ja} and θ_{jc} information added to Packages table.
3. Capacitor value for ceramic resonators deleted in Figure 3.
4. Maximum Power Down current spec corrected to 75 μA from 7.5 μA.
5. Pin numbers deleted from Figure 10.
6. Absolute Maximum Ambient Temperature under Bias changed from "0°C to +70°C" to "−40°C to +85°C".
7. All references to Program Lock Bit and Encryption Array deleted from "Program Verification" section. This information is available in the hardware description.

The following differences exist between the -005 and the -004 versions of the 87C51FA data sheet:

1. Voltage tolerance changed from ±10% to ±20%.
2. Technology changed from CHMOS II-E to CHMOS III-E.
3. QFP package offering added.
4. Asynchronous port reset added.
5. ALE disable paragraph added.
6. C1, C2 guideline clarified in Figure 3.
7. Data sheet status notice and absolute maximum ratings warning reworded.
8. Operating Conditions heading added.
9. RRST changed from 40 KΩ min, 225 KΩ max to 50 KΩ min, 300 kΩ max
10. Typical values deleted for I_{IL}, I_{LI}, I_{TL} and RRST.
11. Note 1 (ALE noise pulses) reworded.
12. Figure 5 I_{CC} graph lines extended from 12 MHz to 16 MHz.
13. Various EPROM programming algorithm changes implemented:
    - — P3.3 control line added to Table 2
    - — Lock Bit 3 added to Table 2
    - — Number of programming pulses decreased from 25 to 5
    - — Figure 12 deleted
14. Number of Signature Bytes changed from 2 to 3.
15. Programming Supply Current changed from 50 mA to 75 mA Max.
16. Program Lock System changed from 2 Lock Bits to 3, and from 32 Encryption Bytes to 64.

DATA SHEET REVISION HISTORY (Continued)

The following are the key differences between the -004 and the -003 versions of the 87C51FA data sheet:

1. Included the 16 MHz device.
2. Deleted the word Maximum from the I_{OL} line of ABSOLUTE MAXIMUM RATINGS.
3. Deleted the $\overline{EA}$ from V_{IH} line of DC Table.
4. Pin capacitance now specified as Typical only.

The following are the key differences between the -003 and the -002 version of the 87C51FA data sheet:

1. Data sheet was upgraded from ADVANCE INFORMATION to PRELIMINARY.
2. The old device name (87C252) was removed from the title.
3. PLCC pin connection diagram was added.
4. Package table was added.
5. Exit from Power Down Mode was clarified.
6. Maximum I_{OL} per I/O was added to ABSOLUTE MAXIMUM RATINGS.
7. Note 4 was added to explain the maximum safe current specification.
8. I_{PD} was improved from 100 μA to 75 μA.
9. Typical DC Characteristics were added for I_{IL}, I_{LI}, I_{TL}, RRST and I_{CC}.
10. Note 5 was added to explain the test conditions for typical values.
11. Timing specifications improved for:
    TAVLL changed from TCLCL−55 to TCLCL−40
    TLLAX changed from TCLCL−35 to TCLCL−30
    TLLPL changed from TCLCL−40 to TCLCL−30
    TRHDZ changed from TCLCL−70 to TCLCL−60
    TQVWX changed from "Address Valid Before WR" to "Data Valid to WR Transition" and changed from TCLCL−60 to TCLCL−50
    TQVWH was added.
12. Data sheet revision summary was added.
13. EA Leakage current not specified.

87C51FA

EXPRESS

- **Extended Temperature Range**
- **Burn-In**
- **3.5 MHz to 12 MHz V_{CC} = 5V ±10%**

The Intel EXPRESS system offers enhancements to the operational specifications of the 8051 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.

June 1988
Order Number: 270619-001

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)		−75	μA	$V_{IN} = 0.45V$
I_{LI}	Input Leakage Current (Port 0 and $\overline{EA}$)		±15	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{TL}	Logical 1 to 0 transition Current (Ports 1, 2, 3)		−750	μA	$V_{IN} = 2.0V$
I_{CC}	Power Supply Current				(Note 1)
	Active Mode		35	mA	
	Idle Mode		7.5	mA	
	Power Down Mode		150	μA	

NOTE:
1. V_{CC} = 4.5V–5.5V, Frequency Range = 3.5 MHz–12 MHz.

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range(2)	Burn-In(3)
P	Plastic	Commercial	No
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD	Cerdip	Extended	No
TN	PLCC	Extended	No
LP	Plastic	Extended	Yes
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

NOTES:
2. Commercial temperature range is 0°C to +70°C. Extended temperature range is −40°C to +85°C.
3. Burn-in is dynamic for a minimum time of 168 hours at +125°C, V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples:

P87C51FA indicates 87C51FA in a plastic package and specified for commercial temperature range, without burn-in.
LD87C51FA indicates 87C51FA in a cerdip package and specified for extended temperature range with burn-in.

intel

87C51FA-20/-3
COMMERCIAL/EXPRESS
20 MHz CHMOS MICROCONTROLLER

87C51FA-20—3.5 MHz to 20 MHz, V_{CC} = 5V ±20%
87C51FA-3—24 MHz Internal Operation, V_{CC} = 5V ±20%

- High Performance CHMOS EPROM
- 24 MHz Internal Operation (-3 only)
- Power Control Modes
- Three 16-Bit Timer/Counters
- Programmable Counter Array with:
  - — High Speed Output,
  - — Compare/Capture,
  - — Pulse Width Modulator,
  - — Watchdog Timer Capabilities
- Up/Down Timer/Counter
- Three Level Program Lock System
- 8K On-Chip EPROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 7 Interrupt Sources
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- TTL Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside in the on-chip EPROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C51FA-20 is a single-chip control oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS®-51 family, the 87C51FA-20 uses the same powerful instruction set, has the same architecture, and is pin for pin compatible with the existing MCS-51 products. The 87C51FA-20 is an enhanced version of the 87C51. It's added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

The 87C51FA-3 has the same 3.5 MHz to 20 MHz frequency range as the 87C51FA-20 when operating out of external program/data memory. When running out of internal program/data memory, the 87C51FA-3 can operate up to 24 MHz.

Throughout this document 87C51FA-20 will refer to both the 87C51FA-20 and the 87C51FA-3.

September 1992
Order Number: 272081-002

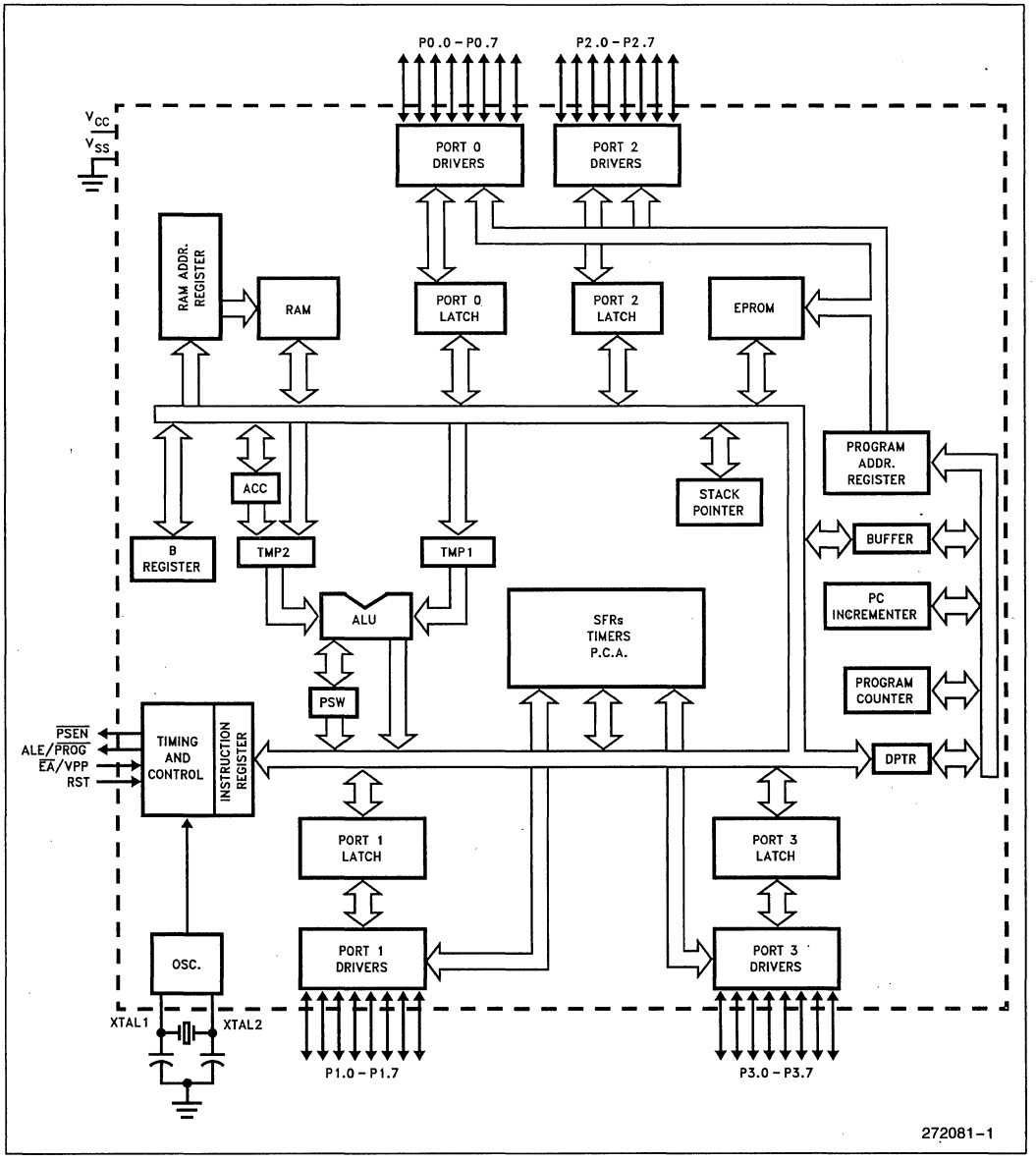


Figure 1. 87C51FA-20 Block Diagram

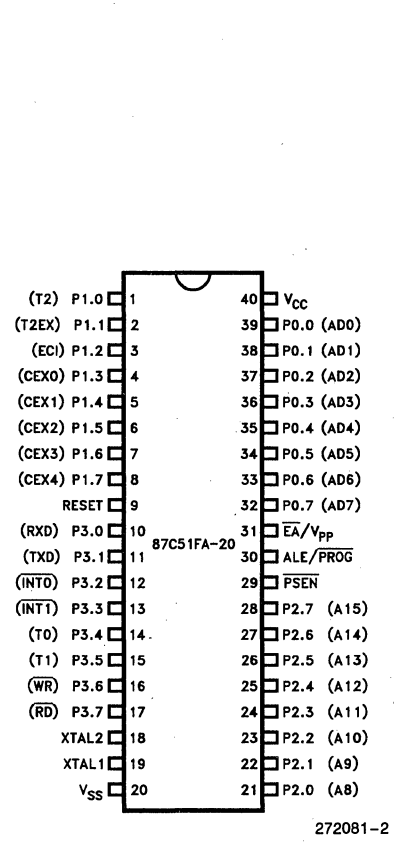
PROCESS INFORMATION

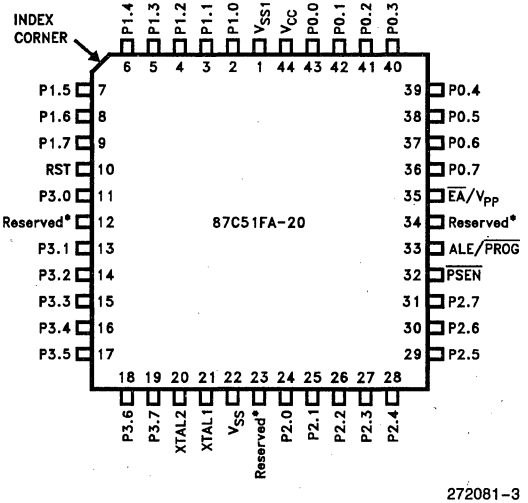
This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

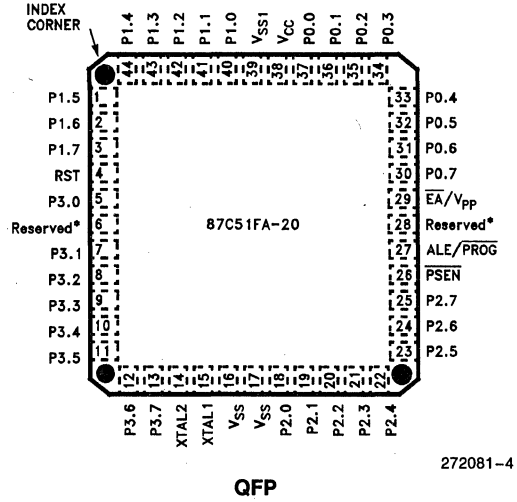
PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
87C51FA-20	P	40-Pin Plastic DIP (OTP)	45°C/W	16°C/W
	D	40-Pin CERDIP (EPROM)	45°C/W	15°C/W
	N	44-Pin PLCC (OTP)	46°C/W	16°C/W
	S	44-Pin QFP (OTP)	97°C/W	24°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.







*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Circuit ground.
V_{SS1}	Secondary ground (connection not necessary). Provided to reduce ground bounce and improve power supply bypassing. **NOTE:** This pin is not a substitute for the V_{SS} pin. Connect V_{SS} and V_{SS1} with the lowest impedance path possible.
Port 0	8-bit, open drain, bidirectional I/O port. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during verification. When used as an I/O port, pullups to V_{CC} may be needed.
Port 1	8-bit bidirectional I/O port. All of the port 1 pins are shared with other functions in the 87C51FA-20. Port 1 is also used as the low-order address byte input during EPROM programming.
Port 2	8-bit bidirectional I/O port. Port 2 also emits the high-order address byte during accesses to 16-bit external memory locations. Some of the Port 2 pins are also used as address bits for EPROM programming.
Port 3	8-bit bidirectional I/O port. All of the port 3 pins are shared with other functions in the 87C51FA-20. Two of the pins are used as control lines ($\overline{RD}$, $\overline{WR}$) for accessing external RAM.
RESET	Reset input to the chip. A high Input for a minimum of two machine cycles with the oscillator running resets the device. The port pins will be reset when a voltage above V_{IH} is applied whether the oscillator is running or not. RST has an internal pulldown.
ALE/$\overline{PROG}$	Address Latch Enable. Provides a signal to demultiplex the address from the address/data bus. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode. This pin is also the program pulse input during EPROM programming.
$\overline{PSEN}$	Program Store Enable. Acts as read strobe for external program memory fetches.
$\overline{EA}$/V_{PP}	External Access Enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external program memory locations 0000H to 0FFFFH. $\overline{EA}$ should be strapped to V_{CC} for internal program executions. If any of the lock bits are programmed, $\overline{EA}$ will be internally latched on reset. This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	Input to the inverting oscillator amplifier.
XTAL2	Output from the inverting oscillator amplifier.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Express	 0 −40	 +70 +85	 °C °C
V_{CC}	Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency	3.5	20	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typical (Note 4)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Note 5) (Ports 1, 2 and 3)			0.3 0.45 1.0	V	I_{OL} = 100 μA I_{OL} = 1.6 mA (Note 1) I_{OL} = 3.5 mA
V_{OL1}	Output Low Voltage (Note 5) (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)			0.3 0.45 1.0	V	I_{OL} = 200 μA I_{OL} = 3.2 mA (Note 1) I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Ports 1, 2 and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −10 μA I_{OH} = −30 μA (Note 2) I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External bus Mode)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA (Note 2) I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3) Commercial Express			 −50 −75	 μA	 V_{IN} = 2.0V
I_{LI}	Input Leakage Current (Port 0) Commercial Express			 ±10 ±15	 μA	 V_{IN} = V_{IL} or V_{IH}

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

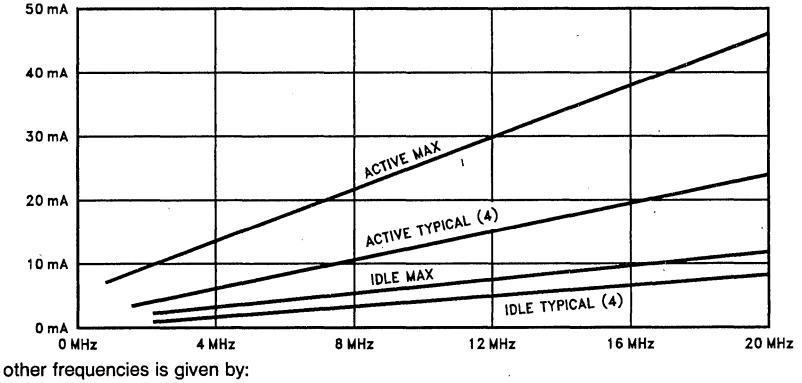
All parameter values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typical (Note 4)	Max	Units	Test Conditions
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)					
	Commercial			−650	μA	V_{IN} = 2.0V
	Express			−750		
RRST	RST Pulldown Resistor	50		300	KΩ	
CIO	Pin Capacitance		10		pF	@1MHz, 25°C
I_{CC}	Power Supply Current Active Mode					
	Commercial		24	47.1	mA	
	Express			55	mA	(Note 3)
	Idle Mode		8	11.4	mA	
	Power Down Mode		5	75	μA	

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitance loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 4–7 for test conditions. Minimum V_{CC} for power down is 2V.
4. Typicals are based on limited number of samples, and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port -
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:

Active Mode

I_{CC} Max = 2.2 × FREQ + 3.14

Idle Mode

I_{CC} Max = 0.49 × FREQ + 1.6

Where Osc Freq is in MHz, I_{CC} is in mA

Figure 3. I_{CC} vs Frequency

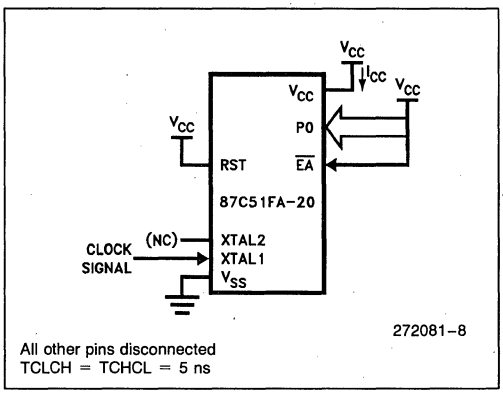


Figure 4. I_{CC} Test Condition, Active Mode

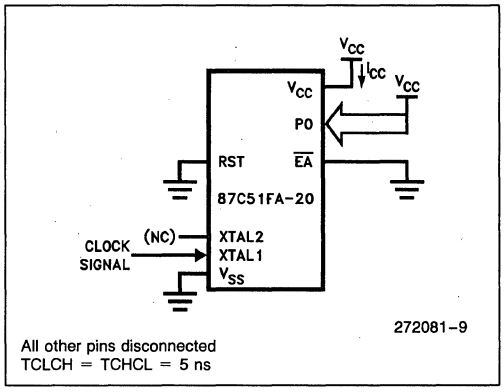


Figure 5. I_{CC} Test Condition Idle Mode

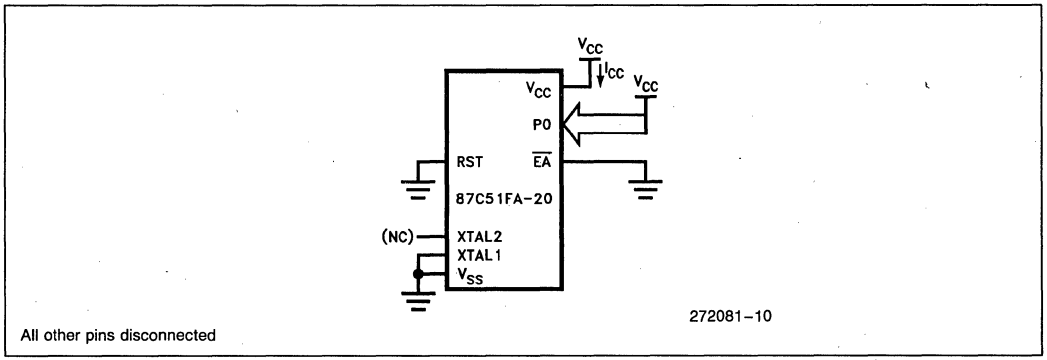


Figure 6. I_{CC} Test Condition, Power Down Mode.
V_{CC} = 2.0V to 5.5V.

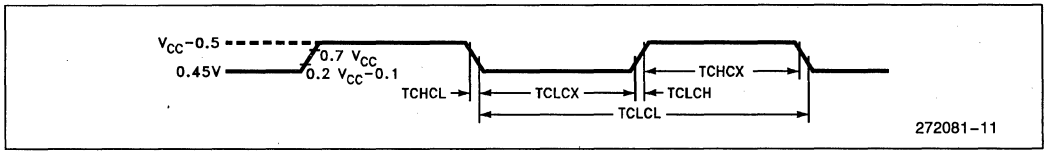


Figure 7. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to PSEN Low

AC CHARACTERISTICS: (Under Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$\frac{1}{\text{TCLCL}}$	Oscillator Frequency 87C51FA-20			3.5	20	MHz
TLHLL	ALE Pulse Width	60		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	10		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	20		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		125		4TCLCL−75	ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	20		TCLCL−30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	105		3TCLCL−45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In		60		3TCLCL−90	ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{\text{PSEN}}$		30		TCLCL−20	ns
TAVIV	Address to Valid Instruction In		145		5TCLCL−105	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	200		6TCLCL−100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	200		6TCLCL−100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		155		5TCLCL−95	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		40		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		310		8TCLCL−90	ns
TAVDV	Address to Valid Data In		360		9TCLCL−90	ns

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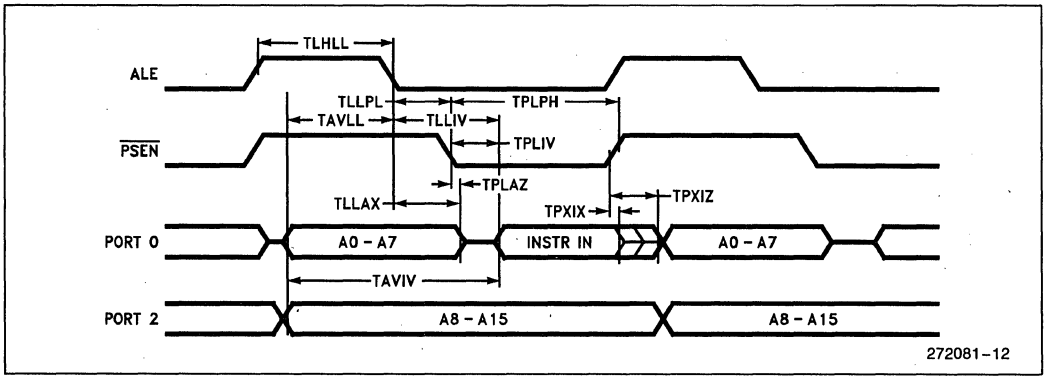
AC CHARACTERISTICS: (Under Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF) (Continued)

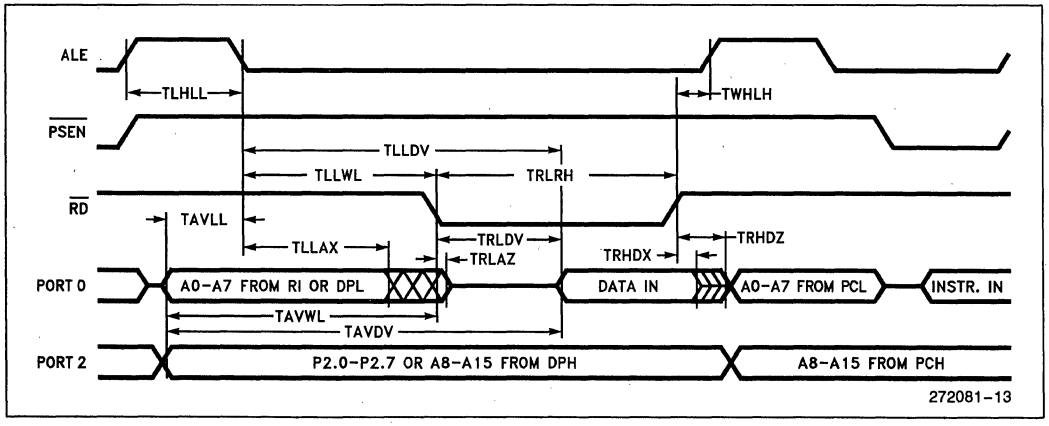
EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	100	200	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	110		4TCLCL−90		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	15		TCLCL−35		ns
TWHQX	Data Hold after $\overline{WR}$	10		TCLCL−40		ns
TQVWH	Data Valid to $\overline{WR}$ High	280		7TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	10	123	TCLCL−40	TCLCL+40	ns

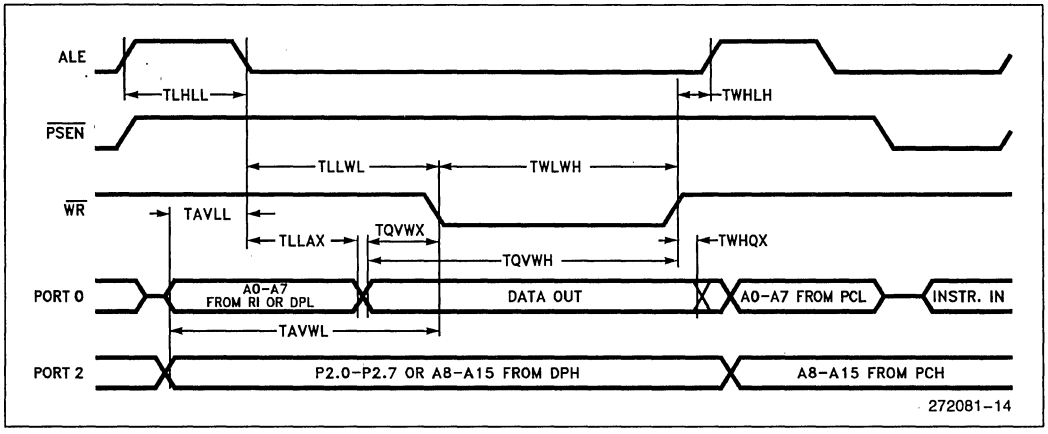
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

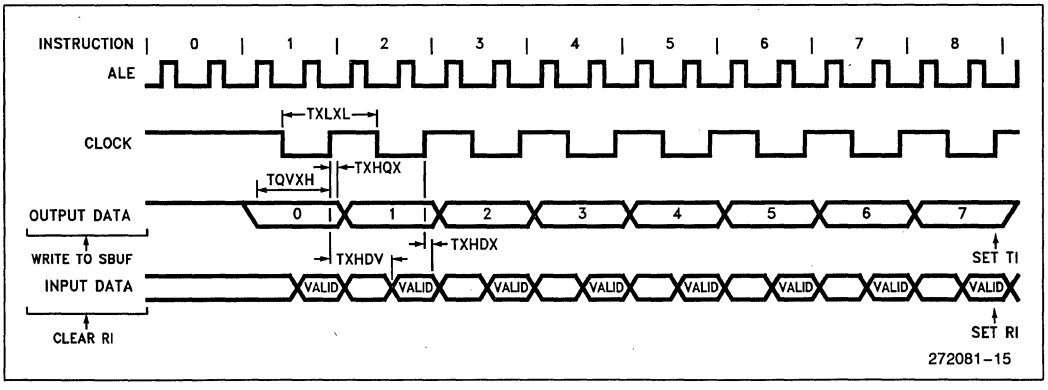


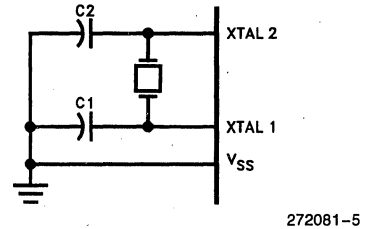
SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	600		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	367		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		367		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS





C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators contact resonator manufacturer.

Figure 8. Oscillator Connections

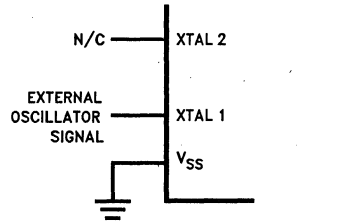
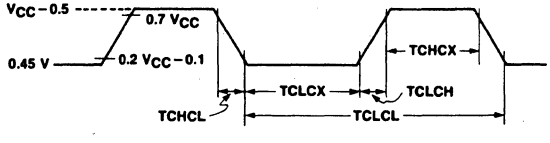


Figure 9. External Clock Drive Configuration

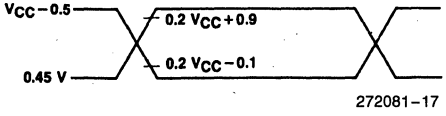
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM

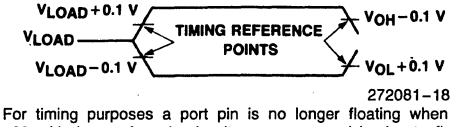


AC TESTING INPUT, OUTPUT WAVEFORMS



AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{OL} max for a Logic "0".

FLOAT WAVEFORMS

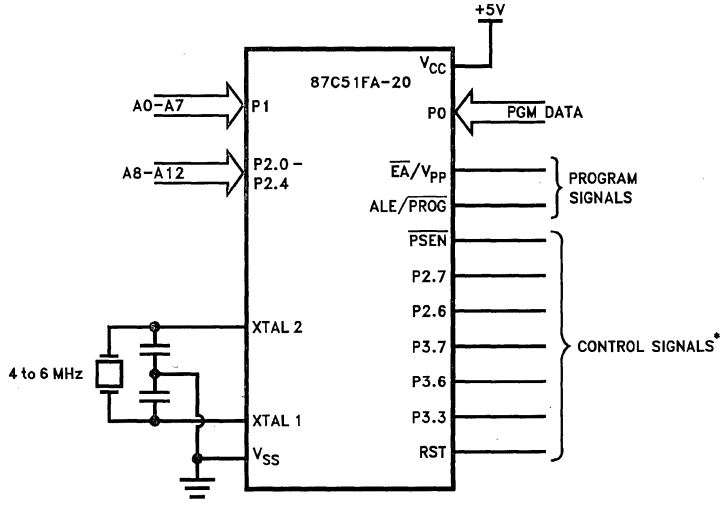


For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

EPROM CHARACTERISTICS

Table 1. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



*See Table 1 for proper input on these pins

Figure 10. EPROM Programming Configuration

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PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51FA-20 the following sequence must be exercised.

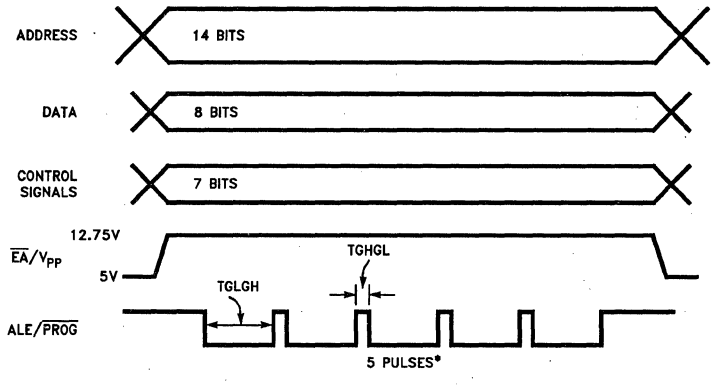
1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse, ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte that is programmed, or after a block of bytes that is programmed. In either case a complete verify of the entire array that has been programmed will ensure a reliable programming of the 87C51FA-20.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.



*5 pulses for EPROM array, 25 pulses for encryption table and lock bits.

Figure 11. Programming Waveforms

Signature Bytes

Location	Contents	Description
30H	89H	Indicates Intel Devices
31H	58H	Indicates FX-Core Product
60H	FAH	Indicates 87C51FA Device

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

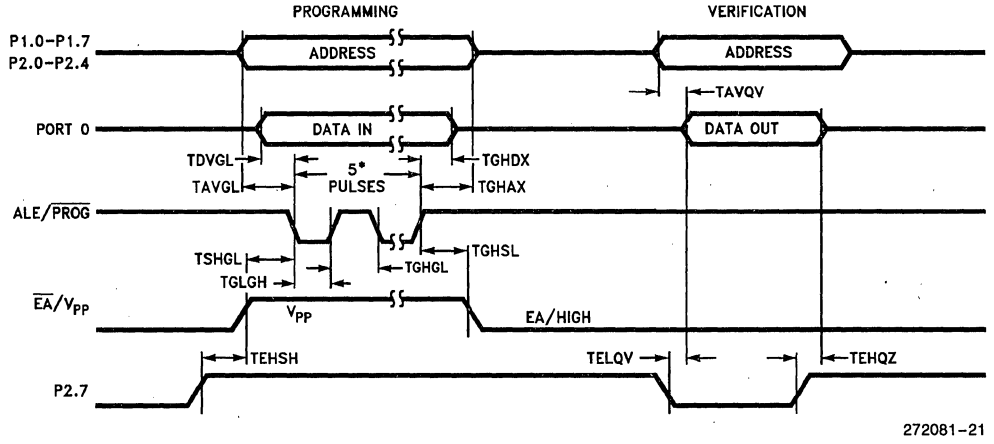
Erasure leaves the all EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 (ENABLE) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*5 pulses for EPROM array, 25 pulses for encryption table and lock bits.

DESIGN CONSIDERATION

- When running out of internal program/data memory, the 87C51FA-3 can be operated using a 24 MHz clock. If the 87C51FA-3 is running out of external program/data memory, the operating frequency must be between 3.5 MHz to 20 MHz. The 87C51FA-3 will not function properly at 24 MHz when running out of external program/data memory.
- Ambient light is known to affect the internal RAM contents during operation. If the 87C51FA-20 application requires the part to be run under ambient lighting, an opaque label should be placed over the window to exclude light.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- The Timer 2 clock out frequency on the 8XC51FA-20 is determined by the equation in the 8XC51FX Hardware Description as shown below:

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

Even though the equation permits a clock-out frequency of 5 MHz with a 20 MHz oscillator, **the maximum output frequency is 4 MHz**. When operating the device above 16 MHz, RCAP2L must be limited to FEH.

DATA SHEET REVISION HISTORY

This data sheet (272081-002) is valid for devices with an "A" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (272081-002) and the previous version (272081-001):

1. Added 87C51FA-3 to 20 MHz data sheet.
2. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	120	125
	4TCLCL−80	4TCLCL−75
TPLIV	3TCLCL−95	3TCLCL−90
TWHQX	0	10
	TCLCL−50	TCLCL−40
TQVWH	200	280
	7TCLCL−150	7TCLCL−70

The following differences exist between revision 1 of the 87C51FA-20 (272081-001) data sheet and the 87C51FA (270258-005) data sheet.

1. All explanatory wording duplicated in the device user's guide was deleted.
2. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	4TCLCL−100	4TCLCL−80
TPLIV	3TCLCL−105	3TCLCL−95
TPXIZ	TCLCL−25	TCLCL−20
TRLDV	5TCLCL−165	5TCLCL−95
TLLDV	8TCLCL−150	8TCLCL−90
TAVDV	9TCLCL−165	9TCLCL−90
TAVWL	4TCLCL−130	4TCLCL−90
TQVWX	TCLCL−50	TCLCL−35

3. TXHQX in the Serial Port Timing Table changed from (2TCLCL − 117) to (2TCLCL − 50).
4. All references to Program Lock Bit and Encryption Array deleted from "Program Verification" section. This information is available in the hardware description.

87C51FB/83C51FB
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 16 KBYTES INTERNAL PROGRAM MEMORY

87C51FB/83C51FB—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C51FB-1/83C51FB-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%
87C51FB-L/83C51FB-L—3.5 MHz to 8 MHz, V_{CC} = 3.3V ±0.3V

- High Performance CHMOS EPROM
- Low Voltage Operation (-L Only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Programmable Counter Array with:
  - — High Speed Output,
  - — Compare/Capture,
  - — Pulse Width Modulator,
  - — Watchdog Timer capabilities
- Up/Down Timer/Counter
- Three Level Program Lock System
- 16K On-Chip EPROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 7 Interrupt Sources
- Four Level Interrupt Priority
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Fully Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 16 Kbytes of the program memory can reside in the on-chip EPROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C51FB/83C51FB is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 87C51FB/83C51FB uses the same powerful instruction set, has the same architecture, and is pin for pin compatible with the existing MCS-51 family of products. The 87C51FB/83C51FB is an enhanced version of the 87C51/80C51BH. It's added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

Applications that require low voltage operation can use the 87C51FB-L/83C51FB-L. The 8XC51FB-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz.

Throughout this document 8XC51FB will refer to both the 83C51FB and the 87C51FB.

October 1992
Order Number: 270563-005

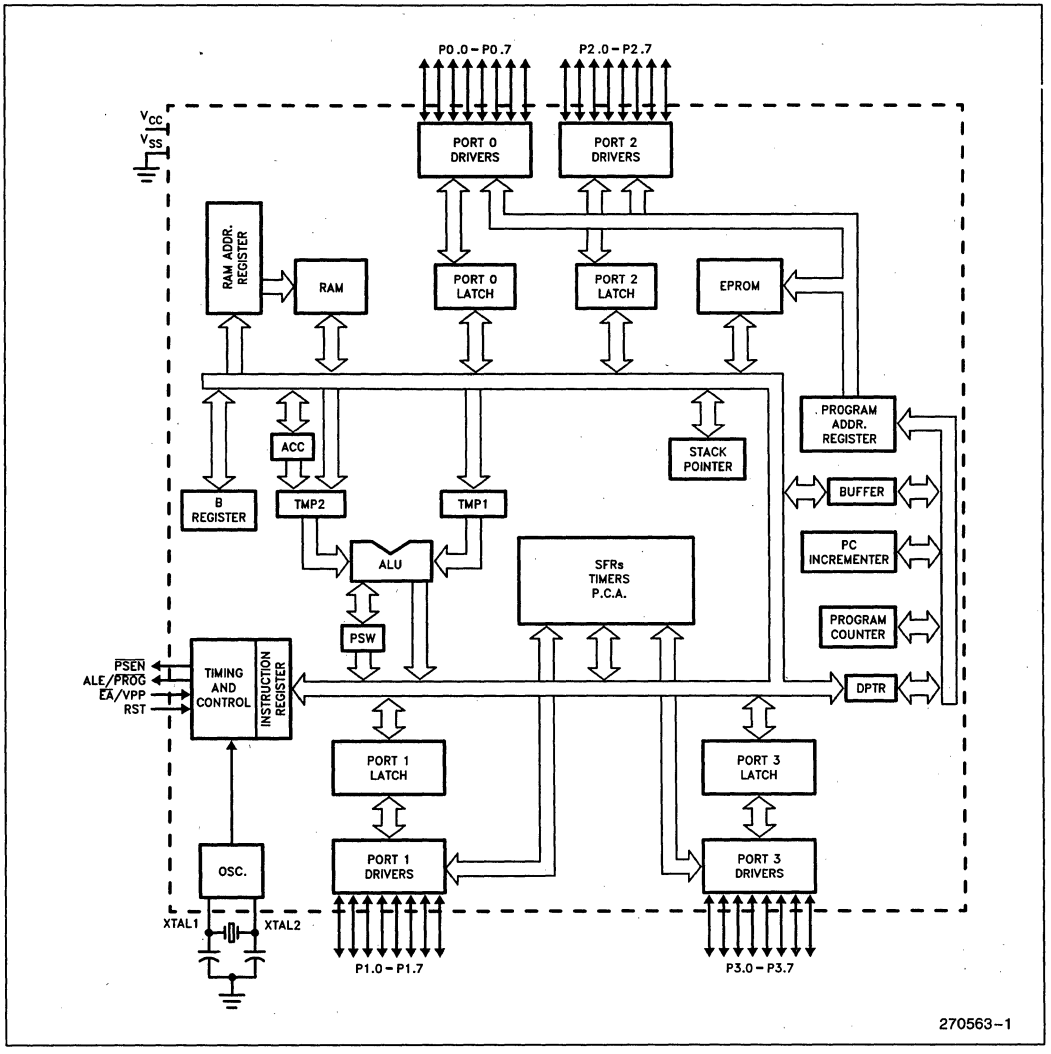


Figure 1. 8XC51FB Block Diagram

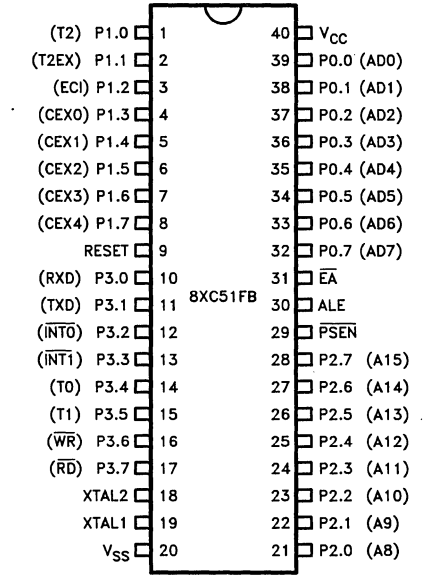
PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components and Reliability Handbook*, Order Number 210997.

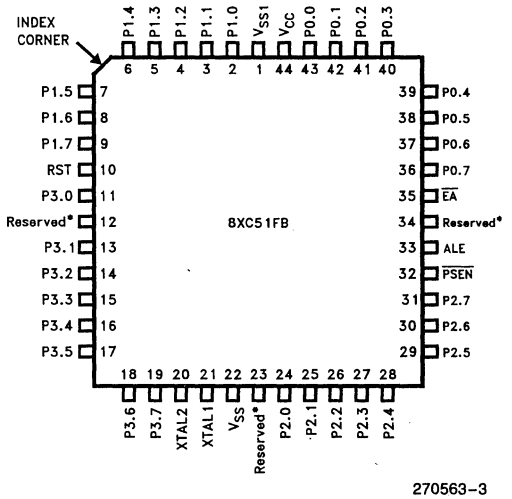
PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC51FB	P	40-Pin Plastic DIP	45°C/W	16°C/W
87C51FB	D	40-Pin CERDIP	45°C/W	15°C/W
8XC51FB	N	44-Pin PLCC	46°C/W	16°C/W
8XC51FB	S	44-Pin QFP	96°C/W	24°C/W

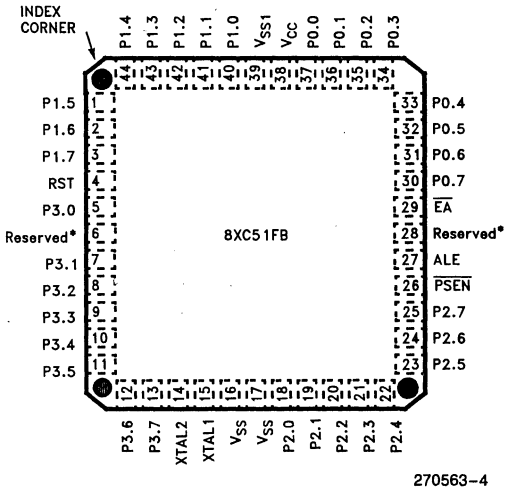
All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



DIP



PLCC



QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin. Connect V_{SS} and V_{SS1} with the lowest impedance path possible.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC51FB:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The Port Pins will be driven to their reset condition when a voltage above V_{IH1} is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51FB.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX instruction. Otherwise the pin is weakly pulled high.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51FB is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

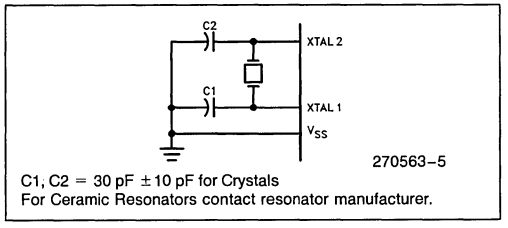
XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but the minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators contact resonator manufacturer.

Figure 3. Oscillator Connections

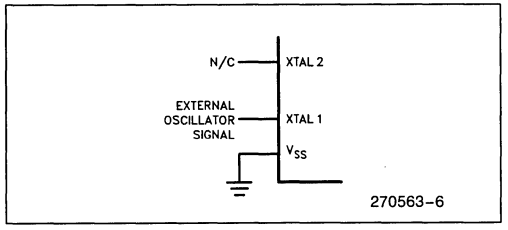


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51FB either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level. The external interrupt or Reset signal must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- The 8CX51FB-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz. Operating beyond these specifications could cause improper device functionality. (To program the 87C51FB-L, follow the same procedure as the 87C51FB.)
- The window on the 87C51FB must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC51FB without the 8XC51FB having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51FB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} . . . . . 0V to +13.0V
Voltage on Any Other Pin to V_{SS} . . −0.5V to +6.5V
I_{OL} Per I/O Pin . . . . . 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This is a production data sheet. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions:

T_A (under Bias) = 0°C to +70°C, V_{CC} = 5V ±20%, V_{SS} = 0V (8XC51FB-L, V_{CC} = 3.3V ±0.3V)

DC CHARACTERISTICS: (Over Operating Conditions)

All parameter values apply to both 5V and 3.3V devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage (Note 5) (Ports 1, 2, and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage (Note 5) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2, and 3, ALE, $\overline{PSEN}$)	V_{CC}−0.3			V	I_{OH} = −10 μA
		V_{CC}−0.7			V	I_{OH} = −30 μA
		V_{CC}−1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC}−0.3			V	I_{OH} = −200 μA
		V_{CC}−0.7			V	I_{OH} = −3.2 mA
		V_{CC}−1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)			±10	μA	0.45V < V_{IN} < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3)			−650	μA	V_{IN} = 2V
RRST	RST Pulldown Resistor	50		300	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current:					(Note 3)
	Active Mode					
	8XC51FB-L at 8 MHz			12	mA	
	All Others at 12 MHz (Figure 5)		20	40	mA	
	Idle Mode at 12 MHz (Figure 5)		5	10	mA	
	Power Down Mode		15	100	μA	

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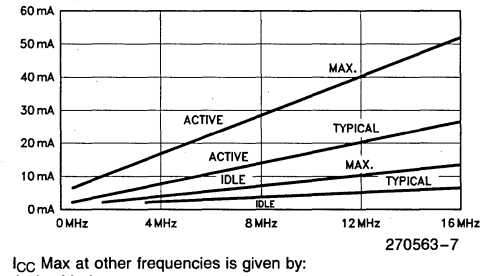
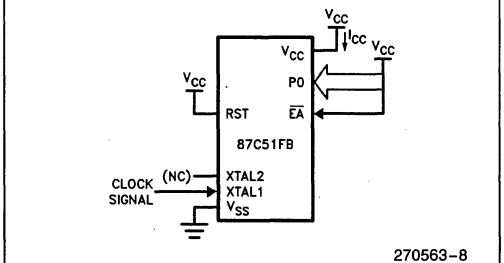
NOTES:
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with Schmitt triggers or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



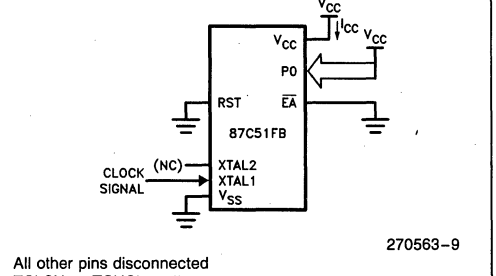
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 5. I_{CC} vs Frequency



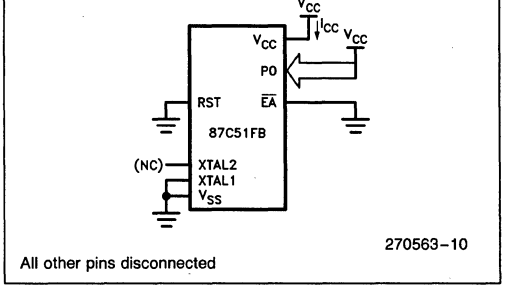
All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition Idle Mode



All other pins disconnected

Figure 8. I_{CC} Test Condition, Power Down Mode V_{CC} = 2.0V to 6.0V

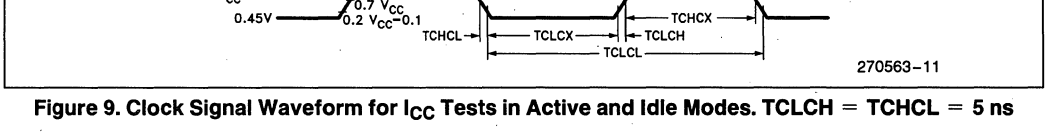


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and $\overline{\text{PSEN}}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	53		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	53		TCLCL−30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		3TCLCL−105	ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{\text{PSEN}}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		312		5TCLCL−105	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
TRLRH	$\overline{\text{RD}}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{\text{RD}}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float After $\overline{\text{RD}}$		107		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{\text{WR}}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid before $\overline{\text{WR}}$	33		TCLCL−50		ns
TWHQX	Data Hold after $\overline{\text{WR}}$	33		TCLCL−50		ns
TQVWH	Data Valid to $\overline{\text{WR}}$ High	433		7TCLCL−150		ns
TRLAZ	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

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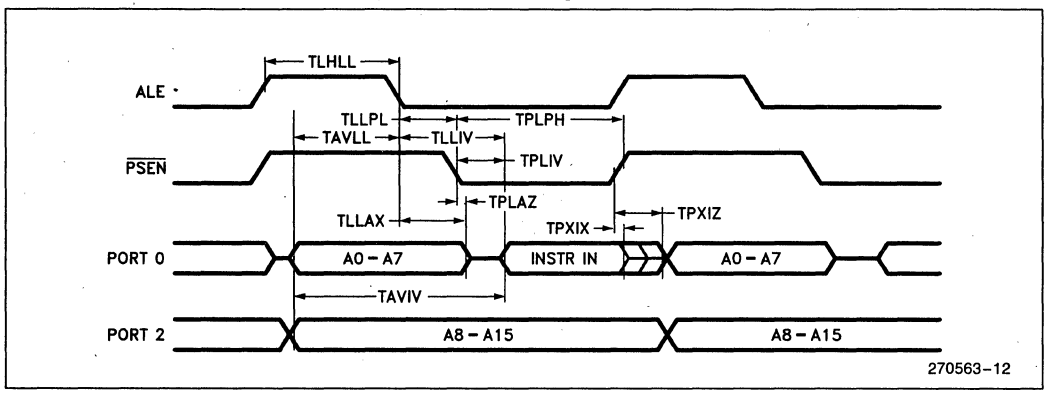
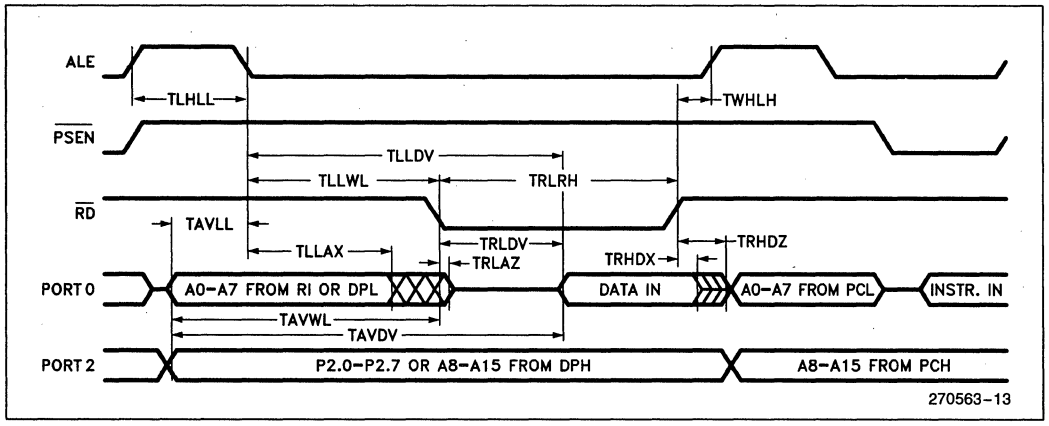
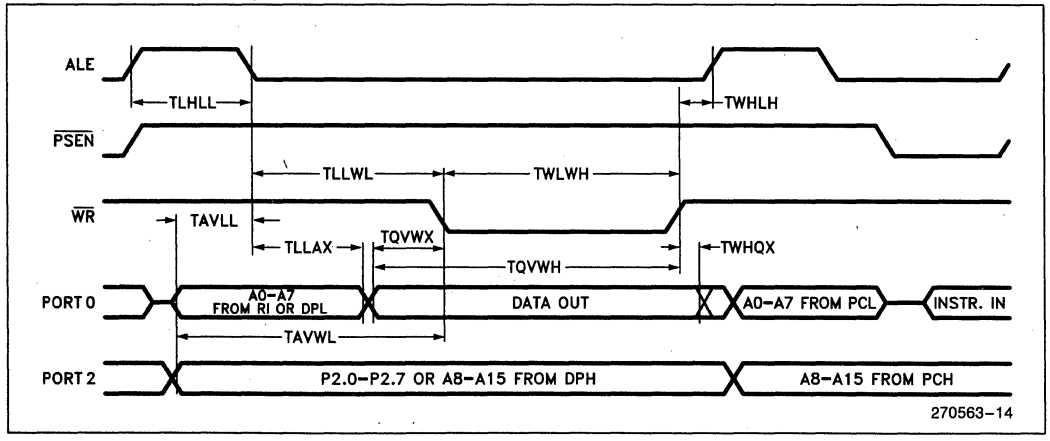
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

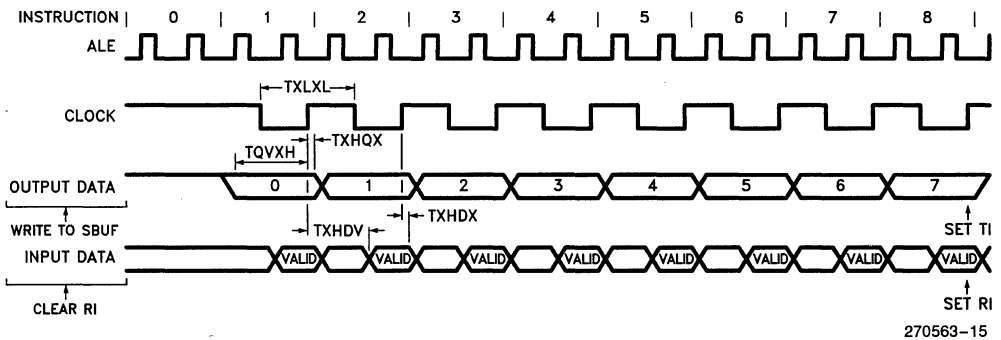


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

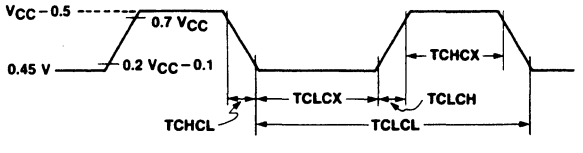
SHIFT REGISTER MODE TIMING WAVEFORMS



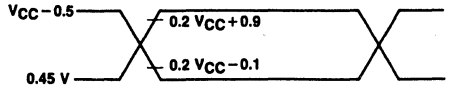
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XC51FB 8XC51FB-1	 3.5 3.5	 12 16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



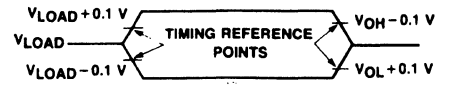
AC TESTING INPUT, OUTPUT WAVEFORMS



270563-17

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



270563-18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA. (-L, $I_{OL}/I_{OH} = \pm 10$ mA.)

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:

- Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.
- Programming specifications for the 87C51FB-L are the same as the standard 87C51FB.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, respectively for A0–A13.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

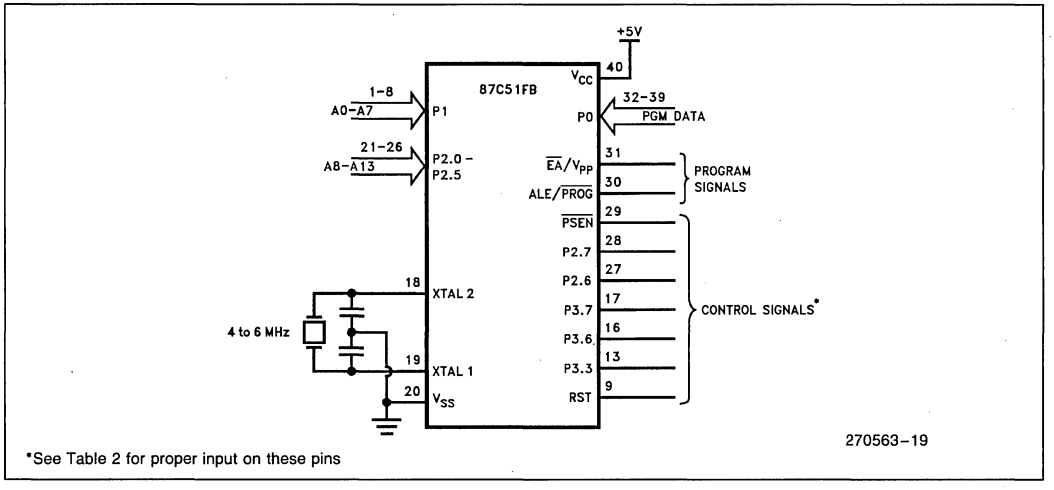


Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51FB the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V $\pm$0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Verification may be done after programming either one byte or a block of bytes. A complete verify of the array will ensure reliable programming of the 87C51FB.

The lock bits cannot be directly verified. They are verified by observing that their features are enabled. Refer to the EPROM Program Lock section in this data sheet for a description of the lock bit features.

ROM and EPROM Lock System

The 87C51FB and the 83C51FB program lock systems, when programmed, protect the onboard program against software piracy.

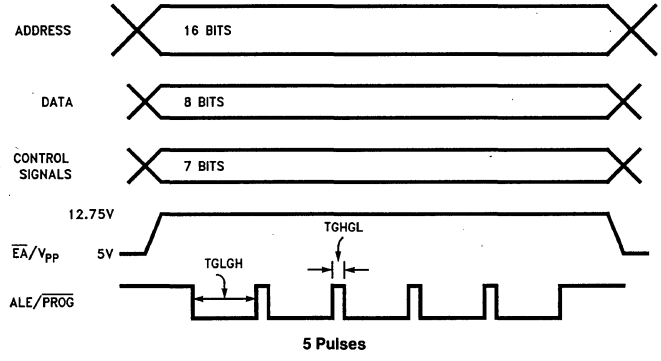


Figure 11. Programming Signal's Waveforms

The 83C51FB has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 3. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C51FB has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 3.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in it's original, unmodified form. For programming the Encryption Array, refer to Table 2 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verification of the byte will produce the encryption byte value. If a large block (> 64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason it is strongly recommended that all unused code bytes be programmed with some value other than 0FFH, and not all of them the same value. This practice will ensure the maximum possible program protection for this feature.

Program Lock Bits

The 87C51FB has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 8XC51FB has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents	
	87C51FB	83C51FB
30H	89H	89H
31H	58H	58H
60H	FBH	FBH/7BH

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-

Table 3. Program Lock Bits and the Features

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

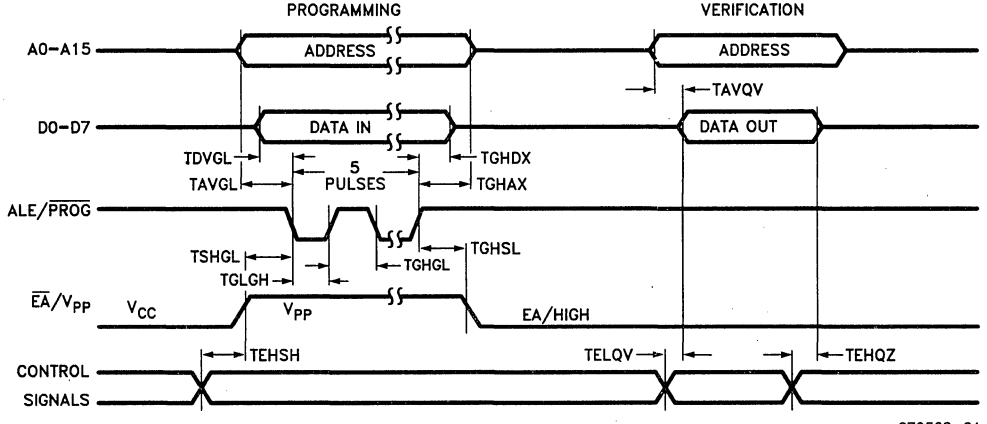
Erasure leaves all the EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



DATA SHEET REVISION HISTORY

This data sheet (270563-005) is valid for devices with an "A" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (270563-005) and the previous version (270563-004):

1. Added 3.3V device to data sheet.
2. Data sheet title was changed from:
   87C51FB/83C51FB CHMOS Single-Chip 8-Bit Microcontroller 16 Kbytes User Programmable EPROM
   to:
   87C51FB/83C51FB CHMOS Single-Chip 8-Bit Microcontroller with 16 Kbytes Internal Program Memory
3. Data sheet status changed from "Preliminary" to "Production".
4. Added process information after block diagram.
5. θ_{ja} and θ_{jc} information added to Packages table.
6. Signature byte location 60H, 83C51FB changed to FBH/7BH.

The following differences exist between the -004 and -003 versions of this data sheet.

1. Name changed from 87C51FB to 87C51FB/83C51FB.
2. Data sheet status changed from "ADVANCE" to "PRELIMINARY".
3. Device -2 version deleted.
4. 4 Level Interrupt Priority added.
5. QFP package offering added.
6. V_{SS1} pin description added.
7. Asynchronous Reset added.
8. ALE disable added.
9. RRST spec changed from 40 KΩ min, 225 KΩ max to 50 KΩ min, 300 KΩ max.
10. Note 1 reworded (ALE noise pulses).
11. Control line (P3.3) added to Table 2 and Figure 10.
12. Programming Algorithm and verification paragraphs reworded to describe programming changes.
13. Figure 11 changed to show 5 programming pulses rather than 25.
14. Figure 12 deleted (Program Verification).
15. Program Memory Lock feature changes:
    — Third lock bit added
    — Encryption array enhanced to 64 bytes
16. Third signature byte added; location and definition included.
17. I_{PP} programming spec changed from 50 mA to 75 mA.

The following are the key differences between the -003 and -002 version of the 87C51FB data sheet:

1. Word "Maximum" was deleted from the I_{OL} line in the Absolute Maximum Ratings.
2. Parameter V_{IL1} was deleted from the DC Characteristics.
3. Note 4, "Care must be taken not to exceed the maximum allowable power dissipation" was deleted from DC Characteristics and from the list of notes and notes were resequenced.
4. Parameter I_{LI1} was deleted from the DC Characteristics.
5. Figure 5 was replaced to show correct I_{CC} curves.
6. External clock capacitive loading note was added.

The following are the differences between the -002 and -001 version of the 87C51FB data sheet:

1. Title changed to include -1 and -2 version of the device.
2. PLCC pin connection diagram was added.
3. Package table was added.
4. Exit from power down mode was clarified.
5. Maximum I_{OL} per I/O pin was added to the Absolute Maximum Ratings.
6. Note 6 was added to explain the maximum safe current specification.
7. Typical values for I_{CC} table were added.
8. Note 5 was added to explain the test conditions for typical values.
9. Timing specifications improved for:
   TLLAX changed from TCLCL − 35 to TCLCL − 30
   TLLPL changed from TCLCL − 40 to TCLCL − 30
   TRHDZ changed from TCLCL − 70 to TCLCL − 60
   TQVWX changed from TCLCL − 60 to TCLCL − 50
   TQVWH was added.
10. Data sheet revision summary was added.

87C51FB-20/-3
83C51FB-20/-3
COMMERCIAL/EXPRESS
20 MHz MICROCONTROLLER

87C51FB-20/83C51FB-20—3.5 MHz to 20 MHz, V_{CC} = 5V ±20%
87C51FB-3/83C51FB-3—24 MHz Internal Operation, V_{CC} = 5V ±20%

- High Performance CHMOS EPROM
- 24 MHz Internal Operation (-3 only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Programmable Counter Array with:
  - — High Speed Output,
  - — Compare/Capture,
  - — Pulse Width Modulator,
  - — Watchdog Timer Capabilities
- Up/Down Timer/Counter
- Three Level Program Lock System
- 16K On-Chip EPROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 7 Interrupt Sources
- Four Level Interrupt Priority
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Fully Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 16 Kbytes of the program memory can reside in the on-chip EPROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 8XC51FB-20/-3 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 8XC51FB-20/-3 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 8XC51FB-20/-3 is an enhanced version of the 87C51/80C51BH. It's added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

The 87C51FB-3/83C51FB-3 has the same 3.5 to 20 MHz frequency range as the 87C51FB-20/83C51FB-20 when operating out of external program/data memory. When running out of internal program/data memory, the 87C51FB-3/83C51FB-3 can operate up to 24 MHz.

Throughout this document 8XC51FB-20 will refer to the 83C51FB-20, 87C51FB-20, 83C51FB-3 and the 87C51FB-3.

October 1992
Order Number: 272080-002

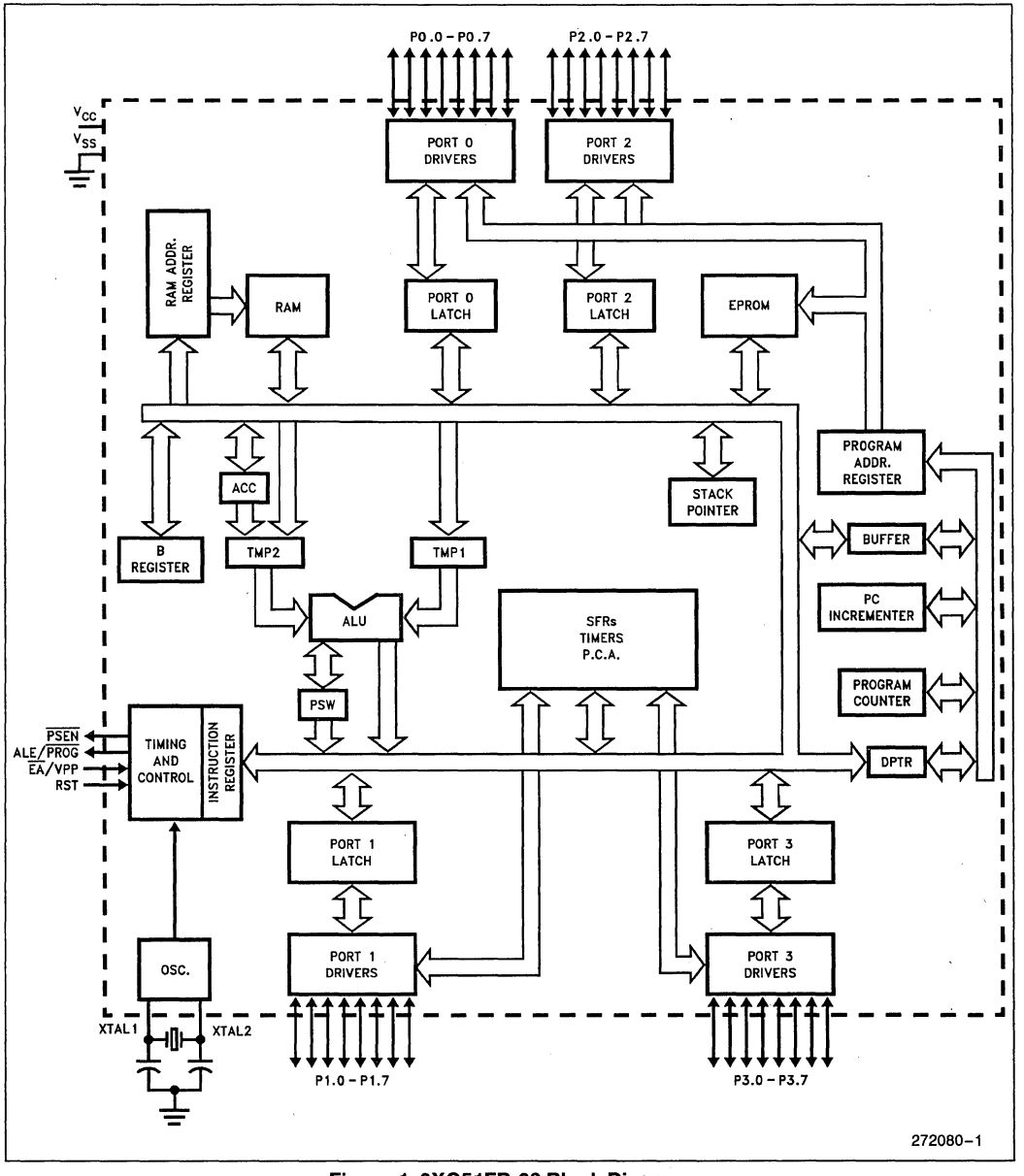


Figure 1. 8XC51FB-20 Block Diagram

PROCESS INFORMATION

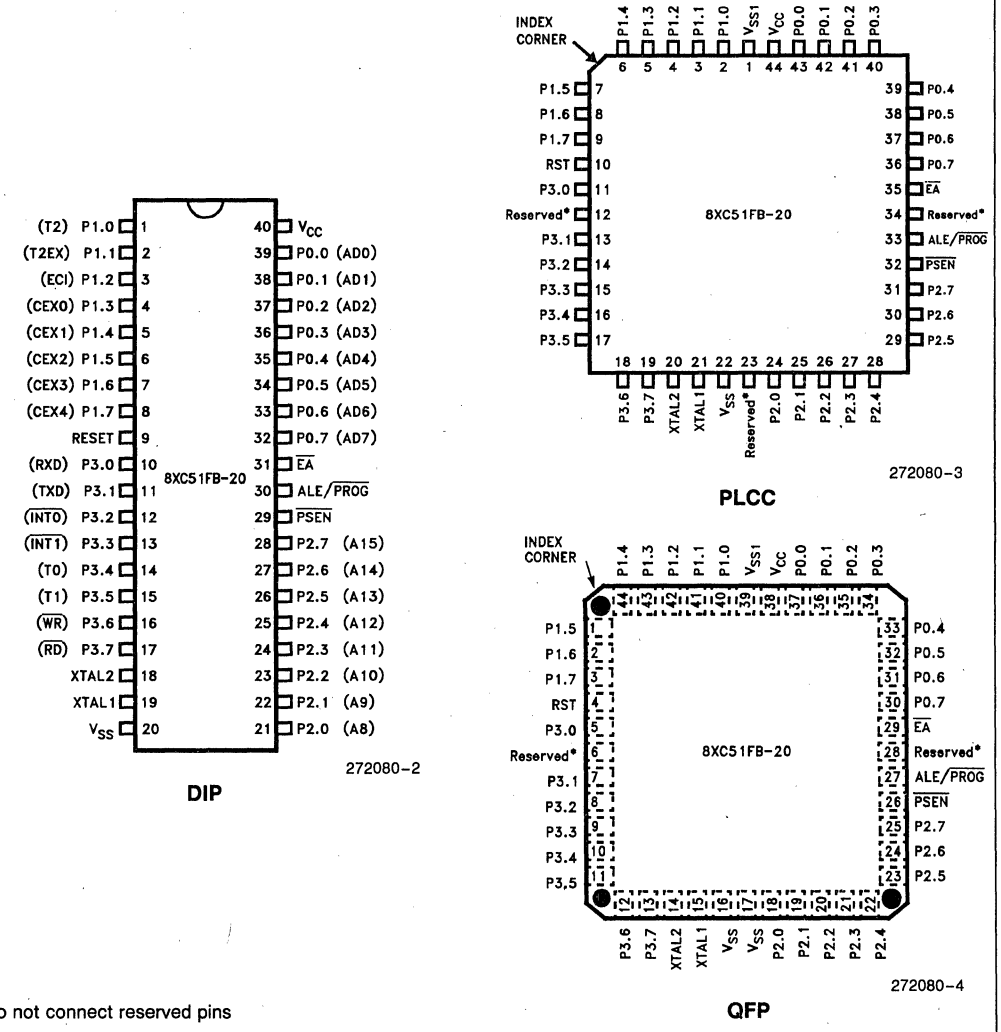
This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components and Reliability Handbook,* Order Number 210997.

8

PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC51FB-20	P	40-Pin Plastic DIP	45°C/W	16°C/W
87C51FB-20	D	40-Pin CERDIP	45°C/W	15°C/W
8XC51FB-20	N	44-Pin PLCC	46°C/W	16°C/W
8XC51FB-20	S	44-Pin QFP	96°C/W	24°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



*Do not connect reserved pins

Figure 2. Pin Connections

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Circuit ground.
V_{SS1}	Secondary ground (connection not necessary). Provided to reduce ground bounce and improve power supply bypassing. **NOTE:** This pin is not a substitute for the V_{SS} pin. Connect V_{SS} and V_{SS1} with the lowest impedance path possible.
Port 0	8-Bit, open drain, bidirectional I/O port. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during verification. When used as an I/O port, pullups to V_{CC} may be needed.
Port 1	8-Bit bidirectional I/O port. All of the port 1 pins are shared with other functions in the 8XC51FB-20. Port 1 is also used as the low-order address byte input during EPROM programming.
Port 2	8-Bit bidirectional I/O port. Port 2 also emits the high-order address byte during accesses to 16-bit external memory locations. Some of the Port 2 pins are also used as address bits for EPROM programming.
Port 3	8-Bit bidirectional I/O port. All of the port 3 pins are shared with other functions in the 8XC51FB-20. Two of the pins are used as control lines ($\overline{RD}$, $\overline{WR}$) for accessing external RAM.
RESET	Reset input to the chip. A high input for a minimum of two machine cycles with the oscillator running resets the device. The port pins will be reset when a voltage above V_{IH} is applied whether the oscillator is running or not. RST has an internal pulldown.
ALE/$\overline{PROG}$	Address Latch Enable. Provides a signal to demultiplex the address from the address/data bus. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode. This pin is also the program pulse input during EPROM programming.
$\overline{PSEN}$	Program Store Enable. Acts as read strobe for external program memory fetches.
$\overline{EA}$/V_{PP}	External Access Enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external program memory locations 0000H to 0FFFFH. $\overline{EA}$ should be strapped to V_{CC} for internal program executions. If any of the lock bits are programmed, $\overline{EA}$ will be internally latched on reset. This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	Input to the inverting oscillator amplifier.
XTAL2	Output from the inverting oscillator amplifier.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Express	 0 −40	 +70 +85	 °C °C
V_{CC}	Supply Voltage	4.0	6.0	V
F_{OSC}	Oscillator Frequency	3.5	20	MHz

DC CHARACTERISTICS (Over Operating Conditions)

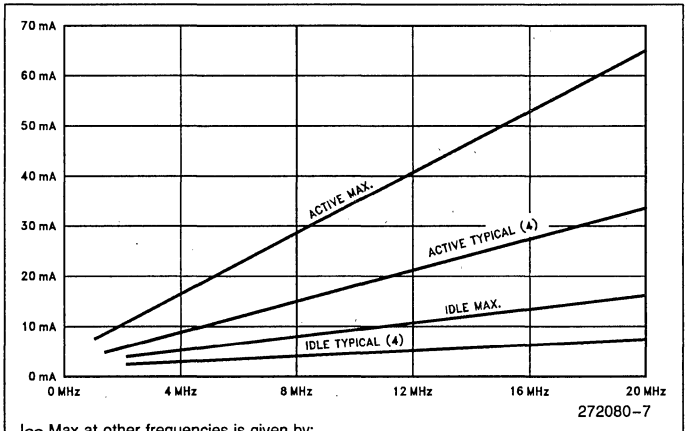
Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage (Note 5) (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage (Note 5) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3)	V_{CC}−0.3			V	I_{OH} = −10 μA
		V_{CC}−0.7			V	I_{OH} = −30 μA
		V_{CC}−1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	V_{CC}−0.3			V	I_{OH} = −200 μA
		V_{CC}−0.7			V	I_{OH} = −3.2 mA
		V_{CC}−1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45V < V_{IN} < V_{CC}

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3) Commercial Express			 −650 −750	 μA μA	 V_{IN} = 2V
R_{RST}	RST Pulldown Resistor	50		300	KΩ	
C_{IO}	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Running at 20 MHz (Figure 5) Idle Mode at 20 MHz (Figure 5) Power Down Mode		 32 7 15	 64 14 100	 mA mA μA	(Note 3)

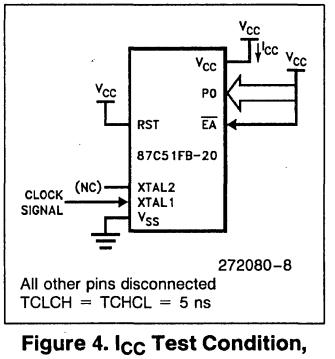
NOTES:
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with Schmitt triggers or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 4–7 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 3. I_{CC} vs Frequency



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 4. I_{CC} Test Condition, Active Mode

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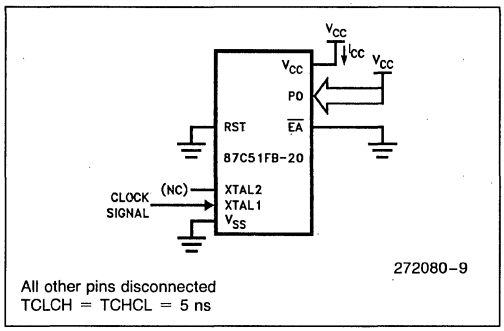


Figure 5. I_{CC} Test Condition Idle Mode

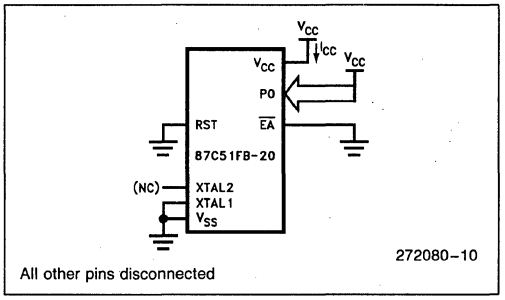


Figure 6. I_{CC} Test Condition, Power Down Mode V_{CC} = 2.0V to 6.0V

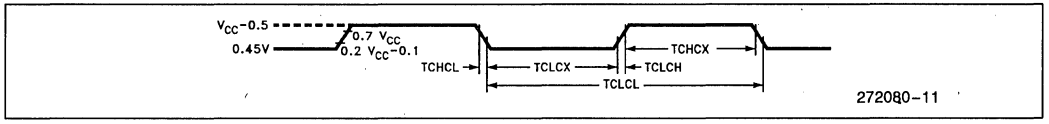


Figure 7. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

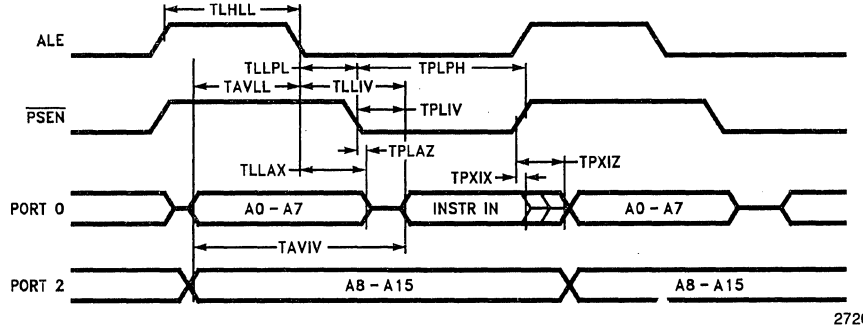
EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	20	MHz
TLHLL	ALE Pulse Width	60		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	10		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	20		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		125		4TCLCL−75	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	20		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	105		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		60		3TCLCL−90	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		30		TCLCL−20	ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TAVIV	Address to Valid Instruction In		145		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	200		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	200		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		155		5TCLCL−95	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		40		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		310		8TCLCL−90	ns
TAVDV	Address to Valid Data In		360		9TCLCL−90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	100	200	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	110		4TCLCL−90		ns
TQVWX	Data Valid before $\overline{WR}$	15		TCLCL−35		ns
TWHQX	Data Hold after $\overline{WR}$	10		TCLCL−40		ns
TQVWH	Data Valid to $\overline{WR}$ High	280		7TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	10	90	TCLCL−40	TCLCL+40	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



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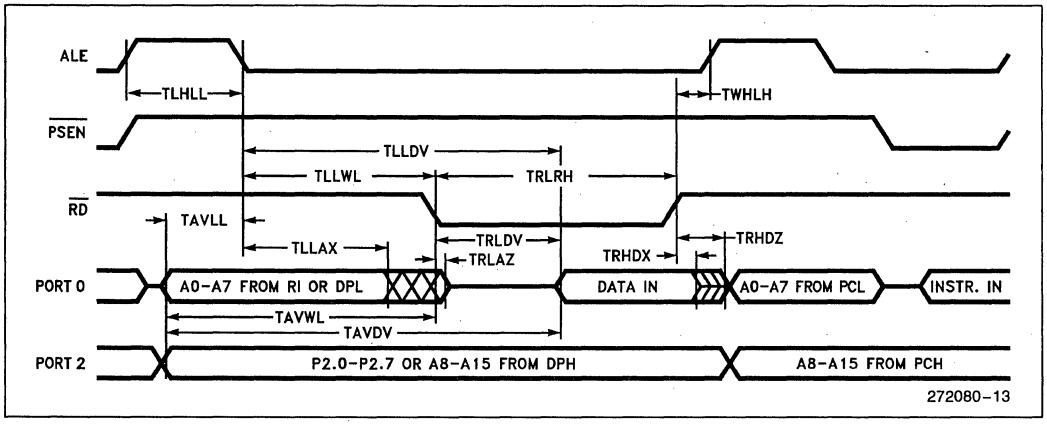
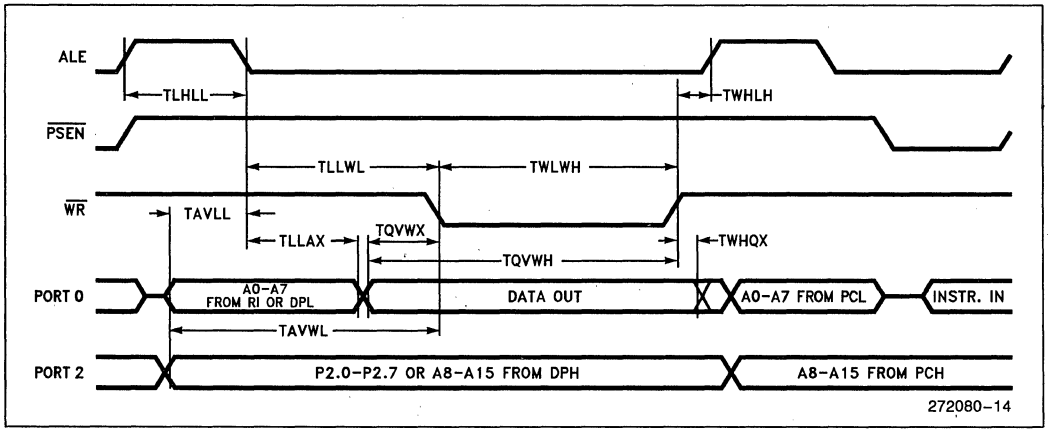
EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

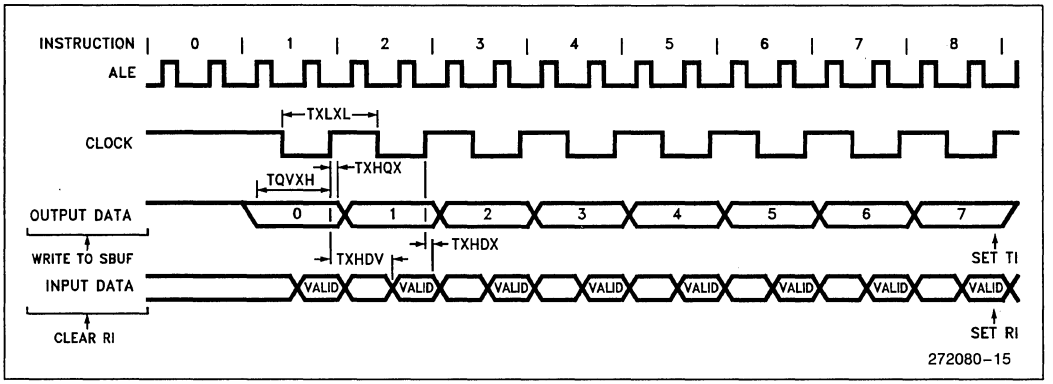


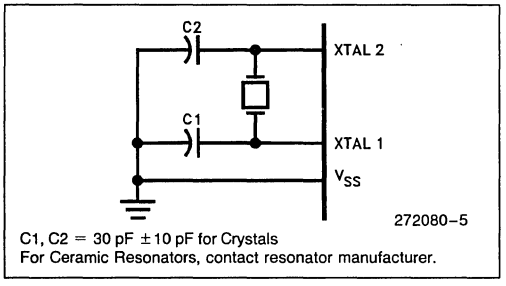
SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	600		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	367		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		367		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS





C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 8. Oscillator Connections

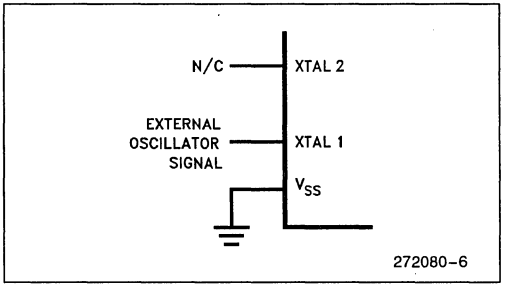
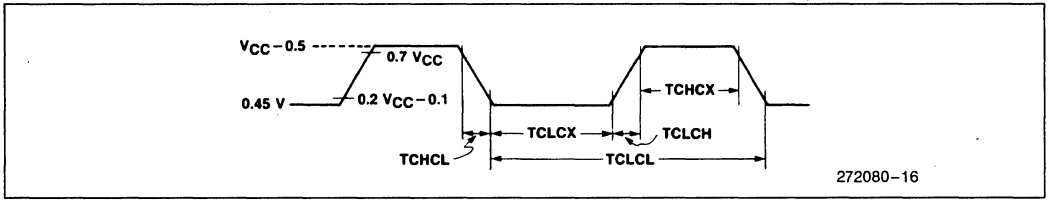


Figure 9. External Clock Drive Configuration

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



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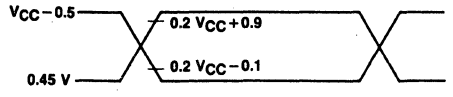
AC TESTING INPUT, OUTPUT WAVEFORMS



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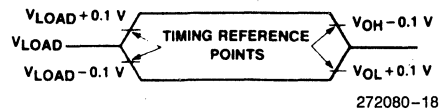
AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



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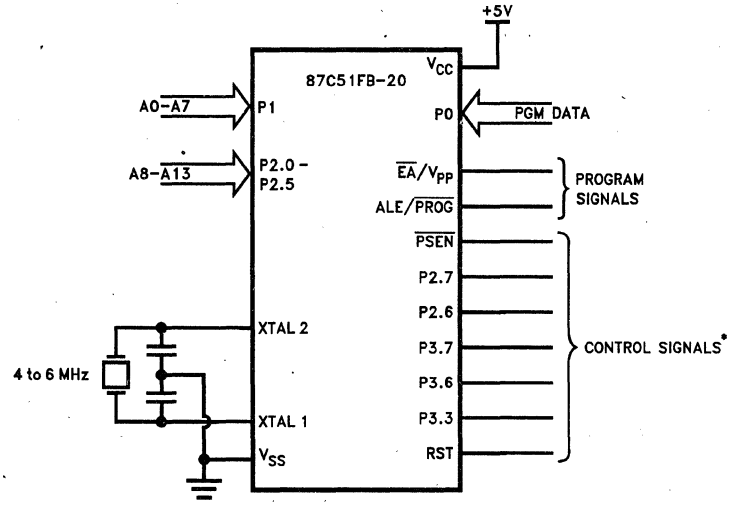
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

PROGRAMMING THE EPROM

Table 1. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



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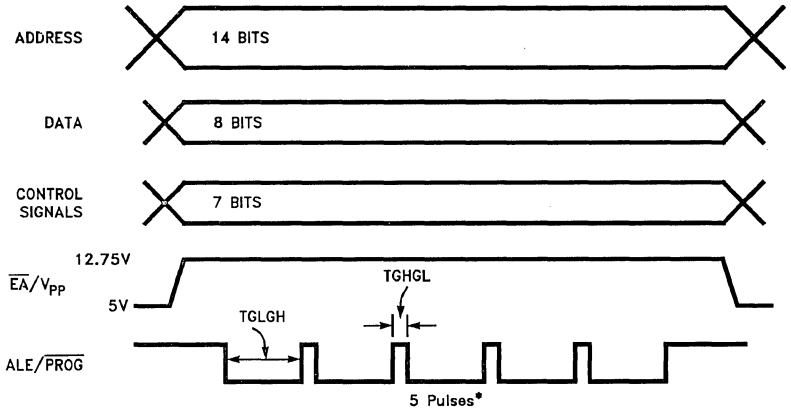
*See Table 1 for proper input on these pins

Figure 10. Programming the EPROM



*5 pulses for the EPROM array, 25 pulses for the Encryption Table and Lock Bits.

Figure 11. Programming Waveforms

Signature Bytes

Location	Contents	Description
30H	89H	Indicates Intel Device
31H	58H	Indicates FX-Core Product
60H	FBH	Indicates 87C51FB-20 Device
60H	7BH	Indicates 83C51FB-20 Device

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

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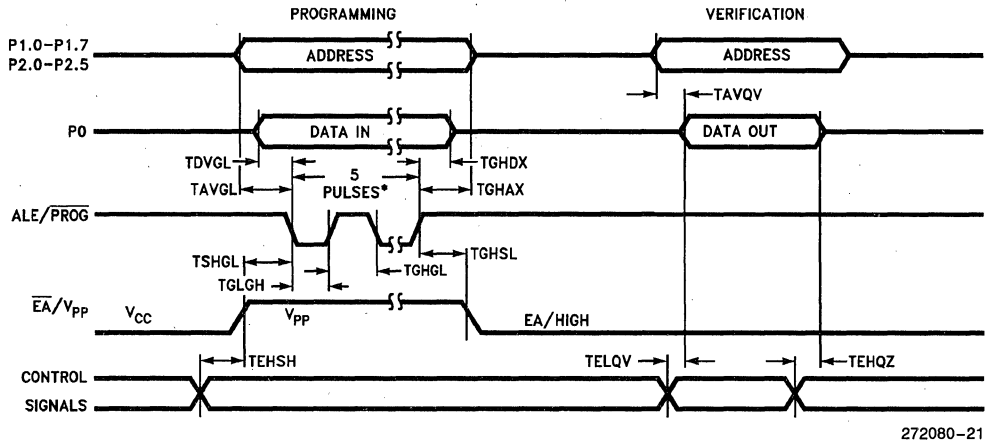
EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



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*5 pulses for the EPROM array, 25 pulses for the Encryption Table and Lock Bits.

DESIGN CONSIDERATIONS

- When running out of internal program/data memory, the 87C51FB-3/83C51FB-3 can be operated using a 24 MHz clock. If the 87C51FB-3/83C51FB-3 is running out of external program/data memory, the operating frequency must be between 3.5 to 20 MHz. The 87C51FB-3/83C51FB-3 will not function properly at 24 MHz when running out of external program/data memory.
- The window on the 87C51FB-20 must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Timer 2 Programmable Clock Out

- The Timer 2 clock out frequency on the 8XC51FB-20 is determined by the equation in the 8XC51FX Hardware Description as shown below.

$$\text{Clock-out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

Even though the equation permits a maximum clock-out frequency of 5 MHz using a 20 MHz oscillator, the maximum output frequency is 4 MHz. When operating the part above 16 MHz, RCAP2L must be limited to a maximum value of FEH.

DATA SHEET REVISION HISTORY

This data sheet (272080-002) is valid for devices with an "A" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (272080-002) and the previous version (272080-001):

1. Added 87C51FB-3/83C51FB-3 to 20 MHz data sheet.
2. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	120	125
	4TCLCL − 80	4TCLCL − 75
TPLIV	3TCLCL − 95	3TCLCL − 90
TWHQX	0	10
	TCLCL−50	TCLCL − 40
TQVWH	200	280
	7TCLCL−150	7TCLCL − 70

The following differences exist between revision 1 of the 87C51FB-20/83C51FB-20 (272080-001) data sheet and the 87C51FB/83C51FB (270563-004) data sheet.

1. All explanatory wording duplicated in the device user's guide was deleted.
2. Pins labeled "NC" changed to "Reserved" in Figure 2.
3. Timer 2 Programmable Clock Out paragraph added.
4. RRST specification in DC Characteristics Table changed from 40 KΩ min, 225 KΩ max to 50 KΩ min, 300 KΩ max.

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5. 20 MHz extension added to Figure 3.
6. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	4TCLCL − 100	4TCLCL − 80
TPLIV	3TCLCL − 105	3TCLCL − 95
TPXIZ	TCLCL − 25	TCLCL − 20
TRLDV	5TCLCL − 165	5TCLCL − 95
TLLDV	8TCLCL − 150	8TCLCL − 90
TAVDV	9TCLCL − 165	9TCLCL − 90
TAVWL	4TCLCL − 130	4TCLCL − 90
TQVWX	TCLCL − 50	TCLCL − 35

7. TXHQX in the Serial Port Timing Table changed from (2TCLCL − 117) to (2TCLCL − 50).

87C51FC/83C51FC
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 KBYTES INTERNAL PROGRAM MEMORY

87C51FC/83C51FC—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C51FC-⅛3C51FC-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%
87C51FC-L/83C51FC-L—3.5 MHz to 8 MHz, V_{CC} = 3.3V ±0.3V

- High Performance CHMOS EPROM
- Low Voltage Operation (-L only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Programmable Counter Array with:
  - — High Speed Output,
  - — Compare/Capture,
  - — Pulse Width Modulator,
  - — Watchdog Timer capabilities
- Up/Down Timer/Counter
- Three Level Program Lock System
- 32K On-Chip EPROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 7 Interrupt Sources
- Four Level Interrupt Priority
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Fully Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 32 Kbytes of the program memory can reside in the on-chip EPROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C51FC/83C51FC is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 87C51FC/83C51FC uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 87C51FC/83C51FC is an enhanced version of the 87C51/80C51BH. It's added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

Applications that require low voltage can use the 87C51FC-L/83C51FC-L. The 8XC51FC-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz.

Throughout this document 8XC51FC will refer to both the 83C51FC and the 87C51FC.

October 1992
Order Number: 270789-004

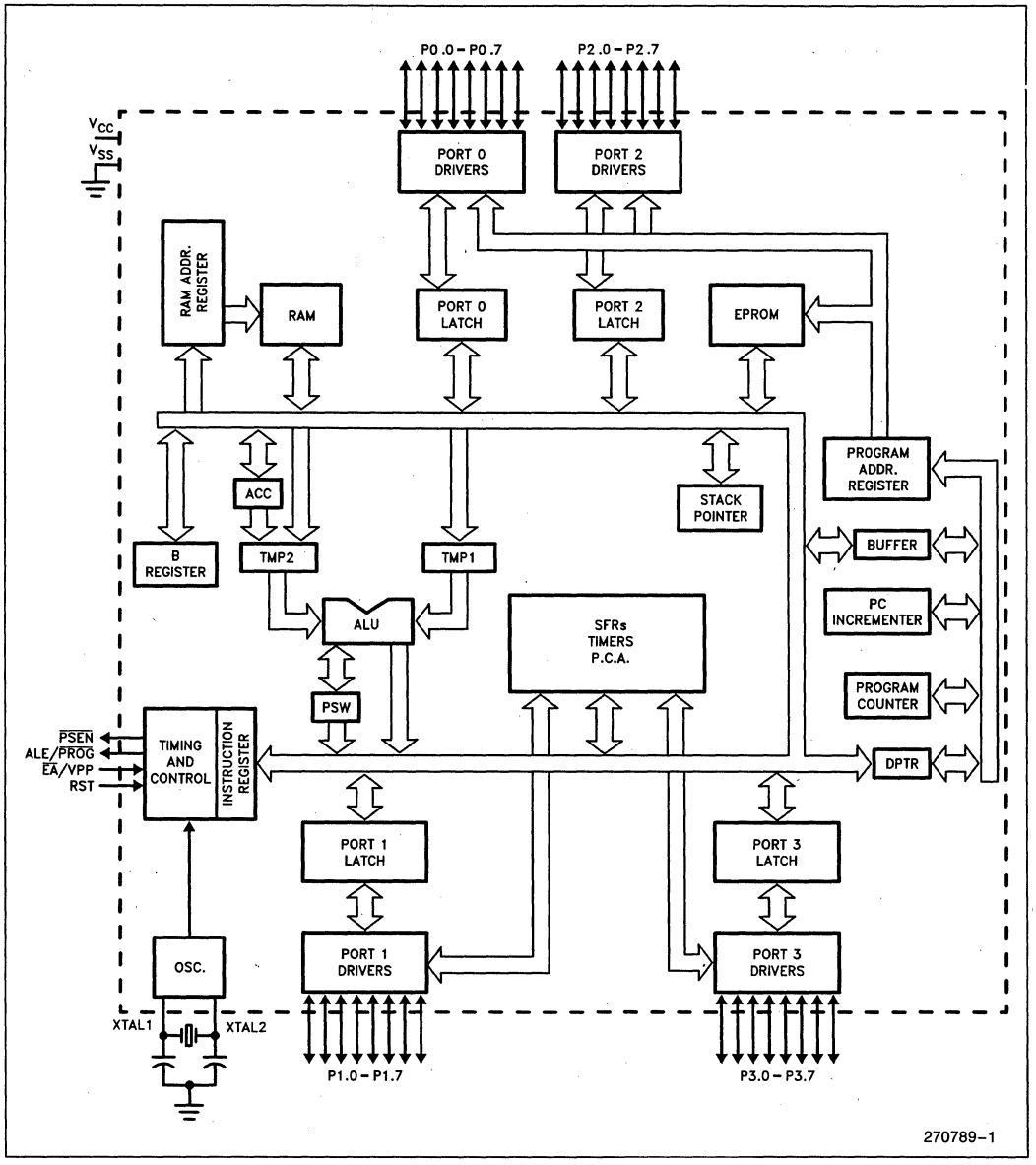

Figure 1. 8XC51FC Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components and Reliability Handbook,* Order Number 210997.

PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC51FC	P	40-Pin Plastic DIP	45°C/W	16°C/W
87C51FC	D	40-Pin CERDIP	36°C/W	13°C/W
8XC51FC	N	44-Pin PLCC	46°C/W	16°C/W
8XC51FC	S	44-Pin QFP	87°C/W	18°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

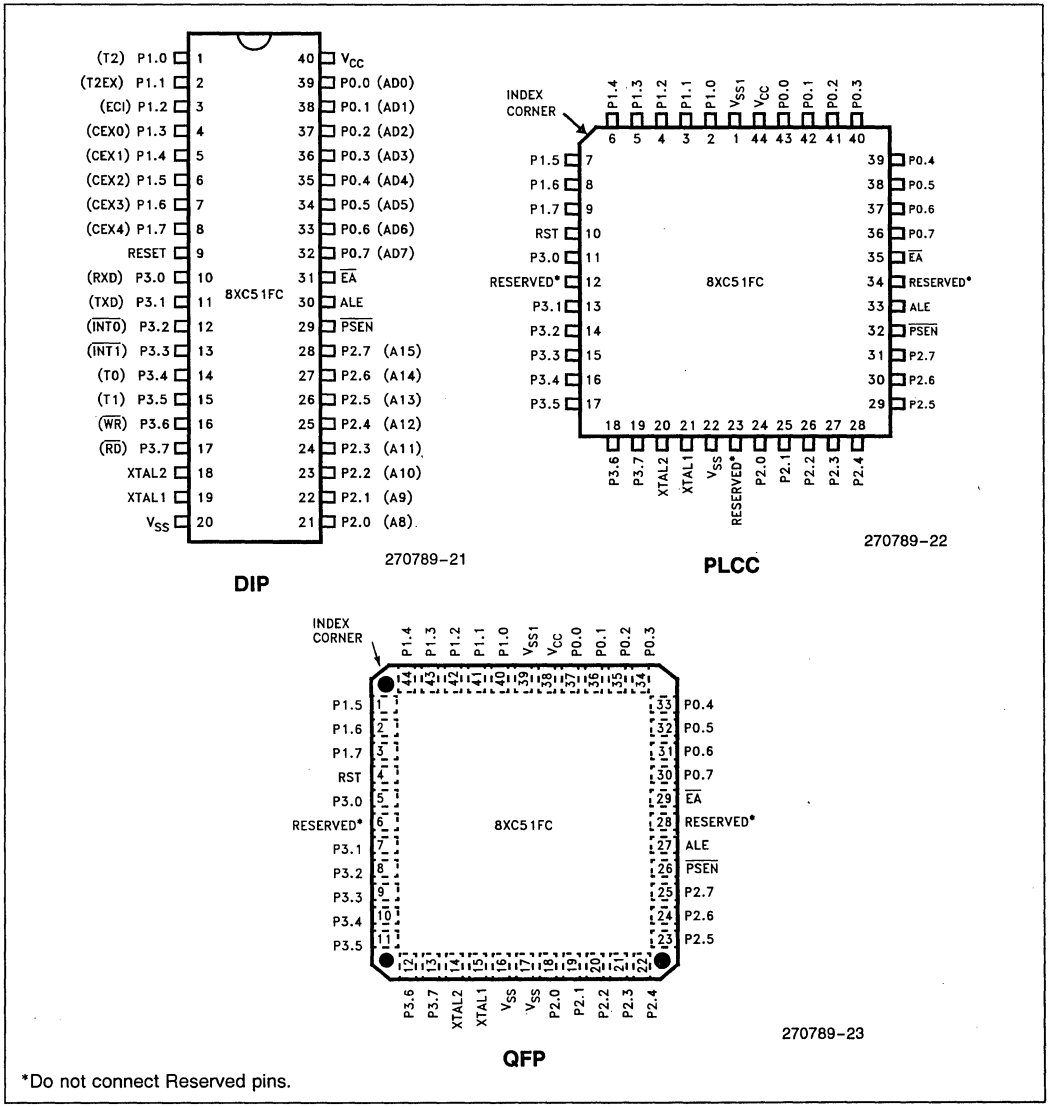

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin. Connect V_{SS} and V_{SS1} with the lowest impedance path possible.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC51FC:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during

accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The Port Pins will be driven to their reset condition when a voltage above V_{IH1} is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51FC.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX instruction. Otherwise the pin is weakly pulled high.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51FC is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

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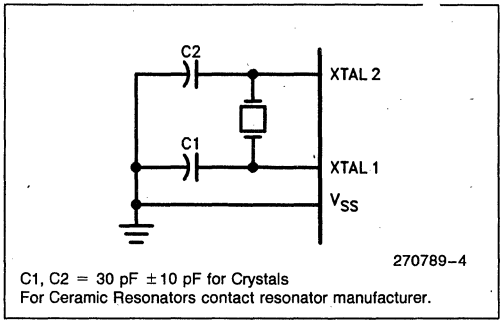

C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators contact resonator manufacturer.

Figure 3. Oscillator Connections

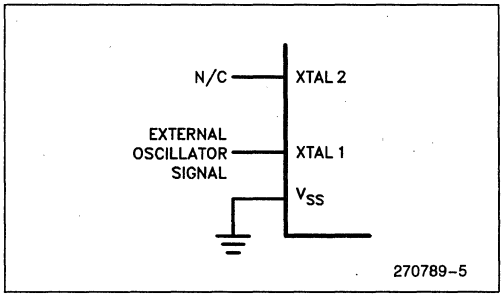

Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51FC either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level. The external interrupt or reset signal must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- The 8XC51FC-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz. Operating beyond these specifications could cause improper device functionality. (To program the 87C51FC-L, follow the same procedure as the 87C51FC.)
- The window on the 87C51FC must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC51FC without the 8XC51FC having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51FC is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins During Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH".

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} .....0V to +13.0V
Voltage on Any Other Pin to V_{SS} ..−0.5V to +6.5V
I_{OL} Per I/O Pin .....15 mA
Power Dissipation.....1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This is a production data sheet. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions: T_A (under Bias) = 0°C to +70°C, V_{CC} = 5V ±20%, V_{SS} = 0V
(8XC51FC-L, V_{CC} = 3.3V ±0.3V)

DC CHARACTERISTICS: (Over Operating Conditions)

All parameter values apply to both 5V and 3.3V devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2, and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)

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DC CHARACTERISTICS: (Over Operating Conditions)

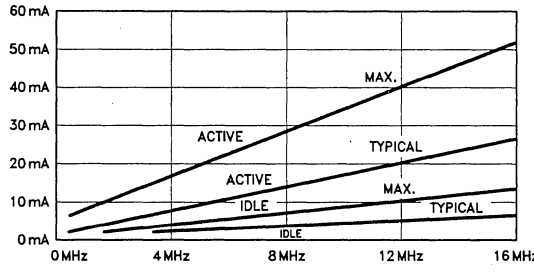
All parameter values apply to both 5V and 3.3V devices unless otherwise indicated. (Continued)

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{OH}	Output High Voltage (Ports 1, 2, and 3, ALE, $\overline{PSEN}$)	$V_{CC}-0.3$			V	$I_{OH} = -10\ \mu A$
		$V_{CC}-0.7$			V	$I_{OH} = -30\ \mu A$
		$V_{CC}-1.5$			V	$I_{OH} = -60\ \mu A$
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$V_{CC}-0.3$			V	$I_{OH} = -200\ \mu A$
		$V_{CC}-0.7$			V	$I_{OH} = -3.2$ mA
		$V_{CC}-1.5$			V	$I_{OH} = -7.0$ mA
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)			−50	μA	$V_{IN} = 0.45V$
I_{LI}	Input leakage Current (Port 0)			±10	μA	$0.45V < V_{IN} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3)			−650	μA	$V_{IN} = 2V$
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current:					(Note 3)
	Active Mode					
	8XC51FC-L at 8 MHz			12	mA	
	All others at 12 MHz (Figure 5)		20	40	mA	
	Idle Mode at 12 MHz (Figure 5)		5	10	mA	
	Power Down Mode		15	100	μA	

NOTES:

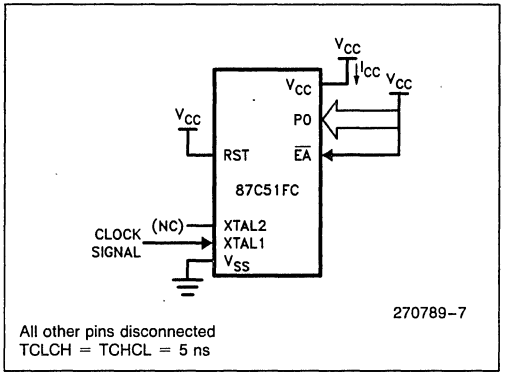
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with Schmitt triggers or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



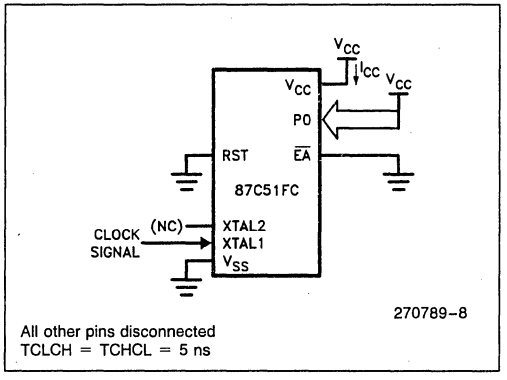
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 5. I_{CC} vs Frequency



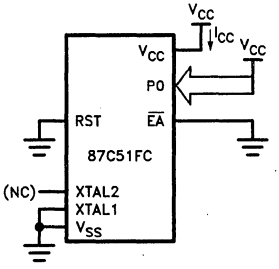
All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition Idle Mode



All other pins disconnected

Figure 8. I_{CC} Test Condition, Power Down Mode. V_{CC} = 2.0V to 6.0V

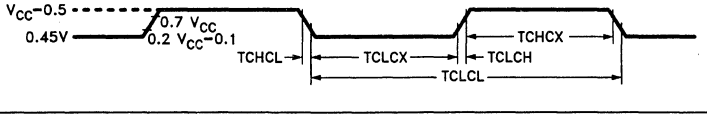


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

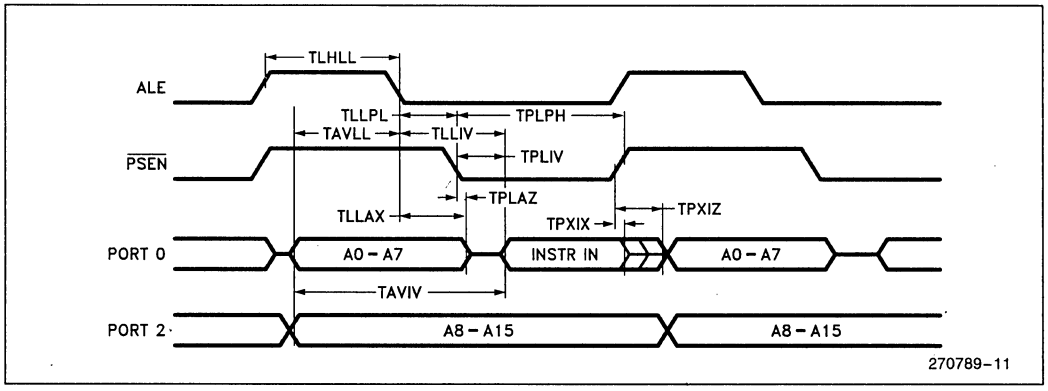
TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

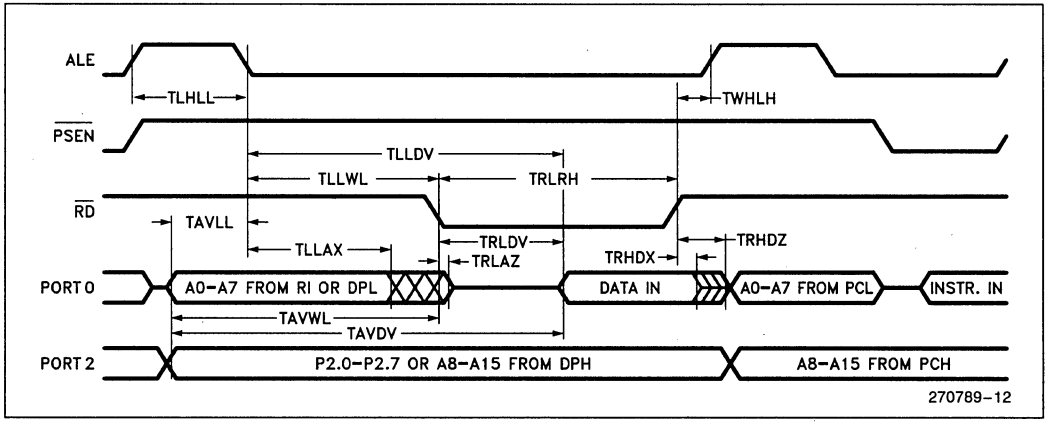
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	53		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	53		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		3TCLCL−105	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		312		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid before $\overline{WR}$	33		TCLCL−50		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL−50		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

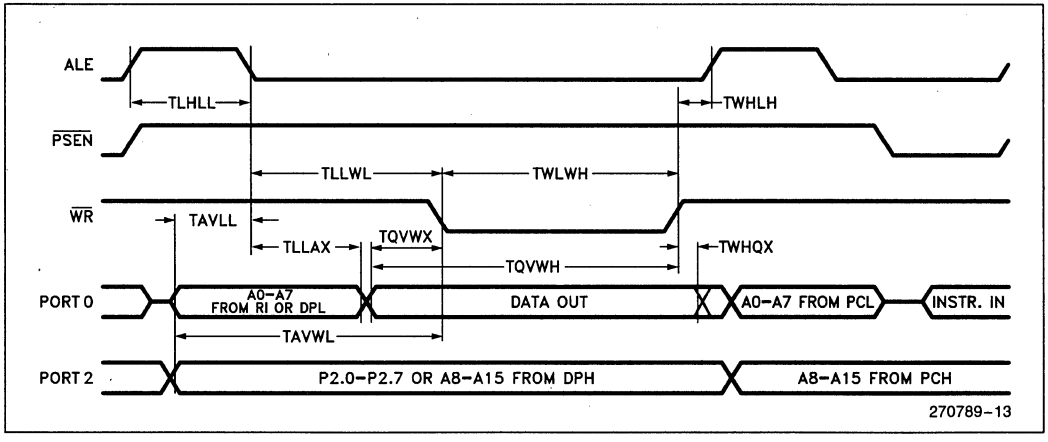
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE



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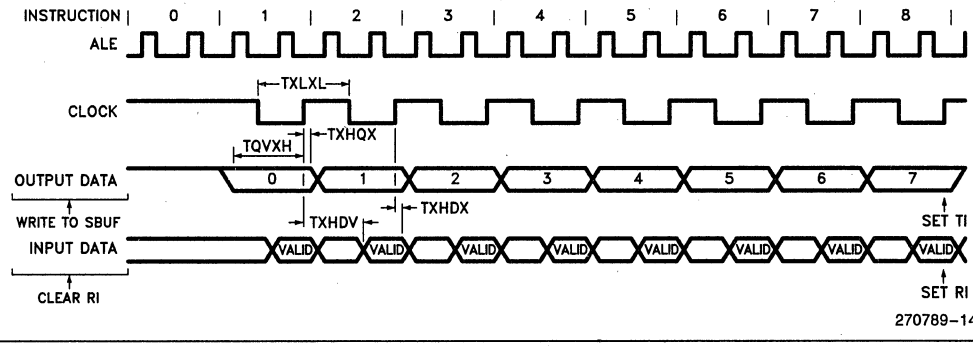
SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		µs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL−133	ns

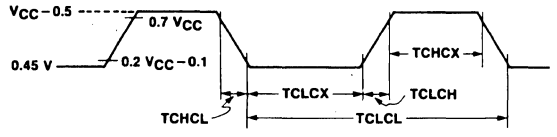
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

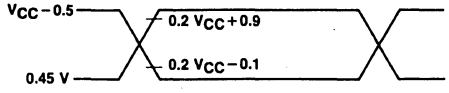
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XC51FC 8XC51FC-1	 3.5 3.5	 12 16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



270789-15

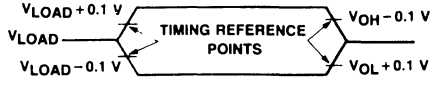
AC TESTING INPUT, OUTPUT WAVEFORMS



270789-16

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



270789-17

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA. (-L, $I_{OL}/I_{OH} = \pm 10$ mA)

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4 respectively for A0–A14.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

8

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51FC the following sequence must be exercised.

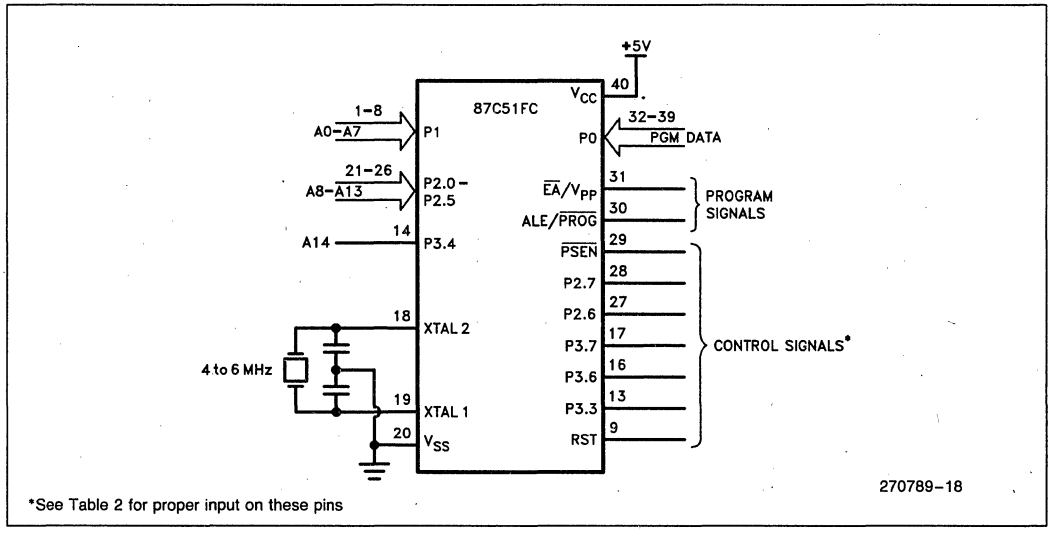
1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. A complete verify of the array will ensure reliable programming of the 87C51FC.

The lock bits cannot be directly verified. They are verified by observing that their features are enabled. Refer to the EPROM Program Lock section in this data sheet.



*See Table 2 for proper input on these pins

Figure 10. Programming the EPROM

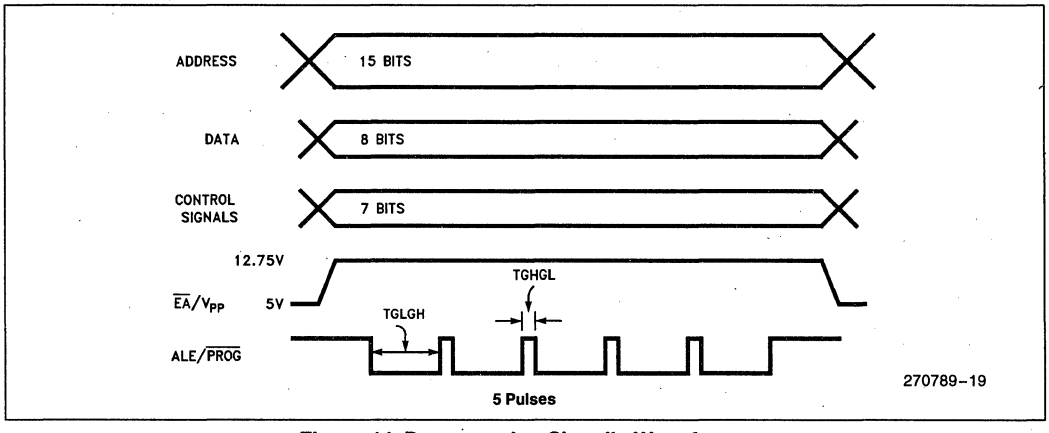


Figure 11. Programming Signal's Waveforms

ROM and EPROM Lock System

The 87C51FC and the 83C51FC program lock systems, when programmed, protect the onboard program against software piracy.

The 83C51FC has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 3. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C51FC has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 3.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in it's original, unmodified form. For programming the Encryption Array, refer to Table 2 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C51FC has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 8XC51FC has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents	
	87C51FC	83C51FC
30H	89H	89H
31H	58H	58H
60H	FCH	FCH/7CH

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

Table 3. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

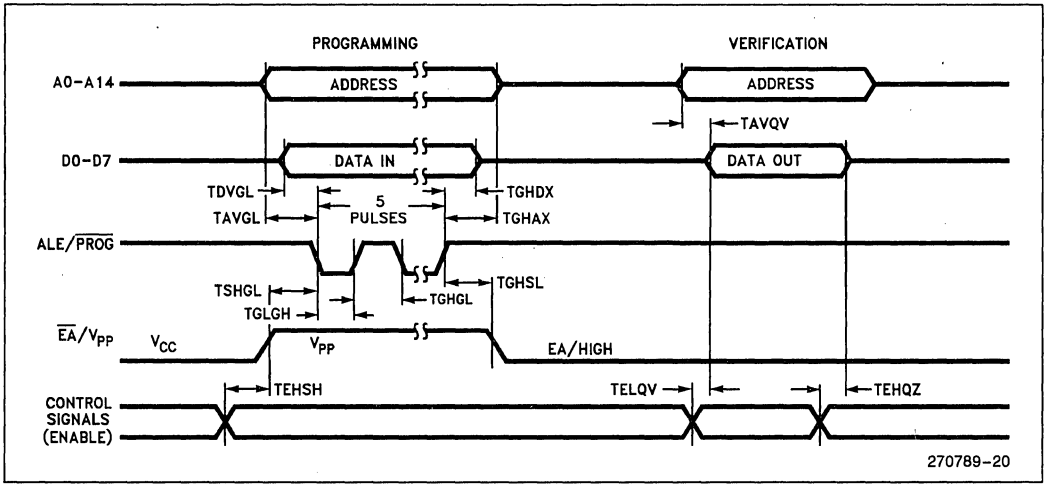
Any other combination of the lock bits is not defined.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



DATA SHEET REVISION HISTORY

The following differences exist between this data sheet (270789-004) and the previous version (270789-003):

1. Added 3.3V device to data sheet.
2. Data sheet title was changed from:

   87C51FC/83C51FC CHMOS Single-Chip 8-Bit Microcontroller 32 Kbytes User Programmable EPROM

   to:

   87C51FC/83C51FC CHMOS Single-Chip 8-Bit Microcontroller with 32 Kbytes Internal Program Memory
3. Data sheet status changed from "Preliminary" to "Production".
4. Added process information after block diagram.
5. θ_{ja} and θ_{jc} information added to Packages table.

The following differences exist between the -003 and -002 versions of this data sheet.

1. QFP package type added.
2. Changed "NC" pin labels to "Reserved".
3. Added second paragraph under "Encryption Array" section.

The following differences exist between the 270789-002 data sheet and the 270789-001 version:

1. Changed title from "87C51FC" to "87C51FC/83C51FC".
2. Changed data sheet status from "Advanced" to "Preliminary".
3. Deleted all references to -2 version.
4. Added "Four Level Interrupt Priority" feature bullet.
5. Changed feature bullet, "Two Level Program Lock System" to read, "Three Level Program Lock System".
6. Revised RST pin description to include asynchronous port reset feature.
7. Changed Figure 3 to read, "= 40 pF ±10 pF for Ceramic Resonators".
8. Added V_{IL1} specification to DC Characteristics Table.
9. Changed test conditions under I_{LI} from 0V to 0.45V for V_{IN} minimum.
10. Changed V_{CC} maximum from 5.5V to 6.0V for I_{CC} Test Condition under Figure 8.
11. Revised Absolute Maximum Ratings warning and data sheet status notice.
12. Reworded DC Characteristics Note 1.
13. Changed 1/TCLCL Minimum specification from 0.5 MHz to 3.5 MHz.
14. Revised "EPROM Program Lock" section to include ROM lock description.
15. Deleted all references to A15 in "Definition of Terms" and Figure 10.
16. Changed number of encryption array address lines from 5 to 6 under "Encryption Array" section.
17. Added signature byte table to "Reading the Signature Bytes" section.
18. Added this revision summary.

87C51FC/83C51FC

EXPRESS

87C51FC/83C51FC—3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
87C51FC-1/83C51FC-1—3.5 MHz to 16 MHz, V_{CC} = 5V ±20%

- **Extended Temperature Range**
- **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here. This data sheet is valid in conjunction with the commercial 87C51FC/83C51FC data sheet, 270789-002.

October 1990
Order Number: 270903-001

Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

D.C. CHARACTERISTICS $T_A = -40°C$ to $+85°C$; $V_{CC} = 5V \pm 20\%$; $V_{SS} = 0V$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		−750	μA	$V_{IN} = 2V$

Table 1. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
D*	Cerdip	Commercial	No
N	PLCC	Commercial	No
TP	Plastic	Extended	No
TD*	Cerdip	Extended	No
TN	PLCC	Extended	No
LP	Plastic	Extended	Yes
LD*	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

NOTE:
- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-in is dynamic for a minimum time of 168 hours at 125°C, $V_{CC} = 6.9V \pm 0.25V$, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

*Available for 87C51FC only.

Examples:

P87C51FC indicates 87C51FC in a plastic package and specified for commercial temperature range, without burn-in.
LD87C51FC indicates 87C51FC in a cerdip package and specified for extended temperature range with burn-in.

DATA SHEET REVISION SUMMARY

This is Rev. 1 of the 87C51FC/83C51FC Express data sheet.

87C51FC-20/-3
83C51FC-20/-3
COMMERCIAL/EXPRESS 20 MHz MICROCONTROLLER

87C51FC-20/83C51FC-20—3.5 MHz to 20 MHz, V_{CC} = 5V ± 20%
87C51FC-3/83C51FC-3—24 MHz Internal Operation, V_{CC} = 5V ± 20%

- High Performance CHMOS EPROM
- 24 MHz Internal Operation (-3 only)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Programmable Counter Array with:
  - — High Speed Output,
  - — Compare/Capture,
  - — Pulse Width Modulator,
  - — Watchdog Timer capabilities
- Up/Down Timer/Counter
- Three Level Program Lock System
- 32K On-Chip EPROM
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 7 Interrupt Sources
- Four Level Interrupt Priority
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS®-51 Fully Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 32 Kbytes of the program memory can reside in the on-chip EPROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 8XC51FC-20/-3 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS-51 family, the 8XC51FC-20/-3 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 8XC51FC-20/-3 is an enhanced version of the 87C51/80C51BH. Its added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

The 87C51FC-3/83C51FC-3 has the same 3.5 MHz to 20 MHz frequency range as the 87C51FC-20/83C51FC-20 when operating out of external program/data memory. When running out of internal program/data memory, the 87C51FC-3/83C51FC-3 can operate up to 24 MHz.

Throughout this document 8XC51FC-20 will refer to the 83C51FC-20, 87C51FC-20, 83C51FC-3 and the 87C51FC-3.

October 1992
Order Number: 272028-002

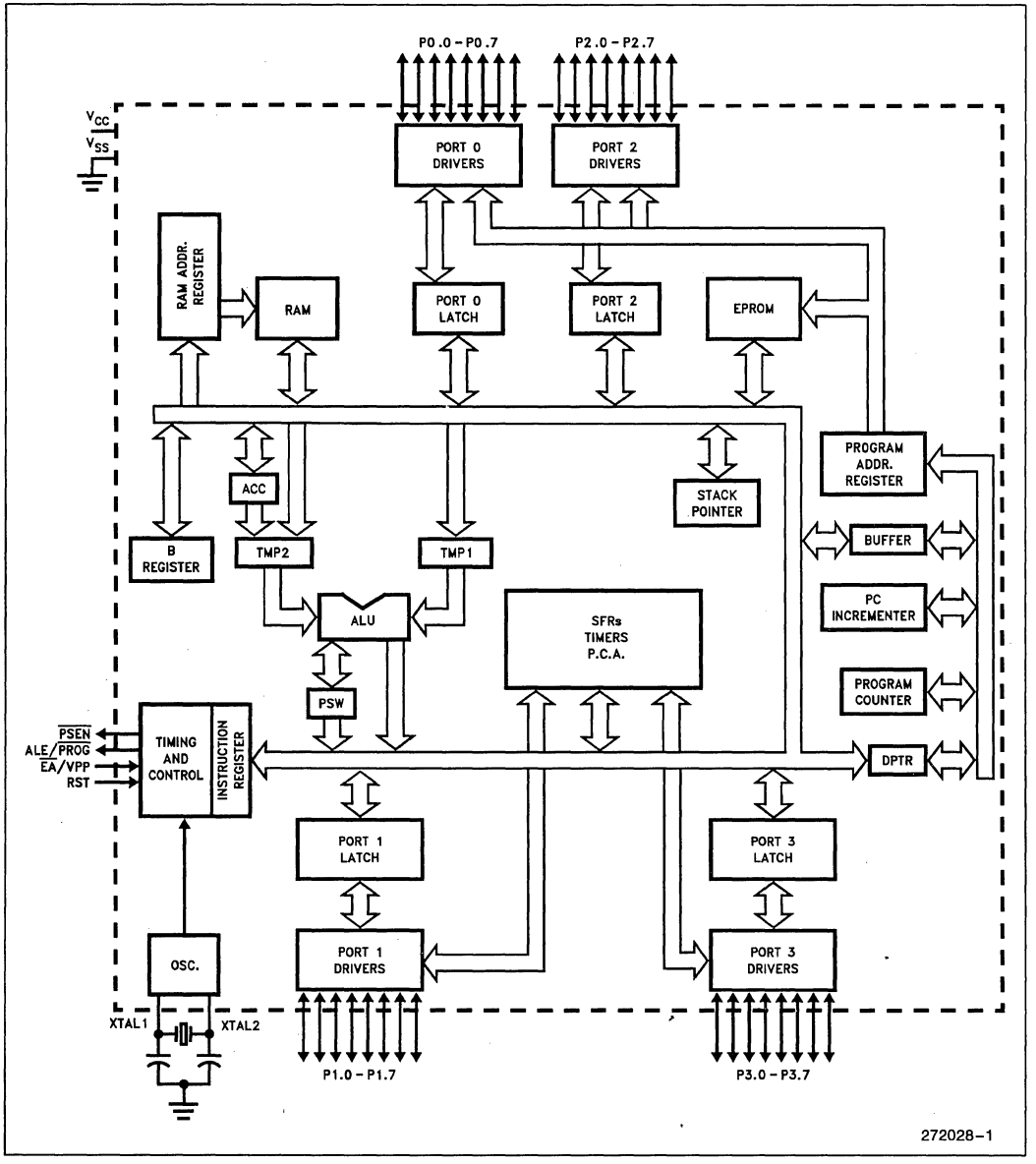


Figure 1. 8XC51FC-20 Block Diagram

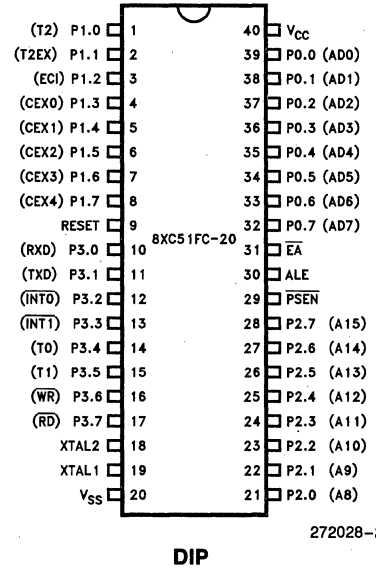
PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components and Reliability Handbook*, Order Number 210997.

PACKAGES

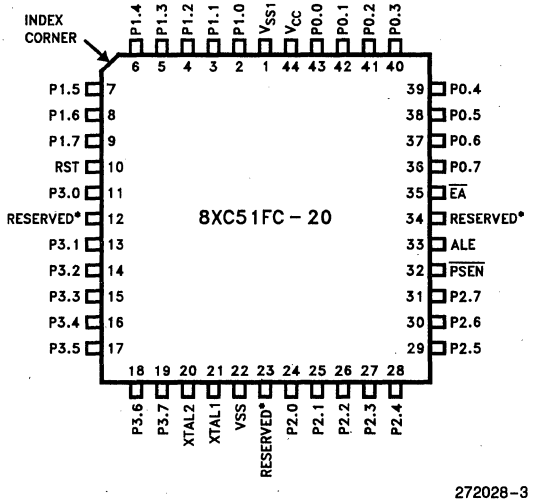
Part	Prefix	Package Type	θ_{ja}	θ_{jc}
8XC51FC-20	P	40-Pin Plastic DIP	45°C/W	16°C/W
87C51FC-20	D	40-Pin CERDIP	36°C/W	13°C/W
8XC51FC-20	N	44-Pin PLCC	46°C/W	16°C/W
8XC51FC-20	S	44-Pin QFP	87°C/W	18°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



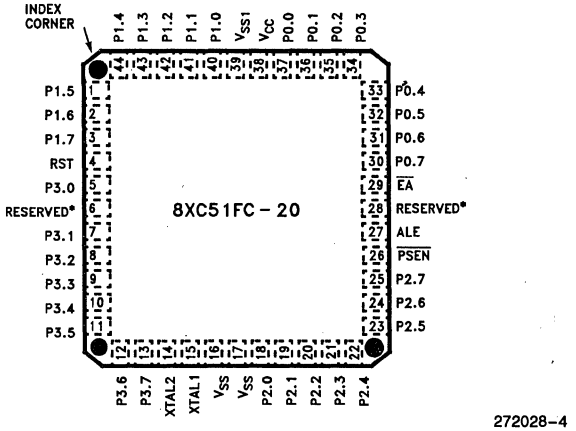
272028-2

DIP



272028-3

PLCC



272028-4

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin. Connect V_{SS} and V_{SS1} with the lowest impedance path possible.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC51FC-20:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it

uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The Port Pins will be driven to their reset condition when a voltage above V_{IH1} is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51FC-20.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX instruction. Otherwise the pin is weakly pulled high.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51FC-20 is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

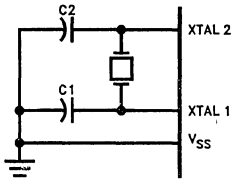
XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but the minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators contact resonator manufacturer.

Figure 3. Oscillator Connections

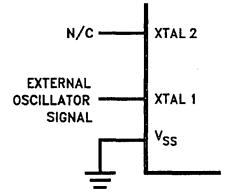


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51FC-20 either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level. The external interrupt or reset signal must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

TIMER 2 PROGRAMMABLE CLOCK OUT

The **maximum** Timer 2 clock out frequency on the 8XC51FC-20 cannot be determined by the equation in the 8XC51FX Hardware Description as shown below.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

Even though the equation permits a maximum clock-out frequency of 5 MHz using a 20 MHz oscillator, the maximum device output frequency is 4 MHz. When using a 20 MHz oscillator, RCAP2L must be limited to a maximum value of FEH.

For a complete description of all Timer 2 functions, please reference the 8XC51FX Hardware Description in the Embedded Microcontrollers and Processors Handbook Volume I.

DESIGN CONSIDERATION

- When running out of internal program/data memory, the 87C51FC-3/83C51FC-3 can be operated using a 24 MHz clock. If the 87C51FC-3/83C51FC-3 is running out of external program/data memory, the operating frequency must be between 3.5 MHz to 20 MHz. The 87C51FC-3/83C51FC-3 will not function properly at 24 MHz when running out of external program/data memory.
- The window on the 87C51FC-20 must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may functionally be impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC51FC-20 without the 8XC51FC-20 having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51FC-20 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins During Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} .....0V to +13.0V
Voltage on Any Other Pin to V_{SS} ..−0.5V to +6.5V
I_{OL} Per I/O Pin .....15 mA
Power Dissipation.....1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Express	 0 −40	 +70 +85	 °C °C
V_{CC}	Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency	3.5	20	MHz

DC CHARACTERISTICS Over Operating Conditions

All parameter values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC}−0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC}−0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC}+0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC}+0.5	V	
V_{OL}	Output Low Voltage(5) (Ports 1, 2, and 3)			0.3	V	I_{OL} = 100 μA(1)
				0.45	V	I_{OL} = 1.6 mA(1)
				1.0	V	I_{OL} = 3.5 mA(1)
V_{OL1}	Output Low Voltage(5) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA(1)
				0.45	V	I_{OL} = 3.2 mA(1)
				1.0	V	I_{OL} = 7.0 mA(1)
V_{OH}	Output High Voltage (Ports 1, 2, and 3, ALE, $\overline{PSEN}$)	V_{CC}−0.3			V	I_{OH} = −10 μA
		V_{CC}−0.7			V	I_{OH} = −30 μA
		V_{CC}−1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC}−0.3			V	I_{OH} = −200 μA
		V_{CC}−0.7			V	I_{OH} = −3.2 mA
		V_{CC}−1.5			V	I_{OH} = −7.0 mA

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DC CHARACTERISTICS Over Operating Conditions (Continued)

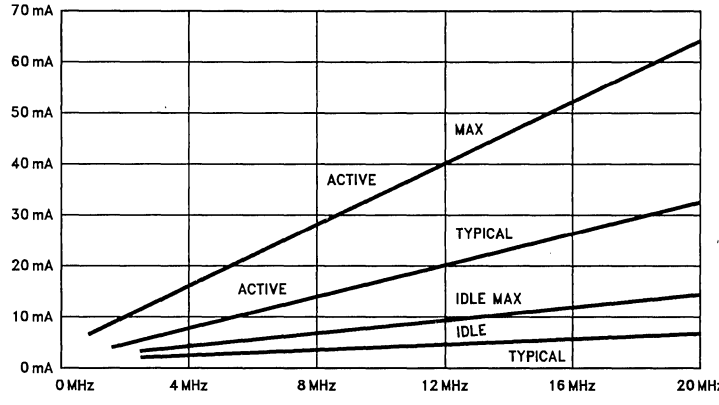
All parameter values apply to both Commercial and Express devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(4)	Max	Unit	Test Conditions
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)			−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)			±10	μA	0.45V < V_{IN} < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3) Commercial Express			 −650 −750	 μA	 V_{IN} = 2V
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Running at 12 MHz (Figure 5) Idle Mode at 12 MHz (Figure 5) Power Down Mode		 20 5 15	 40 10 100	 mA mA μA	(Note 3)

NOTES:

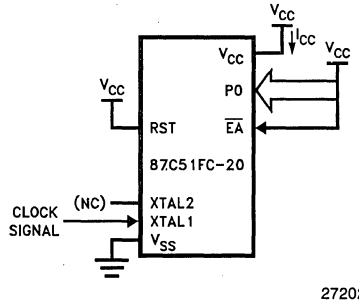
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with Schmitt triggers or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



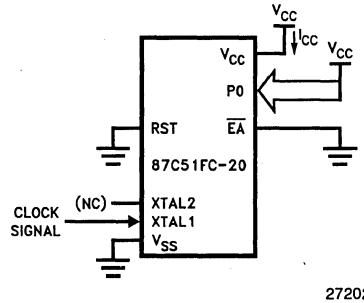
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 5. I_{CC} vs Frequency



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition Idle Mode

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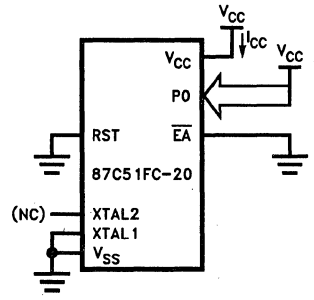


Figure 8. I_{CC} Test Condition, Power Down Mode
V_{CC} = 2.0V to 6.0V

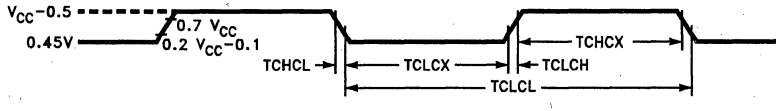


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

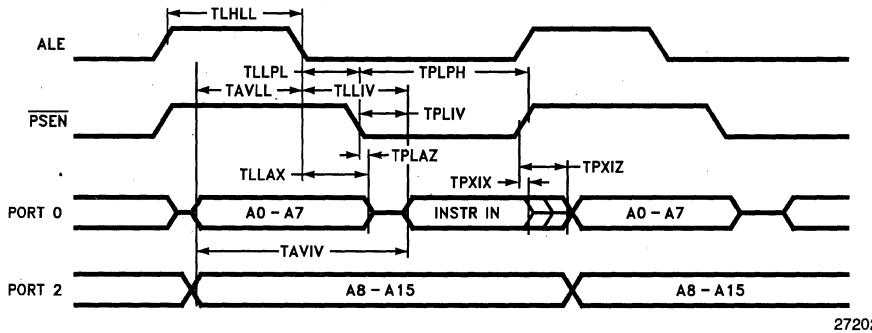
TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

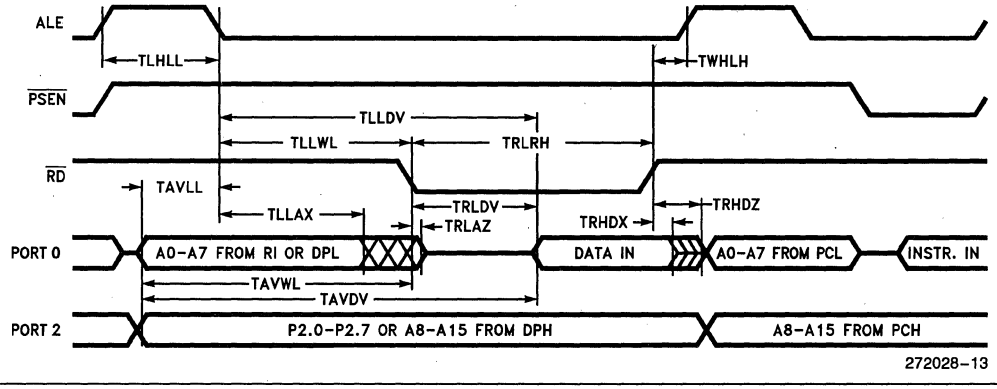
EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	20	MHz
TLHLL	ALE Pulse Width	60		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	10		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	20		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		125		4TCLCL−75	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	20		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	105		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		60		3TCLCL−90	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		30		TCLCL−20	ns
TAVIV	Address to Valid Instruction In		145		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	200		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	200		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		155		5TCLCL−95	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		40		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		310		8TCLCL−90	ns
TAVDV	Address to Valid Data In		360		9TCLCL−90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	100	200	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	110		4TCLCL−90		ns
TQVWX	Data Valid before $\overline{WR}$	15		TCLCL−35		ns
TWHQX	Data Hold after $\overline{WR}$	10		TCLCL−40		ns
TQVWH	Data Valid to $\overline{WR}$ High	280		7TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	10	90	TCLCL−40	TCLCL+40	ns

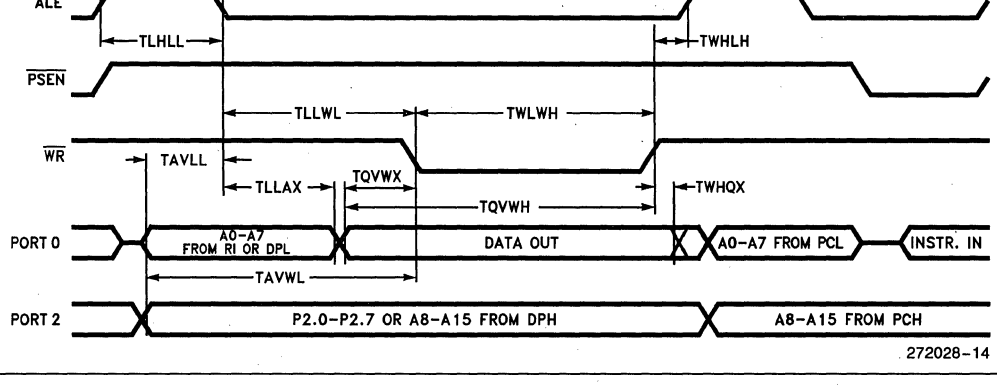
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

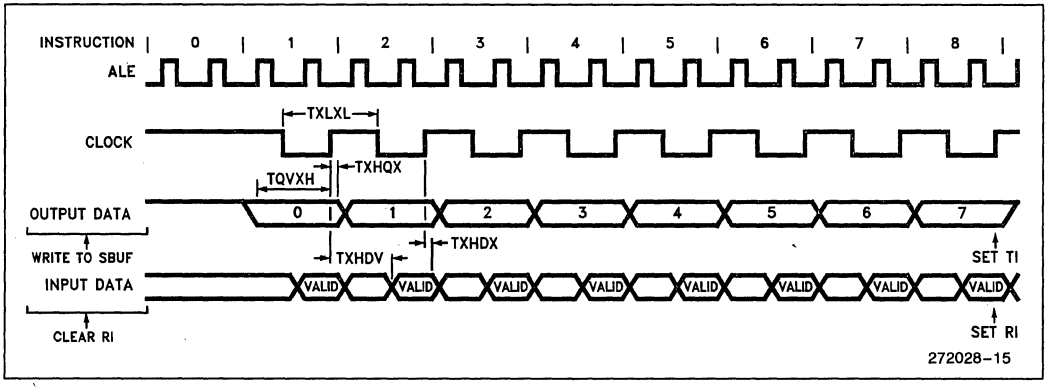


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V; Load Capacitance = 80 pF

Symbol	Parameter	20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	600		12 TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	367		10 TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2 TCLCL − 50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		367		10 TCLCL − 133	ns

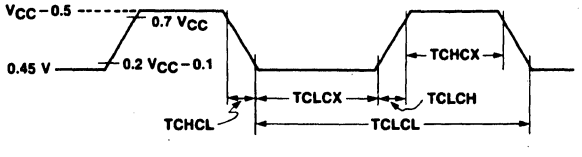
SHIFT REGISTER MODE TIMING WAVEFORMS



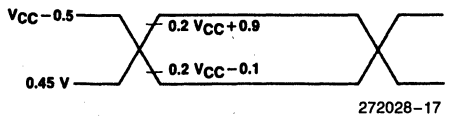
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



AC TESTING INPUT, OUTPUT WAVEFORMS



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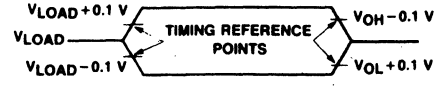
AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



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For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA.

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4 respectively for A0–A14.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

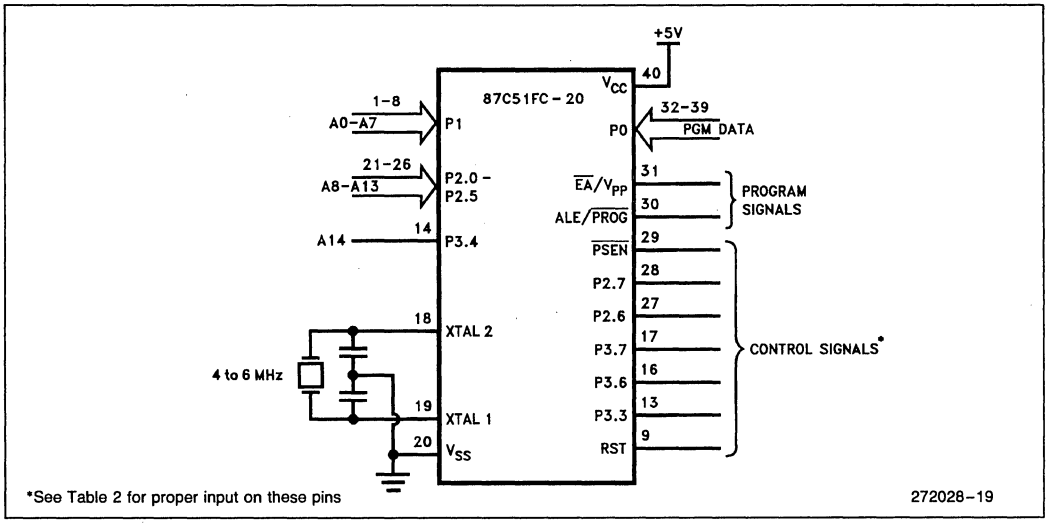

Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51FC-20 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte, or block of bytes that is programmed. A complete verify of the array will ensure reliable programming of the 87C51FC-20.

The lock bits cannot be directly verified. They are verified by observing that their features are enabled. Refer to the EPROM Program Lock section in this data sheet.

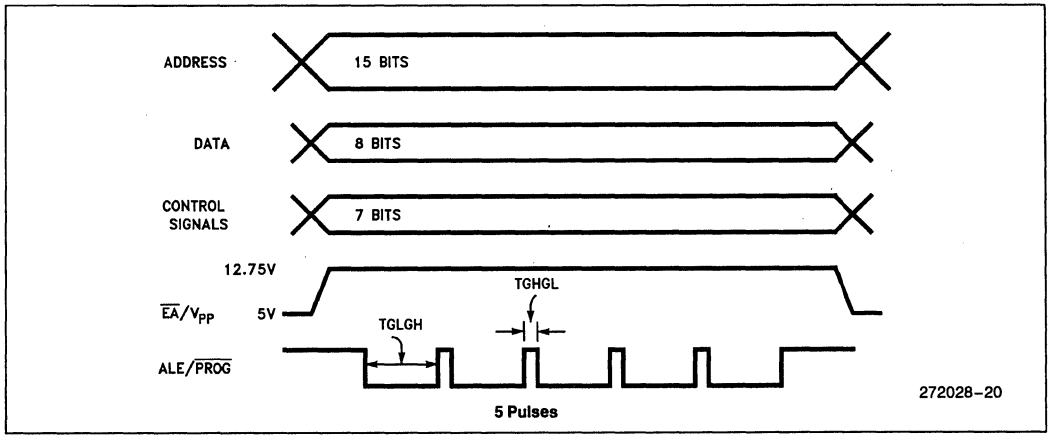

Figure 11. Programming Signal's Waveforms

8

ROM and EPROM Lock System

The 87C51FC-20 and the 83C51FC-20 program lock systems, when programmed, protect the onboard program against software piracy.

The 83C51FC-20 has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 3. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C51FC-20 has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 3.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in it's original, unmodified form. For programming the Encryption Array, refer to Table 2 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C51FC-20 has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 8XC51FC-20 has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents	
	87C51FC-20	83C51FC-20
30H	89H	89H
31H	58H	58H
60H	FCH	FCH/7CH

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

Table 3. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

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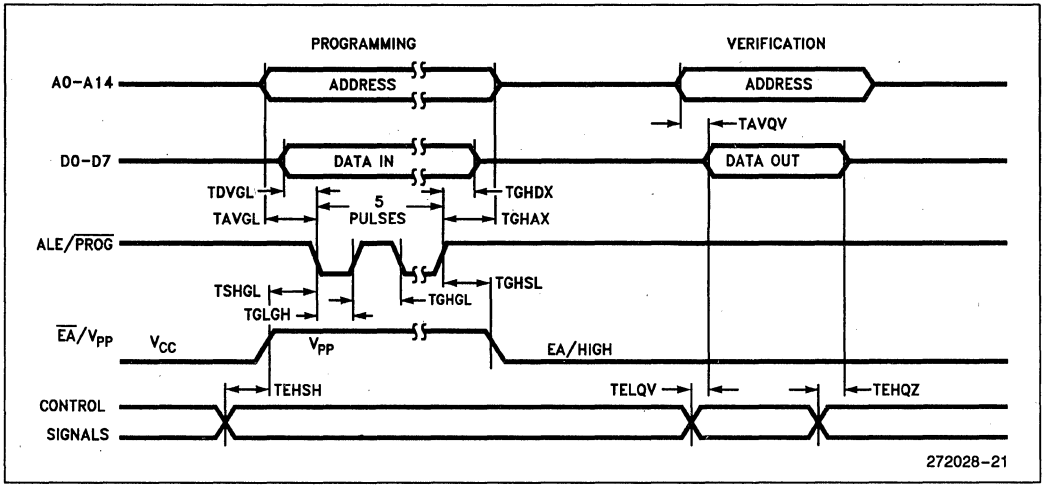
EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



DATA SHEET REVISION SUMMARY

The following differences exist between this data sheet (272028-002) and the previous version (272028-001):

1. Added 87C51FC-3/83C51FC-3 to 20 MHz data sheet.
2. Added EXPRESS version of 8XC51FC-20/-3 to 20 MHz data sheet.
3. Data sheet title was changed from:

   87C51FC-20/83C51FC-20 20 MHz CHMOS Single-Chip 8-Bit Microcontroller with 32 Kbytes User Programmable EPROM

   to:

   87C51FC-20/-3 83C51FC-20/-3 Commercial/Express 20 MHz Microcontroller
4. Added process information after block diagram.
5. θ_{ja} and θ_{jc} information added to Packages Table.
6. Variable Oscillator equations in External Memory Characteristics Table changed as follows:

	From	To
TLLIV	120	125
	4TCLCL−80	4TCLCL−75
TPLIV	3TCLCL−95	3TCLCL−90
TWHQX	0	10
	TCLCL−50	TCLCL−40
TQVWH	200	280
	7TCLCL−150	7TCLCL−70

The following differences exist between revision 1 of the 87C51FC-20/83C51FC-20 (272028-001) data sheet and the 87C51FC/83C51FC (270789-002) data sheet:

1. QFP package added.
2. Pins labeled "NC" changed to "Reserved" on the PLCC pinout.
3. Timer 2 Programmable Clock Out paragraph added.
4. RRST specification in DC Characteristics Table changed from 40 KΩ min, 225 KΩ max to 50 KΩ min, 300 KΩ max.
5. 20 MHz extension added to Figure 3.
6. 12 MHz Oscillator timings changed to 20 MHz in External Program Memory Characteristics and Serial Port Timing Tables.
7. Variable Oscillator equations in External Program Memory Characteristics Table changed as follows:

	From	To
TLLIV	4TCLCL − 100	4TCLCL − 80
TPLIV	3TCLCL − 105	3TCLCL − 95
TPXIZ	TCLCL − 25	TCLCL − 20
TRLDV	5TCLCL − 165	5TCLCL − 95
TLLDV	8TCLCL − 150	8TCLCL − 90
TAVDV	9TCLCL − 165	9TCLCL − 90
TAVWL	4TCLCL − 130	4TCLCL − 90
TQVWX	TCLCL − 50	TCLCL − 35

8. TXHQX in the Serial Port Timing Table changed from (2TCLCL − 117) to (2TCLCL − 50).

8XC51GB Hardware Description and Data Sheets

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intel®

September 1992

87C51GB
Hardware Description

9

Order Number: 270897-003

87C51GB Hardware Description

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1.0 INTRODUCTION TO THE 8XC51GB

The 8XC51GB is a highly integrated 8-bit microcontroller based on the MCS®-51 architecture. As a member of the MCS-51 family, the 8XC51GB is optimized for control applications. Its key features are an analog to digital converter and two programmable counter arrays (PCA) capable of measuring and generating pulse information on ten I/O pins. Also included are an enhanced serial port for multi-processor communications, a serial expansion port, hardware watchdog timer, oscillator fail detection, an up/down timer/counter and a program lock scheme for the on-chip program memory. Since the 8XC51GB is CHMOS, it has two software selectable reduced power modes: Idle Mode and Power Down Mode.

The 8XC51GB used the standard 8051 instruction set and is functionally compatible with the existing MCS-51 family of products.

This document presents a comprehensive description of the on-chip hardware features of the 8XC51GB. It begins with a discussion of how the memory is organized, followed by the instruction set, and then discusses each of the peripherals listed below.

- Six 8-bit Bidirectional Parallel Ports
- Three 16-bit Timer/Counters with
  - One Up/Down Timer/Counter
  - Programmable Clock Output
- Analog to Digital Converter with
  - 8 channels
  - 8-bit resolution
  - compare mode
- Two Programmable Counter Arrays with
  - Compare/Capture
  - Software Timer
  - High Speed Output
  - Pulse Width Modulator
  - Watchdog Timer (PCA only)
- Full-Duplex Programmable Serial Port with
  - Framing Error Detection
  - Automatic Address Recognition
- Serial Expansion Port
  - four programmable modes
  - four selectable frequencies
- Hardware Watchdog Timer
- Reset
  - asynchronous
  - active low
- Oscillator Fail Detection
- Interrupt Structure with
  - 15 interrupt sources
  - Four priority levels
- Power-Saving Modes
  - Idle Mode
  - Power Down Mode

The table below summarizes the product names of the various 8XC51GB products currently available. Throughout this document, the products will generally be referred to as the 8XC51GB. Figure 1 shows a functional block diagram of the 8XC51GB.

ROM Device	OTP Version	ROMless Version	ROM/ OTP Bytes	RAM Bytes
87C51GB	87C51GB	80C51GB	8K	256

2.0 MEMORY ORGANIZATION

All MCS-51 devices have a separate address space for Program Memory and Data Memory. The logical separation of Program and Data Memory allows the Data Memory to be accessed by 8-bit addresses, which can be more quickly stored and manipulated by an 8-bit CPU. Nevertheless, 16-bit Data Memory addresses can also be generated through the DPTR register. Up to 64 Kbytes each of external Program and Data Memory can be addressed.

2.1 Program Memory

Program Memory can only be read, not written to. There can be up to 64 Kbytes of Program Memory. The read strobe for external Program Memory is the signal $\overline{PSEN}$ (Program Store Enable). $\overline{PSEN}$ is not activated for internal program fetches.

If the $\overline{EA}$ (External Access) pin is connected to V_{SS}, all program fetches are directed to external memory. For the ROMless devices, all program fetches must be to external memory. If the $\overline{EA}$ pin is connected to V_{CC}, then program fetches greater than 8K are to external addresses for the 8XC51GB products.

On the 87C51GB with $\overline{EA}$ connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are to internal ROM, and fetches to addresses 2000H through FFFFH are to external memory.

2.2 Data Memory

The 8XC51GB implements 256 bytes of on-chip data RAM. The memory space is divided into three blocks,

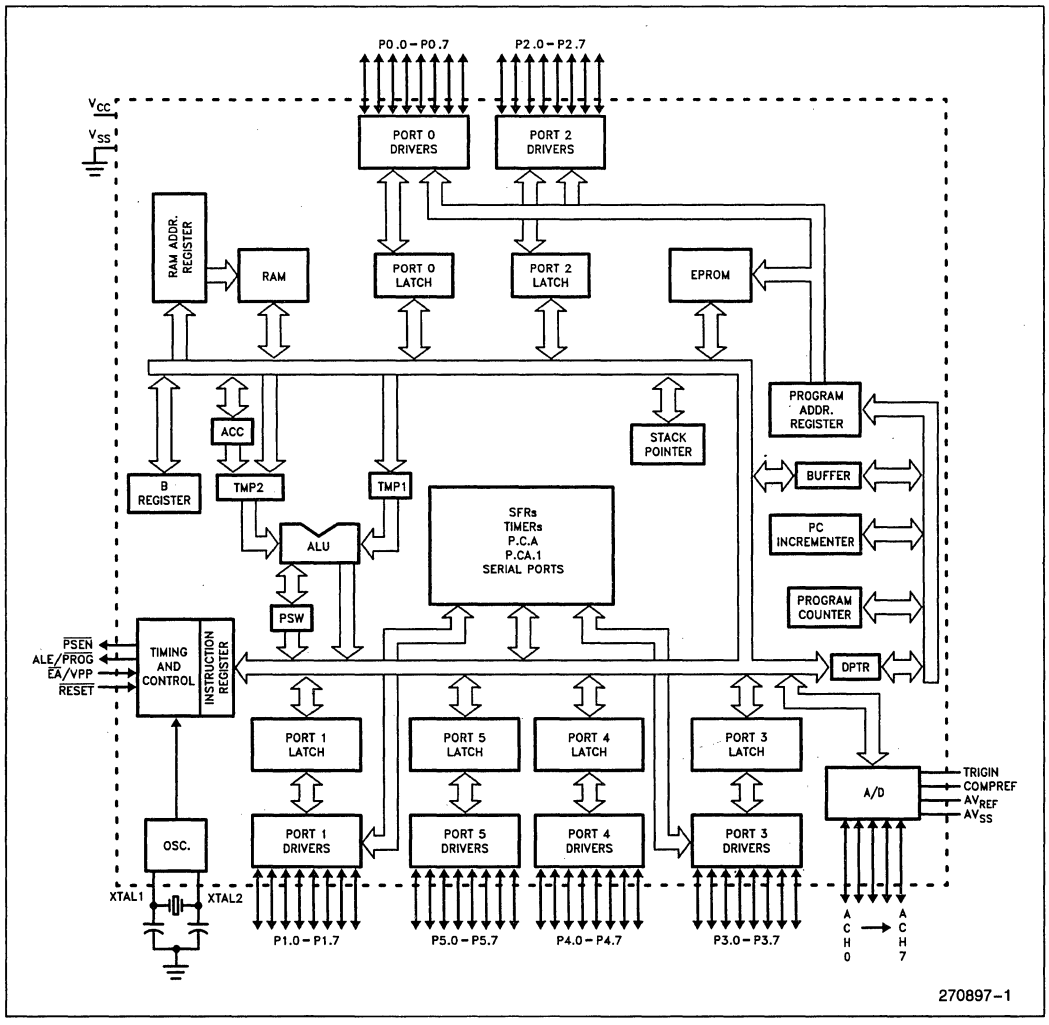

Figure 1. 87C51GB Block Diagram

which are generally referred to as the Lower 128, the Upper 128, and SFR space. The Upper 128 bytes occupy a parallel address space to the Special Function Registers. That means they have the same addresses, but they are physically separate from SFR space.

The Lower 128 bytes of RAM are present in all MCS-51 devices. All of the bytes in the Lower 128 can be accessed by either direct or indirect addressing. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example,

```
MOV 0A0H, data
```

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the upper 128 bytes of data RAM. For example,

```
MOV @R0, data
```

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where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H). Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

3.0 SPECIAL FUNCTION REGISTERS

A map of the on-chip memory area called by the SFR (Special Function Register) space is shown in Table 1. Special Function Registers (SFRs) include the Port latches, timers, peripheral controls, etc. These registers can only be accessed by direct addressing. Sixteen addresses in SFR space are both byte- and bit-addressable. The bit-addressable SFRs are those whose address ends in 000B. The bit addresses in this area are 80H through 0FFH.

Not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have no effect.

Table 1. SFR Mapping and Reset Values

F8	P5 00000000	CH 00000000	CCAP0H XXXXXXXX	CCAP1H XXXXXXXX	CCAP2H XXXXXXXX	CCAP3H XXXXXXXX	CCAP4H XXXXXXXX		FF
F0	*B 00000000				AD7 00000000			SEPSTAT XXXXX000	F7
E8	C1CON 00000000	CL 00000000	CCAP0L XXXXXXXX	CCAP1L XXXXXXXX	CCAP2L XXXXXXXX	CCAP3L XXXXXXXX	CCAP4L XXXXXXXX		EF
E0	*ACC 00000000				AD6 00000000			SEPDAT XXXXXXXX	E7
D8	CCON 00X00000	CMOD 00XXX000	CCAPM0 X0000000	CCAPM1 X0000000	CCAPM2 X0000000	CCAPM3 X0000000	CCAPM4 X0000000		DF
D0	*PSW 00000000				AD5 00000000			SEPCON XX000000	D7
C8	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	P4 00000000				AD4 00000000		EXICON X0000000	ACMP 00000000	C7
B8	*IP X0000000	SADEN 00000000	C1CAP0H XXXXXXXX	C1CAP1H XXXXXXXX	C1CAP2H XXXXXXXX	C1CAP3H XXXXXXXX	C1CAP4H XXXXXXXX	CH1 00000000	BF
B0	*P3 11111111				AD3 00000000	IPAH 00000000	IPA 00000000	IPH X0000000	B7
A8	*IE 00000000	SADDR 00000000	C1CAP0L XXXXXXXX	C1CAP1L XXXXXXXX	C1CAP2L XXXXXXXX	C1CAP3L XXXXXXXX	C1CAP4L XXXXXXXX	CL1 00000000	AF
A0	*P2 00000000				AD2 00000000	OSCR XXXXXXX0	WDTRST XXXXXXXX	IEA 00000000	A7
98	*SCON 00000000	*SBUF XXXXXXXX	C1CAPM0 X0000000	C1CAPM1 X0000000	C1CAPM2 X0000000	C1CAPM3 X0000000	C1CAPM4 X0000000	C1MOD XXXX0000	9F
90	*P1 00000000				AD1 00000000			ACON XX000000	97
88	*TCON 00000000	*TMOD 00000000	*TL0 00000000	*TL1 00000000	*TH0 00000000	*TH1 00000000			8F
80	*P0 11111111	*SP 00000111	*DPL 00000000	*DPH 00000000	AD0 00000000			*PCON** 00XX0000	87

* = Found in the 8051 core (see 8051 Hardware Description for explanations of these SFRs).
** = See description of PCON SFR. Bit PCON.4 is not affected by reset.
X = Undefined.

User software should not write 1's to these unimplemented locations, since they may be used in future MCS-51 products to invoke new features. In that case the reset or inactive values of the new bits will always be 0, and their active values will be 1.

The functions of the SFRs are outlined below. More information on the use of specific SFRs for each peripheral is included in the description of that peripheral.

Accumulator: ACC is the Accumulator register. The mnemonics for Accumulator-Specific instructions, however, refer to the Accumulator simply as A.

B Register: The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer: The Stack Pointer Register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. The stack may reside anywhere in on-chip RAM. On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Data Pointer: The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

Program Status Word: The PSW register contains program status information as detailed in Table 2.

Ports 0 to 5 Registers: P0, P1, P2, P3, P4, and P5 are the SFR latches of Ports 0 through 5 respectively.

Timer Registers: Register pairs (TH0, TL0), (TH1, TL1) and (TH2, TL2) are the 16-bit count registers for Timer/Counters 0, 1, and 2 respectively. Control and status bits are contained in registers TCON and TMOD for Timers 0 and 1 and in registers T2CON and T2MOD for Timer 2. The register pair (RCAP2H, RCAP2L) are the capture/reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Programmable Counter Array (PCA and PCA1) Registers: The 16-bit PCA and PCA1 timer/counters consist of register CH (CH1) and CL (CL1). Registers CCON (C1CON) and CMOD (C1MOD) contain the control and status bits for the PCA (and PCA1). The CCAPMn (n = 0, 1, 2, 3, or 4) and the C1CAPMn registers control the mode for each of the five PCA and the five PCA1 modules. The register pairs (CCAPnH, CCAPnL and C1CAPnH, C1CAPnL) are the 16-bit compare/capture registers for each PCA and PCA1 module.

Serial Port Registers: The Serial Data Buffer, SBUF, is actually two separate registers: a transmit buffer and a receive buffer register. When data is moved to SBUF, it comes from the receive buffer. Register SCON contains the control and status bits for the Serial Port. Registers SADDR and SADEN are used to define the Given and the Broadcast addresses for the Automatic Address Recognition feature.

Table 2. PSW: Program Status Word Register

PSW Address = 0D0H Reset Value = 0000 0000B

Bit Addressable

	CY	AC	F0	RS1	RS0	OV	—	P
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CY	Carry flag.
AC	Auxiliary Carry flag. (For BCD Operations)
F0	Flag 0. (Available to the user for general purposes).
RS1	Register bank select bit 1.
RS0	Register bank select bit 0.

RS1	RS0	Working Register Bank and Address
0	0	Bank 0 (00H–07H)
0	1	Bank 1 (08H–0FH)
1	0	Bank 2 (10H–17H)
1	1	Bank 3 (18H–1FH)

OV	Overflow flag.
—	User definable flag.
P	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the Accumulator, i.e., even parity.

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Serial Expansion Port Registers: The Serial Expansion Port is controlled through the register SEPCON. SEPDAT contains data for the Serial Expansion Port and SEPSTAT is used to monitor its status.

Interrupt Registers: The individual interrupt enable bits are in the IE and IEA registers. One of four priority levels can be selected for each interrupt using the IP, IPH, IPA and IPAH registers. The EXICON register controls the selection of the activation polarity for external interrupts two and three.

Analog to Digital Converter Registers: The results of A/D conversions are placed in registers AD0, AD1, AD2, AD3, AD4, AD5, AD6, and AD7 for analog channels 0 through 7 respectively. The register ACMP contains the results of the A/D comparison feature. ACON is the control register for A/D conversions.

Power Control Register: PCON controls the Power Reduction Modes, Idle and Power Down.

Oscillator Fail Detect Register: The OSCR register is used both to monitor the status of the OFD circuitry and to disable the feature.

Watchdog Timer Register: The WatchDog Timer ReSeT (WDTRST) register is used to keep the watchdog timer from periodically resetting the part.

Table 3. Alternate Port Functions

Port Pin	Alternate Function
P0.0/AD0–P0.7/AD7	Multiplexed Byte of Address/Data for external memory.
P1.0/T2	Timer 2 External Clock Input/Clockout
P1.1/T2EX	Timer 2 Reload/Capture/Direction Control
P1.2/ECI	PCA External Clock Input
P1.3/CEX0	PCA Module 0 Capture Input, Compare/PWM Output
P1.4/CEX1	PCA Module 1 Capture Input, Compare/PWM Output
P1.5/CEX2	PCA Module 2 Capture Input, Compare/PWM Output
P1.6/CEX3	PCA Module 3 Capture Input, Compare/PWM Output
P1.7/CEX4	PCA Module 4 Capture Input, Compare/PWM Output
P2.0/A8–P2.7/A15	High Byte of Address for External Memory
P3.0/RXD	Serial Port Input
P3.1/TXD	Serial Port Output
P3.2/$\overline{\text{INT0}}$	External Interrupt 0
P3.3/$\overline{\text{INT1}}$	External Interrupt 1
P3.4/T0	Timer 0 External Clock Input
P3.5/T1	Timer 1 External Clock Input
P3.6/$\overline{\text{WR}}$	Write Strobe for External Memory
P3.7/$\overline{\text{RD}}$	Read Strobe for External Memory
P4.0/SEPCLK	Clock Source for SEP
P4.1/SEPDAT	Data I/O for SEP
P4.2/ECI1	PCA1 External Clock Input
P4.3/C1EX0	PCA1 Module 0, Capture Input, Compare/PWM Output
P4.4/C1EX1	PCA1 Module 1, Capture Input, Compare/PWM Output
P4.5/C1EX2	PCA1 Module 2, Capture Input, Compare/PWM Output
P4.6/C1EX3	PCA1 Module 3, Capture Input, Compare/PWM Output
P4.7/C1EX4	PCA1 Module 4, Capture Input, Compare/PWM Output
P5.2/INT2	External Interrupt 2
P5.3/INT3	External Interrupt 3
P5.4/INT4	External Interrupt 4
P5.5/INT5	External Interrupt 5
P5.6/INT6	External Interrupt 6

NOTE:
The alternate functions can only be activated if the corresponding bit latch in the port SFR contains a 1. Otherwise the port pin will not go high.

4.0 I/O PORTS

All six ports in the 8XC51GB are bidirectional. Each consists of a latch (Special Function Register P0 through P5), output driver and an input buffer. All the ports, except for Port 0, have Schmitt Trigger inputs.

The output drivers of Ports 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise the Port 2 pins continue to emit the P2 SFR content.

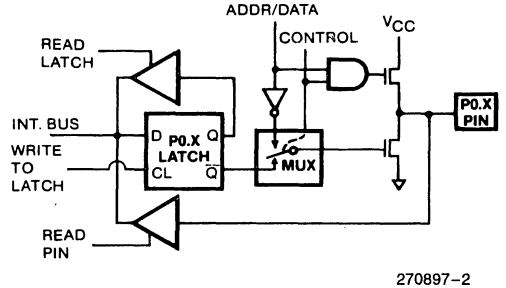
All the Port 1, Port 3, Port 4 and most of Port 5 pins are multi-functional. They are not only port pins, but also serve the functions of various special features as shown in Table 3.

4.1 I/O Configurations

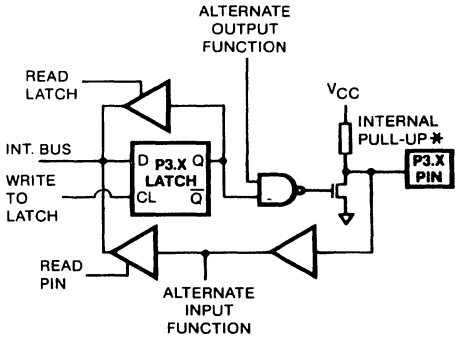
Functional diagrams of a bit latch and I/O buffer in each of the four ports are shown in Figure 2.

The bit latch (one bit in the port's SFR) is represented as a Type D flip-flop, which clocks in a value from the internal bus in response to a "write to latch" signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a "read latch" signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a "read pin" signal from the CPU. Some instructions that read a port activate the "read latch" signal, and others activate the "read pin" signal. Those that read the latch are the Read-Modify-Write instructions.

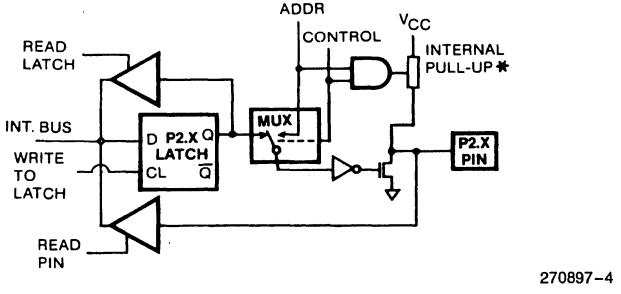
The output drivers of Ports 0 and 2 are switchable to an internal ADDRESS and ADDRESS/DATA bus by an internal control signal for use in external memory accesses. During external memory accesses, the P2 SFR



A. Port 0 Bit



B. Port 1, 3, 4, or 5 Bit



C. Port 2 Bit

*See Figure 4 for details of the internal pullup.

Figure 2. 8XC51GB Port Bit Latches and I/O Buffers

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remains unchanged, but the P0 SFR gets 1s written to it.

If a P1 through P5 latch contains a 1, then the output level is controlled by the signal labeled "alternate output function." The pin level is always available to the pin's alternate input function, if any.

Ports 1 through 5 have internal pullups. Port 0 has open drain outputs. Each I/O line can be independently used as an input or an output (Ports 0 and 2 may not be used as general purpose I/O when being used as the ADDRESS/DATA BUS). To be used as an input, the port bit latch must contain a 1, which turns off the output driver FET. On Ports 1 through 5 the pin is pulled high by the internal pullup, but can be pulled low by an external source.

P1, P2, P4, and P5 reset to a low state. While in reset these pins can sink large amounts of current. If these ports are to be used as inputs and externally driven high while in reset, the user should be aware of possible contention. A simple solution is to use open collector interfaces with these port pins or to buffer the inputs.

Port 0 differs from the other ports in not having internal pullups. The pullup FET in the P0 output driver is used only when the port is emitting 1s during external memory accesses. Otherwise the pullup FET is off. Consequently P0 lines that are being used as output port lines are open drain. Writing a 1 to the bit latch leaves both output FETs off, which floats the pin and allows it to be used as a high-impedance input. Because Ports 1 through 5 have fixed internal pullups they are sometimes called "quasi-bidirectional" ports.

When configured as inputs they pull high and will source current (I_{IL} in the data sheets) when externally pulled low. Port 0, on the other hand, is considered "true" bidirectional, because it floats when configured as an input.

The latches for ports 0 and 3 have 1s written to them by the reset function. If a 0 is subsequently written to a port latch, it can be reconfigured as an input by writing a 1 to it.

4.2 Writing to a Port

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during State 6, Phase 2 of the final cycle of the instruction. However, port latches are sampled by their output buffers only during Phase 1 of any clock period. (During Phase 2 the output buffer holds the value it saw during the previous Phase 1). Consequently, the new value in the port latch won't actually appear at the output pin until the next Phase 1, which will be at S1P1 of the next machine cycle. Refer to Figure 3.

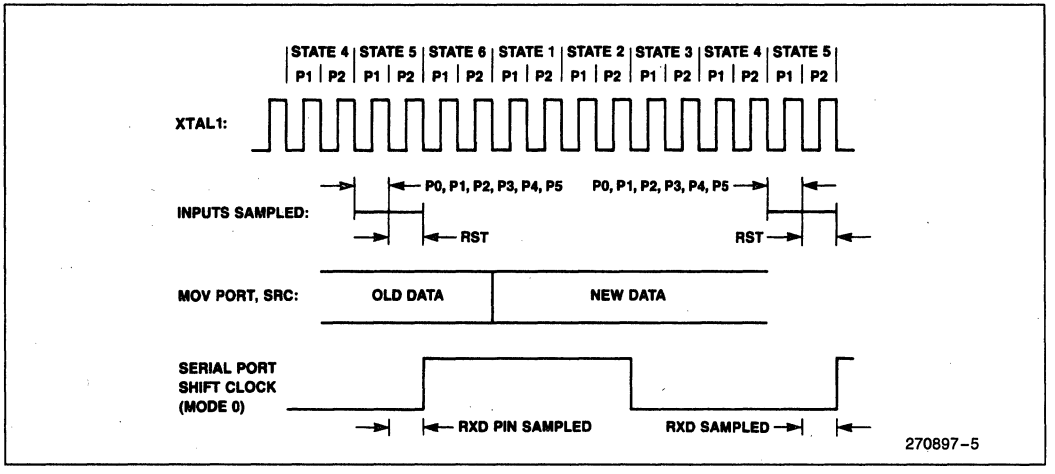


Figure 3. Port Operation

For more information on internal timings refer to the CPU Timing section.

If the change requires a 0-to-1 transition in Ports 1 through 5, an additional pullup is turned on during S1P1 and S1P2 of the cycle in which the transition occurs. This is done to increase the transition speed. The extra pullup can source about 100 times the current that the normal pullup can. The internal pullups are field-effect transistors, not linear resistors. The pullup arrangements are shown in Figure 4.

The pullup consists of three pFETs. Note that an n-channel FET (nFET) is turned on when a logical 1 is applied to its gate, and is turned off when a logical 0 is applied to its gate. A p-channel FET (pFET) is the opposite: it is on when its gate sees a 0, and off when its gate sees a 1.

pFET 1 is the transistor that is turned on for 2 oscillator periods after a 0-to-1 transition in the port latch. A 1 at the port pin turns on pFET3 (a weak pullup), through the inverter. This inverter and pFET form a latch which hold the 1.

If the pin is emitting a 1, a negative glitch on the pin from some external source can turn off pFET2, causing the pin to go into a float state. pFET2 is a very weak pullup which is on whenever the nFET is off, in traditional CMOS style. It's only about $1/10$ the strength of pFET2. Its function is to restore a 1 to the pin in the event the pin had a 1 and lost it to a glitch.

4.3 Port Loading and Interfacing

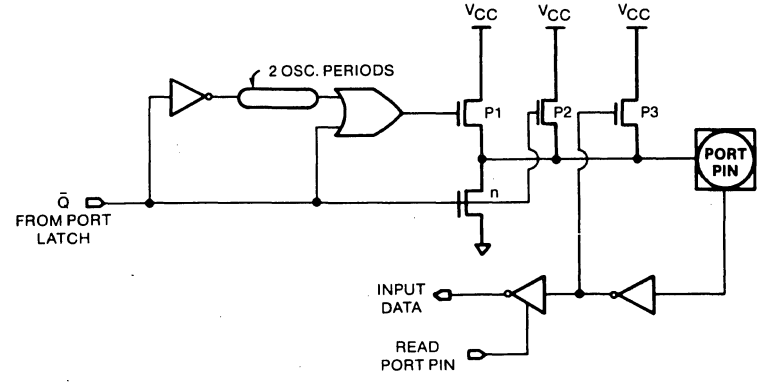
The output buffers of Ports 1 through 5 can each sink at least the amount of current specified by V_{OL} in the data sheet. These port pins can be driven by open-collector and open-drain outputs although 0-to-1 transitions will not be fast since there is little current pulling the pin up. An input 0 turns off pullup pFET2, leaving only the very weak pullup pFET2 to drive the transition.

In external bus mode, Port 0 output buffers can each sink the amount of current specified at the test conditions for VOL1 in the data sheet. However, as port pins they require external pullups to be able to drive any inputs.

See the latest revision of the data sheet for design-in information.

4.4 Read-Modify-Write Instructions

Some instructions that read a port read the latch and others read the pin. Which ones do which? The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called "read-modify-write" instructions. Listed on the following page, are the read-modify-write instructions. When the destination



NOTE:
CHMOS Configuration. pFET 1 is turned on for 2 osc. periods after $\overline{Q}$ mades a 0-to-1 transition. During this time, pFET 1 also turns on pFET 3 through the inverter to form a latch which holds the 1. pFET 2 is also on. Port 2 is similar except that it holds the strong pullup on while emitting 1s that are address bits. (See text, "Accessing External Memory".)

Figure 4. Ports 1, 3, 4, and 5 Internal Pullup Configuration

operand is a port, or a port bit, these instructions read the latch rather than the pin:

ANL	(logical AND, e.g. ANL P1, A)
ORL	(logical OR, e.g. ORL P2, A)
XRL	(logical EX-OR, e.g. XRL P3, A)
JBC	(jump if bit = 1 and clear bit, e.g. JBC P1.1, LABEL)
CPL	(complement bit, e.g. CPL P3.0)
INC	(increment, e.g. INC P2)
DEC	(decrement, e.g. DEC P2)
DJNZ	(decrement and jump if not zero, e.g. DJNZ P3, LABEL)
MOV PX.Y, C	(move carry bit to bit Y of Port X)
CLR PX.Y	(clear bit Y of Port X)
SETB PX.Y	(set bit Y of Port X)

It is not obvious that the last three instructions in this list are read-modify-write instructions, but they are. They read the port byte, all 8 bits, modify the addressed bit, then write the new byte back to the latch.

The reason that read-modify-write instructions are directed to the latch rather than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. When a 1 is written to the bit, the transistor is turned on. If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1.

4.5 Accessing External Memory

Accesses to external memory are of two types: accesses to external Program Memory and accesses to external Data Memory. Accesses to external Program Memory use signal $\overline{PSEN}$ (program store enable) as the read strobe. Accesses to external Data Memory use $\overline{RD}$ or $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory. Refer to Figures 5 through 7.

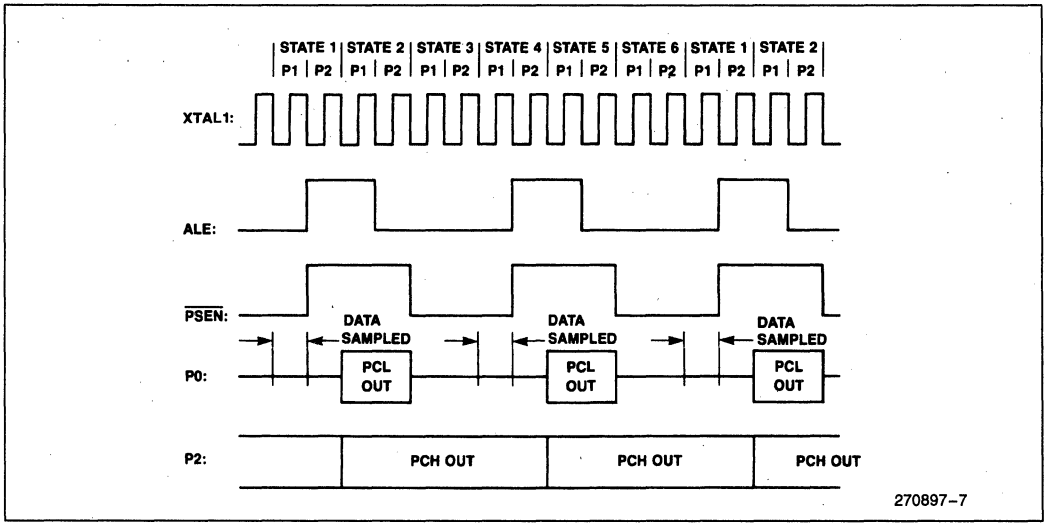


Figure 5. External Program Memory Fetches

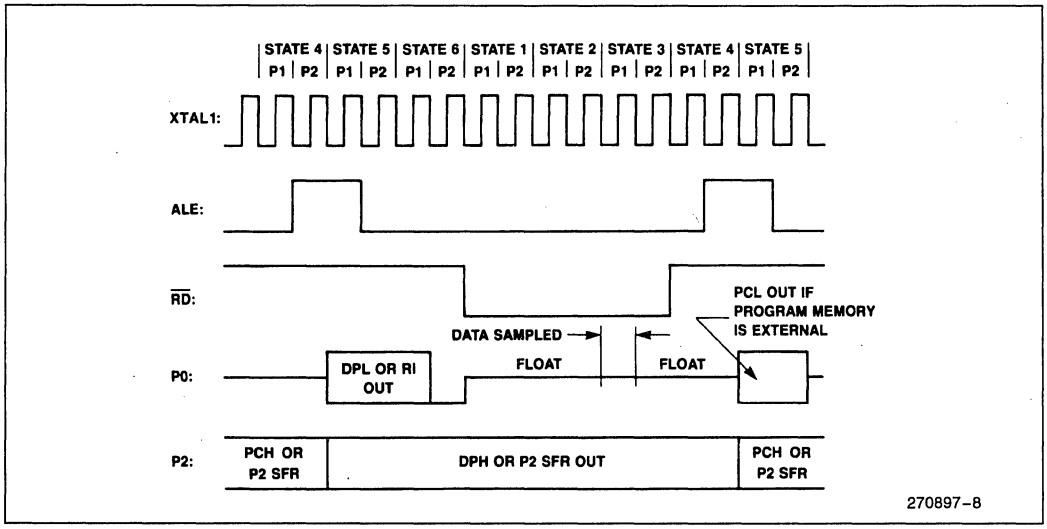


Figure 6. External Data Memory Read Cycle

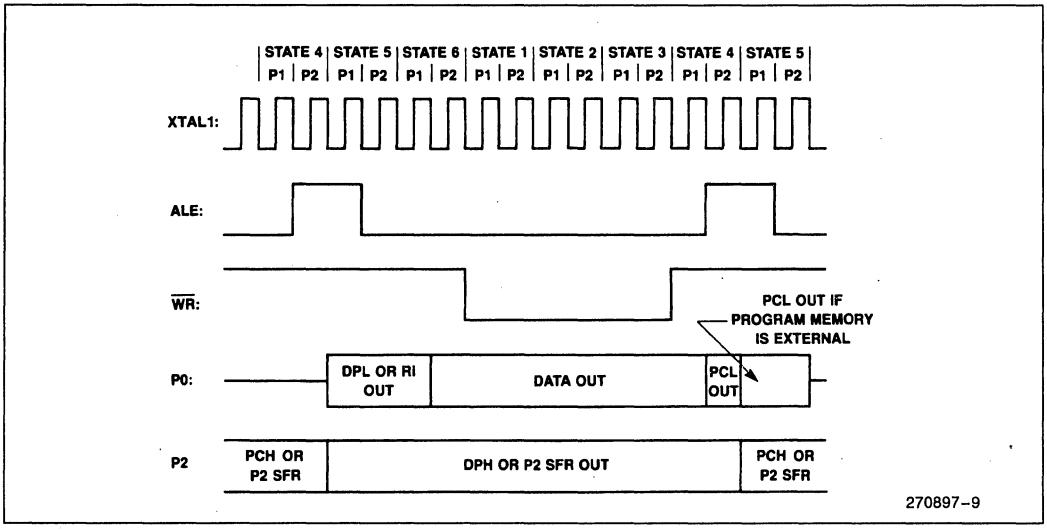


Figure 7. External Data Memory Write Cycle

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Fetches from external Program Memory always use a 16-bit address. Accesses to external Data Memory can use either a 16-bit address (MOVX @ DPTR) or an 8-bit address (MOVX @ Ri).

Whenever a 16-bit address is used, the high byte of the address comes out on Port 2, where it is held for the duration of the read or write cycle. The Port 2 drivers use the strong pullups during the entire time that they are emitting address bits that are 1s. This occurs when the MOVX @ DPTR instruction is executed. During this time the Port 2 latch (the Special Function Register) does not have to contain 1s, and the contents of the Port 2 SFR are not modified. If the external memory cycle is not immediately followed by another external memory cycle, the undisturbed contents of the Port 2 SFR will reappear in the next cycle.

If an 8-bit address is being used (MOVX @ Ri), the contents of the Port 2 SFR remain at the Port 2 pins throughout the external memory cycle. In this case, Port 2 pins can be used to page the external data memory.

In either case, the low byte of the address is time-multiplexed with the data byte on Port 0. The ADDRESS/DATA signal drives both FETs in the Port 0 output buffers. Thus, in external bus mode the Port 0 pins are not open-drain outputs and do not require external pullups. The ALE (Address Latch Enable) signal should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe ($\overline{RD}$) is deactivated.

During any access to external memory, the CPU writes 0FFH to the Port 0 latch (the Special Function Register), thus obliterating the information in the Port 0 SFR. Also, a MOV P0 instruction must not take place during external memory accesses. If the user writes to Port 0 during an external memory fetch, the incoming code byte is corrupted. Therefore, do not write to Port 0 if external program memory is used.

External Program Memory is accessed under two conditions:

1. Whenever signal $\overline{EA}$ is high, or
2. Whenever the program counter (PC) contains an address greater than 1FFFH (8K).

This requires that the ROMless versions have $\overline{EA}$ wired to V_{SS} to enable the lower 8K of program bytes to be fetched from external memory.

When the CPU is executing out of external Program Memory, all 8 bits of Port 2 are dedicated to an output function and may not be used for general purpose I/O. During external program fetches they output the high byte of the PC with the Port 2 drivers using the strong pullups to emit bits that are 1s.

5.0 TIMER/COUNTERS

The 8XC51GB has three 16-bit Timer/Counters: Timer 0, Timer 1, and Timer 2. Each consists of two 8-bit registers: THx and TLx with x = 0, 1, or 2. All three can be configured to operate either as timers or event counters.

In the Timer function, the TLx register is incremented every machine cycle. Thus, you can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin: T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 0 and Timer 1 have four operating modes:

Mode 0: 13-bit timer

Mode 1: 16-bit timer

Mode 2: 8-bit auto-reload timer

Mode 3: Timer 0 as two separate 8-bit timers

Also, its possible to use Timer 1 to generate baud rates.

Timer 2 has three modes of operation:

Timer 2 Capture

Timer 2 Auto-Reload (up or down counting), and

Timer 2 as a Baud Rate Generator

5.1 Timer 0 and Timer 1

The Timer/Counter function is selected by control bits C_Tx in TMOD (Table 4). These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1x, M0x) also in TMOD. Mode 0, Mode 1, and Mode 2 are the same for both Timer/Counters. Mode 3 operation is different for the two timers.

Table 4. TMOD: Timer/Counter Mode Control Register

TMOD Address = 89H Reset Value = 0000 0000B

Not Bit Addressable

	TIMER 1				TIMER 0			
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
GATE	Gating control when set. Timer/Counter 0 or 1 is enabled only while $\overline{INT0}$ or $\overline{INT1}$ pin is high and TR0 or TR1 control pin is set. When cleared, Timer 0 or 1 is enabled whenever TR0 or TR1 control bit is set.
C/$\overline{T}$	Timer or Counter Selector. Clear for Timer operation (input from internal system clock). Set for Counter operation (input from T0 or T1 input pin).

M1	M0	Operating Mode
0	0	8-bit Timer/Counter. THx with TLx as 5-bit prescaler.
0	1	16-bit Timer/Counter. THx and TLx are cascaded; there is no prescaler.
1	0	8-bit auto-reload Timer/Counter. THx holds a value which is to be reloaded into TLx each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter stopped.

MODE 0

Either Timer 0 or Timer 1 in Mode 0 is an 8-bit counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Figure 8 shows the Mode 0 operation for either timer.

As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF0 or TF1. The counted input is enabled to the timer when TR0 or TR1 = 1, and either GATEx = 0 or $\overline{INTx}$ pin = 1. (Setting GATEx = 1 allows the Timer to be controlled by external input $\overline{INTx}$ pin, to facilitate pulse width measurements).

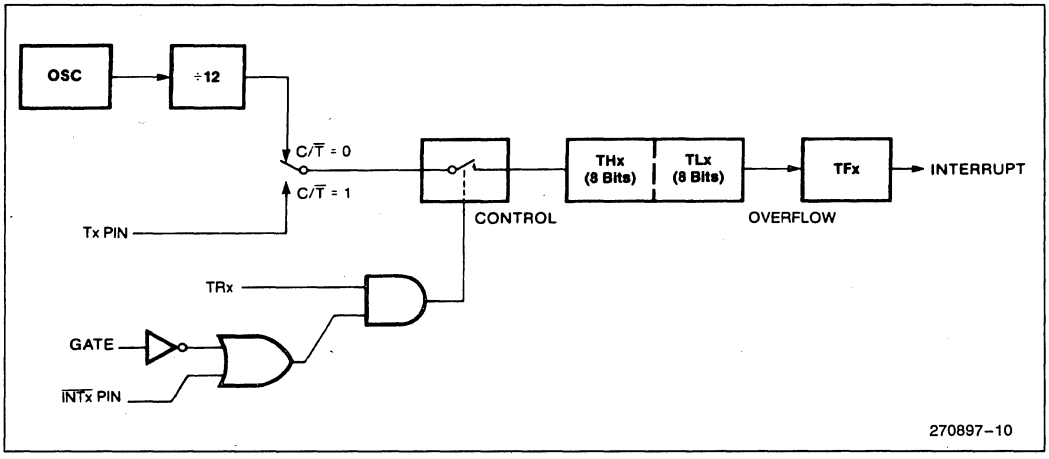

Figure 8. Timer/Counter 0 or 1 in Mode 0: 13-Bit Counter

TRx and TFx are control bits in the SFR TCON. The GATEx bits are in TMOD. There are two different GATE bits: one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

The 13-bit register consists of all 8 bits of THx and the lower 5 bits of TLx. The upper 3 bits of TLx are indeterminate and should be ignored. Setting the run flag (TRx) does not clear these registers.

MODE 1

Mode 1 is the same as Mode 0, except that the Timer register uses all 16-bits. In this mode, THx and TLx are cascaded; there is no prescaler. Refer to Figure 9.

As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF0 or TF1. The counted input is enabled to the timer when TR0 or TR1 = 1, and either GATEx = 0 or $\overline{INTx}$ pin = 1. (Setting GATEx = 1

Table 5. TCON: Timer/Counter Control Register

TCON Address = 88H Reset = 0000 0000B

Bit Addressable

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
7	6	5	4	3	2	1	0

Symbol	Function
TF1	Timer 1 overflow Flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter 1 on/off.
TF0	Timer 0 overflow Flag. Set by hardware on Timer/Counter 0 overflow. Cleared by hardware when processor vectors to interrupt routine.
TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter 0 on/off.
IE1	Interrupt 1 flag. Set by hardware when external interrupt 1 edge is detected (transmitted or level-activated). Cleared when interrupt processed only if transition-activated.
IT1	Interrupt 1 Type control bit. Set/cleared by software to specifiy falling edge/low level triggered external interrupt 1.
IE0	Interrupt 0 flag. Set by hardware when external interrupt 0 edge is detected (transmitted or level-activated). Cleared when interrupt processed only if transition-activated.
IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt 0.

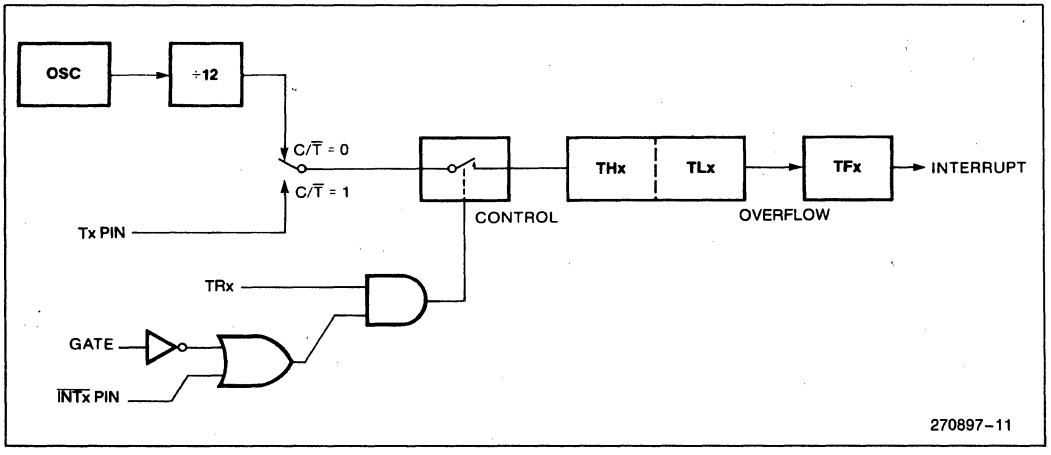

Figure 9. Timer/Counter 0 or 1 in Mode 1: 16-Bit Counter

allows the Timer to be controlled by external input $\overline{INTx}$ pin to facilitate pulse width measurements).

TRx and TFx are control bits in the SRF TCON. The GATEx bits are in TMOD. There are two different GATE bits: one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

MODE 2

Mode 2 configures the Timer register as an 8-bit Counter (TLx) with automatic reload as shown in Figure 10. Overflow from TLx not only sets TFx, but also reloads TLx with the contents of THx, which is preset by software. The reload leaves THx unchanged.

The counted input is enabled to the timer when TR0 or TR1 = 1, and either GATEx = 0 or $\overline{INTx}$ pin = 1. (Setting GATEx = 1 allows the Timer to be controlled by external input $\overline{INTx}$ pin, to facilitate pulse width measurements).

TRx and TFx are control bits in the SFR TCON. The GATEx bits are in TMOD. There are two different GATE bits: one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

MODE 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. TL0 uses the Timer 0 control bits: C_T0, GATE0, TR0, and TF0. TH0 is locked into a

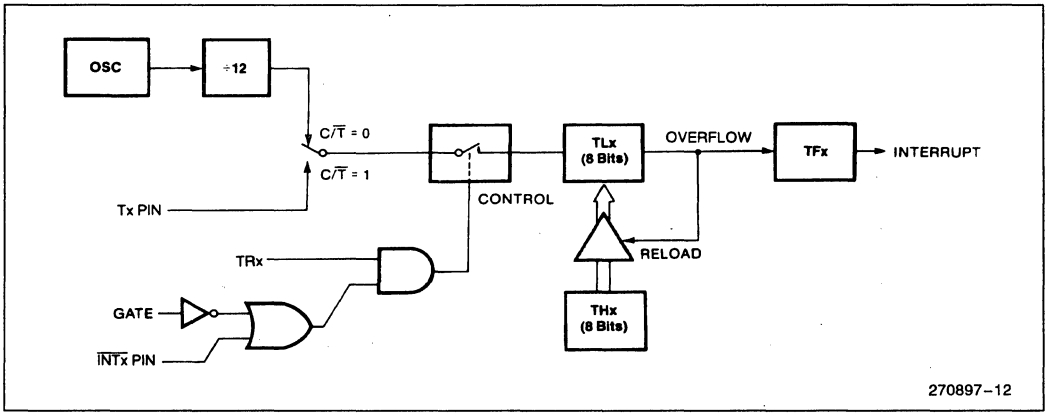

Figure 10. Timer/Counter 1 Mode 2: 8-Bit Auto-Reload

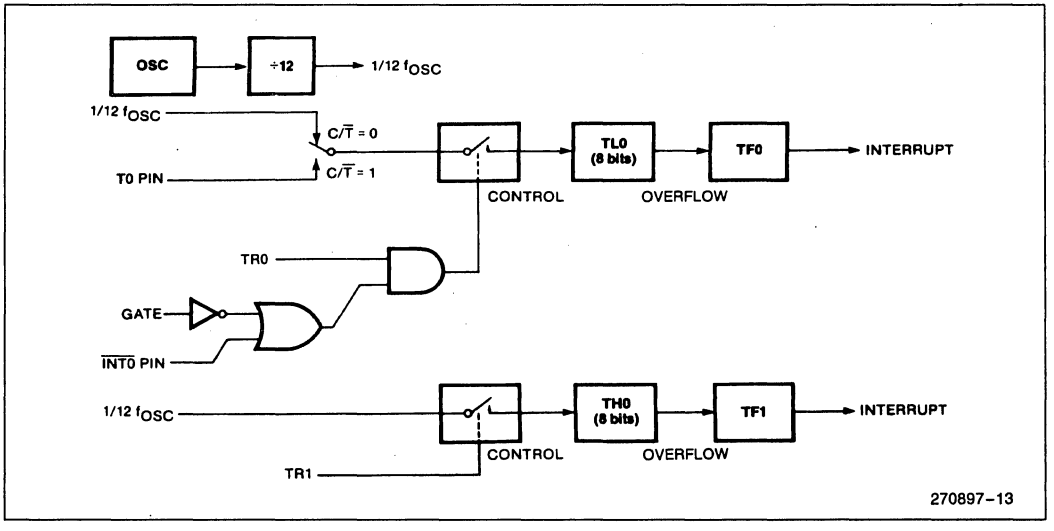

Figure 11. Timer/Counter 0 Mode 3: Two 8-Bit Counters

timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus TH0 now controls the Timer 1 interrupt. The logic for Mode 3 on Timer 0 is shown in Figure 11.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

5.2 Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate either as a timer or as an event counter. This is selected by bit C_T2 in the SFR T2CON (Table 7). It has the following three operating modes:

Timer 2 Capture,

Timer 2 Auto-Reload (up or down counting), and

Timer 2 as a Baud Rate Generator.

The modes are also selected by bits in T2CON as shown in Table 6.

Table 6. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	T2*OE	TR2	Mode
0	0	0	1	16-Bit Auto-Reload
0	1	0	1	16-Bit Capture
1	X	X	1	Baud_Rate Generator
X	0	1	1	Clock-Out on P1.0*
X	X	X	0	Timer Off

*Present only on the 87C51FC.

Table 7. T2CON: Timer/Counter 2 Control Register

T2CON Address = 0C8H Reset Value = 0000 0000B

Bit Addressable

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	Timer or counter select, (Timer 2) 0 = Internal timer (OSC/12 or OSC/2 in baud rate generator mode.) 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload flag. When set, captures will occur on negative transition at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

The T2 Pin has another alternate function on the 87C51GB. It can be configured as a Programmable Clock Out.

TIMER 2 CAPTURE MODE

In the capture mode there are two options selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer on counter which, upon overflow, sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers (TH2 and TL2) to be captured into registers RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. Figure 12 illustrates this.

TIMER 2 AUTO-RELOAD (UP OR DOWN COUNTER)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by a bit named DCEN (Down Counter Enable) located in the SFR T2MOD (see Table 8). Upon reset the DCEN bit is set to 0 so that Timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down depending on the value of the T2EX pin.

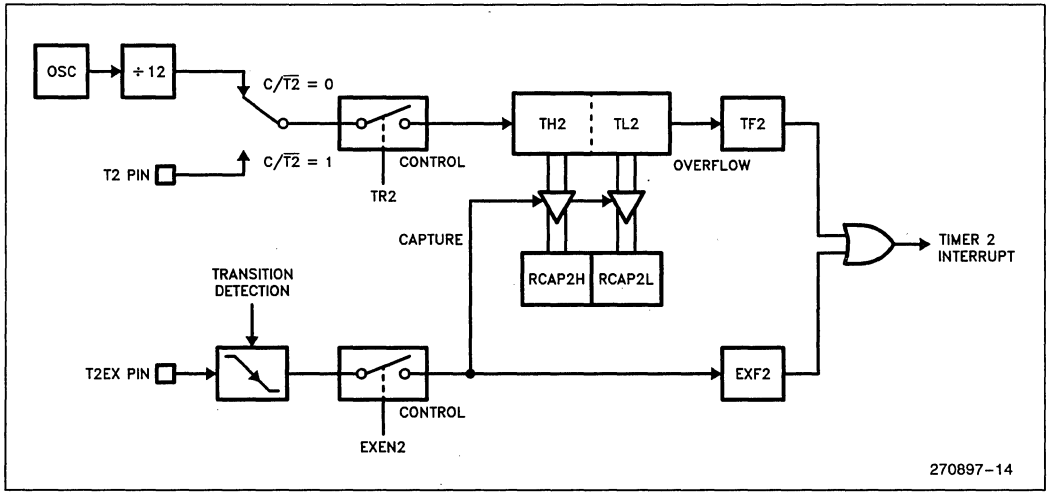

Figure 12. Timer 2 in Capture Mode

Table 8. T2MOD: Timer 2 Mode Control Register

T2MOD Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

—	—	—	—	—	—	T2OE	DCEN
Bit 7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.*
T2OE	Timer 2 Output Enable bit.
DECN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter

*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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In the auto-reload mode with DCEN = 0, there are two options selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Either the TF2 or EXF2 bit can generate the Timer 2 interrupt if it is enabled. Figure 13 shows timer 2 automatically counting up when DCEN = 0.

Setting the DCEN bit enables Timer 2 to count up or down as shown in Figure 14. In this mode the T2EX pin controls the direction of count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit which can then generate an interrupt if it is enabled. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. Now the timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The under-

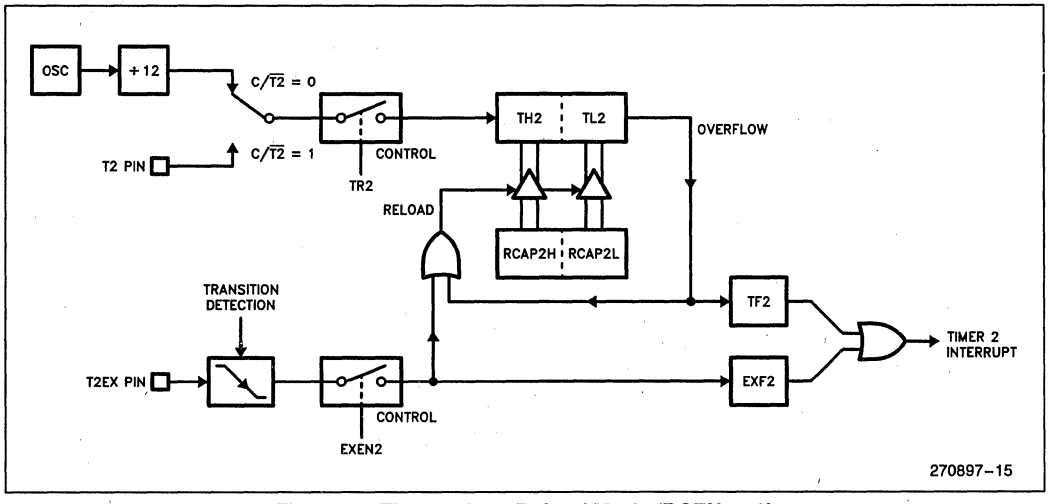

Figure 13. Timer 2 Auto Reload Mode (DCEN = 0)

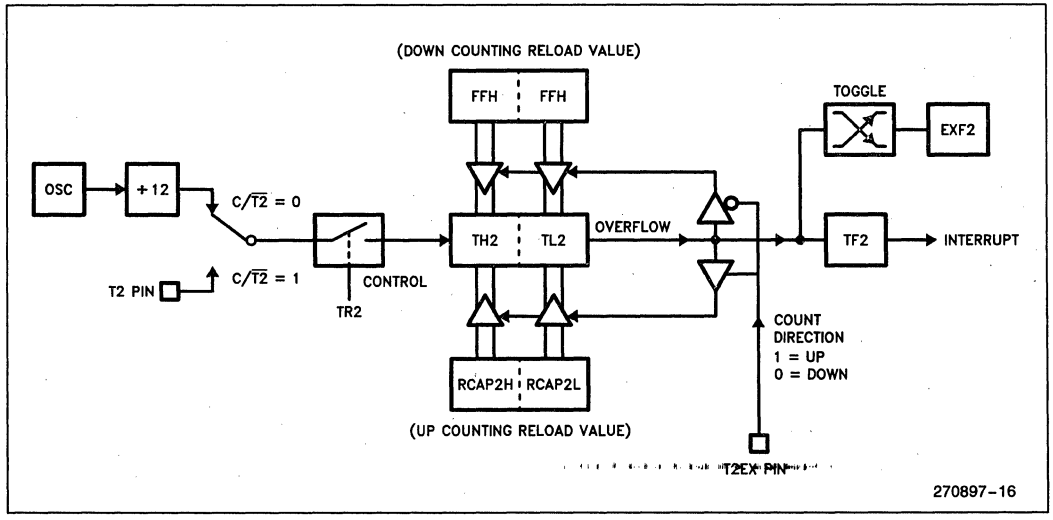

Figure 14. Timer 2 Auto Reload Mode (DCEN = 1)

flow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows. This bit can be used as a 17th bit of resolution if desired. In this operating mode, EXF2 does not generate an interrupt.

5.3 Programmable Clock Out

The 87C51GB has a new feature. A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed (1) to input the external clock for Timer/Counter 2, or (2) to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency. Figure 15 shows Timer 2 in clock-out mode.

To configure the Timer/Counter 2 as a clock generator, bit C_T2 (in T2CON) must be cleared and bit T2OE (in T2MOD) must be set. Bit TR2 (in T2CON) also must be set to start the timer.

The Clock Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

In the Clock Out mode, Timer 2 roll-overs wi: generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the clock-out frequency will be the same.

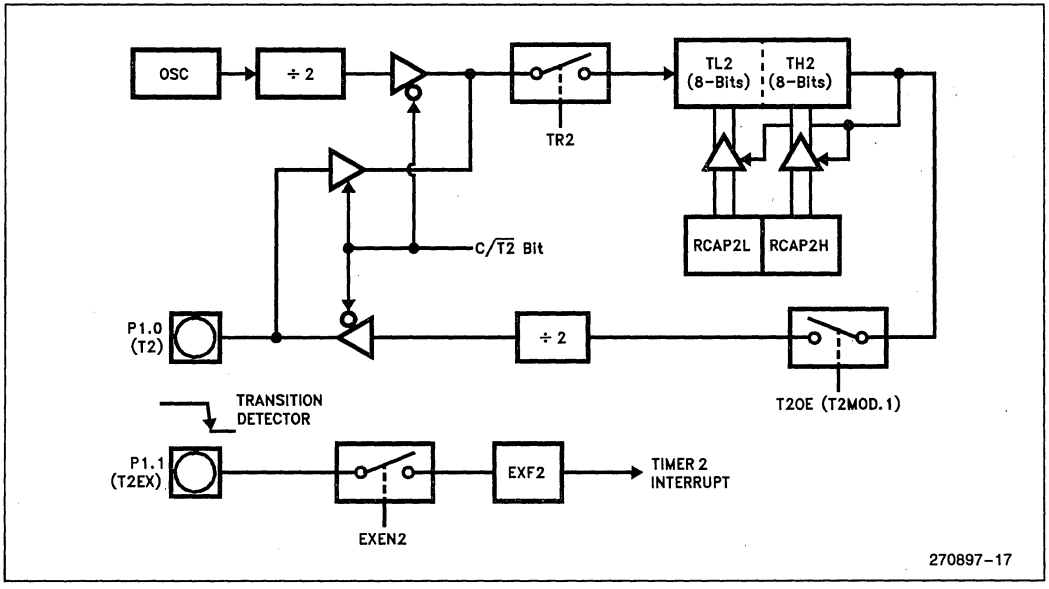

Figure 15. Timer 2 in Clock-Out Mode

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6.0 A/D CONVERTER

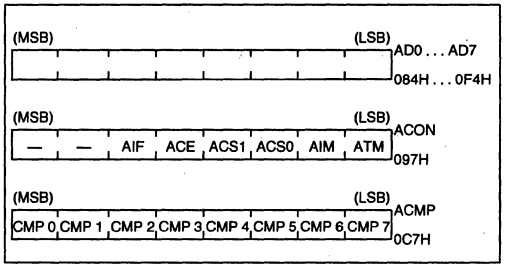
The A/D converter on the 8XC51GB consists of: 8 analog inputs (ACH0–ACH7), an external trigger input (TRIGIN), separate analog voltage supplies (AV_{SS} and AV_{REF}), a comparison reference input (COMPREF) and internal circuitry. The internal circuitry includes: an 8 channel multiplexer, a 256 element resistive ladder, a comparator, sample-and-hold capacitor, successive approximation register, A/D trigger control, a comparison result register and 8 A/D result registers as shown in the A/D block diagram, Figure 16.

AV_{REF} must be held within the tolerances stated on the 8XC51GB data sheet. The accuracy of the A/D cannot be improved, for instance, by tying AV_{REF} to ½ the voltage on V_{CC}.

6.1 A/D Special Function Registers

The A/D has 10 SFRs associated with it. The SFRs are shown in Table 9.

Table 9. A/D SFRs



AD0 through AD7 contain the results of the 8 analog conversion. Each SFR is updated as each conversion is complete, starting with the lowest channel and ending with channel 7.

ACMP is the comparison result register. ACMP is organized differently than all the other SFRs in that CMP0 occupies the MSB and CMP7 the LSB. CMP0

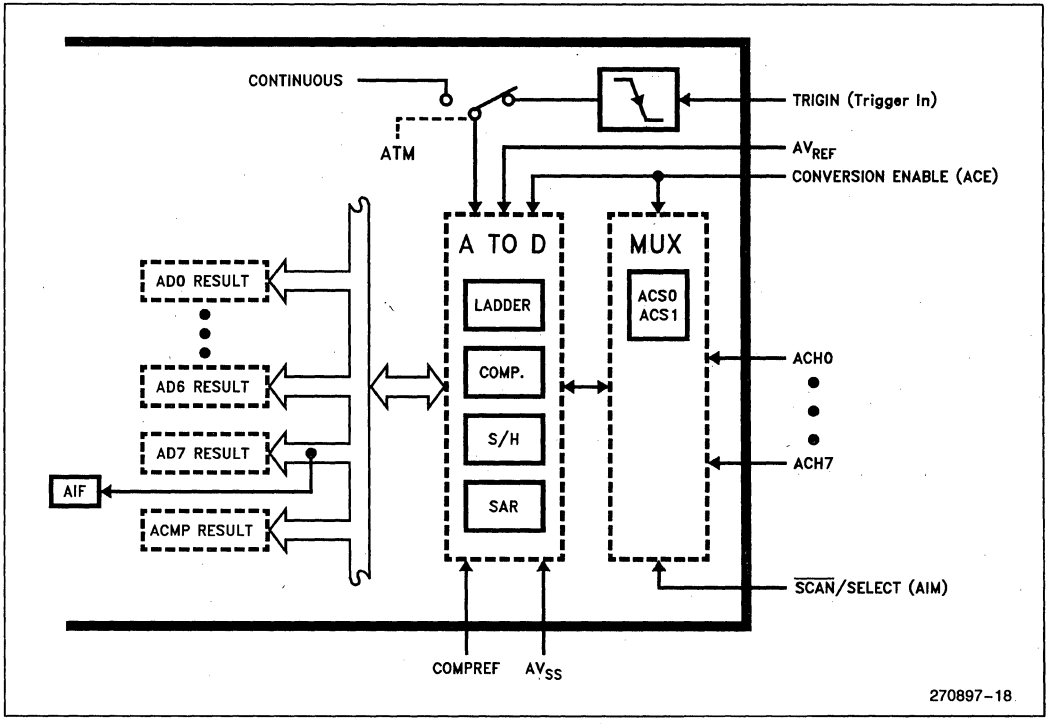


Figure 16. A/D Block Diagram

through CMP7 correspond to analog inputs 0 through 7. CMPn is set to a 1 if the analog input is greater than COMPREF. CMPn is cleared if the analog input is less than or equal to COMPREF.

ACON is the A/D control register and contains the A/D Interrupt Flag (AIF), A/D Conversion Enable (ACE), A/D Channel Select (ACS0 and ACS1), A/D Input Mode (AIM), and A/D Trigger Mode (ATM).

6.2 A/D Comparison Mode

The A/D Comparison mode is always active while the A/D converter is enabled. The Comparison mode is used to compare each analog input against an external reference voltage applied to COMPREF. Whenever the A/D converter is triggered, each bit in ACMP is updated as each analog conversion is completed, starting with channel 0 up to channel 7 regardless of whether Select or Scan mode is invoked. The comparison mode can provide a quicker "greater-than or less-than" decision than can be performed with software and it is more code efficient. It can also be used to convert the analog inputs into digital inputs with a variable threshold. If the comparison mode is not used, COMPREF should be tied to V_{CC} or V_{SS}.

6.3 A/D Trigger Mode

The analog converter can be triggered either internally or externally. To enable internal trigger mode, ATM should be cleared.

When in internal trigger mode, A/D conversions begin in the machine cycle which follows the setting of the ACE bit. The lowest channel (see "A/D Input Modes" below) is converted first, followed by all the other channels in sequence. The AIF flag is set upon completion of the channel 7 conversion. AIF will flag an interrupt if the A/D interrupt is enabled. Once a conversion cycle is completed, a new cycle begins, starting with the lowest channel. If the user wishes each channel to be converted only once, the ACE bit should be cleared. Clearing ACE stops all A/D conversion activity. If a new A/D cycle begins, the result of the previous conversion will be overwritten.

In external mode, the A/D conversions begin when a falling edge is detected at the TRIGIN pin. There is no edge detector on the TRIGIN pin; is it sampled once every machine cycle.

A negative edge is recognized when TRIGIN is high in one machine cycle and low in the next. For this reason, TRIGIN should be held high for at least one machine cycle and low for one machine cycle. Once the falling edge is detected, the A/D conversions begin on the next machine cycle and complete when channel 7 is converted. After channel 7 is converted, AIF is set and the conversions halt until another trigger is detected while ACE = 1. External triggers are ignored while a conversion cycle is in progress.

6.4 A/D Input Modes

The 8XC51GB has two input modes: Scan mode and Select mode. Clearing AIM places the 8XC51GB in Scan mode. In Scan mode the analog conversions occur in the sequence ACH0, ACH1, ACH2, ACH3, ACH4, ACH5, ACH6, and ACH7. The result of each analog conversion is placed in the corresponding analog result register: AD0, AD1, AD2, AD3, AD4, AD5, AD6, and AD7.

Setting AIM activates Select mode. In Select mode, one of the lower 4 analog inputs (ACH0–ACH3) is converted four times. After the first four conversions are complete the cycle continues with ACH4 through ACH7. The results of the first four conversion are placed in the lower four result registers (AD0 through AD3). The rest of the conversions are placed in their matching result register. ACS0 and ACS1 determine which analog inputs are used as shown in Table 10.

Table 10. A/D Channel Selection

ACS1	ACS0	Selected Channel
0	0	ACH0
0	1	ACH1
1	0	ACH2
1	1	ACH3

6.5 Using the A/D with Fewer than 8 Inputs

There are several options for a user who wishes to convert fewer than eight analog input channels. If time is not critical the user can simply wait for the A/D interrupt to be generated by the AIF bit after channel 7 is converted and can ignore the results for unused channels. If a user needs to know the results of a conversion immediately after it occurs, a timer should be used to generate an interrupt. The amount of time required for each A/D conversion is specified in the 8XC51GB data sheet. The user could also periodically poll the result registers, provided he or she is looking only for a change in the analog voltage. Using the Select mode (see above) does not reduce the time required for a conversion cycle but will convert a given channel more frequently.

6.6 A/D in Power Down

The A/D on the 8XC51GB contains circuitry that limits the amount of current dissipated during Power Down mode to leakage current only. For this circuitry to function properly, AV_{REF} should be tied to V_{CC} during power down. The I_{PD} specification in the data sheet includes the current for the entire chip. While AV_{REF} is tied to V_{CC} during Power Down, the voltage may be reduced to the minimum voltage as shown in the data sheet.

7.0 PROGRAMMABLE COUNTER ARRAY

Programmable Counter Arrays (PCAs) provide more timing capabilities with less CPU intervention than the standard timer/counters. Their advantages include reduced software overhead and improved accuracy. For example, a PCA can provide better resolution than Timers 0, 1, and 2 because the PCA clock rate can be three times faster. A PCA can also perform many tasks that these hardware timers cannot (i.e. measure phase differences between signals or generate PWMs).

The 8XC51GB has two PCAs called PCA and PCA1. The following text and figures address only PCA but are also applicable to PCA1 with the following exceptions:

1. PCA1, Module 4 does not support the Watchdog Timer
2. All the SFRs and bits have 1s added to their names (see Table 11).
3. Port 4 is the interface for PCA1:

P4.2	ECI1
P4.3	C1EX1
P4.4	C1EX2
P4.5	C1EX2
P4.6	C1EX3
P4.7	C1EX4

Table 11. PCA and PCA1 SFRs

PCA	PCA1
SFRs:	
CCON	C1CON
CMOD	C1MOD
CCAPM0	C1CAPM0
CCAPM1	C1CAPM1
CCAPM2	C1CAPM2
CCAPM3	C1CAPM3
CCAPM4	C1CAPM4
CL	CL1
CCAP0L	C1CAP0L
CCAP1L	C1CAP1L
CCAP2L	C1CAP2L
CCAP3L	C1CAP3L
CCAP4L	C1CAP4L
CH	CH1
CCAP0H	C1CAP0H
CCAP1H	C1CAP1H
CCAP2H	C1CAP2H
CCAP3H	C1CAP3H
CCAP4H	C1CAP4H
BITS:	
ECI	ECI1
CEX0	C1EX0
CEX1	C1EX1
CEX2	C1EX2
CEX3	C1EX3
CEX4	C1EX4
CCF0	C1CF0
CCF1	C1CF1
CCF2	C1CF2
CCF3	C1CF3
CCF4	C1CF4
CR	CR1
CF	CF1

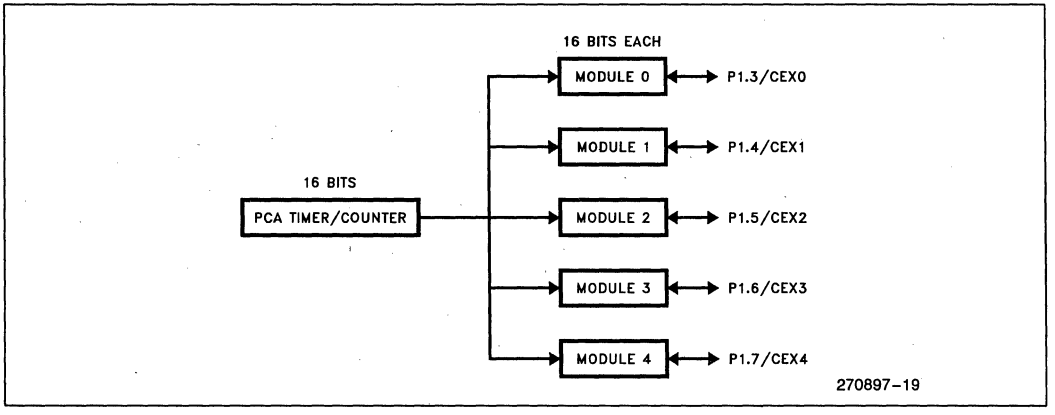


Figure 17. PCA Block Diagram

4. There has been one additional bit added to C1CON to allow both PCAs to be enabled simultaneously.

   The bit is called CRE and occupies bit position 5 of C1CN. Its bit address is 0EDH. When CRE is set, both CR and CR1 must be set to enable PCA1.

Each PCA consists of a 16-bit timer/counter and five 16-bit compare/capture modules as shown in Figure 17. The PCA timer/counter serves as a common time base for the five modules and is the only timer which can service the PCA. Its clock input can be programmed to count any one of the following signals:

Oscillator frequency / 12

Oscillator frequency / 4

Timer 0 overflow

External input on ECI (P1.2).

The compare/capture modules can be programmed in any one of the following modes:

rising and/or falling edge capture

software timer

high speed output

pulse width modulator.

Module 4 can also be programmed as a watchdog timer.

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated whenever the module executes its function. All five modules plus the PCA timer overflow share one PCA interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 pins for external I/O. These pins are listed below. If the port pin is not used for the PCA, it can still be used for standard I/O.

PCA Component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

7.1 PCA Timer/Counter

The PCA has a free-running 16-bit timer/counter consisting of registers CH and CL (the high and low bytes of the count value). These two registers can be read or written to at any time. Reading the PCA timer as a full 16-bit value simultaneously requires using one of the PCA modules in the capture mode and toggling a port pin in software.

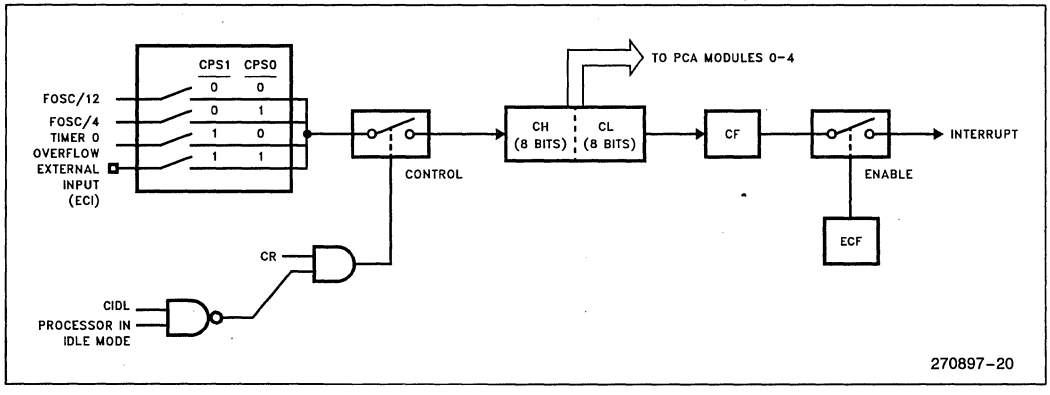


Figure 18. PCA Timer/Counter

The clock input can be selected from the following four modes:

Oscillator frequency / 12:

The PCA timer increments once per machine cycle. With a 16 MHz crystal, the timer increments every 750 ns.

Oscillator frequency / 4:

The PCA timer increments three times per machine cycle. With a 16 MHz crystal, the timer increments every 250 ns.

Timer 0 overflows:

The PCA timer increments whenever Timer 0 overflows. This mode allows a programmable input frequency to the PCA.

External input:

The PCA timer increments when a 1-to-0 transition is detected on the ECI pin (P1.2). The maximum input frequency in this mode is oscillator frequency / 8.

The mode register CMOD (Table 12) contains the Count Pulse Select bits (CPS1 and CPS0) to specify the clock input. This register also contains the ECF bit which enables the PCA counter overflow to generate the PCA interrupt. In addition, the user has the option of turning off the PCA timer during Idle Mode by setting the Counter Idle bit (CIDL). This can further reduce power consumption by an additional 30%.

The CCON (Table 13) register contains two more bits which are associated with the PCA timer/counter. The CF bit gets set by hardware when the counter overflows, and the CR bit is set or cleared to turn the counter on or off.

Table 12. CMOD: PCA Counter Mode Register

CMOD Address = 0D9H Reset Value = 00XX X000B

Not Bit Addressable

	CIDL	WDTE	—	—	—	CPS1	CPS0	ECF
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.
—	Not implemented, reserved for future use.*
CPS1	PCA Count Pulse Select bit 1.
CPS0	PCA Count Pulse Select bit 0.

CPS1	CPS0	Selected PCA Input**
0	0	Internal clock, Fosc÷12
0	1	Internal clock, Fosc÷4
1	0	Timer 0 overflow
1	1	External clock at ECI/P1.2 pin (max. rate = Fosc÷8)

ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
**Fosc = oscillator frequency

Table 13. CCON: PCA Counter Control Register

CCON Address = 0D8H Reset Value = 00X0 0000B

Bit Addressable

	CF	CR	—	CCF4	CCF3	CCF2	CCF1	CCF0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
—	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

***NOTE:**
User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

READING THE PCA TIMER

Some applications may require that the full 16-bit PCA timer value be read simultaneously. Since the timer consists of two 8-bit registers (CH, CL), it would normally take two MOV instructions to read the whole timer value. An invalid read could occur if the registers rolled over in between the execution of the two MOVs.

However, with the PCA Capture Mode the 16-bit timer value can be loaded into the capture registers by toggling a port pin. For example, configure Module 0 to capture falling edges and initialize P1.3 to be high. Then, when the user wants to read the PCA timer, clear P1.3 and the full 16-bit timer value will be saved in the capture registers. It's still optional whether the user wants to generate an interrupt with the capture.

7.2 Compare/Capture Modules

Each of the five compare/capture modules has six possible functions it can perform:

- 16-bit Capture, positive-edge triggered
- 16-bit Capture, negative-edge triggered
- 16-bit Capture, both positive and negative-edge triggered
- 16-bit Software Timer
- 16-bit High Speed Output
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer. The modules can be programmed in any combination of the different modes.

Each module has a mode register called CCAPMn (n = 0, 1, 2, 3, or 4) to select which function it will perform. The ECCFn bit enables the PCA interrupt when a module's event flag is set. The event flags (CCFn) are located in the CCON register and get set when a capture event, software timer, or high speed output event occurs for a given module.

Each module also has a pair of 8-bit compare/capture registers (CCAPnH and CCAPnL) associated with it. These registers store the time when a capture event occurred or when a compare event should occur. For the PWM mode, the high byte register CCAPnH controls the duty cycle of the waveform.

7.3 PCA Capture Mode

Both positive and negative transitions can trigger a capture with the PCA. This gives the PCA the flexibility to measure periods, pulse widths, duty cycles, and phase differences on up to five separate inputs. Setting the CAPPn and/or CAPNn bits in the CCAPMn mode register (Table 14) selects the input trigger—positive and/or negative transition—for module n. Refer to Figure 19.

Table 15 shows the combinations of bits in the CCAPMn register that are valid and have a defined function. Invalid combinations will produce undefined results.

Table 14. CCAPMn: PCA Modules Compare/Capture Registers

CCAPMn Address (n = 0–4): CCAPM0 0DAH, CCAPM1 0DBH, CCAPM2 0DCH, CCAPM3 0DDH, CCAPM4 0DEH — Reset Value = X000 0000B

Not Bit Addressable

	—	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Bit	7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented; reserved for future use*.
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case,the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Table 15. PCA Module Modes (CCAPMn Register)

—	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module Function
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a postive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative-edge trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	x	0	x	Watchdog Timer

X = Don't Care

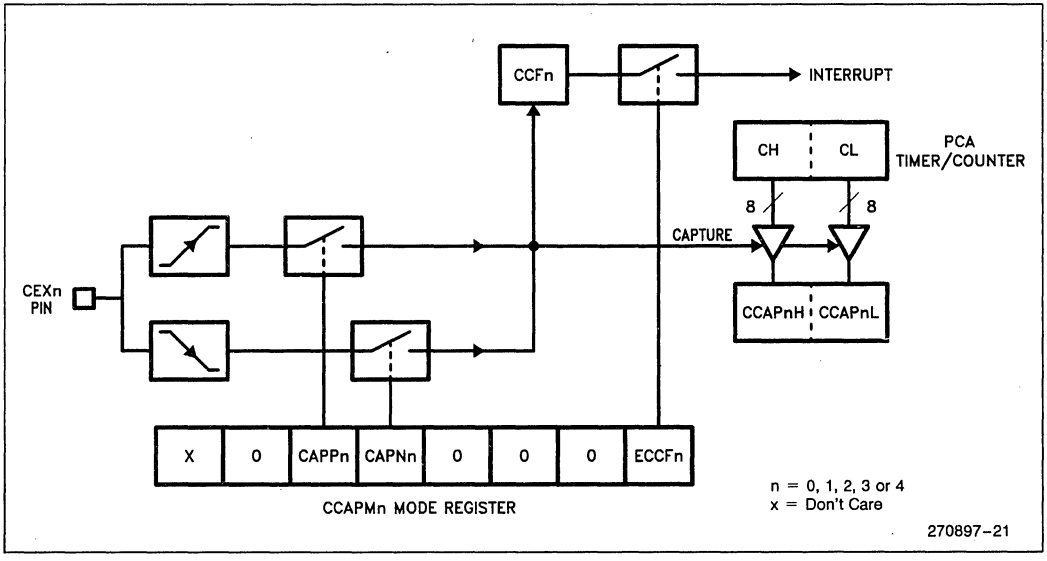


Figure 19. PCA 16-Bit Capture Mode

The external input pins CEX0 through CEX4 are sampled for a transition. When a valid transition is detected (positive and/or negative edge), hardware loads the 16-bit value of the PCA timer (CH, CL) into the module's capture registers (CCAPnH, CCAPnL). The resulting value in the capture registers reflects the PCA timer value at the time a transition was detected on the CEXn pin.

Upon a capture, the module's event flag (CCFn) in CCON is set, and an interrupt is flagged if the ECCFn bit in the mode register CCAPMn is set. The PCA interrupt will then be generated if it is enabled. Since the hardware does not clear an event flag when the interrupt is vectored to, the flag must be cleared in software.

In the interrupt service routine, the 16-bit capture value must be saved in RAM before the next capture event occurs. A subsequent capture on the same CEXn pin will write over the first capture value in CCAPnH and CCAPnL.

The time it takes to service this interrupt routine determines the resolution of back-to-back events with the same PCA module. To store two 8-bit registers and clear the event flags takes at least 9 machine cycles. That includes the call to the interrupt routine. At 12 MHz, this routine would take less than 10 μs. However, depending on the frequency and interrupt latency, the resolution will vary with each application.

7.4 Software Timer Mode

In most applications a software timer is used to trigger interrupt routines which must occur at periodic intervals. The user preloads a 16-bit value in a module's compare registers. When a match occurs between this compare value and the PCA timer value, an event flag is set and an interrupt can then be generated.

In the PCA compare mode, the 16-bit value of the PCA timer is compared with a 16-bit value pre-loaded in the module's compare registers (CCAPnH, CCAPnL) as seen in Figure 20. The comparison occurs three times per machine cycle in order to recognize the fastest possible clock input (i.e. $1/4 \times$ oscillator frequency). Setting the ECOMn bit in the mode register CCAPMn enables the comparator function.

For the Software Timer mode, the MATn bit also needs to be set. When a match occurs between the PCA timer and the compare registers, a match signal is generated and the module's event flag (CCFn) is set. An interrupt is then flagged if the ECCFn bit is set. The PCA interrupt is generated only if it has been properly enabled. Software must clear the event flag before the next interrupt will be flagged.

During the interrupt routine, a new 16-bit compare value can be written to the compare registers (CCAPnH and CCAPnL). Notice, however, that a write to CCAPnL clears the ECOMn bit which temporarily disables the comparator function while these registers are being updated so an invalid match does not occur. A write to CCAPnH sets the ECOMn bit and re-enables the comparator. For this reason, user software should write to CCAPnL first, then CCAPnH.

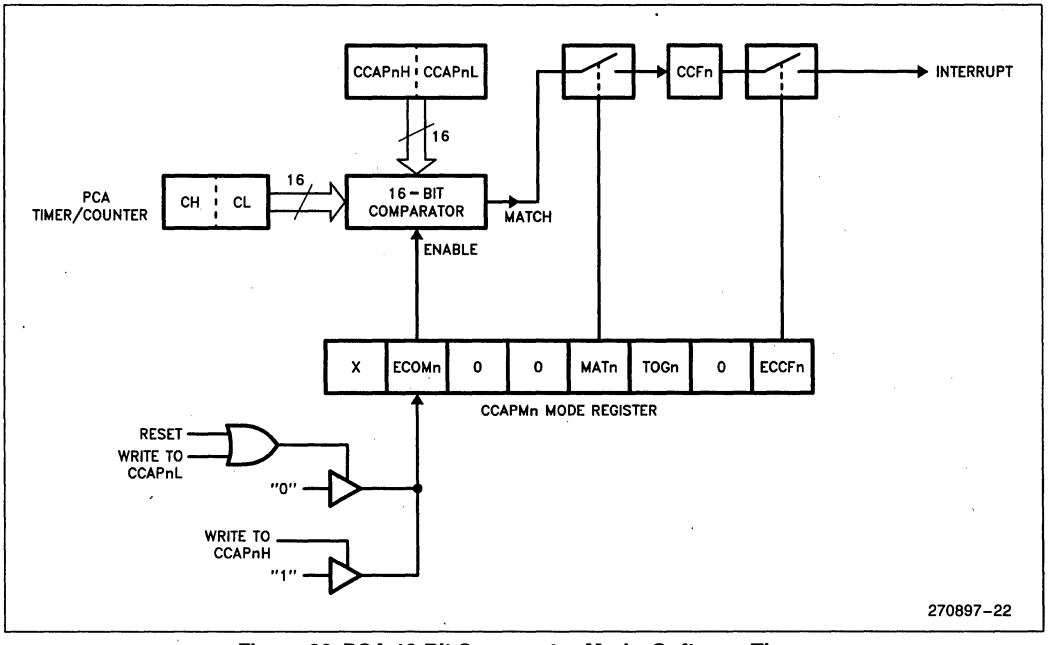


Figure 20. PCA 16-Bit Comparator Mode: Software Timer

7.5 High Speed Output Mode

The High Speed Output (HSO) mode toggles a CEXn pin when a match occurs between the PCA timer and a pre-loaded value in a module's compare registers. For this mode, the TOGn bit needs to be set in addition to the ECOMn and MATn bits in the CCAPMn mode register. By setting or clearing the pin in software, the user can select whether the CEXn pin will change from a logical 0 to a logical 1 or vice versa. The user also has the option of flagging an interrupt when a match event occurs by setting the ECCFn bit. See Figure 21.

The HSO mode is more accurate than toggling port pins in software because the toggle occurs before branching to an interrupt. That is, interrupt latency will not effect the accuracy of the output. In fact, the interrupt is optional. Only if the user wants to change the time for the next toggle is it necessary to update the compare registers. Otherwise, the next toggle will occur when the PCA timer rolls over and matches the last compare value.

Without any CPU intervention, the fastest waveform the PCA can generate with the HSO mode is a 30.5 Hz signal at 16 MHz.

7.6 Watchdog Timer Mode

A Watchdog Timer is a circuit that automatically invokes a reset unless the system being watched sends regular hold-off signals to the Watchdog. These circuits are used in applications that are subject to electrical noise, power glitches, electrostatic discharges, etc., or where high reliability is required.

The Watchdog Timer function is only available on PCA Module 4. If a Watchdog Timer is not needed, Module 4 can still be used in other modes.

As a Watchdog timer, every time the count in the PCA timer matches the value stored in module 4's compare registers, an internal reset is generated (see Figure 22). The bit that selects this mode is WDTE in the CMOD register. Module 4 must be set up in either compare mode as a "Software Timer" or High Speed Output.

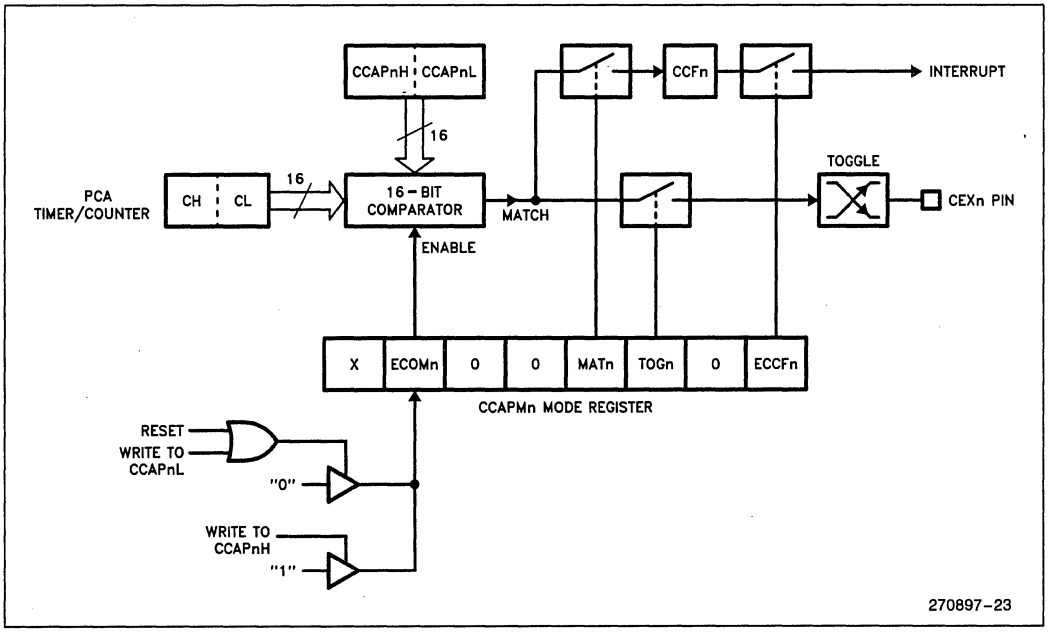


Figure 21. PCA 16-Bit Comparator Mode: High Speed Output

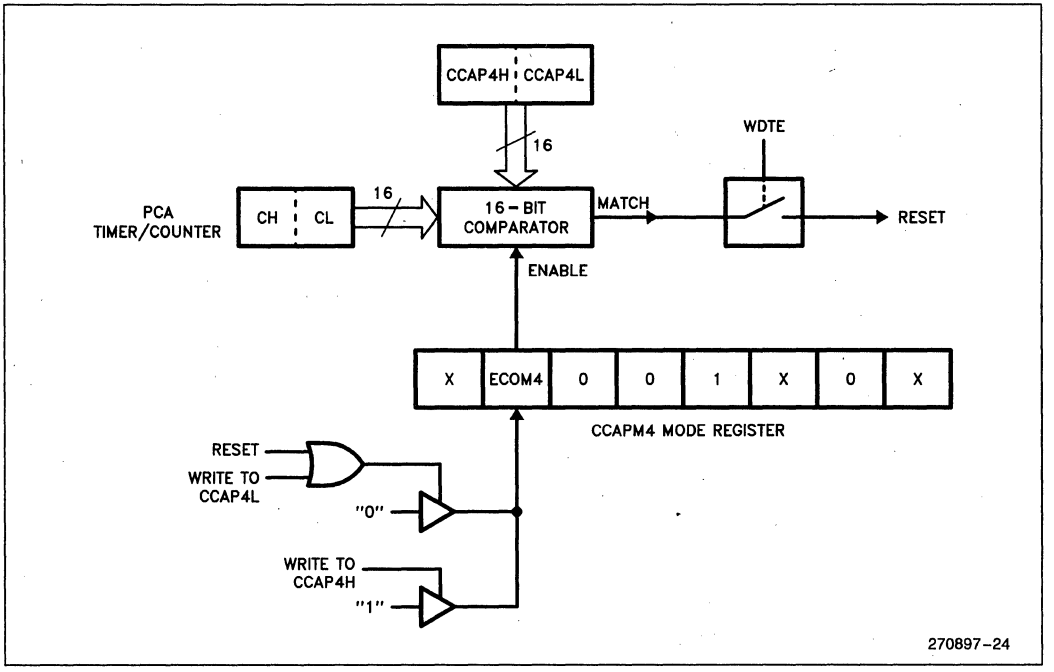


Figure 22. Watchdog Timer Mode

To hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare value,
3. disable the Watchdog by clearing the WDTE bit before a match occurs and then later re-enable it.

The first two options are more reliable because the Watchdog Timer is never disabled as in option #3. The second option is not recommended if other PCA modules are being used since this timer is the time base for all five modules. Thus, in most applications the first solution is the best option.

The watchdog routine should not be part of an interrupt service routine. Why? Because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced, and the watchdog will not reset the controller. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program within 65536 counts of the PCA timer.

7.7 Pulse Width Modulator Mode

Any or all of the five PCA modules can be programmed to be a Pulse Width Modulator. The PWM output can be used to convert digital data to an analog signal by simple external circuitry. The frequency of the PWM depends on the clock source for the PCA timer. With a 16 MHz crystal the maximum frequency of the PWM waveform is 15.6 KHz. Table 16 shows the various frequencies that are possible.

Table 16. PWM Frequencies

PCA Timer Mode	PWM Frequency	
	12 MHz	16 MHz
1/12 Osc. Frequency	3.9 KHz	5.2 KHz
1/4 Osc. Frequency	11.8 KHz	15.6 KHz
Timer 0 Overflow:		
8-bit	15.5 Hz	20.3 Hz
16-bit	0.06 Hz	0.08 Hz
8-bit Auto-Reload	3.9 KHz to 15.3 Hz	5.2 KHz to 20.3 Hz
External Input (Max)	5.9 KHz	7.8 KHz

For this mode, the ECOMn bit and the PWMn bits in the CCAPMn mode register need to be set. The PCA generates 8-bit PWMs by comparing the low byte of the PCA timer (CL) with the low byte of the module's compare registers (CCAPnL). When CL < CCAPnL the output is low. When CL > CCAPnL the output is high. Refer to Figure 23.

The value in CCAPnL controls the duty cycle of the waveform. To change the value in CCAPnL without output glitches, the user must write to the high byte register (CCAPnH). This value is then shifted by hardware into CCAPnL when CL rolls over from 0FFH to 00H which corresponds to the next period of the output.

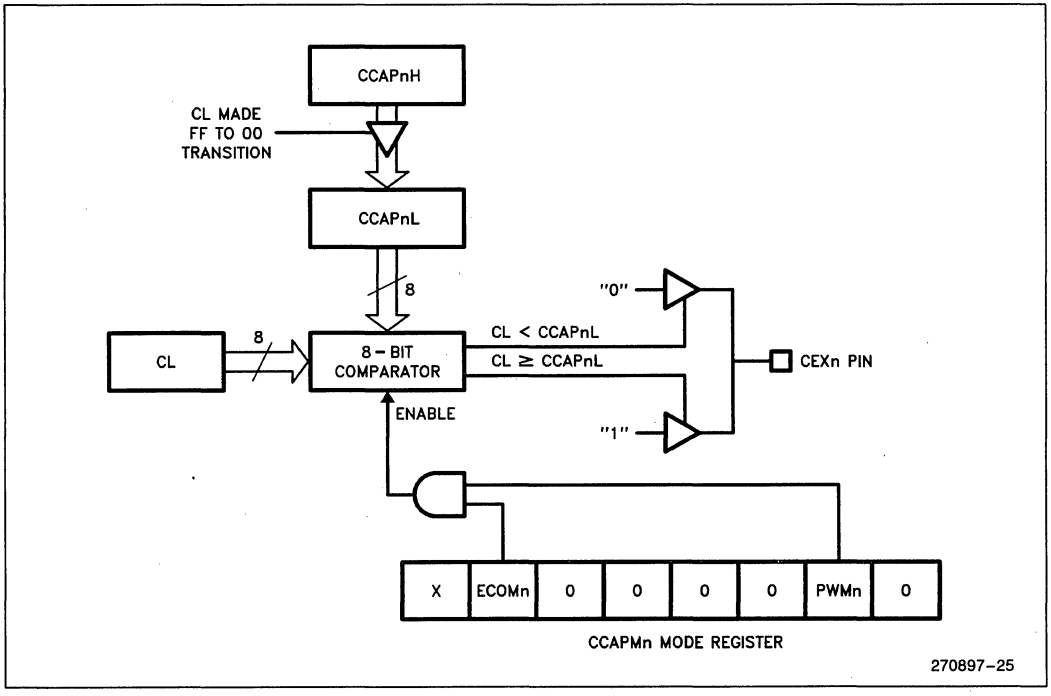


Figure 23. PCA 8-Bit PWM Mode

CCAPnH can contain any integer from 0 to 255 to vary the duty cycle from a 100% to 0.4%. A 0% duty cycle can be obtained by writing directly to the port pin with the CLR bit instruction. To calculate the CCAPnH value for a given duty cycle, use the following equation:

$$CCAPnH = 256 \times (1 - \text{Duty Cycle})$$

where CCAPnH is an 8-bit integer and Duty Cycle is expressed as a fraction. See Figure 24.

8.0 SERIAL PORT

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost).

The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Actually, SBUF is two separate registers, a transmit buffer and a receive buffer. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port control and status register is the Special Function Register SCON (Table 17). This register contains the mode selection bits (SM0 and SM1); the SM2 bit for the multiprocessor modes; the Receive Enable bit (REN); the 9th data bit for transmit and receive (TB8 and RB8); and the serial port interrupt bits (TI and RI).

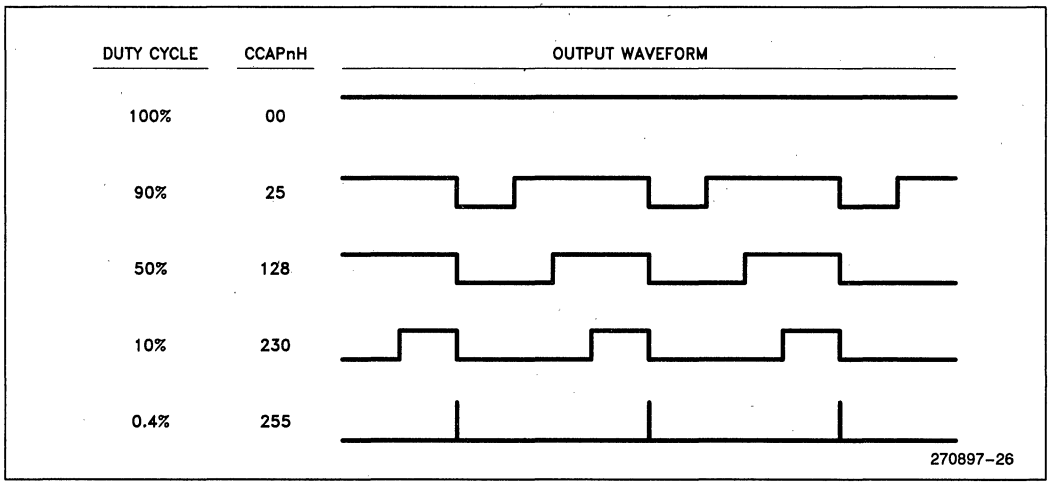


Figure 24. CCAPnH Varies Duty Cycle

Table 17. SCON: Serial Port Control Register

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
Bit:	7 (SMOD0 = 0/1)*	6	5	4	3	2	1	0

Symbol	Function
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0* bit must be set to enable access to the FE bit.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access SM0)
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	$F_{OSC}/12$
0	1	1	8-bit UART	variable
1	0	0	9-bit UART	$F_{OSC}/64$ or $F_{OSC}/32$
1	1	3	9-bit UART	variable

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Cleared by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1 if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0 or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTE:
*SMOD0 is located at PCON6.
**F_{OSC} = oscillator frequency

The serial port can operate in 4 modes:

Mode 0: Shift Register, fixed frequency

Mode 1: 8-Bit UART, variable frequency

Mode 2: 9-Bit UART, fixed frequency

Mode 3: 9-Bit UART, variable frequency

The baud rate in some modes is fixed and in others is generated by Timer 1 or Timer 2.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Mode 0: Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. The baud rate in Mode 1 is variable: you can use either Timer 1 to generate baud rates and/or Timer 2 to generate baud rates. Figure 25 shows the mode 1 Data Frame.

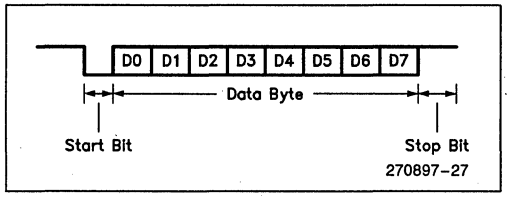


Figure 25. Mode 1 Data Frame

Mode 2: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in SCON, while the stop bit is ignored. (The validity of the stop bit can be checked with Framing Error Detection.) The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency. See Figure 26.

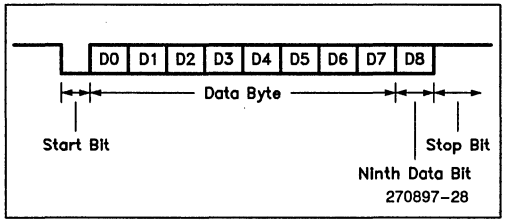


Figure 26. Mode 2 Data Frame

Mode 3: 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except the baud rate. The baud rate in Mode 3 is variable: you can use Timer 1 and/or Timer 2 to generate baud rates. See Figure 27.

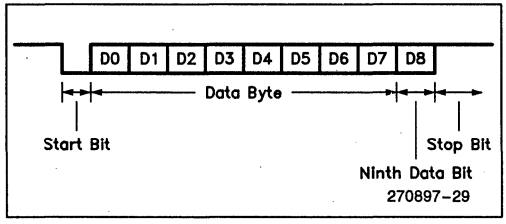


Figure 27. Mode 3 Data Frame

8.1 Framing Error Detection

Framing Error Detection allows the serial port to check for valid stop bits in modes 1, 2, or 3. A missing stop bit can be caused, for example, by noise on the serial lines, or transmission by two CPUs simultaneously.

If a stop bit is missing, a Framing Error bit (FE) is set. The FE bit can be checked in software after each reception to detect communication errors. Once set, the FE bit must be cleared in software. A valid stop bit will not clear FE.

The FE bit is located in SCON and shares the same bit address as SM0. Control bit SMOD0 in the PCON register determines whether the SM0 or FE bit is accessed. If SMOD0 = 0, then accesses to SCON.7 are to SM0. If SMOD0 = 1, then accesses to SCON.7 are to FE.

8.2 Multiprocessor Communications

Modes 2 and 3 provide a 9-bit mode to facilitate multiprocessor communication. The 9th bit allows the controller to distinguish between address and data bytes. The 9th bit is set to 1 for address and set to 0 for data bytes. When receiving, the 9th bit goes into RB8 in SCON. When transmitting, the ninth bit TB8 is set or cleared in software.

The serial port can be programmed such that when the stop bit is received the serial port interrupt will be activated only if the received byte is an address byte (RB8 = 1). This feature is enabled by setting the SM2 bit in SCON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. Remember, an address byte has its 9th bit set to 1, whereas a data byte has its 9th bit set to 0. All the slave processors should have their SM2 bits set to 1 so they will only be interrupted by an address byte. In fact, the 8XC51GB has an Automatic Address Recognition feature which allows only the addressed slave to be interrupted. That is, the address comparison occurs in hardware, not software. (On the 8051 serial port, an address byte interrupts all slaves for an address comparison.)

The addressed slave then clears its SM2 bit and prepares to receive the data bytes that will be coming. The other slaves are unaffected by these data bytes. They are still waiting to be addressed since their SM2 bits are all set.

8.3 Automatic Address Recognition

Automatic Address Recognition reduces the CPU time required to service the serial port. Since the CPU is only interrupted when it receives its own address, the software overhead to compare addresses is eliminated. Automatic address recognition is enabled by setting the SM2 bit in SCON. With this feature enabled in one of the 9-bit modes, the Receive Interrupt (RI) flag will only get set when the received byte corresponds to either a Given or Broadcast address.

The master can selectively communicate with groups of slaves by using the Given Address. Addressing all slaves at once is possible with the Broadcast Address. These addresses are defined for each slave by two Special Function Registers: SADDR and SADEN.

A slave's individual address is specified in SADDR. SADEN is a mask byte that defines don't-cares to form the Given Address. These don't-cares allow flexibility in the user-defined protocol to address one or more slaves at a time. The following is an example of how the user could define Given Addresses to selectively address different slaves.

Slave 1:

SADDR =	1111	0001
SADEN =	1111	1010
GIVEN =	1111	0X0X

Slave 2:

SADDR =	1111	0011
SADEN =	1111	1001
GIVEN =	1111	0XX1

The SADEN bytes are selected such that each slave can be addressed separately. Notice that bit 1 (LSB) is a don't-care for Slave 1's Given Address, but bit 1 = 1 for Slave 2. Thus, to selectively communicate with just Slave 1 the master must send an address with bit 1 = 0 (e.g. 1111 0000). Similarly, bit 2 = 0 for Slave 1, but is a don't-care for Slave 2. Now to communicate with just Slave 2 an address with bit 2 = 1 must be used (e.g. 1111 0111). Finally, for a master to communicate with both slaves at once the address must have bit 1 = 1 and bit 2 = 0.

Notice, however, that bit 3 is a don't-care for both slaves. This allows two different addresses to select both slaves (1111 0001 or 1111 0101). If a third slave was added that required its bit 3 = 0, then the latter address could be used to communicate with Slave 1 and 2 but not Slave 3.

The master can also communicate with all slaves at once with the Broadcast Address. It is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-cares. The don't-cares also allow flexibility in defining the Broadcast Address, but in most applications a Broadcast Address will be 0FFH.

The feature works the same way in the 8-bit mode (Mode 1) as in the 9-bit modes, except that the stop bit takes the place of the 9th data bit. If SM2 is set, the RI flag is set only if the received byte matches the Given or Broadcast Address and is terminated by a valid stop bit. Setting the SM2 bit has no effect in Mode 0.

On reset, the SADDR and SADEN registers are initialized to 00H, which defines the Given and Broadcast Addresses as XXXX XXXX (all don't-cares). This assures the 8XC51GB serial port to be backwards compatibility with other MCS-51 products which do not implement Automatic Addressing.

8.4 Baud Rates

The baud rate in Mode 0 is fixed:

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

The baud rate in Mode 2 depends on the value of bit SMOD1 in Special Function Register PCON. If SMOD1 = 0 (which is the value on reset), the baud rate is 1/64 the oscillator frequency. If SMOD1 = 1, the baud rate is 1/32 the oscillator frequency.

$$\text{Mode 2 Baud Rate} = 2^{\text{SMOD1}} \times \frac{\text{Oscillator Frequency}}{64}$$

The baud rates in Mode 1 and Mode 3 are determined by the Timer 1 overflow rate, or by Timer 2 overflow rate, or by both (one for transmit and the other for receive).

8.5 Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD1 as follows:

$$\text{Modes 1 and 3 Baud Rate} = 2^{\text{SMOD1}} \times \frac{\text{Timer 1 Overflow Rate}}{32}$$

Figure 28 shows how commonly used Baud Rates may be generated. The Timer 1 interrupt should be disabled in this application. Timer 1 can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In most applications, it is configured for "timer" operation in the auto-reload mode (high

nibble of TMOD = 0010B). In this case, the baud rate is given by the formula:

$$\text{Modes 1 and 3 Baud Rate} = 2^{\text{SMOD1}} \times \frac{\text{Oscillator Frequency}}{32 \times 12 \times [256 - (\text{TH1})]}$$

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload.

8.6 Timer 2 to Generate Baud Rates

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. Note that the baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 29.

Baud Rate	F_{OSC}	SMOD	Timer 1		
			C_T	Mode	Reload Value
Mode 0 Max: 1 MHz	12 MHz	X	X	X	X
Mode 2 Max: 375K	12 MHz	1	X	X	X
Modes 1 & 3: 62.5K	12 MHz	1	0	2	FFH
19.2K	11.059 MHz	1	0	2	FDH
9.6K	11.059 MHz	0	0	2	FDH
4.8K	11.059 MHz	0	0	2	FAH
2.4K	11.059 MHz	0	0	2	F4H
1.2K	11.059 MHz	0	0	2	E8H
137.5	11.986 MHz	0	0	2	1DH
110	6 MHz	0	0	2	72H
110	12 MHz	0	0	1	FEEBH

Figure 28. Timer 1 Generated Commonly Used Baud Rates

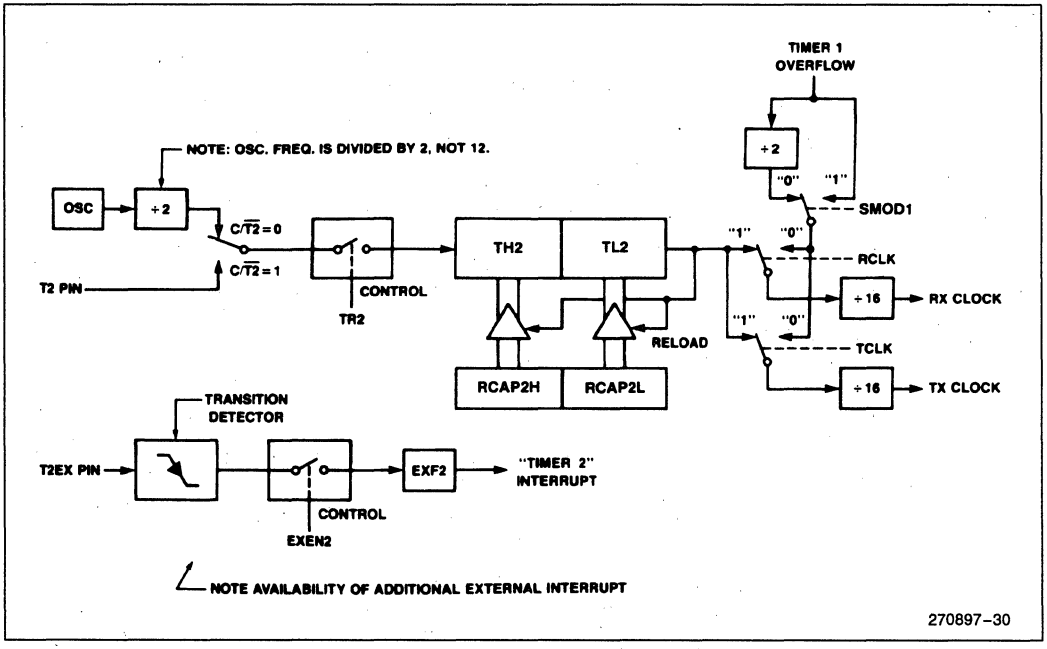


Figure 29. Timer 2 in Baud Rate Generator Mode

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

Timer 2 can be configured for either "timer" or "counter" operation. In most applications, it is configured for "timer" operation (C_T2 = 0). The "Timer" operation is different for Timer 2 when it's being used as a baud rate generator. Normally, as a timer, it increments every machine cycle (1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (½ the oscillator frequency). The baud rate formula is given below:

$$\text{Modes 1 and 3 Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H, RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is valid only if RCLK and/or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition on the T2EX pin will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

Table 18 lists commonly used baud rates and how they can be obtained from Timer 2.

It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the Timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read, but shouldn't be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 18. Timer 2 Generated Baud Rates

Baud Rate	F_{OSC}	Timer 2	
		RCAP2H	RCAP2L
375K	12 MHz	FFH	FFH
9.6K	12 MHz	FFH	D9H
4.8K	12 MHz	FFH	B2H
2.4K	12 MHz	FFH	64H
1.2K	12 MHz	FEH	C8H
300	12 MHz	FBH	1EH
110	12 MHz	F2H	AFH
300	6 MHz	FDH	8FH
110	6 MHz	F9H	57H

9.0 SERIAL EXPANSION PORT

The Serial Expansion Port (SEP) allows a wide variety of serially hosted peripherals to be connected to the 8XC51GB. The SEP has four programmable modes and four clock options. There is a single bi-directional data pin (P4.1) and a clock output pin (P4.0). Data transfers consist of 8 clocks with 8 bits of data received or transmitted. When not transmitting or receiving the data and clock pins are inactive. There are 3 SFRs associated with the SEP as shown in Figure 30.

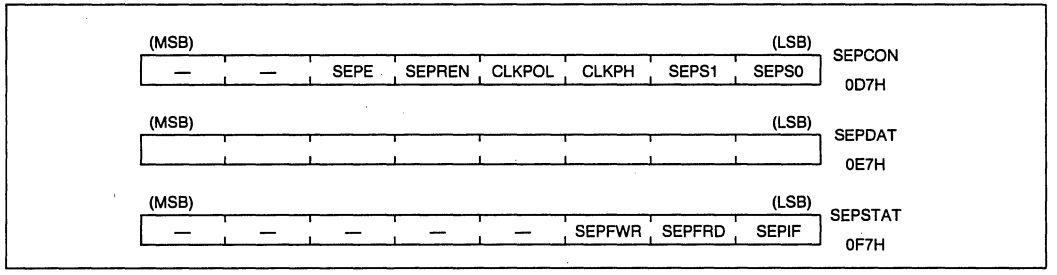


Figure 30. SEP SFRs

None of the SEP SFRs are bit addressable. However, the individual bits of SEPSTAT and SEPCON are significant and have symbolic names associated with them as shown. The meaning of these bits are:

SEPE — SEP Enable bit
SEPREN — SEP Receive ENable
CLKPOL — CLocK POLarity
CLKPH — CLocK PHase
SEPS1 — SEP Speed select 1
SEPS0 — SEP Speed select 0
SEPFWR — SEP Fault during WRite
SEPFRD — SEP Fault during ReaD
SEPIF — SEP Interrupt Flag

9.1 Programmable Modes and Clock Options

The four programmable modes determine the inactive level of the clock pin and which edge of the clock is used for transmission or reception. These four modes are shown in Figure 31. Table 19 shows how the modes are determined.

Table 19. Determination of SEP Modes

CLKPOL	CLKPH	SEP Mode
0	0	SEPMODE0
0	1	SEPMODE1*
1	0	SEPMODE2
1	1	SEPMODE3*

The four clock options determine the rate at which data is shifted out of or into the SEP. All four rates are fractions of the oscillator frequency. Table 20 shows the various rates that can be selected for the SEP.

Table 20. SEP Data Rates

SEPS1	SEPS0	Data Rate
0	0	FOSC/12
0	1	FOSC/24
1	0	FOSC/48
1	1	FOSC/96

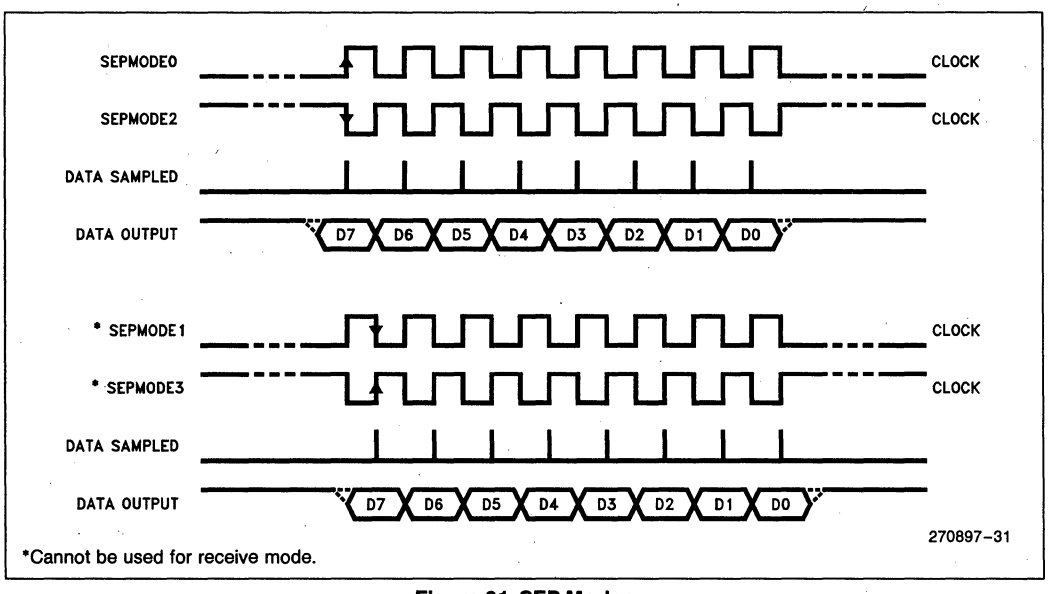


Figure 31. SEP Modes

9.2 SEP Transmission or Reception

To transmit or receive a byte the user should initialize the SEP mode (CLKPOL and CLKPH), clock frequency (SEPS1 and SEPS0), and enable the SEP (SEPE). A transmission then occurs if the user loads data into SEPDATA. A reception occurs if the user sets SEPREN while SEPDATA is empty and a transmission is not in progress. When 8 bits have been received SEPREN will be cleared by hardware. Once the transmission or reception is complete, SEPIF will be set. SEPIF remains set until cleared by software. SEPIF is also the source of the SEP interrupt. Data is transmitted and received MSB first.

If the user attempts to read or write the SEPDATA register or write to the SEPCON register while the SEP is transmitting or receiving an error bit is set. The SEPFWR bit is set if the action occurred while the SEP was transmitting. The SEPFRD bit is set if the action occurred while the SEP was receiving. There is no interrupt associated with these error bits. The bit remains set until cleared by software. The attempted read or write of the register is ignored. The reception of transmission that was in progress will not be affected.

10.0 HARDWARE WATCHDOG TIMER

The hardware WatchDog Timer (WDT) resets the 8XC51GB when it overflows. The WDT is intended as a recovery method in situations where the CPU may be subjected to a software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is *always* enabled and increments while the oscillator is running. There is no way to disable the WDT. This means that the user must still service the WDT while testing or debugging an application. The WDT is loaded with 0 when the 8XC51GB exits reset. The WDT described in this section is not the Watchdog Timer associated with PCA module 4. The WDT does not drive the Reset pin.

10.1 Using the WDT

Since the WDT is automatically enabled while the processor is running, the user only needs to be concerned with servicing it. The 14-bit counter overflows when it reaches 16383 (3FFFH). The WDT increments once every machine cycle. This means the user must reset the WDT at least every 16383 machine cycles. If the user does not wish to use the functionality of the WDT in an application, a timer interrupt can be used to reset the WDT. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT count cannot be read or written. Using a timer interrupt is not recommended in applications that make use of the WDT because interrupts may still be serviced, even after a software upset. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

10.2 WDT During Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down the user does not need to service the WDT. There are two methods of exiting Power Down: by a reset or via a level activated external interrupt which is enabled prior to entering Power Down. If Power Down is exited with reset, servicing of the WDT should occur as it normally does whenever the 8XC51GB is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low which brings the device out of Power Down and starts the oscillator. The user must hold the interrupt low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine for the interrupt used to exit Power Down.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In Idle mode, the oscillator continues to run. To prevent the WDT from resetting the 8XC51GB while in Idle, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

11.0 OSCILLATOR FAIL DETECT

The Oscillator Fail Detect (OFD) circuitry keeps the 8XC51GB in reset when the oscillator speed is below the OFD trigger frequency. The OFD trigger frequency is shown in the data sheet as a minimum and maximum. If the oscillator frequency is below the minimum, the device is held in reset. If the oscillator frequency is greater than the maximum, the device will not be held in reset. If the frequency is between the minimum and maximum, it is indeterminate whether the device will be held in reset or not.

The OFD is automatically enabled when the device comes out of reset or when Power Down is exited with a reset or an interrupt.

The OFD is intended to function only in situations where there is a gross failure of the oscillator, such as a

broken crystal. To fulfill this need the OFD trigger frequency is significantly below the normal operating frequency. The OFD will not reset the 8XC51GB if the oscillator frequency should change to another point within the operating range.

11.1 OFD During Power Down

In Power Down, the 8XC51GB oscillator stops in order to conserve power. To prevent the 8XC51GB from immediately resetting itself out of power down the OFD must be disabled prior to setting the PD bit. Writing the sequence "0E1H, 01EH" to the OSCillatoR (OSCR) SFR, turns the OFD off. Once disabled, the OFD can only be re-enabled by a reset or exit from Power Down with an interrupt. The status of the OFD (whether on or off) can be determined by reading OSCR. The LSB indicates the status of the OFD. The upper 7 bits of OSCR will always be 1s when read. If OSCR = 0FFH, the OFD is enabled. If OSCR = 0FEH, the OFD is disabled.

12.0 INTERRUPTS

The 8XC51GB has a total of 15 interrupt vectors: seven external interrupts ($\overline{INT0}$, $\overline{INT1}$, INT2, INT3, INT4, INT5, and INT6), three timer interrupts (Timers 0, 1, and 2), two PCA interrupts (PCA0 and PCA1), the A/D interrupt, the SEP interrupt, and the serial port interrupt. Figure 32 shows the interrupt sources.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be canceled in software.

12.1 External Interrupts

External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can each be either level-activated or negative edge-triggered, depending on bits IT0 and IT1 in register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{INTx}$ pin. If ITx = 1, external interrupt x is negative edge-triggered.

INT2 and INT3 can each be either negative or positive edge-triggered, depending on bits IT2 and IT3 in register EXICON. If ITx = 0, external interrupt x is negative edge-triggered. If ITx = 1, external interrupt x is positive edge-triggered.

INT4, INT5, and INT6 are positive edge-triggered only.

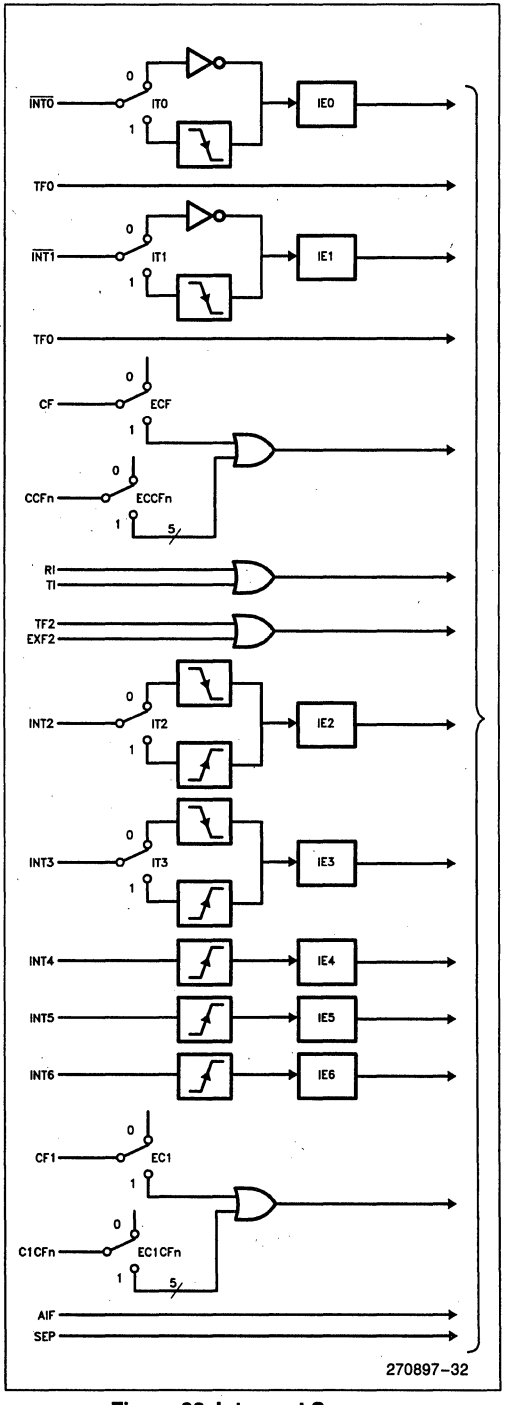


Figure 32. Interrupt Sources

Table 21. EXICON: External Interrupt Control Register

EXICON						Reset Value = X000 0000B		
	Address = 0C6H					Not Bit Addressable		
Bit	7	6	5	4	3	2	1	0
EXICON	—	IE6	IE5	IE4	IE3	IE2	IT3	IT2

Symbol	**Function**
—	Not implemented, reserved for future use.*
IE6	Interrupt 6 Edge flag. This bit is set by hardware when an external interrupt edge is detected.
IE5	Interrupt 5 Edge flag. This bit is set by hardware when an external interrupt edge is detected.
IE4	Interrupt 4 Edge flag. This bit is set by hardware when an external interrupt edge is detected.
IE3	Interrupt 3 Edge flag. This bit is set by hardware when an external interrupt edge is detected.
IE2	Interrupt 2 Edge flag. This bit is set by hardware when an external interrupt edge is detected.
IT3	Interrupt 3 Type control bit. This bit is set or cleared by software to control whether INT3 is positive or negative transition activated. When IT3 is high, IE3 is set by a positive transition on pin INT3. When IT3 is low, IE3 is set by a negative transition on pin INT3.
IT2	Interrupt 2 Type control bit. This bit is set or cleared by software to control whether INT2 is positive or negative transition activated. When IT2 is high, IE2 is set by a positive transition on pin INT2. When IT2 is low, IE2 is set by a negative transition on pin INT2.

*Using software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from reserved bit is indeterminate.

The flags that actually generate the interrupts are bits IE0 and IE1 in TCON and IE2, IE3, IE4, IE5, and IE6 in EXICON. These flags are cleared by hardware when the service routine is vectored to if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source is what controls the request flag, rather than the on-chip hardware. The external interrupts are enabled through bits EX0 and EX1 in the IE register and EX2, EX3, EX4, EX5, and EX6 in the IEA register.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one cycle, and then hold it low for at least one cycle to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called.

If external interrupt $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

12.2 Timer Interrupts

Timer 0 and Timer 1 interrupts are generated by TF0 and TF1 in register TCON, which are set by a rollover in their respective Timer/Counter registers; the exception is Timer 0 in Mode 3. When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to. These timer interrupts are enabled by bits ET0 and ET1 in the IE register.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and the bit will have to be cleared in software. The Timer 2 interrupt is enabled by the ET2 bit in the IE register.

12.3 PCA Interrupt

The PCA interrupts are generated by the logical OR of five event flags (CCFn, C1CFn) and the PCA timer overflow flag (CF, CF1) in the registers CCON and C1CON. None of these flags are cleared by hardware when the service routine is vectored to. Normally the service routine will have to determine which bit flagged the interrupt and clear that bit in software. This allows the user to define the priority of servicing each PCA module.

The PCA interrupt is enabled by bit EC in the IE register. The PCA1 interrupt is enabled by bit EC1 in the IEA register. In addition, the CF (CF1) flag and each of the CCFn (C1CFn) flags must also be individually enabled by bits ECF (ECF1) and ECCFn (EC1CFn) in registers CMOD (C1MOD) and CCAPMn (C1CAPMn), respectively, in order for that flag to be able to cause an interrupt.

12.4 Serial Port Interrupt

The serial port interrupt is generated by the logical OR of bits RI and TI in register SCON. Neither of these flags is cleared by hardware when the service routine is vectored to. The service routine will normally have to determine whether it was RI or TI that generated the interrupt, and the bit will have to be cleared in software. The serial port interrupt is enabled by bit ES in the IE register.

12.5 Interrupt Enable

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable (IE and IEA) registers as shown in Table 22. Note that IE also contains a global disable bit, EA. If EA is set (1), the interrupts are individually enabled or disabled by their corresponding bits in IE and IEA. If EA is clear (0), all interrupts are disabled. Figure 33 shows the interrupt control system.

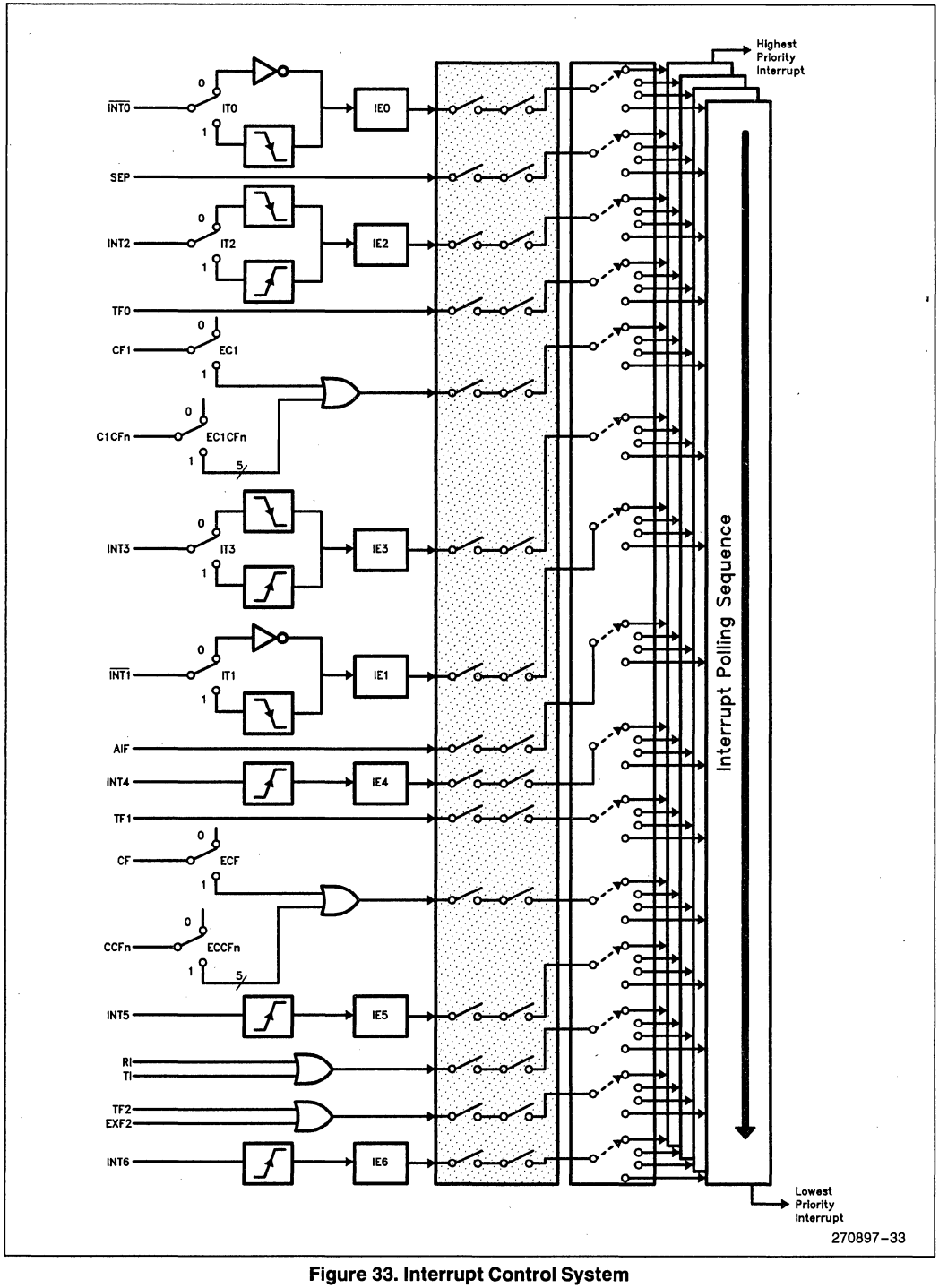


Figure 33. Interrupt Control System

Table 22. Interrupt Enable Registers

IE Address = 0A8H Reset Value = 0000 0000B

Bit Addressable

EA	EC	ET2	ES	ET1	EX1	ET0	EX0
Bit 7	6	5	4	3	2	1	0

IEA Address = 0A7H Reset Value = 0000 0000B

Not Bit Addressable

EAD	EX6	EX5	EX4	EX3	EX2	EC1	ESEP
Bit 7	6	5	4	3	2	1	0

Enable bit = 1 enables the interrupt
Enable bit = 0 disables the interrupt

Symbol	Function
EA	Global disable bit. If EA=0, all Interrupts are disabled. If EA=1, each Interrupt can be individually enabled or disabled by setting or clearing its enable bit.
EC	PCA interrupt enable bit.
ET2	Timer 2 interrupt enable bit
ES	Serial Port interrupt enable bit.
ET1	Timer 1 interrupt enable bit.
EX1	External interrupt 1 enable bit.
ET0	Timer 0 interrupt enable bit.
EX0	External interrupt 0 enable bit.
EAD	A/D converter interrupt enable bit.
EX6	External interrupt 6 enable bit.
EX5	External interrupt 5 enable bit.
EX4	External interrupt 4 enable bit.
EX3	External interrupt 3 enable bit.
EX2	External interrupt 2 enable bit.
EC1	PCA1 interrupt enable bit.
ESEP	Serial Expansion Port interrupt enable bit.

12.6 Interrupt Priorities

Each interrupt source on the 8XC51GB can be individually programmed to one of four priority levels, by setting or clearing the bits in the Interrupt Priority (IP and IPA) registers and the Interrupt Priority High (IPH and IPAH) registers. See Table 23. The IPH registers have the same bit map as the IP registers with an "H" added to each bit's name. This gives each interrupt source two bits for setting the priority levels. The LSB of the Priority Select Bits is in the IP SFR, and the MSB is in the IPH SFR.

A low-priority interrupt can itself be interrupted by a higher priority interrupt, but not by another interrupt of the same priority. The highest priority interrupt cannot be interrupted by any other interrupt source.

If two or more requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence shown in Table 24.

Table 23. Interrupt Priority Registers

IP Address = 0B8H — Reset Value = X000 0000B

Bit Addressable

—	PPC	PT2	PS	PT1	PX1	PT0	PX0

IPA Address = 0B6H — Reset Value = 0000 0000B

Not Bit Addressable

PAD	PX6	PX5	PX4	PX3	PX2	PC1	PSEP

IPH Address = 0B7H — Reset Value = X000 0000B

Not Bit Addressable

—	PPPC	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

IPHA Address = 0B5H — Reset Value = 0000 0000B

Not Bit Addressable

PADH	PX6H	PX5H	PX4H	PX3H	PX2H	PC1H	PSEPH

Priority Bit	Priority Bit H	Priority
0	0	Lowest
0	1	
1	0	
1	1	Highest

Symbol	Function
—	Not Implemented, reserved for future use*
PPC, PPCH	PCA interrupt priority bits
PT2, PT2H	Timer 2 interrupt priority bits
PS, PSH	Serial Port interrupt priority bits
PT1, PT1H	Timer 1 interrupt priority bits
PX1, PX1H	External interrupt 1 interrupt priority bits
PT0, PT0H	Timer 0 interrupt priority bits
PX0, PX0H	External interrupt 0 interrupt priority bits
PAD, PADH	A/D converter interrupt priority bits
PX6, PX6H	External interrupt 6 interrupt priority bits
PX5, PX5H	External interrupt 5 interrupt priority bits
PX4, PX4H	External interrupt 4 interrupt priority bits
PX3, PX3H	External interrupt 3 interrupt priority bits
PX2, PX2H	External interrupt 2 interrupt priority bits
PC1, PC1H	PCA1 interrupt priority bits
PSEP, PSEPH	Serial Expansion Port interrupt priority bits

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Table 24. Interrupt Polling Sequence

1 (Highest)	$\overline{\text{INT0}}$
2	SEP
3	INT2
4	Timer 0
5	PCA1
6	INT3
7	$\overline{\text{INT1}}$
8	A/D
9	INT4
10	Timer 1
11	PCA
12	INT5
13	PCA
14	Timer 2
15 (Lowest)	INT6

Note that the "priority within level" structure is only used to resolve simultaneous requests of the same priority level.

12.7 Interrupt Processing

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. The Timer 2 overflow interrupt is slightly different, as described in the Interrupt Response Time section. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress.
2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3. The instruction in progress is RETI or any write to the IE or IP registers.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any write to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. If the interrupt flag for a level-sensitive external interrupt is active but not being responded to for one of the above conditions and is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The polling cycle/LCALL sequence is illustrated in the Interrupt Response Timing Diagram.

Note that if an interrupt of a higher priority level goes active prior to S5P2 of the machine cycle labeled C3 in the diagram, then in accordance with the above rules it will be vectored to during C5 and C6, without any instruction of the lower priority routine having been executed. This is the fastest possible response when C2 is the final cycle of an instruction other than RETI or write IE or IP.

Thus the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. The hardware-generated LCALL pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to. Table 25 shows the interrupt vector addresses.

Table 25. Interrupt Vector Addresses

Interrupt Source	Interrupt Request Bits	Cleared by Hardware	Vector Address
$\overline{\text{INT0}}$	IE0	No (level) Yes (trans.)	0003H
Timer 0	TF0	Yes	000BH
$\overline{\text{INT1}}$	IE1	No (level) Yes (trans.)	0013H
Timer 1	TF1	Yes	001BH
Serial Port	RI, TI	No	0023H
Timer 2	TF2, EXF2	No	002BH
PCA	CF, CCFn (n = 0–4)	No	0033H
A/D	AIF	No	003BH
PCA1	CF1, C1CCFn (n = 0–4)	No	0043H
SEP	SEPIF	No	004BH
INT2	IE2	Yes	0053H
INT3	IE3	Yes	005BH
INT4	IE4	Yes	0063H
INT5	IE5	Yes	006BH
INT6	IE6	Yes	0073H

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking interrupt was still in progress.

The starting addresses of consecutive interrupt service routines are only 8 bytes apart. That means if consecutive interrupts are being used (IE0 and TF0, for example, or TF0 and IE1), and if the first interrupt routine is more than 7 bytes long, then that routine will have to execute a jump to some other memory location where the service routine can be completed without overlapping the starting address of the next interrupt routine.

12.8 Interrupt Response Time

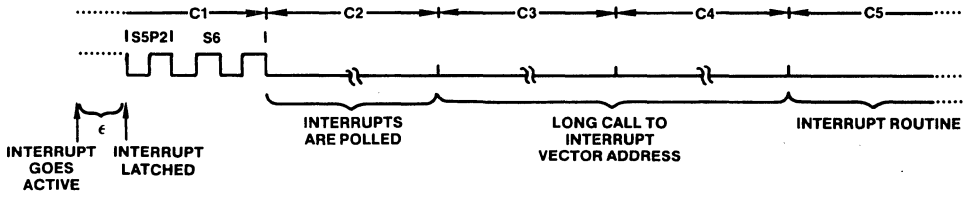
The $\overline{INT0}$ and $\overline{INT1}$ levels are inverted and latched into the Interrupt Flags IE0, and IE1 at S5P2 of every machine cycle. The level of interrupts 2 through 6 are also latched into the appropriate flags (IE2–IE6) in S5P2. Similarly, the Timer 2 flag EXF2 and the Serial Port flags RI and TI are set at S5P2. The values are not actually polled by the circuitry until the next machine cycle.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag TF2 is set at S2P2 and is polled in the same cycle in which the timer overflows.

If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes two cycles. Thus, a minimum of three complete machine cycles elapses between activation of an external interrupt request and the beginning of execution of the service routine's first instruction. See Figure 34.

A longer response time would result if the request is blocked by one of the 3 conditions discussed in the Interrupt Processing section. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than 3 cycles, since the longest instructions (MUL and DIV) are only 4 cycles long, and if the instruction in progress is RETI or write to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one or more cycles to complete the instruction in progress, plus 4 cycles to complete the next instruction if the instruction is MUL or DIV).

Thus, in a single-interrupt system, the response time is always more than 3 cycles and less than 9 cycles.



This is the fastest possible response when C2 is the final cycle of an instruction other than RETI or write IE or IP.

Figure 34. Interrupt Response Timing Diagram

13.0 RESET

The reset input is the $\overline{\text{RESET}}$ pin, which has a Schmitt Trigger input. A reset is accomplished by holding the $\overline{\text{RESET}}$ pin low for at least two machine cycles (24 oscillator periods). On the 8XC51GB, reset is asynchronous to the CPU clock. This means that the oscillator does not have to be running for the I/O pins to be in their reset condition. However, V_{CC} has to be within the specified operating conditions.

Once Reset has reached a high level, the 8XC51GB may remain in its reset state for up to 5 machine cycles. This is caused by the OFD circuitry.

While the $\overline{\text{RESET}}$ pin is low, the port pins, ALE and $\overline{\text{PSEN}}$ are weakly pulled high. After $\overline{\text{RESET}}$ is pulled high, it will take up to 5 machine cycles for ALE and $\overline{\text{PSEN}}$ to start clocking. For this reason, other devices can not be synchronized to the internal timings of the 8XC51GB.

Driving the ALE and $\overline{\text{PSEN}}$ pins to 0 while reset is active could cause the device to go into an indeterminate state.

The internal reset algorithm redefines most of the SFRs. Refer to individual SFRs for their reset values. The internal RAM is not affected by reset. On power up the RAM content is indeterminate.

13.1 Power-On Reset

For CHMOS devices, when V_{CC} is turned on, an automatic reset can be obtained by connecting the $\overline{\text{RESET}}$ pin to V_{SS} through a 1 μF capacitor. The CHMOS devices do not require an external resistor like the HMOS devices because they have an internal pullup on the $\overline{\text{RESET}}$ pin. Figure 35 shows this.

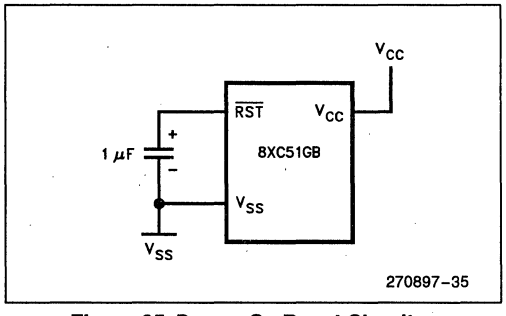


Figure 35. Power-On Reset Circuitry

When power is turned on, the circuit holds the $\overline{\text{RESET}}$ pin high for an amount of time that depends on the capacitor value and the rate at which it charges. To ensure a valid reset the $\overline{\text{RESET}}$ pin must be held low long enough to allow the oscillator to start up plus two machine cycles.

On power up, V_{CC} should rise within approximately ten milliseconds. The oscillator start-up time will depend on the oscillator frequency. For a 10 MHz crystal, the start-up time is typically 1 ms. For a 1 MHz crystal, the start-up time is typically 10 ms.

Powering up the device without a valid reset could cause the CPU to start executing instructions from an indeterminate location. This is because the SFRs, specifically the Program Counter, may not get properly initialized.

14.0 POWER-SAVING MODES

For applications where power consumption is critical, the 8XC51GB provides two power reducing modes of operation: Idle and Power Down. The input through which backup power is supplied during these operations is V_{CC}. The Idle and Power Down modes are activated by setting bits IDL and PD, respectively, in the SFR PCON (Table 26). Figure 36 shows the Idle and Power Down circuitry.

In the Idle mode (IDL = 1), the oscillator continues to run and the Interrupt, Serial Port, PCA, and Timer blocks continue to be clocked, but the clock signal is gated off to the CPU. In Power Down (PD = 1), the oscillator is frozen.

Table 26. PCON: Power Control Register

PCON Address = 87H Reset Value = 00XX 0000B

Not Bit Addressable

	SMOD1	SMOD0	—	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud rate bit. When set to a 1 and Timer 1 is used to generate baud rates, and the Serial Port is used in modes 1, 2, or 3.
SMOD0	When set, Read/Write accesses to SCON.7 are to the FE bit. When clear, Read/Write accesses to SCON.7 are to the SM0 bit.
—	Not implemented, reserved for future use.*
POF	Power Off Flag. Set by hardware on the rising edge of V_{CC}. Set or cleared by software. This flag allows detection of a power failure caused reset. V_{CC} must remain above 3V to retain this bit.
GF1	General-purpose flag bit.
GF0	General-purpose flag bit.
PD	Power Down bit. Setting this bit activates Power Down operation.
IDL	Idle mode bit. Setting this bit activates idle modes operation. If 1s are written to PD and IDL at the same time, PD takes precedence.

NOTE:
*User software should not write 1s to unimplemented bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

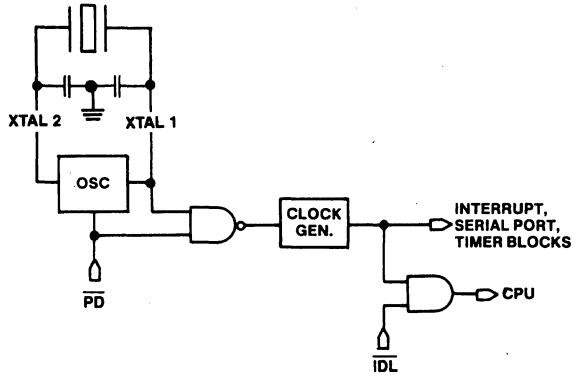


Figure 36. Idle and Power Down Hardware

14.1 Idle Mode

An instruction that sets the IDL bit causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the Interrupt, Timer, and Serial Port functions. The PCA and PCA1 timers can be programmed either to pause or continue operating during Idle with the CIDL (C1IDL) bit in CMOD (C1MOD). The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and $\overline{PSEN}$ hold at logic high levels. Refer to Table 27.

Table 27. Status of the External Pins during Idle Mode

Program Memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Ports 3, 4, 5
Internal	1	1	Data	Data	Data	Data
External	1	1	Float	Data	Address	Data

There are two ways to terminate the Idle Mode. Activation of any enabled interrupt will cause the IDL bit to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into Idle.

The flag bits (GF0 and GF1 in PCON) can be used to give an indication if an interrupt occurred during normal operation or during Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

The signal at the $\overline{RESET}$ pin clears the IDL bit directly and asynchronously. At this time the CPU resumes program execution from where it left off; that is, at the instruction following the one that invoked the Idle Mode. As shown in the Reset Timing diagram, two or three machine cycles of program execution may take place before the internal reset algorithm takes control. On-chip hardware inhibits access to the internal RAM during this time, but access to the port pins is not inhibited. To eliminate the possibility of unexpected outputs at the port pins, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external Data RAM.

14.2 Power Down Mode

An instruction that sets the PD bit causes that to be the last instruction executed before going into the Power Down mode. In this mode the on-chip oscillator is stopped. With the clock frozen, all functions are stopped, but the on-chip RAM and Special Function Registers are held. The port pins output the values held by their respective SFRs, and ALE and $\overline{PSEN}$ output lows. In Power Down, V_{CC} can be reduced to as low as 2V. Care must be taken, however, to ensure that V_{CC} is not reduced before Power Down is invoked. If the Oscillator Fail Detect circuitry is not disabled before entering powerdown, the part will reset itself (see Section 11.0 "Oscillator Fail Detect"). Table 28 shows the status of external pins during Power Down mode.

Table 28. Status of the External Pins during Power Down Mode

Program Memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Ports 3, 4, 5
Internal	0	0	Data	Data	Data	Data
External	0	0	Float	Data	Data	Data

The 8XC51GB can exit Power Down with either a hardware reset or external interrupt. Reset redefines most of the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, $\overline{INT0}$ or $\overline{INT1}$ must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator and bringing the pin back high completes the exit. After the RETI instruction is executed in the interrupt service routine, the next instruction will be the one following the instruction that put the device in Power Down.

14.3 Power Off Flag

The Power Off Flag (POF) located at PCON.4 is set by hardware when V_{CC} rises from 0V to 5V. POF can also be set or cleared by software. This allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is one that is coincident with V_{CC} being turned on to the device after it was turned off. A warm start reset occurs while V_{CC} is still applied to the device and could be generated, for example, by a Watchdog Timer or an exit from Power Down.

Immediately after reset, the user's software can check the status of the POF bit. POF = 1 would indicate a cold start. The software then clears POF and commences its tasks. POF = 0 immediately after reset would indicate a warm start.

V_{CC} must remain above 3V for POF to retain a 0.

15.0 EPROM/OTP PROGRAMMING

The 8XC51GB uses the fast "Quick-Pulse" Programming algorithm. The devices program at V_{PP} = 12.75V (and V_{CC} = 5.0V) using a series of five 100 µs PROG pulses per byte programmed.

15.1 Program Memory Lock

In some microcontroller applications it is desirable that the Program Memory be secure from software piracy. The 8XC51GB has a three-level program lock feature which protects the code of the on-chip EPROM/OTP or ROM.

Within the EPROM/OTP/ROM are 64 bytes of Encryption Array that are initially unprogrammed (all 1s). The user can program the Encryption Array to encrypt the program code bytes during EPROM/OTP/ROM verification. The verification procedure is performed as usual except that each code byte comes out exclusive-NOR'ed (XNOR) with one of the key bytes. Therefore, to read the ROM code the user has to know the 64 key bytes in their proper sequence.

Unprogrammed bytes have the value 0FFH. So if the Encryption Array is left unprogrammed, all the key bytes have the value 0FFH. Since any code byte XNORed with 0FFH leaves the byte unchanged, leaving the Encryption Array unprogrammed in effect bypasses the encryption feature.

PROGRAM LOCK BITS

Also included in the Program Lock scheme are three Lock Bits which can be programmed to disable certain functions as shown in Table 29.

To obtain maximum security of the on-board program and data, all 3 Lock Bits and the Encyption Array must be programmed.

Erasing the EPROM also erases the Encryption Array and the Lock Bits, returning the part to full functionality:

Table 29. EPROM/OTP Lock Bits

Program Lock Bits			Logic Enabled
LB1	LB2	LB3	
U	U	U	No Program Lock features enabled. (Code Verify will still be encrypted by the Encryption Array.)
P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset, and further programming of EPROM is disabled.
P	P	U	Same as above, but Verify is also disabled (option available on EPROM only).
P	P	P	Same as above and all external program execution is inhibited and internal RAM cannot be read externally.

NOTE:
All other combinations of lock bits may produce indeterminate results and should not be used.

16.0 ONCE MODE

The ONCE (ON-Circuit Emulation) mode facilitates testing and debugging of systems using the 8XC51GB without having to remove the device from the circuit. The ONCE mode is invoked by:

1. Pulling ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Holding ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins go into a float state, and the other port pins, ALE, and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit.

Normal operation is restored after a valid reset is applied.

9

17.0 ON-CHIP OSCILLATOR

The on-chip oscillator for the CHMOS devices consists of a single stage linear inverter intended for use as a

crystal-controlled, positive reactance oscillator. In this application the crystal is operating in its fundamental response mode as an inductive reactance in parallel resonance with capacitance external to the crystal. Figure 37 shows the on-chip oscillator circuitry.

The oscillator on the CHMOS devices can be turned off under software control by setting the PD bit in the PCON register (Figure 38). The feedback resistor R_f shown in the figure consists of parallel n- and p-channel FETs controlled by the PD bit, such that R_f is opened when PD = 1. The diodes D1 and D2, which act as clamps to V_{CC} and V_{SS}, are parasitic to the R_f FETs.

The crystal specifications and capacitance values (C1 and C2 in Figure 39) are not critical. 30 pF can be used in these positions at any frequency with good quality crystals. In general, crystals used with these devices typically have the following specifications:

ESR (Equivalent Series Resistance)	
CO (shunt capacitance)	7.0 pF maximum
CL (load capacitance)	30 pF ±3 pF
Drive Level	1 MW

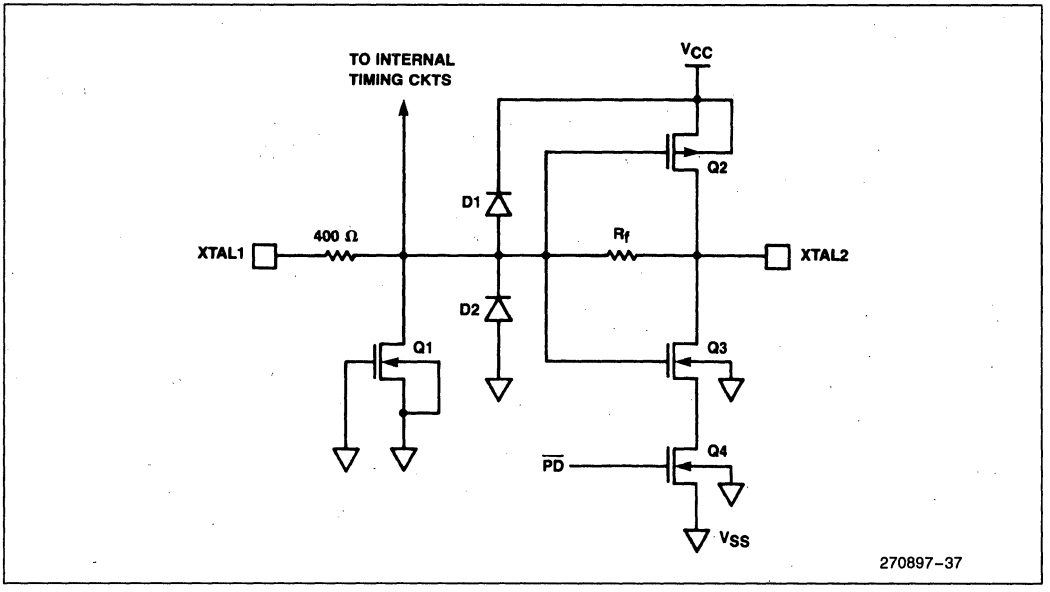


Figure 37. On-Chip Oscillator Circuitry

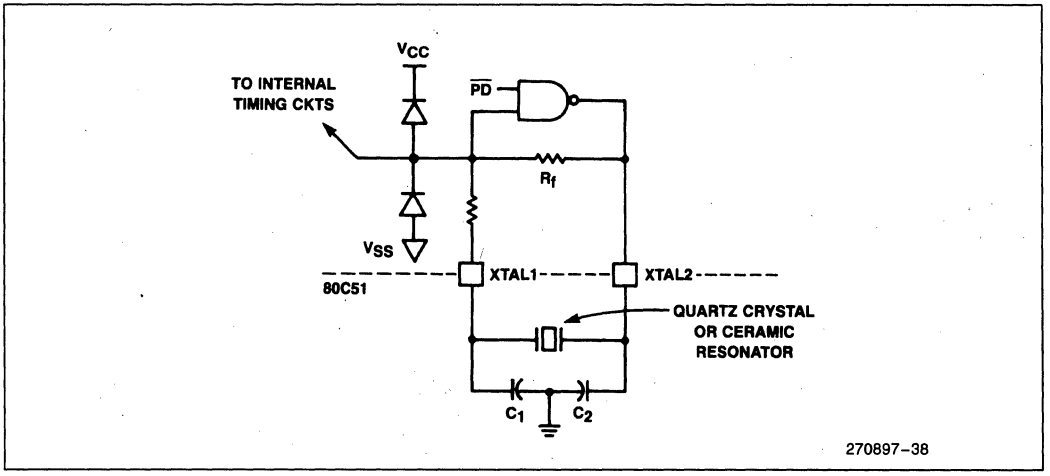


Figure 38. Using the CHMOS On-Chip Oscillator

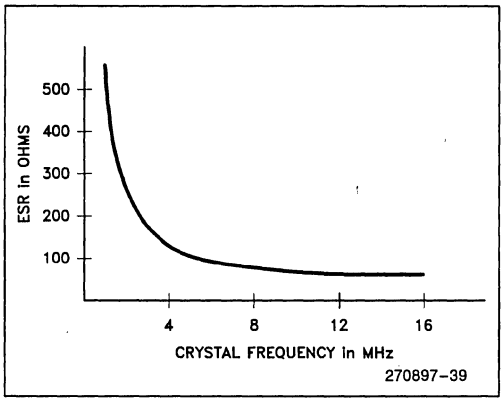


Figure 39. ESR vs Frequency

Frequency, tolerance, and temperature range are determined by the system requirements.

A ceramic resonator can be used in place of the crystal in cost-sensitive applications. When a ceramic resonator is used, C1 and C2 are normally selected as higher values, typically 47 pF. The manufacturer of the ceramic resonator should be consulted for recommendations on the values of these capacitors.

A more in-depth discussion of crystal specifications, ceramic resonators, and the selection of values for C1 and C2 can be found in Application Note AP-155, "Oscillators for Microcontrollers" in the Embedded Control Applications handbook.

To drive the CHMOS parts with an external clock source, apply the external clock signal to XTAL1 and leave XTAL2 floating. Refer to the External Clock Source diagram. This is an important difference from the HMOS parts. With HMOS, the external clock source is applied to XTAL2, and XTAL1 is grounded. See Figure 40.

There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheets must be observed. Refer to the External Clock Specifications for this information.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications, the capacitance will not exceed 20 pF.

18.0 CPU TIMING

The internal clock generator defines the sequence of states that make up a machine cycle. A machine cycle consists of 6 states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency is 12 MHz. Each state is then divided into a Phase 1 and Phase 2 half.

Rise and fall times are dependent on the external loading that each pin must drive. They are approximately 10 ns, measured between 0.8V and 2.0V.

Propagation delays are different for different pins. For a given pin they vary with pin loading, temperature, V_{CC}, and manufacturing lot. If the XTAL1 waveform is taken as the timing reference, propagation delays may vary from 25 ns to 125 ns.

The AC Timings section of the data sheets do not reference any timing to the XTAL1 waveform. Rather, they relate the critical edges of control and input signals to each other. The timings published in the data sheets include the effects of propagation delays under the specified test condition.

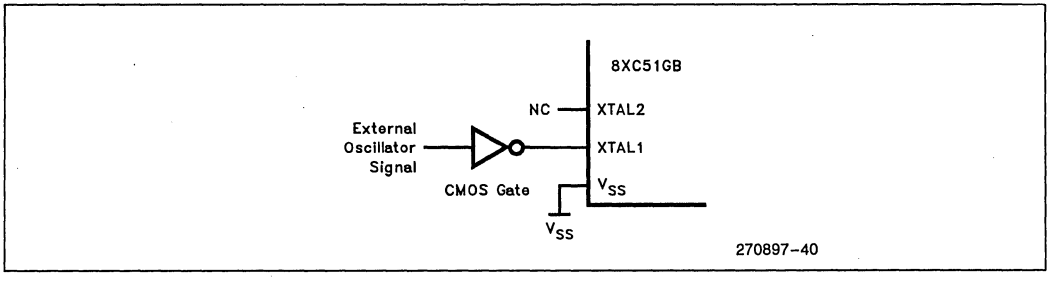


Figure 40. Driving the CHMOS Devices with an External Clock Sources

87C51GB/83C51GB/80C51GB
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

87C51GB—8 Kbytes OTP/8 Kbytes Internal Program Memory
83C51GB—8 Kbytes Factory Programmable ROM
80C51GB—CPU with RAM and I/O
8XC51GB—3.5 MHz to 12 MHz ±20% V_{CC}
8XC51GB-1—3.5 MHz to 16 MHz ±20% V_{CC}

- 8 Kbytes On-Chip ROM/OTP ROM
- 256 Bytes of On-Chip Data RAM
- Two Programmable Counter Arrays with:
  - — 2 x 5 High Speed Input/Output Channels Compare/Capture
  - — Pulse Width Modulators
  - — Watchdog Timer Capabilities
- Three 16-Bit Timer/Counters with
  - — Four Programmable Modes:
  - — Capture, Baud Rate Generation (Timer 2)
- Dedicated Watchdog Timer
- 8-Bit, 8-Channel A/D with:
  - — Eight 8-Bit Result Registers
  - — Four Programmable Modes
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- Serial Expansion Port
- Programmable Clock Out
- 48 Programmable I/O Lines with 40 Schmitt Trigger Inputs
- 15 Interrupt Sources with:
  - — 7 External, 8 Internal Sources
  - — 4 Programmable Priority Levels
- Pre-Determined Port States on Reset
- High Performance CHMOS Process
- TTL and CHMOS Compatible Logic Levels
- Power Saving Modes
- 64K External Data Memory Space
- 64K External Program Memory Space
- Three Level Program Lock System
- ONCE™ (ON-Circuit Emulation) Mode
- Quick Pulse Programming™ Algorithm
- MCS®-51 Fully Compatible Instruction Set
- Boolean Processor
- Oscillator Fail Detect
- Available in 68-Pin PLCC

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside in the on-chip ROM. Also, the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 8XC51GB is a single-chip control oriented microcontroller which is fabricated on Intel's CHMOS III-E technology. The 8XC51GB is an enhanced version of the 8XC51FA and uses the same powerful instruction set and architecture as existing MCS®-51 products. Added features make it an even more powerful microcontroller for applications that require On-Chip A/D, Pulse Width Modulation, High Speed I/O, up/down counting capabilities and memory protection features. It also has a more versatile serial channel that facilitates multiprocessor communications.

July 1992
Order Number: 270869-003

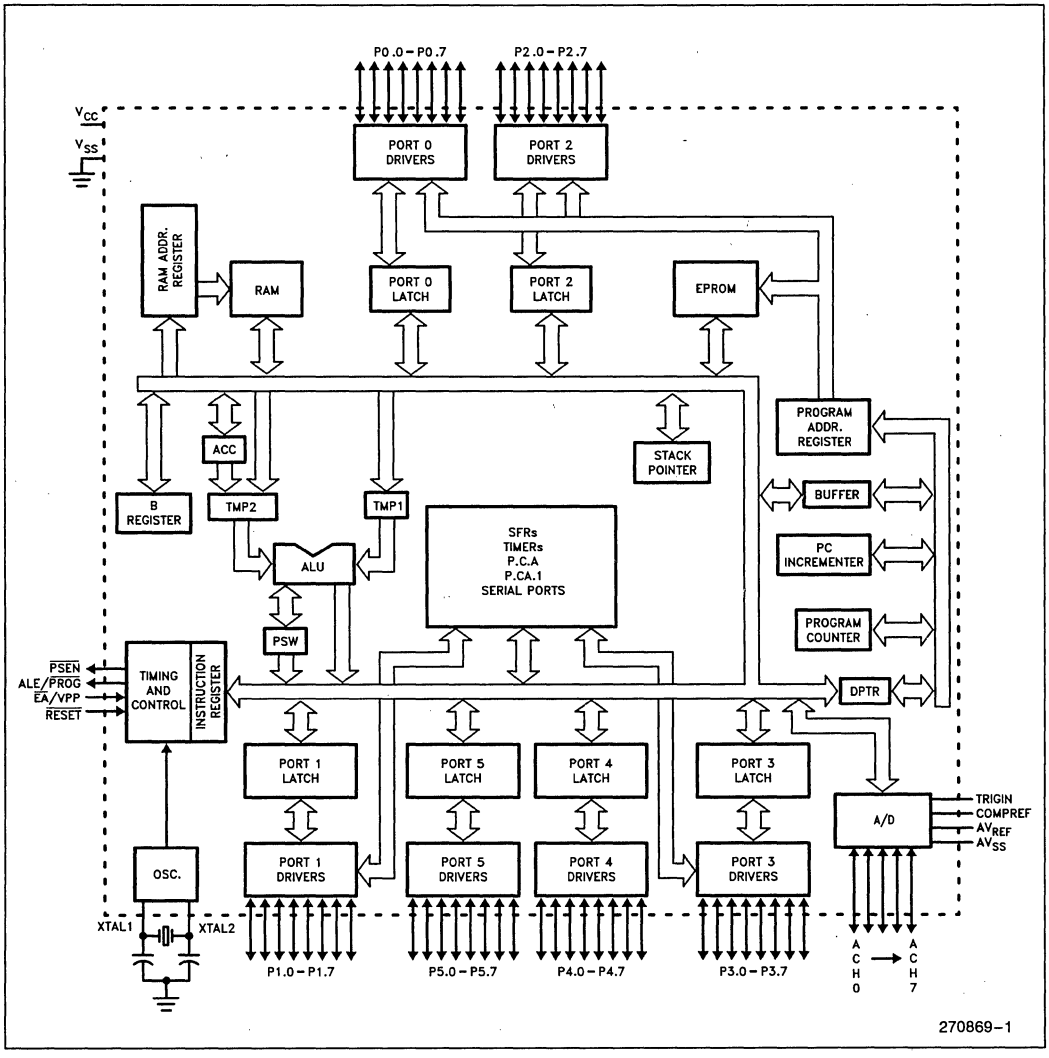


Figure 1. 8XC51GB Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's Components Quality and Reliability Handbook, Order Number 210997.

PACKAGES

Part	Prefix	Package Type	θ_{JA}	θ_{JC}
8XC51GB	N	68-Pin PLCC	N/A	N/A

9

PARALLEL I/O PORTS

The 8XC51GB contains six 8-bit parallel I/O ports. All six ports are bidirectional and consist of a latch, an output driver, and an input buffer. Many of the port pins have multiplexed I/O and control functions.

Port Pins as Outputs

Port 0 has open drain outputs when it is not serving as the external data bus. The internal pullup is active only when the pin is outputting a logic 1 during external memory access. An external pullup resistor is required on Port 0 when it is serving as an output port.

Ports 1, 2, 3, 4, and 5 have quasi-bidirectional outputs. A strong pullup provides a fast rise time when the pin is set to a logic 1. This pullup turns on for two oscillator periods to drive the pin high and then turns off. The pin is held high by a weak pullup.

Writing the P0, P1, P2, P3, P4 or P5 Special Function Register sets the corresponding port pins. All six port registers are bit addressable.

Port Pins as Inputs

The pins of all six ports are configured as inputs by writing a logic 1 to them. Since Port 0 is an open drain port, it provides a very high input impedance. Since pins of Port 1, 2, 3, 4 and 5 have weak pullups (which are always on), they source a small current when driven low externally. All ports except Port 0 have Schmitt trigger inputs.

Port States During Reset

Ports 0 and 3 reset asynchronously to a one and Ports 1, 2, 4, and 5 reset to a zero asynchronously.

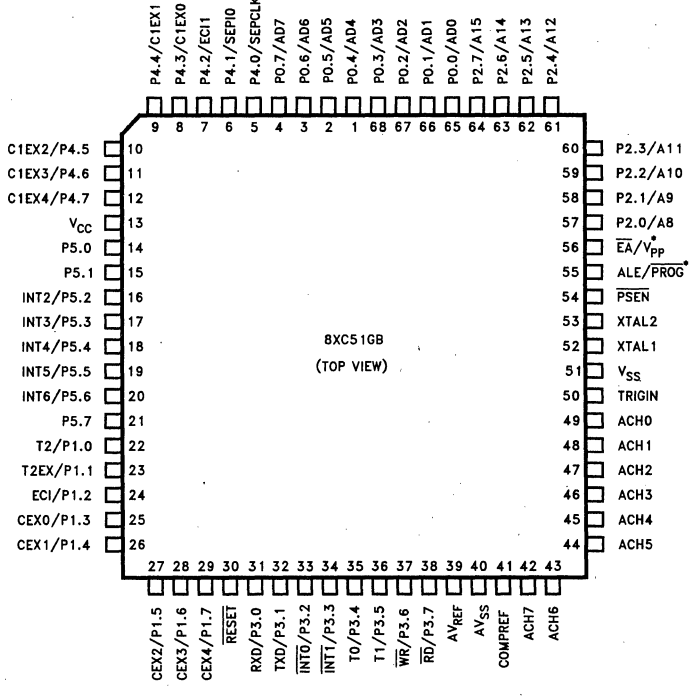
PIN DESCRIPTIONS

The 8XC51GB will be packaged in the 68-lead PLCC package. Its pin assignment is shown in Figure 2.

V_{CC}: Supply Voltage.

V_{SS}: Circuit Ground.

Diagram is for Pin Reference Only. Package Size is Not to Scale.



*OTP only

Figure 2. Pin Connections

ALTERNATE PORT FUNCTIONS

Ports 0, 1, 2, 3, 4 and 5 have alternate functions as well as their I/O function as described below.

Port Pin	Alternate Function
P0.0/AD0–P0.7/AD7	Multiplexed Address/Data for External Memory
P1.0/T2	Timer 2 External Clock Input/Clock-Out
P1.1/T2EX	Timer 2 Reload/Capture/Direction Control
P1.2/ECI	PCA External Clock Input
P1.3/CEX0–P1.7/CEX4	PCA Capture Input, Compare/PWM Output
P2.0/A8–P2.7/A15	High Byte of Address for External Memory
P3.0/RXD	Serial Port Input
P3.1/TXD	Serial Port Output
P3.2/$\overline{\text{INT0}}$	External Interrupt 0
P3.3/$\overline{\text{INT1}}$	External Interrupt 1
P3.4/T0	Timer 0 External Clock Input
P3.5/T1	Timer 1 External Clock Input
P3.6/$\overline{\text{WR}}$	Write Strobe for External Memory
P3.7/$\overline{\text{RD}}$	Read Strobe for External Memory
P4.0/SEPCLK	Clock Source for Serial Expansion Port
P4.1/SEPDAT	Data I/O for the Serial Expansion Port
P4.2/ECI1	PCA1 External Clock Input
P4.3/C1EX0–P4.7/C1EX4	PCA1 Capture Input, Compare/PWM Output
P5.2/INT2–P5.6/INT6	External Interrupt INT2–INT6

$\overline{\text{RST}}$: Reset input. A low on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a voltage below V_{IL} max voltage is applied, whether the oscillator is running or not. An internal pullup resistor permits a power-on reset with only a capacitor connected to V_{SS}.

ALE/$\overline{\text{PROG}}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{\text{PROG}}$) is also the program pulse input during programming of the 87C51GB.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX instruction. Otherwise the pin is weakly pulled high.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{\text{PROG}}$ pin, and the pin will be referred to as the ALE/$\overline{\text{PROG}}$ pin.

$\overline{\text{PSEN}}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51GB is executing code from external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external Data Memory.

$\overline{\text{EA}}$/V_{PP}: External Access enable. $\overline{\text{EA}}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 1FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during programming (OTP only).

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

A/D CONVERTER

The 8XC51GB A/D converter has a resolution of 8 bits and an accuracy of ±1 LSB (±2 LSB for channels 0 and 1). The conversion time for a single channel is 20 μs at a clock frequency of 16 MHz with the sample and hold function included. Independent supply voltages are provided for the A/D. Also, the A/D operates both in Normal Mode or in Idle Mode.

The A/D has 8 analog input pins; ACH0 (A/D CHannel 0) ... ACH7, 1 reference input pin; COMPREF (COMParison REFerence), 1 control input pin; TRIGIN (TRIGger IN), and 2 power pins; AVREF (Voltage REFerence) and analog ground (ANalog GrouND). In addition, the A/D has 8 conversion result registers; ADRES0 (A/D result for channel 0) ... ADRES7, 1 comparison result register; ACMP (Analog Comparison), and 1 control register; ACON (A/D Control).

The control bit ACE (A/D Conversion Enable) in ACON controls whether the A/D is in operation or not. ACE = 0 idles the A/D. ACE = 1 enables A/D conversion. The control bit AIM (A/D Input mode) in ACON controls the mode of channel selection. AIM = 0 is the Scan Mode, and AIM = 1 is the Select Mode. The result registers ADRES4 ... ADRES7 always contain the result of a conversion from the corresponding channels ACH4 ... CH7. However, the result registers ADRES0 ... ADRES3 depend on the mode selected. In the scan mode, ADRES0 ... ADRES3 contain the values from ACH0 ... ACH3. In the Select Mode, one of the four channels ACH0 ... ACH3 is converted four times, and the four values are stored sequentially in locations ADRES0 ... ADRES3. Its channel is selected by bits ACS1 and ACS0 (A/D Channel Select 1 and 0) in ACON.

PROGRAMMABLE COUNTER ARRAYS

The Programmable Counter Arrays (PCA–PCA1) are each made up of a Counter Module and five Register/Comparator Modules as shown below. The 16-bit output of the counter module is available to all five Register/Comparator Modules, providing one common timing reference. Each Register/Comparator Module is associated with a pin of Port 1 or Port 4 and is capable of performing input capture, output compare and pulse width modulation functions. The PCAs are exactly the same in function except for the addition of clock input sources on PCA1.

The PCA Counter and five Register/Comparator Modules each have a status bit in the CCON/C1CON Special Function Registers. These six status bits are set according to the selected modes of operation described below. The CCON/C1CON Register provides a convenient means to determine which of the six PCA/PCA1 interrupts has occurred. The EC Bit in the IE (Interrupt Enable) Special Function Register is a global interrupt enable for the PCA.

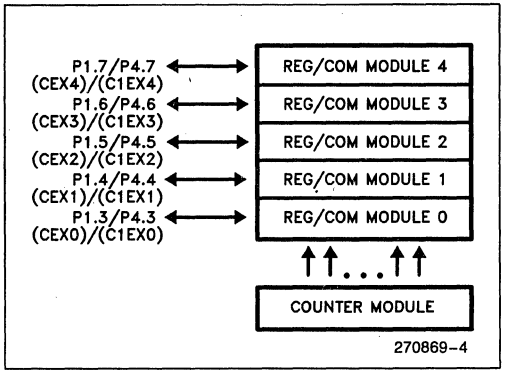


Figure 3. Programmable Counter Arrays

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 4. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL should be driven, while XTAL2 floats, as shown in Figure 5. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

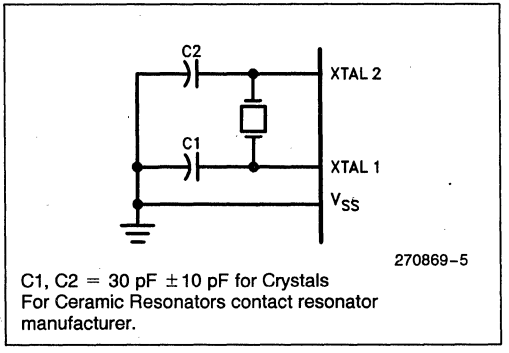


Figure 4. Oscillator Connections

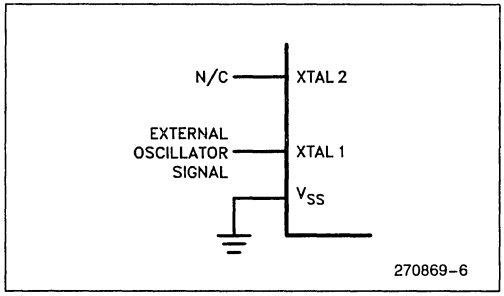


Figure 5. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during idle, peripherals continue to operate, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode. The Watchdog Timer continues to count in Idle Mode and must be serviced to prevent a device RESET while in Idle.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51GB either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt does not redefine the SFR's or change the on-chip RAM. An external interrupt will modify the interrupt associated SFR's in the same way an interrupt will in all other modes. The interrupt must be enabled and configured as level sensitive. To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level. The reset or external interrupt must be held active long enough for the oscillator to restart and stabilize. The Oscillator Fail Detect must be disabled prior to entering Power Down.

DESIGN CONSIDERATIONS

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- As $\overline{\text{RESET}}$ rises, the 8XC51GB will remain in reset for up to 5 machine cycles (60 oscillator periods) after $\overline{\text{RESET}}$ reaches V_{IH1}.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC51GB without removing it from the circuit. The ONCE Mode is invoked by:

1) Pulling ALE low while the device is in reset and $\overline{\text{PSEN}}$ is high;
2) Holding ALE low as $\overline{\text{RESET}}$ is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{\text{PSEN}}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51GB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

Watchdog Timer (WDT)

The 8XC51GB contains a dedicated Watchdog Timer (WDT) to allow recovery from a software or hardware upset. The WDT consists of a 14-bit counter which is cleared on Reset, and subsequently incremented every machine cycle. While the oscillator is running, the WDT will be incrementing and cannot be disabled. The counter may be reset by writing 1EH and E1H in sequence to the WDTRST Special Function Register. If the counter is not reset before it reaches 3FFFH (16383D), the chip will be forced into a reset sequence by the WDT. This works out to 12.28 ms @ 16 MHz. WDTRST is a write only register. The WDT does not force the external reset pin low.

While in Idle mode the WDT continues to count. If the user does not wish to exit Idle with a reset, then the processor must be periodically "woken up" to service the WDT. In Power Down mode, the WDT stops counting and holds its current value.

Serial Expansion Port (SEP)

The Serial Expansion Port is a half-duplex synchronous serial interface with the following features:

Four Clock Frequencies— XTAL/12, 24, 48, 96.

Four Interface Modes— High/Low/Falling/Rising Edges.

Interrupt Driven.

Oscillator Fail Detect (OFD)

The Oscillator Fail Detect circuitry triggers a reset if the oscillator frequency is lower than the OFD trigger frequency. It can be disabled by software by writing E1H followed by 1EH to the OFDCON register. Before going into Power Down Mode, the OFD must be disabled or it will force the GB out of Power Down. The OFD has the following features.

OFD Trigger Frequency: Below 20 KHz, the 8XC51GB will be held in reset. Above 400 KHz, the 8XC51GB will not be held is reset.

Functions in Normal and Idle Modes.

Reactivated by Reset (or External Interrupt Zero/One Pins) after Software Disable.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on EA/V_{PP}
Pin to V_{SS} .....0V to +13.0V*
I_{OL} per I/O Pin .....15 mA
Voltage on Any Other
Pin to V_{SS} .....−0.5V to +6.5V
Power Dissipation.....1.5W
(Based on Package heat transfer limitations, not device power consumption)

*OTP only.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions: T_A (under bias) = 0°C to +70°C, V_{CC} = 5.0V ±20%; V_{SS} = 0V

DC CHARACTERISTICS (Over Operating Conditions)

Symbol	Parameter	Targeted Min	Targeted Typ(1)	Targeted Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (except Port 2 and $\overline{EA}$)	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage (Port 2)	−0.5		0.2 V_{CC} − 0.3	V	
V_{IL2}	Input Low Voltage ($\overline{EA}$)	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (except XTAL1 and $\overline{RST}$)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, $\overline{RST}$)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3, 4 and 5)			0.3	V	I_{OL} = 100 μA (2,3)
				0.45	V	I_{OL} = 1.6 mA (2,3)
				1.0	V	I_{OL} = 3.5 mA (2,3)
V_{OL1}	Output Low Voltage (Port 0, $\overline{PSEN}$, ALE)			0.3	V	I_{OL} = 200 μA (2,3)
				0.45	V	I_{OL} = 3.2 mA (2,3)
				1.0	V	I_{OL} = 7.0 mA (2,3)
V_{OH}	Output High Voltage (Ports 1, 2, 3, 4 and 5, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA (4)
		V_{CC} − 0.7			V	I_{OH} = −30 μA (4)
		V_{CC} − 1.5			V	I_{OH} = −60 μA (4)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC} − 0.3			V	I_{OH} = −200 μA
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA

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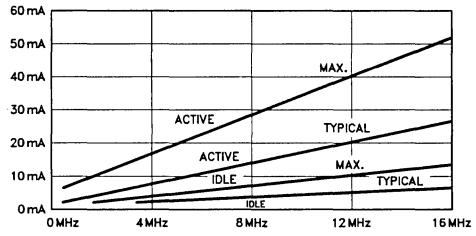
DC CHARACTERISTICS (Over Operating Conditions) (Continued)

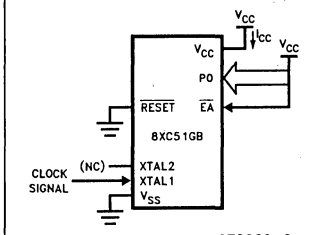
Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, 4, 5)			−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3, 4, 5)			−650	μA	V_{IN} = 2.0V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}
RRST	RST Pullup Resistor	50		300	kΩ	
C_{IO}	Pin Capacitance		10		pF	Freq = 1 MHz T_A = 25°C
I_{PD}	Power Down Current			50	μA	(5)
I_{DL}	Idle Mode Current			18	mA	(5)
I_{CC}	Operating Current			50	mA	(5)
I_{REF}	A/D Converter Reference Current			5	mA	

NOTES:
1. Typical values are obtained using V_{CC} = 5.0V, T_A = 25°C, and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per Port Pin: 10 mA
   Maximum I_{OL} per 8-Bit Port—
   Port 0: 26 mA
   Ports 1–5: 15 mA
   Maximum Total I_{OL} for All Outputs Pins: 101 mA
   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
5. See Figures 6–10 for test conditions. Minimum V_{CC} for Power Down is 2V.



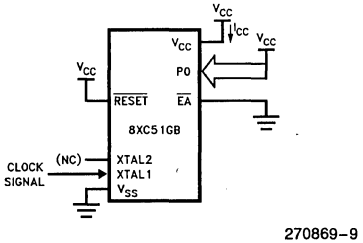
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA. $T_{CLCH} = T_{CHCL} = 5$ ns

Figure 6. I_{CC} vs Frequency



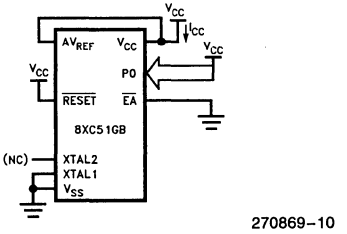
All other pins disconnected.
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition, Active Mode



All other pins disconnected.
TCLCH = TCHCL = 5 ns

Figure 8. I_{CC} Test Condition Idle Mode



All other pins disconnected.

Figure 9. I_{CC} Test Condition, Power Down Mode
V_{CC} = 2.0V to 5.5V

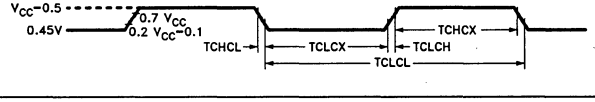


Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

AC SPECIFICATIONS

Over Operating Conditions, Load Capacitance on Port 0, ALE, and $\overline{PSEN}$ = 100 pF, Load Capacitance on all other outputs = 80 pF

EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc.		Variable Osc.		Units
		Min	Max	Min	Max	
1/TCLCL	Osc. Freq.			3.5	16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL − 40		ns
TAVLL	ADDR Valid to ALE Low	43		TCLCL − 40		ns
TLLAX	ADDR Hold after ALE Low	53		TCLCL − 30		ns

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EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS (Continued)

Symbol	Parameter	12 MHz Osc.		Variable Osc.		Units
		Min	Max	Min	Max	
TLLIV	ALE Low to Valid Inst. IN		234		4TCLCL − 100	ns
TLLPL	ALE LOW to $\overline{PSEN}$ LOW	53		TCLCL − 30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL − 45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		145		3TCLCL − 105	ns
TPXIX	Input Instr. Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr. Float after $\overline{PSEN}$		59		TCLCL − 25	ns
TAVIV	ADDR to Valid Instr. In		312		5TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to ADDR Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL − 165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		107		2TCLCL − 60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL − 150	ns
TAVDV	ADDR to Valid Data In		585		9TCLCL − 165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL − 50	3TCLCL + 50	ns
TAVWL	ADDR Valid to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL − 130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL − 50		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL − 50		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7 TCLCL − 150		ns
TRLAZ	$\overline{RD}$ Low to Addr Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL − 40	TCLCL + 40	ns

EXPLANATION OF THE AC SYMBOLS

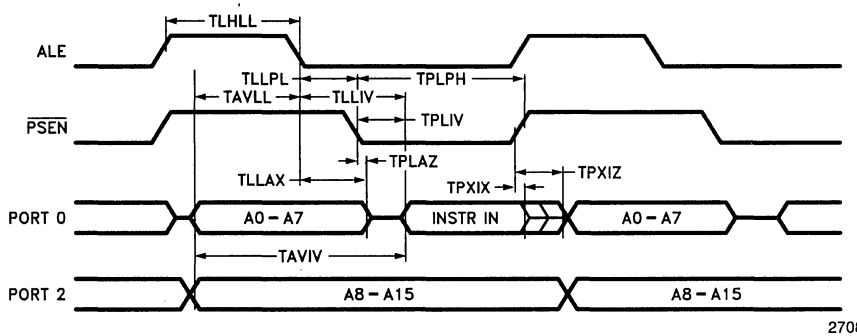
Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for:

A: Address
C: Clock
D: Input Data
H: Logic Level HIGH
I: Instruction (Program Memory Contents)
L: Logic Level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ Signal
T: Time
V: Valid
W: $\overline{WR}$ Signal
X: No Longer a Valid Logic Level
Z: Float

For Example:

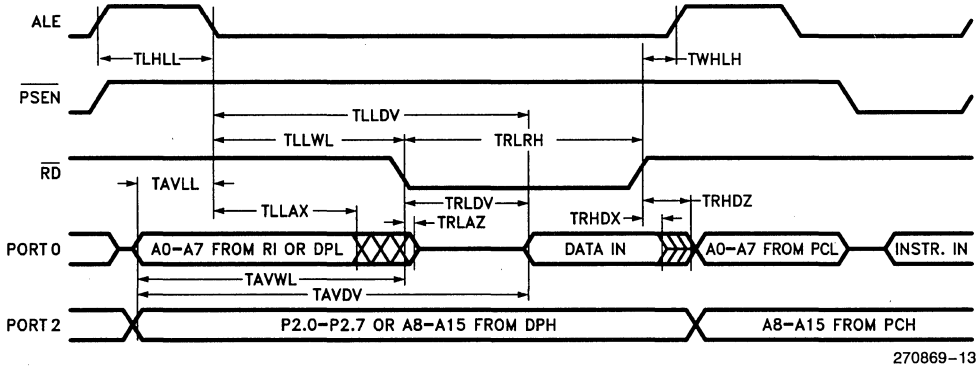
TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

EXTERNAL PROGRAM MEMORY READ CYCLE



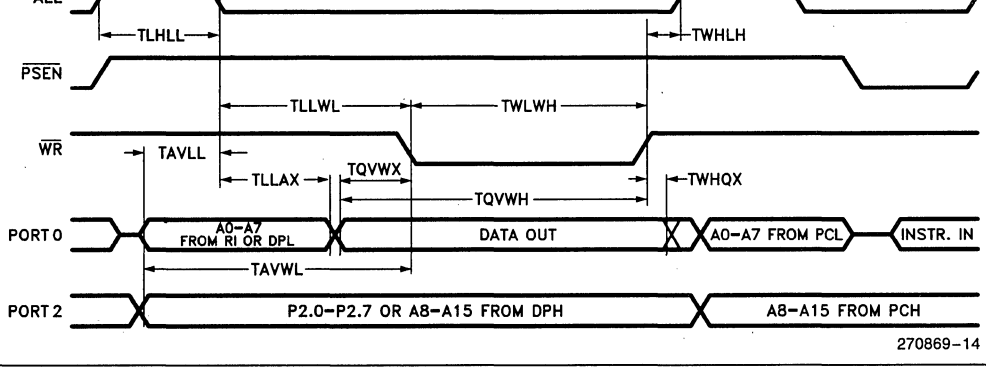
270869-12

EXTERNAL DATA MEMORY READ CYCLE



270869-13

EXTERNAL DATA MEMORY WRITE CYCLE



270869-14

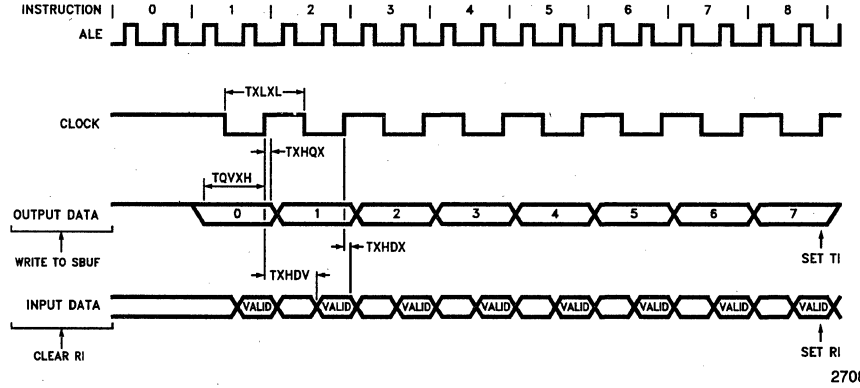
9

SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions, Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL − 117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL − 133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS

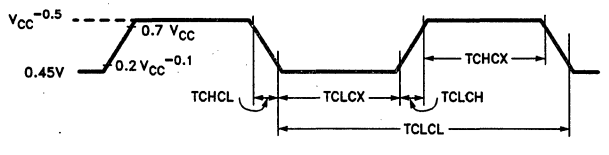


270869-15

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



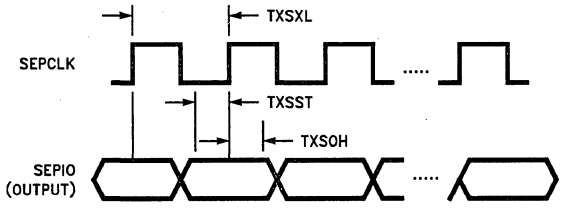
270869-16

SEP AC TIMING SPECIFICATIONS

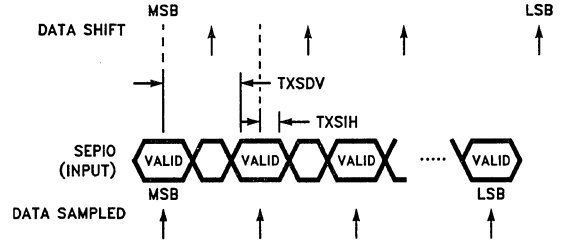
Test Conditions: Over Operating Conditions, Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXSXL	SEPCLK Cycle Time	1		12 TCLCL		μs
TXSST	Output Data Setup to SEPCLK	435		6 TCLCL − 65		ns
TXSOH	Output Data Hold after SEPCLK	445		6 TCLCL − 55		ns
TXSIH	Input Data Hold after SEPCLK Sampling Edge	210		2 TCLCL + 43		ns
TXSDV	Input Data Valid to SEPCLK Sampling Edge		947		12 TCLCL − 53	ns

SEP Waveform (SEPS1 = 0; SEPS0 = 0; CLKPOL = 0; CLKPH = 0)



270869-22



270869-23

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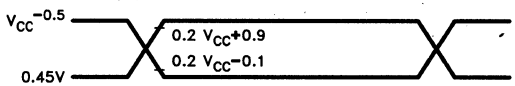
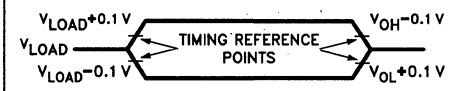
AC TESTING INPUT, OUTPUT WAVEFORMS



270869-17

AC inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.5V for a Logic "0". Timing measurements are made at V_{IH} for a Logic "1" and V_{OL} max for a Logic "0".

FLOAT WAVEFORMS



270869-18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

A TO D CHARACTERISTICS

The absolute conversion accuracy is dependent on the accuracy of AV_{REF}. The specifications given below assume adherence to the Operating Conditions section of this data sheet. Testing is done at $AV_{REF} = 5.12V$, and $V_{CC} = 5.0V$.

OPERATING CONDITIONS

V_{CC} ..... 4.0V to 6.0V
AV_{REF} ..... 4.5V to 5.5V
V_{SS}, AV_{SS} 0V
ACH0-7 ..... AV_{SS} to V_{REF}
T_A ..... 0°C to +70°C Ambient
FOSC (STD Version) ..... 3.5 MHz to 12 MHz
FOSC (-1 Version) ..... 3.5 MHz to 16 MHz

A/D CONVERTER SPECIFICATIONS T_A = 0°C to +70°C

Parameter	Min	Typ*	Max	Units**	Notes
Resolution	256 8		256 8	Levels Bits	
Absolute Error (Ch 2-7)	0		±1	LSB	
Absolute Error (Ch 0 and 1)	0		±2	LSB	
Full Scale Error		±1		LSB	
Zero Offset Error		±1		LSB	
Non-Linearity	0		±1	LSB	
Differential Non-Linearity	0		±1	LSB	
Channel-to-Channel Matching	0		±1	LSB	
Repeatability		±0.25		LSB	

A/D CONVERTER SPECIFICATIONS T_A = 0°C to +70°C (Continued)

Parameter	Min	Typ*	Max	Units**	Notes
Temperature Coefficients:					
Offset		0.003		LSB/°C	
Full Scale		0.003		LSB/°C	
Differential Non-Linearity		0.003		LSB/°C	
Input Capacitance		3		pF	
Off Isolation	−60			dB	(8, 9)
Feedthrough		−60		dB	(8)
V_{CC} Power Supply Rejection		−60		dB	(8)
Input Resistance to Sample-and-Hold Capacitor	750		1.2K	Ω	
DC Input Leakage	0		3.0	μA	

NOTES:
*These values are expected for most parts at 25°C
**AN "LSB" as used here, has a value of approximately 20 mV.
8. DC to 100 KHz
9. Multiplexer Break-Before-Make Guaranteed.
10. There is no indication when a single A/D conversion is complete. Please refer to the 8XC51GB Hardware Description on how to read a single A/D conversion.
11. T_{CY} = 12 TCLCL

A/D Conversion Time		Notes
Per Channel	26 T_{CY}	(10, 11)
8 Conversions	208 T_{CY}	(11)

9

PROGRAMMING THE OTP

The part must be running with a 4 MHz to 6 MHz oscillator. The address of a location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

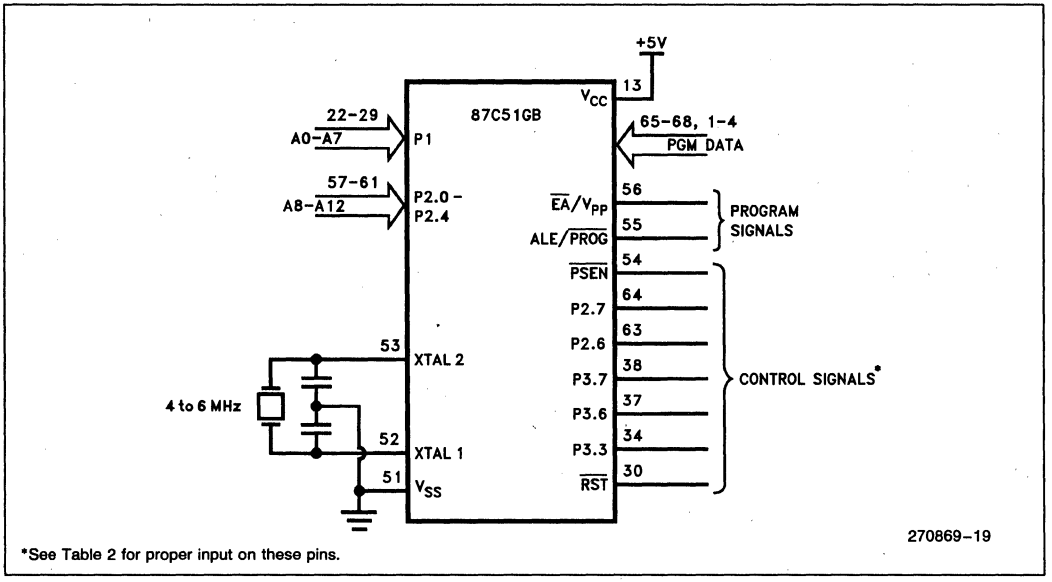
DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.4, respectively for A0–A12.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: $\overline{RST}$, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$



*See Table 2 for proper input on these pins.

Figure 11. Programming the OTP

Table 2. OTP Programming Modes

Mode		$\overline{RST}$	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		L	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		L	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		L	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	L	L	⊓	12.75V	H	H	H	H	H
	Bit 2	L	L	⊓	12.75V	H	H	H	L	L
	Bit 3	L	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		L	H	H	H	L	L	L	L	L

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 11 and 12 for address, data, and control signals set up. To program the 87C51GB the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the OTP array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte that is programmed, or after a block of bytes that is programmed. In either case a complete verify of the array will ensure that it has been programmed correctly.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled. Refer to the Program Lock section in this data sheet.

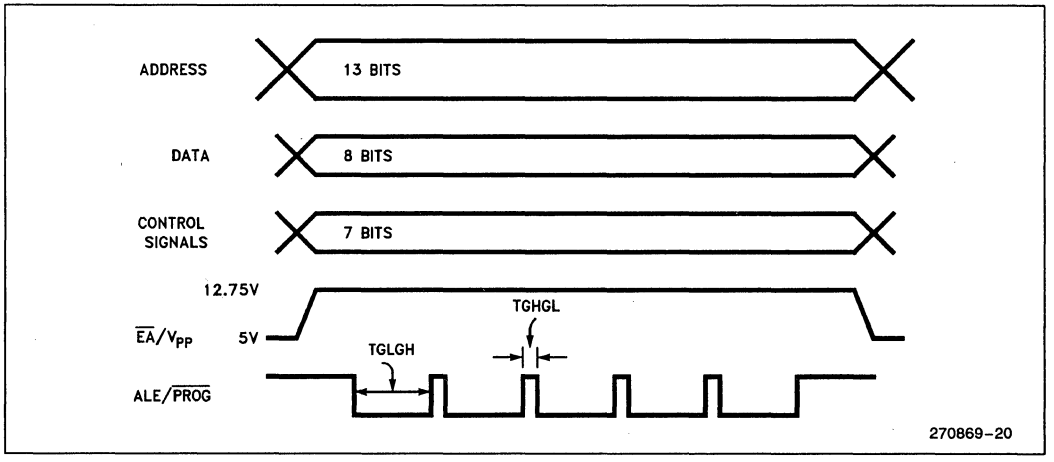


Figure 12. Programming Signal's Waveforms

ROM and EPROM Lock System

The 87C51GB and the 83C51GB program lock systems, when programmed, protect the on-board program against software piracy.

The 83C51GB has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 3. If program protection is desired, the user submits the encryption table with their code, and both the lock bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C51GB has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user programmable. See Table 3.

Encryption Array

Within the programmable array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 2.

When using the encryption array feature, one important factor needs to be considered. If a code byte has the value 0FFH, verification of the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason it is strongly recommended that all unused code bytes be programmed with some value other than 0FFH, and not all of them the same value. This practice will ensure the maximum possible program protection.

Program Lock Bits

The 87C51GB has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code **and data**. The 83C51GB has 1 program lock bit. See line 2 of Table 3.

Reading the Signature Bytes

The 8XC51GB has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents	
	87C51GB	83C51GB
30H	89H	89H
31H	58H	58H
60H	EBH	EBH/6BH

Table 3. Program Lock Bits and the Features

	*Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed).
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

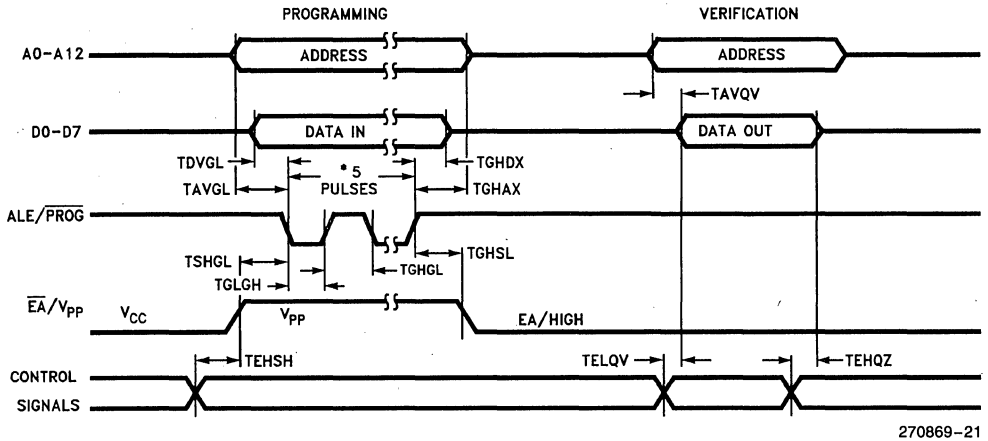
*Any other combination of lock bits is not defined.

OTP PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ± 20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

PROGRAMMING AND VERIFICATION WAVEFORMS



270869-21

*25 Pulses for Encryption Table and Lock Bits.

A/D Glossary of Terms

Absolute Error—The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

Actual Characteristic—The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An actual characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversions under the same conditions.

Break-Before-Make—The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected (e.g., the converter will not short inputs together).

Channel-to-Channel Matching—The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

Characteristic—A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

Code—The digital value output by the converter.

Code Center—The voltage corresponding to the midpoint between two adjacent code transitions.

Code Transition—The point at which the converter changes from an output code of Q, to a code of Q + 1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

Code Width—The voltage corresponding to the difference between two adjacent code transitions.

Crosstalk—See "Off-Isolation".

DC Input Leakage—Leakage current to ground from an analog input pin.

Differential Non-Linearity—The difference between the ideal and actual code widths of the terminal based characteristic.

Feedthrough—Attenuation of a voltage applied on the selected channel of the A/D Converter after the sample window closes.

Full Scale Error—The difference between the expected and actual input voltage corresponding to the full scale code transition.

Ideal Characteristic—A characteristic with its first code transition at V_{IN} = 0.5 LSB, its last code transition at V_{IN} = (V_{REF} − 1.5 LSB) and all code widths equal to one LSB.

Input Resistance—The effective series resistance from the analog input pin to the sample capacitor.

LSB—Least Significant Bit—The voltage corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For an 8-bit converter with a reference voltage of 5.12V, one LSB is 20 mV. Note that this is different than digital LSBs since an uncertainty of two LSBs, when referring to an A/D converter, equals 40 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 80 mV).

Monotonic—The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

No Missed Codes—For each and every output code, there exists a unique input voltage range which produces that code only.

Non-Linearity—The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristic.

Off-Isolation—Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

Repeatability—The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

Resolution—The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

Sample Delay—The delay from receiving the start conversion signal to when the sample window opens.

Sample Delay Uncertainty—The variation in the sample delay.

Sample Time—The time that the sample window is open.

Sample Time Uncertainty—The variation in the sample time.

Sample Window—Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

Successive Approximation—An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

Temperature Coefficients—Change in the stated variable per degree centrigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effect of temperature drift.

Terminal Based Characteristic—An actual characteristic which has been rotated and translated to remove zero offset and full scale error.

V_{CC} Rejection—Attenuation of noise on the V_{CC} line to the A/D converter.

Zero Offset—The difference between the expected and actual input voltage corresponding to the first code transition.

DATA SHEET REVISION SUMMARY

The following differences exist between this data sheet and the previous version (270869-002):

1. Changed data sheet status from "Advance Information" to "Preliminary" and updated associated notices.
2. Added 83C51GB throughout.
3. Added Package and Process Information.
4. Clarified ±2 LSB accuracy for channels 0 and 1 in A/D Converter Section.
5. Added "ROM and EPROM Lock System" section and added 83C51GB to "Program Lock Bits" section.
6. Modified Signature Bytes Table.

The following differences exist between the 270869-002 data sheet and the previous version (270869-001):

1. Changed data sheet status from "Product Preview" to "Advance Information" and updated associated notices.
2. Asynchronous port reset was added to $\overline{\text{RESET}}$ pin description.
3. ALE disable paragraph was added to ALE pin description.
4. C_1, C_2 guidelines clarified in Figure 4.
5. Operating Conditions heading was added.
6. Maximum I_{OL} per I/O pin was added to Absolute Maximum Ratings.
7. $VT+$, $VT-$, V_{HYS}, V_{OL2}, and V_{TL} removed.
8. V_{OL} value for ALE included with V_{OL1}.
9. V_{IL1} and V_{IL2} added.
10. RRST minimum changed from 40K to 50K. RRST maximum changed from 225K to 300K.
11. I_{PD} maximum changed from 200 μA to 50 μA.
12. I_{DL} maximum changed from 15 mA to 18 mA.
13. Typical values for I_{PD}, I_{DL}, I_{CC}, and I_{REF} removed.
14. Note 3 (page 9) was reworded.
15. SEP AC Timings added.
16. A/D Absolute Error for Channels 0 and 1 changed to ±2 LSB.
17. T_{CY} clarified.
18. Encryption array paragraph was added.
19. Corrected pin numbers on Figure 11 to reflect PLCC package.

87C51GB/80C51GB
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Express

87C51GB—8K Bytes OTP/Factory Programmable ROM

80C51GB—CPU with RAM and I/O

3.5 MHz—16 MHz ±20% V_{CC}

- **Extended Temperature Range (−40°C to +85°C)**
- **8K Bytes On-Chip ROM/OTP ROM**
- **256 Bytes of On-Chip Data RAM**
- **Two Programmable Counter Arrays with:**
  - **— 2 x 5 High Speed Input/Output Channels Compare/Capture**
  - **— Pulse Width Modulators**
  - **— Watchdog Timer Capabilities**
- **Three 16-Bit Timer/Counters with**
  - **— Four Programmable Modes:**
  - **— Capture, Baud Rate Generation (Timer 2)**
- **Dedicated Watchdog Timer**
- **8-Bit, 8-Channel A/D with:**
  - **— Eight 8-Bit Result Registers**
  - **— Four Programmable Modes**
- **Programmable Serial Channel with:**
  - **— Framing Error Detection**
  - **— Automatic Address Recognition**
- **Serial Expansion Port**
- **Programmable Clock Out**
- **48 Programmable I/O Lines with:**
  - **— 40 Schmitt Trigger Inputs**
- **15 Interrupt Sources with:**
  - **— 7 External, 8 Internal Sources**
  - **— 4 Programmable Priority Levels**
- **Pre-Determined Port States**
- **High Performance CHMOS Process**
- **TTL and CHMOS Compatible Logic Levels**
- **Power Saving Modes**
- **64K External Data Memory Space**
- **64K External Program Memory Space**
- **Three Level Program Lock System**
- **ONCE™ (ON-Circuit Emulation) Mode**
- **Quick Pulse Programming™ Algorithm**
- **MCS®-51 Fully Compatible Instruction Set**
- **Boolean Processor**
- **Oscillator Fail Detect**
- **Available in 68-Pin PLCC**

The Intel EXPRESS system offers enhancements to the operation specifications of the MCS-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The 87C51GB EXPRESS is packaged in the 68-lead PLCC package. In order to designate a part as an EXPRESS part, a 'T' is added as a prefix to the part number. TN87C51GB denotes an EXPRESS part in a PLCC package.

All A.C. and D.C. parameters in the commercial data sheets apply to the EXPRESS devices.

July 1990
Order Number: 270889-001

83C152 Hardware Description and Data Sheet

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intel®

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August 1990

83C152 Hardware Description

Order Number: 270427-004

83C152 HARDWARE DESCRIPTION

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83C152 HARDWARE DESCRIPTION

1.0 INTRODUCTION

The 83C152 Universal Communications Controller is an 8-bit microcontroller designed for the intelligent management of peripheral systems or components. The 83C152 is a derivative of the 80C51BH and retains the same functionality. The 83C152 is fabricated on the same CHMOS III process as the 80C51BH. What makes the 83C152 different is that it has added functions and peripherals to the basic 80C51BH architecture that are supported by new Special Function Registers (SFRs). These enhancements include: a high speed multi-protocol serial communication interface, two channels for DMA transfers, HOLD/HLDA bus control, a fifth I/O port, expanded data memory, and expanded program memory.

In addition to a standard UART, referred to here as Local Serial Channel (LSC), the 83C152 has an onboard multi-protocol communication controller called the Global Serial Channel (GSC). The GSC interface supports SDLC, CSMA/CD, user definable protocols, and a subset of HDLC protocols. The GSC capabilities include: address recognition, collision resolution, CRC generation, flag generation, automatic retransmission, and a hardware based acknowledge feature. This high speed serial channel is capable of implementing the Data Link Layer and the Physical Link Layer as shown in the OSI open systems communication model. This model can be found in the document "Reference Model for Open Systems Interconnection Architecture", ISO/TC97/SC16 N309.

The DMA circuitry consists of two 8-bit DMA channels with 16-bit addressability. The control signals; Read ($\overline{RD}$), Write ($\overline{WR}$), hold and hold acknowledge (HOLD/HLDA) are used to access external memory. The DMA channels are capable of addressing up to 64K bytes (16 bits). The destination or source address can be automatically incremented. The lower 8 bits of the address are multiplexed on the data bus Port 0 and the upper eight bits of address will be on Port 2. Data is transmitted over an 8-bit address/data bus. Up to 64K bytes of data may be transmitted for each DMA activation.

The new I/O port (P4) functions the same as Ports 1-3, found on the 80C51BH.

Internal memory has been doubled in the 83C152. Data memory has been expanded to 256 bytes, and internal program memory has been expanded to 8K bytes.

There are also some specific differences between the 83C152 and the 80C51BH. The first is that the numbering system between the 83C152 and the 80C51BH is slightly different. The 83C152 and the 80C51BH are factory masked ROM devices. The 80C152 and the 80C31BH are ROMless devices which require the use of external program memory. The second difference is that RESET is active low in the 83C152 and active high in the 80C51BH. This is very important to designers who may currently be using the 80C51BH and planning to use the 83C152, or are planning on using both devices on the same board. The third difference is that GF0 and GF1, general purpose flags in PCON, have been renamed GFIEN and XRCLK. GFIEN enables idle flags to be generated in SDLC mode, and XRCLK enables the receiver to be externally clocked. All of the previously unused bits are now being used and interrupt vectors have been added to support the new enhancements. Programmers using old code generated for the 80C51BH will have to examine their programs to ensure that new bits are properly loaded, and that the new interrupt vectors will not interfere with their program.

Throughout the rest of this manual the 80C152 and the 83C152 will be referred to generically as the "C152".

The C152 is based on the 80C51BH architecture and utilizes the same 80C51BH instruction set. Figure 1.1 is a block diagram of the C152. Readers are urged to compare this block diagram with the 80C51BH block diagram. There have been no new instructions added. All the new features and peripherals are supported by an extension of the Special Function Registers (SFRs). Very little of the information pertaining specifically to the 80C51BH core will be discussed in this chapter. The detailed information on such functions as: the instruction set, port operation, timer/counters, etc., can be found in the MCS®-51 Architecture chapter in the Intel Embedded Controller Handbook. Knowledge of the 80C51BH is required to fully understand this manual and the operation of the C152. To gain a basic understanding on the operation of the 80C51BH, the reader should familiarize himself with the entire MCS-51 chapter of the Embedded Controller Handbook.

Another source of information that the reader may find helpful is Intel's LAN Components User's Manual, order number 230814. Inside are descriptions of various protocols, application examples, and application notes dealing with different serial communication environments.

2.0 COMPARISON OF 80C152 AND 80C51BH FEATURES

2.1 Memory Space

A good understanding of the memory space and how it is used in the operation of MCS-51 products is essential. All the enhancements on the C152 are implemented by accessing Special Function Registers (SFRs), added data memory, or added program memory.

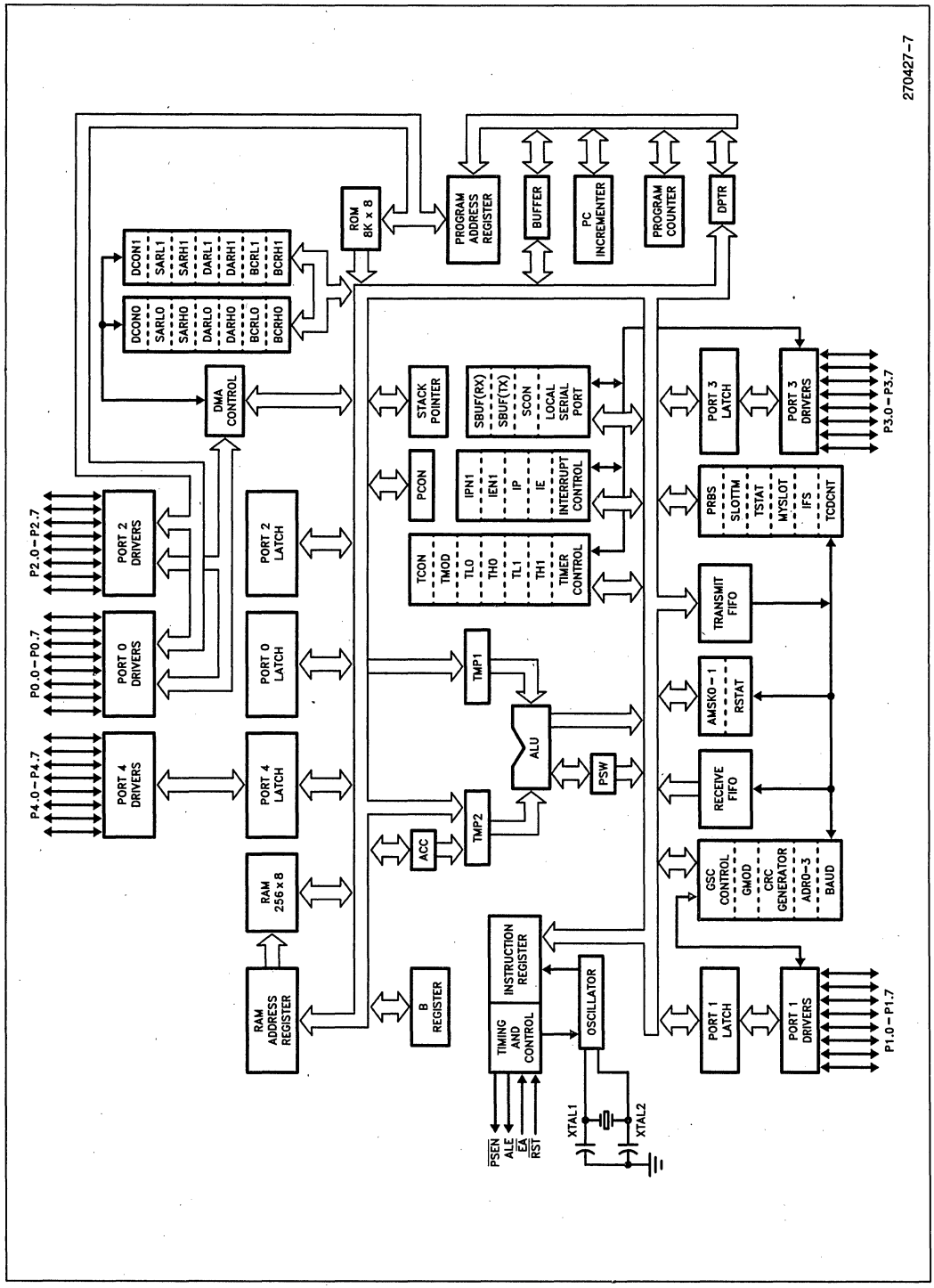


Figure 1.1. Block Diagram

2.1.1 SPECIAL FUNCTION REGISTERS (SFRs)

The following list contains all the SFRs, their names and function. All of the SFRs of the 80C51BH are retained and for a detailed explanation of their operation, please refer to the chapter, "Hardware Description of the 8051 and 8052" that is found in the Embedded Controller Handbook. An overview of the new SFRs is found in Section 2.1.1.1, with a detailed explanation in Section 3.7, Section 4.5, and 6.0.

2.1.1.1 New SFRs

The following descriptions are quick overviews of the new SFRs, and not intended to give a complete understanding of their use. The reader should refer to the detailed explanation in Section 3 for the GSC SFRs, and Section 4 for the DMA SFRs.

ADR 0,1,2,3 - (95H, 0A5H, 0B5H, 0C5H) Contains the four bytes for address matching during GSC operation.

AMSK0 - (0D5H) Selects "don't care" bits to be used with ADR0.

AMSK1 - (0E5H) Selects "don't care" bits to be used with ADR1.

BAUD - (94H) Contains the programmable value for the baud rate generator for the GSC. The baud rate will equal (fosc)/((BAUD + 1) × 8).

BCRL0 - (0E2H) Contains the low byte of a count-down counter that determines when the DMA access for Channel 0 is complete.

BCRH0 - (0E3H) Contains the high byte for count-down counter for Channel 0.

BCRL1 - (0F2H) Same as BCRL0 except for DMA Channel 1.

BCRH1 - (0F3H) Same as BCRH0 except for DMA Channel 1.

BKOFF - (0C4H) An 8-bit count-down timer used with the CSMA/CD resolution algorithm.

DARL0 - (0C2H) Contains the low byte of the destination address for DMA Channel 0.

DARH0 - (0C3H) Contains the high byte of the destination address for DMA Channel 0.

DARL1 - (0D2H) Same as DARL0 except for DMA Channel 1.

DARH1 - (0D3H) Same as DARH0 except for DMA Channel 1.

DCON0 - (92H) Contains the Destination Address Space bit (DAS), Increment Destination Address bit (IDA), Source Address Space bit (SAS), Increment Source Address bit (ISA), DMA Channel Mode bit (DM), Transfer Mode bit (TM), DMA Done bit (DONE), and the GO bit (GO). DCON0 is used to control DMA Channel 0.

DCON1 - (93H) Same as DCON0 except this is for DMA Channel 1.

GMOD - (84H) Contains the Protocol bit (PR), the Preamble Length (PL1,0), CRC Type (CT), Address Length (AL), Mode select (M1,0), and External Transmit Clock (TXC). This register is used for GSC operation only.

IEN1 - (0C8H) Interrupt enable register for DMA and GSC interrupts.

IFS - (0A4H) Determines the number of bit times separating transmitted frames.

IPN1 - (0F8H) Interrupt priority register for DMA and GSC interrupts.

MYSLOT - (0F5H) Contains the Jamming mode bit (DCJ), the Deterministic Collision Resolution Algorithm bit (DCR), and the DCR slot address for the GSC.

P4 - (0C0H) Contains the memory "image" of Port 4.

PRBS - (0E4H) Contains a pseudo-random number to be used in CSMA/CD backoff algorithms. May be read or written to by user software.

RFIFO - (F4H) RFIFO is used to access a 3-byte FIFO that contains the receive data from the GSC.

RSTAT - (0E8H) Contains the Hardware Based Acknowledge Enable bit (HABEN), Global Receive Enable bit (GREN), Receive FIFO Not Empty bit (RFNE), Receive Done bit (RDN), CRC Error bit (CRCE), Alignment Error bit (AE), Receiver Collision/Abort detect bit (RCABT), and the Overrun bit (OVR), used with both DMA and GSC.

SARL0 - (0A2H) Contains the low byte of the source address for DMA transfers.

SARH0 - (0A3H) Contains the high byte of the source address for DMA transfers.

SARL1 - (0B2H) Same as SARL0 but for DMA Channel 1.

SARH1 - (0B3H) Same as SARH1 but for DMA Channel 1.

SLOTTM - (0B4H) Determines the length of the slot time in CSMA/CD.

TCDCNT - (0D4H) Contains the number of collisions in the current frame if using CSMA/CD GSC.

Old(O)/New(N)	Name	Addr	Function
O	A	0E0H	ACCUMULATOR
N	ADR0	095H	GSC MATCH ADDRESS 0
N	ADR1	0A5H	GSC MATCH ADDRESS 1
N	ADR2	0B5H	GSC MATCH ADDRESS 2
N	ADR3	0C5H	GSC MATCH ADDRESS 3
N	AMSK0	0D5H	GSC ADDRESS MASK 0
N	AMSK1	0E5H	GSC ADDRESS MASK 1
O	B	0F0H	B REGISTER
N	BAUD	094H	GSC BAUD RATE
N	BCRL0	0E2H	DMA BYTE COUNT 0 (LOW)
N	BCRH0	0E3H	DMA BYTE COUNT 0 (HIGH)
N	BCRL1	0F2H	DMA BYTE COUNT 1 (LOW)
N	BCRH1	0F3H	DMA BYTE COUNT 1 (HIGH)
N	BKOFF	0C4H	GSC BACKOFF TIMER
N	DARL0	0C2H	DMA DESTINATION ADDR 0 (LOW)
N	DARH0	0C3H	DMA DESTINATION ADDR 0 (HIGH)
N	DARL1	0D2H	DMA DESTINATION ADDR 1 (LOW)
N	DARH1	0D3H	DMA DESTINATION ADDR 1 (HIGH)
N	DCON0	092H	DMA CONTROL 0
N	DCON1	093H	DMA CONTROL 1
O	DPH	083H	DATA POINTER (HIGH)
O	DPL	082H	DATA POINTER (LOW)
N	GMOD	084H	GSC MODE
O	IE	0A8H	INTERRUPT ENABLE REGISTER 0
N	IEN1	0C8H	INTERRUPT ENABLE REGISTER 1
N	IFS	0A4H	GSC INTERFRAME SPACING
O	IP	0B8H	INTERRUPT PRIORITY REGISTER 0
N	IPN1	0F8H	INTERRUPT PRIORITY REGISTER 1
N	MYSLOT	0F5H	GSC SLOT ADDRESS
O	P0	080H	PORT 0
O	P1	090H	PORT 1
O	P2	0A0H	PORT 2
O	P3	0B0H	PORT 3
N	P4	0C0H	PORT 4
N	P5	091H	PORT 5
N	P6	0A1H	PORT 6
O	PCON	087H	POWER CONTROL
N	PRBS	0E4H	GSC PSEUDO-RANDOM SEQUENCE
O	PSW	0D0H	PROGRAM STATUS WORD
N	RFIFO	0F4H	GSC RECEIVE BUFFER
N	RSTAT	0E8H	RECEIVE STATUS (DMA & GSC)
N	SARL0	0A2H	DMA SOURCE ADDR 0 (LOW)
N	SARH0	0A3H	DMA SOURCE ADDR 0 (HIGH)
N	SARL1	0B2H	DMA SOURCE ADDR 1 (LOW)
N	SARH1	0B3H	DMA SOURCE ADDR 1 (HIGH)
O	SBUF	099H	LOCAL SERIAL CHANNEL (LSC) BUFFER
O	SCON	098H	LOCAL SERIAL CHANNEL (LSC) CONTROL
N	SLOTTM	0B4H	GSC SLOT TIME
O	SP	081H	STACK POINTER
N	TCDCNT	0D4H	GSC TRANSMIT COLLISION COUNTER
O	TCON	088H	TIMER CONTROL
N	TFIFO	085H	GSC TRANSMIT BUFFER
O	TH0	08CH	TIMER 0 (HIGH)
O	TH1	08DH	TIMER 1 (HIGH)
O	TL0	08AH	TIMER 0 (LOW)
O	TL1	08BH	TIMER 1 (LOW)
O	TMOD	089H	TIMER MODE
N	TSTAT	0D8H	TRANSMIT STATUS (DMA & GSC)

TFIFO - (85H) TFIFO is used to access a 3-byte FIFO that contains the transmission data for the GSC.

TSTAT - (0D8H) Contains the DMA Service bit (DMA), Transmit Enable bit (TEN), Transmit FIFO Not Full bit (TFNF), Transmit Done bit (TDN), Transmit Collision Detect bit (TCDT), Underrun bit (UR), No Acknowledge bit (NOACK), and the Receive Data Line Idle bit (LNI). This register is used with both DMA and GSC.

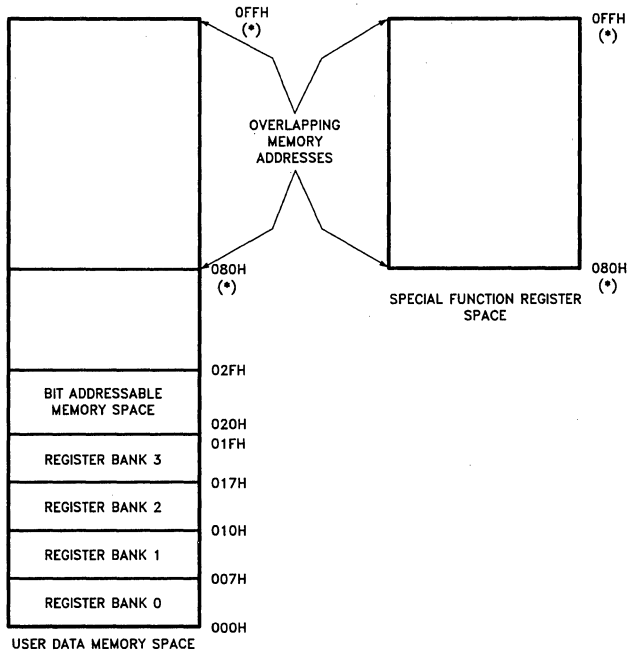
The general purpose flag bits (GF0 and GF1) that exist on the 80C51BH are no longer available on the C152. GF0 has been renamed GFIEN (GSC Flag Idle Enable) and is used to enable idle fill flags. Also GF1 has been renamed XRCLK (External Receive Clock Enable) and is used to enable the receiver to be clocked externally.

2.1.2 DATA MEMORY

Internal data memory consists of 256 bytes as shown in Figure 2.1. The first 128 bytes are addressed exactly like an 80C51BH, using direct addressing.

The addresses of the second 128 bytes of data memory happen to overlap the SFR addresses. The SFRs and their memory locations are shown in Figure 2.2. This means that internal data memory spaces have the same address as the SFR address. However, each type of memory is addressed differently. To access data memory above 80H, indirect addressing or the DMA channels must be used. To access the SFRs, direct addressing is used. When direct addressing is used, the address is the source or destination, e.g. MOV A, 10H, moves the contents of location 10H into the accumulator. When indirect addressing is used, the address of the destination or source exists within another register, e.g. MOV A, @R0. This instruction moves the contents of the memory location addressed by R0 into the accumulator. Directly addressing the locations 80H to 0FFH will access the SFRs. Another form of indirect addressing is with the use of Stack Pointer Operations. If the Stack Pointer contains an address and a PUSH or POP instruction is executed, indirect addressing is actually used. Directly accessing an unused SFR address will give undefined results.

Physically, there are separate SFR memory and data memory spaces allocated on the chip. Since there are separate spaces, the SFRs do not diminish the available data memory space.



***NOTE:**
User data memory above 80H must be addressed indirectly. Using direct addressing above 80H accesses the Special Function Registers.

Figure 2.1. Data Memory Map

External data memory is accessed like an 80C51BH, with "MOVX" instructions. Addresses up to 64K may be accessed when using the Data Pointer (DPTR). When accessing external data memory with the DPTR, the address appears on Port 0 and 2. When using the DPTR, if less than 64K of external data memory is used, the address is emitted on all sixteen pins. This means that when using the DPTR, the pins of Port 2 not used for addresses cannot be used for general purpose I/O. An alternative to using 16-bit addresses with the DPTR is to use R0 or R1 to address the external data memory. When using the registers to address external data memory, the address range is limited to 256 bytes. However, software manipulation of I/O Port 2 pins as normal I/O, allows this 256 bytes restriction to be expanded via bank switching. When using R0 or R1 as data pointers, Port 2 pins that are not used for addressing, can be used as general purpose I/O.

2.1.2.1 Bit Addressable Memory

The C152 has several memory spaces in which the bits are directly addressed by their location. The directly addressable bits and their symbolic names are shown in Figure 2.3A, 2.3B, and 2.3C.

Bit addresses 0 to 7FH reside in on-board user data RAM in byte addresses 20H to 2FH (see Figure 2.3A).

Bit addresses 80H to 0FFH reside in the SFR memory space, but not every SFR is bit addressable, see Figure 2.3B. The addressable bits are scattered throughout the SFRs. The addressable bits occur every eighth SFR address starting at 80H and occupy the entire byte. Most of the bits that are addressable in the SFRs have been given symbolic names. These names will often be referred to in this or other documentation on the C152. Most assemblers also allow the use of the symbolic names when writing in assembly language. These names are shown in Figure 2.3C.

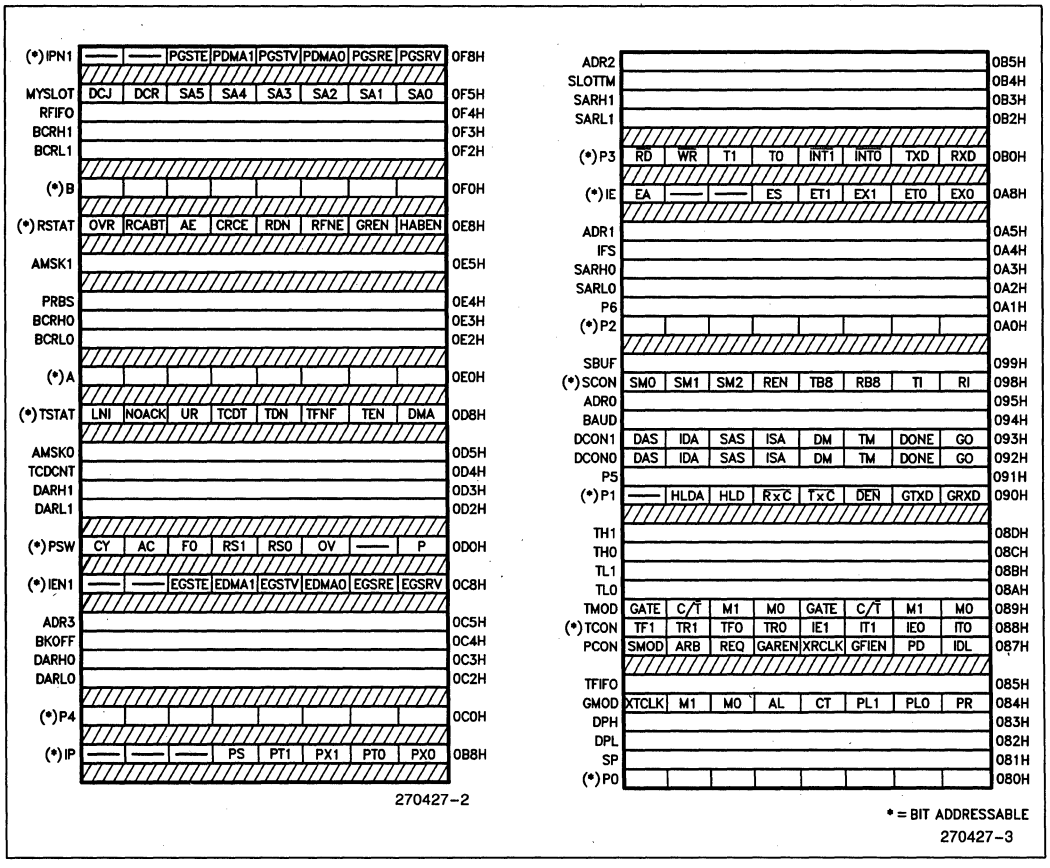


Figure 2.2. Special Function Registers

Data Memory Map (bits):

Byte Address	BIT ADDRESSES (MSB)							(LSB)
020H	07	06	05	04	03	02	01	00
021H	0F	0E	0D	0C	0B	0A	09	08
022H	17	16	15	14	13	12	11	10
023H	1F	1E	1D	1C	1B	1A	19	18
024H	27	26	25	24	23	22	21	20
025H	2F	2E	2D	2C	2B	2A	29	28
026H	37	36	35	34	33	32	31	30
027H	3F	3E	3D	3C	3B	3A	39	38
028H	47	46	45	44	43	42	41	40
029H	4F	4E	4D	4C	4B	4A	49	48
02AH	57	56	55	54	53	52	51	50
02BH	5F	5E	5D	5C	5B	5A	59	58
02CH	67	66	65	64	63	62	61	60
02DH	6F	6E	6D	6C	6B	6A	69	68
02EH	77	76	75	74	73	72	71	70
02FH	7F	7E	7D	7C	7B	7A	79	78

Figure 2.3A. Bit Addresses

Byte Address	BIT ADDRESSES (MSB)							(LSB)	
080H	87	86	85	84	83	82	81	80	(P0)
088H	8F	8E	8D	8C	8B	8A	89	88	(TCON)
090H	97	96	95	94	93	92	91	90	(P1)
098H	9F	9E	9D	9C	9B	9A	99	98	(SCON)
0A0H	A7	A6	A5	A4	A3	A2	A1	A0	(P2)
0A8H	AF	–	–	AC	AB	AA	A9	A8	(IE)
0B0H	B7	B6	B5	B4	B3	B2	B1	B0	(P3)
0B8H	–	–	–	BC	BB	BA	B9	B8	(IP)
0C0H	C7	C6	C5	C4	C3	C2	C1	C0	(P4)
0C8H	–	–	CD	CC	CB	CA	C9	C8	(IEN1)
0D0H	D7	D6	D5	D4	D3	D2	D1	D0	(PSW)
0D8H	DF	DE	DD	DC	DB	DA	D9	D8	(TSTAT)
0E0H	E7	E6	E5	E4	E3	E2	E1	E0	(A)
0E8H	EF	EE	ED	EC	EB	EA	E9	E8	(RSTAT)
0F0H	F7	F6	F5	F4	F3	F2	F1	F0	(B)
0F8H	–	–	FD	FC	FB	FA	F9	F8	(IPN1)

Figure 2.3B. Bit Addresses

Byte Address	SYMBOLIC NAME BIT MAP (MSB)							(LSB)	
080H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	(P0)
088H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	(TCON)
090H	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	(P1)
098H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	(SCON)
0A0H	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	(P2)
0A8H	EA	—	—	ES	ET1	EX1	ET0	EX0	(IE)
0B0H	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	(P3)
0B8H	—	—	—	PS	PT1	PX1	PT0	PX0	(IP)
0C0H	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	(P4)
0C8H	—	—	EGSTE	EDMA1	EGSTV	EDMA0	EGSRE	EGSRV	(IEN1)
0D0H	CY	AC	F0	RS1	RS0	OV	—	P	(PSW)
0D8H	LNI	NOACK	UR	TCDT	TDN	TFNF	TEN	DMA	(TSTAT)
0E0H									(A)
0E8H	OVR	RCABT	AE	CRCE	RDN	RFNE	GREN	HABEN	(RSTAT)
0F0H									(B)
0F8H	—	—	PGSTE	PDMA1	PGSTV	PDMA0	PGSRE	PGSRV	(IPN1)

Figure 2.3C. Bit Addresses

2.1.3 PROGRAM MEMORY

The 83C152 contains 8K of ROM program memory, and the 80C152 uses only external program memory. Figure 2.4 shows the program memory locations and where they reside. The user is allowed a maximum of 64K of program memory. In the 83C152 program memory fetches beyond 8K automatically access external program memory. When program memory is externally addressed, all of the Port 2 pins emit the address. Since all of Port 2 is affected by the address, unused address pins cannot be used as normal I/O ports even if less than 64K of memory is being accessed.

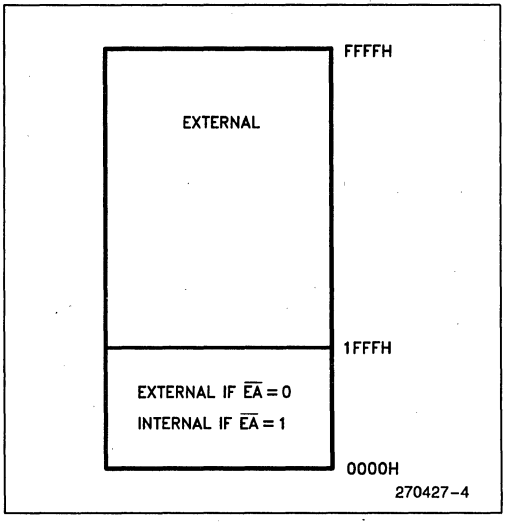


Figure 2.4. Program Memory

2.2 Interrupt Structure

The C152 retains all five interrupts of the 80C51BH. In addition, six new interrupts have been added for a total of 11 available interrupts. Two SFRs have been added to the C152 for control of the new interrupts. These added SFRs are IEN1 (C8H) for enabling the interrupts and IPN1 (F8H) for setting the priority. For an explanation on how the priority of interrupts affects their operation please refer to the MCS-51 Architecture and Hardware Chapters in the Intel Embedded Controller Handbook. A detailed description on how the interrupts function is in the MCS®-51 Architectural Overview.

IEN1 FUNCTIONS			
Symbol	**Position**	**Vector**	**Function**
—	IEN1.7		**RESERVED** and do not exist on chip.
—	IEN1.6		**RESERVED** and do not exist on chip.
EGSTE	IEN1.5	04BH	**GSC TRANSMIT ERROR**—The interrupt service routine at 4BH is invoked if NOACK or TCDT is set when the GSC is under CPU control and EGSTE is enabled. This interrupt service routine is invoked if NOACK, TCDT, or UR is set when the GSC is under DMA control and EGSTE is enabled.
EDMA1	IEN1.4	053H	**DMA CHANNEL REQUEST 1**—The interrupt service routine at 53H is invoked when DCON1.1 (DONE) is set and EDMA1 is enabled.
EGSTV	IEN1.3	043H	**GSC TRANSMIT VALID**—The interrupt service routine at 43H is invoked if TFNF is set when the GSC is under CPU control and EGSTV is enabled. This interrupt service routine is invoked if TDN is set when the GSC is under DMA control and EGSTV is enabled.
EDMA0	IEN1.2	03BH	**DMA CHANNEL REQUEST 0**—The interrupt service routine at 3BH will be invoked when DCON0.1 (DONE) is set and EDMA0 is enabled.
EGSRE	IEN1.1	033H	**GSC RECEIVE ERROR**—The interrupt service routine at 33H is invoked if CRCE, OVR, RCABT, or AE is set when the GSC is under CPU or DMA control and EGSRE is enabled.
EGSRV	IEN1.0	02BH	**GSC RECEIVE VALID**—The interrupt service routine at 2BH is invoked if RFNE is set when the GSC is under CPU control and EGSRV is enabled. This interrupt service routine is invoked if RDN is set when the GSC is under DMA control and EGSRV is enabled.

IPN1 is used the same way the current 80C51BH interrupt priority register (IP) is. By assigning a "1" to the appropriate bit, that interrupt has a higher priority than an interrupt with a "0" assigned to it in the priority register.

The new interrupt priority register (IPN1) contents are:

Symbol	Position	Function
PGSTE	IPN1.5	GSC TRANSMIT ERROR
PDMA1	IPN1.4	DMA CHANNEL REQUEST 1
PGSTV	IPN1.3	GSC TRANSMIT VALID
PDMA0	IPN1.2	DMA CHANNEL REQUEST 0
PGSRE	IPN1.1	GSC RECEIVE ERROR
PGSRV	IPN1.0	GSC RECEIVE VALID

The eleven interrupts are sampled in the following order when assigned the same priority level in the IP and IPN1 registers:

Priority Sequence	Priority Symbolic Address	Priority Symbolic Name	Interrupt Symbolic Address	Interrupt Symbolic Name	Vector Address	
1	IP.0	PX0	IE.0	EX0	03H	(FIRST)
2	IPN1.0	PGSRV	IEN1.0	EGSRV	2BH	
3	IP.1	PT0	IE.1	ET0	0BH	
4	IPN1.1	PGSRE	IEN1.1	EGSRE	33H	
5	IPN1.2	PDMA0	IEN1.2	EDMA0	3BH	
6	IP.2	PX1	IE.2	EX1	13H	
7	IPN1.3	PGSTV	IEN1.3	EGSTV	43H	
8	IPN1.4	PDMA1	IEN1.4	EDMA1	53H	
9	IP.3	PT1	IE.3	ET1	1BH	
10	IPN1.5	PGSTE	IEN1.5	EGSTE	4BH	
11	IP.4	PS	IE.4	ES	23H	(LAST)

2.3 Reset

RESET performs the same operations in both the 80C51BH and the C152 and those conditions that exist at the end of a valid RESET are:

Register	Contents	Register	Contents
ACC	00H	P0–P6	0FFH
ADR0-3	00H	PCON	0XXX0000B
AMSK0	00H	PRBS	00H
AMSK1	00H	PSW	00H
B	00H	RFIFO	INDETERMINATE
BAUD	00H	RSTAT	00000000B
BCRH0	INDETERMINATE	SARH0	INDETERMINATE
BCRH1	INDETERMINATE	SARH1	INDETERMINATE
BCRL0	INDETERMINATE	SARL0	INDETERMINATE
CRL1	INDETERMINATE	SARL1	INDETERMINATE
BKOFF	INDETERMINATE	SBUF	INDETERMINATE
DARH0	INDETERMINATE	SCON	00H
DARH1	INDETERMINATE	SLOTTM	00H
DARL0	INDETERMINATE	SP	07H
DARL1	INDETERMINATE	TCDCNT	INDETERMINATE
DCON0	00H	TCON	00H
DCON1	00H	TFIFO	INDETERMINATE
DPTR	0000H	TH0	00H
GMOD	X0000000B	TH1	00H
IE	0XX00000B	TL0	00H
IEN1	XX000000B	TL1	00H
IFS	00H	TMOD	00H
IP	XXX00000B	TSTAT	XX000100B
IPN1	XX000000B	PC	0000H
MYSLOT	00000000B		

The same conditions apply for both the 80C51BH and C152 for a correct reset pulse or "power-on" reset except that Reset is active low on the C152. Please refer to the 8051/52 Hardware Description Chapter of the Intel Embedded Controller Handbook for an explanation on how to provide a proper power-on reset. Since Reset is active low on the C152, the resistor should be tied to VCC and the capacitor should be tied to VSS.

Because the clocking on part of the GSC circuitry is independent of the processor clock, data may still be transmitted and DEN active for some time after reset is applied. The transmission may continue for a maximum of four machine cycles after reset is first pulled low. Although Reset has to be held low for only three machine cycles to be recognized by the GSC hardware, all of the GSC circuitry may not be reset until four machine cycles have passed. If it is important in the user application that all transmission and DEN becomes inactive at the end of a reset, then Reset will have to be held low for a minimum of four machine cycles.

2.4 Ports 4, 5 and 6

Ports 4, 5 and 6 operation is identical to Ports 1-3 on the 80C51BH. The description of port operation can be found in the 8051/52 Hardware Description Chapter of the Intel Embedded Controller Handbook. Ports 5 and 6 exist only on the "JB" and "JD" version of the C152 and can either function as standard I/O ports or can be configured so that program memory fetches are performed with these two ports. To configure ports 5 and 6 as standard I/O ports, EBEN is tied to a logic low. When in this configuration, ports 5 and 6 operation is identical to that of port 4 except they are not bit addressable. To configure ports 5 and 6 to fetch program memory, EBEN is tied to a logic high. When using ports 5 and 6 to fetch the program memory, the signal EPSEN is used to enable the external memory device instead of PSEN. Regardless of which ports are used to fetch program memory, all data memory fetches occur over ports 0 and 2. The 80C152JB and 80C152JD are available as ROMless devices only. ALE is still used to latch the address in all configurations. Table 2.1 summarizes the control signals and how the ports may be used.

2.5 Timer/Counters

The 80C51BH and C152 have the same pair of 16-bit general purpose timer/counters. The user should refer to the Intel Embedded Controller Handbook which describes the timer/counters and their use. The user should bear in mind, when reading the Intel Embedded Controller Handbook that the C152 does not have the third event timer named Timer 2, which is in the 8052.

2.6 Package

The 83C152 is packaged in a 48 pin DIP and a 68 lead PLCC. This differs from the 40 pin DIP and 44 pin PLCC of the 80C51BH. The larger package is required to accommodate the extra 8 bit I/O port (P4). Figures 2.5A, 2.5B and 2.5C show the packages and the pin names.

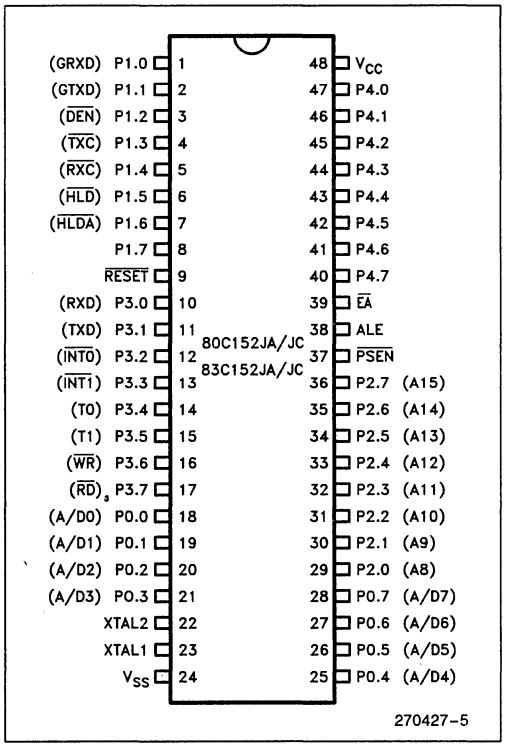


Figure 2.5A. DIP Pin Out

Table 2.1 Program Memory Fetches

EBEN	EA	Program Fetch via	PSEN	EPSEN	Comments
0	0	P0, P2	Active	Inactive	Addresses 0–0FFFFH
0	1	N/A	N/A	N/A	Invalid Combination
1	0	P5, P6	Inactive	Active	Addresses 0–0FFFFH
1	1	P5, P6 P0, P2	Inactive Active	Active Inactive	Addresses 0–1FFFH Addresses ≥ 2000H

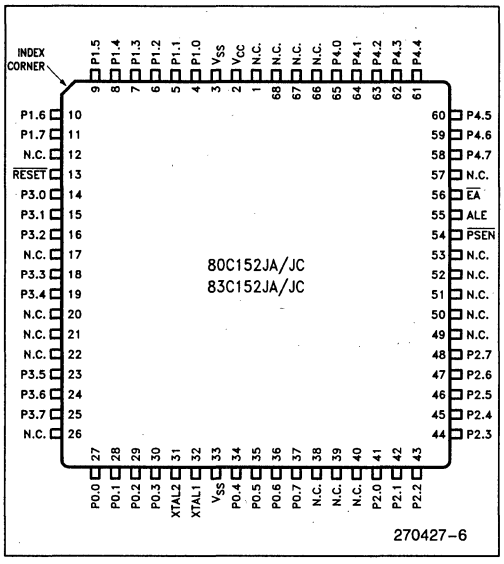


Figure 2.5B. PLCC Pin Out

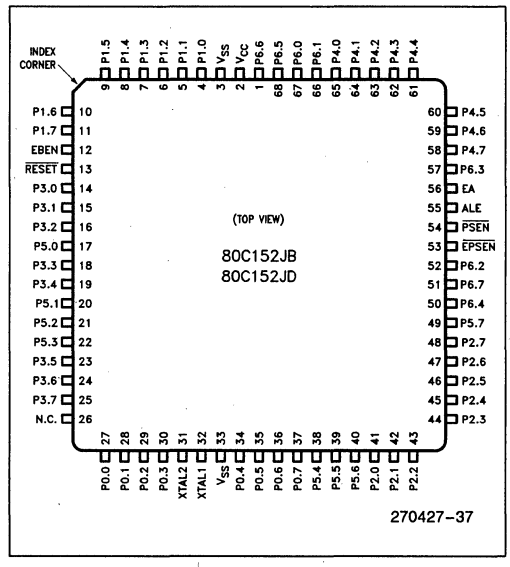


Figure 2.5C. PLCC Pin Out

2.7 Pin Description

The pin description for the 80C51BH also applies to the C152 and is listed below. Changes have been made to the descriptions as they apply to the C152.

PIN DESCRIPTION

Pin #		Description
DIP	PLCC(1)	
48	2	V_{CC}—Supply voltage.
24	3, 33(2)	**VSS**—Circuit ground.
18–21, 25–28	27–30, 34–37	**Port 0**—Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program memory if EBEN is pulled low. During accesses to external Data Memory, Port 0 always emits the low-order address byte and serves as the multiplexed data bus. In these applications it uses strong internal pullups when emitting 1s. Port 0 also outputs the code bytes during program verification. External pullups are required during program verification.

NOTES:
1. N.C. pins on PLCC package may be connected to internal die and should not be used in customer applications.
2. It is recommended that both Pin 3 and Pin 33 be grounded for PLCC devices.

PIN DESCRIPTION (Continued)

<table>
<tr><th colspan="2">Pin #</th><th rowspan="2">Description</th></tr>
<tr><th>DIP</th><th>PLCC(1)</th></tr>
<tr><td>1–8</td><td>4–11</td><td>Port 1—Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.
Port 1 also serves the functions of various special features of the 8XC152, as listed below:
<table>
<tr><th>Pin</th><th>Name</th><th>Alternate Function</th></tr>
<tr><td>P1.0</td><td>GRXD</td><td>GSC data input pin</td></tr>
<tr><td>P1.1</td><td>GTXD</td><td>GSC data output pin</td></tr>
<tr><td>P1.2</td><td>$\overline{\text{DEN}}$</td><td>GSC enable signal for an external driver</td></tr>
<tr><td>P1.3</td><td>$\overline{\text{TXC}}$</td><td>GSC input pin for external transmit clock</td></tr>
<tr><td>P1.4</td><td>$\overline{\text{RXC}}$</td><td>GSC input pin for external receive clock</td></tr>
<tr><td>P1.5</td><td>$\overline{\text{HLD}}$</td><td>DMA hold input/output</td></tr>
<tr><td>P1.6</td><td>$\overline{\text{HLDA}}$</td><td>DMA hold acknowledge input/output</td></tr>
</table></td></tr>
<tr><td>29–36</td><td>41–48</td><td>Port 2—Port 2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.
Port 2 emits the high-order address byte during fetches from external Program Memory if EBEN is pulled low. During accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR and DMA operations), Port 2 emits the high-order address byte. In these applications it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.
Port 2 also receives the high-order address bits during program verification.</td></tr>
<tr><td>10–17</td><td>14–16, 18, 19, 23–25</td><td>Port 3—Port 3 is an 8-bit bi-directional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.
Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:
<table>
<tr><th>Pin</th><th>Name</th><th>Alternate Function</th></tr>
<tr><td>P3.0</td><td>RXD</td><td>Serial input line</td></tr>
<tr><td>P3.1</td><td>TXD</td><td>Serial output line</td></tr>
<tr><td>P3.2</td><td>$\overline{\text{INT0}}$</td><td>External interrupt 0</td></tr>
<tr><td>P3.3</td><td>$\overline{\text{INT1}}$</td><td>External interrupt 1</td></tr>
<tr><td>P3.4</td><td>T0</td><td>Timer 0 external input</td></tr>
<tr><td>P3.5</td><td>T1</td><td>Timer 1 external input</td></tr>
<tr><td>P3.6</td><td>$\overline{\text{WR}}$</td><td>External Data Memory Write strobe</td></tr>
<tr><td>P3.7</td><td>$\overline{\text{RD}}$</td><td>External Data Memory Read strobe</td></tr>
</table></td></tr>
<tr><td>47–40</td><td>65–58</td><td>Port 4—Port 4 is an 8-bit bi-directional I/O port with internal pullups. Port 4 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 4 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. In addition, Port 4 also receives the low-order address bytes during program verification.</td></tr>
</table>

NOTES:
1. N.C. pins on PLCC package may be connected to internal die and should not be used in customer applications.
2. It is recommended that both Pin 3 and Pin 33 be grounded for PLCC devices.

PIN DESCRIPTION (Continued)

Pin #		Description
DIP	PLCC(1)	
9	13	**RST**—Reset input. A logic low on this pin for three machine cycles while the oscillator is running resets the device. An internal pullup resistor permits a power-on reset to be generated using only an external capacitor to V_{SS}. Although the GSC recognizes the reset after three machine cycles, data may continue to be transmitted for up to 4 machine cycles after Reset is first applied.
38	55	**ALE**—Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. While in Reset, ALE remains at a constant high level.
37	54	**PSEN**—Program Store Enable is the Read strobe to External Program Memory. When the 8XC152 is executing from external program memory, PSEN is active (low). When the device is executing code from External Program Memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to External Data Memory. While in Reset, PSEN remains at a constant high level.
39	56	**EA**—External Access enable. EA must be externally pulled low in order to enable the 8XC152 to fetch code from External Program Memory locations 0000H to 0FFFH. EA must be connected to V_{CC} for internal program execution.
23	32	**XTAL1**—Input to the inverting oscillator amplifier and input to the internal clock generating circuits.
22	31	**XTAL2**—Output from the oscillator amplifier.
N/A	17, 20 21, 22 38, 39 40, 49	**Port 5**—Port 5 is an 8-bit bi-directional I/O port with internal pullups. Port 5 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 5 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 5 is also the multiplexed low-order address and data bus during accesses to external program memory if EBEN is pulled high. In this application it uses strong pullups when emitting 1s.
N/A	67, 66 52, 57 50, 68 1, 51	**Port 6**—Port 6 is an 8-bit bi-directional I/O port with internal pullups. Port 6 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 6 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 6 emits the high-order address byte during fetches from external Program Memory if EBEN is pulled high. In this application it uses strong pullups when emitting 1s.
N/A	12	**EBEN**—E-Bus Enable input that designates whether program memory fetches take place via Ports 0 and 2 or Ports 5 and 6. Table 2.1 shows how the ports are used in conjunction with EBEN.
	53	**EPSEN**—E-bus Program Store Enable is the Read strobe to external program memory when EBEN is high. Table 2.1 shows when EPSEN is used relative to PSEN depending on the status of EBEN and EA.

NOTES:
1. N.C. pins on PLCC package may be connected to internal die and should not be used in customer applications.
2. It is recommended that both Pin 3 and Pin 33 be grounded for PLCC devices.

2.8 Power Down and Idle

Both of these operations function identically as in the 80C51BH. Application Note 252, "Designing with the 80C51BH" gives an excellent explanation on the use of the reduced power consumption modes. Some of the items not covered in AP-252 are the considerations that are applicable when using the GSC or DMA in conjunction with the power saving modes.

The GSC continues to operate in Idle as long as the interrupts are enabled. The interrupts need to be enabled, so that the CPU can service the FIFO's. In order to properly terminate a reception or transmission the C152 must not be in idle when the EOF is transmitted or received. After servicing the GSC, user software will need to again invoke the Idle command as the CPU does not automatically re-enter the Idle mode after servicing the interrupts.

The GSC does not operate while in Power Down so the steps required prior to entering Power Down become more complicated. The sequence when entering Power Down and the status of the I/O is of major importance in preventing damage to the C152 or other components in the system. Since the only way to exit Power Down is with a Reset, several problem areas become very significant. Some of the problems that merit careful consideration are cases where the Power Down occurs during the middle of a transmission, and the possibility that other stations are not or cannot enter this same mode. The state of the GSC I/O pins becomes critical and the GSC status will need to be saved before power down is entered. There will also need to be some method of identifying to the CPU that the following Reset is probably not a cold start and that other stations on the link may have already been initialized.

The DMA circuitry stops operation in both Idle and Power Down modes. Since operation is stopped in both modes, the process should be similar in each case. Specific steps that need to be taken include: notification to other devices that DMA operation is about to cease for a particular station or network, proper withdrawal from DMA operation, and saving the status of the DMA channels. Again, the status of the I/O pins during Power Down needs careful consideration to avoid damage to the C152 or other components.

Port 4 returns to its input state, which is high level using weak pullup devices.

2.9 Local Serial Channel

The Local Serial Channel (LSC) is the name given to the UART that exists on all MCS-51 devices. The LSC's function and operation is exactly the same as on the 80C51BH. For a description on the use of the LSC, refer to the 8051/52 Hardware Description Chapter in the Intel Embedded Controller Handbook, under Serial Interface.

3.0 GLOBAL SERIAL CHANNEL

3.1 Introduction

The Global Serial Channel (GSC) is a multi-protocol, high performance serial interface targeted for data rates up to 2 MBPS with on-chip clock recovery, and 2.4 MBPS using the external clock options. In applications using the serial channel, the GSC implements the Data Link Layer and Physical Link Layer as described in the ISO reference model for open systems interconnection.

The GSC is designed to meet the requirements of a wide range of serial communications applications and is optimized to implement Carrier-Sense Multi-Access with Collision Detection (CSMA/CD) and Synchronous Data Link Control (SDLC) protocols. The GSC architecture is also designed to provide flexibility in defining non-standard protocols. This provides the ability to retrofit new products into older serial technologies, as well as the development of proprietary interconnect schemes for serial backplane environments.

The versatility of the GSC is demonstrated by the wide range of choices available to the user. The various modes of operation are summarized in Table 3.1. In subsequent sections, each available choice of operation will be explained in detail.

In using Table 3.1, the parameters listed vertically (on the left hand side) represent an option that is selected (X). The parameters listed horizontally (along the top of the table) are all the parameters that could theoretically be selected (Y). The symbol at the junction of both X and Y determines the applicability of the option Y.

Note, that not all combinations are backwards compatible. For example, Manchester encoding requires half duplex, but half duplex does not require Manchester encoding.

Table 3.1

AVAILABLE OPTIONS → / SELECTED FUNCTION ↓	DATA ENCODING			FLAGS		CRC			DU-PLEX		ACKNOW-LEDGE			ADDRESS RECOG-NITION			BACKOFF			PRE-AMBLE	
N = NOT AVAILABLE M = MANDATORY O = OPTIONAL P = NORMALLY PREFERRED X = N/A	MANCHESTER	NRZ	NRZI	01111110	11/IDLE	NONE	16BITCCIT	32BITAUTO	HALF	FULL	NONE	HARDWARE	USERDEFINED	NONE/ALL	8BIT	16BIT	NORMAL	ALTERNATE	DETERMINISTIC	NONE	8BIT
DATA ENCODING:																					
MANCHESTER(CSMA/CD)	X	N	N	1	P	1	O	O	M	N	O	O	O	O	O	O	O	O	O	N	O
NRZI (SDLC)	N	X	N	P	1	1	O	O	O	O	O	N	P	O	O	O	N	N	N	O	O
NRZ (EXT CLK)	N	N	X	O	O	1	O	O	O	O	O	N	O	O	O	O	O	O	O	O	O
FLAGS:01111110 (SDLC)	N	P	O	X	1	1	O	O	O	O	O	N	P	O	O	O	N	N	N	O	O
11/IDLE	P	N	O	1	X	1	O	O	O	N	O	O	O	O	O	O	O	O	O	1	O
CRC:NONE	1	1	1	1	1	X	N	N	1	N	1	1	1	1	1	1	N	N	N	1	1
16-BIT CCITT	O	O	O	O	O	N	X	N	O	O	O	O	O	O	O	O	O	O	O	O	O
32-BIT AUTODIN II	O	O	O	O	O	N	N	X	O	N	O	O	O	O	O	O	O	O	O	O	O
DUPLEX:HALF	O	O	O	O	O	1	O	O	X	N	O	O	O	O	O	O	O	O	O	O	O
FULL	N	O	O	M	N	N	M	N	N	X	O	N	P	O	O	O	N	N	N	O	O
ACKNOWLEDGEMENT:NONE	O	O	O	O	O	1	O	O	O	O	X	N	N	O	O	O	O	O	O	O	O
HARDWARE	O	N	N	N	O	1	O	O	O	N	N	X	N	O	O	O	N	O	O	N	O
USER DEFINED	O	P	O	O	O	1	O	O	O	P	N	N	X	O	O	O	O	O	O	O	O
ADDRESS RECOGNITION:																					
NONE/ALL	O	O	O	O	O	1	O	O	O	O	O	O	O	X	N	N	O	O	O	O	O
8-BIT	O	O	O	O	O	1	O	O	O	O	O	O	O	N	X	N	O	O	O	O	O
16-BIT	O	O	O	O	O	1	O	O	O	O	O	O	O	N	N	X	O	O	O	O	O
COLLISION RESOLUTION:																					
NORMAL	O	N	O	N	O	N	O	O	M	N	O	N	O	O	O	O	X	N	N	N	O
ALTERNATE	O	N	O	N	O	N	O	O	M	N	O	O	O	O	O	O	N	X	N	N	O
DETERMINISTIC	O	N	O	N	O	N	O	O	M	N	O	O	O	O	O	O	N	N	X	N	O
PREAMBLE:NONE	N	O	O	O	1	1	O	O	O	O	O	N	O	O	O	O	N	N	N	X	N
8-BIT	O	O	O	O	O	1	O	O	O	O	O	O	O	O	O	O	O	O	O	N	X
32-BIT	O	O	O	O	O	1	O	O	O	O	O	O	O	O	O	O	O	O	O	N	N
64-BIT	O	O	O	O	O	1	O	O	O	O	O	O	O	O	O	O	O	O	O	N	N
JAM:D.C.	M	N	N	N	O	N	O	O	M	N	O	O	O	O	O	O	O	O	O	N	O
$\overline{\text{CRC}}$	M	N	N	N	O	N	O	O	M	N	O	O	O	O	O	O	O	O	O	N	O
CLOCKING:EXTERNAL	N	M	N	O	O	N	O	O	O	O	O	N	O	O	O	O	N	N	N	O	O
INTERNAL	O	O	N	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
CONTROL: CPU	O	O	O	O	O	1	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
DMA	O	O	O	O	O	1	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
RAW RECEIVE:	1	1	1	1	1	1	1	1	1	N	1	1	1	1	1	1	O	O	O	1	1
RAW TRANSMIT:	1	1	1	1	1	1	1	1	1	N	1	1	1	1	1	1	N	N	N	1	1
CSMA/CD:	O	N	N	1	P	1	O	O	M	N	O	O	O	O	O	O	O	O	O	N	O
SDLC:	N	O	O	P	1	1	O	O	O	O	O	N	O	O	O	O	N	N	N	P	O

Table 3.1 (Continued)

AVAILABLE OPTIONS → / N=NOT AVAILABLE M=MANDATORY O=OPTIONAL P=NORMALLY PREFERRED X=N/A / SELECTED ↓ FUNCTION	PRE-AMBLE		JAM		CLOCK		CONTROL					
	32 BIT	64 BIT	DC	CRC/	EXTERNAL	INTERNAL	CPU	DMA	RAW RECEIVE	RAW TRANSMIT	CSMA/CD	SDLC
DATA ENCODING:												
MANCHESTER	O	O	O	O	N	M	O	O	O	O	M	N
NRZI	O	O	N	N	N	M	O	O	O	O	N	M
NRZ	O	O	O	O	M	N	O	O	O	O	O	O
FLAGS:01111110	O	O	N	N	O	O	O	O	O	1	1	P
11/IDLE	O	O	O	O	O	O	O	O	O	1	P	1
CRC:NONE	1	1	N	N	1	1	1	1	1	1	1	1
16-BIT CCITT	O	O	O	O	O	O	O	O	1	1	O	O
32-BIT AUTODIN II	O	O	O	O	O	O	O	O	1	1	O	O
DUPLEX:HALF	O	O	O	O	O	O	O	O	O	O	O	O
FULL	O	O	N	N	O	O	O	O	N	N	N	P
ACKNOWLEDGEMENT:NONE	O	O	O	O	O	O	O	O	O	O	O	O
HARDWARE	O	O	O	O	N	O	O	O	N	N	O	N
USER DEFINED	O	O	O	O	O	O	O	O	O	O	O	1
ADDRESS RECOGNITION:												
NONE	O	O	O	O	O	O	O	O	O	O	O	O
8-BIT	O	O	O	O	O	O	O	O	1	1	O	O
16-BIT	O	O	O	O	O	O	O	O	1	1	O	O
COLLISION RESOLUTION:												
NORMAL	O	O	O	O	N	O	O	O	O	N	M	N
ALTERNATE	O	O	O	O	N	O	O	O	O	N	M	N
DETERMINISTIC	O	O	O	O	N	O	O	O	O	N	M	N
PREAMBLE:NONE	N	N	N	N	O	O	O	O	O	O	N	P
8-BIT	N	N	O	O	O	O	O	O	1	1	O	O
32-BIT	X	N	O	O	O	O	O	O	1	1	O	O
64-BIT	N	X	O	O	O	O	O	O	1	1	O	O
JAM:D.C.	O	O	X	N	N	O	O	O	O	N	M	N
$\overline{CRC}$	O	O	N	X	N	O	O	O	O	N	M	N
CLOCKING:EXTERNAL	O	O	N	N	X	N	O	O	O	O	N	O
INTERNAL	O	O	O	O	N	X	O	O	O	O	O	O
CONTROL:CPU	O	O	O	O	O	O	X	N	O	O	O	O
DMA	O	O	O	O	O	O	N	X	O	O	O	O
RAW RECEIVE:	1	1	O	O	1	1	1	1	X	N	1	1
RAW TRANSMIT:	1	1	N	N	1	1	1	1	N	X	1	1
CSMA/CD:	O	O	O	O	N	O	O	O	O	O	X	N
SDLC:	O	O	N	N	O	O	O	O	O	O	N	X

Note 1: Programmable in Raw transmit or receive mode.

Almost all the options available from Table 3.1 can be implemented with the proper software to perform the functions that are necessary for the options selected. In Table 3.1, a judgment has been made by the authors on which options are practical and which are not. What this means is that in Table 3.1, an "N" should be interpreted as meaning that the option is either not practical when implemented with user software or that it cannot be done. An "O" is used when that function is one of several that can be implemented with the GSC without additional user software.

The GSC is targeted to operate at bit rates up to 2.4 MBps using the external clock options and up to 2 MBps using the internal baud rate generator, internal data formatting and on-chip clock recovery. The baud rate generator allows most standard rates to be achieved. These standards include the proposed IEEE802.3 LAN standard (1.0MBps) and the T1 standard (1.544MBps). The baud rate is derived from the crystal frequency. This makes crystal selection important when determining the frequency and accuracy of the baud rate.

The user needs to be aware that after reset, the GSC is in CSMA/CD mode, IFS = 256 bit times, and a bit time equals 8 oscillator periods. The GSC will remain in this mode until the interframe space expires. If the user changes to SDLC mode or the parameters used in CSMA/CD, these changes will not take effect until the interframe space expires. A requirement for the interframe space timer to begin is that the receiver be in an idle state. This makes it possible for the GSC to be in some other mode than the user intends for a significant amount of time after reset. To prevent unwanted GSC errors from occurring, the user should not enable the GSC or the GSC interrupts for 170 machine cycles ((256 × 8)/12) after LNI bit is set.

3.2 CSMA/CD Operation

3.2.1 CSMA/CD OVERVIEW

CSMA/CD operates by sensing the transmission line for a carrier, which indicates link activity. At the end of link activity, a station must wait a period of time, called the deference period, before transmission may begin. The deference period is also known as the interframe space. The interframe space is explained in Section 3.2.3.

With this type of operation, there is always the possibility of a collision occurring after the deference period due to line delays. If a collision is detected after transmission is started, a jamming mechanism is used to ensure that all stations monitoring the line are aware of the collision. A resolution algorithm is then executed to resolve the contention. There are three different modes of collision resolution made available to the user on the C152. Re-transmission is attempted when a resolution algorithm indicates that a station's opportunity has arrived.

Normally, in CSMA/CD, re-transmission slot assignments are intended to be random. This method gives all stations an equal opportunity to utilize the serial communication link but also leaves the possibility of another collision due to two stations having the same slot assignment. There is an option on the C152 which allows all the stations to have their slot assignments previously determined by user software. This pre-assignment of slots is called the deterministic resolution mode. This method allows resolution after the first collision and ensures the access of the link to each station during the resolution. Deterministic resolution can be advantageous when the link is being heavily used and collisions are frequently occurring and in real time applications where determinism is required. Deterministic resolution may also be desirable if it is known beforehand that a certain station's communication needs to be prioritized over those of other stations if it is involved in a collision.

3.2.2 CSMA/CD FRAME FORMAT

The frame format in CSMA/CD consists of a preamble, Beginning of Frame flag (BOF), address field, information field, CRC, and End of Frame flag (EOF) as shown in Figure 3.1.

Figure 3.1 Typical CSMA/CD Frame

PREAMBLE - The preamble is a series of alternating 1s and 0s. The length of the preamble is programmable to be 0, 8, 32, or 64 bits. The purpose of the preamble is to allow all the receivers to synchronize to the same clock edges and identifies to the other stations on-line that there is activity indicating the link is being used. For these reasons zero preamble length is not compatible with standard CSMA/CD, protocols. When using CSMA/CD, the BOF is considered part of the preamble compared to SDLC, where the BOF is not part of the preamble. This means that if zero preamble length were to be used in CSMA/CD mode, no BOF would be generated. It is strongly recommended that zero preamble length never be used in CSMA/CD mode. If the preamble contains two consecutive 0s, the preamble is considered invalid. If the C152 detects an invalid preamble, the frame is ignored.

BOF - In CSMA/CD the Beginning-Of-Frame is a part of the preamble and consists of two sequential 1s. The purpose of the BOF is to identify the end of the preamble and indicate to the receiver(s) that the address will immediately follow.

ADDRESS - The address field is used to identify which messages are intended for which stations. The user must assign addresses to each destination and source. How the addresses are assigned, how they are maintained, and how each transmitter is made aware of which addresses are available is an issue that is left to the user. Some suggestions are discussed in Section 3.5.5. Generally, each address is unique to each station but there are special cases where this is not true. In these special cases, a message is intended for more than one station. These multi-targeted messages are called broadcast or multicast-group addresses. A broadcast address consisting of all 1s will always be received by all stations. A multicast-group address usually is indicated by using a 1as the first address bit. The user can choose to mask off all or selective bits of the address so that the GSC receives all messages or multicast-group messages. The address length is programmable to be 8 or 16 bits. An address consisting of all 1s will always be received by the GSC on the C152. The address bits are always passed from the GSC to the CPU. With user software, the address can be extended beyond 16 bits, but the automatic address recognition will only work on a maximum of 16 bits. User software will have to resolve any remaining address bits.

INFO - This is the information field and contains the data that one device on the link wishes to transmit to another device. It can be of any length the user wishes but needs to be in multiples of 8 bits. This is because multiples of 8 bits are used to transfer data into or out of the GSC FIFOs. The information field is delineated from the rest of the components of the frame by the preceding address field and the following CRC. The receiver determines the position of the end of the information field by passing the bytes through a temporary storage space. When the EOF is received the bytes in temporary storage are the CRC, and the last bit received previous to the CRC constitute the end of the information field.

CRC - The Cyclic Redundancy Check (CRC) is an error checking algorithm commonly used in serial communications. The C152 offers two types of CRC algorithms, a 16-bit and a 32-bit. The 16-bit algorithm is normally used in the SDLC mode and will be described in the SDLC section. In CSMA/CD applications either algorithm can be used but IEEE 802.3 uses a 32-bit CRC. The generation polynomial the C152 uses with the 32-bit CRC is:

$$G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

The CRC generator, as shown in Figure 3.2, operates by taking each bit as it is received and XOR'ing it with bit 31 of the current CRC. This result is then placed in temporary storage. The result of XOR'ing bit 31 with the received bit is then XOR'd with bits 0, 1, 3, 4, 6, 7, 9, 10, 11, 15, 21, 22, 25 as the CRC is shifted right one position. When the CRC is shifted right, the temporary storage space holding the result of XOR'ing bit 31 and the incoming bit is shifted into position 0. The whole process is then repeated with the next incoming or outgoing bit.

The user has no access to the CRC generator or the bits which constitute the CRC while in CSMA/CD. On transmission, the CRC is automatically appended to the data being sent, and on reception, the CRC bits are not normally loaded into the receive FIFO. Instead, they are automatically stripped. The only indication the user has for the status of the CRC is a pass/fail flag. The pass/fail flag only operates during reception. A CRC is considered as passing when the the CRC generator has 11000111 00000100 11011010 01111011B as a remainder after all of the data, including the CRC checksum, from the transmitting station has been cycled through the CRC generator. The preamble, BOF and EOF are not included as part of the CRC algorithm. An interrupt is available that will interrupt the CPU if the CRC of the receiver is invalid. The user can enable the CRC to be passed to the CPU by placing the receiver in the raw receive mode.

This method of calculating the CRC is compatible with IEEE 802.3.

EOF - The End Of Frame indicates when the transmission is completed. The end flag in CSMA/CD consists of an idle condition. An idle condition is assumed when there is no transitions and the link remains high for 2 or more bit times.

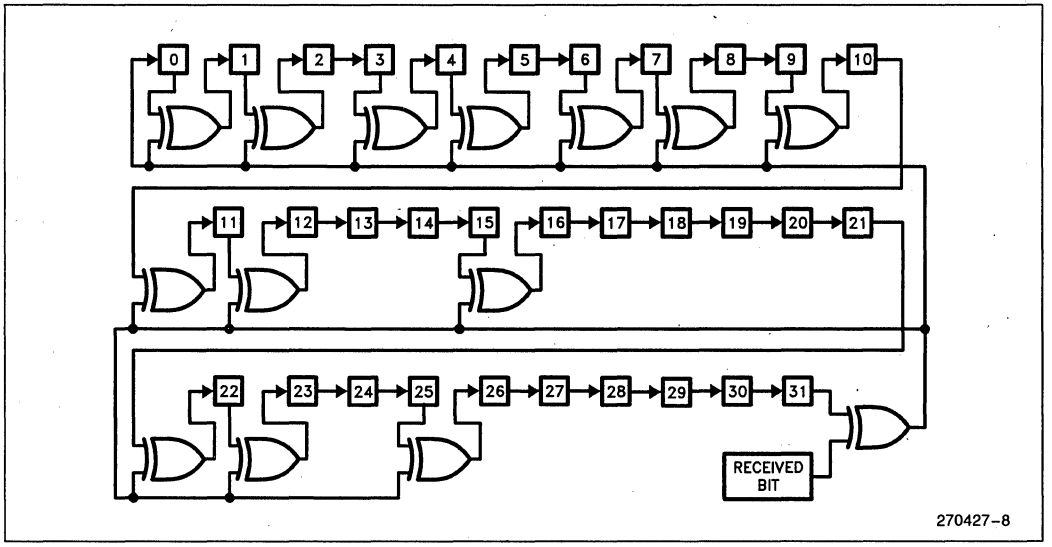


Figure 3.2. CRC Generator

3.2.3 INTERFRAME SPACE

The interframe space is the amount of time that transmission is delayed after the link is sensed as being idle and is used to separate transmitted frames. In alternate backoff mode, the interframe space may also be included in the determination of when retransmissions may actually begin. The C152 allows programmable interframe spaces of even numbers of bit times from 2 to 256. The hardware enforces the interframe space in SDLC mode as well as in CSMA/CD mode.

The period of the interframe space is determined by the contents of IFS. IFS is an SFR that is programmable from 0 to 254. The interframe space is measured in bit times. The value in IFS multiplied by the bit time equals the interframe space unless IFS equals 0. If IFS does equal 0, then the interframe space will equal 256 bit times. One of the considerations when loading the IFS is that only even numbers (LSB must be 0) can be used because only the 7 most significant bits are loaded into IFS. The LSB is controlled by the GSC and determines which half of the IFS is currently being used. In some modes, the interframe space timer is re-triggered if activity is detected during the first half of the period. The GSC determines which half of the interframe space is currently being used by examining the LSB. A one indicates the first half and zero indicates the second half of the IFS.

After reset IFS is 0, which delays the first transmission for both SDLC and CSMA/CD by 256 bit times (after reset, a bit time equals 8 oscillator clock periods).

In most applications, the period of the interframe space will be equal to or greater than the amount of time needed to turn-around the received frame. The turn-around period is the amount of time that is needed by user software to complete the handling of a received frame and be prepared to receive the next frame. An interframe space smaller than the required turn-around period could be used, but would allow some frames to be missed.

When a GSC transmitter has a new message to send, it will first sense the link. If activity is detected, transmission will be deferred to allow the frame in progress to complete. When link activity ceases, the station continues deferring for one interframe space period.

As mentioned earlier, the interframe space is used during the collision resolution period as well as during normal transmission. The backoff method selected affects how the deference period is handled during normal transmission. If normal backoff mode is selected, the interframe space timer is reset if activity occurs during approximately the first half of the interframe space. If alternate backoff or deterministic backoff is selected, the timer is not reset. In all cases when the interframe space timer expires, transmission may begin, regardless if there is activity on the link or not. Although the C152 resets the interframe space timer if activity is detected during the first one-half of the interframe space, this is not necessarily true of all CSMA/CD systems. (IEEE 802.3 recommends that the interframe space be reset if activity is detected during the first two-thirds or less of the interframe space.)

3.2.4 CSMA/CD DATA ENCODING

Manchester encoding/decoding is automatically selected when the user software selects CSMA/CD transmission mode (See Figure 3.3). In Manchester encoding the value of the bit is determined by the transition in the middle of the bit time, a positive transition is decoded as a 1 and a negative transition is decoded as a 0. The Address and Info bytes are transmitted LSB first. The CRC is transmitted MSB first.

If the external 1X clock feature is chosen the transmission mode is always NRZ (see Section 3.5.11). Using CSMA/CD with the external clock option is not supported because the data needs reformatting from NRZ to Manchester for the receiver to be able to detect code violations and collisions.

3.2.5 COLLISION DETECTION

The GSC hardware detects collisions by detecting Manchester waveform violations at its GRXD pin. Three kinds of waveform violations are detected: a missing 0-to-1 transition where one was expected, a 1-to-0 transition where none was expected, and a waveform that stays low (or high) for too short a time.

Jitter Tolerance

A valid Manchester waveform must have a transition at the midpoint of any bit cell, and may have a transition at the edge of any bit cell. Therefore, transitions will nominally be separated by either 1/2 bit-time or 1 bit-time.

The GSC samples the GRXD pin at the rate of 8 x the bit rate. The sequence of samples for the received bit sequence 001 would nominally be:

```
samples:11110000:11110000:00001111:
bit value:     0    :    0    :    1    :
      :<-bit cell->:<-bit cell->:<-bit cell->:
```

The sampling system allows a jitter tolerance of ±1 sample for transitions that are 1/2 bit-time apart, and ±2 samples for transitions that are 1 bit-time apart.

Narrow Pulses

A valid Manchester waveform must stay high or low for at least a half bit-time, nominally 4 sample-times. Jitter tolerance allows a waveform which stays high or low for 3 sample-times to also be considered valid. A sample sequence which shows a second transition only 1 or 2 sample-times after the previous transition is considered to be the result of a collision. Thus, sample sequences such as 0000110000 and 111101111 are interpreted as collisions.

The GSC hardware recognizes the collision to have occurred within 3/8 to 1/2 bit-time following the second transition.

Missing 0-to-1 Transition

A 0-to-1 transition is expected to occur at the center of any bit cell that begins with 0. If the previous 1-to-0 transition occurred at the bit cell edge, a jitter tolerance of ±1 sample is allowed. Sample sequences such as 1111:00001111 and 1111:000001111 are valid, where ":" indicates a bit cell edge. Sequences of the form 1111:000000XXX are interpreted as collisions.

For these kinds of sequences, the GSC recognizes the collision to have occurred within 1 to 1 1/8 bit-times after the previous 1-to-0 transition.

If the previous 1-to-0 transition occurred at the center of the previous bit cell, a jitter tolerance of ±2 samples is allowed. Thus, sample sequences such as 11110000:00001111 and 111100000:000001111 are valid. Sequences of the form 111100000:000000XXX are interpreted as collisions.

For these kinds of sequences, the GSC recognizes the collision to have occurred within 1 5/8 to 1 3/4 bit-times after the previous 1-to-0 transition.

Unexpected 1-to-0 Transition

If the line is at a logic 1 during the first half of a bit cell, then it is expected to make a 1-to-0 transition at the midpoint of the bit cell. If the transition is missed, it is assumed that this bit cell is the first half of an EOF flag

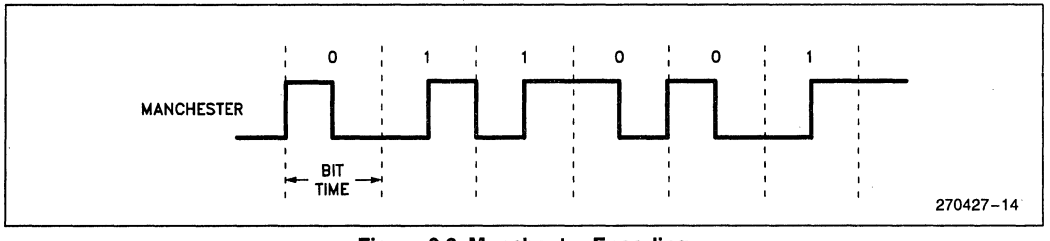


Figure 3.3. Manchester Encoding

(line idle for two bit-times). One bit-time later (which marks the midpoint of the next bit cell), if there is still no 1-to-0 transition, a valid EOF is assumed and the line idle bit (LNI in TSTAT) gets set.

However, if the assumed EOF flag is interrupted by a 1-to-0 transition in the bit-time following the first missing transition, a collision is assumed. In that case the GSC hardware recognizes the collision to have occurred within 1/2 to 5/8 bit-time after the unexpected transition.

3.2.6 RESOLUTION OF COLLISIONS

How the GSC responds to a detected collision depends on what it was doing at the time the collision was detected. What it might be doing is either transmitting or receiving a frame, or it might be inactive.

GSC Inactive

The collision is detected whether the GSC is active or not. If the GSC is neither transmitting nor receiving at the time the collision is detected, it takes no action unless user software has selected the Deterministic Collision Resolution (DCR) algorithm. If DCR has been selected, the GSC will participate in the resolution algorithm.

GSC Receiving

If the GSC is already in the process of receiving a frame at the time the collision is detected, its response depends on whether the first byte of the frame has been transferred into RFIFO yet or not. If that hasn't occurred, the GSC simply aborts the reception, but takes no other action unless DCR has been selected. If DCR has been selected, the GSC participates in the resolution algorithm.

If the reception has already progressed to the point where a byte has been transferred to RFIFO by the time the collision is detected, the receiver is disabled (GREN = 0), and the Receive Error Interrupt flag RCABT is set. If DCR has been selected, the GSC participates in the resolution algorithm.

Incoming bits take 1/2 bit time to get from the GRXD pin to the bit decoder. The bit decoder strips off the preamble/BOF bits, and the first bit after BOF is shifted into a serial strip buffer. The length of the strip buffer is equal to the number of bits in the selected CRC. It is within this buffer that address recognition takes place. If the address is recognized as one for which reception should proceed, then when the first address bit exits the strip buffer it is shifted into an 8-bit shift register. When the shift register is full, its content is transferred to RFIFO. That is the event that determines whether a collision sets RCABT or not.

GSC Transmitting

If the GSC is in the process of transmitting a frame at the time the collision is detected, it will in every case execute its jam/backoff procedure. Its reponse beyond that depends on whether the first byte of the frame has been transferred from TFIFO to the output shift register yet or not. That transfer takes place at the beginning of the first bit of the BOF; that is, 2 bit-times before the end of the preamble/BOF sequence.

If the transfer from TFIFO hasn't occurred yet, the GSC hardware will try again to gain access to the line after its backoff time has expired. Up to 8 automatic restarts can be attempted. If the 8th restart is interrupted by yet another collision, the transmitter is disabled (TEN = 0) and the Transmit Error Interrupt flag TCDT is set.

If the transfer from TFIFO occurs before a collision is detected, the transmitter is disabled (TEN = 0) and the TCDT flag is set.

The response of the GSC to detected collisions is summarized in Figure 3.4.

What the GSC was doing	Response
nothing	None, unless DCR = 1. If DCR = 1, begin DCR countdown.
Receiving a Frame, first byte not in RFIFO yet.	None, unless DCR = 1. If DCR = 1, begin DCR countdown.
Receiving a Frame, first byte already in RFIFO.	Set RCABT, clear GREN. If DCR = 1, begin DCR countdown.
Transmitting a Frame, first byte still in TFIFO	Execute jam/backoff. Restart if collision count ≤8.
Transmitting a Frame, first byte already taken from TFIFO	Execute jam/backoff. Set TCDT, clear TEN.

Figure 3-4. Response to a Detected Collision. References to DCR and the DCR Countdown Have to Do with the Deterministic Collision Resolution Algorithm.

Jam

The jam signal is generated by any 8XC152 that is involved in transmitting a frame at the time a collision is detected at its GRXD pin. This is to ensure that if one transmitting station detects a collision, all the other stations on the network will also detect a collision.

If a transmitting 8XC152 detects a collision during the preamble/BOF part of the frame that it is trying to transmit, it will complete the preamble/BOF and then begin the jam signal in the first bit time after BOF. If the collision is detected later in the frame, the jam signal will begin in the next bit time after the collision was detected.

The jam signal lasts for the same number of bit times as the selected CRC length—either 16- or 32-bit times.

The 8XC152 provides two types of jam signals that can be selected by user software. If the node is DC-coupled to the network, the DC jam can be selected. In this case the GTXD pin is pulled to a logic 0 for the duration of the jam. If the node is AC-coupled to the network, then AC jam must be selected. In this case the GSC takes the CRC it has calculated thus far in the transmission, inverts each bit, and transmits the inverted CRC. The selection of DC or AC jam is made by setting or clearing the DCJ bit, which resides in the SFR named MYSLOT.

When the jam signal is completed, the 8XC152 goes into an idle state. Presumeably, other stations on the network are also generating their own jam signals, after which they too go into an idle state. When the 8XC152 detects the idle state at its own GRXD pin, the backoff sequence begins.

Backoff

There are three software selectable collision resolution algorithms in the 8XC152. The selection is made by writing values to 3 bits:

DCR	M1	M0	Algorithm
0	0	0	Normal Random
0	1	1	Alternate Random
1	1	1	Deterministic

M1 and M0 reside in GMOD, and DCR is in MYSLOT.

In the Normal Random algorithm, the GSC backs off for a random number of slot times and then decides whether to restart the transmission. The backoff time begins as soon as a line idle condition is detected.

The Alternate Random algorithm is the same as the Normal Random except the backoff time doesn't start until an IFS has transpired.

In the Deterministic algorithm, the GSC backs off to await its pre-determined turn.

Random Backoff

In either of the random algorithms, the first thing that happens after a collision is detected is that a 1 gets shifted into the TCDCNT (Transmit Collision Detect Count) register, from the right.

Thus if the software cleared TCDCNT before telling the GSC to transmit, then TCDCNT keeps track of how many times the transmission had to be aborted because of collisions:

TCDCNT =	00000000	first attempt
	00000001	first collision
	00000011	second collision
	00000111	third collision
	00001111	fourth collision
	. . . . .	
	11111111	eighth collision

After TCDCNT gets a 1 shifted into it, the logical AND of TCDCNT and PRBS is loaded into a countdown timer named BKOFF. PRBS is the name of an SFR which contains the output of a pseudo-random binary sequence generator. Its function is to provide a random number for use in the backoff algorithm.

Thus on the first collision BKOFF gets loaded randomly with either 00000000 or 00000001. If there is a second collision it gets loaded with the random selection of 00000000, 00000001, 00000010, or 00000011. On the third collision there will be a random selection among 8 possible numbers. On the fourth, among 16, etc. Figure 3.5 shows the logical arrangement of PRBS, TCDCNT, and BKOFF.

BKOFF starts counting down from its preload value, counting slot times. At any time, the current value in BKOFF can be read by the CPU, but CPU writes to BKOFF have no effect. While BKOFF is counting down, if its current value is not 0, transmission is disabled. The output signal "BKOFF = 0" is asserted when BKOFF reaches 0, and is used to re-enable transmission.

At that time transmission can proceed, subject of course to IFS enforcement, unless:

- shifting a 1 into TCDCNT from the right caused a 1 to shift out from the MSB of TCDCNT, or
- the collision was detected after TFIFO had been accessed by the transmit hardware.

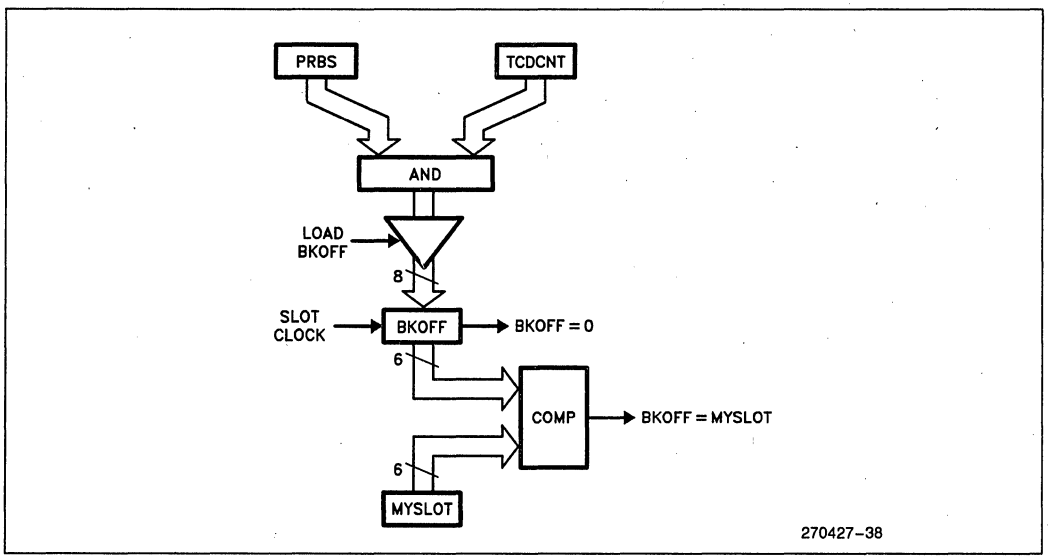


Figure 3.5. Backoff Timer Logic

In either of these cases, the transmitter is disabled (TEN = 0) and the Transmit Error flag TCDT is set. The automatic restart is canceled.

Where the Normal and Alternate Random backoff algorithms differ is that in Normal Random backoff the BKOFF timer starts counting down as soon as a line idle condition is detected, whereas in Alternate Random backoff the BKOFF timer doesn't start counting down till the IFS expires.

The Alternate Random mode was designed for networks in which the slot time is less than the IFS. If the randomly assigned backoff time for a given transmitter happens to be 0, then it is free to transmit as soon as the IFS ends. If the slot time is shorter than the IFS, Normal Random mode would nearly guarantee that if there's a first collision there will be a second collision. The situation is avoided in Alternate Random mode, since the BKOFF countdown doesn't start till the IFS is over.

The unit of count to the BKOFF timer is the slot time. The slot time is measured in bit-times, and is determined by a CPU write to the register SLOTTM. The slot time clock is a 1-byte downcounter which starts its countdown from the value written to SLOTTM. It is decremented each bit time when a backoff is in progress, and when it gets to 1 it generates one tick in the slot time clock. The next state after 1 is the reload value which was written to SLOTTM. If 0 is the value written to SLOTTM, the slot time clock will equal 256 bit times.

A CPU write to SLOTTM accesses the reload register. A CPU read of SLOTTM accesses the downcounter. In most protocols, the slot period must be equal to or greater than the longest round trip propagation time plus the jam time.

Deterministic Backoff

In the Deterministic backoff mode, the GSC is assigned (in software) a slot number. The slot assignment is written to the low 6 bits of the register MYSLOT. This same register also contains, in the 2 high bit positions, the control bits DCJ and DCR.

Slot assignments therefore can run from 0 to 63. It will turn out that the higher the slot assignment, the sooner the GSC will get to restart its transmission in the event of a collision.

The highest slot assignment in the network is written by each station's software into its TCDCNT register. Normally the highest slot assignment is just the total number of stations that are going to participate in the backoff algorithm.

In deterministic backoff mode a collision will not cause a 1 to be shifted into TCDCNT. TCDCNT will still be ANDed with PRBS and the result loaded into BKOFF. In order to insure that all stations have the same value loaded into BKOFF, which determines the first slot number to occur, the PRBS should be loaded with 0FFH; the PRBS will maintain this value until either the 8XC152 is reset or the user writes some other value into PRBS. After BKOFF is loaded it begins counting down slot times as soon as the IFS ends. Slot times are defined by the user, the same way as before, by loading SLOTTM with the number of bit times per slot.

When BKOFF equals the slot assignment (as defined in MYSLOT), the signal "BKOFF = MYSLOT" in Figure 3.5 is asserted for one slot time, during which the GSC can restart its transmission.

While BKOFF is counting down, if any activity is detected at the GRXD pin, the countdown is frozen until the activity ends, a line idle condition is detected, and an IFS transpires. Then the countdown resumes from where it left off.

If a collision is detected at the GRXD pin while BKOFF is counting down, the collision resolution algorithm is restarted from the beginning.

In effect, the GSC "owns" its assigned slot number, but with one exception. Nobody owns slot number 0. Therefore if the GSC is assigned slot number 0, then when BKOFF = 0, this station and any other station that has something to say at this time will have an equal chance to take the line.

3.2.7 HARDWARE BASED ACKNOWLEDGE

Hardware Based Acknowledge (HBA) is a data link packet acknowledging scheme that the user software can enable with CSMA/CD protocol. It is not an option with SDLC protocol however.

In general HBA can give improved system response time and increased effective transmission rates over acknowledge schemes implemented in higher layers of the network architecture. Another benefit is the possibility of early release of the transmit buffer as soon as the acknowledge is received.

The acknowledge consists of a preamble followed by an idle condition. A receiving station with HABEN enabled will send an acknowledge only if the incoming address is unique to the receiving station and if the frame is determined to be correct with no errors. For the acknowledge to be sent, TEN must be set. For the transmitting station to recognize the acknowledge GREN must be set. A zero as the LSB of the address indicates that the address is unique and not a group or broadcast address. Errors can be caused by collisions, incorrect CRC, misalignment, or FIFO overflow. The receiver sends the acknowledge as soon as the line is sensed to be idle. The user must program the interframe space and the preamble length such that the acknowledge is completed before IFS expires. This is normally done by programming IFS larger than the preamble.

A transmitting station with HABEN enabled expects an acknowledge. It must receive one prior to the end of the interframe space, or else an error is assumed and the NOACK bit is set. Setting of the TDN bit is also delayed until the end of the interframe space. Collisions detected during the interframe space will also cause NOACK to be set.

If the user software has enabled DMA servicing of the GSC, an interrupt is generated when TDN is set. TDN will be set at the end of the interframe space if a hardware based acknowledge is required and received. If the GSC is serviced by the CPU, the user must time out the interframe space and then check TDN before disabling the transmitter or transmit error interrupts. NOACK will generate a transmit error interrupt if the transmitter and interrupts are enabled during the interframe space.

3.3 SDLC Operation

3.3.1 SDLC OVERVIEW

SDLC is a communication protocol developed by IBM and widely used in industry. It is based on a primary/secondary architecture and requires that each secondary station have a unique address. The secondary stations can only communicate to the primary station, and then, only when the primary station allows communication to take place. This eliminates the possibility of contention on the serial line caused by the secondary station's trying to transmit simultaneously.

In the C152, SDLC can be configured to work in either full or half duplex. When adhering to strict SDLC protocol, full duplex is required. Full duplex is selected whenever a 16-bit CRC is selected. At the end of a valid reset the 16-bit CRC is selected. To select half duplex with a 16-bit CRC, the receiver must be turned off by user software before transmission. The receiver is turned off by clearing the GREN bit (RSTAT.1). The receiver needs to be turned off because the address that is transmitted is the address of the secondary station's receiver. If not turned off, the receiver could mistake the outgoing message as being intended for itself. When 32-bit CRCs are used, half duplex is the only method available for transmission.

3.3.2 SDLC Frame Format

The format of an SDLC frame is shown in Figure 3.6. The frame consists of a Beginning of Frame flag, Address field, Control Field, Information field (optional), a CRC, and the End of Frame flag.

Figure 3.6. Typical SDLC Frame

BOF - The begin of frame flag for SDLC is 01111110. It is only one of two possible combinations that have six consecutive ones in SDLC. The other possibility is an abort character which consists of eight or more consecutive ones. This is because SDLC utilizes a process called bit stuffing. Bit stuffing is the insertion of a 0 as the next bit every time a sequence of five consecutive 1s is detected. The receiver automatically removes a 0 after every consecutive group of five ones. This removal of the 0 bit is referred to as bit stripping. Bit stuffing is discussed in Section 3.3.4. All the procedures required for bit stuffing and bit stripping are automatically handled by the GSC.

In standard SDLC protocol the BOF signals the start of a frame and is limited to 8 bits in length. Since there is no preamble in SDLC the BOF is considered an entire separate field and marks the beginning of the frame. The BOF also serves as the clock synchronization mechanism and the reference point for determining the position of the address and control fields.

ADDRESS - The address field is used to identify which stations the message is intended for. Each secondary station must have a unique address. The primary station must then be made aware of which addresses are assigned to each station. The address length is specified as 8-bits in standard SDLC protocols but it is expandable to 16-bits in the C152. User software can further expand the number of address bits, but the automatic address recognition feature works on a maximum of 16-bits.

In SDLC the addresses are normally unique for each station. However, there are several classes of messages that are intended for more than one station. These messages are called broadcast and group addressed frames. An address consisting of all 1s will always be automatically received by the GSC, this is defined as the broadcast address in SDLC. A group address is an address that is common to more than one station. The GSC provides address masking bits to provide the capability of receiving group addresses.

If desired, the user software can mask off all the bits of the address. This type of masking puts the GSC in a promiscuous mode so that all addresses are received.

CONTROL - The control field is used for initialization of the system, identifying the sequence of a frame, to identify if the message is complete, to tell secondary stations if a response is expected, and acknowledgement of previously sent frames. The user software is responsible for insertion of the control field as the GSC hardware has no provisions for the management of this field. The interpretation and formation of the control field must also be handled by user software. The information following the control field is typically used for information transfer, error reporting, and various other functions. These functions are accomplished by the format of the control field. There are three formats available. The types of formats are Informational, Supervisory, or Unnumbered. Figure 3.7 shows the various format types and how to identify them.

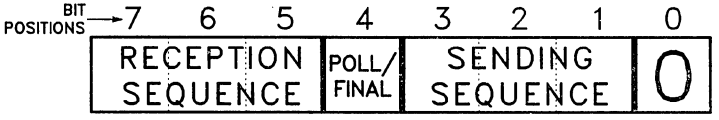
Since the user software is responsible for the implementation of the control field, what follows is a simple explanation on the control field and its functions. For a complete understanding and proper implementation of SDLC, the user should refer to the IBM document, GA27-3093-2, IBM Synchronous Data Link Control General Information. Within that document, is another list of IBM documents which go into detail on the SDLC protocol and its use.

The control field is eight bits wide and the format is determined by bits 0 and 1. If bit 0 is a zero, then the frame is an informational frame. If bit 0 is a one and bit 1 a zero, then it is a supervisory frame, and if bit 0 is a one and bit 1 a one then the frame is an unnumbered frame.

In an informational frame bits 3,2,1 contain the sequence count of the frame being sent.

Bit 4 is the P/F (Poll/Final) bit. If bit 4 equals 1 and originates from the primary, then the secondary station is expected to initiate a transmission. If bit 4 equals 1 and originates from a secondary station, then the frame is the final frame in a transmission.

Bits 7,6,5 contain the sequence count a station expects on the next transmission to it. The sequence count can vary from 000B to 111B. The count then starts over again at 000B after the value 111B is incremented. The acknowledgement is recognized by the receiving station when it decodes bits 7,6,5 of an incoming frame. The station sending the transmission is acknowledging the frames received up to the count represented in bits 7,6,5 (sequence count-1). With this method, up to seven sequential frames may be transmitted prior to an acknowledgement being received. If eight frames were allowed to pass before an acknowledgement, the sequence count would roll over and this would negate the purpose of the sequence numbers.



270427-15

RECEPTION SEQUENCE - The sequence expected in the SENDING SEQUENCE portion of the control byte in the next received frame. This also confirms correct reception of up to seven frames prior to the sequence given.

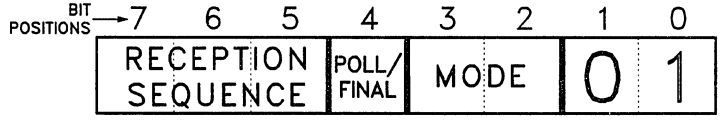
POLL/FINAL - Identifies the frame as being a polling request from the master station or the last in a series of frames from the master or secondary.

SENDING SEQUENCE - Identifies the sequence of the frame being transmitted.

0 - If bit 0 = 0 the frame is identified as a informational format type.

10

INFORMATION FORMAT



270427-16

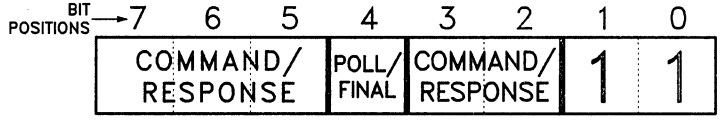
RECEPTION SEQUENCE - Expected sequence of frame for next reception.

POLL/FINAL - Identifies frame as being a polling request from the master station or the last in a series of frames from the master or secondary.

MODE - Identifies whether receiver is ready (00), not ready (10) or a frame was rejected (01). The rejected frame is identified by the reception sequence.

0,1 - If bits 1,0 = 0,1 the frame is identified as a supervisory format type.

SUPERVISORY FORMAT



270427-17

COMMAND/RESPONSE - Identifies the type of command or response.

POLL/FINAL - Identifies frame as being a polling request from the master station or the last in a series of frames from the master or secondary.

1,1 - If bits 1,0 = 1,1 the frame is identified as an unnumbered format type.

NONSEQUENCED FORMAT

270427-18

Figure 3.7. SDLC Control Field

Following the informational control field comes the information to be transferred.

In the supervisory format (bits 1,0 = 0,1) bits 3,2 determine which mode is being used.

When the mode is 00 it indicates that the receive line of the station that sent the supervisory frame is enabled and ready to accept frames.

When the mode is 01, it indicates that previously a received frame was rejected. The value in the receive count identifies which frame(s) need to be retransmitted.

When the mode is 10, the sending station is indicating that its receiver is not ready to accept frames.

Mode 11 is an illegal mode in SDLC protocol.

Bits 7,6,5 represent the value of the sequence the station expects when the next transfer occurs for that station. There is no information following the control field when the supervisory format is used.

In the unnumbered format (bits 1,0 = 1,1) bits 7, 6, 5, 3, 2 (notice bit 4 is missing) indicate commands from the primary to secondary stations or requests of secondary stations to the primary.

The standard commands are:

BITS 7	6	5	3	2	Command
0	0	0	0	0	Unnumbered Information (UI)
0	0	0	0	1	Set initialization mode (SIM)
0	1	0	0	0	Disconnect (DISC)
0	0	1	0	0	Response optional (UP)
1	1	0	0	1	Function descriptor in information field (CFGR)
1	0	1	1	1	Identification in information field. (XID)
1	1	1	0	0	Test pattern in information field. (TEST)

The standard responses are:

BITS 7	6	5	3	2	Command
0	0	0	0	0	Unnumbered information (UI)
0	0	0	0	1	Request for initialization (RIM)
0	0	0	1	1	Station in disconnected mode (DM)
1	0	0	0	1	Invalid frame received (FRMR)
0	1	1	0	0	Unnumbered acknowledgement (UA)
1	1	1	1	1	Signal loss of input (BCN)
1	1	0	0	1	Function descriptor in information field (CFGR)
0	1	0	0	0	Station wants to disconnect (RD)
1	0	1	1	1	Identification in information field (XID)
1	1	1	0	0	Test pattern in information field (TEST)

In an unnumbered frame, information of variable length may follow the control field if UI is used, or information of fixed length may follow if FRMR is used.

As stated earlier, the user software is responsible for the proper management of the control field. This portion of the frame is passed to or from the GSC FIFOs as basic informational type data.

INFO - This is the information field and contains the data that one device on the link wishes to transmit to another device. It can be of any length the user wishes, but must be a multiple of 8 bits. It is possible that some frames may contain no information field. The information field is identified to the receiving stations by the preceding control field and the following CRC. The GSC determines where the last of the information field is by passing the bits through the CRC generator. When the last bit or EOF is received the bits that remain constitute the CRC.

CRC - The Cyclic Redundancy Check (CRC) is an error checking sequence commonly used in serial communications. The C152 offers two types of CRC algorithms, a 16-bit and a 32-bit. The 32-bit algorithm is normally used in CSMA/CD applications and is described in section 3.2.2. In most SDLC applications a 16-bit CRC is used and the hardware configuration that supports 16-bit CRC is shown in Figure 3.8. The generating polynomial that the CRC generator uses with the 16-bit CRC is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The way the CRC operates is that as a bit is received it is XOR'd with bit 15 of the current CRC and placed in temporary storage. The result of XOR'ing bit 15 with the received bit is then XOR'd with bit 4 and bit 11 as the CRC is shifted one position to the right. The bit in temporary storage is shifted into position 0.

The required CRC length for SDLC is 16 bits. The CRC is automatically stripped from the frame and not passed on to the CPU. The last 16 bits are then run though the CRC generator to insure that the correct remainder is left. The remainder that is checked for is 001110100001111B (1D0F Hex). If there is a mismatch, an error is generated. The user software has the option of enabling this interrupt so the CPU is notified.

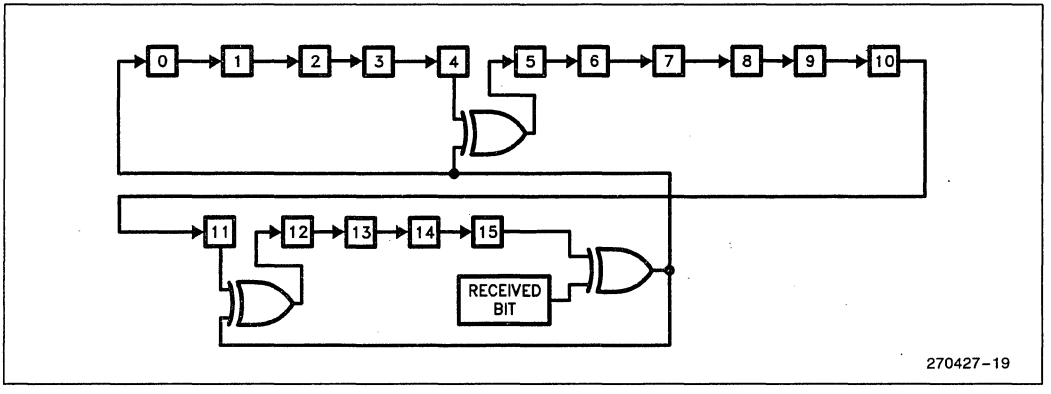


Figure 3.8. 16-Bit CRC

EOF - The End Of Frame (EOF) indicates when the transmission is complete. The EOF is identified by the end flag. An end flag consists of the bit pattern 01111110. The EOF can also serve as the BOF for the next frame.

3.3.3 DATA ENCODING

The transmission of data in SDLC mode is done via NRZI encoding as shown in Figure 3.9. NRZI encoding transmits data by changing the state of the output whenever a 0 is being transmitted. Whenever a 1 is transmitted the state of the output remains the same as the previous bit and remains valid for the entire bit time. When SDLC mode is selected it automatically enables the NRZI encoding on the transmit line and NRZI decoding on the receive line. The Address and Info bytes are transmitted LSB first. The CRC is transmitted MSB first.

3.3.4 BIT STUFFING/STRIPPING

In SDLC mode one of the primary rules of the protocol is that in any normal data transmission, there will never be an occurrence of more than 5 consecutive 1s. The GSC takes care of this housekeeping chore by automatically inserting a 0 after every occurrence of 5 consecutive 1s and the receiver automatically removes a zero after receiving 5 consecutive 1s. All the necessary steps required for implementing bit stuffing and stripping are incorporated into the GSC hardware. This makes the operation transparent to the user. About the only time this operation becomes apparent to the user, is if the actual data on the transmission medium is being monitored by a device that is not aware of the automatic insertion of 0s. The bit stuffing/stripping guarantees that there will be at least one transition every 6 bit times while the line is active.

3.3.5 SENDING ABORT CHARACTER

An abort character is one of the exceptions to the rule that disallows more than 5 consecutive 1s. The abort character consists of any occurrence of seven or more consecutive ones. The simplest way for the C152 to send an abort character is to clear the TEN bit. This causes the output to be disabled which, in turn, forces it to a constant high state. The delay necessary to insure that the link is high for seven bit times is a task that needs to be handled by user software. Other methods of sending an abort character are using the IFS register or using the Raw Transmit mode. Using IFS still entails clearing the TEN bit, but TEN can be immediately re-enabled. The next message will not begin until the IFS expires. The IFS begins timing out as soon as $\overline{DEN}$ goes high which identifies the end of transmission. This also requires that IFS contain a value equal to or greater than 8. This method may have the undesirable effect that $\overline{DEN}$ goes high and disables the external drivers. The other alternative is to switch to Raw Transmit mode. Then, writing 0FFH to TFIFO would generate a high output for 8 bit times. This method would leave $\overline{DEN}$ active during the transmission of the abort character.

When the receiver detects seven or more consecutive 1s and data has been loaded into the receive FIFO, the RCABT flag is set in RSTAT and that frame is ignored. If no data has been loaded into the receive FIFO, there are no abort flags set and that frame is just ignored. A retransmitted frame may immediately follow an abort character, provided the proper flags are used.

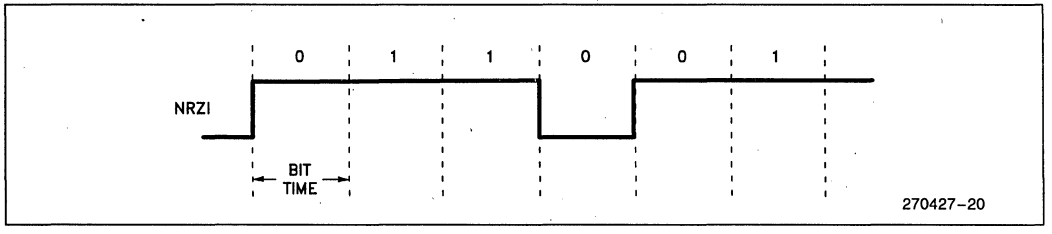


Figure 3.9. NRZI Encoding

3.3.6 LINE IDLE

If 15 or more consecutive 1s are detected by the receiver the Line Idle bit (LNI) in TSTAT is set. The seven 1s from the abort character may be included when sensing for a line idle condition. The same methods used for sending the Abort character can be used for creating the Idle condition. However, the values would need to be changed to reflect 15 bit times, instead of seven bit times.

3.3.7 ACKNOWLEDGEMENT

Acknowledgment in SDLC is an implied acknowledge and is contained in the control field. Part of the control frame is the sequence number of the next expected frame. This sequence number is called the Receive Count. In transmitting the Receive Count, the receiver is in fact acknowledging all the previous frames prior to the count that was transmitted. This allows for the transmission of up to seven frames before an acknowledge is required back to the transmitter. The limitation of seven frames is necessary because the Receive Count in the control field is limited to three binary digits. This means that if an eighth transmission occurred this would cause the next Receive Count to repeat the first count that still is waiting for an acknowledge. This would defeat the purpose of the acknowledgement. The processing and general maintenance of the sequence count must be done by the user software. The Hardware Based Acknowledge option that is provided in the C152 is not compatible with standard SDLC protocol.

3.3.8 PRIMARY/SECONDARY STATIONS

All SDLC networks are based upon a primary/secondary station relationship. There can be only one primary station in a network and all the other stations are considered secondary. All communication is between the primary and secondary station. Secondary station to secondary station direct communication is prohibited. If there is a need for secondary to secondary communication, the user software will have to make allowances for the master to act as an intermediary. Secondary stations are allowed use of the serial line only when the master permits them. This is done by the master polling the secondary stations to see if they have a need to access the serial line. This should prevent any collisions from occurring, provided each secondary station has its own unique address. This arrangement also partially determines the types of networks supported. Normal SDLC networks consist of point-to-point, multi-drop, or ring configurations and the C152 supports all of these. However, some SDLC processors support an automatic one bit delay at each node that is not supported by the C152. In a "Loop Mode" configuration, is is necessary that the transmission be delayed from the reception of the frames from the upstream station before passing the message to the downstream station. This delay is necessary so that a station can decode its own address before the message is passed on. The various networks are shown in Figure 3.10.

3.3.9 HDLC/SDLC COMPARISON

HDLC (High level Data Link Control) is a standard adopted by the International Standards Organization (ISO). The HDLC standard is defined in the ISO document #ISO 6159 - HDLC unbalanced classes of procedures. IBM developed the SDLC protocol as a subset of HDLC. SDLC conforms to HDLC protocol requirements, but is more restrictive. SDLC contains a more precise definition on the modes of operation.

10

Some of the major differences between SDLC and HDLC are:

SDLC	HDLC
Unbalanced (primary/ secondary)	Balanced (peer to peer)
Modulo 8 (no extensions allowed, up to 7 outstanding frames before acknowledge is required)	Modulo 128 (up to 127 outstanding frames before acknowledge is required)
8-bit addressing only	Extended addressing
Byte aligned data	Variable size of data

The C152 does not support HDLC implementation requiring data alignment other than byte alignment. The user will find that many of the protocol parameters are programmable in the C152 which allows easy implementation of proprietary or standard HDLC network. User software needs to implement the control field functions.

3.3.10 USING A PREAMBLE IN SDLC

When transmitting a preamble in SDLC mode, the user should be aware that the pattern of 10101010 . . . is output. NRZI encoding is used in SDLC when the internal baud rate generator is the clock source and this means that a transition will occur every two bit times, when a 0 is transmitted. This compares with some other SDLC devices, most of which transmit the pattern 00000000 . . . which will cause a transition every bit time. Our past experience has shown that the C152 preamble does not cause a problem with most other devices. This is because the preamble is used only to define the relative bit time boundaries within some variation allowed by the receiving station, and the C152 preamble fulfills this function. The C152 does not have any problems with receiving a preamble consisting of all 0s. One note of caution however. If idle fill flags are used in conjunction with a preamble, the addresses 00(00)H and 55(55)H should not be assigned to any C152 as the preamble following the idle fill flags will be interpreted as an address.

3.4 User Defined Protocols

The explanation on the implementation of user defined protocols would go beyond the scope of this manual, but examining Table 3.1 should give the reader a consolidated list of most of the possibilities. In this manual, any deviation from the documents that cover the implementation of CSMA/CD or SDLC are considered user defined protocols. Examples of this would be the use of SDLC with the 32-bit CRC selected or CSMA/CD with hardware based acknowledge.

3.5 Using the GSC

3.5.1 LINE DISCIPLINE

Line discipline is how the management of the transfer of data over the physical medium is controlled. Two types of line discipline will be discussed in this section: full duplex and half duplex.

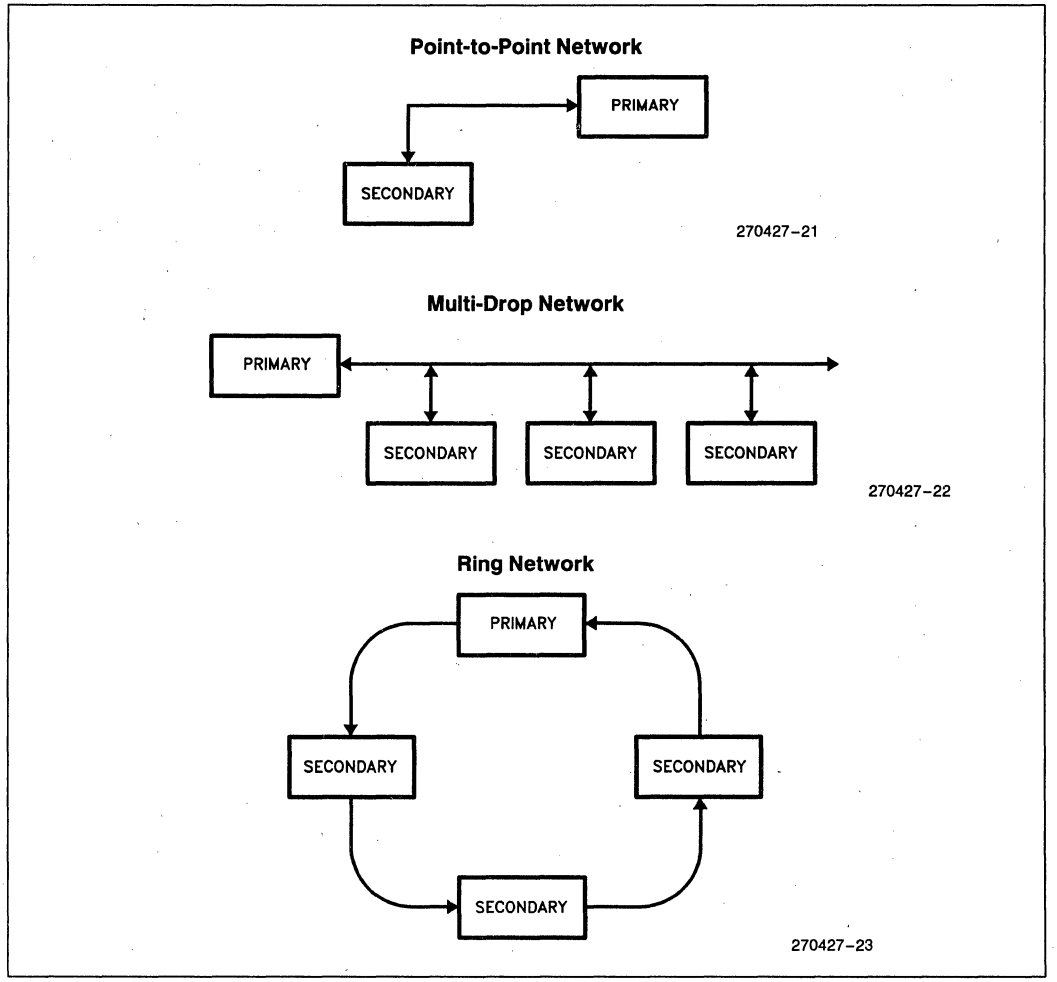


Figure 3.10. SDLC Networks

Full duplex is the simultaneous transmission and reception of data. Full duplex uses anywhere from two to four wires. At least one wire is needed for transmission and one wire for reception. Usually there will also be a ground reference on each signal if the distance from station to station is relatively long. Full-duplex operation in the C152 requires that both the receive and the transmit portion of the GSC are functioning at the same time. Since both the transmitter and receiver are operating, two CRC generators are also needed. The C152 handles this problem by having one 32-bit CRC generator and one 16-bit CRC generator. When supporting full-duplex operation, the 32-bit CRC generator is modified to work as a 16-bit CRC generator. Whenever the 16-bit CRC is selected, the GSC automatically enters the full duplex mode. Half duplex with a 16-bit CRC is discussed in the following paragraph.

Half duplex is the alternate transmission and reception of data over a single common wire. Only one or two wires are needed in half-duplex systems. One wire is needed for the signal and if the distance to be covered is long there will also be a wire for the ground reference. In half-duplex mode, only the receiver or transmitter can operate at one time. When the receiver or transmitter operates is determined by user software, but typically the receiver will always be enabled unless the GSC is transmitting. When using the C152 in half-duplex and the receiver is connected to the transmitter it is possible that a station will receive its' own transmission. This can occur if a broadcast address is sent, the address mask register(s) are filled with all 1s, or the address being sent matches the sending stations address through the use of the address masking registers. The receiver must be disabled by the user while transmitting if any of these conditions will occur, unless the user wants a station to receive its own transmission. The receiver is disabled by clearing GREN (and GAREN if used). Half-duplex operation in the C152 is supported with either 16-bit or 32-bit CRCs. Whenever a 32-bit CRC is selected, only half-duplex operation can be supported by the GSC. It is possible to simulate full-duplex operation with a 32-bit CRC, but this would require that the CRC be performed with software. Calculating the CRC with the CPU would greatly reduce the data rates that could be used with the GSC. Whenever a 16-bit CRC is selected, full-duplex operation is automatically chosen and the GSC must be reconfigured if half-duplex operation is preferred.

3.5.2 PLANNING FOR NETWORK CHANGES AND EXPANSIONS

A complete explanation on how to plan for network expansion will not be covered in this manual as there are far too many possibilities that would need to be discussed. But there are several areas that will have major impact when allowing for changes in the system. In cases where there will never be any changes allowed, expansion plans become a mute issue. However, it is strongly suggested that there always be some allowance for future modifications.

Some of the general areas that will impact the overall scheme on how to incorporate future changes to the system are:

1) Communication of the change to all the stations or the primary station.

2) Maximum distance for communication. This will affect the drivers used and the slot time.

3) More stations may be on the line at one time. This may impact the interframe space or the collision resolution used.

4) If using CSMA/CD without deterministic resolution, any increase in network size will have a negative impact on the average throughput of the network and lower the efficiency. The user will have to give careful consideration when deciding how large a system can ultimately be and still maintain adequate performance.

3.5.3 DMA SERVICING OF GSC CHANNELS

There are two sources that can be used to control the GSC. The first is CPU control and the second is DMA control.

CPU control is used when user software takes care of the tasks such as: loading the TFIFO, reading the RFIFO, checking the status flags, and general tracking of the transmission process. As the number of tasks grow and higher data transfer rates are used, the overhead required by the CPU becomes the dominant consumption of time. Eventually, a point is reached where the CPU is spending 100% of its time responding to the needs of the GSC. An alternative is to have the DMA channels control the GSC.

A detailed explanation on the general use of the DMA channels is covered in Section 4. In this section only those details required for the use of the DMA channels with the GSC will be covered.

The DMA channels can be configured by user software so that the GSC data transfers are serviced by the DMA controller. Since there are two DMA channels, one channel can be used to service the receiver, and one channel can be used to service the transmitter. In using the DMA channels, the CPU is relieved of much of the time required to do the basic servicing of the GSC buffers. The types of servicing that the DMA channels can provide are: loading of the transmit FIFO, removing data from the receive FIFO, notification of the CPU when the transmission or reception has ended, and response to certain error conditions. When using the

DMA channels the source or destination of the data intended for serial transmission can be internal data memory, external data memory, or any of the SFRs.

The only tasks required after initialization of the DMA and GSC registers are enabling the proper interrupts and informing the DMA controller when to start. After the DMA channels are started all that is required of the CPU is to respond to error conditions or wait until the end of transmission.

Initialization of the DMA channels requires setting up the control, source, and destination address registers. On the DMA channel servicing the receiver, the control register needs to be loaded as follows: DCONn.2 = 0, this sets the transfer mode so that response is to GSC interrupts and put the DMA control in alternate cycle mode; DCONn.3 = 1, this enables the demand mode; DCONn.4 = 0, this clears the automatic increment option for the source address; and DCONn.5 = 1, this defines the source as SFR. The DMA channel servicing the receiver also needs its source address register to contain the address of RFIFO (SARHN = XXH, SARLN = 0F4H). On the DMA channel servicing the transmitter, the control register needs to be loaded as follows: DCONn.2 = 0; DCONn.3 = 1; DCONn.6 = 0, this clears the automatic increment option for the destination address; and DCONn.7 = 1, this sets the destination as SFR. The DMA channel serving the transmitter also requires that its destination address register contains the address of TFIFO (DARHN = XXH, DARLN = 85H). Assuming that DCON0 would be serving the receiver and DCON1 the transmitter, DCON0 would be loaded with XX1010X0B and DCON1 would be loaded with 10XX10X0B. The contents of SARH0 and DARH1 do not have any impact when using internal SFRs as the source or destination.

When using the DMA channels to service the GSC, the byte count registers will also need to be initialized.

The Done flag for the DMA channel servicing the receiver should be used if fixed packet lengths only are being transmitted or to insure that memory is not overwritten by long received data packets. Overwriting of data can occur when using a smaller buffer than the packet size. In these cases the servicing of the DMA and/or GSC would be in response to the DMA Done flag when the byte count reaches zero.

In some cases the buffer size is not the limiting factor and the packet lengths will be unknown. In these cases it would be desirable to eliminate the function of the Done flag. To effectively disable the Done flag for the DMA channel servicing the receiver, the byte count should be set to some number larger than any packet that will be received, up to 64K. If not using the Done flag, then GSC servicing would be driven by the receive Done (RDN) flag and/or interrupt. RDN is set when the EOF is detected. When using the RDN flag, RFNE should also be checked to insure that all the data has been emptied out of the receive FIFO.

The byte count register is used for all transmissions and this means that all packets going out will have to be of the same length or the length of the packet to be sent will have to be known prior to the start of transmission. When using the DMA channels to service the GSC transmitter, there is no practical way to disable the Done flag. This is because the transmit done flag (TDN) is set when the transmit FIFO is empty and the last message bit has been transmitted. But, when using the DMA channel to service the transmitter, loads to the TFIFO continue to occur until the byte count reaches 0. This makes it impossible to use TDN as a flag to stop the DMA transfers to TFIFO. It is possible to examine some other registers or conditions, such as the current byte count, to determine when to stop the DMA transfers to TFIFO, but this is not recommended as a way to service the DMA and GSC when transmitting because frequent reading of the DMA registers will cause the effective DMA transfer rate to slow down.

When using the DMA channels, initialization of the GSC would be exactly the same as normal except that TSTAT.0 = 1 (DMA), this informs the GSC that the DMA channels are going to be used to service the GSC. Although only TSTAT is written to, both the receiver and transmitter use this same DMA bit.

The interrupts EGSTE (IEN1.5), GSC transmit error; EGSTV (IEN1.3), GSC transmit valid; EGSRE (IEN1.1), GSC receive error; and EGSRV (IEN1.0), GSC receive valid; need to be enabled. The DMA interrupts are normally not used when servicing the GSC with the DMA channels. To ensure that the DMA interrupts are not responded to is a function of the user software and should be checked by the software to make sure they are not enabled. Priority for these interrupts can also be set at this time. Whether to use high or low priority needs to be decided by the user. When responding to the GSC interrupts, if a buffer is being used to store the GSC information, then the DMA registers used for the buffer will probably need updating.

After this initialization, all that needs to be done when the GSC is actually going to be used is: load the byte count, set-up the source addresses for the DMA channel servicing the transmitter, set-up the destination addresses for the DMA channel servicing the receiver, and start the DMA transfer. The GSC enable bits should be set first and then the GO bits for the DMA. This initiates the data transfers.

This simplifies the maintenance of the GSC and can make the implementation of an external buffer for packetized information automatic.

An external buffer can be used as the source of data for transmission, or the destination of data from the receiver. In this arrangement, the message size is limited to the RAM size or 64K, whichever is smaller. By using an external buffer, the data can be accessed by other devices which may want access to the serial data. The amount of time required for the external data moves will also decrease. Under CPU control, a "MOVX" command would take 24 oscillator periods to complete. Under DMA control, external to internal, or internal to external, data moves take only 12 oscillator periods.

3.5.4 BAUD RATE

The GSC baud rate is determined by the contents of the SFR, BAUD, or the external clock. The formula used to determine the baud rate when using the internal clock is:

(fosc)/((BAUD+1)*8)

For example if a 12 MHz oscillator is used the baud rate can vary from:

12,000,000/((0+1)*8) = 1.5 MBPS

to:

12,000,000/((255+1)*8) = 5.859 KBPS

There are certain requirements that the external clock will need to meet. These requirements are specified in the data sheet. For a description of the use of the GSC with external clock please read Section 3.5.11.

3.5.5 INITIALIZATION

Initialization can be broken down into two major components, 1) initialization of the component so that its serial port is capable of proper communication; and 2) initialization of the system or a station so that intelligible communication can take place.

Most of the initialization of the component has already been discussed in the previous sections. Those items not covered are the parameters required for the component to effectively communicate with other components. These types of issues are common to both system and component initialization and will be covered in the following text.

Initialization of the system can be broken down into several steps. First, are the assumptions of each network station.

The first assumption is that the type of data encoding to be used is predetermined for the system and that each station will adhere to the same basic rules defining that encoding. The second assumption is that the basic protocol and line discipline is predetermined and known. This means that all stations are using CSMA/CD or SDLC or whatever, and that all stations are either full or half duplex. The third assumption is that the baud rate is preset for the whole system. Although the baud rate could probably be determined by the microprocessor just by monitoring the link, it will make it much simpler if the baud rate is known in advance.

One of the first things that will be required during system initialization is the assignment of unique addresses for each station. In a two-station only environment this is not necessary and can be ignored. However, keep in mind, that all systems should be constructed for easy future expansions. Therefore, even in only a two station system, addresses should be assigned. There are three basic ways in which addresses can be assigned. The first, and most common is preassigned addresses that are loaded into the station by the user. This could be done with a DIP-switch, through a keyboard. The second method of assigning addresses is to randomly assign an address and then check for its uniqueness throughout the system, and the third method is to make an inquiry to the system for the assignment of a unique address. Once the method of address assignment is determined, the method should become part of the specifications for the system to which all additions will have to adhere. This, then, is the final assumption.

The negotiation process may not be clear for some readers. The following two procedures are given as a guideline for dynamic address assignment.

In the first procedure, a station assumes a random address and then checks for its uniqueness throughout the system. As a station is initialized into the system it sends out a message containing its assumed address. The format of the message should be such that any station decoding the address recognizes it as a request for initialization. If that address is already used, the receiving station returns a message, with its own address stating that the address in question is already taken. The initializing station then picks another address. When the initializing station sends its inquiry for the address check, a timer is also started. If the timer expires before the inquiry is responded to, then that station assumes the address chosen is okay.

In the second procedure, an initializing station asks for an address assignment from the system. This requires that some station on the link take care of the task of maintaining a record of which addresses are used. This station will be called station-1. When the initializing station, called station-2, gets on the link, it sends out a message with a broadcast address. The format of the message should be such that all other stations on the link recognize it as a request for address assignment. Part of the message from station-2 is a random number generated by the station requesting the address. Station-2 then examines all received messages for this random number. The random number could be the address of the received message or could be within the information section of a broadcast frame. All the stations, except station-1, on the link should ignore the initialization request. Station-1, upon receiving the initialization request, assigns an address and returns it to station-2. Station-1 will be required to format the message in such a manner so that all stations on the link recognize it as a response to initialization. This means that all stations except station-2 ignore the return message.

3.5.6 TEST MODES

There are two test modes associated with the GSC that are made available to the user. The test modes are named Raw Receive and Raw Transmit. The test modes are selected by the proper setting of the two mode bits in GMOD (M0 = GMOD.5, M1 = GMOD.6). If M1,M0 = 0,1 then Raw Transmit is selected. If M1,M0 = 1,0 then Raw Receive is enabled. The 32-bit CRC cannot be used in any of the test modes, or else CRC errors will occur.

In Raw Transmit, the transmit output is internally connected to the Receiver input. This is intended to be used as a local loop-back test mode, so that all data written to the transmitter will be returned by the receiver. Raw Transmit can also be used to transmit user data. If Raw Transmit is used in this way the data is emitted with no preamble, flag, address, CRC, and no bit insertion. The data is still encoded with whatever format is selected, Manchester with CSMA/CD, NRZI with SDLC or as NRZ if external clocks are used. The receiver still operates as normal and in this mode most of the receive functions can be tested.

In Raw Receive, the transmitter should be externally connected to the receiver. To do this a port pin should be used to enable an external device to connect the two pins together. In Raw Receive mode the receiver acts as normal except that all bytes following the BOF are loaded into the receive FIFO, including the CRC. Also address recognition is not active but needs to be performed in software. If SDLC is selected as the protocol, zero-bit deletion is still enabled. The transmitter still operates as normal and in this mode most of the transmitter functions and an external transceiver can be tested. This is also the only way that the CRC can be read by the CPU, but the CRC error bit will not be set.

3.5.7 EXTERNAL DRIVER INTERFACE

A signal is provided from the C152 to enable transmitter drivers for the serial link. This is provided for systems that require more than what the GSC ports are capable of delivering. The voltage and currents that the GSC is capable of providing are the same levels as those for normal port operation. The signal used to enable the external drivers is $\overline{\text{DEN}}$. No similar signal is needed for the receiver.

$\overline{\text{DEN}}$ is active one bit time before transmission begins. In CSMA/CD $\overline{\text{DEN}}$ remains active for two bit times after the CRC is transmitted. In SDLC $\overline{\text{DEN}}$ remains active until the last bit of the EOF is transmitted.

3.5.8 JITTER (RECEIVE)

Data jitter is the difference between the actual transmitted waveform and the exact calculated value(s). In NRZI, data jitter would be how much the actual waveform exceeds or falls short of one calculated bit time. A bit time equals 1/baud rate. If using Manchester encoding, there can be two transitions during one bit time as shown in Figure 3.11. This causes a second parameter to be considered when trying to figure out the complete data jitter amount. This other parameter is the half-bit jitter. The half-bit jitter is comprised of the difference in time that the half-bit transition actually occurs and the calculated value. Jitter is important because if the transition occurs too soon it is considered noise, and if the transition occurs too late, then either the bit is missed or a collision is assumed.

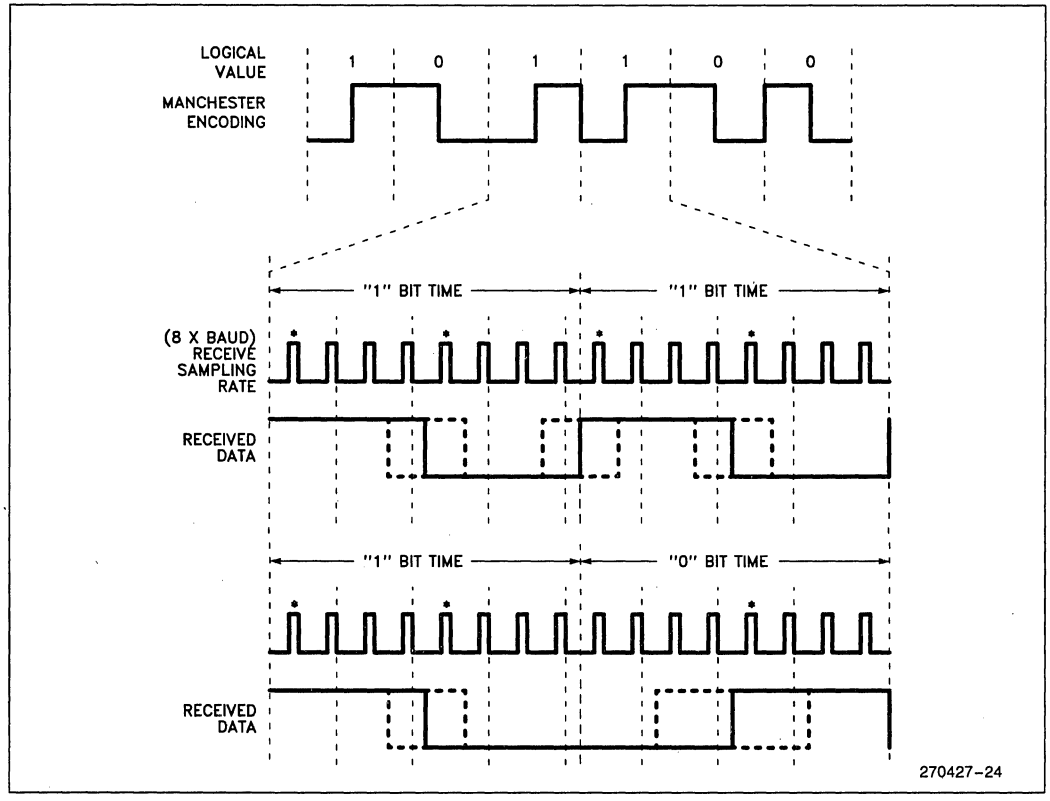


Figure 3.11. Jitter

3.5.9 Transmit Waveforms

The GSC is capable of three types of data encoding, Manchester, NRZI, and NRZ. Figure 3.12 shows examples of all three types of data encoding.

3.5.10 Receiver Clock Recovery

The receiver is always monitored at eight times the baud rate frequency, except when an external clock is used. When using an external clock the receiver is loaded during the clock cycle.

In CSMA/CD mode the receiver synchronizes to the transmitted data during the preamble. If a pulse is detected as being too short it is assumed to be noise or a collision. If a pulse is too long it is assumed to be a collision or an idle condition.

In SDLC the synchronization takes place during the BOF flag. In addition, pulses less than four sample periods are ignored, and assumed to be noise. This sets a lower limit on the pulse size of received zeros.

In CSMA/CD the preamble consists of alternating 1s and 0s. Consequently, the preamble looks like the waveform in Figure 3.13A and 3.13B.

3.5.11 External Clocking

To select external clocking, the user is given three choices. External clocking can be used with the transmitter, with the receiver, or with both. To select external clocking for the transmitter, XTCLK (GMOD.7) has to be set to a 1. To select external clocking for the receiver, XRCLK (PCON.3) has to be set to a 1. Setting both bits to 1 forces external clocking for the receiver and transmitter. The minimum frequency the GSC can be externally clocked at is 0 Hz (D.C.).

The external transmit clock is applied to pin 4 ($\overline{TXC}$), P1.3. The external receive clock is applied to pin 5 ($\overline{RXC}$), P1.4. To enable the external clock function on the port pin, that pin has to be set to a 1 in the appropriate SFR, P1.

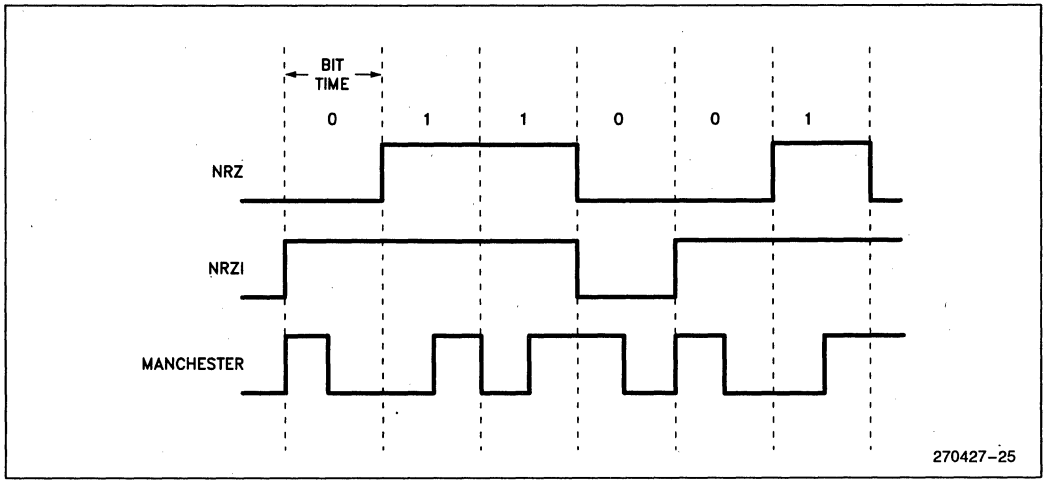


Figure 3.12. Transmit Waveforms

Whenever the external clock option is used, the format of the transmitted and received data is restricted to NRZ encoding and the protocol is restricted to SDLC. With external clock, the bit stuffing/stripping is still active with SDLC protocol.

3.5.12 Determining Receiver Errors

It is possible that several receiver error bits will be set in response to a single cause. The multiple errors that can occur are:

AE and CRCE may both be set when an alignment error occurs due to a bad CRC caused by the misaligned frame.

RCABT, AE, and CRCE may be set when an abort occurs.

OVR, AE, and CRCE may be set when a overrun occurs.

In order to determine the correct cause of the error a specific order should be followed when examining the error bits. This order is:

1) OVR
2) RCBAT
3) AE
4) CRCE

3.5.13 Addressing

There are four 8-bit address registers (ADR0, ADR1, ADR2, ADR3) and two 8-bit address mask registers (AMSK0, AMSK1) in the C152. These function with the GSC receiver only. The transmitted address is treated like any other data. The address is transmitted under software control by placing the address byte(s) at the proper location (usually first) in the sequence of bytes to be output in the outgoing packet.

The C152 can have up to four different 8-bit addresses or two different 16-bit addresses assigned to each station. When using 16-bit addressing, ADR0:ADR1 form one address and ADR2:ADR3 form the second address. If the receiver is enabled, it looks for a matching address after every BOF flag is detected. As the data is received, if the 8th (or 16th) bit does not match the address recognition circuitry, the rest of the frame is ignored and the search continues for another flag. If the address does match the address recognition circuitry, the address and all subsequent data is passed into the receive FIFO until the EOF flag or an error occurs. The address is not stripped and is also passed to RFIFO.

The address masking registers, AMSK0 and AMSK1, work in conjunction with ADR0 and ADR1 respectively to identify "don't care" bits. A 1 in any position in the AMSKn register makes the respective bit in the ADRn register irrelevant. These combinations can then be used for form group addresses. If the masking registers are filled with all 1s, the C152 will receive all packets, which is called the promiscuous mode. If 16-bit addressing is used, AMSK0:AMSK1 form one 16-bit address mask.

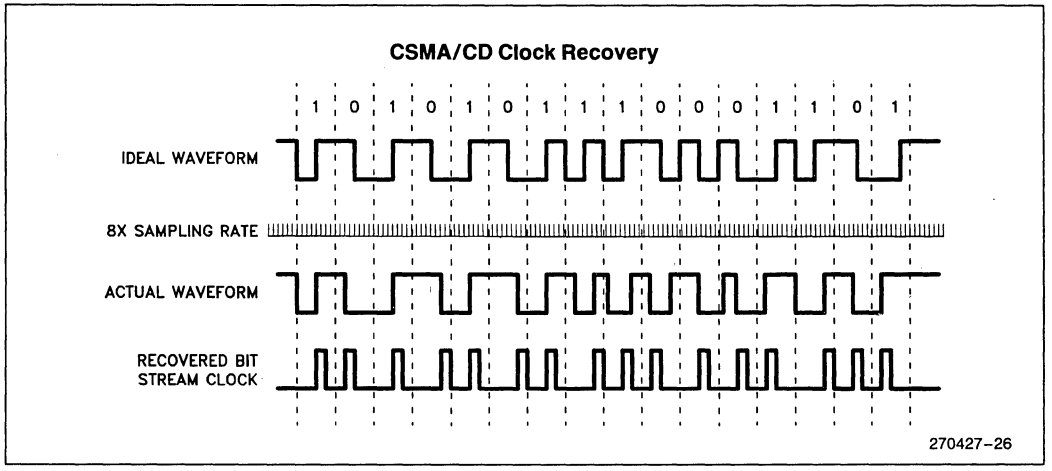


Figure 3.13A. Clock Recovery

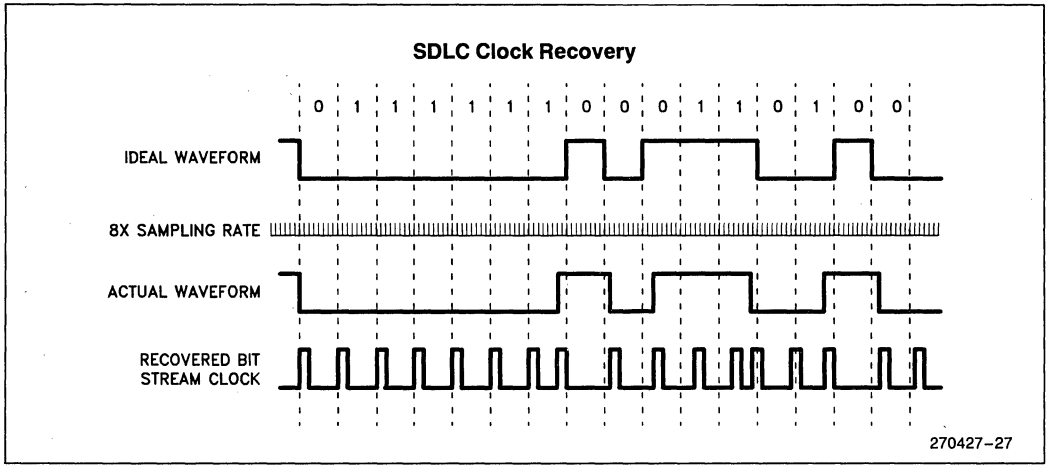


Figure 3.13B. Clock Recovery

3.6 GSC Operation

3.6.1 Determining Line Discipline

In normal operation the GSC uses full or half duplex operation. When using a 32-bit CRC (GMOD.3 = 1), operation can only be half duplex. If using a 16-bit CRC (GMOD.3 = 0), full duplex is selected by default. When using a 16-bit CRC the receiver can be turned off while transmitting (RSTAT.1 = 0), and the transmitter can be turned off during reception (TSTAT.1 = 0). This simulates half-duplex operation when using a 16-bit CRC.

Normally, HDLC uses a 16-bit CRC, so half duplex is determined by turning off the receiver or transmitter. This is so that the receiver will not detect its own address as transmission takes place. This also needs to be done when using CSMA/CD with a 16-bit CRC for the same reason.

3.6.2 CPU/DMA CONTROL OF THE GSC

The data for transmission or reception can be handled by either the CPU (TSTAT.0 = 0) or DMA controller (TSTAT.0 = 1). This allows the user two sets of flags to control the FIFO. Associated with these flags are interrupts, which may be enabled by the user software. Either one or both sets of flags may be used at the same time.

In CPU control mode the flags (RFNE,TFNF) are generated by the condition of the receive or transmit FIFO's. After loading a byte into the transmit FIFO, there is a one machine cycle latency until the TFNF flag is updated. Because of this latency, the status of TFNF should not be checked immediately following the instruction to load the transmit FIFO. If using the interrupts to service the transmit FIFO,the one machine cycle of latency must be considered if the TFNF flag is checked prior to leaving the subroutine.

When using the CPU for control, transmission normally is initiated by setting the TEN bit (TSTAT.1) and then writing to TFIFO. TEN must be set before loading the transmit FIFO, as setting TEN clears the transmit FIFO. TCDCNT should also be checked by user software and cleared if a collision occurred on a prior transmission.

To enable the receiver, GREN (RSTAT.1) is set. After GREN is set, the GSC begins to look for a valid BOF. After detecting a valid BOF the GSC attempts to match the received address byte(s) against the address match registers. When a match occurs the frame is loaded into the GSC. Due to the CRC strip hardware, there is a 40 or 24 bit time delay following the BOF until the first data byte is loaded into RFIFO if the 32 or 16 bit CRC is chosen. If the end of frame is detected before data is loaded into the receive FIFO, the receiver ignores that frame.

If the receiver detects a collision during reception in CSMA/CD mode and if any bytes have been loaded into the receive FIFO, the RCABT flag is set. The GSC hardware then halts reception and resets GREN. The user software needs to filter any collision fragment data which may have been received. If the collision occurred prior to the data being loaded into RFIFO the CPU is not notified and the receiver is left enabled. At the end of a reception the RDN bit is set and GREN is cleared. In HABEN mode this causes an acknowledgement to be transmitted if the frame did not have a broadcast or multi-cast address. The user software can enable the interrupt for RDN to determine when a frame is completed.

In DMA mode the interrupts are generated by the internal "transmit/receive done" (TDN,RDN) conditions. When the CPU responds to TDN or RDN, checks are performed to see if the transmit underrun error has occurred. The underrun condition is only checked when using the DMA channels.

Upon power up the CPU mode is initialized. General DMA control is covered in Section 4.0. DMA control of the GSC is covered in Section 3.5.4. If DMA is to be used for serving the GSC, it must be configured into the serial channel demand mode and the DMA bit in TSTAT has to be set.

3.6.3 COLLISIONS AND BACKOFF

The actions that are taken by the GSC if a collision occurs while transmitting depend on where the collision occurs. If a collision occurs in CSMA/CD mode following the preamble and BOF flag, the TCDT flag is set and the transmit hardware completes a jam. When this type of collision occurs, there will be no automatic retry at transmission. After the jam, control is returned to the CPU and user software must then initiate whatever actions are necessary for a proper recovery. The possibility that data might have been loaded into or from the GSC deserves special consideration. If these fragments of a message have been passed on to other devices, user software may have to perform some extensive error handling or notification. Before starting a new message, the transmit and receive FIFOs will need to be cleared. If DMA servicing is being used the pointers must also be reinitialized. It should be noted that a collision should never occur after the BOF flag in a well designed system, since the system slot time will likely be less than the preamble length. The occurrence of such a situation is normally due to a station on the link that is not adhering to proper CSMA/CD protocol or is not using the same timings as the rest of the network.

A collision occurring during the preamble or BOF flag is the normal type of collision that is expected. When this type of collision occurs the GSC automatically handles the retransmission attempts for as many as eight tries. If on the eighth attempt a collision occurs,

the transmitter is disabled, although the jam and back-off are performed. If enabled, the CPU is then interrupted. The user software should then determine what action to take. The possibilities range from just reporting the error and aborting transmission to reinitializing the serial channel registers and attempt retransmission.

If less than eight attempts are desired TCDCNT can be loaded with some value which will reduce the number of collisions possible before TCDCNT overflows. The value loaded should consist of all 1s as the least significant bits, e.g. 7, 0FH, 3FH. A solid block of 1s is suggested because TCDCNT is used as a mask when generating the random slot number assignment. The TCDCNT register operates by shifting the contents one bit position to the left as each collision is detected. As each shift occurs a 1 is loaded into the LSB. When TCDCNT overflows, GSC operation stops and the CPU is notified by the setting of the TCDT bit which can flag an interrupt.

The amount of time that the GSC has before it must be ready to retransmit after a collision is determined by the mode which is selected. The mode is determined M0 (GMOD.5) and M1 (GMOD.6). If M0 and M1 equal 0,0 (normal backoff) then the minimum period before retransmission will be either the interframe space or the backoff period, whichever is longer. If M0 and M1 equal 1,1 (alternate backoff) then the minimum period before retransmission will be the interframe space plus the backoff period. Both of these are shown in Figure 3.4. Alternate backoff must be enabled if using deterministic resolution. If the GSC is not ready to retransmit by the time its assigned slot becomes available, the slot time is lost and the station must wait until the collision resolution time period has passed.

Instead of waiting for the collision resolution to pass, the transmission could be aborted. The decision to abort is usually dependent on the number of stations on the link and how many collisions have already occurred. The number of collisions can be obtained by examining the register, TCDCNT. The abort is normally implemented by clearing TEN. The new transmission begins by setting TEN and loading TFIFO. The minimum amount of time available to initiate a retransmission would be one interframe space period after the line is sensed as being idle.

As the number of stations approach 256 the probability of a successful transmission decreases rapidly. If there are more than 256 stations involved in the collision there would be no resolution since at least two of the stations will always have the same backoff interval selected.

All the stations monitor the link as long as that station is active, even if not attempting to transmit. This is to ensure that each station always defers the minimum amount of time before attempting a transmission and so that addresses are recognized. However, the collision detect circuitry operates slightly differently.

In normal back-off mode, a transmitting station always monitors the link while transmitting. If a collision is detected one or more of the transmitting stations apply the jam signal and all transmitting stations enter the back-off algorithm. The receiving stations also constantly monitor for a collision but do not take part in the resolution phase. This allows a station to try to transmit in the middle of a resolution period. This in turn may or may not cause another collision. If the new station trying to transmit on the link does so during an unused slot time then there will probably not be a collision. If trying to transmit during a used slot time, then there will probably be a collision. The actions the receiver does take when detecting a collision is to just stop receiving data if data has not been loaded into RFIFO or to stop reception, clear receiver enable (REN) and set the receiver abort flag (RCABT - RSTAT.6).

If deterministic resolution is used, the transmitting stations go through pretty much the same process as in normal back-off, except that the slots are predetermined. All the receivers go through the back-off algorithm and may only transmit during their assigned slot.

3.6.4 SUCCESSFUL ENDING OF TRANSMISSIONS AND RECEPTIONS

In both CSMA/CD and SDLC modes, the TDN bit is set and TEN cleared at the end of a successful transmission. The end of the transmission occurs when the TFIFO is empty and the last byte has been transmitted. In CSMA/CD the user should clear the TCDCNT register after successful transmission.

At the end of a successful reception, the RDN bit is set and GREN is cleared. The end of reception occurs when the EOF flag is detected by the GSC hardware.

3.7 Register Descriptions

ADR0,1,2,3 (95H, 0A5H, 0B5H, 0C5H) - Address Match Registers 0,1,2,3 - Contains the address match values which determines which data will be accepted as valid. In 8 bit addressing mode, a match with any of the four registers will trigger acceptance. In 16 bit addressing mode a match with ADR1:ADR0 or ADR3:ADR2 will be accepted. Addressing mode is determined in GMOD (AL).

AMSK0,1 (0D5H, 0E5H) - Address Match Mask 0,1 - Identifies which bits in ADR0,1 are "don't care" bits. Writing a one to a bit in AMSK0,1 masks out that corresponding bit in ADDR0,1.

BAUD (94H) - GSC Baud Rate Generator - Contains the value of the programmable baud rate. The data rate will equal (frequency of the oscillator)/((BAUD + 1) × (8)). Writing to BAUD actually stores the value in a reload register. The reload register contents are copied into the BAUD register when the Baud register decrements to 00H. Reading BAUD yields the current timer value. A read during GSC operation will give a value that may not be current because the timer could decrement between the time it is read by the CPU and by the time the value is loaded into its destination.

BKOFF (0C4H) - Backoff Timer - The backoff timer is an eight bit count-down timer with a clock period equal to one slot time. The backoff time is used in the CSMA/CD collision resolution algorithm. The user software may read the timer but the value may be invalid as the timer is clocked asynchronously to the CPU. Writing to 0C4H will have no effect.

GMOD (84H)

7	6	5	4	3	2	1	0
XTCLK	M1	M0	AL	CT	PL1	PL0	PR

Figure 3.14. GMOD

GMOD.0 (PR) - Protocol - If set, SDLC protocols with NRZI encoding and SDLC flags are used. If cleared, CSMA/CD link access with Manchester encoding is used. The user software is responsible for setting or clearing this flag.

GMOD.1,2 (PL0,1) - Preamble length

PL1	PL0	LENGTH (BITS)
0	0	0
0	1	8
1	0	32
1	1	64

The length includes the two bit Begin Of Frame (BOF) flag in CSMA/CD but does not include the SDLC flag. In SDLC mode, the BOF is an SDLC flag, otherwise it is two consecutive ones. Zero length is not compatible in CSMA/CD mode. The user software is responsible for setting or clearing these bits.

GMOD.3 (CT) - CRC Type - If set, 32 bit AUTODIN-II-32 is used. If cleared, 16 bit CRC-CCITT is used. The user software is responsible for setting or clearing this flag.

GMOD.4 (AL) - Address Length - If set, 16 bit addressing is used. If cleared, 8 bit addressing is used. In 8 bit mode a match with any of the 4 address registers will be accepted (ADR0, ADR1, ADR2, ADR3). "Don't Care" bits may be masked in ADR0 and ADR1 with AMSK0 and AMSK1. In 16 bit mode, addresses are matched against "ADR1:ADR0" or "ADR3:ADR2". Again, "Don't Care" bits in ADR1:ADR0 can be masked in AMSK1:AMSK0. A received address of all ones will always be recognized in any mode. The user software is responsible for setting or clearing this flag.

GMOD.5,6 (M0,M1) - Mode Select - Two test modes, an optional "alternate backoff" mode, or normal backoff can be enabled with these two bits. The user software is responsible for setting or clearing the mode bits.

M1	M0	Mode
0	0	Normal
0	1	Raw Transmit
1	0	Raw Receive
1	1	Alternate Backoff

In raw receive mode, the receiver operates as normal except that all the bytes following the BOF are loaded into the receive FIFO, including the CRC. The transmitter operates as normal.

In raw transmit mode the transmit output is internally connected to the receiver input. The internal connection is not at the actual port pin, but inside the port latch. All data transmitted is done without a preamble, flag or zero bit insertion, and without appending a CRC. The receiver operates as normal. Zero bit deletion is performed.

In alternate backoff mode the standard backoff process is modified so the the backoff is delayed until the end of the IFS. This should help to prevent collisions constantly happening because the IFS time is usually larger than the slot time.

GMOD.7 (XTCLK) - External Transmit Clock - If set an external 1X clock is used for the transmitter. If cleared the internal baud rate generator provides the transmit clock. The input clock is applied to P1.3 ($\overline{T \times C}$). The user software is responsible for setting or clearing this flag. External receive clock is enabled by setting PCON.3.

IFS (0A4H) - Interframe Spacing - Determines the number of bit times separating transmitted frames in CSMA/CD and SDLC. A bit time is equal to 1/baud rate. Only even interframe space periods can be used. The number written into this register is divided by two and loaded in the most significant seven bits. Complete interframe space is obtained by counting this seven bit number down to zero twice. A user software read of this register will give a value where the seven most significant bits gives the current count value and the least significant bit shows a one for the first count-down and a zero for the second count. The value read may not be valid as the timer is clocked in periods not necessarily associated with the CPU read of IFS. Loading this register with zero results in 256 bit times.

MYSLOT (0F5H) - Slot Address Register

7	6	5	4	3	2	1	0
DCJ	DCR	SA5	SA4	SA3	SA2	SA1	SA0
SAn = SLOT ADDRESS (BITS 5 – 0)							

Figure 3.15. MYSLOT

MYSLOT.0, 1, 2, 3, 4, 5 - Slot Address - The six address bits choose 1 of 64 slot addresses. Address 63 has the highest priority and address 1 has the lowest. A value of zero will prevent a station from transmitting during the collision resolution period by waiting until all the possible slot times have elapsed. The user software normally initializes this address in the operating software.

MYSLOT.6 (DCR) - Deterministic Collision Resolution Algorithm - When set, the alternate collision resolution algorithm is selected. Retriggering of the IFS on reappearance of the carrier is also disabled. When using this feature Alternate Backoff Mode must be selected and several other registers must be initialized. User software must initialize TCDCNT with the maximum number of slots that are most appropriate for a particular application. The PRBS register must be set to all ones. This disables the PRBS by freezing it's contents at 0FFH. The backoff timer is used to count down the number of slots based on the slot timer value setting the period of one slot. The user software is responsible for setting or clearing this flag.

MYSLOT.7 (DCJ) - D.C. Jam - When set selects D.C. type jam, when clear, selects A.C. type jam. The user software is responsible for setting or clearing this flag.

PCON (087H)

7	6	5	4	3	2	1	0
SMOD	ARB	REQ	GAREN	XRCLK	GFIEN	PD	IDL

PCON contains bits for power control, LSC control, DMA control, and GSC control. The bits used for the GSC are PCON.2, PCON.3, and PCON.4.

PCON.2 (GFIEN) - GSC Flag Idle Enable - Setting GFIEN to a 1 caused idle flags to be generated between transmitted frames in SDLC mode. SDLC idle flags consist of 01111110 flags creating the sequence 01111110011111110 . . . . . 011111110. A possible side effect of enabling GFIEN is that the maximum possible latency from writing to TFIFO until the first bit is transmitted increased from approximately 2 bit-times to around 8 bit-times. GFIEN has no effect with CSMA/CD.

PCON.3 (XRCLK) - GSC External Receive Clock Enable - Writing a 1 to XRCLK enables an external clock to be applied to pin 5 (Port 1.4). The external clock is used to determine when bits are loaded into the receiver.

PCON.4 (GAREN) - GSC Auxiliary Receiver Enable Bit - This bit needs to be set to a 1 to enable the reception of back-to-back SDLC frames. A back-to-back SDLC frame is when the EOF and BOF is shared between two sequential frames intended for the same station on the link. If GAREN contains a 0 then the receiver will be disabled upon reception of the EOF and by the time user software re-enables the receiver the first bit(s) may have already passed, in the case of back-to-back frames. Setting GAREN to a 1, prevents the receiver from being disabled by the EOF but GREN will be cleared and can be checked by user software to determine that an EOF has been received. GAREN has no effect if the GSC is in CSMA/CD mode.

PRBS (0E4H) - Pseudo-Random Binary Sequence - This register contains a pseudo-random number to be used in the CSMA/CD backoff algorithm. The number is generated by using a feedback shift register clocked by the CPU phase clocks. Writing all ones to the PRBS will freeze the value at all ones. Writing any other value to it will restart the PRBS generator. The PRBS is initialized to all zero's during RESET. A read of location 0E4H will not necessarily give the seed used in the backoff algorithm because the PRBS counters are clocked by internal CPU phase clocks. This means the contents of the PRBS may have been altered between the time when the seed was generated and before a READ has been internally executed.

RFIFO (0F4H) - Receive FIFO - RFIFO is a 3 byte buffer that is loaded each time the GSC receiver has a byte of data. Associated with RFIFO is a pointer that is automatically updated with each read of the FIFO. A read of RFIFO fetches the oldest data in the FIFO.

RSTAT (0E8H) - Receive Status Register

7	6	5	4	3	2	1	0
OR	RCABT	AE	CRCE	RDN	RFNE	GREN	HABEN

Figure 3.16. RSTAT

RSTAT.0 (HABEN) - Hardware Based Acknowledge Enable - If set, enables the hardware based acknowledge feature. The user software is responsible for setting or clearing this flag.

RSTAT.1 (GREN) - Receiver Enable - When set, the receiver is enabled to accept incoming frames. The user must clear RFIFO with software before enabling the receiver. RFIFO is cleared by reading the contents of RFIFO until RFNE = 0. After each read of RFIFO, it takes one machine cycle for the status of RFNE to be updated. Setting GREN also clears RDN, CRCE, AE, and RCABT. GREN is cleared by hardware at the end of a reception or if any receive errors are detected. The user software is responsible for setting this flag and the GSC or user software can clear it. The status of GREN has no effect on whether the receiver detects a collision in CSMA/CD mode as the receiver input circuitry always monitors the receive pin.

RSTAT.2 (RFNE) - Receive FIFO Not Empty - If set, indicates that the receive FIFO contains data. The receive FIFO is a three byte buffer into which the receive data is loaded. A CPU read of the FIFO retrieves the oldest data and automatically updates the FIFO pointers. Setting GREN to a one will clear the receive FIFO. The status of this flag is controlled by the GSC. It is cleared if user empties receive FIFO.

RSTAT.3 (RDN) - Receive Done - If set, indicates the successful completion of a receiver operation. Will not be set if a CRC, alignment, abort, or FIFO overrun error occurred. The status of this flag is controlled by the GSC.

RSTAT.4 (CRCE) - CRC Error - If set, indicates that a properly aligned frame was received with a mismatched CRC. The status of this flag is controlled by the GSC.

RSTAT.5 (AE) - Alignment Error - In CSMA/CD mode, AE is set if the receiver shift register (an internal serial-to-parallel converter) is not full and the CRC is bad when an EOF is detected. In CSMA/CD the EOF is a line idle condition (see LNI) for two bit times. If the CRC is correct while in CSMA/CD mode, AE is not set and any mis-alignment is assumed to be caused by dribble bits as the line went idle. In SDLC mode, AE is set if a non-byte-aligned flag is received. CRCE may also be set. The setting of this flag is controlled by the GSC.

RSTAT.6 (RCABT) - Receiver Collision/Abort Detect - If set, indicates that a collision was detected after data had been loaded into the receive FIFO in CSMA/CD mode. In SDLC mode, RCABT indicates that 7 consecutive ones were detected prior to the end flag but after data has been loaded into the receive FIFO. AE may also be set. The setting of this flag is controlled by the GSC.

RSTAT.7 (OVR) - Overrun - If set, indicates that the receive FIFO was full and new shift register data was written into it. AE and/or CRCE may also be set. The setting of this flag is controlled by the GSC and it is cleared by user software.

SLOTTM (0BH) - Slot Time - Determines the length of the slot time used in CSMA/CD. A slot time equals (SLOTTM) $\times$ (1 / baud rate). A read of SLOTTM will give the value of the slot time timer but the value may be invalid as the timer is clocked asynchronously to the CPU. Loading SLOTTM with 0 results in 256 bit times.

TCDCNT (0D4H) - Transmit Collision Detect Count - Contains the number of collisions that have occurred if probabilistic CSMA/CD is used. The user software must clear this register before transmitting a new frame so that the GSC backoff hardware can accurately distinguish a new frame from a retransmit attempt.

In deterministic backoff mode, TCDCNT is used to hold the maximum number of slots.

TFIFO (85H) - GSC Transmit FIFO - TFIFO is a 3 byte buffer with an associated pointer that is automatically updated for each write by user software. Writing a byte to TFIFO loads the data into the next available location in the transmit FIFO. Setting TEN clears the transmit FIFO so the transmit FIFO should not be written to prior to setting TEN. If TEN is already set transmission begins as soon as data is written to TFIFO.

TSTAT (0D8) - Transmit Status Register

7	6	5	4	3	2	1	0
LNI	NOACK	UR	TCDT	TDN	TFNF	TEN	DMA

Figure 3.17. TSTAT

TSTAT.0 (DMA) - DMA Select - If set, indicates that DMA channels are used to service the GSC FIFO's and GSC interrupts occur on TDN and RDN, and also enables UR to become set. If cleared, indicates that the GSC is operating in its normal mode and interrupts occur on TFNF and RFNE. For more information on DMA servicing please refer to the DMA section on DMA serial demand mode (4.2.2.3). The user software is responsible for setting or clearing this flag.

TSTAT.1 (TEN) - Transmit Enable - When set causes TDN, UR, TCDT, and NOACK flag to be reset and the TFIFO cleared. The transmitter will clear TEN after a successful transmission, a collision during the data, CRC, or end flag. The user software is responsible for setting but the GSC or user software may clear this flag. If cleared during a transmission the GSC transmit pin goes to a steady state high level. This is the method used to send an abort character in SDLC. Also $\overline{DEN}$ is forced to a high level. The end of transmission occurs whenever the TFIFO is emptied.

TSTAT.2 (TFNF) - Transmit FIFO not full - When set, indicates that new data may be written into the transmit FIFO. The transmit FIFO is a three byte buffer that loads the transmit shift register with data. The status of this flag is controlled by the GSC.

TSTAT.3 (TDN) - Transmit Done - When set, indicates the successful completion of a frame transmission. If HABEN is set, TDN will not be set until the end of the IFS following the transmitted message, so that the acknowledge can be checked. If an acknowledge is expected and not received, TDN is not set. An acknowledge is not expected following a broadcast or multi-cast packet. The status of this flag is controlled by the GSC.

TSTAT.4 (TCDT) - Transmit Collision Detect - If set, indicates that the transmitter halted due to a collision. It is set if a collision occurs during the data or CRC or if there are more than eight collisions. The status of this flag is controlled by the GSC.

TSTAT.5 (UR) - Underrun - If set, indicates that in DMA mode the last bit was shifted out of the transmit register and that the DMA byte count did not equal zero. When an underrun occurs, the transmitter halts without sending the CRC or the end flag. The status of this flag is controlled by the GSC.

TSTAT.6 (NOACK) - No Acknowledge - If set, indicates that no acknowledge was received for the previous frame. Will be set only if HABEN is set and no acknowledge is received prior to the end of the IFS. NOACK is not set following a broadcast or a multicast packet. The status of this flag is controlled by the GSC.

TSTAT.7 (LNI) - Line Idle - If set, indicates the receive line is idle. In SDLC protocol it is set if 15 consecutive ones are received. In CSMA/CD protocol, line idle is set if GR×D remains high for approximately 1.6 bit times. LNI is cleared after a transition on GR×D. The status of this flag is controlled by the GSC.

3.8 Serial Backplane vs. Network Environment

The C152 GSC port is intended to fulfill the needs of both serial backplane environment and the serial communication network environment. The serial backplane is where typically, only processor to processor communications take place within a self contained box. The communication usually only encompasses those items which are necessary to accomplish the dedicated task for the box. In these types of applications there may not be a need for line drivers as the distance between the transmitter and receiver is relatively short. The network environment; however, usually requires transmission of data over large distances and requires drivers and/or repeaters to ensure the data is received on both ends.

10

4.0 DMA Operation

The C152 contains DMA (Direct Memory Accessing) logic to perform high speed data transfers between any two of

Internal Data RAM
Internal SFRs
External Data RAM

If external RAM is involved, the Port 2 and Port 0 pins are used as the address/data bus, and $\overline{RD}$ and $\overline{WR}$ signals are generated as required.

Hardware is also implemented to generate a Hold Request signal and await a Hold Acknowledge response before commencing a DMA that involves external RAM.

Alternatively, the Hold/Hold Acknowledge hardware can be programmed to accept a Hold Request signal from an external device and generate a Hold Acknowledge signal in response, to indicate to the requesting device that the C152 will not commence a DMA to or from external RAM while the Hold Request is active.

4.1 DMA with the 80C152

The C152 contains two identical general purpose 8-bit DMA channels with 16-bit addressability: DMA0 and DMA1. DMA transfers can be executed by either channel independent of the other, but only by one channel at a time. During the time that a DMA transfer is being executed, program execution is suspended. A DMA transfer takes one machine cycle (12 oscillator

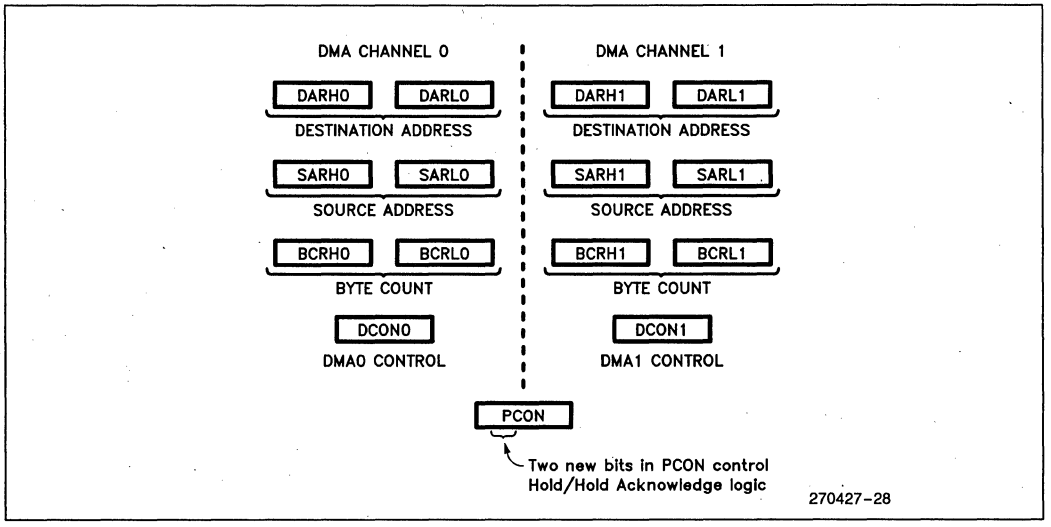


Figure 4.1. DMA Registers

periods) per byte transferred, except when the destination and source are both in External Data RAM. In that case the transfer takes two machine cycles per byte. The term DMA Cycle will be used to mean the transfer of a single data byte, whether it takes 1 or 2 machine cycles.

Associated with each channel are seven SFRs, shown in Figure 4.1. SARLn and SARHn holds the low and high bytes of the source address. Taken together they form a 16-bit Source Address Register. DARLn and DARHn hold the low and high bytes of the destination address, and together form the Destination Address Register. BCRLn and BCRHn hold the low and high bytes of the number of bytes to be transferred, and together form the Byte Count Register. DCONn contains control and flag bits.

Two bits in DCONn are used to specify the physical destination of the data transfer. These bits are DAS (Destination Address Space) and IDA (Increment Destination Address). If DAS = 0, the destination is in data memory external to the C152. If DAS = 1, the destination is internal to the C152. If DAS = 1 and IDA = 0, the internal destination is a Special Function Register (SFR). If DAS = 1 and IDA = 1, the internal destination is in the 256-byte data RAM.

In any case, if IDA = 1, the destination address is automatically incremented after each byte transfer. If IDA = 0, it is not.

Two other bits in DCONn specify the physical source of the data to be transferred. These are SAS (Source Address Space) and ISA (Increment Source Address). If SAS = 0, the source is in data memory external to the C152. If SAS = 1, the source is internal. If SAS = 1 and ISA = 0, the internal source is an SFR. If SAS = 1 and ISA = 1, the internal source is in the 256-byte data RAM.

In any case, if ISA = 1, the source address is automatically incremented after each byte transfer. If ISA = 0, it is not.

The functions of these four control bits are summarized below:

DAS	IDA	Destination	Auto-Increment
0	0	External RAM	no
0	1	External RAM	yes
1	0	SFR	no
1	1	Internal RAM	yes
SAS	**ISA**	**Source**	**Auto-Increment**
0	0	External RAM	no
0	1	External RAM	yes
1	0	SFR	no
1	1	Internal RAM	yes

There are four modes in which the DMA channel can operate. These are selected by the bits DM and TM (Demand Mode and Transfer Mode) in DCONn:

DM	TM	Operating Mode
0	0	Alternate Cycles Mode
0	1	Burst Mode
1	0	Serial Port Demand Mode
1	1	External Demand Mode

The operating modes are described below.

4.1.1 ALTERNATE CYCLE MODE

In Alternate Cycles Mode the DMA is initiated by setting the GO bit in DCONn. Following the instruction that set the GO bit, one more instruction is executed, and then the first data byte is transferred from the source address to the destination address. Then another instruction is executed, and then another byte of data is transferred, and so on in this manner.

Each time a data byte is transferred, BCRn (Byte Count Register for DMA Channel n) is decremented. When it reaches 0000H, on-chip hardware clears the GO bit and sets the DONE bit, and the DMA ceases. The DONE bit flags an interrupt.

4.1.2 BURST MODE

Burst Mode differs from Alternate Cycles mode only in that once the data transfer has begun, program execution is entirely suspended until BCRn reaches 0000H, indicating that all data bytes that were to be transferred have been transferred. The interrupt control hardware remains active during the DMA, so interrupt flags may get set, but since program execution is suspended, the interrupts will not be serviced while the DMA is in progress.

4.1.3 SERIAL PORT DEMAND MODE

In this mode the DMA can be used to service the Local Serial Channel (LSC) or the Global Serial Channel (GSC).

In Serial Port Demand Mode the DMA is initiated by any of the following conditions, if the GO bit is set:

```
Source Address = SBUF       .AND.  RI = 1
Destination Address = SBUF  .AND.  TI = 1
Source Address = RFIFO      .AND.  RFNE = 1
Destination Address = TFIFO .AND.  TFNF = 1
```

Each time one of the above conditions is met, one DMA Cycle is executed; that is, one data byte is transferred from the source address to the destination address. On-chip hardware then clears the flag (RI, TI, RFNE, or TFNF) that initiated the DMA, and decrements BCRn. Note that since the flag that initiated the DMA is cleared, it will not generate an interrupt unless DMA servicing is held off or the byte count equals 0. DMA servicing may be held off when alternate cycle is being used or by the status of the HOLD/HLDA logic. In these situations the interrupt for the LSC may occur before the DMA can clear the RI or TI flag. This is because the LSC is serviced according to the status of RI and TI, whether or not the DMA channels are being used for the transferring of data. The GSC does not use RFNE or TFNF flags when using the DMA channels so these do not need to be disabled. When using the DMA channels to service the LSC it is recommended that the interrupts (RI and TI) be disabled. If the decremented BCRn is 0000H, on-chip hardware then clears the GO bit and sets the DONE bit. The DONE bit flags an interrupt.

4.1.4 EXTERNAL DEMAND MODE

In External Demand Mode the DMA is initiated by one of the External Interrupt pins, provided the GO bit is set. $\overline{\text{INT0}}$ initiates a Channel 0 DMA, and $\overline{\text{INT1}}$ initiates a Channel 1 DMA.

If the external interrupt is configured to be transition-activated, then each 1-to-0 transition at the interrupt pin sets the corresponding external interrupt flag, and generates one DMA Cycle. Then, BCRn is decremented. No more DMA Cycles take place until another 1-to-0 transition is seen at the external interrupt pin. If the decremented BCRn = 0000H, on-chip hardware clears the GO bit and sets the DONE bit. If the external interrupt is enabled, it will be serviced.

If the external interrupt is configured to be level-activated, then DMA Cycles commence when the interrupt pin is pulled low, and continue for as long as the pin is held low and BCRn is not 0000H. If BCRn reaches 0 while the interrupt pin is still low, the GO bit is cleared, the DONE bit is set, and the DMA ceases. If the external interrupt is enabled, it will be serviced.

If the interrupt pin is pulled up before BCRn reaches 0000H, then the DMA ceases, but the GO bit is still 1 and the DONE bit is still 0. An external interrupt is not generated in this case, since in level-activated mode, pulling the pin to a logical 1 clears the interrupt flag. If the interrupt pin is then pulled low again, DMA transfers will continue from where they were previously stopped.

The timing for the DMA Cycle in the transition-activated mode, or for the first DMA Cycle in the level-activated mode is as follows: If the 1-to-0 transition is

detected before the final machine cycle of the instruction in progress, then the DMA commences as soon as the instruction in progress is completed. Otherwise, one more instruction will be executed before the DMA starts. No instruction is executed during any DMA Cycle.

4.2 Timing Diagrams

Timing diagrams for single-byte DMA transfers are shown in Figures 4.2 through 4.5 for four kinds of DMA Cycles: internal memory to internal memory, internal memory to external memory, external memory to internal memory, and external memory to external memory. In each case we assume the C152 is executing out of external program memory. If the C152 is executing out of internal program memory, then $\overline{PSEN}$ is inactive, and the Port 0 and Port 2 pins emit P0 and P2 SFR data. If External Data Memory is involved, the Port 0 and Port 2 pins are used as the address/data bus, and $\overline{RD}$ and/or $\overline{WR}$ signals are generated as needed, in the same manner as in the execution of a MOVX @DPTR instruction.

4.3 Hold/Hold Acknowledge

Two operating modes of Hold/Hold Acknowledge logic are available, and either or neither may be invoked by software. In one mode, the C152 generates a Hold Request signal and awaits a Hold Acknowledge response before commencing a DMA that involves external RAM. This is called the Requester Mode.

In the other mode, the C152 accepts a Hold Request signal from an external device and generates a Hold Acknowledge signal in response, to indicate to the requesting device that the C152 will not commence a DMA to or from external RAM while the Hold Request is active. This is called the Arbiter mode.

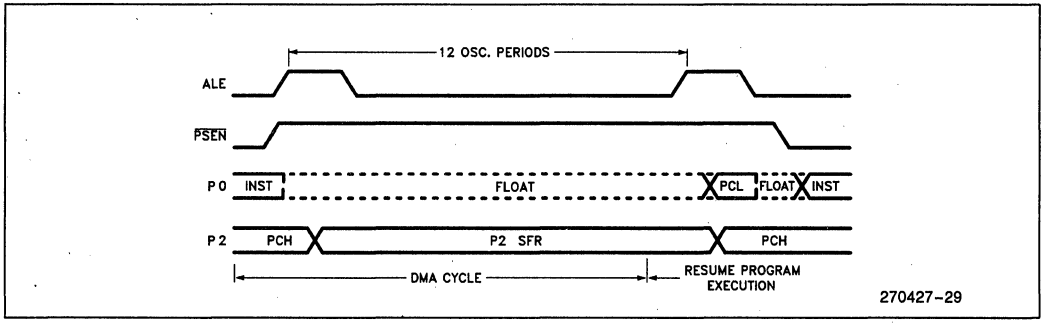


Figure 4.2. DMA Transfer from Internal Memory to Internal Memory

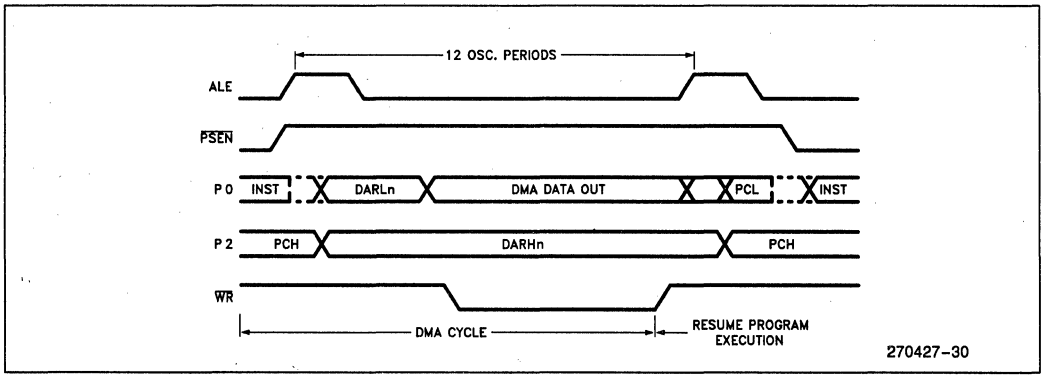


Figure 4.3. DMA Transfer from Internal Memory to External Memory

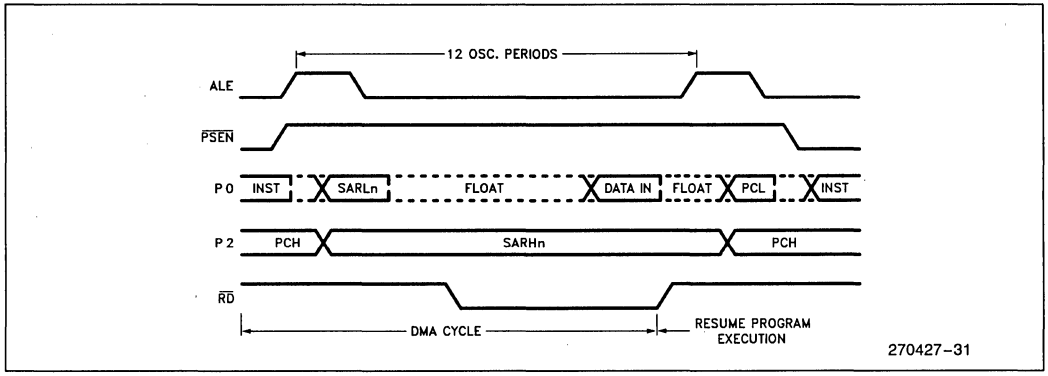


Figure 4.4. DMA Transfer from External Memory to Internal Memory

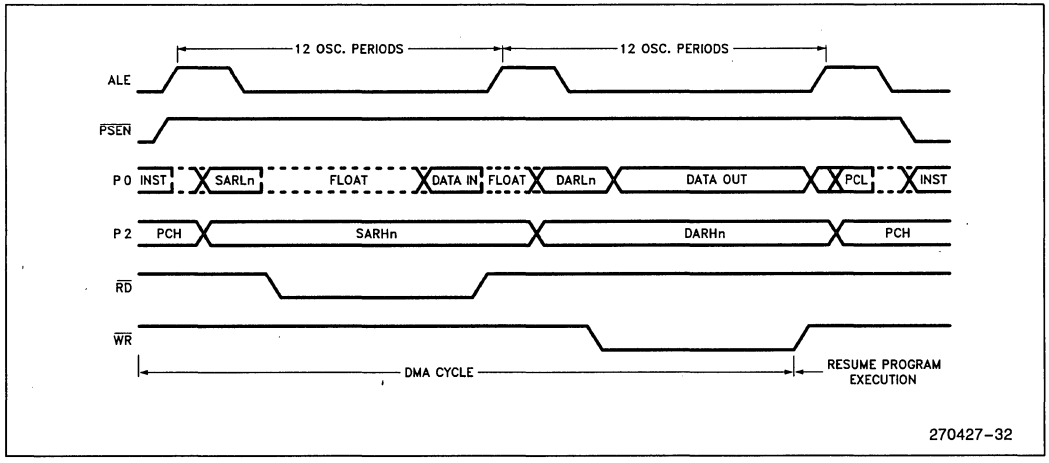


Figure 4.5. DMA Transfer from External Memory to External Memory

4.3.1 REQUESTER MODE

The Requester Mode is selected by setting the control bit REQ, which resides in PCON. In that mode, when the C152 wants to do a DMA to External Data Memory, it first generates a Hold Request signal, $\overline{HLD}$, and waits for a Hold Acknowledge signal, $\overline{HLDA}$, before commencing the DMA operation. Note that program execution continues while $\overline{HLDA}$ is awaited. The DMA is not begun until a logical 0 is detected at the $\overline{HLDA}$ pin. Then, once the DMA has begun, it goes to completion regardless of the logic level at $\overline{HLDA}$.

The protocol is activated only for DMAs (not for program fetches or MOVX operations), and only for DMAs to or from External Data Memory. If the data destination and source are both internal to the C152, the $\overline{HLD}$/$\overline{HLDA}$ protocol is not used.

The $\overline{HLD}$ output is an alternate function of port pin P1.5, and the $\overline{HLDA}$ input is an alternate function of port pin P1.6.

4.3.2 ARBITER MODE

For DMAs that are to be driven by some device other than the C152, a different version of the Hold/Hold Acknowledge protocol is available. In this version, the device which is to drive the DMA sends a Hold Request signal, $\overline{HLD}$, to the C152. If the C152 is currently performing a DMA to or from External Data Memory, it will complete this DMA before responding to the Hold Request. When the C152 responds to the Hold Request, it does so by activating a Hold Acknowledge signal, $\overline{HLDA}$. This indicates that the C152 will not commence a new DMA to or from External Data Memory while $\overline{HLD}$ remains active.

Note that in the Arbiter Mode the C152 does not suspend program execution at all, even if it is executing from external program memory. It does not surrender use of its own bus.

The Hold Request input, $\overline{HLD}$, is at P1.5. The Hold Acknowledge output, $\overline{HLDA}$, is at P1.6. This

version of the Hold/Hold Acknowledge feature is selected by setting the control bit ARB in PCON.

The functions of the ARB and REQ bits in PCON, then, are

ARB	REQ	Hold/Hold Acknowledge Logic
0	0	Disabled
0	1	C152 generates $\overline{HLD}$, detects $\overline{HLDA}$
1	0	C152 detects $\overline{HLD}$, generates $\overline{HLDA}$
1	1	Invalid

4.3.3 USING THE HOLD/HOLD ACKNOWLEDGE

The $\overline{HOLD}/\overline{HOLDA}$ logic only affects DMA operation with external RAM and doesn't affect other operations with external RAM, such as MOVX instruction.

Figure 4.6 shows a system in which two 83C152s are sharing a global RAM. In this system, both CPUs are executing from internal ROM. Neither CPU uses the bus except to access the shared RAM, and such accesses are done only through DMA operations, not by MOVX instructions.

One CPU is programmed to be the Arbiter and the other, to be the Requester. The ALE Switch selects which CPU's ALE signal will be directed to the address latch. The Arbiter's ALE is selected if $\overline{HLDA}$ is high, and the Requester's ALE is selected if $\overline{HLDA}$ is low.

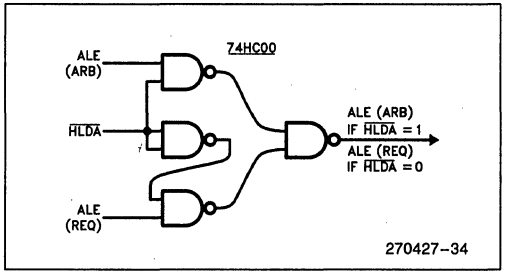


Figure 4.7. ALE Switch Select

The ALE Switch logic can be implemented by a single 74HC00, as shown in Figure 4.7.

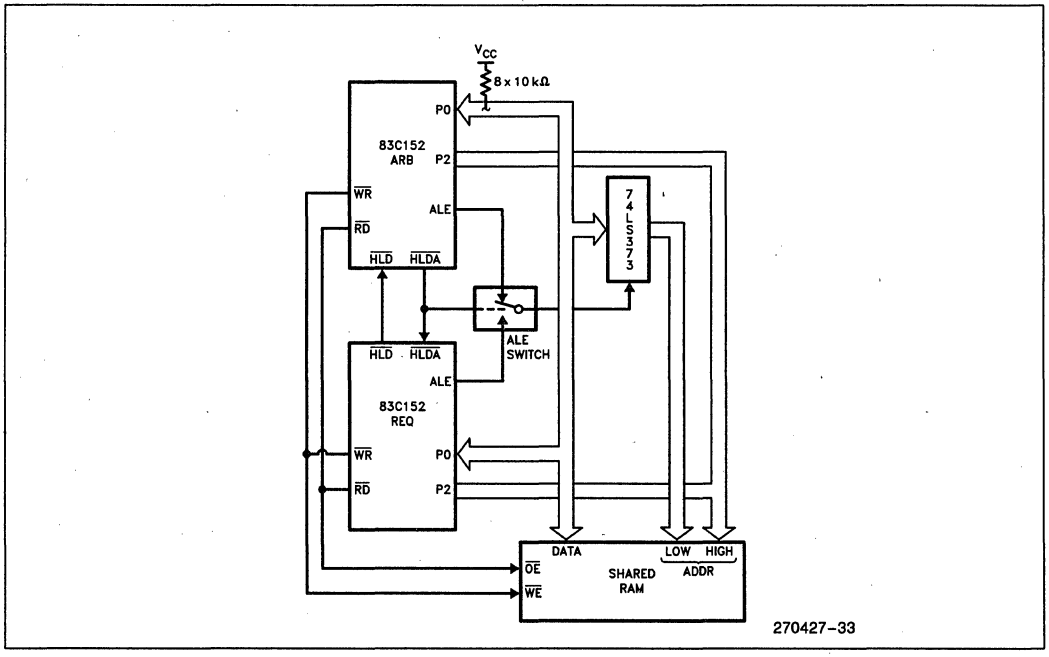


Figure 4.6. Two 83C152s Sharing External RAM

4.3.4 INTERNAL LOGIC OF THE ARBITER

The internal logic of the arbiter is shown in Figure 4.8. In operation an input low at $\overline{HLD}$ sets Q2 if the arbiter's internal signal DMXRQ is low. DMXRQ is the arbiter's "DMA to XRAM Request". Setting Q2 activates $\overline{HLDA}$ through Q3. Q2 being set also disables any DMAs to XRAM that the arbiter might decide to do during the requester's DMA.

Figure 4.9 shows the minimum response time, 4 to 7 CPU oscillator periods, between a transition at the $\overline{HLD}$ input and the response at $\overline{HLDA}$.

When the arbiter wants to DMA the XRAM, it first activates DMXRQ. This signal prevents Q2 from being set if it is not already set. An output low from Q2 enables the arbiter to carry out its DMA to XRAM, and maintains an output high at $\overline{HLDA}$. When the arbiter completes its DMA, the signal DMXRQ goes to O, which enables Q2 to accept signals from the $\overline{HLD}$ input again.

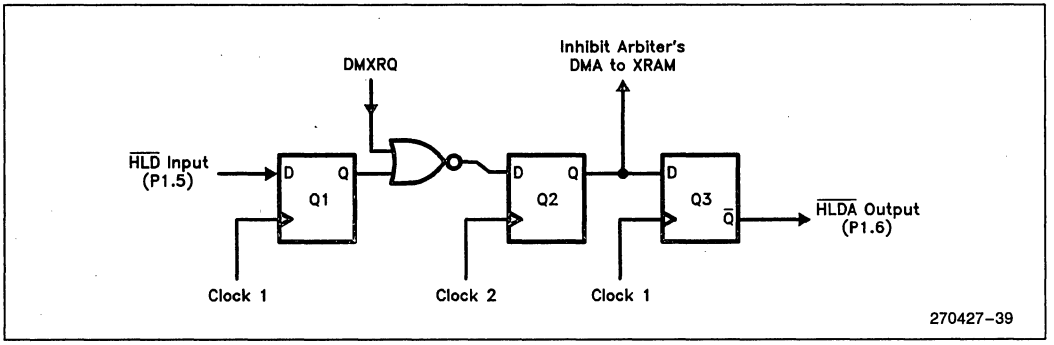


Figure 4.8. Internal Logic of the Arbiter

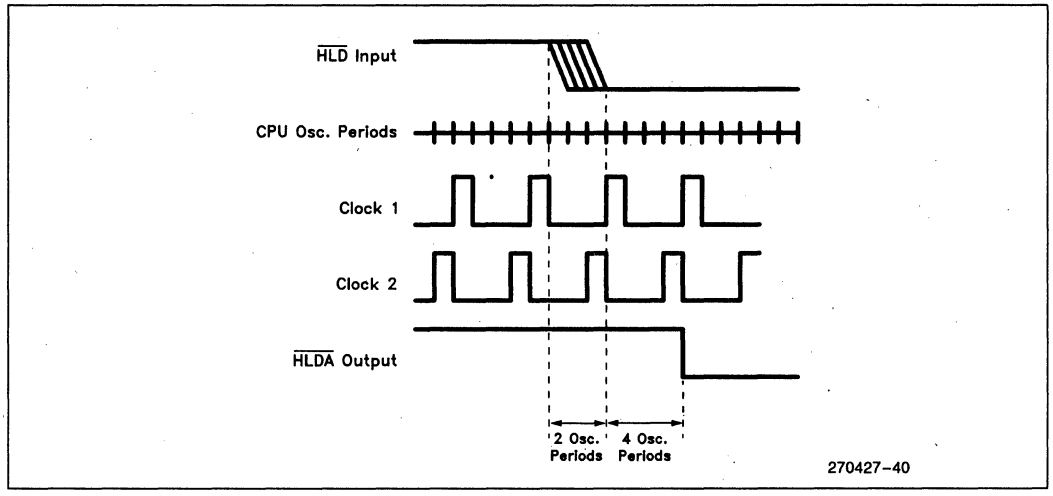


Figure 4.9. Minimum HLD/HLDA Response Time

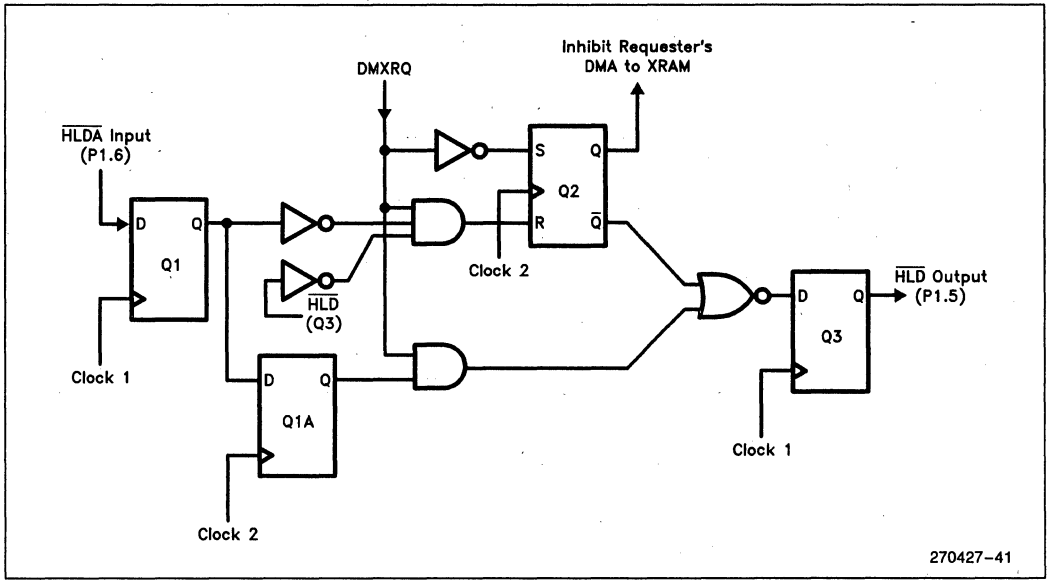


Figure 4.10. Internal Logic of the Requester (Clock 1 and Clock 2 are Shown in Figure 4.9)

4.3.5 Internal Logic of the Requester

The internal logic of the requester is shown in Figure 4.10. Initially, the requester's internal signal DMXRQ (DMA to XRAM Request) is at 0, so Q2 is set and the $\overline{HLD}$ output is high. As long as Q2 stays set, the requester is inhibited from starting any DMA to XRAM.

When the requester wants to DMA the XRAM, it first activates DMXRQ. This signal enables Q2 to be cleared (but doesn't clear it), and, if $\overline{HLDA}$ is high, also activates the $\overline{HLD}$ output.

A 1-to-0 transition from $\overline{HLDA}$ can now clear Q2, which will enable the requester to commence its DMA to XRAM. Q2 being low also maintains an output low at $\overline{HLD}$. When the DMA is completed, DMXRQ goes to 0, which sets Q2 and de-activates $\overline{HLD}$.

Only DMXRQ going to 0 can set Q2. That means once Q2 gets cleared, enabling the requester's DMA to proceed, the arbiter has no way to stop the requester's DMA in progress. At this point, de-activating $\overline{HLDA}$ will have no effect on the requester's use of the bus. Only the requester itself can stop the DMA in progress, and when it does, it de-activates both DMXRQ and $\overline{HLD}$.

If the DMA is in alternate cycles mode, then each time a DMA cycle is completed DMXRQ goes to 0, thus de-activating $\overline{HLD}$. Once $\overline{HLD}$ has been de-activated, it can't be re-asserted till after $\overline{HLDA}$ has been seen to go high (through flip-flop Q1A). Thus every time the DMA is suspended to allow an instruction cycle to proceed, the requester gives up the bus and must renew the request and receive another acknowledge before another DMA cycle to XRAM can proceed. Obviously in this case, the "alternate cycles" mode may consist of single DMA cycles separated by any number of instruction cycles, depending on how long it takes the requester to regain the bus.

A channel 1 DMA in progress will always be overridden by a DMA request of any kind from channel 0. If a channel 1 DMA to XRAM is in progress and is overridden by a channel 0 DMA which does not require the bus, DMXRQ will go to 0 during the channel 0 DMA, thus de-activating $\overline{HLD}$. Again, the requester must renew its request for the bus, and must receive a new 1-to-0 transition in $\overline{HLDA}$ before channel 1 can continue its DMA to XRAM.

4.4 DMA Arbitration

The DMA Arbitration described in this section is not arbitration between two devices wanting to access a shared RAM, but on-chip arbitration between the two DMA channels on the 8XC152.

The 8XC152 provides two DMA channels, either of which may be called into operation at any time in response to real time conditions in the application circuit. Since a DMA cycle always uses the 8XC152's internal bus, and there's only one internal bus, only one DMA channel can be serviced during a single DMA cycle. Executing program instructions also requires the internal bus, so program execution will also be suspended in order for a DMA to take place.

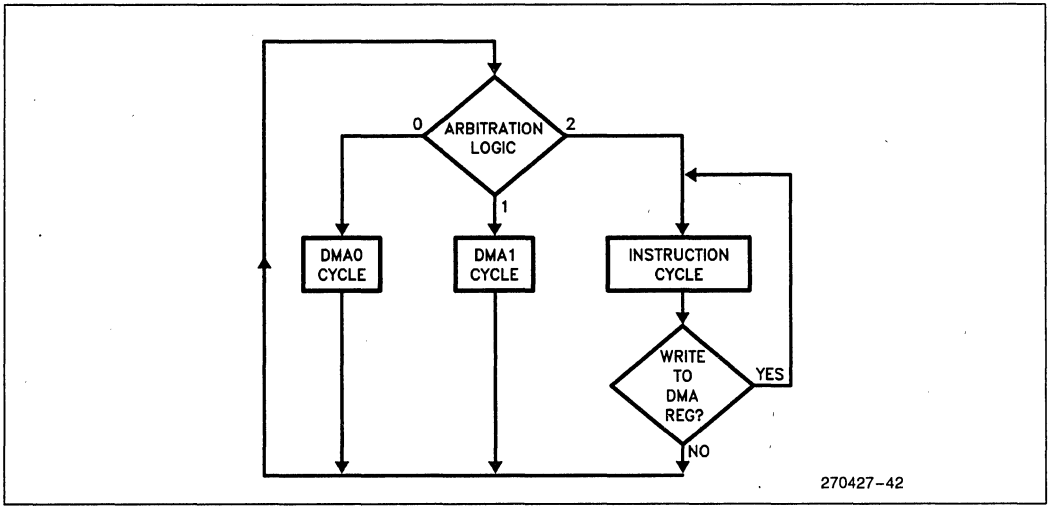


Figure 4.11. Internal Bus Usage

Figure 4.11 shows the three tasks to which the internal bus of the 8XC152 can be dedicated. In this figure, Instruction Cycle means the complete execution of a single instruction, whether it takes 1, 2 or 4 machine cycles. DMA Cycle means the transfer of a single data byte from source to destination, whether it takes 1 or 2 machine cycles. Each time a DMA Cycle or an Instruction Cycle is executed, on-chip arbitration logic determines which type of cycle is to be executed next.

Note that when an instruction is executed, if the instruction wrote to a DMA register (defined in Figure 4.1 but excluding PCON), then another instruction is executed without further arbitration. Therefore, a single write or a series of writes to DMA registers will prevent a DMA from taking place, and will continue to prevent a DMA from taking place until at least one instruction is executed which does not write to any DMA register.

The logic that determines whether the next cycle will be a DMA0 cycle, a DMA1 cycle, or an Instruction Cycle is shown in Figure 4.12 as a pseudo-HLL function. The statements in Figure 4.12 are executed sequentially unless an "if" condition is satisfied, in which case the corresponding "return" is executed and the remainder of the function is not. The return value of 0, 1, or 2 is passed to the arbitration logic block in Figure 4.11 to determine which exit path from the block is used.

The return value is based on the condition of the GO bit for each channel, and on the value returned by another function, named mode__logic ( ). The algorithm for mode__logic ( ) is the same for both channels. The function is shown in Figure 4.13 as a pseudo-HLL function, mode__logic (n), where n = 0 when the function is invoked for DMA channel 0, and n = 1 when it's invoked for DMA channel 1. The value returned by this function is either 0 or 1, and will be passed on to the DMA arbitration logic in Figure 4.12.

Note that the arbitration logic as shown in Figure 4.12 always gives precedence to channel 0 over channel 1. If GO0 is set and mode__logic (0) returns a 1, then a DMA0 cycle is called without further reference to the situation in channel 1. That is not to say a DMA1 Cycle will be interrupted once it has begun. Once a cycle has begun, be it an Instruction Cycle or a DMA Cycle, it will be completed without interruption.

The statements in mode__logic (n), Figure 4.13, are executed sequentially until an "if" condition, based on the DMA mode programmed into DCONn, is satisfied. For example, if the channel is configured to Burst mode, then the first if-condition is satisfied, so the "return 1" expression is executed and the remainder of the function is not.

```
arbitration_logic:

    if (GO0 = 1 .AND. mode_logic(0) = 1) return 0;

    if (GO1 = 1 .AND. mode_logic(1) = 1) return 1;

    else return 2;

    end arbitration_logic;
```

Figure 4.12. DMA Arbitration Logic

```
mode_logic(n):
    if (DCONn indicates burst_mode) return 1;
    if (DCONn indicates extern_demand_mode)
        {
        if (demand_flag = 1) return 1;
        else return 0;
        }
    if (DCONn indicates SP_demand_mode)
        {
        if (SARn = SBUF .AND. RI = 1) return 1;
        if (DARn = SBUF .AND. TI = 1) return 1;
        if (SARn = RFIFO .AND. RFNE = 1) return 1;
        if (DARn = TFIFO .AND. TFNF = 1 .AND.
         previous_cycle = instruction_cycle) return 1;
        else return 0;
        }
    if (DCONn indicates alt_cycles_mode)
        {
        if (DCONm indicates .NOT. alt_cycles_mode
            .OR. GOm = 0)
            {
            if (previous_cycle = instruction_cycle)
                return 1;
            else return 0;
            }
        if (previous_cycle = instruction_cycle
            .AND. previous_dma_cycle = .NOT. DMAn)
            return 1;
        }
    return 0;
    end mode_logic(n);
```

Figure 4.13. DMA Mode Logic

If the channel is configured to External Demand mode, then the first if-condition is not satisfied but the second one is. In that case the block of statements following that if-condition and delimited by {...} is executed: if the demand flag (IEO for channel 0 and IE1 for channel 1) is set, the "return 1" expression is executed and the remainder of the function is not. If the demand flag is not set, the "return 0" expression is executed and the remainder of the function is not.

If the channel is configured to Serial Port Demand mode, the source and destination addresses, SARn and DARn, have to be checked to see which Serial Port buffer is being addressed, and whether its demand flag is set.

SARn refers to the 16-bit source address for "this channel." Note that the condition

SARn = SBUF

cannot be true unless the SAS and ISA bits in DCONn are configured to select SFR space. If SARn is numerically equal to the address of SBUF (99H), and SAS and ISA are configured to select internal RAM rather than SFR space, then SARn refers to location 99H in the "upper 128" of internal RAM, not to SBUF.

If the test for SARn = SBUF *is* true, and if the flag RI is set, mode_logic (n) returns as 1 and the remainder of the function is not executed. Otherwise, execution proceeds to the next if-condition, testing DARn against SBUF and T1 against 1.

The same considerations regarding SAS and ISA in the SARn test are now applied to DAS and IDA in the DARn test. If SFR space isn't selected, no Serial Port buffer is being addressed.

Note that if DMA channel n is configured to Alternate Cycles mode, the logic must examine the other DCON register, DCONm, to determine if the other channel is also configured to Alternate Cycles mode and whether its GO bit is set. In Figure 4.13, the symbol DCONn refers to the DCON register for "this channel," and DCONm refers to "the other channel."

A careful examination of the logic in Figure 4.13 will reveal some idiosyncracies that the user should be aware of. First, the logic allows sequential DMA cycles to be generated to service RFIFO, but not to service TFIFO. This idiosyncracy is due to internal timing conflicts, and results in each individual DMA cycle to TFIFO having to be immediately preceded by an Instruction cycle. The logic disallows that there be two DMAs to TFIFO in a row.

If the user is unaware of this idiosyncracy, it can cause problems in situations where one DMA channel is servicing TFIFO and the other is configured to a completely different mode of operation.

For example, consider the situation where channel 0 is configured to service TFIFO and channel 1 is configured to Alternate Cycles mode. Then DMAs to TFIFO will always override the alternate cycles of channel 1. If TFIFO needs more than 1 byte it will receive them in precendence over channel 1, but each DMA to TFIFO must be preceded by an Instruction cycle. The sequence of cycles might be:

DMA1 cycle
Instruction cycle
DMA1 cycle, during which TFNF gets set
Instruction cycle
DMA0 cycle
Instruction cycle
DMA0 cycle, as a result of which TFNF gets cleared
Instruction cycle
DMA1 cycle
Instruction cycle
DMA1 cycle
Instruction cycle
. . .

The requirement that a DMA to TFIFO be preceded by an Instruction cycle can result in the normal precedence of channel 0 over channel 1 being thwarted. Consider for example the situation where channel 0 is configured to service TFIFO, and is in the process of doing so, and channel 1 decides it wants to do a Burst mode DMA. The sequence of events might be:

Instruction cycle (sets GO bit in DCON1)
Instruction cycle (during which TFNF gets set)
DMA0 cycle
DMA1 cycle
DMA1 cycle
DMA1 cycle
. . .
DMA1 cycle (completes channel 1 burst)
Instruction cycle
DMA0 cycle
Instruction cycle
. . .

This sequence begins with two Instruction cycles. The first one accesses a DMA register (DCON1), and therefore is followed by another Instruction cycle, which presumably does not access a DMA register. After the second Instruction cycle both channels are ready to generate DMA cycles, and channel 0 of course takes precedence. After the DMA0 cycle, channel 0 must wait for an Instruction cycle before it can access TFIFO again. Channel 1, being in Burst mode, doesn't have that restriction, and is therefore granted a DMA1 cycle. After the first DMA1 cycle, channel 0 is still waiting for an Instruction cycle and channel 1 still does not have that restriction. There follows another DMA1 cycle.

The result is that in this particular case channel 0 has to wait until channel 1 completes its Burst mode DMA, and then has to wait for an Instruction cycle to be generated, before it can continue its own DMA to TFIFO. The delay in servicing TFIFO can cause an Underflow condition in the GSC transmission.

The delay will not occur if channel 1 is configured to Alternate Cycles mode, since channel 0 would then see the Instruction cycles it needs to complete its logic requirements for asserting its request.

4.4.1 DMA Arbitration with Hold/Hold Ack

The Hold/Hold Acknowledge feature is invoked by setting either the ARB or REQ bit in PCON. Their effect is to add the requirements of the Hold/Hold Ack protocol to mode_logic ( ). This amounts to replacing every expression "return 1" in Figure 4.13 with the expression "return hld_hlda_logic ()", where hld_hlda_logic ( ) is a function which returns 1 if the Hold/Hold Ack protocol is satisfied, and returns 0 otherwise. A suitable definition for hld_hlda_logic ( ) is shown in Figure 4.14.

4.5 Summary of DMA Control Bits

DCONn	DAS	IDA	SAS	ISA	DM	TM	DONE	GO

DAS specifies the Destination Address Space. If DAS = 0, the destination is in External Data Memory. If DAS = 1 and IDA = 0, the destination is a Special Function Register (SFR). If DAS = 1 and IDA = 1, the destination is in Internal Data RAM.

IDA (Increment Destination Address) If IDA = 1, the destination address is automatically incremented after each byte transfer. If IDA = 0, it is not.

SAS specifies the Source Address Space. If SAS = 0, the source is in External Data Memory. If SAS = 1 and ISA = 0, the source is an SFR. If SAS = 1 and ISA = 1, the source is Internal Data RAM.

ISA (Increment Source Address) If ISA = 1, the source address is automatically incremented after each byte transfer. If ISA = 0, it is not.

DM (Demand Mode) If DM = 1, the DMA Channel operates in Demand Mode. In Demand Mode the DMA is initiated either by an external signal or by a Serial Port flag, depending on the value of the TM bit. If DM = 0, the DMA is requested by setting the GO bit in software.

TM (Transfer Mode) If DM = 1 then TM selects whether a DMA is initiated by an external signal (TM = 1) or by a Serial Port flag (TM = 0). If DM = 0 then TM selects whether the data transfers are to be in bursts (TM = 1) or in alternate cycles (TM = 0).

DONE indicates the completion of a DMA operation and flags an interrupt. It is set to 1 by on-chip hardware when BCRn = 0, and is cleared to 0 by on-chip hardware when the interrupt is vectored to. It can also be set or cleared by software.

```
hold_holda( ):
    if (ARB = 0 .AND. REQ = 0) return 1;
    if SARn = XRAM .OR. DARn = XRAM)
        {
        if (ARB = 1 .AND. HLDA = 1) return 1;
        if (REQ = 1 .AND. HLDA = 0) return 1;
        else return 0;
        }
    return 1;
    end hold_holda( );
```

Figure 4.14. Hold/Hold Acknowledge Logic as a Pseudo-HLL Function

GO is the enable bit for the DMA Channel itself. The DMA Channel is inactive if GO = 0.

PCON	SMOD	ARB	REQ	GAREN	XRCLK	GFIEN	PDN	IDL

ARB enables the DMA logic to detect $\overline{HLD}$ and generate $\overline{HLDA}$. After it has activated $\overline{HLDA}$, the C152 will not begin a new DMA to or from External Data Memory as long as $\overline{HLD}$ is seen to be active. This logic is disabled when ARB = 0, and enabled when ARB = 1.

REQ enables the DMA logic to generate $\overline{HLD}$ and detect $\overline{HLDA}$ before performing a DMA to or from External Data Memory. After it has activated $\overline{HLD}$, the C152 will not begin the DMA until $\overline{HLDA}$ is seen to be active. This logic is disabled when REQ = 0, and enabled when REQ = 1.

5.0 INTERRUPT STRUCTURE

The 8XC152 retains all five interrupts of the 80C51BH. Six new interrupts are added in the 8XC152, to support its GSC and the DMA features. They are as listed below, and the flags that generate them are shown in Figure 5.1.

GSCRV — GSC Receive Valid
GSCRE — GSC Receive Error
GSCTV — GSC Transmit Valid
GSCTE — GSC Transmit Error
DMA0 — DMA Channel 0 Done
DMA1 — DMA Channel 1 Done

As shown in Figure 5.1, the Receive Valid interrupt can be signaled either by the RFNE flag (Receive FIFO Not Empty), or by the RDN flag (Receive Done). Which one of these flags causes the interrupt depends on the setting of the DMA bit in the SFR named TSTAT.

DMA = 0 means the DMA hardware is not configured to service the GSC, so the CPU will service it in software in response to the Receive FIFO not being empty. In that case, RFNE generates the Receive Valid interrupt.

DMA = 1 means the DMA hardware is configured to service the GSC, in which case the CPU need not be interrupted till the receive is complete. In that case, RDN generates the Receive Valid interrupt.

Similarly the Transmit Valid interrupt can be signaled either by the TFNF flag (Transmit FIFO Not Full), or by the TDN flag (Transmit Done), depending on whether the DMA bit is 0 or 1.

Note that setting the DMA bit does not itself configure the DMA channels to service the GSC. That job must be done by software writes to the DMA registers. The DMA bit only selects whether the GSCRV and GSCTV interrupts are flagged by a FIFO needing service or by an "operation done" signal.

The Receive and Transmit Error interrupt flags are generated by the logical OR of a number of error conditions, which are described in Section 3.6.5.

Each interrupt is assigned a fixed location in Program Memory, and the interrupt causes the CPU to jump to that location. All the interrupt flags are sampled at S5P2 of every machine cycle, and then the samples are sequentially polled during the next machine cycle. If more than one interrupt of the same priority is active, the one that is highest in the polling sequence is serviced first. The interrupts and their fixed locations in Program Memory are listed below in the order of their polling sequence.

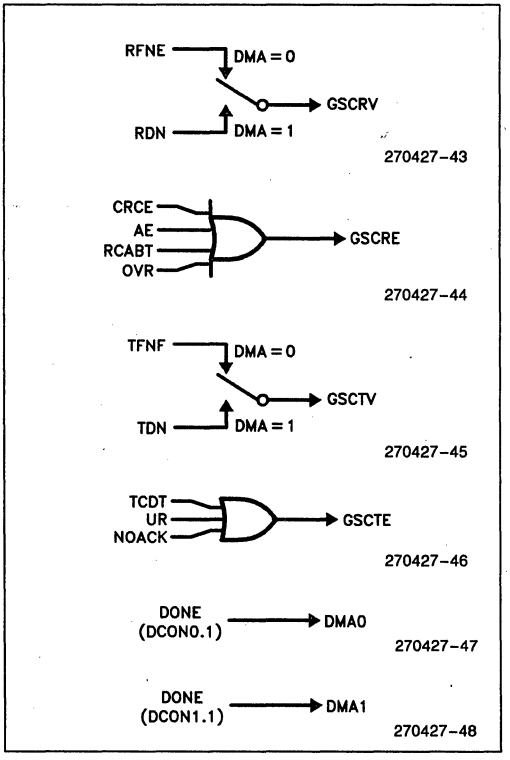


Figure 5.1. Six New Interrupts in the 8XC152

Interrupt	Location	Name
IE0	0003H	External Interrupt 0
GSCRV	002BH	GSC Receive Valid
TF0	000BH	Timer 0 Overflow
GSCRE	0033H	GSC Receive Error
DMA0	003BH	DMA Channel 0 Done
IE1	0013H	External Interrupt 1
GSCTV	0043H	GSC Transmit Valid
DMA1	0053H	DMA Channel 1 Done
TF1	001BH	Timer 1 Overflow
GSCTE	004BH	GSC Transmit Error
TI + RI	0023H	UART Transmit/Receive

Note that the locations of the basic 8051 interrupts are the same as in the rest of the MCS-51 Family. And relative to each other they retain their same positions in the polling sequence.

The locations of the new interrupts all follow the locations of the basic 8051 interrupts in Program Memory, but they are interleaved with them in the polling sequence.

To support the new interrupts a second Interrupt Enable register and a second Interrupt Priority register are implemented in bit-addressable SFR space. The two Interrupt Enable registers in the 8XC152 are as follows:

	7	6	5	4	3	2	1	0
IE:	EA	—	—	ES	ET1	EX1	ET0	EX0

Address of IE in SFR space = 0A8H (bit-addressable)

	7	6	5	4	3	2	1	0
IEN1:	—	—	EGSTE	EDMA1	EGSTV	EDMA0	EGSRE	EGSRV

Address pF IE1 in SFR space = 0C8H (bit-addressable)

The bits in IE are unchanged from the standard 8051 IE register. The bits in IEN1 are as follows:

EGSTE = 1 Enable GSC Transmit Error Interrupt
= 0 Disable
EDMA1 = 1 Enable DMA Channel 1 Done Interrupt
= 0 Disable
EGSTV = 1 Enable GSC Transmit Valid Interrupt
= 0 Disable
EDMA0 = 1 Enable DMA Channel 0 Done Interrupt
= 0 Disable
EGSRE = 1 Enable GSC Receive Error Interrupt
= 0 Disable
EGSRV = 1 Enable GSC Receive Valid Interrupt
= 0 Disable

The two Interrupt Priority registers in the 8XC152 are as follows:

	7	6	5	4	3	2	1	0
IP:	—	—	—	PS	PT1	PX1	PT0	PX0

Address of IP in SFR space = 0B8H (bit-addressable)

	7	6	5	4	3	2	1	0
IPN1:	—	—	PGSTE	PDMA1	PGSTV	PDMA0	PGSRE	PGSRV

Address of IPN1 in SFR space = 0F8H (bit-addressable)

The bits in IP are unchanged from the standard 8051 IP register. The bits in IPN1 are as follows:

PGSTE = 1 GSC Transmit Error Interrupt Priority to High
= 0 Priority to Low
PDMA1 = 1 DMA Channel 1 Done Interrupt Priority to High
= 0 Priority to Low
PGSTV = 1 GSC Transmit Valid Interrupt Priority to High
= 0 Priority to Low
PDMA0 = 1 DMA Channel 0 Done Interrupt Priority to High
= 0 Priority to Low
PGSRE = 1 GSC Receive Error Interrupt Priority to High
= 0 Priority to Low
PGSRV = 1 GSC Receive Valid Interrupt Priority to High
= 0 Priority to Low

Note that these registers all have unimplemented bits ("—"). If these bits are read, they will return unpredictable values. If they are written to, the value written goes nowhere.

It is recommended that user software should never write 1s to unimplemented bits in MCS-51 devices. Future versions of the device may have new bits installed in these locations. If so, their reset value will be 0. Old software that writes 1s to newly implemented bits may unexpectedly invoke new features.

The MCS-51 interrupt structure provides hardware support for only two priority levels, High and Low. With as many interrupt sources as the 8XC152 has, it may be helpful to know how to augment the priority structure in software. Any number of priority levels can be implemented in software by saving and redefining the interrupt enable registers within the interrupt service routines. The technique is described in the "MCS-51" Architectural Overview" chapter in this handbook.

5.1 GSC Transmitter Error Conditions

The GSC Transmitter section reports three kinds of error conditions:

TCDT — Transmitter Collision Detector

UR — Underrun in Transmit FIFO

NOACK — No Acknowledge

These bits reside in the TSTAT register. User software can read them, but only the GSC hardware can write to them. The GSC hardware will set them in response to the various error conditions that they represent. When user software sets the TEN bit, the GSC hardware will at that time clear these flags. This is the only way these flags can be cleared.

The logical OR of these three bits flags the GSC Transmit Error interrupt (GSCTE) and clears the TEN bit, as shown in Figure 5.2. Thus any detected error condition aborts the transmission. No CRC bits are transmitted. In SDLC mode, no EOF flag is generated. In CSMA/CD mode, an EOF is generated by default, since the GTXD pin is pulled to a logic 1 and held there.

The TCDT bit can get set only if the GSC is configured to CSMA/CD mode. In that case, the GSC hardware sets TCDT when a collision is detected during a transmission, and the collision was detected after TFIFO has been accessed. Also, the GSC hardware sets TCDT when a detected collision causes the TCDCNT register to overflow.

The UR bit can get set only if the DMA bit in TSTAT is set. The DMA bit being set informs the GSC hardware that TFIFO is being serviced by DMA. In that case, if the GSC goes to fetch another byte from TFIFO and finds it empty, and the byte count register of the DMA channel servicing TFIFO is not zero, it sets the UR bit.

If the DMA hardware is not being used to service TFIFO, the UR bit cannot get set. If the DMA bit is 0, then when the GSC finds TFIFO empty, it assumes that the transmission of data is complete and the transmission of CRC bits can begin.

The NOACK bit is functional only in CSMA/CD mode, and only when the HABEN bit in RSTAT is set. The HABEN bit turns on the Hardware Based Acknowledge feature, as described in Section 3.2.6. If this feature is not invoked, the NOACK bit will stay at 0.

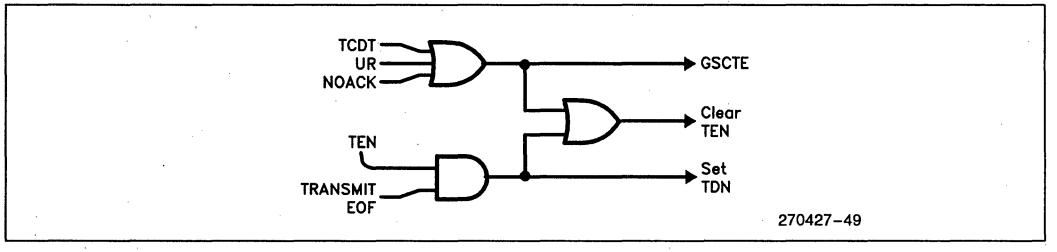


Figure 5.2. Transmit Error Flags (Logic for Clearing TEN, Setting TDN)

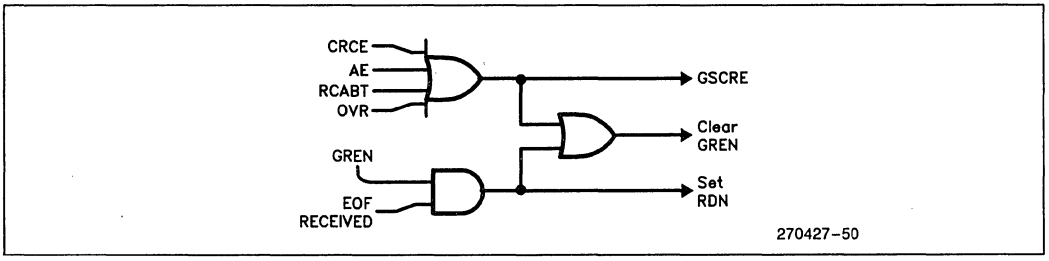


Figure 5.3. Receive Error Flag (Logic for Clearing GREN, setting RDN)

If the NOACK bit gets set, it means the GSC has completed a transmission, and was expecting to receive a hardware based acknowledge from the receiver of the message, but did not receive the acknowledge, or at least did not receive it cleanly. There are three ways the NOACK bit can get set:

1. The acknowledge signal (an unattached preamble) was not received before the IFS was completed.
2. A collision was detected during the IFS.
3. The line was active during the last bit-time of the IFS.

The first condition is an obvious reason for setting the NOACK bit, since that's what the hardware based acknowledge is for. The other two ways the NOACK bit can get set are to guard against the possibility that the transmitting station might mistake an unrelated transmission or transmission fragment for an acknowledge signal.

5.2 GSC Receiver Error Conditions

The GSC Receiver section reports four kinds of error conditions:

CRCE — CRC Error

AE — Alignment Error

RCABT — Receive Abort

OVR — Overrun in Receive FIFO

These bits reside in the RSTAT register. User software can read them, but only the GSC hardware can write to them. The GSC hardware will set them in response to the various error conditions that they represent. When user software sets the GREN bit, the GSC hardware will at that time clear these flags. This is the only way these flags can be cleared.

The logical OR of these four bits flags the GSC Receive Error interrupt (GSCRE) and clears the GREN bit, as shown in Figure 5.3. Note in this figure that any error condition will prevent RDN from being set.

A CRC Error means the CRC generator did not come to its correct value after calculating the CRC of the message plus received CRC. An Alignment Error means the number of bits received between the BOF and EOF was not a multiple of 8.

In SDLC mode, the CRCE bit gets set at the end of any frame in which there is a CRC Error, and the AE bit gets set at the end of any frame in which there is an Alignment Error.

In CSMA/CD mode, if there is no CRC Error, neither CRCE nor AE will get set. If there is a CRC Error and no Alignment Error, the CRCE bit will get set, but not the AE bit. If there is both a CRC Error and an Alignment Error, the AE bit will get set, but not the CRCE bit. Thus in CSMA/CD mode, the CRCE and AE bits are mutually exclusive.

The Receive Abort flag, RCABT, gets set if an incoming frame was interrupted after received data had already passed to the Receive FIFO. In SDLC mode, this can happen if a line idle condition is detected before an EOF flag is. In CSMA/CD mode, it can happen if there is a collision. In either case, the CPU will have to re-initialize whatever pointers and counters it might have been using.

The Overrun Error flag, OVR, gets set if the GSC Receiver is ready to push a newly received byte onto the Receive FIFO, but the FIFO is full.

Up to 7 "dribble bits" can be received after the EOF without causing an error condition.

6.0 GLOSSARY

ADR0,1,2,3 (95H, 0A5H, 0B5H, 0C5H) - Address Match Registers 0,1,2,3 - The contents of these SFRs are compared against the address bits from the serial data on the GSC. If the address matches the SFR, then the C152 accepts that frame. If in 8 bit addressing mode, a match with any of the four registers will trigger acceptance. In 16 bit addressing mode, a match with ADR1:ADR0 or ADR3:ADR2 will be accepted. Address length is determined by GMOD (AL).

AE - Alignment Error, see RSTAT.
AL - Address Length, see GMOD.

AMSK0,1 (0D5H, 0E5H) - Address Match Mask 0,1 - Identifies which bits in ADR0,1 are "don't care" bits. Setting a bit to 1 in AMSK0,1 identifies the corresponding bit in ADDR0,1 as not to be examined when comparing addresses.

BAUD - (94H) Contains the programmable value for the baud rate generator for the GSC. The baud rate will equal (fosc)/((BAUD + 1) × 8).

BCRL0,1 (0E2H, 0F2H) - Byte Count Register Low 0,1 - Contains the lower byte of the byte count. Used during DMA transfers to identify to the DMA channels when the transfer is complete.

BCRH0,1 (0E3H, 0F3H) - Byte Count Register High 0,1 - Contains the upper byte of the byte count.

BKOFF (0C4H) - Backoff Timer - The backoff timer is an eight bit count-down timer with a clock period equal to one slot time. The backoff time is used in the CSMA/CD collision resolution algorithm.

BOF - Beginning of Frame flag - A term commonly used when dealing with packetized data. Signifies the beginning of a frame.

CRC - Cyclic Redundancy Check - An error checking routine that mathematically manipulates a value dependent on the incoming data. The purpose is to identify when a frame has been received in error.

CRCE - CRC Error, see RSTAT.

CSMA/CD - Stands for Carrier Sense, Multiple Access, with Collision Detection.

CT - CRC Type, see GMOD.

DARL0/1 (0C2H, 0D2H) - Destination Address Register Low 0/1 - Contains the lower byte of the destinations' address when performing DMA transfers.

DARH0/1 (0C3H, 0D3H) - Destination Address Register Low 0/1 - Contains the upper byte of the destinations' address when performing DMA transfers.

DAS - Destination Address Space, see DCON.

DCJ - D.C. Jam, see MYSLOT.

DCON0/1 (092H,093H)

7	6	5	4	3	2	1	0
DAS	IDA	SAS	ISA	DM	TM	DONE	GO

The DCON registers control the operation of the DMA channels by determining the source of data to be transferred, the destination of the data to be transfer, and the various modes of operation.

DCON.0 (GO) - Enables DMA Transfer - When set it enables a DMA channel. If block mode is set then DMA transfer starts as soon as possible under CPU control. If demand mode is set then DMA transfer starts when a demand is asserted and recognized.

DCON.1 (DONE) - DMA Transfer is Complete - When set the DMA transfer is complete. It is set when BCR equals 0 and is automatically reset when the DMA vectors to its interrupt routine. If DMA interrupt is disabled and the user software executes a jump on the DONE bit, then the user software must also reset the done bit. If DONE is not set, then the DMA transfer is not complete.

DCON.2 (TM) - Transfer Mode - When set, DMA burst transfers are used if the DMA channel is configured in block mode or external interrupts are used to initiate a transfer if in Demand Mode. When TM is cleared, Alternate Cycle Transfers are used if DMA is in the Block Mode, or Local Serial channel/GSC interrupts are used to initiate a transfer if in Demand Mode.

DCON.3 (DM) - DMA Channel Mode - When set, Demand Mode is used and when cleared, Block Mode is used.

DCON.4 (ISA) - Increment Source Address - When set, the source address registers are automatically incremented during each transfer. When cleared, the source address registers are not incremented.

DCON.5 (SAS) - Source Address Space - When set, the source of data for the DMA transfers is internal data memory if autoincrement is also set. If autoincrement is not set but SAS is, then the source for data will be one of the Special Function Registers. When SAS is cleared, the source for data is external data memory.

DCON.6 (IDA) - Increment Destination Address Space - When set, destination address registers are incremented once after each byte is transferred. When cleared, the destination address registers are not automatically incremented.

DCON.7 (DAS) - Destination Address Space - When set, destination of data to be transferred is internal data memory if autoincrement mode is also set. If autoincrement is not set the destinationwill be one of the Special Function Registers. When DAS is cleared then the destination is external data memory.

DCR - Deterministic Resolution, see MYSLOT.

$\overline{DEN}$ - An alternate function of one of the port 1 pins (P1.2). Its purpose is to enable external drivers when the GSC is transmitting data. This function is always active when using the GSC and if P1.2 is programmed to a 1.

DM - DMA Mode, see DCON0.

DMA - Direct Memory Access mode, see TSTAT.

DONE - DMA done bit, see DCON0.

DPH - Data Pointer High, an SFR that contains the high order byte of a general purpose pointer called the data pointer (DPTR).

DPL - Data Pointer Low, an SFR that contains the low order byte of the data pointer.

EDMA0 - Enable DMA Channel 0 interrupt, see IEN1.

EDMA1 - Enable DMA Channel 1 interrupt, see IEN1.

EGSRE - Enable GSC Receive Error interrupt, see IEN1.

EGSRV - Enable GSC Receive Valid interrupt, see IEN1.

EGSTE - Enable GSC Transmit Error interrupt, see IEN1.

EGSTV - Enable GSC Transmit Valid interrupt, see IEN1.

EOF - A general term used in serial communications. EOF stands for End Of Frame and signifies when the last bits of data are transmitted when using packetized data.

ES - Enable LSC Service interrupt, see IE.

ET0 - Enable Timer 0 interrupt, see IE.

ET1 - Enable Timer 1 interrupt, see IE.

EX0 - Enable External interrupt 0, see IE.

EX1 - Enable External interrupt 1, see IE.

GMOD (84H)

7	6	5	4	3	2	1	0
XTCLK	M1	M0	AL	CT	PL1	PL0	PR

The bits in this SFR, perform most of the configuration on the type of data transfers to be used with the GSC. Determines the mode, address length, preamble length, protocol select, and enables the external clocking of the transmit data.

GMOD.0 (PR) - Protocol - If set, SDLC protocols with NRZI encoding, zero bit insertion, and SDLC flags are used. If cleared, CSMA/CD link access with Manchester encoding is used.

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GMOD.1,2 (PL0,1) - Preamble length

PL1	PL0	LENGTH (BITS)
0	0	0
0	1	8
1	0	32
1	1	64

The length includes the two bit Begin Of frame (BOF) flag in CSMA/CD but does not include the SDLC flag. In SDLC mode, the BOF is an SDLC flag, otherwise it is two consecutive ones. Zero length is not compatible in CSMA/CD mode.

GMOD.3 (CT) - CRC Type - If set, 32-bit AUTODIN-II-32 is used. If cleared, 16-bit CRC-CCITT is used.

GMOD.4 (AL) - Address Length - If set, 16-bit addressing is used. If cleared, 8-bit addressing is used. In 8-bit mode, a match with any of the 4 address registers will allow that frame to be accepted (ADR0, ADR1, ADR2, ADR3). "Don't Care" bits may be masked in ADR0 and ADR1 with AMSK0 and AMSK1. In 16-bit mode, addresses are matched against "ADR1:ADR0" or "ADR3:ADR2". Again, "Don't Care" bits in ADR1:ADR0 can be masked in AMSK1:AMSK0. A received address of all ones will always be recognized in any mode.

GMOD.5, 6 (M0,M1) - Mode Select - Two test modes, an optional "alternate backoff" mode, or normal backoff can be enabled with these two bits.

M1	M0	Mode
0	0	Normal
0	1	Raw Transmit
1	0	Raw Receive
1	1	Alternate Backoff

GMOD.7 (XTCLK) - External Transmit Clock - If set an external 1X clock is used for the transmitter. If cleared the internal baud rate generator provides the

transmit clock. The input clock is applied to P1.3 ($\overline{TxC}$). The user software is responsible for setting or clearing this flag. External receive clock is enabled by setting PCON.3.

GO - DMA Go bit, see DCON0.

GRxD - GSC Receive Data input, an alternate function of one of the port 1 pins (P1.0). This pin is used as the receive input for the GSC. P1.0 must be programmed to a 1 for this function to operate.

GSC - Global Serial Channel - A high-level, multi-protocol, serial communication controller added to the 80C51BH core to accomplish high-speed transfers of packetized serial data.

GTxD - GSC Transmit Data output, an alternate function of one of the port 1 pins (P1.1). This pin is used as the transmit output for the GSC. P1.1 must be programmed to a 1 for this function to operate.

HBAEN - Hardware Based Acknowledge Enable, see RSTAT.

HLDA - Hold Acknowledge, an alternate function of one of the port 1 pins (P1.6). This pin is used to perform the "HOLD ACKNOWLEDGE" function for DMA transfers. HLDA can be an input or an output, depending on the configuration of the DMA channels. P1.6 must be programmed to a 1 for this function to operate.

HOLD - Hold, an alternate function of one of the port 1 pins (P1.5). This pin is used to perform the "HOLD" function for DMA transfers. HOLD can be an input or an output, depending on the configuration of the DMA channels. P1.5 must be programmed to a 1 for this function to operate.

IDA - Increment Destination Address, see DCON0.

IE (0A8H)

7	6	5	4	3	2	1	0
EA			ES	ET1	EX1	ET0	EX0

Interrupt Enable SFR, used to individually enable the Timer and Local Serial Channel interrupts. Also contains the global enable bit which must be set to a 1 to enable any interrupt to be automatically recognized by the CPU.

IE.0 (EX0) - Enables the external interrupt $\overline{INT0}$ on P3.2.

IE.1 (ET0) - Enables the Timer 0 interrupt.

IE.2 (EX1) - Enables the external interrupt $\overline{INT1}$ on P3.3.

IE.3 (ET1) - Enables the Timer 1 interrupt.

IE.4 (ES) - Enables the Local Serial Channel interrupt.

IE.7 (EA) - The global interrupt enable bit. This bit must be set to a 1 for any other interrupt to be enabled.

IEN1 - (0C8H)

7	6	5	4	3	2	1	0
		EGSTE	EDMA1	EGSTV	EDMA0	EGSRE	EGSRV

Interrupt enable register for DMA and GSC interrupts. A 1 in any bit position enables that interrupt.

IEN1.0 (EGSRV) - Enables the GSC valid receive interrupt.

IEN1.1 (EGSRE) - Enables the GSC receive error interrupt.

IEN1.2 (EDMA0) - Enables the DMA done interrupt for Channel 0.

IEN1.3 (EGSTV) - Enables the GSC valid transmit interrupt.

IEN1.4 (EDMA1) - Enables the DMA done interrupt for Channel 1.

IEN1.5 (EGSTE) - Enables the GSC transmit error interrupt

IFS - (0A4H) Interframe Space, determines the number of bit times separating transmitted frames in CSMA/CD and SDLC.

IP (0B8H)

7	6	5	4	3	2	1	0
			PS	PT1	PX1	PT0	PX0

Allows the user software two levels of prioritization to be assigned to each of the interrupts in IE. A 1 assigns the corresponding interrupt in IE a higher interrupt than an interrupt with a corresponding 0.

IP.0 (PX0) - Assigns the priority of external interrupt, $\overline{INT0}$.

IP.1 (PT0) - Assigns the priority of Timer 0 interrupt, T0.

IP.2 (PX1) - Assigns the priority of external interrupt, $\overline{INT1}$.

IP.3 (PT1) - Assigns the priority of Timer 1 interrupt, T1.

IP.4 (PS) - Assigns the priority of the LSC interrupt, SBUF.

IPN1 - (0F8H)

7	6	5	4	3	2	1	0
		PGSTE	PDMA1	PGSTV	PDMA0	PGSRE	PGSRV

Allows the user software two levels of prioritization to be assigned to each of the interrupts in IEN1. A 1 assigns the corresponding interrupt in IEN1 a higher interrupt than an interrupt with a corresponding 0.

IPN1.0 (PGSRV) - Assigns the priority of GSC receive valid interrupt.

IPN1.1 (PGSRE) - Assigns the priority of GSC error receive interrupt.

IPN1.2 (PDMA0) - Assigns the priority of DMA done interrupt for Channel 0.

IPN1.3 (PGSTV) - Assigns the priority of GSC transmit valid interrupt.

IPN1.4 (PDMA1) - Assigns the priority of DMA done interrupt for Channel 1.

IPN1.5 (PGSTE) - Assigns the priority of GSC transmit error interrupt.

ISA - Increment Source Address, see DCON0.

LNI - Line Idle, see TSTAT.

LSC - Local Serial Channel - The asynchronous serial port found on all MCS-51 devices. Uses start/stop bits and can transfer only 1 byte at a time.

M0 - One of two GSC mode bits, see TMOD.

M1 - One of two GSC mode bits, see TMOD

MYSLOT - (0F5H)

7	6	5	4	3	2	1	0
DCJ	DCR	SA5	SA4	SA3	SA2	SA1	SA0

Determines which type of Jam is used, which backoff algorithm is used, and the DCR slot address for the GSC.

MYSLOT.0,1,2,3,4,5 (SA0,1,2,3,4,5) - These bits determine which slot address is assigned to the C152 when using deterministic backoff during CSMA/CD operations on the GSC. Maximum slots available is 63. An address of 00H prevents that station from participating in the backoff process.

MYSLOT.6 (DCR) - Determines which collision resolution algorithm is used. If set to a 1, then the deterministic backoff is used. If cleared, then a random slot assignment is used.

MYSLOT.7 (DCJ) - Determines the type of Jam used during CSMA/CD operation when a collision occurs. If set to a 1 then a low D.C. level is used as the jam signal. If cleared, then $\overline{CRC}$ is used as the jam signal. The jam is applied for a length of time equal to the CRC length.

NOACK - No Acknowledgment error bit, see TSTAT.

NRZI - Non-Return to Zero inverted, a type of data encoding where a 0 is represented by a change in the level of the serial link. A 1 is represented by no change.

OVR - Overrun error bit, see RSTAT.

PR - Protocol select bit, see GMOD. PCON (87H)

7	6	5	4	3	2	1	0
SMOD	ARB	REQ	GAREN	XRCLK	GFIEN	PD	IDL

PCON.0 (IDL) - Idle bit, used to place the C152 into the idle power saving mode.

PCON.1 (PD) - Power Down bit, used to place the C152 into the power down power saving mode.

PCON.2 (GFIEN) - GSC Flag Idle Enable bit, when set, enables idle flags (01111110) to be generated between transmitted frames in SDLC mode.

PCON.3 (XRCLK) - External Receive Clock bit, used to enable an external clock to be used for only the receiver portion of the GSC.

PCON.4 (GAREN) - GSC Auxiliary Receive Enable bit, used to enable the GSC to receive back-to-back SDLC frames. This bit has no effect in CSMA/CD mode.

PCON.5 (REQ) - Requester mode bit, set to a 1 when C152 is to be operated as the requester station during DMA transfers.

PCON.6 (ARB) - Arbiter mode bit, set to a 1 when C152 is to be operated as the arbiter during DMA transfers.

PCON.7 (SMOD) - LSC mode bit, used to double the baud rate on the LSC.

PDMA0 - Priority bit for DMA Channel 0 interrupt, see IPN1.

PDMA1 - Priority bit for DMA Channel 1 interrupt, see IPN1.

PGSRE - Priority bit for GSC Receive Error interrupt, see IPN1.

PGSRV - Priority bit for GSC Receive Valid interrupt, see IPN1.

PGSTE - Priority bit for GSC Transmit Error interrupt, see IPN1.

PGSTV - Priority bit for GSC Transmit Valid interrupt, see IPN1.

PL0 - One of two bits that determines the Preamble Length, see GMOD.

PL1 - One of two bits that determines the Preamble Length, see GMOD.

PRBS - (0E4H) Pseudo-Random Binary Sequence, generates the pseudo-random number to be used in CSMA/CD backoff algorithms.

PS - Priority bit for the LSC service interrupt, see IP.

PT0 - Priority bit for Timer 0 interrupt, see IP.

PT1 - Priority bit for Timer 1 interrupt, see IP.

PX0 - Priority bit for External interrupt 0, see IP.

PX1 - Priority bit for External interrupt 1, see IP.

RCABT - GSC Receiver Abort error bit, see RSTAT.

RDN - GSC Receiver Done bit, see RSTAT.

GREN - GSC Receiver Enable bit, see RSTAT.

RFNE - GSC Receive FIFO Not Empty bit, see RSTAT.

RI - LSC Receive Interrupt bit, see SCON.

RFIFO - (F4H) RFIFO is a 3-byte FIFO that contains the receive data from the GSC.

RSTAT (0E8H) - Receive Status Register

7	6	5	4	3	2	1	0
OVR	RCABT	AE	CRCE	RDN	RFNE	GREN	HABEN

RSTAT.0 (HBAEN) - Hardware Based Acknowledge Enable - If set, enables the hardware based acknowledge feature.

RSTAT.1 (GREN) - Receiver Enable - When set, the receiver is enabled to accept incoming frames. The user must clear RFIFO with software before enabling the receiver. RFIFO is cleared by reading the contents of RFIFO until RFNE = 0. After each read of RFIFO, it takes one machine cycle for the status of RFNE to be updated. Setting GREN also clears RDN, CRCE, AE, and RCABT. GREN is cleared by hardware at the end of a reception or if any receive errors are detected. The status of GREN has no effect on whether the receiver detects a collision in CSMA/CD mode as the receiver input circuitry always monitors the receive pin.

RSTAT.2 (RFNE) - Receive FIFO Not Empty - If set, indicates that the receive FIFO contains data. The receive FIFO is a three byte buffer into which the receive data is loaded. A CPU read of the FIFO retrieves the oldest data and automatically updates the FIFO pointers. Setting GREN to a one will clear the receive FIFO. The status of this flag is controlled by the GSC. This bit is cleared if user software empties receive FIFO.

RSTAT.3 (RDN) - Receive Done - If set, indicates the successful completion of a receiver operation. Will not be set if a CRC, alignment, abort, or FIFO overrun error occurred.

RSTAT.4 (CRCE) - CRC Error - If set, indicates that a properly aligned frame was received with a mismatched CRC.

RSTAT.5 (AE) - Alignment Error - In CSMA/CD mode, AE is set if the receiver shift register (an internal serial-to-parallel converter) is not full and the CRC is bad when an EOF is detected. In CSMA/CD the EOF is a line idle condition (see LNI) for two bit times. If the CRC is correct while in CSMA/CD mode, AE is not set and any mis-alignment is assumed to be caused by dribble bits as the line went idle. In SDLC mode, AE is set if a non-byte-aligned flag is received. CRCE may also be set. The setting of this flag is controlled by the GSC.

RSTAT.6 (RCABT) - Receiver Collision/Abort Detect - If set, indicates that a collision was detected after data had been loaded into the receive FIFO in CSMA/CD mode. In SDLC mode, RCABT indicates that 7 consecutive ones were detected prior to the end flag but after data has been loaded into the receive FIFO. AE may also be set if RCABT is set.

RSTAT.7 (OVR) - Overrun - If set, indicates that the receive FIFO was full and new shift register data was written into it. It is cleared by user software. AE and/or CRCE may also be set if OVR is set.

SARH0 (0A3H) - Source Address Register High 0, contains the high byte of the source address for DMA Channel 0.

SARH1 (0B3H) - Source Address Register High 1, contains the high byte of the source address for DMA Channel 1.

SARL0 (0A2H) - Source Address Register Low 0, contains the low byte of the source address for DMA Channel 0.

SARL1 (0B2H) - Source Address Register Low 1, contains the low byte of the source address for DMA Channel 1.

SAS - Source Address Space bit, see DCON0.

SBUF (099H) - Serial Buffer, both the receive and transmit SFR location for the LSC.

SCON (098H)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SCON.0 (RI) - Receive Interrupt flag.

SCON.1 (TI) - Transmit Interrupt flag.

SCON.2 (RB8) - Receive Bit 8, contains the ninth bit that was received in Modes 2 and 3 or the stop bit in Mode 1 if SM20. Not used in Mode 0.

SCON.3 (TB8) - Transmit Bit 8, the ninth bit to be transmitted in Modes 2 and 3.

SCON.4 (REN) - Receiver Enable, enables reception for the LSC.

SCON.5 (SM2) - Enables the multiprocessor communication feature in Modes 2 and 3 for the LSC.

SCON.6 (SM1) - LSC mode specifier.

SCON.7 (SM2) - LSC mode specifier.

SDLC - Stands for Synchronous Data Link Communication and is a protocol developed by IBM.

SLOTTM - (0B4H) Determines the length of the slot time in CSMA/CD.

SP (081H) - Stack Pointer, an eight bit pointer register used during a PUSH, POP, CALL, RET, or RETI.

TCDCNT - (0D4H) Contains the number of collisions in the current frame if using probabilistic CSMA/CD and contains the maximum number of slots in the deterministic mode.

TCDT - Transmit Collision Detect, see TSTAT.

TCON (088H)

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TCON.0 (IT0) - Interrupt 0 mode control bit.

TCON.1 (IE0) - External interrupt 0 edge flag.

TCON.2 (IT1) - Interrupt 1 mode control bit.

TCON.3 (IE1) - External interrupt 1 edge flag.

TCON.4 (TR0) - Timer 0 run control bit.

CON.5 (TF0) - Timer 0 overflow flag.

TCON.6 (TR1) - Timer 1 run control bit.

TCON.7 (TF1) - Timer 1 overflow flag.

TDN - Transmit Done flag, see TSTAT.

TEN - Transmit Enable bit, see TSTAT.

TFNF - Transmit FIFO Not Full flag, see TSTAT.

TFIFO - (85H) TFIFO is a 3-byte FIFO that contains the transmission data for the GSC.

TH0 (08CH) - Timer 0 High byte, contains the high byte for timer/counter 0.

TH1 (08DH) - Timer 1 High byte, contains the high byte for timer/counter 1.

TI - Transmit Interrupt, see SCON.

TL0 (08AH) - Timer 0 Low byte, contains the low byte for timer/counter 0.

TL1 (08BH) - Timer 1 Low byte, contains the low byte for timer/counter 1.

TM - Transfer Mode, see, DCON0.

TMOD (089H)

7	6	5	4	3	2	1	0
GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

TMOD.0 (M0) - Mode selector bit for Timer 0.

TMOD.1 (M1) - Mode selector bit for Timer 0.

TMOD.2 (C/$\overline{T}$) - Timer/Counter selector bit for Timer 0.

TMOD.3 (GATE) - Gating Mode bit for Timer 0.

TMOD.4 (M0) - Mode selector bit for Timer 1.

TMOD.5 (M1) - Mode selector bit for Timer 1.

TMOD.6 (C/$\overline{T}$) - Timer/Counter selector bit for Timer 1.

TMOD.7 (GATE) - Gating Mode bit for Timer 1.

TSTAT (0D8) - Transmit Status Register

7	6	5	4	3	2	1	0
LNI	NOACK	UR	TCDT	TDN	TFNF	TEN	DMA

TSTAT.0 (DMA) - DMA Select - If set, indicates that DMA channels are used to service the GSC FIFO's and GSC interrupts occur on TDN and RDN, and also enables UR to become set. If cleared, indicates that the GSC is operating in it normal mode and interrupts occur on TFNE and RFNE.For more information on DMA servicing please refer to the DMA section on DMA serial demand mode (4.2.2.3).

TSTAT.1 (TEN) - Transmit Enable - When set causes TDN, UR, TCDT, and NOACK flags to be reset and the TFIFO cleared. The transmitter will clear TEN after a successful transmission, a collision during the data, CRC, or end flag. If cleared during a transmission the GSC transmit pin goes to a steady state high level. This is the method used to send an abort character in SDLC. Also $\overline{DEN}$ is forced to a high level. The end of transmission occurs whenever the TFIFO is emptied.

TSTAT.2 (TFNF) - Transmit FIFO not full - When set, indicates that new data may be written into the transmit FIFO. The transmit FIFO is a three byte buffer that loads the transmit shift register with data.

TSTAT.3 (TDN) - Transmit Done - When set, indicates the successful completion of a frame transmission. If HBAEN is set, TDN will not be set until the end of the IFS following the transmitted message, so that the acknowledge can be checked. If an acknowledge is expected and not received, TDN is not set. An acknowledge is not expected following a broadcast or multi-cast packet.

TSTAT.4 (TCDT) - Transmit Collision Detect - If set, indicates that the transmitter halted due to a collision. It is set if a collision occurs during the data or CRC or if there are more than eight collisions.

TSTAT.5 (UR) - Underrun - If set, indicates that in DMA mode the last bit was shifted out of the transmit register and that the DMA byte count did not equal zero. When an underrun occurs, the transmitter halts without sending the CRC or the end flag.

TSTAT.6 (NOACK) - No Acknowledge - If set, indicates that no acknowledge was received for the previous frame. Will be set only if HBAEN is set and no acknowledge is received prior to the end of the IFS. NOACK is not set following a broadcast or a multicast packet.

TSTAT.7 (LNI) - Line Idle - If set, indicates the receive line is idle. In SDLC protocol it is set if 15 consecutive ones are received. In CSMA/CD protocol, line idle is set if GR$\times$D remains high for approximately 1.6 bit times. LNI is cleared after a transition on GR$\times$D.

TxC - External Clock input for GSC transmitter.

UR - Underrun flag, see TSTAT.

XRCLK - External GSC Receive Clock Enable bit, see PCON.

XTCLK - External GSC Transmit Clock Enable bit, see GMOD.

8XC152JA/JB/JC/JD
UNIVERSAL COMMUNICATION CONTROLLER
8-BIT MICROCONTROLLER

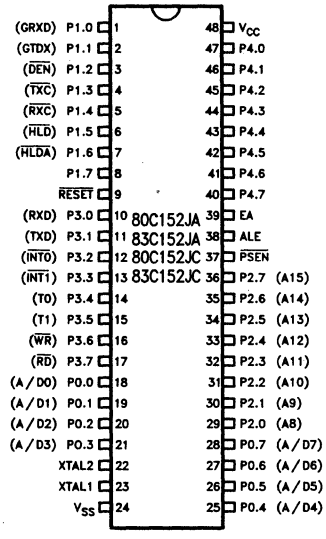
- **8K Factory Mask Programmable ROM Available**

- **Superset of 80C51 Architecture**
- **Multi-Protocol Serial Communication I/O Port (2.048 Mbps/2.4 Mbps Max)**
  - **SDLC/HDLC Only**
  - **CSMA/CD and SDLC/HDLC**
  - **User Definable Protocols**
- **Full Duplex/Half Duplex**
- **MCS®-51 Compatible UART**
- **16.5 MHz Maximum Clock Frequency**
- **Multiple Power Conservation Modes**
- **64KB Program Memory Addressing**
- **64KB Data Memory Addressing**
- **256 Bytes On-Chip RAM**
- **Dual On-Chip DMA Channels**
- **Hold/Hold Acknowledge**
- **Two General Purpose Timer/Counters**
- **5 or 7 I/O Ports**
- **56 Special Function Registers**
- **11 Interrupt Sources**
- **Available in 48 Pin Dual-in-Line Package and 68 Pin Surface Mount PLCC Package**
  (See Packaging Spec. Order #231369)

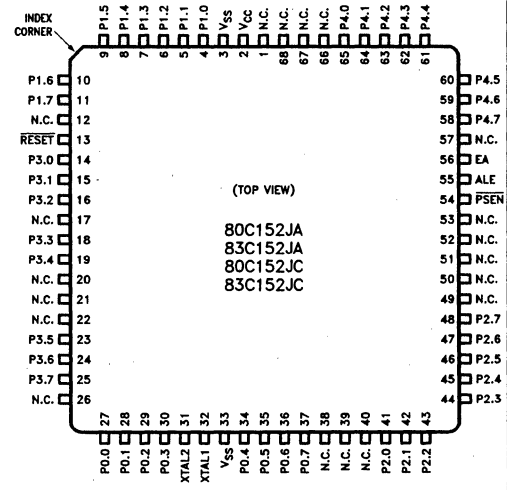
The 80C152, which is based on the MCS®-51 CPU, is a highly integrated single-chip 8-bit microcontroller designed for cost-sensitive, high-speed, serial communications. It is well suited for implementing Integrated Services Digital Networks (ISDN), emerging Local Area Networks, and user defined serial backplane applications. In addition to the multi-protocol communication capability, the 80C152 offers traditional microcontroller features for peripheral I/O interface and control.

Silicon implementations are much more cost effective than multi-wire cables found in board level parallel-to-serial and serial-to-parallel converters. The 83C152 contains, in silicon, all the features needed for the serial-to-parallel conversion. Other 83C152 benefits include: 1) better noise immunity through differential signaling or fiber optic connections, 2) data integrity utilizing the standard, designed in CRC checks, and 3) better modularity of hardware and software designs. All of these—cost, network parameter and real estate improvements—apply to 83C152 serial links between boards or systems and 83C152 serial links on a single board.

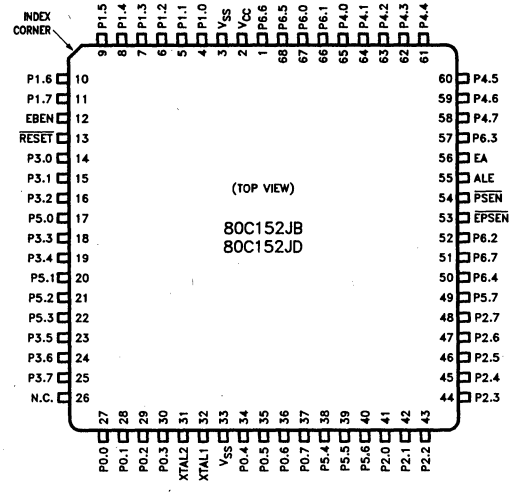
October 1989
Order Number: 270431-003



270431-1



270431-2



270431-3

Figure 1. Connection Diagrams

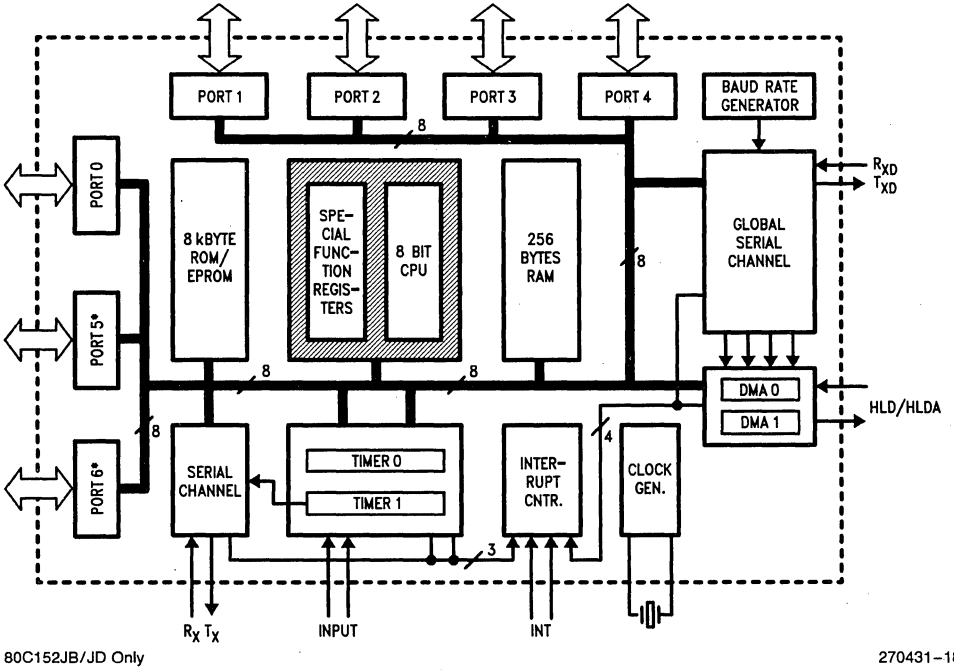


Figure 2. Block Diagram

80C152JB/JD General Description

The 80C152JB/JD is a ROMless extension of the 80C152 Universal Communication controller. The 80C152JB has the same five 8-bit I/O ports of the 80C152, plus an additional two 8-bit I/O ports, Port 5 and Port 6. The 80C152JB/JD also has two additional control pins, EBEN (**E**PROM **B**us **EN**able), and $\overline{\text{EPSEN}}$ (**E**PROM bus **P**rogram **S**tore **EN**able).

EBEN selects the functionality of Port 5 and Port 6. When EBEN is low, these ports are strictly I/O, similar to Port 4. The SFR location for Port 5 is 91H and Port 6 is 0A1H. This means Port 5 and Port 6 are not bit addressable. With EBEN low, all program memory fetches take place via Port 0 and Port 2. (The 80C152 is a ROMless only product). When EBEN is high, Port 5 and Port 6 form an address/data bus called the E-Bus (EPROM-Bus) for program memory operations.

$\overline{\text{EPSEN}}$ is used in conjunction with Port 5 and Port 6 program memory operations. $\overline{\text{EPSEN}}$ functions like $\overline{\text{PSEN}}$ during program memory operation, but supports Port 5 and Port 6. $\overline{\text{EPSEN}}$ is the read strobe to external program memory for Port 5 and Port 6. $\overline{\text{EPSEN}}$ is activated twice during each machine cycle unless an external data memory operation occurs on Port(s) 0 and Port 2. When external data memory is accessed the second activation of $\overline{\text{EPSEN}}$ is skipped, which is the same as when using $\overline{\text{PSEN}}$. Note that data memory fetches cannot be made through Ports 5 and 6.

When EBEN is high and EA is low, all program memory operations take place via Ports 5 and 6. The high byte of the address goes out on Port 6, and the low byte is output on Port 5. ALE is still used to latch the address on Port 5. Next, the op code is read on Port 5. The timing is the same as when using Ports 0 and 2 for external program memory operations.

Table 1. Program Memory Fetches

EBEN	$\overline{\text{EA}}$	Program Fetch via	$\overline{\text{PSEN}}$	$\overline{\text{EPSEN}}$	Comments
0	0	P0, P2	Active	Inactive	Addresses 0–0FFFFH
0	1	N/A	N/A	N/A	Invalid Combination
1	0	P5, P6	Inactive	Active	Addresses 0–0FFFFH
1	1	P5, P6 P0, P2	Inactive Active	Active Inactive	Addresses 0–1FFFH Addresses ≥ 2000H

Table 2. 8XC152 Product Differences

ROMless Version	CSMA/CD and HDLC/SDLC	HDLC/SDLC Only	ROM Version Available	PLCC and DIP	PLCC Only	5 I/O Ports	7 I/O Ports
80C152JA	*		*(83C152JA)	*		*	
80C152JB	*				*		*
80C152JC		*	*(83C152JC)	*		*	
80C152JD		*			*		*

NOTES:
* = options available
0 standard frequency range 3.5 MHz to 12 MHz
0 "–1" frequency range 3.5 MHz to 16.5 MHz

<table>
<tr><th colspan="2">Pin #</th><th>Pin Description</th></tr>
<tr><td>DIP</td><td>PLCC(1)</td><td></td></tr>
<tr><td>48</td><td>2</td><td>V_{CC}—Supply voltage.</td></tr>
<tr><td>24</td><td>3,33(2)</td><td>V_{SS}—Circuit ground.</td></tr>
<tr><td>18-21,
25-28</td><td>27-30,
34-37</td><td>Port 0—Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.
Port 0 is also the multiplexed low-order address and data bus during accesses to external program memory if EBEN is pulled low. During accesses to external Data Memory, Port 0 always emits the low-order address byte and serves as the multiplexed data bus. In these applications it uses strong internal pullups when emitting 1s.
Port 0 also outputs the code bytes during program verification. External pullups are required during program verification.</td></tr>
<tr><td>1-8</td><td>4-11</td><td>Port 1—Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.
Port 1 also serves the functions of various special features of the 8XC152, as listed below:
<table>
<tr><th>Pin</th><th>Name</th><th>Alternate Function</th></tr>
<tr><td>P1.0</td><td>GRXD</td><td>GSC data input pin</td></tr>
<tr><td>P1.1</td><td>GTXD</td><td>GSC data output pin</td></tr>
<tr><td>P1.2</td><td>$\overline{DEN}$</td><td>GSC enable signal for an external driver</td></tr>
<tr><td>P1.3</td><td>$\overline{TXC}$</td><td>GSC input pin for external transmit clock</td></tr>
<tr><td>P1.4</td><td>$\overline{RXC}$</td><td>GSC input pin for external receive clock</td></tr>
<tr><td>P1.5</td><td>$\overline{HLD}$</td><td>DMA hold input/output</td></tr>
<tr><td>P1.6</td><td>$\overline{HLDA}$</td><td>DMA hold acknowledge input/output</td></tr>
</table></td></tr>
<tr><td>29-36</td><td>41-48</td><td>Port 2—Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.
Port 2 emits the high-order address byte during fetches from external Program Memory if EBEN is pulled low. During accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR and DMA operations), Port 2 emits the high-order address byte. In these applications it uses strong internal pullups when emitting 1s.
During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.
Port 2 also receives the high-order address bits during program verification.</td></tr>
<tr><td>10- 17</td><td>14-16,
18, 19,
23-25</td><td>Port 3—Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.
Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:
<table>
<tr><th>Pin</th><th>Name</th><th>Alternate Function</th></tr>
<tr><td>P3.0</td><td>RXD</td><td>Serial input line</td></tr>
<tr><td>P3.1</td><td>TXD</td><td>Serial output line</td></tr>
<tr><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>P3.4</td><td>T0</td><td>Timer 0 external input</td></tr>
<tr><td>P3.5</td><td>T1</td><td>Timer 1 external input</td></tr>
<tr><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write strobe</td></tr>
<tr><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read strobe</td></tr>
</table></td></tr>
</table>

Pin Description (Continued)

Pin #		Pin Description
47-40	65-58	**Port 4**—Port 4 is an 8-bit bidirectional I/O port with internal pullups. Port 4 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 4 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. In addition, Port 4 also receives the low-order address bytes during program verification.
9	13	**$\overline{RST}$**—Reset input. A logic low on this pin for three machine cycles while the oscillator is running resets the device. An internal pullup resistor permits a power-on reset to be generated using only an external capacitor to V_{SS}. Although the GSC recognizes the reset after three machine cycles, data may continue to be transmitted for up to 4 machine cycles after Reset is first applied.
38	55	**ALE**—Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. While in Reset, ALE remains at a constant high level.
37	54	**$\overline{PSEN}$**—Program Store Enable is the Read strobe to External Program Memory. When the 8XC152 is executing from external program memory, $\overline{PSEN}$ is active (low). When the device is executing code from External Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory. While in Reset, $\overline{PSEN}$ remains at a constant high level.
39	56	**$\overline{EA}$**—External Access enable. $\overline{EA}$ must be externally pulled low in order to enable the 8XC152 to fetch code from External Program Memory locations 0000H to 0FFFH. $\overline{EA}$ must be connected to V_{CC} for internal program execution.
23	32	**XTAL1**—Input to the inverting oscillator amplifier and input to the internal clock generating circuits.
22	31	**XTAL2**—Output from the inverting oscillator amplifier.
N/A	17, 20 21, 22 38, 39 40, 49	**Port 5**—Port 5 is an 8-bit bidirectional I/O port with internal pullups. Port 5 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 5 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 5 is also the multiplexed low-order address and data bus during accesses to external program memory if EBEN is pulled high. In this application it uses strong pullups when emitting 1s.
N/A	67, 66 52, 57 50, 68 1, 51	**Port 6**—Port 6 is an 8-bit bidirectional I/O port with internal pullups. Port 6 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 6 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 6 emits the high-order address byte during fetches from external Program Memory if EBEN is pulled high. In this application it uses strong pullups when emitting 1s.
N/A	12	**EBEN**—E-Bus Enable input that designates whether program memory fetches take place via Ports 0 and 2 or Ports 5 and 6. Table 1 shows how the ports are used in conjunction with EBEN.
N/A	53	**$\overline{EPSEN}$**—E-bus Program Store Enable is the Read strobe to external program memory when EBEN is high. Table 2 shows when $\overline{EPSEN}$ is used relative to $\overline{PSEN}$ depending on the status of EBEN and $\overline{EA}$.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

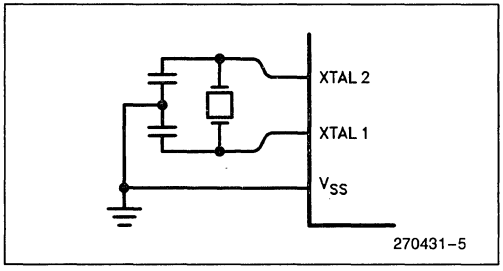


Figure 3. Using the On-Chip Oscillator

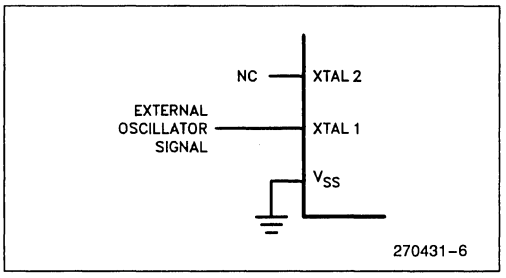


Figure 4. External Clock Drive

10

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while most of the on-chip peripherals remain active. The major peripherals that do not remain active during Idle, are the DMA channels. The Idle Mode is invoked by software. The content of the on-chip RAM and all the Special Function Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

POWER DOWN MODE

In Power Down Mode, the oscillator is stopped and all on-chip functions cease except that the on-chip RAM contents are maintained. The mode Power Down is invoked by software. The Power Down Mode can be terminated only by a hardware reset.

Table 3. Status of the External Pins During Idle and Power Down Modes

80C152JA/83C152JA/80C152JC/83C152JC

Mode	Program Memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3	Port 4
Idle	Internal	1	1	Data	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data	Data
Power Down	Internal	0	0	Data	Data	Data	Data	Data
Power Down	External	0	0†	Float	Data	Data	Data	Data

80C152JB/80C152JD

Mode	Instruction Bus	ALE	$\overline{PSEN}$	$\overline{EPSEN}$	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6
Idle	P0, P2	1	1	1	Float	Data	Address	Data	Data	0FFH	0FFH
Idle	P5, P6	1	1	1	Data	Data	Data	Data	Data	0FFH	Address
Power Down	P0, P2	0	0	1	Float	Data	Data	Data	Data	0FFH	0FFH
Power Down	P5, P6	0	1†	0	Data	Data	Data	Data	Data	0FFH	0FFH

NOTE:
For more detailed information on the reduced power modes refer to the Embedded Controller Handbook, and Application Note AP-252, "Designing with the 80C51BH."
†Note difference of logic level of $\overline{PSEN}$ during Power Down for ROM JA/JC and ROM emulation mode for JC/JD.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any pin to V_{SS} ..−0.5V to (V_{CC} + 0.5V)
Voltage on V_{CC} to VSS.....−0.5V to +6.5V
Power Dissipation .....1.0W(9)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V)

Symbol	Parameter	Min	Typ (Note 3)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (All Except $\overline{EA}$, EBEN)	−0.5		$0.2V_{CC}-0.1$	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$, EBEN)	−0.5		$0.2V_{CC}-0.3$	V	
V_{IH}	Input High Voltage (Except XTAL1, $\overline{RST}$)	$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, $\overline{RST}$)	$0.7V_{CC}$		$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3, 4, 5, 6)			0.45	V	I_{OL} = 1.6 mA (Note 4)
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$, $\overline{EPSEN}$)			0.45	V	I_{OL} = 3.2 mA (Note 4)
V_{OH}	Output High Voltage (Ports 1, 2, 3, 4, 5, 6 COMM9 ALE, $\overline{PSEN}$, $\overline{EPSEN}$)	2.4			V	I_{OH} = −60 μA V_{CC} = 5V ±10%
		$0.9V_{CC}$			V	I_{OH} = −10 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I_{OH} = −400 μA V_{CC} = 5V ±10%
		$0.9V_{CC}$			V	I_{OH} = −40 μA (Note 5)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, 4, 5, 6)			−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3, 4, 5, 6)			−650	μA	V_{IN} = 2V
I_{LI}	Input Leakage (Port 0, $\overline{EA}$)			±10	μA	$0.45<V_{IN}<V_{CC}$
RRST	Reset Pullup Resistor	40			kΩ	
I_{IH}	Logical 1 Input Current (EBEN)			+60	μA	
I_{CC}	Power Supply Current :					
	Active (16.5 MHz)		31	41.1	mA	(Note 6)
	Idle (16.5 MHz)		8	15.4	mA	(Note 6)
	Power Down Mode		10		μA	V_{CC} = 2.0V to 5.5V

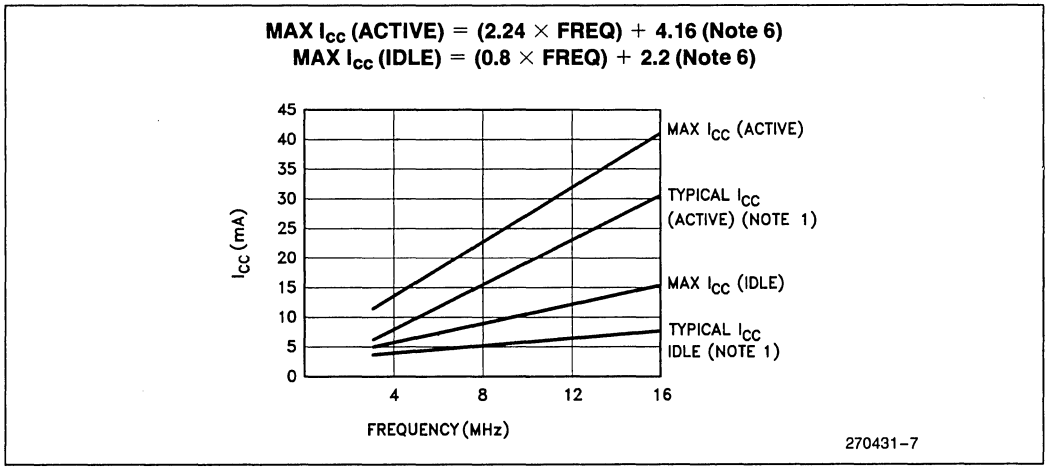


Figure 5. I_{CC} vs Frequency

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address.
C: Clock
D: Input data.
H: Logic level HIGH.
I: Instruction (program memory contents).
L: Logic level LOW, or ALE.
P: $\overline{\text{PSEN}}$.
Q: Output data.
R: $\overline{\text{READ}}$ signal.
T: Time.
V: Valid.
W: $\overline{\text{WRITE}}$ signal.
X: No longer a valid logic level.
Z: Float.

For example,

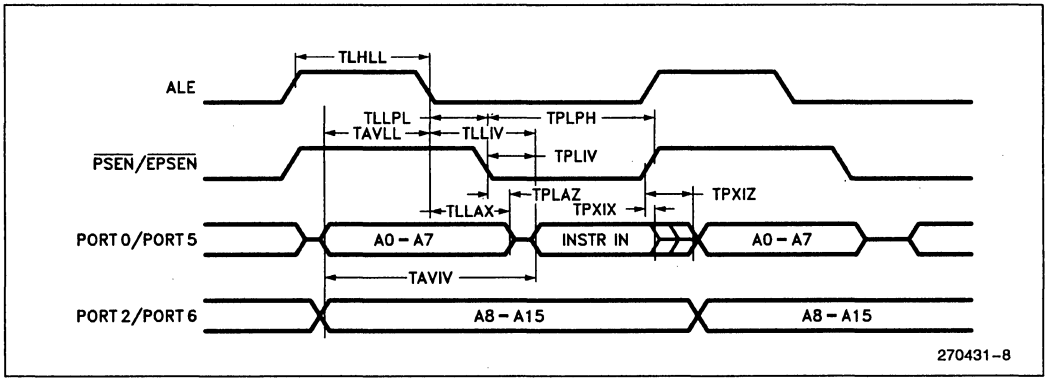
TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{\text{PSEN}}$ Low.

A.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V; Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

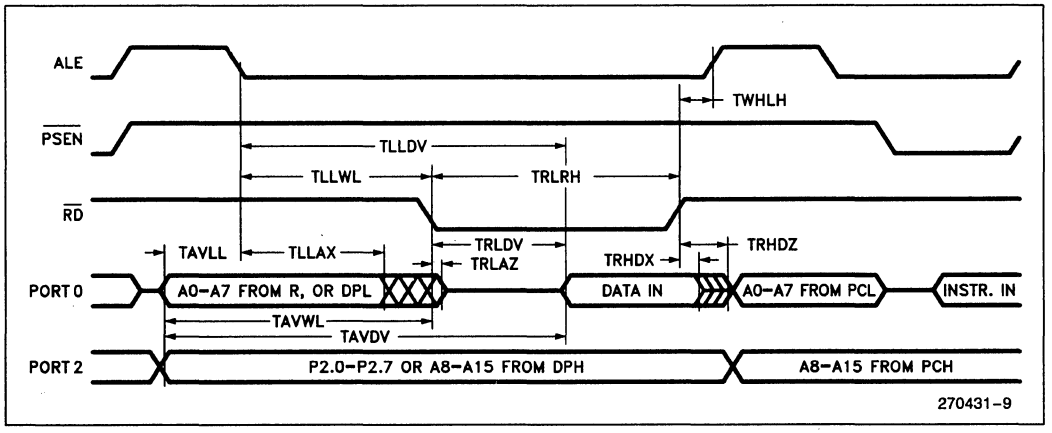
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS (Note 7, 10)

Symbol	Parameter	16.5 MHz		Variable Oscillator		Unit
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 80C152JA/JC 83C152JA/JC 80C152JB/JD			3.5	12	MHz
	80C152JA/JC-1 83C152JA/JC-1 80C152JB/JD-1			3.5	16.5	MHz
TLHLL	ALE Pulse Width	81		2TCLCL-40		ns
TAVLL	Address Valid to ALE Low	5		TCLCL-55		ns
TLLAX	Address Hold After ALE Low	25		TCLCL-35		ns
TLLIV	ALE Low to Valid Instruction In		142		4TCLCL-100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	20		TCLCL-40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	137		3TCLCL-45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		77		3TCLCL-105	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		35		TCLCL-25	ns
TAVIV	Address to Valid Instruction In		198		5TCLCL-105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	263		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	263		6TCLCL-100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		138		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		51		2TCLCL-70	ns
TLLDV	ALE Low to Valid Data In		335		8TCLCL-150	ns
TAVDV	Address to Valid Data In		380		9TCLCL-165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	132	232	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	112		4TCLCL-130		ns
TQVWX(8)	Data Valid to $\overline{WR}$ Transition	196		6TCLCL-167		ns
TWHQX	Data Hold After $\overline{WR}$	10		TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	20	100	TCLCL-40	TCLCL+40	ns

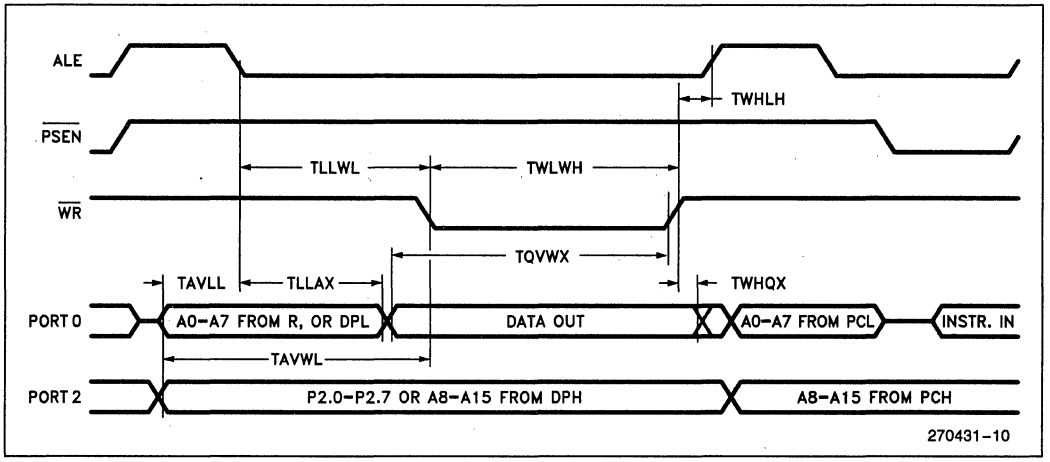
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



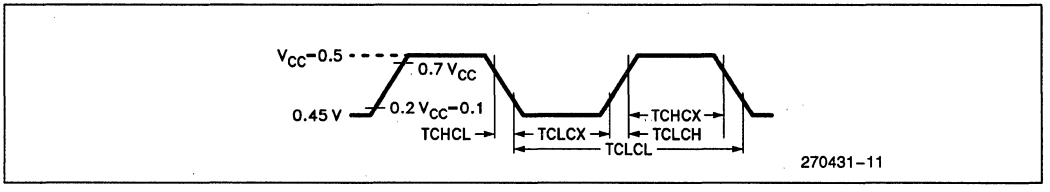
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	16.5	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

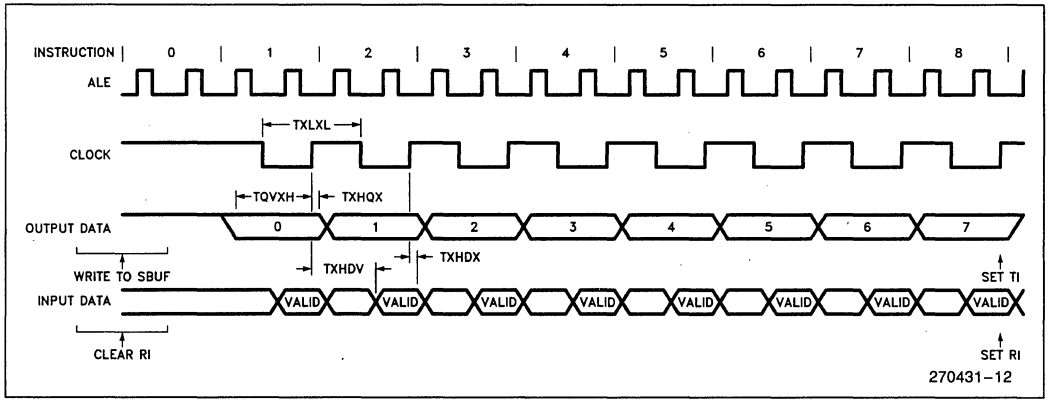
EXTERNAL CLOCK DRIVE WAVEFORM



LOCAL SERIAL CHANNEL TIMING—SHIFT REGISTER MODE

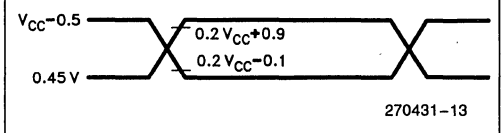
Symbol	Parameter	16.5 MHz		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	727		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	473		10TCLCL-133		ns
TXHQX	Output Data Hold After Clock Rising Edge	4		2TCLCL-117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		473		10TCLCL-133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



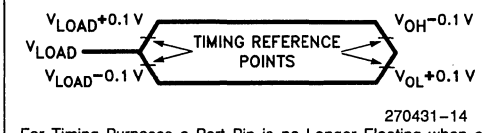
A.C. TESTING:

INPUT, OUTPUT WAVEFORMS



AC Inputs During Testing are Driven at $V_{CC}-0.5$ for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at V_{IH} Min for a Logic "1" and V_{IL} Max for a Logic "0".

FLOAT WAVEFORM

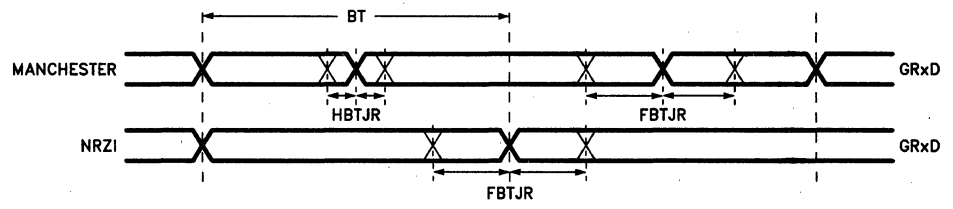


For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs, and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 20$ mA.

GLOBAL SERIAL PORT TIMINGS—Internal Baud Rate Generator

Symbol	Parameter	16.5 MHz (BAUD = 0)		Variable Oscillator		Unit
		Min	Max	Min	Max	
HBTJR	Allowable jitter on the Receiver for ½ bit time (Manchester encoding only)		0.0375		(0.125 × (BAUD+1)× 8TCLCL) −25 ns	μs
FBTJR	Allowable jitter on the Receiver for one full bit time (NRZI and Manchester)		0.10		(0.25 × (BAUD+1)× 8TCLCL) −25 ns	μs
HBTJT	Jitter of data from Transmitter for ½ bit time (Manchester encoding only)		±10		±10	ns
FBTJT	Jitter of data from Transmitter for one full bit time (NRZI and Manchester)		±10		±10	ns
DRTR	Data rise time for Receiver(11)		20		20	ns
DFTR	Data fall time for Receiver(12)		20		20	ns

GSC RECEIVER TIMINGS (INTERNAL BAUD RATE GENERATOR)



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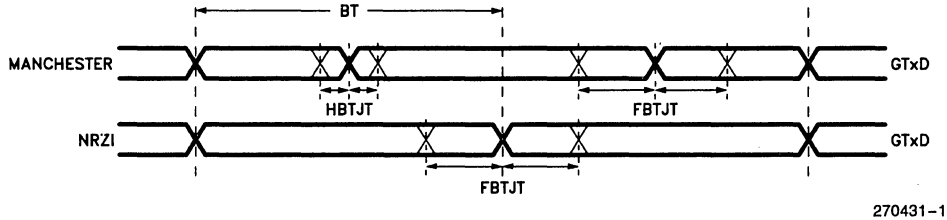
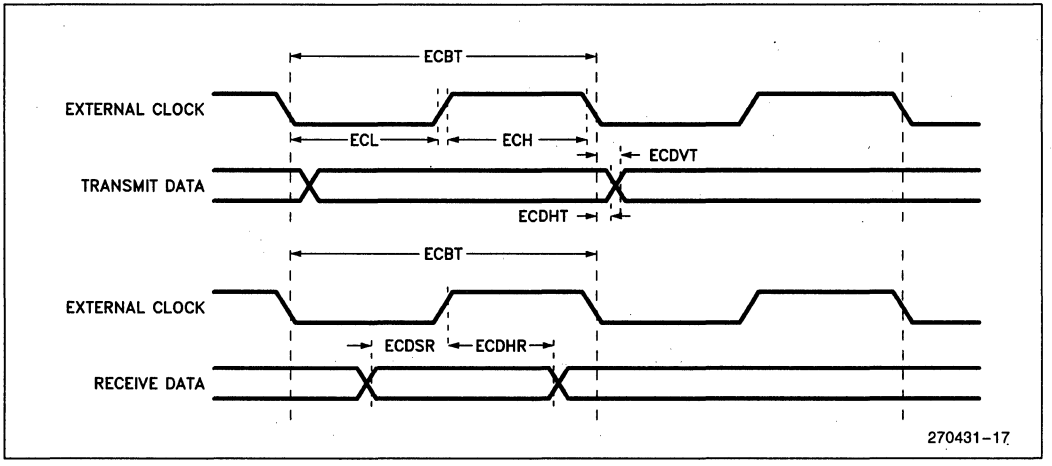
GSC TRANSMIT TIMINGS (INTERNAL BAUD RATE GENERATOR)



GLOBAL SERIAL PORT TIMINGS—External Clock

Symbol	Parameter	16.5 MHz		Variable Oscillator		Unit
		Min	Max	Min	Max	
1/ECBT	GSC Frequency with an External Clock		2.4	0.009	$F_{OSC} \times 0.145$	MHz
ECH	External Clock High	170		2TCLCL + 45 ns		ns
ECL(13)	External Clock Low	170		2TCLCL + 45 ns		ns
ECRT	External Clock Rise Time(11)		20		20	ns
ECFT	External Clock Fall Time(12)		20		20	ns
ECDVT	External Clock to Data Valid Out - Transmit (to External Clock Negative Edge)		150		150	ns
ECDHT	External Clock Data Hold - Transmit (to External Clock Negative Edge)	0		0		ns
ECDSR	External Clock Data Set-up - Receiver (to External Clock Positive Edge)	45		45		ns
ECDHR	External Clock to Data Hold - Receiver (to External Clock Positive Edge)	50		50		ns

GSC TIMINGS (EXTERNAL CLOCK)



NOTES:
1. N.C. pins on PLCC package may be connected to internal die and should not be used in customer applications.
2. It is recommended that both Pin 3 and Pin 33 be grounded for PLCC devices.
3. "Typicals" are based on samples taken from early manufacturing lots and are not guaranteed. The measurements were made with V_{CC} = 5V at room temperature.
4. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
5. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
6. I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; Port 0 pins connected to V_{CC}. "Operating" current is measured with $\overline{EA}$ connected to V_{CC} and $\overline{RST}$ connected to V_{SS}. "Idle" current is measured with $\overline{EA}$ connected to V_{SS}, $\overline{RST}$ connected to V_{CC} and GSC inactive.
7. The specifications relating to external data memory characteristics are also applicable to DMA operations.
8. TQVWX should not be confused with TQVWX as specified for 80C51BH. On 80C152, TQVWX is measured from data valid to rising edge of $\overline{WR}$. On 80C51BH, TQVWX is measured from data valid to falling edge of $\overline{WR}$. See timing diagrams.
9. This value is based on the maximum allowable die temperature and the thermal resistance of the package.
10. All specifications relating to external program memory characteristics are applicable to:
    $\overline{EPSEN}$ for $\overline{PSEN}$
    Port 5 for Port 0
    Port 6 for Port 2
    when EBEN is at a Logical 1 on the 80C152JB/JD.
11. Same as TCLCH, use External Clock Drive Waveform.
12. Same as TCHCL, use External Clock Drive Waveform.
13. When using the same external clock to drive both the receiver and transmitter, the minimum ECL spec effectively becomes 195 ns at all frequencies (assuming 0 ns propagation delay) because ECDVT (150 ns) plus ECDSR (45 ns) requirements must also be met (150 + 45 = 195 ns). The 195 ns requirement would also increase to include the maximum propagation delay between receivers and transmitters.

DESIGN NOTES

Within the 8XC152 there exists a race condition that may set both the RDN and AE bits at the end of a valid reception. This will not cause a problem in the application as long as the following steps are followed:

—Never give the receive error interrupt a higher priority than the valid reception interrupt

—Do not leave the valid reception interrupt service routine when AE is set by using a RETI instruction until AE is cleared. To clear AE set the GREN bit, this enables the receiver. If the user desires that the receiver remain disabled, clear GREN after setting it before leaving the interrupt service routine.

—If the AE bit is checked by user software in response to a valid reception interrupt, the status of AE should be considered invalid.

The race condition is dependent upon both the temperature that the device is currently operating at and the processing the device received during the wafer fabrication.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

DATA SHEET REVISION SUMMARY

The following represent the key differences between the "-003" and the "-002" version of the 80C152/83C152 data sheet. Please review this summary carefully.

1. Removed minimum GSC frequency spec when used with an external clock.
2. Change figure "External Program Memory Read Cycle" to show Port 0/Port 5 address floating after PSEN goes low.
3. Added design note on terminating idle with reset.
4. Added status of PSEN during Power Down mode to Table 3.
5. Moved all notes to back of data sheet.
6. Changed microcomputer to microcontroller.
7. Added External Oscillator start-up capacitance note.

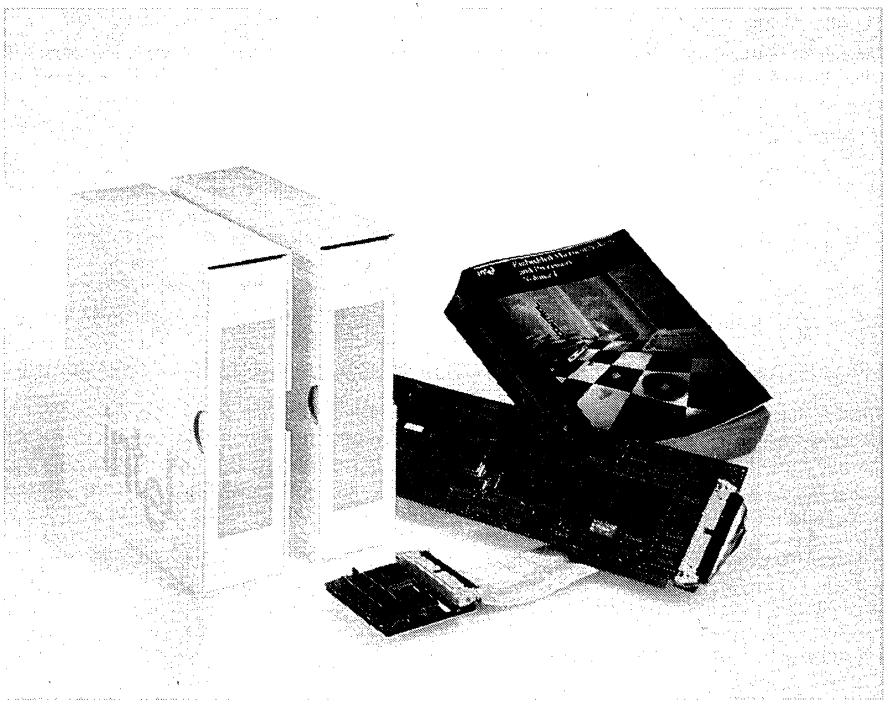
The following represent the key differences between the "-002" and the "-001" version of the 80C152/83C152 data sheet. Please review this summary carefully.

1. Status of data sheet changed from "ADVANCED" to "PRELIMINARY".
2. 80C152JC, 83C152JC, and 80C152JD were added.
3. Added AE/RDN design note.
4. This revision summary was added.
5. Note #13 was added (Effective ECL spec at higher clock rates).
6. Table #2 changed to Table #3 (Status of pins during Idle/Power Down).
7. Current Table #2 was added (JA vs. JB vs. JC vs. JD matrix).
8. Transmit jitter spec changed from ±35 ns and ±70 ns to ±10 ns.

MCS®-51 Development Support Tools

11

DEVELOPMENT TOOLS FOR THE MCS®-51 FAMILY OF MICROCONTROLLERS



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CUT COSTS, NOT CORNERS

Intel supports application development for its MCS-51 family of microcontrollers with a complete set of tools. Development Tools for the MCS-51 include in-circuit emulators, languages, and utilities.

The ICE™-51/PC in circuit emulators are easy to use, powerful, and attractive in price. A windowed user interface and source level debugging simplify use. The sophisticated event recognition features, ability to access debug information during emulation, and performance analysis functions provide debugging power.

The software development tools consist of a macro assembler, PL/M compiler, linker/relocator program, librarian utility, and object-to-hex utility. C compilers for the MCS-51 architecture are available from several vendors. Develop code in the languages you desire, then combine object modules from different languages into a single, fast program. These tools were designed to work with each other, with the MCS-51 architecture, and with the Intel line of MCS-51 emulators.

September 1992
Order Number: 281424-001

FEATURES

FEATURES

Software Support Tools
- ASM-51 macro assembler
- PL/M-51 high-level language
- Linker/relocator program
- Librarian Utility
- Object to hexadecimal converter
- Hosted on IBM PC XT/AT running DOS V 3.0 or later
- Worldwide service and support

Emulator Family
- Color windowed user interface
- Source level debugging with symbolic referencing and display
- Recognition of internal data write, external data read/write, instruction fetch, execution address, external input line state, and trace buffer full events
- AND/OR combination of events
- Qualification of an event by number of occurrences
- Arming of an event conditional on the occurrence of another event
- Access to microcontroller contents/memory during emulation
- 4096 frame trace buffer accessible during emulation
- Emulation and event timers for performance analysis
- User-definable debug and test procedures with variables and literal definitions
- Mappable emulator memory: 64 Kbytes code plus 64 Kbytes xdata
- On-circuit emulation of surface mounted components
- Four input logic pins to capture external events
- Supports component speeds up to 20 MHz

ICE™-51/PC

For ease of use and learning, the ICE-51/PC emulators feature a windowed interface. Each window, such as Memory, Source, Register, and Watch (user variable display), presents a different view of the system. A Custom Window allows a user-defined function. Within each window, option menus, pop-up fill-in-the-blank forms, and scroll keys control the view. Windows may be added, sized, zoomed to full screen, or completely removed.

Pull down menus and function keys streamline emulator use by providing convenient access to common functions. The Command Line Window provides the power user with the most efficient access to all emulator functions.

Augmenting command entry is a syntax guide and recall/editing of prior commands. Of course, command syntax is compatible with prior non-windowed Intel emulators.

Help is at your fingertips. One keystroke pops up the help menu. Help is available for a variety of topics, including emulator commands, window operation, function keys, pull-down menus, and error messages. In addition, a Key Reference Line displays a list of the currently active function keys as well as brief help text for menus and forms.

Source Level Debugging

Source level debugging features complement the windowed user interface. For example, simply use a pull-down menu to load the program. Breakpoints are set by highlighting a line of code within the Source Window and pressing a function key. Set trace specifications through the pop-up fill-in-the-blank form in the Trace Window. And with the current execution point and breakpoints highlighted in color, press a function key to begin emulation.

Scroll to another line in the Source Window and press a function key to execute to that point, bypassing yet retaining the previously set breakpoints. From there, use a pull-down menu to add a variable, referenced symbolically, to the Watch Window. With each press of another function key the program is executed one source line at a time and the Watch Window display is updated.

Source statements and symbolic information are also displayed when memory is disassembled (in the Memory Window) or within the trace buffer (in the Trace Window).

Event Recognition and Trace

To speed the debugging process, the ICE-51/PC user has access to sophisticated event recognition capabilities. Internal data write, external data read/write, instruction fetch, execution address, external input line state, and trace buffer full events may be used as triggers. Compound triggers may be constructed through AND/OR combinations of events. The recognition of an event may be armed based on the occurrence of another event. Events may be further qualified by a number of occurrences. Since this sophistication may lead to complex break/trace definitions, four Break Registers are available to store definitions for reuse.

SPECIFICATIONS

The Fastbreaks feature of the ICE-51/PC emulators allows the user to execute emulator commands with minimal intrusion on emulation. Fastbreaks are typically used for accesses to microcontroller contents or memory. A Fastbreak halts emulation, performs the requested memory access, resumes emulation, and reports back to the user. Emulation is halted only for the few machine cycles necessary to perform the access.

Similarly, the trace buffer is accessible during emulation. The buffer produces 4096 frames of execution address, opcode in hex and mnemonic formats, operands in hex and symbolic formats, bus activity, external line (clips) states, and source code.

To aid performance analysis, an event timer records the time from/to specified events while an emulation timer records the total duration of emulation.

Genuine Intel Tools

The ICE-51/PC provides the most comprehensive support for the Intel MCS-51 family of microcontrollers. When you trust your component selection to Intel, why trust its emulation to someone else? And the ICE-51/PC emulators work better because they work together with products such as C compilers, from leading independent software vendors as well as Intel's own software tools.

Emulator Electrical Characteristics

The AC characteristics for all pins except P0, P2, ALE, and PSEN# are maintained with a maximum capacitive target load 15 pF less than specified in the component data sheet for the 8xC51GB.

The AC timing degradations for P0, P2, ALE, and PSEN# are maintained with a maximum capacitive target load of 70 pF.

The maximum rise and fall times for ALE and PSEN# with a target load of 20 pF are 7 ns and 2 ns respectively.

The maximum rise and fall times for P0 and P2 with a target load of 50 pF are 27 ns and 10 ns respectively. Rise and fall times are specified at the 10% and 90% points.

The emulation processor requires 2 to 3 clock cycles longer to respond to reset.

For external program memory characteristics involving RD# and WR#, observe the following degradations:

- Setup time to RD# is 11 ns longer (max.).
- It takes 30 ns longer for data to appear on the bus with respect to WR# (max.).
- The falling edges of RD# and WR# can be delayed by 70 ns (max.).

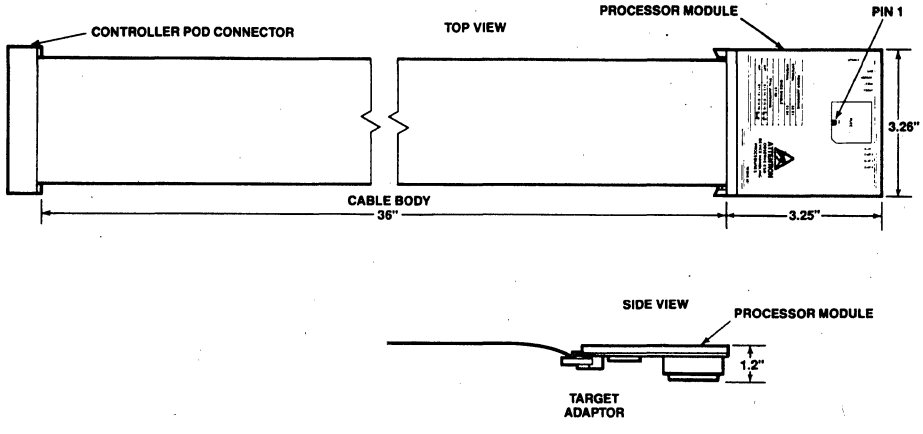
Table C-1 shows the characteristics for external program memory.

Table C-1. External Program Memory Characteristics

Symbol	Parameter	Minimum	Maximum	Units
T_{AVLL}	Address Valid to ALE Low	$0.85\,T_{CLCL} - 19$		ns
T_{LLAX}	Address Hold after ALE Low	10		ns
T_{LLIV}	ALE Low to Valid Instruction In		$3.15\,T_{CLCL} - 18$	ns
T_{LLPL}	ALE Low to PSEN# Low	$0.85\,T_{CLCL} - 1$		ns
T_{PLIV}	PSEN# Low to Valid Instruction In		$2.15\,T_{CLCL} - 18$	ns
T_{PXIZ}	Input Instr Float after PSEN#		24	ns
T_{PXAV}	PSEN# to Address Valid	$T_{CLCL} + 20$		ns
T_{AVIV}	Address to Valid Instruction In		$4.15\,T_{CLCL} - 66$	ns
T_{PLAZ}	PSEN# Low to Address Float		4	ns
T_{LLDV}	ALE Low to Valid Data In		$7.15\,T_{CLCL} - 18$	ns
T_{AVDV}	Address to Valid Data In		$8.15\,T_{CLCL} - 66$	ns

Note: # indicates active-low logic.

SPECIFICATIONS



Note: Processor module dimensions will vary for the ICE-51FX/PC.

Figure 1: Processor Module Dimensions

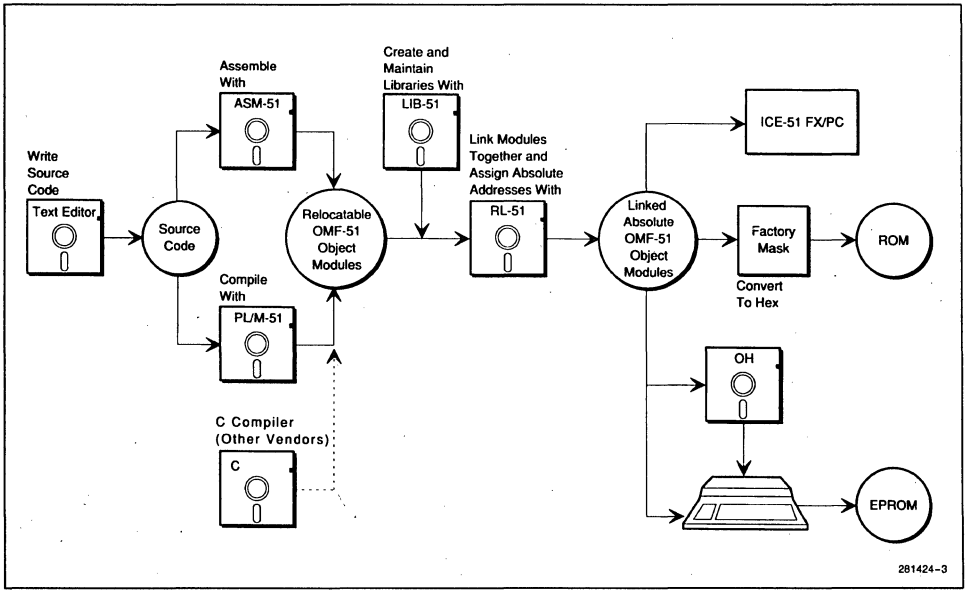


Figure 2: MCS®-51 Application Development Process

SPECIFICATIONS

ASM-51 Macro Assembler

The ASM-51 Macro Assembler provides full and accurate support for the MCS-51 family of microcontrollers. Symbolic access to the many features of the component, an "include" file with appropriate component registers, and memory space definition are a few of the features of the assembler. With the macro facility of ASM-51 common code sequences need only be developed once, saving time in both development and maintenance.

PL/M-51 Compiler

PL/M-51 is a high-level language designed to support the software requirements of the MCS-51 family of microcontrollers. The PL/M-51 compiler translates PL/M high-level language statements into MCS-51 relocatable object code. Major features of the PL/M-51 compiler include:

- Structured programming for ease of maintenance and enhancement. The PL/M-51 language supports modular and structured programming, making programs easier to understand, maintain, and debug.
- Data types to facilitate a variety of common functions. PL/M-51 supports three data types to facilitate various arithmetic, logic, and address functions. The language also uses BASED variables that map more than one variable to the same memory location to save memory space.
- Interrupt attribute to speed coding effort. The INTERRUPT attribute allows you to easily define interrupt handling procedures. The compiler will generate code to save and restore the program status word for INTERRUPT procedures.
- Code optimization for minimizing memory requirements. The PL/M-51 compiler has four different levels of optimization for significantly reducing the size of programs.
- Language compatibility for faster development. PL/M-51 object modules are compatible with object modules generated by all other MCS-51 language translators. This compatibility allows for easy linking of all modules and the ability to do symbolic debugging with the Intel MCS-51 In-Circuit Emulators.

RL-51 Linker/Relocator

Intel's RL-51 utility is used to link multiple MCS-51 object modules into a single program, resolve all references between modules and assign absolute addresses to all relocatable segments. Modules can be written in either ASM-51 or PL/M-51.

LIB-51

The Intel LIB-51 utility creates and maintains libraries of software object modules. Standard modules can be placed in a library and linked to your application programs using RL-51. When using libraries, the linker will link only those modules that are required to satisfy external references.

OH Object to Hexidecimal Converter

The OH utility converts Intel OMF-51 object modules into standard hexidecimal format. This allows the code to be loaded directly into PROM via non-Intel PROM programmers.

Third Party Vendor Tools for MCS®-51

The MCS-51 architecture is supported by a growing number of vendors providing C language compilers. The following vendors provide C language compilers for the Intel MCS-51 Architecture.

Archimedes Software, Inc 415-567-4010 (U.S.)

RSO Tasking 617-894-7800 (U.S.), 31-33-55-8584 (Europe)

Franklin Software, Inc 408-296-8051 (U.S.)

IAR 46-18-15-7920 (Europe)

Microtec Research, Inc 408-980-1300 (U.S.)

Worldwide Service, Support, and Training

To augment its development tools, Intel offers field application engineering expertise and hotline technical support.

Intel also offers a Software Support Contract which includes technical software information, automatic distributions of software and documentation updates, *iCOMMENTS* publication, remote diagnostic software, and a development tools troubleshooting guide.

Intel's 90-day Hardware Support package includes technical hardware information, telephone support, warranty on parts, labor, material, and on-site hardware support.

Intel Development Tools also offers a 30-day, money-back guarantee to customers who are not satisfied after purchasing any Intel development tool.

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SPECIFICATIONS

Configuration and Ordering Information

The ICE-51/PC emulator utilizes an IBM PC XT, PC AT, or compatible personal computer with hard disk drive, 640 Kbytes of memory, and DOS 3.3 or 5.0 as the host system. Emulator host software is provided on both 5.25 and 3.5 inch flexible disk media.

The ICE-51/PC emulators utilize a common emulation controller card with interchangeable target interface boards (TIB). An ICE-51FX/PC may be converted to support the 87C51GB microcontroller by installing a probe kit. Likewise, an ICE-51GX/PC may be converted to an ICE-51FX/PC by installing a probe kit.

A Crystal Power Accessory (CPA) is optionally available for testing the TIB to target system connection. Standalone software execution does not require a CPA.

Emulator Kits

pICE51FXPC ICE-51FX/PC emulator kit. Contains all required emulator hardware and software to execute stand-alone or in-target. Kit includes emulation controller board (8-bit, PC-card form factor), 36" cable (connects controller to probe), target probe fitted with a 40-pin male DIP adapter, and a 44-lead PLCC target adapter. Supports the following components:

1) 8031	9) 80C31BH-1	16) 80C51FA	23) 8752BH
2) 8031AH	10) 80C31BH-2	17) 80C52	24) 87C51
3) 8032AH	11) 80C32	18) 83C51FA	25) 87C51-1
4) 8051	12) 80C51BH	19) 83C51FB	26) 87C51-2
5) 8051AH	13) 80C51BH-1	20) 8751BH	27) 87C51FA
6) 8051AHP	14) 80C51BH-2	21) 8751H	28) 87C51FB
7) 8052AH	15) 80C51BHP	22) 8751H-8	29) 87C51FC
8) 80C31BH			

pICE51GXPC ICE-51GX/PC emulator kit. Contains all required emulator hardware and software to execute stand-alone or in-target. Kit includes emulation controller board (8-bit, PC-card form factor), 36" cable (connects controller to probe), and target probe fitted with a 68-lead male PLCC adapter. Supports 87C51GB components (MCS-51 microcontrollers with on-chip A/D).

Note: 1. PC host software is delivered on 5 ¼" (360 KB) and 3 ½" (720 KB) diskettes
2. Emulator kits do NOT include a CPA (Crystal Power Accessory)

pICE51FXCPA Crystal Power Accessory for ICE-51FX/PC (used to run confidence tests on probe's pin circuitry)

pICE51GXCPA Crystal Power Accessory for ICE-51GX/PC (used to run confidence tests on probe's pin circuitry)

Upgrade Kits

pICE51FXPROBE Conversion kit for existing ICE-51GX/PC emulators (kit includes FX target probe and PC host software)

pICE51GXPROBE Conversion kit for existing ICE-51FX/PC emulators (kit includes GX target probe and PC host software)

Target Adapter

HADPTONC44PLCC target: 44-lead PLCC components (surface-mounted)

Software Tools

D86PLM51NL DOS-hosted PL/M cross-compiler. Language features allow direct architecture access. Optimized for real-time, embedded applications.

D86ASM5INL DOS-hosted macro assembler. Supports all MCS-51 components.

Note: All software tool packages include a relocator/linker (RL-51), an object-to-hex converter (OH), and a librarian (LIB-51).

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ACE51™Fx SOFTWARE

To order ACE51™Fx Software, contact your local Intel Sales Office.

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270865-1

ACE51 ™Fx SOFTWARE MAKES YOU AN ARCHITECTURAL WIZARD—INSTANTLY

If you want to learn 80C51Fx architecture as fast as possible, so that you can develop hardware and software in parallel, Intel has the perfect solution. We call it ACE51™Fx Software.

PC-BASED SOFTWARE TRAINING SPEEDS LEARNING

ACE51™Fx Software is a PC-Based Expert System that uses artificial intelligence technology to guide you through detailed product training.

Its menu-driven software is designed to speed up your learning curve—and reduce your total design time, no matter what level of MCS-51 experience you have. ACE51™Fx software includes:

- A Hypertext Manual
- Peripheral Design Modules
- Application Development Modules

It uses "Hypertext" to efficiently present 80C51Fx documentation by providing highlighted links to related topics. You can follow these links several layers into the documentation—without having to search through hundreds of cross-referenced pages.

CONCENTRATE ON APPLICATIONS INSTEAD OF BIT-BY-BIT PROGRAMMING

After learning the basics of the architecture, you can use the ACE51™Fx design module to program peripherals. So, you can concentrate on application needs versus bit-by-bit programming materials. You'll save design time and minimize programming errors.

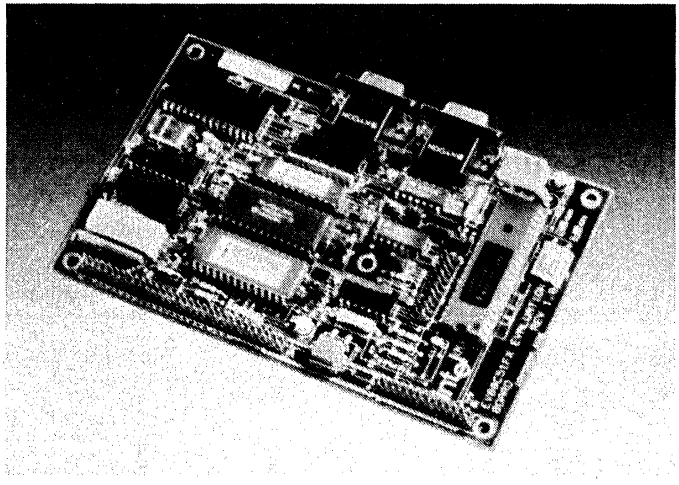
Also, ACE51™Fx Software generates fully commented initialization code and features scoreboards to document just how each peripheral has been programmed. The application development modules provide examples of generating customized code for the Programmable Counter Array (PCA). Application examples include High-Speed Outputs, Software Timers, and measurement of frequency, duty cycle, pulse width and phase differences.

System requirements: IBM compatible XT or AT**, EGA Monitor, hard disk, 1.2 meg floppy drive, 640K memory.

*IBM PC, XT, AT and DOS are registered trademarks of International Business Machines Corporation.

March 1991
Order Number: 270865-002

EV80C51FX EVALUATION BOARD



270972-1

LOW COST CODE EVALUATION TOOL

Intel's EV80C51FX evaluation board provides a hardware environment for code execution and software debugging at a relatively low cost. The board features the 80C51FC, single chip, CHMOS*, 8-bit microcontrollers, the newest member of the industry standard 8051 family. The board allows the user to take full advantage of the power of the 8051. The EV80C51FX provides up to 16 MHz execution of a user's code. Plus, its memory (ROMsim) can be reconfigured to match the user's planned memory system, allowing for exact analysis of code execution speeds in a particular application.

Popular features such as a single line assembler/disassembler, single-step program execution and sixteen software breakpoints are standard on the EV80C51FX. Intel provides a complete code development environment using assembly language (ASM-51) as well as Intel's high-level language PL/M-51 to accelerate development schedules.

The evaluation board is hosted on an IBM PC** or BIOS-compatible clone, already a standard development solution in most of today's engineering environments. The source code for the on-board monitor (written in ASM-51) is public domain. The program is about 3 Kbytes and can be easily modified to be included in the user's target hardware. In this way, the provided PC host software can be used throughout the development phase.

EV80C51FX FEATURES

- Up to 16 MHz Execution Speed
- 32 Kbytes of ROMsim
- Flexible Chip-Select Controller
- Totally CMOS, Low Power Board
- Concurrent Interrogation of Memory and Registers
- Sixteen Software Breakpoints
- Program Step Mode
- High-Level Language Support
- Single Line Assembler/Disassembler
- RS-232-C Communication Link

*CHMOS is patented Intel process.
**IBM PC®, XT, AT and DOS are registered trademarks of International Business Machines Corporation.

August 1991
Order Number: 270972-001

EV80C51FX EVALUATION BOARD

FULL SPEED EXECUTION

The EV80C51FX executes the user's code from on-board ROMsim at up to 16 MHz. By changing crystals on the 80C51FC, any slower execution speed can be evaluated. The board's host interface timing is not affected by this crystal change.

32 KBYTES OF ROMSIM

The board comes with 32 Kbytes of SRAM to be used as ROMsim for the user's code and as data memory if needed.

FLEXIBLE MEMORY DECODING

By changing the Programmable Logic Device (PLD) on the board, the memory on the board can be made to look like the memory system planned for the user's hardware application. The PLD controls the chip-select inputs on the board with 128 byte boundaries of resolution.

TOTALLY CMOS BOARD

The EV80C51FX board is built totally with CMOS components. Its power consumption is therefore very low, requiring 5V at only 225 mA. If the on board LEDs are disabled, the current drops to only 80 mA. The board also requires ±12V at 10 mA.

CONCURRENT INTERROGATION OF MEMORY AND REGISTERS

The monitor for the EV80C51FX allows the user to read and modify internal registers and external memory while the user's code is running in the board.

SIXTEEN SOFTWARE BREAKPOINTS

There are sixteen breakpoints available which automatically substitute an LCALL instruction for a user's instruction at the breakpoint location. The substitution occurs when execution is started. If the code is halted or a breakpoint is reached, the user's code is restored in the ROMsim.

PROGRAM STEP MODE

The stepping mode redirects the external interrupt 1 vector for use by the monitor. All other interrupts are available to the user, and will function as normal.

HIGH-LEVEL LANGUAGE SUPPORT

The host software for the EV80C51FX board is able to load absolute object code generated by ASM-51, PL/M-51 or RL-51, all of which are available from Intel.

SINGLE LINE ASSEMBLER/DISASSEMBLER

The host has a Single Line Assembler, and a Disassembler, to simplify modification and examination of code loaded on the board.

RS-232-C COMMUNICATION LINK

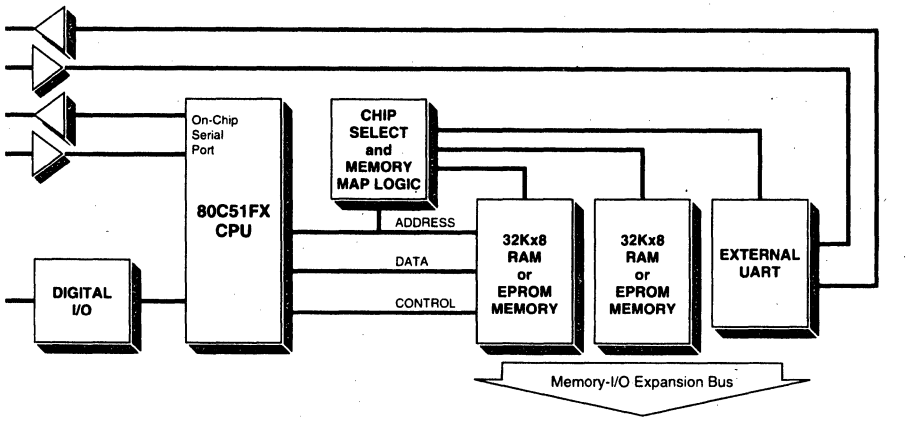
The EV80C51FX communicates with the host using an Intel 82510 UART provided on board. This frees the on-chip UART of the 80C51FC; or for the user's application.

PERSONAL COMPUTER REQUIREMENTS

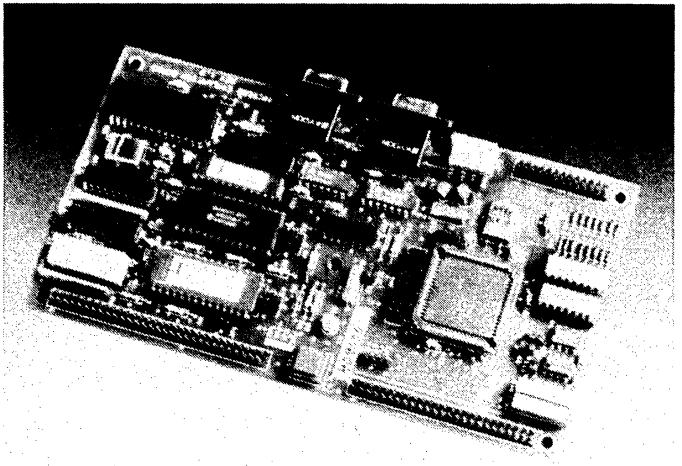
The EV80C51FX Evaluation Board is hosted on an IBM PC**, XT**, AT** or BIOS compatible clone. The PC must meet the following minimum requirements.

- 512 Kbytes of Memory
- One 360 Kbyte floppy Disk Drive
- PC DOS** 3.1 or Later
- A Serial Port (COM1 or COM2) at 9600 Baud
- ASM-51 or PL/M-51
- A text editor such as AEDIT

EV80C51FX EVALUATION BOARD



EV80C51GX EVALUATION BOARD



270974-1

11

LOW COST CODE EVALUATION TOOL

Intel's EV80C51GX evaluation board provides a hardware environment for code execution and software debugging at a relatively low cost. The board features the 80C51GB, single chip, CHMOS*, 8-bit microcontrollers, the newest member of the industry standard 8051 family. The board allows the user to take full advantage of the power of the 8051. The EV80C51GX provides up to 16 MHz execution of a user's code. Plus, its memory (ROMsim) can be reconfigured to match the user's planned memory system, allowing for exact analysis of code execution speeds in a particular application.

Popular features such as a single line asembler/disassembler, single-step program execution and sixteen software breakpoints are standard on the EV80C51GX. Intel provides a complete code development environment using assembly language (ASM-51) as well as Intel's high-level language PL/M-51 to accelerate develpment schedules.

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EV80C51GX FEATURES

- Up to 16 MHz Execution Speed
- 32 Kbytes of ROMsim
- Flexible Chip-Select Controller
- Totally CMOS, Low Power Board
- Concurrent Interrogation of Memory and Registers
- Sixteen Software Breakpoints
- Program Step Mode
- High-Level Language Support
- Single Line Assembler/Disassembler
- RS-232-C Communication Link

*CHMOS is a patented Intel process.
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June 1991
Order Number: 270974-001

EV80C51GX EVALUATION BOARD

FULL SPEED EXECUTION

The EV80C51GX executes the user's code from on-board ROMsim at up to 16 MHz. By changing crystals on the 80C51GB any slower execution speed can be evaluated. The board's host interface timing is not affected by this crystal change.

32 KBYTES of ROMSIM

The board comes with 32 Kbytes of SRAM to be used as ROMsim for the user's code and as data memory if needed.

FLEXIBLE MEMORY DECODING

By changing the Programmable Logic Device (PLD) on the board, the memory on the board can be made to look like the memory system planned for the user's hardware application. The PLD controls the chip-select inputs on the board with 128 byte boundaries of resolution.

TOTALLY CMOS BOARD

The EV80C51GX board is built totally with CMOS components. Its power consumption is therefore very low, requiring 5V at only 250 mA. If the on board LEDs are disabled, the current drops to only 80 mA. The board also requires ±12V at 10 mA.

CONCURRENT INTERROGATION OF MEMORY AND REGISTERS

The monitor for the EV80C51GX allows the user to read and modify internal registers and external memory while the user's code is running in the board.

SIXTEEN SOFTWARE BREAKPOINTS

There are sixteen breakpoints available which automatically substitute an LCALL instruction for a user's instruction at the breakpoint location. The substitution occurs when execution is started. If the code is halted or a breakpoint is reached, the user's code is restored in the ROMsim.

PROGRAM STEP MODE

The stepping mode redirects the external interrupt 1 vector for use by the monitor. All other interrupts are available to the user, and will function as normal.

HIGH-LEVEL LANGUAGE SUPPORT

The host software for the EV80C51GX board is able to load absolute object code generated by ASM-51, PL/M-51 or RL-51, all of which are available from Intel.

SINGLE LINE ASSEMBLER/DISASSEMBLER

The host has a Single Line Assembler, and a Disassembler, to simplify modification and examination of code loaded on the board.

RS-232-C COMMUNICATION LINK

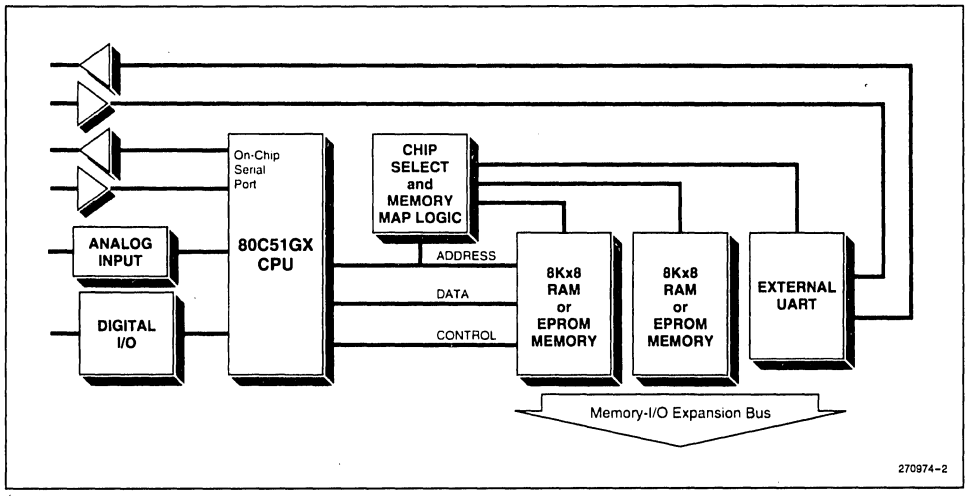
The EV80C51GX communicates with the host using an Intel 82510 UART provided on board. This frees the on-chip UART of the 80C51FC; or for the user's application.

PERSONAL COMPUTER REQUIREMENTS

The EV80C51GX Evaluation Board is hosted on an IBM PC**, XT**, AT** or BIOS compatible clone. The PC must meet the following minimum requirements:

- 512 Kbytes of Memory
- One 360 Kbyte Floppy Disk Drive
- PC DOS** 3.1 or Later
- A Serial Port (COM1 or COM2) at 9600 Baud
- ASM-51 or PL/M-51
- A text editor such as AEDIT

EV80C51GX EVALUATION BOARD



RUPI-44 Family

12

intel®

October 1988

12

The RUPI™-44 Family: Microcontroller with On-Chip Communication Controller

Order Number: 296163-001

THE RUPI™-44 FAMILY: MICROCONTROLLER WITH ON-CHIP COMMUNICATION CONTROLLER

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INTRODUCTION

The RUPI-44 family is designed for applications requiring local intelligence at remote nodes, and communication capability among these distributed nodes. The RUPI-44 integrates onto a single chip Intel's highest performance microcontroller, the 8051-core, with an intelligent and high performance Serial communication controller, called the Serial Interface Unit, or SIU. See Figure 1. This dual controller architecture allows complex control and high speed data communication functions to be realized cost effectively.

The RUPI-44 family consists of three pin compatible parts:

- 8344—8051 Microcontroller with SIU
- 8044—An 8344 with 4K bytes of on-chip ROM program memory
- 8744—An 8344 with 4K bytes of on-chip EPROM program memory

1.0 ARCHITECTURE OVERVIEW

The 8044's dual controller architecture enables the RUPI to perform complex control tasks and high speed communication in a distributed network environment.

The 8044 microcontroller is the 8051-core, and maintains complete software compatibility with it. The microcontroller contains a powerful CPU with on-chip peripherals, making it capable of serving sophisticated real-time control applications such as instrumentation, industrial control, and intelligent computer peripherals. The microcontroller features on-chip peripherals such as two 16-bit timer/counters and 5 source interrupt capability with programmable priority levels. The microcontroller's high performance CPU executes most instructions in 1 microsecond, and can perform an 8 × 8 multiply in 4 microseconds. The CPU features a Boolean processor that can perform operations on 256 directly addressable bits. 192 bytes of on-chip data RAM can be extended to 64K bytes externally. 4K bytes of on-chip program ROM can be extended to 64K bytes externally. The CPU and SIU run concurrently. See Figure 2.

The SIU is designed to perform serial communications with little or no CPU involvement. The SIU supports data rates up to 2.4 Mbps, externally clocked, and 375 Kbps self clocked (i.e., the data clock is recovered by an on-chip digital phase locked loop). SIU hardware supports the HDLC/SDLC protocol: zero bit insertion/deletion, address recognition, cyclic redundancy check, and frame number sequence check are automatically performed.

The SIU's Auto mode greatly reduces communication software overhead. The AUTO mode supports the SDLC Normal Response Mode, by performing secondary station responses in hardware without any CPU involvement. The Auto mode's interrupt control and frame sequence numbering capability eliminates software overhead normally required in conventional systems. By using the Auto mode, the CPU is free to concentrate on real time control of the application.

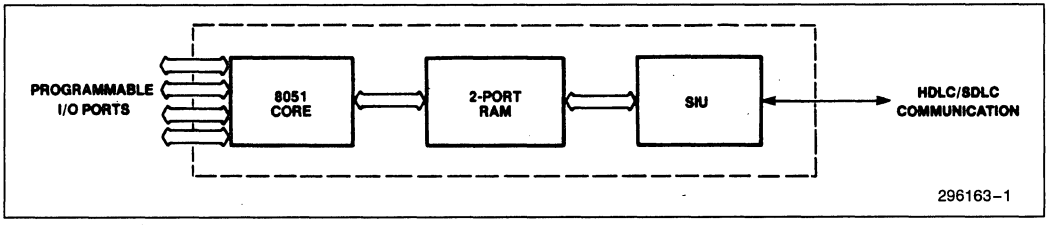

Figure 1. RUPI™-44 Dual Controller Architecture

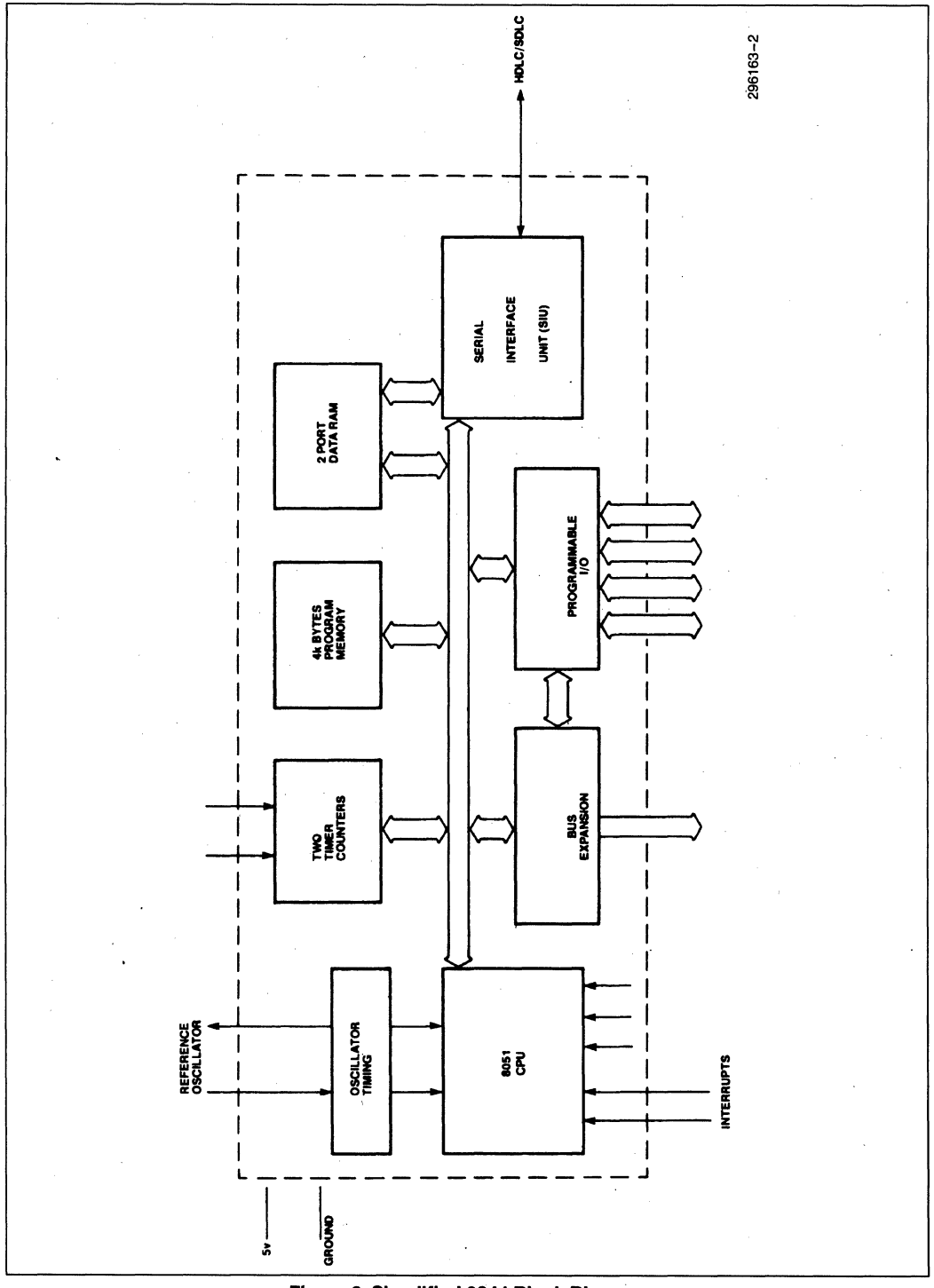

Figure 2. Simplified 8044 Block Diagram

2.0 THE HDLC/SDLC PROTOCOLS

2.1 HDLC/SDLC Advantages over Async

The High Level Data Link Control, HDLC, is a standard communication link control established by the International Standards Organization (ISO). SDLC is a subset of HDLC.

HDLC and SDLC are both well recognized standard serial protocols. The Synchronous Data Link Control, SDLC, is an IBM standard communication protocol. IBM originally developed SDLC to provide efficient, reliable and simple communication between terminals and computers.

The major advantages of SDLC/HDLC over Asynchronous communications protocol (Async):

- SIMPLE: Data Transparency
- EFFICIENT: Well Defined Message-Level Operation
- RELIABLE: Frame Check Sequence and Frame Numbering

The SDLC reduces system complexity. HDLC/SDLC are "data transparent" protocols. Data transparency means that an arbitrary data stream can be sent without concern that some of the data could be mistaken for a protocol controller. Data transparency relieves the communication controller having to detect special characters.

SDLC/HDLC provides more data throughout than Async. SDLC/HDLC runs at Message-level Operation which transmits multiple bytes within the frame, whereas Async is based on character-level operation. Async transmits or receives a character at a time. Since Async requires start and stop bits in every transmission, there is a considerable waste of overhead compared to SDLC/HDLC.

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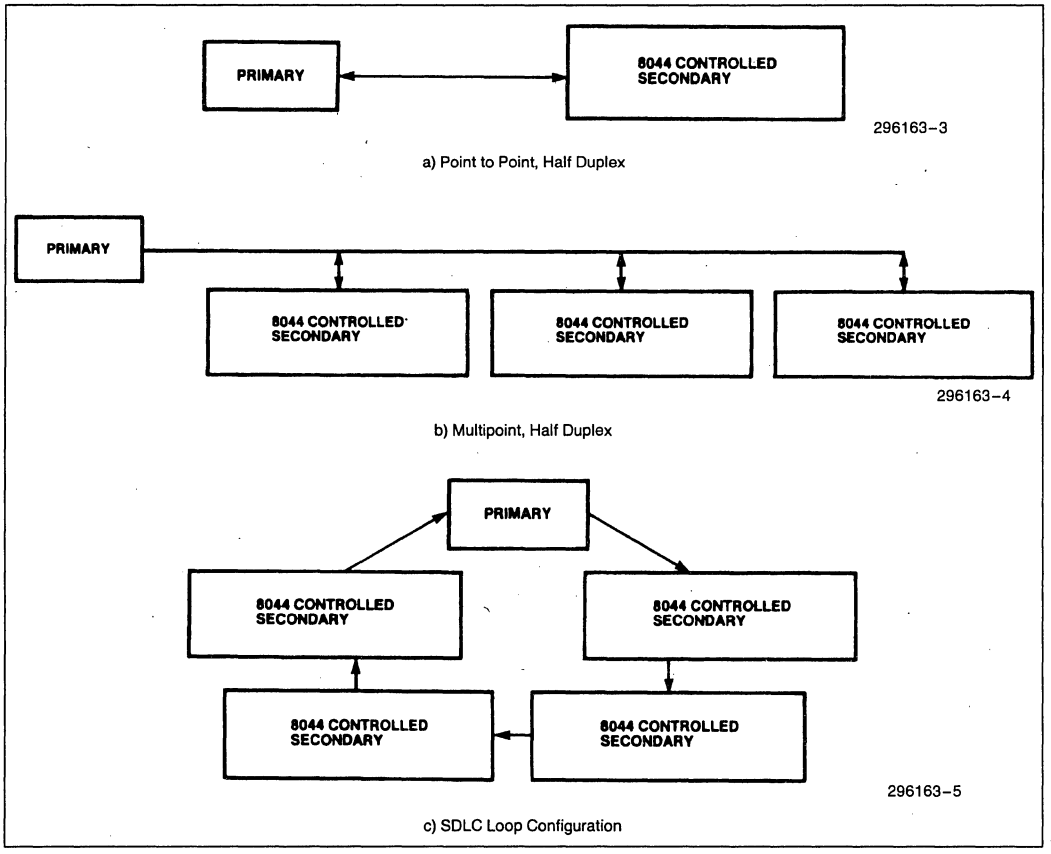


Figure 3. RUPI™-44 Supported Network Configurations

Due to SDLC/HDLC's well delineated field (see Figure 4) the CPU does not have to interpret character by character to determine control field and information field. In the case of Async, CPU must look at each character to interpret what it means. The practical advantage of such feature is straight forward use of DMA for information transfer.

In addition, SDLC/HDLC further improves Data throughput using implied Acknowledgement of transferred information. A station using SDLC/HDLC may acknowledge previously received information while transmitting different information in the same frame. In addition, up to 7 messages may be outstanding before an acknowledgement is required.

The HDLC/SDLC protocol can be used to realize reliable data links. Reliable Data transmission is ensured at the bit level by sending a frame check sequence, cyclic redudancy checking, within the frame. Reliable frame transmission is ensured by sending a frame number identification with each frame. This means that a receiver can sequentially count received frames and at any time infer what the number of the next frame to be received should be. More important, it provides a means for the receiver to identify to the sender some particular frame that it wishes to have resent because of errors.

2.2 HDLC/SDLC Networks

In both the HDLC and SDLC line protocols a (Master) primary station controls the overall network (data link) and issues commands to the secondary (Slave) stations. The latter complies with instructions and responds by sending appropriate responses. Whenever a transmitting station must end transmission prematurely, it sends an abort character. Upon detecting an abort character, a receiving station ignores the transmission block called a frame.

RUPI-44 supported HDLC/SDLC network configurations are point to point (half duplex) multipoint (half duplex), and loop. In the loop configuration the stations themselves act as repeaters, so that long links can be easily realized, see Figure 3.

2.3 Frames

An HDLC/SDLC frame consists of five basic fields: Flag, Address, Control, Data and Error Detection. A frame is bounded by flags—opening and closing flags. An address field is 8 bits wide in SDLC, extendable to 2 or more bytes in HDLC. The control field is also 8 bits wide, extendable to two bytes in HDLC. The SDLC data field or information field may be any number of bytes. The HDLC data field may or may not be on an 8 bit boundary. A powerful error detection code called Frame Check Sequence contains the calculated CRC (Cycle Redundancy Code) for all the bits between the flags. See Figure 4.

In HDLC and SDLC are three types of frames; an Information Frame is used to transfer data, a Supervisory Frame is used for control purposes, and a Nonsequenced Frame is used for initialization and control of the secondary stations.

For a more detailed discussion of higher level protocol functions interested readers may refer to the references listed in Section 2.6.

2.4 Zero Bit Insertion

In data communications, it is desirable to transmit data which can be of arbitrary content. Arbitrary data transmission requires that the data field cannot contain characters which are defined to assist the transmission protocol (like opening flag in HDLC/SDLC communications). This property is referred to as "data transparency". In HDLC/SDLC, this code transparency is made possible by Zero Bit Insertion (ZBI).

The flag has a unique bit pattern: 01111110 (7E HEX). To eliminate the possibility of the data field containing a 7E HEX pattern, a bit stuffing technique called Zero Bit Insertion is used. This technique specifies that during transmission, a binary 0 be inserted by the transmitter after any succession of five contiguous binary 1's. This will ensure that no pattern of 0 1 1 1 1 1 1 0 is ever transmitted between flags. On the receiving side, after receiving the flag, the receiver hardware automatically deletes any 0 following five consecutive 1's. The 8044 performs zero bit insertion and deletion automatically.

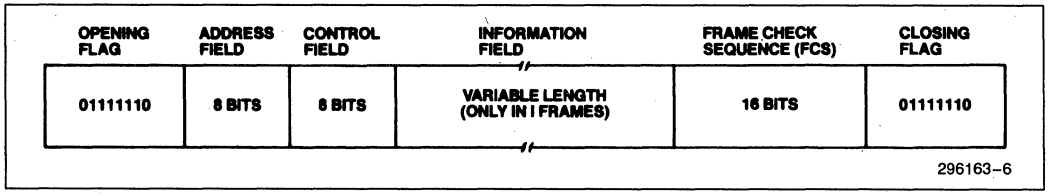


Figure 4. Frame Format

2.5 Non-return to Zero Inverted (NR21)

NRZI is a method of clock and data encoding that is well suited to the HDLC/SDLC protocol. It allows HDLC/SDLC protocols to be used with low cost asynchronous modems. NRZI coding is done at the transmitter to enable clock recovery from the data at the receiver terminal by using standard digital phase locked loop (DPLL) techniques. NRZI coding specifies that the signal condition does not change for transmitting a 1, while a 0 causes a change of state. NRZI coding ensures that an active data line will have a transition at least every 5-bit times (recall Zero Bit Insertion), while contiguous 0's will cause a change of state. Thus, ZBI and NRZI encoding makes it possible for the 8044's on-chip DPLL to recover a receive clock (from received data) synchronized to the received data and at the same time ensure data transparency.

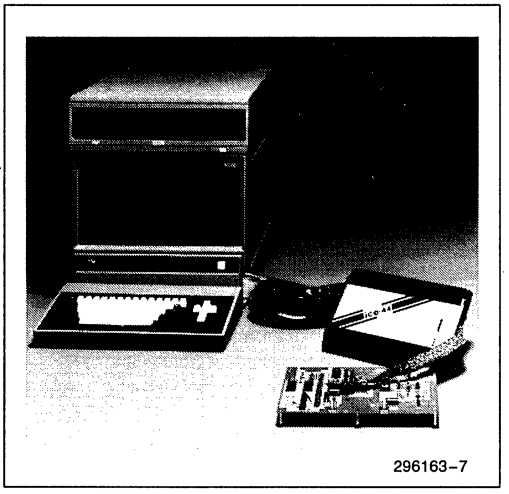
2.6 References

1. *IBM Synchronous Data Link Control General Information GA27-3093-2 File No. GENL-09.*
2. *Standard Network Access Protocol Specification, DATAPAC Trans-Canada Telephone System CCG111.*
3. *IBM 3650 Retail Store System Loop Interface OEM Information, IBM, GA27-3098-0.*
4. *Guidebook to Data Communications, Training Manual, Hewlett-Packard 5955-1715.*
5. *"Serial Backplane Suits Multiprocessor Architectures", Mike Webb, Computer Design, July 1984, pp. 85–96.*
6. *"Serial Bus Simplifies Distributed Control", P.D. MacWilliams, Control Engineering, June 1984, pp. 101–104.*
7. *"Chips Support Two Local Area Networks", Bob Dahlberg, Computer Design, May 1984, pp. 107–114.*
8. *"Build a VLSI-based Workstation for the Ethernet Environment", Mike Webb, EDN, 23 February 1984, pp. 297–307.*
9. *"Networking With the 8044", Young Sohn & Charles Gopen, Digital Design, May 1984, pp. 136–137.*

3.0 RUPI™-44 DESIGN SUPPORT

3.1 Design Tool Support

A critical design consideration is time to market. Intel provides a sophisticated set of design tools to speed hardware and software development time of 8044 based products. These include ICE-44, ASM-51, PL/M-51, and EMV-44.



296163-7

Figure 5. RUPI™-44 Development Support Configuration Intellec® System, ICE™-44 Buffer Box, and ICE-44 Module Plugged into a User Prototype Board

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A primary tool is the 8044 In Circuit Emulator, called ICE-44. See Figure 5. In conjunction with Intel's Intellec® Microprocessor Development System, the ICE-44 emulator allows hardware and software development to proceed interactively. This approach is more effective than the traditional method of independent hardware and software development followed by system integration. With the ICE-44 module, prototype hardware can be added to the system as it is designed. Software and hardware integration occurs while the product is being developed.

The ICE-44 emulator assists four stages of development:

1) Software Debugging

   It can be operated without being connected to the user's system before any of the user's hardware is available. In this stage ICE-44 debugging capabilities can be used in conjunction with the Intellec text editor and 8044 macroassembler to facilitate program development.

2) Hardware Development

   The ICE-44 module's precise emulation characteristics and full-speed program RAM make it a valuable tool for debugging hardware, including the time-critical SDLC serial port, parallel port, and timer interfaces.

3) System Integration

Integration of software and hardware can begin when any functional element of the user system hardware is connected to the 8044 socket. As each section of the user's hardware is completed, it is added to the prototype. Thus, each section of the hardware and software is system tested in real-time operation as it becomes available.

4) System Test

When the user's prototype is complete, it is tested with the final version of the user system software. The ICE-44 module is then used for real-time emulation of the 8044 to debug the system as a completed unit.

The final product verification test may be performed using the 8744 EPROM version of the 8044 microcomputer. Thus, the ICE-44 module provides the user with the ability to debug a prototype or production system at any stage in its development.

A conversion kit, ICE-44 CON, is available to upgrade an ICE-51 module to ICE-44.

Intel's ASM-51 Assembler supports the 8044 special function registers and assembly program development. PL/M-51 provides designers with a high level language for the 8044. Programming in PL/M can greatly reduce development time, and ensure quick time to market.

These tools have recently been expanded with the addition of the EMV-44CON. This conversion kit allows you to convert an EMV-51 into an EMV-44 emulation vehicle. The resultant low cost emulator is designed for use with an iPDS Personal Development System, which also supports the ASM-51 assembler and PL/M-51. See Figure 6.

Emulation support is similar to the ICE-44 with support for Software and Hardware Development, System Integration, and System Test. The iPDS's rugged portability and ease of use also make it an ideal system for production tests and field service of your finished design. In addition, the iPDS offers EPROM programming module for the 8744, and direct communications with the 8044-based BITBUS via an optional iSBX-344 distributed control module.

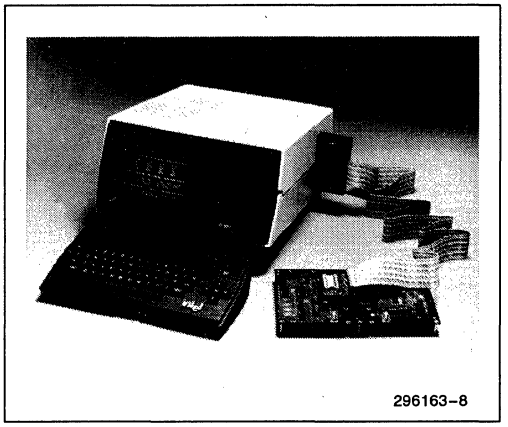

Figure 6. RUPI-44 iPDS Personal Development System, EMV-44 Buffer Box, and EMV-44 Module Plugged into a User Prototype Board

3.2 8051 Workshop

Intel provides 8051 training to its customers through the 5-day 8051 workshop. Familiarity with the 8051 and 8044 is achieved through a combination of lecture and laboratory exercises.

For designers not familiar with the 8051, the workshop is an effective way to become proficient with the 8051 architecture and capabilities.

intel®

October 1988

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8044 Architecture

Order Number: 296164-001

8044 ARCHITECTURE

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GENERAL

The 8044 is based on the 8051 core. The 8044 replaces the 8051's serial port with an intelligent HDLC/SDLC controller called the Serial Interface or SIU. Thus the differences between the two result from the 8044's increased on-chip RAM (192 bytes) and additional special function registers necessary to control the SIU. Aside from the increased memory, the SIU itself, and differences in 5 pins (for the serial port), the 8044 and 8051 are compatible.

This chapter describes the differences between the 8044 and 8051. Information pertaining to the 8051 core, eg. instruction set, port operation, EPROM programming, etc. is located in the 8051 sections of this manual.

A block diagram of the 8044 is shown in Figure 1. The pinpoint is shown on the inside front cover.

1.0 MEMORY ORGANIZATION OVERVIEW

The 8044 maintains separate address spaces for Program Memory and Data Memory. The Program Memory can be up to 64K bytes long, of which the lowest 4K bytes are in the on-chip ROM.

If the $\overline{EA}$ pin is held high, the 8044 executes out of internal ROM unlwess the Program Counter exceeds 0FFFH. Fetches from locations 1000H through FFFFH are directed to external Program Memory.

If the $\overline{EA}$ pin is held low, the 8044 fetches all instructions from external Program Memory.

The Data Memory consists of 192 bytes of on-chip RAM, plus 35 Special Function Registers, in addition to which the device is capable of accessing up to 64K bytes of external data memory.

The Program Memory uses 16-bit addresses. The external Data Memory can use erither 8-bit or 16-bit addresses. The internal Data Memory uses 8-bit addresses, which provide a 256-location address space. The lower 192 addresses access the on-chip RAM. The Special Function Registers occupy various locations in the upper 128 bytes of the same address space.

The lowest 32 bytes in the internal RAM (locations 00 through 1FH) are divided into 4 banks of registers, each bank consisting of 8 bytes. Any one of these banks can be selected to be the "working registers" of the CPU, and can be accessed by a 3-bit address in the same byte as the opcode of an instruction. Thus, a large number of instructions are one-byte instructions.

The next higher 16 bytes of the internal RAM (locations 20H through 2FH) have individually addressable bits. These are provided for use as software flags or for one-bit (Boolean) processing. This bit-addressing capability is an important feature of the 8044. In addition to the 128 individually addressable bits in RAM, twelve of the Special Function Registers also have individually addressable bits.

A memory map is shown in Figure 2.

1.1 Special Function Registers

The Special Function Registers are as follows:

*	ACC	Accumulator (A Register)
*	B	B Register
*	PSW	Program Status Word
	SP	Stack Pointer
	DPTR	Data Pointer (consisting of DPH AND DPL)
*	P0	Port 0
*	P1	Port 1
*	P2	Port 2
*	P3	Port 3
*	IP	Interrupt Priority
*	IE	Interrupt Enable
	TMOD	Timer/Counter Mode
*	TCON	Timer/Counter Control
	TH0	Timer/Counter 0 (high byte)
	TL0	Timer/Counter 0 (low byte)
	TH1	Timer/Counter 1 (high byte)
	TL1	Timer/Counter 1 (low byte)
	SMD	Serial Mode
*	STS	Status/Command
*	NSNR	Send/Receive Count
	STAD	Station Address
	TBS	Transmit Buffer Start Address
	TBL	Transmit Buffer Length
	TCB	Transmit Control Byte
	RBS	Receive Buffer Start Address
	RBL	Receive Buffer Length
	RFL	Received Field Length
	RCB	Received Control Byte
	DMA CNT	DMA Count
	FIFO	FIFO (three bytes)
	SIUST	SIU State Counter
	PCON	Power Control

The registers marked with * are both byte- and bit-addressable.

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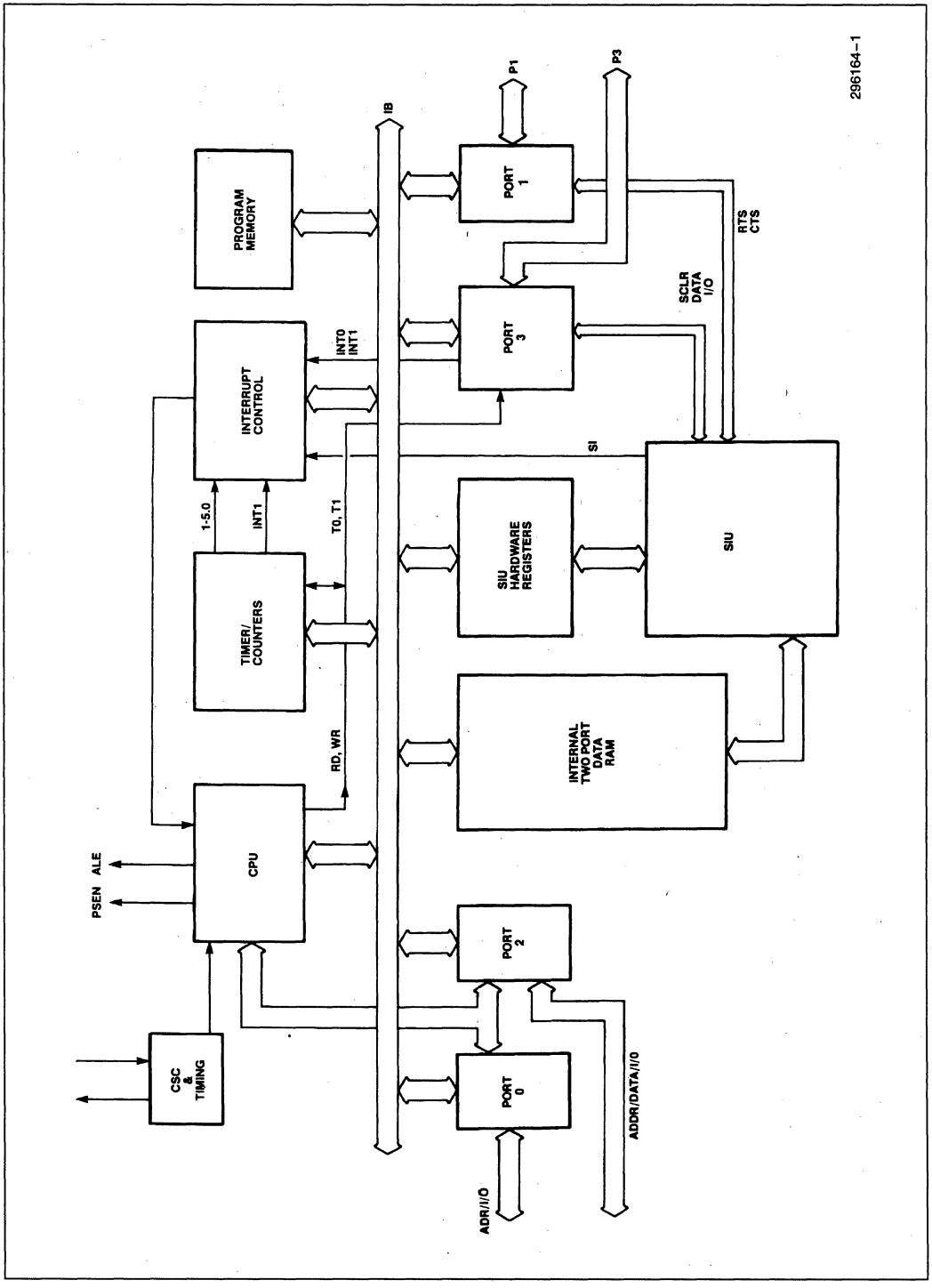

Figure 1. RUPI™ Block Diagram

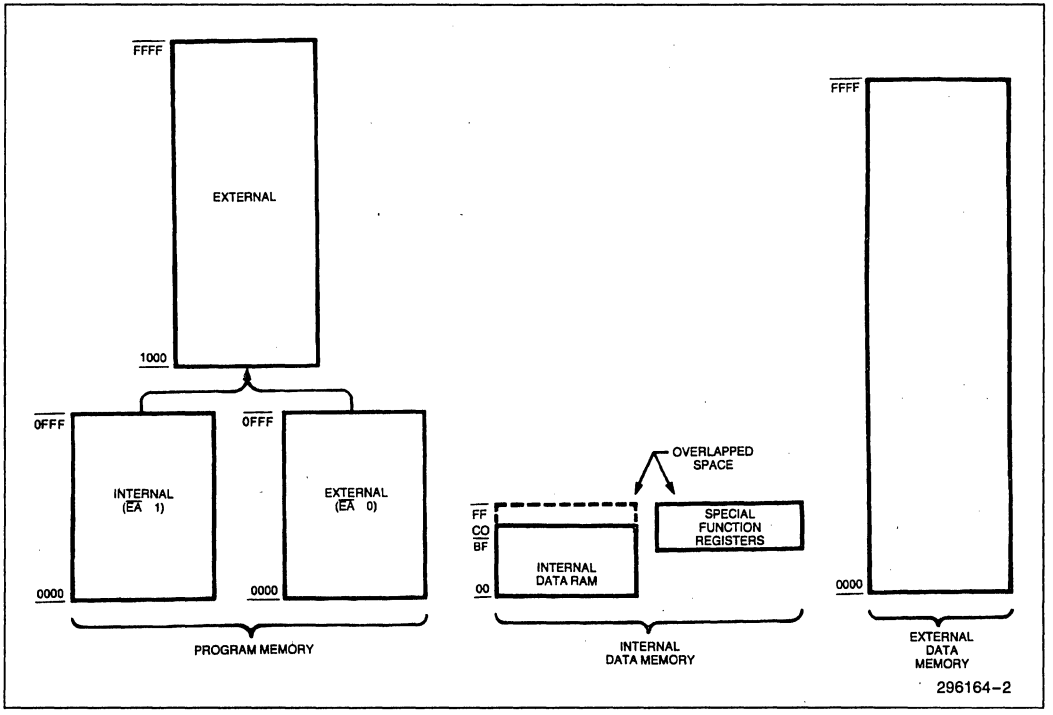

Figure 2. RUPI™-44 Memory Map

Stack Pointer

The Stack Pointer is 8 bits wide. The stack can reside anywhere in the 192 bytes of on-chip RAM. When the 8044 is reset, the stack pointer is initialized to 07H. When executing a PUSH or a CALL, the stack pointer is incremented before data is stored, so the stack would begin at location 08H.

1.2 Interrupt Control Registers

The Interrupt Request Flags are as listed below:

Source	*Request Flag*	*Location*
External Interrupt 0	$\overline{INT0}$, if IT0 = 0 IE0, if IT0 = 1	P3.2 TCON.1
Timer 0 Overflow	TF0	TCON.5
External Interrupt 1	$\overline{INT1}$, if IT1 = 0 IE1, if IT1 = 1	P3.3 TCON.3
Timer 1 Overflow	TF1	TCON.7
Serial Interface Unit	SI	STS.4

External Interrupt control bits IT0 and IT1 are in TCON.0 and TCON.2, respectively. Reset leaves all flags inactive, with IT0 and IT1 cleared.

All the interrupt flags can be set or cleared by software, with the same effect as by hardware.

The Enable and Priority Control Registers are shown below. All of these control bits are set or cleared by software. All are cleared by reset.

IE: Interrupt Enable Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	EA	X	X	ES	ET1	EX1	ET0	EX0

where:

- EA disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
- ES enables or disables the Serial Interface Unit interrupt. If ES = 0, the Serial Interface Unit interrupt is disabled.
- ET1 enables or disables the Timer 1 Overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.

- EX1 enables or disables External Interrupt 1. If EX1 = 0, External Interrupt 1 is disabled.
- ET0 enables or disables the Timer 0 Overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.

IP: Interrupt Priority Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	X	X	X	PS	PT1	PX1	PT0	PX0

where:

- PS defines the Serial Interface Unit interrupt priority level. PS = 1 programs it to the higher priority level.
- PT1 defines the Timer 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.
- PX1 defines the External Interrupt priority level. PX1 = 1 programs it to the higher priority level.
- PT0 defines the Timer 0 interrupt priority level. PT0 = 1 programs it to the higher priority level.
- PX0 defines the External Interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.

2.0 MEMORY ORGANIZATION DETAILS

In the 8044 family the memory is organized over three address spaces and the program counter. The memory spaces shown in Figure 2 are the:

- 64K-byte Program Memory address space
- 64K-byte External Data Memory address space
- 320-byte Internal Data Memory address space

The 16-bit Program Counter register provides the 8044 with its 64K addressing capabilities. The Program Counter allows the user to execute calls and branches to any location within the Program Memory space. There are no instructions that permit program execution to move from the Program Memory space to any of the data memory spaces.

In the 8044 and 8744 the lower 4K of the 64K Program Memory address space is filled by internal ROM and EPROM, respectively. By tying the $\overline{EA}$ pin high, the processor can be forced to fetch from the internal ROM/EPROM for Program Memory addresses 0 through 4K. Bus expansion for accessing Program Memory beyond 4K is automatic since external instruction fetches occur automatically when the Program Counter increases above 4095. If the $\overline{EA}$ pin is tied low all Program Memory fetches are from external memory. The execution speed of the 8044 is the same regardless of whether fetches are from internal or external Program Memory. If all program storage is on-chip, byte location 4095 should be left vacant to prevent an undesired prefetch from external Program Memory address 4096.

Certain locations in Program Memory are reserved for specific programs. Locations 0000 through 0002 are reserved for the initialization program. Following reset, the CPU always begins execution at location 0000. Locations 0003 through 0042 are reserved for the five interrupt-request service programs. Each resource that can request an interrupt requires that its service program be stored at its reserved location.

The 64K-byte External Data Memory address space is automatically accessed when the MOVX instruction is executed.

Functionally the Internal Data Memory is the most flexible of the address spaces. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address space and a 128-byte Special Function Register address space as shown in Figure 3.

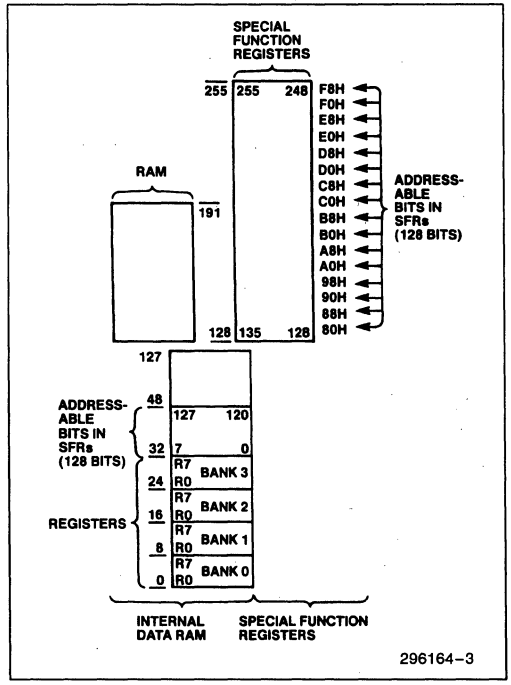

Figure 3. Internal Data Memory Address Space

The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit locations of the on-chip RAM are accessible through Direct Addressing. These bits reside in Internal Data RAM at byte locations 32 through 47. Currently locations 0 through 191 of the Internal Data RAM address space are filled with on-chip RAM.

The stack depth is limited only by the available Internal Data RAM, thanks to an 8-bit reloadable Stack Pointer. The stack is used for storing the Program Counter during subroutine calls and may be used for passing parameters. Any byte of Internal Data RAM or Special Function Register accessible though Direct Addressing can be pushed/popped.

The Special Function Register address space is 128 to 255. All registers except the Program Counter and the four 8-Register Banks reside here. Memory mapping the Special Function Registers allows them to be accessed as easily as internal RAM. As such, they can be operated on by most instructions. In the overlapping memory space (address 128-191), indirect addressing is used to access RAM, and direct addressing is used to access the SFR's. The SFR's at addresses 192–255 are also accessed using direct addressing. The Special Function Registers are listed in Figure 4. Their mapping in the Special Function Register address space is shown in Figures 5 and 6.

Performing a read from a location of the Internal Data memory where neither a byte of Internal Data RAM (i.e., RAM addresses 192-255) nor a Special Function Register exists will access data of indeterminable value.

Architecturally, each memory space is a linear sequence of 8-bit wide bytes. By Intel convention the storage of multi-byte address and data operands in program and data memories is the least significant byte at the low-order address and the most significant byte at the high-order address. Within byte X, the most significant bit is represented by X.7 while the least significant bit is X.0. Any deviation from these conventions will be explicitly stated in the text.

2.1 Operand Addressing

There are five methods of addressing source operands. They are Register Addressing, Direct Addressing, Register-Indirect Addressing, Immediate Addressing

ARITHMETIC REGISTERS:
Accumulator*, B register*,
Program Status Word*
POINTERS:
Stack Pointer, Data Pointer (high & low)
PARALLEL I/O PORTS:
Port 3*, Port 2*, Port 1*, Port 0*
INTERRUPT SYSTEM:
Interrupt Priority Control*,
Interrupt Enable Control*
TIMERS:
Timer Mode, Timer Control*, Timer 1 (high & low), Timer 0 (high & low)
SERIAL INTERFACE UNIT:
Transmit Buffer Start,
Transmit Buffer Length,
Transmit Control Byte,
Send Count Receive Count*,
DMA Count,
Station Address
Receive Field Length
Receive Buffer Start
Receive Buffer Length
Receive Control Byte,
Serial Mode,
Status Register.*

***Bits in these registers are bit addressable.**

Figure 4. Special Function Registers

ARITHMETIC REGISTERS:
Accumulator*, B register*,
Program Status Word*
POINTERS:
Stack Pointer, Data Pointer (high & low)
PARALLEL I/O PORTS:
Port 3*, Port 2*, Port 1*, Port 0*
INTERRUPT SYSTEM:
Interrupt Priority Control*,
Interrupt Enable Control*
TIMERS:
Timer Mode, Timer Control*, Timer 1 (high & low), Timer 0 (high & low)
SERIAL INTERFACE UNIT:
Serial Mode, Status/Command*,
Send/Receive Count*, Station Address,
Transmit Buffer Start Address,
Transmit Buffer Length,
Transmit Control Byte,
Receive Buffer Start Address,
Receive Buffer Length,
Receive Field Length,
Receive Control Byte,
DMA Count,
FIFO (three bytes),
SIU Controller State Counter

***Bits in these registers are bit-addressable.**

Figure 5. Mapping of Special Function Registers

and Base-Register-plus Index-Register-Indirect Addressing. The first three of these methods can also be used to address a destination operand. Since operations in the 8044 require 0 (NOP only), 1, 2, 3 or 4 operands, these five addressing methods are used in combinations to provide the 8044 with its 21 addressing modes.

Most instructions have a "destination, source" field that specifies the data type, addressing methods and operands involved. For operations other than moves, the destination operand is also a source operand. For example, in "subtract-with-borrow A,#5" the A register receives the result of the value in register A minus 5, minus C.

Most operations involve operands that are located in Internal Data Memory. The selection of the Program Memory space or External Data Memory space for a second operand is determined by the operation mnemonic unless it is an immediate operand. The subset of the Internal Data Memory being addressed is determined by the addressing method and address value. For example, the Special Function Registers can be accessed only through Direct Addressing with an address of 128-255. A summary of the operand addressing methods is shown in Figure 6. The following paragraphs describe the five addressing methods.

2.2 Register Addressing

Register Addressing permits access to the eight registers (R7-R0) of the selected Register Bank (RB). One of the four 8-Register Banks is selected by a two-bit field in the PSW. The registers may also be accessed through Direct Addressing and Register-Indirect Addressing, since the four Register Banks are mapped into the lowest 32 bytes of internal Data RAM as shown in Figures 9 and 10. Other Internal Data Memory locations that are addressed as registers are A, B, C, AB and DPTR.

2.3 Direct Addressing

Direct Addressing provides the only means of accessing the memory-mapped byte-wide Special Function Registers and memory mapped bits within the Special Function Registers and Internal Data RAM. Direct Addressing of bytes may also be used to access the lower 128 bytes of Internal Data RAM. Direct Addressing of bits gains access to a 128 bit subset of the Special Function Registers as shown in Figures 5, 6, 9, and 10.

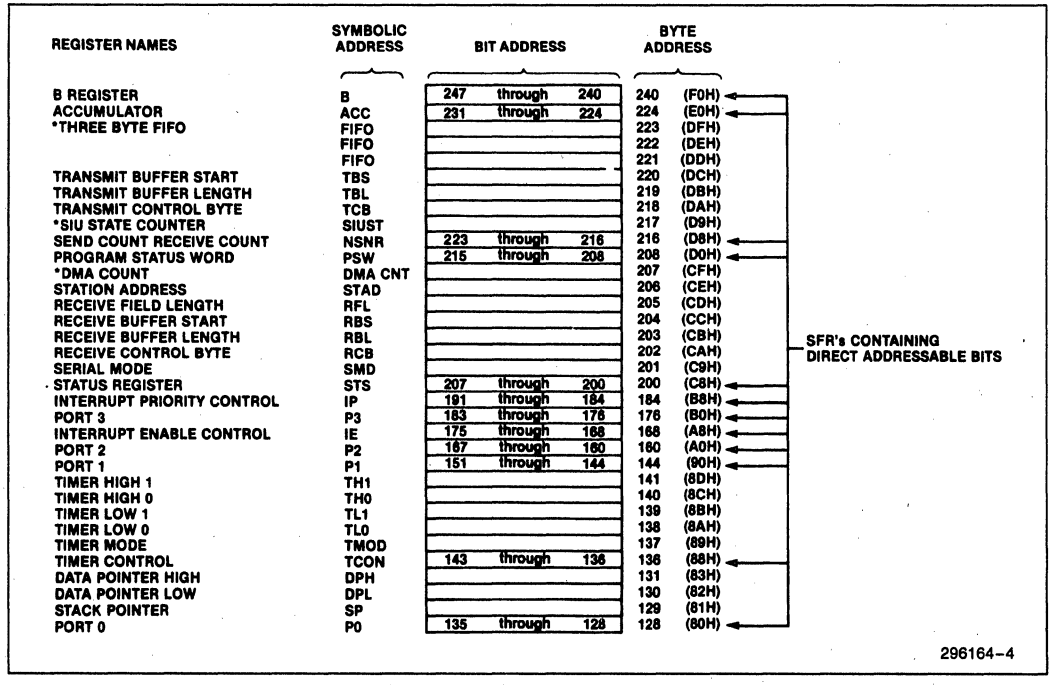

Figure 6. Mapping of Special Function Registers

Direct Byte Address	Bit Address (MSB)							(LSB)	Hardware Register Symbol
240	F7	F6	F5	F4	F3	F2	F1	F0	8
224	E7	E6	E5	E4	E3	E2	E1	E0	ACC
	NS2	NS1	NS0	SES	NR2	NR1	NR0	SER	
216	DF	DE	DD	DC	DB	DA	D9	D8	NSNR
	CY	AC	FO	RS1	RSO	OV		P	
204	D7	D6	D5	D4	D3	D2	D1	D0	PSW
	TBF	RE	RTS	SI	BV	CPB	AM	RBP	
200	CF	CE	CD	CC	CB	CA	C9	C8	STS
				PS	PT1	PX1	PT0	PX0	
184	—	—	—	BC	BB	BA	B9	B8	1P
176	B7	B6	B5	B4	B3	B2	B1	B0	P3
	EA			E5	ET1	EX1	ET0	EX0	
168	AF	—	—	AC	AB	AA	A9	A8	1E
160	A7	A6	A5	A4	A3	A2	A1	A0	P2
144	97	96	95	94	93	92	91	90	P1
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
136	8F	8E	8D	8C	8B	8A	89	88	TCON
128	87	86	85	84	83	82	81	80	P0

Figure 7. Special Function Register Bit Address

- **Register Addressing**
  - **R7-R0**
  - **A, B, C (bit), AB (two bytes), DPTR (double byte)**
- **Direct Addressing**
  - **Lower 128 bytes of Internal Data RAM**
  - **Special Function Registers**
  - **128 bits in subset of Special Function Register address space**
- **Register-Indirect Addressing**
  - **Internal Data RAM [@R1, @R0, @SP (PUSH and POP only)]**
  - **Least Significant Nibbles in Internal Data RAM (@R1, @R0)**
  - **External Data Memory (@R1, @R0, @DPTR)**
- **Immediate Addressing**
  - **Program Memory (in-code constant)**
- **Base-Register-plus Index-Register-Indirect Addressing**
  - **Program Memory (@ DPTR + A, @ PC + A)**

Figure 8. Operand Addressing Methods

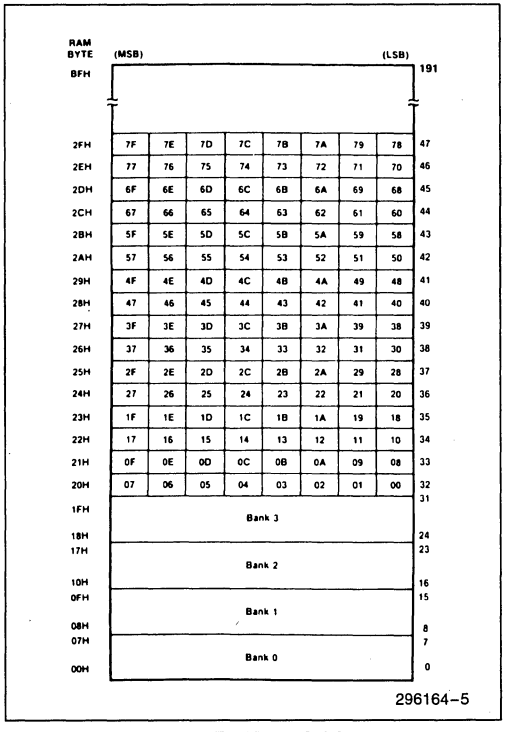

Figure 9. RAM Bit Address

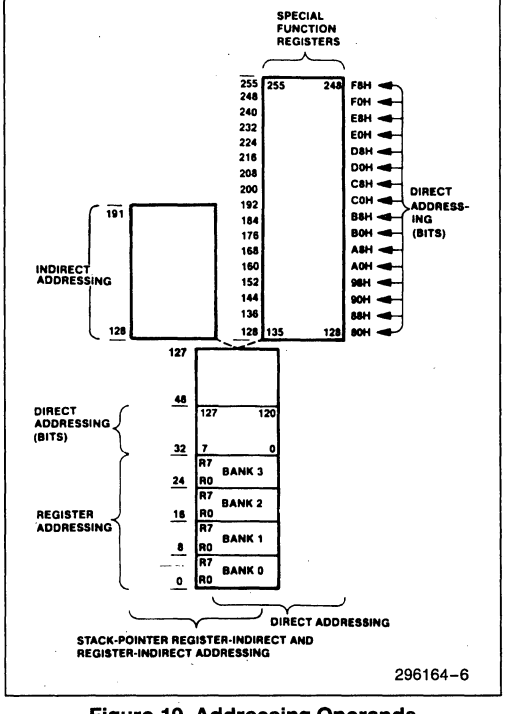

Figure 10. Addressing Operands in Internal Data Memory

Register-Indirect Addressing using the content of R1 or R0 in the selected Register Bank, or using the content of the Stack Pointer (PUSH and POP only), addresses the Internal Data RAM. Register-Indirect Addressing is also used for accessing the External Data Memory. In this case, either R1 or R0 in the selected Register Bank may be used for accessing locations within a 256-byte block. The block number can be preselected by the contents of a port. The 16-bit Data Pointer may be used for accessing any location within the full 64K external address space.

3.0 RESET

Reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) *while the oscillator is running.* The CPU responds by executing an internal reset. It also configures the ALE and PSEN pins as inputs. (They are quasi-bidirectional.) The internal reset is executed during the second cycle in which RST is high and is repeated every cycle until RST goes low. It leaves the internal registers as follows:

Register	Content
PC	0000H
A	00H
B	00H
PSW	00H
SP	07H
DPTR	0000H
P0-P3	0FFH
IP	(XXX00000)
IE	(0XX00000)
TMOD	00H
TCON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
SMD	00H
STS	00H
NSNR	00H
STAD	00H
TBS	00H
TBL	00H
TCB	00H
RBS	00H
RBL	00H
RFL	00H
RCB	00H
DMA CNT	00H
FIFO1	00H
FIFO2	00H
FIFO3	00H
SIUST	01H
PCON	(0XXXXXXX)

The internal RAM is not affected by reset. When VCC is turned on, the RAM content is indeterminate unless VPD was applied prior to VCC being turned off (see Power Down Operation.)

4.0 RUPI™-44 FAMILY PIN DESCRIPTION

VSS: Circuit ground potential.

VCC: Supply voltage during programming (of the 8744), verification (of the 8044 or 8744), and normal operation.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accessses to external memory (during which accesses it activates internal pullups). It also outputs instruction bytes during program verification. (External pullups are required during program verification.) Port 0 can sink eight LS TTL inputs.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the low-order address byte during program verification in the 8044 or 8744. Port 1 can sink/source four LS TTL inputs, It can drive MOS inputs without external pullups.

Two of the Port 1 pins serve alternate functions, as listed below:

Port Pin	*Alternate Function*
P1.6	$\overline{RTS}$ (Request to Send). In a non-loop configuration, $\overline{RTS}$ signals that the 8044 is ready to transmit data.

intel®

October 1988

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The RUPI™-44 Serial Interface Unit

Order Number: 296165-001

THE RUPI™-44 SERIAL INTERFACE UNIT

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SERIAL INTERFACE

The serial interface provides a high-performance communication link. The protocol used for this communication is based on the IBM Synchronous Data Link Control (SDLC). The serial interface also supports a subset of the ISO HDLC (International Standards Organization High-Level Data Link Control) protocol.

The SDLC/HDLC protocols have been accepted as standard protocols for many high-level teleprocessing systems. The serial interface performs many of the functions required to service the data link without intervention from the 8044's own CPU. The programmer is free to concentrate on the 8044's function as a peripheral controller, rather than having to deal with the details of the communication process.

Five pins on the 8044 are involved with the serial interface:

Pin 7	$\overline{RTS}$/P16
Pin 8	$\overline{CTS}$/P17
Pin 10	I/$\overline{O}$/RXD/P30
Pin 11	DATA/TXD/P31
Pin 15	SCLK/T1//P35

Figure 1 is a functional block diagram of the serial interface unit (SIU). More details on the SIU hardware are given later in this chapter.

1.0 DATA LINK CONFIGURATIONS

The serial interface is capable of operating in three serial data link configurations:

1) Half-Duplex, point-to-point
2) Half-Duplex, multipoint (with a half-duplex or full-duplex primary)
3) Loop

Figure 2 shows these three configurations. The RTS (Request to Send) and CTS (Clear to Send) hand-shaking signals are available in the point-to-point and multipoint configurations.

2.0 DATA CLOCKING OPTIONS

The serial interface can operate in an externally clocked mode or in a self clocked mode.

Externally Clocked Mode

In the externally clocked mode, a common Serial Data Clock (SCLK on pin 15) synchronizes the serial bit stream. This clock signal may come from the master CPU or primary station, or from an external phase-locked loop local to the 8044. Figure 3 illustrates the timing relationships for the serial interface signals when the externally clocked mode is used in point-to-point and multipoint data link configurations.

Incoming data is sampled at the rising edge of SCLK, and outgoing data is shifted out at the falling edge of SCLK. More detailed timing information is given in the 8044 data sheet.

Self Clocked (Asynchronous) Mode

The self clocked mode allows data transfer without a common system data clock. Using an on-chip DPLL (digital phase locked loop) the serial interface recovers the data clock from the data stream itself. The DPLL requires a reference clock equal to either 16 times or 32 times the data rate. This reference clock may be externally supplied or internally generated. When the serial interface generates this clock internally, it uses either the 8044's internal logic clock (half the crystal frequency's PH2) or the "timer 1" overflow. Figure 4 shows the serial interface signal timing relationships for the loop configuration, when the unclocked mode is used.

The DPLL monitors the received data in order to derive a data clock that is centered on the received bits. Centering is achieved by detecting all transitions of the received data, and then adjusting the clock transition (in increments of $1/16$ bit period) toward the center of the received bit. The DPLL converges to the nominal bit center within eight bit transitions, worst case.

To aid in the phase locked loop capture process, the 8044 has a NRZI (non-return-to-zero inverted) data encoding and decoding option. NRZI coding specifies that a signal does not change state for a transmitted binary 1, but does change state for a binary 0. Using the NRZI coding with zero-bit insertion, it can be guaranteed that an active signal line undergoes a transition at least every six bit times.

3.0 DATA RATES

The maximum data rate in the externally clocked mode is 2.4M bits per second (bps) a half-duplex configuration, and 1.0M in a loop configuration.

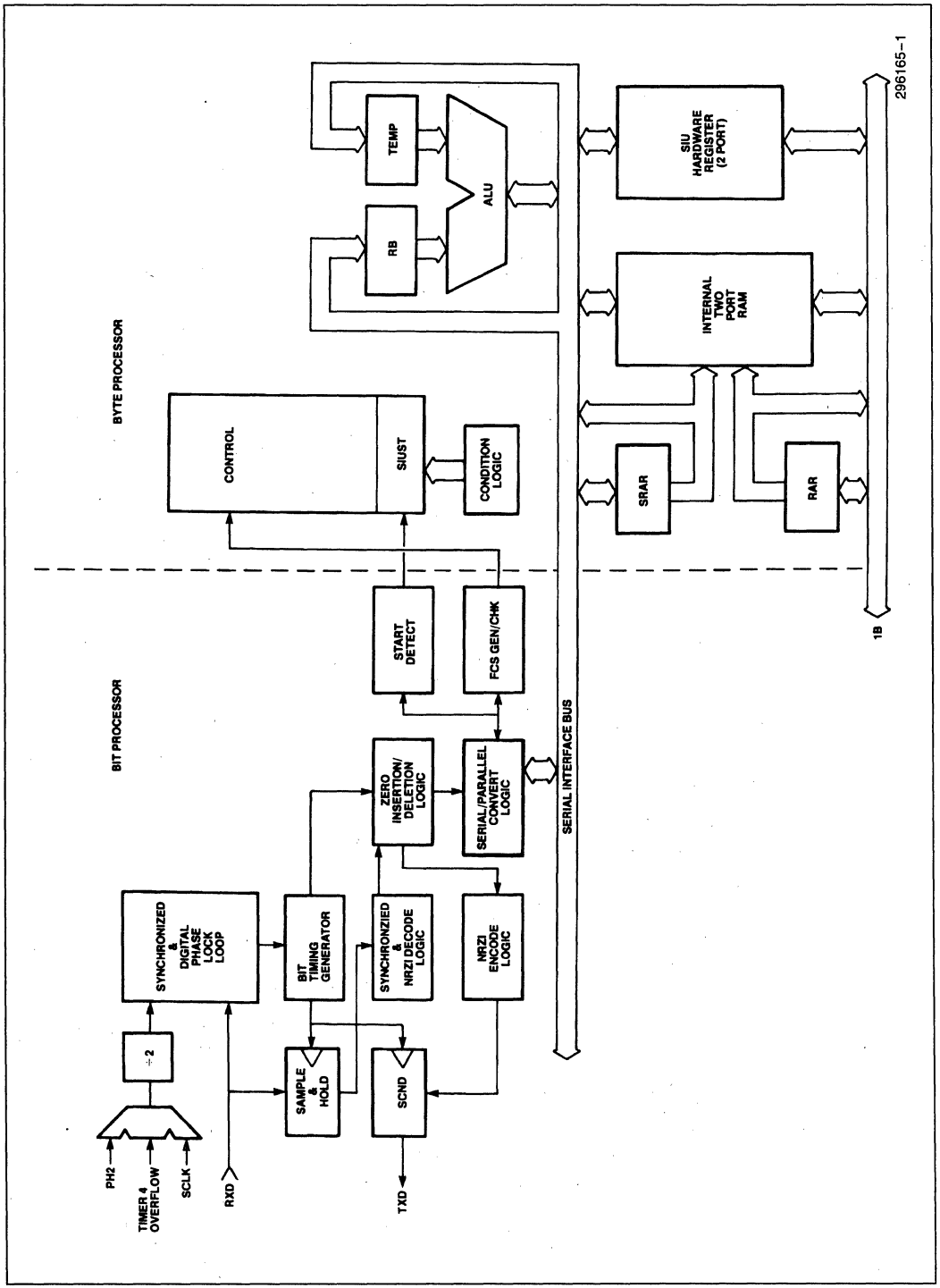

Figure 1. SIU Block Diagram

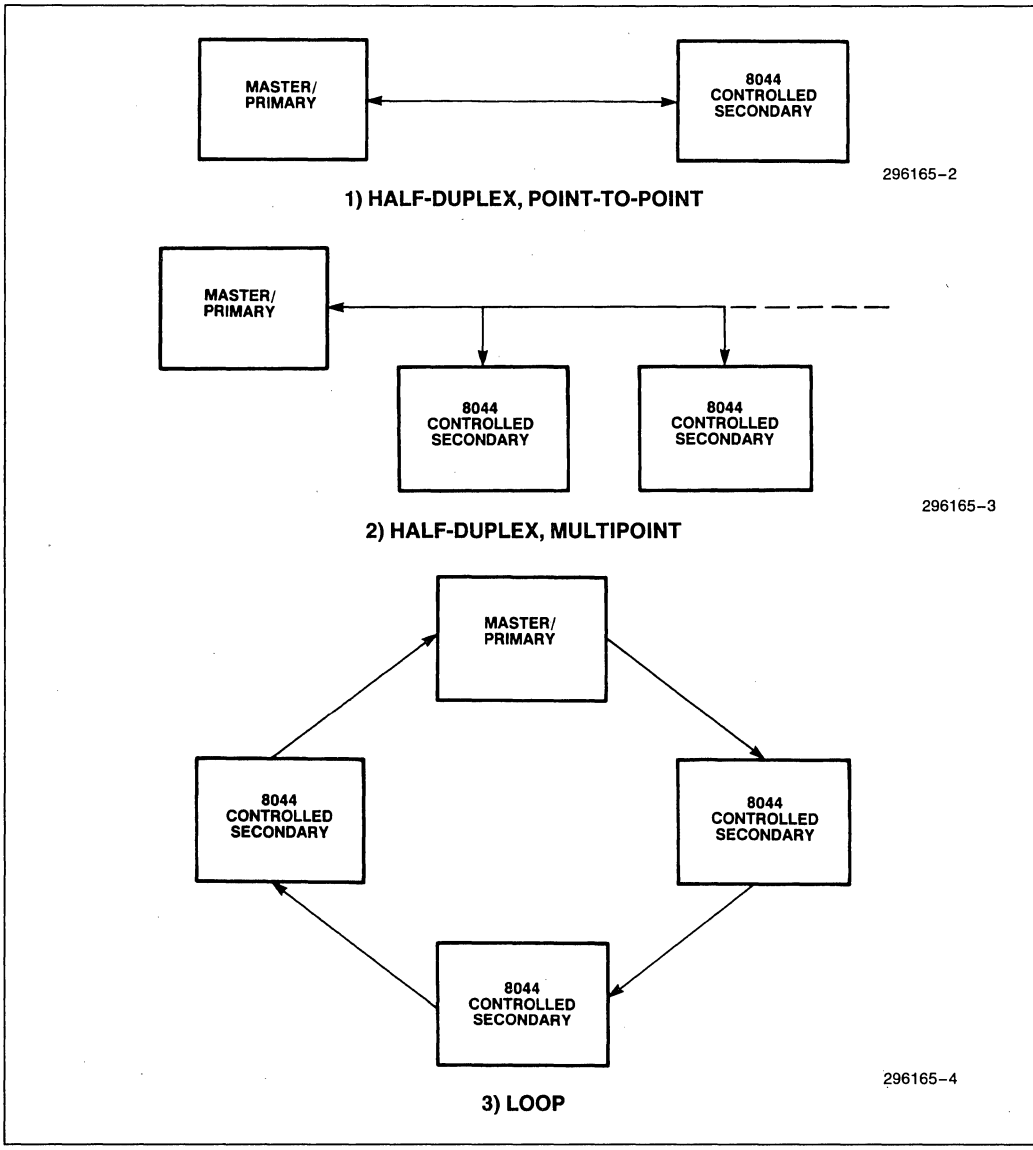

Figure 2. RUPI-44 Data Link Configurations

In the self clocked mode with an external reference clock, the maximum data rate is 375K bps.

In the self clocked mode with an internally generated reference clock, and the 8044 operating with a 12 MHz crystal, the available data rates are 244 bps to 62.5K bps, 187.5K bps and 375K bps.

For more details see the table in the SMD register description, below.

4.0 OPERATIONAL MODES

The Serial Interface Unit (SIU) can operate in either of two response modes:

1) AUTO mode
2) FLEXIBLE (NON-AUTO) mode

In the AUTO mode, the SIU performs in hardware a subset of the SDLC protocol called the normal response mode. The AUTO mode enables the SIU to recognize and respond to certain kinds of SDLC frames without intervention from the 8044's CPU. AUTO mode provides a faster turnaround time and a simplified software interface, whereas NON-AUTO mode provides a greater flexibility with regard to the kinds of operation permitted.

In AUTO mode, the 8044 can act only as a normal response mode secondary station—that is, it can transmit only when instructed to do so by the primary station. All such AUTO mode responses adhere strictly to IBM's SDLC definitions.

In the FLEXIBLE mode, reception or transmission of each frame by the SIU is performed under the control of the CPU. In this mode the 8044 can be either a primary station or a secondary station.

In both AUTO and FLEXIBLE modes, short frames, aborted frames, or frames which have had CRC's are ignored by the SIU.

The basic format of an SDLC frame is as follows:

Flag	Address	Control	Information	FCS	Flag

Format variations consist of omitting one or more of the fields in the SDLC frame. For example, a supervisory frame is formed by omitting the information field. Supervisory frames are used to confirm received frames, indicate ready or busy conditions, and to report errors. More details on frame formats are given in the SDLC Frame Format Options section, below.

4.1 AUTO Mode

To enable the SIU to receive a frame in AUTO mode, the 8044 CPU sets up a receive buffer. This is done by writing two registers—Receive Buffer Start (RBS) Address and Receive Buffer Length (RBL).

The SIU receives the frame, examines the control byte, and takes the appropriate action. If the frame is an information frame, the SIU will load the receive buffer, interrupt the CPU (to have the receive buffer read), and make the required acknowledgement to the primary station. Details on these processes are given in the Operation section, below.

In addition to receiving the information frames, the SIU in AUTO mode is capable of responding to the following commands (found in the control field of supervisory frames) from the primary station:

RR (Receive Ready): Acknowledges that the Primary station has correctly received numbered frames up through $N_R - 1$, and that it is ready to receive frame N_R.

RNR (Receive Not Ready): Indicates a temporary busy condition (at the primary station) due to buffering or other internal constraints. The quantity N_R in the control field indicates the number of the frame expected after the busy condition ends, and may be used to acknowledge the correct reception of the frames up through $N_R - 1$.

REJ (Reject): Acknowledges the correct reception of frames up through $N_R - 1$, and requests transmission or retransmission starting at frame N_R. The 8044 is capable of retransmitting at most the previous frame, and then only if it is still available in the transmit buffer.

UP (Unnumbered Poll): Also called NSP (Non-Sequenced Poll) or ORP (Optional Response Poll). This command is used in the loop configuration.

To enable the SIU to transmit an information frame in AUTO mode, the CPU sets up a transmit buffer. This is done by writing two registers—Transmit Buffer Start (TBS) Address and Transmit Buffer Length (TBL), and filling the transmit buffer with the information to be transmitted.

When the transmit buffer is full, the SIU can automatically (without CPU intervention) send an information frame (I-frame) with the appropriate sequence numbers, when the data link becomes available (when the 8044 is polled for information). After the SIU has transmitted the I-frame, it waits for acknowledgement from the receiving station. If the acknowledgement is

negative, the SIU retransmits the frame. If the acknowledgement is positive, the SIU interrupts the CPU, to indicate that the transmit buffer may be reloaded with new information.

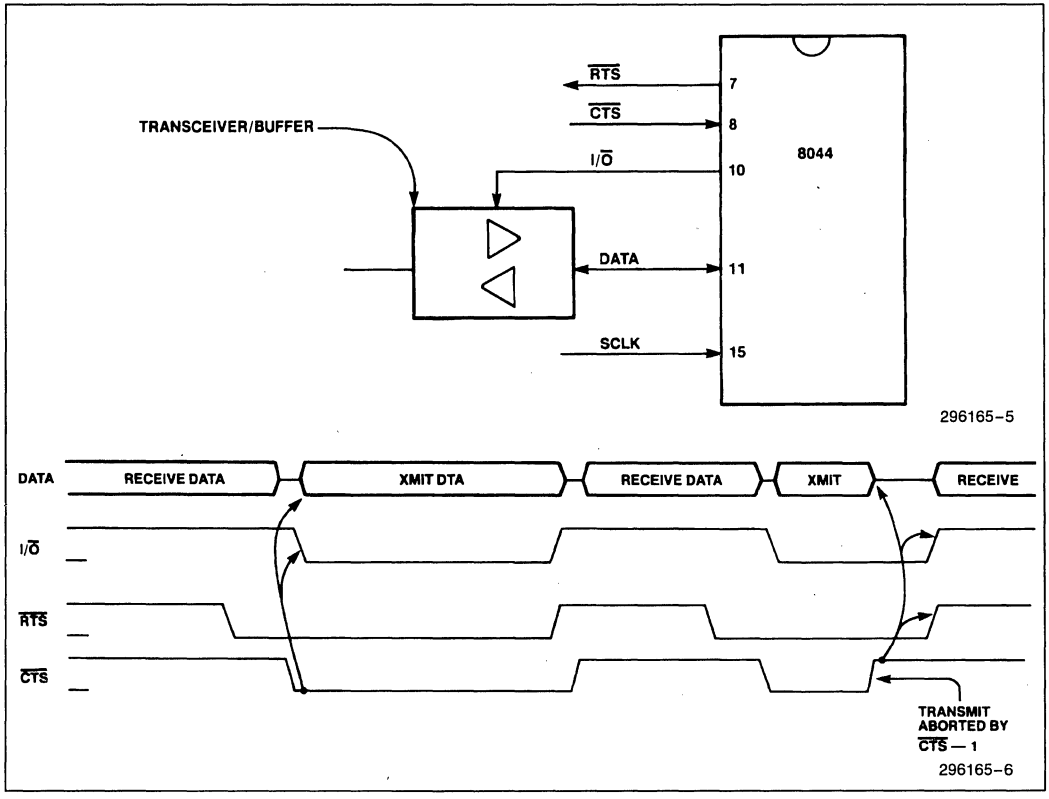

Figure 3. Serial Interface Timing—Clocked Mode

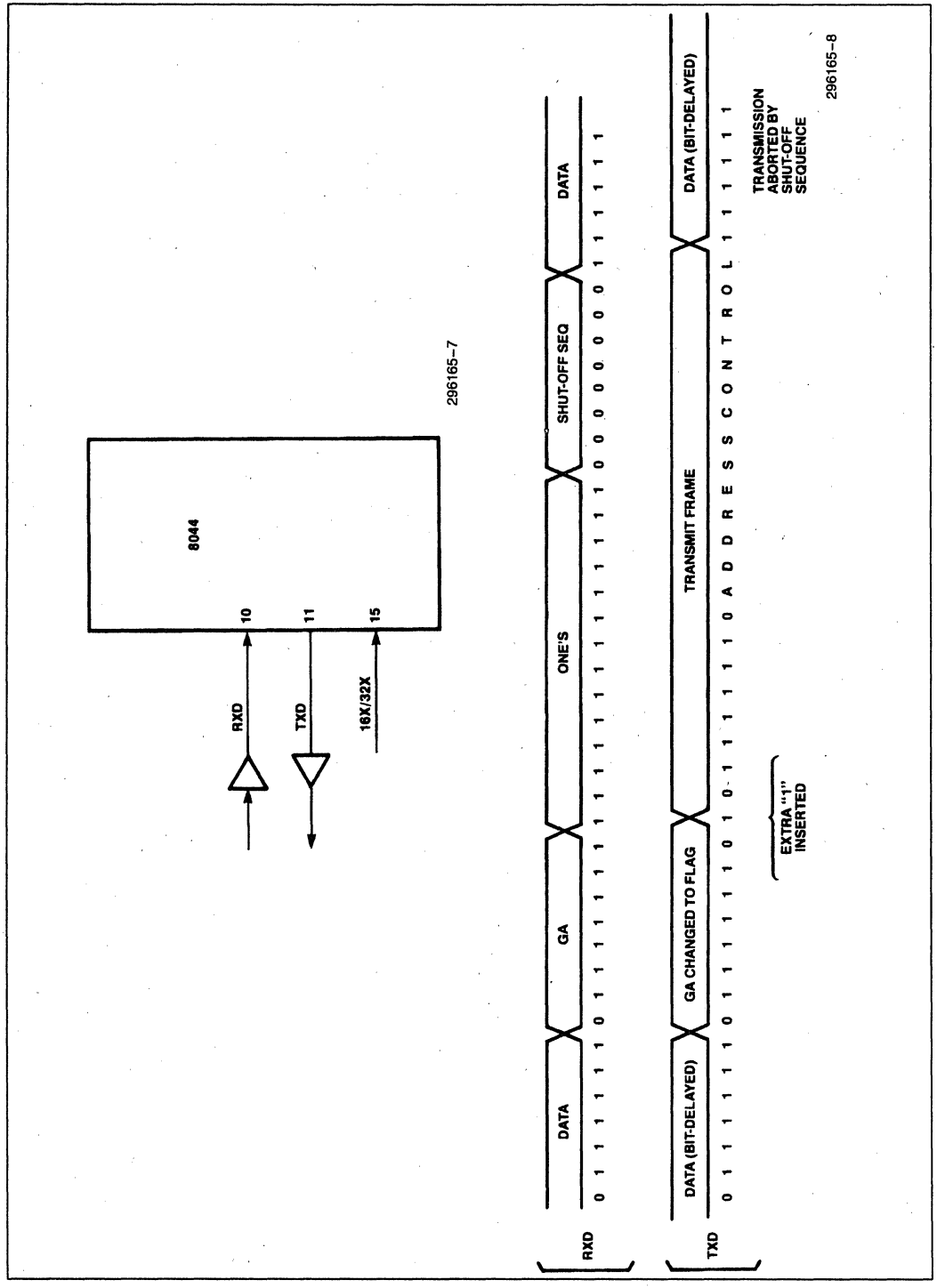

Figure 4. Serial Interface Timing—Self Clocked Mode

In addition to transmitting the information frames, the SIU in AUTO mode is capable of sending the following responses to the primary station:

RR (Receive Ready): Acknowledges that the 8044 has correctly received numbered frames up through $N_R - 1$, and that it is ready to receive frame N_R.

RNR (Receive Not Ready): Indicates a temporary busy condition (at the 8044) due to buffering or other internal constraints. The quantity N_R in the control field indicates the number of the frame expected after the busy condition ends, and acknowledges the correct reception of the frames up through $N_R - 1$.

4.2 FLEXIBLE Mode

In the FLEXIBLE (or non-auto) mode, all reception and transmission is under the control of the CPU. The full SDLC and HDLC protocols can be implemented, as well as any bit-synchronous variants of these protocols.

FLEXIBLE mode provides more flexibility than AUTO mode, but it requires more CPU overhead, and much longer recognition and response times. This is especially true when the CPU is servicing an interrupt that has higher priority than the interrupts from the SIU.

In FLEXIBLE mode, when the SIU receives a frame, it interrupts the CPU. The CPU then reads the control byte from the Receive Control Byte (RCB) register. If the received frame is an information frame, the CPU also reads the information from the receive buffer, according to the values in the Receive Buffer Start (RBS) address register and the Received Field Length (RFL) register.

In FLEXIBLE mode, the 8044 can initiate transmissions without being polled, and thus it can act as the primary station. To initiate transmission or to generate a response, the CPU sets up and enables the SIU. The SIU then formats and transmits the desired frame. Upon completion of the transmission, without waiting for a positive acknowledgement from the receiving station, the SIU interrupts the CPU.

5.0 8044 FRAME FORMAT OPTIONS

As mentioned above, variations on the basic SDLC frame consist of omitting one or more of the fields. The choice of which fields to omit, as well as the selection of AUTO mode versus FLEXIBLE mode, is specified by the settings of the following three bits in the Serial Mode Register (SMD) and the Status/Control Register (STS):

SMD Bit 0: NFCS (No Frame Check Sequence)

SMD Bit 1: NB (Non-Buffered Mode—No Control Field)

STS Bit 1: AM (AUTO Mode or Addressed Mode)

Figure 5 shows how these three bits control the frame format.

The following paragraphs discuss some properties of the standard SDLC format, and the significance of omitting some of the fields.

5.1 Standard SDLC Format

The standard SDLC format consists of an opening flag, an 8-bit address field, an 8-bit control field, an n-byte information field, a 16-bit Frame Check Sequence (FCS), and a closing flag. The FCS is based on the CCITT-CRC polynominal ($X^{16} + X^{12} + X^5 + 1$). The address and control fields may not be extended. Within the 8044, the address field is held in the Station Address (STAD) register, and the control field is held in the Receive Control Byte (RCB) or Transmit Control Byte (TCB) register. The standard SDLC format may be used in either AUTO mode or FLEXIBLE mode.

5.2 No Control Field (Non-Buffered Mode)

When the control field is not present, the RCB and TCB registers are not used. The information field begins immediately after the address field, or, if the address field is also absent, immediately after the opening flag. The entire information field is stored in the 8044's on-chip RAM. If there is no control field, FLEXIBLE mode must be used. Control information may, of course, be present in the information field, and in this manner the No Control Field option may be used for implementing extended control fields.

5.3 No Control Field and No Address Field

The No Address Field option is available only in conjuction with the No Control Field option. The STAD, RCB, and TCB registers are not used. When both these fields are absent, the information field begins immediately after the opening flag. The entire information field is stored in on-chip RAM. FLEXIBLE mode must be used. Formats without an address field have the following applications:

Point-to-point data links (where no addressing is necessary)

Monitoring line activity (receiving all messages regardless of the address field)

Extended addressing

FRAME OPTION	NFCS	NB	AM	FRAME FORMAT
Standard SDLC FLEXIBLE Mode	0	0	0	F | A | C | I | FCS | F
Standard SDLC AUTO Mode	0	0	1	F | A | C | I | FCS | F
No Control Field FLEXIBLE Mode	0	1	1	F | A | I | FCS | F
No Control Field No Address Field FLEXIBLE Mode	0	1	0	F | I | FCS | F
No FCS Field FLEXIBLE Mode	1	0	0	F | A | C | I | F
No FCS Field AUTO Mode	1	0	1	F | A | C | I | F
No FCS Field No Control Field FLEXIBLE Mode	1	1	1	F | A | I | F
No FCS Field No Control Field No Address Field FLEXIBLE Mode	1	1	0	F | I | F

Key to Abbreviations:

F = Flag (01111110)
A = Address Field
C = Control Field
I = Information Field
FCS = Frame Check Sequence

NOTE:
The AM bit is AUTO mode control bit when NB = 0, and Address Mode control bit when NB = 1.

Figure 5. Frame Format Options

5.4 No FCS Field

In the normal case (NFCS = 0), the last 16 bits before the closing flag are the Frame Check Sequence (FCS) field. These bits are not stored in the 8044's RAM. Rather, they are used to compute a cyclic redundancy check (CRC) on the data in the rest of the frame. A received frame with a CRC error (incorrect FCS) is ignored. In transmission, the FCS field is automatically computed by the SIU, and placed in the transmitted frame just prior to the closing flag.

The NFCS bit (SMD Bit 0) gives the user the capability of overriding this automatic feature. When this bit is set (NFCS = 1), all bits from the beginning of the information field to the beginning of the closing flag are treated as part of the information field, and are stored in the on-chip RAM. No FCS checking is done on the received frames, and no FCS is generated for the transmitted frames. The No FCS Field option may be used in conjunction with any of the other options. It is typically used in FLEXIBLE mode, although it does not strictly include AUTO mode. Use of the No FCS Field option AUTO Mode may, however, result in SDLC protocol violations, since the data integrity is not checked by the SIU.

Formats without an FCS field have the following applications:

Receiving and transmitting frames without verifying data integrity.

Using an alternate data verification algorithm.

Using an alternate CRC-16 polynomial (such as $X^{16} + X^{15} + X^2 + 1$), or a 32-bit CRC

Performing data link diagnosis by forcing false CRCs to test error detection mechanisms

In addition to the applications mentioned above, all of the format variations are useful in the support of non-standard bit-synchronous protocols.

6.0 HDLC

In addition to its support of SDLC communications, the 8044 also supports some of the capabilities of HDLC. The following remarks indicate the principal differences between SDLC and HDLC.

HDLC permits any number of bits in the information field, whereas SDLC requires a byte structure (multiple of 8 bits). The 8044 itself operates on byte boundaries, and thus it restricts fields to multiples of 8 bits.

HDLC provides functional extensions to SDLC: an unlimited address field is allowed, and extended frame number sequencing.

HDLC does not support operation in loop configurations.

7.0 SIU SPECIAL FUNCTION REGISTERS

The 8044 CPU communicates with and controls the SIU through hardware registers. These registers are accessed using direct addressing. The SIU special function registers (SIU SFRs) are of three types:

Control and Status Registers

Parameter Registers

ICE Support Registers

7.1 Control and Status Registers

There are three SIU Control and Status Registers:

Serial Mode Register (SMD)

Status/Command Register (STS)

Send/Receive Count Register (NSNR)

The SMD, STS, and NSNR registers are all cleared by system reset. This assures that the SIU will power up in an idle state (neither receiving nor transmitting).

These registers and their bit assignments are described below (see also the More Details on Registers section).

SMD: SERIAL MODE REGISTER (BYTE-ADDRESSABLE)

Bit: 7 6 5 4 3 2 1 0

SCM2	SCM1	SCM0	NRZI	LOOP	PFS	NB	NFCS

The Serial Mode Register (Address C9H) selects the operational modes of the SIU. The 8044 CPU can both read and write SMD. The SIU can read SMD but cannot write to it. To prevent conflict between CPU and SIU access to SMD, the CPU should write SMD only when the Request To Send (RTS) and Receive Buffer Empty (RBE) bits (in the STS register) are both false (0). Normally, SMD is accessed only during initialization.

The individual bits of the Serial Mode Register are as follows:

Bit #	Name	Description
SMD.0	NFCS	No FCS field in the SDLC frame.
SMD.1	NB	Noon-Buffered mode. No control field in the SDLC frame.
SMD.2	PFS	Pre-Frame Sync mode. In this mode, the 8044 transmits two bytes before the first flag of a frame, for DPLL synchronization. If NRZI is enabled, 00H is sent; otherwise, 55H is sent. In either case, 16 pre-frame transitions are guaranteed.
SMD.3	LOOP	Loop configuration.
SMD.4	NRZI	NRZI coding option.
SMD.5	SCM0	Select Clock Mode—Bit 0
SMD.6	SCM1	Select Clock Mode—Bit 1
SMD.7	SCM2	Select Clock Mode—Bit 2

The SCM bits decode as follows:

SCM 2 1 0	Clock Mode	Data Rate (Bits/sec)*
0 0 0	Externally clocked	0–2.4M**
0 0 1	Undefined	
0 1 0	Self clocked, timer overflow	244–62.5K
0 1 1	Undefined	
1 0 0	Self clocked, external 16x	0–375K
1 0 1	Self clocked, external 32x	0–187.5K
1 1 0	Self clocked, internal fixed	375K
1 1 1	Self clocked, internal fixed	187.5K

*Based on a 12 MHz crystal frequency
**0–1M bps in loop configuration

STS: STATUS/COMMAND REGISTER (BIT-ADDRESSABLE)

Bit:	7	6	5	4	3	2	1	0
	TBF	RBE	RTS	SI	BOV	OPB	AM	RBP

The Status/Command Register (Address C8H) provides operational control of the SIU by the 8044 CPU, and enables the SIU to post status information for the CPU's access. The SIU can read STS, and can alter certain bits, as indicated below. The CPU can both read and write STS asynchronously. However, 2-cycle instructions that access STS during both cycles ('JBC/B, REL' and 'MOV /B,C.') should not be used, since the SIU may write to STS between the two CPU accesses.

The individual bits of the Status/Command Register are as follows:

Bit#	Name	Description
STS.0	RBP	Receive Buffer Protect. Inhibits writing of data into the receive buffer. In AUTO mode, RBP forces an RNR response instead of an RR.
STS.1	AM	AUTO Mode/Addressed Mode. Selects AUTO mode where AUTO mode is allowed. If NB is true, (= 1), the AM bit selects the addressed mode. AM may be cleared by the SIU.
STS.2	OPB	Optional Poll Bit. Determines whether the SIU will generate an AUTO response to an optional poll (UP with P = 0). OPB may be set or cleared by the SIU.
STS.3	BOV	Receive Buffer Overrun. BOV may be set or cleared by the SIU.
STS.4	SI	SIU Interrupt. This is one of the five interrupt sources to the CPU. The vector location = 23H. SI may be set by the SIU. It should be cleared by the CPU before returning from an interrupt routine.
STS.5	RTS	Request To Send. Indicates that the 8044 is ready to transmit or is transmitting. RTS may be read or written by the CPU. RTS may be read by the SIU, and in AUTO mode may be written by the SIU.
STS.6	RBE	Receive Buffer Empty. RBE can be thought of as Receive Enable. RBE is set to one by the CPU when it is ready to receive a frame, or has just read the buffer, and to zero by the SIU when a frame has been received.
STS.7	TBF	Transmit Buffer Full. Written by the CPU to indicate that it has filled the transmit buffer. TBF may be cleared by the SIU.

NSNR: SEND/RECEIVE COUNT REGISTER (BIT-ADDRESSABLE)

Bit:	7	6	5	4	3	2	1	0
	NS2	NS1	NS0	SES	NR2	NR1	NR0	SER

The Send/Receive Count Register (Address D8H) contains the transmit and receive sequence numbers, plus tally error indications. The SIU can both read and write NSNR. The 8044 CPU can both read and write NSNR asynchronously. However, 2-cycle instructions that access NSNR during both cycles ('JBC /B, REL', and 'MOV /B,C') should not be used, since the SIU may write to NSNR between the two 8044 CPU accesses.

The individual bits of the Send/Receive Count Register are as follows:

Bit#	Name	Description
NSNR.0	SER	Receive Sequence Error: NS (P) ≠ NR (S)
NSNR.1	NR0	Receive Sequence Counter—Bit 0
NSNR.2	NR1	Receive Sequence Counter—Bit 1
NSNR.3	NR2	Receive Sequence Counter—Bit 2
NSNR.4	SES	Send Sequence Error: NR (P) ≠ NS (S) and NR (P) ≠ NS (S) + 1
NSNR.5	NS0	Send Sequence Counter—Bit 0
NSNR.6	NS1	Send Sequence Counter—Bit 1
NSNR.7	NS2	Send Sequence Counter—Bit 2

7.2 Parameter Registers

There are eight parameter registers that are used in connection with SIU operation. All eight registers may be read or written by the 8044 CPU. RFL and RCB are normally loaded by the SIU.

The eight parameter registers are as follows:

STAD: STATION ADDRESS REGISTER (BYTE-ADDRESSABLE)

The Station Address register (Address CEH) contains the station address. To prevent access conflict, the CPU

should access STAD only when the SIU is idle (RTS = 0 and RBE = 0). Normally, STAD is accessed only during initialization.

TBS: TRANSMIT BUFFER START ADDRESS REGISTER (BYTE-ADDRESSABLE)

The Transmit Buffer Start address register (Address DCH) points to the location in on-chip RAM for the beginning of the I-field of the frame to be transmitted. The CPU should access TBS only when the SIU is not transmitting a frame (when TBF = 0).

TBL: TRANSMIT BUFFER LENGTH REGISTER (BYTE-ADDRESSABLE)

The Transmit Buffer Length register (Address DBH) contains the length (in bytes) of the I-field to be transmitted. A blank I-field (TBL = 0) is valid. The CPU should access TBL only when the SIU is not transmitting a frame (when TBF = 0).

NOTE:
The transmit and receive buffers are not allowed to "wrap around" in the on-chip RAM. A "buffer end" is automatically generated if address 191 (BFH) is reached.

TCB: TRANSMIT CONTROL BYTE REGISTER (BYTE-ADDRESSABLE)

The Transmit Control Byte register (Address DAH) contains the byte which is to be placed in the control field of the transmitted frame, during NON-AUTO mode transmission. The CPU should access TCB only when the SIU is not transmitting a frame (when TBF = 0). The N_S and N_R counters are not used in the NON-AUTO mode.

RBS: RECEIVE BUFFER START ADDRESS REGISTER (BYTE-ADDRESSABLE)

The Receive Buffer Start address register (Address CCH) points to the location in on-chip RAM where the beginning of the I-field of the frame being received is to be stored. The CPU should write RBS only when the SIU is not receiving a frame (when RBE = 0).

RBL: RECEIVE BUFFER LENGTH REGISTER (BYTE-ADDRESSABLE)

The Receive Buffer Length register (Address CBH) contains the length (in bytes) of the area in on-chip RAM allocated for the received I-field. RBL = 0 is valid. The CPU should write RBL only when RBE = 0.

RFL: RECEIVE FIELD LENGTH REGISTER (BYTE-ADDRESSABLE)

The Received Field Length register (Address CDH) contains the length (in bytes) of the received I-field that has just been loaded into on-chip RAM. RFL is loaded by the SIU. RFL = 0 is valid. RFL should be accessed by the CPU only when RBE = 0.

RCB: RECEIVE CONTROL BYTE REGISTER (BYTE-ADDRESSABLE)

The Received Control Byte register (Address CAH) contains the control field of the frame that has just been received. RCB is loaded by the SIU. The CPU can only read RCB, and should only access RCB when RBE = 0.

7.3 ICE Support Registers

The 8044 In-Circuit Emulator (ICE-44) allows the user to exercise the 8044 application system and monitor the execution of instructions in real time.

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The emulator operates with Intel's Intellec® development system. The development system interfaces with the user's 8044 system through an in-cable buffer box. The cable terminates in a 8044 pin-compatible plug, which fits into the 8044 socket in the user's system. With the emulator plug in place, the user can exercise his system in real time while collecting up to 255 instruction cycles of real-time data. In addition, he can single-step the program.

Static RAM is available (in the in-cable buffer box) to emulate the 8044 internal and external program memory and external data memory. The designer can display and alter the contents of the replacement memory in the buffer box, the internal data memory, and the internal 8044 registers, including the SFRs.

Among the SIU SFRs are the following registers that support the operation of the ICE:

DMA CNT: DMA COUNT REGISTER (BYTE-ADDRESSABLE)

The DMA Count register (Address CFH) indicates the number of bytes remaining in the information block that is currently being used.

FIFO: THREE-BYTE (BYTE-ADDRESSABLE)

The Three-Byte FIFO (Address DDH, DEH, and DFH) is used between the eight-bit shift register and the information buffer when an information block is received.

SIUST: SIU STATE COUNTER (BYTE-ADDRESSABLE)

The SIU State Counter (Address D9H) reflects the state of the internal logic which is under SIU control. Therefore, care must be taken not to write into this register.

The SIUST register can serve as a helpful aid to determine which field of a receive frame that the SIU expects next. The table below will help in debugging 8044 reception problems.

SIUST Value	Function
01H	Waiting for opening flag.
08H	Waiting for address field.
10H	Waiting for control field.
18H	Waiting for first byte of I field. This state is only entered if a FCS is expected. It pushes the received byte onto the top of the FIFO.
20H	Waiting for second byte of I field. This state always follows state 18H.
28H	Waiting for I field byte. This state can be entered from state 20H or from states 01H, 08H, or 10H depending upon the SIU's mode configuration. (Each time a byte is received, it is pushed onto the top of the FIFO and the byte at the bottom is put into memory. For no FCS formatted frames, the FIFO is collapsed into a single register).
30H	Waiting for the closing flag after having overflowed the receive buffer. Note that even if the receive frame overflows the assigned receive buffer length, the FCS is still checked.

Examples of SIUST status sequences for different frame formats are shown below. Note that status changes after acceptance of the received field byte.

Table 1. SIUST Status Sequences

										Frame Option		
										NFCS	NB	AM
Example 1:												
Frame Format	(Idle)	F	A	C	I			FCS	F	0	0	1
SIUST Value	01	01	08	10	18	20	28	28	01			
Example 2:												
Frame Format	(Idle)	F	A	I			FCS	F		0	1	1
SIUST Value	01	01	08	18	20	28	28	01				
Example 3:												
Frame Format	(Idle)	F	I			FCS	F			0	1	0
SIUST Value	01	01	18	20	28	28	01					
Example 4:												
Frame Format	(Idle)	F	A	I	F					1	1	1
SIUST Value	01	01	08	28	01							
Example 5:												
Frame Format	(Idle)	F	I		F					1	1	0
SIUST Value	01	01	28		01							
Example 6:												
Frame Format	(Idle)	F	I			I OVERFLOW		FCS	F	0	1	0
SIUST Value	01	01	18	20	28	30		30	01			

8.0 OPERATION

The SIU is initialized by a reset signal (on pin 9), followed by write operations to the SIU SFRs. Once initialized, the SIU can function in AUTO mode or NON-AUTO mode. Details are given below.

8.1 Initialization

Figure 6 is the SIU. Registers SMD, STS, and NSNR are cleared by reset. This puts the 8044 into an idle state—neither receiving nor transmitting. The following registers must be initialized before the 8044 leaves the idle state:

STAD — to establish the 8044's SDLC station address.

SMD — To configure the 8044 for the proper operating mode.

RBS, RBL — to define the area in RAM allocated for the Receive Buffer.

TBS, TBL — to define the area in RAM allocated for the Transmit Buffer.

Once these registers have been initialized, the user may write to the STS register to enable the SIU to leave the idle state, and to begin transmits and/or receives.

Setting RBE to 1 enables the SIU for receive. When RBE = 1, the SIU monitors the received data stream for a flag pattern. When a flag pattern is found, the SIU enters Receive mode and receives the frame.

Setting RTS to 1 enables the SIU for transmit. When RTS = 1, the SIU monitors the received data stream for a GA pattern (loop configuration) or waits for a CTS (non-loop configuration). When the GA or CTS arrives, the SIU enters Transmit mode and transmits a frame.

In AUTO mode, the SIU sets RTS to enable automatic transmissions of appropriate responses.

12

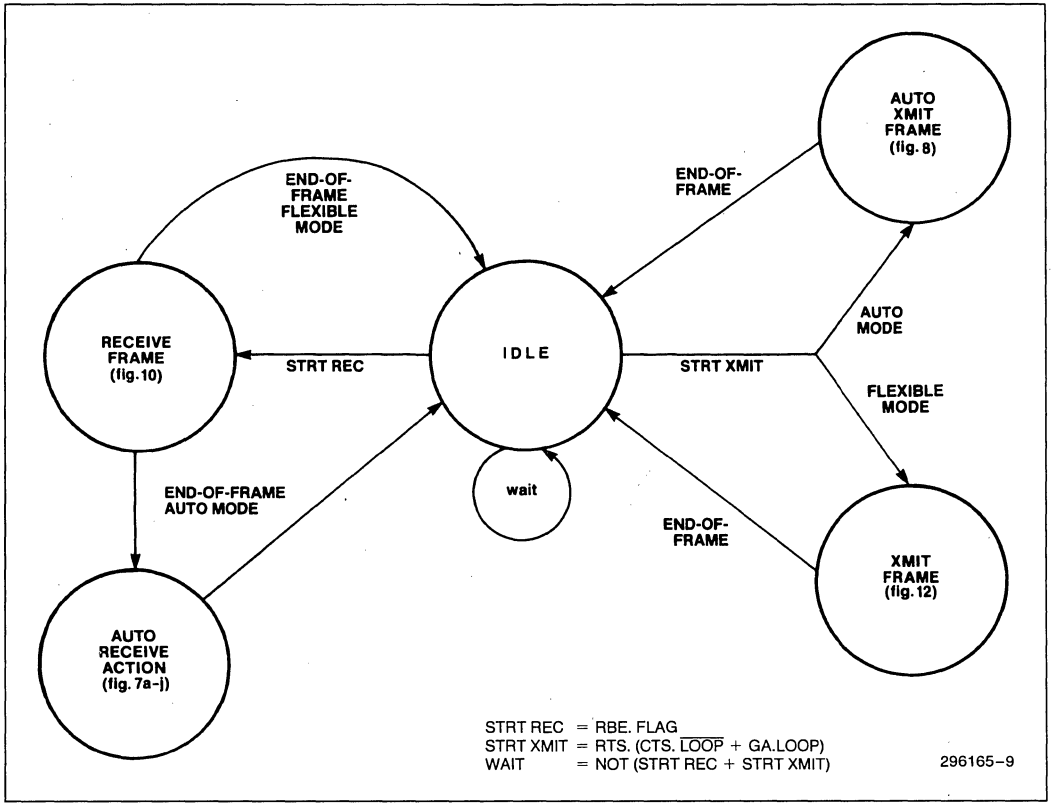

Figure 6. SIU State Diagram

8.2 AUTO Mode

Figure 7 illustrates the receive operations in AUTO mode. The overall operation is shown in Figure 7a. Particular cases are illustrated in Figures 7b through 7j. If any Unnumbered Command other than UP is received, the AM bit is cleared and the SIU responds as if in the FLEXIBLE mode, by interrupting the CPU for supervision. This will also happen if a BOV or SES condition occurs. If the received frame contains a poll, the SIU sets the RTS bit to generate a response.

Figure 8 illustrates the transmit operations in AUTO mode. When the SIU gets the opportunity to transmit, and if the transmit buffer is full, it sends an I-frame. Otherwise, it sends an RR if the buffer is free, or an RNR if the buffer is protected. The sequence counters NS and NR are used to construct the appropriate control fields.

Figure 9 shows how the CPU responds to an SI (serial interrupt) in AUTO mode. The CPU tests the AM bit (in the STS register). If AM = 1, it indicates that the SIU has received either an I-frame, or a positive response to a previously transmitted I-frame.

8.3 FLEXIBLE Mode

Figure 10 illustrates the receive operations in NON-AUTO mode. When the SIU successfully completes a task, it clears RBF and interrupts the CPU by setting SI to 1. The exact CPU response to SI is determined by software. A typical response is shown in Figure 11.

Figure 12 illustrates the transmit operations in FLEXIBLE mode. The SIU does not wait for a positive acknowledge response to the transmitted frame. Rather, it interrupts the CPU (by setting SI to 1) as soon as it finishes transmitting the frame. The exact CPU response to SI is determined by software. A typical response is shown in Figure 13. This response results in another transmit frame being set up. The sequence of operations shown in Figure 13 can also be initiated by the CPU, without an SI. Thus the CPU can initiate a transmission in FLEXIBLE mode without a poll, simply by setting the RTS bit in the STS register. The RTS bit is always used to initiate a transmission, but it is applied to the RTS pin only when a non-loop configuration is used.

8.4 8044 Data Link Particulars

The following facts should be noted:

1) In a non-loop configuration, one or two bits are transmitted before the opening flag. This is necessary for NRZI synchronization.
2) In a non-loop configuration, one to eight extra dribble bits are transmitted after the closing flag. These bits are a zero followed by ones.
3) In a loop configuration, when a GA is received and the 8044 begins transmitting, the sequence is 01111110101111110 ... (FLAG, 1, FLAG, ADDRESS, etc.). The first flag is created from the GA. The second flag begins the message.
4) CTS is sampled after the rising edge of the serial data, at about the center of the bit cell, except during a non-loop, externally clocked mode transmit, in which case it is sampled just after the falling edge.
5) The SIU does not check for illegal I-fields. In particular, if a supervisory command is received in AUTO mode, and if there is also an I-field, it will be loaded into the receive buffer (if RBP = 0), but it cannot cause a BOV.
6) In relation to the Receive Buffer Protect facility, the user should set RFL to 0 when clearing RBP, such that, if the SIU is in the process of receiving a frame, RFL will indicate the proper value when reception of the frame has been completed.

8.5 Turn Around Timing

In AUTO mode, the SIU generates an RTS immediately upon being polled. Assuming that the 8044 sends an information frame in response to the poll, the primary station sends back an acknowledgement. If, in this acknowledgement, the 8044 is polled again, a response may be generated even before the CPU gets around to processing the interrupt caused by the acknowledge. In such a case, the response would be an RR (or RNR), since TBF would have been set to 0 by the SIU, due to the acknowledge.

If the system designer does not wish to take up channel time with RR responses, but prefers to generate a new I-frame as a response, there are several ways to accomplish this:

1) Operate the 8044 in FLEXIBLE mode.
2) Specify that the master should never acknowledge and poll in one message. This is typically how a loop system operates, with the poll operation confined to the UP command. This leaves plenty of time for the 8044 to get its transmit buffer loaded with new information after an acknowledge.
3) The 8044 CPU can clear RTS. This will prevent a response from being sent, or abort it if it is already in progress. A system using external RTS/CTS handshaking could use a one-shot delay RTS or CTS, thereby giving the CPU more time to disable the response.

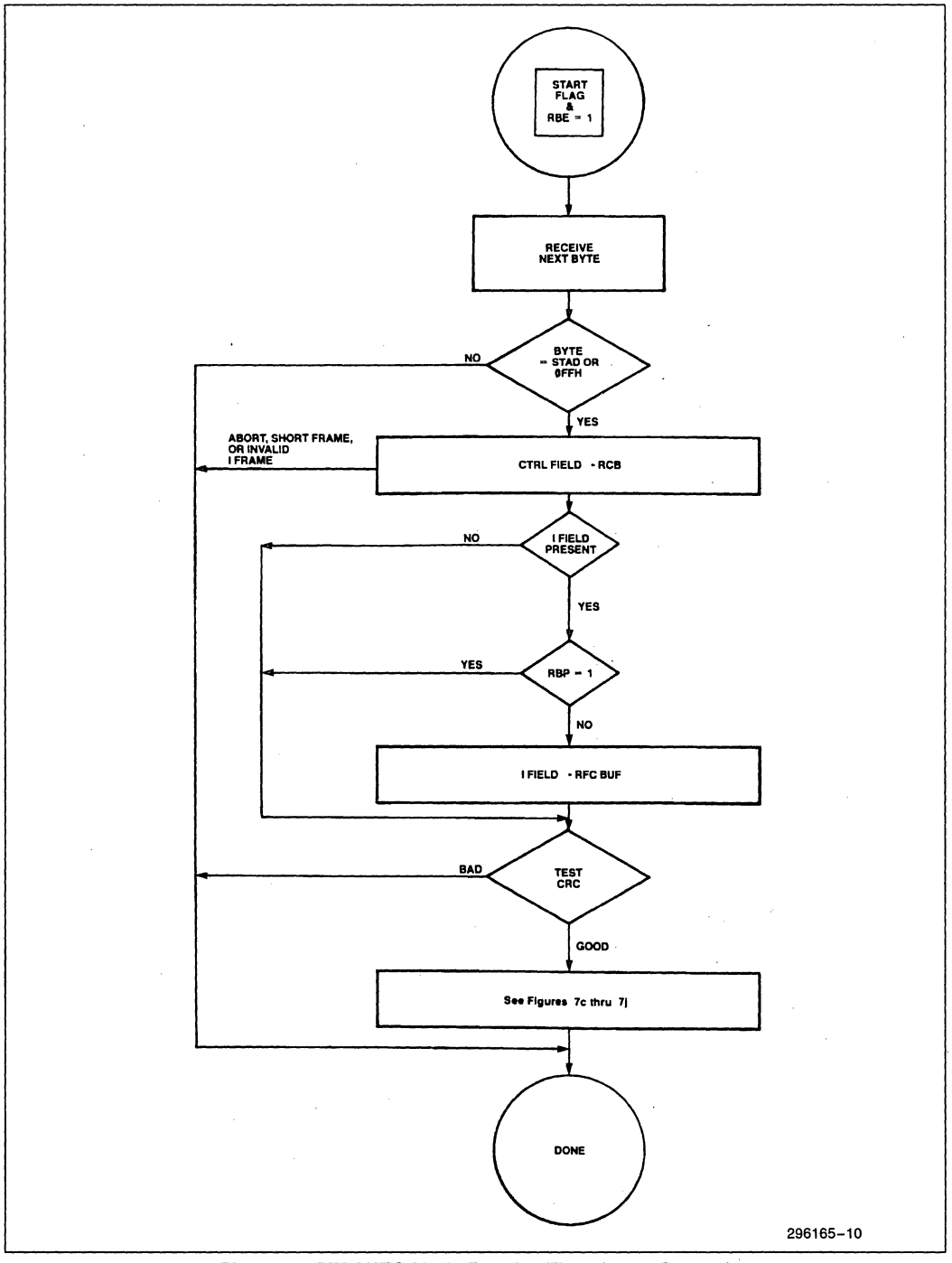

Figure 7a. SIU AUTO Mode Receive Flowchart—General

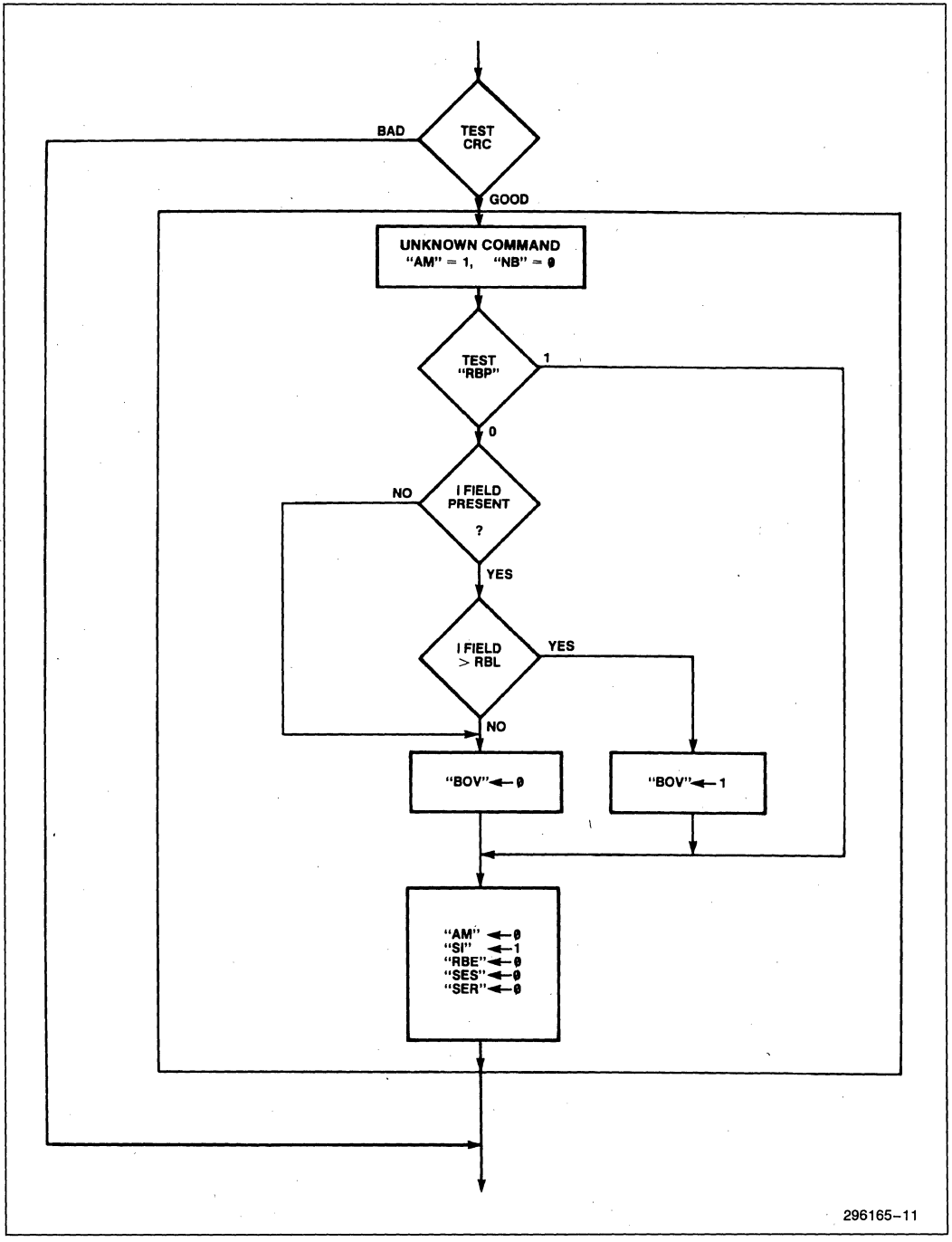

Figure 7b. SIU AUTO Mode Receive Flowchart—Unknown Command

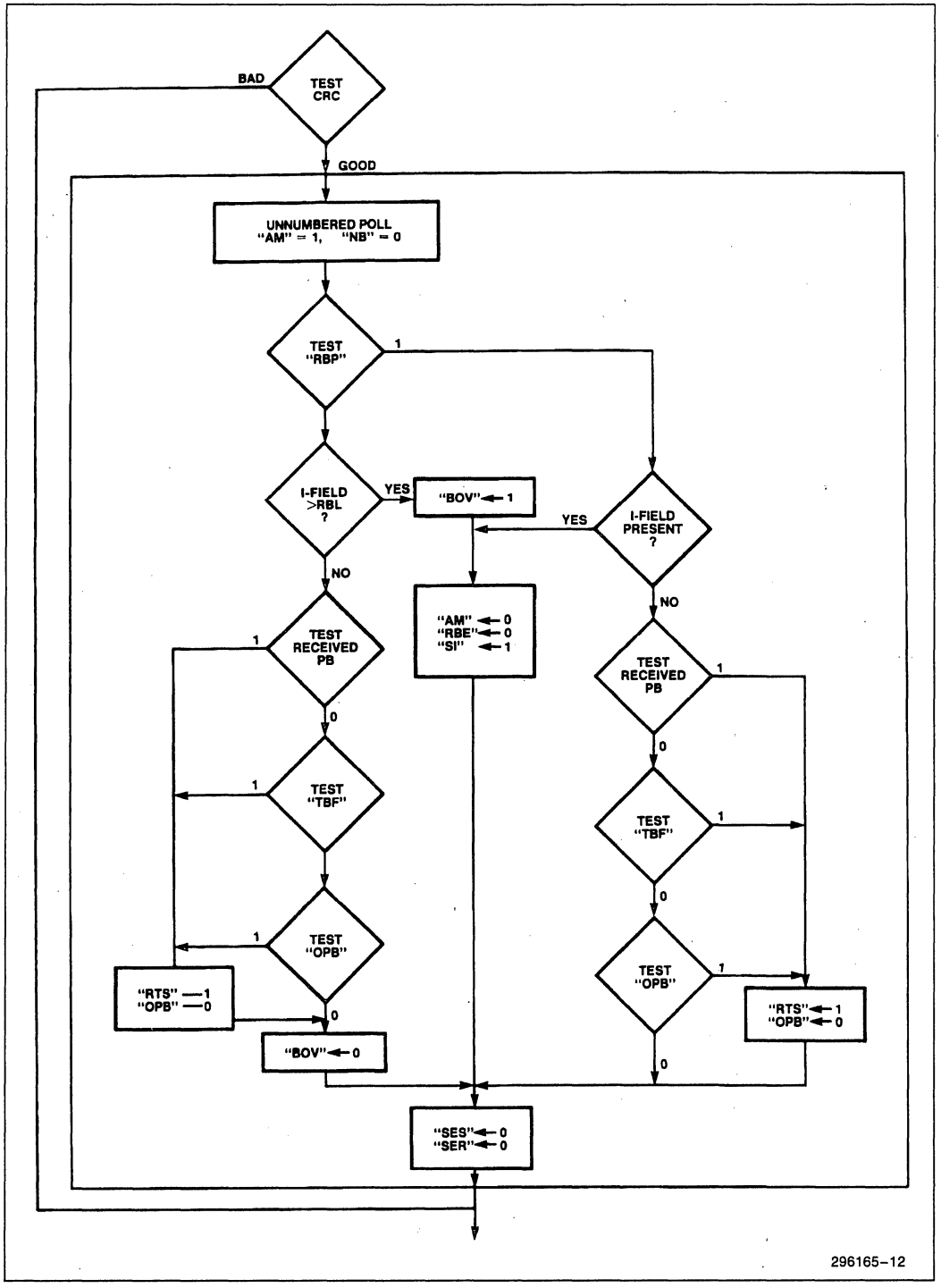

Figure 7c. SIU AUTO Mode Receive Flowchart—Unnumbered Poll

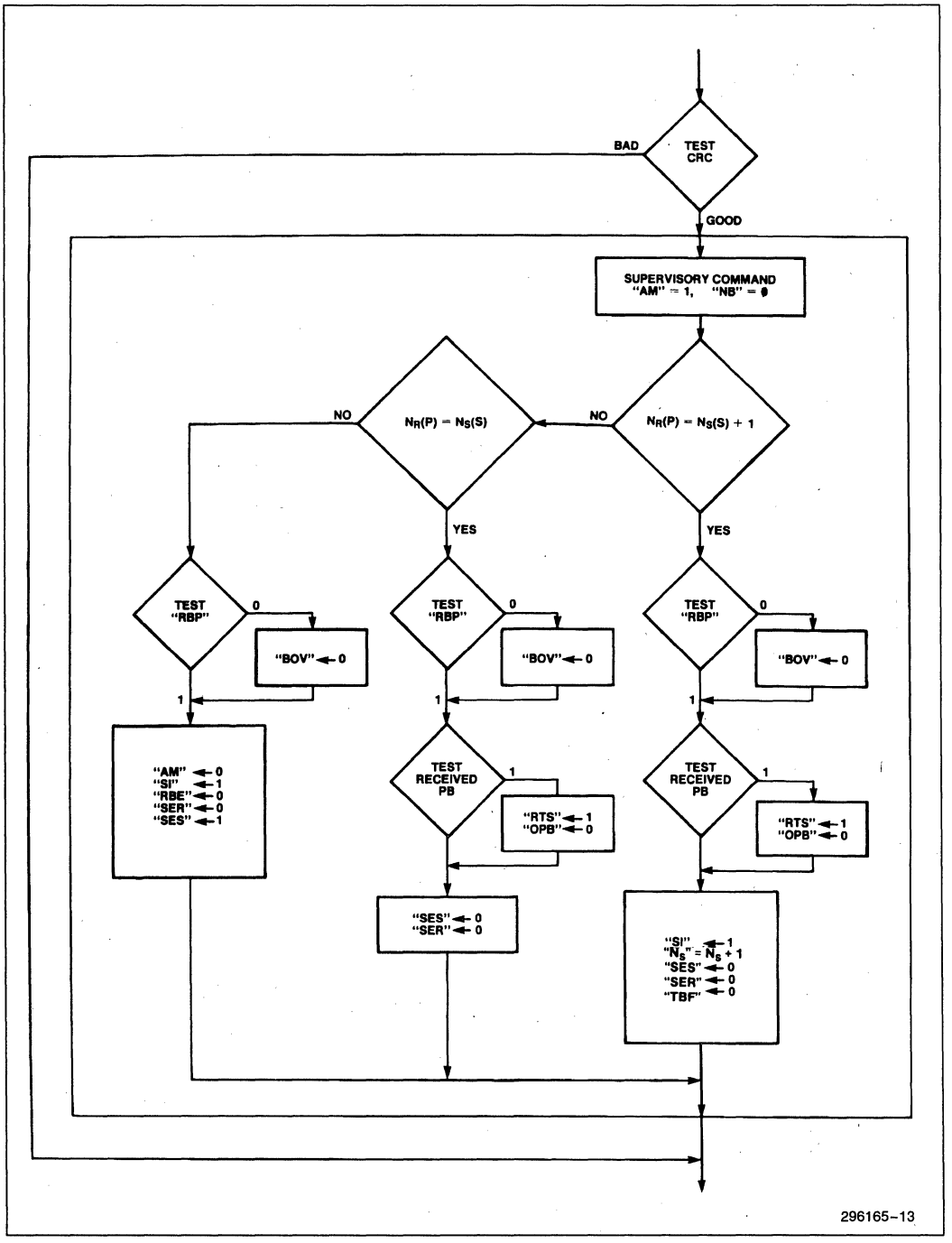

Figure 7d. SIU AUTO Mode Receive Flowchart—Supervisory Command

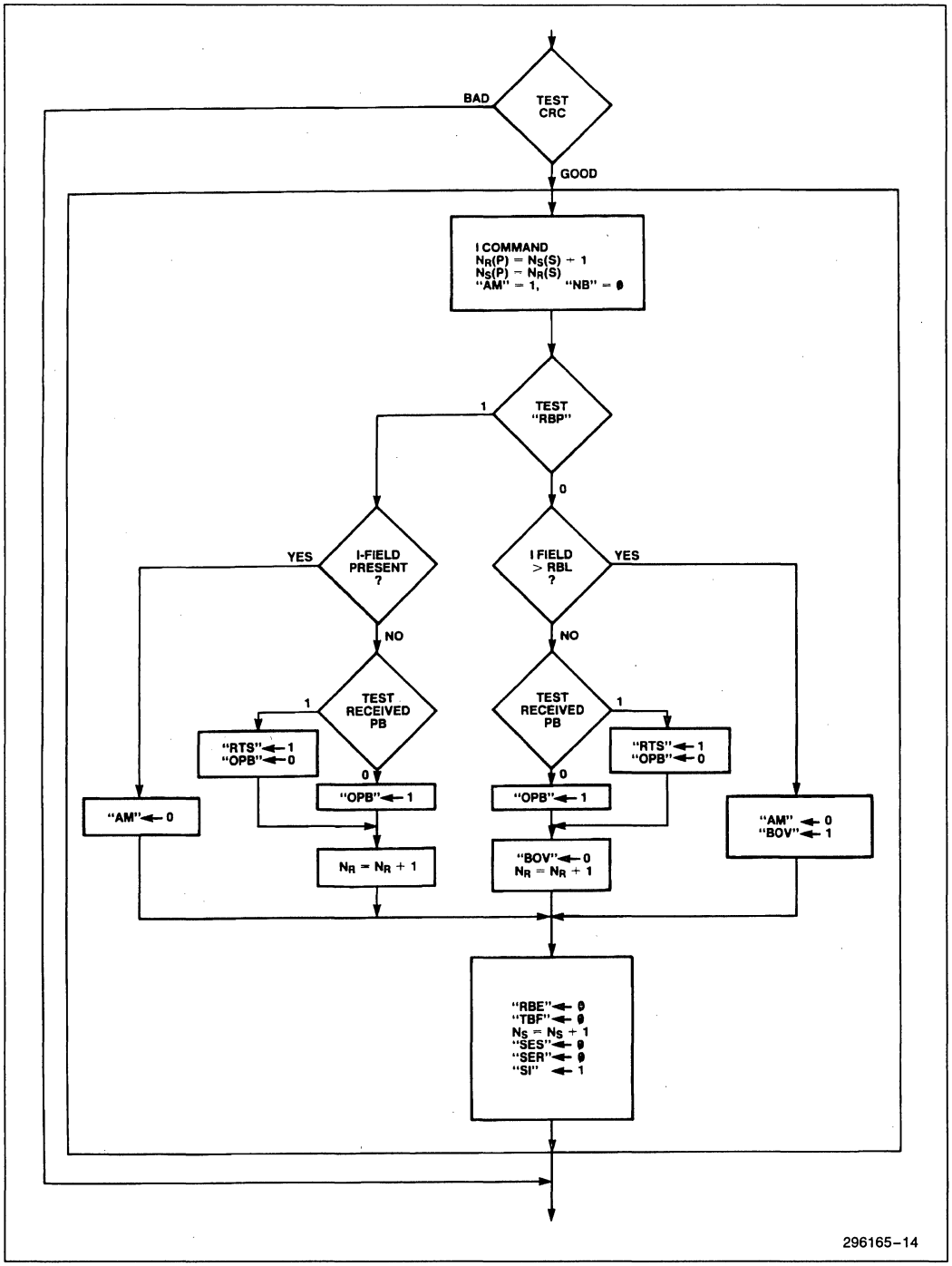

Figure 7e. SIU AUTO Mode Receive Flowchart—I Command: Prior Transmitted I-Field Confirmed, Current Received I-Field in Sequence

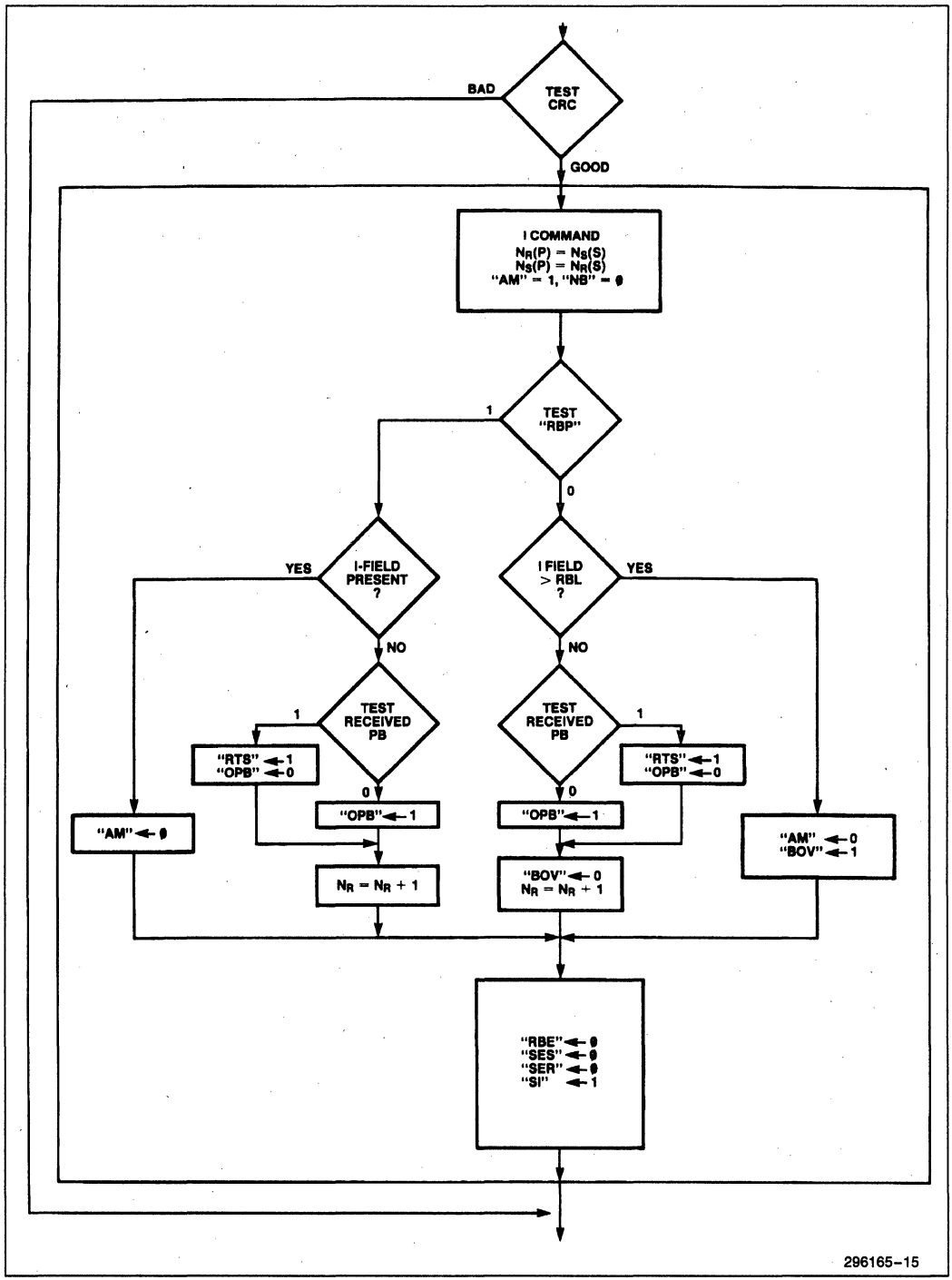

Figure 7f. SIU AUTO Mode Receive Flowchart—I Command: Prior Transmitted I-Field Not Confirmed, Current Received I-Field in Sequence

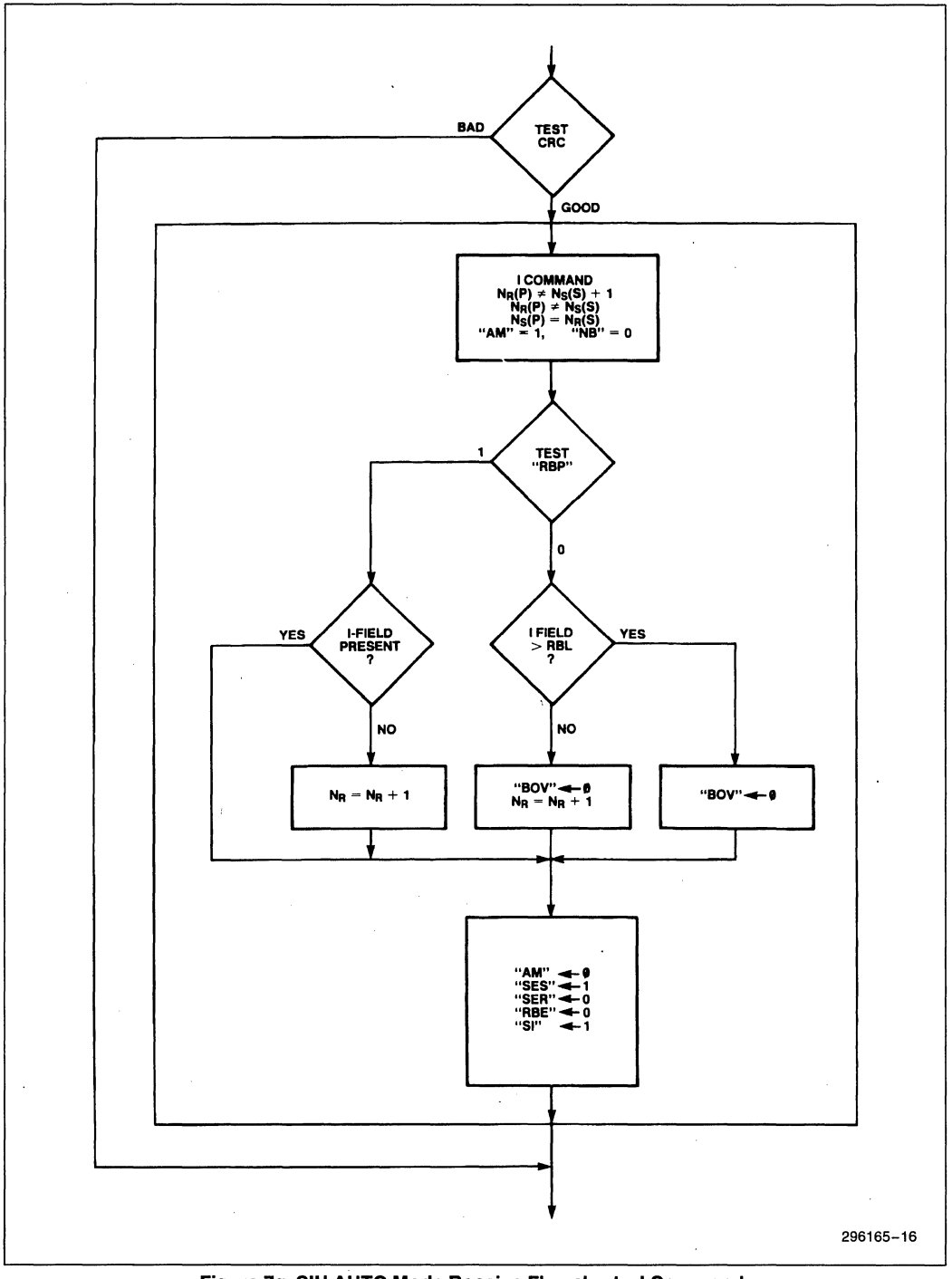

Figure 7g. SIU AUTO Mode Receive Flowchart—I Command: Sequence Error Send, Current Received I-Field in Sequence

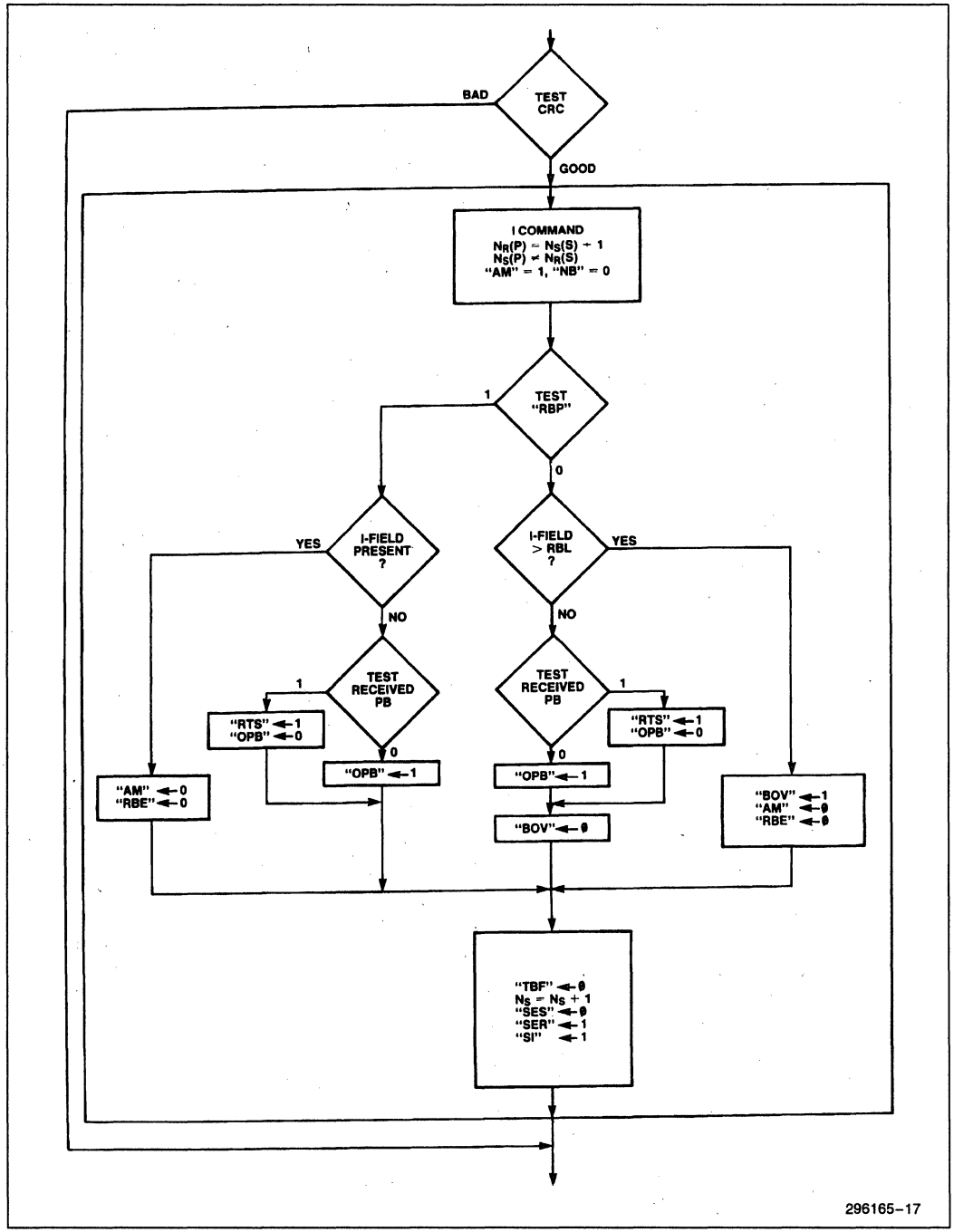

Figure 7h. SIU AUTO Mode Receive Flowchart—I Command: Prior Transmitted I-Field Confirmed Sequence Error Receive

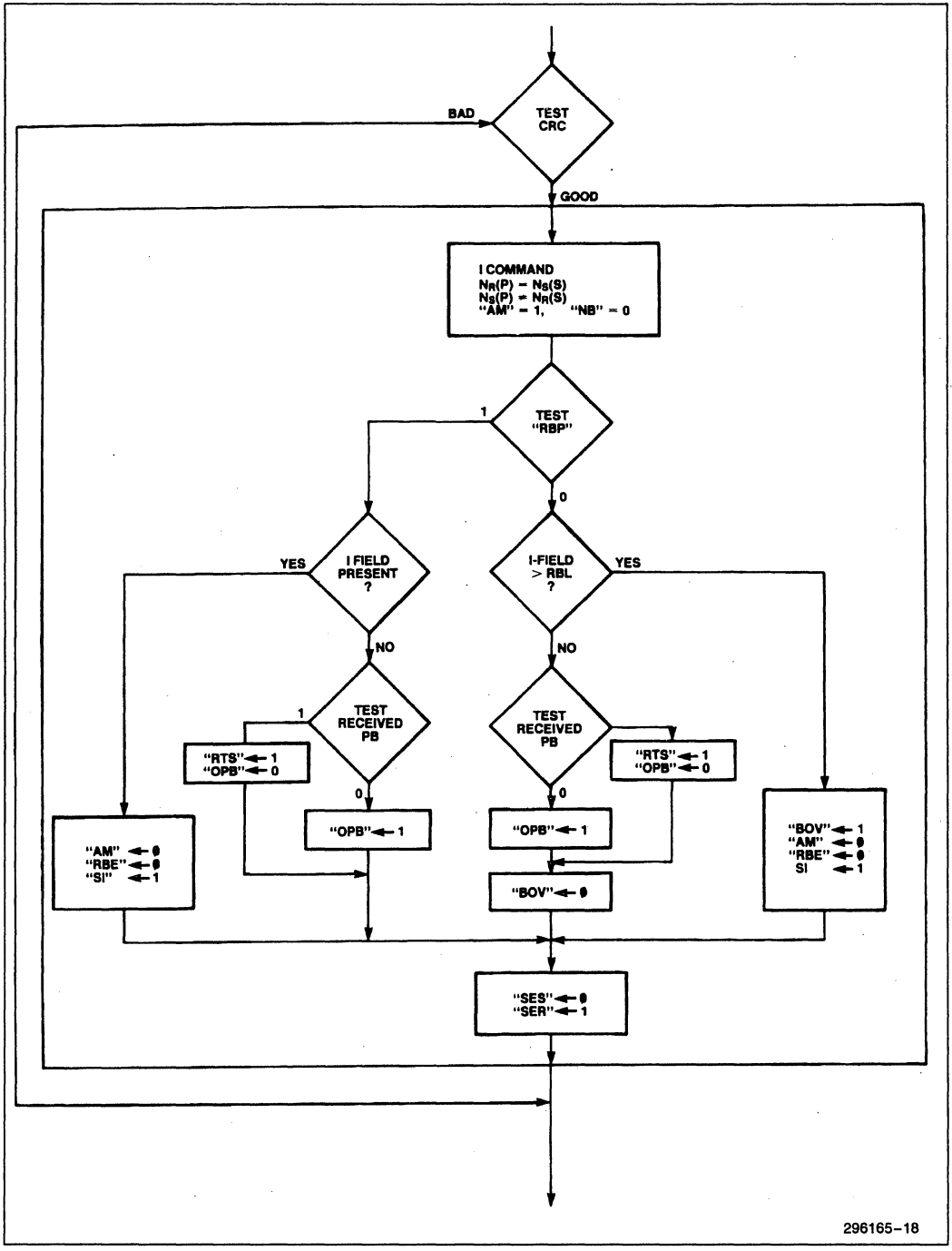

Figure 7i. SIU AUTO Mode Receive Flowchart—I Command: Prior Transmitted I-Field Not Confirmed, Sequence Error Receive

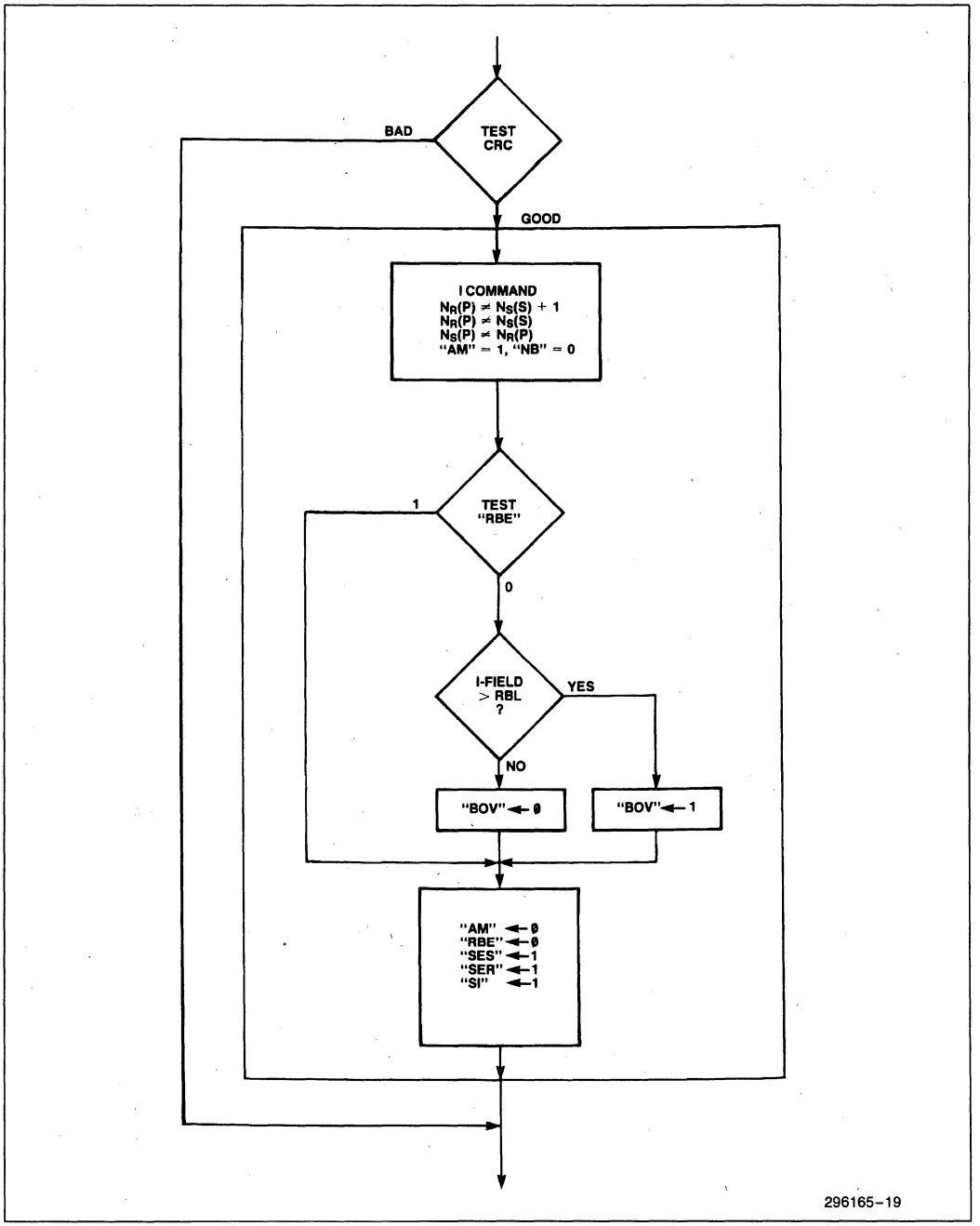

Figure 7j. SIU AUTO Mode Receive Flowchart—I Command: Sequence Error Send and Sequence Error Receive

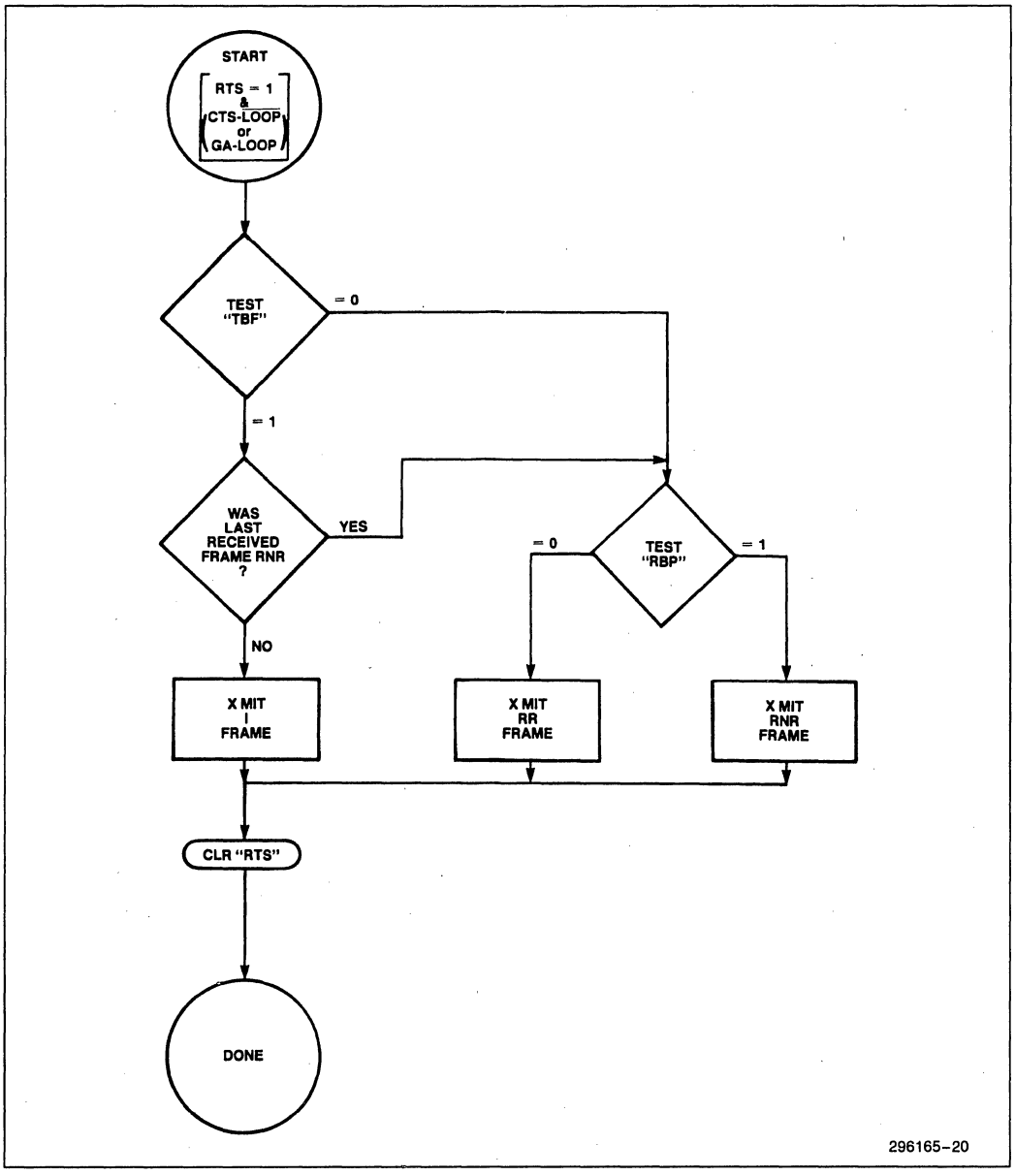

Figure 8. SIU AUTO Mode Transmit Flowchart

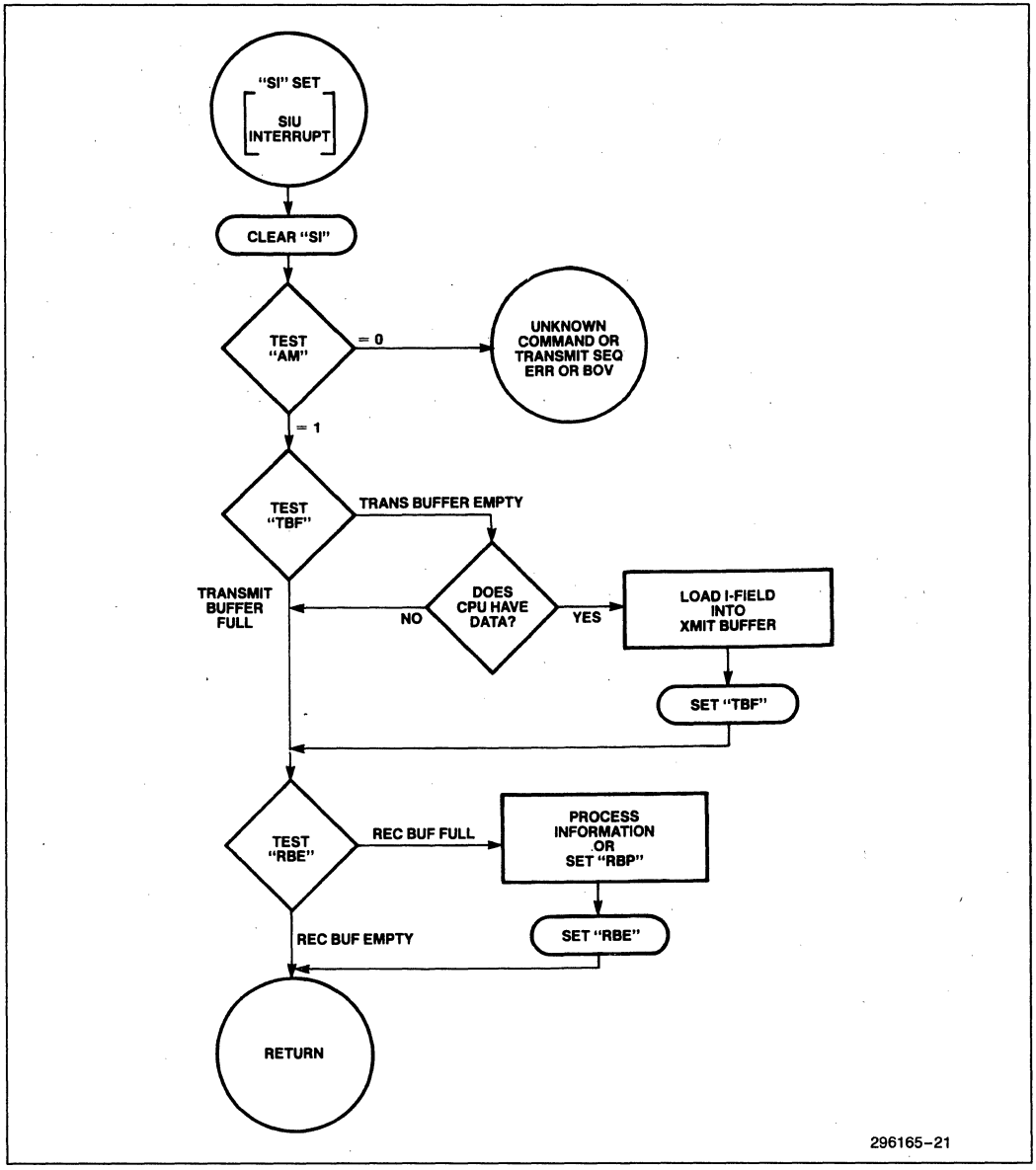

Figure 9. AUTO Mode Response to "SI"

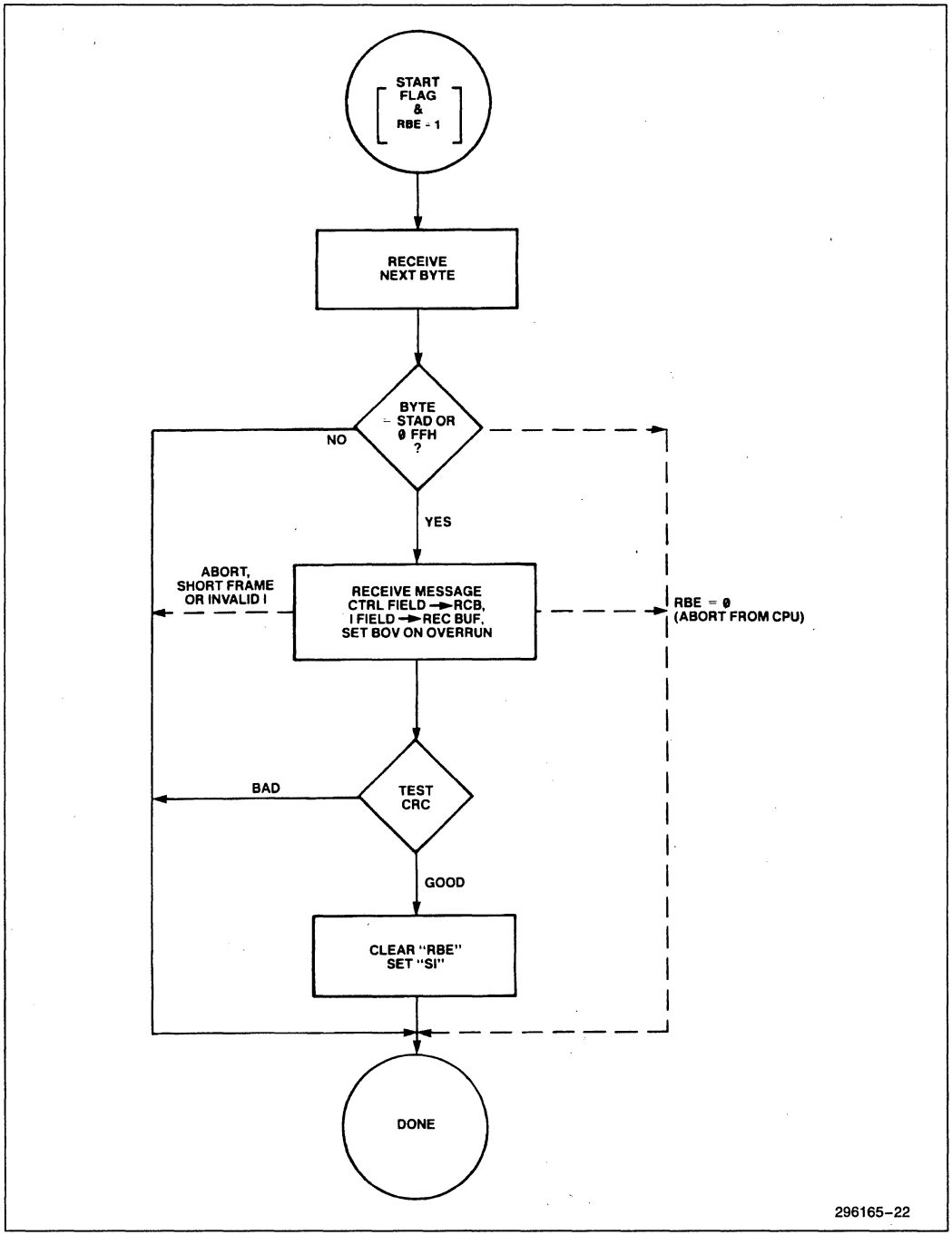

Figure 10. SIU FLEXIBLE Mode Receive Flowchart

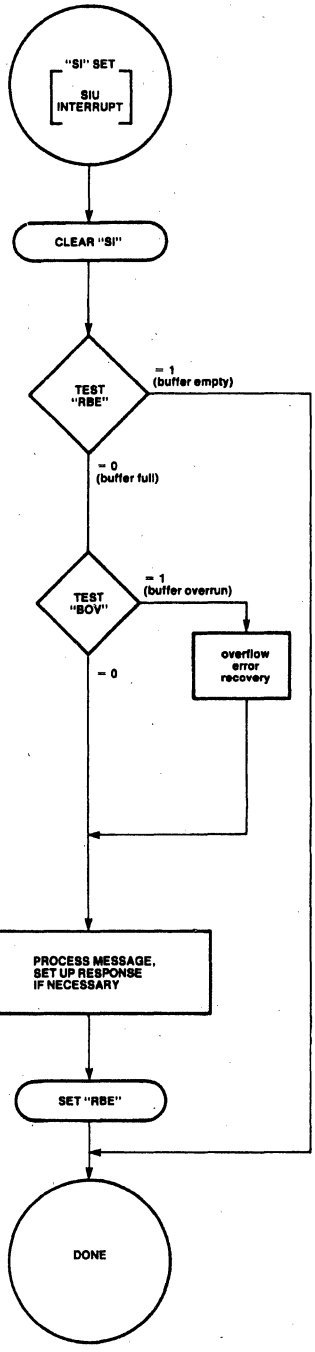

Figure 11. FLEXIBLE Mode Response to Receive "SI"

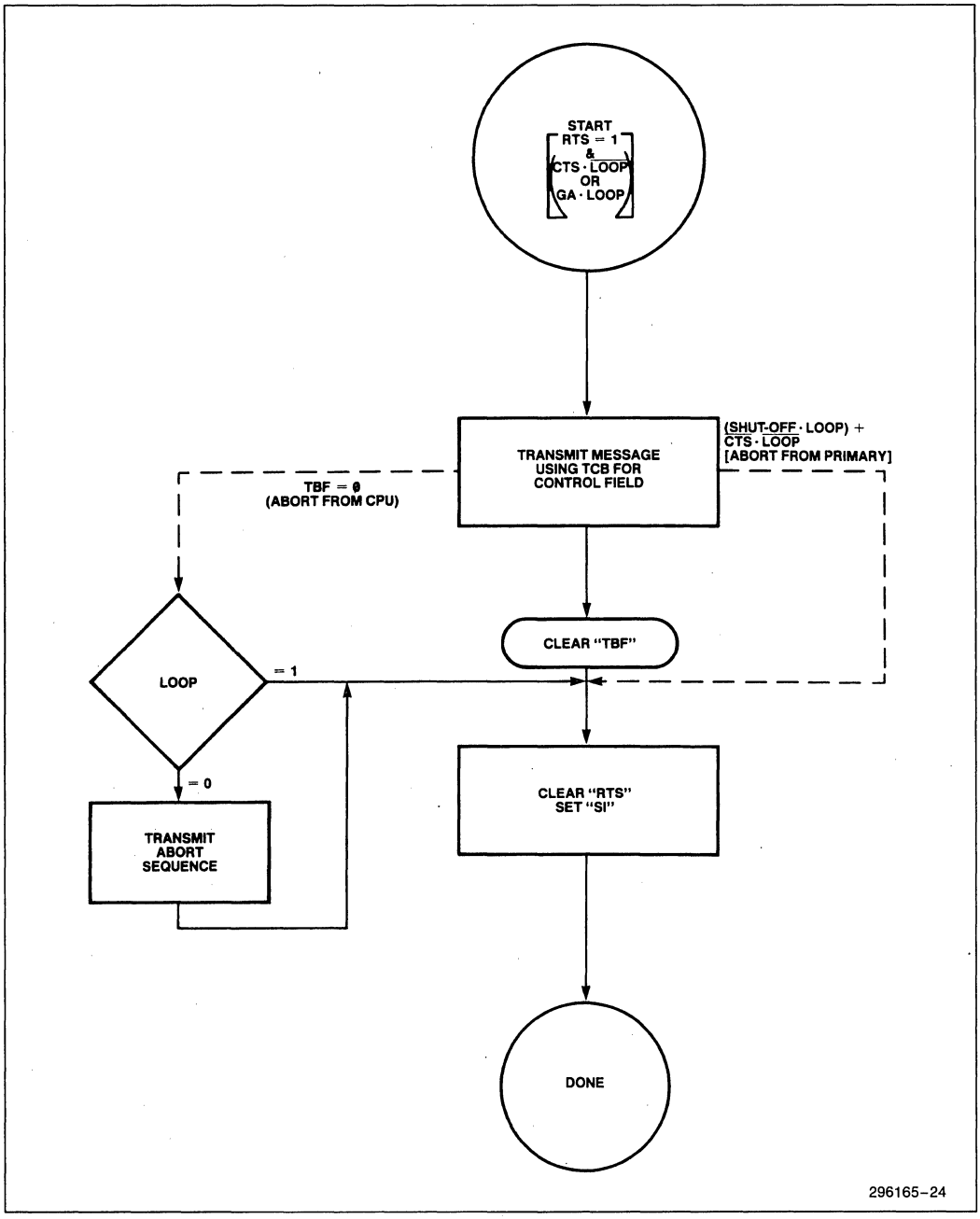

Figure 12. SIU FLEXIBLE Mode Transmit Flowchart

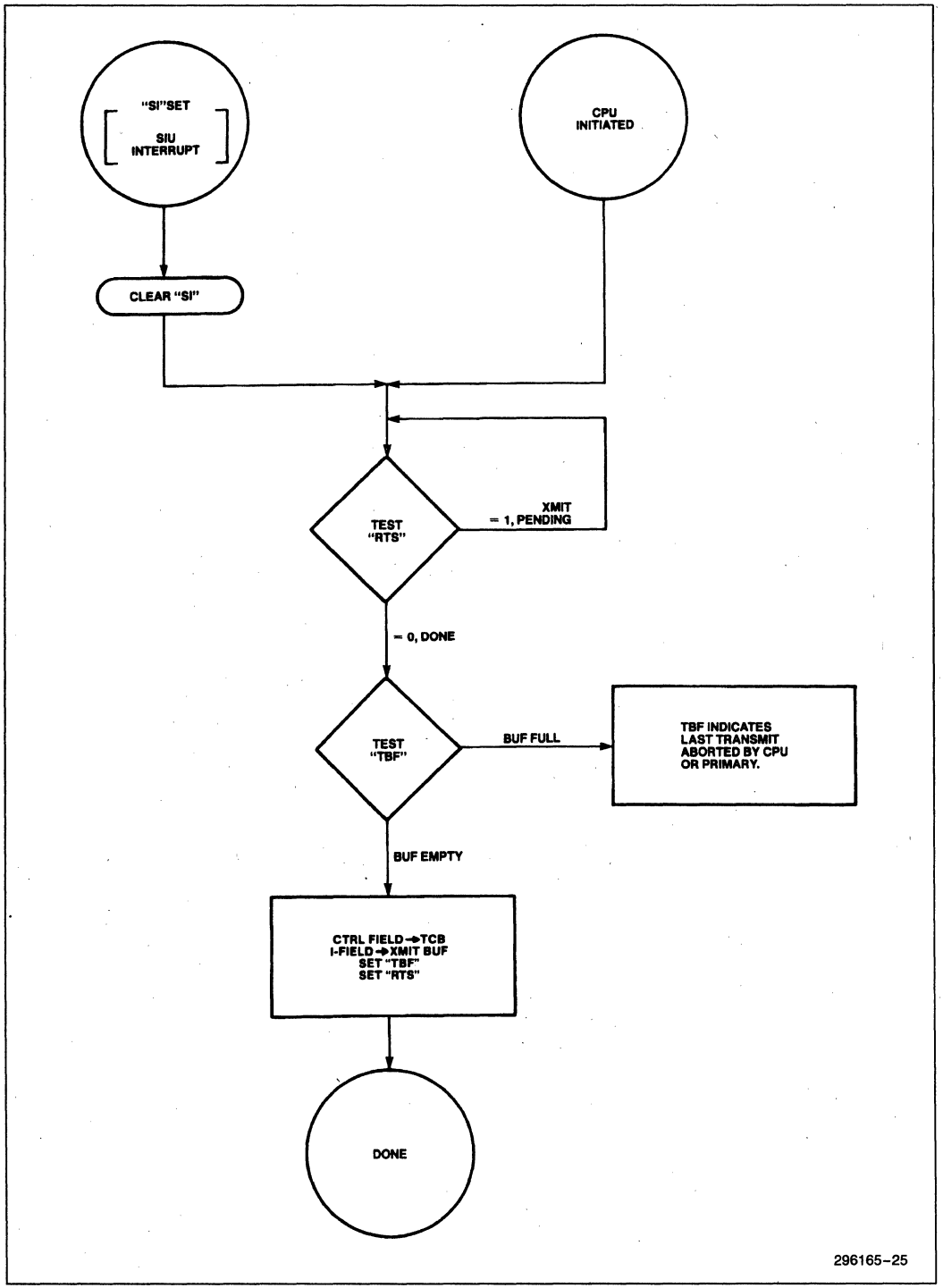

Figure 13. FLEXIBLE Mode Response to Transmit "SI"

9.0 MORE DETAILS ON SIU HARDWARE

The SIU divides functionally into two sections—a bit processor (BIP) and a byte processor (BYP)—sharing some common timing and control logic. As shown in Figure 14, the BIP operates between the serial port pins and the SIU bus, and performs all functions necessary to transmit/receive a byte of data to/from the serial data stream. These operations include shifting, NRZI encoding/decoding, zero insertion/deletion, and FCS generation/checking. The BYP manipulates bytes of data to perform message formatting, and other transmitting and receiving functions. It operates between the SIU bus (SIB) and the 8044's internal bus (IB). The interface between the SIU and the CPU involves an interrupt and some locations in on-chip RAM space which are managed by the BYP.

The maximum possible data rate for the serial port is limited to ½ the internal clock rate. This limit is imposed by both the maximum rate of DMA to the on-chip RAM, and by the requirements of synchronizing to an external clock. The internal clock rate for an 8044 running on a 12 MHz crystal is 6 MHz. Thus the maximum 8044 serial data rate is 3 MHz. This data rate drops down to 2.4 MHz when time is allowed for external clock synchronization.

9.1 The Bit Processor

In the asynchronous (self clocked) modes the clock is extracted from the data stream using the on-chip digital phase-locked-loop (DPLL). The DPLL requires a clock input at 16 times the data rate. This 16 × clock may originate from SCLK, Timer 1 Overflow, or PH2 (one half the oscillator frequency). The extra divide by-two described above allows these sources to be treated alternatively as 32 × clocks.

The DPLL is a free-running four-bit counter running off the 16 × clock. When a transition is detected in the receive data stream, a count is dropped (by suppressing the carry-in) if the current count value is greater than 8. A count is added (by injecting a carry into the second stage rather than the first) if the count is less than 8. No adjustment is made if the transition occurs at the count of 8. In this manner the counter locks in on the point at which transitions in the data stream occur at the count of 8, and a clock pulse is generated when the count overflows to 0.

In order to perform NRZI decoding, the NRZI decoder compares each bit of input data to the previous bit. There are no clock delays in going through the NRZI decoder.

The zero insert/delete circuitry (ZID) performs zero insertion/deletion, and also detects flags, GA's (Go-Ahead's), and aborts (same as GA's) in the data stream. The pattern 1111110 is detected as an early GA, so that the GA may be turned into a flag for loop mode transmission.

The shut-off detector monitors the receive data stream for a sequence of eight zeros, which is a shut-off command for loop mode transmissions. The shut-off detector is a three-bit counter which is cleared whenever a one is found in the receive data stream. Note that the ZID logic could not be used for this purpose, because the receive data must be monitored even when the ZID is being used for transmission.

As an example of the operation of the bit processor, the following sequence occurs in relation to the receive data:

1) RXD is sampled by SCLK, and then synchronized to the internal processor clock (IPC).
2) If the NRZI mode is selected, the incoming data is NRZI decoded.
3) When receiving other than the flag pattern, the ZID deletes the '0' after 5 consecutive '1's (during transmission this zero is inserted). The ZID locates the byte boundary for the rest of the circuitry. The ZID deletes the '0's by preventing the SR (shift register) from receiving a clocking pulse.
4) The FCS (which is a function of the data between the flags—not including the flags) is initialized and started at the detection of the byte boundary at the end of the opening flag. The FCS is computed each bit boundary until the closing flag is detected. Note that the received FCS has gone through the ZID during transmission.

9.2 The Byte Processor

Figure 15 is a block diagram of the byte processor (BYP). The BYP contains the registers and controllers necessary to perform the data manipulations associated with SDLC communications. The BYP registers may be read or written by the CPU over the 8044's internal bus (IB), using standard 8044 hardware register operations. The 8044 register select PLA controls these operations. Three of the BYP registers connect to the IB through the IBS, a sub-bus which also connects to the CPU interrupt control registers.

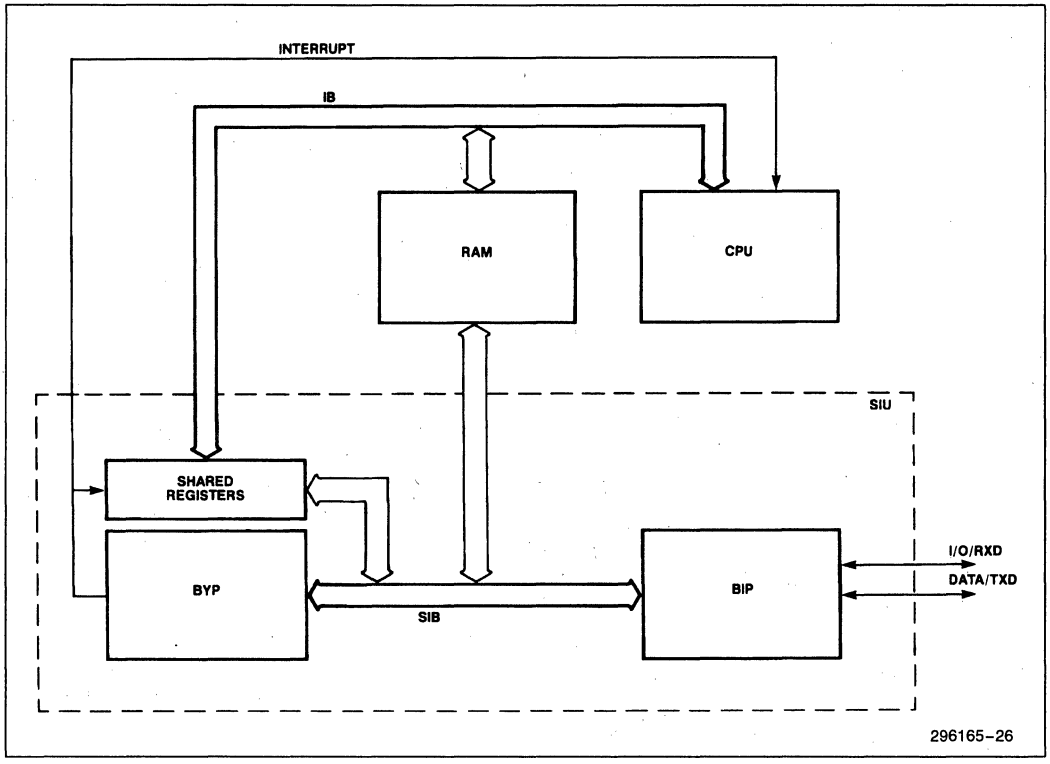

Figure 14. The Bit and Byte Processors

Simultaneous access of a register by both the IB and the SIB is prevented by timing. In particular, RAM access is restricted to alternate internal processor cycles for the CPU and the SIU, in such a way that collisions do not occur.

As an example of the operation of the byte processor, the following sequence occurs in relation to the receive data:

1) Assuming that there is an address field in the frame, the BYP takes the station address from the register file into temporary storage. After the opening flag, the next field (the address field) is compared to the station address in the temporary storage. If a match occurs, the operation continues.
2) Assuming that there is a control field in the frame, the BYP takes the next byte and loads it into the RCB register. The RCB register has the logic to update the NSNR register (increment receive count, set SES and SER flags, etc.).
3) Assuming that there is an information field, the next byte is dumped into RAM at the RBS location. The DMA CNT (RBL at the opening flag) is loaded from the DMA CNT register into the RB register and decremented. The RFL is then loaded into the RB register, incremented, and stored back into the register file.
4) This process continues until the DMA CNT reaches zero, or until a closing flag is received. Upon either event, the BYP updates the status, and, if the CRC is good, the NSNR register.

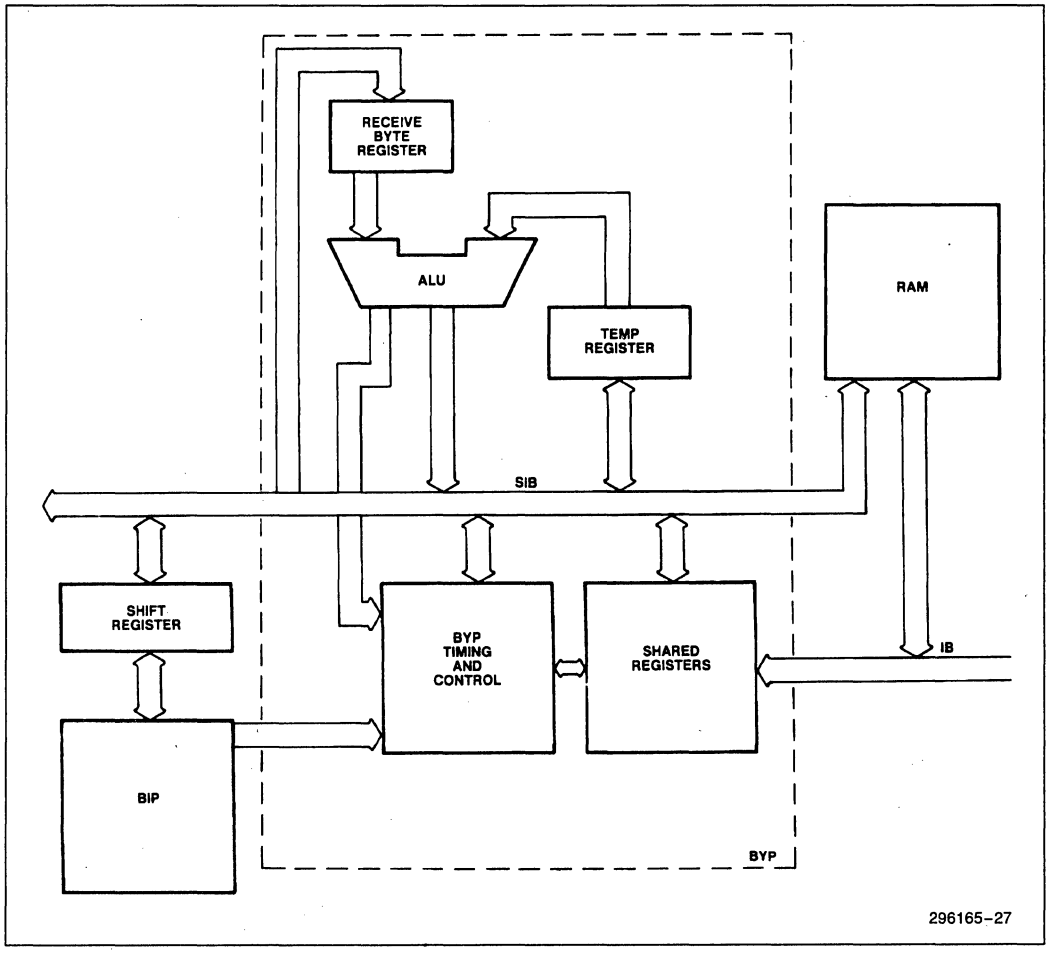

Figure 15. The Byte Processor

10.0 DIAGNOSTICS

An SIU test mode has been provided, so that the on-chip CPU can perform limited diagnostics on the SIU. The test mode utilizes the output latches for P3.0 and P3.1 (pins 10 and 11). These port 3 pins are not useful as out-put ports, since the pins are taken up by the serial port functions. Figure 16 shows the signal routing associated with the SIU test mode.

Writing a 0 to P3.1 enables the serial test mode (P3.1 is set to 1 by reset). In test mode the P3.0 bit is mapped into the received data stream, and the 'write port 3' control signal is mapped into the SCLK path in place of T1. Thus, in test mode, the CPU can send a serial data stream to the SIU by writing to P3.0. The transmit data stream can be monitored by reading P3.1. Each successive bit is transmitted from the SIU by writing to any bit in Port 3, which generates SCLK.

In test mode, the P3.0 and P3.1 pins are placed in a high voltage, high impedance state. When the CPU reads P3.0 and P3.1 the logic level applied to the pin will be returned. In the test mode, when the CPU reads 3.1, the transmit data value will be returned, not the voltage on the pin. The transmit data remains constant for a bit time. Writing to P3.0 will result in the signal being outputted for a short period of time. However, since the signal is not latched, P3.0 will quickly return to a high voltage, high impedance state.

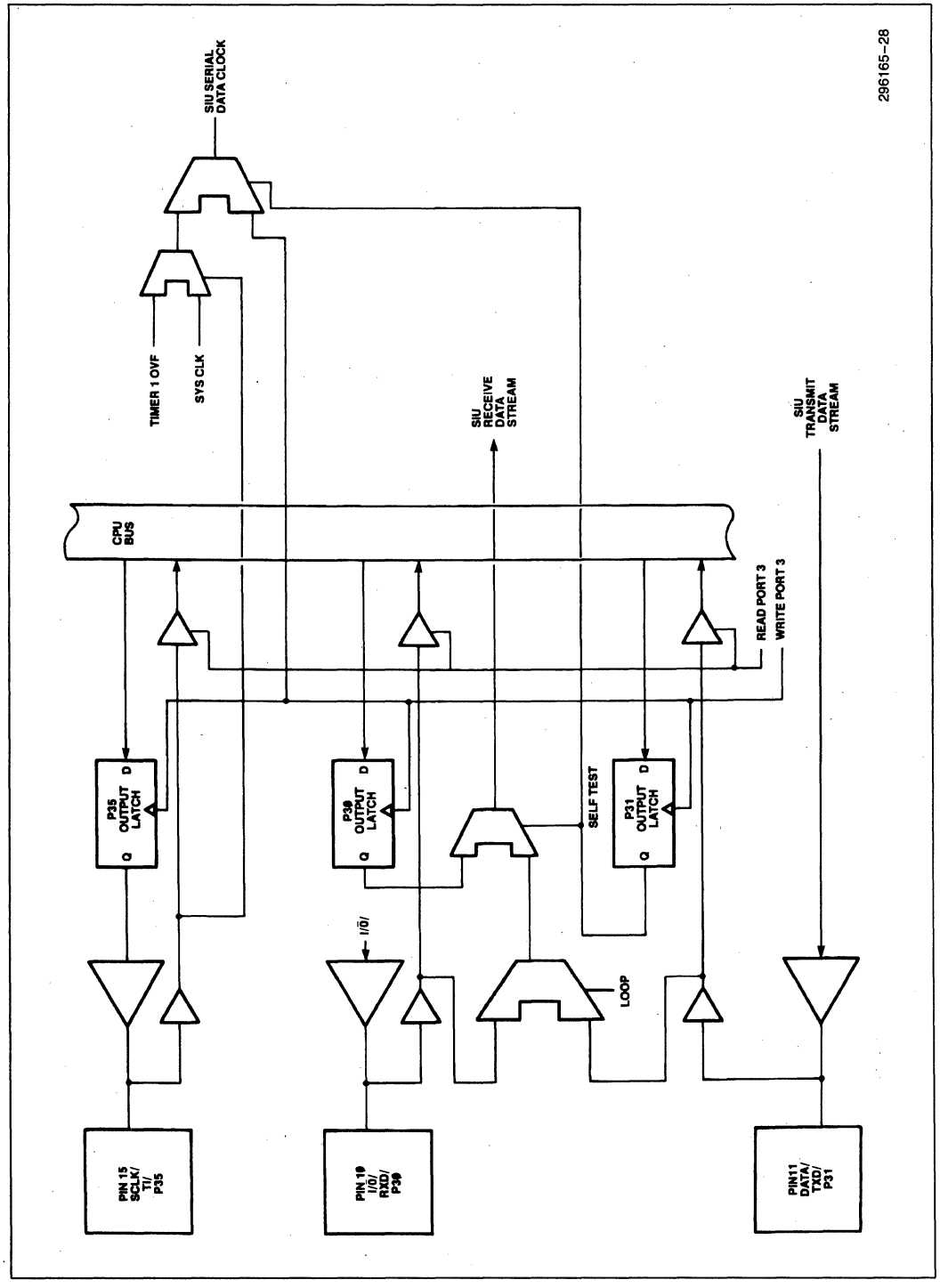

Figure 16. SIU Test Mode

The serial test mode is disabled by writing a 1 to P3.1. Care must be taken that a 0 is never written to P3.1 in the course of normal operation, since this causes the test mode to be entered.

Figure 17 is an example of a simple program segment that can be imbedded into the user's diagnostic program. That example shows how to put the 8044 into "Loop-back mode" to test the basic transmitting and receiving functions of the SIU.

Loop-back mode is functionally equivalent to a hardwire connection between pins 10 and 11 on the 8044.

In this example, the 8044 CPU plays the role of the primary station. The SIU is in the AUTO mode. The CPU sends the SIU a supervisory frame with the poll bit set and an RNR command. The SIU responds with a supervisory frame with the poll bit set and an RR command.

The operation proceeds as follows:

Interrupts are disabled, and the self test mode is enabled by writing a zero to P3.1. This establishes P3.0 as the data path from the CPU to the SIU. CTS (clear-to-send) is enabled by writing a zero to P1.7. The station address is initialized by writing 08AH into the STAD (station address register).

The SIU is configured for receive operation in the clocked mode and in AUTO mode. The CPU then transmits a supervisory frame. This frame consists of an opening flag, followed by the station address, a control field indicating that this is a supervisory frame with an RNR command, and then a closing flag.

Each byte of the frame is transmitted by writing that byte into the A register and then calling the subroutine XMIT8. Two additional SCLKs are generated to guarantee that the last bits in the frame have been clocked into the SIU. Finally the CPU reads the status register (STS). If the operation has proceeded correctly, the status will be 072H. If it is not, the program jumps to the ERROR loop and terminates.

The SIU generates an SI (SIU interrupt) to indicate that it has received a frame. The CPU clears this interrupt, and then begins to monitor the data stream that is being generated by the SIU in response to what it has received. As each bit arrives (via P3.1), it is moved into the accumulator, and the CPU compares the byte in the accumulator with 07EH, which is the opening flag. When a match occurs, the CPU identifies this as byte boundary, and thereafter processes the information byte-to-byte.

The CPU calls the RCV8 subroutine to get each byte into the accumulator. The CPU performs compare operations on (successively) the station address, the control field (which contains the RR response), and the closing flag. If any of these do not compare, the program jumps to the ERROR loop. If no error is found, the program jumps to the DONE loop.

```
MCS-51 MACRO ASSEMBLER    DATA


ISIS-II MCS-51 MACRO ASSEMBLER V2.0
OBJECT MODULE PLACED IN :F1:DATA.OBJ
ASSEMBLER INVOKED BY:  asm51 :f1:data.man device(44)


LOC  OBJ            LINE     SOURCE

                       1
                       2
0000 75C800            3     INIT:   MOV     STS,#00H
0003 C2B1              4             CLR     P3.1            ; Enable self test mode
0005 C297              5             CLR     P1.7            ; Enable CTS
0007 75CE8A            6             MOV     STAD, #8AH      ; Initialize address
                       7
                       8       ; CONFIGURE RECEIVE OPERATION
                       9
000A 75D86A           10             MOV     NSNR, #6AH      ; NS(S)=3, SES=0, NR(S)=5, SER=0
000D 75C901           11             MOV     SMD, #01H       ; NFCS=1
0010 75C8C2           12             MOV     STS, #0C2H      ; TBF=1, RBE=1, AM=1
                      13
                      14     ;    TRANSMIT A SUPERVISORY FRAME FROM THE PRIMARY STATION WITH THE POLL
                      15     ;    BIT SET AND A RNR COMMAND
                      16
0013 747E             17     SEND:   MOV     A, #7EH         ; The SIU receives a flag first
0015 120066           18             CALL    XMITB
0018 748A             19             MOV     A, #8AH         ; The address is next
001A 120066           20             CALL    XMITB
001D 7495             21             MOV     A, #095H        ; RNR SUP FRAME with P/F=1, NR(P)=4
001F 120066           22             CALL    XMITB
0022 747E             23             MOV     A, #7EH         ; Receive closing flag
0024 120066           24             CALL    XMITB
0027 D2B0             25             SETB    P3.0            ; Generate extra SCLK's to
0029 D2B0             26             SETB    P3.0            ; Initiate receive action
                      27
002B E5C8             28             MOV     A, STS          ; Check for appropriate status
002D B4722A           29             CJNE    A, #72H, ERROR
                      30
                      31     ; PREPARE TO RECEIVE RUPI'S RESPONCE TO PRIMARY'S RNR
                      32
                      33
                      34
0030 C2CC             35     RECV:   CLR     SI              ; Clear SI
0032 7400             36             MOV     A, #00H         ; Clear ACC
0034 780C             37             MOV     R3, #12         ; Try 12 times
                      38
                      39     ;  LOOK FOR THE OPENING FLAG
                      40
0036 D2B0             41     WFLAG1: SETB    P3.0            ; SCLK
0038 A2B1             42             MOV     C, P3.1         ; Transmitted data
003A 13               43             RRC     A
003B B47E03           44             CJNE    A, #07EH, WFLG1
003E 020046           45             JMP     CNTINU
0041 DBF3             46     WFLG1:  DJNZ    R3, WFLAG1
0043 02005A           47             JMP     ERROR
                      48
                      49
0046 12005C           50     CNTINU: CALL    RCVB            ; Get SIU's Transmitted address field
0049 B48A0E           51             CJNE    A, #08AH, ERROR
004C 12005C           52             CALL    RCVB            ; Primary expects to receive RR from SIU
004F B4B108           53             CJNE    A, #0B1H, ERROR
0052 12005C           54             CALL    RCVB            ; Receive closing flag
0055 B47E02           55             CJNE    A, #07EH, ERROR
                      56
0058 80FE             57     DONE:   JMP     DONE
                      58
005A 80FE             59     ERROR:  JMP     ERROR
                      60
                      61
005C 7808             62       RCVB: MOV     R0, #08         ; Initialize the bit counter
005E D2B0             63     GETBIT: SETB    P3.0            ; SCLK
0060 A2B1             64             MOV     C, P3.1         ; Transmitted data
0062 13               65             RRC     A
0063 DBF9             66             DJNZ    R0, GETBIT
0065 22               67             RET
                      68
                      69
                      70
0066 7809             71     XMITB:  MOV     R0, #9          ; Initialize the bit counter
0068 13               72        L3:  RRC     A               ; Put the bit to be transmitted
                      73                                     ; in the Carry
0069 D801             74             DJNZ    R0, L1          ; When all bits have been sent
006B 22               75             RET                     ; return
                      76
006C 4004             77          L1: JC      L2              ; If the carry bit is set, set
                      78                                     ; port P3.0 else
006E C2B0             79             CLR     P3.0            ; clear port P3.0
0070 80F6             80             JMP     L3
                      81
0072 D2B0             82          L2: SETB    P3.0
0074 80F2             83             JMP     L3
                      84     end
```

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Figure 17. Loop-Back Mode Software

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November 1989

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8044 Application Examples

Order Number: 296166-001

8044 APPLICATION EXAMPLES

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1.0 INTERFACING THE 8044 TO A MICROPROCESSOR

The 8044 is designed to serve as an intelligent controller for remote peripherals. However, it can also be used as an intelligent HDLC/SDLC front end for a microprocessor, capable of extensively off-loading link control functions for the CPU. In some applications, the 8044 can even be used for communications preprocessing, in addition to data link control.

This section describes a sample hardware interface for attaching the 8044 to an 8088. It is general enough to be extended to other microprocessors such as the 8086 or the 80186.

OVERVIEW

A sample interface is shown in Figure 1. Transmission occurs when the 8088 loads a 64 byte block of memory with some known data. The 8088 then enables the 8237A to DMA this data to the 8044. When the 8044 has received all of the data from the 8237A, it sends the data in a SDLC frame. The frame is captured by the Spectron Datascope™* which displays it on a CRT in hex format.

In reception, the Datascope sends a SDLC information frame to the 8044. The 8044 receives the SDLC frame, buffers it, and sends it to the 8088's memory. In this example the 8044 is being operated in the NON-AUTO mode; therefore, it does not need to be polled by a primary station in order to transmit.

THE INTERFACE

The 8044 does not have a parallel slave port. The 8044's 32 I/O lines can be configured as a local microprocessor bus master. In this configuration, the 8044 can expand the ROM and RAM memory, control peripherals, and communicate with a microprocessor.

The 8044, like the 8051, does not have a Ready line, so there is no way to put the 8044 in wait state. The clock on the 8044 cannot be stopped. Dual port RAM could still be used, however, software arbitration would be the only way to prevent collisions. Another way to interface the 8044 with another CPU is to put a FIFO or queue between the two processors, and this was the method chosen for this design.

Figure 2 shows the schematic of the 8044/8088 interface. It involves two 8-bit tri-state latches, two SR flip-flops, and some logic gates (6 TTL packs). The circuitry implements a one byte FIFO. RS422 transceivers are used, which can be connected to a multidrop link. Figure 3 shows the 8088 and support circuitry; the memory and decoders are not shown. It is a basic 8088 Min Mode system with an 8237A DMA controller and an 8259A interrupt controller.

*Datascope is a trademark of Spectron Inc.

DMA Channel One transfers a block of memory to the tri-state latch, while Channel Zero transfers a block of data from the latch to 8088's memory. The 8044's Interrupt 0 signal vectors the CPU into a routine which reads from the internal RAM and writes to the latch. The 8044's Interrupt 1 signal causes the chip to read from the latch and write to its on-chip data RAM. Both DMA requests and acknowledges are active low.

Initially, when the power is applied, a reset pulse coming from the 8284A initializes the SR flip-flops. In this initialization state, the 8044's transmit interrupt and the 8088's transmit DMA request are active; however, the software keeps these signals disabled until either of the two processors are ready to transmit. The software leaves the receive signals enabled, unless the receive buffers are full. In this way either the 8088 or the 8044 are always ready to receive, but they must enable the transmit signal when they have prepared a block to transmit. After a block has been transmitted or received, the DMA and interrupt signals return to the initial state.

The receive and transmit buffer sizes for the blocks of data sent between the 8044 and the 8088 have a maximum fixed length. In this case the buffer size was 64 bytes. The buffer size must be less than 192 bytes to enable 8044 to buffer the data in its on-chip RAM. This design allows blocks of data that are less than 64 bytes, and accommodates networks that allow frames of varying size. The first byte transferred between the 8088 and the 8044 is the byte count to follow; thus the 8044 knows how many bytes to receive before it transmits the SDLC frame. However, when the 8044 sends data to the 8088's memory, the 8237A will not know if the 8044 will send less than the count the 8237A was programmed for. To solve this problem, the 8237A is operated in the single mode. The 8044 uses an I/O bit to generate an interrupt request to the 8259A. In the 8088's interrupt routine, the 8237A's receive DMA channel is disabled, thus allowing blocks of data less than 64 bytes to be received.

THE SOFTWARE

The software for the 8044 and the 8088 is shown in Table 1. The 8088 software was written in PL/M86, and the 8044 software was written in assembly language.

The 8044 software begins by initializing the stack, interrupt priorities, and triggering types for the interrupts. At this point, the SIU parameter registers are

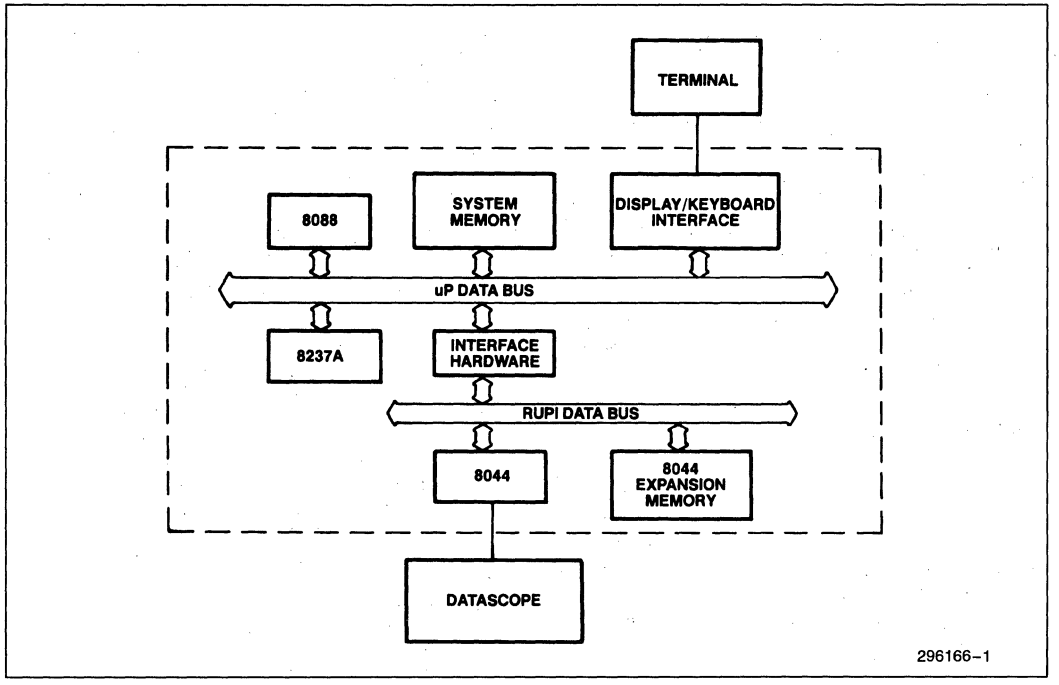

Figure 1. Block Diagram of 8088/8044 Interface Test

initialized. The receive and transmit buffer starting addresses and lengths are loaded for the on-chip DMA. This DMA is for the serial port. The serial station address and the transmit control bytes are loaded too.

Once the initialization has taken place, the SIU interrupt is enabled, and the external interrupt which receives bytes from the 8088 is enabled. Setting the 8044's Receive Buffer Empty (RBE) bit enables the receiver. If this bit is reset, no serial data can be received. The 8044 then waits in a loop for either RECEIVE DMA interrupt or the SERIAL INT interrupt.

The RECEIVE DMA interrupt occurs when the 8237A is transferring a block of data to the 8044. The first time this interrupt occurs, the 8044 reads the latch and loads the count value into the R2 register. On subsequent interrupts, the 8044 reads the latch, loads the data into the transmit buffer, and decrements R2. When R2 reaches zero, the interrupt routine sends the data in an SDLC frame, and disables the RECEIVE DMA interrupt. After the frame has been transmitted, a serial interrupt is generated. The SERIAL INT routine detects that a frame has been transmitted and re-enables the RECEIVE DMA interrupt. Thus, while the frame is being transmitted through the SIU, the 8237A is inhibited from sending data to the 8044's transmit buffer.

The TRANSMIT DMA routine sends a block of data from the 8044's receive buffer to the 8088's memory. Normally this interrupt remains disabled. However, if a serial interrupt occurs, and the SERIAL INT routine detects that a frame has been received, it calls the SEND subroutine. The SEND subroutine loads the number of bytes which were received in the frame into the receive buffer. Register R1 points to the receive buffer and R2 is loaded with the count. The TRANSMIT DMA interrupt is enabled, and immediately upon returning from the SERIAL INT routine, the interrupt is acknowledged. Each time the TRANSMIT DMA interrupt occurs, a byte is read from the receive buffer, written to the latch, and R2 is decremented. When R2 reaches 0, the TRANSMIT DMA interrupt is disabled, the SIU receiver is re-enabled, and the 8044 interrupts the 8088.

CONCLUSION

For the software shown in Table 1, the transfer rate from the 8088's memory to the 8044 was measured at 75K bytes/sec. This transfer rate largely depends upon the number of instructions in the 8044's interrupt service routine. Fewer instructions result in a higher transfer rate.

There are many ways of interfacing the 8044 locally to another microprocessor: FIFO's, dual port RAM with software arbitration, and 8255's are just a few. Alternative approaches, which may be more optimal for certain applications, are certainly possible.

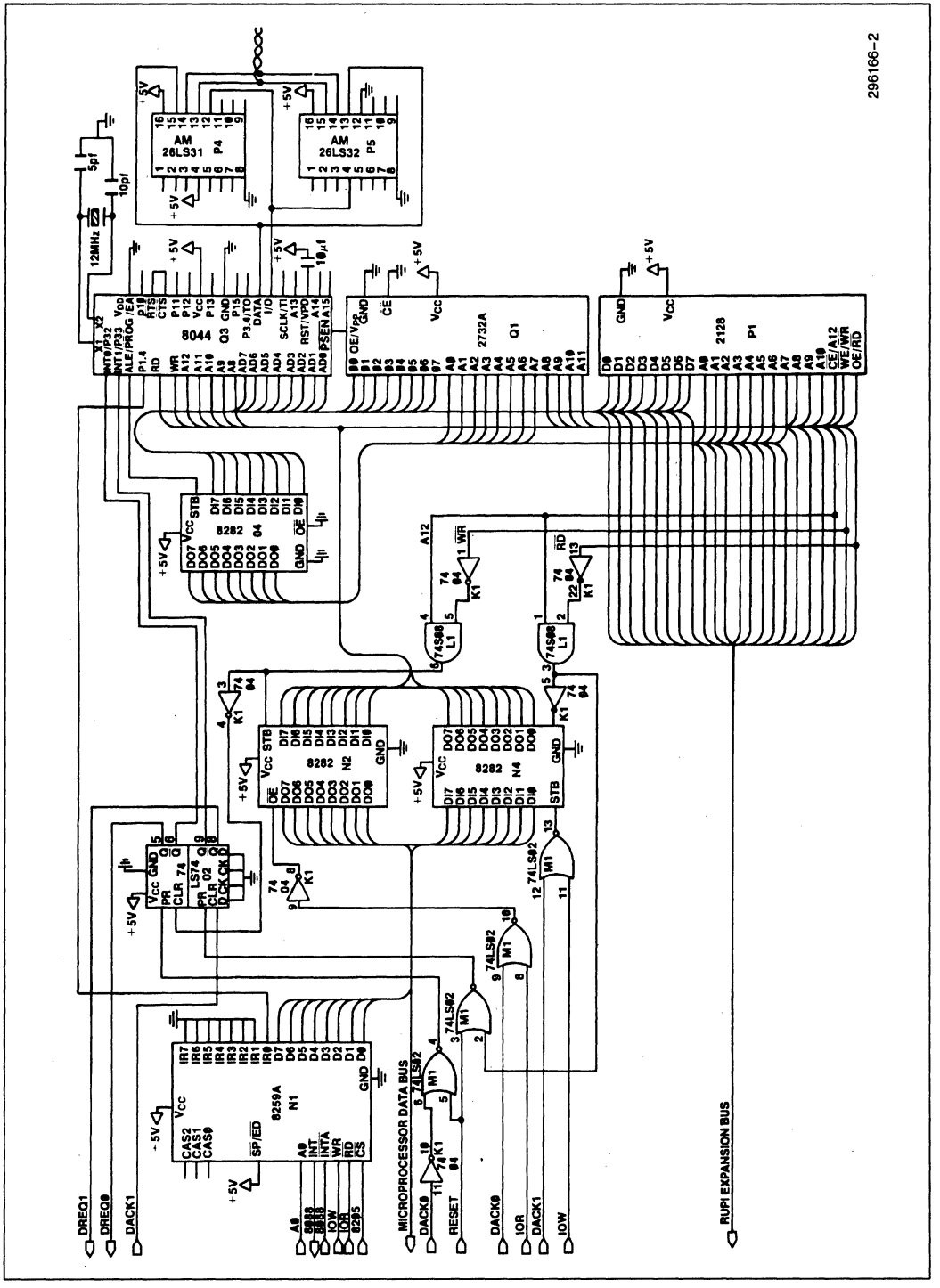

Figure 2. 8044 Interface to the 8088

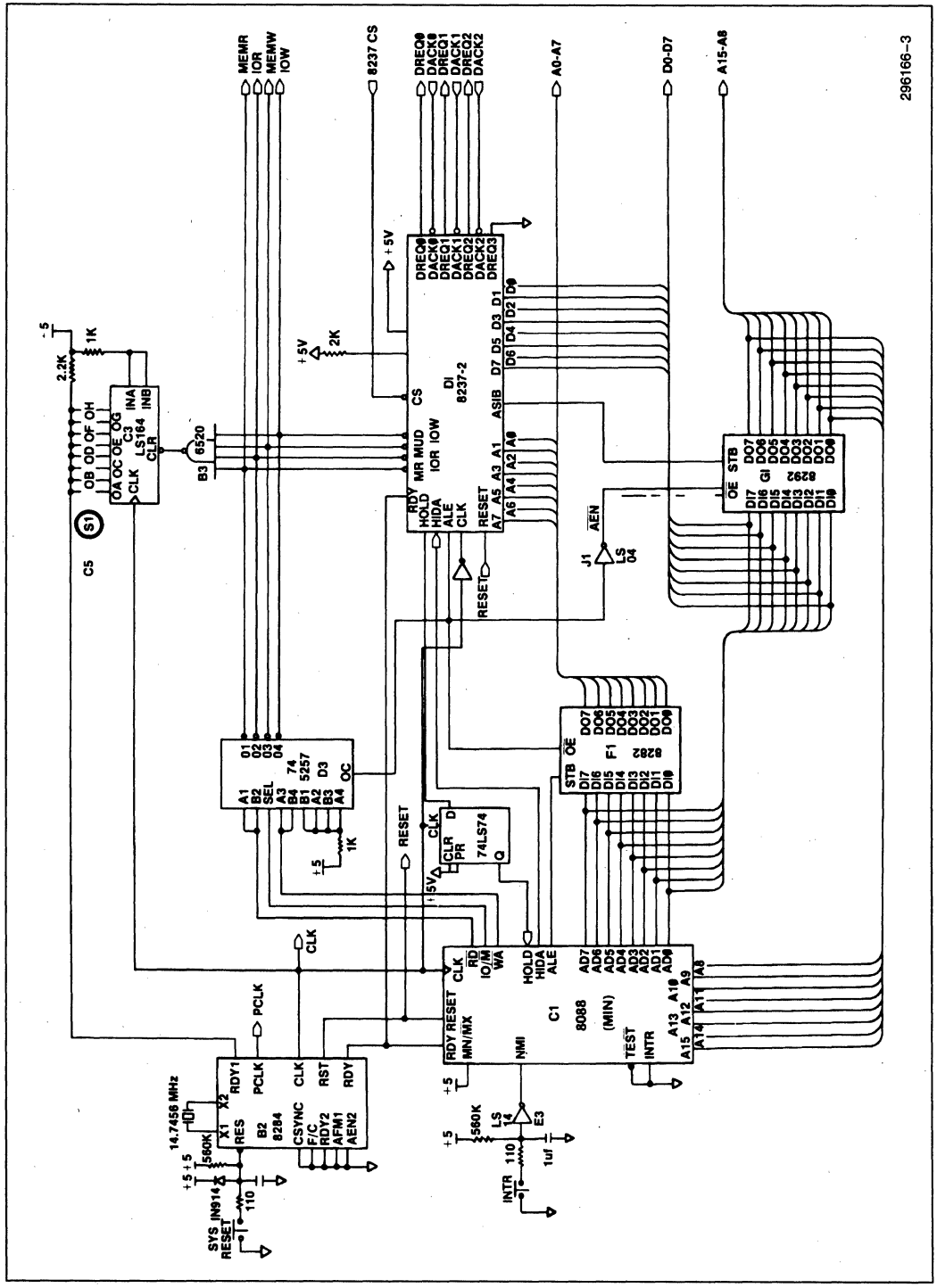

Figure 3. 8088 Min Mode System

Table 1. Transmit and Receive Software for an 8044/8088 System

```
LOC  OBJ    LINE     SOURCE

                1   $debug    title    (8044/8088 INTERFACE)
                2
                3
  0000          4   FIRST_BYTE       BIT      0       ; FLAG
                5
  0000          6            ORG      0
  0000 8024     7            SJMP     INIT
                8
  0026          9            ORG      26H
               10
  0026 7581AA  11   INIT:    MOV      SP, #170        ; INITIALIZE STACK
  0029 75B800  12            MOV      IP, #00         ; ALL INTERRUPTS ARE EQUAL PRIORITY
  002C 75C954  13            MOV      SMD, #54H       ; TIMER 1 OVERFLOW, NRZI, PRE-FRAME SYNC
  002F 758844  14            MOV      TCON, #44H      ; EDGE TRIGGERED EXTERNAL INTERRUPT 1
               15                                      ; LEVEL TRIGGERED EXTERNAL INTERRUPT 0
               16                                      ; TIMER 1 ON
  0032 758DEC  17            MOV      TH1, #0ECH      ; INITIALIZE TIMER, 3125 BPS
  0035 758920  18            MOV      TMOD, #20H      ; TIMER 1 AUTO RELOAD
               19
  0038 75DC6A  20            MOV      TBS, #106       ; SET UP SIU PARAMETER REGISTERS
  003B 75DB40  21            MOV      TBL, #64
  003E 75CC2A  22            MOV      RBS, #42
  0041 75CB40  23            MOV      RBL, #64
  0044 75CE55  24            MOV      STAD, #55H
  0047 75DA11  25            MOV      TCB, #00010001B ; RR, P/F=1
               26
  004A 901000  27            MOV      DPTR, #1000H    ; DPTR POINTS TO TRI-STATE LATCH
  004D D200    28            SETB     FIRST_BYTE      ; FLAG TO INDICATE FIRST BYTE
               29                                      ; FOR RECEIVE INTERRUPT ROUTINE
  004F D2CE    30            SETB     RBE             ; READY TO RECEIVE
  0051 75A894  31            MOV      IE, #10010100B  ; ENABLE RECEIVE DMA AND SIU INTERRUPT
               32
  0054 80FE    33            SJMP     $               ; WAIT HERE FOR INTERRUPTS
               34
  0056 80FE    35   ERROR:   SJMP     ERROR
               36 +1 $EJ
               37   ;*************************  SUBROUTINES  ********************************
               38
  0058 85CD29  39   SEND:    MOV      41, RFL         ; FIRST BYTE IN BLOCK IS COUNT
  005B 7929    40            MOV      R1, #41         ; POINT TO BLOCK OF DATA
  005D AACD    41            MOV      R2, RFL         ; LOAD COUNT
  005F 0A      42            INC      R2
  0060 D2A8    43            SETB     EX0             ; ENABLE DMA TRANSMIT INTERRUPT
  0062 22      44            RET
               45
               46
               47
               48   ;*******************  INTERRUPT SERVICE ROUTINES  **********************
               49
  0063         50   LOC_TMP  SET      $               ; SET UP INTERRUPT TABLE JUMP
  0013         51            ORG      0013H
  0013 020063  52            LJMP     RECEIVE_DMA
  0063         53            ORG      LOC_TMP
               54
               55   RECEIVE_DMA:
```

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Table 1. Transmit and Receive Software for an 8044/8088 System (Continued)

```
                    56
0063 10000E         57          JBC     FIRST_BYTE, L1 ; THE FIRST BYTE TRANSFERRED IS THE COUNT
                    58
0066 E0             59          MOVX    A, @DPTR       ; READ THE LATCH
0067 F6             60          MOV     @R0, A         ; PUT IT IN TRANSMIT BUFFER
0068 08             61          INC     R0
0069 DA08           62          DJNZ    R2, L2         ; AFTER READING BYTES,
                    63
006B D2CF           64          SETB    TBF            ; SEND DATA
006D D2CD           65          SETB    RTS
006F D200           66          SETB    FIRST_BYTE
0071 C2AA           67          CLR     EX1
                    68
0073 32             69  L2:     RETI
                    70
0074 786A           71  L1:     MOV     R0, #106       ; R0 IS A POINTER TO THE TRANSMIT
                    72                                 ; BUFFER STARTING ADDRESS
0076 E0             73          MOVX    A, @DPTR       ; PUT THE FIRST BYTE INTO
0077 FA             74          MOV     R2, A          ; R2 FOR THE COUNT
0078 32             75          RETI
                    76
  0079              77  LOC_TMP SET    $
0003                78          ORG     0003H
0003 020079         79          LJMP    TRANSMIT_DMA
0079                80          ORG     LOC_TMP
                    81
                    82  TRANSMIT_DMA
                    83
0079 E7             84          MOV     A, @R1         ; READ BYTE OUT OF THE RECEIVE BUFFER
007A F0             85          MOVX    @DPTR, A       ; WRITE IT TO THE LATCH
007B 09             86          INC     R1
007C DA08           87          DJNZ    R2, L3         ; WHEN ALL BYTES HAVE BEEN SENT
                    88
007E C2A8           89          CLR     IE. 0          ; DISABLE INTERRUPT
0080 C294           90          CLR     P1. 4          ; CAUSE 8088 INTERRUPT TO TERMINATE DMA
0082 D294           91          SETB    P1. 4
0084 D2CE           92          SETB    RBE            ; ENABLE RECEIVER AGAIN
                    93
0086 32             94  L3:     RETI
                    95
                    96
                    97
  0087              98  LOC_TMP SET    $
0023                99          ORG     0023H
0023 020087        100          LJMP    SERIAL_INT
0087               101          ORG     LOC_TMP
                   102
                   103  SERIAL_INT:
                   104
0087 30CE06        105          JNB     RBE, RCV       ; WAS A FRAME RECEIVED
008A 30CF0B        106          JNB     TBF, XMIT      ; WAS A FRAME TRANSMITTED
008D 020056        107          LJMP    ERROR          ; IF NEITHER ERROR
                   108
0090 20CBC3        109  RCV:    JB      BOV, ERROR     ; IF BUFFER OVERRUN THEN ERROR
0093 1158          110          CALL    SEND           ; SEND THE FRAME TO THE 8088
0095 C2CC          111          CLR     SI
0097 32            112          RETI
                   113
0098 C2CC          114  XMIT:   CLR     SI
```

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Table 1. Transmit and Receive Software for an 8044/8088 System (Continued)

```
009A D2AA       115             SETB    EX1
009C 32         116             RETI
                117
                118             END

SYMBOL TABLE LISTING

NAME                    TYPE    VALUE           ATTRIBUTES

BOV . . . . . B ADDR    00C8H.3 A
ERROR . . . . . C ADDR  0056H   A
EX0 . . . . . B ADDR    00A8H.0 A
EX1 . . . . . B ADDR    00A8H.2 A
FIRST_BYTE . . B ADDR   0020H.0 A
IE . . . . . D ADDR     00A8H   A
INIT . . . . . C ADDR   0026H   A
IP . . . . . D ADDR     00B8H   A
L1 . . . . . C ADDR     0074H   A
L2 . . . . . C ADDR     0073H   A
L3 . . . . . C ADDR     0086H   A
LOC_TMP . . . C ADDR    0087H   A
P1 . . . . . D ADDR     0090H   A
RBE . . . . . B ADDR    00C8H.6 A
RBL . . . . . D ADDR    00CBH   A
RBS . . . . . D ADDR    00CCH   A
RCV . . . . . C ADDR    0090H   A
RECEIVE_DMA . C ADDR    0063H   A
RFL . . . . . D ADDR    00CDH   A
RTS . . . . . B ADDR    00C8H.5 A
SEND . . . . . C ADDR   0058H   A
SERIAL_INT . . C ADDR   0087H   A
SI . . . . . B ADDR     00C8H.4 A
SMD . . . . . D ADDR    00C9H   A
SP . . . . . D ADDR     0081H   A
STAD . . . . . D ADDR   00CEH   A
TBF . . . . . B ADDR    00C8H.7 A
TBL . . . . . D ADDR    00DBH   A
TBS . . . . . D ADDR    00DCH   A
TCB . . . . . D ADDR    00DAH   A
TCON . . . . . D ADDR   0088H   A
TH1 . . . . . D ADDR    008DH   A
TMOD . . . . . D ADDR   0089H   A
TRANSMIT_DMA . C ADDR   0079H   A
XMIT . . . . . C ADDR   0098H   A

REGISTER BANK(S) USED: 0, TARGET MACHINE(S): 8044

ASSEMBLY COMPLETE, NO ERRORS FOUND
```

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Table 2. PL/M-86 Compiler RUPI/8088 Interface Example

```
SERIES-III PL/M-86 V1.0 COMPILATION OF MODULE RUPI_88
OBJECT MODULE PLACED IN :F1:R88.OBJ
COMPILER INVOKED BY:  PLM86.86 :F1:R88.SRC


            $DEBUG
            $TITLE  ('RUPI/8088 INTERFACE EXAMPLE')

  1         RUPI_88: DO;

  2  1          DECLARE

                LIT                 LITERALLY   'LITERALLY',
                TRUE                LIT         '01H',
                FALSE               LIT         '00H',

                RECV_BUFFER(64)     BYTE,
                XMIT_BUFFER(64)     BYTE,
                I                   BYTE,
                WAIT                BYTE,

                                /* 8237 PORTS*/

                MASTER_CLEAR_37     LIT         'OFFDDH',
                COMMAND_37          LIT         'OFFD8H',
                ALL_MASK_37         LIT         'OFFDFH',
                SINGLE_MASK_37      LIT         'OFFDAH',
                STATUS_37           LIT         'OFFD8H',
                REQUEST_REG_37      LIT         'OFFD9H',
                MODE_REG_37         LIT         'OFFDBH',
                CLEAR_BYTE_PTR_37   LIT         'OFFDCH',

                CH0_ADDR            LIT         'OFFD0H',
                CH0_COUNT           LIT         'OFFD1H',
                CH1_ADDR            LIT         'OFFD2H',
                CH1_COUNT           LIT         'OFFD3H',
                CH2_ADDR            LIT         'OFFD4H',
                CH2_COUNT           LIT         'OFFD5H',
                CH3_ADDR            LIT         'OFFD6H',
                CH3_COUNT           LIT         'OFFD7H',

                        /* 8237 BIT ASSIGNMENTS */

                CH0_SEL             LIT         '00H',
                CH1_SEL             LIT         '01H',
                CH2_SEL             LIT         '02H',
                CH3_SEL             LIT         '03H',
                WRITE_XFER          LIT         '04H',
                READ_XFER           LIT         '08H',
                DEMAND_MODE         LIT         '00H',
                SINGLE_MODE         LIT         '40H',
                BLOCK_MODE          LIT         '80H',
                SET_MASK            LIT         '04H',

            $EJECT
                            /* 8259 PORTS */

               STATUS_POLL_59       LIT        'OFFE0H',
               ICW1_59              LIT        'OFFE0H',
               OCW1_59              LIT        'OFFE1H',
               OCW2_59              LIT        'OFFE0H',
               OCW3_59              LIT        'OFFE0H',
               ICW2_59              LIT        'OFFE1H',
               ICW3_59              LIT        'OFFE1H',
               ICW4_59              LIT        'OFFE1H';

                        /* INTERRUPT SERVICE ROUTINE */

  3  1       OFF_RECV_DMA:    PROCEDURE    INTERRUPT 32;

  4  2           OUTPUT(SINGLE_MASK_37)=40H;
  5  2           WAIT=FALSE;
  6  2           END;
```

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Table 2. PL/M-86 Compiler RUPI/8088 Interface Example (Continued)

```
 7   1          DISABLE;

                        /* INITIALIZE 8237 */

 8   1          OUTPUT(MASTER_CLEAR_37)      =0;
 9   1          OUTPUT(COMMAND_37)           =040H;
10   1          OUTPUT(ALL_MASK_37)          =0FH;
11   1          OUTPUT(MODE_REG_37)          =(SINGLE_MODE OR WRITE_XFER OR CH0_SEL);
12   1          OUTPUT(MODE_REG_37)          =(SINGLE_MODE OR READ_XFER OR CH1_SEL);
13   1          OUTPUT(CLEAR_BYTE_PTR_37)    =0;
14   1          OUTPUT(CH0_ADDR)             =00H;
15   1          OUTPUT(CH0_ADDR)             =40H;
16   1          OUTPUT(CH0_COUNT)            =64;
17   1          OUTPUT(CH0_COUNT)            =00;
18   1          OUTPUT(CH1_ADDR)             =40H;
19   1          OUTPUT(CH1_ADDR)             =40H;
20   1          OUTPUT(CH1_COUNT)            =64;
21   1          OUTPUT(CH1_COUNT)            =00;

                        /* INITIALIZE 8259 */

22   1          OUTPUT(ICW1_59)              =13H; /*SINGLE MODE, EDGE TRIGGERED
                                                    INPUT, 8086 INTERRUPT TYPE*/
23   1          OUTPUT(ICW2_59)              =20H; /*INTERRUPT TYPE 32*/
24   1          OUTPUT(ICW4_59)              =03H; /*AUTO-EOI*/
25   1          OUTPUT(OCW1_59)              =0FEH; /*ENABLE INTERRUPT LEVEL 0*/

          $EJECT
26   1          CALL SET$INTERRUPT  (32,OFF_RECV_DMA); /*LOAD INTERRUPT VECTOR LOCATION*/

27   1          XMIT_BUFFER(0)=64; /*THE FIRST BYTE IN THE BLOCK OF DATA IS THE NUMBER
                                      OF BYTES TO BE TRANSFERED; NOT INCLUDING THE FIRST BYTE*/

28   1          DO  I= 1 TO 64;  /* FILL UP THE XMIT_BUFFER WITH DATA */
29   2          XMIT_BUFFER(I)=I;
30   2          END;

31   1          OUTPUT(ALL_MASK_37)=0FCH;    /*ENABLE CHANNEL 1 AND 2 */

32   1          ENABLE;

33   1          WAIT=TRUE;
34   1          DO WHILE WAIT;
35   2          END;                    /* A BLOCK OF DATA WILL BE TRANSFERRED TO THE RUPI.
                                           WHEN THE RUPI RECEIVES A BLOCK OF DATA IT WILL
                                           SEND IT TO THE 8088 MEMORY AND INTERRUPT THE 8088.
                                           THE INTERRUPT SERVICE ROUTINE WILL SHUT OFF THE DMA
                                           CONTROLLER AND SET 'WAIT' FALSE */

36   1          DO WHILE 1;
37   2          END;


38   1      END;



MODULE INFORMATION:

     CODE AREA SIZE     = 00D7H    215D
     CONSTANT AREA SIZE = 0000H      0D
     VARIABLE AREA SIZE = 0082H    130D
     MAXIMUM STACK SIZE = 001EH     30D
     124 LINES READ
     0 PROGRAM WARNINGS
     0 PROGRAM ERRORS

END OF PL/M-86 COMPILATION
```

296166-5

12

A HIGH PERFORMANCE NETWORK USING THE 8044

2.0 INTRODUCTION

This section describes the design of an SDLC data link using the 8044 (RUPI) to implement a primary station and a secondary station. The design was implemented and tested. The following discussion assumes that the reader understands the 8044 and SDLC. This section is divided into two parts. First the data link design example is discussed. Second the software modules used to implement the data link are described. To help the reader understand the discussion of the software, flow charts and software listings are displayed in Appendix A and Appendix B, respectively.

APPLICATION DESCRIPTION

This particular data link design example uses a two wire half-duplex multidrop topology as shown in Figure 4. In an SDLC multidrop topology the primary station communicates with each secondary station. The secondary stations communicate only to the primary. Because of this hierarchial architecture, the logical topology for an SDLC multidrop is a star as shown in Figure 5. Although the physical topology of this data link is multidrop, the easiest way to understand the information flow is to think of the logical (star) topology. The term data link in this case refers to the logical communication pathways between the primary station and the secondary stations. The data links are shown in Figure 5 as two way arrows.

The application example uses dumb async terminals to interface to the SDLC network. Each secondary station has an async terminal connected to it. The secondary stations are in effect protocol converters which allows any async terminal to communicate with any other async terminal on the network. The secondary stations use an 8044 with a UART to convert SDLC to async. Figure 6 displays a block diagram of the data link. The primary station, controls the data link. In addition to data link control the primary provides a higher level layer which is a path control function or networking layer. The primary serves as a message exchange or switch. It receives information from one secondary station and retransmits it to another secondary station. Thus a virtual end to end connection is made between any two secondary stations on the network.

Three separate software modules were written for this network. The first module is a Secondary Station Driver (SSD) which provides an SDLC data link interface and a user interface. This module is a general purpose driver which requires application software to run it. The user interface to the driver provides four functions: OPEN, CLOSE, TRANSMIT, and SIU_RECV. Using these four functions properly will allow any application software to communicate over this SDLC data link without knowing the details of SDLC. The secondary station driver uses the 8044's AUTO mode.

The second module is an example of application software which is linked to the secondary station driver. This module drives the 8215A, buffers data, and interfaces with the secondary station driver's user interface.

The third module is a primary station, which is a standalone program (i.e., it is not linked to any other module). The primary station uses the 8044's NON-AUTO or FLEXIBLE mode. In addition to controlling the data link it acts as a message switch. Each time a secondary station transmits a frame, it places the destination address of the frame in the first byte of the information or I field. When the primary station receives a frame, it removes the first byte in the I field and retransmits the frame to the secondary station whose address matches this byte.

This network provides two complete layers of the OSI (Open Systems Interconnection) reference model: the physical layer and the data link layer. The physical layer implementation uses the RS-422 electrical interface. The mechanical medium consists of ribbon cable and connectors. The data link layer is defined by SDLC. SDLC's use of acknowledgements and frame numbering guarantees that messages will be received in the same order in which they were sent. It also guarantees message integrity over the data link. However this network will not guarantee secondary to secondary message delivery, since there are acknowledgements between secondary stations.

2.1 Hardware

The schematic of the hardware is given in Figure 7. The 8251A is used as an async communications controller, in support of the 8044. TxRDY and RxRDY on the 8251A are both tied to the two available external interrupts of the 8044 since the secondary station driver is totally interrupt driven. The 8044 buffers the data and some variables in a 2016 (2K x 8 static RAM). The 8254 programmable interval timer is employed as a programmable baud rate generator and system clock driver for the 8251A. The third output from the 8254 could be used as an external baud rate generator for the 8044. The 2732A shown in the diagram was not used

since the software for both the primary and secondary stations used far less than the 4K bytes provided on the 8744. For the async interface, the standard RS-232 mechanical and electrical interface was used. For the SDLC channel, a standard two wire three state RS-422 driver is used. A DIP switch connected to one of the available ports on the 8044 allows the baud rate, parity, and stop bits to be changed on the async interface. The primary station hardware does not use the USART, 8254, nor the RS-232 drivers.

2.2 SDLC Basic Repertoire

The SDLC commands and responses implemented in the data link include the SDLC Basic Repertoire as defined in the IBM SDLC General Information manual. Table 3 shows the commands and responses that the primary and the secondary station in this data link design recognize and send.

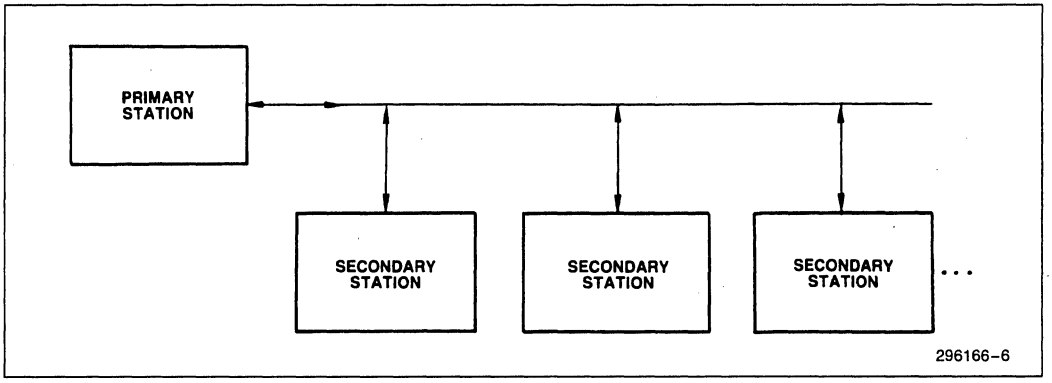


Figure 4. SDLC Multidrop Topology

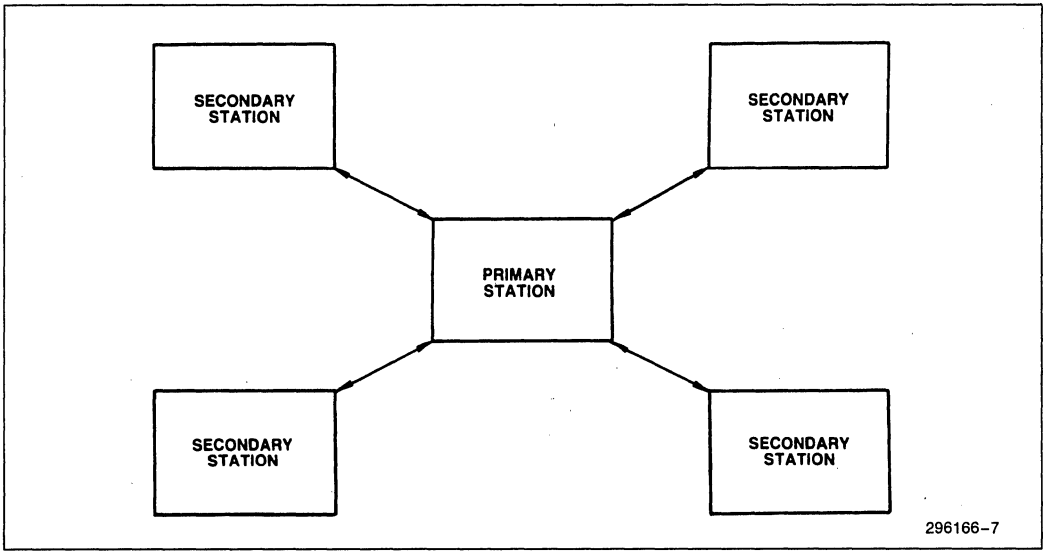


Figure 5. SDLC Logical Topology

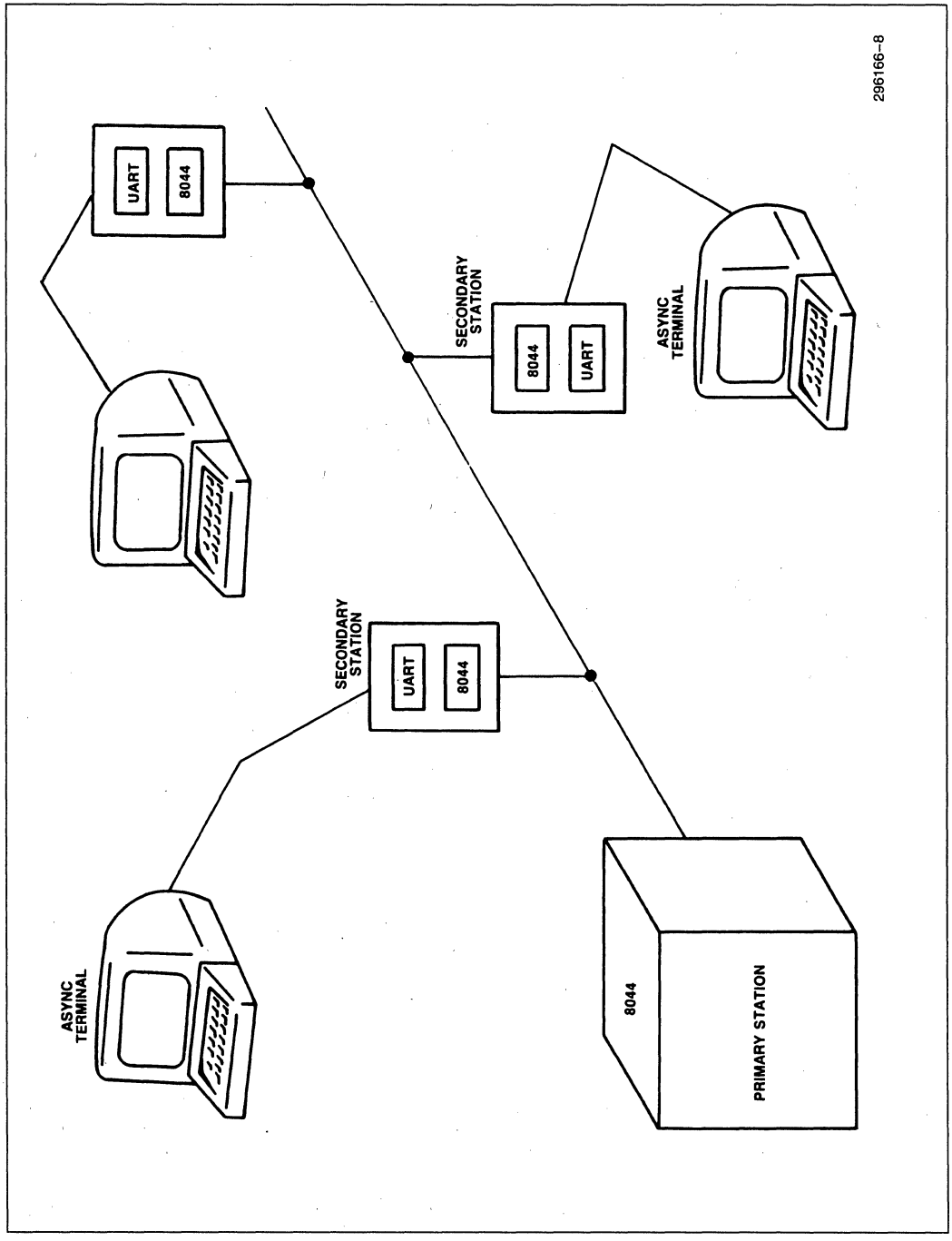


Figure 6. Block Diagram of the Data Link Application Example

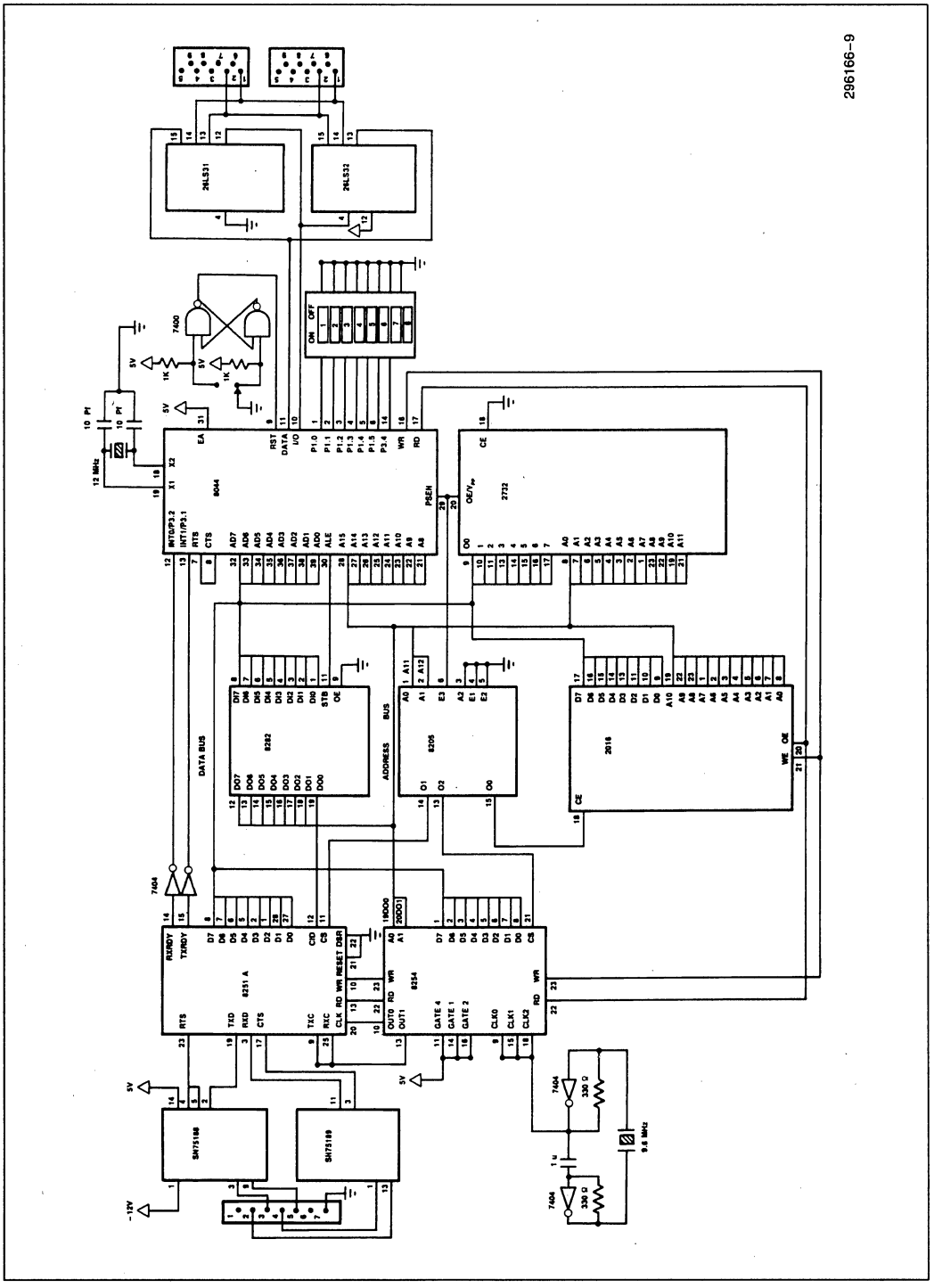


Figure 7. Schematic of Async/SDLC Secondary Station Protocol Converter

Table 3. Data Link Commands and Responses Implemented for This Design

Primary Station

	Responses Recognized	Commands Sent
Unnumbered	UA DM FRMR *RD	SNRM DISC
Supervisory	RR RNR	RR RNR
Information	I	I

Secondary Station

	Commands Recognized	Responses Sent
Unnumbered	SNRM DISC *TEST	UA DM FRMR *RD *TEST
Supervisory	RR RNR REJ	RR RNR
Information	I	I

*not included in the SDLC Basic Repertoire

The term command specifically means all frames which the primary station transmits and the secondary stations receive. Response refers to frames which the secondary stations transmit and the primary station receives.

NUMBER OF OUTSTANDING FRAMES

This particular data link design only allows one outstanding frame before it must receive an acknowledgement. Immediate acknowledgement allows the secondary station drivers to use the AUTO mode. In addition, one outstanding frame uses less memory for buffering, and the software becomes easier to manage.

2.3 Secondary Station Driver using AUTO Mode

The 8044 secondary station driver (SSD) was written as a general purpose SDLC driver. It was written to be linked to an application module. The application software implements the actual application in addition to interfacing to the SSD. The main application could be, a printer or plotter, a medical instrument, or a terminal. The SSD is independent of the main application, it just provides the SDLC communications. Existing 8051 applications could add high performance SDLC communications capability by linking the SSD to the existing software and providing additional software to be able to communicate with the SSD.

DATA LINK INTERFACE AND USER INTERFACE STATES

The SSD has two software interfaces: a data link interface and a user interface as shown in Figure 8. The data link interface is the part of the software which controls the SDLC communications. It handles link access, command recognition/response, acknowledgements, and error recovery. The user interface provides four functions: OPEN, CLOSE, TRANSMIT, and SIU__ RECV. These are the only four functions which the application software has to interface in order to communicate using SDLC. These four functions are common to many I/O drivers like floppy and hard disks, keyboard/CRT, and async communication drivers.

The data link and the user interface each have their own states. Each interface can only be in one state at any time. The SSD uses the states of these two interfaces to help synchronize the application module to the data link.

There are three states which the secondary station data link interface can be in: Logical Disconnect State (L__D__S), Frame Reject State (FRMR__S), and the Information Transfer State (I__T__S). The Logical Disconnect State is when a station is physically connected to the channel but either the primary or secondary have not agreed to enter the Information Transfer State. Both the primary and the secondary stations synchronize to enter into the Information Transfer State. Only when the secondary station is in the I__T__S is it able to transfer data or information to the primary. The Frame Reject State (FRMR__S) indicates that the secondary station has lost software synchronization with the primary or encountered some kind of error condition. When the secondary station is in the FRMR__S, the primary station must reset the secondary to resynchronize.

The user interface has two states, open or closed. In the closed state, the user program does not want to communicate over the network. The communications channel is closed and not available for use. The secondary station tells the primary this by responding to all commands with DM. The primary continues to poll the secondary in case it wants to enter the I__T__S state. When the user program begins communication over the data link it goes into the open state. It does this by calling the OPEN procedure. When the user interface is in the open state it may transfer information to the primary.

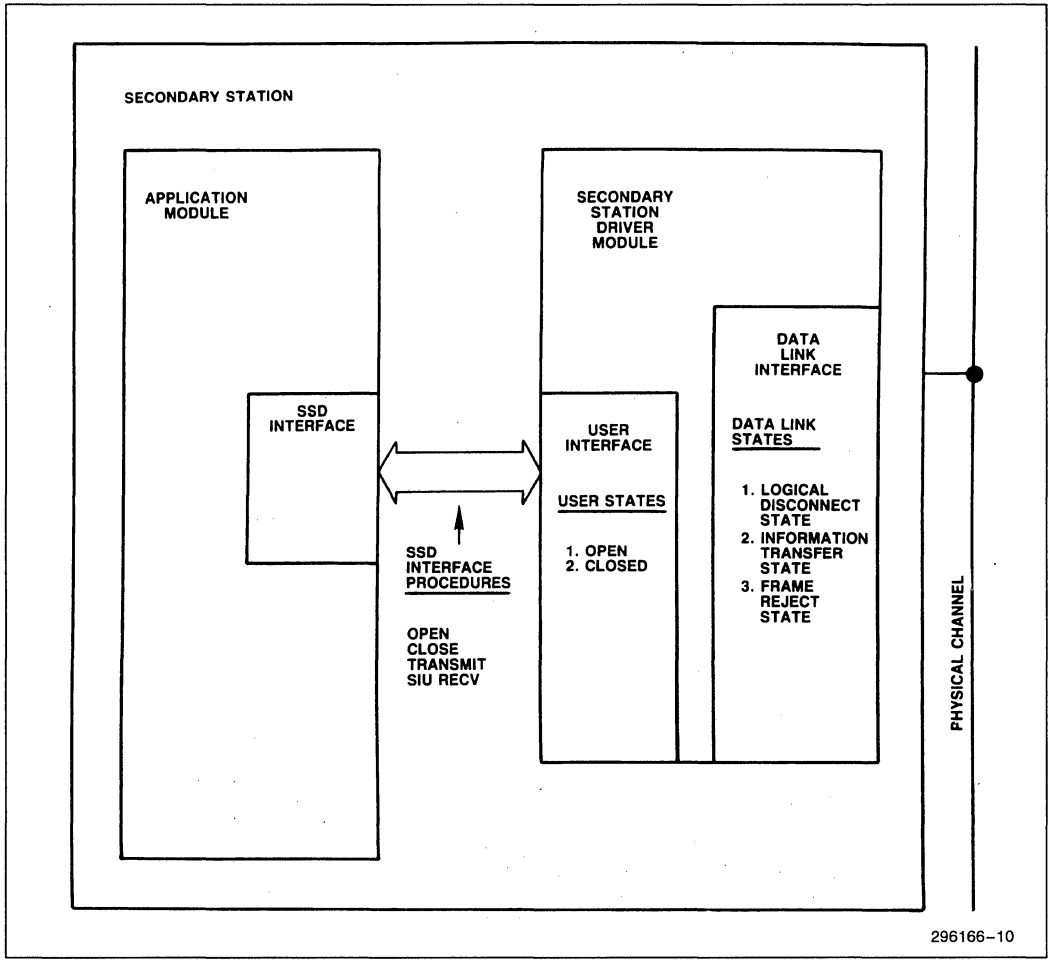


Figure 8. Secondary Station Software Modules

SECONDARY STATION COMMANDS, RESPONSES AND STATE TRANSITIONS

Table 4 shows the commands which the secondary station recognizes and the responses it generates. The first row in Table 4 displays commands the secondary station recognizes and each column shows the potential responses with respect to secondary station. For example, if the secondary is in the Logical Disconnect State it will only respond with DM, unless it receives a SNRM command and the user state is open. If this is the case, then the response will be UA and the secondary station will move into the I_T_S.

Figure 9 shows the state diagram of the secondary station. When power is first applied to the secondary station, it goes into the Logical Disconnect State. As mentioned above, the I_T_S is entered when the secondary station receives a SNRM command and the user state is open. The secondary responds with UA to let the primary know that it has accepted the SNRM and is entering the I_T_S. The I_T_S can go into either the L_D_S or the FRMR_S. The I_T_S goes into the L_D_S if the primary sends the secondary DISC. The secondary has to respond with UA, and then goes into the L_D_S. If the user interface changes from open to close state, then the secondary sends RD. This causes the primary to send a DISC.

The FRMR_S is entered when a secondary station is in the I_T_S and either one of the following conditions occurs.

— A command can not be recognized by the secondary station.
— There is a buffer overrun.
— The Nr that was received from the primary station is invalid.

The secondary station cannot leave the FRMR_S until it receives a SNRM or a DISC command.

SOFTWARE DESCRIPTION OF THE SSD

To aid in following the description of the software, the reader may either look at the flow charts which are given for each procedure, or read the PL/M-51 listing provided in Appendix A.

A block diagram of the software structure of the SSD is given in Figure 10. A complete module is identified by the dotted box, and a procedure is identified by the solid box. Therefore the SIU_RECV procedure is not included in the SSD module, it exists in the application software. Two or more procedures connected by a solid line means the procedure above calls the procedure below. Transmit, Power_on_D, Close, and Open are all called by the application software. Procedures without any solid lines connected above are interrupt procedures. The only interrupt procedure in the SSD module is the SIU_INT.

The entire SSD module is interrupt driven. Its design allows the application program to handle real time events or just dedicate more CPU time to the application program. The SIU_INT is the only interrupt procedure in the SSD. It is automatically entered when an SIU interrupt occurs. This particular interrupt can be the lowest priority interrupt in the system.

Table 4. Secondary Station Responses to Primary Station Commands

Data Link States	Primary Station-Commands					
	I	RR	RNR	SNRM	DISC	TEST
Information Transfer State	I RR RNR RD FRMR	I RR RNR RD FRMR	I RR RNR RD FRMR	RD UA	UA	RD Test
Logical Disconnect State	DM	DM	DM	DM UA	DM	DM
Frame Reject State	FRMR	FRMR	FRMR	UA	UA	FRMR

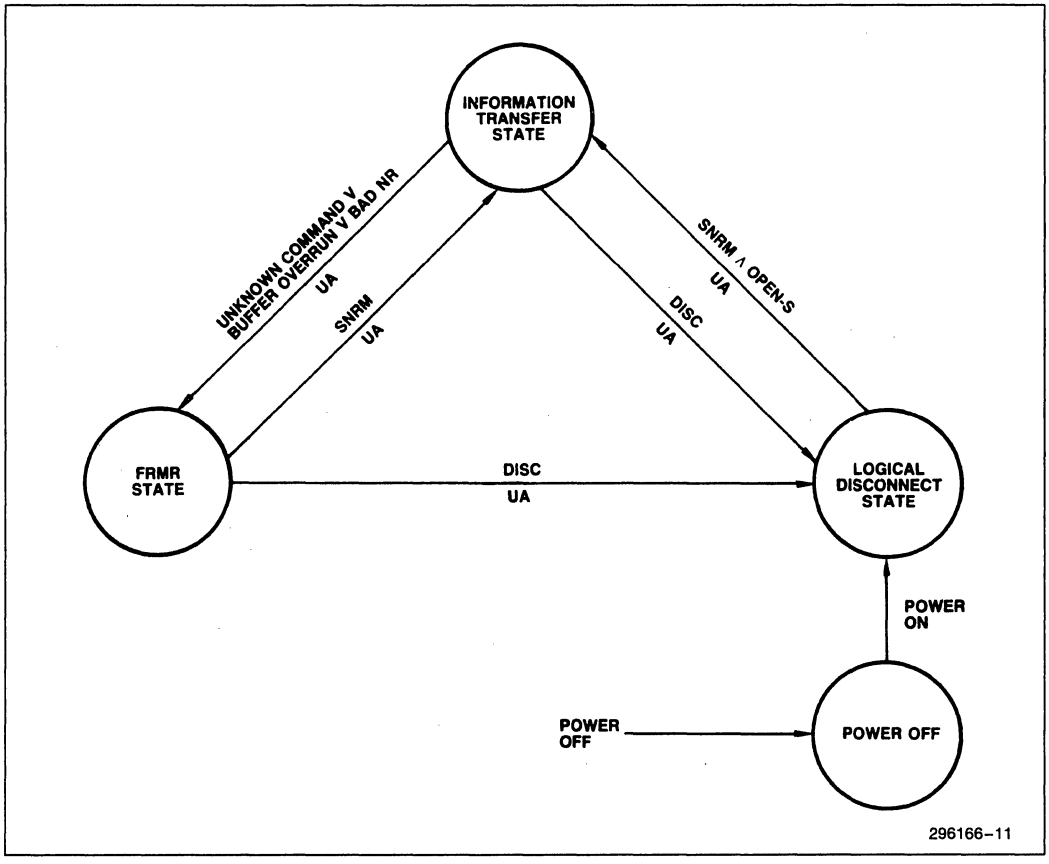


Figure 9. State Diagram of Secondary Station

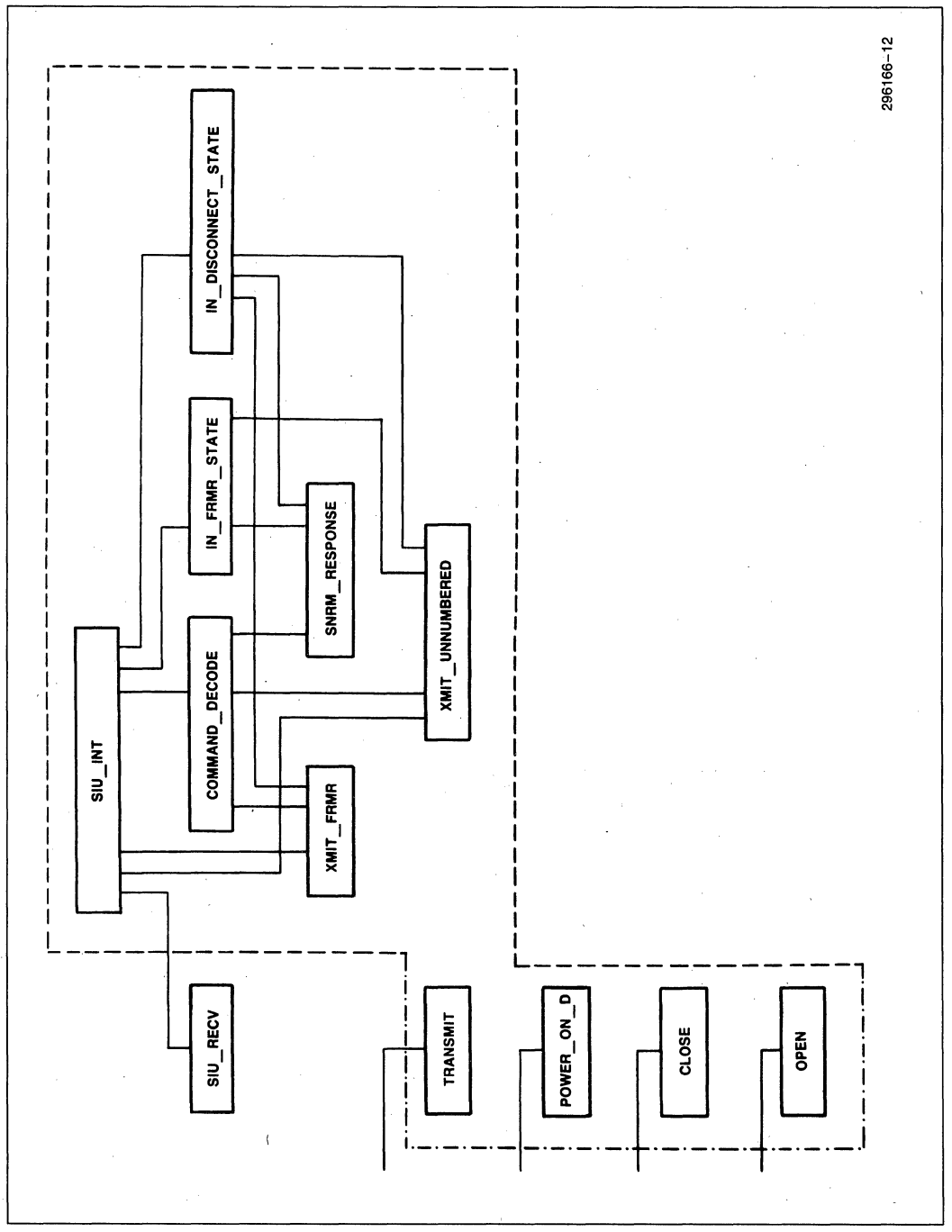


Figure 10. Secondary Station Driver

SSD INITIALIZATION

Upon reset the application software is entered first. The application software initializes its own variables then calls Power_On_D which is the SSD's initialization routine. The SSD's initialization sets up the transmit and receive data buffer pointers (TBS and RBS), the receive buffer length (RBL), and loads the State variables. The STATION_STATE begins in the L_D_S state, and the USER_STATE begins in the closed state. Finally Power_On_D initializes XMIT_BUFFER_EMPTY which is a bit flag. This flag serves as a semaphore between the SSD and the application software to indicate the status of the on chip transmit buffer. The SSD does not set the station address. It is the application software's responsibility to do this. After initialization, the SSD is read to respond to all of the primary station commands. Each time a frame is received with a matching station address and a good CRC, the SIU_INT procedure is entered.

SIU_INT PROCEDURE

The first thing the SIU_INT procedure clears is the serial interrupt_bit (SI) in the STS register. If the SIU_INT procedure returns with this bit set, another SI interrupt will occur.

The SIU_INT procedure is branches three independent cases. The first case is entered if the STATION_STATE is not in the I_T_S. If this is true, then the SIU is not in the AUTO mode, and the CPU will have to respond to the primary on its own. (Remember that the AUTO mode is entered when the STATION_STATE enters into I_T_S.) If the STATION_STATE is in the I_T_S, then either the SIU has just left the AUTO mode, or is still in the AUTO mode. This is the second and third case, respectively.

In the first case, if the STATION_STATE is not in the I_T_S, then it must be in either the L_D_S or the FRMR_S. In either case a separate procedure is called based on which state the station is in. The In_Disconnect_State procedure sends to the primary a DM response, unless it received a SNRM command and the USER_STATE equals open. In that case the SIU sends a UA and enters into the I_T_S. The In_FRMR_State procedure will send the primary the FRMR response unless it received either a DISC or an SNRM. If the primary's command was a DISC, then the secondary will send a UA and enter into the L_D_S. If the primary's command was a SNRM, then the secondary will send a UA, enter into the I_T_S, and clear NSNR register.

For the second case, if the STATION_STATE is in the I_T_S but the SIU left the AUTO mode, then the CPU must determine why the AUTO mode was exited, and generate a response to the primary. There are four reasons for the SIU to automatically leave the AUTO mode. The following is a list of these reasons, and the responses given by the SSD based on each reason.

1. The SIU has received a command field it does not recognize.

   Response: If the CPU recognizes the command, it generates the appropriate response. If neither the SIU nor the CPU recognize the command, then a FRMR response is sent.

2. The SIU has received a Sequence Error Sent (SES = 1 in NSNR register). Nr(P)≠Ns(S)+1, and Nr(P)≠Ns(S).

   Response: Send FRMR.

3. A buffer overrun has occurred. BOV = 1 in STS register.

   Response: Send FRMR.

4. An I frame with data was received while RPB = 1.

   Response: Go back into AUTO mode and send an AUTO mode response

In addition to the above reasons, there is one condition where the CPU forces the SIU out of the AUTO mode. This is discussed in the SSD's User Interface Procedures section in the CLOSED procedure description

Finally, case three is when the STATION_STATE is in the I_T_S and the AUTO mode. The CPU first looks at the TBF bit. If this bit is 0 then the interrupt may have been caused by a frame which was transmitted and acknowledged. Therefore the XMIT_BUFFER_EMPTY flag is set again, indicating that the application software can transmit another frame.

The other reason this section of code could be entered is if a valid I frame was received. When a good I frame is received the RBE bit equals 0. This means that the receiver is disabled. If the primary were to poll the 8044 while RBE = 0, it would time out since no response would be given. Time outs reduce network throughput. To improve network performance, the CPU first sets RBP, then sets RBE. Now when the primary polls the 8044 an immediate RNR response is given. At this point the SSD calls the application software procedure SIU_RECV and passes the length of the data as a parameter. The SIU_RECV procedure reads the data out of the receive buffer then returns to the SSD module. Now that the receive information has been transferred, RBP can be cleared.

COMMAND_DECODE PROCEDURE

The Command_Decode procedure is called from the SIU_INT procedure when the STATION_STATE = I_T_S and the SIU left the AUTO mode as a result of not being able to recognize the receive control byte. Commands which the SIU AUTO mode does not

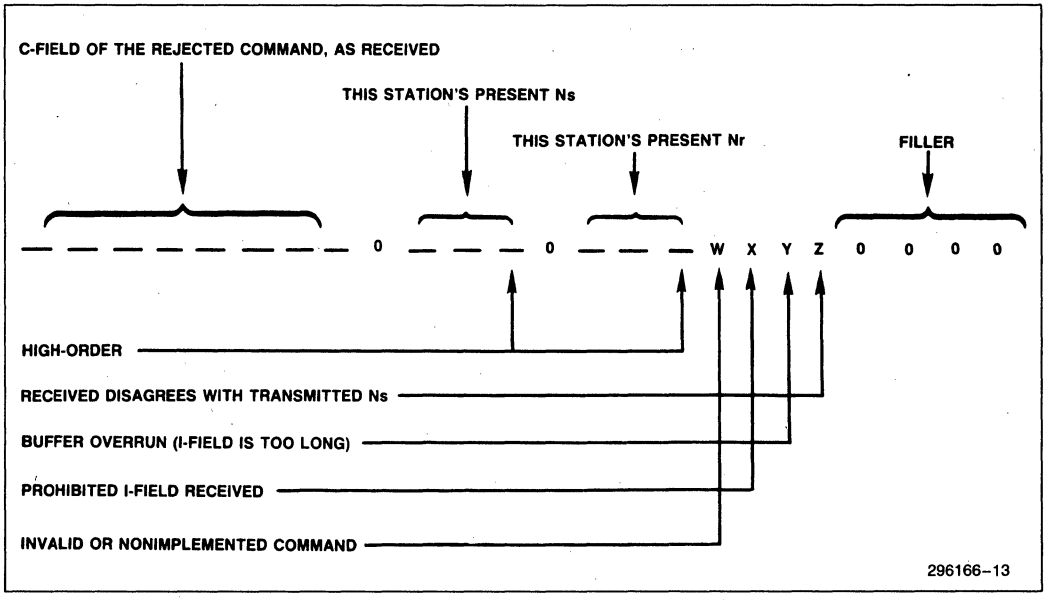


Figure 11. Information Field of the FRMR Response, as Transmitted

recognize are handled here. The commands recognized in this procedure are: SNRM, DISC, and TEST. Any other command received will generate a Frame Reject with the nonimplemented command bit set in the third data byte of the FRMR frame. Any additional unnumbered frame commands which the secondary station is going to implement, should be implemented in this procedure.

IF an SNRM is received the command_decode procedure calls the SNRM_Response procedure. The SNRM_Response procedure sets the STATION_STATE = I_T_S, clears the NSNR register and responds with a UA frame. If a DISC is received, the command_decode procedure sets the STATION_STATE = L_D_S, and responds with a UA frame. When a TEST frame is received, and there is no buffer overrun, the command_decode procedure responds with a TEST frame retransmitting the same data it received. However if a TEST frame is received and there is a buffer overrun, then a TEST frame will be sent without any data, instead of a FRMR with the buffer overrun bit set.

FRAME REJECT PROCEDURES

There are two procedures which handle the FRMR state: XMIT_FRMR and IN_FRMR_STATE. XMIT_FRMR is entered when the secondary station first goes into the FRMR state. The frame reject response frame contains the FRMR response in the command field plus three additional data bytes in the I field. Figure 11 displays the format for the three data bytes in the I field of a FRMR response. The XMIT_FRMR procedure sets up the Frame Reject response frame based on the parameter REASON which is passed to it. Each place in the SSD code that calls the XMIT_FRMR procedure, passes the REASON that this procedure was called, which in turn is communicated to the primary station. The XMIT_FRMR procedure uses three bytes of internal RAM which it initializes for the correct response. The TBS and TBL registers are then changed to point to the FRMR buffer so that when a response is sent these three bytes will be included in the I field.

The IN_FRMR_STATE procedure is called by the SIU_INT procedure when the STATION_STATE already is in the FRMR state and a response is required. The IN_FRMR_STATE procedure will only allow two commands to remove the secondary station from the FRMR state: SNRM and DISC. Any other command which is received while in the FRMR state will result in a FRMR response frame.

XMIT_UNNUMBERED PROCEDURE

This is a general purpose transmit procedure, used only in the FLEXIBLE mode, which sends unnumbered responses to the primary. It accepts the control byte as a parameter, and also expects the TBL register to be set before the procedure is called. This procedure waits until the frame has been transmitted before returning. If

this procedure returned before the transmit interrupt was generated, the SIU_INT routine would be entered. The SIU_INT routine would not be able to distinguish this condition.

SSD's User Interface Procedures—OPEN, CLOSE, TRANSMIT, SIU_RECV—are discussed in the following section.

The OPEN procedure is the simplest of all, it changes the USER_STATE to OPEN_S then returns. This lets the SSD know that the user wants to open the channel for communications. When the SSD receives a SNRM command, it checks the USER_STATE. If the USER_STATE is open, then the SSD will respond with a UA, and the STATION_STATE enters the I_T_S.

The CLOSE procedure is also simple, it changes the USER_STATE to CLOSED_S and sets the AM bit to 0. Note that when the CPU sets the AM bit to 0 it puts the SIU out of the AUTO mode. This event is asynchronous to the events on the network. As a result an I frame can be lost. This is what can happen.

1. AM is set to 0 by the CLOSE Procedure.
2. An I frame is received and an SI interrupt occurs.
3. The SIU_INT procedure enters case 2 (STATION_STATE = I_T_S, and AM = 0).
4. Case 2 detects that the USER_STATE = CLOSED_S, sends an RD response and ignores the fact that an I frame was received.

Therefore it is advised to never call the CLOSE procedure or take the SIU out of the AUTO mode when it is receiving I frames or an I frame will be lost.

For both the TRANSMIT and SIU_RECV procedures, it is the application software's job to put data into the transmit buffer, and take data out of the receive buffer. The SSD does not transfer data in or out of its transmit or receive buffers because it does not know what kind of buffering the application software is implementing. What the SSD does do is notify the application software when the transmit buffer is empty, XMIT_BUFFER_EMPTY = 1, and when the receive buffer is full.

One of the functions that the SSD performs to synchronize the application software to the SDLC data link. However some of the synchronization must also be done by the application software. Remember that the SSD does not want to hang up the application software waiting for some event to occur on the SDLC data link, therefore the SSD always returns to the application software as soon as possible.

For example, when the application software calls the OPEN procedure, the SSD returns immediately. The application software thinks that the SDLC channel is now open and it can transmit. This is not the case. For the channel to be open, the SSD must receive an SNRM from the primary and respond with a UA. However, the SSD does not want to hang up the application software waiting for an SNRM from the primary before returning from the OPEN procedure. When the TRANSMIT procedure is called, the SSD expects the STATION_STATE to be in the I_T_S. If it isn't, the SSD refuses to transmit the data. The TRANSMIT procedure first checks to see if the USER_STATE is open. If not, the USER_STATE_CLOSED parameter is passed back to the application module. The next thing TRANSMIT checks is the STATION_STATE. If this is not open, then TRANSMIT passes back LINK_DISCONNECTED. This means that the USER_STATE is open, but the SSD hasn't received an SNRM command from the primary yet. Therefore, the application software should wait awhile and try again. Based on network performance, one knows the maximum amount of time it will take for a station to be polled. If the application software waits this length of time and tries again but still gets a LINK_DISCONNECTED parameter passed back, higher level recovery must be implemented.

Before loading the transmit buffer and calling the TRANSMIT procedure, the application software must check to see that XMIT_BUFFER_EMPTY = 1. This flag tells the application software that it can write new data into the transmit buffer and call the TRANSMIT procedure. After the application software has verified that XMIT_BUFFER_EMPTY = 1, it fills the transmit buffer with the data and calls the TRANSMIT procedure passing the length of the buffer as a parameter. The TRANSMIT procedure checks for three reasons why it might not be able to transmit the frame. If any of these three reasons are true, the TRANSMIT procedure returns a parameter explaining why it couldn't send the frame. If the application software receives one of these responses, it must rectify the problem and try again. Assuming these three conditions are false, then the SSD clears XMIT_BUFFER_EMPTY, attempts to send the data and returns the parameter DATA_TRANSMITTED. XMIT_BUFFER_EMPTY will not be set to 1 again until the data has been transmitted and acknowledged.

The SIU_RECV procedure must be incorporated into the application software module. When a valid I frame is received by the SIU, it calls the SIU_RECV procedure and passes the length of the received data as a parameter. The SIU_RECV procedure must remove all of the data from the receive buffer before returning to the SIU_INT procedure.

LINKING UP TO THE SSD

Figure 12 shows the necessary parts to include in a PL/M-51 application program that will be linked to the SSD module. RL51 is used to link and locate the SSD and application modules. The command line used to do this is:

```
RL51 SSD.obj,filename.obj,PLM51.LIB TO
filename & RAMSIZE(192)

$registerbank(0)
user$mod: do;
$include (reg44.dcl)
declare
 lit               literally 'literally',
 buffer_length     lit           '60',
 siu_xmit_buffer
 (buffer_length)   byte    external idata,
 siu_recv_buffer
 (buffer_length)   byte        external,
 xmit_buffer_empty bit         external;

/* external procedures */

power_on_d: procedure  external;
end power_on_d;

close: procedure       external using 1;
end close;

open: procedure        external using 1;
end open;

transmit: procedure
(xmit_buffer_length) byte       external;
 declare xmit_buffer_length      byte;
end transmit;

/* local procedures */

siu_recv: procedure (length)     using 1;
public
 declare   length byte,
        •
        •
        •
end siu_recv;
```

Figure 12. Applications Module Link Information

PL/M-51 AND REGISTER BANKS

The 8044 has four register banks. PL/M-51 assumes that an interrupt procedure never uses the same bank as the procedure it interrupts. The USING attribute of a procedure, or the $REGISTERBANK control, can be used to ensure that.

The SSD module uses the $REGISTERBANK(1) attribute. Some procedures are modified with the USING attribute based on the register bank level of the calling procedure.

2.4 Application Module; ASYNC to SDLC Protocol Converter

One of the purposes of this application module is to demonstrate how to interface software to the SSD. Another purpose is to implement and test a practical application. This application software performs I/O with an async terminal through a USART, buffers data, and also performs I/O with the SSD. In addition, it allows the user on the async terminal to: set the station address, set the destination address, and go online and offline. Setting the station address sets the byte in the STAD register. The destination address is the first byte in the I field. Going online or offline results in either calling the OPEN or CLOSE procedure respectively.

After the secondary station powers up, it enters the 'terminal mode', which accepts data from the terminal. However, before any data is sent, the user must configure the station. The station address and destination address must be set, and the station must be placed online. To configure the station the ESC character is entered at the terminal which puts the protocol converter into the 'configure mode'. Figure 13 shows the menu which appears on the terminal screen.

```
(/)8044 Secondary Station
 /

1 - Set the Station Address
2 - Set the Destination Address
3 - Go Online
4 - Go Offline
5 - Return to terminal mode
    Enter option __
```

Figure 13. Menu for the Protocol Converter

In the terminal mode data is buffered up in the secondary station. A Line Feed character 'LF' tells the secondary station to send an I frame. If more than 60 bytes are buffered in the secondary station when a 'LF' is received, the applications software packetizes the data into 60 bytes or less per frame. If a LF is entered when the station is offline, an error message comes on the screen which says 'Unable to Get Online'.

The secondary station also does error checking on the async interface for Parity, Framing Error, and Overrun Error. If one of these errors are detected, an error message is displayed on the terminal screen.

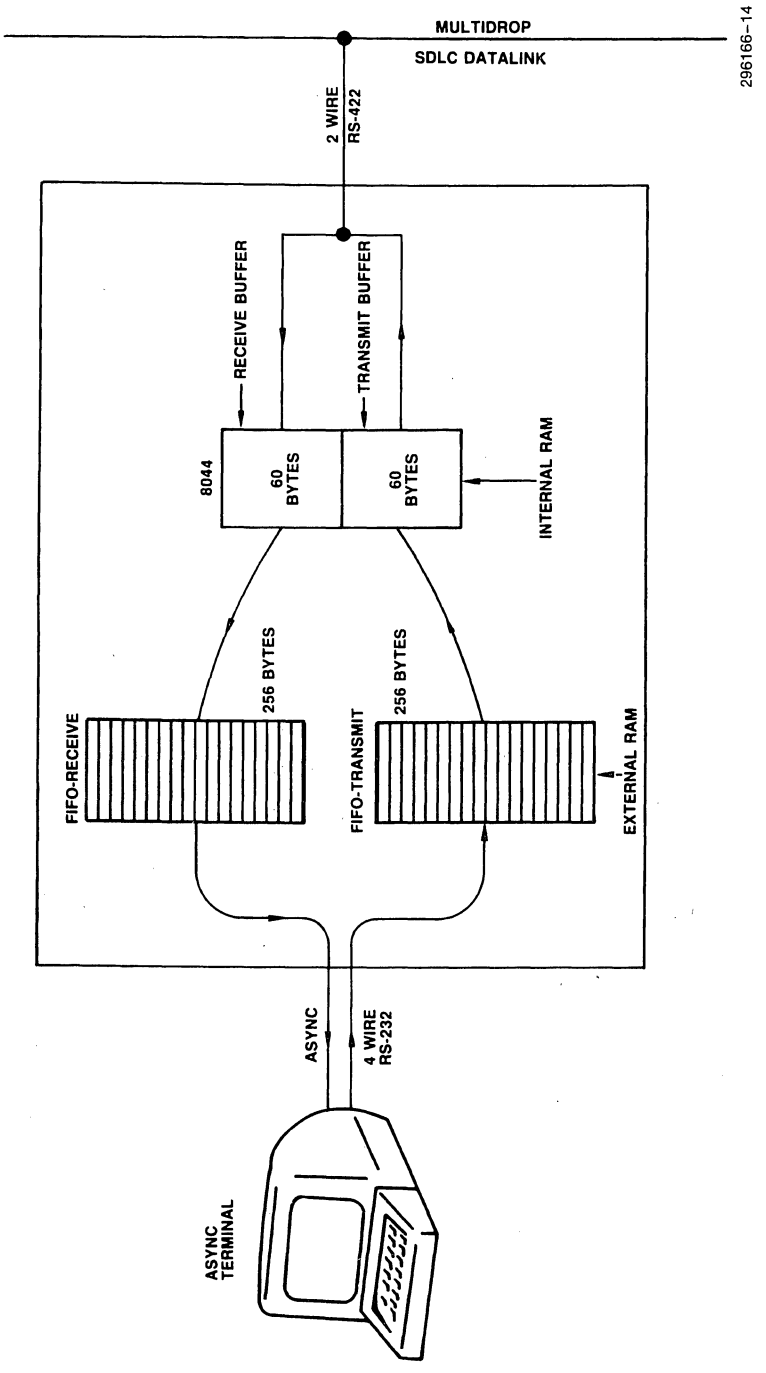


Figure 14. Block Diagram of Secondary Station Protocol Converter Illustrating Buffering

BUFFERING

There are two separate buffers in the application module: a transmit buffer and a receive buffer. The transmit buffer receives data from the USART, and sends data to the SSD. The receive buffer receives data from the SSD, and transmits data to the USART. Each buffer is a 256 byte software FIFO. If the transmit FIFO becomes full and no 'LF' character is received, the secondary station automatically begins sending the data. In addition, the application modules will shut off the terminal's transmitter using CTS until the FIFO has been partially emptied. A block diagram of the buffering for the protocol converter is given in Figure 14.

APPLICATION MODULE SOFTWARE

A block diagram of the application module software is given in Figure 15. There are three interrupt routines in this module: USART_RECV_INT, USART_XMIT_INT, and TIMER_0_INT. The first two are for servicing the USART. TIMER_0_INT is used if the TRANSMIT procedure in the SSD is called and does not return with the DATA_TRANSMITTED parameter. TIMER_0_INT employs Timer 0 to wait a finite amount of time before trying to transmit again. The highest priority interrupt is USART_RECV_INT. The main program and all the procedures it calls use register bank 0, USART_XMIT_INT and TIMER_0_INT and FIFO_R_OUT use bank 1, while USART_RECV_INT and all the procedures it calls use register bank 2.

POWER_ON PROCEDURE

The Power_On procedure initializes all of the chips in the system including the 8044. The 8044 is initialized to use the on-chip DPLL with NRZI coding, PreFrame Sync, and Timer 1 auto reload at a baud rate of 62.5 Kbps. The 8254 and the 8251A are initialized next based on the DIP switch values attached to port 1 on the 8044. Variables and pointers are initialized, then the SSD's Power-Up Procedure, Power_On_D, is called. Finally, the interrupt system is enabled and the main program is entered.

MAIN PROGRAM

The main program is a simple loop which waits for a frame transmit command. A frame transmit command is indicated when the variable SEND_DATA is greater than 0. The value of SEND_DATA equals the number of 'LF' characters in the transmit FIFO, hence it also indicates the number of frames pending transmission. Each time a frame is sent, SEND_DATA is decremented by one. Thus when SEND_DATA is greater than 0, the main program falls down into the next loop which polls the XMIT_BUFFER_EMPTY bit. When XMIT_BUFFER_EMPTY equals 1, the SIU_XMIT_BUFFER can be loaded. The first byte in the buffer is loaded with the destination address while the rest of the buffer is loaded with the data. Bytes are removed from the transmit FIFO and placed into the SIU_XMIT_BUFFER until one of three things happen: 1. a 'LF' character is read out of the FIFO, 2. the number of bytes loaded equals the size of the SIU_XMIT_BUFFER, or 3. the transmit FIFO is empty.

After the SIU_XMIT_BUFFER is filled, the SSD TRANSMIT procedure is called and the results from the procedure are checked. Any result other than DATA_TRANSMITTED will result in several retries within a finite amount of time. If all the retries fail, then the LINK_DISC procedure is called which sends a message to the terminal, 'Unable to Get Online'.

USART_RECV_INT PROCEDURE

When the 8251A receives a character, the RxRDY pin on the 8251A is activated, and this interrupt procedure is entered. The routine reads the USART status register to determine if there are any errors in the character received. If there are, the character is discarded and the ERROR procedure is called which prints the type of error on the screen. If there are no errors, the received character is checked to see if it's an ESC. If it is an ESC, the MENU procedure is called which allows the user to change the configuration. If neither one of these two conditions exists, the received character is inserted into the transmit FIFO. The received character may or may not be echoed back to the terminal based on the dip switch settings.

TRANSMIT FIFO

The transmit FIFO consists of two procedures: FIFO_T_IN and FIFO_T_OUT. FIFO_T_IN inserts a character into the FIFO, and FIFO_T_OUT removes a character from the FIFO. The FIFO itself is an array of 256 bytes called FIFO_T. There are two pointers used as indexes in the array to address the characters: IN_PTR_T and OUT_PTR_T. IN_PTR_T points to the location in the array which will store the next byte of data inserted. OUT_PTR_T points to the next byte of data removed from the array. Both IN_PTR_T and OUT_PTR_T are declared as bytes. The FIFO_T_IN procedure receives a character from the USART_RECV_INT procedure and stores it in the array location pointed to by IN_PTR_T, then IN_PTR_T is incremented. Similarly, when FIFO_T_OUT is called by the main program, to load the SIU_XMIT_BUFFER, the byte in the array

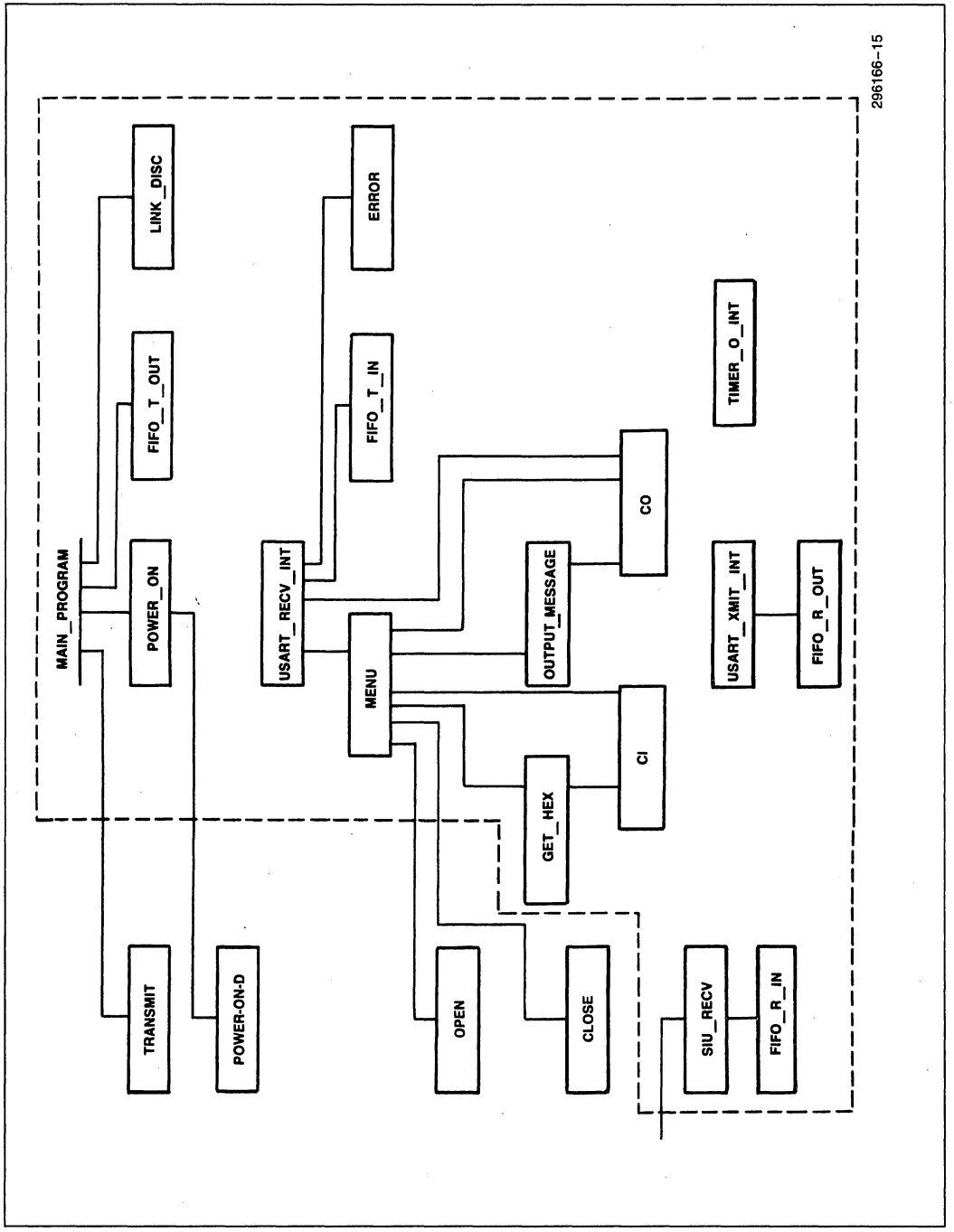


Figure 15. Block Diagram of User Software

pointed to by OUT_PTR_T is read, then OUT_PTR_T is incremented. Since IN_PTR_T and OUT_PTR_T are always incremented, they must be able to roll over when they hit the top of the 256 byte address space. This is done automatically by having both IN_PTR_T and OUT_PTR_T declared as bytes. Each character inserted into the transmit FIFO is tested to see if it's a LF. If it is a LF, the variable SEND_DATA is incremented, which lets the main program know that it is time to send an I frame. Similarly each character removed from the FIFO is tested. SEND_DATA is decremented for every LF character removed from the FIFO.

IN_PTR_T and OUT_PTR_T are also used to indicate how many bytes are in the FIFO, and whether it is full or empty. When a character is placed into the FIFO and IN_PTR_T is incremented, the FIFO is full if IN_PTR_T equals OUT_PTR_T. When a character is read from the FIFO and OUT_PTR_T is incremented, the FIFO is empty if OUT_PTR_T equals IN_PTR_T. If the FIFO is neither full nor empty, then it is in use. A byte called BUFFER_STATUS_T is used to indicate one of these three conditions. The application module uses the buffer status information to control the flow of data into and out of the FIFO. When the transmit FIFO is empty, the main program must stop loading bytes into the SIU_XMIT_BUFFER. Just before the FIFO is full, the async input must be shut off using CTS. Also, if the FIFO is full and SEND_DATA = 0, then SEND_DATA must be incremented to automatically send the data without an LF.

RECEIVE FIFO

The receive FIFO operates in a fashion similar to the transmit FIFO. Data is inserted into the receive FIFO from the SIU_RECV procedure. The SIU_RECV procedure is called by the SIU_INT procedure when a valid I frame is received. The SIU_RECV procedure merely polls the receive FIFO status to see if it's full before transferring each byte from the SIU_RECV_BUFFER into the receive FIFO. If the receive FIFO is full, the SIU_RECV procedure remains polling the FIFO status until it can insert the rest of the data. In the meantime, the SIU AUTO mode is responding to all polls from the primary with a RNR supervisory frame. The USART_XMIT_INT interrupt procedure removes data from the receive FIFO and transmits it to the terminal. The USART transmit interrupt remains enabled while the receive FIFO has data in it. When the receive FIFO becomes empty, the USART transmit interrupt is disabled.

2.5 Primary Station

The primary station is responsible for controlling the data link. It issues commands to the secondary stations and receives responses from them. The primary station controls link access, link level error recovery, and the flow of information. Secondaries can only transmit when polled by the primary.

Most primary stations are either micro/minicomputers, or front end processors to a mainframe computer. The example primary station in this design is standalone. It is possible for the 8044 to be used as an intelligent front end processor for a microprocessor, implementing the primary station functions. This latter type of design would extensively off-load link control functions for the microprocessor. The code listed in this paper can be used as the basis for this primary station design. Additional software is required to interface to the microprocessor. A hardware design example for interfacing the 8044 to a microprocessor can be found in the applications section of this handbook.

The primary station must know the addresses of all the stations which will be on the network. The software for this primary needs to know this before it is compiled, however a more flexible system would download these parameters.

From the listing of the software it can be seen that the variable NUMBER_OF_STATIONS is a literal declaration, which is 2 in this design example. There were three stations tested on this data link, two secondaries and one primary. Following the NUMBER_OF_STATIONS declaration is a table, loaded into the object code file at compile time, which lists the addresses of each secondary station on the network.

REMOTE STATION DATABASE

The primary station keeps a record of each secondary station on the network. This is called the Remote Station Database (RSD). The RSD in this software is an array of structures, which can be found in the listing and also in Figure 16. Each RSD stores the necessary information about that secondary station.

To add additional secondary stations to the network, one simply adjusts the NUMBER_OF_STATIONS declaration, and adds the additional addresses to the SECONDARY_ADDRESSES table. The number of RSDs is automatically allocated at compile time, and the primary automatically polls each station whose address is in the SECONDARY_ADDRESSES table.

Memory for the RSDs resides in external RAM. Based on memory requirements for each RSD, the maximum number of stations can be easily buffered in external RAM. (254 secondary stations is the maximum number SDLC will address on the data link; i.e. 8-bit address, FF H is the broadcast address, and 0 is the null address. Each RSD uses 70 bytes of RAM. 70 x 254 = 17,780.)

The station state, in the RSD structure, maintains the status of the secondary. If this byte indicates that the secondary is in the DISCONNECT_S, then the primary tries to put the station in the I_T_S by sending an SNRM. If the response is a UA then the station state changes into the I_T_S. Any other frame received results in the station state remaining in the DISCONNECT_S. When the RSD indicates that the station state is in the I_T_S, the primary will send either an I, RR, or RNR command, depending on the local and remote buffer status. When the station state equals GO_TO_DISC the primary will send a DISC command. If the response is a UA frame, the station state will change to DISCONNECT_S, else the station state will remain in GO_TO_DISC. The station state is set to GO_TO_DISC when one of the following responses occur:

1. A receive buffer overrun in the primary.
2. An I frame is received and Nr(P) $\neq$ Ns(S).
3. An I frame or a Supervisory frame is received and Ns(P) + 1 $\neq$ Nr(S) and Ns(P) $\neq$ Nr(S).
4. A FRMR response is received.
5. An RD response is received.
6. An unknown response is received.

The send count (Ns) and receive count (Nr) are also maintained in the RSD. Each time an I frame is sent by the primary and acknowledged by the secondary, Ns is incremented. Nr is incremented each time a valid I frame is received. BUFFER_STATUS indicates the status of the secondary station's buffer. If an RR response is received, BUFFER_STATUS is set to BUFFER_READY. If a RNR response is received, BUFFER_STATUS is set to BUFFER_NOT_READY.

BUFFERING

The buffering for the primary station is as follows: within each RSD is a 64 byte array buffer which is initially empty. When the primary receives an I frame, it looks for a match between the first byte of the I frame and the addresses of the secondaries on the network. If a match exists, the primary places the data in the RSD buffer of the destination station. The INFO_LENGTH in the RSD indicates how many bytes are in the buffer. If INFO_LENGTH equals 0, then the buffer is empty. The primary can buffer only one I frame per station. If a second I frame is received while the addressed secondary's RSD buffer is full, the primary cannot receive any more I frames. At this point the primary continues to poll the secondaries using RNR supervisory frame.

PRIMARY STATION SOFTWARE

A block diagram of the primary station software is shown in Figure 17. The primary station software consists of a main program, one interrupt routine, and several procedures. The POWER_ON procedure begins by initializing the SIU's DMA and enabling the receiver. Then each RSD is initialized. The DPLL and the timers are set, and finally the TIMER 0 interrupt is enabled.

The main program consists of an iterative do loop within a do forever loop. The iterative do loop polls each secondary station once through the do loop. The variable STATION_NUMBER is the counter for the iterative do statement which is also used as an index to the array of RSD structures. The primary station issues one command and receives one response from every secondary station each time through the loop. The first statement in the loop loads the secondary station address, indexed by STATION_NUMBER into the array of the RSD structures. Now when the primary sends a command, it will have the secondary's address in the address field of the frame. The automatic address recognition feature is used by the primary to recognize the response from the secondary.

Next, the main program determines the secondary station's state. Based on this state, the primary knows what command to send. If the station is in the DISCONNECT_S, the primary calls the SNRM_P procedure to try and put the secondary in the I_T_S. If the station state is in the GO_TO_DISC state, the DISC_P is called to try and put the secondary in the L_D_S. If the secondary is in neither one of the above two states, then it is in the I_T_S. When the secondary is in the I_T_S, the primary could send one of three commands: I, RR, or RNR. If the RSD's buffer has data in it, indicated by INFO_LENGTH being greater than zero, and the secondary's BUFFER_STATUS equals BUFFER_READY, then an I frame will be sent. Else if RPB = 0, an RR supervisory frame will be sent. If neither one of these cases is true, then an RNR will be sent. The last statement in the main program checks the RPB bit. If set to one, the BUFFER_TRANSFER procedure is called, which transfers the data from the SIU receive buffer to the appropriate RSD buffer.

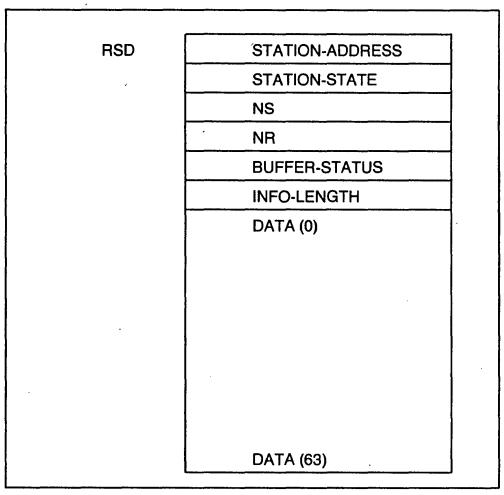


Figure 16. Remote Station Database Structure

RECEIVE TIME OUT

Each time a frame is transmitted, the primary sets a receive time out timer; Timer 0. If a response is not received within a certain time, the primary returns to the main program and continues polling the rest of the stations. The minimum length of time the primary should wait for a response can be calculated as the sum of the following parameters.

1. Propagation time to the secondary station
2. Clear-to-send at the secondary station's DCE
3. Appropriate time for secondary station processing
4. Propagation time from the secondary station
5. Maximum frame length time

The clear-to-send time and the propagation time are negligible for a local network at low bit rates. However, the turnaround time and the maximum frame length time are significant factors. Using the 8044 secondaries in the AUTO mode minimizes turnaround time. The maximum frame length time comes from the fact the 8044 does not generate an interrupt from a received frame until it has been completely received, and the CRC is verified as correct. This means that the time-out is bit rate dependent.

Ns AND Nr CHECK PROCEDURES

Each time an I frame or supervisory frame is received, the Nr field in the control byte must be checked. Since this data link only allows one outstanding frame, a valid Nr would satisfy either one of two equations; Ns(P) + 1 = Nr(S) the I frame previously sent by the primary is acknowledged, Ns(P) = Nr(S) the I frame previously sent is not acknowledged. If either one of these two cases is true, the CHECK_NR procedure returns a parameter of TRUE; otherwise a FALSE parameter is returned. If an acknowledgement is received, the Ns byte in the RSD structure is incremented, and the Information buffer may be cleared. Otherwise the information buffer remains full.

When an I frame is received, the Ns field has to be checked also. If Nr(P) = Ns(S), then the procedure returns TRUE, otherwise a FALSE is returned.

RECEIVE PROCEDURE

The receive procedure is called when a supervisory or information frame is sent, and a response is received before the time-out period. The RECEIVE procedure can be broken down into three parts. The first part is entered if an I frame is received. When an I frame is received, Ns, Nr and buffer overrun are checked. If there is a buffer overrun, or there is an error in either Ns or Nr, then the station state is set to GO_TO_DISC. Otherwise Nr in the RSD is incremented, the receive field length is saved, and the RPB bit is set. By incrementing the Nr field, the I frame just received is acknowledged the next time the primary polls the secondary with an I frame or a supervisory frame. Setting RBP protects the received data, and also tells the main program that there is data to transfer to one of the RSD buffers.

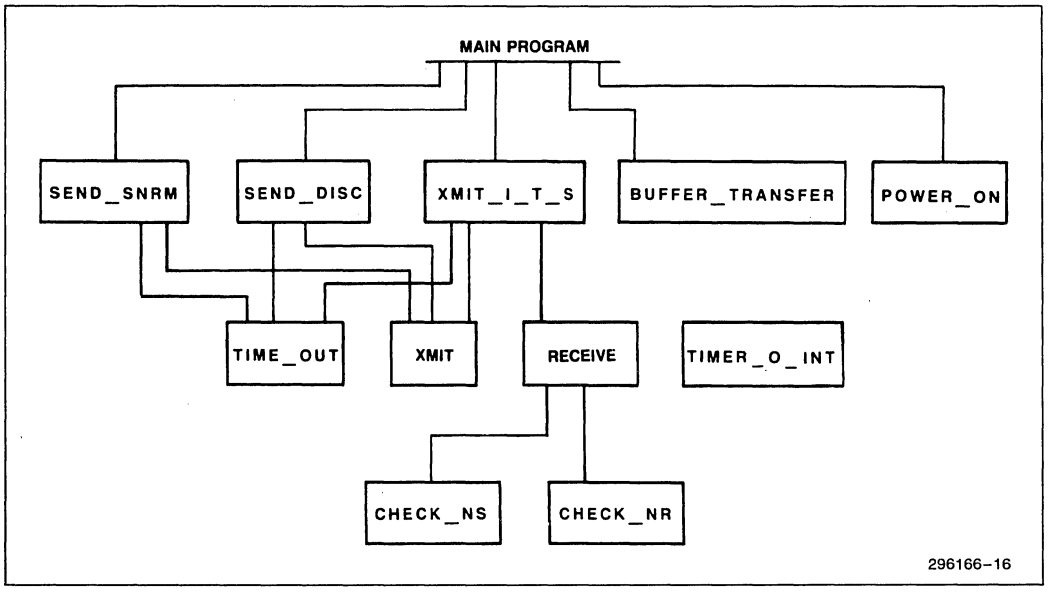


Figure 17. Block Diagram of Primary Station Software Structure

If a supervisory frame is received, the Nr field is checked. If a FALSE is returned, then the station state is set to GO_TO_DISC. If the supervisory frame received was an RNR, buffer status is set to not ready. If the response is not an I frame, nor a supervisory frame, then it must be an Unnumbered frame.

The only Unnumbered frames the primary recognizes are UA, DM, and FRMR. In any event, the station state is set to GO_TO_DISC. However, if the frame received is a FRMR, Nr in the second data byte of the I field is checked to see if the secondary acknowledged an I frame received before it went into the FRMR state. If this is not done and the secondary acknowledged an I frame which the primary did not recognize, the primary transmits the I frame when the secondary returns to the I_T_S. In this case, the secondary would receive duplicate I frames.

APPENDIX A
8044 SOFTWARE FLOWCHARTS

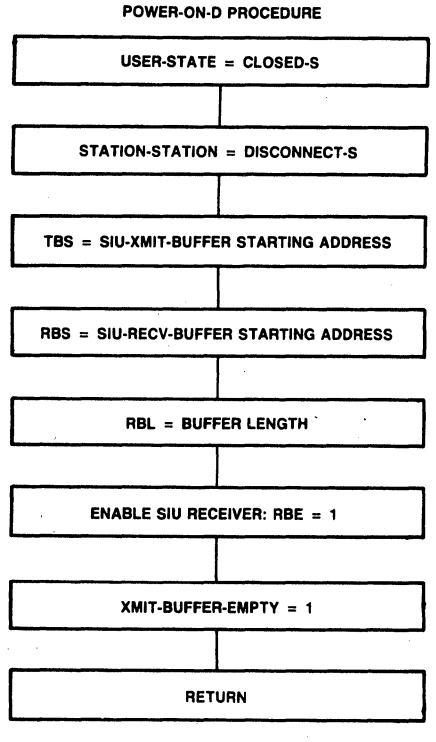
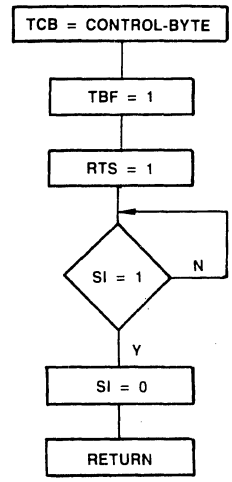


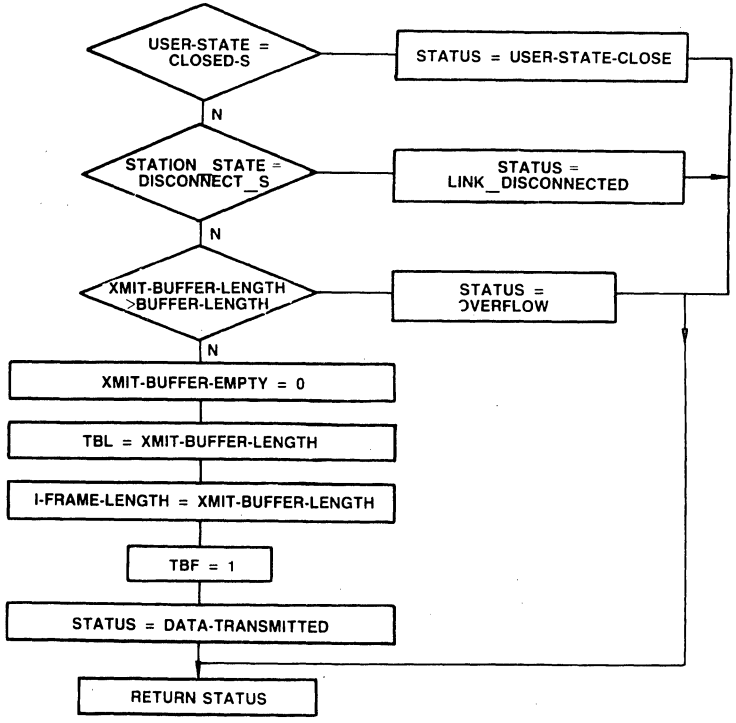
Figure 18. Secondary Station Driver Flow Chart

XMIT—UNNUMBERED PROCEDURE



296166-19

TRANSMIT PROCEDURE



296166-20

Figure 19. Secondary Station Driver Flow Chart

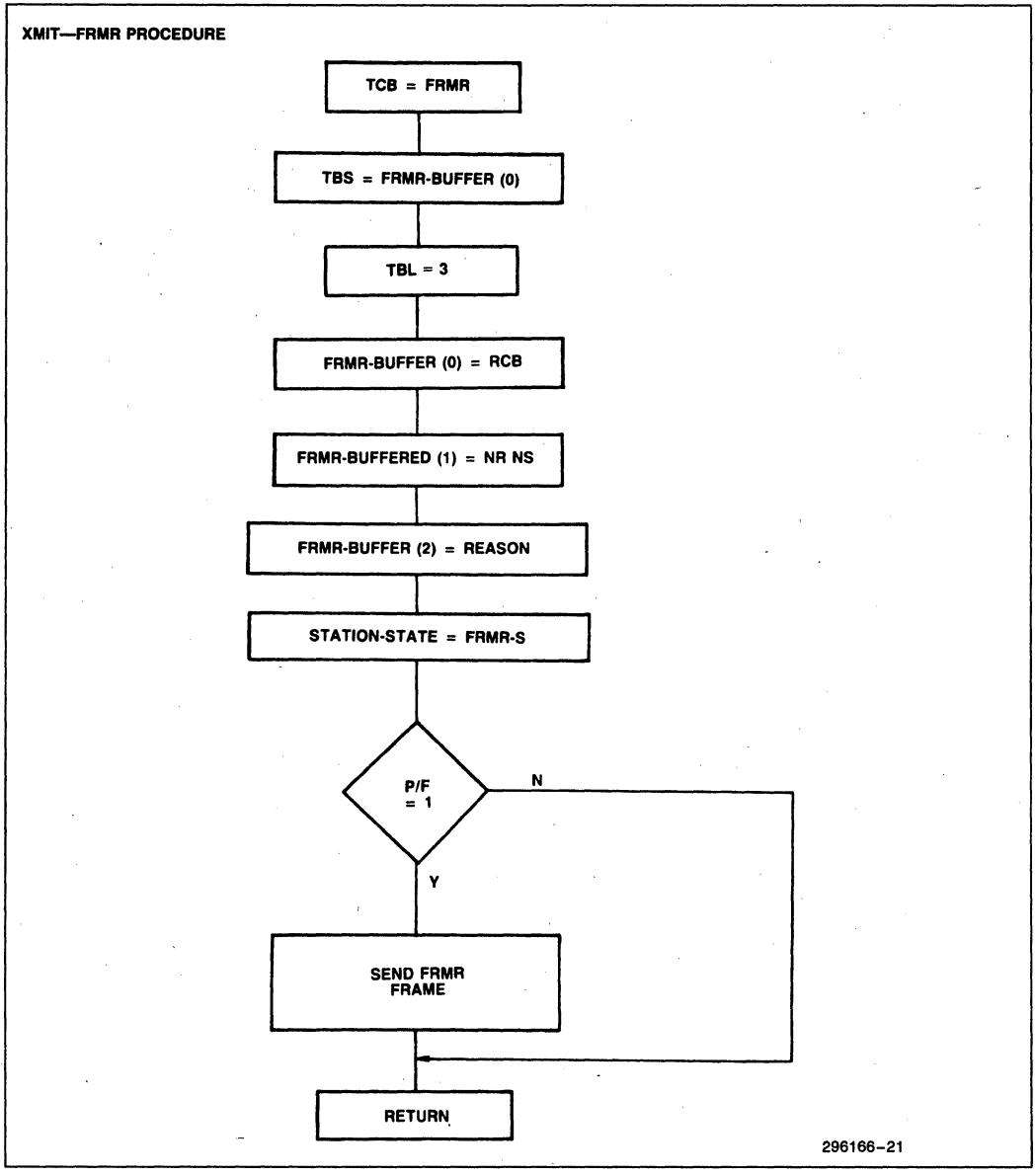
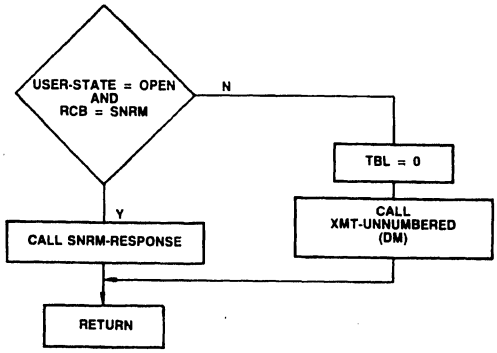


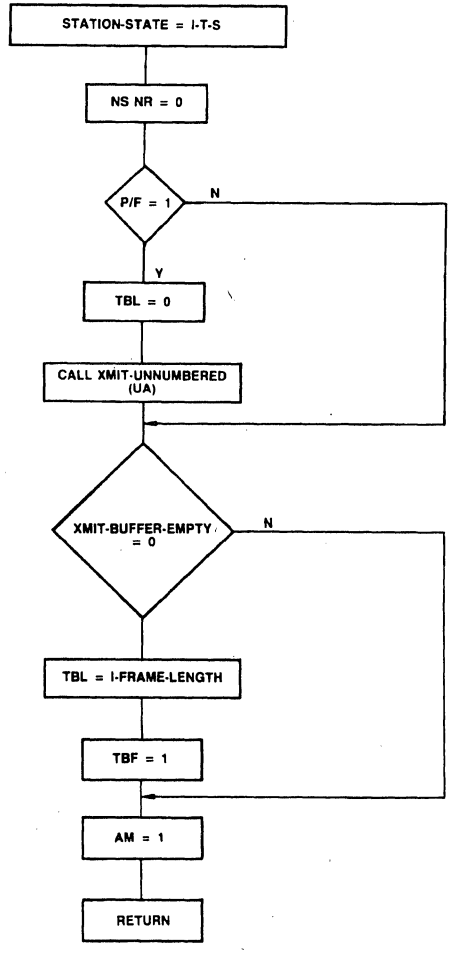
Figure 20. Secondary Station Driver Flow Chart

IN-DISCONNECT-STATE PROCEDURE



296166-22

SNRM-RESPONSE PROCEDURE



296166-23

Figure 21. Secondary Station Driver Flow Chart

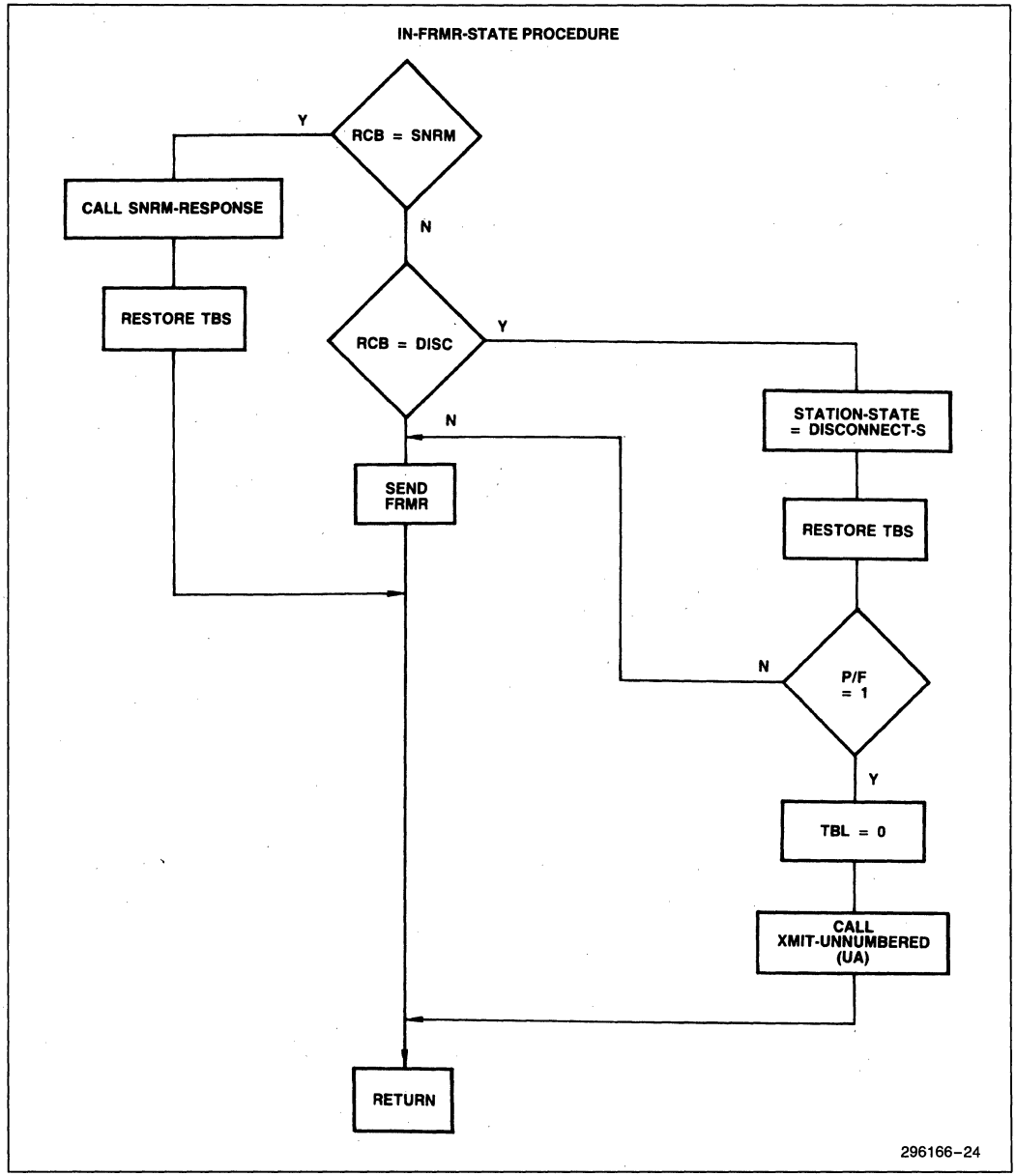
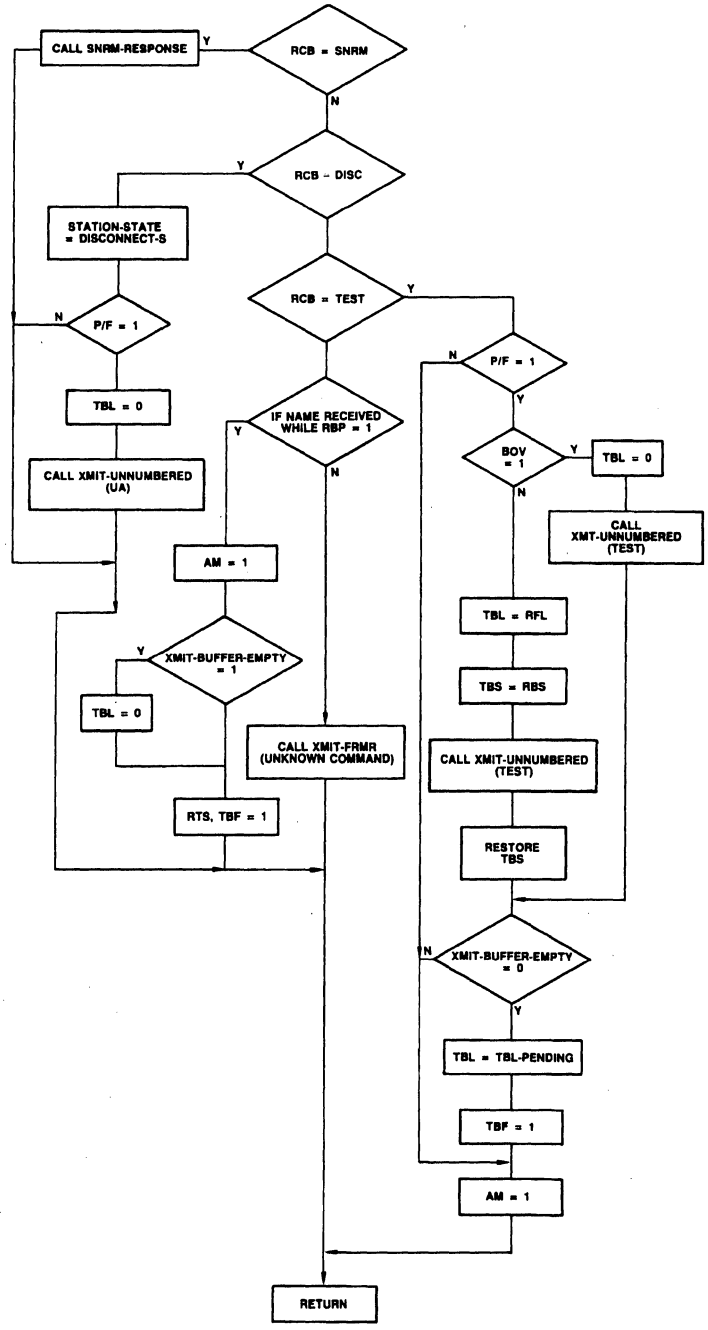


Figure 22. Secondary Station Driver Flow Chart

COMMAND DECODE PROCEDURE



296166-25

Figure 23. Secondary Station Driver Flow Chart

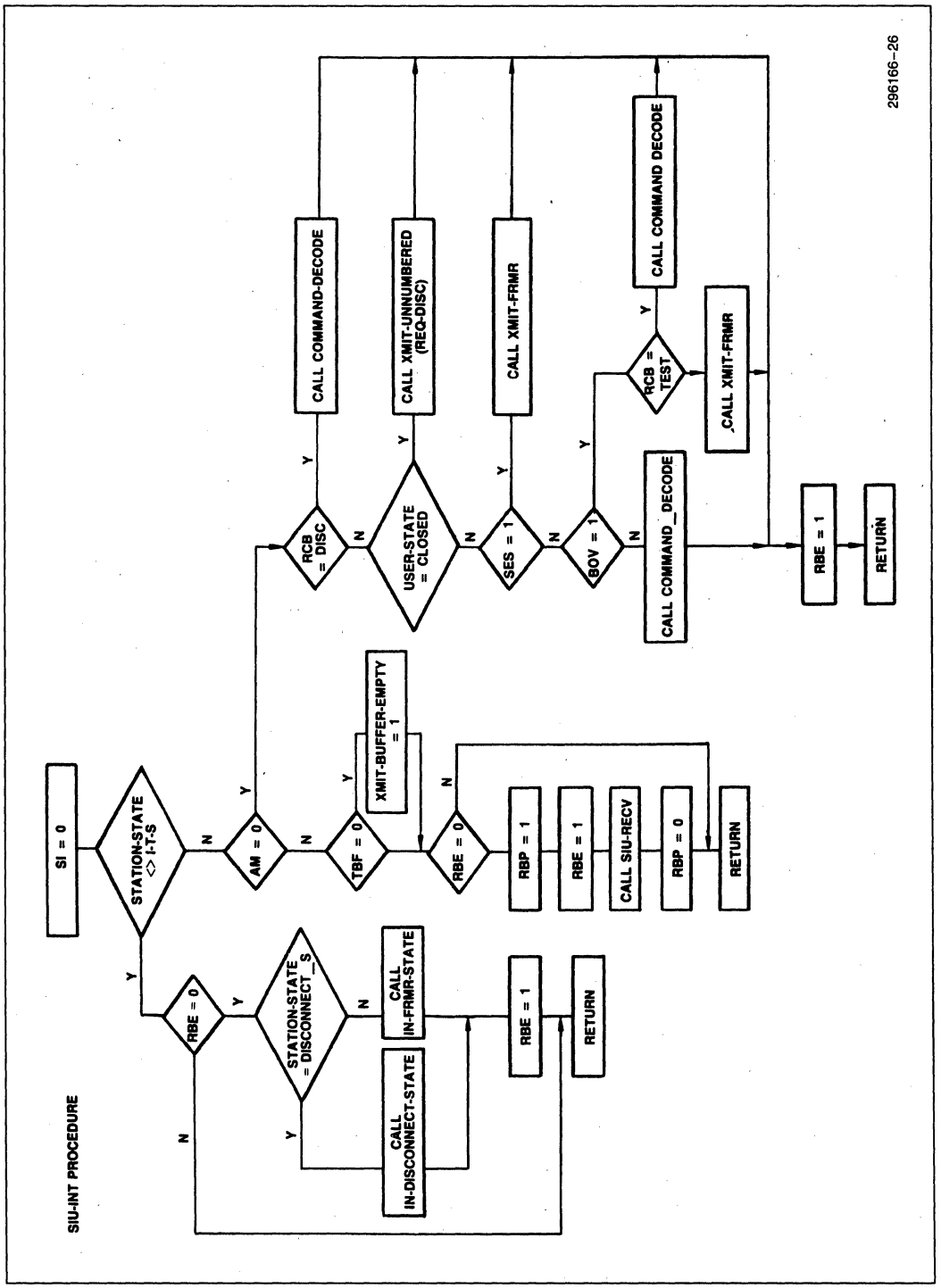


Figure 24. Secondary Station Driver Flow Chart

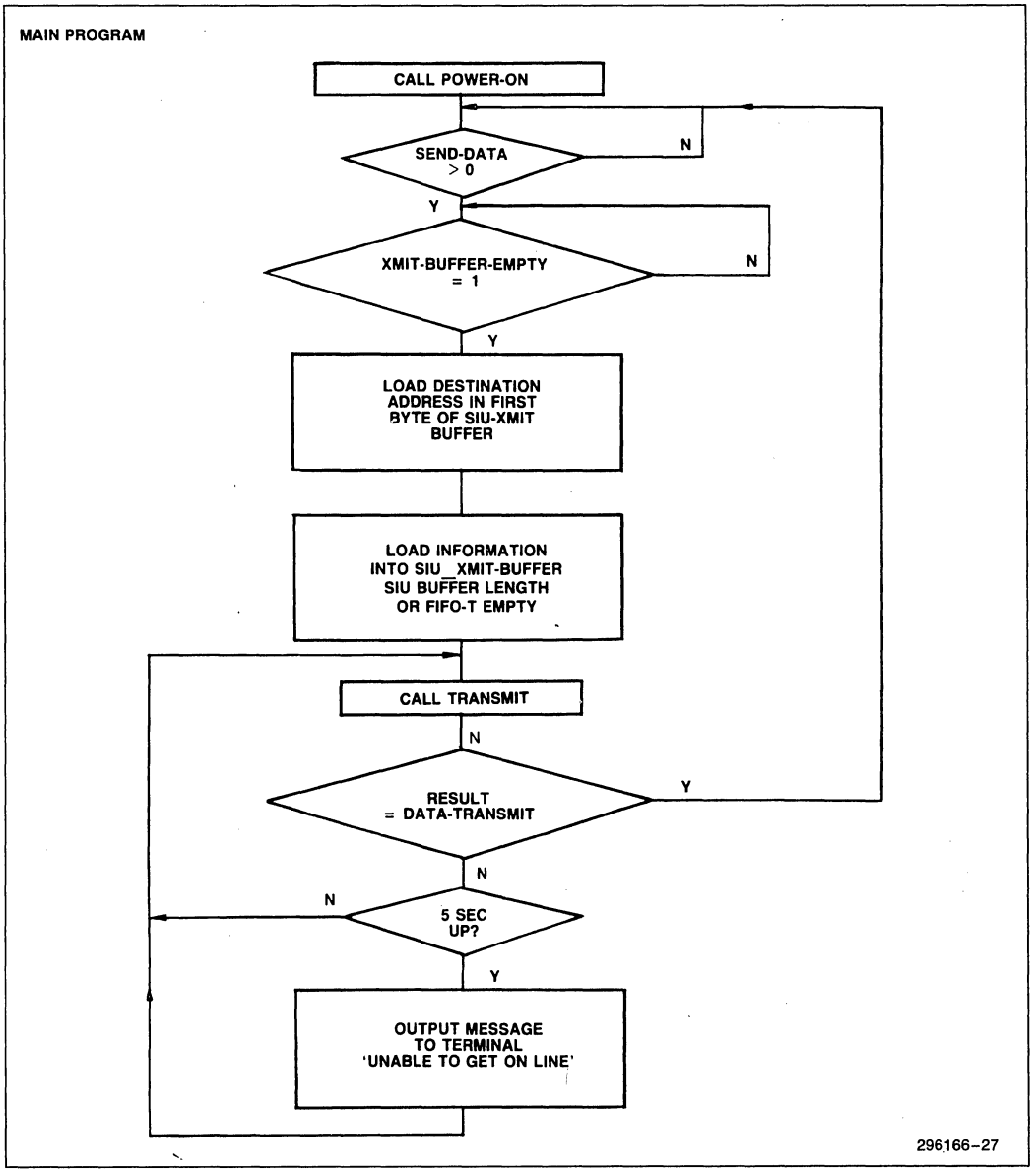


Figure 25. Application Module Flow Chart

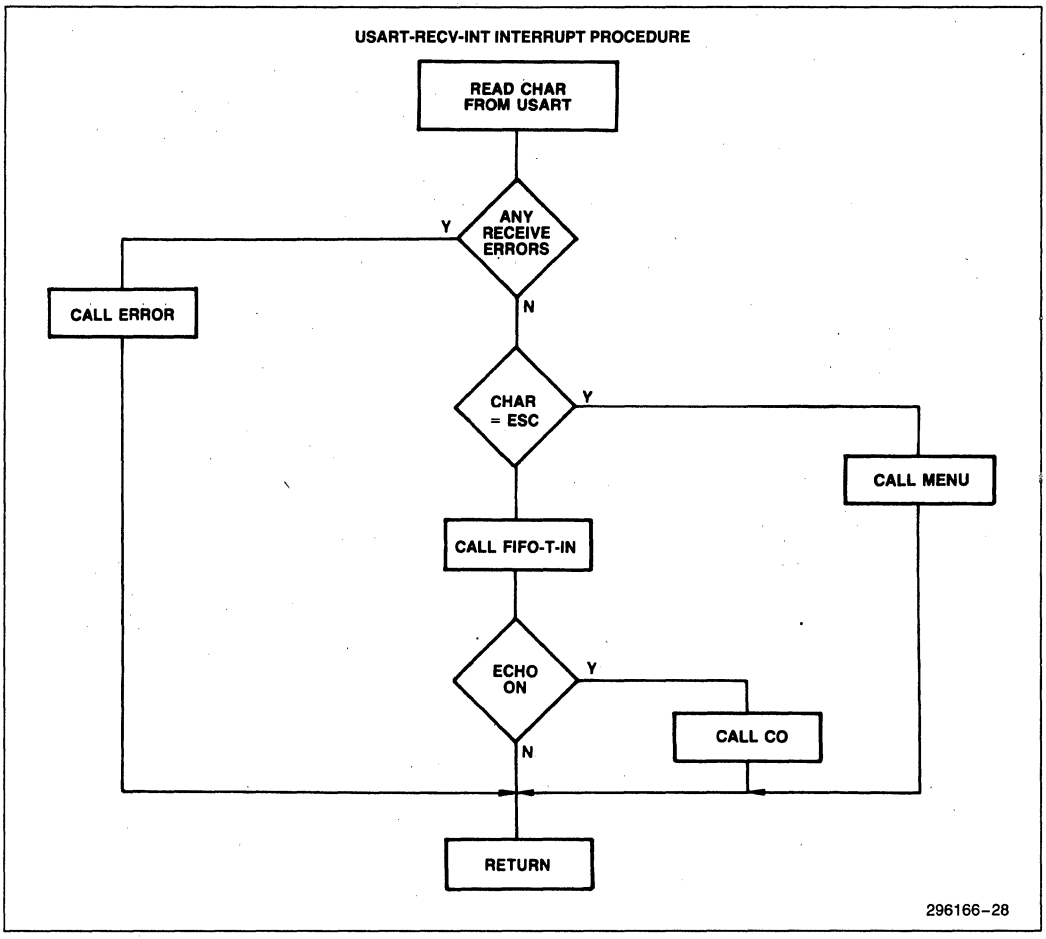


Figure 26. Application Module Flow Chart

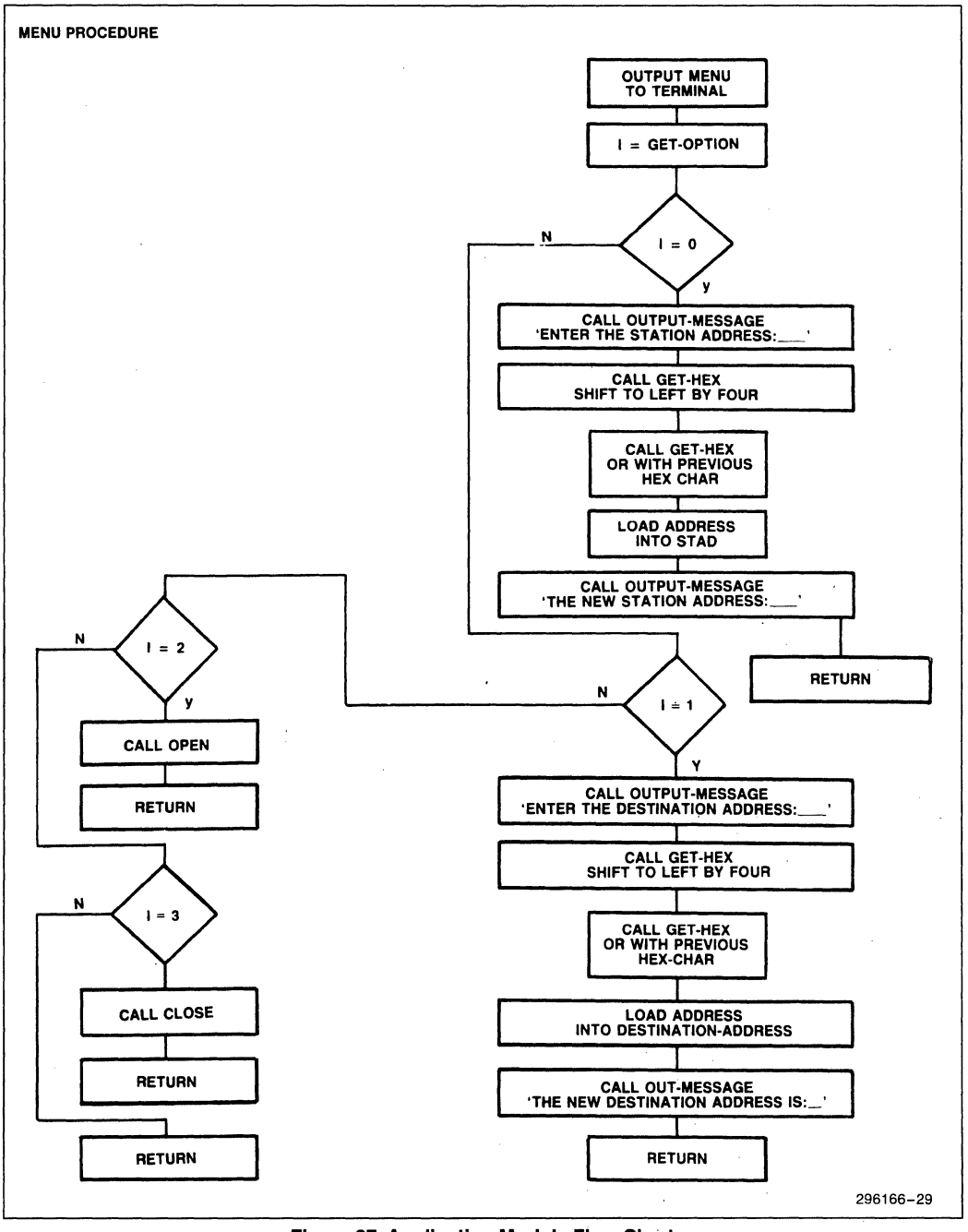


Figure 27. Application Module Flow Chart

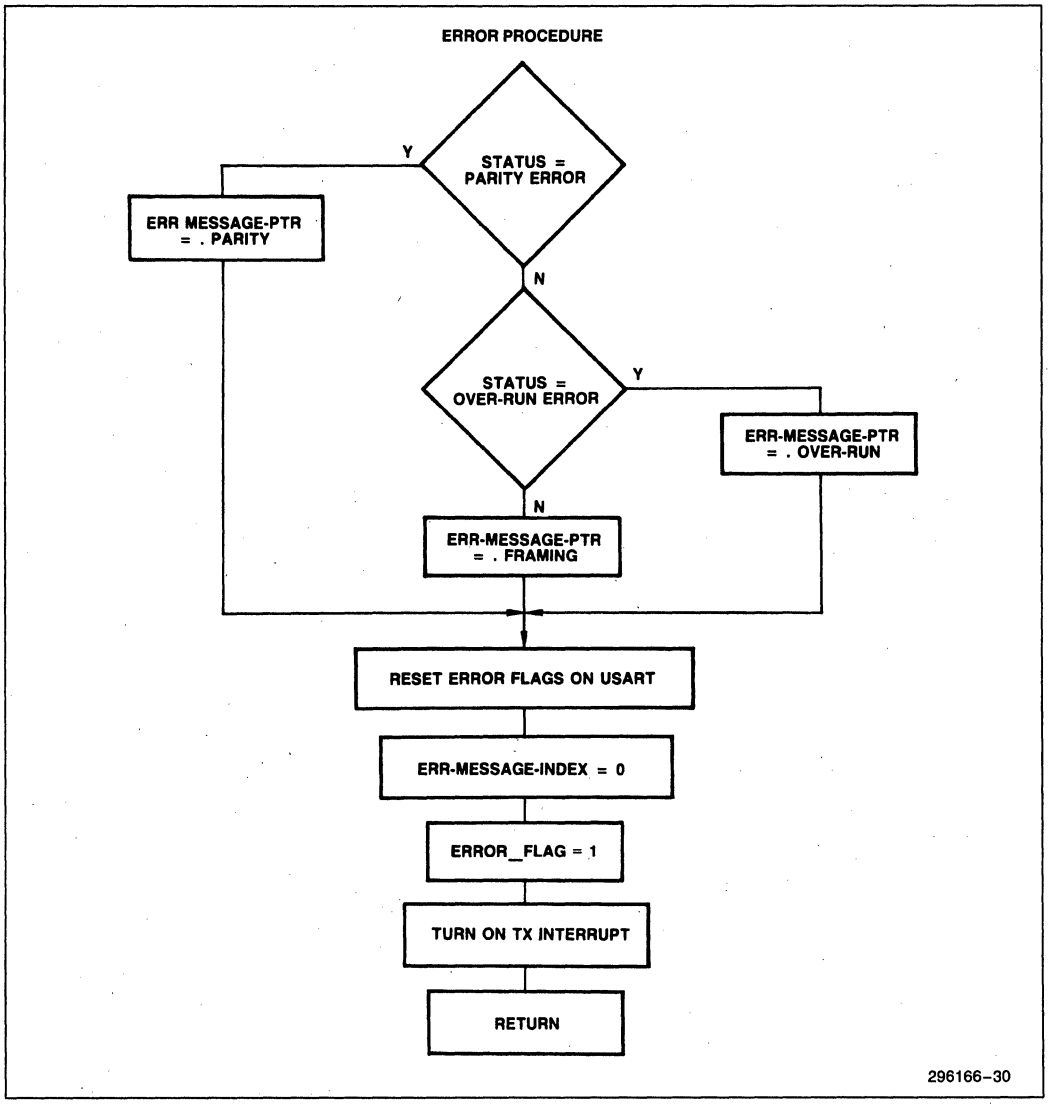


Figure 28. Application Module Flow Chart

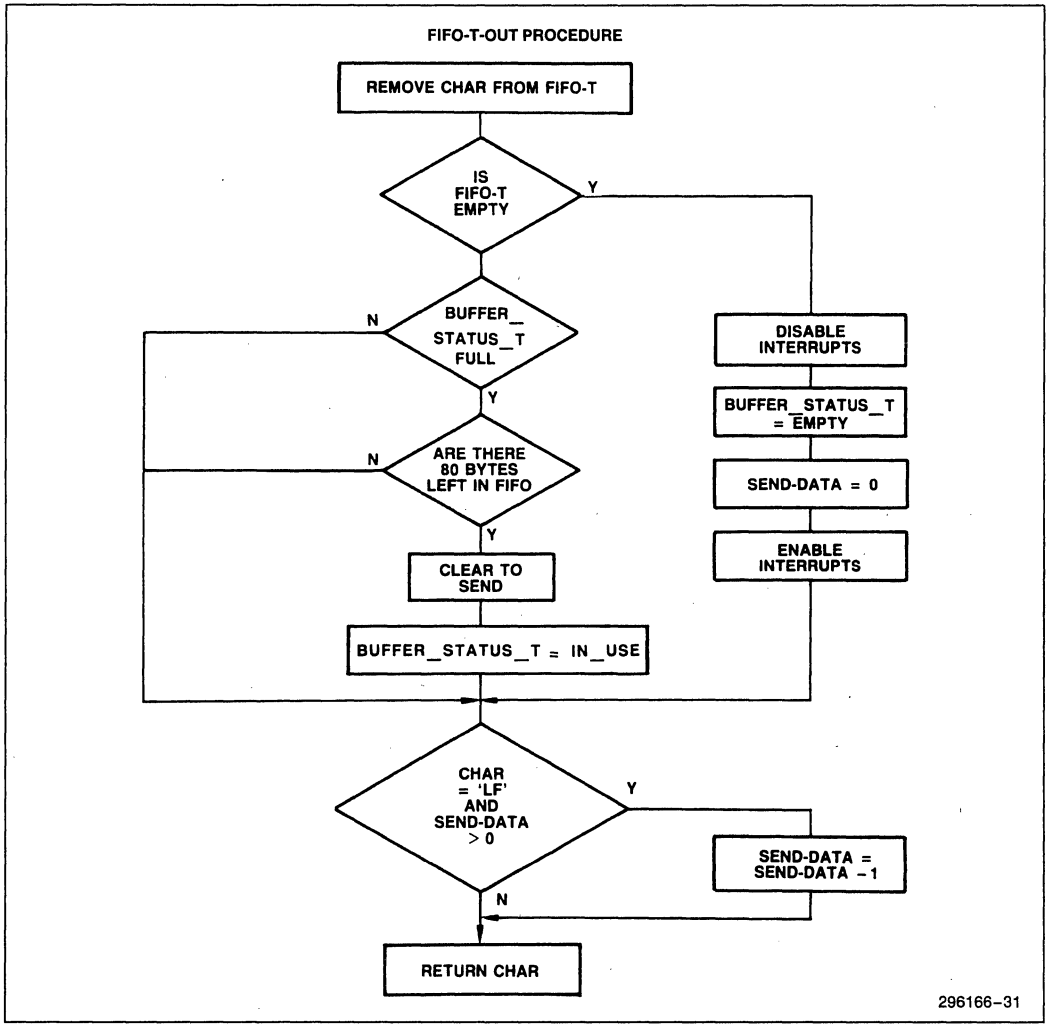


Figure 29. Application Module Flow Chart

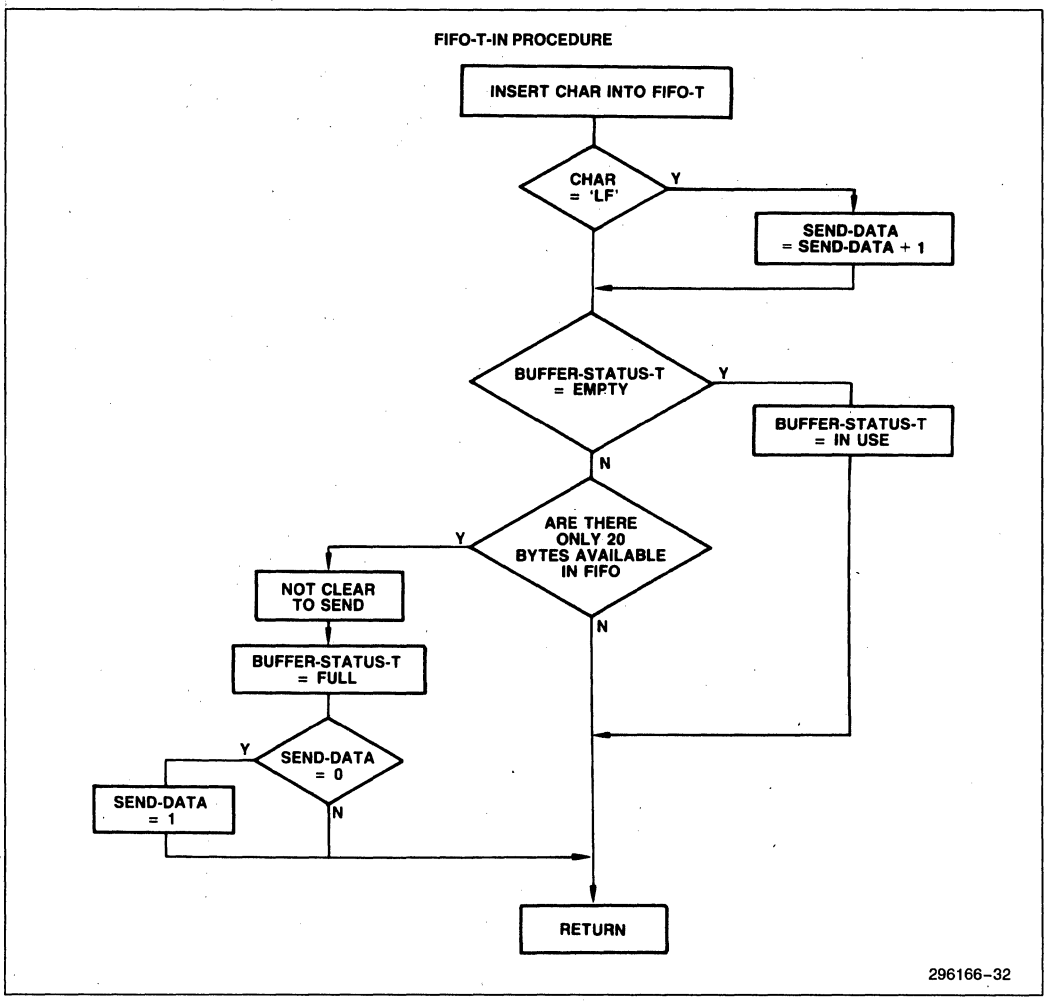


Figure 30. Application Module Flow Chart

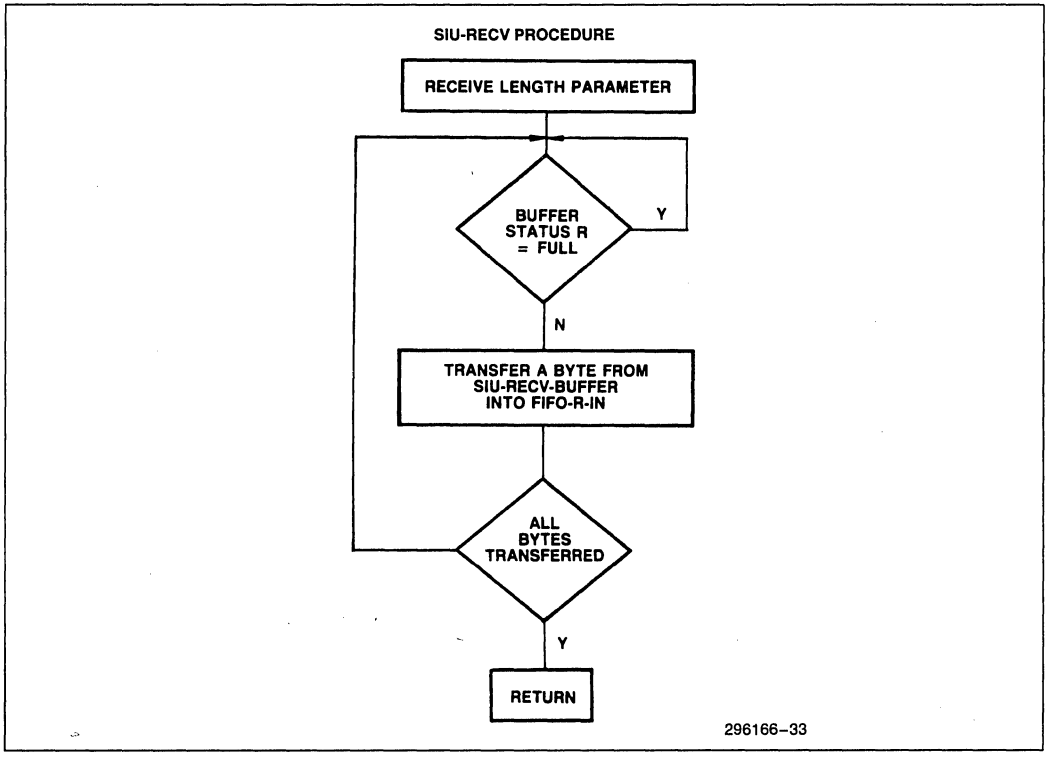


Figure 31. Application Module Flow Chart

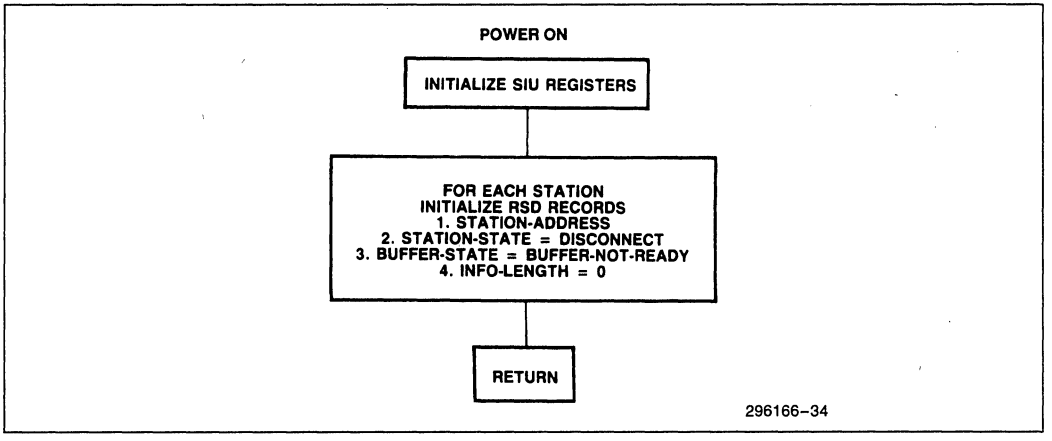


Figure 32. Primary Station Flow Charts

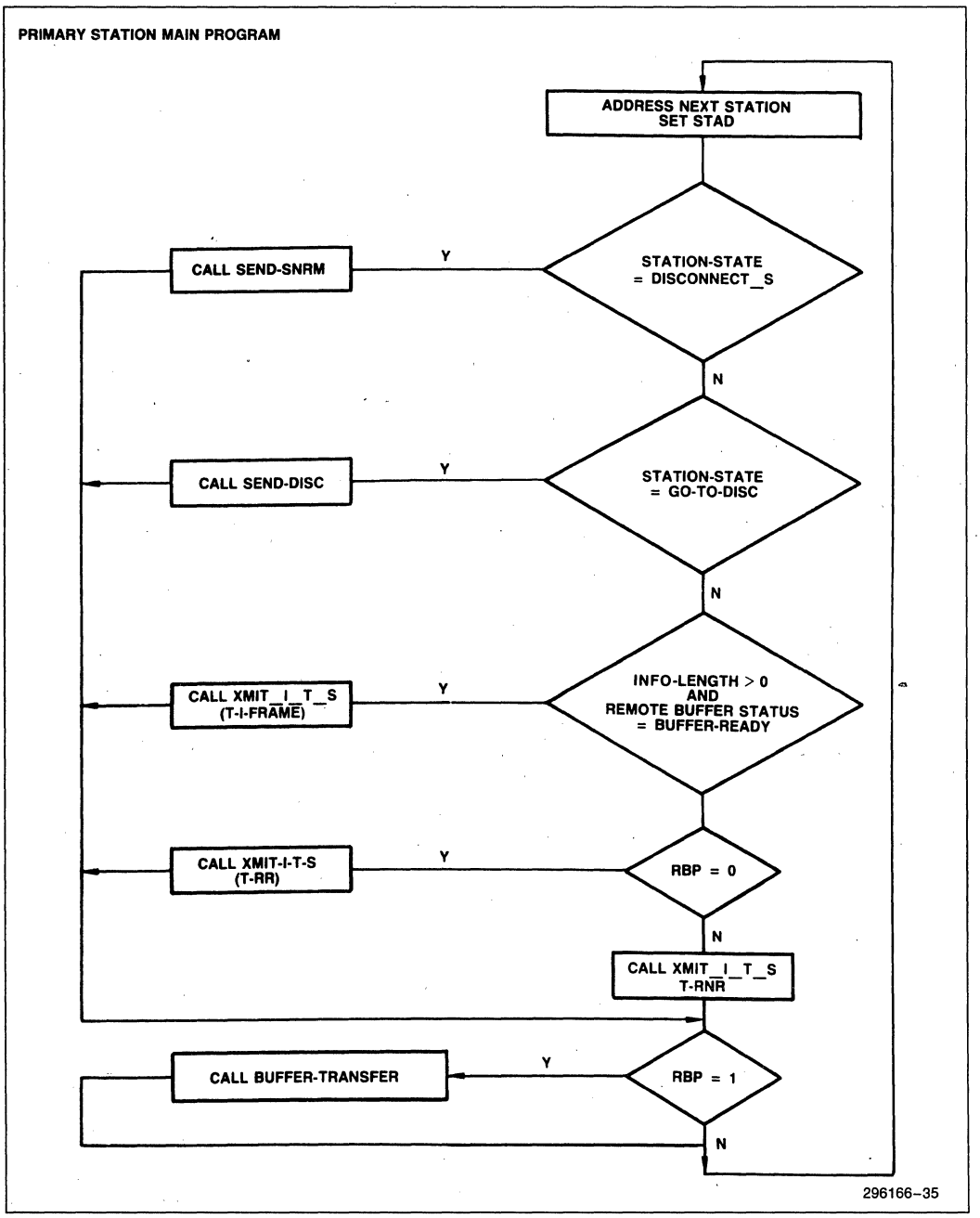


Figure 33. Primary Station Flow Charts

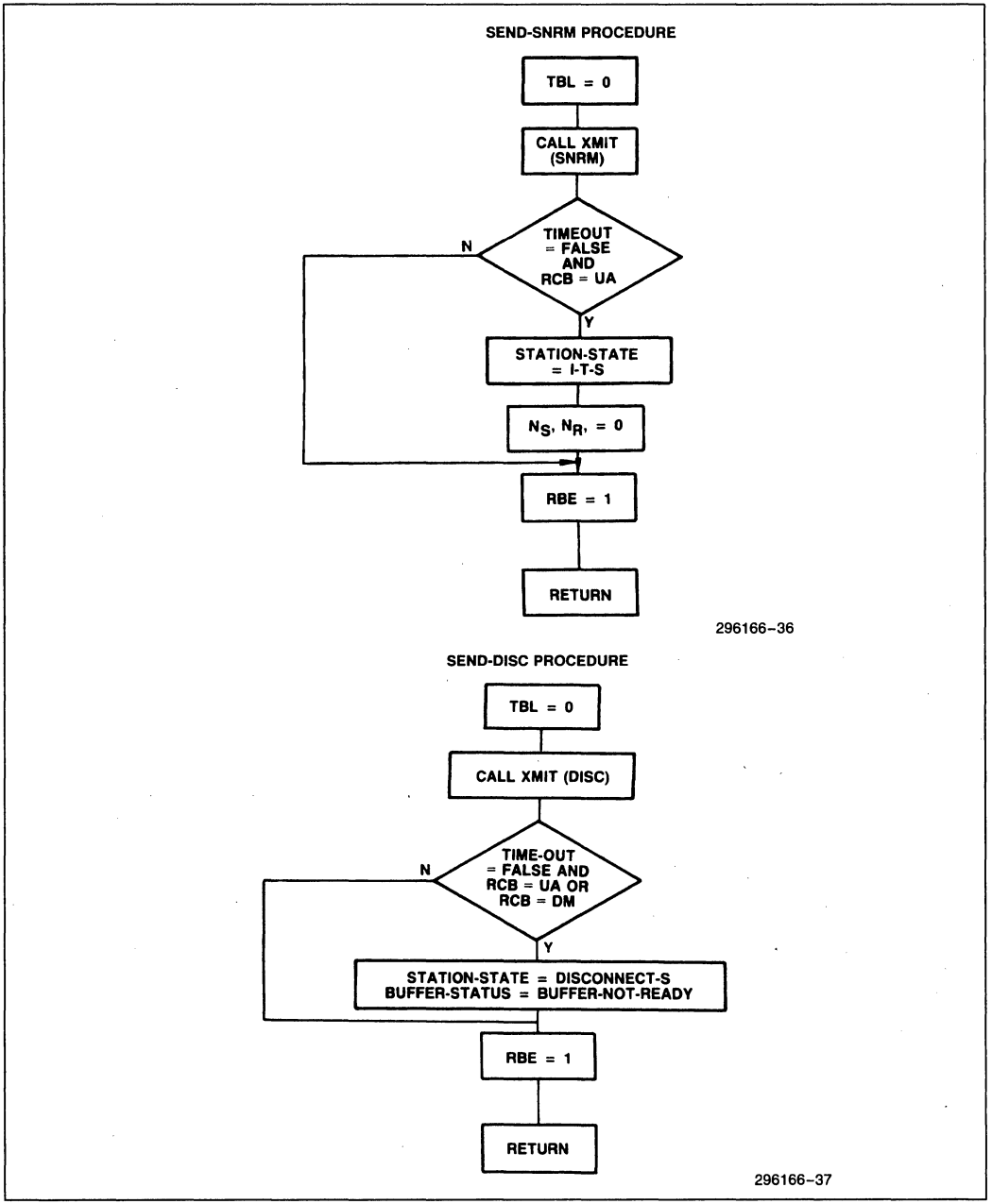
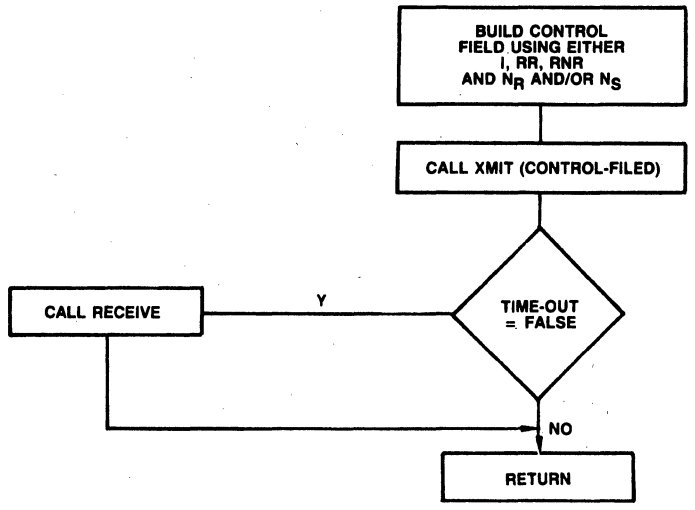


Figure 34. Primary Station Flow Charts

XMIT-T-S PROCEDURE



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XMIT PROCEDURE

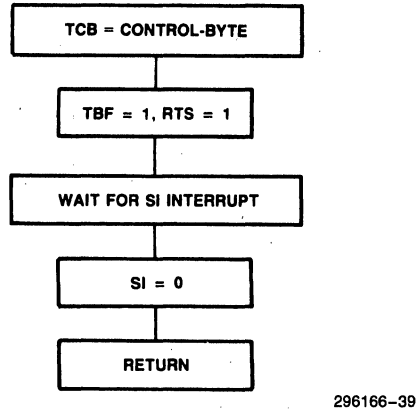

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Figure 35. Primary Station Flow Charts

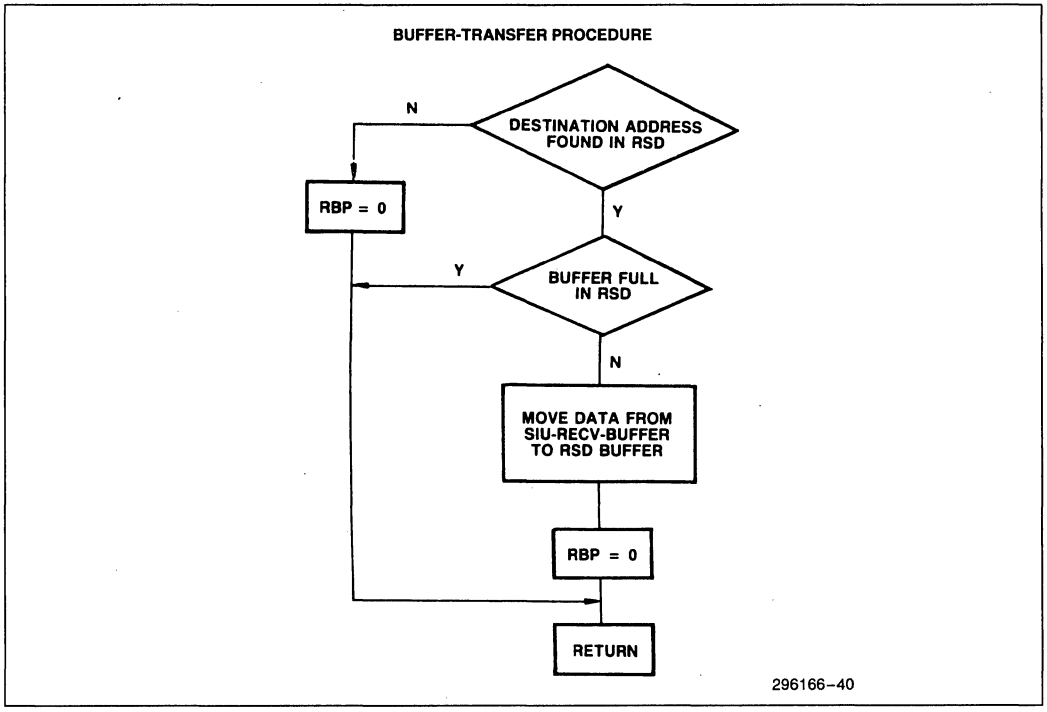

Figure 36. Primary Station Flow Charts

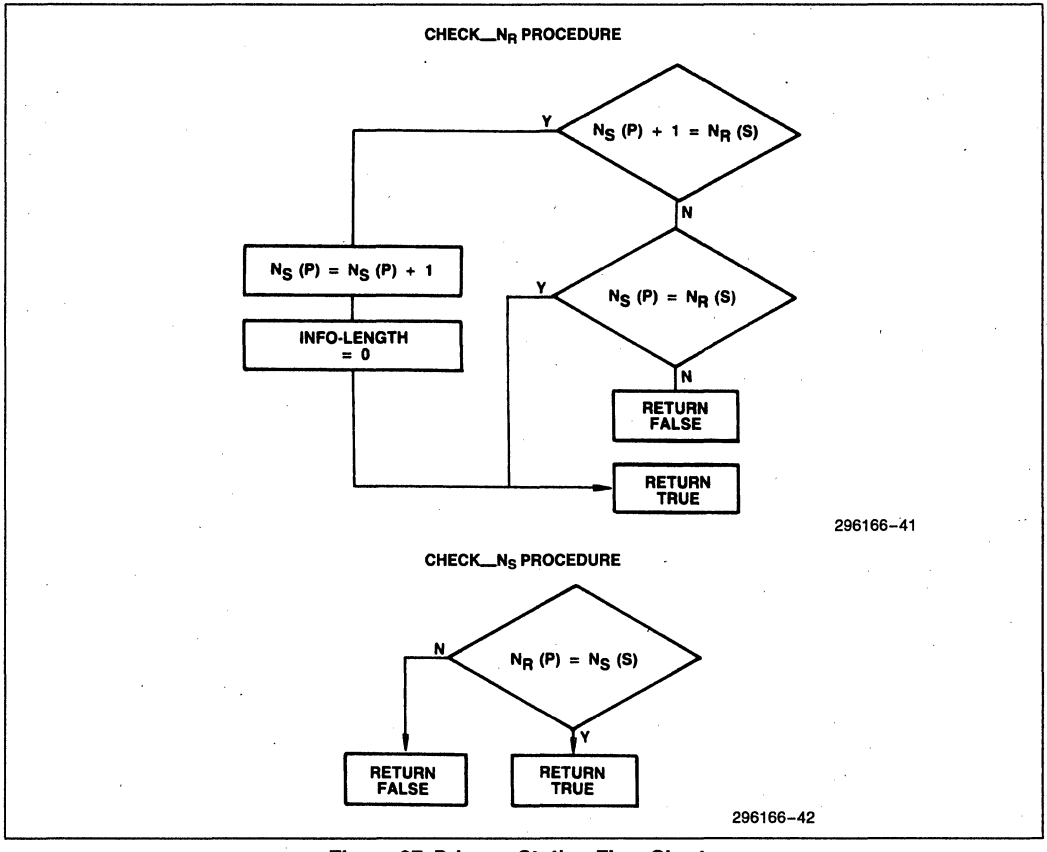

Figure 37. Primary Station Flow Charts

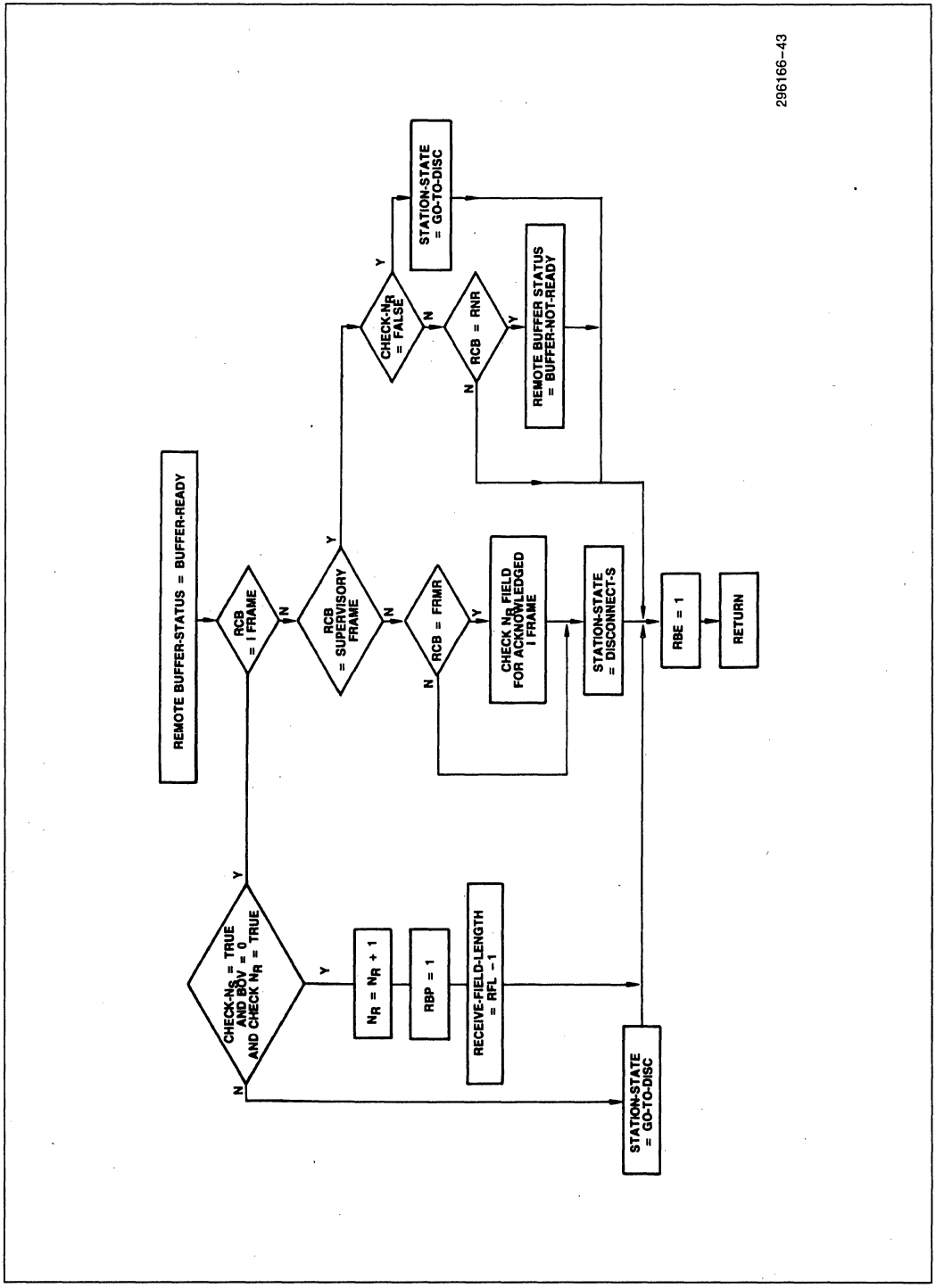

Figure 38. Primary Station Flow Charts

APPENDIX B
LISTINGS OF SOFTWARE MODULES

```
PL/M-51 COMPILER    RUPI-44 Secondary Station Driver                    20:24:47  09/20/83  PAGE   1

ISIS-II PL/M-51 V1.0
COMPILER INVOKED BY:   :F2:PLM51 :F2:APNOTE.SRC


                $TITLE      ('RUPI-44 Secondary Station Driver')
                $DEBUG
                $REGISTERBANK(1)
   1    1       MAIN$MOD:DO;
                $NOLIST

                /* To save paper the RUPI registers are not listed, but this is the statement
                   used to include them:  $INCLUDE (:F2:REG44.DCL) */

   5    1       DECLARE LIT             LITERALLY   'LITERALLY',
                        TRUE            LIT         '0FFH',
                        FALSE           LIT         '00H',
                        FOREVER         LIT         'WHILE 1';

                /* SDLC commands and responses */

   6    1       DECLARE SNRM            LIT         '93H',
                        UA              LIT         '73H',
                        DISC            LIT         '43H',
                        DM              LIT         '1FH',
                        FRMR            LIT         '97H',
                        REQ_DISC        LIT         '53H',
                        UP              LIT         '33H',
                        TEST            LIT         '0E3H',


                               /* User states */

                        OPEN_S            LIT         '00H',
                        CLOSED_S          LIT         '01H',

                               /* Station states */

                        DISCONNECT_S    LIT         '00H', /* LOGICALLY DISCONNECTED STATE*/
                        FRMR_S          LIT         '01H', /* FRAME REJECT STATE */
                        I_T_S           LIT         '02H', /* INFORMATION TRANSFER STATE */


                        /* Status values returned from TRANSMIT procedure */

                        USER_STATE_CLOSED   LIT     '00H',
                        LINK_DISCONNECTED   LIT     '01H',
                        OVERFLOW            LIT     '02H',
                        DATA_TRANSMITTED    LIT     '03H',

                        /* Parameters passed to XMIT_FRMR */

                        UNASSIGNED_C        LIT     '00H',
                        NO_I_FIELD_ALLOWED  LIT     '01H',
                        BUFF_OVERRUN        LIT     '02H',
                        SES_ERR             LIT     '03H',
```

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```
PL/M-51 COMPILER    RUPI-44 Secondary Station Driver                    20:24:47  09/20/83  PAGE  2

                        /* Variables */

                    USER_STATE          BYTE    AUXILIARY,
                    STATION_STATE       BYTE    AUXILIARY,
                    I_FRAME_LENGTH      BYTE    AUXILIARY,

                        /* Buffers */

                    BUFFER_LENGTH                       LIT     '60',
                    SIU_XMIT_BUFFER(BUFFER_LENGTH)      BYTE    PUBLIC    IDATA,
                    SIU_RECV_BUFFER(BUFFER_LENGTH)      BYTE    PUBLIC,
                    FRMR_BUFFER(3)          BYTE,

                        /* Flags */

                    XMIT_BUFFER_EMPTY       BIT PUBLIC;

  7   2     SIU_RECV: PROCEDURE (LENGTH) EXTERNAL;
  8   2         DECLARE LENGTH  BYTE;
  9   1     END SIU_RECV;

 10   2     OPEN: PROCEDURE PUBLIC USING 2;
 11   2         USER_STATE=OPEN_S;
 12   1     END OPEN;

 13   2     CLOSE: PROCEDURE PUBLIC USING 2;
 14   2         AM=0;
 15   2         USER_STATE=CLOSED_S;
 16   1     END CLOSE;

 17   2     POWER_ON_D: PROCEDURE   PUBLIC USING 0;

 18   2         USER_STATE=CLOSED_S;
 19   2         STATION_STATE=DISCONNECT_S;
 20   2         TBS=.SIU_XMIT_BUFFER(0);
 21   2         RBS=.SIU_RECV_BUFFER(0);
 22   2         RBL=BUFFER_LENGTH;
 23   2         RBE=1;      /* Enable the SIU's receiver */
 24   2         XMIT_BUFFER_EMPTY=1;

 25   1     END POWER_ON_D;

 26   2     TRANSMIT: PROCEDURE (XMIT_BUFFER_LENGTH) BYTE   PUBLIC USING 0;

           /* User must check XMIT_BUFFER_EMPTY flag before calling this procedure */

 27   2         DECLARE XMIT_BUFFER_LENGTH  BYTE,
                         I                  BYTE    AUXILIARY,
                         STATUS             BYTE    AUXILIARY;

 28   2         IF USER_STATE=CLOSED_S
                    THEN STATUS=USER_STATE_CLOSED;
 30   2         ELSE IF STATION_STATE=DISCONNECT_S
                    THEN STATUS=LINK_DISCONNECTED;
 32   2         ELSE IF XMIT_BUFFER_LENGTH>BUFFER_LENGTH
                    THEN STATUS=OVERFLOW;
 34   3         ELSE DO;
```

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```
PL/M-51 COMPILER    RUPI-44 Secondary Station Driver                    20:24:47  09/20/83  PAGE   3

  35   3                    XMIT_BUFFER_EMPTY=0;
  36   3                    TBL=XMIT_BUFFER_LENGTH;
  37   3                    I_FRAME_LENGTH=XMIT_BUFFER_LENGTH;  /* Store length in case station
                                                                   is reset by FRMR, SNRM etc. */
  38   3                    TBF=1;
  39   3                    STATUS=DATA_TRANSMITTED;
  40   3                  END;
  41   2              RETURN STATUS;
  42   1      END TRANSMIT;

  43   2      XMIT_UNNUMBERED: PROCEDURE (CONTROL_BYTE) ;

  44   2          DECLARE CONTROL_BYTE    BYTE;

  45   2              TCB=CONTROL_BYTE;
  46   2              TBF=1;
  47   2              RTS=1;
  48   3              DO WHILE NOT SI;
  49   3              END;
  50   2              SI=0;

  51   1      END XMIT_UNNUMBERED;

  52   2      SNRM_RESPONSE: PROCEDURE ;

  53   2          STATION_STATE=I_T_S;
  54   2          NSNR=0;
  55   2          IF (RCB AND 10H) <> 0 /* Respond if polled */
                     THEN DO;
  57   3                    TBL=0;
  58   3                    CALL XMIT_UNNUMBERED(UA);
  59   3                END;
  60   2          IF XMIT_BUFFER_EMPTY=0  /* If an I frame was left pending transmission
                                             then restore it */
              THEN DO;
  62   3                    TBL=I_FRAME_LENGTH;
  63   3                    TBF=1;
  64   3                END;
  65   2          AM=1;

  66   1      END SNRM_RESPONSE;

  67   2      XMIT_FRMR: PROCEDURE (REASON)  ;

  68   2              DECLARE REASON  BYTE;

  69   2              TCB=FRMR;

  70   2              TBS=.FRMR_BUFFER(0);
  71   2              TBL=3;
  72   2              FRMR_BUFFER(0)=RCB;
                      /* Swap nibbles in NSNR */
  73   2              FRMR_BUFFER(1)=(SHL((NSNR AND 0EH),4) OR  SHR((NSNR AND 0E0H),4));
  74   3              DO CASE REASON;
  75   3                  FRMR_BUFFER(2)=01H;   /* UNASSIGNED_C */
```

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```
PL/M-51 COMPILER    RUPI-44 Secondary Station Driver                    20:24:47  09/20/83  PAGE   4

  76   3                FRMR_BUFFER(2)=02H;   /* NO_I_FIELD_ALLOWED */
  77   3                FRMR_BUFFER(2)=04H;   /* BUFF_OVERRUN */
  78   3                FRMR_BUFFER(2)=08H;   /* SEQ_ERR */
  79   3             END;

  80   2            STATION_STATE=FRMR_S;

  81   2            IF (RCB AND 10H) <>0
                        THEN DO;
  83   3                        TBF=1;
  84   3                        RTS=1;
  85   4                        DO WHILE NOT SI;
  86   4                        END;
  87   3                        SI=0;
  88   3                     END;
  89   1      END XMIT_FRMR;


  90   2      IN_DISCONNECT_STATE: PROCEDURE ;/* Called from SIU_INT procedure */

  91   2             IF ((USER_STATE=OPEN_S) AND ((RCB AND OEFH)=SNRM))
                        THEN CALL SNRM_RESPONSE;

  93   2             ELSE IF (RCB AND 10H) <> 0
                          THEN DO;
  95   3                           TBL=0;
  96   3                           CALL XMIT_UNNUMBERED(DM);
  97   3                        END;
  98   1      END IN_DISCONNECT_STATE;


  99   2      IN_FRMR_STATE: PROCEDURE ; /* Called by SIU_INT when a frame has been received
                                           when in the FRMR state */

 100   2          IF (RCB AND OEFH)=SNRM
                     THEN DO;
 102   3                     CALL SNRM_RESPONSE;
 103   3                     TBS=.SIU_XMIT_BUFFER(0);  /* Restore transmit buffer start address */
 104   3                  END;


 105   2          ELSE IF (RCB AND OEFH)=DISC
                     THEN DO;
 107   3                     STATION_STATE=DISCONNECT_S;
 108   3                     TBS=.SIU_XMIT_BUFFER(0);   /* Restore transmit buffer start address */
 109   3                     IF (RCB AND 10H)<> 0
                               THEN DO;
 111   4                                TBL=0;
 112   4                                CALL XMIT_UNNUMBERED(UA);
 113   4                             END;
 114   3                  END;

 115   3          ELSE DO;       /* Receive control byte is something other than DISC or SNRM */
 116   3                  IF (RCB AND 10H) <> 0
                             THEN DO;
 118   4                                TBF=1;
 119   4                                RTS=1;
```

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```
PL/M-51 COMPILER    RUPI-44 Secondary Station Driver                    20:24:47  09/20/83  PAGE   5

 120   5                              DO WHILE NOT SI;
 121   5                              END;
 122   4                           END;
 123   3                 END;

 124   1       END IN_FRMR_STATE;

 125   2       COMMAND_DECODE: PROCEDURE ;


 126   2           IF (RCB AND OEFH)=SNRM
                     THEN  CALL SNRM_RESPONSE;

 128   2           ELSE IF (RCB AND OEFH)=DISC
                         THEN  DO;
 130   3                               STATION_STATE=DISCONNECT_S;
 131   3                               IF (RCB AND 10H)<>0
                                     THEN DO;
 133   4                                       TBL=0;
 134   4                                       CALL XMIT_UNNUMBERED(UA);
 135   4                                    END;
 136   3                          END;

 137   2           ELSE IF (RCB AND OEFH)=TEST
                         THEN DO;
 139   3                               IF (RCB AND 10H)>0  /* Respond if polled */
                                         THEN DO;     /* FOR BOV=1, SEND THE TEST RESPONSE WITHOUT AN I FIELD */
 141   4                                       IF (BOV=1)
                                                 THEN DO;
 143   5                                               TBL=0;
 144   5                                               CALL XMIT_UNNUMBERED(TEST OR 10H);
 145   5                                            END;
 146   5                                       ELSE DO; /* If no BOV, send received I field back to primary */
 147   5                                            TBL=RFL;
 148   5                                            TBS=RBS;
 149   5                                            CALL XMIT_UNNUMBERED(TEST OR 10H);
 150   5                                            TBS=.SIU_XMIT_BUFFER(0);  /* Restore TBS */
 151   5                                         END;

                                                 /* If an I frame was pending, set it up again */

 152   4                                       IF XMIT_BUFFER_EMPTY=0
                                                 THEN DO;
 154   5                                               TBL=I_FRAME_LENGTH;
 155   5                                               TBF=1;
 156   5                                            END;
 157   4                                    END;
 158   3                               AM=1;
 159   3                          END;

 160   2           ELSE IF (RCB AND 01H) = 0 /* Kicked out of the AUTO mode because
                                                an I frame was received while RPB = 1 */
                         THEN DO;
 162   3                               AM = 1;
 163   3                               IF XMIT_BUFFER_EMPTY = 1
                                           THEN TBL = 0;
 165   3                               TBF = 1;     /* Send an AUTO mode response */
```

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```
PL/M-51 COMPILER    RUPI-44 Secondary Station Driver                    20:24:47  09/20/83  PAGE   6

 166   3                        RTS = 1;
 167   3                    END;

 168   2          ELSE CALL XMIT_FRMR(UNASSIGNED_C);  /* Received an undefined or not implemented command */

 169   1      END COMMAND_DECODE;


 170   2      SIU_INT: PROCEDURE INTERRUPT 4;

 171   2              DECLARE     I   BYTE    AUXILIARY;

 172   2              SI=0;
 173   2              IF STATION_STATE<> I_T_S /* Must be in NON-AUTO mode */
                     THEN DO;
 175   3                          IF RBE=0 /* Received a frame?  Give response */
                                 THEN DO;
 177   3                                      DO CASE STATION_STATE;
 178   3                                          CALL IN_DISCONNECT_STATE;
 179   3                                          CALL IN_FRMR_STATE;
 180   3                                      END;
 181   4                                      RBE=1;
 182   4                                  END;
 183   3                      RETURN;
 184   3                      END;

                     /* If the program reaches this point, STATION_STATE=I_T_S
                         which means the SIU either was, or still is in the AUTO MODE */


 185   2              IF AM=0
                     THEN DO;
 187   3                          IF (RCB AND 0EFH)=DISC
                                 THEN CALL COMMAND_DECODE;
 189   3                          ELSE IF USER_STATE=CLOSED_S
                                 THEN DO;
 191   4                                      TBL=0;
 192   4                                      CALL XMIT_UNNUMBERED(REQ_DISC);
 193   4                                  END;
 194   3                          ELSE IF SES=1
                                 THEN CALL XMIT_FRMR(SES_ERR);
 196   3                          ELSE IF SOV=1
                                 THEN DO; /* DON'T SEND FRMR IF A TEST WAS RECEIVED*/
 198   4                                      IF (RCB AND 0EFH)=TEST
                                             THEN CALL COMMAND_DECODE;
 200   4                                      ELSE     CALL XMIT_FRMR(BUFF_OVERRUN);
 201   4                                  END;
 202   3                          ELSE CALL COMMAND_DECODE;
 203   3                          RBE=1;
 204   3                      END;

 205   3              ELSE DO; /* MUST STILL BE IN AUTO MODE */
 206   3                      IF TBF=0
                             THEN XMIT_BUFFER_EMPTY=1;  /* TRANSMITTED A FRAME */
 208   3                      IF RBE=0
                             THEN DO;
```

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```
PL/M-51 COMPILER    RUPI-44 Secondary Station Driver                    20:24:47  09/20/83  PAGE   7

 210   4                                  RBP=1; /* RNR STATE */
 211   4                                  RBE=1; /* RE-ENABLE RECEIVER */
 212   4                                  CALL SIU_RECV(RFL);
 213   4                                  RBP=0; /* RR STATE */
 214   4                              END;
 215   3                      END;
 216   1      END SIU_INT;

 217   1      END MAIN#MOD;

Software and application note written by Charles Yager


WARNING8:
    4 IS THE HIGHEST USED INTERRUPT


MODULE INFORMATION:                 (STATIC+OVERLAYABLE)
    CODE SIZE                       = 028FH         655D
    CONSTANT SIZE                   = 0000H           0D
    DIRECT VARIABLE SIZE            =   3FH+02H      63D+   2D
    INDIRECT VARIABLE SIZE          =   3CH+00H      60D+   0D
    BIT SIZE                        =   01H+00H       1D+   0D
    BIT-ADDRESSABLE SIZE            =   00H+00H       0D+   0D
    AUXILIARY VARIABLE SIZE         = 0006H           6D
    MAXIMUM STACK SIZE              = 0017H          23D
    REGISTER-BANK(S) USED:            0 1 2
    460 LINES READ
    0 PROGRAM ERROR(S)
END OF PL/M-51 COMPILATION
```

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```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                    18:50:53  09/19/83  PAGE   1


ISIS-II PL/M-51 V1.0
COMPILER INVOKED BY:   :f2:plm51 :f2:unote.src


             $TITLE      ('Application Module: Async/SDLC Protocol converter')
             $debug
             $registerbank(0)
   1    1    user$mod:do;
             $NOLIST
   5    1    DECLARE     LIT                 LITERALLY       'LITERALLY',
                         TRUE                LIT             'OFFH',
                         FALSE               LIT             '00H',
                         FOREVER             LIT             'WHILE 1',
                         ESC                 LIT             '1BH',
                         LF                  LIT             '0AH',
                         CR                  LIT             '0DH',
                         BS                  LIT             '08H',
                         BEL                 LIT             '07H',
                         EMPTY               LIT             '00H',
                         INUSE               LIT             '01H',
                         FULL                LIT             '02H',
                         USER_STATE_CLOSED   LIT             '00H',
                         LINK_DISCONNECTED   LIT             '01H',
                         OVERFLOW            LIT             '02H',
                         DATA_TRANSMITTED    LIT             '03H',

                             /* BUFFERS */

                         BUFFER_LENGTH       LIT             '60',
                         SIU_XMIT_BUFFER(BUFFER_LENGTH)      BYTE    EXTERNAL    IDATA,
                         SIU_RECV_BUFFER(BUFFER_LENGTH)      BYTE    EXTERNAL,
                         FIFO_T(256)             BYTE    AUXILIARY,
                         IN_PTR_T                BYTE    AUXILIARY,
                         OUT_PTR_T               BYTE    AUXILIARY,
                         BUFFER_STATUS_T         BYTE    AUXILIARY,
                         FIFO_R(256)             BYTE    AUXILIARY,
                         IN_PTR_R                BYTE    AUXILIARY,
                         OUT_PTR_R               BYTE    AUXILIARY,
                         BUFFER_STATUS_R         BYTE    AUXILIARY,

                             /* Variables and Parameters */

                         LENGTH                  BYTE    AUXILIARY,
                         CHAR                    BYTE    AUXILIARY,
                         I                       BYTE    AUXILIARY,
                         USART_CMD               BYTE    AUXILIARY,
                         DESTINATION_ADDRESS     BYTE    AUXILIARY,
                         SEND_DATA               BYTE    AUXILIARY,
                         RESULT                  BYTE    AUXILIARY,
                         ERR_MESSAGE_INDEX       BYTE    AUXILIARY,
                         ERR_MESSAGE_PTR         WORD    AUXILIARY,

                           /*   Messages Sent to the Terminal   */

                         PARITY(*) BYTE CONSTANT(LF,CR,'Parity Error Detected',LF,CR,00H),
                         FRAME(*) BYTE CONSTANT(LF,CR,'Framing Error Detected',LF,CR,00H),
```

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```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter          18:50:53  09/19/83  PAGE   2

        OVER_RUN(*) BYTE CONSTANT(LF,CR,'Overrun Error Detected',LF,CR,0),
        LINK(*) BYTE CONSTANT(LF,CR,'Unable to Get Online',LF,CR,00H),
        DEST_ADDR(*) BYTE CONSTANT(CR,LF,LF,
                'Enter the destination address: __', BS, BS, 0),

        D_ADDR_ACK(*) BYTE CONSTANT(CR,LF,LF,
                'The new destination address is ',0),

        STAT_ADDR(*) BYTE CONSTANT(CR,LF,LF,
                'Enter the station address: __',BS,BS,0),

        S_ADDR_ACK(*) BYTE CONSTANT(CR,LF,LF,
                'The new station address is ',0),

        ADDR_ACK_FIN(*) BYTE CONSTANT('H',CR,LF,LF,0),



        SIGN_ON(*)  BYTE CONSTANT(CR, LF,LF,
        '(\/)  RUPI-44 Secondary Station', CR, LF,
        ' \/', CR, LF, LF,
        '1 - Set the Station Address',LF,CR,
        '2 - Set the Destination Address',CR,LF,
        '3 - Go Online',CR,LF,
        '4 - Go Offline',CR,LF,
        '5 - Return to terminal mode',CR,LF,LF,
        '    Enter option: _', BS, 0),

        FIN(*)  BYTE CONSTANT(CR,LF,LF,0),


        /* Characters Received From the Terminal */

        HEX_TABLE(17) BYTE CONSTANT('0123456789ABCDEF',BEL),
        MENU_CHAR(6) BYTE CONSTANT('12345',BEL),

          /* Flags and Bits */

        XMIT_BUFFER_EMPTY       BIT     EXTERNAL, /* Semaphore  for RUPI SIOU Transmit Buffer */
        STOP_BIT                BIT     AT(147) REG, /* Terminal parameters */
        ECHO                    BIT     AT(0B4H) REG,
        WAIT                    BIT,            /* Timeout flag */
        ERROR_FLAG              BIT,            /* Error message Flag */

          /* Peripheral Addresses */

        UBART_STATUS            BYTE    AT(0801H) AUXILIARY,
        UBART_DATA              BYTE    AT(0800H) AUXILIARY,
        TIMER_CONTROL           BYTE    AT(1003H) AUXILIARY,
        TIMER_0                 BYTE    AT(1000H) AUXILIARY,
        TIMER_1                 BYTE    AT(1001H) AUXILIARY,
        TIMER_2                 BYTE    AT(1002H) AUXILIARY;


           /* External Procedures */
```

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```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                18:50:53  09/19/83  PAGE   3


   6   2      POWER_ON_D: PROCEDURE   EXTERNAL;
   7   1      END POWER_ON_D;

   8   2      CLOSE: PROCEDURE EXTERNAL USING 2;
   9   1      END CLOSE;

  10   2      OPEN: PROCEDURE EXTERNAL USING 2;
  11   1      END OPEN;

  12   2      TRANSMIT:   PROCEDURE   (XMIT_BUFFER_LENGTH)    BYTE    EXTERNAL;
  13   2                  DECLARE XMIT_BUFFER_LENGTH  BYTE;
  14   1      END TRANSMIT;

                          /* Local Procedures */

  15   2      TIMER_0_INT: PROCEDURE INTERRUPT 1 USING 1;
  16   2          WAIT=0;
  17   1      END TIMER_0_INT;

  18   2      POWER_ON:   PROCEDURE USING 0;

  19   2              DECLARE TEMP    BYTE    AUXILIARY;

  20   2              SMD=54H;                /* Using DPLL, NRZI, PFS, TIMER 1, @ 62.5 Kbps */
  21   2              TMOD=21H;               /* Timer 0 16 bit, Timer 1 auto reload */
  22   2              TH1=0FFH;
  23   2              TCON=40H;

  24   2              TIMER_CONTROL=37H;   /* Initialize USART's system clock: 8254 */
  25   2              TIMER_0=04H;
  26   2              TIMER_0=00H;
  27   2              TIMER_CONTROL=77H;  /* Initialize TxC, RxC  */

              /*        Definition for dip switch tied to P1.0 to P1.6

                        Bit Rate    3       2       1
                       ---------------------------------
                          300       on      on      on
                         1200       on      on      off
                         2400       on      off     on
                         4800       on      off     off
                         9600       off     on      on
                        19200       off     on      off

                        Stop bit     4
                       ------------------
                            1        on
                            2        off

                        Parity      6       5
                       ---------------------------
                        off         on      on
                        odd         on      off
                        off         off     on
                        even        off     off
```

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```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                18:50:53  09/19/83  PAGE   4


                        Echo        7
                        ____________
                        on          on
                        off         off                 */

  28   2              TEMP=P1 AND 07H;  /* Read the dip switch to determine the bit rate */
  29   2              IF TEMP>5
                         THEN TEMP=0;
  31   3              DO CASE TEMP;
            /* 300 */
  32   4                  DO;
  33   4                      TIMER_1=83H;
  34   4                      TIMER_1=20H;
  35   4                  END;

  36   4        /* 1200 */  DO;
  37   4                      TIMER_1=20H;
  38   4                      TIMER_1=05H;
  39   4                  END;

  40   4        /* 2400 */  DO;
  41   4                      TIMER_1=60H;
  42   4                      TIMER_1=02H;
  43   4                  END;

  44   4        /* 4800 */  DO;
  45   4                      TIMER_1=30H;
  46   4                      TIMER_1=01H;
  47   4                  END;

  48   4        /* 9600 */  DO;
  49   4                      TIMER_1=65H;
  50   4                      TIMER_1=0;
  51   4                  END;

  52   4        /* 19200 */ DO;
  53   4                      TIMER_1=33H;
  54   4                      TIMER_1=0;
  55   4                  END;
  56   3              END;

  57   2              USART_STATUS=0;   /* Software power-on reset for 8251A */
  58   2              USART_STATUS=0;
  59   2              USART_STATUS=0;
  60   2              USART_STATUS=40H;

  61   2              TEMP=0AH;         /* Determine the parity and # of stop bits */
  62   2              TEMP=TEMP OR (P1 AND 30H);
  63   2              IF STOP_BIT=1
                         THEN TEMP=TEMP OR 0C0H;
  65   2              ELSE TEMP=TEMP OR 40H;

  66   2              USART_STATUS=TEMP;  /* USART Mode Word */
  67   2              USART_STATUS, USART_CMD=27H; /*USART Command Word RTS, RxE, DTR, TxEN=1*/

  68   2              STAD=0FFH;
```

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12

```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                    18:50:53  09/19/83  PAGE   5


  69   2              SEND_DATA=0; /* Intialize Flags */
  70   2             IN_PTR_T, OUT_PTR_T, IN_PTR_R, OUT_PTR_R = 0;/*Initialize FIFO PTRs*/
  71   2              BUFFER_STATUS_T, BUFFER_STATUS_R= EMPTY;
  72   2              CALL POWER_ON_D;
  73   2              IP=01H;           /* USART's RxRdy is the highest priority */
                                        /* Both external interrupts are level triggered*/
  74   2              IE=93H;           /* Enable USART RxRdy, SI, and Timer 0 interrupts*/
  75   2              ERROR_FLAG=0;
  76   1      END POWER_ON;

  77   2      FIFO_R_IN: PROCEDURE (CHAR) USING 1;
  78   2          DECLARE CHAR    BYTE;

  79   2          FIFO_R(IN_PTR_R)=CHAR;
  80   2          IN_PTR_R=IN_PTR_R+1;

  81   2          IF BUFFER_STATUS_R=EMPTY
                      THEN DO;
  83   3                       EA=0;
  84   3                       BUFFER_STATUS_R=INUSE;
  85   3                       EX1=1;       /* Enable USART's TxD interrupt */
  86   3                       EA=1;
  87   3                   END;
  88   2          ELSE IF ((BUFFER_STATUS_R=INUSE) AND (IN_PTR_R=OUT_PTR_R))
                       THEN BUFFER_STATUS_R=FULL;

  90   1      END FIFO_R_IN;

  91   2      FIFO_R_OUT: PROCEDURE BYTE USING 1;

  92   2          DECLARE CHAR    BYTE    AUXILIARY;

  93   2          CHAR=FIFO_R(OUT_PTR_R);
  94   2          OUT_PTR_R=OUT_PTR_R+1;
  95   2          IF OUT_PTR_R=IN_PTR_R
                      THEN DO;
  97   3                       EX1=0;  /* Shut off TxD interrupt */
  98   3                       BUFFER_STATUS_R=EMPTY;
  99   3                   END;
 100   2          ELSE IF ((BUFFER_STATUS_R=FULL) AND (OUT_PTR_R-20=IN_PTR_R))
                       THEN BUFFER_STATUS_R=INUSE;

 102   2          RETURN CHAR;

 103   1      END FIFO_R_OUT;


 104   2      USART_XMIT_INT: PROCEDURE INTERRUPT 2 USING 1;
```

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```
PL/M-51 COMPILER    Application Module: Async/BDLC Protocol converter                    18:50:53  09/19/83  PAGE   6

 105   2          DECLARE
                        MESSAGE BASED ERR_MESSAGE_PTR(1)    BYTE    CONSTANT;

 106   2          IF ERROR_FLAG
                   THEN DO;
 108   3                  IF MESSAGE(ERR_MESSAGE_INDEX)<>0  /* Then continue to send the message */
 110   4                     THEN DO;
 111   4                             USART_DATA = MESSAGE(ERR_MESSAGE_INDEX);
 112   4                             ERR_MESSAGE_INDEX=ERR_MESSAGE_INDEX+1;
                                  END;

 113   4                     ELSE DO; /* If message is done reset ERROR_FLAG and shut off interrupt if FIFO is empty */
 114   4                             ERROR_FLAG=0;
 115   4                             IF BUFFER_STATUS_R = EMPTY
                                        THEN EX1=0;
 117   4                           END;
 118   3                 END;

 119   2          ELSE USART_DATA=FIFO_R_OUT;

 120   1      END USART_XMIT_INT;


 121   2      SIU_RECV: PROCEDURE (LENGTH) PUBLIC USING 1;

 122   2          DECLARE LENGTH  BYTE,
                         I       BYTE    AUXILIARY;

 123   3          DO I=0 TO LENGTH-1;
 124   4             DO WHILE BUFFER_STATUS_R=FULL; /* Check to see if fifo is full */
 125   4             END;
 126   3             CALL FIFO_R_IN(SIU_RECV_BUFFER(I));
 127   3          END;

 128   1      END SIU_RECV;


 129   2      FIFO_T_IN: PROCEDURE (CHAR) USING 2;

 130   2          DECLARE CHAR         BYTE;

 131   2          FIFO_T(IN_PTR_T)=CHAR;
 132   2          IN_PTR_T=IN_PTR_T+1;
 133   2          IF CHAR=LF
                   THEN SEND_DATA=SEND_DATA+1;

 135   2          IF BUFFER_STATUS_T=EMPTY
                   THEN BUFFER_STATUS_T=INUSE;
 137   2          ELSE IF ((BUFFER_STATUS_T=INUSE) AND (IN_PTR_T+20=OUT_PTR_T))
                        THEN DO; /* Stop reception using CTS */
 139   3                          USART_STATUS, USART_CMD=USART_CMD AND NOT(20H);
 140   3                          BUFFER_STATUS_T=FULL;
 141   3                          IF SEND_DATA=0
                                     THEN SEND_DATA=1;/*If the buffer is full and no LF
                                                        has been received then send data */
 143   3                        END;
 144   1      END FIFO_T_IN;
```

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```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                    18:50:53  09/19/83  PAGE   7


 145   2      FIFO_T_OUT: PROCEDURE BYTE ;

 146   2          DECLARE CHAR     BYTE    AUXILIARY;

 147   2          CHAR=FIFO_T(OUT_PTR_T);
 148   2          OUT_PTR_T=OUT_PTR_T+1;
 149   2          IF OUT_PTR_T=IN_PTR_T   /* Then FIFO_T is empty */
                     THEN DO;
 151   3                  EA=0;
 152   3                  BUFFER_STATUS_T=EMPTY;
 153   3                  SEND_DATA=0;
 154   3                  EA=1;
 155   3                END;
 156   2          ELSE IF ((BUFFER_STATUS_T=FULL) AND (OUT_PTR_T-80=IN_PTR_T))
                        THEN DO;
 158   3                       USART_STATUS, USART_CMD=USART_CMD OR 20H;
 159   3                       BUFFER_STATUS_T=INUSE;
 160   3                     END;
 161   2          IF (CHAR=LF AND SEND_DATA>0) THEN SEND_DATA=SEND_DATA-1;
 163   2          RETURN CHAR;
 164   1      END FIFO_T_OUT;

 165   2      ERROR: PROCEDURE (STATUS) USING 2;

 166   2              DECLARE STATUS      BYTE;

 167   2              IF (STATUS AND 08H)<>0
                         THEN ERR_MESSAGE_PTR=.PARITY;
 169   2              ELSE IF (STATUS AND 10H)<>0
                         THEN ERR_MESSAGE_PTR=.OVER_RUN;
 171   2              ELSE IF (STATUS AND 20H)<>0
                         THEN ERR_MESSAGE_PTR=.FRAME;

 173   2              USART_STATUS=(USART_CMD OR 10H); /* Reset error flags on USART */

 174   2              ERR_MESSAGE_INDEX = 0;
 175   2              ERROR_FLAG=1;
 176   2              EX1=1;              /* Turn on Tx Interrupt */

 177   1      END ERROR;

 178   2      LINK_DISC: PROCEDURE ;

              /* This procedure sends the message 'Unable to Get Online' to the terminal */

 179   2          DECLARE MESSAGE_PTR WORD    AUXILIARY,
                         MESSAGE     BASED   MESSAGE_PTR(1)      BYTE    CONSTANT,
                         J           BYTE    AUXILIARY,
                         EX1_STORE   BIT;


 180   2          EX1_STORE=EX1;     /* Shut off async transmit interrupt */
 181   2          EX1=0;
 182   2          MESSAGE_PTR=.LINK;
 183   2          J=0;
 184   3          DO WHILE (MESSAGE(J)<>0);
```

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```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                    18:50:53  09/19/83  PAGE   8

 185   4              DO WHILE (USART_STATUS AND 01H)=0;  /* Wait for TxRDY on USART */
 186   4              END;
 187   3              USART_DATA=MESSAGE(J);
 188   3              J=J+1;
 189   3          END;
 190   2          EX1=EX1_STORE;    /* Restore async transmit interrupt */
 191   1      END LINK_DISC;


 192   2      CO: PROCEDURE (CHAR) USING 2;
 193   2              DECLARE CHAR    BYTE;

 194   3              DO WHILE (USART_STATUS AND 01H) = 0;
 195   3              END;
 196   2              USART_DATA=CHAR;

 197   1      END CO;

 198   2      CI: PROCEDURE BYTE USING 2;

 199   3          DO WHILE (USART_STATUS AND 02H) = 0;
 200   3          END;
 201   2          RETURN USART_DATA;

 202   1      END CI;


 203   2      GET_HEX: PROCEDURE BYTE USING 2;

 204   2          DECLARE CHAR    BYTE    AUXILIARY,
                         I       BYTE    AUXILIARY;

 205   2          LO: CHAR=CI;

 206   3              DO I=0 TO 15;
 207   3                  IF CHAR=HEX_TABLE(I)
                             THEN GOTO L1;
 209   3              END;

 210   2          L1: CALL CO(HEX_TABLE(I));
 211   2              IF I=16
                         THEN GOTO LO;

 213   2              RETURN I;

 214   1      END GET_HEX;

 215   2      OUTPUT_MESSAGE: PROCEDURE (MESSAGE_PTR) USING 2;
 216   2          DECLARE MESSAGE_PTR WORD,
                         MESSAGE     BASED   MESSAGE_PTR(1)  BYTE CONSTANT,
                         I           BYTE    AUXILIARY;

 217   2          I=0;

 218   3          DO WHILE MESSAGE(I) <> 0;
 219   3              CALL CO(MESSAGE(I));
 220   3              I=I+1;
```

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```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                18:50:53  09/19/83  PAGE   9

221   3           END;

222   1       END OUTPUT_MESSAGE;


223   2       MENU: PROCEDURE USING 2;

224   2           DECLARE I                BYTE    AUXILIARY,
                      CHAR               BYTE    AUXILIARY,
                      STATION_ADDRESS    BYTE    AUXILIARY;


225   2       START:
                  CALL OUTPUT_MESSAGE(.SIGN_ON);

226   2           M0: CHAR=CI;     /* Read a character */

227   3               DO I=0 TO 4;
228   3                   IF CHAR=MENU_CHAR(I)
                            THEN GOTO M1;
230   3               END;

231   2           M1: CALL CO(MENU_CHAR(I));
232   2               IF I=5
                        THEN GOTO M0;

234   3           DO CASE I;

235   4               DO;
236   4                   CALL OUTPUT_MESSAGE(.STAT_ADDR);

237   4                   STATION_ADDRESS=SHL(GET_HEX,4);

238   4                   STATION_ADDRESS=(STATION_ADDRESS OR GET_HEX);

239   4                   STAD=STATION_ADDRESS;

240   4                   CALL OUTPUT_MESSAGE(.S_ADDR_ACK);

241   4                   CALL CO(HEX_TABLE(SHR(STATION_ADDRESS,4)));
242   4                   CALL CO(HEX_TABLE(0FH AND STATION_ADDRESS));

243   4                   CALL OUTPUT_MESSAGE(.ADDR_ACK_FIN);
244   4               END;

245   4               DO;

246   4                   CALL OUTPUT_MESSAGE(.DEST_ADDR);

247   4                   DESTINATION_ADDRESS=SHL(GET_HEX,4);

248   4                   DESTINATION_ADDRESS=(DESTINATION_ADDRESS OR GET_HEX );

249   4                   CALL OUTPUT_MESSAGE(.D_ADDR_ACK);
```

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```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                    18:50:53  09/19/83  PAGE  10

 250   4                  CALL CO(HEX_TABLE(SHR(DESTINATION_ADDRESS,4)));
 251   4                  CALL CO(HEX_TABLE(OFH AND DESTINATION_ADDRESS));

 252   4                  CALL OUTPUT_MESSAGE(.ADDR_ACK_FIN);
 253   4              END;

 254   4              DO;
 255   4                  CALL OUTPUT_MESSAGE(.FIN);
 256   4                  CALL OPEN;
 257   4              END;


 258   4              DO;
 259   4                  CALL OUTPUT_MESSAGE(.FIN);
 260   4                  CALL CLOSE;
 261   4              END;

 262   3              CALL OUTPUT_MESSAGE(.FIN);

 263   3          END; /* DO CASE */

 264   1      END MENU;


 265   2      USART_RECV_INT: PROCEDURE INTERRUPT 0 USING 2;

 266   2          DECLARE CHAR        BYTE    AUXILIARY,
                         STATUS      BYTE    AUXILIARY;


 267   2          CHAR=USART_DATA;
 268   2          STATUS=USART_STATUS AND 38H;
 269   2          IF STATUS<>0
                     THEN CALL ERROR(STATUS);
 271   2          ELSE IF CHAR=ESC
                         THEN CALL MENU;
 273   3          ELSE DO;
 274   3                  CALL FIFO_T_IN(CHAR);
 275   3                  IF ECHO=0
                             THEN CALL CO(CHAR);
 277   3               END;

 278   1      END USART_RECV_INT;


 279   1      BEGIN:
              CALL POWER_ON;

 280   2          DO FOREVER;
 281   2              IF SEND_DATA>0
                         THEN DO;
 283   4                          DO WHILE NOT(XMIT_BUFFER_EMPTY); /*Wait until SIU_XMIT_BUFFer
                                                                     is empty */
 284   4                          END;
 285   3                          LENGTH, CHAR =1;
 286   3                          SIU_XMIT_BUFFER(0)=DESTINATION_ADDRESS;
 287   4                          DO WHILE ((CHAR<>LF) AND (LENGTH<BUFFER_LENGTH) AND (BUFFER_STATUS_T<>EMPTY));
```

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12

```
PL/M-51 COMPILER    Application Module: Async/SDLC Protocol converter                18:50:53  09/19/83  PAGE  11

 288   4                              CHAR=FIFO_T_OUT;
 289   4                              SIU_XMIT_BUFFER(LENGTH)=CHAR;
 290   4                              LENGTH=LENGTH+1;
 291   4                         END;

            /* If the line entered at the terminal is greater than BUFFER_LENGTH char, send the
               first BUFFER_LENGTH char; then send the rest; since the SIU buffer is only BUFFER_LENGTH bytes */
 292   3      L1:                 I=0; /* Use I to count the number of unsuccesful
                                        transmits */

 293   3      RETRY:         RESULT=TRANSMIT(LENGTH); /* Send the message */
 294   3                         IF RESULT<>DATA_TRANSMITTED
                                    THEN DO;
                               /* Wait 50 msec for link to connect then try again */
 296   4                                 WAIT=1;
 297   4                                 TH0=3CH;
 298   4                                 TL0=0AFH;
 299   4                                 TR0=1;
 300   5                                 DO WHILE WAIT;
 301   5                                 END;
 302   4                                 TR0=0;
 303   4                                 I=I+1;
 304   5                                 IF I>100 THEN DO;  /* Wait 5 sec to get on line else
                                                             send error message to terminal
                                                             and try again  */
 306   5                                                       CALL LINK_DISC;
 307   5                                                       GOTO L1;
 308   5                                                    END;
 309   4                                 GOTO RETRY;
 310   4                              END;
 311   3                         END;

 312   2          END;
 313   1      END USER$MOD;



WARNINGS:
    2 IS THE HIGHEST USED INTERRUPT


MODULE INFORMATION:                (STATIC+OVERLAYABLE)
    CODE SIZE                      = 0682H       1714D
    CONSTANT SIZE                  = 01CFH        463D
    DIRECT VARIABLE SIZE           =   00H+05H      0D+  5D
    INDIRECT VARIABLE SIZE         =   00H+00H      0D+  0D
    BIT SIZE                       =   02H+01H      2D+  1D
    BIT-ADDRESSABLE SIZE           =   00H+00H      0D+  0D
    AUXILIARY VARIABLE SIZE        = 021FH        543D
    MAXIMUM STACK SIZE             = 0028H         40D
    REGISTER-BANK(S) USED:           0 1 2
    713 LINES READ
    0 PROGRAM ERROR(S)
END OF PL/M-51 COMPILATION
```

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```
PL/M-51 COMPILER    RUPI-44 Primary Station                    20:47:13  09/26/83  PAGE   1

ISIS-II PL/M-51 V1.0
COMPILER INVOKED BY:   :F2:PLM51 :F2:PNOTE.SRC


                $TITLE      ('RUPI-44 Primary Station')
                $DEBUG
                $REGISTERBANK(0)
  1   1         MAIN$MOD:DO;

                /* To save paper the RUPI registers are not listed, but this is the statement
                   used to include them:  $INCLUDE (:F2:REG44.DCL) */

                $NOLIST

  5   1         DECLARE LIT             LITERALLY   'LITERALLY',
                        TRUE            LIT         '0FFH',
                        FALSE           LIT         '00H',
                        FOREVER         LIT         'WHILE 1';

                /* SDLC COMMANDS AND RESPONSES */

  6   1         DECLARE SNRM            LIT         '93H',
                        UA              LIT         '73H',
                        DISC            LIT         '53H',
                        DM              LIT         '1FH',
                        FRMR            LIT         '97H',
                        REQ_DISC        LIT         '53H',
                        UP              LIT         '33H',
                        TEST            LIT         '0F3H',
                        RR              LIT         '11H',
                        RNR             LIT         '15H',


                              /* REMOTE STATION BUFFER STATUS */

                        BUFFER_READY        LIT         '0',
                        BUFFER_NOT_READY    LIT         '1',

                              /* STATION STATES */
                        DISCONNECT_S    LIT         '00H', /* LOGICALLY DISCONNECTED STATE*/
                        GO_TO_DISC      LIT         '01H',
                        I_T_S           LIT         '02H', /* INFORMATION TRANSFER STATE */


                        /* PARAMETERS PASSED TO XMIT_I_T_S */
                        T_I_FRAME           LIT     '00H',
                        T_RR                LIT     '01H',
                        T_RNR               LIT     '02H',


                        /* SECONDARY STATION IDENTIFICATION */

                        NUMBER_OF_STATIONS  LIT     '2',
                        SECONDARY_ADDRESSES(NUMBER_OF_STATIONS)
                                            BYTE    CONSTANT(55H,43H),
```

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```
PL/M-51 COMPILER    RUPI-44 Primary Station                    20:47:13  09/26/83  PAGE   2


                        /* Remote Station Database */

                    RSD(NUMBER_OF_STATIONS) STRUCTURE
                    (STATION_ADDRESS     BYTE,
                     STATION_STATE       BYTE,
                     NS                  BYTE,
                     NR                  BYTE,
                     BUFFER_STATUS       BYTE,  /* The status of the secondary stations buffer */
                     INFO_LENGTH         BYTE,
                     DATA(64)            BYTE)   AUXILIARY,


                        /* VARIABLES */
                    STATION_NUMBER       BYTE    AUXILIARY,
                    RECV_FIELD_LENGTH    BYTE    AUXILIARY,
                    WAIT                 BIT;

                        /* BUFFERS */
                    SIU_XMIT_BUFFER(64)      BYTE    IDATA,
                    SIU_RECV_BUFFER(64)      BYTE;


  7   2     POWER_ON: PROCEDURE ;

  8   2         DECLARE I   BYTE    AUXILIARY;

  9   2             TBS=.SIU_XMIT_BUFFER(0);
 10   2             RBS=.SIU_RECV_BUFFER(0);
 11   2             RBL=64;       /* 64 Byte receive buffer */
 12   2             RBE=1;        /* Enable the SIU's receiver */

 13   3             DO I= 0 TO NUMBER_OF_STATIONS-1;

 14   3                 RSD(I).STATION_ADDRESS=SECONDARY_ADDRESSES(I);
 15   3                 RSD(I).STATION_STATE=DISCONNECT_S;
 16   3                 RSD(I).BUFFER_STATUS=BUFFER_NOT_READY;
 17   3                 RSD(I).INFO_LENGTH=0;

 18   3             END;

 19   2             SMD=54H; /* Using DPLL, NRZI, PFS, TIMER 1, @ 62.5 Kbps */
 20   2             TMOD=21H;
 21   2             TH1=0FFH;
 22   2             TCON=40H; /* Use timer 0 for receive time out interrupt */
 23   2             IE=82H;

 24   1     END POWER_ON;

 25   2     XMIT: PROCEDURE (CONTROL_BYTE);

 26   2         DECLARE CONTROL_BYTE    BYTE;

 27   2             TCB=CONTROL_BYTE;
 28   2             TBF=1;
```

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```
PL/M-51 COMPILER    RUPI-44 Primary Station                    20:47:13  09/26/83  PAGE   3

  29   2              RTS=1;
  30   3              DO WHILE NOT SI;
  31   3              END;
  32   2              SI=0;

  33   1      END XMIT;


  34   2      TIMER_0_INT: PROCEDURE INTERRUPT 1  USING 1;
  35   2          WAIT=0;
  36   1      END TIMER_0_INT;


  37   2      TIME_OUT: PROCEDURE BYTE;          /* Time_out returns true if there wasn't
                                                    a frame received within 200 msec.
                                                    If there was a frame received within
                                                    200 msec then time_out returns false. */
  38   2          DECLARE     I   BYTE    AUXILIARY;

  39   3          DO I=0 TO 3;

  40   3              WAIT=1;
  41   3              TH0=3CH;
  42   3              TL0=0AFH;
  43   3              TR0=1;
  44   4                  DO WHILE WAIT;
  45   4                      IF SI=1
                                 THEN GOTO T_01;
  47   4                  END;
  48   3          END;

  49   2          RETURN TRUE;

  50   2      T_01:
                  SI=0;
  51   2              RETURN FALSE;

  52   1      END TIME_OUT;

  53   2      SEND_DISC: PROCEDURE;

  54   2                  TBL=0;
  55   2                  CALL XMIT(DISC);
  56   2                  IF TIME_OUT=FALSE
                              THEN IF RCB=UA OR RCB=DM
  57   3                                 THEN DO;
  59   3                                         RSD(STATION_NUMBER).BUFFER_STATUS=BUFFER_NOT_READY;
  60   3                                         RSD(STATION_NUMBER).STATION_STATE=DISCONNECT_S;
  61   3                                     END;
  62   2                  RBE=1;

  63   1      END SEND_DISC;


  64   2      SEND_SNRM: PROCEDURE;

  65   2          TBL=0;
```

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```
PL/M-51 COMPILER    RUPI-44 Primary Station                                  20:47:13  09/26/83  PAGE   4

  66   2          CALL XMIT(SNRM);
  67   2          IF (TIME_OUT=FALSE) AND (RCB=UA)
                        THEN DO;
  69   3                          RSD(STATION_NUMBER).STATION_STATE=I_T_S;
  70   3                          RSD(STATION_NUMBER).NS=0;
  71   3                          RSD(STATION_NUMBER).NR=0;
  72   3                       END;
  73   2          RBE=1;

  74   1      END SEND_SNRM;


  75   2      CHECK_NS: PROCEDURE BYTE;

               /* Check the Ns Field of the received frame.  If Nr(P)=Ns(S) return true */

  76   2          IF (RSD(STATION_NUMBER).NR=(SHR(RCB,1) AND 07H))
                  THEN RETURN TRUE;
  78   2              ELSE RETURN FALSE;

  79   1      END CHECK_NS;

  80   2      CHECK_NR: PROCEDURE BYTE;

              /* Check the Nr field of the received frame.  If Ns(P)+1=Nr(S) then the frame
                  has been acknowledged, else if Ns(P)=Nr(S) then the frame has not been
                  acknowledged, else reset the secondary */

  81   2          IF (((RSD(STATION_NUMBER).NS + 1) AND 07H) = SHR(RCB,5))
                      THEN DO;
  83   3                      RSD(STATION_NUMBER).NS=((RSD(STATION_NUMBER).NS+1) AND 07H);
  84   3                      RSD(STATION_NUMBER).INFO_LENGTH=0;
  85   3                   END;
  86   2          ELSE IF (RSD(STATION_NUMBER).NS <> SHR(RCB,5))
                       THEN RETURN FALSE;

  88   2          RETURN TRUE;

  89   1      END CHECK_NR;


  90   2      RECEIVE: PROCEDURE ;

  91   2              DECLARE     I   BYTE    AUXILIARY;

  92   2              RSD(STATION_NUMBER).BUFFER_STATUS=BUFFER_READY;

               /* If an RNR was received buffer_status will be changed in the supervisory
                  frame decode section futher down in this procedure, any other response
                  means the remote stations buffer is ready  */

  93   2              IF (RCB AND 01H)=0
                      THEN DO;   /* I Frame Received */
  95   3                       IF (CHECK_NS=TRUE AND BOV=0 AND CHECK_NR=TRUE)
                               THEN DO;
  97   4                                   RSD(STATION_NUMBER).NR=((RSD(STATION_NUMBER).NR+1) AND 07H);
  98   4                                   RBP=1;
```

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```
PL/M-51 COMPILER    RUPI-44 Primary Station                                    20:47:13  09/26/83  PAGE   5

 99   4                                    RECV_FIELD_LENGTH=RFL-1;
100   4                                END;

101   3                             ELSE RSD(STATION_NUMBER).STATION_STATE=GO_TO_DISC;
102   3                          END;
103   2                  ELSE IF (RCB AND 03H)=01H
                             THEN DO;  /* Supervisory frame received */
105   3                                IF CHECK_NR=FALSE
                                         THEN RSD(STATION_NUMBER).STATION_STATE=GO_TO_DISC;

107   3                                ELSE IF ((RCB AND 0FH)=05H) /* then RNR */
                                             THEN RSD(STATION_NUMBER).BUFFER_STATUS=BUFFER_NOT_READY;
109   3                             END;

110   3                  ELSE DO;         /* Unnumbered frame or unknown frame received */
111   3                           IF RCB=FRMR
                                  THEN DO;    /* If FRMR was received check Nr for an
                                                 acknowledged I frame  */
113   4                                    RCB=SIU_RECV_BUFFER(1);
114   4                                    I=CHECK_NR;
115   4                                 END;
116   3                           RSD(STATION_NUMBER).STATION_STATE=GO_TO_DISC;
117   3                       END;

118   2                  RBE=1;

119   1          END RECEIVE;



120   2          XMIT_I_T_S: PROCEDURE (TEMP);

121   2              DECLARE      TEMP     BYTE;

122   2                  IF TEMP=T_I_FRAME
                           THEN DO;    /* Transmit I frame */
                                /* Transfer the station buffer into internal ram */

124   4                                DO TEMP=0 TO RSD(STATION_NUMBER).INFO_LENGTH-1;
125   4                                SIU_XMIT_BUFFER(TEMP)=RSD(STATION_NUMBER).DATA(TEMP);
126   4                                END;

                                       /* Build the I frame control field */

127   3                                TEMP=(SHL(RSD(STATION_NUMBER).NR,5) OR SHL(RSD(STATION_NUMBER).NS,1) OR 10H);
128   3                                TBL=RSD(STATION_NUMBER).INFO_LENGTH;
129   3                                CALL XMIT(TEMP);
130   3                                IF TIME_OUT=FALSE
                                           THEN CALL RECEIVE;
132   3                           END;

133   3                  ELSE DO;    /* Transmit RR or RNR*/
134   3                           IF TEMP=T_RR
                                      THEN TEMP=RR;
136   3                           ELSE TEMP=RNR;
```

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```
PL/M-51 COMPILER    RUPI-44 Primary Station                          20:47:13  09/26/83  PAGE   6

 137   3                    TEMP=(SHL(RSD(STATION_NUMBER).NR,5) OR TEMP);
 138   3                    TBL=0;
 139   3                    CALL XMIT(TEMP);
 140   3                    IF TIME_OUT=FALSE
                                THEN CALL RECEIVE;
 142   3                END;
 143   1      END XMIT_I_T_S;

 144   2      BUFFER_TRANSFER: PROCEDURE;

 145   2          DECLARE     I       BYTE    AUXILIARY,
                             J       BYTE    AUXILIARY;


 146   3          DO I=0 TO NUMBER_OF_STATIONS-1;
 147   3              IF RSD(I).STATION_ADDRESS=SIU_RECV_BUFFER(0)
                        THEN GOTO T1;
 149   3          END;

 150   2        T1:   IF I=NUMBER_OF_STATIONS  /* If the addressed station does not exits,
                                                  then discard the data */
                        THEN DO;
 152   3                        RBP=0;
 153   3                        RETURN;
 154   3                    END;
 155   2              ELSE IF RSD(I).INFO_LENGTH=0
                        THEN DO;
 157   3                        RSD(I).INFO_LENGTH=RECV_FIELD_LENGTH;
 158   4                        DO J=1 TO RECV_FIELD_LENGTH;
 159   4                            RSD(I).DATA(J-1)=SIU_RECV_BUFFER(J);
 160   4                        END;
 161   3                        RBP=0;
 162   3                    END;

 163   1      END BUFFER_TRANSFER;


 164   1      BEGIN:
              CALL POWER_ON;

 165   2          DO FOREVER;

 166   3              DO STATION_NUMBER=0 TO NUMBER_OF_STATIONS-1;
 167   3                  STAD=RSD(STATION_NUMBER).STATION_ADDRESS;
 168   3                  IF RSD(STATION_NUMBER).STATION_STATE = DISCONNECT_S
                            THEN CALL SEND_SNRM;
 170   3                  ELSE IF RSD(STATION_NUMBER).STATION_STATE = GO_TO_DISC
                            THEN CALL SEND_DISC;
 172   3                  ELSE IF ((RSD(STATION_NUMBER).INFO_LENGTH>0) AND
                                 (RSD(STATION_NUMBER).BUFFER_STATUS=BUFFER_READY))
                            THEN CALL XMIT_I_T_S(T_I_FRAME);
 174   3                  ELSE IF RBP=0
                            THEN CALL XMIT_I_T_S(T_RR);
 176   3                  ELSE CALL XMIT_I_T_S(T_RNR);

 177   3                  IF RBP=1
                            THEN CALL BUFFER_TRANSFER;
```

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```
PL/M-51 COMPILER    RUPI-44 Primary Station                          20:47:13  09/26/83  PAGE   7

 179   3              END;

 180   2          END;

 181   1      END MAIN$MOD;



WARNINGS:
    1 IS THE HIGHEST USED INTERRUPT


MODULE INFORMATION:                 (STATIC+OVERLAYABLE)
    CODE SIZE                       = 053DH       1341D
    CONSTANT SIZE                   = 0002H          2D
    DIRECT VARIABLE SIZE            =   40H+02H     64D+  2D
    INDIRECT VARIABLE SIZE          =   40H+00H     64D+  0D
    BIT SIZE                        =   01H+00H      1D+  0D
    BIT-ADDRESSABLE SIZE            =   00H+00H      0D+  0D
    AUXILIARY VARIABLE SIZE         = 0093H        147D
    MAXIMUM STACK SIZE              = 0019H         25D
    REGISTER-BANK(S) USED:            0 1
    456 LINES READ
    0 PROGRAM ERROR(S)
END OF PL/M-51 COMPILATION
```

296166-68

8044AH/8344AH/8744H
HIGH PERFORMANCE 8-BIT MICROCONTROLLER WITH ON-CHIP SERIAL COMMUNICATION CONTROLLER

- **8044AH—Includes Factory Mask Programmable ROM**
- **8344AH—For Use with External Program Memory**
- **8744H—Includes User Programmable/Eraseable EPROM**

8051 MICROCONTROLLER CORE

- **Optimized for Real Time Control 12 MHz Clock, Priority Interrupts, 32 Programmable I/O Lines, Two 16-bit Timer/Counters**
- **Boolean Processor**
- **4K × 8 ROM, 192 × 8 RAM**
- **64K Accessible External Program Memory**
- **64K Accessible External Data Memory**
- **4 μs Multiply and Divide**

SERIAL INTERFACE UNIT (SIU)

- **Serial Communication Processor that Operates Concurrently to CPU**
- **2.4 Mbps Maximum Data Rate**
- **375 Kbps using On-Chip Phase Locked Loop**
- **Communication Software in Silicon:**
  - **Complete Data Link Functions**
  - **Automatic Station Response**
- **Operates as an SDLC Primary or Secondary Station**

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The RUPI-44 family integrates a high performance 8-bit Microcontroller, the Intel 8051 Core, with an Intelligent/high performance HDLC/SDLC serial communication controller, called the Serial Interface Unit (SIU). See Figure 1. This dual architecture allows complex control and high speed data communication functions to be realized cost effectively.

Specifically, the 8044's Microcontroller features: 4K byte On-Chip program memory space; 32 I/O lines; two 16-bit timer/event counters; a 5-source; 2-level interrupt structure; a full duplex serial channel; a Boolean processor; and on-chip oscillator and clock circuitry. Standard TTL and most byte-oriented MCS-80 and MCS-85 peripherals can be used for I/O amd memory expansion.

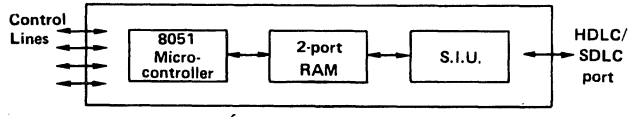
The Serial Interface Unit (SIU) manages the interface to a high speed serial link. The SIU offloads the On-Chip 8051 Microcontroller of communication tasks, thereby freeing the CPU to concentrate on real time control tasks.

The RUPI-44 family consists of the 8044, 8744, and 8344. All three devices are identical except in respect of on-chip program memory. The 8044 contains 4K bytes of mask-programmable ROM. User programmable EPROM replaces ROM in the 8744. The 8344 addresses all program memory externally.

The RUPI-44 devices are fabricated with Intel's reliable +5 volt, silicon-gate HMOSII technology and packaged in a 40-pin DIP.

The 8744H is available in a hermetically sealed, ceramic, 40-lead dual in-line package which includes a window that allows for EPROM erasure when exposed to ultraviolet light (See Erasure Characteristics). During normal operation, ambient light may adversely affect the functionality of the chip. Therefore applications which expose the 8744H to ambient light may require an opaque label over the window.

8044's Dual Controller Architecture



231663-1

Figure 1. Dual Controller Architecture

September 1990
Order Number: 231663-004

Table 1. RUPI™-44 Family Pin Description

VSS

Circuit ground potential.

VCC

+5V power supply during operation and program verification.

PORT 0

Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads (six in 8744).

PORT 1

Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.

In non-loop mode two of the I/O lines serve alternate functions:

— $\overline{RTS}$ (P1.6). Request-to-Send output. A low indicates that the RUPI-44 is ready to transmit.

— $\overline{CTS}$ (P1.7) Clear-to-Send input. A low indicates that a receiving station is ready to receive.

PORT 2

Port 2 is an 8-bit quasi-bidirection I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

PORT 3

Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS LTT loads.

In addition to I/O, some of the pins also serve alternate functions as follows:

— I/$\overline{O}$ RxD (P3.0). In point-to-point or multipoint configurations, this pin controls the direction of pin P3.1. Serves as Receive Data input in loop and diagnostic modes.

— DATA TxD (P3.1) In point-to-point or multipoint configurations, this pin functions as data input/output. In loop mode, it serves as transmit pin. A '0' written to this pin enables diagnostic mode.

— $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0.

— $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1.

— TO (P3.4). Input to counter 0.

— SCLK T1 (P3.5). In addition to I/O, this pin provides input to counter 1 or serves as SCLK (serial clock) input.

— $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.

— $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.

RST

A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor ($\approx$8.2KΩ) from RST to V_{SS} permits power-on reset when a capacitor ($\approx 10\mu f$) is also connected from this pin to V_{CC}.

ALE/$\overline{PROG}$

Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. It also receives the program pulse input for programming the EPROM version.

$\overline{PSEN}$

The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

$\overline{EA}$/VPP

When held at a TTL high level, the RUPI-44 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the RUPI-44 fetches all instructions from external Program Memory. The pin also receives the 21V EPROM programming supply voltage on the 8744.

Table 1. RUPI™-44 Family Pin Description (Continued)

XTAL 1	XTAL 2
Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2.	Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

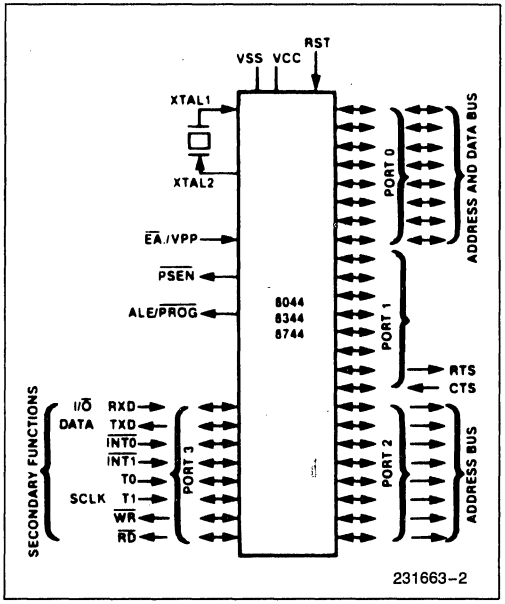


Figure 2. Logic Symbol

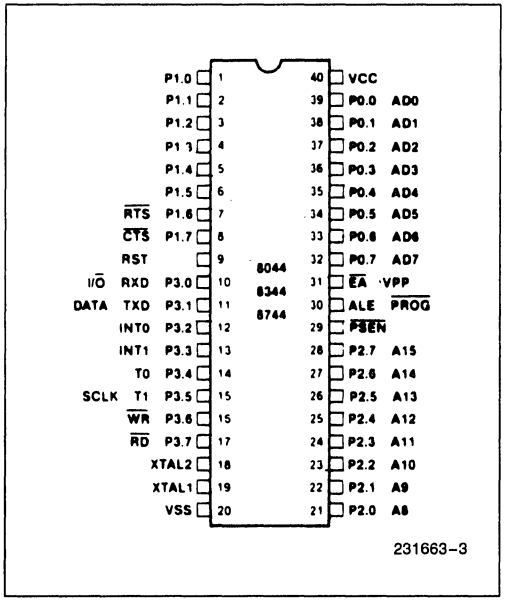


Figure 3A. DIP Pin Configuration

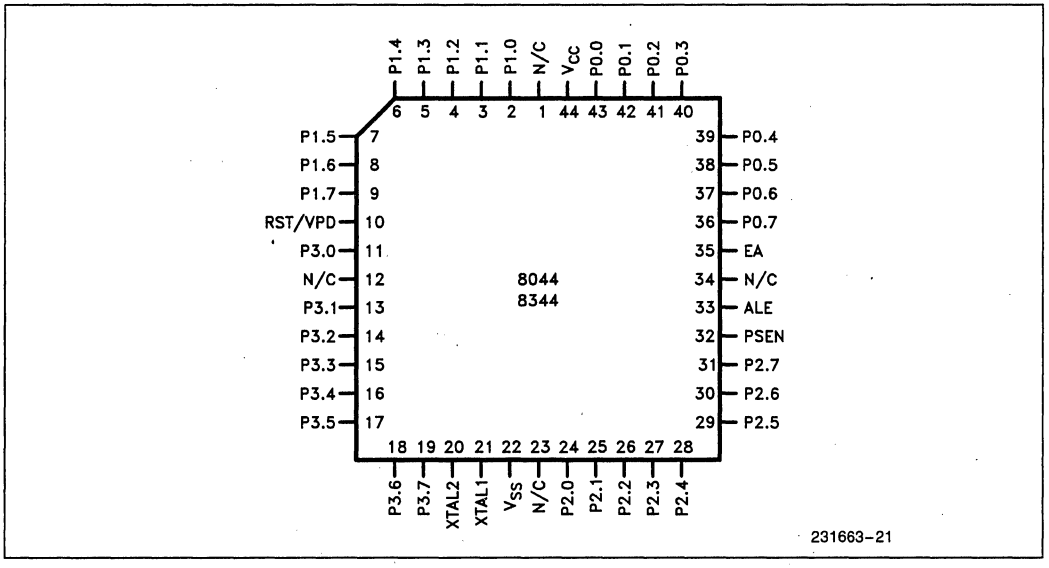


Figure 3B. PLCC Pin Configuration

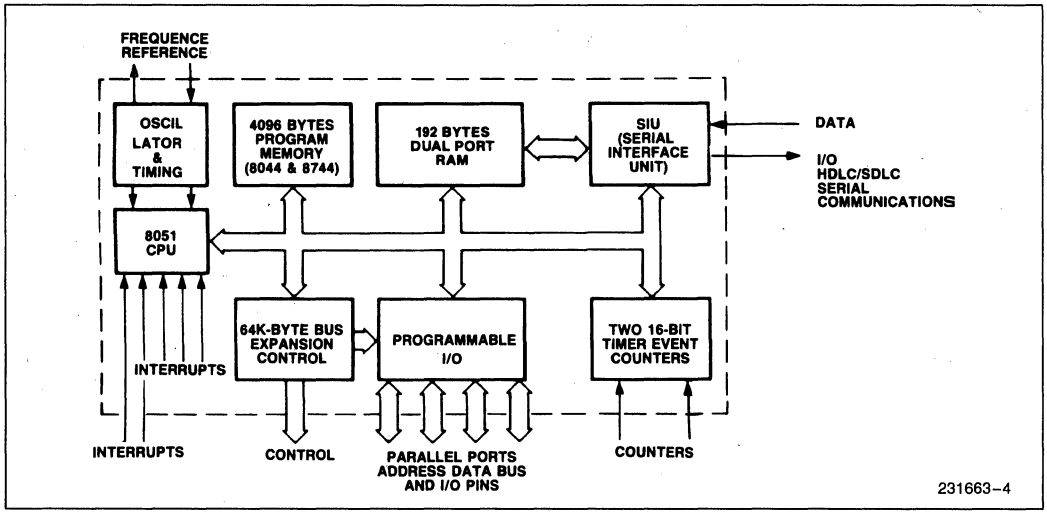


Figure 4. Block Diagram

FUNCTIONAL DESCRIPTION

General

The 8044 integrates the powerful 8051 microcontroller with an intelligent Serial Communication Controller to provide a single-chip solution which will efficiently implement a distributed processing or distributed control system. The microcontroller is a self-sufficient unit containing ROM, RAM, ALU, and its own peripherals. The 8044's architecture and instruction set are identical to the 8051's. The 8044 replaces the 8051's serial interface with an intelligent SDLC/HDLC Serial Interface Unit (SIU). 64 more bytes of RAM have been added to the 8051 RAM array. The SIU can communicate at bit rates up to 2.4 M bps. The SIU works concurrently with the Microcontroller so that there is no throughput loss in either unit. Since the SIU possesses its own intelligence, the CPU is off-loaded from many of the communications tasks, thus dedicating more of its computing power to controlling local peripherals or some external process.

The Microcontroller

The microcontroller is a stand-alone high-performance single-chip computer intended for use in sophisticated real-time application such as instrumentation, industrial control, and intelligent computer peripherals.

The major features of the microcontroller are:

- 8-bit CPU
- on-chip oscillator
- 4K bytes of ROM
- 192 bytes of RAM
- 32 I/O lines
- 64K address space for external Data Memory
- 64K address space for external Program Memory
- two fully programmable 16-bit timer/counters
- a five-source interrupt structure with two priority levels
- bit addressability for Boolean processing

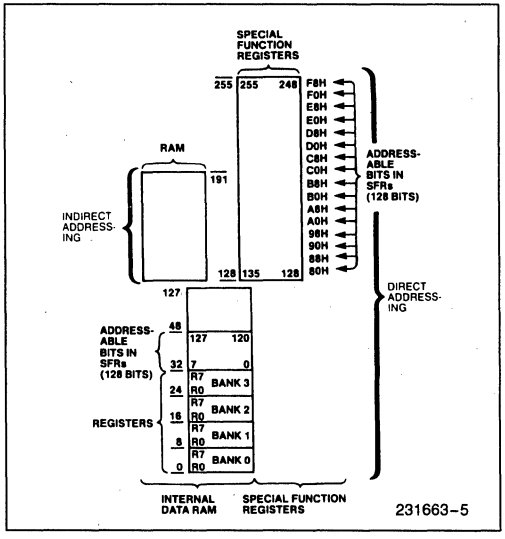


Figure 5. Internal Data Memory Address Space

- 1 μs instruction cycle time for 60% of the instructions 2 μs instruction cycle time for 40% of the instructions
- 4 μs cycle time for 8 by 8 bit unsigned Multiply/Divide

INTERNAL DATA MEMORY

Functionally the Internal Data Memory is the most flexible of the address spaces. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address space and a 128-bit Special Function Register address space as shown in Figure 5.

The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit locations of the on-chip RAM are accessible through Direct Addressing. These bits reside in Internal Data RAM at byte locations 32 through 47. Currently locations 0 through 191 of the Internal Data RAM address space are filled with on-chip RAM.

Parallel I/O

The 8044 has 32 general-purpose I/O lines which are arranged into four groups of eight lines. Each group is called a port. Hence there are four ports; Port 0, Port 1, Port 2, and Port 3. Up to five lines from Port 3 are dedicated to supporting the serial channel when the SIU is invoked. Due to the nature of the serial port, two of Port 3's I/O lines (P3.0 and P3.1) do not have latched outputs. This is true whether or not the serial channel is used.

Port 0 and Port 2 also have an alternate dedicated function. When placed in the external access mode, Port 0 and Port 2 become the means by which the 8044 communicates with external program memory. Port 0 and Port 2 are also the means by which the 8044 communicates with external data memory. Peripherals can be memory mapped into the address space and controlled by the 8044.

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Table 2. MCS®-51 Instruction Set Description

Mnemonic		Description	Byte	Cyc
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB	A,#data	Subtract immed data from A with Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic		Description	Byte	Cyc
LOGICAL OPERATIONS				
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@RI	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@RI	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1

Mnemonic		Description	Byte	Cyc
LOGICAL OPERATIONS (Continued)				
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@RI	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2

Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic		Description	Byte	Cyc
DATA TRANSFER (Continued)				
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit) addr	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind RAM w A	1	1
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry Flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry Flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C/bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,/bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2
PROGRAM AND MACHINE CONTROL				
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute Jump	2	2
LJMP	addr16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp, immed, to A & Jump if Not Equal	3	2

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Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic	Description	Byte	Cyc
PROGRAM AND MACHINE CONTROL (Continued)			
CJNE Rn,#data,rel	Comp, immed, to reg & Jump if Not Equal	3	2
CJNE @Ri,#data, rel	Comp, immed, to ind. & Jump if Not Equal	3	2
DJNZ Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP	No operation	1	1

Notes on data addressing modes:

Rn — Working register R0-R7

direct — 128 internal RAM locations, any I/O port, control or status register

@Ri — Indirect internal RAM location addressed by register R0 or R1

Notes on data addressing modes:

(Continued)

#data — 8-bit constant included in instruction

#data16 — 16-bit constant included as bytes 2 & 3 of instruction

bit — 128 software flags, any I/O pin, controll or status bit

Notes on program addressing modes:

addr16 — Destination address for LCALL & LJMP may be anywhere within the 64-K program memory address space

Addr11 — Destination address for ACALL & AJMP will be within the same 2-K page of program memory as the first byte of the following instruction

rel — SJMP and all conditional jumps include an 8-bit offset byte, Range is +127 −128 bytes relative to first byte of the following instruction

Timer/Counters

The 8044 contains two 16-bit counters which can be used for measuring time intervals, measuring pulse widths, counting events, generating precise periodic interrupt requests, and clocking the serial communications. Internally the Timers are clocked at 1/12 of the crystal frequency, which is the instruction cycle time. Externally the counters can run up to 500 KHz.

Interrupt System

External events and the real-time driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two priority level, nested interrupt system is provided. Interrupt response latency ranges from 3 μsec to 7 μsec when using a 12 MHz clock.

All five interrupt sources can be mapped into one of the two priority levels. Each interrupt source can be enabled or disabled individually or the entire interrupt system can be enabled or disabled. The five interrupt sources are: Serial Interface Unit, Timer 1, Timer 2, and two external interrupts. The external interrupts can be either level or edge triggered.

Serial Interface Unit (SIU)

The Serial Interface Unit is used for HDLC/SDLC communications. It handles Zero Bit Insertion/Deletion, Flags automatic access recognization, and a 16-bit cyclic redundancy check. In addition it implements in hardware a subset of the SDLC protocol certain applications it is advantageous to have the CPU control the reception or transmission of every single frame. For this reason the SIU has two modes of operation: "AUTO" and "FLEXIBLE" (or "NON-AUTO"). It is in the AUTO mode that the SIU responds to SDLC frames without CPU intervention; whereas, in the FLEXIBLE mode the reception or transmission of every single frame will be under CPU control.

There are three control registers and eight parameter registers that are used to operate the serial interface. These registers are shown in Figure 5 and Figure 6. The control register set the modes of operation and provide status information. The eight parameter registers buffer the station address, receive and transmit control bytes, and point to the on-chip transmit and receive buffers.

Data to be received or transmitted by the SIU must be buffered anywhere within the 192 bytes of on-chip RAM. Transmit and receive buffers are not allowed to "wrap around" in RAM; a "buffer end" is generated after address 191 is reached.

REGISTER NAMES	SYMBOLIC ADDRESS	BIT ADDRESS	BYTE ADDRESS
B REGISTER	B	247 through 240	240 (F0H)
ACCUMULATOR	ACC	231 through 224	224 (E0H)
*THREE BYTE FIFO	FIFO		223 (DFH)
	FIFO		222 (DEH)
	FIFO		221 (DDH)
TRANSMIT BUFFER START	TBS		220 (DCH)
TRANSMIT BUFFER LENGTH	TBL		219 (DBH)
TRANSMIT CONTROL BYTE	TCB		218 (DAH)
* SIU STATE COUNTER	SIUST		217 (D9H)
SEND COUNT RECEIVE COUNT	NSNR	223 through 216	216 (D8H)
PROGRAM STATUS WORD	PSW	215 through 208	208 (D0H)
*DMA COUNT	DMA CNT		207 (CFH)
STATION ADDRESS	STAD		206 (CEH)
RECEIVE FIELD LENGTH	RFL		205 (CDH)
RECEIVE BUFFER START	RBS		204 (CCH)
RECEIVE BUFFER LENGTH	RBL		203 (CBH)
RECEIVE CONTROL BYTE	RCB		202 (CAH)
SERIAL MODE	SMD		201 (C9H)
STATUS REGISTER	STS	207 through 200	200 (C8H)
INTERRUPT PRIORITY CONTROL	IP	191 through 184	184 (B8H)
PORT 3	P3	183 through 176	176 (B0H)
INTERRUPT ENABLE CONTROL	IE	175 through 168	168 (A8H)
PORT 2	P2	167 through 160	160 (A0H)
PORT 1	P1	151 through 144	144 (90H)
TIMER HIGH 1	TH1		141 (8DH)
TIMER HIGH 0	TH0		140 (8CH)
TIMER LOW 1	TL1		139 (8BH)
TIMER LOW 0	TL0		138 (8AH)
TIMER MODE	TMOD		137 (89H)
TIMER CONTROL	TCON	143 through 136	136 (88H)
DATA POINTER HIGH	DPH		131 (83H)
DATA POINTER LOW	DPL		130 (82H)
STACK POINTER	SP		129 (81H)
PORT 0	P0	135 through 128	128 (80H)

SFR's CONTAINING DIRECT ADDRESSABLE BITS

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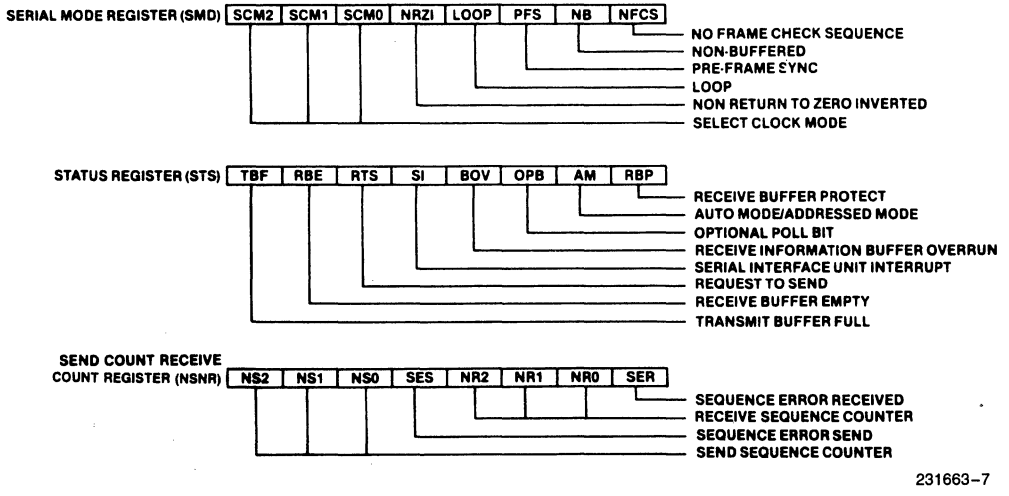
NOTE:
*ICE Support Hardware registers. Under normal operating conditions there is no need for the CPU to access these registers.

Figure 5. Mapping of Special Function Registers



231663-7

Figure 6. Serial Interface Unit Control Registers

With the addition of only a few bytes of code, the 8044's frame size is not limited to the size of its internal RAM (192 bytes), but rather by the size of external buffer with no degradation of the RUPI's features (e.g. NRZI, zero bit insertion/deletion, address recognition, cyclic redundancy check). There is a special function register called SIUST whose contents dictates the operation of the SIU. At low data rates, one section of the SIU (the Byte Processor) performs no function during known intervals. For a given data rate, these intervals (stand-by mode) are fixed. The above characteristics make it possible to program the CPU to move data to/from external RAM and to force the SIU to perform some desired hardware tasks while transmission or reception is taking place. With these modifications, external RAM can be utilized as a transmit and received buffer instead of the internal RAM.

AUTO Mode

In the AUTO mode the SIU implements in hardware a subset of the SDLC protocol such that it responds to many SDLC frames without CPU intervention. All AUTO mode responses to the primary station will comform to IBM's SDLC definition. The advantages of the AUTO mode are that less software is required to implement a secondary station, and the hardware generated response to polls is much faster than doing it in software. However, the Auto mode can not be used at a primary station.

To transmit in the AUTO mode the CPU must load the Transmit Information Buffer, Transmit Buffer Start register, Transmit Buffer Length register, and set the Transmit Buffer Full bit. The SIU automatically responds to a poll by transmitting an information frame with the P/F bit in the control field set. When the SIU receives a positive acknowledgement from the primary station, it automatically increments the Ns field in the NSNR register and interrupts the CPU. A negative acknowledgement would cause the SIU to retransmit the frame.

To receive in the AUTO mode, the CPU loads the Receive Buffer Start register, the Receive Buffer Length register, clears the Receive Buffer Protect bit, and sets the Receive Buffer Empty bit. If the SIU is polled in this state, and the TBF bit indicates that the Transmit Buffer is empty, an automatic RR response will be generated. When a valid information frame is received the SIU will automatically increment Nr in the NSNR register and interrupt the CPU.

While in the AUTO mode the SIU can recognize and respond to the following commands without CPU intervention: I (Information), RR (Receive Ready), RNR (Receive Not Ready), REJ (Reject), and UP (Unnumbered Poll). The SIU can generate the following responses without CPU intervention: I (Information), RR (Receive Ready), and RNR (Receive Not Ready).

When the Receive Buffer Empty bit (RBE) indicates that the Receive Buffer is empty, the receiver is enabled, and when the RBE bit indicates that the Receive Buffer is full, the receiver is disabled. Assuming that the Receiver Buffer is empty, the SIU will respond to a poll with an I frame if the Transmit Buffer is full. If the Transmit Buffer is empty, the SIU will respond to a poll with a RR command if the Receive Buffer Protect bit (RBP) is cleared, or an RNR command if RBP is set.

FLEXIBLE (or NON-AUTO) Mode

In the FLEXIBLE mode all communications are under control of the CPU. It is the CPU's task to encode and decode control fields, manage acknowledgements, and adhere to the requirements of the HDLC/SDLC protocols. The 8044 can be used as a primary or a secondary station in this mode.

To receive a frame in the FLEXIBLE mode, the CPU must load the Receive Buffer Start register, the Receive Buffer Length register, clear the Receive Buffer Protect bit, and set the Receive Buffer Empty bit. If a valid opening flag is received and the address field matches the byte in the Station Address register or the address field contains a broadcast address, the 8044 loads the control field in the receive control byte register, and loads the I field in the receive buffer. If there is no CRC error, the SIU interrupts the CPU, indicating a frame has just been received. If there is a CRC error, no interrupt occurs. The Receive Field Length register provides the number of bytes that were received in the information field.

To transmit a frame, the CPU must load the transmit information buffer, the Transmit Buffer Start register, the Transmit Buffer Length register, the Transmit Control Byte, and set the TBF and the RTS bit. The SIU, unsolicited by an HDLC/SDLC frame, will transmit the entire information frame, and interrupt the CPU, indicating the completion of transmission. For supervisory frames or unnumbered frames, the transmit buffer length would be 0.

CRC

The FCS register is initially set to all 1's prior to calculating the FCS field. The SIU will not interrupt the CPU if a CRC error occurs (in both AUTO and FLEXIBLE modes). The CRC error is cleared upon receiving of an opening flag.

Frame Format Options

In addition to the standard SDLC frame format, the 8044 will support the frames displayed in Figure 7. The standard SDLC frame is shown at the top of this figure. For the remaining frames the information field will incorporate the control or address bytes and the frame check sequences; therefore these fields will be stored in the Transmit and Receive buffers. For example, in the non-buffered mode the third byte is treated as the beginning of the information field. In the non-addressed mode, the information field begins after the opening flag. The mode bits to set the frame format options are found in the Serial Mode register and the Status register.

FRAME OPTION	NFCS	NB	AM[1]	FRAME FORMAT
Standard SDLC NON-AUTO Mode	0	0	0	F A C I FCS F
Standard SDLC AUTO Mode	0	0	1	F A C I FCS F
Non-Buffered Mode NON-AUTO Mode	0	1	1	F A I FCS F
Non-Addressed Mode NON-AUTO Mode	0	1	0	F I FCS F
No FCS Field NON-AUTO Mode	1	0	0	F A C I F
No FCS Field AUTO Mode	1	0	1	F A C I F
No FCS Field Non-Buffered Mode NON-AUTO Mode	1	1	1	F A I F
No FCS Field Non-Addressed Mode NON-AUTO Mode	1	1	0	F I F

Mode Bits:
AM — "AUTO" Mode/Addressed Mode
NB — Non-Buffered Mode
NFCS — No FCS Field Mode

Key to Abbreviations:
F = Flag (01111110)
A = Address Field
C = Control Field
I = Information Field
FCS= Frame Check Sequence

Note 1:
The AM bit function is controlled by the NB bit. When NB = 0, AM becomes AUTO mode select, when NB = 1, AM becomes Address mode select.

Figure 7. Frame Format Options

Extended Addressing

To realize an extended control field or an extended address field using the HDLC protocol, the FLEXIBLE mode must be used. For an extended control field, the SIU is programmed to be in the non-buffered mode. The extended control field will be the first and second bytes in the Receive and Transmit Buffers. For extended addressing the SIU is placed in the non-addressed mode. In this mode the CPU must implement the address recognition for received frames. The addressing field will be the initial bytes in the Transmit and Receive buffers followed by the control field.

The SIU can transmit and receive only frames which are multiples of 8 bits. For frames received with other than 8-bit multiples, a CRC error will cause the SIU to reject the frame.

SDLC Loop Networks

The SIU can be used in an SDLC loop as a secondary or primary station. When the SIU is placed in the Loop mode it receives the data on pin 10 and transmits the data one bit time delayed on pin 11. It can also recognize the Go ahead signal and change it into a flag when it is ready to transmit. As a secondary station the SIU can be used in the AUTO or FLEXIBLE modes. As a primary station the FLEXIBLE mode is used; however, additional hardware is required for generating the Go Ahead bit pattern. In the Loop mode the maximum data rate is 1 Mbps clocked or 375 Kpbs self-clocked.

SDLC Multidrop Networks

The SIU can be used in a SDLC non-loop configuration as a secondary or primary station. When the SIU is placed in the non-loop mode, data is received and transmitted on pin 11, and pin 10 drives a tri-state buffer. In non-loop mode, modem interface pins, RTS and CTS, become available.

Data Clocking Options

The 8044's serial port can operate in an externally clocked or self clocked system. A clocked system provides to the 8044 a clock synchronization to the data. A self-clocked system uses the 8044's on-chip Digital Phase Locked Loop (DPLL) to recover the clock from the data, and clock this data into the Serial Receive Shift Register.

In this mode, a clock synchronized with the data is externally fed into the 8044. This clock may be generated from an External Phase Locked Loop, or possibly supplied along with the data. The 8044 can transmit and receive data in this mode at rates up to 2.4 Mbps.

This self clocked mode allows data transfer without a common system data clock. An on-chip Digital Phase Locked Loop is employed to recover the data clock which is encoded in the data stream. The DPLL will converge to the nominal bit center within eight bit transitions, worst case. The DPLL requires a reference clock of either 16 times (16x) or 32 times (32x) the data rate. This reference clock may be externally applied or internally generated. When internally generated either the 8044's internal logic clock (crystal frequency divided by two) or the timer 1 overflow is used as the reference clock. Using the internal timer 1 clock the data rates can vary from 244 to 62.5 Kbps. Using the internal logic clock at a 16x sampling rate, receive data can either be 187.5 Kbps, or 375 Kbps. When the reference clock for the DPLL is externally applied the data rates can vary from 0 to 375 Kbps at a 16x sampling rate.

To aid in a Phase Locked Loop capture, the SIU has a NRZI (Non Return to Zero Inverted) data encoding and decoding option. Additionally the SIU has a preframe sync option that transmits two bytes of alternating 1's and 0's to ensure that the receive station DPLL will be synchronized with the data by the time it receives the opening flag.

Control and Status Registers

There are three SIU Control and Status Registers:

Serial Mode Register (SMD)

Status/Command Register (STS)

Send/Receive Count Register (NSNR)

The SMD, STS, and NSNR, registers are all cleared by system reset. This assures that the SIU will power up in an idle state (neither receiving nor transmitting).

These registers and their bit assignments are described below.

SMD: Serial Mode Register (byte-addressable)

Bit 7:	6	5	4	3	2	1	0
SCM2	SCM1	SCM0	NRZI	LOOP	PFS	NB	NFCS

The Serial Mode Register (Address C9H) selects the operational modes of the SIU. The 8044 CPU can both read and write SMD. The SIU can read SMD but cannot write to it. To prevent conflict between CPU and SIU access to SMD, the CPU should write SMD only when the Request To Send (RTS) and

Receive Buffer Empty (RBE) bits (in the STS register) are both false (0). Normally, SMD is accessed only during initialization.

The individual bits of the Serial Mode Register are as follows:

Bit #	Name	Description
SMD.0	NFCS	No FCS field in the SDLC frame.
SMD.1	NB	Non-Buffered mode. No control field in the SDLC frame.
SMD.2	PFS	Pre-Frame Sync mode. In this mode, the 8044 transmits two bytes before the first flag of a frame, for DPLL synchronization. If NRZI is enabled, 00H is sent; otherwise, 55H is sent. In either case, 16 preframe transitions are guaranteed.
SMD.3	LOOP	Loop configuration.
SMD.4	NRZI	NRZI coding option. If bit = 1, NRZI coding is used. If bit = 0, then it is straight binary (NRZ).
SMD.5	SCM0	Select Clock Mode—Bit 0
SMD.6	SCM1	Select Clock Mode—Bit 1
SMD.7	SCM2	Select Clock Mode—Bit 2

The SCM bits decode as follows:

SCM				Data Rate
2	1	0	Clock Mode	(Bits/sec)*
0	0	0	Externally clocked	0-2.4M**
0	0	1	Reserved	
0	1	0	Self clocked, timer overflow	244-62.5K
0	1	1	Reserved	
1	0	0	Self clocked, external 16x	0-375K
1	0	1	Self clocked, external 32x	0-187.5K
1	1	0	Self clocked, internal fixed	375K
1	1	1	Self clocked, internal fixed	187.5K

NOTES:
*Based on a 12 Mhz crystal frequency
**0-1 M bps in loop configuration

STS: Status/Command Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	TBF	RBE	RTS	SI	BOV	OPB	AM	RBP

The Status/Command Register (Address C8H) provides operational control of the SIU by the 8044 CPU, and enables the SIU to post status information for the CPU's access. The SIU can read STS, and can alter certain bits, as indicated below. The CPU can both read and write STS asynchronously. However, 2-cycle instructions that access STS during both cycles ('JBC/B, REL' and 'MOV/B, C.') should not be used, since the SIU may write to STS between the two CPU accesses.

The individual bits of the Status/Command Register are as follows:

Bit #	Name	Description
STS.0	RBP	Receive Buffer Protect. Inhibits writing of data into the receive buffer. In AUTO mode, RBP forces an RNR response instead of an RR.
STS.1	AM	AUTO Mode/Addressed Mode. Selects AUTO mode where AUTO mode is allowed. If NB is true, (= 1), the AM bit selects the addressed mode. AM may be cleared by the SIU.
STS.2	OPB	Optional Poll Bit. Determines whether the SIU will generate an AUTO response to an optional poll (UP with P = 0). OPM may be set or cleared by the SIU.
STS.3	BOV	Receive Buffer Overrun. BOV may be set or cleared by the SIU.
STS.4	SI	SIU Interrupt. This is one of the five interrupt sources to the CPU. The vector location = 23H. SI may be set by the SIU. It should be cleared by the CPU before returning from an interrupt routine.
STS.5	RTS	Request To Send. Indicates that the 8044 is ready to transmit or is transmitting. RTS may be read or written by the CPU. RTS may be read by the SIU, and in AUTO mode may be written by the SIU.
STS.6	RBE	Receive Buffer Empty. RBE can be thought of as Receive Enable. RBE is set to one by the CPU when it is ready to receive a frame, or has just read the buffer, and to zero by the SIU when a frame has been received.
STS.7	TBF	Transmit Buffer Full. Written by the CPU to indicate that it has filled the transmit buffer. TBF may be cleared by the SIU.

NSNR: Send/Receive Count Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	NS2	NS1	NS0	SES	NR2	NR1	NR0	SER

The Send/Receive Count Register (Address D8H) contains the transmit and receive sequence numbers, plus tally error indications. The SIU can both read and write NSNR. The 8044 CPU can both read and write NSNR asynchronously. However, 2-cycle instructions that access NSNR during both cycles ('JBC /B, REL,' and 'MOV /B,C') should not be used, since the SIU may write to NSMR between the two 8044 CPU accesses.

The individual bits of the Send/Receive Count Register are as follows:

Bit #	Name	Description
NSNR.0	SER	Receive Sequence Error: NS (P) ≠ NR (S)
NSNR.1	NR0	Receive Sequence Counter—Bit 0
NSNR.2	NR1	Receive Sequence Counter—Bit 1
NSNR.3	NR2	Receive Sequence Counter—Bit 2
NSNR.4	SES	Send Sequence Error: NR (P) ≠ NS (S) and NR (P) ≠ NS (S) + 1
NSNR.5	NS0	Send Sequence Counter—Bit 0
NSNR.6	NS1	Send Sequence Counter—Bit 1
NSNR.7	NS2	Send Sequence Counter—Bit 2

Parameter Registers

There are eight parameter registers that are used in connection with SIU operation. All eight registers may be read or written by the 8044 CPU. RFL and RCB are normally loaded by the SIU.

The eight parameter registers are as follows:

STAD: Station Address Register (byte-addressable)

The Station Address register (Address CEH) contains the station address. To prevent acess conflict, the CPU should access STAD only when the SIU is idle (RTS = 0 and RBE = 0). Normally, STAD is accessed only during initialization.

TBS: Transmit Buffer Start Address Register (byte-addressable)

The Transmit Buffer Start address register (Address DCH) points to the location in on-chip RAM for the beginning of the I-field of the frame to be transmitted. The CPU should access TBS only when the SIU is not transmitting a frame (when TBF = 0).

TBL: Transmit Buffer Length Register (byte = addressable)

The Transmit Buffer Length register (Address DBH) contains the length (in bytes) of the I-field to be transmitted. A blank I-field (TBL = 0) is valid. The CPU should access TBL only when the SIU is not transmitting a frame (when TBF = 0).

NOTE:
The transmit and receive buffers are not allowed to "wrap around" in the on-chip RAM. A "buffer end" is automatically generated if address 191 (BFH) is reached.

TCB: Transmit Control Byte Register (byte-addressable)

The Transmit Control Byte register (Address DAH) contains the byte which is to be placed in the control field of the transmitted frame, during NON-AUTO mode transmission. The CPU should access TCB only when the SIU is not transmitting a frame (when TBF = 0). The N_S and N_R counters are not used in the NON-AUTO mode.

RBS: Receive Buffer Start Address Register (byte-addressable)

The Receive Buffer Start address register (Address CCH) points to the location in on-chip RAM where the beginning of the I-field of the frame being received is to be stored. The CPU should write RBS only when the SIU is not receiving a frame (when RBE = 0).

RBL: Receive Buffer Length Register (byte-addressable)

The Receive Buffer Length register (Address CBH) contains the length (in bytes) of the area in on-chip RAM allocated for the received I-field. RBL=0 is valid. The CPU should write RBL only when RBE=0.

RFL: Receive Field Length Register (byte-addressable)

The Receive Field Length register (Address CDH) contains the length (in bytes) of the received I-field that has just been loaded into on-chip RAM. RFL is loaded by the SIU. RFL = 0 is valid. RFL should be accessed by the CPU only when RBE = 0.

RCB: Receive Control Byte Register (byte-addressable)

The Received Control Byte register (Address CAH) contains the control field of the frame that has just been received. RCB is loaded by the SIU. The CPU can only read RCB, and should only access RCB when RBE = 0.

ICE Support

The 8044 In-Circuit Emulator (ICE-44) allows the user to exercise the 8044 application system and monitor the execution of instructions in real time.

The emulator operates with Intel's Intellec™ development system. The development system interfaces with the user's 8044 system through an in-cable buffer box. The cable terminates in a 8044 pin-compatible plug, which fits into the 8044 socket in the user's system. With the emulator plug in place, the user can excercise his system in real time while collecting up to 255 instruction cycles of real-time data. In addition, he can single-step the program.

Static RAM is available (in the in-cable buffer box) to emulate the 8044 internal and external program memory and external data memory. The designer can display and alter the contents of the replacement memory in the buffer box, the internal data memory, and the internal 8044 registers, including the SFR's.

SIUST: SIU State Counter (byte-addressable)

The SIU State Counter (Address D9H) reflects the state of the internal logic which is under SIU control. Therefore, care must be taken not to write into this register. This register provides a useful means for debugging 8044 receiver problem.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature.....−65°C to −150°C
Voltage on $\overline{EA}$, VPP Pin to VSS...−0.5V to −21.5V
Voltage on Any Other Pin to VSS ....−0.5V to −7V
Power Dissipation 2W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, VCC = 5V = 10%, VSS = 0V

Symbol	Parameter		Min	Max	Unit	Test Conditions
VIL	Input Low Voltage (Except $\overline{EA}$ Pin of 8744H)		−0.5	0.8	V	
VIL1	Input Low Voltage to $\overline{EA}$ Pin of 8744H		0	0.8	V	
VIH	Input High Voltage (Except XTAL2, RST)		2.0	VCC + 0.5	V	
VIH1	Input High Voltage to XTAL2, RST		2.5	VCC + 0.5	V	XTAL1 = VSS
VOL	Output Low Voltage (Ports 1, 2, 3)*			0.45	V	IOL = 1.6mA
VOL1	Output Low Voltage (Port 0,ALE,$\overline{PSEN}$)*					
		8744H		0.60 0.45	V V	IOL = 3.2 mA IOL = 2.4 mA
		8044AH/8344AH		0.45	V	IOL = 3.2 mA
VOH	Output High Voltage (Ports 1, 2, 3)		2.4		V	IOH = −80 μA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)		2.4		V	IOH = −400 μA
IIL	Logical 0 Input Current (Ports 1, 2, 3)			−500	μA	Vin = 0.45V
IIL1	Logical 0 Input Current to $\overline{EA}$ Pin of 8744H only			−15	mA	
IIL2	Logical 0 Input Current (XTAL2)			−3.6	mA	Vin = 0.45V
ILI	Input Leakage Current (Port 0) 8744H 8044AH/8344AH			 ±100 ±10	 μA μA	 0.45 < Vin < VCC 0.45 < Vin < VCC
IIH	Logical 1 Input Current to $\overline{EA}$ Pin of 8744H			500	μA	
IIH1	Input Current to RST to Activate Reset			500	μA	Vin < (VCC − 1.5V)
ICC	Power Supply Current: 8744H 8044AH/8344AH			 285 170	 mA mA	All Outputs Disconnected: $\overline{EA}$ = VCC
CIO	Pin Capacitance			10	pF	Test Freq. = 1MHz(1)

***NOTES:**
1. Sampled not 100% tested. T_A = 25°C.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pin when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, VCC = 5V ± 10%, VSS = 0V, Load Capacitance for Port 0, ALE, and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		Unit
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	127		2TCLCL-40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL-40		ns
TLLAX[1]	Address Hold After ALE Low	48		TCLCL-35		ns
TLLIV	ALE Low to Valid Instr in					ns
	8744H		183		4TCLCL-150	
	8044AH/8344AH		233		4TCLCL-100	
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width					
	8744H	190		3TCLCL-60		ns
	8044AH/8344AH	215		3TCLCL-35		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr in					
	8744H		100		3TCLCL-150	ns
	8044AH/8344AH		125		3TCLCL-125	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ[2]	Input Instr Float After $\overline{PSEN}$		63		TCLCL-20	ns
TPXAV[2]	$\overline{PSEN}$ to Address Valid	75		TCLCL-8		ns
TAVIV	Address to Valid Instr in					
	8744H		267		5TCLCL-150	ns
	8044AH/8344AH		302		5TCLCL-115	ns
TAZPL	Address Float to $\overline{PSEN}$	−25		−25		ns

NOTES:
1. TLLAX for access to program memory is different from TLLAX for data memory.
2. Interfacing RUPI-44 devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		Unit
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL-100		ns
TLLAX	Address Hold after ALE	48		TCLCL-35		ns
TRLDV	$\overline{RD}$ Low to Valid Data in		252		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL-70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL-50	3TLCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL-130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition					
	8744H	13		TCLCL-70		ns
	8044AH/8344AH	23		TCLCL-60		ns
TQVWH	Data Setup Before $\overline{WR}$ High	433		7TCLCL-150		ns
TWHQX	Data Held After $\overline{WR}$	33		TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		25		25	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High					
	8744H	33	133	TCLCL-50	TCLCL+50	ns
	8044AH/8344AH	43	123	TCLCL-40	TCLCL+50	ns

NOTE:
1. TLLAX for access to program memory is different from TLLAX for access data memory.

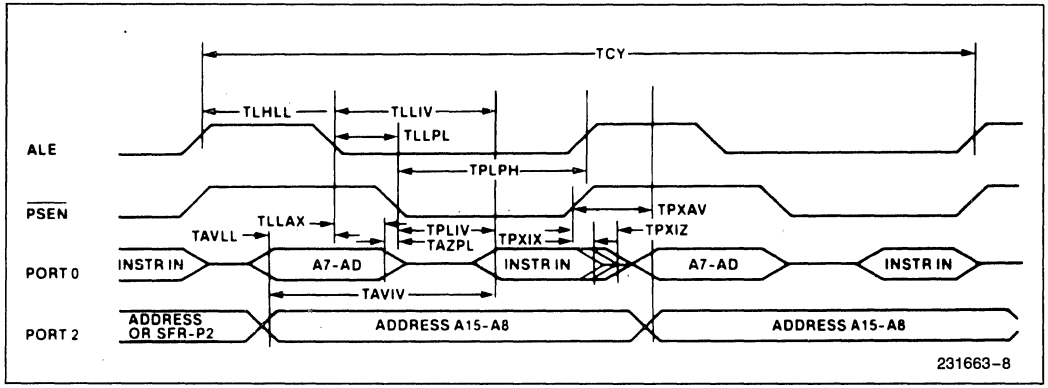
Serial Interface Characteristics

Symbol	Parameter	Min	Max	Unit
TDCY	Data Clock	420		ns
TDCL	Data Clock Low	180		ns
TDCH	Data Clock High	100		ns
tTD	Transmit Data Delay		140	ns
tDSS	Data Setup Time	40		ns
tDHS	Data Hold Time	40		ns

WAVEFORMS

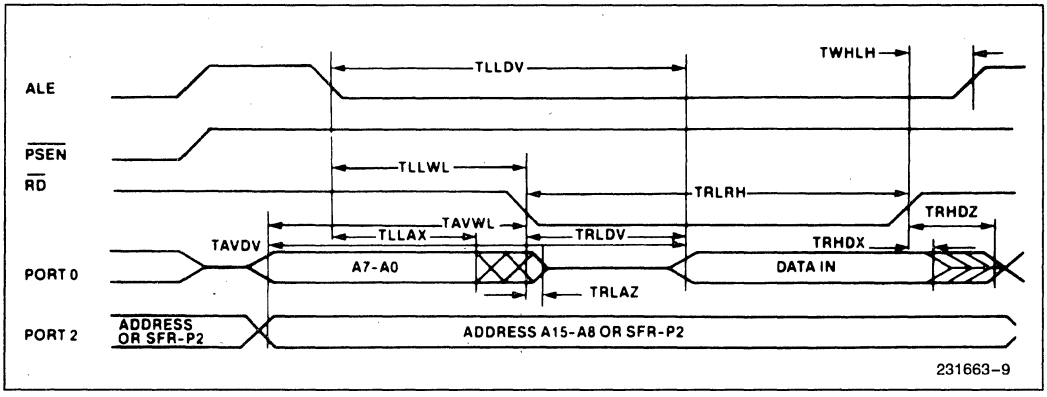
Memory Access

PROGRAM MEMORY READ CYCLE

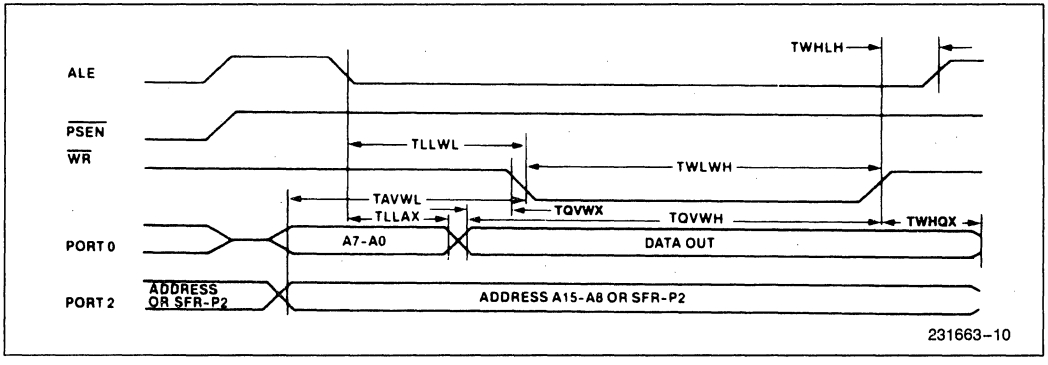


12

DATA MEMORY READ CYCLE

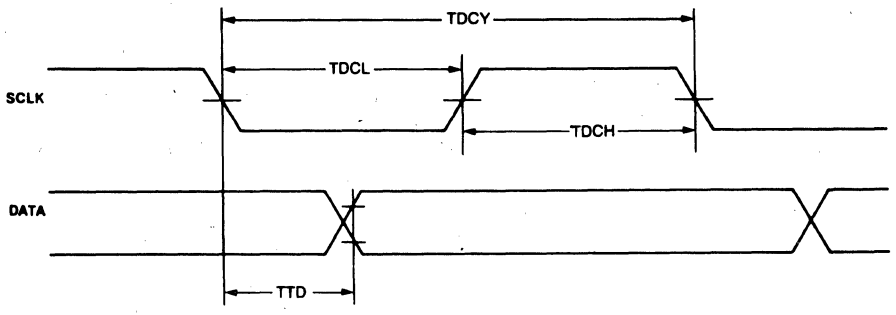


DATA MEMORY WRITE CYCLE

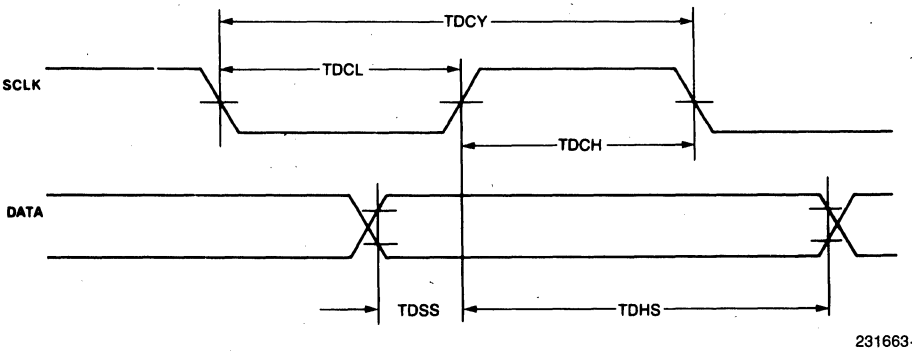


SERIAL I/O WAVEFORMS

SYNCHRONOUS DATA TRANSMISSION

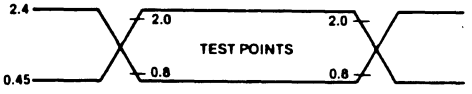


SYNCHRONOUS DATA RECEPTION



AC TESTING INPUT, OUTPUT, FLOAT WAVEFORMS

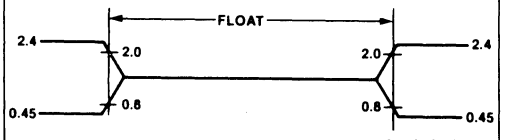
INPUT/OUTPUT



231663-13

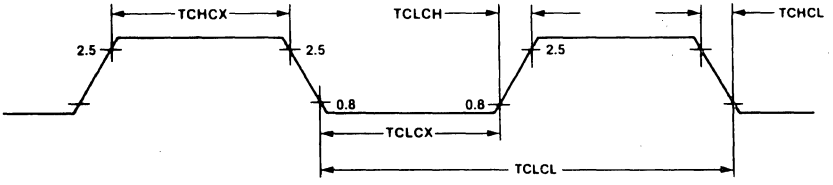
AC testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT



231663-14

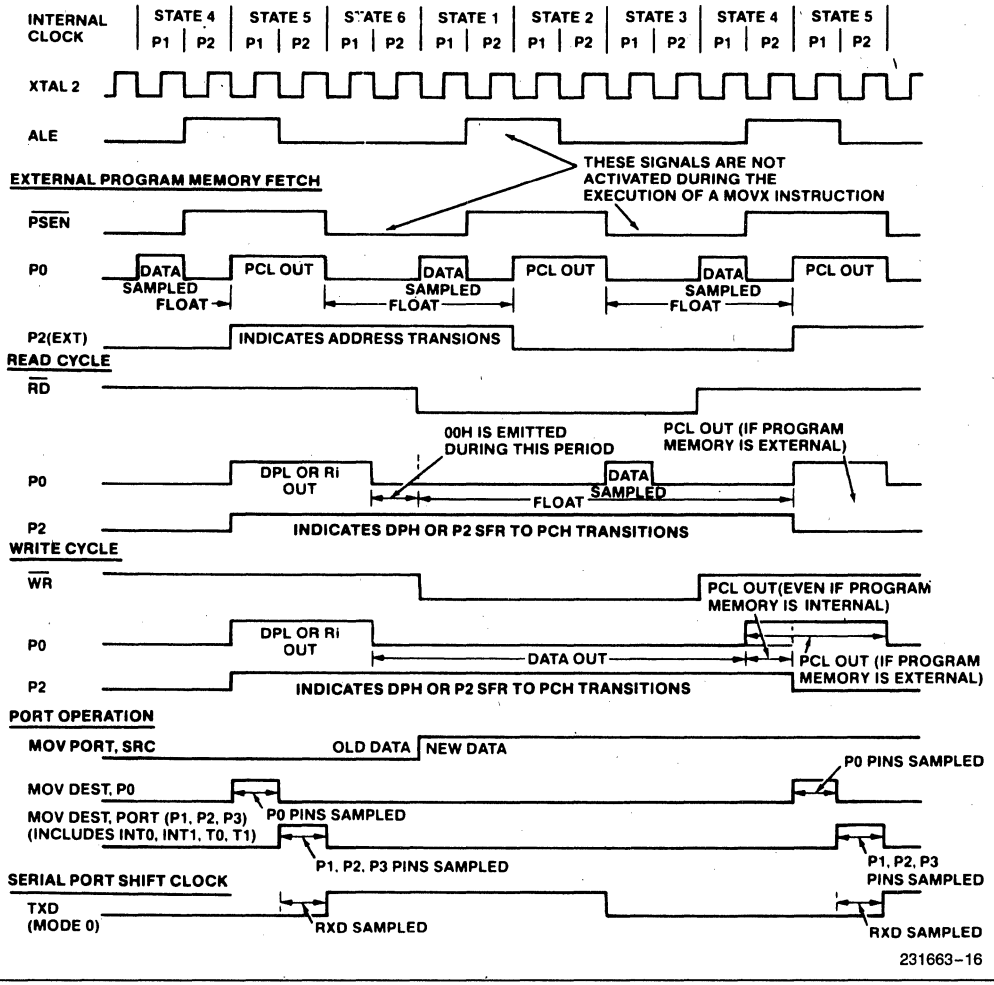
EXTERNAL CLOCK DRIVE XTAL2



231663-15

Symbol	Parameter	Variable Clock Freq = 3.5 MHz to 12 MHz		Unit
		Min	Max	
TCLCL	Oscillator Period	83.3	285.7	ns
TCHCX	High Time	20	TCLCL-TCLCX	ns
TCLCX	Low Time	20	TCLCL-TCHCX	ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

CLOCK WAVEFORMS



231663-16

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

8744H EPROM CHARACTERISTICS

Erasure Characteristics

Erasure of the 8744H Program Memory begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Ångstroms. Since sunlight and fluorescent lighting have wavelengths in this range, constant exposure to these light sources over an extended period of time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause unintentional erasure. If an application subjects the 8744H to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Ångstroms) to an integrated dose of at least 15 W-sec/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Programming the EPROM

To be programmed, the 8744H must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0-P2.3 of Port 2, while the data byte is applied to Port 0. Pins P2.4-P2.6 and $\overline{\text{PSEN}}$ should be held low, and P2.7 and RST high. (These are all TTL levels except RST, which requires 2.5V for high.) $\overline{\text{EA}}$/VPP is held normally high, and is pulsed to +21V. While EA/VPP is at 21V, the ALE/$\overline{\text{PROG}}$ pin, which is normally being held high, is pulsed low for 50 msec. Then EA/VPP is returned to high. This is illustrated in Figure 8. Detailed timing specifications are provided in the EPROM Programming and Verification Characteristics section of this data sheet.

Program Memory Security

The program memory security feature is developed around a "security bit" in the 8744H EPROM array. Once this "hidden bit" is programmed, electrical access to the contents of the entire program memory array becomes impossible. Activation of this feature is accomplished by programming the 8744H as described in "Programming the EPROM" with the exception that P2.6 is held at a TTL high rather than a TTL low. In addition, Port 1 and P2.0-P2.3 may be in any state. Figure 9 illustrates the security bit programming configuration. Deactivating the security feature, which again allows programmability of the EPROM, is accomplished by exposing the EPROM to ultraviolet light. This exposure, as described in "Erasure Characteristics," erases the entire EPROM array. Therefore, attempted retrieval of "protected code" results in its destruction.

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Program Verification

Program Memory may be read only when the "security feature" has not been activated. Refer to Figure 10 for Program Verification setup. To read the Program Memory, the following procedure can be used. The unit must be running with a 4 to 6 MHz oscillator. The address of a Program Memory location to be read is applied to Port 1 and pins P2.0-P2.3 of Port 2. Pins P2.4-P2.6 and $\overline{\text{PSEN}}$ are held at TTL low, while the ALE/$\overline{\text{PROG}}$, RST, and $\overline{\text{EA}}$/VPP pins are held at TTL high. (These are all TTL levels except RST, which requires 2.5V for high.) Port 0 will be the data output lines. P2.7 can be used as a read strobe. While P2.7 is held high, the Port 0 pins float. When P2.7 is strobed low, the contents of the addressed location will appear at Port 0. External pullups (e.g., 10K) are required on Port 0 during program verification.

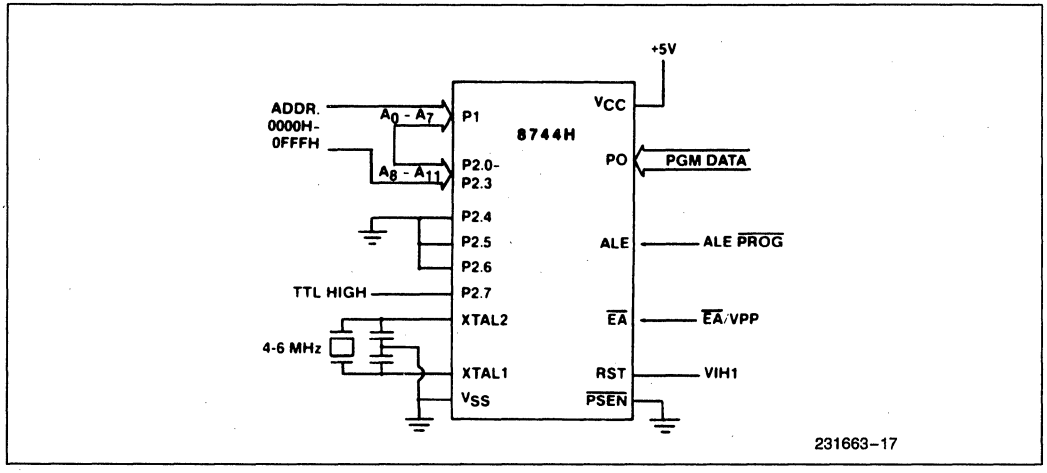

Figure 8. Programming Configuration

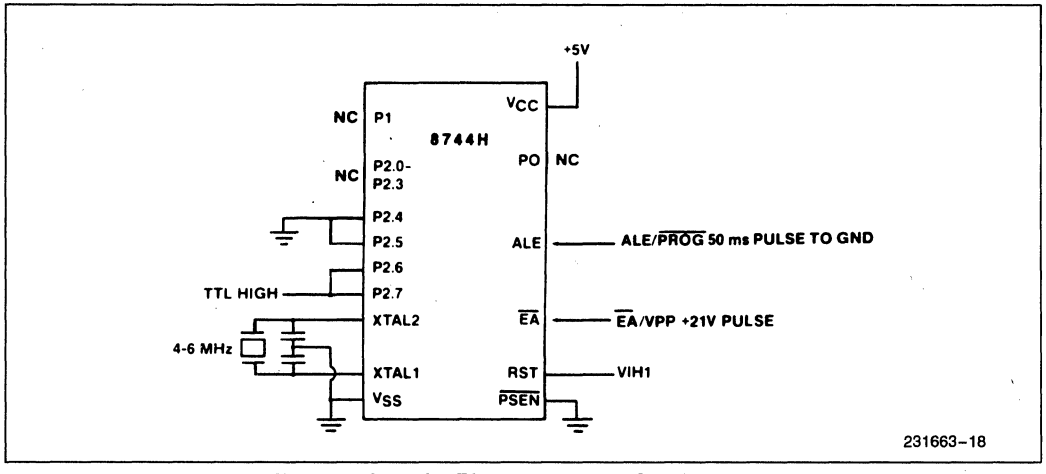

Figure 9. Security Bit Programming Configuration

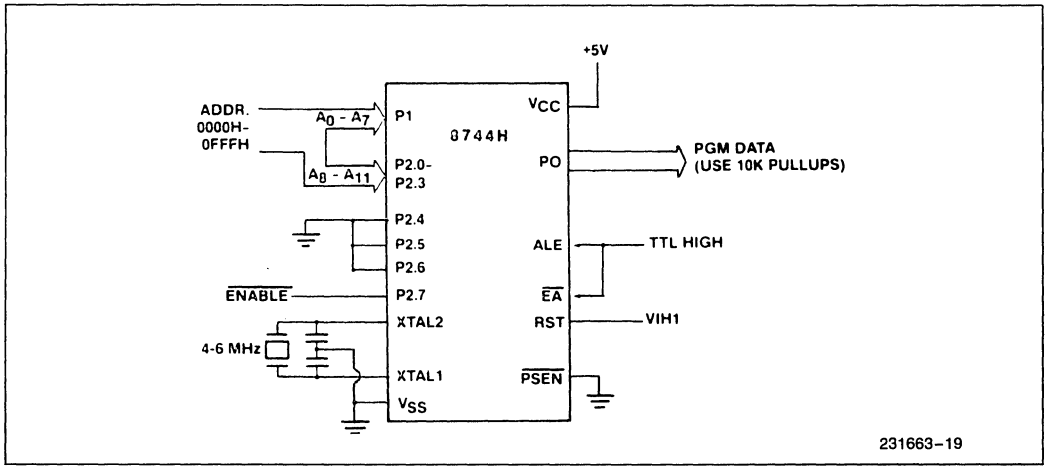

Figure 10. Program Verification Configuration

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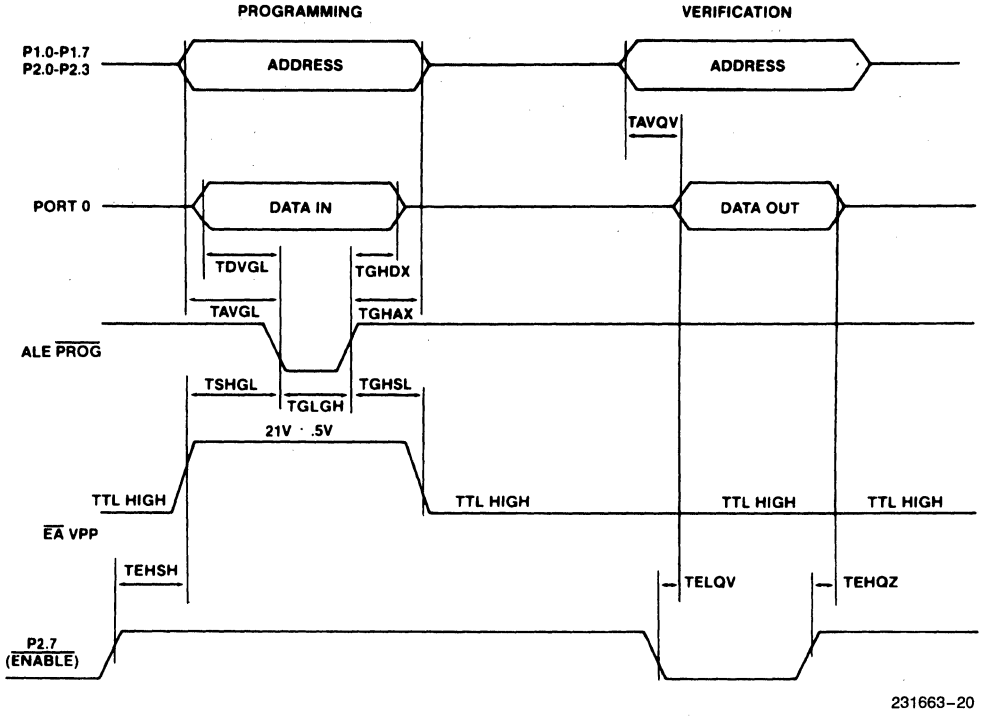
EPROM PROGRAMMING, SECURITY BIT PROGRAMMING AND VERIFICATION CHARACTERISTICS

TA = 21°C to 27°C, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	20.5	21.5	V
IPP	Programming Current		30	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	$\overline{ENABLE}$ High to Vpp	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$	10		μsec
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		μsec
TGLGH	$\overline{PROG}$ Width	45	55	msec
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ to Data Valid		48TCLCL	
TEHQZ	Data Float after $\overline{ENABLE}$	0	48TCLCL	

EPROM PROGRAMMING, SECURITY BIT PROGRAMMING AND VERIFICATION WAVEFORMS



MCS®-80/85 Data Sheets 13

8080A/8080A-1/8080A-2
8-BIT N-CHANNEL MICROPROCESSOR

- **TTL Drive Capability**
- **2 μs (−1:1.3 μs, −2:1.5 μs) Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **6 General Purpose Registers and an Accumulator**
- **16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary, and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**
- **Available in EXPRESS — Standard Temperature Range**
- **Available in 40-Lead Cerdip and Plastic Packages**
  (See Packaging Spec. Order #231369)

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

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The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

NOTE:
The 8080A is functionally and electrically compatible with the Intel 8080.

November 1986
Order Number: 231453-001

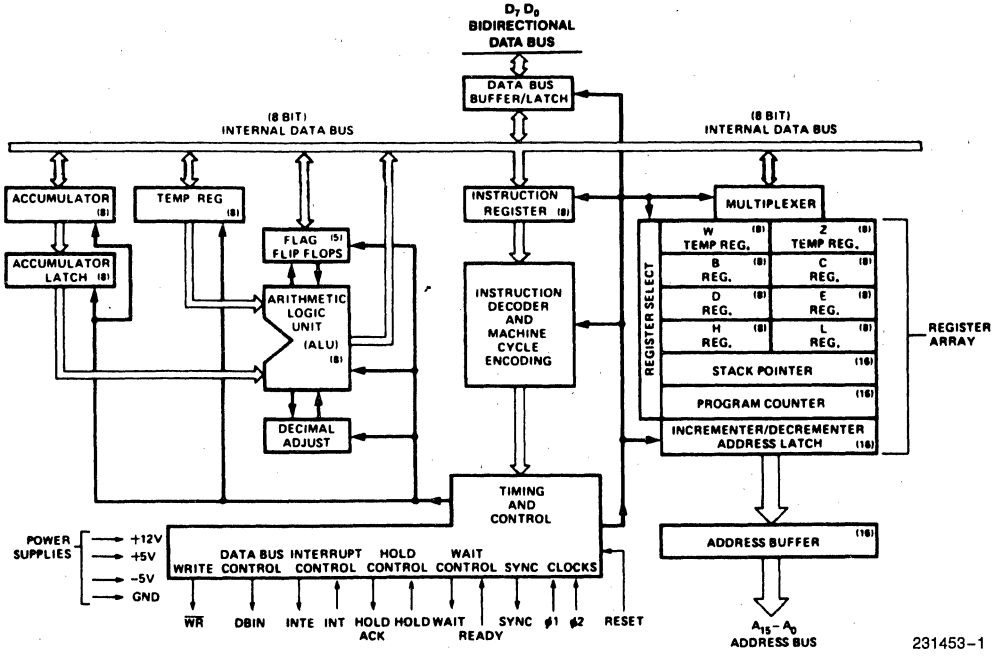


Figure 1. Block Diagram

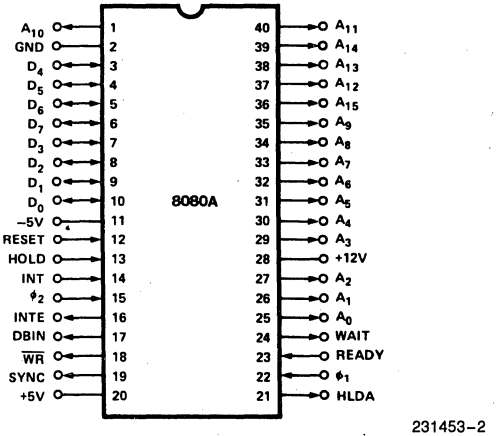


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
$A_{15}-A_0$	O	**ADDRESS BUS:** The address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.
D_7-D_0	I/O	**DATA BUS:** The data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.
SYNC	O	**SYNCHRONIZING SIGNAL:** The SYNC pin provides a signal to indicate the beginning of each machine cycle.
DBIN	O	**DATA BUS IN:** The DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.
READY	I	**READY:** The READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.
WAIT	O	**WAIT:** The WAIT signal acknowledges that the CPU is in a WAIT state.
$\overline{WR}$	O	**WRITE:** The $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR} = 0$).
HOLD	I	**HOLD:** The HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these busses for the current machine cycle. It is recognized under the following conditions: • the CPU is in the HALT state. • the CPU is in the T2 or TW state and the READY signal is active. As a result of entering the HOLD state the CPU ADDRESS BUS ($A_{15}-A_0$) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.
HLDA	O	**HOLD ACKNOWLEDGE:** The HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at: • T3 for READ memory or input. • The Clock Period following T3 for WRITE memory or OUTPUT operation. In either case, the HLDA signal appears after the rising edge of ϕ_2.
INTE	O	**INTERRUPT ENABLE:** Indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.
INT	I	**INTERRUPT REQUEST:** The CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.
RESET[1]	I	**RESET:** While the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.
V_{SS}		**GROUND:** Reference.
V_{DD}		**POWER:** +12 ±5% V.
V_{CC}		**POWER:** +5 ±5% V.
V_{BB}		**POWER:** −5 ±5% V.
ϕ_1, ϕ_2		**CLOCK PHASES:** 2 externally supplied clock phases. (non TTL compatible)

NOTE:
1. The RESET signal must be active for a minimum of 3 clock cycles.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
All Input or Output Voltages with Respect to V_{BB} .....−0.3V to +20V
V_{CC}, V_{DD} and V_{SS} with Respect to V_{BB} .....−0.3V to +20V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

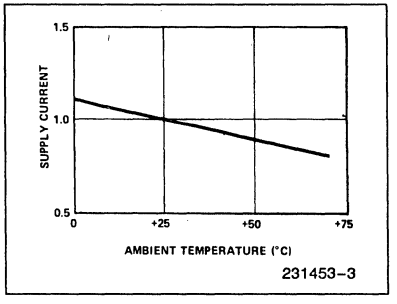
T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V; unless otherwise noted

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS} − 1		V_{SS} + 0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD} + 1	V	
V_{IL}	Input Low Voltage	V_{SS} − 1		V_{SS} + 0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9 mA on All Outputs, I_{OH} = −150 μA.
V_{OH}	Output High Voltage	3.7			V	
$I_{DD\ (AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation T_{CY} = 0.48 μs
$I_{CC\ (AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	
$I_{BB\ (AV)}$	Avg. Power Supply Current (V_{BB})		0.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \le V_{CLOCK} \le V_{DD}$
I_{DL}	Data Bus Leakage in Input Mode			−100 −2.0	μA mA	$V_{SS} \le V_{IN} \le V_{SS}$ + 0.8V V_{SS} + 0.8V $\le V_{IN} \le V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 −100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

CAPACITANCE

T_A = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = −5V

Symbol	Parameter	Typ	Max	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pF	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pF	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pF	Returned to V_{SS}



Typical Supply Current vs Temperature, Normalized
ΔI Supply/ΔT_A = −0.45%/°C

A.C. CHARACTERISTICS (8080A) T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V; unless otherwise noted

Symbol	Parameter	Min	Max	−1 Min	−1 Max	−2 Min	−2 Max	Unit	Test Condition
t_{CY}(3)	Clock Period	0.48	2.0	0.32	2.0	0.38	2.0	μs	
t_r, t_f	Clock Rise and Fall Time	0	50	0	25	0	50	ns	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		50		60		ns	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		145		175		ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0		0		0		ns	
t_{D2}	Delay ϕ_1 to ϕ_2	70		60		70		ns	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		60		70	ns		
t_{DA}	Address Output Delay From ϕ_2		200		150		175	ns	C_L = 100 pF
t_{DD}	Data Output Delay From ϕ_2		200		180		200	ns	
t_{DC}	Signal Output Delay From ϕ_1 or ϕ_2 (SYNC, WR, WAIT, HLDA)		120		110		120	ns	C_L = 50 pF
t_{DF}	DBIN Delay From ϕ_2	25	140	25	130	25	140	ns	
t_{DI}(1)	Delay for Input Bus to Enter Input Mode		t_{DF}		t_{DF}		t_{DF}	ns	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		10		20		ns	
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		120		130		ns	
t_{DH}(1)	Data Hold Time From ϕ_2 and DBIN	(1)		(1)		(1)		ns	
t_{IE}	INTE Output Delay From ϕ_2		200		200		200	ns	C_L = 50 pF
t_{RS}	READY Setup Time During ϕ_2	120		90		90		ns	
t_{HS}	HOLD Setup Time During ϕ_2	140		120		120		ns	
t_{IS}	INT Setup Time During ϕ_2	120		100		100		ns	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		0		0		ns	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120		120		120	ns	
t_{AW}	Address Stable Prior to WR	(5)		(5)		(5)		ns	
t_{DW}	Output Data Stable Prior to WR	(6)		(6)		(6)		ns	
t_{WD}	Output Data Stable From WR	(7)		(7)		(7)		ns	
t_{WA}	Address Stable From WR	(7)		(7)		(7)		ns	
t_{HF}	HLDA to Float Delay	(8)		(8)		(8)		ns	
t_{WF}	WR to Float Delay	(9)		(9)		(9)		ns	
t_{AH}	Address Hold Time After DBIN During HLDA	−20		−20		−20		ns	

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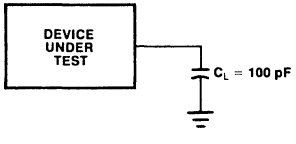
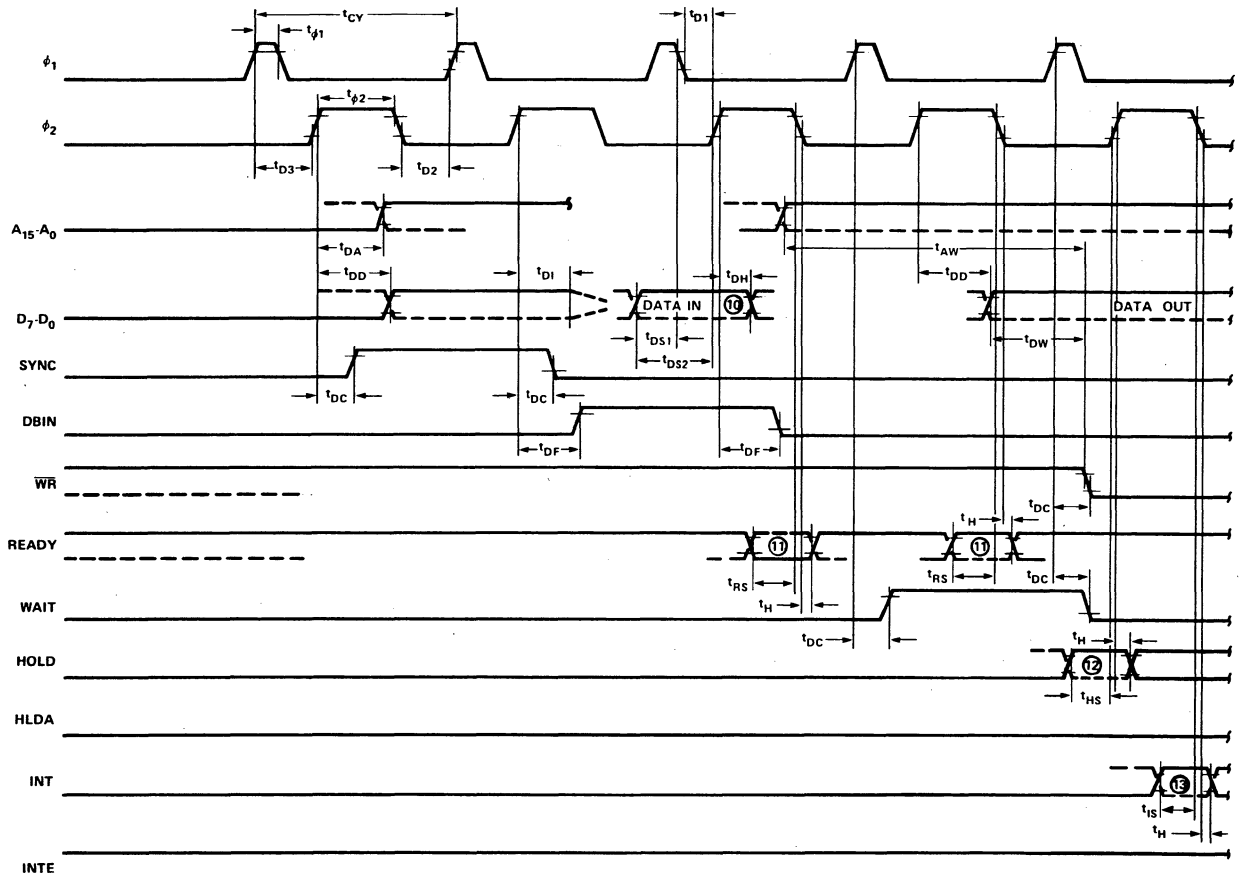
A.C. TESTING LOAD CIRCUIT



231453-4

C_L = 100 pF
C_L Includes Jig Capacitance

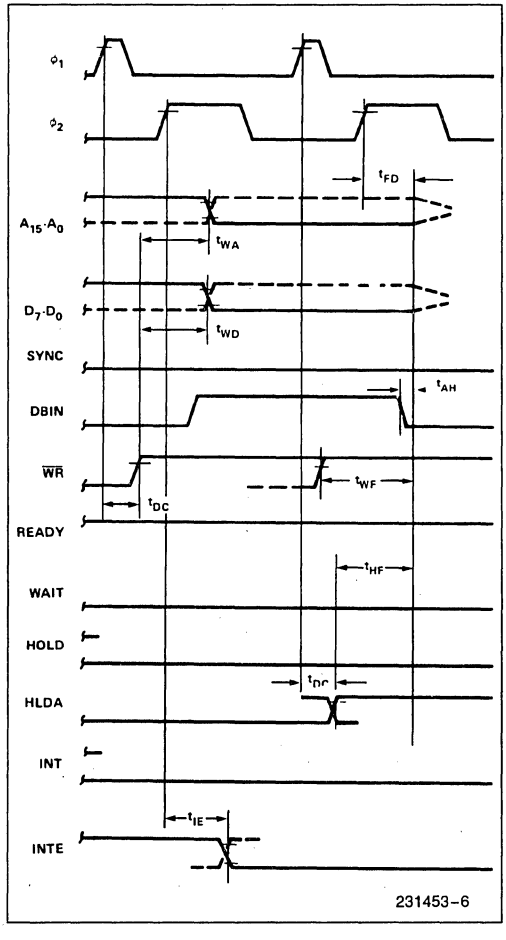
WAVEFORMS



231453-5

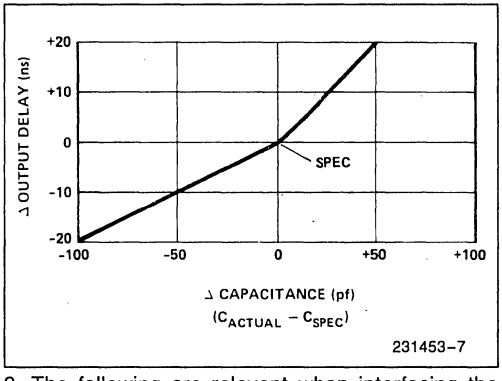
NOTE:
Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V

WAVEFORMS (Continued)



NOTES:
(Parenthesis gives −1, −2 specifications, respectively.)
1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured.
t_{DH} = 50 ns or t_{DF}, whichever is less.
2. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq$ 480 ns (−1:320 ns, − 2:380 ns).

Typical Δ Output Delay vs Δ Capacitance



3. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from 0.8V to 3.3V = 100 ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60 ns @ C_L = SPEC.
   c) If C_L = SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.
4. $t_{AW} = 2\ t_{CY} - t_{D3} - t_{r\phi2} - 140$ ns (−1:110 ns, − 2:130 ns).
5. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$ ns (−1:150 ns, − 2:170 ns).
6. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
7. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ ns.
8. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ ns.
9. Data in must be stable for this period during DBIN T_3. Both t_{DS1} and t_{DS2} must be satisfied.
10. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
11. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
12. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
13. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

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INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to they system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Immediate mode or I/O instructions
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Jump, call or direct load and store instructions
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS OR OPERAND 1	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS OR OPERAND 2	

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

Table 2. Instruction Set Summary

Mnemonic*	Instruction Code (1) D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description	Clock Cycles (2)
MOVE, LOAD, AND STORE			
MOVr1,r2	0 1 D D D S S S	Move register to register	5
MOV M,r	0 1 1 1 0 S S S	Move register to memory	7
MOV r,M	0 1 D D D 1 1 0	Move memory to register	7
MVI r	0 0 D D D 1 1 0	Move immediate register	7
MVI M	0 0 1 1 0 1 1 0	Move immediate memory	10
LXI B	0 0 0 0 0 0 0 1	Load immediate register Pair B & C	10
LXI D	0 0 0 1 0 0 0 1	Load immediate register Pair D & E	10
LXI H	0 0 1 0 0 0 0 1	Load immediate register Pair H & L	10
STAX B	0 0 0 0 0 0 1 0	Store A indirect	7
STAX D	0 0 0 1 0 0 1 0	Store A indirect	7
LDAX B	0 0 0 0 1 0 1 0	Load A indirect	7
LDAX D	0 0 0 1 1 0 1 0	Load A indirect	7
STA	0 0 1 1 0 0 1 0	Store A direct	13
LDA	0 0 1 1 1 0 1 0	Load A direct	13
SHLD	0 0 1 0 0 0 1 0	Store H & L direct	16
LHLD	0 0 1 0 1 0 1 0	Load H & L direct	16
XCHG	1 1 1 0 1 0 1 1	Exchange D & E, H & L Registers	4
STACK OPS			
PUSH B	1 1 0 0 0 1 0 1	Push register Pair B & C on stack	11
PUSH D	1 1 0 1 0 1 0 1	Push register Pair D & E on stack	11
PUSH H	1 1 1 0 0 1 0 1	Push register Pair H & L on stack	11
PUSH PSW	1 1 1 1 0 1 0 1	Push A and Flags on stack	11
POP B	1 1 0 0 0 0 0 1	Pop register Pair B & C off stack	10
POP D	1 1 0 1 0 0 0 1	Pop register Pair D & E off stack	10
POP H	1 1 1 0 0 0 0 1	Pop register Pair H & L off stack	10
POP PSW	1 1 1 1 0 0 0 1	Pop A and Flags off stack	10
XTHL	1 1 1 0 0 0 1 1	Exchange top of stack, H & L	18
SPHL	1 1 1 1 1 0 0 1	H & L to stack pointer	5
LXI SP	0 0 1 1 0 0 0 1	Load immediate stack pointer	10
INX SP	0 0 1 1 0 0 1 1	Increment stack pointer	5
DCX SP	0 0 1 1 1 0 1 1	Decrement stack pointer	5
JUMP			
JMP	1 1 0 0 0 0 1 1	Jump unconditional	10
JC	1 1 0 1 1 0 1 0	Jump on carry	10
JNC	1 1 0 1 0 0 1 0	Jump on no carry	10
JZ	1 1 0 0 1 0 1 0	Jump on zero	10
JNZ	1 1 0 0 0 0 1 0	Jump on no zero	10
JP	1 1 1 1 0 0 1 0	Jump on positive	10
JM	1 1 1 1 1 0 1 0	Jump on minus	10
JPE	1 1 1 0 1 0 1 0	Jump on parity even	10
JPO	1 1 1 0 0 0 1 0	Jump on parity odd	10
PCHL	1 1 1 0 1 0 0 1	H & L to program counter	5
CALL			
CALL	1 1 0 0 1 1 0 1	Call unconditional	17
CC	1 1 0 1 1 1 0 0	Call on carry	11/17
CNC	1 1 0 1 0 1 0 0	Call on no carry	11/17
CZ	1 1 0 0 1 1 0 0	Call on zero	11/17
CNZ	1 1 0 0 0 1 0 0	Call on no zero	11/17
CP	1 1 1 1 0 1 0 0	Call on positive	11/17
CM	1 1 1 1 1 1 0 0	Call on minus	11/17
CPE	1 1 1 0 1 1 0 0	Call on parity even	11/17
CPO	1 1 1 0 0 1 0 0	Call on parity odd	11/17
RETURN			
RET	1 1 0 0 1 0 0 1	Return	10
RC	1 1 0 1 1 0 0 0	Return on carry	5/11
RNC	1 1 0 1 0 0 0 0	Return on no carry	5/11
RZ	1 1 0 0 1 0 0 0	Return on zero	5/11
RNZ	1 1 0 0 0 0 0 0	Return on no zero	5/11
RP	1 1 1 1 0 0 0 0	Return on positive	5/11
RM	1 1 1 1 1 0 0 0	Return on minus	5/11
RPE	1 1 1 0 0 0 0 0	Return on parity even	5/11
RPO	1 1 1 0 0 0 0 0	Return on parity odd	5/11
RESTART			
RST	1 1 A A A 1 1 1	Restart	11
INCREMENT AND DECREMENT			
INR r	0 0 D D D 1 0 0	Increment register	5
DCR r	0 0 D D D 1 0 1	Decrement register	5
INR M	0 0 1 1 0 1 0 0	Increment memory	10
DCR M	0 0 1 1 0 1 0 1	Decrement memory	10
INX B	0 0 0 0 0 0 1 1	Increment B & C registers	5
INX D	0 0 0 1 0 0 1 1	Increment D & E registers	5
INX H	0 0 1 0 0 0 1 1	Increment H & L registers	5
DCX B	0 0 0 0 1 0 1 1	Decrement B & C	5
DCX D	0 0 0 1 1 0 1 1	Decrement D & E	5
DCX H	0 0 1 0 1 0 1 1	Decrement H & L	5
ADD			
ADD r	1 0 0 0 0 S S S	Add register to A	4
ADC r	1 0 0 0 1 S S S	Add register to A with carry	4
ADD M	1 0 0 0 0 1 1 0	Add memory to A	7
ADC M	1 0 0 0 1 1 1 0	Add memory to A with carry	7
ADI	1 1 0 0 0 1 1 0	Add immediate to A	7
ACI	1 1 0 0 1 1 1 0	Add immediate to A with carry	7
DAD B	0 0 0 0 1 0 0 1	Add B & C to H & L	10
DAD D	0 0 0 1 1 0 0 1	Add D & E to H & L	10
DAD H	0 0 1 0 1 0 0 1	Add H & L to H & L	10
DAD SP	0 0 1 1 1 0 0 1	Add stack pointer to H & L	10

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Table 2. Instruction Set Summary (Continued)

Mnemonic*	Instruction Code (1) D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description	Clock Cycles (2)
SUBTRACT			
SUB r	1 0 0 1 0 S S S	Subtract register from A	4
SBB r	1 0 0 1 1 S S S	Subtract register from A with borrow	4
SUB M	1 0 0 1 0 1 1 0	Subtract memory from A	7
SBB M	1 0 0 1 1 1 1 0	Subtract memory from A with borrow	7
SUI	1 1 0 1 0 1 1 0	Subtract immediate from A	7
SBI	1 1 0 1 1 1 1 0	Subtract immediate from A with borrow	7
LOGICAL			
ANA r	1 0 1 0 0 S S S	And register with A	4
XRA r	1 0 1 0 1 S S S	Exclusive or register with A	4
ORA r	1 0 1 1 0 S S S	Or register with A	4
CMP r	1 0 1 1 1 S S S	Compare register with A	4
ANA M	1 0 1 0 0 1 1 0	And memory with A	7
XRA M	1 0 1 0 1 1 1 0	Exclusive Or memory with A	7
ORA M	1 0 1 1 0 1 1 0	Or memory with A	7
CMP M	1 0 1 1 1 1 1 0	Compare memory with A	7
ANI	1 1 1 0 0 1 1 0	And immediate with A	7
XRI	1 1 1 0 1 1 1 0	Exclusive Or immediate with A	7
ORI	1 1 1 1 0 1 1 0	Or immediate with A	7
CPI	1 1 1 1 1 1 1 0	Compare immediate with A	7

Mnemonic*	Instruction Code (1) D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description	Clock Cycles (2)
ROTATE			
RLC	0 0 0 0 0 1 1 1	Rotate A left	4
RRC	0 0 0 0 1 1 1 1	Rotate A right	4
RAL	0 0 0 1 0 1 1 1	Rotate A left through carry	4
RAR	0 0 0 1 1 1 1 1	Rotate A right through carry	4
SPECIALS			
CMA	0 0 1 0 1 1 1 1	Complement A	4
STC	0 0 1 1 0 1 1 1	Set carry	4
CMC	0 0 1 1 1 1 1 1	Complement carry	4
DAA	0 0 1 0 0 1 1 1	Decimal adjust A	4
INPUT/OUTPUT			
IN	1 1 0 1 1 0 1 1	Input	10
OUT	1 1 0 1 0 0 1 1	Output	10
CONTROL			
EI	1 1 1 1 1 0 1 1	Enable Interrupts	4
DI	1 1 1 1 0 0 1 1	Disable Interrupt	4
NOP	0 0 0 0 0 0 0 0	No-operation	4
HLT	0 1 1 1 0 1 1 0	Halt	7

NOTES:
1. DDD or SSS: B = 000, C = 001, D = 010, E = 011, H = 100, L = 101, Memory = 110, A = 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

8085AH/8085AH-2/8085AH-1
8-BIT HMOS MICROPROCESSORS

- **Single +5V Power Supply with 10% Voltage Margins**
- **3 MHz, 5 MHz and 6 MHz Selections Available**
- **20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz**
- **1.3 μs Instruction Cycle (8085AH); 0.8 μs (8085AH-2); 0.67 μs (8085AH-1)**
- **100% Software Compatible with 8080A**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One Is Non-Maskable) Plus an 8080A-Compatible Interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64K Bytes of Memory**
- **Available in 40-Lead Cerdip and Plastic Packages**
  (See Packaging Spec., Order #231369)

The Intel 8085AH is a complete 8-bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085AH (CPU), 8156H (RAM/IO) and 8755A (EPROM/IO)] while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085AH.

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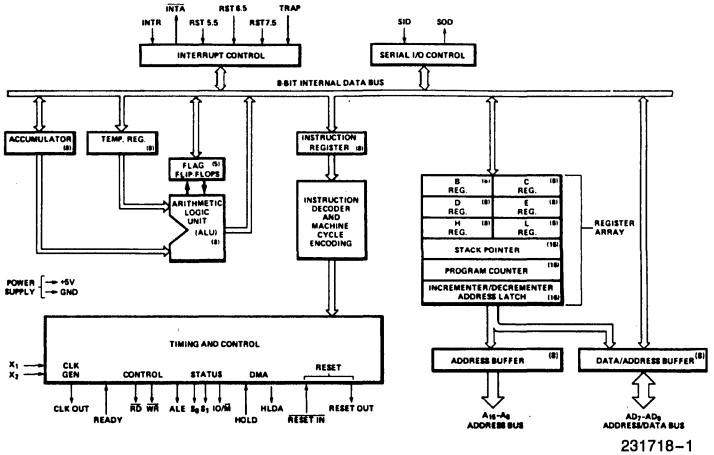
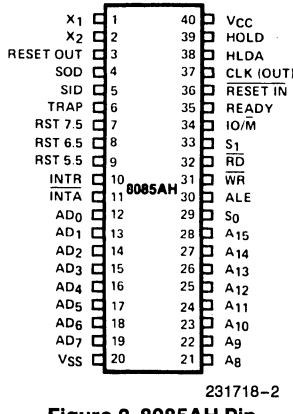
The 8085AH incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a higher level of system integration.

The 8085AH uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of 8155H/8156H/8755A memory products allow a direct interface with the 8085AH.



231718-1

Figure 1. 8085AH CPU Functional Block Diagram



231718-2

Figure 2. 8085AH Pin Configuration

September 1987
Order Number: 231718-001

Table 1. Pin Description

Symbol	Type	Name and Function
A_8–A_{15}	O	**ADDRESS BUS:** The most significant 8 bits of memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7}	I/O	**MULTIPLEXED ADDRESS/DATA BUS:** Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE	O	**ADDRESS LATCH ENABLE:** It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1 and IO/$\overline{M}$	O	**MACHINE CYCLE STATUS:** **IO/$\overline{M}$ S_1 S_0 Status** 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge * 0 0 Halt * X X Hold * X X Reset * = 3-state (high impedance) X = unspecified S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$	O	**READ CONTROL:** A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	O	**WROTE CONTROL:** A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY	I	**READY:** If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	I	**HOLD:** Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	O	**HOLD ACKNOWLEDGE:** Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HILDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.
INTR	I	**INTERRUPT REQUEST:** Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

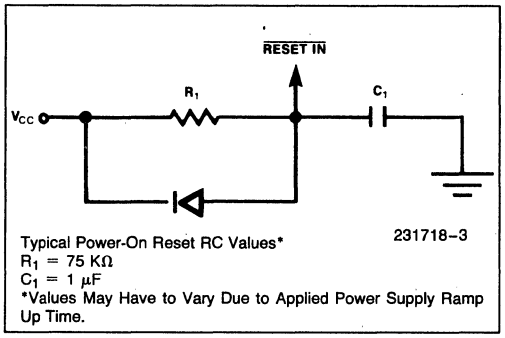
Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
$\overline{INTA}$	O	**INTERRUPT ACKNOWLEDGE:** Is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	I	**RESTART INTERRUPTS:** These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupt is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP	I	**TRAP:** Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5–7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.)
$\overline{RESET\ IN}$	I	**RESET IN:** Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, $\overline{RESET\ IN}$ must remain low for at least 10 ms after minimum V_{CC} has been reached. For proper reset operation after the power-up duration, $\overline{RESET\ IN}$ should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as $\overline{RESET\ IN}$ is applied.
RESET OUT	O	**RESET OUT:** Reset Out indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2	I	**X_1 and X_2:** Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	O	**CLOCK:** Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID	I	**SERIAL INPUT DATA LINE:** The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	O	**SERIAL OUTPUT DATA LINE:** The output SOD is set or reset as specified by the SIM instruction.
V_{CC}		**POWER:** +5 volt supply.
V_{SS}		**GROUND:** Reference.

Table 2. Interrupt Priority, Restart Address and Sensitivity

Name	Priority	Address Branched to(1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising Edge AND High Level until Sampled
RST 7.5	2	3CH	Rising Edge (Latched)
RST 6.5	3	34H	High Level until Sampled
RST 5.5	4	2CH	High Level until Sampled
INTR	5	(Note 2)	High Level until Sampled

NOTES:
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.



Typical Power-On Reset RC Values*
R_1 = 75 KΩ
C_1 = 1 μF
*Values May Have to Vary Due to Applied Power Supply Ramp Up Time.

Figure 3. Power-On Reset Circuit

FUNCTIONAL DESCRIPTION

The 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel, depletion load, silicon gate technology (HMOS), and requires a single +5V supply. Its basic clock speed is 3 MHz (8085AH), 5 MHz (8085AH-2), or 6 MHz (8085-AH-1), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (8085AH), a RAM/IO (8156H), and an EPROM/IO chip (8755A).

The 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 Bits
PC	Program Counter	16-Bit Address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8-Bits x 6 or 16 Bits x 3
SP	Stack Pointer	16-Bit Address
Flags or F	Flag Register	5 Flags (8-Bit Space)

The 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085AH provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085AH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

INTERRUPT AND SERIAL I/O

The 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupt cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 2.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive.*

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$. (See SIM, Chapter 5 of the 8080/8085 User's Manual.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the

highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive.* The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 4 illustrates the TRAP interrupt request circuitry within the 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

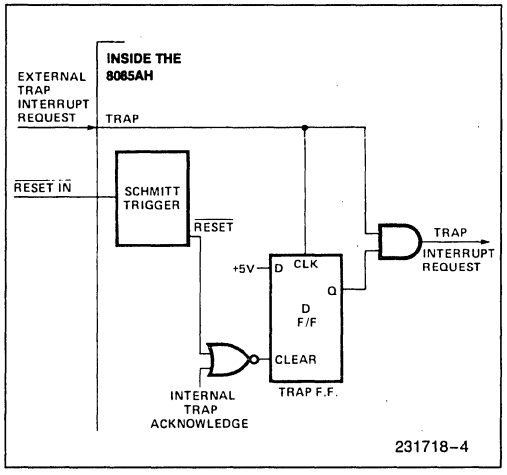


Figure 4. TRAP and RESET In Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5–7.5 will provide current Interrupt Enable status, revealing that interrupts are disabled. See the description of the RIM instruction in the 8080/8085 Family User's Manual.

The serial I/O system is also controlled by the RIM and SIM instruction. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X_1 AND X_2 INPUTS

You may drive the clock inputs of the 8085AH, 8085AH-2, or 8085AH-1 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The crystal frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085AH is operated with a 6 MHz crystal (for 3 MHz clock), the 8085AH-2 operated with a 10 MHz crystal (for 5 MHz clock), and the 8085AH-1 can be operated with a 12 MHz crystal (for 6 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
C_L (load capacitance) $\leq$ 30 pF
C_S (Shunt capacitance) $\leq$ 7 pF
R_S (equivalent shunt resistance) $\leq 75\Omega$
Drive level: 10 mW
Frequency tolerance: $\pm 0.005\%$ (suggested)

Note the use of the 20 pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC citcuit may be used as the frequency-determining network for the 8085AH, providing that its frequency tolerance of approximately $\pm 10\%$ is acceptable. The components are chosen from the formula:

$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085AH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 5 shows the recommended clock driver circuits. Note in d and e that pullup resistors are required to assure that the high level voltage of the input is at least 4V and maximum low level voltage of 0.8V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figure 5d). If the driving frequency is from 6 MHz to 12 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a push-pull source (Figure 5e). To prevent self-oscillation of the 8085AH, be sure that X_2 is not coupled back to X_1 through the driving circuit.

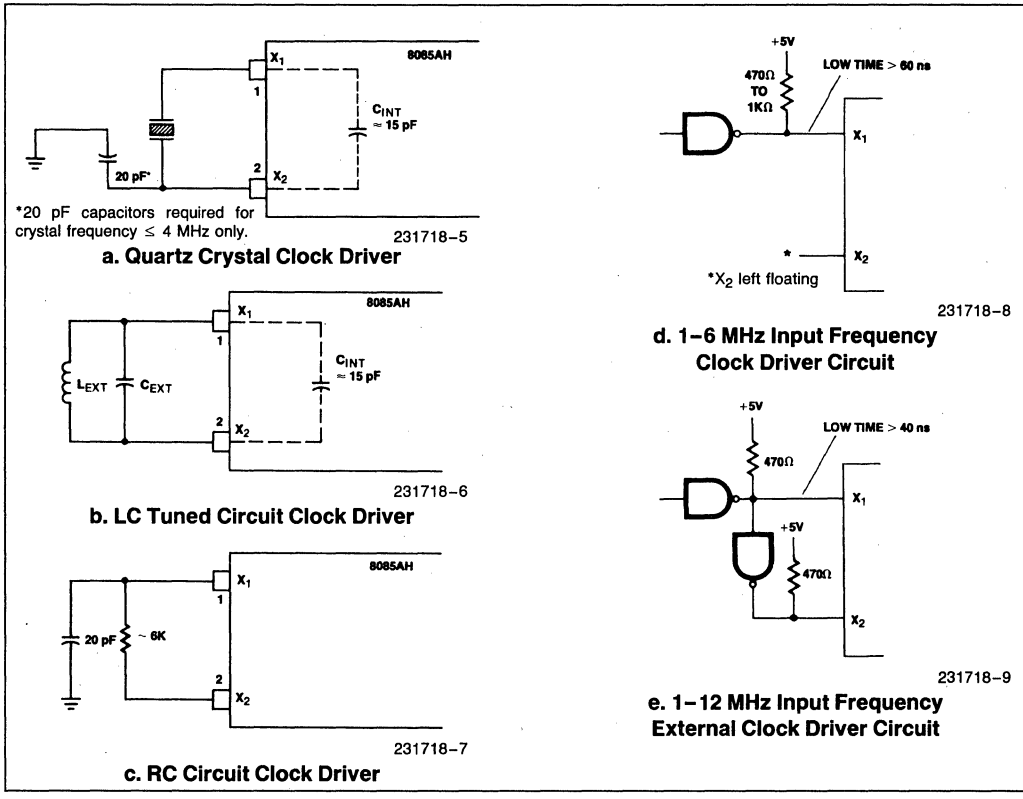


Figure 5. Clock Driver Circuits

GENERATING AN 8085AH WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 6 may be used to insert one WAIT state in each 8085AH machine cycle.

The D flip-flops should be chosen so that
- CLK is rising edge-triggered
- CLEAR is low-level active.

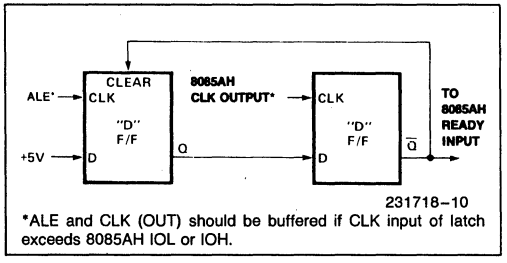


Figure 6. Generation of a Wait State for 8085AH CPU

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085AH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

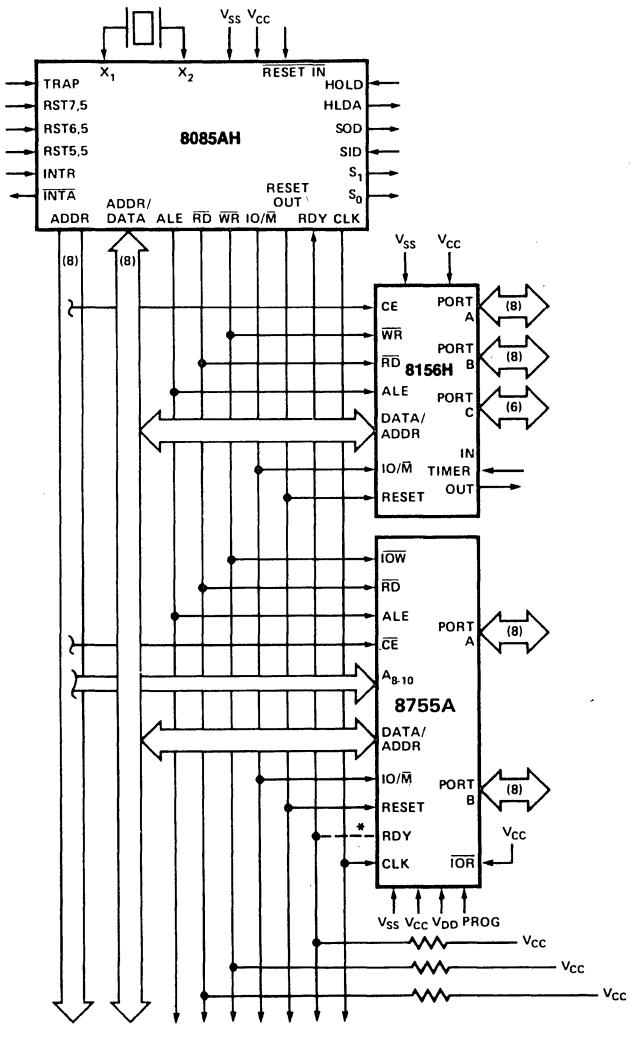
The 8085AH family includes memory components, which are directly compatible to the 8085AH CPU. For example, a system consisting of the three chips, 8085AH, 8156H and 8755A will have the following features:

- 2K Bytes EPROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 7.

In addition to the standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 8 shows the system configuration of Memory Mapped I/O using 8085AH.

The 8085AH CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8-bit latch as shown in Figure 9.



***NOTE:**
Optional Connection

Figure 7. 8085AH Minimum System (Standard I/O Technique)

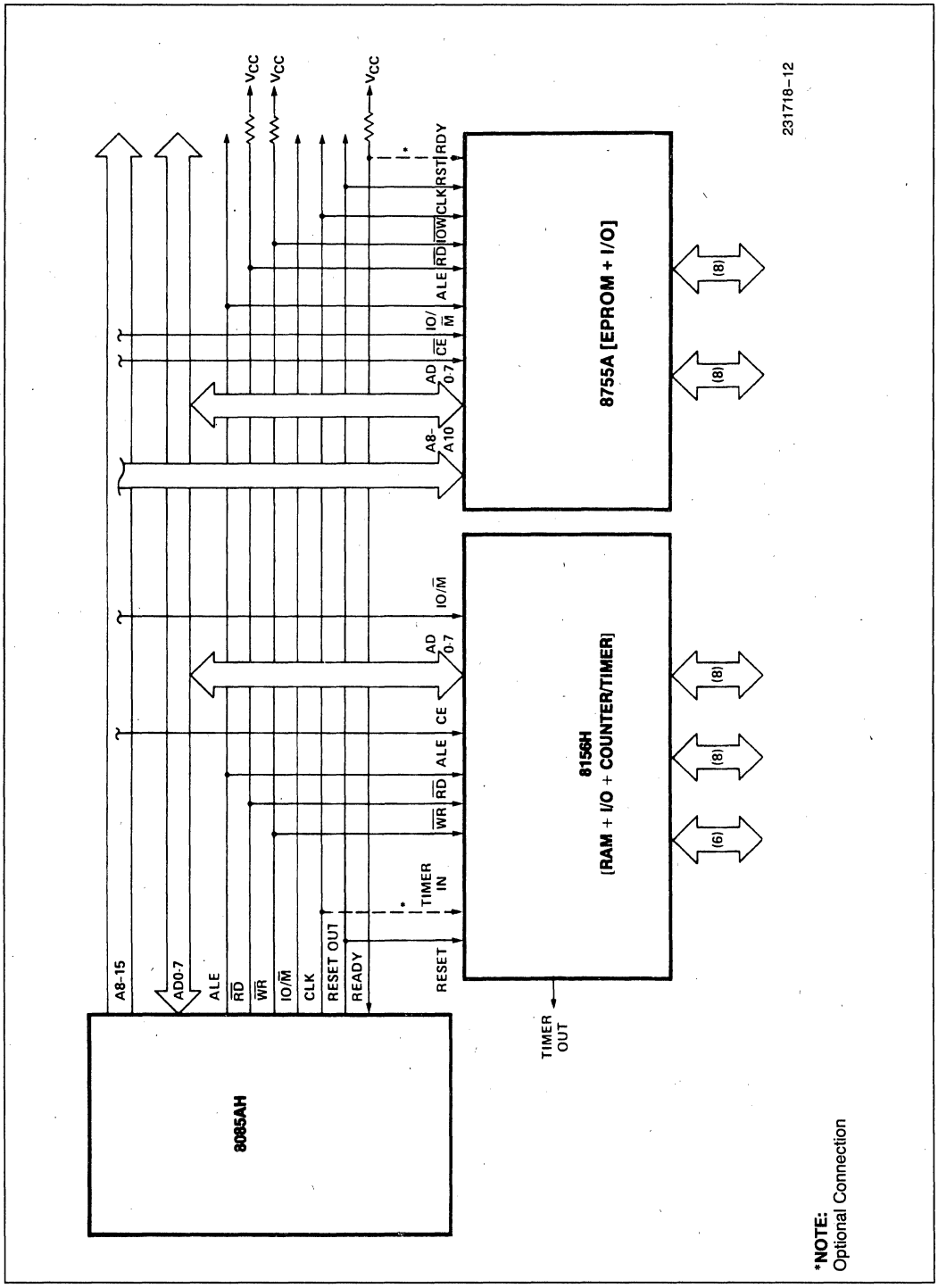


Figure 8. 8085 Minimum System (Memory Mapped I/O)

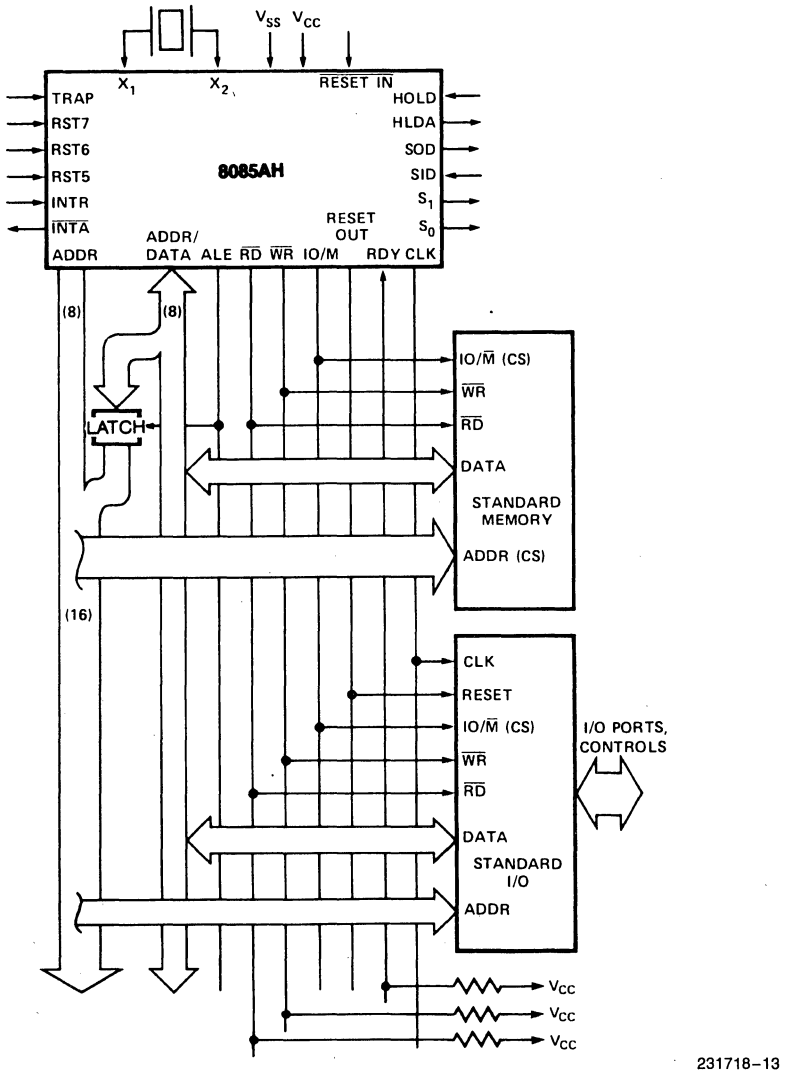


Figure 9. 8085 System (Using Standard Memories)

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BASIC SYSTEM TIMING

The 8085AH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 10 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 3.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless $\overline{WAIT}$ or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 4.

Table 3. 8085AH Machine Cycle Chart

Machine Cycle			Status			Control		
			IO/$\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI):	DAD	0	1	0	1	1	1
		ACK.OF RST,TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Table 4. 8085AH Machine State Chart

Machine State	Status & Buses				Control		
	S1,S0	IO/$\overline{M}$	A_8–A_{15}	AD_0–AD_7	$\overline{RD}$, $\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified
*ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
†$IO/\overline{M}$ = 1 during T_4–T_6 of INA machine cycle.

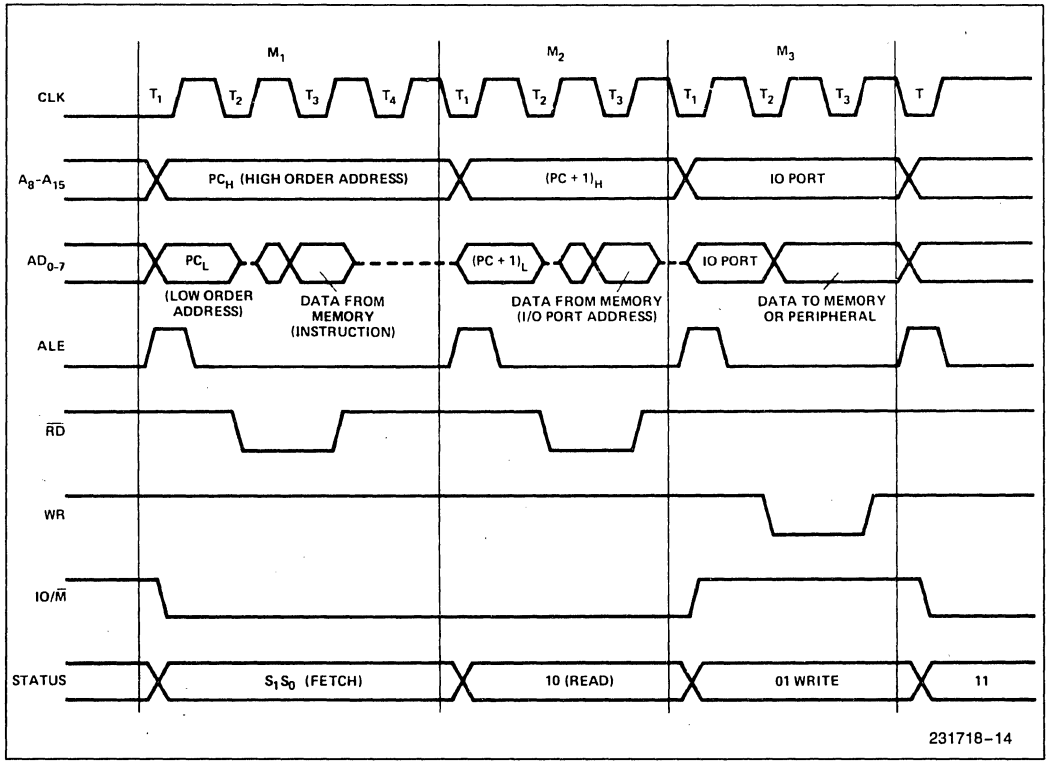

Figure 10. 8085AH Basic System Timing

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin
with Respect to Ground.....−0.5V to +7V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

8085AH, 8085AH-2: T_A = 0°C to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V; unless otherwise specified*
8085AH-1: T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V; unless otherwise specified*

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current		135	mA	8085AH, 8085AH-2
			200	mA	8085AH-1
I_{IL}	Input Leakage		±10	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \le V_{OUT} \le V_{CC}$
V_{ILR}	Input Low Level, RESET	−0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} + 0.5	V	
V_{HY}	Hysteresis, RESET	0.15		V	

A.C. CHARACTERISTICS

8085AH, 8085AH-2: T_A = 0°C to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V*
8085AH-1: T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V

Symbol	Parameter	8085AH (2)		8085AH-2 (2)		8085AH-1 (2)		Units
		Min	Max	Min	Max	Min	Max	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	167	2000	ns
t_1	CLK Low Time (Standard CLK Loading)	80		40		20		ns
t_2	CLK High Time (Standard CLK Loading)	120		70		50		ns
t_r, t_f	CLK Rise and Fall Time		30		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	20	120	20	100	20	100	ns
t_{XKF}	X_1 Rising to CLK Falling	20	150	20	110	20	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control (1)	270		115		70		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		60		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350		225	ns
t_{AFR}	Address Float after Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0		0	ns
t_{AL}	A_{8-15} Valid before Trailing Edge of ALE (1)	115		50		25		ns

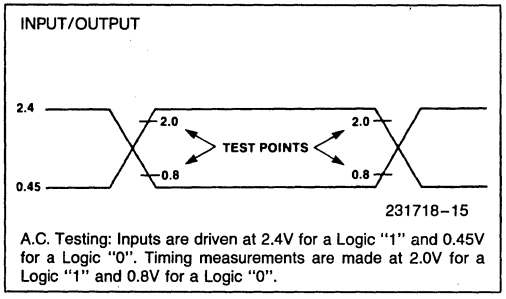
***NOTE:**
For Extended Temperature EXPRESS use M8085AH Electricals Parameters.

A.C. CHARACTERISTICS (Continued)

Symbol	Parameter	8085AH (2)		8085AH-2 (2)		8085AH-1 (2)		Units
		Min	Max	Min	Max	Min	Max	
t_{ALL}	A_{0-7} Valid before Trailing Edge of ALE	90		50		25		ns
t_{ARY}	READY Valid from Address Valid		220		100		40	ns
t_{CA}	Address (A_{8-15}) Valid after Control	120		60		30		ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		230		150		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		0		ns
t_{DW}	Data Valid to Trialing Edge of $\overline{WRITE}$	420		230		140		ns
t_{HABE}	HLDA to Bus Enable		210		150		150	ns
t_{HABF}	Bus Float after HLDA		210		150		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		0		ns
t_{HDH}	HOLD Hold Time	0		0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		120		ns
t_{INH}	INTR Hold Time	0		0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		150		ns
t_{LA}	Address Hold Time after ALE	100		50		20		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		25		ns
t_{LCK}	ALE Low During CLK High	100		50		15		ns
t_{LDR}	ALE to Valid Data during Read		460		270		175	ns
t_{LDW}	ALE to Valid Data during Write		200		140		110	ns
t_{LL}	ALE Width	140		80		50		ns
t_{LRY}	ALE to READY Stable		110		30		10	ns
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		90		50		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300		150		75	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		160		ns
t_{RDH}	Data Hold Time after $\overline{READ}$ $\overline{INTA}$	0		0		0		ns
t_{RYH}	READY Hold Time	0		0		5		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		100		ns
t_{WD}	Data Valid after Trailing Edge of $\overline{WRITE}$	100		60		30		ns
t_{WDL}	LEADING Edge of $\overline{WRITE}$ to Data Valid		40		20		30	ns

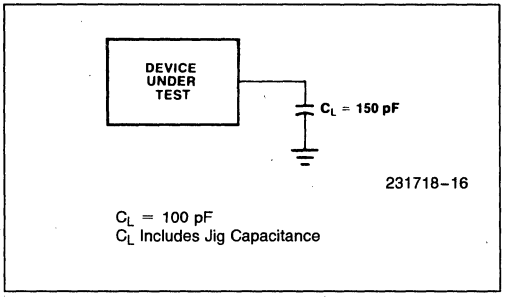
NOTES:
1. A_8–A_{15} address Specs apply IO/$\overline{M}$, S_0, and S_1 except A_8–A_{15} are undefined during T_4–T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
2. *Test Conditions:* t_{CYC} = 320 ns (8085AH)/200 ns (8085AH-2);/167 ns (8085AH-1); C_L = 150 pF.
3. For all output timing where C ≠ 150 pF use the following correction factors:
   25 pF ≤ C_L < 150 pF: −0.10 ns/pF
   150 pF < C_L ≤ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. To calculate timing specifications at other values of t_{CYC} use Table 5.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

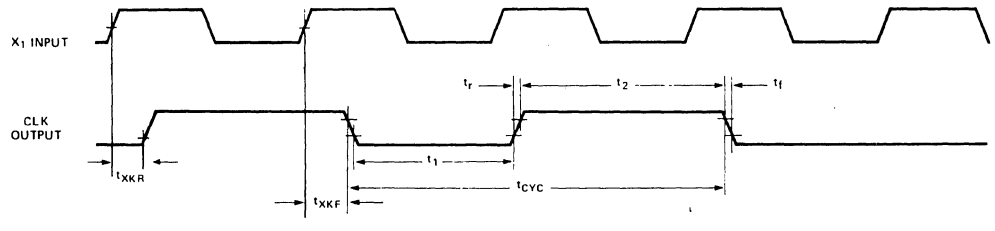
Table 5. Bus Timing Specification as a T_{CYC} Dependent

Symbol	8085AH	8085AH-2	8085AH-1	
t_{AL}	(1/2)T − 45	(1/2)T − 50	(1/2)T − 58	Minimum
t_{LA}	(1/2)T − 60	(1/2)T − 50	(1/2)T − 63	Minimum
t_{LL}	(1/2)T − 20	(1/2)T − 20	(1/2)T − 33	Minimum
t_{LCK}	(1/2)T − 60	(1/2)T − 50	(1/2)T − 68	Minimum
t_{LC}	(1/2)T − 30	(1/2)T − 40	(1/2)T − 58	Minimum
t_{AD}	(5/2 + N)T − 225	(5/2 + N)T − 150	(5/2 + N)T − 192	Maximum
t_{RD}	(3/2 + N)T − 180	(3/2 + N)T − 150	(3/2 + N)T − 175	Maximum
t_{RAE}	(1/2)T − 10	(1/2)T − 10	(1/2)T − 33	Minimum
t_{CA}	(1/2)T − 40	(1/2)T − 40	(1/2)T − 53	Minimum
t_{DW}	(3/2 + N)T − 60	(3/2 + N)T − 70	(3/2 + N)T − 110	Minimum
t_{WD}	(1/2)T − 60	(1/2)T − 40	(1/2)T − 53	Minimum
t_{CC}	(3/2 + N)T − 80	(3/2 + N)T − 70	(3/2 + N)T − 100	Minimum
t_{CL}	(1/2)T − 110	(1/2)T − 75	(1/2)T − 83	Minimum
t_{ARY}	(3/2)T − 260	(3/2)T − 200	(3/2)T − 210	Maximum
t_{HACK}	(1/2)T − 50	(1/2)T − 60	(1/2)T − 83	Minimum
t_{HABF}	(1/2)T + 50	(1/2)T + 50	(1/2)T + 67	Maximum
t_{HABE}	(1/2)T + 50	(1/2)T + 50	(1/2)T + 67	Maximum
t_{AC}	(2/2)T − 50	(2/2)T − 85	(2/2)T − 97	Minimum
t_1	(1/2)T − 80	(1/2)T − 60	(1/2)T − 63	Minimum
t_2	(1/2)T − 40	(1/2)T − 30	(1/2)T − 33	Minimum
t_{RV}	(3/2)T − 80	(3/2)T − 80	(3/2)T − 90	Minimum
t_{LDR}	(4/2 + N)T − 180	(4/2)T − 130	(4/2)T − 159	Maximum

NOTE:
N is equal to the total WAIT states. T = t_{CYC}.

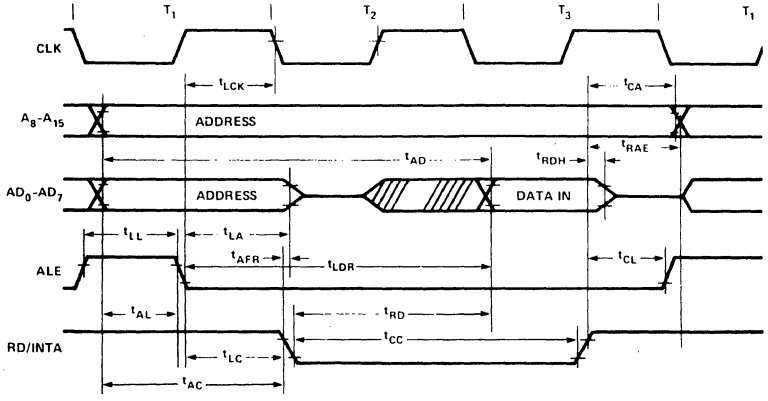
WAVEFORMS

CLOCK



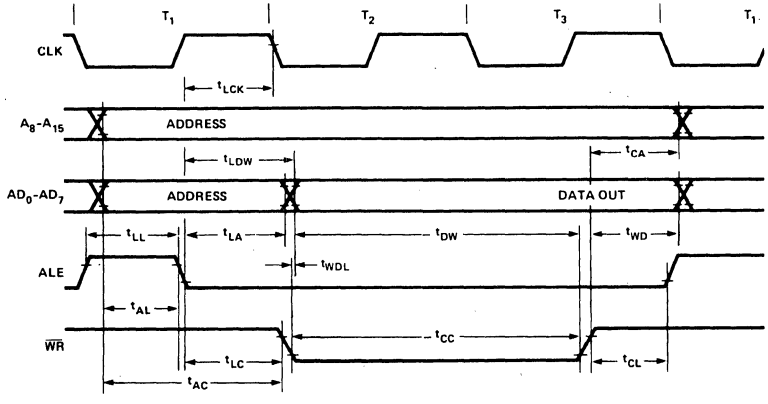
231718-17

READ



231718-18

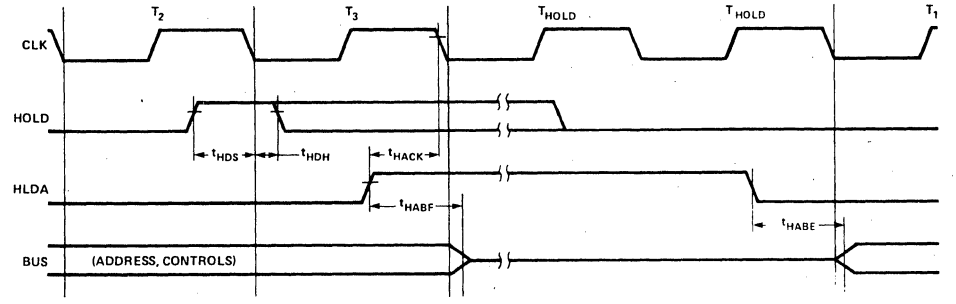
WRITE



231718-19

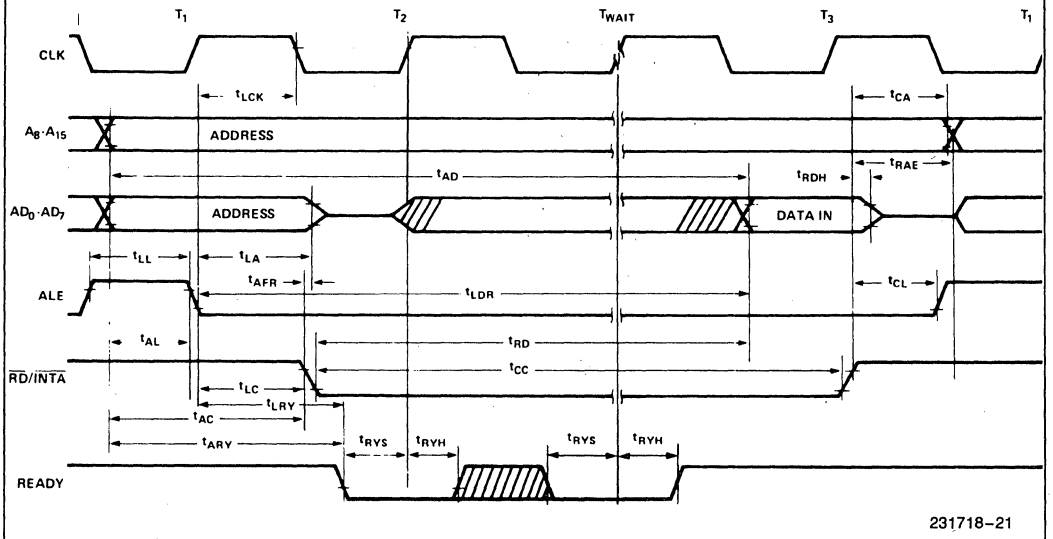
WAVEFORMS (Continued)

HOLD



231718-20

READ OPERATION WITH WAIT CYCLE (TYPICAL)—SAME READY TIMING APPLIES TO WRITE

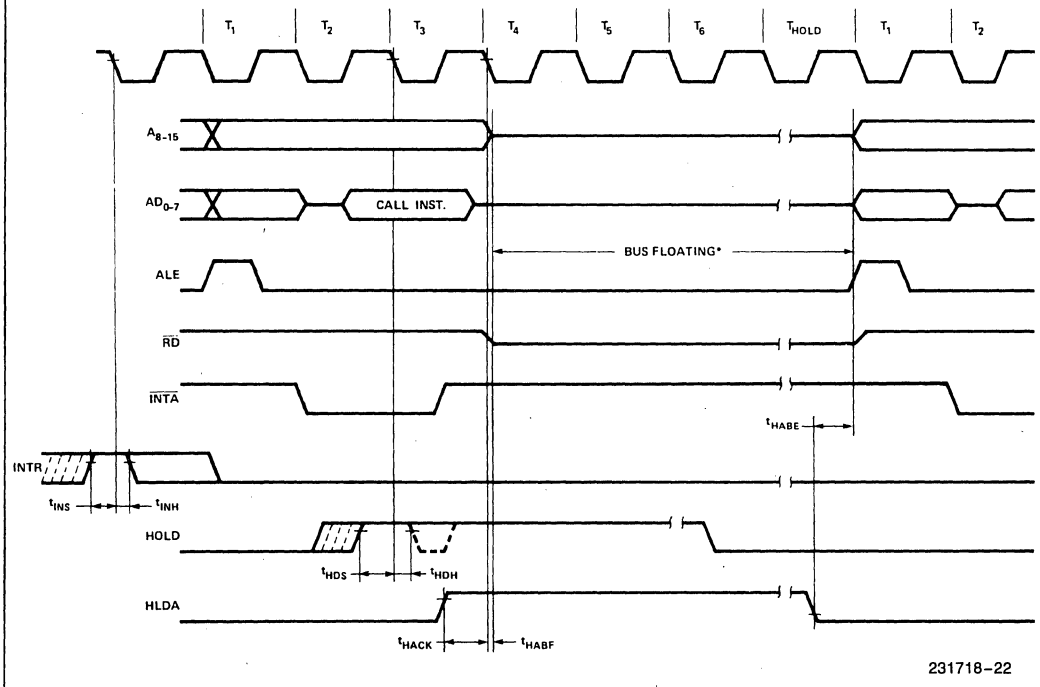


231718-21

NOTE:
1. Ready must remain stable during setup and hold times.

WAVEFORMS (Continued)

INTERRUPT AND HOLD



***NOTE:**
IO/$\overline{M}$ is also floating during this time.

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Table 6. Instruction Set Summary

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
MOVE, LOAD AND STORE		
MOVr1 r2	0 1 D D D S S S	Move register to register
MOV M.r	0 1 1 1 0 S S S	Move register to memory
MOV r.M	0 1 D D D 1 1 0	Move memory to register
MVI r	0 0 D D D 1 1 0	Move immediate register
MVI M	0 0 1 1 0 1 1 0	Move immediate memory
LXI B	0 0 0 0 0 0 0 1	Load immediate register Pair B & C
LXI D	0 0 0 1 0 0 0 1	Load immediate register Pair D & E
LXI H	0 0 1 0 0 0 0 1	Load immediate register Pair H & L
STAX B	0 0 0 0 0 0 1 0	Store A indirect
STAX D	0 0 0 1 0 0 1 0	Store A indirect
LDAX B	0 0 1 0 1 0 1 0	Load A indirect
LDAX D	0 0 0 1 1 0 1 0	Load A indirect
STA	0 0 1 1 0 0 1 0	Store A direct
LDA	0 0 1 1 1 0 1 0	Load A direct
SHLD	0 0 1 0 0 0 1 0	Store H & L direct
LHLD	0 0 1 0 1 0 1 0	Load H & L direct
XCHG	1 1 1 0 1 0 1 1	Exchange D & E, H & L Registers
STACK OPS		
PUSH B	1 1 0 0 0 1 0 1	Push register Pair B & C on stack
PUSH D	1 1 0 1 0 1 0 1	Push register Pair D & E on stack
PUSH H	1 1 1 0 0 1 0 1	Push register Pair H & L on stack
PUSH PSW	1 1 1 1 0 1 0 1	Push A and Flags on stack
POP B	1 1 0 0 0 0 0 1	Pop register Pair B & C off stack
POP D	1 1 0 1 0 0 0 1	Pop register Pair D & E off stack
POP H	1 1 1 0 0 0 0 1	Pop register Pair H & L off stack

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
STACK OPS (Continued)		
POP PSW	1 1 1 1 0 0 0 1	Pop A and Flags off stack
XTHL	1 1 1 0 0 0 1 1	Exchange top of stack, H & L
SPHL	1 1 1 1 1 0 0 1	H & L to stack pointer
LXI SP	0 0 1 1 0 0 0 1	Load immediate stack pointer
INX SP	0 0 1 1 0 0 1 1	Increment stack pointer
DCX SP	0 0 1 1 1 0 1 1	Decrement stack pointer
JUMP		
JMP	1 1 0 0 0 0 1 1	Jump unconditional
JC	1 1 0 1 1 0 1 0	Jump on carry
JNC	1 1 0 1 0 0 1 0	Jump on no carry
JZ	1 1 0 0 1 0 1 0	Jump on zero
JNZ	1 1 0 0 0 0 1 0	Jump on no zero
JP	1 1 1 1 0 0 1 0	Jump on positive
JM	1 1 1 1 1 0 1 0	Jump on minus
JPE	1 1 1 0 1 0 1 0	Jump on parity even
JPO	1 1 1 0 0 0 1 0	Jump on parity odd
PCHL	1 1 1 0 1 0 0 1	H & L to program counter
CALL		
CALL	1 1 0 0 1 1 0 1	Call unconditional
CC	1 1 0 1 1 1 0 0	Call on carry
CNC	1 1 0 1 0 1 0 0	Call on no carry
CZ	1 1 0 0 1 1 0 0	Call on zero
CNZ	1 1 0 0 0 1 0 0	Call on no zero
CP	1 1 1 1 0 1 0 0	Call on positive
CM	1 1 1 1 1 1 0 0	Call on minus
CPE	1 1 1 0 1 1 0 0	Call on parity even
CPO	1 1 1 0 0 1 0 0	Call on parity odd
RETURN		
RET	1 1 0 0 1 0 0 1	Return
RC	1 1 0 1 1 0 0 0	Return on carry
RNC	1 1 0 1 0 0 0 0	Return on no carry
RZ	1 1 0 0 1 0 0 0	Return on zero

Table 6. Instruction Set Summary (Continued)

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
RETURN (Continued)		
RNZ	1 1 0 0 0 0 0 0	Return on no zero
RP	1 1 1 1 0 0 0 0	Return on positive
RM	1 1 1 1 1 0 0 0	Return on minus
RPE	1 1 1 0 1 0 0 0	Return on parity even
RPO	1 1 1 0 0 0 0 0	Return on parity odd
RESTART		
RST	1 1 A A A 1 1 1	Restart
INPUT/OUTPUT		
IN	1 1 0 1 1 0 1 1	Input
OUT	1 1 0 1 0 0 1 1	Output
INCREMENT AND DECREMENT		
INR r	0 0 D D D 1 0 0	Increment register
DCR r	0 0 D D D 1 0 1	Decrement register
INR M	0 0 1 1 0 1 0 0	Increment memory
DCR M	0 0 1 1 0 1 0 1	Decrement memory
INX B	0 0 0 0 0 0 1 1	Increment B & C registers
INX D	0 0 0 1 0 0 1 1	Increment D & E registers
INX H	0 0 1 0 0 0 1 1	Increment H & L registers
DCX B	0 0 0 0 1 0 1 1	Decrement B & C
DCX D	0 0 0 1 1 0 1 1	Decrement D & E
DCX H	0 0 1 0 1 0 1 1	Decrement H & L
ADD		
ADD r	1 0 0 0 0 S S S	Add register to A
ADC r	1 0 0 0 1 S S S	Add register to A with carry
ADD M	1 0 C 0 0 1 1 0	Add memory to A
ADC M	1 0 0 0 1 1 1 0	Add memory to A with carry
ADI	1 1 0 0 0 1 1 0	Add immediate to A
ACI	1 1 0 0 1 1 1 0	Add immediate to A with carry
DAD B	0 0 0 0 1 0 0 1	Add B & C to H & L

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
ADD (Continued)		
DAD D	0 0 0 1 1 0 0 1	Add D & E to H & L
DAD H	0 0 1 0 1 0 0 1	Add H & L to H & L
DAD SP	0 0 1 1 1 0 0 1	Add stack pointer to H & L
SUBTRACT		
SUB r	1 0 0 1 0 S S S	Subtract register from A
SBB r	1 0 0 1 1 S S S	Subtract register from A with borrow
SUB M	1 0 0 1 0 1 1 0	Subtract memory from A
SBB M	1 0 0 1 1 1 1 0	Subtract memory from A with borrow
SUI	1 1 0 1 0 1 1 0	Subtract immediate from A
SBI	1 1 0 1 1 1 1 0	Subtract immediate from A with borrow
LOGICAL		
ANA r	1 0 1 0 0 S S S	And register with A
XRA r	1 0 1 0 1 S S S	Exclusive OR register with A
ORA r	1 0 1 1 0 S S S	OR register with A
CMP r	1 0 1 1 1 S S S	Compare register with A
ANA M	1 0 1 0 0 1 1 0	And memory with A
XRA M	1 0 1 0 1 1 1 0	Exclusive OR memory with A
ORA M	1 0 1 1 0 1 1 0	OR memory with A
CMP M	1 0 1 1 1 1 1 0	Compare memory with A
ANI	1 1 1 0 0 1 1 0	And immediate with A
XRI	1 1 1 0 1 1 1 0	Exclusive OR immediate with A
ORI	1 1 1 1 0 1 1 0	OR immediate with A
CPI	1 1 1 1 1 1 1 0	Compare immediate with A

Table 6. Instruction Set Summary (Continued)

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
ROTATE		
RLC	0 0 0 0 0 1 1 1	Rotate A left
RRC	0 0 0 0 1 1 1 1	Rotate A right
RAL	0 0 0 1 0 1 1 1	Rotate A left through carry
RAR	0 0 0 1 1 1 1 1	Rotate A right through carry
SPECIALS		
CMA	0 0 1 0 1 1 1 1	Complement A
STC	0 0 1 1 0 1 1 1	Set carry
CMC	0 0 1 1 1 1 1 1	Complement carry
DAA	0 0 1 0 0 1 1 1	Decimal adjust A

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
CONTROL		
EI	1 1 1 1 1 0 1 1	Enable Interrupts
DI	1 1 1 1 0 0 1 1	Disable Interrupt
NOP	0 0 0 0 0 0 0 0	No-operation
HLT	0 1 1 1 0 1 1 0	Halt
NEW 8085AH INSTRUCTIONS		
RIM	0 0 1 0 0 0 0 0	Read Interrupt Mask
SIM	0 0 1 1 0 0 0 0	Set Interrupt Mask

NOTES:
1. DDS or SSS: B 000, C 001, D 010, E011, H 100, L101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

8155H/8156H/8155H-2/8156H-2
2048-BIT STATIC HMOS RAM WITH I/O PORTS AND TIMER

- **Single +5V Power Supply with 10% Voltage Margins**
- **30% Lower Power Consumption than the 8155 and 8156**
- **256 Word x 8 Bits**
- **Completely Static Operation**
- **Internal Address Latch**
- **2 Programmable 8-Bit I/O Ports**
- **1 Programmable 6-Bit I/O Port**
- **Programmable 14-Bit Binary Counter/ Timer**
- **Compatible with 8085AH and 8088 CPU**
- **Multiplexed Address and Data Bus**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel® 8155H and 8156H are RAM and I/O chips implemented in N-Channel, depletion load, silicon gate technology (HMOS), to be used in the 8085AH and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330 ns for use with the 8085H-2 and the 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

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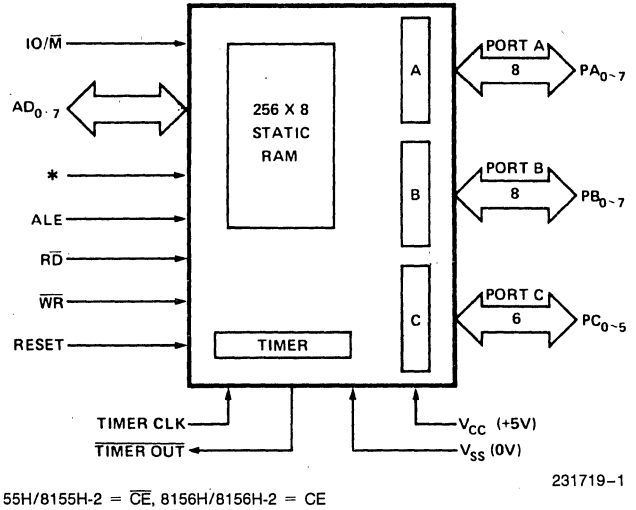


*8155H/8155H-2 = $\overline{CE}$, 8156H/8156H-2 = CE

Figure 1. Block Diagram

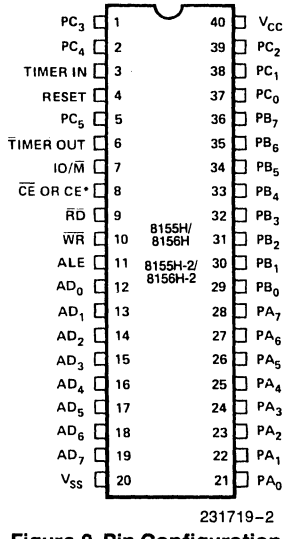


Figure 2. Pin Configuration

December 1986
Order Number: 231719-001

Table 1. Pin Description

Symbol	Type	Name and Function
RESET	I	**RESET:** Pulse provided by the 8085AH to initialize the system (connect to 8085AH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085AH clock cycle times.
AD_{0-7}	I/O	**ADDRESS/DATA:** 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155H/56H on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$	I	**CHIP ENABLE:** On the 8155H, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156H, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	I	**READ CONTROL:** Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$	I	**WRITE CONTROL:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$.
ALE	I	**ADDRESS LATCH ENABLE:** This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O MEMORY:** Selects memory if low and I/O and command/status registers if high.
PA_{0-7} (8)	I/O	**PORT A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7} (8)	I/O	**PORT B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5} (6)	I/O	**PORT C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0—A INTR (Port A Interrupt) PC_1—ABF (Port A Buffer Full) PC_2—$\overline{A\ STB}$ (Port A Strobe) PC_3—B INTR (Port B Interrupt) PC_4—B BF (Port B Buffer Full) PC_5—$\overline{B\ STB}$ (Port B Strobe)
TIMER IN	I	**TIMER INPUT:** Input to the timer-counter.
$\overline{TIMER\ OUT}$	O	**TIMER OUTPUT:** This output can be either a square wave or a pulse, depending on the timer mode.
V_{CC}		**VOLTAGE:** +5V supply.
V_{SS}		**GROUND:** Ground reference.

FUNCTIONAL DESCRIPTION

The 8155H/8156H contains the following:

- 2K Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA_{0-7}, PB_{0-7}, PC_{0-5}) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

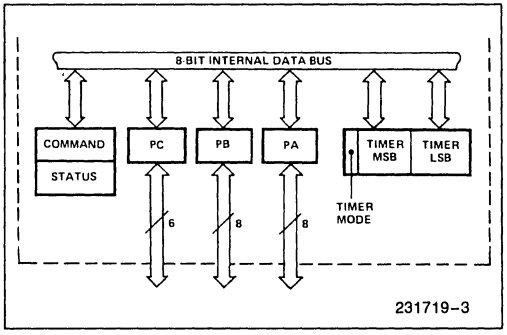
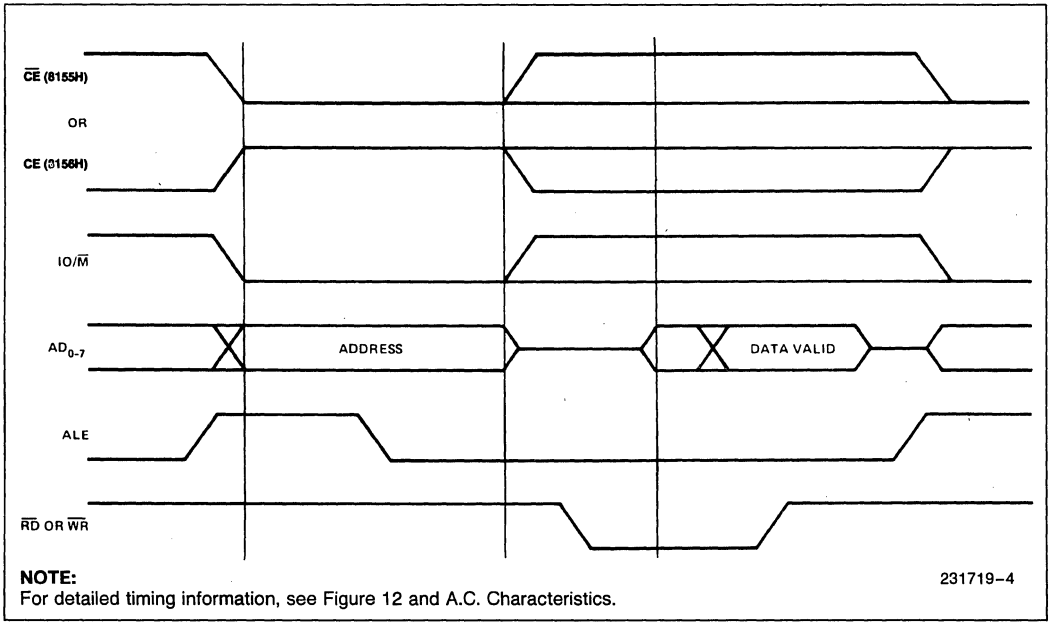


Figure 3. 8155H/8156H Internal Registers



NOTE:
For detailed timing information, see Figure 12 and A.C. Characteristics.

Figure 4. 8155H/8156H On-Board Memory Read/Write Cycle

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PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0–3) define the mode of the ports, two bits (4–5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6–7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 5. The contents of the command register may never be read.

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0–5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 6. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

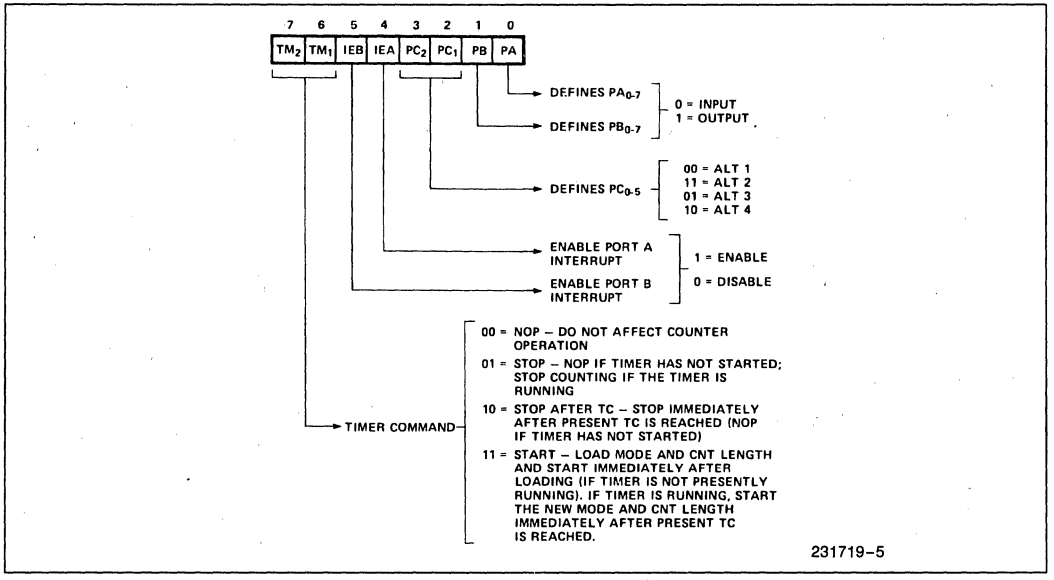


Figure 5. Command Register Bit Assignment

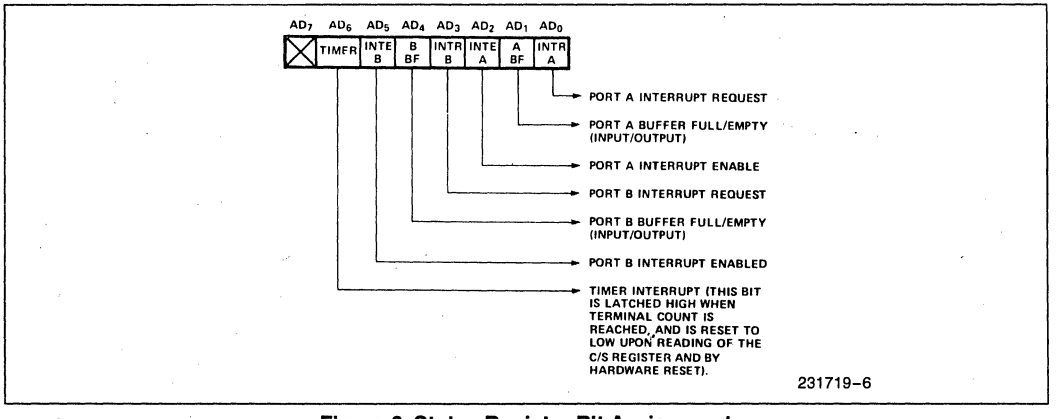


Figure 6. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the 8155H/8156H consists of five registers: (see Figure 7.)

- **Command/Status Register (C/S)**—Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.
  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.
  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.
- **PA Register**—This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.
- **PB Register**—This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.
- **PC Register**—This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.
  When PC_{0-5} is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155H sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 2.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

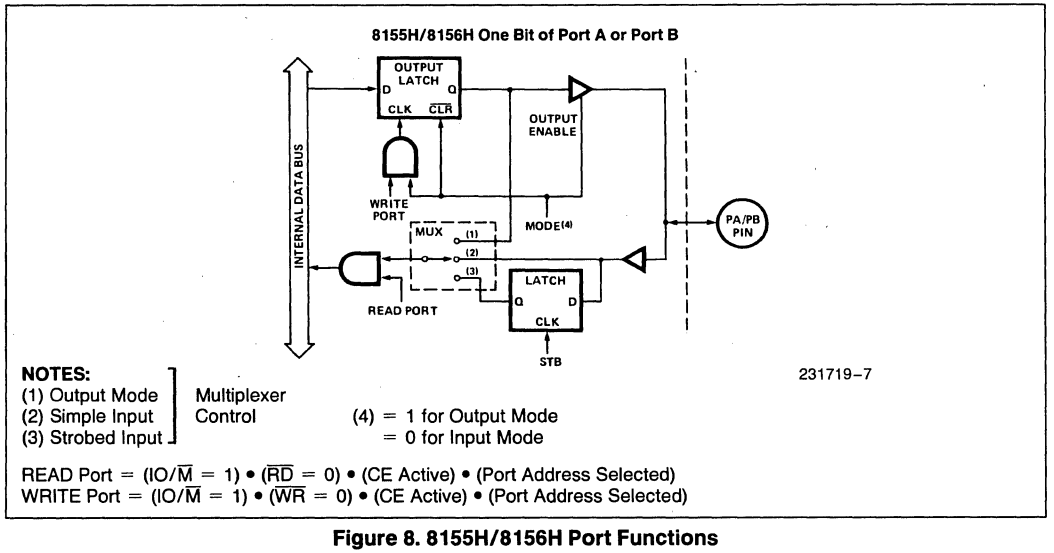
Control	Input Mode	Output Mode
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O Address†								Selection
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	Port C—General Purpose I/O or Control
X	X	X	X	X	1	0	0	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care.
†: I/O Address must be qualified by CE = 1 (8156H) or $\overline{CE}$ = 0 (8155H) and IO/$\overline{M}$ = 1 in order to select the appropriate register.

Figure 7. I/O Port and Timer Addressing Scheme

Figure 8 shows how I/O PORTS A and B are structured within the 8155H and 8156H:



NOTES:
(1) Output Mode
(2) Simple Input
(3) Strobed Input
Multiplexer Control

(4) = 1 for Output Mode
= 0 for Input Mode

READ Port = (IO/$\overline{M}$ = 1) • ($\overline{RD}$ = 0) • (CE Active) • (Port Address Selected)
WRITE Port = (IO/$\overline{M}$ = 1) • ($\overline{WR}$ = 0) • (CE Active) • (Port Address Selected)

Figure 8. 8155H/8156H Port Functions

Table 2. Port Control Assignment

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the 8155H/8156H are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pin will go low. When the 8155H/56H is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 9 shows how the 8155H/8156H I/O ports might be configured in a typical MCS®-85 system.

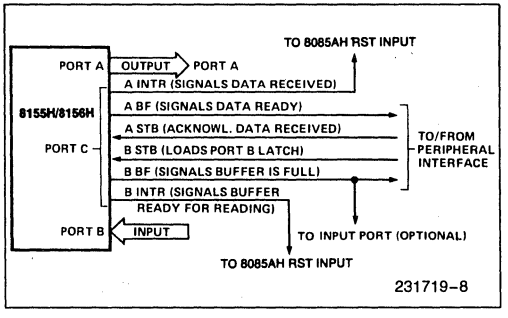


Figure 9. Example: Command Register = 00111001

TIMER SECTION

The time is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 7.)

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0–13 of the high order count register will specify the length of the next count and bits 14–15 of the high order register will specify the timer output mode (see Figure 10). The value loaded into the count length register can have any value from 2H through 3FFFH in Bits 0–13.

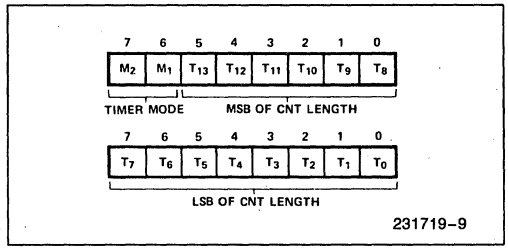


Figure 10. Timer Format

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 11.

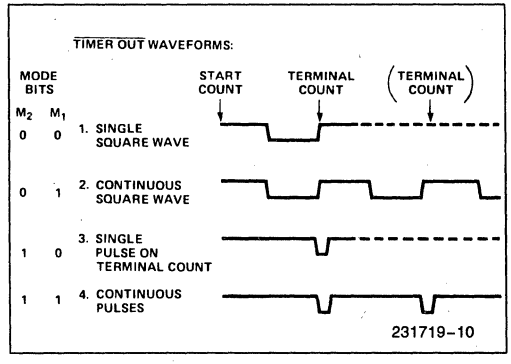


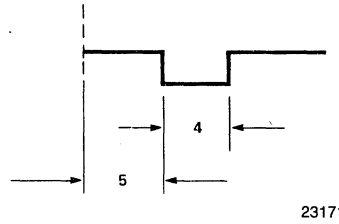
Figure 11. Timer Modes

Bits 6–7 (TM_2 and TM_1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM_2	TM_1	
0	0	NOP—Do not affect counter operation.
0	1	STOP—NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC—Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START—Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you **must** issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 12.



NOTE:
5 and 4 refer to the number of clocks in that time period.

Figure 12. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the 8155H is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155H/8156H chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085AH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add ½ of the full original count (½ full count—1 if full count is odd).

NOTE:
If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155H/56H always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

13

8085AH MINIMUM SYSTEM CONFIGURATION

Figure 13a shows a minimum system using three chips, containing:

- 256 Bytes RAM
- 2K Bytes EPROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

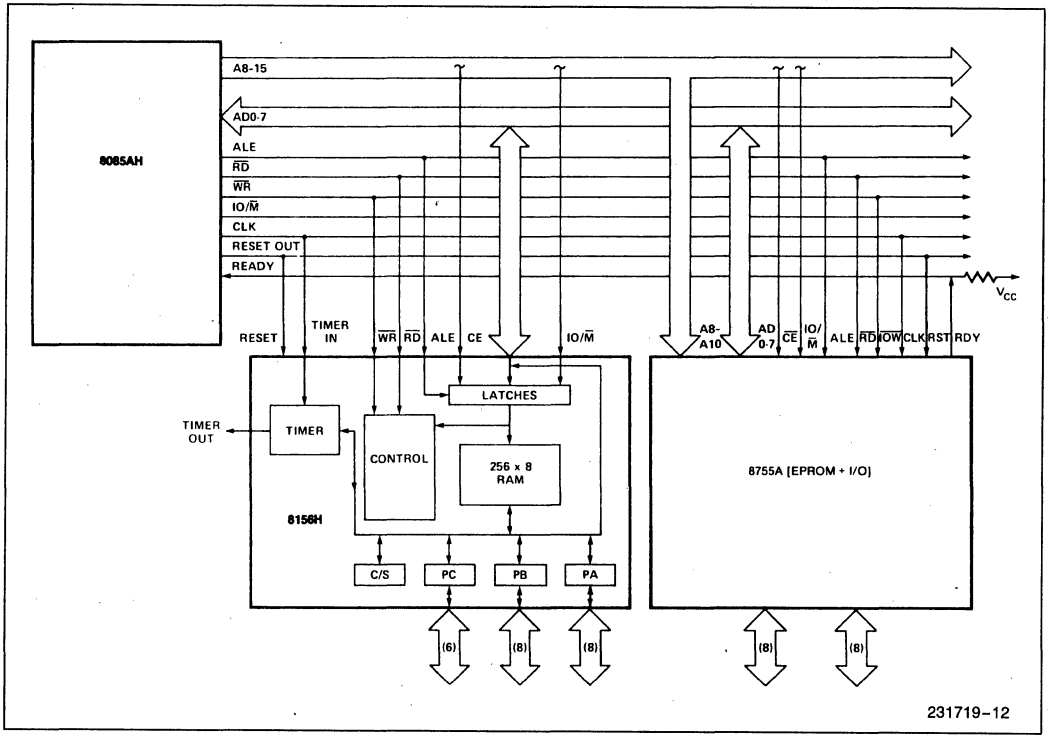


Figure 13a. 8085AH Minimum System Configuration (Memory Mapped I/O)

8088 FIVE CHIP SYSTEM

Figure 13b shows a five chip system containing:

- 1.25K Bytes RAM
- 2K Bytes EPROM
- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels

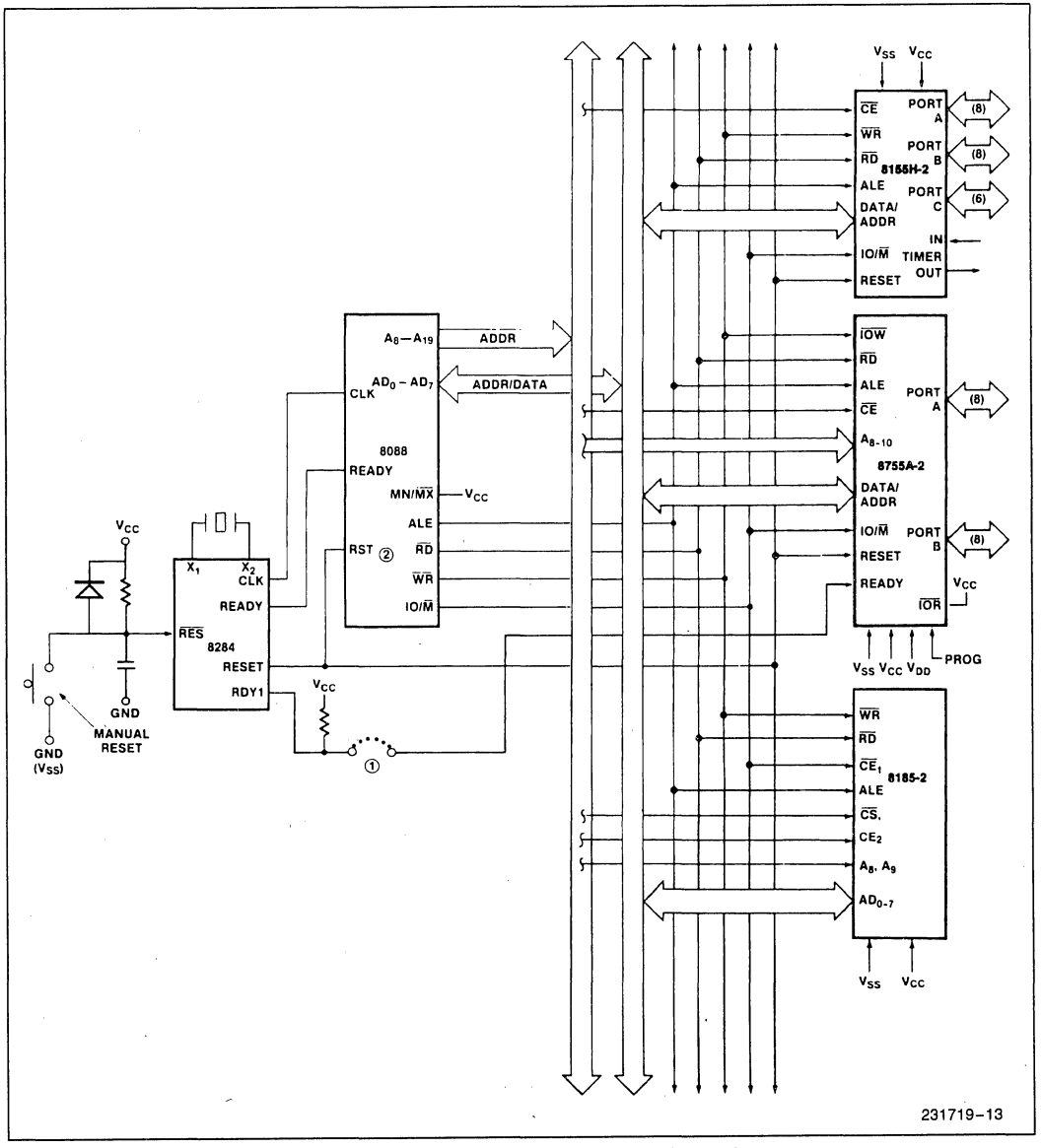


Figure 13b. 8088 Five Chip System Configuration

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin
with Respect to Ground.....−0.5V to +7V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Leakage		±10	μA	$0V \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45V \le V_{OUT} \le V_{CC}$
I_{CC}	V_{CC} Supply Current		125	mA	
I_{IL} (CE)	Chip Enable Leakage 8155H 8156H		 +100 −100	 μA μA	$0V \le V_{IN} \le V_{CC}$

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

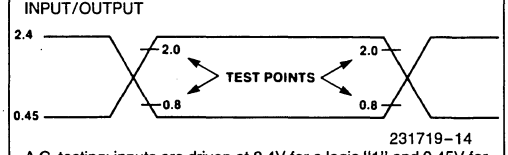
Symbol	Parameter	8155H/8156H		8155H-2/8156H-2		Units
		Min	Max	Min	Max	
t_{AL}	Address to Latch Setup Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{LD}	Latch to Data Out Valid		350		270	ns
t_{AD}	Address Stable to Data Out Valid		400		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float after READ	0	100	0	80	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CLL}	WRITE Control to Latch Enable for C/S Register	125		125		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to WRITE Setup Time	150		100		ns
t_{WD}	Data In Hold Time after WRITE	25		25		ns
t_{RV}	Recovery Time between Controls	300		200		ns
t_{WP}	WRITE to Port Output		400		300	ns

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10% (Continued)

Symbol	Parameter	8155H/8156H		8155H-2/8156H-2		Units
		Min	Max	Min	Max	
t_{PR}	Port Input Setup Time	70		50		ns
t_{RP}	Port Input Hold Time	50		10		ns
t_{SBF}	Strobe to Buffer Full		400		300	ns
t_{SS}	Strobe Width	200		150		ns
t_{RBE}	READ to Buffer Empty		400		300	ns
t_{SI}	Strobe to INTR On		400		300	ns
t_{RDI}	READ to INTR Off		400		300	ns
t_{PSS}	Port Setup Time to Strobe	50		0		ns
t_{PHS}	Port Hold Time After Strobe	120		100		ns
t_{SBE}	Strobe to Buffer Empty		400		300	ns
t_{WBF}	WRITE to Buffer Full		400		300	ns
t_{WI}	WRITE to INTR Off		400		300	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400		300	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400		300	ns
t_{RDE}	Data Bus Enable from READ Control	10		10		ns
t_1	TIMER-IN Low Time	80		40		ns
t_2	TIMER-IN High Time	120		70		ns
t_{WT}	WRITE to TIMER-IN (for writes which start counting)	360		200		ns

13

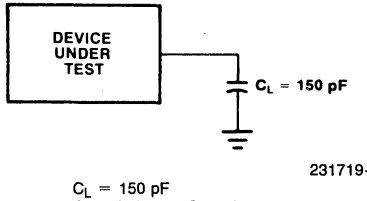
A.C. TESTING INPUT, OUTPUT WAVEFORM



231719-14

A.C. testing: inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

A.C. TESTING LOAD CIRCUIT

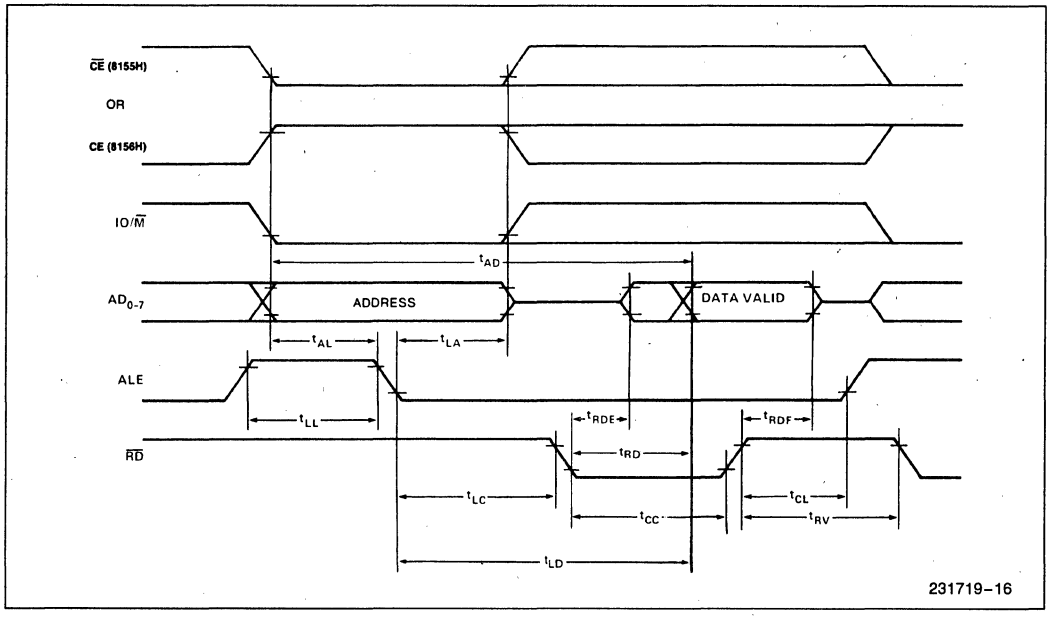


231719-15

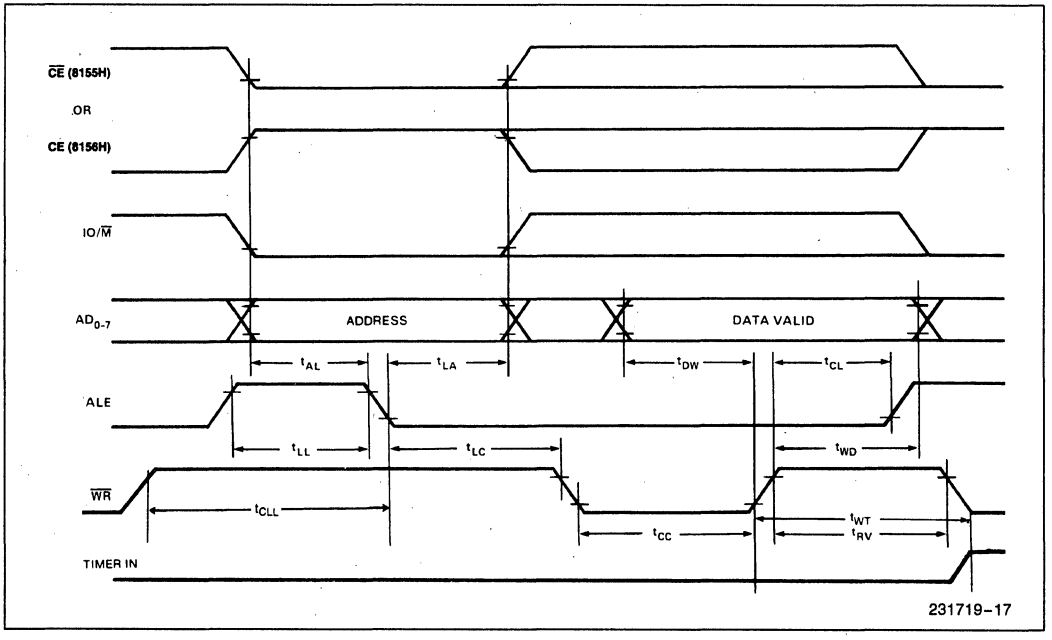
C_L = 150 pF
C_L Includes Jig Capacitance

WAVEFORMS

READ

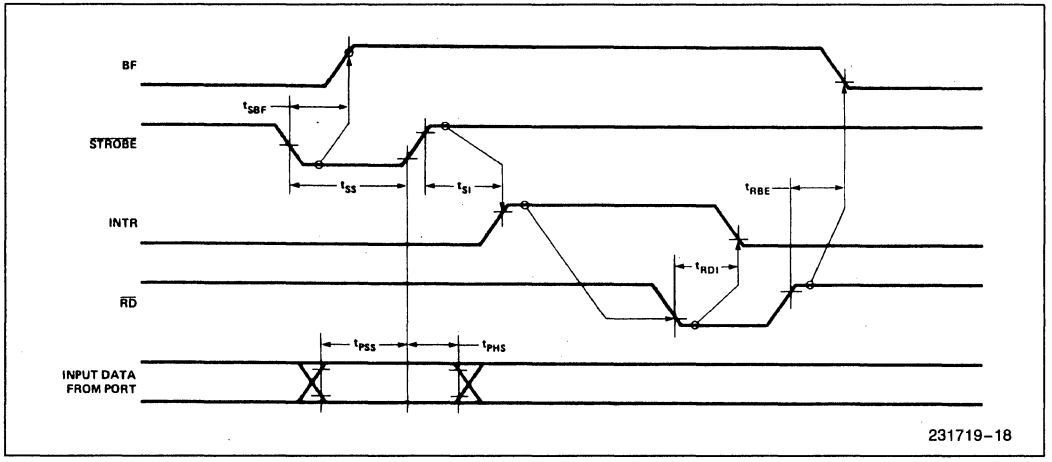


WRITE

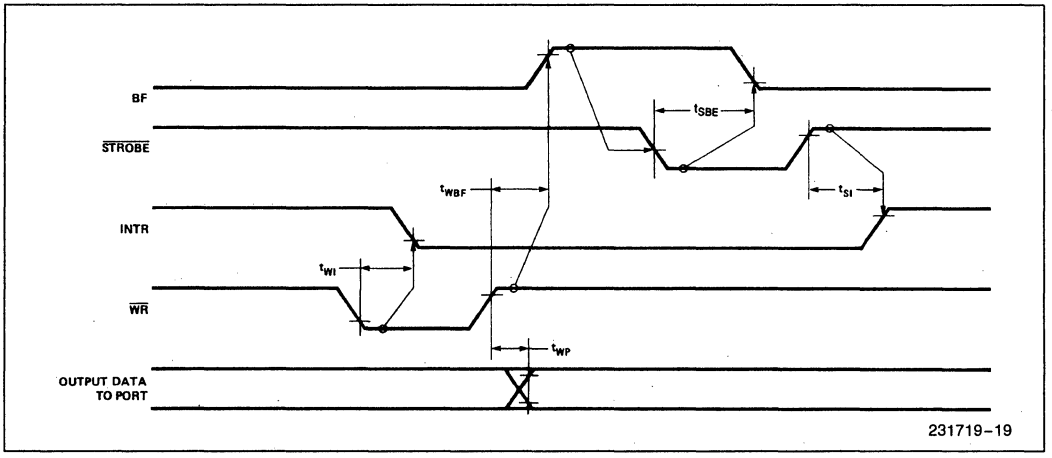


WAVEFORMS (Continued)

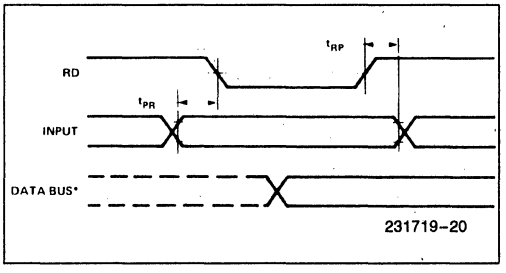
STROBED INPUT



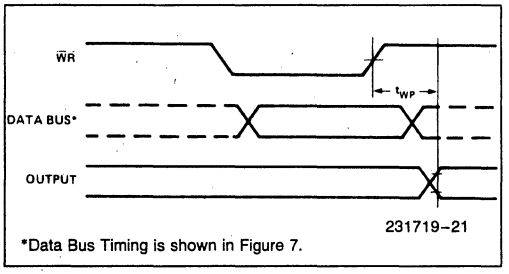
STROBED OUTPUT



BASIC INPUT



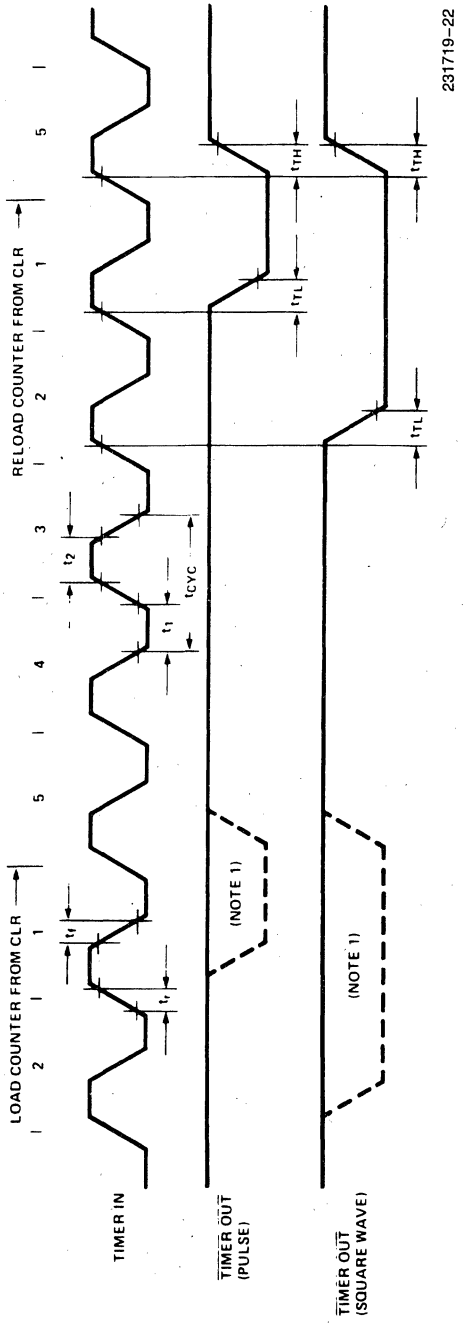
BASIC OUTPUT



*Data Bus Timing is shown in Figure 7.

WAVEFORMS (Continued)

TIMER OUTPUT COUNTDOWN FROM 5 TO 1



NOTE:
1. The timer output is periodic if in an automatic reload mode (M_1 Mode bit = 1).

8185/8185-2
1024 x 8-BIT STATIC RAM FOR MCS®-85

- **Multiplexed Address and Data Bus**
- **Directly Compatible with 8085AH and 8088 Microprocessors**
- **Low Operating Power Dissipation**
- **Low Standby Power Dissipation**
- **Single +5V Supply**
- **High Density 18-Pin Package**

The Intel 8185 is an 8192-bit static random access memory (RAM) organized as 1024 words by 8-bits using N-channel Silicon-Gate MOS technology. The multiplexed address and data bus allows the 8185 to interface directly to the 8085AH and 8088 microprocessors to provide a maximum level of system integration.

The low standby power dissipation minimizes system power requirements when the 8185 is disabled.

The 8185-2 is a high-speed selected version of the 8185 that is compatible with the 5 MHz 8085AH-2 and the 5 MHz 8088.

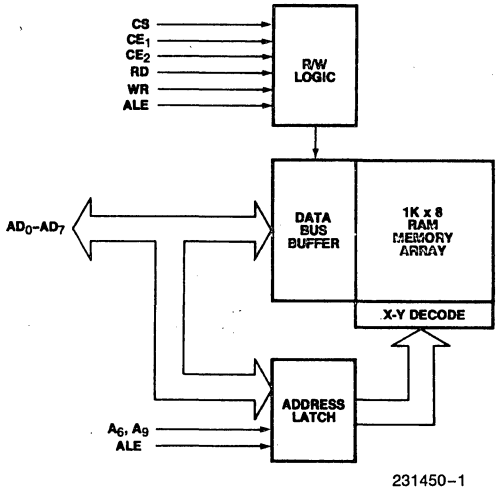


Figure 1. Block Diagram

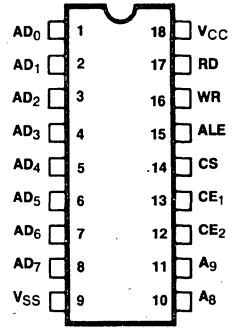


Figure 2. Pin Configuration

Pin Names

AD_0–AD_7	Address/Data Lines
A_8, A_9	Address Lines
CS	Chip Select
CE_1	Chip Enable (IO/M)
CE_2	Chip Enable
ALE	Address Latch Enable
WR	Write Enable

November 1989
Order Number: 231450-002

FUNCTIONAL DESCRIPTION

The 8185 has been designed to provide for direct interface to the multiplexed bus structure and bus timing of the 8085A microprocessor.

At the beginning of an 8185 memory access cycle, the 8-bit address on AD_{0-7}, A_8 and A_9, and the status of $\overline{CE_1}$ and CE_2 are all latched internally in the 8185 by the falling edge of ALE. If the latched status of both $\overline{CE_1}$ and CE_2 are active, the 8185 powers itself up, but no action occurs until the $\overline{CS}$ line goes low and the appropriate $\overline{RD}$ or $\overline{WR}$ control signal input is activated.

The $\overline{CS}$ input is not latched by the 8185 in order to allow the maximum amount of time for address decoding in selecting the 8185 chip. Maximum power consumption savings will occur, however, only when $\overline{CE_1}$ and CE_2 are activated selectively to power down the 8185 when it is not in use. A possible connection would be to wire the 8085A's IO/$\overline{M}$ line to the 8185's $\overline{CE_1}$ input, thereby keeping the 8185 powered down during I/O and interrupt cycles.

Table 1. Truth Table for Power Down and Function Enable

$\overline{CE_1}$	CE_2	$\overline{CS}$	(CS*)(2)	8185 Status
1	X	X	0	Power Down and Function Disable(1)
X	0	X	0	Power Down and Function Disable(1)
0	1	1	0	Powered Up and Function Disable(1)
0	1	0	1	Powered Up and Enabled

NOTES:
X = Don't Care.
1: Function Disable implies Data Bus in high impedance state and not writing.
2: CS* = ($\overline{CE_1}$ = 0) × (CE_2 = 1) × ($\overline{CS}$ = 0).
CS* = 1 signifies all chip enables and chip select active.

Table 2. Truth Table for Control and Data Bus Pin Status

(CS*)	$\overline{RD}$	$\overline{WR}$	AD_{0-7} During Data Portion of Cycle	8185 Function
0	X	X	Hi-Impedance	No Function
1	0	1	Data from Memory	Read
1	1	0	Data to Memory	Write
1	1	1	Hi-Impedance	Reading, but not Driving Data Bus

NOTE:
X = Don't Care.

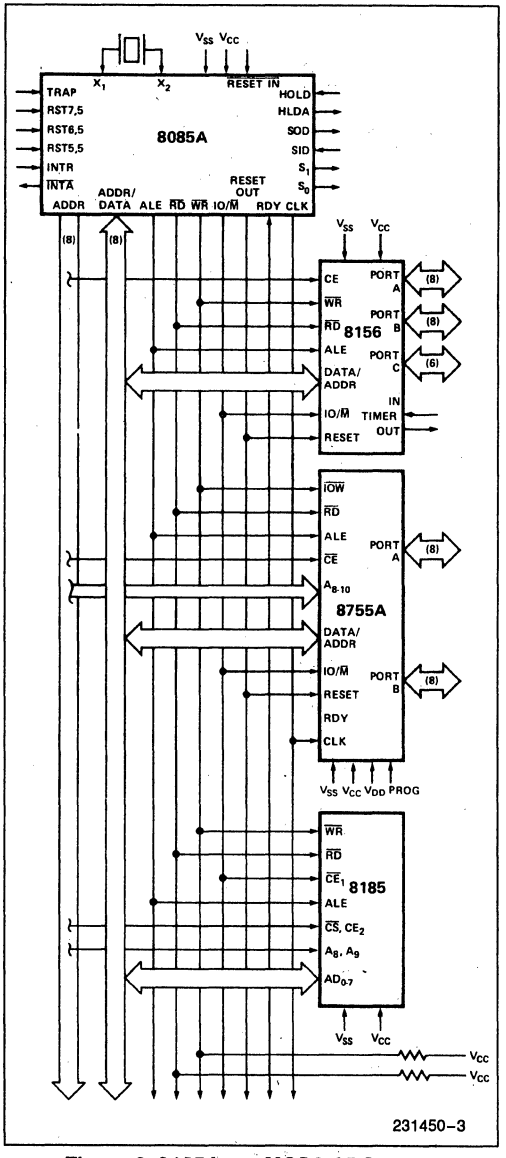


Figure 3. 8185 in an MCS®-85 System

4 Chips:
2K Bytes EPROM
1.25K Bytes RAM
38 I/O Lines
1 Counter/Timer
2 Serial I/O Lines
5 Interrupt Inputs

iAPX 88 FIVE CHIP SYSTEM:

- 1.25K Bytes RAM
- 2K Bytes EPROM
- 38 I/O Pins
- 1 Internal Timer
- 2 Interrupt Levels

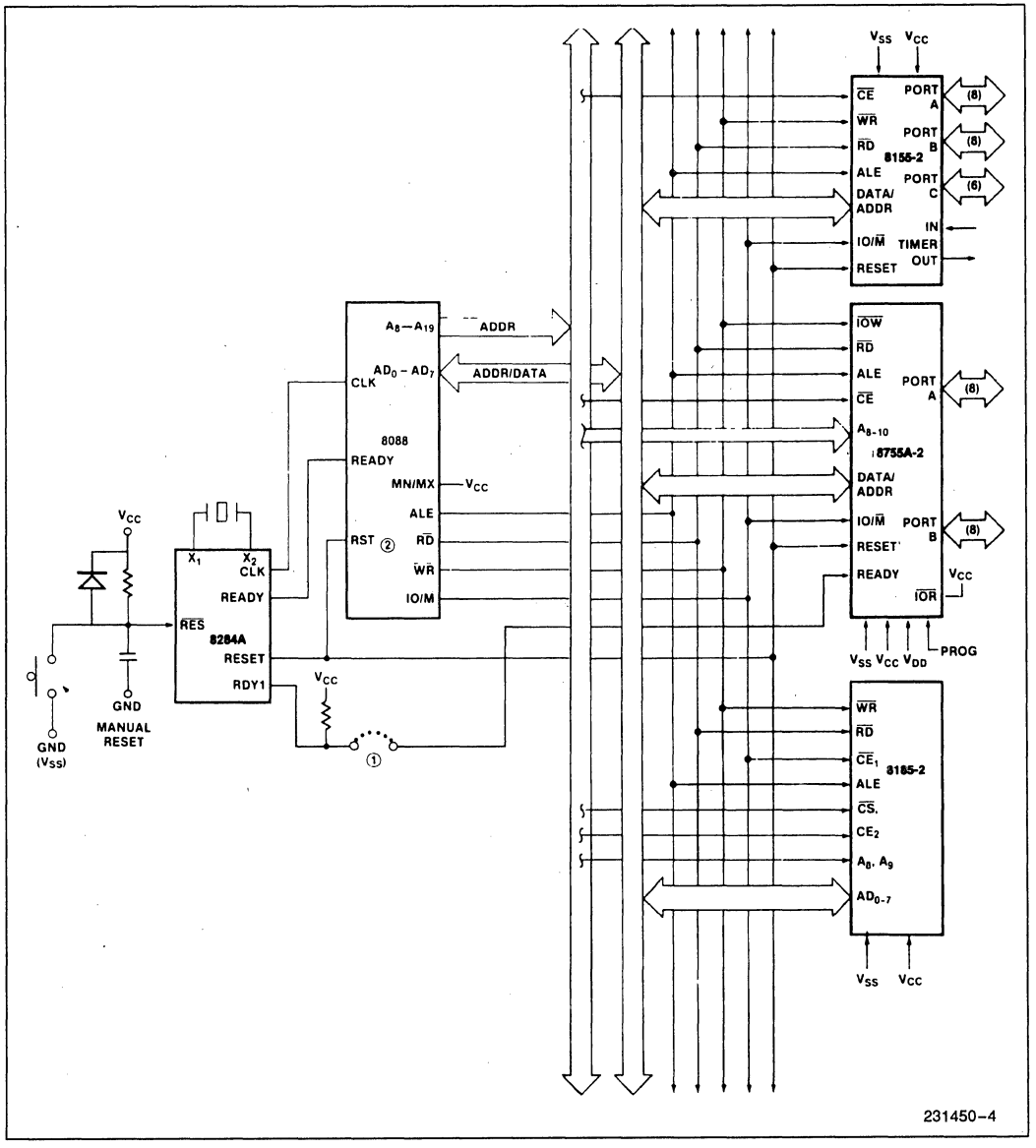


Figure 4. iAPX 88 Five Chip System Configuration

13

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
with Respect to Ground . . . . . −0.5V to +7V
Power Dissipation 1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

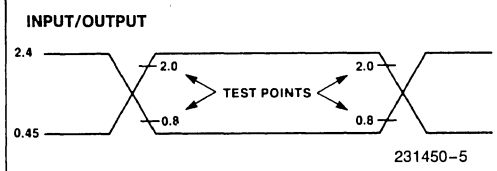
D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4			I_{OH} = −400 μA
I_{IL}	Input Leakage		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current Powered Up		100	mA	
	Powered Down		35	mA	

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	8185		8185-2		
		Min	Max	Min	Max	Units
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time After Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{LD}	ALE to Data Out Valid		300		200	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float After READ	0	100	0	80	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to WRITE Set Up Time	150		150		ns
t_{WD}	Data In Hold Time After WRITE	20		20		ns
t_{SC}	Chip Select Set Up to Control Line	10		10		ns
t_{CS}	Chip Select Hold Time After Control	10		10		ns
t_{ALCE}	Chip Enable Set Up to ALE Falling	30		10		ns
t_{LACE}	Chip Enable Hold Time After ALE	50		30		ns

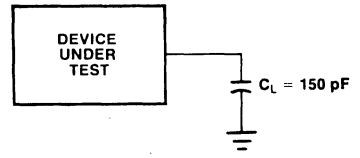
A.C. TESTING INPUT, OUTPUT WAVEFORM



231450-5

A.C. Testing: Inputs Are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing Measurements Are Made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

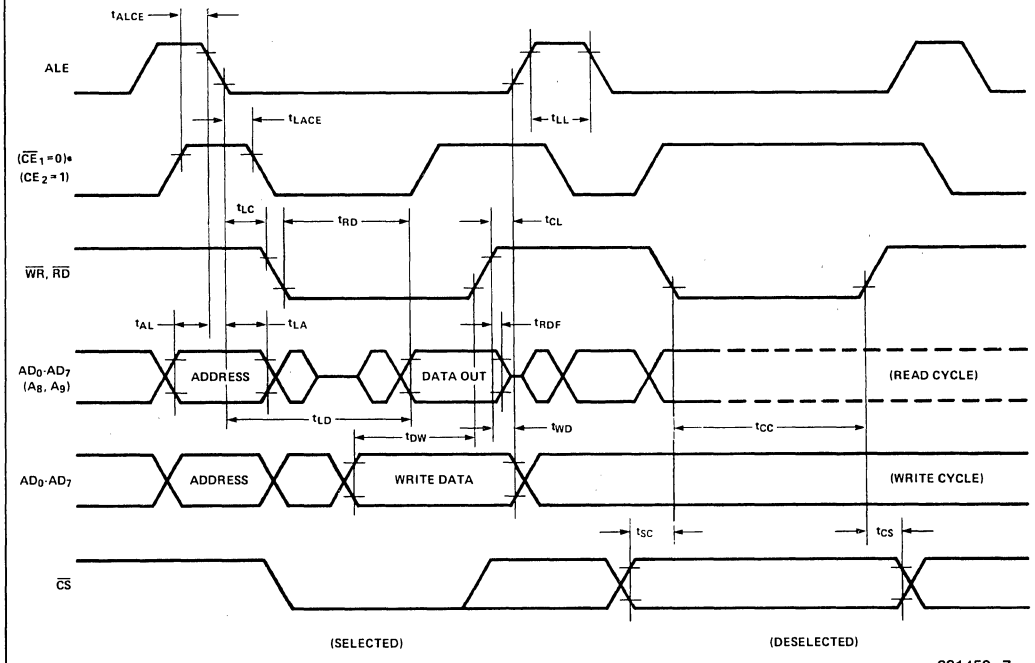
A.C. TESTING LOAD CIRCUIT



231450-6

C_L = 150 pF
C_L Includes Jig Capacitance

WAVEFORM



231450-7

13

8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

- **Single Chip Clock Generator/Driver for 8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**
- **Available in EXPRESS — Standard Temperature Range**
- **Available in 16-Lead Cerdip Package** (See Packaging Spec, Order #231369)

The Intel 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

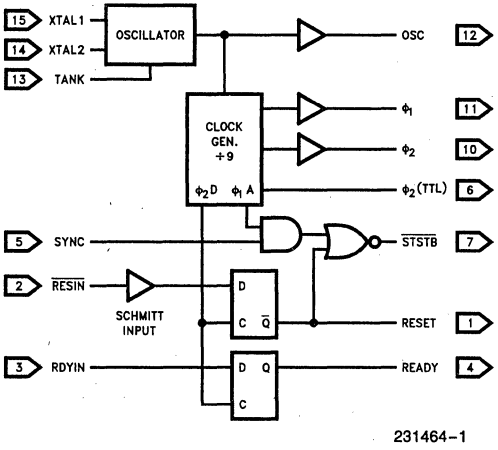
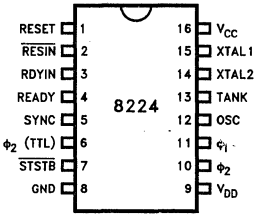


Figure 1. Block Diagram



$\overline{RESIN}$	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
$\overline{STSTB}$	Status STB (Active Low)
ϕ_1	8080 Clocks
ϕ_2	

XTAL 1	Connections for Crystal
XTAL 2	
TANK	Used with Overtone XTAL
OSC	Oscillator Output
ϕ_2 (TTL)	ϕ_2 CLK (TTL Level)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

Figure 2. Pin Configuration

November 1992
Order Number: 231464-001

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Supply Voltage, V_{CC} .....−0.5V to +7V
Supply Voltage, V_{DD} .....−0.5V to +13.5V
Input Voltage .....−1.5V to +7V
Output Current .....100 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%, V_{DD} = +12V ±5%

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
I_F	Input Current Loading			−0.25	mA	V_F = 0.45V
I_R	Input Leakage Current			10	μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.6			V	Reset Input
		2.0			V	All Other Inputs
V_{IH}−V_{IL}	RESIN Input Hysteresis	0.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage			0.45	V	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} = 2.5 mA
				0.45	V	All Other Outputs I_{OL} = 15 mA
V_{OH}	Output "High" Voltage ϕ_1, ϕ_2	9.4			V	I_{OH} = −100 μA
	READY, RESET	3.6			V	I_{OH} = −100 μA
	All Other Outputs	2.4			V	I_{OH} = −1 mA
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

NOTE:
1. For crystal frequencies of 18 MHz connect 510Ω resistors between the X1 input and ground as well as the X2 input and ground to prevent oscillation at harmonic frequencies.

Crystal Requirements

Tolerance: 0.005% at 0°C–70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20 pF–35 pF
Equivalent Resistance: 75Ω–20Ω

Power Dissipation (Min): 4 mW

***NOTE:**
With tank circuit use 3rd overtone mode.

A.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9} - 20$ ns			ns	C_L = 20 pF to 50 pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9} - 35$ ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9} - 14$ ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9} + 20$ ns		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	−5		+15	ns	ϕ_2 TTL, CL = 30 R_1 = 300Ω R_2 = 600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9} - 30$ ns		$\frac{6tcy}{9}$	ns	$\overline{STSTB}$, C_L = 15 pF R_1 = 2K R_2 = 4K
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9} - 15$ ns			ns	
t_{DRS}	RDYIN Setup Time to Status Strobe	$50\text{ ns} - \frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	$\frac{4tcy}{9} - 25$ ns			ns	Ready & Reset C_L = 10 pF R_1 = 2K R_2 = 4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$		ns	
f_{max}	Maximum Oscillating Frequency			27	MHz	
C_{in}	Input Capacitance			8	pF	V_{CC} = +5.0V V_{DD} = +12V V_{BIAS} = 2.5V f = 1 MHz

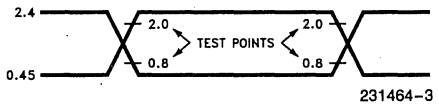
NOTE:
These formulas are based on the internal workings of the part and intended for customer convenience. Actual testing of the part is done at t_{cy} = 488.28 ns.

A.C. CHARACTERISTICS (Continued)

For t_{CY} = 488.28 ns; T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY} = 488.28 ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 pF to 50 pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	−5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	Ready & Reset Loaded to 2 mA/10 pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	−167			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

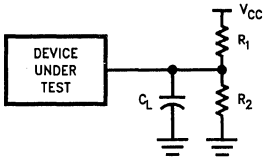
A.C. TESTING, INPUT, OUTPUT WAVEFORM



231464-3

A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0" (unless otherwise noted).

A.C. TESTING LOAD CIRCUIT



231464-4

C_L Includes Jig Capacitance

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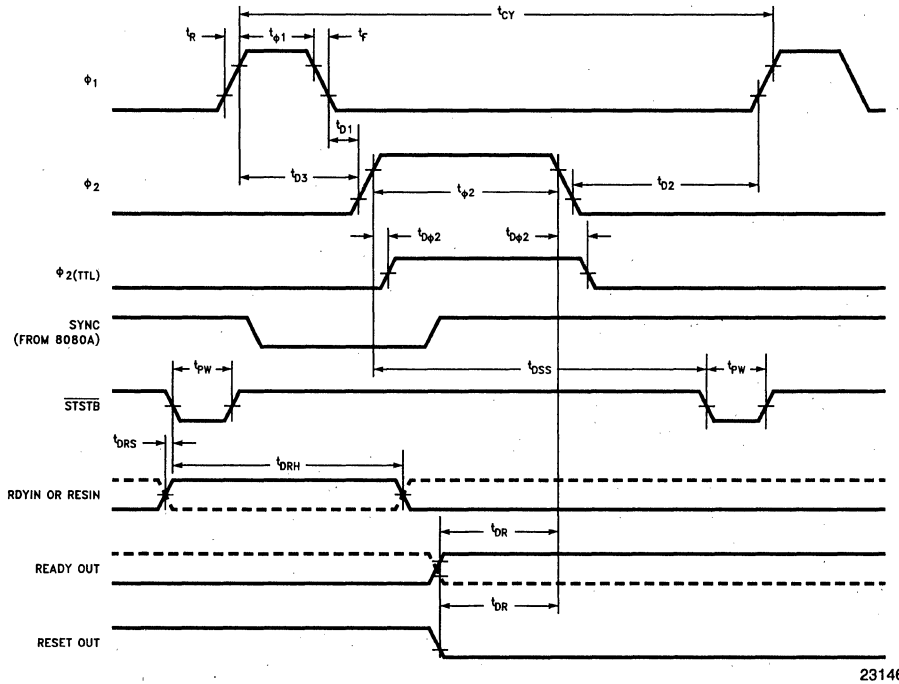
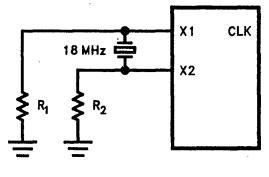
WAVEFORMS



231464-5

VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

CLOCK HIGH AND LOW TIME (USING X1, X2)



231464-6

8228
SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- **Single Chip System Control for MCS®-80 Systems**
- **Built-In Bidirectional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **Reduces System Package Count**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **Available in EXPRESS — Standard Temperature Range**
- **Available in 28-Lead Cerdip and Plastic Packages**
  (See Packaging Spec, Order #231369)

The Intel® 8228 is a single chip system controller and bus driver for MCS®-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable design of MCS-80 systems.

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NOTE:
The specifications for the 3228 are identical with those for the 8228.

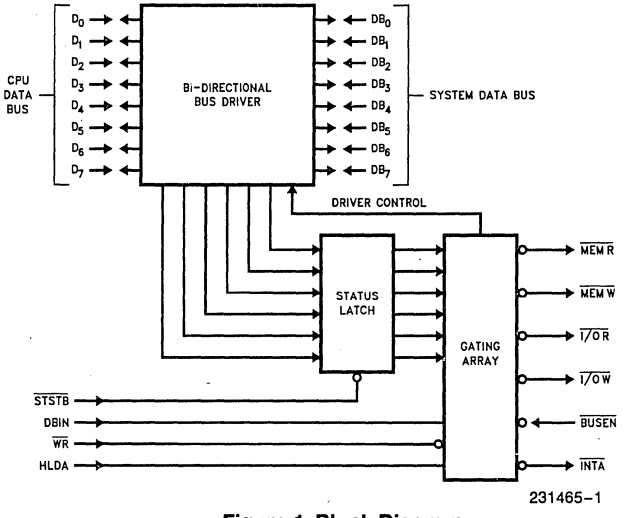

Figure 1. Block Diagram

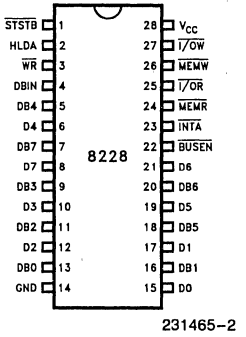

Figure 2. Pin Configuration

D7-D0	Data Bus (8080 Side)
DB7-DB0	Data Bus (System Side)
I/OR	I/O Read
I/OW	I/O Write
MEMR	Memory Read
MEMW	Memory Write
DBIN	DBIN (from 8080)

INTA	Interrupt Acknowledge
HLDA	HLDA (from 8080)
WR	WR (from 8080)
BUSEN	Bus Enable Input
STSTB	Status Strobe (from 8224)
VCC	+5V
GND	0 Volts

November 1992
Order Number: 231465-002

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Supply Voltage, V_{CC} .....−0.5V to +7V
Input Voltage .....−1.5 to +7V
Output Current .....100 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±5%

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ(1)	Max		
V_C	Input Clamp Voltage, All Input			0.75	−1.0	V	V_{CC} = 4.75V; I_C = −5 mA
I_F	Input Load Current	$\overline{STSTB}$			500	μA	V_{CC} = 5.25V
		D_2 & D_6			750	μA	V_F = 0.45V
		D_0, D_1, D_4, D_5 & D_7			250	μA	
		All Other Inputs			250	μA	
I_R	Input Leakage Current	$\overline{STSTB}$			100	μA	V_{CC} = 5.25V V_R = 5.25V
		DB_0–DB_7			20	μA	
		All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs		0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current			140	190	mA	V_{CC} = 5.25V
V_{OL}	Output Low Voltage	D_0–D_7			0.45	V	V_{CC} = 4.75V; I_{OL} = 2 mA
		All Other Outputs			0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage	D_0–D_7	3.6	3.8		V	V_{CC} = 4.75V; I_{OH} = −10μA
		All Other Outputs	2.4			V	I_{OH} = −1 mA
I_{OS}	Short Circuit Current, All Outputs		15		90	mA	V_{CC} = 5V
$I_{O\ (off)}$	Off State Output Current All Control Outputs				100	μA	V_{CC} = 5.25V; V_O = 5.25V
					−100	μA	V_O = 0.45V
I_{INT}	INTA Current				5	mA	(See INTA Test Circuit)

NOTE:
1. Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz

1. This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits			Unit
		Min	Typ(1)	Max	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Limits		Unit	Conditions
		Min	Max		
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0–D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0–D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	C_L = 100 pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	C_L = 100 pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	C_L = 25 pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	C_L = 25 pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	45	ns	C_L = 100 pF
t_{WE}	Delay to Enable System Bus DB_0–DB_7 after $\overline{STSTB}$		30	ns	C_L = 100 pF
t_{WD}	Delay from 8080 Bus D_0–D_7 to System Bus DB_0–DB_7 during Write	5	40	ns	C_L = 100 pF
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0–DB_7		30	ns	C_L = 100 pF
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	C_L = 100 pF

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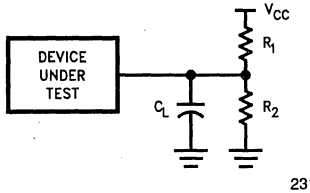
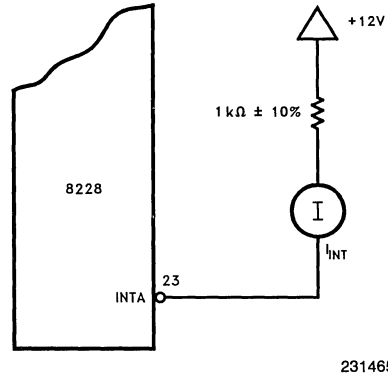
A.C. TESTING LOAD CIRCUIT



231465-3

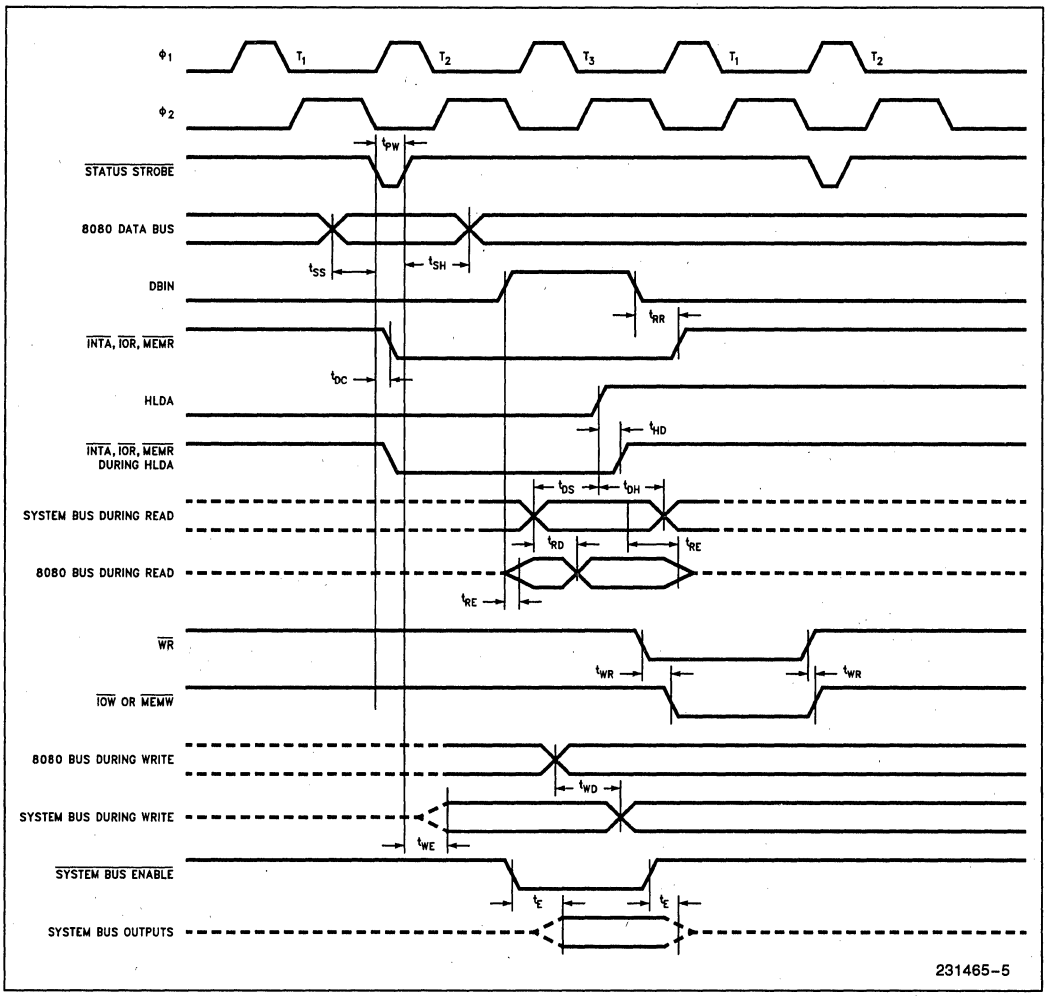
For D_0–D_7: R_1 = 4 KΩ, R_2 = ∞Ω, C_L = 25 pF.
For all other outputs: R_1 = 500Ω, R_2 = 1 KΩ, C_L = 100 pF.

INTA Test Circuit (for RST 7)



231465-4

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0–D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

8755A
16,384-BIT EPROM WITH I/O

- **2048 Words x 8 Bits**
- **Single +5V Power Supply (V_{CC})**
- **Directly Compatible with 8085AH**
- **U.V. Erasable and Electrically Reprogrammable**
- **Internal Address Latch**
- **2 General Purpose 8-Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40-Pin DIP**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the 8085AH microprocessor systems. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085AH CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

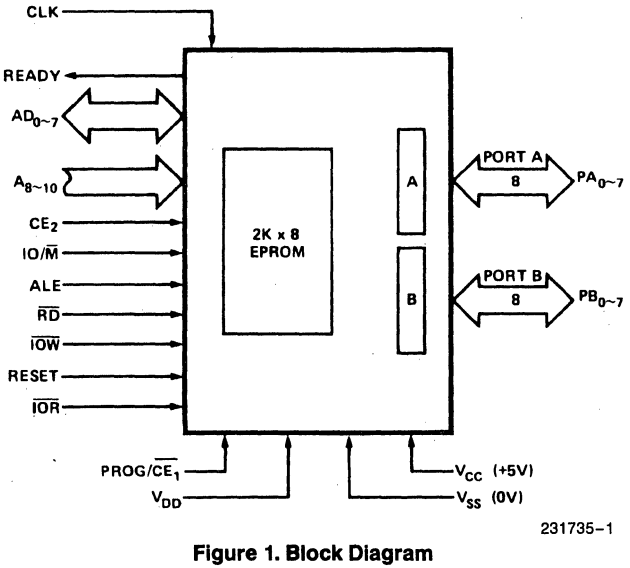


Figure 1. Block Diagram

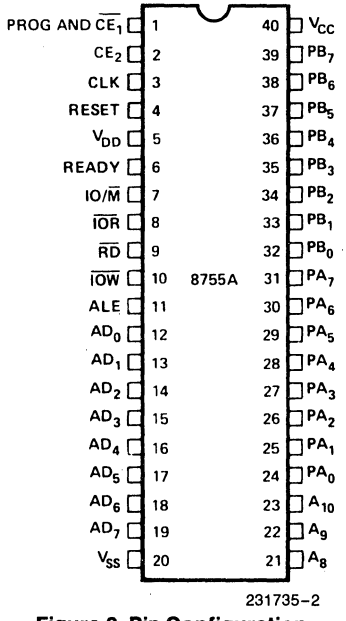


Figure 2. Pin Configuration

November 1986
Order Number: 231735-002

Table 1. Pin Description

Symbol	Type	Name and Function
ALE	I	**ADDRESS LATCH ENABLE:** When Address Latch Enable goes *high,* AD_{0-7}, $IO/\overline{M}$, A_{8-10}, CE_2, and $\overline{CE_1}$ enter the address latches. The signals, (AD, $IO/\overline{M}$, AD_{8-10}, CE_2, $\overline{CE_1}$) are latched in at the trailing edge of ALE.
AD_{0-7}	I	**BIDIRECTIONAL ADDRESS/DATA BUS:** The lower 8 bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B is selected based on the latched value of AD_0. IF $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.
AD_{8-10}	I	**ADDRESS BUS:** These are the high order bits of the PROM address. They do not affect I/O operations.
PROG/$\overline{CE_1}$ CE_2	I	**CHIP ENABLE INPUTS:** $\overline{CE_1}$ is active low and CE_2 is active high. The 8755A can be accessed only when *both* Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7}, and READY ouputs will be in a high impedance state. $\overline{CE_1}$ is also used as a programming pin. (See section on programming.)
$IO/\overline{M}$	I	**I/O MEMORY:** If the latched $IO/\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$	I	**READ:** If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.
$\overline{IOW}$	I	**I/O WRITE:** If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of $IO/\overline{M}$ is ignored.
CLK	I	**CLOCK:** The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE_1}$ low, CE_2 high, and ALE high.
READY	O	**READY** is a 3-state output controlled by $\overline{CE_1}$, CE_2, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK. (See Figure 6c.)
PA_{0-7}	I/O	**PORT A:** These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0, AD_1. Read Operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 and AD_1 low, *or* $IO/\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 and AD_1 low.
PB_{0-7}	I/O	**PORT B:** The general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0 and a 0 from AD_1.
RESET	I	**RESET:** In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$	I	**I/O READ:** When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of $IO/\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}		**POWER:** +5V supply.
V_{SS}		**GROUND:** Reference.
V_{DD}		**POWER SUPPLY:** V_{DD} is a programming voltage, and must be tied to V_{CC} when the 8755A is being read. For programming, a high voltage is supplied with V_{DD} = 25V, typical. (See section on programming.)

FUNCTIONAL DESCRIPTION

PROM Section

The 8755A contains an 8-bit address latch which allows it to interface directly to MCS®-48 and MCS®-85 processors without additional hardware.

The PROM section of the chip is addressed by the 11-bit address and the Chip Enables. The address, $\overline{CE_1}$ and CE_2 are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the PROM location addressed by the latched address are put out on the AD_{0-7} lines (provided that V_{DD} is tied to V_{CC}).

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers (DDR) in 8755A determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the 8755A are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's cannot be read.

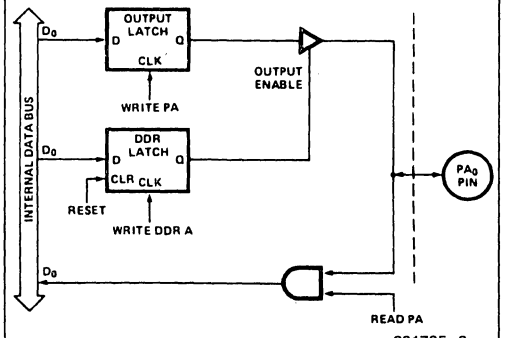
AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD_{0-7} is written into I/O port selected by the latched value of AD_{0-1}. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high. (Glitch free output.)

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O Ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

8755A ONE BIT OF PORT A AND DDR A



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WRITE PA = ($\overline{IOW}$ = 0) • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)
WRITE DDR A = ($\overline{IOW}$ = 0) • (CHIP ENABLES ACTIVE) • (DDR A ADDRESS SELECTED)
READ PA = {(IO/$\overline{M}$ = 1) • ($\overline{RD}$ = 0) + ($\overline{IOR}$ = 0)} • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)

NOTE:
Write PA is not qualified by IO/$\overline{M}$.

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the Output Latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

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ERASURE CHARACTERISTICS

The erasure characteristics of the 8755A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8755A in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755A window to prevent unintentional erasure.

The recommended erasure procedure for the 8755A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 8755A should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

Initially, and after each erasure, all bits of the EPROM portions of the 8755A are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755A can be programmed on the Intel Universal Programmer (iUP), and iUPF8744A programming module.

The program mode itself consists of programming a single address at a time, giving a single 50 msec pulse for every address. Generally, it is desirable to have a verify cycle after a program cycle for the same address as shown in the attached timing diagram. **In the verify cycle (i.e., normal memory read cycle) 'V_{DD}' should be at +5V.**

SYSTEM APPLICATIONS

System Interface with 8085AH

A system using the 8755A can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE_2 and $\overline{CE_1}$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the 8085AH system can use up to 5 8755A's without requiring a CE decoder. See Figure 4.

If a memory mapped I/O approach is used the 8755A will be selected by the combination of both the Chip Enables and IO/$\overline{M}$ using AD_{8-15} address lines. See Figure 3.

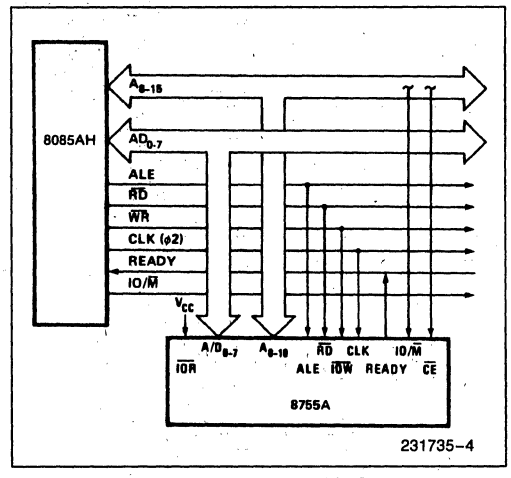
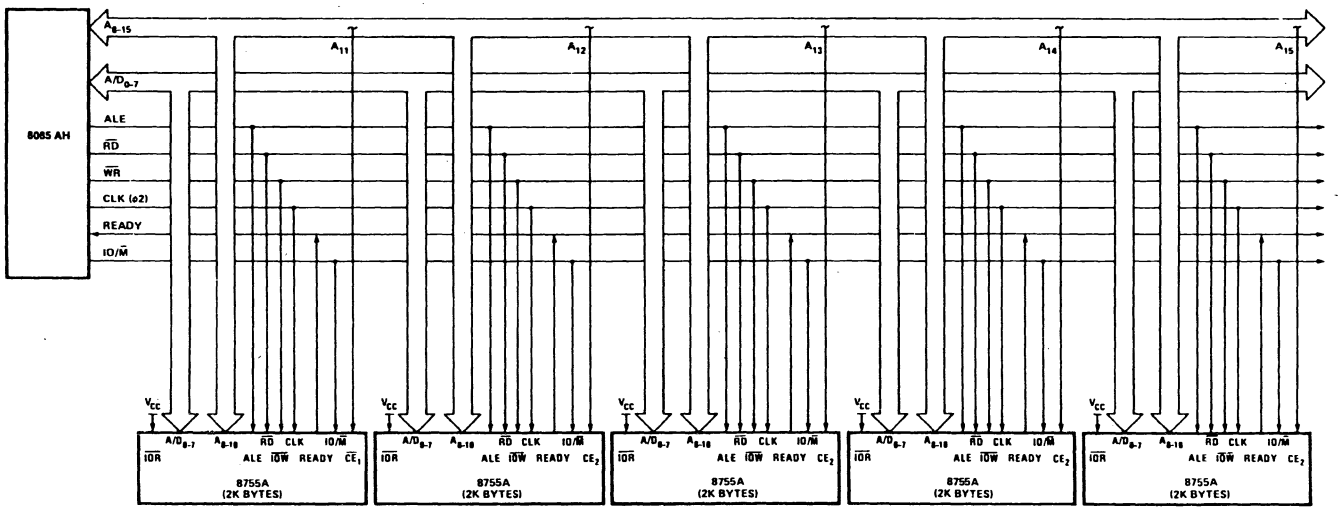


Figure 3. 8755A In 8085AH System (Memory-Mapped I/O)



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NOTE:
Use $\overline{CE_1}$ for the first 8755A in the system, and CE_2 for the other 8755A's. Permits up to 5-8755A's in a system without CE decoder.

Figure 4. 8755A in 8085AH System (Standard I/O)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on any Pin
with Respect to Ground.....−0.5V to +7V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = V_{DD} = 5V ±5%

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	V_{CC} = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Leakage		10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45V \le V_{OUT} \le V_{CC}$
I_{CC}	V_{CC} Supply Current		180	mA	
I_{DD}	V_{DD} Supply Current		30	mA	V_{DD} = V_{CC}
C_{IN}	Capacitance of Input Buffer		10	pF	f_C = 1 μHz
$C_{I/O}$	Capacitance of I/O Buffer		15	pF	f_C = 1 μHz

D.C. CHARACTERISTICS—PROGRAMMING

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V, V_{DD} = 25V ±1V

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Programming Voltage (during Write to EPROM)	24	25	26	V
I_{DD}	Prog Supply Current		15	30	mA

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	8755A		Unit
		Min	Max	
t_{CYC}	Clock Cycle Time	320		ns
T_1	CLK Pulse Width	80		ns
T_2	CLK Pulse Width	120		ns
t_f, t_r	CLK Rise and Fall Time		30	ns
t_{AL}	Address to Latch Set Up Time	50		ns
t_{LA}	Address Hold Time after Latch	80		ns
t_{LC}	Latch to READ/WRITE Control	100		ns
t_{RD}	Valid Data Out Delay from READ Control*		170	ns
t_{AD}	Address Stable to Data Out Valid**		450	ns
t_{LL}	Latch Enable Width	100		ns
t_{RDF}	Data Bus Float after READ	0	100	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		ns
t_{CC}	READ/WRITE Control Width	250		ns
t_{DW}	Data in Write Set Up Time	150		ns
t_{WD}	Data in Hold Time after WRITE	30		ns
t_{WP}	WRITE to Port Output		400	ns
t_{PR}	Port Input Set Up Time	50		ns
t_{RP}	Port Input Hold Time to Control	50		ns
t_{RYH}	READY HOLD Time to Control	0	160	ns
t_{ARY}	ADDRESS (CE) to READY		160	ns
t_{RV}	Recovery Time between Controls	300		ns
t_{RDE}	READ Control to Data Bus Enable	10		ns

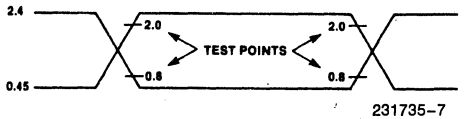
NOTES:
C_{LOAD} = 150 pF.
*Or $T_{AD} - (T_{AL} + T_{LC})$, whichever is greater.
**Defines ALE to Data Out Valid in conjunction with T_{AL}.

A.C. CHARACTERISTICS—PROGRAMMING

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V, V_{DD} = 25V ±1V

Symbol	Parameter	Min	Typ	Max	Unit
t_{PS}	Data Setup Time	10			ns
t_{PD}	Data Hold Time	0			ns
t_S	Prog Pulse Setup Time	2			μs
t_H	Prog Pulse Hold Time	2			μs
t_{PR}	Prog Pulse Rise Time	0.01	2		μs
t_{PF}	Prog Pulse Fall Time	0.01	2		μs
t_{PRG}	Prog Pulse Width	45	50		ms

A.C. TESTING INPUT, OUTPUT WAVEFORM



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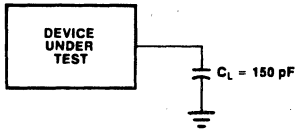
A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



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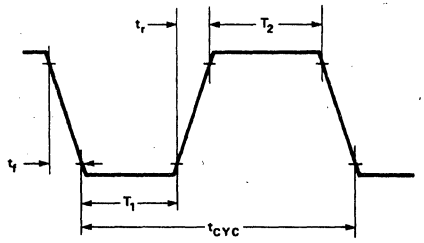
C_L = 150 pF
C_L Includes Jig Capacitance

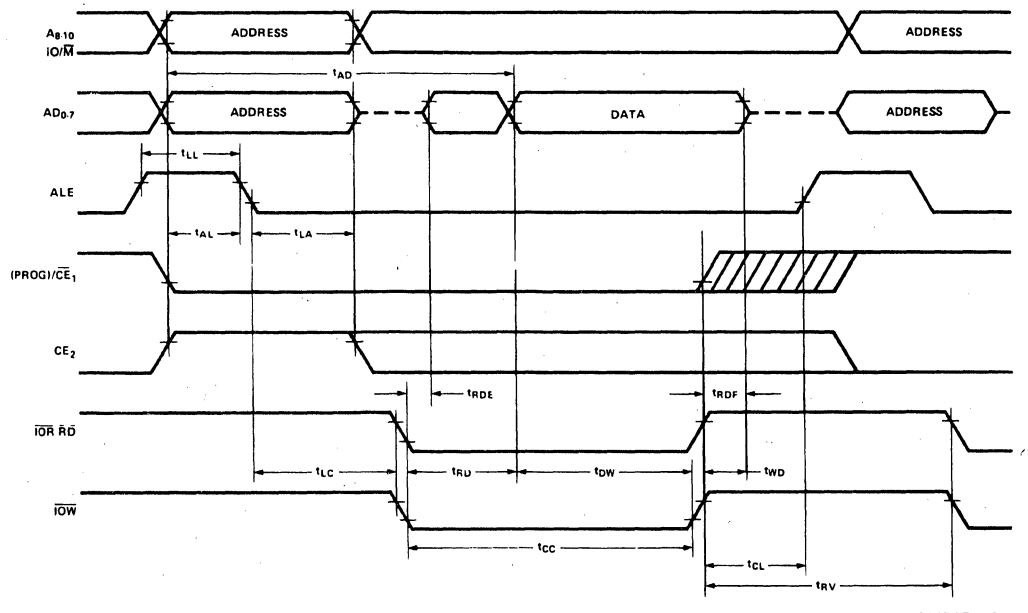
WAVEFORMS

CLOCK SPECIFICATION FOR 8755A



231735-9

PROM READ, I/O READ AND WRITE

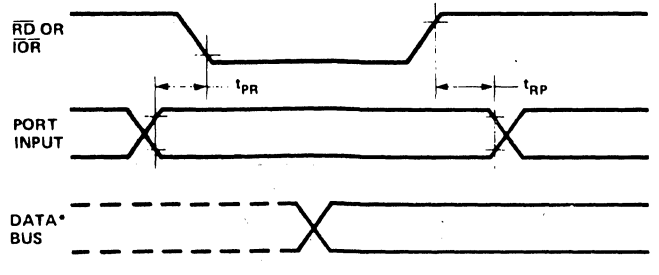


231735-10

Please note that **$\overline{CE_1}$ must remain low for the entire cycle.**

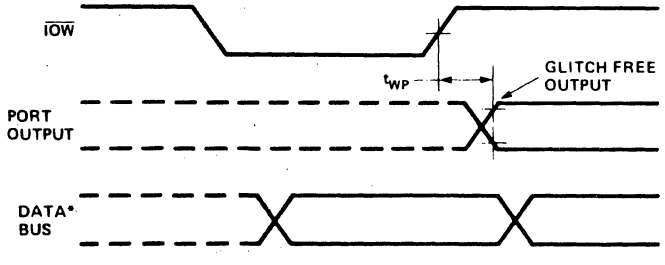
WAVEFORMS (Continued)

I/O PORT



231735-11

A. Input Mode



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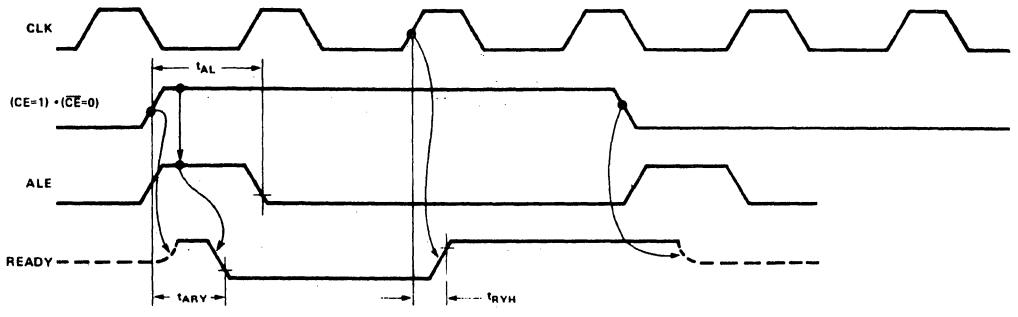
B. Output Mode

13

WAIT STATE (READY = 0)



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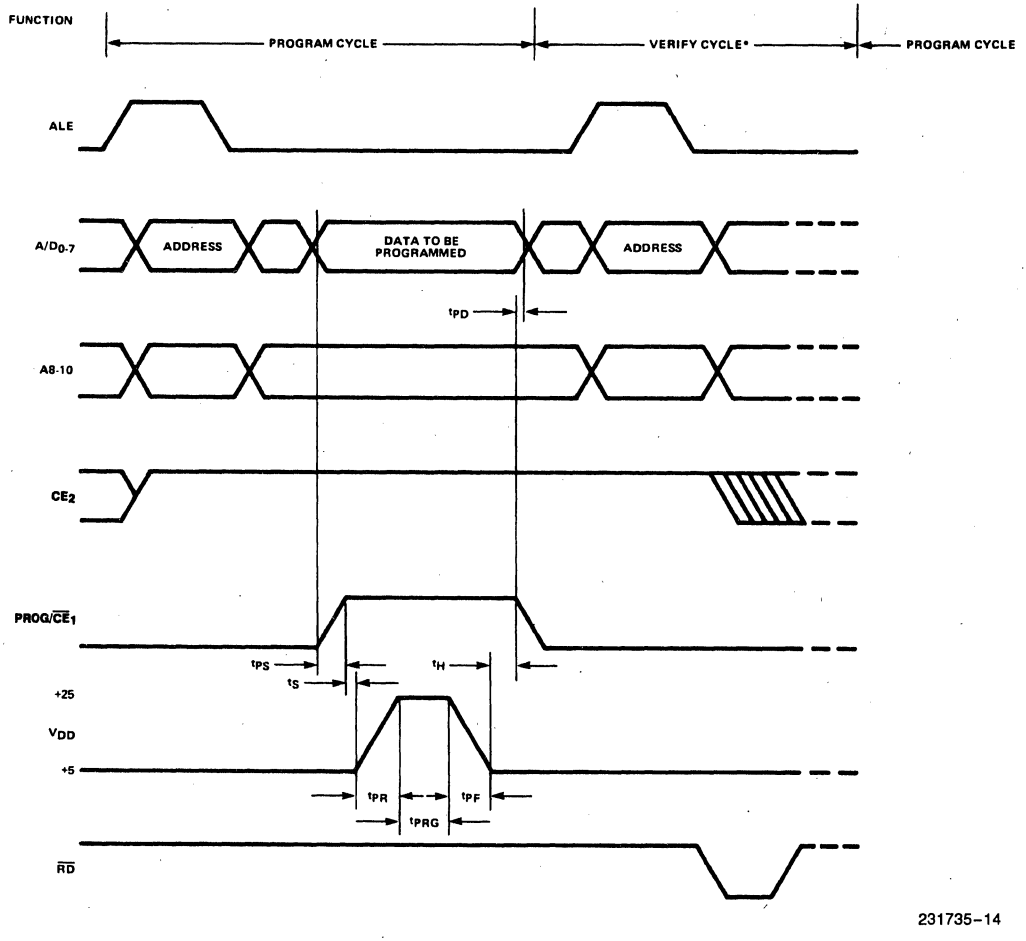
WAVEFORMS (Continued)

8755A PROGRAM MODE



*Verify cycle is a regular Memory Read Cycle (with V_{DD} = +5V for 8755A).

MCS®-96 Architectural Overview and Quick References

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intel®

September 1992

MCS®-96 Architectural Overview

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Order Number: 272109-002

MCS-96 Architectural Overview

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1.0 INTRODUCTION

The MCS-96 family members are all high performance microcontrollers with a 16-bit CPU and at least 230 bytes of on-chip RAM. The Intel MCS-96 family easily handles high speed calculations and fast input/output (I/O) operations. Typical applications include closed-loop control and mid-range digital signal processing. Modems, motor control system, printers, engine control system, photocopiers, anti-lock brakes, air conditioner control systems, disk drives and medical instrumentation all use MCS-96 products.

All of the MCS-96 components share a common instruction set and architecture. However, the CHMOS components have enhancements to provide higher performance with lower power consumption. To further decrease power usage, idle and power-down modes are available on these devices. These microcontrollers contain dedicated I/O subsystems and perform 16-bit arithmetic instructions including multiply and divide operations.

This overview briefly describes the MCS-96 instruction set and architecture and provides descriptions for the 8X9X, 80C196KB, 80C196KC and 80C196KR key features. Comprehensive user's guides that contain more information about these devices are available. Figure 1.1 shows a block diagram of the MCS-96 architecture.

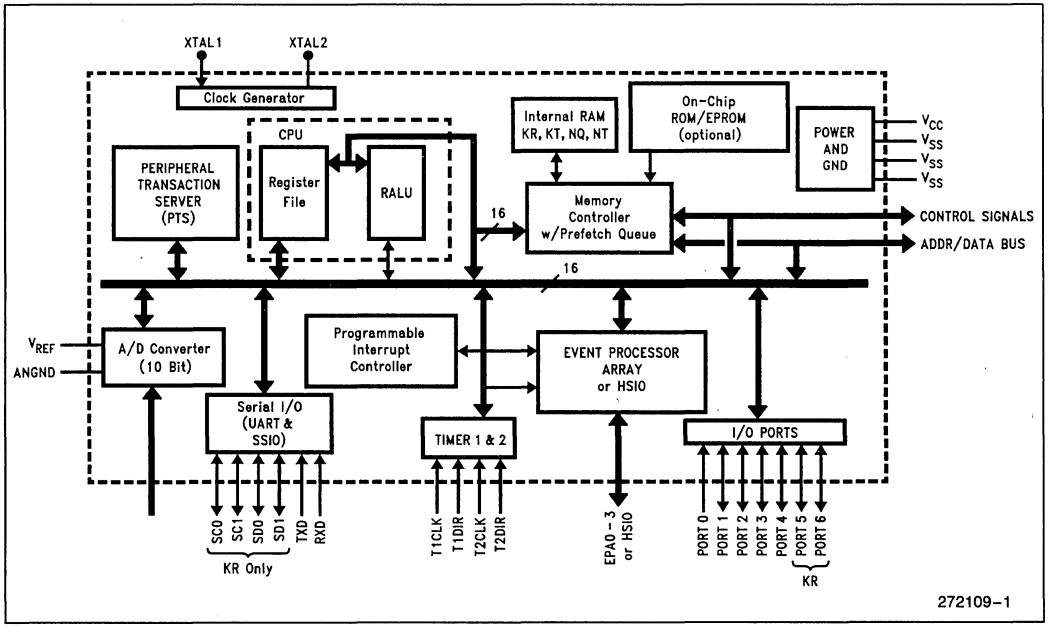

Figure 1.1. MCS-96 Block Diagram

2.0 THE CPU

The major components of the MCS-96 CPU are the Register File and the Register/Arithmetic Logic Unit (RALU). Locations 00H through 17H are the I/O control registers or Special Function Registers (SFRs). Locations 18H and 19H contain the stack pointer, which can serve as general purpose RAM when not performing stack operations. The remaining bytes of the register file serve as general purpose RAM, accessible as bytes, words or double-words.

Calculations performed by the CPU take place in the RALU. The RALU shown in Figure 2.1 contains a 17-bit ALU, the Program Status Word (PSW), the Program Counter (PC), a loop counter and three temporary registers. The RALU operates directly on the Register File, thus eliminating accumulator bottleneck and providing for direct control of I/O operations through the SFRs.

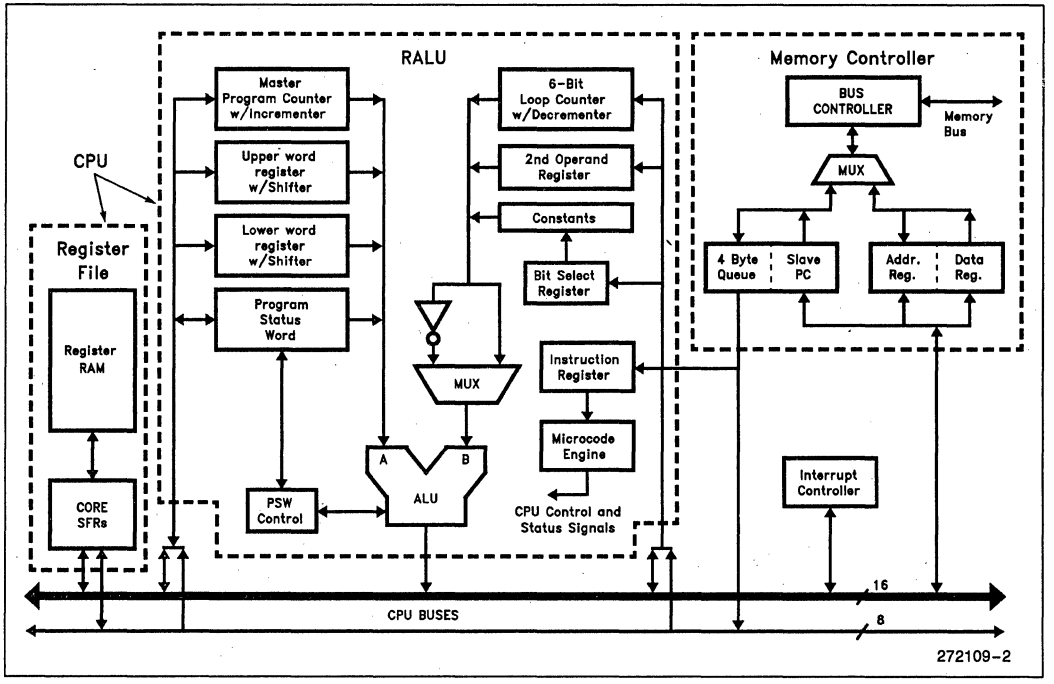

Figure 2.1 Block Diagram of the Register File, RALU, Memory Controller and Interrupt Controller

3.0 THE ARCHITECTURE

The MCS-96 supports a complete instruction set which includes bit operations, byte operations, word operations, double-word operations (unsigned 32-bit), long operations (signed 32-bit), flag manipulations as well as jump and call instructions. All the standard logical and arithmetic instructions function as both byte and word operations. The Jump Bit Set and Jump Bit Clear instructions can operate on any of the SFRs or bytes in the lower register file. These fast bit manipulations allow for rapid I/O functions.

Byte and word operations make-up most of the instruction set. The assembly language ASM-96 uses a "B" suffix on a mnemonic for a byte operation, otherwise the mnemonic refers to a word operation. One, two or three operand forms exist for many of the instructions.

Long and double-word operations include shifts, normlize, multiply and divide. The divide instruction functions as a 32-bit by 16-bit divide that generates a 16-bit quotient and 16-bit remainder. The word multiply operates as a 16-bit by 16-bit multiply with a 32-bit result. Both operations can function in either the signed or unsigned mode. The normalize instruction and sticky bit flag provide hardware support for the software floating point package (FPAL-96).

3.1 Addressing Modes

The MCS-96 instruction set supports the following addressing modes: register-direct, indirect, indirect with auto-increment, immediate, short-indexed and long-indexed. These modes increase the flexibility and overall execution speed of the MCS-96 devices. Each instruction uses at least one of the addressing modes. These modes and formats are shown in Figure 3.1.

```
Mnem      Dest or Src1                ;One operand direct
Mnem      Dest, Src1                  ;Two operand direct
Mnem      Dest, Src1, Src2            ;Three operand direct

Mnem      #Src1                       ;One operand immediate
Mnem      Dest, #Src1                 ;Two operand immediate
Mnem      Dest, Src1, #Src2           ;Three operand immediate

Mnem      [addr]                      ;One operand indirect
Mnem      [addr]+                     ;One operand indirect auto-increment
Mnem      Dest, [addr]                ;Two operand indirect
Mnem      Dest, [addr]+               ;Two operand indirect auto-increment
Mnem      Dest, Src1, [addr]          ;Three operand indirect
Mnem      Dest, Src1, [addr]+         ;Three operand indirect auto-increment

Mnem      Dest, offs[addr]            ;Two operand indexed (short or long)
Mnem      Dest, Src1, offs[addr]      ;Three operand indexed (short or long)
```

```
Where:
Mnem = instruction mnemonic
Dest = destination register
Src1, Src2 = source registers
addr = word register used in computing the address of an operand
offs = offset used in computing the address of an operand
```

Figure 3.1 Instruction Format

The register-direct and immediate addressing modes execute faster than the other addressing modes. The register-direct addressing mode provides access to the addresses in the register file and the SFRs. The indexed modes provide for direct access to the remainder of the 64K address space. Immediate addressing uses the data following the opcode as the operand.

Both of the indirect addressing modes use the value in a word register as the address of the operand. The indirect auto-increment mode increments a word address by one after a byte operation and two after a word operation. This addressing mode provides easy access into look-up tables.

The long-indexed addressing mode provides direct access to any of the locations in the 64K address space. This mode forms the address of the operand by adding a 16-bit 2's complement value to the contents of a word register. Indexing with the zero register allows "direct" addressing to any location. The short-indexed addressing mode forms the address of the operand by adding an 8-bit 2's complement value to the contents of a word register.

The 8XC196NT has 9 new instructions which have been implemented to support addressing the extended 1 Mbyte address space of the 8XC196NT family. Four extended load and store instructions using indirect, indirect auto increment, or extended indexed addressing, can be used to address the 1 Mbyte address space. Three instructions are for extended calls, branches, and jumps. An extended version of the interruptible and non-interruptible block moves have also been implemented.

The multiple addressing modes of the MCS-96 make it easy to program in assembly language and provide an excellent interface to high-level languages. The instructions accepted by the assembler consist of mnemonics followed by either addresses or data. Refer to the Quick Reference section for Instruction Summary tables for each device. The MCS-96 Macro Assembler Users Guide contains additional ASM96 information.

4.0 8X9X PERIPHERALS

Standard I/O Ports—The 8X9X has five 8-bit I/O ports. Port 0 is an input port that is also the anlog input for the A/D converter. Port 1 is a quasi-bidirectional port. Port 2 contains three types of port lines: quasi-bidirectional, input and output. Other functions on the 8X9X share the input and output lines with Port 2. Ports 3 and 4 are open-drain bidirectional ports that share their pins with the address/data bus.

Timers—The 8X9X has two 16-bit timers, Timer1 and Timer2. An internal clock increments the Timer1 value every 8 state times. (A state time is 3 oscillator periods.) An external clock increments Timer2 on every positive and negative transition. Either an internal or external source can reset Timer2. Timer1 and Timer2 can generate an interrupt when crossing the 0FFFFH/0000H boundary. The 8X9X also includes separate, dedicated timers for the Serial Port baud rate generator and Watchdog Timer. The Watchdog Timer is an internal timer that resets the system if the software fails to operate properly.

Table 1. MCS-96 Family Devices

Product	Timers	HSIO /EPA	A/D CHS	Serial Port	Synch. Serial Port	PWMS	PTS	Slave Port	3-Phase Waveform Generator
8098	2	HSIO	4	YES		1			
8097BH	2	HSIO	8	YES		1			
8097JF	2	HSIO	8	YES		1			
80C198	2	HSIO	4	YES		1			
80C196KB	2	HSIO	8	YES		1			
80C196KC	2	HSIO	8	YES		3	YES		
80C196KD	2	HSIO	8	YES		3	YES		
80C196KR	2	EPA	8	YES	YES		YES	YES	
80C196KT	2	EPA	8	YES	YES		YES	YES	
80C196NT	2	EPA	4	YES	YES		YES	YES	
80C196MC	2	EPA	13	YES			YES		YES

High Speed Input Unit (HSI)—The 8X9X HSI unit can record times of external events with a 9 state time resolution. It can monitor four independently configurable HSI lines and capture the value of Timer1 when an event(s) takes place. The four types of events that can trigger captures include: rising edges only, falling edges only, rising or falling edges, or every eighth rising edge. The HSI unit can store up to 8 entries (Timer1 values). Reading the HSI holding register unloads the earliest entry placed in the FIFO. The HSI unit can generate an interrupt when loading an entry into the HSI holding register or loading the sixth entry into the FIFO.

High Speed Output Unit (HSO)—The 8X9X HSO unit can trigger events at specified times based on Timer1 or Timer2. These programmable events include: starting an A/D conversion, resetting Timer2, generating up to four software time delays, and setting or clearing one or more of the 6 HSO output lines. The HSO unit stores pending events and the specified times in a Content Addressable Memory (CAM) file. This file stores up to eight commands. Each command specifies the action time, the nature of the action, whether an interrupt is to occur, and whether Timer1 or Timer2 is the reference timer. Every 8 state times the HSO compares the CAM locations for time matches. The HSO unit triggers the specified event when it finds a time match. A command is cleared from the CAM as soon as it executes.

The Serial Port—The Serial Port on the 8X9X has one synchronous (Mode 0) and three asynchronous modes (Modes 1, 2 and 3). The asynchronous modes are full duplex, meaning they can transmit and receive data simultaneously. The receiver on the 8X9X is buffered so the reception of a second byte may begin before the first byte is read. The most common use of Mode 0, the synchronous mode, is to expand the I/O capability of the 8X9X using shift registers. Mode 1 is the standard asynchronous mode used for normal serial communication. The data frame for Mode 1 consists of 10 bits: a start bit, 8 data bits (LSB first) and a stop bit. If parity is enabled (PEN = 1), an even parity bit is sent instead of the 8th data bit. Modes 2 and 3 are 9-bit modes commonly used for multiprocessor communications. The data frame used in these modes consists of 11 bits: a start bit, nine data bits (LSB first) and a stop bit. Devices in Mode 2 will interrupt upon reception only if the 9th data bit is set. Devices in Mode 3 will always interrupt upon reception. Mode 3 also allows transmission of 8 data bits plus an even parity bit.

Pulse Width Modulator (PWM)—The PWM output waveform is a variable duty cycle pulse that repeats every 256 state times. The Pulse Width Modulator of the 8X9X can provide useful signals for a variety of applications. The PWM output can perform digital to analog conversions and drive several types of motors that require a PWM waveform for more efficient operation.

A/D Converter—The 8X9X A/D Converter converts an analog input to a 10-bit digital equivalent. The main components of the A/D Converter are: 8 analog inputs, an 8 to 1 multiplexer, a sample and hold capacitor and the resistor ladder. The A/D Quick Reference section defines the A/D terms. The A/D Converter can start a conversion immediately or the High Speed Output unit can trigger a conversion at a preprogrammed time. The A/D Converter performs a conversion in 88 state times. Upon completion of each conversion the converter can generate a conversion complete interrupt. The 8X9X provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 21 interrupt sources and 8 interrupt vectors on the 8X9X. When the interrupt controller detects one of the 8 interrupts it sets the corresponding bit in the interrupt pending register. Individual interrupts are enabled or disabled by setting or clearing bits in the interrupt mask register. When the interrupt controller decides to process an interrupt, it executes a "call" to an Interrupt Service Routine (ISR). The corresponding interrupt vector contains the address of the ISR. The interrupt controller then clears the associated pending bit.

5.0 8XC196KB PERIPHERALS

Standard I/O Ports—The 8XC196KB has five 8-bit I/O ports. Port 0 is an input port that is also the analog input for the A/D converter. Port 1 is a quasi-bidirectional port. Port 2 contains three types of port lines: quasi-bidirectional, input and output. Other functions on the 8XC196KB share the input and output lines with Port 2. Ports 3 and 4 are open-drain bidirectional ports that share their pins with the address/data bus.

Timers—The 8XC196KB has two 16-bit timers, Timer1 and Timer2. An internal clock increments the Timer1 value every 8 state times. (A state time is 2 oscillator periods.) An external clock increments or decrements Timer2 on every positive and negative transition. Either an internal or external source can reset Timer2. Timer1 can generate an interrupt when crossing the 0FFFFH/0000H boundary. Timer2 can generate an interrupt when crossing the 0FFFFH/0000H boundary or the 7FFFH/8000H boundary. The 8XC196KB also includes separate, dedicated timers for the baud rate generator and Watchdog Timer. The Watchdog Timer is an internal timer that resets the system if the software fails to operate properly.

High Speed Input Unit (HSI)—The 8XC196KB HSI unit can record times of external events with a 9 state time resolution. It can monitor four independently configurable HSI lines and capture the value of Timer1 when an event(s) takes place. The four types of events that can trigger captures include: rising edges only, falling edges only, rising or falling edges, or every eighth rising edge. The HSI unit can store up to 8 entries (Timer1 values), 7 in the 7-level FIFO and 1 in the HSI holding register. Reading the HSI holding register unloads the earliest entry placed in the FIFO. The HSI unit can generate an interrupt when: loading an entry into the HSI holding register, loading the fourth entry into the FIFO or loading the sixth entry into the FIFO.

High Speed Output Unit (HSO)—The 8XC196KB HSO unit can trigger events at specified times based on Timer1 or Timer2. These programmable events include: starting an A/D conversion, resetting Timer2, generating up to four software time delays, and setting or clearing one or more of the 6 HSO output lines. The HSO unit stores pending events and the specified times in a Content Addressable Memory (CAM) file. This file stores up to eight commands. Each command specifies the action time, the nature of the action, whether an interrupt is to occur, and whether Timer1 or Timer2 is the reference timer. Every 8 state times the HSO compares the CAM locations for time matches. The HSO unit triggers the specified event when it finds a time match. A command can either clear from the CAM as soon as it executes or remain in the CAM as a locked CAM entry and continue to execute whenever its time tag matches the reference timer. Locked entries are useful in applications requiring periodic or repetitive events to occur such as multiple PWMs.

The Serial Port—The Serial Port on the 8XC196KB has one synchronous (Mode 0) and three asynchronous modes (Modes 1, 2 and 3). The asynchronous modes are full duplex, meaning they can transmit and receive data simultaneously. The receiver on the 8XC196KB is buffered so the reception of a second byte may begin before the first byte is read. The transmitter is also double buffered and can generate continual transmissions. The most common use of Mode 0, the synchronous mode, is to expand the I/O capability of the 8XC196KB using shift registers. Mode 1 is the standard asynchronous mode used for normal serial communication. The data frame for Mode 1 consists of 10 bits: a start bit, 8 data bits (LSB first) and a stop bit. If parity is enabled (PEN = 1), an even parity bit is sent instead of the 8th data bit. Modes 2 and 3 are 9-bit modes commonly used for multiprocessor communications. The data frame used in these modes consists of 11 bits: a start bit, nine data bits (LSB first) and a stop bit. Devices in Mode 2 will interrupt upon reception only if the 9th data bit is set. Devices in Mode 3 will always interrupt upon reception. Mode 3 also allows transmission of 8 data bits plus an even parity bit.

Pulse Width Modulator (PWM)—The Pulse Width Modulator of the 8XC196KB can provide useful signals for a variety of applications. The PWM output can perform digital to analog conversions and drive several types of motors that require a PWM waveform for more efficient operaton. The PWM output waveform is a variable duty cycle pulse that repeats every 256 state times or 512 state times.

A/D Converter—The 8XC196KB A/D Converter converts an analog input to a 10-bit digital equivalent. The main components of the A/D Converter are: 8 analog inputs, an 8 to 1 multiplexer, a sample and hold capacitor and the resistor ladder. Refer to the data sheet for all specifications on A/D performance. The A/D Quick Reference section defines the A/D terms. The A/D Converter can start a conversion immediately or the High Speed Output unit can trigger a conversion at a preprogrammed time. The A/D Converter can perform a conversion in either 91 state times for low crystal frequencies and 158 state times for higher crystal frequencies. Upon completion of each conversion the converter generates a conversion complete interrupt. The 8XC196KB provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 28 interrupt sources and 16 interrupt vectors on the 8XC196KB. Additionally, there are 2 special interrupt vectors for Software Trap and Unimplemented Opcodes. When the interrupt controller detects one of the 16 interrupts it sets the corresponding bit in one of two interrupt pending registers. Individual interrupts are enabled or disabled by setting or clearing bits in the interrupt mask registers. When the interrupt controller decides to process an interrupt, it executes a "call" to an Interrupt Service Routine (ISR). The corresponding interrupt vector contains the address of the ISR. The interrupt controller then clears the associated pending bit.

6.0 8XC196KC and 8XC196KD PERIPHERALS

Standard I/O Ports—The 8XC196KC/KD has five 8-bit I/O ports. Port 0 is an input port that is also the analog input for the A/D converter. Port 1 is a quasi-bidirectional port that shares pins with two PWM outputs. Port 2 contains three types of port lines: quasi-bidirectional, input and output. Other functions on the 8XC196KC/KD share the input and output lines with Port 2. Ports 3 and 4 are open-drain bidirectional ports that share their pins with the address/data bus.

Timers—The 8XC196KC/KD has two 16-bit timers, Timer1 and Timer2. An internal clock increments the Timer1 value every 8 state times. (A state time is 2 oscillator periods.) An internal clock or an external clock can drive Timer2. When clocked internally Timer2 can increment every 1 or 8 state times. When clocked externally Timer2 increments or decrements on every positive and negative transition. Either an internal or external source can reset Timer2. Timer1 can generate an interrupt when crossing the 0FFFFH/0000H boundary. Timer2 can generate an interrupt when crossing the 0FFFFH/0000H boundary or the 7FFFH/8000H boundary. The 8XC196KC/KD also includes separate, dedicated timers for the baud rate generator and Watchdog Timer. The Watchdog Timer is an internal timer that resets the system if the software fails to operate properly.

High Speed Input Unit (HSI)—The 8XC196KC/KD HSI unit can record times of external events with a 9 state time resolution. It can monitor four independently configurable HSI lines and capture the value of Timer1 when an event(s) takes place. The four types of events that can trigger captures include: rising edges only, falling edges only, rising or falling edges, or every eighth rising edge. The HSI unit can store up to 8 entries (Timer1 values), 7 in the 7-level FIFO and 1 in the HSI holding register. Reading the HSI holding register unloads the earliest entry placed in the FIFO. The HSI unit can generate an interrupt when: loading an entry into the HSI holding register, loading the fourth entry into the FIFO or loading the sixth entry into the FIFO.

High Speed Output Unit (HSO)—The 8XC196KC/KD HSO unit can trigger events at specified times based on Timer1 or Timer2. These programmable events include: starting an A/D conversion, resetting Timer2, generating up to four software timers, and setting or clearing one or more of the 6 HSO output lines. The HSO unit stores pending events and the specified times in a Content Addressable Memory (CAM) file. This file stores up to eight commands. Each command specifies the action time, the nature of the action, whether an interrupt is to occur, and whether Timer1 or Timer2 is the reference timer. Every 8 state times the HSO compares the CAM locations for time matches. The HSO unit triggers the specified event when it finds a time match. A command can either clear from the CAM as soon as it executes or remain in the CAM as a locked CAM entry and continue to execute whenever its time tag matches the reference timer. Locked entries are useful in applications requiring periodic or repetitive events to occur such as multiple PWMs.

The Serial Port—The Serial Port on the 8XC196KC/KD has one synchronous (Mode 0) and three asynchronous modes (Modes 1, 2 and 3). The asynchronous modes are full duplex, meaning they can transmit and receive data simultaneously. The receiver on the 8XC196KC/KD is buffered so the reception of a second byte may begin before the first byte is read. The transmitter is also double bufered and can generate continual transmissions. The most common use of Mode 0, the synchronous mode, is to expand the I/O capability of the 8XC196KC/KD using shift registers. Mode 1 is the standard asynchronous mode used for normal serial communication. The data frame for Mode 1 consists of 10 bits: a start bit, 8 data bits (LSB first) and a stop bit. If parity is enabled (PEN = 1), an even parity bit is sent instead of the 8th data bit. Modes 2 and 3 are 9-bit modes commonly used for multiprocessor communications. The data frame used in these modes consists of 11 bits: a start bit, nine data bits (LSB first) and a stop bit. Devices in Mode 2 will interrupt upon reception only if the 9th data bit is set. Devices in Mode 3 will always interrupt upon reception. Mode 3 also allows transmission of 8 data bits plus an even parity bit.

Pulse Width Modulator (PWM)—The 8CX196KC/KD has 3 PWM outputs. The output waveform is a variable duty cycle pulse which is selectable to repeat every 256 state times or 512 state times. Several types of motors require a PWM waveform for most efficient operation. Additionally, filtering this waveform will produce a DC level that can change in 256 steps by varying the duty cycle.

A/D Converter—The 8XC196KC/KD A/D Converter converts an analog input to a digital equivalent. Resolution is either 8 or 10 bits with programmable sample and convert times. The main components of the A/D Converter are: a sample and hold, an 8-channel multiplexer, and an 8-bit or 10-bit successive approximation analog-to-digital converter. Refer to the data sheet for all specifications on A/D performance. The A/D Quick Reference section defines the A/D terms. The converter can start a conversion immediately or the High Speed Output unit can trigger a conversion at a preprogrammed time. Upon completion of each conversion the converter generates a conversion complete interrupt. The 8XC196KC/KD provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 28 interrupt sources and 16 interrupt vectors on the 8XC196KC/KD. In addition there are 2 special interrupt vectors (Software Trap and Unimplemented Opcode) used in Intel development tools or evaluation boards. When the interrupt controller detects one of the 16 interrupts it sets the corresponding bit in one of two interrupt pending registers. Individual interrupts are enabled or disabled by setting or clearing bits in the interrupt mask registers. When the interrupt controller decides to process an interrupt, it executes a "call" to an Interrupt Service Routine (ISR). The corresponding interrupt vector contains the address of the ISR. The interrupt controller then clears the associated pending bit.

Peripheral Transaction Server (PTS)—The PTS is a microcoded hardware interrupt processor. It responds to interrupts with a fixed set of actions. These actions consist of: transferring data, starting an A/D conversion, reading the HSI FIFO and loading HSO events. The PTS completes these tasks much faster than using interrupt driven service routines. The PTS can service all interrupts except NMI, Trap and Unimplemented Opcode. Each interrupt managed by the PTS requires a block of data called the PTS Control Block (PTSCB). Each PTSCB requires 8 data bytes in register RAM. The PTSCB determines: the type of PTS, the number of PTS responses (if applicable), the source for data and the destination (if applicable). PTS cycles have a higher priority than interrupts and may temporarily suspend interrupt service routines.

7.0 8XC196KR and 8XC196KT PERIPHERALS

Standard I/O Ports—The 8XC196KR/KT has six 8-bit I/O ports. Each pin operates as a dedicated input or output. Most pins also have an alternate function. The KR/KT does not use the quasi-bidirectional port pins found on previous MCS-96 devices. As an input, the pin is a true high impedance with no pull-ups or pull-downs. Most ports (Ports 1, 2, 5 and 6) have direction registers (Px__DIR), mode registers (Px__MODE), data input registers (Px__PIN) and data output registers (Px__REG). This allows the user to configure each port pin as input, output, open-drain output or alternate function. Ports 3 and 4 have Px__PIN and Px__REG registers and lack internal pull-ups. As standard outputs, these pins can only function in open-drain mode and need external pull-ups. Ports 3 and 4 also are the multiplexed address/data bus. When emitting the address, an internal pull-up device is active and does not need external pull-ups. Port 0 is the analog input port, and only has a Px__PIN register because there are no output drivers. As a digital port, Port 0 pins can only function as inputs.

Event Processor Array (EPA)—The EPA performs input event capture and output event generation functions using Timer1 and Timer2. It consists of 10 capture/compare modules, 2 compare only modules and the 2 timers. In capture mode, when an external event occurs the EPA stores the value of the timer, generates an interrupt or both. A rising, falling, or any edge can trigger a capture. All captures are double buffered. In compare mode, when the timer matches the value in the compare register the EPA changes the state of an output pin, generates an interrupt, or both. The EPA sets, resets or toggles the pin when the compare occurs. The timers can count up or count down. The clock source to the timers can be internal or external. The clock also goes through a programmable prescaler. The prescaler divides the oscillator frequency within a range of 1 to 64. The EPA also allows two channels to control a single output pin that is useful for high-speed PWM generation.

Serial I/O Port (SIO)—The SIO (also known as the UART) supports 8- or 9-bit data frames with one synchronous mode and 3 asynchronous modes. The synchronous mode transmits or receives 8 bits of data without start or stop bits and generates a shift clock. All other devices must synchronize to the 8XC196KR/KT's shift clock. The asynchronous frames contain a start and stop bit, making them either 10 or 11 bits long. The 11-bit frames allow implementation of specialized multiprocessor communication interfaces. Two of the asynchronous modes support parity error detection. All three asynchronous modes support full or half duplex operation. Also included is a dedicated baud rate generator. The SIO on the 8XC196KR/KT is compatible with all MCS-96 and MCS-51 devices.

Synchronous Serial I/O Port (SSIO)—The SSIO includes two Serial I/O communication ports with separate data and clock pins. The data format is eight data bits only. The clock and data pins can be inputs or outputs. This peripheral supports several standard synchronous serial protocols. A handshake mode allows two serial channels to transfer data without requiring extra lines to convey their status. The handshake mode also permits servicing of the SSIO by the PTS. The serial channel includes a dedicated baud rate generator. Each channel has a single byte buffer. If clocked externally, both channels can simultaneously operate at different frequencies. Maximum baud rate is $1/8$ the oscillator frequency. The transmission or reception of a byte sets an interrupt pending flag.

A/D Converter—Converts analog inputs to a digital equivalent. Resolution is either 8 or 10 bits with programmable sample and convert times. The main components of the A/D converter are: 8 analog inputs, 8 to 1 multiplexer, sample and hold capacitor and the resistor ladder. Refer to the data sheet for all specifications on A/D performance. The A/D Quick Reference section defines the A/D terms. Another function implemented with the A/D converter is threshold detection. The converter generates an interrupt when the analog input is greater than or less than a programmed digital value. The KR/KT provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 37 interrupt sources and 18 interrupt vectors on the 8XC196KR/KT. With so many more sources than vectors, the KR/KT implements indirect interrupts. 17 of the interrupts are direct, which means each interrupt has one source and a dedicated vector location. The remaining 20 interrupt sources are the indirect interrupts. The term indirect is used because they share the same interrupt vector and another register identifies the interrupt source. The register, EPAIPV, contains the highest ending interrupt. EPAIPV is read to determine the interrupt needing sevice. The TIJMP instruction with EPAIPV simplifies the servicing of indirect interrupts. The direct interrupts include: NMI, External Interrupt, Trap, Unimplemented Opcode, SIO interrupts, SSIO interrupts, slave port interrupts, A/D converter and the lower 4 EPA channels. The indirect interrupts include: the upper 6 EPA channels, the 2 compare channels, all 10 EPA overruns and both timer overflows.

Peripheral Transaction Server (PTS)—The PTS is a microcoded hardware interrupt processor. It responds to interrupts with a fixed set of actions. These actions consist of: transferring data, starting an A/D conversion or generating PWM outputs. The PTS completes these tasks much faster than using interrupt driven service routines. The PTS can service all interrupts except NMI, Trap and Unimplemented Opcode. The register PTSSEL selects the interrupts handled by the PTS. Each interrupt managed by the PTS requires a block of data called the PTS Control Block (PTSCB). Each PTSCB requires 8 data bytes in register RAM. The PTSCB determines: the type of PTS, the number of PTS responses (if applicable), the source for data and the destination (if applicable). PTS cycles have a higher priority than interrupts and may temporarily suspend interrupt service routines.

Slave Port—The slave port is an interface between the KR/KT and a microprocessor. The KR/KT sits on the address/data bus of the processor and is accessed as a memory mapped peripheral. The slave port includes: a chip select input, 8-bit bidirectional data bus, an address input line, ALE input (to latch the address), $\overline{WR}$ and $\overline{RD}$ inputs to input/output data and an interrupt output. The address line and the $\overline{RD}/\overline{WR}$ select which registers are accessed (Output data, Status output, Input data or Command input). The various control signals and port structure allow the KR/KT and the processor to communicate with each other without having to be synchronized.

8.0 8XC196NT PERIPHERALS

Extended Address Port (EPORT)—The 80C196NT is the first member of the MCS-96 family to offer addressing that exceeds 64 Kbytes. The 80C196NT has a 1 Mbyte liner address space which is implemented through 4 address lines added by the EPORT. EPORT lines are individually assigned to function as either address or I/O. When assigned as I/O, they have the same functionality as a standard I/O port. As an input, the pin is a true high-impedance with no pull-ups or pull-downs. As an output, the pin is either complementary or open-drain. When assigned as address, the EPORT outputs address A16–A19. The address is strongly driven through the entire bus cycle, eliminating the need for an address latch.

Standard I/O Ports—The 8XC196NT has six 8-bit I/O ports. Each pin operates as a dedicated input or output. Most pins also have an alternate function. The NT does not use the quasi-bidirectional port pins found on previous MCS-96 devices. As an input, the pin is a true high impedance with no pull-ups or pull-downs. Most ports (Ports 1, 2, 5 and 6) have direction registers (Px__DIR), mode registers (Px__MODE), data input registers (Px__PIN) and data output registers (Px__REG). This allows the user to configure each port pin as input, output, open-drain output or alternate function. Ports 3 and 4 have Px__PIN and Px__REG registers and lack internal pull-ups. As standard outputs, these pins can only function in open-drain mode and need external pull-ups. Ports 3 and 4 also are the multiplexed address/data bus. When emitting the address, an internal pull-up device is active and does not need external pull-ups. Port 0 is the analog input port, and only has a Px__PIN register because there are no output drivers. As a digital port, Port 0 pins can only function as inputs.

Event Processor Array (EPA)—The EPA performs input event capture and output event generation functions using Timer1 and Timer2. It consists of 10 capture/compare modules, 2 compare only modules and the 2 timers. In capture mode, when an external event occurs the EPA stores the value of the timer, generates an interrupt or both. A rising, falling, or any edge can trigger a capture. All captures are double buffered. In compare mode, when the timer matches the value in the compare register the EPA changes the state of an output pin, generates an interrupt, or both. The EPA sets, resets or toggles the pin when the compare occurs. The timers can count up or count down. The clock source to the timers can be internal or external. The clock also goes through a programmable prescaler. The prescaler divides the oscillator frequency within a range of 1 to 64. The EPA also allows two channels to control a single output pin that is useful for high-speed PWM generation.

Serial I/O Port (SIO)—The SIO (also known as the UART) supports 8- or 9-bit data frames with one synchronous mode and 3 asynchronous modes. The synchronous mode transmits or receives 8 bits of data without start or stop bits and generates a shift clock. All other devices must synchronize to the 8XC196NT's shift clock. The asynchronous frames contain a start and stop bit, making them either 10 or 11 bits long. The 11-bit frames allow implementation of specialized multiprocessor communication interfaces. Two of the asynchronous modes support parity error detection. All three asynchronous modes support full or half duplex operation. Also included is a dedicated baud rate generator. The SIO on the 8XC196NT is compatible with all MCS-96 and MCS-51 devices.

Synchronous Serial I/O Port (SSIO)—The SSIO includes two Serial I/O communication ports with separate data and clock pins. The data format is eight data bits only. The clock and data pins can be inputs or outputs. This peripheral supports several standard synchronous serial protocols. A handshake mode allows two serial channels to transfer data without requiring extra lines to convey their status. The handshake mode also permits servicing of the SSIO by the PTS. The serial channel includes a dedicated baud rate generator. Each channel has a single byte buffer. If clocked externally, both channels can simultaneously operate at different frequencies. Maximum baud rate is $\frac{1}{8}$ the oscillator frequency. The transmission or reception of a byte sets an interrupt pending flag.

A/D Converter—Converts analog inputs to a digital equivalent. Resolution is either 8 or 10 bits with programmable sample and convert times. The main components of the A/D converter are: 4 analog inputs, 4 to 1 multiplexer, sample and hold capacitor and the resistor ladder. Refer to the data sheet for all specifications on A/D performance. The A/D Quick Reference section defines the A/D terms. Another function implemented with the A/D converter is threshold detection. The converter generates an interrupt when the analog input is greater than or less than a programmed digital value. The NT provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 37 interrupt sources and 18 interrupt vectors on the 8XC196NT. With so many more sources than vectors, the NT implements indirect interrupts. 17 of the interrupts are direct, which means each interrupt has one source and a dedicated vector location. The remaining 20 interrupt sources are the indirect interrupts. The term indirect is used because they share the same interrupt vector and another register identifies the interrupt source. The register, EPAIPV, contains the highest ending interrupt. EPAIPV is read to determine the interrupt needing service. The TIJMP instruction with EPAIPV simplifies the servicing of indirect interrupts. The direct interrupts include: NMI, External Interrupt, Trap, Unimplemented Opcode, SIO interrupts, SSIO interrupts, slave port interrupts, A/D converter and the lower 4 EPA channels. The indirect interrupts include: the upper 6 EPA channels, the 2 compare channels, all 10 EPA overruns and both timer overflows.

Peripheral Transaction Server (PTS)—The PTS is a microcoded hardware interrupt processor. It responds to interrupts with a fixed set of actions. These actions consist of: transferring data, starting an A/D conversion or generating PWM outputs. The PTS completes these tasks much faster than using interrupt driven service routines. The PTS can service all interrupts except NMI, Trap and Unimplemented Opcode. The register PTSSEL selects the interrupts handled by the PTS. Each interrupt managed by the PTS requires a block of data called the PTS Control Block (PTSCB). Each PTSCB requires 8 data bytes in register RAM. The PTSCB determines: the type of PTS, the number of PTS responses (if applicable), the source for data and the destination (if applicable). PTS cycles have a higher priority than interrupts and may temporarily suspend interrupt service routines.

Slave Port—The slave port is an interface between the NT and a microprocessor. The NT sits on the address/data bus of the processor and is accessed as a memory mapped peripheral. The slave port includes: a chip select input, 8-bit bidirectional data bus, an address input line, ALE input (to latch the address), $\overline{WR}$ and $\overline{RD}$ inputs to input/output data and an interrupt output. The address line and the $\overline{RD}/\overline{WR}$ select which registers are accessed (Output data, Status output, Input data or Command input). The various control signals and port structure allow the NT and the processor to communicate with each other without having to be synchronized.

9.0 8XC196MC PERIPHERALS

On-Chip Peripherals—The 8XC196MC's on-chip peripherals provide special functions useful in a variety of applications. The peripherals are monitored and controlled via special function registers (SFRs) that can be accessed indirectly or windowed and thereby treated as CPU "accumulators."

I/O Ports—The 8XC196MC has 7 I/O ports, labeled 0–6. Individual port pins are multiplexed to serve for standard I/O or to carry special signals. All ports are 8-bit except port 1 which is a 5-bit port.

Ports 0, 1, 2 and 6 are controlled by SFRs that can be directly addressed by the RALU through a window in the register file. Ports 0 and 1 serve as input to the 13-channel A/D, and can also be read as digital inputs. Port 2 can be configured either as standard I/O ports or to serve special functions. Port 6 is the output port for the PWM and WG units.

Ports 3, 4 and 5 are memory mapped and cannot be windowed. These ports are accessed only via 16-bit addresses. Ports 3 and 4 also serve as the 16-bit external address/data bus. The Port 5 lines can be selected for standard I/O or to serve as system bus control pins.

Timers and the Event Processor Array (EPA)—The Event Processor Array (EPA) performs input and output functions associated with timers 1 and 2. In the input mode the EPA monitors an input pin for signal transitions and records the timer value when the event occurs. The "captured" event is thus tagged with its time. In the output mode the EPA waits until the timer matches a stored time value and then sets, clears or toggles an output pin. This is a "compare" event. Both capture and compare events initiate interrupts which can be handled by a normal service routine or the PTS. The 8XC196MC has 4 capture/compare modules and 4 compare-only modules.

The two 16-bit timers can be clocked by the internal clock generator or by external sources. An external "quadrature clocking" mode is available for monitoring speed and direction from a position encoder.

Pulse Width Modulation Unit—The 8XC196MC has a PWM module that provides two PWM outputs. This module is in addition to the waveform generator. The

duty cycle and the period of each output is programmable through a respective 8-bit register. The module has an 8-bit counter, two 8-bit PWM compare registers and an 8-bit period register. The PWM output pins are controlled with bits in the output control register of the waveform generator.

A/D Converter—The 13-channel A/D converter can perform 10-bit conversions or faster 8-bit conversions. Automated A/D conversions and result storage are facilitated by the A/D scan mode of the PTS. The sample-and-hold times and the conversion times are programmable. The A/D can also act as a programmable comparator and issue an interrupt when the input crosses a threshold. Conversions can be performed on the analog ground and reference voltage, and the results can be used to calculate gain and zero offset errors. The zero offset compensation circuit is also programmable, enabling automatic offset adjustment.

Interrupt Controller and Peripheral Transaction Server (PTS)—The 8XC196MC's flexible interrupt handling system has two main components: the programmable interrupt controller and the Peripheral Transaction Server (PTS). The interrupt controller has a hardware priority scheme that can be modified by user software. These interrupts are serviced by user-written interrupt service routines. The user can select most interrupts to be serviced by the PTS instead of the programmable interrupt controller. The PTS has several microcoded hardware interrupt service routines whose execution is interleaved with normal instruction execution. The result is high-speed, low-overhead interrupt handling. The PTS can perform single and burst transfers of bytes or 16-bit words between any memory locations, manage multiple analog-to-digital (A/D) conversions and control a software serial channel which allows either synchronous or asynchronous operations.

Waveform Generator—The Waveform Generator (WG) produces 3 pairs of complimentary PWM signals. This peripheral is optimized for controlling 3-phase induction AC motors. It can also control brushless DC motors and DC to AC inverters. A dead-time generator and phase inverter circuit provide non-overlapping on-timers for each PWM output pair. Each signal is independently programmable.

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August 1992

8X9X
Quick Reference

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Order Number: 272110-002

8X9X Quick Reference

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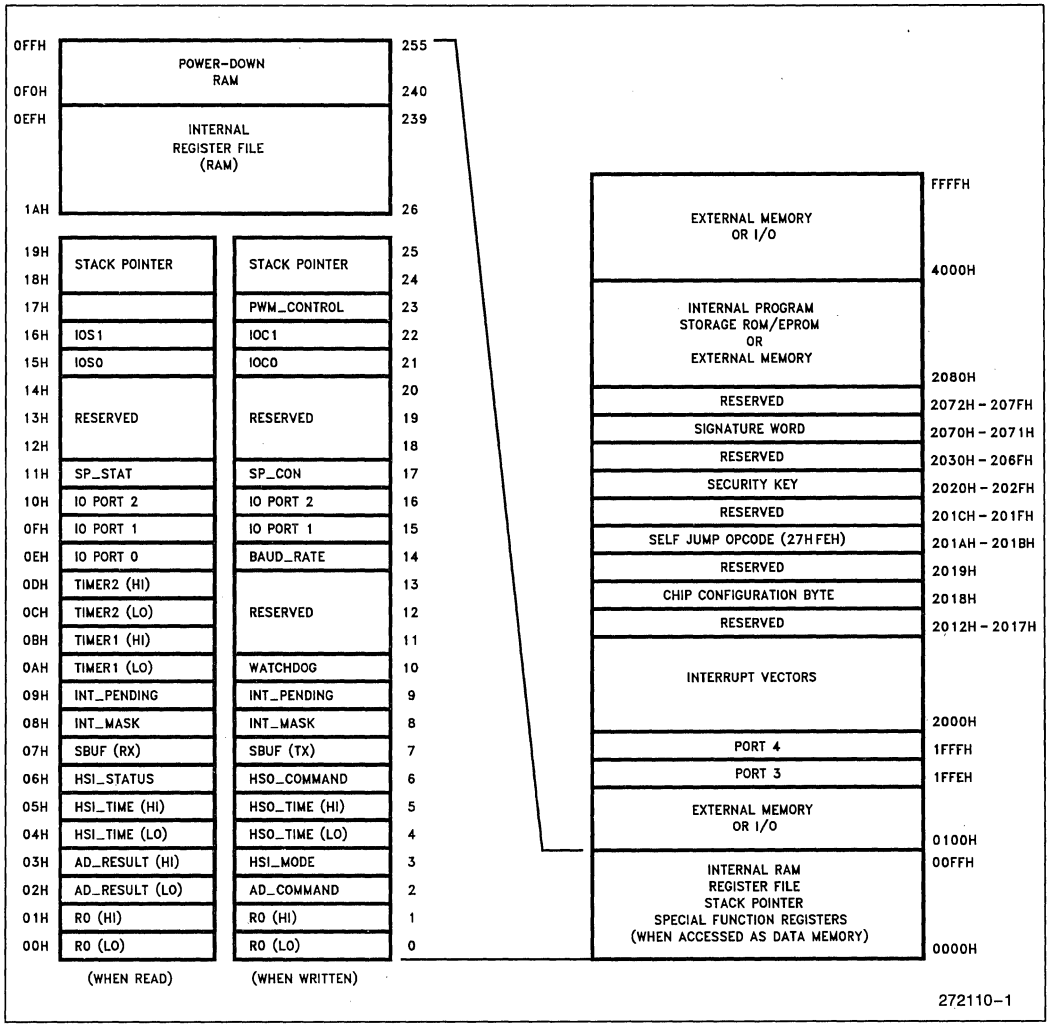
1.0 MEMORY AND SFR MAP



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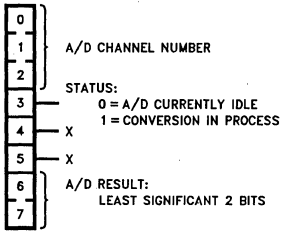
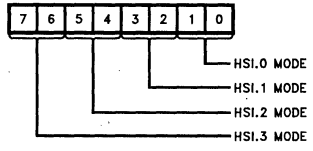
2.0 SFR BIT SUMMARY

A/D Result LO (02H)



272110-2

HSI_Mode (03H)

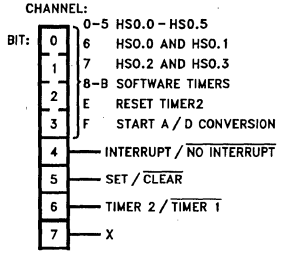


WHERE EACH 2 - BIT MODE CONTROL FIELD DEFINES ONE OF 4 POSSIBLE MODES:

00 8 POSITIVE TRANSITIONS
01 EACH POSITIVE TRANSITION
10 EACH NEGATIVE TRANSITION
11 EVERY TRANSITION (POSITIVE AND NEGATIVE)

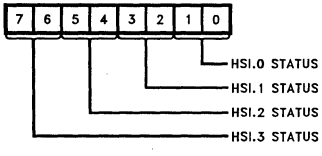
272110-3

HSO Command (06H)



272110-4

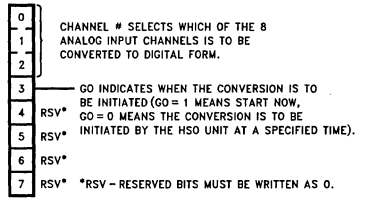
HSI_Status (06H)



WHERE FOR EACH 2 - BIT STATUS FIELD THE LOWER BIT INDICATES WHETHER OR NOT AN EVENT HAS OCCURRED ON THIS PIN AND THE UPPER BIT INDICATES THE CURRENT STATUS OF THE PIN.

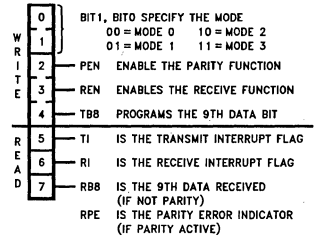
272110-5

A/D Command (02H)



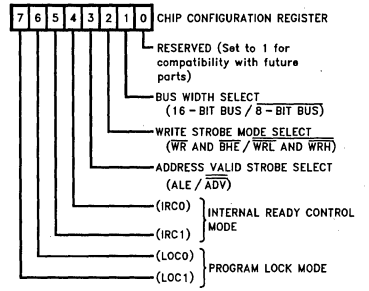
272110-6

SPCON/SPSTAT (11H)



272110-7

Chip Configuration



272110-8

Internal Ready Control

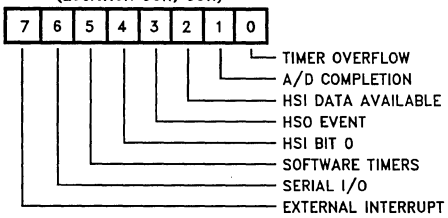
IRC1	IRC0	Description
0	0	Limit to 1 Wait State
0	1	Limit to 2 Wait States
1	0	Limit to 3 Wait States
1	1	Disable Internal Ready Control

Program Lock Modes

LOC1	LOC0	Protection
0	0	Read and Write Protected
0	1	Read Protected
1	0	Write Protected
1	1	No Protection

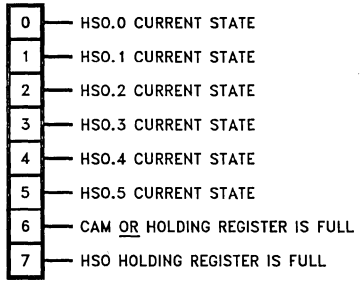
Interrupt Pending/Mask Register

(LOCATION 08H, 09H)



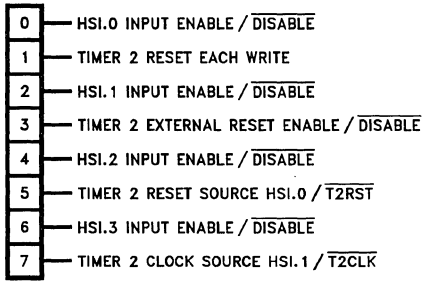
272110-9

IOS0 (15H)



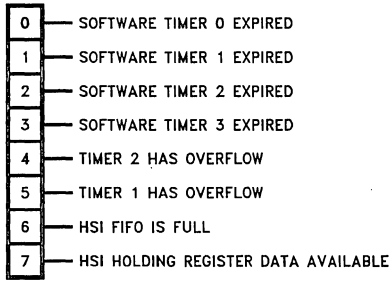
272110-12

IOC0 (15H)



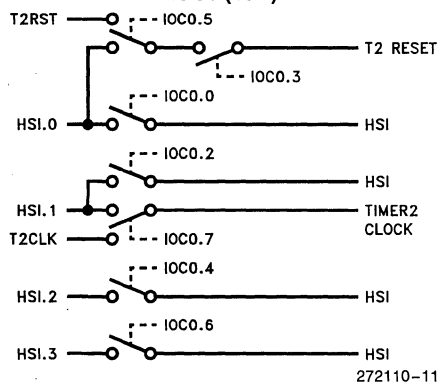
272110-10

IOS1 (16H)



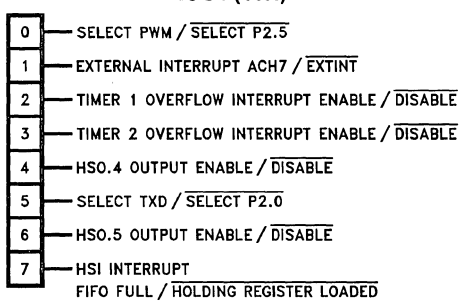
272110-13

IOC0 (15H)



272110-11

IOC1 (16H)



272110-14

PSW Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Z	N	V	VT	C	—	I	ST	<Interrupt Mask Reg>							

3.0 PIN DEFINITION TABLE

Pin Name	68L PLCC	68L PGA or LCC	64L SDIP	48L DIP
ACH0	6	4	4	
ACH1	5	5	3	
ACH2	7	3	5	
ACH3	4	6	2	
ACH4	11	67	9	43
ACH5	10	68	8	42
ACH6	8	2	6	40
ACH7	9	1	7	41
AD0	60	18	58	32
AD1	59	19	57	31
AD2	58	20	56	30
AD3	57	21	55	29
AD4	56	22	54	28
AD5	55	23	53	27
AD6	54	24	52	26
AD7	53	25	51	25
AD8	52	26	50	24
AD9	51	27	49	23
AD10	50	28	48	22
AD11	49	29	47	21
AD12	48	30	46	20
AD13	47	31	45	19
AD14	46	32	44	18
AD15	45	33	43	17
$\overline{ADV}$	62	16	60	34
ALE	62	16	60	34
ANGND	12	66	10	44
$\overline{BHE}$	41	37	39	15
BUSWIDTH	64	14		
CLKOUT	65	13		
$\overline{EA}$	2	8	1	39
EXTINT	15	63	13	47
HSI.0	24	54	22	3
HSI.1	25	53	23	4
HSI.2	26	52	24	5
HSI.3	27	51	25	6

Pin Name	68L PLCC	68L PGA or LCC	64L SDIP	48L DIP
HSO.0	28	50	26	7
HSO.1	29	49	27	8
HSO.2	34	44	32	9
HSO.3	35	43	33	10
HSO.4	26	52	24	5
HSO.5	27	51	25	6
INST	63	15		
NMI	3	7		
P0.0	6	4	4	
P0.1	5	5	3	
P0.2	7	3	5	
P0.3	4	6	2	
P0.4	11	67	9	43
P0.5	10	68	8	42
P0.6	8	2	6	40
P0.7	9	1	7	41
P1.0	19	59	17	
P1.1	20	58	18	
P1.2	21	57	19	
P1.3	22	56	20	
P1.4	23	55	21	
P1.5	30	48	28	
P1.6	31	47	29	
P1.7	32	46	30	
P2.0	18	60	16	2
P2.1	17	61	15	1
P2.2	15	63	13	47
P2.3	44	34	42	
P2.4	42	36	40	
P2.5	39	39	37	13
P2.6	33	45	31	
P2.7	38	40	36	
P3.0	60	18	58	32
P3.1	59	19	57	31
P3.2	58	20	56	30
P3.3	57	21	55	29

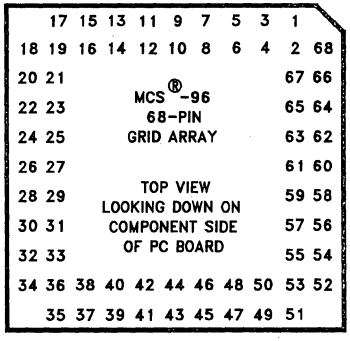
3.0 PIN DEFINITION TABLE (Continued)

Pin Name	68L PLCC	68L PGA or LCC	64L SDIP	48L DIP
P3.4	56	22	54	28
P3.5	55	23	53	27
P3.6	54	24	52	26
P3.7	53	25	51	25
P4.0	52	26	50	24
P4.1	51	27	49	23
P4.2	50	28	48	22
P4.3	49	29	47	21
P4.4	48	30	46	20
P4.5	47	31	45	19
P4.6	46	32	44	18
P4.7	45	33	43	17
PALE	17	61	15	1
$\overline{PDO}$	39	39	37	13
PMOD.0	11	67	9	43
PMOD.1	10	68	8	42
PMOD.2	8	2	6	40
PMOD.3	9	1	7	41
$\overline{PROG}$	15	63	13	47
PVER	18	60	16	2
PWM	39	39	37	13

Pin Name	68L PLCC	68L PGA or LCC	64L SDIP	48L DIP
$\overline{RD}$	61	17	59	33
READY	43	35	41	16
$\overline{RESET}$	16	62	14	48
RXD	17	61	15	1
SALE	18	60	16	2
$\overline{SPROG}$	39	39	37	13
T2CLK	44	34	42	
T2RST	42	36	40	
TXD	18	60	16	2
V_{CC}	1	9	64	38
V_{PD}	14	64	12	46
V_{PP}	37	41	35	12
V_{REF}	13	65	11	45
V_{SS1}	68	10	34	11
V_{SS2}	36	42	63	37
$\overline{WR}$	40	38	38	14
$\overline{WRL}$	40	38	38	14
$\overline{WRH}$	41	37	39	25
XTAL1	67	11	62	36
XTAL2	66	12	61	35

4.0 PACKAGE PIN ASSIGNMENT

Pins Facing Down

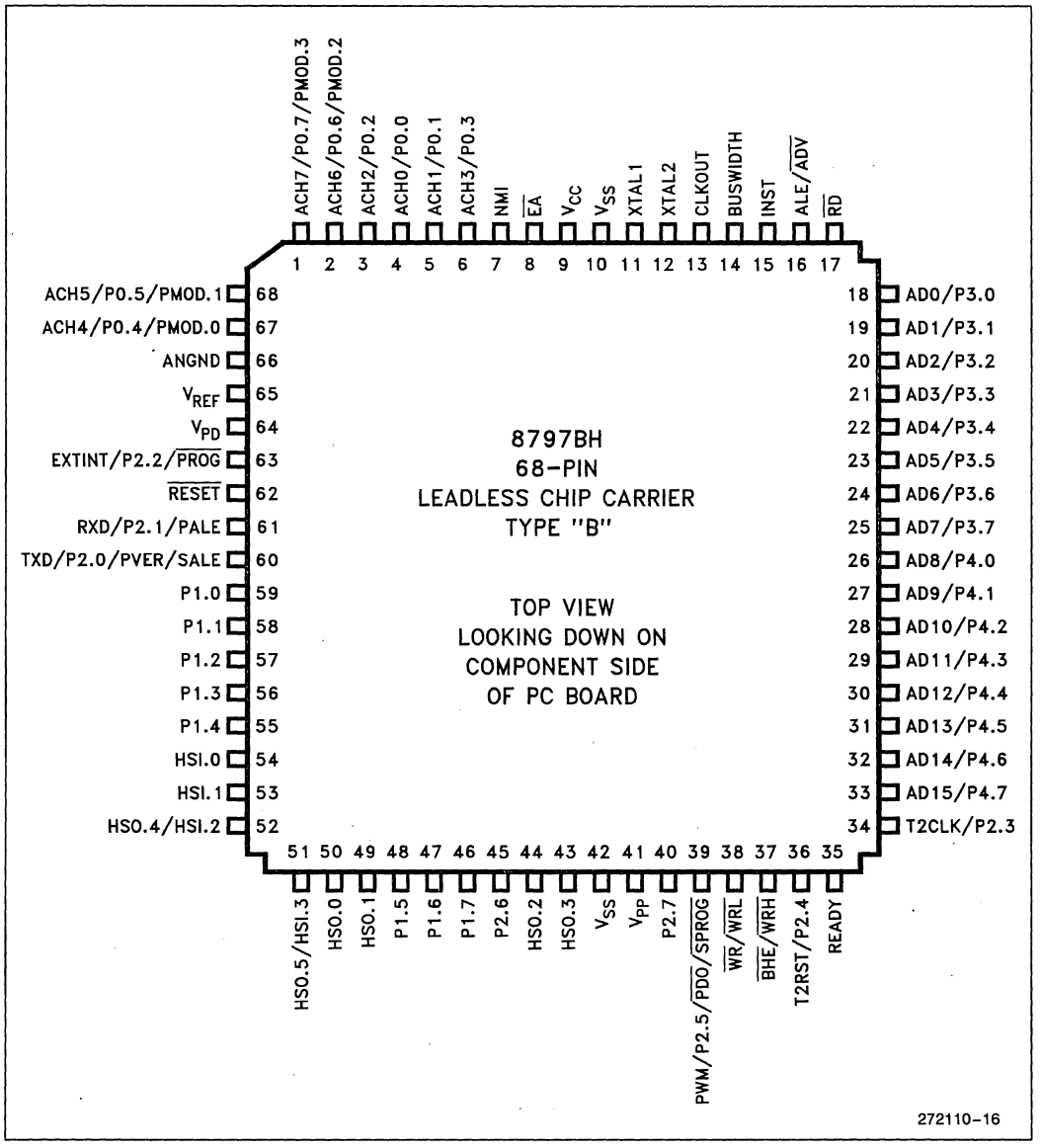


272110-15

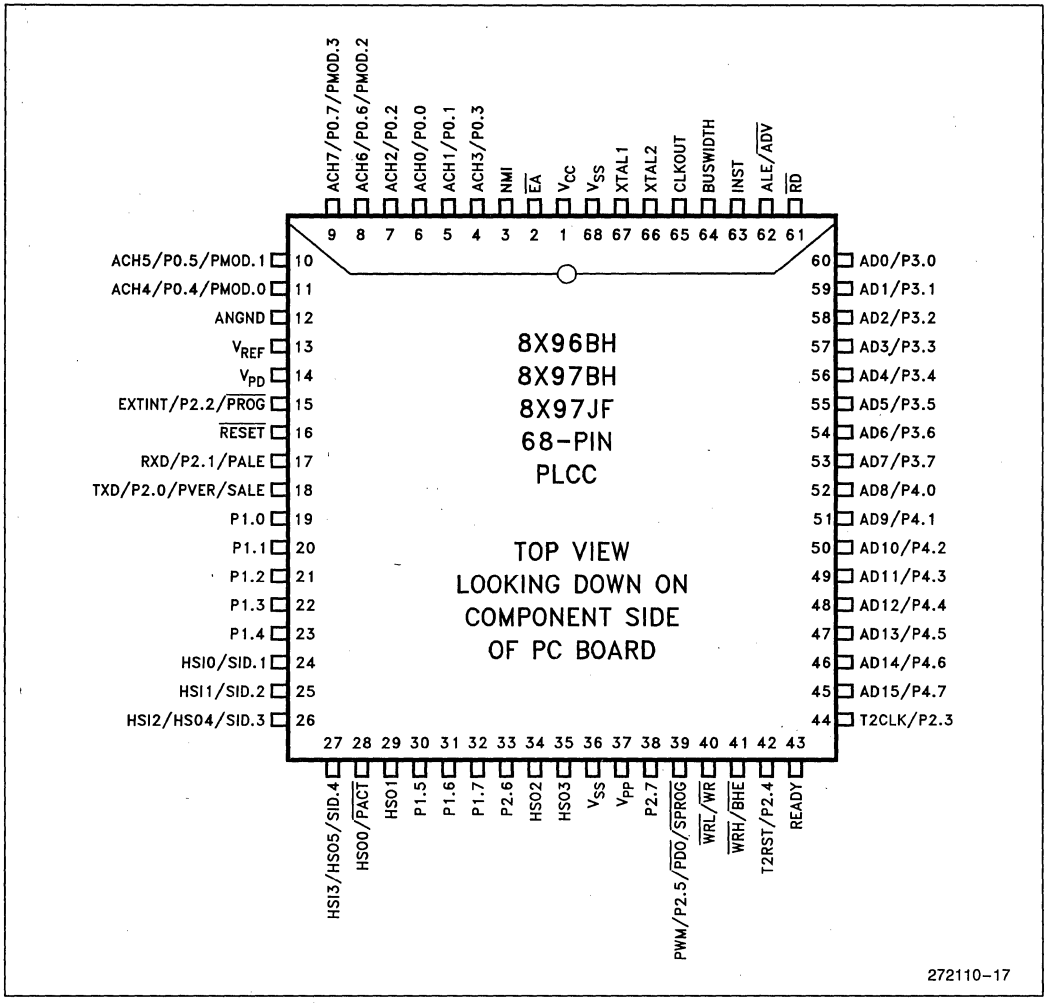
PGA	Description
1	ACH7/P0.7/PMOD.3
2	ACH6/P0.6/PMOD.2
3	ACH2/P0.2
4	ACH0/P0.0
5	ACH1/P0.1
6	ACH3/P0.3
7	NMI
8	$\overline{EA}$
9	V_{CC}
10	V_{SS}
11	XTAL1
12	XTAL2
13	CLKOUT
14	BUSWIDTH
15	INST
16	ALE/$\overline{ADV}$
17	$\overline{RD}$
18	AD0/P3.0
19	AD1/P3.1
20	AD2/P3.2
21	AD3/P3.3
22	AD4/P3.4
23	AD5/P3.5

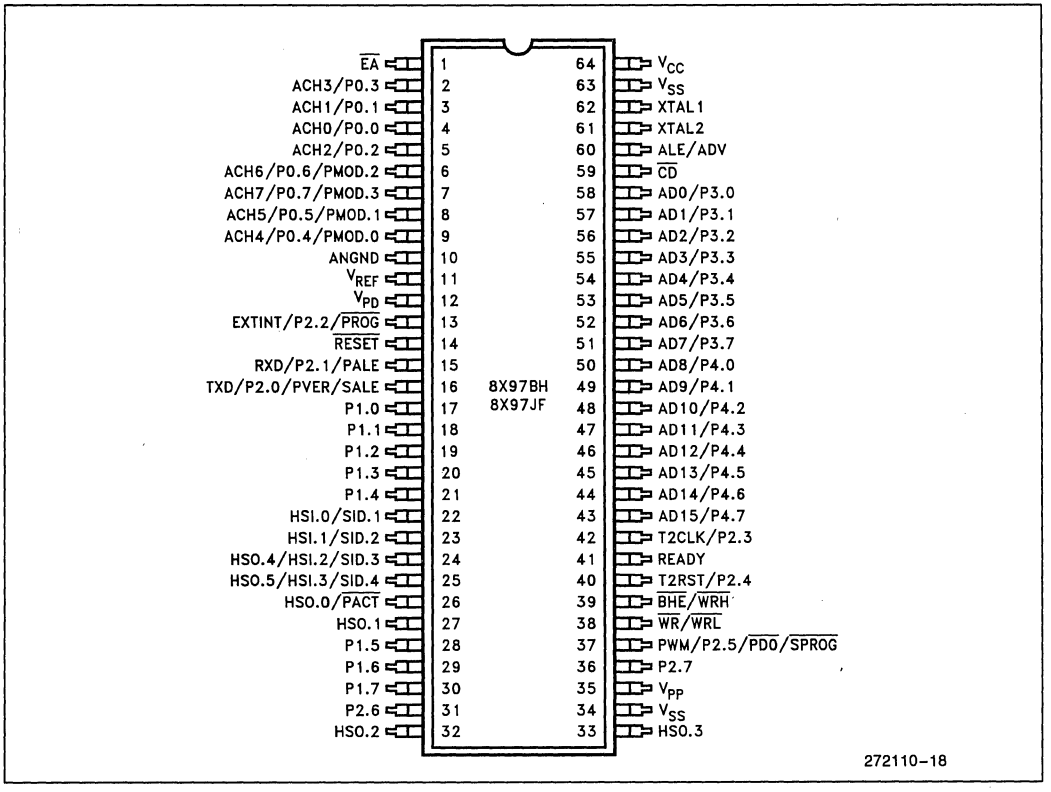
PGA	Description
24	AD6/P3.6
25	AD7/P3.7
26	AD8/P4.0
27	AD9/P4.1
28	AD10/P4.2
29	AD11/P4.3
30	AD12/P4.4
31	AD13/P4.5
32	AD14/P4.6
33	AD15/P4.7
34	T2CLK/P2.3
35	READY
36	T2RST/P2.4
37	$\overline{BHE}$/$\overline{WRH}$
38	$\overline{WR}$/$\overline{WRL}$
39	PWM/P2.5/$\overline{PDO}$/$\overline{SPROG}$
40	P2.7
41	V_{PP}
42	V_{SS}
43	HSO.3
44	HSO.2
45	P2.6
46	P1.7

PGA	Description
47	P1.6
48	P1.5
49	HSO.1
50	HSO.0
51	HSO.5/HSI.3
52	HSO.4/HSI.2
53	HSI.1
54	HSI.0
55	P1.4
56	P1.3
57	P1.2
58	P1.1
59	P1.0
60	TXD/P2.0/PVER/SALE
61	RXD/P2.1/PALE
62	$\overline{RESET}$
63	EXTINT/P2.2/$\overline{PROG}$
64	V_{PD}
65	V_{REF}
66	ANGND
67	ACH4/P0.4/PMOD.0
68	ACH5/P0.5/PMOD.1


ACH7/P0.7/PMOD.3
ACH6/P0.6/PMOD.2
ACH2/P0.2
ACH0/P0.0
ACH1/P0.1
ACH3/P0.3
NMI
EA
VCC
VSS
XTAL1
XTAL2
CLKOUT
BUSWIDTH
INST
ALE/ADV
RD
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
ACH5/P0.5/PMOD.1 68
ACH4/P0.4/PMOD.0 67
ANGND 66
VREF 65
VPD 64
EXTINT/P2.2/PROG 63
RESET 62
RXD/P2.1/PALE 61
TXD/P2.0/PVER/SALE 60
P1.0 59
P1.1 58
P1.2 57
P1.3 56
P1.4 55
HSI.0 54
HSI.1 53
HSO.4/HSI.2 52
18 AD0/P3.0
19 AD1/P3.1
20 AD2/P3.2
21 AD3/P3.3
22 AD4/P3.4
23 AD5/P3.5
24 AD6/P3.6
25 AD7/P3.7
26 AD8/P4.0
27 AD9/P4.1
28 AD10/P4.2
29 AD11/P4.3
30 AD12/P4.4
31 AD13/P4.5
32 AD14/P4.6
33 AD15/P4.7
34 T2CLK/P2.3
8797BH
68-PIN
LEADLESS CHIP CARRIER
TYPE "B"
TOP VIEW
LOOKING DOWN ON
COMPONENT SIDE
OF PC BOARD
51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35
HSO.5/HSI.3
HSO.0
HSO.1
P1.5
P1.6
P1.7
P2.6
HSO.2
HSO.3
VSS
VPP
P2.7
PWM/P2.5/PDO/SPROG
WR/WRL
BHE/WRH
T2RST/P2.4
READY
272110-16

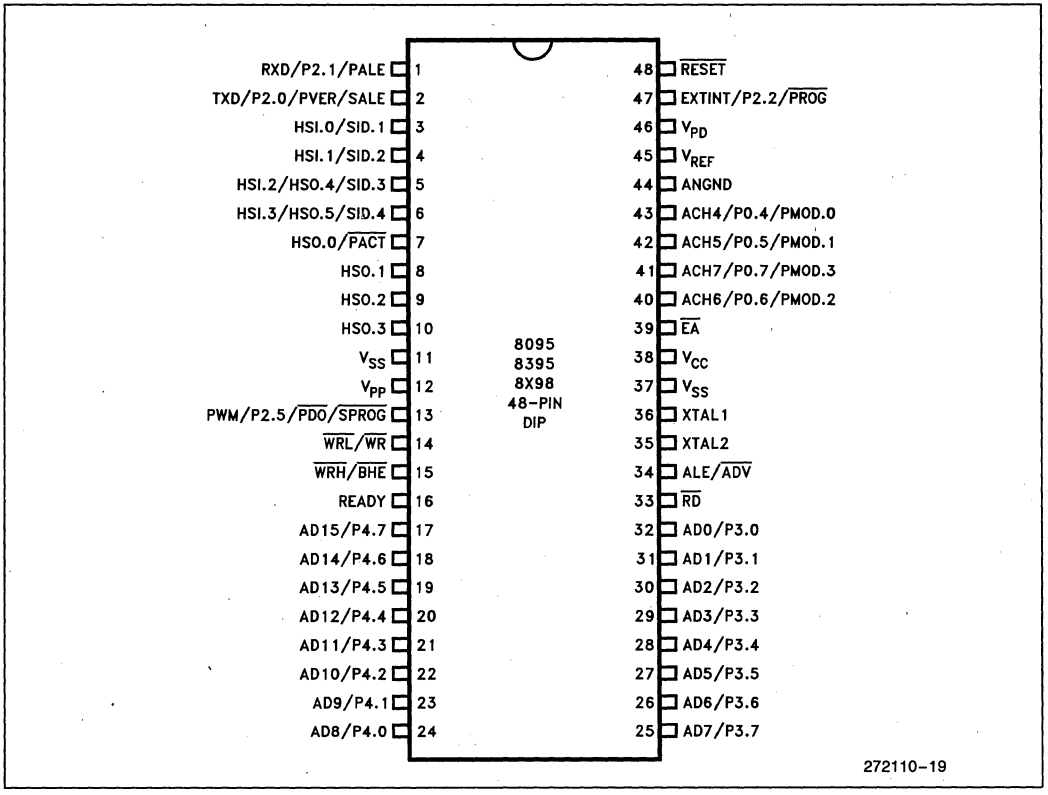
14


ACH7/P0.7/PMOD.3
ACH6/P0.6/PMOD.2
ACH2/P0.2
ACH0/P0.0
ACH1/P0.1
ACH3/P0.3
NMI
EA
VCC
VSS
XTAL1
XTAL2
CLKOUT
BUSWIDTH
INST
ALE/ADV
RD
9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61
ACH5/P0.5/PMOD.1 10
ACH4/P0.4/PMOD.0 11
ANGND 12
VREF 13
VPD 14
EXTINT/P2.2/PROG 15
RESET 16
RXD/P2.1/PALE 17
TXD/P2.0/PVER/SALE 18
P1.0 19
P1.1 20
P1.2 21
P1.3 22
P1.4 23
HSI0/SID.1 24
HSI1/SID.2 25
HSI2/HS04/SID.3 26
60 AD0/P3.0
59 AD1/P3.1
58 AD2/P3.2
57 AD3/P3.3
56 AD4/P3.4
55 AD5/P3.5
54 AD6/P3.6
53 AD7/P3.7
52 AD8/P4.0
51 AD9/P4.1
50 AD10/P4.2
49 AD11/P4.3
48 AD12/P4.4
47 AD13/P4.5
46 AD14/P4.6
45 AD15/P4.7
44 T2CLK/P2.3
8X96BH
8X97BH
8X97JF
68-PIN
PLCC
TOP VIEW
LOOKING DOWN ON
COMPONENT SIDE
OF PC BOARD
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
HSI3/HS05/SID.4
HS00/PACT
HS01
P1.5
P1.6
P1.7
P2.6
HS02
HS03
VSS
VPP
P2.7
PWM/P2.5/PDO/SPROG
WRL/WR
WRH/BHE
T2RST/P2.4
READY
272110-17



Shrink-DIP Package

14


RXD/P2.1/PALE 1
TXD/P2.0/PVER/SALE 2
HSI.0/SID.1 3
HSI.1/SID.2 4
HSI.2/HSO.4/SID.3 5
HSI.3/HSO.5/SID.4 6
HSO.0/PACT 7
HSO.1 8
HSO.2 9
HSO.3 10
VSS 11
VPP 12
PWM/P2.5/PDO/SPROG 13
WRL/WR 14
WRH/BHE 15
READY 16
AD15/P4.7 17
AD14/P4.6 18
AD13/P4.5 19
AD12/P4.4 20
AD11/P4.3 21
AD10/P4.2 22
AD9/P4.1 23
AD8/P4.0 24
8095
8395
8X98
48-PIN
DIP
48 RESET
47 EXTINT/P2.2/PROG
46 VPD
45 VREF
44 ANGND
43 ACH4/P0.4/PMOD.0
42 ACH5/P0.5/PMOD.1
41 ACH7/P0.7/PMOD.3
40 ACH6/P0.6/PMOD.2
39 EA
38 VCC
37 VSS
36 XTAL1
35 XTAL2
34 ALE/ADV
33 RD
32 AD0/P3.0
31 AD1/P3.1
30 AD2/P3.2
29 AD3/P3.3
28 AD4/P3.4
27 AD5/P3.5
26 AD6/P3.6
25 AD7/P3.7
272110-19

5.0 PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which must be connected.
V_{PD}	RAM standby supply voltage (5V). This voltage must be present during normal operation. In a Power Down condition (i.e., V_{CC} drops to zero), if $\overline{RESET}$ is activated before V_{CC} drops below spec and V_{PD} continues to be held within spec., the top 16 bytes in the Register File will retain their contents.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected to use A/D or Port 0.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the EPROM devices. It should be +12.75V for programming and will float to 5V otherwise. The pin should not be above V_{CC} for ROM and CPU devices. This pin must be left floating in the application circuit for EPROM devices.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT*†	Output of the internal clock generator. The frequency of CLKOUT is 1/3 the oscillator frequency. It has a 33% duty cycle.
$\overline{RESET}$	Reset input to the chip. Input low for a minimum 10 XTAL1 cycles to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
BUSWIDTH*†	Input for bus width selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. If this pin is left unconnected, it will rise to V_{CC}.
NMI*†	A positive transition causes a vector to external memory location 0000H.
INST*†	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ = +12.75V causes execution to begin in the Programming Mode.
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is activated only during external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.

5.0 PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available in the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0‡	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1†	8-bit quasi-bidirectional I/O port.
Port 2†	8-bit multi-functional port. Six of its pins are shared with other functions in the 8096BH, the remaining 2 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus. Ports 3 and 4 are also used as a command, address and data path by EPROM devices operating in the Programming Mode.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming Mode indicates that programming is in progress. A high signal indicates programming is complete.
PVAL	A low signal in Auto Programming Mode indicates that the device was programmed correctly.
SALE	A falling edge of Auto Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (output from master).
$\overline{\text{SPROG}}$	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming data (output from master).
SID	Assigns a pin of Ports 3 and 4 to each slave to pass programming verification.
PALE	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that Ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
PVAL	A high signal in Slave Programming Mode indicates the device was programmed correctly.
$\overline{\text{PDO}}$	A low signal in Slave Programming Mode indicates that the PROG pulse was applied for longer than allowed.

*Not available on Shrink-DIP package.
†Not available on 48-pin device.
‡Port 0.0.1.2.3 not available on 48-pin device.

6.0 OPCODE TABLE

Opcode	Instruction
00	SKIP
01	CLR
02	NOT
03	NEG
04	XCH
05	DEC
06	EXT
07	INC
08	SHR
09	SHL
0A	SHRA
0B	RESERVED**
0C	SHRL
0D	SHLL
0E	SHRAL
0F	NORML
10	RESERVED**
11	CLRB
12	NOTB
13	NEGB
14	XCHB
15	DECB
16	EXTB
17	INCB
18	SHRB
19	SHLB
1A	SHRAB
1B	RESERVED**
1C	RESERVED**
1D	RESERVED**
1E	RESERVED**
1F	RESERVED**
20	SJMP
21	SJMP
22	SJMP
23	SJMP
24	SJMP
25	SJMP
26	SJMP
27	SJMP
28	SCALL
29	SCALL
2A	SCALL
2B	SCALL
2C	SCALL
2D	SCALL
2E	SCALL
2F	SCALL
30	JBC
31	JBC
32	JBC
33	JBC

Opcode	Instruction
34	JBC
35	JBC
36	JBC
37	JBC
38	JBS
39	JBS
3A	JBS
3B	JBS
3C	JBS
3D	JBS
3E	JBS
3F	JBS
40	AND DIRECT (3 OPS)
41	AND IMMEDIATE (3 OPS)
42	AND INDIRECT (3 OPS)
43	AND INDEXED (3 OPS)
44	ADD DIRECT (3 OPS)
45	ADD IMMEDIATE (3 OPS)
46	ADD INDIRECT (3 OPS)
47	ADD INDEXED (3 OPS)
48	SUB DIRECT (3 OPS)
49	SUB IMMEDIATE (3 OPS)
4A	SUB INDIRECT (3 OPS)
4B	SUB INDEXED (3 OPS)
4C	MULU DIRECT (3 OPS)
4D	MULU IMMEDIATE (3 OPS)
4E	MULU INDIRECT (3 OPS)
4F	MULU INDEXED (3 OPS)
50	ANDB DIRECT (3 OPS)
51	ANDB IMMEDIATE (3 OPS)
52	ANDB INDIRECT (3 OPS)
53	ANDB INDEXED (3 OPS)
54	ADDB DIRECT (3 OPS)
55	ADDB IMMEDIATE (3 OPS)
56	ADDB INDIRECT (3 OPS)
57	ADDB INDEXED (3 OPS)
58	SUBB DIRECT (3 OPS)
59	SUBB IMMEDIATE (3 OPS)
5A	SUBB INDIRECT (3 OPS)
5B	SUBB INDEXED (3 OPS)
5C	MULUB DIRECT (3 OPS)
5D	MULUB IMMEDIATE (3 OPS)
5E	MULUB INDIRECT (3 OPS)
5F	MULUB INDEXED (3 OPS)
60	AND DIRECT (2 OPS)
61	AND IMMEDIATE (2 OPS)
62	AND INDIRECT (2 OPS)
63	AND INDEXED (2 OPS)
64	ADD DIRECT (2 OPS)
65	ADD IMMEDIATE (2 OPS)
66	ADD INDIRECT (2 OPS)
67	ADD INDEXED (2 OPS)

6.0 OPCODE TABLE (Continued)

Opcode	Instruction
68	SUB DIRECT (2 OPS)
69	SUB IMMEDIATE (2 OPS)
6A	SUB INDIRECT (2 OPS)
6B	SUB INDEXED (2 OPS)
6C	MULU DIRECT (2 OPS)
6D	MULU IMMEDIATE (2 OPS)
6E	MULU INDIRECT (2 OPS)
6F	MULU INDEXED (2 OPS)
70	ANDB DIRECT (2 OPS)
71	ANDB IMMEDIATE (2 OPS)
72	ANDB INDIRECT (2 OPS)
73	ANDB INDEXED (2 OPS)
74	ADDB DIRECT (2 OPS)
75	ADDB IMMEDIATE (2 OPS)
76	ADDB INDIRECT (2 OPS)
77	ADDB INDEXED (2 OPS)
78	SUBB DIRECT (2 OPS)
79	SUBB IMMEDIATE (2 OPS)
7A	SUBB INDIRECT (2 OPS)
7B	SUBB INDEXED (2 OPS)
7C	MULUB DIRECT (2 OPS)
7D	MULUB IMMEDIATE (2 OPS)
7E	MULUB INDIRECT (2 OPS)
7F	MULUB INDEXED (2 OPS)
80	OR DIRECT
81	OR IMMEDIATE
82	OR INDIRECT
83	OR INDEXED
84	XOR DIRECT
85	XOR IMMEDIATE
86	XOR INDIRECT
87	XOR INDEXED
88	CMP DIRECT
89	CMP IMMEDIATE
8A	CMP INDIRECT
8B	CMP INDEXED
8C	DIVU DIRECT
8D	DIVU IMMEDIATE
8E	DIVU INDIRECT
8F	DIVU INDEXED
90	ORB DIRECT
91	ORB IMMEDIATE
92	ORB INDIRECT
93	ORB INDEXED
94	XORB DIRECT
95	XORB IMMEDIATE
96	XORB INDIRECT
97	XORB INDEXED
98	CMPB DIRECT
99	CMPB IMMEDIATE
9A	CMPB INDIRECT
9B	CMPB INDEXED

Opcode	Instruction
9C	DIVUB DIRECT
9D	DIVUB IMMEDIATE
9E	DIVUB INDIRECT
9F	DIVUB INDEXED
A0	LD DIRECT
A1	LD IMMEDIATE
A2	LD INDIRECT
A3	LD INDEXED
A4	ADDC DIRECT
A5	ADDC IMMEDIATE
A6	ADDC INDIRECT
A7	ADDC INDEXED
A8	SUBC DIRECT
A9	SUBC IMMEDIATE
AA	SUBC INDIRECT
AB	SUBC INDEXED
AC	LDBZE DIRECT
AD	LDBZE IMMEDIATE
AE	LDBZE INDIRECT
AF	LDBZE INDEXED
B0	LDB DIRECT
B1	LDB IMMEDIATE
B2	LDB INDIRECT
B3	LDB INDEXED
B4	ADDCB DIRECT
B5	ADDCB IMMEDIATE
B6	ADDCB INDIRECT
B7	ADDCB INDEXED
B8	SUBCB DIRECT
B9	SUBCB IMMEDIATE
BA	SUBCB INDIRECT
BB	SUBCB INDEXED
BC	LDBSE DIRECT
BD	LDBSE IMMEDIATE
BE	LDBSE INDIRECT
BF	LDBSE INDEXED
C0	ST DIRECT
C1	RESERVED**
C2	ST INDIRECT
C3	ST INDEXED
C4	STB DIRECT
C5	RESERVED**
C6	STB INDIRECT
C7	STB INDEXED
C8	PUSH DIRECT
C9	PUSH IMMEDIATE
CA	PUSH INDIRECT
CB	PUSH INDEXED
CC	POP DIRECT
CD	RESERVED**
CE	POP INDIRECT
CF	POP INDEXED

6.0 OPCODE TABLE (Continued)

Opcode	Instruction
D0	JNST
D1	JNH
D2	JGT
D3	JNC
D4	JNVT
D5	JNV
D6	JGE
D7	JNE
D8	JST
D9	JH
DA	JLE
DB	JC
DC	JVT
DD	JV
DE	JLT
DF	JE
E0	DJNZ
E1	RESERVED**
E2	RESERVED**
E3	BR (INDIRECT)
E4	RESERVED**
E5	RESERVED**
E6	RESERVED**
E7	LJMP

Opcode	Instruction
E8	RESERVED**
E9	RESERVED**
EA	RESERVED**
EB	RESERVED**
EC	RESERVED**
ED	RESERVED**
EE	RESERVED**
EF	LCALL
F0	RET
F1	RESERVED**
F2	PUSHF
F3	POPF
F4	RESERVED**
F5	RESERVED**
F6	RESERVED**
F7	TRAP
F8	CLRC
F9	SETC
FA	DI
FB	EI
FC	CLRVT
FD	NOP
FE	*DIV/DIVB/MUL/MULB
FF	RST

*Two Byte Instruction
**Opcodes which do not have a corresponding instruction will not generate an interrupt if executed.

7.0 INSTRUCTION SUMMARY

Mnemonic	Oper-ands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D ← D + A	↕	↕	↕	↕	↑	—	
ADD/ADDB	3	D ← B + A	↕	↕	↕	↕	↑	—	
ADDC/ADDCB	2	D ← D + A + C	↓	↕	↕	↕	↑	—	
SUB/SUBB	2	D ← D − A	↕	↕	↕	↕	↑	—	
SUB/SUBB	3	D ← B − A	↕	↕	↕	↕	↑	—	
SUBC/SUBCB	2	D ← D − A + C − 1	↓	↕	↕	↕	↑	—	
CMP/CMPB	2	D − A	↕	↕	↕	↕	↑	—	
MUL/MULU	2	D, D + 2 ← D * A	—	—	—	—	—	?	2
MUL/MULU	3	D, D + 2 ← B * A	—	—	—	—	—	?	2
MULB/MULUB	2	D, D + 1 ← D * A	—	—	—	—	—	?	3
MULB/MULUB	3	D, D + 1 ← B * A	—	—	—	—	—	?	3
DIVU	2	D ← (D, D + 2)/A, D + 2 ← remainder	—	—	—	↕	↑	—	2
DIVUB	2	D ← (D, D + 1)/A, D + 1 ← remainder	—	—	—	↕	↑	—	3
DIV	2	D ← (D, D + 2)/A, D + 2 ← remainder	—	—	—	?	↑	—	
DIVB	2	D ← (D, D + 1)/A, D + 1 ← remainder	—	—	—	?	↑	—	
AND/ANDB	2	D ← D and A	↕	↕	0	0	—	—	
AND/ANDB	3	D ← B and A	↕	↕	0	0	—	—	
OR/ORB	2	D ← D or A	↕	↕	0	0	—	—	
XOR/XORB	2	D ← D (excl. or) A	↕	↕	0	0	—	—	
LD/LDB	2	D ← A	—	—	—	—	—	—	
ST/STB	2	A ← D	—	—	—	—	—	—	
LDBSE	2	D ← A; D + 1 ← SIGN(A)	—	—	—	—	—	—	3, 4
LDBZE	2	D ← A; D + 1 ← 0	—	—	—	—	—	—	3, 4
PUSH	1	SP ← SP − 2; (SP) ← A	—	—	—	—	—	—	
POP	1	A ← (SP); SP ← SP + 2	—	—	—	—	—	—	
PUSHF	0	SP ← SP − 2; (SP) ← PSW; PSW ← 0000H I ← 0	0	0	0	0	0	0	
POPF	0	PSW ← (SP); SP ← SP + 2; I ← ↕	↕	↕	↕	↕	↕	↕	
SJMP	1	PC ← PC + 11-bit offset	—	—	—	—	—	—	5
LJMP	1	PC ← PC + 16-bit offset	—	—	—	—	—	—	5
BR [indirect]	1	PC ← (A)	—	—	—	—	—	—	
SCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 11-bit offset	—	—	—	—	—	—	5
LCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 16-bit offset	—	—	—	—	—	—	5
RET	0	PC ← (SP); SP ← SP + 2	—	—	—	—	—	—	

7.0 INSTRUCTION SUMMARY (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
J (conditional)	1	PC ← PC + 8-bit offset (if taken)	—	—	—	—	—	—	5
JC	1	Jump if C = 1	—	—	—	—	—	—	5
JNC	1	Jump if C = 0	—	—	—	—	—	—	5
JE	1	Jump if Z = 1	—	—	—	—	—	—	5
JNE	1	Jump if Z = 0	—	—	—	—	—	—	5
JGE	1	Jump if N = 0	—	—	—	—	—	—	5
JLT	1	Jump if N = 1	—	—	—	—	—	—	5
JGT	1	Jump if N = 0 and Z = 0	—	—	—	—	—	—	5
JLE	1	Jump if N = 1 or Z = 1	—	—	—	—	—	—	5
JH	1	Jump if C = 1 and Z = 0	—	—	—	—	—	—	5
JNH	1	Jump if C = 0 or Z = 1	—	—	—	—	—	—	5
JV	1	Jump if V = 1	—	—	—	—	—	—	5
JNV	1	Jump if V = 0	—	—	—	—	—	—	5
JVT	1	Jump if VT = 1; Clear VT	—	—	—	—	0	—	5
JNVT	1	Jump if VT = 0; Clear VT	—	—	—	—	0	—	5
JST	1	Jump if ST = 1	—	—	—	—	—	—	5
JNST	1	Jump if ST = 0	—	—	—	—	—	—	5
JBS	3	Jump if Specified Bit = 1	—	—	—	—	—	—	5, 6
JBC	3	Jump if Specified Bit = 0	—	—	—	—	—	—	5, 6
DJNZ	1	D ← D − 1; if D ≠ 0 then PC ← PC + 8-bit offset	—	—	—	—	—	—	5
DEC/DECB	1	D ← D − 1	↙	↙	↙	↙	↑	—	
NEG/NEGB	1	D ← 0 − D	↙	↙	↙	↙	↑	—	
INC/INCB	1	D ← D + 1	↙	↙	↙	↙	↑	—	
EXT	1	D ← D; D + 2 ← Sign (D)	↙	↙	0	0	—	—	2
EXTB	1	D ← D; D + 1 ← Sign (D)	↙	↙	0	0	—	—	3
NOT/NOTB	1	D ← Logical Not (D)	↙	↙	0	0	—	—	
CLR/CLRB	1	D ← 0	1	0	0	0	—	—	
SHL/SHLB/SHLL	2	C ← msb — — — — — — lsb ← 0	↙	?	↙	↙	↑	—	7
SHR/SHRB/SHRL	2	0 → msb — — — — — — lsb → C	↙	?	↙	0	—	↙	7
SHRA/SHRAB/SHRAL	2	msb → msb — — — — — — lsb → C	↙	↙	↙	0	—	↙	7
SETC	0	C ← 1	—	—	1	—	—	—	
CLRC	0	C ← 0	—	—	0	—	—	—	
CLRVT	0	VT ← 0	—	—	—	—	0	—	

7.0 INSTRUCTION SUMMARY (Continued)

Mnemonic	Oper-ands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
RST	0	PC ← 2080H	0	0	0	0	0	0	8
DI	0	Disable All Interrupts (I ← 0)	—	—	—	—	—	—	
EI	0	Enable All Interrupts (I ← 1)	—	—	—	—	—	—	
NOP	0	PC ← PC + 1	—	—	—	—	—	—	
SKIP	0	PC ← PC + 2	—	—	—	—	—	—	
NORML	2	Left shift till msb = 1; D ← shift count	✓	?	0	—	—	—	7
TRAP	0	SP ← SP − 2; (SP) ← PC PC ← (2010H)	—	—	—	—	—	—	9

NOTES:
1. If the mnemonic ends in "B", a byte operation is performed, otherwise a word operation is done. Operands D, B and A must conform to the alignment rules for the required operand type. D and B are locations in the Register File; A can be located anywhere in memory.
2. D, D + 2 are consecutive WORDS in memory; D is DOUBLE-WORD aligned.
3. D, D + 1 are consecutive BYTES in memory; D is WORD aligned.
4. Changes a byte to a word.
5. Offset is a 2's complement number.
6. Specified bit is one of the 2048 bits in the register file.
7. The "L" (Long) suffix indicates double-word operation.
8. Initiates a Reset by pulling $\overline{\text{RESET}}$ low. Software should re-initialize all the necessary registers with code starting at 2080H.
9. The assembler will not accept this mnemonic.

8.0 OPCODES, INSTRUCTION LENGTH AND STATE TIMES

MNEMONIC	OPERANDS	DIRECT			IMMEDIATE			INDIRECT⊙ NORMAL			INDIRECT⊙ AUTO-INC.		INDEXED⊙ SHORT			INDEXED⊙ LONG	
		OPCODE	BYTES	STATE TIMES	OPCODE	BYTES	STATE TIMES	OPCODE	BYTES	STATE① TIMES	BYTES	STATE① TIMES	OPCODE	BYTES	STATE① TIMES⑧	BYTES	STATE① TIMES⑧
ARITHMETIC INSTRUCTIONS																	
ADD	2	64	3	4	65	4	5	66	3	6/11	3	7/12	67	4	6/11	5	7/12
ADD	3	44	4	5	45	5	6	46	4	7/12	4	8/13	47	5	7/12	6	8/13
ADDB	2	74	3	4	75	3	4	76	3	6/11	3	7/12	77	4	6/11	5	7/12
ADDB	3	54	4	5	55	4	5	56	4	7/12	4	8/13	57	5	7/12	6	8/13
ADDC	2	A4	3	4	A5	4	5	A6	3	6/11	3	7/12	A7	4	6/11	5	7/12
ADDCB	2	B4	3	4	B5	3	4	B6	3	6/11	3	7/12	B7	4	6/11	5	7/12
SUB	2	68	3	4	69	4	5	6A	3	6/11	3	7/12	6B	4	6/11	5	7/12
SUB	3	48	4	5	49	5	6	4A	4	7/12	4	8/13	4B	5	7/12	6	8/13
SUBB	2	78	3	4	79	3	4	7A	3	6/11	3	7/12	7B	4	6/11	5	7/12
SUBB	3	58	4	5	59	4	5	5A	4	7/12	4	8/13	5B	5	7/12	6	8/13
SUBC	2	A8	3	4	A9	4	5	AA	3	6/11	3	7/12	AB	4	6/11	5	7/12
SUBCB	2	B8	3	4	B9	3	4	BA	3	6/11	3	7/12	BB	4	6/11	5	7/12
CMP	2	88	3	4	89	4	5	8A	3	6/11	3	7/12	8B	4	6/11	5	7/12
CMPB	2	98	3	4	99	3	4	9A	3	6/11	3	7/12	9B	4	6/11	5	7/12
MULU	2	6C	3	25	6D	4	26	6E	3	27/32	3	28/33	6F	4	27/32	5	28/33
MULU	3	4C	4	26	4D	5	27	4E	4	28/33	4	29/34	4F	5	28/33	6	29/34
MULUB	2	7C	3	17	7D	3	17	7E	3	19/24	3	20/25	7F	4	19/24	5	20/25
MULUB	3	5C	4	18	5D	4	18	5E	4	20/25	4	21/26	5F	5	20/25	6	21/26
MUL	2	②	4	29	②	5	30	②	4	31/36	4	32/37	②	5	31/36	6	32/37
MUL	3	②	5	30	②	6	31	②	5	32/37	5	33/38	②	6	32/37	7	33/38
MULB	2	②	4	21	②	4	21	②	4	23/28	4	24/29	②	5	23/28	6	24/29
MULB	3	②	5	22	②	5	22	②	5	24/29	5	25/30	②	6	24/29	7	25/30
DIVU	2	8C	3	25	8D	4	26	8E	3	28/32	3	29/33	8F	4	28/32	5	29/33
DIVUB	2	9C	3	17	9D	3	17	9E	3	20/24	3	21/25	9F	4	20/24	5	21/25
DIV	2	②	4	29	②	5	30	②	4	32/36	4	33/37	②	5	32/36	6	33/37
DIVB	2	②	4	21	②	4	21	②	4	24/28	4	25/29	②	5	24/28	6	25/29

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NOTES:

*Long indexed and Indirect + instructions have identical opcodes with Short indexed and Indirect modes, respectively. The second byte of instructions using any Indirect or indexed addressing mode specifies the exact mode used. If the second byte is even, use Indirect or Short indexed. If it is odd, use Indirect + or Long indexed. In all cases the second byte of the instruction always specifies an even (word) location for the address referenced.

① Number of state times shown for internal/external operands.

② The opcodes for signed multiply and divide are the opcodes for the unsigned functions with an "FE" appended as a prefix.

⑧ State times shown for 16-bit bus.

8.0 OPCODES, INSTRUCTION LENGTH AND STATE TIMES (Continued)

MNEMONIC	OPERANDS	DIRECT			IMMEDIATE			INDIRECT⑥					INDEXED⑥				
								NORMAL			AUTO-INC.		SHORT			LONG	
		OPCODE	BYTES	STATE TIMES	OPCODE	BYTES	STATE TIMES	OPCODE	BYTES	STATE① TIMES	BYTES	STATE① TIMES	OPCODE	BYTES	STATE① TIMES⑥	BYTES	STATE① TIMES⑥
LOGICAL INSTRUCTIONS																	
AND	2	60	3	4	61	4	5	62	3	6/11	3	7/12	63	4	6/11	5	7/12
AND	3	40	4	5	41	5	6	42	4	7/12	4	8/13	43	5	7/12	6	8/13
ANDB	2	70	3	4	71	3	4	72	3	6/11	3	7/12	73	4	6/11	5	7/12
ANDB	3	50	4	5	51	4	5	52	4	7/12	4	8/13	53	5	7/12	6	8/13
OR	2	80	3	4	81	4	5	82	3	6/11	3	7/12	83	4	6/11	5	7/12
ORB	2	90	3	4	91	3	4	92	3	6/11	3	7/12	93	4	6/11	5	7/12
XOR	2	84	3	4	85	4	5	86	3	6/11	3	7/12	87	4	6/11	5	7/12
XORB	2	94	3	4	95	3	4	96	3	6/11	3	7/12	97	4	6/11	5	7/12
DATA TRANSFER INSTRUCTIONS																	
LD	2	A0	3	4	A1	4	5	A2	3	6/11	3	7/12	A3	4	6/11	5	7/12
LDB	2	B0	3	4	B1	3	4	B2	3	6/11	3	7/12	B3	4	6/11	5	7/12
ST	2	C0	3	4	—	—	——	C2	3	7/11	3	8/12	C3	4	7/11	5	8/12
STB	2	C4	3	4	—	—	——	C6	3	7/11	3	8/12	C7	4	7/11	5	8/12
LDBSE	2	BC	3	4	BD	3	4	BE	3	6/11	3	7/12	BF	4	6/11	5	7/12
LDBZE	2	AC	3	4	AD	3	4	AE	3	6/11	3	7/12	AF	4	6/11	5	7/12
STACK OPERATIONS (internal stack)																	
PUSH	1	C8	2	8	C9	3	8	CA	2	11/15	2	12/16	CB	3	11/15	4	12/16
POP	1	CC	2	12	—	—	——	CE	2	14/18	2	14/18	CF	3	14/18	4	14/18
PUSHF	0	F2	1	8													
POPF	0	F3	1	9													
STACK OPERATIONS (external stack)																	
PUSH	1	C8	2	12	C9	3	12	CA	2	15/19	2	16/20	CB	3	15/19	4	16/20
POP	1	CC	2	14	—	—	——	CE	2	16/20	2	16/20	CF	3	16/20	4	16/20
PUSHF	0	F2	1	12													
POPF	0	F3	1	13													

JUMPS AND CALLS							
MNEMONIC	OPCODE	BYTES	STATES	MNEMONIC	OPCODE	BYTES	STATES
LJMP	E7	3	8	LCALL	EF	3	13/16⑤
SJMP	20-27④	2	8	SCALL	28-2F④	2	13/16⑤
BR[ ]	E3	2	8	RET	F0	1	12/16⑤
				TRAP③	F7	1	21/24

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NOTES:
① Number of state times shown for internal/external operands.
③ The assembler does not accept this mnemonic.
④ The least significant 3 bits of the opcode are concatenated with the following 8 bits to form an 11-bit, 2's complement, offset for the relative call or jump.
⑤ State times for stack located internal/external.
⑥ State times shown for 16-bit bus.

8.0 OPCODES, INSTRUCTION LENGTH AND STATE TIMES (Continued)

CONDITIONAL JUMPS

All conditional jumps are 2 byte instructions. They require 8 state times if the jump is taken, 4 if it is not.(8)

MNEMONIC	OPCODE	MNEMONIC	OPCODE	MNEMONIC	OPCODE	MNEMONIC	OPCODE
JC	DB	JE	DF	JGE	D6	JGT	D2
JNC	D3	JNE	D7	JLT	DE	JLE	DA
JH	D9	JV	DD	JVT	DC	JST	D8
JNH	D1	JNV	D5	JNVT	D4	JNST	D0

JUMP ON BIT CLEAR OR BIT SET

These instructions are 3 byte instructions. They require 9 state times if the jump is taken, 5 if it is not.(8)

	BIT NUMBER							
MNEMONIC	0	1	2	3	4	5	6	7
JBC	30	31	32	33	34	35	36	37
JBS	38	39	3A	3B	3C	3D	3E	3F

LOOP CONTROL

MNEMONIC	OPCODE	BYTES	STATE TIMES
DJNZ	EO	3	5/9 STATE TIME (NOT TAKEN/TAKEN)(8)

SINGLE REGISTER INSTRUCTIONS

MNEMONIC	OPCODE	BYTES	STATES(8)	MNEMONIC	OPCODE	BYTES	STATES(8)
DEC	05	2	4	EXT	06	2	4
DECB	15	2	4	EXTB	16	2	4
NEG	03	2	4	NOT	02	2	4
NEGB	13	2	4	NOTB	12	2	4
INC	07	2	4	CLR	01	2	4
INCB	17	2	4	CLRB	11	2	4

SHIFT INSTRUCTIONS

INSTR MNEMONIC	WORD		INSTR MNEMONIC	BYTE		INSTR MNEMONIC	DBL WD		STATE TIMES(8)
	OP	B		OP	B		OP	B	
SHL	09	3	SHLB	19	3	SHLL	0D	3	7 + 1 PER SHIFT(7)
SHR	08	3	SHRB	18	3	SHRL	0C	3	7 + 1 PER SHIFT(7)
SHRA	0A	3	SHRAB	1A	3	SHRAL	0E	3	7 + 1 PER SHIFT(7)

8.0 OPCODES, INSTRUCTION LENGTH AND STATE TIMES (Continued)

SPECIAL CONTROL INSTRUCTIONS

MNEMONIC	OPCODE	BYTES	STATES(8)	MNEMONIC	OPCODE	BYTES	STATES(8)
SETC	F9	1	4	DI	FA	1	4
CLRC	F8	1	4	EI	FB	1	4
CLRVT	FC	1	4	NOP	FD	1	4
RST(6)	FF	1	166	SKIP	00	2	4

NORMALIZE

MNEMONIC	OPCODE	BYTES	STATE TIMES
NORML	0F	3	11 + 1 PER SHIFT

NOTES:
6. This instruction takes 2 states to pull $\overline{\text{RESET}}$ low, then holds it low for at least one state time to initiate a reset. The reset takes 13 states, at which time the program restarts at location 2080H.
7. Execution will take at least 8 states, even for 0 shift.
8. State times shown for 16-bit bus.

9.0 INTERRUPT TABLE

Vector	Vector Location		Priority
	(High Byte)	(Low Byte)	
Software Trap	2011H	2010H	Not Applicable
Extint	200FH	200EH	7 (Highest)
Serial Port	200DH	200CH	6
Software Timers	200BH	200AH	5
HSI.0	2009H	2008H	4
High Speed Outputs	2007H	2006H	3
HSI Data Available	2005H	2004H	2
A/D Conversion Complete	2003H	2002H	1
Timer Overflow	2001H	2000H	0 (Lowest)

10.0 FORMULAS

Baud Rate Calculations

Using XTAL1:

Mode 0: $\text{Baud Rate} = \frac{\text{XTAL1 frequency}}{4 * (B + 1)}; B \neq 0$

Others: $\text{Baud Rate} = \frac{\text{XTAL1 frequency}}{64 * (B + 1)}$

Using T2CLK:

Mode 0: $\text{Baud Rate} = \frac{\text{T2CLK frequency}}{B}; B \neq 0$

Others: $\text{Baud Rate} = \frac{\text{T2CLK frequency}}{16 * B}; B \neq 0$

Note that B cannot equal 0, except when using XTAL1 in other than Mode 0.

8X9XBH Signature Word

Device	Signature Word
879XBH	896FH
839XBH	896EH
809XBH	Undefined

11.0 RESET STATUS

Register	RESET Value
Port 1	XXXXXXXXB
Port 2	XX0XXXX1B
Port 3	11111111B
Port 4	11111111B
PWM Control	00H
Serial Port (Transmit)	undefined
Serial Port (Receive)	undefined
Baud Rate Register	undefined
Serial Port Control	XXXX0XXXB
Serial Port Status	X00XXXXXB
A/D Command	undefined
A/D Result	undefined
Interrupt Pending	undefined
Interrupt Mask	00000000B
Timer 1	0000H
Timer 2	0000H
WDT	0000H
HSI Mode	XXXXXXXXB
HSI Status	undefined
IOS0	00000000B
IOS1	00000000B
IOC0	X0X0X0X0B
IOC1	X0X0XXX1B
HSI FIFO	empty
HSI CAM	empty
HSO SFR	000000B
PSW	0000H
Stack Pointer	undefined
Program Counter	2080H
Port 1	weak pullups
Port 2.6, Port 2.7	weak pullups
Ports 3 and 4	floating
HSO.0, HSO.1, HSO.2, HSO.3	low
HSO.4, HSO.5	floating
$\overline{RD}$	high
$\overline{WR}/\overline{WRL}$	high
ALE/$\overline{ADV}$	high
$\overline{BHE}/\overline{WRH}$	high
INST	low

intel®

September 1992

8XC196KB
Quick Reference

Order Number: 272111-002

8XC196KB Quick Reference

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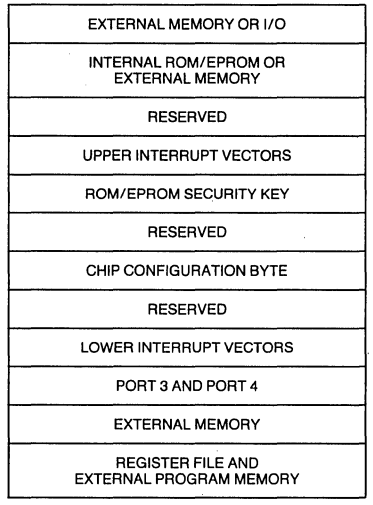
1.0 MEMORY MAP



NOTE:
Code executed in locations 0 to 0FFH will be forced external.

2.0 SFR MAP

	HWINDOW 0 when Read	HWINDOW 0 when Written	HWINDOW 15 when Read	HWINDOW 15 when Written
19H	SP (HI)	SP (HI)	SP (HI)	SP (HI)
18H	SP (LO)	SP (LO)	SP (LO)	SP (LO)
17H	IOS2	PWM_CONTROL	PWM_CONTROL	IOS2
16H	IOS1	IOC1	IOC1	IOS1
15H	IOS0	IOC0	IOC0	IOS0
14H	WSR	WSR	WSR	WSR
13H	INT_MASK1	INT_MASK1	INT_MASK1	INT_MASK1
12H	INT_PEND1	INT_PEND1	INT_PEND1	INT_PEND1
11H	SP_STAT	SP_CON	SP_CON	SP_STAT
10H	PORT2	PORT2	RESERVED**	RESERVED**
0FH	PORT1	PORT1	RESERVED**	RESERVED**
0EH	PORT0	BAUD_REG	RESERVED**	RESERVED**
0DH	TIMER2 (HI)	TIMER2 (HI)	T2CAPTURE(HI)	T2CAPTURE(HI)
0CH	TIMER2 (LO)	TIMER2 (LO)	T2CAPTURE(LO)	T2CAPTURE(LO)
0BH	TIMER1 (HI)	IOC2	IOC2	TIMER1 (HI)
0AH	TIMER1 (LO)	WATCHDOG	WATCHDOG	TIMER1 (LO)
09H	INT_PEND	INT_PEND	INT_PEND	INT_PEND
08H	INT_MASK	INT_MASK	INT_MASK	INT_MASK
07H	SBUF (RX)	SBUF (TX)	SBUF(TX)	SBUF(RX)
06H	HSI_STATUS	HSO_COMMAND	HSO_COMMAND	HSI_STATUS
05H	HSI_TIME (HI)	HSO_TIME (HI)	HSO_TIME(HI)	HSI_TIME (HI)
04H	HSI_TIME (LO)	HSO_TIME (LO)	HSO_TIME(LO)	HSI_TIME (LO)
03H	AD_RESULT (HI)	HSI_MODE	HSI_MODE	AD_RESULT (HI)
02H	AD_RESULT (LO)	AD_COMMAND	AD_COMMAND	AD_RESULT (LO)
01H	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)
00H	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)

**Reserved registers should not be written or read.

CCR (2018H: Byte)

7	6	5	4	3	2	1	0
LOC1	LOC0	IRC1	IRC0	ALE	WR	BW0	PD

PD 1 = Powerdown Mode Enabled
0 = Powerdown Mode Disabled

BW0 1 = Buswidth is BUSWIDTH pin Controlled
0 = Buswidth is 8-Bit

WR 1 = $\overline{WR/BHE}$
0 = $\overline{WRL/WRH}$

ALE 1 = ALE
0 = $\overline{ADV}$

IRC0, 1 READY Control. (See Table Below)

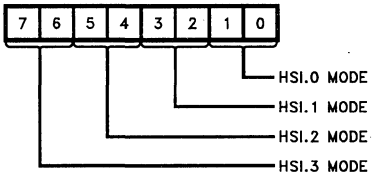
LOC0, 1 ROM, EPROM Protection. (See Table Below)

IRC1	IRC0	Max Wait States
0	0	1 Wait State
0	1	2 Wait States
1	0	3 Wait States
1	1	READY Pin Controlled

LOC1	LOC0	Max Wait States
0	0	Read and Write Protected
0	1	Read Protected Only
1	0	Write Protected Only
1	1	No Protection

3.0 SFR BIT SUMMARY

HSI_MODE (03H HWIN0 Write)
(03H HWIN15 Read)

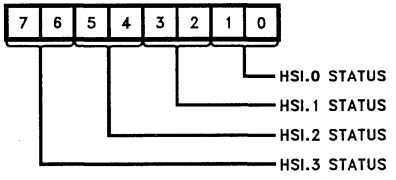


WHERE EACH 2 – BIT MODE CONTROL FIELD DEFINES ONE OF 4 POSSIBLE MODES:

00 8 POSITIVE TRANSITIONS
01 EACH POSITIVE TRANSITION
10 EACH NEGATIVE TRANSITION
11 EVERY TRANSITION (POSITIVE AND NEGATIVE)

272111-1

HSI_STATUS (06H HWIN0 Read)
(06H HWIN15 Write)

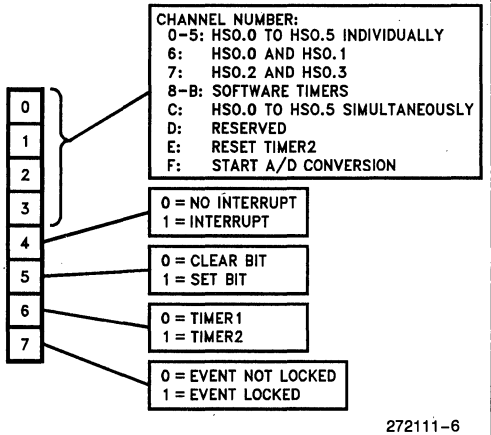


WHERE FOR EACH 2 – BIT STATUS FIELD THE LOWER BIT INDICATES WHETHER OR NOT AN EVENT HAS OCCURRED ON THIS PIN AND THE UPPER BIT INDICATES THE CURRENT STATUS OF THE PIN.

272111-2

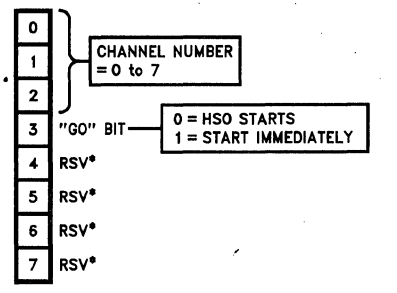
14

HSO_COMMAND (06H HWIN0 Write)
(06H HWIN15 Read)



272111-6

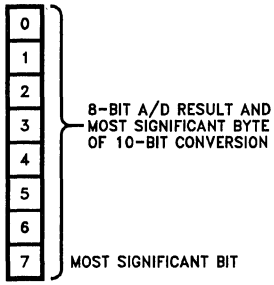
AD_COMMAND (02H HWIN0 Write)
(02H HWIN15 Read)



*RSV – RESERVED BITS MUST BE WRITTEN AS 0

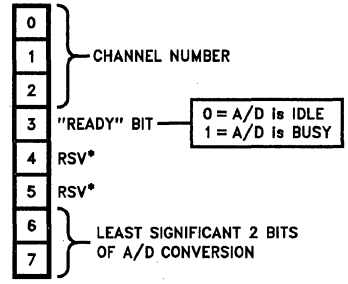
272111-4

AD_RESULT (HI) (03H HWIN0 Read)
(03H HWIN15 Write)



272111-3

AD_RESULT (LO) (02H HWIN0 Read)
(02H HWIN15 Write)



*RSV – RESERVED BITS MUST BE WRITTEN AS 0

272111-5

INT_MASK (08H All Windows R/W)
INT_PEND (09H All Windows R/W)

7	6	5	4	3	2	1	0
EXT INT	SER PORT	SOFT TIMER	HSI.0 PIN	HSO PIN	HSI DATA	A/D DONE	TIMER OVF

272111-19

NOTE:
MASK and PEND bits share the same names.

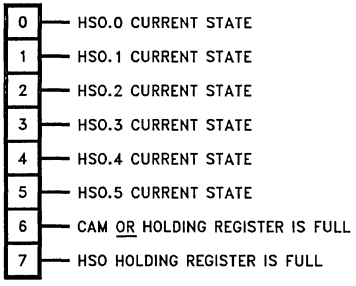
INT_MASK1 (13H All Windows R/W)
INT_PEND1 (12H All Windows R/W)

7	6	5	4	3	2	1	0
NMI*	FIFO FULL	EXT INT1	T2 OVF	T2 CAP	HSI FIFO FULL	RI	TI

272111-20

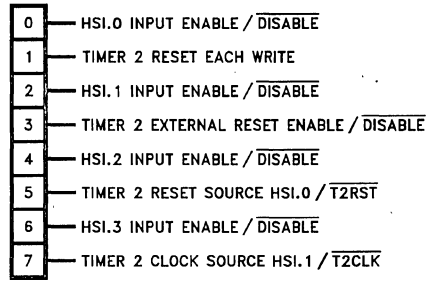
NOTE:
MASK1 and PEND1 bits share the same names.
*NMI is a reserved bit, must be = 0.

IOS0 (15H HWIN0 Read)
(15H HWIN15 Write)



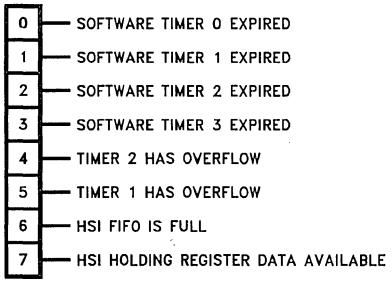
272111-7

IOC0 (15H HWIN0 Write)
(15H HWIN15 Read)



272111-9

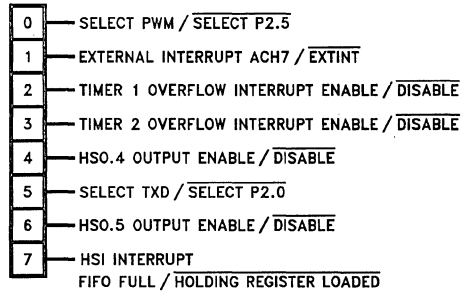
IOS1 (16H HWIN0 Read)
(16H HWIN15 Write)



BITS 0 - 5 ARE CLEARED WHEN READ

272111-8

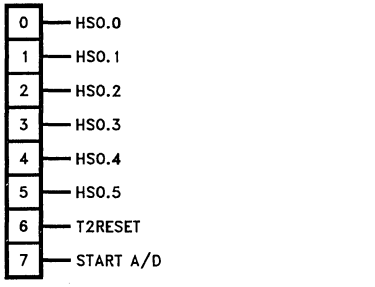
IOC1 (16H HWIN0 Write)
(16H HWIN15 Read)



272111-10

IOS2 (17H HWIN0 Read)
(17H HWIN15 Write)

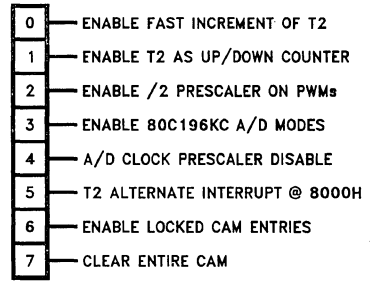
INDICATES WHICH HSO EVENT OCCURRED



IOS2 IS CLEARED WHEN READ

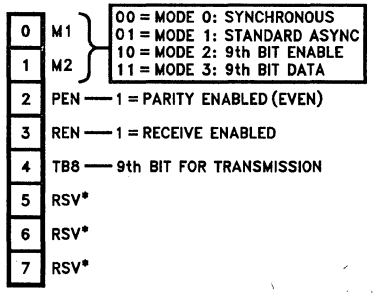
272111-18

IOC2 (0BH HWIN0 Write)
(0BH HWIN15 Read)



272111-17

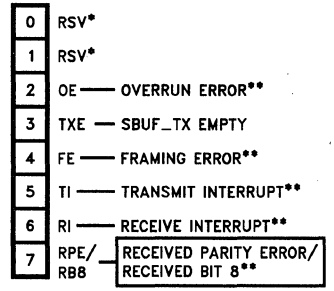
SP_CON (11H HWIN0 Write)
(11H HWIN15 Read)



*RSV – RESERVED BITS MUST BE WRITTEN AS 0

272111-11

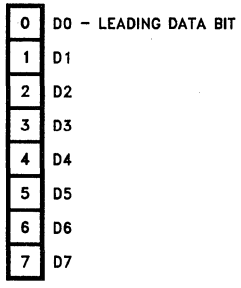
SP_STAT (11H HWIN0 Read)
(11H HWIN15 Write)



*RSV – RESERVED BITS MUST BE WRITTEN AS 0
**THESE BITS CLEARED WHEN READ

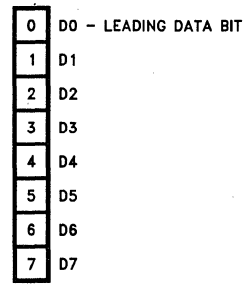
272111-12

SBUF_TX (07H HWIN0 Write)
(07H HWIN15 Read)



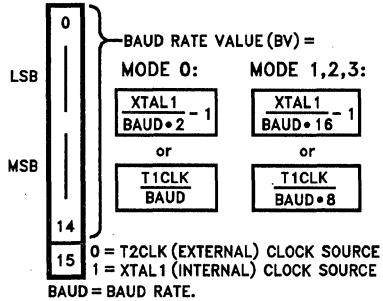
272111-13

SBUF_RX (07H HWIN0 Read)
(07H HWIN15 Write)



272111-14

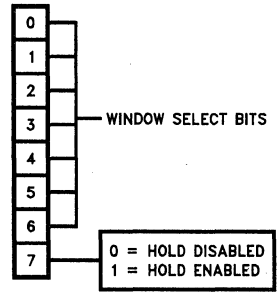
BAUD_REG (0EH HWIN0 Write)



BAUD = BAUD RATE.
MUST WRITE BV AS 2 CONSECUTIVE BYTES, LSB FIRST.

272111-15

WSR (14H All Windows R/W)



272111-16

4.0 PIN DEFINITION TABLE

8XC196KB, 8XC198, 8XC194 Pin Definition Table

Pin Name	8XC196KB			8XC198		8XC194	
	68L PLCC	68L PGA	80L QFP	52L PLCC	80L QFP	52L PLCC	80L QFP
ACH0	6	4	18	N/A	N/C	N/A	N/C
ACH1	5	5	17	N/A	N/C	N/A	N/C
ACH2	7	3	19	N/A	N/C	N/A	N/C
ACH3	4	6	16	N/A	N/C	N/A	N/C
ACH4	11	67	24	9	24	N/A	N/C
ACH5	10	68	23	8	23	N/A	N/C
ACH6	8	2	20	6	20	N/A	N/C
ACH7	9	1	21	7	21	N/A	N/C
AD0	60	18	2	48	2	48	2
AD1	59	19	1	47	1	47	1
AD2	58	20	80	46	80	46	80
AD3	57	21	78	45	78	45	78
AD4	56	22	77	44	77	44	77
AD5	55	23	76	43	76	43	76
AD6	54	24	74	42	74	42	74
AD7	53	25	73	41	73	41	73
AD8	52	26	72	40	72	40	72
AD9	51	27	71	39	71	39	71
AD10	50	28	70	38	70	38	70
AD11	49	29	69	37	69	37	69
AD12	48	30	68	36	68	36	68
AD13	47	31	67	35	67	35	67
AD14	46	32	66	34	66	34	66
AD15	45	33	65	33	65	33	65
ADV	62	16	4	50	4	50	4
AINC	42	36	61	30	61	30	61
ALE	62	16	4	50	4	50	4
ANGND	12	66	25	10	25	10	25
BHE	41	37	60	N/A	N/C	N/A	N/C
BREQ	30	48	46	N/A	N/C	N/A	N/C
BUSWIDTH	64	14	6	N/A	N/A	N/A	N/A
CDE*	14	64	N/A	N/A	N/A	N/A	N/A
CLKOUT	65	13	7	N/A	N/C	N/A	N/C
EA	2	8	14	5	14	5	14
EXTINT	15, 9	63, 25	28, 21	13	28, 21	13	28, 21
HOLD	32	46	48	N/A	N/C	N/A	N/C
HLDA	31	47	47	N/A	N/C	N/A	N/C
HSI.0	24	54	39	17	39	17	39
HSI.1	25	53	40	18	40	18	40
HSI.2	26	52	41	19	41	19	41
HSI.3	27	51	43	20	43	20	43

4.0 PIN DEFINITION TABLE (Continued)

8XC196KB, 8XC198, 8XC194 Pin Definition Table

Pin Name	8XC196KB			8XC198		8XC194	
	68L PLCC	68L PGA	80L QFP	52L PLCC	80L QFP	52L PLCC	80L QFP
HSO.0	28	50	44	21	44	21	44
HSO.1	29	49	45	22	45	22	45
HSO.2	34	44	50	23	50	23	50
HSO.3	35	43	53	25	53	25	53
HSO.4	26	52	41	19	41	19	41
HSO.5	27	51	43	20	43	20	43
INST	63	15	5	51	5	51	5
NMI	3	7	15	N/A	N/A	N/A	N/A
P0.0	6	4	18	N/A	N/C	N/A	N/C
P0.1	5	5	17	N/A	N/C	N/A	N/C
P0.2	7	3	19	N/A	N/C	N/A	N/C
P0.3	4	6	16	N/A	N/C	N/A	N/C
P0.4	11	67	24	9	24	9	24
P0.5	10	68	23	8	23	8	23
P0.6	8	2	20	6	20	6	20
P0.7	9	1	21	7	21	7	21
P1.0	19	59	34	N/A	N/C	N/A	N/A
P1.1	20	58	35	N/A	N/C	N/A	N/C
P1.2	21	57	36	N/A	N/C	N/A	N/C
P1.3	22	56	37	N/A	N/C	N/A	N/C
P1.4	23	55	38	N/A	N/C	N/A	N/C
P1.5	30	48	46	N/A	N/C	N/A	N/C
P1.6	31	47	47	N/A	N/C	N/A	N/C
P1.7	32	46	48	N/A	N/C	N/A	N/C
P2.0	18	60	32	16	32	16	32
P2.1	17	61	31	15	31	15	31
P2.2	15	63	28	13	28	13	28
P2.3	44	34	64	32	64	32	64
P2.4	42	36	61	30	61	30	61
P2.5	39	39	58	28	58	28	58
P2.6	33	45	49	N/A	N/C	N/A	N/C
P2.7	38	40	57	N/A	N/C	N/A	N/C
P3.0	60	18	2	48	2	48	2
P3.1	59	19	1	47	1	47	1
P3.2	58	20	80	46	80	46	80
P3.3	57	21	78	45	78	45	78
P3.4	56	22	77	44	77	44	77
P3.5	55	23	76	43	76	43	76
P3.6	54	24	74	42	74	42	74
P3.7	53	25	73	41	73	41	73

4.0 PIN DEFINITION TABLE (Continued)

8XC196KB, 8XC198, 8XC194 Pin Definition Table

Pin Name	8XC196KB			8XC198		8XC194	
	68L PLCC	68L PGA	80L QFP	52L PLCC	80L QFP	52L PLCC	80L QFP
P4.0	52	26	72	40	72	40	72
P4.1	51	27	71	39	71	39	71
P4.2	50	28	70	38	70	38	70
P4.3	49	29	69	37	69	37	69
P4.4	48	30	68	36	68	36	68
P4.5	47	31	67	35	67	35	67
P4.6	46	32	66	34	66	34	66
P4.7	45	33	65	33	65	33	65
PALE	17	61	31	15	31	15	31
PMODE.0	11	67	24	9	24	9	24
PMODE.1	10	68	23	8	23	8	23
PMODE.2	8	2	20	6	20	6	20
PMODE.3	9	1	21	7	21	7	21
PROG	15	63	28	13	28	13	28
RESET	16	62	30	14	30	14	30
RXD	17	61	31	15	31	15	31
SID.0	24	54	39	17	39	17	39
SID.1	25	53	40	18	40	18	40
SID.2	26	52	41	19	41	19	41
SID.3	27	51	43	20	43	20	43
T2CAPTURE	38	40	57	N/A	N/C	N/A	N/C
T2CLK	44	34	64	32	64	32	64
T2RST	42	36	61	30	61	30	61
T2UPDN	33	45	49	N/A	N/C	N/A	N/C
TXD	18	60	32	16	32	16	32
V_{CC}	1	9	12, 13, 29, 52, 75	4	12, 13, 29, 52, 75	4	12, 13, 29, 52, 75
V_{PP}	37	41	56	27	56	27	56
V_{REF}	13	65	26	11	26	11	26
V_{SS}	68, 36	10, 42	10, 11, 27, 33, 42, 51, 54, 55, 63, 79	3, 12, 24, 26, 52	6, 10, 11, 15, 27, 33, 42, 51, 54, 55, 63, 79	3, 12, 24, 26, 52	6, 10, 11, 15, 27, 33, 42, 51, 54, 55, 63, 79
WR	40	38	59	29	59	29	59
WRL	40	38	59	29	59	29	59
WRH	41	37	60	N/A	N/C	N/A	N/C
XTAL1	67	11	9	2	9	2	9
XTAL2	66	12	8	1	8	1	8

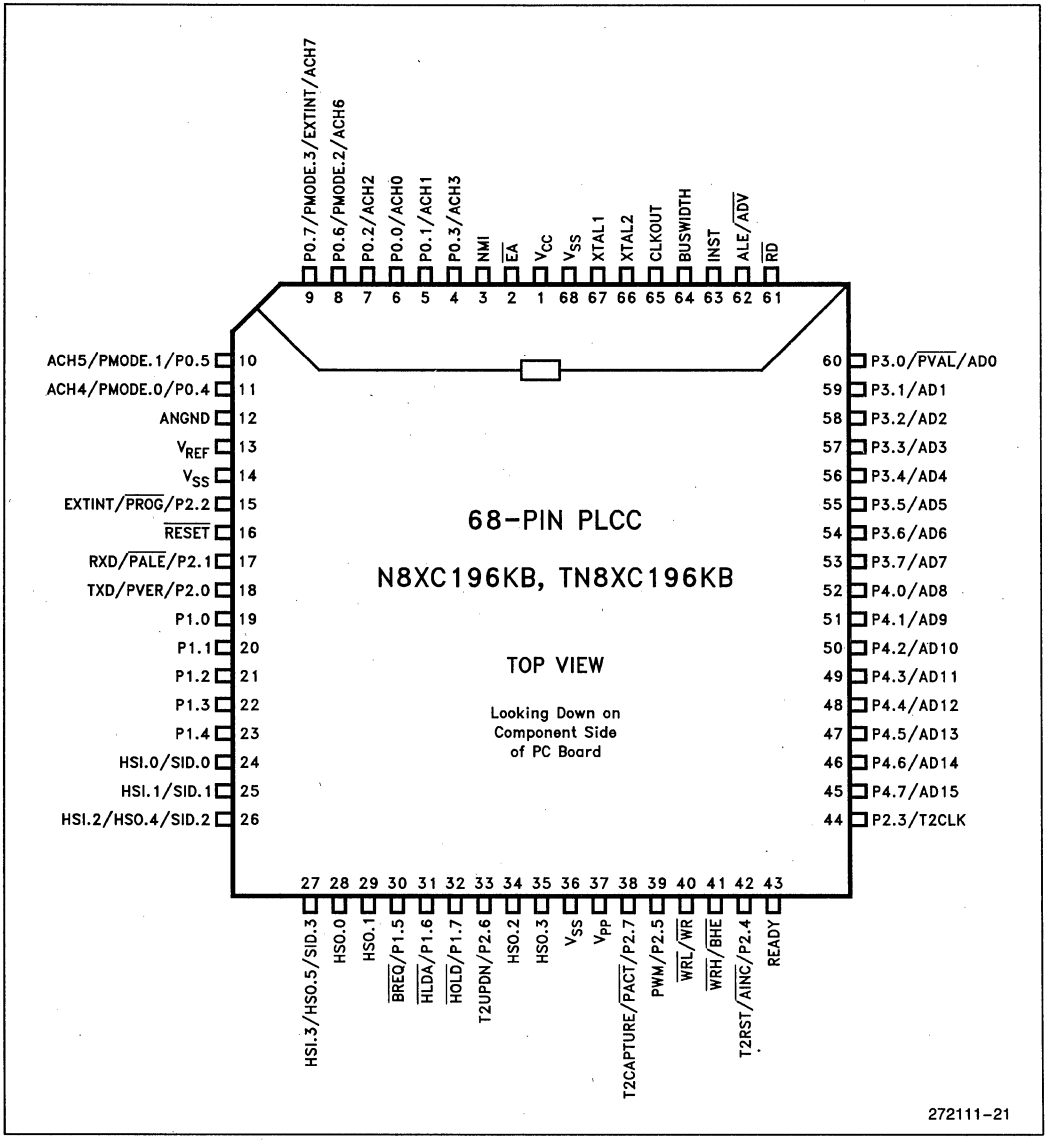
NOTES:

*CDE This pin was formerly the Clock Detect Enable pin. This is not functional, and this pin must be connected to V_{SS}.

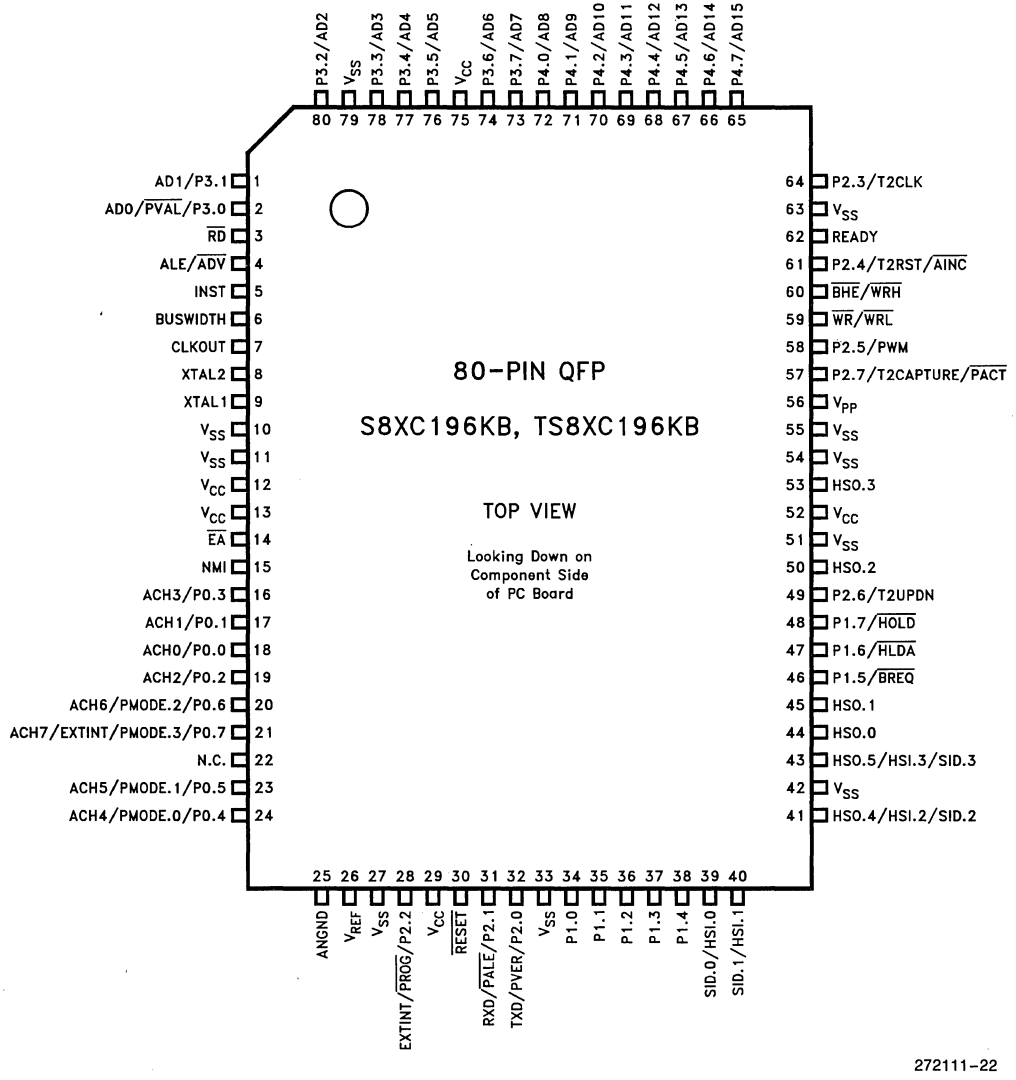
N/A = Not Available

N/C = No Connect. Do not connect these pins.

5.0 PACKAGE PIN ASSIGNMENTS



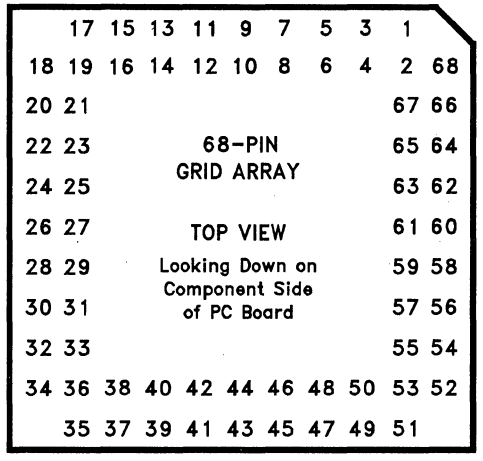
68-Pin PLCC Package Diagram



NOTE:
N.C. means No Connect (do not connect these pins).

80-Pin QFP Package Diagram

14



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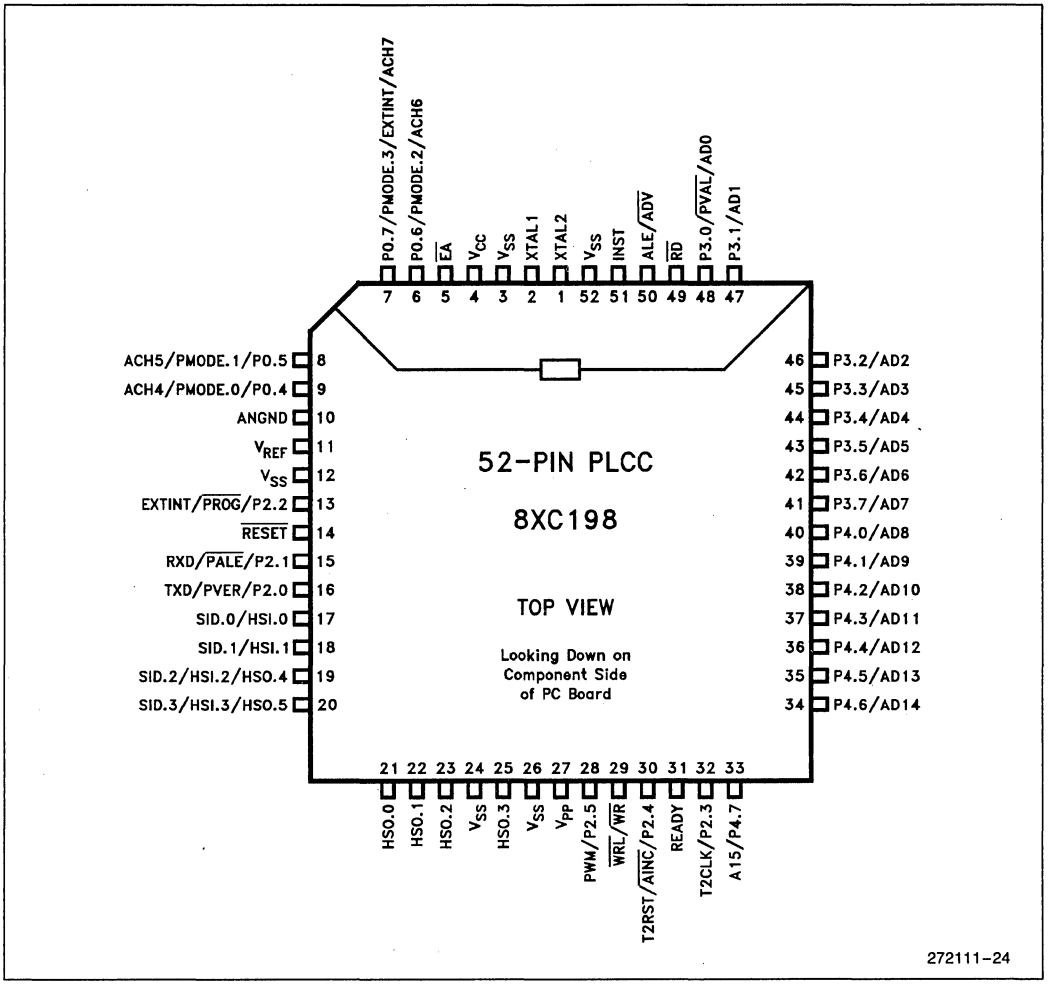
68-Pin PGA Package (Top View) 80C196KB Only

PGA	Description
1	ACH7/P0.7/PMODE.3
2	ACH6/P0.6/PMODE.2
3	ACH2/P0.2
4	ACH0/P0.0
5	ACH1/P0.1
6	ACH3/P0.3
7	NMI
8	$\overline{EA}$
9	V_{CC}
10	V_{SS}
11	XTAL1
12	XTAL2
13	CLKOUT
14	BUSWIDTH
15	INST
16	ALE/$\overline{ADV}$
17	$\overline{RD}$
18	AD0/P3.0/$\overline{PVAL}$
19	AD1/P3.1
20	AD2/P3.2
21	AD3/P3.3
22	AD4/P3.4
23	AD5/P3.5

PGA	Description
24	AD6/P3.6
25	AD7/P3.7/EXTINT
26	AD8/P4.0
27	AD9/P4.1
28	AD10/P4.2
29	AD11/P4.3
30	AD12/P4.4
31	AD13/P4.5
32	AD14/P4.6
33	AD15/P4.7
34	T2CLK/P2.3
35	READY
36	T2RST/P2.4/$\overline{AINC}$
37	$\overline{BHE}$/$\overline{WRH}$
38	$\overline{WR}$/$\overline{WRL}$
39	PWM/P2.5
40	P2.7/T2CAPTURE/$\overline{PACT}$
41	V_{PP}
42	V_{SS}
43	HSO.3/SID3
44	HSO.2/SID2
45	P2.6/T2UPDN
46	P1.7/$\overline{HOLD}$

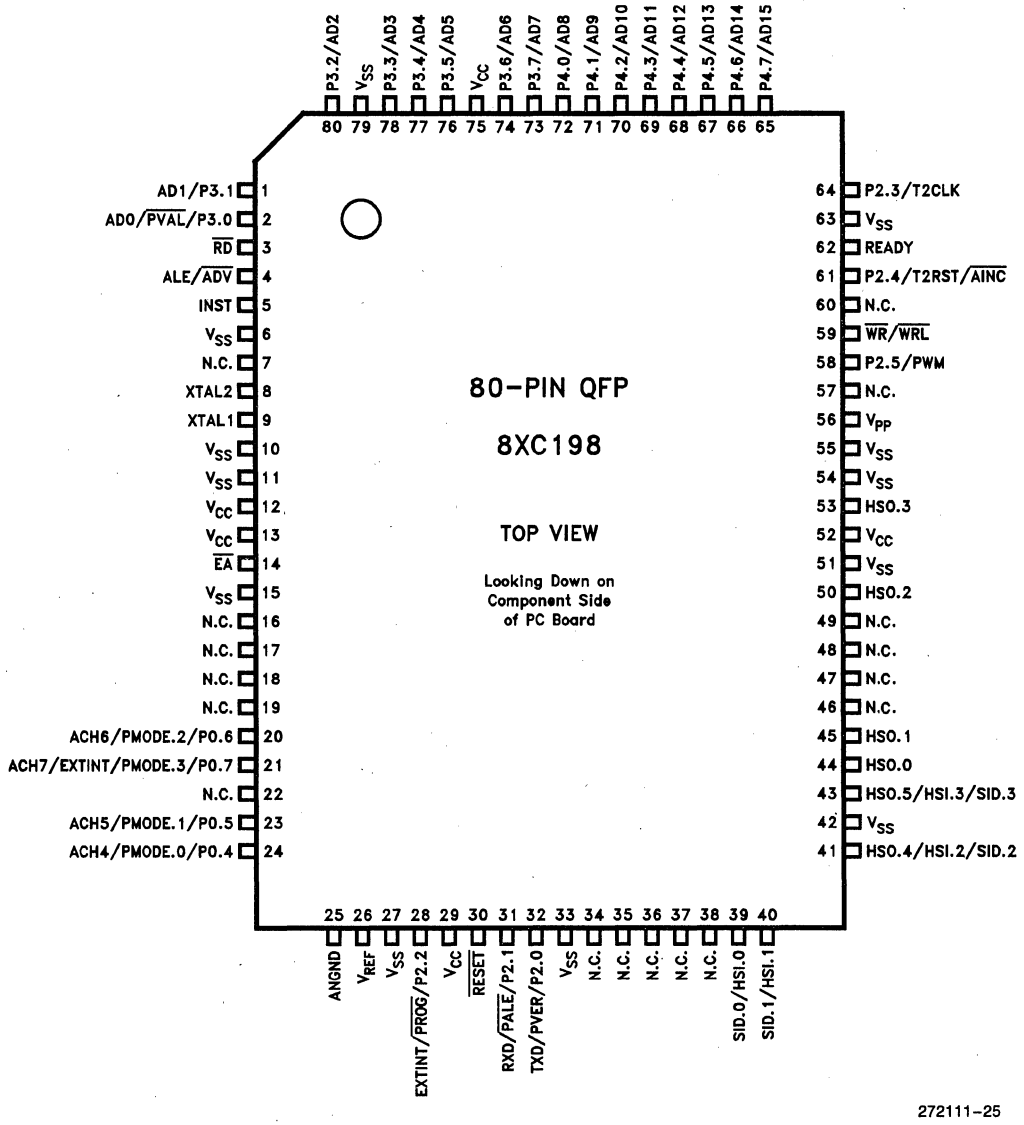
PGA	Description
47	P1.6/$\overline{HLDA}$
48	P1.5/$\overline{BREQ}$
49	HSO.1
50	HSO.0
51	HSO.5/HSI.3/SID.3
52	HSO.4/HSI.2/SID.2
53	HSI.1/SID.1
54	HSI.0/SID.0
55	P1.4
56	P1.3
57	P1.2
58	P1.1
59	P1.0
60	TSD/P2.0/PVER
61	RXD/P2.1/$\overline{PALE}$
62	$\overline{RESET}$
63	EXTINT/P2.2/$\overline{PROG}$
64	V_{SS}(1)
65	V_{REF}
66	ANGND
67	ACH4/P0.4/PMODE.0
68	ACH5/P0.5/PMODE.1

NOTE:
1. This pin was formerly the Clock Detect Enable pin. This function is not guaranteed to work. This pin must be directly connected to V_{SS}.



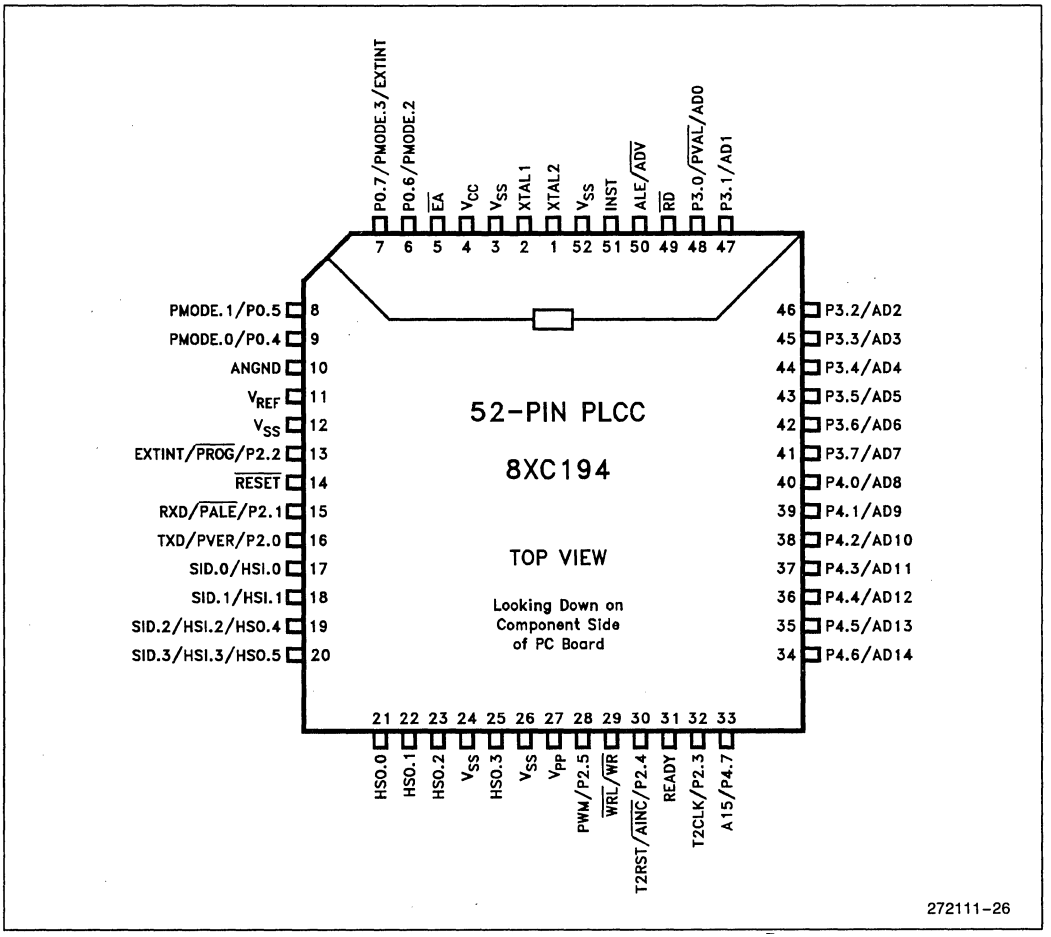
52-Pin PLCC Package Diagram

14



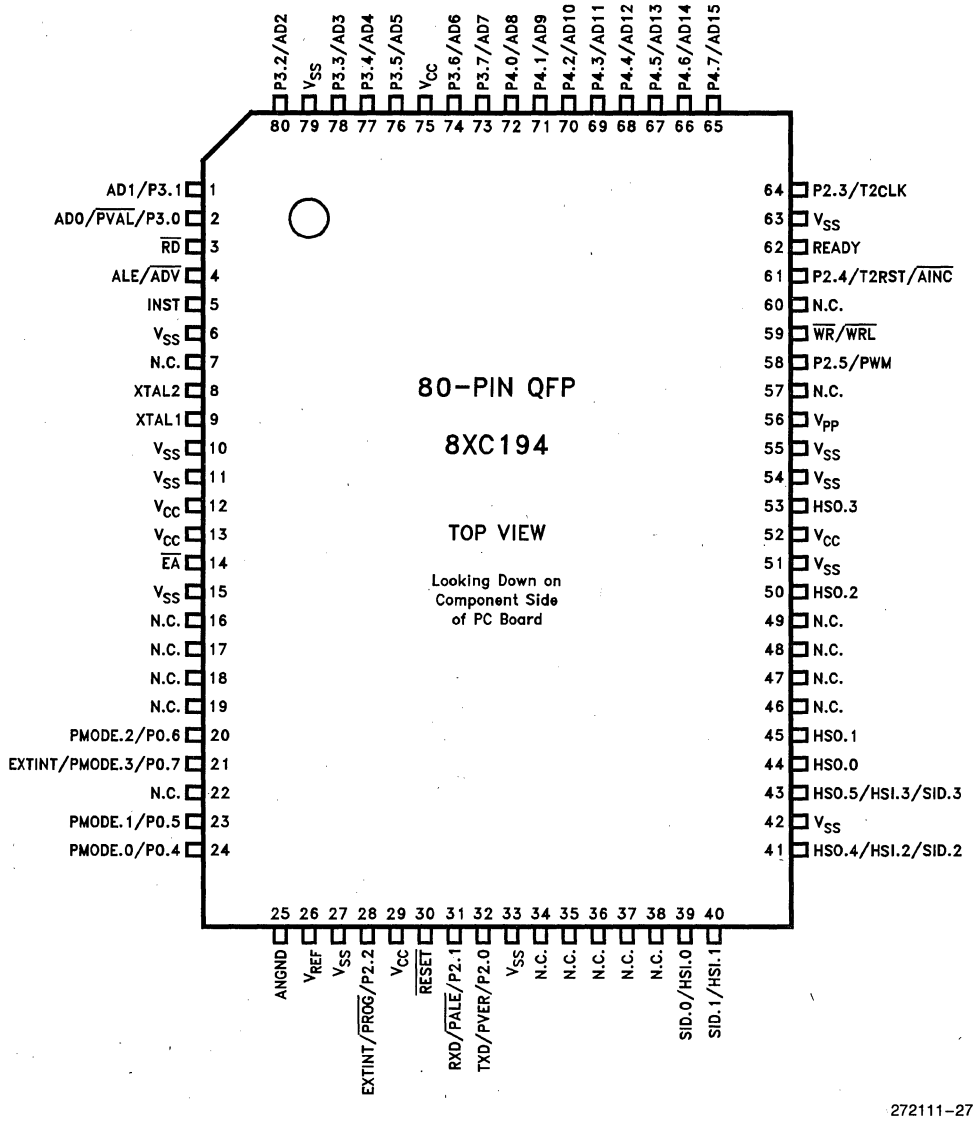
NOTE:
N.C. means No Connect (do not connect these pins).

80-Pin QFP Package Diagram



52-Pin PLCC Package Diagram

14



NOTE:
N.C. means No Connect (do not connect these pins).

80-Pin QFP Package Diagram

6.0 PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of them must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage. Also timing pin for the return from power down circuit. Connect this pin with a 1 μF capacitor to V_{SS}. If this function is not used, connect to V_{CC}.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input and open-drain output. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. RESET has an internal pullup.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch and output low indicates a data fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{\text{BHE}}$ = 1), to the high byte only (A0 = 1, $\overline{\text{BHE}}$ = 0), or both bytes (A0 = 0, $\overline{\text{BHE}}$ = 0). If the $\overline{\text{WRH}}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles.

6.0 PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle (held not ready) is available through configuration of CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit. The HSI pins are also used as the SID in Slave Programming Mode.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. Three pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins set the Programming Mode.
Port 1	8-bit quasi-bidirectional I/O port. These pins are shared with $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and $\overline{\text{BREQ}}$.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 87C196KB.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus. Enabled by setting WSR.7.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2, and 3. The TxD function is enabled by setting IOC1.5. In mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. The RxD function is enabled by setting SPCON.3. In mode 0 the pin functions as input or output data.
EXTINT	A rising edge on the EXTINT pin will generate an external interrupt. EXTINT is selected as the external interrupt source by setting IOC1.1 high.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2. The external reset function is enabled by setting IOCO.3. T2RST is enabled as the reset source by clearing IOCO.5.
PWM	Port 2.5 can be enabled as a PWM output by setting IOC1.0. The duty cycle of the PWM is determined by the value loaded into the PWM-CONTROL register (17H).
T2UPDN	The T2UPDN pin controls the direction of Timer2 as an up or down counter. The Timer2 up/down function is enabled by setting IOC2.1.
T2CAP	A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register (location 0CH in Window 15).
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
SID	Slave ID Number. Used to assign each slave a pin of Port 3 or 4 to use for passing programming verification acknowledgement. For example, if gang programming in the Slave Programming Mode, the slave with SID = 001 will use Port 3.1 to signal correct or incorrect program verification.

6.0 PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PACT}}$	Programming Active. Used in the Auto Programming Mode to indicate when programming activity is complete.
$\overline{\text{PVAL}}$	Program Valid. This signal indicates the success or failure of programming in the Auto Programming Mode. A zero indicates successful programming.
PVER	Program Verification. Used in Slave Programming and Auto CLB Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
PORT 3 and 4 During Programming	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory. Should have pullups to V_{CC} (15 kΩ).

7.0 OPCODE TABLE

00	SKIP
01	CLR
02	NOT
03	NEG
04	RESERVED
05	DEC
06	EXT
07	INC
08	SHR
09	SHL
0A	SHRA
0B	RESERVED
0C	SHRL
0D	SHLL
0E	SHRAL
0F	NORML
10	RESERVED
11	CLRB
12	NOTB
13	NEGB
14	RESERVED

15	DECB
16	EXTB
17	INCB
18	SHRB
19	SHLB
1A	SHRAB
1B	RESERVED
1C	RESERVED
1D	RESERVED
1E	RESERVED
1F	RESERVED
20	SJMP
21	SJMP
22	SJMP
23	SJMP
24	SJMP
25	SJMP
26	SJMP
27	SJMP
28	SCALL
29	SCALL

2A	SCALL
2B	SCALL
2C	SCALL
2D	SCALL
2E	SCALL
2F	SCALL
30	JBC
31	JBC
32	JBC
33	JBC
34	JBC
35	JBC
36	JBC
37	JBC
38	JBS
39	JBS
3A	JBS
3B	JBS
3C	JBS
3D	JBS
3E	JBS

7.0 OPCODE TABLE (Continued)

3F	JBS
40	AND DIRECT (3 OPS)
41	AND IMMEDIATE (3 OPS)
42	AND INDIRECT (3 OPS)
43	AND INDEXED (3 OPS)
44	ADD DIRECT (3 OPS)
45	ADD IMMEDIATE (3 OPS)
46	ADD INDIRECT (3 OPS)
47	ADD INDEXED (3 OPS)
48	SUB DIRECT (3 OPS)
49	SUB IMMEDIATE (3 OPS)
4A	SUB INDIRECT (3 OPS)
4B	SUB INDEXED (3 OPS)
4C	MULU DIRECT (3 OPS)
4D	MULU IMMEDIATE (3 OPS)
4E	MULU INDIRECT (3 OPS)
4F	MULU INDEXED (3 OPS)
50	ANDB DIRECT (3 OPS)
51	ANDB IMMEDIATE (3 OPS)
52	ANDB INDIRECT (3 OPS)
53	ANDB INDEXED (3 OPS)
54	ADDB DIRECT (3 OPS)
55	ADDB IMMEDIATE (3 OPS)
56	ADDB INDIRECT (3 OPS)
57	ADDB INDEXED (3 OPS)
58	SUBB DIRECT (3 OPS)
59	SUBB IMMEDIATE (3 OPS)
5A	SUBB INDIRECT (3 OPS)
5B	SUBB INDEXED (3 OPS)
5C	MULUB DIRECT (3 OPS)
5D	MULUB IMMEDIATE (3 OPS)
5E	MULUB INDIRECT (3 OPS)
5F	MULUB INDEXED (3 OPS)
60	AND DIRECT (2 OPS)
61	AND IMMEDIATE (2 OPS)
62	AND INDIRECT (2 OPS)
63	AND INDEXED (2 OPS)

64	ADD DIRECT (2 OPS)
65	ADD IMMEDIATE (2 OPS)
66	ADD INDIRECT (2 OPS)
67	ADD INDEXED (2 OPS)
68	SUB DIRECT (2 OPS)
69	SUB IMMEDIATE (2 OPS)
6A	SUB INDIRECT (2 OPS)
6B	SUB INDEXED (2 OPS)
6C	MULU DIRECT (2 OPS)
6D	MULU IMMEDIATE (2 OPS)
6E	MULU INDIRECT (2 OPS)
6F	MULU INDEXED (2 OPS)
70	ANDB DIRECT (2 OPS)
71	ANDB IMMEDIATE (2 OPS)
72	ANDB INDIRECT (2 OPS)
73	ANDB INDEXED (2 OPS)
74	ADDB DIRECT (2 OPS)
75	ADDB IMMEDIATE (2 OPS)
76	ADDB INDIRECT (2 OPS)
77	ADDB INDEXED (2 OPS)
78	SUBB DIRECT (2 OPS)
79	SUBB IMMEDIATE (2 OPS)
7A	SUBB INDIRECT (2 OPS)
7B	SUBB INDEXED (2 OPS)
7C	MULUB DIRECT (2 OPS)
7D	MULUB IMMEDIATE (2 OPS)
7E	MULUB INDIRECT (2 OPS)
7F	MULUB INDEXED (2 OPS)
80	OR DIRECT
81	OR IMMEDIATE
82	OR INDIRECT
83	OR INDEXED
84	XOR DIRECT
85	XOR IMMEDIATE
86	XOR INDIRECT
87	XOR INDEXED
88	CMP DIRECT

89	CMP IMMEDIATE
8A	CMP INDIRECT
8B	CMP INDEXED
8C	DIVU DIRECT
8D	DIVU IMMEDIATE
8E	DIVU INDIRECT
8F	DIVU INDEXED
90	ORB DIRECT
91	ORB IMMEDIATE
92	ORB INDIRECT
93	ORB INDEXED
94	XORB DIRECT
95	XORB IMMEDIATE
96	XORB INDIRECT
97	XORB INDEXED
98	CMPB DIRECT
99	CMPB IMMEDIATE
9A	CMPB INDIRECT
9B	CMPB INDEXED
9C	DIVUB DIRECT
9D	DIVUB IMMEDIATE
9E	DIVUB INDIRECT
9F	DIVUB INDEXED
A0	LD DIRECT
A1	LD IMMEDIATE
A2	LD INDIRECT
A3	LD INDEXED
A4	ADDC DIRECT
A5	ADDC IMMEDIATE
A6	ADDC INDIRECT
A7	ADDC INDEXED
A8	SUBC DIRECT
A9	SUBC IMMEDIATE
AA	SUBC INDIRECT
AB	SUBC INDEXED
AC	LDBZE DIRECT
AD	LDBZE IMMEDIATE

7.0 OPCODE TABLE (Continued)

AE	LDBZE INDIRECT
AF	LDBZE INDEXED
B0	LDB DIRECT
B1	LDB IMMEDIATE
B2	LDB INDIRECT
B3	LDB INDEXED
B4	ADDCB DIRECT
B5	ADDCB IMMEDIATE
B6	ADDCB INDIRECT
B7	ADDCB INDEXED
B8	SUBCB DIRECT
B9	SUBCB IMMEDIATE
BA	SUBCB INDIRECT
BB	SUBCB INDEXED
BC	LDBSE DIRECT
BD	LDBSE IMMEDIATE
BE	LDBSE INDIRECT
BF	LDBSE INDEXED
C0	ST DIRECT
C1	BMOV
C2	ST INDIRECT
C3	ST INDEXED
C4	STB DIRECT
C5	CMPL
C6	STB INDIRECT
C7	STB INDEXED
C8	PUSH DIRECT
C9	PUSH IMMEDIATE

CA	PUSH INDIRECT
CB	PUSH INDEXED
CC	POP DIRECT
CD	RESERVED
CE	POP INDIRECT
CF	POP INDEXED
D0	JNST
D1	JNH
D2	JGT
D3	JNC
D4	JNVT
D5	JNV
D6	JGE
D7	JNE
D8	JST
D9	JH
DA	JLE
DB	JC
DC	JVT
DD	JV
DE	JLT
DF	JE
E0	DJNZ
E1	DJNZW
E2	RESERVED
E3	BR (INDIRECT)
E4	RESERVED

E5	RESERVED
E6	RESERVED
E7	LJMP
E8	RESERVED
E9	RESERVED
EA	RESERVED
EB	RESERVED
EC	RESERVED
ED	RESERVED
EE	RESERVED
EF	LCALL
F0	RET
F1	RESERVED
F2	PUSHF
F3	POPF
F4	PUSHA
F5	POPA
F6	IDLPD
F7	TRAP
F8	CLRC
F9	SETC
FA	DI
FB	EI
FC	CLRVT
FD	NOP
FE	*DIV/DIVB/MUL/MULB
FF	RST

NOTE:
*Two Byte Instruction
RESERVED—Execution of reserved instructions will cause unimplemented opcode interrupt.

8.0 INSTRUCTION SET SUMMARY

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D ← D + A	↕	↕	↕	↕	↑	–	
ADD/ADDB	3	D ← B + A	↕	↕	↕	↕	↑	–	
ADDC/ADDCB	2	D ← D + A + C	↓	↕	↕	↕	↑	–	
SUB/SUBB	2	D ← D − A	↕	↕	↕	↕	↑	–	
SUB/SUBB	3	D ← B − A	↕	↕	↕	↕	↑	–	
SUBC/SUBCB	2	D ← D − A + C − 1	↓	↕	↕	↕	↑	–	
CMP/CMPB	2	D − A	↕	↕	↕	↕	↑	–	
MUL/MULU	2	D,D + 2 ← D × A	–	–	–	–	–	–	2
MUL/MULU	3	D,D + 2 ← B × A	–	–	–	–	–	–	2
MULB/MULUB	2	D,D + 1 ← D × A	–	–	–	–	–	–	3
MULB/MULUB	3	D,D + 1 ← B × A	–	–	–	–	–	–	3
DIVU	2	D ← (D,D + 2) /A,D + 2 ← remainder	–	–	–	↕	↑	–	2
DIVUB	2	D ← (D,D + 1) /A,D + 1 ← remainder	–	–	–	↕	↑	–	3
DIV	2	D ← (D,D + 2) /A,D + 2 ← remainder	–	–	–	↕	↑	–	
DIVB	2	D ← (D,D + 1) /A,D + 1 ← remainder	–	–	–	↕	↑	–	
AND/ANDB	2	D ← D AND A	↕	↕	0	0	–	–	
AND/ANDB	3	D ← B AND A	↕	↕	0	0	–	–	
OR/ORB	2	D ← D OR A	↕	↕	0	0	–	–	
XOR/XORB	2	D ← D (ecxl. or) A	↕	↕	0	0	–	–	
LD/LDB	2	D ← A	–	–	–	–	–	–	
ST/STB	2	A ← D	–	–	–	–	–	–	
LDBSE	2	D ← A; D + 1 ← SIGN(A)	–	–	–	–	–	–	3,4
LDBZE	2	D ← A; D + 1 ← 0	–	–	–	–	–	–	3,4
PUSH	1	SP ← SP − 2; (SP) ← A	–	–	–	–	–	–	
POP	1	A ← (SP); SP + 2	–	–	–	–	–	–	
PUSHF	0	SP ← SP − 2; (SP) ← PSW; PSW ← 0000H; I ← 0	0	0	0	0	0	0	
POPF	0	PSW ← (SP); SP ← SP + 2; I ← ↕	↕	↕	↕	↕	↕	↕	
SJMP	1	PC ← PC + 11-bit offset	–	–	–	–	–	–	5
LJMP	1	PC ← PC + 16-bit offset	–	–	–	–	–	–	5
BR[indirect]	1	PC ← (A)	–	–	–	–	–	–	
SCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 11-bit offset	–	–	–	–	–	–	5
LCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 16-bit offset	–	–	–	–	–	–	5

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
RET	0	PC ← (SP); SP ← SP + 2	–	–	–	–	–	–	
J (conditional)	1	PC ← PC + 8-bit offset (if taken)	–	–	–	–	–	–	5
JC	1	Jump if C = 1	–	–	–	–	–	–	5
JNC	1	Jump if C = 0	–	–	–	–	–	–	5
JE	1	Jump if Z = 1	–	–	–	–	–	–	5
JNE	1	Jump if Z = 0	–	–	–	–	–	–	5
JGE	1	Jump if N = 0	–	–	–	–	–	–	5
JLT	1	Jump if N = 1	–	–	–	–	–	–	5
JGT	1	Jump if N = 0 and Z = 0	–	–	–	–	–	–	5
JLE	1	Jump if N = 1 or Z = 1	–	–	–	–	–	–	5
JH	1	Jump if C = 1 and Z = 0	–	–	–	–	–	–	5
JNH	1	Jump if C = 0 or Z = 1	–	–	–	–	–	–	5
JV	1	Jump if V = 1	–	–	–	–	–	–	5
JNV	1	Jump if V = 0	–	–	–	–	–	–	5
JVT	1	Jump if VT = 1; Clear VT	–	–	–	–	0	–	5
JNVT	1	Jump if VT = 0; Clear VT	–	–	–	–	0	–	5
JST	1	Jump if ST = 1	–	–	–	–	–	–	5
JNST	1	Jump if ST = 0	–	–	–	–	–	–	5
JBS	3	Jump if Specified Bit = 1	–	–	–	–	–	–	5,6
JBC	3	Jump if Specified Bit = 0	–	–	–	–	–	–	5,6
DJNZ/ DJNZW	1	D ← D − 1; If D ≠ 0 then PC ← PC + 8-bit offset	–	–	–	–	–	–	5 10
DEC/DECB	1	D ← D − 1	↕	↕	↕	↕	↑	–	
NEG/NEGB	1	D ← 0 − D	↕	↕	↕	↕	↑	–	
INC/INCB	1	D ← D + 1	↕	↕	↕	↕	↑	–	
EXT	1	D ← D; D + 2 ← Sign (D)	↕	↕	0	0	–	–	2
EXTB	1	D ← D; D + 1 ← Sign (D)	↕	↕	0	0	–	–	3
NOT/NOTB	1	D ← Logical Not (D)	↕	↕	0	0	–	–	
CLR/CLRB	1	D ← 0	1	0	0	0	–	–	
SHL/SHLB/SHLL	2	C ← msb - - - - - lsb ← 0	↕	↕	↕	↕	↑	–	7
SHR/SHRB/SHRL	2	0 → msb - - - - - lsb → C	↕	↕	↕	0	–	↕	7
SHRA/SHRAB/SHRAL	2	msb → msb - - - - - lsb → C	↕	↕	↕	0	–	↕	7
SETC	0	C ← 1	–	–	1	–	–	–	
CLRC	0	C ← 0	–	–	0	–	–	–	

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8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
CLRVT	0	VT ← 0	–	–	–	–	0	–	
RST	0	PC ← 2080H	0	0	0	0	0	0	8
DI	0	Disable All Interrupts (I ← 0)	–	–	–	–	–	–	
EI	0	Enable All Interrupts (I ← 1)	–	–	–	–	–	–	
NOP	0	PC ← PC + 1	–	–	–	–	–	–	
SKIP	1	PC ← PC + 2	–	–	–	–	–	–	
NORML	2	Left shift till msb = 1; D ← shift count	↙	↙	0	–	–	–	7
TRAP	0	SP ← SP – 2; (SP) ← PC; PC ← (2010H)	–	–	–	–	–	–	9
PUSHA	1	SP ← SP-2; (SP) ← PSW; PSW ← 0000H; SP ← SP-2; (SP) ← IMASK1/WSR; IMASK1 ← 00H	0	0	0	0	0	0	
POPA	1	IMASK1/WSR ← (SP); SP ← SP+2 PSW ← (SP); SP ← SP+2	↙	↙	↙	↙	↙	↙	
IDLPD	1	IDLE MODE IF KEY=1; POWERDOWN MODE IF KEY =2; CHIP RESET OTHERWISE	–	–	–	–	–	–	
CMPL	2	D-A	↙	↙	↙	↙	↑	–	
BMOV	2	[PTR_HI]+ ← [PTR_LOW]+ ; UNTIL COUNT=0	–	–	–	–	–	–	

NOTES:
1. If the mnemonic ends in "B" a byte operation is performed, otherwise a word operation is done. Operands D, B and A must conform to the alignment rules for the required operand type. D and B are locations in the Register File; A can be located anywhere in memory.
2. D,D + 2 are consecutive WORDS in memory; D is DOUBLE-WORD aligned.
3. D,D + 1 are consecutive BYTES in memory; D is WORD aligned.
4. Changes a byte to word.
5. Offset is a 2's complement number.
6. Specified bit is one of the 2048 bits in the register file.
7. The "L" (Long) suffix indicates double-word operation.
8. Initiates a Reset by pulling $\overline{\text{RESET}}$ low. Software should re-initialize all the necessary registers with code starting at 2080H.
9. The assembler will not accept this mnemonic.
10. The DJNZW instruction is not guaranteed to work.

9.0 INSTRUCTION LENGTH/OPCODE

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL(1)	A-INC(1)	SHORT(1)	LONG(1)
ADD (3-op)	4/44	5/45	4/46	4/46	5/47	6/47
SUB (3-op)	4/48	5/49	4/4A	4/4A	5/4B	6/4B
ADD (2-op)	3/64	4/65	3/66	3/66	4/67	5/67
SUB (2-op)	3/68	4/69	3/6A	3/6A	4/6B	5/6B
ADDC	3/A4	4/A5	3/A6	3/A6	4/A7	5/A7
SUBC	3/A8	4/A9	3/AA	3/AA	4/AB	5/AB
CMP	3/88	4/89	3/8A	3/8A	4/8B	5/8B
ADDB (3-op)	4/54	4/55	4/56	4/56	5/57	6/57
SUBB (3-op)	4/58	4/59	4/5A	4/5A	5/5B	6/5B
ADDB (2-op)	3/74	3/75	3/76	3/76	4/77	5/77
SUBB (2-op)	3/78	3/79	3/7A	3/7A	4/7B	5/7B
ADDCB	3/B4	3/B5	3/B6	3/B6	4/B7	5/B7
SUBCB	3/B8	3/B9	3/BA	3/BA	4/BB	5/BB
CMPB	3/98	3/99	3/9A	3/9A	4/9B	5/9B
MUL (3-op)	5/(2)	6/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULU (3-op)	4/4C	5/4D	4/4E	4/4E	5/4F	6/4F
MUL (2-op)	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULU (2-op)	3/6C	4/6D	3/6E	3/6E	4/6F	5/6F
DIV	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVU	3/8C	4/8D	3/8E	3/8E	4/8F	5/8F
MULB (3-op)	5/(2)	5/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULUB (3-op)	4/5C	4/5D	4/5E	4/5E	5/5F	6/5F
MULB (2-op)	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULUB (2-op)	3/7C	3/7D	3/7E	3/7E	4/7F	5/7F
DIVB	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVUB	3/9C	3/9D	3/9E	3/9E	4/9F	5/9F
AND (3-op)	4/40	5/41	4/42	4/42	5/43	6/43
AND (2-op)	3/60	4/61	3/62	3/62	4/63	5/63
OR (2-op)	3/80	4/81	3/82	3/82	4/83	5/83
XOR	3/84	4/85	3/86	3/86	4/87	5/87
ANDB (3-op)	4/50	4/51	4/52	4/52	5/53	5/53
ANDB (2-op)	3/70	3/71	3/72	3/72	4/73	4/73
ORB (2-op)	3/90	3/91	3/92	3/92	4/93	5/93
XORB	3/94	3/95	3/96	3/96	4/97	5/97
PUSH	2/C8	3/C9	2/CA	2/CA	3/CB	4/CB
POP	2/CC	—	2/CE	2/CE	3/CF	4/CF

9.0 INSTRUCTION LENGTH/OPCODE (Continued)

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL	A-INC	SHORT	LONG
LD	3/A0	4/A1	3/A2	3/A2	4/A3	5/A3
LDB	3/B0	3/B1	3/B2	3/B2	4/B3	5/B3
ST	3/C0	—	3/C2	3/C2	4/C3	5/C3
STB	3/C4	—	3/C6	3/C6	4/C7	5/C7
LDBSE	3/BC	3/BD	3/BE	3/BE	4/BF	5/BF
LBSZE	3/AC	3/AD	3/AE	3/AE	4/AF	5/AF

Mnemonic	Length/Opcode
PUSHF	1/F2
POPF	1/F3
PUSHA	1/F4
POPA	1/F5
TRAP	1/F7
LCALL	3/EF
SCALL	2/28–2F(3)
RET	1/F0
LJMP	3/E7
SJMP	2/20–27(3)
BR[ ]	2/E3
JNST	1/D0
JST	1/D8
JNH	1/D1
JH	1/D9
JGT	1/D2
JLE	1/DA
JNC	1/B3
JC	1/D8
JNVT	1/D4
JVT	1/DC
JNV	1/D5
JV	1/DD
JGE	1/D6
JLT	1/DE
JNE	1/D7
JE	1/DF
JBC	3/30–37
JBS	3/38–3F

Mnemonic	Length/Opcode
DJNZ	3/E0
DJNZW	3/E1(4)
NORML	3/0F
SHRL	3/0C
SHLL	3/0D
SHRAL	3/0E
SHR	3/08
SHRB	3/18
SHL	3/09
SHLB	3/19
SHRA	3/0A
SHRAB	3/1A
CLRC	1/F8
SETC	1/F9
DI	1/FA
EI	1/FB
CLRVT	1/FC
NOP	1/FD
RST	1/FF
SKIP	2/00
IDLPD	1/F6
BMOV	3/C1

NOTES:
1. Indirect and indirect + share the same opcodes, as do short and long indexed opcodes. If the second byte is even, use indirect or short indexed. If odd, use indirect or long indexed.
2. The opcodes for signed multiply and divide are the unsigned opcode with an "FE" prefix.
3. The 3 least significant bits of the opcode are concatenated with the 8 bits to form an 11-bit, 2's complement offset.
4. The DJNZW instruction is not guaranteed to work.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES)

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL*	A-INC*	SHORT*	LONG*
ADD (3-op)	5	6	7/10	8/11	7/10	8/11
SUB (3-op)	5	6	7/10	8/11	7/10	8/11
ADD (2-op)	4	5	6/8	7/9	6/8	7/9
SUB (2-op)	4	5	6/8	7/9	6/8	7/9
ADDC	4	5	6/8	7/9	6/8	7/9
SUBC	4	5	6/8	7/9	6/8	7/9
CMP	4	5	6/8	7/9	6/8	7/9
ADDB (3-op)	5	5	7/10	8/11	7/10	8/11
SUBB (3-op)	5	5	7/10	8/11	7/10	8/11
ADDB (2-op)	4	4	6/8	7/9	6/8	7/9
SUBB (2-op)	4	4	6/8	7/9	6/8	7/9
ADDCB	4	4	6/8	7/9	6/8	7/9
SUBCB	4	4	6/8	7/9	6/8	7/9
CMPB	4	4	6/8	7/9	6/8	7/9
MUL (3-op)	16	17	18/21	19/22	19/22	20/23
MULU (3-op)	14	15	16/19	17/19	17/20	18/21
MUL (2-op)	16	17	18/21	19/22	19/22	20/23
MULU (2-op)	14	15	16/19	17/19	17/20	18/21
DIV	26	27	28/31	29/32	29/32	30/33
DIVU	24	25	26/29	27/30	27/30	28/31
MULB (3-op)	12	12	14/17	15/18	15/18	16/19
MULUB (3-op)	10	10	12/15	12/16	12/16	14/17
MULB (2-op)	12	12	14/17	15/18	15/18	16/19
MULUB (2-op)	10	10	12/15	13/15	12/16	14/17
DIVB	18	18	20/23	21/24	21/24	22/25
DIVUB	16	16	18/21	19/22	19/22	20/23
AND (3-op)	5	6	7/10	8/11	7/10	8/11
AND (2-op)	4	5	6/8	7/9	6/8	7/9
OR (2-op)	4	5	6/8	7/9	6/8	7/9
XOR	4	5	6/8	7/9	6/8	7/9
ANDB (3-op)	5	5	7/10	8/11	7/10	8/11
ANDB (2-op)	4	4	6/8	7/9	6/8	7/9
ORB (2-op)	4	4	6/8	7/9	6/8	7/9
XORB	4	4	6/8	7/9	6/8	7/9
LD, LDB	4, 4	5, 4	5/8	6/8	6/9	7/10
ST, STB	4, 4	–	5/8	6/9	6/9	7/10
LDBSE	4	4	5/8	6/8	6/9	7/10
LDBZE	4	4	5/8	6/8	6/9	7/10
BMOV	internal/internal: 6 + 8 per word external/internal: 6 + 11 per word external/external: 6 + 14 per word					
PUSH (int stack)	6	7	9/12	10/13	10/13	11/14
POP (int stack)	8	–	10/12	11/13	11/13	12/14
PUSH (ext stack)	8	9	11/14	12/15	12/15	13/16
POP (ext stack)	11	–	13/15	14/16	14/16	15/17

*Times for operands as: SFRs and internal RAM (0–1FFH)/memory controller (200H–0FFFFH)

NOTE:
1. Execution times for memory controller references may be one to two states higher depending on the number of bytes in the prefetch queue. Internal stack is 200H–1FFH and external stack is 200H–0FFFFH.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

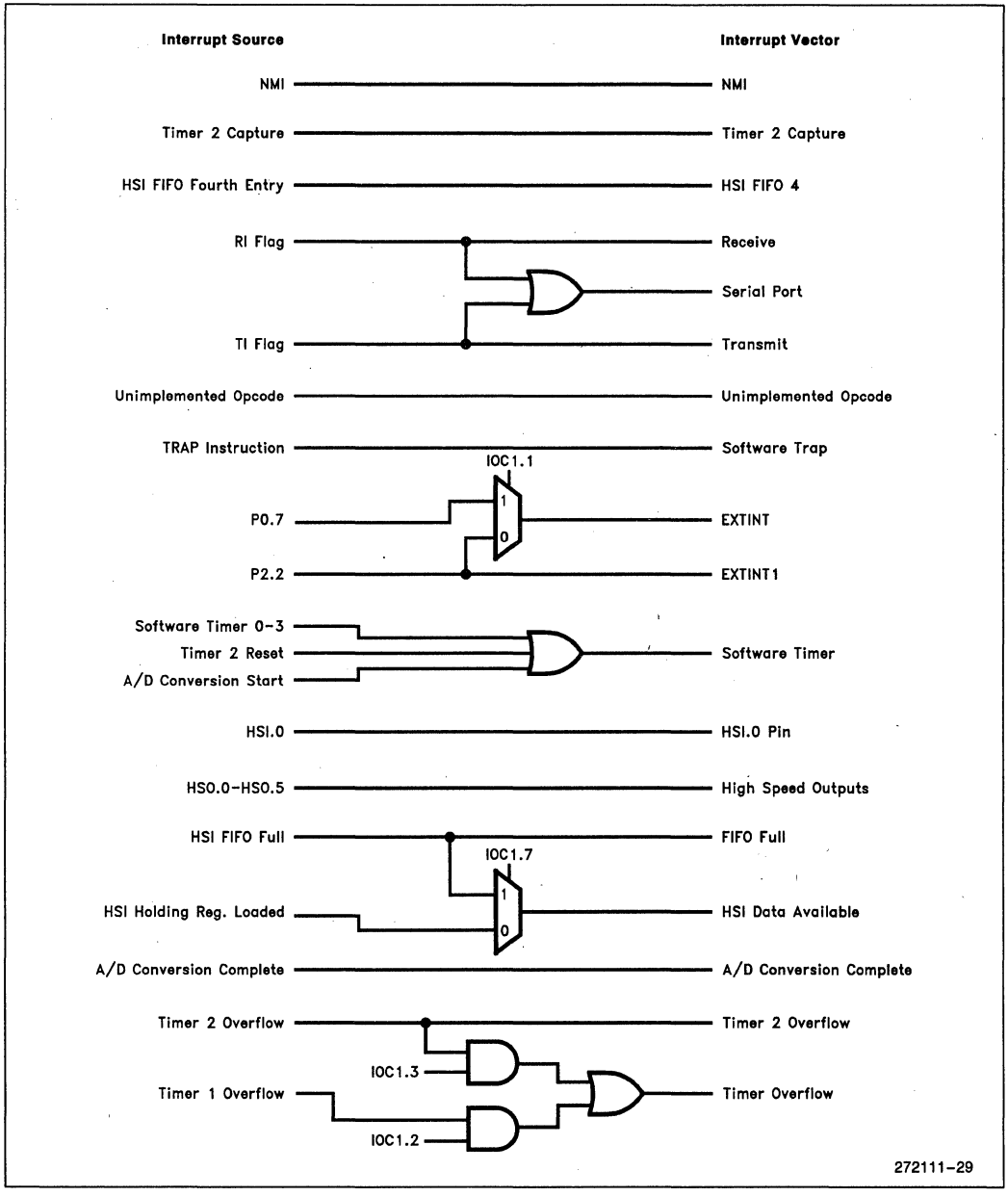
MNEMONIC		MNEMONIC	
PUSHF (int stack)	6	PUSHF (ext stack)	8
POPF (int stack)	7	POPF (ext stack)	10
PUSHA (int stack)	12	PUSHA (ext stack)	18
POPA (int stack)	12	POPA (ext stack)	18
TRAP (int stack)	16	TRAP (ext stack)	18
LCALL (int stack)	11	LCALL (ext stack)	13
SCALL (int stack)	11	SCALL (ext stack)	13
RET (int stack)	11	RET (ext stack)	14
CMPL	7	DEC/DECB	3
CLR/CLRB	3	EXT/EXTB	4
NOT/NOTB	3	INC/INCB	3
NEG/NEGB	3		
LJMP	7		
SJMP	7		
BR [indirect]	7		
JNST, JST	4/8 jump not taken/jump taken		
JNH, JH	4/8 jump not taken/jump taken		
JGT, JLE	4/8 jump not taken/jump taken		
JNC, JC	4/8 jump not taken/jump taken		
JNVT, JVT	4/8 jump not taken/jump taken		
JNV, JV	4/8 jump not taken/jump taken		
JGE, JLT	4/8 jump not taken/jump taken		
JNE, JE	4/8 jump not taken/jump taken		
JBC, JBS	5/9 jump not taken/jump taken		
DJNZ	5/9 jump not taken/jump taken		
DJNZW (Note 1)	5/9 jump not taken/jump taken		
NORML	8 + 1 per shift (9 for 0 shift)		
SHRL	7+ 1 per shift (8 for 0 shift)		
SHLL	7 + 1 per shift (8 for 0 shift)		
SHRAL	7 + 1 per shift (8 for 0 shift)		
SHR/SHRB	6 + 1 per shift (7 for 0 shift)		
SHL/SHLB	6 + 1 per shift (7 for 0 shift)		
SHRA/SHRAB	6 + 1 per shift (7 for 0 shift)		
CLRC	2		
SETC	2		
DI	2		
EI	2		
CLRVT	2		
NOP	2		
RST	15 (includes fetch of configuration byte)		
SKIP	3		
IDLPD	8/25 (proper key/improper key)		

NOTE:
1. The DJNZW instruction is not guaranteed to work.

11.0 INTERRUPT TABLE

80C196KB Interrupt Priorities

Number	Source	Vector Location	Priority
INT15	NMI	203EH	15
INT14	HSI FIFO Full	203CH	14
INT13	EXTINT1	203AH	13
INT12	TIMER2 Overflow	2038H	12
INT11	TIMER2 Capture	2036H	11
INT10	4th Entry into HSI FIFO	2034H	10
INT09	RI	2032H	9
INT08	TI	2030H	8
SPECIAL	Unimplemented Opcode	2012H	N/A
SPECIAL	Trap	2010H	N/A
INT07	EXTINT	200EH	7
INT06	Serial Port	200CH	6
INT05	Software Timer	200AH	5
INT04	HSI.0 Pin	2008H	4
INT03	High Speed Outputs	2006H	3
INT02	HSI Data Available	2004H	2
INT01	A/D Conversion Complete	2002H	1
INT00	Timer Overflow	2000H	0


Interrupt Source
Interrupt Vector
NMI
NMI
Timer 2 Capture
Timer 2 Capture
HSI FIFO Fourth Entry
HSI FIFO 4
RI Flag
TI Flag
Receive
Serial Port
Transmit
Unimplemented Opcode
Unimplemented Opcode
TRAP Instruction
Software Trap
IOC1.1
P0.7
P2.2
EXTINT
EXTINT1
Software Timer 0-3
Timer 2 Reset
A/D Conversion Start
Software Timer
HSI.0
HSI.0 Pin
HSO.0-HSO.5
High Speed Outputs
HSI FIFO Full
FIFO Full
IOC1.7
HSI Holding Reg. Loaded
HSI Data Available
A/D Conversion Complete
A/D Conversion Complete
Timer 2 Overflow
Timer 2 Overflow
IOC1.3
Timer 1 Overflow
Timer Overflow
IOC1.2
272111-29

12.0 FORMULAS

Baud Rate

Asynchronous Modes 1, 2 and 3:

$$\text{BAUD\_REG} = \frac{\text{XTAL1}}{\text{Baud Rate} \times 16} - 1$$

$$\text{or} \quad \frac{\text{T2CLK}}{\text{Baud Rate} \times 8}$$

Synchronous Mode 0:

$$\text{BAUD\_REG} = \frac{\text{XTAL1}}{\text{Baud Rate} \times 2} - 1$$

$$\text{or} \quad \frac{\text{T2CLK}}{\text{Baud Rate}}$$

A/D Sample and Conversion Times

Clock Prescaler On (IOC2.4 = 0)

Convert Time: 158 States = 26.33 μs @ 12 MHz

Sample Time: 15 States = 2.50 μs @ 12 MHz

Clock Prescaler Off (IOC2.4 = 1)

Convert Time: 91 States = 22.75 μs @ 8 MHz

Sample Time: 8 States = 2.00 μs @ 8 MHz

Pulse Width Modulation (PWM)

PWM_Control = 256 × Duty Cycle

or

PWM_Control = 512 × Duty Cycle

State Time

$$1 \text{ State Time} = \frac{2}{\text{XTAL1}} = 2T_{OSC}$$

Signature Word and Voltage Levels

Description	Location	Value
Signature Word	2070H	897CH
Programming V_{CC}	2072H	040H (5.0V)
Programming V_{PP}	2073H	0A3H (12.75V)

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13.0 RESET STATUS

Pin Name Name	Multiplexed Port Pins	Value of the Pin on Reset
$\overline{\text{RESET}}$		Mid-Sized Pullup
ALE		Weak Pullup
$\overline{\text{RD}}$		Weak Pullup
$\overline{\text{BHE}}$		Weak Pullup
$\overline{\text{WR}}$		Weak Pullup
INST		Weak Pullup
$\overline{\text{EA}}$		Undefined Input*
READY		Undefined Input*
NMI		Undefined Input*
BUSWIDTH		Undefined Input*
CLKOUT		Phase 2 of Clock
System Bus	P3.0–P4.7	Weak Pullup
ACH0–7	P0.0–P0.7	Undefined Input*
PORT1	P1.0–P1.7	Weak Pullups
TXD	P2.0	Weak Pullup
RXD	P2.1	Undefined Input*
EXTINT	P2.2	Undefined Input*
T2CLK	P2.3	Undefined Input*
T2RST	P2.4	Undefined Input*
PWM	P2.5	Weak Pulldown
—	P2.6–P2.7	Weak Pullups
HSI0–HSI1		Undefined Input*
HSI2/HSO4		Undefined Input*
HSI3/HSO5		Undefined Input*
HSO0–HSO3		Weak Pulldown

Register Name	Value
AD_RESULT	7FF0H**
HSI_STATUS	x0x0x0x0B
SBUF(RX)	00H
INT_MASK	00000000B
INT_PENDING	00000000B
TIMER1	0000H
TIMER2	0000H
IOPORT1	11111111B
IOPORT2	11000001B
SP_STAT/SP_CON	00001011B
IMASK1	00000000B
IPEND1	00000000B
WSR	XXXX0000B
HSI_MODE	11111111B
IOC2	X0000000B
IOC0	000000X0B
IOC1	00100001B
PWM_CONTROL	00H
IOPORT3	11111111B
IOPORT4	11111111B
IOS0	00000000B
IOS1	00000000B
IOS2	00000000B

NOTE:
*These pins must be driven and not left floating.
**The RESET value of AD_RESULT for devices with a change indicator of "E", "F", and "G" is 7FC0H.

intel®

September 1992

8XC196KC
Quick Reference

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Order Number: 272112-002

8XC196KC Quick Reference

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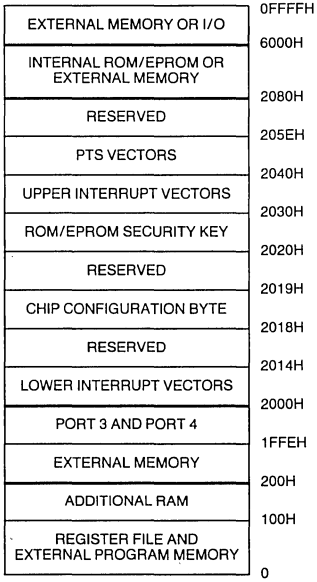
1.0 MEMORY MAP



NOTE:
Code executed in locations 0 to 1FFH will be forced external.

2.0 SFR MAP

	HWINDOW 0 when Read	HWINDOW 0 when Written	HWINDOW 1 Read/Write	HWINDOW 15 when Read	HWINDOW 15 when Written
19H	SP (HI)	SP (HI)	SP (HI)	SP (HI)	SP (HI)
18H	SP (LO)	SP (LO)	SP (LO)	SP (LO)	SP (LO)
17H	IOS2	PWM0_CONTROL	PWM2_CONTROL	PWM0_CONTROL	IOS2
16H	IOS1	IOC1	PWM1_CONTROL	IOC1	IOS1
15H	IOS0	IOC0	RESERVED	IOC0	IOS0
14H	WSR	WSR	WSR	WSR	WSR
13H	INT_MASK1	INT_MASK1	INT_MASK1	INT_MASK1	INT_MASK1
12H	INT_PEND1	INT_PEND1	INT_PEND1	INT_PEND1	INT_PEND1
11H	SP_STAT	SP_CON	RESERVED**	SP_CON	SP_STAT
10H	PORT2	PORT2	RESERVED**	RESERVED	RESERVED**
0FH	PORT1	PORT1	RESERVED**	RESERVED	RESERVED**
0EH	PORT0	BAUD_REG	RESERVED**	RESERVED	RESERVED**
0DH	TIMER2 (HI)	TIMER2 (HI)	RESERVED**	T2CAPTURE (HI)	T2CAPTURE (HI)
0CH	TIMER2 (LO)	TIMER2 (LO)	IOC3*	T2CAPTURE (LO)	T2CAPTURE (LO)
0BH	TIMER1 (HI)	IOC2	RESERVED**	IOC2	TIMER1 (HI)
0AH	TIMER1 (LO)	WATCHDOG	RESERVED**	WATCHDOG	TIMER1 (LO)
09H	INT_PEND	INT_PEND	INT_PEND	INT_PEND	INT_PEND
08H	INT_MASK	INT_MASK	INT_MASK	INT_MASK	INT_MASK
07H	SBUF (RX)	SBUF (TX)	PTSSRV (HI)	SBUF (TX)	SBUF (RX)
06H	HSI_STATUS	HSO_COMMAND	PTSSRV (LO)	HSO_COMMAND	HSI_STATUS
05H	HSI_TIME (HI)	HSO_TIME (HI)	PTSSEL(HI)	HSO_TIME (HI)	HSI_TIME (HI)
04H	HSI_TIME (LO)	HSO_TIME (LO)	PTSSEL(LO)	HSO_TIME (LO)	HSI_TIME (LO)
03H	AD_RESULT (HI)	HSI_MODE	AD_TIME	HSI_MODE	AD_RESULT (HI)
02H	AD_RESULT (LO)	AD_COMMAND	RESERVED**	AD_COMMAND	AD_RESULT (LO)
01H	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)
00H	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)

*Formerly labeled T2CONTROL or T2CNTC
**Reserved bytes must be written with zero.

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8XC196KC CHIP CONFIGURATION BYTE

CCR (2018H: Byte)

7	6	5	4	3	2	1	0
LOC1	LOC0	IRC1	IRC0	ALE	WR	BW0	PD

PD 1 = Powerdown mode enabled
0 = Powerdown mode disabled

BW0 1 = Buswidth is BUSWIDTH pin controlled
0 = Buswidth is 8-bit

WR 1 = $\overline{WR}/\overline{BHE}$
0 = $\overline{WRL}/\overline{WRH}$

ALE 1 = ALE
0 = $\overline{ADV}$

IRC0, 1 READY control. (see Table below)

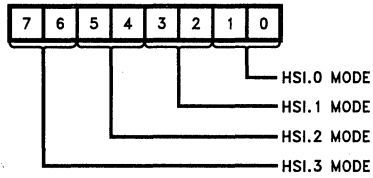
LOC0, 1 ROM, EPROM Protection. (see Table below)

IRC1	IRC0	Max Wait States
0	0	1 Wait State
0	1	2 Wait States
1	0	3 Wait States
1	1	READY Pin Controlled

LOC1	LOC0	Function
0	0	Read and Write Protected
0	1	Read Protected Only
1	0	Write Protected Only
1	1	No Protection

3.0 SFR BIT SUMMARY

HSI_MODE (03H HWIN0 Write) (03H HWIN15 Read)

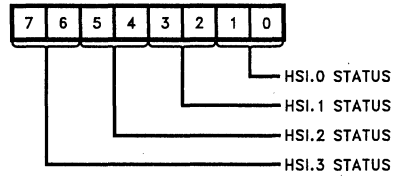


WHERE EACH 2 - BIT MODE CONTROL FIELD DEFINES ONE OF 4 POSSIBLE MODES:

00 8 POSITIVE TRANSITIONS
01 EACH POSITIVE TRANSITION
10 EACH NEGATIVE TRANSITION
11 EVERY TRANSITION (POSITIVE AND NEGATIVE)

272112-1

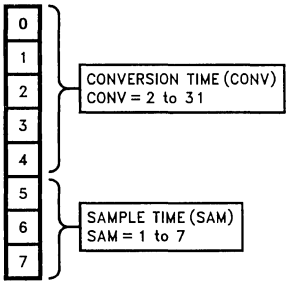
HSI_STATUS (06H HWIN0 Read) (06H HWIN15 Write)



WHERE FOR EACH 2 - BIT STATUS FIELD THE LOWER BIT INDICATES WHETHER OR NOT AN EVENT HAS OCCURRED ON THIS PIN AND THE UPPER BIT INDICATES THE CURRENT STATUS OF THE PIN.

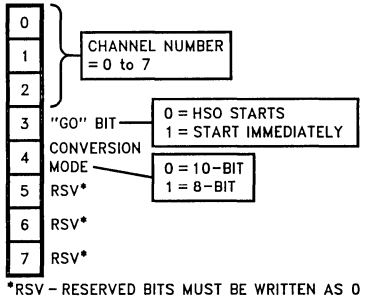
272112-2

AD_TIME (03H HWIN1 R/W)



272112-3

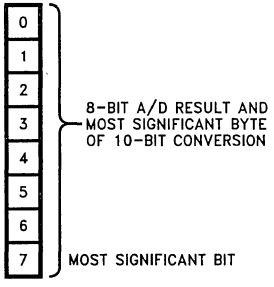
AD_COMMAND (02H HWIN0 Write) (02H HWIN15 Read)



*RSV – RESERVED BITS MUST BE WRITTEN AS 0

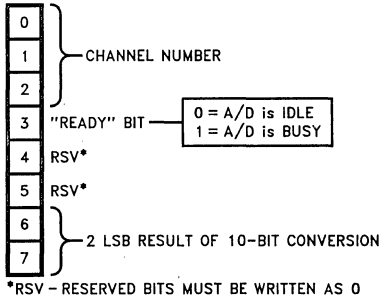
272112-4

AD_RESULT (HI) (03H HWIN0 Read) (03H HWIN15 Write)



272112-5

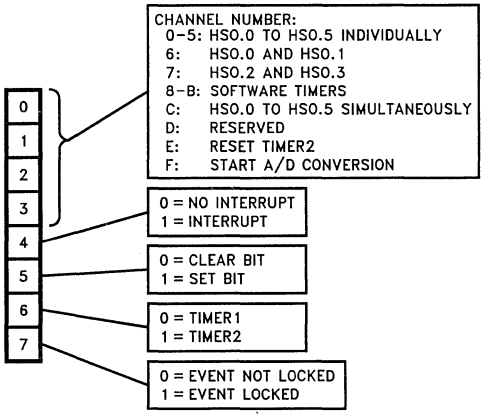
AD_RESULT (LO) (02H HWIN0 Read) (02H HWIN15 Write)



*RSV – RESERVED BITS MUST BE WRITTEN AS 0

272112-6

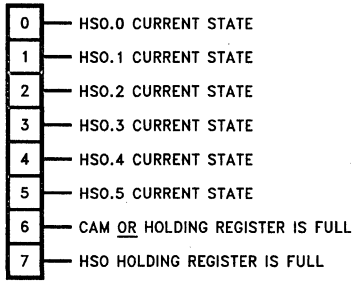
HSO_COMMAND (06H HWIN0 Write) (06H HWIN15 Read)



272112-7

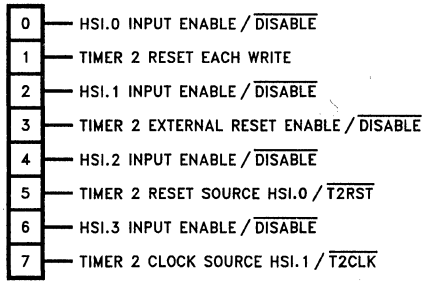
14

IOS0 (15H HWIN0 Read) (15H HWIN15 Write)



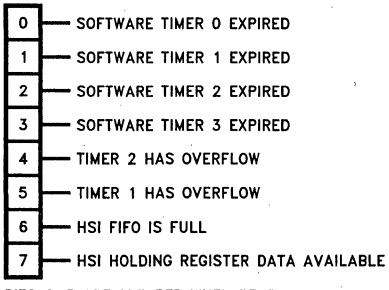
272112-8

IOC0 (15H HWIN0 Write) (15H HWIN15 Read)



272112-9

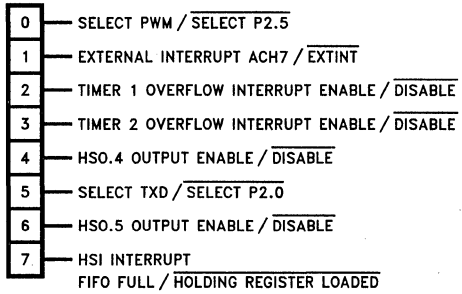
IOS1 (16H HWIN0 Read) (16H HWIN15 Write)



BITS 0-5 ARE CLEARED WHEN READ

272112-10

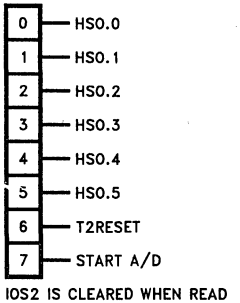
IOC1 (16H HWIN0 Write) (16H HWIN15 Read)



272112-11

IOS2 (17H HWIN0 Read) (17H HWIN15 Write)

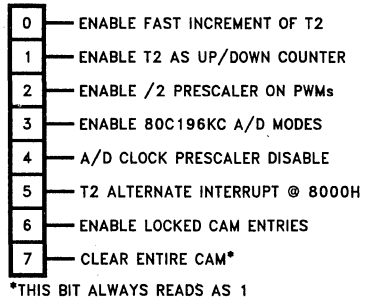
INDICATES WHICH HSO EVENT OCCURRED



IOS2 IS CLEARED WHEN READ

272112-19

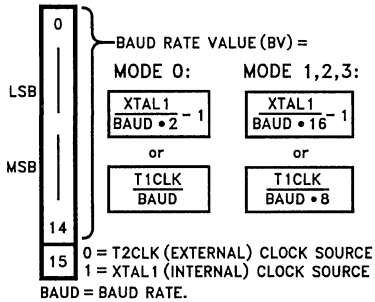
IOC2 (0BH HWIN0 Write) (0BH HWIN15 Read)



*THIS BIT ALWAYS READS AS 1

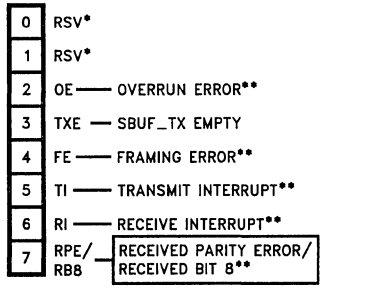
272112-18

BAUD_REG (0EH HWIN0 Write)



272112-14

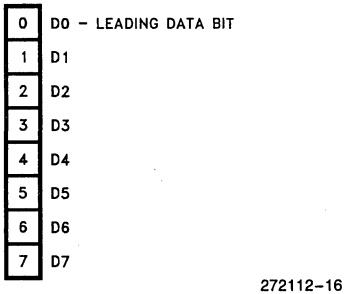
SP_STAT (11H HWIN0 Read) (11H HWIN15 Write)



*RSV – RESERVED BITS MUST BE WRITTEN AS 0
**THESE BITS CLEARED WHEN READ

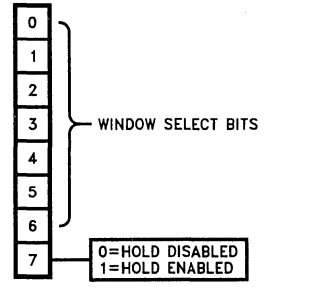
272112-15

SBUF_RX (07H HWIN0 Read) (07H HWIN15 Write)



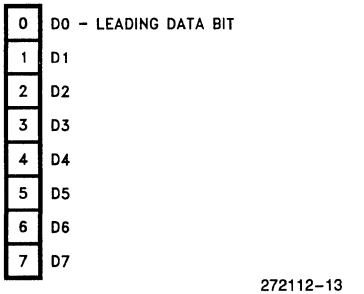
272112-16

WSR (14H all windows R/W)



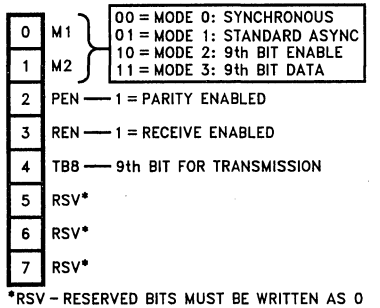
272112-17

SBUF_TX (07H HWIN0 Write) (07H HWIN15 Read)



272112-13

SP_CON (11H HWIN0 Write) (11H HWIN15 Read)



*RSV – RESERVED BITS MUST BE WRITTEN AS 0

272112-12

14

INT_MASK (08H all windows R/W)
INT_PEND (09H all windows R/W)

7	6	5	4	3	2	1	0
EXT INT	SER PORT	SOFT TIMER	HSI.0 PIN	HSO PIN	HSI DATA AVAIL	A/D DONE	TIMER OVF

272112-20

NOTE:
MASK and PEND bits share the same names

INT_MASK1 (13H all windows R/W)
INT_PEND1 (12H all windows R/W)

7	6	5	4	3	2	1	0
NMI*	FIFO FULL	EXT INT1	T2 OVF	T2 CAP	HSI4	RI	TI

* NMI IS A RESERVED BIT, MUST BE WRITTEN AS 0.

272112-21

NOTE:
MASK and PEND bits share the same names

PTSSRV (06H: Word in HWIN1 Read/Write)
PTSSEL (04H: Word in HWIN1 Read/Write)

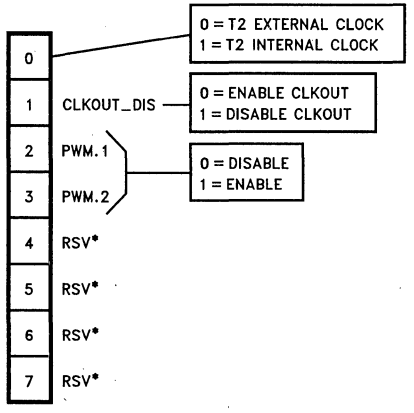
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV*	FIFO FULL	EXT INT1	T2 OVF	T2 CAP	HSI FIFO FULL	RI	TI	EXT INT	SER PORT	SOFT TIMER	HSI.1 PIN	HSO PIN	HSI DATA	A/D DONE	TIMER OVF

* RSV - RESERVED BIT MUST BE WRITTEN AS 0

272112-22

NOTE:
PTSSRV and PTSSEL bits share the same names

IOC3 (0CH HWIN1 READ/WRITE)



272112-27

NOTE:
*RSV—Reserved bits must be = 0
CLKOUT_DIS only available on C-step or later KC

4.0 8XC196KC PIN DEFINITION TABLE

Pin Name	68L PLCC	80L QFP	80L SQFP
ACH0	6	18	17
ACH1	5	17	16
ACH2	7	19	18
ACH3	4	16	15
ACH4	11	24	22
ACH5	10	23	21
ACH6	8	20	19
ACH7	9	21	20
AD0	60	2	80
AD1	59	1	79
AD2	58	80	78
AD3	57	78	77
AD4	56	77	76
AD5	55	76	75
AD6	54	74	74
AD7	53	73	73
AD8	52	72	70
AD9	51	71	69
AD10	50	70	68
AD11	49	69	67
AD12	48	68	66
AD13	47	67	65
AD14	46	66	64
AD15	45	65	63
$\overline{ADV}$	62	4	2
$\overline{AINC}$	42	61	59
ALE	62	4	2
ANGND	12	25	23
$\overline{BHE}$	41	60	58
$\overline{BREQ}$	30	46	44
BUSWIDTH	64	6	4
CPVER	33	49	47
CLKOUT	65	7	5
$\overline{EA}$	2	14	12
EXTINT	15, 9	28, 21	26
$\overline{HOLD}$	32	48	46

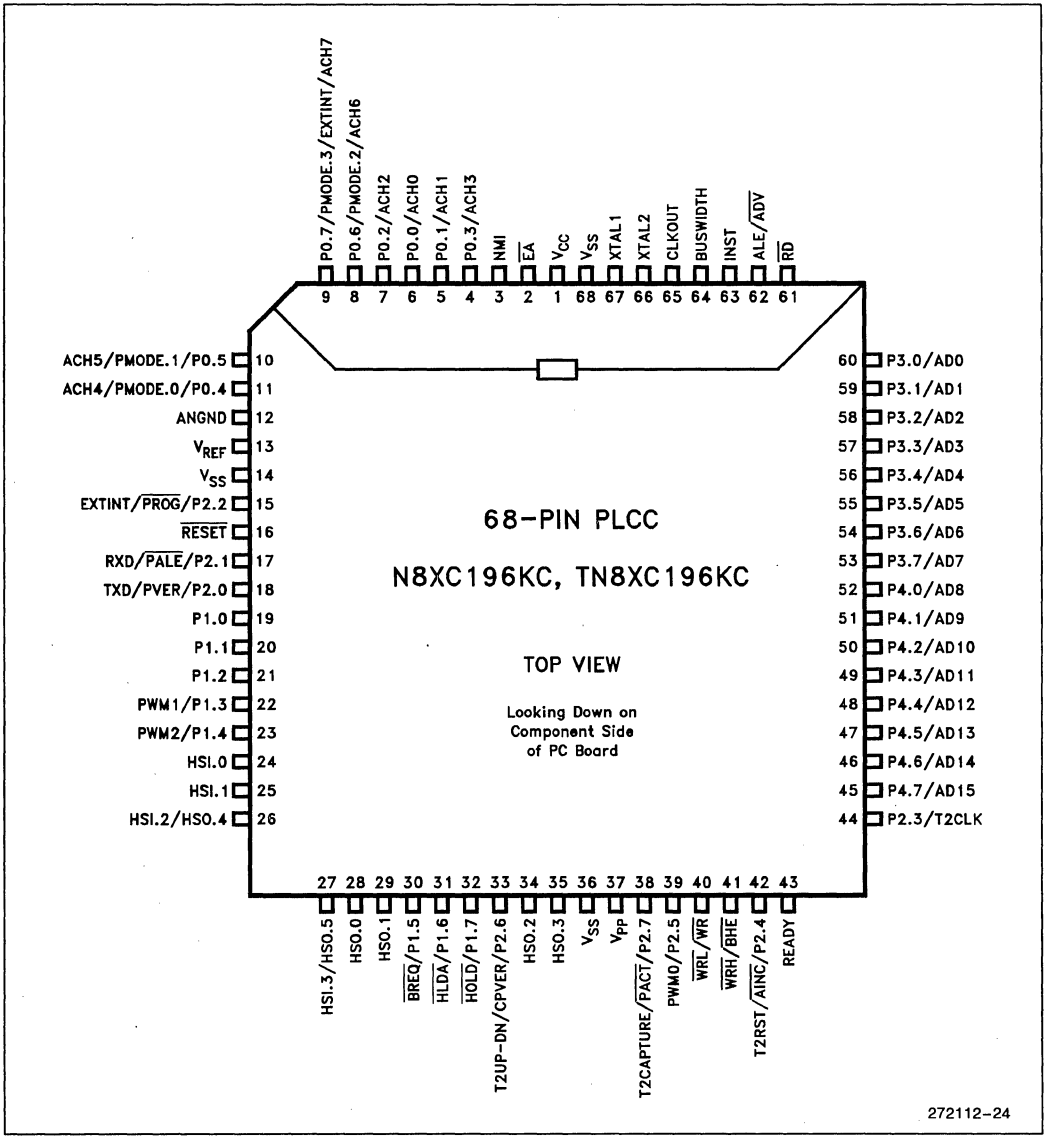
Pin Name	68L PLCC	80L QFP	80L SQFP
$\overline{HLDA}$	31	47	45
HSI.0	24	39	37
HSI.1	25	40	38
HSI.2	26	41	39
HSI.3	27	43	41
HSO.0	28	44	42
HSO.1	29	45	43
HSO.2	34	50	48
HSO.3	35	53	51
HSO.4	26	41	39
HSO.5	27	43	41
INST	63	5	3
NMI	3	15	13
P0.0	6	18	17
P0.1	5	17	16
P0.2	7	19	18
P0.3	4	16	15
P0.4	11	24	22
P0.5	10	23	21
P0.6	8	20	19
P0.7	9	21	20
P1.0	19	34	32
P1.1	20	35	33
P1.2	21	36	34
P1.3	22	37	35
P1.4	23	38	36
P1.5	30	46	44
P1.6	31	47	45
P1.7	32	48	46
P2.0	18	32	30
P2.1	17	31	29
P2.2	15	28	26
P2.3	44	64	62
P2.4	42	61	59
P2.5	39	58	56
P2.6	33	49	47

4.0 8XC196KC PIN DEFINITION TABLE (Continued)

Pin Name	68L PLCC	80L QFP	80L SQFP
P2.7	38	57	55
P3.0	60	2	80
P3.1	59	1	79
P3.2	58	80	78
P3.3	57	78	77
P3.4	56	77	76
P3.5	55	76	75
P3.6	54	74	74
P3.7	53	73	73
P4.0	52	72	70
P4.1	51	71	69
P4.2	50	70	68
P4.3	49	69	67
P4.4	48	68	66
P4.5	47	67	65
P4.6	46	66	64
P4.7	45	65	63
$\overline{\text{PACT}}$	38	57	55
$\overline{\text{PALE}}$	17	31	29
PMODE.0	11	24	22
PMODE.1	10	23	21
PMODE.2	8	20	19
PMODE.3	9	21	20
$\overline{\text{PROG}}$	15	28	26
PVER	18	32	30

Pin Name	68L PLCC	80L QFP	80L SQFP
PWM0	39	58	56
PWM1	22	37	35
PWM2	23	38	36
$\overline{\text{RD}}$	61	3	1
READY	43	62	60
$\overline{\text{RESET}}$	16	30	28
RXD	17	31	29
T2CAPTURE	38	57	55
T2CLK	44	64	62
T2RST	42	61	59
T2UP-DN	33	49	47
TXD	18	32	30
V_{CC}	1	12, 13, 29, 52, 75	10, 11, 27, 50
V_{PP}	37	56	54
V_{REF}	13	26	24
V_{SS}	14, 36, 68	10, 11, 27, 33, 42, 51, 54, 55, 63, 79	8, 9, 25, 31, 40, 49, 52, 53, 61
$\overline{\text{WR}}$	40	59	57
$\overline{\text{WRL}}$	40	59	57
$\overline{\text{WRH}}$	41	60	58
XTAL1	67	9	7
XTAL2	66	8	6

5.0 PACKAGE PIN ASSIGNMENTS



68-Lead PLCC Package Diagram

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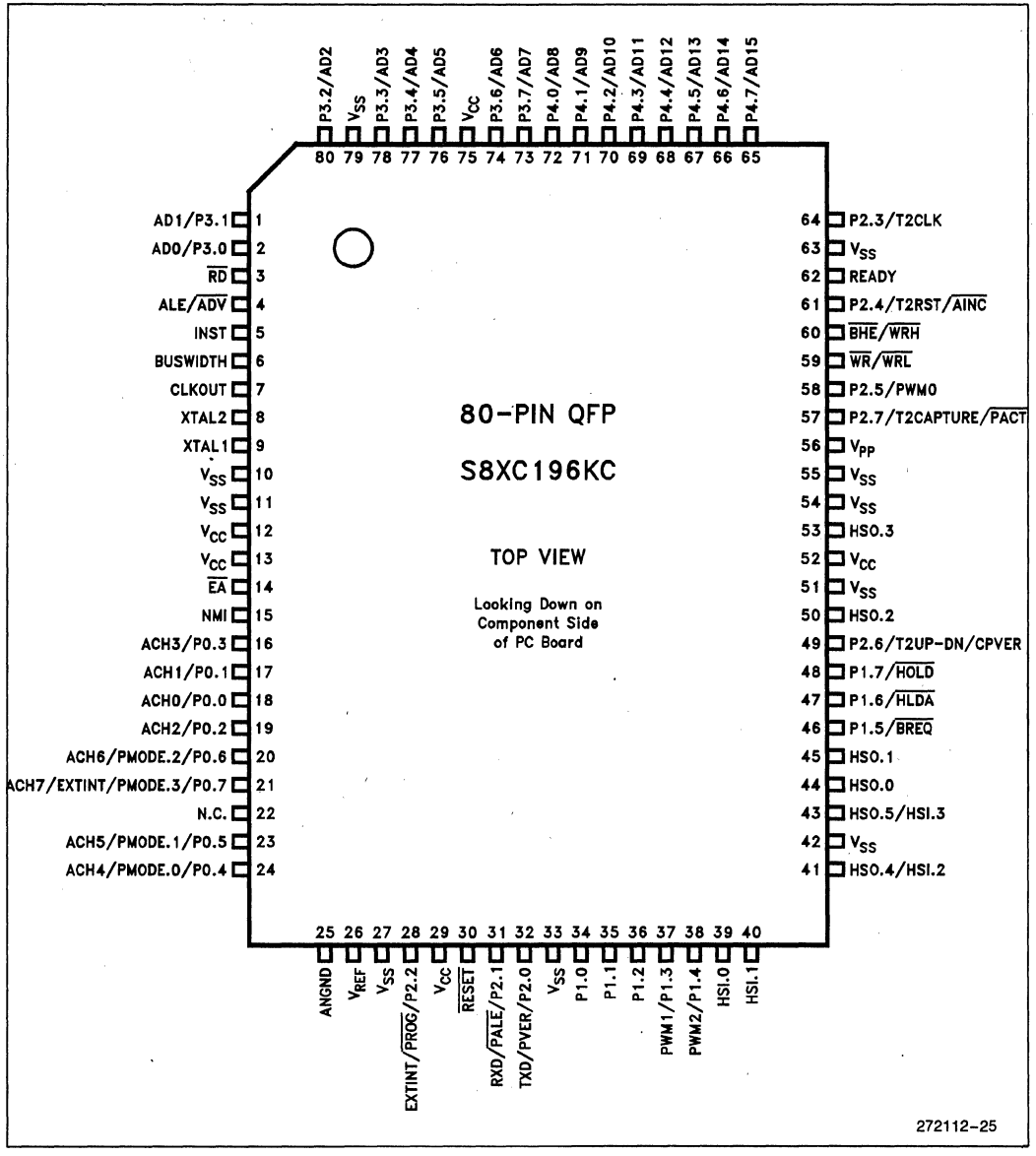


80-Lead QFP Package Diagram

6.0 PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of them must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage. Also timing pin for the return from power down circuit. Connect this pin with a 1 μF capacitor to V_{SS}. If this function is not used, connect to V_{CC}.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input and open-drain output. Hold low to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch and output low indicates a data fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{\text{BHE}}$ = 1), to the high byte only (A0 = 1, $\overline{\text{BHE}}$ = 0), or both bytes (A0 = 0, $\overline{\text{BHE}}$ = 0). If the $\overline{\text{WRH}}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle (held not ready) is available through configuration of CCR.

6.0 PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit. The HSI pins are also used as the SID in Slave Programming Mode.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. Three pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins set the Programming Mode.
Port 1	8-bit quasi-bidirectional I/O port. These pins are shared with $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and $\overline{\text{BREQ}}$.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 87C196KB.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus. Enabled by setting WSR.7.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. The TxD function is enabled by setting IOC1.5. In mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. The RxD function is enabled by setting SPCON.3. In mode 0 the pin functions as input or output data.
EXTINT	A rising edge on the EXTINT pin will generate an external interrupt. EXTINT is selected as the external interrupt source by setting IOC1.1 high.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2. The external reset function is enabled by setting IOCO.3. T2RST is enabled as the reset source by clearing IOCO.5.
PWM0-2	Port 2.5 can be enabled as a PWM output. The duty cycle of the PWM is determined by the value loaded into the PWM-CONTROL registers.
T2UPDN	The T2UPDN pin controls the direction of Timer2 as an up or down counter. The Timer2 up/down function is enabled by setting IOC2.1.
T2CAP	A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register (location 0CH in Window 15).
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PACT}}$	Programming Active. Used in the Auto Programming Mode to indicate when programming activity is complete.
PVER	Program Verification. Used in Slave Programming and Auto Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low input signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

6.0 PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
PORT 3 and 4 (During Programming)	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory.
CPVER	Cumulative Program Output Verification. Pin is high if all locations since entering a programming mode have programmed correctly.

7.0 OPCODE TABLE

00	SKIP
01	CLR
02	NOT
03	NEG
04	XCH
05	DEC
06	EXT
07	INC
08	SHR
09	SHL
0A	SHRA
0B	XCH
0C	SHRL
0D	SHLL
0E	SHRAL
0F	NORML
10	RESERVED
11	CLRB
12	NOTB
13	NEGB
14	XCHB
15	DECB
16	EXTB
17	INCB
18	SHRB
19	SHLB
1A	SHRAB
1B	XCHB
1C	RESERVED
1D	RESERVED
1E	RESERVED
1F	RESERVED
20	SJMP
21	SJMP
22	SJMP
23	SJMP
24	SJMP
25	SJMP
26	SJMP
27	SJMP
28	SCALL
29	SCALL
2A	SCALL
2B	SCALL
2C	SCALL

2D	SCALL
2E	SCALL
2F	SCALL
30	JBC
31	JBC
32	JBC
33	JBC
34	JBC
35	JBC
36	JBC
37	JBC
38	JBS
39	JBS
3A	JBS
3B	JBS
3C	JBS
3D	JBS
3E	JBS
3F	JBS
40	AND DIRECT (3 OPS)
41	AND IMMEDIATE (3 OPS)
42	AND INDIRECT (3 OPS)
43	AND INDEXED (3 OPS)
44	ADD DIRECT (3 OPS)
45	ADD IMMEDIATE (3 OPS)
46	ADD INDIRECT (3 OPS)
47	ADD INDEXED (3 OPS)
48	SUB DIRECT (3 OPS)
49	SUB IMMEDIATE (3 OPS)
4A	SUB INDIRECT (3 OPS)
4B	SUB INDEXED (3 OPS)
4C	MULU DIRECT (3 OPS)
4D	MULU IMMEDIATE (3 OPS)
4E	MULU INDIRECT (3 OPS)
4F	MULU INDEXED (3 OPS)
50	ANDB DIRECT (3 OPS)
51	ANDB IMMEDIATE (3 OPS)
52	ANDB INDIRECT (3 OPS)
53	ANDB INDEXED (3 OPS)
54	ADDB DIRECT (3 OPS)
55	ADDB IMMEDIATE (3 OPS)
56	ADDB INDIRECT (3 OPS)
57	ADDB INDEXED (3 OPS)
58	SUBB DIRECT (3 OPS)
59	SUBB IMMEDIATE (3 OPS)

5A	SUBB INDIRECT (3 OPS)
5B	SUBB INDEXED (3 OPS)
5C	MULUB DIRECT (3 OPS)
5D	MULUB IMMEDIATE (3 OPS)
5E	MULUB INDIRECT (3 OPS)
5F	MULUB INDEXED (3 OPS)
60	AND DIRECT (2 OPS)
61	AND IMMEDIATE (2 OPS)
62	AND INDIRECT (2 OPS)
62	AND INDEXED (2 OPS)
64	ADD DIRECT (2 OPS)
65	ADD IMMEDIATE (2 OPS)
66	ADD INDIRECT (2 OPS)
67	ADD INDEXED (2 OPS)
68	SUB DIRECT (2 OPS)
69	SUB IMMEDIATE (2 OPS)
6A	SUB INDIRECT (2 OPS)
6B	SUB INDEXED (2 OPS)
6C	MULU DIRECT (2 OPS)
6D	MULU IMMEDIATE (2 OPS)
6E	MULU INDIRECT (2 OPS)
6F	MULU INDEXED (2 OPS)
70	ANDB DIRECT (2 OPS)
71	ANDB IMMEDIATE (2 OPS)
72	ANDB INDIRECT (2 OPS)
73	ANDB INDEXED (2 OPS)
74	ADDB DIRECT (2 OPS)
75	ADDB IMMEDIATE (2 OPS)
76	ADDB INDIRECT (2 OPS)
77	ADDB INDEXED (2 OPS)
78	SUBB DIRECT (2 OPS)
79	SUBB IMMEDIATE (2 OPS)
7A	SUBB INDIRECT (2 OPS)
7B	SUBB INDEXED (2 OPS)
7C	MULUB DIRECT (2 OPS)
7D	MULUB IMMEDIATE (2 OPS)
7E	MULUB INDIRECT (2 OPS)
7F	MULUB INDEXED (2 OPS)
80	OR DIRECT
81	OR IMMEDIATE
82	OR INDIRECT
83	OR INDEXED
84	XOR DIRECT
85	XOR IMMEDIATE
86	XOR INDIRECT

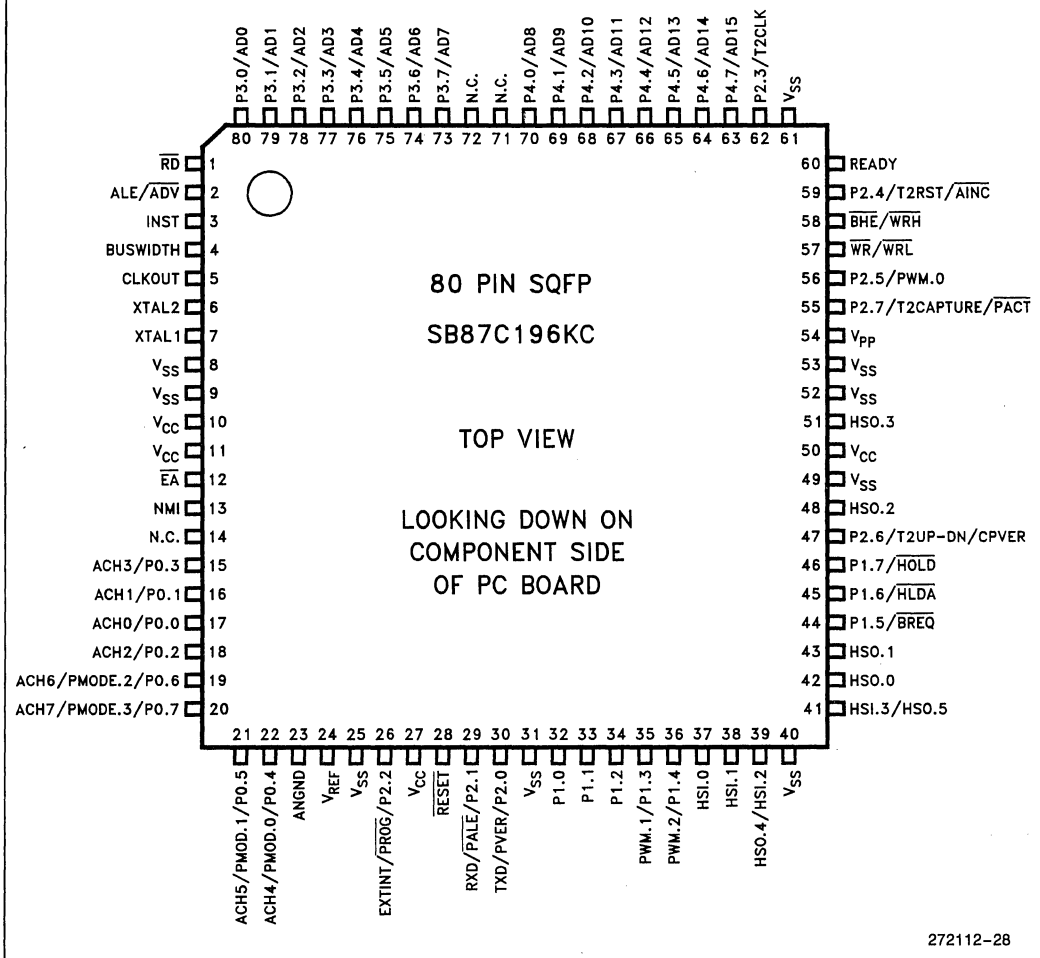
7.0 OPCODE TABLE (Continued)

87	XOR INDEXED
88	CMP DIRECT
89	CMP IMMEDIATE
8A	CMP INDIRECT
8B	CMP INDEXED
8C	DIVU DIRECT
8D	DIVU IMMEDIATE
8E	DIVU INDIRECT
8F	DIVU INDEXED
90	ORB DIRECT
91	ORB IMMEDIATE
92	ORB INDIRECT
93	ORB INDEXED
94	XORB DIRECT
95	XORB IMMEDIATE
96	XORB INDIRECT
97	XORB INDEXED
98	CMPB DIRECT
99	CMPB IMMEDIATE
9A	CMPB INDIRECT
9B	CMPB INDEXED
9C	DIVUB DIRECT
9D	DIVUB IMMEDIATE
9E	DIVUB INDIRECT
9F	DIVUB INDEXED
A0	LD DIRECT
A1	LD IMMEDIATE
A2	LD INDIRECT
A3	LD INDEXED
A4	ADDC DIRECT
A5	ADDC IMMEDIATE
A6	ADDC INDIRECT
A7	ADDC INDEXED
A8	SUBC DIRECT
A9	SUBC IMMEDIATE
AA	SUBC INDIRECT
AB	SUBC INDEXED
AC	LDBZE DIRECT
AD	LDBZE IMMEDIATE
AE	LDBZE INDIRECT
AF	LDBZE INDEXED

B0	LDB DIRECT
B1	LDB IMMEDIATE
B2	LDB INDIRECT
B3	LDB INDEXED
B4	ADDCB DIRECT
B5	ADDCB IMMEDIATE
B6	ADDCB INDIRECT
B7	ADDCB INDEXED
B8	SUBCB DIRECT
B9	SUBCB IMMEDIATE
BA	SUBCB INDIRECT
BB	SUBCB INDEXED
BC	LDBSE DIRECT
BD	LDBSE IMMEDIATE
BE	LDBSE INDIRECT
BF	LDBSE INDEXED
C0	ST DIRECT
C1	BMOV
C2	ST INDIRECT
C3	ST INDEXED
C4	STB DIRECT
C5	CMPL
C6	STB INDIRECT
C7	STB INDEXED
C8	PUSH DIRECT
C9	PUSH IMMEDIATE
CA	PUSH INDIRECT
CB	PUSH INDEXED
CC	POP DIRECT
CD	BMOVI
CE	POP INDIRECT
CF	POP INDEXED
D0	JNST
D1	JNH
D2	JGT
D3	JNC
D4	JNVT
D5	JNV
D6	JGE
D7	JNE
D8	JST

D9	JH
DA	JLE
DB	JC
DC	JVT
DD	JV
DE	JLT
DF	JE
E0	DJNZ
E1	DJNZW
E2	TIJMP
E3	BR (INDIRECT)
E4	RESERVED
E5	RESERVED
E6	RESERVED
E7	LJMP
E8	RESERVED
E9	RESERVED
EA	RESERVED
EB	RESERVED
EC	DPTS
ED	EPTS
EE	RESERVED**
EF	LCALL
F0	RET
F1	RESERVED
F2	PUSHF
F3	POPF
F4	PUSHA
F5	POPA
F6	IDLPD
F7	TRAP
F8	CLRC
F9	SETC
FA	DI
FB	EI
FC	CLRVT
FD	NOP
FE	*DIV/DIVB/MUL/MULB
FF	RST

NOTE:
*Two Byte Instruction
RESERVED—Execution of RESERVED instructions will cause unimplemented opcode interrupt.
**Opcode EE is reserved, but it does not generate an unimplemented opcode interrupt.



NOTE:
N.C. means No Connect (do not connect these pins).

80-Pin SQFP Package

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8.0 INSTRUCTION SET SUMMARY

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D ← D + A	↕	↕	↕	↕	↑	–	
ADD/ADDB	3	D ← B + A	↕	↕	↕	↕	↑	–	
ADDC/ADDCB	2	D ← D + A + C	↓	↕	↕	↕	↑	–	
SUB/SUBB	2	D ← D − A	↕	↕	↕	↕	↑	–	
SUB/SUBB	3	D ← B − A	↕	↕	↕	↕	↑	–	
SUBC/SUBCB	2	D ← D − A + C − 1	↓	↕	↕	↕	↑	–	
CMP/CMPB	2	D − A	↕	↕	↕	↕	↑	–	
MUL/MULU	2	D,D + 2 ← D × A	–	–	–	–	–	–	2
MUL/MULU	3	D,D + 2 ← B × A	–	–	–	–	–	–	2
MULB/MULUB	2	D,D + 1 ← D × A	–	–	–	–	–	–	3
MULB/MULUB	3	D,D + 1 ← B × A	–	–	–	–	–	–	3
DIVU	2	D ← (D,D + 2) /A,D + 2 ← remainder	–	–	–	↕	↑	–	2
DIVUB	2	D ← (D,D + 1) /A,D + 1 ← remainder	–	–	–	↕	↑	–	3
DIV	2	D ← (D,D + 2) /A,D + 2 ← remainder	–	–	–	↕	↑	–	
DIVB	2	D ← (D,D + 1) /A,D + 1 ← remainder	–	–	–	↕	↑	–	
AND/ANDB	2	D ← D AND A	↕	↕	0	0	–	–	
AND/ANDB	3	D ← B AND A	↕	↕	0	0	–	–	
OR/ORB	2	D ← D OR A	↕	↕	0	0	–	–	
XOR/XORB	2	D ← D (ecxl. or) A	↕	↕	0	0	–	–	
LD/LDB	2	D ← A	–	–	–	–	–	–	
ST/STB	2	A ← D	–	–	–	–	–	–	
XCH/XCHB	2	D ← A, A ← D	–	–	–	–	–	–	
LDBSE	2	D ← A; D + 1 ← SIGN(A)	–	–	–	–	–	–	3,4
LDBZE	2	D ← A; D + 1 ← 0	–	–	–	–	–	–	3,4
PUSH	1	SP ← SP − 2; (SP) ← A	–	–	–	–	–	–	
POP	1	A ← (SP); SP + 2	–	–	–	–	–	–	
PUSHF	0	SP ← SP − 2; (SP) ← PSW; PSW ← 0000H; I ← 0	0	0	0	0	0	0	
POPF	0	PSW ← (SP); SP ← SP + 2; I ← ↕	↕	↕	↕	↕	↕	↕	
SJMP	1	PC ← PC + 11-bit offset	–	–	–	–	–	–	5
LJMP	1	PC ← PC + 16-bit offset	–	–	–	–	–	–	5
BR[indirect]	1	PC ← (A)	–	–	–	–	–	–	
TIJMP	3	PC ← [A] + 2 * ([B] AND C)	–	–	–	–	–	–	
SCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 11-bit offset	–	–	–	–	–	–	5
LCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 16-bit offset	–	–	–	–	–	–	5

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
RET	0	PC ← (SP); SP ← SP + 2	–	–	–	–	–	–	
J (conditional)	1	PC ← PC + 8-bit offset (if taken)	–	–	–	–	–	–	5
JC	1	Jump if C = 1	–	–	–	–	–	–	5
JNC	1	Jump if C = 0	–	–	–	–	–	–	5
JE	1	Jump if Z = 1	–	–	–	–	–	–	5
JNE	1	Jump if Z = 0	–	–	–	–	–	–	5
JGE	1	Jump if N = 0	–	–	–	–	–	–	5
JLT	1	Jump if N = 1	–	–	–	–	–	–	5
JGT	1	Jump if N = 0 and Z = 0	–	–	–	–	–	–	5
JLE	1	Jump if N = 1 or Z = 1	–	–	–	–	–	–	5
JH	1	Jump if C = 1 and Z = 0	–	–	–	–	–	–	5
JNH	1	Jump if C = 0 or Z = 1	–	–	–	–	–	–	5
JV	1	Jump if V = 1	–	–	–	–	–	–	5
JNV	1	Jump if V = 0	–	–	–	–	–	–	5
JVT	1	Jump if VT = 1; Clear VT	–	–	–	–	0	–	5
JNVT	1	Jump if VT = 0; Clear VT	–	–	–	–	0	–	5
JST	1	Jump if ST = 1	–	–	–	–	–	–	5
JNST	1	Jump if ST = 0	–	–	–	–	–	–	5
JBS	3	Jump if Specified Bit = 1	–	–	–	–	–	–	5,6
JBC	3	Jump if Specified Bit = 0	–	–	–	–	–	–	5,6
DJNZ/ DJNZW	1	D ← D − 1; If D ≠ 0 then PC ← PC + 8-bit offset	–	–	–	–	–	–	5
DEC/DECB	1	D ← D − 1	↙	↙	↙	↙	↑	–	
NEG/NEGB	1	D ← 0 − D	↙	↙	↙	↙	↑	–	
INC/INCB	1	D ← D + 1	↙	↙	↙	↙	↑	–	
EXT	1	D ← D; D + 2 ← Sign (D)	↙	↙	0	0	–	–	2
EXTB	1	D ← D; D + 1 ← Sign (D)	↙	↙	0	0	–	–	3
NOT/NOTB	1	D ← Logical Not (D)	↙	↙	0	0	–	–	
CLR/CLRB	1	D ← 0	1	0	0	0	–	–	
SHL/SHLB/SHLL	2	C ← msb - - - - - lsb ← 0	↙	↙	↙	↙	↑	–	7
SHR/SHRB/SHRL	2	0 → msb - - - - - lsb → C	↙	↙	↙	0	–	↙	7
SHRA/SHRAB/SHRAL	2	msb → msb - - - - - lsb → C	↙	↙	↙	0	–	↙	7
SETC	0	C ← 1	–	–	1	–	–	–	
CLRC	0	C ← 0	–	–	0	–	–	–	

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8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
CLRVT	0	VT ← 0	–	–	–	–	0	–	
RST	0	PC ← 2080H	0	0	0	0	0	0	8
DI	0	Disable All Interupts (I ← 0)	–	–	–	–	–	–	
EI	0	Enable All Interupts (I ← 1)	–	–	–	–	–	–	
DPTS	0	Disable all PTS Cycles (PSE = 0)	–	–	–	–	–	–	
EPTS	0	Enable all PTS Cycles (PSE = 1)	–	–	–	–	–	–	
NOP	0	PC ← PC + 1	–	–	–	–	–	–	
SKIP	1	PC ← PC + 2	–	–	–	–	–	–	
NORML	2	Left shift till msb = 1; D ← shift count	↙	↙	0	–	–	–	7
TRAP	0	SP ← SP − 2; (SP) ← PC; PC ← (2010H)	–	–	–	–	–	–	9
PUSHA	1	SP ← SP-2; (SP) ← PSW; PSW ← 0000H; SP ← SP-2; (SP) ← IMASK1/WSR; IMASK1 ← 00H	0	0	0	0	0	0	
POPA	1	IMASK1/WSR ← (SP); SP ← SP+2 PSW ← (SP); SP ← SP+2	↙	↙	↙	↙	↙	↙	
IDLPD	1	IDLE MODE IF KEY=1; POWERDOWN MODE IF KEY =2; CHIP RESET OTHERWISE	–	–	–	–	–	–	
CMPL	2	D-A	↙	↙	↙	↙	↑	–	
BMOV, BMOVi	2	[PTR_HI]+ ← [PTR_LOW]+ ; UNTIL COUNT=0	–	–	–	–	–	–	

NOTES:
1. If the mnemonic ends in "B" a byte operation is performed, otherwise a word operation is done. Operands D, B and A must conform to the alignment rules for the required operand type. D and B are locations in the Register File; A can be located anywhere in memory.
2. D,D + 2 are consecutive WORDS in memory; D is DOUBLE-WORD aligned.
3. D,D + 1 are consecutive BYTES in memory; D is WORD aligned.
4. Changes a byte to word.
5. Offset is a 2's complement number.
6. Specified bit is one of the 2048 bits in the register file.
7. The "L" (Long) suffix indicates double-word operation.
8. Initiates a Reset by pulling $\overline{\text{RESET}}$ low. Software should re-initialize all the necessary registers with code starting at 2080H.
9. The assembler will not accept this mnemonic.

9.0 INSTRUCTION LENGTH/OPCODE

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL(1)	A-INC(1)	SHORT(1)	LONG(1)
ADD (3-op)	4/44	5/45	4/46	4/46	5/47	6/47
SUB (3-op)	4/48	5/49	4/4A	4/4A	5/4B	6/4B
ADD (2-op)	3/64	4/65	3/66	3/66	4/67	5/67
SUB (2-op)	3/68	4/69	3/6A	3/6A	4/6B	5/6B
ADDC	3/A4	4/A5	3/A6	3/A6	4/A7	5/A7
SUBC	3/A8	4/A9	3/AA	3/AA	4/AB	5/AB
CMP	3/88	4/89	3/8A	3/8A	4/8B	5/8B
ADDB (3-op)	4/54	4/55	4/56	4/56	5/57	6/57
SUBB (3-op)	4/58	4/59	4/5A	4/5A	5/5B	6/5B
ADDB (2-op)	3/74	3/75	3/76	3/76	4/77	5/77
SUBB (2-op)	3/78	3/79	3/7A	3/7A	4/7B	5/7B
ADDCB	3/B4	3/B5	3/B6	3/B6	4/B7	5/B7
SUBCB	3/B8	3/B9	3/BA	3/BA	4/BB	5/BB
CMPB	3/98	3/99	3/9A	3/9A	4/9B	5/9B
MUL (3-op)	5/(2)	6/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULU (3-op)	4/4C	5/4D	4/4E	4/4E	5/4F	6/4F
MUL (2-op)	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULU (2-op)	3/6C	4/6D	3/6E	3/6E	4/6F	5/6F
DIV	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVU	3/8C	4/8D	3/8E	3/8E	4/8F	5/8F
MULB (3-op)	5/(2)	5/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULUB (3-op)	4/5C	4/5D	4/5E	4/5E	5/5F	6/5F
MULB (2-op)	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULUB (2-op)	3/7C	3/7D	3/7E	3/7E	4/7F	5/7F
DIVB	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVUB	3/9C	3/9D	3/9E	3/9E	4/9F	5/9F
AND (3-op)	4/40	5/41	4/42	4/42	5/43	6/43
AND (2-op)	3/60	4/61	3/62	3/62	4/63	5/63
OR (2-op)	3/80	4/81	3/82	3/82	4/83	5/83
XOR	3/84	4/85	3/86	3/86	4/87	5/87
ANDB (3-op)	4/50	4/51	4/52	4/52	5/53	5/53
ANDB (2-op)	3/70	3/71	3/72	3/72	4/73	4/73
ORB (2-op)	3/90	3/91	3/92	3/92	4/93	5/93
XORB	3/94	3/95	3/96	3/96	4/97	5/97
PUSH	2/C8	3/C9	2/CA	2/CA	3/CB	4/CB
POP	2/CC	—	2/CE	2/CE	3/CF	4/CF

9.0 INSTRUCTION LENGTH/OPCODE (Continued)

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL	A-INC	SHORT	LONG
LD	3/A0	4/A1	3/A2	3/A2	4/A3	5/A3
LDB	3/B0	3/B1	3/B2	3/B2	4/B3	5/B3
ST	3/C0	—	3/C2	3/C2	4/C3	5/C3
STB	3/C4	—	3/C6	3/C6	4/C7	5/C7
XCH	3/04	—	—	—	4/0B	5/0B
XCHB	3/14	—	—	—	4/1B	5/1B
LDBSE	3/BC	3/BD	3/BE	3/BE	4/BF	5/BF
LBSZE	3/AC	3/AD	3/AE	3/AE	4/AF	5/AF

Mnemonic	Length/Opcode
PUSHF	1/F2
POPF	1/F3
PUSHA	1/F4
POPA	1/F5
TRAP	1/F7
LCALL	3/EF
SCALL	2/28–2F(3)
RET	1/F0
LJMP	3/E7
SJMP	2/20–27(3)
BR[ ]	2/E3
TIJMP	4/E2
JNST	1/D0
JST	1/D8
JNH	1/D1
JH	1/D9
JGT	1/D2
JLE	1/DA
JNC	1/B3
JC	1/D8
JNVT	1/D4
JVT	1/DC
JNV	1/D5
JV	1/DD
JGE	1/D6
JLT	1/DE
JNE	1/D7

Mnemonic	Length/Opcode
JE	1/DF
JBC	3/30–37
JBS	3/38–3F
DJNZ	3/E0
DJNZW	3/E1
NORML	3/0F
SHRL	3/0C
SHLL	3/0D
SHRAL	3/0E
SHR	3/08
SHRB	3/18
SHL	3/09
SHLB	3/19
SHRA	3/0A
SHRAB	3/1A
CLRC	1/F8
SETC	1/F9
DI	1/FA
EI	1/FB
DPTS	1/EC
EPTS	1/ED
CLRVT	1/FC
NOP	1/FD
RST	1/FF
SKIP	2/00
IDLPD	1/F6
BMOV	3/C1
BMOVi	3/CD

NOTES:
1. Indirect and indirect + share the same opcodes, as do short and long indexed opcodes. If the second byte is even, use indirect or short indexed. If odd, use indirect or long indexed.
2. The opcodes for signed multiply and divide are the unsigned opcode with an "FE" prefix.
3. The 3 least significant bits of the opcode are concatenated with the 8 bits to form an 11-bit, 2's complement offset.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES)

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL*	A-INC*	SHORT*	LONG*
ADD (3-op)	5	6	7/10	8/11	7/10	8/11
SUB (3-op)	5	6	7/10	8/11	7/10	8/11
ADD (2-op)	4	5	6/8	7/9	6/8	7/9
SUB (2-op)	4	5	6/8	7/9	6/8	7/9
ADDC	4	5	6/8	7/9	6/8	7/9
SUBC	4	5	6/8	7/9	6/8	7/9
CMP	4	5	6/8	7/9	6/8	7/9
ADDB (3-op)	5	5	7/10	8/11	7/10	8/11
SUBB (3-op)	5	5	7/10	8/11	7/10	8/11
ADDB (2-op)	4	4	6/8	7/9	6/8	7/9
SUBB (2-op)	4	4	6/8	7/9	6/8	7/9
ADDCB	4	4	6/8	7/9	6/8	7/9
SUBCB	4	4	6/8	7/9	6/8	7/9
CMPB	4	4	6/8	7/9	6/8	7/9
MUL (3-op)	16	17	18/21	19/22	19/22	20/23
MULU (3-op)	14	15	16/19	17/19	17/20	18/21
MUL (2-op)	16	17	18/21	19/22	19/22	20/23
MULU (2-op)	14	15	16/19	17/19	17/20	18/21
DIV	26	27	28/31	29/32	29/32	30/33
DIVU	24	25	26/29	27/30	27/30	28/31
MULB (3-op)	12	12	14/17	15/18	15/18	16/19
MULUB (3-op)	10	10	12/15	12/16	12/16	14/17
MULB (2-op)	12	12	14/17	15/18	15/18	16/19
MULUB (2-op)	10	10	12/15	13/15	12/16	14/17
DIVB	18	18	20/23	21/24	21/24	22/25
DIVUB	16	16	18/21	19/22	19/22	20/23
AND (3-op)	5	6	7/10	8/11	7/10	8/11
AND (2-op)	4	5	6/8	7/9	6/8	7/9
OR (2-op)	4	5	6/8	7/9	6/8	7/9
XOR	4	5	6/8	7/9	6/8	7/9
ANDB (3-op)	5	5	7/10	8/11	7/10	8/11
ANDB (2-op)	4	4	6/8	7/9	6/8	7/9
ORB (2-op)	4	4	6/8	7/9	6/8	7/9
XORB	4	4	6/8	7/9	6/8	7/9
LD, LDB	4, 4	5, 4	5/8	6/8	6/9	7/10
ST, STB	4, 4	–	5/8	6/9	6/9	7/10
XCH, XCHB	5, 5	–	–	–	8/13	9/14
LDBSE	4	4	5/8	6/8	6/9	7/10
LDBZE	4	4	5/8	6/8	6/9	7/10
BMOV	6+8 per word +3 for each memory controller reference					
BMOVi	7+8 per word + 14 for each interrupt +3 for each memory controller reference					
PUSH (int stack)	6	7	9/12	10/13	10/13	11/14
POP (int stack)	8	–	10/12	11/13	11/13	12/14
PUSH (ext stack)	8	9	11/14	12/15	12/15	13/16
POP (ext stack)	11	–	13/15	14/16	14/16	15/17

*Times for operands addressed as SFRs and internal RAM (0-1FFH)/memory controller references (200-0FFFFH)).

NOTES:
1. Execution times for memory controller references may be one to two states higher depending on the number of bytes in the prefetch queue.
2. INT stack is 0-1FFH and EXT stack is 200-0FFFFH.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

MNEMONIC		MNEMONIC	
PUSHF (int stack)	6	PUSHF (ext stack)	8
POPF (int stack)	7	POPF (ext stack)	10
PUSHA (int stack)	12	PUSHA (ext stack)	18
POPA (int stack)	12	POPA (ext stack)	18
TRAP (int stack)	16	TRAP (ext stack)	18
LCALL (int stack)	11	LCALL (ext stack)	13
SCALL (int stack)	11	SCALL (ext stack)	13
RET (int stack)	11	RET (ext stack)	14
CMPL	7	DEC/DECB	3
CLR/CLRB	3	EXT/EXTB	4
NOT/NOTB	3	INC/INCB	3
NEG/NEGB	3		
LJMP	7		
SJMP	7		
BR [indirect]	7		
TIJMP	15 + 3 for each memory controller reference		
JNST, JST	4/8 jump not taken/jump taken		
JNH, JH	4/8 jump not taken/jump taken		
JGT, JLE	4/8 jump not taken/jump taken		
JNC, JC	4/8 jump not taken/jump taken		
JNVT, JVT	4/8 jump not taken/jump taken		
JNV, JV	4/8 jump not taken/jump taken		
JGE, JLT	4/8 jump not taken/jump taken		
JNE, JE	4/8 jump not taken/jump taken		
JBC, JBS	5/9 jump not taken/jump taken		
DJNZ	5/9 jump not taken/jump taken		
DJNZW	6/10 jump not taken/jump taken		
NORML	8 + 1 per shift (9 for 0 shift)		
SHRL	7+ 1 per shift (8 for 0 shift)		
SHLL	7 + 1 per shift (8 for 0 shift)		
SHRAL	7 + 1 per shift (8 for 0 shift)		
SHR/SHRB	6 + 1 per shift (7 for 0 shift)		
SHL/SHLB	6 + 1 per shift (7 for 0 shift)		
SHRA/SHRAB	6 + 1 per shift (7 for 0 shift)		
CLRC	2		
SETC	2		
DI	2		
EI	2		
DPTS	2		
EPTS	2		
CLRVT	2		
NOP	2		
RST	20 (includes fetch of configuration byte)		
SKIP	3		
IDLPD	8/25 (proper key/improper key)		

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

PTS CYCLES	
Single Transfer	18 (+ 3 for each memory controller reference)
Block Transfer	13 (+ 7 for each transfer, 1 minimum + 3 for each memory controller reference)
A/D Mode (SFRs/internal RAM)	21
(MEMORY CONT)	25
HSI MODE (SFRs/internal RAM)	12 (+ 10 for each transfer, 1 minimum)
(MEMORY CONT)	16 (+ 10 for each transfer, 1 minimum)
HSO MODE (SFRs/internal RAM)	11 (+ 10 for each transfer, 1 minimum)
(MEMORY CONT)	15 (+ 11 for each transfer, 1 minimum)

11.0 INTERRUPT TABLE

80C196KC Interrupt Priorities

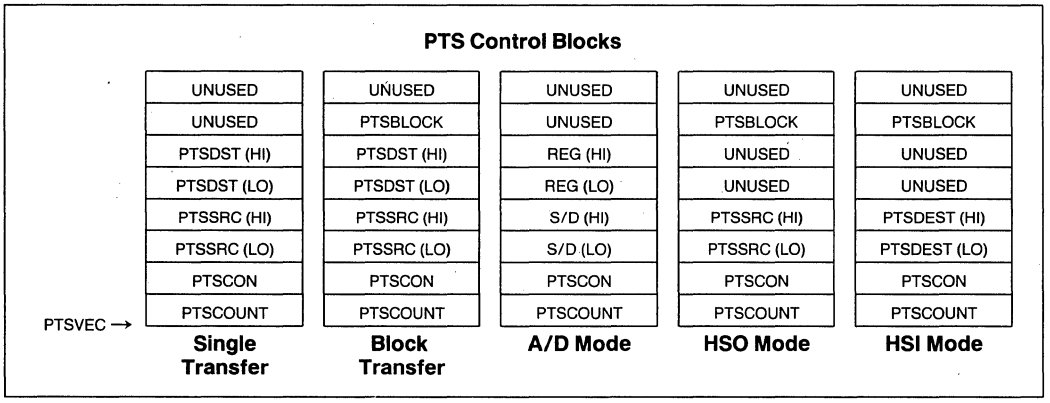
Number	Source	Vector Location	Priority
INT15	NMI	203EH	15
N/A	PTS	Table	(1, 2)
INT14	HSI FIFO Full	203CH	14
INT13	EXTINT1	203AH	13
INT12	TIMER2 Overflow	2038H	12
INT11	TIMER2 Capture	2036H	11
INT10	4th Entry into HSI FIFO	2034H	10
INT09	RI	2032H	9
INT08	TI	2030H	8
SPECIAL	Unimplemented Opcode	2012H	N/A
SPECIAL	Trap	2010H	N/A
INT07	EXTINT	200EH	7
INT06	Serial Port	200CH	6
INT05	Software Timer	200AH	5
INT04	HSI.0 Pin	2008H	4
INT03	High Speed Outputs	2006H	3
INT02	HSI Data Available	2004H	2
INT01	A/D Conversion Complete	2002H	1
INT00	Timer Overflow	2000H	0

PTS Vector Table

PTS Vector	Location
HSI FIFO Full	205CH
EXTINT1	205AH
TIMER2 Overflow	2058H
TIMER2 Capture	2056H
4th HSI FIFO Entry	2054H
RI	2052H
TI	2050H
EXTINT	204EH
Serial Port	204CH
Software Timer	204AH
HSI.0 Pin	2048H
High Speed Outputs	2046H
HSI Data Available	2044H
A/D Conversion Complete	2042H
Timer Overflow	2040H

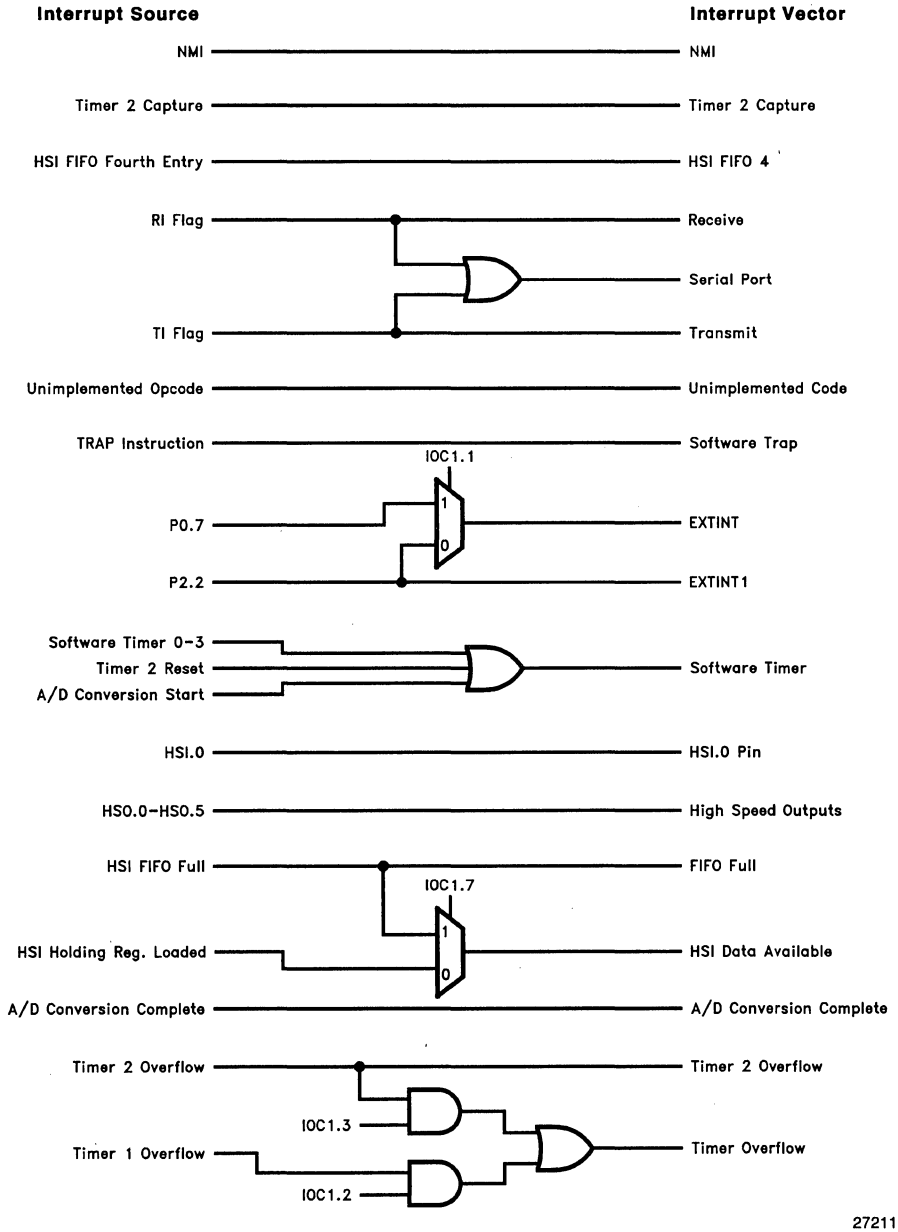
NOTES:
1. PTS interrupts have higher priority than all other interrupts except NMI.
2. PTS priorities are in the same order as conventional interrupts.

11.0 INTERRUPT TABLE (Continued)



11.0 INTERRUPT TABLE (Continued)

80C196KC Interrupt Sources



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12.0 FORMULAS

Baud Rate

Asynchronous Modes 1, 2 and 3:

$$BAUD\_REG = \frac{XTAL1}{Baud\ Rate * 16} - 1$$

or

$$\frac{T2CLK}{Baud\ Rate * 8}$$

Synchronous Mode 0:

$$BAUD\_REG = \frac{XTAL1}{Baud\ Rate * 2} - 1$$

or

$$\frac{T2CLK}{Baud\ Rate}$$

A/D Conversion

$$10\text{-Bit value} = INT\left[\frac{1023 * (V_{IN} - ANGND)}{(V_{REF} - ANGND)}\right]$$

$$8\text{-Bit value} = INT\left[\frac{255 * (V_{IN} - ANGND)}{(V_{REF} - ANGND)}\right]$$

$$SAM = \frac{(T_{SAM} * F_{OSC}) - 2}{8}$$

$$T_{SAM} = \frac{(8 * SAM) + 2}{F_{OSC}}$$

$$CONV = \frac{(T_{CONV} * F_{OSC}) + 3}{2 \times B}$$

$$T_{CONV} = \frac{(2 * B * CONV) - 3}{F_{OSC}}$$

T_{CONV} = Conversion time, μs

T_{SAMP} = Sample time, μs

SAM = Value loaded into AD_TIME bits 5, 6, 7. Must equal 1 through 7

CONV = Value loaded into AD_TIME bits 0–5. Must equal 2 through 31

XTAL1 = Processor frequency, MHz

B = 8 for 8-bit conversion

B = 10 for 10-bit conversion

Pulse Width Modulation (PWM)

PWM_CONTROL = 256 * duty cycle or

PWM_CONTROL = 512 * duty cycle

State Time

$$1\ STATE\ TIME = \frac{2}{XTAL1} = 2\ T_{OSC}$$

Signature Word and Voltage Levels

Description	Location	Value
Signature Word	70H	879CH
Programming V_{CC}	72H	040H 5.0V
Programming V_{PP}	73H	0A0H 12.50V

13.0 RESET STATUS

SFR Reset Status

Register Name	Value
AD_RESULT	7FF0H
AD_TIME	0FFH
HSI_STATUS	X0X0X0X0B
SBUF(RX)	00H
INT_MASK	00000000B
INT_PENDING	00000000B
TIMER1	0000H
TIMER2	0000H
IOPORT1	11111111B
IOPORT2	11000001B
SP_STAT/SP_CON	00001011B
IMASK1	00000000B
IPEND1	00000000B
WSR	XXXX0000B
HSI_MODE	11111111B
IOC2	X0000000B
IOC0	000000X0B
IOC1	00100001B
PWM_CONTROLS	00H
IOPORT3	11111111B
IOPORT4	11111111B
IOS0	00000000B
IOS1	00000000B
IOS2	00000000B
IOC3*	11110010B

NOTE:
*Was previously called T2CONTROL or T2CNTC.

8XC196KC Pin Reset Stats

Pin Name	Multiplexed Port Pins	Pin Status during Reset	Pin Status after Reset
ACH0–ACH7	P0.0–P0.7	Undefined Inputs(1)	Undefined Inputs(1)
PORT1	P1.0–P1.7	Weak Pull-Ups (I_{IL} Spec)	Weak Pull-Ups (I_{IL} Spec)
TXD	P2.0	Strong Pull-Up (I_{LI1} Spec)	Strongly Driven
RXD	P2.1	Undefined Input(3)	Undefined Input(3)
EXTINT	P2.2	Undefined Input(3)	Undefined Input(3)
T2CLK	P2.3	Undefined Input(3)	Undefined Input(3)
T2RST	P2.4	Undefined Input(3)	Undefined Input(3)
PWM0	P2.5	Medium Pull-Down	Strongly Driven
—	P2.6–P2.7	Weak Pull-Ups	Weak Pull-Ups
AD0–AD15	P3.0–P4.7	Weak Pull-Ups	Address/Data Bus or Open-Drain I/O(2)
HSI.0, HSI.1	—	Undefined Input(3)	Undefined Input(3)
HSI.2/HSO.4	—	Undefined Input(3)	Undefined Input(3)
HSI.3/HSO.5	—	Undefined Input(3)	Undefined Input(3)
HSO.0–HSO.3	—	Weak Pull-Down	Weak Pull-Down
ALE	—	Weak Pull-Up	Strongly Driven
$\overline{BHE}$	—	Weak Pull-Up	Strongly Driven
BUSWIDTH	—	Undefined Input(3)	Undefined Input(3)
CLKOUT	—	CLKOUT (Strongly Driven)	CLKOUT (Strongly Driven)
$\overline{EA}$	—	Undefined Input(3)	Undefined Input(3)
INST	—	Weak Pull-Down	Strongly Driven
NMI	—	Weak Pull-Down (I_{IH1} Spec)	Weak Pull-Down (I_{IH1} Spec)
$\overline{RD}$	—	Weak Pull-Up	Strongly Driven
READY	—	Undefined Input(3)	Undefined Input(3)
$\overline{RESET}$	—	Medium Pull-Up (R_{RST} Spec)	Medium Pull-Up (R_{RST} Spec)
$\overline{WR}$	—	Weak Pull-Up	Strongly Driven

NOTES:
1. These pins are allowed to float. However, it is recommended that unused pins be tied high or low.
2. The state of these pins depends on device configuration. If the address/data bus is active, the pins act as a strongly driven bus; otherwise, they act as an open-drain I/O port and are left floating.
3. These pins must be driven and not left floating. Input voltage must not exceed V_{CC} during power-up.
4. Consult the 8XC196KC/KD data sheet for specifications.

8XC196KC Pin Status Descriptions

Pin Status	Approximate Value
Weak Pull-Up	70 μA
Medium Pull-Up	1 mA
Strong Pull-Up	12 mA
Weak Pull-Down	200 μA
Medium Pull-Down	1 mA
Strongly Driven High	See V_{OH} Specification
Strongly Driven Low	See V_{OL} Specification

NOTE:
These typical maximum values are approximate; they are provided for reference only and are not guaranteed.

intel®

October 1992

8XC196KD
Quick Reference

Order Number: 272265-001

8XC196KD Quick Reference

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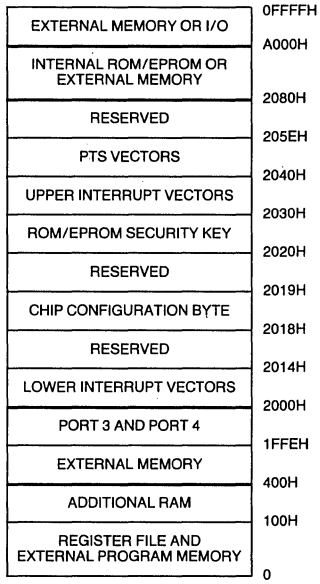
1.0 MEMORY MAP



NOTE:
Code executed in locations 0 to 1FFH will be forced external.

2.0 SFR MAP

	HWINDOW 0 when Read	HWINDOW 0 when Written	HWINDOW 1 Read/Write	HWINDOW 15 when Read	HWINDOW 15 when Written
19H	SP (HI)	SP (HI)	SP (HI)	SP (HI)	SP (HI)
18H	SP (LO)	SP (LO)	SP (LO)	SP (LO)	SP (LO)
17H	IOS2	PWM0_CONTROL	PWM2_CONTROL	PWM0_CONTROL	IOS2
16H	IOS1	IOC1	PWM1_CONTROL	IOC1	IOS1
15H	IOS0	IOC0	RESERVED	IOC0	IOS0
14H	WSR	WSR	WSR	WSR	WSR
13H	INT_MASK1	INT_MASK1	INT_MASK1	INT_MASK1	INT_MASK1
12H	INT_PEND1	INT_PEND1	INT_PEND1	INT_PEND1	INT_PEND1
11H	SP_STAT	SP_CON	RESERVED**	SP_CON	SP_STAT
10H	PORT2	PORT2	RESERVED**	RESERVED	RESERVED**
0FH	PORT1	PORT1	RESERVED**	RESERVED	RESERVED**
0EH	PORT0	BAUD_REG	RESERVED**	RESERVED	RESERVED**
0DH	TIMER2 (HI)	TIMER2 (HI)	RESERVED**	T2CAPTURE (HI)	T2CAPTURE (HI)
0CH	TIMER2 (LO)	TIMER2 (LO)	IOC3*	T2CAPTURE (LO)	T2CAPTURE (LO)
0BH	TIMER1 (HI)	IOC2	RESERVED**	IOC2	TIMER1 (HI)
0AH	TIMER1 (LO)	WATCHDOG	RESERVED**	WATCHDOG	TIMER1 (LO)
09H	INT_PEND	INT_PEND	INT_PEND	INT_PEND	INT_PEND
08H	INT_MASK	INT_MASK	INT_MASK	INT_MASK	INT_MASK
07H	SBUF (RX)	SBUF (TX)	PTSSRV (HI)	SBUF (TX)	SBUF (RX)
06H	HSI_STATUS	HSO_COMMAND	PTSSRV (LO)	HSO_COMMAND	HSI_STATUS
05H	HSI_TIME (HI)	HSO_TIME (HI)	PTSSEL(HI)	HSO_TIME (HI)	HSI_TIME (HI)
04H	HSI_TIME (LO)	HSO_TIME (LO)	PTSSEL(LO)	HSO_TIME (LO)	HSI_TIME (LO)
03H	AD_RESULT (HI)	HSI_MODE	AD_TIME	HSI_MODE	AD_RESULT (HI)
02H	AD_RESULT (LO)	AD_COMMAND	RESERVED**	AD_COMMAND	AD_RESULT (LO)
01H	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)	ZERO_REG (HI)
00H	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)	ZERO_REG (LO)

*Formerly labeled T2CONTROL or T2CNTC
**Reserved bytes must be written with zero.

8XC196KD CHIP CONFIGURATION BYTE

CCR (2018H: Byte)

7	6	5	4	3	2	1	0
LOC1	LOC0	IRC1	IRC0	ALE	WR	BW0	PD

PD 1 = Powerdown mode enabled
0 = Powerdown mode disabled

BW0 1 = Buswidth is BUSWIDTH pin controlled
0 = Buswidth is 8-bit

WR 1 = $\overline{WR}/\overline{BHE}$
0 = $\overline{WRL}/\overline{WRH}$

ALE 1 = ALE
0 = $\overline{ADV}$

IRC0, 1 READY control. (see Table below)

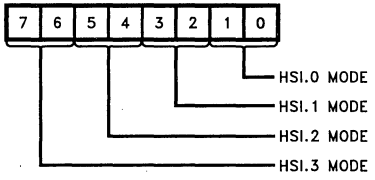
LOC0, 1 ROM, EPROM Protection. (see Table below)

IRC1	IRC0	Max Wait States
0	0	1 Wait State
0	1	2 Wait States
1	0	3 Wait States
1	1	READY Pin Controlled

LOC1	LOC0	Function
0	0	Read and Write Protected
0	1	Read Protected Only
1	0	Write Protected Only
1	1	No Protection

3.0 SFR BIT SUMMARY

HSI_MODE (03H HWIN0 Write) (03H HWIN15 Read)

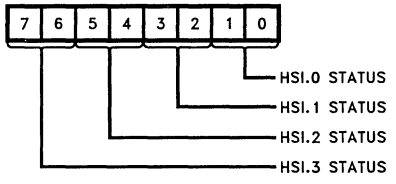


WHERE EACH 2-BIT MODE CONTROL FIELD DEFINES ONE OF 4 POSSIBLE MODES:

00 8 POSITIVE TRANSITIONS
01 EACH POSITIVE TRANSITION
10 EACH NEGATIVE TRANSITION
11 EVERY TRANSITION (POSITIVE AND NEGATIVE)

272265-1

HSI_STATUS (06H HWIN0 Read) (06H HWIN15 Write)

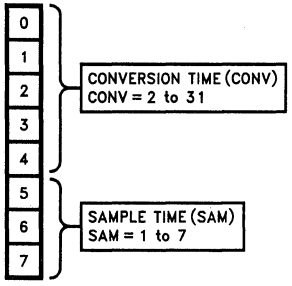


WHERE FOR EACH 2-BIT STATUS FIELD THE LOWER BIT INDICATES WHETHER OR NOT AN EVENT HAS OCCURRED ON THIS PIN AND THE UPPER BIT INDICATES THE CURRENT STATUS OF THE PIN.

272265-2

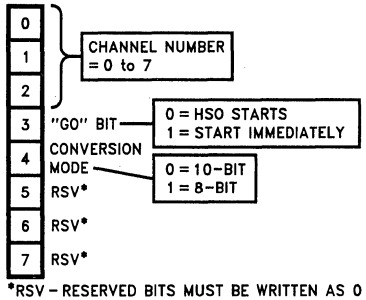
14

AD_TIME (03H HWIN1 R/W)



272265-3

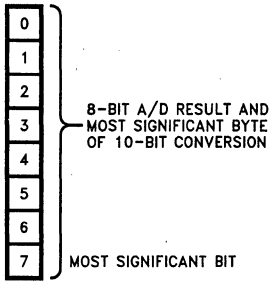
AD_COMMAND (02H HWIN0 Write)
(02H HWIN15 Read)



*RSV - RESERVED BITS MUST BE WRITTEN AS 0

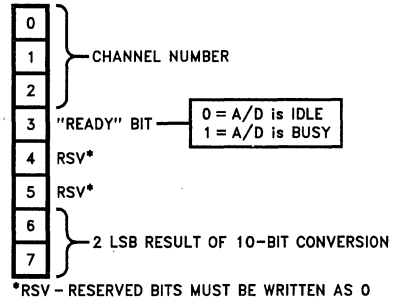
272265-4

AD_RESULT (HI) (03H HWIN0 Read)
(03H HWIN15 Write)



272265-5

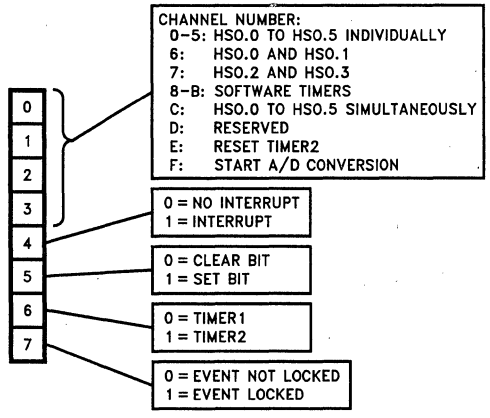
AD_RESULT (LO) (02H HWIN0 Read)
(02H HWIN15 Write)



*RSV - RESERVED BITS MUST BE WRITTEN AS 0

272265-6

HSO_COMMAND (06H HWIN0 Write)
(06H HWIN15 Read)



272265-7

IOS0 (15H HWIN0 Read) (15H HWIN15 Write)

0	HSO.0 CURRENT STATE
1	HSO.1 CURRENT STATE
2	HSO.2 CURRENT STATE
3	HSO.3 CURRENT STATE
4	HSO.4 CURRENT STATE
5	HSO.5 CURRENT STATE
6	CAM OR HOLDING REGISTER IS FULL
7	HSO HOLDING REGISTER IS FULL

272265-8

IOC0 (15H HWIN0 Write) (15H HWIN15 Read)

0	HSI.0 INPUT ENABLE / $\overline{\text{DISABLE}}$
1	TIMER 2 RESET EACH WRITE
2	HSI.1 INPUT ENABLE / $\overline{\text{DISABLE}}$
3	TIMER 2 EXTERNAL RESET ENABLE / $\overline{\text{DISABLE}}$
4	HSI.2 INPUT ENABLE / $\overline{\text{DISABLE}}$
5	TIMER 2 RESET SOURCE HSI.0 / $\overline{\text{T2RST}}$
6	HSI.3 INPUT ENABLE / $\overline{\text{DISABLE}}$
7	TIMER 2 CLOCK SOURCE HSI.1 / $\overline{\text{T2CLK}}$

272265-9

IOS1 (16H HWIN0 Read) (16H HWIN15 Write)

0	SOFTWARE TIMER 0 EXPIRED
1	SOFTWARE TIMER 1 EXPIRED
2	SOFTWARE TIMER 2 EXPIRED
3	SOFTWARE TIMER 3 EXPIRED
4	TIMER 2 HAS OVERFLOW
5	TIMER 1 HAS OVERFLOW
6	HSI FIFO IS FULL
7	HSI HOLDING REGISTER DATA AVAILABLE

BITS 0-5 ARE CLEARED WHEN READ

272265-10

IOC1 (16H HWIN0 Write) (16H HWIN15 Read)

0	SELECT PWM / $\overline{\text{SELECT P2.5}}$
1	EXTERNAL INTERRUPT ACH7 / $\overline{\text{EXTINT}}$
2	TIMER 1 OVERFLOW INTERRUPT ENABLE / $\overline{\text{DISABLE}}$
3	TIMER 2 OVERFLOW INTERRUPT ENABLE / $\overline{\text{DISABLE}}$
4	HSO.4 OUTPUT ENABLE / $\overline{\text{DISABLE}}$
5	SELECT TXD / $\overline{\text{SELECT P2.0}}$
6	HSO.5 OUTPUT ENABLE / $\overline{\text{DISABLE}}$
7	HSI INTERRUPT FIFO FULL / $\overline{\text{HOLDING REGISTER LOADED}}$

272265-11

IOS2 (17H HWIN0 Read) (17H HWIN15 Write)

INDICATES WHICH HSO EVENT OCCURRED

0	HSO.0
1	HSO.1
2	HSO.2
3	HSO.3
4	HSO.4
5	HSO.5
6	T2RESET
7	START A/D

IOS2 IS CLEARED WHEN READ

272265-12

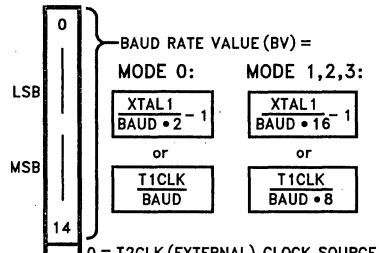
IOC2 (0BH HWIN0 Write) (0BH HWIN15 Read)

0	ENABLE FAST INCREMENT OF T2
1	ENABLE T2 AS UP/DOWN COUNTER
2	ENABLE /2 PRESCALER ON PWMs
3	ENABLE 80C196KC A/D MODES
4	A/D CLOCK PRESCALER DISABLE
5	T2 ALTERNATE INTERRUPT @ 8000H
6	ENABLE LOCKED CAM ENTRIES
7	CLEAR ENTIRE CAM*

*THIS BIT ALWAYS READS AS 1

272265-13

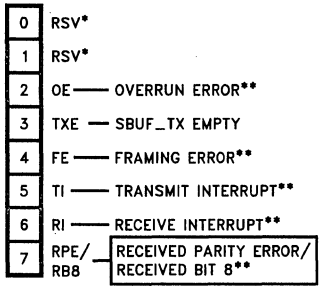
BAUD_REG (0EH HWIN0 Write)



BAUD = BAUD RATE.
MUST WRITE BV AS 2 CONSECUTIVE BYTES, LSB FIRST.

272265-14

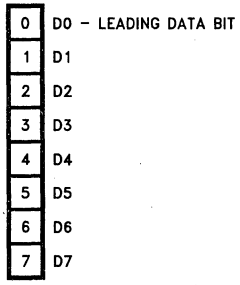
SP_STAT (11H HWIN0 Read) (11H HWIN15 Write)



*RSV - RESERVED BITS MUST BE WRITTEN AS 0
**THESE BITS CLEARED WHEN READ

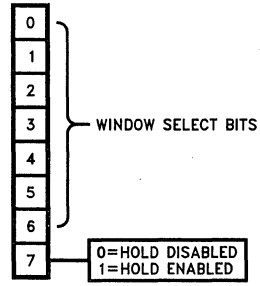
272265-15

SBUF_RX (07H HWIN0 Read) (07H HWIN15 Write)



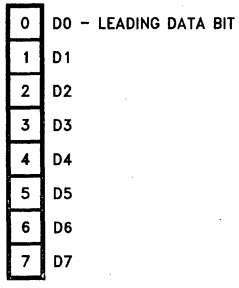
272265-16

WSR (14H all windows R/W)



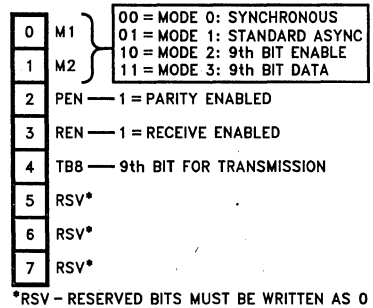
272265-17

SBUF_TX (07H HWIN0 Write) (07H HWIN15 Read)



272265-18

SP_CON (11H HWIN0 Write) (11H HWIN15 Read)



*RSV - RESERVED BITS MUST BE WRITTEN AS 0

272265-19

INT_MASK (08H all windows R/W)
INT_PEND (09H all windows R/W)

7	6	5	4	3	2	1	0
EXT INT	SER PORT	SOFT TIMER	HSI.0 PIN	HSO PIN	HSI DATA AVAIL	A/D DONE	TIMER OVF

272265-20

NOTE:
MASK and PEND bits share the same names

INT_MASK1 (13H all windows R/W)
INT_PEND1 (12H all windows R/W)

7	6	5	4	3	2	1	0
NMI*	FIFO FULL	EXT INT1	T2 OVF	T2 CAP	HSI4	RI	TI

*NMI IS A RESERVED BIT, MUST BE WRITTEN AS 0

272265-21

NOTE:
MASK and PEND bits share the same names

PTSSRV (06H: Word in HWIN1 Read/Write)
PTSSEL (04H: Word in HWIN1 Read/Write)

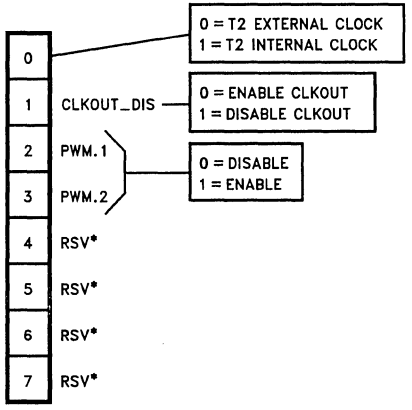
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSV*	FIFO FULL	EXT INT1	T2 OVF	T2 CAP	HSI FIFO FULL	RI	TI	EXT INT	SER PORT	SOFT TIMER	HSI.1 PIN	HSO PIN	HSI DATA	A/D DONE	TIMER OVF

*RSV - RESERVED BIT MUST BE WRITTEN AS 0

272265-22

NOTE:
PTSSRV and PTSSEL bits share the same names

IOC3 (0CH HWIN1 Read/Write)



272265-23

NOTE:
*RSV—Reserved bits must be = 0

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4.0 8XC196KD PIN DEFINITION TABLE

Pin Name	68L PLCC	80L QFP	80L SQFP
ACH0	6	18	17
ACH1	5	17	16
ACH2	7	19	18
ACH3	4	16	15
ACH4	11	24	22
ACH5	10	23	21
ACH6	8	20	19
ACH7	9	21	20
AD0	60	2	80
AD1	59	1	79
AD2	58	80	78
AD3	57	78	77
AD4	56	77	76
AD5	55	76	75
AD6	54	74	74
AD7	53	73	73
AD8	52	72	70
AD9	51	71	69
AD10	50	70	68
AD11	49	69	67
AD12	48	68	66
AD13	47	67	65
AD14	46	66	64
AD15	45	65	63
$\overline{\text{ADV}}$	62	4	2
$\overline{\text{AINC}}$	42	61	59
ALE	62	4	2
ANGND	12	25	23
$\overline{\text{BHE}}$	41	60	58
$\overline{\text{BREQ}}$	30	46	44
BUSWIDTH	64	6	4
CPVER	33	49	47
CLKOUT	65	7	5
$\overline{\text{EA}}$	2	14	12
EXTINT	15, 9	28, 21	26
$\overline{\text{HOLD}}$	32	48	46

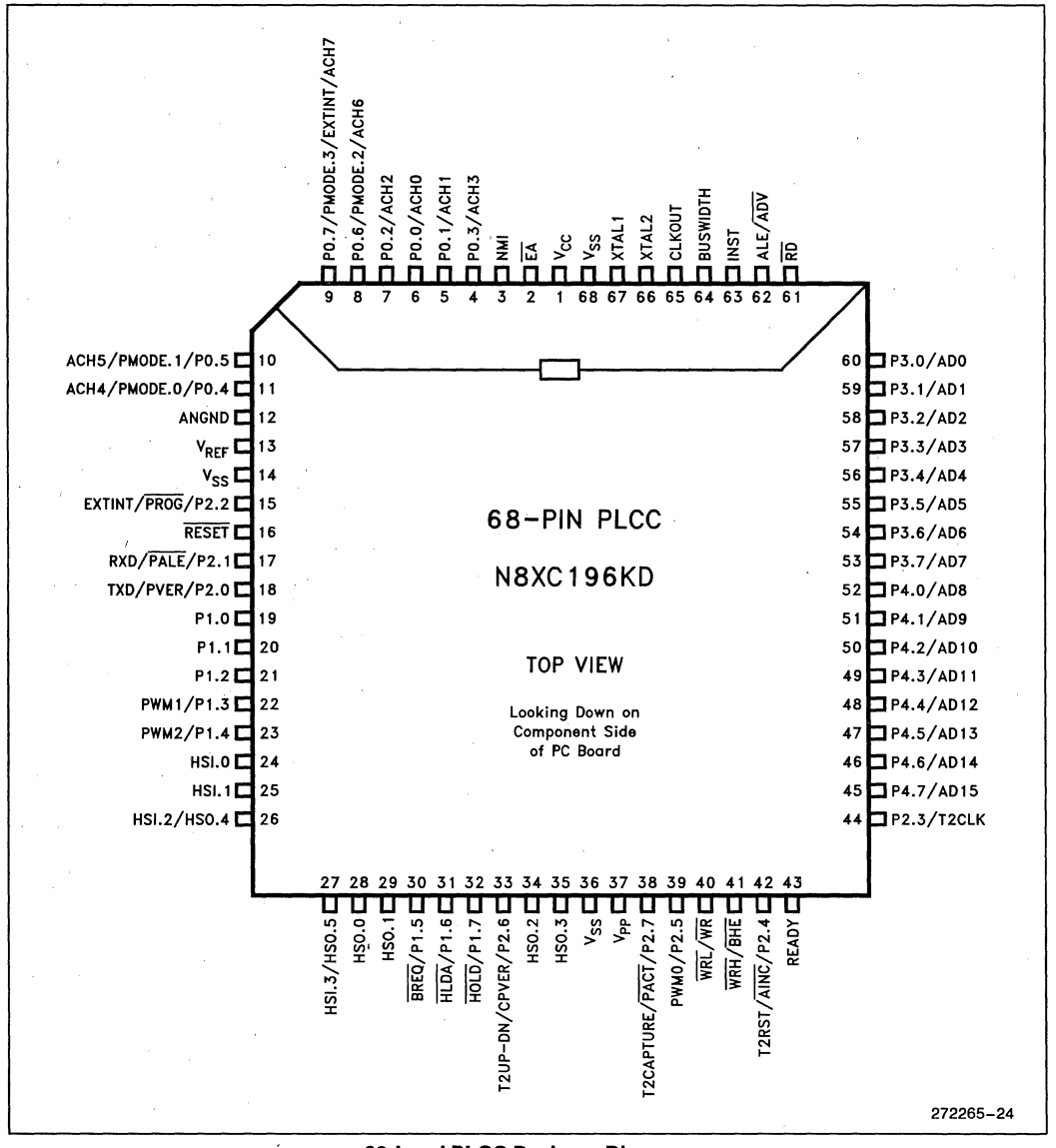
Pin Name	68L PLCC	80L QFP	80L SQFP
$\overline{\text{HLDA}}$	31	47	45
HSI.0	24	39	37
HSI.1	25	40	38
HSI.2	26	41	39
HSI.3	27	43	41
HSO.0	28	44	42
HSO.1	29	45	43
HSO.2	34	50	48
HSO.3	35	53	51
HSO.4	26	41	39
HSO.5	27	43	41
INST	63	5	3
NMI	3	15	13
P0.0	6	18	17
P0.1	5	17	16
P0.2	7	19	18
P0.3	4	16	15
P0.4	11	24	22
P0.5	10	23	21
P0.6	8	20	19
P0.7	9	21	20
P1.0	19	34	32
P1.1	20	35	33
P1.2	21	36	34
P1.3	22	37	35
P1.4	23	38	36
P1.5	30	46	44
P1.6	31	47	45
P1.7	32	48	46
P2.0	18	32	30
P2.1	17	31	29
P2.2	15	28	26
P2.3	44	64	62
P2.4	42	61	59
P2.5	39	58	56
P2.6	33	49	47

4.0 8XC196KD PIN DEFINITION TABLE (Continued)

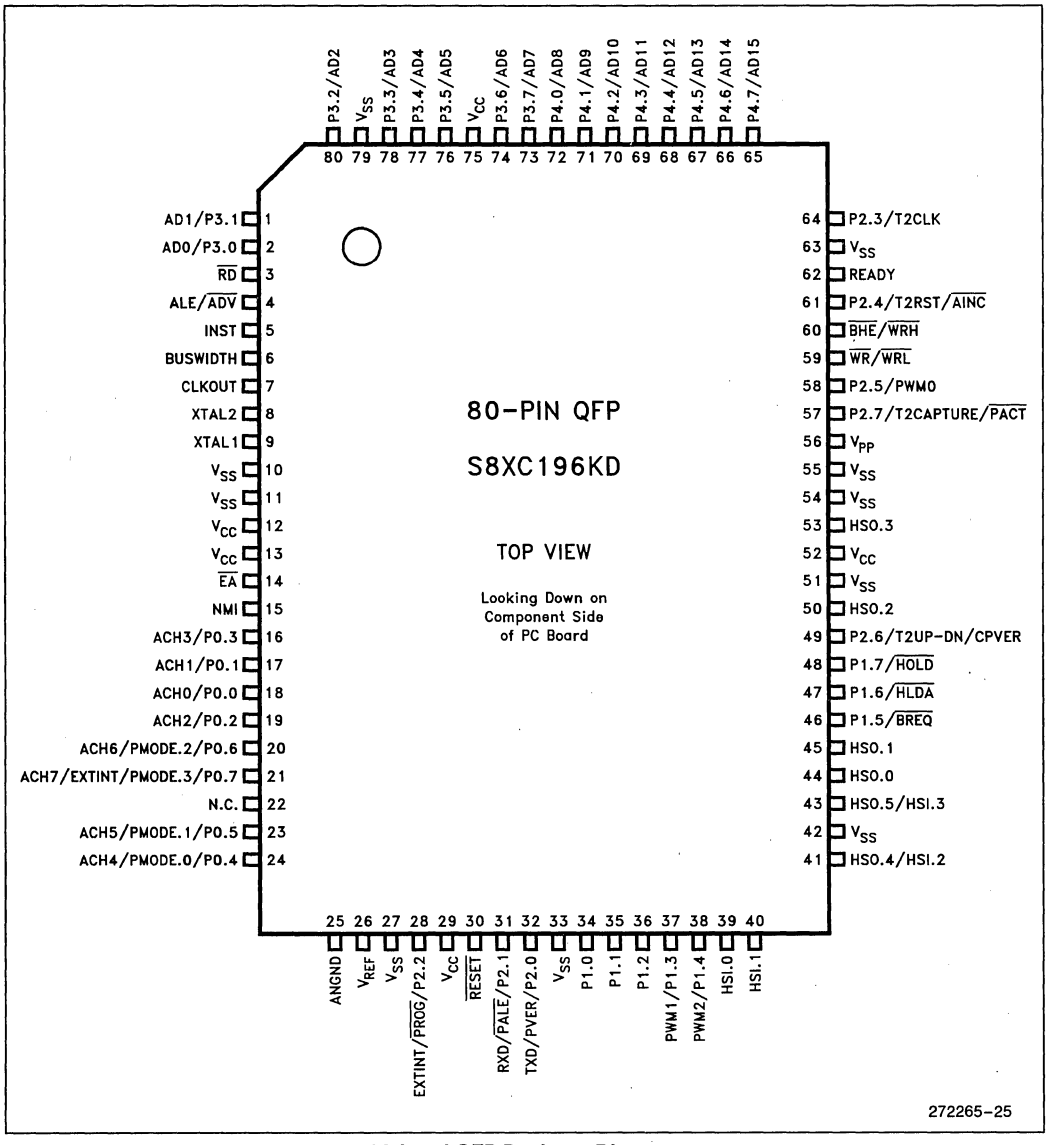
Pin Name	68L PLCC	80L QFP	80L SQFP
P2.7	38	57	55
P3.0	60	2	80
P3.1	59	1	79
P3.2	58	80	78
P3.3	57	78	77
P3.4	56	77	76
P3.5	55	76	75
P3.6	54	74	74
P3.7	53	73	73
P4.0	52	72	70
P4.1	51	71	69
P4.2	50	70	68
P4.3	49	69	67
P4.4	48	68	66
P4.5	47	67	65
P4.6	46	66	64
P4.7	45	65	63
$\overline{PACT}$	38	57	55
$\overline{PALE}$	17	31	29
PMODE.0	11	24	22
PMODE.1	10	23	21
PMODE.2	8	20	19
PMODE.3	9	21	20
$\overline{PROG}$	15	28	26
PVER	18	32	30

Pin Name	68L PLCC	80L QFP	80L SQFP
PWM0	39	58	56
PWM1	22	37	35
PWM2	23	38	36
$\overline{RD}$	61	3	1
READY	43	62	60
$\overline{RESET}$	16	30	28
RXD	17	31	29
T2CAPTURE	38	57	55
T2CLK	44	64	62
T2RST	42	61	59
T2UP-DN	33	49	47
TXD	18	32	30
V_{CC}	1	12, 13, 29, 52, 75	10, 11, 27, 50
V_{PP}	37	56	54
V_{REF}	13	26	24
V_{SS}	14, 36, 68	10, 11, 27, 33, 42, 51, 54, 55, 63, 79	8, 9, 25, 31, 40, 49, 52, 53, 61
$\overline{WR}$	40	59	57
$\overline{WRL}$	40	59	57
$\overline{WRH}$	41	60	58
XTAL1	67	9	7
XTAL2	66	8	6

5.0 PACKAGE PIN ASSIGNMENTS



68-Lead PLCC Package Diagram



80-Lead QFP Package Diagram

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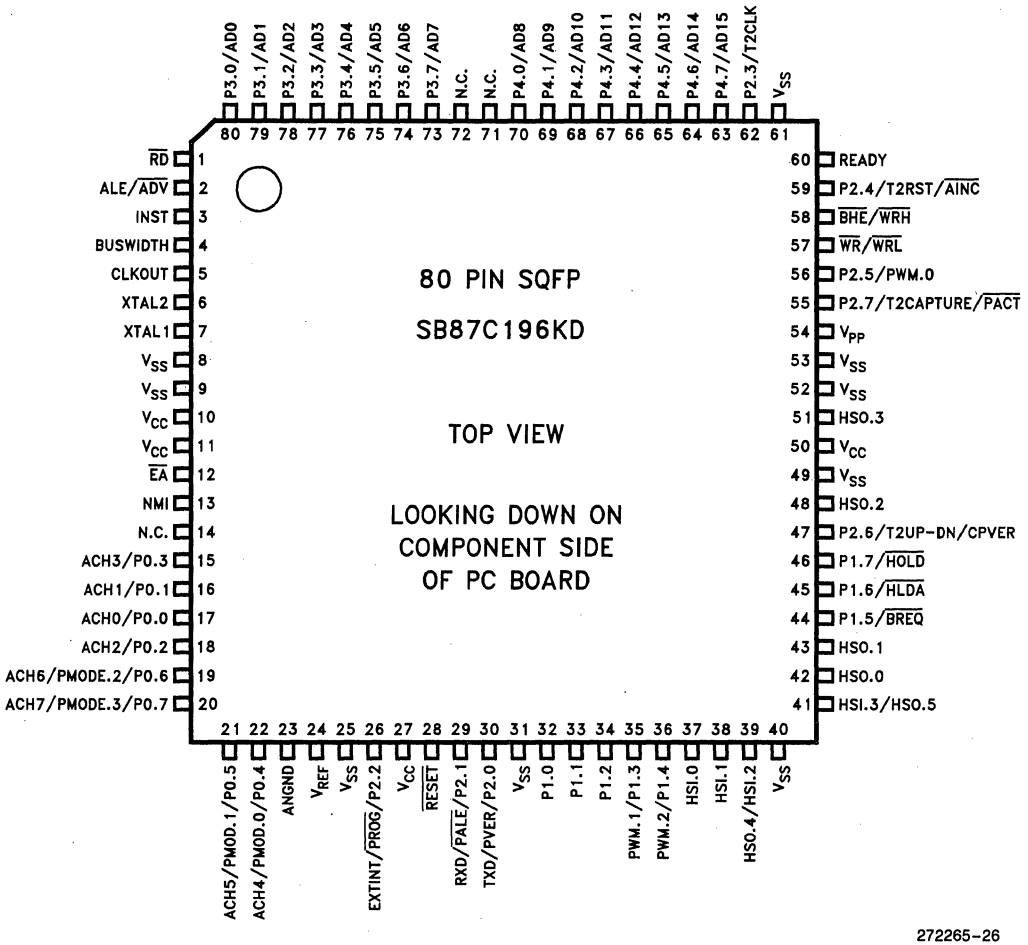


NOTE:
N.C. means No Connect (do not connect these pins).

80-Pin SQFP Package

6.0 PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of them must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage. Also timing pin for the return from power down circuit. Connect this pin with a 1 μF capacitor to V_{SS}. If this function is not used, connect to V_{CC}.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input and open-drain output. Hold low to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch and output low indicates a data fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{\text{BHE}}$ = 1), to the high byte only (A0 = 1, $\overline{\text{BHE}}$ = 0), or both bytes (A0 = 0, $\overline{\text{BHE}}$ = 0). If the $\overline{\text{WRH}}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle (held not ready) is available through configuration of CCR.

6.0 PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit. The HSI pins are also used as the SID in Slave Programming Mode.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. Three pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins set the Programming Mode.
Port 1	8-bit quasi-bidirectional I/O port. These pins are shared with $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and $\overline{\text{BREQ}}$.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 87C196KB.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus. Enabled by setting WSR.7.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. The TxD function is enabled by setting IOC1.5. In mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. The RxD function is enabled by setting SPCON.3. In mode 0 the pin functions as input or output data.
EXTINT	A rising edge on the EXTINT pin will generate an external interrupt. EXTINT is selected as the external interrupt source by setting IOC1.1 high.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2. The external reset function is enabled by setting IOCO.3. T2RST is enabled as the reset source by clearing IOCO.5.
PWM0–2	Port 2.5 can be enabled as a PWM output. The duty cycle of the PWM is determined by the value loaded into the PWM-CONTROL registers.
T2UPDN	The T2UPDN pin controls the direction of Timer2 as an up or down counter. The Timer2 up/down function is enabled by setting IOC2.1.
T2CAP	A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register (location 0CH in Window 15).
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PACT}}$	Programming Active. Used in the Auto Programming Mode to indicate when programming activity is complete.
PVER	Program Verification. Used in Slave Programming and Auto Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low input signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

6.0 PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
PORT 3 and 4 (During Programming)	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory.
CPVER	Cumulative Program Output Verification. Pin is high if all locations since entering a programming mode have programmed correctly.

7.0 OPCODE TABLE

00	SKIP
01	CLR
02	NOT
03	NEG
04	XCH
05	DEC
06	EXT
07	INC
08	SHR
09	SHL
0A	SHRA
0B	XCH
0C	SHRL
0D	SHLL
0E	SHRAL
0F	NORML
10	RESERVED
11	CLRB
12	NOTB
13	NEGB
14	XCHB
15	DECB
16	EXTB
17	INCB
18	SHRB
19	SHLB
1A	SHRAB
1B	XCHB
1C	RESERVED
1D	RESERVED
1E	RESERVED
1F	RESERVED
20	SJMP
21	SJMP
22	SJMP
23	SJMP
24	SJMP
25	SJMP
26	SJMP
27	SJMP
28	SCALL
29	SCALL
2A	SCALL
2B	SCALL
2C	SCALL
2D	SCALL
2E	SCALL
2F	SCALL
30	JBC
31	JBC
32	JBC
33	JBC
34	JBC
35	JBC
36	JBC
37	JBC
38	JBS
39	JBS
3A	JBS
3B	JBS
3C	JBS
3D	JBS
3E	JBS
3F	JBS
40	AND DIRECT (3 OPS)
41	AND IMMEDIATE (3 OPS)
42	AND INDIRECT (3 OPS)
43	AND INDEXED (3 OPS)
44	ADD DIRECT (3 OPS)
45	ADD IMMEDIATE (3 OPS)
46	ADD INDIRECT (3 OPS)
47	ADD INDEXED (3 OPS)
48	SUB DIRECT (3 OPS)
49	SUB IMMEDIATE (3 OPS)
4A	SUB INDIRECT (3 OPS)
4B	SUB INDEXED (3 OPS)
4C	MULU DIRECT (3 OPS)
4D	MULU IMMEDIATE (3 OPS)
4E	MULU INDIRECT (3 OPS)
4F	MULU INDEXED (3 OPS)
50	ANDB DIRECT (3 OPS)
51	ANDB IMMEDIATE (3 OPS)
52	ANDB INDIRECT (3 OPS)
53	ANDB INDEXED (3 OPS)
54	ADDB DIRECT (3 OPS)
55	ADDB IMMEDIATE (3 OPS)
56	ADDB INDIRECT (3 OPS)
57	ADDB INDEXED (3 OPS)
58	SUBB DIRECT (3 OPS)
59	SUBB IMMEDIATE (3 OPS)
5A	SUBB INDIRECT (3 OPS)
5B	SUBB INDEXED (3 OPS)
5C	MULUB DIRECT (3 OPS)
5D	MULUB IMMEDIATE (3 OPS)
5E	MULUB INDIRECT (3 OPS)
5F	MULUB INDEXED (3 OPS)
60	AND DIRECT (2 OPS)
61	AND IMMEDIATE (2 OPS)
62	AND INDIRECT (2 OPS)
62	AND INDEXED (2 OPS)
64	ADD DIRECT (2 OPS)
65	ADD IMMEDIATE (2 OPS)
66	ADD INDIRECT (2 OPS)
67	ADD INDEXED (2 OPS)
68	SUB DIRECT (2 OPS)
69	SUB IMMEDIATE (2 OPS)
6A	SUB INDIRECT (2 OPS)
6B	SUB INDEXED (2 OPS)
6C	MULU DIRECT (2 OPS)
6D	MULU IMMEDIATE (2 OPS)
6E	MULU INDIRECT (2 OPS)
6F	MULU INDEXED (2 OPS)
70	ANDB DIRECT (2 OPS)
71	ANDB IMMEDIATE (2 OPS)
72	ANDB INDIRECT (2 OPS)
73	ANDB INDEXED (2 OPS)
74	ADDB DIRECT (2 OPS)
75	ADDB IMMEDIATE (2 OPS)
76	ADDB INDIRECT (2 OPS)
77	ADDB INDEXED (2 OPS)
78	SUBB DIRECT (2 OPS)
79	SUBB IMMEDIATE (2 OPS)
7A	SUBB INDIRECT (2 OPS)
7B	SUBB INDEXED (2 OPS)
7C	MULUB DIRECT (2 OPS)
7D	MULUB IMMEDIATE (2 OPS)
7E	MULUB INDIRECT (2 OPS)
7F	MULUB INDEXED (2 OPS)
80	OR DIRECT
81	OR IMMEDIATE
82	OR INDIRECT
83	OR INDEXED
84	XOR DIRECT
85	XOR IMMEDIATE
86	XOR INDIRECT

7.0 OPCODE TABLE (Continued)

87	XOR INDEXED
88	CMP DIRECT
89	CMP IMMEDIATE
8A	CMP INDIRECT
8B	CMP INDEXED
8C	DIVU DIRECT
8D	DIVU IMMEDIATE
8E	DIVU INDIRECT
8F	DIVU INDEXED
90	ORB DIRECT
91	ORB IMMEDIATE
92	ORB INDIRECT
93	ORB INDEXED
94	XORB DIRECT
95	XORB IMMEDIATE
96	XORB INDIRECT
97	XORB INDEXED
98	CMPB DIRECT
99	CMPB IMMEDIATE
9A	CMPB INDIRECT
9B	CMPB INDEXED
9C	DIVUB DIRECT
9D	DIVUB IMMEDIATE
9E	DIVUB INDIRECT
9F	DIVUB INDEXED
A0	LD DIRECT
A1	LD IMMEDIATE
A2	LD INDIRECT
A3	LD INDEXED
A4	ADDC DIRECT
A5	ADDC IMMEDIATE
A6	ADDC INDIRECT
A7	ADDC INDEXED
A8	SUBC DIRECT
A9	SUBC IMMEDIATE
AA	SUBC INDIRECT
AB	SUBC INDEXED
AC	LDBZE DIRECT
AD	LDBZE IMMEDIATE
AE	LDBZE INDIRECT
AF	LDBZE INDEXED

B0	LDB DIRECT
B1	LDB IMMEDIATE
B2	LDB INDIRECT
B3	LDB INDEXED
B4	ADDCB DIRECT
B5	ADDCB IMMEDIATE
B6	ADDCB INDIRECT
B7	ADDCB INDEXED
B8	SUBCB DIRECT
B9	SUBCB IMMEDIATE
BA	SUBCB INDIRECT
BB	SUBCB INDEXED
BC	LDBSE DIRECT
BD	LDBSE IMMEDIATE
BE	LDBSE INDIRECT
BF	LDBSE INDEXED
C0	ST DIRECT
C1	BMOV
C2	ST INDIRECT
C3	ST INDEXED
C4	STB DIRECT
C5	CMPL
C6	STB INDIRECT
C7	STB INDEXED
C8	PUSH DIRECT
C9	PUSH IMMEDIATE
CA	PUSH INDIRECT
CB	PUSH INDEXED
CC	POP DIRECT
CD	BMOVI
CE	POP INDIRECT
CF	POP INDEXED
D0	JNST
D1	JNH
D2	JGT
D3	JNC
D4	JNVT
D5	JNV
D6	JGE
D7	JNE
D8	JST

D9	JH
DA	JLE
DB	JC
DC	JVT
DD	JV
DE	JLT
DF	JE
E0	DJNZ
E1	DJNZW
E2	TIJMP
E3	BR (INDIRECT)
E4	RESERVED
E5	RESERVED
E6	RESERVED
E7	LJMP
E8	RESERVED
E9	RESERVED
EA	RESERVED
EB	RESERVED
EC	DPTS
ED	EPTS
EE	RESERVED**
EF	LCALL
F0	RET
F1	RESERVED
F2	PUSHF
F3	POPF
F4	PUSHA
F5	POPA
F6	IDLPD
F7	TRAP
F8	CLRC
F9	SETC
FA	DI
FB	EI
FC	CLRVT
FD	NOP
FE	*DIV/DIVB/MUL/MULB
FF	RST

NOTE:
*Two Byte Instruction
RESERVED—Execution of RESERVED instructions will cause unimplemented opcode interrupt.
**Opcode EE is reserved but does not generate an unimplimented opcode interrupt.

8.0 INSTRUCTION SET SUMMARY

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D ← D + A	✓	✓	✓	✓	↑	–	
ADD/ADDB	3	D ← B + A	✓	✓	✓	✓	↑	–	
ADDC/ADDCB	2	D ← D + A + C	↓	✓	✓	✓	↑	–	
SUB/SUBB	2	D ← D − A	✓	✓	✓	✓	↑	–	
SUB/SUBB	3	D ← B − A	✓	✓	✓	✓	↑	–	
SUBC/SUBCB	2	D ← D − A + C − 1	↓	✓	✓	✓	↑	–	
CMP/CMPB	2	D − A	✓	✓	✓	✓	↑	–	
MUL/MULU	2	D,D + 2 ← D × A	–	–	–	–	–	–	2
MUL/MULU	3	D,D + 2 ← B × A	–	–	–	–	–	–	2
MULB/MULUB	2	D,D + 1 ← D × A	–	–	–	–	–	–	3
MULB/MULUB	3	D,D + 1 ← B × A	–	–	–	–	–	–	3
DIVU	2	D ← (D,D + 2) /A,D + 2 ← remainder	–	–	–	✓	↑	–	2
DIVUB	2	D ← (D,D + 1) /A,D + 1 ← remainder	–	–	–	✓	↑	–	3
DIV	2	D ← (D,D + 2) /A,D + 2 ← remainder	–	–	–	✓	↑	–	
DIVB	2	D ← (D,D + 1) /A,D + 1 ← remainder	–	–	–	✓	↑	–	
AND/ANDB	2	D ← D AND A	✓	✓	0	0	–	–	
AND/ANDB	3	D ← B AND A	✓	✓	0	0	–	–	
OR/ORB	2	D ← D OR A	✓	✓	0	0	–	–	
XOR/XORB	2	D ← D (ecxl. or) A	✓	✓	0	0	–	–	
LD/LDB	2	D ← A	–	–	–	–	–	–	
ST/STB	2	A ← D	–	–	–	–	–	–	
XCH/XCHB	2	D ← A, A ← D	–	–	–	–	–	–	
LDBSE	2	D ← A; D + 1 ← SIGN(A)	–	–	–	–	–	–	3,4
LDBZE	2	D ← A; D + 1 ← 0	–	–	–	–	–	–	3,4
PUSH	1	SP ← SP − 2; (SP) ← A	–	–	–	–	–	–	
POP	1	A ← (SP); SP + 2	–	–	–	–	–	–	
PUSHF	0	SP ← SP − 2; (SP) ← PSW; PSW ← 0000H; I ← 0	0	0	0	0	0	0	
POPF	0	PSW ← (SP); SP ← SP + 2; I ← ✓	✓	✓	✓	✓	✓	✓	
SJMP	1	PC ← PC + 11-bit offset	–	–	–	–	–	–	5
LJMP	1	PC ← PC + 16-bit offset	–	–	–	–	–	–	5
BR[indirect]	1	PC ← (A)	–	–	–	–	–	–	
TIJMP	3	PC ← [A] + 2 * ([B] AND C)	–	–	–	–	–	–	
SCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 11-bit offset	–	–	–	–	–	–	5
LCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 16-bit offset	–	–	–	–	–	–	5

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
RET	0	PC ← (SP); SP ← SP + 2	–	–	–	–	–	–	
J (conditional)	1	PC ← PC + 8-bit offset (if taken)	–	–	–	–	–	–	5
JC	1	Jump if C = 1	–	–	–	–	–	–	5
JNC	1	Jump if C = 0	–	–	–	–	–	–	5
JE	1	Jump if Z = 1	–	–	–	–	–	–	5
JNE	1	Jump if Z = 0	–	–	–	–	–	–	5
JGE	1	Jump if N = 0	–	–	–	–	–	–	5
JLT	1	Jump if N = 1	–	–	–	–	–	–	5
JGT	1	Jump if N = 0 and Z = 0	–	–	–	–	–	–	5
JLE	1	Jump if N = 1 or Z = 1	–	–	–	–	–	–	5
JH	1	Jump if C = 1 and Z = 0	–	–	–	–	–	–	5
JNH	1	Jump if C = 0 or Z = 1	–	–	–	–	–	–	5
JV	1	Jump if V = 1	–	–	–	–	–	–	5
JNV	1	Jump if V = 0	–	–	–	–	–	–	5
JVT	1	Jump if VT = 1; Clear VT	–	–	–	–	0	–	5
JNVT	1	Jump if VT = 0; Clear VT	–	–	–	–	0	–	5
JST	1	Jump if ST = 1	–	–	–	–	–	–	5
JNST	1	Jump if ST = 0	–	–	–	–	–	–	5
JBS	3	Jump if Specified Bit = 1	–	–	–	–	–	–	5,6
JBC	3	Jump if Specified Bit = 0	–	–	–	–	–	–	5,6
DJNZ/ DJNZW	1	D ← D − 1; If D ≠ 0 then PC ← PC + 8-bit offset	–	–	–	–	–	–	5
DEC/DECB	1	D ← D − 1	↙	↙	↙	↙	↑	–	
NEG/NEGB	1	D ← 0 − D	↙	↙	↙	↙	↑	–	
INC/INCB	1	D ← D + 1	↙	↙	↙	↙	↑	–	
EXT	1	D ← D; D + 2 ← Sign (D)	↙	↙	0	0	–	–	2
EXTB	1	D ← D; D + 1 ← Sign (D)	↙	↙	0	0	–	–	3
NOT/NOTB	1	D ← Logical Not (D)	↙	↙	0	0	–	–	
CLR/CLRB	1	D ← 0	1	0	0	0	–	–	
SHL/SHLB/SHLL	2	C ← msb - - - - - lsb ← 0	↙	↙	↙	↙	↑	–	7
SHR/SHRB/SHRL	2	0 → msb - - - - - lsb → C	↙	↙	↙	0	–	↙	7
SHRA/SHRAB/SHRAL	2	msb → msb - - - - - lsb → C	↙	↙	↙	0	–	↙	7
SETC	0	C ← 1	–	–	1	–	–	–	
CLRC	0	C ← 0	–	–	0	–	–	–	

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
CLRVT	0	VT ← 0	–	–	–	–	0	–	
RST	0	PC ← 2080H	0	0	0	0	0	0	8
DI	0	Disable All Interupts (I ← 0)	–	–	–	–	–	–	
EI	0	Enable All Interupts (I ← 1)	–	–	–	–	–	–	
DPTS	0	Disable all PTS Cycles (PSE = 0)	–	–	–	–	–	–	
EPTS	0	Enable all PTS Cycles (PSE = 1)	–	–	–	–	–	–	
NOP	0	PC ← PC + 1	–	–	–	–	–	–	
SKIP	1	PC ← PC + 2	–	–	–	–	–	–	
NORML	2	Left shift till msb = 1; D ← shift count	↕	↕	0	–	–	–	7
TRAP	0	SP ← SP − 2; (SP) ← PC; PC ← (2010H)	–	–	–	–	–	–	9
PUSHA	1	SP ← SP-2; (SP) ← PSW; PSW ← 0000H; SP ← SP-2; (SP) ← IMASK1/WSR; IMASK1 ← 00H	0	0	0	0	0	0	
POPA	1	IMASK1/WSR ← (SP); SP ← SP+2 PSW ← (SP); SP ← SP+2	↕	↕	↕	↕	↕	↕	
IDLPD	1	IDLE MODE IF KEY=1; POWERDOWN MODE IF KEY =2; CHIP RESET OTHERWISE	–	–	–	–	–	–	
CMPL	2	D-A	↕	↕	↕	↕	↑	–	
BMOV, BMOVi	2	[PTR__HI] + ← [PTR__LOW] + ; UNTIL COUNT=0	–	–	–	–	–	–	

NOTES:
1. If the mnemonic ends in "B" a byte operation is performed, otherwise a word operation is done. Operands D, B and A must conform to the alignment rules for the required operand type. D and B are locations in the Register File; A can be located anywhere in memory.
2. D,D + 2 are consecutive WORDS in memory; D is DOUBLE-WORD aligned.
3. D,D + 1 are consecutive BYTES in memory; D is WORD aligned.
4. Changes a byte to word.
5. Offset is a 2's complement number.
6. Specified bit is one of the 2048 bits in the register file.
7. The "L" (Long) suffix indicates double-word operation.
8. Initiates a Reset by pulling $\overline{\text{RESET}}$ low. Software should re-initialize all the necessary registers with code starting at 2080H.
9. The assembler will not accept this mnemonic.

9.0 INSTRUCTION LENGTH/OPCODE

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL(1)	A-INC(1)	SHORT(1)	LONG(1)
ADD (3-op)	4/44	5/45	4/46	4/46	5/47	6/47
SUB (3-op)	4/48	5/49	4/4A	4/4A	5/4B	6/4B
ADD (2-op)	3/64	4/65	3/66	3/66	4/67	5/67
SUB (2-op)	3/68	4/69	3/6A	3/6A	4/6B	5/6B
ADDC	3/A4	4/A5	3/A6	3/A6	4/A7	5/A7
SUBC	3/A8	4/A9	3/AA	3/AA	4/AB	5/AB
CMP	3/88	4/89	3/8A	3/8A	4/8B	5/8B
ADDB (3-op)	4/54	4/55	4/56	4/56	5/57	6/57
SUBB (3-op)	4/58	4/59	4/5A	4/5A	5/5B	6/5B
ADDB (2-op)	3/74	3/75	3/76	3/76	4/77	5/77
SUBB (2-op)	3/78	3/79	3/7A	3/7A	4/7B	5/7B
ADDCB	3/B4	3/B5	3/B6	3/B6	4/B7	5/B7
SUBCB	3/B8	3/B9	3/BA	3/BA	4/BB	5/BB
CMPB	3/98	3/99	3/9A	3/9A	4/9B	5/9B
MUL (3-op)	5/(2)	6/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULU (3-op)	4/4C	5/4D	4/4E	4/4E	5/4F	6/4F
MUL (2-op)	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULU (2-op)	3/6C	4/6D	3/6E	3/6E	4/6F	5/6F
DIV	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVU	3/8C	4/8D	3/8E	3/8E	4/8F	5/8F
MULB (3-op)	5/(2)	5/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULUB (3-op)	4/5C	4/5D	4/5E	4/5E	5/5F	6/5F
MULB (2-op)	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULUB (2-op)	3/7C	3/7D	3/7E	3/7E	4/7F	5/7F
DIVB	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVUB	3/9C	3/9D	3/9E	3/9E	4/9F	5/9F
AND (3-op)	4/40	5/41	4/42	4/42	5/43	6/43
AND (2-op)	3/60	4/61	3/62	3/62	4/63	5/63
OR (2-op)	3/80	4/81	3/82	3/82	4/83	5/83
XOR	3/84	4/85	3/86	3/86	4/87	5/87
ANDB (3-op)	4/50	4/51	4/52	4/52	5/53	5/53
ANDB (2-op)	3/70	3/71	3/72	3/72	4/73	4/73
ORB (2-op)	3/90	3/91	3/92	3/92	4/93	5/93
XORB	3/94	3/95	3/96	3/96	4/97	5/97
PUSH	2/C8	3/C9	2/CA	2/CA	3/CB	4/CB
POP	2/CC	—	2/CE	2/CE	3/CF	4/CF

9.0 INSTRUCTION LENGTH/OPCODE (Continued)

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL	A-INC	SHORT	LONG
LD	3/A0	4/A1	3/A2	3/A2	4/A3	5/A3
LDB	3/B0	3/B1	3/B2	3/B2	4/B3	5/B3
ST	3/C0	—	3/C2	3/C2	4/C3	5/C3
STB	3/C4	—	3/C6	3/C6	4/C7	5/C7
XCH	3/04	—	—	—	4/0B	5/0B
XCHB	3/14	—	—	—	4/1B	5/1B
LDBSE	3/BC	3/BD	3/BE	3/BE	4/BF	5/BF
LBSZE	3/AC	3/AD	3/AE	3/AE	4/AF	5/AF

Mnemonic	Length/Opcode
PUSHF	1/F2
POPF	1/F3
PUSHA	1/F4
POPA	1/F5
TRAP	1/F7
LCALL	3/EF
SCALL	2/28–2F(3)
RET	1/F0
LJMP	3/E7
SJMP	2/20–27(3)
BR[ ]	2/E3
TIJMP	4/E2
JNST	1/D0
JST	1/D8
JNH	1/D1
JH	1/D9
JGT	1/D2
JLE	1/DA
JNC	1/B3
JC	1/D8
JNVT	1/D4
JVT	1/DC
JNV	1/D5
JV	1/DD
JGE	1/D6
JLT	1/DE
JNE	1/D7

Mnemonic	Length/Opcode
JE	1/DF
JBC	3/30–37
JBS	3/38–3F
DJNZ	3/E0
DJNZW	3/E1
NORML	3/0F
SHRL	3/0C
SHLL	3/0D
SHRAL	3/0E
SHR	3/08
SHRB	3/18
SHL	3/09
SHLB	3/19
SHRA	3/0A
SHRAB	3/1A
CLRC	1/F8
SETC	1/F9
DI	1/FA
EI	1/FB
DPTS	1/EC
EPTS	1/ED
CLRVT	1/FC
NOP	1/FD
RST	1/FF
SKIP	2/00
IDLPD	1/F6
BMOV	3/C1
BMOVi	3/CD

NOTES:
1. Indirect and indirect + share the same opcodes, as do short and long indexed opcodes. If the second byte is even, use indirect or short indexed. If odd, use indirect or long indexed.
2. The opcodes for signed multiply and divide are the unsigned opcode with an "FE" prefix.
3. The 3 least significant bits of the opcode are concatenated with the 8 bits to form an 11-bit, 2's complement offset.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES)

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL*	A-INC*	SHORT*	LONG*
ADD (3-op)	5	6	7/10	8/11	7/10	8/11
SUB (3-op)	5	6	7/10	8/11	7/10	8/11
ADD (2-op)	4	5	6/8	7/9	6/8	7/9
SUB (2-op)	4	5	6/8	7/9	6/8	7/9
ADDC	4	5	6/8	7/9	6/8	7/9
SUBC	4	5	6/8	7/9	6/8	7/9
CMP	4	5	6/8	7/9	6/8	7/9
ADDB (3-op)	5	5	7/10	8/11	7/10	8/11
SUBB (3-op)	5	5	7/10	8/11	7/10	8/11
ADDB (2-op)	4	4	6/8	7/9	6/8	7/9
SUBB (2-op)	4	4	6/8	7/9	6/8	7/9
ADDCB	4	4	6/8	7/9	6/8	7/9
SUBCB	4	4	6/8	7/9	6/8	7/9
CMPB	4	4	6/8	7/9	6/8	7/9
MUL (3-op)	16	17	18/21	19/22	19/22	20/23
MULU (3-op)	14	15	16/19	17/19	17/20	18/21
MUL (2-op)	16	17	18/21	19/22	19/22	20/23
MULU (2-op)	14	15	16/19	17/19	17/20	18/21
DIV	26	27	28/31	29/32	29/32	30/33
DIVU	24	25	26/29	27/30	27/30	28/31
MULB (3-op)	12	12	14/17	15/18	15/18	16/19
MULUB (3-op)	10	10	12/15	12/16	12/16	14/17
MULB (2-op)	12	12	14/17	15/18	15/18	16/19
MULUB (2-op)	10	10	12/15	13/15	12/16	14/17
DIVB	18	18	20/23	21/24	21/24	22/25
DIVUB	16	16	18/21	19/22	19/22	20/23
AND (3-op)	5	6	7/10	8/11	7/10	8/11
AND (2-op)	4	5	6/8	7/9	6/8	7/9
OR (2-op)	4	5	6/8	7/9	6/8	7/9
XOR	4	5	6/8	7/9	6/8	7/9
ANDB (3-op)	5	5	7/10	8/11	7/10	8/11
ANDB (2-op)	4	4	6/8	7/9	6/8	7/9
ORB (2-op)	4	4	6/8	7/9	6/8	7/9
XORB	4	4	6/8	7/9	6/8	7/9
LD, LDB	4, 4	5, 4	5/8	6/8	6/9	7/10
ST, STB	4, 4	–	5/8	6/9	6/9	7/10
XCH, XCHB	5, 5	–	–	–	8/13	9/14
LDBSE	4	4	5/8	6/8	6/9	7/10
LDBZE	4	4	5/8	6/8	6/9	7/10
BMOV	6+8 per word +3 for each memory controller reference					
BMOVi	7+8 per word + 14 for each interrupt +3 for each memory controller reference					
PUSH (int stack)	6	7	9/12	10/13	10/13	11/14
POP (int stack)	8	–	10/12	11/13	11/13	12/14
PUSH (ext stack)	8	9	11/14	12/15	12/15	13/16
POP (ext stack)	11	–	13/15	14/16	14/16	15/17

*Times for operands addressed as SFRs and internal RAM (0-1FFH)/memory controller references (200–0FFFFH)).

NOTES:
1. Execution times for memory controller references may be one to two states higher depending on the number of bytes in the prefetch queue.
2. INT stack is 0–1FFH and EXT stack is 200–0FFFFH.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

MNEMONIC		MNEMONIC	
PUSHF (int stack)	6	PUSHF (ext stack)	8
POPF (int stack)	7	POPF (ext stack)	10
PUSHA (int stack)	12	PUSHA (ext stack)	18
POPA (int stack)	12	POPA (ext stack)	18
TRAP (int stack)	16	TRAP (ext stack)	18
LCALL (int stack)	11	LCALL (ext stack)	13
SCALL (int stack)	11	SCALL (ext stack)	13
RET (int stack)	11	RET (ext stack)	14
CMPL	7	DEC/DECB	3
CLR/CLRB	3	EXT/EXTB	4
NOT/NOTB	3	INC/INCB	3
NEG/NEGB	3		
LJMP	7		
SJMP	7		
BR [indirect]	7		
TIJMP	15 + 3 for each memory controller reference		
JNST, JST	4/8 jump not taken/jump taken		
JNH, JH	4/8 jump not taken/jump taken		
JGT, JLE	4/8 jump not taken/jump taken		
JNC, JC	4/8 jump not taken/jump taken		
JNVT, JVT	4/8 jump not taken/jump taken		
JNV, JV	4/8 jump not taken/jump taken		
JGE, JLT	4/8 jump not taken/jump taken		
JNE, JE	4/8 jump not taken/jump taken		
JBC, JBS	5/9 jump not taken/jump taken		
DJNZ	5/9 jump not taken/jump taken		
DJNZW	6/10 jump not taken/jump taken		
NORML	8 + 1 per shift (9 for 0 shift)		
SHRL	7+ 1 per shift (8 for 0 shift)		
SHLL	7 + 1 per shift (8 for 0 shift)		
SHRAL	7 + 1 per shift (8 for 0 shift)		
SHR/SHRB	6 + 1 per shift (7 for 0 shift)		
SHL/SHLB	6 + 1 per shift (7 for 0 shift)		
SHRA/SHRAB	6 + 1 per shift (7 for 0 shift)		
CLRC	2		
SETC	2		
DI	2		
EI	2		
DPTS	2		
EPTS	2		
CLRVT	2		
NOP	2		
RST	20 (includes fetch of configuration byte)		
SKIP	3		
IDLPD	8/25 (proper key/improper key)		

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

PTS CYCLES	
Single Transfer	18 (+ 3 for each memory controller reference)
Block Transfer	13 (+ 7 for each transfer, 1 minimum + 3 for each memory controller reference)
A/D Mode (SFRs/internal RAM)	21
(MEMORY CONT)	25
HSI MODE (SFRs/internal RAM)	12 (+ 10 for each transfer, 1 minimum)
(MEMORY CONT)	16 (+ 10 for each transfer, 1 minimum)
HSO MODE (SFRs/internal RAM)	11 (+ 10 for each transfer, 1 minimum)
(MEMORY CONT)	15 (+ 11 for each transfer, 1 minimum)

11.0 INTERRUPT TABLE

80C196KD Interrupt Priorities

Number	Source	Vector Location	Priority
INT15	NMI	203EH	15
N/A	PTS	Table	(1, 2)
INT14	HSI FIFO Full	203CH	14
INT13	EXTINT1	203AH	13
INT12	TIMER2 Overflow	2038H	12
INT11	TIMER2 Capture	2036H	11
INT10	4th Entry into HSI FIFO	2034H	10
INT09	RI	2032H	9
INT08	TI	2030H	8
SPECIAL	Unimplemented Opcode	2012H	N/A
SPECIAL	Trap	2010H	N/A
INT07	EXTINT	200EH	7
INT06	Serial Port	200CH	6
INT05	Software Timer	200AH	5
INT04	HSI.0 Pin	2008H	4
INT03	High Speed Outputs	2006H	3
INT02	HSI Data Available	2004H	2
INT01	A/D Conversion Complete	2002H	1
INT00	Timer Overflow	2000H	0

PTS Vector Table

PTS Vector	Location
HSI FIFO Full	205CH
EXTINT1	205AH
TIMER2 Overflow	2058H
TIMER2 Capture	2056H
4th HSI FIFO Entry	2054H
RI	2052H
TI	2050H
EXTINT	204EH
Serial Port	204CH
Software Timer	204AH
HSI.0 Pin	2048H
High Speed Outputs	2046H
HSI Data Available	2044H
A/D Conversion Complete	2042H
Timer Overflow	2040H

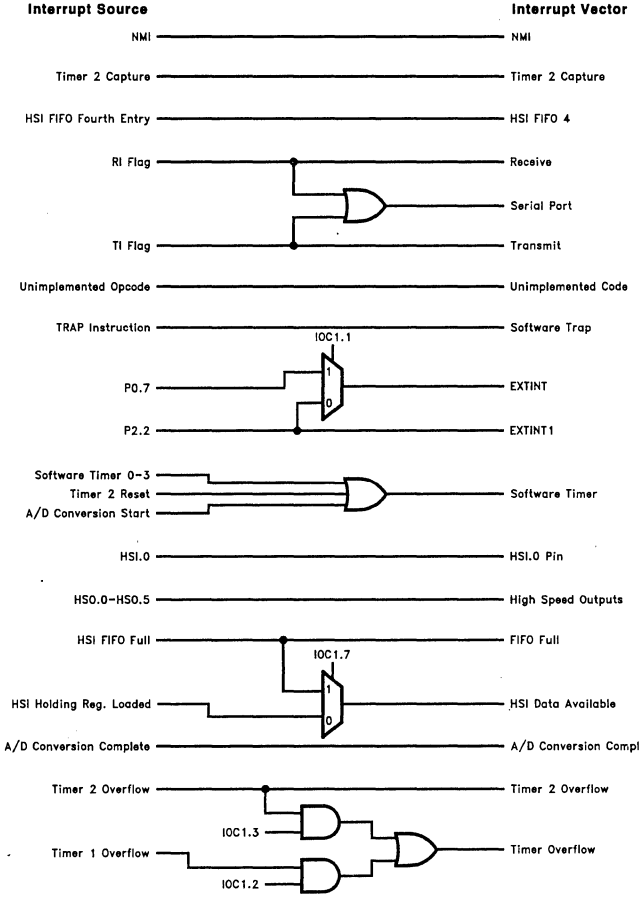
NOTES:
1. PTS interrupts have higher priority than all other interrupts except NMI.
2. PTS priorities are in the same order as conventional interrupts.

11.0 INTERRUPT TABLE (Continued)

PTS Control Blocks

	Single Transfer	Block Transfer	A/D Mode	HSO Mode	HSI Mode
	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED
	UNUSED	PTSBLOCK	UNUSED	PTSBLOCK	PTSBLOCK
	PTSDST (HI)	PTSDST (HI)	REG (HI)	UNUSED	UNUSED
	PTSDST (LO)	PTSDST (LO)	REG (LO)	UNUSED	UNUSED
	PTSSRC (HI)	PTSSRC (HI)	S/D (HI)	PTSSRC (HI)	PTSDEST (HI)
	PTSSRC (LO)	PTSSRC (LO)	S/D (LO)	PTSSRC (LO)	PTSDEST (LO)
	PTSCON	PTSCON	PTSCON	PTSCON	PTSCON
PTSVEC →	PTSCOUNT	PTSCOUNT	PTSCOUNT	PTSCOUNT	PTSCOUNT

80C196KD Interrupt Sources



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12.0 FORMULAS

Baud Rate

Asynchronous Modes 1, 2 and 3:

$$\text{BAUD\_REG} = \frac{\text{XTAL1}}{\text{Baud Rate} * 16} - 1$$

$$\text{or} \quad \frac{\text{T2CLK}}{\text{Baud Rate} * 8}$$

Synchronous Mode 0:

$$\text{BAUD\_REG} = \frac{\text{XTAL1}}{\text{Baud Rate} * 2} - 1$$

$$\text{or} \quad \frac{\text{T2CLK}}{\text{Baud Rate}}$$

A/D Conversion

$$\text{10-Bit value} = \text{INT}\left[\frac{1023 * (V_{IN} - \text{ANGND})}{(V_{REF} - \text{ANGND})}\right]$$

$$\text{8-Bit value} = \text{INT}\left[\frac{255 * (V_{IN} - \text{ANGND})}{(V_{REF} - \text{ANGND})}\right]$$

$$\text{SAM} = \frac{(T_{SAM} * F_{OSC}) - 2}{8}$$

$$T_{SAM} = \frac{(8 * \text{SAM}) + 2}{F_{OSC}}$$

$$\text{CONV} = \frac{(T_{CONV} * F_{OSC}) + 3}{2 * B}$$

$$T_{CONV} = \frac{(2 * B * \text{CONV}) - 3}{F_{OSC}}$$

T_{CONV} = Conversion time, μs

T_{SAMP} = Sample time, μs

SAM = Value loaded into AD_TIME bits 5, 6, 7. Must equal 1 through 7

CONV = Value loaded into AD_TIME bits 0–5. Must equal 2 through 31

XTAL1 = Processor frequency, MHz

B = 8 for 8-bit conversion

B = 10 for 10-bit conversion

Pulse Width Modulation (PWM)

PWM_CONTROL = 256 * duty cycle or

PWM_CONTROL = 512 * duty cycle

State Time

$$1 \text{ STATE TIME} = \frac{2}{\text{XTAL1}} = 2\,T_{OSC}$$

Signature Word and Voltage Levels

Description	Location	Value
Signature Word	70H	879CH
Programming V_{CC}	72H	040H 5.0V
Programming V_{PP}	73H	0A0H 12.50V

13.0 RESET STATUS

SFR Reset Status

Register Name	Value
AD_RESULT	7FF0H
AD_TIME	0FFH
HSI_STATUS	X0X0X0X0B
SBUF(RX)	00H
INT_MASK	00000000B
INT_PENDING	00000000B
TIMER1	0000H
TIMER2	0000H
IOPORT1	11111111B
IOPORT2	11000001B
SP_STAT/SP_CON	00001011B
IMASK1	00000000B
IPEND1	00000000B
WSR	XXXX0000B
HSI_MODE	11111111B
IOC2	X0000000B
IOC0	000000X0B
IOC1	00100001B
PWM_CONTROLS	00H
IOPORT3	11111111B
IOPORT4	11111111B
IOS0	00000000B
IOS1	00000000B
IOS2	00000000B
IOC3	11110010B

8XC196KD Pin Reset Status

Pin Name	Multiplexed Port Pins	Pin Status During Reset	Pin Status After Reset
ACH0–ACH7	P0.0–P0.7	Undefined Inputs(1)	Undefined Inputs(1)
PORT1	P1.0–P1.7	Weak Pull-ups (I_{IL} Spec)	Weak Pull-ups (I_{IL} Spec)
TXD	P2.0	Strong Pull-up (I_{IL2} Spec)	Strongly Driven
RXD	P2.1	Undefined Input(3)	Undefined Input(3)
EXTINT	P2.2	Undefined Input(3)	Undefined Input(3)
T2CLK	P2.3	Undefined Input(3)	Undefined Input(3)
T2RST	P2.4	Undefined Input(3)	Undefined Input(3)
PWM0	P2.5	Medium Pull-down	Strongly Driven
	P2.6–P2.7	Weak Pull-ups	Weak Pull-ups
AD0–AD15	P3.0–P4.7	Weak Pull-ups	Address/Data Bus or Open-Drain I/O(2)
HSI.0, HSI.1		Undefined Input(3)	Undefined Input(3)
HSI.2/HSO.4		Undefined Input(3)	Undefined Input(3)
HSI.3/HSO.5		Undefined Input(3)	Undefined Input(3)
HSO.0/HSO.3		Weak Pull-down	Weak Pull-down
ALE		Weak Pull-up	Strongly Driven
$\overline{BHE}$		Weak Pull-up	Strongly Driven
BUSWIDTH		Undefined Input(3)	Undefined Input(3)
CLKOUT		CLKOUT (Strongly Driven)	CLKOUT (Strongly Driven)
$\overline{EA}$		Undefined Input(3)	Undefined Input(3)
INST		Weak Pull-down	Strongly Driven
NMI		Weak Pull-down (I_{IH1} Spec)	Weak Pull-down (I_{IH1} Spec)
$\overline{RD}$		Weak Pull-up	Strongly Driven
READY		Undefined Input(3)	Undefined Input(3)
$\overline{RESET}$		Medium Pull-up (R_{RST} Spec)	Medium Pull-up (R_{RST} Spec)
$\overline{WR}$		Weak Pull-up	Strongly Driven

NOTES:
1. These pins are allowed to float. However, it is recommended that unused pins be tied high or low.
2. The state of these pins depends on device configuration. If the address/data bus is active, the pins act as a strongly driven bus; otherwise, they act as an open-drain I/O port and are left floating.
3. These pins must be driven and not left floating. Input voltage must not exceed V_{CC} during power-up.
4. Consult the 8XC196KC/KD data sheet for specifications.

8XC196KD Pin Status Descriptions

Pin Status	Approximate Value
Weak Pull-up	70 μA
Medium Pull-up	1 mA
Strong Pull-up	12 mA
Weak Pull-down	200 μA
Medium Pull-down	1 mA
Strongly Driven High	See V_{OH} Specification
Strongly Driven Low	See V_{OL} Specification

NOTE:
These typical maximum values are approximate; they are provided for reference only and are not guaranteed.

intel®

October 1991

8XC196KR
Quick Reference

Order Number: 272113-001

8XC196KR Quick Reference

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1.0 MEMORY MAP

0FFFFH 06000H	External Memory
05FFFH 02080H	Internal ROM/EPROM or External Memory
0207FH 0205EH	Reserved
0205DH 02040H	PTS Vectors
0203FH 02030H	Interrupt Vectors (Upper)
0202FH 02020H	ROM/EPROM Security Key
0201FH 0201BH	Reserved
0201AH	CCB1
02019H	Reserved
02018H	CCB0
02017H 02014H	Reserved
02013H 02000H	Interrupt Vectors (Lower)
01FFFH 01F00H	Internal SFRs
01EFFH 00500H	External Memory
004FFH 00400H	Internal RAM
003FFH 00200H	External Memory
001FFH 00000H	Register File

2.0 SFR MAP

CPU Special Function Registers

17H	(Reserved)	0BH	(Reserved)
16H	(Reserved)	0AH	WATCHDOG
15H	(Reserved)	09H	INT_PEND
14H	WSR	08H	INT_MASK
13H	INT_MASK1	07H	PTSSRV (Hi)
12H	INT_PEND1	06H	PTSSRV (Lo)
11H	(Reserved)	05H	PTSSEL (Hi)
10H	(Reserved)	04H	PTSSEL (Lo)
0FH	(Reserved)	03H	Read as FFH
0EH	(Reserved)	02H	Read as FFH
0DH	(Reserved)	01H	ZERO_REG (Hi)
0CH	(Reserved)	00H	ZERO_REG (Lo)

Memory Mapped I/O SFRs

	HIGH BYTE	LOW BYTE
1FFEH	P4_PIN	P3_PIN
1FFCH	P4_REG	P3_REG
1FFAH	SLP_CON	SLP_CMD
1FF8H	(Reserved)	SLP_STAT
1FF6H	P5_PIN	USFR
1FF4H	P5_REG	(Reserved)
1FF2H	P5_DIR	(Reserved)
1FF0H	P5_MODE	(Reserved)

Port 0, Port 1 and Port 6 SFRs

	HIGH BYTE	LOW BYTE
1FDEH	(Reserved)	(Reserved)
1FDCH	(Reserved)	(Reserved)
1FDAH	(Reserved)	P0_PIN
1FD8H	(Reserved)	(Reserved)
1FD6H	P6_PIN	P1_PIN
1FD4H	P6_REG	P1_REG
1FD2H	P6_DIR	P1_DIR
1FD0H	P6_MODE	P1_MODE

Port 2 SFRs

	HIGH BYTE	LOW BYTE
1FCEH	P2_PIN	(Reserved)
1FCCH	P2_REG	(Reserved)
1FCAH	P2_DIR	(Reserved)
1FC8H	P2_MODE	(Reserved)

Serial I/O and Synchronous SIO SFRs

	HIGH BYTE	LOW BYTE
1FBEH	(Reserved)	(Reserved)
1FBCH	SP_BAUD (Hi)	SP_BAUD (Lo)
1FBAH	SP_CON	SBUF_TX
1FB8H	SP_STATUS	SBUF_RX
1FB6H	(Reserved)	(Reserved)
1FB4H	(Reserved)	SSIO_BAUD
1FB2H	SSIO0_CON	SSIO0_BUF
1FB0H	SSIO1_CON	SSIO1_BUF

A/D and EPA Interrupt SFRs

	HIGH BYTE	LOW BYTE
1FAEH	AD_TIME	AD_TEST
1FACH	AD_COMMAND (Hi)	AD_COMMAND (Lo)
1FAAH	AD_RESULT (Hi)	AD_RESULT (Lo)
1FA8H	(Reserved)	EPAIPV
1FA6H	(Reserved)	EPA_PEND1
1FA4H	(Reserved)	EPA_MASK1
1FA2H	EPA_PEND (Hi)	EPA_PEND (Lo)
1FA0H	EPA_MASK (Hi)	EPA_MASK (Lo)

Timer 1 and Timer 2 SFRs

	HIGH BYTE	LOW BYTE
1F9EH	TIMER2 (Hi)	TIMER2 (Lo)
1F9CH	(Reserved)	T2CONTROL
1F9AH	TIMER1 (Hi)	TIMER1 (Lo)
1F98H	(Reserved)	T1CONTROL

EPA SFRs

	HIGH BYTE	LOW BYTE
1F8EH	COMP1_TIME (Hi)	COMP1_TIME (Lo)
1F8CH	(Reserved)	COMP1_CON
1F8AH	COMP0_TIME (Hi)	COMP0_TIME (Lo)
1F88H	(Reserved)	COMP0_CON
1F86H	EPA9_TIME (Hi)	EPA9_TIME (Lo)
1F84H	(Reserved)	EPA9_CON
1F82H	EPA8_TIME (Hi)	EPA8_TIME (Lo)
1F80H	(Reserved)	EPA8_CON
1F7EH	EPA7_TIME (Hi)	EPA7_TIME (Lo)
1F7CH	(Reserved)	EPA7_CON
1F7AH	EPA6_TIME (Hi)	EPA6_TIME (Lo)
1F78H	(Reserved)	EPA6_CON
1F76H	EPA5_TIME (Hi)	EPA5_TIME (Lo)
1F74H	(Reserved)	EPA5_CON
1F72H	EPA4_TIME (Hi)	EPA4_TIME (Lo)
1F70H	(Reserved)	EPA4_CON
1F6EH	EPA3_TIME (Hi)	EPA3_TIME (Lo)
1F6CH	EPA3_CON (Hi)	EPA3_CON (Lo)
1F6AH	EPA2_TIME (Hi)	EPA2_TIME (Lo)
1F68H	(Reserved)	EPA2_CON
1F66H	EPA1_TIME (Hi)	EPA1_TIME (Lo)
1F64H	EPA1_CON (Hi)	EPA1_CON (Lo)
1F62H	EPA0_TIME (Hi)	EPA0_TIME (Lo)
1F60H	(Reserved)	EPA0_CON

3.0 SFR BIT SUMMARY

EPAx_CONTROL

8	7	6	5	4	3	2	1	0
RM	TB	CE	M1	M0	RE	AD	ROT	ON/RT

RM: "1" Enables Remapping (EPA1 & EPA3 Only)
TB: "0" Selects Timer1, "1" Selects Timer2
CE: "0" Disables Comparator, "1" Enables Comparator
M1, M0: Mode Bits

M1, M0	Capture:	Compare:
00	No Op	Interrupt Only
01	Capture Negative	Output "0"
10	Capture Positive	Output "1"
11	Capture All Edges	Toggle Output

RE: Reenable Entry = "1" (Lock Entry)
AD: Start A/D
ROT: Reset Opposite Time Base
ON/RT: Overrun and Reset Timer Enable

EPAIPV 1FA8H: Byte

7	6	5	4	3	2	1	0
0	0	0	PV4	PV3	PV2	PV1	PV0

PV4–PV0: Returns the encoded highest priority interrupt. Value from 1H–14H.

0H = No Interrupt Pending	0AH = OVRINT4
14H = EPAINT4	09H = OVRINT5
13H = EPAINT5	08H = OVRINT6
12H = EPAINT6	07H = OVRINT7
11H = EPAINT7	06H = OVRINT8
10H = EPAINT8	05H = OVRINT9
0FH = EPAINT9	04H = Compare Channel 0
0EH = OVRINT0	03H = Compare Channel 1
0DH = OVRINT1	02H = TIMER1 Overflow
0CH = OVRINT2	01H = TIMER2 Overflow
0BH = OVRINT3	

SP_CON 1FBBH: Byte

7	6	5	4	3	2	1	0
X	X	X	TB8	REN	PEN	M2	M1

TB8: 9th Bit for Transmission
REN: Enables the Receiver
PEN: Enables Parity (Even)
M2, M1:
00: Mode 0/Sync
01: Mode 1/Async (std)
10: Mode 2/Async (9th Bit Enable)
11: Mode 3/Async (9th Bit Data)

SP_BAUD 1FBCH: Word

Mode 0:

$$\frac{XTAL1}{Baud * 2} - 1$$

or

$$\frac{T1CLK}{Baud}$$

Mode 1, 2, 3:

$$\frac{XTAL}{Baud * 16} - 1$$

or

$$\frac{T1CLK}{Baud * 8}$$

PORT 1/2/5/6 Control

Px_MODE = "1" for Peripheral Control
Px_MODE = "0" for Standard Port
Px_DIR = "1" for INPUT or OPEN DRAIN OUTPUT
Px_DIR = "0" for OUTPUT (PUSH/PULL)
Px_PIN is for PORT READs
Px_REG is for PORT WRITEs

TxCONTROL 1F98H: Byte = T1, 1F9CH: Byte = T2

7	6	5	4	3	2	1	0
CE	UD	M2	M1	M0	P2	P1	P0

CE: "0" Disables Timer, "1" Enables Timer
UD: "0" Counts Down, "1" Counts Up

M2, M1, M0—Mode Bits

000	Clock = Internal/Direction = UD
x01	Clock = External/Direction = UD
010	Clock = Internal/Direction = TxDIR
011	Clock = External/Direction = TxDIR
100	Clock = T1 Overflow/Direction = UD
110	Clock = T1 Overflow/Direction = T1
111	Quadrature Count (TxCLK/TxDIR)

P2, P1, P0—Prescale Bits

000	÷ 1 (250 ns @ 16 MHz) Xtal•4
001	÷ 2 (500 ns @ 16 MHz) Xtal•8
010	÷ 4 (1 μs @ 16 MHz) Xtal•16
011	÷ 8 (2 μs @ 16 MHz) Xtal•32
100	÷ 16 (4 μs @ 16 MHz) Xtal•64
101	÷ 32 (8 μs @ 16 MHz) Xtal•128
110	÷ 64 (16 μs @ 16 MHz) Xtal•256
111	Reserved

INT_MASK/INT_MASK1 08H/13H: Byte
INT_PEND/INT_PEND1 09H/12H: Byte
PTS_SRV 06: Word
PTS_SELECT 04H: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rsv	EXT INT	rsv	RI	TI	SSIO1	SSIO0	CBF	IBF	OBE	A/D Done	INT EPA0	INT EPA1	INT EPA2	INT EPA3	INT EPAX

AD_TEST 1FAEH: Byte

7	6	5	4	3	2	1	0
0	0	0	0	OF1	OF0	V_{REF}	A_{GND}

A_{GND}: Convert on AnGND
V_{REF}: Convert on V_{REF}
OF1, OF0: Offset Adjust
00: No Adjustment
01: ADD 2.5 mV
10: SUB 2.5 mV
11: SUB 5.0 mV

SP_STATUS 1FB9H: Byte

7	6	5	4	3	2	1	0
RB8/RPE	RI	TI	FE	TXE	OE	X	X

RP8: Set if 9th Bit set (No Parity)
RPE: Set if Parity Enabled and Parity Error
RI: Set after Last Data Bit Received
TI: Set at Beginning of STOP Bit
FE: Set if No STOP Bit Found
TXE: Set when Byte is in SBUF_TX
OE: Set if Overrun Error Occurred

AD_TIME 1FAFH: Byte

7	6	5	4	3	2	1	0
Sample Time				Conversion Time (CONV)			

SAM = 1 to 7 CONV = 2 to 31

Total Conversion Time:
T = (4 * SAM) + (B*(CONV + 1) + 2.5)
Where B = 8 for 8-Bit, 10 for 10-Bit

AD_COMMAND 1FACH: Byte/Word

7	6	5	4	3	2	1	0
0	0	T	M	GO	Channel #		

Channel # = 0 to 7
GO: "1" to Start Now/"0" for EPA Start
M: "0" = 10-Bit/"1" = 8-Bit Conversion
"0" = Detect High/"1" = Detect Low
T: "0" = Normal Conversion/"1" = Threshold Detect

EPA_MASK1/EPA_PEND1 1FA4H/1FA6H: Byte
EPA_MASK/EPA_PEND 1FA0H/1FA2H: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT EPA4	INT EPA5	INT EPA6	INT EPA7	INT EPA8	INT EPA9	OVR EPA0	OVR EPA1	OVR EPA2	OVR EPA3	OVR EPA4	OVR EPA5	OVR EPA6	OVR EPA7	OVR EPA8	OVR EPA9

7	6	5	4	3	2	1	0
rsv	rsv	rsv	rsv	COMP CH0	COMP CH1	OVR TIMR1	OVR TIMR2

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CCB0 2018H: Byte

0	PD	"1" Enables Powerdown
1	BW0	
2	WR	"1" = $\overline{WR}$/BHE – "0" = $\overline{WRL}$/$\overline{WRH}$
3	ALE	"1" = ALE – "0" = $\overline{ADV}$
4	IRC0	
5	IRC1	
6	LOC0	"0" Enables Write Lock
7	LOC1	"0" Enables Read Lock

201AH: Byte **CCB1**

Reserved Must Be "0"	0	0
	IRC2	1
	BW1	2
"0" = Always Enabled	WDE	3
Reserved Must Be "0DH"	1	4
	0	5
	1	6
	1	7

BW1	BW0	Bus Width
0	0	ILLEGAL
0	1	16-Bit Only
1	0	8-Bit Only
1	1	BUSW Pin Controlled

IRC2	IRC1	IRC0	Max Wait States
0	0	0	Zero Wait States
0	1	X	Illegal
0	X	1	Illegal
1	0	0	1 Wait State
1	0	1	2 Wait States
1	1	0	3 Wait States
1	1	1	INFINITE

SLP_CON 1FFBH: Byte

7	6	5	4	3	2	1	0
0	0	0	0	SLP	SLPL	IBEmask	OBFmask

SLP = 1 Enables Slave Port Operation
= 0 Disables Slave Port Operation and Clears Bits, CBE, IBE, and OBF in SLP_STAT

SLPL = 1 ALE Latches SLP_ADDR from AD1 (P3.1)
= 0 ALE is SLP_ADDR

IBEmask = 1 IBE Can Affect SLPINT
= 0 IBE Cannot Affect SLPINT

OBFmask = 1 OBF Can Affect SLPINT
= 0 OBF Cannot Affect SLPINT

SLP_STAT 1FF8H: Byte

7	6	5	4	3	2	1	0
STAT					CBE	IBE	OBF

STAT These bits are written by the 8XC196KR user and defined by the 8XC196KR user for communication flags.

CBE (Command Buffer Empty)
= 1 After 8XC196KR Reads SLPCMD
= 0 After Master Writes to SLPCMD or SLP = 0 in SLP_CON

IBE (Input Buffer Empty)
= 1 After 8XC196KR Reads SLPDIN
= 0 After Master Writes to SLPDIN, or SLP = 0 in SLP_CON

OBF (Output Buffer Full)
= 1 After 8XC196KR Writes to SLPDOUT
= 0 After Master Reads SLPDOUT

USFR 1FF6H (Read Only): Byte

7	6	5	4	3	2	1	0
RSV	RSV	RSV	DEI	DED	RSV	RSV	RSV

NOTE:
Do not write to location 1FF6H. Bits DED and DEI are written as specified in users manual.

Device	DEI	DED
87C196KR	UPROM Bit	UPROM Bit
83C196KR	N/A	N/A

DED—Disable External Data
DEI—Disable External Instructions

SSIOx_CON Registers 1FB1H: Byte = SSIO0
1FB3H: Byte = SSIO1

7	6	5	4	3	2	1	0
M/$\overline{S}$	T/$\overline{R}$	TRT	THS	STE	ATR	OUF	TBS

M/$\overline{S}$ Master/$\overline{\text{Slave}}$
T/$\overline{R}$ Transmit $\overline{\text{Receive}}$
TRT Transmitter/Receiver Toggle
THS Transceiver Handshake Select
STE Single Transfer Enable
ATR Auto Transfer Re-Enable
OUF Overflow/Underflow Flag
TBS Transceiver/Buffer Status

AD_RESULT 1FAAH: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8 MSB								2 LSB		RSV	RSV	BUSY	A/D Channel		

A/D Channel Channel Number: 0–7
BUSY 0 = A/D Idle
1 = A/D in Use
RSV Reserved
2 LSB 2 Least Significant Bits
8 MSB 8 Most Significant Bits
Bit 4, 5 0

WSR 14H: Byte

7	6	5	4	3	2	1	0
HLDEN	Window Select Bits						

HLDEN = 0 Disables HOLD/HLDA
= 1 Enables HOLD/HLDA

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4.0 PIN DEFINITION TABLE

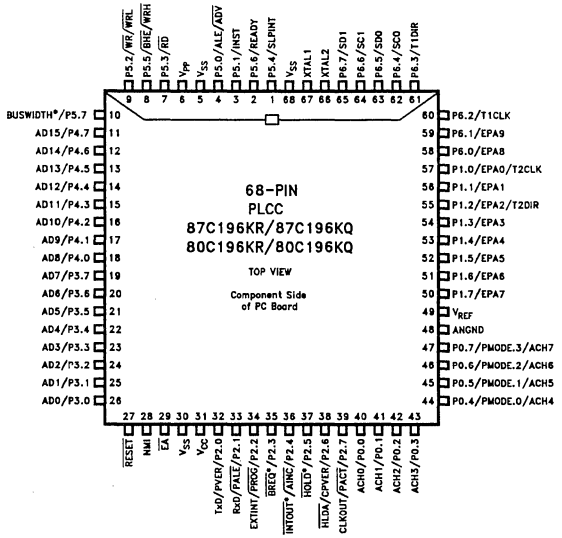
68 PLCC	52 PLCC	Function
40		ACH0
41		ACH1
42	33	ACH2
43	34	ACH3
44	35	ACH4
45	36	ACH5
46	37	ACH6
47	38	ACH7
26	22	AD0
25	21	AD1
24	20	AD2
23	19	AD3
22	18	AD4
21	17	AD5
20	16	AD6
19	15	AD7
18	14	AD8
17	13	AD9
16	12	AD10
15	11	AD11
14	10	AD12
13	09	AD13
12	08	AD14
11	07	AD15
04	02	$\overline{\text{ADV}}$
36	30	$\overline{\text{AINC}}$
04	02	ALE
48	39	ANGND
08		$\overline{\text{BHE}}$
35		$\overline{\text{BREQ}}$
10		BUSWIDTH
39	32	CLKOUT
38	31	CPVER
29	24	$\overline{\text{EA}}$
57	44	EPA0
56	43	EPA1

68 PLCC	52 PLCC	Function
55	42	EPA2
54	41	EPA3
53		EPA4
52		EPA5
51		EPA6
50		EPA7
58	45	EPA8
59	46	EPA9
34	29	EXTINT
38	31	$\overline{\text{HLDA}}$
37		$\overline{\text{HOLD}}$
03		INST
36	30	$\overline{\text{INTOUT}}$
28		NMI
40		P0.0
41		P0.1
42	33	P0.2
43	34	P0.3
44	35	P0.4
45	36	P0.5
46	37	P0.6
47	38	P0.7
57	44	P1.0
56	43	P1.1
55	42	P1.2
54	41	P1.3
53		P1.4
52		P1.5
51		P1.6
50		P1.7
32	27	P2.0
33	28	P2.1
34	29	P2.2
35		P2.3
36	30	P2.4

68 PLCC	52 PLCC	Function
37		P2.5
38	31	P2.6
39	32	P2.7
26	22	P3.0
25	21	P3.1
24	20	P3.2
23	19	P3.3
22	18	P3.4
21	17	P3.5
20	16	P3.6
19	15	P3.7
18	14	P4.0
17	13	P4.1
16	12	P4.2
15	11	P4.3
14	10	P4.4
13	09	P4.5
12	08	P4.6
11	07	P4.7
04	02	P5.0
03		P5.1
09	06	P5.2
07	05	P5.3
01		P5.4
08		P5.5
02		P5.6
10		P5.7
58	45	P6.0
59	46	P6.1
60		P6.2
61		P6.3
62	47	P6.4
63	48	P6.5
64	49	P6.6

68 PLCC	52 PLCC	Function
65	50	P6.7
39	32	$\overline{\text{PACT}}$
33	28	$\overline{\text{PALE}}$
44	35	PMODE.0
45	36	PMODE.1
46	37	PMODE.2
47	38	PMODE.3
34	29	$\overline{\text{PROG}}$
32	27	PVER
07	05	$\overline{\text{RD}}$
02		READY
27	23	$\overline{\text{RESET}}$
33	28	RXD
62	47	SC0
64	49	SC1
63	48	SD0
65	50	SD1
01		SLPINT
60		T1CLK
61		T1DIR
57		T2CLK
55		T2DIR
32	27	TXD
31	26	V_{CC}
06	04	V_{PP}
49	40	V_{REF}
05	01	V_{SS}
30	03	V_{SS}
68	25	V_{SS}
09	06	$\overline{\text{WR}}$
08		$\overline{\text{WRH}}$
09	06	$\overline{\text{WRL}}$
67	52	XTAL1
66	51	XTAL2

5.0 PACKAGE PIN ASSIGNMENTS



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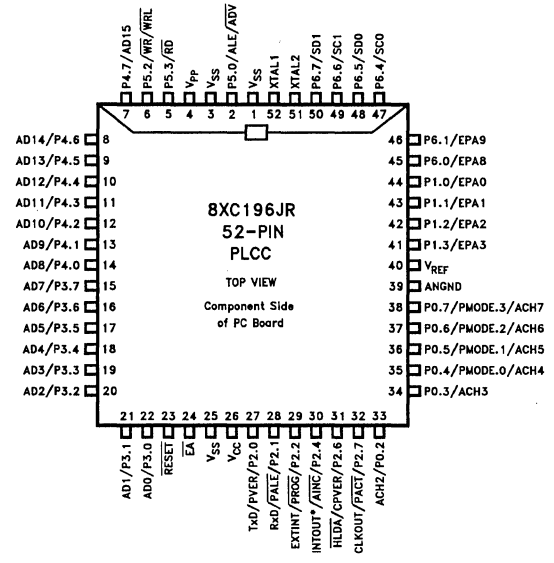
NOTE:
*In earlier versions of documentation these pins were referred to as:
$\overline{\text{INTOUT}}$ → $\overline{\text{INTINTOUT}}$
$\overline{\text{BREQ}}$ → $\overline{\text{INTB}}$
BUSWIDTH → BUSW
$\overline{\text{HOLD}}$ → $\overline{\text{HLD}}$



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NOTE:
*In earlier versions of documentation these pins were referred to as:
$\overline{\text{INTOUT}}$ → $\overline{\text{INTINTOUT}}$
$\overline{\text{BREQ}}$ → $\overline{\text{INTB}}$
BUSWIDTH → BUSW
$\overline{\text{HOLD}}$ → $\overline{\text{HLD}}$

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6.0 PIN DESCRIPTION

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS1}, V_{SS2}, V_{SS3}	Digital circuit ground (0V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference and supply voltage for the A/D converter and Port0 (+5V). Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from power-down circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, connect V_{PP} to V_{CC}.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
ACH0–ACH7/PORT0	Analog inputs to the on-chip A/D converter. Also a digital input pin.*
ALE/$\overline{ADV}$/P5.0	Address Latch Enable or Address Valid output. Goes low to latch and demultiplex the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle, providing a chip select for external memory. $\overline{ADV}$ is active only during external memory accesses. Also a standard I/O pin.*
$\overline{BHE}$/$\overline{WRH}$/P5.5	Byte High Enable or Write High output. $\overline{BHE}$ = 0 when accessing odd (high) bytes or complete words in external memory. $\overline{WRH}$ = 0 when writing to odd bytes or complete words in external memory. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory cycles. Also a standard I/O pin.*
$\overline{BREQ}$/P2.3	Bus Request output. Active low when the bus controller is in hold and has a pending external memory cycle. Also a standard I/O pin.*
BUSWIDTH/P5.7	Input for bus width selection. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. Also a standard I/O pin.*
CLOCKOUT/P2.7	Output of the internal clock generator. A 50% duty cycle signal at 1/2 XTAL1 frequency. Also a standard I/O pin.*
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ = 1 directs memory accesses from locations 2000H through 5FFFH to on-chip EPROM/ROM. $\overline{EA}$ = 0 directs all memory accesses to off-chip memory. $\overline{EA}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{EA}$ is latched at reset.
EPA0–7/P1.0–1.7 EPA8–9/P6.0–6.1	I/O pins for the Event Processor Array. EPA0 and EPA2 also function as T2CLK and T2DIR. Also a standard I/O pin.*
EXTINT/P2.2	External Interrupt input pin. A positive transition sets the EXTINT interrupt pending flag. The minimum high and low times are 2 oscillator cycles. Also a standard I/O pin.*
INST/P5.1	Instruction fetch signal. Output high during the entire bus cycle of an external instruction fetch. INST is active only during external memory fetches; during internal memory fetches, INST is low. Also a standard I/O pin.*
$\overline{INTOUT}$/P2.4	Interrupt output indicating that a pending interrupt requires use of the external bus. Also a standard I/O pin.*
$\overline{HLDA}$/P2.6	Bus Hold Acknowledge output indicating release of the bus in response to a HOLD request. Also a standard I/O pin.* This is also a TEST MODE enable pin. Do not use it as an input without careful hardware evaluation.

*These pins may be used for the system or peripheral functions or as a standard I/O pin.

6.0 PIN DESCRIPTION (Continued)

Symbol	Name and Function
$\overline{HOLD}$/P2.5	Bus Hold request input. $\overline{HOLD}$ is sent by another processor to request control of 8XC196KR system bus. Also a standard I/O pin.*
NMI	Non-Maskable interrupt input pin. A positive transition causes a non-maskable interrupt vector through memory location 203EH. If not used, this pin should be tied to V_{SS}. May be used by Intel Evaluation boards.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port 0 pins should not be left floating. In EPROM devices these pins are also used to select the Programming Mode.
PORT1	8-bit bidirectional standard I/O port. All of its pins are shared with the EPA.
PORT2	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (TxD, RxD, EXTINT, $\overline{BREQ}$, $\overline{INTOUT}$, $\overline{HOLD}$, $\overline{HLDA}$, $\overline{CLKOUT}$).
PORT3 PORT4	8-bit bidirectional standard I/O with open drain outputs. These pins are shared with the multiplexed address/data bus which uses complementary drivers.
PORT5	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (ALE/ADV, INST, $\overline{WR}$/$\overline{WRL}$, $\overline{RD}$, SLPINT, $\overline{BHE}$/$\overline{WRH}$, READY, BUSWIDTH).
PORT6	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (EPA8, EPA9, T1CLK, T1DIR, SC0, SD0, SC1, SD1).
$\overline{RD}$/P5.3	Read signal output to external memory. $\overline{RD}$ is low only during external memory reads. Also a standard I/O pin.*
READY/P5.6	Ready input to lengthen external memory cycles. If READY = 1, CPU operation continues in a normal manner. If READY = 0 wait states are added. Also a standard I/O pin.*
$\overline{RESET}$	Reset input to the chip. Held low for at least 16 state times to reset the chip. The subsequent low to high transition starts the reset sequence. Input high for normal operation. $\overline{RESET}$ has an internal pullup.
RXD/P2.1	Receive data input pin for the Serial I/O (SIO) port. Also a standard I/O pin.*
SLPINT/P5.4	Slave Port Interrupt output pin. Also a standard I/O pin.*
SSIO/P6.4–P6.7 (SC0, SD0, SC1, SD1)	Synchronous Serial I/O pins. SC0/SC1 are clock pins and SD0/SD1 are data pins. Also a standard I/O pin.*
T1CLK/P6.2	TIMER1 Clock input. TIMER1 increments or decrements on both rising and falling edges. Also a standard I/O pin.*
T1DIR/P6.3	TIMER1 Direction input. TIMER1 increments when this pin is high and decrements when this pin is low. Also a standard I/O pin.*
T2CLK/P1.0	TIMER2 Clock Input. TIMER2 increments or decrements on both rising and falling edges. Also a standard I/O pin.*
T2DIR/P1.2	TIMER2 Direction input. TIMER2 increments when this pin is high and decrements when this pin is low. Also a standard I/O pin.*
TXD/P2.0	Transmit data output pin for the Serial I/O (SIO) port. Also a standard I/O pin.*
$\overline{WR}$/$\overline{WRL}$/P5.2	Write and Write Low output to external memory. $\overline{WR}$ goes low for every external write. $\overline{WRL}$ goes low only for writes to even addresses. $\overline{WR}$/$\overline{WRL}$ is active only during external memory writes. Also a standard I/O pin.*
XTAL1	Input of the oscillator invertor and the internal clock generator. If using an external clock source connect it to this pin.
XTAL2	Output of the oscillator invertor. Leave floating unless connected to a crystal/ resonator circuit.

*These pins may be used for the system or peripheral functions or as a standard I/O pin.

6.0 PIN DESCRIPTION (Continued)

Programming Mode Pin Definitions

Name	Name and Function
PMODE P0.4–7	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by an 8XC196KR that is in Slave Programming Mode. Used to indicate that Port 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge latches data on PBUS and begins programming. Rising edge inputs ends programming.
PACT	Programming Active. Used to indicate when programming activity is complete.
PVER	Programming Verification. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low input enables the auto increment mode. Auto increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
PORTS 3 and 4	Address/Command/Data Bus. Used to pass commands, addresses and data to and from 8XC196KRs. Also used in the Auto Programming Mode as a regular system bus to access external memory.
CPVER	Cumulative Program Verification. Pin is high if all locations since entering a programming mode have programmed correctly.

7.0 OPCODE TABLE

00	SKIP
01	CLR
02	NOT
03	NEG
04	XCH
05	DEC
06	EXT
07	INC
08	SHR
09	SHL
0A	SHRA
0B	XCH
0C	SHRL
0D	SHLL
0E	SHRAL
0F	NORML
10	RESERVED
11	CLRB
12	NOTB
13	NEGB
14	XCHB
15	DECB
16	EXTB
17	INCB
18	SHRB
19	SHLB
1A	SHRAB
1B	XCHB
1C	RESERVED
1D	RESERVED
1E	RESERVED
1F	RESERVED
20	SJMP
21	SJMP
22	SJMP
23	SJMP
24	SJMP
25	SJMP
26	SJMP
27	SJMP
28	SCALL
29	SCALL
2A	SCALL
2B	SCALL
2C	SCALL
2D	SCALL
2E	SCALL

2F	SCALL
30	JBC
31	JBC
32	JBC
33	JBC
34	JBC
35	JBC
36	JBC
37	JBC
38	JBS
39	JBS
3A	JBS
3B	JBS
3C	JBS
3D	JBS
3E	JBS
3F	JBS
40	AND DIRECT (3 OPS)
41	AND IMMEDIATE (3 OPS)
42	AND INDIRECT (3 OPS)
43	AND INDEXED (3 OPS)
44	ADD DIRECT (3 OPS)
45	ADD IMMEDIATE (3 OPS)
46	ADD INDIRECT (3 OPS)
47	ADD INDEXED (3 OPS)
48	SUB DIRECT (3 OPS)
49	SUB IMMEDIATE (3 OPS)
4A	SUB INDIRECT (3 OPS)
4B	SUB INDEXED (3 OPS)
4C	MULU DIRECT (3 OPS)
4D	MULU IMMEDIATE (3 OPS)
4E	MULU INDIRECT (3 OPS)
4F	MULU INDEXED (3 OPS)
50	ANDB DIRECT (3 OPS)
51	ANDB IMMEDIATE (3 OPS)
52	ANDB INDIRECT (3 OPS)
53	ANDB INDEXED (3 OPS)
54	ADDB DIRECT (3 OPS)
55	ADDB IMMEDIATE (3 OPS)
56	ADDB INDIRECT (3 OPS)
57	ADDB INDEXED (3 OPS)
58	SUBB DIRECT (3 OPS)
59	SUBB IMMEDIATE (3 OPS)
5A	SUBB INDIRECT (3 OPS)
5B	SUBB INDEXED (3 OPS)
5C	MULUB DIRECT (3 OPS)
5D	MULUB IMMEDIATE (3 OPS)

5E	MULUB INDIRECT (3 OPS)
5F	MULUB INDEXED (3 OPS)
60	AND DIRECT (2 OPS)
61	AND IMMEDIATE (2 OPS)
62	AND INDIRECT (2 OPS)
63	AND INDEXED (2 OPS)
64	ADD DIRECT (2 OPS)
65	ADD IMMEDIATE (2 OPS)
66	ADD INDIRECT (2 OPS)
67	ADD INDEXED (2 OPS)
68	SUB DIRECT (2 OPS)
69	SUB IMMEDIATE (2 OPS)
6A	SUB INDIRECT (2 OPS)
6B	SUB INDEXED (2 OPS)
6C	MULU DIRECT (2 OPS)
6D	MULU IMMEDIATE (2 OPS)
6E	MULU INDIRECT (2 OPS)
6F	MULU INDEXED (2 OPS)
70	ANDB DIRECT (2 OPS)
71	ANDB IMMEDIATE (2 OPS)
72	ANDB INDIRECT (2 OPS)
73	ANDB INDEXED (2 OPS)
74	ADDB DIRECT (2 OPS)
75	ADDB IMMEDIATE (2 OPS)
76	ADDB INDIRECT (2 OPS)
77	ADDB INDEXED (2 OPS)
78	SUBB DIRECT (2 OPS)
79	SUBB IMMEDIATE (2 OPS)
7A	SUBB INDIRECT (2 OPS)
7B	SUBB INDEXED (2 OPS)
7C	MULUB DIRECT (2 OPS)
7D	MULUB IMMEDIATE (2 OPS)
7E	MULUB INDIRECT (2 OPS)
7F	MULUB INDEXED (2 OPS)
80	OR DIRECT
81	OR IMMEDIATE
82	OR INDIRECT
83	OR INDEXED
84	XOR DIRECT
85	XOR IMMEDIATE
86	XOR INDIRECT
87	XOR INDEXED
88	CMP DIRECT
89	CMP IMMEDIATE
8A	CMP INDIRECT
8B	CMP INDEXED
8C	DIVU DIRECT

7.0 OPCODE TABLE (Continued)

8D	DIVU IMMEDIATE
8E	DIVU INDIRECT
8F	DIVU INDEXED
90	ORB DIRECT
91	ORB IMMEDIATE
92	ORB INDIRECT
93	ORB INDEXED
94	XORB DIRECT
95	XORB IMMEDIATE
96	XORB INDIRECT
97	XORB INDEXED
98	CMPB DIRECT
99	CMPB IMMEDIATE
9A	CMPB INDIRECT
9B	CMPB INDEXED
9C	DIVUB DIRECT
9D	DIVUB IMMEDIATE
9E	DIVUB INDIRECT
9F	DIVUB INDEXED
A0	LD DIRECT
A1	LD IMMEDIATE
A2	LD INDIRECT
A3	LD INDEXED
A4	ADDC DIRECT
A5	ADDC IMMEDIATE
A6	ADDC INDIRECT
A7	ADDC INDEXED
A8	SUBC DIRECT
A9	SUBC IMMEDIATE
AA	SUBC INDIRECT
AB	SUBC INDEXED
AC	LDBZE DIRECT
AD	LDBZE IMMEDIATE
AE	LDBZE INDIRECT
AF	LDBZE INDEXED
B0	LDB DIRECT
B1	LDB IMMEDIATE
B2	LDB INDIRECT
B3	LDB INDEXED

B4	ADDCB DIRECT
B5	ADDCB IMMEDIATE
B6	ADDCB INDIRECT
B7	ADDCB INDEXED
B8	SUBCB DIRECT
B9	SUBCB IMMEDIATE
BA	SUBCB INDIRECT
BB	SUBCB INDEXED
BC	LDBSE DIRECT
BD	LDBSE IMMEDIATE
BE	LDBSE INDIRECT
BF	LDBSE INDEXED
C0	ST DIRECT
C1	BMOV
C2	ST INDIRECT
C3	ST INDEXED
C4	STB DIRECT
C5	CMPL
C6	STB INDIRECT
C7	STB INDEXED
C8	PUSH DIRECT
C9	PUSH IMMEDIATE
CA	PUSH INDIRECT
CB	PUSH INDEXED
CC	POP DIRECT
CD	BMOVI
CE	POP INDIRECT
CF	POP INDEXED
D0	JNST
D1	JNH
D2	JGT
D3	JNC
D4	JNVT
D5	JNV
D6	JGE
D7	JNE
D8	JST
D9	JH

DA	JLE
DB	JC
DC	JVT
DD	JV
DE	JLT
DF	JE
E0	DJNZ
E1	DJNZW
E2	TIJMP
E3	BR (INDIRECT)
E4	RESERVED
E5	RESERVED
E6	RESERVED
E7	LJMP
E8	RESERVED
E9	RESERVED
EA	RESERVED
EB	RESERVED
EC	DPTS
ED	EPTS
EE	RESERVED
EF	LCALL
F0	RET
F1	RESERVED
F2	PUSHF
F3	POPF
F4	PUSHA
F5	POPA
F6	IDPLD
F7	TRAP
F8	CLRC
F9	SETC
FA	DI
FB	EI
FC	CLRVT
FD	NOP
FE	*DIV/DIVB/MUL/MULB
FF	RST

*Two Byte Instruction - This opcode is placed as the first byte of an instruction to make it a signed operation instead of unsigned.

8.0 INSTRUCTION SET SUMMARY

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D = D + A	↕	↕	↕	↕	↑		
ADD/ADDB	3	D = B + A	↕	↕	↕	↕	↑		
ADDC/ADDCB	2	D = D + A + C	↓	↕	↕	↕	↑		
SUB/SUBB	2	D = D − A	↕	↕	↕	↕	↑		
SUB/SUBB	3	D = B − A	↕	↕	↕	↕	↑		
SUBC/SUBCB	2	D = D − A + C − 1	↓	↕	↕	↕	↑		
CMP/CMPB/CMPL	2	D − A	↕	↕	↕	↕	↑		
MUL/MULU	2	D,D + 2 = D × A							3
MUL/MULU	3	D,D + 2 = B × A							3
MULB/MULUB	2	D,D + 1 = D × A							4
MULB/MULUB	3	D,D + 1 = B × A							4
DIVU	2	D = (D,D + 2)/A,D + 2 = Remainder				↕	↑		3
DIVUB	2	D = (D,D + 1)/A,D + 1 = Remainder				↕	↑		4
DIV	2	D = (D,D + 2)/A,D + 2 = Remainder				↕	↑		
DIVB	2	D = (D,D + 1)/A,D + 1 = Remainder				↕	↑		
AND/ANDB	2	D = D and A	↕	↕	0	0			
AND/ANDB	3	D = B and A	↕	↕	0	0			
OR/ORB	2	D = D or A	↕	↕	0	0			
XOR/XORB	2	D = D (exclusive or) A	↕	↕	0	0			
LD/LDB	2	D = A							
ST/STB	2	A = D							
XCH	2	D ⟷ A; D + 1 ⟷ A + 1							
XCHB	2	D ⟷ A							
BMOV, BMOVI	2	(PTR_HI) + = (PTR_LOW) +; Until COUNT = 0							
LDBSE	2	D = A; D + 1 = Sign (A)							4, 5
LDBZE	2	D = A; D + 1 = 0							4, 5
PUSH	1	SP = SP − 2; (SP) = A							
POP	1	A = (SP); SP = SP + 2							
PUSHF	0	SP = SP − 2; (SP) = PSW; PSW = 0; I = 0; PSE = 0	0	0	0	0	0	0	11
POPF	0	PSW = (SP); SP = SP + 2; I ← ↕	↕	↕	↕	↕	↕	↕	11
PUSHA	0	SP = SP − 2; (SP) = PSW; PSW = 0000H; SP = SP − 2; (SP) = IMASK1/WSR; IMASK1 = 00H; I = 0; PSE = 0	0	0	0	0	0	0	
POPA	0	IMASK1/WSR = (SP); SP = SP + 2; PSW = (SP); SP = SP + 2	↕	↕	↕	↕	↕	↕	

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8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
SJMP	1	PC = PC + 11-Bit-Offset							6
LJMP	1	PC = PC + 16-Bit-Offset							6
BR[Indirect]	1	PC = (A)							
TIJMP	3	PC = ([index] and MASK)2 + (Table)							
TRAP	0	SP = SP − 2; (SP) = PC; PC = (2010H)							10
SCALL	1	SP = SP − 2; (SP) = PC; PC = PC + 11-Bit-Offset							6
LCALL	1	SP = SP − 2; (SP) = PC; PC = PC + 16-Bit-Offset							6
RET	0	PC = (SP); SP = SP + 2							
J(conditioned)	1	PC = PC + 8-Bit-Offset (If Taken)							6
JC	1	Jump if C = 1							6
JNC	1	Jump if C = 0							6
JE	1	Jump if Z = 1							6
JNE	1	Jump if Z = 0							6
JGE	1	Jump if N = 0							6
JLT	1	Jump if N = 1							6
JGT	1	Jump if N = 0 and Z = 0							6
JLE	1	Jump if N = 1 or Z = 1							6
JH	1	Jump if C = 1 and Z = 0							6
JNH	1	Jump if C = 0 or Z = 1							6
JV	1	Jump if V = 0							6
JNV	1	Jump if V = 1							6
JVT	1	Jump if VT = 1; Clear VT					0		6
JNVT	1	Jump if VT = 0; Clear VT					0		6
JST	1	Jump if ST = 1							6
JNST	1	Jump if ST = 0							6
JBS	3	Jump if Specific Bit = 1							6,7
JBC	3	Jump if Specific Bit = 0							6,7
DJNZ/DJNZW	1	D = D − 1; If D ≠ 0 then PC = PC + 8-Bit-Offset							6
DEC/DECB	1	D = D − 1	↙	↙	↙	↙	↑		
NEG/NEGB	1	D = 0 − D	↙	↙	↙	↙	↑		
INC/INCB	1	D = D + 1	↙	↙	↙	↙	↑		
EXT	1	D = D;D + 2 = Sign (D)	↙	↙	0	0			3
EXTB	1	D = D;D + 1 = Sign (D)	↙	↙	0	0			4
NOT/NOTB	1	D = Logical Not (D)	↙	↙	0	0			
CLR/CLRB	1	D = 0	1	0	0	0			

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
SHL/SHLB/SHLL	2	C ← msb○○○lsb ← 0	↙	↙	↙	↙	↑		8
SHR/SHRB/SHRL	2	0 → msb○○○lsb → C	↙	↙	↙	0		↙	8
SHRA/SHRAB/SHRAL	2	msb → msb○○○lsb → C	↙	↙	↙	0		↙	8
NORML	2	Left Shift until msb = 1;D = Shift Count	↙	↙	0				8
SETC	0	C = 1			1				
CLRC	0	C = 0			0				
CLRVT	0	VT = 0					0		
RST	0	PC = 2080H	0	0	0	0	0	0	9
DI	0	Disable All Interrupts (I = 0)							
EI	0	Enable All Interupts (I = 1)							
DPTS	0	Disable PTS Interrupts (PSE = 0)							
EPTS	0	Enable PTS Interrupts (PSE = 1)							
NOP	0	PC = PC + 1							
SKIP	0	PC = PC + 2							
IPLPD	1	Idle Mode IF Key = 1; Powerdown Mode IF Key = 2 Chip RESET Otherwise							

NOTES:
1. If the mnemonic ends in "B" a byte operation is performed, otherwise a word operation is performed. Operands D, B and A must conform to the alignment rules for the required operand type. D and B are locations in the Lower Register File; A can be located anywhere in memory.
2. The symbols indicate the effects on the flags:
   - ↙ Cleared or set as appropriate
   - 0 Cleared
   - 1 Set
   - ↑ Set if appropriate; never cleared
   - ↓ Cleared if appropriate; never set
3. D, D + 2 are consecutive WORDs in memory; D is DOUBLE-WORD aligned.
4. D, D + 1 are consecutive BYTEs in memory; D is WORD aligned.
5. Changes a BYTE to WORD.
6. Offset is a 2's complement number.
7. Specific Bit must be in or windowed into the Lower Register File.
8. The "L" (LONG) suffix indicates DOUBLE-WORD operations.
9. Initiates a RESET by pulling RESET low. Software should re-initialize all the neccessary registers with code starting at 2080H.
10. The assembler does not accept this mnemonic (use the macro file for definition).
11. I = Interrupt Enable (PSW1).

9.0 INSTRUCTION LENGTH/OPCODES

Mnemonic	Direct	Immed	Indirect		Indexed	
			Normal(1)	A-Inc(1)	Short(1)	Long(1)
ADD (3-op)	4/44	5/45	4/46	4/46	5/47	6/47
SUB (3-op)	4/48	5/49	4/4A	4/4A	5/4B	6/4B
ADD (2-op)	3/64	4/65	3/66	3/66	4/67	5/67
SUB (2-op)	3/68	4/69	3/6A	3/6A	4/6B	5/6B
ADDC	3/A4	4/A5	3/A6	3/A6	4/A7	5/A7
SUBC	3/A8	4/A9	3/AA	3/AA	4/AB	5/AB
CMP	3/88	4/89	3/8A	3/8A	4/8B	5/8B
ADDB (3-op)	4/54	4/55	4/56	4/56	5/57	6/57
SUBB (3-op)	4/58	4/59	4/5A	4/5A	5/5B	6/5B
ADDB (2-op)	3/74	3/75	3/76	3/76	4/77	5/77
SUBB (2-op)	3/78	3/79	3/7A	3/7A	4/7B	5/7B
ADDCB	3/B4	3/B5	3/B6	3/B6	4/B7	5/B7
SUBCB	3/B8	3/B9	3/BA	3/BA	4/BB	5/BB
CMPB	3/98	3/99	3/9A	3/9A	4/9B	5/9B
MUL (3-op)	5/(2)	6/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULU (3-op)	4/4C	5/4D	4/4E	4/4E	5/4F	6/4F
MUL (2-op)	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULU (2-op)	3/6C	4/6D	3/6E	3/6E	4/6F	5/6F
DIV	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVU	3/8C	4/8D	3/8E	3/8E	4/8F	5/8F
MULB (3-op)	5/(2)	5/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULUB (3-op)	4/5C	4/5D	4/5E	4/5E	5/5F	6/5F
MULB (2-op)	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULUB (2-op)	3/7C	3/7D	3/7E	3/7E	4/7F	5/7F
DIVB	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVUB	3/9C	3/9D	3/9E	3/9E	4/9F	5/9F
AND (3-op)	4/40	5/41	4/42	4/42	5/43	6/43
AND (2-op)	3/60	4/61	3/62	3/62	4/63	5/63
OR (2-op)	3/80	4/81	3/82	3/82	4/83	5/83
XOR	3/84	4/85	3/86	3/86	4/87	5/87
ANDB (3-op)	4/50	4/51	4/52	4/52	5/53	5/53
ANDB (2-op)	3/70	3/71	3/72	3/72	4/73	4/73
ORB (2-op)	3/90	3/91	3/92	3/92	4/93	5/93
XORB	3/94	3/95	3/96	3/96	4/97	5/97
PUSH	2/C8	3/C9	2/CA	2/CA	3/CB	4/CB
POP	2/CC	—	2/CE	2/CE	3/CF	4/CF
LD	3/A0	4/A1	3/A2	3/A2	4/A3	5/A3
LDB	3/B0	3/B1	3/B2	3/B2	4/B3	5/B3
ST	3/C0	—	3/C2	3/C2	4/C3	5/C3
STB	3/C4	—	3/C6	3/C6	4/C7	5/C7

9.0 INSTRUCTION LENGTH/OPCODES (Continued)

Mnemonic	Direct	Immed	Indirect		Indexed	
			Normal(1)	A-Inc(1)	Short(1)	Long(1)
XCH	3/04	—	—	—	4/0B	5/0B
XCHB	3/14	—	—	—	4/1B	5/1B
LDBSE	3/BC	3/BD	3/BE	3/BE	4/BF	5/BF
LBSZE	3/AC	3/AD	3/AE	3/AE	4/AF	5/AF

Mnemonic	Length/Opcode
PUSHF	1/F2
POPF	1/F3
PUSHA	1/F4
POPA	1/F5
TRAP	1/F7
LCALL	3/EF
SCALL	2/28-2F(3)
RET	1/F0
LJMP	3/E7
SJMP	2/20-27(3)
BR[ ]	2/E3
TIJMP	4/E2
JNST	1/D0
JST	1/D8
JNH	1/D1
JH	1/D9
JGT	1/D2
JLE	1/DA
JNC	1/B3
JC	1/D8
JNVT	1/D4
JVT	1/DC
JNV	1/D5
JV	1/DD
JGE	1/D6
JLT	1/DE
JNE	1/D7
JE	1/DF
JBC	3/30-37
JBS	3/38-3F

Mnemonic	Length/Opcode
DJNZ	3/E0
DJNZW	3/E1
NORML	3/0F
SHRL	3/0C
SHLL	3/0D
SHRAL	3/0E
SHR	3/08
SHRB	3/18
SHL	3/09
SHLB	3/19
SHRA	3/0A
SHRAB	3/1A
CLRC	1/F8
SETC	1/F9
DI	1/FA
EI	1/FB
DPTS	1/EC
EPTS	1/ED
CLRVT	1/FC
NOP	1/FD
RST	1/FF
SKIP	2/00
IDLPD	1/F6
BMOV	3/C1
BMOVi	3/CD

NOTES:
1. Indirect and indirect + share the same opcodes, as do short and long indexed opcodes. If the second byte is even, use indirect or short indexed. If odd, use indirect or long indexed.
2. The opcodes for signed multiply and divide are the unsigned opcode with an "FE" prefix.
3. The 3 least significant bits of the opcode are concatenated with the 8 bits to form an 11-bit, 2's complement offset.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES)

Instruction	Direct	Immediate	Indirect		Indexed	
			Normal	A-Inc	Short	Long
ADD (3op)	5	6	7/10	8/11	7/10	8/11
SUB (3op)	5	6	7/10	8/11	7/10	8/11
ADD (2op)	4	5	6/8	7/9	6/8	7/9
SUB (2op)	4	5	6/8	7/9	6/8	7/9
ADDC	4	5	6/8	7/9	6/8	7/9
SUBC	4	5	6/8	7/9	6/8	7/9
CMP	4	5	6/8	7/9	6/8	7/9
ADDB (3op)	5	5	7/10	8/11	7/10	8/11
SUBB (3op)	5	5	7/10	8/11	7/10	8/11
ADDB (2op)	4	4	6/8	7/9	6/8	7/9
SUBB (2op)	4	4	6/8	7/9	6/8	7/9
ADDCB	4	4	6/8	7/9	6/8	7/9
SUBCB	4	4	6/8	7/9	6/8	7/9
CMPB	4	4	6/8	7/9	6/8	7/9
CMPL	7					
MUL (3op)	16	17	18/21	19/22	19/22	20/23
MULU (3op)	14	15	16/19	17/20	17/20	18/21
MUL (2op)	16	17	18/21	19/22	19/22	20/23
MULU (2op)	14	15	16/19	17/20	17/20	18/21
DIV	26	27	28/31	29/32	29/32	30/33
DIVU	24	25	26/29	27/30	27/30	28/31
MULB (3op)	12	12	14/17	15/18	15/18	16/19
MULUB (3op)	10	10	12/15	12/16	12/16	14/17
MULB (2op)	12	12	14/17	15/18	15/18	16/19
MULUB (2op)	10	10	12/15	12/16	12/16	14/17
DIVB	18	18	20/23	21/24	21/24	22/25
DIVUB	16	16	18/21	19/22	19/22	20/23
AND (3op)	5	6	7/10	8/11	7/10	8/11
AND (2op)	4	5	6/8	7/9	6/8	7/9
OR	4	5	6/8	7/9	6/8	7/9
XOR	4	5	6/8	7/9	6/8	7/9
ANDB (3op)	5	5	7/10	8/11	7/10	8/11
ANDB (2op)	4	4	6/8	7/9	6/8	7/9
ORB	4	4	6/8	7/9	6/8	7/9
XORB	4	4	6/8	7/9	6/8	7/9
LD	4	5	5/8	6/8	6/9	7/10
ST	4		5/8	6/9	6/9	7/10
XCH	5				8/13	9/14
LDB	4	4	5/8	6/8	6/9	7/10
STB	4		5/8	6/9	6/9	7/10
XCHB	5				8/13	9/14

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed	
			Normal	A-Inc	Short	Long
BMOV	6 + 8 per Word		6 + 11/14 per Word			
BMOVI	7 + 8 per Word +14 for Each Interrupt		7 + 11/14 per Word +14 for Each Interrupt			
LDBSE, LDBZE	4	4	5/7	6/8	6/8	7/9
PUSH (int)	6	7	9/12	10/13	10/13	11/14
POP (int)	8		10/12	11/13	11/13	12/14
PUSHF (int)	6					
POPF (int)	7					
PUSHA (int)	12					
POPA (int)	12					
PUSH (ext)	8	9	11/14	12/15	12/15	13/16
POP (ext)	11		13/15	14/16	14/16	15/17
PUSHF (ext)	8					
POPF (ext)	10					
PUSHA (ext)	18					
POPA (ext)	18					
LJMP	7					
SJMP	7					
BR[indirect]	7					
TIJMP	15 (+3 for External Reference)					
TRAP (int)	16					
LCALL (int)	11					
SCALL (int)	11					
RET (int)	11					
TRAP (ext)	18					
LCALL (ext)	13					
SCALL (ext)	13					
RET (ext)	14					
JNST, JST	4/8 Jump Not Taken/Jump Taken					
JNH, JH	4/8 Jump Not Taken/Jump Taken					
JGT, JLE	4/8 Jump Not Taken/Jump Taken					
JNC, JC	4/8 Jump Not Taken/Jump Taken					
JNVT, JVT	4/8 Jump Not Taken/Jump Taken					
JNV, JV	4/8 Jump Not Taken/Jump Taken					
JGE, JLT	4/8 Jump Not Taken/Jump Taken					
JNE, JE	4/8 Jump Not Taken/Jump Taken					
JBS, JBC	5/9 Jump Not Taken/Jump Taken					
DJNZ	5/9 Jump Not Taken/Jump Taken					
DJNZW	6/10 Jump Not Taken/Jump Taken					

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed	
			Normal	A-Inc	Short	Long
CLR, NOT, NEG	3					
DEC, INC	3					
EXT	4					
CLRB, NOTB	3					
DECB, INCB	3					
NEGB	3					
EXTB	4					
NORML	8 + 1 per Shift (9 for 0 Shift)					
SHRL	7 + 1 per Shift (8 for 0 Shift)					
SHLL	7 + 1 per Shift (8 for 0 Shift)					
SHRAL	7 + 1 per Shift (8 for 0 Shift)					
SHR	6 + 1 per Shift (7 for 0 Shift)					
SHL	6 + 1 per Shift (7 for 0 Shift)					
SHRA	6 + 1 per Shift (7 for 0 Shift)					
SHRB	6 + 1 per Shift (7 for 0 Shift)					
SHLB	6 + 1 per Shift (7 for 0 Shift)					
SHRAB	6 + 1 per Shift (7 for 0 Shift)					
CLRC	2					
SETC	2					
DI	2					
EI	2					
DPTS	2					
EPTS	2					
CLRVT	2					
NOP	2					
RST	20 (Includes Fetch of CCB0/CCB1)					
SKIP	3					
IDLPD	8/25 (Proper Key/Improper Key)					
PTS						
Single Transfer	18	(+3 for Ext Reference, + 1 If XFER Count = 0)				
Burst Transfer	13	(+7 for Each Transfer, 1 Minimum +3 for Each Memory Controller Reference)				
PWM Modes	15					
A/D Scan Mode	21/25					

NOTES:
The timing figures are minimum execution times expressed as state times (one period of CLKOUT = two oscillator periods) and are based on the following assumptions:
1. The opcode, along with any required operands, have been pre-fetched and reside in the instruction queue.
2. The bus controller operates with the 16-bit bus selected and without wait states for external memory references and pre-fetches. For instructions with indirect or indexed addressing, execution times separated by a slash are for instructions requiring a fetch from internal/external memory.
3. Times for jumps, calls and returns include the 4 state times required to flush the pre-fetch queue and to fetch the opcode at the destination address. This is reflected in the jump taken/not-taken times shown in the table.

11.0 INTERRUPT TABLE

Name	Source	Vector	Priority
INT15	NMI	203EH	32 (Highest)
PTS14	EXTINT Pin	205CH	31
PTS13	Reserved	205AH	30
PTS12	Receive SIO	2058H	29
PTS11	Transmit SIO	2056H	28
PTS10	SSIO Channel 1 Transfer	2054H	27
PTS09	SSIO Channel 0 Transfer	2052H	26
PTS08	Command Buffer Full (SLP)	2050H	25
PTS07	Input Buffer Full (SLP)	204EH	24
PTS06	Output Buffer Empty (SLP)	204CH	23
PTS05	A/D Conversion Complete	204AH	22
PTS04	EPA0	2048H	21
PTS03	EPA1	2046H	20
PTS02	EPA2	2044H	19
PTS01	EPA3	2042H	18
PTS00	EPA4–9, Overrun (EPA0–9), Compare0–1, Timer Overflow	2040H	17
INT14	EXTINT Pin	203CH	16
INT13	Reserved	203AH	15
INT12	Receive SIO	2038H	14
INT11	Transmit SIO	2036H	13
INT10	SSIO Channel 1 Transfer	2034H	12
INT09	SSIO Channel 0 Transfer	2032H	11
INT08	Command Buffer Full (SLP)	2030H	10
N/A	UNIMPLEMENTED OPCODE	2012H	09
N/A	TRAP	2010H	08
INT07	Input Buffer Full (SLP)	200EH	07
INT06	Output Buffer Empty (SLP)	200CH	06
INT05	A/D Conversion Complete	200AH	05
INT04	EPA0	2008H	04
INT03	EPA1	2006H	03
INT02	EPA2	2004H	02
INT01	EPA3	2002H	01
INT00	EPA4–9, Overrun (EPA0–9), Compare0–1, Timer Overflow	2000H	00 (Lowest)

12.0 FORMULAS

State Time = 2 Oscillator Periods

TIJMP Calculation—

Destination = ([INDEX] AND INDEX_MASK) × 2 + [TBASE]

EPA Prescaler—

P2	P1	P0	
0	0	0	÷ 1
0	0	1	÷ 2
0	1	0	÷ 4
0	1	1	÷ 8
1	0	0	÷ 16
1	0	1	÷ 32
1	1	0	÷ 64
1	1	1	Reserved

SIO Baud Rate—

Modes 1, 2 and 3

$$SP\_BAUD = \frac{XTAL1\ Frequency}{Baud\ Rate \times 16} - 1 \qquad (B \geq 0, SP\_BAUD.15 = 1)$$

$$SP\_BAUD = \frac{T1CLK\ Frequency}{Baud\ Rate \times 8} - 1 \qquad (B > 0, SP\_BAUD.15 = 0)$$

Mode 0

$$SP\_BAUD = \frac{XTAL1\ Frequency}{Baud\ Rate \times 2} - 1 \qquad (B > 0, SP\_BAUD.15 = 1)$$

$$SP\_BAUD = \frac{T1CLK\ Frequency}{Baud\ Rate} - 1 \qquad (B > 0, SP\_BAUD.15 = 0)$$

SSIO Baud Rate—

$$SSIO.0 - SSIO.6 = \frac{XTAL1\ Frequency}{Baud\ Rate \times 8} - 1$$

A/D—

Sample States = 4 × SAM + 1
(SAM = AD_TIME.5 − AD_TIME.7)

Conversion States = B × (CONV + 1) + 1.5
(CONV = AD_TIME.0 − AD_TIME.4)
(B = 8 for 8-Bit Conversion)
(B = 10 for 10-Bit Conversion)

Total Conversion Time = State Time × [(4 × SAM) + (B × (CONV + 1)) + 2.5]

Programming Pulse Width—

$$PPR = \frac{((PPW) \times (FOSC)) - 144}{144} + 32768$$

13.0 RESET STATUS

SFR	Reset Value
AD_RESULT	7F80H
AD_COMMAND	0C0H
AD_TEST	0C0H
AD_TIME	0FFH
SSIO0_BUF, SSIO1_BUF	00H
SSIO0_CON, SSIO1_CON	00H
SSIO_BAUD (Baud Rate Control (Read))	0XXXXXXXB
SSIO_BAUD (Baud Rate Down Count (Write))	00H
SBUF_RX, SBUF_TX	00H
SP_STAT	0BH
SP_CON	EOH
SP_BAUD	0000H
COMP0_CON, COMP1_CON	00H
COMP0_TIME, COMP1_TIME	0000H
EPA1_CON, EPA3_CON	0000H
EPAx_CON (x = 0, 2, 4–9)	00H
EPAx_TIME (x = 0–9)	0000H
TIMER1, TIMER2	0000H
T1CONTROL, T2CONTROL	00H
EPA_MASK, EPA_MASK1	00H
EPA_PEND, EPA_PEND1	00H
EPAIPV	00H
P0_PIN, P1_PIN, P3_PIN, P4_PIN, P6_PIN	XXH
P1_MODE, P6_MODE	00H
P1_DIR, P5_DIR, P6_DIR	0FFH
P1_REG, P3_REG, P4_REG, P5_REG, P6_REG	0FFH
P2_PIN, P5_PIN	1XXXXXXXB
P2_MODE, P5_MODE	80H
P2_DIR, P2_REG	7FH
INT_MASK, INT_PEND	00H
INT_MASK1, INT_PEND1	00H
PTSSRV, PTSSEL	0000H
WSR	00H

Pin States, during Reset, Idle and Powerdown

Pin Name	Reset	Idle	PD
$\overline{\text{RESET}}$	wk1	wk1	wk1
ALE (P5.0)	wk1	(A)	(A)
INST (P5.1)	wk0	(A)	(A)
$\overline{\text{RD}}$ (P5.3), $\overline{\text{WR}}$ (P5.2), SPLINT (P5.4)	wk1	(I)	(I)
$\overline{\text{BHE}}$ (P5.5)	wk1	(B)	(B)
READY (P5.6), BUSW (P5.7)	wk1	(C)	(C)
$\overline{\text{EA}}$, NMI	HZ	HZ	HZ
P3, P4/AD (EA = 0)	wk1	HZ	HZ
P3, P4/AD (EA = 1)	wk1	ODIO	ODIO
ACH/PO	HZ	HZ	HZ
P1	wk1	(D)	(D)
CLKOUT (P2.7)	clk, LZ	(E)	(G)
P2.0–P2.6	wk1	(E)	(E)
P6.0–P6.7	wk1	(F)	(F)
V_{PP}	HZ	1, LZ	1, LZ
XTAL1	HZ	HZ	HZ
XTAL2	osc, LZ	osc, LZ	(H)

NOTES:
(A) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 1, then LZ 0. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 0, then HZ.
(B) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 1, then LZ 1. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 0, then HZ.
(C) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1, then HZ.
(D) If P1_MODE.x = 0, port is as programmed. If P1_MODE.x = 1, pin is as specified by P1_DIR and associated peripheral.
(E) If P2_MODE.x = 0, port is as programmed. If P2_MODE.x = 1, pin is as specified by P2_DIR and associated peripheral.
(F) If P6_MODE.x = 0, port is as programmed. If P6_MODE.x = 1, pin is as specified by P6_DIR and associated peripheral.
(G) If P2_MODE.7 = 0, port is as programmed. If P2_MODE.7 = 1, then LZ 0.
(H) If XTAL1 = 1, then LZ 0. IF XTAL1 = 0, then LZ 1.
(I) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1, then pin is as specified by P5_DIR and associated peripheral.
HZ = High impedance
LZ = Low Impedance
wk1 = Weakly pulled high
ODIO = Open drain input/output
osc = Oscillator
wk0 = Weakly pulled low

intel®

8XC196KT
Quick Reference

October 1992
Order Number: 272269-001

8XC196KT Quick Reference

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1.0 MEMORY MAP

0FFFFH A000H	24 Kbytes External Memory
9FFFH 2080H	Internal ROM/EPROM or External Memory
207FH 205EH	Reserved
205DH 2050H	PTS Vectors
203FH 2030H	Interrupt Vector (Upper)
202FH 2020H	ROM/EPROM Security Key
201FH 201CH	Reserved. Must = 0FFH
201BH	Reserved. Must = 20H
201AH	CCB1
2019H	Reserved. Must = 20H
2018H	CCB0
2017H 2014H	Reserved. Must = 0FFH
2013H 2000H	Interrupt Vectors (Lower)
1FFFH 1F00H	Internal SFR's
1EFFH 0600H	External Memory
05FFH 0400H	Internal RAM
03FFH 0000H	Register File

2.0 SFR MAP

CPU Special Function Registers

17H	(Reserved)	0BH	(Reserved)
16H	(Reserved)	0AH	WATCHDOG
15H	(Reserved)	09H	INT_PEND
14H	WSR	08H	INT_MASK
13H	INT_MASK1	07H	PTSSRV (Hi)
12H	INT_PEND1	06H	PTSSRV (Lo)
11H	(Reserved)	05H	PTSSEL (Hi)
10H	(Reserved)	04H	PTSSEL (Lo)
0FH	(Reserved)	03H	Read as FFH
0EH	(Reserved)	02H	Read as FFH
0DH	(Reserved)	01H	ZERO_REG (Hi)
0CH	(Reserved)	00H	ZERO_REG (Lo)

Memory Mapped I/O SFRs

	HIGH BYTE	LOW BYTE
1FFEH	P4_PIN	P3_PIN
1FFCH	P4_REG	P3_REG
1FFAH	SLP_CON	SLP_CMD
1FF8H	(Reserved)	SLP_STAT
1FF6H	P5_PIN	USFR
1FF4H	P5_REG	(Reserved)
1FF2H	P5_DIR	(Reserved)
1FF0H	P5_MODE	(Reserved)
1FE0H	(Reserved)	IRAM_REG

Port 0, Port 1 and Port 6 SFRs

	HIGH BYTE	LOW BYTE
1FDEH	(Reserved)	(Reserved)
1FDCH	(Reserved)	(Reserved)
1FDAH	(Reserved)	P0_PIN
1FD8H	(Reserved)	(Reserved)
1FD6H	P6_PIN	P1_PIN
1FD4H	P6_REG	P1_REG
1FD2H	P6_DIR	P1_DIR
1FD0H	P6_MODE	P1_MODE

Port 2 SFRs

	HIGH BYTE	LOW BYTE
1FCEH	P2_PIN	(Reserved)
1FCCH	P2_REG	(Reserved)
1FCAH	P2_DIR	(Reserved)
1FC8H	P2_MODE	(Reserved)

Serial I/O and Synchronous SIO SFRs

	HIGH BYTE	LOW BYTE
1FBEH	(Reserved)	(Reserved)
1FBCH	SP_BAUD (Hi)	SP_BAUD (Lo)
1FBAH	SP_CON	SBUF_TX
1FB8H	SP_STATUS	SBUF_RX
1FB6H	(Reserved)	(Reserved)
1FB4H	(Reserved)	SSIO_BAUD
1FB2H	SSIO0_CON	SSIO0_BUF
1FB0H	SSIO1_CON	SSIO1_BUF

A/D and EPA Interrupt SFRs

	HIGH BYTE	LOW BYTE
1FAEH	AD_TIME	AD_TEST
1FACH	AD_COMMAND (Hi)	AD_COMMAND (Lo)
1FAAH	AD_RESULT (Hi)	AD_RESULT (Lo)
1FA8H	(Reserved)	EPAIPV
1FA6H	(Reserved)	EPA_PEND1
1FA4H	(Reserved)	EPA_MASK1
1FA2H	EPA_PEND (Hi)	EPA_PEND (Lo)
1FA0H	EPA_MASK (Hi)	EPA_MASK (Lo)

Timer 1 and Timer 2 SFRs

	HIGH BYTE	LOW BYTE
1F9EH	TIMER2 (Hi)	TIMER2 (Lo)
1F9CH	(Reserved)	T2CONTROL
1F9AH	TIMER1 (Hi)	TIMER1 (Lo)
1F98H	(Reserved)	T1CONTROL

EPA SFRs

	HIGH BYTE	LOW BYTE
1F8EH	COMP1_TIME (Hi)	COMP1_TIME (Lo)
1F8CH	(Reserved)	COMP1_CON
1F8AH	COMP0_TIME (Hi)	COMP0_TIME (Lo)
1F88H	(Reserved)	COMP0_CON
1F86H	EPA9_TIME (Hi)	EPA9_TIME (Lo)
1F84H	(Reserved)	EPA9_CON
1F82H	EPA8_TIME (Hi)	EPA8_TIME (Lo)
1F80H	(Reserved)	EPA8_CON
1F7EH	EPA7_TIME (Hi)	EPA7_TIME (Lo)
1F7CH	(Reserved)	EPA7_CON
1F7AH	EPA6_TIME (Hi)	EPA6_TIME (Lo)
1F78H	(Reserved)	EPA6_CON
1F76H	EPA5_TIME (Hi)	EPA5_TIME (Lo)
1F74H	(Reserved)	EPA5_CON
1F72H	EPA4_TIME (Hi)	EPA4_TIME (Lo)
1F70H	(Reserved)	EPA4_CON
1F6EH	EPA3_TIME (Hi)	EPA3_TIME (Lo)
1F6CH	EPA3_CON (Hi)	EPA3_CON (Lo)
1F6AH	EPA2_TIME (Hi)	EPA2_TIME (Lo)
1F68H	(Reserved)	EPA2_CON
1F66H	EPA1_TIME (Hi)	EPA1_TIME (Lo)
1F64H	EPA1_CON (Hi)	EPA1_CON (Lo)
1F62H	EPA0_TIME (Hi)	EPA0_TIME (Lo)
1F60H	(Reserved)	EPA0_CON

3.0 SFR BIT SUMMARY

EPAx_CONTROL

8	7	6	5	4	3	2	1	0
RM	TB	CE	M1	M0	RE	AD	ROT	ON/RT

RM: "1" Enables Remapping (EPA1 & EPA3 Only)
TB: "0" Selects Timer1, "1" Selects Timer2
CE: "0" Disables Comparator, "1" Enables Comparator
M1, M0: Mode Bits

M1, M0	Capture:	Compare:
00	No Op	Interrupt Only
01	Capture Negative	Output "0"
10	Capture Positive	Output "1"
11	Capture All Edges	Toggle Output

RE: Reenable Entry = "1" (Lock Entry)
AD: Start A/D
ROT: Reset Opposite Time Base
ON/RT: Overrun and Reset Timer Enable

EPAIPV 1FA8H: Byte

7	6	5	4	3	2	1	0
0	0	0	PV4	PV3	PV2	PV1	PV0

PV4–PV0: Returns the encoded highest priority interrupt. Value from 1H–14H.

0H = No Interrupt Pending	0AH = OVRINT4
14H = EPAINT4	09H = OVRINT5
13H = EPAINT5	08H = OVRINT6
12H = EPAINT6	07H = OVRINT7
11H = EPAINT7	06H = OVRINT8
10H = EPAINT8	05H = OVRINT9
0FH = EPAINT9	04H = Compare Channel 0
0EH = OVRINT0	03H = Compare Channel 1
0DH = OVRINT1	02H = TIMER1 Overflow
0CH = OVRINT2	01H = TIMER2 Overflow
0BH = OVRINT3	

SP_CON 1FBBH: Byte

7	6	5	4	3	2	1	0
X	X	X	TB8	REN	PEN	M2	M1

TB8: 9th Bit for Transmission
REN: Enables the Receiver
PEN: Enables Parity (Even)
M2, M1:
00: Mode 0/Sync
01: Mode 1/Async (std)
10: Mode 2/Async (9th Bit Enable)
11: Mode 3/Async (9th Bit Data)

SP_BAUD 1FBCH: Word

Mode 0:

$$\frac{XTAL1}{Baud * 2} - 1$$

or

$$\frac{T1CLK}{Baud}$$

Mode 1, 2, 3:

$$\frac{XTAL}{Baud * 16} - 1$$

or

$$\frac{T1CLK}{Baud * 8}$$

PORT 1/2/5/6 Control

Px_MODE = "1" for Peripheral Control
Px_MODE = "0" for Standard Port
Px_DIR = "1" for INPUT or OPEN DRAIN OUTPUT
Px_DIR = "0" for OUTPUT (PUSH/PULL)
Px_PIN is for PORT READs
Px_REG is for PORT WRITEs

TxCONTROL 1F98H: Byte = T1
1F9CH: Byte = T2

7	6	5	4	3	2	1	0
CE	UD	M2	M1	M0	P2	P1	P0

CE: "0" Disables Timer, "1" Enables Timer
UD: "0" Counts Down, "1" Counts Up

M2, M1, M0—Mode Bits

000	Clock = Internal/Direction = UD
x01	Clock = External/Direction = UD
010	Clock = Internal/Direction = TxDIR
011	Clock = External/Direction = TxDIR
100	Clock = T1 Overflow/Direction = UD
110	Clock = T1 Overflow/Direction = T1
111	Quadrature Count (TxCLK/TxDIR)

P2, P1, P0—Prescale Bits

000	÷ 1 (250 ns @ 16 MHz) Xtal*4
001	÷ 2 (500 ns @ 16 MHz) Xtal*8
010	÷ 4 (1 μs @ 16 MHz) Xtal*16
011	÷ 8 (2 μs @ 16 MHz) Xtal*32
100	÷ 16 (4 μs @ 16 MHz) Xtal*64
101	÷ 32 (8 μs @ 16 MHz) Xtal*128
110	÷ 64 (16 μs @ 16 MHz) Xtal*256
111	Reserved

INT_MASK/INT_MASK1 **08H/13H: Byte** **PTS_SRV** 06: Word
INT_PEND/INT_PEND1 **09H/12H: Byte** **PTS_SELECT** 04H: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rsv	EXT INT	rsv	RI	TI	SSIO1	SSIO0	CBF	IBF	OBE	A/D Done	INT EPA0	INT EPA1	INT EPA2	INT EPA3	INT EPAX

AD_TEST 1FAEH: Byte

7	6	5	4	3	2	1	0
0	0	0	0	OF1	OF0	V_{REF}	A_{GND}

A_{GND}: Convert on AnGND
V_{REF}: Convert on V_{REF}
OF1, OF0: Offset Adjust
00: No Adjustment
01: ADD 2.5 mV
10: SUB 2.5 mV
11: SUB 5.0 mV

SP_STATUS 1FB9H: Byte

7	6	5	4	3	2	1	0
RB8/RPE	RI	TI	FE	TXE	OE	X	X

RP8: Set if 9th Bit set (No Parity)
RPE: Set if Parity Enabled and Parity Error
RI: Set after Last Data Bit Received
TI: Set at Beginning of STOP Bit
FE: Set if No STOP Bit Found
TXE: Set when Byte is in SBUF_TX
OE: Set if Overrun Error Occurred

AD_TIME 1FAFH: Byte

7	6	5	4	3	2	1	0
Sample Time				Conversion Time (CONV)			

SAM = 1 to 7 CONV = 2 to 31

Total Conversion Time:
T = (4 * SAM) + (B*(CONV + 1) + 2.5)
Where B = 8 for 8-Bit, 10 for 10-Bit

AD_COMMAND 1FACH: Byte/Word

7	6	5	4	3	2	1	0
0	0	T	M	GO	Channel #		

Channel # = 0 to 7
GO: "1" to Start Now/"0" for EPA Start
M: "0" = 10-Bit/"1" = 8-Bit Conversion
"0" = Detect High/"1" = Detect Low
T: "0" = Normal Conversion/"1" = Threshold Detect

EPA_MASK1/EPA_PEND1 1FA4H/1FA6H: Byte
EPA_MASK/EPA_PEND 1FA0H/1FA2H: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT EPA4	INT EPA5	INT EPA6	INT EPA7	INT EPA8	INT EPA9	OVR EPA0	OVR EPA1	OVR EPA2	OVR EPA3	OVR EPA4	OVR EPA5	OVR EPA6	OVR EPA7	OVR EPA8	OVR EPA9

7	6	5	4	3	2	1	0
rsv	rsv	rsv	rsv	COMP CH0	COMP CH1	OVR TIMR1	OVR TIMR2

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CCB (2018H : Byte)

0	PD	=	"1" Enables Powerdown
1	BW0	=	See Table
2	WR	=	"1" = $\overline{WR}$/BHE; "0" = $\overline{WRL}$/$\overline{WRH}$
3	ALE	=	"1" = ALE - "0" = $\overline{ADV}$
4	IRC0	=	See Table
5	IRC1	=	
6	LOC0	=	See Table
7	LOC1	=	

CCB1 (201AH : Byte)

0	0	=	Reserved Must Be "0"
1	IRC2	=	See Table
2	BW1	=	See Table
3	WDE	=	"0" = Always Enabled
4	1	=	Reserved Must Be "01"
5	0	=	
6	MSEL0	=	See Table
7	MSEL1	=	

LOC1	LOC0	Function
0	0	Read and Write Protected
0	1	Write Protected Only
1	0	Read Protected Only
1	1	No Protection

IRC2	IRC1	IRC0	Max Wait States
0	0	0	Zero Wait States
1	0	0	1 Wait State
1	0	1	2 Wait States
1	1	0	3 Wait States
1	1	1	INFINITE

MSEL1	MSEL0	Bus Timing Mode
0	0	Mode 0 (1-Wait KR)
0	1	Mode 1 (Long R/W)
1	0	Mode 2 (Early Address)
1	1	Mode 3 (KR Compatible)

BW1	BW0	Bus Width
0	0	ILLEGAL
0	1	16-Bit Only
1	0	8-Bit Only
1	1	BW Pin Controlled

SLP_CON 1FFBH: Byte

7	6	5	4	3	2	1	0
0	0	0	0	SLP	SLPL	IBEmask	OBFmask

SLP = 1 Enables Slave Port Operation
= 0 Disables Slave Port Operation and Clears Bits, CBE, IBE, and OBF in SLP_STAT

SLPL = 1 ALE Latches SLP_ADDR from AD1 (P3.1)
= 0 ALE is SLP_ADDR

IBEmask = 1 IBE Can Affect SLPINT
= 0 IBE Cannot Affect SLPINT

OBFmask = 1 OBF Can Affect SLPINT
= 0 OBF Cannot Affect SLPINT

SLP_STAT 1FF8H: Byte

7	6	5	4	3	2	1	0
STAT					CBE	IBE	OBF

STAT These bits are written by the 8XC196KT user and defined by the 8XC196KT user for communication flags.

CBE (Command Buffer Empty)
= 1 After 8XC196KT Reads SLPCMD
= 0 After Master Writes to SLPCMD or SLP = 0 in SLP_CON

IBE (Input Buffer Empty)
= 1 After 8XC196KT Reads SLPDIN
= 0 After Master Writes to SLPDIN, or SLP = 0 in SLP_CON

OBF (Output Buffer Full)
= 1 After 8XC196KT Writes to SLPDOUT
= 0 After Master Reads SLPDOUT

USFR 1FF6H (Read Only): Byte

7	6	5	4	3	2	1	0
RSV	RSV	RSV	DEI	DED	RSV	RSV	RSV

NOTE:
Do not write to location 1FF6H. Bits DED and DEI are written as specified in users manual.

Device	DEI	DED
87C196KR	UPROM Bit	UPROM Bit
83C196KR	N/A	N/A

DED—Disable External Data
DEI—Disable External Instructions

SSIOx_CON Registers 1FB1H: Byte = SSIO0
1FB3H: Byte = SSIO1

7	6	5	4	3	2	1	0
M/$\overline{S}$	T/$\overline{R}$	TRT	THS	STE	ATR	OUF	TBS

M/$\overline{S}$ Master/$\overline{Slave}$
T/$\overline{R}$ Transmit/$\overline{Receive}$
TRT Transmitter/Receiver Toggle
THS Transceiver Handshake Select
STE Single Transfer Enable
ATR Auto Transfer Re-Enable
OUF Overflow/Underflow Flag
TBS Transceiver/Buffer Status

AD_RESULT 1FAAH: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8 MSB								2 LSB		RSV	RSV	BUSY	A/D Channel		

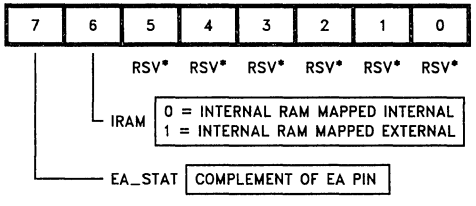
A/D Channel Channel Number: 0–7
BUSY 0 = A/D Idle
1 = A/D in Use
RSV Reserved
2 LSB 2 Least Significant Bits
8 MSB 8 Most Significant Bits
Bit 4, 5 0

WSR 14H: Byte

7	6	5	4	3	2	1	0
HLDEN	Window Select Bits						

HLDEN = 0 Disables HOLD/HLDA
= 1 Enables HOLD/HLDA

IRAM_CON 1FE0H: Byte



272269-1

EA_STAT not effected by write
*RSV—reserved bit must be = 0

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4.0 PIN DEFINITION TABLE

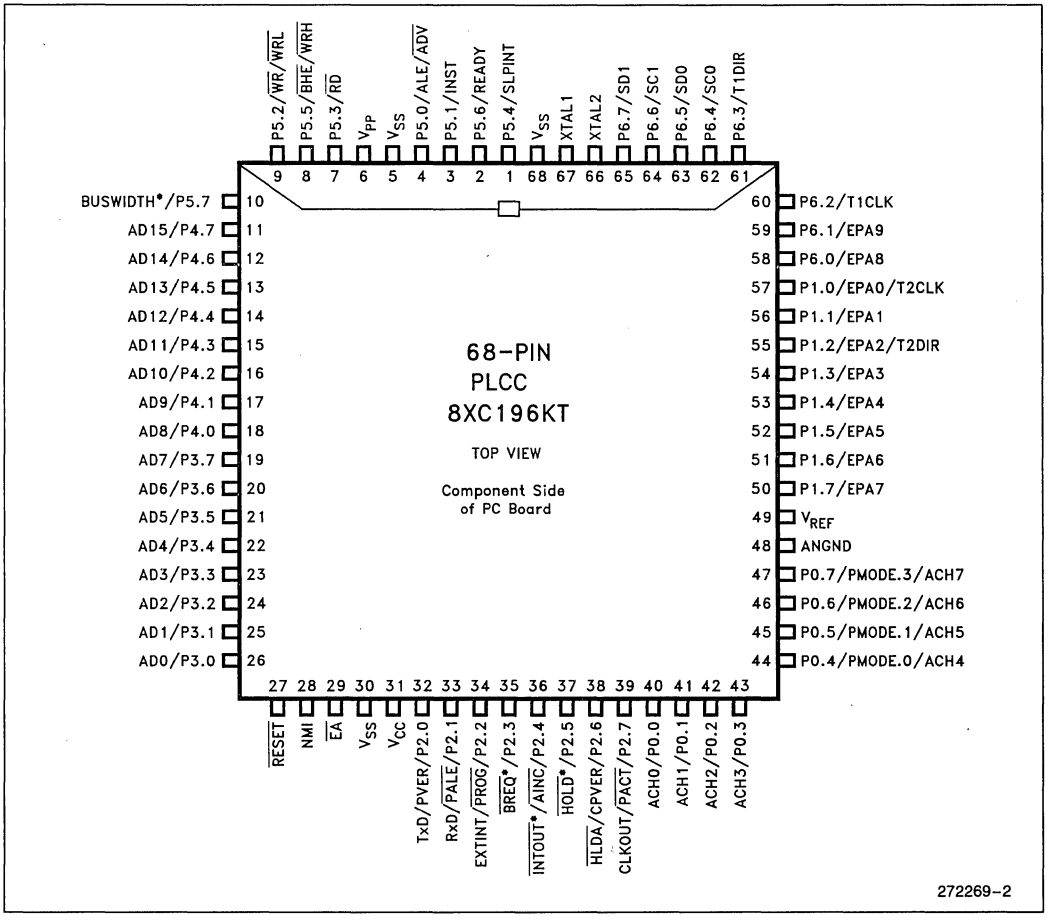
68 PLCC	Function
40	ACH0
41	ACH1
42	ACH2
43	ACH3
44	ACH4
45	ACH5
46	ACH6
47	ACH7
26	AD0
25	AD1
24	AD2
23	AD3
22	AD4
21	AD5
20	AD6
19	AD7
18	AD8
17	AD9
16	AD10
15	AD11
14	AD12
13	AD13
12	AD14
11	AD15
04	$\overline{\text{ADV}}$
36	$\overline{\text{AINC}}$
04	ALE
48	ANGND
08	$\overline{\text{BHE}}$
35	$\overline{\text{BREQ}}$
10	BUSWIDTH
39	CLKOUT
38	CPVER
29	$\overline{\text{EA}}$
57	EPA0
56	EPA1

68 PLCC	Function
55	EPA2
54	EPA3
53	EPA4
52	EPA5
51	EPA6
50	EPA7
58	EPA8
59	EPA9
34	EXTINT
38	$\overline{\text{HLDA}}$
37	$\overline{\text{HOLD}}$
03	INST
36	$\overline{\text{INTOUT}}$
28	NMI
40	P0.0
41	P0.1
42	P0.2
43	P0.3
44	P0.4
45	P0.5
46	P0.6
47	P0.7
57	P1.0
56	P1.1
55	P1.2
54	P1.3
53	P1.4
52	P1.5
51	P1.6
50	P1.7
32	P2.0
33	P2.1
34	P2.2
35	P2.3
36	P2.4

68 PLCC	Function
37	P2.5
38	P2.6
39	P2.7
26	P3.0
25	P3.1
24	P3.2
23	P3.3
22	P3.4
21	P3.5
20	P3.6
19	P3.7
18	P4.0
17	P4.1
16	P4.2
15	P4.3
14	P4.4
13	P4.5
12	P4.6
11	P4.7
04	P5.0
03	P5.1
09	P5.2
07	P5.3
01	P5.4
08	P5.5
02	P5.6
10	P5.7
58	P6.0
59	P6.1
60	P6.2
61	P6.3
62	P6.4
63	P6.5
64	P6.6

68 PLCC	Function
65	P6.7
39	$\overline{\text{PACT}}$
33	$\overline{\text{PALE}}$
44	PMODE.0
45	PMODE.1
46	PMODE.2
47	PMODE.3
34	$\overline{\text{PROG}}$
32	PVER
07	$\overline{\text{RD}}$
02	READY
27	$\overline{\text{RESET}}$
33	RXD
62	SC0
64	SC1
63	SD0
65	SD1
01	SLPINT
60	T1CLK
61	T1DIR
57	T2CLK
55	T2DIR
32	TXD
31	V_{CC}
06	V_{PP}
49	V_{REF}
05	V_{SS}
30	V_{SS}
68	V_{SS}
09	$\overline{\text{WR}}$
08	$\overline{\text{WRH}}$
09	$\overline{\text{WRL}}$
67	XTAL1
66	XTAL2

5.0 PACKAGE PIN ASSIGNMENTS



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6.0 PIN DESCRIPTION

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS1}, V_{SS2}, V_{SS3}	Digital circuit ground (0V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference and supply voltage for the A/D converter and Port0 (+5V). Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from power-down circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, connect V_{PP} to V_{CC}.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
ACH0–ACH7/PORT0	Analog inputs to the on-chip A/D converter. Also a digital input pin.*
ALE/$\overline{ADV}$/P5.0	Address Latch Enable or Address Valid output. Goes low to latch and demultiplex the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle, providing a chip select for external memory. $\overline{ADV}$ is active only during external memory accesses. Also a standard I/O pin.*
$\overline{BHE}$/$\overline{WRH}$/P5.5	Byte High Enable or Write High output. $\overline{BHE}$ = 0 when accessing odd (high) bytes or complete words in external memory. $\overline{WRH}$ = 0 when writing to odd bytes or complete words in external memory. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory cycles. Also a standard I/O pin.*
$\overline{BREQ}$/P2.3	Bus Request output. Active low when the bus controller is in hold and has a pending external memory cycle. Also a standard I/O pin.*
BUSWIDTH/P5.7	Input for bus width selection. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. Also a standard I/O pin.*
CLOCKOUT/P2.7	Output of the internal clock generator. A 50% duty cycle signal at 1/2 XTAL1 frequency. Also a standard I/O pin.*
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ = 1 directs memory accesses from locations 2000H through 9FFFH to on-chip EPROM/ROM. $\overline{EA}$ = 0 directs all memory accesses to off-chip memory. $\overline{EA}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{EA}$ is latched at reset.
EPA0–7/P1.0–1.7 EPA8–9/P6.0–6.1	I/O pins for the Event Processor Array. EPA0 and EPA2 also function as T2CLK and T2DIR. Also a standard I/O pin.*
EXTINT/P2.2	External Interrupt input pin. A positive transition sets the EXTINT interrupt pending flag. The minimum high and low times are 2 oscillator cycles. Also a standard I/O pin.*
INST/P5.1	Instruction fetch signal. Output high during the entire bus cycle of an external instruction fetch. INST is active only during external memory fetches; during internal memory fetches, INST is low. Also a standard I/O pin.*
$\overline{INTOUT}$/P2.4	Interrupt output indicating that a pending interrupt requires use of the external bus. Also a standard I/O pin.*
$\overline{HLDA}$/P2.6	Bus Hold Acknowledge output indicating release of the bus in response to a HOLD request. Also a standard I/O pin.* This is also a TEST MODE enable pin. Do not use it as an input without careful hardware evaluation.

*These pins may be used for the system or peripheral functions or as a standard I/O pin.

6.0 PIN DESCRIPTION (Continued)

Symbol	Name and Function
$\overline{HOLD}$/P2.5	Bus Hold request input. $\overline{HOLD}$ is sent by another processor to request control of 8XC196KT system bus. Also a standard I/O pin.*
NMI	Non-Maskable interrupt input pin. A positive transition causes a non-maskable interrupt vector through memory location 203EH. If not used, this pin should be tied to V_{SS}. May be used by Intel Evaluation boards.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port 0 pins should not be left floating. In EPROM devices these pins are also used to select the Programming Mode.
PORT1	8-bit bidirectional standard I/O port. All of its pins are shared with the EPA.
PORT2	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (TxD, RxD, EXTINT, $\overline{BREQ}$, $\overline{INTOUT}$, $\overline{HOLD}$, $\overline{HLDA}$, $\overline{CLKOUT}$).
PORT3 PORT4	8-bit bidirectional standard I/O with open drain outputs. These pins are shared with the multiplexed address/data bus which uses complementary drivers.
PORT5	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (ALE/ADV, INST, $\overline{WR}$/$\overline{WRL}$, $\overline{RD}$, SLPINT, $\overline{BHE}$/$\overline{WRH}$, READY, BUSWIDTH).
PORT6	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (EPA8, EPA9, T1CLK, T1DIR, SC0, SD0, SC1, SD1).
$\overline{RD}$/P5.3	Read signal output to external memory. $\overline{RD}$ is low only during external memory reads. Also a standard I/O pin.*
READY/P5.6	Ready input to lengthen external memory cycles. If READY = 1, CPU operation continues in a normal manner. If READY = 0 wait states are added. Also a standard I/O pin.*
$\overline{RESET}$	Reset input to the chip. Held low for at least 16 state times to reset the chip. The subsequent low to high transition starts the reset sequence. Input high for normal operation. $\overline{RESET}$ has an internal pullup.
RXD/P2.1	Receive data input pin for the Serial I/O (SIO) port. Also a standard I/O pin.*
SLPINT/P5.4	Slave Port Interrupt output pin. Also a standard I/O pin.*
SSIO/P6.4–P6.7 (SC0, SD0, SC1, SD1)	Synchronous Serial I/O pins. SC0/SC1 are clock pins and SD0/SD1 are data pins. Also a standard I/O pin.*
T1CLK/P6.2	TIMER1 Clock input. TIMER1 increments or decrements on both rising and falling edges. Also a standard I/O pin.*
T1DIR/P6.3	TIMER1 Direction input. TIMER1 increments when this pin is high and decrements when this pin is low. Also a standard I/O pin.*
T2CLK/P1.0	TIMER2 Clock Input. TIMER2 increments or decrements on both rising and falling edges. Also a standard I/O pin.*
T2DIR/P1.2	TIMER2 Direction input. TIMER2 increments when this pin is high and decrements when this pin is low. Also a standard I/O pin.*
TXD/P2.0	Transmit data output pin for the Serial I/O (SIO) port. Also a standard I/O pin.*
$\overline{WR}$/$\overline{WRL}$/P5.2	Write and Write Low output to external memory. $\overline{WR}$ goes low for every external write. $\overline{WRL}$ goes low only for writes to even addresses. $\overline{WR}$/$\overline{WRL}$ is active only during external memory writes. Also a standard I/O pin.*
XTAL1	Input of the oscillator invertor and the internal clock generator. If using an external clock source connect it to this pin.
XTAL2	Output of the oscillator invertor. Leave floating unless connected to a crystal/ resonator circuit.

*These pins may be used for the system or peripheral functions or as a standard I/O pin.

6.0 PIN DESCRIPTION (Continued)

Programming Mode Pin Definitions

Name	Name and Function
PMODE PO.4–7	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by an 8XC196KT that is in Slave Programming Mode. Used to indicate that Port 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge latches data on PBUS and begins programming. Rising edge inputs ends programming.
PACT	Programming Active. Used to indicate when programming activity is complete.
PVER	Programming Verification. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low input enables the auto increment mode. Auto increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
PORTS 3 and 4	Address/Command/Data Bus. Used to pass commands, addresses and data to and from 8XC196KTs. Also used in the Auto Programming Mode as a regular system bus to access external memory.
CPVER	Cumulative Program Verification. Pin is high if all locations since entering a programming mode have programmed correctly.

7.0 OPCODE TABLE

00	SKIP
01	CLR
02	NOT
03	NEG
04	XCH
05	DEC
06	EXT
07	INC
08	SHR
09	SHL
0A	SHRA
0B	XCH
0C	SHRL
0D	SHLL
0E	SHRAL
0F	NORML
10	RESERVED
11	CLRB
12	NOTB
13	NEGB
14	XCHB
15	DECB
16	EXTB
17	INCB
18	SHRB
19	SHLB
1A	SHRAB
1B	XCHB
1C	EST INDIRECT**
1D	EST INDEXED**
1E	ESTB INDIRECT**
1F	ESTB INDEXED**
20	SJMP
21	SJMP
22	SJMP
23	SJMP
24	SJMP
25	SJMP
26	SJMP
27	SJMP
28	SCALL
29	SCALL
2A	SCALL
2B	SCALL
2C	SCALL
2D	SCALL
2E	SCALL

2F	SCALL
30	JBC
31	JBC
32	JBC
33	JBC
34	JBC
35	JBC
36	JBC
37	JBC
38	JBS
39	JBS
3A	JBS
3B	JBS
3C	JBS
3D	JBS
3E	JBS
3F	JBS
40	AND DIRECT (3 OPS)
41	AND IMMEDIATE (3 OPS)
42	AND INDIRECT (3 OPS)
43	AND INDEXED (3 OPS)
44	ADD DIRECT (3 OPS)
45	ADD IMMEDIATE (3 OPS)
46	ADD INDIRECT (3 OPS)
47	ADD INDEXED (3 OPS)
48	SUB DIRECT (3 OPS)
49	SUB IMMEDIATE (3 OPS)
4A	SUB INDIRECT (3 OPS)
4B	SUB INDEXED (3 OPS)
4C	MULU DIRECT (3 OPS)
4D	MULU IMMEDIATE (3 OPS)
4E	MULU INDIRECT (3 OPS)
4F	MULU INDEXED (3 OPS)
50	ANDB DIRECT (3 OPS)
51	ANDB IMMEDIATE (3 OPS)
52	ANDB INDIRECT (3 OPS)
53	ANDB INDEXED (3 OPS)
54	ADDB DIRECT (3 OPS)
55	ADDB IMMEDIATE (3 OPS)
56	ADDB INDIRECT (3 OPS)
57	ADDB INDEXED (3 OPS)
58	SUBB DIRECT (3 OPS)
59	SUBB IMMEDIATE (3 OPS)
5A	SUBB INDIRECT (3 OPS)
5B	SUBB INDEXED (3 OPS)
5C	MULUB DIRECT (3 OPS)
5D	MULUB IMMEDIATE (3 OPS)

5E	MULUB INDIRECT (3 OPS)
5F	MULUB INDEXED (3 OPS)
60	AND DIRECT (2 OPS)
61	AND IMMEDIATE (2 OPS)
62	AND INDIRECT (2 OPS)
63	AND INDEXED (2 OPS)
64	ADD DIRECT (2 OPS)
65	ADD IMMEDIATE (2 OPS)
66	ADD INDIRECT (2 OPS)
67	ADD INDEXED (2 OPS)
68	SUB DIRECT (2 OPS)
69	SUB IMMEDIATE (2 OPS)
6A	SUB INDIRECT (2 OPS)
6B	SUB INDEXED (2 OPS)
6C	MULU DIRECT (2 OPS)
6D	MULU IMMEDIATE (2 OPS)
6E	MULU INDIRECT (2 OPS)
6F	MULU INDEXED (2 OPS)
70	ANDB DIRECT (2 OPS)
71	ANDB IMMEDIATE (2 OPS)
72	ANDB INDIRECT (2 OPS)
73	ANDB INDEXED (2 OPS)
74	ADDB DIRECT (2 OPS)
75	ADDB IMMEDIATE (2 OPS)
76	ADDB INDIRECT (2 OPS)
77	ADDB INDEXED (2 OPS)
78	SUBB DIRECT (2 OPS)
79	SUBB IMMEDIATE (2 OPS)
7A	SUBB INDIRECT (2 OPS)
7B	SUBB INDEXED (2 OPS)
7C	MULUB DIRECT (2 OPS)
7D	MULUB IMMEDIATE (2 OPS)
7E	MULUB INDIRECT (2 OPS)
7F	MULUB INDEXED (2 OPS)
80	OR DIRECT
81	OR IMMEDIATE
82	OR INDIRECT
83	OR INDEXED
84	XOR DIRECT
85	XOR IMMEDIATE
86	XOR INDIRECT
87	XOR INDEXED
88	CMP DIRECT
89	CMP IMMEDIATE
8A	CMP INDIRECT
8B	CMP INDEXED
8C	DIVU DIRECT

7.0 OPCODE TABLE (Continued)

8D	DIVU IMMEDIATE
8E	DIVU INDIRECT
8F	DIVU INDEXED
90	ORB DIRECT
91	ORB IMMEDIATE
92	ORB INDIRECT
93	ORB INDEXED
94	XORB DIRECT
95	XORB IMMEDIATE
96	XORB INDIRECT
97	XORB INDEXED
98	CMPB DIRECT
99	CMPB IMMEDIATE
9A	CMPB INDIRECT
9B	CMPB INDEXED
9C	DIVUB DIRECT
9D	DIVUB IMMEDIATE
9E	DIVUB INDIRECT
9F	DIVUB INDEXED
A0	LD DIRECT
A1	LD IMMEDIATE
A2	LD INDIRECT
A3	LD INDEXED
A4	ADDC DIRECT
A5	ADDC IMMEDIATE
A6	ADDC INDIRECT
A7	ADDC INDEXED
A8	SUBC DIRECT
A9	SUBC IMMEDIATE
AA	SUBC INDIRECT
AB	SUBC INDEXED
AC	LDBZE DIRECT
AD	LDBZE IMMEDIATE
AE	LDBZE INDIRECT
AF	LDBZE INDEXED
B0	LDB DIRECT
B1	LDB IMMEDIATE
B2	LDB INDIRECT
B3	LDB INDEXED

B4	ADDCB DIRECT
B5	ADDCB IMMEDIATE
B6	ADDCB INDIRECT
B7	ADDCB INDEXED
B8	SUBCB DIRECT
B9	SUBCB IMMEDIATE
BA	SUBCB INDIRECT
BB	SUBCB INDEXED
BC	LDBSE DIRECT
BD	LDBSE IMMEDIATE
BE	LDBSE INDIRECT
BF	LDBSE INDEXED
C0	ST DIRECT
C1	BMOV
C2	ST INDIRECT
C3	ST INDEXED
C4	STB DIRECT
C5	CMPL
C6	STB INDIRECT
C7	STB INDEXED
C8	PUSH DIRECT
C9	PUSH IMMEDIATE
CA	PUSH INDIRECT
CB	PUSH INDEXED
CC	POP DIRECT
CD	BMOVI
CE	POP INDIRECT
CF	POP INDEXED
D0	JNST
D1	JNH
D2	JGT
D3	JNC
D4	JNVT
D5	JNV
D6	JGE
D7	JNE
D8	JST
D9	JH

DA	JLE
DB	JC
DC	JVT
DD	JV
DE	JLT
DF	JE
E0	DJNZ
E1	DJNZW
E2	TIJMP
E3	BR (INDIRECT)
E4	EBMOVI**
E5	RESERVED
E6	EJMP**
E7	LJMP
E8	ELD INDIRECT**
E9	ELD INDEXED**
EA	ELDB INDIRECT**
EB	ELDB INDEXED**
EC	DPTS
ED	EPTS
EE	RESERVED
EF	LCALL
F0	RET
F1	ECALL**
F2	PUSHF
F3	POPF
F4	PUSHA
F5	POPA
F6	IDPLD
F7	TRAP
F8	CLRC
F9	SETC
FA	DI
FB	EI
FC	CLRVT
FD	NOP
FE	*DIV/DIVB/MUL/MULB
FF	RST

*Two Byte Instruction - This opcode is placed as the first byte of an instruction to make it a signed operation instead of unsigned.

**These instructions exist for compatibility with future devices, and are not tested on the 8XC196KT.

8.0 INSTRUCTION SET SUMMARY

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D = D + A	↕	↕	↕	↕	↑		
ADD/ADDB	3	D = B + A	↕	↕	↕	↕	↑		
ADDC/ADDCB	2	D = D + A + C	↓	↕	↕	↕	↑		
SUB/SUBB	2	D = D − A	↕	↕	↕	↕	↑		
SUB/SUBB	3	D = B − A	↕	↕	↕	↕	↑		
SUBC/SUBCB	2	D = D − A + C − 1	↓	↕	↕	↕	↑		
CMP/CMPB/CMPL	2	D − A	↕	↕	↕	↕	↑		
MUL/MULU	2	D,D + 2 = D × A							3
MUL/MULU	3	D,D + 2 = B × A							3
MULB/MULUB	2	D,D + 1 = D × A							4
MULB/MULUB	3	D,D + 1 = B × A							4
DIVU	2	D = (D,D + 2)/A,D + 2 = Remainder				↕	↑		3
DIVUB	2	D = (D,D + 1)/A,D + 1 = Remainder				↕	↑		4
DIV	2	D = (D,D + 2)/A,D + 2 = Remainder				↕	↑		
DIVB	2	D = (D,D + 1)/A,D + 1 = Remainder				↕	↑		
AND/ANDB	2	D = D and A	↕	↕	0	0			
AND/ANDB	3	D = B and A	↕	↕	0	0			
OR/ORB	2	D = D or A	↕	↕	0	0			
XOR/XORB	2	D = D (exclusive or) A	↕	↕	0	0			
LD/LDB	2	D = A							
ELD/ELDB	2	D = A							
ST/STB	2	A = D							
EST/ESTB	2	A = D							
XCH	2	D ⟷ A; D + 1 ⟷ A + 1							
XCHB	2	D ⟷ A							
BMOV, BMOVI/EBMOVI	2	(PTR_HI) + = (PTR_LOW) +; Until COUNT = 0							
LDBSE	2	D = A; D + 1 = Sign (A)							4, 5
LDBZE	2	D = A; D + 1 = 0							4, 5
PUSH	1	SP = SP − 2; (SP) = A							
POP	1	A = (SP); SP = SP + 2							
PUSHF	0	SP = SP − 2; (SP) = PSW; PSW = 0; I = 0; PSE = 0	0	0	0	0	0	0	11
POPF	0	PSW = (SP); SP = SP + 2; I ← ↕	↕	↕	↕	↕	↕	↕	11
PUSHA	0	SP = SP − 2; (SP) = PSW; PSW = 0000H; SP = SP − 2; (SP) = IMASK1/WSR; IMASK1 = 00H; I = 0; PSE = 0	0	0	0	0	0	0	
POPA	0	IMASK1/WSR = (SP); SP = SP + 2; PSW = (SP); SP = SP + 2	↕	↕	↕	↕	↕	↕	
SJMP	1	PC = PC + 11-Bit-Offset							6

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8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
LJMP	1	PC = PC + 16-Bit-Offset							6
EJMP	1	PC = PC + 24 = Bit-Offset							6, 12
EBR [Indirect]	1	PC = (A)							12
TIJMP	3	PC = ([index] and MASK)2 + (Table)							
TRAP	0	SP = SP − 2; (SP) = PC; PC = (2010H)							10
ECALL	1	SP = SP − 4; (SP) = PC PC = PC + 20-Bit Offset							6, 12
LCALL (16-Bit Mode)	1	SP = SP − 2; (SP) = PC PC = PC + 16-Bit Offset							6
LCALL (24-Bit Mode)	1	SP = SP − 4; (SP) = PC PC = PC + 16-Bit Offset							6, 13
SCALL (16-Bit Mode	1	SP = SP − 2; (SP) = PC PC = PC + 11-Bit Offset							6
SCALL (24-Bit Mode)	1	SP = SP − 4; (SP) = PC PC = PC + 11-Bit Offset							6, 13
RET (16-Bit Mode)	0	PC = (SP); SP = SP + 2							
RET (24-Bit Mode)	0	PC = (SP); SP = SP + 4							13
J(conditioned)	1	PC = PC + 8-Bit-Offset (If Taken)							6
JC	1	Jump if C = 1							6
JNC	1	Jump if C = 0							6
JE	1	Jump if Z = 1							6
JNE	1	Jump if Z = 0							6
JGE	1	Jump if N = 0							6
JLT	1	Jump if N = 1							6
JGT	1	Jump if N = 0 and Z = 0							6
JLE	1	Jump if N = 1 or Z = 1							6
JH	1	Jump if C = 1 and Z = 0							6
JNH	1	Jump if C = 0 or Z = 1							6
JV	1	Jump if V = 0							6
JNV	1	Jump if V = 1							6
JVT	1	Jump if VT = 1; Clear VT					0		6
JNVT	1	Jump if VT = 0; Clear VT					0		6
JST	1	Jump if ST = 1							6
JNST	1	Jump if ST = 0							6
JBS	3	Jump if Specific Bit = 1							6, 7
JBC	3	Jump if Specific Bit = 0							6, 7
DJNZ/DJNZW	1	D = D − 1; If D ≠ 0 then PC = PC +8-Bit-Offset							6

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
DEC/DECB	1	D = D − 1	✓	✓	✓	✓	↑		
NEG/NEGB	1	D = 0 − D	✓	✓	✓	✓	↑		
INC/INCB	1	D = D + 1	✓	✓	✓	✓	↑		
EXT	1	D = D;D + 2 = Sign (D)	✓	✓	0	0			3
EXTB	1	D = D;D + 1 = Sign (D)	✓	✓	0	0			4
NOT/NOTB	1	D = Logical Not (D)	✓	✓	0	0			
CLR/CLRB	1	D = 0	1	0	0	0			
SHL/SHLB/SHLL	2	C ← msb•••lsb ← 0	✓	✓	✓	✓	↑		8
SHR/SHRB/SHRL	2	0 → msb•••lsb → C	✓	✓	✓	0		✓	8
SHRA/SHRAB/SHRAL	2	msb → msb•••lsb → C	✓	✓	✓	0		✓	8
NORML	2	Left Shift until msb = 1;D = Shift Count	✓	✓	0				8
SETC	0	C = 1			1				
CLRC	0	C = 0			0				
CLRVT	0	VT = 0					0		
RST	0	PC = 2080H	0	0	0	0	0	0	9
DI	0	Disable All Interrupts (I = 0)							
EI	0	Enable All Interupts (I = 1)							
DPTS	0	Disable PTS Interrupts (PSE = 0)							
EPTS	0	Enable PTS Interrupts (PSE = 1)							
NOP	0	PC = PC + 1							
SKIP	0	PC = PC + 2							
IPLPD	1	Idle Mode IF Key = 1; Powerdown Mode IF Key = 2 Chip RESET Otherwise							

NOTES:
1. If the mnemonic ends in "B" a byte operation is performed, otherwise a word operation is performed. Operands D, B and A must conform to the alignment rules for the required operand type. D and B are locations in the Lower Register File; A can be located anywhere in memory.
2. The symbols indicate the effects on the flags:
   - ✓ Cleared or set as appropriate
   - 0 Cleared
   - 1 Set
   - ↑ Set if appropriate; never cleared
   - ↓ Cleared if appropriate; never set
3. D, D + 2 are consecutive WORDs in memory; D is DOUBLE-WORD aligned.
4. D, D + 1 are consecutive BYTEs in memory; D is WORD aligned.
5. Changes a BYTE to WORD.
6. Offset is a 2's complement number.
7. Specific Bit must be in or windowed into the Lower Register File.
8. The "L" (LONG) suffix indicates DOUBLE-WORD operations.
9. Initiates a RESET by pulling RESET low. Software should re-initialize all the neccessary registers with code starting at 2080H.
10. The assembler does not accept this mnemonic (use the macro file for definition).
11. I = Interrupt Enable (PSW1).
12. These instructions will only function in 24-bit mode.
13. These instructions push/pop two additional bytes on/off stack in 24-bit mode.

9.0 INSTRUCTION LENGTH/OPCODES

Mnemonic	Direct	Immed	Indirect		Indexed	
			Normal(1)	A-Inc(1)	Short(1)	Long(1)
ADD (3-op)	4/44	5/45	4/46	4/46	5/47	6/47
SUB (3-op)	4/48	5/49	4/4A	4/4A	5/4B	6/4B
ADD (2-op)	3/64	4/65	3/66	3/66	4/67	5/67
SUB (2-op)	3/68	4/69	3/6A	3/6A	4/6B	5/6B
ADDC	3/A4	4/A5	3/A6	3/A6	4/A7	5/A7
SUBC	3/A8	4/A9	3/AA	3/AA	4/AB	5/AB
CMP	3/88	4/89	3/8A	3/8A	4/8B	5/8B
ADDB (3-op)	4/54	4/55	4/56	4/56	5/57	6/57
SUBB (3-op)	4/58	4/59	4/5A	4/5A	5/5B	6/5B
ADDB (2-op)	3/74	3/75	3/76	3/76	4/77	5/77
SUBB (2-op)	3/78	3/79	3/7A	3/7A	4/7B	5/7B
ADDCB	3/B4	3/B5	3/B6	3/B6	4/B7	5/B7
SUBCB	3/B8	3/B9	3/BA	3/BA	4/BB	5/BB
CMPB	3/98	3/99	3/9A	3/9A	4/9B	5/9B
MUL (3-op)	5/(2)	6/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULU (3-op)	4/4C	5/4D	4/4E	4/4E	5/4F	6/4F
MUL (2-op)	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULU (2-op)	3/6C	4/6D	3/6E	3/6E	4/6F	5/6F
DIV	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVU	3/8C	4/8D	3/8E	3/8E	4/8F	5/8F
MULB (3-op)	5/(2)	5/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULUB (3-op)	4/5C	4/5D	4/5E	4/5E	5/5F	6/5F
MULB (2-op)	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULUB (2-op)	3/7C	3/7D	3/7E	3/7E	4/7F	5/7F
DIVB	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVUB	3/9C	3/9D	3/9E	3/9E	4/9F	5/9F
AND (3-op)	4/40	5/41	4/42	4/42	5/43	6/43
AND (2-op)	3/60	4/61	3/62	3/62	4/63	5/63
OR (2-op)	3/80	4/81	3/82	3/82	4/83	5/83
XOR	3/84	4/85	3/86	3/86	4/87	5/87
ANDB (3-op)	4/50	4/51	4/52	4/52	5/53	5/53
ANDB (2-op)	3/70	3/71	3/72	3/72	4/73	4/73
ORB (2-op)	3/90	3/91	3/92	3/92	4/93	5/93
XORB	3/94	3/95	3/96	3/96	4/97	5/97
PUSH	2/C8	3/C9	2/CA	2/CA	3/CB	4/CB
POP	2/CC	—	2/CE	2/CE	3/CF	4/CF
LD	3/A0	4/A1	3/A2	3/A2	4/A3	5/A3
LDB	3/B0	3/B1	3/B2	3/B2	4/B3	5/B3
ELD			3/E8	3/E8		6/E9
ELDB			3/EA	3/EA		6/EB
ST	3/C0	—	3/C2	3/C2	4/C3	5/C3
STB	3/C4	—	3/C6	3/C6	4/C7	5/C7
EST			3/1C	3/1C		6/1D
ESTB			3/1E	3/1E		6/1F

9.0 INSTRUCTION LENGTH/OPCODES (Continued)

Mnemonic	Direct	Immed	Indirect		Indexed	
			Normal(1)	A-Inc(1)	Short(1)	Long(1)
XCH	3/04	—	—	—	4/0B	5/0B
XCHB	3/14	—	—	—	4/1B	5/1B
LDBSE	3/BC	3/BD	3/BE	3/BE	4/BF	5/BF
LBSZE	3/AC	3/AD	3/AE	3/AE	4/AF	5/AF

Mnemonic	Length/Opcode
PUSHF	1/F2
POPF	1/F3
PUSHA	1/F4
POPA	1/F5
TRAP	1/F7
LCALL	3/EF
SCALL	2/28–2F(3)
ECALL	4/F1
RET	1/F0
LJMP	3/E7
SJMP	2/20–27(3)
EJMP	4/E6
BR[ ]	2/E3
TIJMP	4/E2
JNST	1/D0
JST	1/D8
JNH	1/D1
JH	1/D9
JGT	1/D2
JLE	1/DA
JNC	1/B3
JC	1/D8
JNVT	1/D4
JVT	1/DC
JNV	1/D5
JV	1/DD
JGE	1/D6
JLT	1/DE
JNE	1/D7
JE	1/DF
JBC	3/30–37
JBS	3/38–3F

Mnemonic	Length/Opcode
DJNZ	3/E0
DJNZW	3/E1
NORML	3/0F
SHRL	3/0C
SHLL	3/0D
SHRAL	3/0E
SHR	3/08
SHRB	3/18
SHL	3/09
SHLB	3/19
SHRA	3/0A
SHRAB	3/1A
CLRC	1/F8
SETC	1/F9
DI	1/FA
EI	1/FB
DPTS	1/EC
EPTS	1/ED
CLRVT	1/FC
NOP	1/FD
RST	1/FF
SKIP	2/00
IDLPD	1/F6
BMOV	3/C1
BMOVi	3/CD
EBMOVi	3/E4

NOTES:
1. Indirect and indirect + share the same opcodes, as do short and long indexed opcodes. If the second byte is even, use indirect or short indexed. If odd, use indirect or long indexed.
2. The opcodes for signed multiply and divide are the unsigned opcode with an "FE" prefix.
3. The 3 least significant bits of the opcode are concatenated with the 8 bits to form an 11-bit, 2's complement offset.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES)

Instruction	Direct	Immediate	Indirect		Indexed		Extended
			Normal	A-Inc	Short	Long	
ADD (3op)	5	6	7/10	8/11	7/10	8/11	
SUB (3op)	5	6	7/10	8/11	7/10	8/11	
ADD (2op)	4	5	6/8	7/9	6/8	7/9	
SUB (2op)	4	5	6/8	7/9	6/8	7/9	
ADDC	4	5	6/8	7/9	6/8	7/9	
SUBC	4	5	6/8	7/9	6/8	7/9	
CMP	4	5	6/8	7/9	6/8	7/9	
ADDB (3op)	5	5	7/10	8/11	7/10	8/11	
SUBB (3op)	5	5	7/10	8/11	7/10	8/11	
ADDB (2op)	4	4	6/8	7/9	6/8	7/9	
SUBB (2op)	4	4	6/8	7/9	6/8	7/9	
ADDCB	4	4	6/8	7/9	6/8	7/9	
SUBCB	4	4	6/8	7/9	6/8	7/9	
CMPB	4	4	6/8	7/9	6/8	7/9	
CMPL	7						
MUL (3op)	16	17	18/21	19/22	19/22	20/23	
MULU (3op)	14	15	16/19	17/20	17/20	18/21	
MUL (2op)	16	17	18/21	19/22	19/22	20/23	
MULU (2op)	14	15	16/19	17/20	17/20	18/21	
DIV	26	27	28/31	29/32	29/32	30/33	
DIVU	24	25	26/29	27/30	27/30	28/31	
MULB (3op)	12	12	14/17	15/18	15/18	16/19	
MULUB (3op)	10	10	12/15	12/16	12/16	14/17	
MULB (2op)	12	12	14/17	15/18	15/18	16/19	
MULUB (2op)	10	10	12/15	12/16	12/16	14/17	
DIVB	18	18	20/23	21/24	21/24	22/25	
DIVUB	16	16	18/21	19/22	19/22	20/23	
AND (3op)	5	6	7/10	8/11	7/10	8/11	
AND (2op)	4	5	6/8	7/9	6/8	7/9	
OR	4	5	6/8	7/9	6/8	7/9	
XOR	4	5	6/8	7/9	6/8	7/9	
ANDB (3op)	5	5	7/10	8/11	7/10	8/11	
ANDB (2op)	4	4	6/8	7/9	6/8	7/9	
ORB	4	4	6/8	7/9	6/8	7/9	
XORB	4	4	6/8	7/9	6/8	7/9	
LD	4	5	5/8	6/8	6/9	7/10	

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed		Extended
			Normal	A-Inc	Short	Long	
ST	4		5/8	6/9	6/9	7/10	
LDB	4	4	5/8	6/8	6/9	7/10	
STB	4		5/8	6/9	6/9	7/10	
ELD			6/9	8/11			8/11
EST			6/9	8/11			8/11
ELDB			6/9	8/11			8/11
ESTB			6/9	8/11			8/11
XCH	5				8/13	9/14	
STB	4				8/13	9/14	
XCHB	5				8/13	9/14	
BMOV	6 + 8 per Word		6 + 11/14 per Word				
BMOVI	7 + 8 per Word +14 for Each Interrupt		7 + 11/14 per Word +14 for Each Interrupt				
EBMOVI			8 + 14/20 per Word +16 for Each Interrupt				
LDBSE, LDBZE	4	4	5/7	6/8	6/8	7/9	
PUSH (int)	6	7	9/12	10/13	10/13	11/14	
POP (int)	8		10/12	11/13	11/13	12/14	
PUSHF (int)	6						
POPF (int)	7						
PUSHA (int)	12						
POPA (int)	12						
PUSH (ext)	8	9	11/14	12/15	12/15	13/16	
POP (ext)	11		13/15	14/16	14/16	15/17	
PUSHF (ext)	8						
POPF (ext)	10						
PUSHA (ext)	18						
POPA (ext)	18						
EJMP (24-Bit Mode)	8						
LJMP	7						
SJMP	7						
EBR[Indirect](24-Bit Mode)	9						
BR[Indirect]	7						
TIJMP (Internal Table)	15						
TIJMP (External Table)	18						
TRAP (24-Bit Mode, Int)	19						
TRAP (16-Bit Mode, Int)	16						

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed		Extended
			Normal	A-Inc	Short	Long	
ECALL (24-Bit Mode, Int)	16						
LCALL (16-Bit Mode, Int)	11						
LCALL (24-Bit Mode, Int)	15						
SCALL (16-Bit Mode, Int	11						
SCALL (24-Bit Mode, Int)	15						
RET (24-Bit Mode, Int)	16						
RET (16-Bit Mode, Int)	11						
TRAP (24-Bit Mode, Ext)	25						
TRAP (16-Bit Mode, Ext)	18						
ECALL (24-Bit Mode, Ext)	22						
LCALL (16-Bit Mode, Ext)	13						
LCALL (24-Bit Mode, Ext)	18						
SCALL (16-Bit Mode, Ext)	13						
SCALL (24-Bit Mode, Ext)	18						
RET (24-Bit Mode, Ext)	22						
RET (16-Bit Mode, Ext)	14						
JNST, JST	4/8 Jump Not Taken/Jump Taken						
JNH, JH	4/8 Jump Not Taken/Jump Taken						
JGT, JLE	4/8 Jump Not Taken/Jump Taken						
JNC, JC	4/8 Jump Not Taken/Jump Taken						
JNVT, JVT	4/8 Jump Not Taken/Jump Taken						
JNV, JV	4/8 Jump Not Taken/Jump Taken						
JGE, JLT	4/8 Jump Not Taken/Jump Taken						
JNE, JE	4/8 Jump Not Taken/Jump Taken						
JBS, JBC	5/9 Jump Not Taken/Jump Taken						
DJNZ	5/9 Jump Not Taken/Jump Taken						
DJNZW	6/10 Jump Not Taken/Jump Taken						
CLR, NOT, NEG	3						
DEC, INC	3						
EXT	4						
CLRB, NOTB	3						
DECB, INCB	3						
NEGB	3						
EXTB	4						
NORML	8 + 1 per Shift (9 for 0 Shift)						

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed		Extended
			Normal	A-Inc	Short	Long	
SHRL	7 + 1 per Shift (8 for 0 Shift)						
SHLL	7 + 1 per Shift (8 for 0 Shift)						
SHRAL	7 + 1 per Shift (8 for 0 Shift)						
SHR	6 + 1 per Shift (7 for 0 Shift)						
SHL	6 + 1 per Shift (7 for 0 Shift)						
SHRA	6 + 1 per Shift (7 for 0 Shift)						
SHRB	6 + 1 per Shift (7 for 0 Shift)						
SHLB	6 + 1 per Shift (7 for 0 Shift)						
SHRAB	6 + 1 per Shift (7 for 0 Shift)						
CLRC	2						
SETC	2						
DI	2						
EI	2						
DPTS	2						
EPTS	2						
CLRVT	2						
NOP	2						
RST	20 (Includes Fetch of CCB0/CCB1)						
SKIP	3						
IDLPD	8/25 (Proper Key/Improper Key)						
PTS							
Single Transfer	18	(+3 for Ext Reference, + 1 If XFER Count = 0)					
Burst Transfer	13	(+7 for Each Transfer, 1 Minimum +3 for Each Memory Controller Reference)					
PWM Modes	15						
A/D Scan Mode	21/25						

NOTES:
The timing figures are minimum execution times expressed as state times (one period of CLKOUT = two oscillator periods) and are based on the following assumptions:
1. The opcode, along with any required operands, have been pre-fetched and reside in the instruction queue.
2. The bus controller operates with the 16-bit bus selected and without wait states for external memory references and pre-fetches. For instructions with indirect or indexed addressing, execution times separated by a slash are for instructions requiring a fetch from internal/external memory.
3. Times for jumps, calls and returns include the 4 state times required to flush the pre-fetch queue and to fetch the opcode at the destination address. This is reflected in the jump taken/not-taken times shown in the table.

11.0 INTERRUPT TABLE

Name	Source	Vector	Priority
INT15	NMI	203EH	32 (Highest)
PTS14	EXTINT Pin	205CH	31
PTS13	Reserved	205AH	30
PTS12	Receive SIO	2058H	29
PTS11	Transmit SIO	2056H	28
PTS10	SSIO Channel 1 Transfer	2054H	27
PTS09	SSIO Channel 0 Transfer	2052H	26
PTS08	Command Buffer Full (SLP)	2050H	25
PTS07	Input Buffer Full (SLP)	204EH	24
PTS06	Output Buffer Empty (SLP)	204CH	23
PTS05	A/D Conversion Complete	204AH	22
PTS04	EPA0	2048H	21
PTS03	EPA1	2046H	20
PTS02	EPA2	2044H	19
PTS01	EPA3	2042H	18
PTS00	EPA4–9, Overrun (EPA0–9), Compare0–1, Timer Overflow	2040H	17
INT14	EXTINT Pin	203CH	16
INT13	Reserved	203AH	15
INT12	Receive SIO	2038H	14
INT11	Transmit SIO	2036H	13
INT10	SSIO Channel 1 Transfer	2034H	12
INT09	SSIO Channel 0 Transfer	2032H	11
INT08	Command Buffer Full (SLP)	2030H	10
N/A	UNIMPLEMENTED OPCODE	2012H	09
N/A	TRAP	2010H	08
INT07	Input Buffer Full (SLP)	200EH	07
INT06	Output Buffer Empty (SLP)	200CH	06
INT05	A/D Conversion Complete	200AH	05
INT04	EPA0	2008H	04
INT03	EPA1	2006H	03
INT02	EPA2	2004H	02
INT01	EPA3	2002H	01
INT00	EPA4–9, Overrun (EPA0–9), Compare0–1, Timer Overflow	2000H	00 (Lowest)

12.0 FORMULAS

State Time = 2 Oscillator Periods

TIJMP Calculation—

Destination = ([INDEX] AND INDEX_MASK) × 2 + [TBASE]

EPA Prescaler—

P2	P1	P0	
0	0	0	÷ 1
0	0	1	÷ 2
0	1	0	÷ 4
0	1	1	÷ 8
1	0	0	÷ 16
1	0	1	÷ 32
1	1	0	÷ 64
1	1	1	Reserved

SIO Baud Rate—

Modes 1, 2 and 3

$$SP\_BAUD = \frac{XTAL1\ Frequency}{Baud\ Rate \times 16} - 1 \qquad (B \geq 0, SP\_BAUD.15 = 1)$$

$$SP\_BAUD = \frac{T1CLK\ Frequency}{Baud\ Rate \times 8} - 1 \qquad (B > 0, SP\_BAUD.15 = 0)$$

Mode 0

$$SP\_BAUD = \frac{XTAL1\ Frequency}{Baud\ Rate \times 2} - 1 \qquad (B > 0, SP\_BAUD.15 = 1)$$

$$SP\_BAUD = \frac{T1CLK\ Frequency}{Baud\ Rate} - 1 \qquad (B > 0, SP\_BAUD.15 = 0)$$

SSIO Baud Rate—

$$SSIO.0 - SSIO.6 = \frac{XTAL1\ Frequency}{Baud\ Rate \times 8} - 1$$

A/D—

Sample States = 4 × SAM + 1
(SAM = AD_TIME.5 − AD_TIME.7)

Conversion States = B × (CONV + 1) + 1.5
(CONV = AD_TIME.0 − AD_TIME.4)
(B = 8 for 8-Bit Conversion)
(B = 10 for 10-Bit Conversion)

Total Conversion Time = State Time × [(4 × SAM) + (B × (CONV + 1)) + 2.5]

Programming Pulse Width—

$$PPR = \frac{((PPW) \times (FOSC)) - 144}{144} + 32768$$

13.0 RESET STATUS

SFR	Reset Value
AD_RESULT	7F80H
AD_COMMAND	0C0H
AD_TEST	0C0H
AD_TIME	0FFH
SSIO0_BUF, SSIO1_BUF	00H
SSIO0_CON, SSIO1_CON	00H
SSIO_BAUD (Baud Rate Control (Read))	0XXXXXXXB
SSIO_BAUD (Baud Rate Down Count (Write))	00H
SBUF_RX, SBUF_TX	00H
SP_STAT	0BH
SP_CON	EOH
SP_BAUD	0000H
COMP0_CON, COMP1_CON	00H
COMP0_TIME, COMP1_TIME	0000H
EPA1_CON, EPA3_CON	0000H
EPAx_CON (x = 0, 2, 4–9)	00H
EPAx_TIME (x = 0–9)	0000H
TIMER1, TIMER2	0000H
T1CONTROL, T2CONTROL	00H
EPA_MASK, EPA_MASK1	00H
EPA_PEND, EPA_PEND1	00H
EPAIPV	00H
P0_PIN, P1_PIN, P3_PIN, P4_PIN, P6_PIN	XXH
P1_MODE, P6_MODE	00H
P1_DIR, P5_DIR, P6_DIR	0FFH
P1_REG, P3_REG, P4_REG, P5_REG, P6_REG	0FFH
P2_PIN, P5_PIN	1XXXXXXXB
P2_MODE, P5_MODE	80H
P2_DIR, P2_REG	7FH
INT_MASK, INT_PEND	00H
INT_MASK1, INT_PEND1	00H
PTSSRV, PTSSEL	0000H
WSR	00H

Pin States, during Reset, Idle and Powerdown

Pin Name	Reset	Idle	PD
$\overline{\text{RESET}}$	wk1	wk1	wk1
ALE (P5.0)	wk1	(A)	(A)
INST (P5.1)	wk0	(A)	(A)
$\overline{\text{RD}}$ (P5.3), $\overline{\text{WR}}$ (P5.2), SPLINT (P5.4)	wk1	(I)	(I)
$\overline{\text{BHE}}$ (P5.5)	wk1	(B)	(B)
READY (P5.6), BUSW (P5.7)	wk1	(C)	(C)
$\overline{\text{EA}}$, NMI	HZ	HZ	HZ
P3, P4/AD (EA = 0)	wk1	HZ	HZ
P3, P4/AD (EA = 1)	wk1	ODIO	ODIO
ACH/PO	HZ	HZ	HZ
P1	wk1	(D)	(D)
CLKOUT (P2.7)	clk, LZ	(E)	(G)
P2.0–P2.6	wk1	(E)	(E)
P6.0–P6.7	wk1	(F)	(F)
V_{PP}	HZ	1, LZ	1, LZ
XTAL1	HZ	HZ	HZ
XTAL2	osc, LZ	osc, LZ	(H)

NOTES:
(A) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 1, then LZ 0. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 0, then HZ.
(B) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 1, then LZ 1. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 0, then HZ.
(C) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1, then HZ.
(D) If P1_MODE.x = 0, port is as programmed. If P1_MODE.x = 1, pin is as specified by P1_DIR and associated peripheral.
(E) If P2_MODE.x = 0, port is as programmed. If P2_MODE.x = 1, pin is as specified by P2_DIR and associated peripheral.
(F) If P6_MODE.x = 0, port is as programmed. If P6_MODE.x = 1, pin is as specified by P6_DIR and associated peripheral.
(G) If P2_MODE.7 = 0, port is as programmed. If P2_MODE.7 = 1, then LZ 0.
(H) If XTAL1 = 1, then LZ 0. IF XTAL1 = 0, then LZ 1.
(I) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1, then pin is as specified by P5_DIR and associated peripheral.
HZ = High impedance
LZ = Low Impedance
wk1 = Weakly pulled high
ODIO = Open drain input/output
osc = Oscillator
wk0 = Weakly pulled low

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8XC196MC Quick Reference

Order Number: 272114-002

8XC196MC Quick Reference

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1.0 MEMORY MAP

8XC196MC Memory Map

0FFFFH 06000H	External Memory		
05FFFH 02080H	Internal ROM/EPROM or External Memory		
0207FH 02000H	Reserved Memory (Internal ROM/EPROM or External Memory)		
01FFFH 01F00H	Internal Special Function Registers (SFRs)		
01EFFH 00200H	External Memory		
001FFH 00100H	Register RAM	Upper Register File (Address with indirect or indexed modes or through windows.)	Register File
000FFH 00018H	Register RAM	Lower Register File (Address with direct indirect or indexed modes.)	
00017H 00000H	CPU SFRs		

8XC196MC Reserved Memory

0207FH 02074H	Reserved
02073H 02072H	Programming Voltages
02071H 02070H	Signature Word
0206FH 0205EH	Reserved
0205DH 02040H	Peripheral Transaction Server (PTS) Vectors
0203FH 02030H	Interrupt Vectors (Upper)
0202FH 02020H	Security Key
0201FH 0201EH 0201DH 0201CH	20H Reserved 20H Reserved
0201BH 0201AH 02019H 02018H	20H CCB1 (Chip Configuraton Byte 1) 20H CCB (Chip Configuration Byte 0)
02017H 02014H	Reserved
02013H 02000H	Interrupt Vectors (Lower)

NOTE:
Reserved locations must be filled with 0FFH unless noted.

2.0 SFR MAP

CORE SFR MAP

0019H:	SP (HI)
0018H:	SP (LO)
0017H:	reserved
0016H:	reserved
0015H:	reserved
0014H:	WSR
0013H:	INT_MASK1
0012H:	INT_PEND1
0011H:	reserved
0010H:	reserved
000FH:	reserved
000EH:	reserved
000DH:	reserved
000CH:	reserved
000BH:	reserved
000AH:	WATCHDOG
0009H:	INT_PEND
0008H:	INT_MASK
0007H:	PTSSRV (HI)
0006H:	PTSSRV (LO)
0005H:	PTSSEL (HI)
0004H:	PTSSEL (LO)
0003H:	reserved
0002H:	reserved
0001H:	ZERO_REG (HI)
0000H:	ZERO_REG (LO)

PERIPHERAL SFR MAP

1FFFH:	P4_PIN
1FFEH:	P3_PIN
1FFDH:	P4_REG
1FFCH:	P3_REG
1FF8H - 1FFBH:	reserved
1FF7H:	P5_PIN
1FF6H:	USFR
1FF5H:	P5_REG
1FF4H:	reserved
1FF3H:	P5_DIR
1FF2H:	reserved
1FF1H:	P5_MODE
1FD7H - 1FF0H:	reserved
1FD6H:	P2_PIN
1FD5H:	reserved
1FD4H:	P2_REG
1FD3H:	reserved
1FD2H:	P2_DIR
1FD1H:	reserved
1FD0H:	P2_MODE
1FCFH:	reserved
1FCEH:	WG_PROTECT
1FCCH:	WG_CON
1FCAH:	WG_COUNT
1FC8H:	WG_RELOAD
1FC6H:	WG_COMP3
1FC4H:	WG_COMP2
1FC2H:	WG_COMP1
1FC0H:	WG_OUT
1FBFH:	reserved
1FBEH:	PI_PEND
1FBDH:	reserved
1FBCH:	PI_MASK
1FB7H - 1FBBH:	reserved
1FB6H:	PWM_PER_CNT
1FB5H:	reserved
1FB4H:	PWM_PERIOD
1FB3H:	reserved
1FB2H:	PWM1
1FB1H:	reserved
1FB0H:	PWM0
1FAFH:	AD_TIME
1FADH:	reserved
1FAEH:	AD_TEST
1FACH:	AD_COMMAND
1FAAH:	AD_RESULT
1FA9H:	P1_PIN
1FA8H:	P0_PIN
1F80H - 1FA7H:	reserved
1F7EH:	TIMER2*
1F7DH:	reserved
1F7CH:	T2CONTROL
1F7AH:	TIMER1 *
1F79H:	reserved
1F78H:	T1CONTROL
1F74H - 1F77H:	reserved
1F72H:	T1RELOAD
1F68H - 1F71H:	reserved
1F66H:	COMP3_TIME *
1F65H:	reserved
1F64H:	COMP3_CON
1F62H:	COMP2_TIME *
1F61H:	reserved
1F60H:	COMP2_CON
1F5EH:	COMP1_TIME *
1F5DH:	reserved
1F5CH:	COMP1_CON
1F5AH:	COMP0_TIME *
1F59H:	reserved
1F58H:	COMP0_CON
1F50H - 1F57H:	reserved
1F4EH:	CAPCOMP3_TIME *
1F4DH:	reserved
1F4CH:	CAPCOMP3_CON
1F4AH:	CAPCOMP2_TIME *
1F49H:	reserved
1F48H:	CAPCOMP2_CON
1F46H:	CAPCOMP1_TIME *
1F45H:	reserved
1F44H:	CAPCOMP1_CON
1F42H:	CAPCOMP0_TIME *
1F41H:	reserved
1F40H:	CAPCOMP0_CON

NOTE:
*These registers can only be addressed as word registers, not as separate byte registers.

3.0 SFR BIT SUMMARY

CHIP CONFIGURATION BYTES

CCB (2018H)

msb							lsb
LOC1	LOC0	IRC1	IRC0	ALE	WR	BW0	PD

CCB1 (201AH)

msb							lsb
1*	1*	0*	1*	WD	BW1	IRC2	0*

*: These bits are reserved and must be written as indicated.

WD: Watch Dog Timer Disable.

0 = Starts RUNNING immediately and cannot be stopped.

1 = Does not run until enabled in software.

BW1–BW0: Bus Width. These two bits separately, OR along with BUSWIDTH pin determine the external bus width (8-bit or 16-bit wide).

BW1	BW0	BUSWIDTH (pin)	Bus Width
0	0	x	Illegal
0	1	X	16
1	0	x	8
1	1	0	8
1	1	1	16

LOC0: Internal OTPROM Write Protect.
LOC0 = 1 No Write protection.
LOC0 = 0 Address locations 2000H to 5FFFH are write protected.

LOC1: Internal OTPROM Read Protect.
LOC1 = 1 No read protection.
LOC1 = 0 Address locations 2080H to 5FFFH are read protected, also locations 2020H to 202FH are read/write protected.

IRC2, IRC1, IRC0: Internal Ready Control. They limit the number of the wait states to be asserted in the external bus operation.

IRC2	IRC1	IRC0	Number of Wait States
0	0	0	0
0	X	1	Illegal
0	1	X	Illegal
1	0	0	1
1	0	1	2
1	1	0	3
1	1	1	Infinite

ALE: ALE/$\overline{\text{ADV}}$
ALE = 0 The ALE pin becomes $\overline{\text{ADV}}$
ALE = 1 The ALE pin remains ALE

WR: $\overline{\text{Write Strobe Mode}}$/Standard Mode
WR = 0 The BHE pin becomes $\overline{\text{WRH}}$ and $\overline{\text{WR}}$ becomes $\overline{\text{WRL}}$
WR = 1 The $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ are unchanged

PD: Power Down Enable
PD = 0 The power down instruction does not have any effect
PD = 1 The power down instruction is enabled

WINDOW SELECT REGISTER

WSR (0014H)

msb							lsb
W7	W6	W5	W4	W3	W2	W1	W0

W7–W0: Window select bits

0000 0000 No windowing

01XX XXXX 32 Byte windowing

001X XXXX 64 Byte windowing

0001 XXXX 128 Byte windowing

The window select bits are combined with the register address to access the RAM area in locations 0000 through 1FFH or the upper SFR area in locations 1C00H through 1FFFH.

PROGRAM STATUS WORD

PSW

msb								lsb
Z	N	V	VT	C	PSE	I	ST	INT MASK

Z: Zero Flag
N: Negative Flag
V: Overflow Flag
VT: Overflow Trap Flag
C: Carry Flag
PSE: PTS Enable bit
IE: Interrupt Enable bit
ST: Sticky Bit Flag

PORT 2 AND PORT 5 CONTROL REGISTERS

Pn_MODE (n = 2 @ 1FD0H, n = 5 @ 1FF1H)

7	6	5	4	3	2	1	0

Pn_REG (n = 2 @ 1FD4H, n = 5 @ 1FF5H)

7	6	5	4	3	2	1	0

Pn_DIR (n = 2 @ 1FD2H, n = 5 @ 1FF3H)

7	6	5	4	3	2	1	0

Pn_PIN (n = 2 @ 1FD6H, n = 5 @ 1FF7H)

7	6	5	4	3	2	1	0

Pn_PIN contains the pin data delayed by ½ state time.

Each pin of Port 2 can be programmed to function in one of the following modes:

Mode	Dir	Reg	Pull Up	Pull Down	Function
0	0	0	OFF	ON	Output 0
0	0	1	ON	OFF	Output 1
0	1	0	OFF	ON	Open Drain 0
0	1	1	OFF	OFF	Open Drain 1 (Input)
1	X	X	System Pin	System Pin	System Pin

Each pin of Port 5 can be programmed to function in one of the following modes.

Mode	Dir	Reg	Pull Up	Pull Down	Function
X	0	0	OFF	ON	Output 0
X	0	1	ON	OFF	Output 1
X	1	0	OFF	ON	Open Drain 0
X	1	1	OFF	OFF	Open Drain 1 (Input)

AD COMMAND REGISTER

AD_COMMAND (1FACH)

msb							lsb
7	6	5	4	3	2	1	0

0–3: Channel Select
4: GO, indicates when to begin conversion
GO = 1 means start now
GO = 0 means EPA controls when to start conversion.
5, 6: CONVERSION MODE:
00 = 10-bit
01 = 8-bit
10 = Threshold detect high
11 = Threshold detect low
7: Reserved, write 0.

AD TIME REGISTER

AD_TIME (1FAFH)

msb							lsb
7	6	5	4	3	2	1	0

0–4: Conversion Time = n + 1 state times (n = 2 to 31).
5–7: Sample Time = 4n + 1 state times (n = 1 to 7).

AD RESULT REGISTER (READ)

AD_RESULT (1FAAH)

msb						lsb
15–6					5	4	3	2	1	0

0–3: Channel Number
4: Busy
0 = AD is idle
1 = Conversion is in progress
5: Reserved
6–15: 10-bit AD result

AD RESULT REGISTER (WRITE)

AD_RESULT (1FAAH)

msb						lsb
15–8	7–5	4	3	2	1	0

0–3: Channel Number

4: Busy
0 = AD is idle
1 = conversion is in progress

5–7: Reserved, write 0

8–15: SAR value. Writing to the AD_RESULT register selects the threshold detection value. Presetting the ASR is required before selecting one of the threshold detect modes.

TIMER 1 CONTROL REGISTER

T1CONTROL (1F78H)

msb							lsb
CE	UD	M2	M1	M0	P2	P1	P0

CE: 1 = timer/counter enabled
0 = timer/counter disabled

UD: 1 = count up
0 = count down

M2 M1 M0: EPA Clock source and direction mode select.

M2	M1	M0	Clock Source	Clock Direction
0	0	0	Internal	UD Bit
0	0	1	External	UD Bit
0	1	0	Internal	External Pin
0	1	1	External	External Pin
1	0	0	Reserved	
1	1	0	Reserved	
1	1	1	Quadrature Clocking(1)	

NOTE:
1. The counter input clock and the count direction is taken from the quadrature clocking circuit.

P2 P1 P0: EPA Clock control bits.

P2	P1	P0	Input Divide By	Resolution (at 16 MHz)
0	0	0	1	250 ns
0	0	1	2	500 ns
0	1	0	4	1 μs
0	1	1	8	2 μs
1	0	0	16	4 μs
1	0	1	32	8 μs
1	1	0	64	16 μs
1	1	1	1	enable T1RELOAD

AD_TEST (1FAEH)

msb							lsb
7	6	5	4	3	2	1	0

0–1: Reserved

2–4: Adjust offset

b4	b3	b2
0	0	0—no change
0	0	1—add 2.5 mV
1	0	0—sub 2.5 mV
1	0	1—sub 5.0 mV
X	1	X—reserved

5–7: Reserved

TIMER 2 CONTROL REGISTER

T2 CONTROL (1F7CH)

msb							lsb
CE	UD	M2	M1	M0	P2	P1	P0

CE: 1 = timer/counter enabled
0 = timer/counter disabled

UD: 1 = Count up
0 = Count down

M2 M1 M0: EPA Clock source and direction mode select.

M2	M1	M0	Clock Source	Clock Direction
0	0	0	Internal	UD Bit
0	0	1	Reserved	
0	1	0	Reserved	
0	1	1	Reserved	
1	0	0	T1 Over/Underflow	UD Bit
1	1	0	T1 Over/Underflow	Timer 1
1	1	1	Reserved	

P2 P1 P0: Timer prescalar control

P2	P1	P0	Input Divide By	Resolution (at 16 MHz)
0	0	0	1	250 ns
0	0	1	2	500 ns
0	1	0	4	1 μs
0	1	1	8	2 μs
1	0	0	16	4 μs
1	0	1	32	8 μs
1	1	0	64	16 μs
1	1	1	Reserved	

CAPTURE/COMPARE CONTROL REGISTERS

CAPCOMPn_CON

msb							lsb
TB	CE	M1	M0	RE	PFE	ROT	ON/RT

n	Address
0	1F40H
1	1F44H
2	1F48H
3	1F4CH

TB: 1 = selects TIMER2 as time base
0 = selects TIMER1 as time base

CE: 1 = enables compare mode
0 = disables capture mode

M1, M0: Mode Selects
On Capture Mode (CE = 0)
00 = no operation
01 = capture − edge
10 = capture + edge
11 = capture ± edge
On Compare Mode (CE = 1)
00 = no compare
01 = clear output pin
10 = set output pin
11 = toggle output pin

PFE: 1 = peripheral function enable
0 = no action

RE: 1 = output event is automatically enabled after execution
0 = output event is disabled after execution

ROT: Reset Opposite Timer
On Capture Mode (CE = 0)
1 = reset opposite timer
0 = no action
On Compare Mode (CE = 1)
1 = reset opposite timer
0 = reset selected timer

ON/RT: Overwrite New/Reset Timer
On Capture Mode (CE = 0)
1 = old data of CCn_BUFF lost on data overrun
0 = new data lost on data overrun
On Compare Mode (CE = 1)
1 = reset timer (selected by TB and ROT)
0 = no action

CAPTURE/COMPARE CONTROL REGISTERS (Continued)

TB	CE	M1	M0	RE	PFE	ROT	ON/RT	Operating Mode
Capture:								
X	0	0	0	—	X	X	X	No Operation (No Interrupt)
X	0	1	0	—	X	X	X	Capture on Positive Transition
X	0	0	1	—	X	X	X	Capture on Negative Transition
X	0	1	1	—	X	X	X	Capture on Either Transition
X	0	X	1	—	X	1	X	Reset Opposite Timer
X	0	1	X	—	X	1	X	Reset Opposite Timer
X	0	X	1	—	1	X	X	Peripheral Function Enable
X	0	1	X	—	1	X	X	Peripheral Function Enable
X	0	X	1	—	X	X	X	Generate Interrupt
X	0	1	X	—	X	X	X	Generate Interrupt
Compare:								
X	1	0	1	X	X	X	X	Reset Output Pin
X	1	1	0	X	X	X	X	Set Output Pin
X	1	1	1	X	X	X	X	Toggle Output Pin
X	1	X	X	X	X	0	1	Reset Associated Time Base Timer
X	1	X	X	X	X	1	1	Reset Opposite Time Base Timer
X	1	X	X	X	1	X	X	Peripheral Function Enable
X	1	X	X	X	X	X	X	Generate Interrupt
X	1	0	0	X	0	X	0	Generate Interrupt Only (Soft Timer)

X: Bit selects additional options
—: Bit is not used in Capture Mode

COMPARE CONTROL REGISTER

COMPn_CON

msb							lsb
TB	CE	M1	M0	RE	PFE	ROT	ON/RT

n	ADDRESS
0	1F58H
1	1F5CH
2	1F60H
3	1F64H

TB: 1 = TIMER2 as time base
0 = TIMER1 as time base

CE: 1 = enables comparator
0 = disables comparator

M1, M0: 00 = no action on output pin
01 = clear output pin
10 = set output pin
11 = toggle output pin

PFE: 1 = peripheral function enable
0 = no action

RE: 1 = output event is automatically re-enabled after execution
0 = output event is disabled after execution

ROT: 1 = reset opposite timer (timer not selected by TB)
0 = reset selected timer (selected by TB)

ON/RT: 1 = reset timer (selected by ROT)
0 = no action

COMPARE CONTROL REGISTER (Continued)

TB	CE	M1	M0	RE	PFE	ROT	RT	Operating Mode
X	0	X	X	X	X	X	X	No Operation (No Interrupt)
X	1	0	1	X	X	X	X	Reset Output Pin
X	1	1	0	X	X	X	X	Set Output Pin
X	1	1	1	X	X	X	X	Toggle Output Pin
X	1	X	X	X	X	0	1	Reset Associated Time Base Timer
X	1	X	X	X	X	1	1	Reset Opposite Time Base Timer
X	1	X	X	X	1	X	X	Peripheral Function Enable
X	1	X	X	X	X	X	X	Generate Interrupt
X	1	0	0	X	0	X	0	Generate Interrupt Only (Soft Timer)

X: Bit selects additional options

COMPARE TIME REGISTER

Scheduled time for programmed event. This register must only be read and written as a word.

COMPn_TIME

msb															lsb
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

n	ADDRESS
0	1F42H
1	1F46H
2	1F4AH
3	1F4EH

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PERIPHERAL INTERRUPT MASK REGISTER

PI_MASK (1FBCH)

msb							lsb
—	—	—	WG	—	TF2	—	TF1

—: Reserved, write 0

WG: Waveform Generator interrupt mask

TF2: Timer/Counter 2 overflow interrupt mask

TF1: Timer/Counter 1 overflow interrupt mask

NOTE:
A logical 1 in the bit position allows the corresponding function to set its interrupt pending flag.

PERIPHERAL INTERRUPT PENDING REGISTER

PI_PEND (1FBEH)

msb							lsb
—	—	—	WG	—	TF2	—	TF1

—: Reserved, write 0

WG: Waveform Generator status flag

TF2: Timer/Counter 2 overflow status flag

TF1: Timer/Counter 1 overflow status flag

NOTE:
This register can be read but not written. When read, all bits in this register are reset. Therefore, the value of the register must be stored in a shadow register if more than one bit of this register is used.

WAVE GENERATOR CONTROL REGISTER

WG_CON (1FCCH)

msb															lsb
—	—	M1	M0	CS	EC	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

—: Reserved, write 0

M1, M0: Mode bits

Mode	Mode Bit		PWM Output	Counter Operation	Reload Triggering Signal	
	M1	M0			for WG_COMPn	for WG_OUT (Note 1)
0	0	0	Center	Up/Dn	(WG_Count)match	(WG_Count)match
1	0	1	Center	Up/Dn	(WG_Count)match or (WG_Count) = 1	(WG_Count)match or (WG_Count) = 1
2	1	0	Edge	Up	(WG_Count)match	(WG_Count)match or
3	1	1	Edge	Up	(WG_Count)match or EPA event	EPA event

CS: Counter Status
1 = up counting
0 = down counting

EC: Enable/Disable Counter (WG_Count)
1 = enable counting
0 = disable counting

D9–D0: 10 bit Down Counter value

NOTE:
1. The WG_OUT reload trigger signals are enabled when the SYNC bit in the Output Control Register (WG_OUT) is 1.

WG COMPARE REGISTER

WG_COMPn

msb															lsb
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

n	Address
1	1FC2H
2	1FC4H
3	1FC6H

WG_COMP controls the duty cycle of the waveform generator outputs.

WG RELOAD REGISTER

WG_RELOAD (1FC8H)

msb															lsb
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

WAVE GENERATOR OUTPUT CONTROL REGISTER

WG_OUT (1FC0H)

msb															lsb
OP1	OP0	SYNC	PE1	PE0	PH32	PH22	PH12	P1	P0	PH31	PH30	PH21	PH20	PH11	PH10

OP1: Output Polarity for positive-phase outputs
- 1 = P6.1, P6.3 and P6.5 are active-high
- 0 = P6.1, P6.3 and P6.5 are active-low

OP0: Output Polarity for negative-phase outputs
- 1 = P6.0, P6.2 and P6.4 are active-high
- 0 = P6.0, P6.2 and P6.4 are active-low

SYNC: Synchronize Loading of Output Buffer
- 1 = outputs are synchronized with Reload triggering signal for WG_COMPn
- 0 = outputs are not synchronized with WG_COMPn

PE1, PE0: Enable P6.7, P6.6 (respectively) as PWM output

P1, P0: P6.7, P6.6 (respectively) output value

PEn	Pn	Pin Output
0	0	0
0	1	1
1	X	PWM output

PH12 PH11 PH10 → control P6.0 and P6.1
PH22 PH21 PH20 → control P6.2 and P6.3
PH32 PH31 PH30 → control P6.4 and P6.5

PHn2	PHn1	PHn0	WGn OP1 = 1	WGn OP1 = 0	$\overline{WGn}$ OP0 = 1	$\overline{WGn}$ OP0 = 0	(n = 1, 2, or 3)
0	0	0	Low	High	Low	High	
0	0	1	Low	High	High	Low	
0	1	0	High	Low	Low	High	
0	1	1	High	Low	High	Low	
1	0	0	Low	High	Low	High	
1	0	1	Low	High	$\overline{PWM}$	PWM	
1	1	0	$\overline{PWM}$	PWM	Low	High	
1	1	1	$\overline{PWM}$	PWM	PWM	$\overline{PWM}$	

WG PROTECTION CONTROL REGISTER

WG_PROTECT (1FCEH)

msb							lsb
—	—	—	—	ES	IT	DP	EO

ES: Enable Sampling Circuitry
- 1 = protection/interrupt triggered by sampling
- 0 = protection/interrupt triggered by edge

IT: Interrupt Type control bit
- 1 = rising edge/high trigger
- 0 = falling edge/low trigger

DP: Disable/Enable Protection Circuit
- 1 = disable protection output
- 0 = enable protection output

EO: Enable/Disable Output. Must be set when port is used as output
- 1 = enable output
- 0 = disable output

PTS VECTORS PTSVEC, PTSVEC1

Each PTS vector points to internal RAM space and must be aligned to a quad word boundary.

msb													lsb
r	r	r	r	r	r	b	b	b	b	b	b	b	0 0 0

r . . . r Reserved (Write 0)

b . . . b Upper bits of the 10-bit pointer to the PTS Control Block located in Internal Ram.

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PTSCON—GENERAL TRANSFER MODES

msb							lsb
M2	M1	M0	B/W	SU	DU	SI	DI

M2, M1, M0: 000 = PTS Burst Transfer Mode
100 = PTS Single Transfer Mode

B/W: 1 = Transfer in bytes
0 = Transfer in words

SU: 1 = Update PTSSRC at end of each PTS cycle
0 = No update

DU: 1 = Update PTSDST at end of each PTS cycle
0 = No update

SI: 1 = Source address auto-increment
0 = No auto-increment

DI: 1 = Destination address auto-increment
0 = No auto-increment

PTSCON—A/D MODE

msb							lsb
M2	M1	M0	0	UPDT	0	1	1

M2, M1, M0: 110 = PTS A/D mode

UPDT: 1 = Update SRC/DST pointer
0 = No update

0: Write 0 to these bits

1: Write 1 to these bits

PTSCON—SERIAL PORT MODES

msb							lsb
M2	M1	M0	SA	0	0	SA	MAJ

M2, M1, M0: 011 = Transmit mode
001 = Receive mode

SA: 1 = Synchronous mode
0 = Asynchronous mode

MAJ: 1 = Enable Majority Sample mode
1 = Disable Majority Sample mode

0: Write 0 to these bits

PTSCON1—ASIO MODE

msb							lsb
0	RPAR	PEN	0	0	0	FE	TPAR

PEN: Parity Enable bit
1 = Enable
0 = Disable

FE: Framing Error flag
1 = The Stop Bit received was not a 1. It must be reset at the start of every reception.
0 = No Error

TPAR: Transmit Parity Control. This bit must be initialized at the start of every reception.
1 = Odd
0 = Even

RPAR: Receive Parity Control/Status. This bit has two functions, control and status. Before reception, initialize for Even (0) or Odd (1) parity. If at the end of a reception this bit is a 1, a parity error has occurred. This bit must be initialized before the start of each reception.

0: Write 0 to these bits

PTSCON1—SSIO MODE

msb							lsb
0	0	0	0	0	0	TRC	0

TRC: Transmit/Receive Control
1 = Receive/Transmit bit on first PTS request and every other one thereafter
0 = Receive/Transmit data bit on second PTS request and every other one thereafter. Throughout the transmission/reception, this bit is toggled.

0: Write 0 to these bits

4.0 PIN DEFINITION TABLE

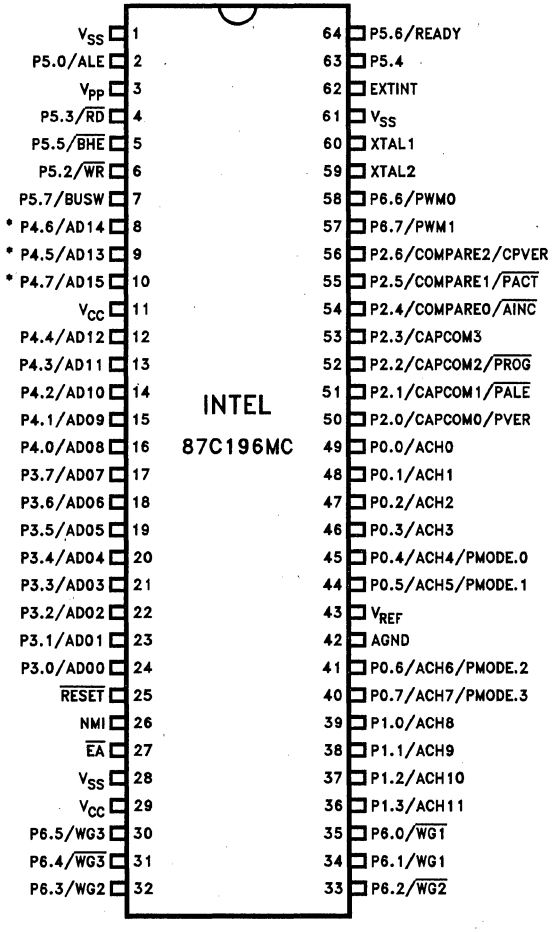
8XC196MC Package Pin Assignments

PLCC Pin #	QFP Pin #	SDIP Pin #	Description	PLCC Pin #	QFP Pin #	SDIP Pin #	Description
1	73	63	P5.4	43	31		V_{SS}
2	74	64	P5.6/READY	44	32	33	P6.2/$\overline{WG2}$
3	75		P5.1/INST	45	33	34	P6.1/WG1
4	76	1	V_{SS}	46	34	35	P6.0/$\overline{WG1}$
5	77	2	P5.0/ALE	47	35	36	P1.3/ACH11
6	78	3	V_{PP}	48	36	37	P1.2/ACH10
7	79	4	P5.3/$\overline{RD}$	49	37		V_{SS}
8	80	5	P5.5/$\overline{BHE}$	50	38		P1.4/ACH12
9			NC	51	39	38	P1.1/ACH9
10	1	6	P5.2/$\overline{WR}$	52	40	39	P1.0/ACH8
11	2	7	P5.7/BUSW	53	41	40	P0.7/ACH7/PMODE.3
12	3	10	P4.7/AD15	54	42	41	P0.6/ACH6/PMODE.2
13	4	8	P4.6/AD14	55	43	42	AGND
14	5	11	V_{CC}	56	44	43	V_{REF}
15	6	9	P4.5/AD13	57	45	44	P0.5/ACH5/PMODE.1
16	7		CLKOUT	58	46	45	P0.4/ACH4/PMODE.0
17	8	12	P4.4/AD12	59	47	46	P0.3/ACH3
18	9	13	P4.3/AD11	60	48	47	P0.2/ACH2
19	10	14	P4.2/AD10	61	49	48	P0.1/ACH1
20	11	15	P4.1/AD09	62	50	49	P0.0/ACH0
21	12	16	P4.0/AD08	63	51		NC
22			NC	64	52	50	P2.0/CAPCOMP0/PVER
23			NC	65	53	51	P2.1/CAPCOMP1/PALE
24	13	17	P3.7/AD07	66	54		NC
25	14	18	P3.6/AD06	67	55		NC
26	15	19	P3.5/AD05	68	56	52	P2.2/CAPCOMP2/$\overline{PROG}$
27	16	20	P3.4/AD04	69	57	53	P2.3/CAPCOMP2
28	17	21	P3.3/AD03	70	58		P2.7/COMPARE3
29	18	22	P3.2/AD02	71	59		NC
30	19	23	P3.1/AD01	72	60		NC
31	20	24	P3.0/AD00	73	61	54	P2.4/COMPARE0/$\overline{AINC}$
32	21		NC	74	62	55	P2.5/COMPARE1/$\overline{PACT}$
33	22	25	$\overline{RESET}$	75	63	56	P2.6/COMPARE2/CPVER
34	23	26	NMI	76	64	57	P6.7/PWM1
35			NC	77	65	58	P6.6/PWM0
36	24	27	EA	78	66		NC
37	25	28	V_{SS}	79	67		NC
38	26		V_{SS}	80	68		NC
39	27	29	V_{CC}	81	69	59	XTAL2
40	28	30	P6.5/WG3	82	70	60	XTAL1
41	29	31	P6.4/$\overline{WG3}$	83	71	61	V_{SS}
42	30	32	P6.3/WG2	84	72	62	EXTINT

5.0 PACKAGE PIN ASSIGNMENT

Package Prefix Identification Table

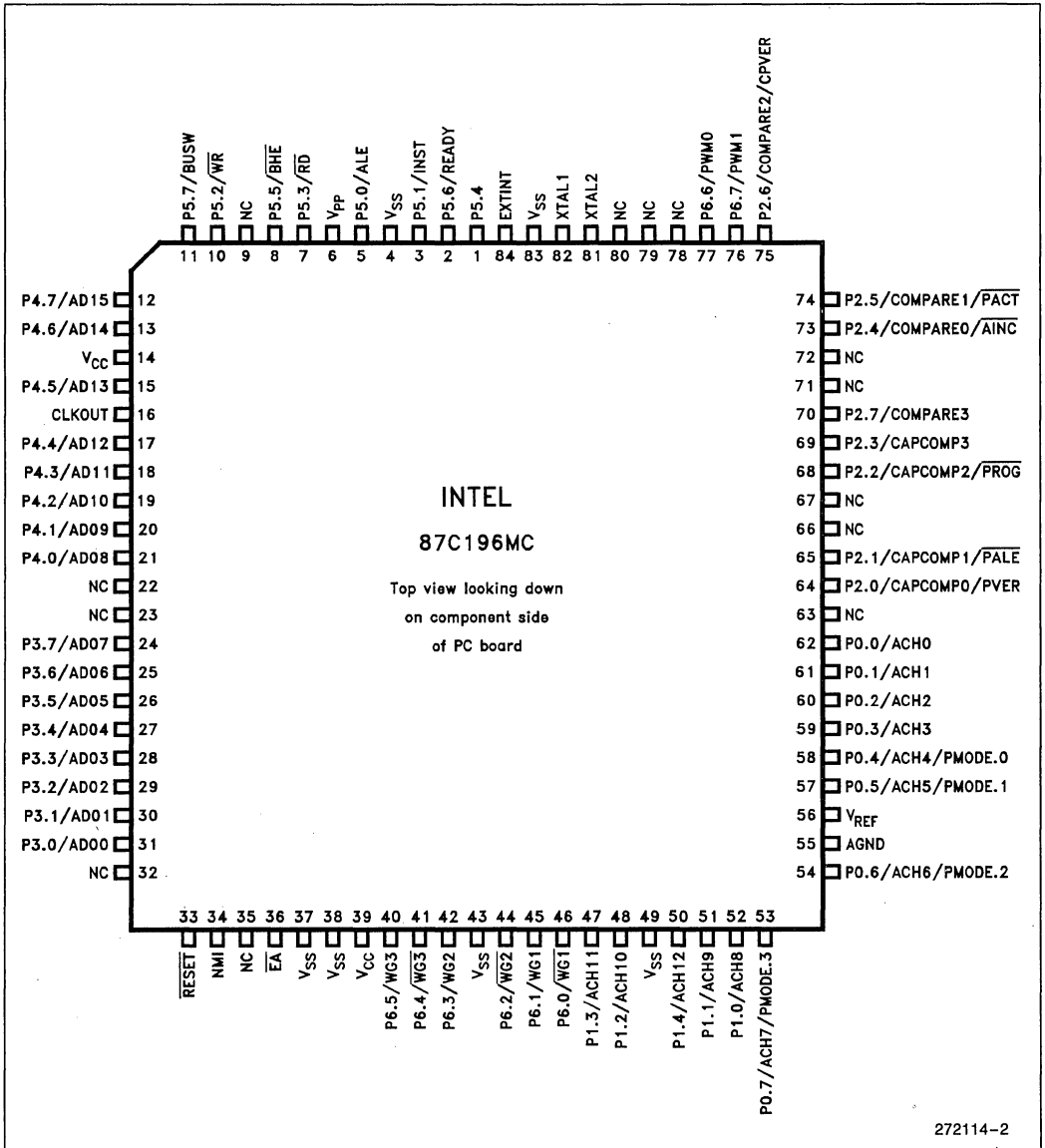
Package	Device
PLCC	N87C196MC
EIAJQFP	S87C196MC
SDIP	U87C196MC



272114-1

NOTE:
*The pin sequence is correct.

64-Lead SDIP Package Pinout



NOTE:
NC means No Connect. Do not connect these pins.

84-Lead PLCC Package Pinout

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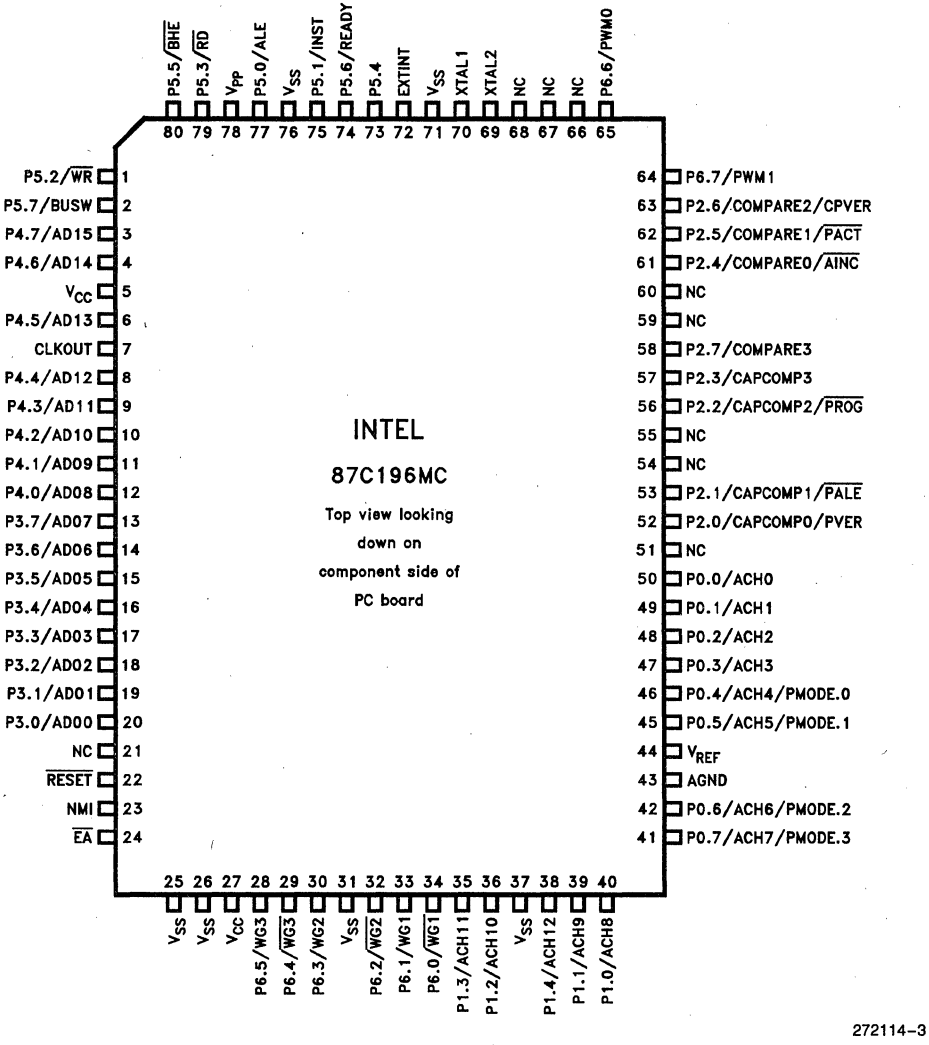

NOTE:
NC means No Connect. Do not connect these pins.

80-Lead Shrink EIAJQFP (Quad Flat Pack)

6.0 PIN DESCRIPTIONS

Symbol	Name and Function
ACH0–ACH12 (P0.0–P0.7, P1.0–P1.4)	Analog inputs to the on-chip A/D converter. ACH0–7 share the input pins with P0.0–7 and ACH8–12 share pins with P1.0–4. If the A/D is not used, the port pins can be used as standard input ports.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
ALE/$\overline{ADV}$ (P5.0)	Address Latch Enable or Address Valid output, as selected by CCR. Both options allow a latch to demultiplex the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. When the pin is ALE, the address can be latched on the falling edge. ALE/$\overline{ADV}$ is active only during external memory accesses. Can be used as standard I/O when not used as ALE/ADV.
$\overline{BHE}$/$\overline{WRH}$ (P5.5)	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. If the $\overline{WRH}$ function is selected, the pin will go low when the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory cycles. Can be used as standard I/O when not used as a bus control signal.
BUSWIDTH (P5.7)	Input for bus width selection. If CCR bits 1 and 2 = 1, this pin dynamically controls the bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If it is high, a 16-bit cycle occurs. This pin can be used as standard I/O when not used as BUSWIDTH.
CAPCOMP0–CAPCOMP3 (P2.0–P2.3)	The EPA Capture/Compare pins. These pins share P2.0–P2.3. If not used for EPA, they can be configured as standard I/O pins.
CLKOUT	Output of the internal clock generator. The frequency is ½ of the oscillator frequency. It has a 50% duty cycle.
COMPARE0–COMPARE3 (P2.4–P2.7)	The EPA Compare pins. These pins share P2.4–P2.7. If not used for EPA, they can be configured as standard I/O pins.
$\overline{EA}$	External Access enable pin. $\overline{EA}$ = 0 causes all memory accesses to be external to the chip. $\overline{EA}$ = 1 causes memory accesses from locations 2000H to 5FFFH to be from the on-chip OTPROM/ROM. $\overline{EA}$ = 12.5V causes execution to begin in the programming mode. $\overline{EA}$ is latched at reset.
EXTINT	A programmable input on this pin causes a maskable interrupt vector through memory location 203CH. The input may be selected to be a positive/negative edge or a high/low level.
INST (P5.1)	INST is high during the instruction fetch from the external memory and throughout the bus cycle. It is low otherwise. This pin can be configured as standard I/O if not used as INST.
NMI	A positive transition on this pin causes a non-maskable interrupt which vectors to memory location 203EH. If not used, it should be tied to V_{SS}. May be used by Intel Evaluation boards.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port0 pins should not be left floating. These pins also used to select programming modes in the OTPROM devices.
PORT1	5-bit high impedance input-only port. P1.0–P1.4 are also used as A/D converter inputs. In addition, P1.2 and P1.3 can be used as Timer 1 clock input and direction select respectively.

6.0 PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
PORT2	8-bit bidirectional I/O port. All of the Port2 pins are shared with the EPA I/O pins (CAPCOMP0–3 and COMPARE0–3).
PORT3, PORT4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which uses strong internal pullups.
PORT5	8-bit bidirectional I/O port. 7 of the pins are shared bus control signals ($\overline{ALE}$, INST, $\overline{WR}$, $\overline{RD}$, $\overline{BHE}$, READY, BUSWIDTH). Can be used as standard I/O.
PORT6	8-bit output-only port. P6.6 and P6.7 output PWM and the rest are used as the Wave Generator outputs. Can be used as standard output ports.
PWM0, PWM1 (P6.6, P6.7)	Programmable duty cycle, programmable frequency Pulse Width Modulator pins. The duty cycle has a resolution of 256 steps, and the frequency can vary from 122 Hz to 31 KHz (16 MHz input clock). Pins may be configured as standard output if PWM is not used.
$\overline{RD}$ (P5.3)	Read signal output to external memory. $\overline{RD}$ is low only during external memory reads. Can be used as standard I/O when not used as $\overline{RD}$.
READY (P5.6)	Ready input to lengthen external memory cycles. If READY = 0, the memory controller inserts wait states until the next positive transition of CLKOUT occurs with READY = 1. Can be used as standard I/O when not used as READY.
$\overline{RESET}$	Reset input to and open drain output from the chip. Held low for at least 16 state times to reset the chip. Input high for normal operation. $\overline{RESET}$ has an Ohmic internal pullup resistor.
T1CLK (P1.2)	Timer 1 Clock input. This pin has two other alternate functions: ACH10 and P1.2.
T1DIR (P1.3)	Timer 1 Direction input. This pin has two other alternate functions: ACH11 and P1.3.
V_{PP}	The programming voltage is applied to this pin. It is also the timing pin for the return from Power Down circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If the Power Down feature is not used, connect the pin to V_{CC}.
WG1–WG3/$\overline{WG1}$–$\overline{WG3}$ (P6.0–P6.5)	3-phase output signals and their complements used in motor control applications. The pins can also be configured as standard output pins.
$\overline{WR}$/$\overline{WRL}$ (P5.2)	Write and Write Low output to external memory. $\overline{WR}$ will go low every external write. $\overline{WRL}$ will go low only for external writes to an even byte. Can be used as standard I/O when not used as $\overline{WR}$/$\overline{WRL}$.
XTAL1	Input of the oscillator inverter and the internal clock generator. This pin should be used when using an external clock source.
XTAL2	Output of the oscillator inverter.

Programming Mode Pin Definitions

Name	Name and Function
PMODE.0–3 (P0.4–7)	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operation.
$\overline{\text{PALE}}$ (P2.1)	Programming ALE Input. Accepted by an 8XC196MC that is in slave programming mode. Used to indicate that port 3 and 4 contain a command/ address.
$\overline{\text{PROG}}$ (P2.2)	Programming. Falling edge latches data on PBUS and begins programming. Rising edge input ends programming.
$\overline{\text{PACT}}$ (P2.5)	Programming Active. Use to indicate when programming activity is complete.
PVER (P2.0)	Programming Verification. Signal is low after rising edge of PROG if they programming was not successful.
$\overline{\text{AINC}}$ (P2.4)	Auto Increment. Active low input enables the auto increment mode. Auto increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
PORTS 3 and 4 (During Programming)	Address/Command/Data Bus. Used to pass commands, addresses and data to and from 8XC196MC. Also used in the auto programming mode as a regular system bus to access external memory.
CPVER (P2.6)	Cumulative Program Verification. Pin is high if all locations since entering a programming mode have programmed correctly.

Programming Mode PMODE Values

PMODE	Programming Mode
0	Reserved
1–4	Reserved
5	Slave Programming
6	ROM Dump
7–8	Reserved
9	UPROM Programming
0AH–0BH	Reserved
0CH	Auto Programming
0DH	PCCB Programming
0EH–0FH	Reserved

7.0 OPCODE TABLE

00	SKIP	31	JBC	61	AND IMMEDIATE (2 OPS)
01	CLR	32	JBC	62	AND INDIRECT (2 OS)
02	NOT	33	JBC	63	AND INDEXED (2 OPS)
03	NEG	34	JBC	64	ADD DIRECT (2 OPS)
04	XCH	35	JBC	65	ADD IMMEDIATE (2 OPS)
05	DEC	36	JBC	66	ADD INDIRECT (2 OPS)
06	EXT	37	JBC	67	ADD INDEXED (2 OPS)
07	INC	38	JBS	68	SUB DIRECT (2 OPS)
08	SHR	39	JBS	69	SUB IMMEDIATE (2 OPS)
09	SHL	3A	JBS	6A	SUB INDIRECT (2 OPS)
0A	SHRA	3B	JBS	6B	SUB INDEXED (2 OPS)
0B	XCH	3C	JBS	6C	MULU DIRECT (2 OPS)
0C	SHRL	3D	JBS	6D	MULU IMMEDIATE (2 OPS)
0D	SHLL	3E	JBS	6E	MULU INDIRECT (2 OPS)
0E	SHRAL	3F	JBS	6F	MULU INDEXED (2 OPS)
0F	NORMAL	40	AND DIRECT (3 OPS)	70	ANDB DIRECT (2 OPS)
10	RESERVED	41	AND IMMEDIATE (3 OPS)	71	ANDB IMMEDIATE (2 OPS)
11	CLRB	42	AND INDIRECT (3 OPS)	72	ANDB INDIRECT (2 OPS)
12	NOTB	43	AND INDEXED (3 OPS)	73	ANDB INDEXED (2 OPS)
13	NEGB	44	ADD DIRECT (3 OPS)	74	ADDB DIRECT (2 OPS)
14	XCHB	45	ADD IMMEDIATE (3 OPS)	75	ADDB IMMEDIATE (2OPS)
15	DECB	46	ADD INDIRECT (3 OPS)	76	ADDB INDIRECT (2 OPS)
16	EXTB	47	ADD INDEXED (3 OPS)	77	ADDB INDEXED (2 OPS)
17	INCB	48	SUB DIRECT (3 OPS)	78	SUBB DIRECT (2 OPS)
18	SHRB	49	SUB IMMEDIATE (3 OPS)	79	SUBB IMMEDIATE (2 OPS)
19	SHLB	4A	SUB INDIRECT (3 OPS)	7A	SUBB INDIRECT (2 OPS)
1A	SHRAB	4B	SUB INDEXED (3 OPS)	7B	SUBB INDEXED (2 OPS)
1B	XCHB	4C	MULU DIRECT (3 OPS)	7C	MULUB DIRECT (2 OPS)
1C	RESERVED	4D	MULU IMMEDIATE (3 OPS)	7D	MULUB IMMEDIATE (2 OPS)
1D	RESERVED	4E	MULU INDIRECT (3 OPS)	7E	MULUB INDIRECT (2 OPS)
1E	RESERVED	4F	MULU INDEXED (3 OPS)	7F	MULUB INDEXED (2 OPS)
1F	RESERVED	50	ANDB DIRECT (3 OPS)	80	OR DIRECT
20	SJMP	51	ANDB IMMEDIATE (3 OPS)	81	OR IMMEDIATE
21	SJMP	52	ANDB INDIRECT (3 OPS)	82	OR INDIRECT
22	SJMP	53	ANDB INDEXED (3 OPS)	83	OR INDEXED
23	SJMP	54	ADDB DIRECT (3 OPS)	84	XOR DIRECT
24	SJMP	55	ADDB IMMEDIATE (3 OPS)	85	XOR IMMEDIATE
25	SJMP	56	ADDB INDIRECT (3 OPS)	86	XOR INDIRECT
26	SJMP	57	ABBD INDEXED (3 OPS)	87	XOR INDEXED
27	SJMP	58	SUBB DIRECT (3 OPS)	88	CMP DIRECT
28	SCALL	59	SUBB IMMEDIATE (3 OPS)	89	CMP IMMEDIATE
29	SCALL	5A	SUBB INDIRECT (3 OPS)	8A	CMP INDIRECT
2A	SCALL	5B	SUBB INDEXED (3 OPS)	8B	CMP INDEXED
2B	SCALL	5C	MULUB DIRECT (3 OPS)	8C	DIVU DIRECT
2C	SCALL	5D	MULUB IMMEDIATE (3 OPS)	8D	DIVU IMMEDIATE
2D	SCALL	5E	MULUB INDIRECT (3 OPS)	8E	DIVU INDIRECT
2E	SCALL	5F	MULUB INDEXED (3 OPS)	8F	DIVU INDEXED
2F	SCALL	60	AND DIRECT (2 OPS)		
30	JBC				

7.0 OPCODE TABLE (Continued)

90	ORB DIRECT	B6	ADDCB INDIRECT	DB	JC
91	ORB IMMEDIATE	B7	ADDCB INDEXED	DC	JVT
92	ORB INDIRECT	B8	SUBCB DIRECT	DD	JV
93	ORB INDEXED	B9	SUBCB IMEDIATE	DE	JLT
94	XORB DIRECT	BA	SUBCB INDIRECT	DF	JE
95	XORB IMMEDIATE	BB	SUBCB INDEXED	E0	DJNZ
96	XORB INDIRECT	BC	LDBSE DIRECT	E1	DJNZW
97	XORB INDEXED	BD	LDBSE IMMEDIATE	E2	TIJMP
98	CMPB DIRECT	BE	LDBSE INDIRECT	E3	BR (INDIRECT)
99	CMPB IMMEDIATE	BF	LDBSE INDEXED	E4	RESERVED
9A	CMPB INDIRECT	C0	ST DIRECT	E5	RESERVED
9B	CMPB INDEXED	C1	BMOV	E6	RESERVED
9C	DIVUB DIRECT	C2	ST INDIRECT	E7	LJMP
9D	DIVUB IMMEDIATE	C3	ST INDEXED	E8	RESERVED
9E	DIVUB INDIRECT	C4	STB DIRECT	E9	RESERVED
9F	DIVUB INDEXED	C5	CMPL	EA	RESERVED
A0	LD DIRECT	C6	STB INDIRECT	EB	RESERVED
A1	LD IMMEDIATE	C7	STB INDEXED	EC	DPTS
A2	LD INDIRECT	C8	PUSH DIRECT	ED	EPTS
A3	LD INDEXED	C9	PUSH IMMEDIATE	EE	RESERVED
A4	ADDC DIRECT	CA	PUSH INDIRECT	EF	LCALL
A5	ADDC IMMEDIATE	CB	PUSH INDEXED	F0	RET
A6	ADDC INDIRECT	CC	POP DIRECT	F1	RESERVED
A7	ADDC INDEXED	CD	BMOVI	F2	PUSHF
A8	SUBC DIRECT	CE	POP INDIRECT	F3	POPF
A9	SUBC IMMEDIATE	CF	POP INDEXED	F4	PUSHA
AA	SUBC INDIRECT	D0	JNST	F5	POPA
AB	SUBC INDEXED	D1	JNH	F6	IDLPD
AC	LDBZE DIRECT	D2	JGT	F7	TRAP
AD	LDBZE IMMMEDIATE	D3	JNC	F8	CLRC
AE	LDBZE INDIRECT	D4	JNVT	F9	SETC
AF	LDBZE INDEXED	D5	JNV	FA	DI
B0	LDB DIRECT	D6	JGE	FB	EI
B1	LDB IMMEDIATE	D7	JNE	FC	CLRVT
B2	LDB INDIRECT	D8	JST	FD	NOP
B3	LDB INDEXED	D9	JH	FE	*DIV/DIVB/MUL/MULB
B4	ADDCB DIRECT	DA	JLE	FF	RST
B5	ADDCB IMMEDIATE				

NOTES:
*Two byte instruction
RESERVED—Execution of reserved instructions will cause Unimplemented Opcode interrupt.

8.0 INSTRUCTION SET SUMMARY

Mnemonic	Operands	Operation(1)	Flags(2) Z	N	C	V	VT	ST	Notes
ADD/ADDB	2	D = D + A	↗	↗	↗	↗	↑		
ADD/ADDB	3	D = B + A	↗	↗	↗	↗	↑		
ADDC/ADDCB	2	D = D + A + C	↓	↗	↗	↗	↑		
SUB/SUBB	2	D = D − A	↗	↗	↗	↗	↑		
SUB/SUBB	3	D = B − A	↗	↗	↗	↗	↑		
SUBC/SUBCB	2	D = D − A + C − 1	↓	↗	↗	↗	↑		
CMP/CMPB/CMPL	2	D − A	↗	↗	↗	↗	↑		
MUL/MULU	2	D,D + 2 = D × A							3
MUL/MULU	3	D,D + 2 = D × A							3
MULB/MULUB	2	D,D + 1 = D × A							4
MULB/MULUB	3	D,D + 1 = B × A							4
DIVU	2	D = (D,D + 2)/A,D + 2 = remainder				↗	↑		3
DIVUB	2	D = (D,D + 1)/A,D + 1 = remainder				↗	↑		4
DIV	2	D = (D,D + 2)/A,D +2 = remainder				↗	↑		
DIVB	2	D = (D,D + 1)/A,D + 1 = remainder				↗	↑		
AND/ANDB	2	D = D and A	↗	↗	0	0			
AND/ANDB	3	D = B and A	↗	↗	0	0			
OR/ORB	2	D = D or B	↗	↗	0	0			
XOR/XORB	2	D = D (exclusive or) A	↗	↗	0	0			
LD/LDB	2	D = A							
ST/STB	2	A = D							
XCH	2	D ⟷ A; D + 1 ⟷ A + 1							
XCHB	2	D ⟷ A							
BMOV, BMOVI	2	(PTR__HI) + = (PTR__LOW) +; Until COUNT = 0							
LDBSE	2	D = A; D + 1 = Sign (A)							4, 5
LDBZE	2	D = A; D + 1 = 0							4, 5
PUSH	1	SP = SP − 2; (SP) = A							
POP	1	A = (SP); SP = SP + 2							
PUSHF	0	SP = SP − 2; (SP) = PSW; PSW = 0; I = 0; PSE = 0	0	0	0	0	0	0	11
POPF	0	PSW = (SP); SP = SP + 2;1 → ↗	↗	↗	↗	↗	↗	↗	11
PUSHA	0	SP = SP − 2;(SP) = PSW;PSW = 0000h; SP = SP −2;(SP) = IMASKI/WSR; IMASKI = 00h; I = 0; PSE = 0	0	0	0	0	0	0	11

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation(1)	Flags(2) Z	N	C	V	VT	ST	Notes
POPA	0	IMASKI/WSR = (SP); SP = SP + 2; PSW = (SP); SP = SP + 2	✓	✓	✓	✓	✓	✓	
SJMP	1	PC = PC + 11-Bit-Offset							6
LJMP	1	PC = PC + 16-Bit-Offset							6
BR[Indirect]	1	PC = (A)							
TIJMP	3	PC = ([index] and MASK)2 + (Table)							
TRAP	0	SP = SP −2; (SP) = PC; PC = (2010h)							10
SCALL	1	SP = SP − 2; (SP) = PC; PC = PC + 11-Bit Offset							6
LCALL	1	SP = SP − 2; (SP) = PC. PC = PC + 16-Bit-Offset							6
RET	0	PC = (SP); SP = SP + 2							
J (conditional)	1	PC = PC + 8-Bit-Offset (If Taken)							6
JC	1	Jump if C = 1							6
JNC	1	Jump if C = 0							6
JE	1	Jump if Z = 1							6
JNE	1	Jump if Z = 0							6
JGE	1	Jump if N = 0							6
JLT	1	Jump if N = 1							6
JGT	1	Jump if N = 0 and Z = 0							6
JLE	1	Jump if N = 1 or Z = 1							6
JH	1	Jump if C = 1 and Z = 0							6
JNH	1	Jump if C = 0 or Z = 1							6
JV	1	Jump if V = 1							6
JNV	1	Jump if V = 0							6
JVT	1	Jump if VT = 1; Clear VT					0		6
JNVT	1	Jump if VT = 0; Clear VT					0		6
JST	1	Jump if ST = 1							6
JNST	1	Jump if ST = 0							6
JBS	3	Jump if Specific Bit = 1							6, 7
JBC	3	Jump if Specific Bit = 0							6, 7
DJNZ/DJNZW	1	D = D − 1; If D ≠ 0 then PC = PC + 8-Bit-Offset							6
DEC/DECB	1	D = D − I	✓	✓	✓	✓	↑		
NEG/NEGB	1	D = 0 − D	✓	✓	✓	✓	↑		

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8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation(1)	Flags(2) Z	N	C	V	VT	ST	Notes
INC/INCB	1	D = D + 1	✓	✓	✓	✓	↑		
EXT	1	D = D; D + 2 = Sign (D)	✓	✓	0	0			3
EXTB	1	D = D; D + 1 Sign (D)	✓	✓	0	0			4
NOT/NOTB	1	D = Logical Not (D)	✓	✓	0	0			
CLR/CLRB	1	D = 0	1	0	0	0			
SHL/SHLB/SHLL	2	C ← msb . . .lsb ← 0	✓	✓	✓	✓	↑		8
SHR/SHRB/SHRL	2	0 → msb . . . lsb → C	✓	✓	✓	0		✓	8
SHRA/SHRAB/SHRAL	2	msb → msb . . . lsb → C	✓	✓	✓	0		✓	8
NORML	2	Left Shift until msb = 1; D = Shift Count	✓	✓	0				8
SETC	0	C = 1			1				
CLRC	0	C = 0			0				
CLRVT	0	VT = 0					0		
RST	0	PC = 2080H	0	0	0	0	0	0	9
DI	0	Disable All Interrupts (I = 0)							
EI	0	Enable All Interrupts (I = 1)							
DPTS	0	Disable PTS Interrupts (PSE = 0)							
EPTS	0	Enable PTS Interrupts (PSE = 1)							
NOP	0	PC = PC + 1							
SKIP	0	PC = PC + 2							
IPLPD	1	Idle Mode IF Key = 1; Powerdown Mode IF Key = 2 Chip RESET Otherwise							

NOTES:
1. If the mnemonic ends in "B" a byte operation is performed, otherwise a word operation is performed. Operands D, B and A must conform to the alignment rules for the required operand type. D and B are locations in the Lower Register File; A can be located anywhere in memory.
2. The symbols indicate the effects on the flags:
   - ✓ Cleared or set as appropriate
   - 0 Cleared
   - 1 Set
   - ↑ Set if appropriate; never cleared
   - ↓ Cleared if appropriate; never set
3. D.D + 2 are consecutive WORDs in memory; D is DOUBLE-WORD aligned.
4. D.D + 1 are consecutive BYTEs in memory; D is WORD aligned.
5. Changes a BYTE to WORD.
6. Offset is a 2's complement number.
7. Specific Bit must be in or windowed into the Lower Register File.
8. The "L" (LONG) suffix indicates DOUBLE-WORD operations.
9. Initiates a RESET by pulling RESET low. Software should re-initialize all the necessary registers with code starting at 2080H.
10. The assembler does not accept this mnemonic (use the macro file for definition).
11. I = Interrupt Enable (PSW.9).

9.0 INSTRUCTION LENGTH/OPCODES

Mnemonic	Direct	Immed	Indirect		Indexed	
			Normal(1)	A-inc(1)	Short(1)	Long(1)
ADD (3-op)	4/44	5/45	4/46	4/46	5/47	6/47
SUB (3-op)	4/48	5/49	4/4A	4/4A	5/4B	6/4B
ADD (2-op)	3/64	4/65	3/66	3/66	4/67	5/67
SUB (2-op)	3/68	4/69	3/6A	3/6A	4/6B	5/6B
ADDC	3/A4	4/A5	3/A6	3/A6	4/A7	5/A7
SUBC	3/A8	4/A9	3/AA	3/AA	4/AB	5/AB
CMP	3/88	4/89	3/8A	3/8A	4/8B	5/8B
ADDB (3-op)	4/54	4/55	4/56	4/56	5/57	6/57
SUBB (3-op)	4/58	4/59	4/5A	4/5A	5/5B	6/5B
ADDB (2-op)	3/74	3/75	3/76	3/76	4/77	5/77
SUBB (2-op)	3/78	3/79	3/7A	3/7A	4/7B	5/7B
ADDCB	3/B4	3/B5	3/B6	3/B6	4/B7	5/B7
SUBCB	3/B8	3/B9	3/BA	3/BA	4/BB	5/BB
CMPB	3/98	3/99	3/9A	3/9A	4/9B	5/9B
MUL (3-op)	5/(2)	6/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULU (3-op)	4/4C	5/4D	4/4E	4/4E	5/4F	6/4F
MUL (2-op)	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULU (2-op)	3/6C	4/6D	3/6E	3/6E	4/6F	5/6F
DIV	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVU	3/8C	4/8D	3/8E	3/8E	4/8F	5/8F
MULB (3-op)	5/(2)	5/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULUB (3-op)	4/5C	4/5D	4/5E	4/5E	5/5F	6/5F
MULB (2-op)	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULUB (2-op)	3/7C	3/7D	3/7E	3/7E	4/7F	5/7F
DIVB	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVUB	3/9C	3/9D	3/9E	3/9E	4/9F	5/9F
AND (3-op)	4/40	5/41	4/42	4/42	5/43	6/43
AND (2-op)	3/60	4/61	3/62	3/62	4/63	5/63
OR (2-op)	3/80	4/81	3/82	3/82	4/83	5/83
XOR	3/84	4/85	3/86	3/86	4/87	5/87
ANDB (3-op)	4/50	4/51	4/52	4/52	5/53	5/53
ANDB (2-op)	3/70	3/71	3/72	3/72	4/73	4/73
ORB (2-op)	3/90	3/91	3/92	3/92	4/93	5/93
XORB	3/94	3/95	3/96	3/96	4/97	5/97
PUSH	2/C8	3/C9	2/CA	2/CA	3/CB	4/CB
POP	2/CC	—	2/CE	2/CE	3/CF	4/CF

Instruction Length (in bytes)/Opcode

Mnemonic	Direct	Immed	Indirect		Indexed	
			Normal	A-inc	Short	Long
LD	3/A0	4/A1	3/A2	3/A2	4/A3.	5/A3
LDB	3/B0	3/B1	3/B2	3/B2	4/B3	5/B3
ST	3/C0	—	3/C2	3/C2	4/C3	5/C3
STB	3/C4	—	3/C6	3/C6	4/C7	5/C7
XCH	3/04	—	—	—	4/0B	5/0B
XCHB	3/14	—	—	—	4/1B	5/1B
LDBSE	3/BC	3/BD	3/BE	3/BE	4/BF	5/BF
LBSZE	3/AC	3/AD	3/AE	3/AE	4/AF	5/AF

Mnemonic	Length/Opcode
PUSHF	1/F2
POPF	1/F3
PUSHA	1/F4
POPA	1/F5
TRAP	1/F7
LCALL	3/EF
SCALL	2/28-2F(3)
RET	1/F0
LJMP	3/E7
SJMP	2/20-27(3)
BR[ ]	2/E3
TIJMP	4/E2
JNST	1/D0
JST	1/D8
JNH	1/D1
JH	1/D9
JGT	1/D2
JLE	1/DA
JNC	1/B3
JC	1/D8
JNVT	1/D4
JVT	1/DC
JNV	1/D5
JV	1/DD
JGE	1/D6
JLT	1/DE
JNE	1/D7
JE	1/DF
JBC	3/30-37
JBS	3/38-3F

Mnemonic	Length/Opcode
DJNZ	3/E0
DJNZW	3/E1
NORML	3/0F
SHRL	3/0C
SHLL	3/0D
SHRAL	3/0E
SHR	3/08
SHRB	3/18
SHL	3/09
SHLB	3/19
SHRA	3/0A
SHRAB	3/1A
CLRC	1/F8
SETC	1/F9
DI	1/FA
EI	1/FB
DPTS	1/EC
EPTS	1/ED
CLRVT	1/FC
NOP	1/FD
RST	1/FF
SKIP	2/00
IDLPD	1/F6
BMOV	3/C1
BMOVI	3/CD

NOTES:
1. Indirect and indirect + share the same opcodes, as do short and long indexed opcodes. If the second byte is even, use indirect or short indexed. If odd, use indirect or long indexed.
2. The opcodes for signed multiply and divide are the unsigned opcode with an "FE" prefix.
3. The 3 least significant bits of the opcode are concatenated with the 8 bits to form an 11-bit, 2's complement offset.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES)

Instruction	Direct	Immediate	Indirect		Indexed	
			Normal	A-inc	Short	Long
ADD (3op)	5	6	7/10	8/11	7/10	8/11
SUB (3op)	5	6	7/10	8/11	7/10	8/11
ADD (2op)	4	5	6/8	7/9	6/8	7/9
SUB (2op)	4	5	6/8	7/9	6/8	7/9
ADDC	4	5	6/8	7/9	6/8	7/9
SUBC	4	5	6/8	7/9	6/8	7/9
CMP	4	5	6/8	7/9	6/8	7/9
ADDB (3op)	5	5	7/10	8/11	7/10	8/11
SUBB (3op)	5	5	7/10	8/11	7/10	8/11
ADDB (2op)	4	4	6/8	7/9	6/8	7/9
SUBB (2op)	4	4	6/8	7/9	6/8	7/9
ADDCB	4	4	6/8	7/9	6/8	7/9
SUBCB	4	4	6/8	7/9	6/8	7/9
CMPB	4	4	6/8	7/9	6/8	7/9
CMPL	7					
MUL (3op)	16	17	18/21	19/22	19/22	20/23
MULU (3op)	14	15	16/19	17/20	17/20	18/21
MUL (2op)	16	17	18/21	19/22	19/22	20/23
MULU (2op)	14	15	16/19	17/20	17/20	18/21
DIV	26	27	28/31	29/32	29/32	30/33
DIVU	24	25	26/29	27/30	27/30	28/31
MULB (3op)	12	12	14/17	15/18	15/18	16/19
MULUB (3op)	10	10	12/15	12/16	12/16	14/17
MULB (2op)	12	12	14/17	15/18	15/18	16/19
MULUB (2op)	10	10	12/15	12/16	12/16	14/17
DIVB	18	18	20/23	21/24	21/24	22/25
DIVUB	16	16	18/21	19/22	19/22	20/23
AND (3op)	5	6	7/10	8/11	7/10	8/11
AND (2op)	4	5	6/8	7/9	6/8	7/9
OR	4	5	6/8	7/9	6/8	7/9
XOR	4	5	6/8	7/9	6/8	7/9
ANDB (3op)	5	5	7/10	8/11	7/10	8/11
ANDB (2op)	4	4	6/8	7/9	6/8	7/9
ORB	4	4	6/8	7/9	6/8	7/9
XORB	4	4	6/8	7/9	6/8	7/9
LD	4	5	5/8	6/8	6/9	7/10
ST	4		5/8	6/9	6/9	7/10
XCH	5				8/13	9/14
LDB	4	4	5/8	6/8	6/9	7/10

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed	
			Normal	A-inc	Short	Long
STB	4		5/8	6/9	6/9	7/10
XCHB	5				8/13	9/14
BMOV	6 + 8 per Word		6 + 11 14 per Word			
BMOVI	7 + 8 per Word + 14 for Each Interrupt		7 + 11/ 14 per Word + 14 for Each Interrupt			
LDBSE, LDBZE	4	4	5/7	6/8	6/8	7/9
PUSH (int)	6	7	9/12	10/13	10/13	11/14
POP (int)	8		10/12	11/13	11/13	12/14
PUSHF (int)	6					
POPF (int)	7					
PUSHA (int)	12					
POPA (int)	12					
PUSH (ext)	8	9	11/14	12/15	12/15	13/16
POP (ext)	11		13/15	14/16	14/16	15/17
PUSHF (ext)	8					
POPF (ext)	10					
PUSHA (ext)	18					
POPA (ext)	18					
LJMP	7					
SJMP	7					
BR [indirect]	7					
TIJMP	15 (+ 3 for External Reference)					
TRAP (int)	16					
LCALL (int)	11					
SCALL (int)	11					
RET (int)	11					
TRAP (ext)	18					
LCALL (ext)	13					
SCALL (ext)	13					
RET (ext)	14					
JNST, JST	4/8 Jump Not Taken/Jump Taken					
JNH, JH	4/8 Jump Not Taken/Jump Taken					
JGT, JLE	4/8 Jump Not Taken/Jump Taken					
JNC, JC	4/8 Jump Not Taken/Jump Taken					
JNVT, JVT	4/8 Jump Not Taken/Jump Taken					
JNV, JV	4/8 Jump Not Taken/Jump Taken					
JGE, JLT	4/8 Jump Not Taken/Jump Taken					
JNE, JE	4/8 Jump Not Taken/Jump Taken					
JBS, JBC	5/9 Jump Not Taken/Jump Taken					
DJNZ	5/9 Jump Not Taken/Jump Taken					
DJNZW	6/10 Jump Not Taken/Jump Taken					

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect Normal	Indirect A-inc	Indexed Short	Indexed Long
CLR, NOT, NEG	3					
DEC, INC	3					
EXT	4					
CLRB, NOTB	3					
DECB, INCB	3					
NEGB	3					
EXT	4					
NORML	8 + 1 per Shift (9 for 0 Shift)					
SHRL	7 + 1 per Shift (8 for 0 Shift)					
SHLL	7 + 1 per Shift (8 for 0 Shift)					
SHRAL	7 + 1 per Shift (8 for 0 Shift)					
SHR	6 + 1 per Shift (7 for 0 Shift)					
SHL	6 + 1 per Shift (7 for 0 Shift)					
SHRA	6 + 1 per Shift (7 for 0 Shift)					
SHRB	6 + 1 per Shift (7 for 0 Shift)					
SHLB	6 + 1 per Shift (7 for 0 Shift)					
SHRAB	6 + 1 per Shift (7 for 0 Shift)					
CLRC	2					
SETC	2					
DI	2					
EI	2					
DPTS	2					
EPTS	2					
CLRVT	2					
NOP	2					
RST	20 (Includes Fetch of CCB/CCB1)					
SKIP	3					
IDLPD	8/25 (Proper Key/Improper Key)					
PTS						
Single Transfer	18	(+ 3 for Ext Reference, + 1 If XFER Count = 0				
Burst Transfer	13	(+ 7 for Each Transfer, 1 Minimum + 3 for Each Memory Controller Reference)				
PWM Modes	15					
A/D Scan Mode	12/25					

NOTES:
The timing figures are minimum execution times expressed as state times (one period of CLKOUT = two oscillator periods. Section 11.3) and are based on the following assumptions:
1. The opcode, along with any required operands, have been pre-fetched and reside in the instruction queue.
2. The bus controller operates with the 16-bit bus selected and without wait states for external memory references and pre-fetches. For instructions with indirect or indexed addressing, execution times separated by a slash are for instructions requiring a fetch from internal/external memory.
3. Times for jumps, calls, and returns include the 4 state times required to flush the pre-fetch queue and to fetch the opcode a the destination address. This is reflected in the jump taken/not-taken times shown in the table.

11.0 INTERRUPT TABLE

8XC196MC Summary of Interrupts and Priorities

Number	Source	Symbol	Vector Location	Priority
INT15	Non-Maskable Interrupt	NMI	203EH	15
PTS14–PTS0	PTS	*	*	*
INT14	EXTINT Pin	EXTINT	203CH	14
INT13	WG_COUNTER	WG	203AH	13
INT12	Reserved	—	2038H	12
INT11	Reserved	—	2036H	11
INT10	Reserved	—	2034H	10
INT09	COMPARE3	CM3	2032H	9
INT08	CAPCOMP3	CP3	2030H	8
N/A	Unimplemented Opcode	N/A	2012H	N/A
N/A	TRAP Instruction	N/A	2010H	N/A
INT07	COMPARE2	CM2	2003H	7
INT06	CAPCOMP2	CP2	200CH	6
INT05	COMPARE1	CM1	200AH	5
INT04	CAPCOMP1	CP1	2008H	4
INT03	COMPARE0	CM0	2006H	3
INT02	CAPCOMP0	CP0	2004H	2
INT01	A/D Complete	A/D DONE	2002H	1
INT00	T1/T2 Overflow	TOVF	2000H	0

NOTE:
*Refer to PTS Vector Table

Interrupt SFRs. The Interrupt SFRs are listed with their addresses:

SFR	Address
INT_MASK	08H
INT_PEND	09H
INT_PEND1	12H
INT_MASK1	13H

PTS Vector Table

Priority	Name	Source	PTS Vector
HIGHEST	PTS14	EXTINT	205CH
•	PTS13	WG_COUNT	205AH
•	PTS12	RESERVED	2058H
•	PTS11	RESERVED	2056H
•	PTS10	RESERVED	2054H
•	PTS9	COMPARE3	2052H
•	PTS8	CAPCOMP3	2050H
•	PTS7	COMPARE2	204EH
•	PTS6	CAPCOMP2	204CH
•	PTS5	COMPARE2	204AH
•	PTS4	CAPCOMP1	2048H
•	PTS3	COMPARE0	2046H
•	PTS2	CAPCOMP0	2044H
•	PTS1	A/D Done	2042H
LOWEST	PTS0	TOVF	2040H

The end-of-PTS interrupt is treated as a normal interrupt. It vectors through the associated location in the normal interrupt vector table (Table 11.1). For example, if the A/D interrupt is selected by the PTS, an A/D interrupt is directed to its PTSCB by the PTS vector at 2042H; its end-of-PTS interrupt is at 2002H. Thus, the user would write an end-of-PTS interrupt routine for TI and store a vector pointing to it at location 2002H.

An end-of-PTS interrupt has higher priority than any normal interrupt (with the exception of NMI). Within the group of end-of-PTS interrupts, the priorities are the same as for normal interrupts.

12.0 FORMULAS

State Time = 2 Oscillator periods = $\frac{2}{F_{OSC}}$

TIJMP Calculation—

Destination = ([INDEX] and INDEX_MASK) * 2 + [TBASE]

EPA Prescaler

P2	P1	P0	Divide By
0	0	0	÷ 1
0	0	1	÷ 2
0	1	0	÷ 4
0	1	1	÷ 8
1	0	0	÷ 16
1	0	1	÷ 32
1	1	0	÷ 64
1	1	1	Reserved

A/D—

$$SAM = \frac{(T_{SAM} * F_{OSC}) - 2}{8}$$

$$T_{SAM} = \frac{(8 * SAM) + 2}{F_{OSC}}$$

$$CONV = \frac{(T_{CONV} * F_{OSC}) + 3}{2 * B}$$

$$T_{CONV} = \frac{(2 * B * CONV) - 3}{F_{OSC}}$$

Programming Pulse Width—

$$PPR = \frac{((PPW) * (F_{OSC})) - 144}{144} + 32768$$

SIO Baud Rate—

BAUDCONST = F_{OSC}/(4 * Baud Rate * EPA prescale)

SSIO Baud Rate—

BAUDCONST = F_{OSC}/(8 * Baud Rate * EPA prescale)

Wave Generator Up/Down Mode—

WG_RELOAD = (F_{OSC} * PWM Period)/4

Wave Generator Up Mode—

WG_RELOAD = (F_{OSC} * PWM Period)/2

13.0 RESET STATUS

Pin States during RESET, Idle or Powerdown

Pin Name	Reset	Idle	Powerdown
$\overline{\text{RESET}}$	wk1	wk1	wk1
P5.0 (ALE)	wk1 *	(A)	(A)
P5.1 (INST)	wk1	(B)	(B)
P5.2 ($\overline{\text{WR}}$)	wk1 *	(C)	(C)
P5.3 ($\overline{\text{RD}}$)	wk1 *	(C)	(C)
P5.4	mdl *	(C)	(C)
P5.5 ($\overline{\text{BHE}}$)	wk1	(C)	(C)
P5.6 (READY)	wk1	(D)	(D)
P5.7 (BUSWIDTH)	wk1	(D)	(D)
$\overline{\text{EA}}$	HZ	HZ	HZ
NMI	wk0	wk0	wk0
P3, P4 ($\overline{\text{EA}}$ = 0)	wk1	HZ	HZ
P3, P4 ($\overline{\text{EA}}$ = 1)	wk1	ODIO	ODIO
CLKOUT	clk	clk	0, LZ
EXTINT	HZ	HZ	HZ
P0 (ACH)	HZ	HZ	HZ
P1 (ACH)	HZ	HZ	HZ
P2.0	wk1 *	(E)	(E)
P2.[7, 5:1]	wk1 *	(E)	(E)
P2.6	mdl *	(E)	(E)
P6. [5:0]	wk1	(F)	(F)
P6. [7:6]	wk0	(F)	(F)
V_{PP}	HZ	1, LZ	1, LZ
XTAL1	HZ	HZ	HZ
XTAL2	osc, LZ	osc, LZ	(G)

HZ —High Impedance
LZ —Low Impedance
wk1 —Weakly Pulled High
wk0 —Weakly Pulled Low
mdl —Medium Strength High
ODIO —Open Drain IO

* These pins are also used to control test mode entry.

(A) if P5_MODE.0 = 0 then port value
if P5_MODE.0 = 1 and OCR.3 = 1 (ALE mode) then LZ 0
if P5_MODE.0 = 1 and OCR.3 = 0 (ADV mode) then LZ 1

(B) if P5_MODE.1 = 0 then port value
if P5_MODE.1 = 1 then LZ 0

(C) if P5_MODE.y = 0 then port value
if P5_MODE.y = 1 then LZ 1

(D) if P5_MODE.y = 0 then port value
if P5_MODE.y = 1 then HZ

(E) if P2_MODE.y = 0 then port value
if P2_MODE.y = 1 then as peripheral specifies

(F) if output port then port value
if special function then as peripheral specifies

(G) if XTAL1 = 1 then LZ 0
if XTAL1 = 0 then LZ 1

SFR Reset Values

CAPCOMP0_TIME	INDETERMINATE
CAPCOMP1_TIME	INDETERMINATE
CAPCOMP2_TIME	INDETERMINATE
CAPCOMP3_TIME	INDETERMINATE
COMP0_TIME	INDETERMINATE
COMP1_TIME	INDETERMINATE
COMP2_TIME	INDETERMINATE
COMP3_TIME	INDETERMINATE
T1RELOAD	INDETERMINATE
P0_PIN	FFH (when pin is not driven)
P1_PIN	FFH (when pin is not driven)
AD_RESULT (LO)	C0H
AD_RESULT (HI)	FFH
AD_COMMAND	80H
AD_TEST	C0H
AD_TIME	FFH
PI_MASK	AAH
PI_PEND	AAH
WG_COUNT	INDETERMINATE
WG_CON	C0H
WG_PROTECT	F0H
P2_DIR, P2_REG	FFH
P2_PIN	FFH (when pin is not driven)
P5_MODE	80H IF $\overline{EA}$ = HIGH, A9H IF $\overline{EA}$ = LOW
P5_DIR, P5_PIN	FFH
P5_REG	FFH (when pin is not driven)
USFR	02H
P3_REG, P4_REG	FFH
P3_PIN, P4_PIN	FFH (when pin is not driven)

NOTE:
This table lists all the registers that their reset value is not 0.
Given values include the reserved bits (when applicable).

intel®

October 1992

8XC196NT/NQ
Quick Reference

Order Number: 272270-001

8XC196NT/NQ Quick Reference

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1.0 MEMORY MAP

FFFFFFH FFA000H	External Memory
FF9FFFH FF2080H	Internal ROM/EPROM or External Memory
FF207FH FF205EH	Reserved
FF205DH FF2040H	PTS Vectors
FF203FH FF2030H	Interrupt Vectors (Upper)
FF202FH FF2020H	ROM/EPROM Security Key
FF201FH FF201DH	Reserved
FF201CH	CCB2
FF201BH	Reserved
FF201AH	CCB1
FF2019H	Reserved
FF2018H	CCB0
FF2017H FF2014H	Reserved
FF2013H FF2000H	Interrupt Vectors (Lower)
FF1FFFH FF0600H	External Memory
FF05FFH FF0400H	Internal RAM
FF03FFH FF0100H	External Memory
FF00FFH FF0000H	Reserved for ICE
FEFFFFH 100000H	Expansion Memory for future devices
0FFFFFH • • 00A000H	984 Kbytes External Memory
009FFFH 002080H	Internal ROM/EPROM or External Memory
00207FH 00205EH	Reserved
00205DH 002040H	PTS Vectors
00203FH 002030H	Interrupt Vectors (Upper)
00202FH 002020H	ROM/EPROM Security Key
00201FH 00201DH	Reserved
00201CH	CCB2
00201BH	Reserved
00201AH	CCB1
002019H	Reserved
002018H	CCB0
002017H 002014H	Reserved
002013H 002000H	Interrupt Vectors (Lower)
001FFFH 001F00H	Internal SFRs
001EFFH 000600H	External Memory
0005FFH 000400H	Internal RAM
0003FFH 000000H	Register File

NOTE: Addresses FF2000H to FF9FFFH are remapped to 2000H to 09FFFH when $\overline{EA}$ is high and CCB2.2 is set. Otherwise they are external memory.

2.0 SFR MAP

CPU Special Function Registers

17H	(Reserved)	0BH	(Reserved)
16H	(Reserved)	0AH	WATCHDOG
15H	(Reserved)	09H	INT_PEND
14H	WSR	08H	INT_MASK
13H	INT_MASK1	07H	PTSSRV (Hi)
12H	INT_PEND1	06H	PTSSRV (Lo)
11H	(Reserved)	05H	PTSSEL (Hi)
10H	(Reserved)	04H	PTSSEL (Lo)
0FH	(Reserved)	03H	Read as FFH
0EH	(Reserved)	02H	Read as FFH
0DH	(Reserved)	01H	ZERO_REG (Hi)
0CH	(Reserved)	00H	ZERO_REG (Lo)

Memory Mapped I/O SFRs

	HIGH BYTE	LOW BYTE
1FFEH	P4_PIN	P3_PIN
1FFCH	P4_REG	P3_REG
1FFAH	SLP_CMD	SLP_CMD
1FF8H	(Reserved)	SLP_STAT
1FF6H	P5_PIN	USFR
1FF4H	P5_REG	(Reserved)
1FF2H	P5_DIR	(Reserved)
1FF0H	P5_MODE	(Reserved)
1FEEH	(Reserved)	(Reserved)
1FECH	(Reserved)	(Reserved)
1FEAH	(Reserved)	(Reserved)
1FE8H	(Reserved)	(Reserved)
1FE6H	EP_PIN	(Reserved)
1FE4H	EP_REG	(Reserved)
1FE2H	EP_DIR	(Reserved)
1FE0H	EP_MODE	IRAM_REG

Port 0, Port 1 and Port 6 SFRs

	HIGH BYTE	LOW BYTE
1FDEH	(Reserved)	(Reserved)
1FDCH	(Reserved)	(Reserved)
1FDAH	(Reserved)	P0_PIN
1FD8H	(Reserved)	(Reserved)
1FD6H	P6_PIN	P1_PIN
1FD4H	P6_REG	P1_REG
1FD2H	P6_DIR	P1_DIR
1FD0H	P6_MODE	P1_MODE

Port 2 SFRs

	HIGH BYTE	LOW BYTE
1FCEH	P2_PIN	(Reserved)
1FCCH	P2_REG	(Reserved)
1FCAH	P2_DIR	(Reserved)
1FC8H	P2_MODE	(Reserved)

Serial I/O and Synchronous SIO SFRs

	HIGH BYTE	LOW BYTE
1FBEH	(Reserved)	(Reserved)
1FBCH	SP_BAUD (Hi)	SP_BAUD (Lo)
1FBAH	SP_CON	SBUF_TX
1FB8H	SP_STATUS	SBUF_RX
1FB6H	(Reserved)	(Reserved)
1FB4H	(Reserved)	SSIO_BAUD
1FB2H	SSIO0_CON	SSIO0_BUF
1FB0H	SSIO1_CON	SSIO1_BUF

A/D and EPA Interrupt SFRs

	HIGH BYTE	LOW BYTE
1FAEH	AD_TIME	AD_TEST
1FACH	AD_COMMAND (Hi)	AD_COMMAND (Lo)
1FAAH	AD_RESULT (Hi)	AD_RESULT (Lo)
1FA8H	(Reserved)	EPAIPV
1FA6H	(Reserved)	EPA_PEND1
1FA4H	(Reserved)	EPA_MASK1
1FA2H	EPA_PEND (Hi)	EPA_PEND (Lo)
1FA0H	EPA_MASK (Hi)	EPA_MASK (Lo)

Timer 1 and Timer 2 SFRs

	HIGH BYTE	LOW BYTE
1F9EH	TIMER2 (Hi)	TIMER2 (Lo)
1F9CH	(Reserved)	T2CONTROL
1F9AH	TIMER1 (Hi)	TIMER1 (Lo)
1F98H	(Reserved)	T1CONTROL

EPA SFRs

	HIGH BYTE	LOW BYTE
1F8EH	COMP1_TIME (Hi)	COMP1_TIME (Lo)
1F8CH	(Reserved)	COMP1_CON
1F8AH	COMP0_TIME (Hi)	COMP0_TIME (Lo)
1F88H	(Reserved)	COMP0_CON
1F86H	EPA9_TIME (Hi)	EPA9_TIME (Lo)
1F84H	(Reserved)	EPA9_CON
1F82H	EPA8_TIME (Hi)	EPA8_TIME (Lo)
1F80H	(Reserved)	EPA8_CON
1F7EH	EPA7_TIME (Hi)	EPA7_TIME (Lo)
1F7CH	(Reserved)	EPA7_CON
1F7AH	EPA6_TIME (Hi)	EPA6_TIME (Lo)
1F78H	(Reserved)	EPA6_CON
1F76H	EPA5_TIME (Hi)	EPA5_TIME (Lo)
1F74H	(Reserved)	EPA5_CON
1F72H	EPA4_TIME (Hi)	EPA4_TIME (Lo)
1F70H	(Reserved)	EPA4_CON
1F6EH	EPA3_TIME (Hi)	EPA3_TIME (Lo)
1F6CH	EPA3_CON (Hi)	EPA3_CON (Lo)
1F6AH	EPA2_TIME (Hi)	EPA2_TIME (Lo)
1F68H	(Reserved)	EPA2_CON
1F66H	EPA1_TIME (Hi)	EPA1_TIME (Lo)
1F64H	EPA1_CON (Hi)	EPA1_CON (Lo)
1F62H	EPA0_TIME (Hi)	EPA0_TIME (Lo)
1F60H	(Reserved)	EPA0_CON

3.0 SFR BIT SUMMARY

EPAx_CONTROL

8	7	6	5	4	3	2	1	0
RM	TB	CE	M1	M0	RE	AD	ROT	ON/RT

RM: "1" Enables Remapping (EPA1 & EPA3 Only)
TB: "0" Selects Timer1, "1" Selects Timer2
CE: "0" Disables Comparator, "1" Enables Comparator
M1, M0: Mode Bits

M1, M0	Capture:	Compare:
00	No Op	Interrupt Only
01	Capture Negative	Output "0"
10	Capture Positive	Output "1"
11	Capture All Edges	Toggle Output

RE: Reenable Entry = "1" (Lock Entry)
AD: Start A/D
ROT: Reset Opposite Time Base
ON/RT: Overrun and Reset Timer Enable

EPAIPV 1FA8H: Byte

7	6	5	4	3	2	1	0
0	0	0	PV4	PV3	PV2	PV1	PV0

PV4–PV0: Returns the encoded highest priority interrupt. Value from 1H–14H.

0H = No Interrupt Pending	0AH = OVRINT4
14H = EPAINT4	09H = OVRINT5
13H = EPAINT5	08H = OVRINT6
12H = EPAINT6	07H = OVRINT7
11H = EPAINT7	06H = OVRINT8
10H = EPAINT8	05H = OVRINT9
0FH = EPAINT9	04H = Compare Channel 0
0EH = OVRINT0	03H = Compare Channel 1
0DH = OVRINT1	02H = TIMER1 Overflow
0CH = OVRINT2	01H = TIMER2 Overflow
0BH = OVRINT3	

SP_CON 1FBBH: Byte

7	6	5	4	3	2	1	0
X	X	X	TB8	REN	PEN	M2	M1

TB8: 9th Bit for Transmission
REN: Enables the Receiver
PEN: Enables Parity (Even)
M2, M1:
00: Mode 0/Sync
01: Mode 1/Async (std)
10: Mode 2/Async (9th Bit Enable)
11: Mode 3/Async (9th Bit Data)

SP_BAUD 1FBCH: Word

Mode 0:

$$\frac{XTAL1}{Baud * 2} - 1$$

or

$$\frac{T1CLK}{Baud}$$

Mode 1, 2, 3:

$$\frac{XTAL}{Baud * 16} - 1$$

or

$$\frac{T1CLK}{Baud * 8}$$

PORT 1/2/5/6 Control

Px_MODE = "1" for Peripheral Control
Px_MODE = "0" for Standard Port
Px_DIR = "1" for INPUT or OPEN DRAIN OUTPUT
Px_DIR = "0" for OUTPUT (PUSH/PULL)
Px_PIN is for PORT READs
Px_REG is for PORT WRITEs

TxCONTROL 1F98H: Byte = T1, 1F9CH: Byte = T2

7	6	5	4	3	2	1	0
CE	UD	M2	M1	M0	P2	P1	P0

CE: "0" Disables Timer, "1" Enables Timer
UD: "0" Counts Down, "1" Counts Up

M2, M1, M0—Mode Bits

000	Clock = Internal/Direction = UD
x01	Clock = External/Direction = UD
010	Clock = Internal/Direction = TxDIR
011	Clock = External/Direction = TxDIR
100	Clock = T1 Overflow/Direction = UD
110	Clock = T1 Overflow/Direction = T1
111	Quadrature Count (TxCLK/TxDIR)

P2, P1, P0—Prescale Bits

000	÷ 1 (250 ns @ 16 MHz) Xtal•4
001	÷ 2 (500 ns @ 16 MHz) Xtal•8
010	÷ 4 (1 μs @ 16 MHz) Xtal•16
011	÷ 8 (2 μs @ 16 MHz) Xtal•32
100	÷ 16 (4 μs @ 16 MHz) Xtal•64
101	÷ 32 (8 μs @ 16 MHz) Xtal•128
110	÷ 64 (16 μs @ 16 MHz) Xtal•256
111	Reserved

INT_MASK/INT_MASK1 08H/13H: Byte
INT_PEND/INT_PEND1 09H/12H: Byte
PTS_SRV 06: Word
PTS_SELECT 04H: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rsv	EXT INT	rsv	RI	TI	SSI01	SSIO0	CBF	IBF	OBE	A/D Done	INT EPA0	INT EPA1	INT EPA2	INT EPA3	INT EPAX

AD_TEST 1FAEH: Byte

7	6	5	4	3	2	1	0
0	0	0	0	OF1	OF0	V_{REF}	A_{GND}

A_{GND}: Convert on AnGND
V_{REF}: Convert on V_{REF}
OF1, OF0: Offset Adjust
00: No Adjustment
01: ADD 2.5 mV
10: SUB 2.5 mV
11: SUB 5.0 mV

SP_STATUS 1FB9H: Byte

7	6	5	4	3	2	1	0
RB8/RPE	RI	TI	FE	TXE	OE	X	X

RP8: Set if 9th Bit set (No Parity)
RPE: Set if Parity Enabled and Parity Error
RI: Set after Last Data Bit Received
TI: Set at Beginning of STOP Bit
FE: Set if No STOP Bit Found
TXE: Set when Byte is in SBUF_TX
OE: Set if Overrun Error Occurred

AD_TIME 1FAFH: Byte

7	6	5	4	3	2	1	0
Sample Time				Conversion Time (CONV)			

SAM = 1 to 7 CONV = 2 to 31

Total Conversion Time:
T = (4 * SAM) + (B*(CONV + 1) + 2.5)
Where B = 8 for 8-Bit, 10 for 10-Bit

AD_COMMAND 1FACH: Byte/Word

7	6	5	4	3	2	1	0
0	0	T	M	GO	Channel #		

Channel # = 0 to 7
GO: "1" to Start Now/"0" for EPA Start
M: "0" = 10-Bit/"1" = 8-Bit Conversion
"0" = Detect High/"1" = Detect Low
T: "0" = Normal Conversion/"1" = Threshold Detect

EPA_MASK1/EPA_PEND1 1FA4H/1FA6H: Byte
EPA_MASK/EPA_PEND 1FA0H/1FA2H: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT EPA4	INT EPA5	INT EPA6	INT EPA7	INT EPA8	INT EPA9	OVR EPA0	OVR EPA1	OVR EPA2	OVR EPA3	OVR EPA4	OVR EPA5	OVR EPA6	OVR EPA7	OVR EPA8	OVR EPA9

7	6	5	4	3	2	1	0
rsv	rsv	rsv	rsv	COMP CH0	COMP CH1	OVR TIMR1	OVR TIMR2

CCB (FF2018H: Byte)

0	PD	=	"1" Enables Powerdown
1	BW0	=	See Table
2	WR	=	"1" = $\overline{WR}$/BHE "0" = $\overline{WRL}$/$\overline{WRH}$
3	ALE	=	"1" = ALE – "0" = $\overline{ADV}$
4	IRC0	=	} See Table
5	IRC1	=	
6	LOC0	=	} See Table
7	LOC1	=	

CCB1 (FF201AH: Byte)

0	LDCCB2	=	1—Fetch CCB2 0—Do Not Fetch CCB2
1	IRC2	=	See Table
2	BW1	=	See Table
3	WDE	=	"0" = Always Enabled
4	1	=	} Reserved must
5	0	=	} be "01"
6	MSEL0	=	} See Table
7	MSEL1	=	} See Table

CCB2 (FF201CH: Byte)

0	1	
1	MODE16	= "0" — 24-bit mode = "1" — 16-bit mode
2	REMAP	= "0" — EPROM @ FF2000H only = "1" — EPROM also mapped to 02000H.
3	1	
4	1	
5	1	
6	1	
7	1	

LOC1	LOC0	Function
0	0	Read and Write Protected
0	1	Write Protected Only
1	0	Read Protected Only
1	1	No Protection

IRC2	IRC1	IRC0	Max Wait States
0	0	0	Zero Wait States
1	0	0	1 Wait State
1	0	1	2 Wait States
1	1	0	3 Wait States
1	1	1	INFINITE

MSEL1	MSEL0	Bus Timing Mode
0	0	Mode 0 (1-Wait KR)
0	1	Mode 1 (Long R/W)
1	0	Mode 2 (Early Address)
1	1	Mode 3 (KR Compatible)

BW1	BW0	Bus Width
0	0	ILLEGAL
0	1	16-Bit Only
1	0	8-Bit Only
1	1	BW Pin Controlled

SLP_CON 1FFBH: Byte

7	6	5	4	3	2	1	0
0	0	0	0	SLP	SLPL	IBEmask	OBFmask

SLP = 1 Enables Slave Port Operation
= 0 Disables Slave Port Operation and Clears Bits, CBE, IBE, and OBF in SLP_STAT

SLPL = 1 ALE Latches SLP_ADDR from AD1 (P3.1)
= 0 ALE is SLP_ADDR

IBEmask = 1 IBE Can Affect SLPINT
= 0 IBE Cannot Affect SLPINT

OBFmask = 1 OBF Can Affect SLPINT
= 0 OBF Cannot Affect SLPINT

SLP_STAT 1FF8H: Byte

7	6	5	4	3	2	1	0
STAT					CBE	IBE	OBF

STAT These bits are written by the 8XC196NT/NQ user and defined by the 8XC196NT/NQ user for communication flags.

CBE (Command Buffer Empty)
= 1 After 8XC196NT/NQ Reads SLPCMD
= 0 After Master Writes to SLPCMD or SLP = 0 in SLP_CON

IBE (Input Buffer Empty)
= 1 After 8XC196NT/NQ Reads SLPDIN
= 0 After Master Writes to SLPDIN, or SLP = 0 in SLP_CON

OBF (Output Buffer Full)
= 1 After 8XC196NT/NQ Writes to SLPDOUT
= 0 After Master Reads SLPDOUT

USFR 1FF6H (Read Only): Byte

7	6	5	4	3	2	1	0
RSV	RSV	RSV	DEI	DED	RSV	RSV	RSV

NOTE:
Do not write to location 1FF6H. Bits DED and DEI are written as specified in users manual.

Device	DEI	DED
87C196NT/NQ	UPROM Bit	UPROM Bit

DED—Disable External Data
DEI—Disable External Instructions

SSIOx_CON Registers 1FB1H: Byte = SSIO0
1FB3H: Byte = SSIO1

7	6	5	4	3	2	1	0
M/$\overline{S}$	T/$\overline{R}$	TRT	THS	STE	ATR	OUF	TBS

M/$\overline{S}$ Master/$\overline{Slave}$
T/$\overline{R}$ Transmit $\overline{Receive}$
TRT Transmitter/Receiver Toggle
THS Transceiver Handshake Select
STE Single Transfer Enable
ATR Auto Transfer Re-Enable
OUF Overflow/Underflow Flag
TBS Transceiver/Buffer Status

AD_RESULT 1FAAH: Word

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8 MSB								2 LSB		RSV	RSV	BUSY	A/D Channel		

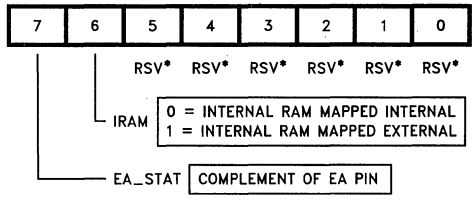
A/D Channel Channel Number: 0–7
BUSY 0 = A/D Idle
1 = A/D in Use
RSV Reserved
2 LSB 2 Least Significant Bits
8 MSB 8 Most Significant Bits
Bit 4, 5 0

WSR 14H: Byte

7	6	5	4	3	2	1	0
HLDEN	Window Select Bits						

HLDEN = 0 Disables HOLD/HLDA
= 1 Enables HOLD/HLDA

IRAM_CON (1FE0H: BYTE)



EA_STAT NOT EFFECTED BY WRITE
*RSV--RESERVED BIT MUST BE = 0

272270-2

4.0 PIN DEFINITION TABLE

68 PLCC	Function
44	ACH4
45	ACH5
46	ACH6
47	ACH7
30	AD0
29	AD1
28	AD2
27	AD3
26	AD4
25	AD5
24	AD6
23	AD7
22	AD8
21	AD9
20	AD10
19	AD11
18	AD12
17	AD13
16	AD14
15	AD15
14	AD16
13	AD17
12	AD18
11	AD19
04	$\overline{ADV}$
40	$\overline{AINC}$
04	ALE
48	ANGND
08	$\overline{BHE}$
39	$\overline{BREQ}$
10	BUSWIDTH
43	CLKOUT
42	CPVER
33	$\overline{EA}$
14	EP0

68 PLCC	Function
13	EP1
12	EP2
11	EP3
57	EPA0
56	EPA1
55	EPA2
54	EPA3
53	EPA4
52	EPA5
51	EPA6
50	EPA7
58	EPA8
59	EPA9
38	EXTINT
42	$\overline{HLDA}$
41	$\overline{HOLD}$
03	INST
40	$\overline{INTOUT}$
32	NMI
44	P0.4
45	P0.5
46	P0.6
47	P0.7
57	P1.0
56	P1.1
55	P1.2
54	P1.3
53	P1.4
52	P1.5
51	P1.6
50	P1.7
36	P2.0
37	P2.1
38	P2.2

68 PLCC	Function
39	P2.3
40	P2.4
41	P2.5
42	P2.6
43	P2.7
30	P3.0
29	P3.1
28	P3.2
27	P3.3
26	P3.4
25	P3.5
24	P3.6
23	P3.7
22	P4.0
21	P4.1
20	P4.2
19	P4.3
18	P4.4
17	P4.5
16	P4.6
15	P4.7
04	P5.0
03	P5.1
09	P5.2
01	P5.4
08	P5.5
02	P5.6
10	P5.7
58	P6.0
59	P6.1
60	P6.2
61	P6.3
62	P6.4
63	P6.5

68 PLCC	Function
64	P6.6
65	P6.7
43	$\overline{PACT}$
37	$\overline{PALE}$
44	PMODE.0
45	PMODE.1
46	PMODE.2
47	PMODE.3
38	$\overline{PROG}$
36	PVER
07	$\overline{RD}$
02	READY
31	$\overline{RESET}$
37	RXD
62	SC0
64	SC1
63	SD0
65	SD1
01	SLPINT
60	T1CLK
61	T1DIR
57	T2CLK
55	T2DIR
36	TXD
35	V_{CC}
06	V_{PP}
49	V_{REF}
05	V_{SS}
34	V_{SS}
09	$\overline{WR}$
08	$\overline{WRH}$
09	$\overline{WRL}$
67	XTAL1
66	XTAL2

5.0 PACKAGE PIN ASSIGNMENTS

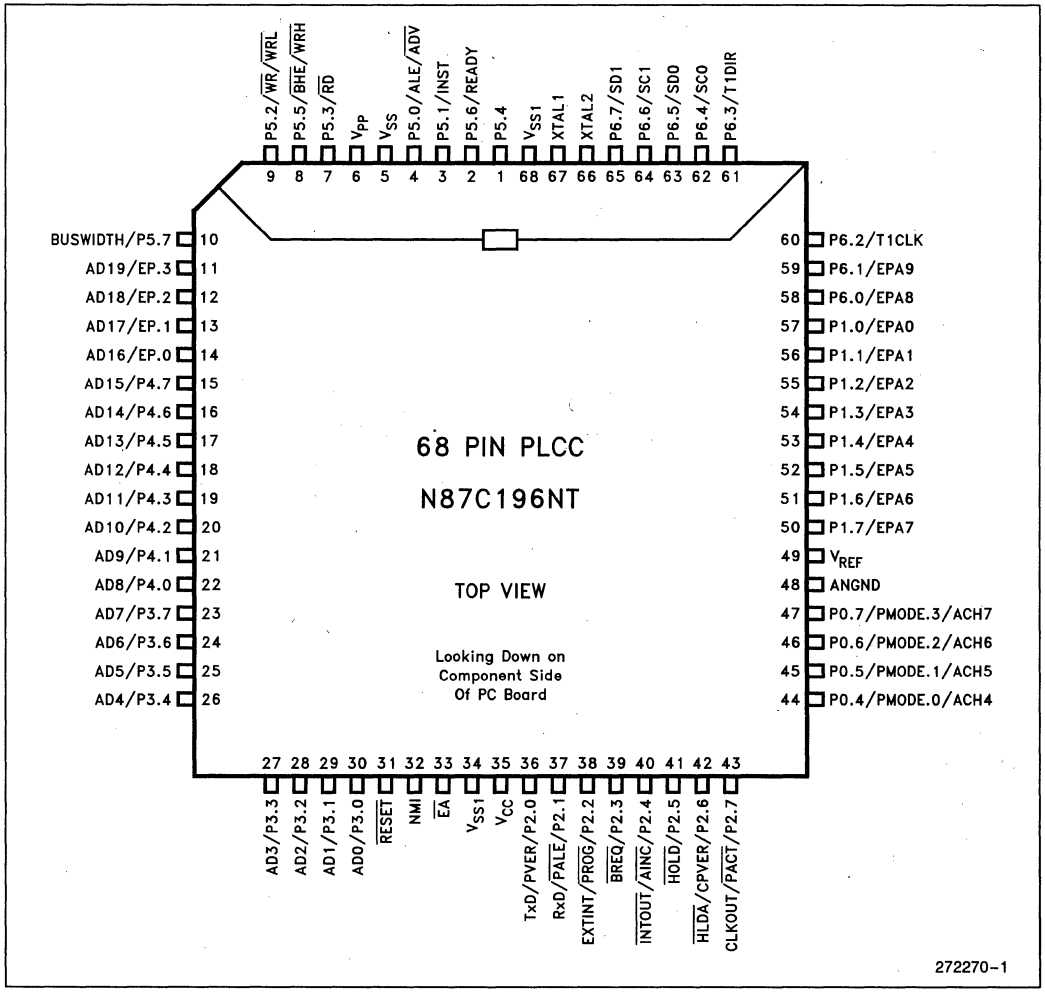


Figure 1. 68-Pin PLCC Package Diagram

6.0 PIN DESCRIPTION

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS1}, V_{SS2}, V_{SS3}	Digital circuit ground (0V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference and supply voltage for the A/D converter and Port0 (+5V). Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from power-down circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, connect V_{PP} to V_{CC}.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
ACH4–ACH7/PORT0	Analog inputs to the on-chip A/D converter. Also a digital input pin.*
ALE/$\overline{\text{ADV}}$/P5.0	Address Latch Enable or Address Valid output. Goes low to latch and demultiplex the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive (high) at the end of the bus cycle, providing a chip select for external memory. $\overline{\text{ADV}}$ is active only during external memory accesses. Also a standard I/O pin.*
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$/P5.5	Byte High Enable or Write High output. $\overline{\text{BHE}}$ = 0 when accessing odd (high) bytes or complete words in external memory. $\overline{\text{WRH}}$ = 0 when writing to odd bytes or complete words in external memory. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is only valid during 16-bit external memory cycles. Also a standard I/O pin.*
$\overline{\text{BREQ}}$/P2.3	Bus Request output. Active low when the bus controller is in hold and has a pending external memory cycle. Also a standard I/O pin.*
BUSWIDTH/P5.7	Input for bus width selection. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. Also a standard I/O pin.*
CLOCKOUT/P2.7	Output of the internal clock generator. A 50% duty cycle signal at 1/2 XTAL1 frequency. Also a standard I/O pin.*
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ = 1 directs memory accesses from locations 0F2000H through 0F9FFFH to on-chip EPROM/ROM. $\overline{\text{EA}}$ = 0 directs all memory accesses to off-chip memory. $\overline{\text{EA}}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{\text{EA}}$ is latched at reset.
EPA0–7/P1.0–1.7 EPA8–9/P6.0–6.1	I/O pins for the Event Processor Array. EPA0 and EPA2 also function as T2CLK and T2DIR. Also a standard I/O pin.*
EPORT	4-bit bidirectional standard I/O port. These pins are shared with the extended address bus, A16–A19. Pin function is selected on a per pin basis.
EXTINT/P2.2	External Interrupt input pin. A positive transition sets the EXTINT interrupt pending flag. The minimum high and low times are 2 oscillator cycles. Also a standard I/O pin.*
INST/P5.1	Instruction fetch signal. Output high during the entire bus cycle of an external instruction fetch. INST is active only during external memory fetches; during internal memory fetches, INST is low. Also a standard I/O pin.*
$\overline{\text{INTOUT}}$/P2.4	Interrupt output indicating that a pending interrupt requires use of the external bus. Also a standard I/O pin.*
$\overline{\text{HLDA}}$/P2.6	Bus Hold Acknowledge output indicating release of the bus in response to a HOLD request. Also a standard I/O pin.* This is also a TEST MODE enable pin. Do not use it as an input without careful hardware evaluation.

*These pins may be used for the system or peripheral functions or as a standard I/O pin.

6.0 PIN DESCRIPTION (Continued)

Symbol	Name and Function
HOLD/P2.5	Bus Hold request input. HOLD is sent by another processor to request control of 8XC196NT/NQ system bus. Also a standard I/O pin.*
NMI	Non-Maskable interrupt input pin. A positive transition causes a non-maskable interrupt vector through memory location FF203EH. If not used, this pin should be tied to V_{SS}. May be used by Intel Evaluation boards.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port 0 pins should not be left floating. In EPROM devices these pins are also used to select the Programming Mode.
PORT1	8-bit bidirectional standard I/O port. All of its pins are shared with the EPA.
PORT2	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (TxD, RxD, EXTINT, BREQ, INTOUT, HOLD, HLDA, CLKOUT).
PORT3 PORT4	8-bit bidirectional standard I/O with open drain outputs. These pins are shared with the multiplexed address/data bus which uses complementary drivers.
PORT5	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (ALE/ADV, INST, WR/WRL, RD, SLPINT, BHE/WRH, READY, BUSWIDTH).
PORT6	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (EPA8, EPA9, T1CLK, T1DIR, SC0, SD0, SC1, SD1).
RD/P5.3	Read signal output to external memory. RD is low only during external memory reads. Also a standard I/O pin.*
READY/P5.6	Ready input to lengthen external memory cycles. If READY = 1, CPU operation continues in a normal manner. If READY = 0 wait states are added. Also a standard I/O pin.*
RESET	Reset input to the chip. Held low for at least 16 state times to reset the chip. The subsequent low to high transition starts the reset sequence. Input high for normal operation. RESET has an internal pullup.
RXD/P2.1	Receive data input pin for the Serial I/O (SIO) port. Also a standard I/O pin.*
SLPINT/P5.4	Slave Port Interrupt output pin. Also a standard I/O pin.*
SSIO/P6.4–P6.7 (SC0, SD0, SC1, SD1)	Synchronous Serial I/O pins. SC0/SC1 are clock pins and SD0/SD1 are data pins. Also a standard I/O pin.*
T1CLK/P6.2	TIMER1 Clock input. TIMER1 increments or decrements on both rising and falling edges. Also a standard I/O pin.*
T1DIR/P6.3	TIMER1 Direction input. TIMER1 increments when this pin is high and decrements when this pin is low. Also a standard I/O pin.*
T2CLK/P1.0	TIMER2 Clock Input. TIMER2 increments or decrements on both rising and falling edges. Also a standard I/O pin.*
T2DIR/P1.2	TIMER2 Direction input. TIMER2 increments when this pin is high and decrements when this pin is low. Also a standard I/O pin.*
TXD/P2.0	Transmit data output pin for the Serial I/O (SIO) port. Also a standard I/O pin.*
WR/WRL/P5.2	Write and Write Low output to external memory. WR goes low for every external write. WRL goes low only for writes to even addresses. WR/WRL is active only during external memory writes. Also a standard I/O pin.*
XTAL1	Input of the oscillator invertor and the internal clock generator. If using an external clock source connect it to this pin.
XTAL2	Output of the oscillator invertor. Leave floating unless connected to a crystal/ resonator circuit.

*These pins may be used for the system or peripheral functions or as a standard I/O pin.

6.0 PIN DESCRIPTION (Continued)

Programming Mode Pin Definitions

Name	Name and Function
PMODE P0.4–7	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by an 8XC196NT/NQ that is in Slave Programming Mode. Used to indicate that Port 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge latches data on PBUS and begins programming. Rising edge inputs ends programming.
PACT	Programming Active. Used to indicate when programming activity is complete.
PVER	Programming Verification. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low input enables the auto increment mode. Auto increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
PORTS 3 and 4	Address/Command/Data Bus. Used to pass commands, addresses and data to and from 8XC196NT/NQs. Also used in the Auto Programming Mode as a regular system bus to access external memory.
CPVER	Cumulative Program Verification. Pin is high if all locations since entering a programming mode have programmed correctly.

7.0 OPCODE TABLE

00	SKIP
01	CLR
02	NOT
03	NEG
04	XCH
05	DEC
06	EXT
07	INC
08	SHR
09	SHL
0A	SHRA
0B	XCH
0C	SHRL
0D	SHLL
0E	SHRAL
0F	NORML
10	RESERVED
11	CLRB
12	NOTB
13	NEGB
14	XCHB
15	DECB
16	EXTB
17	INCB
18	SHRB
19	SHLB
1A	SHRAB
1B	XCHB
1C	EST INDIRECT
1D	EST INDEXED
1E	ESTB INDIRECT
1F	ESTB INDEXED
20	SJMP
21	SJMP
22	SJMP
23	SJMP
24	SJMP
25	SJMP
26	SJMP
27	SJMP
28	SCALL
29	SCALL
2A	SCALL
2B	SCALL
2C	SCALL
2D	SCALL
2E	SCALL

2F	SCALL
30	JBC
31	JBC
32	JBC
33	JBC
34	JBC
35	JBC
36	JBC
37	JBC
38	JBS
39	JBS
3A	JBS
3B	JBS
3C	JBS
3D	JBS
3E	JBS
3F	JBS
40	AND DIRECT (3 OPS)
41	AND IMMEDIATE (3 OPS)
42	AND INDIRECT (3 OPS)
43	AND INDEXED (3 OPS)
44	ADD DIRECT (3 OPS)
45	ADD IMMEDIATE (3 OPS)
46	ADD INDIRECT (3 OPS)
47	ADD INDEXED (3 OPS)
48	SUB DIRECT (3 OPS)
49	SUB IMMEDIATE (3 OPS)
4A	SUB INDIRECT (3 OPS)
4B	SUB INDEXED (3 OPS)
4C	MULU DIRECT (3 OPS)
4D	MULU IMMEDIATE (3 OPS)
4E	MULU INDIRECT (3 OPS)
4F	MULU INDEXED (3 OPS)
50	ANDB DIRECT (3 OPS)
51	ANDB IMMEDIATE (3 OPS)
52	ANDB INDIRECT (3 OPS)
53	ANDB INDEXED (3 OPS)
54	ADDB DIRECT (3 OPS)
55	ADDB IMMEDIATE (3 OPS)
56	ADDB INDIRECT (3 OPS)
57	ADDB INDEXED (3 OPS)
58	SUBB DIRECT (3 OPS)
59	SUBB IMMEDIATE (3 OPS)
5A	SUBB INDIRECT (3 OPS)
5B	SUBB INDEXED (3 OPS)
5C	MULUB DIRECT (3 OPS)
5D	MULUB IMMEDIATE (3 OPS)

5E	MULUB INDIRECT (3 OPS)
5F	MULUB INDEXED (3 OPS)
60	AND DIRECT (2 OPS)
61	AND IMMEDIATE (2 OPS)
62	AND INDIRECT (2 OPS)
63	AND INDEXED (2 OPS)
64	ADD DIRECT (2 OPS)
65	ADD IMMEDIATE (2 OPS)
66	ADD INDIRECT (2 OPS)
67	ADD INDEXED (2 OPS)
68	SUB DIRECT (2 OPS)
69	SUB IMMEDIATE (2 OPS)
6A	SUB INDIRECT (2 OPS)
6B	SUB INDEXED (2 OPS)
6C	MULU DIRECT (2 OPS)
6D	MULU IMMEDIATE (2 OPS)
6E	MULU INDIRECT (2 OPS)
6F	MULU INDEXED (2 OPS)
70	ANDB DIRECT (2 OPS)
71	ANDB IMMEDIATE (2 OPS)
72	ANDB INDIRECT (2 OPS)
73	ANDB INDEXED (2 OPS)
74	ADDB DIRECT (2 OPS)
75	ADDB IMMEDIATE (2 OPS)
76	ADDB INDIRECT (2 OPS)
77	ADDB INDEXED (2 OPS)
78	SUBB DIRECT (2 OPS)
79	SUBB IMMEDIATE (2 OPS)
7A	SUBB INDIRECT (2 OPS)
7B	SUBB INDEXED (2 OPS)
7C	MULUB DIRECT (2 OPS)
7D	MULUB IMMEDIATE (2 OPS)
7E	MULUB INDIRECT (2 OPS)
7F	MULUB INDEXED (2 OPS)
80	OR DIRECT
81	OR IMMEDIATE
82	OR INDIRECT
83	OR INDEXED
84	XOR DIRECT
85	XOR IMMEDIATE
86	XOR INDIRECT
87	XOR INDEXED
88	CMP DIRECT
89	CMP IMMEDIATE
8A	CMP INDIRECT
8B	CMP INDEXED
8C	DIVU DIRECT

7.0 OPCODE TABLE (Continued)

8D	DIVU IMMEDIATE
8E	DIVU INDIRECT
8F	DIVU INDEXED
90	ORB DIRECT
91	ORB IMMEDIATE
92	ORB INDIRECT
93	ORB INDEXED
94	XORB DIRECT
95	XORB IMMEDIATE
96	XORB INDIRECT
97	XORB INDEXED
98	CMPB DIRECT
99	CMPB IMMEDIATE
9A	CMPB INDIRECT
9B	CMPB INDEXED
9C	DIVUB DIRECT
9D	DIVUB IMMEDIATE
9E	DIVUB INDIRECT
9F	DIVUB INDEXED
A0	LD DIRECT
A1	LD IMMEDIATE
A2	LD INDIRECT
A3	LD INDEXED
A4	ADDC DIRECT
A5	ADDC IMMEDIATE
A6	ADDC INDIRECT
A7	ADDC INDEXED
A8	SUBC DIRECT
A9	SUBC IMMEDIATE
AA	SUBC INDIRECT
AB	SUBC INDEXED
AC	LDBZE DIRECT
AD	LDBZE IMMEDIATE
AE	LDBZE INDIRECT
AF	LDBZE INDEXED
B0	LDB DIRECT
B1	LDB IMMEDIATE
B2	LDB INDIRECT
B3	LDB INDEXED

B4	ADDCB DIRECT
B5	ADDCB IMMEDIATE
B6	ADDCB INDIRECT
B7	ADDCB INDEXED
B8	SUBCB DIRECT
B9	SUBCB IMMEDIATE
BA	SUBCB INDIRECT
BB	SUBCB INDEXED
BC	LDBSE DIRECT
BD	LDBSE IMMEDIATE
BE	LDBSE INDIRECT
BF	LDBSE INDEXED
C0	ST DIRECT
C1	BMOV
C2	ST INDIRECT
C3	ST INDEXED
C4	STB DIRECT
C5	CMPL
C6	STB INDIRECT
C7	STB INDEXED
C8	PUSH DIRECT
C9	PUSH IMMEDIATE
CA	PUSH INDIRECT
CB	PUSH INDEXED
CC	POP DIRECT
CD	BMOVI
CE	POP INDIRECT
CF	POP INDEXED
D0	JNST
D1	JNH
D2	JGT
D3	JNC
D4	JNVT
D5	JNV
D6	JGE
D7	JNE
D8	JST
D9	JH

DA	JLE
DB	JC
DC	JVT
DD	JV
DE	JLT
DF	JE
E0	DJNZ
E1	DJNZW
E2	TIJMP
E3	**EBR (INDIRECT)
E4	EBMOVI
E5	RESERVED
E6	EJMP
E7	LJMP
E8	ELD INDIRECT
E9	ELD INDEXED
EA	ELDB INDIRECT
EB	ELDB INDEXED
EC	DPTS
ED	EPTS
EE	RESERVED
EF	LCALL
F0	RET
F1	ECALL
F2	PUSHF
F3	POPF
F4	PUSHA
F5	POPA
F6	IDPLD
F7	TRAP
F8	CLRC
F9	SETC
FA	DI
FB	EI
FC	CLRVT
FD	NOP
FE	*DIV/DIVB/MUL/MULB
FF	RST

*Two Byte Instruction - This opcode is placed as the first byte of an instruction to make it a signed operation instead of unsigned.

8.0 INSTRUCTION SET SUMMARY

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D = D + A	↕	↕	↕	↕	↑		
ADD/ADDB	3	D = B + A	↕	↕	↕	↕	↑		
ADDC/ADDCB	2	D = D + A + C	↓	↕	↕	↕	↑		
SUB/SUBB	2	D = D − A	↕	↕	↕	↕	↑		
SUB/SUBB	3	D = B − A	↕	↕	↕	↕	↑		
SUBC/SUBCB	2	D = D − A + C − 1	↓	↕	↕	↕	↑		
CMP/CMPB/CMPL	2	D − A	↕	↕	↕	↕	↑		
MUL/MULU	2	D,D + 2 = D × A							3
MUL/MULU	3	D,D + 2 = B × A							3
MULB/MULUB	2	D,D + 1 = D × A							4
MULB/MULUB	3	D,D + 1 = B × A							4
DIVU	2	D = (D,D + 2)/A,D + 2 = Remainder				↕	↑		3
DIVUB	2	D = (D,D + 1)/A,D + 1 = Remainder				↕	↑		4
DIV	2	D = (D,D + 2)/A,D + 2 = Remainder				↕	↑		
DIVB	2	D = (D,D + 1)/A,D + 1 = Remainder				↕	↑		
AND/ANDB	2	D = D and A	↕	↕	0	0			
AND/ANDB	3	D = B and A	↕	↕	0	0			
OR/ORB	2	D = D or A	↕	↕	0	0			
XOR/XORB	2	D = D (exclusive or) A	↕	↕	0	0			
LD/LDB	2	D = A							
ELD/ELDB	2	D = A							
ST/STB	2	A = D							
EST/ESTB	2	A = D							
XCH	2	D ⟷ A; D + 1 ⟷ A + 1							
XCHB	2	D ⟷ A							
BMOV, BMOVI/EBMOVI	2	(PTR_HI) + = (PTR_LOW) +; Until COUNT = 0							
LDBSE	2	D = A; D + 1 = Sign (A)							4, 5
LDBZE	2	D = A; D + 1 = 0							4, 5
PUSH	1	SP = SP − 2; (SP) = A							
POP	1	A = (SP); SP = SP + 2							
PUSHF	0	SP = SP − 2; (SP) = PSW; PSW = 0; I = 0; PSE = 0	0	0	0	0	0	0	11
POPF	0	PSW = (SP); SP = SP + 2; I ← ↕	↕	↕	↕	↕	↕	↕	11
PUSHA	0	SP = SP − 2; (SP) = PSW; PSW = 0000H; SP = SP − 2; (SP) = IMASK1/WSR; IMASK1 = 00H; I = 0; PSE = 0	0	0	0	0	0	0	
POPA	0	IMASK1/WSR = (SP); SP = SP + 2; PSW = (SP); SP = SP + 2	↕	↕	↕	↕	↕	↕	

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
SJMP	1	PC = PC + 11-Bit-Offset							6
LJMP	1	PC = PC + 16-Bit-Offset							6
EJMP	1	PC = PC + 24-Bit Offset							6, 12
EBR[Indirect]	1	PC = (A)							12
TIJMP	3	PC = ([index] and MASK)2 + (Table)							
TRAP	0	SP = SP − 2; (SP) = PC; PC = FF2010H							10
ECALL	1	SP = SP − 4; (SP) = PC PC = PC + 24-Bit Offset							6, 12
LCALL (16-Bit Mode)	1	SP = SP − 2; (SP) = PC PC = PC + 16-Bit Offset							6
LCALL (24-Bit Mode)	1	SP = SP − 4; (SP) = PC PC = PC + 16-Bit Offset							6, 13
SCALL (16-Bit Mode	1	SP = SP − 2; (SP) = PC PC = PC + 11-Bit Offset							6
SCALL (24-Bit Mode)	1	SP = SP − 4; (SP) = PC PC = PC + 11-Bit Offset							6, 13
RET (16-Bit Mode)	0	PC = (SP); SP = SP + 2							
RET (24-Bit Mode)	0	PC = (SP); SP = SP + 4							13
J(conditioned)	1	PC = PC + 8-Bit-Offset (If Taken)							6
JC	1	Jump if C = 1							6
JNC	1	Jump if C = 0							6
JE	1	Jump if Z = 1							6
JNE	1	Jump if Z = 0							6
JGE	1	Jump if N = 0							6
JLT	1	Jump if N = 1							6
JGT	1	Jump if N = 0 and Z = 0							6
JLE	1	Jump if N = 1 or Z = 1							6
JH	1	Jump if C = 1 and Z = 0							6
JNH	1	Jump if C = 0 or Z = 1							6
JV	1	Jump if V = 0							6
JNV	1	Jump if V = 1							6
JVT	1	Jump if VT = 1; Clear VT					0		6
JNVT	1	Jump if VT = 0; Clear VT					0		6
JST	1	Jump if ST = 1							6
JNST	1	Jump if ST = 0							6
JBS	3	Jump if Specific Bit = 1							6, 7
JBC	3	Jump if Specific Bit = 0							6, 7
DJNZ/DJNZW	1	D = D − 1; If D ≠ 0 then PC = PC + 8-Bit-Offset							6

8.0 INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Operands	Operation(1)	Flags(2)						Notes
			Z	N	C	V	VT	ST	
DEC/DECB	1	D = D − 1	✓	✓	✓	✓	↑		
NEG/NEGB	1	D = 0 − D	✓	✓	✓	✓	↑		
INC/INCB	1	D = D + 1	✓	✓	✓	✓	↑		
EXT	1	D = D;D + 2 = Sign (D)	✓	✓	0	0			3
EXTB	1	D = D;D + 1 = Sign (D)	✓	✓	0	0			4
NOT/NOTB	1	D = Logical Not (D)	✓	✓	0	0			
CLR/CLRB	1	D = 0	1	0	0	0			
SHL/SHLB/SHLL	2	C ← msb•••lsb ← 0	✓	✓	✓	✓	↑		8
SHR/SHRB/SHRL	2	0 → msb•••lsb → C	✓	✓	✓	0		✓	8
SHRA/SHRAB/SHRAL	2	msb → msb•••lsb → C	✓	✓	✓	0		✓	8
NORML	2	Left Shift until msb = 1;D = Shift Count	✓	✓	0				8
SETC	0	C = 1			1				
CLRC	0	C = 0			0				
CLRVT	0	VT = 0					0		
RST	0	PC = 2080H	0	0	0	0	0	0	9
DI	0	Disable All Interrupts (I = 0)							
EI	0	Enable All Interupts (I = 1)							
DPTS	0	Disable PTS Interrupts (PSE = 0)							
EPTS	0	Enable PTS Interrupts (PSE = 1)							
NOP	0	PC = PC + 1							
SKIP	0	PC = PC + 2							
IPLPD	1	Idle Mode IF Key = 1; Powerdown Mode IF Key = 2 Chip RESET Otherwise							

NOTES:
1. If the mnemonic ends in "B" a byte operation is performed, otherwise a word operation is performed. Operands D, B and A must conform to the alignment rules for the required operand type. D and B are locations in the Lower Register File; A can be located anywhere in memory.
2. The symbols indicate the effects on the flags:
   - ✓ Cleared or set as appropriate
   - 0 Cleared
   - 1 Set
   - ↑ Set if appropriate; never cleared
   - ↓ Cleared if appropriate; never set
3. D, D + 2 are consecutive WORDs in memory; D is DOUBLE-WORD aligned.
4. D, D + 1 are consecutive BYTEs in memory; D is WORD aligned.
5. Changes a BYTE to WORD.
6. Offset is a 2's complement number.
7. Specific Bit must be in or windowed into the Lower Register File.
8. The "L" (LONG) suffix indicates DOUBLE-WORD operations.
9. Initiates a RESET by pulling RESET low. Software should re-initialize all the neccessary registers with code starting at FF2080H.
10. The assembler does not accept this mnemonic (use the macro file for definition).
11. I = Interrupt Enable (PSW1).
12. These instructions will only function in 24-bit mode.
13. These instructions push/pop 2 additional bytes on/off stack in 24-bit mode.

9.0 INSTRUCTION LENGTH/OPCODES

Mnemonic	Direct	Immed	Indirect		Indexed	
			Normal(1)	A-Inc(1)	Short(1)	Long(1)
ADD (3-op)	4/44	5/45	4/46	4/46	5/47	6/47
SUB (3-op)	4/48	5/49	4/4A	4/4A	5/4B	6/4B
ADD (2-op)	3/64	4/65	3/66	3/66	4/67	5/67
SUB (2-op)	3/68	4/69	3/6A	3/6A	4/6B	5/6B
ADDC	3/A4	4/A5	3/A6	3/A6	4/A7	5/A7
SUBC	3/A8	4/A9	3/AA	3/AA	4/AB	5/AB
CMP	3/88	4/89	3/8A	3/8A	4/8B	5/8B
ADDB (3-op)	4/54	4/55	4/56	4/56	5/57	6/57
SUBB (3-op)	4/58	4/59	4/5A	4/5A	5/5B	6/5B
ADDB (2-op)	3/74	3/75	3/76	3/76	4/77	5/77
SUBB (2-op)	3/78	3/79	3/7A	3/7A	4/7B	5/7B
ADDCB	3/B4	3/B5	3/B6	3/B6	4/B7	5/B7
SUBCB	3/B8	3/B9	3/BA	3/BA	4/BB	5/BB
CMPB	3/98	3/99	3/9A	3/9A	4/9B	5/9B
MUL (3-op)	5/(2)	6/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULU (3-op)	4/4C	5/4D	4/4E	4/4E	5/4F	6/4F
MUL (2-op)	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULU (2-op)	3/6C	4/6D	3/6E	3/6E	4/6F	5/6F
DIV	4/(2)	5/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVU	3/8C	4/8D	3/8E	3/8E	4/8F	5/8F
MULB (3-op)	5/(2)	5/(2)	5/(2)	5/(2)	6/(2)	7/(2)
MULUB (3-op)	4/5C	4/5D	4/5E	4/5E	5/5F	6/5F
MULB (2-op)	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
MULUB (2-op)	3/7C	3/7D	3/7E	3/7E	4/7F	5/7F
DIVB	4/(2)	4/(2)	4/(2)	4/(2)	5/(2)	6/(2)
DIVUB	3/9C	3/9D	3/9E	3/9E	4/9F	5/9F
AND (3-op)	4/40	5/41	4/42	4/42	5/43	6/43
AND (2-op)	3/60	4/61	3/62	3/62	4/63	5/63
OR (2-op)	3/80	4/81	3/82	3/82	4/83	5/83
XOR	3/84	4/85	3/86	3/86	4/87	5/87
ANDB (3-op)	4/50	4/51	4/52	4/52	5/53	5/53
ANDB (2-op)	3/70	3/71	3/72	3/72	4/73	4/73
ORB (2-op)	3/90	3/91	3/92	3/92	4/93	5/93
XORB	3/94	3/95	3/96	3/96	4/97	5/97
PUSH	2/C8	3/C9	2/CA	2/CA	3/CB	4/CB
POP	2/CC		2/CE	2/CE	3/CF	4/CF
LD	3/A0	4/A1	3/A2	3/A2	4/A3	5/A3
LDB	3/B0	3/B1	3/B2	3/B2	4/B3	5/B3
ELD			3/E8	3/E8		6/E9
ELDB			3/EA	3/EA		6/EB
ST	3/C0		3/C2	3/C2	4/C3	5/C3
STB	3/C4		3/C6	3/C6	4/C7	5/C7
EST			3/1C	3/1C		6/1D
ESTB			3/1E	3/1E		6/1F

9.0 INSTRUCTION LENGTH/OPCODES (Continued)

Mnemonic	Direct	Immed	Indirect		Indexed	
			Normal(1)	A-Inc(1)	Short(1)	Long(1)
XCH	3/04	—	—	—	4/0B	5/0B
XCHB	3/14	—	—	—	4/1B	5/1B
LDBSE	3/BC	3/BD	3/BE	3/BE	4/BF	5/BF
LBSZE	3/AC	3/AD	3/AE	3/AE	4/AF	5/AF

Mnemonic	Length/Opcode
PUSHF	1/F2
POPF	1/F3
PUSHA	1/F4
POPA	1/F5
TRAP	1/F7
LCALL	3/EF
SCALL	2/28–2F(3)
ECALL	4/F1
RET	1/F0
LJMP	3/E7
SJMP	2/20–27(3)
EJMP	4/E6
EBR[ ]	2/E3
TIJMP	4/E2
JNST	1/D0
JST	1/D8
JNH	1/D1
JH	1/D9
JGT	1/D2
JLE	1/DA
JNC	1/B3
JC	1/D8
JNVT	1/D4
JVT	1/DC
JNV	1/D5
JV	1/DD
JGE	1/D6
JLT	1/DE

Mnemonic	Length/Opcode
JNE	1/D7
JE	1/DF
JBC	3/30–37
JBS	3/38–3F
DJNZ	3/E0
DJNZW	3/E1
NORML	3/0F
SHRL	3/0C
SHLL	3/0D
SHRAL	3/0E
SHR	3/08
SHRB	3/18
SHL	3/09
SHLB	3/19
SHRA	3/0A
SHRAB	3/1A
CLRC	1/F8
SETC	1/F9
DI	1/FA
EI	1/FB
DPTS	1/EC
EPTS	1/ED
CLRVT	1/FC
NOP	1/FD
RST	1/FF
SKIP	2/00
IDLPD	1/F6
BMOV	3/C1
BMOVi	3/CD
EBMOVI	3/E4

NOTES:
1. Indirect and indirect + share the same opcodes, as do short and long indexed opcodes. If the second byte is even, use indirect or short indexed. If odd, use indirect or long indexed.
2. The opcodes for signed multiply and divide are the unsigned opcode with an "FE" prefix.
3. The 3 least significant bits of the opcode are concatenated with the 8 bits to form an 11-bit, 2's complement offset.

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES)

Instruction	Direct	Immediate	Indirect		Indexed		Extended
			Normal	A-Inc	Short	Long	
ADD (3op)	5	6	7/10	8/11	7/10	8/11	
SUB (3op)	5	6	7/10	8/11	7/10	8/11	
ADD (2op)	4	5	6/8	7/9	6/8	7/9	
SUB (2op)	4	5	6/8	7/9	6/8	7/9	
ADDC	4	5	6/8	7/9	6/8	7/9	
SUBC	4	5	6/8	7/9	6/8	7/9	
CMP	4	5	6/8	7/9	6/8	7/9	
ADDB (3op)	5	5	7/10	8/11	7/10	8/11	
SUBB (3op)	5	5	7/10	8/11	7/10	8/11	
ADDB (2op)	4	4	6/8	7/9	6/8	7/9	
SUBB (2op)	4	4	6/8	7/9	6/8	7/9	
ADDCB	4	4	6/8	7/9	6/8	7/9	
SUBCB	4	4	6/8	7/9	6/8	7/9	
CMPB	4	4	6/8	7/9	6/8	7/9	
CMPL	7						
MUL (3op)	16	17	18/21	19/22	19/22	20/23	
MULU (3op)	14	15	16/19	17/20	17/20	18/21	
MUL (2op)	16	17	18/21	19/22	19/22	20/23	
MULU (2op)	14	15	16/19	17/20	17/20	18/21	
DIV	26	27	28/31	29/32	29/32	30/33	
DIVU	24	25	26/29	27/30	27/30	28/31	
MULB (3op)	12	12	14/17	15/18	15/18	16/19	
MULUB (3op)	10	10	12/15	12/16	12/16	14/17	
MULB (2op)	12	12	14/17	15/18	15/18	16/19	
MULUB (2op)	10	10	12/15	12/16	12/16	14/17	
DIVB	18	18	20/23	21/24	21/24	22/25	
DIVUB	16	16	18/21	19/22	19/22	20/23	
AND (3op)	5	6	7/10	8/11	7/10	8/11	
AND (2op)	4	5	6/8	7/9	6/8	7/9	
OR	4	5	6/8	7/9	6/8	7/9	
XOR	4	5	6/8	7/9	6/8	7/9	
ANDB (3op)	5	5	7/10	8/11	7/10	8/11	
ANDB (2op)	4	4	6/8	7/9	6/8	7/9	
ORB	4	4	6/8	7/9	6/8	7/9	
XORB	4	4	6/8	7/9	6/8	7/9	
LD	4	5	5/8	6/8	6/9	7/10	

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed		Extended
			Normal	A-Inc	Short	Long	
ST	4		5/8	6/9	6/9	7/10	
LDB	4	4	5/8	6/8	6/9	7/10	
STB	4		5/8	6/9	6/9	7/10	
ELD			6/9	8/11			8/11
EST			6/9	8/11			8/11
ELDB			6/9	8/11			8/11
ESTB			6/9	8/11			8/11
XCH	5				8/13	9/14	
STB	4				8/13	9/14	
XCHB	5				8/13	9/14	
BMOV	6 + 8 per Word		6 + 11/14 per Word				
BMOVI	7 + 8 per Word +14 for Each Interrupt		7 + 11/14 per Word +14 for Each Interrupt				
EBMOVI			8 + 14/20 per Word +16 for Each Interrupt				
LDBSE, LDBZE	4	4	5/7	6/8	6/8	7/9	
PUSH (int)	6	7	9/12	10/13	10/13	11/14	
POP (int)	8		10/12	11/13	11/13	12/14	
PUSHF (int)	6						
POPF (int)	7						
PUSHA (int)	12						
POPA (int)	12						
PUSH (ext)	8	9	11/14	12/15	12/15	13/16	
POP (ext)	11		13/15	14/16	14/16	15/17	
PUSHF (ext)	8						
POPF (ext)	10						
PUSHA (ext)	18						
POPA (ext)	18						
EJMP (24-Bit Mode)	8						
LJMP	7						
SJMP	7						
EBR[Indirect](24-Bit Mode)	9						
BR[Indirect]	7						
TIJMP (Internal Table)	15						
TIJMP (External Table)	18						
TRAP (24-Bit Mode, Int)	19						
TRAP (16-Bit Mode, Int)	16						

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed		Extended
			Normal	A-Inc	Short	Long	
ECALL (24-Bit Mode, Int)	16						
LCALL (16-Bit Mode, Int)	11						
LCALL (24-Bit Mode, Int)	15						
SCALL (16-Bit Mode, Int	11						
SCALL (24-Bit Mode, Int)	15						
RET (24-Bit Mode, Int)	16						
RET (16-Bit Mode, Int)	11						
TRAP (24-Bit Mode, Ext)	25						
TRAP (16-Bit Mode, Ext)	18						
ECALL (24-Bit Mode, Ext)	22						
LCALL (16-Bit Mode, Ext)	13						
LCALL (24-Bit Mode, Ext)	18						
SCALL (16-Bit Mode, Ext)	13						
SCALL (24-Bit Mode, Ext)	18						
RET (24-Bit Mode, Ext)	22						
RET (16-Bit Mode, Ext)	14						
JNST, JST	4/8 Jump Not Taken/Jump Taken						
JNH, JH	4/8 Jump Not Taken/Jump Taken						
JGT, JLE	4/8 Jump Not Taken/Jump Taken						
JNC, JC	4/8 Jump Not Taken/Jump Taken						
JNVT, JVT	4/8 Jump Not Taken/Jump Taken						
JNV, JV	4/8 Jump Not Taken/Jump Taken						
JGE, JLT	4/8 Jump Not Taken/Jump Taken						
JNE, JE	4/8 Jump Not Taken/Jump Taken						
JBS, JBC	5/9 Jump Not Taken/Jump Taken						
DJNZ	5/9 Jump Not Taken/Jump Taken						
DJNZW	6/10 Jump Not Taken/Jump Taken						
CLR, NOT, NEG	3						
DEC, INC	3						
EXT	4						
CLRB, NOTB	3						
DECB, INCB	3						
NEGB	3						
EXTB	4						
NORML	8 + 1 per Shift (9 for 0 Shift)						
SHRL	7 + 1 per Shift (8 for 0 Shift)						
SHLL	7 + 1 per Shift (8 for 0 Shift)						

10.0 INSTRUCTION EXECUTION TIMES (IN STATE TIMES) (Continued)

Instruction	Direct	Immediate	Indirect		Indexed		Extended
			Normal	A-Inc	Short	Long	
SHRAL	7 + 1 per Shift (8 for 0 Shift)						
SHR	6 + 1 per Shift (7 for 0 Shift)						
SHL	6 + 1 per Shift (7 for 0 Shift)						
SHRA	6 + 1 per Shift (7 for 0 Shift)						
SHRB	6 + 1 per Shift (7 for 0 Shift)						
SHLB	6 + 1 per Shift (7 for 0 Shift)						
SHRAB	6 + 1 per Shift (7 for 0 Shift)						
CLRC	2						
SETC	2						
DI	2						
EI	2						
DPTS	2						
EPTS	2						
CLRVT	2						
NOP	2						
RST	20 (Includes Fetch of CCB0/CCB1)						
SKIP	3						
IDLPD	8/25 (Proper Key/Improper Key)						
PTS							
Single Transfer	18	(+3 for Ext Reference, + 1 If XFER Count = 0)					
Burst Transfer	13	(+7 for Each Transfer, 1 Minimum +3 for Each Memory Controller Reference)					
PWM Modes	15						
A/D Scan Mode	21/25						

NOTES:
The timing figures are minimum execution times expressed as state times (one period of CLKOUT = two oscillator periods) and are based on the following assumptions:
1. The opcode, along with any required operands, have been pre-fetched and reside in the instruction queue.
2. The bus controller operates with the 16-bit bus selected and without wait states for external memory references and pre-fetches. For instructions with indirect or indexed addressing, execution times separated by a slash are for instructions requiring a fetch from internal/external memory.
3. Times for jumps, calls and returns include the 4 state times required to flush the pre-fetch queue and to fetch the opcode at the destination address. This is reflected in the jump taken/not-taken times shown in the table.

11.0 INTERRUPT TABLE

Name	Source	Vector	Priority
INT15	NMI	FF203EH	32 (Highest)
PTS14	EXTINT Pin	FF205CH	31
PTS13	Reserved	FF205AH	30
PTS12	Receive SIO	FF2058H	29
PTS11	Transmit SIO	FF2056H	28
PTS10	SSIO Channel 1 Transfer	FF2054H	27
PTS09	SSIO Channel 0 Transfer	FF2052H	26
PTS08	Command Buffer Full (SLP)	FF2050H	25
PTS07	Input Buffer Full (SLP)	FF204EH	24
PTS06	Output Buffer Empty (SLP)	FF204CH	23
PTS05	A/D Conversion Complete	FF204AH	22
PTS04	EPA0	FF2048H	21
PTS03	EPA1	FF2046H	20
PTS02	EPA2	FF2044H	19
PTS01	EPA3	FF2042H	18
PTS00	EPA4–9, Overrun (EPA0–9), Compare0–1, Timer Overflow	FF2040H	17
INT14	EXTINT Pin	FF203CH	16
INT13	Reserved	FF203AH	15
INT12	Receive SIO	FF2038H	14
INT11	Transmit SIO	FF2036H	13
INT10	SSIO Channel 1 Transfer	FF2034H	12
INT09	SSIO Channel 0 Transfer	FF2032H	11
INT08	Command Buffer Full (SLP)	FF2030H	10
N/A	UNIMPLEMENTED OPCODE	FF2012H	09
N/A	TRAP	FF2010H	08
INT07	Input Buffer Full (SLP)	FF200EH	07
INT06	Output Buffer Empty (SLP)	FF200CH	06
INT05	A/D Conversion Complete	FF200AH	05
INT04	EPA0	FF2008H	04
INT03	EPA1	FF2006H	03
INT02	EPA2	FF2004H	02
INT01	EPA3	FF2002H	01
INT00	EPA4–9, Overrun (EPA0–9), Compare0–1, Timer Overflow	FF2000H	00 (Lowest)

12.0 FORMULAS

State Time = 2 Oscillator Periods

TIJMP Calculation—

Destination = ([INDEX] AND INDEX_MASK) × 2 + [TBASE]

EPA Prescaler—

P2	P1	P0	
0	0	0	÷ 1
0	0	1	÷ 2
0	1	0	÷ 4
0	1	1	÷ 8
1	0	0	÷ 16
1	0	1	÷ 32
1	1	0	÷ 64
1	1	1	Reserved

SIO Baud Rate—

Modes 1, 2 and 3

$$SP\_BAUD = \frac{XTAL1\ Frequency}{Baud\ Rate \times 16} - 1 \qquad (B \geq 0, SP\_BAUD.15 = 1)$$

$$SP\_BAUD = \frac{T1CLK\ Frequency}{Baud\ Rate \times 8} - 1 \qquad (B > 0, SP\_BAUD.15 = 0)$$

Mode 0

$$SP\_BAUD = \frac{XTAL1\ Frequency}{Baud\ Rate \times 2} - 1 \qquad (B > 0, SP\_BAUD.15 = 1)$$

$$SP\_BAUD = \frac{T1CLK\ Frequency}{Baud\ Rate} - 1 \qquad (B > 0, SP\_BAUD.15 = 0)$$

SSIO Baud Rate—

$$SSIO.0 - SSIO.6 = \frac{XTAL1\ Frequency}{Baud\ Rate \times 8} - 1$$

A/D—

Sample States = 4 × SAM + 1
(SAM = AD_TIME.5 − AD_TIME.7)

Conversion States = B × (CONV + 1) + 1.5
(CONV = AD_TIME.0 − AD_TIME.4)
(B = 8 for 8-Bit Conversion)
(B = 10 for 10-Bit Conversion)

Total Conversion Time = State Time × [(4 × SAM) + (B × (CONV + 1)) + 2.5]

Programming Pulse Width—

$$PPR = \frac{((PPW) \times (FOSC)) - 144}{144} + 32768$$

13.0 RESET STATUS

SFR	Reset Value
AD_RESULT	7F80H
AD_COMMAND	0C0H
AD_TEST	0C0H
AD_TIME	0FFH
SSIO0_BUF, SSIO1_BUF	00H
SSIO0_CON, SSIO1_CON	00H
SSIO_BAUD (Baud Rate Control (Read))	0XXXXXXXB
SSIO_BAUD (Baud Rate Down Count (Write))	00H
SBUF_RX, SBUF_TX	00H
SP_STAT	0BH
SP_CON	EOH
SP_BAUD	0000H
COMP0_CON, COMP1_CON	00H
COMP0_TIME, COMP1_TIME	0000H
EPA1_CON, EPA3_CON	0000H
EPAx_CON (x = 0, 2, 4–9)	00H
EPAx_TIME (x = 0–9)	0000H
TIMER1, TIMER2	0000H
T1CONTROL, T2CONTROL	00H
EPA_MASK, EPA_MASK1	00H
EPA_PEND, EPA_PEND1	00H
EPAIPV	00H
P0_PIN, P1_PIN, P3_PIN, P4_PIN, P6_PIN, EP_PIN	XXH
P1_MODE, P6_MODE	00H
P1_DIR, P5_DIR, P6_DIR	0FFH
P1_REG, P3_REG, P4_REG, P5_REG, P6_REG, EP_REG	0FFH
P2_PIN, P5_PIN	1XXXXXXXB
P2_MODE, P5_MODE	80H
P2_DIR, P2_REG	7FH
INT_MASK, INT_PEND	00H
INT_MASK1, INT_PEND1	00H
PTSSRV, PTSSEL	0000H
WSR	00H

Pin States, during Reset, Idle and Powerdown

Pin Name	Reset	Idle	PD
$\overline{\text{RESET}}$	wk1	wk1	wk1
ALE (P5.0)	wk1	(A)	(A)
INST (P5.1)	wk0	(A)	(A)
$\overline{\text{RD}}$ (P5.3), $\overline{\text{WR}}$ (P5.2), SPLINT (P5.4)	wk1	(I)	(I)
$\overline{\text{BHE}}$ (P5.5)	wk1	(B)	(B)
READY (P5.6), BUSW (P5.7)	wk1	(C)	(C)
$\overline{\text{EA}}$, NMI	HZ	HZ	HZ
EP, P3, P4/AD (EA = 0)	wk1	HZ	HZ
EP, P3, P4/AD (EA = 1)	wk1	ODIO	ODIO
ACH/PO	HZ	HZ	HZ
P1	wk1	(D)	(D)
CLKOUT (P2.7)	clk, LZ	(E)	(G)
P2.0–P2.6	wk1	(E)	(E)
P6.0–P6.7	wk1	(F)	(F)
V_{PP}	HZ	1, LZ	1, LZ
XTAL1	HZ	HZ	HZ
XTAL2	osc, LZ	osc, LZ	(H)

NOTES:
(A) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 1, then LZ 0. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 0, then HZ.
(B) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 1, then LZ 1. If P5_MODE.x = 1 and $\overline{\text{HLDA}}$ = 0, then HZ.
(C) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1, then HZ.
(D) If P1_MODE.x = 0, port is as programmed. If P1_MODE.x = 1, pin is as specified by P1_DIR and associated peripheral.
(E) If P2_MODE.x = 0, port is as programmed. If P2_MODE.x = 1, pin is as specified by P2_DIR and associated peripheral.
(F) If P6_MODE.x = 0, port is as programmed. If P6_MODE.x = 1, pin is as specified by P6_DIR and associated peripheral.
(G) If P2_MODE.7 = 0, port is as programmed. If P2_MODE.7 = 1, then LZ 0.
(H) If XTAL1 = 1, then LZ 0. IF XTAL1 = 0, then LZ 1.
(I) If P5_MODE.x = 0, port is as programmed. If P5_MODE.x = 1, then pin is as specified by P5_DIR and associated peripheral.
HZ = High impedance
LZ = Low Impedance
wk1 = Weakly pulled high
ODIO = Open drain input/output
osc = Oscillator
wk0 = Weakly pulled low

intel®

October 1991

MCS®-96 A/D Converter Quick Reference

14

Order Number: 272115-001

1.0 The MCS-96 A/D Converter

Analog inputs to the MCS-96 family are handled by the A/D converter system. As shown in Figure 1, the converter system has an 8 channel multiplexer, a sample and hold, and a 10-bit successive approximation A/D converter. Conversions can be performed on one of 8 channels, the inputs of which share pins with port 0.

There are various versions of the A/D converter, depending on the specific device type. The 8X9X family offers a 10-bit fixed conversion time. The 8XC196KB family offers a 10-bit conversion with either a fast or slow conversion time. The 8XC196KC family offers an 8- or 10-bit conversion with programmable sample and convert times. The 8XC196KR has all of the KC features, with the addition of offset correction and internal conversion of V_{ref} and ANGND. The 8XC196MC includes all of the KR features, and the multiplexer has been expanded to 13 analog input channels.

This chapter describes the basic operation and terminology of the A/D converter. The different devices control the A/D in different ways, but the principals of operation remain the same throughout.

1.1 A/D Conversion Process

The conversion process is initiated by an HSO or EPA command, or by writing a one to the GO Bit in the A/D Control Register. Either activity causes a start conversion signal to be sent to the A/D converter control logic.

Once the A/D unit receives a start conversion signal, there is a one state time delay before sampling (Sample Delay) while the successive approximation register is reset and the proper multiplexer channel is selected. After the sample delay, the multiplexer output is connected to the sample capacitor and remains connected for the sample time. After the "sample window" closes, the input to the sample capacitor is disconnected from the multiplexer so that changes on the input pin will not alter the stored charge while the conversion is in progress. The comparator is then auto-zeroed and the conversion begins. The sample delay and sample time uncertainties are each approximately ±50 ns, independent of clock speed.

To perform the actual analog-to-digital conversion the MCS-96 implements a successive approximation algorithm. The converter hardware consists of a 256-resistor ladder, a comparator, coupling capacitors and a 10-bit successive approximation register (SAR) with logic that guides the process. The resistor ladder provides 20 mV steps (V_{REF} = 5.12V), while capacitive coupling creates 5 mV steps within the 20 mV ladder voltages. Therefore, 1024 internal reference voltages are available for comparison against the analog input to generate a 10-bit conversion result.

A successive approximation conversion is performed by comparing a sequence of reference voltages, to the analog input, in a binary search for the reference voltage that most closely matches the input. The ½ full scale reference voltage is the first tested. This corresponds to a 10-bit result where the most significant bit is zero, and all other bits are ones (0111.1111.11b). If the analog input was less than the test voltage, bit 10 of the SAR is left a zero, and a new test voltage of ¼ full scale (0011.1111.11b) is tried. If this test voltage was lower than the analog input, bit 9 of the SAR is set and bit 8 is cleared for the next test (0101.1111.11b). This binary search continues until 10 tests have occurred, at which time the valid 10-bit conversion result resides in the SAR where it can be read by software.

1.2 A/D Interface Suggestions

The external interface circuitry to an analog input is highly dependent upon the application, and can impact converter characteristics. In the external circuit's design, important factors such as input pin leakage, sample capacitor size and multiplexer series resistance from the input pin to the sample capacitor must be considered.

These factors are idealized in Figure 1. The external input circuit must be able to charge a sample capacitor (C_S) through a series resistance (R_I) to an accurate voltage given a DC leakage (I_L). Typically C_S is around 2 pF, R_I is around 5 KΩ and I_L is specified as 3 μA. In determining the necessary source impedance R_S, the value of V_{BIAS} is not important.

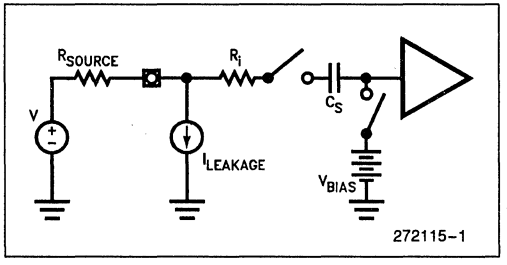


Figure 1. Idealized A/D Sampling Circuitry

External circuits with source impedances of 1 KΩ or less will be able to maintain an input voltage within a tolerance of about ±0.61 LSB (1.0 KΩ × 3.0 μA = 3.0 mV) given the DC leakage. Source impedances above 2 KΩ can result in an external error of at least one LSB due to the voltage drop caused by the 3 μA leakage. In addition, source impedances above 25 KΩ may degrade converter accuracy as a result of the internal sample capacitor not being fully charged during the sample window.

If large source impedances degrade converter accuracy because the sample capacitor is not charged during the sample time, an external capacitor connected to the pin compensates for this. Since the sample capacitor is 2 pF, a 0.005 μF capacitor (2048 * 2 pF) will charge the sample capacitor to an accurate input voltage of ±0.5 LSB. An external capacitor does not compensate for the voltage drop across the source resistance, but charges the sample capacitor fully during the sample time.

Placing an external capacitor on each analog input will also reduce the sensitivity to noise, as the capacitor combines with series resistance in the external circuit to form a low-pass filter. In practice, one should include a small series resistance prior to the external capacitor on the analog input pin and choose the largest capacitor value practical, given the frequency of the signal being converted. This provides a low-pass filter on the input, while the resistor will also limit input current during over-voltage conditions.

Figure 2 shows a simple analog interface circuit based upon the discussion above. The circuit in the figure also provides limited protection against over-voltage conditions on the analog input. Should the input voltage inappropriately drop significantly below ground, diode D2 will forward bias at about 0.8 DCV. Since the specification of the pin on most devices has an absolute maximum low voltage of −0.3V, this will leave about 0.5V across the 270Ω resistor, or about 2 mA of current. This should limit the current to a safe amount. Note that if any input pins are driven much beyond V_{REF} or below ANGND, the accuracy of all analog input channels may be adversely affected. This is because the input protection circuit will start to conduct, thus injecting current into the internal reference circuitry and upsetting the reference voltage. Refer to the data sheet for exact device specifications.

However, before any circuit is used in an actual application, it should be thoroughly analyzed for applicability to the specific problem at hand.

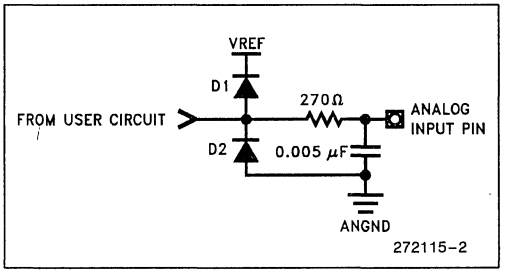


Figure 2. Suggested A/D Input Circuit

ANALOG REFERENCES

Reference supply levels and noise strongly influence the absolute accuracy of the conversion. For this reason, it is recommended that the ANGND pin be tied to the V_{SS} pins close to the device. Bypass capacitors should also be used between V_{REF} and ANGND. ANGND should be within about a tenth of a volt of V_{SS}. V_{REF} should be well regulated and used only for the A/D converter. The V_{REF} supply needs to be able to source around 5 mA.

Note that if only ratiometric information is desired, V_{REF} can be connected to V_{CC}. In addition, V_{REF} and ANGND must be connected even if the A/D converter is not being used. Remember that Port 0 receives its power from the V_{REF} and ANGND pins even when it is used as digital I/O.

1.3 The A/D Transfer Function

The conversion result is a 8- or 10-bit ratiometric representation of the input voltage, so the numerical value obtained from the conversion will be:

$$\text{INT}\,[255 \times (V_{IN} - \text{ANGND})/(V_{REF} - \text{ANGND})] \text{ or}$$

$$\text{INT}\,[1023 \times (V_{IN} - \text{ANGND})/(V_{REF} - \text{ANGND})]$$

This produces a stair-stepped transfer function when the output code is plotted versus input voltage (see Figure 3). The resulting digital codes can be taken as simple ratiometric information, or they provide information about absolute voltages or relative voltage changes on the inputs. The more demanding the application is on the A/D converter, the more important it is to fully understand the converter's operation. For simple applications, knowing the absolute error of the converter is sufficient. However, closing a servo-loop with analog inputs necessitates a detailed understanding of an A/D converter's operation and errors.

The errors inherent in an analog-to-digital conversion process are many: quantizing error, zero offset, full-scale error, differential non-linearity and non-linearity. These are "transfer function" errors related to the A/D converter. In addition, converter temperature drift, V_{CC} rejection, sample-hold feedthrough, multiplexer off-isolation, channel-to-channel matching and random noise should be considered. Fortunately, one "Absolute Error" specification is available which describes the sum total of all deviations between the actual conversion process and an ideal converter. However, the various sub-components of error are important in many applications. These error components are described in the text below where ideal and actual converters are compared.

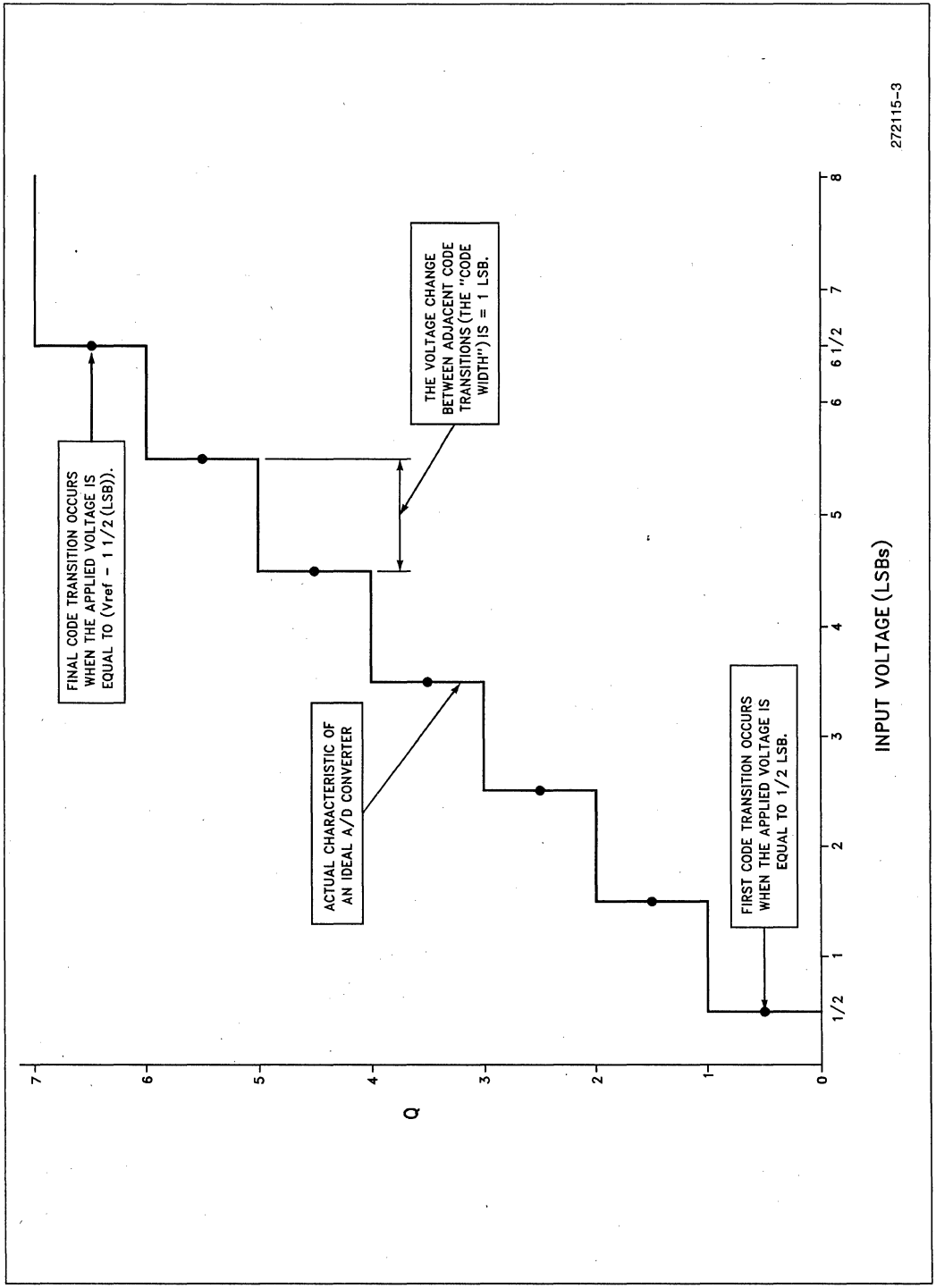


Figure 3. Ideal A/D Characteristic

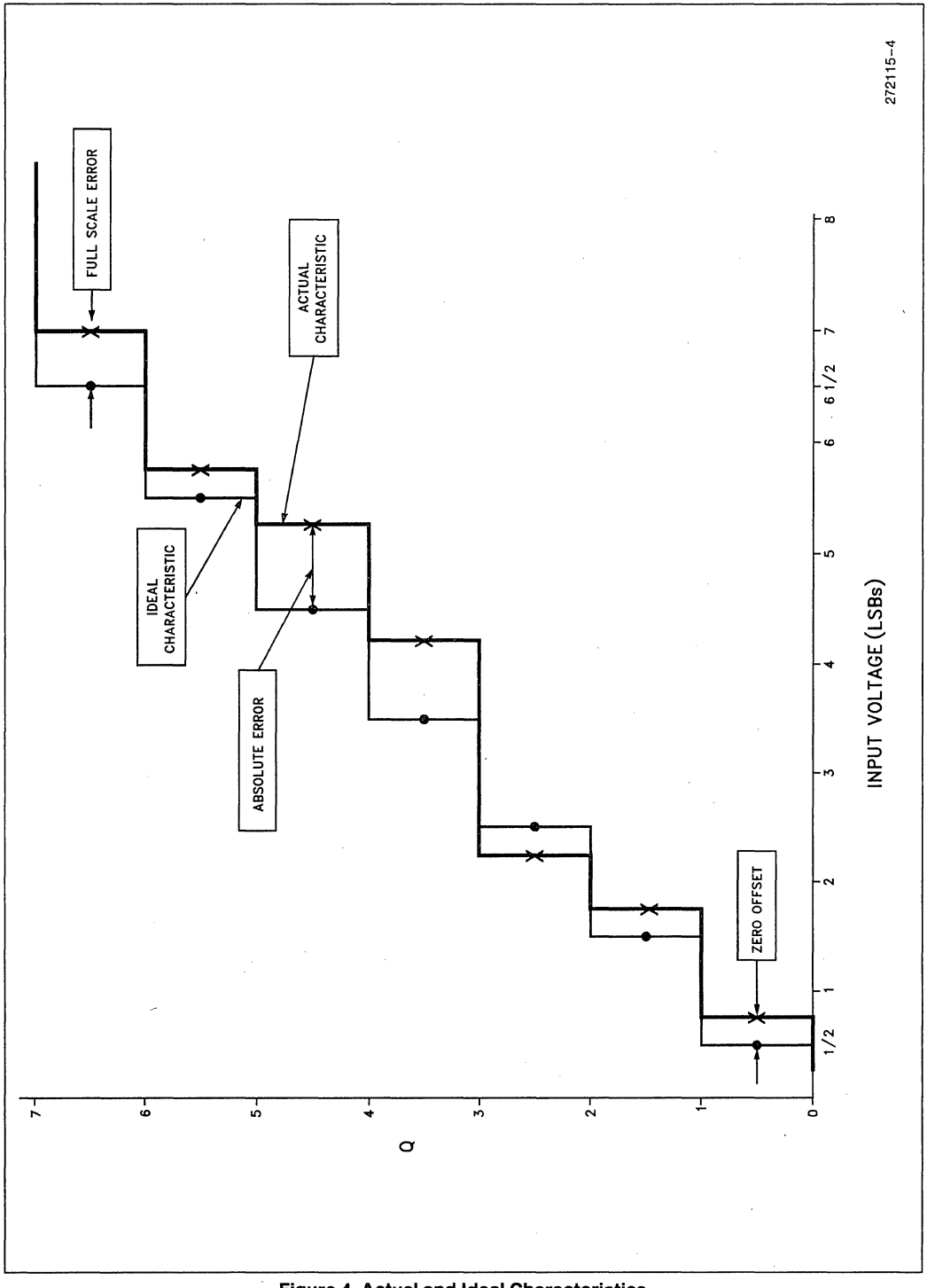


Figure 4. Actual and Ideal Characteristics

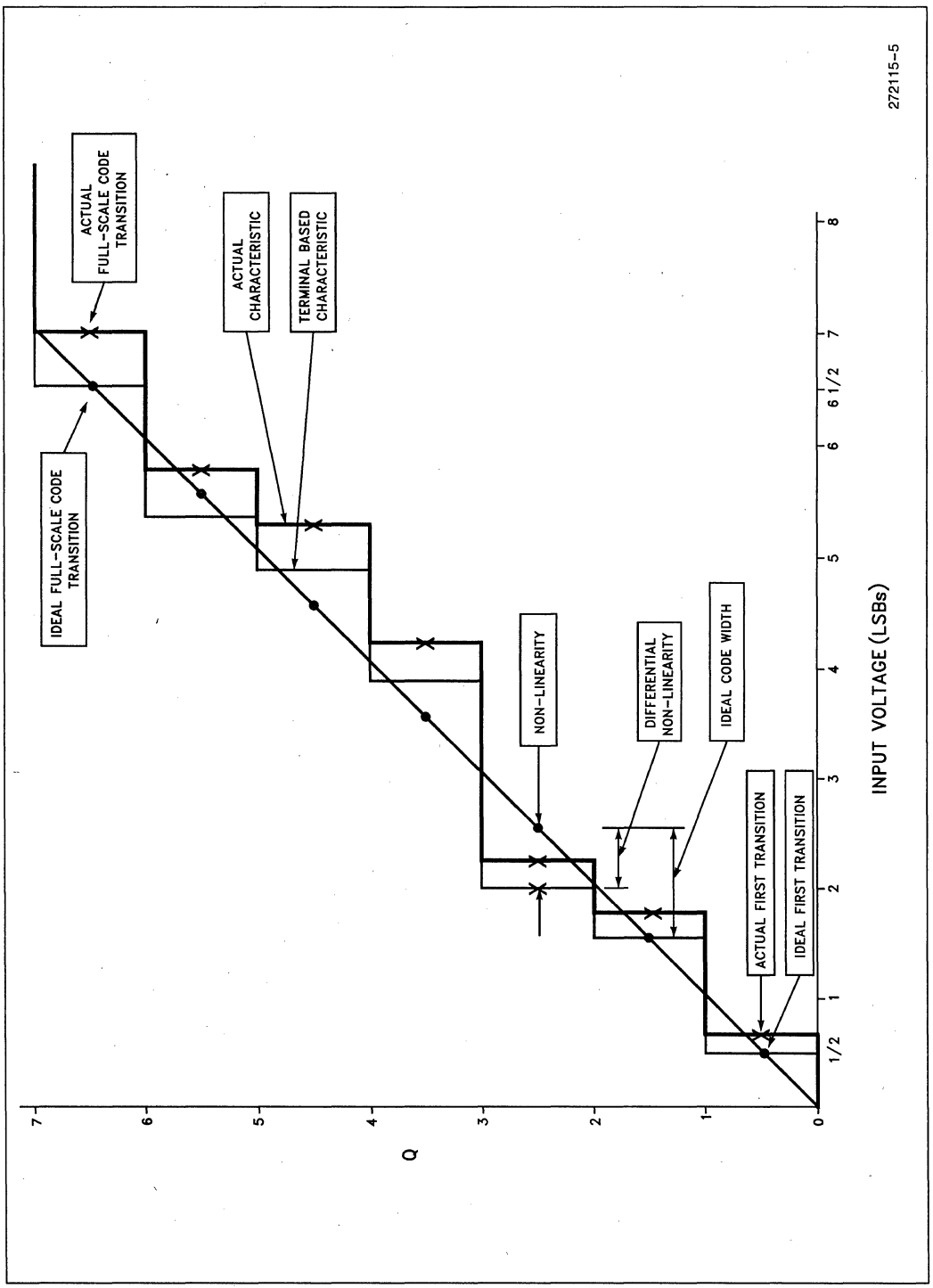


Figure 5. Terminal Based Characteristic

An unavoidable error simply results from the conversion of a continuous voltage to an integer digital representation. This error is called quantizing error, and is always ±0.5 LSB. Quantizing error is the only error seen in a perfect A/D converter, and is obviously present in actual converters. Figure 3 shows the transfer function for an ideal 3-bit A/D converter (i.e., the Ideal Characteristic).

Note that in Figure 3 the Ideal Characteristic possesses unique qualities: its first code transition occurs when the input voltage is 0.5 LSB; its full-scale code transition occurs when the input voltage equals the full-scale reference minus 1.5 LSB; and its code widths are all exactly one LSB. These qualities result in a digitization without offset, full-scale or linearity errors. In other words, a perfect conversion.

Figure 4 shows an Actual Characteristic of a hypothetical 3-bit converter, which is not perfect. When the Ideal Characteristic is overlaid with the imperfect characteristic, the actual converter is seen to exhibit errors in the location of the first and final code transitions and code widths. The deviation of the first code transition from ideal is called "zero offset", and the deviation of the final code transition from ideal is "full-scale error". The deviation of the code widths from ideal causes two types of errors. Differential Non-Linearity and Non-Linearity. Differential Non-Linearity is a local linearity error measurement, whereas Non-Linearity is an overall linearity error measure.

Differential Non-Linearity is the degree to which actual code widths differ from the ideal one LSB width. It gives the user a measure of how much the input voltage may have changed in order to produce a one count change in the conversion result. Non-Linearity is the worst case deviation of code transitions from the corresponding code transitions of the Ideal Characteristic. Non-Linearity describes how much Differential Non-Linearities could add up to produce an overall maximum departure from a linear characteristic. If the Differential Non-Linearity errors are too large, it is possible for an A/D converter to miss codes or exhibit non-monotonicity. Neither behavior is desirable in a closed-loop system. A converter has no missed codes if there exists for each output code a unique input voltage range that produces that code only. A converter is monotonic if every subsequent code change represents an input voltage change in the same direction.

Differential Non-Linearity and Non-Linearity are quantified by measuring the Terminal Based Linearity Errors. A Terminal Based Characteristic results when an Actual Characteristic is shifted and rotated to eliminate zero offset and full-scale error (see Figure 5). The Terminal Based Characteristic is similar to the Actual Characteristic that would be seen if zero offset and full-scale error were externally trimmed away. In practice, this is done by using input circuits which include gain and offset trimming. In addition, V_{REF} could also be closely regulated and trimmed within the specified range to affect full-scale error.

Other factors that affect a real A/D Converter system include sensitivity to temperature, failure to completely reject all unwanted signals, multiplexer channel dissimilarities and random noise. Fortunately these effects are small.

Temperature sensitivities are described by the rate at which typical specifications change with a change in temperature.

Undesired signals come from three main sources. First, noise on V_{CC}–V_{CC} Rejection. Second, input signal changes on the channel being converted after the sample window has closed–Feedthrough. Third, signals applied to channels not selected by the multiplexer–Off-Isolation.

Finally, multiplexer on-channel resistances differ slightly from one channel to the next causing Channel-to-Channel Matching errors, and random noise in general results in Repeatability errors.

1.4 A/D Glossary of Terms

Figures 3, 4 and 5 display many of these terms. Refer to AP-406 'MCS-96 Analog Acquisition Primer' for additional information on the A/D terms.

ABSOLUTE ERROR–The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

ACTUAL CHARACTERISTIC–The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An Actual Characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversion under the same conditions.

BREAK-BEFORE-MAKE–The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected. (e.g., the converter will not short inputs together.)

CHANNEL-TO-CHANNEL MATCHING–The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

CHARACTERISTIC–A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

CODE–The digital value output by the converter.

CODE CENTER–The voltage corresponding to the midpoint between two adjacent code transitions.

CODE TRANSITION–The point at which the converter changes from an output code of Q, to a code of Q+1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

CODE WIDTH–The voltage corresponding to the difference between two adjacent code transitions.

CROSSTALK–See "Off-Isolation".

DC INPUT LEAKAGE–Leakage current to ground from an analog input pin.

DIFFERENTIAL NON-LINEARITY–The difference between the ideal and actual code widths of the terminal based characteristic of a converter.

FEEDTHROUGH–Attenuation of a voltage applied on the selected channel of the A/D converter after the sample window closes.

FULL SCALE ERROR–The difference between the expected and actual input voltage corresponding to the full scale code transition.

IDEAL CHARACTERISTIC–A characteristic with its first code transition at V_{IN} = 0.5 LSB, its last code transition at V_{IN} = (V_{REF} − 1.5 LSB) and all code widths equal to one LSB.

INPUT RESISTANCE–The effective series resistance from the analog input pin to the sample capacitor.

LSB (LEAST SIGNIFICANT BIT)–The voltage value corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For a 10-bit converter with a reference voltage of 5.12 volts, one LSB is 5.0 mV. Note that this is different than digital LSBs, since an uncertainty of two LSBs, when referring to an A/D converter, equals 10 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 20 mV.)

MONOTONIC–The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

NO MISSED CODES–For each and every output code, there exists a unique input voltage range which produces that code only.

NON-LINEARITY–The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristics.

OFF-ISOLATION–Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

REPEATABILITY–The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

RESOLUTION–The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

SAMPLE DELAY–The delay from receiving the start conversion signal to when the sample window opens.

SAMPLE DELAY UNCERTAINTY–The variation in the Sample Delay.

SAMPLE TIME–The time that the sample window is open.

SAMPLE TIME UNCERTAINTY–The variation in the sample time.

SAMPLE WINDOW–Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

SUCCESSIVE APPROXIMATION–An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

TEMPERATURE COEFFICIENTS–Change in the stated variable per degree centigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effects of temperature drift.

TERMINAL BASED CHARACTERISTIC–An Actual Characteristic which has been rotated and translated to remove zero offset and full-scale error.

V_{CC} REJECTION–Ratio of the change in the A/D characteristic to the change in V_{CC}.

ZERO OFFSET–The difference between the expected and actual input voltage corresponding to the first code transition.

8X9X Data Sheets

15

809XBH/839XBH/879XBH
COMMERCIAL/EXPRESS HMOS MICROCONTROLLER

- **879XBH: an 809XBH with 8 Kbytes of On-Chip EPROM**
- **839XBH: an 809XBH with 8 Kbytes of On-Chip ROM**

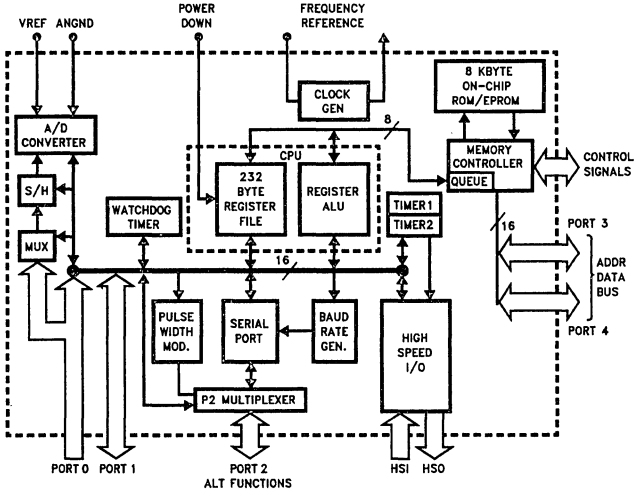
- **232 Byte Register File**
- **Register-to-Register Architecture**
- **10-Bit A/D Converter with S/H**
- **Five 8-Bit I/O Ports**
- **20 Interrupt Sources**
- **Pulse-Width Modulated Output**
- **ROM/EPROM Lock**
- **Run-Time Programmable EPROM**
- **Extended Temperature Available**
- **High Speed I/O Subsystem**
- **Full Duplex Serial Port**
- **Dedicated Baud Rate Generator**
- **6.25 μs 16 x 16 Multiply**
- **6.25 μs 32/16 Divide**
- **16-Bit Watchdog Timer**
- **Four 16-Bit Software Timers**
- **Two 16-Bit Counter/Timers**
- **Extended Burn-In Available**

The MCS®-96 family of 16-bit microcontrollers consists of many members, all of which are designed for high-speed control functions. The MCS-96 family members produced using Intel's HMOS-III process are described in this data sheet.

The CPU supports bit, byte, and word operations. Thirty-two bit double-words are supported for a subset of the instruction set. With a 12 MHz input frequency the 8096BH can do a 16-bit addition in 1.0 μs and a 16 x 16-bit multiply or 32/16 divide in 6.25 μs. Instruction execution times average 1 to 2 μs in typical applications.

Four high-speed trigger inputs are provided to record the times at which external events occur. Six high-speed pulse generator outputs are provided to trigger external events at preset times. The high-speed output unit can simultaneously perform software timer functions. Up to four 16-bit software timers can be in operation at once.

The on-chip A/D converter includes a Sample and Hold, and converts up to 8 multiplexed analog input channels to 10-bit digital values. With a 12 MHz crystal, each conversion takes 22 μs. This feature is only available on the 8X95BHs and 8X97BHs, with the 8X95BHs having 4 multiplexed analog inputs.



270090-50

Figure 1. 8X9XBH Block Diagram

July 1992
Order Number: 270090-010

Also provided on-chip are a serial port, a Watchdog Timer and a pulse-width modulated output signal.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

With the extended burn-in option, the burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.5V, following the guidelines in MIL-STD-883, Method 1015.

See the Packaging Information for extended temperature and extended burn-in designators.

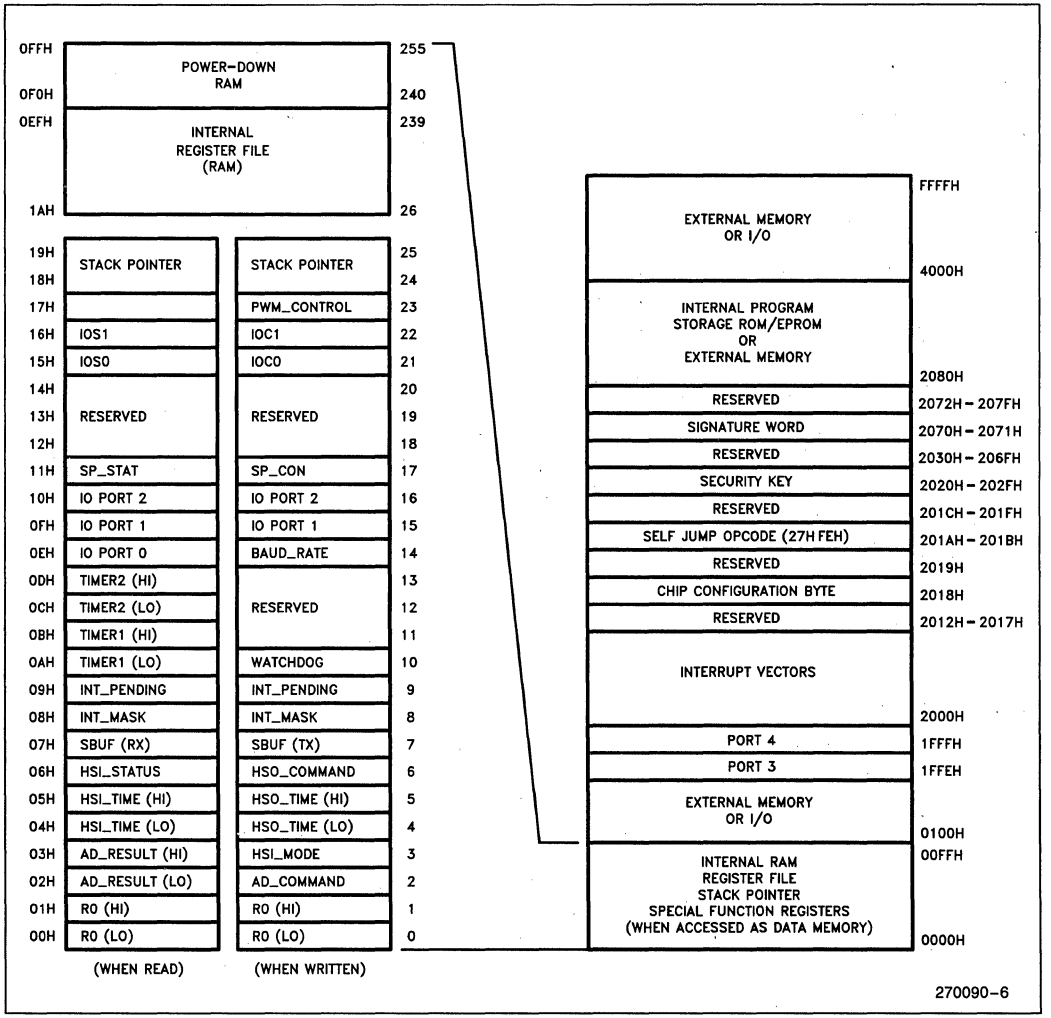


Figure 2. 8X9XBH Memory Map

PACKAGING

The 8096BH is available in 48-pin, 64-pin and 68-pin packages, with and without A/D, and with and without on-chip ROM or EPROM. The 8096BH numbering system is shown in Figure 3. Figures 5–10 show the pinouts for the 48-, 64- and 68-pin packages. The 48-pin version is offered in a Dual-In-Line package while the 68-pin versions come in a Plastic Leaded Chip Carrier (PLCC), a Pin Grid Array (PGA) or a Type "B" Leadless Chip Carrier.

	Factory Masked ROM			CPU			User Programmable					
							EPROM			OTP		
	68-Pin	64-Pin	48-Pin	68-Pin	64-Pin	48-Pin	68-Pin	64-Pin	48-Pin	68-Pin	64-Pin	48-Pin
ANALOG	8397BH	8397BH	8395BH	8097BH	8097BH	8095BH	8797BH		8795BH	8797BH	8797BH	
NO ANALOG	8396BH			8096BH								

Figure 3. 8X9X Packaging

Package Designators:
N = PLCC
C = Ceramic DIP
A = Ceramic Pin Grid Array
P = Plastic DIP
R = Ceramic LCC
U = Shrink DIP

Prefix Designators:
T = Extended Temperature
L = Extended Temperature with 160 Hours Burn-in

Package Type	θ_{ja}	θ_{jc}
68L PGA	35°C/W	10°C/W
68L PLCC	37°C/W	13°C/W
68L LCC	28°C/W	14°C/W
64L Shrink DIP	56°C/W	—
48L Plastic DIP	38°C/W	19°C/W
48L Ceramic DIP	26°C/W	6.5°C/W

Figure 4. 8X9XBH Thermal Characteristics

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

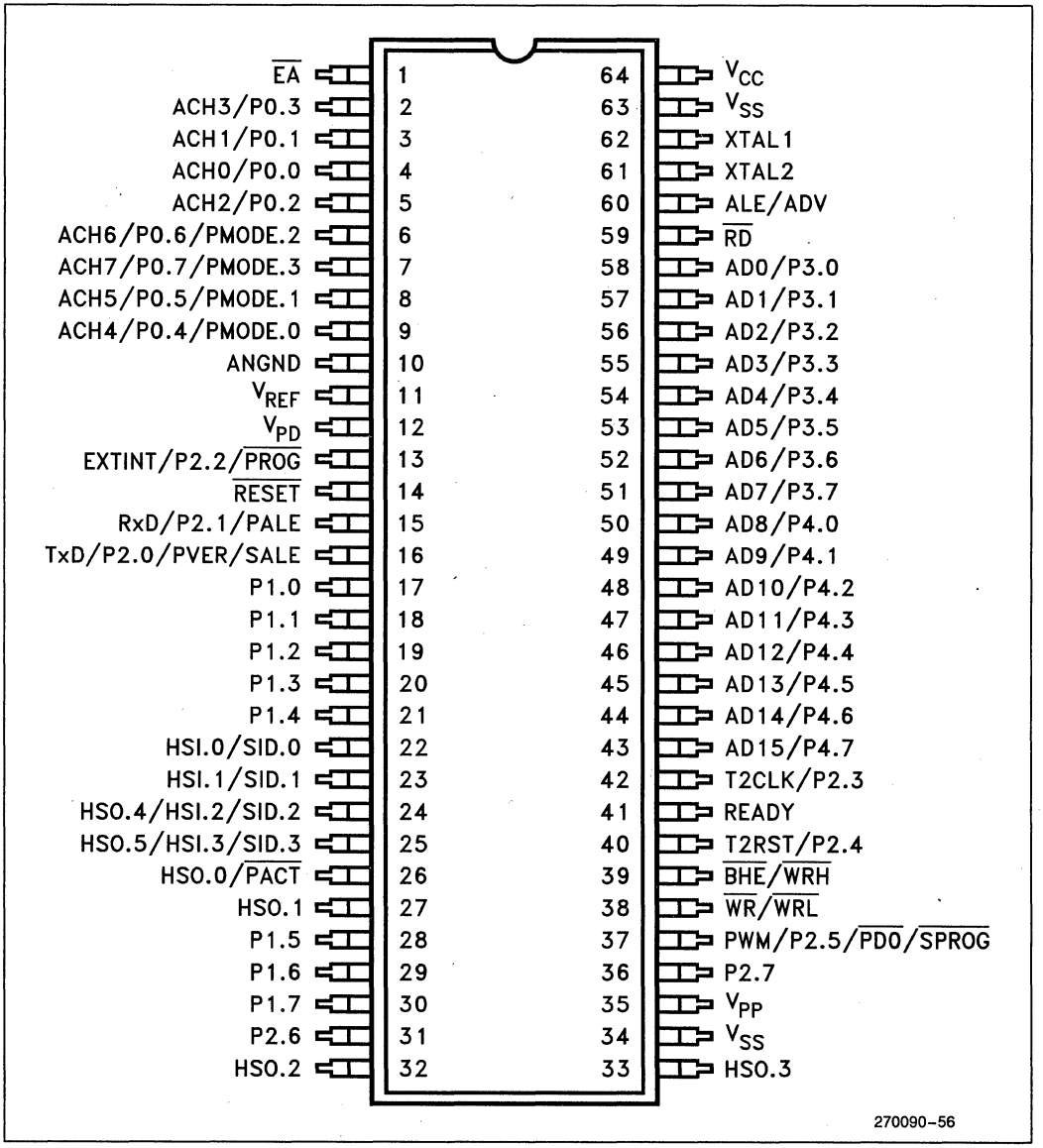


Figure 5. 64-Pin Shrink-DIP Package

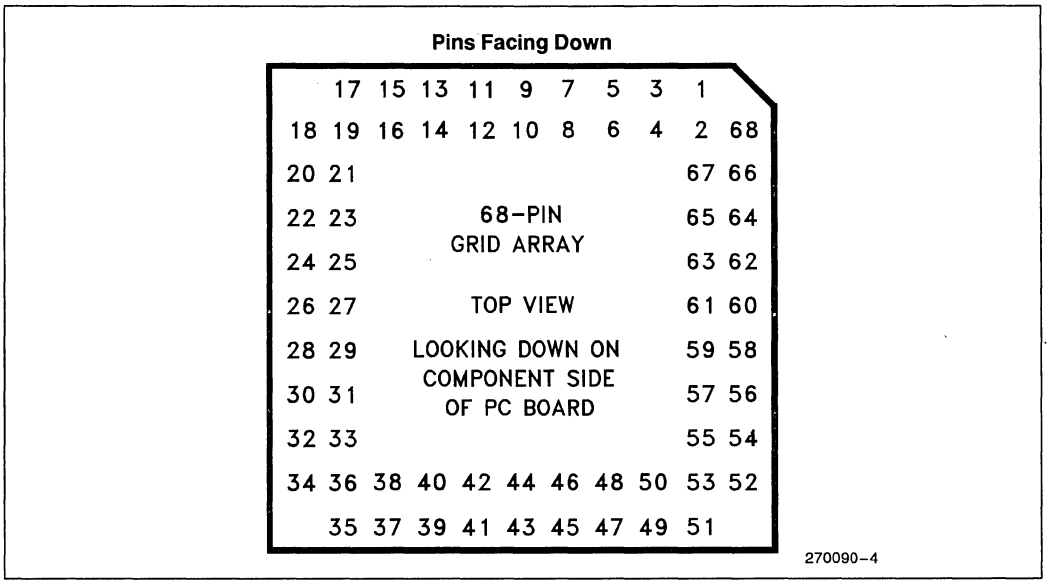


Figure 6. 68-Pin PGA Package

PGA	Description	PGA	Description	PGA	Description
1	ACH7/P0.7/PMODE.3	24	AD6/P3.6	47	P1.6
2	ACH6/P0.6/PMODE.2	25	AD7/P3.7	48	P1.5
3	ACH2/P0.2	26	AD8/P4.0	49	HSO.1
4	ACH0/P0.0	27	AD9/P4.1	50	HSO.0/$\overline{\text{PACT}}$
5	ACH1/P0.1	28	AD10/P4.2	51	HSO.5/HSI.3/SID.3
6	ACH3/P0.3	29	AD11/P4.3	52	HSO.4/HSI.2/SID.2
7	NMI	30	AD12/P4.4	53	HSI.1/SID.1
8	$\overline{\text{EA}}$	31	AD13/P4.5	54	HSI.0/SID.0
9	V_{CC}	32	AD14/P4.6	55	P1.4
10	V_{SS}	33	AD15/P4.7	56	P1.3
11	XTAL1	34	T2CLK/P2.3	57	P1.2
12	XTAL2	35	READY	58	P1.1
13	CLKOUT	36	T2RST/P2.4	59	P1.0
14	BUSWIDTH	37	$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	60	TXD/P2.0/PVER/SALE
15	INST	38	$\overline{\text{WR}}$/$\overline{\text{WRL}}$	61	RXD/P2.1/$\overline{\text{PALE}}$
16	ALE/$\overline{\text{ADV}}$	39	PWM/P2.5/$\overline{\text{PDO}}$/$\overline{\text{SPROG}}$	62	$\overline{\text{RESET}}$
17	$\overline{\text{RD}}$	40	P2.7	63	EXTINT/P2.2/$\overline{\text{PROG}}$
18	AD0/P3.0	41	V_{PP}	64	V_{PD}
19	AD1/P3.1	42	V_{SS}	65	V_{REF}
20	AD2/P3.2	43	HSO.3	66	ANGND
21	AD3/P3.3	44	HSO.2	67	ACH4/P0.4/PMODE.0
22	AD4/P3.4	45	P2.6	68	ACH5/P0.5/PMODE.1
23	AD5/P3.5	46	P1.7		

Figure 7. PGA Function Pinouts

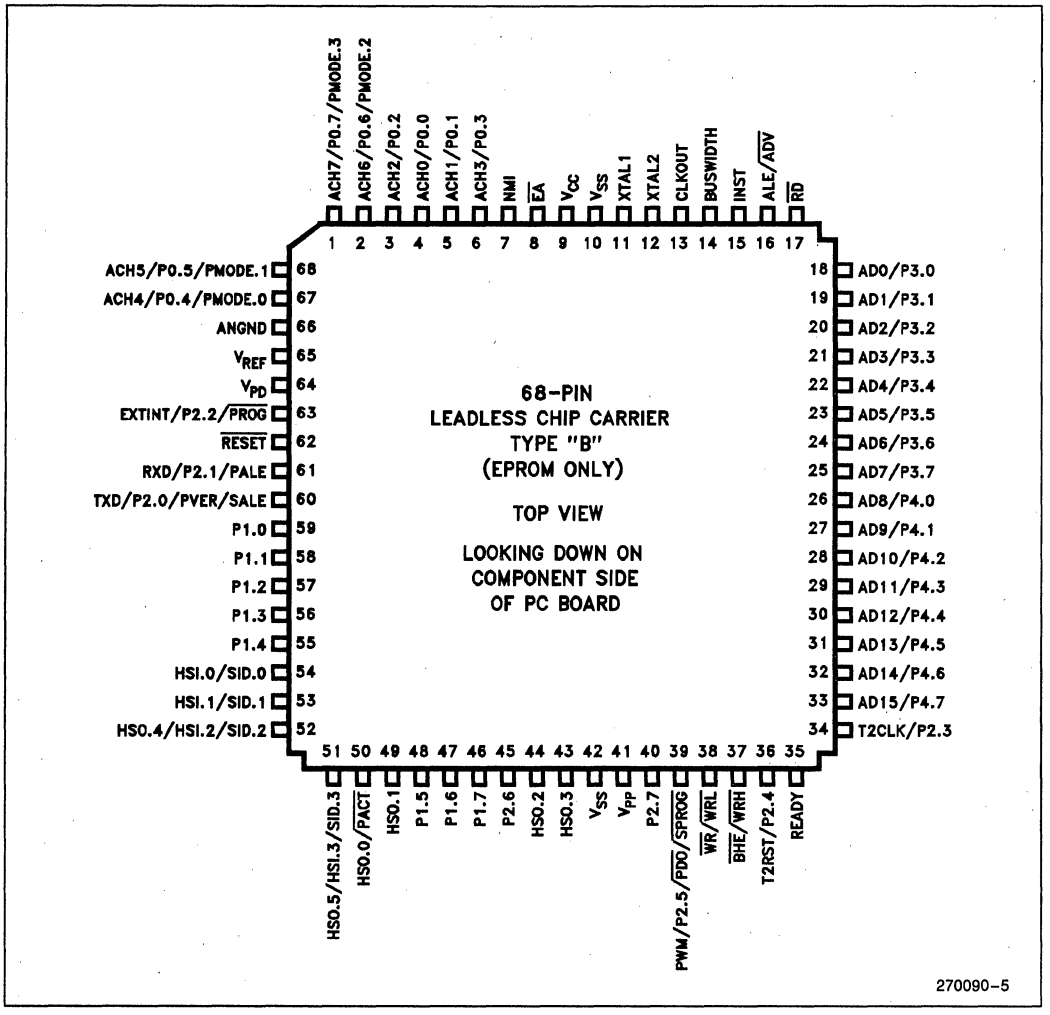


Figure 8. 68-Pin LCC Package

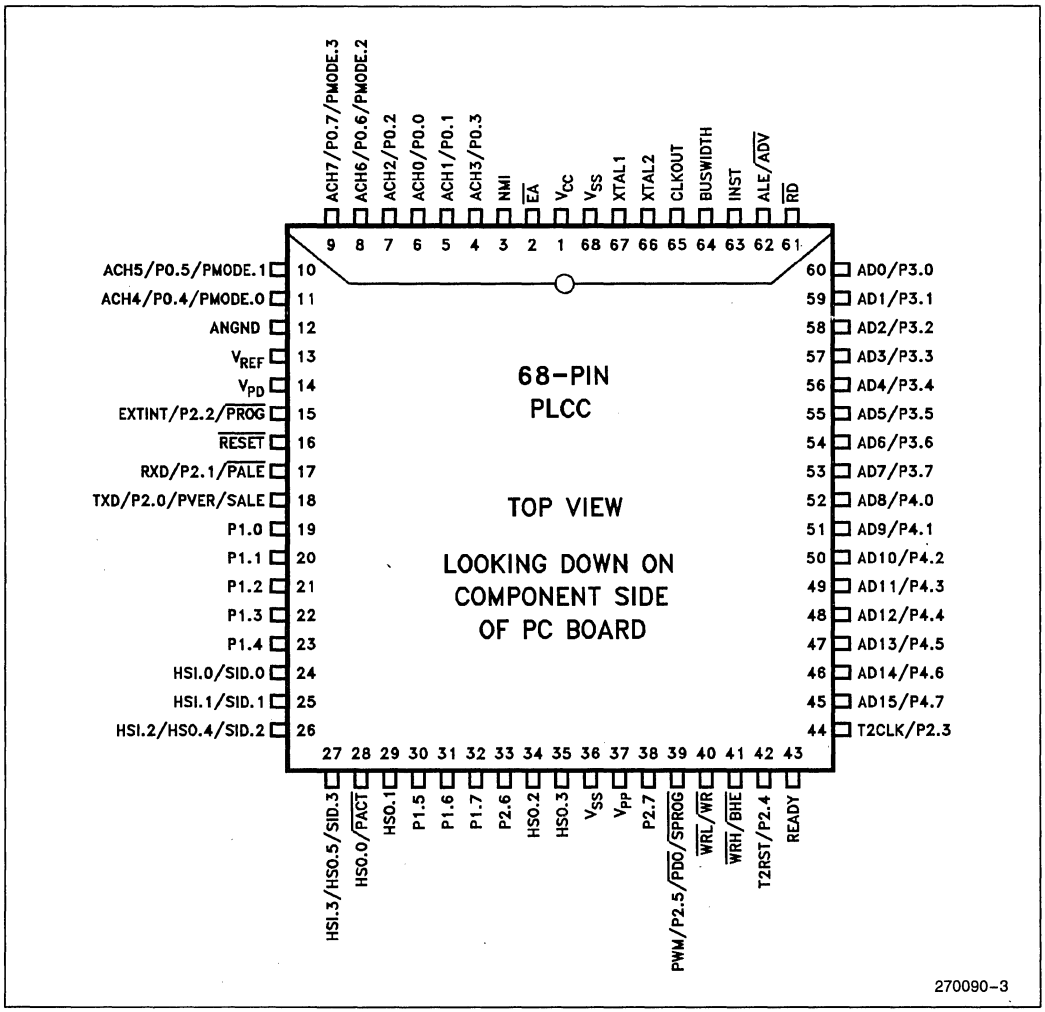


Figure 9. 68-Pin PLCC Package

15

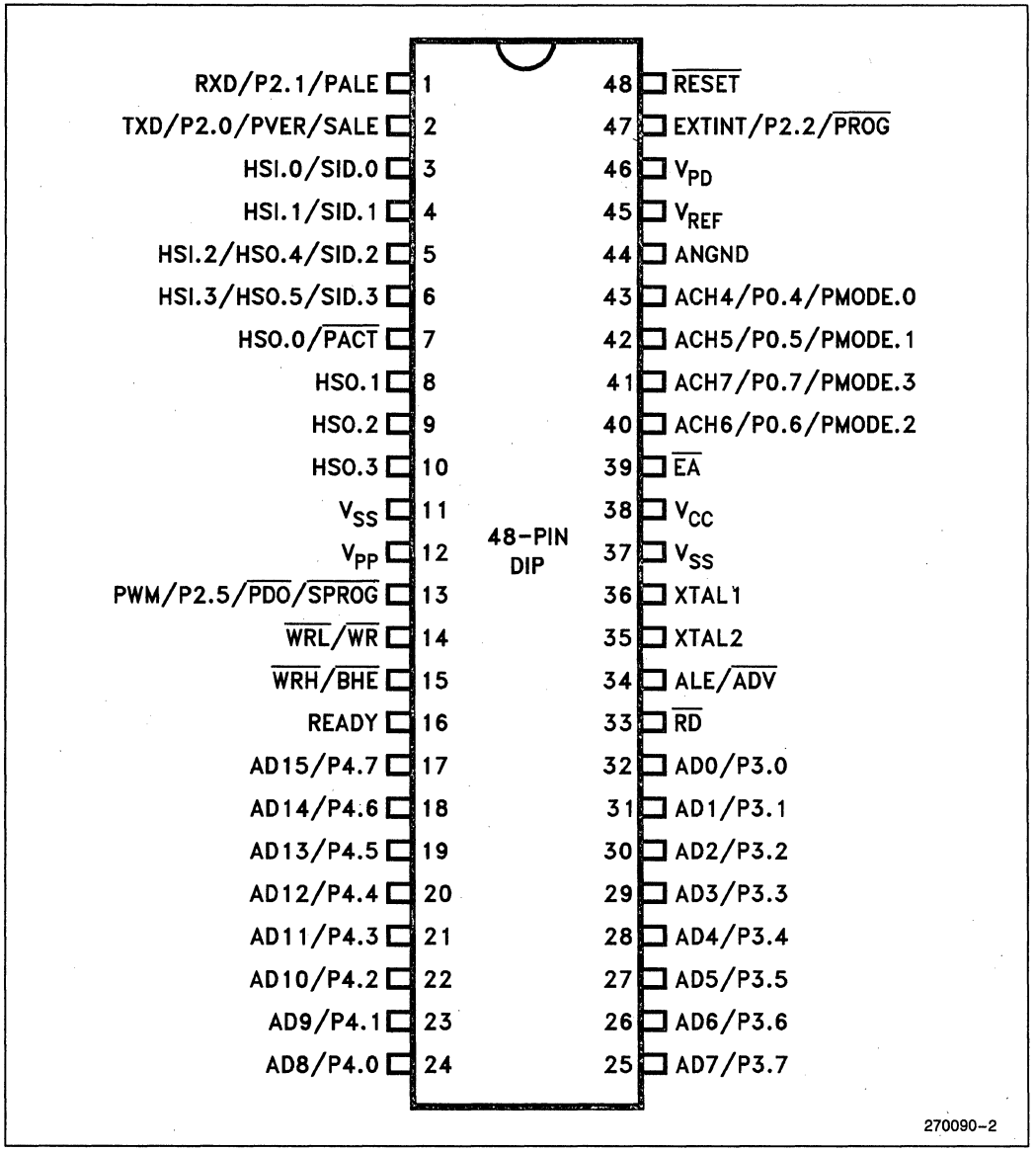


Figure 10. 48-Pin DIP Package

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which must be connected.
V_{PD}	RAM standby supply voltage (5V). This voltage must be present during normal operation. In a Power Down condition (i.e. V_{CC} drops to zero), if $\overline{RESET}$ is activated before V_{CC} drops below spec and V_{PD} continues to be held within spec., the top 16 bytes in the Register File will retain their contents.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected to use A/D or Port 0.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the EPROM devices. It should be +12.75V for programming and will float to 5V otherwise. The pin should not be above V_{CC} for ROM and CPU devices. This pin must be left floating in the application circuit for EPROM devices.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT*†	Output of the internal clock generator. The frequency of CLKOUT is 1/3 the oscillator frequency. It has a 33% duty cycle.
$\overline{RESET}$	Reset input to the chip. Input low for a minimum 10 XTAL1 cycles to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
BUSWIDTH*†	Input for bus width selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. If this pin is left unconnected, it will rise to V_{CC}.
NMI*†	A positive transition causes a vector to external memory location 0000H.
INST*†	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ equal to 12.75V causes the device to enter the Programming Mode.
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes high at the end of the bus cycle. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is activated only during external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition of CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available in the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0‡	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1†	8-bit quasi-bidirectional I/O port.
Port 2†	8-bit multi-functional port. Six of its pins are shared with other functions in the 8096BH, the remaining 2 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Ports 3 and 4 are also used as a command, address and data path by EPROM devices operating in the Programming Mode.*
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming Mode indicates that programming is in progress. A high signal indicates programming is complete.
PVAL	A low signal in Auto Programming Mode indicates that the device programmed correctly.
SALE	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (output from master).
$\overline{\text{SPROG}}$	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming data (output from master).
SID	Assigns a pin of Ports 3 and 4 to each slave to pass programming verification.
PALE	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that Ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
PVAL	A high signal in Slave Programming Mode indicates the device programmed correctly.
$\overline{\text{PDO}}$	A low signal in Slave Programming Mode indicates that the PROG pulse was applied for longer than allowed.

*Not available on Shrink-DIP package
†Not available on 48-pin device
‡Port 0.0.1.2.3 not available on 48-pin device

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias −55°C to +125°C

Storage Temperature .....−60°C to +150°C

Voltage from $\overline{EA}$ or V_{PP} to V_{SS} or ANGND .....−0.3V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND .....−0.3V to +7.0V(1)

Average Output Current from Any Pin .....10 mA

Power Dissipation(2) 1.5W

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM and CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature Under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	6.0	12	MHz
V_{PD}	Power-Down Supply Voltage	4.50	5.50	V

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

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DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current **Commercial** Temp.		240	mA	All Outputs Disconnected.
I_{CC}	V_{CC} Supply Current **Extended** Temp.		270	mA	
I_{CC1}	V_{CC} Supply Current ($T_A \geq 70°C$)		185	mA	
I_{PD}	V_{PD} Supply Current		1	mA	Normal operation and Power-Down.
I_{REF}	V_{REF} Supply Current **Commercial** Temp.		8	mA	
I_{REF}	V_{REF} Supply Current **Extended** Temp.		10	mA	
V_{IL}	Input Low Voltage	−0.3	+0.8	V	

DC CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input High Voltage (Except $\overline{RESET}$, NMI, XTAL1)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, $\overline{RESET}$ Rising	2.4	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage, $\overline{RESET}$ Falling (Hysteresis)	2.1	V_{CC} + 0.5	V	
V_{IH3}	Input High Voltage, NMI, XTAL1	2.2	V_{CC} + 0.5	V	
I_{LI}	Input Leakage Current to each pin of HSI, P3, P4, and to P2.1.		±10	μA	V_{in} = 0 to V_{CC}
I_{LI1}	DC Input Leakage Current to each pin of P0		+3	μA	V_{in} = 0 to V_{CC}
I_{IH}	Input High Current to $\overline{EA}$		100	μA	V_{IH} = 2.4V
I_{IL}	Input Low Current to each pin of P1, and to P2.6, P2.7 **Commercial** Temp.		−125	μA	V_{IL} = 0.45V
I_{IL}	Input Low Current to each pin of P1, and to P2.6, P2.7 **Extended** Temp.		−150	μA	V_{IL} = 0.45V
I_{IL1}	Input Low Current to $\overline{RESET}$	−0.25	−2	mA	V_{IL} = 0.45V
I_{IL2}	Input Low Current P2.2, P2.3, P2.4, READY, BUSWIDTH		−50	μA	V_{IL} = 0.45V
V_{OL}	Output Low Voltage on Quasi-Bidirectional port pins and P3, P4 when used as ports		0.45	V	I_{OL} = 0.8 mA (Note 1)
V_{OL1}	Output Low Voltage on Quasi-Bidirectional port pins and P3, P4 when used as ports		0.75	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OL2}	Output Low Voltage on Standard Output pins, $\overline{RESET}$ and Bus/Control Pins		0.45	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OH}	Output High Voltage on Quasi-Bidirectional pins	2.4		V	I_{OH} = −20 μA (Note 1)
V_{OH1}	Output High Voltage on Standard Output pins and Bus/Control pins	2.4		V	I_{OH} = −200 μA (Note 1)
I_{OH3}	Output High Current on $\overline{RESET}$	−50		μA	V_{OH} = 2.4V
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	F_{TEST} = 1.0 MHz

NOTES:
1. Quasi-bidirectional pins include those on P1, for P2.6 and P2.7. Standard Output Pins include TXD, RXD (Mode 0 only), PWM, and HSO pins. Bus/Control pins include CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, INST and AD0–15.
2. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V.
   I_{OL} on quasi-bidirectional pins and Ports 3 and 4 when used as ports: 4.0 mA
   I_{OL} on standard output pins and $\overline{RESET}$: 8.0 mA
   I_{OL} on Bus/Control pins: 2.0 mA
3. During normal (non-transient) operation the following limits apply:
   Total I_{OL} on Port 1 must not exceed 8.0 mA.
   Total I_{OL} on P2.0, P2.6, $\overline{RESET}$ and all HSO pins must not exceed 15 mA.
   Total I_{OL} on Port 3 must not exceed 10 mA.
   Total I_{OL} on P2.5, P2.7, and Port 4 must not exceed 20 mA.

AC CHARACTERISTICS

Test Conditions: Load Capacitance on Output Pins = 80 pF

TIMING REQUIREMENTS (The system must meet these specifications to work with the 8X9XBH.)

Symbol	Parameter	Min	Max	Units
T_{CLYX}(2, 3)	READY Hold after CLKOUT Edge	0(1)		ns
T_{LLYV}	End of ALE/$\overline{ADV}$ to READY Valid		$2T_{OSC} - 70$	ns
T_{LLYH}	End of ALE/$\overline{ADV}$ to READY High	$2T_{OSC} + 40$	$4T_{OSC} - 80$	ns
T_{YLYH}	Non-Ready Time		1000	ns
T_{AVDV}(4)	Address Valid to Input Data Valid		$5T_{OSC} - 120$(5)	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$3T_{OSC} - 100$(5)	ns
T_{RHDX}	Data Hold after $\overline{RD}$ Inactive	0		ns
T_{RHDZ}	$\overline{RD}$ Inactive to Input Data Float	0	$T_{OSC} - 25$	ns
T_{AVGV}(2, 4)	Address Valid to BUSWIDTH Valid		$2T_{OSC} - 125$	ns
T_{LLGX}(2, 3)	BUSWIDTH Hold after ALE/$\overline{ADV}$ Low	$T_{OSC} + 40$		ns
T_{LLGV}(2, 3)	ALE/$\overline{ADV}$ Low to BUSWIDTH Valid		$T_{OSC} - 75$	ns
T_{RLPV}	Reset Low to Ports Valid		$10T_{OSC}$	ns

NOTES:
1. If the 48-pin or 64-pin device is being used then this timing can be generated by assuming that the CLKOUT falling edge has occurred at $2T_{OSC}$ + 55 (TLLCH(max) + TCHCL(max)) after the falling edge of ALE.
2. Pins not bonded out on 64-pin devices.
3. Pins not bonded out on 48-pin devices.
4. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.
5. If wait states are used, add $3T_{OSC}$ * N where N = number of wait states.

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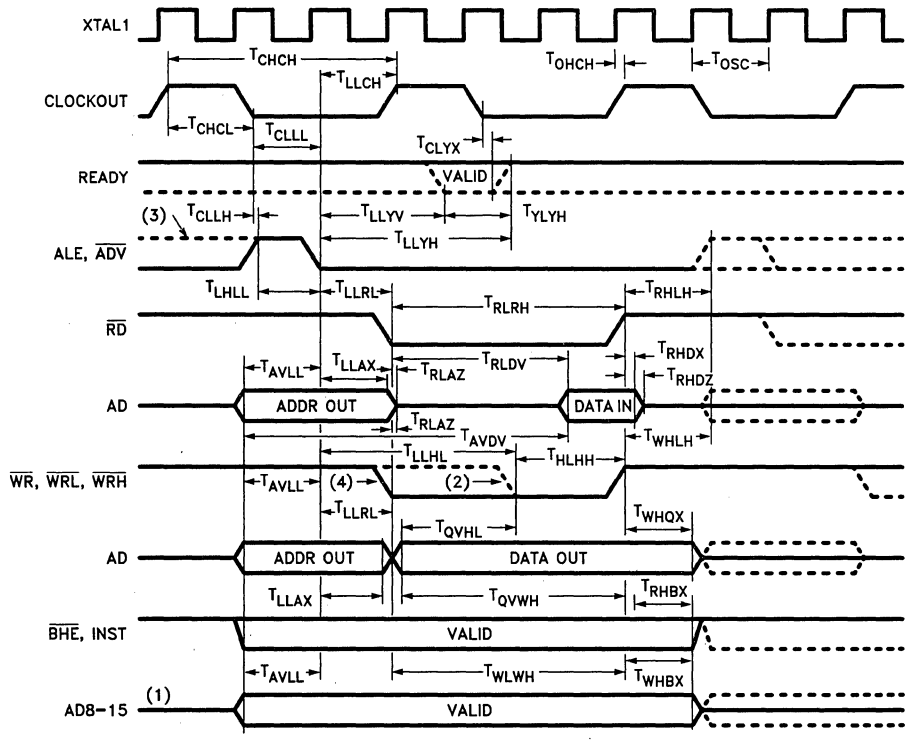
TIMING RESPONSES (MCS-96 devices meet these specs.)

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	6.0	12.0	MHz
T_{OSC}	Oscillator Period	83	166	ns
T_{OHCH}	XTAL1 Rising Edge to Clockout Rising Edge	0(4)	120(4)	ns
T_{CHCH}(1, 4)	CLKOUT Period(3)	3 T_{OSC}(3)	3 T_{OSC}(3)	ns
T_{CHCL}(1, 4)	CLKOUT High Time	T_{OSC} − 35	T_{OSC} + 10	ns
T_{CLLH}(1, 4)	CLKOUT Low to ALE High	−30	+15	ns
T_{LLCH}(4)	ALE/$\overline{ADV}$ Low to CLKOUT High(1)	T_{OSC} − 25	T_{OSC} + 45	ns
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 30	T_{OSC} + 35(5)	ns
T_{AVLL}(6)	Address Setup to End of ALE/$\overline{ADV}$	T_{OSC} − 50		ns
T_{RLAZ}(7)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Commercial** Temp.	Typ. = 0	10	ns
T_{RLAZ}(7)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Extended** Temp.		25	ns
T_{LLRL}	End of ALE/$\overline{ADV}$ to $\overline{RD}$ or $\overline{WR}$ Active	T_{OSC} − 40		ns
T_{LLAX}(7)	Address Hold after End of ALE/$\overline{ADV}$	T_{OSC} − 40		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	3 T_{OSC} − 35(2)		ns
T_{QVWH}	Output Data Valid to End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	3 T_{OSC} − 60(2)		ns
T_{WHQX}	Output Data Hold after $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	T_{OSC} − 50		ns
T_{WHLH}	End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 75		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	3 T_{OSC} − 30(2)		ns
T_{RHLH}	End of $\overline{RD}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 45		ns
T_{CLLL}(4)	CLOCKOUT Low(1) to ALE/$\overline{ADV}$ Low	T_{OSC} − 40	T_{OSC} + 35	ns
T_{RHBX}(4)	$\overline{RD}$ High to INST(1), $\overline{BHE}$, AD8-15 Inactive	T_{OSC} − 25	T_{OSC} + 30	ns
T_{WHBX}(4)	$\overline{WR}$ High to INST(1), $\overline{BHE}$, AD8-15 Inactive	T_{OSC} − 50	T_{OSC} + 100	ns
T_{HLHH}	$\overline{WRL}$, $\overline{WRH}$ Low to $\overline{WRL}$, $\overline{WRH}$ High	2 T_{OSC} − 35	2 T_{OSC} + 40	ns
T_{LLHL}	ALE/$\overline{ADV}$ Low to $\overline{WRL}$, $\overline{WRH}$ Low	2 T_{OSC} − 30	2 T_{OSC} + 55	ns
T_{QVHL}	Output Data Valid to $\overline{WRL}$, $\overline{WRH}$ Low	T_{OSC} − 60		ns

NOTES:
1. Pins not bonded out on 64-pin devices.
2. If more than one wait state is desired, add 3 T_{OSC} for each additional wait state.
3. CLKOUT is directly generated as a divide by 3 of the oscillator. The period will be 3 T_{OSC} ±10 ns if T_{OSC} is constant and the rise and fall times on XTAL1 are less than 10 ns.
4. CLKOUT, INST, and $\overline{BHE}$ pins not bonded out on 48-pin and 64-pin devices.
5. Max spec applies only to ALE. Min spec applies to both ALE and $\overline{ADV}$.
6. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.
7. The term " Address" in this definition applies to AD0–7 for 8-bit cycles, and AD0–15 for 16-bit cycles.

WAVEFORM—SYSTEM BUS TIMINGS

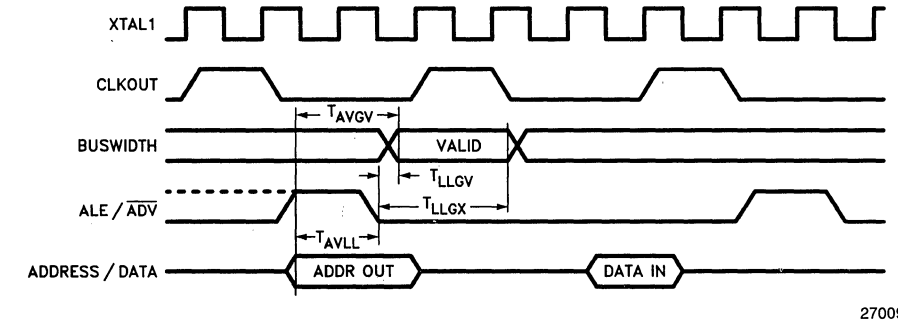


270090-47

NOTES:
1. 8-bit bus only.
2. 8-bit or 16-bit bus and write strobe mode selected.
3. When ADV selected.
4. 8- or 16-bit bus and no write strobe mode selected.

15

WAVEFORM—BUSWIDTH* TIMINGS



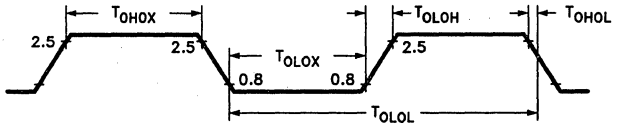
270090-35

*Buswidth is not bonded out on 48- and 64-pin devices.

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{OLOL}$	Oscillator Frequency	6	12	MHz
T_{OHOX}	High Time	25		ns
T_{OLOX}	Low Time	30		ns
T_{OLOH}	Rise Time		15	ns
T_{OHOL}	Fall Time		15	ns

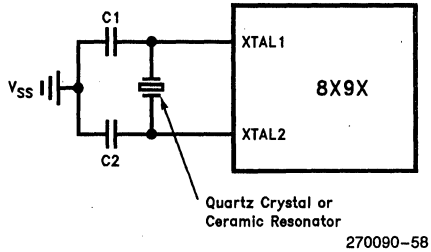
EXTERNAL CLOCK DRIVE WAVEFORMS



270090-48

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

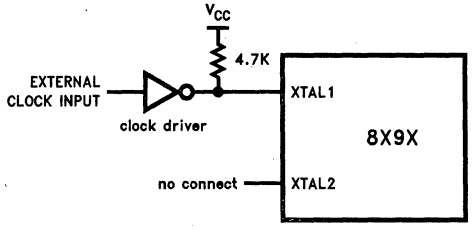
EXTERNAL CRYSTAL CONNECTIONS



270090-58

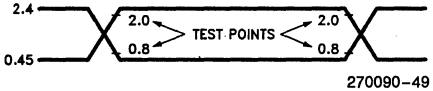
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 30 pF and C2 = 30 pF. When using ceramic resonators, consult manufacturerer for recommended capacitor values.

EXTERNAL CLOCK CONNECTIONS



270090-59

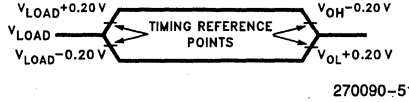
AC TESTING INPUT, OUTPUT WAVEFORMS



270090-49

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

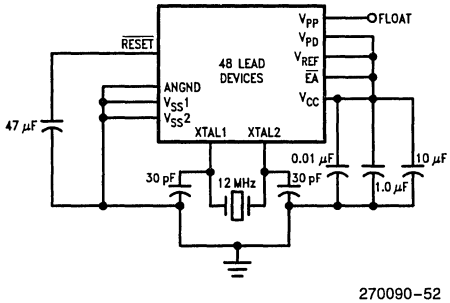
AC TESTING FLOAT WAVEFORMS



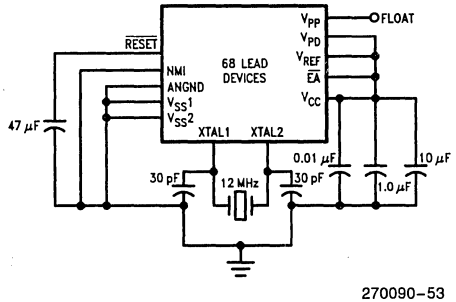
270090-51

For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs, and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 8$ mA.

MINIMUM HARDWARE CONFIGURATION CIRCUITS



270090-52



270090-53

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

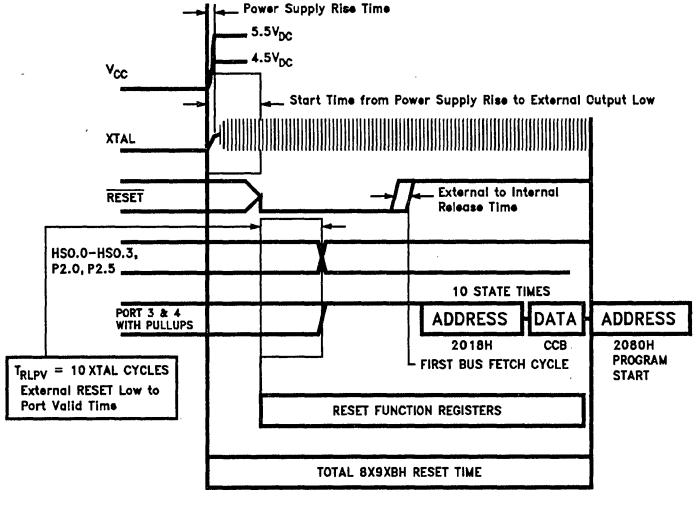
SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Load Capacitance = 80 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	2 T_{OSC} − 70		ns
T_{XHQV}	Next Output Data Valid After Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		5 T_{OSC}	ns

15

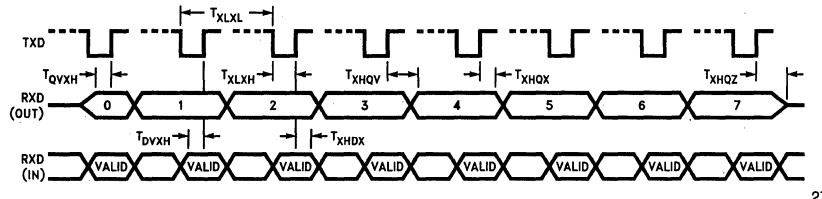
WAVEFORM—T_{RLPV}



270090-60

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



270090-36

A/D CONVERTER SPECIFICATIONS

A/D Converter operation is verified only on the 8097BH, 8397BH, 8095BH, 8395BH, 8797BH, 8795BH.

The absolute conversion accuracy is dependent on the accuracy and stability of V_{REF}.

See the MCS-96 A/D Converter Quick Reference for definitions of A/D Converter terms.

Parameter	Typical*	Minimum	Maximum	Units**	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±4	LSBs	
Full Scale Error	−0.5 ±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±4	LSBs	
Differential Non-Linearity		>−1	+2	LSBs	
Channel-to-Channel Matching		0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 3
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Series Resistance		1K	5K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Delay		3 T_{OSC} − 50	3 T_{OSC} + 50	ns	2
Sample Time		12 T_{OSC} − 50	12 T_{OSC} + 50	ns	
Sampling Capacitor			2	pF	

NOTES:
* These values are expected for most devices at 25°C.
** An "LSB", as used here, is defined in the MCS-96 A/D Converter Quick Reference and has a value of approximately 5 mV.
1. DC to 100 KHz.
2. For starting the A/D with an HSO Command.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages during Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	9.0	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
$F_{OSC}1$	Oscillator Frequency during Auto and Slave Programming	6.0	6.0	MHz
$F_{OSC}2$	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

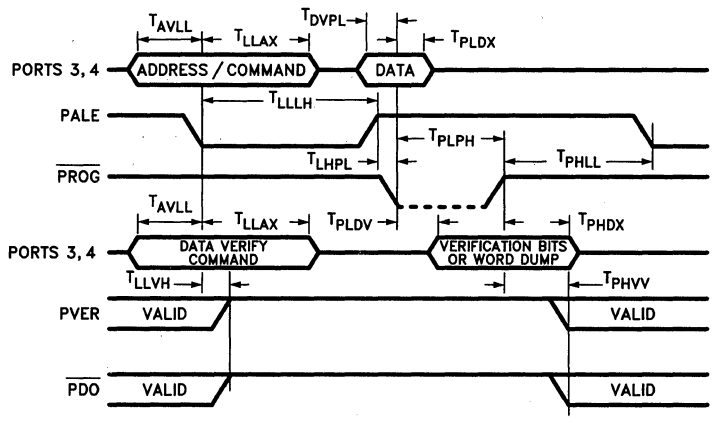
AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{AVLL}	ADDRESS/COMMAND Valid to PALE Low	0		T_{OSC}
T_{LLAX}	ADDRESS/COMMAND Hold After PALE Low	80		T_{OSC}
T_{DVPL}	Output Data Setup Before $\overline{PROG}$ Low	0		T_{OSC}
T_{PLDX}	Data Hold After $\overline{PROG}$ Falling	80		T_{OSC}
T_{LLLH}	PALE Pulse Width	180		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	250 T_{OSC}	100 μs + 144 T_{OSC}	
T_{LHPL}	PALE High to $\overline{PROG}$ Low	250		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next PALE Low	600		T_{OSC}
T_{PHDX}	Data Hold After $\overline{PROG}$ High	30		T_{OSC}
T_{PHVV}	$\overline{PROG}$ High to PVER/$\overline{PDO}$ Valid	500		T_{OSC}
T_{LLVH}	PALE Low to PVER/$\overline{PDO}$ High	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to VERIFICATION/DUMP Data Valid	100		T_{OSC}
T_{SHLL}	RESET High to First PALE Low (not shown)	2000		T_{OSC}

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (Whenever Programming)		100	mA

WAVEFORM—EPROM PROGRAMMING



8X9XBH ERRATA

Devices covered by this data sheet (see Revision History) have the following errata.

1. INDEXED, 3 OPERAND MULTIPLY

The displacement portion of an indexed, three operand (byte or word) multiply may not be in the range of 200H thru 17FFH inclusive. If you must use these displacements, execute an indexed, two operand multiply and a move if necessary.

2. HSI FIFO OPERATION

The High Speed Input (HSI) has three deviations from the specifications. Note that "events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine states may be lost.

B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-lag value to be skipped every nine timer counts. Events may receive a time-tag one count later than expected.

C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into an **empty** FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within 9 states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time tags will be at least two counts apart.

3. RESERVED LOCATION 2019H

The 1990 Architectural Overview recommended that address 2019H be loaded with 0FFH. The recommendation is now 20H.

4. RESERVED LOCATION 201CH

Reading reserved location 201CH, either internally or externally, will return "201C" as data.

5. SERIAL PORT SECTION

Serial Port Flags—Reading SP_STAT may not clear the TI or RI flag if that flag was set within two state times prior to the read. In addition, the parity error bit (RPE/RB8) may not be correct if it is read within two state times after RI is set. Use the following code to replace ORB sp_image, SP_STAT.

```
SP_READ: LDB TEMP, SP_STAT
         ORB SP_IMAGE, TEMP
         JBS TEMP,5,SP_READ; if TI is
         set then read again
         JBS TEMP,6,SP_READ; if RI is
         set then read again
         ANDB SP_IMAGE,#7FH; clear
         false RB8/RPE
         ORB SP_IMAGE, TEMP; load
         correct RB8/RPE
```

DATA SHEET REVISION HISTORY

This data sheet (270090-010) is valid for devices marked with an "E" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The difference between this data sheet (-010) and the previous one (-009) is the I_{OL}/I_{OH} for float waveform testing changed from ±15 mA to ±8 mA (this data sheet).

The following differences exist between (-009) data sheet and (-008).

1. The Express (extended temperature and burn-in options) were added to this data sheet. The 8X9XBH Express data sheet (270433-004) is now obsolete.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed. No specification changes made.
3. Added Reserved Location 201CH errata.

The following differences exist between the -008 data sheet and the -007 data sheet.

1. The -007 data sheet was valid for devices marked with a "D" at the end of the top side tracking number.
2. The following errata were removed: RESET and the Quasi-Bidirectional Ports, Software RESET Timing, and Using T2CLK as the source for Timer2.
3. The HSI FIFO Operation errata definition was changed to match change in the HSI FIFO Operation.

The following differences exist between the -007 data sheet and the -006 data sheet.

1. T_{CCLH} changed from Min = −20 ns, Max = +25 ns to Min = −30 ns, Max = +15 ns.
2. T_{XHQX} changed from Min = 2 T_{OSC} − 50 ns to Min = 2 T_{OSC} − 70 ns.
3. T_{QLOX} changed from Min = 25 ns to Min = 30 ns.
4. An errata was added changing the recommendation for address 2019H from 0FFH to 20H.
5. The power supply sequencing section has been deleted. The information is in the Hardware Design Information.
6. The method of identifying the current change indicator was added to the differences between the -005 and -004 data sheets.
7. A bug was not documented in the -004 data sheet and was fixed before the -005 data sheet. Information on the bug was added to the difference between the -005 and -004 data sheets.

Differences between -006 and -005 data sheets.

1. All EPROM programming mode information has been deleted and moved to the Hardware Design Information chapter.
2. Shrink-DIP package information has been added.
3. A new RESET timing specification has been added for clarity.
4. Software Reset pin timing information has been added.
5. HSO I_{OL} specifications have been improved so that all HS0 pins have the same drive capability.
6. Port 3 and Port 4 pin descriptions were clarified, indicating the necessity of pullup if the pins are used as ports.
7. HSI FIFO overflow description added.

Differences between the -005 and the -004 data sheets.

1. The -005 data sheet corresponds to devices marked with a "D" at the end of the topside tracking number. The -004 data sheet corresponded to devices which are not marked with a "D".
2. Much of the description of device functionality has been deleted. All of this information is already in the MCS-96 Architectural Overview.
3. The A/D converter specification for Differential Non-linearity has been changed to be a minimum of > −1 lsbs to a maximum of +2 LSBs.
4. 8X9XBH errata section. The JBS and JBC on Port 0 errata has been fixed on the latest device stepping.
5. 8X9XBH errata section. The errata for the 48-pin devices has been fixed on the latest device stepping.This errata caused the upper 8 bits on the Address/Data bus to be latched when resetting into an 8-bit external memory system.
6. 8X9XBH errata section. An errata existed which caused the device to be held in RESET for extended periods of time with the internal RESET pin pulled down internally. The condition occurred when the XTAL inputs were driven before V_{CC} was stable and within the data sheet specification. The condition was worse at cold. This errata was not documented in the -004 data sheet. It has been fixed on the latest device stepping.
7. 8X9XBH errata section. Errata 3 and 4 have been added to the errata list. These errata exist for all steppings of the device.

Differences between the -004 and the -003 data sheets.

1. The bus control figures and bus timing diagrams were modified to more accurately describe their operation. In particular the 8-bit bus modes now reflect the use of Write Strobe Mode.
2. Additional text was added to the Analog/Digital description of the conversion process to clarify its operation and usefulness.
3. Text was added to the interrupt description section to indicate the maximum transition speed of the input signal relative to the CPU's state timing. A figure was included to graphically demonstrate the interrupt response timing.
4. The pin descriptions were modified to indicate that V_{PP} must normally float in the application.
5. The input low voltage specification (V_{IL1}) was deleted and is covered by the V_{IL} specification.
6. A suggested minimum configuration circuit was added to the material.
7. The A/D Converter Specifications for Differential Non-Linearity has been corrected to be a maximum of +2 LSB's.
8. The EPROM programming section figures were corrected to indicate the correct interface to a 2764A-2. A reset circuit was added to these figures and the signal $\overline{PVAL}$ (Port 3.X and Port 4.X) is now identified as the valid signal for program verification in the Auto Programming Mode. Text was added to this section to reference the requirement of using the Auto Configuration Byte Programming Mode for 48-lead devices. Figure 22A was edited for corrections to the text, and now indicates PVER (Port 2.0). The EPROM circuits were corrected to show 6 MHz operation for programming devices from internal microcode.
9. The protected memory section was edited to indicate that the CPU will enter a "JUMP ON SELF" condition when ROM/EPROM dump mode is complete.
10. An 8X9XBH ERRATA section was added.
11. This REVISION HISTORY was added.

8097JF/8397JF/8797JF COMMERCIAL/EXPRESS HMOS MICROCONTROLLER

8797JF: an 8097JF with 16 Kbytes of On-Chip EPROM
8397JF: an 8097JF with 16 Kbytes of On-Chip ROM

- 232 Byte Register File
- 256 Bytes XRAM for Code
- 10-Bit A/D Converter with S/H
- Five 8-Bit I/O Ports
- 20 Interrupt Sources
- Pulse-Width Modulated Output
- ROM/EPROM Lock
- Run-Time Programmable EPROM (OTP)
- Extended Temperature Available
- High Speed I/O Subsystem
- Full Duplex Serial Port
- Dedicated Baud Rate Generator
- 6.25 μs 16 x 16 Multiply
- 6.25 μs 32/16 Divide
- 16-Bit Watchdog Timer
- Four 16-Bit Software Timers
- Two 16-Bit Counter/Timers
- Extended Burn-In Available

The MCS-96 family of 16-bit microcontrollers consists of many members, all of which are designed for high-speed control functions. The MCS-96 family members produced using Intel's HMOS-III process are described in this data sheet.

The CPU supports bit, byte, and word operations. Thirty-two bit double-words are supported for a subset of the instruction set. With a 12 MHz input frequency the 8097JF can do a 16-bit addition in 1.0 μs and a 16 x 16-bit multiply or 32/16 divide in 6.25 μs. Instruction execution times average 1 to 2 μs in typical applications.

Four high-speed trigger inputs are provided to record the times at which external events occur. Six high-speed pulse generator outputs are provided to trigger external events at preset times. The high-speed output unit can simultaneously perform software timer functions. Up to four 16-bit software timers can be in operation at once.

The on-chip A/D converter includes a Sample and Hold, and converts up to 8 multiplexed analog input channels to 10-bit digital values. With a 12 MHz crystal, each conversion takes 22 μs.

Also provided on-chip are a serial port, a Watchdog Timer and a pulse-width modulated output signal.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

With the extended burn-in option, the burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ± 0.5V, following the guidelines in MIL-STD-883, Method 1015.

See the Packaging information for extended temperature and extended burn-in designators.

July 1992
Order Number: 270795-006

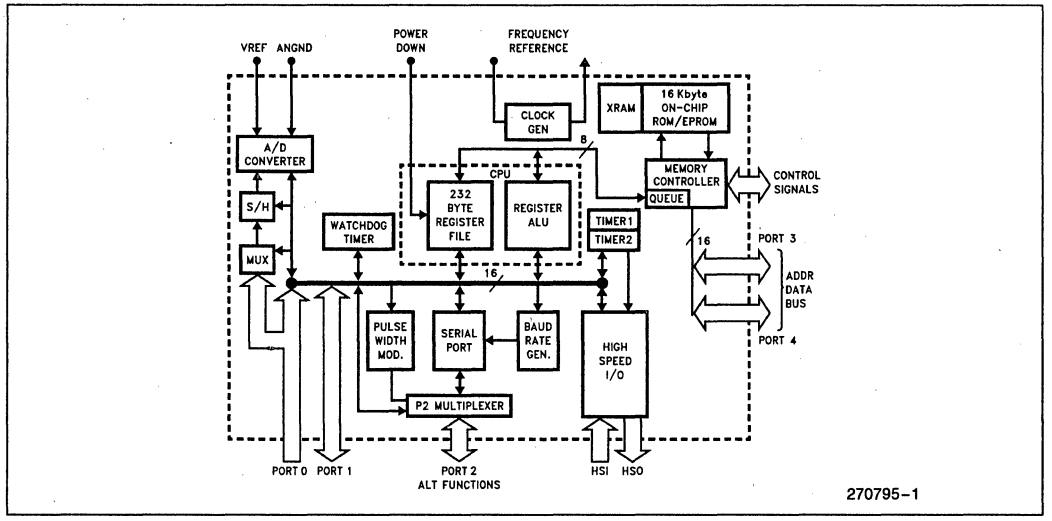


Figure 1. 8X97JF Block Diagram

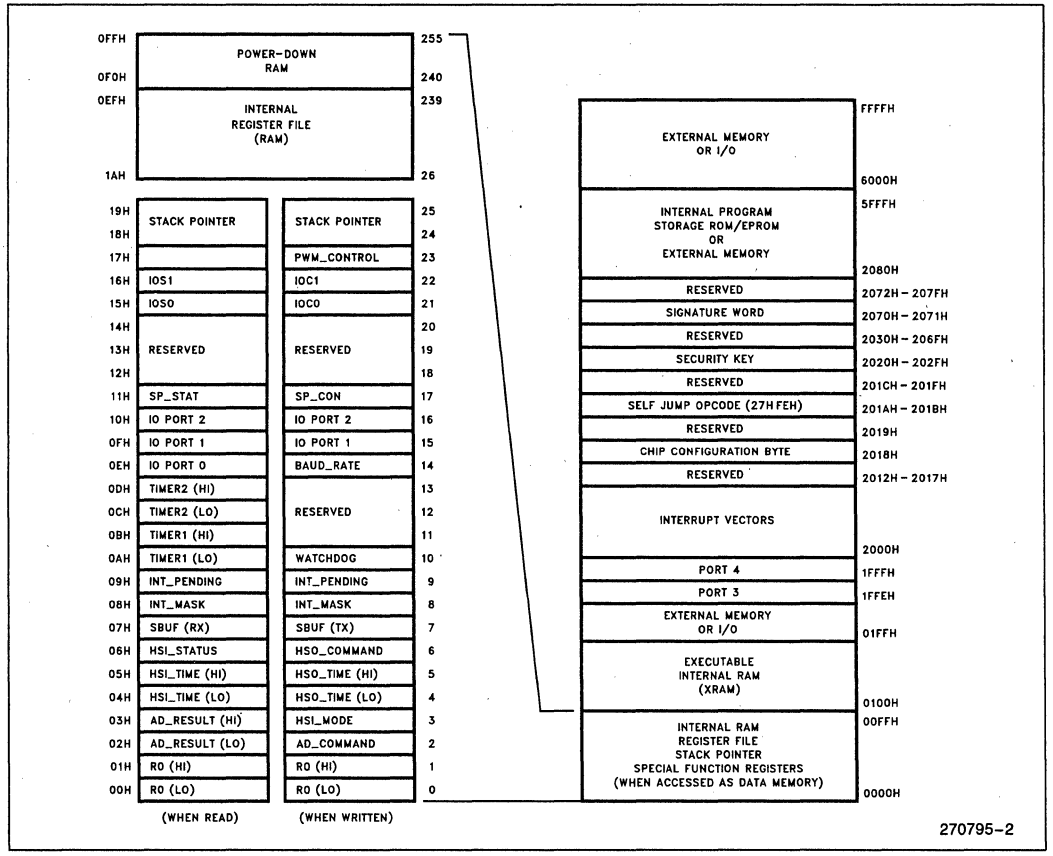


Figure 2. 8X97JF Memory Map

PACKAGING

The 8097JF is available in 64-pin and 68-pin packages, with and without on-chip ROM or EPROM. The 8097JF numbering system is shown in Figure 3. Figures 5–6 show the pinouts for the 64- and 68-pin packages. The 64-pin version is offered in a Shrink-DIP package while the 68-pin versions come in a Plastic Leaded Chip Carrier (PLCC).

8X97JF PACKAGING

Factory Masked ROM		CPU		User Programmable OTP	
68-Pin	64-Pin	68-Pin	64-Pin	68-Pin	64-Pin
8397JF	8397JF	8097JF	8097JF	8797JF	8797JF

Figure 3. The 8097JF Family Nomenclature

Package Designators:
N = PLCC
U = Shrink DIP

Prefix Designators:
T = Extended Temperature
L = Extended Temperature with 160 hrs Burn-in

Package Type	θ_{ja}	θ_{jc}
68L PLCC	37°C/W	13°C/W
64L Shrink DIP	56°C/W	—

Figure 4. 8X97JF Thermal Characteristics

All thermal impedance data is approximate for static air conditions a 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

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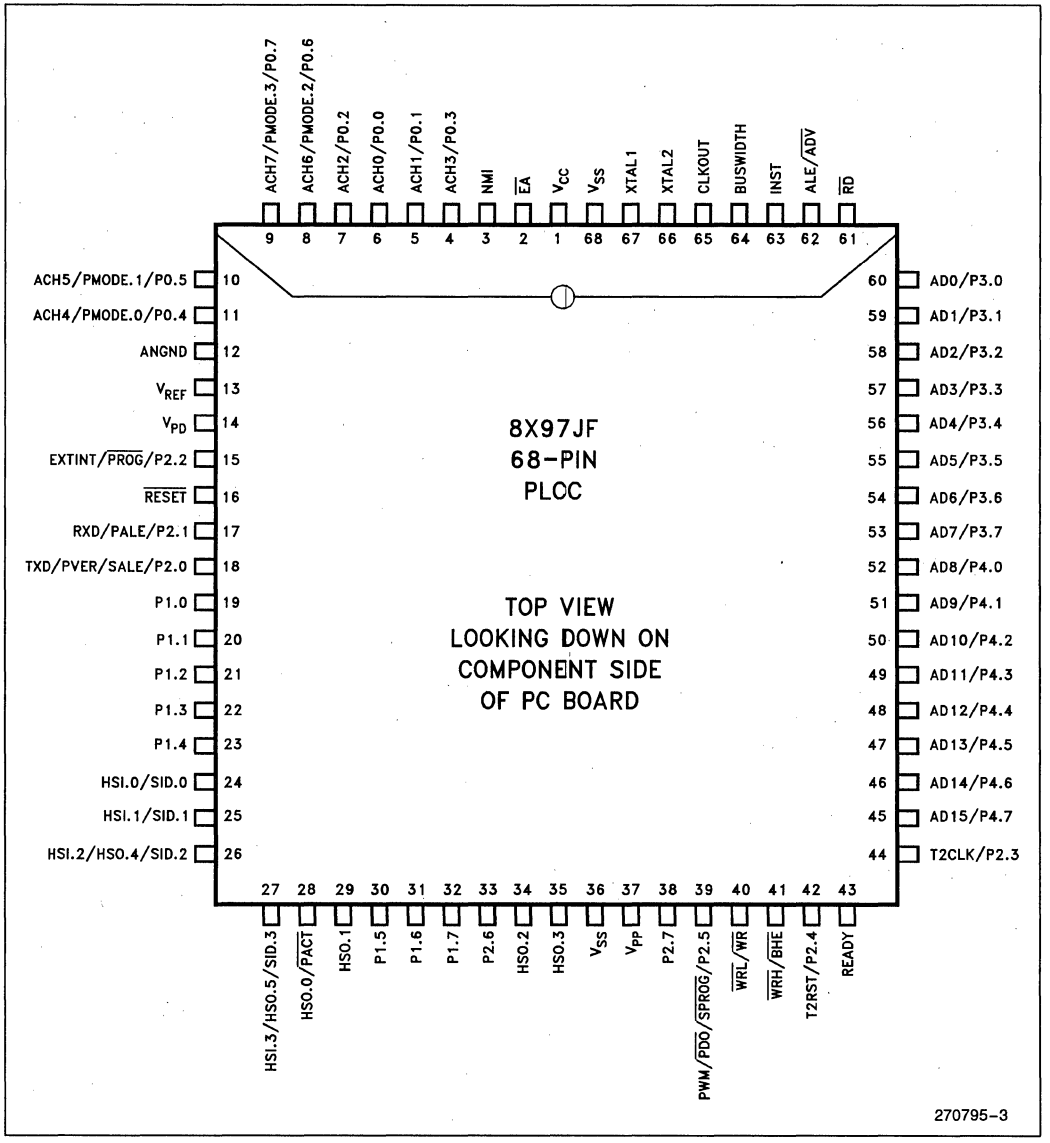

Figure 5. 68-Pin PLCC Package

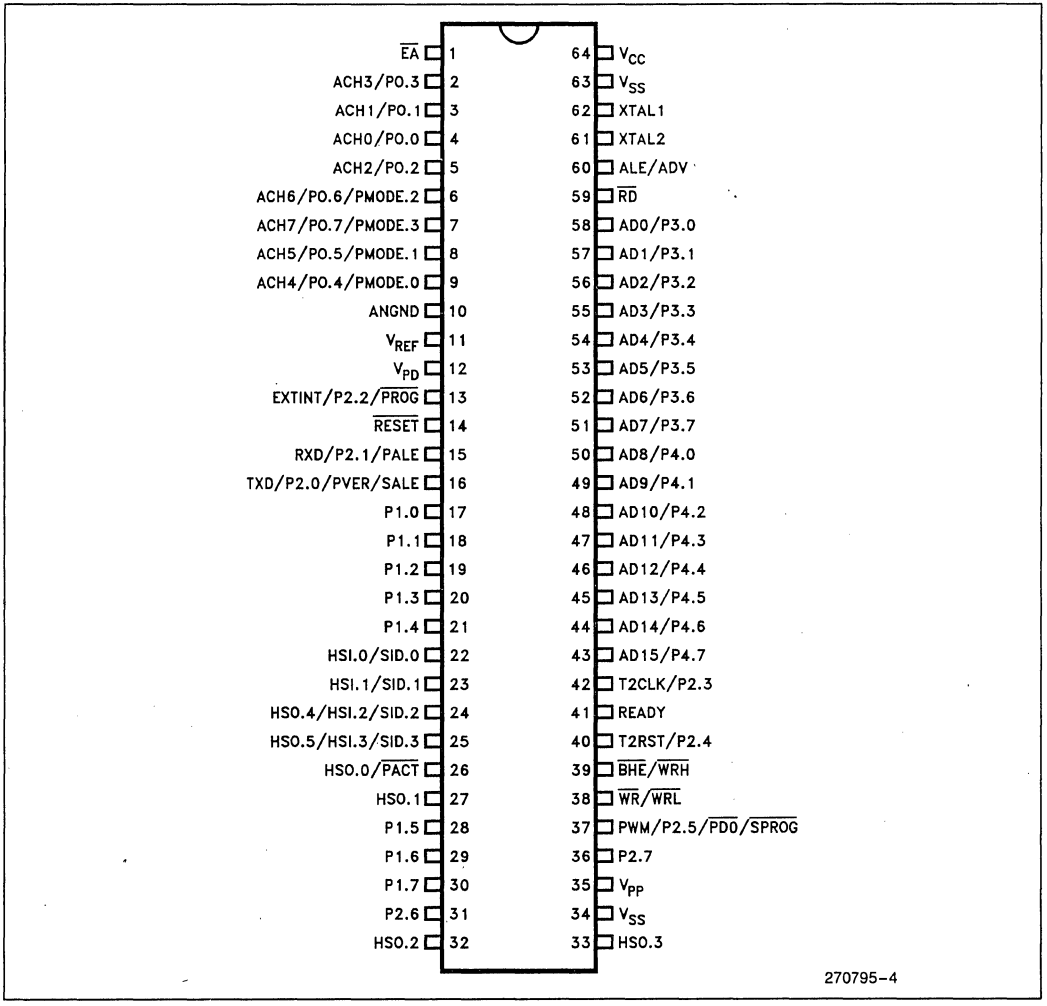

Figure 6. Shrink-DIP Package

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PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which must be connected.
V_{PD}	RAM standby supply voltage (5V). This voltage must be present during normal operation. In a Power Down condition (i.e., V_{CC} drops to zero), if $\overline{RESET}$ is activated before V_{CC} drops below spec and V_{PD} continues to be held within spec., the top 16 bytes in the Register File will retain their contents.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected to use A/D or Port 0.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the EPROM devices. It should be +12.75V for programming and will float to 5V otherwise. It should not be above V_{CC} for ROM or CPU devices. This pin must be left floating in the application circuit for EPROM devices.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT*	Output of the internal clock generator. The frequency of CLKOUT is 1/3 the oscillator frequency. It has a 33% duty cycle.
$\overline{RESET}$	Reset input to the chip. Input low for a minimum of 10 XTAL1 cycles to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
BUSWIDTH*	Input for bus width selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. If this pin is left unconnected, it will rise to V_{CC}.
NMI*	A positive transition causes a vector to external memory location 0000H.
INST*	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 5FFF to be directed to on-chip ROM/EPROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ = +12.75V causes the device to enter the Programming Mode.
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is activated only during external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.

*Not available on Shrink-DIP Package

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition of CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available in the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. Six of its pins are shared with other functions in the 8096JF, the remaining 2 are quasi-bidirectional. These pins are also used to input and output control signals on EPROM devices in Programming Mode.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus, which has strong internal pull-ups. Ports 3 and 4 are also used as a command, address and data path by EPROM devices operating in the Programming Mode.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming Mode indicates that programming is in progress. A high signal indicates programming is complete.
PVAL	A low signal in Auto Programming Mode indicates that the device programmed correctly.
SALE	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (output from master).
$\overline{\text{SPROG}}$	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming data (output from master).
SID	Assigns a pin of Ports 3 and 4 to each slave to pass programming verification.
PALE	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that Ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
PVAL	A high signal in Slave Programming Mode indicates the device programmed correctly.
$\overline{\text{PDO}}$	A low signal in Slave Programming Mode indicates that the PROG pulse was applied for longer than allowed.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −60°C to +150°C
Voltage from $\overline{EA}$ or V_{PP}
to V_{SS} or ANGND ..... −0.3V to +13.0V
Voltage from Any Other Pin to
V_{SS} or ANGND ..... −0.3V to +7.0V(1)
Average Output Current from Any Pin ..... 10 mA
Power Dissipation(2) 1.5W

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM and CPU only devices.
2. Power dissipation is based on package heat transfer characteristics, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics specified in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature Under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	6.0	12	MHz
V_{PD}	Power-Down Supply Voltage	4.50	5.50	V

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current **Commercial** Temp.		300	mA	All Outputs Disconnected
I_{CC}	V_{CC} Supply Current **Extended** Temp.		330	mA	
I_{CC}	V_{CC} Supply Current ($T_A \geq 70°C$)		245	mA	
I_{PD}	V_{PD} Supply Current		1	mA	Normal operation and Power-Down
I_{REF}	V_{REF} Supply Current **Commercial** Temp.		8	mA	
I_{REF}	V_{REF} Supply Current **Extended** Temp.		10	mA	
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IL1}	Input Low Voltage, $\overline{RESET}$ **Commercial** Temp.	−0.3	+0.8	V	
V_{IL1}	Input Low Voltage, $\overline{RESET}$ **Extended** Temp.	−0.3	+0.7	V	

DC CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input High Voltage (Except $\overline{RESET}$, NMI, XTAL1)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, $\overline{RESET}$ Rising	2.4	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage, $\overline{RESET}$ Falling (Hysteresis)	2.1	V_{CC} + 0.5	V	
V_{IH3}	Input High Voltage, NMI, XTAL1 **Commercial** Temp.	2.2	V_{CC} + 0.5	V	
V_{IH3}	Input High Voltage, NMI, XTAL1 **Extended** Temp.	2.3	V_{CC} + 0.5	V	
I_{LI}	Input Leakage Current to each pin of HSI, P3, P4, and to P2.1		±10	μA	V_{IN} = 0 to V_{CC}
I_{LI1}	DC Input Leakage Current to each pin of P0		+3	μA	V_{IN} = 0 to V_{CC}
I_{IH}	Input High Current to $\overline{EA}$		100	μA	V_{IH} = 2.4V
I_{IL}	Input Low Current to each pin of P1, and to P2.6, P2.7 **Commercial** Temp.		−125	μA	V_{IL} = 0.45V
I_{IL}	Input Low Current to each pin of P1, and to P2.6, P2.7 **Extended** Temp.		−150	μA	V_{IL} = 0.45V
I_{IL1}	Input Low Current to $\overline{RESET}$	−0.25	−2	mA	V_{IL} = 0.45V
I_{IL2}	Input Low Current P2.2, P2.3, P2.4, READY, BUSWIDTH		−50	μA	V_{IL} = 0.45V
V_{OL}	Output Low Voltage on Quasi-Bidirectional port pins and P3, P4 when used as ports		0.45	V	I_{OL} = 0.8 mA (Note 1)
V_{OL1}	Output Low Voltage on Quasi-Bidirectional port pins and P3, P4 when used as ports		0.75	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OL2}	Output Low Voltage on Standard Output pins, $\overline{RESET}$ and Bus/Control Pins		0.45	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OH}	Output High Voltage on Quasi-Bidirectional pins	2.4		V	I_{OH} = −20 μA (Note 1)
V_{OH1}	Output High Voltage on Standard Output pins and Bus/Control pins	2.4		V	I_{OH} = −200 μA (Note 1)
I_{OH3}	Output High Current on $\overline{RESET}$	−50		μA	V_{OH} = 2.4V
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	F_{TEST} = 1.0 MHz

NOTES:
1. Quasi-bidirectional pins include those on P1, for P2.6 and P2.7. Standard Output Pins include TXD, RXD (Mode 0 only), PWM and HSO pins. Bus/Control pins include CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, INST and AD0–15.
2. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V.
   I_{OL} on quasi-bidirectional pins and Ports 3 and 4 when used as ports: 4.0 mA
   I_{OL} on standard output pins and $\overline{RESET}$: 8.0 mA
   I_{OL} on Bus/Control pins: 2.0 mA
3. During normal (non-transient) operation the following limits apply:
   Total I_{OL} on Port 1 must not exceed 8.0 mA.
   Total I_{OL} on P2.0, P2.6, $\overline{RESET}$ and all HSO pins must not exceed 15 mA.
   Total I_{OL} on Port 3 must not exceed 10 mA.
   Total I_{OL} on P2.5, P2.7, and Port 4 must not exceed 20 mA.

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AC CHARACTERISTICS

Test Conditions: Load Capacitance on Output Pins = 80 pF

TIMING REQUIREMENTS (The system must meet these specifications to work with the 8X97JF)

Symbol	Parameter	Min	Max	Units
T_{CLYX}(3)	READY Hold after CLKOUT Edge	0(1)		ns
T_{LLYV}	End of ALE/$\overline{ADV}$ to READY Valid		$2T_{OSC} - 70$	ns
T_{LLYH}	End of ALE/$\overline{ADV}$ to READY High	$2T_{OSC} + 40$	$4T_{OSC} - 80$	ns
T_{YLYH}	Non-Ready Time		1000	ns
T_{AVDV}(2)	Address Valid to Input Data Valid		$5T_{OSC} - 120$(4)	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$3T_{OSC} - 100$(4)	ns
T_{RHDX}	Data Hold after $\overline{RD}$ Inactive	0		ns
T_{RHDZ}	$\overline{RD}$ Inactive to Input Data Float	0	$T_{OSC} - 25$	ns
T_{AVGV}(2,3)	Address Valid to BUSWIDTH Valid		$2T_{OSC} - 125$	ns
T_{LLGX}(3)	BUSWIDTH Hold after ALE/$\overline{ADV}$ Low	$T_{OSC} + 40$		ns
T_{LLGV}(3)	ALE/$\overline{ADV}$ Low to BUSWIDTH Valid		$T_{OSC} - 100$	ns
T_{RLPV}	Reset Low to Ports Valid		$10T_{OSC}$	ns

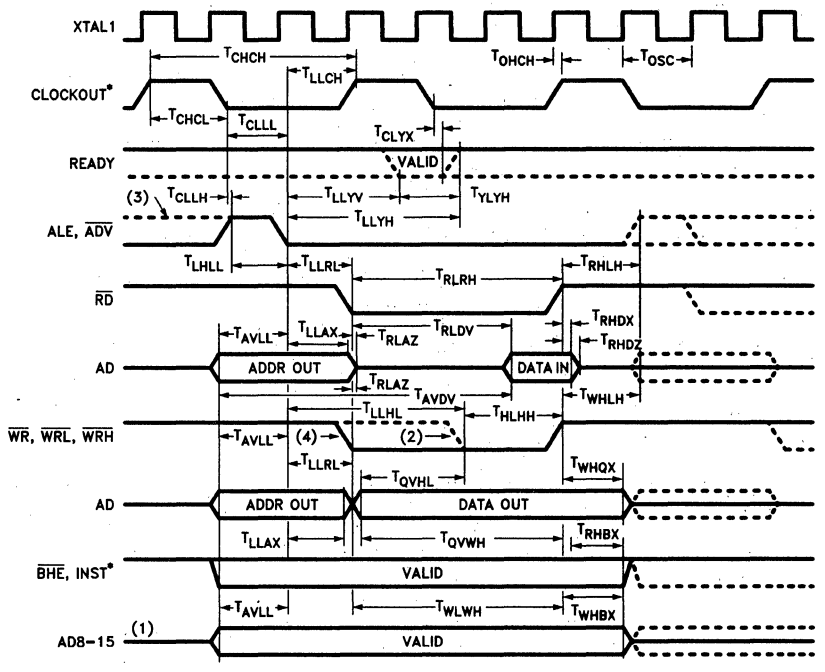
NOTES:
1. If the 64-pin device is being used then this timing can be generated by assuming that the CLKOUT falling edge has occurred at $2T_{OSC}$ + 55 (TLLCH(max) + TCHCL(max)) after the falling edge of ALE.
2. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.
3. Pins not bonded out on 64-pin devices.
4. If wait states are used, add $3T_{OSC}$ * N where N = number of wait states.

TIMING RESPONSES (8X97JF devices meet these specs.)

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	6.0	12.0	MHz
T_{OSC}	Oscillator Period	83	166	ns
T_{OHCH}(3)	XTAL1 Rising Edge to Clockout Rising Edge	0	120	ns
T_{CHCH}(3)	CLKOUT Period	3 T_{OSC}(2)	3 T_{OSC}(2)	ns
T_{CHCL}(3)	CLKOUT High Time	T_{OSC} − 35	T_{OSC} + 10	ns
T_{CLLH}(3)	CLKOUT Low to ALE High	− 30	+ 15	ns
T_{LLCH}(3)	ALE/$\overline{ADV}$ Low to CLKOUT High	T_{OSC} − 25	T_{OSC} + 45	ns
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 30	T_{OSC} + 35(4)	ns
T_{AVLL}(5)	Address Setup to End of ALE/$\overline{ADV}$	T_{OSC} − 50		ns
T_{RLAZ}(6)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Commercial** Temp.	Typ. = 0	10	ns
T_{RLAZ}(6)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Extended** Temp.		25	ns
T_{LLRL}	End of ALE/$\overline{ADV}$ to $\overline{RD}$ or $\overline{WR}$ Active	T_{OSC} − 40		ns
T_{LLAX}(6)	Address Hold after End of ALE/$\overline{ADV}$	T_{OSC} − 40		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	3 T_{OSC} − 35(1)		ns
T_{QVWH}	Output Data Valid to End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	3 T_{OSC} − 60(1)		ns
T_{WHQX}	Output Data Hold after $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	T_{OSC} − 50		ns
T_{WHLH}	End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 75		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	3 T_{OSC} − 30(1)		ns
T_{RHLH}	End of $\overline{RD}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 45		ns
T_{CLLL}(3)	CLOCKOUT Low to ALE/$\overline{ADV}$ Low	T_{OSC} − 40	T_{OSC} + 35	ns
T_{RHBX}(3)	$\overline{RD}$ High to INST, $\overline{BHE}$, AD8-15 Inactive	T_{OSC} − 25	T_{OSC} + 30	ns
T_{WHBX}(3)	$\overline{WR}$ High to INST, $\overline{BHE}$, AD8-15 Inactive	T_{OSC} − 50	T_{OSC} + 100	ns
T_{HLHH}	$\overline{WRL}$, $\overline{WRH}$ Low to $\overline{WRL}$, $\overline{WRH}$ High	2 T_{OSC} − 35	2 T_{OSC} + 40	ns
T_{LLHL}	ALE/$\overline{ADV}$ Low to $\overline{WRL}$, $\overline{WRH}$ Low	2 T_{OSC} − 30	2 T_{OSC} + 55	ns
T_{QVHL}	Output Data Valid to $\overline{WRL}$, $\overline{WRH}$ Low	T_{OSC} − 60		ns

NOTES:
1. If more than one wait state is desired, add 3 T_{OSC} for each additional wait state.
2. CLKOUT is directly generated as a divide by 3 of the oscillator. The period will be 3 T_{OSC} ±10 ns if T_{OSC} is constant and the rise and fall times on XTAL1 are less than 10 ns.
3. CLKOUT, INST and $\overline{BHE}$ pins not bonded out on 64-lead package.
4. Max spec applies only to ALE. Min spec applies to both ALE and $\overline{ADV}$.
5. The term "Address Valid" applies to AD0–15, $\overline{BHE}$ and INST.
6. The term " Address" in this specification applies to AD0–7 for 8-bit cycles, and AD0–15 for 16-bit cycles.

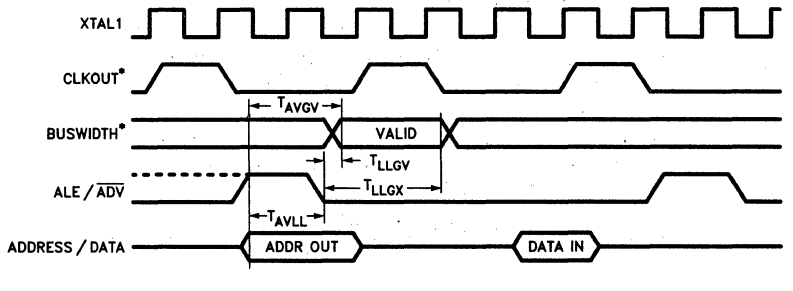
WAVEFORM—SYSTEM BUS TIMINGS



270795-18

NOTES:
1. 8-bit bus only.
2. 8-bit or 16-bit bus and write strobe mode selected.
3. When ADV selected.
4. 8- or 16-bit bus and no write strobe mode selected.

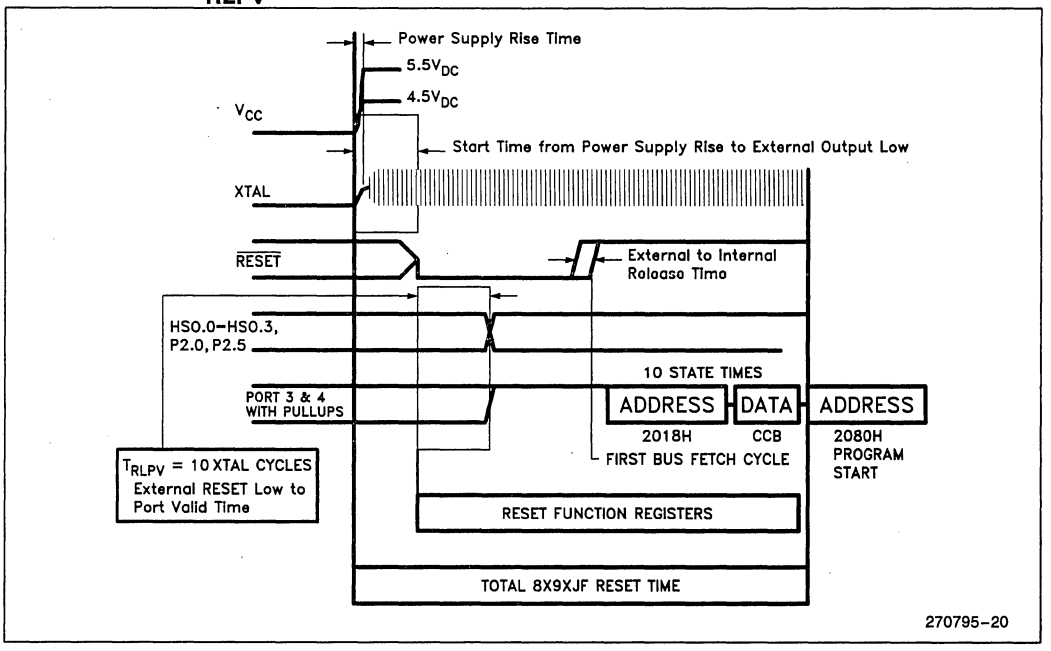
WAVEFORM—BUSWIDTH* TIMINGS



270795-19

*Not available on 64-lead package.

WAVEFORM—T_{RLPV}



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{OLOL}$	Oscillator Frequency	6	12	MHz
T_{OHOX}	High Time	25		ns
T_{OLOX}	Low Time	30		ns
T_{OLOH}	Rise Time		15	ns
T_{OHOL}	Fall Time		15	ns

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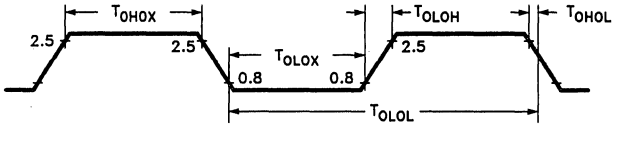
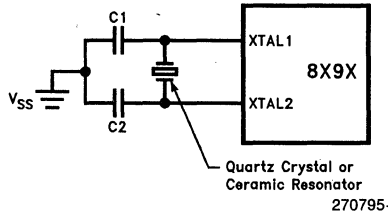
EXTERNAL CLOCK DRIVE WAVEFORMS



An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

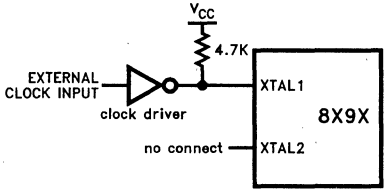
EXTERNAL CRYSTAL CONNECTIONS



270795-5

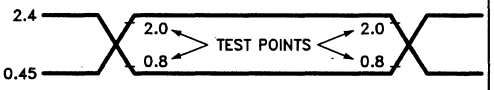
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 30 pF and C2 = 30 pF. When using ceramic resonators, consult manufacturer for recommended capacitor values.

EXTERNAL CLOCK CONNECTIONS



270795-6

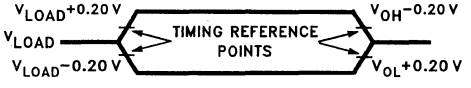
AC TESTING INPUT, OUTPUT WAVEFORMS



270795-23

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

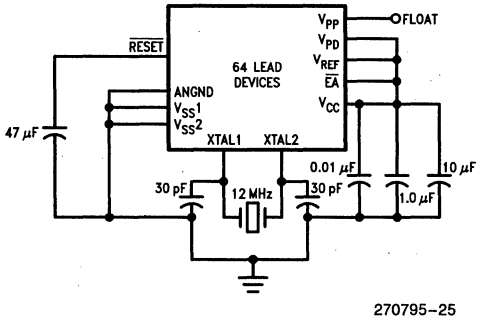
FLOAT WAVEFORMS



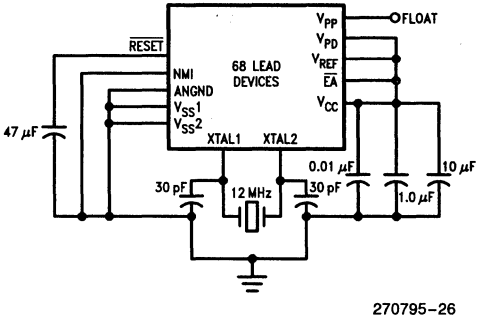
270795-24

For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs, and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 8$ mA.

MINIMUM HARDWARE CONFIGURATION CIRCUITS



270795-25



270795-26

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

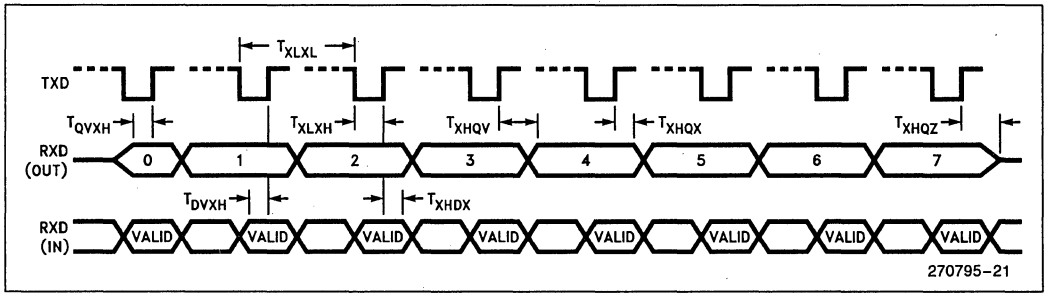
SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Load Capacitance = 80 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	2 T_{OSC} − 70		ns
T_{XHQV}	Next Output Data Valid After Clock Rising Edge		2 T_{OSC} +50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} +200		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		5 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



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A/D CONVERTER SPECIFICATIONS

The absolute conversion accuracy is dependent on the accuracy and stability of V_{REF}.

See the MCS-96 A/D Converter Quick Reference for definitions of A/D Converter terms.

Parameter	Typical*	Minimum	Maximum	Units**	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±4	LSBs	
Full Scale Error	−0.5 ±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±4	LSBs	
Differential Non-Linearity		>−1	+2	LSBs	
Channel-to-Channel Matching		0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 3
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Series Resistance		1K	5K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Delay		$3\,T_{OSC} - 50$	$3\,T_{OSC} + 50$	ns	2
Sample Time		$12\,T_{OSC} - 50$	$12\,T_{OSC} + 50$	ns	
Sampling Capacitor			2	pF	

NOTES:
* These values are expected for most devices at 25°C.
** An "LSB", as used here, is defined in the MCS-96 A/D Converter Quick Reference and has a value of approximately 5 mV.
1. DC to 100 KHz.
2. For starting the A/D with an HSO Command.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

OTP EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages during Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	9.0	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
F_{OSC}(1)	Oscillator Frequency during Auto and Slave Programming	6.0	6.0	MHz
F_{OSC}(2)	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

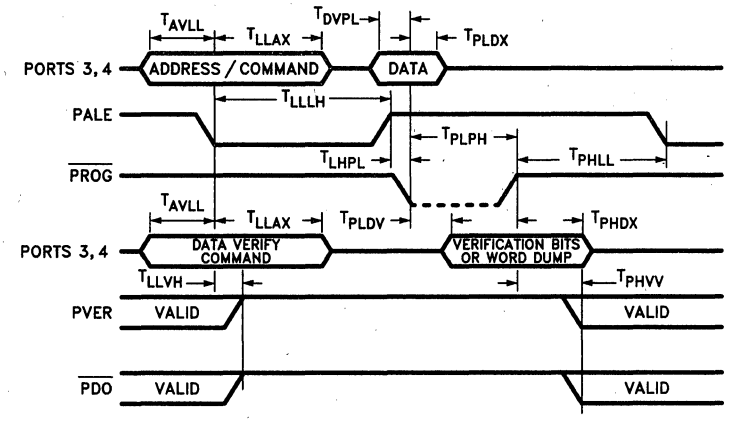
AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{AVLL}	ADDRESS/COMMAND Valid to PALE Low	0		T_{OSC}
T_{LLAX}	ADDRESS/COMMAND Hold After PALE Low	80		T_{OSC}
T_{DVPL}	Output Data Setup Before $\overline{PROG}$ Low	0		T_{OSC}
T_{PLDX}	Data Hold After $\overline{PROG}$ Falling	80		T_{OSC}
T_{LLLH}	PALE Pulse Width	180		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	250 T_{OSC}	100 μs + 144 T_{OSC}	
T_{LHPL}	PALE High to $\overline{PROG}$ Low	250		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next PALE Low	600		T_{OSC}
T_{PHDX}	Data Hold After $\overline{PROG}$ High	30		T_{OSC}
T_{PHVV}	$\overline{PROG}$ High to PVER/$\overline{PDO}$ Valid	500		T_{OSC}
T_{LLVH}	PALE Low to PVER/$\overline{PDO}$ High	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to VERIFICATION/DUMP Data Valid	100		T_{OSC}
T_{SHLL}	RESET High to First PALE Low (not shown)	2000		T_{OSC}

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (Whenever Programming)		100	mA

WAVEFORM—EPROM PROGRAMMING (OTP)



REVISION HISTORY

This data sheet (270795-005) is valid for devices with a "B" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following difference exists between this -006 data sheet and the previous one -005.

1. The I_{OL}/I_{OH} for float waveform testing changed from ±15 mA to ±8 mA (this data sheet).

The following differences exist between -005 and -004.

1. The Express (extended temperature and burn-in options) were added to this data sheet. The 8X9XJF EXPRESS data sheet (270796-001) is now obsolete.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed. No spec changes were made.
3. Added Reserved Location 201CH errata.

The following differences exist between the -004 data sheet and the -003 data sheet.

1. The -003 data sheet was valid only for devices marked with an "A" at the end of the top side tracking number.
2. Added V_{IL1} (Input Low Voltage, $\overline{RESET}$)

The following differences exist between the -003 data sheet and the -002 data sheet.

1. The reserved location section and the power supply sequencing section has been deleted. This information is in the Hardware Design Information.
2. The Software Reset Timing bug was removed from the Functional Deviations. The RESET pin will pull down for at least 2 states if a software reset or watchdog timer overflow occurs.

Differences between the -002 and -001 data sheets.

1. The TLLGV spec has been changed from Max = T_{OSC} − 75 ns to Max = T_{OSC} = 100 ns.
2. The TCLLH spec has been changed from Min = −20 ns and Max = +25 ns to Min = −30 ns and Max = +15 ns.
3. The TXHQX spec has been changed from Min = 2 T_{OSC} − 50 ns to 2T_{OSC} − 70 ns.
4. The TOLOX spec has been changed from Min = 25 ns to Min = 30 ns.
5. Added "20" recommendation for reserved address 2019H to EPROM specification.
6. Added errata.

8X97JF ERRATA

Devices covered by this data sheet (see Revision History) have the following errata.

1. INDEXED, 3 OPERAND MULTIPLY

   The displacement portion of an indexed, three operand (byte or word) multiply may not be in the range of 200H thru 17FFH inclusive. If you must use these displacements, execute an indexed, two operand multiply and a move if necessary.

2. 8X97JF HIGH SPEED INPUTS

   The High Speed Input (HSI) has three deviations from the specifications. Note that "events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

   A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine state times may be lost.

   B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-tag value to be skipped every nine timer counts. Events may receive a time tag one count later than expected.

   C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into any **empty** FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within 9 states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time-tags will be at least two counts apart.

3. RESERVED LOCATION 2019H

   The 1990 Architectural Overview recommends that reserved location 2019H be filled with hex value FFH. The recommendation is now to fill 2019H with hex value 20H.

4. RESERVED LOCATION 201CH

   Reading reserved location 201CH, either internally or externally, will return "201C" as data.

5. SERIAL PORT SECTION

   Serial Port Flags—Reading SP_STAT may not clear the TI or RI flag if that flag was set within two state times prior to the read. In addition, the parity error bit (RPE/RB8) may not be correct if it is read within two state times after RI is set. Use the following code to replace ORB sp_image, SP_STAT.

```
SP_READ: LDB TEMP, SP_STAT
         ORB SP_IMAGE, TEMP
         JBS TEMP,5,SP_READ; if TI
         is set then read again
         JBS TEMP,6,SP_READ; if RI
         is set then read again
         ANDB SP_IMAGE,#7FH; clear
         false RB8/RPE
         ORB SP_IMAGE, TEMP; load
         correct RB8/RPE
```

8098/8398/8798
COMMERCIAL/EXPRESS HMOS MICROCONTROLLER

- **8798: an 8098 with 8 Kbytes of On-Chip EPROM**
- **8398: an 8098 with 8 Kbytes of On-Chip ROM**

- **232 Byte Register File**
- **Register-to-Register Architecture**
- **10-Bit A/D Converter with S/H**
- **Two 8-Bit and Two 4-Bit I/O Ports**
- **20 Interrupt Sources**
- **Pulse-Width Modulated Output**
- **ROM/EPROM Lock**
- **High Speed I/O Subsystem**
- **Extended Temperature Available**
- **Full Duplex Serial Port**
- **Dedicated Baud Rate Generator**
- **6.25 μs 16 x 16 Multiply**
- **6.25 μs 32/16 Divide**
- **16-Bit Watchdog Timer**
- **Four 16-Bit Software Timers**
- **Two 16-Bit Counter/Timers**
- **Run-Time Programmable EPROM**
- **Extended Burn-In Available**

The MCS®-96 family of 16-bit microcontrollers consists of many members, all of which are designed for high-speed control functions. The 8X98 members were designed specifically for those applications that require the speed of a 16-bit microcontroller but are limited by board space and cost requirements to an 8-bit external bus. The 8X98 members are produced using Intel's HMOS-III process.

The CPU supports bit, byte, and word operations. Thirty-two bit double-words are supported for a subset of the instruction set. With a 12 MHz input frequency the 8098 can do a 16-bit addition in 1.0 μs and a 16 x 16-bit multiply or 32/16 divide in 6.25 μs. Instruction execution times average 1 to 2 μs in typical applications.

Four high-speed trigger inputs are provided to record the times at which external events occur. Six high-speed pulse generator outputs are provided to trigger external events at preset times. The high-speed output unit can simultaneously perform software timer functions. Up to four 16-bit software timers can be in operation at once.

The on-chip A/D converter includes a Sample and Hold, and converts up to 4 multiplexed analog input channels to 10-bit digital values. With a 12 MHz crystal, each conversion takes 22 μs.

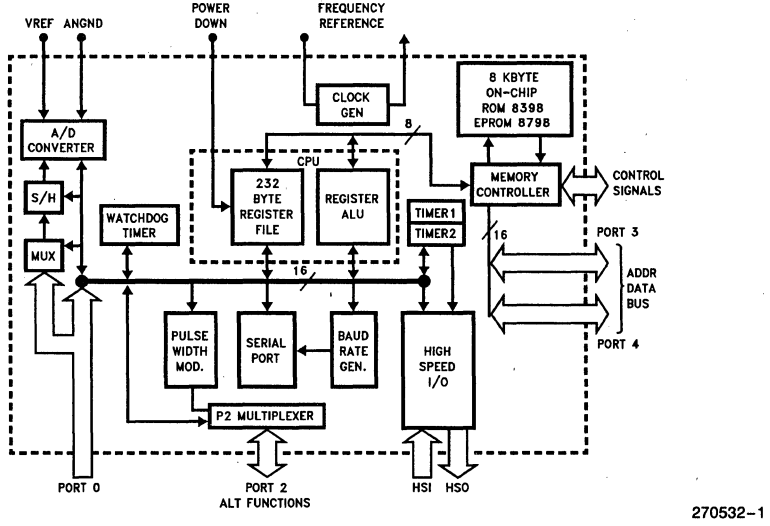


Figure 1. 8X98 Block Diagram

August 1992
Order Number: 270532-008

Also provided on-chip are a serial port, a Watchdog Timer and a pulse-width modulated output signal.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

With the extended burn-in option, the burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.5V, following the guidelines in MIL-STD-883, Method 1015.

See the Packaging information for extended temperature and extended burn-in designators.

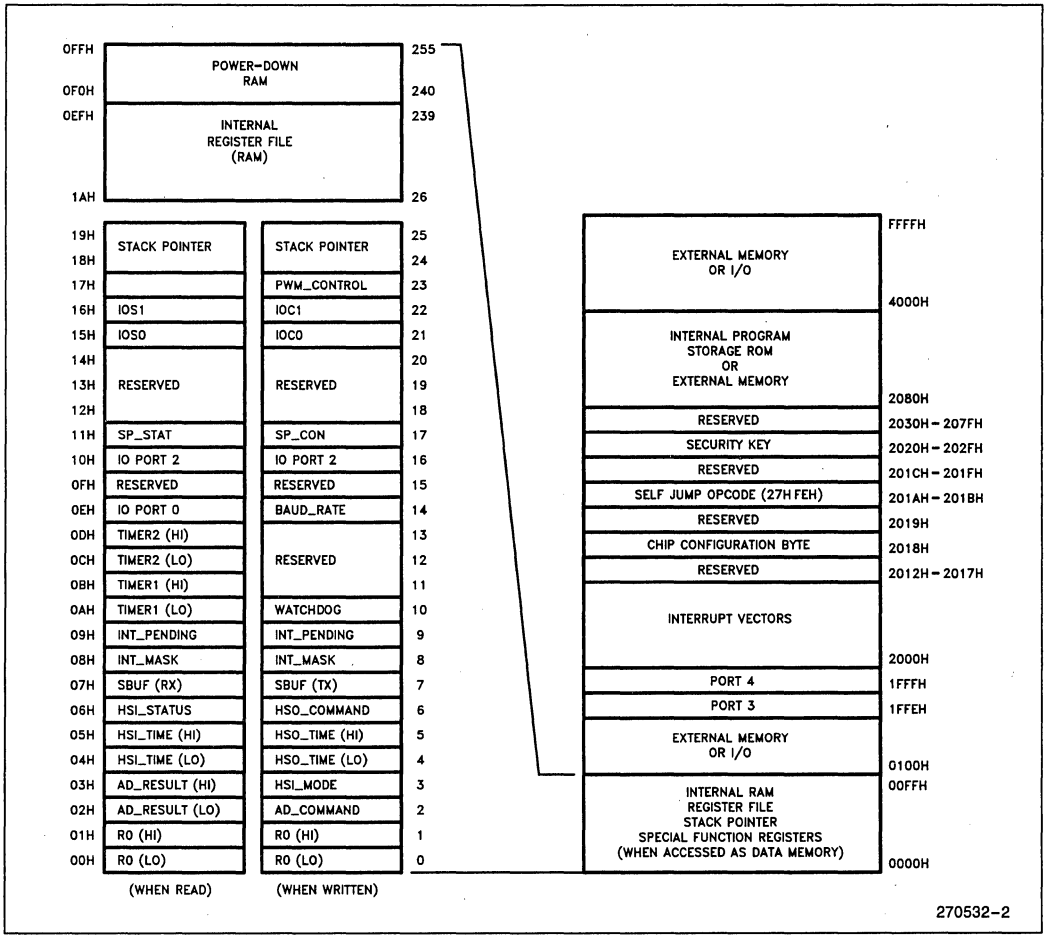


Figure 2. 8X98 Memory Map

15

PACKAGING

The 8098 is available in a 48-pin package with and without on-chip ROM or EPROM. The MCS-96 numbering system for the 8X98 devices is shown in Figure 4. Figure 6 shows the pinout for the 48-pin package. The 48-pin version is offered in a Dual-In-Line package.

Factory Masked ROM	CPU	User Programmable	
		EPROM	OTP
48-Pin	48-Pin	48-Pin	48-Pin
8398	8098	8798	8798

Figure 3. MCS®-96 Packaging—8098

Package Designators:
C = Ceramic DIP
P = Plastic DIP

Prefix Designators:
T = Extended Temperature
L = Extended Temperature with 160 Hours Burn-In

Package Type	θ_{ja}	θ_{jc}
48L Plastic DIP	38°C/W	19°C/W
48L Ceramic DIP	26°C/W	6.5°C/W

Figure 4. 8X98 Thermal Characteristics

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

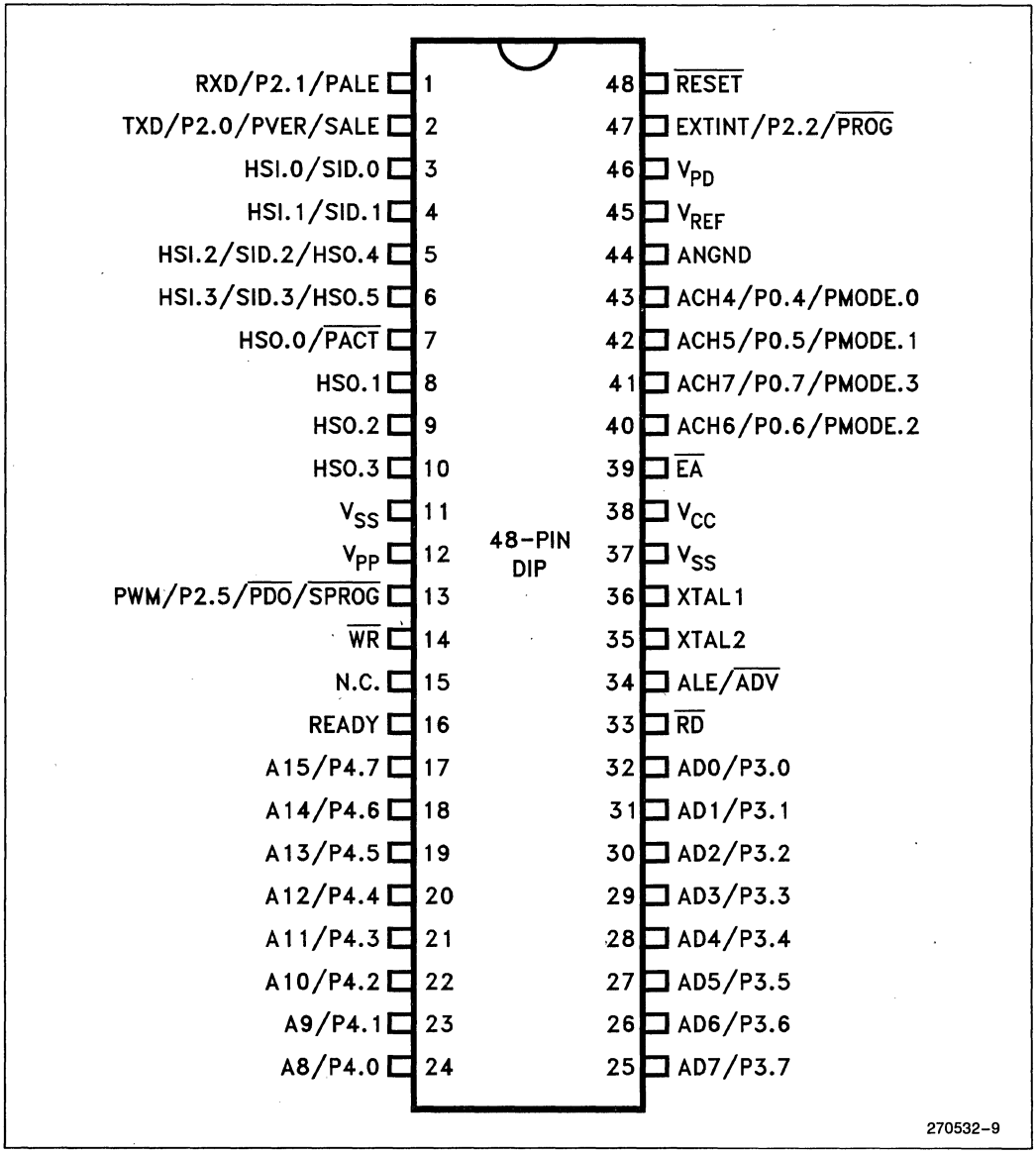


Figure 5. 48-Pin Package

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PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which must be connected.
V_{PD}	RAM standby supply voltage (5V). This voltage must be present during normal operation. In a Power Down condition (i.e. V_{CC} drops to zero), if $\overline{RESET}$ is activated before V_{CC} drops below spec and V_{PD} continues to be held within spec., the top 16 bytes in the Register File will retain their contents.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the EPROM devices. It should be 12.75V when programming and will float to 5V otherwise. The pin should not be above V_{CC} for ROM or CPU devices. This pin must float in the application circuit on EPROM devices.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
$\overline{RESET}$	Reset input to the chip. Input low for a minimum 10XTAL1 cycles to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ equal to +12.75V causes the device to enter the Programming Mode.
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$	Write output to external memory. $\overline{WR}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition of CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available in the CCR.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	4-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 2	4-bit multi-functional port. Its pins are shared with other functions in the 8098.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Ports 3 and 4 are also used as a command, address and data path by EPROM devices in the Programming Mode.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming Mode indicates that programming is in progress. A high signal indicates programming is complete.
PVAL	A low signal in Auto Programming Mode indicates that the device programmed correctly.
SALE	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (output from master).
$\overline{\text{SPROG}}$	A falling edge in Auto Programming Mode indicates that Ports 3 and 4 contain valid programming data (output from master).
SID	Assigns a pin of Ports 3 and 4 to each slave to pass programming verification.
PALE	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that Ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that Ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
PVAL	A high signal in Slave Programming Mode indicates the device programmed correctly.
$\overline{\text{PDO}}$	A low signal in Slave Programming Mode indicates that the PROG pulse was applied for longer than allowed.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias −55°C to +125°C

Storage Temperature .....−60°C to +150°C

Voltage from $\overline{EA}$ or V_{PP} to V_{SS} or ANGND .....−0.3V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND .....−0.3V to +7.0V(1)

Average Output Current from Any Pin .....10 mA

Power Dissipation(2) 1.5W

NOTES:
1. This includes V_{PP} on ROM and CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics specified in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	C
T_A	Ambient Temperature Under Bias **Extended** Temp.	−40	+85	C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	6.0	12	MHz
V_{PD}	Power-Down Supply Voltage	4.50	5.50	V

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current **Commercial** Temp.		240	mA	All Outputs Disconnected.
I_{CC}	V_{CC} Supply Current **Extended** Temp.		270	mA	
I_{CC}	V_{CC} Supply Current ($T_A \geq 70°C$)		185	mA	
I_{PD}	V_{PD} Supply Current		1	mA	Normal operation and Power-Down.
I_{REF}	V_{REF} Supply Current **Commercial** Temp.		8	mA	
I_{REF}	V_{REF} Supply Current **Extended** Temp.		10	mA	
V_{IL}	Input Low Voltage	−0.3	+0.8	V	

DC CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input High Voltage (Except $\overline{RESET}$, NMI, XTAL1)	2.0	$V_{CC}+0.5$	V	
V_{IH1}	Input High Voltage, $\overline{RESET}$ Rising	2.4	$V_{CC}+0.5$	V	
V_{IH2}	Input High Voltage, $\overline{RESET}$ Falling Hysteresis	2.1	$V_{CC}+0.5$	V	
V_{IH3}	Input High Voltage, NMI, XTAL1	2.2	$V_{CC}+0.5$	V	
I_{LI}	Input Leakage Current to each pin of HSI, P3, P4, and to P2.1.		± 10	μA	V_{in} = 0 to V_{CC}
I_{LI1}	DC Input Leakage Current to each pin of P0		+3	μA	V_{in} = 0 to V_{CC}
I_{IH}	Input High Current to $\overline{EA}$		100	μA	V_{IH} = 2.4V
I_{IL}	Input Low Current to each pin of P1 and to P2.6, P2.7 **Commercial** Temp.		−125	μA	V_{IL} = 0.45V
I_{IL}	Input Low Current to each pin of P1 and to P2.6, P2.7 **Extended** Temp.		−150	μA	
I_{IL1}	Input Low Current to $\overline{RESET}$	−0.25	−2	mA	V_{IL} = 0.45V
I_{IL2}	Input Low Current P2.2		−50	μA	V_{IL} = 0.45V
V_{OL}	Output Low Voltage on P3, P4 when used as ports		0.45	V	I_{OL} = 0.8 mA (Note 1)
V_{OL1}	Output Low Voltage on P3, P4 when used as ports		0.75	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OL2}	Output Low Voltage on Standard Output pins, $\overline{RESET}$ and Bus/Control Pins		0.45	V	I_{OL} = 2.0 mA (Notes 1, 2, 3)
V_{OH1}	Output High Voltage on Standard Output pins and Bus/Control pins	2.4		V	I_{OH} = −200 μA (Note 1)
I_{OH3}	Output High Current on $\overline{RESET}$	−50		μA	V_{OH} = 2.4V
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	F_{TEST} = 1.0 MHz

NOTES:
1. Standard Output Pins include TXD, RXD (Mode 0 only), PWM, and HSO pins. Bus/Control pins include ALE, $\overline{RD}$, $\overline{WR}$, AD0–AD7 and A8–A15.
2. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V.
   I_{OL} on Ports 3 and 4 when used as ports: 4.0 mA
   I_{OL} on standard output pins and $\overline{RESET}$: 8.0 mA
   I_{OL} on Bus/Control pins: 2.0 mA
3. During normal (non-transient) operation the following limits apply:
   Total I_{OL} on P2.0, $\overline{RESET}$ and all HSO pins must not exceed 15 mA.
   Total I_{OL} on Port 3 must not exceed 10 mA.
   Total I_{OL} on P2.5 and Port 4 must not exceed 20 mA.

AC CHARACTERISTICS Test Conditions: Load Capacitance on Output Pins = 80 pF

TIMING REQUIREMENTS (The system must meet these specifications to work with the 8X98.)

Symbol	Parameter	Min	Max	Units
T_{LLYV}	End of ALE/$\overline{ADV}$ to READY Valid		2 T_{OSC} − 70	ns
T_{LLYH}	End of ALE/$\overline{ADV}$ to READY High	2 T_{OSC} + 40	4 T_{OSC} − 80	ns
T_{YLYH}	Non-Ready Time		1000	ns
T_{AVDV}(1)	Address Valid to Input Data Valid		5 T_{OSC} − 120(2)	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		3 T_{OSC} − 100(2)	ns
T_{RHDX}	Data Hold after $\overline{RD}$ Inactive	0		ns
T_{RHDZ}	$\overline{RD}$ Inactive to Input Data Float	0	T_{OSC} − 25	ns

NOTE:
1. The term "Address Valid" applies to A0–A15.
2. If wait states are used, add 3 Tosc * N where N = number of states.

TIMING RESPONSES (8X98 devices meet these specs.)

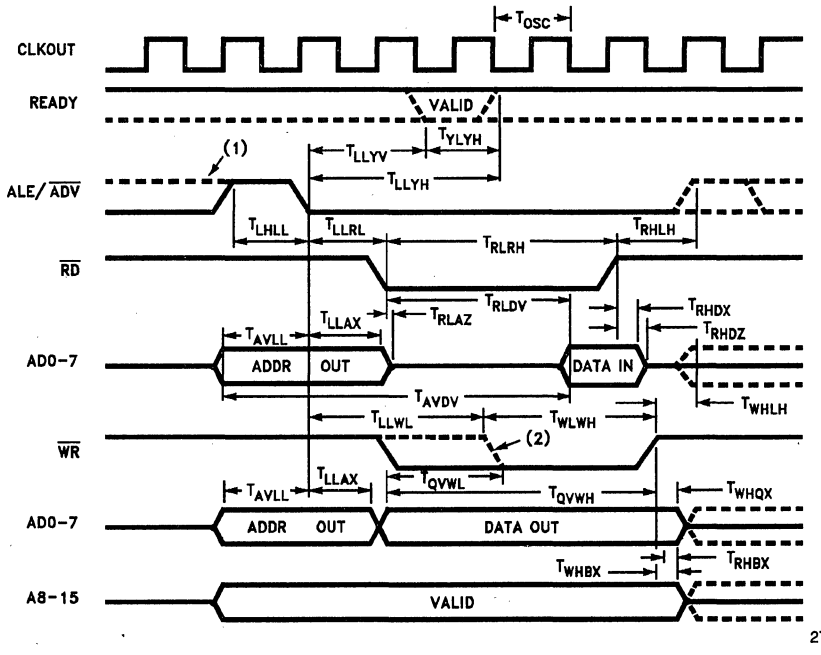
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	6.0	12.0	MHz
T_{OSC}	Oscillator Period	83	166	ns
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 30	T_{OSC} + 35(3)	ns
T_{AVLL}(4)	Address Setup to End of ALE/$\overline{ADV}$	T_{OSC} − 50		ns
T_{RLAZ}(5)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Commercial** Temp.	Typ. = 0	10	ns
T_{RLAZ}(5)	$\overline{RD}$ or $\overline{WR}$ Low to Address Float **Extended** Temp.		25	ns
T_{LLRL}	End of ALE/$\overline{ADV}$ to $\overline{RD}$ Active	T_{OSC} − 40		ns
T_{LLAX}(5)	Address Hold after End of ALE/$\overline{ADV}$	T_{OSC} − 40		ns
T_{WLWH}(6)	$\overline{WR}$ Pulse Width	3 T_{OSC} − 35(2)		ns
T_{WLWH}(7)	$\overline{WR}$ Pulse Width	2 T_{OSC} − 35(2)	2 T_{OSC} + 40	ns
T_{QVWH}	Output Data Valid to End of $\overline{WR}$	3 T_{OSC} − 60(2)		ns
T_{WHQX}	Output Data Hold after $\overline{WR}$	T_{OSC} − 50		ns
T_{WHLH}	End of $\overline{WR}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 75		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	3 T_{OSC} − 30(2)		ns

TIMING RESPONSES (8X98 devices meet these specs.) (Continued)

Symbol	Parameter	Min	Max	Units
T_{RHLH}	End of $\overline{RD}$ to ALE/$\overline{ADV}$ High	T_{OSC} − 45		ns
T_{RHBX}	$\overline{RD}$ High to A8–A15 Inactive	T_{OSC} − 25	T_{OSC} + 30	ns
T_{WHBX}	$\overline{WR}$ High to A8–A15 Inactive	T_{OSC} − 50	T_{OSC} + 100	ns
T_{LLWL}(6)	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	T_{OSC} − 40		ns
T_{LLWL}(7)	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	2 T_{OSC} − 30	2 T_{OSC} + 55	ns
T_{QVWL}(6)	Output Data Valid to $\overline{WR}$ Low	T_{OSC} − 60		ns
T_{QVWL}(7)	Output Data Valid to $\overline{WR}$ Low	T_{OSC} − 30		ns

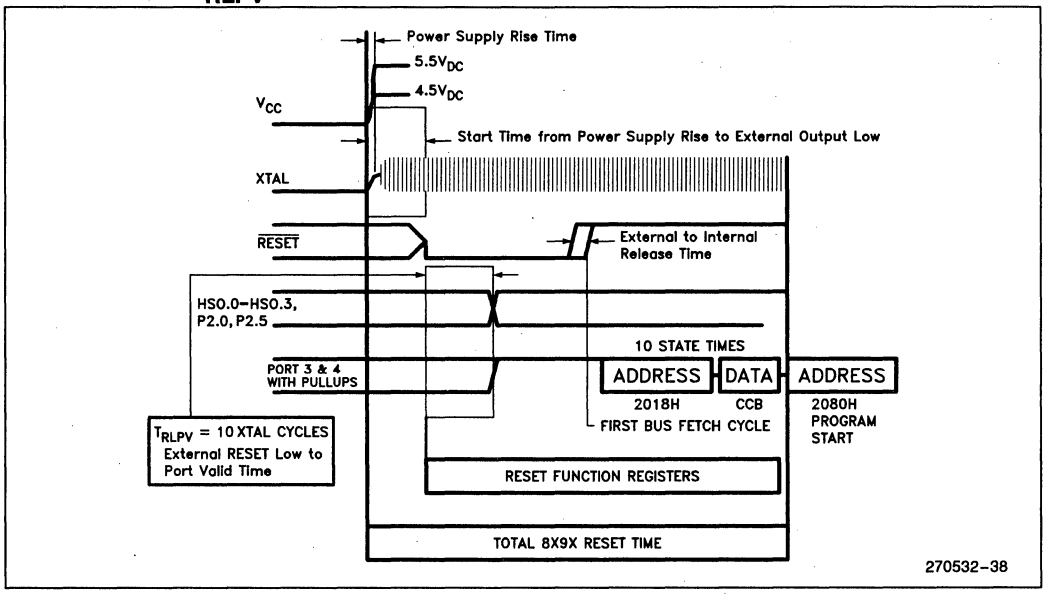
NOTES:
2. If more than one wait state is desired, add 3 Tosc for each additional wait state.
3. Max spec applies only to ALE. Min spec applies to both ALE and $\overline{ADV}$.
4. The term "Address Valid" applies to AD0–AD7, A8–A15.
5. The term "Address" in this definition applies to AD0–AD7.
6. Write Strobe Mode is not selected.
7. Write Strobe Mode is selected.

WAVEFORM—SYSTEM BUS TIMINGS



NOTES:
1. When $\overline{ADV}$ selected.
2. When Write Strobe Mode selected

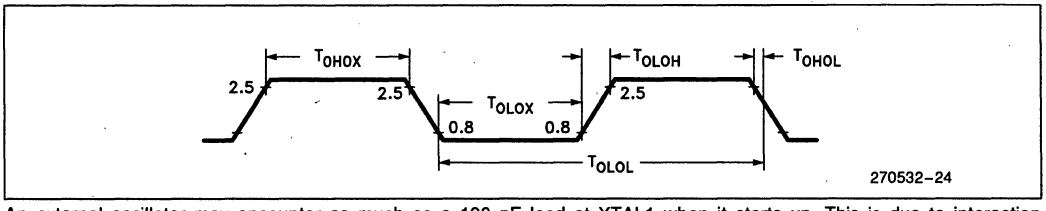
WAVEFORM—T_{RLPV}



EXTERNAL CLOCK DRIVE

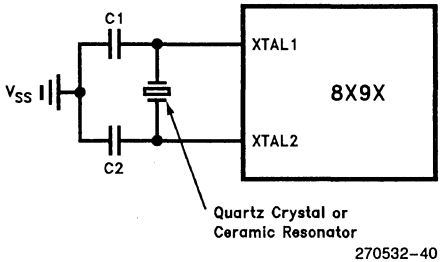
Symbol	Parameter	Min	Max	Units
$1/T_{OLOL}$	Oscillator Frequency	6	12	MHz
T_{OHOX}	High Time	25		ns
T_{OLOX}	Low Time	30		ns
T_{OLOH}	Rise Time		15	ns
T_{OHOL}	Fall Time		15	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

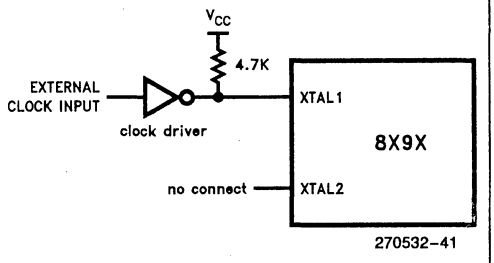
EXTERNAL CRYSTAL CONNECTIONS



270532-40

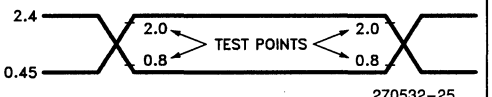
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 30 pF, C2 = 30 pF. When using ceramic resonators, consult manufacturer for recommended capacitor values.

EXTERNAL CLOCK CONNECTIONS



270532-41

AC TESTING INPUT, OUTPUT WAVEFORMS



270532-25

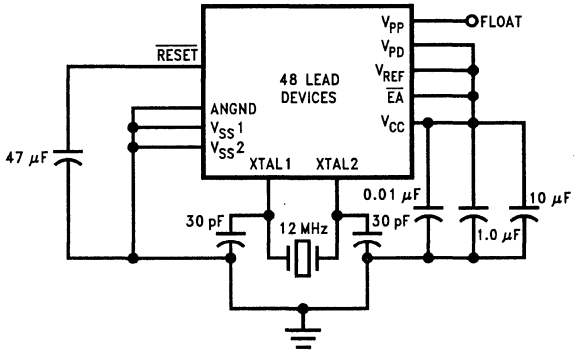
AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS

270532-26

For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs, and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 8$ mA.

MINIMUM HARDWARE CONFIGURATION CIRCUIT



270532-42

15

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

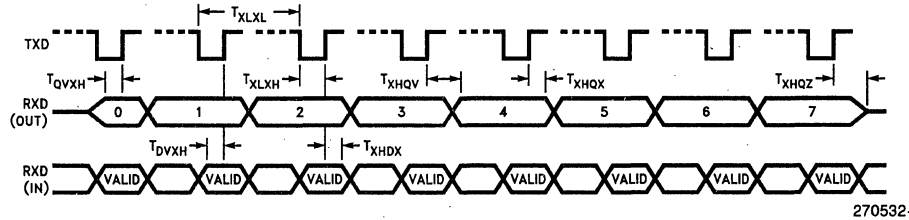
SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Load Capacitance = 80 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	2 T_{OSC} − 70		ns
T_{XHQV}	Next Output Data Valid After Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		5 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



270532-23

A/D CONVERTER SPECIFICATIONS

The absolute conversion accuracy is dependent on the accuracy and stability of V_{REF}.

See the MCS-96 A/D Converter Quick Reference for definition of A/D Converter Terms.

Parameter	Typical*(1)	Minimum	Maximum	Units**	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±4	LSBs	
Full Scale Error	−0.5 ±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±4	LSBs	
Differential Non-Linearity		> −1	+2	LSBs	
Channel-to-Channel Matching		0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 3
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Series Resistance		1K	5K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Delay		$3\,T_{OSC} - 50$	$3\,T_{OSC} + 50$	ns	2
Sample Time		$12\,T_{OSC} - 50$	$12\,T_{OSC} + 50$	ns	
Sampling Capacitor	2			pF	

NOTES:
* These values are expected for most parts at 25°C.
** An "LSB", as used here, is defined in the MCS-96 A/D Converter Quick Reference and has a value of approximately 5 mV.
1. DC to 100 KHz.
2. For starting the A/D with an HSO Command.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

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EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages during Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	9.0	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
$F_{OSC}1$	Oscillator Frequency during Auto and Slave Programming	6.0	6.0	MHz
$F_{OSC}2$	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

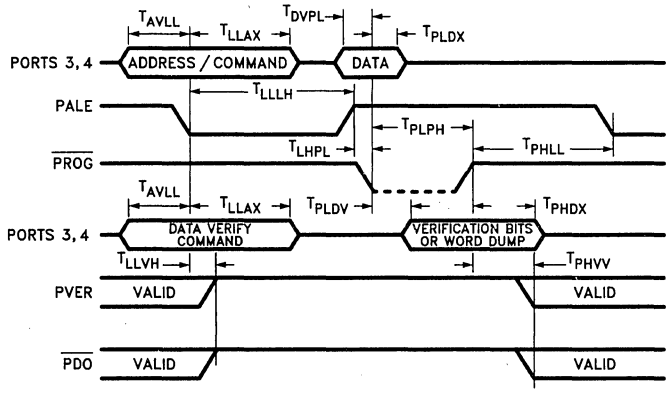
AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{AVLL}	ADDRESS/COMMAND Valid to PALE Low	0		T_{OSC}
T_{LLAX}	ADDRESS/COMMAND Hold After PALE Low	80		T_{OSC}
T_{DVPL}	Output Data Setup Before $\overline{PROG}$ Low	0		T_{OSC}
T_{PLDX}	Data Hold After $\overline{PROG}$ Falling	80		T_{OSC}
T_{LLLH}	PALE Pulse Width	180		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	250 T_{OSC}	100 μs + 144 T_{OSC}	
T_{LHPL}	PALE High to $\overline{PROG}$ Low	250		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next PALE Low	600		T_{OSC}
T_{PHDX}	Data Hold After $\overline{PROG}$ High	30		T_{OSC}
T_{PHVV}	$\overline{PROG}$ High to PVER/$\overline{PDO}$ Valid	500		T_{OSC}
T_{LLVH}	PALE Low to PVER/$\overline{PDO}$ High	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to VERIFICATION/DUMP Data Valid	100		T_{OSC}
T_{SHLL}	RESET High to First PALE Low (not shown)	2000		T_{OSC}

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (Whenever Programming)		100	mA

WAVEFORM—EPROM PROGRAMMING



270532-37

DIFFERENCES BETWEEN THE 8X9XBH AND 8X98

1. CCB.1 must be set to a logical 0 on the 8X98.
2. The following 8X9XBH pins and corresponding functions are not available on the 8X98:

   BUSWIDTH

   CLKOUT

   INST

   NMI

   Port 0.0–0.3 (ACH0–3)

   Port 1.0–1.7

   Port 2.6

   Port 2.7

   P2.3 (T2CLK)

   P2.4 (T2RST).

8X98 ERRATA

Devices covered by this data sheet (see Revision History) have the following errata.

1. INDEXED, 3 OPERAND MULTIPLY

The displacement portion of an indexed, three operand (byte or word) multiply may not be in the range of 200H thru 17FFH inclusive. If you must use these displacements, execute an indexed, two operand multiply and a move if necessary.

2. HSI FIFO OPERATION

The High Speed Input (HSI) has three deviations from the specifications. Note that "events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine states may be lost.

B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-tag value to be skipped every nine timer counts. Events may receive a time-tag one count later than expected.

C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into an **empty** FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within nine states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time-tags will be at least two counts apart.

3. RESERVED LOCATION 2019H

The 1990 Architectural Overview recommended that address 2019H be filled with hex value 0FFH. The recommendation is now 20H.

4. RESERVED LOCATION 201CH

Reading reserved location 201CH, either internally or externally, will return "201C" as data.

5. SERIAL PORT SECTION

Serial Port Flags—Reading SP_STAT may not clear the TI or RI flag if that flag was set within two state times prior to the read. In addition, the parity error bit (RPE/RB8) may not be correct if it is read within two state times after RI is set. Use the following code to replace ORB sp_image, SP_STAT.

```
SP_READ:  LDB  TEMP, SP_STAT
          ORB  SP_IMAGE, TEMP
          JBS  TEMP, 5, SP_READ; if
          TI is set then read again
          JBS  TEMP, 6; SP_READ; if
          RI is set then read again
          ANDB SP_IMAGE,#7FH; clear
          false RB8/RPE
          ORB  SP_IMAGE, TEMP; load
          correct RB8/RPE
```

DATA SHEET REVISION HISTORY

This data sheet (270532-008) is valid for devices with an "E" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The difference between -007 and -008 is the I_{OL}/I_{OH} for the float waveform testing changed from ±15 mA to ±8 mA.

The following differences exist between (-007) data sheet and the (-006).

1. The Express (extended temperature and burn-in options) were added to this data sheet. The 8X98 Express data sheet (270914-002) is now obsolete.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed. No specification changes were made.
3. Added Reserved Location 201CH errata.

The following differences exist between the -006 data sheet and the -005 data sheet.

1. The -005 data sheet was valid for devices marked with a "D" at the end of the top side tracking number.
2. The following errata were removed: RESET and the Quasi-Bidirectional Ports, Software RESET Timing, and Using T2CLK as the source for Timer2.
3. The HSI FIFO Operation errata definition was changed to match a change in the HSI FIFO operation.

The following differences exist between the -005 data sheet and the -004 data sheet.

1. Most of the functional description has been removed. This information is in the MCS-96 Architectural Overview.
2. Information on programming the Chip Configuration Register has been added.
3. T_{XHQX} changed from Min = 2 T_{OSC} − 50 ns to Min = 2 T_{OSC} − 70 ns.
4. T_{QLOX} changed from Min = 25 ns to Min = 30 ns.
5. Added AC timings specifications to clarify Write Strobe Mode specifications.
6. The differences between the 8X9XBH and the 8X98 have been added.
7. An errata has been added changing the recommendation for address 2019H from 0FFH to 20H.

Differences between the -004 and -003 data sheets.

1. All EPROM programming mode information has been moved to the Hardware Design Information Chapter.
2. CCB RESET FETCH and JBS/JBC on Port 0 anamolies have been corrected on the current steppings of the 8X98.
3. New information regarding T2CLK and new information about RESET of the Quasi Ports have been added to the Errata section.
4. The Extended Reset errata has been eliminated on the silicon and in the data sheet.
5. HSI Mode register is undefined until the user code initializes this register.
6. Minimum DNL us now > −1 LSB.
7. HSI FIFO overflow description added.

Differences between the -002 and -003 data sheets.

1. All 8798 EPROM information has been added as a complete section after the Analog Section.
2. The chip configuration byte values now indicate the use of WRITE STROBE with 8-bit systems. Write Strobe design text was added to the explanation.
3. The interrupt information now includes a worst case timing diagram.
4. The EPROM 8798 was added as necessary throughout the text.
5. NMI pin information was deleted.
6. Reset Register Status was added and the state of the HSO pins after RESET.
7. A diagram of the Interrupt Pending Register is now included.

8. A diagram of the PSW Register was added.
9. V_{IL1} was deleted. This was a RESET pin characteristic that has been improved to match the other characteristics.
10. The Differential Non-Linearity specification in the A/D converter specifications was corrected to read +2 LSBs.
11. Power On Reset — New information on Extended Reset Time was added to the Errata Section.

8XC196KB Data Sheets

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80C196KB10/83C196KB10/80C196KB12/83C196KB12 COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

83C196KB — 8 Kbytes of Factory Mask-Programmed ROM
80C196KB — ROMless

- 8 Kbytes of On-Chip ROM Available
- 232 Byte Register File
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- 2.3 μs 16 x 16 Multiply (12 MHz)
- 4.0 μs 32/16 Divide (12 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Extended Temperature Available
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- Pulse-Width-Modulated Output
- Four 16-Bit Software Timers
- 10-Bit A/D Converter with Sample/Hold
- $\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Bus Protocol
- 10 MHz and 12 MHz Available
- Extended Burn-In Available

The 80C196KB 16-bit microcontroller is a high performance member of the MCS®-96 microcontroller family. The 80C196KB is compatible with the 8096BH and uses a true superset of the 8096BH instructions. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

The 80C196KB has a 232-byte register file and an optional 8 Kbyte of on-chip ROM. Bit, byte, word and some 32-bit operations are available on the 80C196KB. With a 12 MHz oscillator a 16-bit addition takes 0.66 μs, and the instruction times average 0.5 μs to 1.5 μs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter. Also provided on-chip are an A/D converter, serial port, watchdog timer and a pulse-width-modulated output signal.

The 80C196KB10 and 83C196KB10 have a maximum guaranteed frequency of 10 MHz. The 80C196KB12 and 83C196KB12 have a maximum guaranteed frequency of 12 MHz. All references to the 80C196KB also refer to the 80C196KB10, 83C196KB10, 80C196KB12 and 83C196KB12 unless otherwise noted.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. With the extended burn-in option, the burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.5V, following the guidelines in MIL-STD-883, Method 1015. The specifications which are different for the extended temperature and extended burn-in devices are listed in this data sheet. Otherwise, the commercial specifications apply for both.

November 1991
Order Number: 270918-002

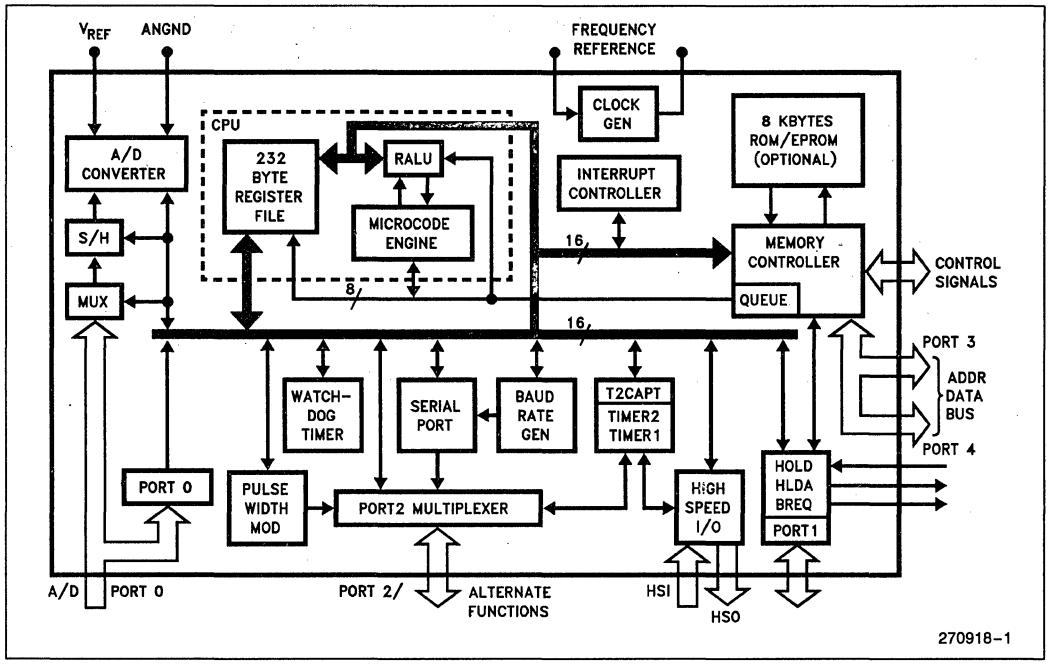

Figure 1. 80C196KB Block Diagram

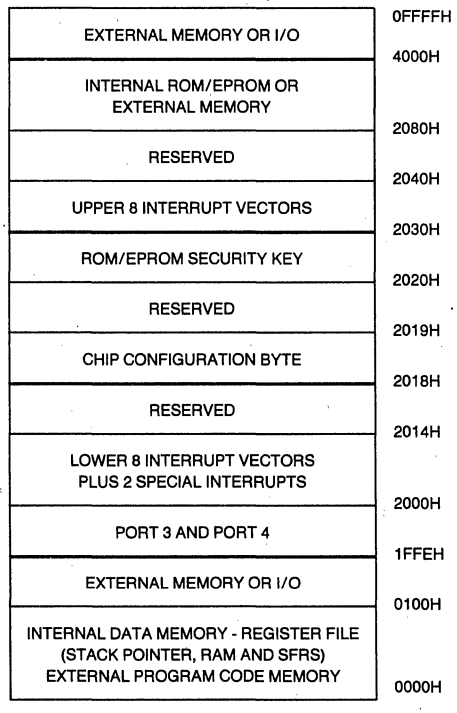

Figure 2. Memory Map

PACKAGING

The 80C196KB is available in a 68-pin PLCC package, an 80-pin QFP package and a 68-pin PGA package. Contact your local sales office to determine the exact ordering code for the part desired.

Package Designators: N = 68-pin PLCC, S = 80-pin QFP and A = 68-pin PGA.

Prefix Designators: T = extended temperature, L = extended temperature with extended burn-in.

Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PGA	28°C/W	3.5°C/W
PLCC	35°C/W	12°C/W
QFP	85°C/W	—

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

PGA	PLCC	Description	PGA	PLCC	Description	PGA	PLCC	Description
1	9	ACH7/P0.7	24	54	AD6/P3.6	47	31	P1.6/$\overline{\text{HLDA}}$
2	8	ACH6/P0.6	25	53	AD7/P3.7	48	30	P1.5/$\overline{\text{BREQ}}$
3	7	ACH2/P0.2	26	52	AD8/P4.0	49	29	HSO.1
4	6	ACH0/P0.0	27	51	AD9/P4.1	50	28	HSO.0
5	5	ACH1/P0.1	28	50	AD10/P4.2	51	27	HSO.5/HSI.3
6	4	ACH3/P0.3	29	49	AD11/P4.3	52	26	HSO.4/HSI.2
7	3	NMI	30	48	AD12/P4.4	53	25	HSI.1
8	2	$\overline{\text{EA}}$	31	47	AD13/P4.5	54	24	HSI.0
9	1	V_{CC}	32	46	AD14/P4.6	55	23	P1.4
10	68	V_{SS}	33	45	AD15/P4.7	56	22	P1.3
11	67	XTAL1	34	44	T2CLK/P2.3	57	21	P1.2
12	66	XTAL2	35	43	READY	58	20	P1.1
13	65	CLKOUT	36	42	T2RST/P2.4	59	19	P1.0
14	64	BUSWIDTH	37	41	$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	60	18	TXD/P2.0
15	63	INST	38	40	$\overline{\text{WR}}$/$\overline{\text{WRL}}$	61	17	RXD/P2.1
16	62	ALE/$\overline{\text{ADV}}$	39	39	PWM/P2.5	62	16	$\overline{\text{RESET}}$
17	61	$\overline{\text{RD}}$	40	38	P2.7/T2CAPTURE	63	15	EXTINT/P2.2
18	60	AD0/P3.0	41	37	V_{PP}	64	14	V_{SS}(1)
19	59	AD1/P3.1	42	36	V_{SS}	65	13	V_{REF}
20	58	AD2/P3.2	43	35	HSO.3/SID3	66	12	ANGND
21	57	AD3/P3.3	44	34	HSO.2/SID2	67	11	ACH4/P0.4
22	56	AD4/P3.4	45	33	P2.6/T2UP-DN	68	10	ACH5/P0.5
23	55	AD5/P3.5	46	32	P1.7/$\overline{\text{HOLD}}$			

NOTE:
1. This pin was formerly the Clock Detect Enable pin. This function is not guaranteed to work. This pin must be directly connected to V_{SS}.

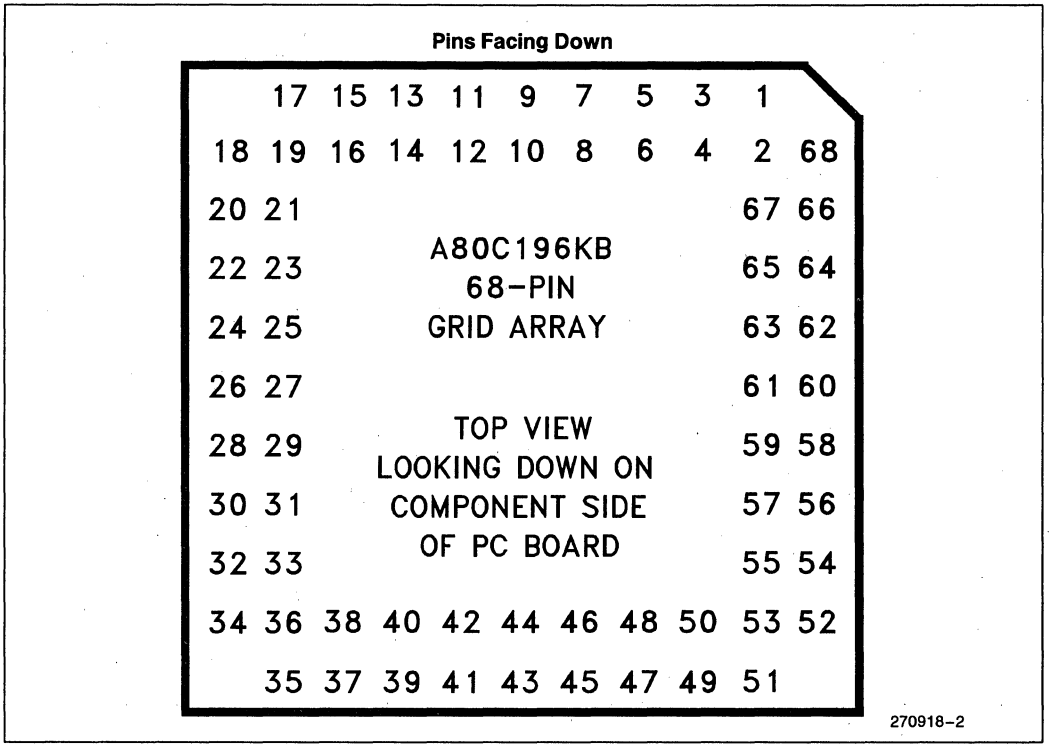

Figure 3. 68-Pin Package (Pin Grid Array—Top View)

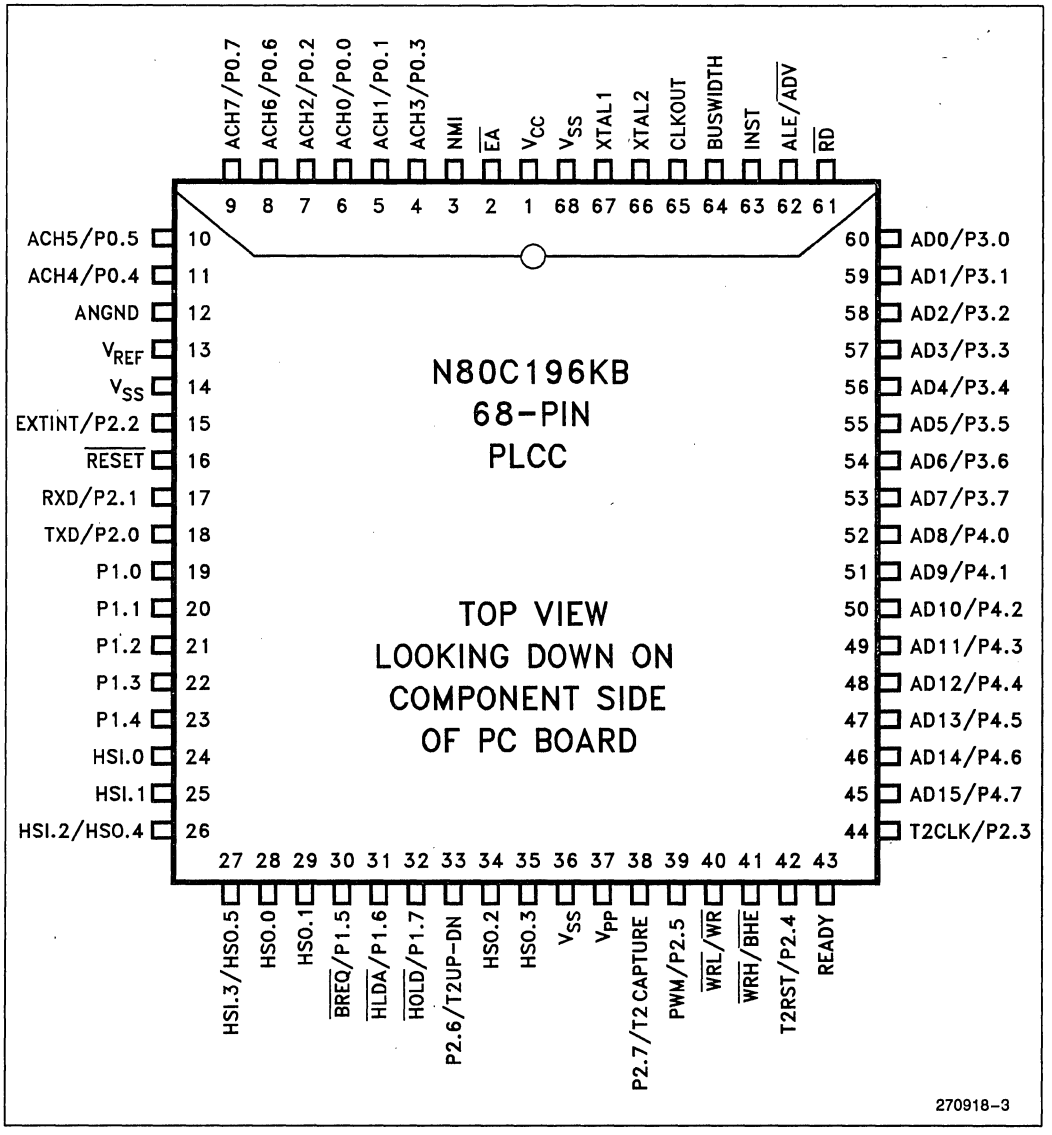

Figure 4. 68-Pin Package (PLCC—Top View)

16

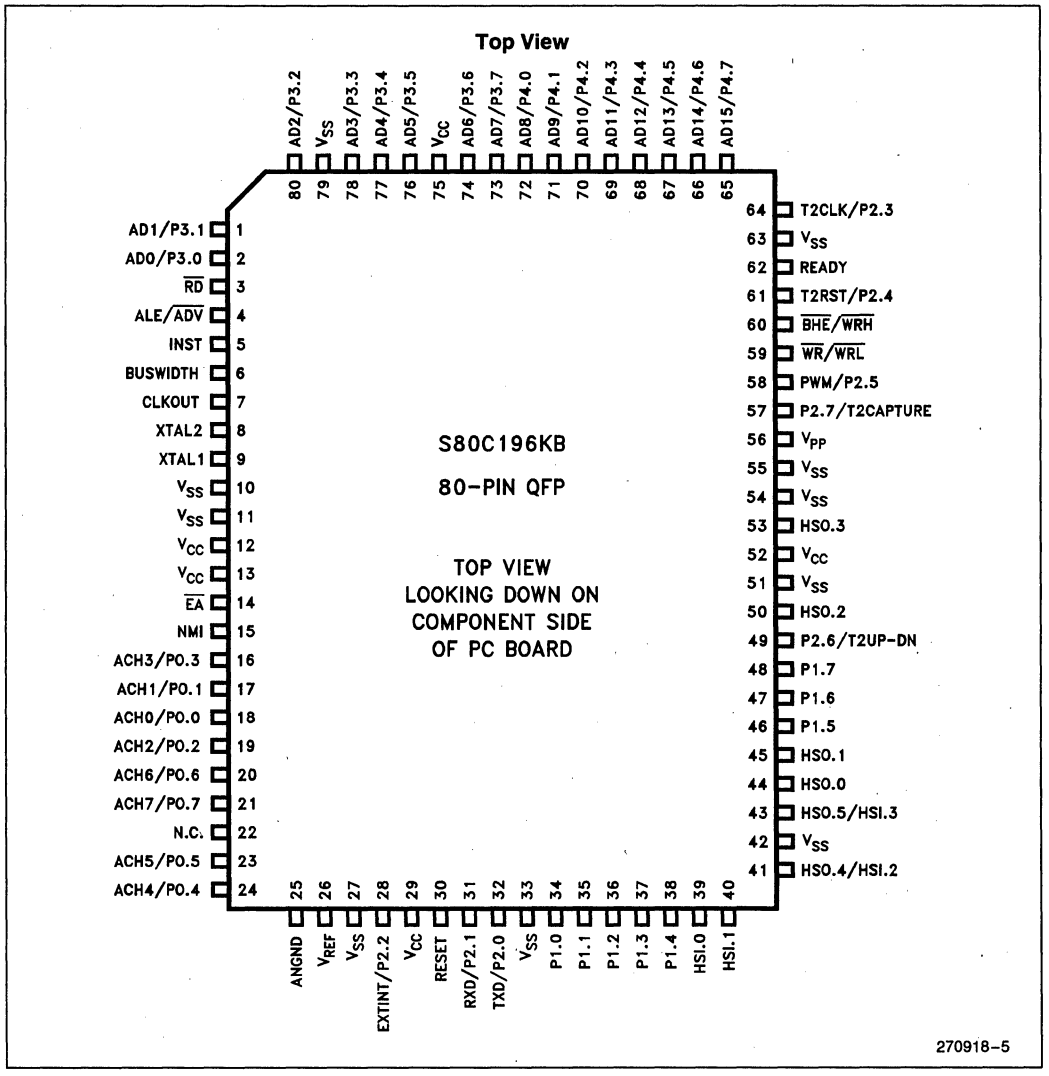

Figure 5. 80-Pin Quad Flat Pack (QFP)

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS}. If this function is not used, connect to V_{CC}. This pin is the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input and open-drain output. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition re- synchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{\text{EA}}$ must be tied low for the 80C196KB ROMless device.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{\text{BHE}}$ = 1), to the high byte only (A0 = 1, $\overline{\text{BHE}}$ = 0), or both bytes (A0 = 0, $\overline{\text{BHE}}$ = 0). If the $\overline{\text{WRH}}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available through configuration of CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit. The HSI pins are also used as the SID in Slave Programming Mode on the EPROM device.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins set the Programming Mode on the EPROM device.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 80C196KB.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Available as I/O only on the ROM and EPROM devices.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus. Enabled by setting WSR.7.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. The TxD function is enabled by setting IOC1 5. In mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. The RxD function is enabled by setting SPCON.3. In mode 0 the pin functions as input or output data.
EXTINT	A rising edge on the EXTINT pin will generate an external interrupt. EXTINT is selected as the external interrupt source by setting IOC1.1 high.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2. The external reset function is enabled by setting IOCO.03 T2RST is enabled as the reset source by clearing IOCO.5.
PWM	Port 2.5 can be enabled as a PWM output by setting IOC1.O The duty cycle of the PWM is determined by the value loaded into the PWM-CONTROL register (17H).
T2UP-DN	The T2UP-DN pin controls the direction of Timer2 as an up or down counter. The Timer2 up/down function is enabled by setting IOC2.1.
T2CAP	A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register (location 0CH in Window 15).

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS} ..... −0.5V to +7.0V
Power Dissipation(1) 1.5W

NOTE:
1. Power Dissipation is based on package heat transfer, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency **12 MHz**	3.5	12	MHz
F_{OSC}	Oscillator Frequency **10 MHz**	3.5	10	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Description	Min	Typ(7)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −10 µA I_{OH} = −30 µA I_{OH} = −60 µA

NOTES:
1. All pins except RESET and XTAL1.
2. Holding these pins below V_{IH} in Reset may cause the part to enter test modes.

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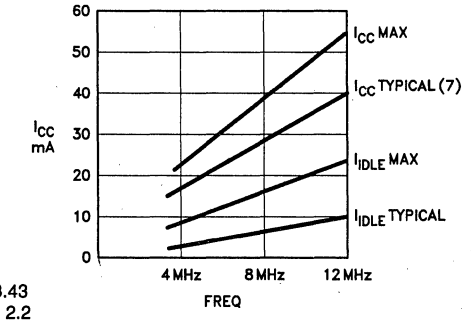
DC CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ(7)	Max	Units	Test Conditions
I_{LI}	Input Leakage Current (Std. Inputs)			±10	µA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			+3	µA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	µA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)			−50	µA	$V_{IN} = 0.45V$
I_{IL1}	Logical 0 Input Current in Reset (Note 2) (ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, INST, P2.0)			−1.2	mA	$V_{IN} = 0.45$ V
Hyst	Hysteresis on RESET Pin	300			mV	
I_{CC}	Active Mode Current in Reset		40	55	mA	XTAL1 = 12 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Converter Reference Current		2	5	mA	
I_{IDLE}	Idle Mode Current		10	22	mA	
I_{CC1}	Active Mode Current		15	22	mA	XTAL1 = 3.5 MHz
I_{PD}	Powerdown Mode Current		5	50	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:
(Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, CDE, $\overline{EA}$, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.



I_{CC} Max = 3.88 × FREQ + 8.43
I_{IDLE} Max = 1.65 × FREQ + 2.2

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Figure 6. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 10/12 MHz

The system must meet these specifications to work with the 80C196KB:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup 80C196KB10/83C196KB10 80C196KB12/83C196KB12		 $2T_{OSC} - 90$ $2T_{OSC} - 85$	 ns ns	
T_{LLYV}	ALE Low to READY Setup 80C196KB10/83C196KB10 80C196KB12/83C196KB12		 $T_{OSC} - 80$ $T_{OSC} - 72$	 ns ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 85$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 70$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid 80C196KB10/83C196KB10 80C196KB12/83C196KB12		 $3T_{OSC} - 70$ $3T_{OSC} - 67$	 ns ns	 (Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid 80C196KB10/83C196KB10 80C196KB12/83C196KB12		 $T_{OSC} - 30$ $T_{OSC} - 23$	 ns ns	 (Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. When using wait states, add $2T_{OSC} \times n$, where n = number of wait states.

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AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 10/12 MHz

The 80C196KB will meet these specifications:

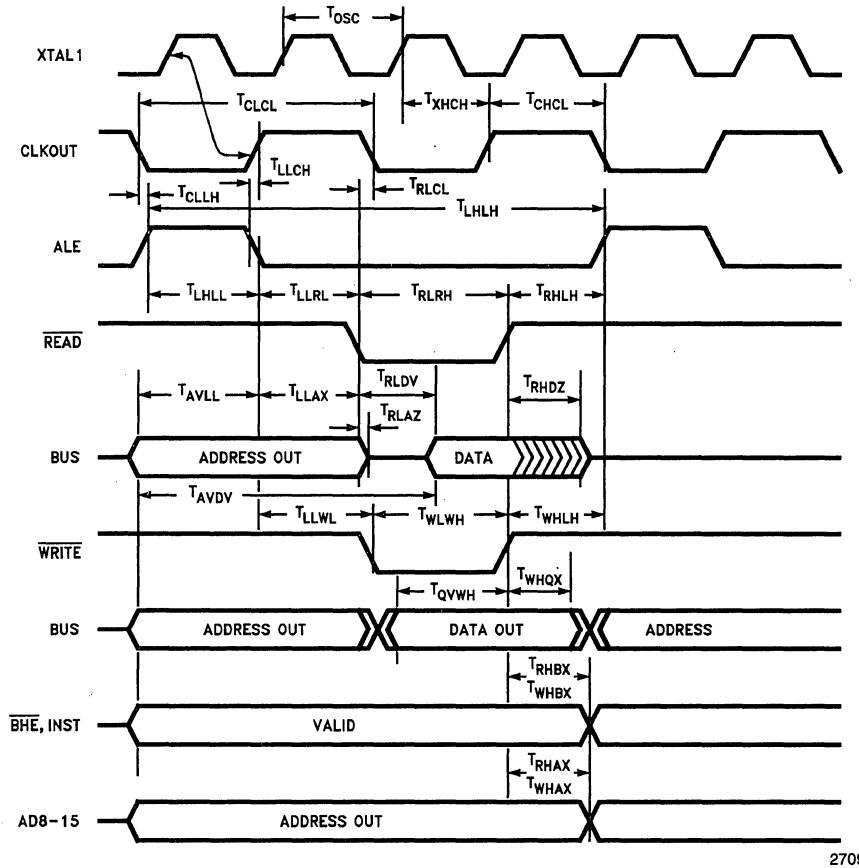
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on $XTAL_1$				
	80C196KB10/83C196KB10	3.5	10	MHz	(Note 2)
	80C196KB12/83C196KB12	3.5	12	MHz	(Note 2)
T_{OSC}	$1/F_{XTAL}$				
	80C196KB10/83C196KB10	100	286	ns	
	80C196KB12/83C196KB12	83	286	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	40	110	ns	(Note 3)
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC}+10	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 5)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC}+10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 20			
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 40		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	5	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	(Note 5)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 4)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		10	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge				
	80C196KB10/83C196KB10	T_{OSC} − 30		ns	(Note 5)
	80C196KB12/83C196KB12	T_{OSC} − 23		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	10	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30	T_{OSC} + 5	ns	(Note 5)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	(Note 4)
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 10		ns	
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 50		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	T_{OSC} − 25		ns	

NOTES:

T_{OSC} = 83.3 ns at 12 MHz; T_{OSC} = 100 ns at 10 MHz.

1. Customers whose applications require an 83C196KB to meet the 80C196KB specifications listed above should contact an Intel Field Sales Representative.
2. Testing performed at 3.5 MHz. However, the part is static by design and will typically operate below 1 Hz.
3. Typical specification, not guaranteed.
4. Assuming back-to-back bus cycles.
5. When using wait states, add 2 T_{OSC} × n, where n = number of wait states.

System Bus Timings



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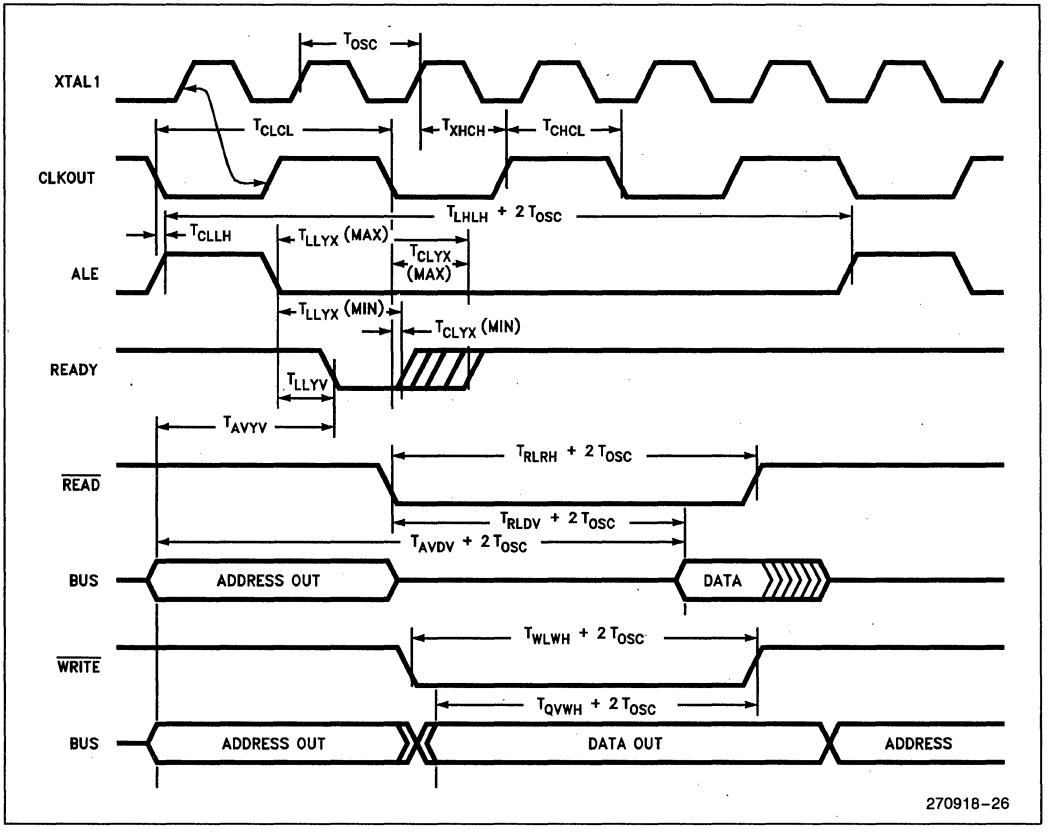
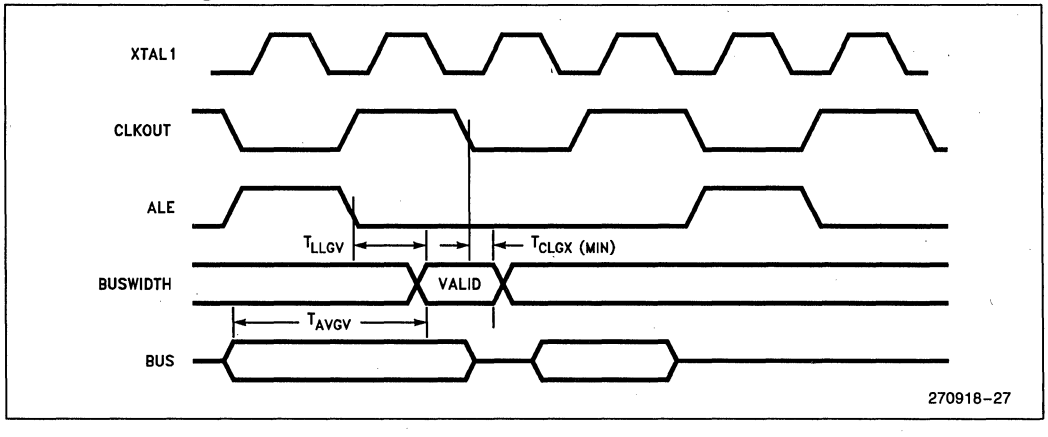
READY Timings (One Wait State)



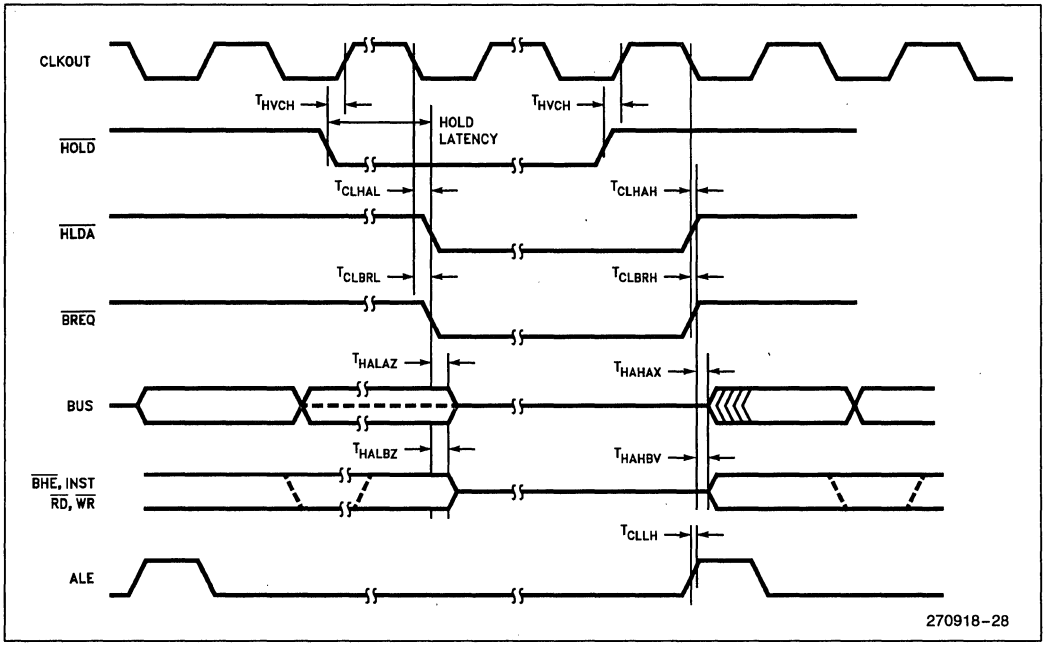
Buswidth Timings



HOLD/HLDA TIMINGS

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	$\overline{HOLD}$ Setup	85		ns	1
T_{CLHAL}	CLKOUT Low to $\overline{HLDA}$ Low	−15	15	ns	
T_{CLBRL}	CLKOUT Low to $\overline{BREQ}$ Low	−15	15	ns	
T_{HALAZ}	$\overline{HLDA}$ Low to Address Float		20	ns	
T_{HALBZ}	$\overline{HLDA}$ Low to BHE, INST, RD, WR Float			ns	
T_{CLHAH}	CLKOUT Low to $\overline{HLDA}$ High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to $\overline{BREQ}$ High	−15	15	ns	
T_{HAHAX}	$\overline{HLDA}$ High to Address No Longer Float	−5		ns	
T_{HAHBV}	$\overline{HLDA}$ High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−20		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

NOTE:
1. To guarantee recognition at next clock.



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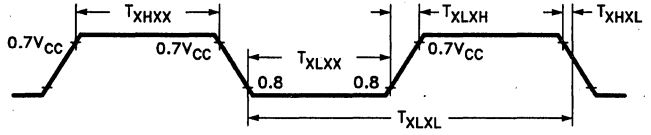
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency			
	80C196KB10	3.5	10.0	MHz
	80C196KB12	3.5	12.0	MHz
T_{XLXL}	Oscillator Frequency			
	80C196KB10	100	286	ns
	80C196KB12	83	286	ns
T_{XHXX}	High Time	32		ns
T_{XLXX}	Low Time	32		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



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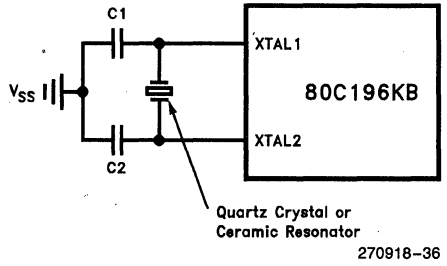
An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

EXTERNAL CRYSTAL CONNECTIONS



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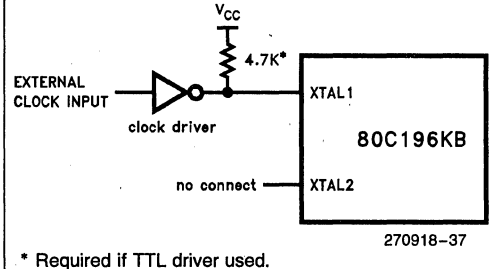
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = C2 ≈ 20 pF. When using ceramic resonators, consult manufacturer for recommended capacitor values.

EXTERNAL CLOCK CONNECTIONS



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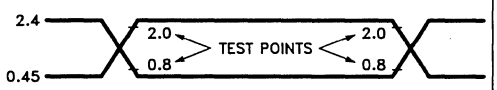
* Required if TTL driver used.
Not needed if CMOS driver is used.

AC TESTING INPUT, OUTPUT WAVEFORMS



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AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS

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For Timing Purposes a Port Pin is no Longer Floating when a 150 mV change from Load Voltage Occurs and Begins to Float when a 150 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H - High
L - Low
V - Valid
X - No Longer Valid
Z - Floating

Signals:

A - Address
B - $\overline{BHE}$
BR - $\overline{BREQ}$
C - CLKOUT
D - DATA IN
G - Buswidth
H - $\overline{HOLD}$
HA - $\overline{HLDA}$
L - ALE/$\overline{ADV}$
Q - DATA OUT
R - $\overline{RD}$
W - $\overline{WR}/\overline{WRH}/\overline{WRL}$
X - XTAL1
Y - READY

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} −50	4 T_{OSC} +50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} +50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} +50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

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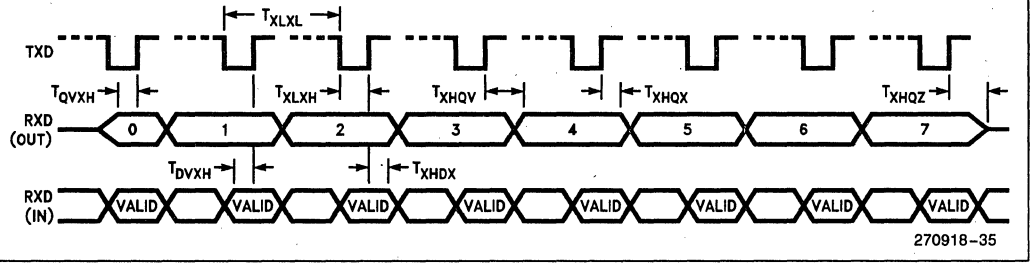
WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



A TO D CHARACTERISTICS

There are two modes of A/D operation: with or without clock prescaler. The speed of the A/D converter can be adjusted by setting a clock prescaler on or off. At high frequencies more time is needed for the comparator to settle. The maximum frequency with the clock prescaler disabled is 8 MHz. The conversion times with the prescaler turned on or off is shown in the table below.

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

See the MCS-96 A/D Quick Reference for definition of A/D terms.

Conversion Time

Clock Prescaler On IOC2.4 = 0	Clock Prescaler Off IOC2.4 = 1
158 States 26.33 μs @ 12 MHz	91 States 22.75 μs @ 8 MHz

A/D CONVERTER SPECIFICATIONS

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		512 9	1024 10	Levels Bits	
Absolute Error		0	±4	LSBs	
Full Scale Error	0.25 ±0.50			LSBs	
Zero Offset Error	−0.25 ±0.50			LSBs	
Non-Linearity Error	1.5 ±2.5	0	±4	LSBs	
Differential Non-Linearity Error		>−1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		1K	5K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Time: Prescaler On Prescaler Off	15 8			States States	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

EXTENDED TEMPERATURE/EXTENDED BURN-IN ONLY SPECIFICATIONS

Symbols	Description	Min	Max	Units
RESET Hysteresis	Hysteresis on RESET Pin	TBD		mV
I_{PD}	Powerdown Mode Current		TBD	mA
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 65$	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns
T_{AVDV}	Address Valid to Input Data Valid		$3\,T_{OSC} - 60$	ns
T_{RLDV}	$\overline{RD}$ Low to Input Data Valid		$T_{OSC} - 25$	ns
T_{LHLL}	ALE High Period	$T_{OSC} - 12$	$T_{OSC} + 12$	ns
T_{RHAX}	AD_8–AD_{15} Hold after $\overline{RD}$ Rising	$T_{OSC} - 50$		ns
T_{HALAZ}	$\overline{HLDA}$ Low to Address Float		−25	ns
T_{HALBZ}	$\overline{HLDA}$ Low to $\overline{BHE}$, INST, RD, $\overline{WR}$ Float		−30	ns
T_{HAHBV}	$\overline{HLDA}$ High to $\overline{BHE}$, INST, RD, $\overline{WR}$ Valid	−25		ns
A/D Absolute Error	Absolute Error		±6	LSBs

FUNCTIONAL DEVIATIONS

1. The DJNZW instruction is not guaranteed to be functional. The instruction, if encountered, will not cause an unimplemented opcode interrupt. (The opcode for DJNZW is 0E1 Hex.) The DJNZ (byte) instruction works correctly and should be used instead.
2. The CDE function is not guaranteed to work. The CDE pin must be directly connected to V_{SS}.
3. The HSI unit has two errata: one dealing with resolution and the other with first entries into the FIFO.

   The HSI resolution is 9 states instead of 8 states. Events on the same line may be lost if they occur faster than once every 9 state times.

   There is a mismatch between the 9 state time HSI resolution and the 8 state time timer. This causes one time value to be unused every 9 timer counts. Events may receive a time-tag one count later than expected because of this "skipped" time value.

   If the first two events into an empty FIFO (not including the Holding Register) occur in the same internal phase, both are recorded with one time-tag. Otherwise, if the second event occurs within 9 states after the first, its time-tag is one count later than the first's. If this is the "skipped" time value, the second event's time-tag is 2 counts later than the first's.

   If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register after 8 state times, leaving the FIFO empty again. If the second event occurs after this time, it will act as a new first event into an empty FIFO.
4. The serial port Framing Error flag fails to indicate an error if the bit preceding the stop bit is a 1. This is the case in both the 8-bit and 9-bit modes. False framing errors are never generated.
5. The serial port RI flag is not generated after the first byte is received. The problem does not occur if the baud rate is reloaded after each reception.
6. If the unsigned divide instruction (byte or word) is the last instruction in the queue as HOLD or READY is asserted, the result may be incorrect.

DATA SHEET REVISION HISTORY

This data sheet (270918-002) is valid for devices marked with a "B" at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet and the previous version (-001).

1. The commercial and Express (extended temperature and extended burn-in) devices were combined in this data sheet. The Express only data sheet (270780-002) is now obsolete.
2. The EPROM devices were removed from this data sheet. They are now in a separate data sheet (270909).
3. The 80C196KB devices were removed from this data sheet. Only the 80C196KB10, 83C196KB10, 80C196KB12 and 83C196KB12 devices are now covered.
4. Changes were made to the format of the data sheet and the SFR descriptions were removed.
5. Two errata were added: the serial port RI flag and the DIVIDE during HOLD/READY.
6. Three specifications for the extended temperature and extended burn-in devices were changed: V_{IH2} Min was changed from 2.4V to 2.6V, T_{XHCH} Min was changed from 35 ns to 40 ns, and T_{HVCH} Min was changed from 90 ns to 85 ns.

The -001 data sheet integrated the 87C196KB (order number 270590-003) and the 83C196KB/80C196KB (order number 270634-003) data sheets. The following differences exist between the -001 data sheet and each of the above mentioned data sheets.

1. The status of the data sheet was upgraded from ADVANCE INFORMATION to PRELIMINARY.
2. The warning about the ABSOLUTE MAXIMUM RATINGS was reworded and a notice of disclaimer was added to the electrical specifications section.
3. V_{IH2} was increased from 2.2V to 2.6V.
4. I_{IL1} was increased from $-950\ \mu A$ to -1.2 mA. This change was documented in the previous revision of the data sheets but the DC Characteristics table did not reflect the change.
5. Maximum I_{PD} specification was added to the DC table and I_{PD} note was deleted.

80C198/83C198/80C194/83C194 COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

83C198 — 8 Kbytes of Factory Mask-Programmed ROM
80C198 — ROMless

- **232 Byte Register File**
- **Register-to-Register Architecture**
- **28 Interrupt Sources/16 Vectors**
- **2.3 μs 16 x 16 Multiply (12 MHz)**
- **4.0 μs 32/16 Divide (12 MHz)**
- **Powerdown and Idle Modes**
- **16-Bit Watchdog Timer**
- **8-Bit External Bus**
- **Extended Temperature Available**
- **Full Duplex Serial Port**
- **High Speed I/O Subsystem**
- **16-Bit Timer**
- **16-Bit Counter**
- **Pulse-Width-Modulated Output**
- **Four 16-Bit Software Timers**
- **10-Bit A/D Converter with Sample/Hold**
- **Extended Burn-In Available**

The 80C198 is the low cost member of the CHMOS MCS®-96 microcontroller family. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

The 83C198 is an 80C198 with 8 Kbytes on-chip ROM. In this document, the 80C198 will also refer to the 83C198, 80C194 and 83C194 unless otherwise stated. Bit, byte, word and some 32-bit operations are available on the 80C198. With a 12 MHz oscillator a 16-bit addition takes 0.66 μs, and the instruction times average 0.5 μs to 1.5 μs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or counter. Also provided on-chip are an A/D converter, serial port, watchdog timer and a pulse-width-modulated output signal.

The 80C194 and 83C194 do not have the on-chip A/D converter.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. With the extended burn-in option, the burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.5V, following the guidelines in MIL-STD-883, Method 1015. The specifications which are different for the extended temperature and extended burn-in devices are listed in this data sheet. Otherwise, the commercial specifications apply for both.

MCS®-96 is a registered trademark of Intel Corporation.

October 1991
Order Number: 270815-003

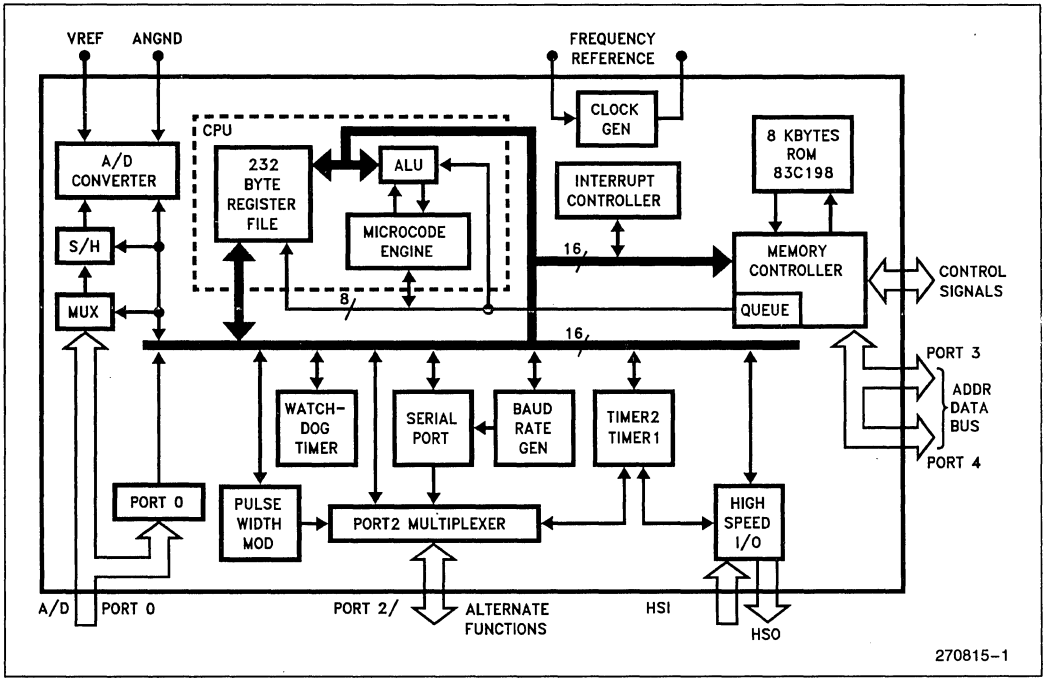


Figure 1. 80C198/80C198 Block Diagram

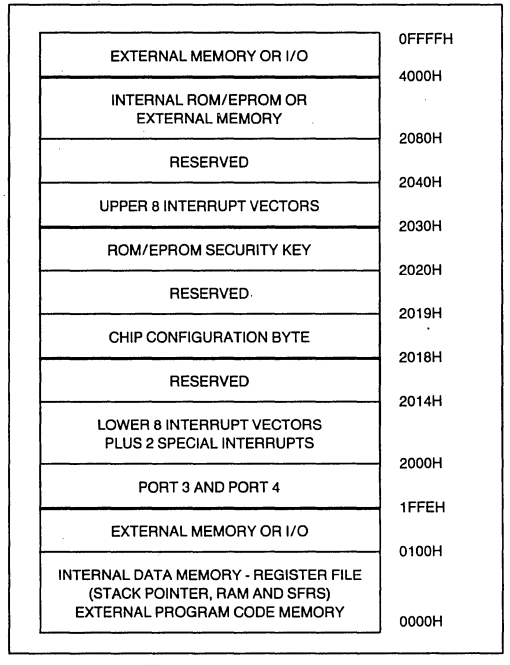


Figure 2. Memory Map

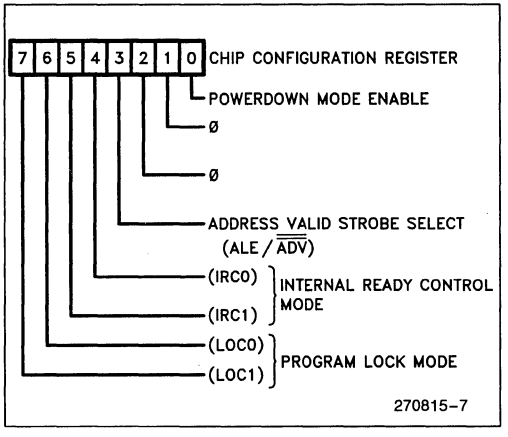


Figure 3. Chip Configuration (2018H)

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PACKAGING

The 80C198 and 83C198 are available in a 52-pin PLCC package and an 80-pin QFP package. Contact your local sales office to determine the exact ordering code for the part desired.

Package Designators:
N = 52-pin PLCC
S = 80-pin QFP

Prefix Designators:
T = Extended temperature
L = Extended temperature and extended burn-in

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	12°C/W
QFP	85°C/W	—

Figure 4. 8XC198 Thermal Characteristics

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

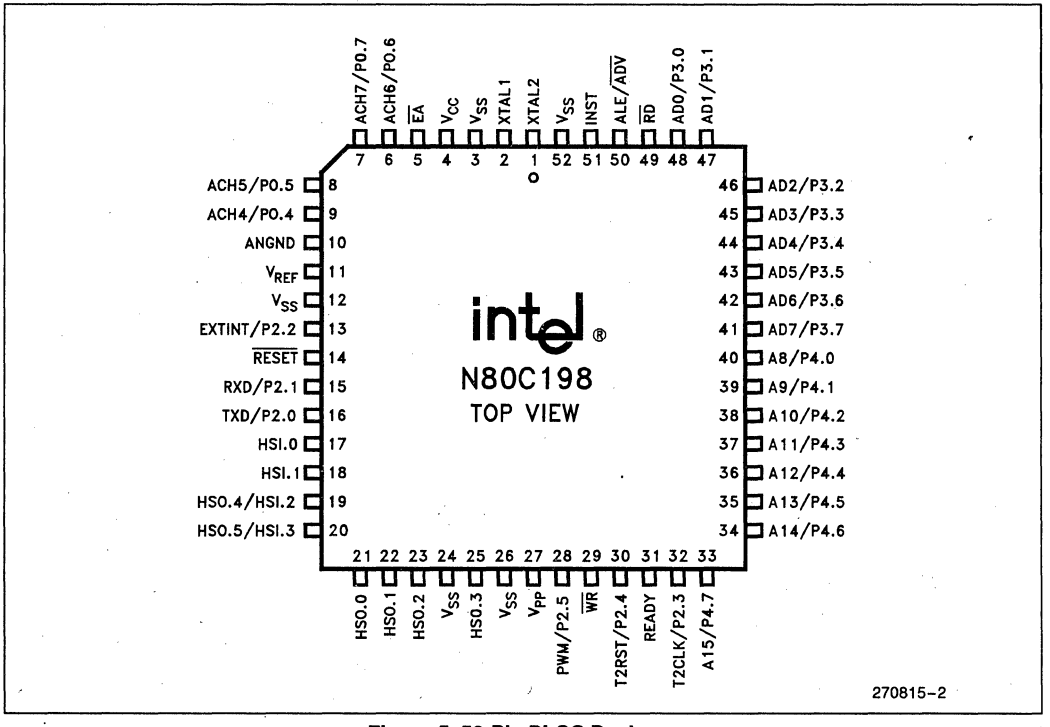
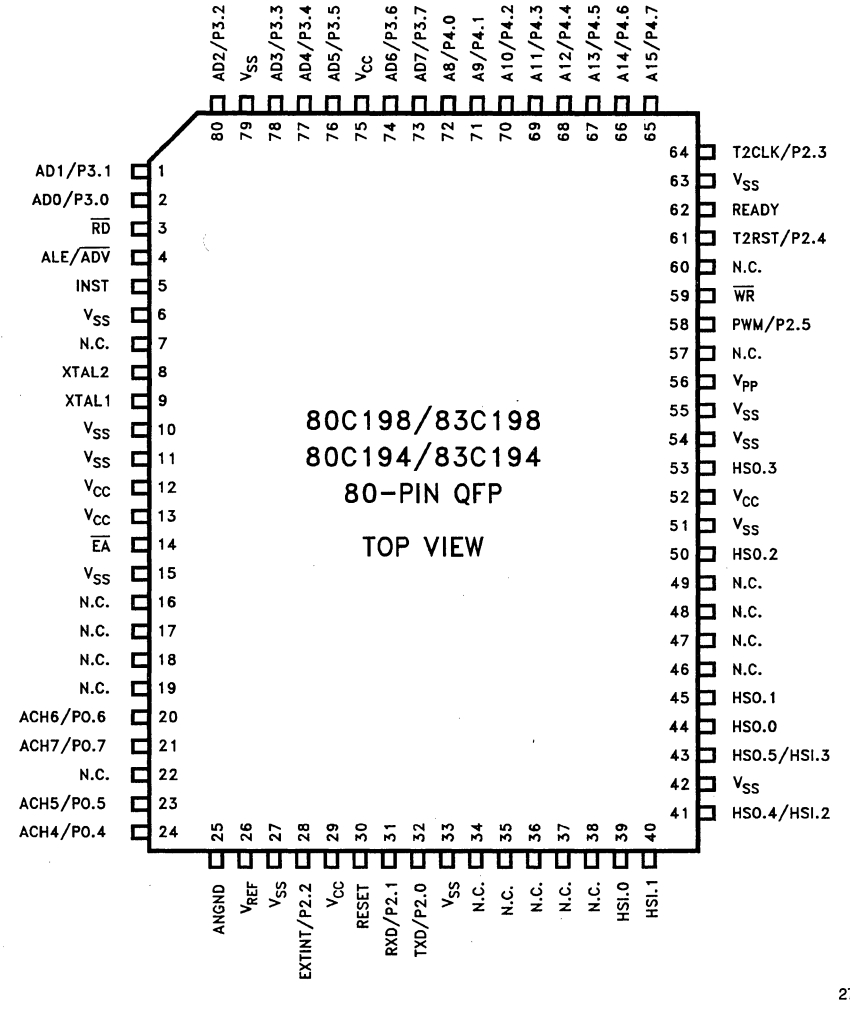


Figure 5. 52-Pin PLCC Package



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 6. 80-Pin QFP Package

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PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	The PLCC package has 5 V_{SS} pins and the QFP package has 12 V_{SS} pins. All must be connected to circuit ground.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS}. If this function is not used, connect to V_{CC}. This pin is the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
$\overline{\text{RESET}}$	Reset input to and open-drain output from the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition commences the Reset Sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. RESET has an internal pullup.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$	Write output to external memory. $\overline{\text{WR}}$ will go low for every external write.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available through configuration of CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	4-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins set the Programming Mode on the EPROM device.
Port 2	Multi-functional port. All of its pins are shared with other functions in the 80C198.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Available as I/O only on the ROM and EPROM devices.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. The TxD function is enabled by setting IOC1 5. In mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. The RxD function is enabled by setting SPCON.3. In mode 0 the pin functions as input or output data.
EXTINT	A positive transition on the EXTINT pin will generate an external interrupt. EXTINT is selected as the external interrupt source by setting IOC1.1 high.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2. The external reset function is enabled by setting IOCO.03 T2RST is enabled as the reset source by clearing IOCO.5.
PWM	Port 2.5 can be enabled as a PWM output by setting IOC1.O The duty cycle of the PWM is determined by the value loaded into the PWM-CONTROL register (17H).

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS} ..... −0.5V to +7.0V
Power Dissipation(1) 1.5W

NOTE:
1. Power dissipation is based on package heat transfer, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature Under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	3.5	12	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 32 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)		+3	μA	$0 < V_{IN} < V_{REF}$
I_{IL1}	Logical 0 Input Current in Reset (Note 2) (ALE, $\overline{RD}$, $\overline{WR}$, INST, P2.0)		−1.2	mA	V_{IN} = 0.45 V
Hyst	Hysteresis on RESET Pin	300		mV	

NOTE:
1. All pins except RESET and XTAL1.
2. Holding these pins below V_{IH} in Reset may cause the part to enter test modes.

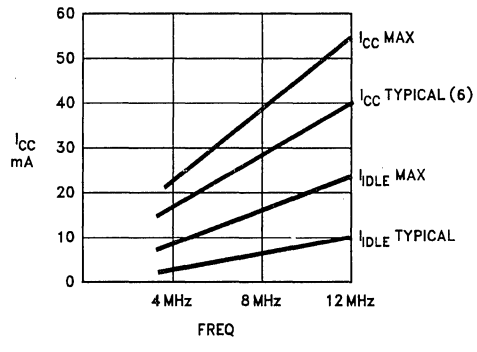
DC CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ(6)	Max	Units	Test Conditions
I_{CC}	Active Mode Current in Reset		40	55	mA	XTAL1 = 12 MHz
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current		10	22	mA	
I_{CC1}	Active Mode Current		15	22	mA	XTAL1 = 3.5 MHz
I_{PD}	Powerdown Mode Current		5	50	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:
(Notes apply to all specifications)
1. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, INST, HSO pins, PWM/P2.5, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
2. Standard Inputs include HSI pins, $\overline{EA}$, READY, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
3. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on Standard Output pins: 10 mA
4. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
5. During normal (non-transient) conditions the following total current limits apply:

HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, $\overline{WR}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST	I_{OL}: 13 mA	I_{OH}: 13 mA

6. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.



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I_{CC} Max = 3.88 × FREQ + 8.43
I_{IDLE} Max = 1.65 × FREQ + 2.2

Figure 7. I_{CC} and I_{IDLE} vs Frequency

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AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12 MHz

The system must meet these specifications to work with the 80C198/83C198:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to Ready Setup		$2T_{OSC} - 85$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 60$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 2)
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

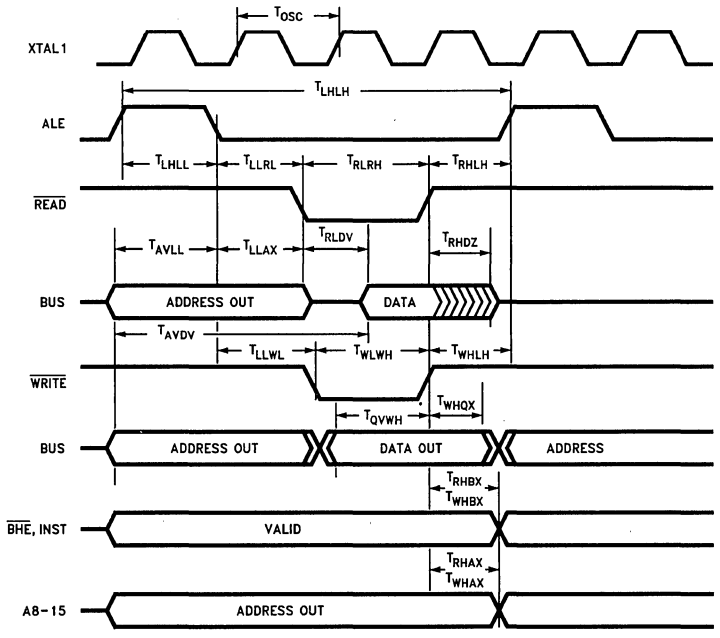
NOTES:
1. If max is exceeded, additional wait states will occur.
2. When using wait states, add $2T_{OSC} \times n$, where n = number of wait states.

The 80C198/83C198 will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on $XTAL_1$	3.5	12	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$	83	286	ns	
T_{LHLH}	ALE Cycle Time	$4T_{OSC}$		ns	(Note 4)
T_{LHLL}	ALE High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC} - 20$		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC} - 40$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC} - 30$		ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC} - 5$	$T_{OSC} + 25$	ns	(Note 4)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	$T_{OSC} + 25$	ns	(Note 3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		10	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC} - 10$		ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC} - 23$		ns	(Note 4)
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC} - 30$	$T_{OSC} + 5$	ns	(Note 4)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 2.5$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC} - 10$	$T_{OSC} + 15$	ns	(Note 3)
T_{WHBX}	INST Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{RHBX}	INST Hold after $\overline{RD}$ Rising Edge	$T_{OSC} - 10$		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	$T_{OSC} - 50$		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	$T_{OSC} - 25$		ns	

NOTES:
1. Testing performed at 3.5 MHz. However, the part is static by design and will typically operate below 1 Hz.
2. Typical specification, not guaranteed.
3. Assuming back-to-back bus cycles.
4. When using wait states, add $2T_{OSC} \times n$, where n = number of wait states.

System Bus Timings



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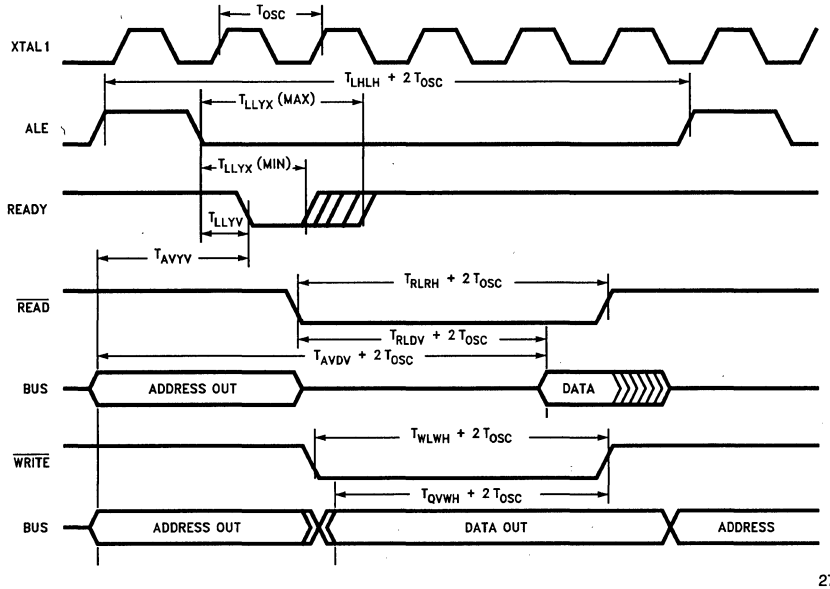
READY Timings (One Wait State)



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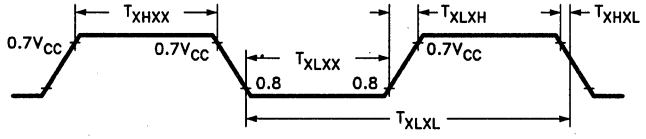
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	3.5	12.0	MHz
T_{XLXL}	Oscillator Period	83	286	ns
T_{XHXX}	High Time	32		ns
T_{XLXX}	Low Time	32		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

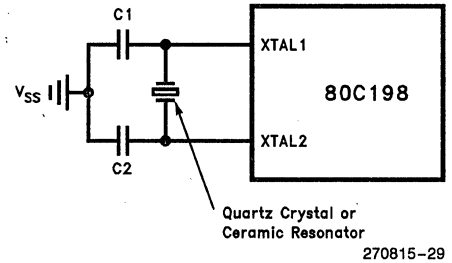
EXTERNAL CLOCK DRIVE WAVEFORMS



270815-25

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

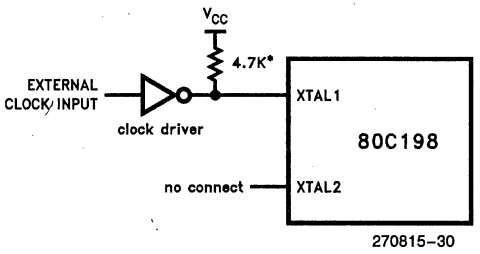
EXTERNAL CRYSTAL CONNECTIONS



270815-29

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF and C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended capacitor values.

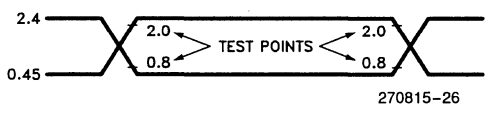
EXTERNAL CLOCK CONNECTIONS



270815-30

*Required if TTL driver used.
Not needed if CMOS driver is used.

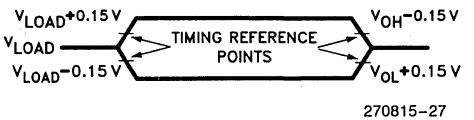
AC TESTING INPUT, OUTPUT WAVEFORMS



270815-26

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



270815-27

For Timing Purposes a Port Pin is no Longer Floating when a 150 mV change from Load Voltage Occurs and Begins to Float when a 150 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H - High
L - Low
V - Valid
X - No Longer Valid
Z - Floating

Signals:

A - Address
D - DATA IN
L - ALE/$\overline{ADV}$
Q - DATA OUT
R - $\overline{RD}$
W - $\overline{WR}$
X - XTAL1
Y - READY

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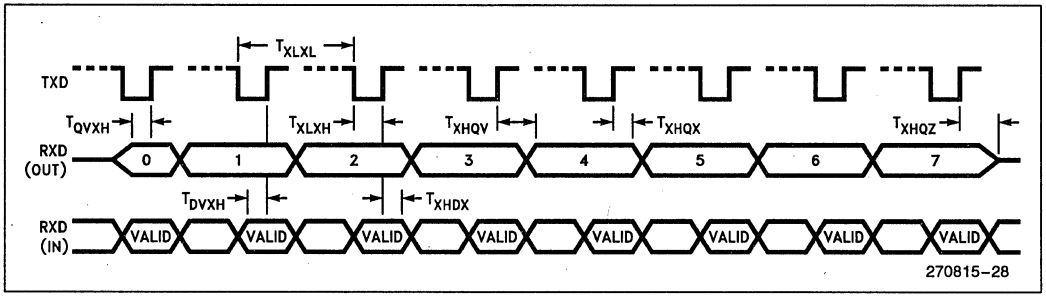
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} +50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



A TO D CHARACTERISTICS

There are two modes of A/D operation: with or without clock prescaler. The speed of the A/D converter can be adjusted by setting a clock prescaler on or off. At high frequencies more time is needed for the comparator to settle. The maximum frequency with the clock prescaler disabled is 8 MHz. The conversion times with the prescaler turned on or off is shown in the table below.

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

The 80C194/83C194 does not have an A/D converter.

See the MCS-96 A/D Quick Reference for definition of A/D terms.

Conversion Time

Clock Prescaler On IOC2.4 = 0	Clock Prescaler Off IOC2.4 = 1
158 States 26.33 μs @ 12 MHz	91 States 22.75 μs @ 8 MHz

A/D CONVERTER SPECIFICATIONS

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		512 9	1024 10	Levels Bits	
Absolute Error		0	±4	LSBs	
Full Scale Error	0.25 ±0.50			LSBs	
Zero Offset Error	−0.25 ±0.50			LSBs	
Non-Linearity Error	1.5 ±2.5	0	±4	LSBs	
Differential Non-Linearity Error		>−1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		1K	5K	Ω	
DC Input Leakage		0	3.0	μA	4
Sample Time: Prescaler On Prescaler Off	15 8			States States	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

EXTENDED TEMPERATURE/EXTENDED BURN-IN ONLY SPECIFICATIONS

Symbol	Description	Min	Max	Units
RESET Hysteresis	Hysteresis on RESET Pin	TBD		mV
IPD	Powerdown Mode Current		TBD	mA
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 65$	ns
T_{AVDV}	Address Valid to Input Data Valid		$3\,T_{OSC} - 60$	ns
T_{RLDV}	$\overline{RD}$ Low to Input Data Valid		$T_{OSC} - 25$	ns
T_{LHLL}	ALE High Period	$T_{OSC} - 12$	$T_{OSC} + 12$	ns
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising	$T_{OSC} - 50$		ns
A/D Absolute Error	Absolute Error		+6	LSBs

FUNCTIONAL DEVIATIONS

1. The DJNZW instruction is not guaranteed to be functional. The instruction, if encountered, will not cause an unimplemented opcode interrupt. (The opcode for DJNZW is 0E1 Hex.) The DJNZ (byte) instruction works correctly and should be used instead.
2. The HSI unit has two errata: one dealing with resolution and the other with first entries into the FIFO.

   The HSI resolution is 9 states instead of 8 states. Events on the same line may be lost if they occur faster than once every 9 state times.

   There is a mismatch between the 9 state time HSI resolution and the 8 state time timer. This causes one time value to be unused every 9 timer counts. Events may receive a time-tag one count later than expected because of this "skipped" time value.

   If the first two events into an empty FIFO (not including the Holding Register) occurs within 9 states after the first, its time-tag is one count later than the first's. If this is the "skipped" time value, the second event's time-tag is 2 counts later than the first's.

   If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register after 8 state times, leaving the FIFO empty again. If the second event occurs after this time, it will act as a new first event into an empty FIFO.
3. The serial port Framing Error flag fails to indicate an error if the bit preceding the stop bit is a 1. This is the case in both the 8-bit and 9-bit modes. False framing errors are never generated.
4. The serial port RI flag is not generated after the first byte is received. The problem does not occur if the baud rate is reloaded after each reception.
5. If the unsigned divide instruction (byte or word) is the last instruction in the queue as HOLD or READY is asserted, the result may be incorrect.

REVISION HISTORY

This data sheet (270815-003) is valid for devices marked with a "B" at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet and the previous version (-002).

1. The Express (extended temperature and extended burn-in) devices were added to this data sheet.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed.
3. Four errata were added: the CDE pin, the HSI resolution, the serial port framing error flag, the serial port RI flag and the DIVIDE during HOLD/READY.
4. One specification for the extended temperature and extended burn-in devices was changed: V_{IH2} Min was changed from 2.4V to 2.6V.

Differences between -002 and the -001 version of the 80C198 data sheet.

1. V_{SS} pin description was altered to reflect the correct number of pins.
2. V_{IH2} Min was changed from 2.2V to 2.6V.
3. Max I_{PD} was added and the I_{PD} note was deleted.

For more detailed information on the 80C198, refer to the *80C196KB User's Guide*, order number 270651. The *80C196KB User's Guide* applies to the 80C198 except for the design considerations listed above. Because the 80C198 is a reduced pin count version, some 80C196KB features are not available and are listed here:

1. PORT 1. PORT1 is a quasi-bidirectional port.
   A. HOLD/HLDA. This feature is multiplexed on PORT1.5–.7 and is not available.
2. The A/D converter loses four of its input channels, ACH0–3.
3. T2CAPTURE (P2.7) Timer2 Capture feature is not available.
4. T2UP/DN (P2.6) The Timer2 UP/DOWN feature is not available.
5. CLKOUT
6. NMI
7. BUSWIDTH
8. BHE
9. PACT

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8XC196KB/8XC196KB16
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

- 8 Kbytes of On-Chip ROM/OTP Available
- 232 Byte Register File
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- 1.75 μs 16 x 16 Multiply (16 MHz)
- 3.0 μs 32/16 Divide (16 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- 12 MHz and 16 MHz Available
- Dedicated 15-Bit Baud Rate Generator
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- Pulse-Width-Modulated Output
- Four 16-Bit Software Timers
- 10-Bit A/D Converter with Sample/Hold
- $\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Bus Protocol
- Extended Temperature Available

The 8XC196KB is a 16-bit microcontroller available in three different memory varieties: ROMless (80C196KB), 8K ROM (83C196KB) and 8K OTP (One Time Programmable—87C196KB). The 8XC196KB is a high performance member of the MCS-96 microcontroller family. The 8XC196KB has the same peripheral set as the 8096BH and has a true superset of the 8096BH instructions. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

Bit, byte, word and some 32-bit operations are available on the 80C196KB. With a 16 MHz oscillator a 16-bit addition takes 0.50 μs, and the instruction times average 0.37 μs to 1.1 μs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter. Also provided on-chip are an A/D converter, serial port, watchdog timer and a pulse-width-modulated output signal.

The 8XC196KB has a maximum guaranteed frequency of 12 MHz. The 8XC196KB16 has a maximum guaranteed frequency of 16 MHz. All references to the 80C196KB also refer to the 80C196KB16; 83C196KB, Rxxx; 87C196KB and 87C196KB16 unless otherwise noted. The ROM device does not have a speed indicator at the end of the device name. Instead it has a ROM code number.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

Package Designators: N = 68-pin PLCC, S = 80-pin QFP (commercial only). Prefix Designators: T = Extended Temperature.

October 1992
Order Number: 270909-004

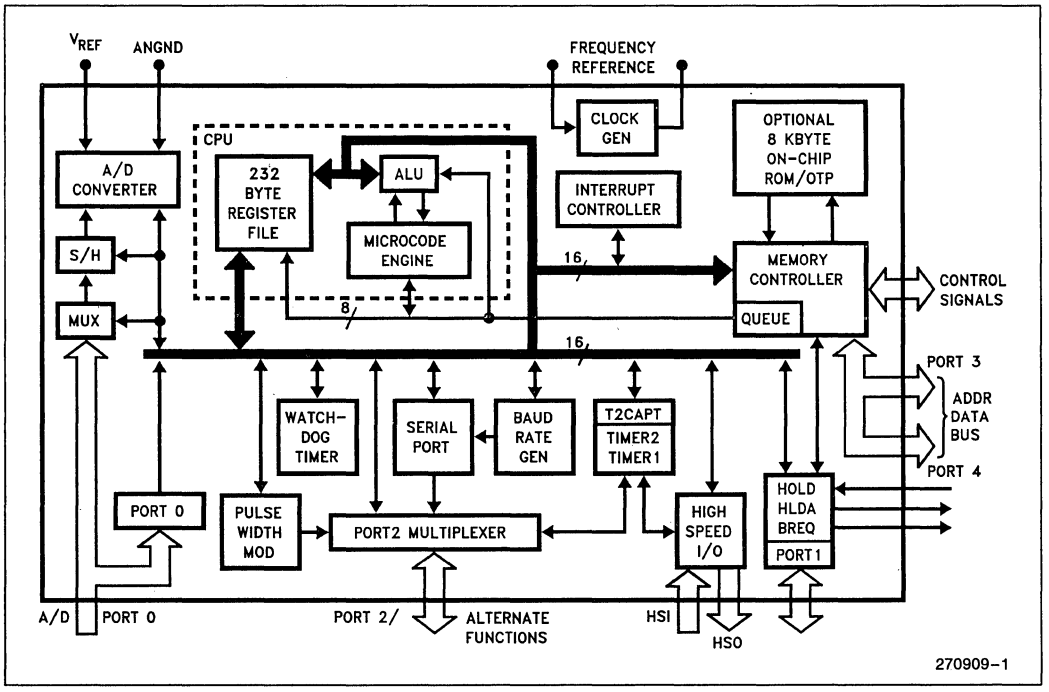

Figure 1. 8XC196KB Block Diagram

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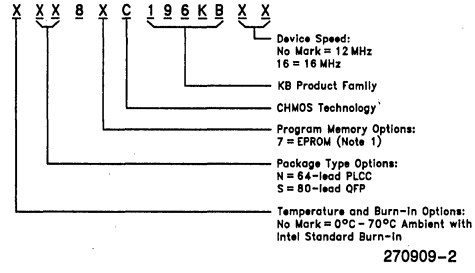
PROCESS INFORMATION

This device is manufactured on P629.0 and 629.1, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196KB16 is 68-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 2. The 8XC196KB Nomenclature

Table 1. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	70°C/W	4°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 2. 8XC196KB Memory Map

Description	Address
External Memory or I/O	0FFFFH 04000H
Internal ROM/EPROM or External Memory (Determined by $\overline{EA}$)	3FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4 Word Addressable Only	1FFFH 1FFEH
External Memory	1FFDH 0100H
232 Bytes Register RAM (Note 1)	00FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 00FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KB quick reference for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

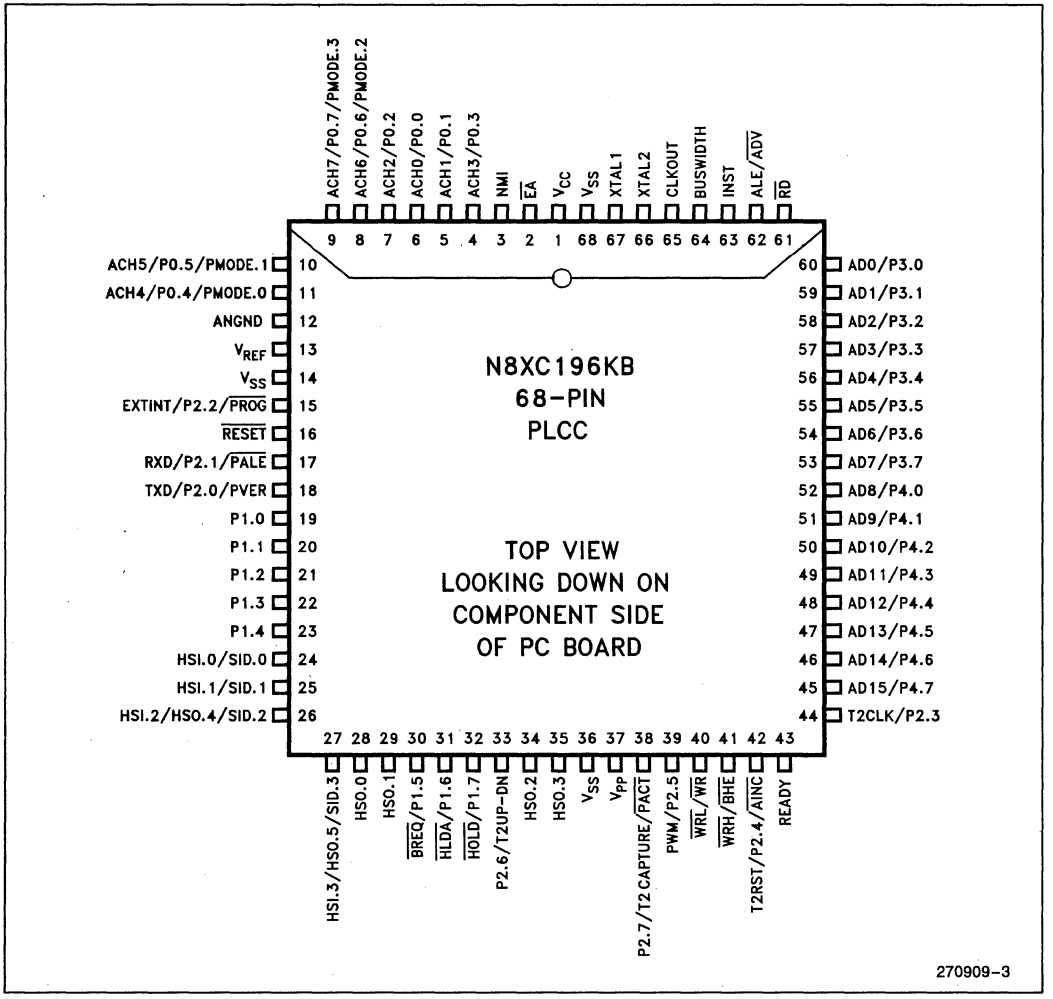


Figure 3. 68-Pin Package (PLCC Top View)

NOTE:
The above pin out diagram applies to the OTP (87C196KB) device. The OTP device uses all of the programming pins shown above. The ROM (83C196KB) device only uses programming pins: $\overline{AINC}$, $\overline{PALE}$, PMODE.n, and $\overline{PROG}$. The ROMless (80C196KB) doesn't use any of the programming pins.

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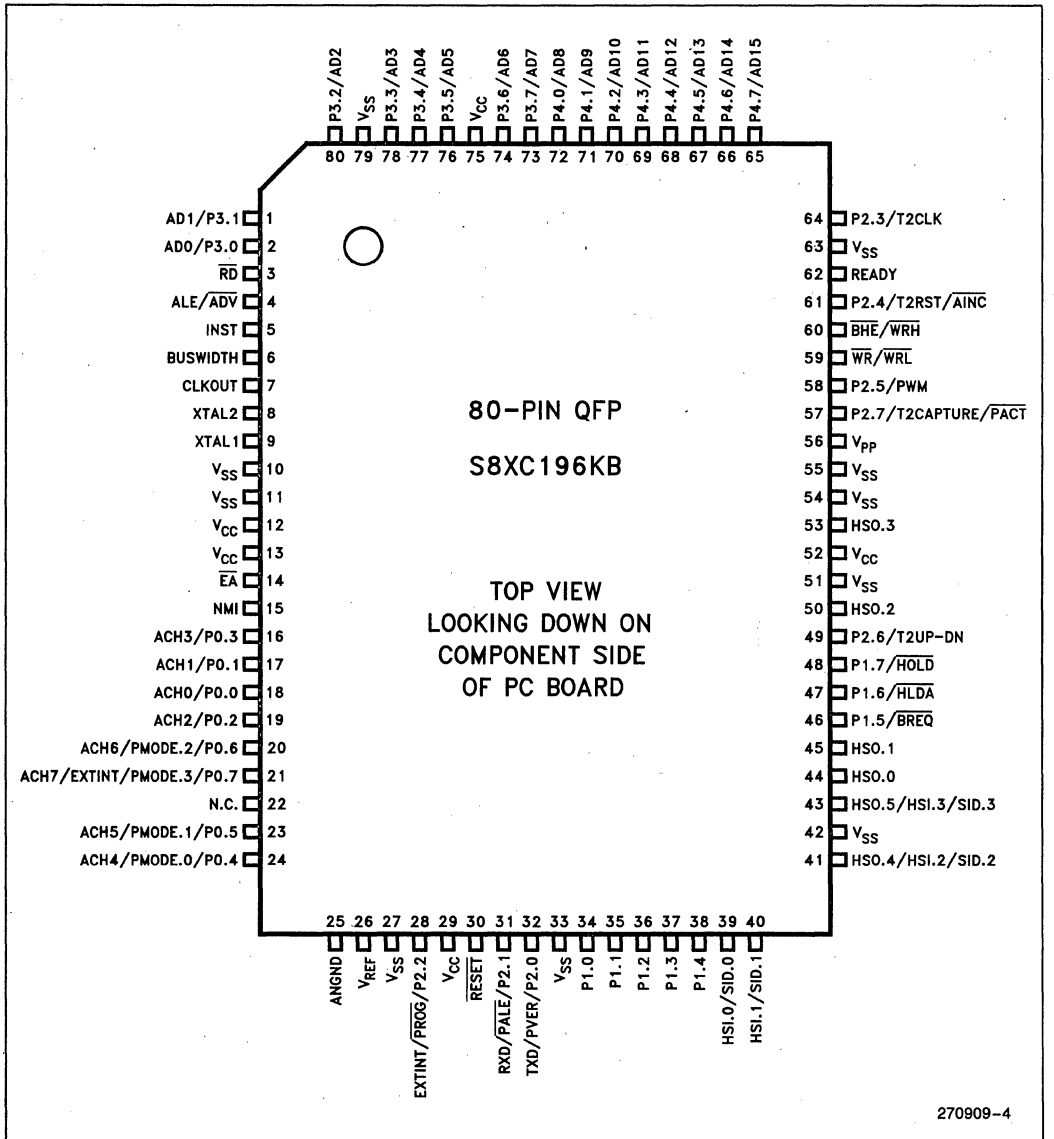

NOTE:
N.C. means No Connect (do not connect these pins).

Figure 4. 80-Pin QFP Package

NOTE:
The above pin out diagram applies to the OTP (87C196KB) device. The OTP device uses all of the programming pins shown above. The ROM (83C196KB) device only uses programming pins: $\overline{\text{AINC}}$, $\overline{\text{PALE}}$, PMODE.n, and $\overline{\text{PROG}}$. The ROMless (80C196KB) doesn't use any of the programming pins.

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of them must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}. Connect V_{SS} and ANGND at chip to avoid noise problems.
V_{PP}	Programming voltage. Also timing pin for the return from power down circuit.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input to and open-drain output from the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch and output low indicates a data fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/OTPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being addressed. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle (held not ready) is available in the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 0	8-bit high impedance input-only port. Three pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port. These pins are shared with $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and $\overline{\text{BREQ}}$.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 87C196KB. Pins P2.6 and P2.7 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus, which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus. Enabled by setting WSR.7.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. In Mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. In Mode 0 the pin functions as input or output data.
EXTINT	A rising edge on the EXTINT pin will generate an external interrupt.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2.
PWM	The pulse width modulator output.
T2UP-DN	The T2UPDN pin controls the direction of Timer2 as an up or down counter.
T2CAPTURE	A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register.
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
SID	Slave ID Number. Used to assign each slave a pin of Port 3 or 4 to use for passing programming verification acknowledgement.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PACT}}$	Programming Active. Used in the Auto Programming Mode to indicate when programming activity is complete.
$\overline{\text{PVAL}}$	Program Valid. This signal indicates the success or failure of programming in the Auto Programming Mode. A zero indicates successful programming.
PVER	Program Verification. Used in Slave Programming and Auto CLB Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
Ports 3 and 4 (Programming Mode)	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory. Should have pullups to V_{CC} when used in slave programming mode.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS} ..... −0.5V to +7.0V
Power Dissipation(1) 1.5W

NOTE:
1. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency **12 MHz**	3.5	12	MHz
F_{OSC}	Oscillator Frequency **16 MHz**	3.5	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage(1)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 µA I_{OH} = −30 µA I_{OH} = −60 µA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	µA	0 < V_{IN} < V_{CC} − 0.3V
I_{LI1}	Input Leakage Current (Port 0)		+3	µA	0 < V_{IN} < V_{REF}
I_{TL}	1 to 0 Transition Current (QBD Pins)		−650	µA	V_{IN} = 2.0V
I_{IL}	Logical 0 Input Current (QBD Pins)(4)		−50	µA	V_{IN} = 0.45V

NOTE:
All pins except RESET and XTAL1.

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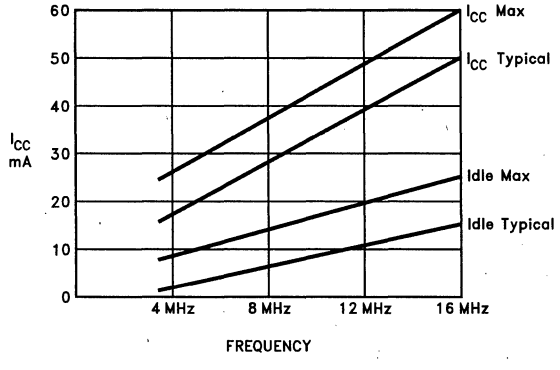
DC CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ(7)	Max	Units	Test Conditions
I_{IL1}	Logical 0 Input Current in Reset ALE, $\overline{RD}$, INST			−7	mA	V_{IN} = 0.45V
I_{IH1}	Logical 1 Input Current on NMI Pin			100	μA	V_{IN} = 2.0V
Hyst.	Hysteresis on RESET Pin	300			mV	
I_{CC}	Active Mode Current in Reset		50	60	mA	XTAL1 = 16 MHz
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF}$ = 5.5V
I_{IDLE}	Idle Mode Current		10	25	mA	
I_{CC1}	Active Mode Current		15	25	mA	XTAL1 = 3.5 MHz
I_{PD}	Powerdown Mode Current		5	30	μA	$V_{CC} = V_{PP} = V_{REF}$ = 5.5V
R_{RST}	Reset Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:
(Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, CDE, $\overline{EA}$, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC}$ = 5V.



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I_{CC} Max = 3.88 × FREQ + 8.43
I_{IDLE} Max = 1.65 × FREQ + 2.2

Figure 6. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The system must meet these specifications to work with the 87C196KB:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 60$	ns	(Note 3)
T_{YLYH}	NonREADY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 60$	ns	(Note 3)
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. When using wait states, add $2T_{OSC} \times n$ where n = number of wait states.
3. These timings are included for compatibility with −90 and BH products. They should not be used for newer high-speed designs.

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AC CHARACTERISTICS (Continued)

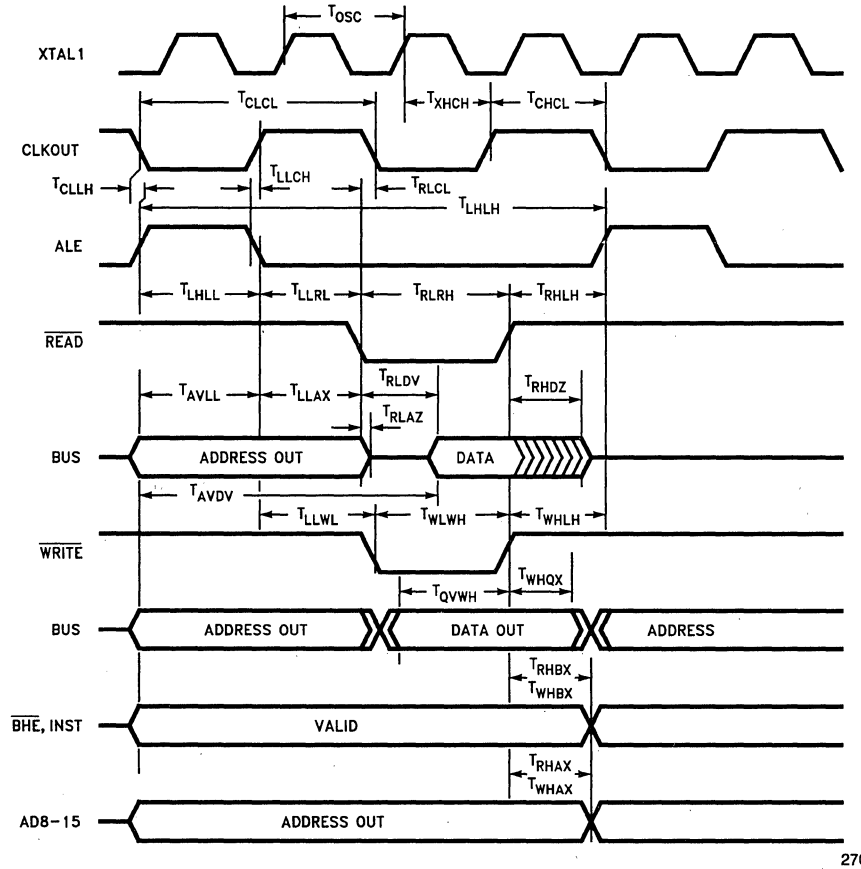
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The 87C196KB will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 **12 MHz**	3.5	12.0	MHz	(Note 2)
F_{XTAL}	Frequency on XTAL1 **16 MHz**	3.5	16.0	MHz	(Note 2)
T_{OSC}	$1/F_{XTAL}$ **12 MHz**	83.3	286	ns	
T_{OSC}	$1/F_{XTAL}$ **16 MHz**	62.5	286	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC}+10	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	+10	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 3)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC}+10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 20		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 35		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+25	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC}−5	T_{OSC} + 25	ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 1)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	(Note 3)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 15	T_{OSC} + 5	ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 15	T_{OSC} + 10	ns	(Note 1)
T_{WHBX}	$\overline{BHE}$, INST HOLD after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{RHBX}	$\overline{BHE}$, INST HOLD after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 hold after $\overline{WR}$ Rising Edge	T_{OSC} − 30		ns	
T_{RHAX}	AD8–15 hold after $\overline{RD}$ Rising Edge	T_{OSC} − 25		ns	

NOTES:
1. Assuming back-to-back bus cycles.
2. Testing performed at 3.5 MHz, however, the device is static by design and will typically operate below 1 Hz.
3. When using wait states, all 2 T_{OSC}+ n where n = number of wait states.

System Bus Timings



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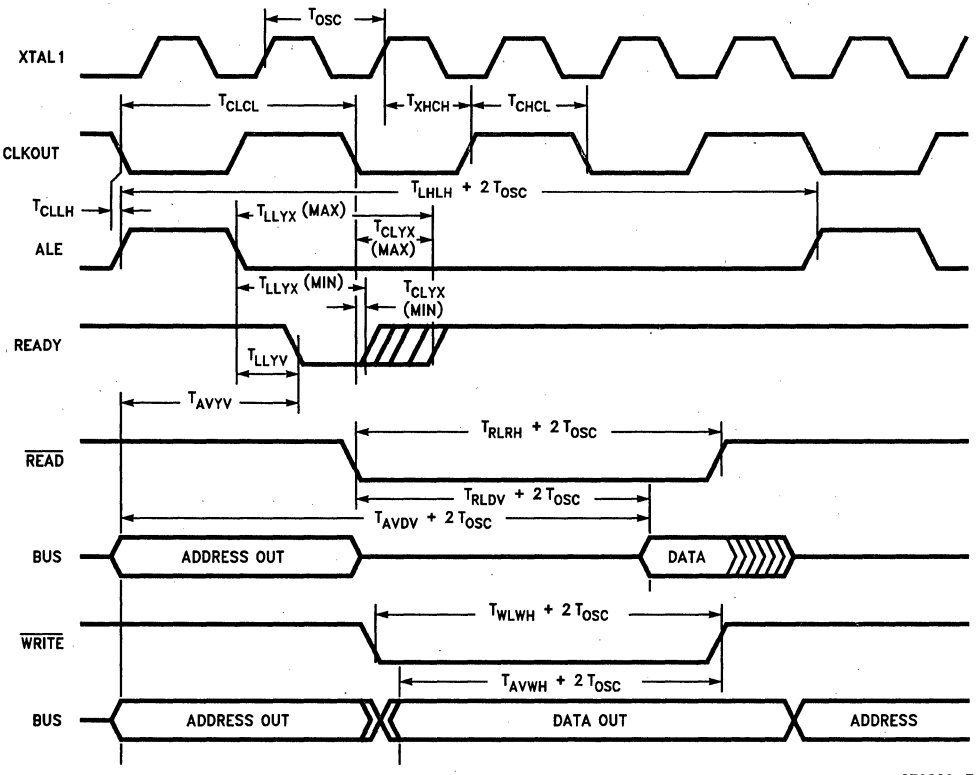
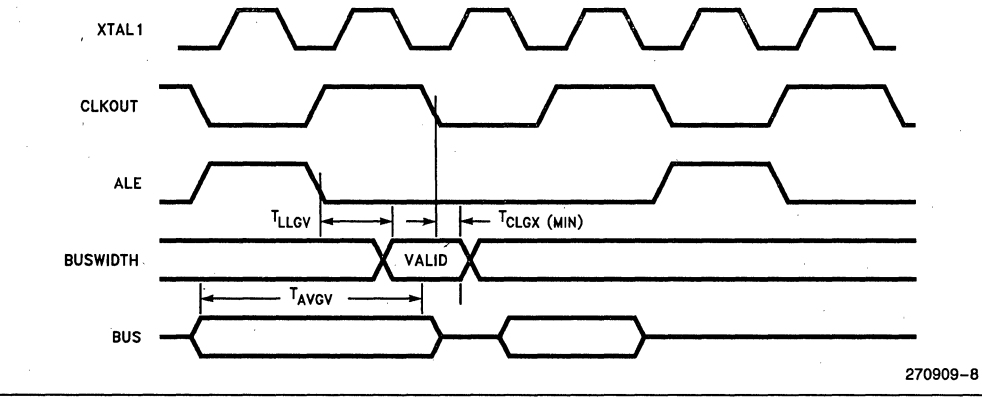
READY Timings (One Wait State)



Buswidth Bus Timings



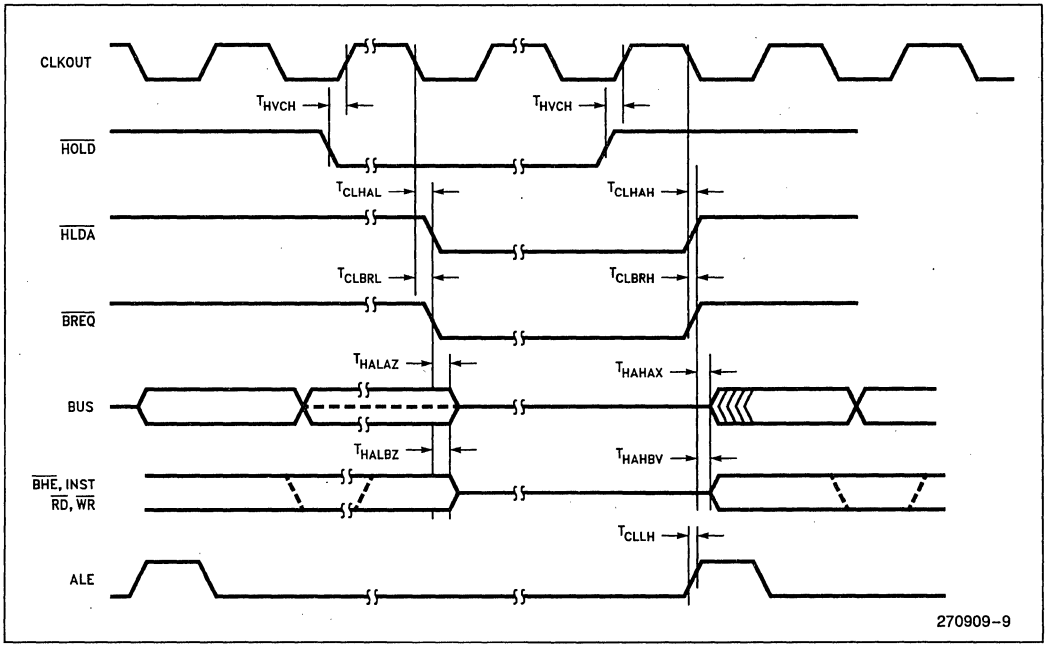
HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to HLDA Low		15	ns	
T_{CLBRL}	CLKOUT Low to BREQ Low		15	ns	
T_{HALAZ}	HLDA Low to Address Float		10	ns	
T_{HALBZ}	HLDA Low to BHE, INST, RD, WR Float		10	ns	
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	
T_{HAHAV}	HLDA High to Address Valid	0		ns	
T_{HAHBX}	HLDA High to BHE, INST, RD, WR No Longer Float	−20		ns	
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	0		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

NOTE:
1. To guarantee recognition at next clock.

Maximum Hold Latency

Bus Cycle Type	Latency
Internal Access	1.5 States
16-Bit External Execution	2.5 States
8-Bit External	4.5 States



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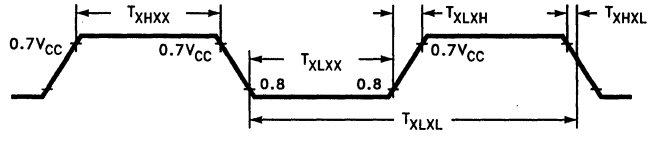
EXTERNAL CLOCK DRIVE

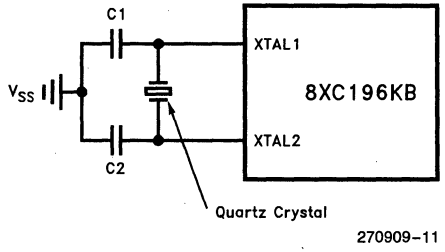
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency **12 MHz**	3.5	12.0	MHz
$1/T_{XLXL}$	Oscillator Frequency **16 MHz**	3.5	16	MHz
T_{XLXL}	Oscillator Period **12 MHz**	83.3	286	ns
T_{XLXL}	Oscillator Period **16 MHz**	62.5	286	ns
T_{XHXX}	High Time	21.25		ns
T_{XLXX}	Low Time	21.25		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



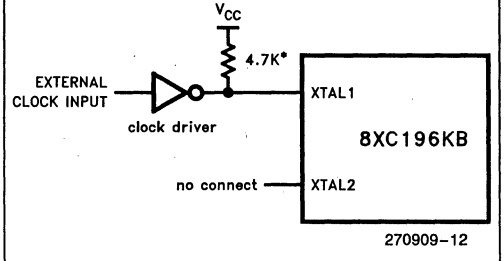
An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications, the capacitance will not exceed 20 pF.

EXTERNAL CRYSTAL CONNECTIONS



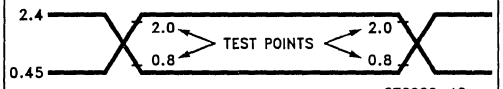
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

EXTERNAL CLOCK CONNECTIONS



* Required if open-collector TTL driver used
Not needed if CMOS driver is used.

AC TESTING INPUT, OUTPUT WAVEFORMS



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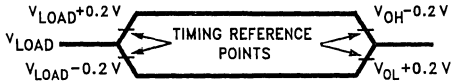
AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



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For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H - High
L - Low
V - Valid
X - No Longer Valid
Z - Floating

Signals:

A - Address
B - $\overline{BHE}$
BR - $\overline{BREQ}$
C - CLKOUT
D - DATA IN
G - Buswidth
H - $\overline{HOLD}$
HA - $\overline{HLDA}$
L - ALE/$\overline{ADV}$
Q - DATA OUT
R - $\overline{RD}$
W - $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X - XTAL1
Y - READY

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10-BIT A/D CHARACTERISTICS

At a clock speed of 6 MHz or less, the clock prescaler should be disabled. This is accomplished by setting IOC2.4 = 1.

At higher frequencies (greater than 6 MHz) the clock prescaler should be enabled (IOC2.4 = 0) to allow the comparator to settle.

The table below shows two different clock speeds and their corresponding A/D conversion and sample times.

State times are calculated as follows:

$$\text{state time} = \frac{2}{\text{XTAL1}}$$

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

See the MCS-96 A/D Converter Quick Reference for definition of A/D terms.

Example Sample and Conversion Times

A/D Clock Prescaler	Clock Speed (MHz)	Sample Time (States)	Sample Time at Clock Speed (μs)	Conversion Time (States)	Conversion Time at Clock Speed (μs)
IOC2.4 = 0 → ON	16	15	1.875	156.5	19.6
IOC2.4 = 1 → OFF	6	8	2.667	89.5	29.8

A/D CONVERTER SPECIFICATIONS

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ±0.50			LSBs	
Zero Offset Error	−0.25 ±0.50			LSBs	
Non-Linearity Error	1.5 ±2.5	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
DC Input Leakage		0	3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages During Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	12.50	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
F_{OSC}	Oscillator Frequency **12 MHz**	6.0	12.0	MHz
F_{OSC}	Oscillator Frequency **16 MHz**	6.0	16.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	40		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	50		T_{OSC}
T_{LLVL}	$\overline{PALE}$ Low to PVER Low		60	T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	40		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	120		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	120		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	40		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to PVER Low		90	T_{OSC}

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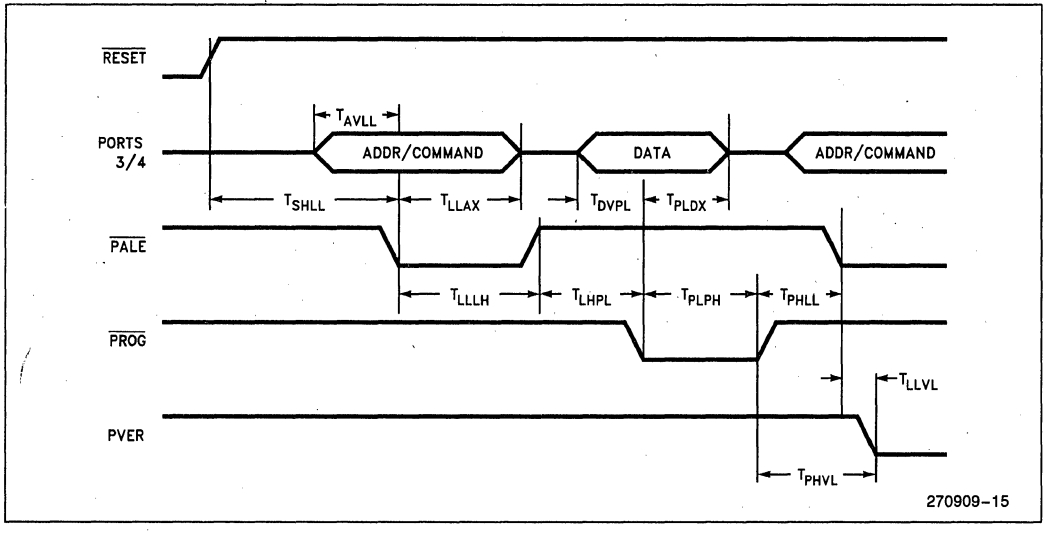
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

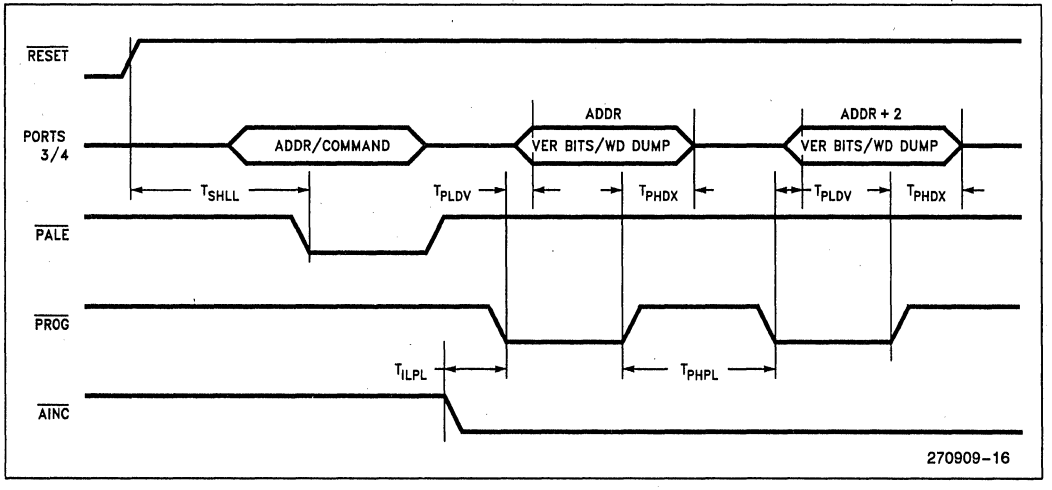
NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

EPROM PROGRAMMING WAVEFORMS

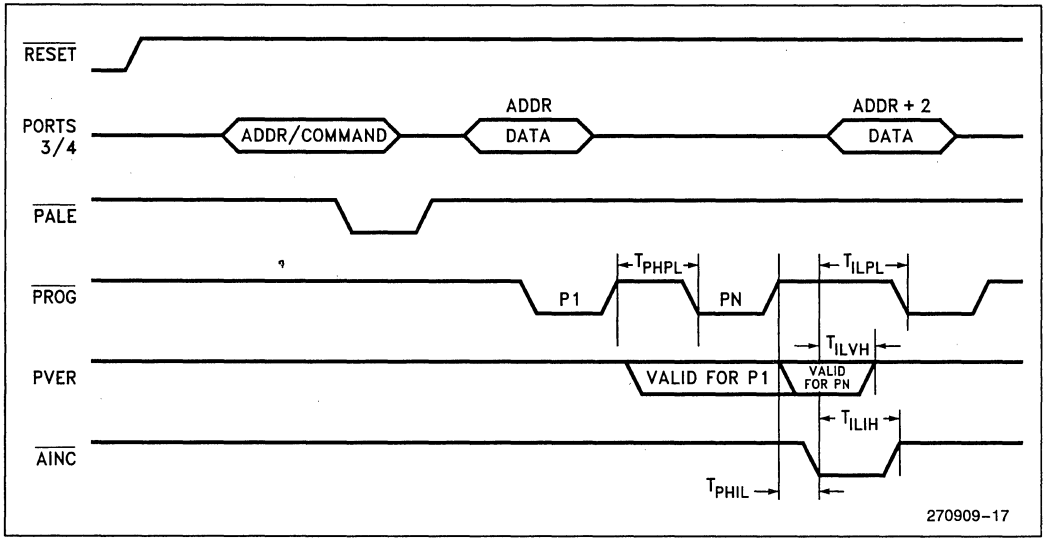
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} +50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		2 T_{OSC}	ns

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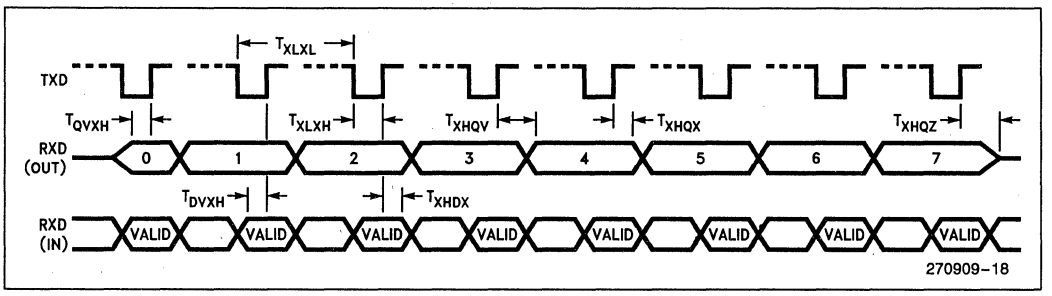
WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



FUNCTIONAL DEVIATIONS

Devices marked with an "E", "F" or "G" have the following errata.

1. High Speed Inputs

The High Speed Input (HSI) has three deviations from the specifications.

NOTE:
"Events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine state may be lost.

B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-tag value to be skipped every nine timer counts. Events may receive a time-tag one count later than expected.

C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into an empty FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within 9 states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time-tags will be at least two counts apart.

2. CMPL with RO

Using CMPL with register 0 can set incorrect flags. Don't use register 0 with the compare long (CMPL) instruction. Use another long word register and set it equal to zero. See tech bit MC0692.

REVISION HISTORY

This data sheet (270909-004) is valid for devices with an "E", "F" or "G" at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (270909-004) and (270909-003):

1. The ROM (80C196KB), and ROMless (83C196KB) were combined with this data sheet resulting in no specification differences.
2. The description of the prescalar bit for the A/D has been enhanced.
3. T_{HAHBV}MIN was −15 ns (270909-003). Now T_{HAHBV}MIN is −20 ns (270909-004).
4. T_{XHQZ}MAX was 1 TOSC (270909-003). Now T_{XHQZ}MAX is 2 TOSC (270909-004). This should have no impact on designs using synchronous serial mode 0.
5. The change indicators for the 80C196KB are "E", "F" and "G". Previously there was only one change indicator "E". The change indicator is used for tracking purposes. The change indicator is the last character in the FPO number. The FPO number is the second line on the top side of the device.

The following differences exist between (-003) and version (-002).

1. The 12 MHz and 16 MHz devices were combined in this data sheet. The 87C196KB 12 MHz only data sheet (272035-001) is now obsolete.

2. Changes were made to the format of the data sheet and the SFR descriptions were removed.
3. The -002 version of this data sheet was valid for devices marked with a "B" or a "D" at the end of the top side tracking number.
4. The OSCILLATOR errata was removed.
5. An errata was not documented in the -002 data sheet for devices marked with a "B" or a "D". This is the DIVIDE DURING HOLD/READY errata. When HOLD or READY is active and DIV/DIVB is the last instruction in the queue, the divide result may be incorrect.
6. T_{XCH} was changed from Min = 40 ns to Min = 20 ns.
7. T_{RLCL} was changed from Min = 5 ns to Min = 4 ns.
9. I_{IL1} was changed from Max = −6 mA to Max = −7 mA.
10. T_{HAHBV} was changed from Min = −10 ns to Min = −15 ns.

Differences between the -002 and -001 data sheets.

1. The -001 version of this data sheet was valid for devices marked with a "C" at the end of the top side tracking number.
2. Added 64L SDIP and 80L QFP packages.
3. Added IIH1.
4. Changed T_{CHWH} Min from − 10 ns to − 5 ns.
5. Changed T_{CHWH} Max from + 10 ns to + 15 ns.
6. Changed T_{WLWH} Min from T_{OSC} − 20 ns to T_{OSC} − 15 ns.
7. Changed T_{WHQX} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
8. Changed T_{WHLH} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
9. Changed T_{WHLH} Max from T_{OSC} + 15 ns to T_{OSC} + 10 ns.
10. Changed T_{WHBX} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
11. Changed T_{HVCH} Min from 85 ns to 55 ns.
12. Remove T_{HVCH} Max.
13. Changed T_{CLHAL} Min from − 10 ns to − 15 ns.
14. Changed T_{CLHAL} Max from 20 ns to 15 ns.
15. Changed T_{CLBRL} Min from − 10 ns to − 15 ns.
16. Changed T_{CLBRL} Max from 20 ns to 15 ns.
17. Changed T_{HAHAX} Min from − 10 ns to − 15 ns.
18. Added HSI description to Functional Deviations.
19. Added Oscillator description to Functional Deviations.

8XC198
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

8 Kbytes of OTPROM

- 8 Kbytes of On-Chip OTPROM or ROM
- 232 Byte Register File
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- 1.75 μs 16 x 16 Multiply (16 MHz)
- 3.0 μs 32/16 Divide (16 MHz)
- Powerdown and Idle Modes
- 16-Bit Watchdog Timer
- 8-Bit External Bus
- 16 MHz Standard
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Counter
- Pulse-Width-Modulated Output
- Four 16-Bit Software Timers
- 10-Bit A/D Converter with Sample/Hold
- Extended Temperature Available

The 8XC198 family offers low-cost entry into Intel's powerful MCS®-96 16-bit microcontroller architecture. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

The 8XC198 is the 8-bit bus version of the 8XC196KB. The prefixes mean: 80 (ROMless), 83 (ROM), 87 (OTP) One Time Programmable. The ROM and OTP are available in 8 Kbytes.

Bit, byte, word and some 32-bit operations are available on the 8XC198. With a 16 MHz oscillator a 16-bit addition takes 0.50 μs, and the instruction times average 0.37 μs to 1.1 μs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or counter. Also provided on-chip are an A/D converter, serial port, watchdog timer and a pulse-width-modulated output signal.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. Wth the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

October 1992
Order Number: 272034-003

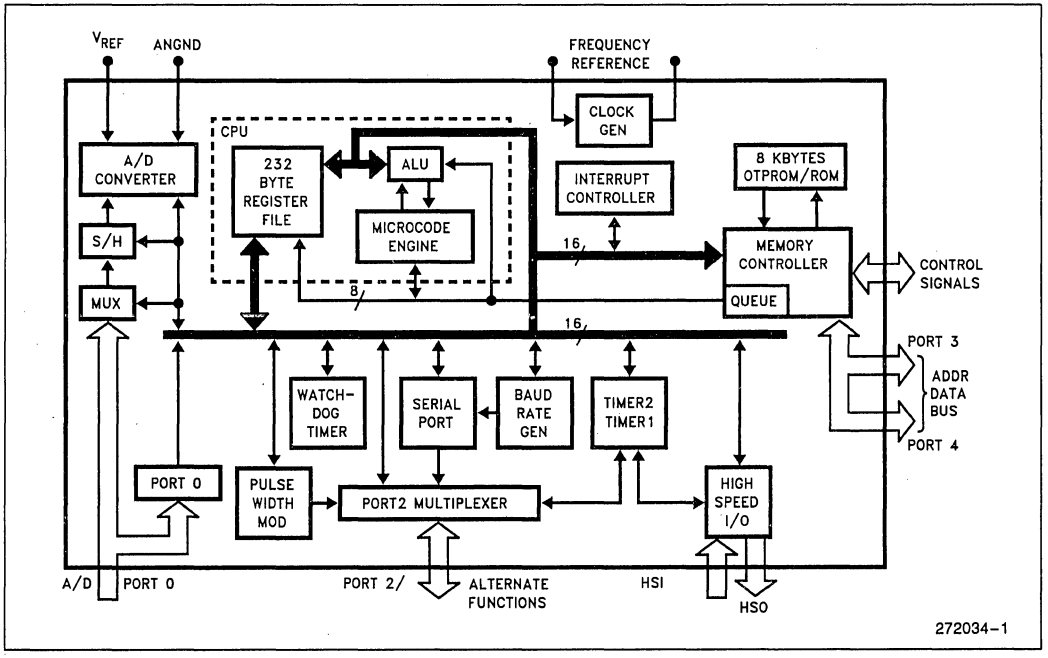


Figure 1. 87C198 Block Diagram

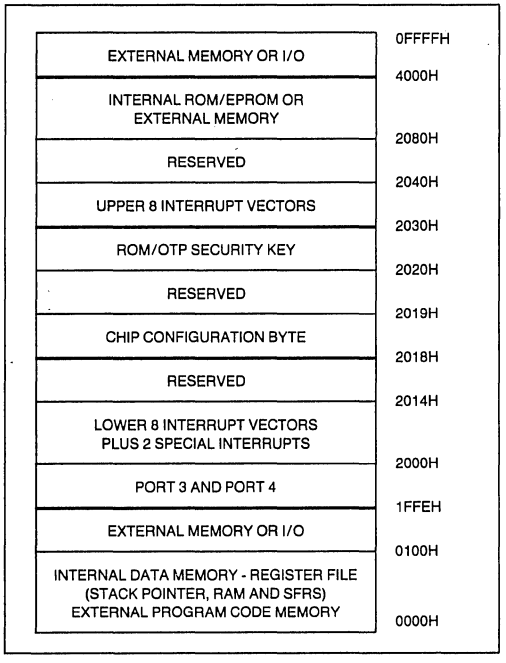


Figure 2. Memory Map

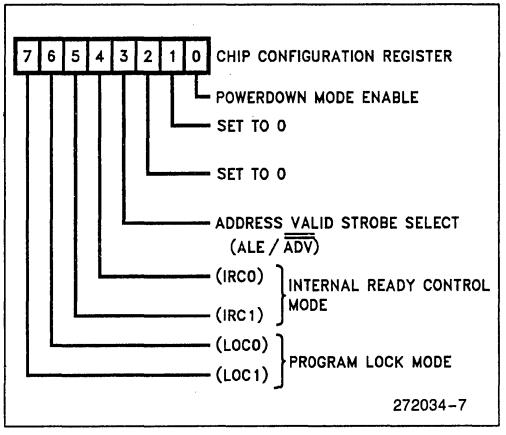


Figure 3. Chip Configuration (2018H)

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WARNING:
Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

PACKAGING

The 8XC198 is available in a 52-pin PLCC package and an 80-pin QFP package. Contact your local sales office to determine the exact ordering code for the part desired.

Package Designators:
N = 52-pin PLCC
S = 80-pin QFP

Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	40°C/W	
QFP	70°C/W	4°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

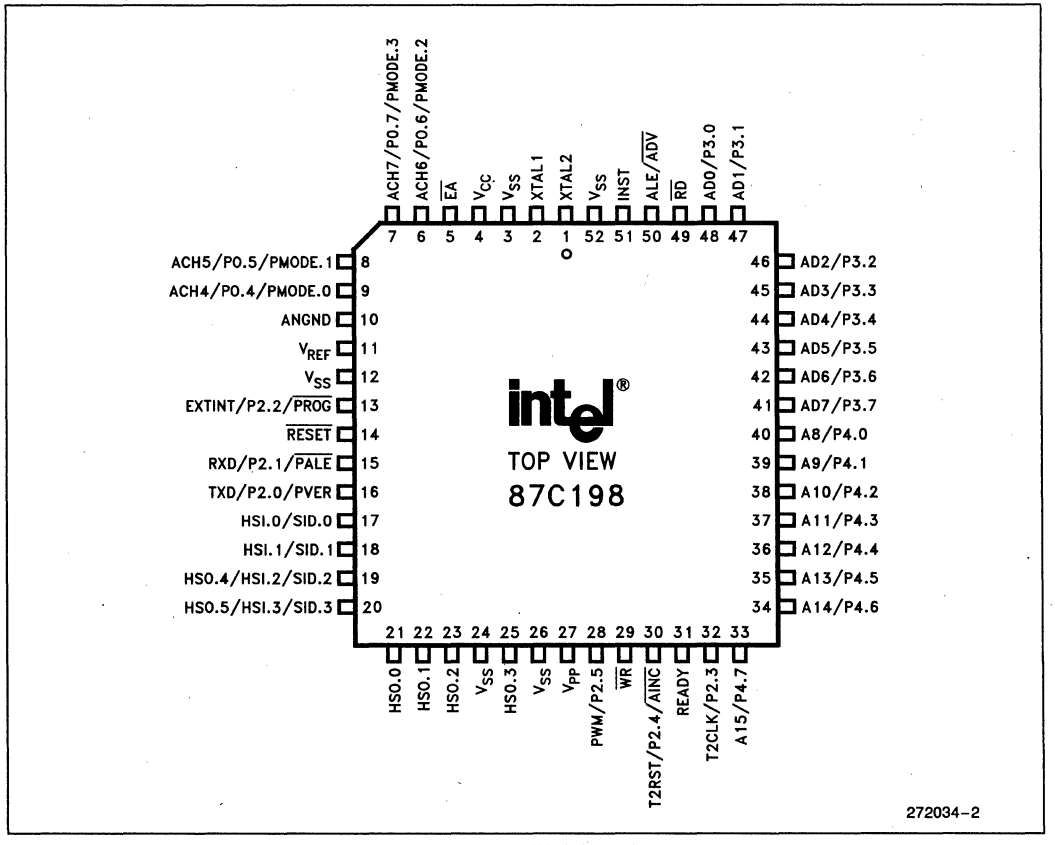
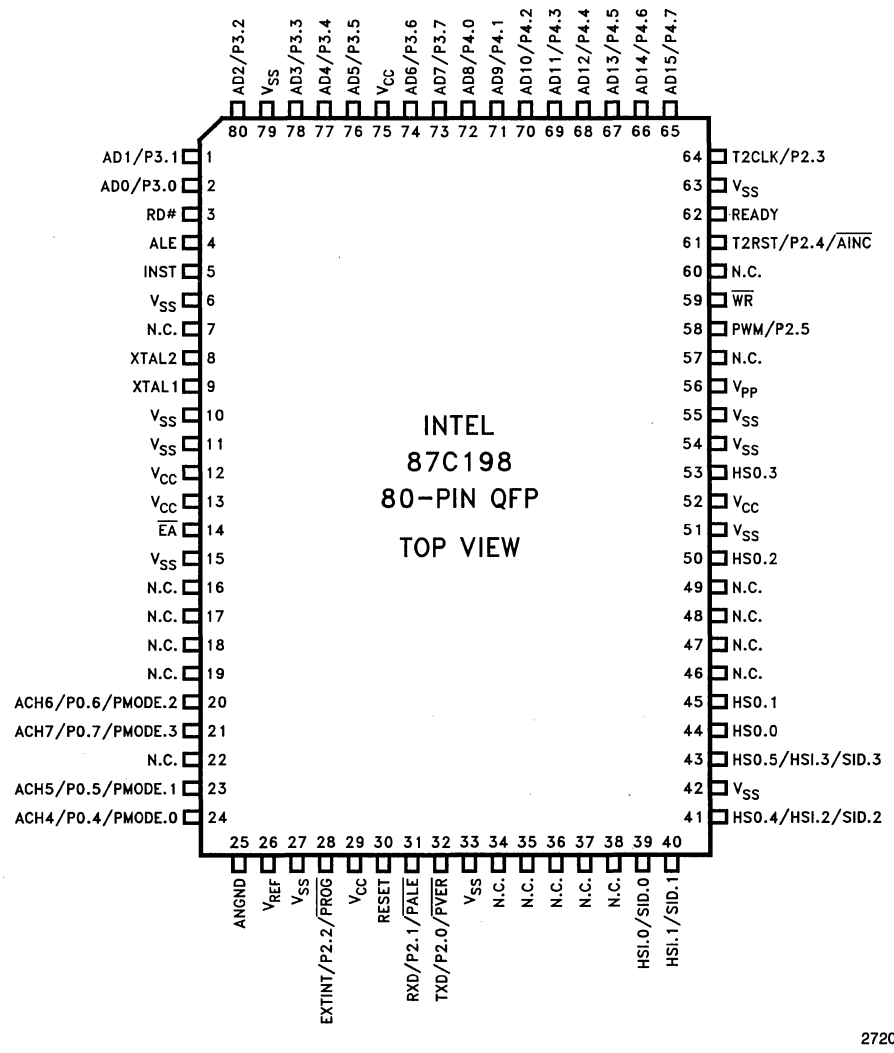


Figure 4. 52-Pin PLCC Package

NOTE:
The above pinout diagram applies to the OTP (87C198) device. The OTP device uses all of the programming pins shown above. The ROM (83C198) device only uses programming pins: **AINC, PALE, PMODE.n** and **PROG**. The ROMless (80C198) doesn't use any of the programming pins.



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 5. 80-Pin QFP Package

NOTE:
The above pinout diagram applies to the OTP (87C198) device. The OTP device uses all of the programming pins shown above. The ROM (83C198) device only uses programming pins: **AINC, PALE, PMODE.n** and **PROG**. The ROMless (80C198) doesn't use any of the programming pins.

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PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	The PLCC package has 5 V_{SS} pins and the QFP package has 12 V_{SS} pins. All must be connected to digital ground.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming Voltage. Also, timing pin for the return from powerdown circuit.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
$\overline{RESET}$	Reset input to and open-drain output from the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition commences the 10-state Reset Sequence.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$	Write output to external memory. $\overline{WR}$ will go low for every external write.
READY	Ready input to lengthen external memory cycles. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available through configuration of CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	4-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins set the Programming Mode on the EPROM device.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 2	Multi-functional port. All of its pins are shared with other functions in the 80C198.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Available as I/O only on the ROM and EPROM devices.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. In mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. In mode 0 the pin functions as input or output data.
EXTINT	A positive transition on the EXTINT pin will generate an external interrupt.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2.
PWM	The PWM output.
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
SID	Slave ID Number. Used to assign each slave a pin of Port 3 or 4 to use for passing programming verification acknowledgement.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PVAL}}$	Program Valid. This signal indicates the success or failure of programming in the Auto Programming Mode. A zero indicates successful programming.
PVER	Program Verification. Used in Slave Programming and Auto CLB Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
PORTS 3 and 4 (when programming)	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory. Should have pullups to V_{CC} (15 kΩ).

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +150°C

Voltage on V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.3V to +13.0V

Voltage on Any Other Pin to V_{SS} .. −0.5V to +7.0V

Power Dissipation(1) 1.5W

NOTE:
1. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency **16 MHz**	3.5	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (1)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 32 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	µA	0 < V_{IN} < V_{CC} − 0.3V
I_{LI1}	Input Leakage Current (Port 0)		+3	µA	0 < V_{IN} < V_{REF}
I_{IL1}	Logical 0 Input Current in Reset (ALE, $\overline{RD}$, INST)		−6	mA	V_{IN} = 0.45 V
Hyst	Hysteresis on RESET Pin	300		mV	

NOTE:
1. All pins except RESET and XTAL1.

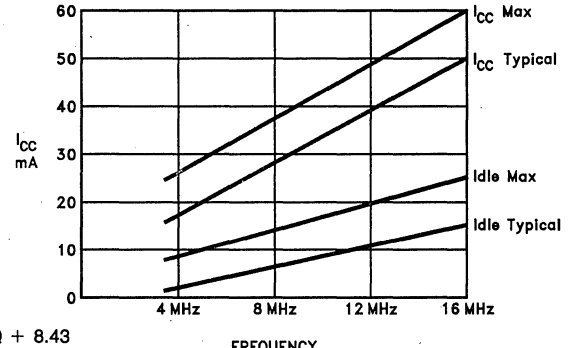
DC CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ(6)	Max	Units	Test Conditions
I_{CC}	Active Mode Current in Reset		50	60	mA	XTAL1 = 16 MHz
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current		10	25	mA	
I_{CC1}	Active Mode Current		15	25	mA	XTAL1 = 3.5 MHz
I_{PD}	Powerdown Mode Current		5	30	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:
(Notes apply to all specifications)
1. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, INST, HSO pins, PWM/P2.5, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
2. Standard Inputs include HSI pins, $\overline{EA}$, READY, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
3. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on Standard Output pins: 10 mA
4. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
5. During normal (non-transient) conditions the following total current limits apply:

HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, $\overline{WR}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST	I_{OL}: 13 mA	I_{OH}: 13 mA

6. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.



I_{CC} Max = 3.88 × FREQ + 8.43
I_{IDLE} Max = 1.65 × FREQ + 2.2

272034-22

Figure 8. I_{CC} and I_{IDLE} vs Frequency

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AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The system must meet these specifications to work with the 87C198:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to Ready Setup		$2T_{OSC} - 75$	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 2)
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. When using wait states, add $2T_{OSC} \times n$, where n = number of wait states.

AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The 87C198 will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 **12 MHz**	3.5	12	MHz	(Note 1)
F_{XTAL}	Frequency on XTAL1 **16 MHz**	3.5	16	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$ **12 MHz**	83.3	286	ns	
T_{OSC}	$1/F_{XTAL}$ **16 MHz**	62.5	286	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 3)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 20		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 35		ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	(Note 3)
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 15	T_{OSC} + 5	ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 15	T_{OSC} + 10	ns	(Note 2)
T_{WHBX}	INST Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{LLBX}	INST Hold after ALE Rising Edge	T_{OSC} − 10		ns	
T_{RHBX}	INST Hold after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 30		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	T_{OSC} − 25		ns	

NOTES:
1. Testing performed at 3.5 MHz. However, the part is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. When using wait states, add 2 T_{OSC} × n, where n = number of wait states.

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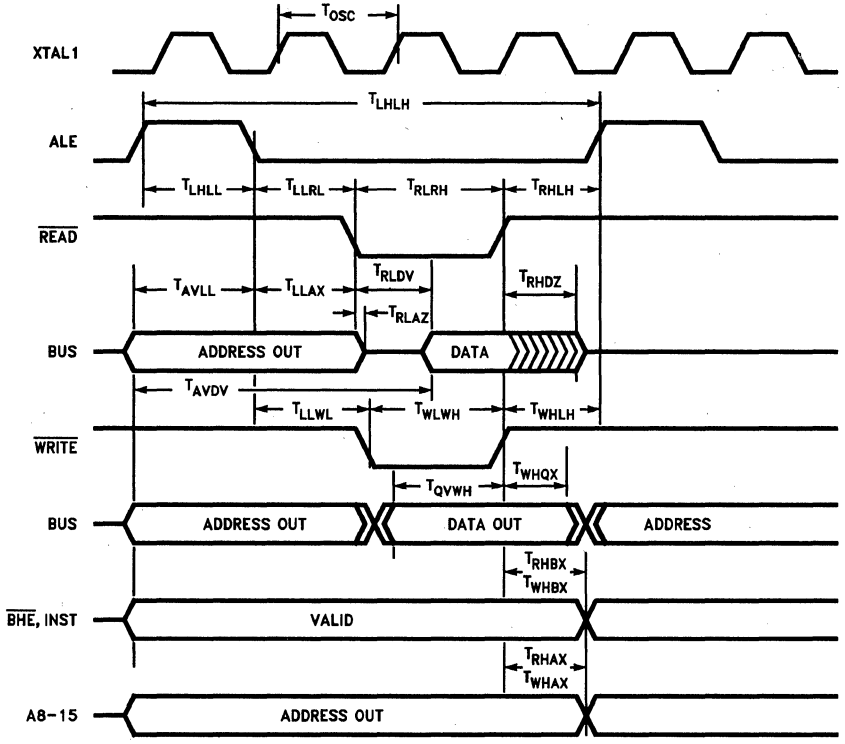
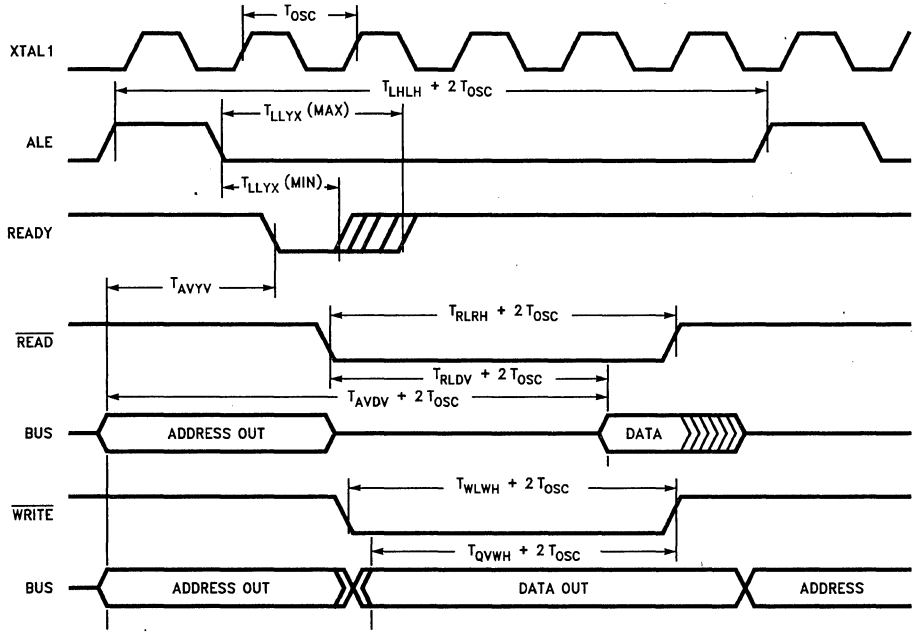
System Bus Timings



READY Timings (One Wait State)



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency **12 MHz**	3.5	12.0	MHz
$1/T_{XLXL}$	Oscillator Frequency **16 MHz**	3.5	16.0	MHz
T_{XLXL}	Oscillator Period **12 MHz**	83.3	286	ns
T_{XLXL}	Oscillator Period **16 MHz**	62.5	286	ns
T_{XHXX}	High Time	21.25		ns
T_{XLXX}	Low Time	21.25		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

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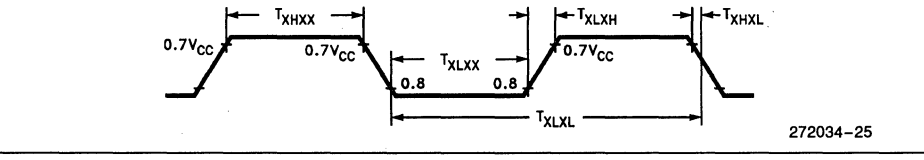
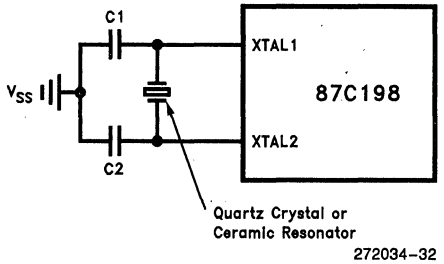
EXTERNAL CLOCK DRIVE WAVEFORMS



An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

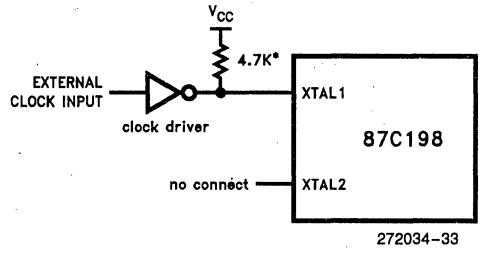
EXTERNAL CRYSTAL CONNECTIONS



272034-32

NOTE:
Keep oscillator components close to chip and use short direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators consult manufacturer for recommended capacitor values.

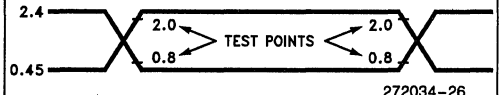
EXTERNAL CLOCK CONNECTIONS



272034-33

NOTE:
*Required if open collector TTL driver used. Not needed if CMOS driver is used.

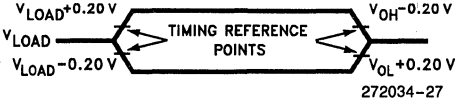
AC TESTING INPUT, OUTPUT WAVEFORMS



272034-26

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



272034-27

For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H - High
L - Low
V - Valid
X - No Longer Valid
Z - Floating

Signals:

A - Address
D - DATA IN
L - ALE/$\overline{ADV}$
Q - DATA OUT
R - $\overline{RD}$
W - $\overline{WR}$
X - XTAL1
Y - READY

10-BIT AID CHARACTERISTICS

At a clock speed of 6 MHz or less, the clock prescaler should be disabled. This is accomplished by setting IOC2.4 = 1.

At higher frequencies (greater than 6 MHz) the clock prescaler should be turned on (IOC2.4 = 0) to allow the comparator to settle.

The table below shows two different clock speeds and their corresponding A/D conversion and sample times.

State times are calculated as follows:

$$\text{state time} = \frac{2}{f_{XTAL1}}$$

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

See the MCS-96 A/D Converter Quick Reference for definition of A/D terms.

Example Sample and Conversion Times

AID Clock Prescaler	Clock Speed (MHz)	Sample Time (States)	Sample Time at Clock Speed (μs)	Conversion Time (States)	Conversion Time at Clock Speed (μs)
IOC2.4 = 0 → ON	16	15	1.875	156.5	19.6
IOC2.4 = 1 → OFF	6	8	2.667	89.5	29.8

A/D CONVERTER SPECIFICATIONS

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ±0.50			LSBs	
Zero Offset Error	−0.25 ±0.50			LSBs	
Non-Linearity Error	1.5 ±2.5	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Time: Prescaler On Prescaler Off	15 8			States States	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages during Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	12.50	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
F_{OSC}	Oscillator Frequency **16 MHz**	6.0	16.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

AC EPROM PROGRAMMING CHARACTERISTICS

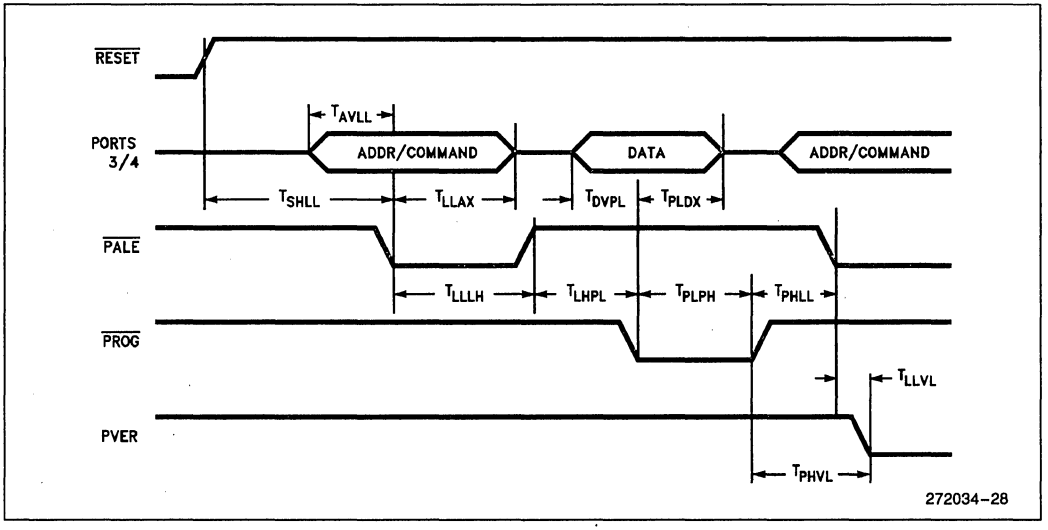
Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	40		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	50		T_{OSC}
T_{LLVL}	$\overline{PALE}$ Low to PVER Low		60	T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	40		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	120		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	120		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	40		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to PVER Low		90	T_{OSC}

DC EPROM PROGRAMMING CHARACTERISTICS

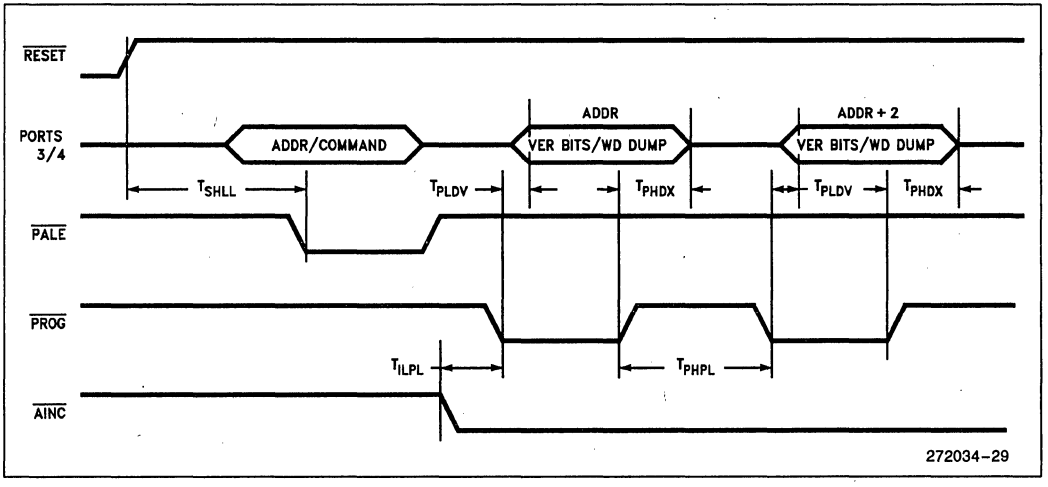
Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



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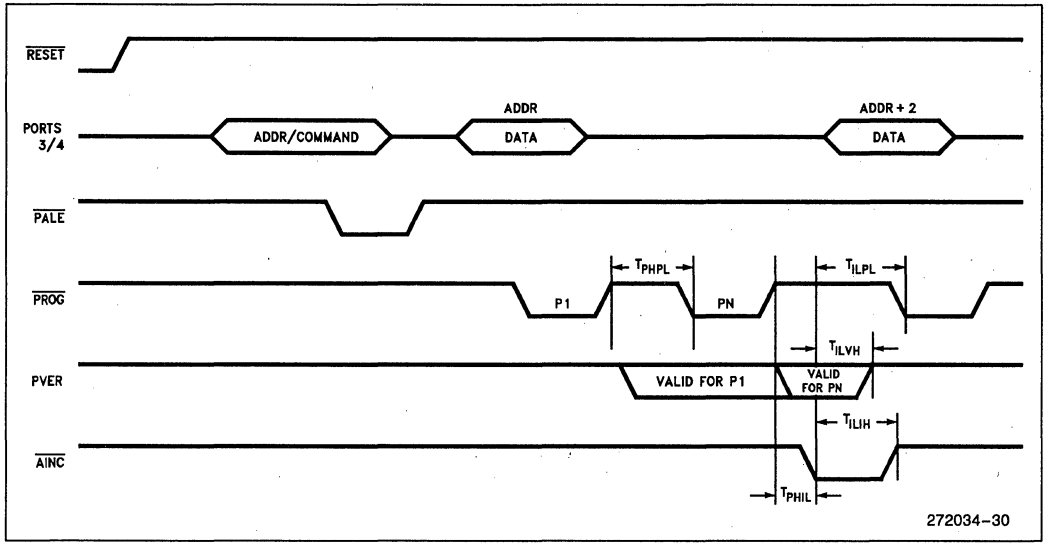
SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



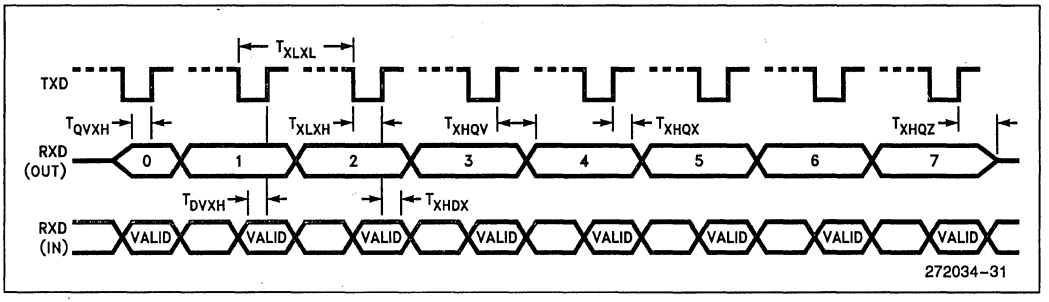
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} + 50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		2 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



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FUNCTIONAL DEVIATIONS

Devices marked with an "E", "F", or "G" have the following errata.

1. HIGH SPEED INPUTS

The High Speed Input (HSI) has three deviations from the specifications.

NOTE:
"Events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine states may be lost.

B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-tag value to be skipped every nine timer counts. Events may receive a time-tag one count later than expected.

C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into an empty FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within 9 states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time-tags will be at least two counts apart.

2. CMPL with R0

Using CMPL with register 0 can set incorrect flags. Don't use register 0 with the compare long instruction. Use another long word register and set it equal to zero. See Techbit MC0692.

REVISION HISTORY

This data sheet (272034-003) is valid for devices marked with an "E", "F", or "G" at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet and the previous version (-002).

1. This data sheet added the ROMless and ROM devices 80C198 and 83C198 respectively.
2. The description of the A/D converter prescalar bit was improved.

8XC196KC Data Sheet

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8XC196KC
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

87C196KC—16 Kbytes of On-Chip EPROM
80C196KC—ROMless

- **16 MHz Operation**
- **232 Byte Register File**
- **256 Bytes of Additional RAM**
- **Register-to-Register Architecture**
- **28 Interrupt Sources/16 Vectors**
- **Peripheral Transaction Server**
- **1.75 μs 16 x 16 Multiply (16 MHz)**
- **3.0 μs 32/16 Divide (16 MHz)**
- **Powerdown and Idle Modes**
- **Five 8-Bit I/O Ports**
- **16-Bit Watchdog Timer**
- **Extended Temperature Available**
- **Dynamically Configurable 8-Bit or 16-Bit Buswidth**
- **Full Duplex Serial Port**
- **High Speed I/O Subsystem**
- **16-Bit Timer**
- **16-Bit Up/Down Counter with Capture**
- **3 Pulse-Width-Modulated Outputs**
- **Four 16-Bit Software Timers**
- **8- or 10-Bit A/D Converter with Sample/Hold**
- **$\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Bus Protocol**
- **OTP One-Time Programmable Version**

The 80C196KC 16-bit microcontroller is a high performance member of the MCS®-96 microcontroller family. The 80C196KC is an enhanced 80C196KB device with 488 bytes RAM, 16 MHz operation and an optional 16 Kbytes of ROM/EPROM. Intel's CHMOS IV process provides a high performance processor along with low power consumption.

The 87C196KC is an 80C196KC with 16 Kbytes on-chip EPROM. In this document, the 80C196KC will refer to all products unless otherwise stated.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended (Express) temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

See the Packaging information for extended temperature designators.

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MCS®-96 is a registered trademark of Intel Corporation.

November 1991
Order Number: 270942-002

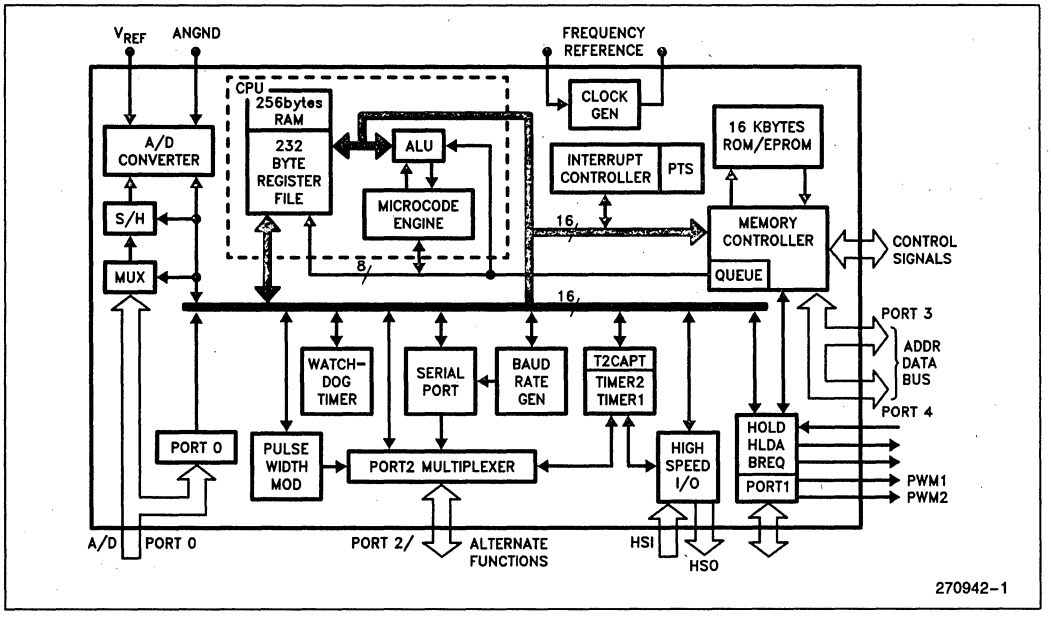

Figure 1. 80C196KC Block Diagram

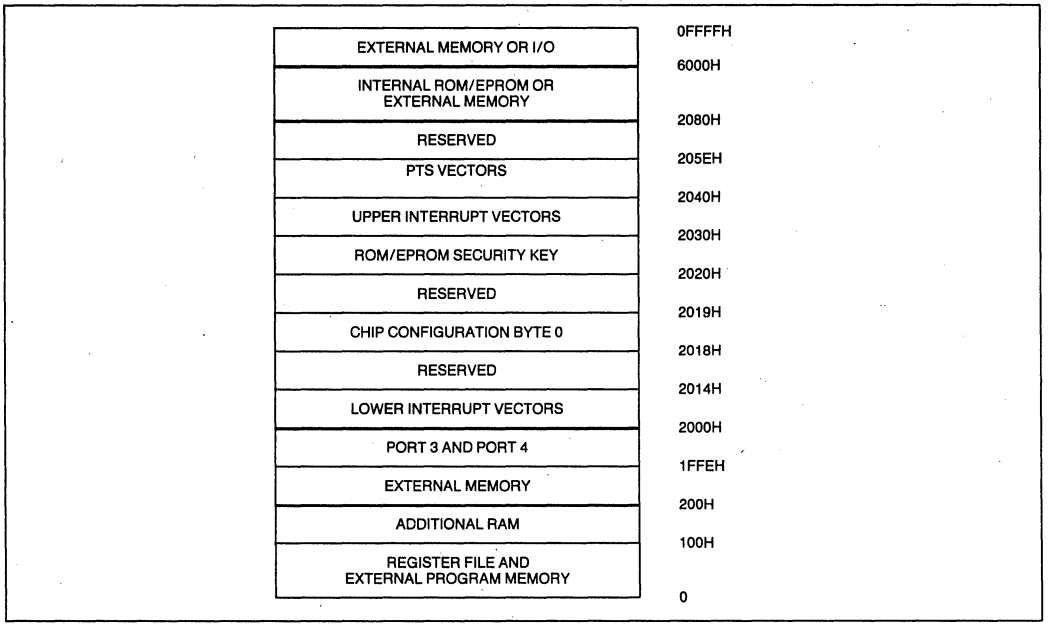

Figure 2. Memory Map

Process Information

This device is manufactured on PX29.5, a CHMOS IV process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* order number 210997.

Table 1. Prefix Identification

Device	Commercial QFP	Commercial PLCC	Express PLCC
80C196KC	S80C196KC	N80C196KC	TN80C196KC
87C196KC	S87C196KC*	N87C196KC*	TN87C196KC*

*OTP Version
Package Designators: N = 68-pin PLCC, S = 80-pin QFP
Prefix Designators: T = Extended Temperature

Table 2. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	42°C/W	—

All thermal data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and applications. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

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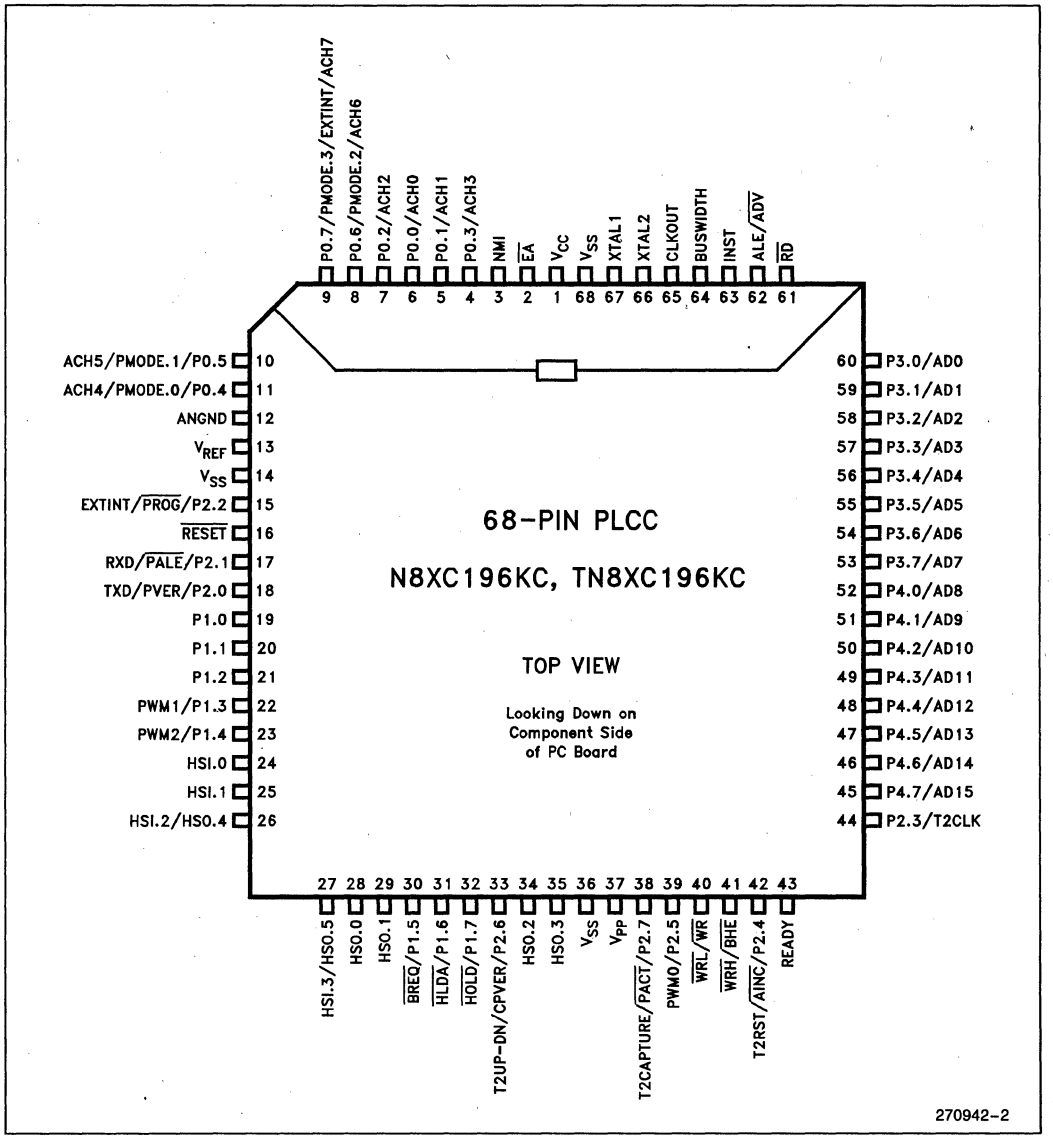

Figure 3. 68-Lead PLCC Package

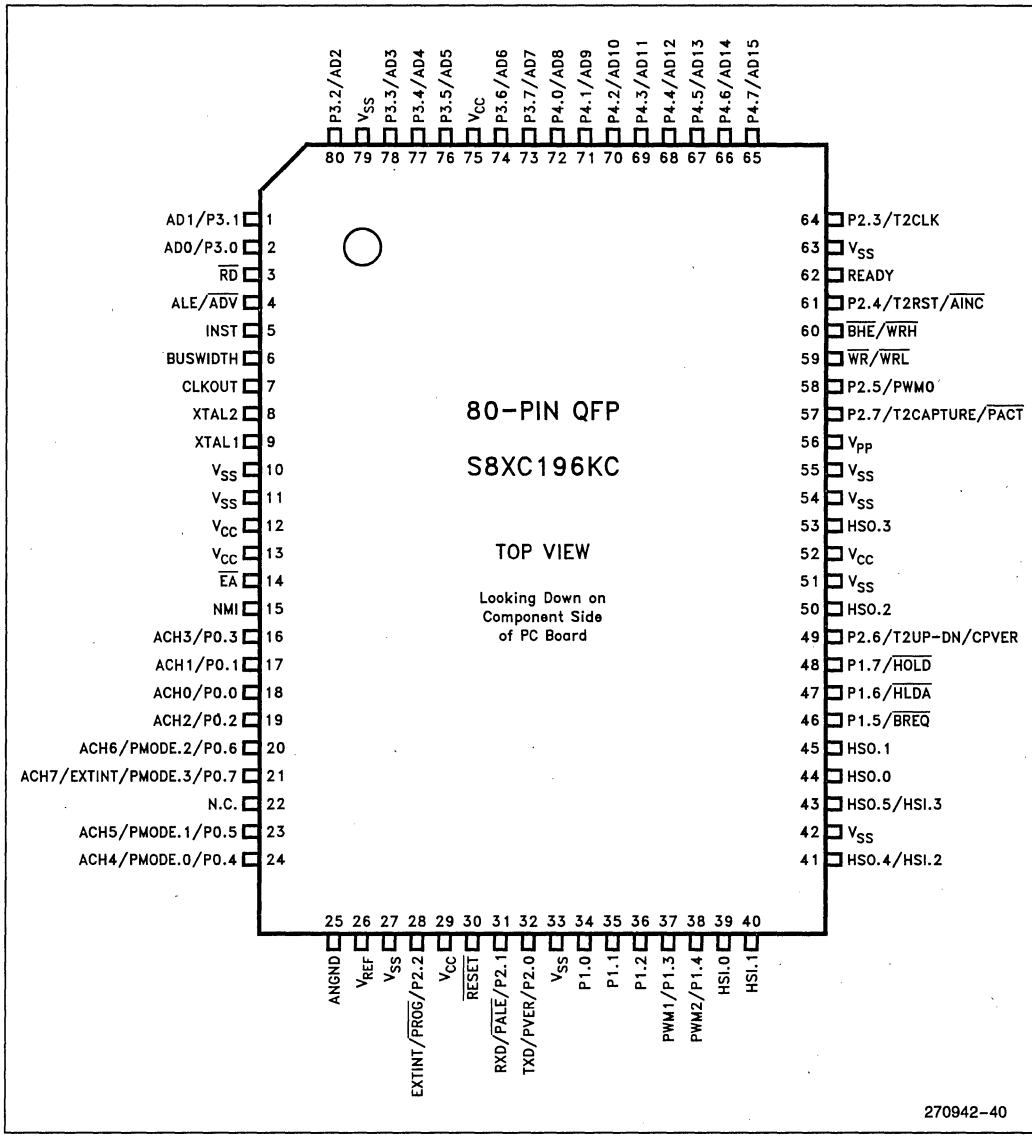

Figure 4. S8XC196KC 80-Pin QFP Package

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PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of which must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used V_{PP} may be tied to V_{CC}. This pin is the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency.
$\overline{\text{RESET}}$	Reset input and open drain output.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal high causes memory accesses to locations 2000H through 5FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to low causes accesses to those locations to be directed to off-chip memory. Also used to enter programming mode.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being written. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 80C196KC. Pins 2.6 and 2.7 are quasi-bidirectional.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
PVAL	A low signal in Auto Programming Mode indicates that the device programmed correctly. A high signal in Slave Programming Mode indicates the device programmed correctly.
$\overline{\text{PALE}}$	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programmig Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
$\overline{\text{AINC}}$	Auto Increment. Active low input signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS} ..... −0.5V to +7.0V(1)
Voltage from $\overline{EA}$ or
V_{PP} to V_{SS} or ANGND ..... +13.00V
Power Dissipation ..... 1.5W(2)

NOTE:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature Under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
F_{OSC}	Oscillator Frequency	8	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.2		V_{CC} + 0.5	V	
V_{HYS}	Hysteresis on $\overline{RESET}$	150			mV	V_{CC} = 5.0V
V_{OL}	Output Low Voltage			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)			0.8	V	I_{OL} = +0.4 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA

DC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -10\ \mu A$ $I_{OH} = -30\ \mu A$ $I_{OH} = -60\ \mu A$
I_{OH1}	Logical 1 Output Current in Reset. Do not exceed this or device may enter test modes.	−0.8			mA	$V_{IH} = V_{CC} - 1.5V$
I_{IL1}	Logical 0 Input Current in Reset. Maximum current that must be sunk by external device to ensure test mode entry.			−6.0	mA	$V_{IN} = 0.45V$
I_{IH1}	Logical 1 Input Current. Maximum current that external device must source to initiate NMI.			+100	μA	$V_{IN} = V_{CC} = 5.5V$
I_{LI}	Input Leakage Current (Std. Inputs)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	μA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	μA	$V_{IN} = 0.45V$
I_{IL1}	Ports 3 and 4 in Reset			−70	μA	$V_{IN} = 0.45V$
I_{CC}	Active Mode Current in Reset		50	70	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Converter Reference Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	
I_{PD}	Powerdown Mode Current		15	TBD	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	$V_{CC} = 5.5V, V_{IN} = 4.0V$
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
1. All pins except RESET and XTAL1.
2. Violating these specifications in Reset may cause the part to enter test modes.
3. Commercial specifications apply to express parts except where noted.
4. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
5. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
6. Standard Inputs include HSI pins, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
7. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below $V_{CC} - 0.7V$:
   - I_{OL} on Output pins: 10 mA
   - I_{OH} on quasi-bidirectional pins: self limiting
   - I_{OH} on Standard Output pins: 10 mA
8. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
9. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

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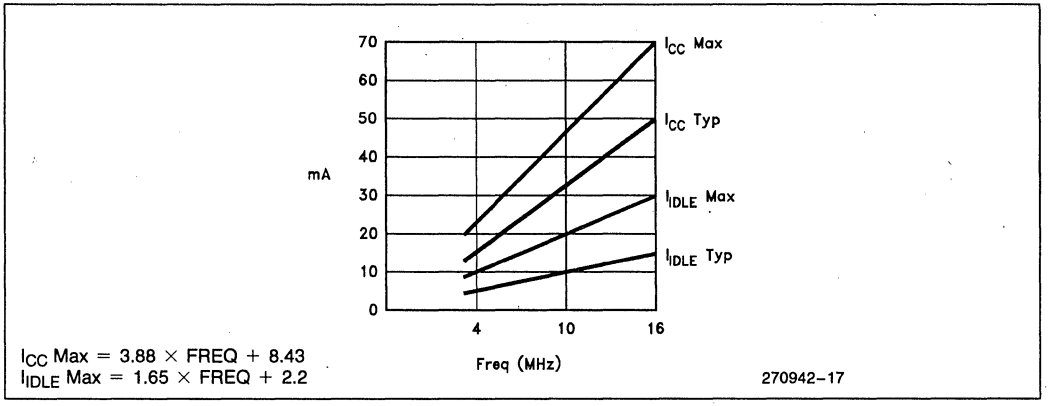


Figure 5. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 80C196KC:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 68$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 68$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 60$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 22$	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

AC CHARACTERISTICS (Continued)

For user over specified operating conditions.

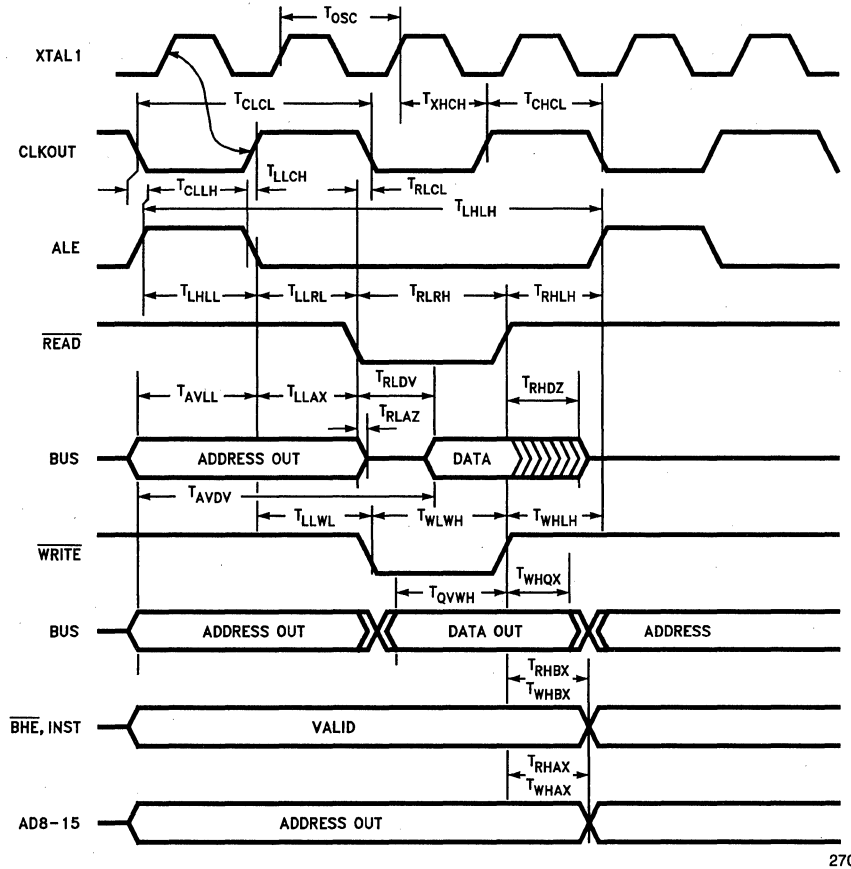
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The 80C196KC will meet these specifications:

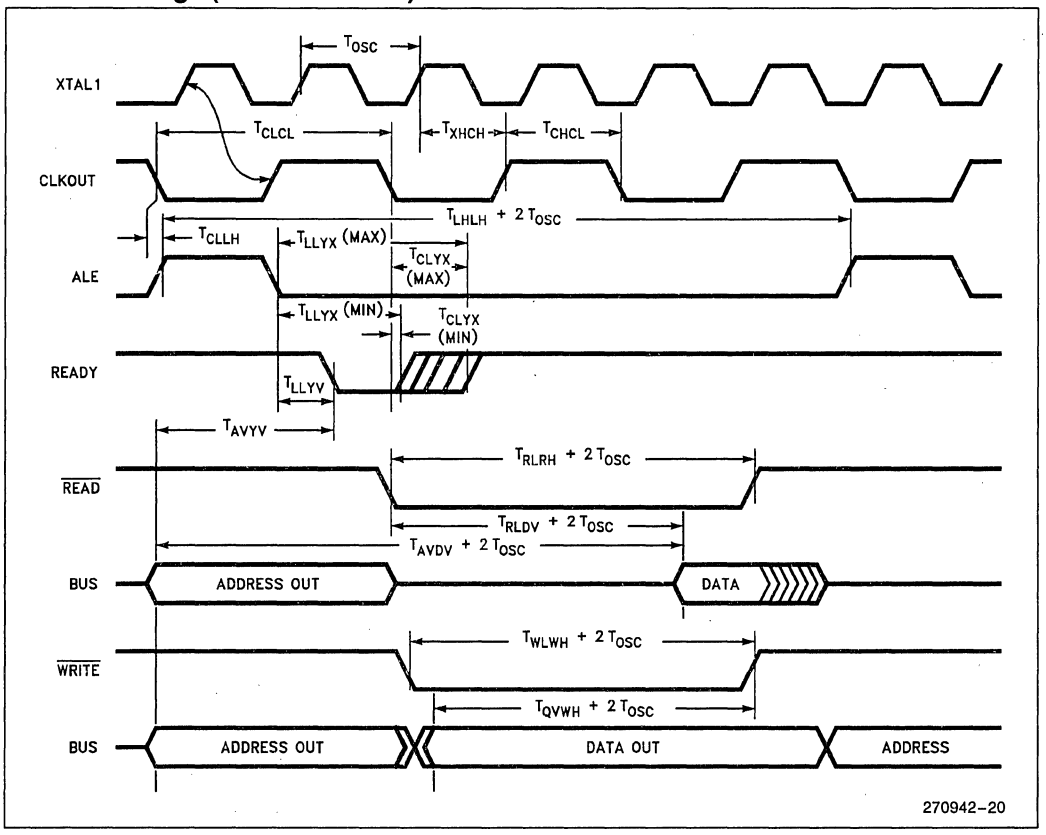
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on $XTAL_1$	8	16	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$	62.5	125	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	$T_{OSC}-10$	$T_{OSC}+15$	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 4)
T_{LHLL}	ALE High Period	$T_{OSC}-10$	$T_{OSC}+10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC}-15$			
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC}-40$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC}-30$		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC}-5$		ns	(Note 4)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	$T_{OSC}+25$	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC}-10$		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC}-23$			(Note 4)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC}-20$		ns	(Note 4)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-25$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC}-10$	$T_{OSC}+15$	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	$T_{OSC}-10$		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	$T_{OSC}-30$		ns	(Note 3)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	$T_{OSC}-10$		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	$T_{OSC}-30$		ns	(Note 3)

NOTES:
1. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. 8-Bit bus only.
4. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

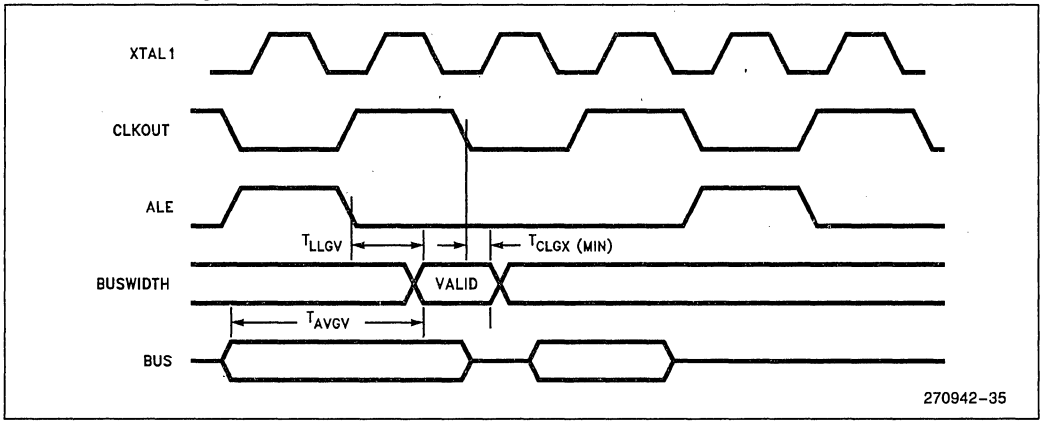
System Bus Timings



READY Timings (One Wait State)



Buswidth Timings



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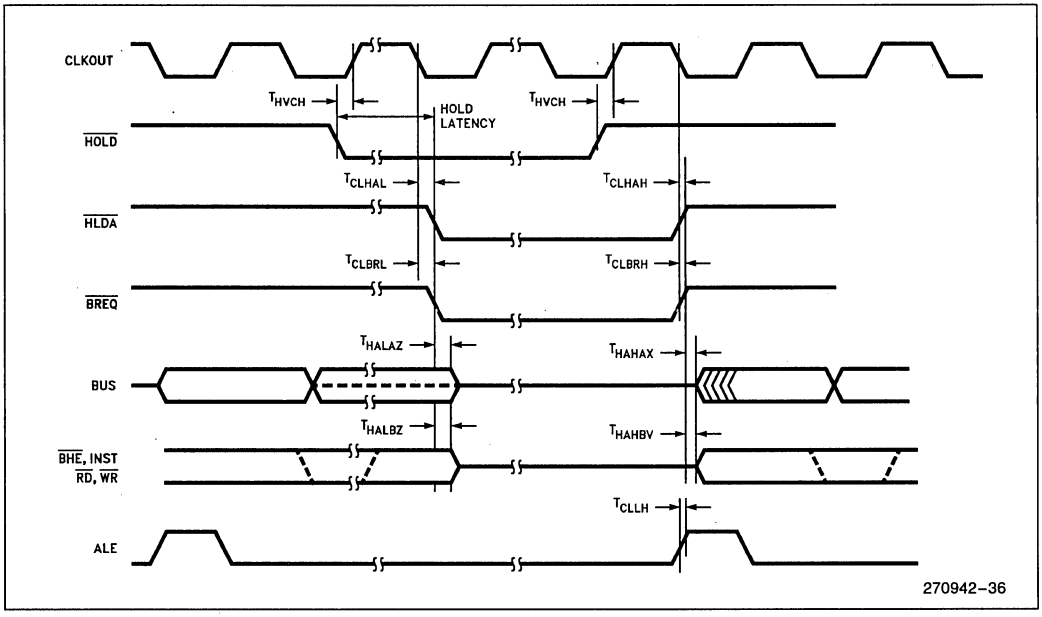
$\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	$\overline{\text{HOLD}}$ Setup	55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to $\overline{\text{HLDA}}$ Low	−15	15	ns	
T_{CLBRL}	CLKOUT Low to $\overline{\text{BREQ}}$ Low	−15	15	ns	
T_{HALAZ}	$\overline{\text{HLDA}}$ Low to Address Float		10	ns	
T_{HALBZ}	$\overline{\text{HLDA}}$ Low to $\overline{\text{BHE}}$, INST, $\overline{\text{RD}}$, $\overline{\text{WR}}$ Weakly Driven		15	ns	
T_{CLHAH}	CLKOUT Low to $\overline{\text{HLDA}}$ High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to $\overline{\text{BREQ}}$ High	−15	15	ns	
T_{HAHAX}	$\overline{\text{HLDA}}$ High to Address No Longer Float	−15		ns	
T_{HAHBV}	$\overline{\text{HLDA}}$ High to BHE, INST, RD, WR Valid	−10		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

NOTE:
1. To guarantee recognition at next clock.

DC SPECIFICATIONS IN HOLD

Description	Min	Max	Units
Weak Pullups on $\overline{\text{ADV}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{WRL}}$, $\overline{\text{BHE}}$	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4



Maximum Hold Latency

Bus Cycle Type	
Internal Execution	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

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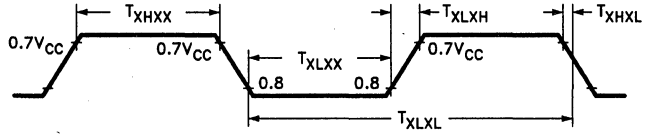
EXTERNAL CLOCK DRIVE

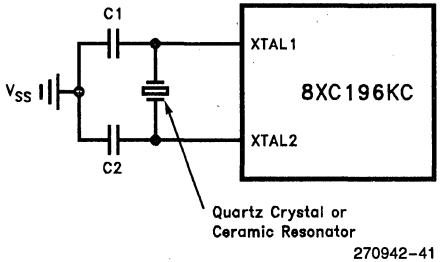
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	20		ns
T_{XLXX}	Low Time	20		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



270942-21

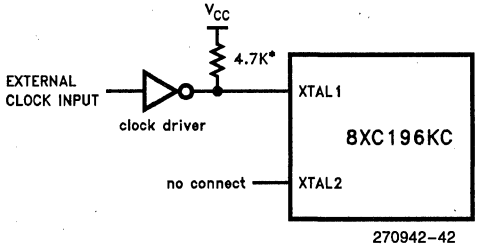
EXTERNAL CRYSTAL CONNECTIONS



270942-41

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = C2 ≈ 20 pF. When using ceramic resonators, consult manufacturer for recommended capacitor values.

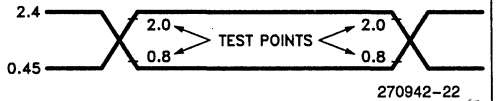
EXTERNAL CLOCK CONNECTIONS



270942-42

NOTE:
*Required if TTL driver used.
Not needed if CMOS driver is used.

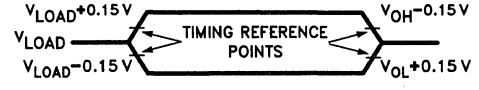
AC TESTING INPUT, OUTPUT WAVEFORMS



270942-22

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



270942-23

For Timing Purposes a Port Pin is no Longer Floating when a 150 mV change from Load Voltage Occurs and Begins to Float when a 150 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
BR— $\overline{BREQ}$
R— $\overline{RD}$
W— $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X— XTAL1
Y— READY
Q— Data Out

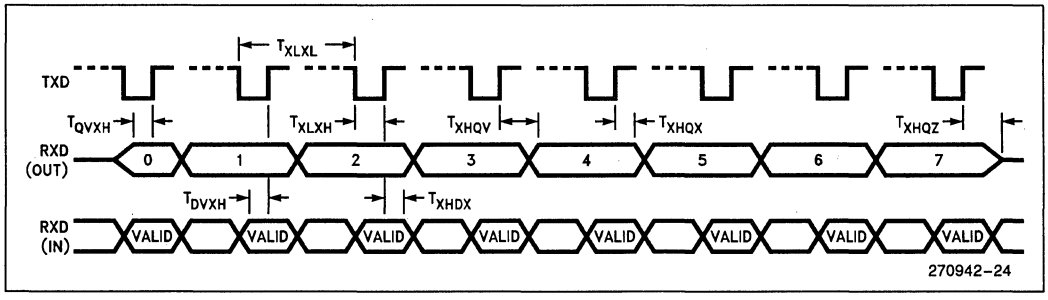
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} −50	4 T_{OSC} +50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} −50	2 T_{OSC} +50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



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A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
T_{SAM}	Sample Time	3.0		µs(1)
T_{CONV}	Conversion Time	10	20	µs(1)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTE:
ANGND and V_{SS} should nominally be at the same potential, 0.00V.
1. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Non-Linearity	1.0 ± 2.0	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 2
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	µA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approxiimately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of all channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
T_{SAM}	Sample Time	2.0		μs(1)
T_{CONV}	Conversion Time	7	20	μs(1)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTE:
ANGND and V_{SS} should nominally be at the same potential, 0.00V.
1. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±1	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±1	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ωs	4
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of all channels being converted.
7. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency During Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency During Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

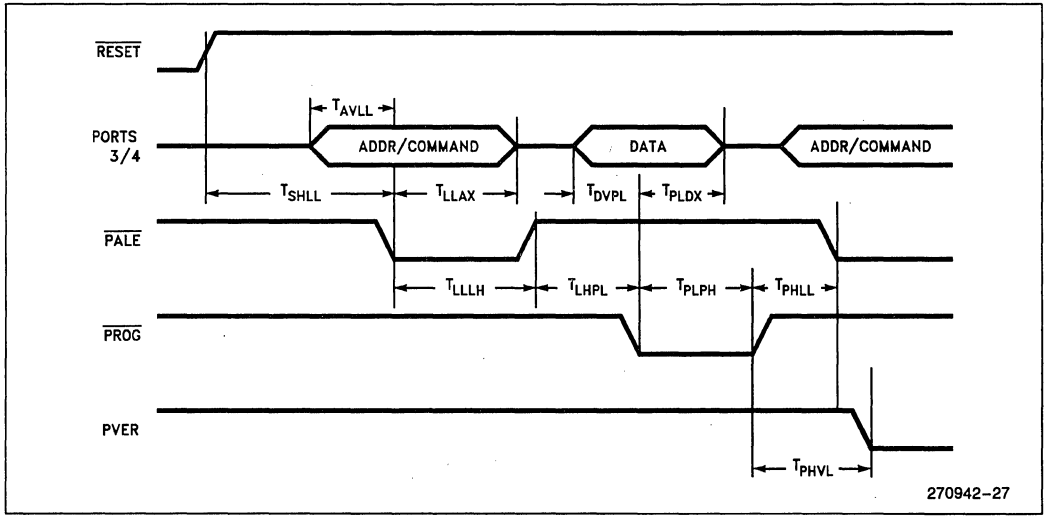
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

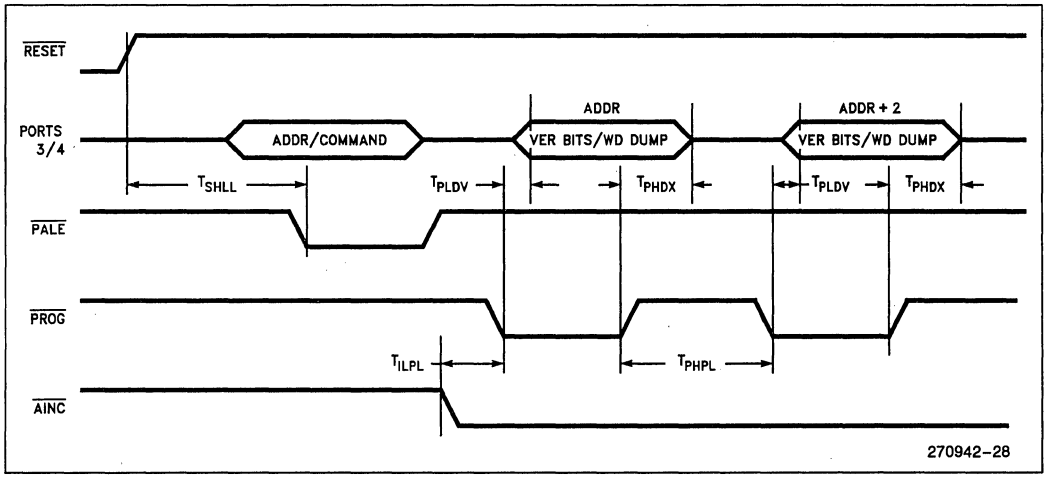
NOTE:
V_{PP} must be within 1V of V_{CC} while V_{CC} < 4.5V. V_{PP} must not have a low impedance path to ground of V_{SS} while V_{CC} > 4.5V.

EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



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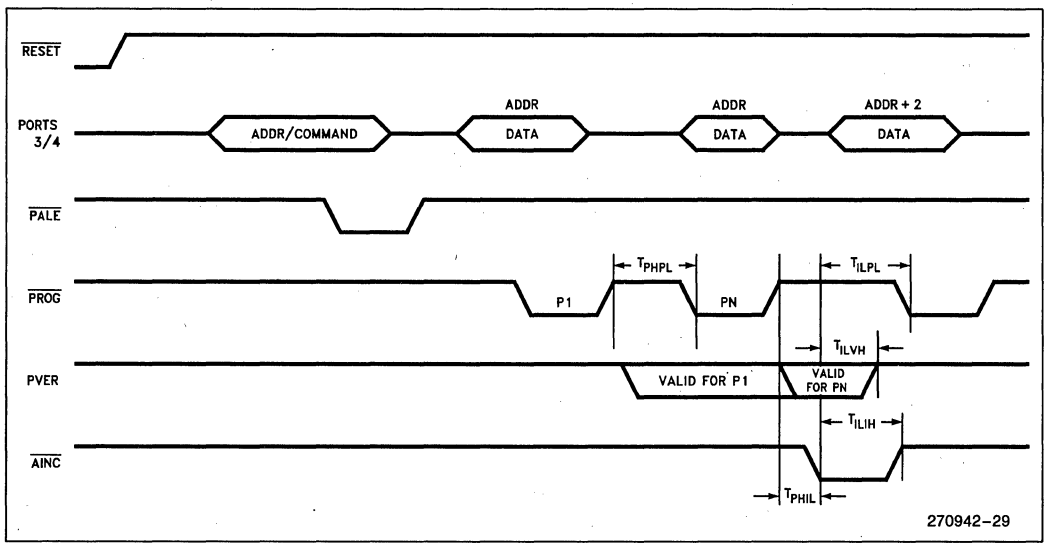
SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



80C196KB TO 80C196KC DESIGN CONSIDERATIONS

1. Memory Map. The 80C196KC has 512 bytes of RAM/SFRs and 16K of ROM/EPROM. The extra 256 bytes of RAM will reside in locations 100H–1FFH and the extra 8K of ROM/EPROM will reside in locations 4000H–5FFFH. These locations are external memory on the 80C196KB.
2. The CDE pin on the KB has become a V_{SS} pin on the KC to support 16 MHz operation.
3. EPROM programming. The 80C196KC has a different programming algorithm to support 16K of on-board memory. When performing Run-Time Programming, use the section of code on page 99 of the 80C196KC User's Guide, order number 270704-003.
4. ONCE™ Mode Entry. The ONCE mode is entered on the 80C196KC by driving the TXD pin low on the rising edge of RESET. The TXD pin is held high by a pullup that is specified at 1.4 mA and remain at 2.0V. This Pullup must not be overridden or the 80C196KC will enter the ONCE mode.
5. During the bus HOLD state, the 80C196KC weakly holds RD, WR, ALE, BHE and INST in their inactive states. The 80C196KB only holds ALE in its inactive state.
6. A RESET pulse from the 80C196KC is 16 states rather than 4 states as on the 80C196KB (i.e., a watchdog timer overflow). This provides a longer RESET pulse for other devices in the system.

80C196KC ERRATA

1. NMI during PTS skips an address: When an NMI interrupts a PTS routine, the first byte of the instruction following completion of the PTS cycle is lost. This results in incorrect code execution. Workaround: NMI must be disabled using external hardware during any PTS activity.
2. QBD port glitch. There is a strong negative glitch on all QBD Port pins (P1.x and P2.6, P2.7) synchronous with the first falling edge of CLKOUT. This glitch lasts about 10 ns, and only occurs one time following initial application of V_{CC}. The time for the pin to return to V_{CC} may be several microseconds, depending on pin loading capacitance. Workaround: External systems and devices should be disabled from responding to this glitch until after the first CLKOUT falling edge has occurred.
3. Divide error during HOLD or READY. The result of a signed divide instruction may be off by one if executed while the device is held off the bus by HOLD or READY and the queue is empty. Specific timings of HOLD or READY going active or inactive must be met. Workaround for HOLD: disable HOLD during signed divide operations (using hardware or software). Workaround for READY: problem will only occur if unlimited wait state mode is selected, and 14 or more wait states are inserted.
4. The HSI unit has two errata: one dealing with resolution and the other with first entries into the FIFO.

The HSI resolution is 9 states instead of 8 states. Events on the same line may be lost if they occur faster than once every 9 state times.

There is a mismatch between the 9 state time HSI resolution and the 8 state time timer. This causes one time value to be unused every 9 timer counts.

Events may receive a time-tag on one count later than expected because of this "skipped" time value.

If the first two events into an empty FIFO (not including the Holding Register) occur in the same internal phase, both are recorded with one time-tag. Otherwise, if the second event occurs within 9 states after the first, its time-tag is one count later than the first time tag. If this is the "skipped" time value, the second event's time-tag is 2 counts later than the first's.

If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register after 8 state times, leaving the FIFO empty again. If the second event occurs after this time, it will act as a new first event into an empty FIFO.

DATA SHEET REVISION HISTORY

This data sheet is valid for devices with a "D" or "E" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are the important differences between the -001 and -002 versions of data sheet 270942.

1. Express and Commercial devices are combined into one data sheet. The Express only data sheet 270794-001 is obsolete.
2. Removed KB/KC feature set differences, pin definition table, and SFR locations and bitmaps.
3. Added programming pin function to package drawings and pin descriptions.
4. Changed absolute maximum temperature under bias from 0°C to +70°C to −55°C to +125°C.
5. Replaced V_{OH2} specification with I_{OH1} and I_{IL1} specifications.
6. Added I_{IH1} specification for NMI pulldown resistors.
7. Added maximum hold latency table.
8. Added external oscillator and external clock circuit drawings.
9. Changed Clock Drive T_{XHXX} and T_{XLXX} Min spec to 20 ns.
10. Fixed Serial Port T_{XLXH} specification.
11. Added 8- and 10-bit mode A/D operating conditions tables.
12. Specified operating range for sample and convert times.
13. Added specification for voltage on analog input pin.
14. Put operating conditions for EPROM programming into tabular format.

The following differences exist between data sheet 270942-001 and 270741-003.

1. ONCE MODE V_{IL} errata removed.
2. V_{REF} Min changed from 4.5V to 4.0V.

The following differences exist between the -002 and -003 versions of data sheet 270741.

1. 80-Pin QFP package added, 68-pin Cerquad package deleted.
2. The following DC Characteristics were added:
   V_{HYS} $\overline{\text{RESET}}$ Hysteresis spec added
   I_{IL1}, AD BUS in RESET current Max added

DATA SHEET REVISION HISTORY (Continued)

3. The following AC Characteristics were changed:

   T_{AVYV} Max from $2T_{OSC}$-75 to $2T_{OSC}$-68

   T_{AVGV} Max from $2T_{OSC}$-75 to $2T_{OSC}$-68

   T_{WLWH} Min from T_{OSC}-30 to T_{OSC}-20

   T_{XHCH} Min changed from 30 ns to 20 ns

   T_{HALBZ} Max changed from 10 ns to 15 ns

4. Under 10-bit A/D Characteristics:

   Sample Time/Convert Time Testing Conditions added.

   Typical values added for Full Scale Error, Zero Offset Error, Non-Linearity and Channel-to-Channel Matching.

   Max Absolute Error changed from ±8 to ±3 LSBs

   Max Non-Linearity changed from ±8 to ±3 LSBs

5. Under 8-bit Mode A/D Characteristics:

   Max Absolute Error changed from ±2 to ±1 LSBs

   Max Non-Linearity changed from ±2 to ±1 LSBs

   Typical Full Scale Error changed from ±1 to ±0.5 LSBs

   Typical Zero Offset Error changed from ±2 to ±0.5 LSBs

6. The minimum frequency at which the device is tested was changed to 8.0 MHz from 3.5 MHz. Thus, data sheet specifications are guaranteed from 8 MHz to 16 MHz. However, the device is static and will function below 1 Hz.
7. The T2CONTROL (T2CNTC) SFR was renamed IOC3.
8. ONCE MODE V_{IL} errata added. Other errata removed.
9. The A-Step device corresponding to data sheet 270741-002 had bits IOC1.4 and IOC1.6 reversed. The problem was corrected in the B-1 Step device corresponding to data sheet 270741-003.

The following are the important differences between the -001 and -002 versions of data sheet 270741. Please review this revision history carefully.

1. The 83C196KC (ROM) was added to the product line.
2. The OTP version of the EPROM was added to the product line.
3. $\overline{HOLD}/\overline{HLDA}$ Specifications were added.
4. The I_{OL} test condition on V_{OL1} has changed to −0.5 mA from −0.4 mA.
5. The I_{OH} test condition V_{OH2} has changed to 0.8 mA from 1.4 mA.
6. BMOVi errata was added.
7. Errata was added for the HSI resolution and first event anomalies.
8. Errata was added for the serial port Framing Error anomaly.

8XC196KD Data Sheets 18

8XC196KD/8XC196KD20
COMMERCIAL CHMOS MICROCONTROLLER

87C196KD—32 Kbytes of On-Chip OTPROM

- **16 MHz and 20 MHz Available**
- **1000 Byte Register RAM**
- **Register-to-Register Architecture**
- **28 Interrupt Sources/16 Vectors**
- **Peripheral Transaction Server**
- **1.4 μs 16 x 16 Multiply (20 MHz)**
- **2.4 μs 32/16 Divide (20 MHz)**
- **Powerdown and Idle Modes**
- **Five 8-Bit I/O Ports**
- **16-Bit Watchdog Timer**
- **Dynamically Configurable 8-Bit or 16-Bit Buswidth**
- **Full Duplex Serial Port**
- **High Speed I/O Subsystem**
- **16-Bit Timer**
- **16-Bit Up/Down Counter with Capture**
- **3 Pulse-Width-Modulated Outputs**
- **Four 16-Bit Software Timers**
- **8- or 10-Bit A/D Converter with Sample/Hold**
- **$\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ Bus Protocol**
- **OTP One-Time Programmable Version**

The 8XC196KD 16-bit microcontroller is a high performance member of the MCS®-96 microcontroller family. The 8XC196KD is an enhanced 80C196KC device with 1000 bytes RAM, 16 MHz operation and an optional 32 Kbytes of ROM/EPROM. Intel's CHMOS III-E process provides a high performance processor along with low power consumption.

The 8XC196KD has a maximum guaranteed frequency of 16 MHz. The 8XC196KD20 has a maximum guaranteed frequency of 20 MHz. Unless otherwise noted, all references to the 8XC196KD also refer to the 8XC196KD20.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

June 1992
Order Number: 272145-002

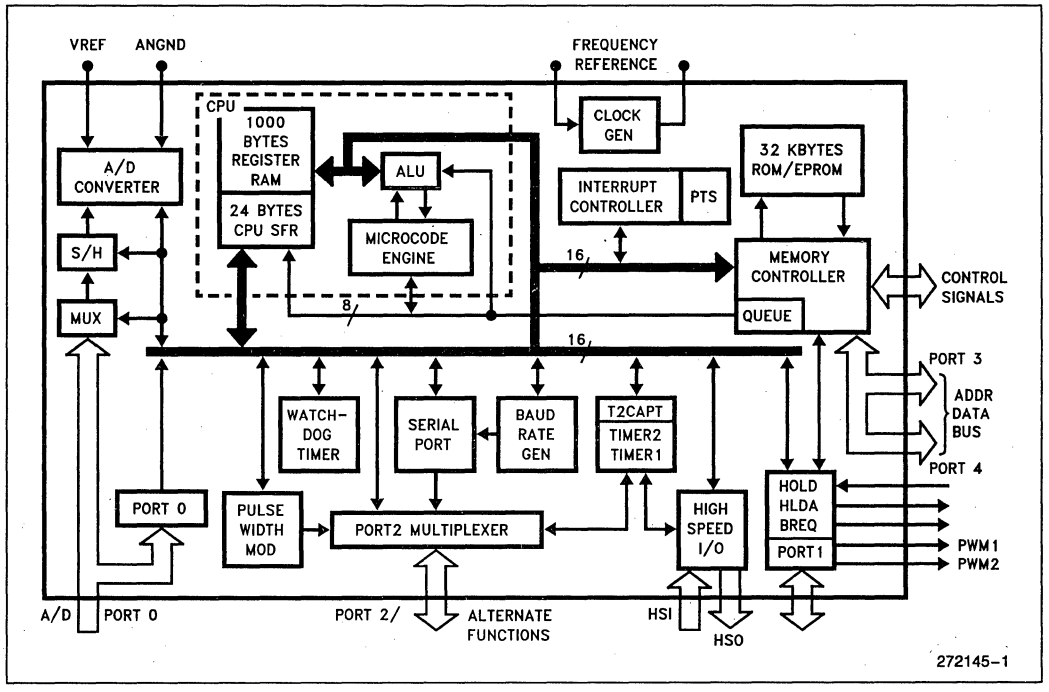
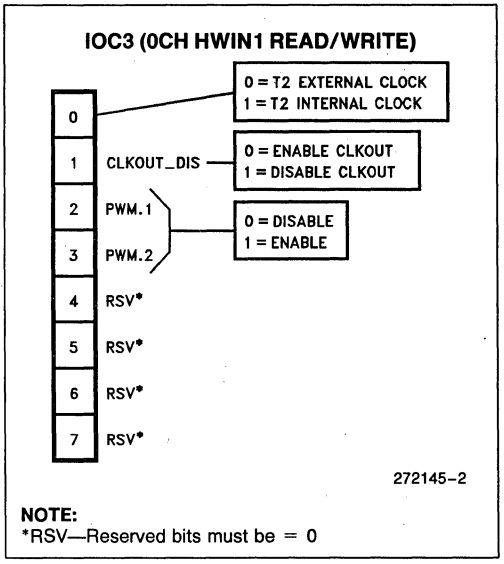


Figure 1. 8XC196KD Block Diagram

87C196KD ENHANCED FEATURE SET OVER THE 87C196KC

1. The 87C196KD has twice the RAM and twice the OTPROM space of the 87C196KC.
2. The vertical windowing scheme has been extended to allow all 1000 bytes of register RAM to be windowed into the lower register file.
3. A CLKOUT disable bit has been added to the IOC3 SFR. This can be used to reduce noise in systems not requiring the CLKOUT signal.



NOTE:
*RSV—Reserved bits must be = 0

Figure 2. 87C196KD New SFR Bit (CLKOUT Disable)

8XC196KD VERTICAL WINDOWING MAP

Table 1. 128-Byte Windows

Address to Remap	Device Series	WSR Contents
0380H	KD	X001 0111B = 17H
0300H	KD	X001 0110B = 16H
0280H	KD	X001 0101B = 15H
0200H	KD	X001 0100B = 14H
0180H	KC, KD	X001 0011B = 13H
0100H	KC, KD	X001 0010B = 12H
0080H	KC, KD	X001 0001B = 11H
0000H	KC, KD	X001 0000B = 10H

Window in Lower Register File: 80H–FFH

Table 2. 64-Byte Windows

Address to Remap	Device Series	WSR Contents
03C0H	KD	X010 1111B = 2FH
0380H	KD	X010 1110B = 2EH
0340H	KD	X010 1101B = 2DH
0300H	KD	X010 1100B = 2CH
02C0H	KD	X010 1011B = 2BH
0280H	KD	X010 1010B = 2AH
0240H	KD	X010 1001B = 29H
0200H	KD	X010 1000B = 28H
01C0H	KC, KD	X010 0111B = 27H
0180H	KC, KD	X010 0110B = 26H
0140H	KC, KD	X010 0101B = 25H
0100H	KC, KD	X010 0100B = 24H
00C0H	KC, KD	X010 0011B = 23H
0080H	KC, KD	X010 0010B = 22H
0040H	KC, KD	X010 0001B = 21H
0000H	KC, KD	X010 0000B = 20H

Window in Lower Register File: C0H–FFH

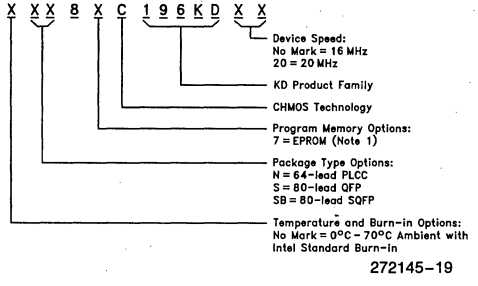
Table 3. 32-Byte Windows

Address to Remap	Device Series	WSR Contents
03E0H	KD	X101 1111B = 5FH
03C0H	KD	X101 1110B = 5EH
03A0H	KD	X101 1101B = 5DH
0380H	KD	X101 1100B = 5CH
0360H	KD	X101 1011B = 5BH
0340H	KD	X101 1010B = 5AH
0320H	KD	X101 1001B = 59H
0300H	KD	X101 1000B = 58H
02E0H	KD	X101 0111B = 57H
02C0H	KD	X101 0110B = 56H
02A0H	KD	X101 0101B = 55H
0280H	KD	X101 0100B = 54H
0260H	KD	X101 0011B = 53H
0240H	KD	X101 0010B = 52H
0220H	KD	X101 0001B = 51H
0200H	KD	X101 0000B = 50H
01E0H	KC, KD	X100 1111B = 4FH
01C0H	KC, KD	X100 1110B = 4EH
01A0H	KC, KD	X100 1101B = 4DH
0180H	KC, KD	X100 1100B = 4CH
0160H	KC, KD	X100 1011B = 4BH
0140H	KC, KD	X100 1010B = 4AH
0120H	KC, KD	X100 1001B = 49H
0100H	KC, KD	X100 1000B = 48H
00E0H	KC, KD	X100 0111B = 47H
00C0H	KC, KD	X100 0110B = 46H
00A0H	KC, KD	X100 0101B = 45H
0080H	KC, KD	X100 0100B = 44H
0060H	KC, KD	X100 0011B = 43H
0040H	KC, KD	X100 0010B = 42H
0020H	KC, KD	X100 0001B = 41H
0000H	KC, KD	X100 0000B = 40H

Window in Lower Register File: E0H–FFH

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196KD20 is 68-Lead PLCC OTPROM, 20 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 3. The 8XC196KD Family Nomenclature

Table 4. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	56°C/W	12°C/W
SQFP	TBD	TBD

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 5. 8XC196KD Memory Map

Description	Address
External Memory or I/O	0FFFFH 0A000H
Internal ROM/EPROM or External Memory (Determined by $\overline{EA}$)	9FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4 Word Addressable Only	1FFFH 1FFEH
External Memory	1FFDH 0400H
1000 Bytes Register RAM (Note 1)	03FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 03FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KC for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

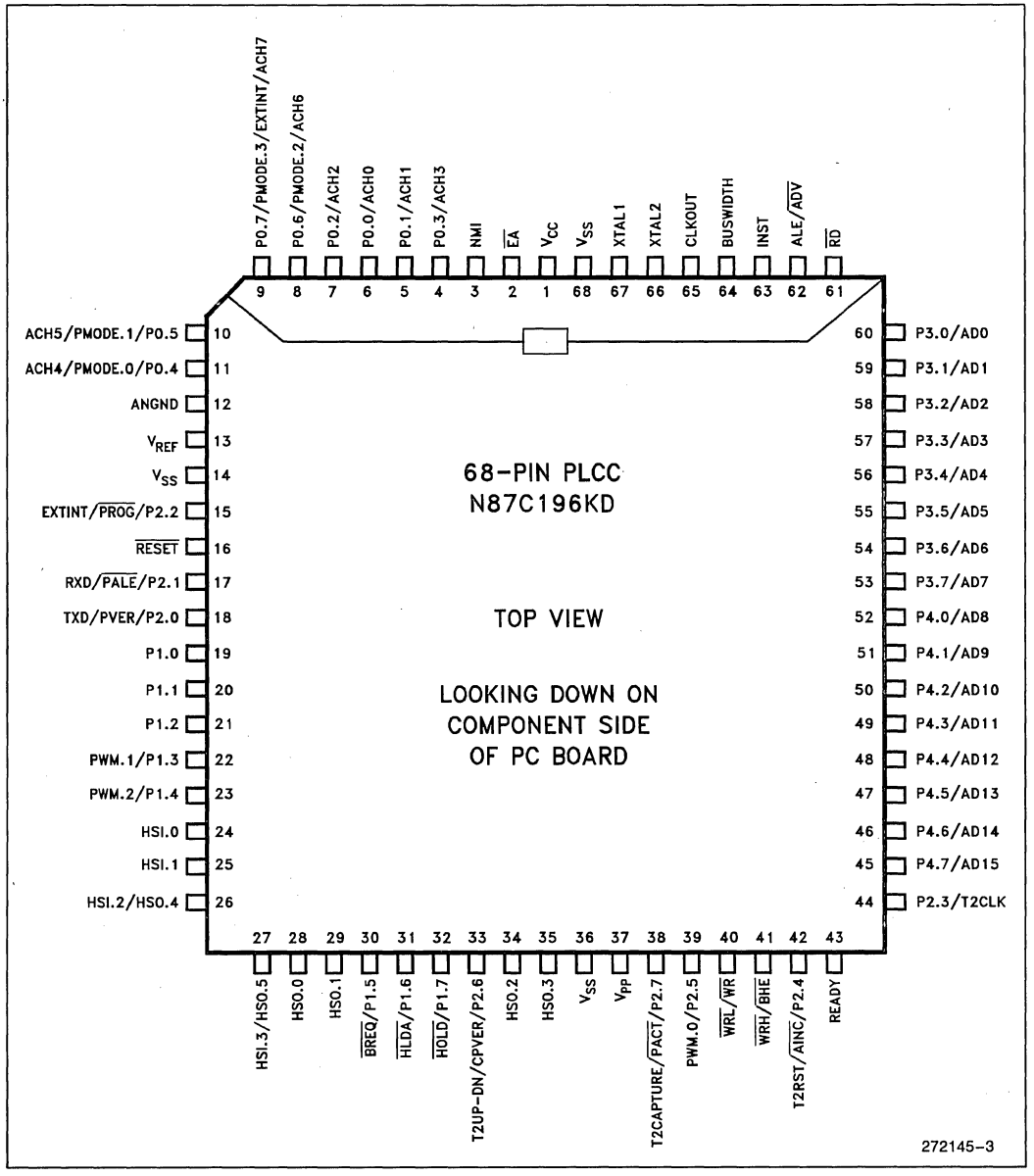


Figure 4. 68-Pin PLCC Package

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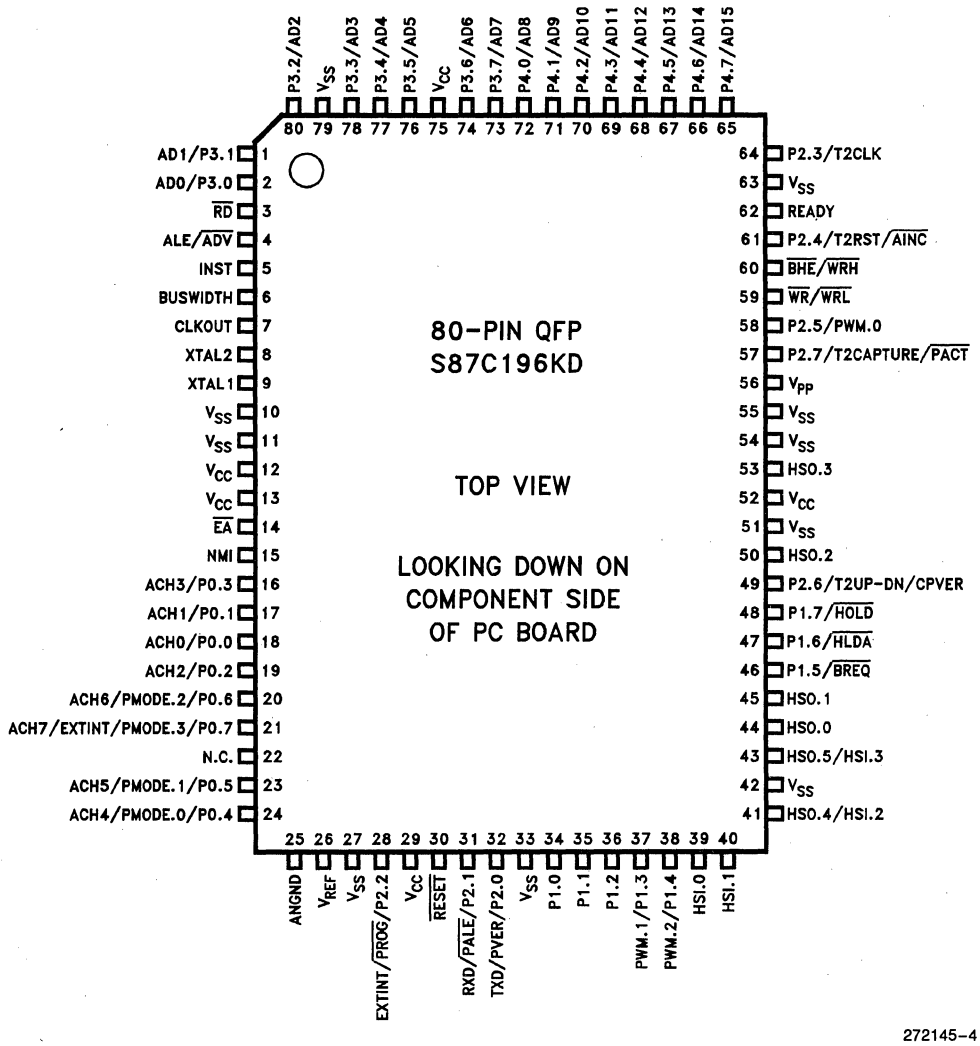
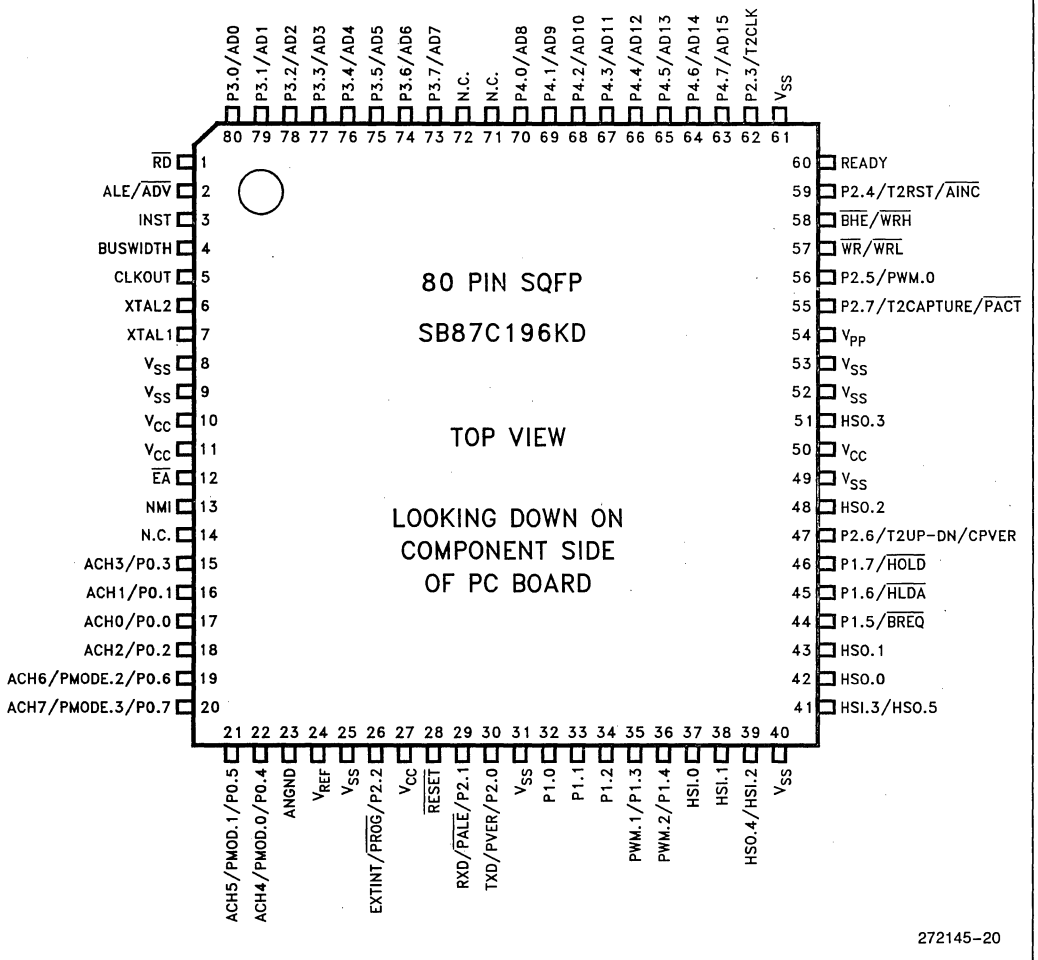


NOTE:
N.C. means No Connect (do not connect these pins).

Figure 5. 80-Pin QFP Package



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 6. 80-Pin SQFP Package

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PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of which must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. This pin also supplies the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency.
$\overline{\text{RESET}}$	Reset input and open drain output.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal high causes memory accesses to locations 2000H through 9FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal low causes accesses to those locations to be directed to off-chip memory. Also used to enter programming mode.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being written. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 80C196KD. Pins 2.6 and 2.7 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
$\overline{\text{PALE}}$	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
CPVER	Cummulative Program Output Verification. Pin is high if all locations have programmed correctly since entering a programming mode.
$\overline{\text{AINC}}$	Auto Increment. Active low input enables the auto increment mode. Auto increment allows reading or writing sequential EPROM locations without address transactions across the PBUS for each read or write.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS}
Except EA and V_{PP} ..... −0.5V to +7.0V(1)
Voltage from $\overline{EA}$ or
V_{PP} to V_{SS} or ANGND ..... −0.5V to +13.00V
Power Dissipation ..... 1.5W(2)

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V_{SS} − 0.4	V_{SS} + 0.4	V(1)
F_{OSC}	Oscillator Frequency **(8XC196KD)**	8	16	MHz
F_{OSC}	Oscillator Frequency **(8XC196KD20)**	8	20	MHz

NOTE:
1. ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0	V_{CC} + 0.5	V	
V_{HYS}	Hysteresis on $\overline{RESET}$	300		mV	V_{CC} = 5.0V
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.2	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)		0.8	V	I_{OL} = +0.4 mA
V_{OH}	Output High Voltage (Standard Outputs) (Note 4)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs) (Note 3)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 µA I_{OH} = −30 µA I_{OH} = −60 µA

DC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
I_{OH1}	Logical 1 Output Current in Reset on P2.0. Do not exceed this or device may enter test modes.	−0.8			mA	$V_{IH} = V_{CC} - 1.5V$
I_{IL1}	Logical 0 Input Current in Reset on P2.0. Maximum current that must be sunk by external device to ensure test mode entry.			−12.0	mA	$V_{IN} = 0.45V$
I_{IH1}	Logical 1 Input Current. Maximum current that external device must source to initiate NMI.			+200	μA	$V_{IN} = 2.4V$
I_{LI}	Input Leakage Current (Std. Inputs) (Note 5)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	μA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	μA	$V_{IN} = 0.45V$
I_{IL1}	AD Bus in Reset			−70	μA	$V_{IN} = 0.45V$
I_{CC}	Active Mode Current in Reset **(8XC196KD)**		65	75	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{CC}	Active Mode Current in Reset **(8XC196KD20)**		80	92	mA	XTAL1 = 20 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current **(8XC196KD)**		17	25	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current **(8XC196KD20)**		21	30	mA	XTAL1 = 20 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current		8	15	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	$V_{CC} = 5.5V, V_{IN} = 4.0V$
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
1. All pins except RESET and XTAL1.
2. Violating these specifications in Reset may cause the part to enter test modes.
3. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
4. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
5. Standard Inputs include HSI pins, READY, BUSWIDTH, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
6. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   - I_{OL} on Output pins: 10 mA
   - I_{OH} on quasi-bidirectional pins: self limiting
   - I_{OH} on Standard Output pins: 10 mA
7. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
8. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

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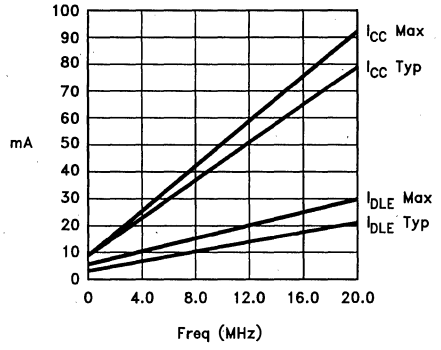


I_{CC} Max = 4.13 × Frequency + 9 mA
I_{CC} Typ = 3.50 × Frequency + 9 mA
I_{IDLE} Max = 1.25 × Frequency + 5 mA
I_{IDLE} Typ = 0.88 × Frequency + 3 mA

NOTE:
Frequencies below 8 MHz are shown for reference only; no testing is performed.

Figure 7. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 80C196KD:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} − 68	ns	
T_{LLYV}	ALE Low to READY Setup		T_{OSC} − 70	ns	(Note 3)
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	T_{OSC} − 15	2 T_{OSC} − 40	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		2 T_{OSC} − 68	ns	
T_{LLGV}	ALE Low to Buswidth Setup		T_{OSC} − 60	ns	(Note 3)
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 55	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 22	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 45	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.
3. These timings are included for compatibility with older −90 and BH products. They should not be used for newer high-speed designs.

AC CHARACTERISTICS (Continued)

For use over specified operating conditions.

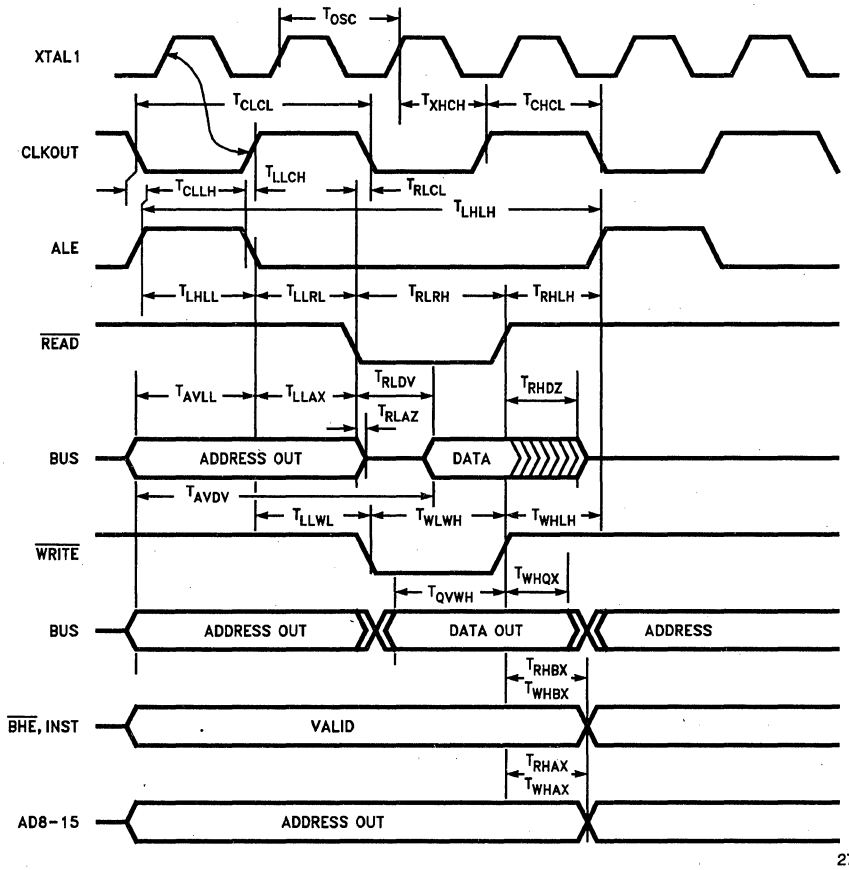
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16/20 MHz

The 80C196KD will meet these specifications:

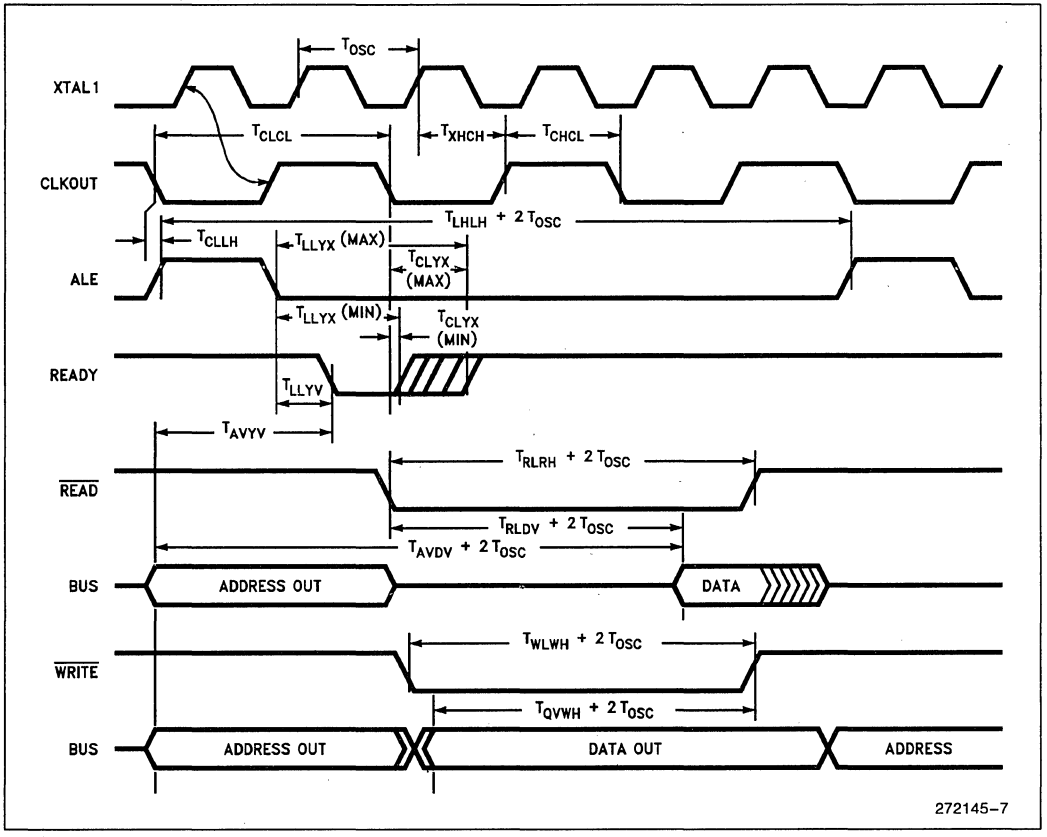
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 **(8XC196KD)**	8	16	MHz	(Note 1)
F_{XTAL}	Frequency on XTAL1 **(8XC196KD20)**	8	20	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$ **(8XC196KD)**	62.5	125	ns	
T_{OSC}	$1/F_{XTAL}$ **(8XC196KD20)**	50	125	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC}+15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	+15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 4)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC}+10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15			
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 35		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 30		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns	(Note 4)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23			(Note 4)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 20		ns	(Note 4)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 25		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	T_{OSC} − 30		ns	(Note 3)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	T_{OSC} − 25		ns	(Note 3)

NOTES:
1. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. 8-Bit bus only.
4. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

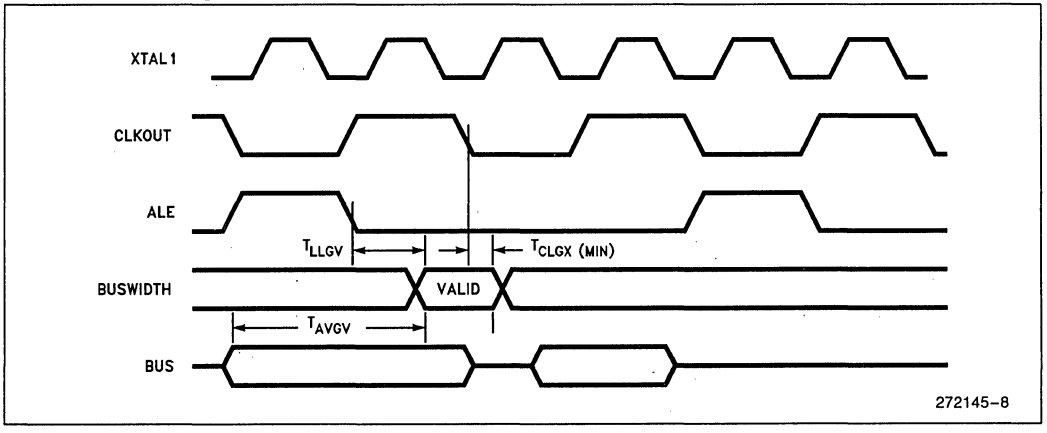
System Bus Timings



READY Timings (One Wait State)



Buswidth Timings



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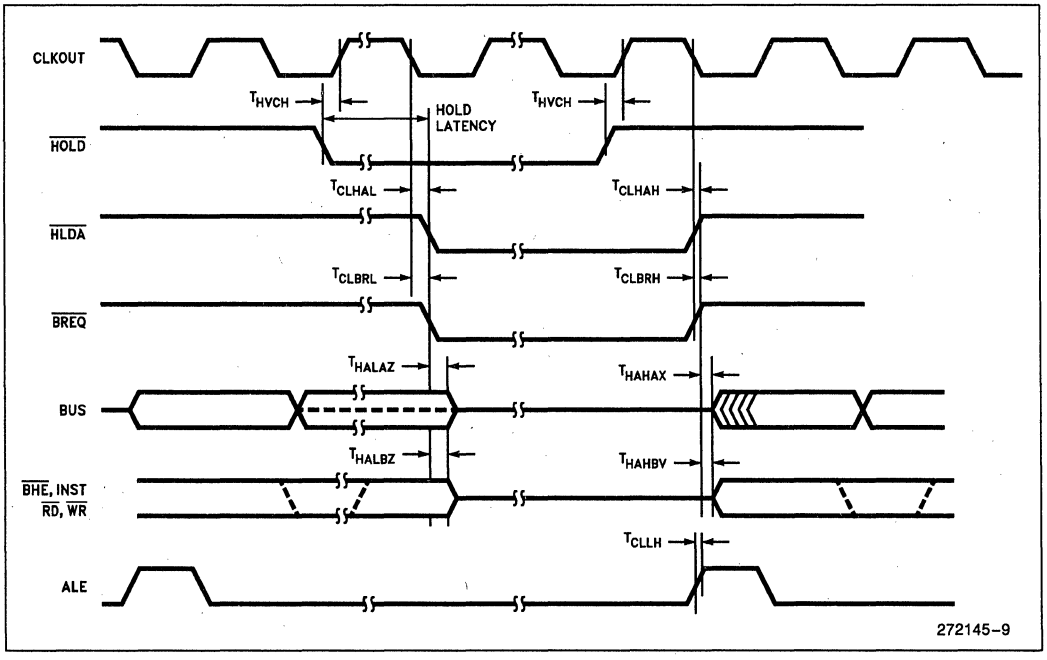
HOLD/HLDA TIMINGS

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	$\overline{HOLD}$ Setup	+55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to $\overline{HLDA}$ Low	−15	+15	ns	
T_{CLBRL}	CLKOUT Low to $\overline{BREQ}$ Low	−15	+15	ns	
T_{HALAZ}	$\overline{HLDA}$ Low to Address Float		+15	ns	
T_{HALBZ}	$\overline{HLDA}$ Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+20	ns	
T_{CLHAH}	CLKOUT Low to $\overline{HLDA}$ High	−15	+15	ns	
T_{CLBRH}	CLKOUT Low to $\overline{BREQ}$ High	−15	+15	ns	
T_{HAHAX}	$\overline{HLDA}$ High to Address No Longer Float	−15		ns	
T_{HAHBV}	$\overline{HLDA}$ High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10	+15	ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	+15	ns	

NOTE:
1. To guarantee recognition at next clock.

DC SPECIFICATIONS IN HOLD

Description	Min	Max	Units
Weak Pullups on $\overline{ADV}$, $\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{BHE}$	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4



MAXIMUM HOLD LATENCY

Bus Cycle Type	
Internal Execution	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

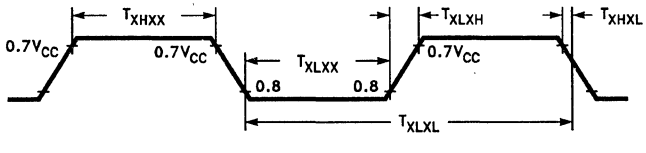
EXTERNAL CLOCK DRIVE (8XC196KD)

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	20		ns
T_{XLXX}	Low Time	20		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE (8XC196KD20)

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	20.0	MHz
T_{XLXL}	Oscillator Period	50	125	ns
T_{XHXX}	High Time	17		ns
T_{XLXX}	Low Time	17		ns
T_{XLXH}	Rise Time		8	ns
T_{XHXL}	Fall Time		8	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



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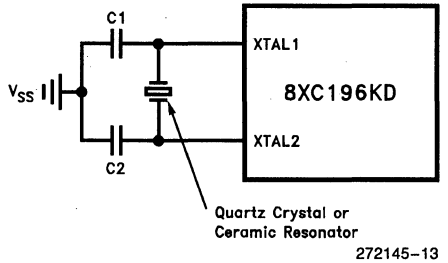
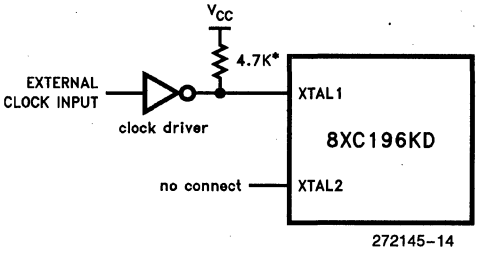
EXTERNAL CRYSTAL CONNECTIONS



272145-13

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using ceramic crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators consult manufacturer for recommended capacitor values.

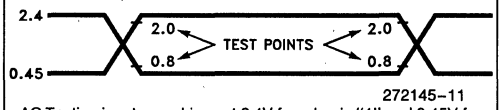
EXTERNAL CLOCK CONNECTIONS



272145-14

NOTE:
*Required if TTL driver used.
Not needed if CMOS driver is used.

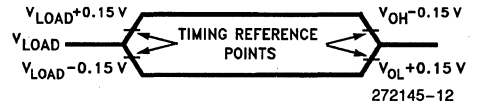
AC TESTING INPUT, OUTPUT WAVEFORMS



272145-11

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



272145-12

For Timing Purposes a Port Pin is no Longer Floating when a 150 mV change from Load Voltage Occurs, and Begins to Float when a 150 mV change from the Loaded V_{OH}/V_{OL} Level occurs I_{OL}/I_{OH} = ±15 mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
BR— $\overline{BREQ}$
R— $\overline{RD}$
W— $\overline{WR}/\overline{WRH}/\overline{WRL}$
X— XTAL1
Y— READY
Q— Data Out

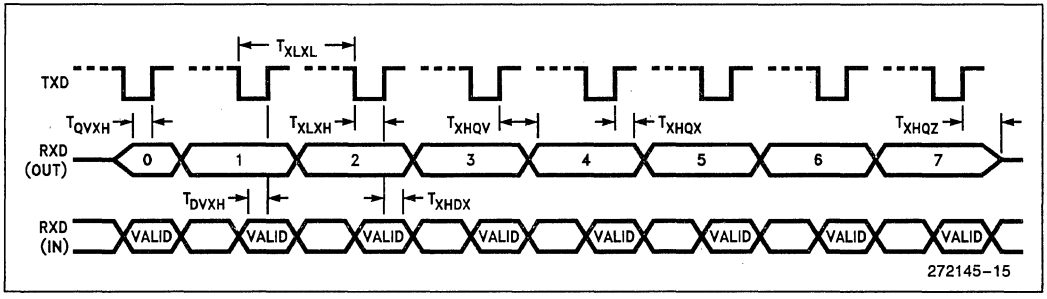
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE (MODE 0)

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} −50	4 T_{OSC} +50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} −50	2 T_{OSC} +50	ns
T_{QVXH}	Output Data Valid to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE (MODE 0)



A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V_{SS} − 0.40	V_{CC} + 0.40	V
T_{SAM}	Sample Time	1.0		µs(1)
T_{CONV}	Conversion Time	10	20	µs(1)
F_{OSC}	Oscillator Frequency **(8XC196KD)**	8.0	16.0	MHz
F_{OSC}	Oscillator Frequency **(8XC196KD20)**	8.0	20.0	MHz

NOTE:
1. The value of AD__TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Non-Linearity	1.0 ± 2.0	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	µA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approxiimately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms.)
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V_{SS} −0.40	V_{SS} + 0.40	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	7	20	μs(1)
F_{OSC}	Oscillator Frequency **(8XC109KD)**	8.0	16.0	MHz
F_{OSC}	Oscillator Frequency **(8XC196KD20)**	8.0	20.0	MHz

NOTE:
1. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±1	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±1	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming **(8XC196KD)**	6.0	16.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming **(8XC196KD20)**	6.0	20.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC EPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

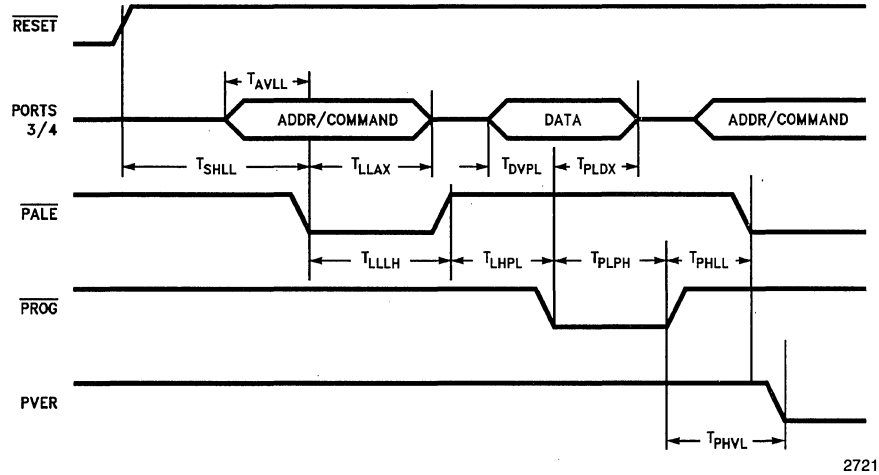
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

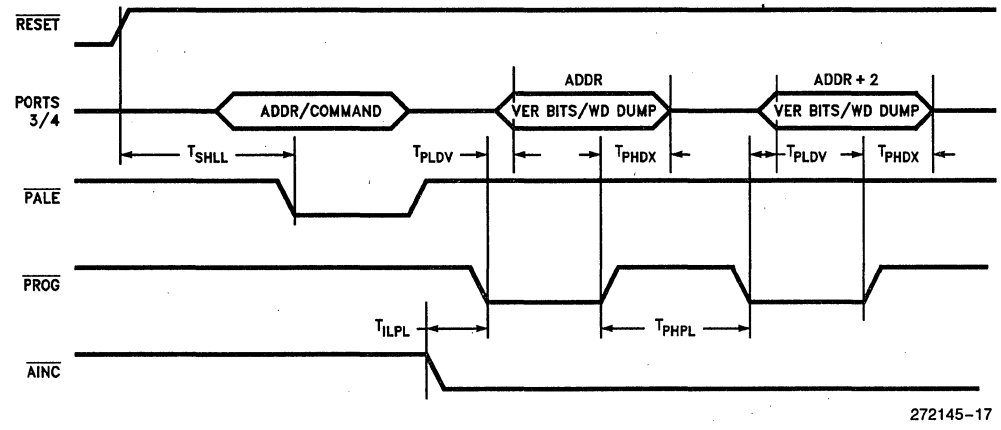
EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



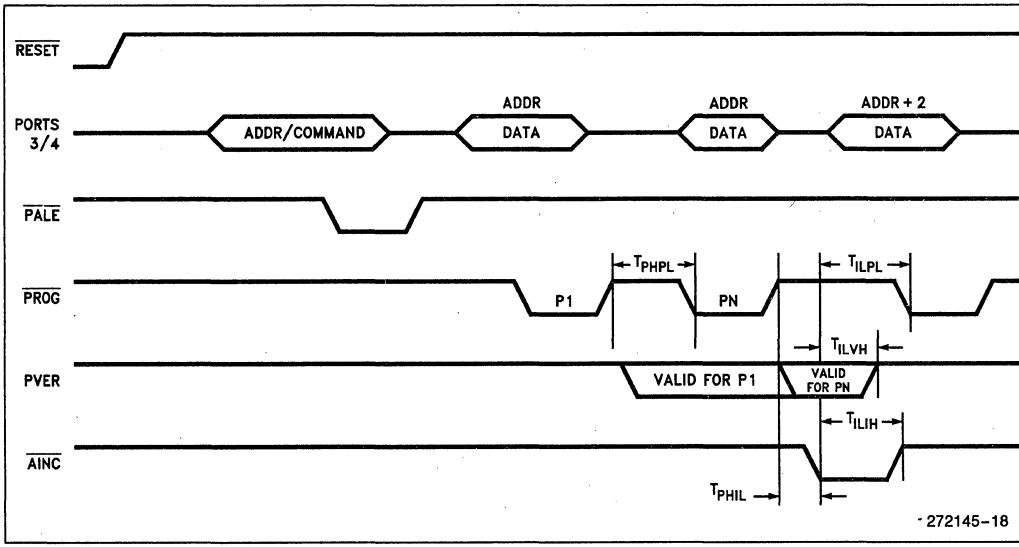
NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



NOTE:
P3.0 must be low ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



8XC196KC TO 8XC196KD DESIGN CONSIDERATIONS

1. Memory Map. The 8XC196KD has 1024 bytes of RAM/SFRs and 32K of OTPROM. The extra 512 bytes of RAM reside in locations 0200H to 03FFH, and the extra 16 Kbytes of OTPROM reside in locations 6000H to 9FFFH. On the 87C196KC these locations are always external, so KC code may have to be modified to run on the KD.
2. The vertical window scheme has been extended to include all on-chip RAM.
3. IOC3.1 controls the CLKOUT signal. This bit must be 0 to enable CLKOUT.
4. The 87C196KD has a different autoprogramming algorithm to support 32K of on-chip OTPROM.

XC196KD ERRATA

8XC196KD

None known.

DATA SHEET REVISION HISTORY

This data sheet is valid for devices with a "B" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are important differences between the 272145-001 and 272145-002 data sheets:

1. Added 20 MHz specifications.
2. Added 80-lead SQFP package pinout.
3. Changed QFP Package θ_{JA} to 56°C/W from 42°C/W.
4. Changed V_{HYS} to 300 mV from 150 mV.
5. Changed I_{CC} Typical specification at 16 MHz to 65 mA from 50 mA.
6. Changed I_{CC} Maximum specification at 16 MHz to 75 mA from 70 mA.
7. Changed I_{IDLE} Typical specification to 17 mA from 15 mA.
8. Changed I_{IDLE} Maximum specification to 25 mA from 30 mA.
9. Changed I_{PD} Typical specification to 8 μA from 15 μA.
10. Added I_{PD} Maximum specification.
11. Changed T_{CLDV} Maximum specification to $T_{OSC} - 45$ from $T_{OSC} - 50$.
12. Changed T_{LLAX} Minimum specification to $T_{OSC} - 35$ from $T_{OSC} - 40$.
13. Changed T_{CHWH} Minimum specification to -5 from -10.
14. Changed T_{RHAX} Minimum specification to $T_{OSC} - 25$ from $T_{OSC} - 30$.
15. Changed T_{HALAZ} Maximum specification to $+15$ from $+10$.
16. Changed T_{HALBZ} Maximum specification to $+20$ from $+15$.
17. Added T_{HAHBV} Maximum specification.
18. Changed T_{SAM} for 10-bit mode to 1 μs from 3 μs.
19. Changed T_{SAM} for 8-bit mode to 1 μs from 2 μs.
20. Changed I_{IH1} test condition to $V_{IN} = 2.4V$ from 5.5V.
21. Changed I_{IH1} maximum specification to $+200$ μA from $+100$ μA.
22. Removed NMI from list of standard inputs.
23. Updated I_{CC} and I_{IDLE} vs frequency graph.
24. Updated note under DC EPROM Programming Characteristics.
25. Changed I_{LI1} maximum specification to -12 mA from -6 mA.

8XL196KD
COMMERCIAL CHMOS MICROCONTROLLER

87L196KD—32 Kbytes of On-Chip OTPROM

- **3.0V to 3.6V Operation**
- **16 MHz Operation**
- **1000 Byte Register RAM**
- **Register-to-Register Architecture**
- **28 Interrupt Sources/16 Vectors**
- **Peripheral Transaction Server**
- **1.75 μs 16 x 16 Multiply (16 MHz)**
- **3.0 μs 32/16 Divide (16 MHz)**
- **Powerdown and Idle Modes**
- **Five 8-Bit I/O Ports**
- **16-Bit Watchdog Timer**
- **Dynamically Configurable 8-Bit or 16-Bit Buswidth**
- **Full Duplex Serial Port**
- **High Speed I/O Subsystem**
- **16-Bit Timer**
- **16-Bit Up/Down Counter with Capture**
- **3 Pulse-Width-Modulated Outputs**
- **Four 16-Bit Software Timers**
- **8- or 10-Bit A/D Converter with Sample/Hold**
- **OTP One-Time Programmable Version**

The 8XL196KD 16-bit microcontroller is a high performance member of the MCS®-96 microcontroller family. The 8XL196KD is an enhanced 80C196KC device with 3.3V operation, 1000 bytes RAM, 16 MHz operation and an optional 32 Kbytes of ROM/EPROM. Intel's CHMOS III-E process provides a high performance processor along with low power consumption.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

October 1992
Order Number: 272254-001

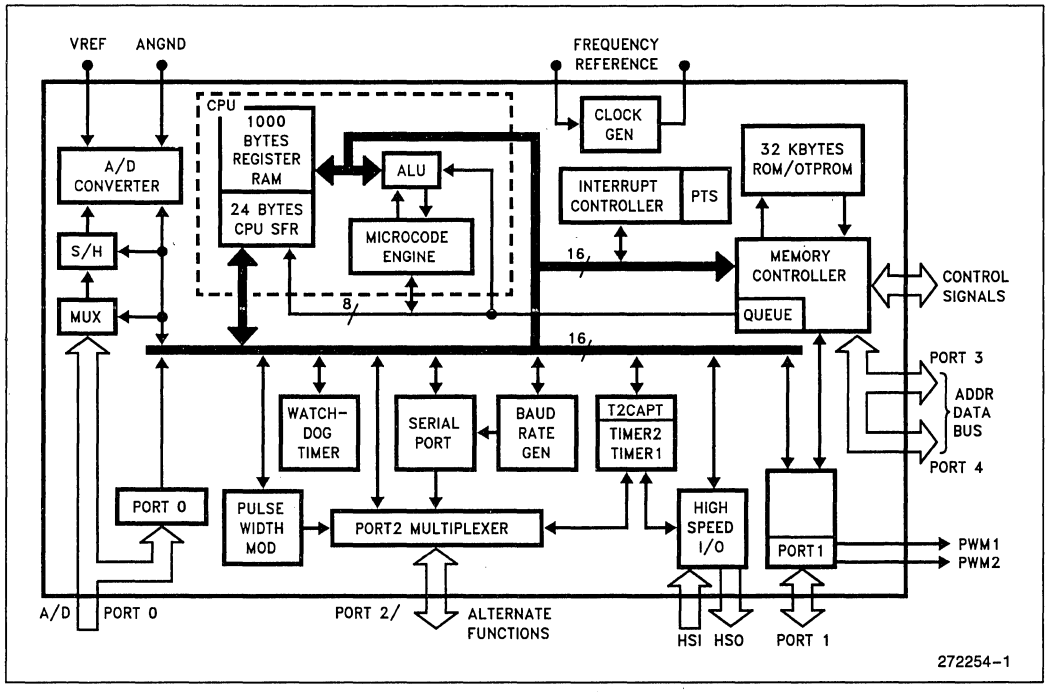


Figure 1. 8XL196KD Block Diagram

87L196KD ENHANCED FEATURE SET OVER THE 87C196KC

1. The 87L196KD has twice the RAM and twice the OTPROM space of the 87C196KC.
2. The vertical windowing scheme has been extended to allow all 1000 bytes of register RAM to be windowed into the lower register file.

FUNCTIONAL DIFFERENCES BETWEEN THE 8XC196KD AND THE 8XL196KD

1. The $\overline{\text{HOLD}}/\overline{\text{HLDA}}$ bus protocol is not supported on the 8XL196KD.
2. The CLKOUT disable bit (IOC3.1) is not supported on the 8XL196KD.
3. Run-time programming is not supported on the 8XL196KD.

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8XL196KD VERTICAL WINDOWING MAP

Table 1. 128-Byte Windows

Address to Remap	Device Series	WSR Contents
0380H	KD	X001 0111B = 17H
0300H	KD	X001 0110B = 16H
0280H	KD	X001 0101B = 15H
0200H	KD	X001 0100B = 14H
0180H	KC, KD	X001 0011B = 13H
0100H	KC, KD	X001 0010B = 12H
0080H	KC, KD	X001 0001B = 11H
0000H	KC, KD	X001 0000B = 10H

Window in Lower Register File: 80H–FFH

Table 2. 64-Byte Windows

Address to Remap	Device Series	WSR Contents
03C0H	KD	X010 1111B = 2FH
0380H	KD	X010 1110B = 2EH
0340H	KD	X010 1101B = 2DH
0300H	KD	X010 1100B = 2CH
02C0H	KD	X010 1011B = 2BH
0280H	KD	X010 1010B = 2AH
0240H	KD	X010 1001B = 29H
0200H	KD	X010 1000B = 28H
01C0H	KC, KD	X010 0111B = 27H
0180H	KC, KD	X010 0110B = 26H
0140H	KC, KD	X010 0101B = 25H
0100H	KC, KD	X010 0100B = 24H
00C0H	KC, KD	X010 0011B = 23H
0080H	KC, KD	X010 0010B = 22H
0040H	KC, KD	X010 0001B = 21H
0000H	KC, KD	X010 0000B = 20H

Window in Lower Register File: C0H–FFH

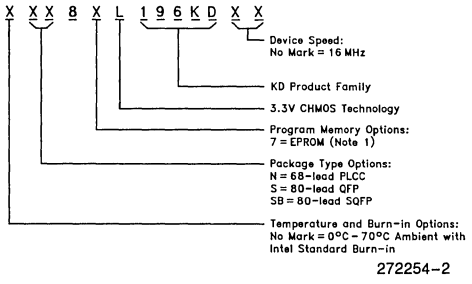
Table 3. 32-Byte Windows

Address to Remap	Device Series	WSR Contents
03E0H	KD	X101 1111B = 5FH
03C0H	KD	X101 1110B = 5EH
03A0H	KD	X101 1101B = 5DH
0380H	KD	X101 1100B = 5CH
0360H	KD	X101 1011B = 5BH
0340H	KD	X101 1010B = 5AH
0320H	KD	X101 1001B = 59H
0300H	KD	X101 1000B = 58H
02E0H	KD	X101 0111B = 57H
02C0H	KD	X101 0110B = 56H
02A0H	KD	X101 0101B = 55H
0280H	KD	X101 0100B = 54H
0260H	KD	X101 0011B = 53H
0240H	KD	X101 0010B = 52H
0220H	KD	X101 0001B = 51H
0200H	KD	X101 0000B = 50H
01E0H	KC, KD	X100 1111B = 4FH
01C0H	KC, KD	X100 1110B = 4EH
01A0H	KC, KD	X100 1101B = 4DH
0180H	KC, KD	X100 1100B = 4CH
0160H	KC, KD	X100 1011B = 4BH
0140H	KC, KD	X100 1010B = 4AH
0120H	KC, KD	X100 1001B = 49H
0100H	KC, KD	X100 1000B = 48H
00E0H	KC, KD	X100 0111B = 47H
00C0H	KC, KD	X100 0110B = 46H
00A0H	KC, KD	X100 0101B = 45H
0080H	KC, KD	X100 0100B = 44H
0060H	KC, KD	X100 0011B = 43H
0040H	KC, KD	X100 0010B = 42H
0020H	KC, KD	X100 0001B = 41H
0000H	KC, KD	X100 0000B = 40H

Window in Lower Register File: E0H–FFH

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87L196KD is 68-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 2. The 8XL196KD Family Nomenclature

Table 4. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	56°C/W	12°C/W
SQFP	TBD	TBD

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 5. 8XL196KD Memory Map

Description	Address
External Memory or I/O	0FFFFH 0A000H
Internal ROM/OTPROM or External Memory (Determined by $\overline{EA}$)	9FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4 Word Addressable Only	1FFFH 1FFEH
External Memory	1FFDH 0400H
1000 Bytes Register RAM (Note 1)	03FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 03FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KC for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

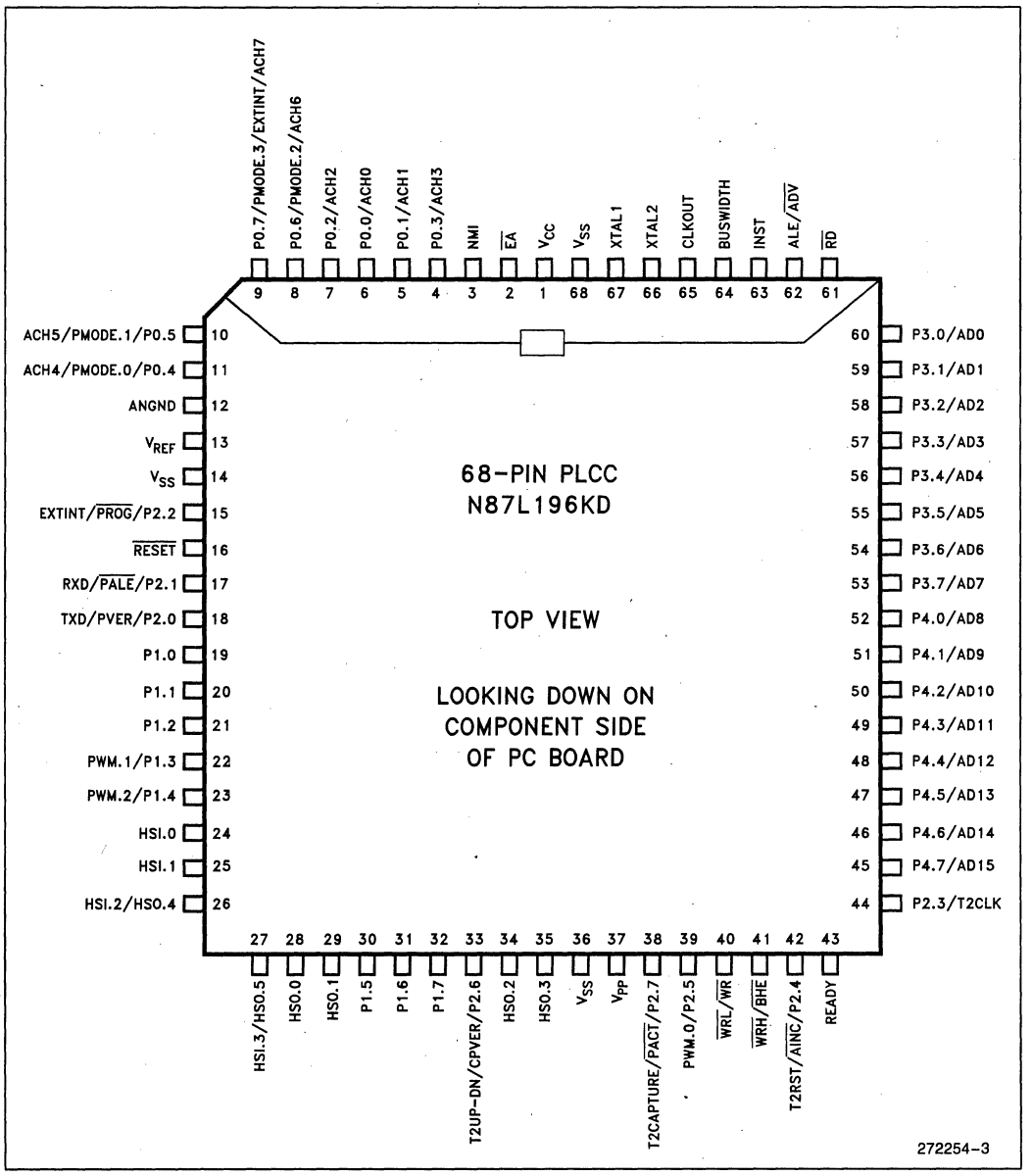
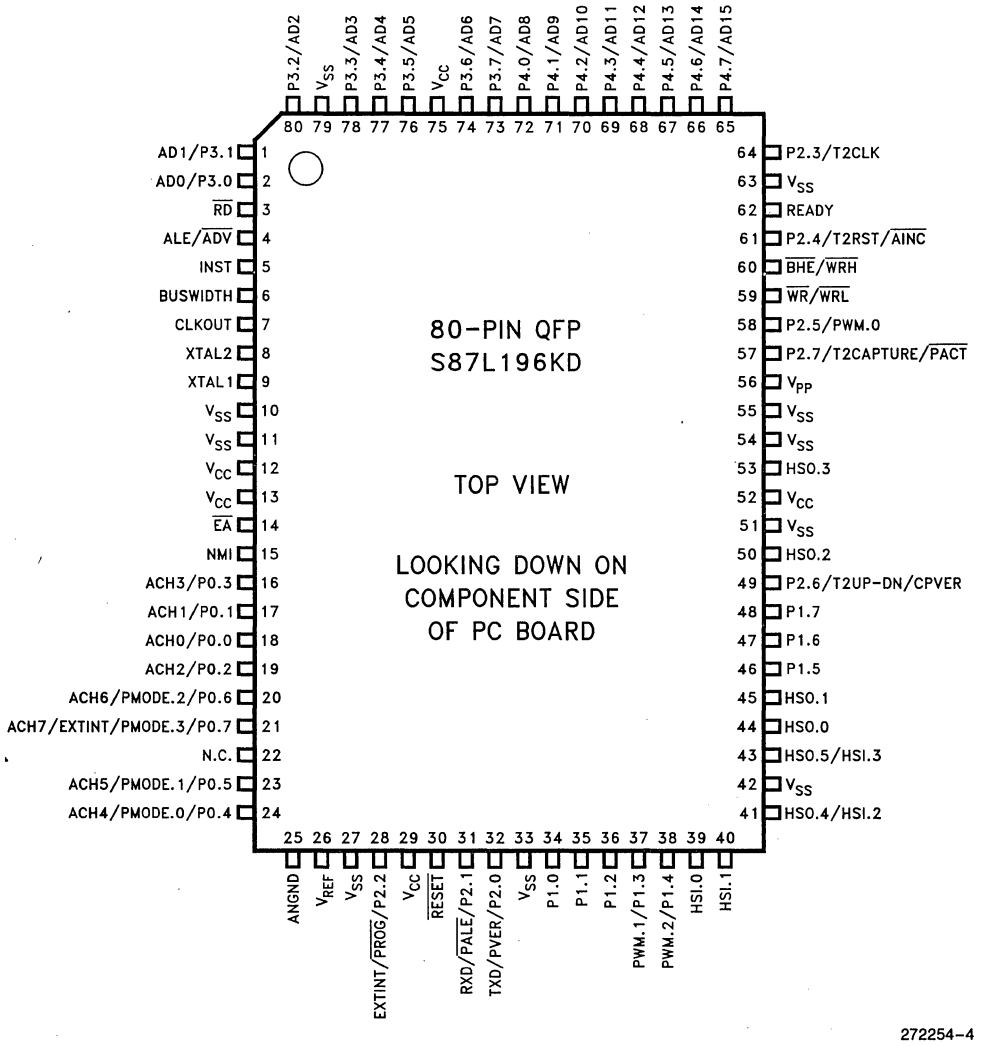


Figure 3. 68-Pin PLCC Package



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 4. 80-Pin QFP Package

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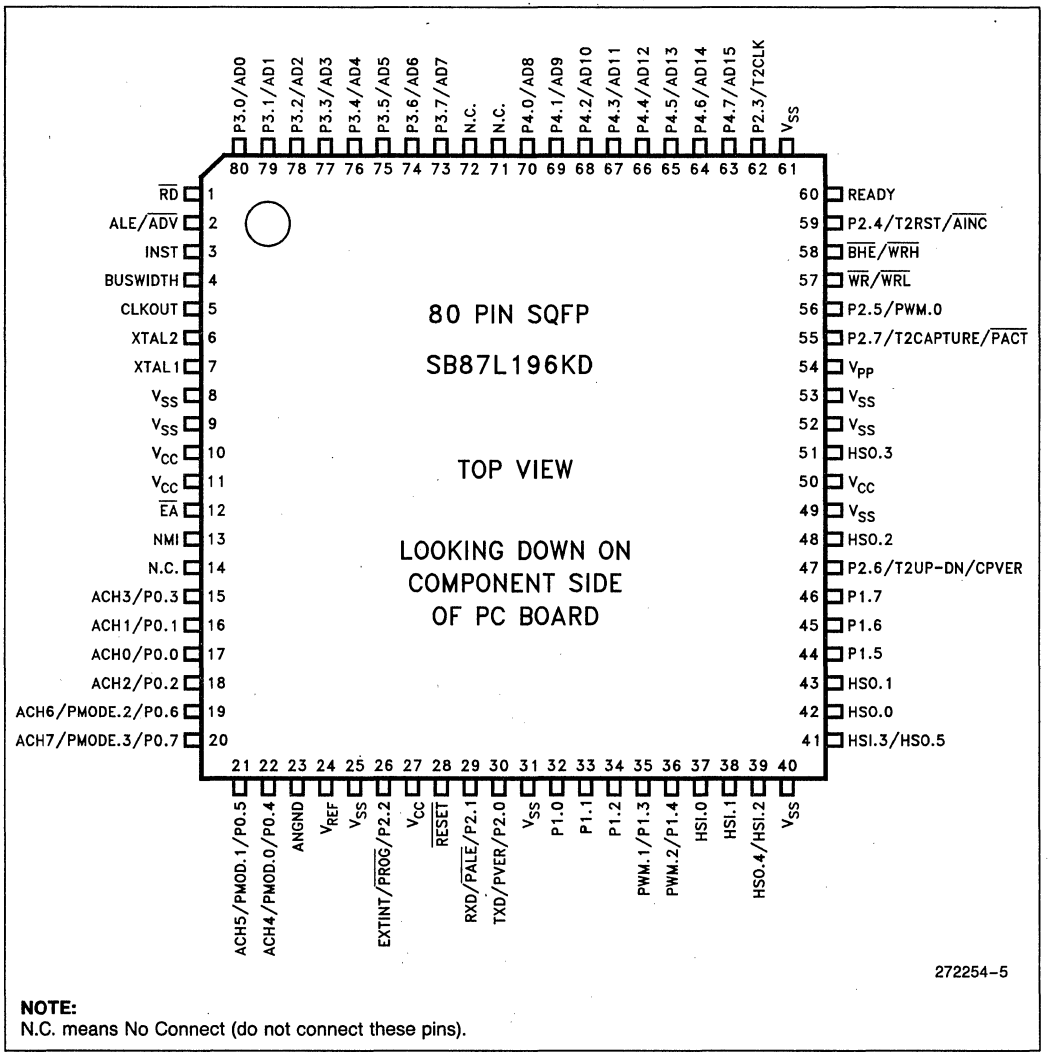

NOTE:
N.C. means No Connect (do not connect these pins).

Figure 5. 80-Pin SQFP Package

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (3.3V).
V_{SS}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of which must be connected.
V_{REF}	Reference voltage for the A/D converter (3.3V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. This pin also supplies the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency.
$\overline{\text{RESET}}$	Reset input and open drain output.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal high causes memory accesses to locations 2000H through 9FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal low causes accesses to those locations to be directed to off-chip memory. Also used to enter programming mode.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being written. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 80C196KD. Pins 2.6 and 2.7 are quasi-bidirectional,
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
PMODE	Determines the OTPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
$\overline{\text{PALE}}$	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
CPVER	Cummulative Program Output Verification. Pin is high if all locations have programmed correctly since entering a programming mode.
$\overline{\text{AINC}}$	Auto Increment. Active low input enables the auto increment mode. Auto increment allows reading or writing sequential EPROM locations without address transactions across the PBUS for each read or write.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS}
Except EA and V_{PP} ..... −0.5V to +7.0V(1)
Voltage from $\overline{EA}$ or
V_{PP} to V_{SS} or ANGND ..... −0.5V to +13.00V
Power Dissipation ..... 1.5W(2)

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

TARGETED OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	3.00	3.60	V
V_{REF}	Analog Supply Voltage	3.00	3.60	V
ANGND	Analog Ground Voltage	V_{SS} − 0.3	V_{SS} + 0.3	V(1)
F_{OSC}	Oscillator Frequency	8	16	MHz

NOTE:
1. ANGND and V_{SS} should be nominally at the same potential.

TARGETED DC CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IL1}	Input Low Voltage on Quasi-Bidirectional Pins	−0.3	+0.7	V	
V_{IL2}	Input Low Voltage on Reset	−0.3	+0.6	V	
V_{IH}	Input High Voltage (Note 1)	2.0	V_{CC} + 0.3	V	
V_{HYS}	Hysteresis on $\overline{RESET}$	150		mV	V_{CC} = 3.3V
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.3	V	
V_{IH2}	Input High Voltage on RESET	2.2	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)		0.8	V	I_{OL} = +0.4 mA
V_{OH}	Output High Voltage (Standard Outputs) (Note 4)	2.4		V	I_{OH} = −2.0 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs) (Note 3)	2.4		V	I_{OH} = −30 μA

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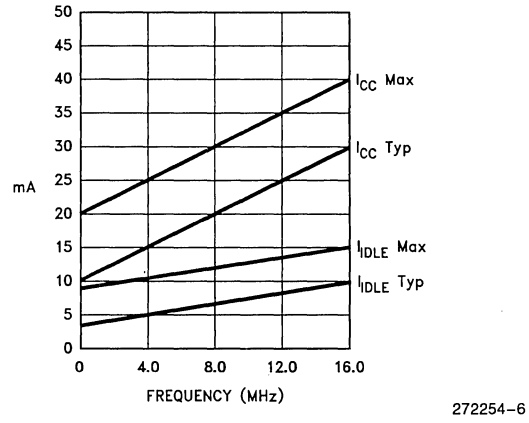
TARGETED DC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
I_{OH1}	Logical 1 Output Current in Reset on P2.0. Do not exceed this or device may enter test modes.	TBD			mA	V_{IH} = 2.0V
I_{IL2}	Logical 0 Input Current in Reset on P2.0. Maximum current that must be sunk by external device to ensure test mode entry.			TBD	mA	V_{IN} = 0.45V
I_{IH1}	Logical 1 Input Current. Maximum current that external device must source to initiate NMI.			TBD	μA	V_{IN} = 2.0V
I_{LI}	Input Leakage Current (Std. Inputs) (Note 5)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	μA	V_{IN} = 1.2V
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	μA	V_{IN} = 0.40V
I_{IL1}	AD Bus in Reset			−70	μA	V_{IN} = 0.40V
I_{CC}	Active Mode Current in Reset		30	40	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF}$ = 3.6V
I_{IDLE}	Idle Mode Current		10	15	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF}$ = 3.6V
I_{PD}	Powerdown Mode Current		8	15	μA	$V_{CC} = V_{PP} = V_{REF}$ = 3.6V
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF}$ = 3.6V
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
1. All pins except RESET.
2. Violating these specifications in Reset may cause the part to enter test modes.
3. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
4. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
5. Standard Inputs include HSI pins, READY, BUSWIDTH, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
6. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   - I_{OL} on Output pins: 10 mA
   - I_{OH} on quasi-bidirectional pins: self limiting
   - I_{OH} on Standard Output pins: 10 mA
7. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
8. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA



NOTE:
Frequencies below 8 MHz are shown for reference only; no testing is performed.

Figure 6. I_{CC} and I_{IDLE} vs Frequency

TARGETED AC CHARACTERISTICS

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 80L196KD:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} − 90	ns	
T_{YLYH}	Non READY Time		No upper limit	ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		2 T_{OSC} − 68	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 60	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 30	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 50	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

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TARGETED AC CHARACTERISTICS (Continued)

For use over specified operating conditions.

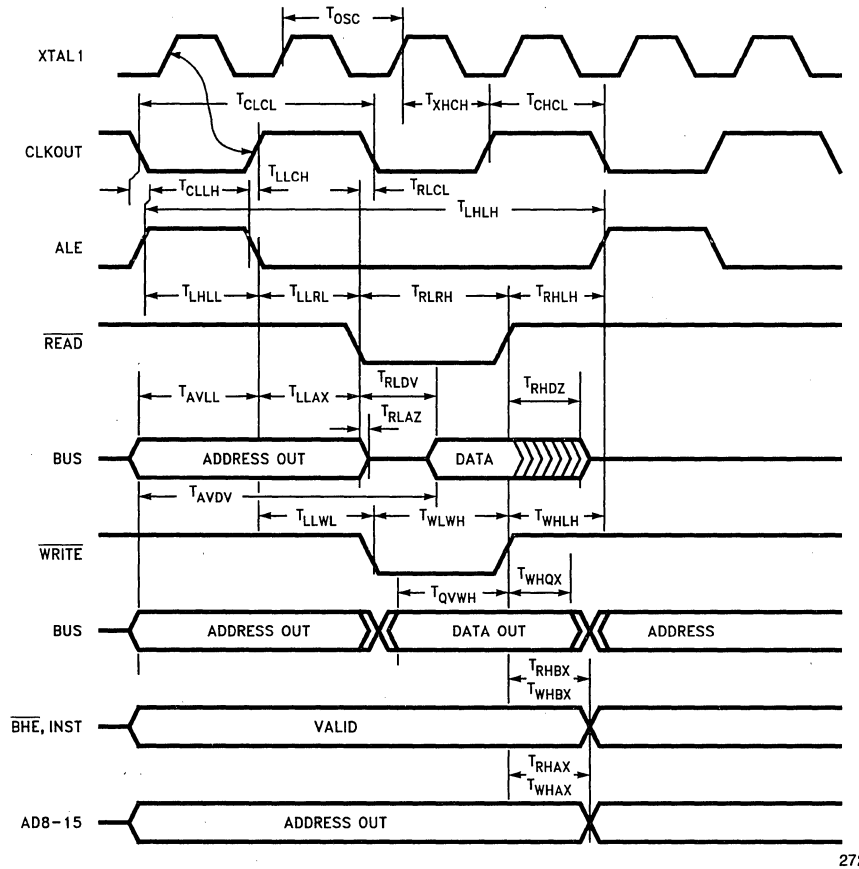
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The 80L196KD will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1	8	16	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$	62.5	125	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	$2\,T_{OSC}$		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC}+15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	+33	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	$4\,T_{OSC}$		ns	(Note 4)
T_{LHLL}	ALE High Period	T_{OSC} − 14	T_{OSC}+10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15			
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 42		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns	(Note 4)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 37	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 17		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23			(Note 4)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 20		ns	(Note 4)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 33		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 19	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	T_{OSC} − 30		ns	(Note 3)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	T_{OSC} − 30		ns	(Note 3)

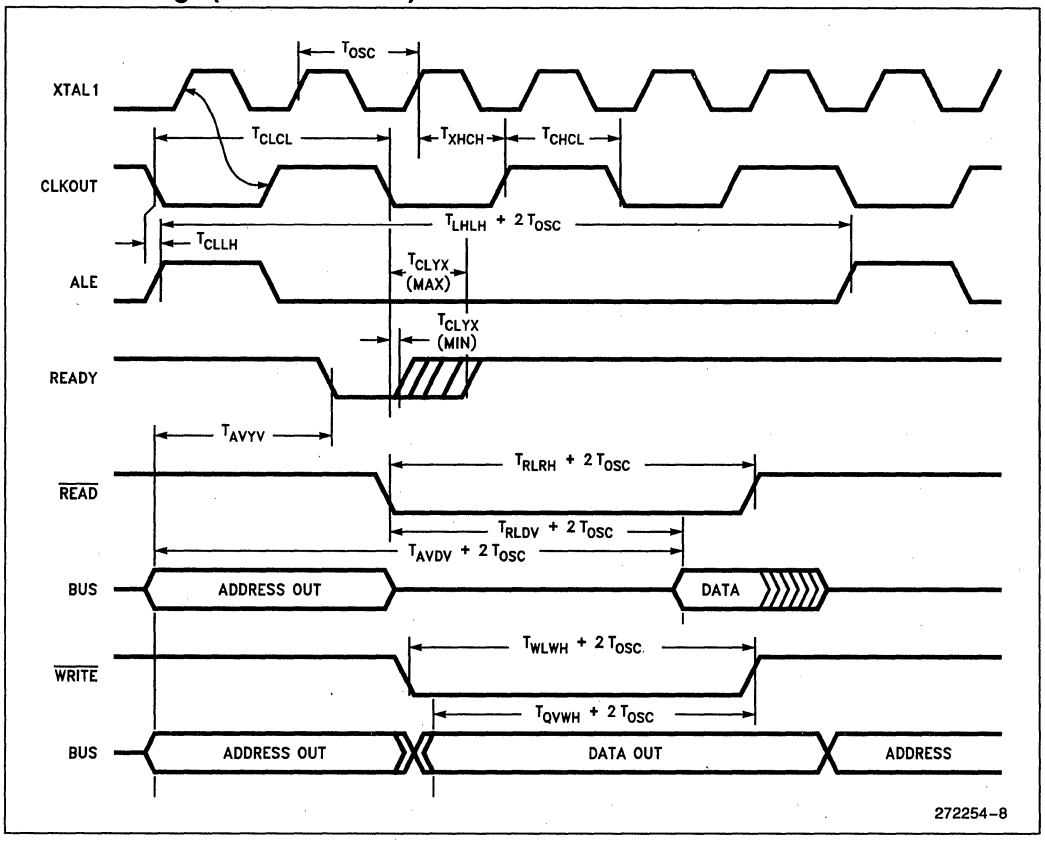
NOTES:
1. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. 8-Bit bus only.
4. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

System Bus Timings

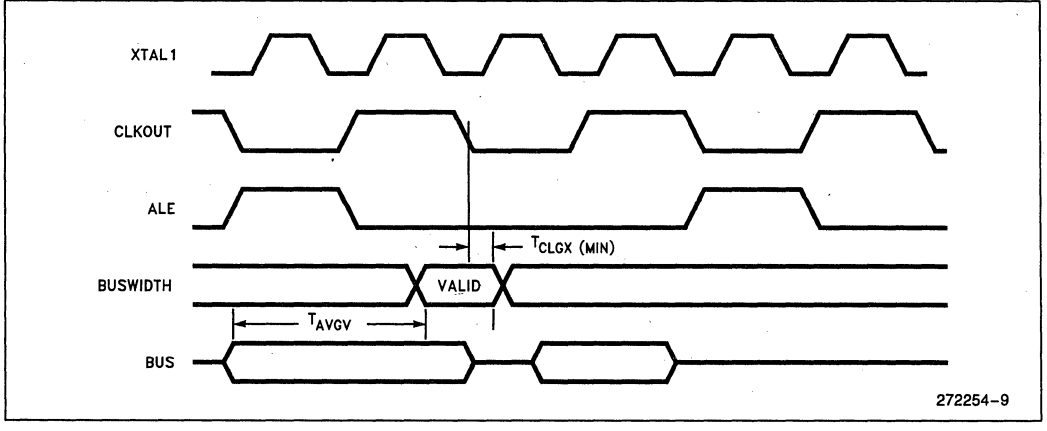


18

READY Timings (One Wait State)



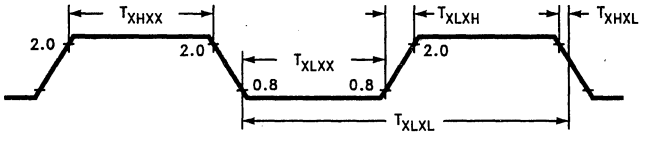
Buswidth Timings



EXTERNAL CLOCK DRIVE (8XL196KD)

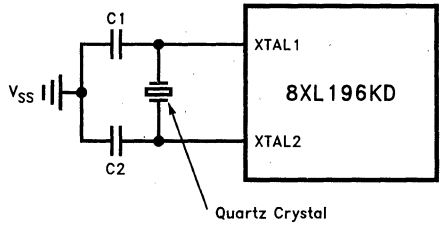
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	20		ns
T_{XLXX}	Low Time	20		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



272254-10

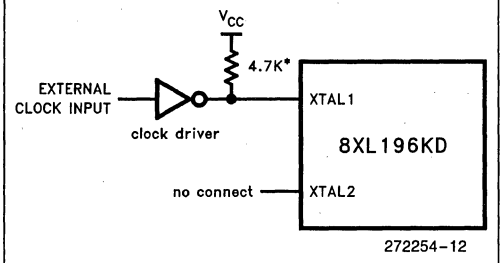
EXTERNAL CRYSTAL CONNECTIONS



272254-11

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using ceramic crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators consult manufacturer for recommended circuitry.

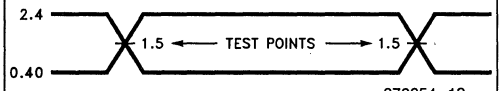
EXTERNAL CLOCK CONNECTIONS



272254-12

NOTE:
*Required if TTL driver used.
Not needed if CMOS driver is used.

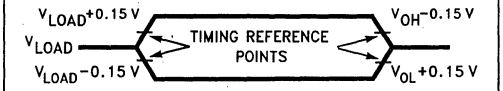
AC TESTING INPUT, OUTPUT WAVEFORMS



272254-13

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.40V for a Logic "0" Timing measurements are made at 1.5V for a Logic "1" and for a Logic "0".

FLOAT WAVEFORMS



272254-14

For Timing Purposes a Port Pin is no Longer Floating when a 150 mV change from Load Voltage Occurs, and Begins to Float when a 150 mV change from the Loaded V_{OH}/V_{OL} Level occurs I_{OL}/I_{OH} = ±15 mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
BR— $\overline{BREQ}$
R— $\overline{RD}$
W— $\overline{WR}/\overline{WRH}/\overline{WRL}$
X— XTAL1
Y— READY
Q— Data Out

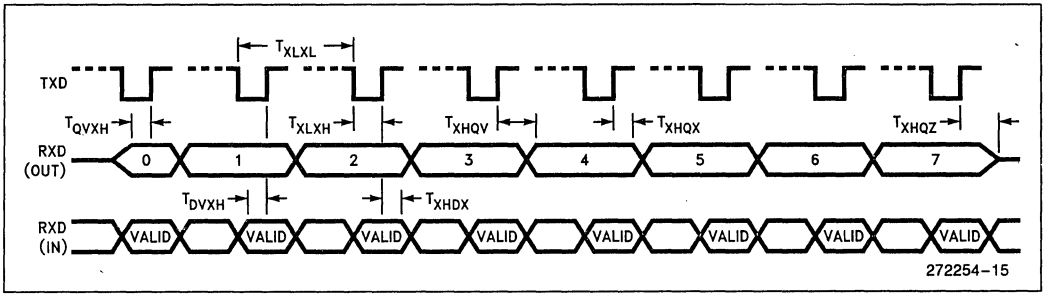
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE (MODE 0)

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} −50	4 T_{OSC} +50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} −50	2 T_{OSC} +50	ns
T_{QVXH}	Output Data Valid to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE (MODE 0)



A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

TARGETED 10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
V_{CC}	Digital Supply Voltage	3.0	3.6	V
V_{REF}	Analog Supply Voltage	3.0	3.6	V
ANGND	Analog Ground Voltage	V_{SS} − 0.30	V_{CC} + 0.30	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	10	20	μs(1)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTE:
1. The value of AD__TIME is selected to meet these specifications.

TARGETED 10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Non-Linearity	1.0 ± 2.0	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		ANGND − 0.3	V_{REF} + 0.3	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approxiimately 3 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms.)
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

TARGETED 8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
V_{CC}	Digital Supply Voltage	3.0	3.6	V
V_{REF}	Analog Supply Voltage	3.0	3.6	V
ANGND	Analog Ground Voltage	V_{SS} −0.30	V_{SS} + 0.30	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	7	20	μs(1)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTE:
1. The value of AD_TIME is selected to meet these specifications.

TARGETED 8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±1	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±1	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		V_{SS} − 0.3	V_{REF} + 0.3	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approximately 12 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

OTPROM SPECIFICATIONS

TARGETED OPERATING CONDITIONS DURING PROGRAMMING

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC OTPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

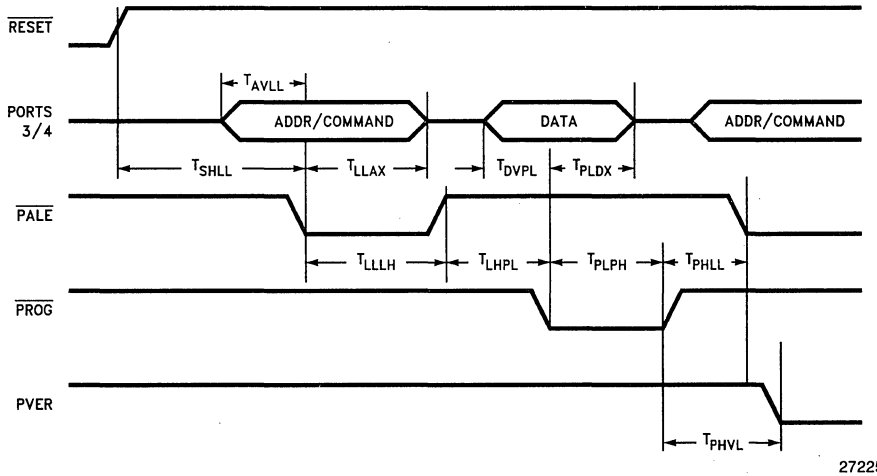
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

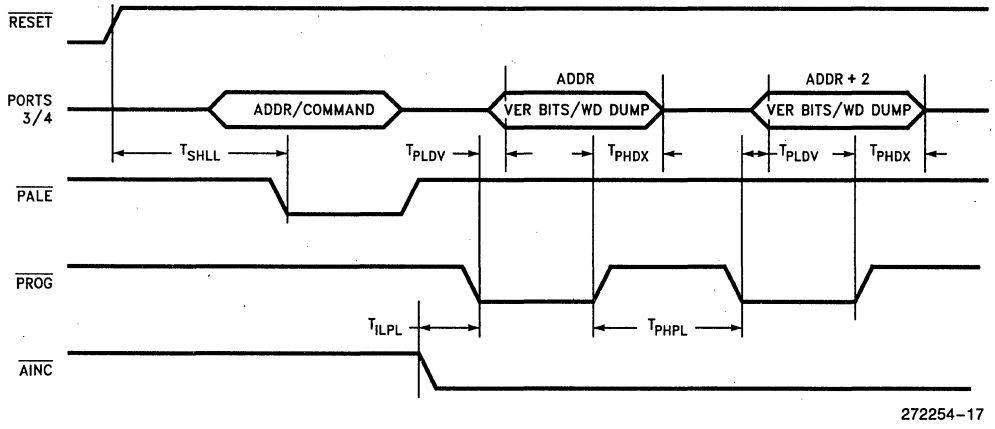
EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



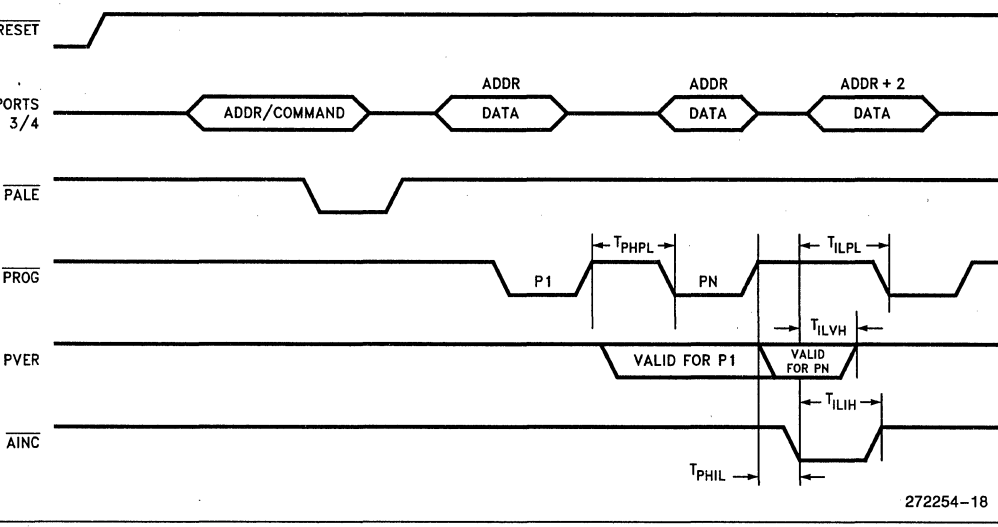
NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



NOTE:
P3.0 must be low ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



8XL196KD ERRATA

None known.

DATA SHEET REVISION HISTORY

This data sheet is valid for devices with a "B" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

8XC196KR Data Sheet

19

8XC196KR/KQ/JR/JQ
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

87C196KR/KQ/JR/JQ—16 Kbytes of On-Chip OTPROM
80C196KR/KQ/JR/JQ—ROMless

- High Performance CHMOS 16-Bit CPU
- 16 MHz Operating Frequency
- Up to 488 Bytes of On-Chip Register RAM
- 256 Bytes of Additional RAM (Code or Data RAM)
- Register-Register Architecture
- 8 Channel/10-Bit A/D with Sample/Hold
- 37 Prioritized Interrupt Sources
- Up to Seven 8-Bit (56) I/O Ports
- Full Duplex Serial I/O Port (SIO) and Full Duplex Synchronous Serial I/O Port (SSIO) with Dedicated Baud Rate Generators
- Interprocessor Communication Slave Port
- Watchdog Timer
- High-Speed Peripheral Transaction Server (PTS)
- Two Programmable 16-Bit Timer/Counters with Prescale, Cascading, Standard and Quadrature Counting Inputs
- 10 High-Speed Capture/Compare (EPA)
- Two Dedicated High Speed Compare Registers
- Two Flexible 16-Bit Timer/Counters
- Quadrature Counting Inputs
- Flexible 8-/16-Bit External Bus
- Programmable Bus (HOLD/HLDA)
- 1.75 μs 16 x 16 Multiply
- 3 μs 32/16 Divide
- Extended Temperature Available
- 68-Pin and 52-Pin PLCC Packages

Device	Pins/Package	OTPROM	Reg RAM	Internal RAM	I/O	EPA	SIO	SSIO	A/D
87C196KR	68 p PLCC	16K	512	256	56	10	Y	Y	8
87C196KQ	68 p PLCC	12K	384	128	56	10	Y	Y	8
87C196JR	52 p PLCC	16K	512	256	41	6	Y	Y	6
87C196JQ	52 p PLCC	12K	384	128	41	6	Y	Y	6
80C196KR	68 p PLCC	0	512	256	56	10	Y	Y	8
80C196KQ	68 p PLCC	0	384	128	56	10	Y	Y	8
80C196JR	52 p PLCC	0	512	256	41	6	Y	Y	6
80C196JQ	52 p PLCC	0	384	128	41	6	Y	Y	6

The 87C196KR/KQ/JR/JQ devices represent the 4th generation of MCS®-96 products implemented on Intel's advanced 1 micron process technology. These products are members of the 80C196 family of devices and the instruction set is the same as that of the 80C196KC. The 87C196JR is a 52-lead version of the 87C196KR device, while the 87C196KQ/JQ are memory scalars of the 87C196KR/JR.

The MCS-96® family members are all high-performance microcontrollers with a 16-bit CPU. The 87C196KR is composed of the high-speed (16 MHz) core as well as the following peripherals: up to 16 Kbytes of on-chip EPROM, up to 512 bytes of Register RAM, 256 bytes of Code RAM, an eight-channel 10-bit analog to digital converter, an (8096 compatible) asynchronous/synchronous serial I/O port, an additional synchronous serial I/O port, 10 modularized multiplexed capture and compare channels (called the Event Processor Array), a sophisticated prioritized interrupt structure with the programmable Peripheral Transaction Server (PTS).

September 1992
Order Number: 270912-004

Additional register space is allocated for the EPA and can be windowed into the lower Register RAM area.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended (**Express**) temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

See the prefix identification for extended temperature designators.

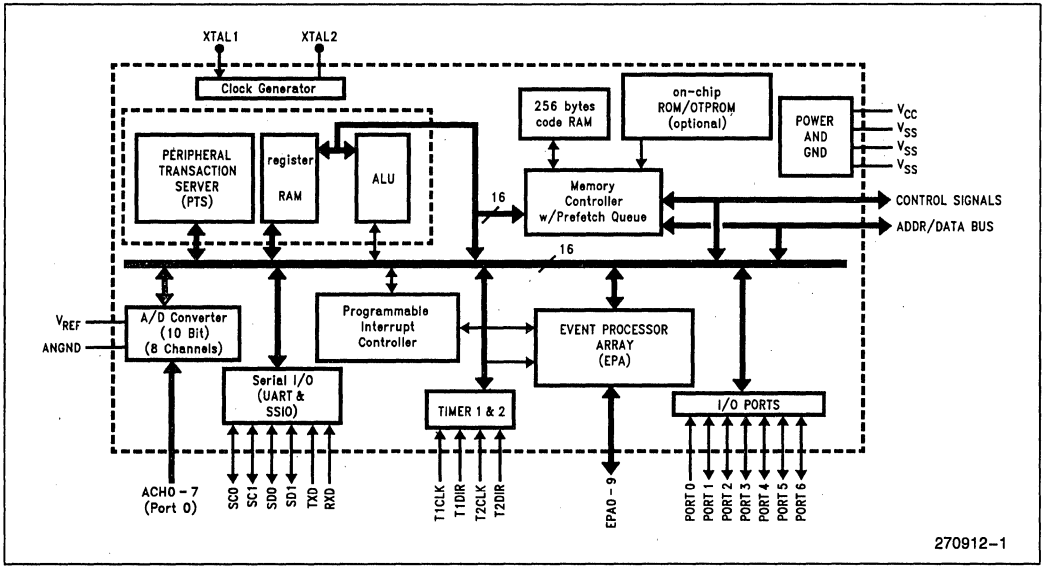


Figure 1. Block Diagram

0FFFFH 06000H	External Memory
05FFFH 02080H	Internal ROM/EPROM or External Memory
0207FH 0205EH	Reserved
0205DH 02040H	PTS Vectors
0203FH 02030H	Interrupt Vectors (upper)
0202FH 02020H	ROM/EPROM Security Key
0201FH	Reserved
0201BH	Reserved (must contain 20H)
0201AH	CCB1
02019H	Reserved (must contain 20H)

02018H	CCB0
02017H 02014H	Reserved
02013H 02000H	Interrupt Vectors (lower)
01FFFH 01F00H	Internal SFRs
01EFFH 00500H	External Memory
004FFH 00400H	Internal RAM
003FFH 00200H	External Memory
001FFH 18H	Register File
17H 00H	CPU SFR's

NOTES:
1. Reserved memory locations must contain 0FFH unless noted.
2. Reserved SFR bit locations must contain 0H unless noted.
3. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

Process Information

The 8XC196KR/JR/KQ/JQ is manufactured on PX29.5, a CHMOS IV process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

Table 1. Prefix Identification

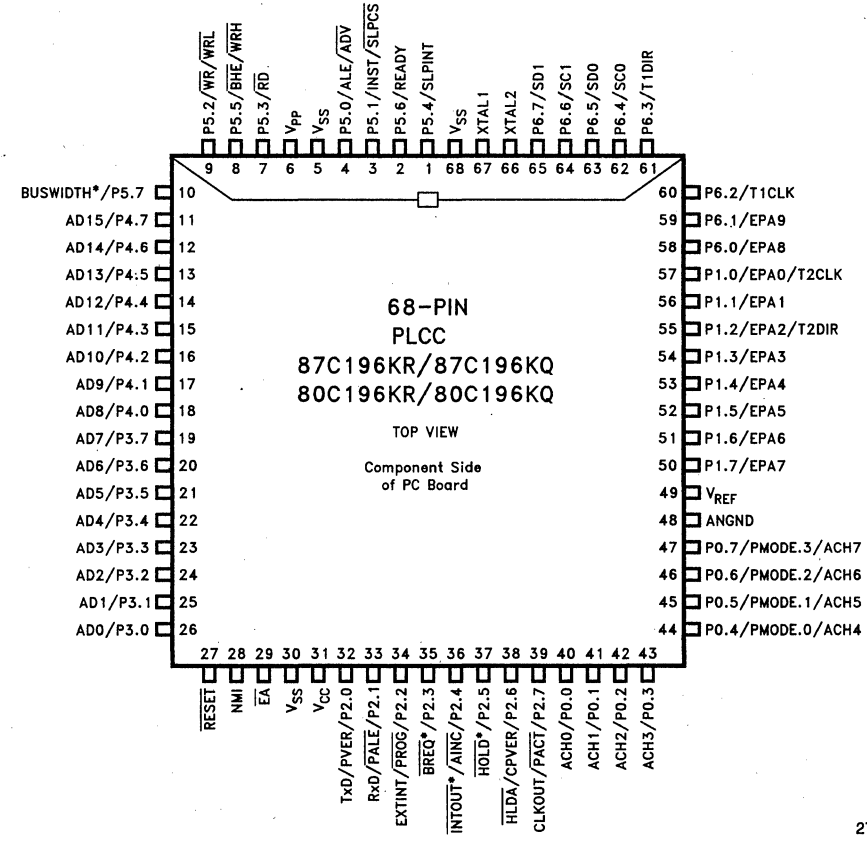
Device	Commercial PLCC	Express PLCC
80C196KR	N80C196KR	*TN80C196KR
80C196JR	N80C196JR	*TN80C196JR
80C196KQ	N80C196KQ	*TN80C196KQ
80C196JQ	N80C196JQ	*TN80C196JQ
87C196KR	N87C196KR	*TN87C196KR
87C196JR	N87C196JR	*TN87C196JR
87C196KQ	N87C196KQ	*TN87C196KQ
87C196JQ	N87C196JQ	*TN87C196JQ

*T = Extended Temperature, no burn-in.

Table 2. Thermal Characteristics

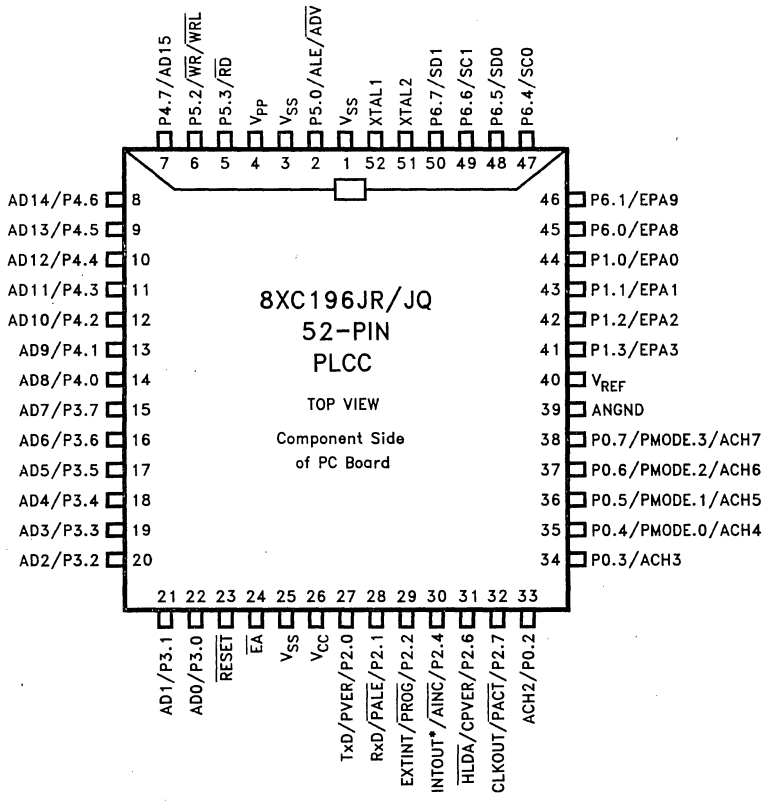
Package	θ_{ja}	θ_{jc}
52-Lead PLCC	35°C/W	12°C/W
68-Lead PLCC	35°C/W	13°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See Intel *Packaging Handbook,* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



NOTE:
*In earlier versions of documentation these pins were referred to as:
$\overline{\text{INTOUT}}$ → $\overline{\text{INTINTOUT}}$
$\overline{\text{BREQ}}$ → $\overline{\text{INTB}}$
BUSWIDTH → BUSW
$\overline{\text{HOLD}}$ → $\overline{\text{HLD}}$

Figure 2. Package Diagrams



NOTE:
*In earlier versions of documentation these pins were referred to as:
$\overline{\text{INTOUT}}$ → $\overline{\text{INTINTOUT}}$
$\overline{\text{BREQ}}$ → $\overline{\text{INTB}}$
BUSWIDTH → BUSW
$\overline{\text{HOLD}}$ → $\overline{\text{HLD}}$

Figure 2. Package Diagrams (Continued)

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the OTPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit. If this function is not used, V_{PP} must be tied to V_{CC}.
ACH0–ACH7/PORT0	Analog inputs to the on-chip A/D converter.
$\overline{AINC}$	Input to automatically increment the address when in Programming mode.
ALE/$\overline{ADV}$/P5.0	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options allow a latch to demultiplex the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. When the pin is ALE, the address can be latched on the falling edge. ALE/$\overline{ADV}$ is active only during external memory accesses. Can be used as standard I/O when not used as ALE.
$\overline{BHE}$/$\overline{WRH}$/P5.5	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory cycles. Can be used as standard I/O when not used as $\overline{BHE}$/$\overline{WRH}$.
$\overline{BREQ}$/P2.3	Bus Request output activated when the bus controller has a pending external memory cycle. Can be used as standard I/O when not used as $\overline{BREQ}$.
BUSWIDTH/P5.7	Input for bus width selection. If CCR bit 1 = 1 and CCR1 bit 2 = 1, this pin dynamically controls the Bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. Can be used as standard I/O when not used as BUSWIDTH.
CLKOUT/P2.7	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Can be used as standard I/O when not used as CLKOUT.
CPVER	Cumulative Program Verify output. Indicates when all EPROM locations program correctly.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ = 1 causes memory accesses from locations 2000H to 5FFFH to be directed to on-chip EPROM/ROM. $\overline{EA}$ = 0 causes all memory accesses to be directed to off-chip memory. $\overline{EA}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{EA}$ is latched at reset.
EPA0–7/PORT1 EPA8-9/P6.0–6.1	Event Processor Array pin for High Speed capture and compare. EPA0 and EPA2 also function as T2CLK and T2DIR. Can be used as standard I/O when not used as EPA or T2 clock functions.
EXTINT/P2.2	A positive transition on this pin causes a maskable interrupt vector through memory location 203CH. May be used as standard I/O if not used as EXTINT.
$\overline{HLDA}$/P2.6	Bus Hold Acknowledge output indicating release of the bus. Can be used as standard I/O when not used as $\overline{HLDA}$.
$\overline{HOLD}$/P2.5	Bus Hold input requesting control of the bus. Can be used as standard I/O when not used as $\overline{HOLD}$.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
INST/P5.1	Output high during an external memory instruction fetch. INST is valid throughout the bus cycle. INST is low otherwise. Can be used as standard I/O when not used as INST.
$\overline{\text{INTOUT}}$/P2.4	Interrupt output indicating that a pending interrupt requires use of the external bus. Can be used as standard I/O if not used as $\overline{\text{INTOUT}}$.
NMI	A positive transition causes a non-maskable interrupt vector through memory location 203EH. If not used, this pin should be tied to V_{SS}. May be used by Intel Evaluation boards.
$\overline{\text{PACT}}$	Output that indicates when the device is currently programming itself. Not active during slave programming.
$\overline{\text{PALE}}$	Input to latch the address during programming modes.
PMODE.0–PMODE.3	Programming mode select inputs.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port 0 pins should not be left floating. These pins are also used as inputs by EPROM parts to select the Programming Mode.
PORT1	8-bit bidirectional standard I/O port. All of its pins are shared with the EPA.
PORT2	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (TxD, RxD, EXTINT, $\overline{\text{BREQ}}$, $\overline{\text{INTOUT}}$, $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$, CLKOUT).
PORT3 PORT4	8-bit bidirectional standard I/O with open drain outputs. These pins are shared with the multiplexed address/data bus which uses strong internal pullups.
PORT5	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (ALE/$\overline{\text{ADV}}$, INST, $\overline{\text{WR}}$/$\overline{\text{WRL}}$, $\overline{\text{RD}}$, SLPINT, $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, READY, BUSWIDTH).
PORT6	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (EPA8, EPA9, T1CLK, T1DIR, SC0, SD0, SC1, SD1).
$\overline{\text{PROG}}$	Programming mode enable input.
PVER	Program Verify output. Goes high after a byte/word is programmed to indicate a successful operation.
$\overline{\text{RD}}$/P5.3	Read signal output to external memory. $\overline{\text{RD}}$ is low only during external memory reads. Can be used as standard I/O when not used as $\overline{\text{RD}}$.
READY/P5.6	Ready input to lengthen external memory cycles. If READY = 1, CPU operation continues in a normal manner. If READY = 0 with the appropriate timings, the memory controller inserts wait states until the next positive transition of CLKOUT occurs with READY = 1. Can be used as standard I/O when not used as READY.
$\overline{\text{RESET}}$	Reset input to and output from the chip. Held low for at least 16 state times to reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
RXD/P2.1	Receive data input pin for the Serial I/O port. Can be used as standard I/O if not used as RXD.
$\overline{\text{SLPCS}}$	Slave port chip select input pin. Can be used as standard I/O if not used as $\overline{\text{SLPCS}}$.
SLPINT/P5.4	Slave Port Interrupt Output pin. Can be used as standard I/O when not used as SLPINT.
SSIO/P6.4–6.7 (SC0, SD0, SC1, SD1)	Synchronous Serial I/O pins. SC0/SC1 serve as clock pins and SD0/SD1 are data pins. Can be used as standard I/O if not used for serial I/O.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
T1CLK/P6.2	TIMER1 Clock input. The timer increments or decrements on both positive and negative edges. Can be used as standard I/O when not used as T1CLK.
T1DIR/P6.3	TIMER1 Direction input. The timer increments when this pin is high and decrements when this pin is low. Can be used as standard I/O when not used as T1DIR.
T2CLK/P1.0	TIMER2 Clock input. The timer increments or decrements on both positive and negative edges. Can be used as standard I/O when not used as T2CLK.
T2DIR/P1.2	TIMER2 Direction input. The timer increments when this pin is high and decrements when this pin is low. Can be used as standard I/O when not used as T2DIR.
TXD/P2.0	Transmit data output pins for the Serial I/O port. Can be used as standard I/O if not used as TXD.
$\overline{WR}$/$\overline{WRL}$/P5.2	Write and Write Low output to external memory. $\overline{WR}$ will go low for every external write. $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is active only during external memory writes. Can be used as standard I/O when not used as $\overline{WR}$/$\overline{WRL}$.
XTAL1	Input of the oscillator inverter and the internal clock generator. This pin should be used when using an external clock source.
XTAL2	Output of the oscillator inverter.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... −60°C to +150°C

Ambient Temperature under Bias ..... −55°C to +125°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND ..... −0.5V to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation..... 1.0W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

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OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	16	MHz(4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

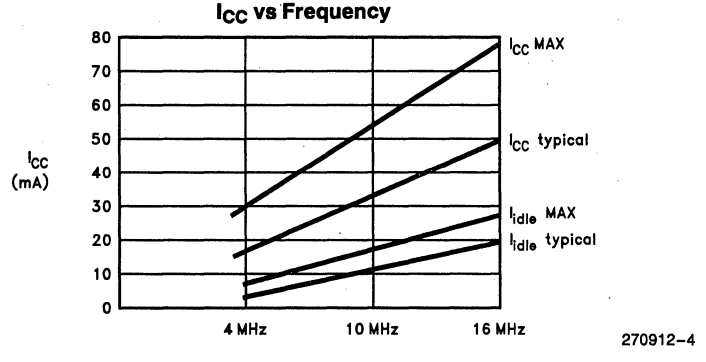
DC CHARACTERISTICS (Over Specified Operating Conditions)(9)

Symbol	Parameter	Min	Typ(6)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (All Pins)	−0.5V		0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Outputs Configured as Push/Pull)			0.3 0.45 1.5	V V V	I_{OL} = 200 μA(3, 5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Outputs Configured as Push/Pull)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA(3, 5, 8) I_{OH} = −3.2 mA I_{OH} = −7.0 mA
V_{OH2}	Output High Voltage in RESET	V_{CC} − 1V			V	I_{OH} = −15 μA(1, 7)
I_{LI}	Input Leakage Current (Std. Inputs)			±10	μA	$V_{SS} < V_{IN} < V_{CC}$ − 0.3V(2)
I_{LI1}	Input Leakage Current (Port 0—A/D Inputs)		±1	±3	μA	$V_{SS} < V_{IN} < V_{REF}$
I_{IH}	Input High Current (NMI)			+175	μA	$V_{SS} < V_{IN} < V_{CC}$ − 0.3V(10)

DC CHARACTERISTICS (Over Specified Operating Conditions)(9) (Continued)

Symbol	Parameter	Min	Typ(6)	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		60	75	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While Device in Reset)
I_{REF}	A/D Reference Supply Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current(6)		50	TBD	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz
R_{WPU}	Weak Pullup Resistance (Approx)		150K		Ω	(6)

NOTES:
1. All BD (Bidirectional) pins except INST and CLKOUT. BD pins include Port1, Port2, Port3, Port4, Port5 (as a port), and Port6.
2. Standard Input pins include XTAL1, $\overline{EA}$, $\overline{RESET}$, and Port 1/2/3/4/5/6 when setup as inputs.
3. All Bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is Static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{OL}/I_{OH} currents per pin will be characterized and published at a later date.
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.0V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. This specification applies to P3/4 only when used as an address bus supplying the address.
9. All voltages are referenced relative to V_{SS}. When used, V_{SS} refers to the device pin.
10. Worst case is at upper limit of test conditions.



NOTES:
I_{CC} Max = 3.88 × FREQ + 13.43
I_{idle} Max = 1.65 × FREQ + 2.2

AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 87C196KR/KQ/JR/JQ:

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC}-75$	ns(2)
T_{LLYV}	ALE Low to READY Setup		$T_{OSC}-70$	ns(2)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC}-30$	ns(1, 2)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC}-15$	$2T_{OSC}-40$	ns(1, 2)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC}-75$	ns(2)
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC}-60$	ns(2)
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns(2)
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC}-55$	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC}-22$	ns
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC}-50$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns

NOTE:
1. If max is exceeded, additional wait states will occur.
2. Does not apply to JR/JQ.

AC CHARACTERISTICS (Over Specified Operating Conditions)

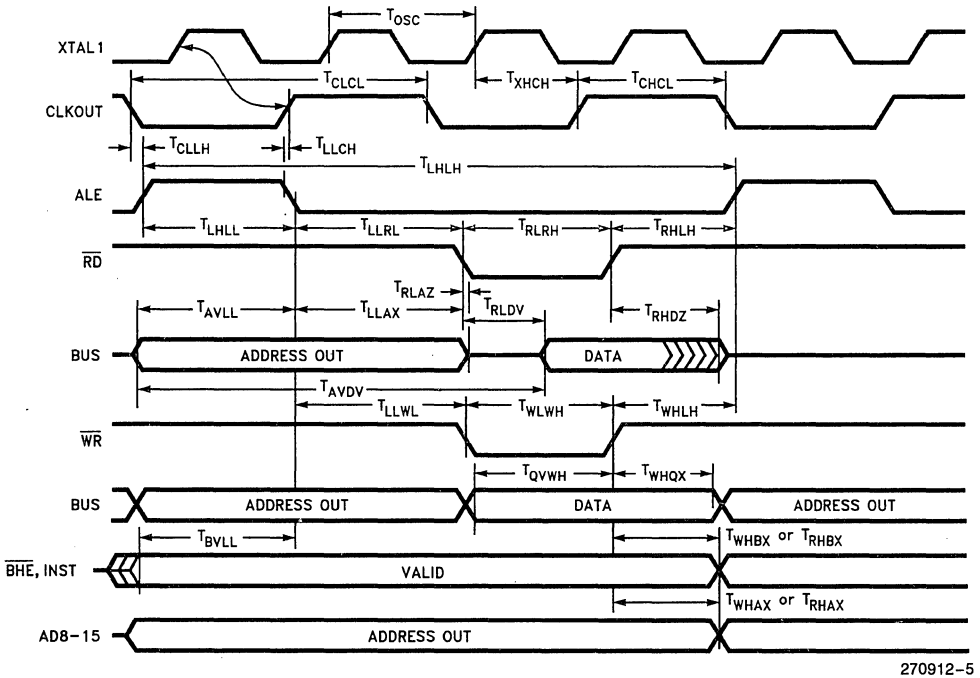
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 87C196KR/KQ/JR/JQ will meet these specifications.

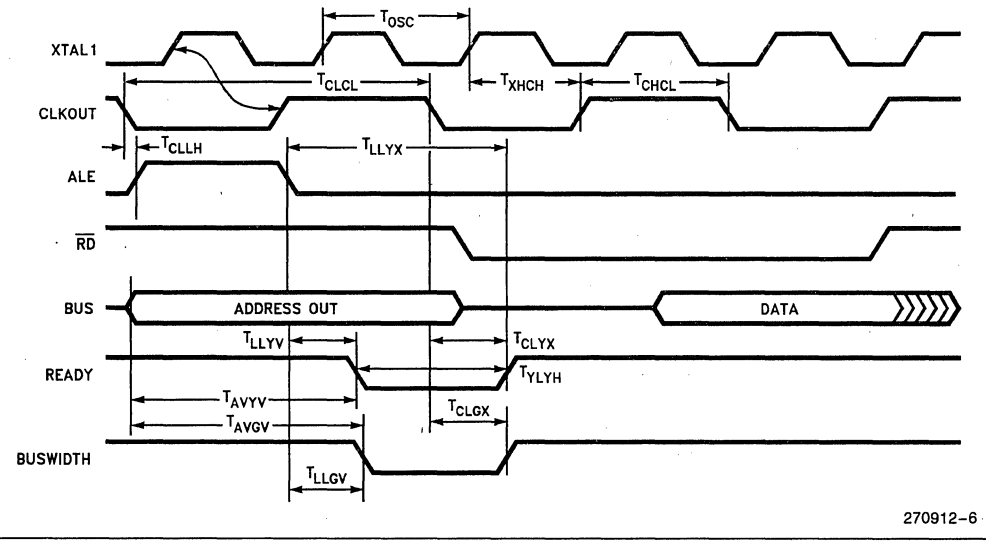
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	4.0	16.0	MHz(1)
T_{OSC}	Oscillator Period (1/Fxtal)	62.5	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns(2)
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	$T_{OSC}-10$	$T_{OSC}+15$	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	15	ns
T_{LLCH}	ALE/$\overline{ADV}$ Falling Edge to CLKOUT Rising	−20	15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Period	$T_{OSC}-10$	$T_{OSC}+10$	ns
T_{AVLL}	Address Setup to ALE/$\overline{ADV}$ Falling Edge	$T_{OSC}-15$		ns
T_{LLAX}	Address Hold after ALE/$\overline{ADV}$ Falling Edge	$T_{OSC}-40$		ns
T_{LLRL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC}-30$		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC}-5$		ns(5)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge	T_{OSC}	$T_{OSC}+25$	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC}-10$		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	−5	25	ns
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC}-23$		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC}-30$		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-25$		ns
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge	$T_{OSC}-10$	$T_{OSC}+15$	ns(3)
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-10$		ns(6)
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-30$(4)		ns
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ Rising Edge	$T_{OSC}-10$		ns(6)
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	$T_{OSC}-30$(4)		ns
T_{BVLL}	BHE Valid to ALE Falling Edge	$T_{OSC}-15$		ns(6)

NOTES:
1. Testing performed at 4.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 $T_{OSC} \times n$, where n = number of wait states.
6. Does not apply to JR/JQ.

System Bus Timing



Buswidth Timings



HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	65		ns	(1, 2)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	15	ns	(2)
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	15	ns	(2)
T_{AZHAL}	HLDA Low to Address Float		25	ns	(2)
T_{BZHAL}	HLDA Low to BHE, INST, RD, WR Weakly Driven		25	ns	(2)
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	(2)
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	(2)
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	(2)
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	−10		ns	(2)
T_{CLLH}	CLKOUT Low to ALE High	−10	15	ns	

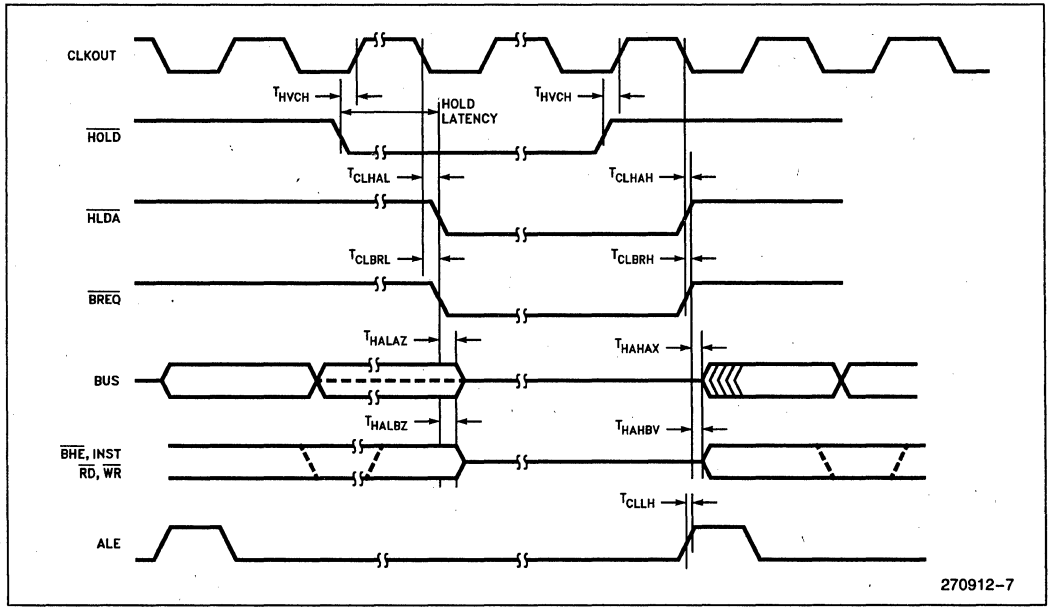
NOTE:
1. To guarantee recognition at next clock.
2. Does not apply to JR/JQ.

HOLD LATENCY

	Max
Internal Access	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

DC SPECIFICATIONS IN HOLD

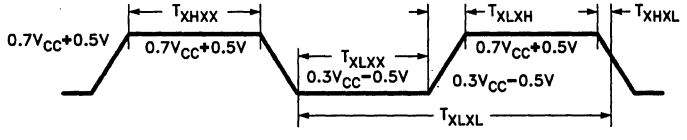
Parameter	Min	Max	Units
Weak Pullups on ADV, RD, WR, WRL, BHE	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4V



EXTERNAL CLOCK DRIVE

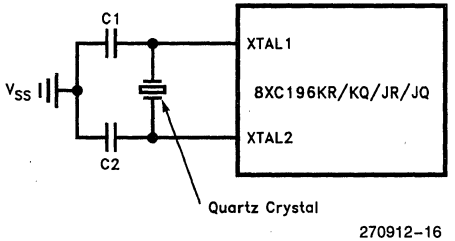
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4.0	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	250	ns
T_{XHXX}	High Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



270912-8

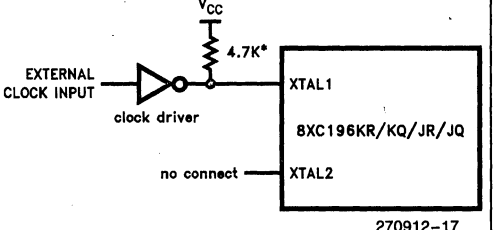
EXTERNAL CRYSTAL CONNECTIONS



270912-16

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using quartz crystals, typically C1 ≈ 22 pF and C2 ≈ 22 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

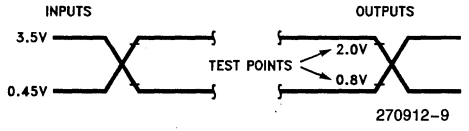
EXTERNAL CLOCK CONNECTIONS



270912-17

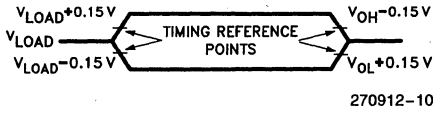
*Required if TTL driver used.
Not needed if CMOS driver is used.

AC TESTING INPUT, OUTPUT WAVEFORMS



NOTE:
AC Testing Inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS



NOTE:
For Timing Purposes a Port Pin is no longer floating when a 150 mV change from Load Voltage Occurs and Begins to Float when a 150 mV change from the Loading V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \leq 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
BR— $\overline{BREQ}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
Q— Data Out
R— $\overline{RD}$
W— $\overline{WR}/\overline{WRH}/\overline{WRI}$
X— XTAL1
Y— READY

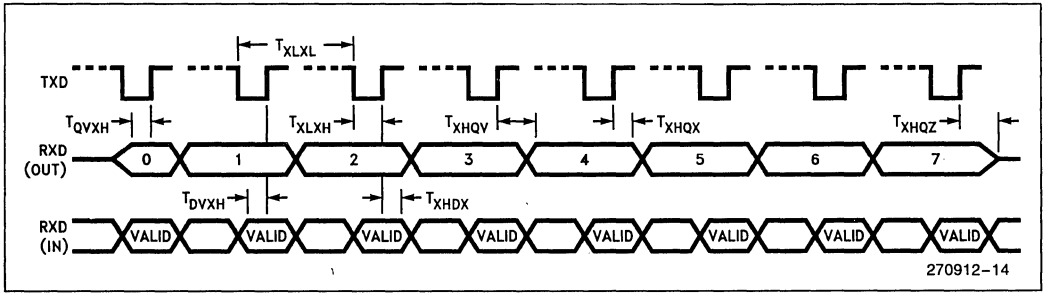
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE (MODE 0)

SERIAL PORT TIMING—SHIFT REGISTER MODE (Over Specified Operating Conditions)
Test Conditions: Load Capacitance = 100 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	$8\ T_{OSC}$		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	$4\ T_{OSC}-50$	$4\ T_{OSC}+50$	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	$3\ T_{OSC}$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	$2\ T_{OSC}-50$		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		$2\ T_{OSC}+50$	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	$2\ T_{OSC}+200$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		$5\ T_{OSC}$	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE (MODE 0)

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



A TO D

The speed of the A/D converter in the 10-bit or 8-bit modes can be adjusted by setting the AD_TIME special function register to the appropriate value. The AD_TIME register only programs the speed at which the conversions are performed, not the speed it can convert correctly.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

A/D CONVERTER SPECIFICATION

After a conversion is started, the device is placed in the IDLE mode until the conversion is complete. Testing is performed at V_{REF} = 5.12V.

There is an AD_TEST register that allows for conversion on ANGND and V_{REF} as well as zero offset adjustment. The Absolute Error listed is WITHOUT doing any adjustments.

10-BIT A/D OPERATING CONDITIONS(1)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50(2)	V
T_{SAM}	Sample Time	2.0		μs(3)
T_{CONV}	Conversion Time	16.5	19.5	μs(3)
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5V.
3. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical (1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3	LSBs
Differential Non-Linearity		> −0.5	+0.5	LSBs
Channel-to-Channel Matching	±0.1	0	±1	LSBs
Repeatability	±0.25	0		LSBs
Temperature Coefficients: Offset Fullscale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	1.2K	Ω(4)
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V
Sampling Capacitor	2			pF
DC Input Leakage		0	±3	μA

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal multiplexer, to sample capacitor.

8-BIT A/D OPERATING CONDITIONS(1)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50(2)	V
T_{SAM}	Sample Time	2.0		µs(3)
T_{CONV}	Conversion Time	16.5	19.5	µs(3)
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5V.
3. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

The 8-bit mode trades off resolution for a faster conversion time. The AD_TIME register must be used when performing an 8-bit conversion.

Parameter	Typ(1)	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±2	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±2	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB(2, 3)	
Feedthrough	−60			dB(2)	
V_{CC} Power Supply Rejection	−60			dB(2)	
Input Series Resistance		750	1.2K	Ω	
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V	
Sampling Capacitor	2			pF	
DC Input Leakage		0	±3	µA	

NOTES:
*An "LSB", as used here, has a value of approximately 20 mV.
1. Typical values are expected for most devices at 25°C.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal multiplexer, to sample capacitor.

OTPROM PROGRAMMING

OPERATING CONDITIONS DURING PROGRAMMING(3)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}	Supply Voltage during Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage during Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	$\overline{EA}$ Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).

AC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(1)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the word dump mode. For programming pulses use 100 μs.

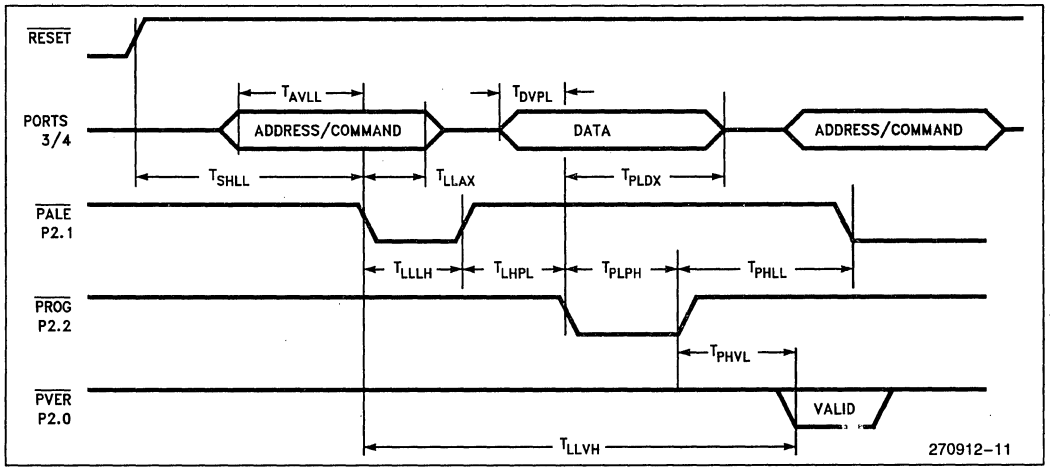
DC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		100	mA

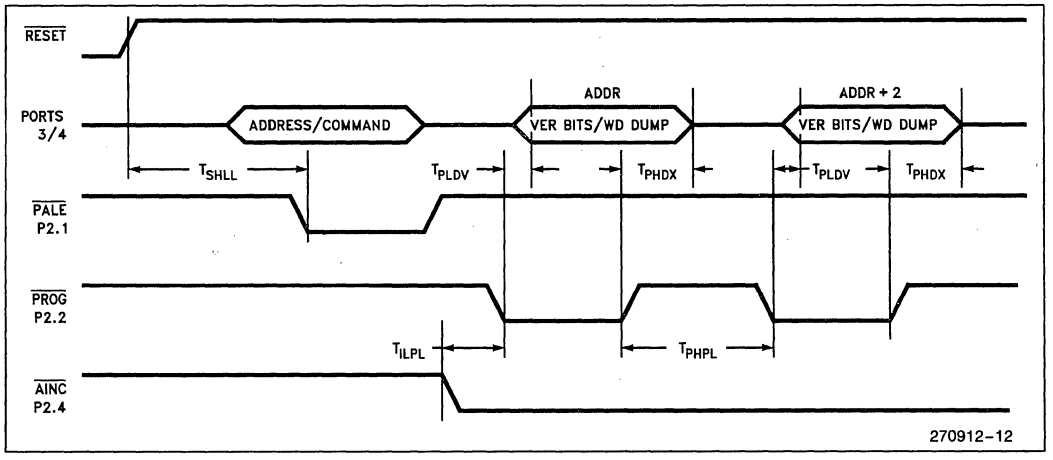
NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

OTPROM PROGRAMMING WAVEFORMS

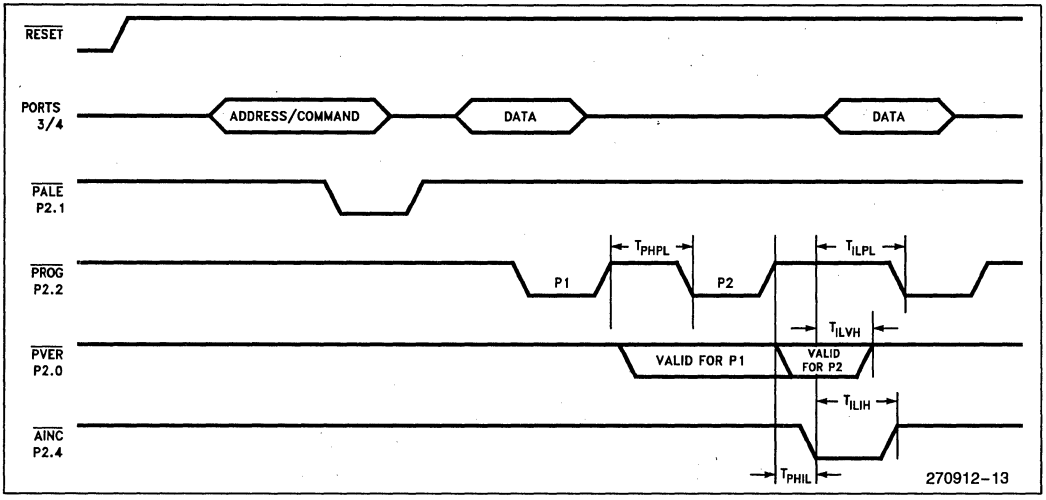
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



87C196KR/87C196JR ERRATA

1. I_{0H2}

Current devices do not meet the test condition for V_{OH2} of -15 μA. Instead the devices are guaranteed to source a minimum of -6 μA.

87C196KR/87C196JR DESIGN CONSIDERATIONS

1. EPA Timers

Special care must be taken when resetting/writing the EPA timers. This is more of a software technique than a device errata. For example: The EPA timers do not generate a "time valid" signal when the counter is either reset or written. This means that if a compare event is programmed in the EPA/Compare channel for a value of "0000H" (when reset) or equal to a written value, the compared event will NOT happen. However, if the timers are allowed to increment/decrement to that value, that compare event WILL occur.

2. Port 6.4, 6.5, 6.6, 6.7

The user is not allowed to modify the P6_REG register when these pins are configured as Special Function P6_MODE.x = 1). During software manipulation of these registers, it is a good practice to first change the P6_MODE register, then modify the P6_REG register when switching from SF to LSIO.

3. P2.7 (CLKOUT)

Port 2.7 (CLKOUT) does not operate in open drain mode.

4. Current versions of the 8XC196KQ/JQ are fabricated with 16K of internal OTPROM, 512 bytes of register RAM, and 256 bytes of internal RAM. The memory map of the 8XC196KQ/JQ is identical to the 8XC196KR/JR. However, the extra memory locations are not tested and should not be used. Intel may disable this extra memory on future versions of the 8XC196KQ/JQ. Any software that relies on reading or writing these locations may not function correctly on future devices.

   Two steps the user should always incorporate to insure future compatibility are:

   A) The program must contain a jump to a location greater than 16K before the 12K boundary is reached. This is necessary only if greater than 12K of program memory is required and portions of the program executes from internal OTPROM.

   B) Use program memory from 12K to 16K only if $\overline{EA}$ is tied to ground. Never use data memory from 180H to 1FFH or from 480H to 4FFH.

52-LEAD DEVICES

Intel offers a 52-lead version of the 87C196KR device: the 87C196JR and 87C196JQ devices.

It is important to point out some functionality differences because of future devices or to remain software consistent with the 68-lead device. Because of the absence of pins on the 52-lead device some functions are not supported.

52-Lead Unsupported Functions:
- Analog Channels 0 and 1
- INST Pin Functionality
- SLPINT Pin Support
- HLD/HLDA Functionality
- External Clocking/Direction of Timer1
- WRH or BHE Functions
- Dynamic Buswidth
- Dynamic Wait State Control

The following is a list of recommended practices when using the 52-lead device:

(1) **External Memory.** Use an 8-bit bus mode only. There is neither a WRH or BUSWIDTH pin. The bus cannot dynamically switch from 8- to 16-bit or vice versa. Set the CCB bytes to an 8-bit only mode, using WR function only.

(2) **Wait State Control.** Use the CCB bytes to configure the maximum number of wait states. If the READY pin is selected to be a system function, the device will lockup waiting for READY. If the READY pin is configured as LSIO (default after RESET), the internal logic will receive a logic "0" level and insert the CCB defined number of wait states in the bus cycle. DON'T USE IRC = "111".

(3) **NMI Support.** The NMI is not bonded out. Make the NMI vector at location 203Eh vector to a Return instruction. This is for glitch safety protection only.

(4) **Auto-Programming Mode.** The 52-lead device will ONLY support the 16-bit zero wait state bus during auto-programming.

(5) **EPA4 through EPA7.** Since the JR and JQ devices use the KR silicon, these functions are in the device, just not bonded out. A programmer can use these as compare only channels or for other functions like software timer, start and A/D, or reset timers.

(6) **Slave Port Support.** The Slave port can still be used on the 52-lead devices. The only function removed is the SLPINT output function.

(7) **Port Functions.** Some port pins have been removed. P5.7, P5.6, P5.5, P5.1, P6.2, P6.3, P1.4 through P1.7, P2.3, P2.5, P0.0 and P0.1. The Px_REG, Px_MODE, and Px_DIR registers can still be updated and read. The programmer should not use the corresponding bits associated with the removed port pins to conditionally branch in software. Treat these bits as RESERVED.

Additionally, these port pins should be setup internally by software as follows:

1. Written to Px_REG as "1" or "0".
2. Configured as Push/Pull, Px_DIR as "0".
3. Configured as LSIO.

This configuration will effectively strap the pin either high or low. *DO NOT Configure as Open Drain output "1", or as an Input pin. This device is CMOS.*

REVISION HISTORY

This data sheet (270912-003) supercedes 270912-002 and is valid for devices with a "C" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify that you have the latest version before finalizing a design or ordering devices.

1. Removed the following errata:
   - Slave Programming Mode
   - EPA__MASK1/EPA__PEND1
   - BMOVI
   - PTS and Other Interrupts
   - Serial Port Framing Error
   - Remap Mode on EPA3
   - A/D Abort
   - PTS/NMI Conflict
   - Data Output Register Cleared
   - Divide Error during HOLD/READY
   - SIO Mode 0
   - EPAIPV Multiplied by Two
   - (These were fixed on the C-step)
2. Moved the following from Errata to Design Considerations:
   - EPA Timers
   - Port 6.4, 6.5, 6.6, 6.7 (and reworded)
   - P2.7 (CLKOUT)
   - Oscillator Noise Sensitivity
3. Added New Errata:
   - I_{OH2} (also existed on A-step)
4. Added SLPCS to Package Diagrams and Pin Descriptions
5. Added T_{BVLL}
6. Added I_{IH} for NMI
7. Added notes to AC Characteristics identifying specifications that do not apply to JR/JQ
8. Changed T_{CLLH} from -5 ns to -10 ns under HOLD/HLDA Timings
9. Changed T_{HVCH} from 55 ns to 65 ns
10. Changed T_{AZHAL} from 10 ns to 25 ns
11. Changed T_{BZHAL} from 10 ns to 25 ns
12. Changed I_{CC} (max) from 70 mA to 75 mA
13. Changed I_{CC} formula from (3.88 $\times$ Freq + 8.43) to (3.88X Freq + 13.43)
14. Changed V_{OH2} test point from -50 μA to -15 μA
15. Changed Note 1 in DC parameters
16. Changed External Clock min/max, high/low times from percentage to ratio of T_{OSC}
17. Removed NMI from standard inputs (Note 2 under DC Characteristics)
18. Removed V_{OL1} spec
19. Removed T_{CLBV}
20. Added JQ/KQ design consideration

Data sheet 270912-002 supercedes 270912-001 and is valid for devices with an "A" at the end of the topside tracking number.

1. Removed:
   - CPU features descriptions
   - Peripheral features descriptions
   - SFR Operation (placed in Quick Reference)
   - SFR Maps (placed in Quick Reference)
   - SFR Bit Maps (placed in Quick Reference)
   - I_{IL} in DC Characteristics
   - T_{CLHAL} Max and T_{CLBRH} Max
   - Incorrect Sample and Convert time table from 8-bit A/D
2. Added:
   - Express options
   - Bullets on front page
   - Memory Map
   - Process Information
   - Prefix Identification
   - Thermal Characteristics
   - Programming functions to pin-out and pin descriptions
   - Ambient Temperature under Bias to Absolute Maximum Ratings
   - Note relating to Power Dissipation in Absolute Maximum Rating
   - Notes 8 and 9 to DC Characteristics
   - T_{CLBV} to AC Characteristics
   - Title to Buswidth timing diagram
   - T_{YLYH} to Buswidth timing diagram
   - Hold latency spec
   - External Crystal Connection diagram
   - External Clock Connection diagram
   - 10-bit A/D Operating Conditions Table
   - Title to 10-bit and 8-bit mode A/D Characteristics
   - Voltage on Analog Input Pin specification
   - Sampling Capacitor typical value
   - Note 4 to 10-bit and 8-bit A/D Specifications
   - 8-bit A/D Operating Conditions Table

Off Isolation, Feedthrough, V_{CC} Power Supply Rejection, Input Series Resistance, Voltage on Analog Input Pin, Sampling Capacitor and DC Input Leakage to 8-bit A/D specifications

Notes 1, 2 and 3 to EPROM Programming Conditions

New Errata (Items 10 to 16)

3. Changed:

Title of data sheet from "8XC196KR/KQ/JR/JQ 16-BIT HIGH PERFORMANCE CHMOS MICROCONTROLLER" to "8XC196KR/KQ/JR/JQ COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER"

Several bullets on cover sheet

Register RAM numbers in table on front page to match device

Operating conditions to tabular format

Note 1 in DC Characteristics to include Ports 3 and 4

0 to V_{SS} for I_{LI} and I_{LI1} in DC Characteristics

Format of symbols in AC Characteristics

T_{CLCH} to T_{CLLH} in System Bus Timing diagram

T_{XLXL} Max from 286 ns to 250 ns

T_{XHXX} from T_{OSC} − 44 ns to 35%/65%

T_{XLXX} from T_{OSC} − 44 ns to 35%/65%

T_{XLXH} from T_{OSC} − 50 ns to 10 ns

T_{XHXL} from T_{OSC} − 50 ns to 10 ns

AC Testing Input, Output Waveform

Introductory text on A to D Characteristics and Converter Specification

DC Input Leakage from ±1 μA to ±3 μA in A/D Specifications.

Power Dissipation from 0.5W to 1.0W.

Wording in Float Waveform from 100 mV to 150 mV.

EPROM Programming Characteristics to Operating Conditions table.

Data sheet (270912-001) is valid for devices with an "A" at the end of the topside tracking number. This is the first version of the data sheet.

8XC196NT/8XC196NQ and 8XC196KT Data Sheets

20

8XC196NT/8XC196NQ CHMOS MICROCONTROLLER WITH 1 MBYTE LINEAR ADDRESS SPACE

- High Performance CHMOS 16-Bit CPU
- Up to 32 Kbytes of On-Chip EPROM
- Up to 1 Kbyte of On-Chip Register RAM
- Up to 512 Bytes of Additional RAM (Internal RAM)
- Register-Register Architecture
- 4 Channel/10-Bit A/D with Sample/Hold
- 37 Prioritized Interrupt Sources
- Up to Seven 8-Bit (56) I/O Ports
- Full Duplex Serial I/O Port
- Dedicated Baud Rate Generator
- Interprocessor Communication Slave Port
- Selectable Bus Timing Modes for Flexible Interfacing
- Oscillator Fail Detection Circuitry
- High Speed Peripheral Transaction Server (PTS)
- Two Dedicated 16-Bit High-Speed Compare Registers
- 10 High Speed Capture/Compare (EPA)
- Full Duplex Synchronous Serial I/O Port (SSIO)
- Two Flexible 16-Bit Timer/Counters
- Quadrature Counting Inputs
- Flexible 8-/16-Bit External Bus (Programmable)
- Programmable Bus (HOLD/HLDA)
- 1.75 μs 16 x 16 Multiply
- 3 μs 32/16 Divide
- 68-Pin Package

Device	Pins/Package	EPROM	Reg RAM	Code RAM	Address Space	I/O	EPA	A/D
8XC196NT	68P PLCC	32K	1K	512	1 Mbyte	56	10	4
8XC196NQ	68P PLCC	12K	360	128	1 Mbyte	56	10	4

X = 7 EPROM Device

The 8XC196NT 16-bit microcontroller is a high performance member of the MCS(r)-96 microcontroller family. The 8XC196NT is an enhanced 8XC196KR device with 1 Mbyte linear address space, 1000 byte register RAM, 512 bytes internal RAM, 16 MHz operation and an optional 32 Kbytes of ROM/EPROM. Intel's CHMOS III-E process provides a high performance processor along with low power consumption.

The 8XC196NT has a maximum guaranteed frequency of 16 MHz. Unless otherwise noted, all references to the 8XC196NT also refer to the 8XC196NQ.

Ten high-speed capture/compare modules are provided. As capture modules event times with 250 ns resolution can be recorded and generate interrupts. As compare modules events such as toggling of a port pin, starting an A/D conversion, pulse width modulation, and software timers can be generated. Events can be based on the timer or up/down counter.

October 1992
Order Number: 272267-001

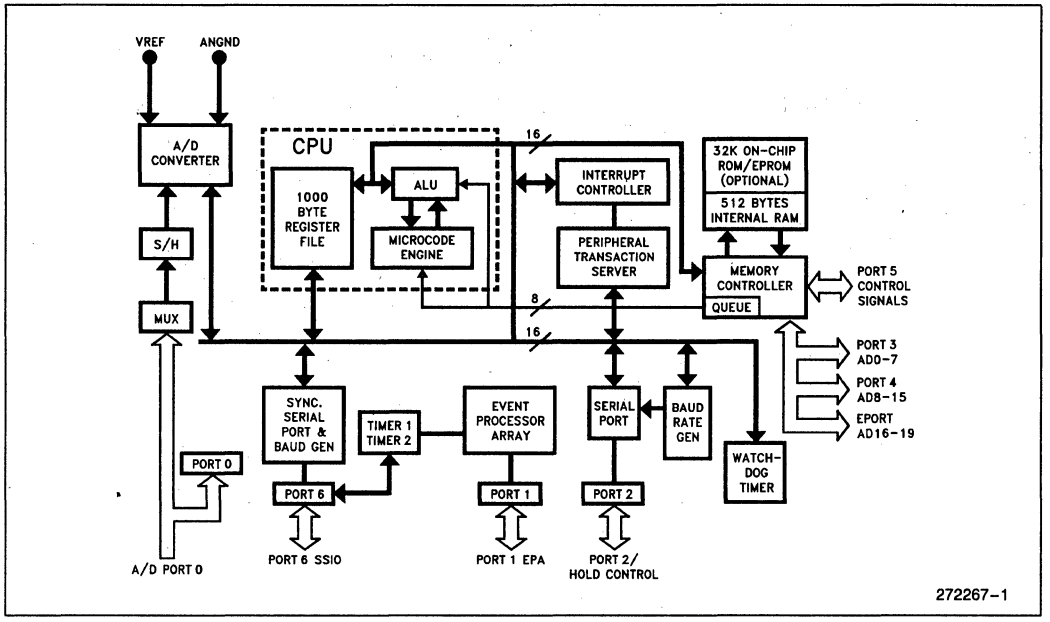


Figure 1. 8XC196NT Block Diagram

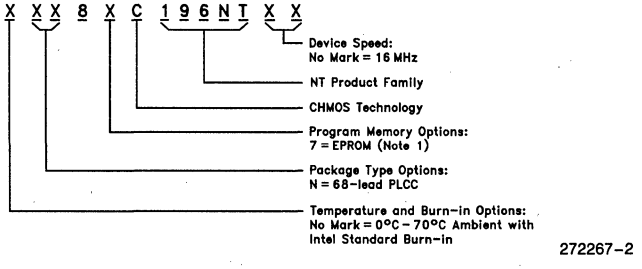
PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
PLCC	36.5°C/W	13°C/W



EXAMPLE: N87C196NT is 68-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 3. The 8XC186NT Familiy Nomenclature

8XC196NT Memory Map

Address	Description
FFFFFFH FFA000H	External Memory
FF9FFFH FF2080H	Internal EPROM or External Memory (Determined by $\overline{EA}$ Pin) RESET at FF2080H
FF207FH FF2000H	Reserved Memory (Internal EPROM or External Memory) (Determined by $\overline{EA}$ Pin)
FF1FFFH FF0600H	External Memory
FF05FFH FF0400H	Internal RAM (Identically Mapped into 00400H–005FFH)
FF03FFH FF0100H	External Memory
FF00FFH FF0000H	Reserved for ICE
FEFFFFH 100000H	External Memory for future devices
0FFFFFH 0A000H	984 Kbytes External Memory
09FFFH 02080H	Internal EPROM or External Memory (Note 1)
0207FH 02000H	Reserved Memory (Internal EPROM or External Memory) (Notes 1, 3, and 6)
01FFFH 01FE0H	Memory Mapped Special Function Registers (SFR's)
01FDFH 01F00H	Internal Special Function Registers (SFR's) (Note 5)
01EFFH 00600H	External Memory
005FFH 00400H	Internal Code or Data RAM (Address with Indirect or Indexed Modes)
003FFH 00100H	Register RAM } Upper Register File (Address with Indirect or Indexed Modes or through Windows.) (Note 2)
000FFH 00018H	Register RAM } Lower Register File (Address with Direct, Indirect, or Indexed Modes.) (Notes 2, 4)
00017H 00000H	CPU SFR's } Lower Register File (Address with Direct, Indirect, or Indexed Modes.) (Notes 2, 4)

NOTES:
1. These areas are mapped internal EPROM if the REMAP bit (CCB2.2) is set and EA = H. Otherwise they are external memory.
2. Code executed in locations 00000H to 003FFH will be forced external.
3. Reserved memory locations must contain 0FFH unless noted.
4. Reserved SFR bit locations must be written with 0.
5. Refer to 8XC196NT for SFR descriptions.
6. **WARNING:** The contents or functions of reserved memory locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.
7. The 8XC196NT internally uses 24 bit address, but only 20 address lines are bonded out allowing 1 Mbyte external address space.

8XC196NT/NQ EXTENDED ADDRESSING INSTRUCTIONS

There are 9 new instructions which have been implemented to support extended addressing in the 8XC196NT family.

For the following examples, wreg is a word register, treg is a 32-bit register (only the lower 24 bits are used for addressing) which must be long word aligned (divisable by 4), and XXX is a 24-bit offset. wreg and treg must be located in the lower register file.

ELD Extended Load. May be used in the following addressing modes:

ELD wreg,[treg]	Indirect Mode
ELD wreg,[treg] +	Indirect Autoincrement Mode
ELD wreg,XXX[treg]	Extended Indexed Mode

ELDB Extended Load Byte. May be used in the following addressing modes:

ELDB wreg,[treg]	Indirect Mode
ELDB wreg,[treg] +	Indirect Autoincrement Mode
ELDB wreg,XXX[treg]	Extended Indexed Mode

EST Extended Store. May be used in the following addressing modes:

EST wreg,[treg]	Indirect Mode
EST wreg,[treg] +	Indirect Autoincrement Mode
EST wreg,XXX[treg]	Extended Indexed Mode

ESTB Extended Store Byte. May be used in the following addressing modes:

ESTB wreg,[treg]	Indirect Mode
ESTB wreg,[treg] +	Indirect Autoincrement Mode
ESTB wreg,XXX[treg]	Extended Indexed Mode

EBMOV Extended Block Move (non-interruptable). For the following example, ereg is a quad-word (64-bit) register, which must be aligned on quad word boundary (divisable by 8). The source of the block is a 24-bit address at location ereg, and the destination of the block is a 24-bit address at location ereg + 4. wreg is a word register containing the number of words to move. ereg and wreg must be in the lower register file.

```
EBMOV ereg, wreg
```

EBMOVI Interruptable Extended Block Move. Identical to EBMOV except EBMOVI is interruptable.

```
EBMOVI ereg, wreg
```

EJMP Extended Jump. Functional in 24-bit mode only (MODE16 = 0). This is an unconditional relative jump. The distance from the end of this instruction to the target label is added to the 24-bit program counter, effecting the jump. The target label may be anywhere in the 1 Mbyte address space.

```
EJMP any_label
```

EBR Extended Branch. Indirect unconditional jump functional in 24-bit mode only (MODE16 = 0). The 24-bit program counter is loaded with the 24-bit address contained in treg. Program execution continues at the address specified in treg.

```
EBRI [treg]
```

ECALL Extended Call. Functional in 24-bit mode only (MODE16 = 0). The contents of the 24-bit program counter are pushed on the stack in two words (32 bits). Then the distance from the target label is added to the 24-bit program counter, effecting the call. The target label may be anywhere in the 16M address space.

```
. ECALL any_subroutine
```

NOTES:

The new extended instructions support 24-bit addressing, but the 8XC196NT only supports accessing 1 Mbyte external memory.

When operating in the 24-bit mode (MODE16 = 0), all calls, returns, and interrupts always push/pop 4 bytes on the stack. Extra state times are required for this operation, so code using these instructions will execute slower than code in 16-bit mode.

Location 00H (the "zero" register) will always be read as zero, even when read as double word.

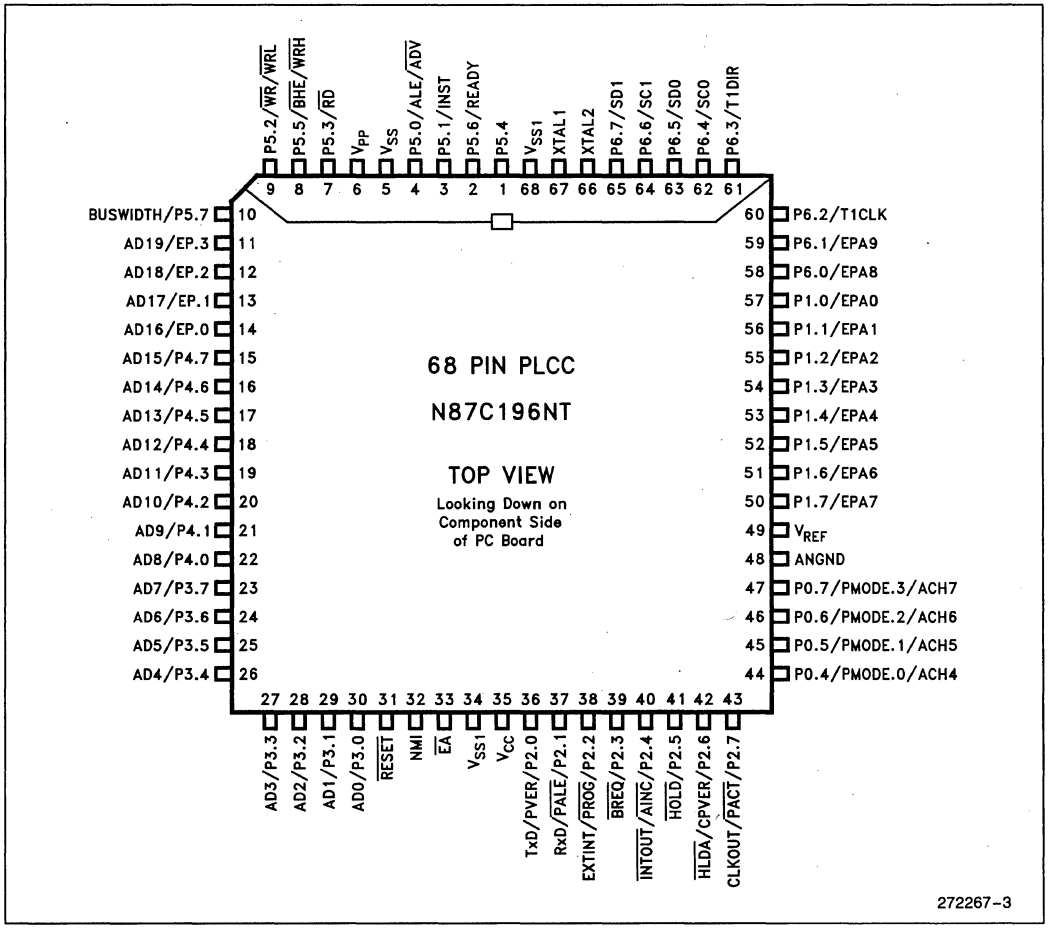


Figure 2. 68-Pin PLCC Package Diagram

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}, V_{SSI}, V_{SSI}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
P.27/CLKOUT	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Also LSIO pin.
$\overline{RESET}$	Reset input to and open-drain output from the chip. $\overline{RESET}$ has an internal pullup.
P5.7/BUSWIDTH	Input for bus width selection. If CCR bit 1 is a one and CCR1 bit 2 is a one, this pin dyamically controls the Buswidth of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs, if BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is "0" and CCR1 bit 2 is "1", all bus cycles are 8-bit, if CCR bit 1 is "1" and CCR1 bit 2 is "0", all bus cycles are 16-bit. CCR bit 1 = "0" and CCR1 bit 2 = "0" is illegal. Also an LSIO pin when not used as BUSWIDTH.
NMI	A positive transition causes a non maskable interrupt vector through memory location 203EH.
P5.1/INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches, during internal EPROM fetches INST is held low. Also LSIO when not INST.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a high causes memory accesses to locations 0FF2000H through 0FF9FFFH to be directed to on-chip EPROM/ROM. $\overline{EA}$ equal to a low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{EA}$ is latched at reset.
$\overline{HOLD}$	Bus Hold Input requesting control of the bus.
$\overline{HLDA}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{BREQ}$	Bus Request output activated when the bus controller has a pending external memory cycle.
P5.0/ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. $\overline{ADV}$ can be used as a chip select for external memory. ALE/$\overline{ADV}$ is active only during external memory accesses. Also LSIO when not used as ALE.
P5.3/$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is active only during external memory reads or LSIO when not used as $\overline{RD}$.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
P5.2/$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR, $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is active during external memory writes. Also an LSIO pin when not used as $\overline{WR}$/$\overline{WRL}$.
P5.5/$\overline{BHE}$/$\overline{WRH}$	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects that bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{BHE}$ = 1), to the high byte only (A0 = 1, $\overline{BHE}$ = 0) or both bytes (A0 = 0, $\overline{BHE}$ = 0). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory write cycles. Also an LSIO pin when not BHE/$\overline{WRH}$.
P5.6/READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The max number of wait states inserted into the bus cycle is controlled by the CCR/ CCR1. Also an LSIO pin when READY is not selected.
P5.4/SLPINT	Dual function I/O pin. As a bidirectional port pin or as a system function. The system function is a Slave Port Interrupt Output Pin.
P6.2/T1CLK	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Clock input. The TIMER1 will increment or decrement on both positive and negative edges of this pin.
P6.3/T1DIR	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Direction input. The TIMER1 will increment when this pin is high and decrements when this pin is low.
PORT1/EPA0–7 P6.0–6.1/EPA8–9	Dual function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare. EPA0 and EPA2 have yet another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH4–7	4-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts to select the Programming Mode.
P6.3–6.7/SSIO	Dual function I/O ports that have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data, providing full duplex capability.
PORT 2	8-bit multi-functional port. All of its pins are shared with other functions.
PORT 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
EPORT	8-bit bidirectional standard and I/O port. These bits are shared with the extended address bus, A16–A19. Pin function is selected on a per pin basis.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND ..... −0.5 to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation..... 0.5W

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	16	MHz (Note 4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Under Listed Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current			90	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While device in Reset)
I_{REF}	A/D Reference Supply Current			5	mA	
I_{IDLE}	Idle Mode Current			40	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current(6)		50	75	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$(11)
V_{IL}	Input Low Voltage (all pins)	−0.5V		0.3 V_{CC}	V	For PORT0(10)
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5	V	For PORT0(10)
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	XTAL1 Input Pin Only(1)
V_{IH2}	Input High Voltage on RESET	0.7 V_{CC}		V_{CC} + 0.5	V	RESET input pin only
V_{OL}	Output Low Voltage (Outputs Configured as Complementary)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA(3,5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Outputs Configured as Complementary)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200µA(3,5) I_{OH} = −3.2 mA I_{OH} = −7.0 mA
I_{LI}	Input Leakage Current (Std. Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
I_{LI1}	Input Leakage Current (Port 0)			±3	µA	$V_{CC} < V_{IN} < V_{REF}$
I_{IL}	Logical 0 Input Current			−70	µA	V_{IN} = 0.45V(1)

DC CHARACTERISTICS (Under Listed Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OL1}	Output Low Voltage in RESET			0.8	V	(Note 7)
V_{OH1}	SLPINT (P5.4) and HLDA (P2.6) Output High Voltage in RESET	2.0			V	I_{OH} = 0.8 mA(7)
V_{OH2}	Output High Voltage in RESET	$V_{CC}-1V$			V	I_{OH} = −6 µA(1)
C_S	Pin Capacitance (Any pin to V_{SS})			10	pF	f_{test} = 1.0 MHz
R_{WPU}	Weak Pullup Resistance		150K		Ω	(Note 6)

NOTES:
1. All BD (bidirectional) pins except INST and CLKOUT. INST and CLKOUT are excluded due to their not being weakly pulled high in reset. BD pins include Port1, Port2, Port3, Port4, Port5, Port6 and EPORT except SPLINT (P5.4) and HLDA (P2.6).
2. Standard input pins include XTAL1, $\overline{EA}$, RESET, and Port 1/2/5/6 and EPORT when setup as inputs.
3. All bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{OL}/I_{OH} currents per pin will be characterized and published at a later date.
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.0V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. TBD = To Be Determined.
9. Pullup present during return from powerdown condition.
10. When P0 is used as analog inputs, refer to A/D specifications for this characteristic.
11. For temperatures <100°C typical is 10 µA.

8XC196NT/NQ ADDITIONAL BUS TIMING MODES

The 8XC196NT and NQ devices have 3 additional bus timing modes for external memory interfacing.

MODE 3:

Mode 3 is the standard timing mode. Use this mode for systems that emulate the 8XC196KR bus timings.

MODE 0:

Mode 0 is the standard timing mode, but 1 (minimum) wait state is always inserted in external bus cycles.

MODE 1:

Mode 1 is the long R/W mode. This mode advances $\overline{RD}$ and $\overline{WR}$ signals by 1 T_{OSC} creating a 2 T_{OSC} $\overline{RD}/\overline{WR}$ low time. ALE is also advanced by 0.5 T_{OSC} but ALE high time remains 1 T_{OSC}.

MODE 2:

Mode 2 is the long R/W mode with Early Address. Mode 2 is similar to Mode 1 with respect to RD, WR, and ALE signals. Additionally, the address is output on the bus 0.5 T_{OSC} earlier in the bus cycle.

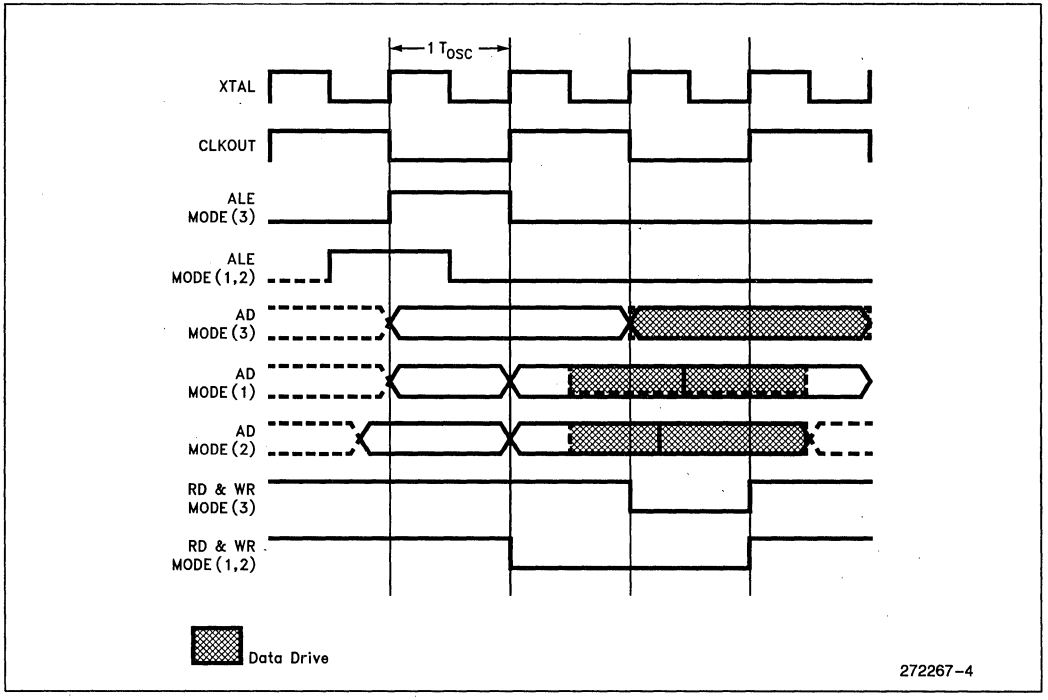


Figure 3. Detailed MODE 1, 2, 3, Comparison

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:
H—High
L—Low
V—Valid
X—No Longer Valid
Z—Floating

Signals:
A—Address
B—$\overline{BHE}$
BR—$\overline{BREQ}$
C—CLKOUT
D—DATA
G—Buswidth
H—$\overline{HOLD}$
HA—$\overline{HLDA}$
L—ALE/$\overline{ADV}$
Q—Data Out
RD—$\overline{RD}$
W—$\overline{WR}$/$\overline{WRH}$/$\overline{WRI}$
X—XTAL1
Y—READY

BUS MODE 0 and 3—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2T_{OSC} - 75$	ns(3)
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns(3)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2T_{OSC} - 75$	ns(2, 3)
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns(2, 3)
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns(2)
T_{RLDV}	RD active to input Data Valid		$T_{OSC} - 30$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of RD to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after RD High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2T_{OSC} \times n$, where n = number of wait states.
3. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add $2T_{OSC}$ to the specification.

BUS MODE 0 and 3—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

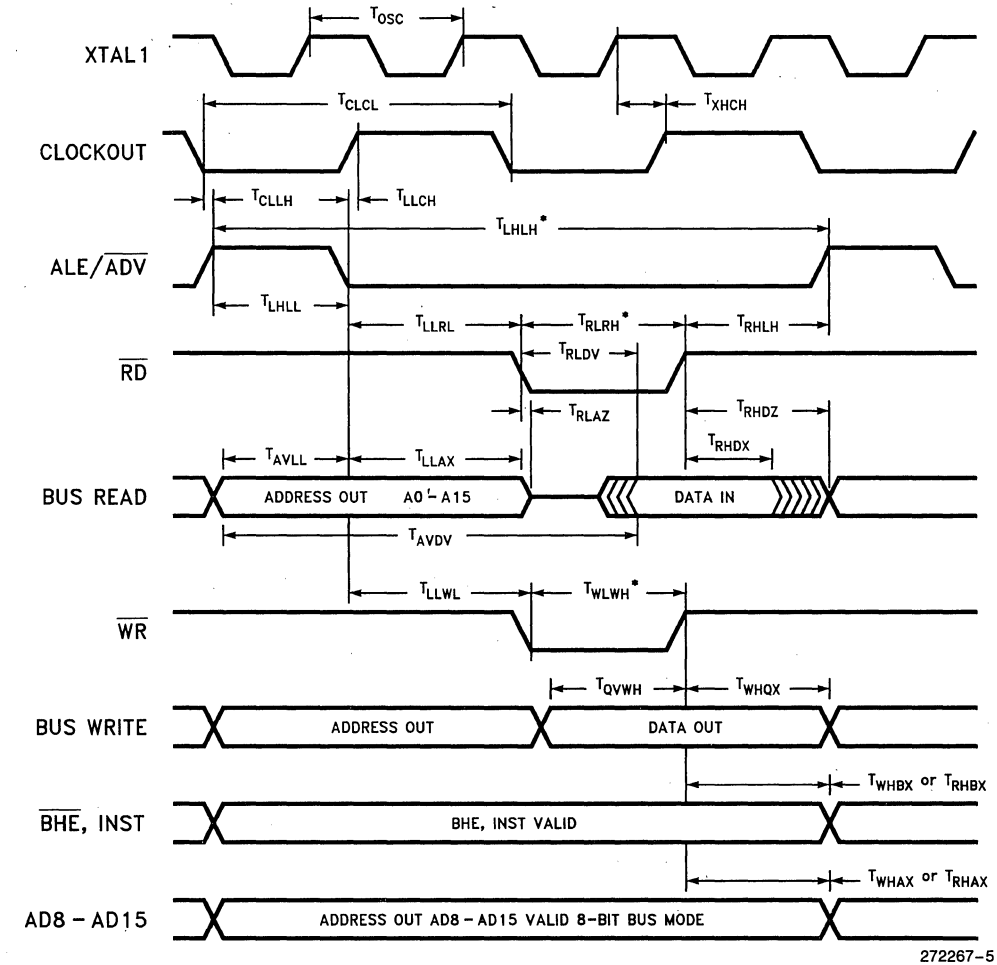
The 8XC196NT will meet these specifications

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	4.0	16.0	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20		ns
T_{OFD}	Clock Failure to Reset Pulled Low(6)	4	40	µs
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 30	ns
T_{CLLH}	CLKOUT Low to ALE/ADV High	−20	+15	ns
T_{LLCH}	ALE/ADV Low to CLKOUT High	−20	+15	ns
T_{LHLH}	ALE/ADV Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/ADV High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 25		ns
T_{LLAX}	Address Hold After ALE/ADV Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/ADV Low to RD Low	T_{OSC} − 30		ns
T_{RLCL}	RD Low to CLKOUT Low	+4	+40	ns
T_{RLRH}	RD Low Period	T_{OSC} − 5		ns(5)
T_{RHLH}	RD High to ALE/ADV High	T_{OSC}	T_{OSC} + 25	ns(3)
T_{RLAZ}	RD Low to Address Float		+5	ns
T_{LLWL}	ALE/ADV Low to WR Low	T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to WR Low	−20	+25	ns
T_{QVWH}	Data Valid before WR High	T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to WR High	−10	+15	ns
T_{WLWH}	WR Low Period	T_{OSC} − 30		ns(5)
T_{WHQX}	Data Hold after WR High	T_{OSC} − 25		ns
T_{WHLH}	WR High to ALE/ADV High	T_{OSC} − 10	T_{OSC} + 15	ns(3)
T_{WHBX}	BHE, INST Hold after WR High	T_{OSC} − 15		ns
T_{WHAX}	AD8–15 Hold after WR High	T_{OSC} − 30		ns(4)
T_{RHBX}	BHE, INST Hold after RD High	T_{OSC} − 10		ns
T_{RHAX}	AD8–15 Hold after RD High	T_{OSC} − 30		ns(4)

NOTES:

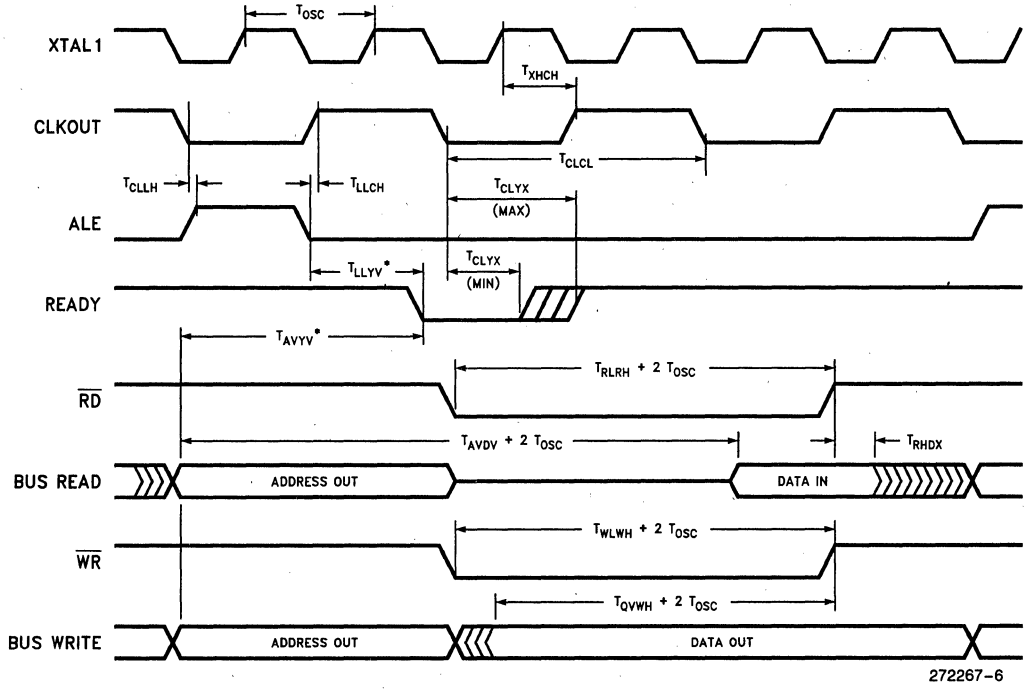
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.
6. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure. The OFD circuitry is enabled by programming the UPROM location 0778H with the value 0004H. NT/NQ customer QROM codes need to equate location 2016H to the value 0CDEH if the oscillator fail detect (OFD) function is desired. Intel manufacturing uses location 2016H as a flag to determine whether or not to program the Clock Detect Enable (CDE) bit. Programming the CDE bit enables oscillator fail detection.

BUS MODE 0 and 3—8XC196NT SYSTEM BUS TIMING



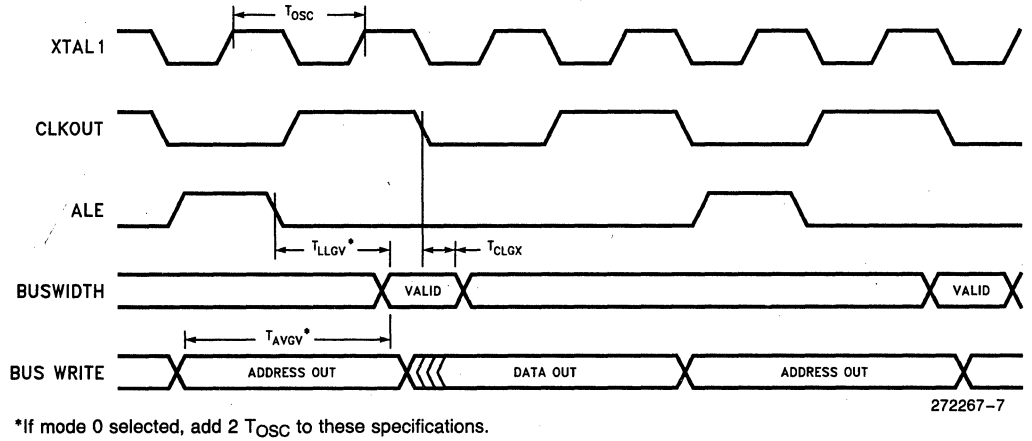
*If mode 0 operation is selected, add 2 T_{OSC} to this time.

8XC196NT MODE 0 and 3—READY TIMINGS (ONE WAIT STATE)



*If mode 0 selected, one wait state is always added. If additional wait states are required, add 2 T_{OSC} to these specifications.

MODE 0 and 3—8XC196NT BUSWIDTH TIMINGS



*If mode 0 selected, add 2 T_{OSC} to these specifications.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2\ T_{OSC} - 75$	ns
T_{LLYV}	ALE Low to READY Setup		$1.5\ T_{OSC} - 70$	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\ T_{OSC} - 75$	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		$1.5\ T_{OSC} - 60$	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3\ T_{OSC} - 60$	ns(2)
T_{RLDV}	RD active to input Data Valid		$2\ T_{OSC} - 44$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of RD to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after RD High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2\ T_{OSC} \times n$, where n = number of wait states.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

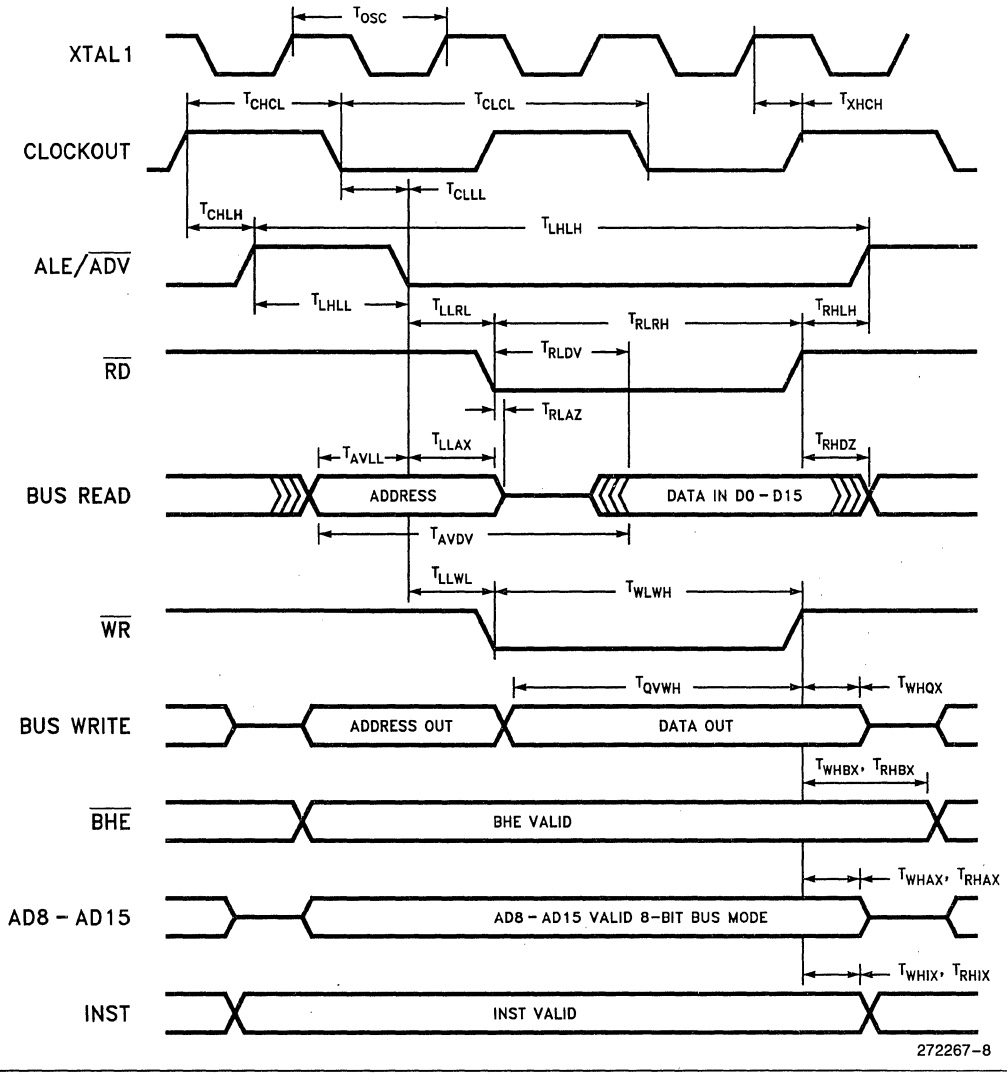
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196NT will meet these specifications

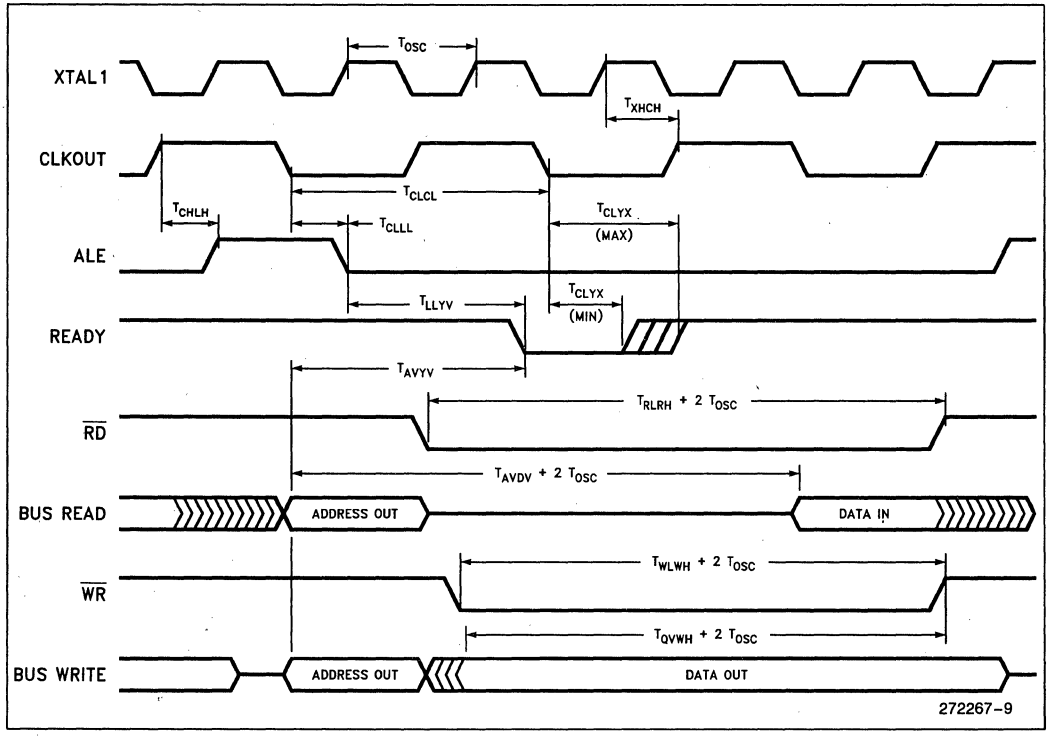
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	16.0	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/ADV High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 15	ns
T_{CLLL}	CLKOUT LOW to ALE/ADV Low	0.5 T_{OSC} − 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/ADV Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/ADV High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	0.5 T_{OSC} − 20		ns
T_{LLAX}	Address Hold After ALE/ADV Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/ADV Low to RD Low	0.5 T_{OSC} − 10		ns
T_{RLCL}	RD Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} + 30	ns
T_{RLRH}	RD Low Period	2 T_{OSC} − 20		ns(5)
T_{RHLH}	RD High to ALE/ADV High	0.5 T_{OSC}	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	RD Low to Address Float		+5	ns
T_{LLWL}	ALE/ADV Low to WR Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to WR Low	T_{OSC} − 25	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before WR High	2 T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to WR High	−10	+15	ns
T_{WLWH}	WR Low Period	2 T_{OSC} − 20		ns(5)
T_{WHQX}	Data Hold after WR High	0.5 T_{OSC} − 25		ns
T_{WHLH}	WR High to ALE/ADV High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 10	ns(3)
T_{WHBX}	BHE Hold after WR High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after WR High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after WR High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	BHE Hold after RD High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after RD High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after RD High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

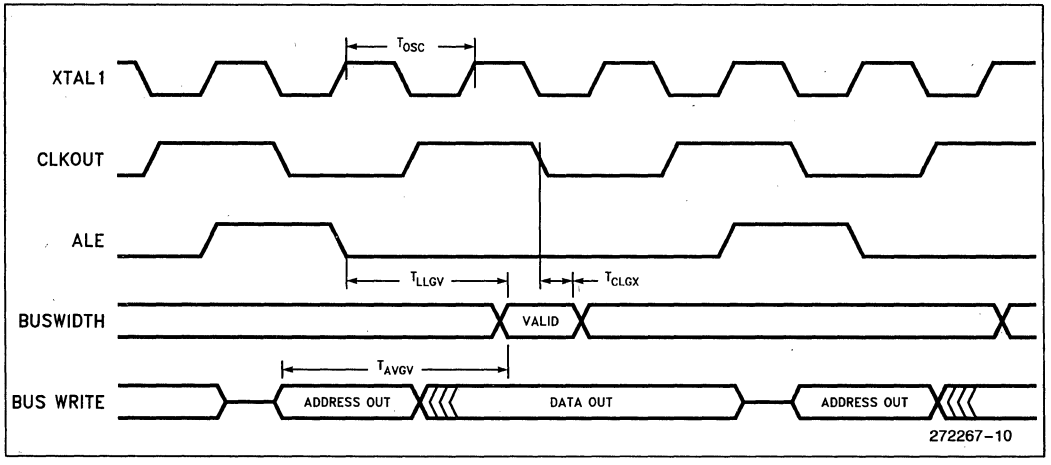
MODE 1—8XC196NT SYSTEM BUS TIMING



MODE 1—8XC196NT READY TIMINGS (ONE WAIT STATE)



MODE 1—8XC196NT BUSWIDTH TIMINGS



BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		2.5 T_{OSC} − 75	ns
T_{LLYV}	ALE Low to READY Setup		1.5 T_{OSC} − 70	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		2.5 T_{OSC} − 75	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		1.5 T_{OSC} − 60	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3.5 T_{OSC} − 55	ns(2)
T_{RLDV}	RD active to input Data Valid		2 T_{OSC} − 44	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 60	ns
T_{RHDZ}	End of RD to Input Data Float		0.5 T_{OSC}	ns
T_{RHDX}	Data Hold after RD High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

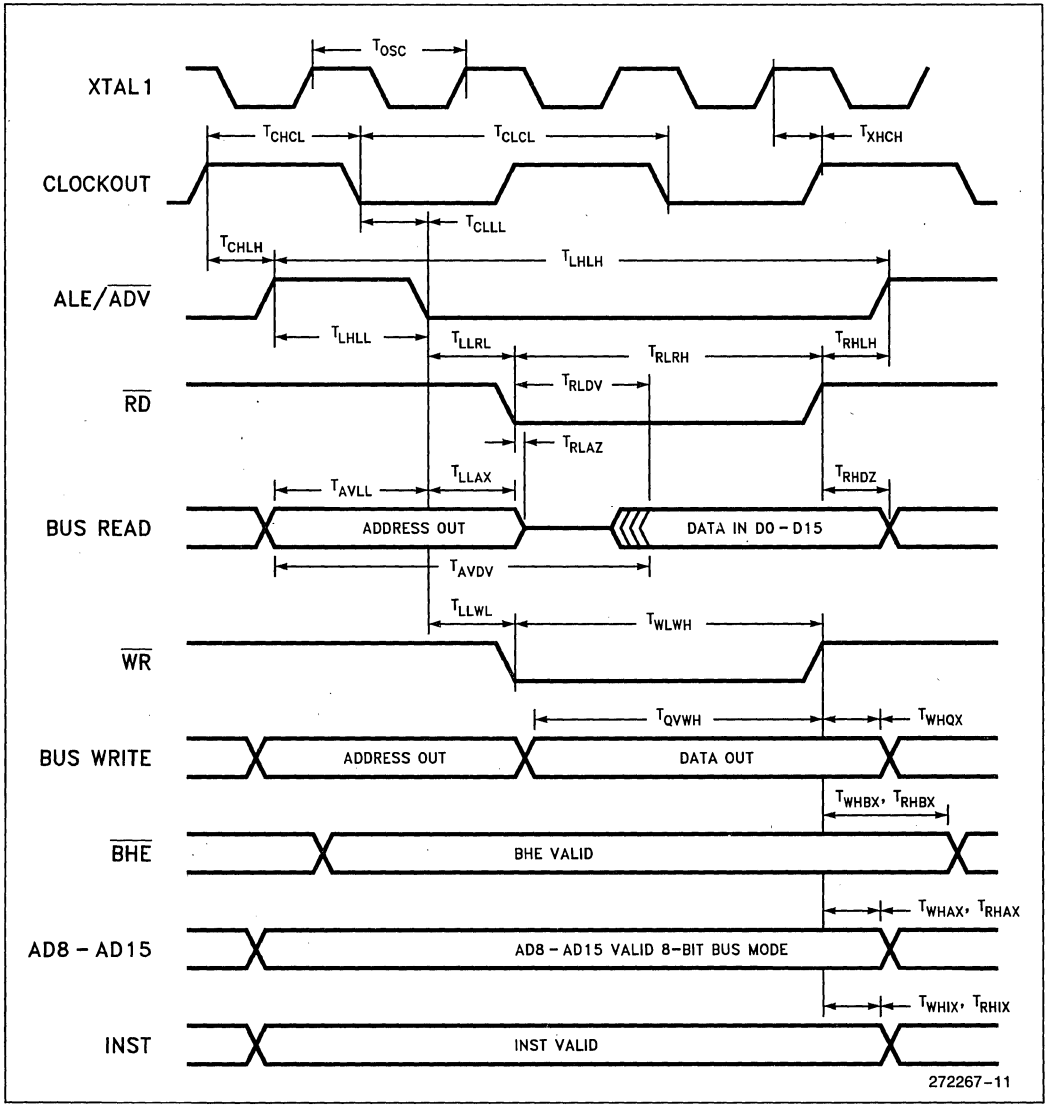
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196NT will meet these specifications

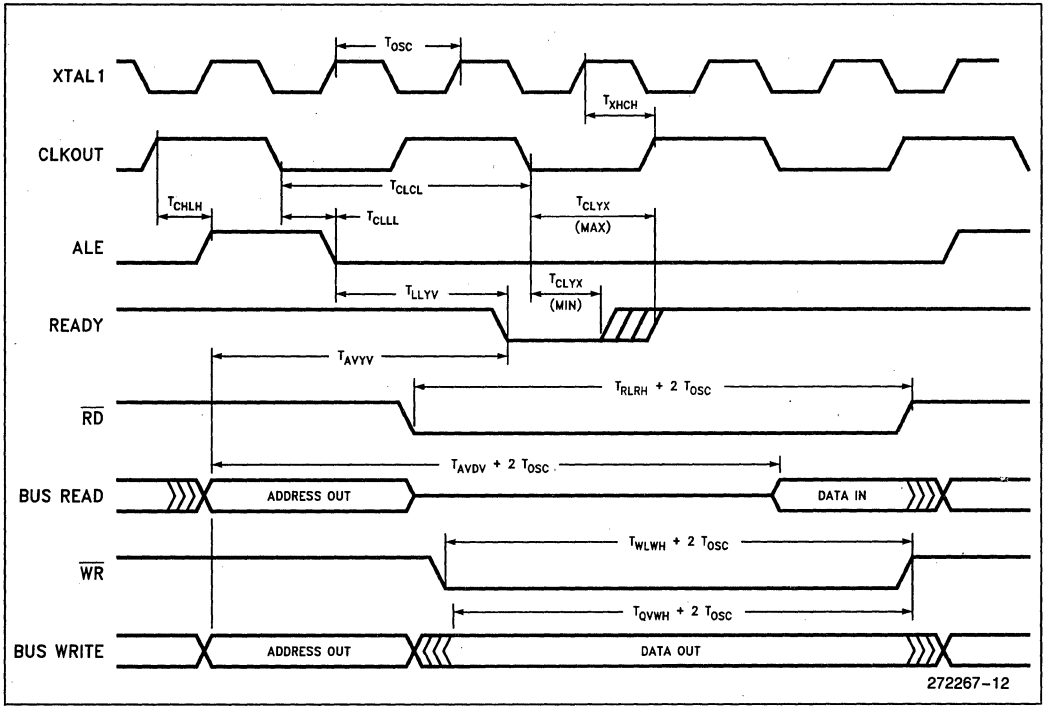
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	16.0	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+85	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/ADV High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 15	ns
T_{CLLL}	CLKOUT LOW to ALE/ADV Low	0.5 T_{OSC} − 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/ADV Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/ADV High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/ADV Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/ADV Low to RD Low	0.5 T_{OSC} − 10		ns
T_{RLCL}	RD Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} + 30	ns
T_{RLRH}	RD Low Period	2 T_{OSC} − 20		ns(5)
T_{RHLH}	RD High to ALE/ADV High	0.5 T_{OSC} − 5	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	RD Low to Address Float		+5	ns
T_{LLWL}	ALE/ADV Low to WR Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to WR Low	T_{OSC} − 22	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before WR High	2 T_{OSC} − 25		ns
T_{CHWH}	CLKOUT High to WR High	−10	+15	ns
T_{WLWH}	WR Low Period	2 T_{OSC} − 20		ns(5)
T_{WHQX}	Data Hold after WR High	0.5 T_{OSC} − 25		ns
T_{WHLH}	WR High to ALE/ADV High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 10	ns(3)
T_{WHBX}	BHE Hold after WR High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after WR High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after WR High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	BHE Hold after RD High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after RD High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after RD High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

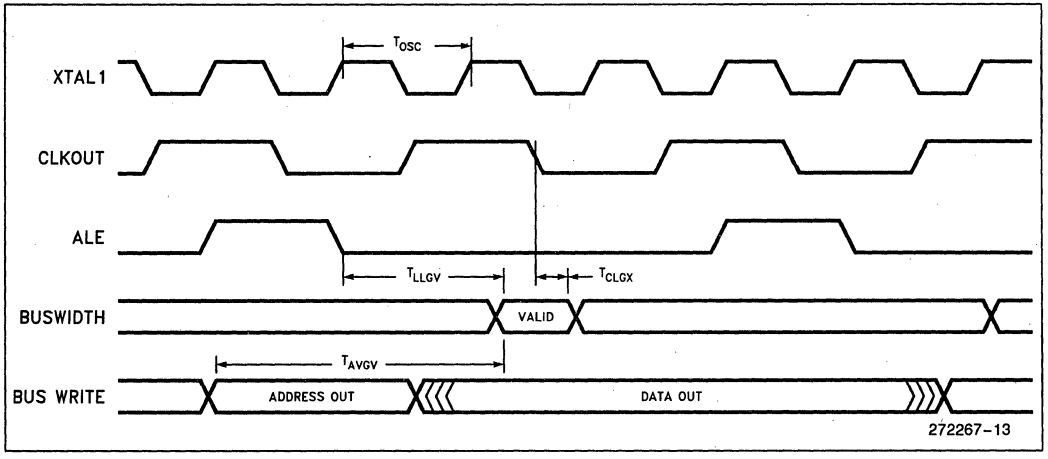
MODE 2—8XC196NT SYSTEM BUS TIMING



MODE 2—8XC196NT READY TIMINGS (ONE WAIT STATE)



MODE 2—8XC196NT BUSWIDTH TIMINGS



BUS MODE 0, 1, 2, and 3—HOLD/HOLDA TIMINGS (Over Specified Operation Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD Setup Time	+65		ns(1)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	+15	ns
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	+15	ns
T_{AZHAL}	HLDA Low to Address Float		+25	ns
T_{BZHAL}	HLDA Low to BHE, INST, RD, WR Weakly Driven		+25	ns
T_{CLHAH}	CLKOUT Low to HLDA High	−25	+15	ns
T_{CLBRH}	CLKOUT Low to BREQ High	−25	+25	ns
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	−10		ns

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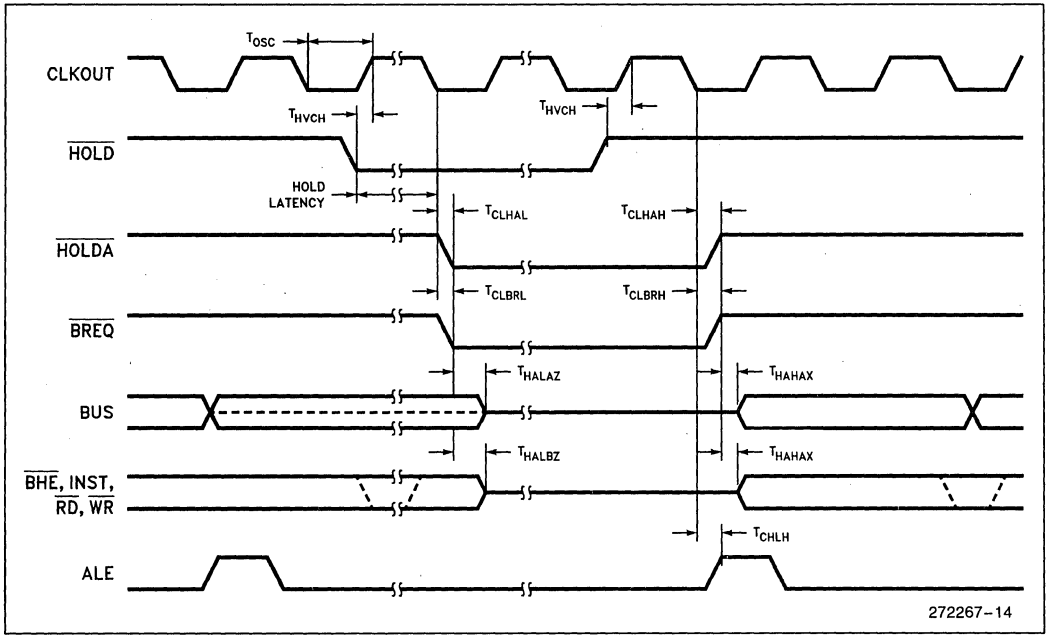
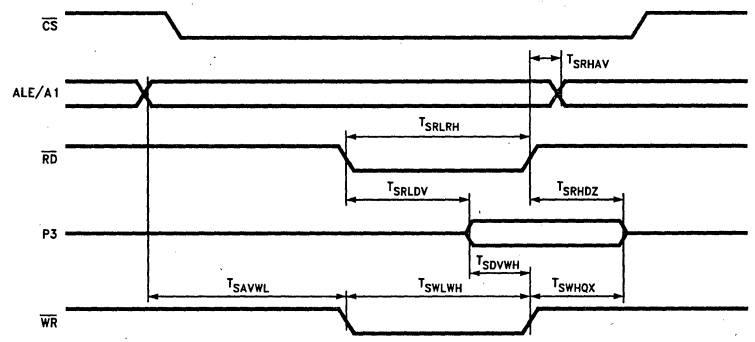
NOTE:
1. To guarantee recognition at next clock.

8XC196NT $\overline{HOLD}$/$\overline{HOLDA}$ TIMINGS



AC CHARACTERISTICS—SLAVE PORT

SLAVE PORT WAVEFORM—(SLPL = 0)



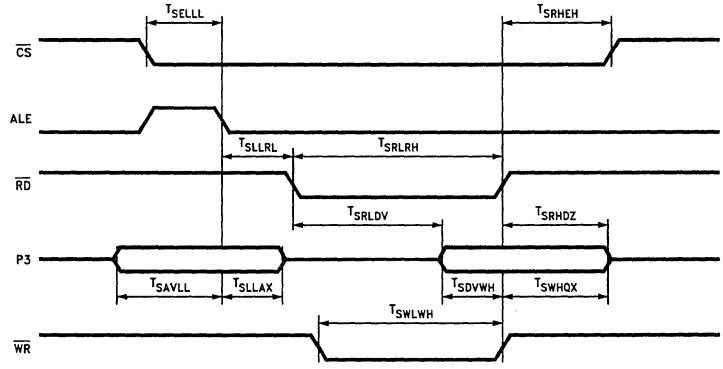
SLAVE PORT TIMING—(SLPL = 0, 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SAVWL}	Address Valid to $\overline{WR}$ Low	50		ns
T_{SRHAV}	$\overline{RD}$ High to Address Valid	60		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 16 MHz, T_{OSC} = 60 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

AC CHARACTERISTICS—SLAVE PORT (Continued)

SLAVE PORT WAVEFORM—(SLPL = 1)



SLAVE PORT TIMING—(SLPL = 1, 2, 3)

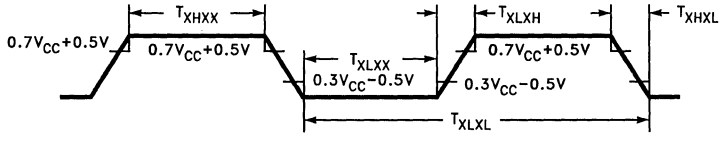
Symbol	Parameter	Min	Max	Units
T_{SELLL}	$\overline{CS}$ Low to ALE Low	20		ns
T_{SRHEH}	$\overline{RD}$ or $\overline{WR}$ High to $\overline{CS}$ High	60		ns
T_{SLLRL}	ALE Low to $\overline{RD}$ Low	T_{OSC}		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SAVLL}	Address Valid to ALE Low	20		ns
T_{SLLAX}	ALE Low to Address Invalid	20		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 16 MHz, T_{OSC} = 60 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

EXTERNAL CLOCK DRIVE

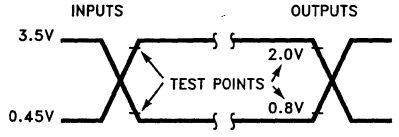
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	250	ns
T_{XHXX}	High Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



272267-17

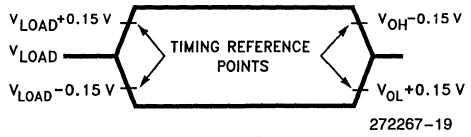
AC TESTING INPUT, OUTPUT WAVEFORMS



272267-18

AC Testing inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS

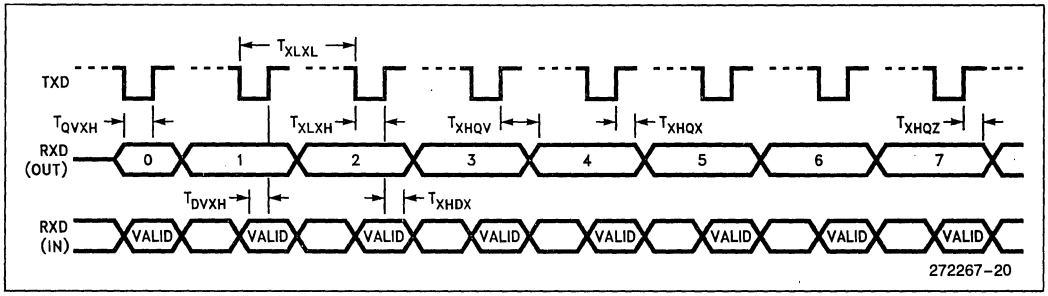


272267-19

For timing purposes a Port Pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq 15$ mA.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



AC CHARACTERISTICS—SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFTING REGISTER MODE

Test Conditions: T_A = −40°C to +125°C; V_{CC} = 5.0V ±10%; V_{SS} = 0.0V; Load Capacitance = pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}(1)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(1)	Last Clock Rising to Output Float		5 T_{OSC}	ns

NOTE:
1. Parameters not tested.

A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	10	15	μs(2)
F_{OSC}	Oscillator Frequency	4.0	16.0	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3.0	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3.0	LSBs
Differential Non-Linearity		−0.75	+0.75	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	μA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An "LSB" as used here has a value of approximately 20 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	7	20	μs(2)
F_{OSC}	Oscillator Frequency	4.0	16.0	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

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8-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1.0	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1.0	LSBs
Differential Non-Linearity		−0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	μA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An "LSB" as used here has a value of approximately 20 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	°C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	16.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC EPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(2)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run-time programming is done with F_{OSC} = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5V ±0.5V, T_C = 25°C ±5°C and V_{PP} = 12.5V ±0.25V. For run-time programming over a full operating range, contact factory.
3. This specification is for the word dump mode. For programming pulses use Modified Quick Pulse Algorithm.

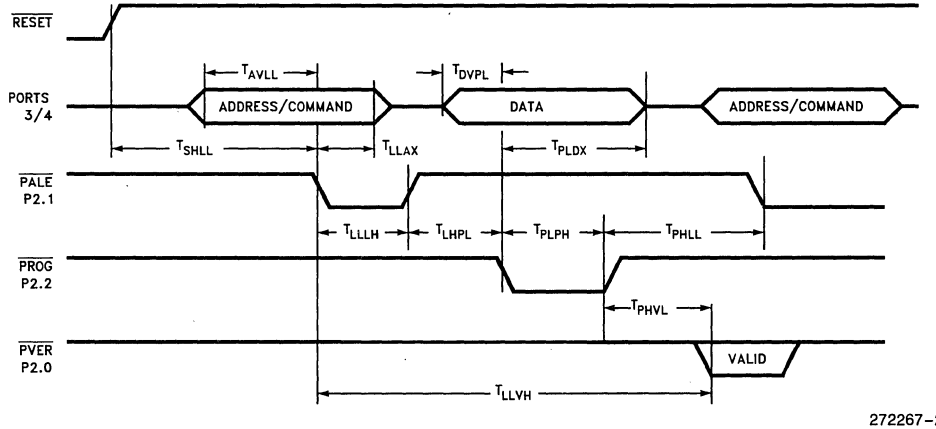
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		200	mA

NOTE:
Do not apply V_{PP} unti V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

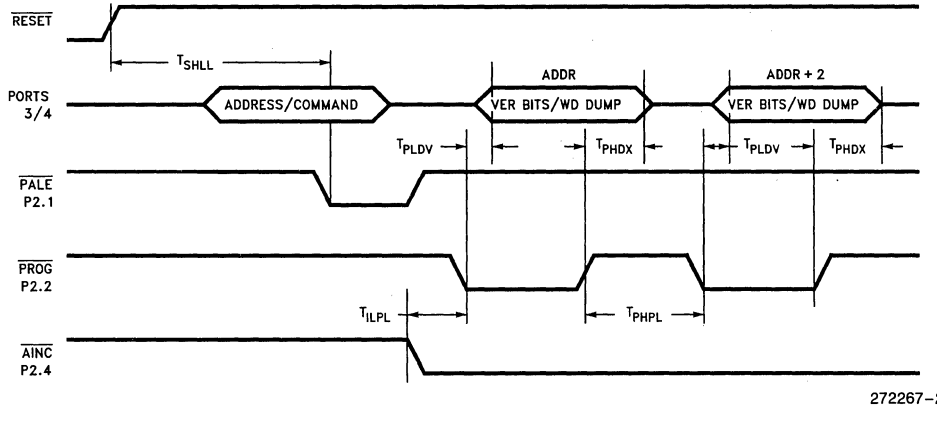
EPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



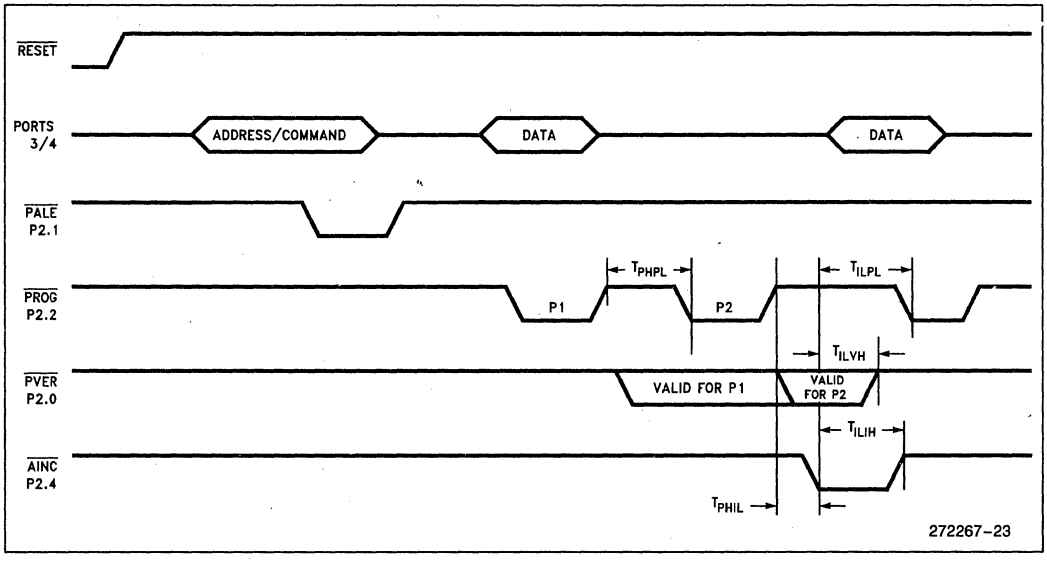
NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP MODE WITH AUTO INCREMENT



NOTE:
P3.0 must be low("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



8XC196NT/NQ ERRATA

The following is a list of all known functional deviations for 8XC196NT/NQ devices. C-step devices can be identified by a special mark following the eight digit FPO number on the top of the package. For C-step devices, this mark is a "C".

1. Base-indexed ELD, ELDB, EST, ESTB instructions: The ELD, ELDB, EST, ESTB instructions using the base-indexed addressing mode do not function when executed from external memory. For example:

```
ELD 20h, #0b1000h[RO]          ;does not work
```

workaround:

```
LD   30h, #1000h    ;30-32h forms pointer
LD   32h, #000bh    ;to extended memory
ELD  20h, [30h]     ;this mode works
                     correctly
```

2. 24-bit mode auto-increment across 64K boundaries. When in 24-bit mode (MODE16 = 0), the auto increment addressing mode does not increment correctly across 64K boundaries.

8XC196KT
COMMERCIAL CHMOS MICROCONTROLLER

- High Performance CHMOS 16-Bit CPU
- Up to 32 Kbytes of On-Chip EPROM
- Up to 1 Kbyte of On-Chip Register RAM
- Up to 512 Bytes of Additional RAM (Internal RAM)
- Register-Register Architecture
- 8 Channel/10-Bit A/D with Sample/Hold
- 37 Prioritized Interrupt Sources
- Up to Seven 8-Bit (56) I/O Ports
- Full Duplex Serial I/O Port
- Dedicated Baud Rate Generator
- Interprocessor Communication Slave Port
- Selectable Bus Timing Modes for Flexible Interfacing
- Oscillator Fail Detection Circuitry
- High Speed Peripheral Transaction Server (PTS)
- Two Dedicated 16-Bit High-Speed Compare Registers
- 10 High Speed Capture/Compare (EPA)
- Full Duplex Synchronous Serial I/O Port (SSIO)
- Two Flexible 16-Bit Timer/Counters
- Quadrature Counting Inputs
- Flexible 8-/16-Bit External Bus (Programmable)
- Programmable Bus (HOLD/HLDA)
- 1.75 μs 16 x 16 Multiply
- 3 μs 32/16 Divide
- 68-Pin PLCC Package

Device	Pins/Package	EPROM	Reg RAM	Code RAM	Address Space	I/O	EPA	A/D
8XC196KT	68-Pin PLCC	32K	1K	512	64 Kbyte	56	10	8

X = 7 EPROM Device

The 8XC196KT 16-bit microcontroller is a high performance member of the MCS®-96 microcontroller family. The 8XC196KT is an enhanced 8XC196KR device with 1000 byte register RAM, 512 bytes internal RAM, 16 MHz operation and an optional 32 Kbytes of ROM/EPROM. Intel's CHMOS III-E process provides a high performance processor along with low power consumption.

The 8XC196KT has a maximum guaranteed frequency of 16 MHz.

Ten high-speed capture/compare modules are provided. As capture modules event times with 250 ns resolution can be recorded and generate interrupts. As compare modules events such as toggling of a port pin, starting an A/D conversion, pulse width modulation, and software timers can be generated. Events can be based on the timer or up/down counter.

October 1992
Order Number: 272266-001

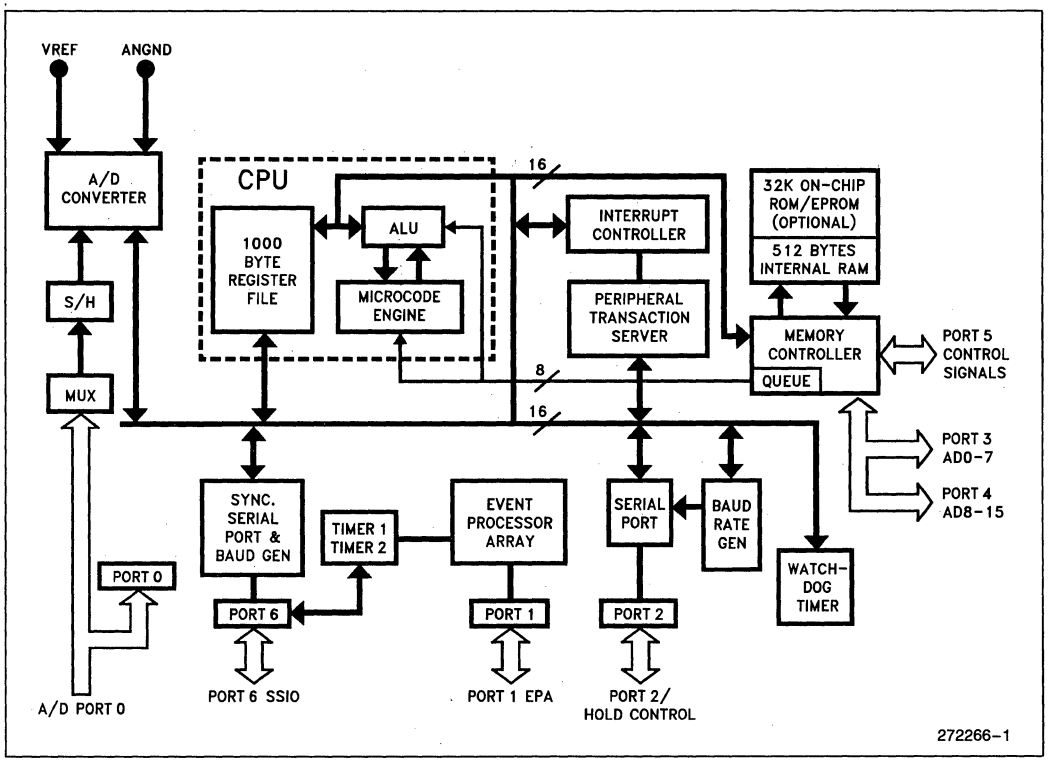
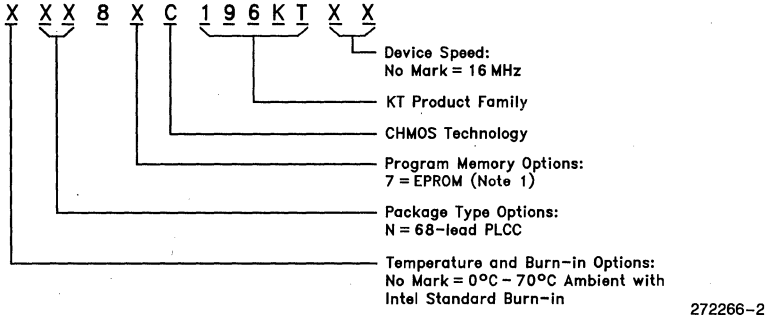


Figure 1. 8XC196KT Block Diagram



EXAMPLE: N87C196KT is 68-Lead PLCC OTPROM.
For complete package dimensional data, refer to the Intel Packaging Handbok (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 2. The 8XC196KT Family Nomenclature

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.

Table 1. Thermal Characteristics

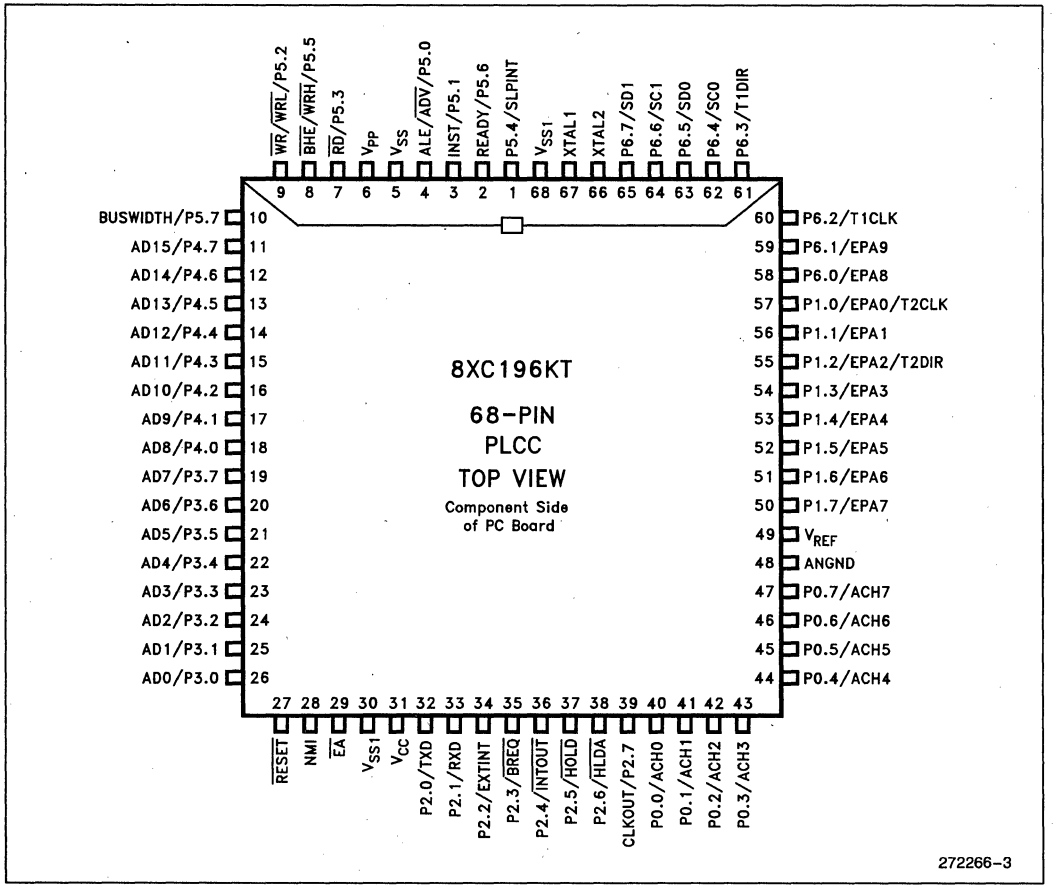
Package Type	θ_{ja}	θ_{jc}
PLCC	36.5°C/W	13°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

8XC196KT Memory Map

FFFFH A000H	24 Kbytes External Memory	
9FFFH 2080H	Internal EPROM or External Memory	
207FH 2000H	Reserved Memory (Internal EPROM or External Memory)(4, 5)	
1FFFH 1FE0H	Memory Mapped Special Function Registers (SFR's)	
1FDFH 1F00H	Internal Special Function Registers (SFR's)(4)	
1EFFH 0600H	External Memory	
05FFH 0400H	Internal Code or Data RAM (Address with Indirect or Indexed Modes)	
03FFH 0100H	Register RAM	Upper Register File (Address with Indirect or Indexed Modes or through Windows)(1)
00FFH 0018H	Register RAM	Lower Register File (Address with Direct, Indirect, or Indexed Modes)(1, 3)
0017H 0000H	CPU SFR's	

NOTES:
1. Code executed in locations 0000H to 03FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must be written with 0.
4. Refer to 8XC196KT for SFR descriptions.
5. **WARNING:** The contents or functions of reserved memory locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.


8XC196KT
68-PIN
PLCC
TOP VIEW
Component Side
of PC Board
9 WR/WRL/P5.2
8 BHE/WRH/P5.5
7 RD/P5.3
6 VPP
5 VSS
4 ALE/ADV/P5.0
3 INST/P5.1
2 READY/P5.6
1 P5.4/SLPINT
68 VSS1
67 XTAL1
66 XTAL2
65 P6.7/SD1
64 P6.6/SC1
63 P6.5/SD0
62 P6.4/SCO
61 P6.3/T1DIR
10 BUSWIDTH/P5.7
11 AD15/P4.7
12 AD14/P4.6
13 AD13/P4.5
14 AD12/P4.4
15 AD11/P4.3
16 AD10/P4.2
17 AD9/P4.1
18 AD8/P4.0
19 AD7/P3.7
20 AD6/P3.6
21 AD5/P3.5
22 AD4/P3.4
23 AD3/P3.3
24 AD2/P3.2
25 AD1/P3.1
26 AD0/P3.0
60 P6.2/T1CLK
59 P6.1/EPA9
58 P6.0/EPA8
57 P1.0/EPA0/T2CLK
56 P1.1/EPA1
55 P1.2/EPA2/T2DIR
54 P1.3/EPA3
53 P1.4/EPA4
52 P1.5/EPA5
51 P1.6/EPA6
50 P1.7/EPA7
49 VREF
48 ANGND
47 P0.7/ACH7
46 P0.6/ACH6
45 P0.5/ACH5
44 P0.4/ACH4
27 RESET
28 NMI
29 EA
30 VSS1
31 VCC
32 P2.0/TXD
33 P2.1/RXD
34 P2.2/EXTINT
35 P2.3/BREQ
36 P2.4/INTOUT
37 P2.5/HOLD
38 P2.6/HLDA
39 CLKOUT/P2.7
40 P0.0/ACH0
41 P0.1/ACH1
42 P0.2/ACH2
43 P0.3/ACH3
272266-3

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}, V_{SSI}, V_{SSI}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
P.27/CLKOUT	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Also LSIO pin.
$\overline{RESET}$	Reset input to and open-drain output from the chip.
P5.7/BUSWIDTH	Input for bus width selection. If CCR bit 1 is a one and CCR1 bit 2 is a one, this pin dyamically controls the Buswidth of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs, if BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is "0" and CCR1 bit 2 is "1", all bus cycles are 8-bit, if CCR bit 1 is "1" and CCR1 bit 2 is "0", all bus cycles are 16-bit. CCR bit 1 = "0" and CCR1 bit 2 = "0" is illegal. Also an LSIO pin when not used as BUSWIDTH.
NMI	A positive transition causes a non maskable interrupt vector through memory location 203EH.
P5.1/INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches, during internal EPROM fetches INST is held low. Also LSIO when not INST.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal to a high causes memory accesses to locations 2000H through 9FFFH to be directed to on-chip EPROM/ROM. $\overline{EA}$ equal to a low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{EA}$ is latched at reset.
$\overline{HOLD}$	Bus Hold input requesting control of the bus.
$\overline{HLDA}$	Bus hold acknowledge output indicating release of the bus.
$\overline{BREQ}$	Bus request output activated when the bus controller has a pending external memory cycle.
P5.0/ALE/$\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. $\overline{ADV}$ can be used as a chip select for external memory. ALE/$\overline{ADV}$ is active only during external memory accesses. Also LSIO when not used as ALE.
P5.3/$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is active only during external memory reads or LSIO when not used as $\overline{RD}$.
P5.2/$\overline{WR}$/$\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR, $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is active during external memory writes. Also an LSIO pin when not used as $\overline{WR}$/$\overline{WRL}$.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
P5.5/$\overline{BHE}$/$\overline{WRH}$	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects that bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{BHE}$ = 1), to the high byte only (A0 = 1, $\overline{BHE}$ = 0) or both bytes (A0 = 0, $\overline{BHE}$ = 0). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory write cycles. Also an LSIO pin when not BHE/$\overline{WRH}$.
P5.6/READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The max number of wait states inserted into the bus cycle is controlled by the CCR/ CCR1. Also an LSIO pin when READY is not selected.
P5.4/SLPINT	Dual function I/O pin. As a bidirectional port pin or as a system function. The system function is a Slave Port Interrupt Output Pin.
P6.2/T1CLK	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Clock input. The TIMER1 will increment or decrement on both positive and negative edges of this pin.
P6.3/T1DIR	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Direction input. The TIMER1 will increment when this pin is high and decrements when this pin is low.
PORT1/EPA0–7 P6.0–6.1/EPA8–9	Dual function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare. EPA0 and EPA2 have yet another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH0–7	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts to select the Programming Mode.
P6.3–6.7/SSIO	Dual function I/O ports that have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data, providing full duplex capability.
PORT 2	8-bit multi-functional port. All of its pins are shared with other functions.
PORT 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND ..... −0.5 to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation 0.5W

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	16	MHz (Note 4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Under Listed Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current			90	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Reference Supply Current			5	mA	(While device in Reset)
I_{IDLE}	Idle Mode Current			40	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current		50	75	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$(6, 11)
V_{IL}	Input Low Voltage (all pins)	−0.5V		0.3 V_{CC}	V	For PORT0(10)
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5	V	For PORT0(10)
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	XTAL1 Input Pin Only(1)
V_{IH2}	Input High Voltage on RESET	0.7 V_{CC}		V_{CC} + 0.5	V	RESET input pin only
V_{OL}	Output Low Voltage (Outputs Configured as Complementary)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA(3,5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Outputs Configured as Complementary)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200µA(3,5) I_{OH} = −3.2 mA I_{OH} = −7.0 mA
I_{LI}	Input Leakage Current (Std. Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
I_{LI1}	Input Leakage Current (Port 0)			±3	µA	$V_{SS} < V_{IN} < V_{REF}$
I_{IL}	Logical 0 Input Current			−70	µA	V_{IN} = 0.45V(1)

DC CHARACTERISTICS (Under Listed Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH1}	SLPINT (P5.4) and HLDA (P2.6) Output High Voltage in RESET	2.0			V	I_{OH} = 0.8 mA(7)
V_{OH2}	Output High Voltage in RESET	$V_{CC}-1V$			V	I_{OH} = −6 μA(1)
C_S	Pin Capacitance (Any pin to V_{SS})			10	pF	f_{test} = 1.0 MHz(6)
R_{WPU}	Weak Pullup Resistance		150K		Ω	(Note 6)

NOTES:
1. All BD (bidirectional) pins except INST and CLKOUT. INST and CLKOUT are excluded due to their not being weakly pulled high in reset. BD pins include Port1, Port2, Port3, Port4, Port5 and Port6 except SPLINT (P5.4) and HLDA (P2.6).
2. Standard input pins include XTAL1, $\overline{EA}$, RESET, and Port 1/2/5/6 when setup as inputs.
3. All bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{OL}/I_{OH} currents per pin will be characterized and published at a later date.
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.0V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. When P0 is used as analog inputs, refer to A/D specifications for this characteristic.
9. For temperatures <100°C typical is 10 μA.

8XC196KT ADDITIONAL BUS TIMING MODES

The 8XC196KT devices have 3 additional bus timing modes for external memory interfacing.

MODE 3:

Mode 3 is the standard timing mode.

MODE 0:

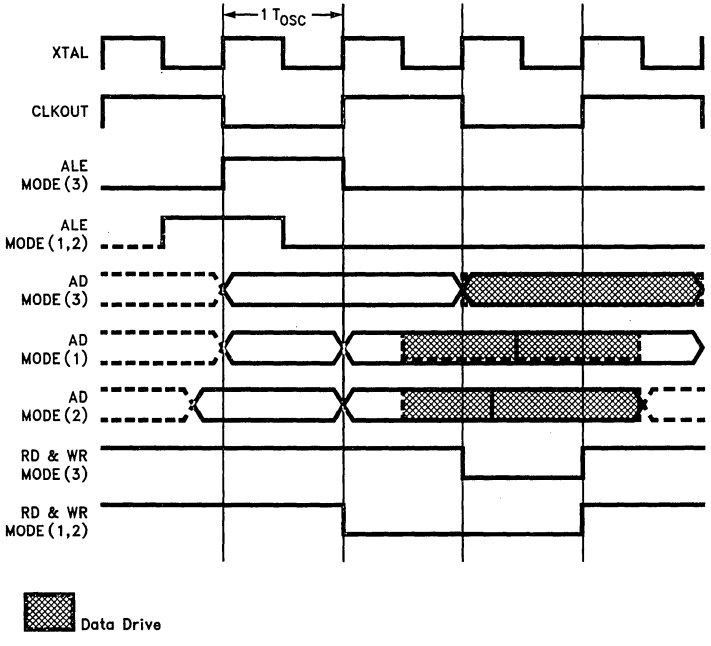
Mode 0 is the standard timing mode, but 1 (minimum) wait state is always inserted in external bus cycles.

MODE 1:

Mode 1 is the long R/W mode. This mode advances $\overline{RD}$ and $\overline{WR}$ signals by 1 T_{OSC} creating a 2 T_{OSC} $\overline{RD}/\overline{WR}$ low time. ALE is also advanced by 0.5 T_{OSC} but ALE high time remains 1 T_{OSC}.

MODE 2:

Mode 2 is the long R/W mode with Early Address. Mode 2 is similar to Mode 1 with respect to RD, WR, and ALE signals. Additionally, the address is output on the bus 0.5 T_{OSC} earlier in the bus cycle.



Detailed MODE 1, 2, 3, Comparison

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:
H—High
L—Low
V—Valid
X—No Longer Valid
Z—Floating

Signals:
A—Address
B—$\overline{BHE}$
BR—$\overline{BREQ}$
C—CLKOUT
D—DATA
G—Buswidth
H—$\overline{HOLD}$
HA—$\overline{HLDA}$
L—ALE/$\overline{ADV}$
Q—Data Out
RD—$\overline{RD}$
W—$\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X—XTAL1
Y—READY

BUS MODE 0 AND 3 AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196KT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2\ T_{OSC} - 75$	ns(3)
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns(3)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\ T_{OSC} - 75$	ns(2, 3)
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns(2, 3)
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3\ T_{OSC} - 55$	ns(2)
T_{RLDV}	RD active to input Data Valid		$T_{OSC} - 30$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of RD to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after RD High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 Tosc × n, where n = number of wait states.
3. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add 2 Tosc to the specification.

BUS MODE 0 AND 3 AC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

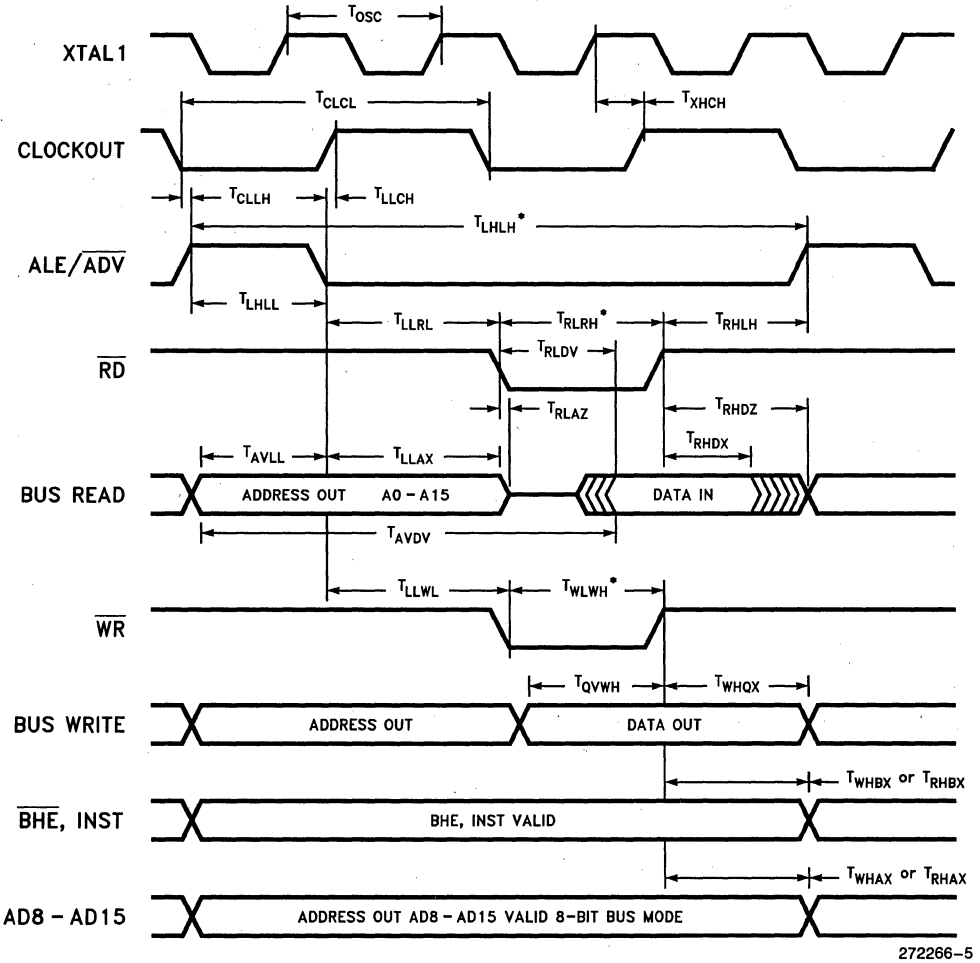
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196KT will meet these specifications

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	4.0	16.0	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20		ns
T_{OFD}	Clock Failure to Reset Pulled Low(6)	4	40	μs
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 30	ns
T_{CLLH}	CLKOUT Low to ALE/ADV High	−20	+15	ns
T_{LLCH}	ALE/ADV Low to CLKOUT High	−20	+15	ns
T_{LHLH}	ALE/ADV Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/ADV High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 25		ns
T_{LLAX}	Address Hold After ALE/ADV Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/ADV Low to RD Low	T_{OSC} − 30		ns
T_{RLCL}	RD Low to CLKOUT Low	+4	+40	ns
T_{RLRH}	RD Low Period	T_{OSC} − 5		ns(5)
T_{RHLH}	RD High to ALE/ADV High	T_{OSC}	T_{OSC} + 25	ns(3)
T_{RLAZ}	RD Low to Address Float		+5	ns
T_{LLWL}	ALE/ADV Low to WR Low	T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to WR Low	−20	+25	ns
T_{QVWH}	Data Valid before WR High	T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to WR High	−10	+15	ns
T_{WLWH}	WR Low Period	T_{OSC} − 30		ns(5)
T_{WHQX}	Data Hold after WR High	T_{OSC} − 25		ns
T_{WHLH}	WR High to ALE/ADV High	T_{OSC} − 10	T_{OSC} + 15	ns(3)
T_{WHBX}	BHE, INST Hold after WR High	T_{OSC} − 15		ns
T_{WHAX}	AD8–15 Hold after WR High	T_{OSC} − 30		ns(4)
T_{RHBX}	BHE, INST Hold after RD High	T_{OSC} − 10		ns
T_{RHAX}	AD8–15 Hold after RD High	T_{OSC} − 30		ns(4)

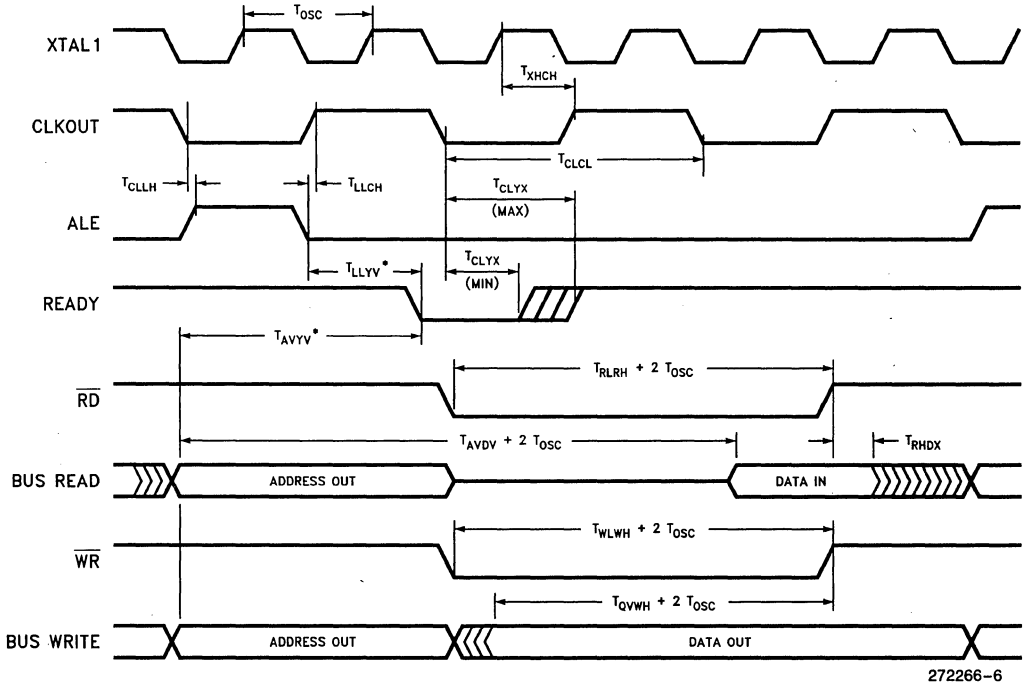
NOTES:
1. Testing performed at 4.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 Tosc × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.
6. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure. The OFD circuitry is enabled by programming the UPROM location 0778H with the value 0004H. KT customer QROM codes need to equate location 2016H to the value 0CDEH if the oscillator fail detect (OFD) function is desired. Intel manufacturing uses location 2016H as a flag to determine whether or not to program the Clock Detect Enable (CDE) bit. Programming the CDE bit enables oscillator fail detection.

BUS MODE 0 AND 3 8XC196KT SYSTEM BUS TIMING



* If mode 0 operation is selected, add 2 T_{OSC} to this time.

MODE 0 AND 3 8XC196KT READY TIMINGS (ONE WAIT STATE)



*If mode 0 selected, one wait state is always added. If additional wait states are required, add 2 Tosc to these specifications.

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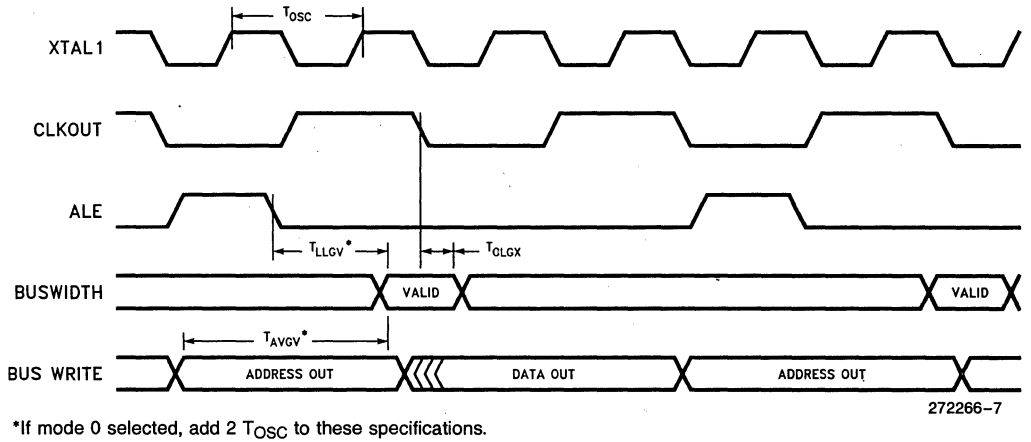
8XC196KT BUSWIDTH TIMINGS



*If mode 0 selected, add 2 T_{OSC} to these specifications.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196KT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2\ T_{OSC} - 75$	ns
T_{LLYV}	ALE Low to READY Setup		$1.5\ T_{OSC} - 70$	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\ T_{OSC} - 75$	nd
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{1.5\ OSC} - 60$	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3\ T_{OSC} - 60$	ns(2)
T_{RLDV}	RD Active to input Data Valid		$T_{OSC} - 44$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of RD to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after RD High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 Tosc × n, where n = number of wait states. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add 2 Tosc to the specification.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

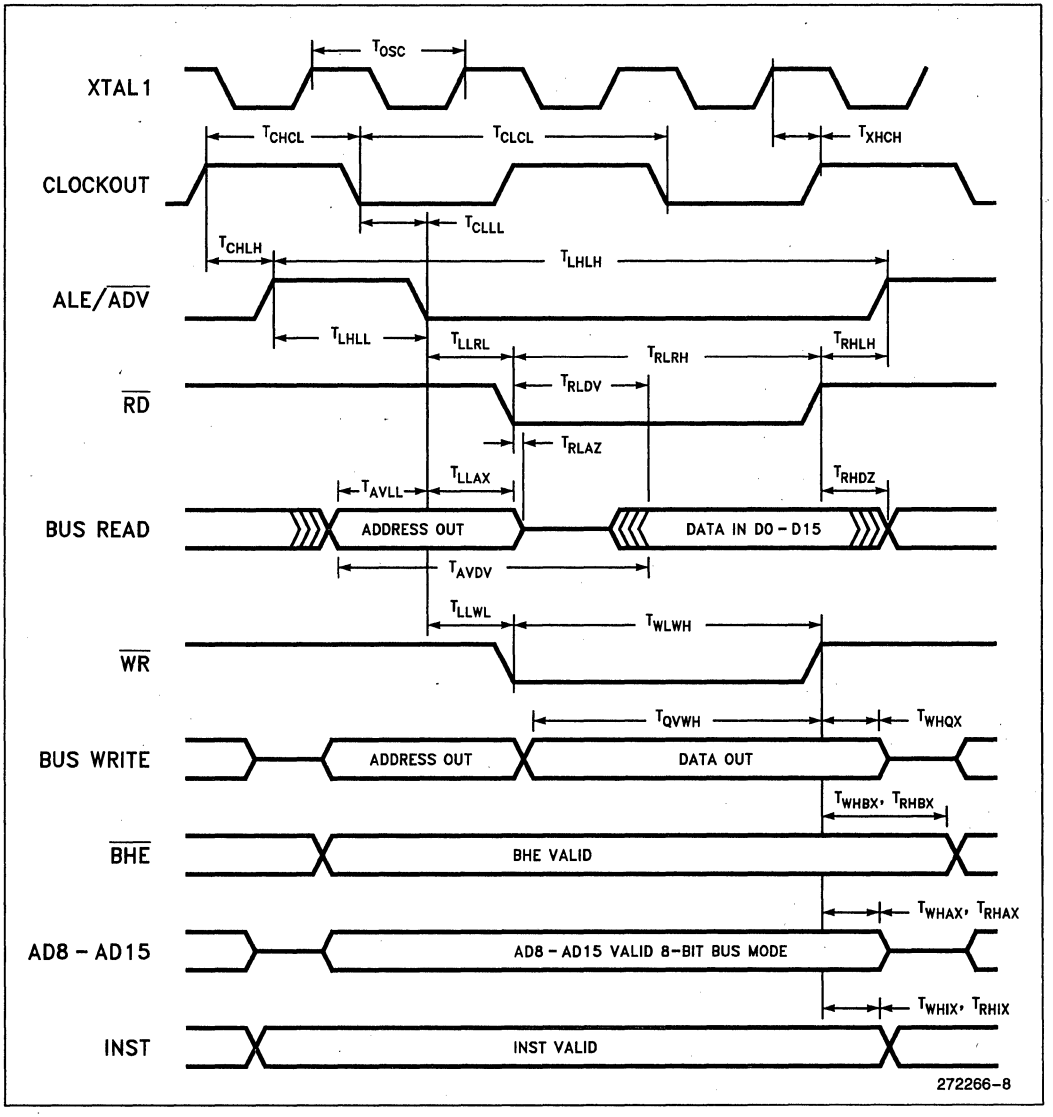
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196KT will meet these specifications

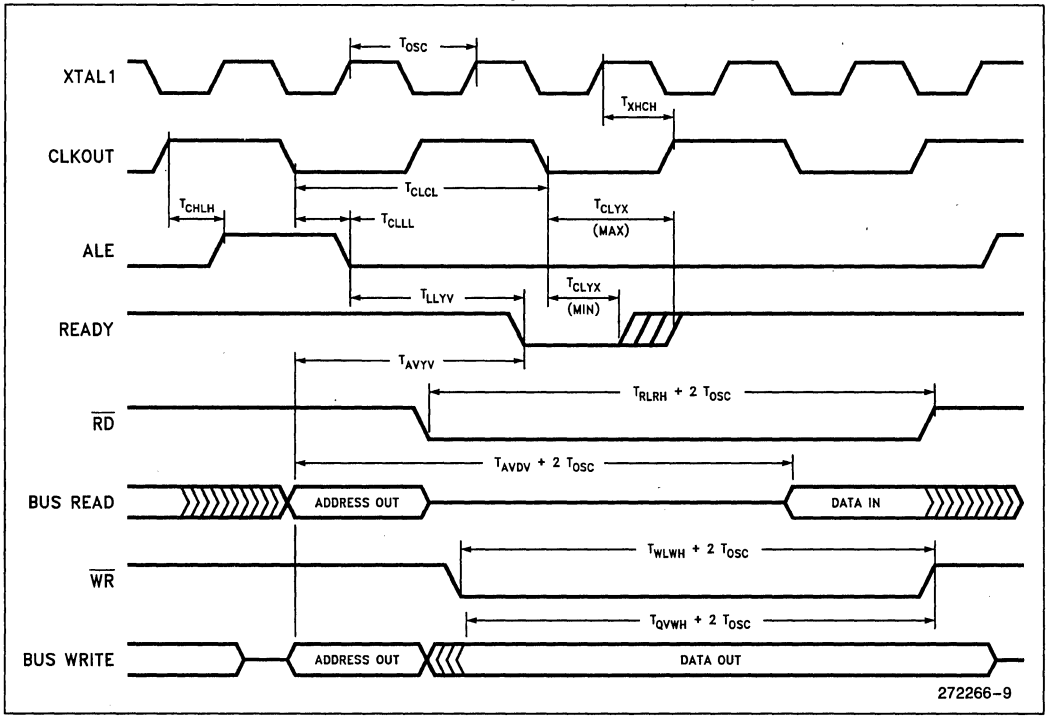
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	4.0	16.0	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20		ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CLLL}	CLKOUT Low to ALE/ADV Low	0.5 T_{OSC} − 25	0.5 T_{OSC}+15	ns
T_{LHLH}	ALE/ADV Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/ADV High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 20		ns
T_{LLAX}	Address Hold After ALE/ADV Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/ADV Low to RD Low	0.5 T_{OSC} − 10		ns
T_{RLCL}	RD Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} +30	ns
T_{RLRH}	RD Low Period	2T_{OSC} − 20		ns(5)
T_{RHLH}	RD High to ALE/ADV High	0.5 T_{OSC}	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	RD Low to Address Float		+5	ns
T_{LLWL}	ALE/ADV Low to WR Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to WR Low	T_{OSC} − 25	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before WR High	2 T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to WR High	−10	+15	ns
T_{WLWH}	WR Low Period	2 T_{OSC} − 20		ns(5)
T_{WHQX}	Data Hold after WR High	0.5 T_{OSC} − 25		ns
T_{WHLH}	WR High to ALE/ADV High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 10	ns(3)
T_{WHBX}	BHE Hold after WR High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after WR High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after WR High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	BHE Hold after RD High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after RD High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after RD High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.

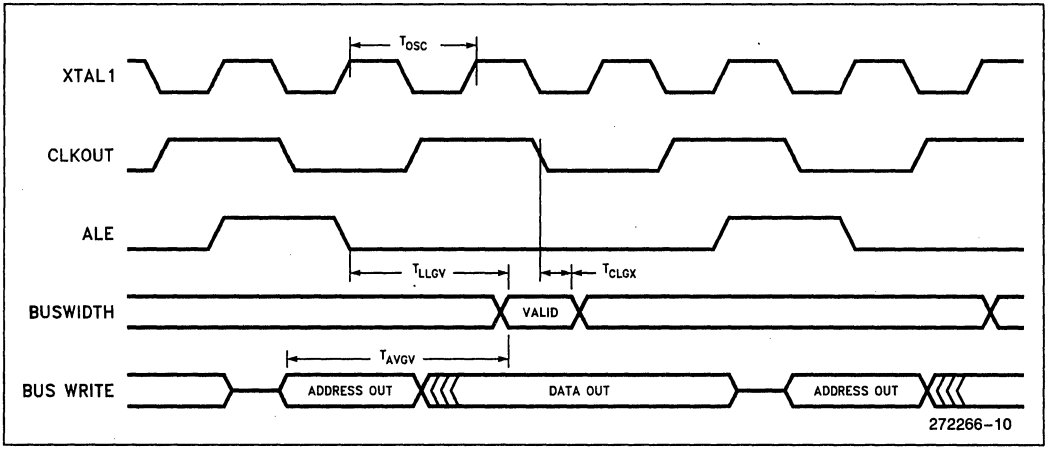
MODE 1—8XC196KT SYSTEM BUS TIMING



MODE 1—8XC196KT READY TIMINGS (ONE WAIT STATE)



MODE 1—8XC196KT BUSWIDTH TIMINGS



BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196KT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		2.5 T_{OSC} − 75	ns
T_{LLYV}	ALE Low to READY Setup		1.5 T_{OSC} − 70	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		2.5 T_{OSC} − 75	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{1.5\ OSC}$ − 60	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3.5 T_{OSC} − 55	ns(2)
T_{RLDV}	RD Active to Input Data Valid		2 T_{OSC} − 44	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 60	ns
T_{RHDZ}	End of RD to Input Data Float		0.5 T_{OSC}	ns
T_{RHDX}	Data Hold after RD High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 Tosc × n, where n = number of wait states. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add 2 Tosc to the specification.

BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

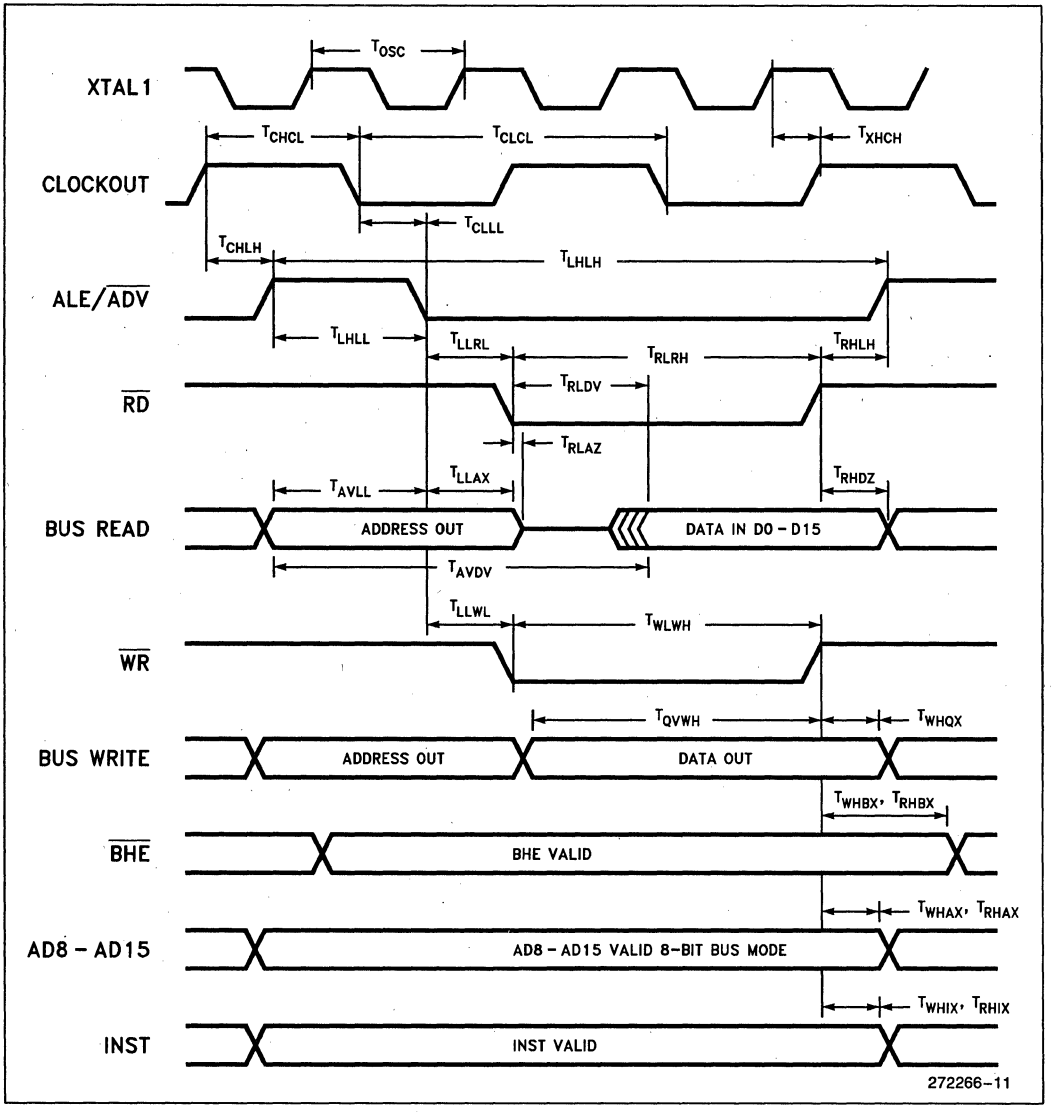
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196KT will meet these specifications

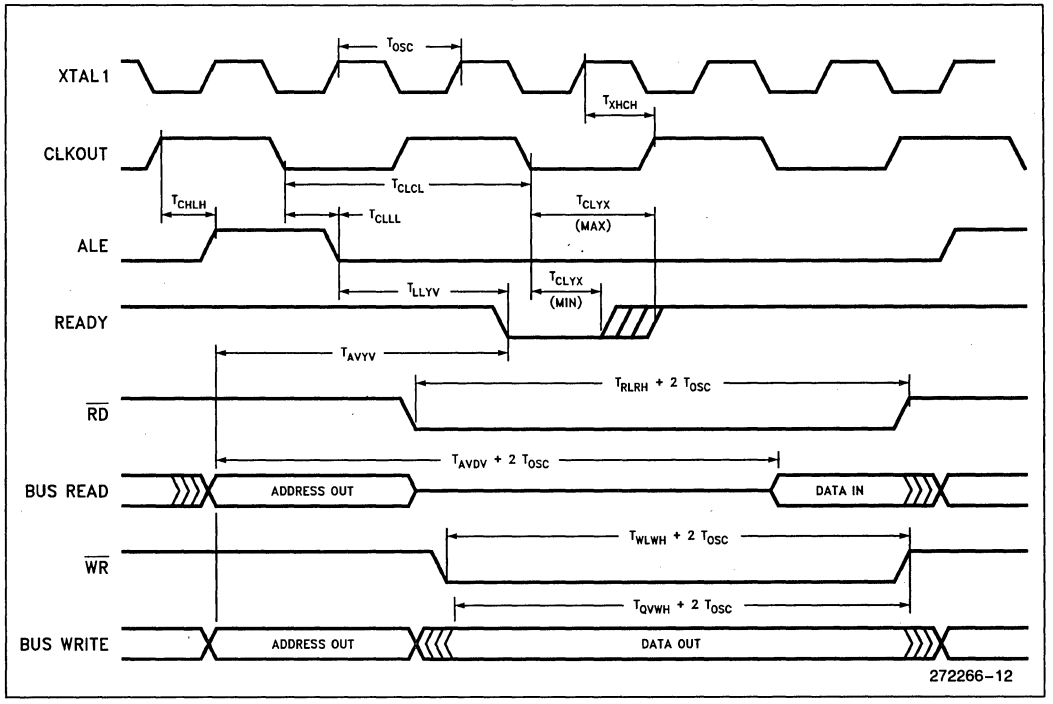
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	16.0	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+85	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CLLL}	CLKOUT Low to ALE/ADV Low	0.5 T_{OSC}−25	0.5 T_{OSC}+15	ns
T_{LHLH}	ALE/ADV Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/ADV High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/ADV Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/ADV Low to RD Low	0.5 T_{OSC} − 10		ns
T_{RLCL}	RD Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} +30	ns
T_{RLRH}	RD Low Period	2T_{OSC} − 20		ns(5)
T_{RHLH}	RD High to ALE/ADV High	0.5 T_{OSC}−5	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	RD Low to Address Float		+5	ns
T_{LLWL}	ALE/ADV Low to WR Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to WR Low	T_{OSC} − 22	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before WR High	2 T_{OSC} − 25		ns
T_{CHWH}	CLKOUT High to WR High	−10	+15	ns
T_{WLWH}	WR Low Period	2 T_{OSC} − 20		ns(5)
T_{WHQX}	Data Hold after WR High	0.5 T_{OSC} − 25		ns
T_{WHLH}	WR High to ALE/ADV High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 10	ns(3)
T_{WHBX}	BHE Hold after WR High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after WR High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after WR High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	BHE Hold after RD High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after RD High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after RD High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.

MODE 2—8XC196KT SYSTEM BUS TIMING



MODE 2—8XC196KT READY TIMINGS (ONE WAIT STATE)



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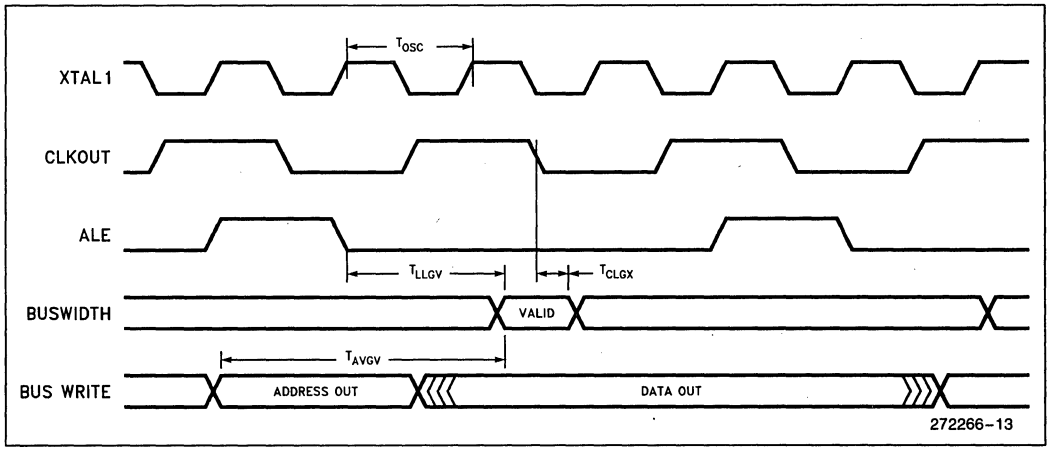
MODE 2—8XC196KT BUSWIDTH TIMINGS



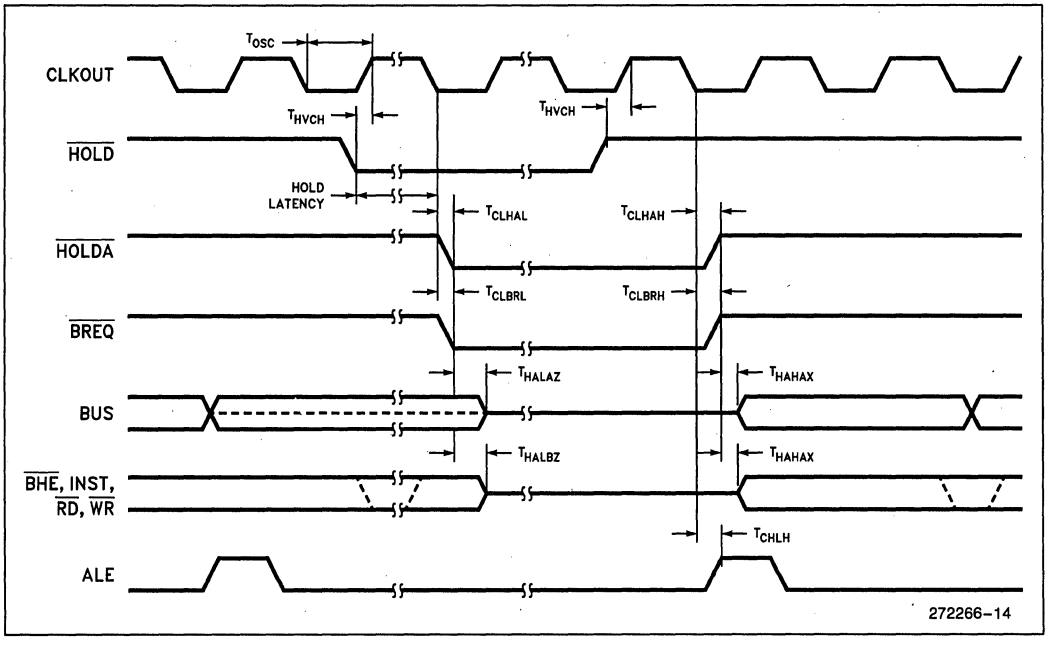
BUS MODE 0, 1, 2, and 3 HOLD/HOLDA TIMINGS (Over Specified Operation Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

Symbol	Parameter	Min	Max	Units
T_{HVCH}	$\overline{HOLD}$ Setup Time	+65		ns(1)
T_{CLHAL}	CLKOUT Low to $\overline{HLDA}$ Low	−15	+15	ns
T_{CLBRL}	CLKOUT Low to $\overline{BREQ}$ Low	−15	+15	ns
T_{AZHAL}	$\overline{HLDA}$ Low to Address Float		+25	ns
T_{BZHAL}	$\overline{HLDA}$ Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+25	ns
T_{CLHAH}	CLKOUT Low to $\overline{HLDA}$ High	−25	+15	ns
T_{CLBRH}	CLKOUT Low to $\overline{BREQ}$ High	−25	+25	ns
T_{HAHAX}	$\overline{HLDA}$ High to Address No Longer Float	−15		ns
T_{HAHBV}	$\overline{HLDA}$ High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10		ns

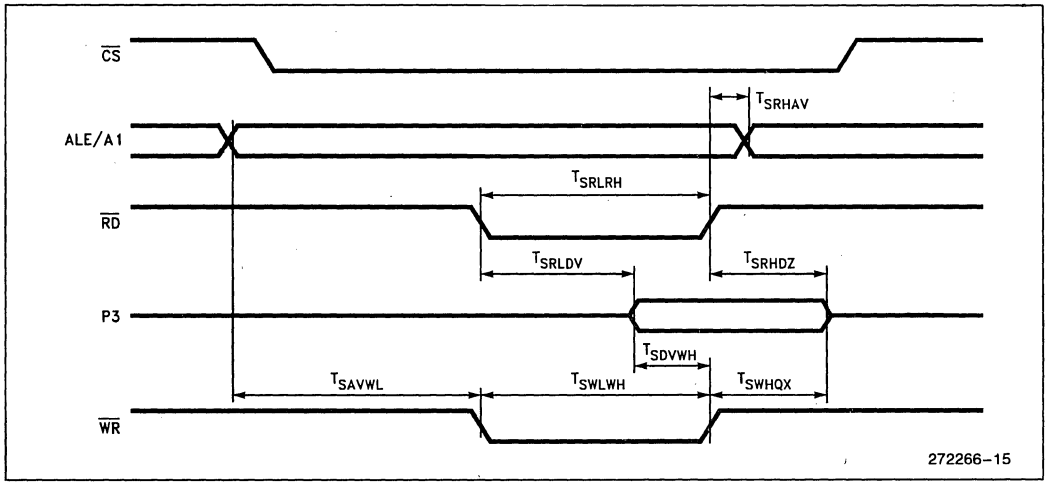
NOTE:
1. To guarantee recognition at next clock.

8XC196KT $\overline{HOLD}$/$\overline{HOLDA}$ TIMINGS



AC CHARACTERISTICS—SLAVE PORT

SLAVE PORT WAVEFORM—(SLPL = 0)



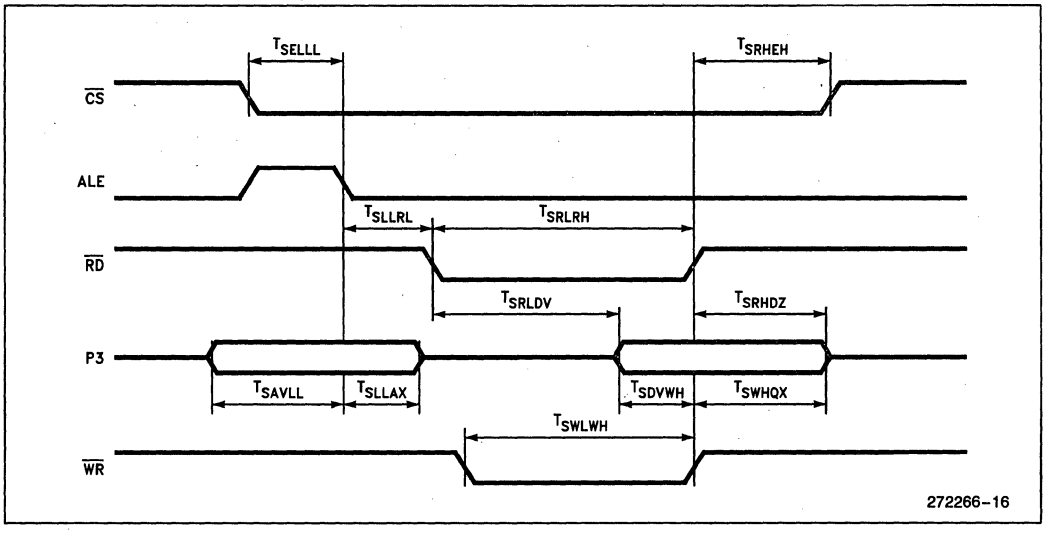
SLAVE PORT TIMING—(SLPL = 0, 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SAVWL}	Address Valid to $\overline{WR}$ Low	50		ns
T_{SRHAV}	$\overline{RD}$ High to Address Valid	60		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 16 MHz, T_{OSC} = 60 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

AC CHARACTERISTICS—SLAVE PORT (Continued)

SLAVE PORT WAVEFORM—(SLPL = 1)



SLAVE PORT TIMING—(SLPL = 1, 2, 3)

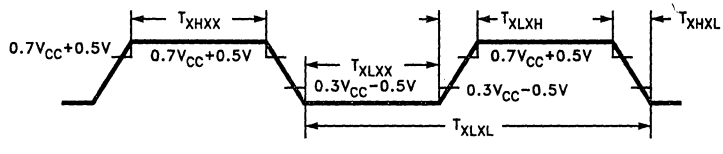
Symbol	Parameter	Min	Max	Units
T_{SELLL}	$\overline{CS}$ Low to ALE Low	20		ns
T_{SRHEH}	$\overline{RD}$ or $\overline{WR}$ High to $\overline{CS}$ High	60		ns
T_{SLLRL}	ALE Low to $\overline{RD}$ Low	T_{OSC}		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SAVLL}	Address Valid to ALE Low	20		ns
T_{SLLAX}	ALE Low to Address Invalid	20		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 16 MHz, T_{OSC} = 60 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	250	ns
T_{XHXX}	High Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



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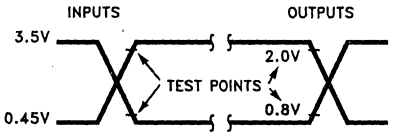
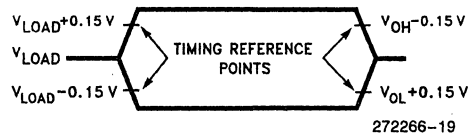
AC TESTING INPUT, OUTPUT WAVEFORMS



272266-18

AC Testing inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS

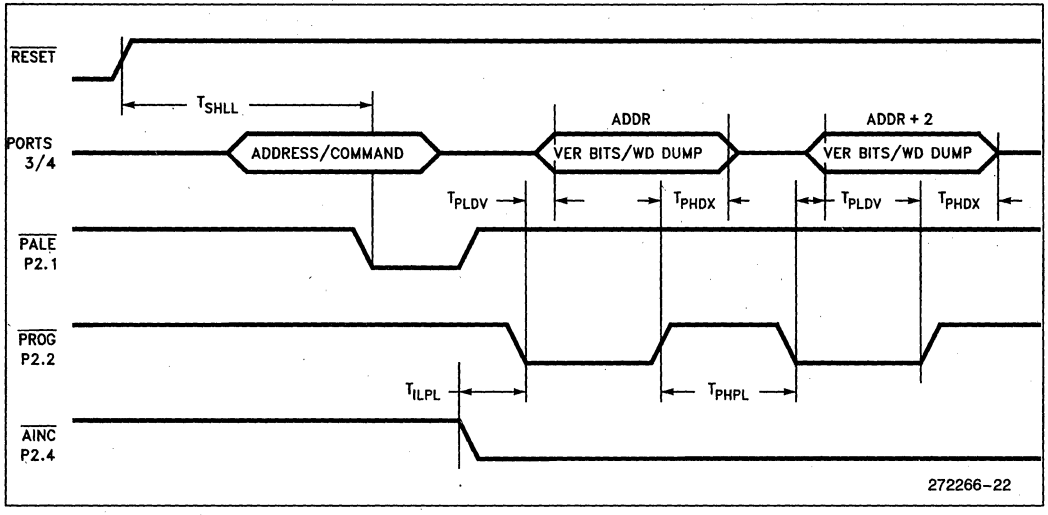


272266-19

For timing purposes a Port Pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq 15$ mA.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



AC CHARACTERISTICS—SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFTING REGISTER MODE

Test Conditions: T_A = −40°C to +125°C; V_{CC} = 5.0V ±10%; V_{SS} = 0.0V; Load Capacitance = pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} − 50	T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}(1)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(1)	Last Clock Rising to Output Float		5 T_{OSC}	ns

NOTE:
1. Parameters not tested.

A TO D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	1.0		µs(2)
T_{CONV}	Conversion Time	10	15	µs(2)
F_{OSC}	Oscillator Frequency	4.0	16.0	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3.0	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3.0	LSBs
Differential Non-Linearity		−0.75	+0.75	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	µA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An "LSB" as used here has a value of approximately 20 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	1.0		µs(2)
T_{CONV}	Conversion Time	7	20	µs(2)
F_{OSC}	Oscillator Frequency	4.0	16.0	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1.0	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1.0	LSBs
Differential Non-Linearity		−0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	µA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An "LSB" as used here has a value of approximately 20 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}	Supply Voltage during Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage during Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	16.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

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AC EPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(2)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run-time programming is done with Fosc = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5V ±0.5V, T_C = 25°C ±5°C and V_{PP} = 12.5V ±0.25V. For run-time programming over a full operating range, contact factory.
2. Programming specifications are not tested, but guaranteed by design.
3. This specification is for the word dump mode. For programming pulses use Modified Quick Pulse Algorithm.

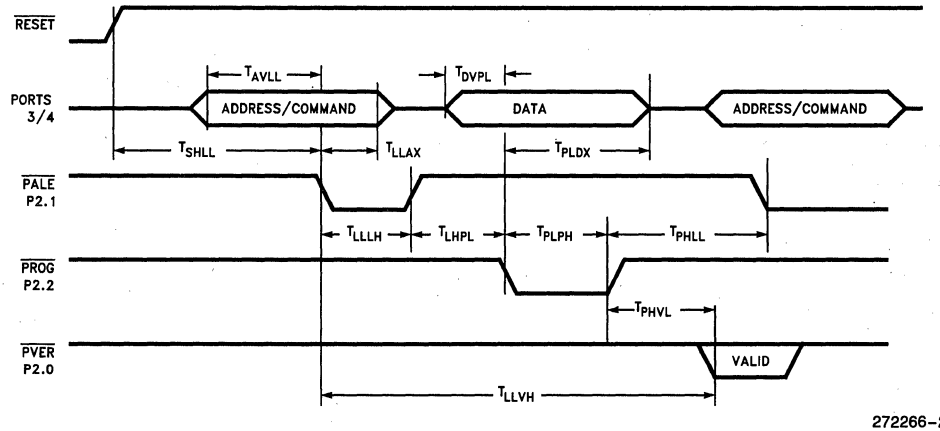
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		200	mA

NOTE:
Don not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

EPROM PROGRAMMING WAVEFORMS

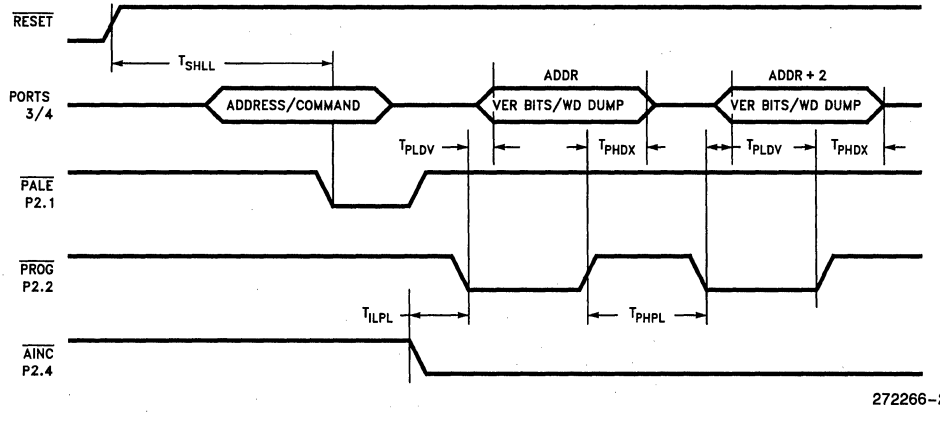
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



272266-21

NOTE:
P3.0 must be HIGH ("1")

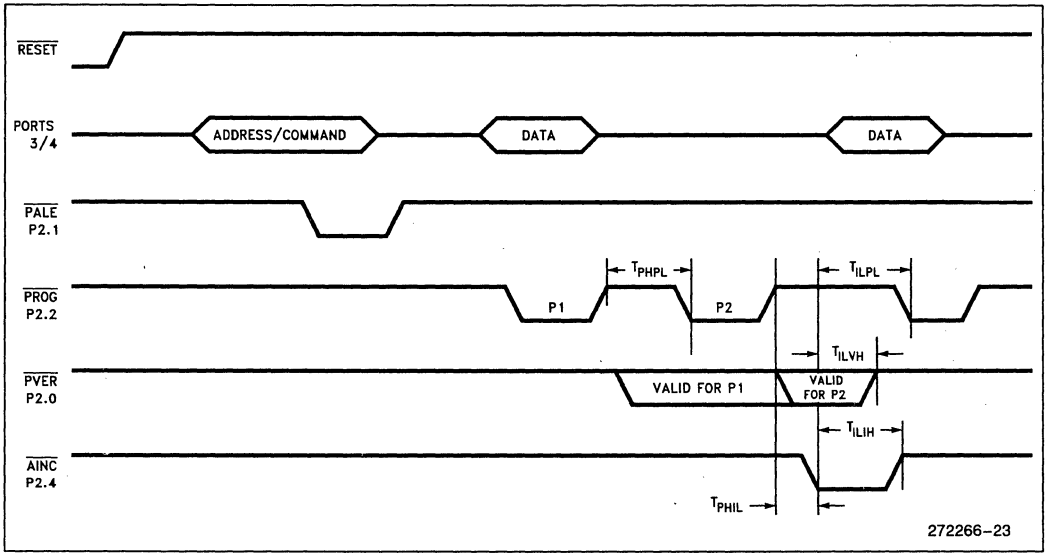
SLAVE PROGRAMMING MODE IN WORD DUMP MODE WITH AUTO INCREMENT



272266-22

NOTE:
P3.0 must be LOW ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



8XC196KT ERRATA

The following is a list of all known functional deviations for 8XC196KT devices. C-step devices can be identified by a special mark following the eight digit FPO number on the top of the package. For C-step devices, this mark is a "C".

1. The following reserved op-codes do not generate the unimplemented op-code interrupt: 1Ch, 1Dh, 1Eh, 1Fh, E3h, E4h, E6h, E8h, E9h, EAh, EBh and F1h.

8XC196MC Data Sheet

21

8XC196MC INDUSTRIAL MOTOR CONTROL MICROCONTROLLER

87C196MC 16 Kbytes of On-Chip OTPROM*
83C196MC 16 Kbytes of On-Chip ROM

- **High Performance CHMOS 16-Bit CPU**
- **16 Kbytes of On-Chip OTPROM/ROM**
- **488 bytes of On-Chip Register RAM**
- **Register to Register Architecture**
- **Up to 53 I/O Lines**
- **Peripheral Transaction Server (PTS) with 11 Prioritized Sources**
- **Event Processor Array (EPA)**
  - **— 4 High Speed Capture/Compare Modules**
  - **— 4 High Speed Compare Modules**
- **Extended Temperature Standard**
- **Two 16-Bit Timers with Quadrature Decoder Input**
- **3-Phase Complementary Waveform Generator**
- **13 Channel 8/10-Bit A/D with Sample/Hold with Zero Offset Adjustment H/W**
- **14 Prioritized Interrupt Sources**
- **Flexible 8/16-Bit External Bus**
- **1.75 μs 16 x 16 Multiply**
- **3 μs 32/16 Divide**
- **Idle and Power Down Modes**

21

The 8XC196MC is a 16-bit microcontroller designed primarily to control 3 phase AC induction and DC brushless motors. The 8XC196MC is based on Intel's MCS®-96 16-bit architecture and is manufactured with Intel's CHMOS process.

The 8XC196MC has a three phase waveform generator specifically designed for use in "Inverter" motor control applications. This peripheral allows for pulse width modulation, three phase sine wave generation with minimal CPU intervention. It generates 3 complementary non-overlapping PWM pulses with resolutions of 0.125 μs (edge trigger) or 0.250 μs (centered).

The 8XC196MC has 16 Kbytes on-chip OTPROM/ROM and 488 bytes of on-chip RAM. It is available in three packages; PLCC (84-L), SDIP (64-L) and EIAJ/QFP (80-L).

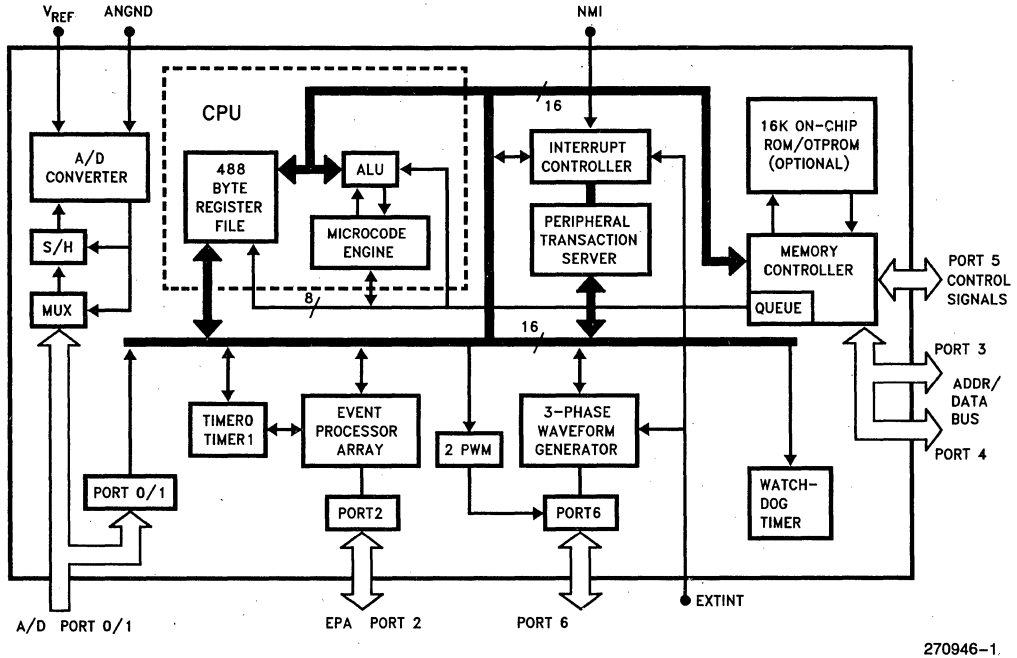
Note that the 64-L SDIP package does not include P1.4, P2.7, P5.1 and the CLKOUT pins.

Operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

The 87C196MC contains 16 Kbytes on-chip OTPROM. The 83C196MC contains 16 Kbytes on-chip ROM. All references to the 80C196MC also refers to the 83C196MC and 87C196MC unless noted.

*OTPROM (One Time Programmable Read Only Memory) is the same as EPROM but it comes in an unwindowed package and cannot be erased. It is user programmable.

September 1992
Order Number: 270946-004

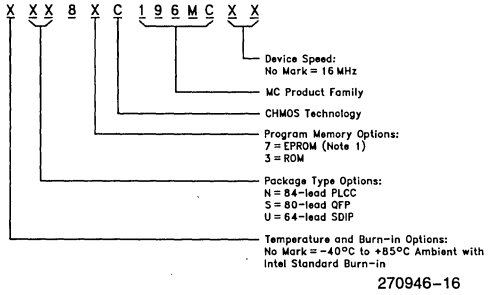


NOTE:
Connections between the standard I/O ports and the bus are not shown.

Figure 1. 87C196MC Block Diagram

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196MC is 84-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 3. The 8XC196MC Family Nomenclature

Thermal Characteristics

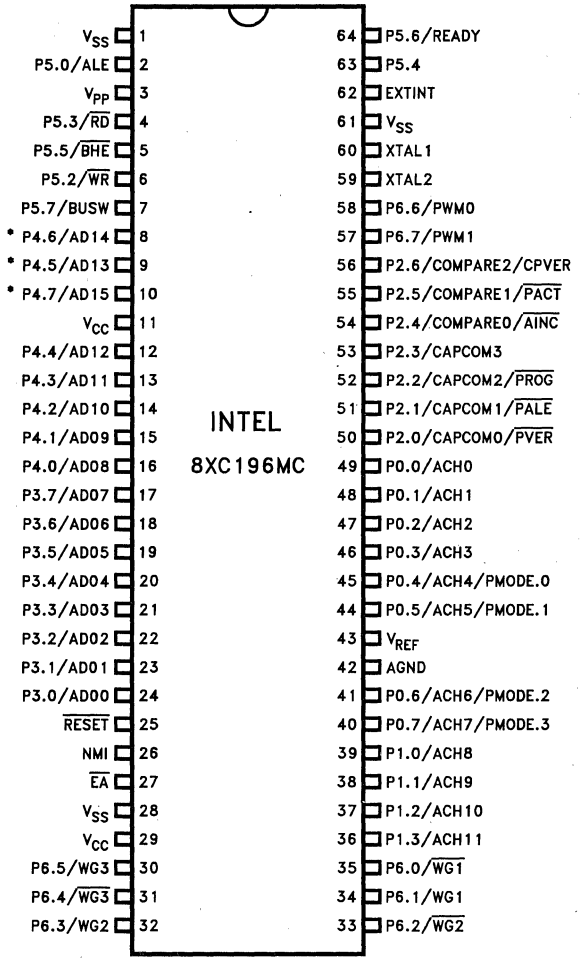
Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	56°C/W	12°C/W
SDIP	TBD	TBD

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

8XC196MC Memory Map

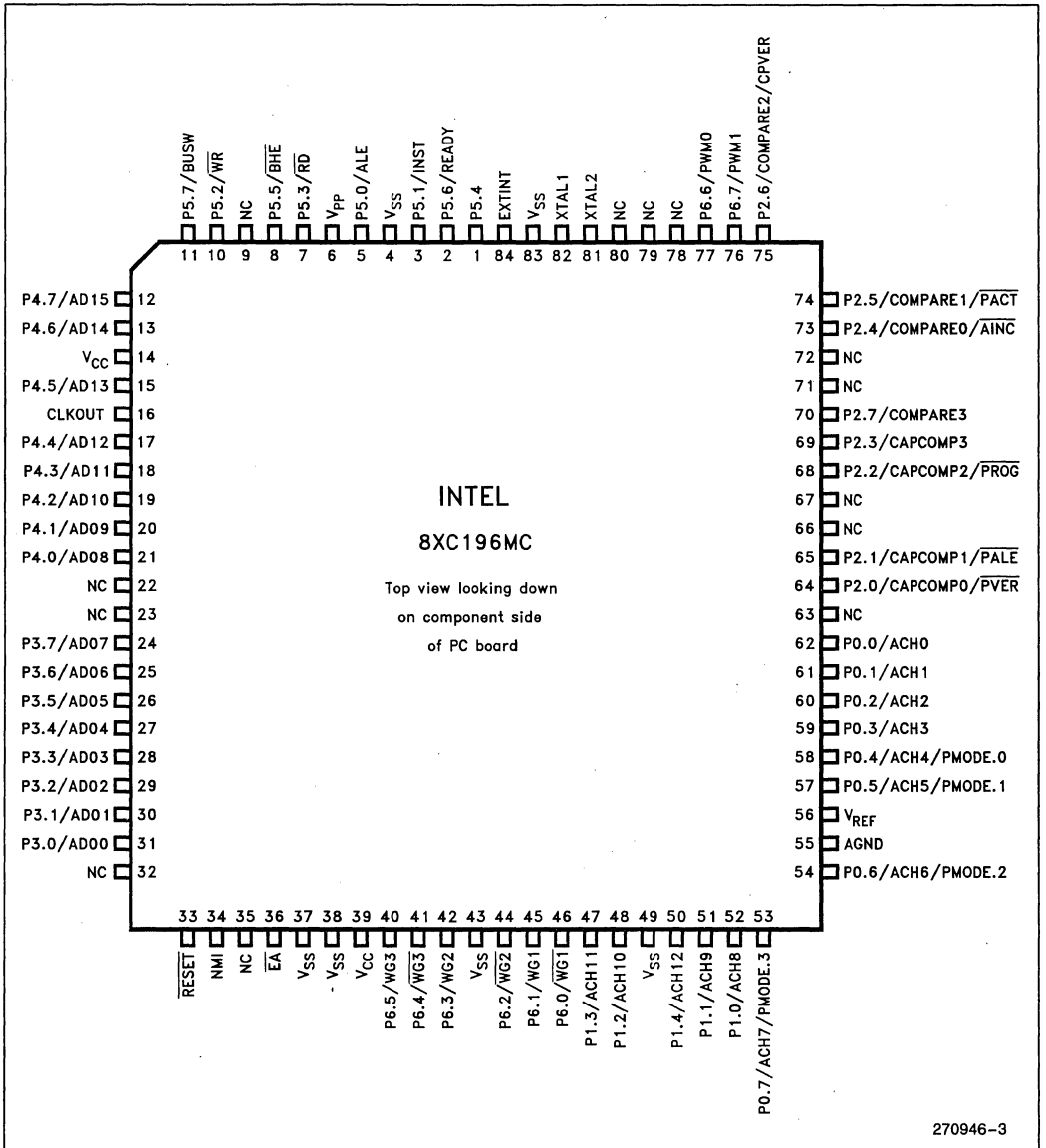
Description	Address
External Memory or I/O	0FFFFH 06000H
Internal ROM/EPROM or External Memory (Determined by $\overline{EA}$)	5FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201CH
Reserved. Must Contain 20H (Note 5)	201BH
CCB1	201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB0	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
SFR's	1FFFH 1F00H
External Memory	1EFFH 0200H
488 Bytes Register RAM (Note 1)	01FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 03FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KC for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.



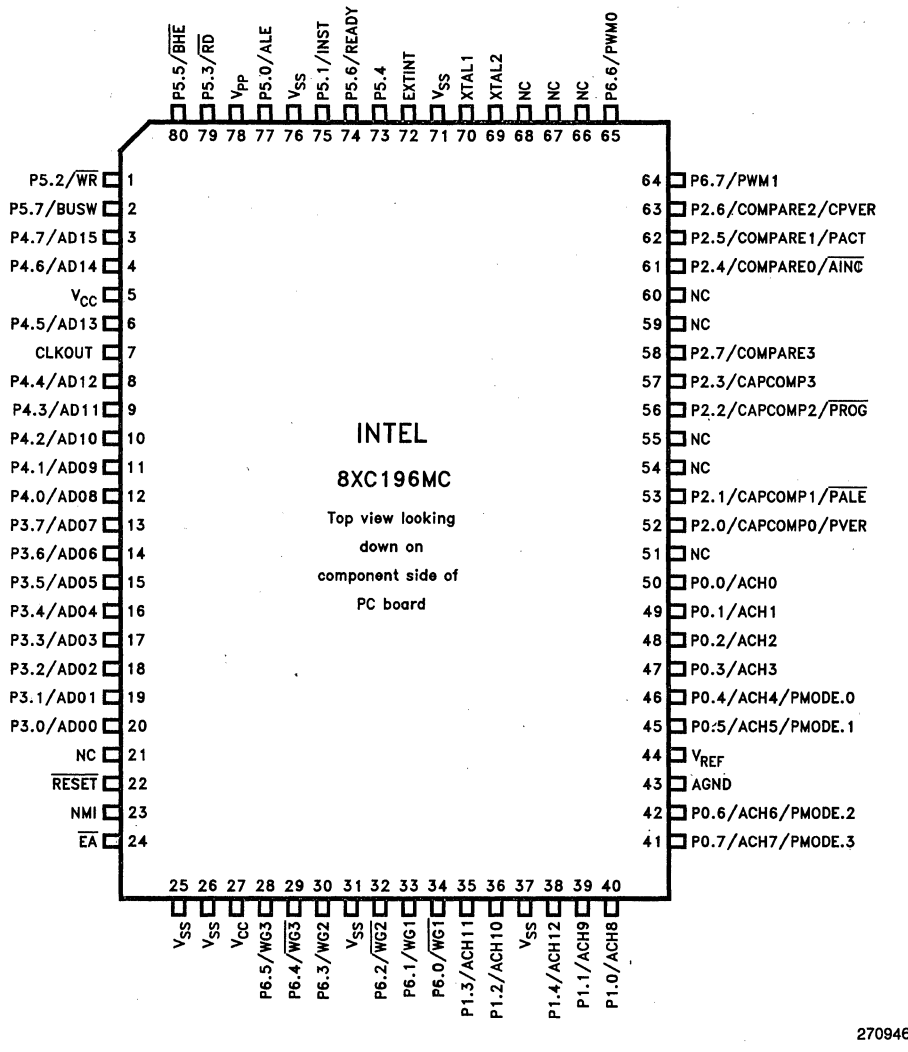
NOTE:
*The pin sequence is correct.
The 64-Lead SDIP package does not include the following pins: P1.4/ACH12, P2.7/COMPARE3, P5.1/INST, CLKOUT.

Figure 2. 64-Lead Shrink DIP (SDIP) Package



NOTE:
NC means No Connect. Do not connect these pins.

Figure 3. 84-Lead PLCC Package



NOTE:
NC means No Connect. Do not connect these pins.

Figure 4. 80-Lead Shrink EIAJQFP (Quad Flat Pack)

PIN DESCRIPTIONS (Alphabetically Ordered)

Symbol	Function
ACH0–ACH12 (P0.0–P0.7, P1.0–P1.4)	Analog inputs to the on-chip A/D converter. ACH0–7 share the input pins with P0.0–7 and ACH8–12 share pins with P1.0–4. If the A/D is not used, the port pins can be used as standard input ports.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
ALE/$\overline{ADV}$(P5.0)	Address Latch Enable or Address Valid output, as selected by CCR. Both options allow a latch to demultiplex the address/data bus on the signal's falling edge. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. ALE/$\overline{ADV}$ is active only during external memory accesses. Can be used as standard I/O when not used as ALE/ADV.
$\overline{BHE}$/$\overline{WRH}$ (P5.5)	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.
BUSWIDTH (P5.7)	Input for bus width selection. If CCR bits 1 and 2 = 1, this pin dynamically controls the bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If it is high, a 16-bit cycle occurs. This pin can be used as standard I/O when not used as BUSWIDTH.
CAPCOMP0–CAPCOMP3 (P2.0–P2.3)	The EPA Capture/Compare pins. These pins share P2.0–P2.3. If not used for the EPA, they can be configured as standard I/O pins.
CLKOUT	Output of the internal clock generator. The frequency is ½ of the oscillator frequency. It has a 50% duty cycle.
COMPARE0–COMPARE3 (P2.4–P2.7)	The EPA Compare pins. These pins share P2.4–P2.7. If not used for the EPA, they can be configured as standard I/O pins.
$\overline{EA}$	External Access enable pin. $\overline{EA}$ = 0 causes all memory accesses to be external to the chip. $\overline{EA}$ = 1 causes memory accesses from location 2000H to 5FFFH to be from the on-chip OTPROM/QROM. $\overline{EA}$ = 12.5V causes execution to begin in the programming mode. $\overline{EA}$ is latched at reset.
EXTINT	A programmable input on this pin causes a maskable interrupt vector through memory location 203CH. The input may be selected to be a positive/negative edge or a high/low level using WG_PROTECT (1FCEH).
INST (P5.1)	INST is high during the instruction fetch from the external memory and throughout the bus cycle. It is low otherwise. This pin can be configured as standard I/O if not used as INST.
NMI	A positive transition on this pin causes a non-maskable interrupt which vectors to memory location 203EH. If not used, it should be tied to V_{SS}. May be used by Intel Evaluation boards.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port0 pins should not be left floating. These pins also used to select programming modes in the OTPROM devices.
PORT1	5-bit high impedance input-only port. P1.0–P1.4 are also used as A/D converter inputs. In addition, P1.2 and P1.3 can be used as Timer 1 clock input and direction select respectively.
PORT2	8-bit bidirectional I/O port. All of the Port2 pins are shared with the EPA I/O pins (CAPCOMP0–3 and COMPARE0–3).
PORT3 PORT4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which uses strong internal pullups.
PORT5	8-bit bidirectional I/O port. 7 of the pins are shared with bus control signals ($\overline{ALE}$, INST, $\overline{WR}$, $\overline{RD}$, $\overline{BHE}$, READY, BUSWIDTH). Can be used as standard I/O.

PIN DESCRIPTIONS (Alphabetically Ordered) (Continued)

Symbol	Function
PORT6	8-bit output port. P6.6 and P6.7 output PWM, the others are used as the Wave Form Generator outputs. Can be used as standard output ports.
PWM0, PWM1 (P6.6, P6.7)	Programmable duty cycle, Programmable frequency Pulse Width Modulator pins. The duty cycle has a resolution of 256 steps, and the frequency can vary from 122 Hz to 31 KHz (16 MHz input clock). Pins may be configured as standard output if PWM is not used.
$\overline{RD}$ (P5.3)	Read signal output to external memory. $\overline{RD}$ is low only during external memory reads. Can be used as standard I/O when not used as $\overline{RD}$.
READY (P5.6)	Ready input to lengthen external memory cycles. If READY = 0, the memory controller inserts wait states until the next positive transition of CLKOUT occurs with READY = 1. Can be used as standard I/O when not used as READY.
$\overline{RESET}$	Reset input to and open-drain output from the chip. Held low for at least 16 state times to reset the chip. Input high for normal operation. $\overline{RESET}$ has an Ohmic internal pullup resistor.
T1CLK (P1.2)	Timer 0 Clock input. This pin has two other alternate functions: ACH10 and P1.2.
T1DIR (P1.3)	Timer 0 Direction input. This pin has two other alternate functions: ACH11 and P1.3.
V_{PP}	The programming voltage is applied to this pin. It is also the timing pin for the return from Power Down circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If the Power Down feature is not used, connect the pin to V_{CC}.
WG1–WG3/$\overline{WG1}$–$\overline{WG3}$ (P6.0–P6.5)	3 phase output signals and their complements used in motor control applications. The pins can also be configured as standard output pins.
$\overline{WR}$/$\overline{WRL}$ (P5.2)	Write and Write Low output to external memory. $\overline{WR}$ will go low every external write. $\overline{WRL}$ will go low only for external writes to an even byte. Can be used as standard I/O when not used as $\overline{WR}$/$\overline{WRL}$.
XTAL1	Input of the oscillator inverter and the internal clock generator. This pin should be used when using an external clock source.
XTAL2	Output of the oscillator inverter.
PMODE (P0.4–7)	Determines the EPROM programming mode.
$\overline{PACT}$ (P2.5)	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
$\overline{PALE}$ (P2.1)	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{PROG}$ (P2.2)	A falling edge in Slave Programming Mode begins programming. A rising edge ends programming.
PVER (P2.0)	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
CPVER (P2.6)	Cumulative Program Verification. Pin is high if all locations since entering a programming mode have programmed correctly.
$\overline{AINC}$ (P2.4)	Auto Increment. Active low input enables the auto increment mode. Auto increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage from $\overline{EA}$ or V_{PP}
to V_{SS} or ANGND ..... +13.00V
Voltage on V_{PP} or $\overline{EQ}$
to V_{SS} or ANGND ..... −0.5V to 13.0V
Voltage on Any Other Pin
to V_{SS} or ANGND ..... −0.5V to +7.0V(1)
Power Dissipation ..... 1.5W(2)

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
F_{OSC}	Oscillator Frequency	8	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential. Also V_{SS} and V_{SS1} must be at the same potential.

DC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage Port 2 and 5, P6.6, P7, CLKOUT		0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage on Port 3/4		1.0	V	I_{OL} = 15 mA
V_{OL2}	Output Low Voltage on Port 6.0–6.5		0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
$V_{th+}-V_{th-}$	Hysteresis Voltage Width on $\overline{RESET}$ and All Input Pins except Port 3, Port 4 and Port 5 besides P5.3	0.2		V	Typical

DC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Leakage Current on All Input Only Pins			±10	µA	$0V < V_{IN} < V_{CC}-0.3V$ (in RESET)
I_{LI1}	Input Leakage Current on Port0 and Port1			±3	µA	$0V < V_{IN} < V_{REF}$
I_{IL}	Input Low Current on BD Ports (Note 1)			−70	µA	$V_{IN} = 0.3\ V_{CC}$
I_{IL1}	Input Low Current on P5.4 and P2.6 during Reset			−7	mA	$0.2\ V_{CC}$
I_{OH}	Output High Current on P5.4 and P2.6 during Reset	−2			mA	$0.7\ V_{CC}$
I_{CC}	Active Mode Current in Reset		50	70	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Conversion Reference Current		2	5	mA	
I_{IDL}	Idle Mode Current		15	30	mA	
I_{PD}	Power-Down Mode Current		5	50	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	$\overline{\text{RESET}}$ Pin Pullup Resistor	6k		65k	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:

1. BD (Bidirectional ports) include:
   P2.0–P2.7, except P2.6
   P3.0–P3.7
   P4.0–P4.7
   P5.0–P5.3
   P5.5–P5.7
2. During normal (non-transient) conditions, the following total current limits apply:

P6.0–P6.5	I_{OL}: 40 mA	I_{OH}: 28 mA
P3	I_{OL}: 90 mA	I_{OH}: 42 mA
P4	I_{OL}: 90 mA	I_{OH}: 42 mA
P5, CLKOUT	I_{OL}: 35 mA	I_{OH}: 35 mA
P2, P6.6, P6.7	I_{OL}: 63 mA	I_{OH}: 63 mA

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H — High
L — Low
V — Valid
X — No Longer Valid
Z — Floating

Signals:

A — Address
B — $\overline{BHE}$
C — CLKOUT
D — DATA
G — Buswidth
H — $\overline{HOLD}$
HA — $\overline{HLDA}$
L — ALE/$\overline{ADV}$
BR — $\overline{BREQ}$
R — $\overline{RD}$
W — $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X — XTAL1
Y — READY
Q — Data Out

AC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

The system must meet the following specifications to work with the 87C196MC:

Symbol	Parameter	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1	8	16	MHz	3
T_{OSC}	1/F_{XTAL}	62.5	125	ns	
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} − 75	ns	
T_{LLYV}	ALE Low to READY Setup		T_{OSC} − 70	ns	4
T_{YLYH}	Not READY Time	No Upper Limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns	1
T_{LLYX}	READY Hold after ALE Low	T_{OSC} − 15	2 T_{OSC} − 40	ns	1
T_{AVGV}	Address Valid to BUSWIDTH Setup		2 T_{OSC} − 75	ns	
T_{LLGV}	ALE Low to BUSWIDTH Setup		T_{OSC} − 60	ns	4
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 55	ns	2
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 22	ns	2
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 50	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.
3. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
4. These timings are included for compatibility with older −90 and BH products. They should not be used for newer high-speed designs.

AC ELECTRICAL CHARACTERISTICS (Continued)

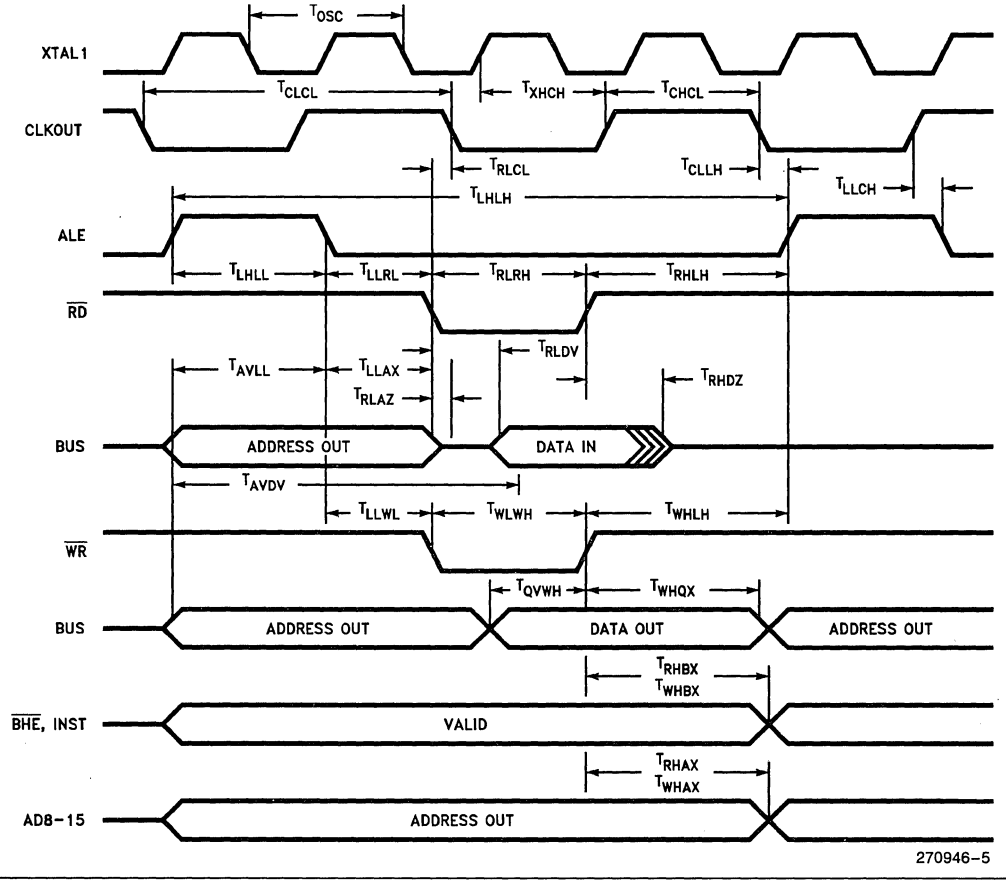
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

The 87C196MC will meet the following timing specifications:

Symbol	Parameter	Min	Max	Units	Notes
T_{XHCH}	XTAL1 to CLKOUT High or Low	30	110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	3
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15		ns	
T_{LLAX}	Address Hold after ALE Falling	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling	T_{OSC} − 30		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	3
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	1
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30		ns	3
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 25		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	1
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ Rising	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising	T_{OSC} − 30		ns	2
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ Rising	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising	T_{OSC} − 30		ns	2

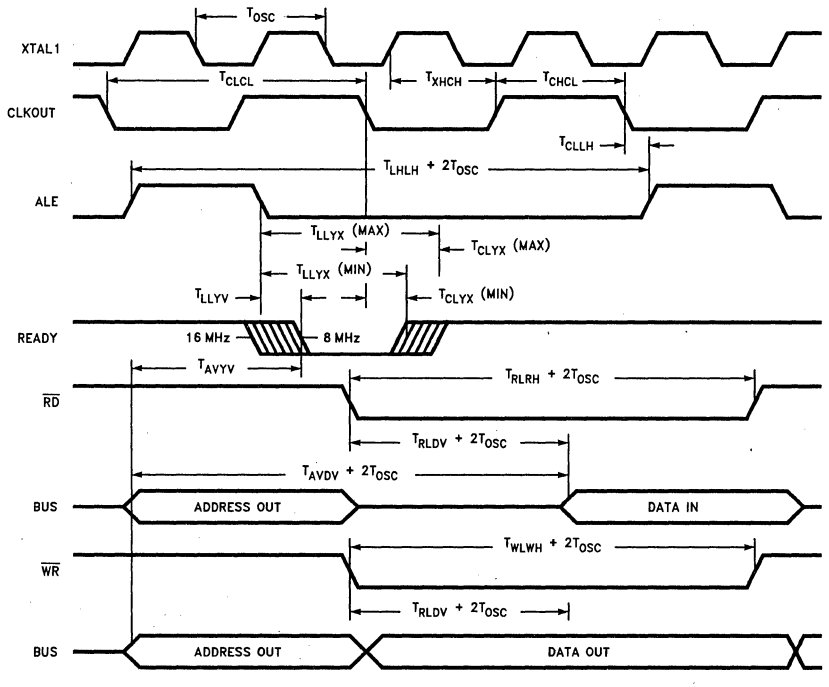
NOTES:
1. Assuming back to back cycles.
2. 8-bit bus only.
3. If wait states are used, add 2 T_{OSC}*N, where N = number of wait states.

SYSTEM BUS TIMINGS



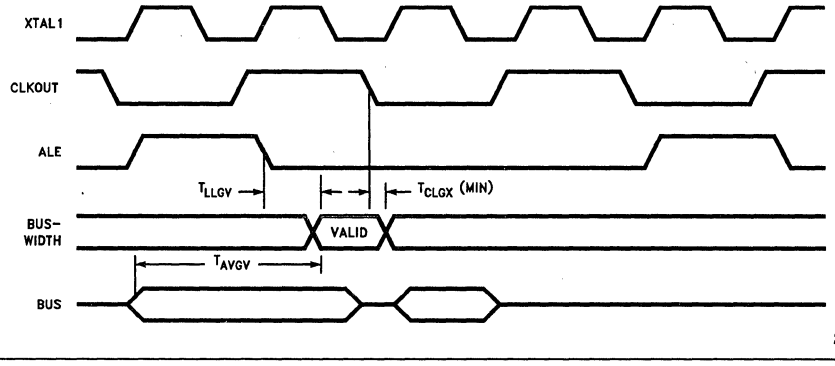
21

READY TIMINGS (One Wait State)



270946-6

BUSWIDTH TIMINGS

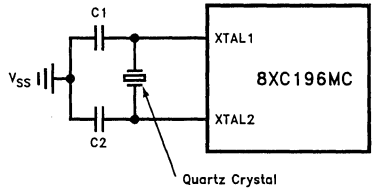


270946-7

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	22		ns
T_{XLXX}	Low Time	22		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

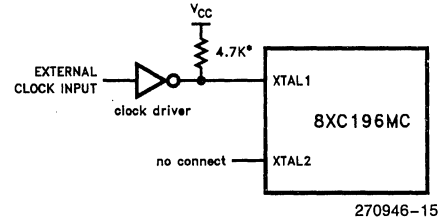
EXTERNAL CRYSTAL CONNECTIONS



270946-14

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

EXTERNAL CLOCK CONNECTIONS



270946-15

* Required if TTL driver used.
Not needed if CMOS driver is used.

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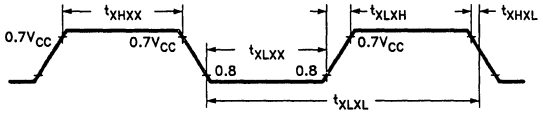
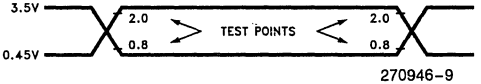
EXTERNAL CLOCK DRIVE WAVEFORMS



270946-8

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

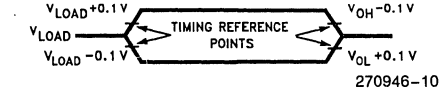
AC TESTING INPUT, OUTPUT WAVEFORMS



270946-9

AC Testing inputs are driven at 3.5V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



270946-10

For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \leq \pm 15$ mA.

A TO D CHARACTERISTICS

The sample and conversion time of the A/D converter in the 8-bit or 10-bit modes is programmed by loading a byte into the AD_TIME Special Function Register. This allows optimizing the A/D operation for specific applications. The AD_TIME register is functional for all possible values, but the accuracy of the A/D converter is only guaranteed for the times specificed in the operating conditions table.

The value loaded into AD_TIME bits 5, 6, 7 determines the sample time, T_{SAM}, and is calculated using the following formula:

$$SAM = \frac{(T_{SAM} \times F_{OSC}) - 2}{8}$$

T_{SAM} = Sample time, μs
F_{OSC} = Processor frequency, MHz
SAM = Value loaded into AD_TIME bits 5, 6, 7

SAM must be in the range 1 through 7.

The value loaded into AD_TIME bits 0–5 determines the conversion time, T_{CONV}, and is calculated using the following formula:

$$CONV = \frac{(T_{CONV} \times F_{OSC}) - 3}{2B} - 1$$

T_{CONV} = Conversion time, μs
F_{OSC} = Processor frequency, MHz
B = 8 for 8-bit conversion
B = 10 for 10-bit conversion
CONV = Value loaded into AD_TIME bits 0–5

CONV must be in the range 2 through 31.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the analog portion of the converter and input port pins. There is also an AD_TEST SFR that allows for conversion on ANGND and V_{REF} as well as adjusting the zero offset. The absolute error listed is WITHOUT doing any adjustments.

A/D CONVERTER SPECIFICATION

The specifications given assume adherence to the operating conditions section of this data sheet. Testing is performed with V_{REF} = 5.12V and 16.0 MHz operating frequency. After a conversion is started, the device is placed in the IDLE mode until the conversion is complete.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	10.0	20.0	μs(2)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTES:
ANGND and V_{SS} should nominally be at the same potential.
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Levels Bits
Absolute Error		0	±4	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±4	LSBs
Differential Non-Linearity		>−1	+2	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	2K	Ω(4)
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5, 6)
Sampling Capacitor	3			pF
DC Input Leakage	±1	0	±3.0	μA

NOTES:
*An "LSB", as used here has a value of approximately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	7.0	20.0	μs(2)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTES:
ANGND and V_{SS} should nominally be at the same potential.
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over the Above Operating Conditions)

Parameter	Typical(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1	LSBs
Differential Non-Linearity		>−1	+1	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25			LSBs
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	2K	Ω(4)
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V(5, 6)
Sampling Capacitor	3			pF
DC Input Leakage	±1	0	±3.0	μA

NOTES:
*An "LSB" as used here, has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}	Supply Voltage during Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage during Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
T_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

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AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	PROG High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

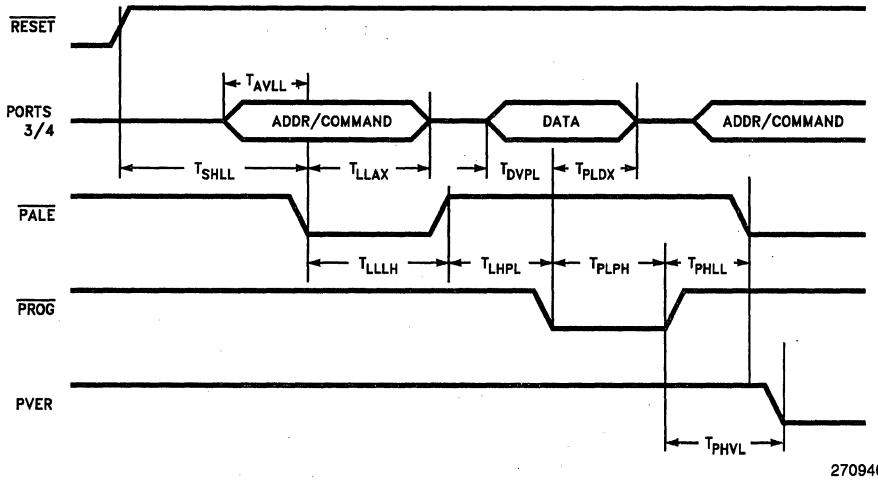
NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

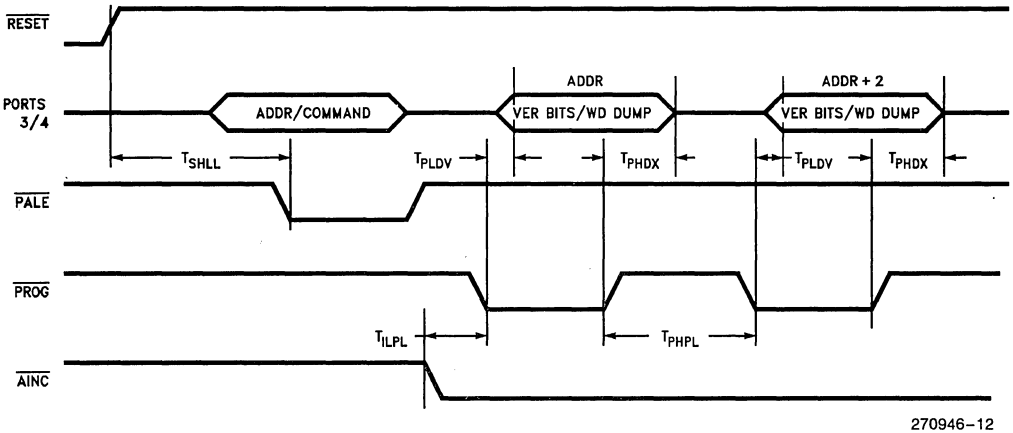
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



2709461-11

NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



NOTE:
P3.0 must be low ("0")

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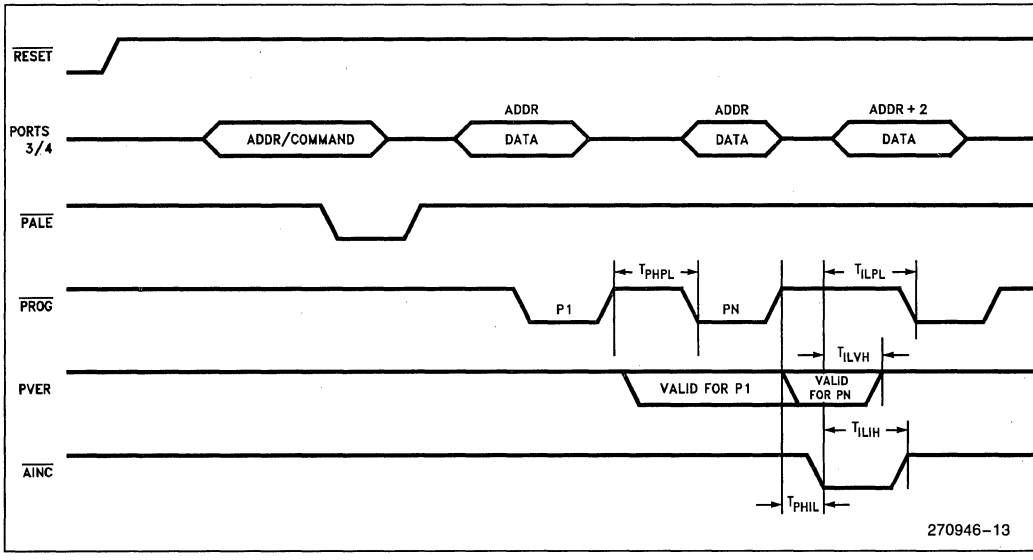
SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



87C196MC DESIGN CONSIDERATIONS

When an indirect shift during divide occurs the upper 3 bits of the shift count are not masked completely. If the shift count register has the value 32*n where n = 1, 3, 5 or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

DATA SHEET REVISION HISTORY

This data sheet (270946-004) is valid for devices with a "B" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following important differences exist between this data sheet (270946-002) and the previous version (270946-003):

1. The data sheet was reorganized to standard format.
2. Added 83C196MC device.
3. Added package thermal characteristics.
4. Added note on missing pins on SDIP package.
5. Removed SFR maps (now in user's manual).
6. Added note on T_{LLYV} and T_{LLGV} specifications.
7. Changed 10-bit mode T_{CONV} (MIN) to 10.0 μs from 15.0 μs.
8. Changed 10-bit mode T_{CONV} (MAX) to 20.0 μs from 18.0 μs.
9. Changed VREF (MIN) in 8- and 10-bit mode to 4.0V from 4.5V.

The following important differences exist between data sheet 270946-003 and the previous version (270946-002):

1. The data sheet title was changed to better reflect the purpose of the 87C196MC as an AC Inverter/DC Brushless Motor Control Microcontroller.
2. The standard temperature range for this part now covers $-40°C$ to $+85°C$.
3. EXTINT function description now includes WG_PROTECT (1FCEH) as the name and address of the register used to select positive/negative or high/low detection for EXTINT.
4. The memory range 01F00H–01FBFH was added to the SFR map as RESERVED.
5. I_{IL} changed from -60 μA to -70 μA.
6. I_{REF} changed from 5 mA to 2 mA maximum and the typical specification was removed.
7. The READY description of the READY TIMINGS (One Wait State) graphic was modified to denote the shifting of the leading edge of READY versus frequency. At 16 MHz the falling edge of READY occurs before the falling edge of ALE.
8. AC Testing Input, Output Waveform was changed to reflect inputs driven at 3.5V for a Logic "1" and .45V for a Logic "0" and timing measurements made at 2.0V for a Logic "1" and 0.8V for a Logic "0".
9. Float Waveform was changed from $I_{OL}/I_{OH} = \pm 15$ mA to $I_{OL}/I_{OH} \leq \pm 15$ mA
10. AD_TIME register for 10-bit conversions was changed from 0C7H to 0D8H. The number of sample time states was changed from 24 to 25 states, the conversion time states was changed from 80 to 240 states, and the total conversion time for AD_TIME = D8H replaced the total conversion time for AD_TIME = C7H.
11. The number of sample time states for an 8-bit conversion was changed from 20 states to 21 states.
12. There is a single entry in the ERRATA section of this version of the data sheet concerning the results of an indirect shift during divide.

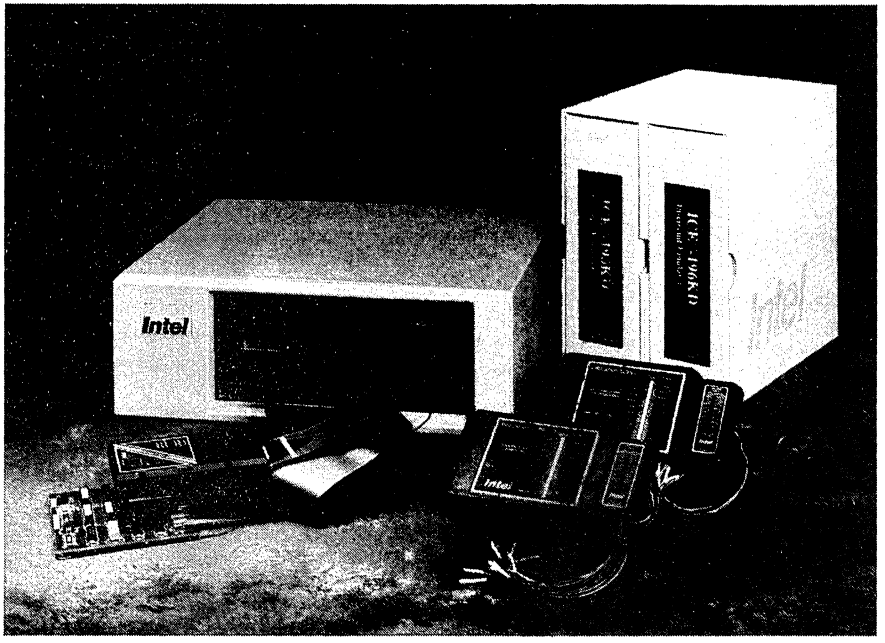
The following important differences exist between this data sheet (270946-002) and the previous version (270946-001):

1. T_A Ambient Temperature Under Bias Min changed from $-20°C$ to $-40°C$.
2. I_{REF} A/D Conversion Reference Current Max changed from 5 mA to 2 mA.
3. Testing levels changed from TTL values to CMOS values.
4. A/D Input Series Resistance Max changed from 1.2 KΩ to 2 KΩ.

MCS®-96 Development Support Tools

22

ICE™-196KD/HX IN-CIRCUIT EMULATOR



280902-1

22

REAL-TIME IN-CIRCUIT EMULATION FOR MCS®-96 MICROCONTROLLERS

Intel's ICE™-196KD/HX In-Circuit Emulator (ICE) is an easy-to-use, full-featured tool to help you develop, integrate, and test your MCS-96 microcontroller-based products.

The ICE-196KD/HX supports all component variations offered in the following Intel MCS-96 families: 8xC196KD, 8xC196KC, 8xC196KB, 8xC198, and 8xC194.

The emulator supports all component types as differentiated by ROM, EPROM, and ROMless; as well as components differentiated by temperature, reliability screenings, package types, and speeds (up to 20 MHz). Precise and reliable emulation is assured due to the emulator's matching of the component's electrical and timing characteristics.

FEATURES

- Real-time, Transparent, In-Circuit Emulation at Speeds up to 20 MHz
- On-Circuit Emulation (ONCE) for Emulating Surface-Mounted 8xC196 Devices
- Execution and Bus *Breaks* (including Breaks on Internal Events and "Fastbreaks")
- Execution and Bus *Trace*
- Internal and External Bus Event Recognition
- 128 Kbytes of Zero-Waitstate, Mappable ICE Memory
- Source-Level, Symbolic Debugging
- Full-Color, Windowed, Easy-to-Use Interface (with Pull-Down Menus, Pop-Up Help, Hypertext Browsing, Function Keys, . . .)
- Stand-Alone Operation and Self-Test Diagnostics
- Hosted on IBM PC XTs, ATs, PS/2s and 100% Compatible Machines (Serial Connection from PC to Emulator at up to 57.6 Kbaud)

*IBM PC/AT is a registered trademark of International Business Machines.

September 1992
Order Number: 280902-003

FEATURES

SOPHISTICATED, POWERFUL CAPABILITIES

Event Recognition

To aid the debugging process, the ICE-196KD/HX user has access to very sophisticated event recognition capabilities. Triggering can occur based on:

- Instruction Fetches
- Execution Addresses
- External Data Reads or Writes at a range of addresses
- Internal/External Data Reads or Writes at a specific address
- Internal/External Data Reads or Writes at a specific value
- Internal/External Data Reads or Writes at a range of values
- Signals from an External Device (causing an asynchronous break)
- CLIPSIN Status (8 external Clips available), or
- Trace Buffer Full Events

Compound triggers may be constructed through AND/OR combinations of events. Specifically:

- OR combinations of execution/bus events
- OR combinations of bus/bus events
- AND combinations of bus/bus events

The trace buffer is accessible during emulation. The buffer can contain up to 2048-frames of information such as:

- Addresses
- Opcodes in Hex and Mnemonic Formats
- Operands in Hex and Symbolic Formats
- Bus Address/Data
- Processor Status Bits
- Logic Clips Information

In addition, the ICE-196KD/HX offers the following break and trace features:

- Recognizes up to 255 execution addresses; either specific addresses or address ranges.
- FASTBREAKS: emulation is immediately broken only for the duration of a requested memory access (typically 25 μs at 20 MHz).
- A deferred FASTBREAK option: a FASTBREAK is honored only after reaching a specified address.
- Conditional arming and disarming of *break* specifications (2-state state machine).
- Conditional arming and disarming of *trace* specifications.
- Ability to reprogram break and trace specifications during emulation.
- Break and trace REGISTERS for storing complex break/trace definitions for reuse.

Execution Control

- Single-step execution of machine instructions, high-level language statements, or procedure call blocks.
- Functions to disassemble/assemble memory in the form of machine instructions and to display/modify program variables and special function registers.
- Symbolic referencing to memory locations and information in trace and memory disassembly displays.

System Resources

- The 128 Kbytes of mappable, zero-waitstate ICE memory can be used to:
- Execute and debug programs before target hardware exists
- Simulate non-existent or non-working target memory
- Overlay target EPROM space (avoiding the inconvenience of programming EPROMs).
- Event counters.
- To aid performance analysis, an event timer records the time from/to specified events while an emulation timer records the total duration of emulation.
- Synchronized multi-emulator start and break signals and a trigger out signal for synchronization with an external logic analyzer or other device are available.
- Eight external logic input lines may be used to trigger an action in the emulator. The status of the external lines is captured in the trace buffer.
- The user may qualify events with an external input SYSIN line.
- A SYSOUT output may be used to stimulate an action in the target system based on a recognized event.

FEATURES

Easy To Use

For ease of use and learning, the ICE-196KD/HX emulator can be operated via a command line interface or with Intel's windowed user interface. The command line style (with syntax guide) is compatible with previous emulators, while the windowed interface has the same look and feel as other Intel emulators and software debuggers.

Windows and Pull-Down Menus

Each window presents a different view of the system. Select and move between a COMMAND LINE window, a SOURCE window, a REGISTER window, a TRACE window, a MEMORY window, or a WATCH window (where user variables are displayed). In addition, a CUSTOM window can perform user-defined functions. Within each window, option menus, pop-up fill-in-the-blank forms, and scroll keys control the view. As expected, windows may be added, sized, zoomed to full screen, or removed completely.

Help at Your Fingertips

Both indexed and context sensitive help is available. A *hypertext* capability lets you easily move between help subjects. In addition, a Key Reference Line displays a list of the currently active function keys as well as brief help text for menus and forms.

Source Level Debugging

Source level debugging with Intel's C-96, ASM-96, and PL/M-96 is synergistic with the windowed user interface. For example, simply use a pull-down menu to load the program. Then set a breakpoint at a souce line by pointing to the line of code in the SOURCE window and pressing a function key. Set trace specifications by using a pop-up, fill-in-the-blank form. With the current execution location highlighted, simply press a function key to begin emulation.

Genuine Intel Tools

The ICE-196KD/HX emulator provides the most comprehensive support for Intel's MCS-96 family of microcontrollers. When you trust your component selection to Intel, why trust its emulation to someone else?

Worldwide Service, Support, and Training

To augment its development tools, Intel offers field application engineering expertise, hotline technical support, and on-site service.

Intel also offers software support which includes technical software information, automatic distributions of software and documentation updates, iCOMMENTS publication, remote diagnostic software, and a development tools troubleshooting guide.

Intel's standard 90-day Hardware Support package includes technical hardware information, telephone support, warranty on parts, labor, material, and on-site hardware support.

Intel Development Tools also offers a 30-day, money-back guarantee to customers who are not satisfied after purchasing any Intel development tool.

intel

SPECIFICATIONS

Host Requirements

Emulator requires an IBM PC AT, XT, PS/2 or 100% compatible machine with 640 Kbytes of RAM and a hard disk running DOS 3.3 or 5.0.

Electrical Characteristics

Power supply: 100V–120V or 200V–240V
50 Hz or 60 Hz
5 amps (AC max) @ 120V
2 amps (AC max) @ 240V

Electrical Considerations

The emulator processor's user-pin timings and loading are identical to the 8xC196KD component except as follows:

- Additional pin capacitance (approximate):
  - Target Interface Board (TIB) — 12 pf (30 pf max)
  - pin 32 (P1.7/HOLD#) — 70 pf
  - pin 63 (INST) — 60 pf
  - pin 16 (RESET#) — 325 pf
  - all pins when using adapter with a flexible cable (ex. KADPTCA68PLCC) — 10 pf
- DC loading:

  Pin 1 (V_{CC}) may draw an additional 5 mA (15 mA worst case @ 5.5V) due to power sensing circuitry.

  Sensing circuitry may also draw approximately ±0.1 mA (maximum) DC current from any 8xC196KD output pin.
- AC timings:
  - pin 32 (P1.7/HOLD#) — degraded 1 ns
  - pin 63 (INST) if jumper E5–E6 is installed — degraded 1 ns
  - pin 16 (RESET#) — degraded 15 ns

Target Considerations

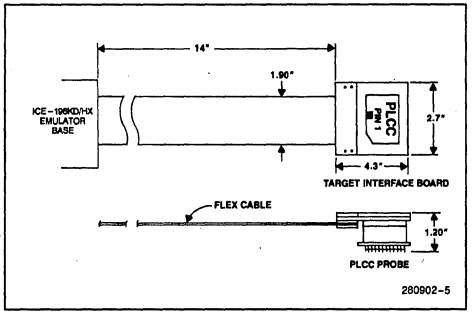
The acceptable target Vcc range is 4.5V to 5.5V and the maximum V_{CC} power consumption of the processor is 1.5W at 20 MHz.

Environmental Characteristics

Operating temperature: 10°C to 40°C

Operating humidity: maximum 85% relative humidity, non-condensing

Processor Module Dimensions



Physical Characteristics

Target Probe

Width: 6.9cm (2.7")
Height: 3.0cm (1.2")
Length: 11.0cm (4.34")

Emulator Chassis		*Power Supply*	
Width:	34cm (13⅜")	Width:	18cm (7½")
Height:	12cm (4½")	Height:	10cm (4")
Depth:	27cm (10⅝")	Depth:	28cm (11")
Weight:	3.2 kg (7 lb.)	Weight:	7kg (15 lb.)

Probe Cable Length: 40 cm (17")

Serial Cable Length: 3.65m (12')

ORDERING INFORMATION

Emulators

Order Code	Description
PICE196KDHXDZ	Complete, fully-featured emulator kit. Contains all required emulator hardware and software to execute stand-alone or in-target. Kit includes: • emulator base chassis and serial cable • external power supply and power cord • Emulation Control Board (ECB II) • ICE Base Board (IBB II) • Break/Trace Board (BTB) • 64 Kbyte Optional Memory Board (OMB) • CLIPSIN and CLIPSOUT pods • Crystal Power Accessory (CPA) (used for diagnostics and stand-alone operation) • Target Interface Board (TIB) fitted with a 68-lead PLCC adapter • PC host software (featuring iWHI: Intel's Windowed Human Interface) • all user documentation

NOTE: host software is delivered on 5¼" high density (1.2 Mb) and 3½" standard (720 Kb) density diskettes

Software Tools

Order Code	Description
D86C96NL	DOS-hosted "CC" cross compiler closely conforming to ANSI C standards, with architectural extensions to support all MCS-96 components. Optimized for real-time embedded applications.
D86PLM96NL	DOS-hosted PL/M cross-compiler. Architectural extensions support all MCS-96 components. Optimized for real-time, embedded applications.
D86ASM96NL	DOS-hosted macro assembler. Supports all MCS-96 components.

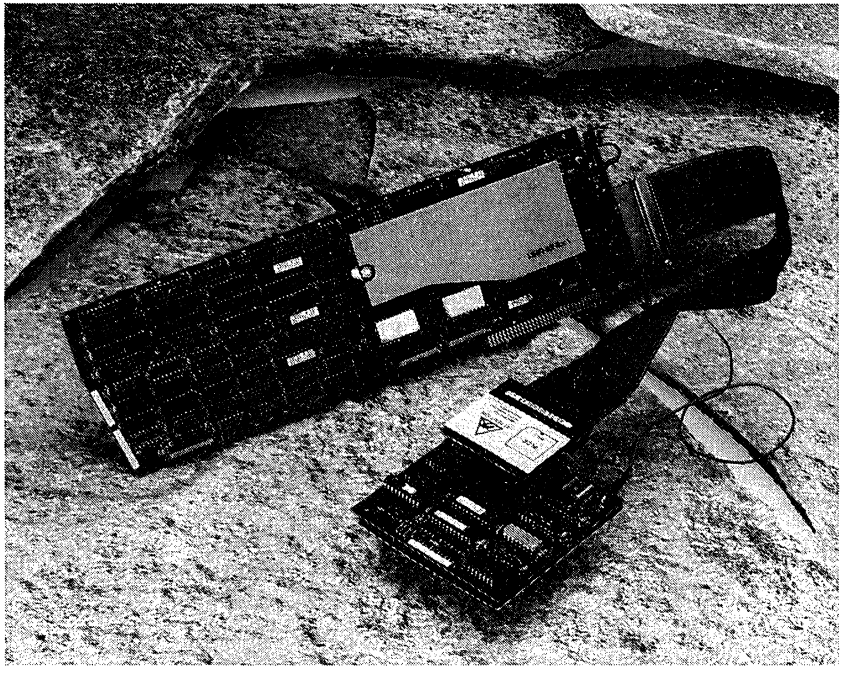
NOTE: All software tool packages include a relocater/linker (RL-96), an object-to-hex converter (OH), a floating point arithmetic library (FPAL-96), and a librarian (LIB-96).

Target Adapters

Order Code	Description
KADPT52PLCC	target: 52-lead PLCC components (socketed)
KADPTCA68PLCC	target: 68-lead PLCC components (socketed)
KADPTONC68PLCC	target: 68-lead PLCC components (surface-mounted 8xC196 components)
KADPTCA68PGA	target: 68-lead PGA components (socketed)
KADPT64SDIP	target: 64-pin "shrink"-DIP components (socketed)
I196ADPTCA80Q	complete probe cable assembly for 80-lead QFP (EIAJ) component for minimal signal degradation
I196CONV80Q	converter for existing PLCC probe to 80-lead QFP (EIAJ) component

intel®

ICE™-196KD/PC IN-CIRCUIT EMULATOR



280917-1

REAL-TIME IN-CIRCUIT EMULATION FOR MCS®-96 MICROCONTROLLERS

Intel's ICE-196KD/PC In-Circuit Emulator is a low-cost, PC-card form factor emulator that delivers real-time, high-level debugging capabilities to help you develop, integrate, and test your MCS-96 microcontroller-based products.

The ICE-196KD/PC emulator supports all component variations offered in the following Intel MCS-96 families:

- 8xC196KD
- 8xC196KC
- 8xC196KB
- 8xC194
- 8xC198

The emulator supports all component types as differentiated by ROM, EPROM, and ROMless; as well as components differentiated by temperature, reliability screenings, package types, and speeds (at up to 16 MHz).

FEATURES

- Real-time, transparent, in-target emulation at speeds up to 16 MHz
- Execution *breaks* (3 specific or 1 range breakpoint)
- Execution *trace* (2048 frame trace buffer)
- 64 Kbytes of zero-waitstate, mappable ICE memory
- Source-level, symbolic debugging
- Stand-alone operation and self-test diagnostics
- Hosted on IBM PC XTs, ATs, PS/2 Model 30s, and 100% compatible machines
- 30 Day money back guarantee

August 1992
Order Number: 280917-003

FEATURES

REAL-TIME EMULATION

The ICE-196KD/PC emulator provides real-time, transparent in-circuit emulation for all components in the 8xC196KD, 8xC196KC, 8xC196KB, 8xC198, and 8xC194 microcontroller families. Running in-circuit, the emulator is able to operate at up to 16 MHz for all target processors.

The ICE-196KD/PC emulator connects to your target via a 16" (40 cm) flex cable. A 68-lead PLCC target adapter is included with the ICE-196KD/PC emulator. Other target adapters supporting other package types are available separately (see "Ordering Information").

MAPPABLE MEMORY

The ICE-196KD/PC emulator contains 64 Kbytes of zero-waitstate ICE memory that can be used to:

- execute and debug programs before target hardware exists
- simulate non-existent or non-working target memory
- overlay target EPROM space (saving time and bother by avoiding the need to program EPROMs).

The ICE memory can be set up as READ-ONLY, WRITE-ONLY, or READ/WRITE.

TRACE BUFFER

The ICE-196KD/PC emulator contains a 2048 frame trace buffer for keeping a history of actual instruction execution. The trace buffer can be conditionally turned off to collect a user specified number of trace frames. Trace information can be displayed as disassembled assembly instructions, or as disassembled assembly instructions intermixed with the original high-level language source code.

BREAKPOINTS

Three execution address breakpoints or one address range breakpoint can be active at any one time. The ICE-196KD/PC emulator allows any number of breakpoints to be defined and activated when needed.

SYMBOLIC SUPPORT AND SOURCE CODE DISPLAY

Full C-96, PL/M-96, and ASM-96 language symbolics (including variable typing and scope), are supported by the ICE-196KD/PC emulator. As an example, source-level, symbolic debugging affords you the convenience of

- setting breakpoints symbolically
  go til line #25
- referencing memory symbolically
  display MY_ARRAY length
  MY_ARRAY_SIZE as characters

You can browse through your original source code, and optionally, the high-level "C" or PL/M source will be displayed when breakpoints are reached.

STANDALONE OPERATION FOR SOFTWARE DEBUGGING

Code can be downloaded for execution on the target system. Or, by using the supplied Crystal Power Accessory (CPA) and mappable ICE memory), code can be downloaded and executed in the emulator itself. This capability allows you to prototype and debug your target software prior to hardware availability.

VERSATILE AND POWERFUL HOST SOFTWARE

The ICE-196KD/PC emulator host software features on-line help, a command line syntax guide, a built-in editor (for creating/editing PROCs, editing source, or viewing the trace buffer), an assembler/disassembler, and a macro command language (for building command procedures).

To augment its development tools, Intel offers field application engineering expertise and hotline technical support.

Intel Development Tools also offers a 30-day, money-back guarantee to customers who are not satisfied after purchasing any Intel development tool.

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SPECIFICATIONS

HOST REQUIREMENTS

The ICE-196KD/PC emulator is hosted on IBM PC XTs, ATs, PS/2 Model 30s, and 100% compatible machines with 640 Kbytes of RAM and a hard disk running DOS 3.3 or 5.0. Though the emulator card plugs into a single 8-bit PC slot, two slots should be reserved for clearance.

ELECTRICAL CONSIDERATIONS

- Additional pin capacitance:
  - all pins: 60 pF
  - all pins when using an adapter with flexible cable (ex: KADPTCA68PLCC): 70 pF
- Cable propagation delay:
  - best case: 5.5 ns
  - worst case: 11.0 ns
- Operating frequency: 3.5 MHz to 16 MHz (CPA runs at 16 MHz only)

TARGET CONSIDERATIONS

The acceptable target V_{CC} range is 4.5V to 5.5V and the maximum V_{cc} power consumption of the processor is 1.5W at 16 MHz.

When entering or exiting emulation, the ICE-196KD/PC emulator will use two bytes on the user stack to store the current instruction pointer.

ENVIRONMENTAL CHARACTERISTICS

Operating temperature: 10°C to 40°C

Operating humidity: maximum 85% relative humidity, non-condensing

ORDERING INFORMATION

order code	description
PICE196KDPC	Complete emulator kit. Contains all required emulator hardware and software to execute stand-alone or in-target. Kit includes: • Emulator controller board (PC-card form factor) • Target Interface Board (TIB) fitted with a 68-lead PLCC adapter • Crystal Power Accessory (CPA) (required for diagnostics and stand-alone operation) • PC host software • All user documentation

NOTE: Host software is delivered on 5-¼" (360 Kb) and 3-½" (720 Kb) diskettes

SOFTWARE TOOLS

order code	description
D86C96NL	DOS-hosted, closely conforming ANSI "C" cross-compiler. Architectural extensions support all MCS-96 components. Optimized for real-time, embedded applications.
D86PLM96NL	DOS-hosted PL/M cross-compiler. Language features allow direct architecture access. Optimized for real-time, embedded applications.
D86ASM96NL	DOS-hosted macro assembler. Supports all MCS-96 components.

NOTE: All software tool packages include a relocater/linker (RL-96), an object-to-hex converter (OH), a floating point arithmetic library (FPAL-96), and a librarian (LIB-96).

TARGET ADAPTERS

order code	description
KADPT52PLCC	target: 52-lead PLCC components (socketed)
KADPTCA68PLCC	target: 68-lead PLCC components (socketed)
KADPTCA68PGA	target: 68-pin PGA components (socketed)
KADPT64SDIP	target: 64-pin "shrink"-DIP components (socketed)
I196ADPTCA80Q	complete probe cable assembly for 80-lead QFP (EIAJ) component for minimal signal degradation
I196CONV80Q	converter for existing PLCC probe to 80-lead QFP (EIAJ) component

MCS®-96 SOFTWARE DEVELOPMENT PACKAGES

280793-1

COMPLETE SOFTWARE DEVELOPMENT SUPPORT FOR THE MCS®-96 FAMILY OF MICROCONTROLLERS

Intel supports application development for the MCS®-96 family of microcontrollers with a complete set of development languages and utilities. These tools include a macro assembler, a C compiler, a PL/M compiler, linker/relocator program, floating point arithmetic library, a librarian utility, and an object-to-hex utility. Develop code in the language(s) you desire, then combine object modules from different languages into a single, fast program.

FEATURES

- Software tools support all members of Intel's MCS®-96 family
- ASM-96 macro assembler for speed critical code
- iC-96 package for structured C language programming, closely conforming to ANSI standards with many hardware specific extensions
- PL/M-96 package for the maintainability and reliability of a high-level language with support for many low-level hardware functions
- Linker/Relocator program for linking modules generated in assembler, PL/M or C and assigning absolute addresses to relocatable code. RL-96 prepares your code for execution in target with a simple, one-step operation
- 32-bit Floating Point Arithmetic Library to reduce your development effort and to allow fast, highly optimized numerics-intensive processing
- Library utility for creating and maintaining software object module libraries
- PROM building utility that converts object modules into standard hexadecimal format for easy download into various PROM programmers
- Hosted on IBM PC XT/AT with PC-DOS 3.0 or above

September 1992
Order Number: 280793-004

FEATURES

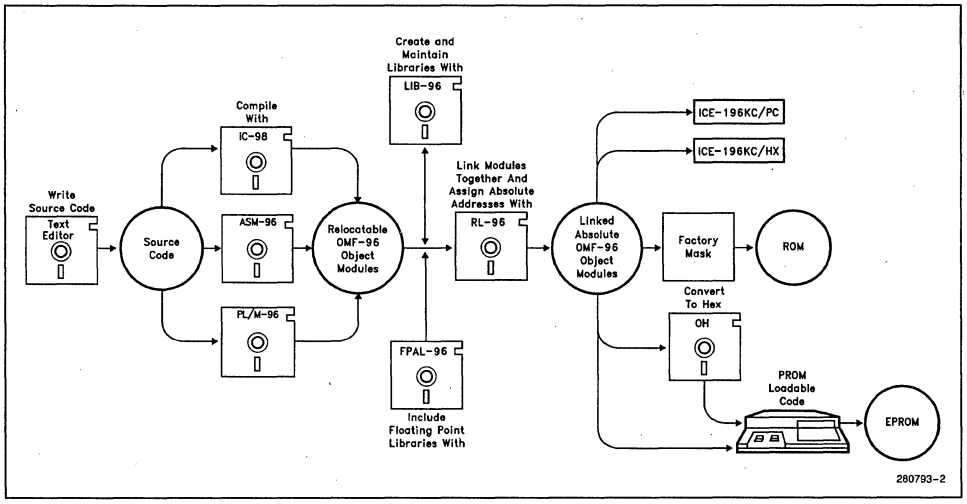

Figure 1. MCS®-96 Application Development Process

ASM-96 MACROASSEMBLER

ASM-96 is the macroassembler for the MCS-96 family of microcontrollers, including the 80C196. ASM-96 translates symbolic assembly language mnemonics into relocatable object code.

The macro facility in ASM-96 saves development and maintenance time, since common code sequences need only be developed once. The assembler also supports symbolic access to the many features of MCS-96 microcontrollers and provides an "include" file with all MCS-96 registers defined.

PL/M-96 SOFTWARE PACKAGE

PL/M-96 is a high-level programming language designed to support the software requirements of advanced 16-bit microcontrollers. The PL/M-96 compiler translates PL/M high-level language statements into 8096 relocatable object code. Major features of the PL/M-96 compiler include:

- **Structured programming.** The PL/M language supports modular and structured programming, making programs easier to understand, maintain, and debug.
- **Built-in functions.** PL/M-96 includes an extensive list of functions, including TYPE CONVERSION functions, STRING manipulations, and functions for interrogating MCS-96 hardware flags.
- **Interrupt handling.** The INTERRUPT attribute allows you to define interrupt handling procedures. The compiler generates code to save and restore the program status word for procedures.
- **Compiler controls.** Compile-time options increase the flexibility of the PL/M-96 compiler. These controls include: optimization, conditional compilation, the inclusion of common PL/M source files from disk, cross-reference of symbols, and optional assembly language code in the listing file.
- **Data types.** PL/M-96 supports seven data types, allowing PL/M-96 to perform three different kinds of arithmetic: signed, unsigned, and floating point.
- **Language compatibility.** PL/M-96 object modules are compatible with all other object modules generated by Intel MCS-96 translators.

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FEATURES

iC-96 SOFTWARE PACKAGE

Intel's iC-96 is a structured programming language designed to support applications for the 16-bit family of MCS-96 microcontrollers. Major features of the iC-96 compiler include:

- **Standard language.** iC-96 closely conforms to ANSI C standards. iC-96 code is fully linkable via RL-96 with both PL/M-96 and ASM-96 modules via an "ALIEN" attribute. This allows programmers to utilize the optimal language for any application.
- **Architecture Support.** iC-96 generates code which is fully optimized for the MCS-96 architecture. iC-96 provides an INTERRUPT attribute, which allows you to define interrupt handlers in C. Library routines allow you to enable and disable interrupts directly from C. A REENTRANT/ NOREENTRANT control included in iC-96 allows the compiler to identify procedures appropriately, thus making efficient use of the large MCS-96 register set.
- **In-Line Assembly.** With the in-line assembly feature of iC-96, you can embed assembly language instructions within your C code for added programming flexibility.
- **Symbolics.** The iC-96 compiler boosts programmer productivity by providing extensive debug information, including symbols. Debug information can be used to debug application code using either the VLSiCE-96 emulator for the MCS-96 architecture or the ICE-196 KxPC/Hx emulators for the 8xC19x components.

RUN-TIME LIBRARY LINKER/LOCATOR

Intel's RL-196 utility is used to link multiple MCS-96 object modules into a single program and then assign absolute addresses to all relocatable addresses in the new program. Modules can be written in ASM-96, PL/M-96, or iC-96. The RL-96 utility also promotes programmer productivity by encouraging modular programming. Because applications can be broken into separate modules, they're easier to design, test and maintain. Standard modules can be reused in different applications, saving software development time.

FPAL-96 FLOATING POINT ARITHMETIC LIBRARY

FPAL-96 is a library of single-precision 32-bit floating point arithmetic functions. These functions are compatible with the IEEE floating point standard for accuracy and reliability and include an error-handler library.

LIB-96

The Intel LIB-96 utility creates and maintains libraries of software object modules. Standard modules can be placed in a library, and linked into your applications programs using RL-96.

OH-96

The OH-96 utility converts Intel OMF-96 object modules into standard hexadecimal format. This allows the code to be loaded directly into a PROM via non-Intel PROM programmers.

SERVICE, SUPPORT, AND TRAINING

Intel augments its MCS-96 architecture family development tools with field application engineering expertise, telephone hot-line support, and software and hardware maintenance contracts. This full line of services will ensure your design success.

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ORDERING INFORMATION

D86ASM96NL*	96 Assembler for PC XT or AT system (or compatible), running DOS 3.0 or higher
D86PLM96NL*	PL/M-96 Software Package for PC XT or AT system (or compatible), running DOS 3.0 or higher
D86C96NL*	iC-96 Software Package for PC XT or AT system (or compatible), running DOS 3.0 or higher

*Also includes: Relocator/Linker, Object-to-hex Converter, Floating Point, Arithmetic Library, and Librarian

*Ap*BUILDER INTERACTIVE APPLICATION PROGRAMMING PACKAGE

272198-1

Become An Architectural Wizard Instantly

A windows-based software tool that is a learning vehicle, reference guide and programmer all in one. *Ap*BUILDER is a powerful new design tool for the embedded control applications programmer, created specifically to speed up your learning curve and reduce your total design time no matter what level of processor experience you have. *Ap*BUILDER software provides you with peripheral design capabilities, an interactive instruction and register editor, a click-on highlight feature and a hypertext* utility for hardware reference users' manuals.

The *Ap*BUILDER programming package saves you time and energy by providing a simple mechanism for configuring an embedded processor. And it's flexible too. There's a design section that allows you to select the functionality of each integrated peripheral. If you want to program a specific register, *Ap*BUILDER software provides the on-line capability of picking and choosing the bits you want to set within the register itself. In both cases, *Ap*BUILDER software converts the user's selection into useable assembly language code.

*Ap*BUILDER's block diagram screens give a graphic overview of the unique features of a selected device. With the ability to view multiple products quickly and easily, *Ap*BUILDER software becomes a valuable tool in helping you choose which processor is best suited for your application.

Multiple hypertext windowed utilities are organized throughout the *Ap*BUILDER software, enabling you to access an extraordinary amount of data quickly and easily. With the click of a button you have access to hardware reference manuals, data sheets, fact sheets, commonly asked questions and general help information.

*Hypertext: The linking of related information. By selecting a highlighted word in a body of text, information about that word is retrieved and displayed.

October 1992
Order Number: 272198-001

*Ap*BUILDER INTERACTIVE APPLICATION PROGRAMMING PACKAGE

Product Highlights

- On-line Peripheral Programming
- Hypertext reference documentation
- Windows screens for ease of use
- Supports 186 and MCS®-96 families

Features

Multi-Level Programming Capabilities

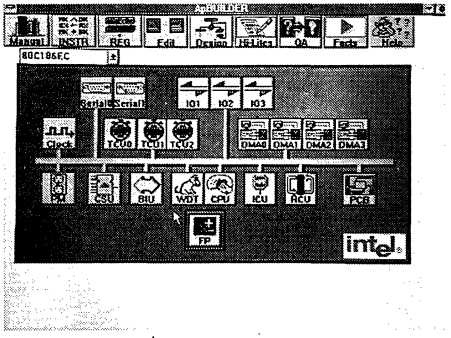
- Design section generates initialization code for integrated peripherals based on system functionality
- Simple on-screen templates allow for register programming
- Instruction editor to confirm assembly instruction syntax, giving options for possible source and destination locations
- Translates and converts all requirements to source code

Programming Modules Linked to Reference Documentation for Specific Functions

- Keyed summary lists provide extensive search and retrieval capabilities
- Help references go several layers deep within the on-line reference documentation
- Features like browse, forward, back and previous search provide easy movement through megabytes of documentation

Click-On Highlight

- View product features, data sheets, fact sheets and answers to commonly asked questions
- Unique icons make retrieving valuable product information simple and straightforward



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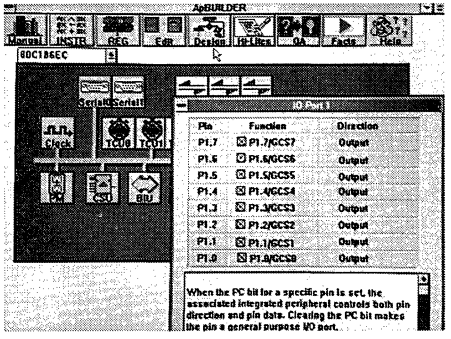
***Ap*BUILDER Menu**



272198-4

Programs I/O Ports

Benefits

- Reduction of total design time by removing the programming hassle associated with the configuration of an embedded processor
- Flexibility to program a single register or a series of peripherals
- Conversion of high level peripheral configurations to useable low level assembly language code
- Graphic overview of the unique features of a selected device
- Hypertext help available quickly and easily with the click of a button
- Enables you to select the best processor for your application

*Ap*BUILDER INTERACTIVE APPLICATION PROGRAMMING PACKAGE

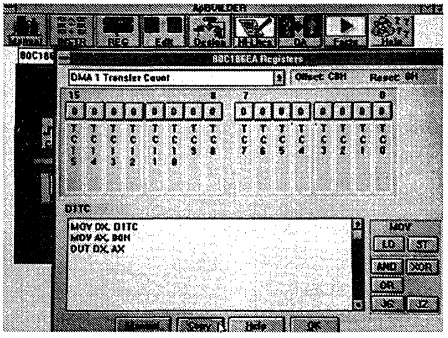
Summary

- Provides a simple and straightforward mechanism for constructing the building blocks necessary for embedded processor applications
- Enables you to focus on your application needs rather than wasting time programming bit by bit

System Requirements

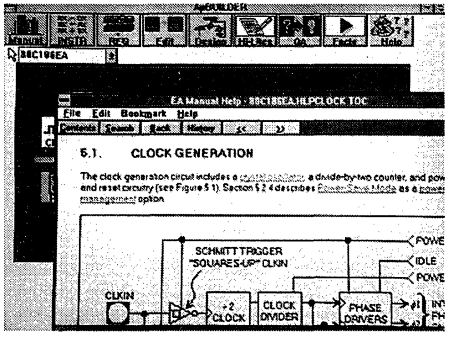
Windows 3.0, IBM compatible 386 PC or above, VGA monitor, 16M of hard disk, 1.44M floppy drive, 4M memory and a mouse.

The *Ap*Builder may be ordered through the Intel literature department Order No. 272216.



272198-3

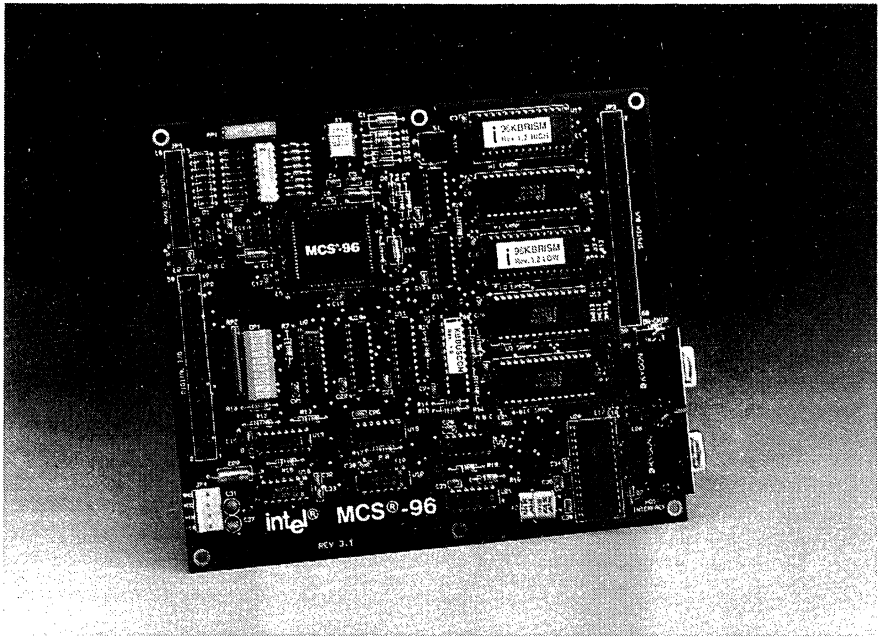
Programs a DMA Register



272198-5

Hypertext Reference Data

EV80C196KX EVALUATION BOARDS



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LOW COST CODE EVALUATION TOOL

The EV80C196KX (MCS®-96) family consists of the EV8097BH, EV80C196KB, EV80C196KC, and the EV80C196KD evaluation boards. They provide a hardware environment for code execution and software debugging at a relatively low cost. Each board features an advanced microcontroller that is a member of the industry standard MCS-96 family. The boards allow the user to take full advantage of the power of the MCS-96. Their memory (ROMsim) can be reconfigured to match the user's planned memory system, allowing for exact analysis of code execution speeds in a particular application.

Popular features such as a symbolic single line assembler/disassembler, single-step program execution, and sixteen software breakpoints are standard. Intel provides a complete code development environment using assembler (ASM-96) as well as high-level languages such as Intel's iC-96 or PL/M-96 to accelerate development schedules.

Each evaluation board is hosted on an IBM PC** or BIOS-compatible clone, already a standard development solution in most of today's engineering environments. The source code for the on-board monitor (written in ASM-96) is public domain. The program is about 1K, and can be easily modified to be included in the user's target hardware. In this way, the provided PC host software can be used throughout the development phase.

MCS is a registered trademark of Intel Corporation.
**IBM PC, XT, AT are registered trademarks of International Business Machines Corporation.

October 1992
Order Number: 272222-001

EV80C196KX EVALUATION BOARDS

FEATURES

- Zero Wait-State Full Speed Execution
  - — 12 MHz Execution Speed for EV80C196KB
  - — 12 MHz Execution Speed for EV8097BH
  - — 16 MHz Execution Speed for EV80C196KC
  - — 20 MHz Execution Speed for EV80C196KD
- 24K Bytes of ROMsim
- Flexible Wait-State, Buswidth, Chip-Select Controller
- Total CMOS, Low Power Board (EV8097BH features NMOS)
- Concurrent Interrogation of Memory and Registers
- Sixteen Software Breakpoints
- Two Single Step Modes
- High-Level Language Support
- Symbolic Debug
- RS-232-C Communication Link

FULL SPEED EXECUTION

The MCS-96 evaluation board executes the user's code from on board ROMsim at full speed with zero wait-states. By changing crystals, slower execution speed can be evaluated. The board's host interface timing is not affected by this crystal change.

24K BYTES OF ROMsim

The boards come with 24K bytes of SRAM to be used as ROMsim for the user's code and as data memory if needed. 16K bytes of this memory are configured as sixteen bits wide, and 8K bytes are configured as eight bits wide. The user can therefore evaluate the speed of the part executing from either buswidth.

FLEXIBLE MEMORY DECODING

By changing the Programmable Logic Device (PLD) on the board, the memory on the board can be made to look like the memory system planned for the user's hardware application. The PLD controls the buswidth and the chip-select inputs on the board. It also controls the number of wait states generated during a memory cycle. These features can all be selected with 256 byte boundaries of resolution.

TOTALLY CMOS BOARDS

Built totally with CMOS components (except the 8097BH which features NMOS), power consumption is very low, requiring 5V at only 300 mA. If the on board LEDs are disabled, the current drops to only 180 mA. The boards also require ±12V at 15 mA.

CONCURRENT INTERROGATION OF MEMORY AND REGISTERS

The monitor allows the user to read and modify internal registers and external memory while the user's code is running in the board.

SIXTEEN SOFTWARE BREAKPOINTS

There are sixteen breakpoints available which automatically substitute a TRAP instruction for a user's instruction at the breakpoint location. The substitution occurs when execution is started. If the code is halted or a breakpoint is reached, the user's code is restored in the ROMsim.

TWO STEP MODES

There are two single-step modes available. The first stepping mode locks out all interrupts which might occur during the step. The second mode enables interrupts, and treats subroutine calls and interrupt routines as one indivisible instruction.

HIGH LEVEL LANGUAGE SUPPORT

The host software for the boards can load absolute object code generated by ASM-96, iC-96, PL/M-96 or RL-96, all of which are available from Intel.

SYMBOLIC DEBUG

The host has a Single Line Assembler, and a Disassembler, which recognize symbolics generated by Intel software tools.

RS-232-C COMMUNICATION LINK

The boards communicate with the host using an Intel 82510 UART provided on board. This frees the on-chip UART for the user's application.

PERSONAL COMPUTER REQUIREMENTS

The Evaluation Boards are hosted on an IBM PC, XT, AT** or BIOS compatible clone. The PC must meet the following minimum requirements:

- 512K Bytes of Memory
- One 360K Byte Floppy Disk Drive
- PC DOS** 3.1 or Later
- A Serial Port (COM1 or COM2) at 9600 Baud
- ASM-96, iC-96 or PL/M-96
- A text editor such as AEDIT

EV80C196KX EVALUATION BOARDS

GETTING STARTED

POWERING UP THE BOARD

Power (+5V, ±12V) must be connected to JP4 as shown on the board's silkscreen next to JP4 and in Figure 5. Included with the board is a packet containing a Molex connector and crimp terminals for your convenience.

Power supply requirements for the MCS-96 Evaluation Boards are as follows:

+5 V_{DC} ±5% @ 280 mA (180 mA if LEDs are disabled by removing jumper shunt E6)

+12 V_{DC} ±20% @ 15 mA

−12 V_{DC} ±20% @ 15 mA

Upon power-up (or after a reset) the board goes through initialization. When completed, a continuous shifting-pattern is displayed on the Port 1 LEDs.

CONNECTING TO THE PC

Once users have applied power to the board, they need to connect P1 to a PC serial port. P1 is configured to interface pin-to-pin with a standard nine-pin AT-type serial connector. Users should make certain that they use a cable providing all nine signals, as they are all needed for proper operation of the host interface.

STARTING THE HOST SOFTWARE

After connecting power and a host PC, the host interface can be invoked. Install the disk in drive A of the system. At the DOS prompt type:

A:ECM96<CR>

After a moment, the PC sould display the iECM96 monitor screen.

NOTE: If users have a 25-pin serial port it will be necessary to make a 25-pin to 9-pin adaptor (see Users Manual for details).

HARDWARE OVERVIEW

The Evaluation Board is delivered with a MCS-96 microcontroller, 8 K-words and 8K bytes of user code/data memory, a UART for host communications and analog-input filtering with a precision voltage reference. Also included, is programmable chip-select, bus-width and wait-state-counter logic which allows you to custom tailor the board to look like your own system. The board's physical dimensions are 6½" x 7¾" with an overall height of ¾". There are six main sections to the board: Processor, Memory, Host Interface, Digital I/O, Analog Inputs and Decoding.

MEMORY

There are five 28-in memory sockets provided on each board: U1, U6, U8, U13, U14. The sockets are designed to support byte-wide, JEDEC-pinout, memory devices of various types and sizes, i.e., 8K x 8 SRAM or 16K x 8 EPROM. U1 and U8, U6 and U13 are connected as two 16-bit memory banks and U14 is connected as an 8-bit memory bank.

HOST INTERFACE

The PC host interface is accomplished with the 82510 UART (U20) connected to P1 via RS-232 drivers. The UART resides in the address range 1E00H–1EFFH. Therefore, register 0 in the UART would be at address 1E00H of the MCS-96 microcontroller, register 1 would be at 1E01H, register 2 would be at 1E02H, etc., up to register 7 at 1E07H. The registers will repeat again with register 0 at 1E08H due to the limited decoding granularity of the EPLD. Pin 12 of the UART, OUT1#, is used to tell the PC host when the MCS-96 microcontroller is executing user code by a true level on the Ring Indicator input of the host serial port.

DIGITAL I/O

With the exception of the NMI input, which is used by the Host Interface, all Digital I/O functions of the MCS-96 microcontrollers are available to users. There are eight LEDs on-board along with buffer/drivers which allow users to quickly observe the state of Port 1, HS0.0 and P2.5/PWM. The TxD and RxD pins of the MCS-96 microcontroller (Port 2.0 and Port 2.1) are connected to RS-232 buffer/drivers, which are connected to P2. All of the I/O signals are available on JP2.

ANALOG INPUTS

The Port 0 inputs of the MCS-96 microcontroller double as both digital and analog inputs. Each board includes circuitry to make the analog inputs easier to use. A precision voltage source for V_{REF} is provided on board (U3 and U4) which can be carefully adjusted by trimming RP1. Also, jumper shunt E4 allows V_{REF} to be connected to V_{CC} instead of the output of U3. By removing E4 entirely, an off board reference can be connected to JP1. By removing jumper shunt E2, ANGND can be isolated from V_{SS}. Protective clamping diodes are installed on each channel. RC networks are provided in sockets (to allow users to change the input impedance to match their application) on all of the analog input channels. If Port 0 is to be used as a digital input, it is recommended that the capacitors be removed, and the resistors replaced with wires. For additional connection information, refer to Figure 1. The ground and power planes beneath the analog circuitry (D1, D2, R3, C2, U3, U4, JP1 and the analog connections on the 80C196KX board) are isolated from the digital power and ground planes of the board to keep noise from the analog inputs.

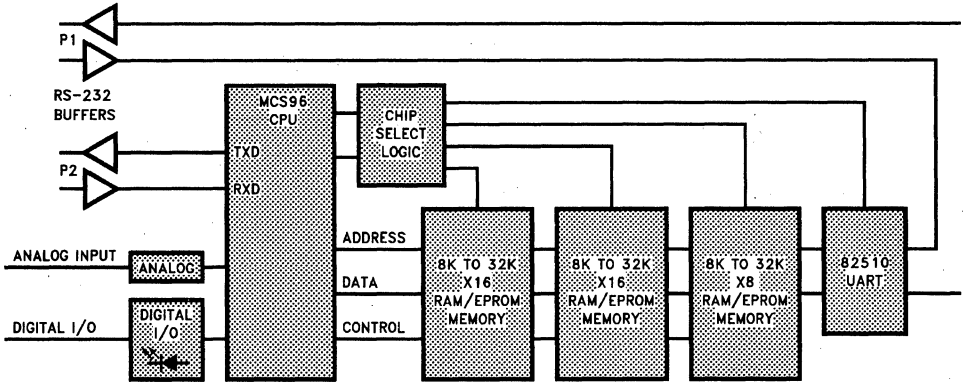

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Figure 1. Block Diagram of the EV80C196KX Board

Bank No.	Even Bytes I.C.	Odd Bytes I.C.	Enable Signal	Memory Type
0	U8	U1	CE0	8K x 16-Bit Monitor EPROM from 0–FFH and 1D00H–1DFFH
1	U13	U6	CE1	8K x 16-Bit ROMsim/RAM from 2000H–5FFFH
2	U14	U14	CE2	8K x 8-Bit ROMsim/RAM from 6000H–7FFFH

DECODING

The decoding logic on each board serves three purposes; to provide Chip-Enable signals to memory and peripheral devices, to select the bus width for the device(s) being accessed and to provide wait states for slow devices. This section is provided should users need to modify the memory configuration of the board. It is not necessary to understand this section for normal usage of the board.

The heart of the decoding logic is U12, a 24-pin 5AC312 Intel EPLD or a C22V10 programmable logic array which is socketed to allow easy changes. For the sake of convenience it will be referred to as "the EPLD" throughout this text. The EPLD uses latched addresses A8–A15 along the CLKOUT, HLDA#, RESET# and STALE (Stretched ALE) from the MCS-96 microcontroller as decode inputs.

There are 4 enable outputs from the EPLD, all of which are low-level true, however only one should be true at a time to avoid bus contention. They are decoded from the address lines, and an internally-latched signal called MAP. MAP is cleared when the RESET# input is true, and set when the Monitor EPROMs are accessed in the address range 1D00H–1DFFH. MAP will always be set when the board is in the USER mode.

The BUSWIDTH output of the EPLD, pin 16, is fed into the buswidth pin of the MCS-96 microcontroller. Therefore, it is driven low for accesses to 8-bit memory and high for accesses to 16-bit memory. As shipped, it goes low simultaneously with CE2 or CS510 as these are the only areas of memory mapped as 8-bit.

Programmed into the EPLD is a 3-bit wait-state machine clocked by the rising edge of CLKOUT from the MCS-96 microcontroller. The transition sequence of the wait-state machine is controlled by the current state of the machine and inputs to the EPLD.

CE0 Pin 21	(Address Range 2000H–27FF and Not Map) or Address Range 0H–FFH or Address Range 1D00H–1DFFH	Enables Memory in U1 and U8 (Monitor EPROM as Shipped)
CE1 Pin 22	(Address Range 2000H–27FFH and Map) or Address Range 2800H–5FFFH	Enables Memory in U6 and U13 (User 16-Bit ROMsim/RAM as Shipped)
CE2 Pin 15	(Address Range 6000H–7FFFH)	Enables Memory in U14 (User 8-Bit ROMsim/RAM as Shipped)
CS510 Pin 14	(Address Range 1E00H–1EFFH)	Enables U20, the 82510 UART, Which is Used for Host Communications

Memory Type	Wait States	Enable Signal	Memory Region in User Mode
ROMsim/RAM	0	CE1	2000H–5FFFH
ROMsim/RAM	0	CE2	6000H–7FFFH
Monitor EPROM	1	CE0	0000H–00FFH, 1D00H–1DFFH
82510 UART	2	CS510	1E00H–1EFFH
Unimplemented	0	N/A	0100H–1CFFH, C000H–FFFFH
Unimplemented	1	N/A	8000H–BFFFH

JP1 Analog Input Connector
2x25 Pin Molex 39-51-2604 or Equiv.

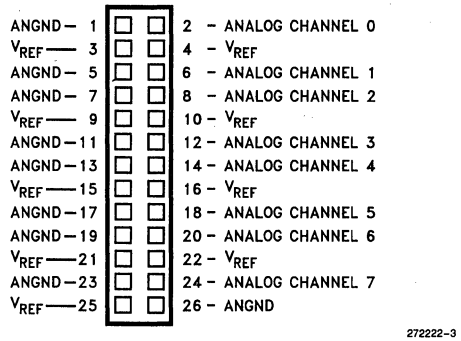


Figure 2

JP2 I/O Expansion Connector
2x25 Pin Molex 39-51-5004 or Equiv.

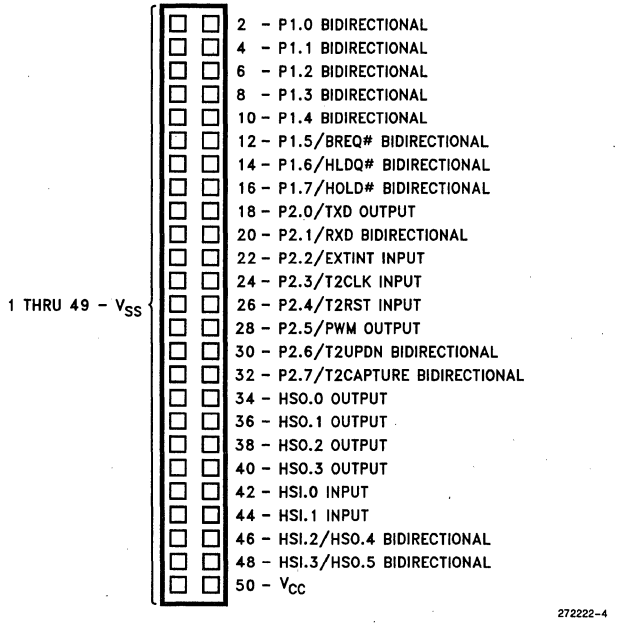


Figure 3

JP3 Memory-I/O Expansion Connector
2x30 Pin Molex 39-51-6004 or Equiv.

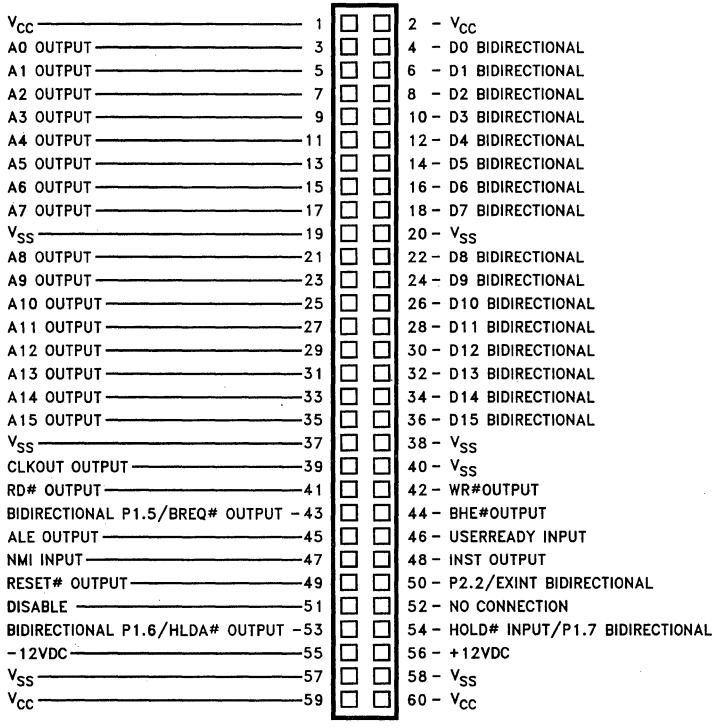


Figure 4

JP4 Power Supply Connector
4 Pin Molex 26-03-3041 or Equiv.

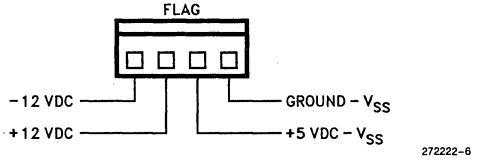
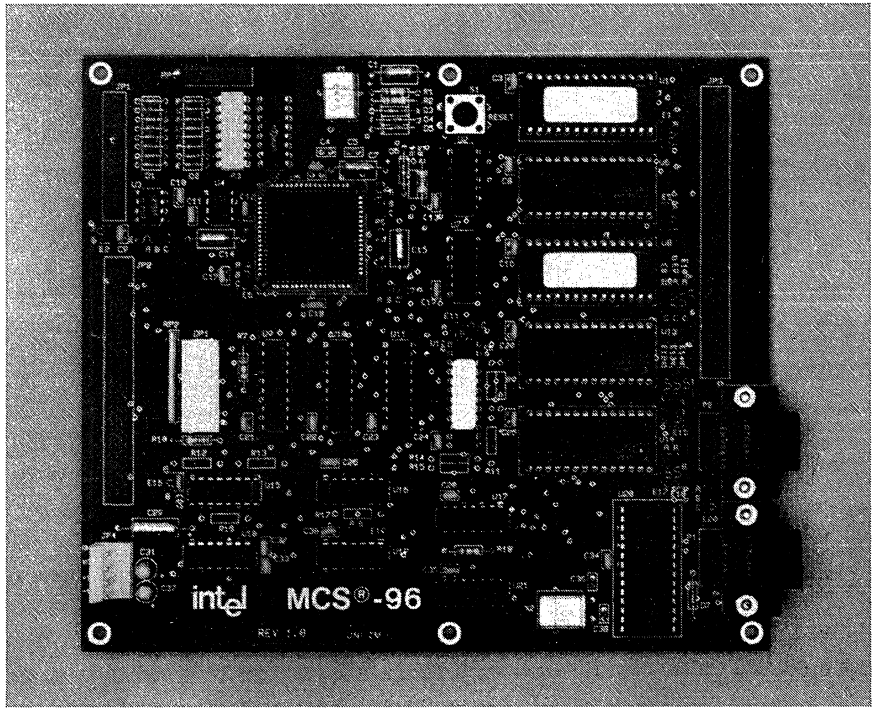


Figure 5

These evaluation boards may be purchased through your local Intel distributor or Intel sales office. Call 1-800-468-8118 for more information (U.S. and Canada).

EV80C196KR EVALUATION BOARD



272078-1

Low Cost Code Evaluation Tool

Intel's EV80C196KR evaluation board provides a hardware environment for code execution and software debugging at a relatively low cost. The board features the 80C196KR advanced, CHMOS*, single chip, 16-bit microcontroller, the newest member of the industry standard MCS®-96 family. The board allows the user to take full advantage of the power of the MCS-96. The EV80C196KR provides zero wait state, 16 MHz execution of a user's code. Plus its memory (ROMsim) can be reconfigured to match the user's planned memory system, allowing for exact analysis of code execution speeds in a particular application.

Popular features such as a symbolic debug, single line assembler/disassembler, single-step program execution and sixteen software breakpoints are standard on the EV80C196KR. Intel provides a complete code development environment using assembly language (ASM-96) as well as Intel's high-level languages such as iC-96 or PL/M-96 to accelerate development schedules.

The evaluation board is hosted on an IBM PC** or BIOS-compatible clone, already a standard development solution in most of today's engineering environments. The source code for the on-board monitor (written in ASM-96) is public domain. The program is about 1 Kbyte and can be easily modified to be included in the user's target hardware. In this way, the provided PC host software can be used throughout the development phase.

*CHMOS is a patented Intel process.
**IBM PC, XT, AT and DOS are registered trademarks of International Business Machines Corporation.

October 1991
Order Number: 272078-001

EV80C196KR EVALUATION BOARD

EV80C196KR Features

- Zero Wait State 16 MHz Execution Speed
- 24 Kbytes of ROMsim
- Flexible Wait State, Buswidth, Chip-Select Controller
- Totally CMOS, Low Power Board
- Concurrent Interrogation of Memory and Registers
- Sixteen Software Breakpoints
- Two Single-Step Modes
- High-Level Language Support
- Symbolic Debug
- Single Line Assembler/Disassembler
- RS-232C Communications Link

Full Speed Execution

The EV80C196KR executes the user's code from on-board ROMsim at 16 MHz with zero wait states. By changing crystals on the 80C196KR, any slower execution speed can be evaluated. The board's host interface timing is not effected by this crystal change.

24 Kbytes of ROMsim

The board comes with 24 Kbytes of SRAM to be used as ROMsim for the user's application code and as data memory if needed. 16 Kbytes of this memory are configured as sixteen-bit wide and 8 Kbytes are configured as eight-bit wide. The user can therefore evaluate the speed of the part executing from either bus width.

Flexible Memory Decoding

By changing the Programmable Logic Device (PLD) on the board, the memory can be made to look like the memory system planned for the user's hardware application. The PLD controls the bus width of the 80C196KR and the chip-select inputs on the board with 256-byte boundaries of resolution. It also controls the number of wait states (zero to four) generated by the 80C196KR during a memory cycle.

Totally CMOS Board

The EV80C196KR board is built totally with CMOS components. Its power consumption is therefore very low, requiring 5 volts at only 300 mA. If the board LEDs are disabled, the current drops to only 165 mA. The board also requires ±12 volts at 15 mA.

Concurrent Interrogation of Memory and Registers

The monitor for the EV80C196KR allows the user to read and modify internal registers and external memory while the user's code is running on the board.

Sixteen Software Breakpoints

There are sixteen breakpoints available which automatically substitute a TRAP instruction at the breakpoint location. The substitution occurs when execution is started. If the code is halted or a breakpoint is reached, the user's code is restored to the ROMsim.

Two Steps Modes

There are two single-step modes available. The first stepping mode locks out all interrupts which might occur during the step. The second mode enables interrupts, and treats subroutine calls and interrupt routines as indivisible instructions.

High-Level Language Support

The host software for the EV80C196KR board is able to load absolute object code generated by ASM-96, iC-96, PL/M-96 or RL-96, all of which are available from Intel.

Symbolic Debug

The host has a single-line assembler, and a disassembler, that recognize symbolics generated by Intel software tools.

RS-232C Communications Link

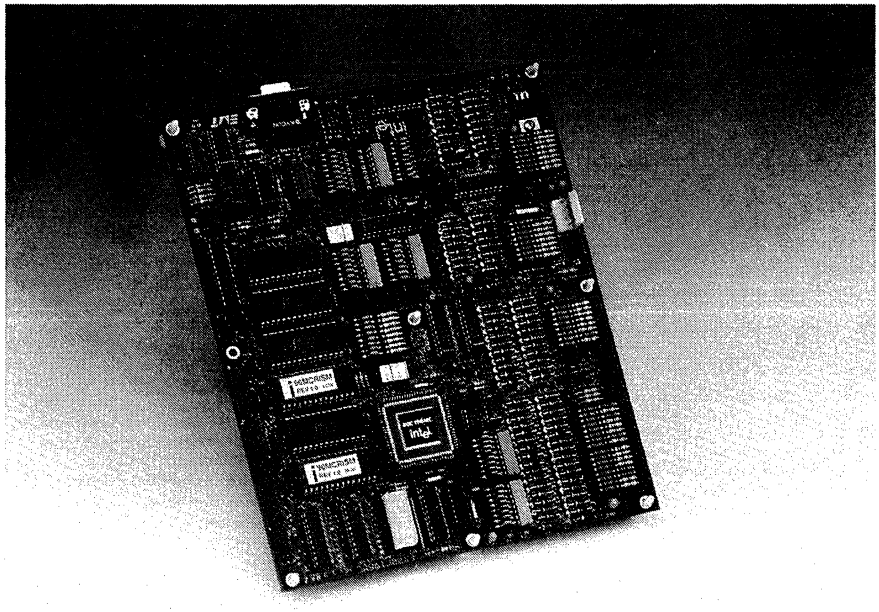
The EV80C196KR communicates with the host using an Intel 82510 UART provided on the board. This frees the on-chip UART of the 80C196KR for the user's application.

Personal Computer Requirements

The EV80C196KR Evaluation Board is hosted on an IBM PC, XT, AT** or BIOS-compatible clone. The PC must meet the following minimum requirements.

- 512 Kbytes of Memory
- One 360 Kbyte Floppy Disk Drive
- PC DOS** Version 3.1 or later
- A Serial Port (COM1 or COM2) at 9600 Baud
- ASM-96 or PL/M-96
- A text editor such as AEDIT

EV80C196MC EVALUATION BOARD



272215-01

LOW COST CODE EVALUATION TOOL

Intel's EV80C196 evaluation board provides a hardware environment for code execution and software debugging at a relatively low cost. The board features the 80C196MC advanced, CHMOS*, 16-bit microcontroller, the newest member of the industry standard MCS®-96 family. The board allows the user to take full advantage of the power of the MCS-96. The EV80C196MC provides zero wait-state, 16 MHz execution of a user's code. Plus, its memory (ROMsim) can be reconfigured to match the user's planned memory system, allowing for exact analysis of code execution speeds in a particular application.

Popular features such as a symbolic single line assembler/disassembler, single-step program execution, and sixteen software breakpoints are standard on the EV80C196MC. Intel provides a complete code development environment using assembler (ASM-96) as well as high-level languages such as Intel's iC-96 or PL/M-96 to accelerate development schedules.

The evaluation board is hosted on an IBM PC** or BIOS-compatible clone, already a standard development solution in most of today's engineering environments. The source code for the on-board monitor (written in ASM-96) is public domain. The program is about 1K, and can be easily modified to be included in the user's target hardware. In this way, the provided PC host software can be used throughout the development phase.

*CHMOS is a patented Intel process.
**EBM PC, XT, AT and DOS are registered trademarks of International Business Machines Corporation.

October 1992
Order Number: 272215-001

FEATURES

EV80C196MC FEATURES

- Zero Wait-State 16 MHz Exection Speed
- 24 Kbytes of ROMsim
- Flexible Wait-State, Buswidth, Chip Select Controller
- Totally CMOS, Low Power Board
- Concurrent Interrogation of Memory and Registers
- Sixteen Software Breakpoints
- Two Single-Step Modes
- High-Level Language Support
- Symbolic Debug
- RS-232-C Communication Link

FULL SPEED EXECUTION

The EV80C196MC executes the user's code from on-board ROMsim at 16 MHz with zero wait-states. By changing crystals on the 80C196MC, any slower execution speed can be evaluated. The board's host inteface timing is not affected by this crystal change.

24 Kbytes OF ROMsim

The board comes with 24 Kbytes of SRAM to be used as ROMsim for the user's code and as data memory if needed. 16 Kbytes of this memory are configured as sixteen bits wide, and 8 Kbytes are configured as eight bits wide. The user can therefore evaluate the speed of the part executing from either buswidth.

FLEXIBLE MEMORY DECODING

By changing the Programmable Logic Device (PLD) on the board, the memory on the board can be made to look like the memory system planned for the user's hardware application. The PLD controls the buswidth of the 80C196MC and the chip-select inputs on the board. It also controls the number of wait-states (zero to three) generated by the 80C196MC during a memory cycle. These features can all be selected with 256 byte boundaries of resolution.

TOTALLY CMOS BOARD

The EV80C196MC board is built totally with CMOS components. Its power consumption is therefore very low, requiring 5V at only 300 mA. If the on-board LEDs are disabled, the current drops to only 170 mA. The board also requires ±12V.

CONCURRENT INTERROGATION OF MEMORY AND REGISTERS

The monitor for the EV80C196MC allows the user to read and modify internal registers and external memory while the user's code is running in the board.

SIXTEEN SOFTWARE BREAKPOINTS

There are sixteen breakpoints available which automatically substitute a TRAP instruction for a user's instruction at the breakpoint location. The substitution occurs when execution is started. If the code is halted or a breakpoint is reached, the user's code is restored in the ROMsim.

TWO STEP MODES

There are two single-step modes available. The first stepping mode locks out all interrupts which might occur during the step. The second mode enables interrupts, and treats subroutine calls and interrupt routines as one indivisible instruction.

HIGH-LEVEL LANGUAGE SUPPORT

The host software for the EV80C196MC board is able to load absolute object code generated by ASM-96, iC-96, PL/M-96 or RL-96, all of which are available from Intel.

FEATURES

SYMBOLIC DEBUG

The host has a Single Line Assembler, and a Disassembler, which recognize symbolics generated by Intel software tools.

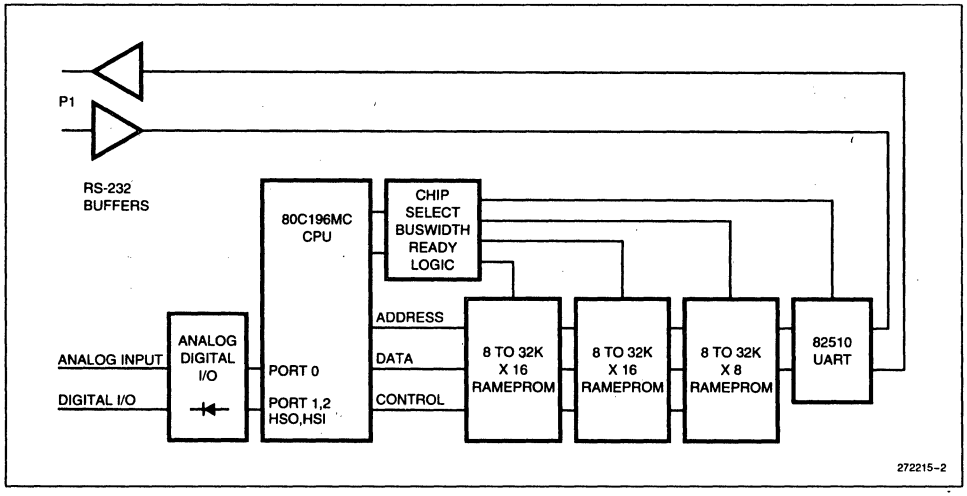
RS-232-C COMMUNICATION LINK

The EV80C196MC communicates with the host using an Intel 82510 UART provided on board.

PERSONAL COMPUTER REQUIREMENTS

The EV80C196MC Evaluation Board is hosted on an IBM PC, XT, AT** or BIOS compatible clone. The PC must meet the following minimum requirements:

- 512 Kbytes of Memory
- One 360 Kbyte Floppy Disk Drive
- PC DOS** 3.1 or Later
- A Serial Port (COM1 or COM2) at 9600 Baud
- ASM-96, iC-96 or PL/M-96
- A text editor such as AEDIT



Block Diagram of the 80C196MC Board

MCS®-51 and MCS-96 Packaging Information

23

intel®

October 1991

MCS®-51 and MCS®-96 Packaging Information

23

Order Number: 272118-001

MCS-51 and MCS-96 Packaging Information

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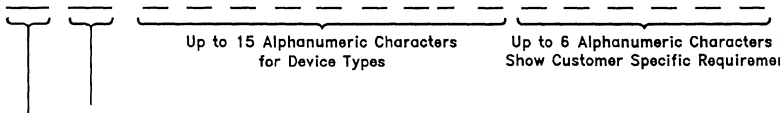
44-Lead QFP	23-6
48-Lead Plastic DIP	23-7
48-Lead Ceramic DIP	23-8
64-Lead Plastic Shrink DIP	23-9
68-Lead LCC	23-10
68-Lead PGA	23-11
80-Lead QFP	23-12
100-Lead PQFP	23-13
44/52/68/84-Lead PLCC	23-14

Intel Product Identification Codes



Package Type

A	–	Ceramic Pin Grid Array
C	–	Ceramic Dual In-Line Package
D	–	Cerdip Dual In-Line Package
KU	–	Plastic Quad Flatpack Package, Fine Pitch, Die Up
N	–	Plastic Leaded Chip Carrier
P	–	Plastic Dual In-Line Package
R	–	Ceramic Leadless Chip Carrier
S	–	Quad Flatpack Package
U	–	Plastic Dual In-Line Package (Shrink)

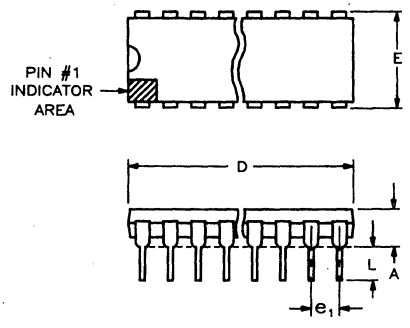
L	–	Indicates extended operating temperature range (−40°C to +85°C) express product with 160 ± 8 hrs. dynamic burn-in.
Q	–	Indicates commercial temperature range (0°C to 70°C) express product with 160 ± 8 hrs. dynamic burn-in
T	–	Indicates extended temperature range (−40°C to +85°C) express product without burn-in.

272118-12

EXAMPLES:

N80C196KR	PLCC, 16 MHz, Commercial Temperature Range
LN87C54	PLCC, 12 MHz, Extended Temperature Range (Express)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE (TYPE N)

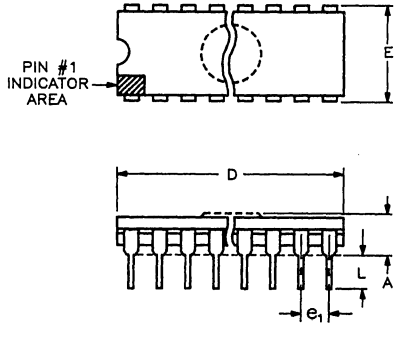


272118-1

Family: Plastic Dual In-Line Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	5	0.2
D	53	2.1
E	16	0.6
e_1	2.5	0.10
L	3	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

40-LEAD CERDIP DUAL IN-LINE PACKAGE (TYPE D)

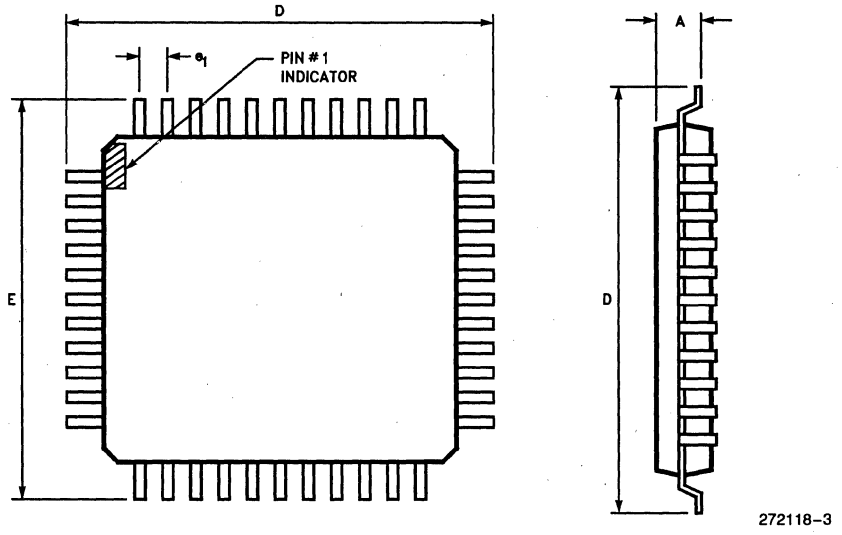


272118-2

Family: Cerdip Dual In-Line Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	5.8	0.2
D	53	2.1
E	16	0.6
e_1	2.5	0.10
L	3	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

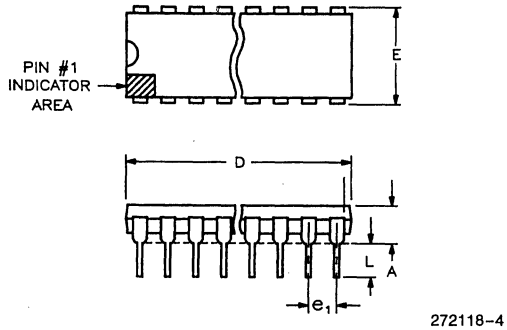
44-LEAD QUAD FLATPACK PACKAGE (TYPE S) VARIATION: SQUARE



Family: Quad Flatpack Package	
Symbol	**Millimeters Approx***
A	3
D	13
E	13
e_1	0.8

*For exact dimensions consult the Packaging Handbook (#240800).

48-LEAD PLASTIC DUAL IN-LINE PACKAGE (TYPE N)

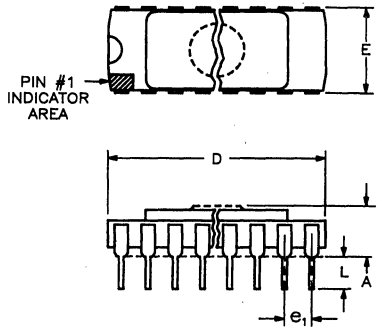


272118-4

Family: Plastic Dual In-Line Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	5	0.2
D	62	2.5
E	16	0.6
e_1	2.5	0.1
L	3	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

48-LEAD CERAMIC DUAL IN-LINE PACKAGE (TYPE C)

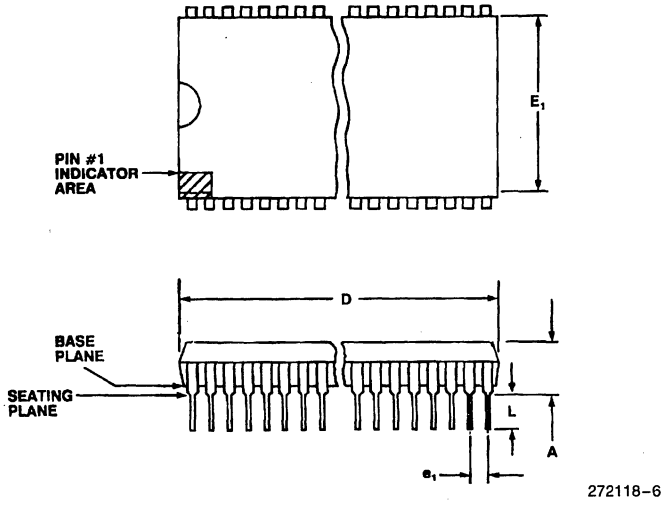


272118-5

Family: Ceramic Side Braze Dual In-Line		
Symbol	**Millimeters Approx***	**Inches Approx***
A	6(1)	0.2(1)
A	7(2)	0.3(2)
D	62	2.5
E	16	0.6
e_1	2.5	0.1
L	3	0.1

NOTES:
1. Solid LID
2. EPROM LID
*For exact dimensions consult the Packaging Handbook (#240800).

64-LEAD PLASTIC DUAL IN-LINE PACKAGE (SHRINK) (TYPE U)

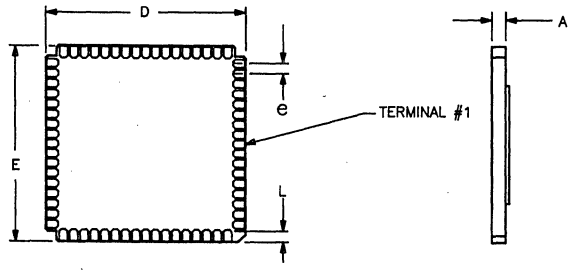


272118-6

Family: Plastic Dual In-Line Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	6	0.3
D	59	2.3
E_1	18	0.7
e_1	1.8	0.07
L	3	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

68-CERAMIC LEADLESS CHIP CARRIER (TYPE R) VARIATION: B

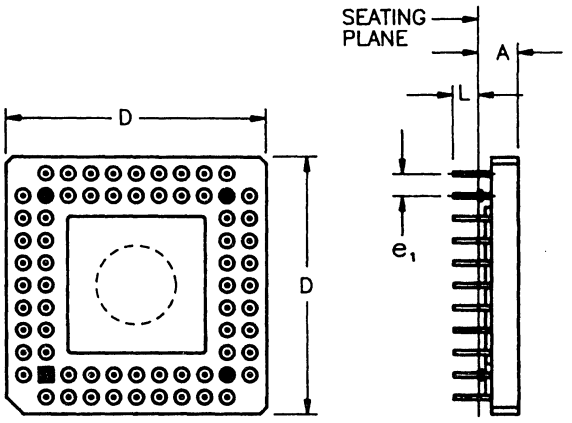


272118-7

Family: Ceramic Leadless Chip Carrier		
Symbol	**Millimeters Approx***	**Inches Approx***
A	3	0.1
D	25	1.0
E	25	1.0
e	1.3	0.05
L	1	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

68-LEAD CERAMIC PIN GRID ARRAY PACKAGE (TYPE A)

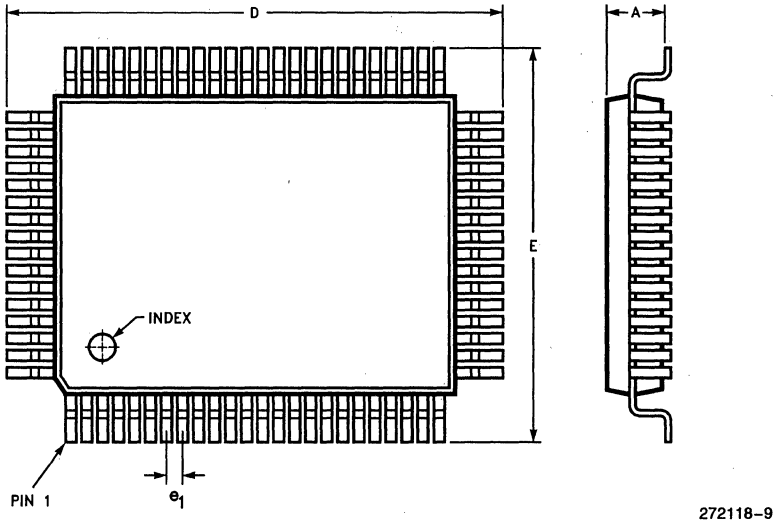


272118-8

Family: Ceramic Pin Grid Array Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	5	0.2
D	30	1.2
e_1	2.5	0.1
L	2	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

80-LEAD QUAD FLATPACK PACKAGE (TYPE S) VARIATION: RECTANGULAR

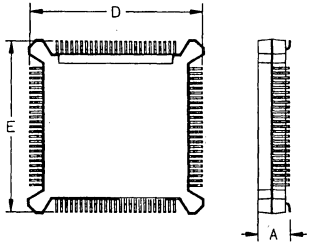


272118-9

Family: Quad Flatpack Package	
Symbol	**Millimeters Approx***
A	3
D	25
E	19
e_1	0.8

*For exact dimensions consult the Packaging Handbook (#240800).

100-LEAD PLASTIC QUAD FLATPACK PACKAGE (TYPE KU)

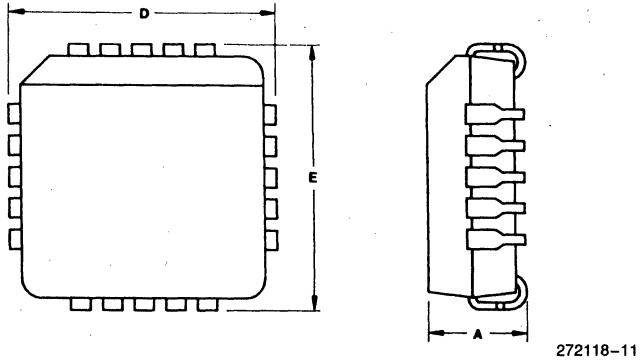


272118-10

Family: Plastic Quad Flatpack (0.025 Inch (0.635mm) Pitch)			
Symbol	**Description**	**Inches Approx***	**Millimeters Approx***
A	Package Height	0.2	5
D, E	Terminal Dimension	0.9	23

*For exact dimensions consult the Packaging Handbook (#240800).

42/52/68/84-LEAD PLASTIC LEADED CHIP CARRIER (TYPE N)



272118-11

Family: Plastic Leaded Chip Carrier—Square		
Symbol	44-Lead	
	Millimeters Approx*	Inches Approx*
A	5	0.2
D	18	0.7
E	18	0.7

Family: Plastic Leaded Chip Carrier—Square						
Symbol	Millimeters Approx*			Inches Approx*		
	68-Lead	52-Lead	84-Lead	68-Lead	52-Lead	84-Lead
A	5	5	5	0.2	0.2	0.2
D	26	21	31	1.0	0.8	1.2
E	26	21	31	1.0	0.8	1.2

*For exact dimensions consult the Packaging Handbook (#240800).

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