聯陽半導體
ITE Tech. Inc.

IT8705F/IT8705AF

Simple Low Pin Count Input / Output (Simple LPC I/O)

Preliminary Specification V0.4

INTEGRATED TECHNOLOGY EXPRESS, INC.

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Revision History

Note: Words in bold typeface in the revisions below indicate the changes.

Section	Revision	Page No.
1	• The feature of Flash ROM Interface was revised. • Added a new feature "**Only for IT8705AF**".	1
2	• In the fourth paragraph, "There is also a flash ROM interface with Address (FA[0:18])" was changed into "There is also a flash ROM interface with Address **(FA[0:19])**".	3
4	• Pin 26 was revised to "FA10/**VID_O5**/GP32". • Pin 27 was revised to "FA11/**VID_I5/**GP33". • Pin 49 was revised to "JSACX/GP40/**FAN_TAC1S** 5". • Pin 50 was revised to "JSACY/GP41/ **FAN_TAC2S**". • Pin 51 was revised to "JSAB1/GP42/ **FAN_TAC3S**". • Pin 52 was revised to "JSAB2/GP43/ **FAN_CTL3S**". • Pin 55 was revised to "JSBB1/GP46/ **FAN_CTL1S**". • Pin 56 was revised to "JSBB2/GP47/ **FAN_CTL2S**". • Pin 61 was revised to "DRVB#/SCCLK/**FA19**". • Pin 87 was revised to "**TMPIN3/COPEN#**". • Pin 91 was revised to "VIN7/**TMPIN3**".	7
5	• In table 5-3, the signal and description of pin 91 and 87 were revised. • In table 5-7, the signal, attribute and description of pin 49 to 52 and pin 55 to 56 were revised. • In table 5-10, the signal, attribute and description of pin 61 were revised. • In table 5-11, the signal, attribute and description of pin 26 to 31 were revised.	10-18
6	• In section six, the signal and description of pin 26, 27, 49 to 52, 55, 56 and 80 were revised.	22-23
8	• In table 8-1, index 2Bh was added.	28
	• In table 8-7, index D8h, D9h and DAh were added.	32
	• In section 8.3.5, the default value was changed into "**03h**"	35
	• In section 8.3.6, the description of bit 5 was revised. • In section 8.3.7, the description of bit 1 was revised.	36
	• Section 8.3.14 GPIO Set 4 Alternate Multi-Function Pin Selection Register (Index=2Bh, Default=00h) was added.	42
	• In section 8.5.5, 8.6.5 and 8.6.6, the description of bit 3 was revised.	45-47
	• In section 8.8.10, the description of bit 2 was revised.	52

Section	Revision	Page No.
	• Added the following three sections: 8.9.16 Flash ROM I/F Special Write Mask Based Address MSB Register (Index=D8h, Default=00h) 8.9.17 Flash ROM I/F Special Write Mask Based Address LSB Register (Index=D9h, Default=00h) 8.9.18 Flash ROM I/F Special Write Mask Size Control Register (Index=DAh, Default=00h)	57
	• In section 8.9.22, the description of bit 7-6 was revised.	59
	• Section 8.9.30 VID Input Register and section 8.9.31 VID Output Register were revised.	61
9	• In Table 9-2. Environment Controller Registers, the Registers or Action for index 0Ah, 0Ch, 18h, 19h, 1Ah, 1Bh, 1Ch, 1Dh, 48h, 56h, 57h, 61h –64h, 69h, 6Ah-6Ch, and 71h-74h were revised.	77-79
	• Added section 9.5.3.2.11 Reserved Register (Index=0Ah).	81
	• Added section 9.5.3.2.13 Fan Tachometer 16-bit Counter Enable Register.	82
	• In section 9.5.3.2.16Fan Controller Main Control Register, the descriptions of pin 6-4 and 3 were revised.	82
	• In section 9.5.3.2.17FAN_CTL Control Register, the descriptions of pin 6-4 and 3 were revised.	83
	• Added the following eight sections: 9.5.3.2.21Fan Tachometer 1-3 Extended Reading Registers 9.5.3.2.22Fan Tachometer 1-3 Extended Limit Registers 9.5.3.2.32 Thermal Diode Zero Degree Adjust 1 Register 9.5.3.2.33 Thermal Diode Zero Degree Adjust 2 Register and Code ID Register 9.5.3.2.42FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers 9.5.3.2.43FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Full Speed Registers 9.5.3.2.44FAN_CTL3-1 SmartGuardian Automatic Mode Start PWM Registers 9.5.3.2.45FAN_CTL3-1 SmartGuardian Automatic Mode Control Registers	84-88
	• In section 9.5.4.5 Fan Tachometer, the content was revised to “The Fan Tachometer inputs gate a 22.5 kHz clock into an 8-bit **or a 16-bit** counter (maximum count=255 **or 65535**) for one period of the input signals.’’	90
	• In section 9.5.4.7FAN Controller FAN_CTL’s ON-OFF and SmartGuardian Modes, the last paragraph was revised.	92

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1. Features

- **Low Pin Count Interface**
  - Compliant with Intel LPC Interface Specification Rev.1.0 (Sept. 29, 1997)
  - Supports Serial IRQ Protocol
  - Supports PCI PME# Interface

- **PC98/PC99, ACPI Compliant**
  - PC98 & PC99 compliant
  - Register sets compatible with “Plug and Play ISA Specification Rev. 1.0a”
  - ACPI V. 1.0 compliant
  - Supports 9 logical devices

- **Enhanced Hardware Monitor**
  - Built-in 8-bit Analog to Digital Converter
  - 3 thermal inputs from remote thermistors or thermal diode or diode-connected transistor
  - 8 voltage monitor inputs (VBAT is measured internally.)
  - Watch Dog comparison of all monitored values

- **Fan Speed Controller**
  - Provides Fan ON/OFF and PWM control
  - 3 programmable Pulse Width Modulation (PWM) Fan control outputs
  - Each PWM output supports 128 steps of PWM modes
  - Monitors 3 Fan tachometer inputs

- **Game Port**
  - Built-in 558 quad timers and buffer chips
  - Supports direct connection of two joysticks
  - Game port signals are multiplexed with GPIOs

- **Two 16C550 UARTs**
  - Supports two standard Serial ports
  - UART1 is dedicated for Serial port
  - UART2 supports either Serial Port or IrDA 1.0/ASKIR
  -

- **MIDI Interface**
  - UART implementation
  - Supports direct connection to MPU-401 MIDI

- **Consumer Remote Control (TV remote) IR with Power-up Feature**

- **IEEE 1284 Parallel Port**
  - Standard mode -- Bi-directional SPP compliant
  - Enhanced mode -- EPP V.1.7 and 1.9 compliant
  - High speed mode -- ECP, IEEE 1284 compliant
  - Backdrive current reduction
  - Printer power-on damage reduction
  - Supports POST (Power-On Self Test) Data Port

- **Floppy Disk Controller**
  - Supports two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives
  - Enhanced digital data separator
  - 3-Mode drives supported
  - Supports automatic write protection via software

- **Smart Card Reader**
  - Compliant with Personal Computer Smart Card (PC/SC) Working Group standard
  - Compliant with smart card (ISO 7816) protocols
  - Supports card present detect
  - Supports one programmable clock frequency, 7.1 MHz, and 3.5 MHz (default) card clocks

- **48 General Purpose I/O Pins**
  - Input mode supports switch de-bounce
  - SMI is routed through GPIOs
  - Power LED Blinking Control
  - Hardware Monitor Warning Beep Output
  - External IRQ Inputs Routing into Serial IRQ
  - Watch Dog Timer

- **Flash ROM Interface**
  - Up to 8M bits flash supported

- **Single 24/48 MHz Clock Inputs**

- **Only for IT8705AF**
  - 1 chassis open detection input with low power Flip-Flop backed by the battery

- **128-Pin QFP**

2. General Description

The IT8705F is a LPC Interface based highly integrated Super I/O. The IT8705F provides the most commonly used legacy Super I/O functionality plus the latest Environment Control initiatives, such as Hardware Monitor, Fan Speed Controller and ITE's "SmartGuardian" function. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.0" (Sept. 29, 1997). The IT8705F meets the "Microsoft® PC98 & PC99 System Design Guide" requirements and is ACPI compliant.

The IT8705F features the enhanced hardware monitor providing 3 thermal inputs from remote thermistors, thermal diode or diode-connected transistor (2N3904). The device also provides the ITE innovative intelligent automatic Fan ON/OFF & speed control functions (SmartGuardian) to reduce overall system noise and power consumption. It also features a PC/SC and ISO 7816 compliant Smart Card Reader.

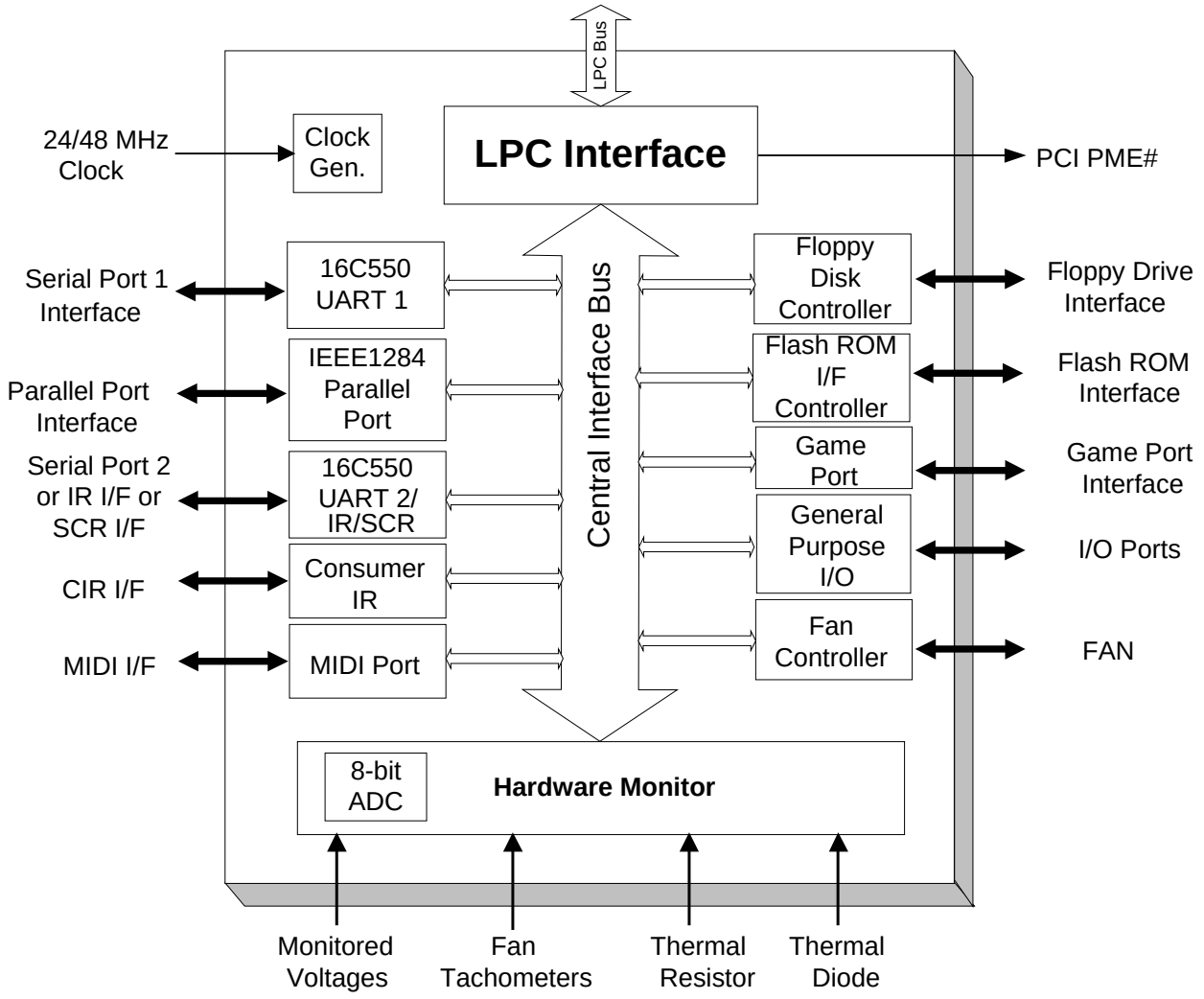
The IT8705F has integrated nine logical devices, featuring an Environment Controller (controls three Fans). The Environment Controller has temperature, voltage and Fan Speed monitors. One Fan Speed Controller is responsible to control three fan speeds through three 128 steps of Pulse Width Modulation (PWM) output pins and to monitor three fans' tachometer inputs.

Other features include one high-performance 2.88MB floppy disk controller, with digital data separator, supporting two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives. One multi-mode high-performance parallel port features the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9 are supported), and the IEEE 1284 compliant Extended Capabilities Port (ECP). Two 16C550 standard compatible enhanced UARTs perform asynchronous communication, and support SIR and one consumer remote control (TV remote) IR, one MPU-401 UART mode compatible MIDI port, one game port with built-in 558 quad timers and buffer chips to support direct connection of 2 joysticks, and six ports (44 GPIO pins). There is also a flash ROM interface with Address (FA[0:19]), Data (FD[0:7]), and supporting three control signals FCS#, FWE# and FRD#. In addition, a SmartGuardian engine is provided to monitor the system condition and reacts to the detected condition accordingly.

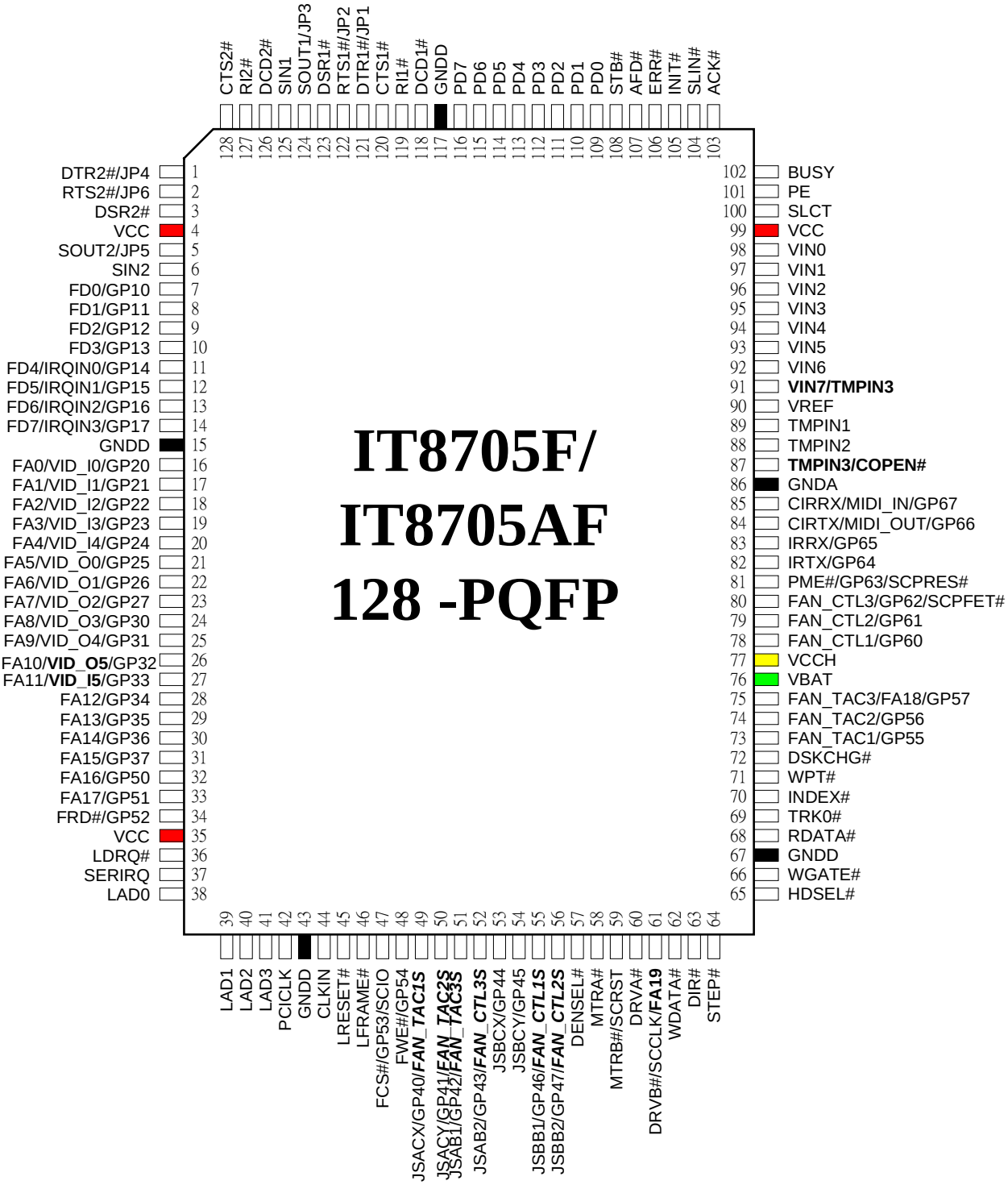
These nine logical devices can be individually enabled or disabled via software configuration registers. The IT8705F utilizes power-efficient circuitry to reduce power consumption. Once a logical device is disabled, the inputs are gated inhibit, the outputs are TRI-STATE and the input clock is disabled. The IT8705F requires a single 48/24 MHz clock input and operates with a single +5V power supply.

The IT8705F is available in 128-pin PQFP (Plastic Quad Flat Package).

3. Block Diagram



4. Pin Configuration



Top View

Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DTR2#/JP4	33	FA17/GP51	65	HDSEL#	97	VIN1
2	RTS2#/JP6	34	FRD#/GP52	66	WGATE#	98	VIN0
3	DSR2#	35	VCC	67	GNDD	99	VCC
4	VCC	36	LDRQ#	68	RDATA#	100	SLCT
5	SOUT2	37	SERIRQ	69	TRK0#	101	PE
6	SIN2	38	LAD0	70	INDEX#	102	BUSY
7	FD0/GP10	39	LAD1	71	WPT#	103	ACK#
8	FD1/GP11	40	LAD2	72	DSKCHG#	104	SLIN#
9	FD2/GP12	41	LAD3	73	FAN_TAC1/GP55	105	INIT#
10	FD3/GP13	42	PCICLK	74	FAN_TAC2/GP56	106	ERR#
11	FD4/IRQIN0/ GP14	43	GNDD	75	FAN_TAC3/FA18/ GP57	107	AFD#
12	FD5/IRQIN1/ GP15	44	CLKIN	76	VBAT	108	STB#
13	FD6/IRQIN2/ GP16	45	LRESET#	77	VCCH	109	PD0
14	FD7/IRQIN3/ GP17	46	LFRAME#	78	FAN_CTL1/GP60	110	PD1
15	GNDD	47	FCS#/SCIO/GP53	79	FAN_CTL2/GP61	111	PD2
16	FA0/VID_I0/GP20	48	FWE#/GP54	80	FAN_CTL3/GP62/ SCPFET#	112	PD3
17	FA1/VID_I1/GP21	49	JSACX/GP40/ FAN_TAC1S	81	PME#/GP63/ SCPRES#	113	PD4
18	FA2/VID_I2/GP22	50	JSACY/GP41/ FAN_TAC2S	82	IRTX/MIDI_OUT/ GP64	114	PD5
19	FA3/VID_I3/GP23	51	JSAB1/GP42/ FAN_TAC3S	83	IRRX/MIDI_IN/ GP65	115	PD6
20	FA4/VID_I4/GP24	52	JSAB2/GP43/ FAN_CTL3S	84	CIRTX/GP66	116	PD7
21	FA5/VID_O0/ GP25	53	JSBCX/GP44	85	CIRRX/GP67	117	GNDD
22	FA6/VID_O1/ GP26	54	JSBCY/GP45	86	GNDA	118	DCD1#
23	FA7/VID_O2/ GP27	55	JSBB1/GP46/ FAN_CTL1S	87	TMPIN3/COPEN#	119	RI1#
24	FA8/VID_O3/ GP30	56	JSBB2/GP47/ FAN_CTL2S	88	TMPIN2	120	CTS1#
25	FA9/VID_O4/ GP31	57	DENSEL#	89	TMPIN1	121	DTR1#/JP1
26	FA10/VID_O5/GP 32	58	MTRA#	90	VREF	122	RTS1#/JP2
27	FA11/ VID_I5/GP33	59	MTRB#/SCRST	91	VIN7/TMPIN3	123	DSR1#
28	FA12/GP34	60	DRVA#	92	VIN6	124	SOUT1/JP3
29	FA13/GP35	61	DRVB#/SCCLK/ FA19	93	VIN5	125	SIN1
30	FA14/GP36	62	WDATA#	94	VIN4	126	DCD2#
31	FA15/GP37	63	DIR#	95	VIN3	127	RI2#
32	FA16/GP50	64	STEP#	96	VIN2	128	CTS2#

5. IT8705F Pin Descriptions

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Signal	Attribute	Power	Description
4, 35, 99	VCC	PWR		***+5V Power Supply.***
76	VBAT	PWR		***+3.3V Battery Supply.***
77	VCCH	PWR		***+5V VCC Help Supply.***
15, 43, 67, 117	GNDD	GND		***Digital Ground.***
86	GNDA	GND		***Analog Ground.***

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Signal	Attribute	Power	Description
36	LDRQ#	DO16	VCC	***LPC DMA Request #.*** An encoded signal for DMA channel select.
37	SERIRQ	DIO16	VCC	***Serial IRQ.***
38 – 41	LAD[0:3]	DIO16	VCC	***LPC Address/Data 0-3.*** 4-bit LPC address / bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
42	PCICLK	DI	VCC	***LPC Clock.*** 33 MHz PCI Clock Input.
45	LRESET#	DI	VCC	***LPC RESET #.***
46	LFRAME#	DI	VCC	***LPC Frame #.*** This signal indicates the start of the LPC cycle.
81	PME#/ GP63/ SCPRES#	DOD8/ DIOD8/ DI	VCCH	***Power Management Event # / General Purpose I/O 63. / Smart Card Present Detect #.*** • The first function of this pin is the power management event #, and supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from D3 (cold) state. This pin is backed by VCCH. • The second function of this pin is the General Purpose I/O Port 6 Bit 3. • The third function of this pin is Smart Card Present Detect #. This pin provides the Smart Card insertion detection for the Smart Card Reader interface. Upon detecting the insertion of the Smart Card, this pin will trigger the power-on event. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of Hardware Monitor Signals Note1

Pin(s) No.	Signal	Attribute	Power	Description
98 – 92	VIN[0:6]	AI	VCC	***Voltage Analog Inputs [0:7].*** 0 to 4.096V FSR Analog Inputs.
91	VIN7/ TMPIN3	AI	VCC	***Voltage Analog Input 7/ External Thermal Input 3.*** • The first function of this pin is Regulated referenced voltage for 3 external temperature sensors and negative voltage monitor. • The second function of this pin is External Thermal Input 3, Connected to thermistor [1:3] or thermal diode [1:3]. • The function configuration of this pin is determined by programming the software configuration registers.
90	VREF	AO	VCC	***Reference Voltage Output.*** Regulated referenced voltage for 3 external temperature sensors and negative voltage monitor.
89 – 88	TMPIN[1:2]	AI	VCC	***External Thermal Inputs [1:2].*** Connected to thermistor [1:2] or thermal diode [1:2].
87 (IT8705F)	TMPIN3	AI	VCC	***External Thermal Inputs 3. (If IT8705F)*** Connected to thermistor [1:3] or thermal diode [1:3].
87 (IT8705AF)	COPEN#	DIOD8	VCCH or VBAT	***Case Open Detection #. (If IT8705AF)*** The Case Open Detection is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss.
73 – 74	FAN_TAC [1:2]/ GP5[5:6]	DI/ DIOD8	VCC	***Fan Tachometer Inputs [1:2]*** / ***General Purpose I/O 5[5:6].*** • The first functions of these pins are Fan tachometer inputs [1:2]. (0 to +5V amplitude fan tachometer input) • The second functions of these pins are General Purpose I/O Port 5 Bits 5-6. • The function configurations of these pins are determined by programming the software configuration registers.
75	FAN_TAC3 / FA18/ GP57	DI/ DO/ DIOD8	VCC	***Fan Tachometer Inputs 3 / Flash ROM Interface Address 18 / General Purpose I/O 57.*** • The first function of this pin is Fan Tachometer Inputs 3 (0 to +5V amplitude fan tachometer input). • The second function of this pin is the Flash ROM Interface Address 18. • The third function of this pin is General Purpose I/O Port 5 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-4. Pin Description of Fan Controller Signals [Note]

Pin(s) No.	Signal	Attribute	Power	Description
78 – 79	**FAN_CTL [1:2]/ GP6[0:1]**	DOD8/ DIOD8	VCCH	***FAN Control Outputs [1:2] / General Purpose I/O 6[0:1].*** • The first functions of these pins are Fan Control Outputs [1:2]. (PWM output signal to Fan's FET.) • The second functions of these pins are General Purpose I/O Port 6 Bits 0-1. • The function configurations of these pins are determined by programming the software configuration registers.
80	**FAN_CTL3/ GP62/ SCPFET#**	DOD8/ DIOD8/ DOD8	VCCH	***FAN Control Output 3 / General Purpose I/O 62 / Smart Card Power FET Control Output#.*** • The first functions of these pins are Fan Control Outputs [1:3]. (PWM output signal to Fan's FET.) • The second functions of these pins are General Purpose I/O Port 6 Bits 0-2. • The third function of this pin is Smart Card Power FET Control Output #. The Smart Card Reader interface requires this pin to drive an external Power FET to supply the current for the Smart Card (65 mA typical, 100 mA short to ground). • The function configurations of these pins are determined by programming the software configuration registers.

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 5-5. Pin Description of Infrared Port Signals [Note]

Pin(s) No.	Signal	Attribute	Power	Description
82	**IRTX/GP64**	DO8/ DIOD8	VCCH	***Infrared Transmit Output / General Purpose I/O 64.*** • The first function of this pin is the Infrared Transmit Output. • The second function of this pin is the General Purpose I/O Port 6 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.
83	**IRRX/GP65**	DI/ DIOD8	VCCH	***Infrared Receive Input / General Purpose I/O 65.*** • The first function of this pin is the Infrared Receive Input. • The second function of this pin is the General Purpose I/O Port 6 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
84	**CIRTX/ MIDI_OUT/ GP66**	DO8/ DO8/ DIOD8	VCCH	***Consumer Infrared Transmit Output / MIDI Output / General Purpose I/O 66.*** • The first function of this pin is the Consumer Infrared Transmit Output. • The second function of this pin is the MIDI Output. • The third function of this pin is the General Purpose I/O Port 6 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.

Table5-6. Pin Description of Infrared Port Signals [Note] [cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
85	**CIRRX/ MIDI_IN/ GP67**	DI/ DI/ DIOD8	VCCH	***Consumer Infrared Receive Input / MIDI Input / General Purpose I/O 67.*** • The first function of this pin is the Consumer Infrared Receive Input. • The second function of this pin is the MIDI Input. • The third function of this pin is the General Purpose I/O Port 6 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 5-6. Pin Description of Game Port Signals

Pin(s) No.	Signal	Attribute	Power	Description
49	**JSACX/ GP40/ FAN_TAC1S**	DIOD8/ DIOD8/ DI	VCC	***Joystick A Coordinate X / General Purpose I/O 40 / Second Port of FAN_TAC1.*** • The first function of this pin is the joystick A Coordinate X. • The second function of this pin is the General Purpose I/O Port 4 Bit 0. • The third function of this pin is the second port of FAN_TAC1. • The function configuration of this pin is determined by programming the software configuration registers.
50	**JSACY/ GP41/ FAN_TAC2S**	DIOD8/ DIOD8/ DI	VCC	***Joystick A Coordinate Y / General Purpose I/O 41 / Second Port of FAN_TAC2.*** • The first function of this pin is the joystick A Coordinate Y. • The second function of this pin is the General Purpose I/O Port 4 Bit 1. • The third function of this pin is the second port of FAN_TAC2. • The function configuration of this pin is determined by programming the software configuration registers.
51	**JSAB1/ GP42/ FAN_TAC3S**	DI/ DIOD8/ DI	VCC	***Joystick A Button 1 / General Purpose I/O 42 / Second Port of FAN_TAC3.*** • The first function of this pin is the joystick A Button 1. • The second function of this pin is the General Purpose I/O Port 4 Bit 2. • The third function of this pin is the second port of FAN_TAC3. • The function configuration of this pin is determined by programming the software configuration registers.
52	**JSAB2/ GP43/ FAN_CTL3S**	DI/ DIOD8/ DOD8	VCC	***Joystick A Button 2 / General Purpose I/O 43 / Second Port of FAN_CTL3.*** • The first function of this pin is the joystick A Button 2. • The second function of this pin is the General Purpose I/O Port 4 Bit 3. • The third function of this pin is the second port of FAN_CTL3. • The function configuration of this pin is determined by programming the software configuration registers.
53	**JSBCX/ GP44**	DIOD8/ DIOD8	VCC	***Joystick B Coordinate X / General Purpose I/O 44.*** • The first function of this pin is the joystick B Coordinate X. • The second function of this pin is the General Purpose I/O Port 4 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-6. Pin Description of Game Port Signals [cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
54	**JSBCY/ GP45**	DIOD8/ DIOD8	VCC	***Joystick B Coordinate Y / General Purpose I/O 45.*** • The first function of this pin is the joystick B Coordinate Y. • The second function of this pin is the General Purpose I/O Port 4 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
55	**JSBB1/ GP46/ FAN_CTL1S**	DI/ DIOD8/ DOD8	VCC	***Joystick B Button 1 / General Purpose I/O 46 / Second Port of FAN_CTL1.*** • The first function of this pin is the joystick B Button 1 Input. • The second function of this pin is the General Purpose I/O Port 4 Bit 6. • The third function of this pin is the second port of FAN_CTL1. • The function configuration of this pin is determined by programming the software configuration registers.
56	**JSBB2/ GP47/ FAN_CTL2S**	DI/ DIOD8/ DOD8	VCC	***Joystick B Button 2 / General Purpose I/O 47 / Second Port of FAN_CTL2.*** • The first function of this pin is the joystick B Button 2 Input. • The second function of this pin is the General Purpose I/O Port 4 Bit 7. • The third function of this pin is the second port of FAN_CTL2. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-7. Pin Description of Serial Port 1 Signals

Pin(s) No.	Signal	Attribute	Power	Description
118	**DCD1#**	DI	VCC	***Data Carrier Detect 1 #.*** When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
119	**RI1#**	DI	VCC	***Ring Indicator 1 #.*** When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
120	**CTS1#**	DI	VCC	***Clear to Send 1 #.*** When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
121	**DTR1#/JP1**	DO8/DI	VCC	***Data Terminal Ready 1 # / JP1.*** When the signal is low, this output indicates to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. During LRESET#, this pin is input for JP1 power-on strapping option.

Table 5-7. Pin Description of Serial Port 1 Signals[cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
122	RTS1#/JP2	DO8/DI	VCC	***Request to Send 1 # / JP2.*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. During LRESET#, this pin is input for JP2 power-on strapping option.
123	DSR1#	DI	VCC	***Data Set Ready 1 #.*** When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-7. Pin Description of Serial Port 1 Signals [cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
124	SOUT1/JP3	DO8/DI	VCC	***Serial Data Out 1 / JP3.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation. During LRESET#, this pin is input for JP3 power-on strapping option.
125	SIN1	DI	VCC	***Serial Data In 1.*** This input receives serial data from the communications link.

Table 5-8. Pin Description of Serial Port 2 Signals

Pin(s) No.	Signal	Attribute	Power	Description
126	DCD2#	DI	VCC	***Data Carrier Detect 2 #.*** When this signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
127	RI2#	DI	VCC	***Ring Indicator 2 #.*** When this signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI signal is a MODEM status input whose condition can be tested by reading the MSR register.
128	CTS2#	DI	VCC	***Clear to Send 2 #.*** When this signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
1	DTR2#/JP4	DO8/DI	VCC	***Data Terminal ready 2 # / JP4.*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. *During LRESET#, this pin is input for JP4 power-on strapping option.*

Table 5-8. Pin Description of Serial Port 2 Signals[cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
2	**RTS2#/JP6**	DO8/DI	VCC	***Request to Send 2 # / JP6.*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. *During LRESET#, this pin is input for JP6 power-on strapping option.*
3	**DSR2#**	DI	VCC	***Data Set Ready 2 #.*** When this signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
5	**SOUT2/JP5**	DO8/DI	VCC	***Serial Data Out 2 / JP5.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. *During LRESET#, this pin is input for JP5 power-on strapping option.*
6	**SIN2**	DI	VCC	***Serial Data In 2.*** This input receives serial data from the communications link.

Table 5-9. Pin Description of Parallel Port Signals

Pin(s) No.	Signal	Attribute	Power	Description
100	**SLCT**	DI	VCC	***Printer Select.*** This signal goes high when the line printer has been selected.
101	**PE**	DI	VCC	***Printer Paper End.*** This signal is set high by the printer when it runs out of paper.
102	**BUSY**	DI	VCC	***Printer Busy.*** This signal goes high when the line printer has a local operation in progress and cannot accept data.
103	**ACK#**	DI	VCC	***Printer Acknowledge #.*** This signal goes low to indicate that the printer has already received a character and is ready to accept another.
104	**SLIN#**	DIO24	VCC	***Printer Select Input #.*** When this signal is low, the printer is selected. This signal is derived from the complement of the bit 3 of the printer control register.
105	**INIT#**	DIO24	VCC	***Printer Initialize #.*** When this signal is active low, this signal is derived from the bit 2 of the printer control register, and is used to initialize the printer.
106	**ERR#**	DI	VCC	***Printer Error #.*** When this signal is active low, it indicates that the printer has encountered an error. The error message can be read from the bit 3 of the printer status register.
107	**AFD#**	DIO24	VCC	***Printer Auto Line Feed #.*** This signal is active low, and is derived from the complement of the bit 1 of the printer control register, and is used to advance one line after each line is printed.

Table 5-9. Pin Description of Parallel Port Signals[cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
108	STB#	DIO24	VCC	***Printer Strobe #.*** This signal is active low, and is derived from the complement of the bit 0 of the printer control register, and is used to strobe the printing data into the printer.
109 – 116	PD[0:7]	DIO24	VCC	***Parallel Port Data Bus 0-7.*** This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is de-selected.

Table 5-10. Pin Description of Floppy Disk Controller Signals

Pin(s) No.	Signal	Attribute	Power	Description
57	DENSEL#	DO40	VCC	***FDD Density Select #.*** DENSEL# is high for high data rates (500 Kbps, 1 Mbps). DENSEL# is low for low data rates (250 Kbps, 300 Kbps).
58	MTRA#	DO40	VCC	***FDD Motor A Enable #.*** Active low.
59	MTRB#/ SCRST	DO40/ DOD40	VCC	***FDD Motor B Enable #. / Smart Card Reset.*** • The first function of this pin is FDD Motor B Enable #. • The second function of this pin is Smart Card Reset. • The function configuration of this pin is decided by the software configuration registers.
60	DRVA#	DO40	VCC	***FDD Drive A Enable #.*** Active low.
61	DRVB#/ SCCLK/ FA19	DO40/ DOD40/ DO8	VCC	***FDD Drive B Enable # / Smart Card Clock.*** • The first function of this pin is the FDD Drive B Enable #. • The second function of this pin is Smart Card Clock. Three different card clocks are selectable from this pin: high speed (7.1 MHz), low speed (Default: 3.5 MHz) and a programmable card clock. • The third function of this pin is the Flash ROM Interface Address 19. • The function configuration of this pin is determined by the software configuration registers.
62	WDATA#	DO40	VCC	***FDD Write Serial Data to the Drive #.*** Active low.
63	DIR#	DO40	VCC	***FDD Head Direction #.*** This output determines the direction the FDC head movement during the SEEK operation. When the output is high, the head will step in. Otherwise, the head will step out.
64	STEP#	DO40	VCC	***FDD Step Pulse #.*** Active low.
65	HDSEL#	DO40	VCC	***FDD Head Select #.*** Active low.
66	WGATE#	DO40	VCC	***FDD Write Gate Enable #.*** Active low.
68	RDATA#	DI	VCC	***FDD Read Disk Data #.*** Active low. Serial data input from the FDD.
69	TRK0#	DI	VCC	***FDD Track 0 #.*** Active low. Indicates that the head of the selected drive is on track 0.
70	INDEX#	DI	VCC	***FDD Index #.*** Active low. Indicates the beginning of a disk track.

Table 5-10. Pin Description of Floppy Disk Controller Signals[cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
71	**WPT#**	DI	VCC	***FDD Write Protect #.*** Active low. Indicates that the disk of the selected drive is write-protected.
72	**DSKCHG#**	DI	VCC	***Floppy Disk Change #.*** Active low. This is an input pin that senses whether the drive door has been opened or a diskette has been changed.

Table 5-11. Pin Description of Flash ROM Interface Signals

Pin(s) No.	Signal	Attribute	Power	Description
7 – 10	**FD[0:3]/ GP1[0:3]**	DO8/ DIOD8	VCC	***Flash ROM Interface Data [0:3]/ General Purpose I/O 1[0:3].*** • The first functions of these pins are the Flash ROM interface Data [0:3]. • The second functions of these pins are the General Purpose I/O Port 1 Bits 0-3. • The function configurations of these pins are determined by programming the software configuration registers.
11 – 14	**FD[4:7]/ GP1[4:7]/ IRQIN[0:3]**	DO8/ DIOD8/ DI	VCC	***Flash ROM Interface Data [4:7]/ General Purpose I/O 1[4:7] /Interrupt Request Routing Input [0: 3].*** • The first functions of these pins are the Flash ROM interface Data [4:7]. • The second functions of these pins are the General Purpose I/O Port 1 Bits 4-7. • The third functions of these pins are the Interrupt Request Routing Input [0:3]. • The function configurations of these pins are determined by programming the software configuration registers.
16 – 20	**FA[0:4]/ GP2[0:4]/ VID_I[0:4]**	DO8/ DIOD8/ DI	VCC	***Flash ROM Interface Address[0:4] / General Purpose I/O 2[0:4] / Voltage ID Input [0:4].*** • The first functions of these pins are the Flash ROM Interface Address [0:4]. • The second functions of these pins are the General Purpose I/O Port 2 Bits 0-4. • The third functions of these pins are the Voltage ID Input [0:4]. • The function configurations of these pins are determined by programming the software configuration registers.
21 – 23	**FA[5:7]/ GP2[5:7]/ VID_O[0:2]**	DO8/ DIOD8/ DO8	VCC	***Flash ROM Interface Address[5:7] / General Purpose I/O 2[5:7] / Voltage ID Output [0:2].*** • The first functions of these pins are the Flash ROM Interface Address [5:7]. • The second functions of these pins are the General Purpose I/O Port 2 Bits 5-7. • The third functions of these pins are the Voltage ID Output [0:2]. • The function configurations of these pins are determined by programming the software configuration registers.

Table 5-11. Pin Description of Flash ROM Interface Signals[cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
24 – 25	**FA[8:9]/ GP3[0:1]/ VID_O[3:4]**	DO8/ DIOD8/ DO8	VCC	***Flash ROM Interface Address[8:9] / General Purpose I/O 3[0:1] / Voltage ID Output [3:4].*** • The first functions of these pins are the Flash ROM Interface Address [8:9]. • The second functions of these pins are the General Purpose I/O Port 3 Bits 0-1. • The third functions of these pins are the Voltage ID Output [3:4]. • The function configuration of this pin is determined by programming the software configuration registers.
26	**FA10/ GP32/ VID_O5**	DO8/ DIOD8/ DO8	VCC	***Flash ROM Interface Address 10 / General Purpose I/O 32 / Voltage ID Output 5.*** • The first functions of these pins are the Flash ROM Interface Address 10. • The second functions of these pins are the General Purpose I/O Port 3 Bit 2. • The third functions of these pins are the Voltage ID Output 5. • The function configuration of this pin is determined by programming the software configuration registers.
27	**FA11/ GP33/ VID_I5**	DO8/ DIOD8/ DI	VCC	***Flash ROM Interface Address 11 / General Purpose I/O 33/ Voltage ID Input 5.*** • The first functions of these pins are the Flash ROM Interface Address 11. • The second functions of these pins are the General Purpose I/O Port 3 Bits 3. • The third functions of these pins are the Voltage ID Input 5. • The function configuration of this pin is determined by programming the software configuration registers.
28 – 31	**FA[12:15]/ GP3[4:7]**	DO8/ DIOD8	VCC	***Flash ROM Interface Address[12:15] / General Purpose I/O 3[4:7].*** • The first functions of these pins are the Flash ROM Interface Address [12:15]. • The second functions of these pins are the General Purpose I/O Port 3 Bits 4-7. • The function configuration of this pin is determined by programming the software configuration registers.
32 – 33	**FA[16:17]/ GP5[0:1]**	DO8/ DIOD8	VCC	***Flash ROM Interface Address[16:17]/ General Purpose I/O 5[0:1].*** • The first function of these pins is Flash ROM Interface address [16:17]. • The second function of these pins is General Purpose I/O Port 5 Bits 0-1. • The function configurations of these pins are determined by programming the software configuration registers.

Table 5-11. Pin Description of Flash ROM Interface Signals[cont'd]

Pin(s) No.	Signal	Attribute	Power	Description
34	**FRD#/GP52**	DO8/ DIOD8	VCC	***Flash ROM Interface Read Strobe # / General Purpose I/O 52.*** • The first function of this pin is the Flash ROM Interface Read Strobe#. • The second function of this pin is the General Purpose I/O Port 5 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
47	**FCS#/GP53 / SCIO**	DO8/ DIOD8/ DIOD8	VCC	***Flash ROM Interface Chip Select # / General Purpose I/O 53 / Smart Card Serial Data I/O.*** • The first function of this pin is the Flash ROM Interface Chip Select #. • The second function of this pin is the General Purpose I/O Port 5 Bit 3. • The third function of this pin is Smart Card Serial Data I/O. • The function configuration of this pin is determined by programming the software configuration registers.
48	**FWE#/GP54**	DO8/ DIOD8	VCC	***Flash ROM Interface Write Enable #/ General Purpose I/O 54.*** • The first function of this pin is the Flash ROM Interface Write Enable #. • The second function of this pin is the General Purpose I/O Port 5 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-12. Pin Description of Miscellaneous Signals

Pin(s) No.	Signal	Attribute	Power	Description
44	**CLKIN**	DI	VCC	***24 MHz or 48 MHz Clock Input.***

IO Cell:

DO: Digital Output
DO8: 8mA Digital output buffer
DO16: 16mA Digital output buffer
DO40: 48mA Digital output buffer
DOD40: 48mA Digital Open-Drain output buffer

DIOD8: 8mA Digital Open-Drain Input/Output buffer

DIO8: 8mA Digital Input/Output buffer
DIO24: 24mA Digital Input/Output buffer

DI: Digital Input
AI: Analog Input
AO: Analog Output

Note 1: In addition to providing a highly integrated chip, ITE has also implemented a "SmartGuardian Utility" for hardware monitor application, providing a total solution for customers. The "SmartGuardian Utility" and the application circuit of hardware monitor function (the function arrangement of VIN0-7, TMPIN1-3, FAN_TAC1-3 and FAN_CTL1-3) are interdependent; that is, the " Smart Guardian Utility" is programmed according to the application circuit of hardware monitor function. ITE strongly recommends customers to follow the referenced application circuit of IT8705F to reduce the "time-to-market" schedule.

Pin No.	Signal	Recommended Function Arrangement
98	VIN0	2 Volt for VCORE1 of CPU.
97	VIN1	2 Volt for VCORE2 of CPU.
96	VIN2	3.3 Volt for system.
95	VIN3	5 Volt for system.
94	VIN4	+12 Volt for system.
93	VIN5	-12 Volt for system.
92	VIN6	-5 Volt for system.
91	VIN7	5 Volt for Standby power.

6. List of GPIO Pins

Table 6-1. General Purpose I/O Group 1

Signal	Pin #	Attribute	Description
FD0/GP10	**7**	DO8/ DIOD8	***Flash ROM Interface Data 0 / General Purpose I/O Port 1 Bit 0.***
FD1/GP11	**8**	DO8/ DIOD8	***Flash ROM Interface Data 1 / General Purpose I/O Port 1 Bit 1.***
FD2/GP12	**9**	DO8/ DIOD8	***Flash ROM Interface Data 2 / General Purpose I/O Port 1 Bit 2.***
FD3/GP13	**10**	DO8/ DIOD8	***Flash ROM Interface Data 3 / General Purpose I/O Port 1 Bit 3.***
FD4/IRQIN 0/GP14	**11**	DO8/DI/ DIOD8	***Flash ROM Interface Data 4 / Interrupt Request Routing Input 0 / General Purpose I/O Port 1 Bit 4.***
FD5/IRQIN 1/GP15	**12**	DO8/DI/ DIOD8	***Flash ROM Interface Data 5 / Interrupt Request Routing Input 1 / General Purpose I/O Port 1 Bit 5.***
FD6/IRQIN 2/GP16	**13**	DO8/DI/ DIOD8	***Flash ROM Interface Data 6 / Interrupt Request Routing Input 2 / General Purpose I/O Port 1 Bit 6.***
FD7/IRQIN 3/GP17	**14**	DO8/DI/ DIOD8	***Flash ROM Interface Data 7 / Interrupt Request Routing Input 3 / General Purpose I/O Port 1 Bit 7.***

Table 6-2. General Purpose I/O Group 2

Signal	Pin #	Attribute	Description
FA0/GP20/ VID_I0	**16**	DO8/ DIOD8/DI	***Flash ROM Interface Address 0 / General Purpose I/O Port 2 Bit 0 / Voltage ID Input 0.***
FA1/GP21 /VID_I1	**17**	DO8/ DIOD8/DI	***Flash ROM Interface Address 1 / General Purpose I/O Port 2 Bit 1 / Voltage ID Input 1.***
FA2/GP22/ VID_I2	**18**	DO8/ DIOD8/DI	***Flash ROM Interface Address 2 / General Purpose I/O Port 2 Bit 2 / Voltage ID Input 2.***
FA3GP23/ VID_I3	**19**	DO8/ DIOD8/DI	***Flash ROM Interface Address 3 / General Purpose I/O Port 2 Bit 3 / Voltage ID Input 3.***
FA4/GP24/ VID_I4	**20**	DO8/ DIOD8/DI	***Flash ROM Interface Address 4 / General Purpose I/O Port 2 Bit 4 / Voltage ID Input 4.***
FA5/GP25/ VID_O0	**21**	DO8/ DIOD8/DO	***Flash ROM Interface Address 5 / General Purpose I/O Port 2 Bit 5 / Voltage ID Output 0.***
FA6/GP26/ VID_O1	**22**	DO8/ DIOD8/DO	***Flash ROM Interface Address 6 / General Purpose I/O Port 2 Bit 6 / Voltage ID Output 1.***
FA7/GP27/ VID_O2	**23**	DO8/ DIOD8/DO	***Flash ROM Interface Address 7 / General Purpose I/O Port 2 Bit 7 / Voltage ID Output 2.***

Table 6-3. General Purpose I/O Group 3

Signal	Pin #	Attribute	Description
FA8/GPIO30/VID_O3	**24**	DO8/ DIOD8/DO	***Flash ROM Interface Address 8 / General Purpose I/O Port 3 Bit 0 / Voltage ID Output 3.***
FA9/GPIO31/VID_O4	**25**	DO8/ DIOD8/DO	***Flash ROM Interface Address 9 / General Purpose I/O Port 3 Bit 1 / Voltage ID Output 4.***
FA10/ GPIO32/ VID_O5	**26**	DO8/ DIOD8/ DO8	***Flash ROM Interface Address 10 / General Purpose I/O Port 3 Bit 2 / Voltage ID Output 5.***
FA11/ GPIO33/ VID_I5	**27**	DO8/ DIOD8/ DI	***Flash ROM Interface Address 11 / General Purpose I/O Port 3 Bit 3 / Voltage ID Input 5.***
FA12/ GPIO34	**28**	DO8/ DIOD8	***Flash ROM Interface Address 12 / General Purpose I/O Port 3 Bit 4.***
FA13/ GPIO35	**29**	DO8/ DIOD8	***Flash ROM Interface Address 13 / General Purpose I/O Port 3 Bit 5.***
FA14/ GPIO36	**30**	DO8/ DIOD8	***Flash ROM Interface Address 14 / General Purpose I/O Port 3 Bit 6.***
FA15/ GPIO37	**31**	DO8/ DIOD8	***Flash ROM Interface Address 15 / General Purpose I/O Port 3 Bit 7.***

Table 6-4. General Purpose I/O Group 4

Signal	Pin #	Attribute	Description
JSACX/ GP40/ FAN_TAC1S	**49**	DIOD8/ DIOD8/ DI	***Joystick A Coordinate X / General Purpose I/O Port 4 Bit 0/ Second Port of FAN_TAC1.***
JSACY/ GP41/ FAN_TAC2S	**50**	DIOD8/ DIOD8/ DI	***Joystick A Coordinate Y / General Purpose I/O Port 4 Bit 1/ Second Port of FAN_TAC2.***
JSAB1/ GP42/ FAN_TAC3S	**51**	DI/ DIOD8/ DI	***Joystick A Button 1 / General Purpose I/O Port 4 Bit 2 / Second Port of FAN_TAC3.***
JSAB2/ GP43/ FAN_CTL3S	**52**	DI/ DIOD8	***Joystick A Button 2 / General Purpose I/O Port 4 Bit 3/ Second Port of FAN_CTL3.***
JSBCX/ GP44	**53**	DIOD8/ DIOD8	***Joystick B Coordinate X / General Purpose I/O Port 4 Bit 4.***
JSBCY/ GP45	**54**	DIOD8/ DIOD8	***Joystick B Coordinate Y / General Purpose I/O Port 4 Bit 5.***

Table 6-5. General Purpose I/O Group 4[cont'd]

Signal	Pin #	Attribute	Description
JSBB1/ GP46/ FAN_CTL1 S	**55**	DI/ DIOD8	***Joystick B Button 1 / General Purpose I/O Port 4 Bit 6/ Second Port of FAN_CTL1.***
JSBB2/ GP47/ FAN_CTL2 S	**56**	DI/ DIOD8	***Joystick B Button 2 / General Purpose I/O Port 4 Bit 7/ Second Port of FAN_CTL2.***

Table 6-5. General Purpose I/O Group 5

Signal	Pin #	Attribute	Description
FA16/ GP50	**32**	DO8/ DIOD8	***Flash ROM Interface Address 16 / General Purpose I/O Port 5 Bit 0.***
FA17/ GP51	**33**	DO8/ DIOD8	***Flash ROM Interface Address 17 / General Purpose I/O Port 5 Bit 1.***
FRD#/ GP52	**34**	DO8/ DIOD8	***Flash ROM Interface Read Strobe # / General Purpose I/O Port 5 Bit 2.***
FCS#/ GP53/ SCIO	**47**	DO8/DIOD 8/DIOD8	***Flash ROM Interface Chip Select # / General Purpose I/O Port 5 Bit 3 / Smart Card Serial Data I/O.***
FWE#/ GP54	**48**	DO8/ DIOD8	***Flash ROM Interface Write Enable # / General Purpose I/O Port 5 Bit 4.***
FAN_TAC1 / GP55	**73**	DI/ DIOD8	***Fan Tachometer Input 1 / General Purpose I/O Port 5 Bit 5.***
FAN_TAC2 / GP56	**74**	DI/ DIOD8	***Fan Tachometer Input 2 / General Purpose I/O Port 5 Bit 6.***
FAN_TAC3 / FA18/GP57	**75**	DI/DO8/ DIOD8	***Fan Tachometer Input 3 / Flash ROM Interface Address 18 / General Purpose I/O Port 5 Bit 7.***

Table 6-6. General Purpose I/O Group 6[Note]

Signal	Pin #	Attribute	Description
FAN_CTL1/ GP60	**78**	DOD8/ DIOD8	***Fan Control Output 1 / General Purpose I/O Port 6 Bit 0.***
FAN_CTL2/ GP61	**79**	DOD8/ DIOD8	***Fan Control Output 2 / General Purpose I/O Port 6 Bit 1.***
FAN_CTL3/ GP62/ SCPFET#	**80**	DOD8/ DIOD8/ DOD8	***Fan Control Output 3 / General Purpose I/O Port 6 Bit 2 / Smart Card Power FET Control Output#.***
PME#/GP6 3/SCPRES #	**81**	DOD8/ DIOD8/DI	***Power Management Event # / General Purpose I/O Port 6 Bit 3 / Smart Card Present Detect#.***

Table 6-8. General Purpose I/O Group 6[Note] [cont'd]

Signal	Pin #	Attribute	Description
IRTX/GP64	**82**	DO8/ DIOD8	***Infrared Transmit Output / General Purpose I/O Port 6 Bit 4.***
IRRX/GP65	**83**	DI/ DIOD8	***Infrared Receive Input / General Purpose I/O Port 6 Bit 5.***
CIRTX/ MIDI_OUT/ GP66	**84**	DO8/ DO8/ DIOD8	***Consumer Infrared Transmit Output / MIDI Output / General Purpose I/O Port 6 Bit 6.***
CIRRX/ MIDI_IN/ GP67	**85**	DI/DI/ DIOD8	***Consumer Infrared Receive Input / MIDI Input / General Purpose I/O Port 6 Bit 7.***

Note: The GPIO registers of these pins are powered by VCC, not VCCH.

Table 6-7. Programming of Pins 82, 83, 84, and 85

Programming Condition			Pin 82
All, 2Ah, Bit 4	**LDN4, F4h, Bit 6**	**LDN7, F0h, Bit 5**	
1	X	X	GP64
0	0	X	IRTX
0	1	0	IRTX
0	1	1	CIRTX

Programming Condition		Pin 83
All, 2Ah, Bit 5	**LDN4, F4h, Bit 6**	
1	X	GP65
0	0	IRRX
0	1	IRRX/CIRRX

Programming Condition		Pin 84
All, 2Ah, Bit 6	**LDN4, F4h, Bit 6**	
1	X	GP66
0	0	CIRTX
0	1	MIDI_OUT

Programming Condition		Pin 85
All, 2Ah, Bit 7	**LDN4, F4h, Bit 6**	
1	X	GP67
0	0	CIRRX
0	1	MIDI_IN

7. Power On Strapping Options

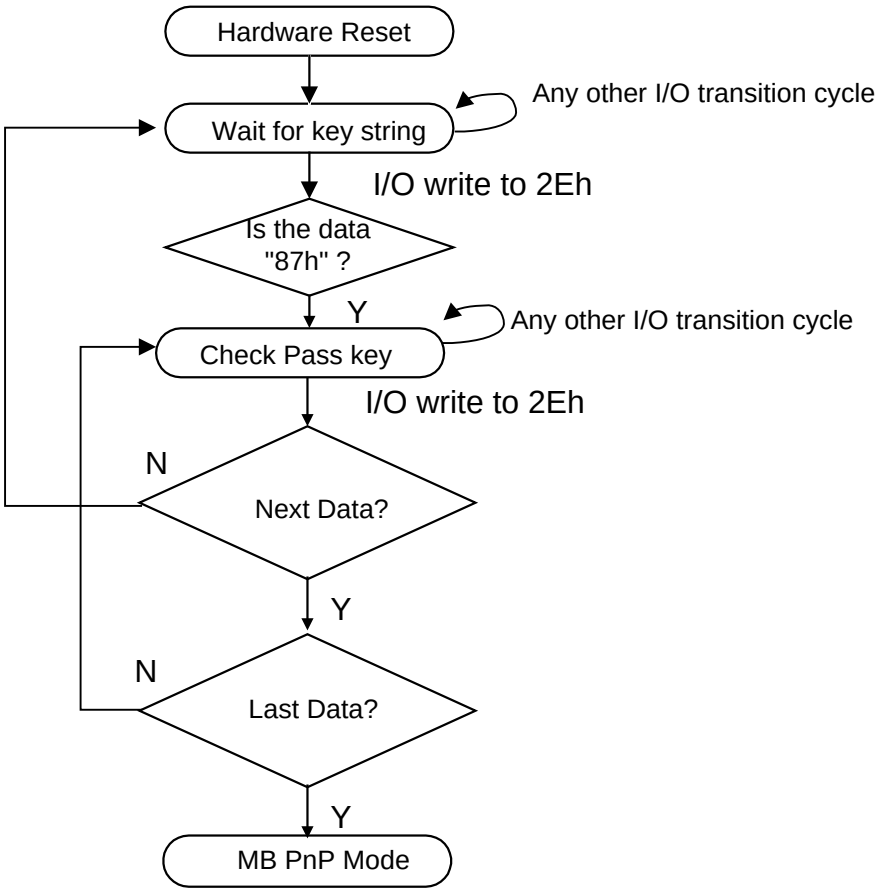
Table 7-1. Power On Strapping Options

	Signal	Description
JP1	Flash_Seg1	Flash ROM Interface Address Segment 1 (FFFF0000h-FFFFFFFFh, FFFE0000h-FFFEFFFFh) Enable.
JP2	Flash_Seg2	Flash ROM Interface Address Segment 2 (FFEF0000h-FFEFFFFh, FFEE0000h-FFEEFFFFh) Enable.
JP3	Flash_Seg3	Flash ROM Interface Address Segment 3 (FFF80000h-FFFDFFFFh, FFFE0000h-FFFEFFFFh) Enable.
JP4	Flash_Seg4	Flash ROM Interface Address Segment 4 (000F0000h-000FFFFFh, 000E0000h-000EFFFFh) Enable.
JP5	4M_Flash_En	4M Flash ROM Enable (Pin 75 is selected as FA18).
JP6	Chip_sel	Chip selection in Configuration.

8. Configuration

8.1 Configuring Sequence Description

After the hardware reset or power-on reset, the IT8705F enters the normal mode with all logical devices disabled.



There are three steps to completing the Motherboard mode of configuration. Step one is to enter the MB PnP mode. Step two is modifying the data of configuration registers. Step three is exiting the MB PnP mode. These three steps are explained below. Please note that step three must be followed or an undefined state will occur.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, 4 special I/O write operations must be performed during Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four I/O write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) as required in the next step.

	Address Port	Data Port
87h, 01h, 55h, 55h;	2Eh	2Fh
or 87h, 01h, 55h, AAh;	4Eh	4Fh

(2) Modifying the Data of the Configuration Registers

Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global Configuration registers. All registers can be accessed in this mode.

(3) Exit the MB PnP Mode

Set bit 1 of the Configure Control Register (Index: 02h) to "1" to exit the MB PnP mode.

8.2 Description of the Configuration Registers

All the registers will be reset to the default states when RESET is activated, except EC's PME registers.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number(LDN)
All	20h	RO	87h	Chip ID Byte 1
All	21h	RO	05h	Chip ID Byte 2
All	22h	W-RO	00h	Configuration Select and Chip Version
All	23h	R/W	00h	Software Suspend
All	24h	R/W	-	Clock Selection and Flash ROM I/F Control Register
05h*1	25h	R/W	00h	GPIO Set 1 Multi-Function Pin Selection Register
05h*1	26h	R/W	00h	GPIO Set 2 Multi-Function Pin Selection Register
05h*1	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
05h*1	28h	R/W	FFh	GPIO Set 4 Multi-Function Pin Selection Register
05h*1	29h	R/W	E0h	GPIO Set 5 Multi-Function Pin Selection Register
05h*1	2Ah	R/W	FFh	GPIO Set 6 Multi-Function Pin Selection Register
04h*1	2Bh	R/W	00h	GPIO Set 4 Alternate Multi-Function Pin Selection Register
F4h*1	2Eh	R/W	00h	Test Mode Register 1
F4h*1	2Fh	R/W	00h	Test Mode Register 2

Table 8-2. FDC Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Table 8-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register

Table 8-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	50h	Serial Port 2 Special Configuration Register 2
02h	F2h	R/W	00h	Serial Port 2 Special Configuration Register 3
02h	F3h	R/W	7Fh	Serial Port 2 Special Configuration Register 4

Table 8-5. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	64h	R/W	00h	POST Data Port Base Address MSB Register
03h	65h	R/W	80h	POST Data Port Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select[*2]
03h	F0h	R/W	03h[*3]	Parallel Port Special Configuration Register

Table 8-6. Environment Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
04h	30h	R/W	00h	Environment Controller Activate
04h	60h	R/W	02h	Environment Controller Primary Base Address MSB Register
04h	61h	R/W	90h	Environment Controller Primary Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	Environment Controller Interrupt Level Select
04h	F0h	R/W	00h	PME Event Enable Register
04h	F1h	R/W	00h	PME Status Register
04h	F2h	R/W	00h	PME Control Register 1
04h	F3h	R/W	00h	Environment Controller Special Configuration Register
04h	F4h	R-R/W	00h	PME Control Register 2
04h	F5h	R/W	-	PME Special Code Index Register
04h	F6h	R/W	-	PME Special Code Data Register

Table 8-7. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
05h	60h	R/W	00h	Simple I/O Base Address MSB Register
05h	61h	R/W	00h	Simple I/O Base Address LSB Register
05h	62h	R/W	00h	Panel Button De-bounce Base Address MSB Register
05h	63h	R/W	00h	Panel Button De-bounce Base Address LSB Register
05h	64h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
05h	65h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
05h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
05h	71h	R/W	00h	IRQ Routing Input 0 and 1Interrupt Level Select Register
05h	72h	R/W	00h	IRQ Routing Input 2 and 3 Interrupt Level Select Register
05h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
05h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
05h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
05h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
05h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
05h	B5h	R/W	00h	GPIO Set 6 Pin Polarity Register
05h	B8h	R/W	00h	GPIO Set 1 Pin Internal Pull-up Enable Register
05h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
05h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
05h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
05h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
05h	BDh	R/W	00h	GPIO Set 6 Pin Internal Pull-up Enable Register
05h	C0h	R/W	00h	Simple I/O Set 1 Enable Register
05h	C1h	R/W	00h	Simple I/O Set 2 Enable Register
05h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
05h	C3h	R/W	00h	Simple I/O Set 4 Enable Register

Table 8-7. GPIO Configuration Registers [cont'd]

LDN	Index	R/W	Reset	Configuration Registers or Action
05h	C4h	R/W	00h	Simple I/O Set 5 Enable Register
05h	C5h	R/W	00h	Simple I/O Set 6 Enable Register
05h	C8h	R/W	00h	Simple I/O Set 1 Output Enable Register
05h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
05h	CAh	R/W	00h	Simple I/O Set 3 Output Enable Register
05h	CBh	R/W	00h	Simple I/O Set 4 Output Enable Register
05h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register
05h	CDh	R/W	00h	Simple I/O Set 6 Output Enable Register
05h	D0h	R/W	00h	Panel Button De-bounce Control Register
05h	D1h	R/W	00h	Panel Button De-bounce Set 1 Enable Register
05h	D2h	R/W	00h	Panel Button De-bounce Set 2 Enable Register
05h	D3h	R/W	00h	Panel Button De-bounce Set 3 Enable Register
05h	D4h	R/W	00h	Panel Button De-bounce Set 4 Enable Register
05h	D5h	R/W	00h	Panel Button De-bounce Set 5 Enable Register
05h	D6h	R/W	00h	Panel Button De-bounce Set 6 Enable Register
05h	D8h	R/W	00h	Flash ROM I/F Special Write Mask Based Address MSB Register
05h	D9h	R/W	00h	Flash ROM I/F Special Write Mask Based Address LSB Register
05h	DAh	R/W	00h	Flash ROM I/F Special Write Mask Size Control Register
05h	F0h	R/W	00h	SMI# Control Register
05h	F1h	R/W	00h	Reserved
05h	F2h	R/W	00h	SMI# Status Register
05h	F5h	R/W	00h	SMI# Pin Mapping
05h	F6h	R/W	00h	Hardware Monitor Alert Beep Pin Mapping Register
05h	F7h	R/W	00h	GP LED Blinking 1 Pin Mapping Register
05h	F8h	R/W	00h	GP LED Blinking 1 Control Register
05h	F9h	R/W	00h	GP LED Blinking 2 Pin Mapping Register
05h	FAh	R/W	00h	GP LED Blinking 2 Control Register
05h	FBh	R/W	00h	Watch Dog Timer Control Register
05h	FCh	R/W	00h	Watch Dog Timer Time-out output Pin Mapping Register
05h	FDh	R/W	00h	Watch Dog Timer Time-out Value Register
05h	FEh	RO	--	VID Input Register
05h	FFh	R/W	00h	VID Output Register

Table 8-8. Game Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
06h	30h	R/W	00h	Game Port Activate
06h	60h	R/W	02h	Game Port Base Address MSB Register
06h	61h	R/W	01h	Game Port Base Address LSB Register

Table 8-9. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
07h	30h	R/W	00h	Consumer IR Activate
07h	60h	R/W	03h	Consumer IR Base Address MSB Register
07h	61h	R/W	10h	Consumer IR Base Address LSB Register
07h	70h	R/W	0Bh	Consumer IR Interrupt Level Select
07h	F0h	R/W	00h	Consumer IR Special Configuration Register

Table 8-10. MIDI Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
08h	30h	R/W	00h	MIDI Port Activate
08h	60h	R/W	03h	MIDI Port Base Address MSB Register
08h	61h	R/W	00h	MIDI Port Base Address LSB Register
08h	70h	R/W	0Ah	MIDI Port Interrupt Level Select
08h	F0h	R/W	00h	MIDI Port Special Configuration Register

Notes:

1: All these registers can be read from all LDNs.

2: When the ECP mode is not enabled, this register is **read only** as “04h”, and cannot be written.

3: When the bit 2 of the base address of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

8.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 8-11. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0 FDC	Base + (2 - 5) and + 7	
LDN=1 SERIAL PORT 1	Base + (0 -7)	
LDN=2 SERIAL PORT 2	Base1 + (0 -7)	COM Port
LDN=3 PARALLEL PORT	Base1 + (0 -3) Base1 + (0 -7) Base1 + (0 -3) and Base2 + (0 -3) Base1 + (0 -7) and Base2 + (0 -3) Base3	SPP SPP+EPP SPP+ECP SPP+EPP+ECP POST Data Port
LDN=4 Environment Controller	Base1 + (0 -7) Base2 + (0 -3)	Environment Controller PME#
LDN=5 GPIO		-
LDN=6 Game Port	Base + (0 -1)	-
LDN=7 Consumer IR	Base + (0 -7)	-
LDN=8 MIDI Port	Base + (0 -1)	-

8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	**Reserved**
1	**Return to the "Wait for Key" state.** This bit is used when the configuration sequence is completed.
0	Reset all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This **read/write** register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, the ACTIVATE command is only effective for the selected logical devices.

8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)

This **read only** register is the Chip ID Byte 1. Bits [7:0]=87h when read.

8.3.4 Chip ID Byte 2 (Index=21h, Default=05h)

This **read only** register is the Chip ID Byte 2. Bits [7:0]=05h when read.

8.3.5 Configuration Select and Chip Version (Index=22h, Default=03h)

Bit	Description
7	**Configuration Select** This bit is used to select the chip, which needed to be configured. When there are two IT8705F chips in a system, to write "1" this bit will select JP6=1 (power-on strapping value of RTS2#) to be configured. The chip with JP6=0 will exit the configuration mode. To write "0", the chip with JP6=0 will be configured and the chip with JP6=0 will exit. If no write on this register, both chips will be configured.
6-4	**Reserved**
3-0	**Version**

8.3.6 Software Suspend (Index=23h, Default=00h)

Bit	Description
7-6	**SCRPRES# Select** 00: Pin 81 01: Pin 79 10: Pin 75 11: Pin 74
5	**Special Customer ID Enable.** ***This bit can not be viewed on public SPEC.*** **This bit enables IT8705F to report the special Customer ID.** 0: Disable (default) 1: Enable.
4	**Reserved**
0	**Software Suspend** This register is the Software Suspend register. When the bit 0 is set, the IT8705F enters the "Software Suspend" state. All the devices remain inactive until this bit is cleared or when the wake-up event occurs. The wake-up event occurs at any transition on signals RI1# (pin 119) and RI2# (pin 127).

8.3.7 Clock Selection and Flash ROM I/F Control Register (Index=24h, Default=ssssss000b)

The default values of bits 7-3 depend on the power-on strapping of JP1-5.

Bit	Description
7	**Flash ROM Interface Address Segment 4 (000F0000h-000FFFFFh, 000E0000h-000EFFFFh) Enable**
6	**Flash ROM Interface Address Segment 3 (FFF80000h-FFFDFFFFh, FFFE0000h-FFFEFFFFh) Enable**
5	**Flash ROM Interface Address Segment 2 (FFEF0000h-FFEFFFFh, FFEE0000h-FFEEFFFFh) Enable**
4	**Flash ROM Interface Address Segment 1 (FFFF0000h-FFFFFFFFh, FFFE0000h-FFFEFFFFh) Enable**
3	**4M bits Flash ROM Enable (Pin 75 is selected as FA18)**
2	**Flash ROM I/F Writes Enable**
1	**8M bits Flash ROM Enable (Pin 61 is selected as FA19)**
0	**CLKIN Frequency** 0: 48 MHz. 1: 24 MHz.

8.3.8 GPIO Set 1 Multi-Function Pin Selection Register (Index=25h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 14** 0: Select the Flash ROM Interface Data 7. 1: Select the General Purpose I/O 17.
6	**Perform the function selection of pin 13** 0: Select the Flash ROM Interface Data 6. 1: Select the General Purpose I/O 16.
5	**Perform the function selection of pin 12** 0: Select the Flash ROM Interface Data 5. 1: Select the General Purpose I/O 15.
4	**Perform the function selection of pin 11** 0: Select the Flash ROM Interface Data 4. 1: Select the General Purpose I/O 14.
3	**Perform the function selection of pin 10** 0: Select the Flash ROM Interface Data 3. 1: Select the General Purpose I/O 13.
2	**Perform the function selection of pin 9** 0: Select the Flash ROM Interface Data 2. 1: Select the General Purpose I/O 12.
1	**Perform the function selection of pin 8** 0: Select the Flash ROM Interface Data 1. 1: Select the General Purpose I/O 11.
0	**Perform the function selection of pin 7** 0: Select the Flash ROM Interface Data 0. 1: Select the General Purpose I/O 10.

8.3.9 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 23** 0: Select the Flash ROM Interface Address 7. 1: Select the General Purpose I/O 27.
6	**Perform the function selection of pin 22** 0: Select the Flash ROM Interface Address 6. 1: Select the General Purpose I/O 26.
5	**Perform the function selection of pin 21** 0: Select the Flash ROM Interface Address 5. 1: Select the General Purpose I/O 25.
4	**Perform the function selection of pin 20** 0: Select the Flash ROM Interface Address 4. 1: Select the General Purpose I/O 24.
3	**Perform the function selection of pin 19** 0: Select the Flash ROM Interface Address 3. 1: Select the General Purpose I/O 23.
2	**Perform the function selection of pin 18** 0: Select the Flash ROM Interface Address 2. 1: Select the General Purpose I/O 22.
1	**Perform the function selection of pin 17** 0: Select the Flash ROM Interface Address 1. 1: Select the General Purpose I/O 21.
0	**Perform the function selection of pin 16** 0: Select the Flash ROM Interface Address 0. 1: Select the General Purpose I/O 20.

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 31** 0: Select the Flash ROM Interface Address15. 1: Select the General Purpose I/O 37.
6	**Perform the function selection of pin 30** 0: Select the Flash ROM Interface Address 14. 1: Select the General Purpose I/O 36.
5	**Perform the function selection of pin 29** 0: Select the Flash ROM Interface Address13. 1: Select the General Purpose I/O 35.

GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h) [cont'd]

Bit	Description
4	**Perform the function selection of pin 28** 0: Select the Flash ROM Interface Address 12. 1: Select the General Purpose I/O 34.
3	**Perform the function selection of pin 27** 0: Select the Flash ROM Interface Address 11. 1: Select the General Purpose I/O 33.
2	**Perform the function selection of pin 26** 0: Select the Flash ROM Interface Address 10. 1: Select the General Purpose I/O 32.
1	**Perform the function selection of pin 25** 0: Select the Flash ROM Interface Address 9. 1: Select the General Purpose I/O 31.
0	**Perform the function selection of pin 24** 0: Select the Flash ROM Interface Address 8. 1: Select the General Purpose I/O 30.

8.3.11 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=FFh)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 56** 0: Select the Joystick B Button 2. 1: Select the General Purpose I/O 47.
6	**Perform the function selection of pin 55** 0: Select the Joystick B Button 1. 1: Select the General Purpose I/O 46.
5	**Perform the function selection of pin 54** 0: Select the Joystick B Coordinate Y. 1: Select the General Purpose I/O 45.
4	**Perform the function selection of pin 53** 0: Select the Joystick B Coordinate X. 1: Select the General Purpose I/O 44.
3	**Perform the GP43 function of pin 52** 0: Select the Joystick A Button 2. 1: Select the General Purpose I/O 43.
2	**Perform the function selection of pin 51** 0: Select the Joystick A Button 1. 1: Select the General Purpose I/O 42.
1	**Perform the function selection of pin 50** 0: Select the Joystick A Coordinate Y. 1: Select the General Purpose I/O 41.
0	**Perform the function selection of pin 49** 0: Select the Joystick A Coordinate X. 1: Select the General Purpose I/O 40.

8.3.12 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=E0h)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 75** If 4M bits Flash ROM (bit 3 of Index 24h register) is enabled, this bit is no used. 0: Select the Fan Tachometer Input 3. 1: Select the General Purpose I/O 57.
6	**Perform the function selection of pin 74** 0: Select the Fan Tachometer Input 2. 1: Select the General Purpose I/O 56.
5	**Perform the function selection of pin 73** 0: Select the Fan Tachometer Input 1. 1: Select the General Purpose I/O 55.
4	**Perform the function selection of pin 48** 0: Select the Flash ROM Interface Write Enable #. 1: Select the General Purpose I/O 54.
3	**Perform the function selection of pin 47** 0: Select the Flash ROM Interface Chip Select #. 1: Select the General Purpose I/O 53.
2	**Perform the function selection of pin 34** 0: Select the Flash ROM Interface Read Strobe #. 1: Select the General Purpose I/O 52.
1	**Perform the function selection of pin 33** 0: Select the Flash ROM Interface Address 17. 1: Select the General Purpose I/O 51.
0	**Perform the function selection of pin 32** 0: Select the Flash ROM Interface Address 16. 1: Select the General Purpose I/O 50.

8.3.13 GPIO Set 6 Multi-Function Pin Selection Register (Index=2Ah, Default=FFh)

If the enabled bits are not set (0), the multi-function pins will perform the default functions. On the other hand, if they are set (1), they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=05h.

Bit	Description
7	**Perform the function selection of pin 85** 0: Select the Consumer Infrared Receive Input (if bit 6 of PCR2 is low) or MIDI Input (if bit 6 of PCR2 is high). 1: Select the General Purpose I/O 67.
6	**Perform the function selection of pin 84** 0: Select the Consumer Infrared Transmit Output (if bit 6 of PCR2 is low) or MIDI Output (if bit 6 of PCR2 is high). 1: Select the General Purpose I/O 66.
5	**Perform the function selection of pin 83** 0: Select the Infrared Receive Input. 1: Select the General Purpose I/O 65.
4	**Perform the function selection of pin 82** 0: Select the Infrared Transmit Output. 1: Select the General Purpose I/O 64.
3	**Perform the function selection of pin 81** 0: Select the Power Management Event #. 1: Select the General Purpose I/O 63.
2	**Perform the function selection of pin 80** 0: Select the Fan Control Output 3. 1: Select the General Purpose I/O 62.
1	**Perform the function selection of pin 79** 0: Select the Fan Control Output 2. 1: Select the General Purpose I/O 61.
0	**Perform the function selection of pin 78** 0: Select the Fan Control Output 1. 1: Select the General Purpose I/O 60.

8.3.14 GPIO Set 4 Alternate Multi-Function Pin Selection Register (Index=2Bh, Default=00h)

This register can be read from any LDN, but can only be written if LDN=04h.

Bit	Description
7	**ALTE_PIN56,** Alternate function control of pin 56. 0: The function of pin 56 is defined by bit7 of GPIO Set 4 Multi-Function Pin Selection Register. 1: The function of pin 56 is FAN_CTL2.
6	**ALTE_PIN55,** Alternate function control of pin 55. 0: The function of pin 55 is defined by bit6 of GPIO Set 4 Multi-Function Pin Selection Register. 1: The function of pin 55 is FAN_CTL1.
5-4	**Reserved.**
3	**ALTE_PIN52,** Alternate function control of pin 52. 0: The function of pin 52 is defined by bit3 of GPIO Set 4 Multi-Function Pin Selection Register. 1: The function of pin 52 is FAN_CTL3.
2	**ALTE_PIN51,** Alternate function control of pin 51. 0: The function of pin 51 is defined by bit2 of GPIO Set 4 Multi-Function Pin Selection Register. 1: The function of pin 51 is FAN_TAC3.
1	**ALTE_PIN50,** Alternate function control of pin 50. 0: The function of pin 50 is defined by bit1 of GPIO Set 4 Multi-Function Pin Selection Register. 1: The function of pin 50 is FAN_TAC0.
0	**ALTE_PIN49,** Alternate function control of pin 49. 0: The function of pin 49 is defined by bit0 of GPIO Set 4 Multi-Function Pin Selection Register. 1: The function of pin 49 is FAN_TAC1.

8.3.15 Test Mode Register 1 (Index=2Eh, Default=00h)

This register is the Test 1 Register and is reserved for ITE. It should not be set.

8.3.16 Test Mode Register 2 (Index=2Fh, Default=00h)

This register is the Test 2 Register and is reserved for ITE. It should not be set.

8.4 FDC Configuration Registers (LDN=00h)

8.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**FDC Enable** 0: Disabled. 1: Enabled.

8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only, with "0h" for Base Address [15:12]**
3-0	**FDC Base Address MSB** Mapped as Base Address [11:8].

8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	**FDC Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**FDC Interrupt Level Select** Select the interrupt level [note1] for FDC.

8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	**Reserved** with default "00h".
2-0	**FDC DMA Channel Select** Select the DMA channel [note2] for FDC.

8.4.6 FDC Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-4	**Reserved** with default “00h”.
3	**FDC IRQ Sharing** 1: IRQ sharing. 0: Normal IRQ.
2	**Floppy A/B Swap** 1: Swap Floppy Drives A, B. 0: Normal.
1	**3 mode/AT Mode** 1: 3-mode. 0: AT mode.
0	**Software Write Protect** 1: Software Write Protect. 0: Normal.

8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)

Bit	Description
7-4	**Reserved** with default “0000b”.
3-2	**FDD B Data Rate Table Select (DRT1-0)**
1-0	**FDD A Data Rate Table Select (DRT1-0)**

8.5 Serial Port 1 Configuration Registers (LDN=01h)

8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 1 Enable** 1: Enabled. 0: Disabled.

8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Serial Port 1 Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Serial Port 1 Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only as "000b".**

8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	**Reserved:** default = "0h."
3-0	**Serial Port 1 Interrupt Level Select** Select the interrupt level [note1] for Serial Port 1.

8.5.5 Serial Port 1 Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-4	**Reserved:** default = "00h".
3	**IRQ mode selection** 1: No IRQ will be generated when MCR bit3 is from high to low. 0: Normal (default).
2-1	**Clock Source** 00: 24 MHz/13 (Standard). Others: Reserved.
0	**IRQ Sharing Enable** 1: IRQ sharing. 0: Normal.

8.6 Serial Port 2 Configuration Registers (LDN=02h)

8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 2 Enable** 1: Enabled. 0: Disabled.

8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only:** with "0h" for Base Address[15:12].
3-0	**Serial Port 2 Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Serial Port 2 Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only:** as "000b".

8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**Serial Port 2 Interrupt Level Select** Select the interrupt level [note1] for Serial Port 2.

8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-4	**Reserved:** with default "00h".
3	**IRQ mode selection** 1: No IRQ will be generated when MCR bit3 is from high to low. 0: Normal (default).
2-1	**Clock Source** 00: 24 MHz/13 (Standard). Others: Reserved.
0	**IRQ Sharing Enable** 1: IRQ sharing. 0: Normal.

8.6.6 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	**IR Rx2Tx Delay Mode** 1:No transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode. 0: Transmission delays (40 bits) when the SIR or ASKIR is switched from RX mode to TX mode.
6	**IR Tx2Rx Delay Mode** 1: No reception delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode. 0: Reception delays (40 bits) when the SIR or ASKIR is switched from TX mode to RX mode.
5	**Reserved**
4	**Half Duplex Enable** 1: Half Duplex (default). 0: Full Duplex.
3	**SIRRX Polarity selection** 1: low pulse. 0: high pulse (default).
2-0	**UART 2 Function Select** 000: Standard 001: IrDA SIR 010: ASKIR 100 : Smart Card Reader (SCR) Others: Reserved

8.6.7 Serial Port 2 Special Configuration Register 3 (Index=F2h, Default=00h)

Bit	Description
7	**COM_PNP_EN** 0: Disable COM Port device Plug-and-Play operation (default). 1: Enable COM Port device Plug-and-Play operation.
6-5	**Reserved**
4	**PNP_ID** This bit is only available when bit 7=1. 0: PNP_ID Access mode (default). 1: Normal Plug-and-Play operation mode.
3	**Reserved**
2	**SCPFET# Polarity** 0: Active low (default). 1: Active high.
1-0	**SCR Clock Select** 00: Stop 01: 3.5 MHz 10: 7.1 MHz 11: Special Divisor (96 MHz/DIV96M)

8.6.8 Serial Port 2 Special Configuration Register 4 (Index=F3h, Default=7Fh)

Bit	Description
7	**Reserved**
6-0	**SCR Clock Special Divisor (DIV96M)** When the SCR Clock Select is 11b, the SCCLK output clock frequency is 96MHz / DIV96M.

8.7 Parallel Port Configuration Registers (LDN=03h)

8.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Parallel Port Enable** 1: Enabled. 0: Disabled.

8.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12].
3-0	**Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If the bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	**Base Address LSB** **Read/write**, mapped as Base Address[7:2].
1-0	**Read only** as “00b”.

8.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12].
3-0	**Secondary Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	**Secondary Base Address LSB** **Read/write**, mapped as Base Address[7:2].
1-0	**Read only** as “00b”.

8.7.6 POST Data Port Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as “0h” for Base Address[15:12].
3-0	**POST Data Port Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.7.7 POST Data Port Base Address LSB Register (Index=65h, Default=80h)

Bit	Description
7-0	**POST Data Port Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.7.8 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	**Reserved** with default “0h”.
3-0	**Interrupt Level Select** Select the interrupt level [note1] for Parallel Port.

8.7.9 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	**Reserved** with default “00h”.
2-0	**DMA Channel Select** Select the DMA channel [note2] for Parallel Port.

8.7.10 Parallel Port Special Configuration Register (Index=F0h, Default=03h)

Bit	Description
7-4	**Reserved**
3	**POST Data Port Disable** 1: POST Data Port Disable. 0: POST Data Port Enable.
2	**IRQ Sharing Enable** 1: IRQ sharing. 0: Normal.
1-0	**Parallel Port Mode** 00: SPP (Standard Parallel Port mode) 01: SPP & EPP (Enhanced Parallel Port) 10: SPP & ECP (Extended Capabilities Parallel Port) 11: SPP & EPP & ECP

If the bit 1 is set, ECP mode is enabled. If the bit 0 is set, EPP mode is enabled. These two bits are independent. However, according to the EPP spec., when Parallel Port Primary Base Address bit 2 is set to 1, the EPP mode cannot be enabled.

8.8 Environment Controller Configuration Registers (LDN=04h)

8.8.1 Environment Controller Activate Register (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Environment Controller Enable** 1: Enabled. 0: Disabled.

8.8.2 Environment Controller Primary Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**E.C. Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.8.3 Environment Controller Primary Base Address LSB Register (Index=61h, Default=90h)

Bit	Description
7-3	**E.C. Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

8.8.4 PME Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**PME Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.8.5 PME Direct Access Base Address LSB Register (Index=63h, Default=30h)

Bit	Description
7-3	**PME Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

8.8.6 Environment Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**E.C. Interrupt Level Select** Select the interrupt level [note1] for Environment Controller.

8.8.7 PME Event Enable Register (Index=F0h, Default=00h)

Bit	Description
7	It is set to 1 when VCCH is OFF. Writing 1 to clear this bit. This bit is ineffective when a “0” is written to this bit.
6-3	**Reserved**
2	**RI2# Event Enable** 1: RI2# event enabled. 0: RI2# event disabled.
1	**RI1# Event Enable** 1: RI1# event enabled. 0: RI1# event disabled.
0	**CIR Event Enable** 1: CIR event enabled. 0: CIR event disabled.

8.8.8 PME Status Register (Index=F1h, Default=00h)

Bit	Description
7	It is set to 1 when VCC is ON during previous AC power failure, and 0 when VCC power is OFF.
6-3	**Reserved**
2	**RI2# Event Detected** 1: RI2# event detected. 0: RI2# event undetected.
1	**RI1# Event Detected** 1: RI1# event detected. 0: RI1# event undetected.
0	**CIR Event Detected** 1: CIR event detected. 0: CIR event undetected.

8.8.9 PME Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	**PER and PSR Normal Run Access Enable**
6-0	**Reserved**

8.8.10 Environment Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-3	**Reserved**
2	**PIN91_SEL, the function selection of pin 91.** 1: The function of pin 91 is TMPIN3. 0: The function of pin 91 is VIN7. (Default).
1	**Reserved**
0	**EC IRQ Sharing Enable** 1: IRQ sharing. 0: Normal.

8.8.11 PME Control Register 2 (PCR2) (Index=F4h, Default=00h)

Bit	Description
7	**Reserved**
6	**This bit is active when the related pins are not selected as GPIO function.** 1: SIR/ASKIR and CIR ports use the same pins (Pin 82 and Pin 83). Pins 84 and 85 are defined at MIDI port. 0: Pins 82 and 83 are defined at SIR/ASKIR port, and pins 84 and 85 are defined at CIR port.
5-0	**Reserved**

8.8.12 PME Special Code Index Register (Index=F5h)

Bit	Description
7-6	**Reserved** (should be filled “00b”).
5-0	Indicate which Identification Key Code or CIR code register is to be read/written via 0xF6.

8.8.13 PME Special Code Data Register (Index=F6h)

There are 20 CIR event codes (Index 20h-32h) stored in this port. The index pointer is changed by PME Special Code Index Register. The first byte (Index 20h) is used to specify the pattern length in bytes. Bits[7:4] are used when VCC is ON, and bits[3:0] are used when VCC goes OFF. The minimum byte number is 3 (when bits[7:4] or bits[3:0]=0h), and the maximum byte number is 18 (when bits[7:4] or bits[3:0] =Fh).

8.9 GPIO Configuration Registers (LDN=05h)

8.9.1 Simple I/O Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**Simple IO Base Address MSB** **Read/write**, mapped as Base Address [11:8].

8.9.2 Simple I/O Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-0	**Simple IO Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.9.3 Panel Button De-bounce Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**P.B.D Base Address MSB** **Read/write**, mapped as Base Address [11:8].

8.9.4 Panel Button De-bounce Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	**P.B.D Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.9.5 SMI# Normal Run Access Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**SMI Base Address MSB** **Read/write**, mapped as Base Address [11:8].

8.9.6 SMI# Normal Run Access Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-0	**SMI Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.9.7 Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)

Bit	Description
7-4	**Reserved**
3-0	**P.B.D Interrupt Level Select** Select the interrupt level [note1] for Panel Button De-bounce.

8.9.8 IRQ Routing Input 0 and 1 Interrupt Level Select Register (Index=71h, Default=00h)

Bit	Description
7-4	**IRQIN1 Interrupt Level Select** Select the interrupt level [note1] for IRQIN1.
3-0	**IRQIN0 Interrupt Level Select** Select the interrupt level [note1] for IRQIN0.

8.9.9 IRQ Routing Input 2 and 3 Interrupt Level Select Register (Index=72h, Default=00h)

Bit	Description
7-4	**IRQIN3 Interrupt Level Select** Select the interrupt level [note1] for IRQIN3.
3-0	**IRQIN2 Interrupt Level Select** Select the interrupt level [note1] for IRQIN2.

8.9.10 GPIO Pin Set 1, 2, 3, 4, 5 and 6 Polarity Registers (Index=B0h, B1h, B2h, B3h, B4h and B5h, Default=00h)

These registers are used to program the GPIO pin type as either polarity inverting or non-inverting.

Bit	Description
7-0	**GPIO Polarity Inverting** For each bit: 1: GPIO pin type is polarity inverting. 0: GPIO pin type is polarity non-inverting.

8.9.11 GPIO Pin Set 1, 2, 3, 4, 5 and 6 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh, BCh and BDh, Default=00h)

These registers are used to enable the GPIO pin internal pull-up.

Bit	Description
7-0	**GPIO Pull-up Enable** For each bit: 1: Enable GPIO pin internal pull-up. 0: Disable GPIO pin internal pull-up.

8.9.12 Simple I/O Set 1, 2, 3, 4, 5 and 6 Enable Registers (Index=C0h, C1h, C2h, C3h,C4h and C5h, Default=00h)

These registers are used to select the functions of either the Simple I/O or the Alternate function.

Bit	Description
7-0	**Simple GPIO Enable** For each bit: 1: Select the Simple I/O function. 0: Select the Alternate function.

8.9.13 Simple I/O Set 1, 2, 3, 4, 5 and 6 Output Enable Registers (Index=C8h,C9h,CAh,CBh,CCh and CDh, Default=00h)

These registers are used to determine the direction of the Simple I/O.

Bit	Description
7-0	**GPIO Output Enable** For each bit: 0: The direction of the Simple I/O is input mode. 1: The direction of the Simple I/O is output mode.

8.9.14 Panel Button De-bounce Control Register (Index=D0h, Default=00h)

Bit	Description
7-5	**Reserved**
4	**IRQ Sharing** 0: Disabled. 1: Enabled.
3	**IRQ Output Type** 0: Edge. 1: Level.
2	**IRQ Output Enable** 0: Disabled. 1: Enabled.
1-0	**De-bounce Time Selection** 00: 8 ms (6 ms ignored, 8 ms passed) 01: 16 ms (12 ms ignored, 16 ms passed) 10: 32 ms (24 ms ignored, 21 ms passed) 11: 64 ms (48 ms ignored, 64 ms passed)

8.9.15 Panel Button De-bounce Set 1, 2, 3, 4, 5 and 6 Enable Registers (Index=D1h, D2h, D3h, D4h, D5h and D6h, Default=00h)

These registers are used to enable Panel Button De-bounce for each pin.

Bit	Description
7-0	**P.B.D Enable** For each bit: 1: Enable Panel Button De-bounce. 0: Disable Panel Button De-bounce

8.9.16 Flash ROM I/F Special Write Mask Based Address MSB Register (Index=D8h, Default=00h)

Bit	Description
7-0	**Flash ROM I/F Special Write Mask Based Address [18:11]**

8.9.17 Flash ROM I/F Special Write Mask Based Address LSB Register (Index=D9h, Default=00h)

Bit	Description
7-2	**Flash ROM I/F Special Write Mask Based Address [10:5]**
1	**Reserved**
0	**Flash ROM I/F Special Write Mask Based Address 19**

8.9.18 Flash ROM I/F Special Write Mask Size Control Register (Index=DAh, Default=00h)

Bit	Description
7-5	**Reserved**
4-1	**Flash ROM I/F Special Write Mask Size Control** 0h: 32 bytes (Address 4-0 will not be compared) 1h: 64 bytes (Address 5-0 will not be compared) 2h: 128 bytes (Address 6-0 will not be compared) 3h: 256 bytes (Address 7-0 will not be compared) 4h: 512 bytes (Address 8-0 will not be compared) 5h: 1024 bytes (Address 9-0 will not be compared) 6h: 2048 bytes (Address 10-0 will not be compared) 7h: 4096 bytes (Address 11-0 will not be compared)
0	**Flash ROM I/F Special Write Mask Enable** 0: Disable (default) 1: Enable.

8.9.19 SMI# Control Register (Index=F0h, Default=00h)

Bit	Description
7	**Reserved**
6	**SMI# of MIDI IRQ Enable** Enable the generation of an SMI# due to MIDI Port's IRQ (EN_CIRQ).
5	**SMI# of CIR IRQ Enable** Enable the generation of an SMI# due to CIR's IRQ (EN_CIRQ).
4	**SMI# of EC IRQ Enable** Enable the generation of an SMI# due to Environment Controller's IRQ (EN_ECIRQ).
3	**SMI# of PPORT IRQ Enable** Enable the generation of an SMI# due to Parallel Port's IRQ (EN_PIRQ).
2	**SMI# of UART2 IRQ Enable** Enable the generation of an SMI# due to Serial Port 2's IRQ (EN_S2IRQ).
1	**SMI# of UART1 IRQ Enable** Enable the generation of an SMI# due to Serial Port 1's IRQ (EN_S1IRQ).
0	**SMI# of FDC IRQ Enable** Enable the generation of an SMI# due to FDC's IRQ (EN_FIRQ).

8.9.20 SMI# Status Register (Index=F2h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7	**Reserved**
6	The generation of an SMI# due to MIDI Port's IRQ.
5	The generation of an SMI# due to CIR's IRQ.
4	The generation of an SMI# due to Environment Controller's IRQ.
3	The generation of an SMI# due to Parallel Port's IRQ.
2	The generation of an SMI# due to Serial Port 2's IRQ.
1	The generation of an SMI# due to Serial Port 1's IRQ.
0	The generation of an SMI# due to FDC's IRQ.

8.9.21 SMI# Pin Mapping Register (Index=F5h, Default=00h)

Bit	Description
7	**Reserved**
6	**SMI# Direct Access Enable** 0: Disable SMI# Direct Access (default) 1: Enable SMI# Direct Access.
5-0	**SMI# Pin Location** Please see Location mapping table [note3].

8.9.22 Hardware Monitor Alert Beep Pin Mapping Register (Index=F6h, Default=00h)

Bit	Description
7-6	**Hardware Monitor Thermal Output Pin Location** 00: None 01: Reserved 10: Pin 49 11: Pin 59
5-0	**Hardware Monitor Alert Beep Pin Location** Please see Location mapping table [note3].

8.9.23 GP LED Blinking 1 Pin Mapping Register (Index=F7h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 1 Pin Location** Please see Location mapping table [note3].

8.9.24 GP LED Blinking 1 Control Register (Index=F8h, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 1 Active Pulse Control** 0: 1/2 duty (default) 1: short active pulse.
2-1	**GP LED Blinking 1 Frequency Select** 00: 4 Hz (default) 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 1 Active Mode** 0: Blinking mode (default). 1: Always active.

8.9.25 GP LED Blinking 2 Pin Mapping Register (Index=F9h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 2 Pin Location** Please see Location mapping table [note3].

8.9.26 GP LED Blinking 2 Control Register (Index=FAh, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 2 Active Pulse Control** 0: 1/2 duty (default). 1: short active pulse.
2-1	**GP LED Blinking 2 Frequency Select** 00: 4 Hz (default) 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 2 Active Mode** 0: Blinking mode (default). 1: Always active.

8.9.27 Watch Dog Timer Control Register (Index=FBh, Default=00h)

Bit	Description
7	**CIR Interrupt to Reset WDT Counter Enable** 0: Disable a CIR Interrupt to reset WDT Counter (default). 1: Enable a CIR Interrupt to reset WDT Counter.
6-5	**Reserved**
4	**A read from or write to the Game Port Base Address to Reset WDT Counter Enable** 0: Disable a read from or write to Game port base address to reset WDT Counter (default). 1: Enable a read from or write to Game port base address to reset WDT Counter.
3	**WDT Counter Unit Select** 0: Minute (default). 1: Second.
2	**Reserved**
1	**Direct Time Out Control** This bit is self-clearing. 0: Normal (default). 1: Direct Time out regardless of the counter.
0	**WDT Status** 0: No time-out after last re-load counter value (default). 1: The timer was time-out.

8.9.28 Watch Dog Timer Time-out Output Pin Mapping Register (Index=FCh, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Watch Dog Timer Time-out Output Pin Location** Please see Location mapping table [note3].

8.9.29 Watch Dog Timer Time-out Value Register (Index=FDh, Default=00h)

Bit	Description
7-0	**Watch Dog Timer Time-out Value** Watch Dog Timer Counter Time-out value (1~256 unit(s)).

8.9.30 VID Input Register (Index=FEh, Default= --)

Bit	Description
7-6	**Reserved**
5-0	**VID_I[5:0]** These bits are read-only. When read, they will perform the states of pins VID_I[5:0].

8.9.31 VID Output Register (Index=FFh, Default=00h)

Bit	Description
7	**VID_O[5:0] Output Select** 0: Translate VID_I[5:0] directly (default). 1: Output the desired value (bits [5:0] of this register).
6	**Reserved**
5-0	**Output Value of VID_O[5:0]** These bits are desired output value of VID_O[5:0].

8.10 Game Port Configuration Registers (LDN=06h)

8.10.1 Game Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Game Port Enable** 1: Enabled. 0: Disabled.

8.10.2 Game Port Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**Game Port Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.10.3 Game Port Base Address LSB Register (Index=61h, Default=01h)

Bit	Description
7-0	**Game Port Base Address LSB** **Read/write**, mapped as Base Address[7:0].

8.11 Consumer IR Configuration Registers (LDN=07h)

8.11.1 Consumer IR Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Consumer IR Enable** 1: Enabled. 0: Disabled.

8.11.2 Consumer IR Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**CIR Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.11.3 Consumer IR Base Address LSB Register (Index=61h, Default=10h)

Bit	Description
7-3	**CIR Base Address LSB** **Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

8.11.4 Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**CIR Interrupt Level Select** Select the interrupt level [note1] for Consumer IR.

8.11.5 Consumer IR Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-1	**Reserved** with default "00h".
0	1: IRQ sharing. 0: Normal.

8.12 MIDI Port Configuration Registers (LDN=08h)

8.12.1 MIDI Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**MIDI Port Enable** 1: Enabled. 0: Disabled.

8.12.2 MIDI Port Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**MIDI Base Address MSB** **Read/write**, mapped as Base Address[11:8].

8.12.3 MIDI Port Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-1	**MIDI Base Address LSB** **Read/write**, mapped as Base Address[7:3].
0	**Read only** as "000b".

8.12.4 MIDI Port Interrupt Level Select (Index=70h, Default=0Ah)

Bit	Description
7-4	**Reserved** with default "0h".
3-0	**MIDI Port Interrupt Level Select** Select the interrupt level [note1] for MIDI port.

8.12.5 MIDI Port Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-6	**MID_IN Location Select** 00: Pin 85. Please refer to Section 6 (default) 01: Pin 79 10: Pin 74 11: Pin 7
5-4	**MID_OUT Location Select** 00: Pin 84. Please refer to Section 6 (default) 01: Pin 78 10: Pin 73 11: Pin 8
3	**FIFO Disable** 0: Enabled (default). 1: Disabled.
2-1	**Receive FIFO Trigger Level** 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
0	**MIDI Port Interrupt Mode Select** 0: Normal (default). 1: IRQ sharing.

Note 1: **Interrupt Level Mapping**

Fh-Dh: not valid
Ch: IRQ12
.
.
3h: IRQ3
2h: not valid
1h: IRQ1
0h: no interrupt selected

Note 2: **DMA Channel Mapping**

7h-5h: not valid
4h: no DMA channel selected
3h: DMA3
2h: DMA2
1h: DMA1
0h: DMA0

Note 3: **Location Mapping Table**

Location	Description
001 000	GP10 (pin 7)
001 001	GP11 (pin 8)
001 010	GP12 (pin 9)
001 011	GP13 (pin 10)
001 100	GP14 (pin 11)
001 101	GP15 (pin 12)
001 110	GP16 (pin 13)
001 111	GP17 (pin 14)
010 000	GP20 (pin 16)
010 001	GP21 (pin 17)
010 010	GP22 (pin 18)
010 011	GP23 (pin 19)
010 100	GP24 (pin 20)
010 101	GP25 (pin 21)
010 110	GP26 (pin 22)
010 111	GP27 (pin 23)
011 000	GP30 (pin 24)
011 001	GP31 (pin 25)
011 010	GP32 (pin 26)
011 011	GP33 (pin 27)
011 100	GP34 (pin 28)
011 101	GP35 (pin 29)

Note 3: **Location Mapping Table [cont'd]**

Location	Description
011 110	GP36 (pin 30)
011 111	GP37 (pin 31)
100 000	GP40 (pin 49)
100 001	GP41 (pin 50)
100 010	GP42 (pin 51)
100 011	GP43 (pin 52)
100 100	GP44 (pin 53)
100 101	GP45 (pin 54)
100 110	GP46 (pin 55)
100 111	GP47 (pin 56)
101 000	GP50 (pin 32)
101 001	GP51 (pin 33)
101 010	GP52 (pin 34)
101 011	GP53 (pin 47)
101 100	GP54 (pin 48)
101 101	GP55 (pin 73)
101 110	GP56 (pin 74)
101 111	GP57 (pin 75)
110 000	GP60 (pin 78), powered by VCCH
110 001	GP61 (pin 79), powered by VCCH
110 010	GP62 (pin 80), powered by VCCH
110 011	GP63 (pin 81), powered by VCCH
110 100	GP64 (pin 82), powered by VCCH
110 101	GP65 (pin 83), powered by VCCH
110 110	GP66 (pin 84), powered by VCCH
110 111	GP67 (pin 85), powered by VCCH
else	Reserved

9. Functional Description

9.1 LPC Interface

The IT8705F supports the peripheral site of the LPC I/F as described in the LPC Interface Specification Rev.1.0 (Sept. 29,1997). In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK (PCICLK)), the IT8705F also supports LDRQ#, SERIRQ and PME#.

9.1.1 LPC Transactions

The IT8705F supports some parts of the cycle types described in the LPC I/F specification. Memory read and Memory write cycles are used for the Flash I/F. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Super I/O module processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will make reactions according to the DMA requests from the DMA devices in the Super I/O modules, and decides whether to ignore the current transaction or not.

The FDC and ECP are 8-bit DMA devices, so if the LPC host initializes a DMA transaction with data size of 16/32 bits, the LPC interface will process the first 8-bit data and response with a SYNC ready (0000b) which will terminate the DMA burst. The LPC interface will then re-issue another LDRQ# message to assert DREQn after finishing the current DMA transaction.

9.1.2 LDRQ# Encoding

The Super I/O module provides two DMA devices: the FDC and the ECP. The LPC Interface provides LDRQ# encoding to reflect the DREQ[3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to track DMA requests rapidly. But, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there is at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages, and sends those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

9.2 Serialized IRQ

The IT8705F conforms to the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature, and is able to interface with most PC chipsets. The IT8705F encodes the parallel interrupts to an SERIRQ which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

9.2.1 Continuous Mode

When in the continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the Turn-around State of current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events, even though no IRQn status is changed. The SERIRQ enter the continuous mode following a system reset.

9.2.2 Quiet Mode

In the Quiet mode, when one SIRQ Slave detects its input IRQn/events have been changed, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence. In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity means low mode power consumption.

9.2.3 Waveform Samples of SERIRQ Sequence

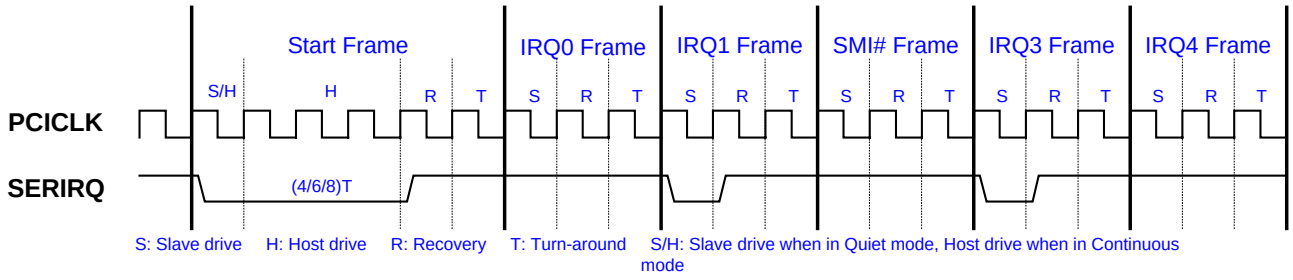


Figure 9-1. Start Frame Timings

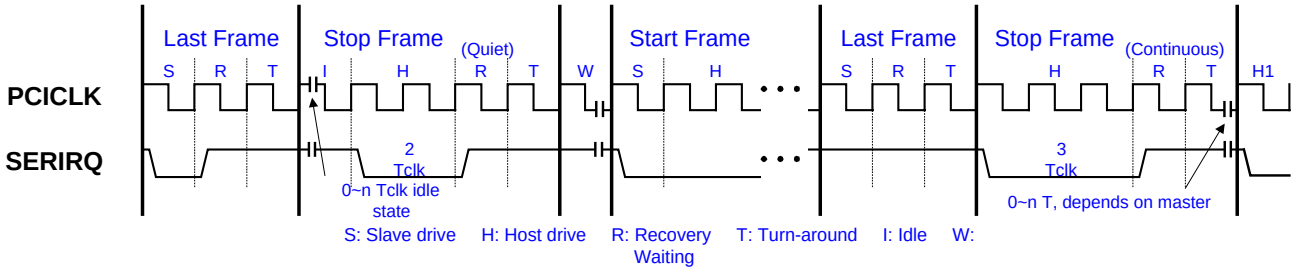


Figure 9-2. Stop Frame Timings

9.2.4 SERIRQ Sampling Slot

Slot Number	IRQn / Events	# of Clocks Past Start	IT8705F
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32-22	Unassigned	95 / 65	-

9.3 General Purpose I/O

The IT8705F provides six sets of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection registers (Index=25h, 26h, 27h, 28h, 29h and 2Ah of the Global Configuration Registers) are set. GPIO function includes the simple I/O function and alternate function, and the function selection is determined by the Simple I/O Enable Registers (LDN=05h, Index=C0h, C1h, C2h, C3h and C4h).

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. The accessed I/O ports are programmable. Base Address is programmed on the GPIO Simple I/O Base Address LSB & MSB registers (LDN=05h, Index=60h and 61h).

The Panel Button De-bounce is an input function. After the panel button de-bounce is enabled, a related status bit will be set when an active low pulse is detected on a GPIO pin. The status bits will be cleared by writing “1” to them. Panel Button De-bounce Interrupt will be issued if any one of the status bit is set. However, the new setting status will not issue another interrupt unless the previous status bit is cleared before being set.

The SMI# is a non-maskable interrupt dedicated to the transparent power management. It consists of different enabled interrupts generated from each of the functional blocks in the IT8705F. The interrupts redirect the SMI# output via the SMI# Control Register. The SMI# Status Register 1 is used to read the status of the SMI input events. All the SMI# status register bits can be cleared when the corresponding source events become invalidated. These bits can be cleared by writing “1” to themselves. The SMI# event can be programmed as pulse mode or level mode whenever an SMI# event occurs. The logic equation of the SMI# event is described below:

SMI# event = (EN_FIRQ and FIRQ) or (EN_S1IRQ and S1IRQ) or (EN_S2IRQ and S2IRQ) or (EN_PIRQ and PIRQ) or (EN_EC and EC_SMI) or (EN_CIRIRQ or CIRIRQ) or (EN_MIDIIRQ or MIDIIRQ).

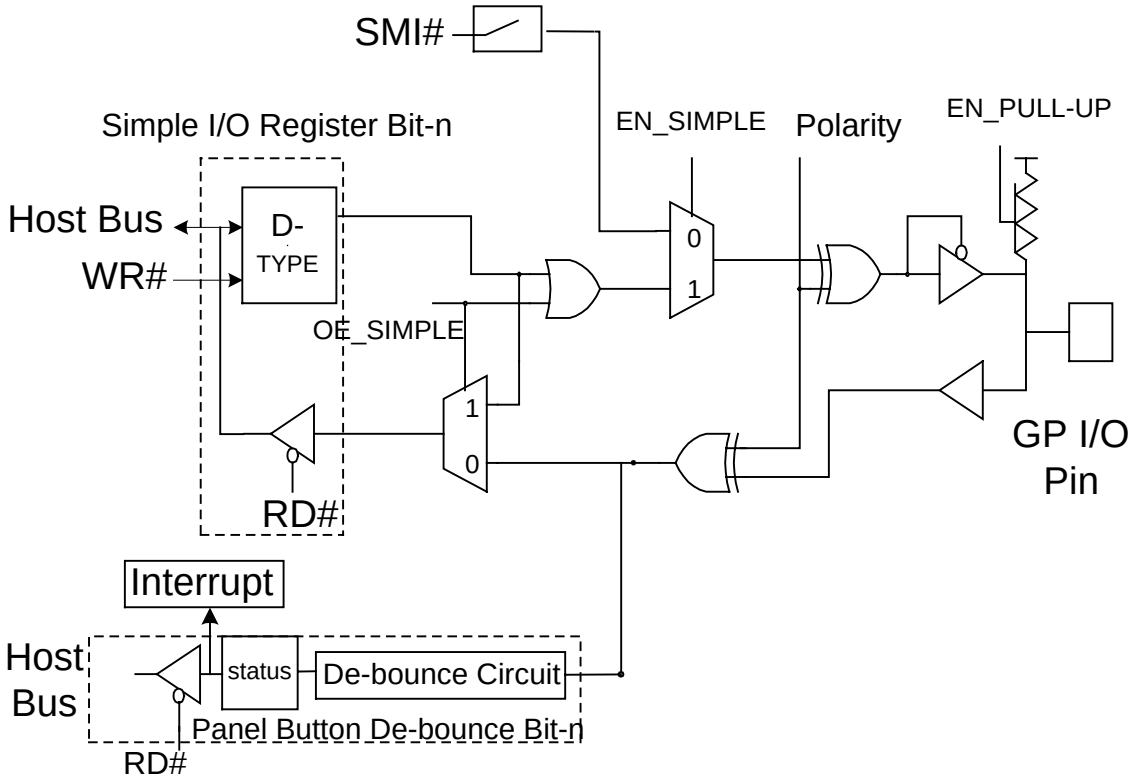


Figure 9-3. General Logic of GPIO Function

9.4 Power Management Event (PME#)

PME# is used to wake up the system from low-power states (S1-S5). There are three types of PME# events: RI1#, RI2# and CIR events. RI1# and RI2# are Ring Indicator of Modem status at ACPI S1 or S2. A falling edge on these pins issues PME# events if the enable bits are set.

A CIR event is generated if the input CIR RX pattern is the same as the previous stored pattern stored at PME Special Code Index and Data Registers (LDN=04h, Index=F5h, and F6h). The total maximum physical codes are nineteen bytes (from Index 20h to 32h). The first byte (Index 20h) is used to specify the pattern length in bytes. Bits[7:0] are used when VCC is ON; and bits[3:0] when VCC goes OFF. The length represented in each 4 bits will be incremented by 3 internally as the actual length to be compared. For most of the CIR protocols, the first several bytes are always the same for each key (or pattern). The differences are always placed in the last several bytes. Thus, the system designer can program the IT8705F to generate a CIR PME# event as any keys when VCC is ON and a special key (i.e. POWER-ON) when VCC power goes OFF.

9.5 Environment Controller (Enhanced Hardware Monitor and Fan Controller)

9.5.1 Overview

The Environment Controller (EC), built in the IT8705F, includes eight voltage inputs, three temperature sensor inputs, three Fan Tachometer inputs, and three sets of advanced Fan Controllers. The EC monitors the hardware environment and executes environmental control for personal computers.

The IT8705F contains an 8-bit ADC (Analog-to-Digital Converter), responsible for monitoring the voltages and temperatures. The ADC converts the analog inputs, ranging from 0V to 4.096V, to 8-bit digital bytes. Thanks to the additional external components, the analog inputs are able to monitor different voltage ranges, in addition to monitoring the fixed input range of 0V to 4.096V. The temperature sensor inputs can be converted to 8-bit digital bytes, and monitor the temperature around the thermistors or thermal diode. A built-in ROM is also provided to adjust the non-linear characteristics of thermistors.

Fan Tachometer inputs are digital inputs with an acceptable range of 0V to 5V, and are responsible for measuring the Fan's tachometer pulse periods. FAN_TAC1 and FAN_TAC2 are equipped with programmable divisors, and can be used to measure different fan speed ranges. FAN_TAC3 is equipped with the fixed divisor, and can only be used in the default range.

The EC of the IT8705F provides multiple internal registers and an interrupt generator for programmers to monitor the environment and control the FANs.

9.5.2 Interfaces

LPC Bus: The Environment Controller of the IT8705F decodes two addresses.

Table 9-1. Address Map on the ISA Bus

Register or Ports	Address
Address register of the EC	Base+05h
Data register of the EC	Base+06h

Note 1. The Base Address is determined by the Logical Device configuration registers of the Environment Controller (LDN=04h, registers index= 60h, 61h).

To access an EC register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

The BUSY bit (bit 7) in the address register (Base+05h) will be set during the ISA driver access. If the BUSY bit is set, it means an ISA driver is accessing, and other drivers are limited to reading the address register (Base+05h) only. These ISA drivers can only access the address register after the BUSY bit is cleared. By checking this bit status before accessing the address register, multiple ISA drivers can access the EC at one time, and are not required to communicate with each other.

9.5.3 Registers

9.5.3.1 Address Port (Base+05h, Default=00h):

Bit	Description
7	**Outstanding; Read only** This bit is set when a data write is performed to Address Port via the LPC Bus.
6-0	Index: Internal Address of RAM and Registers.

Table 9-2. Environment Controller Registers

Index	R/W	Default	Registers or Action
00h	R/W	08h	Configuration
01h	R	00h	Interrupt Status 1
02h	R	00h	Interrupt Status 2
03h	R	00h	Interrupt Status 3
04h	R/W	00h	SMI# Mask 1
05h	R/W	00h	SMI# Mask 2
06h	R/W	00h	SMI# Mask 3
07h	R/W	00h	Interrupt Mask 1
08h	R/W	00h	Interrupt Mask 2
09h	R/W	00h	Interrupt Mask 3
0Ah	R	-	Reserved Register
0Bh	R/W	09h	Fan Tachometer Divisor Register
0Ch	R/W	00h	Fan Tachometer 16-bit Counter Enable Register
0Dh	R	-	Fan Tachometer 1 Reading Register
0Eh	R	-	Fan Tachometer 2 Reading Register
0Fh	R	-	Fan Tachometer 3 Reading Register
10h	R/W	-	Fan Tachometer 1 Limit Register
11h	R/W	-	Fan Tachometer 2 Limit Register
12h	R/W	-	Fan Tachometer 3 Limit Register
13h	R/W	00h	Fan Controller Main Control Register
14h	R/W	00h	FAN_CTL Control Register
15h	R/W	00h	FAN_CTL1 PWM Control Register
16h	R/W	00h	FAN_CTL2 PWM Control Register
17h	R/W	00h	FAN_CTL3 PWM Control Register
18h	R	-	Fan Tachometer 1 Extended Reading Register
19h	R	-	Fan Tachometer 2 Extended Reading Register
1Ah	R	-	Fan Tachometer 3 Extended Reading Register
1Bh	R/W	-	Fan Tachometer 1 Extended Limit Register

Table9-3. Environment Controller Registers[cont'd]

Index	R/W	Default	Registers or Action
1Ch	R/W	-	Fan Tachometer 2 Extended Limit Register
1Dh	R/W	-	Fan Tachometer 3 Extended Limit Register
20h	R	-	VIN0 Voltage Reading Register
21h	R	-	VIN1 Voltage Reading Register
22h	R	-	VIN2 Voltage Reading Register
23h	R	-	VIN3 Voltage Reading Register
24h	R	-	VIN4 Voltage Reading Register
25h	R	-	VIN5 Voltage Reading Register
26h	R	-	VIN6 Voltage Reading Register
27h	R	-	VIN7 Voltage Reading Register
28h	R	-	VBAT Voltage Reading Register
29h	R	-	TMPIN1 Temperature Reading Register
2Ah	R	-	TMPIN2 Temperature Reading Register
2Bh	R	-	TMPIN3 Temperature Reading Register
30h	R/W	-	VIN0 High Limit Register
31h	R/W	-	VIN0 Low Limit Register
32h	R/W	-	VIN1 High Limit Register
33h	R/W	-	VIN1 Low Limit Register
34h	R/W	-	VIN2 High Limit Register
35h	R/W	-	VIN2 Low Limit Register
36h	R/W	-	VIN3 High Limit Register
37h	R/W	-	VIN3 Low Limit Register
38h	R/W	-	VIN4 High Limit Register
39h	R/W	-	VIN4 Low Limit Register
3Ah	R/W	-	VIN5 High Limit Register
3Bh	R/W	-	VIN5 Low Limit Register
3Ch	R/W	-	VIN6 High Limit Register
3Dh	R/W	-	VIN6 Low Limit Register
3Eh	R/W	-	VIN7 High Limit Register
3Fh	R/W	-	VIN7 Low Limit Register
40h	R/W	-	TMPIN1 High Limit Register
41h	R/W	-	TMPIN1 Low Limit Register
42h	R/W	-	TMPIN2 High Limit Register
43h	R/W	-	TMPIN2 Low Limit Register

Table9-4. Environment Controller Registers[cont'd]

Index	R/W	Default	Registers or Action
44h	R/W	-	TMPIN3 High Limit Register
45h	R/W	-	TMPIN3 Low Limit Register
48h	R/W	-	Reserved
50h	R/W	00h	ADC Voltage Channel Enable Register
51h	R/W	00h	ADC Temperature Channel Enable Register
52h	R/W	7Fh	TMPIN1 Thermal Output Limit Register
53h	R/W	7Fh	TMPIN2 Thermal Output Limit Register
54h	R/W	7Fh	TMPIN3 Thermal Output Limit Register
56h	R/W	56h	Thermal Diode 1 Zero Degree Adjust Register
57h	R/W	56h	Thermal Diode 2 Zero Degree Adjust Register
58h	R	90h	ITE Vendor ID Register
59h	R/W	56h	Thermal Diode 3 Zero Degree Adjust Register
5Bh	R	12h	Core ID Register
5Ch	R/W	00h	Beep Event Enable Register
5Dh	R/W	00h	Beep Frequency Divisor of Fan Event Register
5Eh	R/W	00h	Beep Frequency Divisor of Voltage Event Register
5Fh	R/W	00h	Beep Frequency Divisor of Temperature Event Register
60h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of OFF Register
61h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers
62h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Full Speed Registers
63h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Start PWM Registers
64h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Control Registers
68h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of OFF Register
69h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers
6Ah	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Full Speed Registers
6Bh	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Start PWM Registers
6Ch	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Control Registers
70h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of OFF Register
71h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers
72h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Full Speed Registers
73h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Start PWM Registers
74h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Control Registers

9.5.3.2 Register Description

9.5.3.2.1Configuration Register (Index=00h, Default=18h)

Bit	R/W	Description
7	R/W	Initialization. A “1” restores all registers to their individual default values, except the Serial Bus Address register. This bit clears itself when the default value is “0.”
6	R/W	**Update VBAT Voltage Reading**
5	R/W	**COPEN# cleared; Write “1” to clear COPEN#**
4	R	**Read Only**, Always “1.”
3	R/W	INT_Clear. A “1” disables the SMI# and IRQ outputs with the contents of interrupt status bits remain unchanged.
2	R/W	**IRQ enables the IRQ Interrupt output**
1	R/W	SMI# Enable. A “1” enables the SMI# Interrupt output.
0	R/W	Start. A “1” enables the startup of monitoring operations while a “0” sends the monitoring operation in the STANDBY mode.

9.5.3.2.2 Interrupt Status Register 1 (Index=01h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-5	R	**Reserved**
4	R	A “1” indicates a Case Open event has occurred.
3	R	**Reserved**
2-0	R	A “1” indicates the FAN_TAC3-1 Count limit has been reached.

9.5.3.2.3 Interrupt Status Register 2 (Index=02h, Default=00h)

Reading this register will clear itself after the read operation is completed.

Bit	R/W	Description
7-0	R	A “1” indicates a High or Low limit of VIN7-0 has been reached.

9.5.3.2.4 Interrupt Status Register 3 (Index=03h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-3	R	**Reserved**
2-0	R	A “1” indicates a High or Low limit of Temperature 3-1 has been reached.

9.5.3.2.5 SMI# Mask Register 1 (Index=04h, Default=00h)

Bit	R/W	Description
7-6	R/W	**Reserved**
4	R/W	A “1” disables the Case Open Intrusion interrupt status bit for SMI#.
3	R/W	**Reserved**
2-0	R/W	A “1” disables the FAN_TAC3-1 interrupt status bit for SMI#.

9.5.3.2.6 SMI# Mask Register 2 (Index=05h, Default=00h)

Bit	R/W	Description
7-0	R/W	A "1" disables the VIN7-0 interrupt status bit for SMI#.

9.5.3.2.7 SMI# Mask Register 3 (Index=06h, Default=00h)

Bit	R/W	Description
7-3	R/W	**Reserved**
2-0	R/W	A "1" disables the Temperature 3-1 interrupt status bit for SMI#.

9.5.3.2.8 Interrupt Mask Register 1 (Index=07h, Default=00h)

Bit	R/W	Description
7-5	R/W	**Reserved**
4	R/W	A "1" disables the Case Open Intrusion interrupt status bit for IRQ.
3	R/W	**Reserved**
2-0	R/W	A "1" disables the FAN_TAC3-1 interrupt status bit for IRQ.

9.5.3.2.9 Interrupt Mask Register 2 (Index=08h, Default=00h)

Bit	R/W	Description
7-0	R/W	A "1" disables the VIN7-0 interrupt status bit for IRQ.

9.5.3.2.10 Interrupt Mask Register 3 (Index=09h, Default=00h)

Bit	R/W	Description
7-3	R/W	**Reserved**
2-0	R/W	A "1" disables the Temperature 3-1 interrupt status bit for IRQ.

9.5.3.2.11 Reserved Register (Index=0Ah)

9.5.3.2.12 Fan Tachometer Divisor Register (Index=0Bh, Default=09h)

Bit	R/W	Description
7	-	**Reserved**
6	R/W	**FAN_TAC3 Counter Divisor** 0: divided by 2 1: divided by 8
5-3	R/W	**FAN_TAC2 Counter Divisor** 000: divided by 1 100: divided by 16 001: divided by 2 101: divided by 32 010: divided by 4 110: divided by 64 011: divided by 8 111: divided by 128
2-0	R/W	**FAN_TAC1 Counter Divisor** 000: divided by 1 100: divided by 16 001: divided by 2 101: divided by 32 010: divided by 4 110: divided by 64 011: divided by 8 111: divided by 128

9.5.3.2.13 Fan Tachometer 16-bit Counter Enable Register (Index=0Ch, Default=00h)

Bit	R/W	Description
7-3	-	**Reserved**
2	R/W	**FAN_TAC3 16-bit Counter Divisor Enable.** 0: disable 1: enable.
1	R/W	**FAN_TAC2 16-bit Counter Divisor Enable.** 0: disable 1: enable.
0	R/W	**FAN_TAC1 16-bit Counter Enable.** 0: disable 1: enable.

9.5.3.2.14 Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)

Bit	R/W	Description
7-0	R	The number of counts of the internal clock per revolution.

9.5.3.2.15 Fan Tachometer 1-3 Limit Registers (Index=10h-12h)

Bit	R/W	Description
7-0	R/W	**Limit Value**

9.5.3.2.16 Fan Controller Main Control Register (Index=13h, Default=00h)

Bit	R/W	Description
7	R	**Reserved**
6-4	R/W	**FAN_TAC3-1 Enable** 0: disable 1: enable
3	R/W	**FAN_CTL Automatic mode full speed control.** 0: Full speeds of FAN_CTL1-3 automatic mode are independent. 1: All FAN_CTL1-3 will enter full speed when any temperature exceeds full Speed Temperature Limit
2-0	R/W	**FAN_CTL3-1 Output Mode Selection** 0: ON/OFF mode. 1: SmartGuardian mode.

9.5.3.2.17 FAN_CTL Control Register (Index=14h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN_CTL Polarity** 0: Active Low. 1: Active High
6-4	R/W	**PWM base clock select** 000: 48Mhz. 001: 24Mhz. 010: 12Mhz 011: 8Mhz 100: 6Mhz 101: 3Mhz 110: 1.5Mhz 111: 0.75Mhz
3	R/W	**PWM Minimum Duty Select** 0: 0 %. For a given PWM value, the actual duty is PWM/128 X 100%. 1: 20 %. For a given PWM value (not 00h), the actual duty is (PWM+32)/160 X 100%. If the given PWM value is 00h, the actual duty will be 0%
2-0	R/W	**FAN_CTL3-1 ON/OFF Mode Control** These bits are only available when the relative output modes are selected in ON/OFF mode. 0: OFF. 1: ON.

9.5.3.2.18 FAN_CTL1 PWM Control Register (Index=15h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN_CTL1 PWM mode Automatic/Software Operation Selection** 0: Software operation. 1: Automatic operation.
6-0	R/W	128 steps of PWM control when in Software operation (bit 7=0), or Temperature input selection when in Automatic operation (bit 7=1). Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.5.3.2.19 FAN_CTL2 PWM Control Register (Index=16h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN_CTL2 PWM mode Automatic/Software Operation Selection** 0: Software Operation 1: Automatic Operation
6-0	R/W	128 steps of PWM control when in Software operation (bit 7=0), or Temperature input selection when in Automatic operation (bit 7=1). Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.5.3.2.20 FAN_CTL3 PWM Control Register (Index=17h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN_CTL3 PWM mode Automatic/Software Operation Selection** 0: Software Operation 1: Automatic Operation
6-0	R/W	128 steps of PWM control when in Software operation (bit 7=0), or Temperature input selection when in Automatic operation (bit 7=1). Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.5.3.2.21 Fan Tachometer 1-3 Extended Reading Registers (Index=18h-1Ah)

Bit	R/W	Description
7-0	R	**The number of counts of the internal clock per revolution. [15:8]**

9.5.3.2.22 Fan Tachometer 1-3 Extended Limit Registers (Index=1Bh-1Dh)

Bit	R/W	Description
7-0	R	**Limit Value. [15:8]**

9.5.3.2.23 VIN7-VIN0 Voltage Reading Registers (Index=27h-20h)

Bit	R/W	Description
7-0	R	**Voltage Reading Values**

9.5.3.2.24 VBAT Voltage Reading Register (Index=28h)

Bit	R/W	Description
7-0	R	**VBAT Voltage Reading Value**

9.5.3.2.25 TMPIN3-1 Temperature Reading Registers (Index=2Bh-29h)

Bit	R/W	Description
7-0	R	**Temperature Reading Values**

9.5.3.2.25.1VIN7-0 High Limit Registers (Index=3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h)

Bit	R/W	Description
7-0	R/W	**High Limit Value**

9.5.3.2.26 VIN7-0 Low Limit Registers (Index=3Fh, 3Dh, 3Bh, 39h, 37h, 35h, 33h, 31h)

Bit	R/W	Description
7-0	R/W	**Low Limit Value**

9.5.3.2.27 TMPIN3-1 High Limit Registers (Index=44h, 42h, 40h)

Bit	R/W	Description
7-0	R/W	**High Limit Value**

9.5.3.2.28 TMPIN3-1 Low Limit Registers (Index=45h, 43h, 41h)

Bit	R/W	Description
7-0	R/W	**Low Limit value.**

9.5.3.2.29 ADC Voltage Channel Enable Register (Index=50h, Default=00h)

Bit	R/W	Description
7-0	R/W	**ADC VIN7-VIN0 Scan Enable**

9.5.3.2.30 ADC Temperature Channel Enable Register (Index=51h, Default=00h)

TMPIN3-1 cannot be enabled in both Thermal Resistor mode and Thermal Diode (Diode connected Transistor) mode.

Bit	R/W	Description
7-6	R/W	**Reserved**
5-3	R/W	TMPIN3-1 are enabled in Thermal Resistor mode.
2-0	R/W	TMPIN3-1 are enabled in Thermal Diode (or Diode-connected Transistor) mode.

9.5.3.2.31 TMPIN3-1 Thermal Output Limit Registers (Index=54h-52h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Thermal Output Limit Value.**

9.5.3.2.32 Thermal Diode Zero Degree Adjust 1 Register (Index=56h, Default=56h)

This register is **read only** unless the bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	**Thermal Diode 1 Zero Degree Voltage Value (default: 0.664V 156h).**

9.5.3.2.33 Thermal Diode Zero Degree Adjust 2 Register (Index=57h, Default=56h)

This register is **read only** unless the bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	**Thermal Diode 2 Zero Degree Voltage Value (default: 0.664V 156h).**

9.5.3.2.34 Vendor ID Register (Index=58h, Default=90h)

Bit	R/W	Description
7-0	R	**ITE Vendor ID. Read Only.**

9.5.3.2.35Thermal Diode Zero Degree 3 Adjust Register (Index=59h, Default=56h)

This register is **read only** unless the bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	**Thermal Diode 3 Zero Degree Voltage Value (default: 0.664V 156h).**

9.5.3.2.36 Code ID Register (Index=5Bh, Default=12h)

Bit	R/W	Description
7-0	R	**ITE Vendor ID. Read Only.**

9.5.3.2.37 Beep Event Enable Register (Index=5Ch, Default=00h)

Bit	R/W	Description
7	R/W	Thermal Diode Zero Degree Adjust register write enable.
6-3	R/W	**Reserved**
2	R/W	Enables Beep action when TMPINs exceed limit.
1	R/W	Enables Beep action when VINs exceed limit.
0	R/W	Enables Beep action when FAN_TACs exceed limit.

9.5.3.2.38 Beep Frequency Divisor of Fan Event Register (Index=5Dh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor. Tone=500/(bits[7:4]+1).**
3-0	R/W	**Frequency Divisor. Frequency=10K/(bits[3:0]+1).**

9.5.3.2.39 Beep Frequency Divisor of Voltage Event Register (Index=5Eh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor. Tone=500/(bits[7:4]+1).**
3-0	R/W	**Frequency Divisor. Frequency=10K/(bits[3:0]+1).**

9.5.3.2.40 Beep Frequency Divisor of Temperature Event Register (Index=5Fh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor. Tone=500/(bits[7:4]+1).**
3-0	R/W	**Frequency Divisor. Frequency=10K/(bits[3:0]+1).**

9.5.3.2.41 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of OFF Registers (Index=70h, 68h, 60h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan OFF.**

9.5.3.2.42 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers (Index=71h, 69h, 61h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan start.**

9.5.3.2.43 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Full Speed Registers (Index=72h, 6Ah, 62h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit value of Fan Full Speed**

9.5.3.2.44 FAN_CTL3-1 SmartGuardian Automatic Mode Start PWM Registers (Index=73h, 6Bh, 63h, Default=00h)

Bit	R/W	Description
7	R/W	**Reserved**
6-0	R/W	**Start PWM Value**

9.5.3.2.45 FAN_CTL3-1 SmartGuardian Automatic Mode Control Registers (Index=74h, 6Ch, 64h, Default=00h)

Bit	R/W	Description
7	R/W	**Temperature Smoothing.** This bit enables the temperature smoothing process for the Automatic Fan Control. 0: Disable 1: Enable
6	R/W	**Reserved**
5	R/W	**Fan Spin-up Feedback enables**. This bit enables FAN_TAC reading to stop the "spin-up" of FAN_CTL. 0: Disable 1: Enable.
4-3	R/W	**Fan Spin-up time.** When FAN_CTL is not ON/OFF mode, it will spin-up in full on (7Fh) when the tachometer reading register is higher than the minimum limit and the spin-up time does not expire (if bit5=1). 00: 0 seconds 01: 125 ms (+- 10%) 10: 325ms (+- 10%) 11: 1000ms (+- 10%).
2-0	R/W	**Slope PWM** 000: 0 PWM value/℃ 001: 1 PWM value/℃ 010: 2 PWM value/℃ 011: 4 PWM value/℃ 100: 8 PWM value/℃ 101: 16 PWM value/℃ 110: 32 PWM value/℃ 111: 64 PWM value/℃

9.5.4 Operation

9.5.4.1 Power On RESET and Software RESET

When the system power is first applied, the EC performs a "power on reset" on the registers which are returned to default values (due to system hardware reset), and the EC will acquire a monitored value before it goes inactive. The ADC is active to monitor the VBAT pin and then goes inactive. Except the function of the Serial Bus Interface Address register, a software reset (bit 7 of Configuration register) is able to accomplish all the functions as the hardware reset does.

9.5.4.2 Starting Conversion

The monitoring function in the EC is activated when the bit 3 of Configuration Register is cleared (low) and bit 0 of Configuration Register is set (high). Otherwise, several enable bits should be set to enable the monitoring function. Those enable bits are categorized into three groups: positive voltages, temperatures and FAN Tachometer inputs. Before the EC monitoring function can be used, the steps below should be followed:

1. Set the Limits
2. Set the interrupt Masks
3. Set the Enable bits

The EC monitoring process can then be started.

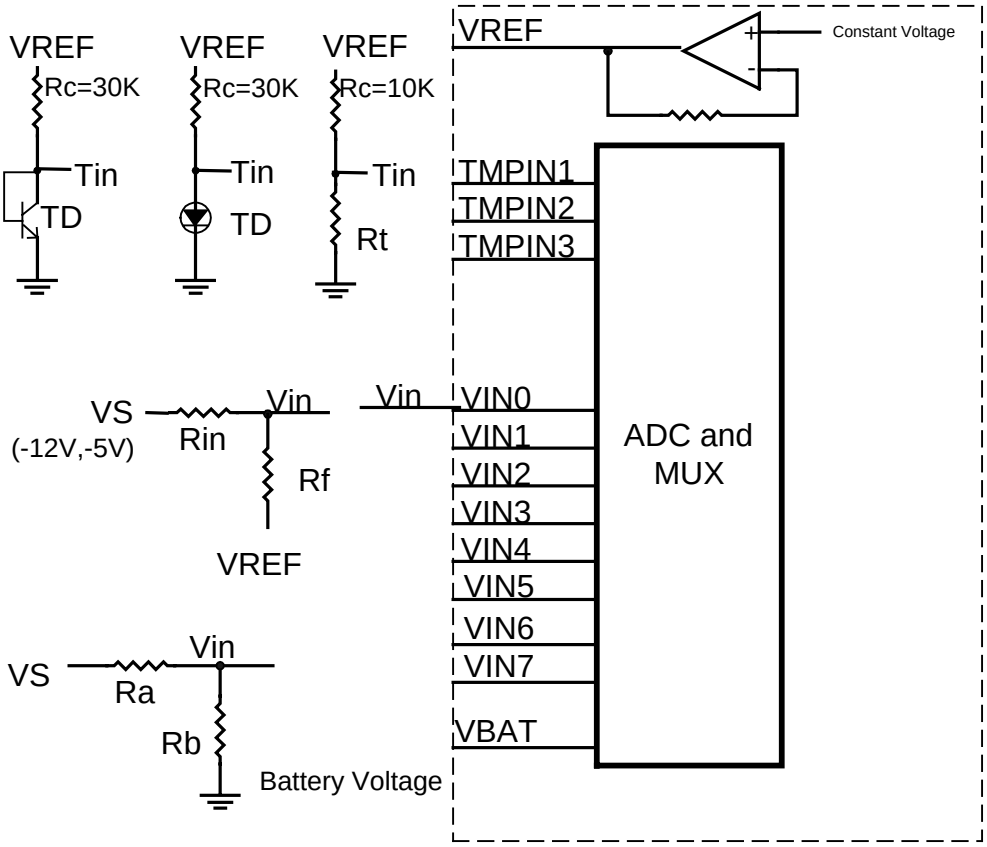


Figure 9-4. Application Example. Resistor should provide approximately 2V at the Analog Inputs.

9.5.4.3 Voltage and Temperature Inputs

The 8-bit ADC has a 16mV LSB, with a 0V to 4.096V input range. The 2.5V and 3.3V supplies of PC applications can be directly connected to the inputs. The 5V and 12V inputs should be divided into the acceptable range. When the divided circuit is used to measure the positive voltage, the recommended range for Ra and Rb is from 10KΩ to 100KΩ. The negative voltage can be measured by the same divider unless the divider is connected to VREF (constant voltage, 4.096V), not ground. The temperature measurement system of the EC converts the voltage of the TMPINs to 8-bit two's-complement. The system also includes an OP amp providing a constant voltage. It also additionally includes an external thermistor, a constant resistance, the ADC and a conversion table ROM.

Temperature	Digital Output Format	
	Binary	Hex
+ 125°C	01111101	7Dh
+ 25°C	00011001	19h
+ 1°C	00000001	01h
+ 0°C	00000000	00h
- 1°C	11111111	FFh
- 25°C	11100111	E7h
- 55°C	11001001	C9h

With the addition of the external application circuit, the actual voltages are calculated as below:

Positive Voltage: Vs = Vin X (Ra+Rb) / Rb
Negative Voltage: Vs = (1+Rin/Rf) X Vin – (Rin/Rf) X VREF

All the analog inputs are equipped with the internal diodes that clamp the input voltage exceeding the power supply and ground. But, the current limiting input resistor is recommended since no dividing circuit is available.

9.5.4.4 Layout and Grounding

A separate and low-impedance ground plane for analog ground is needed in achieving accurate measurement. The analog ground also provides a ground point for the voltage dividers including the temperature loops and analog components. Analog components such as voltage dividers, feedback resistors and the constant resistors of the temperature loops should be located as close as possible to the IT8705F. But, the thermistors of the temperature loops should be positioned within the measuring area. In addition, the power supply bypass, and the parallel combination of 10μF and 0.1μF bypass capacitors connected between VCC and analog ground, should also be located as close as possible to the IT8705F.

Due to the small differential voltage of thermal diode (diode-connected transistor), there are many PCB layout's recommendations:

- Position the sensor as close as possible
- Ground of the sensor should be directly short to GNDA with excellent noise immunity
- Keep trace away from the noise source. (High voltage, fast data bus, fast clock , CRTs …)
- Wider trace width (10 mil at least) and guard ground (flanking and under) are recommended
- Position 0.1μF bypass capacitors as close to IT8705F as possible

9.5.4.5 Fan Tachometer

The Fan Tachometer inputs gate a 22.5 kHz clock into an 8-bit or a 16-bit counter (maximum count=255 or 65535) for one period of the input signals. Several divisors, located in FAN Divisor Register, are provided for FAN_TAC1, FAN_TAC2, and FAN_TAC3, and are used to modify the monitoring range. Counts are based on 2 pulses per revolution tachometer output.

RPM = 1.35 X 10^6 / (Count X Divisor)

The maximum input signal range is from 0 to VCC. The additional application is needed to clamp the input voltage and current.

9.5.4.6 Interrupt of the EC

The EC generates interrupts as a result of each of its Limit registers on the analog voltage, temperature, and FAN monitor. All the interrupts are indicated in two Interrupt Status Registers. The IRQ and SMI# outputs have individual mask registers. These two Interrupts can also be enabled/disabled in the Configuration Register. The Interrupt Status Registers will be reset after being read. When the Interrupt Status Registers are cleared, the Interrupt lines will also be cleared. When a read operation is completed before the completion of the monitoring loop sequence, it indicates an Interrupt Status Register has been cleared. Due to slow monitoring sequence, the EC needs 1.5 seconds to allow all the EC Registers to be safely updated between completed read operations. When the bit 3 of the Configuration Register is set to high, the Interrupt lines are cleared and the monitoring loop will be stopped. The loop will resume when this bit is cleared.

All the analog voltage inputs have high and low Limit Registers that generate Interrupts, except that the FAN monitoring inputs only have low Limit Register to warn the host. The IT8705F provides two modes dedicated to temperature interrupts in the EC: "Interrupt" mode and "Comparator" mode.

In "Interrupt" mode, an interrupt will be generated whenever the temperature exceeds Th limit, and the corresponding Interrupt status bits will be set to high until being reset by reading Interrupt Status Register 3. Once an interrupt event has occurred by crossing Th limit, then after being reset, an interrupt will only occur again when the temperature goes below TL limit. Again, it will set the corresponding status bit to high until being reset by reading the Interrupt Status Register 3.

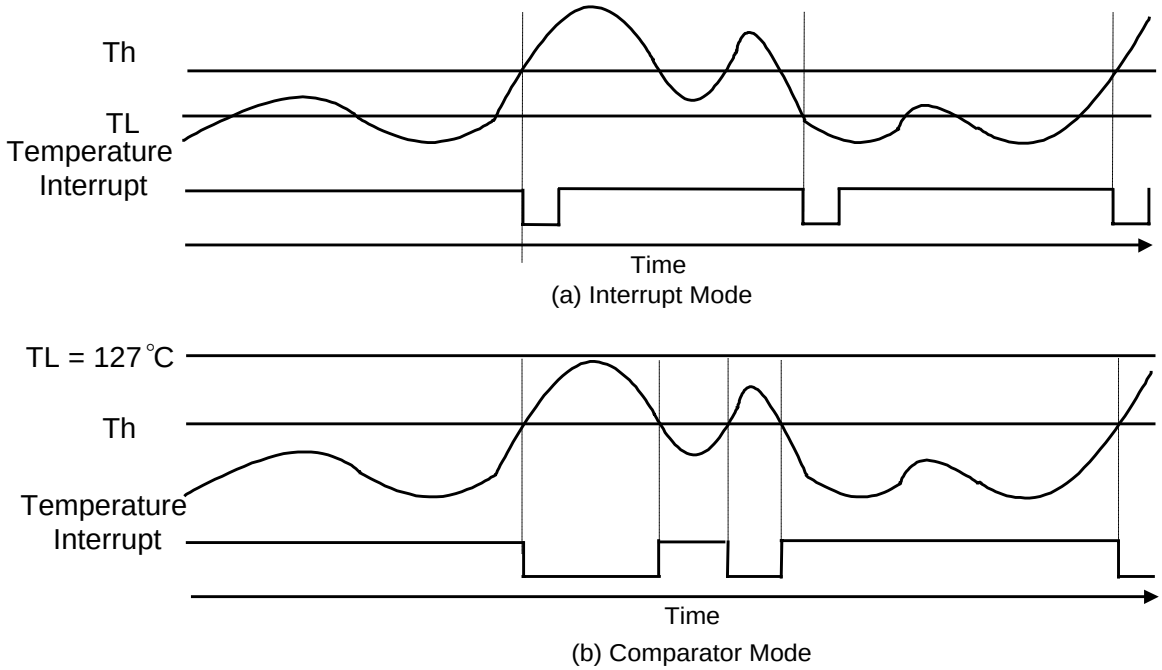


Figure 9-5. Temperature Interrupt Response Diagram

When the TL limit register is set to 127°C, the temperature interrupts enter the **"Comparator" mode**. In this mode, an interrupt will be generated whenever the temperature exceeds the Th limit. The interrupt will also be cleared by reading the Interrupt Status Register 3, but the interrupt will be set again following the completion of another measurement cycle. It will remain set until the temperature goes below the Th limit.

9.5.4.7 FAN Controller FAN_CTL's ON-OFF and SmartGuardian Modes

The IT8705F provides an advanced FAN Controller. Two modes are provided for each controller: ON_OFF and SmartGuardian modes. The former is a logical ON or OFF, and the latter is a PWM output. With the addition of external application circuits the FAN's voltage values can be varied easily. There are also two mode options in the SmartGuardian mode: software and automatic modes. In the software mode, the PWM value is subject to the changes in the values of bits 6-0 of FAN_CTL 1-3 PWM Control Registers (Index=15h, 16h, 17h). With the application circuits, FAN_CTL can generate 128 steps of voltage. So, the FAN_CTL 1-3 PWM Control Registers can vary the voltage by changing the PWM value. Fan speeds or other voltage control cooling device can be varied in 128 steps.

In the automatic mode, the PWM value is subject to the temperature inputs by linear changing. When the temperature exceeds a start limit, FAN_CTL spins in a start PWM value (LDN4, Index 73h, 6Bh, 63h). If the temperature increases X ℃, the PWM value will increase X * K. (K is a constant value, and is determined in bits 2-0 of FAN_CTL 3-1 SmartGuardian Automatic mode control registers). When the temperature decreases, the PWM value will decrease in the same ratio. When the temperature is lower than the start limit but larger than the OFF limit (LDN4, Index 70h, 68h, 60h), FAN_CTL will not stop, but keep in start PWM value until the temperature is lower than the OFF limit. (Hysteresis) When the temperature exceeds Full Speed limit (LDN4, Index 72h, 6Ah, 62h), FAN_CTL will be full on no matter it (start PWM value + X*K) is larger or smaller than full on PWM value (128).

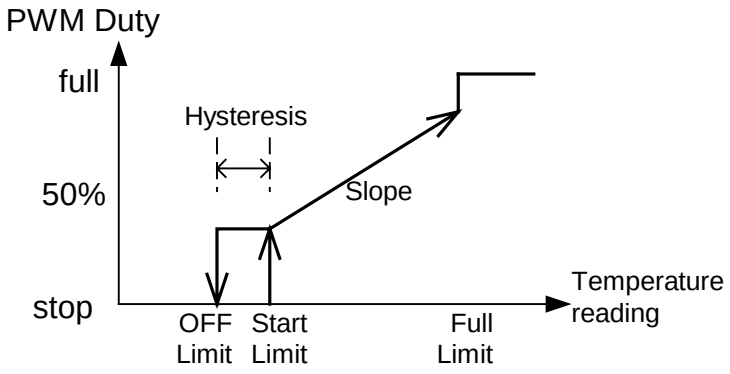


Figure 9-6. SmartGuardian Automatic Mode

9.6 Floppy Disk Controller (FDC)

9.6.1 Introduction

The Floppy Disk Controller provides the interface between a host processor and up to two floppy disk drives. It integrates a controller and a digital data separator with write precompensation, data rate selection logic, microprocessor interface, and a set of registers.

The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in PC/AT mode and supports 3-mode type drives. Additionally, the FDC is software compatible with the 82077.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD.

The controller manages data transfers using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution, and Result. Not all commands utilize all these three phases.

9.6.2 Reset

The IT8705F device implements both software and hardware reset options for the FDC. Either type of the resets will reset the FDC, terminating all operations and placing the FDC into an idle state. A reset during a write to the disk will corrupt the data and the corresponding CRC.

9.6.3 Hardware Reset (LRESET# Pin)

When the FDC receives a LRESET# signal, all registers of the FDC core are cleared (except those programmed by the SPECIFY command). To exit the reset state, the host must clear the DOR bit.

9.6.4 Software Reset (DOR Reset and DSR Reset)

When the reset bit in the DOR or the DSR is set, all registers of the FDC core are cleared. A reset performed by setting the reset bit in the DOR has higher priority over a reset performed by setting the reset bit in the DSR. In addition, to exit the reset state, the DSR bit is self-clearing, while the host must clear the DOR bit.

9.6.5 Digital Data Separator

The internal digital data separator is comprised of a digital PLL and associated support circuitry. It is responsible for synchronizing the raw data signal read from the floppy disk drive. The synchronized signal is used to separate the encoded clock from the data pulses.

9.6.6 Write Precompensation

Write precompensation is a method that can be used to adjust the effects of bit shift on data as it is written to the disk. It is harder for the data separator to read data that has been subject to bit shifting. Soft read errors can occur due to such bit shifting. Write precompensation predicts where the bit shifting might occur within a data pattern and shifts the individual data bits back to their nominal positions. The FDC permits the selections of write precompensation via the Data Rate Select Register (DSR) bits 2 through 4.

9.6.7 Data Rate Selection

Selecting one of the four possible data rates for the attached floppy disks is accomplished by setting the Diskette Control Register (DCR) or Data Rate Select Register (DSR) bits to 0 and 1. The data rate is determined by the last value that is written to either the DCR or the DSR. When the data rate is set, the data separator clock is scaled appropriately.

9.6.8 Status, Data and Control Registers

9.6.8.1 Digital Output Register (DOR, FDC Base Address + 02h)

This is a **read/write** register. It controls drive selection and motor enables as well as a software reset bit and DMA enable. The I/O interface reset may be used at any time to clear the DOR's contents.

Table 9-3. Digital Output Register (DOR)

Bit	Symbol	R/W	Description
7-6	-	-	**Reserved**
5	MOTB EN	R/W	**Drive B Motor Enable** 0: Disable Drive B Motor. 1: Enable Drive B Motor.
4	MOTA EN	R/W	**Drive A Motor Enable** 0: Disable Drive A Motor. 1: Enable Drive A Motor.
3	DMAEN	R/W	**Disk Interrupt and DMA Enable** 0: Disable disk interrupt and DMA (DRQx, DACKx#, TC and INTx). 1: Enable disk interrupt and DMA.
2	RESET#	R/W	**FDC Function Reset** 0: Reset FDC Function. 1: Clear Reset of FDC Function. This reset does not affect the DSR, DCR or DOR.
1	-	-	**Reserved**
0	DVSEL	R/W	**Drive Selection** 0: Select Drive A. 1: Select Drive B.

9.6.8.2 Tape Drive Register (TDR, FDC Base Address + 03h)

This is a **read/write** register and is included for 82077 software compatibility. The contents of this register are not used internal to the device.

Table 9-4. Tape Drive Register (TDR)

Bit	Symbol	R/W	Description
7-2	-	-	**Undefined**
1-0	TP_SEL [1:0]	R/W	**Tape Drive Selection** TP_SEL[1:0] : Drive selected 00: None 01: 1 10: 2 11: 3

9.6.8.3 Main Status Register (MSR, FDC Base Address + 04h)

This is a **read only** register. It indicates the general status of the FDC, and is able to receive data from the host. The MSR should be read before each byte is sent to or received from the Data register, except when in DMA mode.

Table 9-5. Main Status Register (MSR)

Bit	Symbol	R/W	Description
7	RQM	RO	**FDC Request for Master** 0: The FDC is busy and cannot receive data from the host. 1: The FDC is ready and the host can transfer data.
6	DIO	RO	**Data I/O Direction** Indicate the direction of data transfer once a RQM has been set 0: Write. 1: Read.
5	NDM	RO	**Non-DMA Mode** This bit selects Non-DMA mode of operation 0: DMA mode selected. 1: Non-DMA mode selected. This mode is selected via the SPECIFY command during the Execution phase of a command.
4	CB	RO	**Diskette Control Busy** Indicate a command is in progress (the FDD is busy) 0: A command has been executed and the end of the Result phase has been reached. 1: A command is being executed.
3-2	-	-	**Reserved**
1	DBB	RO	**Drive B Busy** Indicate Whether Drive B is in the SEEK portion of a command 0: Not busy. 1: Busy.
0	DAB	RO	**Drive A Busy** Indicate Whether Drive A is in the SEEK portion of a command 0: Not busy. 1: Busy.

9.6.8.4 Data Rate Select Register (DSR, FDC Base Address + 04h)

This is a **write only** register. It is used to determine the data rate, amount of write precompensation, power down mode, and software reset. The data rate of the floppy controller is the most recent write of either the DSR or DCR. The DSR is unaffected by a software reset. The DSR can be set to 02h by a hardware reset, and the “02h” represents the default precompensation, and 250 Kbps in data transfer rate.

Table 9-6. Data Rate Select Register (DSR)

<table>
<tr><th>Bit</th><th>Symbol</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>S/W RESET</td><td>WO</td><td>Software Reset
Software Reset. It is active high and shares the same function with the RESET# of the DOR except that this bit is self-clearing.</td></tr>
<tr><td>6</td><td>POWER DOWN</td><td>WO</td><td>Power Down
When this bit is written with a “1”, the floppy controller is put into manual low power mode. The clocks of the floppy controller and data separator circuits will be turned off until a software reset or the Data Register or Main Status Register is accessed.</td></tr>
<tr><td>5</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>4-2</td><td>PRE-COMP 2-0</td><td>WO</td><td>Precompensation Select
These three bits are used to determine the value of write precompensation that will be applied to the WDATA# pin. Track 0 is the default starting track number, which can be changed by the CONFIGURE command for precompensation.
<table>
<tr><th>PRE_COMP</th><th>Precompensation Delay</th></tr>
<tr><td>111</td><td>0.0 ns</td></tr>
<tr><td>001</td><td>41.7 ns</td></tr>
<tr><td>010</td><td>83.3 ns</td></tr>
<tr><td>011</td><td>125.0 ns</td></tr>
<tr><td>100</td><td>166.7 ns</td></tr>
<tr><td>101</td><td>208.3 ns</td></tr>
<tr><td>110</td><td>250.0 ns</td></tr>
<tr><td>000</td><td>Default</td></tr>
</table>
Default Precompensation Delays
<table>
<tr><th>Data Rate</th><th>Precompensation Delay</th></tr>
<tr><td>1 Mbps</td><td>41.7 ns</td></tr>
<tr><td>500 Kbps</td><td>125.0 ns</td></tr>
<tr><td>300 Kbps</td><td>125.0 ns</td></tr>
<tr><td>250 Kbps</td><td>125.0 ns</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>DRATE1-0</td><td>WO</td><td>Data Rate Select
<table>
<tr><th>Bits 1-0</th><th>Data Transfer Rate</th></tr>
<tr><td>00</td><td>500 Kbps</td></tr>
<tr><td>01</td><td>300 Kbps</td></tr>
<tr><td>10</td><td>250 Kbps (default)</td></tr>
<tr><td>11</td><td>1 Mbps</td></tr>
</table></td></tr>
</table>

9.6.8.5 Data Register (FIFO, FDC Base Address + 05h)

This is an 8-bit **read/write** register. It transfers command information, diskette drive status information, and the result phase status between the host and the FDC. The FIFO consists of several registers in a stack, and only one register in the stack is permitted to transfer information or status to the data bus at a time.

Table 9-7. Data Register (FIFO)

Bit	Symbol	R/W	Description
7-0		R/W	**Data** Command information, diskette drive status, or Result phase status data.

9.6.8.6 Digital Input Register (DIR, FDC Base Address + 07h)

This is a **read only** register and shares this address with the Diskette Control Register (DCR).

Table 9-8. Digital Input Register (DIR)

Bit	Symbol	R/W	Description
7	DSKCHG	RO	**Diskette Change** Indicate the inverting value of the bit monitored from the input of the Floppy Disk Change pin (DSKCHG#).
6-0	-	-	**Undefined**

9.6.8.7 Diskette Control Register (DCR, FDC Base Address + 07h)

This is a **write only** register and shares this address with the Digital Input Register (DIR). The DCR register controls the data transfer rate for the FDC.

Table 9-9. Diskette Control Register (DCR)

Bit	Symbol	R/W	Description
7-2	-	-	**Reserved** Always 0.
1-0	DRATE1-0	WO	**Data Rate Select** **Bits 1-0** **Data Transfer Rate** 00 500 Kbps 01 300 Kbps 10 250 Kbps 11 1 Mbps

9.6.9 Controller Phases

The FDC handles data transfers and control commands in three phases: Command, Execution and Result. Not all commands utilize all these three phases.

9.6.9.1 Command Phase

Upon reset, the FDC enters the Command phase and is ready to receive commands from the host. The host must verify that MSR bit 7 (RQM) = 1 and MSR bit 6 (DIO) = 0, indicating the FDC is ready to receive data. For each command, a defined set of command codes and parameter bytes must be transferred to the FDC in a given order. See sections 9.6.11 and 9.6.12 for details on the various commands. RQM is set false (0) after each byte read cycle, and set true (1) when a new parameter byte is required. The Command phase is completed when this set of bytes has been received by the FDC. The FDC automatically enters the next controller phase and the FIFO is disabled.

9.6.9.2 Execution Phase

Upon the completion of the Command phase, the FDC enters the Execution phase. It is in this phase that all data transfers occur between the host and the FDC. The SPECIFY command indicates whether this data transfer occurs in DMA or non-DMA mode. Each data byte is transferred via an IRQx or DRQx# based upon the DMA mode. On reset, the CONFIGURE command can automatically enable or disable the FIFO. The Execution phase is completed when all data bytes have been received. If the command executed does not require a Result phase, the FDC is ready to receive the next command.

9.6.9.3 Result Phase

For commands that require data written to the FIFO, the FDC enters the Result phase when the IRQ or DRQ is activated. The MSR bit 7 (RQM) and MSR bit 6 (DIO) must equal to 1 to read the data bytes. The Result phase is completed when the host has read each of the defined set of result bytes for the given command. Right after the completion of the phase, RQM is set to 1, DIO is set to 0, and the MSR bit 4 (CB) is cleared, indicating the FDC is ready to receive the next command.

9.6.9.4 Result Phase Status Registers

For commands that contain a Result phase, these **read only** registers indicate the status of the most recently executed command.

Table 9-10. Status Register 0 (ST0)

Bit	Symbol	R/W	Description
7-6	IC	RO	**Interrupt Code** 00: Execution of the command has been completed correctly 01: Execution of the command began, but failed to complete successfully 10: INVALID command 11: Execution of the command was not completed correctly, due to a polling error
5	SE	RO	**Seek End** The FDC executed a SEEK or RE-CALIBRATE command.
4	EC	RO	**Equipment Check** The TRK0# pin was not set after a RE-CALIBRATE command was issued.
3	NU	RO	**Not Used**
2	H	RO	**Head Address** The current head address.
1	DSB	RO	**Drive B selected** Drive B selected.
0	DSA	RO	**Drive A selected** Drive A selected.

Table 9-11. Status Register 1 (ST1)

Bit	Symbol	R/W	Description
7	EN	RO	**End of Cylinder** Indicate the FDC attempted to access a sector beyond the final sector of the track. This bit will be set if the Terminal Count (TC) signal is not issued after a READ DATA or WRITE DATA command.
6	-	-	**Unused.** Always “0”.
5	DE	RO	**Data Error** A CRC error occurred in either the ID field or the data field of a sector.
4	OR	RO	**Overrun/ Underrun** An overrun on a READ operation or underrun on a WRITE operation occurs when the FDC is not serviced by the CPU or DMA within the required time interval.
3	-	-	**Reserved.** Always "0".
2	ND	RO	**No Data** No data is available to the FDC when either of the following conditions is met: The floppy disk cannot find the indicated sector while the READ DATA or READ DELETED DATA commands are executed While executing a READ ID command, an error occurs upon reading the ID field while executing a READ A TRACK command, the FDC cannot find the starting sector
1	NW	RO	**Not Writeable** Set when a WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK command is being executed on a write-protected diskette.
0	MA	RO	**Missing Address Mark** This flag bit is set when either of the following conditions is met: The FDC cannot find a Data Address Mark or a Deleted Data Address Mark on the specified track The FDC cannot find any ID address on the specified track after two index pulses are detected from the INDEX# pin

Table 9-12. Status Register 2 (ST2)

Bit	Symbol	R/W	Description
7	-	-	**Unused.** Always "0".
6	CM	RO	**Control Mark** This flag bit is set when either of the following conditions is met: 1. The FDC finds a Deleted Data Address Mark during a READ DATA command 2. The FDC finds a Data Address Mark during a READ DELETED DATA command
5	DD	RO	**Data Error in Data Field** This flag bit is set when a CRC error is found in the data field.
4	WC	RO	**Wrong Cylinder** This flag bit is set when the track address in the ID field is different from the track address specified in the FDC.
3	SH	RO	**Scan Equal Hit** This flag bit is set when the condition of "equal" is satisfied during a SCAN command.

Table 9-15. Status Register 2 (ST2)[cont'd]

Bit	Symbol	R/W	Description
2	SN	RO	**Scan Not Satisfied** This flag bit is set when the FDC cannot find a sector on the cylinder during a SCAN command.
1	BC	RO	**Bad Cylinder** This flag bit is set when the track address equals "FFh" and is different from the track address in the FDC.
0	MD	RO	**Missing Data Address Mark** This flag bit is set when the FDC cannot find a Data Address Mark or Deleted Data Address Mark.

Table 9-13. Status Register 3 (ST3)

Bit	Symbol	R/W	Description
7	FT	RO	**Fault** Indicate the current status of the Fault signal from the FDD.
6	WP	RO	**Write Protect** Indicate the current status of the Write Protect signal from the FDD.
5	RDY	RO	**Ready** Indicate the current status of the Ready signal from the FDD.
4	TK0	RO	**Track 0** Indicate the current status of the Track 0 signal from the FDD.
3	TS	RO	**Two Side** Indicate the current status of the Two Side signal from the FDD.
2	HD	RO	**Head Address** Indicate the current status of the Head Select signal to the FDD.
1-0	US1, US0	RO	**Unit Select** Indicate the current status of the Unit Select signals to the FDD.

9.6.10 Command Set

The FDC utilizes a defined set of commands to communicate with the host. Each command is comprised of a unique first byte, which contains the op-code, and a series of additional bytes, which contain the required set of parameters and results. The op-code byte indicates to the FDC how many additional bytes should be expected for the command being written. The descriptions use a common set of parameter byte symbols, which are presented in Table 9-14. The FDC commands may be executed whenever the FDC is in the Command phase. The FDC checks to see that the first byte is a valid command and, if so, proceeds. An interrupt is issued if it is not a valid command.

Table 9-14. Command Set Symbol Descriptions

Symbol	Name	Description
C	Cylinder Number	The current/selected cylinder (track) number: 0 – 255.
D	Data	The data pattern to be written into a sector.
DC3–DC0	Drive Configuration Bit3-0	Designate which drives are perpendicular drives on the PERPENDICULAR MODE command.
DIR	Direction Control	**Read/write** Head Step Direction Control. 0 = Step Out; 1 = Step In.
DR0, DR1	Disk Drive Select	The selected drive number: 0 or 1.
DTL	Data Length	When N is defined as 00h, DTL designates the number of data bytes which users are going to read out or write into the Sector. When N is not 00h, DTL is undefined.
DFIFO	Disable FIFO	A “1” will disable the FIFO (default). A “0” will enable the FIFO.
EC	Enable Count	If EC=1, DTL of VERIFY command will be SC.
EIS	Enable Implied Seek	If EIS=1, a SEEK operation will be performed before executing any READ or WRITE command that requires the C parameter.
EOT	End of Track	The final sector number on a cylinder. During a READ or WRITE operation, the FDC stops data transfer after the sector number is equal to EOT.
GAP2	Gap 2 Length	By PERPENDICULAR MODE command, this parameter changes Gap 2 length in the format.
GPL	Gap Length	The length of Gap 3. During a FORMAT command, it determines the size of Gap 3.
H	Head Address	The Head number 0 or 1, as specified in the sector ID field. (H = HD in all command words.)
HD	Head	The selected Head number 0 or 1. It also controls the polarity of HDSEL#. (H = HD in all command words.)
HLT	Head Load Time	The Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The Head Unload Time after a READ or WRITE operation has been executed (16 to 240 ms in 16 ms increments).
LOCK		If LOCK=1, DFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command will not be affected by a software reset. If LOCK=0 (default), the above parameters will be set to their default values following a software reset.

Table 9-14. Command Set Symbol Descriptions [cont'd]

Symbol	Name	Description
MFM	FM or MFM Mode	If MFM is low, FM Mode (single density) is selected. If MFM is high, MFM Mode (double density) is selected.
MT	Multi-Track	If MT is high, a Multi-Track operation is to be performed. In this mode, the FDC will automatically start searching for sector 1 on side 1 after finishing a READ/WRITE operation on the last sector on side 0.
N	Number	The number of data bytes written into a sector, where: 00 :128 bytes (PC standard) 01 :256 bytes 02 :512 bytes … 07 :16 Kbytes
NCN	New Cylinder Number	A new cylinder number, which is to be reached as a result of the SEEK operation. Desired position of Head.
ND	Non-DMA Mode	When ND is high, the FDC operates in the non-DMA Mode.
OW	Overwrite	If OW=1, DC3-0 of the PERPENDICULAR MODE command can be modified. Otherwise, those bits cannot be changed.
PCN	Present Cylinder Number	The cylinder number at the completion of a SENSE INTERRUPT STATUS command. Position of Head at present time.
POLLD	Polling Disable	If POLLD=1, the internal polling routine is disabled.
PRETRK	Precompensation Starting Track Number	Programmable from track 0 –255.
R	Record	The sector number, which will be read or written.
RCN	Relative Cylinder Number	To determine the related cylinder offset from present cylinder as used by the RELATIVE SEEK command.
SC		The number of sectors per cylinder.
SK	Skip	If SK=1, the Read Data operation will skip sectors with a Deleted Data Address Mark. Or, the Read Deleted Data operation only accesses sectors with a Deleted Data Address Mark.
SRT	Step Rate Time	The Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives (F=1 ms, E=2 ms, etc.).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0–3 stand for one of four registers that store the status information after a command has been executed. This information is available during the Result phase after command execution. These registers should not be confused with the Main Status Register (selected by A_0 = 0). ST0–3 may be **read only** after a command has been executed and contain information associated with that particular command.
STP		If STP = 1 during a SCAN operation, the data in contiguous sectors are compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.

Table 9-15. Command Set Summary

READ DATA									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	MT	MFM	SK	0	0	1	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution.
	RO	H								
	RO	R								
	RO	N								

READ DELETED DATA									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	MT	MFM	SK	0	1	1	0	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution.
	RO	H								
	RO	R								
	RO	N								

READ A TRACK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	0	0	0	0	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and main system cylinder's contents from index hole to EOT.
Result	RO	ST0								Sector ID information before the command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

WRITE DATA									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	0	0	0	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

WRITE DELETED DATA									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	MT	MFM	0	0	1	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL								
Execution										Data transfer between the FDD and the main system.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

FORMAT A TRACK									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	0	MFM	0	0	1	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	N								Bytes/Sector
	WO	SC								Sectors/Cylinder
	WO	GPL								Gap 3
	WO	D								Filler Byte
Execution	WO	C								Input Sector Parameters per-sector
	WO	H								
	WO	R								
	WO	N								
Result	RO	ST0								FDC formats an entire cylinder
	RO	ST1								Status information after command execution
	RO	ST2								
	RO	Undefined								
	RO	Undefined								
	RO	Undefined								
	RO	Undefined								

SCAN EQUAL									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	SK	1	0	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	STP								
Execution										Data transferred from the system to controlle6r is compared to data read from disk.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

SCAN LOW OR EQUAL									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	MT	MFM	SK	1	1	0	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	STP								
Execution										Data transferred from the system to controller is compared to data read from disk.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

SCAN HIGH OR EQUAL									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	MT	MFM	SK	1	1	1	0	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	STP								
Execution										Data transferred from the system to controller is compared to data read from disk.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

VERIFY									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	MT	MFM	SK	1	0	1	1	0	Command Codes
	WO	EC	0	0	0	0	HDS	DR1	DR0	
	WO	C								Sector ID information before the command execution
	WO	H								
	WO	R								
	WO	N								
	WO	EOT								
	WO	GPL								
	WO	DTL/SC								
Execution										No data transfer takes place.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information after command execution
	RO	H								
	RO	R								
	RO	N								

READ ID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	MFM	0	0	1	0	1	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
Execution										The first correct ID information on the Cylinder is stored in the Data Register.
Result	RO	ST0								Status information after command execution
	RO	ST1								
	RO	ST2								
	RO	C								Sector ID information during execution phase
	RO	H								
	RO	R								
	RO	N								

CONFIGURE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	1	0	0	1	1	Configure Information
	WO	0	0	0	0	0	0	0	0	
	WO	0	EIS	DFIFO	POLLD	FIFOTHR				
		PRETRK								
Execution										

RE-CALIBRATE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	0	1	1	1	Command Codes
	WO	0	0	0	0	0	0	DR1	DR0	
Execution										Head retracted to Track 0

SEEK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	1	1	1	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	NCN								
Execution										Head is positioned over proper cylinder on diskette.

RELATIVE SEEK									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	1	DIR	0	0	1	1	1	1	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
	WO	RCN								
Execution										Head is stepped in or out a programmable number of tracks.

DUMPREG									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	0	0	0	0	1	1	1	0	Command Codes
Execution										Registers placed in FIFO
Result	RO	PCN-Drive 0								
	RO	PCN-Drive 1								
	RO	PCN-Drive 2								
	RO	PCN-Drive 3								
	RO	SRT				HUT				
	RO	HLT							ND	
	RO									
	RO	LOCK	0	DC3	DC2	DC1	DC0	GAP	WG	
	RO	0	DIS	DFIFO	POLLD	FIFOTHR				
	RO	PRETRK								

LOCK									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	LOCK	0	0	1	0	1	0	0	Command Codes
Result	RO	0	0	0	LOCK	0	0	0	0	

VERSION									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	0	0	0	1	0	0	0	0	Command Codes
Result	RO	1	0	0	1	0	0	0	0	Enhanced Controller

SENSE INTERRUPT STATUS									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	WO	0	0	0	0	1	0	0	0	Command Codes
Result	RO	ST0								Status information at the end of each SEEK operation
	RO	PCN								

SENSE DRIVE STATUS									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	0	1	0	0	Command Codes
	WO	0	0	0	0	0	HDS	DR1	DR0	
Result	RO	ST3								Status information about FDD

SPECIFY									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	0	0	0	1	1	Command Codes
	WO	SRT				HUT				
	WO	HLT							ND	

PERPENDICULAR MODE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	0	0	0	1	0	0	1	0	Command Codes
	WO	OW	0	DC3	DC2	DC1	DC0	GAP	WG	

INVALID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	WO	Invalid codes								INVALID Command Codes (NO-OP: FDC goes into standby state)
Result	RO	ST0								ST0 = 80h

9.6.11 Data Transfer Commands

All data transfer commands utilize the same parameter bytes (except for FORMAT A TRACK command) and return the same result data bytes. The only difference between them is the five bits (0–4) of the first byte.

9.6.11.1 READ DATA

The READ DATA command contains nine command bytes that place the FDC into the Read Data mode. Each READ operation is initialized by a READ DATA command. The FDC locates the sector to be read by matching ID Address Marks and ID fields from the command with the information on the diskette. The FDC then transfers the data to the FIFO. When the data from the given sector has been read, the READ DATA command is completed and the sector address is automatically incremented by 1. The data from the next sector is read and transferred to the FIFO in the same manner. Such a continuous read function is called a "Multi-Sector Read Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops sending data, but continues to read data from the current sector and checks the CRC bytes until the end of the sector is reached and the read operation is completed.

The sector size is determined by the N parameter value as calculated in the equation below:
Sector Size = $2^{(7+N\ value)}$ bytes.

The DTL parameter determines the number of bytes to be transferred. Therefore, if N = 00h, setting the sector size to 128 and the DTL parameter value is less than this, the remaining bytes will be read and checked for CRC errors by the FDC. If this occurs in a write operation, the remaining bytes will be filled with 0. If the sector size is not 128 (N > 00h), DTL should be set to FFh.

In addition to performing Multi-Sector Read operations, the FDC can perform Multi-Track Read operations. When the MT parameter is set, the FDC can read both sides of a disk automatically.

The combination of N and MT parameter values determines the amount of data that can be transferred during either type of READ operation. Table 9-16 shows the maximum data transfer capacity and the final sector the FDC reads based on these parameters.

Table 9-16. Effects of MT and N Bits

MT	N	Maximum Transfer Capacity	Final Sector Read from Disk
0	1	256 X 26 = 6656	26 on side 0 or side 1
1	1	256 X 52 = 13312	26 on side 1
0	2	512 X 15 = 7680	15 on side 0 or side 1
1	2	512 X 30 = 15360	15 on side 1
0	3	1024 X 8 = 8192	8 on side 0 or side 1
1	3	1024 X 16 = 16384	16 on side 1

9.6.11.2 READ DELETED DATA

The READ DELETED DATA command is the same as the READ DATA command, except that a Deleted Data Address Mark (as opposed to a Data Address Mark) is read at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.6.11.3 READ A TRACK

After receiving a pulse from the INDEX# pin, the READ A TRACK command reads the entire data field from each sector of the track as a continuous block. If any ID or Data Field CRC error is found, the FDC continues to read data from the track and indicates the error at the end. Because the Multi-Track [and Skip] operation[s] is[are] not allowed under this command, the MT and SK bits should be low (0) during the command execution.

This command terminates normally when the number of sectors specified by EOT has not been read. If, however, no ID Address Mark has been found by the second occurrence of the INDEX pulse, the FDC will set the IC code in the ST0 to 01, indicating an abnormal termination, and then finish the command.

9.6.11.4 WRITE DATA

The WRITE DATA command contains nine command bytes that place the FDC into the Write Data mode. Each WRITE operation is initialized by a WRITE DATA command. The FDC locates the sector to be written by reading ID fields and matching the sector address from the command with the information on the diskette. Then the FDC reads the data from the host via the FIFO and writes the data into the sector's data field. Finally, the FDC computes the CRC value, storing it in the CRC field, and increments the sector number (stored in the R parameter) by 1. The next data field is written into the next sector in the same manner. Such a continuous writes function is called a "Multi-Sector Write Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops writing data and fills the remaining data field with 0s. If a check of the CRC value indicates an error in the sector ID Field, the FDC will set the IC code in the ST0 to 01 and the DE bit in the ST1 to 1, indicating an abnormal termination, and then terminate the WRITE DATA command. The maximum data transfer capacity and the DTL, N, and MT parameters are the same as in the READ DATA command.

9.6.11.5 WRITE DELETED DATA

The WRITE DELETED DATA command is the same as the WRITE DATA command, except that a Deleted Data Address Mark (instead of a Data Address Mark) is written at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.6.11.6 FORMAT A TRACK

The FORMAT A TRACK command is used to format an entire track. Initialized by an INDEX pulse, it writes data to the Gaps, Address Marks, ID fields and Data fields according to the density mode selected (FM or MFM). The Gap and Data field values are controlled by the host-specified values programmed into N, SC, GPL, and D during the Command phase. The Data field is filled with the data byte specified by D. The four data bytes per sector (C, H, R, and N) needed to fill the ID field are supplied by the host. The C, R, H, and N values must be renewed for each new sector of a track. Only the R parameter value must be changed when a sector is formatted, allowing the disk to be formatted with non-sequential sector addresses. These steps are repeated until a new INDEX pulse is received, at which point the FORMAT A TRACK command is terminated.

9.6.11.7 SCAN

The SCAN command allows the data read from the disk to be compared with the data sent from the system. There are three SCAN commands:

SCAN EQUAL Disk Data = System Data

SCAN HIGH OR EQUAL Disk Data ≥ System Data

SCAN LOW OR EQUAL Disk Data ≤ System Data

The SCAN command execution continues until the scan condition has been met, or the EOT has been reached, or if TC is asserted. Read errors on the disk have the same error condition as the READ DATA command. If the SK bit is set, sectors with deleted data address marks are ignored. If all sectors read are skipped, the command terminates with bit 3 of the ST2 being set. The Result phase of the command is shown below:

Table 9-17. SCAN Command Result

Command	Status Register		Condition
	D2	D3	
SCAN EQUAL	0	1	Disk = System
	1	0	Disk ≠ System
SCAN HIGH OR EQUAL	0	1	Disk = System
	0	0	Disk > System
	1	0	Disk < System
SCAN LOW OR EQUAL	0	1	Disk = System
	0	0	Disk < System
	1	0	Disk > System

9.6.11.8 VERIFY

The VERIFY command is used to read logical sectors containing a Normal Data Address Mark from the selected drive without transferring the data to the host. This command acts like a READ DATA command except that no data is transferred to the host. This command is designed for post-format or post write verification. Data is read from the disk, as the controller checks for valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value. Because no data is transferred to the host, the TC (Terminal Count of DMA) cannot be used to terminate this command. An implicit TC will be issued to the FDC by setting the EC bit. This implicit TC will occur when the SC value has been decrement to 0. This command can also be terminated by clearing the EC bit and when the EOT value equals to the final sector to be checked.

Table 9-18. VERIFY Command Result

MT	EC	SC/EOT	Termination Result
0	0	SC = DTL EOT ≤ # Sectors per side	No Errors
0	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
0	1	SC ≤ # Sectors Remaining and EOT ≤ # Sectors per side	No Errors
0	1	SC > # Sectors Remaining or EOT > # Sectors per side	Abnormal Termination
1	0	SC = DTL EOT > # Sectors per side	No Errors
1	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
1	1	SC ≤ # Sectors Remaining and EOT ≤ # Sectors per side	No Errors
1	1	SC > # Sectors Remaining or EOT > # Sectors per side	Abnormal Termination

9.6.12 Control Commands

The control commands do not transfer any data. Instead they are used to monitor and manage the data transfer. Three of the Control commands generate an interrupt when finished — READ ID, RE-CALIBRATE and SEEK. It is strongly recommended that a SENSE INTERRUPT STATUS command be issued after these commands to capture their valuable interrupt information. The RE-CALIBRATE, SEEK, and SPECIFY commands do not return any result bytes.

9.6.12.1 READ ID

The READ ID command is used to find the actual recording head position. It stores the first readable ID field value into the FDC registers. If the FDC cannot find an ID Address Mark by the time a second INDEX pulse is received, an abnormal termination will be generated by setting the IC code in the ST0 to 01.

9.6.12.2 CONFIGURE

The CONFIGURE command determines some special operation modes of the controller. It needs not be issued if the default values of the controller meet the system requirements.
EIS: Enable Implied Seeks. A Seek operation is performed before a READ, WRITE, SCAN, or VERIFY commands.
0 = Disable (default).
1 = Enable.
DFIFO: Disable FIFO.
0 = Enable.
1 = Disable (default).
POLLD: Disable polling of the drives.
0 = Enable (default). When enabled, a single interrupt is generated after a reset.
1 = Disable.
FIFOTHR: The FIFO threshold in the execution phase of data transfer commands. They are programmable from 00 to 0F hex (1 bytes to 16 bytes). Defaults to one byte.
PRETRK: The Pre-compensation Start Track Number. They are programmable from track 0 to FF hex (track 0 to track 255). Defaults to track 0.

9.6.12.3 RE-CALIBRATE

The RE-CALIBRATE command retracts the FDC read/write head to the track 0 position, resetting the value of the PCN counter and checking the TRK0# status. If TRK0# is low, the DIR# pin remains low and step pulses are issued. If TRK0# is high, SE [and EC bits] of ST0 are set high, and the command is terminated. When TRK0# remains low for 79 step pulses, the RE-CALIBRATE command is terminated by setting SE and EC bits of ST0 high. Consequently, for disks that can accommodate more than 80 tracks, more than one RE-CALIBRATE command is required to retract the head to the physical track 0.

The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another RE-CALIBRATE command in parallel with the current command.

On power-up, software must issue a RE-CALIBRATE command to properly initialize the FDC and its attached drives.

9.6.12.4 SEEK

The SEEK command controls the FDC read/write head movement from one track to another. The FDC compares the current head position, stored in PCN, with NCN values after each step pulse to determine what direction to move the head, if required. The direction of movement is determined below:

PCN < NCN — Step In: Set DIR# signal to 1 and issues step pulses
PCN > NCN — Step Out: Set DIR# signal to 0 and issues step pulses
PCN = NCN — Terminate the command by setting the ST0 SE bit to 1

The impulse rate of step pulse is controlled by Stepping Rate Time (SRT) bit in the SPECIFY command. The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another SEEK command in parallel with the current command.

9.6.12.5 RELATIVE SEEK

The RELATIVE SEEK command steps the selected drive in or out in a given number of steps. The DIR bit is used to determine to step in or out. RCN (Relative Cylinder Number) is used to determine how many tracks to step the head in or out from the current track. After the step operation is completed, the controller generates an interrupt, but the command has no Result phase. No other command except the SENSE INTERRUPT STATUS command should be issued while a RELATIVE SEEK command is in progress.

9.6.12.6 DUMPREG

The DUMPREG command is designed for system run-time diagnostics, and application software development, and debug. This command has one byte of Command phase and 10 bytes of Result phase, which return the values of parameters set in other commands.

9.6.12.7 LOCK

The LOCK command allows the programmer to fully control the FIFO parameters after a hardware reset. If the LOCK bit is set to 1, the parameters DFIFO, FIFOTHR, and PRETRK in the CONFIGURE command are not affected by a software reset. If the bit is set to 0, those parameters are set to default values after a software reset.

9.6.12.8 VERSION

The VERSION command is used to determine the controller being used. In Result phase, a value of 90 hex is returned in order to be compatible with the 82077.

9.6.12.9 SENSE INTERRUPT STATUS

The SENSE INTERRUPT STATUS command resets the interrupt signal (IRQ) generated by the FDC, and identifies the cause of the interrupt via the IC code and SE bit of the ST0, as shown in Table 9-22.

It may be necessary to generate an interrupt when any of the following conditions occur:

- Before any Data Transfer or READ ID command
- After SEEK or RE-CALIBRATE commands (no result phase exists)
- When a data transfer is required during an Execution phase in the non-DMA mode

Table 9-19. Interrupt Identification

SE	IC Code	Cause of Interrupt
0	11	Polling.
1	00	Normal termination of SEEK or RE-CALIBRATE command.
1	01	Abnormal termination of SEEK or RE-CALIBRATE command.

9.6.12.10 SENSE DRIVE STATUS

The SENSE DRIVE STATUS command acquires drive status information. It has no Execution phase.

9.6.12.11 SPECIFY

The SPECIFY command sets the initial values for the HUT (Head Unload Time), HLT (Head Load Time), SRT (Step Rate Time), and ND (Non-DMA mode) parameters. The possible values for HUT, SRT, and HLT are shown in Table 9-20, Table 9-21 and Table 9-22 respectively. The FDC is operated in DMA or non-DMA mode based on the value specified by the ND parameters.

Table 9-20. HUT Values (ms)

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	128	256	426	512
1	8	16	26.7	32
…	…	…	…	…
E	112	224	373	448
F	120	240	400	480

Table 9-21. SRT Values (ms)

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	8	16	26.7	32
1	7.5	15	25	30
…	…	…	…	…
E	1	2	3.33	4
F	0.5	1	1.67	2

Table 9-22. HLT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
00	128	256	426	512
01	1	2	3.33	4
02	2	4	6.7	8
…	…	…	…	…
7E	126	252	420	504
7F	127	254	423	508

9.6.12.12 PERPENDICULAR MODE

The PERPENDICULAR MODE command is used to support the unique READ/WRITE/FORMAT commands of Perpendicular Recording disk drives (4 Mbytes unformatted capacity). This command configures each of the four logical drives as a perpendicular or conventional disk drive via the DC3-DC0 bits or with the GAP and WG control bits. Perpendicular Recording drives operate in "Extra High Density" mode at 1 Mbps, and are downward compatible with 1.44 Mbyte and 720 Kbyte drives at 500 Kbps (High Density) and 250 Kbps (Double Density) respectively. This command should be issued during the initialization of the floppy controller. Then, when a drive is accessed for a FORMAT A TRACK or WRITE DATA command, the controller adjusts the format or Write Data parameters based on the data rate. If WG and GAP are used (not set to 00), the operation of the FDC is based on the values of GAP and WG. If WG and GAP are set to 00, setting DCn to 1 will set drive n to Perpendicular mode. DC3-DC0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset.

Table 9-23. Effects of GAP and WG on FORMAT A TRACK and WRITE DATA Commands

GAP	WG	Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
0	0	Conventional	22 bytes	0 byte
0	1	Perpendicular (500 Kbps)	22 bytes	19 bytes
1	0	Reserved (Conventional)	22 bytes	0 byte
1	1	Perpendicular (1 Mbps)	41 bytes	38 bytes

Table 9-24. Effects of Drive Mode and Data Rate on FORMAT A TRACK and WRITE DATA Commands

Data Rate	Drive Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
250/300/500 Kbps	Conventional	22 bytes	0 byte
	Perpendicular	22 bytes	19 bytes
1 Mbps	Conventional	22 bytes	0 byte
	Perpendicular	41 bytes	38 bytes

9.6.12.13 INVALID

The INVALID command indicates when an undefined command has been sent to FDC. The FDC will set the bit 6 and the bit 7 in the Main Status Register to 1 and terminate the command without issuing an interrupt.

9.6.13 DMA Transfers

DMA transfers are enabled by the SPECIFY command and are initiated by the FDC by activating the LDRQ# cycle during a DATA TRANSFER command. The FIFO is enabled directly by asserting the LPC DMA cycles.

9.6.14 Low Power Mode

When writing a 1 to the bit 6 of the DSR, the controller is set to low power mode immediately. All the clock sources including Data Separator, Microcontroller, and Write precompensation unit will be gated. The FDC can be resumed from the low-power state in two ways. One is a software reset via the DOR or DSR; and the other is a read or write to either the Data Register or Main Status Register. The second method is more preferred since all internal register values are retained.

9.7 Serial Port (UART) Register Description

The IT8705F incorporates two enhanced serial ports that perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Each of the serial channels individually contains a programmable baud rate generator, which is capable of dividing the input clock by a number ranging from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

Table 9-25. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

9.7.1 Data Registers

The TBR and RBR individually holds from five to eight data bits. If the transmitted data is less than eight bits, it aligns to the LSB. Either received or transmitted data is buffered by a shift register, and is latched first by a holding register. The bit 0 of any word is first received and transmitted.

(1) Receiver Buffer Register (RBR) (Read only, Address offset=0, DLAB=0)

This register receives and holds the incoming data. It contains a non-accessible shift register which converts the incoming serial data stream into a parallel 8-bit word.

(2) Transmitter Buffer Register (TBR) (Write only, Address offset=0, DLAB=0)

This register holds and transmits the data via a non-accessible shift register, and converts the outgoing parallel data into a serial stream before transmission.

9.7.2 Control Registers: IER, IIR, FCR, DLL, DLM, LCR and MCR

(1) Interrupt Enable Register (IER) (Read/write, Address offset=1, DLAB=0)

The IER is used to enable (or disable) four active high interrupts which activate the interrupt outputs with its lower four bits: IER(0), IER(1), IER(2), and IER(3).

Table 9-26. Interrupt Enable Register Description

Bit	Default	Description
7-4	-	**Reserved**
3	0	**Enable MODEM Status Interrupt** Set this bit high to enable the Modem Status Interrupt when one of the Modem Status Registers changes its bit status.
2	0	**Enable Receiver Line Status Interrupt** Set this bit high to enable the Receiver Line Status Interrupt, which is caused when, Overrun, Parity, Framing or Break occurs.
1	0	**Enable Transmitter Holding Register Empty Interrupt** Set this bit high to enable the Receiver Line Status Interrupt which is caused when Overrun, Parity, Framing or Break errors occur.
0	0	**Enable Received Data Available Interrupt** Set this bit high to enable the Received Data Available Interrupt.

(2) Interrupt Identification Register (IIR) (Read only, Address offset=2)

This register facilitates the host CPU to determine interrupt priority and its source. The priority of four existing interrupt levels is listed below:

1. Received Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the type of interrupt is stored in the IIR which is accessed by the host, the serial channel holds back all interrupts and indicates the pending interrupts with the highest priority to the host. Any new interrupts will not be acknowledged until the host access is completed. The contents of the IIR are described in the table on the next page:

Table 9-27. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	X	X	1	-	None	None	-
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	Read LSR
0	1	0	0	Second	Received Data Available	Received Data Available	Read RBR or FIFO drops below the trigger level
1	1	0	0	Second	Character Time-out Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time	Read RBR
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Read IIR if THRE is the Interrupt Source Write THR
0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, DCD#	Read MSR

Note: X = Not defined.

IIR(0): Used to indicate a pending interrupt in either a hard-wired prioritized or polled environment with a logic 0 state. In such a case, IIR contents may be used as a pointer to the appropriate interrupt service routine.
IIR(1), IIR(2): Used to identify the highest priority interrupt pending.
IIR(3): In non-FIFO mode, this bit is a logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out interrupt is pending.
IIR(4), IIR(5): Always logic 0.
IIR(6), IIR(7): Are set when FCR(0) = 1.

(3) FIFO Control Register (FCR) (Write Only, Address offset=2)

This register is used to enable/clear the FIFO, and set the RCVR FIFO trigger level.

Table 9-28. FIFO Control Register Description

Bit	Default	Description
7-6	-	**Receiver Trigger Level Select** These bits set the trigger levels for the RCVR FIFO interrupt.
5-4	0	**Reserved**
3	0	This bit doesn't affect the Serial Channel operation. RXRDY and TXRDY functions are not available on this chip.
2	0	**Transmitter FIFO Reset** This self-clearing bit clears all contents of the XMIT FIFO and resets its related counter to 0 via a logic "1."
1	0	**Receiver FIFO Reset** Setting this self-clearing bit to logic 1 clears all contents of the RCVR FIFO and resets its related counter to 0 (except the shift register).
0	0	**FIFO Enable** XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT and RCVR FIFOs are disabled and cleared respectively when this bit is cleared to low. This bit must be logic 1 if the other bits of the FCR are written, or they will not be properly programmed. When this register is switched to non-FIFO mode, all its contents are cleared.

Table 9-29. Receiver FIFO Trigger Level Encoding

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

(4) Divisor Latches (DLL, DLM) (Read/write, Address offset=0,1 DLAB=1)

Two 8-bit Divisor Latches (DLL and DLM) store the divisor values in a 16-bit binary format. They are loaded during the initialization to generate a desired baud rate.

(5) Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG which can take any clock input (from DC to 8 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking with an external clock oscillator. The DLL or DLM is a number of 16-bit format, providing the divisor range from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

Table 9-30. Baud Rates Using (24 MHz ÷ 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

(6) Scratch Pad Register (Read/write, Address offset=7)

This 8-bit register does not control the UART operation in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general purpose data.

(7) Line Control Register (LCR) (Read/write, Address offset=3)

LCR controls the format of the data character and supplies the information of the serial line. Its contents are described on the next page:

Table 9-31. Line Control Register Description

Bit	Default	Description
7	0	**Divisor Latch Access Bit (DLAB)** Must be set to high to access the Divisor Latches of the baud rate generator during READ or WRITE operations. It must be set low to access the Data Registers (RBR and TBR) or the Interrupt Enable Register.
6	0	**Set Break** Force the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and this state will be preserved until a low level resetting LCR(6), enabling the serial port to alert the terminal in a communication system.
5	0	**Stick Parity** When this bit and LCR(3) are high at the same time, the parity bit is transmitted, and then detected by receiver, in opposite state by LCR(4) to force the parity bit into a known state and to check the parity bit in a known state.
4	0	**Even Parity Select** When parity is enabled (LCR(3) = 1), LCR(4) = 0 selects odd parity, and LCR(4) = 1 selects even parity.
3	0	**Parity Enable** A parity bit, located between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.
2	0	**Number of Stop Bits** This bit specifies the number of stop bits in each serial character, as summarized in Table 9-32.
1-0	00	**Word Length Select [1:0]** 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

Table 9-32. Stop Bits Number Encoding

LCR (2)	Word Length	No. of Stop Bits
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

(8) MODEM Control Register (MCR) (Read/write, Address offset=4)

Control the interface by the modem or data set (or device emulating a modem).

Table 9-33. Modem Control Register Description

Bit	Default	Description
7-5	-	**Reserved**
4	0	**Internal Loop Back** Provide a loopback feature for diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. The four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs and forced to inactive high. The transmitted data are then immediately received, allowing the processor to verify the transmit and receive data path of the serial channel.
3	0	**Out2** This bit enables the serial port interrupt output by logic 1.
2	0	**Out1** This bit does not have an output pin and can only be read or written by the CPU.
1	0	**Request to Send (RTS)** Control the Request to Send (RTS#) which is in an inverse logic state with that of MCR(1).
0	0	**Data Terminal Ready (DTR)** Control the Data Terminal ready (DTR#) which is in an inverse logic state with the MCR(0).

9.7.3 Status Registers: LSR and MSR

(1) Line Status Register (LSR) (Read/write, Address offset=5)

This register provides status indications and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the LSR are described below:

Table 9-34. Line Status Register Description

Bit	Default	Description
7	0	**Error in Receiver FIFO** In 16450 mode, this bit is always 0. In the FIFO mode, it sets high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.
6	1	**Transmitter Empty** This read only bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty. Otherwise, this bit is "0," and has the same function in the FIFO mode.
5	1	**Transmitter Holding Register Empty** Transmitter Holding Register Empty (THRE). This read only bit indicates that the TBR is empty and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by a read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and cleared when at least one byte is written to the XMIT FIFO.

Table 9-38. Line Status Register Description[cont'd]

Bit	Default	Description
4	0	**Line Break** Break Interrupt (BI) status bit indicates that the last character received was a break character, (invalid but entire character), including parity and stop bits. This occurs when the received data input is held in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be generated in the IIR with the IER(2) enabled previously.
3	0	**Framing Error** Framing Error (FE) bit, a logic 1, indicates that the stop bit in the received character was not valid. It resets low when the CPU reads the contents of the LSR.
2	0	**Parity Error** The parity error (PE) indicates by a logic 1 that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset to "0" whenever the LSR is read by the CPU.
1	0	**Overrun Error** Overrun Error (OE) bit indicates by a logic 1 that the RBR has been overwritten by the next character before it had been read by the CPU. In the FIFO mode, the OE occurs when the FIFO is full and the next character has been completely received by the Shift Register. It will be reset when the LSR is read by the CPU.
0	0	**Data Ready** A logic "1" indicates a character has been received by the RBR. And a logic "0" indicates all the data in the RBR or the RCVR FIFO have been read.

(2) MODEM Status Register (MSR) (Read/write, Address offset=6)

This 8-bit register indicates the current state of the control lines with modems or peripheral devices in addition to this current state information. Four of these eight bits MSR(4) - MSR(7) can provide the state change information when a modem control input changes state. It is reset low when the host reads the MSR.

Table 9-35. Modem Status Register Description

Bit	Default	Description
7	0	**Data Carrier Detect** Receive Line Signal Detect - Indicates the complement status of Receive Line Signal Detect (DCD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of the MCR.
6	0	**Ring Indicator** Ring Indicator (RI#) - Indicates the complement status to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 in the MCR.
5	0	**Data Set Ready** Data Set Ready (DSR#) - Indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR# in the MCR.
4	0	**Clear to Send** Clear to Send (CTS#) – Indicates the complement of CTS# input. When the serial channel is in the loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# in the MCR.
3	0	**Delta Data Carrier Detect** Indicate that the DCD# input state has been changed since the last time read by the host.
2	0	**Trailing Edge Ring Indicator** Indicate that the RI input state to the serial channel has been changed from a low to high since the last time read by the host. The change to logic 1 does not activate the TERI.
1	0	**Delta Data Set Ready** Delta Data Set Ready (DDSR) - A logic "1" indicates that the DSR# input state to the serial channel has been changed since the last time read by the host.
0	0	**Delta Clear to Send** This bit indicates the CTS# input to the chip has changed state since the last time the MSR was read.

9.7.4 Reset

Reset of the IT8705F should be held to an idle mode reset high for 500 ns until initialization, and this causes the following:

Initialization of the transmitter and receiver internal clock counters.

Table 9-36. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5 and 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 low, bits 4-7 input signals
SOUT0, SOUT1	Reset	High
RTS0#, RTS1#, DTR0#, DTR1#	Reset	High
IRQ of Serial Port	Reset	High Impedance

9.7.5 Programming

Each serial channel of the IT8705F is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Even though the control register can be written in any given order, the IER should be the last register written because it controls the interrupt enables. After the port is programmed, these registers can still be updated whenever the port is not transferring data.

9.7.6 Software Reset

This approach allows the serial port returning to a completely known state without a system reset. This is achieved by writing the required data to the LCR, DLL, DLM and MCR. The LSR and RBR must be read before enabling interrupts to clear out any residual data or status bits that may be invalid for subsequent operations.

9.7.7 Clock Input Operation

The input frequency of the Serial Channel is 24 MHz ÷ 13, not exactly 1.8432 MHz.

9.7.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When setting FCR(0)=1 and IER(0)=1, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

a. The receive data available interrupt, the IIR, and receive data available indication will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level

b. The receiver line status interrupt has higher priority over the received data available interrupt

c.The time-out timer will be reset after receiving a new character or after the host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the host reads one character from the RCVR FIFO

RCVR FIFO time-out Interrupt: By enabling the RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

a. The RCVR FIFO time-out interrupt will occur only if there is at least one character in the FIFO whenever the interval between the most recent received serial character and the most recent host read from the FIFO is longer than four consecutive character times

b. The RLCK clock signal input is used to calculate character times

c. The time-out timer will be reset after receiving a new character or after the host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the host reads one character from the RCVR FIFO

(2) XMIT Interrupt

By setting FCR(0) and IER(1) to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt occurs under the conditions described below:

a. The transmitter interrupt occurs when the XMIT FIFO is empty, and it will be reset if the Transmitter Holding Register (THR) is written or the IIR is read

b. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following condition occurs: THRE = 1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate, if it is enabled. Once the first transmitter interrupt is enabled, the THRE indication is delayed one character time minus the last stop bit time

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR (0)=1, and IER(0), IER(1), IER(2), IER(3) or all are “0”]

Either or both XMIT and RCVR can be in this operation mode. The operation mode can be programmed by users and is responsible for checking the RCVR and XMIT status via the LSR described below:

LSR(7): RCVR FIFO error indication.

LSR(6): XMIT FIFO and Shift register empty.

LSR(5): XMIT FIFO empty indication.

LSR(4) - LSR(1): Specify that errors have occurred. Character error status is handled in the same way as in the interrupt mode. The IIR is not affected since IER(2)=0.

LSR(0): This bit is high whenever the RCVR FIFO contains at least one byte.

No trigger level is reached or time-out condition indicated in the FIFO Polled mode.

9.8 Parallel Port

The IT8705F incorporates one multi-mode high performance parallel port, which supports the IBM AT, PS/2 compatible bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). Please refer to the IT8705F Configuration registers and Configuration Description for information on enabling/disabling, changing the base address of the parallel port, and operation mode selection.

Table 9-37. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	76	STB#	WRITE#	NStrobe
2-9	71-68, 66-63	PD0 - 7	PD0 - 7	PD0 – 7
10	62	ACK#	INTR	nAck
11	61	BUSY	WAIT#	Busy PeriphAck(2)
12	60	PE	(NU) (1)	PError nAckReverse(2)
13	59	SLCT	(NU) (1)	Select
14	77	AFD#	DSTB#	nAutoFd HostAck(2)
15	75	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	73	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	74	SLIN#	ASTB#	nSelectIn

Notes: 1. NU: Not used.
2. Fast mode.
3. For more information, please refer to the IEEE 1284 standard.

9.8.1 SPP and EPP Modes

Table 9-38. Address Map and Bit Map for SPP and EPP Modes

Register	Address	R/W	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1H	RO	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2H	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base 1+4H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base 1+5H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base 1+6H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base 1+7H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note: 1.The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

(1)Data Port (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by the bit 5 of the logic state of the control port register. It forwards directions when the bit is low and reverses directions when the bit is high.

(2)Status Port (Base Address 1 + 01h)

This is a **read only** register. Writing to this register has no effects. The contents of this register are latched during an IOR cycle.
Bit 7 - BUSY#: Inverse of printer BUSY signal. A logic "0" means that the printer is busy and cannot accept another character. A logic "1" means that it is ready to accept the next character.
Bit 6 - ACK#: Printer acknowledge, a logic "0" means that the printer has received a character and is ready to accept another. A logic "1" means that it is still processing the last character.
Bit 5 - PE: Paper end, a logic "1" indicates the paper end.
Bit 4 - SLCT: Printer selected, a logic "1" means that the printer is on line.
Bit 3 - ERR#: Printer error signal, a logic "0" means an error has been detected.
Bits 1, 2: Reserved, these bits are always "1" when read.
Bit 0 - TMOUT: This bit is valid only in EPP mode and indicates that a 10-msec time-out has occurred in EPP operation. A logic "0" means no time-out occurred and a logic “1” means that a time-out error has been detected. This bit is cleared by a LRESET# or by writing a logic “1” to it. When the IT8705F is selected to non-EPP mode (SPP or ECP), this bit is always logic "1" when read.

(3)Control Port (Base Address 1 + 02h)

This port provides all output signals to control the printer. The register can be read and written.
Bits 6, 7: Reserved, these two bits are always "1" when read.
Bit 5 - PDDIR: Data port direction control. This bit determines the direction of the data port. Set this bit "0" to output the data port to PD bus and "1" to input from PD bus.
Bit - 4 IRQE: Interrupt request enable. Setting this bit "1" enables the interrupt requests from the parallel port to the host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.
Bit - 3 SLIN: Inverse of SLIN# pin, setting this bit to "1" selects the printer.
Bit - 2 INIT: Initiate printer, setting this bit to "0" initializes the printer.
Bit - 1 AFD: Inverse of the AFD# pin, setting this bit to "1" causes the printer to automatically advance one line after each line is printed.
Bit 0 - STB: Inverse of the STB# pin. This pin controls the data strobe signal to the printer.

(4)EPP Address Port (Base Address 1 + 03h)

The EPP Address Port is only available in the EPP mode. When the host writes to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O write cycle is on this address) causes an EPP ADDRESS WRITE cycle. When the host reads from this port, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O read cycle is on this address) causes an EPP ADDRESS read cycle.

(5)EPP Data Ports 0-3 (Base Address 1 + 04h - 07h)

The EPP Data Ports are only available in the EPP mode. When the host writes to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is on this address) causes an EPP DATA WRITE cycle. When the host reads from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O read cycle is on this address) causes an EPP DATA read cycle.

9.8.2 EPP Mode Operation

When the parallel port of the IT8705F is set in the EPP mode, the SPP mode is also available. If no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by the SPP control port. The direction of the data port is controlled by the bit 5 of the control port register. There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY (Internal signal: When active, the IT8705F will issue Long Wait in SYNC field) high (EPP read/write cycle) to WAIT# being de-asserted. If a time-out occurs, the current EPP read/write cycle is aborted and a logic "1" will be read in the bit 0 of the status port register. The host must write 0 to bits 0, 1, 3 of the control port register before any EPP read/write cycle (EPP spec.) The pins STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP read/write cycle.

(1) EPP ADDRESS WRITE

1. The host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.
2. The chip asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus, allowing the host to complete the I/O write cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(2) EPP ADDRESS READ

1. The host reads a byte from the EPP Address Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts ASTB# after IOR becomes active.
3. The peripheral drives the PD bus valid and de-asserts WAIT, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7, allowing the host to complete the I/O read cycle.
4. The peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

(3) EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04H - 07H). The chip drives D0- D7 onto PD0 -PD7.
2. The chip asserts WRITE# (STB#) and DSTB# (AFD#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to the PD bus, allowing the host to complete the I/O write cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts writes to terminate the cycle.

(4) EPP DATA READ

1. The host reads a byte from the EPP DATA Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts DSTB# after IOR becomes active.
3. The peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7, allowing the host to complete the I/O read cycle.
4. The peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.8.3 ECP Mode Operation

This mode is both software and hardware compatible with the existing parallel ports, allowing ECP to be used as a standard LPT port when the ECP mode is not required. It provides an automatic high-burst-bandwidth channel that supports DMA or the ECP mode in both forward and reverse directions. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and increase the maximum bandwidth allowed. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports run-length encoded (RLE) decompression in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8705F does not support hardware RLE compression. For a detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 9-39. Bit Map of the ECP Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	NFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

(1) ECP Register Definitions

Table 9-40. ECP Register Definitions

Name	Address	R/W	ECP Mode	Function
data	Base 1 +000H	R/W	000-001	Data Register
ecpAFifo	Base 1 +000H	R/W	011	ECP FIFO (Address)
dsr	Base 1 +001H	R/W	All	Status Register
dcr	Base 1 +002H	R/W	All	Control Register
cFifo	Base 2 +000H	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000H	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000H	R/W	110	Test FIFO
cnfgA	Base 2 +000H	RO	111	Configuration Register A
cnfgB	Base 2 +001H	R/W	111	Configuration Register B
ecr	Base 2 +002H	R/W	All	Extended Control Register

Notes: 1. The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

2. The Base address 2 depends on the Logical Device configuration registers of Parallel Port (0X62, 0X63).

(2) ECP Mode Descriptions

Table 9-41. ECP Mode Descriptions

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: Please refer to the ECP Register Description on pages 125-126 for a detailed description of the mode selection.

(3) ECP Pin Descriptions

Table 9-42. ECP Pin Descriptions

Pin	Symbol	Type	Description
76	**nStrobe (HostClk)**	O	Used for handshaking with Busy to write data and addresses into the peripheral device.
71-68, 66-63	**PD0-PD7**	I/O	Address or data or RLE data.
62	**nAck (PeriphClk)**	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the host.
61	**Busy (PeriphACK)**	I	The peripheral uses this signal for flow control in the forward direction (hand-shaking with nStrobe). In the reverse direction, this signal is used to determine whether a command or data information is present on PD0-PD7.
60	**PError (nAckReverse)**	I	Used to acknowledge nInit from the peripheral which drives this signal low, allowing the host to drive the PD bus.
59	**Select**	I	Printer On-Line indication.
77	**nAutoFd (HostAck)**	O	In the reverse direction, it is used for handshaking between the nAcK and the host. When it is asserted, a peripheral data byte is requested. In the forward direction, this signal is used to determine whether a command or data information is present on PD0 - PD7.
75	**nFault (nPeriphRequest)**	I	In the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while in ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to the host, which has the ultimate control over the transfer direction.
73	**nInit (nReverseRequest)**	O	The host may drive this signal low to place the PD bus in the reverse direction. In the ECP mode, the peripheral is permitted to drive the PD bus when nInit is low, and nSelectIn is high.
74	**NSelectIn (1284 Active)**	O	Always inactive (high) in the ECP mode.

(4) Data Port (Base 1+00h, Modes 000 and 001)

Its contents will be cleared by a RESET. In a write operation, the contents of the LPC data fields are latched by the Data Register. The contents are then sent without being inverted to PD0~ PD7. In a read operation, the contents of data ports are read and sent to the host.

(5) ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)

Any data byte written to this port are placed in the FIFO and tagged as an ECP Address/RLE. The hardware then automatically sends this data to the peripheral. Operation of this port is valid only in the forward direction (dcr(5)=0).

(6) Device Status Register (dsr) (Base 1 +01h, Mode All)

Bits 0, 1 and 2 of this register are not implemented. These bit states are remained at high in a read operation of the Printer Status Register.
dsr(7): This bit is the inverted level of the Busy input.
dsr(6): This bit is the state of the nAck input.
dsr(5): This bit is the state of the PError input.
dsr(4): This bit is the state of the Select input.
dsr(3): This bit is the state of the nFault input.
dsr(2)-dsr(0): These bits are always 1.

(7) Device Control Register (dcr) (Base 1+02h, Mode All)

Bits 6 and 7 of this register have no function. They are set high during the read operation, and cannot be written. Contents in bits 0-5 are initialized to “0” when the RESET pin is active.
dcr(7)-dcr(6): These two bits are always high.
dcr(5): Except in the modes 000 and 010, setting this bit low means that the PD bus is in output operation; setting it high, in input operation. This bit will be forced to low in mode 000.
dcr(4): Setting this bit high enables the interrupt request from the peripheral to the host due to a rising edge of the nAck input.
dcr(3): It is inverted and output to SelectIn.
dcr(2): It is output to nInit without inversion.
dcr(1): It is inverted and output to nAutoFd.
dcr(0): It is inverted and output to nStrobe.

(8) Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written or DMA transferred from the host to this FIFO are sent by a hardware handshaking to the peripheral according to the standard parallel port protocol. This operation is only defined for the forward direction.

(9) ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the host to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The host can receive these bytes by performing read operations or DMA transfers from this FIFO.

(10) Test FIFO (tFifo) (Base 2+00h, Mode 110)

The host may operate read/write or DMA transfers to this FIFO in any direction. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Making a read operation from an empty tFifo causes the last data byte to return.

(11) Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This **read only** register indicates to the system that interrupts are ISA-Pulses compatible. This is an 8-bit implementation by returning a 10h.

(12) Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is **read only**.
cnfgB(7): A logic "0" read indicates that the chip does not support hardware RLE compression.
cnfgB(6): Reserved
cnfgB(5)-cnfg(3): A value 000 read indicates that the interrupt must be selected with jumpers.
cnfgB(2)-cnfg(0): A value 000 read indicates that the DMA channel is jumpered 8-bit DMA.

(13) Extended Control Register (ecr) (Base 2+02h, Mode All)

ECP function control register.
ecr(7)-ecr(5): These bits are used for read/write and mode selection.

Table 9-43. Extended Control Register (ECR) Mode and Description

ECR	Mode and Description
000	**Standard Parallel Port Mode** The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	**PS/2 Parallel Port Mode** It is similar to the SPP mode, except that the dcr(5) is **read/write**. When dcr(5) is 1, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	**Parallel Port Data FIFO Mode** This mode is similar to the 000 mode, except that the host writes or DMA transfers the data bytes to the FIFO. The FIFO data is then transmitted to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	**ECP Parallel Port Mode** In the forward direction, bytes placed into the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral under the ECP protocol. In the reverse direction, bytes are transmitted to the ecpDFifo from the ECP port.
100, 101	**Reserved** Not defined.
110	**Test mode** In this mode, the FIFO data may be read or written, but it cannot be sent to the peripheral.
111	**Configuration mode** In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ecr(4): nErrIntrEn, read/write, Valid in ECP(011) Mode
1: Disable the interrupt generated on the asserting edge of the nFault input.
0: Enable the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted, or if this bit is written from 1 to 0 in the low-level nFault.

ecr(3): dmaEn, read/write
1: Enable DMA. DMA starts when serviceIntr (ecr(2)) is 0.
0: Disable DMA unconditionally.

ecr(2): ServiceIntr, read/write
1: Disable DMA and all service interrupts.
0: Enable the service interrupts. This bit will be set to "1" by hardware when one of the three service interrupts has occurred.
Writing "1" to this bit will not generate an interrupt.
Case 1: dmaEn=1
During DMA, this bit is set to 1 (a service interrupt generated) if the terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0
This bit is set to 1 (a service interrupt generated) whenever there are writeIntrThreshold or more bytes space free in the FIFO.

Case 3: dmaEn=0, dcr(5)=1

This bit is set to 1 (a service interrupt generated) whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

ecr(1): full, **read only**.
1: The FIFO is full and cannot accept another byte.
0: The FIFO has at least 1 free data byte space.
ecr(0): empty, **read only**.
1: The FIFO is empty.
0: The FIFO contains at least 1 data byte.

(14) Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks that happen before data is transferred are software-controlled. Setting mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between the FIFO and the ECP port.

From the mode 000 or 001, it may be immediately switched to any other mode. To change directions, the mode must first be set to 001.

In the extended forward mode, the FIFO must be cleared and all the signals must be de-asserted before returning to mode 000 or 001. In ECP reverse mode, all data must be read from the FIFO before returning to mode 000 or 001. Usually, unneeded data is accumulated during ECP reverse handshaking, when the mode is changed during a data transfer. In such conditions, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs that may occur while handshaking signals are being processed, these guidelines must be followed.

(15) Software Operation (ECP)

Before the ECP operation can begin, it is first necessary for the host to switch the mode to 000 in order to negotiate with the parallel port. During this process, the host determines whether the peripheral supports the ECP protocol.

After this negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, the direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfers are PWord wide and PWord aligned. Permitted only in the forward direction, Address/RLE transfers are byte-wide. The ECP Address/RLE bytes may be automatically transmitted by writing to the ecpAFifo. Similarly, data PWords may be automatically sent via the ecpDFifo.

To change directions, the host switches mode to 001. It then negotiates either the forward or reverse channel, sets direction to 1 or 0, and finally switches mode to 001. If the direction is set to 1, the hardware performs handshaking for each ECP data byte read, then tries to fill the FIFO. At this time, PWords may be read from the ecpDFifo while it retains data. It is also possible to perform the ECP transfers by handshaking with individual bytes under programmed control in mode = 001, or 000, even though this is a comparatively time-consuming approach.

(16) Hardware Operation (DMA)

The Standard PC DMA protocol (through LDRQ#) is followed. As in the programmed I/O case, software sets the direction and state. Next, the desired count and memory addresses are programmed into DMA controller. The dmaEn is set to 1, and the serviceIntr is set to 0. To complete the process, the DMA channel with the DMA controller is unmasked. The contents in the FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from the FIFO located at 0 x 400. By generating an interrupt and asserting a serviceIntr. DMA is disabled when the DMA controller reaches the terminal count. By not asserting LDRQ# for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while performing a data transfer, the host DMA controller is disabled, serviceIntr is then set to 1, and dmaEn is next set to 0. If the contents in FIFO are empty or full, the DMA will start again. This is first done by enabling the host DMA controller, and then setting dmaEn to 1. Finally, serviceIntr is set to 0. Upon the completion of a DMA transfer in the forward direction, the software program must wait until the contents in FIFO are empty and the busy line is low to make sure that all data can reach the peripheral device successfully.

(17) Interrupts

It is necessary to generate an interrupt when any of the following states are reached:

1. serviceIntr = 0, dmaEn = 0, direction = 0, and the number of PWords in the FIFO is greater than or equal to writeIntrThreshold
2. serviceIntr = 0, dmaEn = 0, direction = 1, and the number of PWords in the FIFO is greater than or equal to readIntrThreshold
3. serviceIntr = 0, dmaEn = 1, and DMA reaches the terminal count
4. nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted
5. ackIntEn = 1. In current implementations of using existing parallel ports, the interrupt generated may be either edge or level trigger type

(18) Interrupt Driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is “0” and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is “0” and the number of available PWords in the FIFO is equal to readIntrThreshold. If it is full, the FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to readIntrThreshold may be read from the FIFO in a single burst. In the Test mode, software can determine the values of writeIntrThreshold, readIntrThreshold, and FIFO depth while accessing the FIFO.

Any PC LPC bus implementation that is adjusted to expedite DMA or I/O transfer must ensure that the bandwidth on the ISA is maintained on the interface. Although the LPC (even PCI) bus of PC cannot be directly controlled, the interface bandwidth of ECP port can be constrained to perform at the optimum speed.

(19) Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or close to the permitted peak bandwidth of 500 KB/sec. The state machine does not examine nAck, but just begins the next DMA based on the Busy signal.

9.9 Consumer Remote Control (TV Remote) IR (CIR)

9.9.1 Overview

The CIR is used in Consumer Remote Control equipment, and is a programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequencies, baud rate divisor values and sensitivity ranges, the CIR registers are able to support the popular protocols such as RC-5, NEC, and RECS-80. Software driver programming can support new protocols.

9.9.2 Features

- Supports 30 kHz - 57kHz (low frequency) or 400 kHz – 500 kHz (high frequency) carrier transmission
- Baud rates up to 115200 BPS (high frequency)
- Demodulation optional
- Supports transmission run-length encoding and deferral functions
- 32-byte FIFO for data transmission or data reception

9.9.3 Block Diagram

The CIR consists of the Transmitter and Receiver parts. The Transmitter part is responsible for transmitting data to the FIFO, processing the FIFO data by serialization, modulation and sending out the data through the LED device. The Receiver part is responsible for receiving data, processing data by demodulation, deserialization and storing data in the Receiver FIFO.

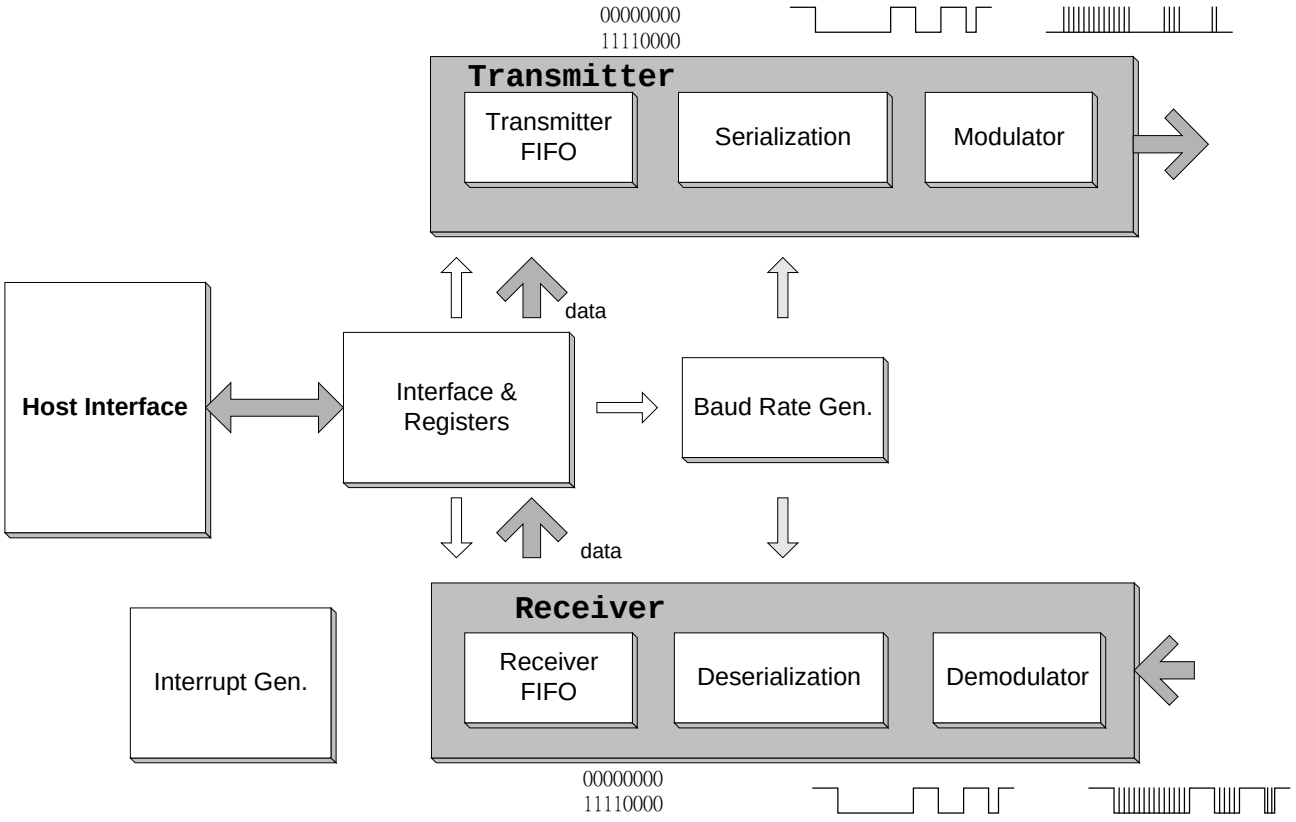


Figure 9-7. CIR Block Diagram

9.9.4 Transmit Operation

The data written to the Transmitter FIFO will be exactly serialized from LSB to MSB, modulated with carrier frequency and sent to the CIRTX output. The data is either in bit-string format or run-length decode.

Before the data transmission can begin, code byte write operations must be performed to the Transmitter FIFO DR. The bit TXRLE in the TCR1 should be set to "1" before the run-length decodes data can be written into the Transmitter FIFO. Setting TXENDF in the TCR1 will enable the data transmission deferral, and avoid the transmitter FIFO underrun. The bit width of the serialized bit string is determined by the value programmed in the baud rate divisor registers BDLR and BDHR. When the bits HCFS and CFQ[4:0] are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bits TXMPM[1:0] and TXMPW[2:0] specify the pulse numbers in a bit width and the required duty cycles of the carrier pulse according to the communication protocol. Only a logic "0" can activate the Transmitter LED in the format of a series of modulating pulses.

9.9.5 Receive Operation

The Receiver function is enabled if the bit RXEN in the RCR is set to "1". Either demodulated or modulated RX# signal is loaded into the Receiver FIFO, and the bit RXEND in the RCR determines the demodulation logic should be used or not. Determine the baud rate by programming the baud rate divisor registers BDLR and BDHR, and the carrier frequencies by programming the bits HCFS and CFQ[4:0]. Set RDWOS to "0" to syn. The bit RXACT in the RCR is set to "1" when the serial data or the selected carrier is incoming, and the sampled data will then be kept in the Receiver FIFO. Write "1" to the bit RXACT to stop the Receiver operation; "0" to the bit RXEN to disable the Receiver.

9.9.6 Register Descriptions and Address

Table 9-44. List of CIR Registers

Address	R/W	Default	Register Name
Base + 0h	R/W	FFh	CIR Data Register (DR)
Base + 1h	R/W	00h	CIR Interrupt Enable Register (IER)
Base + 2h	R/W	01h	CIR Receiver Control Register (RCR)
Base + 3h	R/W	00h	CIR Transmitter Control Register 1 (TCR1)
Base + 4h	R/W	5Ch	CIR Transmitter Control Register 2 (TCR2)
Base + 5h	RO	00h	CIR Transmitter Status Register (TSR)
Base + 6h	RO	00h	CIR Receiver Status Register (RSR)
Base + 5h	R/W	00h	CIR Baud Rate Divisor Low Byte Register (BDLR)
Base + 6h	R/W	00h	CIR Baud Rate Divisor High Byte Register (BDHR)
Base + 7h	R/W	01h	CIR Interrupt Identification Register (IIR)

9.9.6.1 CIR Data Register (DR)

The DR, an 8-bit **read/write** register, is the data port for CIR. Data are transmitted and received through this register.

Address: Base address + 0h

Bit	R/W	Default	Description
7 – 0	R/W	FFh	**CIR Data Register (DR[7:0])** Writing data to this register causes data to be written to the Transmitter FIFO. Reading data from this register causes data to be received from the Receiver FIFO.

9.9.6.2 CIR Interrupt Enable Register (IER)

The IER, an 8-bit r**ead/write** register, is used to enable the CIR interrupt request.

Address: Base address + 1h

Bit	R/W	Default	Description
7 – 6	-	-	**Reserved for ITE Use**
5	R/W	0	**RESET (RESET)** This bit is a software reset function. Writing a “1” to this bit resets the registers of DR, IER, TCR1, BDLR, BDHR and IIR. This bit is then cleared to initial value automatically.
4	R/W	0	**Baud Rate Register Enable Function Enable (BR)** This bit is used to control the baud rate registers enable read/write function. Set this bit to “1” to enable the baud rate registers for CIR. Set this bit to “0” to disable the baud rate registers for CIR.
3	R/W	0	**Interrupt Enable Function Control (IEC)** This bit is used to control the interrupt enable function. Set this bit to “1” to enable the interrupt request for CIR. Set this bit to “0” to disable the interrupt request for CIR.
2	R/W	0	**Receiver FIFO Overrun Interrupt Enable (RFOIE)** This bit is used to control Receiver FIFO Overrun Interrupt request. Set this bit to “1” to enable Receiver FIFO Overrun Interrupt request. Set this bit to “0” to disable Receiver FIFO Overrun Interrupt request.
1	R/W	0	**Receiver Data Available Interrupt Enable (RDAIE)** This bit is used to enable Receiver Data Available Interrupt request. The Receiver will generate this interrupt when the data available in the FIFO exceeds the FIFO threshold level. Set this bit to “1” to enable Receiver Data Available Interrupt request. Set this bit to “0” to disable Receiver Data Available Interrupt request.
0	R/W	0	**Transmitter Low Data Level Interrupt Enable (TLDLIE)** This bit is used to enable Transmitter Low Data Level Interrupt request. The Transmitter will generate this interrupt when the data available in the FIFO is less than the FIFO threshold level. Set this bit to “1” to enable Transmitter Low Data Level Interrupt request. Set this bit to “0” to disable Transmitter Low Data Level Interrupt request.

9.9.6.3 CIR Receiver Control Register (RCR)

The RCR, an 8-bit **read/write** register, is used to control the CIR Receiver.

Address: Base address + 2h

Bit	R/W	Default	Description
7	R/W	0	**Receiver Data Without Sync. (RDWOS)** This bit is used to control the sync. logic for Receiving data. Set this bit to “1” to obtain the receiving data without sync. logic. Set this bit to “0” to obtain the receiving data in sync. logic.
6	R/W	0	**High-Speed Carrier Frequency Select (HCFS)** This bit is used to select Carrier Frequency between high-speed and low-speed. **030-58 kHz (Default)** 1400-500 kHz
5	R/W	0	**Receiver Enable (RXEN)** This bit is used to enable Receiver function. Set this bit to 1’ to enable the Receiver function. Set this bit to”0” to disable the Receiver function. When the Receiver is enabled, RXACT will be active if the selected carrier frequency is received.
4	R/W	0	**Receiver Demodulation Enable (RXEND)** This bit is used to control the Receiver Demodulation logic. Set this bit to “1” to enable Receiver Demodulation logic. Set this bit to “0” to disable Receiver Demodulation logic. If the Receiver device can not demodulate the correct carrier, set this bit to “1”.
3	R/W	0	**Receiver Active (RXACT)** This bit is used to control the Receiver operation. This bit is set to “0” when the Receiver is inactive. This bit will be set to “1” when the Receiver detects a pulse (RXEND=0) or pulse-train (RXEND=1) with correct carrier frequency. The Receiver then starts to sample the input data when Receiver Active is set. Write a “1” to this bit to clear the Receiver Active condition and make the Receiver enter the inactive mode.
2-0	R/W	001	**Receiver Demodulation Carrier Range (RXDCR[2:0])** These three bits are used to set the tolerance of the Receiver Demodulation carrier frequency. See Table 9-46 and Table 9-47.

9.9.6.4 CIR Transmitter Control Register 1 (TCR1)

The TCR1, an 8-bit **read/write** register, is used to control the Transmitter.

Address: Base address + 3h

Bit	R/W	Default	Description
7	R/W	0	**FIFO Clear (FIFOCLR)** Writing a "1" to this bit clears the FIFO. This bit is then cleared to "0" automatically.
6	R/W	0	**Internal Loopback Enable (ILE)** This bit is used to execute internal loopback for test and must be "0" in normal operation. Set this bit to "0" to disable the Internal Loopback mode. Set this bit to "1" to enable the Internal Loopback mode.
5 - 4	R/W	0	**FIFO Threshold Level (FIFOTL)** These two bits are used to set the FIFO threshold level. The FIFO length is 32 bytes for TX or RX function (ILE = 0) in normal operation and 16 bytes for both TX and RX in internal loopback mode (ILE = 1). **16-Byte Mode / 32-Byte Mode** **00 / 1 / 1(Default)** 01 / 3 / 7 10 / 7 / 17 11 / 13 / 25
3	R/W	0	**Transmitter Run Length Enable (TXRLE)** This bit controls the Transmitter Run-Length encoding/decoding mode, which condenses a series of "1" or "0" into one byte with the bit value stored in bit 7 and number of bits minus 1 in bits 6 – 0. Set this bit to "1" to enable the Transmitter Run-Length encoding/decoding mode. Set this bit to "0" to disable the Transmitter Run-Length encoding/decoding mode.
2	R/W	0	**Transmitter Deferral (TXENDF)** This bit is used to avoid Transmitter underrun condition. When this bit is set to "1", the Transmitter FIFO data will be retained until the transmitter time-out condition occurs or the FIFO reaches full.
1 – 0	R/W	0	**Transmitter Modulation Pulse Mode (TXMPM[1:0])** These two bits are used to define the Transmitter modulation pulse mode. **TXMPM[1:0] Modulation Pulse Mode** C_pls mode (Default): Pulses are generated continuously for the entire logic "0" bit time 8_pls mode: 8 pulses are generated for each logic "0" bit 6_pls mode: 6 pulses are generated for each logic "0" bit 11: Reserved

9.9.6.5 CIR Transmitter Control Register 2 (TCR2)

The TCR2, an 8-bit **read/write** register, is used to determine the carrier frequency.

Address: Base address + 4h

Bit	R/W	Default	Description
7 – 3	R/W	01011	**Carrier Frequency (CFQ[4:0])** These five bits are used to determine the modulation carrier frequency. See Table 9-45.
2 – 0	R/W	100	**Transmitter Modulation Pulse Width (TXMPW[2:0])** These three bits are used to set the Transmitter Modulation pulse width. The duty cycle of the carrier will be determined according to the settings of Carrier Frequency and the selection of Transmitter Modulation Pulse Width.

TXMPW[2:0]	HCFS = 0	HCFS = 1
000	Reserved	Reserved
001	Reserved	Reserved
010	6 µs	0.7 µs
011	7 µs	0.8 µs
100	**8.7 µs**	**0.9µs (Default)**
101	10.6 µs	1.0 µs
110	13.3 µs	1.16 µs
111	Reserved	Reserved

Table 9-45. Modulation Carrier Frequency

CFQ	Low Frequency (HCFS =0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	**38 kHz (Default)**	**480 kHz (Default)**
01100	39 kHz	-
01101	40 kHz	500 kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44 kHz	-
10010	45 kHz	-
10011	46 kHz	-
10100	47 kHz	-
10101	48 kHz	-
10110	49 kHz	-
10111	50 kHz	-
11000	51 kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55 kHz	-
11101	56 kHz	-
11110	57 kHz	-
11111	58 kHz	-

Table 9-46. Receiver Demodulation Low Frequency (HCFS = 0)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28k
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29k
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30k
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31k
00101	30	34	28	36	26	38	24	40	22	42	20	44	32k
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33k
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34k
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35k
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36k
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37k
01011	**35.63**	**40.38**	**33.25**	**42.75**	**30.88**	**45.13**	28.5	**47.5**	**26.13**	**49.88**	**23.75**	**52.25**	**38k**
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39k
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40k
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41k
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42k
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43k
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.25	57.75	27.5	60.5	44k
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45k
10011	43.13	48.88	40.25	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46k
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47k
10101	45	51	42	54	39	57	36	60	33	63	30	66	48k
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49k
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50k
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51k
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52k
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53k
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54k
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55k
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56k
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57k

Table 9-47. Receiver Demodulation High Frequency (HCFS = 1)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00011	375	425	350	450	325	475	300	500	275	525	250	550	400k
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450k
01011	450	510	420	540	390	570	360	600	330	630	300	660	**480k**
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500k

9.9.6.6 CIR Baud Rate Divisor Low Byte Register (BDLR)

The BDLR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base address + 5h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor Low Byte (BDLR[7:0])** These bits are the low byte of the register used to divide the Baud Rate clock.

9.9.6.7 CIR Baud Rate Divisor Register High Byte (BDHR)

The BDHR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base address + 6h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor High Byte (BDHR[7:0])** These bits are the high byte of the register used to divide the Baud Rate clock.

Baud rate divisor = 115200 / baud rate
Ex1: 2400 bps → 115200 /2400 = 48 → 48(d) = 0030(h)
BDHR = 00(h), BDLR = 30(h)
Ex2: bit width = 0.565 ms → 1770 bps → 115200 / 1770 = 65 (d) = 41(h)
BDHR = 00(h), BDLR = 41(h)

9.9.6.8 CIR Transmitter Status Register (TSR)

The TSR, an 8-bit **read only** register, provides the Transmitter FIFO status.

Address: Base address + 5h

Bit	R/W	Default	Description
7-6	RO	-	**Reserved**
5-0	RO	000000	**Transmitter FIFO Byte Count (TXFBC[5:0])** Return the number of bytes left in the Transmitter FIFO.

9.9.6.9 CIR Receiver FIFO Status Register (RSR)

The RSR, an 8-bit **read only** register, provides the Receiver FIFO status.

Address: Base address + 6h

Bit	R/W	Default	Description
7	RO	0	**Receiver FIFO Time-out (RXFTO)** This bit will be set to "1" when a Receiver FIFO time-out condition occurs. The conditions that must exist for a Receiver FIFO time-out condition to occur include the followings: a. At least one byte has been in the Receiver FIFO is not empty for 64 ms or more, and b. The receiver has been inactive (RXACT=0) for over 64 ms or more, and c. More than 64 ms have elapsed since the last byte was read from the Receiver FIFO by the CPU
6	-	-	**Reserved**
5 – 0	RO	000000	**Receiver FIFO Byte Count (RXFBC)** Return the number of bytes left in the Receiver FIFO.

9.9.6.10 CIR Interrupt Identification Register (IIR)

The IIR, an 8-bit **read only** register, is used to identify the pending interrupt.

Address: Base address + 7h

Bit	R/W	Default	Description
7 - 3	-	-	**Reserved**
2 – 1	RO	00	**Interrupt Identification (IID[1:0])** These two bits are used to identify the source of the pending interrupt. **IID[1:0] Interrupt Source** 00 No interrupt 01 Transmitter Low Data Level Interrupt 10 Receiver Data Stored Interrupt 11 Receiver FIFO Overrun Interrupt
0	RO	1	**Interrupt Pending (IIP)** This bit will be set to "1" while an interrupt is pending.

9.10 Game Port Interface

The Game port integrates four timers for two joysticks. The IT8705F allows the Game Port base address to be located within the host I/O address space 100h to 0FFFh. Currently, most game software assume that the Game (or Joystick) I/O port is located at 201h.

A write to the Game port base address will trigger four timers. A read from the same address returns four bits that correspond to the output from the four timers, and other four status bits corresponding to the joystick buttons will also be returned. A button value of 0 indicates that the button is pressed. When the Game port base address is written, the X/Y timer bits go high. Once the Game port base address is written, each timer output remains high for a duration of time determined by the current joystick position.

9.10.1 Game Port (Base+0h)

Bit	Symbol	Description
7	JSBB2	**Joystick B, Button 2 (pin 56 of Joystick connector)**
6	JSBB1	**Joystick B, Button 1 (pin 55 of Joystick connector)**
5	JSBCY	**Joystick B, Coordinate Y (pin 54 of Joystick connector)**
4	JSBCX	**Joystick B, Coordinate X (pin 53 of Joystick connector)**
3	JSAB2	**Joystick A, Button 2 (pin 52 of Joystick connector)**
2	JSAB1	**Joystick A, Button 1 (pin 51 of Joystick connector)**
1	JSACY	**Joystick A, Coordinate Y (pin 50 of Joystick connector)**
0	JSACX	**Joystick A, Coordinate X (pin 49 of Joystick connector)**

9.11 FLASH ROM Interface

The IT8705F offers a solution for BIOS ROM on ISA-less bus MB. The IT8705F incorporates a unique BIOS ROM interface. The interface decodes the memory cycle of the LPC protocol and translates to an ISA-like memory cycle. As illlustrated in Figure 9-8, the width of the address bus is 18 bits, enabling the interface to support 4MB, 2MB and 1MB ROM chips. The width of the data bus is 8-bit wide. Three control signals are supported by the interface: FCS#, FWE# and FRD#. These three control signals are connected to the chip enable, write enable and output enable signal pins respectively on the ROM chip.

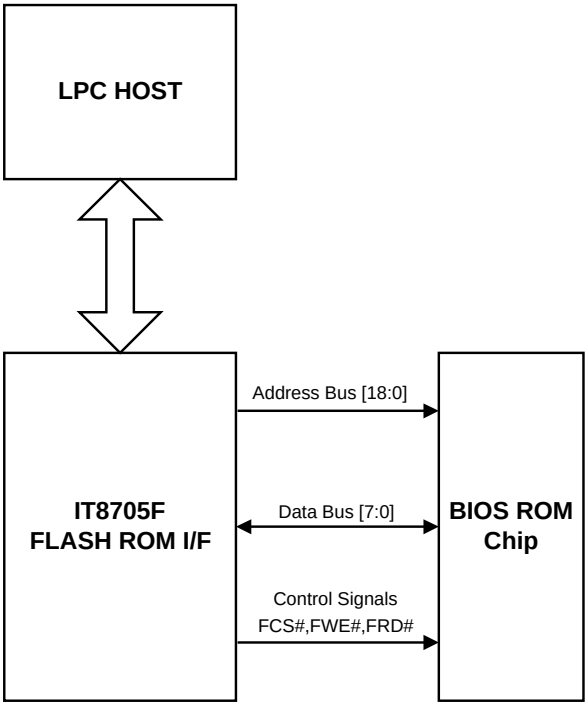


Figure 9-8. FLASH ROM Interface Diagram

Please refer to Table 7-1 decode segments where the BIOS ROM can be located. The selection of decode segment is decided by the power-on strapping. The FCS# signal is asserted when the address of LPC memory cycle falls in the specified segment. The FWE# and FRD# will be asserted as the command type in the memory cycle.

9.12 MIDI Interface

The IT8705F supports the MIDI capability by incorporating hardware to emulate the MPU-401 in the UART mode. It is software compatible with MPU-401 interface, but only supports the **UART mode** (non-intelligent mode). The UART is used to convert parallel data to the serial data required by MIDI. The serial data format is RS-232 like: 1 start bit, 8 data bits, and 1 stop bit. The serial data rate is fixed at 31.25 Kbaud.

9.12.1 MPU-401 Register Interface

The MPU-401 logical device occupies two consecutive I/O spaces. The device also uses an interrupt. Both the base address and the interrupt level are programmable. MIDI Base+0 is the MIDI Data port, and MIDI Base+ 1 is the Command/Status port.

MIDI Data Port: The MIDI Data Port is used to transmit and receive MIDI data. When in UART mode, all transmit data is transferred through a 16-byte FIFO and receive data through another 16-byte FIFO.

MIDI Data Port, MIDI Base+0

Bit	R/W	Description
7-0	R/W	**D7-D0** MIDI data 7-0.

Command/Status Port: The Command register is used to send instructions to the MPU-401. The Status register is used to receive buffer status information from the MPU-401. These two registers occupy the same I/O address.

Command Port, MIDI Base+1

Bit	R/W	Description
7-0	WO	**C7-C0** MIDI instruction command code 7-0.

Status Port, MIDI Base+1

Bit	R/W	Description
7	RO	**RXS** Receive buffer status flag: 0: Data in Receive Buffer. 1: Receive Buffer empty.
6	RO	**TXS** Transmit buffer status flag: 0: Transmit Buffer not full. 1: Transmit Buffer full.
5-0	-	**Reserved, always report 3Fh**

9.12.2 Operation

In the IT8705F, only two MPU-401 device instructions are available: RESET (code: FFh) and UART mode command (code: 3Fh). After power-up reset, the interface is in the **Intelligent mode** (non-UART mode). In this mode, the operation is defined below:

1. All reads of the Data port, MIDI Base+0, return the acknowledged code(FEh). Because only two commands are available, the receive buffer is always loaded with an acknowledge code in the Intelligent mode.
2. All writes to the Data port, MIDI Base+0, are ignored.
3. All writes to the Command port, MIDI Base+1, are monitored and acknowledged as follows:

3Fh: Set the interface into the UART mode and loads an acknowledged code (FEh) into the receive buffer which generates an interrupt
FFh: Set the interface into the initialization condition
Others: Not implemented

UART Mode:

1. All reads of the Data port, MIDI Base+0, return the next byte in the receive buffer FIFO. The serial data received from the MIDI_IN pin is stored in the receive buffer FIFO. The bit 7 RXS of the Status register is updated to reflect the new receive buffer FIFO status. The receive data available interrupt will be issued only if the FIFO has reached its programmed trigger level. The interrupts will be cleared as soon as the FIFO drops below its trigger level. The trigger level is programmable by changing bits 2-1 of the MIDI port Special Configuration Register, LDN8_F0h.
2.
3. All writes to the Data port, MIDI Base+0, are placed in the transmit buffer FIFO. Whenever the transmit buffer FIFO is not empty, the data bytes are read from the buffer in turn and sent out from the MIDI_OUT pin. The bit 6 TXS of the Status Register is updated to reflect the new transmit buffer FIFO status.
4.
5.
6. All writes to the Command port, MIDI Base+1, are monitored and acknowledged below:

FFh: Set the interface into the initialization condition. The interface returns to the intelligent mode
Others: No operation

10. DC Electrical Characteristics

Absolute Maximum Ratings*

Applied Voltage ..... -0.5V to 7.0V

Input Voltage (Vi) ..... -0.5V to VCC+0.5V

Output Voltage (Vo) ..... -0.5V to VCC + 0.3V

Operation Temperature (Topt) .... 0°C to +70°C

Storage Temperature ..... -55°C to +125°C

Power Dissipation 300mW

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DIO24 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 24 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -12 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DIO16 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 16 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -16 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DIO8 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -8 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)[cont'd]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DO40 Type Buffer						
V_{OL}	Low Output Voltage			0.5	V	I_{OL} = 48 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -8 mA
DI Type Buffer						
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC

11. AC Characteristics (Vcc = 5.0V ± 5%, Ta = 0°C to + 70°C)

11.1 Clock Input Timings

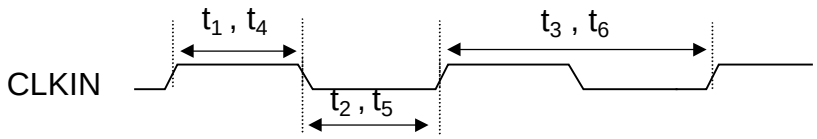


Figure 11-1. Clock Input Timings

Table 11-1. Clock Input Timings AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Clock high pulse width when CLKIN=48 MHz[1]		10.5		nsec
t_2	Clock low pulse width when CLKIN=48 MHz [1]		10.5		nsec
t_3	Clock period when CLKIN=48MHz [1]		21		nsec
t_4	Clock high pulse width when CLKIN=24 MHz [1]		21		nsec
t_5	Clock low pulse width when CLKIN=24 MHz [1]		21		nsec
t_6	Clock period when CLKIN=24 MHz [1]		42		nsec

Not tested. Guaranteed by design.

11.2 LCLK (PCICLK) and LRESET#

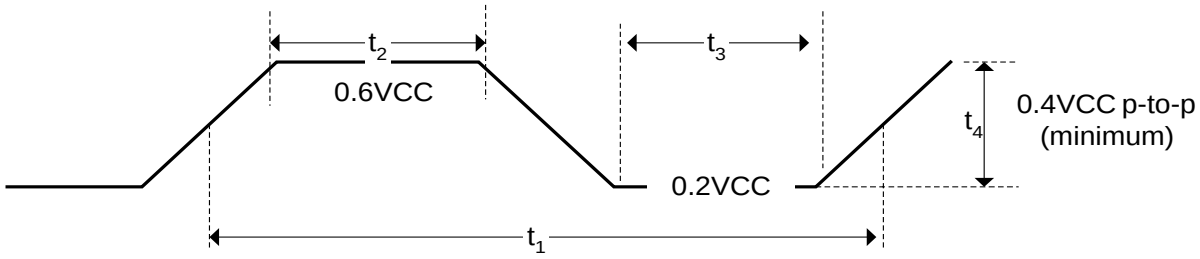


Figure 11-2. LCLK (PCICLK) and LRESET# Timings

Table 11-2. LCLK (PCICLK) and LRESET# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK cycle time	28			nsec
t_2	LCLK high time	11			nsec
t_3	LCLK low time	11			nsec
t_4	LRESET# low pulse width	1.5			µsec

11.3 LPC and SERIRQ Timings

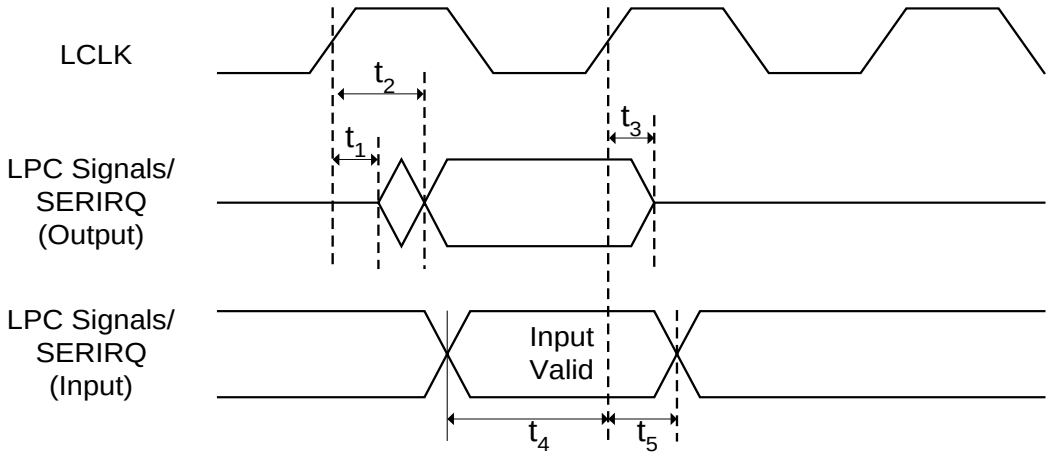


Figure 11-3. LPC and SERIRQ Timings

Table 11-3. LPC and SERIRQ Timings AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay	3			nsec
t_2	Output valid delay			12	nsec
t_3	Active to float delay			6	nsec
t_4	Input setup time	9			nsec
t_5	Input hold time	3			nsec

11.4 Serial Port, ASKIR, SIR and Consumer Remote Control Timings

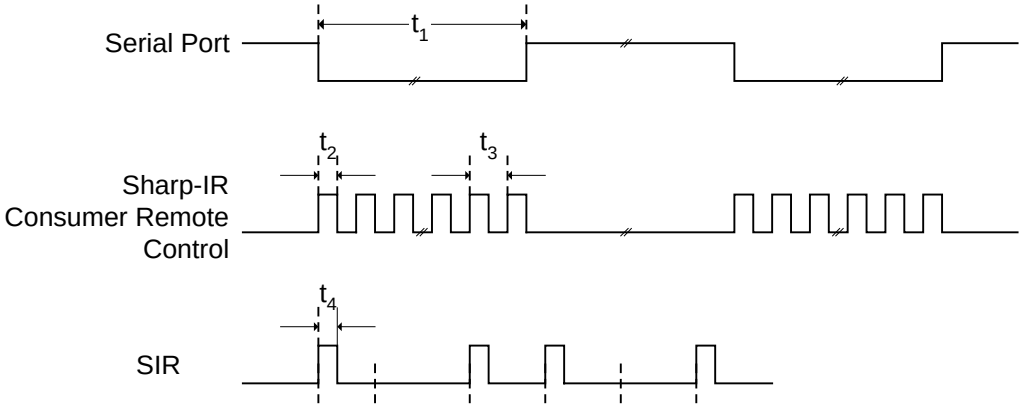


Figure 11-4. Serial Port, ASKIR, SIR and Consumer Remote Control Timings

Table 11-4. Serial Port, ASKIR, SIR and Consumer Remote Control Timings AC Table

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single bit time in serial port and ASKIR	Transmitter	t_{BTN} – 25 [1]	t_{BTN} + 25	nsec
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	nsec
t_2	Modulation signal pulse width in ASKIR	Transmitter	950	1050	nsec
		Receiver	500		nsec
t_3	Modulation signal period in ASKIR	Transmitter	1975	2025	nsec
		Receiver	2000X(23/24)	2000X(25/24)	nsec
t_4	SIR signal pulse width	Transmitter, Variable	(3/16) x t_{BTN} – 25	(3/16) x t_{BTN} + 25	nsec
		Transmitter, Fixed	1.48	1.78	µsec
		Receiver	1		µsec

t_{BTN} is the nominal bit time in Serial Port, ASKIR, and SIR. It is determined by the setting on the Baud Rate Generator Divisor registers.

11.5 Modem Control Timings

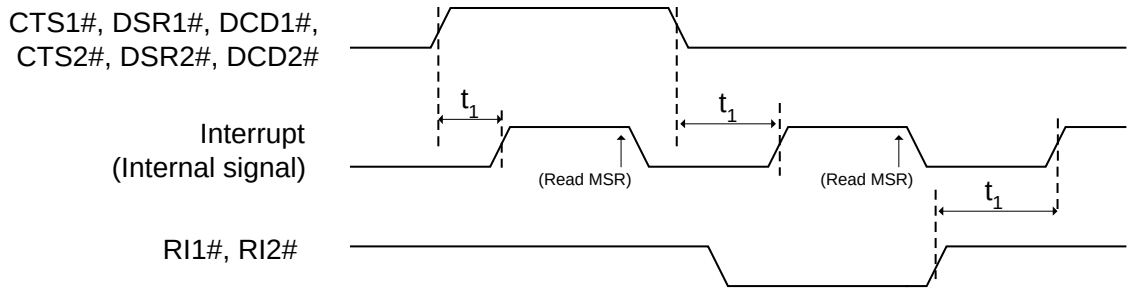


Figure 11-5. Modem Control Timings

Table 11-5. Modem Control Timings AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay			40	nsec

11.6 Floppy Disk Drive Timings

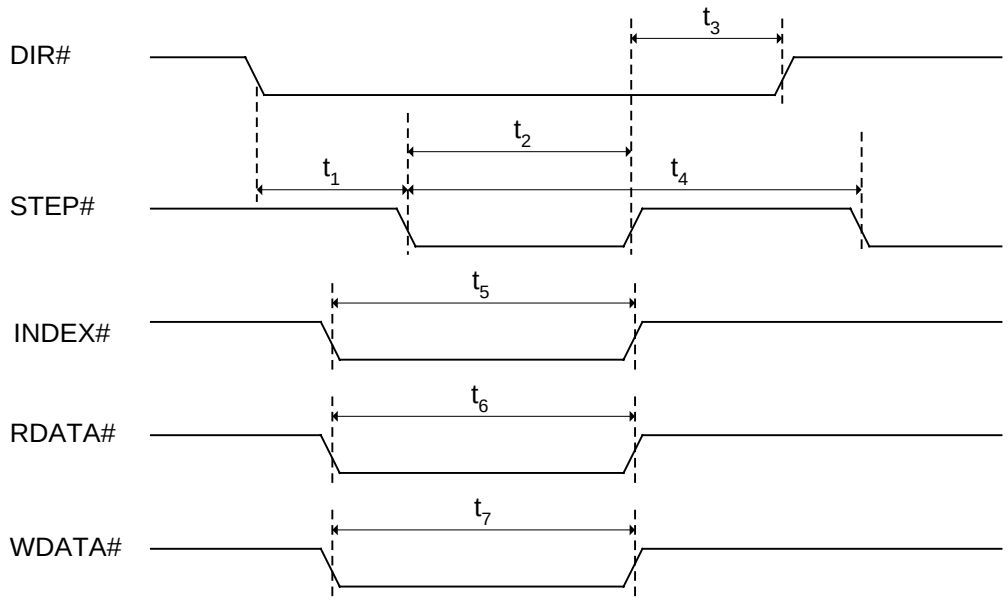


Figure 11-6. Floppy Disk Drive Timings

Table 11-6. Floppy Disk Drive Timings AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	DIR# active to STEP# low		4X t_{mclk} [1]		nsec
t_2	STEP# active time (low)		24X t_{mclk}		nsec
t_3	DIR# hold time after STEP#		t_{SRT} [2]		msec
t_4	STEP# cycle time		t_{SRT}		msec
t_5	INDEX# low pulse width	2X t_{mclk}			nsec
t_6	RDATA# low pulse width	40			nsec
t_7	WDATA# low pulse width		1X t_{mclk}		nsec

1. t_{mclk} is the cycle of main clock for the microcontroller of FDC. t_{mclk} =8M/ 4M/ 2.4M/ 2M for 1M/ 500K/ 300K/ 250K bps transfer rates respectively.
2. t_{SRT} is the cycle of the Step Rate Time. Please refer to the functional description of the SPECITY command of FDC.

11.7 EPP Address or Data Write Cycle

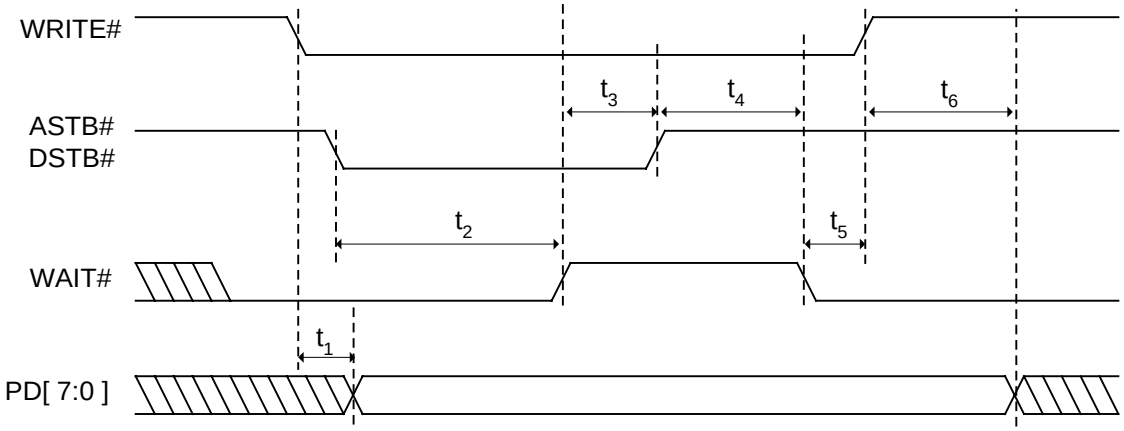


Figure 11-7. EPP Address or Data Write Cycle

Table 11-7. EPP Address or Data Write Cycle AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	WRITE# asserted to PD[7:0] valid			50	nsec
t_2	ASTB# or DSTB# asserted to WAIT# de-asserted	0		10	nsec
t_3	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_4	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_5	WAIT# asserted to WRITE# de-asserted	65			nsec
t_6	PD[7:0] invalid after WRITE# de-asserted	0			nsec

11.8 EPP Address or Data Read Cycle

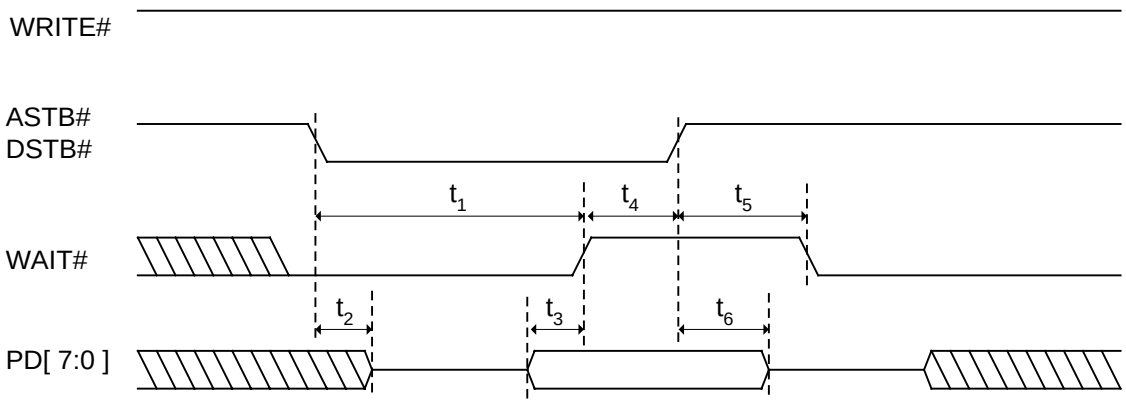


Figure 11-8. EPP Address or Data Read Cycle

Table 11-8. EPP Address or Data Read Cycle AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	ASTB# or DSTB# asserted to WAIT# de-asserted			10	nsec
t_2	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			nsec
t_3	PD[7:0] valid to WAIT# de-asserted	0			nsec
t_4	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_5	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_6	PD[7:0] invalid after ASTB# or DSTB# de-asserted	20			nsec

11.9 ECP Parallel Port Forward Timings

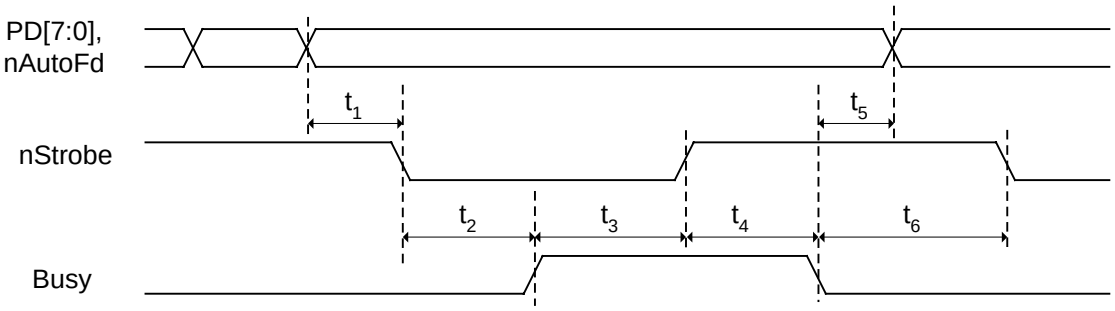


Figure 11-9. ECP Parallel Port Forward Timings

Table 11-9. ECP Parallel Port Forward Timings AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] and nAutoFd valid to nStrobe asserted			50	nsec
t_2	nStrobe asserted to Busy asserted	0			nsec
t_3	Busy asserted to nStrobe de-asserted	70		170	nsec
t_4	nStrobe de-asserted to Busy de-asserted	0			nsec
t_5	Busy de-asserted to PD[7:0] and nAutoFd changed	80		180	nsec
t_6	Busy de-asserted to nStrobe asserted	70		170	nsec

11.10 ECP Parallel Port Backward Timings

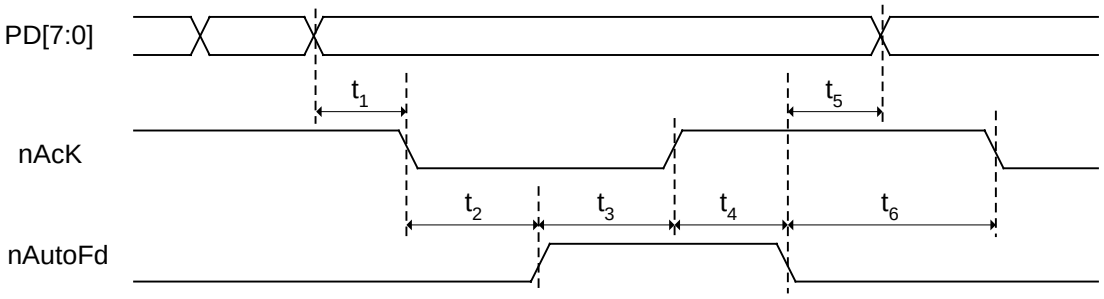


Figure 11-10. ECP Parallel Port Backward Timings

Table 11-10. ECP Parallel Port Backward Timings AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] valid to nAck asserted	0			nsec
t_2	nAck asserted to nAutoFd asserted	70		170	nsec
t_3	nAutoFd asserted to nAck de-asserted	0			nsec
t_4	nAck de-asserted to nAutoFd de-asserted	70		170	nsec
t_5	nAutoFd de-asserted to PD[7:0] changed	0			nsec
t_6	nAutoFd de-asserted to nAck asserted	0			nsec

11.11 Flash ROM I/F Write Timings

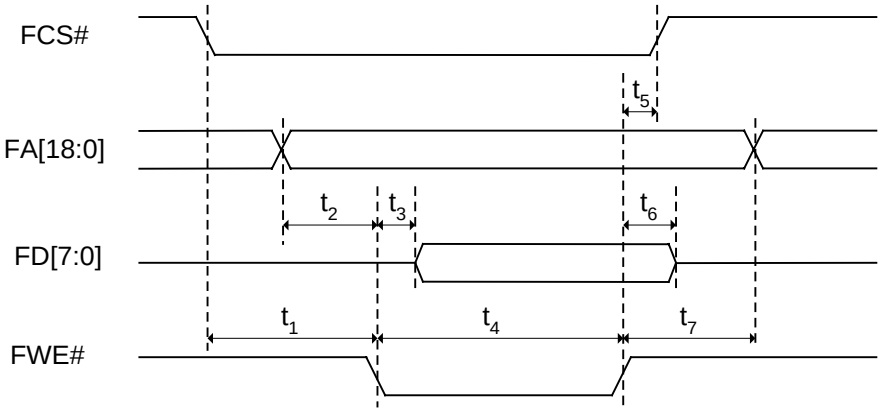


Figure 11-11. Flash ROM I/F Write Timings

Table 11-11. Flash ROM I/F Write Timing AC Table

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
t_1	FCS# valid to FWE# asserted	$11Xt_{pci}$			nsec
t_{28}	FA[18:0] valid to FWE# asserted	$4Xt_{pci}$			nsec
t_3	FWE# asserted to FD[7:0] valid		$1Xt_{pci}$		nsec
t_4	FWE# active pulse width		$20Xt_{pci}$		nsec
t_5	FWE# de-asserted to FCS# changed		$(1/2)Xt_{pci}$		nsec
t_6	FWE# de-asserted to FD[7:0] invalid		$1Xt_{pci}$		nsec
t_7	FWE# de-asserted to FA[18:0] changed	$3Xt_{pci}$			nsec

1. t_{pci} is cycle of PCICLK.

11.12 Flash ROM I/F Read Timings

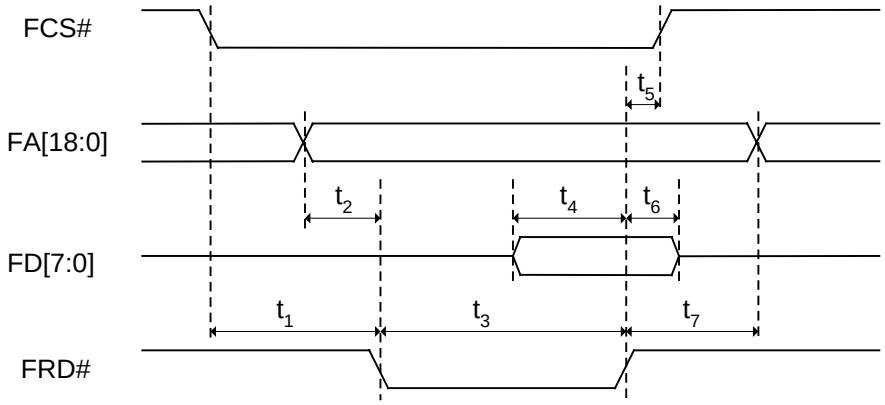


Figure 11-12. Flash ROM I/F Read Timings

Table 11-12. Flash ROM I/F Read Timings AC Table

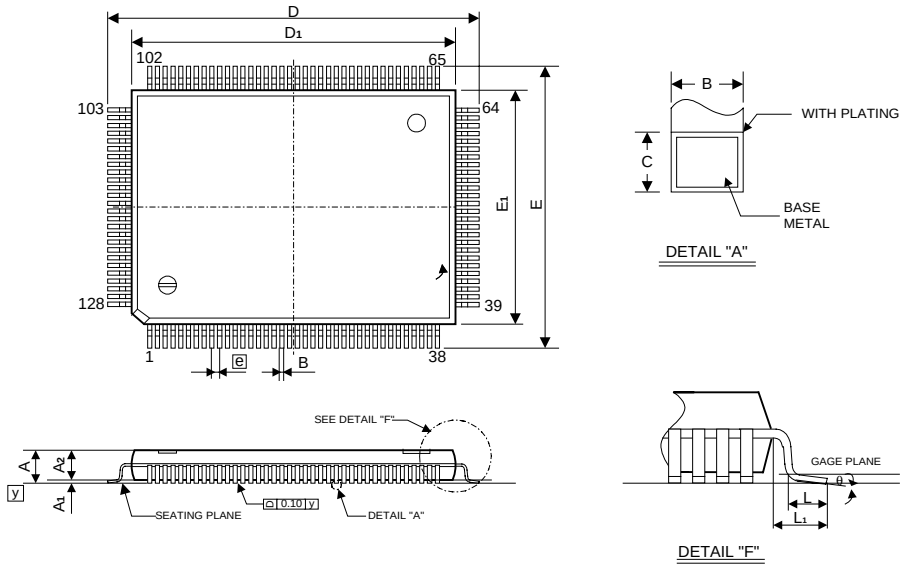
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
t_1	FCS# valid to FRD# asserted	$9Xt_{pci}$			nsec
t_2	FA[18:0] valid to FRD# asserted	$1Xt_{pci}$			nsec
t_3	FRD# active pulse width		$20Xt_{pci}$		nsec
t_4	FD[7:0] setup time	$4Xt_{pci}$			nsec
t_5	FRD# de-asserted to FCS# changed		$1Xt_{pci}$		nsec
t_6	FD[7:0] hold time	0			nsec
t_7	FRD# de-asserted to FA[18:0] changed		$5Xt_{pci}$		nsec

1. t_{pci} is cycle of PCICLK.

12. Package Information

QFP 128L Outline Dimensions

unit: inches/mm



Symbol	Dimension in Inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A_1	0.010	-	-	0.25	-	-
A_2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. DIMENSIONS D_1 AND E_1 DO NOT INCLUDE MOLD PROTRUSION. BUT MOLD MISMATCH IS INCLUDED.
2. DIMENSIONS B DOES NOT INCLUDE DAMBAR PROTRUSION.
3. CONTROLLING DIMENSION: MILLIMETER.

13. Ordering Information

Part No.	Package
IT8705F	128 QFP