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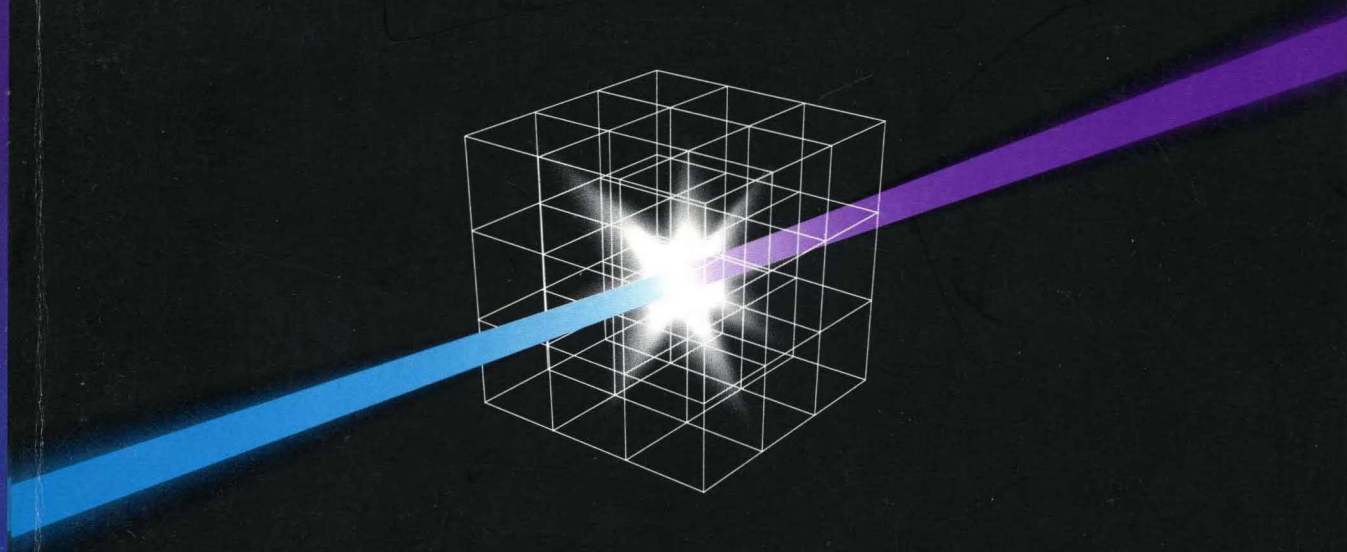


GAL® DATA BOOK

Lattice® Semiconductor Corporation

Lattice
GAL® DATA BOOK
1991

GAL PRODUCT INDEX

Commercial Grade Devices

DEVICE	PINS	t_{PD} (ns)	I_{CC} (mA)	DESCRIPTION	PAGE
GAL16V8A/B	20	7.5, 10, 15, 25	55, 90, 115	E²CMOS Generic PLD	2-1
GAL20V8A/B	24	7.5, 10, 15, 25	55, 90, 115	E²CMOS Generic PLD	2-25
GAL18V10	20	15, 20	115	E²CMOS Universal PLD	2-47
GAL22V10/B	24	10, 15, 25	130	E²CMOS Universal PLD	2-61
GAL26CV12	28	15, 20	130	E²CMOS Universal PLD	2-81
GAL20RA10	24	12, 15, 20, 30	100	E²CMOS Asynchronous PLD	2-95
GAL6001	24	30, 35	150	E²CMOS FPLA	2-109
ispGAL16Z8	24	20, 25	90	E²CMOS In-System-Programmable PLD	2-121

Industrial Grade Devices

DEVICE	PINS	t_{PD} (ns)	I_{CC} (mA)	DESCRIPTION	PAGE
GAL16V8A/B	20	10, 15, 20, 25	65, 130	E²CMOS Generic PLD	2-1
GAL20V8A	24	15, 20, 25	65, 130	E²CMOS Generic PLD	2-25
GAL18V10	20	20	125	E²CMOS Universal PLD	2-47
GAL22V10/B	24	15, 20, 25	150	E²CMOS Universal PLD	2-61
GAL26CV12	28	20	150	E²CMOS Universal PLD	2-81
GAL20RA10	24	20	120	E²CMOS Asynchronous PLD	2-95

MIL-STD-883C Grade Devices

DEVICE	PINS	t_{PD} (ns)	I_{CC} (mA)	DESCRIPTION	PAGE
GAL16V8A/B	20	10, 15, 20, 25, 30	65, 130	E²CMOS Generic PLD	3-5
GAL20V8A	24	15, 20, 25, 30	65, 130	E²CMOS Generic PLD	3-13
GAL22V10/B	24	15, 20, 25, 30	150	E²CMOS Universal PLD	3-19
GAL20RA10	24	20, 25	120	E²CMOS Asynchronous PLD	3-27

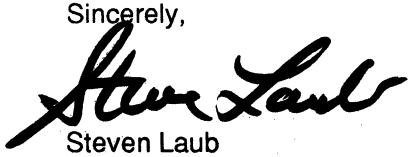
Thank you for your interest in our high performance GAL product line.

As the inventor and world leader of the GAL® device, we at Lattice are dedicated to providing you with the fastest, highest quality and most flexible solution to your logic needs.

In our new 1991 Data Book, you will see that we have substantially expanded our product line and continue to offer the world's highest performance CMOS programmable logic devices.

We look forward to satisfying all of your programmable logic requirements.

Sincerely,



Steven Laub
Vice President and General Manager

GAL Data Book

1991

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TELEX 277338 LSC UR

Section 1: Introduction to Generic Array Logic

Section 2: GAL Datasheets

Section 3: GAL Military Products

Section 4: Quality and Reliability

Section 5: Technical Notes

Section 6: Article Reprints

Section 7: General Information

Introduction to Generic Array Logic

INTRODUCTION

Lattice Semiconductor, located in Hillsboro, Oregon, was founded in 1983 to design, develop and manufacture high-performance semiconductor components. It is a firm belief at Lattice that technological evolution can be accelerated through the continued development of higher-speed and architecturally superior products.

GAL devices are ideal for four important reasons:

1. GAL devices have inherently superior quality and reliability.

2. GAL devices can directly replace PAL devices in nearly every application.

3. GAL devices have the low power consumption of CMOS, one-fourth to one-half that of bipolar devices.

4. GAL devices utilize Output Logic Macrocells (OLMCs), which allow the user to configure outputs as needed.

THE GAL CONCEPT

E^2CMOS — THE IDEAL TECHNOLOGY

Of the three major technologies available for producing PLDs, the technology of choice is clearly E^2CMOS. E^2CMOS offers testability, quality, high speed, low power, and instant erasure.

TESTABILITY

The biggest advantage of E^2CMOS over competing technologies is its inherent testability. Capitalizing on very fast (100ms) erase times, Lattice repeatedly patterns and erases all devices during manufacture. Lattice tests each GAL device for AC, DC, and functional characteristics. The result is guaranteed 100% programming and functional yields.

LOW POWER

Another advantage of E^2CMOS technology is the low power consumption of CMOS. CMOS provides users the immediate benefit of decreased system power requirements allowing for higher reliability and cooler running systems. Low power CMOS technology also permits circuit designs of much higher functional density, because of lower junction temperatures and power requirements on chip. The user benefits because higher functional density means further reduction of chip count and smaller boards in the system.

HIGH SPEED

Also advantageous is the very high speed attainable with Lattice's state-of-the-art E^2CMOS process. Lattice GAL devices are as fast or faster than bipolar and UVCMOS PLDs.

PROTOTYPING AND ERROR RECOVERY

Finally, E^2CMOS gives the user instant erasability with no additional handling or special packages necessary. This provides ideal products for prototyping because designs can be revised instantly, with no waste and no waiting. On the manufacturing floor instant erasability can also be a big advantage for dealing with pattern changes or error recovery. If a GAL device is accidentally programmed to the wrong pattern, simply reprogram the device. No other technology offers this advantage.

Introduction to Generic Array Logic

A LOOK AT OTHER TECHNOLOGIES

Here, the technologies that compete with E²CMOS — bipolar and UVCMOS — are compared with the E²CMOS approach.

BIPOLAR

Bipolar fuse-link technology was the first available for programmable logic devices. Although it offers high speed, it is saddled with high power dissipation. High power dissipation increases your system power supply and cooling requirements, and limits the functional density of bipolar devices.

Another weakness of this technology is the one-time-programmable fuses. Complete testing of bipolar PLDs is impossible because the fuse array cannot be tested before programming. Bipolar PLD manufacturers must rely on complex schemes using test rows and columns to simulate and correlate their device's performance. The result is programming failures at the customer location. Any misprogrammed devices due to mistakes during prototyping or errors on the production floor must be discarded because bipolar PLDs cannot be reprogrammed.

UVCMOS

UVCMOS addresses many weaknesses of the bipolar approach but introduces many shortcomings of its own. This technology requires less power and is reprogrammable, but reprogrammability comes at the expense of slower speeds.

Testability is increased over bipolar since the "fuse" array can be programmed and tested by the manufacturer. The problem here is the long (20 minutes) erase times coupled with the requirement of exposing the devices to ultraviolet light for erasing. This becomes a very expensive step in the manufacturing process. Because of the time involved, patterning and erasing is performed only once — a compromised rather than complete functional test.

Additionally, the devices must be housed in expensive windowed packages to allow users to erase them. Again, programming these devices is time-consuming and cumbersome due to the 20-minute UV exposure required to erase them. As a cost-cutting measure, UVCMOS PLD manufacturers offer their devices in windowless packages. Although windowless packages are less expensive, they cannot be completely tested or reprogrammed. These factors significantly detract from the desirability of this technology.

THE GAL ADVANTAGE

GAL devices are ideal programmable logic devices because, as the name implies, they are architecturally generic. Lattice has employed the macrocell approach, which allows users to define the architecture and functionality of each output. The key benefit to the user is the freedom from being restricted to any specific architecture. This is advantageous at both the manufacturing level and the design level.

DESIGN ADVANTAGES

Early programmable logic devices gave the user the ability to specify a function, but limited them to specific, predetermined output architectures. Comparing the GAL device with fixed-architecture programmable logic devices is much like comparing these same fixed PLDs with SSI/MSI devices. The GAL family is the next generation in simplified system design. The user does not have to search for the architecture that best suits a particular design. Instead, the GAL family's generic architecture lets him configure as he goes.

MANUFACTURING ADVANTAGES

The one-device-does-all approach greatly simplifies manufacturing flow. Inventorying one generic-architecture GAL device type versus having to monitor and maintain many different device types, saves money and minimizes paperwork. Manufacturing flow is much smoother because the handling process is greatly simplified. A generic architecture GAL device also reduces the risk of running out of inventory and halting production, which can be very expensive. Reduced chance of obsolete inventory and easier QA tracking are additional benefits of the generic architecture.

THE IDEAL PACKAGE

Programmable logic devices are ideal for designing today's systems. Lattice Semiconductor believes that the ideal design approach should be supported with the ideal products. It was on this premise that GAL devices were invented. The ideal device—with a generic architecture—fabricated with the ideal process technology, E²CMOS.

Section 1: Introduction to Generic Array Logic

Section 2: GAL Datasheets

Section 3: GAL Military Products

Section 4: Quality and Reliability

Section 5: Technical Notes

Section 6: Article Reprints

Section 7: General Information

DEFINITION OF DATASHEET LEVELS

Datasheet Identification	Product Status	Definition
Preliminary	Sampling or Pre-Production	This datasheet contains preliminary data and supplementary data will be published at a later date. Lattice reserves the right to make changes at any time without notice.
No Identification	Full Production	This datasheet contains final specifications. Lattice reserves the right to make changes at any time without notice.

GAL16V8B
GAL16V8A

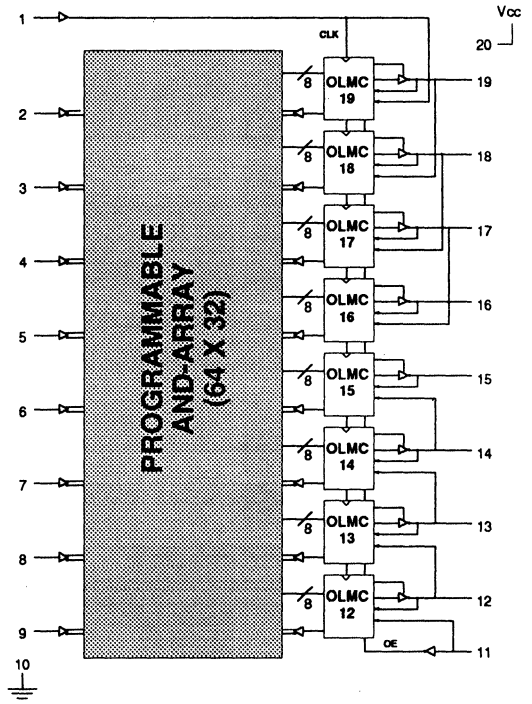
High Performance E²CMOS PLD

2

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **7.5 ns Maximum Propagation Delay**
  - **Fmax = 100 MHz**
  - **5 ns Maximum from Clock Input to Data Output**
  - **TTL Compatible 24 mA Outputs**
  - **UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **75mA Typ Icc on Low Power Device**
  - **45mA Typ Icc on Quarter Power Device**
- **ACTIVE PULL-UPS ON ALL PINS (GAL16V8B)**
- **E² CELL TECHNOLOGY**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **100% Tested/Guaranteed 100% Yields**
  - **High Speed Electrical Erasure (<100ms)**
  - **20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **Maximum Flexibility for Complex Logic Designs**
  - **Programmable Output Polarity**
  - **Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **DMA Control**
  - **State Machine Control**
  - **High Speed Graphics Processing**
  - **Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

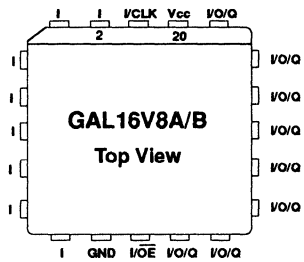
The GAL16V8B, at 7.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8A/B are the PAL architectures listed in the table of the macrocell description section. GAL16V8A/B devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

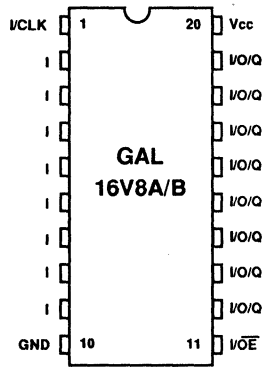
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

PIN CONFIGURATION

PLCC



DIP



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April 1991.Rev.A

GAL16V8A/B ORDERING INFORMATION

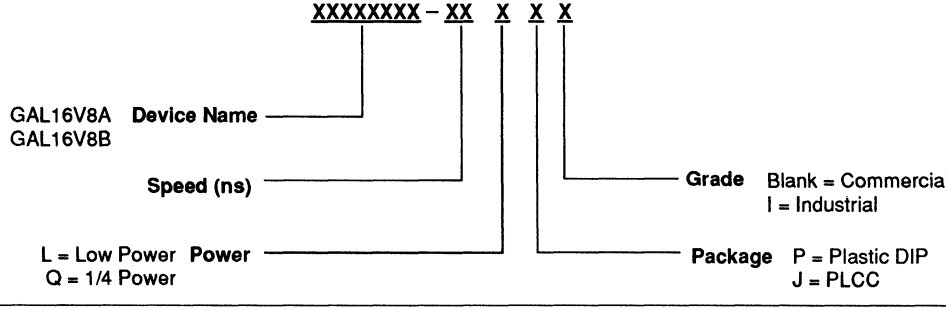
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	115	GAL16V8B-7LP	20-Pin Plastic DIP
			115	GAL16V8B-7LJ	20-Lead PLCC
10	10	7	115	GAL16V8B-10LP	20-Pin Plastic DIP
			115	GAL16V8B-10LJ	20-Lead PLCC
			115	GAL16V8A-10LP	20-Pin Plastic DIP
			115	GAL16V8A-10LJ	20-Lead PLCC
15	12	10	55	GAL16V8A-15QP	20-Pin Plastic DIP
			55	GAL16V8A-15QJ	20-Lead PLCC
			115	GAL16V8A-15LP	20-Pin Plastic DIP
			115	GAL16V8A-15LJ	20-Lead PLCC
25	15	12	55	GAL16V8A-25QP	20-Pin Plastic DIP
			55	GAL16V8A-25QJ	20-Lead PLCC
			90	GAL16V8A-25LP	20-Pin Plastic DIP
			90	GAL16V8A-25LJ	20-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL16V8B-10LPI	20-Pin Plastic DIP
			130	GAL16V8B-10LJI	20-Lead PLCC
15	12	10	130	GAL16V8B-15LPI	20-Pin Plastic DIP
			130	GAL16V8B-15LJI	20-Lead PLCC
			130	GAL16V8A-15LPI	20-Pin Plastic DIP
			130	GAL16V8A-15LJI	20-Lead PLCC
20	13	11	65	GAL16V8A-20QPI	20-Pin Plastic DIP
			65	GAL16V8A-20QJI	20-Lead PLCC
25	15	12	65	GAL16V8A-25QPI	20-Pin Plastic DIP
			65	GAL16V8A-25QJI	20-Lead PLCC
			130	GAL16V8A-25LPI	20-Pin Plastic DIP
			130	GAL16V8A-25LJI	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple, complex,** and **registered.** Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8A/B. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8A and GAL16V8B can emulate. It also shows the OLMC mode under which the GAL16V8A/B emulates the PAL architecture.

PAL Architectures Emulated by GAL16V8A/B	GAL16V8A/B Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

REGISTERED MODE

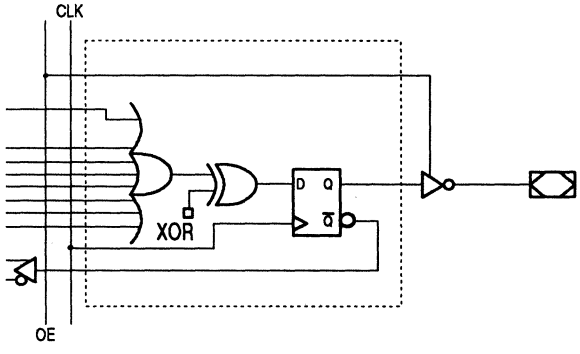
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

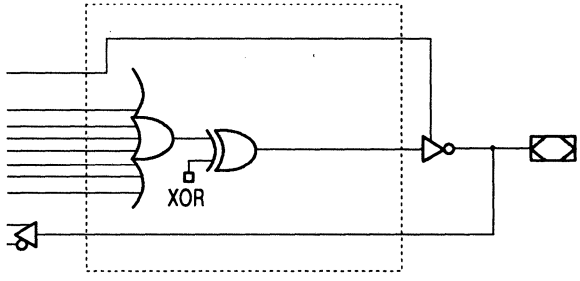
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.



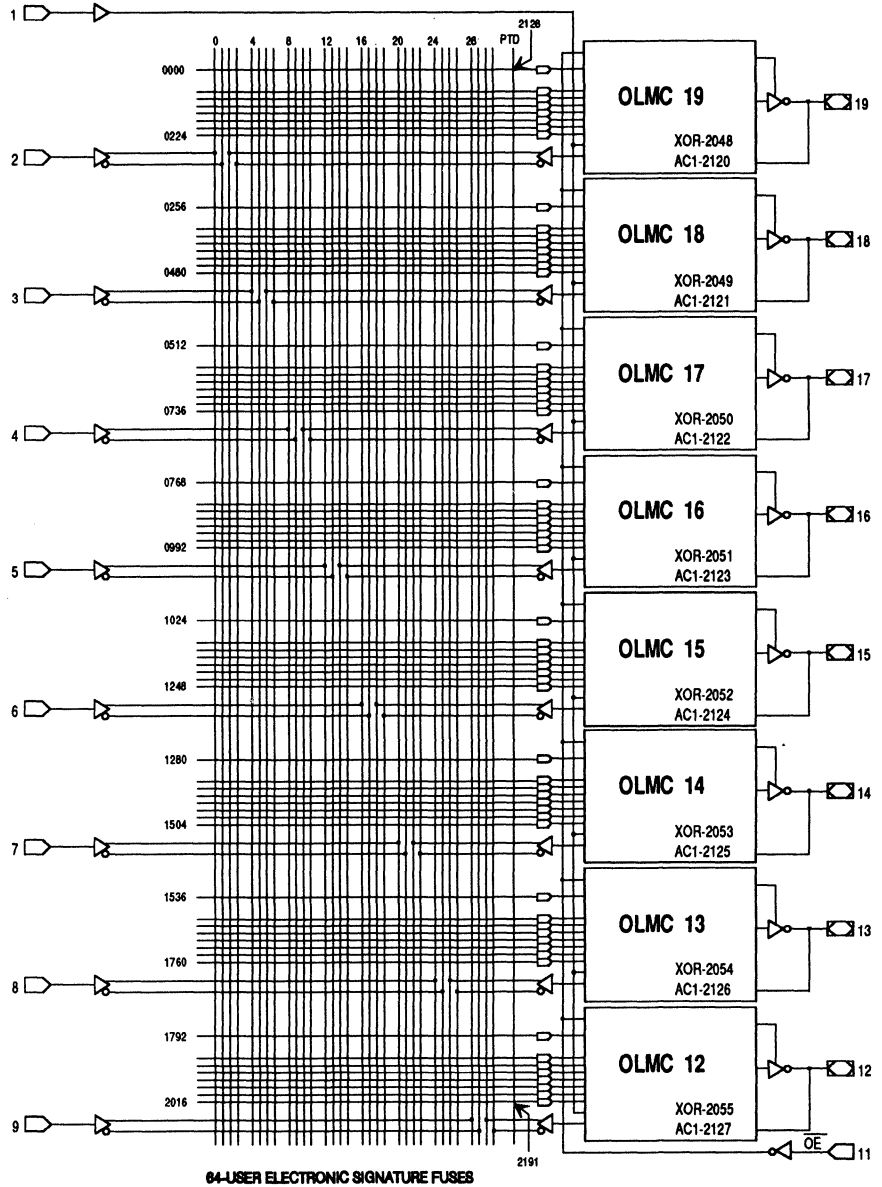
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...	.... 2118, 2119
Byte 7 | Byte 6	.... Byte 1 | Byte 0
M S B	L S B

SYN-2192
AC0-2193

COMPLEX MODE

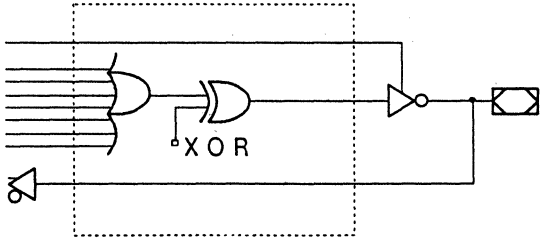
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

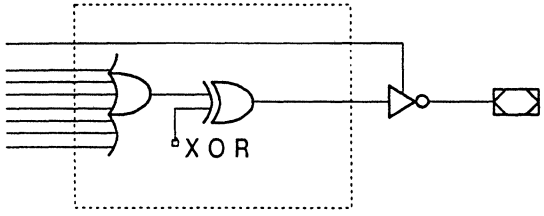
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 13 through Pin 18 are configured to this function.



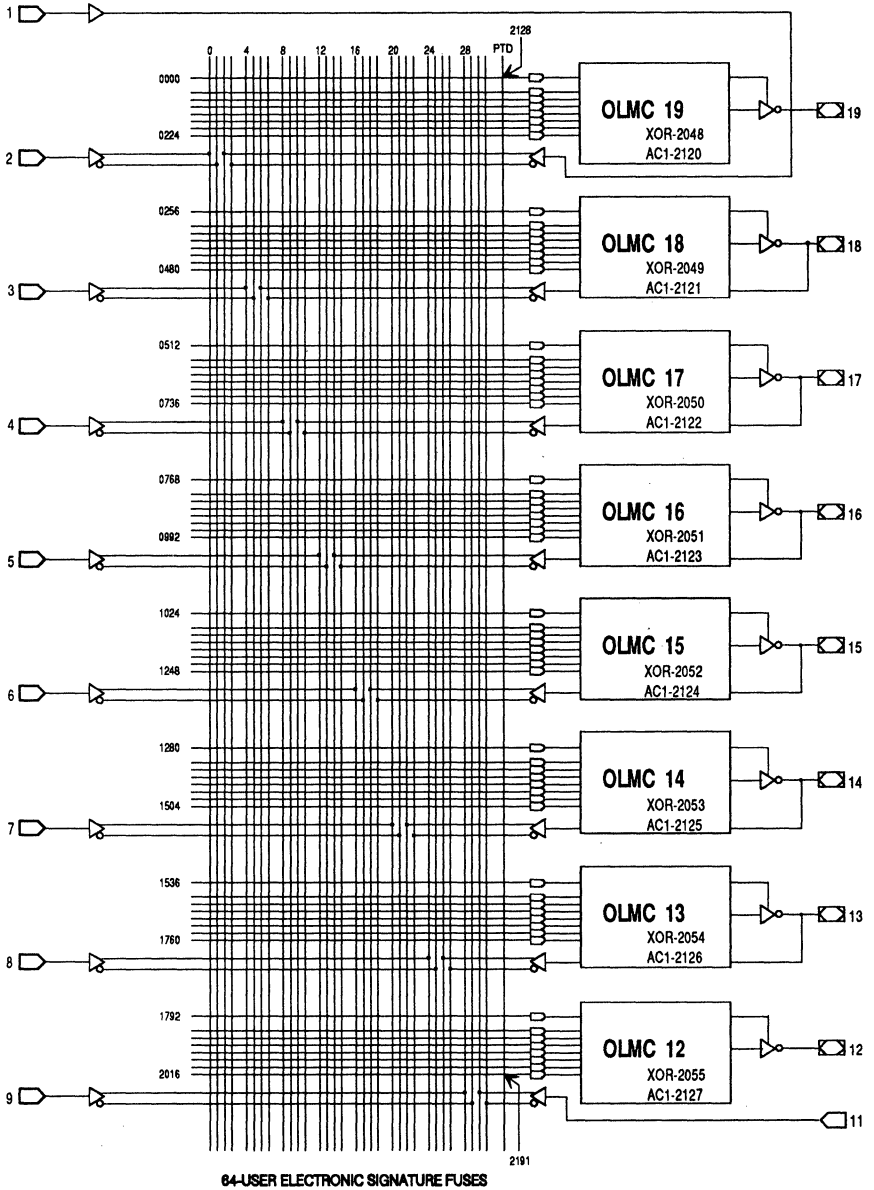
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...	.... 2118, 2119
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2192
AC0-2193

SIMPLE MODE

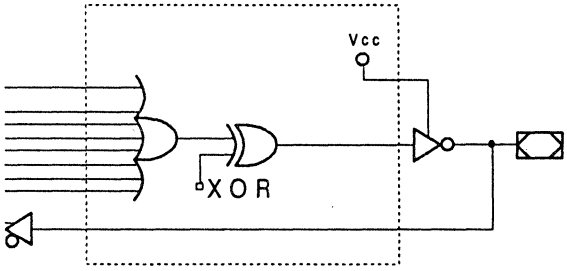
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

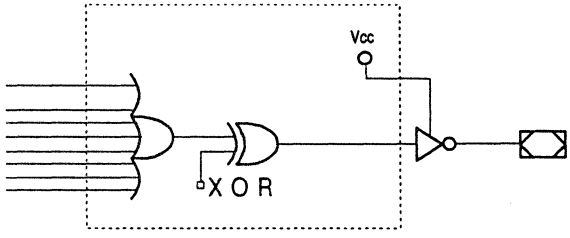
Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used as input or I/O pins, and are only available as dedicated outputs.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



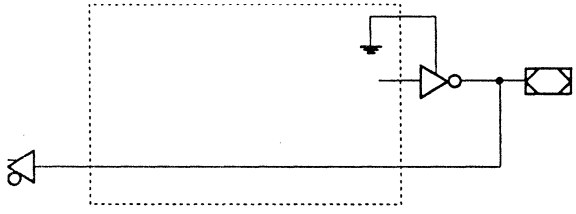
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 15 & 16 are permanently configured to this function.



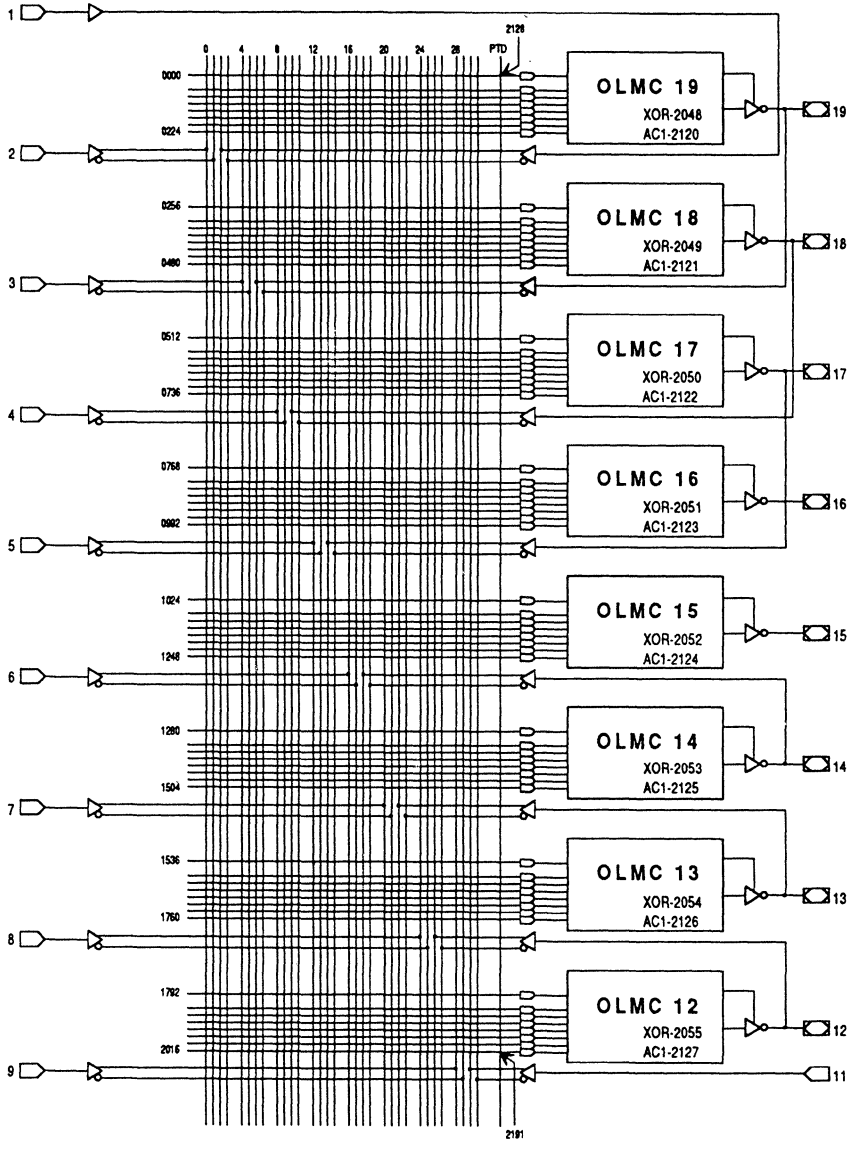
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...	.... 2118, 2119
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2192
AC0-2193

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Ambient Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) .....0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz Outputs Open (no load)	—	75	115	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION		-7		-10		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	8 outputs switching	3	7.5	3	10	ns
			1 output switching	—	7	—	—	ns
tco	1	Clock to Output Delay		2	5	2	7	ns
tcf[2]	—	Clock to Feedback Delay		—	3	—	6	ns
tsu	—	Setup Time, Input or Feedback before Clock↑		7	—	10	—	ns
th	—	Hold Time, Input or Feedback after Clock↑		0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		83.3	—	58.8	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		100	—	62.5	—	MHz
	1	Maximum Clock Frequency with No Feedback		100	—	62.5	—	MHz
twh[4]	—	Clock Pulse Duration, High		5	—	8	—	ns
twl[4]	—	Clock Pulse Duration, Low		5	—	8	—	ns
ten	2	Input or I/O to Output		3	9	3	10	ns
	2	OE↓ to Output		2	6	2	10	ns
tdis	3	Input or I/O to Output		2	9	2	10	ns
	3	OE↑ to Output		1.5	6	1.5	10	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

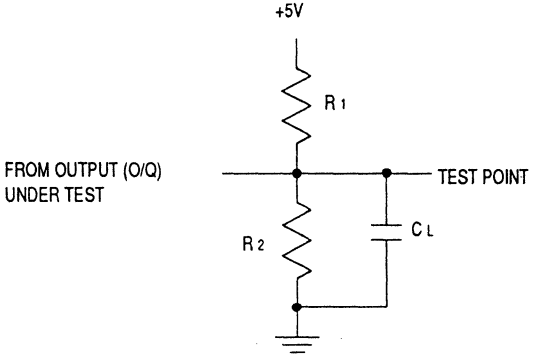
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION			MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage				Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage				2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)			—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$			—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}			—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}			2.4	—	—	V
I_{OL}	Low Level Output Current				—	—	24	mA
I_{OH}	High Level Output Current				—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C			–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V Outputs Open (no load)	f_{toggle} = 15MHz	L -25	—	75	90	mA
			f_{toggle} = 25MHz	L -10/-15	—	75	115	mA
			f_{toggle} = 15MHz	Q -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-10		-15		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	10	3	15	3	25	ns
tco	1	Clock to Output Delay	2	7	2	10	2	12	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	8	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	58.8	—	45.5	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	50	—	40	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	41.6	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	8	—	12	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	8	—	12	—	ns
ten	2	Input or I/O to Output Enabled	—	10	—	15	—	25	ns
	2	OE↓ to Output Enabled	—	10	—	15	—	20	ns
tdis	3	Input or I/O to Output Disabled	—	10	—	15	—	25	ns
	3	OE↑ to Output Disabled	—	10	—	15	—	20	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

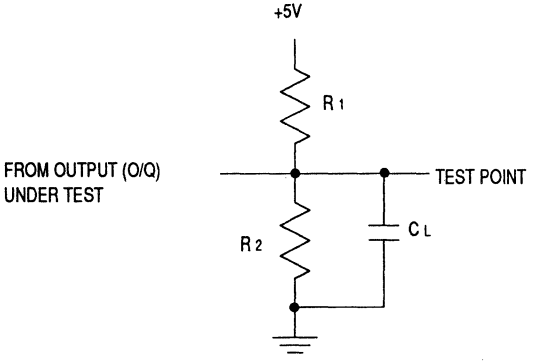
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF



CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Ambient Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
Ambient Temperature (T_A) .....–40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz Outputs Open (no load)	—	75	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-10		-15		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	10	3	15	ns
tco	1	Clock to Output Delay	2	7	2	10	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	8	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	58.8	—	45.5	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	62.5	—	50	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	8	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	8	—	ns
ten	2	Input or I/O to Output	3	10	—	15	ns
	2	OE↓ to Output	2	10	—	15	ns
tdis	3	Input or I/O to Output	2	10	—	15	ns
	3	OE↑ to Output	1.5	10	—	15	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

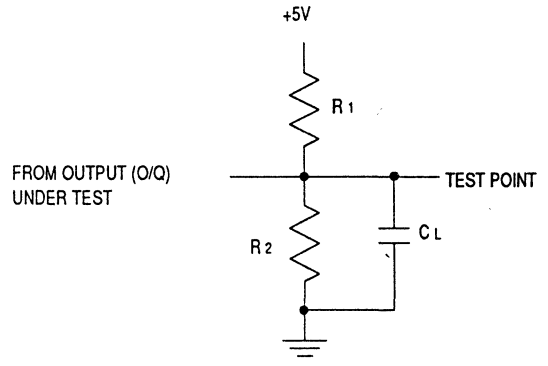
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V, Outputs Open (no load), f_{toggle} = 25MHz, L -15/-25	—	75	130	mA
		f_{toggle} = 15MHz, Q -20/-25	—	45	65	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-15		-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	15	3	20	3	25	ns
tco	1	Clock to Output Delay	2	10	2	11	2	12	ns
tcf[2]	—	Clock to Feedback Delay	—	8	—	9	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	12	—	13	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	45.5	—	41.6	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	45.4	—	40	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	50	—	41.6	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	10	—	12	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	10	—	12	—	ns
ten	2	Input or I/O to Output	—	15	—	20	—	25	ns
	2	OE↓ to Output	—	15	—	18	—	20	ns
tdis	3	Input or I/O to Output	—	15	—	20	—	25	ns
	3	OE↑ to Output	—	15	—	18	—	20	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

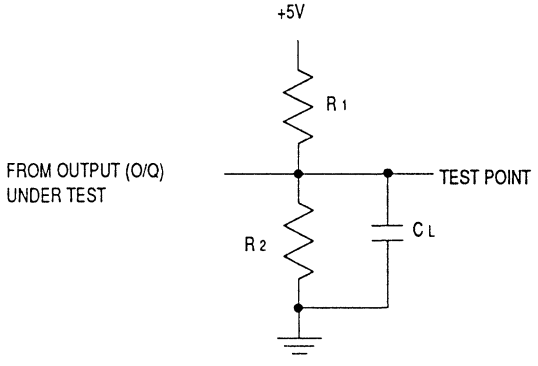
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

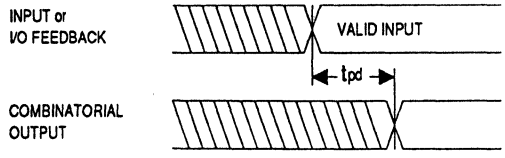
Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

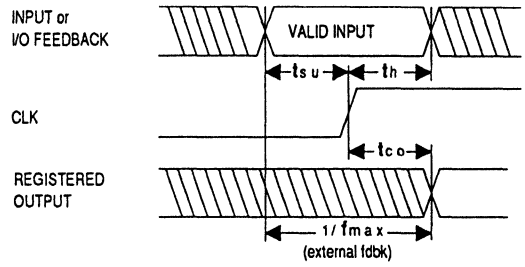


CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

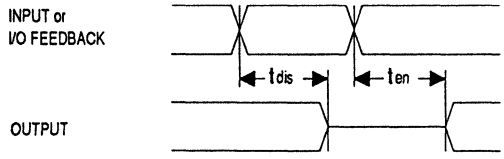
SWITCHING WAVEFORMS



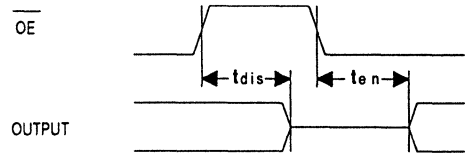
Combinatorial Output



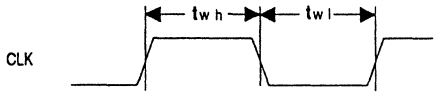
Registered Output



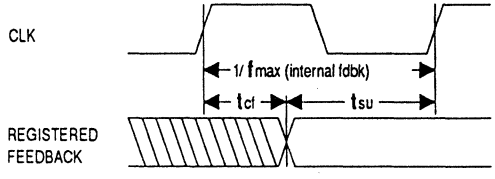
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

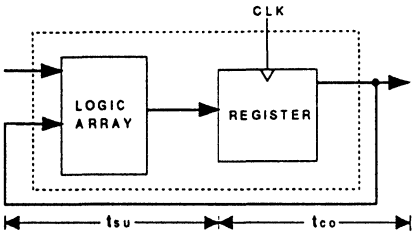


Clock Width



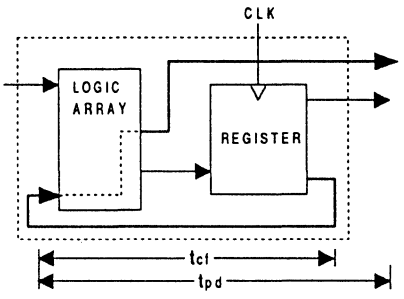
fmax with Feedback

fmax DESCRIPTIONS



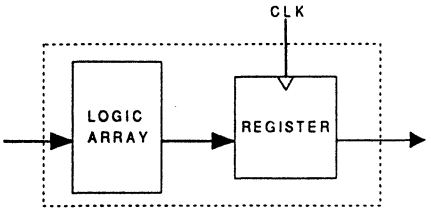
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.



fmax With No Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL16V8A and GAL16V8B device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter checksum.

SECURITY CELL

A security cell is provided in the GAL16V8A and GAL16V8B devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL16V8A and GAL16V8B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

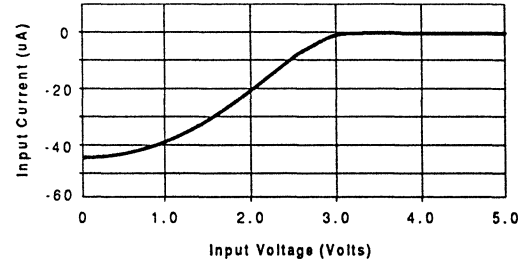
The GAL16V8A and GAL16V8B devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

INPUT BUFFERS

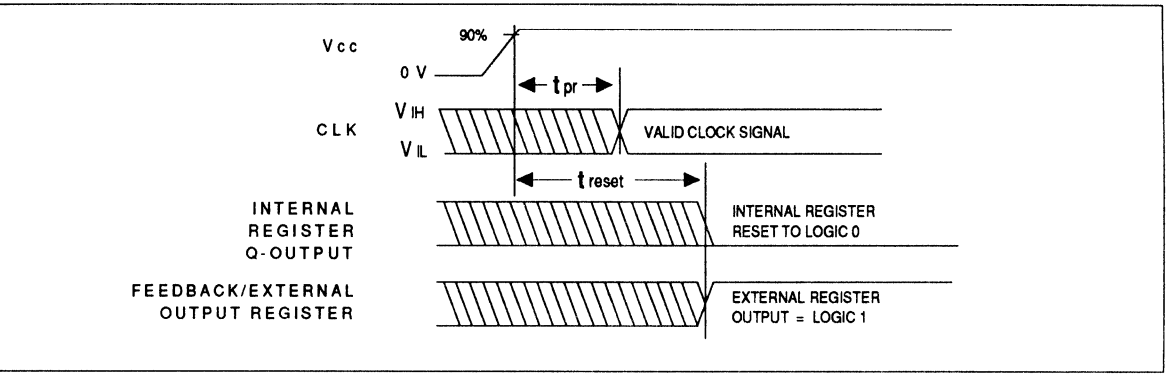
GAL16V8A and GAL16V8B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL16V8B input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). In contrast, the GAL16V8A does not have active pull-ups within their input structures. Lattice recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic



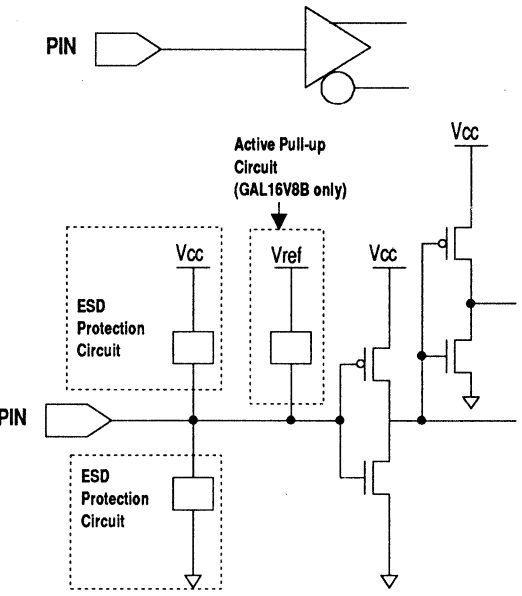
POWER-UP RESET



Circuitry within the GAL16V8A and GAL16V8B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

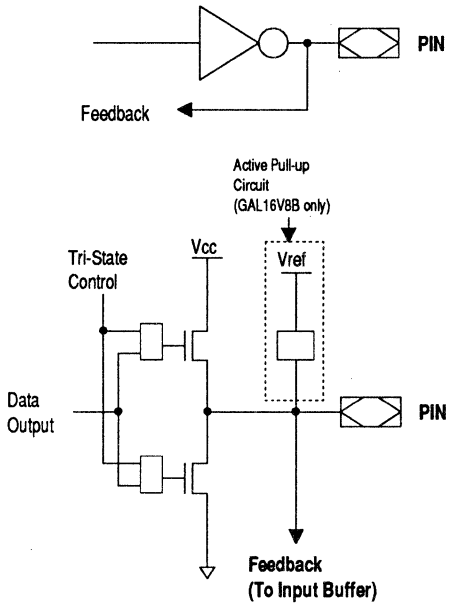
The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16V8A and GAL16V8B. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. Vref = 3.2V

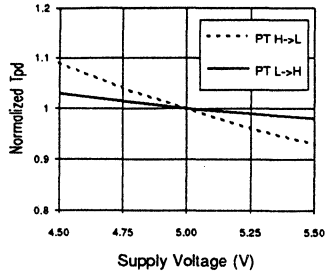
Typical Input



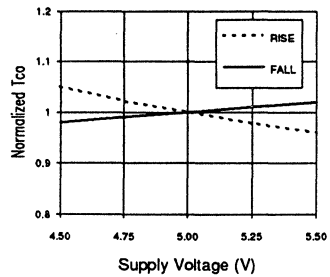
Typ. Vref = 3.2V

Typical Output

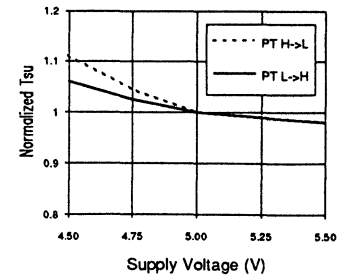
Normalized Tpd vs Vcc



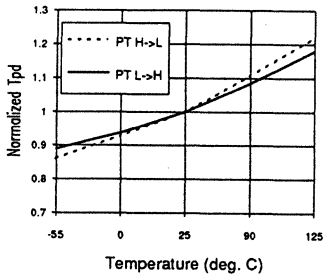
Normalized Tco vs Vcc



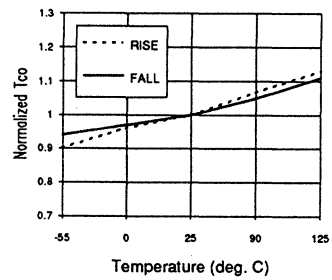
Normalized Tsu vs Vcc



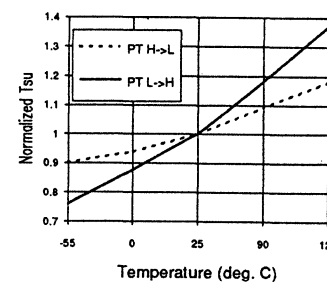
Normalized Tpd vs Temp



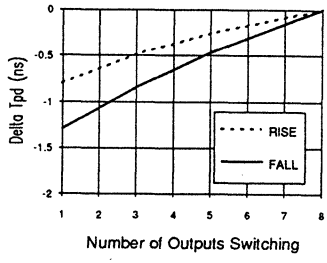
Normalized Tco vs Temp



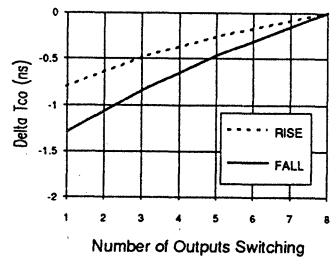
Normalized Tsu vs Temp



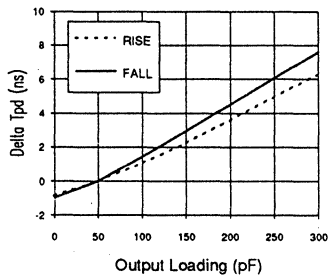
Delta Tpd vs # of Outputs Switching



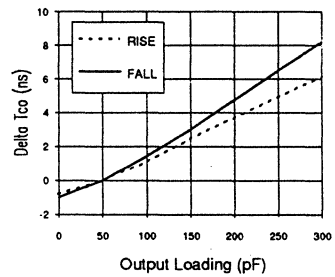
Delta Tco vs # of Outputs Switching



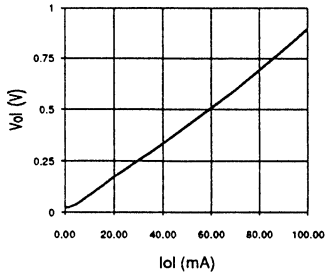
Delta Tpd vs Output Loading



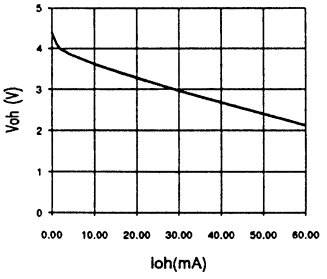
Delta Tco vs Output Loading



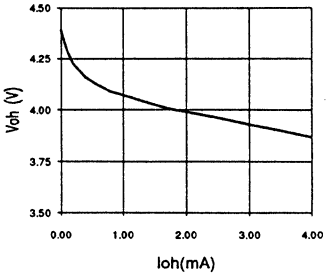
Vol vs Iol



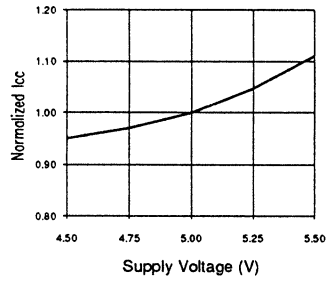
Voh vs Ioh



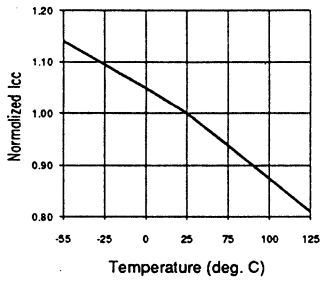
Voh vs Ioh



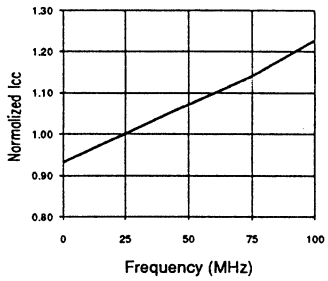
Normalized Icc vs Vcc



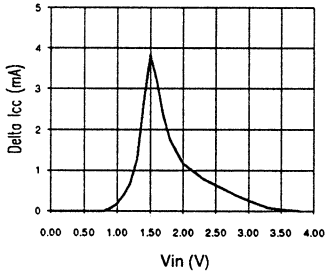
Normalized Icc vs Temp



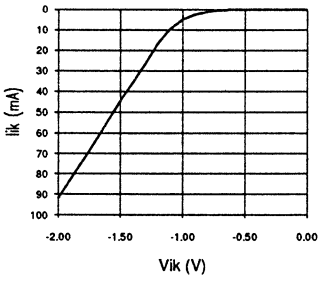
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

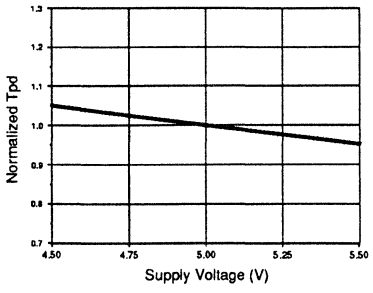


Input Clamp (Vik)

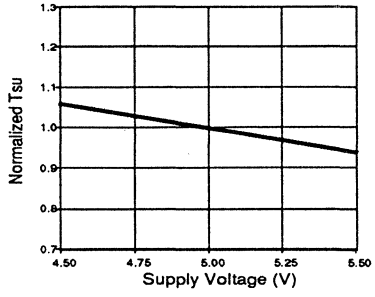


Typical Characteristics

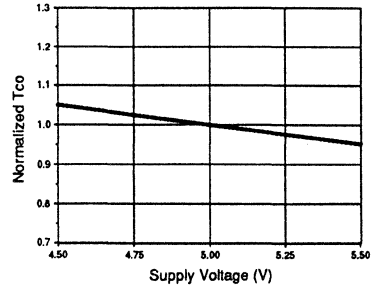
Normalized Tpd vs. Vcc



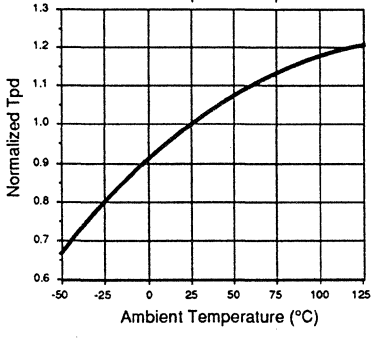
Normalized Tsu vs. Vcc



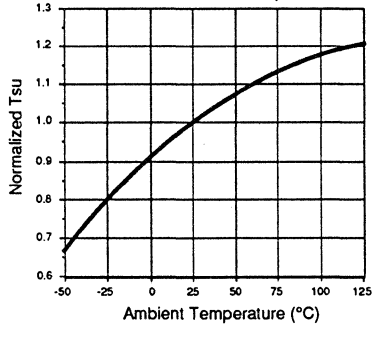
Normalized Tco vs. Vcc



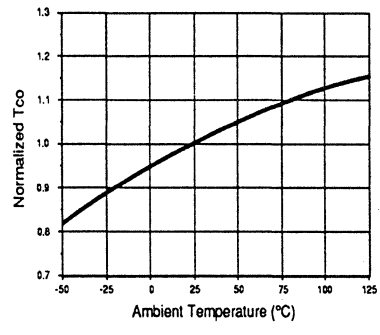
Normalized Tpd vs. Temperature



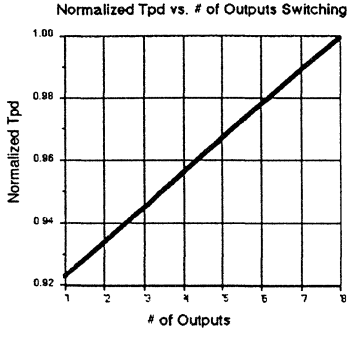
Normalized Tsu vs. Temperature



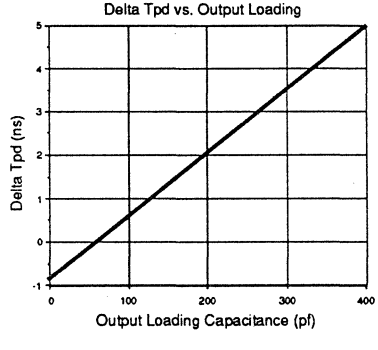
Normalized Tco vs. Temperature



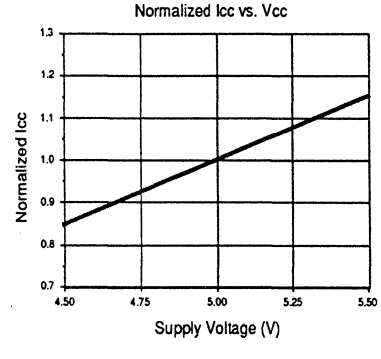
Normalized Tpd vs. # of Outputs Switching



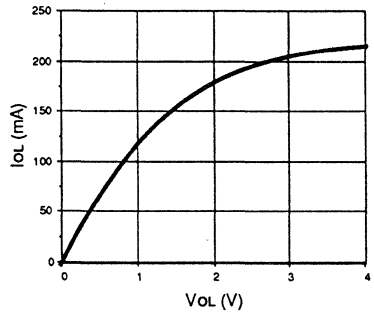
Delta Tpd vs. Output Loading



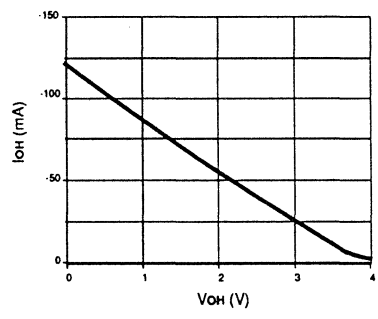
Normalized Icc vs. Vcc



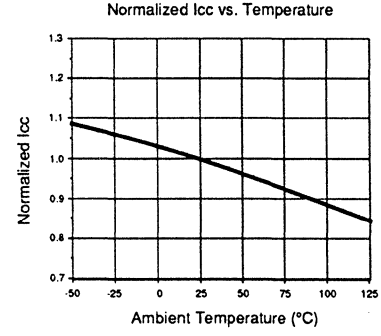
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



Normalized Icc vs. Temperature



GAL20V8B
GAL20V8A

High Performance E²CMOS PLD

2

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Fmax = 100 MHz**
  - **— 5 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 24 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc on Low Power Device**
  - **— 45mA Typ Icc on Quarter Power Device**
- **ACTIVE PULL-UPS ON ALL PINS (GAL20V8B)**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

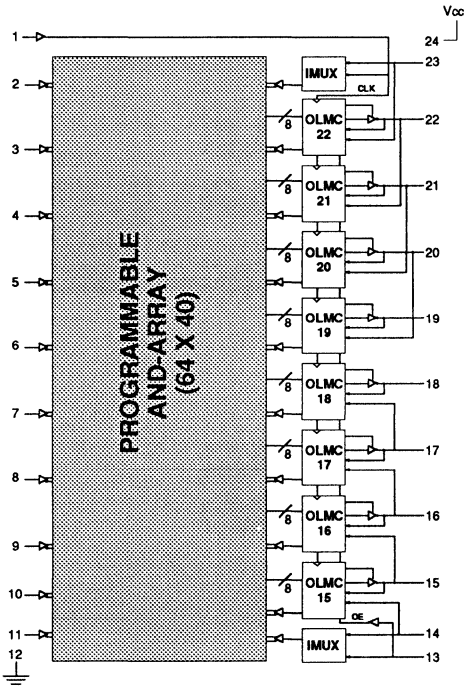
DESCRIPTION

The GAL20V8B, at 7.5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

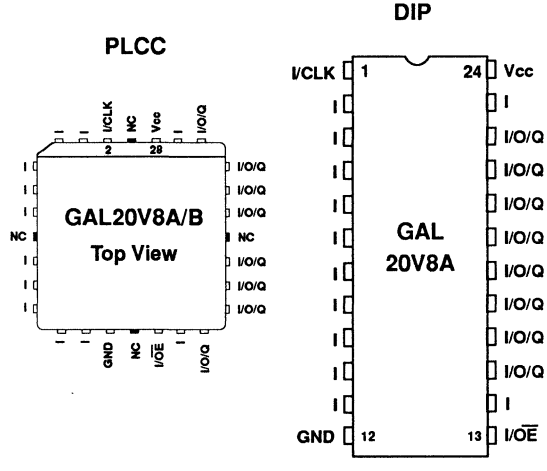
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20V8A/B are the PAL architectures listed in the table of the macrocell description section. GAL20V8A/B devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

May 1991.Rev.A

GAL20V8A/B ORDERING INFORMATION

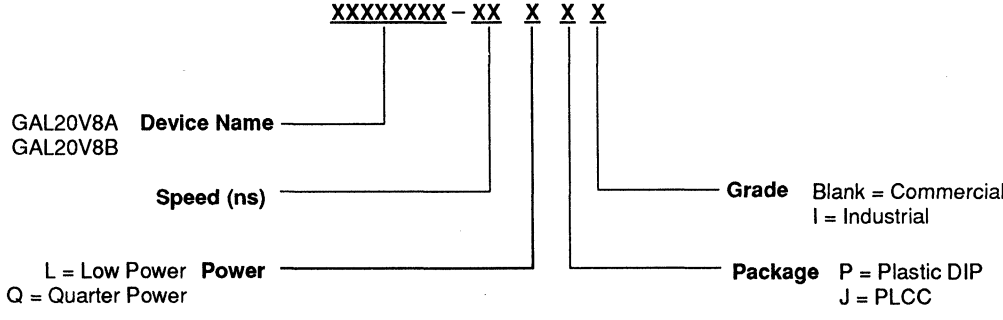
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	115	GAL20V8B-7LJ	28-Lead PLCC
10	10	7	115	GAL20V8B-10LJ	28-Lead PLCC
			115	GAL20V8A-10LP	24-Pin Plastic DIP
			115	GAL20V8A-10LJ	28-Lead PLCC
15	12	10	55	GAL20V8A-15QP	24-Pin Plastic DIP
			55	GAL20V8A-15QJ	28-Lead PLCC
			115	GAL20V8A-15LP	24-Pin Plastic DIP
			115	GAL20V8A-15LJ	28-Lead PLCC
25	15	12	55	GAL20V8A-25QP	24-Pin Plastic DIP
			55	GAL20V8A-25QJ	28-Lead PLCC
			90	GAL20V8A-25LP	24-Pin Plastic DIP
			90	GAL20V8A-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	12	10	130	GAL20V8A-15LPI	24-Pin Plastic DIP
			130	GAL20V8A-15LJI	28-Lead PLCC
20	13	11	65	GAL20V8A-20QPI	24-Pin Plastic DIP
			65	GAL20V8A-20QJI	28-Lead PLCC
25	15	12	65	GAL20V8A-25QPI	24-Pin Plastic DIP
			65	GAL20V8A-25QJI	28-Lead PLCC
			130	GAL20V8A-25LPI	24-Pin Plastic DIP
			130	GAL20V8A-25LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8A/B. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL20V8A and GAL20V8B can emulate. It also shows the OLMC mode under which the devices emulate the PAL architecture.

PAL Architectures Emulated by GAL20V8A/B	GAL20V8A/B Global OLMC Mode
20R8	Registered
20R6	Registered
20R4	Registered
20RP8	Registered
20RP6	Registered
20RP4	Registered
20L8	Complex
20H8	Complex
20P8	Complex
14L8	Simple
16L6	Simple
18L4	Simple
20L2	Simple
14H8	Simple
16H6	Simple
18H4	Simple
20H2	Simple
14P8	Simple
16P6	Simple
18P4	Simple
20P2	Simple

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 13 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 22 and pin 15 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 18 and 19) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R	GAL20V8_C7	GAL20V8_C8	GAL20V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL20V8A
PLDesigner	P20V8R[2]	P20V8C[2]	P20V8C[2]	P20V8A
TANGO-PLD	G20V8R	G20V8C	G20V8AS[3]	G20V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

REGISTERED MODE

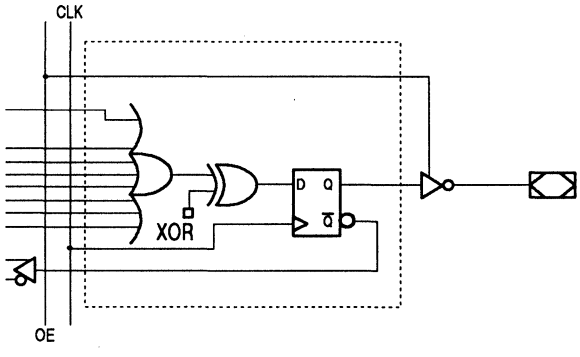
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

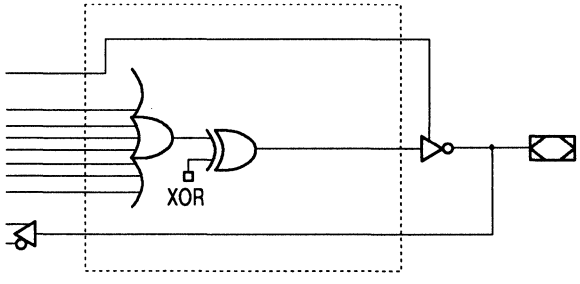
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 13 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$.



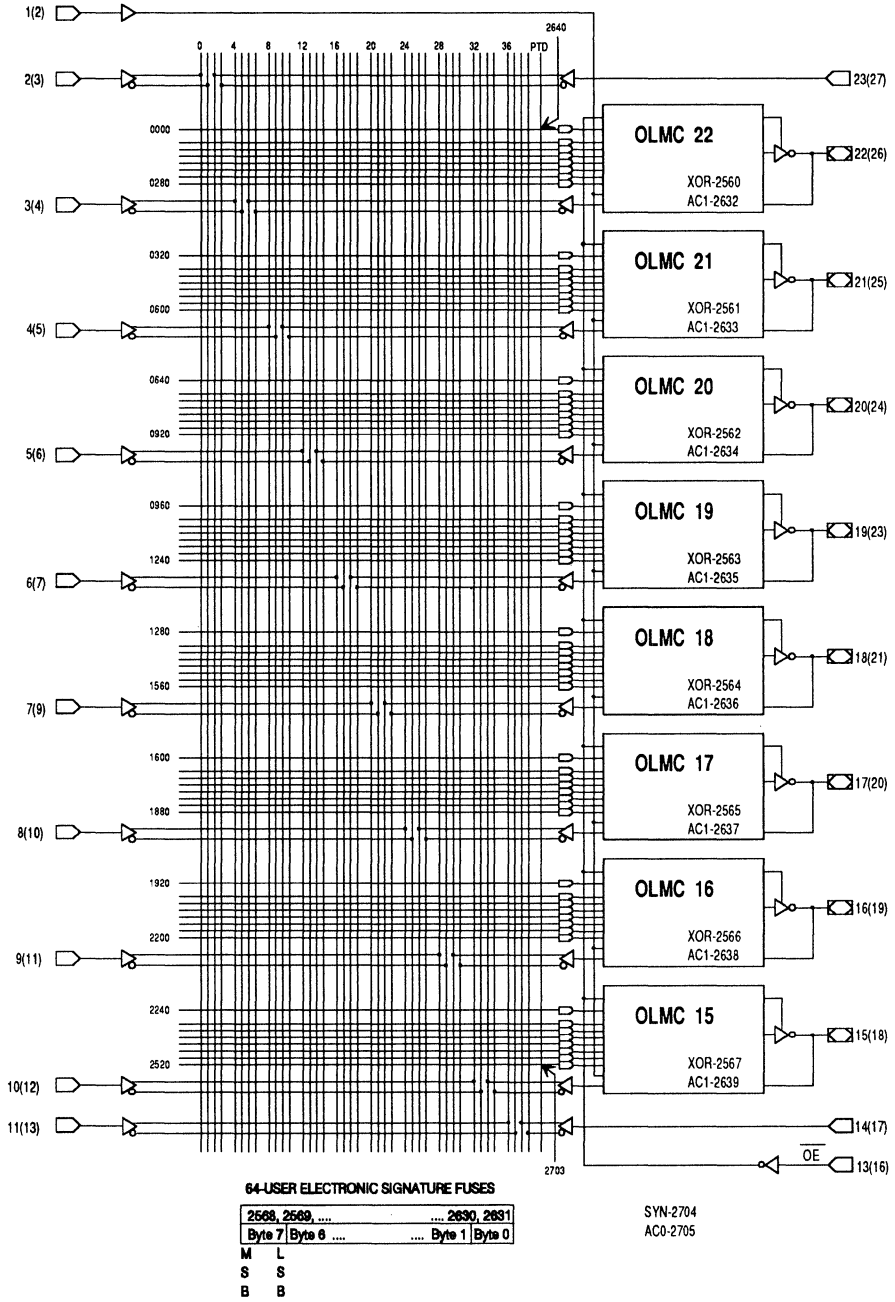
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 Byte 6	.... Byte 1 Byte 0

MSB LSB

SYN-2704
AC0-2705

COMPLEX MODE

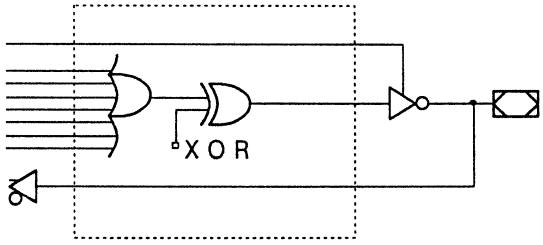
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

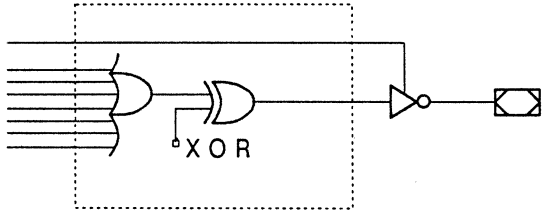
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 16 through Pin 21 are configured to this function.



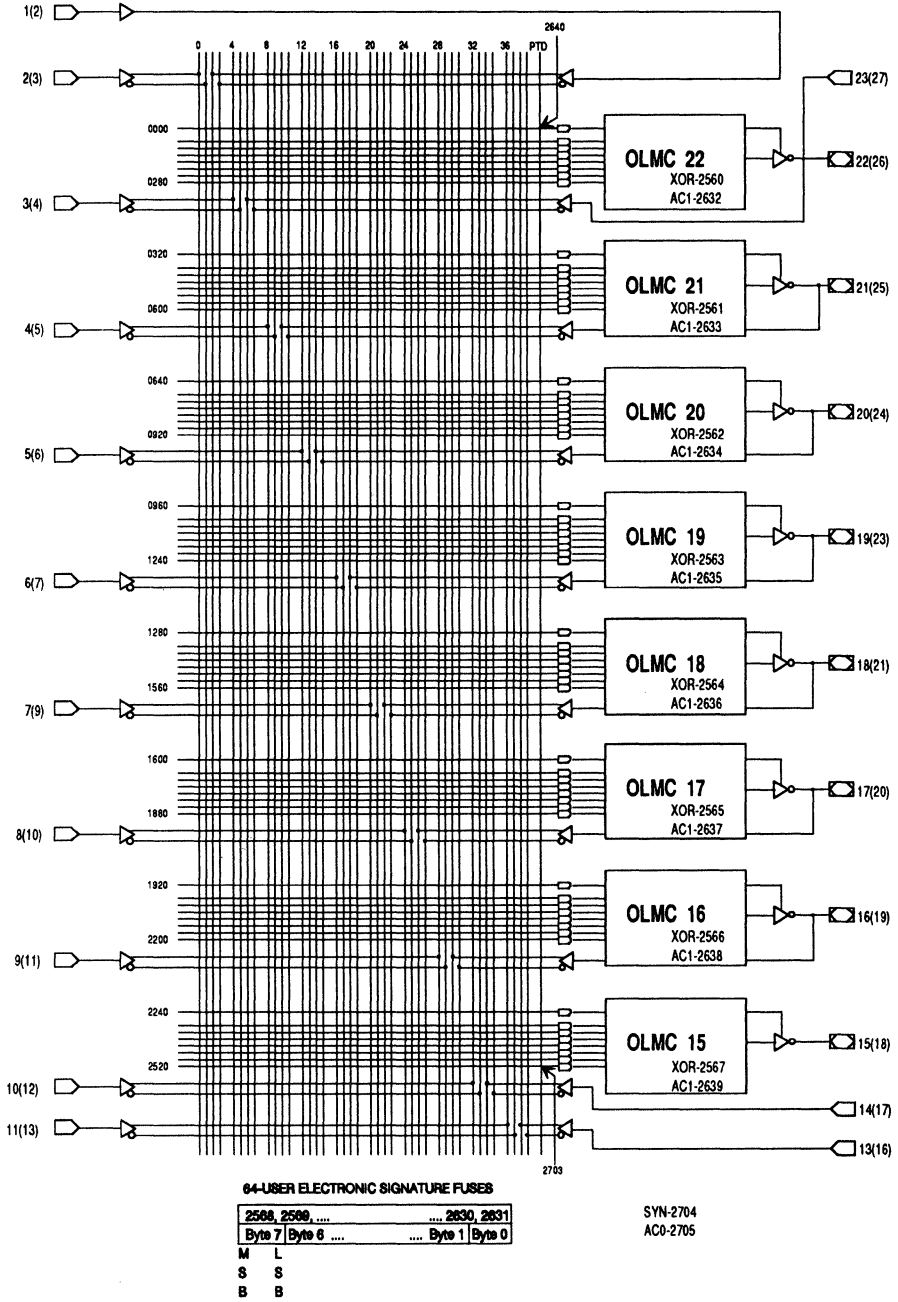
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 15 and Pin 22 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 | Byte 6	.... Byte 1 | Byte 0

M S B — L S B

SYN-2704
AC0-2705

SIMPLE MODE

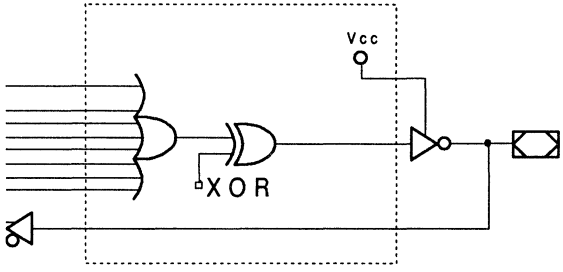
In the Simple mode, pins are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

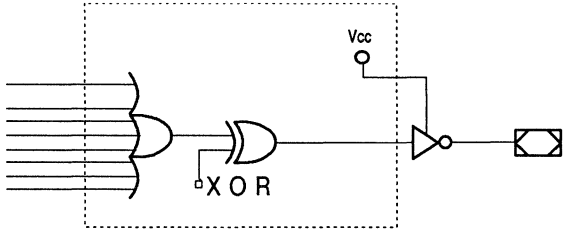
Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 18 & 19) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



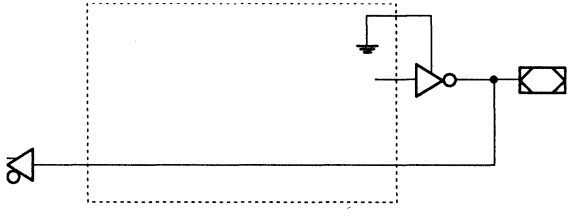
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 18 & 19 are permanently configured to this function.



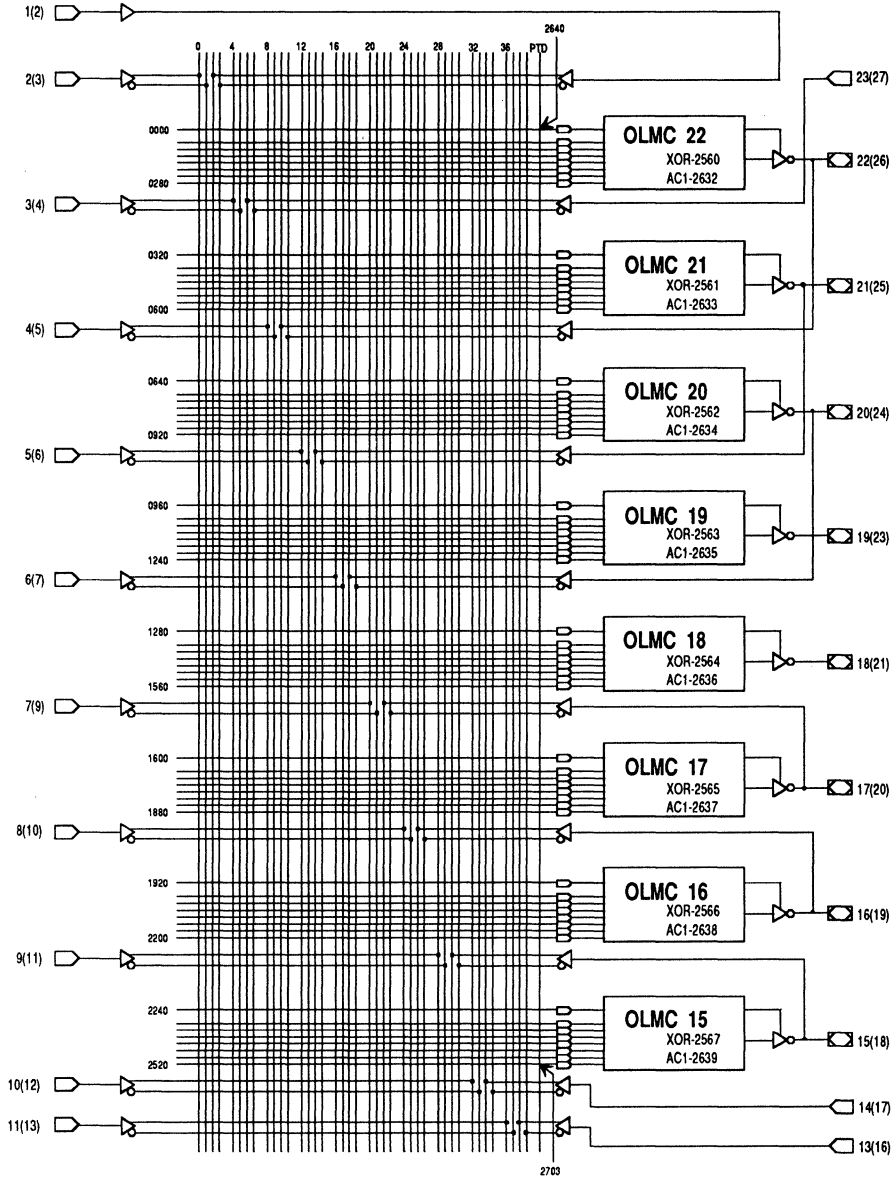
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 Byte 6	.... Byte 1 Byte 0

M S B — L S B

SYN-2704
AC0-2705

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Ambient Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) .....0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz Outputs Open (no load)	—	75	115	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION		-7		-10		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	8 outputs switching	3	7.5	3	10	ns
			1 output switching	—	7	—	—	ns
t_{co}	1	Clock to Output Delay		2	5	2	7	ns
t_{cf}[2]	—	Clock to Feedback Delay		—	3	—	6	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑		7	—	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑		0	—	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		83.3	—	58.8	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		100	—	62.5	—	MHz
	1	Maximum Clock Frequency with No Feedback		100	—	62.5	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High		5	—	8	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low		5	—	8	—	ns
t_{en}	2	Input or I/O to Output		3	9	3	10	ns
	2	OE↓ to Output		2	6	2	10	ns
t_{dis}	3	Input or I/O to Output		2	9	2	10	ns
	3	OE↑ to Output		1.5	6	1.5	10	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

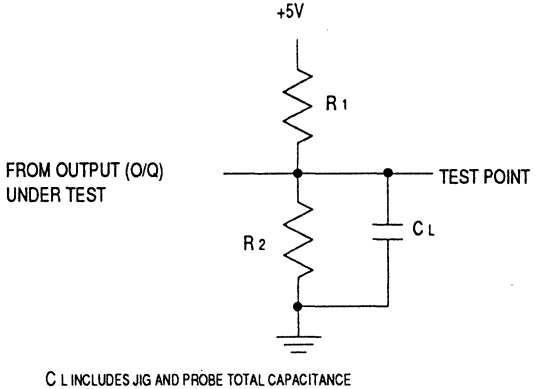
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Ambient Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) .....0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION			MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage				Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage				2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)			—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$			—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}			—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}			2.4	—	—	V
I_{OL}	Low Level Output Current				—	—	24	mA
I_{OH}	High Level Output Current				—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C			–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V Outputs Open (no load)	f_{toggle} = 15MHz	L -25	—	75	90	mA
			f_{toggle} = 25MHz	L -10/-15	—	75	115	mA
			f_{toggle} = 15MHz	Q -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-10		-15		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	10	3	15	3	25	ns
tco	1	Clock to Output Delay	2	7	2	10	2	12	ns
tcf[2]		Clock to Feedback Delay	—	7	—	8	—	10	ns
tsu		Setup Time, Input or Feedback before Clock↑	10	—	12	—	15	—	ns
th		Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	58.8	—	45.5	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	50	—	40	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	41.7	—	MHz
twh[4]		Clock Pulse Duration, High	8	—	8	—	12	—	ns
twl[4]		Clock Pulse Duration, Low	8	—	8	—	12	—	ns
ten	2	Input or I/O to Output Enabled	—	10	—	15	—	25	ns
	2	OE↓ to Output Enabled	—	10	—	15	—	20	ns
tdis	3	Input or I/O to Output Disabled	—	10	—	15	—	25	ns
	3	OE↑ to Output Disabled	—	10	—	15	—	20	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

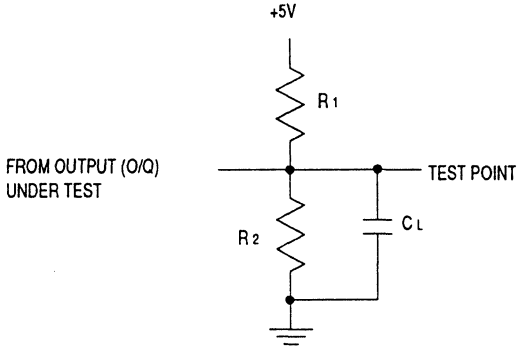
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Ambient Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
Ambient Temperature (T_A) .....–40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION			MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage				Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage				2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)			—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$			—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}			—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}			2.4	—	—	V
I_{OL}	Low Level Output Curren:				—	—	24	mA
I_{OH}	High Level Output Current				—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V	V_{OUT} = 0.5V	T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V Outputs Open (no load)	f_{toggle} = 25MHz	L -15/-25	—	75	130	mA
			f_{toggle} = 15MHz	Q -20/-25	—	45	65	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-15		-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	15	3	20	3	25	ns
tco	1	Clock to Output Delay	2	10	2	11	2	12	ns
tcf[2]		Clock to Feedback Delay	—	8	—	9	—	10	ns
tsu		Setup Time, Input or Feedback before Clock↑	12	—	13	—	15	—	ns
th		Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	45.5	—	41.6	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	45.4	—	40	—	MHz
	1	Maximum Clock Frequency with External Feedback	62.5	—	50	—	41.6	—	MHz
twh[4]		Clock Pulse Duration, High	8	—	10	—	12	—	ns
twl[4]		Clock Pulse Duration, Low	8	—	10	—	12	—	ns
ten	2	Input or I/O to Output	—	15	—	20	—	25	ns
	2	OE↓ to Output	—	15	—	18	—	20	ns
tdis	3	Input or I/O to Output	—	15	—	20	—	25	ns
	3	OE↑ to Output	—	15	—	18	—	20	ns

) Refer to **Switching Test Conditions** section.
) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
) Refer to **fmax Descriptions** section.
) Clock pulses of widths less than the specification may be detected as valid clock signals.

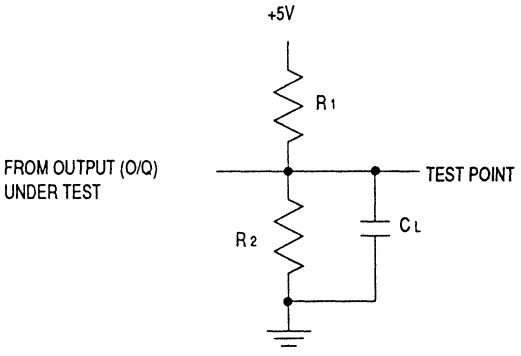
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

-state levels are measured 0.5V from steady-state active evel.

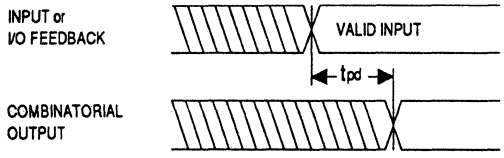
Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

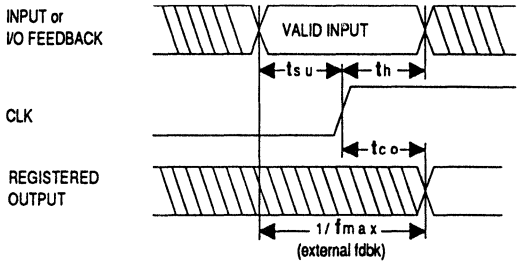


C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

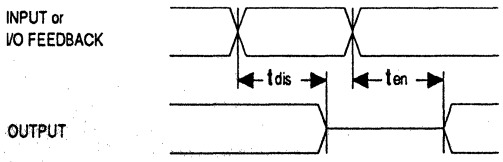
SWITCHING WAVEFORMS



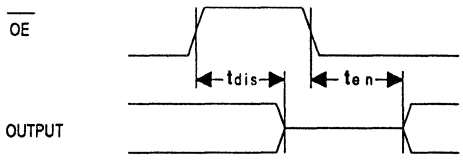
Combinatorial Output



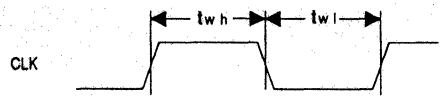
Registered Output



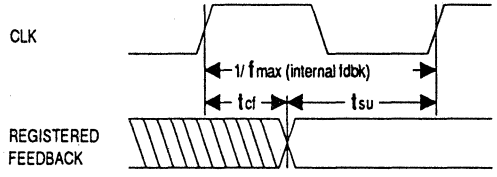
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

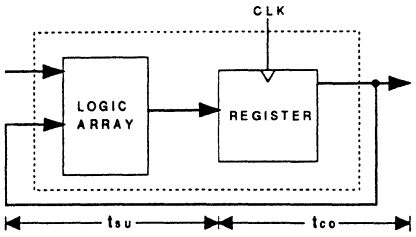


Clock Width



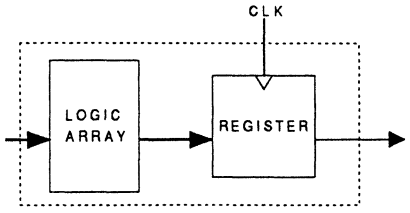
fmax with Feedback

fmax DESCRIPTIONS



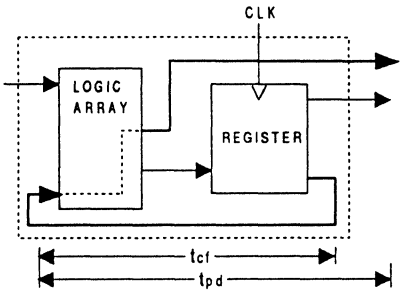
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax Without Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL20V8A/B device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter checksum.

SECURITY CELL

The security cell is provided on all GAL20V8A/B devices to prevent unauthorized copying of the array patterns. Once programmed, the circuitry enabling array is disabled, preventing further programming or verification of the array. The cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

LATCH-UP PROTECTION

GAL20V8A/B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

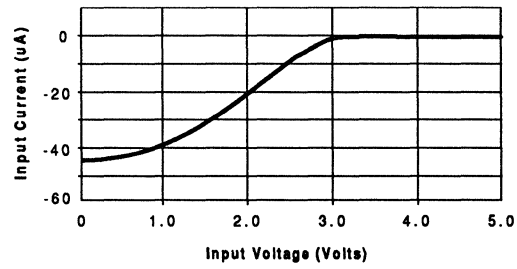
GAL20V8A/B devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

INPUT BUFFERS

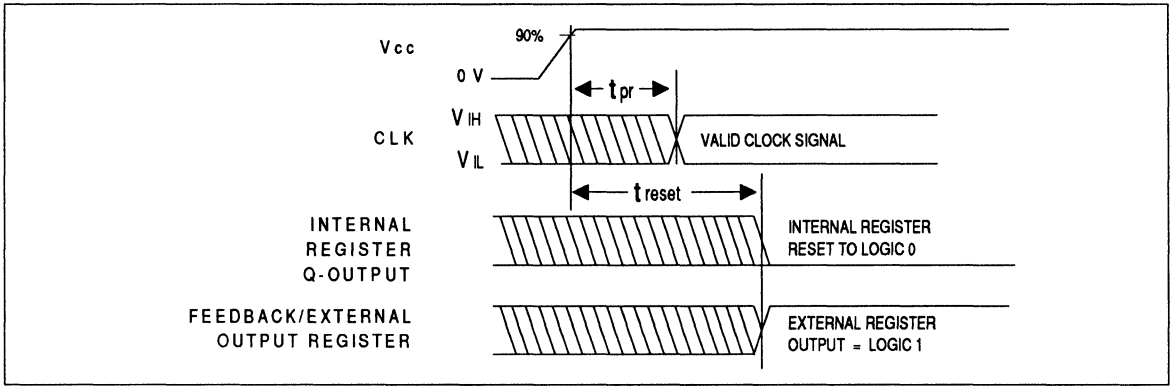
GAL20V8A and GAL20V8B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL20V8B input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). In contrast, the GAL20V8A does not have active pull-ups within their input structures. Lattice recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic



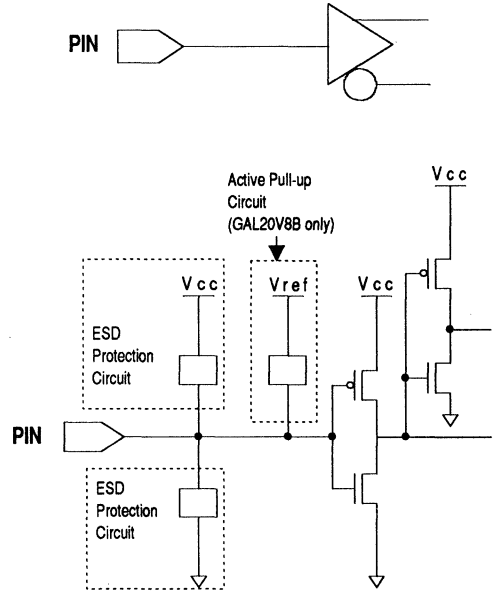
POWER-UP RESET



Circuitry within the GAL20V8A and GAL20V8B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

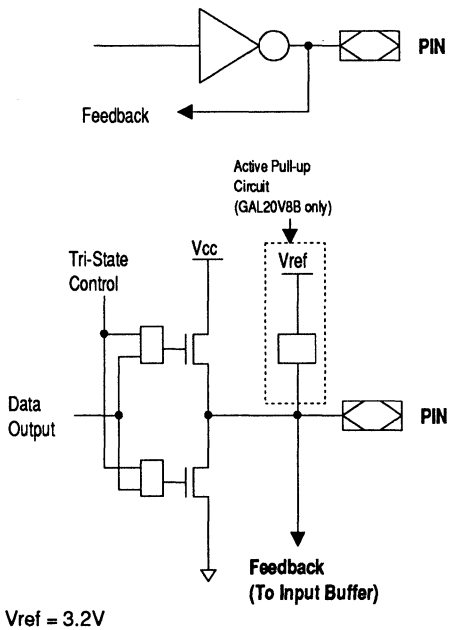
The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20V8A and GAL20V8B. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. Vref = 3.2V

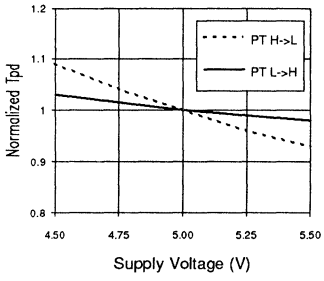
Typical Input



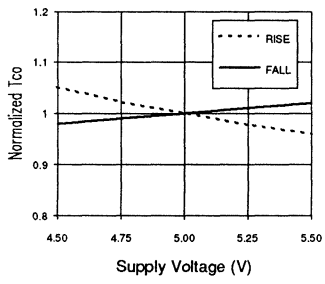
Typ. Vref = 3.2V

Typical Output

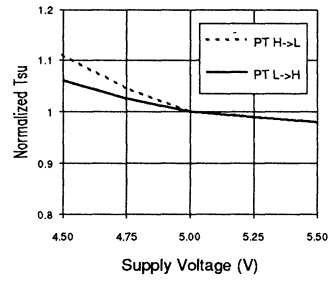
Normalized Tpd vs Vcc



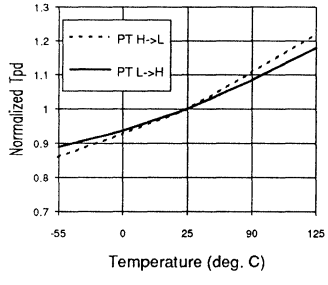
Normalized Tco vs Vcc



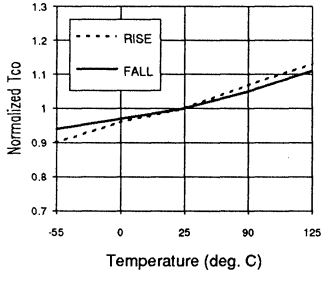
Normalized Tsu vs Vcc



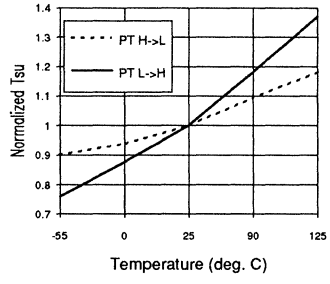
Normalized Tpd vs Temp



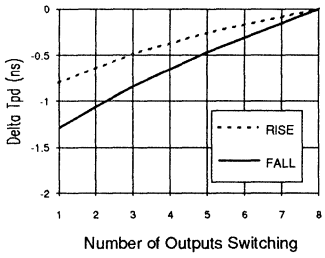
Normalized Tco vs Temp



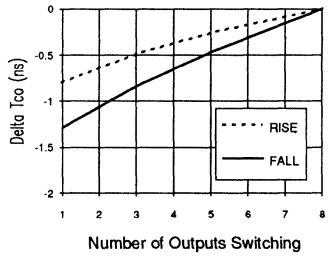
Normalized Tsu vs Temp



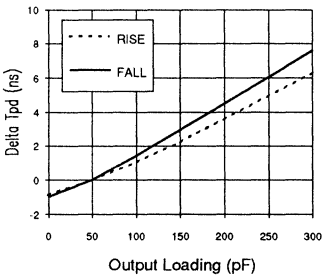
Delta Tpd vs # of Outputs Switching



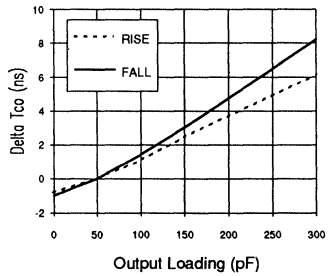
Delta Tco vs # of Outputs Switching



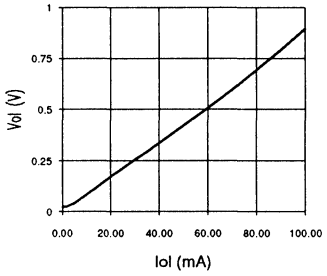
Delta Tpd vs Output Loading



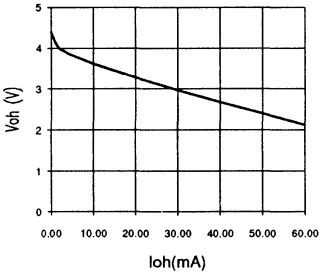
Delta Tco vs Output Loading



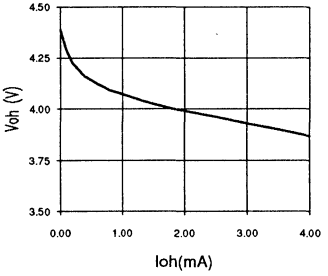
Vol vs Iol



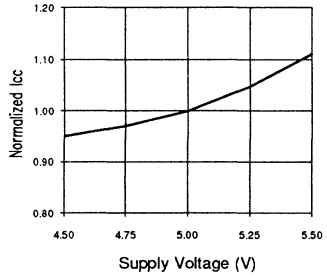
Voh vs Ioh



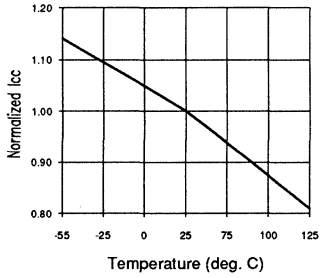
Voh vs Ioh



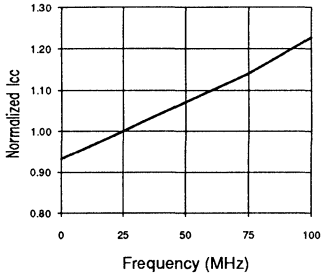
Normalized Icc vs Vcc



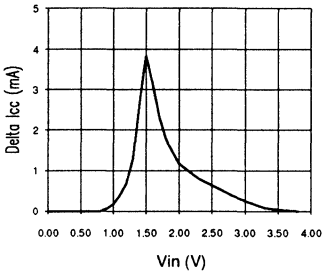
Normalized Icc vs Temp



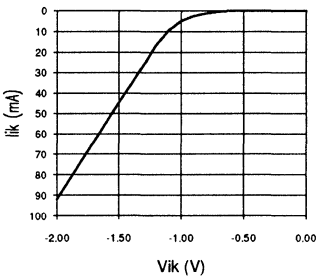
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

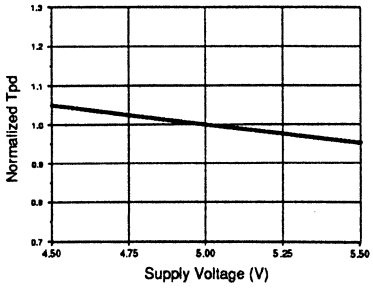


Input Clamp (Vik)

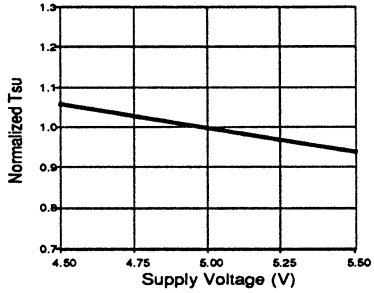


Typical Characteristics

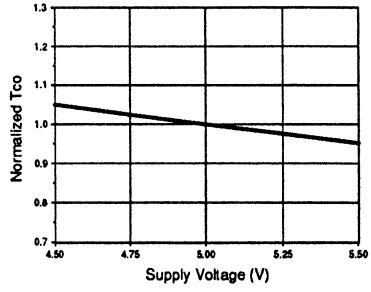
Normalized Tpd vs. Vcc



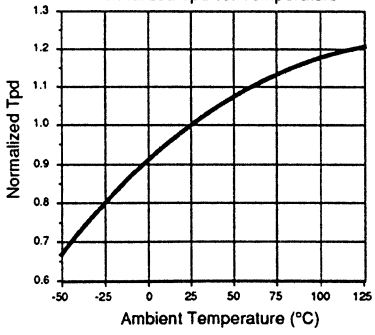
Normalized Tsu vs. Vcc



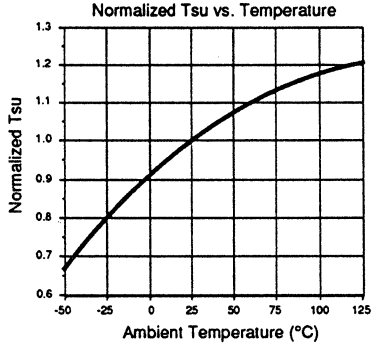
Normalized Tco vs. Vcc



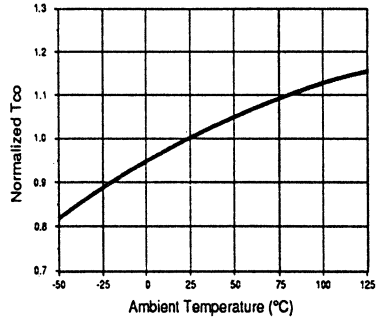
Normalized Tpd vs. Temperature



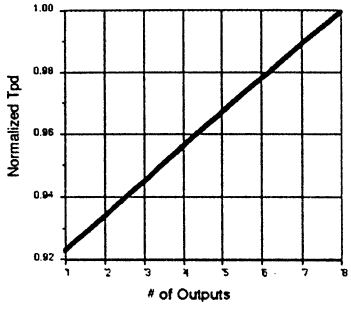
Normalized Tsu vs. Temperature



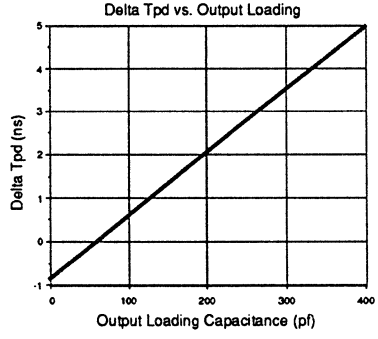
Normalized Tco vs. Temperature



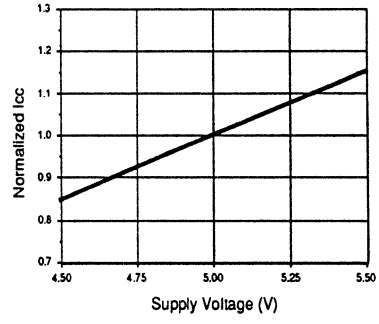
Normalized Tpd vs. # of Outputs Switching



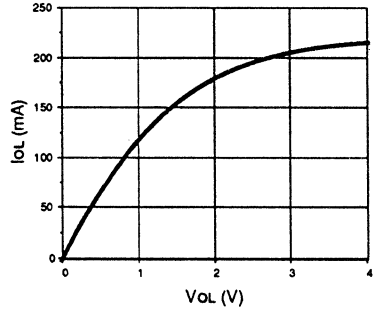
Delta Tpd vs. Output Loading



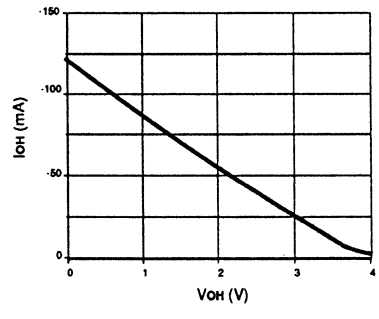
Normalized Icc vs. Vcc



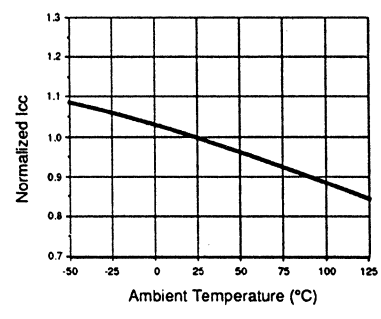
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



Normalized Icc vs. Temperature



GAL18V10

High Performance E²CMOS PLD
Generic Array Logic™

2

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 10ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **LOW POWER CMOS**
  - **— 75 mA Typical Icc**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (50ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Uses Standard 22V10 Macrocells**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

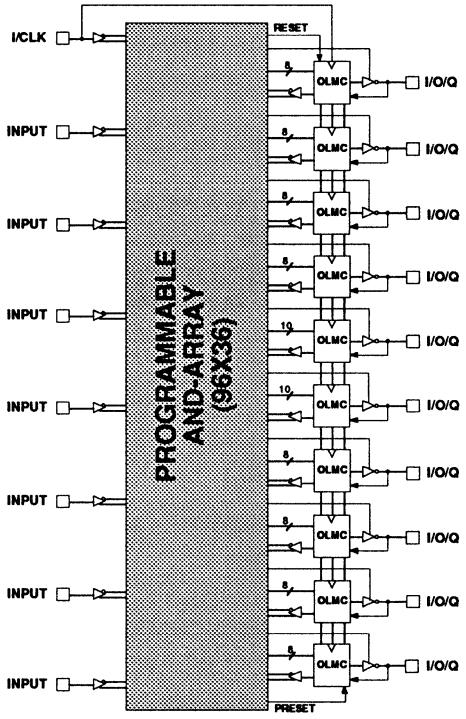
DESCRIPTION

The GAL18V10, at 15 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance 20 pin PLD available on the market. CMOS circuitry allows the GAL18V10 to consume much less power when compared to its bipolar counterparts. The E² technology offers high speed (50ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

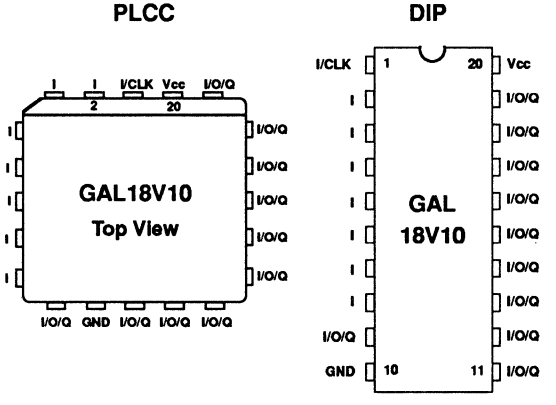
By building on the popular 22V10 architecture, the GAL18V10 allows the designer to be immediately productive, eliminating the learning curve. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL18V10 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIAGRAMS



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124 U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

April 1991.Rev.A

GAL18V10 ORDERING INFORMATION

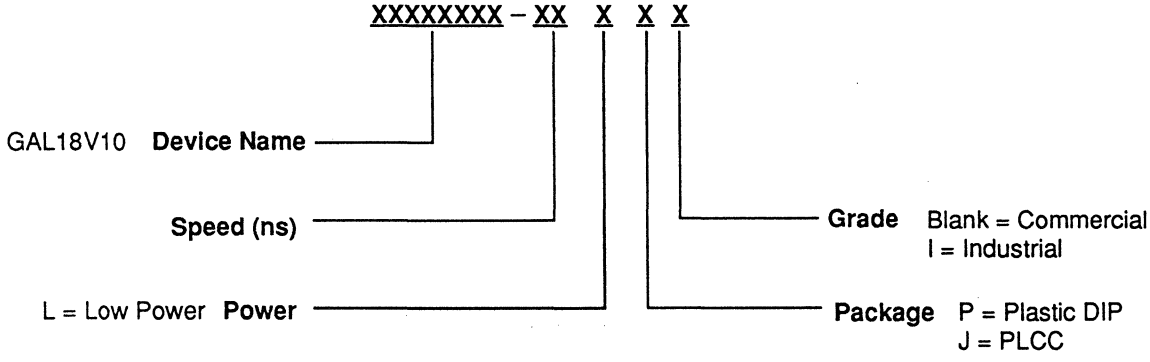
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	10	115	GAL18V10-15LP	20-Pin Plastic DIP
			115	GAL18V10-15LJ	20-Lead PLCC
20	12	12	115	GAL18V10-20LP	20-Pin Plastic DIP
			115	GAL18V10-20LJ	20-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	12	12	125	GAL18V10-20LPI	20-Pin Plastic DIP
			125	GAL18V10-20LJI	20-Lead PLCC

PART NUMBER DESCRIPTION



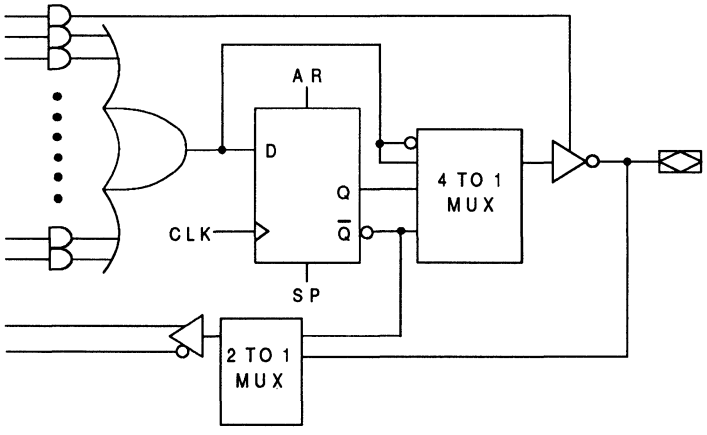
OUTPUT LOGIC MACROCELL (OLMC)

The GAL18V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to ten product terms (pins 14 and 15), and the other eight OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configgured as either active high or active low.

The GAL18V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL18V10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL18V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the the following page.

REGISTERED

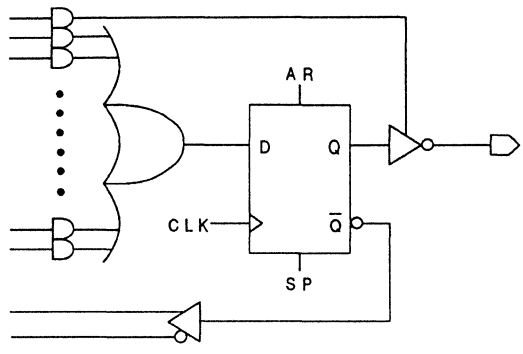
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

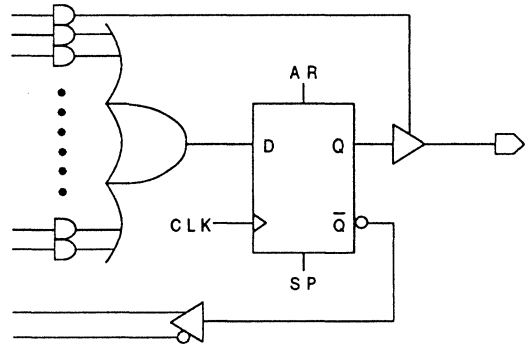
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

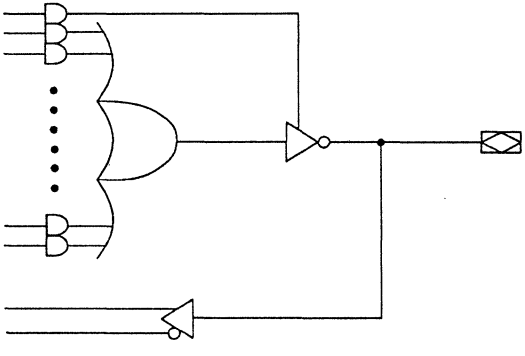
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

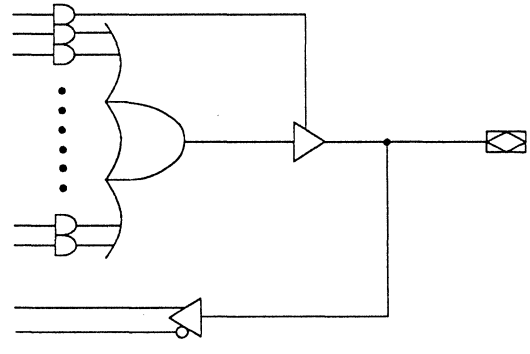
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

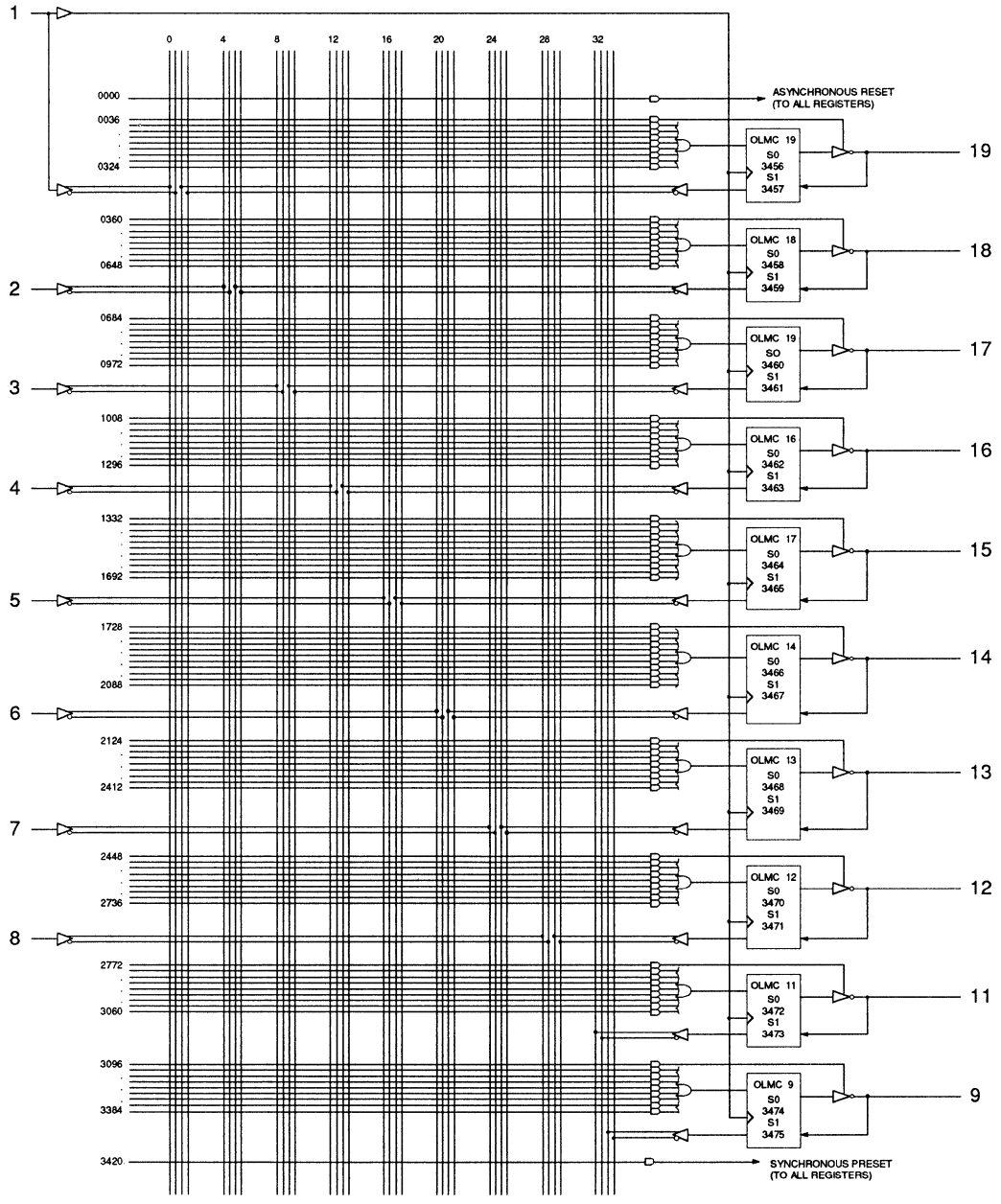
$S_0 = 0$
$S_1 = 1$



ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL18V10 LOGIC DIAGRAM / JEDEC FUSE MAP



3476, 3477 ...	Electronic Signature						... 3538, 3539
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15Mhz Outputs Open	—	75	115	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	15	—	20	ns
tco	1	Clock to Output Delay	—	10	—	12	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu +tco)	50	—	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	8	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	8	—	ns
ten	2	Input or I/O to Output Enabled	—	15	—	20	ns
tdis	3	Input or I/O to Output Disabled	—	15	—	20	ns
tar	1	Input or I/O to Asynchronous Reset of Register	—	20	—	20	ns
tarw	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
tarr	—	Asynchronous Reset to Clock↑ Recovery Time	15	—	15	—	ns
tspr	—	Synchronous Preset to Clock↑ Recovery Time	10	—	12	—	ns

) Refer to **Switching Test Conditions** section.
) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
) Refer to **fmax Description** section.
) Clock pulses of widths less than the specification may be detected as valid clock signals.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V ftoggle = 15Mhz Outputs Open	—	90	125	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

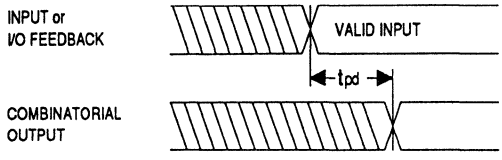
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

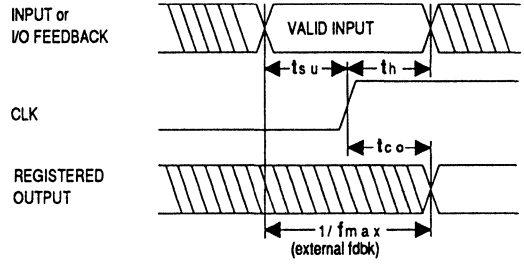
PARAMETER	TEST COND.[1]	DESCRIPTION	-20		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	20	ns
t_{co}	1	Clock to Output Delay	—	12	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	12	—	ns
t_{h}	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	8	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	25	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock↑ Recovery Time	15	—	ns
t_{spr}	—	Synchronous Preset to Clock↑ Recovery Time	12	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

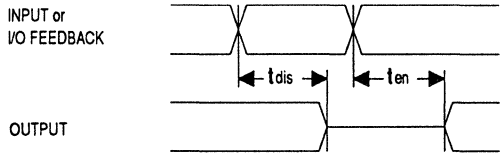
SWITCHING WAVEFORMS



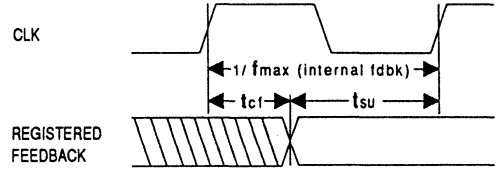
Combinatorial Output



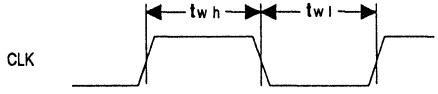
Registered Output



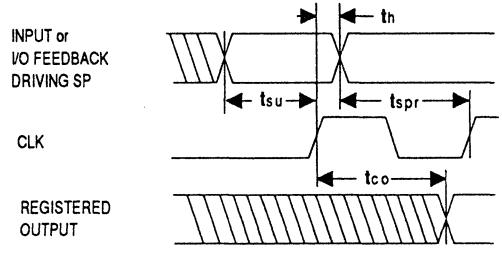
Input or I/O to Output Enable/Disable



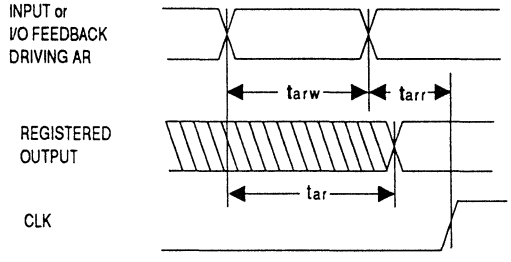
fmax with Feedback



Clock Width

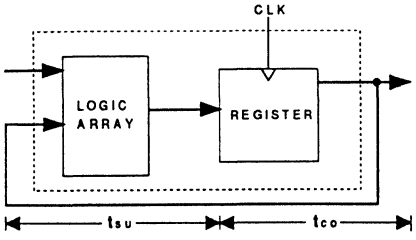


Synchronous Preset



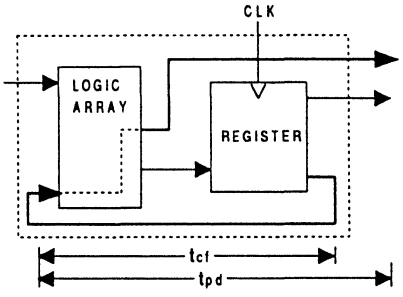
Asynchronous Reset

fmax DESCRIPTIONS



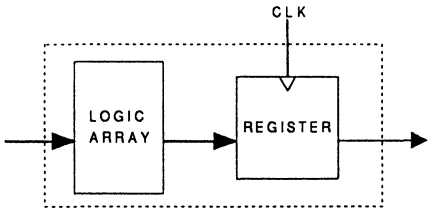
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.



fmax With No Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.

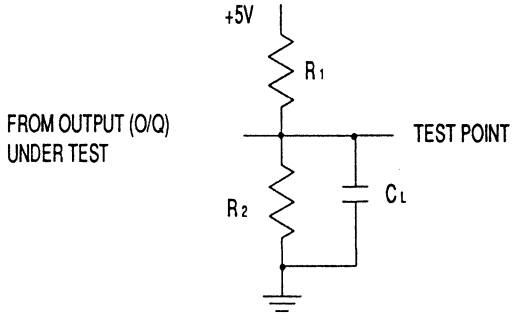
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		300Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL18V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided in every GAL18V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL18V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

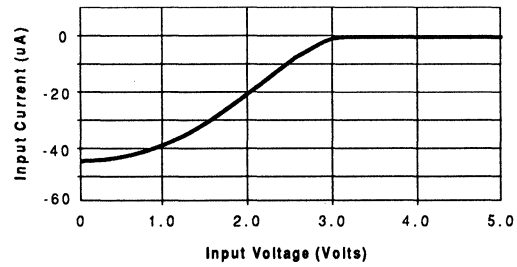
The GAL18V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

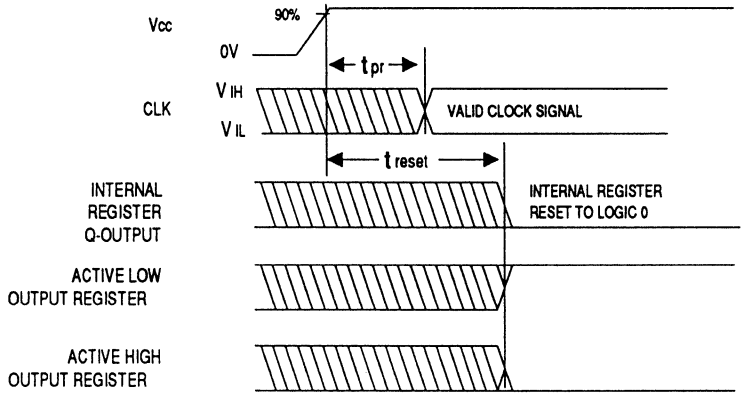
GAL18V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device.

Typical Input Current



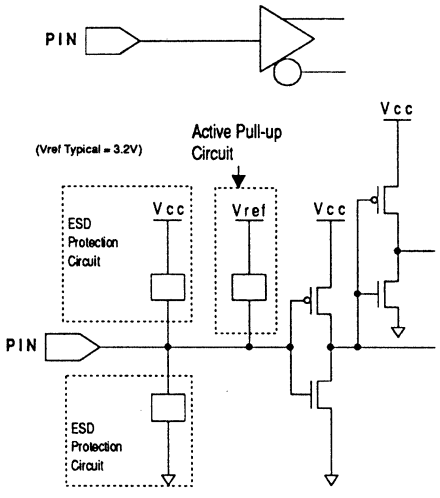
POWER-UP RESET



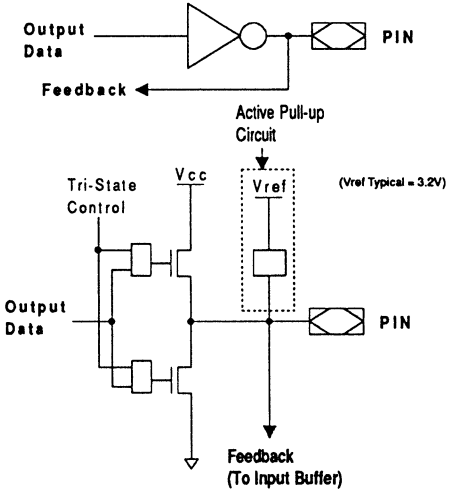
Circuitry within the GAL18V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL18V10. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



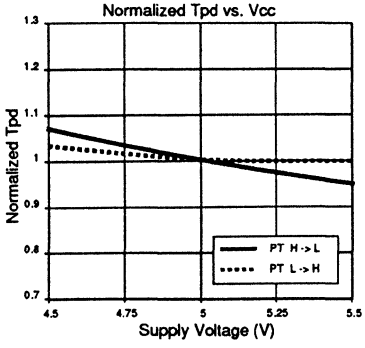
Input



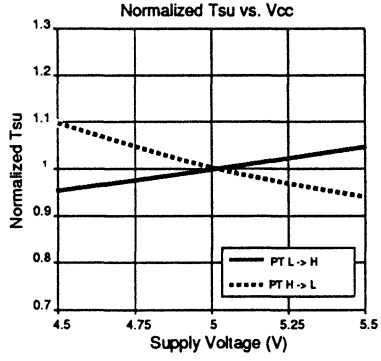
Output

Typical Characteristics

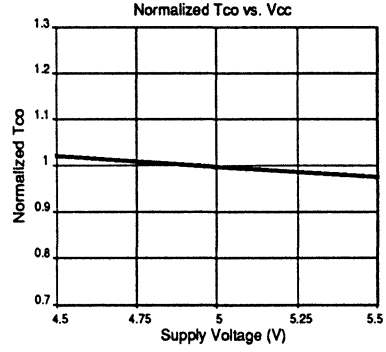
Normalized Tpd vs. Vcc



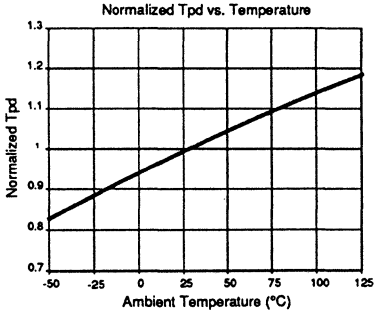
Normalized Tsu vs. Vcc



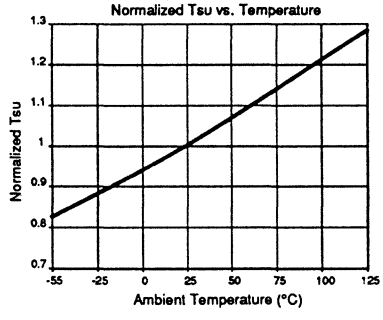
Normalized Tco vs. Vcc



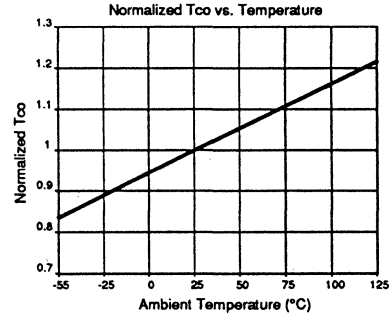
Normalized Tpd vs. Temperature



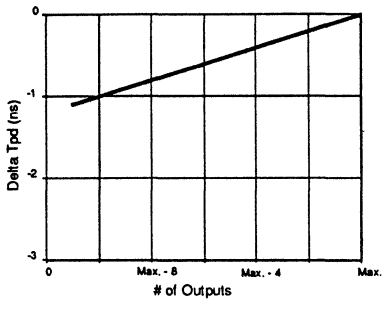
Normalized Tsu vs. Temperature



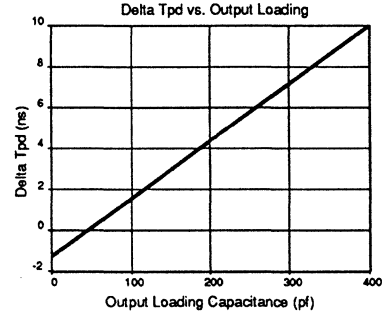
Normalized Tco vs. Temperature



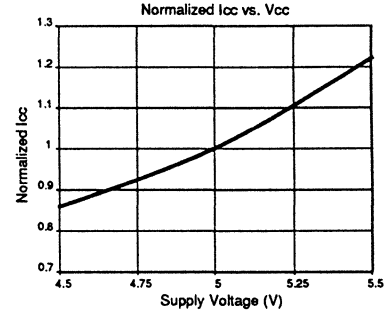
Delta Tpd vs. # of Outputs Switching



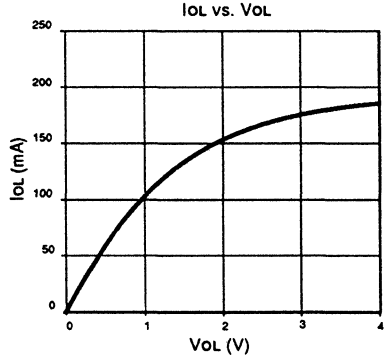
Delta Tpd vs. Output Loading



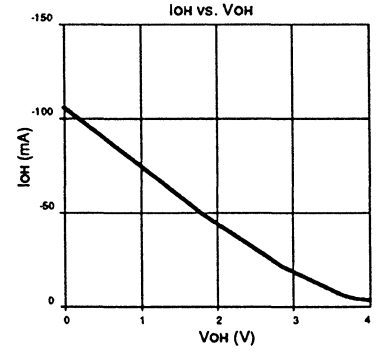
Normalized Icc vs. Vcc



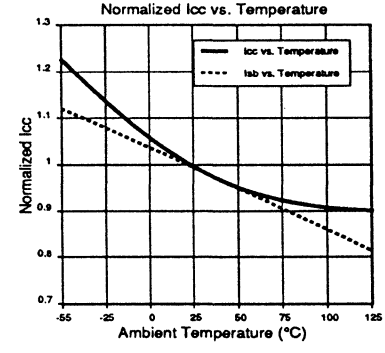
IOL vs. VOL



IOH vs. VOH



Normalized Icc vs. Temperature



GAL22V10B
GAL22V10

High Performance E²CMOS PLD

2

FEATURES

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 10 ns Maximum Propagation Delay
  - Fmax = 105 MHz
  - 7 ns Maximum from Clock Input to Data Output
  - TTL Compatible 16 mA Outputs
  - UltraMOS® Advanced CMOS Technology
- ACTIVE PULL-UPS ON ALL PINS
- COMPATIBLE WITH STANDARD 22V10 DEVICES
  - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices
- 50% REDUCTION IN POWER VERSUS BIPOLAR
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- TEN OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
- PRELOAD AND POWER-ON RESET OF REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

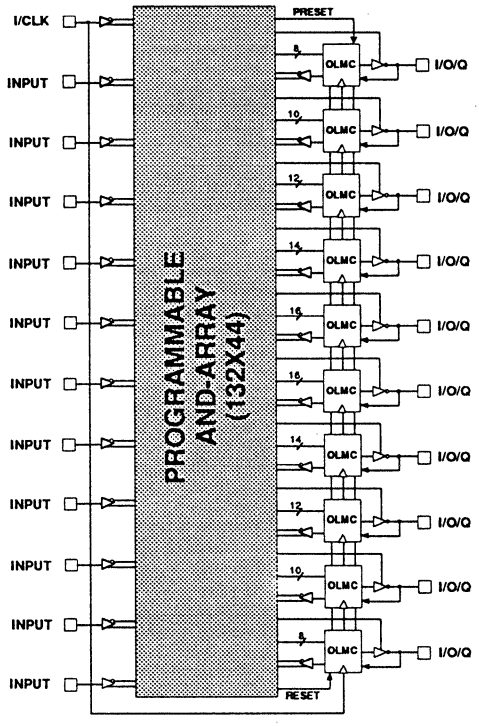
DESCRIPTION

The GAL22V10B, at 10ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

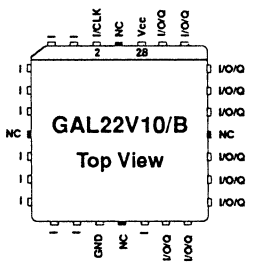
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM

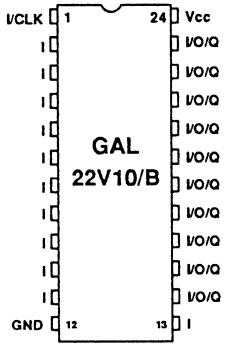


PACKAGE DIAGRAMS

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124 U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

April 1991.Rev.A

GAL22V10/B ORDERING INFORMATION

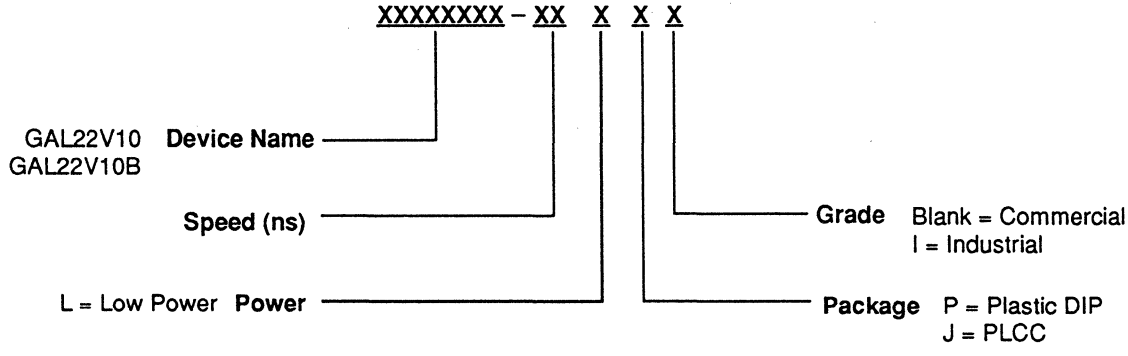
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	7	7	130	GAL22V10B-10LP	24-Pin Plastic DIP
			130	GAL22V10B-10LJ	28-Lead PLCC
15	10	8	130	GAL22V10B-15LP	24-Pin Plastic DIP
			130	GAL22V10B-15LJ	28-Lead PLCC
15	12	8	130	GAL22V10-15LP	24-Pin Plastic DIP
			130	GAL22V10-15LJ	28-Lead PLCC
25	15	15	130	GAL22V10-25LP	24-Pin Plastic DIP
			130	GAL22V10-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	8	150	GAL22V10B-15LPI	24-Pin Plastic DIP
			150	GAL22V10B-15LJI	28-Lead PLCC
20	14	10	150	GAL22V10-20LPI	24-Pin Plastic DIP
			150	GAL22V10-20LJI	28-Lead PLCC
25	15	15	150	GAL22V10-25LPI	24-Pin Plastic DIP
			150	GAL22V10-25LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



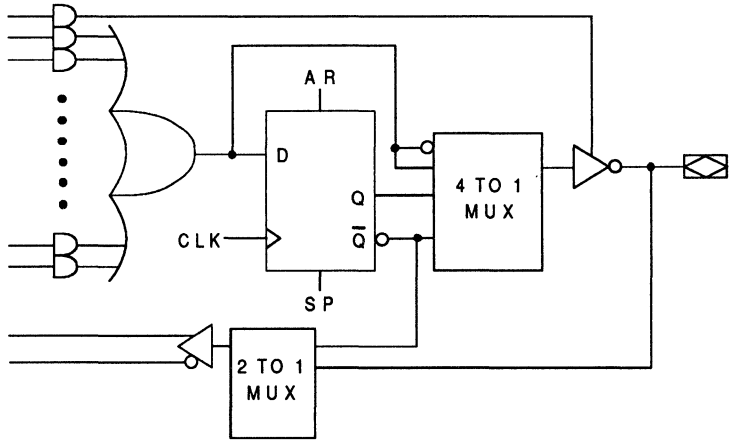
OUTPUT LOGIC MACROCELL (OLMC)

The GAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL22V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

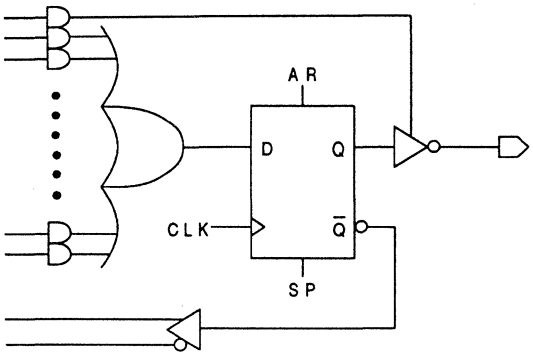
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

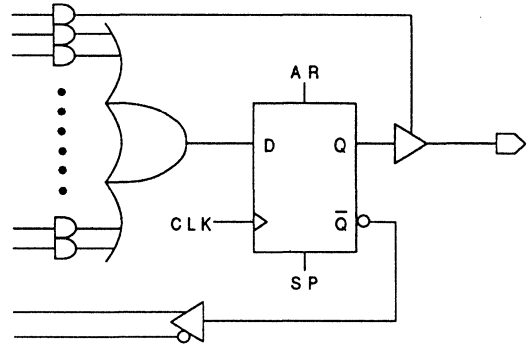
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

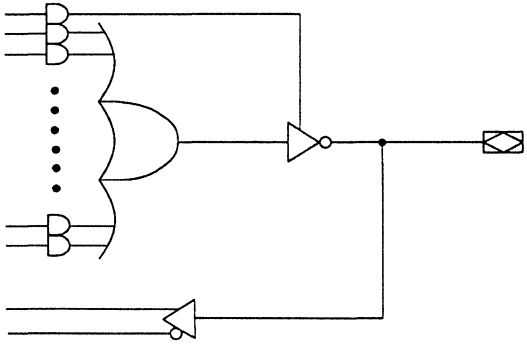
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

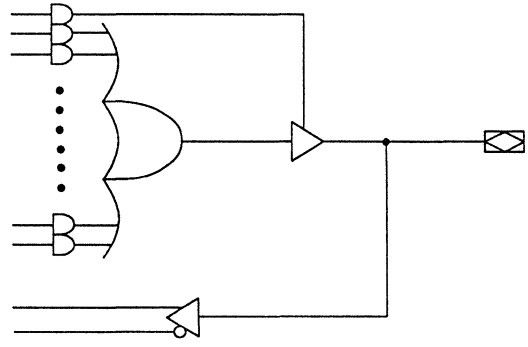
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$



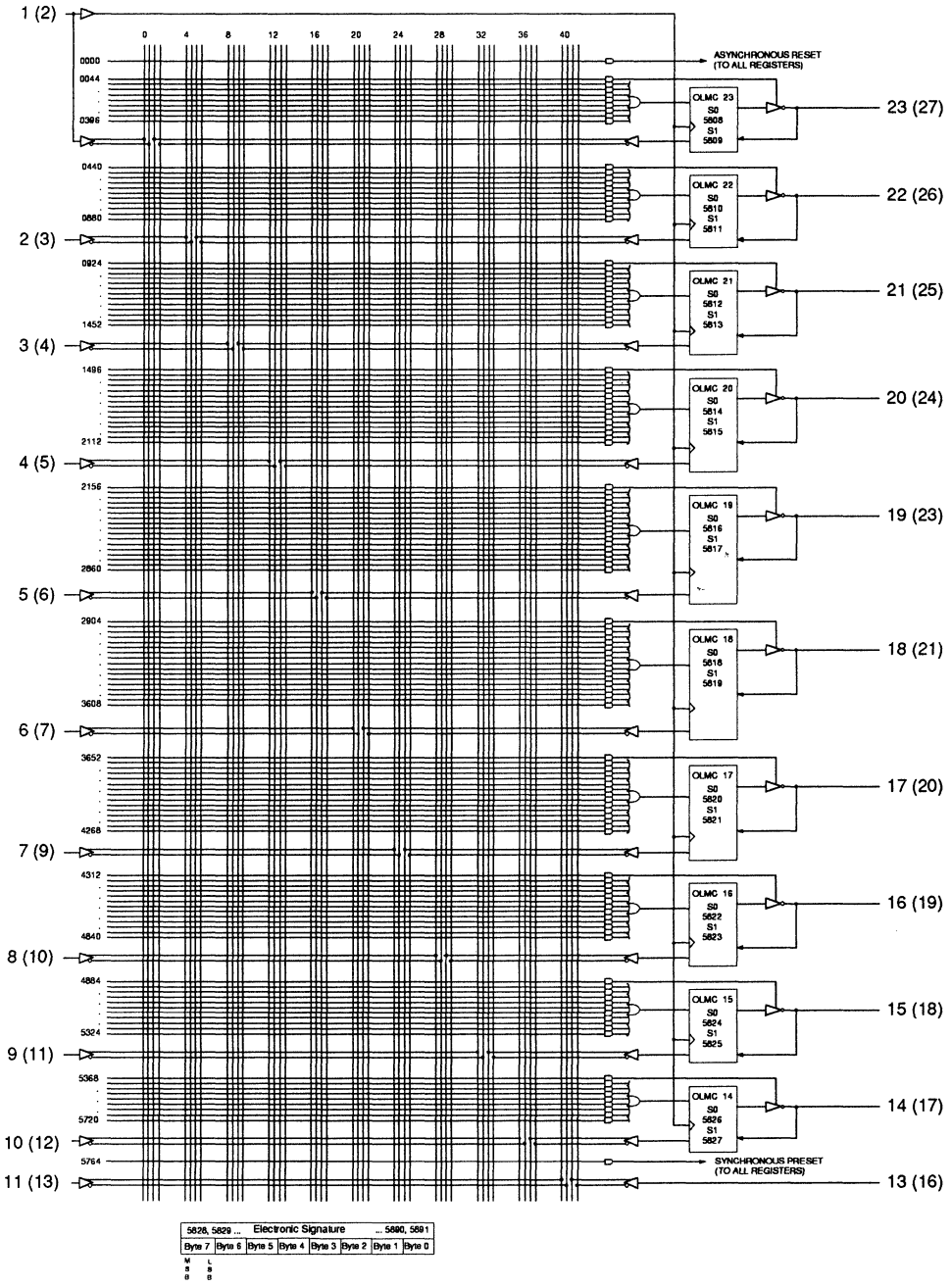
ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL22V10 LOGIC DIAGRAM / JEDEC FUSE MAP

2

DIP (PLCC) Package Pinouts



ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V

Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 25Mhz Outputs Open	—	90	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-10		-15		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	10	3	15	ns
t_{co}	1	Clock to Output Delay	2	7	2	8	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	2.5	—	2.5	ns
t_{su_1}	—	Setup Time, Input or Feedback before Clock↑	7	—	10	—	ns
t_{su_2}	—	Setup Time, SP before Clock↑	10	—	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	71.4	—	55.5	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	105	—	80	—	MHz
	1	Maximum Clock Frequency with No Feedback	105	—	83.3	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	4	—	6	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	4	—	6	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	10	3	15	ns
t_{dis}	3	Input or I/O to Output Disabled	3	9	3	15	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	3	13	3	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	8	—	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock↑ Recovery Time	8	—	10	—	ns
t_{spr}	—	Synchronous Preset to Clock↑ Recovery Time	10	—	10	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–150	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	90	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-15		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	15	3	25	ns
t_{co}	1	Clock to Output Delay	2	8	2	15	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	5	—	13	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	12	—	15	—	ns
t_{h}	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	33.3	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	35.7	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	38.5	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	8	—	13	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	8	—	13	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	15	3	25	ns
t_{dis}	3	Input or I/O to Output Disabled	3	15	3	25	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	3	20	3	25	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	25	—	ns
t_{arr}	—	Asynchronous Reset to Clock↑ Recovery Time	15	—	25	—	ns
t_{spr}	—	Synchronous Preset to Clock↑ Recovery Time	12	—	15	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	-30	—	-130	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 25Mhz Outputs Open	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-15		UNITS
			MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	3	15	ns
t_{co}	1	Clock to Output Delay	2	8	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	5	ns
t_{su_1}	—	Setup Time, Input or Feedback before Clock↑	10	—	ns
t_{su_2}	—	Setup Time, SP before Clock↑	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55.5	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	66.6	—	MHz
	1	Maximum Clock Frequency with No Feedback	66.6	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	6	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	6	—	ns
t_{en}	2	Input or I/O to Output Enabled	3	15	ns
t_{dis}	3	Input or I/O to Output Disabled	3	15	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	3	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock↑ Recovery Time	10	—	ns
t_{spr}	—	Synchronous Preset to Clock↑ Recovery Time	12	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-150	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

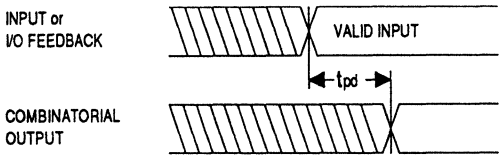
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

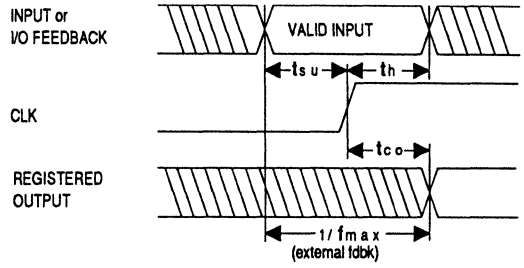
PARAMETER	TEST COND.[1]	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	20	—	25	ns
t_{co}	1	Clock to Output Delay	—	10	—	15	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	8	—	13	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	14	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	41.6	—	33.3	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	45.4	—	35.7	—	MHz
	1	Maximum Clock Frequency with No Feedback	50	—	38.5	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	10	—	13	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	10	—	13	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	—	25	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	—	25	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	25	—	25	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	20	—	25	—	ns
t_{arr}	—	Asynchronous Reset to Clock↑ Recovery Time	20	—	25	—	ns
t_{spr}	—	Synchronous Preset to Clock↑ Recovery Time	14	—	15	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

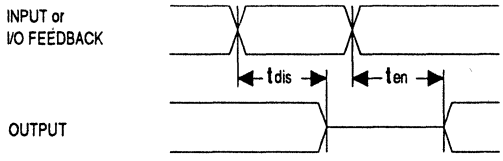
SWITCHING WAVEFORMS



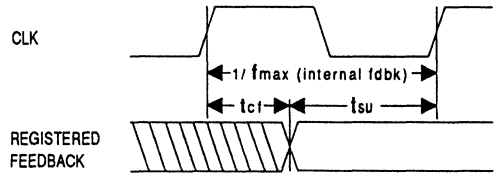
Combinatorial Output



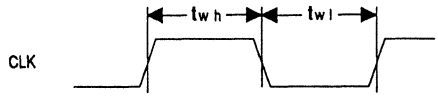
Registered Output



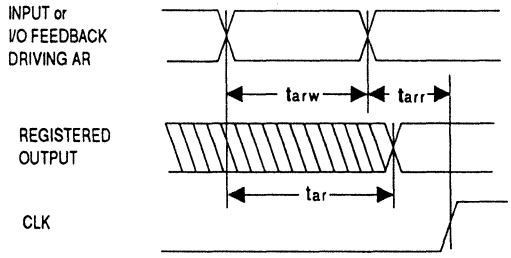
Input or I/O to Output Enable/Disable



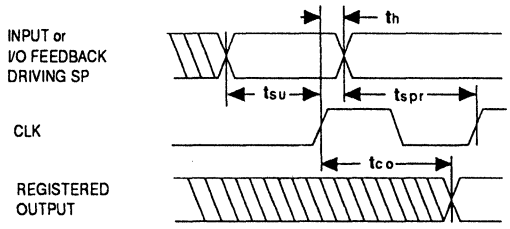
fmax with Feedback



Clock Width

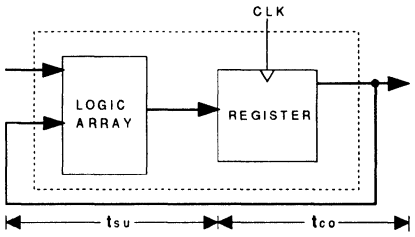


Asynchronous Reset



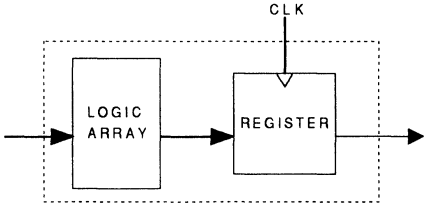
Synchronous Preset

fmax DESCRIPTIONS



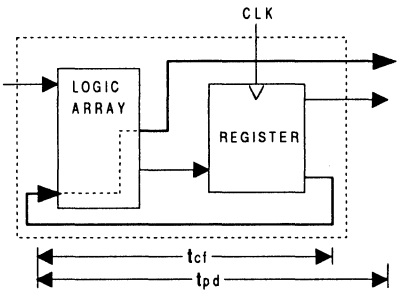
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax With No Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/ internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

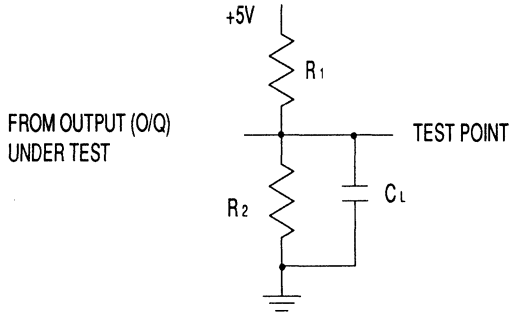
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		300Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL22V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22V10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22V10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL22V10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every GAL22V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL22V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

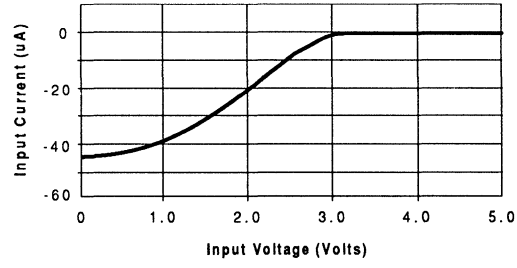
The GAL22V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

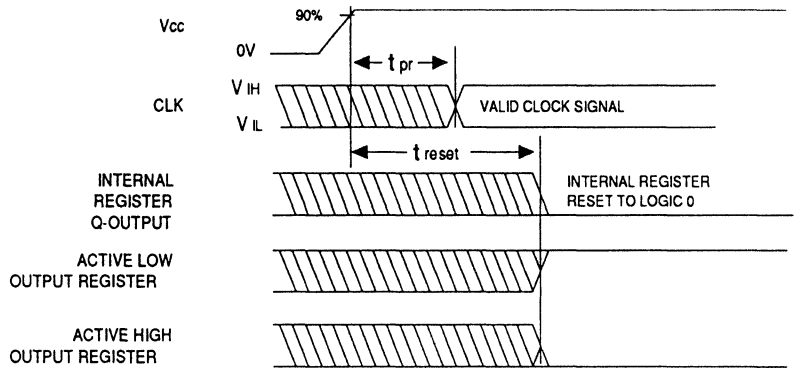
GAL22V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Current



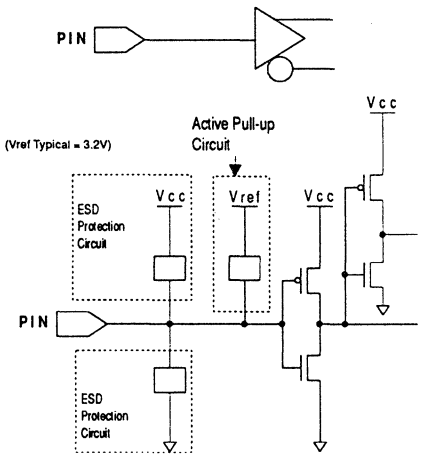
POWER-UP RESET



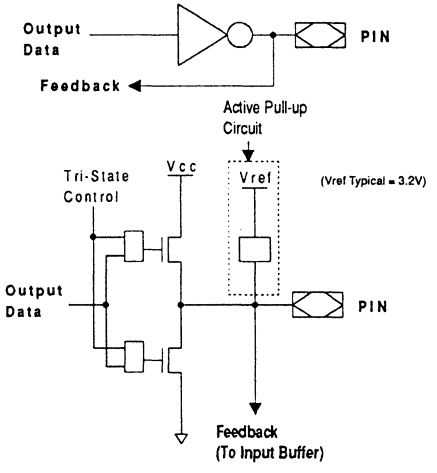
Circuitry within the GAL22V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL22V10. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



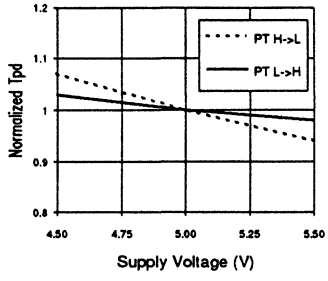
Input



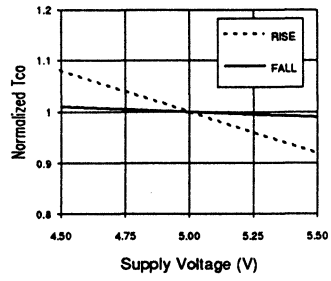
Output

Typical Characteristics

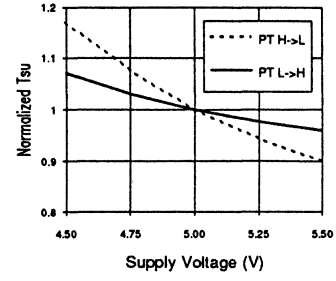
Normalized Tpd vs Vcc



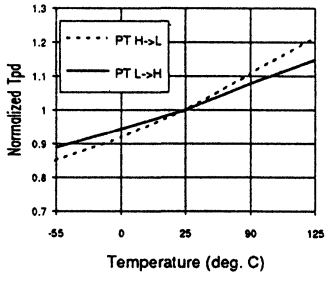
Normalized Tco vs Vcc



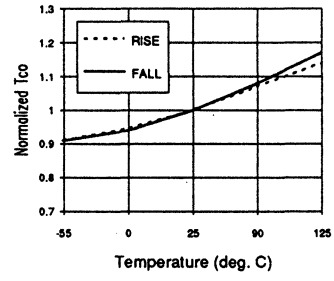
Normalized Tsu vs Vcc



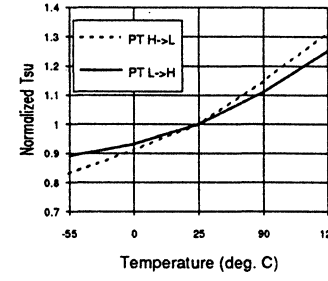
Normalized Tpd vs Temp



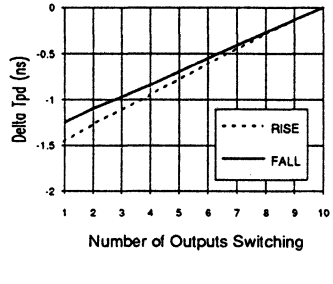
Normalized Tco vs Temp



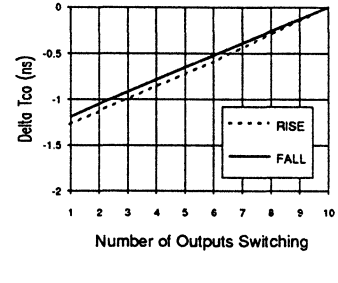
Normalized Tsu vs Temp



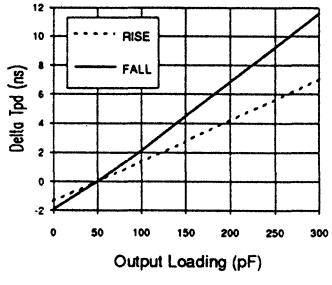
Delta Tpd vs # of Outputs Switching



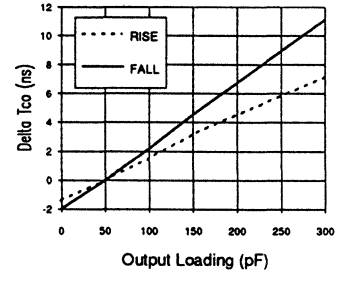
Delta Tco vs # of Outputs Switching



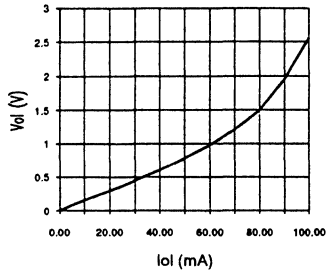
Delta Tpd vs Output Loading



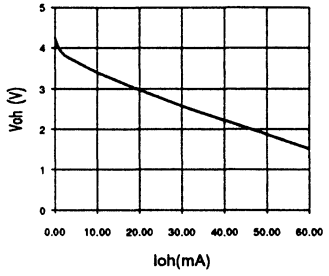
Delta Tco vs Output Loading



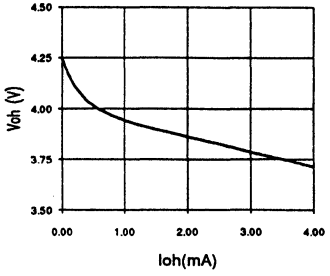
Vol vs Iol



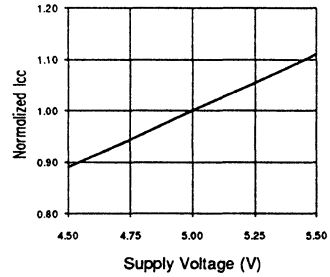
Voh vs Ioh



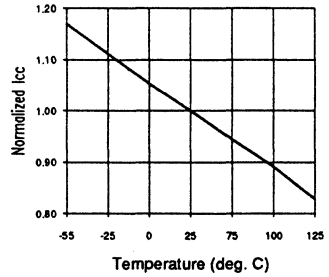
Voh vs Ioh



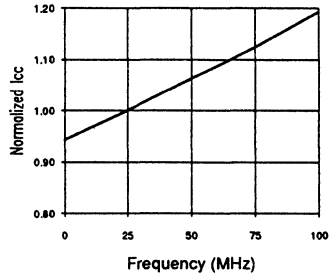
Normalized Icc vs Vcc



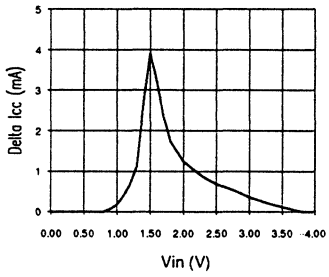
Normalized Icc vs Temp



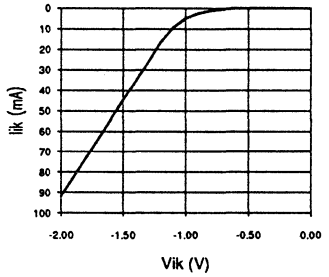
Normalized Icc vs Freq.



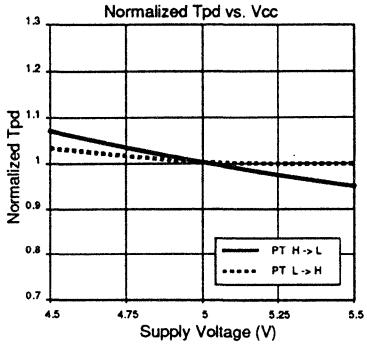
Delta Icc vs Vin (1 input)

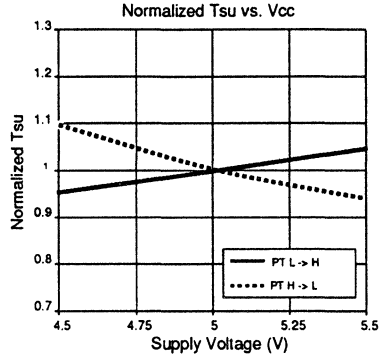


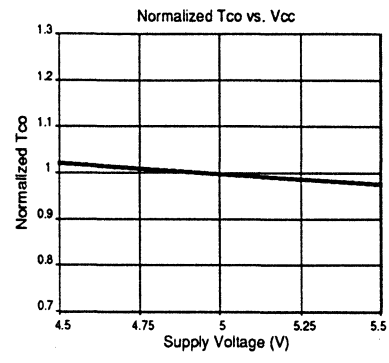
Input Clamp (Vik)

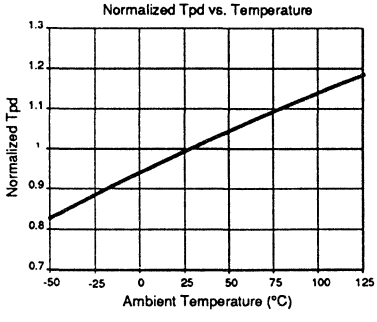


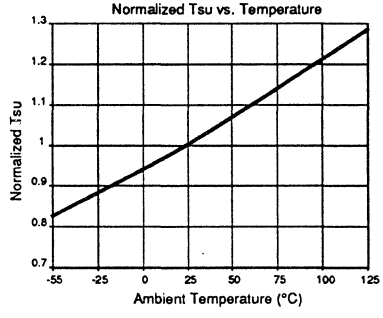
Typical Characteristics

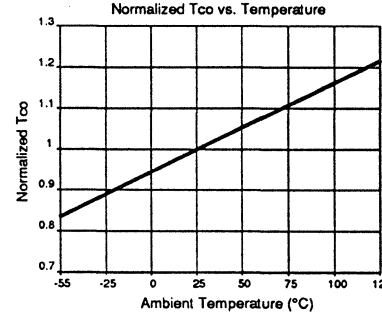


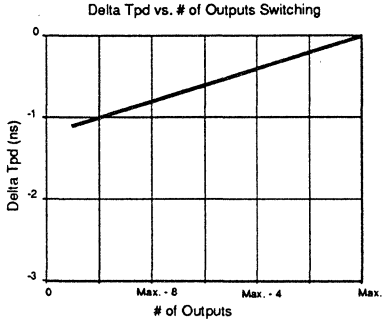


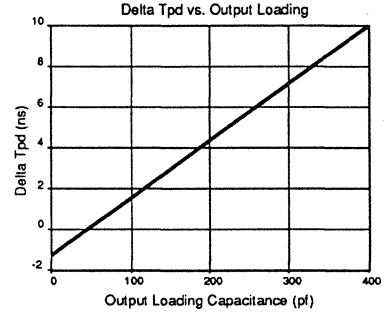


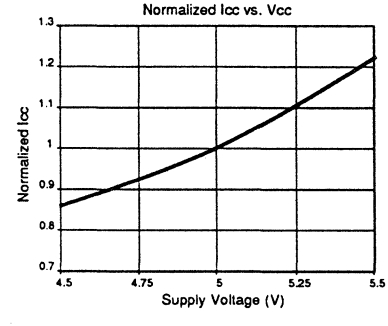


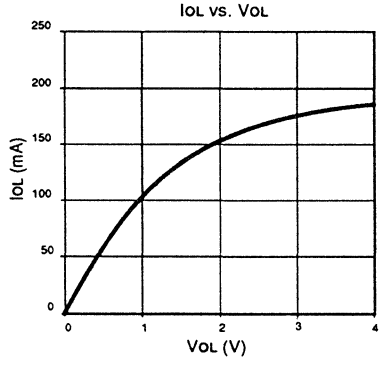


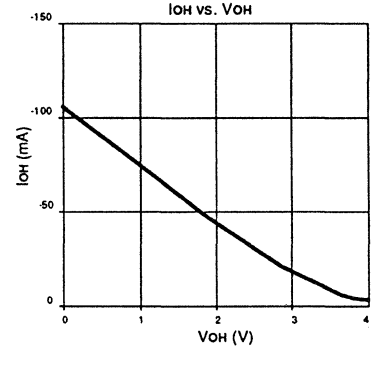


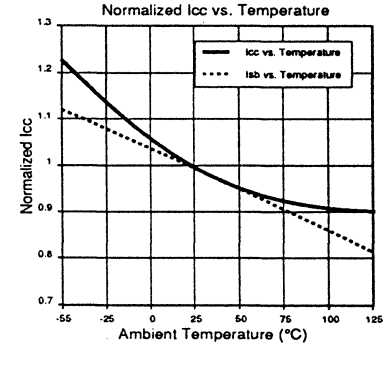












GAL26CV12

High Performance E²CMOS PLD Generic Array Logic™

2

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 10ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 8 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL PINS**
- **LOW POWER CMOS**
  - **— 90 mA Typical Icc**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (50ms)**
  - **— 20 Year Data Retention**
- **TWELVE OUTPUT LOGIC MACROCELLS**
  - **— Uses Standard 22V10 Macrocells**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

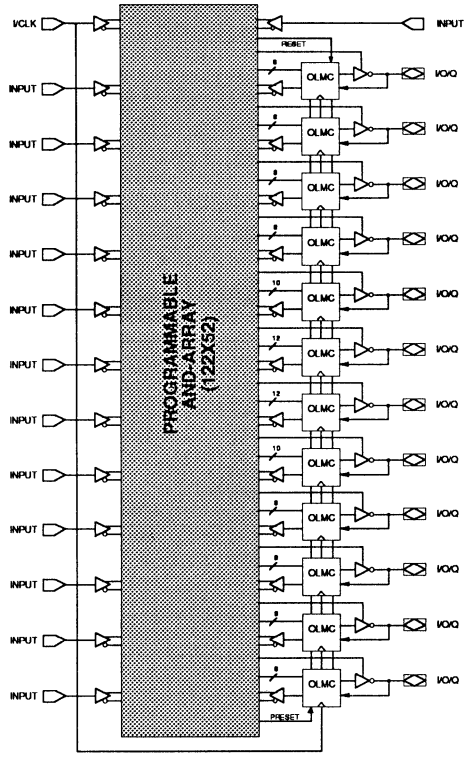
DESCRIPTION

The GAL26CV12, at 15 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance 28 pin PLD available on the market. E² technology offers high speed (50ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

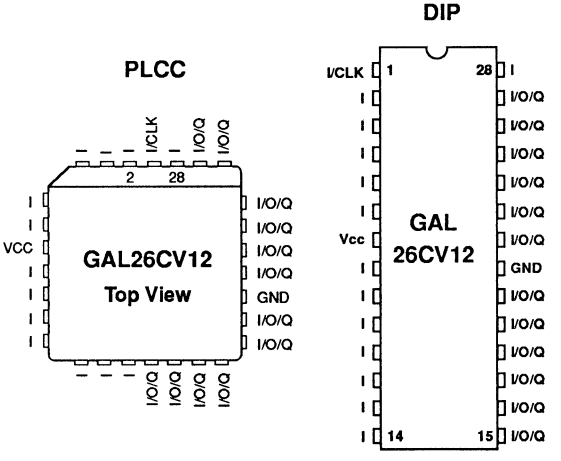
By building on the popular 22V10 architecture, the GAL26CV12 allows the designer to be immediately productive, eliminating the learning curve. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL26CV12 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIAGRAMS



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124 U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

April 1991.Rev.A

GAL26CV12 ORDERING INFORMATION

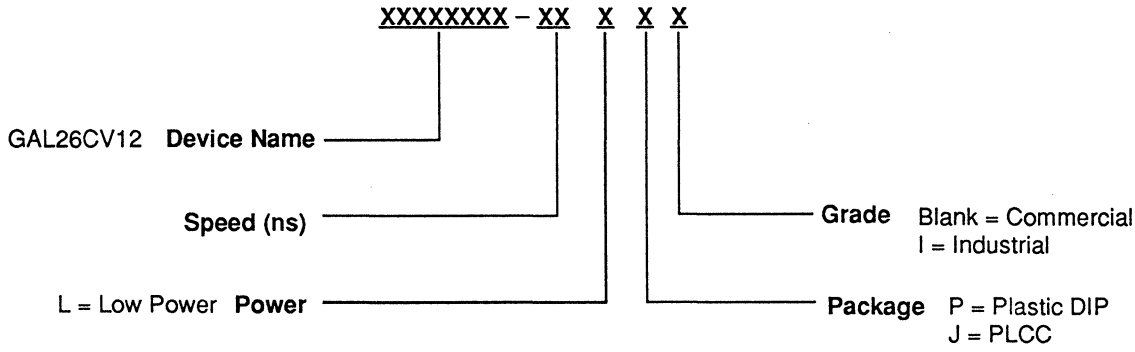
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	10	130	GAL26CV12-15LP	28-Pin Plastic DIP
			130	GAL26CV12-15LJ	28-Lead PLCC
20	12	12	130	GAL26CV12-20LP	28-Pin Plastic DIP
			130	GAL26CV12-20LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	12	12	150	GAL26CV12-20LPI	28-Pin Plastic DIP
			150	GAL26CV12-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



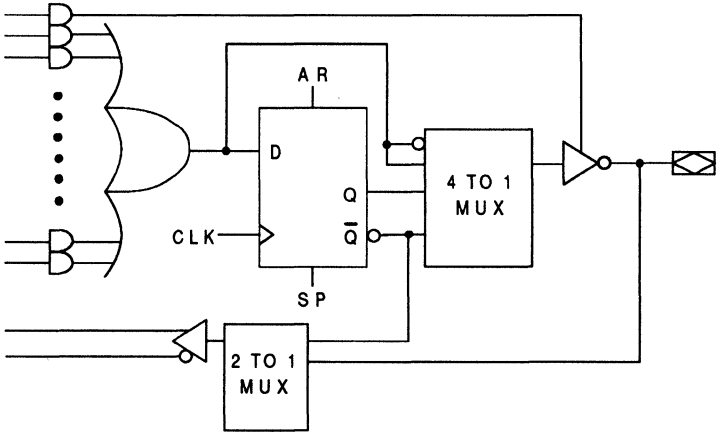
OUTPUT LOGIC MACROCELL (OLMC)

The GAL26CV12 has a variable number of product terms per OLMC. Of the twelve available OLMCs, two OLMCs have access to twelve product terms (pins 20 and 22), two have access to ten product terms (pins 19 and 23), and the other six OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL26CV12 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL26CV12 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL26CV12 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the the following page.

REGISTERED

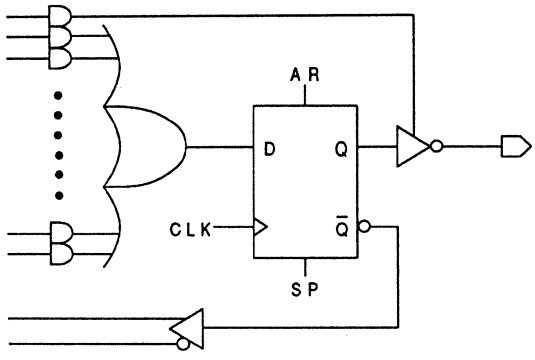
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

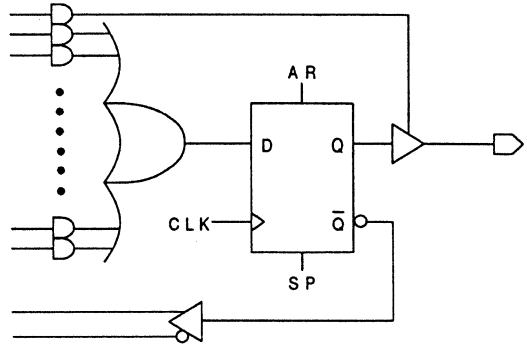
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

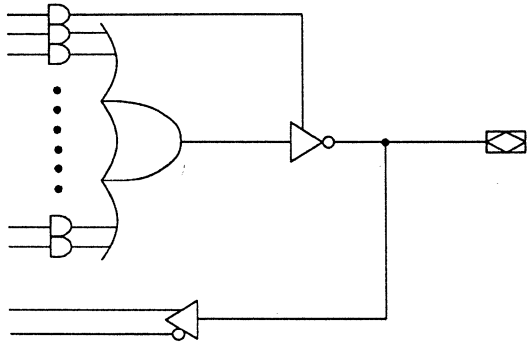
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

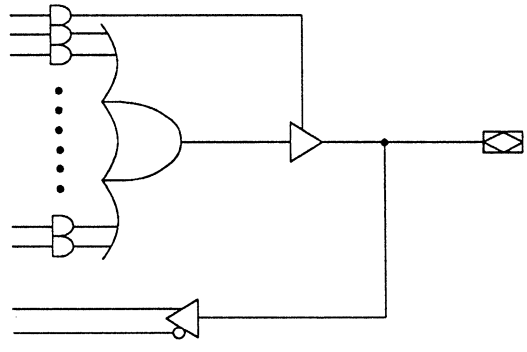
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

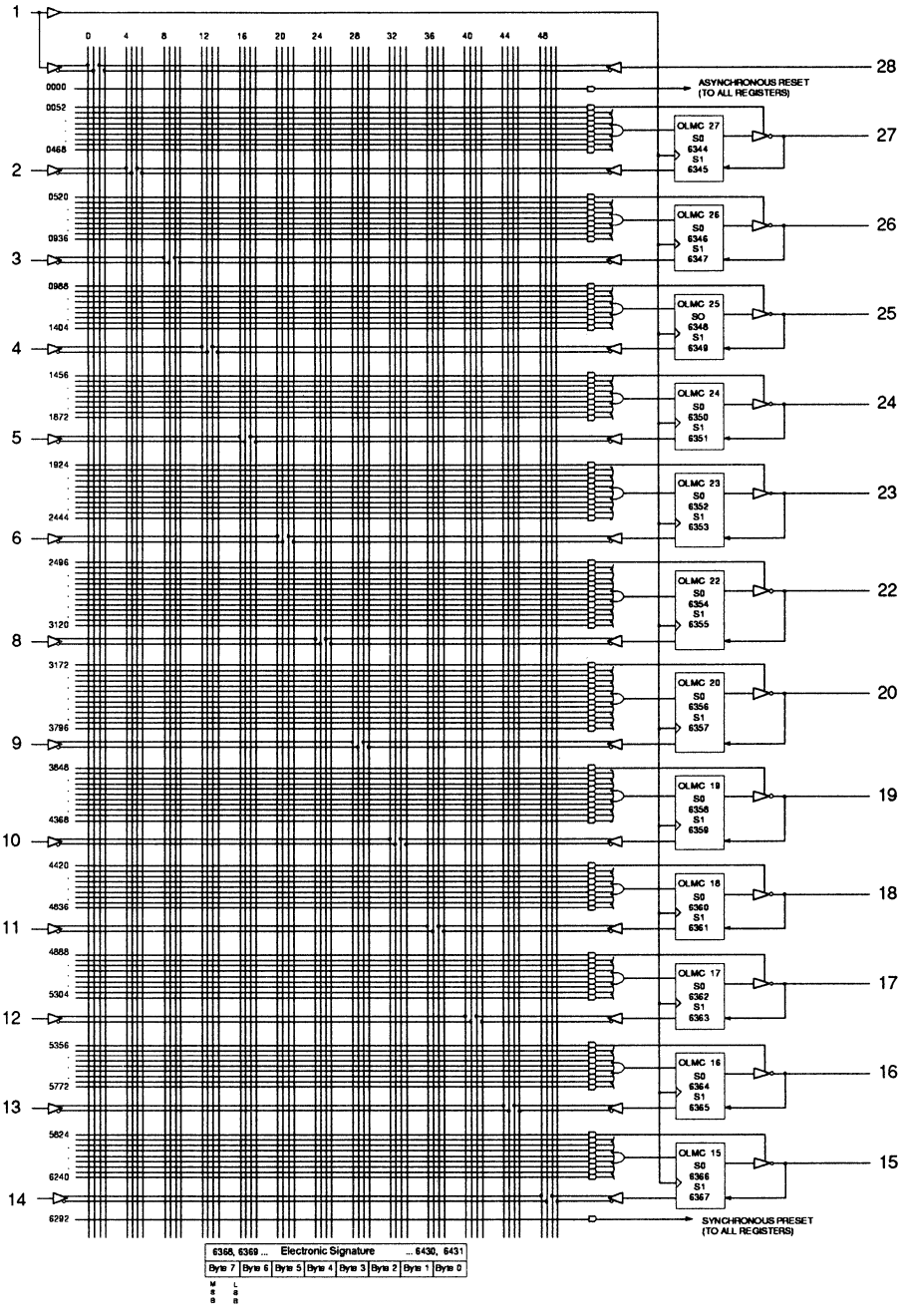
$S_0 = 0$
$S_1 = 1$



ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL26CV12 LOGIC DIAGRAM / JEDEC FUSE MAP



ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V f_{toggle} = 15Mhz Outputs Open	—	90	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	15	—	20	ns
tco	1	Clock to Output Delay	—	10	—	12	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	8	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	8	—	ns
ten	2	Input or I/O to Output Enabled	—	15	—	20	ns
tdis	3	Input or I/O to Output Disabled	—	15	—	20	ns
tar	1	Input or I/O to Asynchronous Reset of Register	—	20	—	20	ns
tarw	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
tarr	—	Asynchronous Reset to Clock↑ Recovery Time	15	—	15	—	ns
tspr	—	Synchronous Preset to Clock↑ Recovery Time	10	—	12	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

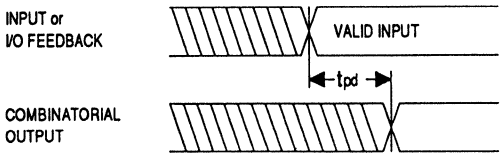
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

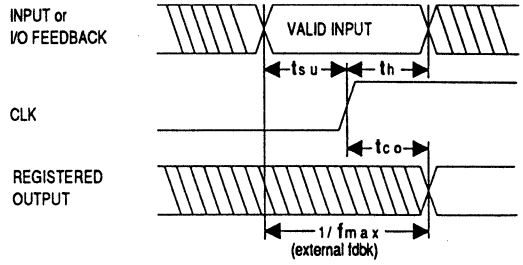
PARAMETER	TEST COND.[1]	DESCRIPTION	-20		UNITS
			MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	20	ns
tco	1	Clock to Output Delay	—	12	ns
tcf[2]	—	Clock to Feedback Delay	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	ns
ten	2	Input or I/O to Output Enabled	—	20	ns
tdis	3	Input or I/O to Output Disabled	—	20	ns
tar	1	Input or I/O to Asynchronous Reset of Register	—	25	ns
tarw	—	Asynchronous Reset Pulse Duration	15	—	ns
tarr	—	Asynchronous Reset to Clock↑ Recovery Time	15	—	ns
tspr	—	Synchronous Preset to Clock↑ Recovery Time	12	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

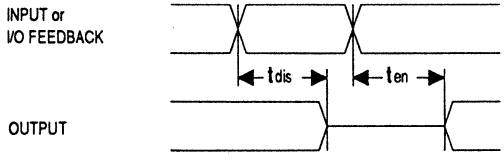
SWITCHING WAVEFORMS



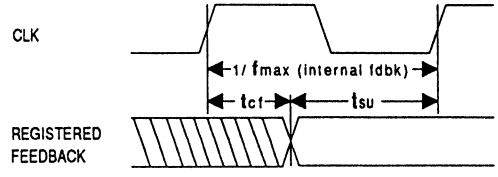
Combinatorial Output



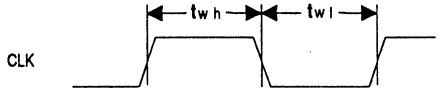
Registered Output



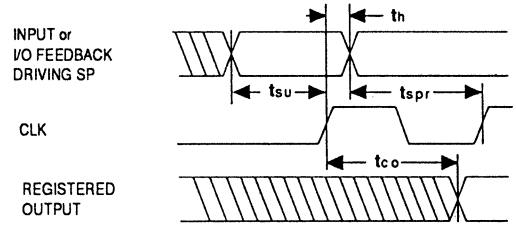
Input or I/O to Output Enable/Disable



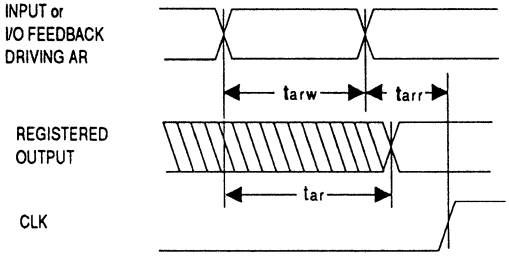
fmax with Feedback



Clock Width

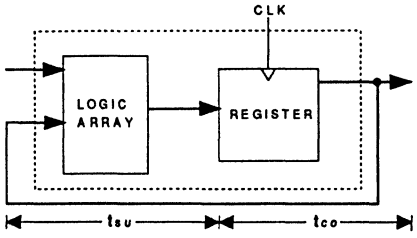


Synchronous Preset



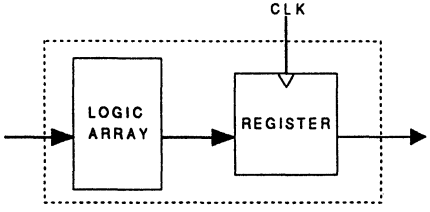
Asynchronous Reset

fmax SPECIFICATIONS



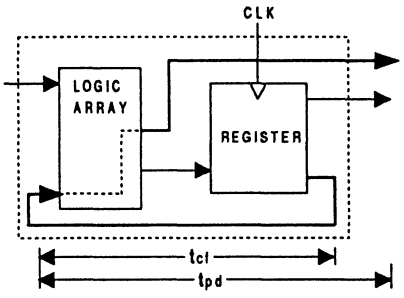
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax With No Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

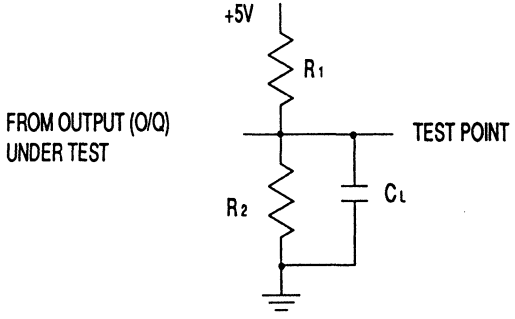
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		470Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	470Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	470Ω	390Ω	5pF



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL26CV12 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided in every GAL26CV12 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL26CV12 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

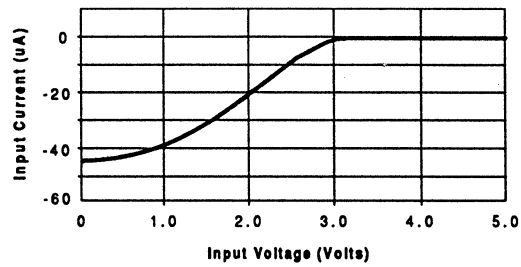
The GAL26CV12 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

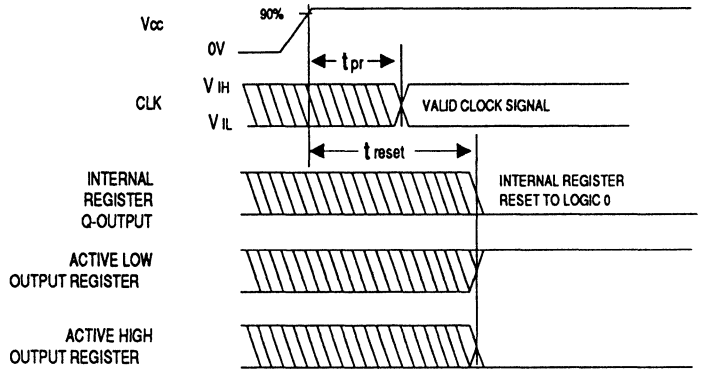
GAL26CV12 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic much less than bipolar TTL logic.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device.

Typical Input Current



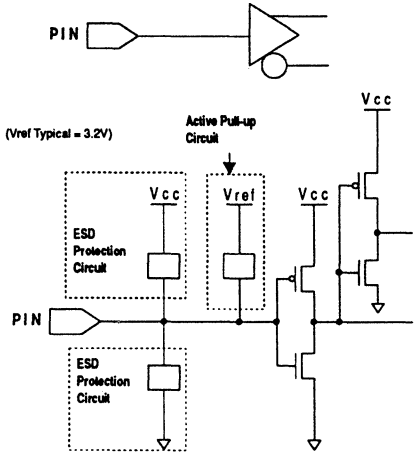
POWER-UP RESET



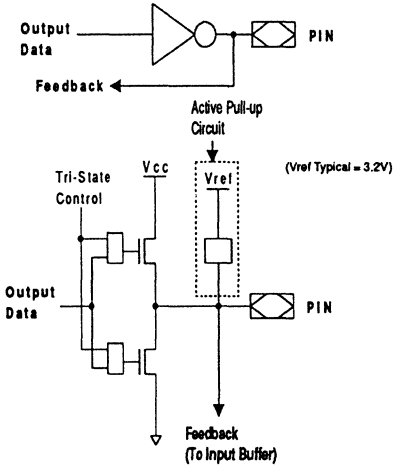
Circuitry within the GAL26CV12 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL26CV12. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



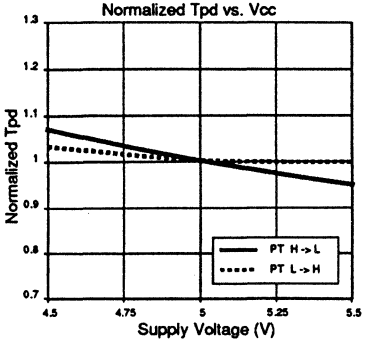
Input



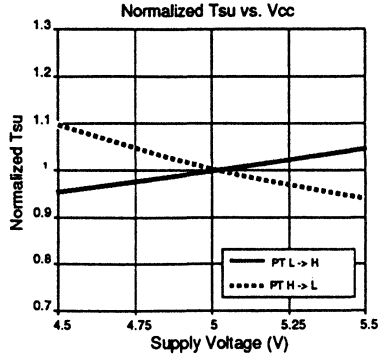
Output

Typical Characteristics

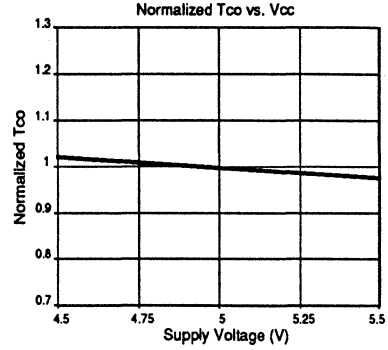
Normalized Tpd vs. Vcc



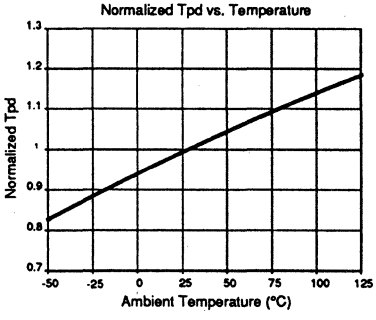
Normalized Tsu vs. Vcc



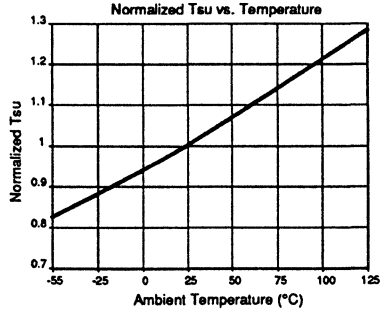
Normalized Tco vs. Vcc



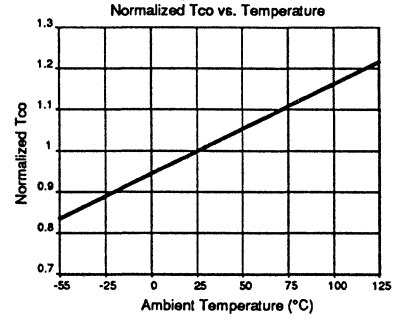
Normalized Tpd vs. Temperature



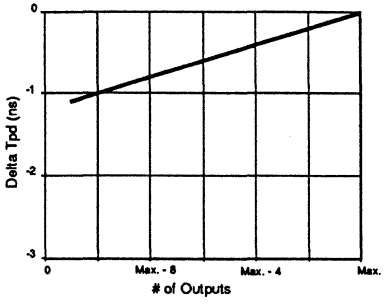
Normalized Tsu vs. Temperature



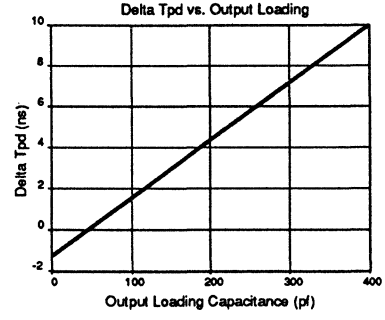
Normalized Tco vs. Temperature



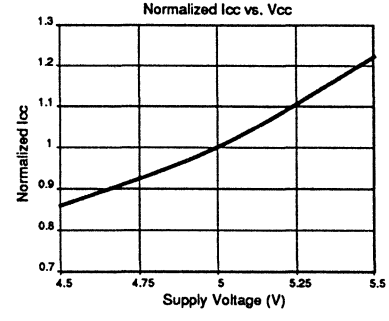
Delta Tpd vs. # of Outputs Switching



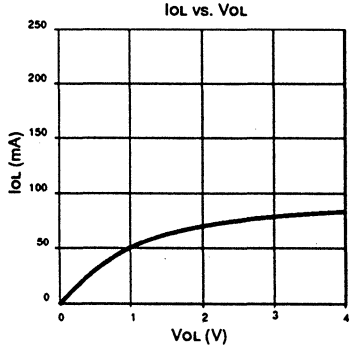
Delta Tpd vs. Output Loading



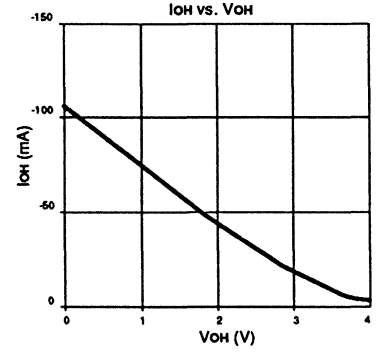
Normalized Icc vs. Vcc



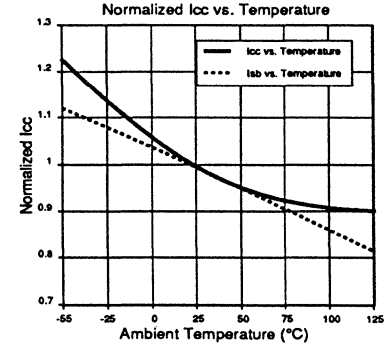
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



Normalized Icc vs. Temperature



GAL20RA10

High-Speed Asynchronous E²CMOS PLD
Generic Array Logic™

2

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 12 ns Maximum Propagation Delay**
  - **— Fmax = 71.4 MHz**
  - **— 12 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 8 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ I_{cc}**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<50 ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Independent Programmable Clocks**
  - **— Independent Asynchronous Reset and Preset**
  - **— Registered or Combinatorial with Polarity**
  - **— Full Function and Parametric Compatibility with PAL20RA10**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— State Machine Control**
  - **— Standard Logic Consolidation**
  - **— Multiple Clock Logic Designs**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

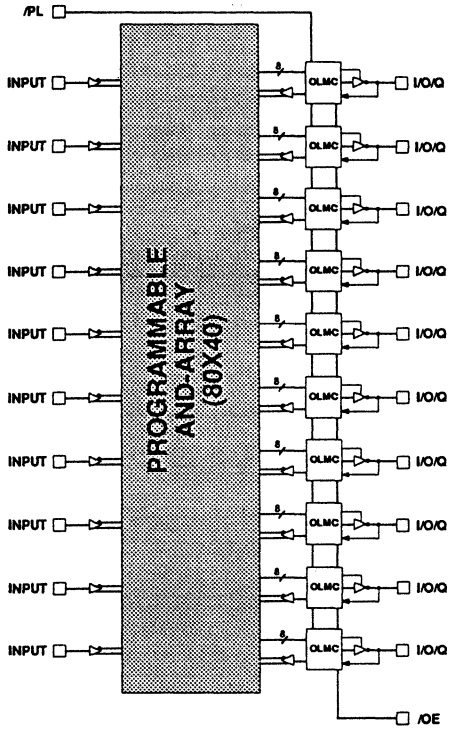
DESCRIPTION

The GAL20RA10 combines a high performance CMOS process with electrically erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. Lattice's E²CMOS circuitry achieves power levels as low as 75mA typical I_{cc} which represents a substantial savings in power when compared to bipolar counterparts. E² technology offers high speed (<50ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

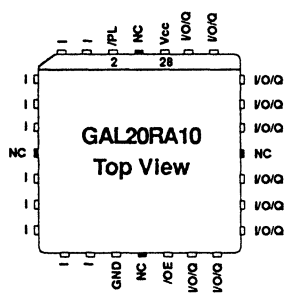
Unique test circuitry and reprogrammable cells allow complete AC,DC, and functional testing during manufacturing. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM

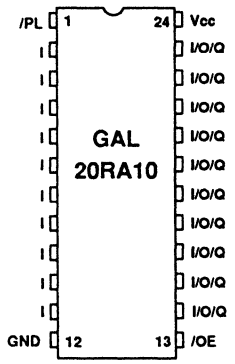


PIN CONFIGURATION

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

April 1991.Rev.B

GAL20RA10 ORDERING INFORMATION

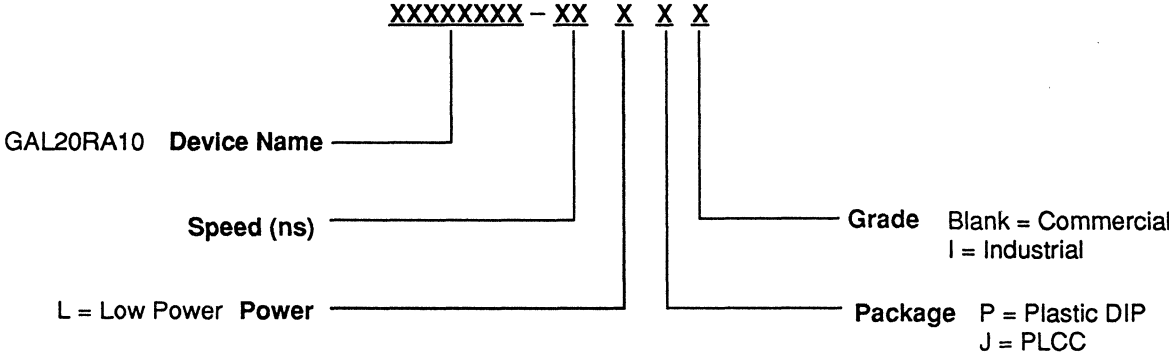
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
12	4	12	100	GAL20RA10-12LP	24-Pin Plastic DIP
			100	GAL20RA10-12LJ	28-Lead PLCC
15	7	15	100	GAL20RA10-15LP	24-Pin Plastic DIP
			100	GAL20RA10-15LJ	28-Lead PLCC
20	10	20	100	GAL20RA10-20LP	24-Pin Plastic DIP
			100	GAL20RA10-20LJ	28-Lead PLCC
30	20	30	100	GAL20RA10-30LP	24-Pin Plastic DIP
			100	GAL20RA10-30LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	10	20	120	GAL20RA10-20LPI	24-Pin Plastic DIP
			120	GAL20RA10-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The GAL20RA10 consists of 10 D flip-flops with individual asynchronous programmable reset, preset and clock product terms. The sum of four product terms and an Exclusive-OR provide a programmable polarity D-input to each flip-flop. An output enable term combined with the dedicated output enable pin provides tri-state control of each output. Each OLMC has a flip-flop bypass, allowing any combination of registered or combinatorial outputs.

The GAL20RA10 has 10 dedicated input pins and 10 programmable I/O pins, which can be either inputs, outputs, or dynamic I/O. Each pin has a unique path to the logic array. All macrocells have the same type and number of data and control product terms, allowing the user to exchange I/O pin assignments without restriction.

INDEPENDENT PROGRAMMABLE CLOCKS

An independent clock control product term is provided for each GAL20RA10 macrocell. Data is clocked into the flip-flop on the active edge of the clock product term. The use of individual clock control product terms allow up to ten separate clocks. These clocks can be derived from any pin or combination of pins and/or feedback from other flip-flops. Multiple clock sources allow a number of asynchronous register functions to be combined into a single GAL20RA10. This allows the designer to combine discrete logic functions into a single device.

PROGRAMMABLE POLARITY

The polarity of the D-input to each macrocell flip-flop is individually programmable to be active high or low. This is accomplished with a programmable Exclusive-OR gate on the D-input of each flip-flop. While any one of the four logic function product terms are active the D-input to the flip-flop will be low if the Exclusive-OR bit is set to zero(0) and high if the Exclusive-OR bit is set to one(1). It should be noted that the programmable polarity only affects the data latched into the flip-flop on the active edge of the clock product term. The reset, preset and preload will alter the state of the flip-flop independent of the state of programmable polarity bit. The ability to program the active polarity of the D-inputs can be used to reduce the total number of product terms used, by allowing the DeMorganization of the logic functions. This logic reduction is accomplished by the logic compiler, and does not require the designer to define the polarity.

OUTPUT ENABLE

The output of each GAL20RA10 macrocell is controlled by the "AND'ing" of an independent output enable product term and a common active low output enable pin(13). The output is enabled while the output enable product term is active and the output enable pin(13) is low. This output control structure allows several output enable alternatives.

ASYNCHRONOUS RESET AND PRESET

Each GAL20RA10 macrocell has an independent asynchronous reset and preset control product term. The reset and preset product terms are level sensitive, and will hold the flip-flop in the reset or preset state while the product term is active independent of the clock or D-inputs. It should be noted that the reset and preset term alter the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low.

RESET	PRESET	FUNCTION
0	0	Registered function of data product term
1	0	Reset register to "0" (device pin = "1")
0	1	Preset register to "1" (device pin = "0")
1	1	Register-bypass (combinatorial output)

COMBINATORIAL CONTROL

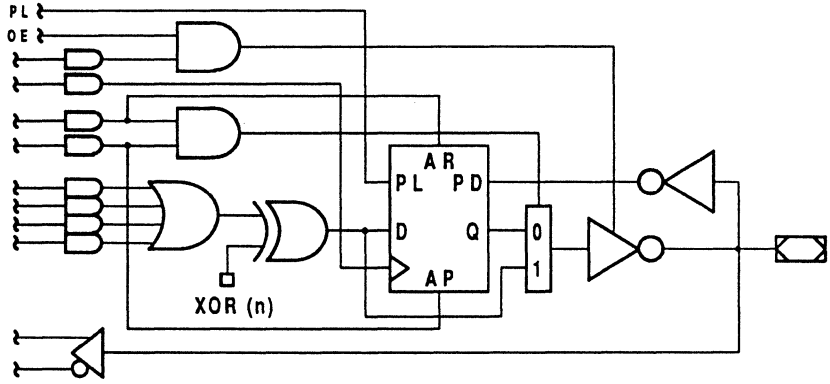
The register in each GAL20RA10 macrocell may be bypassed by asserting both the reset and preset product terms. While both product terms are active the flip-flop is bypassed and the D- input is presented directly to the inverting output buffer. This provides the designer the ability to dynamically configure any macrocell as a combinatorial output, or to fix the macrocell as combinatorial only by forcing both reset and preset product terms active. Some logic compilers will configure macrocells as registered or combinatorial based on the logic equations, others require the designer to force the reset and preset product terms active for combinatorial macrocells.

PARALLEL FLIP-FLOP PRELOAD

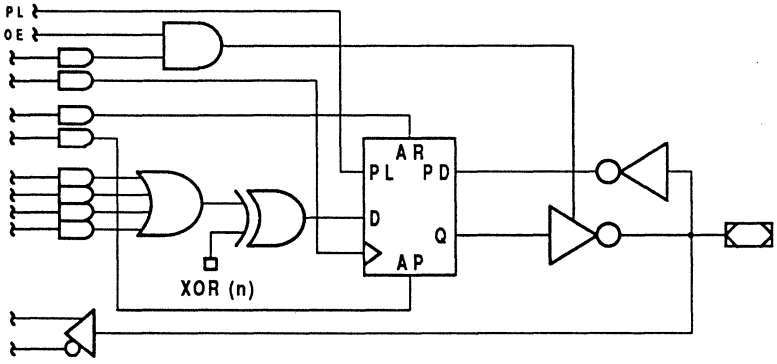
The flip-flops of a GAL20RA10 can be reset or preset from the I/O pins by applying a logic low to the preload pin (1) and applying the desired logic level to each I/O pin. The I/O pins must remain valid for the preload setup and hold time. All 10 flip-flops are reset or preset during preload, independent of all other OLMC inputs.

A logic low on an I/O pin during preload will preset the flip-flop, a logic high will reset the flip-flop. The output of any flip-flop to be preloaded must be disabled. Enabling the output during preload will maintain the current logic state. It should be noted that the preload alters the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low. Note that the common output enable pin (13) will disable all 10 outputs of the GAL20RA10 when held high.

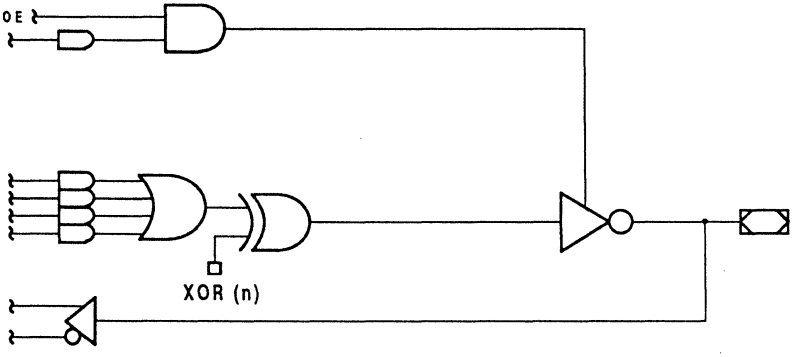
OUTPUT LOGIC MACROCELL DIAGRAM



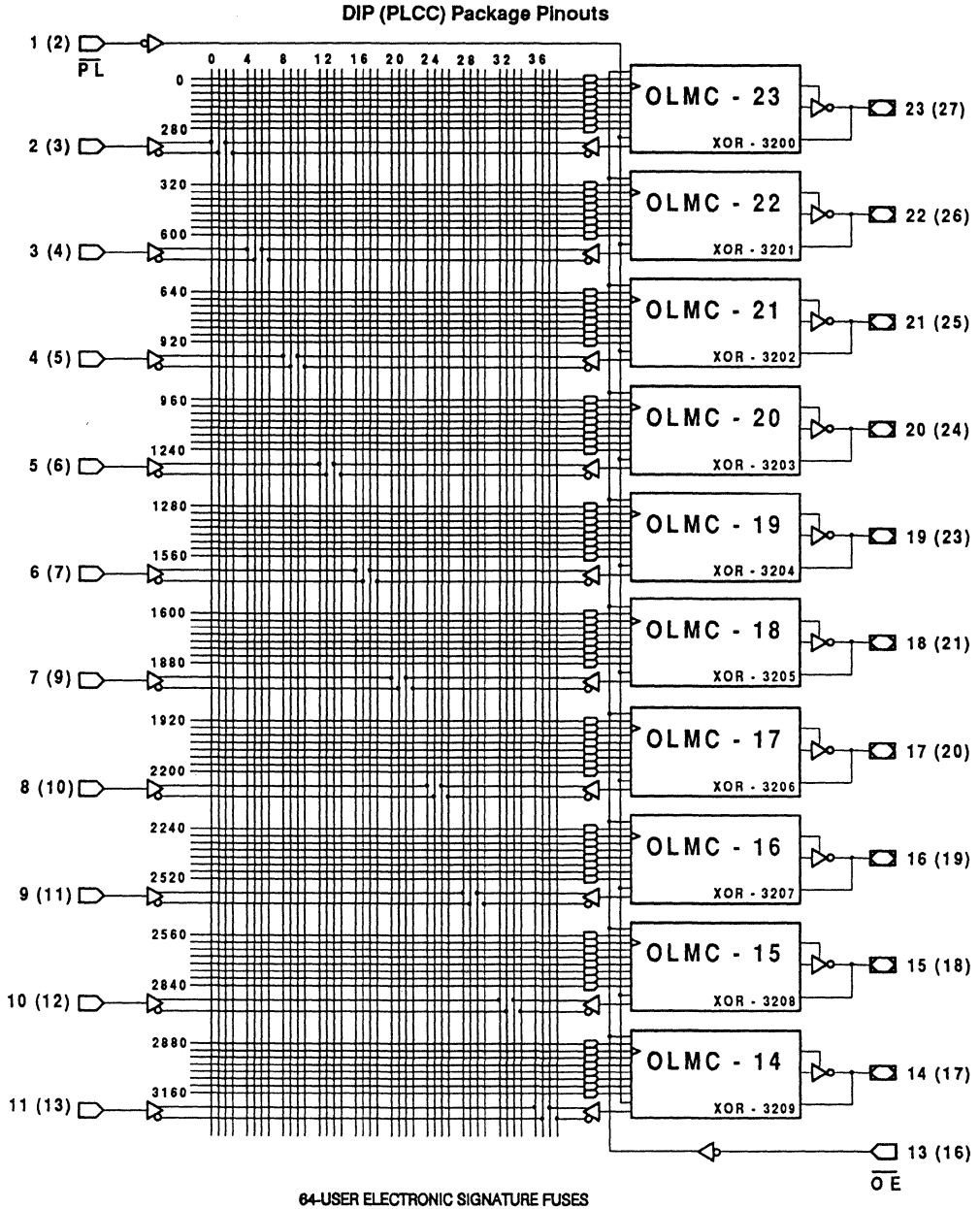
OUTPUT LOGIC MACROCELL CONFIGURATION (REGISTERED with POLARITY)



OUTPUT LOGIC MACROCELL CONFIGURATION (COMBINATORIAL with POLARITY)



GAL20RA10 LOGIC DIAGRAM



64-USER ELECTRONIC SIGNATURE FUSES

3210, 3211, ...	.... 3272, 3273
Byte 7 | Byte 6	.... Byte 1 | Byte 0

M L
S S
B B

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Ambient Temperature with
Power Applied .....-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) .....0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	75	100	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-12		-15		-20		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	12	—	15	—	20	—	30	ns
tco	1	Clock to Output Delay	—	12	—	15	—	20	—	30	ns
tsu	—	Setup Time, Input or Feedback before Clock	4	—	7	—	10	—	20	—	ns
th	—	Hold Time, Input or Feedback after Clock	3	—	3	—	3	—	10	—	ns
fmax[2]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	62.5	—	45.0	—	33.3	—	20.0	—	MHz
	1	Maximum Clock Frequency without Feedback	71.4	—	50.0	—	41.7	—	25.0	—	MHz
twh[3]	—	Clock Pulse Duration, High	7	—	10	—	12	—	20	—	ns
twl[3]	—	Clock Pulse Duration, Low	7	—	10	—	12	—	20	—	ns
ten / tdis	2,3	Input or I/O to Output Enabled / Disabled	—	12	—	15	—	20	—	30	ns
ten / tdis	2,3	$\overline{OE}$ to Output Enabled / Disabled	—	9	—	12	—	15	—	20	ns
tar / tap	1	Input or I/O to Asynchronous Reset / Preset	—	12	—	15	—	20	—	30	ns
tarw / tapw	—	Asynchronous Reset / Preset Pulse Duration	12	—	15	—	20	—	20	—	ns
tarr / tapr	—	Asynchronous Reset / Preset Recovery Time	7	—	10	—	12	—	20	—	ns
twp	—	Preload Pulse Duration	12	—	15	—	20	—	30	—	ns
tsp	—	Preload Setup Time	7	—	10	—	15	—	25	—	ns
thp	—	Preload Hold Time	7	—	10	—	15	—	25	—	ns

1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Descriptions** section.
3) Clock pulses of widths less than the specification may be detected as valid clock signals.

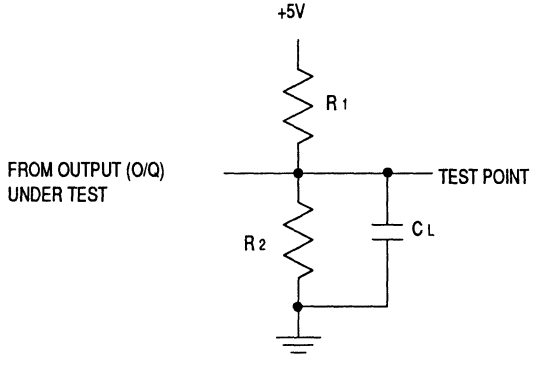
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		470Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	470Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	470Ω	390Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Ambient Temperature with
Power Applied .....-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Industrial Devices:
Ambient Temperature (T_A) .....-40 to +85°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	75	120	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-20		UNITS
			MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	20	ns
tco	1	Clock to Output Delay	—	20	ns
tsu	—	Setup Time, Input or Feedback before Clock	10	—	ns
th	—	Hold Time, Input or Feedback after Clock	3	—	ns
fmax[2]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	33.3	—	MHz
	1	Maximum Clock Frequency without Feedback	41.7	—	MHz
twh[3]	—	Clock Pulse Duration, High	12	—	ns
twl[3]	—	Clock Pulse Duration, Low	12	—	ns
ten / tdis	2,3	Input or I/O to Output Enabled / Disabled	—	20	ns
ten / tdis	2,3	$\overline{OE}$ to Output Enabled / Disabled	—	15	ns
tar / tap	1	Input or I/O to Asynchronous Reset / Preset	—	20	ns
tarw / tapw	—	Asynchronous Reset / Preset Pulse Duration	20	—	ns
tarr / tapr	—	Asynchronous Reset / Preset Recovery Time	12	—	ns
twp	—	Preload Pulse Duration	20	—	ns
tsp	—	Preload Setup Time	15	—	ns
thp	—	Preload Hold Time	15	—	ns

1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Descriptions** section.
3) Clock pulses of widths less than the specification may be detected as valid clock signals.

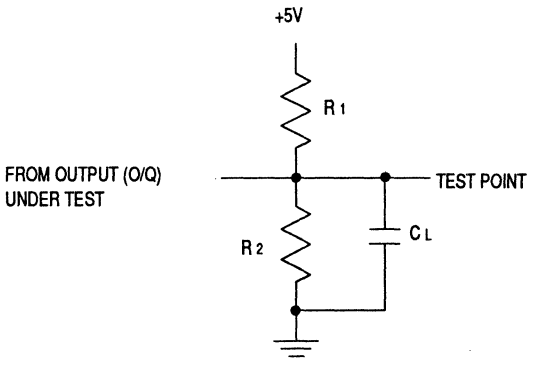
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

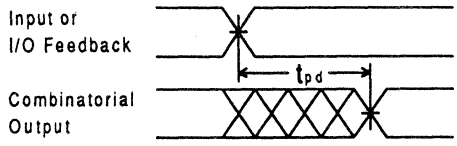
Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		470Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	470Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	470Ω	390Ω	5pF

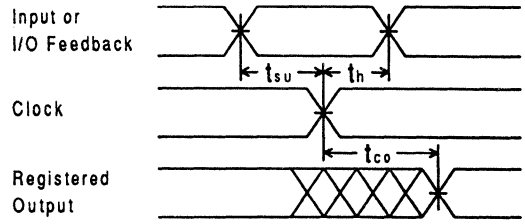


C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

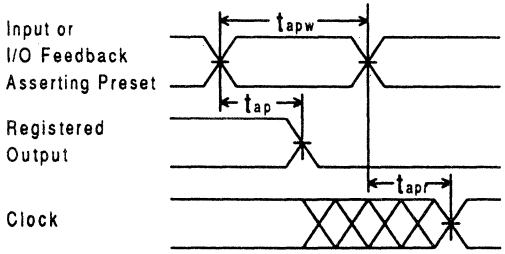
SWITCHING WAVEFORMS



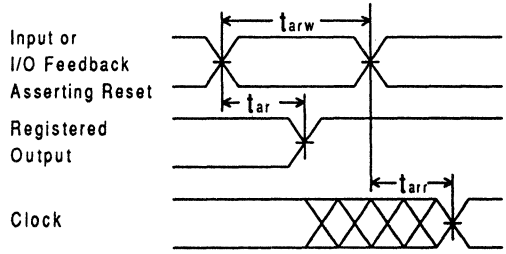
Combinatorial Output



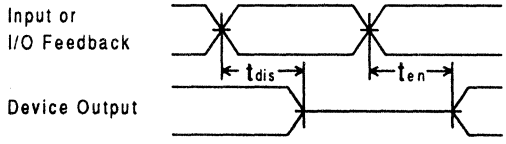
Registered Output



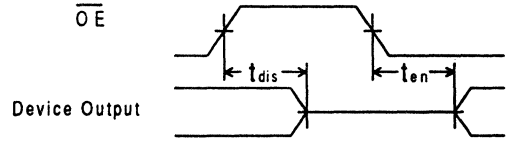
Asynchronous Preset



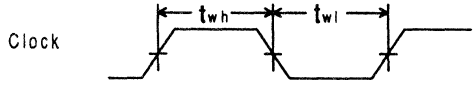
Asynchronous Reset



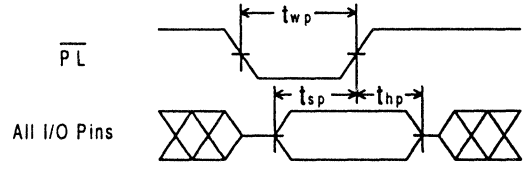
Input or I/O Feedback to Enable / Disable



OE to Enable / Disable

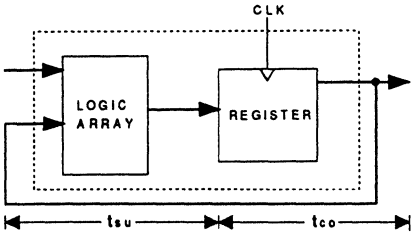


Clock Width



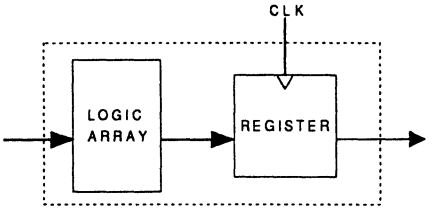
Parallel Preload

fmax DESCRIPTIONS



fmax with External Feedback 1/(tsu+tco)

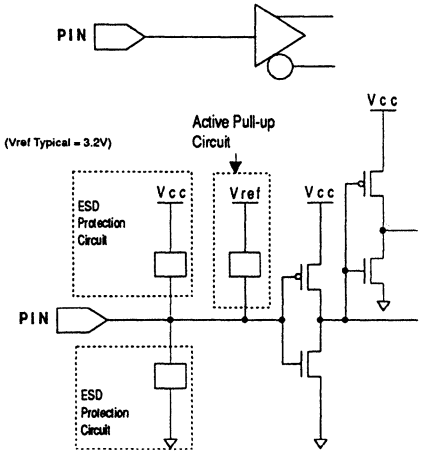
Note: fmax with external feedback is calculated from measured tsu and tco.



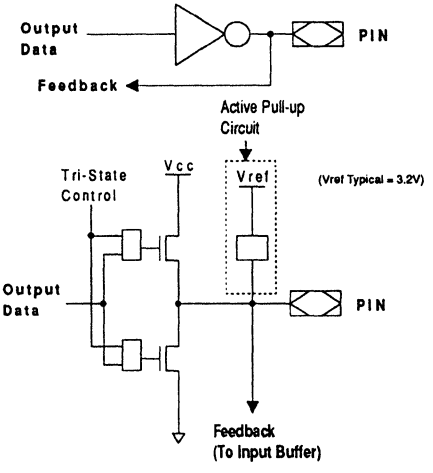
fmax With No Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



Output

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20RA10 device. It contains 64 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits if programmed to any value other then zero(0) will alter the checksum of the device.

SECURITY CELL

A security cell is provided in every GAL20RA10 devices as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

LATCH-UP PROTECTION

GAL20RA10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

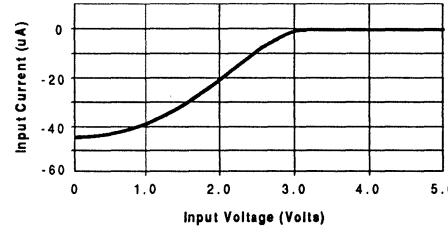
GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

INPUT BUFFERS

GAL20RA10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance and present a much lighter load to the driving logic than traditional bipolar devices.

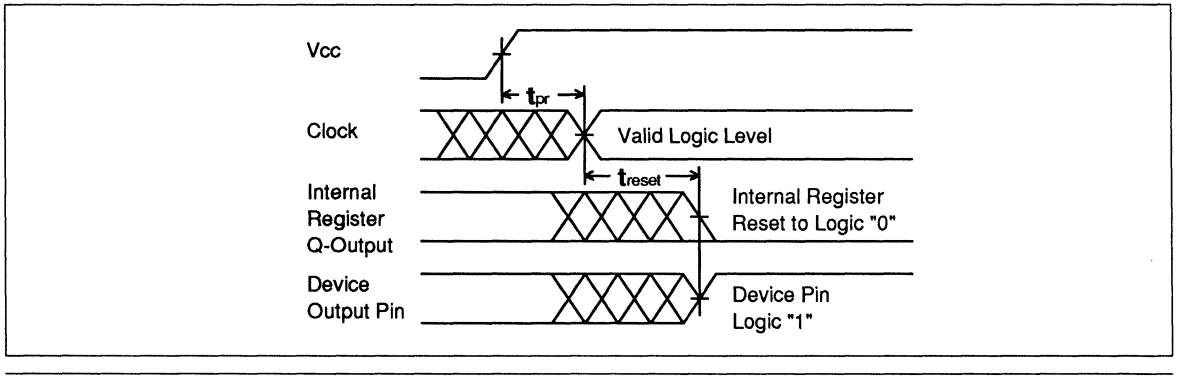
GAL20RA10 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Typical Input Pull-up Characteristic

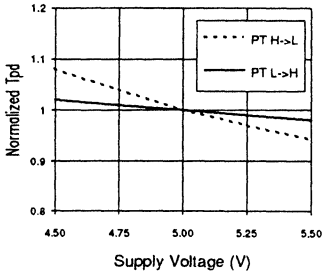


POWER-UP RESET

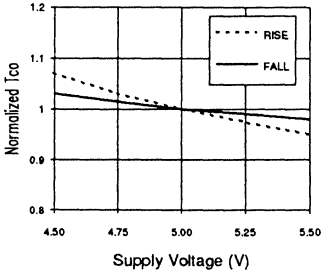
Circuitry within the GAL20RA10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20RA10. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.



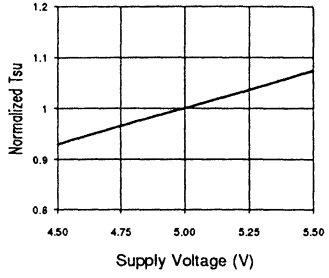
Normalized Tpd vs Vcc



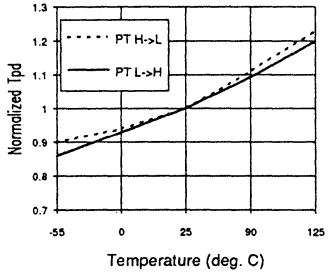
Normalized Tco vs Vcc



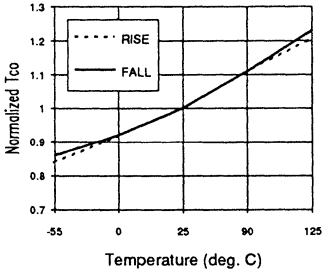
Normalized Tsu vs Vcc



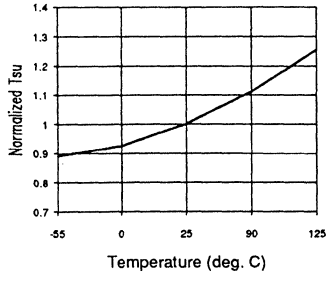
Normalized Tpd vs Temp



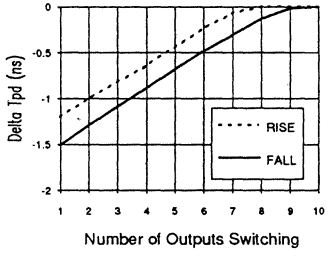
Normalized Tco vs Temp



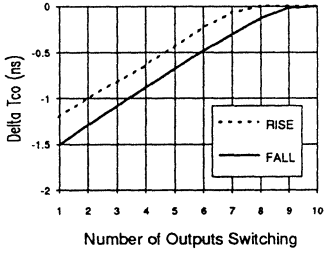
Normalized Tsu vs Temp



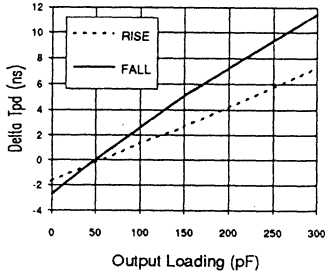
Delta Tpd vs # of Outputs Switching



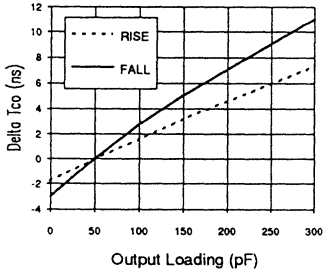
Delta Tco vs # of Outputs Switching



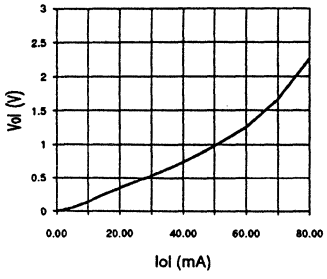
Delta Tpd vs Output Loading



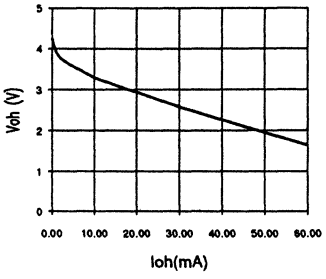
Delta Tco vs Output Loading



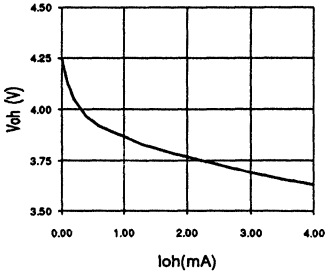
Vol vs Iol



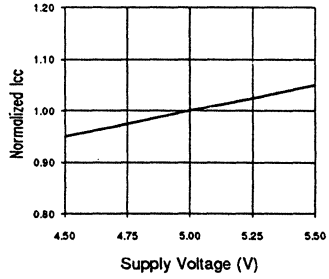
Voh vs Ioh



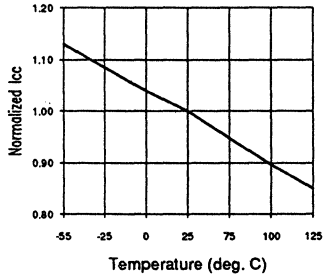
Voh vs Ioh



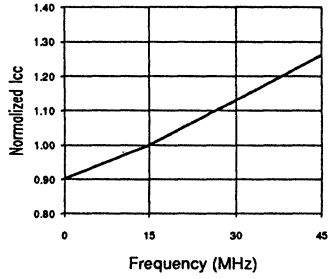
Normalized Icc vs Vcc



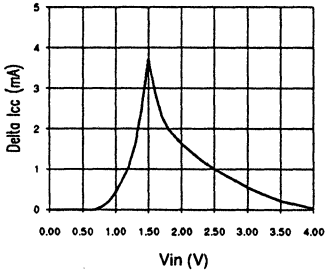
Normalized Icc vs Temp



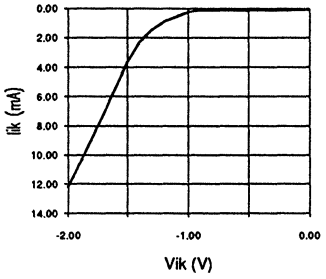
Normalized Icc vs Freq.



Delta Icc vs Vin (1 Input)



Input Clamp (Vik)



GAL6001

High Performance E²CMOS FPLA Generic Array Logic™

2

FEATURES

- **ELECTRICALLY ERASABLE CELL TECHNOLOGY**
  - **Instantly Reconfigurable Logic**
  - **Instantly Reprogrammable Cells**
  - **Guaranteed 100% Yields**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **Low Power: 90mA Typical**
  - **High Speed: 12ns Max. Clock to Output Delay**
    25ns Min. Setup Time
    30ns Max. Propagation Delay
- **UNPRECEDENTED FUNCTIONAL DENSITY**
  - **78 x 64 x 36 FPLA Architecture**
  - **10 Output Logic Macrocells**
  - **8 Buried Logic Macrocells**
  - **20 Input and I/O Logic Macrocells**
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - **Asynchronous or Synchronous Clocking**
  - **Separate State Register and Input Clock Pins**
  - **Functionally Supersets Existing 24-pin PAL® and IFL™ Devices**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **SPACE SAVING 24-PIN, 300-MIL DIP**
- **HIGH SPEED PROGRAMMING ALGORITHM**
- **APPLICATIONS INCLUDE:**
  - **Sequencer**
  - **State Machine Control**
  - **Multiple PLD Device Integration**

DESCRIPTION

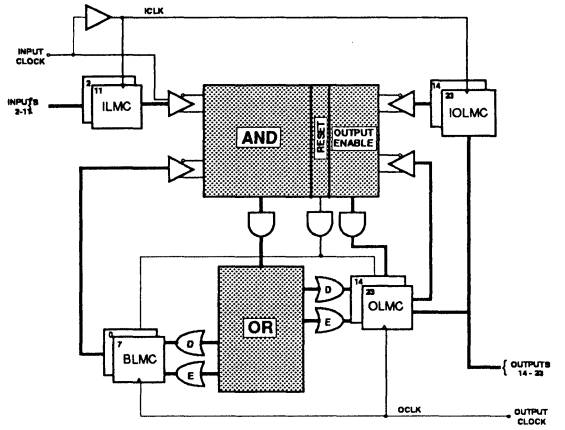
Using a high performance E²CMOS technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package.

The GAL6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. This allows Lattice to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

Programming is accomplished using standard hardware and software tools. In addition, an Electronic Signature is available for storage of user specified data, and a security cell is provided to protect proprietary designs.

FUNCTIONAL BLOCK DIAGRAM



MACROCELL NAMES

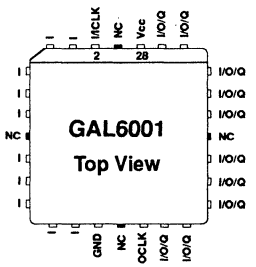
ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

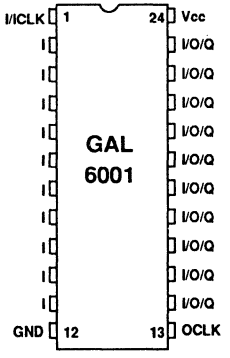
I_0 - I_{10}	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION

PLCC



DIP



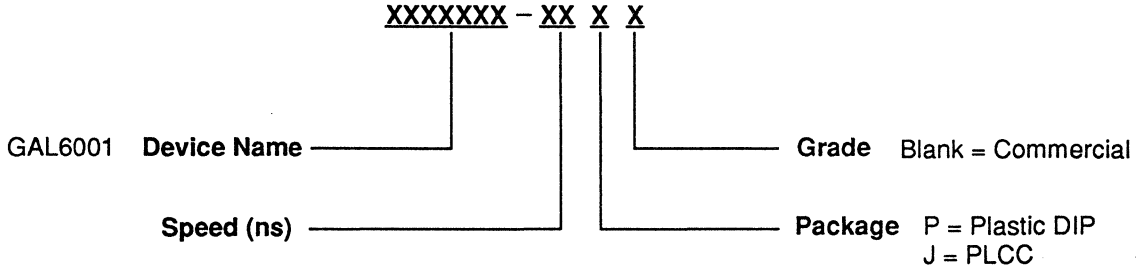
LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon U.S.A.
Tel. (503) 681-0118 or 1-800-FAST GAL; FAX (503) 681-3037

GAL6001 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Fclk (MHz)	Icc (mA)	Ordering #	Package
30	27	150	GAL6001-30P	24-Pin Plastic DIP
		150	GAL6001-30J	28-Lead PLCC
35	22.9	150	GAL6001-35P	24-Pin Plastic DIP
		150	GAL6001-35J	28-Lead PLCC

GAL6001 ORDERING INFORMATION



INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide systems designers with unparalled design flexibility. With the GAL6001, external registers and latches are not necessary.

Both the ILMC and the IOLMC are block configurable. However, the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinational, "D-type register with sum term (asynchronous) clock", or "D/E-type register." Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the "D" XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all "E" sum terms is selected through the "E" XOR.

When the macrocell is configured as a "D/E type registered", the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.

When the macrocell is configured as a "D type register with a sum term clock", the register is always enabled and its "E" sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

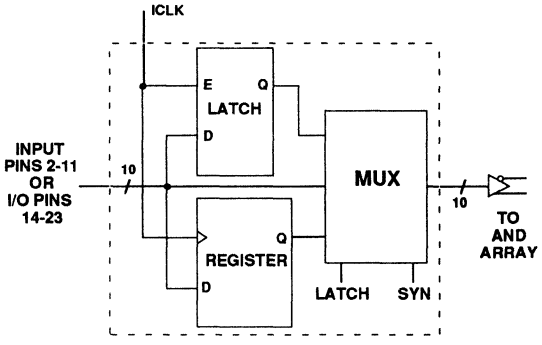
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an output pin, a logic one will occur because of the inverting output buffer.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer and always present). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried (the associated OLMC pin is an input), or dynamically buried with the use of the output enable product term.

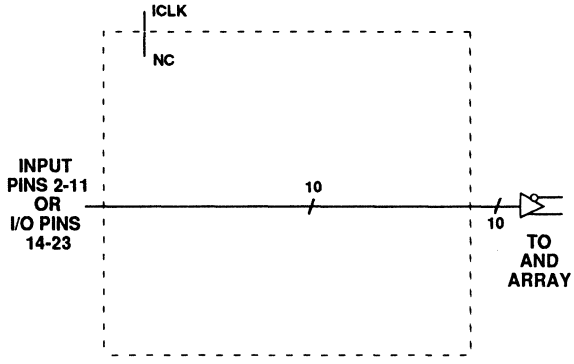
The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

The three macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

ILMC AND IOLMC CONFIGURATIONS

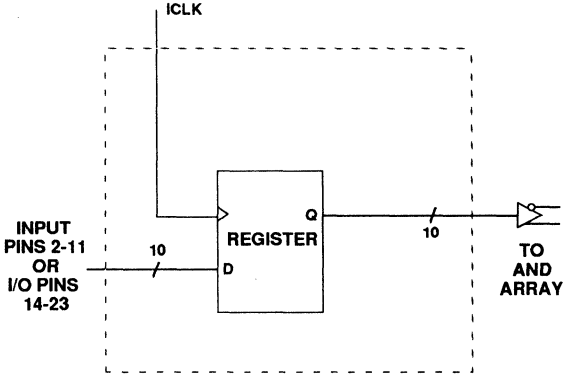


ILMC/IOLMC
Generic Block Diagram



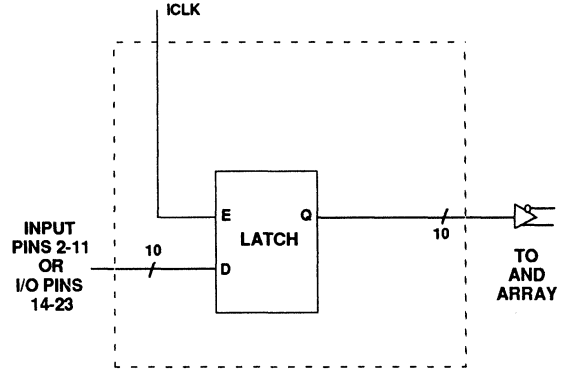
Asynchronous Input

LATCH	SYN
1	1



Registered Input

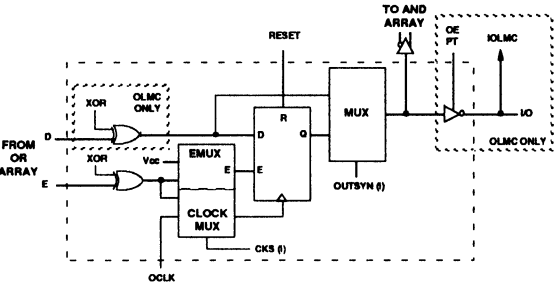
LATCH	SYN
1	0



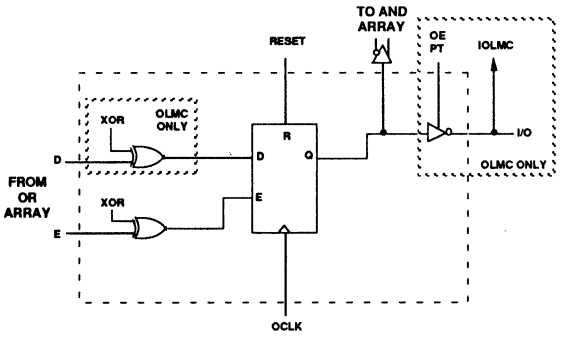
Latched Input

LATCH	SYN
0	0

OLMC AND BLMC CONFIGURATIONS

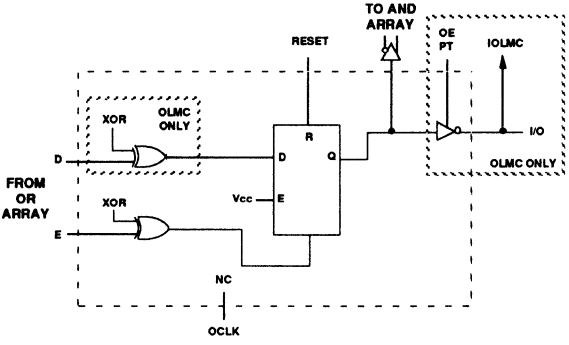


OLMC/BLMC
Generic Block Diagram



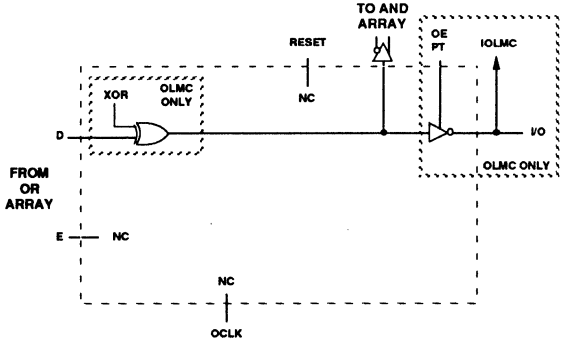
D/E Type Registered

CKS(i)	OUTSYN(i)
1	0



D Type Register with Sum Term Asynchronous Clock

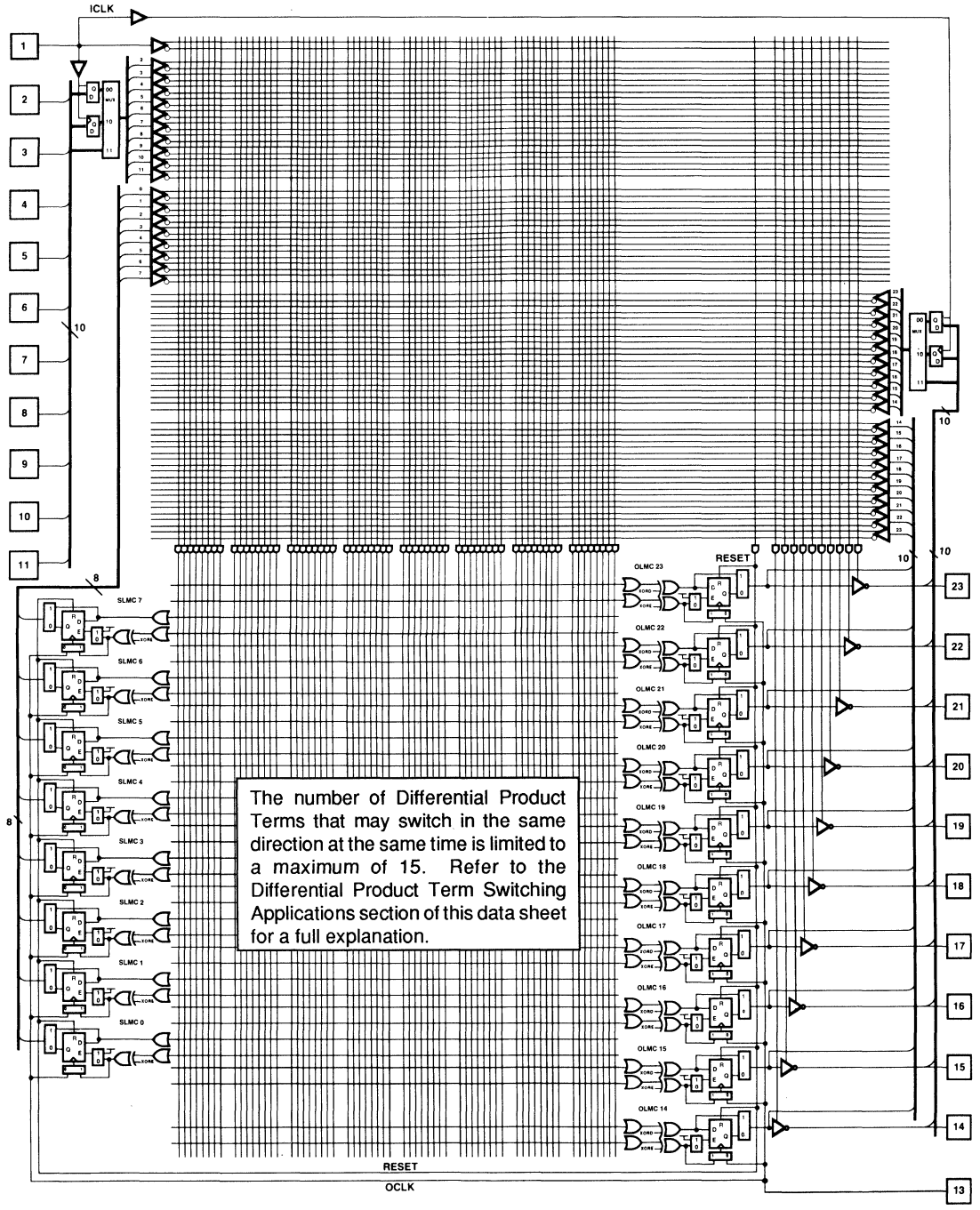
CKS(i)	OUTSYN(i)
0	0



Combinational

CKS(i)	OUTSYN(i)
0	1

GAL6001 LOGIC DIAGRAM



The number of Differential Product Terms that may switch in the same direction at the same time is limited to a maximum of 15. Refer to the Differential Product Term Switching Applications section of this data sheet for a full explanation.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V ftoggle = 15MHz Outputs Open (no load)	—	90	150	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

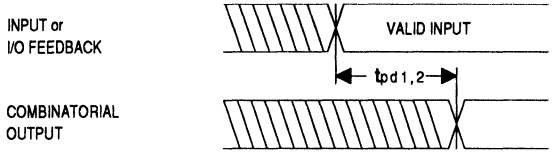
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

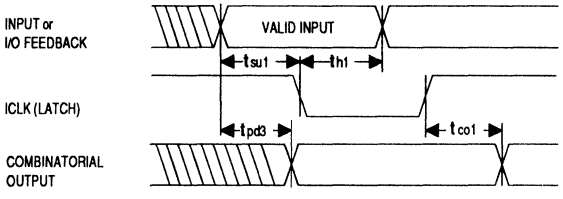
PARAMETER	TEST COND[1].	DESCRIPTION	-30		-35		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd1}	1	Combinatorial Input to Combinatorial Output	—	30	—	35	ns
t_{pd2}	1	Feedback or I/O to Combinational Output	—	30	—	35	ns
t_{pd3}	1	Transparent Latch Input to Combinatorial Output	—	35	—	40	ns
t_{co1}	1	Input Latch ICLK↑ to Combinatorial Output Delay	—	35	—	40	ns
t_{co2}	1	Input Reg. ICLK↑ to Combinatorial Output Delay	—	35	—	40	ns
t_{co3}	1	Output D/E Reg. OCLK↑ to Output Delay	—	12	—	13.5	ns
t_{co4}	1	Output D Reg. Sum Term CLK↑ to Output Delay	—	35	—	40	ns
t_{su1}	—	Setup Time, Input before Input Latch ICLK↓	2.5	—	3.5	—	ns
t_{su2}	—	Setup Time, Input before Input Reg. ICLK↑	2.5	—	3.5	—	ns
t_{su3}	—	Setup Time, Input or Feedback before D/E Reg. OCLK↑	25	—	30	—	ns
t_{su4}	—	Setup Time, Input or Feedback before D Reg. Sum Term CLK↑	7.5	—	10	—	ns
t_{su5}	—	Setup Time, Input Reg. ICLK↑ before D/E Reg. OCLK↑	30	—	35	—	ns
t_{su6}	—	Setup Time, Input Reg. ICLK↑ before D Reg. Sum Term CLK↑	15	—	17	—	ns
t_{h1}	—	Hold Time, Input after Input Latch ICLK↓	5	—	5	—	ns
t_{h2}	—	Hold Time, Input after Input Reg. ICLK↑	5	—	5	—	ns
t_{h3}	—	Hold Time, Input or Feedback after D/E Reg. OCLK↑	-5	—	-5	—	ns
t_{h4}	—	Hold Time, Input or Feedback after D Reg. Sum Term CLK↑	10	—	12.5	—	ns
f_{max}	—	Maximum Clock Frequency, OCLK	27	—	22.9	—	MHz
t_{wh1}[2]	—	ICLK or OCLK Pulse Duration, High	10	—	10	—	ns
t_{wh2}[2]	—	Sum Term CLK Pulse Duration, High	15	—	15	—	ns
t_{wl1}[2]	—	ICLK or OCLK Pulse Duration, Low	10	—	10	—	ns
t_{wl2}[2]	—	Sum Term CLK Pulse Duration, Low	15	—	15	—	ns
t_{arw}	—	Reset Pulse Duration	15	—	15	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	25	—	30	ns
t_{dis}	3	Input or I/O to Output Disabled	—	25	—	30	ns
t_{ar}	1	Input or I/O to Asynchronous Reg. Reset	—	35	—	35	ns
t_{arr1}	—	Asynchronous Reset to OCLK Recovery Time	20	—	20	—	ns
t_{arr2}	—	Asynchronous Reset to Sum Term CLK Recovery Time	10	—	10	—	ns

1) Refer to **Switching Test Conditions** section.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

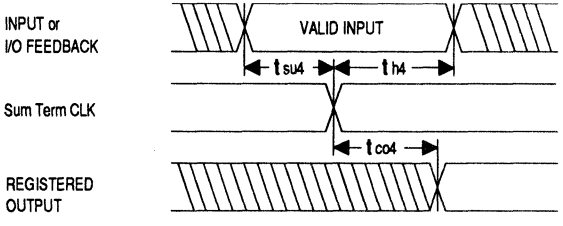
SWITCHING WAVEFORMS



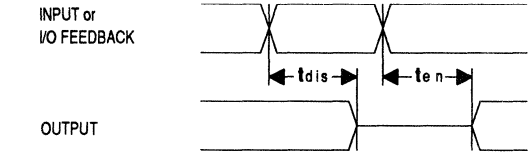
Combinatorial Output



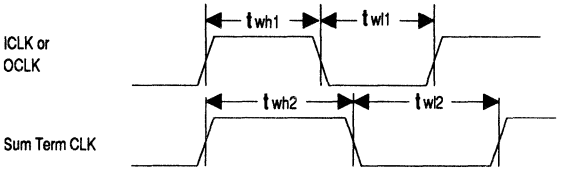
Latched Input



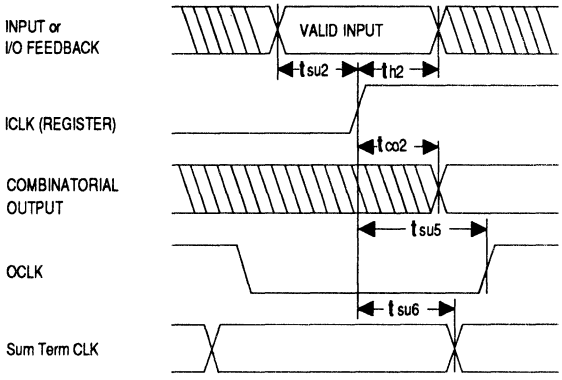
Registered Output (Sum Term CLK)



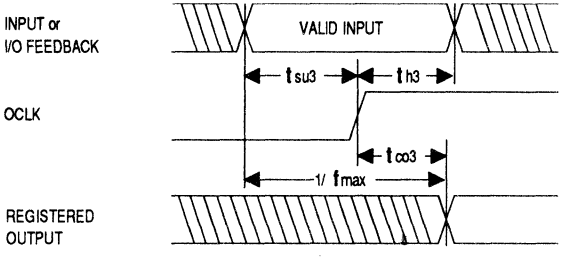
Input or I/O to Output Enable/Disable



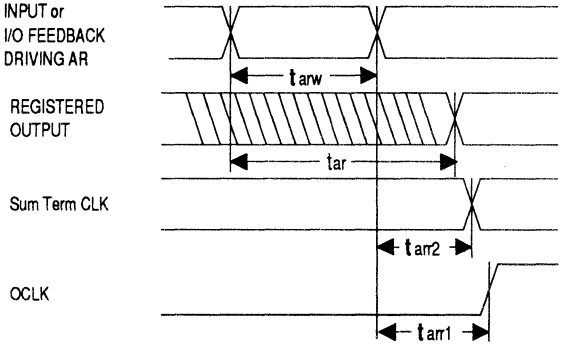
Clock Width



Registered Input



Registered Output (OCLK)



Asynchronous Reset

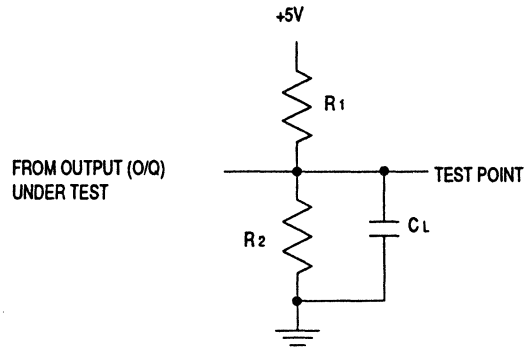
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		300Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ARRAY DESCRIPTION

The GAL6001 contains two E^2 reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complement forms). 64 product terms serve as inputs to the OR array. The RESET product term generates the RESET signal described in the Output and Buried Logic Macrocells section. There are 10 output enable product terms which allow device pins 14-23 to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE WORD

An electronic signature (ES) is provided with every GAL6001 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

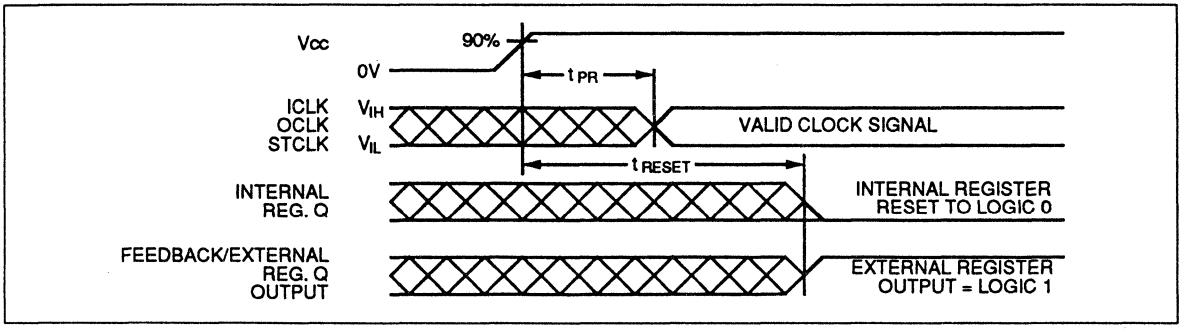
GAL6001 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL6001 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6001. First, the Vcc rise must be monotonic. Second, the clock inputs must become a proper TTL level within the specified time (t_{PR}, 100µs). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

$$DPTS = \left| (P\text{-}Terms)_{LH} - (P\text{-}Terms)_{HL} \right|$$

DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

A software utility is available from Lattice Applications Engineering that will perform this calculation on any GAL6001 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice representative or by contacting Lattice Applications Engineering Dept. (Tel: 503-681-0118 or 800-FASTGAL; FAX: 681-3037).

ispGAL16Z8

In-System Programmable High Performance E²CMOS PLD

2

FEATURES

IN-SYSTEM-PROGRAMMABLE — 5-VOLT ONLY
- **Change Logic "On The Fly" in Seconds**
- **Non-volatile E² Technology**

MINIMUM 10,000 ERASE/WRITE CYCLES

DIAGNOSTIC MODE FOR CONTROLLING AND OBSERVING SYSTEM LOGIC

HIGH PERFORMANCE E²CMOS® TECHNOLOGY
- **20 ns Maximum Propagation Delay**
- **Fmax = 41.6 MHz**
- **90 mA MAX Icc**

E² CELL TECHNOLOGY
- **100% Tested/Guaranteed 100% Yields**
- **20 Year Data Retention**

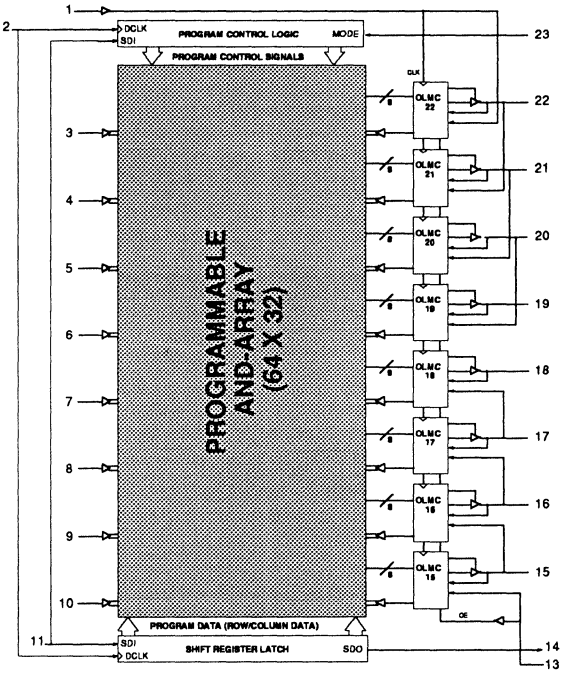
EIGHT OUTPUT LOGIC MACROCELLS
- **Maximum Flexibility for Complex Logic Designs**
- **Programmable Output Polarity**
- **Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**

PRELOAD AND POWER-ON RESET OF REGISTERS
- **100% Functional Testability**

APPLICATIONS INCLUDE:
- **Reconfigurable Interfaces and Decoders**
- **"Soft" Hardware (Generic Systems)**
- **Copy Protection and Security Schemes**
- **Reconfiguring Systems for Testing**

ELECTRONIC SIGNATURE FOR IDENTIFICATION

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

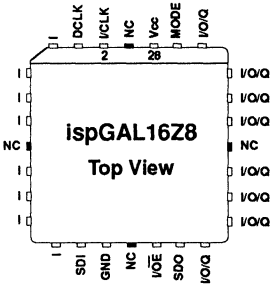
The Lattice ispGAL® 16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system programmability and in-system diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage programming signals. Using Lattice's proprietary UltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin ispGAL16Z8 is architecturally and parametrically identical to the 20-pin GAL16V8, but includes 4 extra pins to control in-system programming. These pins are not associated with normal logic functions and are used only during programming and diagnostic operations. This 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

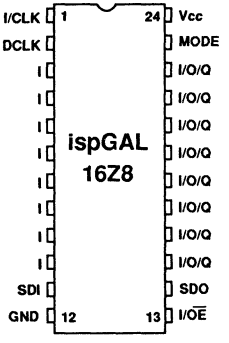
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products.

PIN CONFIGURATION

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

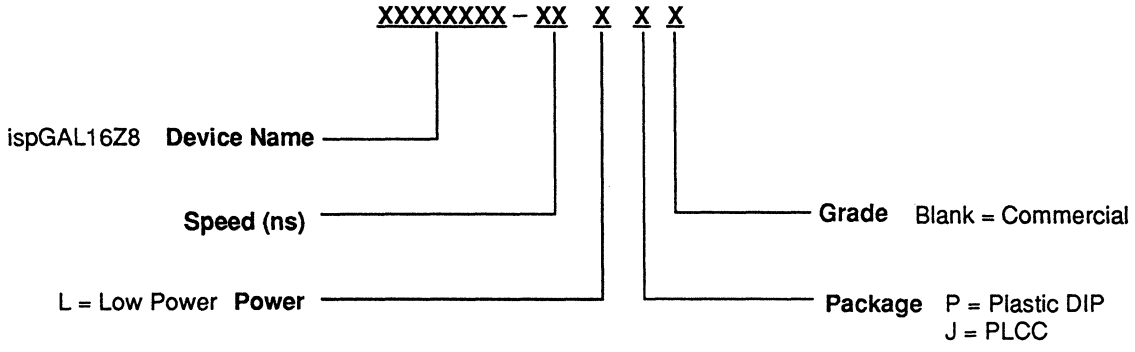
April 1991.Rev.A

ispGAL16Z8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	15	15	90	ispGAL16Z8-20LP	24-Pin Plastic DIP
			90	ispGAL16Z8-20LJ	28-Lead PLCC
25	20	15	90	ispGAL16Z8-25LP	24-Pin Plastic DIP
			90	ispGAL16Z8-25LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells, the XOR bit of each macrocell controls the polarity of the output in any of the three modes, and the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in an ispGAL16Z8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8, and therefore the ispGAL16Z8, can emulate. It also shows the OLMC mode under which the ispGAL16Z8 emulates the PAL architecture.

PAL Architectures Emulated by ispGAL16Z8	ispGAL16Z8 Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

The ispGAL16Z8 can be treated as a GAL16V8, and tools are provided by Lattice to use GAL16V8 JEDEC files to program ispGAL16Z8 devices.

When using compiler software to configure the device, the user must pay special attention to the following restrictions:

In **registered mode** pin 1 and pin 13 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 18 and pin 19 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner-most pins (pins 18 and 19) will not have feedback, as these pins are always configured as dedicated combinatorial output. All macrocells are always either dedicated inputs or dedicated outputs in this mode.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8S	P16V8
CUPL	G16V8MS	G16V8MA	G16V8S	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

REGISTERED MODE

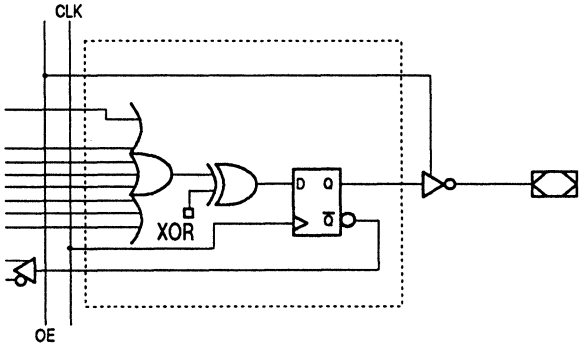
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

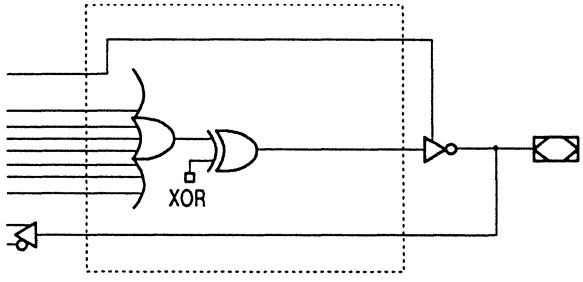
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 13 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 13 are permanently configured as CLK and $\overline{OE}$.



Combinatorial Configuration for Registered Mode

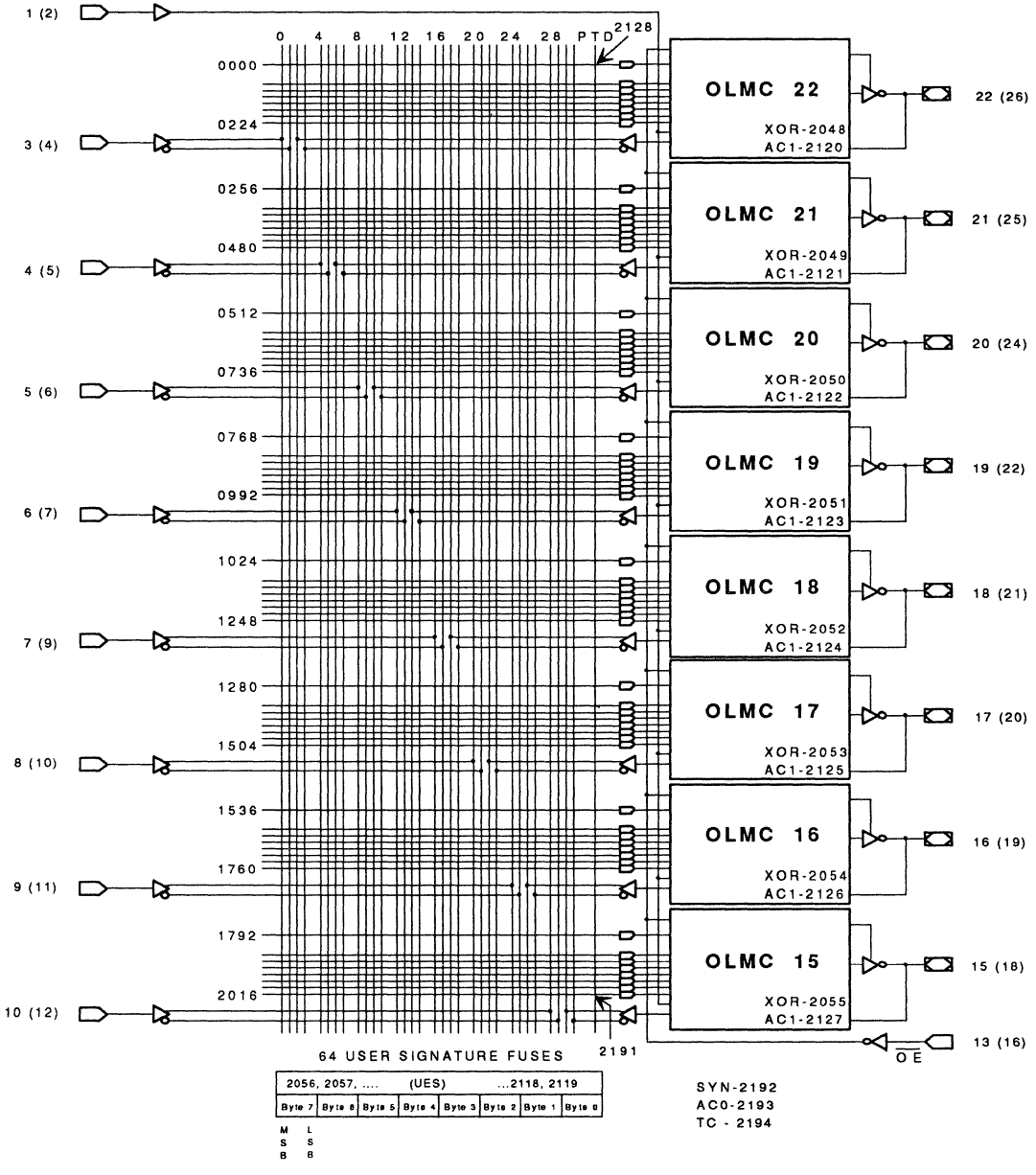
- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 13 are permanently configured as CLK and $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

2

DIP (PLCC) Package Pinouts



COMPLEX MODE

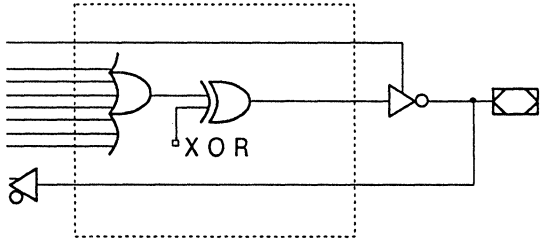
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

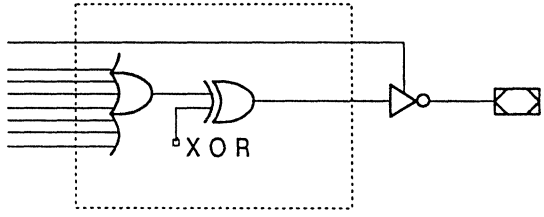
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pins 16 through Pin 21 are configured to this function.



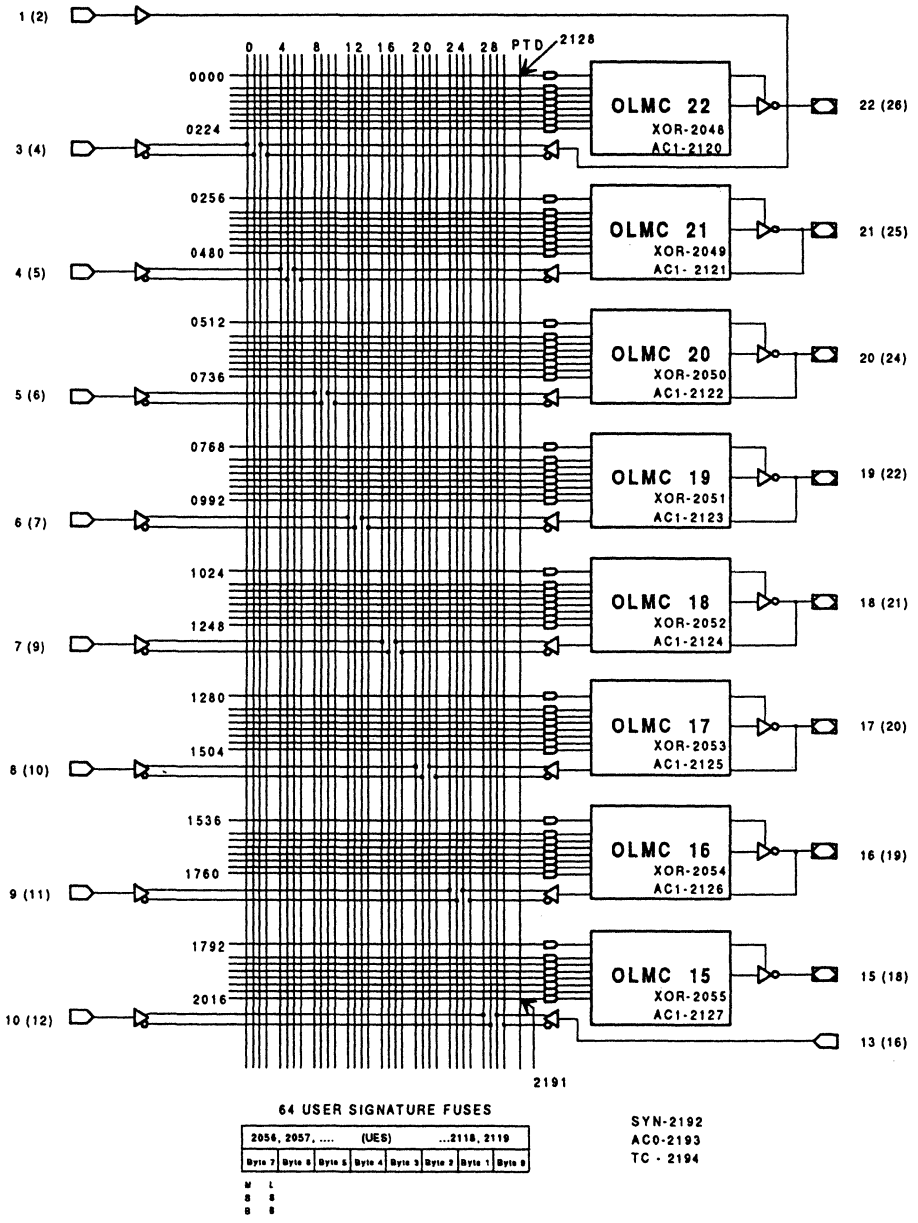
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pins 15 and Pin 22 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



SIMPLE MODE

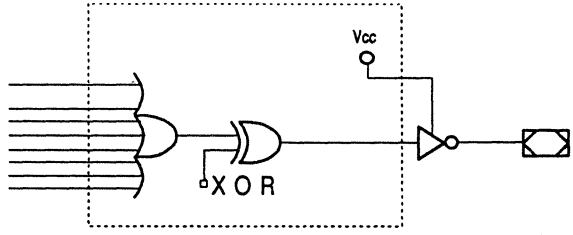
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

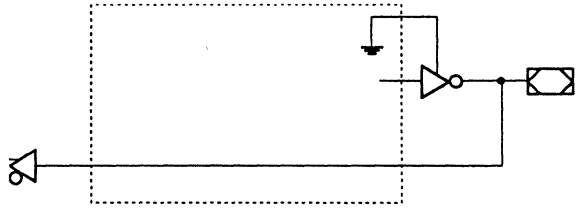
Pins 1 and 13 are always available as data inputs into the AND array. The center two macrocells (pins 18 & 19) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMCs can be configured to this configuration.
- Pins 18 & 19 are permanently configured to this function.



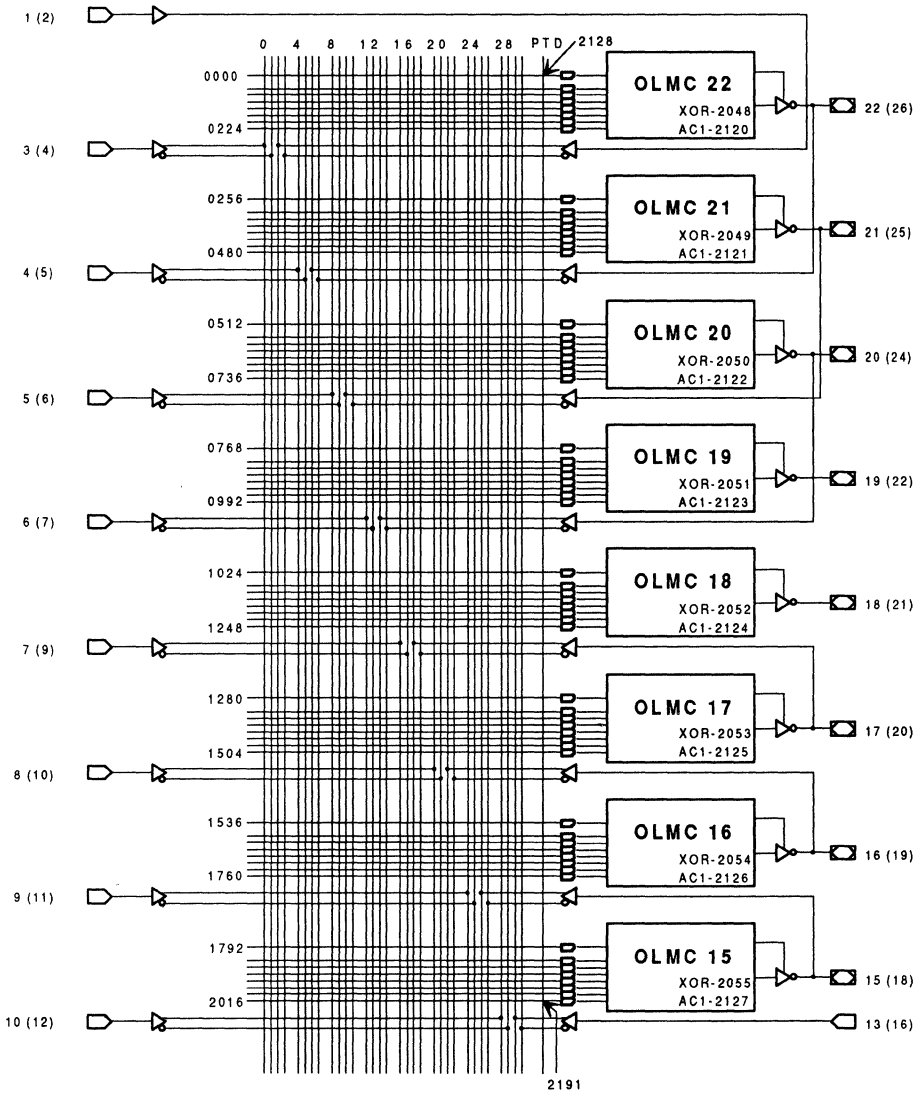
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMCs **except** pins 18 & 19 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64 USER SIGNATURE FUSES

2056, 2057, ... (UES) ...2118, 2119							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

MSB LSB

SYN-2192
AC0-2193
TC - 2194

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	Vcc = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	75	90	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	20	3	25	ns
t_{co}	1	Clock to Output Delay	2	15	2	15	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	15	—	20	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}[2]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	33.3	—	28.5	—	MHz
	1	Maximum Clock Frequency with No Feedback	41.6	—	33.3	—	MHz
t_{wh}[3]	—	Clock Pulse Duration, High	12	—	15	—	ns
t_{wl}[3]	—	Clock Pulse Duration, Low	12	—	15	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	—	25	ns
	2	OE↓ to Output Enabled	—	18	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	—	25	ns
	3	OE↑ to Output Disabled	—	18	—	20	ns

1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Description** section.
3) Clock pulses of widths less than the specification may be detected as valid clock signals.

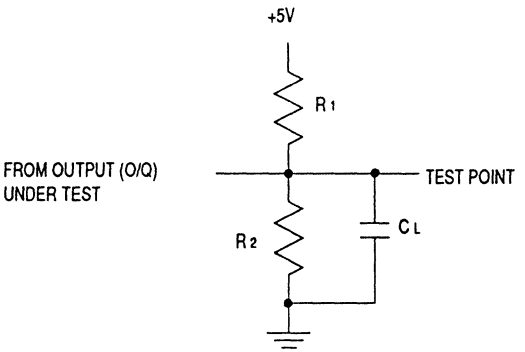
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

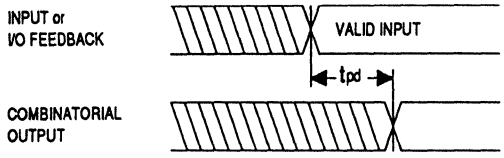
Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

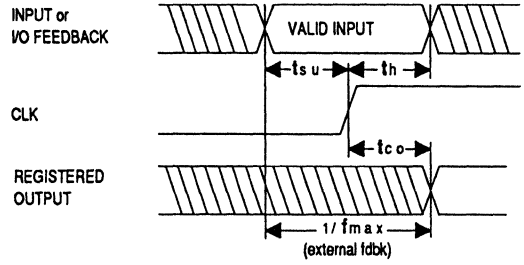


C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

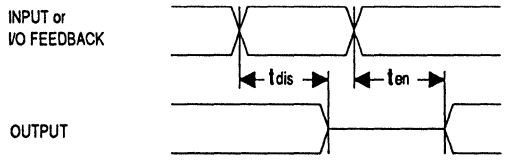
SWITCHING WAVEFORMS



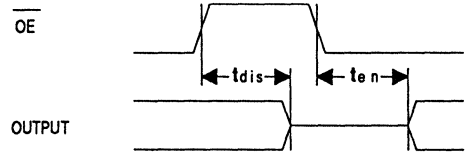
Combinatorial Output



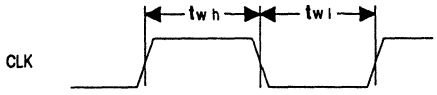
Registered Output



Input or I/O to Output Enable/Disable

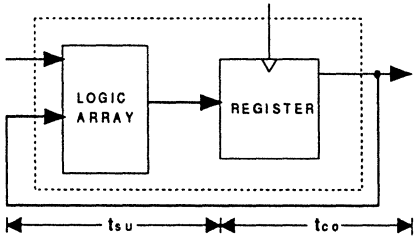


$\overline{OE}$ to Output Enable/Disable



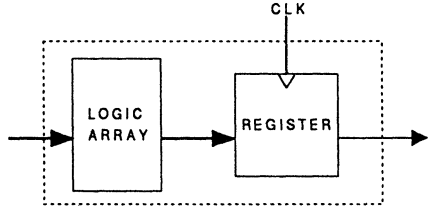
Clock Width

fmax DESCRIPTIONS



fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax With No Feedback

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided as part of the ispGAL16Z8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

The security cell is provided on the ispGAL16Z8 device to prevent unauthorized copying of the logic pattern. Once programmed, this cell prevents further read access to the functional bits in the device. The cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

LATCH-UP PROTECTION

The ispGAL16Z8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

TC CELL

The ispGAL16Z8 devices are equipped with a TC (Tri-State Control) cell which controls the state of the outputs when the device is being programmed. Since the device is programmed while on the circuit board, and connected to other devices, the state of the outputs is very important. Depending on how the TC cell is programmed, the outputs will either be tri-stated or latched upon entering the programming/diagnostic mode.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

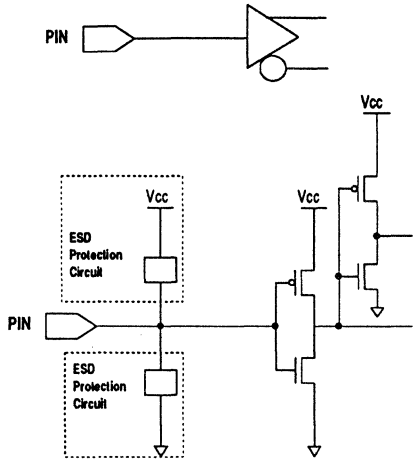
The ispGAL16Z8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any state condition can be forced for test sequencing.

INPUT BUFFERS

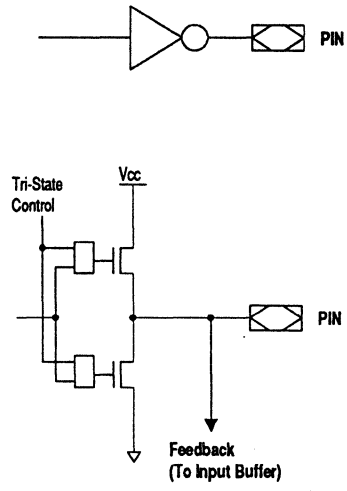
The ispGAL16Z8 devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load the driving logic much less than traditional bipolar devices. Because the inputs are connected to a CMOS gate, there is no inherent pull-up structure, as there is with bipolar devices. Therefore, they cannot be depended on to float high (or to any particular state), and must be tied to the desired logic state.

Unused inputs and tri-stated I/Os should not be left floating. Lattice recommends that they be connected to Vcc, Ground, or another driven input. Doing so will tend to increase noise immunity and reduce Icc for the device.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

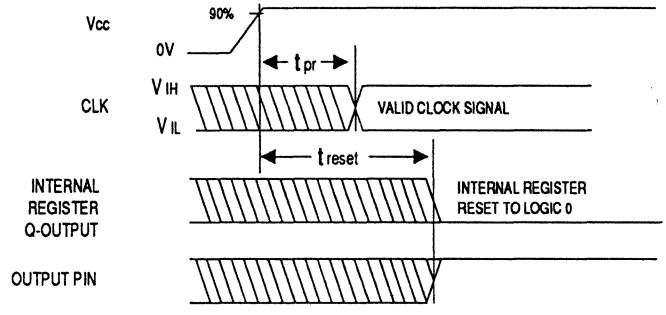


Input



Output

POWER-UP RESET



Circuitry within the ispGAL16Z8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

Section 1: Introduction to Generic Array Logic

Section 2: GAL Datasheets

Section 3: GAL Military Products

Section 4: Quality and Reliability

Section 5: Technical Notes

Section 6: Article Reprints

Section 7: General Information

Military Program Overview

CORPORATE PHILOSOPHY

Lattice Semiconductor is committed to leadership in performance and quality. Our family of military GAL devices is consistent with this philosophy. Lattice manufactures all devices under strict Quality Assurance guidelines. All grades, Commercial through Military 883C, are monitored under a quality program conformant to MIL-M-38510 Appendix A with inspections conformant to MIL-I-45208.

Lattice Semiconductor has been manufacturing GAL devices since 1984. The engineering analysis and characterization during this time has been focused into our current design, process and manufacturing test procedures to assure superior product which meet all datasheet and quality goals.

Complete review of the procedures and technical data can be arranged at our facility near Portland, Oregon. Factory audits of our documentation and processes are also welcomed.

QUALITY AND TESTABILITY

Lattice Semiconductor processes its GAL devices to strict conformance with MIL-STD-883C Class B. In conjunction with the military flow, the inherent testability of E^2CMOS technology allows Lattice to achieve a quality level superior to other PLD technologies.

All GAL devices are patterned and tested dozens of times throughout the manufacturing flow. Every GAL device is tested under worst case configurations to assure customers achieve 100% yields. Tests are performed using the same E^2 cell array that will be used for the final patterning of the devices. This 100% "actual test" philosophy does away with the correlated and simulated testing that is necessary with bipolar and UV (EPROM) based PLD devices.

RELIABILITY

Lattice Semiconductor performs extensive reliability testing prior to product release. This testing continues in the form of Reliability Monitors that are run on an ongoing basis to assure continued process integrity. A formal, written report of these test results is updated regularly and can be obtained from your local Lattice Sales Representative.

The reliability testing performed includes extensive analysis of fundamental design and process integrity. The reprogrammable nature of GAL devices allows for an inherently more thorough reliability evaluation than other programmable alternatives.

MIL–STD–883C COMPLIANCE

MIL–STD–883C provides a uniform and precise method for environmental, mechanical and electrical testing which ensures the suitability of microelectronic devices for use in military and aerospace systems. Table I summarizes the MIL–STD–883C, Class B flow. Table II summarizes the conformance testing required by MIL-STD-883C, Method 5005, for quality conformance testing of Lattice military microcircuits.

MIL-M-38510

MIL–M–38510, when used in conjunction with MIL–STD–883C, defines design, packaging, material, marking, sampling, qualification and quality system requirements for military devices.

GROUP DATA

Group A and B data is taken on every inspection lot per MIL-STD-883C, Class B requirements. This data, along with Generic Group C and D data can be supplied, upon written request, with your device shipment. Your Lattice sales representative can advise you of charges and leadtime necessary for providing this data.

STANDARD MILITARY DRAWINGS

Lattice actively supports the DESC Standard Military Drawing (SMD) Program. The SMD Program offers a cost effective alternative to source control drawings and provides standardized MIL-STD-883C product specifications to simplify military procurement.

Lattice recognizes the growing demand for SMD qualified devices, and in response, all new 883C product released by Lattice will be submitted to DESC for SMD qualification. Customers may facilitate this process by submitting a "Nonstandard Part Approval Request", DD Form 2052, to DESC. This form allows you to recommend to DESC the qualification of Lattice devices to SMD status.

A list of currently available SMD qualified devices is provided (see Military Ordering Information). Contact your local Lattice sales representative for the latest status of SMD qualifications in process with DESC.

MILITARY SCREENING FLOW (TABLE I)

Screen	Method	Requirement
Internal Visual	2010 Cond. B	100%
Temp. Cycling	1010 Cond. C	100%
Constant Acceleration	2001 Cond. E	100%
Hermeticity Fine Gross	1014 Cond. A or B Cond. C	100%
Endurance Test	1033	100%
Retention Test	Unbiased Bake 48 HRS. T_A = 150°C	100%
Pre Burn-In Electrical	Applicable Device Specification Tc = 25°C	100%
Dynamic Burn-In	1015 Cond. D	100%
Post Burn-In Electrical	Applicable Device Specification Tc = 25°C PDA = 5%	100%
Final Electrical Test	Applicable Device Specification Tc = 125°C	100%
Final Electrical Test	Applicable Device Specification Tc = - 55°C	100%
External Visual	2009	100%
QCI Sample Selection	MIL-M-38510H Sec. 4.5 and MIL-STD-883C Sec. 1.2	Sample

MILITARY QUALITY CONFORMANCE INSPECTIONS (TABLE II)

Subgroup	Method	Sample
GROUP A: Electrical Tests		
Subgroups 1, 7, 9 Electrical Test	Applicable Device Spec. 25°C	LTPD = 2
Subgroups 2, 8A, 10 Electrical Test	Applicable Device Spec. Max. Operating Temp.	LTPD = 2
Subgroups 3, 8B, 11 Electrical Test	Applicable Device Spec. Min. Operating Temp.	LTPD = 2
GROUP B: Mechanical Tests		
Subgroup 2 Solvent Resistance	2015	4(0)
Subgroup 3 Solderability	2003	LTPD = 10
Subgroup 5 Bond Strength	2011	LTPD = 15
GROUP C: Chip Integrity Tests		
Subgroup 1 Dynamic Life Test End Point Electrical	1005, 1,000 HRS. 125°C Applicable Device Spec.	LTPD = 5
Subgroup 2 Unbiased Retention End Point Electrical	1,000 HRS. 150°C Applicable Device Spec.	LTPD = 5
GROUP D: Environmental Integrity		
Subgroup 1 Physical Dimensions	2016	LTPD = 15
Subgroup 2 Lead Integrity Hermeticity	2004, Cond. B 1014	LTPD = 5
Subgroup 3 Thermal Shock Temp. Cycle Moisture Resistance Hermeticity Visual Examination Endpoint Electrical	1011, Cond. B, 15 Cycles 1010, Cond. C, 100 Cycles 1004 1014 1004, 1010 Applicable Device Spec.	LTPD = 15
Subgroup 4 Mechanical Shock Vibration Constant Acceleration Hermeticity Visual Examination Endpoint Electrical	2002, Cond. B 2007, Cond. A 2001, Cond. E 1014 1010, 1011 Applicable Device Spec.	LTPD = 15
Subgroup 5 Salt Atmosphere Hermeticity Visual Examination	1009, Cond. A 1014 1009	LTPD = 15
Subgroup 6 Internal Water Vapor	1018 < 5,000 PPM, 100°C	3(0)
Subgroup 7 Lead Finish Adhesion	2025	LTPD = 15
Subgroup 8 Lid Torque	2024	5(0)

Military Ordering Information

Lattice offers the most comprehensive line of military E²CMOS Programmable Logic Devices. Lattice recognizes the trend in military device procurement towards using SMD compliant devices and encourages customers to use the SMD number, where it exists, when ordering parts. Listed below are Lattice's military qualified devices and their corresponding SMD numbers. Please contact your local Lattice representative for the latest product listing.

Military Products Selector Guide

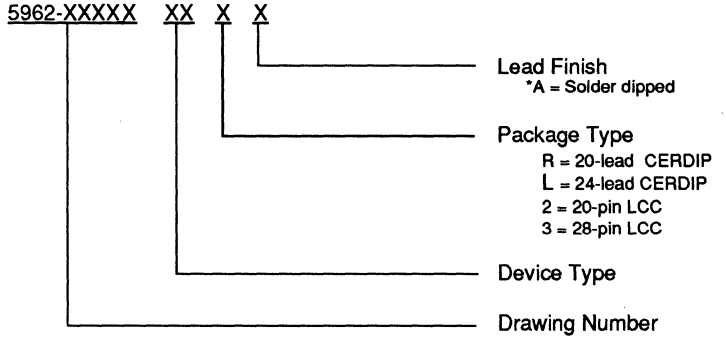
DEVICE TYPE	Tpd (ns)	Icc (mA)	PACKAGE	LATTICE PART #	SMD #
GAL16V8	10	130	20-Pin CERDIP	GAL16V8B-10LD/883C	5962-8983904RA
		130	20-Pin LCC	GAL16V8B-10LR/883C	5962-89839042A
	15	130	20-Pin CERDIP	GAL16V8A-15LD/883C	5962-8983903RA
		130	20-Pin LCC	GAL16V8A-15LR/883C	5962-89839032A
	20	65	20-Pin CERDIP	GAL16V8A-20QD/883C	5962-8983906RA
		65	20-Pin LCC	GAL16V8A-20QR/883C	5962-89839062A
		130	20-Pin CERDIP	GAL16V8A-20LD/883C	5962-8983902RA
		130	20-Pin LCC	GAL16V8A-20LR/883C	5962-89839022A
	25	65	20-Pin CERDIP	GAL16V8A-25QD/883C	5962-8983905RA
		65	20-Pin LCC	GAL16V8A-25QR/883C	5962-89839052A
	30	130	20-Pin CERDIP	GAL16V8A-30LD/883C	5962-8983901RA
		130	20-Pin LCC	GAL16V8A-30LR/883C	5962-89839012A
GAL20V8	15	130	24-Pin CERDIP	GAL20V8A-15LD/883C	5962-8984003LA
		130	28-Pin LCC	GAL20V8A-15LR/883C	5962-89840033A
	20	65	24-Pin CERDIP	GAL20V8A-20QD/883C	Contact Factory
		65	28-Pin LCC	GAL20V8A-20QR/883C	Contact Factory
		130	24-Pin CERDIP	GAL20V8A-20LD/883C	5962-8984002LA
		130	28-Pin LCC	GAL20V8A-20LR/883C	5962-89840023A
	25	65	24-Pin CERDIP	GAL20V8A-25QD/883C	Contact Factory
		65	28-Pin LCC	GAL20V8A-25QR/883C	Contact Factory
	30	130	24-Pin CERDIP	GAL20V8A-30LD/883C	5962-8984001LA
		130	28-Pin LCC	GAL20V8A-30LR/883C	5962-89840013A
GAL22V10	15	150	24-Pin CERDIP	GAL22V10B-15LD/883C	5962-8984103LA
		150	28-Pin LCC	GAL22V10B-15LR/883C	5962-89841033A
	20	150	24-Pin CERDIP	GAL22V10-20LD/883C	5962-8984102LA
		150	28-Pin LCC	GAL22V10-20LR/883C	5962-89841023A
	25	150	24-Pin CERDIP	GAL22V10-25LD/883C	5962-8984104LA
		150	28-Pin LCC	GAL22V10-25LR/883C	5962-89841043A
	30	150	24-Pin CERDIP	GAL22V10-30LD/883C	5962-8984101LA
		150	28-Pin LCC	GAL22V10-30LR/883C	5962-89841013A
GAL20RA10	20	120	24-Pin CERDIP	GAL20RA10-20LD/883C	Contact Factory
		120	28-Pin LCC	GAL20RA10-20LR/883C	Contact Factory
	25	120	24-Pin CERDIP	GAL20RA10-25LD/883C	Contact Factory
		120	28-Pin LCC	GAL20RA10-25LR/883C	Contact Factory

DESC Standard Military Drawing Listing

SMD #	LATTICE PART #
5962-89839012A	GAL16V8A-30LR/883C
5962-8983901RA	GAL16V8A-30LD/883C
5962-89839022A	GAL16V8A-20LR/883C
5962-8983902RA	GAL16V8A-20LD/883C
5962-89839032A	GAL16V8A-15LR/883C
5962-8983903RA	GAL16V8A-15LD/883C
5962-89839042A	GAL16V8B-10LR/883C
5962-8983904RA	GAL16V8B-10LD/883C
5962-89839052A	GAL16V8A-25QR/883C
5962-8983905RA	GAL16V8A-25QD/883C
5962-89839062A	GAL16V8A-20QR/883C
5962-8983906RA	GAL16V8A-20QD/883C
5962-89840013A	GAL20V8A-30LR/883C

SMD #	LATTICE PART #
5962-8984001LA	GAL20V8A-30LD/883C
5962-89840023A	GAL20V8A-20LR/883C
5962-8984002LA	GAL20V8A-20LD/883C
5962-89840033A	GAL20V8A-15LR/883C
5962-8984003LA	GAL20V8A-15LD/883C
5962-89841013A	GAL22V10-30LR/883C
5962-8984101LA	GAL22V10-30LD/883C
5962-89841023A	GAL22V10-20LR/883C
5962-8984102LA	GAL22V10-20LD/883C
5962-89841033A	GAL22V10B-15LR/883C
5962-8984103LA	GAL22V10B-15LD/883C
5962-89841043A	GAL22V10-25LR/883C
5962-8984104LA	GAL22V10-25LD/883C

Standard Military Drawing Number Description



* no other lead finish currently available.

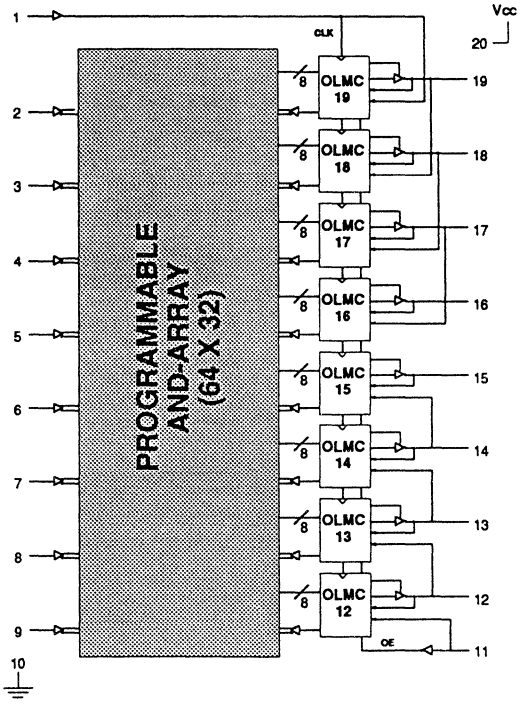
GAL16V8B/883C
GAL16V8A/883C

High Performance E²CMOS PLD

FEATURES

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 10 ns Maximum Propagation Delay
  - Fmax = 62.5 MHz
  - 7 ns Maximum from Clock Input to Data Output
  - TTL Compatible 24 mA Outputs
  - UltraMOS® Advanced CMOS Technology
- 50% to 75% REDUCTION IN POWER FROM BIPOLAR
  - 75mA Typ Icc on Low Power Device
  - 45mA Typ Icc on Quarter Power Device
- ACTIVE PULL-UPS ON ALL PINS (GAL16V8B)
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

FUNCTIONAL BLOCK DIAGRAM



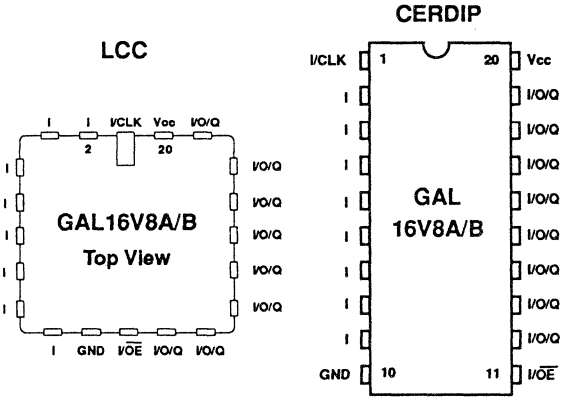
DESCRIPTION

The GAL16V8B/883C and GAL16V8A/883C are high performance E²CMOS programmable logic devices processed in full compliance to MIL-STD-883C. These military grade devices combine a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed/power performance available in the 883C qualified PLD market. The GAL16V8B/883C, at 10ns maximum propagation delay time, is the world's fastest military qualified CMOS PLD. CMOS circuitry allows the GAL16V8A quarter power devices to consume just 45mA typical Icc, which represents a 75% savings in power when compared to bipolar counterparts.

Generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL16V8A/883C and GAL16V8B/883C are capable of emulating all standard 20-pin PAL® devices with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

PIN CONFIGURATION



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503)681-3037

April 1991.Rev.A

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{cc} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{cc} +1.0V
Off-state output voltage applied .....–2.5 to V_{cc} +1.0V
Storage Temperature .....–65 to 150°C
Case Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_c) .....–55 to 125°C
Supply voltage (V_{cc})
with Respect to Ground .....+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le Vcc$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	–2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25 MHz Outputs Open (no load)	—	75	130	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-10		UNITS
			MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	2	10	ns
tco	1	Clock to Output Delay	1	7	ns
tcf[2]	—	Clock to Feedback Delay	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	58.8	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	ns
ten	2	Input or I/O to Output	—	10	ns
	2	OE↓ to Output	—	10	ns
tdis	3	Input or I/O to Output	—	10	ns
	3	OE↑ to Output	—	10	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

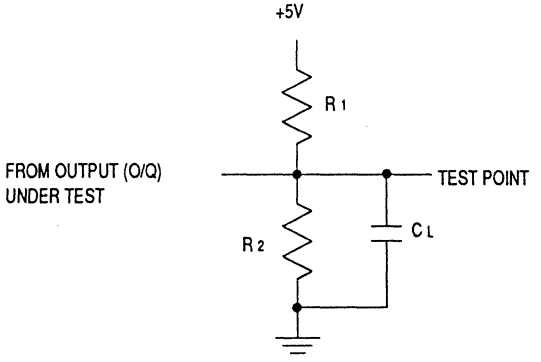
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		390Ω	750Ω	50pF
2	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
3	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Case Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) ..... –55 to 125°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	–2.0	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V	L -15/-20/-30	—	75	130	mA
		Outputs Open (no load) f_{toggle} = 25MHz	Q -20/-25	—	45	65	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-15		-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	15	3	20	3	25	3	30	ns
tco	1	Clock to Output Delay	2	12	2	15	2	15	2	20	ns
tcf[2]	—	Clock to Feedback Delay	—	12	—	15	—	15	—	20	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	12	—	15	—	20	—	25	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with No Feedback	50	—	41.6	—	33.3	—	33.3	—	MHz
twh[4]	—	Clock Pulse Duration, High	10	—	12	—	15	—	15	—	ns
twl[4]	—	Clock Pulse Duration, Low	10	—	12	—	15	—	15	—	ns
ten	2	Input or I/O to Output	—	15	—	20	—	25	—	30	ns
	2	OE↓ to Output	—	15	—	18	—	20	—	25	ns
tdis	3	Input or I/O to Output	—	15	—	20	—	25	—	30	ns
	3	OE↑ to Output	—	15	—	18	—	20	—	25	ns

) Refer to **Switching Test Conditions** section.
) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
) Refer to **fmax Descriptions** section.
) Clock pulses of widths less than the specification may be detected as valid clock signals.

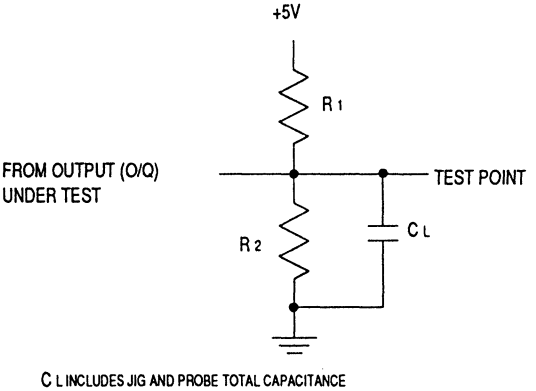
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

-state levels are measured 0.5V from steady-state active vel.

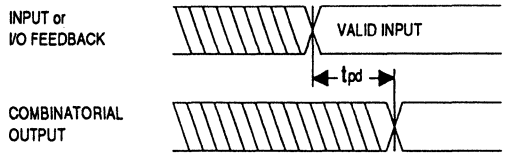
utput Load Conditions (see figure)

Test Condition		R1	R2	CL
1		390Ω	750Ω	50pF
2	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
3	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF

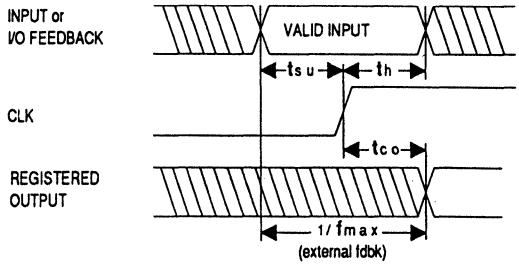


C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

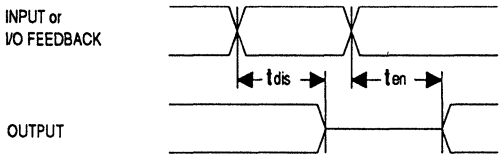
SWITCHING WAVEFORMS



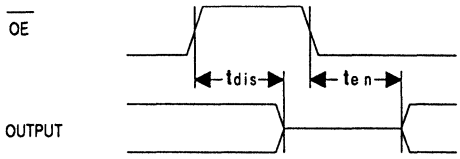
Combinatorial Output



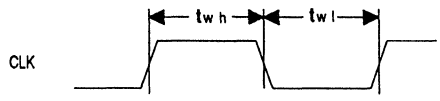
Registered Output



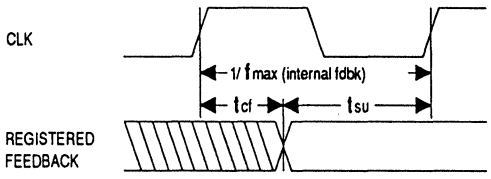
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

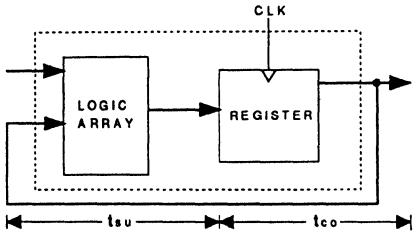


Clock Width



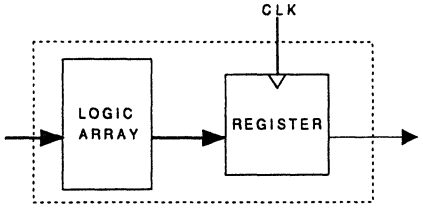
fmax with Feedback

fmax DESCRIPTIONS



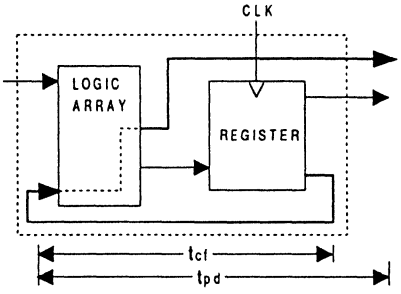
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax Without Feedback

Note: fmax with no feedback may be less than 1/twh + twl this is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/ internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

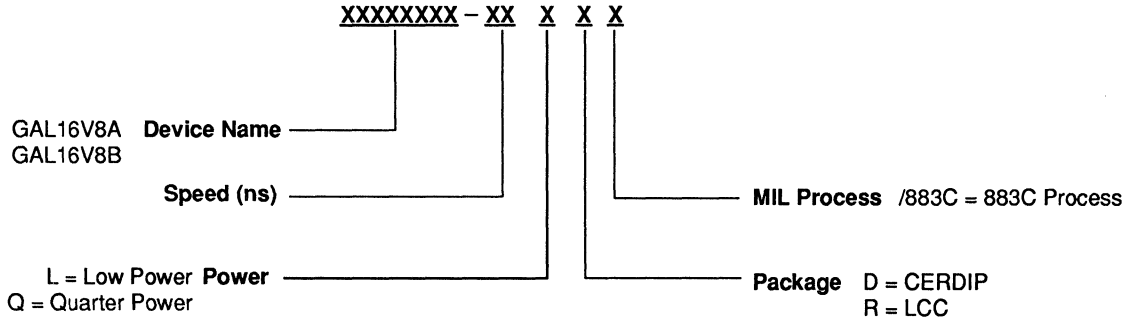
3

GAL16V8A/B ORDERING INFORMATION (MIL-STD-883C and SMD)

					Ordering #	
Tpd (ns)	**Tsu (ns)**	**Tco (ns)**	**Icc (mA)**	**Package**	**MIL-STD-883C**	**SMD #**
10	10	7	130	20-Pin CERDIP	GAL16V8B-10LD/883C	5962-8983904RA
			130	20-Pin LCC	GAL16V8B-10LR/883C	5962-89839042A
15	12	12	130	20-Pin CERDIP	GAL16V8A-15LD/883C	5962-8983903RA
			130	20-Pin LCC	GAL16V8A-15LR/883C	5962-89839032A
20	15	15	65	20-Pin CERDIP	GAL16V8A-20QD/883C	5962-8983906RA
			65	20-Pin LCC	GAL16V8A-20QR/883C	5962-89839062A
			130	20-Pin CERDIP	GAL16V8A-20LD/883C	5962-8983902RA
			130	20-Pin LCC	GAL16V8A-20LR/883C	5962-89839022A
25	20	15	65	20-Pin CERDIP	GAL16V8A-25QD/883C	5962-8983905RA
			65	20-Pin LCC	GAL16V8A-25QR/883C	5962-89839052A
30	25	20	130	20-Pin CERDIP	GAL16V8A-30LD/883C	5962-8983901RA
			130	20-Pin LCC	GAL16V8A-30LR/883C	5962-89839012A

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

PART NUMBER DESCRIPTION



GAL20V8A/883C

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 15 ns Maximum Propagation Delay
  - Fmax = 50 MHz
  - 12 ns Maximum from Clock Input to Data Output
  - TTL Compatible 24 mA Outputs
  - UltraMOS® Advanced CMOS Technology
- 50% to 75% REDUCTION IN POWER FROM BIPOLAR
  - 75mA Typ I_{cc} on Low Power Device
  - 45mA Typ I_{cc} on Quarter Power Device
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<50ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

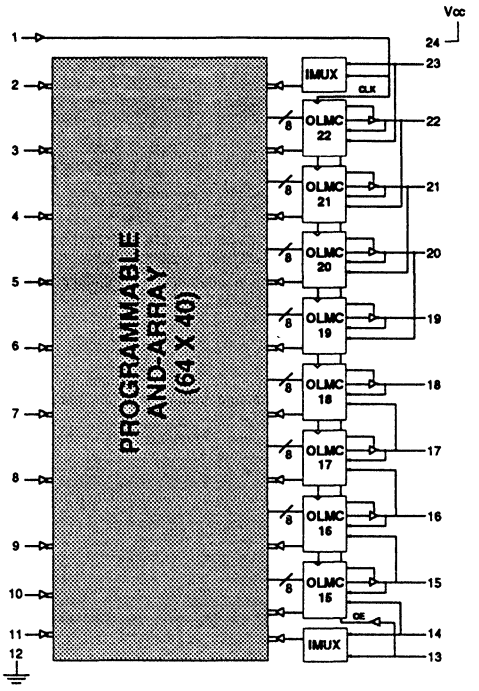
DESCRIPTION

The GAL20V8A/883C is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883C. The GAL20V8A/883C, at 15ns maximum propagation delay time, is the world's fastest military qualified 24-pin CMOS PLD. CMOS circuitry allows the GAL20V8A quarter power device to consume just 45mA typical Icc, which represents a 75% savings in power when compared to bipolar counterparts.

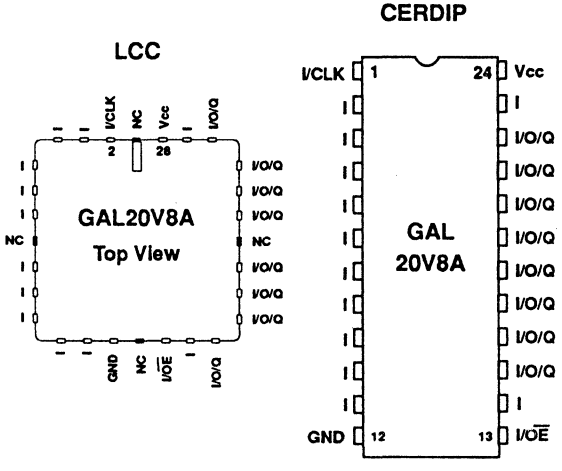
Generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20V8A/883C is capable of emulating all standard 24-pin PAL® devices with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

April 1991.Rev.A

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{cc} .....–0.5 to +7V
Input voltage applied.....–2.5 to V_{cc} +1.0V
Off-state output voltage applied .....–2.5 to V_{cc} +1.0V
Storage Temperature .....–65 to 150°C
Case Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) .....–55 to 125°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	–2.0	mA
I_{OS}[1]	Output Short Circuit Current	Vcc = 5V Vout = 0.5V T_A = 25°C		–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V	L -15/-20/-30	—	75	130	mA
		Outputs Open (no load) f_{toggle} = 25MHz	Q -20/-25	—	45	65	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-15		-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	15	3	20	3	25	3	30	ns
tco	1	Clock to Output Delay	2	12	2	15	2	15	2	20	ns
tcf[2]	—	Clock to Feedback Delay	—	12	—	15	—	15	—	20	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	12	—	15	—	20	—	25	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with No Feedback	50	—	41.6	—	33.3	—	33.3	—	MHz
twh[4]	—	Clock Pulse Duration, High	10	—	12	—	15	—	15	—	ns
twl[4]	—	Clock Pulse Duration, Low	10	—	12	—	15	—	15	—	ns
ten	2	Input or I/O to Output	—	15	—	20	—	25	—	30	ns
	2	OE↓ to Output	—	15	—	18	—	20	—	25	ns
tdis	3	Input or I/O to Output	—	15	—	20	—	25	—	30	ns
	3	OE↑ to Output	—	15	—	18	—	20	—	25	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

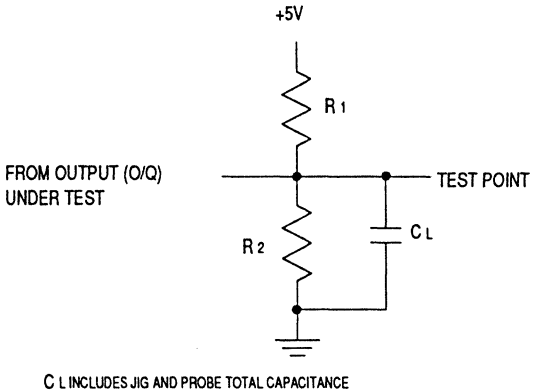
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

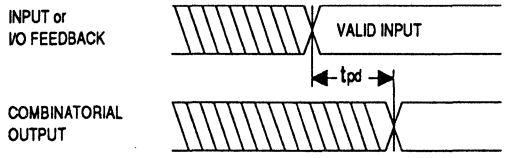
Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		390Ω	750Ω	50pF
2	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
3	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF

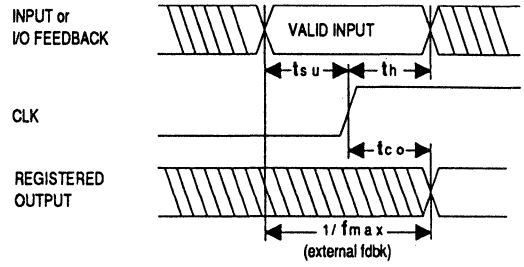


C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

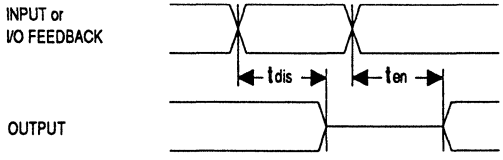
SWITCHING WAVEFORMS



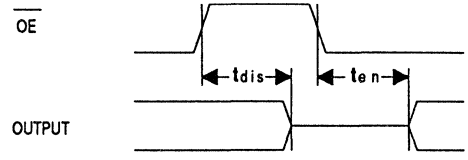
Combinatorial Output



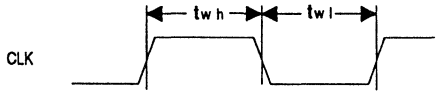
Registered Output



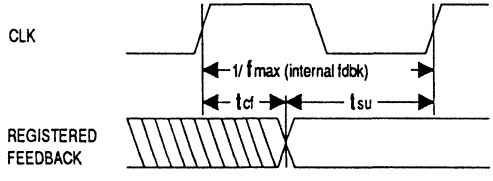
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

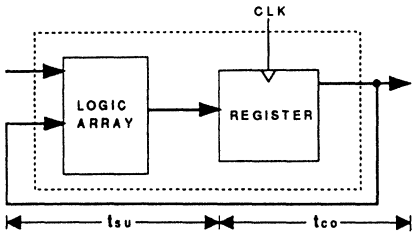


Clock Width



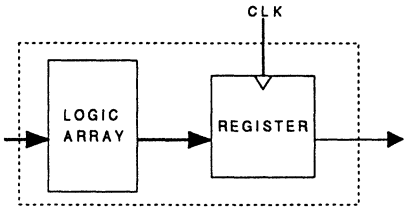
fmax with Feedback

fmax DESCRIPTIONS



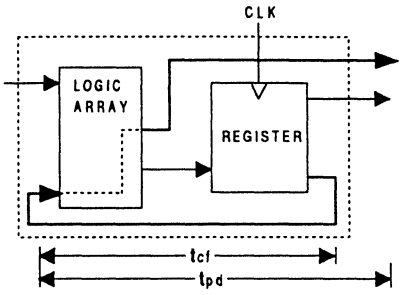
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax Without Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

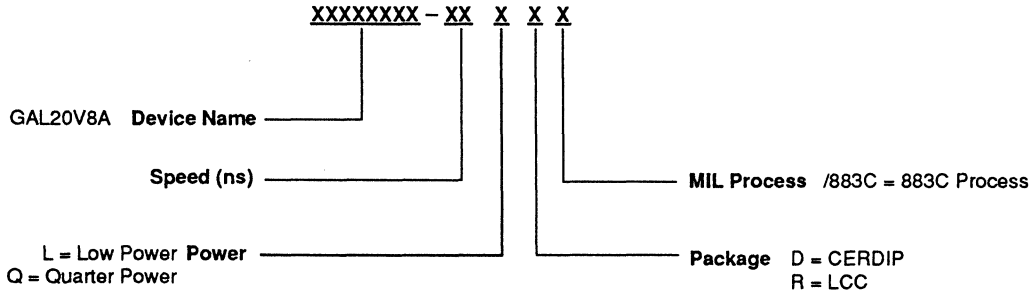
3

GAL20V8A ORDERING INFORMATION (MIL-STD-883C and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering # MIL-STD-883C	Ordering # SMD #
15	12	12	130	24-Pin CERDIP	GAL20V8A-15LD/883C	5962-8984003LA
			130	28-Pin LCC	GAL20V8A-15LR/883C	5962-89840033A
20	15	15	65	24-Pin CERDIP	GAL20V8A-20QD/883C	Contact Factory
			65	28-Pin LCC	GAL20V8A-20QR/883C	Contact Factory
			130	24-Pin CERDIP	GAL20V8A-20LD/883C	5962-8984002LA
			130	28-Pin LCC	GAL20V8A-20LR/883C	5962-89840023A
25	20	15	65	24-Pin CERDIP	GAL20V8A-25QD/883C	Contact Factory
			65	28-Pin LCC	GAL20V8A-25QR/883C	Contact Factory
30	25	20	130	24-Pin CERDIP	GAL20V8A-30LD/883C	5962-8984001LA
			130	28-Pin LCC	GAL20V8A-30LR/883C	5962-89840013A

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

PART NUMBER DESCRIPTION



GAL22V10B/883C
GAL22V10/883C

High Performance E²CMOS PLD

FEATURES

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - — 15 ns Maximum Propagation Delay
  - — Fmax = 62.5 MHz
  - — 8ns Maximum from Clock Input to Data Output
  - — TTL Compatible 12 mA Outputs
  - — UltraMOS® Advanced CMOS Technology
- ACTIVE PULL-UPS ON ALL PINS
- COMPATIBLE WITH STANDARD 22V10 DEVICES
  - — Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices
- 50% REDUCTION IN POWER VERSUS BIPOLAR
- E² CELL TECHNOLOGY
  - — Reconfigurable Logic
  - — Reprogrammable Cells
  - — 100% Tested/Guaranteed 100% Yields
  - — High Speed Electrical Erasure (<100ms)
  - — 20 Year Data Retention
- TEN OUTPUT LOGIC MACROCELLS
  - — Maximum Flexibility for Complex Logic Designs
- PRELOAD AND POWER-ON RESET OF REGISTERS
  - — 100% Functional Testability
- APPLICATIONS INCLUDE:
  - — DMA Control
  - — State Machine Control
  - — High Speed Graphics Processing
  - — Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

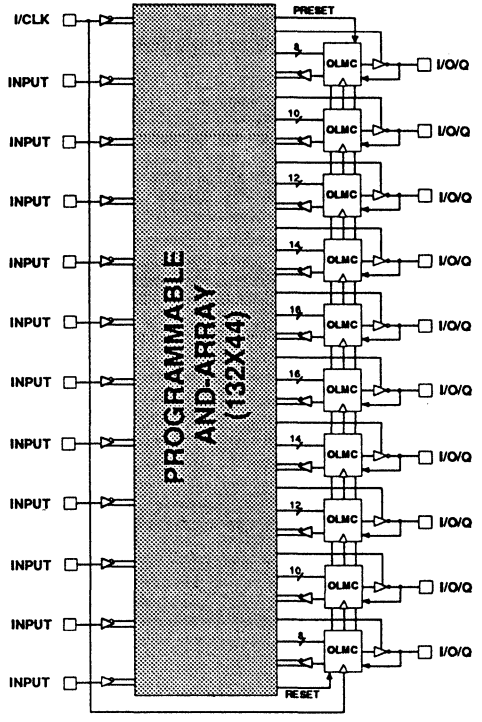
DESCRIPTION

The GAL22V10B/883C and GAL22V10/883C are high performance E²CMOS programmable logic devices processed in full compliance to MIL-STD-883C. These military grade devices combine a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available of any military qualified 22V10 device. CMOS circuitry allows the GAL22V10/B to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10B and GAL22V10 are fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

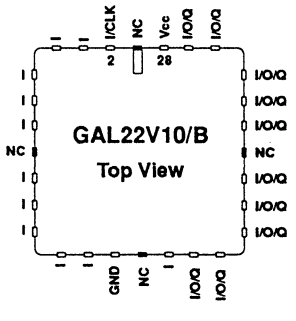
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products.

FUNCTIONAL BLOCK DIAGRAM

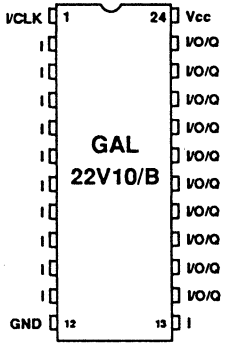


PACKAGE DIAGRAMS

LCC



CERDIP



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124 U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

April 1991.Rev.A

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{cc} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{cc} +1.0V
Off-state output voltage applied ..... -2.5 to V_{cc} +1.0V
Storage Temperature ..... -65 to 150°C
Case Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) ..... -55 to 125°C
Supply Voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	–2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-15		UNITS
			MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	15	ns
tco	1	Clock to Output Delay	—	8	ns
tcf[2]	—	Clock to Feedback Delay	—	8	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	ns
ten	2	Input or I/O to Output Enabled	—	15	ns
tdis	3	Input or I/O to Output Disabled	—	15	ns
tar	1	Input or I/O to Asynchronous Reset of Register	—	20	ns
tarw	—	Asynchronous Reset Pulse Duration	15	—	ns
tarr	—	Asynchronous Reset to Clock↑ Recovery Time	15	—	ns
tspr	—	Synchronous Preset to Clock↑ Recovery Time	12	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{cc} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{cc} +1.0V
Off-state output voltage applied ..... -2.5 to V_{cc} +1.0V
Storage Temperature ..... -65 to 150°C
Case Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_c) ..... -55 to 125°C
Supply Voltage (V_{cc})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-150	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	–2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V f_{toggle} = 15Mhz Outputs Open	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

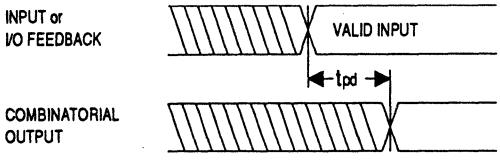
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

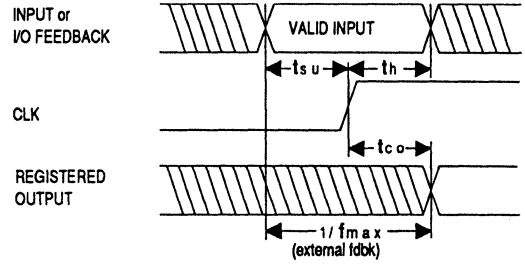
PARAMETER	TEST COND.[1]	DESCRIPTION	-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinatorial Output	—	20	—	25	—	30	ns
t_{co}	1	Clock to Output Delay	—	15	—	20	—	20	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	15	—	20	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	17	—	20	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	31.2	—	25	—	22	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	31.2	—	25	—	22	—	MHz
	1	Maximum Clock Frequency with No Feedback	33	—	33	—	25	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	15	—	15	—	20	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	15	—	15	—	20	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	20	—	25	—	25	ns
t_{dis}	3	Input or I/O to Output Disabled	—	20	—	25	—	25	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	25	—	30	—	30	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	20	—	25	—	30	—	ns
t_{arr}	—	Asynchronous Reset to Clock↑ Recovery Time	20	—	25	—	30	—	ns
t_{spr}	—	Synchronous Preset to Clock↑ Recovery Time	17	—	20	—	25	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

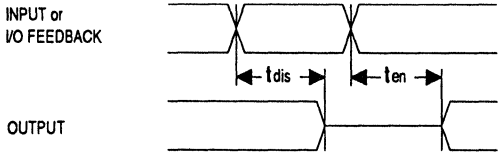
SWITCHING WAVEFORMS



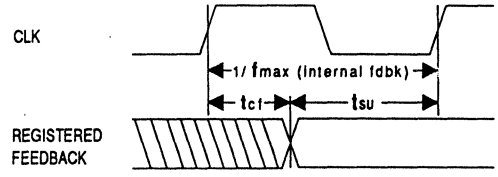
Combinatorial Output



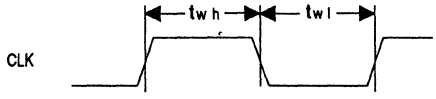
Registered Output



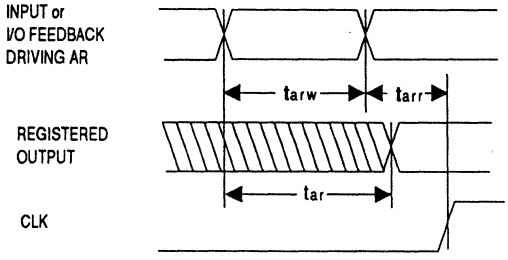
Input or I/O to Output Enable/Disable



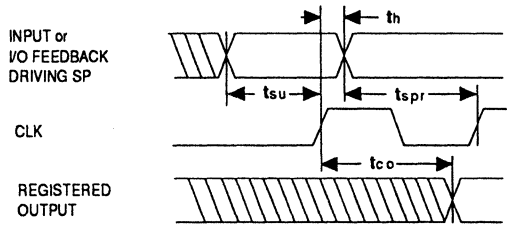
fmax with Feedback



Clock Width

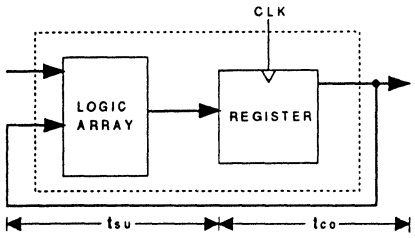


Asynchronous Reset



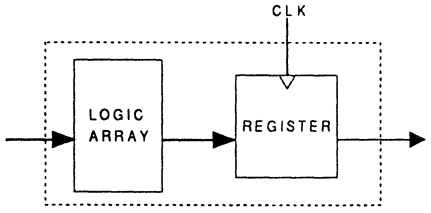
Synchronous Preset

fmax DESCRIPTIONS



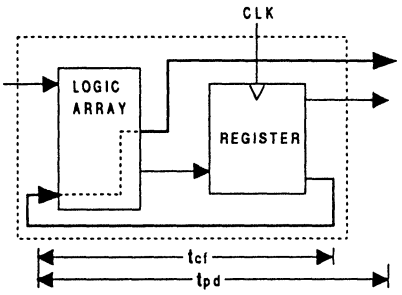
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax With No Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/ internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

3

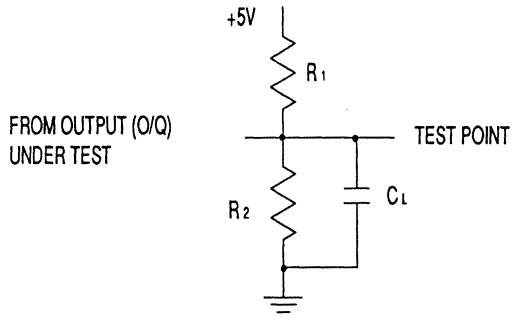
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		390Ω	750Ω	50pF
2	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
3	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF



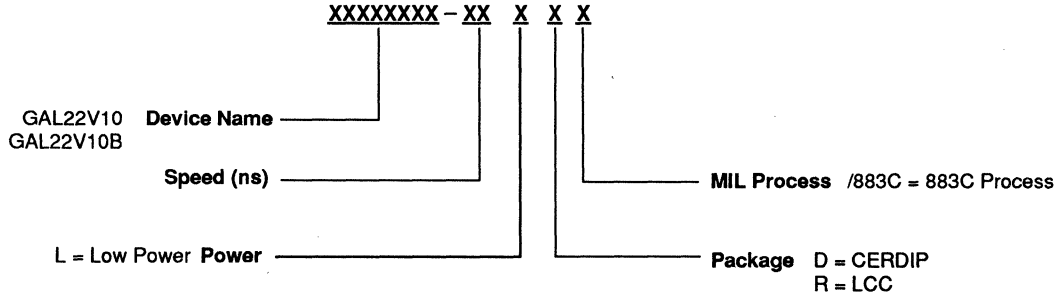
C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

GAL22V10/B ORDERING INFORMATION (MIL-STD-883C and SMD)

					Ordering #	
Tpd (ns)	**Tsu (ns)**	**Tco (ns)**	**Icc (mA)**	**Package**	**MIL-STD-883C**	**SMD #**
15	12	8	150	24-Pin CERDIP	GAL22V10B-15LD/883C	5962-8984103LA
			150	28-Pin LCC	GAL22V10B-15LR/883C	5962-89841033A
20	17	15	150	24-Pin CERDIP	GAL22V10-20LD/883C	5962-8984102LA
			150	28-Pin LCC	GAL22V10-20LR/883C	5962-89841023A
25	20	20	150	24-Pin CERDIP	GAL22V10-25LD/883C	5962-8984104LA
			150	28-Pin LCC	GAL22V10-25LR/883C	5962-89841043A
30	25	20	150	24-Pin CERDIP	GAL22V10-30LD/883C	5962-8984101LA
			150	28-Pin LCC	GAL22V10-30LR/883C	5962-89841013A

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

PART NUMBER DESCRIPTION



GAL20RA10/883C

High-Speed Asynchronous E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 20 ns Maximum Propagation Delay**
  - **— Fmax = 41.7 MHz**
  - **— 20 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 8 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<50 ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Independent Programmable Clocks**
  - **— Independent Asynchronous Reset and Preset**
  - **— Registered or Combinatorial with Polarity**
  - **— Full Function and Parametric Compatibility with PAL20RA10**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— State Machine Control**
  - **— Standard Logic Consolidation**
  - **— Multiple Clock Logic Designs**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

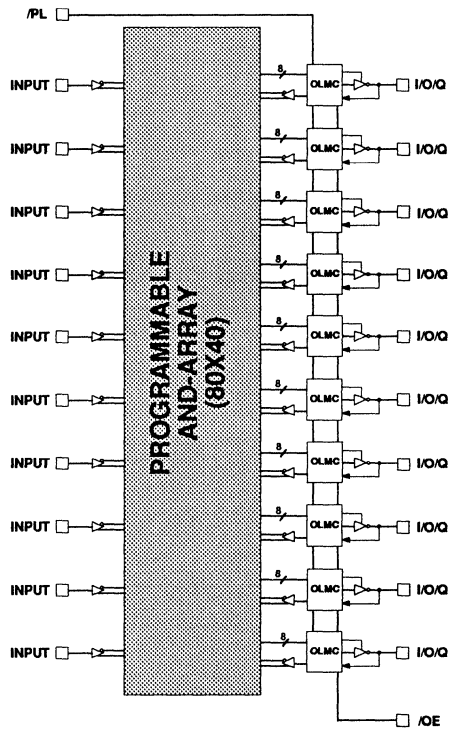
DESCRIPTION

The GAL20RA10/883C is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883C. With a 20ns maximum propagation delay time, it is the fastest military grade 20RA10 device on the market. In addition to speed performance, Lattice's Electrically Erasable (E^2) floating gate technology provides low power performance. The GAL20RA10's typical Icc of 75mA, represents a 50% savings in power when compared to bipolar counterparts. E^2 technology also offers high speed (<50ms) erase times providing the ability to reprogram or test the devices quickly and efficiently.

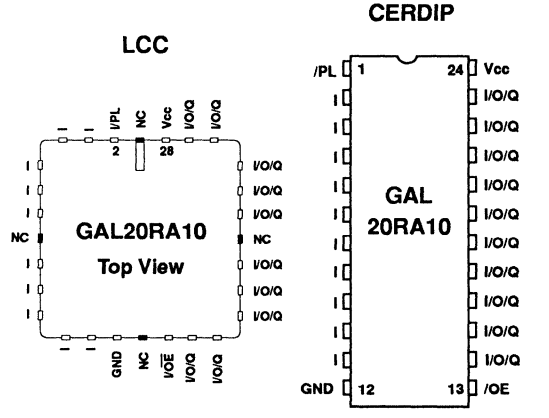
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE guarantees data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503)681-3037

April 1991.Rev.A

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Case Temperature with
Power Applied .....-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Military Devices:
Case Temperature (T_C) .....-55 to +125°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	75	120	mA

1) The leakage current is due to the internal pull-up on all pins. See the **Input Buffer** section in the commercial datasheet for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	20	—	25	ns
tco	1	Clock to Output Delay	—	20	—	25	ns
tsu	—	Setup Time, Input or Feedback before Clock	10	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock	3	—	5	—	ns
fmax[2]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	33.3	—	25.0	—	MHz
	1	Maximum Clock Frequency with No Feedback	41.7	—	33.3	—	MHz
twh[3]	—	Clock Pulse Duration, High	12	—	15	—	ns
twl[3]	—	Clock Pulse Duration, Low	12	—	15	—	ns
ten / tdis	2,3	Input or I/O to Output Enabled / Disabled	—	20	—	25	ns
ten / tdis	2,3	$\overline{OE}$ to Output Enabled / Disabled	—	15	—	15	ns
tar / tap	1	Input or I/O to Asynchronous Reset / Preset	—	20	—	25	ns
tarw / tapw	—	Asynchronous Reset / Preset Pulse Duration	20	—	25	—	ns
tarr / tapr	—	Asynchronous Reset / Preset Recovery Time	12	—	20	—	ns
twp	—	Preload Pulse Duration	20	—	25	—	ns
tsp	—	Preload Setup Time	15	—	20	—	ns
thp	—	Preload Hold Time	15	—	20	—	ns

1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Descriptions** section.
3) Clock pulses of widths less than the specification may be detected as valid clock signals.

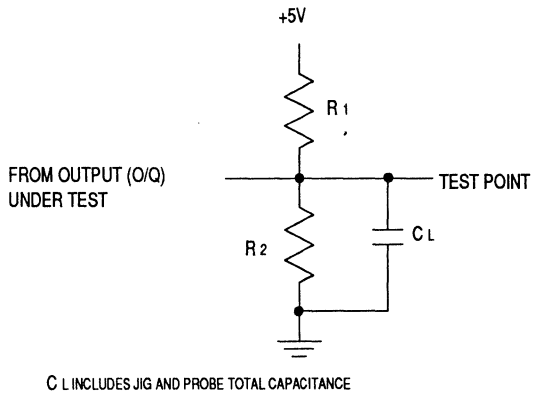
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

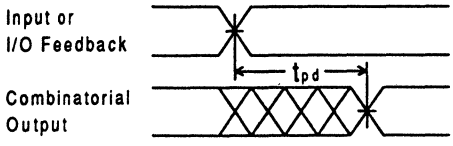
Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		470Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	470Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	470Ω	390Ω	5pF

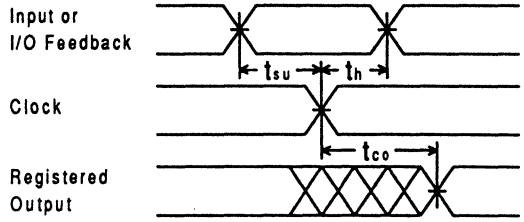


C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

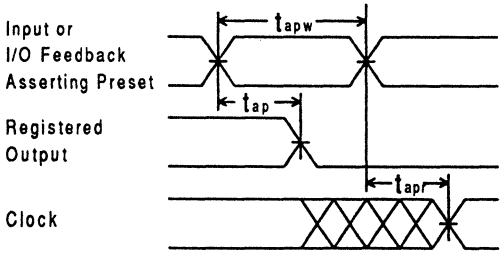
SWITCHING WAVEFORMS



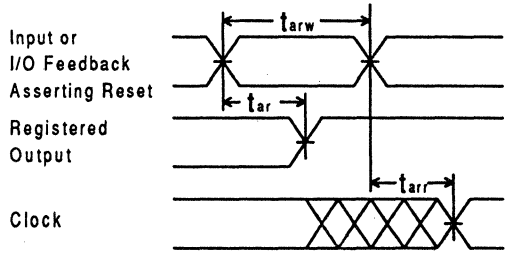
Combinatorial Output



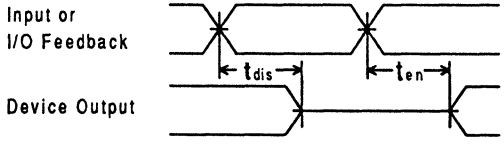
Registered Output



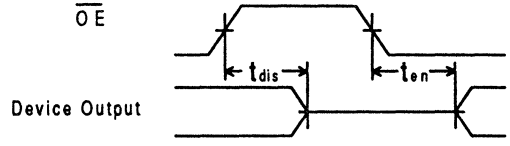
Asynchronous Preset



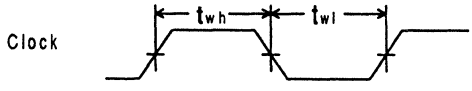
Asynchronous Reset



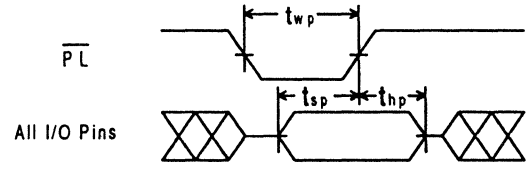
Input or I/O Feedback to Enable / Disable



OE to Enable / Disable

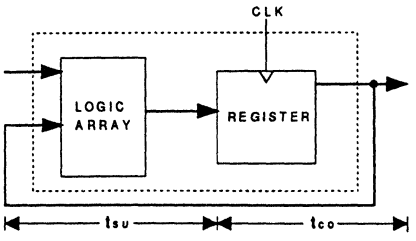


Clock Width



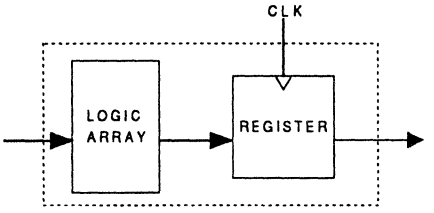
Parallel Preload

fmax DESCRIPTIONS



fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.

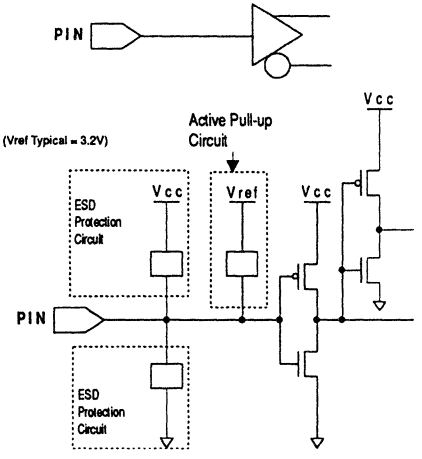


fmax With No Feedback

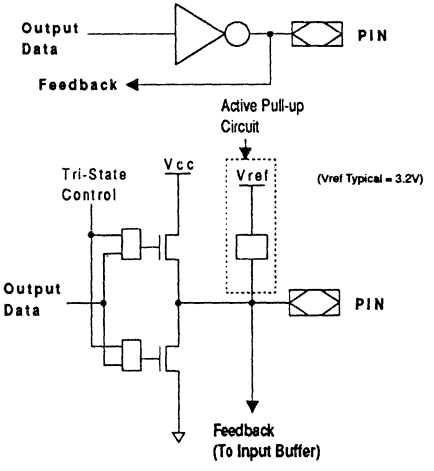
Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.

3

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input

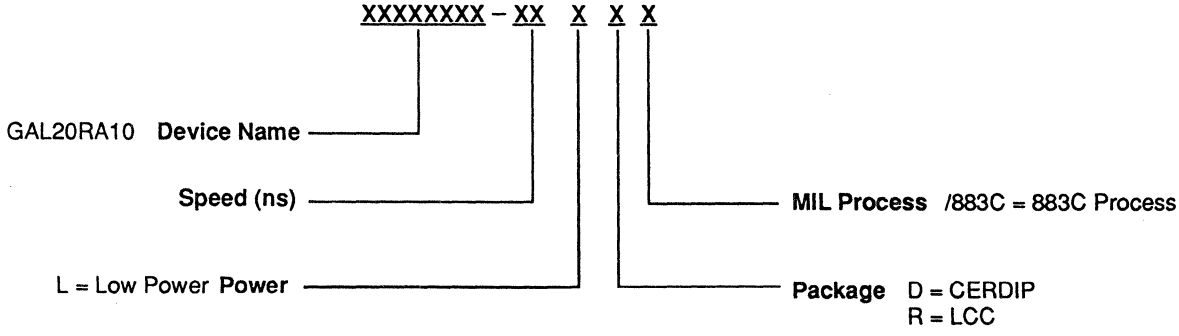


Output

GAL20RA10/883C MILITARY GRADE ORDERING INFORMATION

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering # MIL-STD-883C	Ordering # SMD #
20	10	20	120	24-Pin CERDIP	GAL20RA10-20LD/883C	Contact Factory
				28-Pin LCC	GAL20RA10-20LR/883C	Contact Factory
25	15	25	120	24-Pin CERDIP	GAL20RA10-25LD/883C	Contact Factory
				28-Pin LCC	GAL20RA10-25LR/883C	Contact Factory

PART NUMBER DESCRIPTION



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Quality Assurance Program

INTRODUCTION

Lattice views quality assurance as a corporate responsibility and an integral part of all planning activities. Lattice's Quality Assurance organization is independent from Manufacturing and has direct access to top management, assuring sufficient authority is afforded to quality issues.

Lattice's quality program is in full compliance to the quality assurance requirements of MIL-M-38510 Appendix A and all inspection system requirements of MIL-I-45208.

QUALIFICATION

All new products, processes and vendors must pass predefined evaluations before receiving initial qualification release. Major changes to products, processes or vendors require additional qualificaton before implementation. To assure continuing conformance to reliability requirements, a weekly accelerated monitor program is maintained on all processes and wafer fabrication sites.

IN-PROCESS CONTROL

Qualified product must be manufactured under strict quality controls that start with regulated procurement and documented inspection plans for all incoming materials. Sample testing and in-line monitoring as well as statistical process control charts provide constant feedback at each critical step of the manufacturing process. Nonconforming material is identified, segregated, analyzed and dispositioned according to procedures that also require corrective action be specified to eliminate the cause of the defect.

CALIBRATION

All critical equipment involved in the manufacture, testing, or inspection of Lattice product must meet the requirements of our established calibration system that is in compliance to MIL-STD-45662.

TRAINING

All Lattice manufacturing personnel complete a comprehensive training program and obtain formal certification for each production operation before they are allowed to manufacture products. Operators must be recertified on a periodic basis to assure ongoing compliance to all written procedures and specifications.

SUBCONTRACTOR CONTROL

All subcontracted operations must be performed by sources exhibiting a quality program commensurate to that of Lattice. These vendors are audited at least once every year to monitor their compliance to Lattice's Quality Assurance Program. Any major audit discrepancy requires corrective action and may result in disqualification.

DOCUMENT CONTROL

Lattice's document control system is under the direction of Quality Assurance and has the responsibility of assuring that every product has adequate written documentation released before production begins.

Drawings and specifications related to materials, processes, testing, products and subcontractors are maintained by the Document Control Department. A numbering system identifies each document by revision status, function and category.

Any change to existing documentation must be properly approved and released before implementation of the change. The change is implemented only if approved by the appropriate functional groups.

CONTROL OF NONCONFORMING MATERIAL

All identified failures from qualification testing, inspections, customer returns or in-process screening are processed through Lattice's Failure Analysis group to determine the cause or relevancy of the failure and initiate corrective actions to eliminate the cause. All failure analysis reports are reviewed by Quality Assurance to convey awareness of any potential problems and assure that proper corrective action is taken.

Lattice has a Material Review Board (MRB) to investigate the cause of nonconformance and disposition the material. Lattice and customer specification requirements are thoroughly reviewed during MRB dispositions. The MRB consists of representatives from Manufacturing, Engineering, and Quality Assurance.

Product returned by customers (RMA) shall be analyzed and dispositioned with respect to Lattice and customer specifications.

Finished Wafer Process Control Points for Commercial/Industrial Devices

STEP	CHARACTERISTICS	CHART TYPE	RESPONSIBILITY
Wafer Parametric Test	Test Structure Performance	Cp, K	Engineering
Die Functional Test	Functional, AC, DC Performance	Trend	Engineering
Wafer Saw	Kerf Width	X-R	Production
Die Attach	Visual Defects	P	Production
Wire Bond	Pull Test	X-R	Quality Assurance
Mold	Mold Tool Temp	X-R	Production
Deflash Trim Form	Visual Defects Coplanarity (PLCC only)	P X-R	Production Production
Solder Plate	Thickness % Pb	X-R P	Quality Assurance Quality Assurance
Assembly Final Visual	Visual Defects	P	Quality Assurance
Test	Functional, AC, DC Performance	Trend	Engineering
Topside Mark	Visual Defects	P	Production
Lead Straighten	Splay, Lead Alignment (PDIP only)	P	Production
Final QA	Visual Defects	P	Quality Assurance
Final QA Test	Functional, AC, DC Performance	P	Quality Assurance

Qualification Program

INTRODUCTION

Lattice has an intensive qualification program for examining and testing new products, processes, and vendors in order to insure the highest levels of quality. Lattice's Reliability Engineering Group is responsible for defining and implementing this qualification program.

The following table outlines the steps which must be performed before a new product, package or process is qualified. The requirements listed below are general guidelines. Detailed information on Lattice's qualification process is available to customers upon request.

Qualification Requirements

Test	# of Samples	Duration		
		New Product	New Wafer Process	New Package
125° C Operating Lifetest (5.25V)	300	1,000 Hours	2,000 Hours	2,000 Hours[1]
150° C Biased Retention Bake (5.25V)	450	1,000 Hours	2,000 Hours	2,000 Hours[1]
Endurance Cycling	75	10,000 Cycles	10,000 Cycles	N/A
ESD	48	End of Test	End of Test	N/A
Latch-Up Immunity	27	End of Test	End of Test	N/A
Temperature Cycling (-65 to 150° C)	150	1,000 Cycles	1,000 Cycles	1,000 Cycles
Biased 85/85 (5V)	225	N/A	1,000 Hours	1,000 Hours
Autoclave (121° C, 15psig)	150	N/A	336 Hours	336 Hours
Lead Integrity (DIP only)	9	N/A	N/A	End of Test
Solderability	9	N/A	N/A	End of Test
Centrifuge	75	N/A	N/A	End of Test
Bond Strength	12	N/A	N/A	End of Test

1. Required for new assembly technologies only.

RELIABILITY MONITOR PROGRAM

The Reliability Monitor Program provides for a weekly reliability monitor of Lattice products. The program assures that all Lattice processes, products, and packages comply on a continuing basis with established reliability and quality levels.

The Reliability Monitor Program is designed to monitor all fab and assembly facilities as well as each process technology in production. A summary of the program test and sampling plan is shown below.

Weekly Reliability Monitor Program

Test	# of Samples	Duration
125° C Operating Lifetest (7.00V)	70	160 Hours
200° C Biased Retention Bake (5.25V)	70	160 Hours
Autoclave (121° C, 15psiq)	35	160 Hours

E²CMOS Testability Improves Quality

INTRODUCTION

The inherent testability of Lattice's E²CMOS PLDs significantly improves their quality and reliability. By using electrically erasable EEPROM technology to produce GAL devices, Lattice is able to perform 100% AC/DC, functional, and parametric testing of every single device. In order to achieve the highest quality levels, Lattice programs and tests each device repeatedly throughout the manufacturing process.

ACTUAL TEST VS. SIMULATED TEST

Why is "actual test" so significant? PLDs, unlike most other semiconductor devices, have a programmable element that determines the final device functionality and AC/DC performance. These programmable elements can be fabricated from metal link fuses, programmable diodes or transistors, volatile static RAM cells, UV EPROM cells or electrically erasable EEPROM cells. Each of these technologies carries a different variability of programming success and a variance in the impact of the programming success on the performance and reliability of the device.

The most common programmable elements are the metal fuse, EPROM cell and EEPROM cell. Of these element types, only the EEPROM cell can be thoroughly tested by the manufacturer prior to shipment to an end user OEM.

EEPROM ALLOWS ACTUAL TEST

Each of the methods identified above can be programmed. In this manner they are all the same. The differences become apparent when the erase times are analyzed. Metal link and One-Time Programmable (OTP) devices cannot be erased. UV EPROM devices can be erased, however the time required is 20-30 minutes (and an expensive windowed package). EEPROM devices, on the other hand, offer instant erasability on the order of 50 ms (thousandth's of a second). The advantage of this instant erase for manufacturing test is significant. Instant erase allows instant re-patterning for additional testing. EEPROM technology has been used for PLD manufacturing by Lattice for more than half a decade. Lattice refers to their high performance EEPROM technology as E²CMOS technology. Extensive reliability studies of the technology have been performed with industry-wide acceptance, including the military.

OTHER METHODS ARE IMPRECISE

All PLD devices must be tested to some degree to validate functionality and performance. Technologies that are not erasable or offer lengthy erase times severely constrain the test flexibility. Since the normal "user" programmable elements cannot be programmed during manufacture (all elements must be available for end-user programming) the manufacturers resort to using simulated and correlated performance of test rows, test columns and phantom or dummy-test arrays. At best, this is a statistical measure of the actual device performance. One need only look at the "normal" programming yield fallout of 0.5 —> 3% or the "acceptable" post-programming test vector & board yield fallout of 0.5 —> 2% to know that this correlation is weak. The quality systems of today are measuring defects in the parts per million (PPM). A six sigma program requires less than 3.4 PPM, four orders of magnitude less than that achievable with non-testable PLDs.

ACTUAL MATRIX PATTERNING

The unique capability of E²CMOS devices to be instantly electrically erased allows these devices to be patterned multiple times during Lattice's manufacturing test. Normal array cells in the programmable matrix are patterned, erased & tested again and again. The test rows or columns, phantom arrays, etc., that are used with other technologies are not necessary with E²CMOS devices. Programmability of every cell is checked dozens of times.

Historically, the checking of a successful programming operation consisted of no more than a pass/fail verification step. This digital, black/white style check is not adequate to assure that the cell is programmed properly with sufficient margin to guarantee long-term reliable performance of the device. E²CMOS devices have an additional cell verification step that consists of an analog measure (to millivolt accuracy) of the actual charge stored on the cell. This data is used for extensive reliability and quality measurements and testing.

WORST CASE AC/DC TESTING

A PLD does not have a defined function until the engineer patterns the device with his custom pattern. The manufacturer, when considering the testing of a PLD, must consider the hundreds of different architecture and functional variations that can be created by the end user. Each configuration of architecture brings on a different set of worst case pattern and stimulus conditions. Quick

application of a series of worst case patterns that cover all of the permutations of input combinations, array load & switching, and output configuration is required.

E²CMOS devices offer instant erasability to address this reconfiguration & test problem. Testing each additional worst case configuration takes fractions of a second, allowing dozens of patterns to be checked to assure performance to rated speeds even under the most grueling AC pattern. The final result is a device with defects reduced from PPH (parts per hundred) to PPM (parts per million).■

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GAL Metastability Report

INTRODUCTION

The dictionary definition of metastability is "a situation that is characterized by a slight margin of stability." When applied to bi-stable (digital) logic, the term refers to an undesirable marginally stable output state between VIL max and VIH min.

Metastability can occur in bi-stable storage elements (registers, latches, memories, etc.) when setup and/or hold times are violated. Since setup and hold times vary with temperature and operating voltage, among other factors, the times referred to here are not the min/max numbers printed in data sheets, but rather the actual times for the given set of operating conditions. Typical applications where such times are likely to be violated include bus & memory arbiters, interfaces, synchronizers, and other state machines employing asynchronous inputs or asynchronous clocks.

Metastability manifests itself in a number of different ways. Common responses are (shown as they might be captured on a digital oscilloscope in Figure 1): runt pulse (1a), decreased output slew rate (1b), output oscillation (1c), and increased clock-to-output time (1d). By definition, the phenomenon of metastability is statistical in nature. Not only is entry into the state uncertain, but the time spent there is also variable.

Because PLDs are commonplace in today's designs, a thorough understanding of their metastable behavior is crucial. In some applications, output anomalies shorter than one clock cycle may be acceptable, but in applications where the register output is used as a control signal (clock, bus grant, chip select, etc.) for other circuitry, faults such as runt pulses and oscillation cannot be tolerated.

This report will not study the causes or characteristics of metastability in great detail; excellent material has already been prepared on this subject [1-5]. Rather, this report will introduce a mathematical model for the metastable phenomenon, discuss potential test methodologies, present and compare test results from various bipolar and CMOS PLDs, and discuss how to interpret the data. This report will close with suggestions on how to design metastable tolerant systems.

DERIVATION OF CONSTANTS

The basic premise of all metastability models is that a device's output is more likely to have settled to a valid state in time(t) than in time(t-n). In fact, the failure probability distribution follows an exponential curve. Figure 2 shows a typical failure frequency plot.

It is accepted [1] that metastable failures can be accurately modeled by the equation:

$$\log \text{Failure} = \log \text{MAX} - b(\Delta - \Delta o) \qquad (1)$$

In this equation, MAX represents the maximum failure rate for a particular environment, Δ is the time delayed before sampling the DUT (Device Under Test) output, and Δo is the time at which the number of failures starts to decrease. On a failure frequency plot (such as the one in Figure 2), Δo represents the knee of the curve. The constant b is rate at which the frequency of failures decreases after the knee is reached.

Recall that:

$$\log X = a \ln (X), \text{ where } a = \log (e)$$

Substituting this into (1):

$$a \cdot \ln \text{Failure} = a \cdot \ln \text{MAX} - b(\Delta - \Delta o) \qquad (2)$$

MAX is related to the clock frequency (fCLOCK) and data frequency (fDATA). That is,

$$\text{MAX} = (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) \qquad (3)$$

Substituting (3) into (2) and applying some algebra:

$$a \cdot \ln \text{Failure} = a \cdot \ln (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) - b(\Delta - \Delta o)$$

$$\ln \text{Failure} - \ln (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) = -b/a(\Delta - \Delta o)$$

Setting k2 = b/a and rearranging the equation yields:

$$\text{Failure} = (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) e^{-k2(\Delta - \Delta o)} \qquad (4)$$

When used with equation (4), the constants k1, k2, and Δo, completely describe a particular device's metastable characteristics; they indicate how quickly a device can resolve the metastable condition. Devices which transition out of the metastable region quickly are characterized by a small Δo and a large k2.

The constant k1 is peculiar to the test apparatus (it can be thought of as a "scaling factor"). The maximum metastable failure rate (MAX) is limited by fCLOCK; a failure cannot occur if the device isn't clocked. Likewise, it is true that a metastable failure cannot occur unless data has changed. So, if fDATA < fCLOCK, then MAX = fDATA. This was the case in the test fixture Lattice used (fCLOCK=10MHZ, fDATA=2.5MHz). Substituting MAX = fDATA back into equation (3) yields: k1 = 1/fCLOCK, so k1 = 100ns for our tests.

5

TEST FIXTURE

The goal of testing a particular device's metastable characteristics is to generate real numbers for the constants k2 and Δo. To do this, the device must first be forced into the metastable state. This is done by intentionally violating setup and/or hold times. Once metastable, the output can be observed on an oscilloscope or used to increment an event counter.

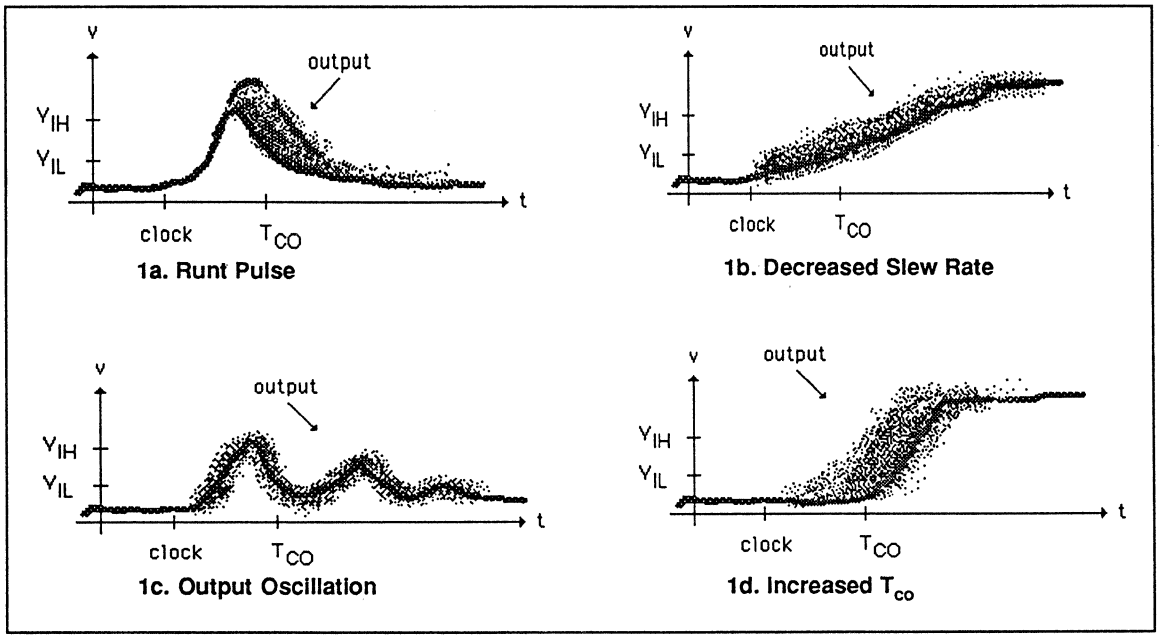
Traditional Approach

One approach to characterizing a device's metastable behavior employs a test fixture similar to that shown in Figure 3a. In such a fixture, data to the device includes a "jitter band" so that the device sees changing data as it is clocked. The DUT output is fed to a window comparator to determine when it is in the metastable region (between VIL max and VIH min). The comparator output can be sampled periodically and used to increment an event counter.

This method of testing, though it directly yields MTBF numbers, has some drawbacks. The first is that it does not distinguish between the different types of metastable behavior (runt pulse, oscillation, slow rise/fall time, delayed transition), and it may have difficulty detecting every type. Also, the registers used in the detector circuit itself may become metastable, which would adversely affect the results.

A New Approach

The test method used to gather data for this report used the circuit shown in Figure 3b. The tester employed an "infinite precision" variable delay circuit to control clock placement



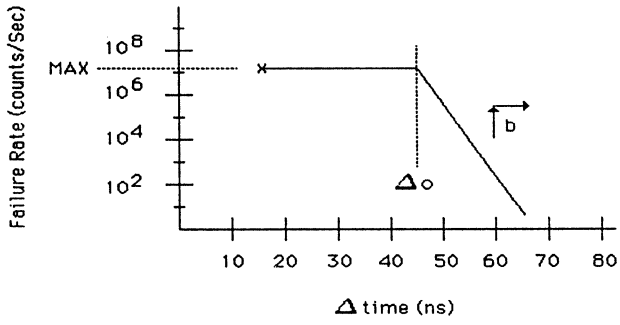


Figure 2. Typical Failure Frequency Plot

with respect to data. This arrangement allowed exact worst case placement of the clock, so as to induce metastability with nearly every clock pulse.

Using a digital oscilloscope (Tektronix 11403A) in point accumulate mode, metastable failures were recorded over a lengthy period of time. A hardcopy was then made and the constants empirically obtained (details below).

The oscilloscope approach, being visual in nature, enables the designer to make educated decisions regarding maximum clock and data rates, as well as the suitability of using the output to drive other circuitry. The five minute sample period used in our tests contained approximately 750 million failures. Much longer sample periods were evaluated, but they provided no perceptible gain in usable information.

A slight disadvantage of this approach is that extracting k2 and Δo values from the hardcopies is not straightforward. Because each point on the hardcopy can represent any number of actual samples (between one and 1.5 million), one cannot simply count the points at time(t) for the MTBF at that time (although, in the case of the scattered points, the probability is low that a single isolated point represents more than one sample).

To generate values for k2 and Δo, it was necessary to refer to previous metastability studies [1]. By studying the output plots of devices with known constants, certain relationships were established. For example, it was determined that Δo represents the time from the leading edge of the output until the "dot density" starts to decrease measurably. It should be noted that Δo in previous studies included device propagation delays, whereas in our test it does not.

The time from Δo until the dot density equals zero was defined to be the "time to metastable release" or simply time(r). The relationship between k2 and time(r) is given below in (5), and shown graphically in Figure 4. Recall that MAX=2.5x10^6 and a=log(e).

$$k2 = \log(MAX) / (time(r) \cdot a) = 14.73/time(r) \qquad (5)$$

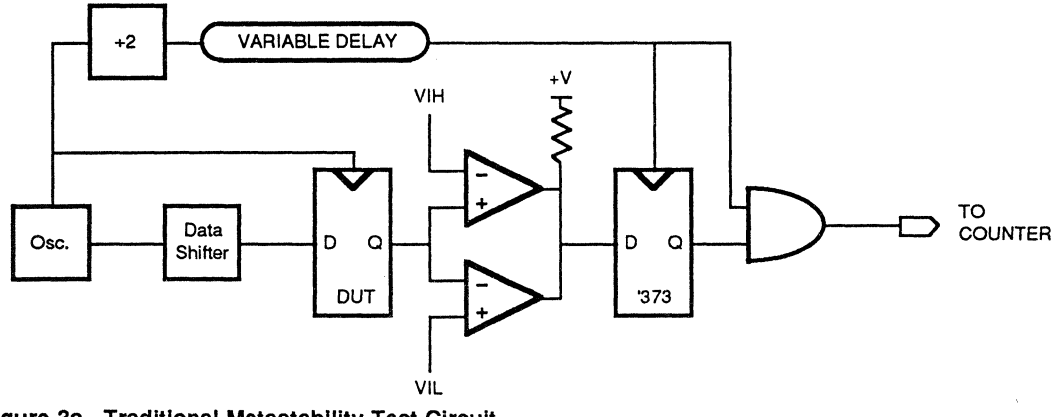


Figure 3a. Traditional Metastability Test Circuit

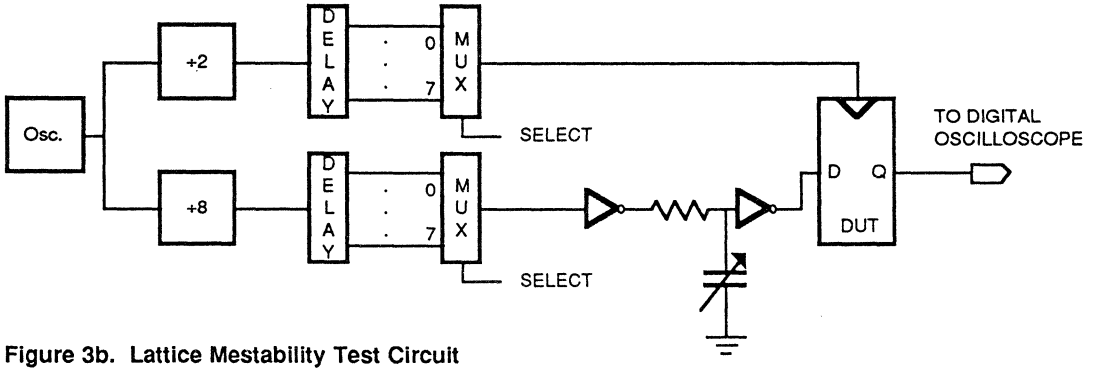


Figure 3b. Lattice Mestability Test Circuit

5

INTERPRETING THE RESULTS

In addition to examining E²CMOS GAL devices, this study also tested several bipolar PAL devices as well as other CMOS PLDs. To insure that the results of this study would be relevant, all necessary precautions were observed: the devices were of recent vintage and were acquired blindly through distributors; multiple samples of each device were tested and the results combined; all devices had either fixed 16R8 architectures or were configured to emulate the 16R8 architecture; the devices were programmed from the same JEDEC fuse map file (the source equations and the JEDEC fuse map file are presented in Listing 1).

Plots 1 through 6 on the following pages are some of the oscilloscope plots generated for this study. The top waveform in each plot is the clock signal, the middle trace is the metastable data output and the bottom trace is the histogram of the accumulated samples between 1V and 2V of the output signal. The horizontal scale is 2ns per division, so the exact clock to output time of the metastable output condition can be read directly. The vertical scale is 2V per division for the top trace, and 1V per division for the middle trace.

The middle waveform in each plot is the metastable device output which is the only signal captured in point accumulate mode. In every case, the output signal plot shows two stable levels after the transition. This is a direct result of the "indecision" caused by metastability; on some cycles the output settled to a high level, while on others it settled to a low level.

Plot 4 shows the response of a bipolar PAL16R8-7. Notice the very well defined runt pulse (this correlates with previous data gathered on similar devices by the manufacturer [1]). The absence of a secondary trace along ground indicates that the output always starts to transition to a high level, even when it finally settles to a low level. This characteristic makes the device unsuitable for use in control path applications (when metastability is possible). All of the bipolar parts examined showed similar results.

Plot 1, 2 and 3 are from GAL16V8B-7, GAL22V10B-10 and GAL6001-30, respectively. Aside from the fact that setup time violations may cause t_{co} to increase by a small (but random) amount, the outputs are very clean and well behaved. The fact that there are no runt pulses or other anomalies is extremely significant, as the GAL6001 not only allows asynchronous clocking, but encourages that activity. Although GAL6001 is a much slower device as compared to GAL16V8 and GAL22V10, the similar metastable characteristics of the GAL6001 to the much faster GAL devices indicate that the inherent metastable characteristics of all the GAL devices have consistently desirable characteristics across all speed grades. Comparing Plot 1, 2 and 3 with Plot 4 and 5 shows that characteristics of the GAL devices are superior to those of bipolar PLDs. Plot 6 illustrates metastable characteristics of the TTL flip-flop (TISN74AS74).

For reference purposes, Plots 7 through 9 are included. Plot 7 shows a normal (ie. non-metastable) GAL16V8B-7 transition; and Plot 8 a normal PAL16R8-7 transition. Plot 9 is the normal transition of the TTL flip-flop (TI SN74AS74). For consistency, only rising edges have been shown. Our tests also covered falling edges which, in general, were interesting but did not provide any additional information.

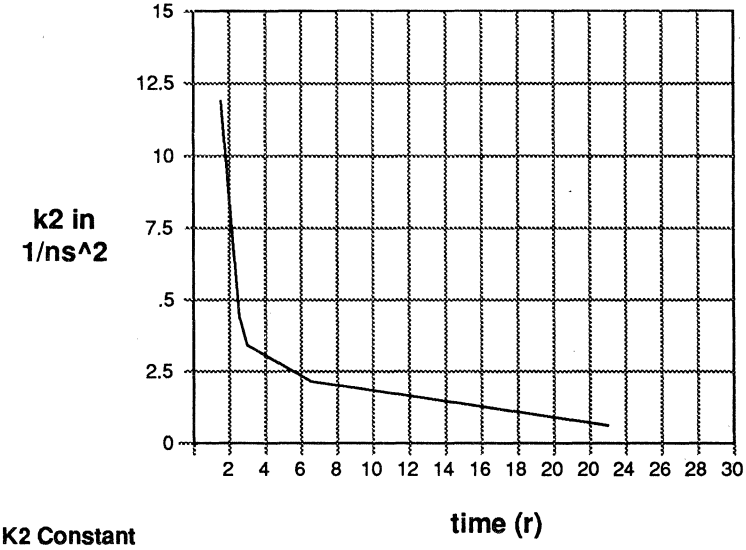


Figure 4. K2 Constant

For a more quantitative look at the phenomenon of metastability, refer to the table beneath each plot. These tables list the measured values of the constants Δo and k2 for the device whose plot is shown, and for similar devices. Recall that large k2 and small Δo values are desirable. The numbers in the tables correlate closely with the results of earlier tests [1,5], confirming the validity of our test method.

Since all current GAL devices possess very similar register and output buffer circuitry, and all are fabricated using the same basic process, the data shown in Table 1 for the GAL16V8 is considered applicable to all devices and speed grades in the GAL family.

USING THE RESULTS

If a register enters the metastable state in a system, then data was obviously unstable as the register was being clocked. The argument over which data should have been captured (old or new) is academic as the register will randomly pick one or the other. Signals in most asynchronous systems are active for more than one clock cycle, so if they are missed initially, they could be captured on a subsequent clock cycle.

It is the task of the state machine designer to take adequate precautions against metastability causing illegal states to be entered. One way to do this is by using "gray codes" when ordering states. Gray code state equations allow only one state bit to change during a state transition. Thus, the worst metastability could do would be to delay a state transition by one clock cycle. If more than one bit were allowed to change, the outcome would be purely random, and probably illegal. Figure 5 shows examples of both cases.

Other solutions are to externally (or internally) synchronize the asynchronous signals, or to increase cycle times to allow time for metastable outputs to settle. An example of the latter solution is given below.

It is worth noting at this point that state machines (synchronous or asynchronous) can fail for reasons other than metastability. A not insignificant component of a PLD's specified setup time is directly attributable to internal data skewing [2]. Data skewing is the inevitable result of differing signal path lengths, loading conditions, and gate delays. Stated another way, each input to output path has its own set of actual AC specifications. If insufficient setup time has passed, different "versions" of the same data may be present at the inputs of different registers as they are clocked. A good example of this is:

```
Output_Pin19 := Input_Pin2;
Output_Pin15 := !Input_Pin2;
```

If clocked at precisely the right moment after an input transition, one register will capture old data while the other captures new data, resulting in a system failure. This condition, though also the result of a setup time violation, should not be confused with metastability (the "incorrect" data that is captured has normal output characteristics); it is, pure and simply, the result of a violation of specifications.

Example
To determine the maximum clock rate (given an acceptable error rate) that a particular device will allow in an asynchronous environment, equation (4) is used. For example, the system shown in Figure 6 utilizes a 9600 baud (bits/sec) asynchronous data stream. The system clock period is tCO+tPD+tSU+Δ. For one failure per year:

$$3.2\times10^{-8} = [(1\times10^{-7})(1/(\Delta+22))(9600)]e^{-[4(\Delta-.44)]}$$

Solving for Δ yields Δ=2.22ns, or about 2ns, for a cycle time of 24ns. Referring back to Plot 1, the additional delay of 2ns intuitively makes sense. Remember, in terms of setup and hold time violations, the oscilloscope plots were made under worst case failure conditions; the scattered dots could represent MTBFs of days, years, or even millenniums in a typical asynchronous environment.

Due to the extremely quick metastable settling times of GAL devices, a relatively small increase in the cycle time will produce a dramatic improvement in reliability.

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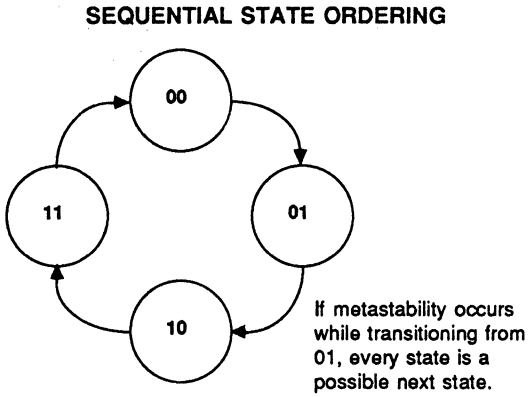


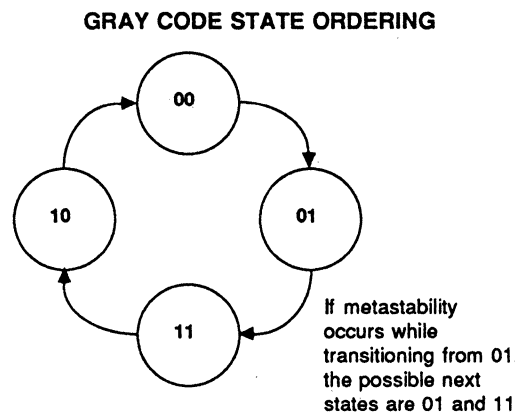


Figure 5.

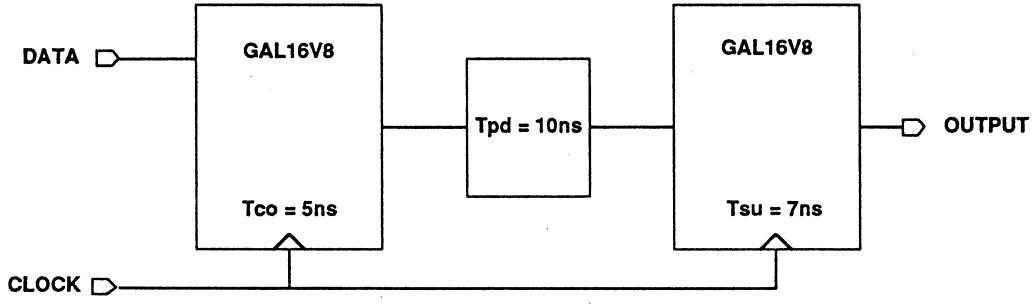


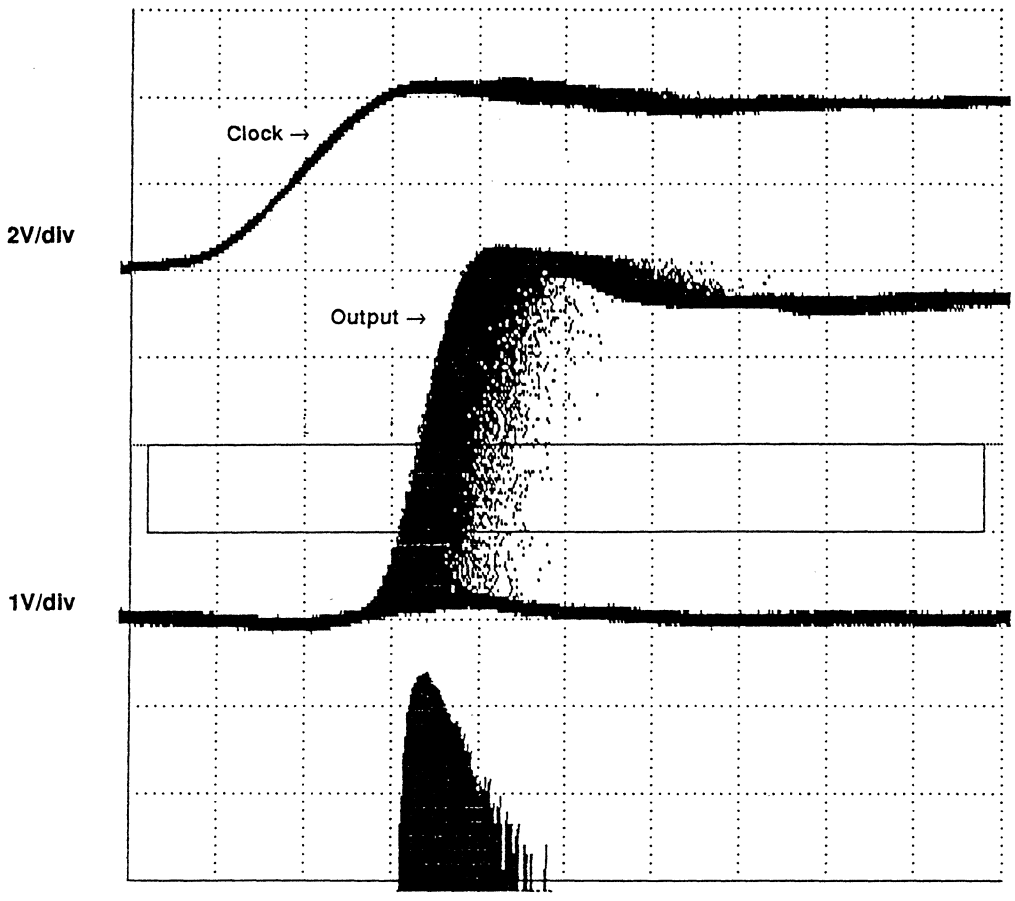
Figure 6.

```
MODULE metastable

TITLE 'Metastable Test
Pattern'

uOO Device 'P16R8';

d       PIN   2;
q1,q2   PIN   12,19;
        EQUATIONS
q1 := d;
q2 := d;
        End metastable
```

Listing 1a. Source equations

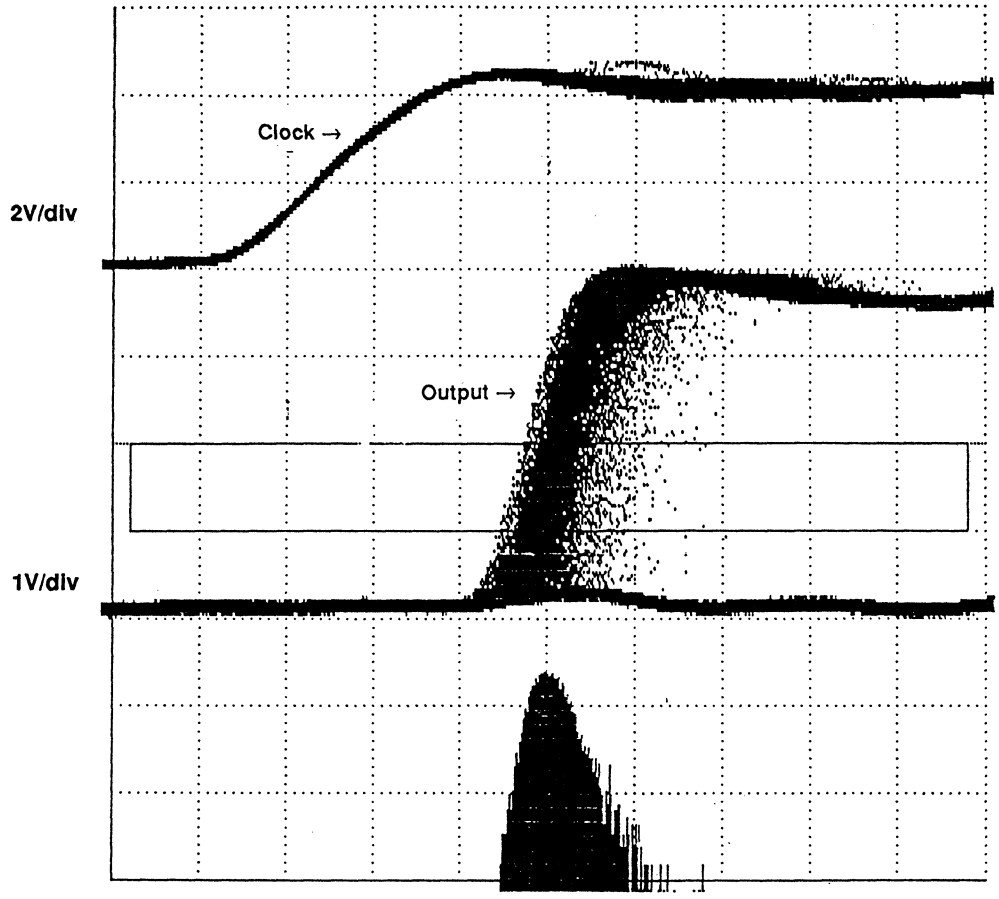
```
JEDEC file for: P16R8
Metastability Test Pattern*
QP20* QF2048* F0*
L0000 10111111111111111111111111111111*
L1792 10111111111111111111111111111111*
C07F4*
```

Listing 1b. JEDEC file



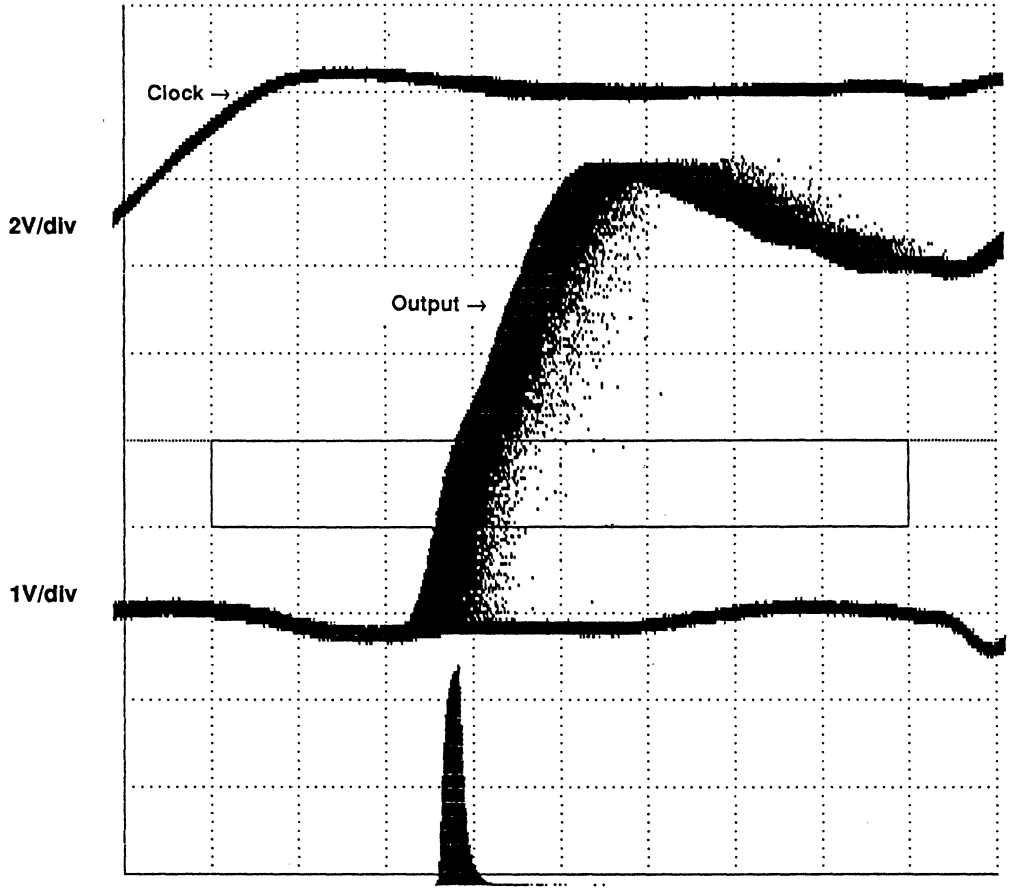
Plot 1. GAL16V8B-7 Metastable Output

Part #	Manufacturer	Δo (ns)	k2 (1/ns²)
GAL16V8B-7	Lattice	.44	5.0



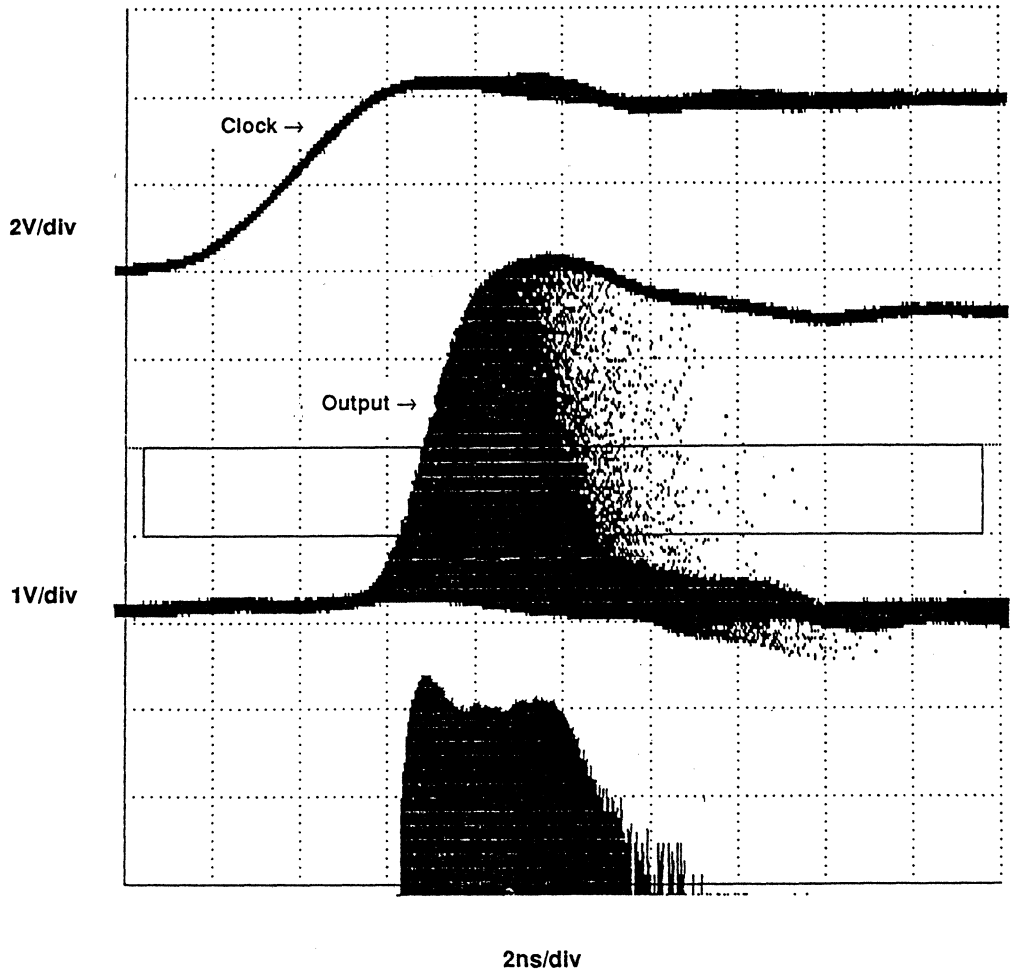
Plot 2. GAL22V10B-10 Metastable Output

Part #	Manufacturer	Δo (ns)	k2 (1/ns²)
GAL22V10B-10	Lattice	.51	5.2



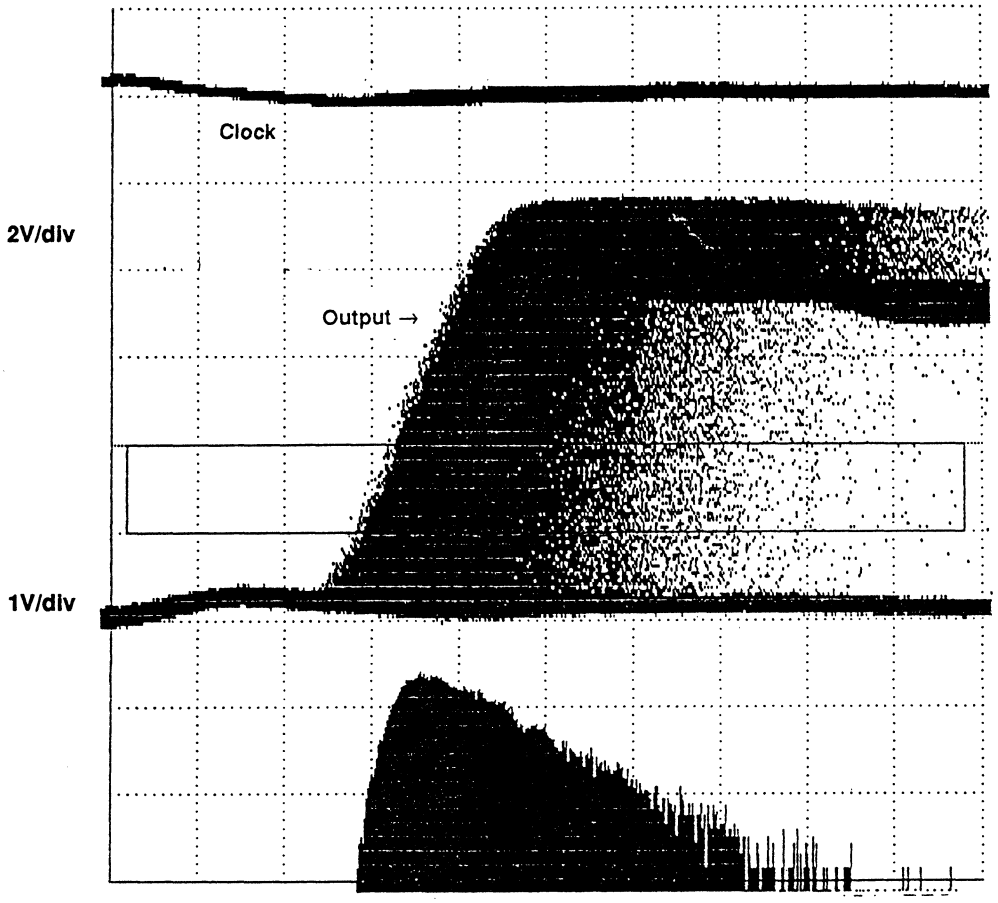
Plot 3. GAL6001-30 Metastable Output

Part #	Manufacturer	Δo (ns)	k2 (1/ns²)
GAL6001-30	Lattice	.22	7.3



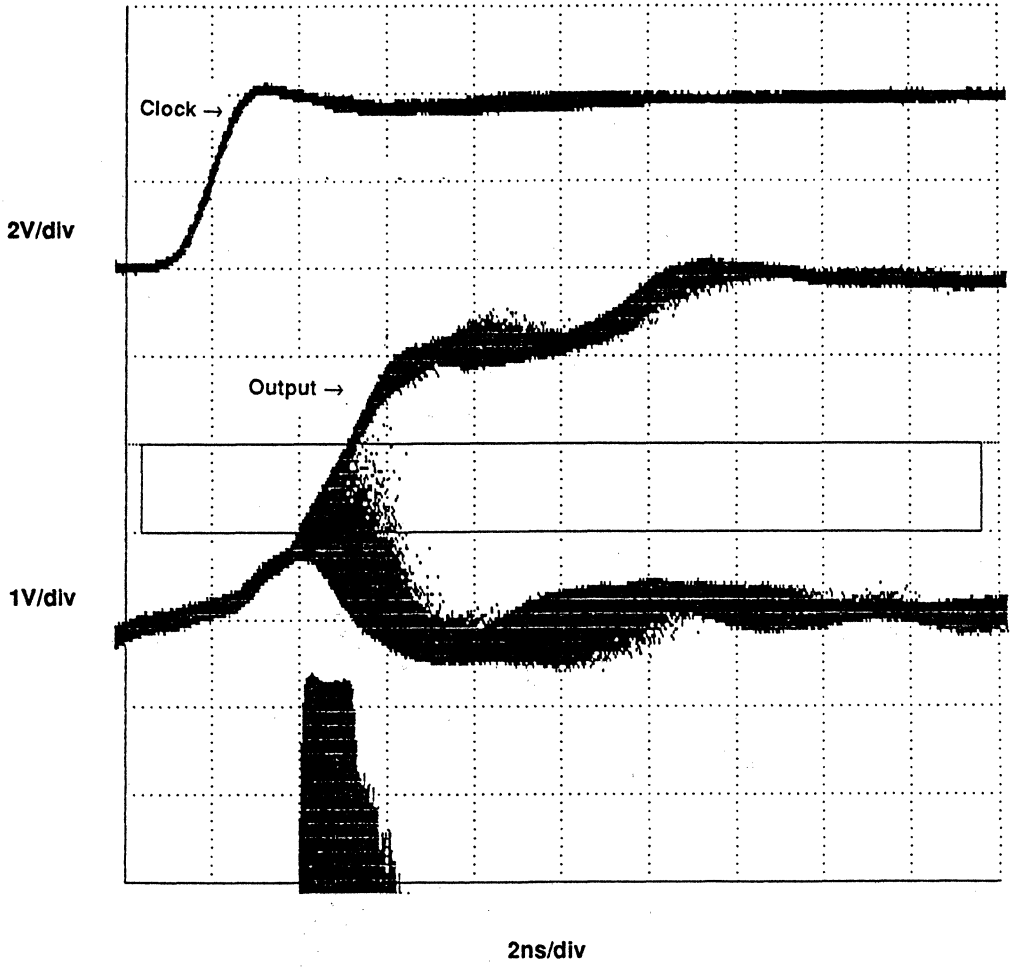
Plot 4. PAL16R8-7 Metastable Output

Part #	Manufacturer	Δo (ns)	k2 (1/ns²)
PAL16R8-7	AMD	1.2	2.5



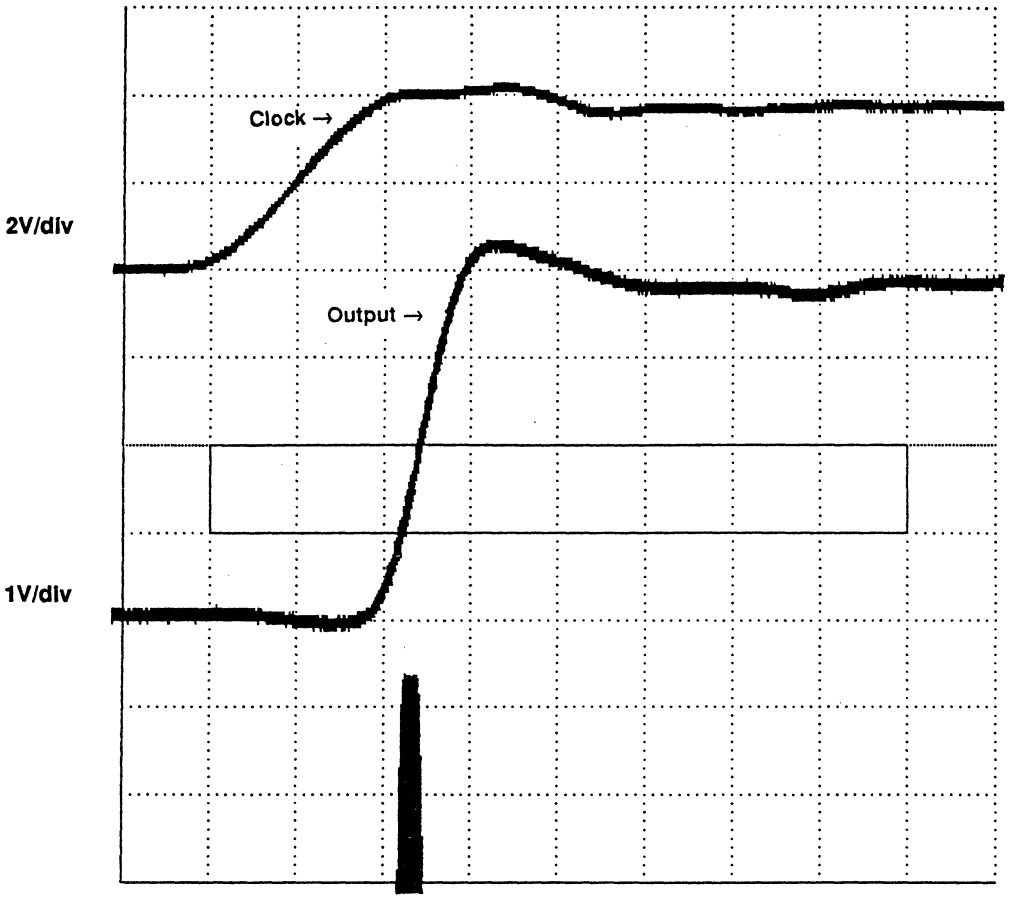
Plot 5. TIBPAL16R6-7 Metastable Output

Part #	Manufacturer	Δo (ns)	k2 ($1/ns^2$)
TIBPAL16R6-7	TI	1.5	1.5

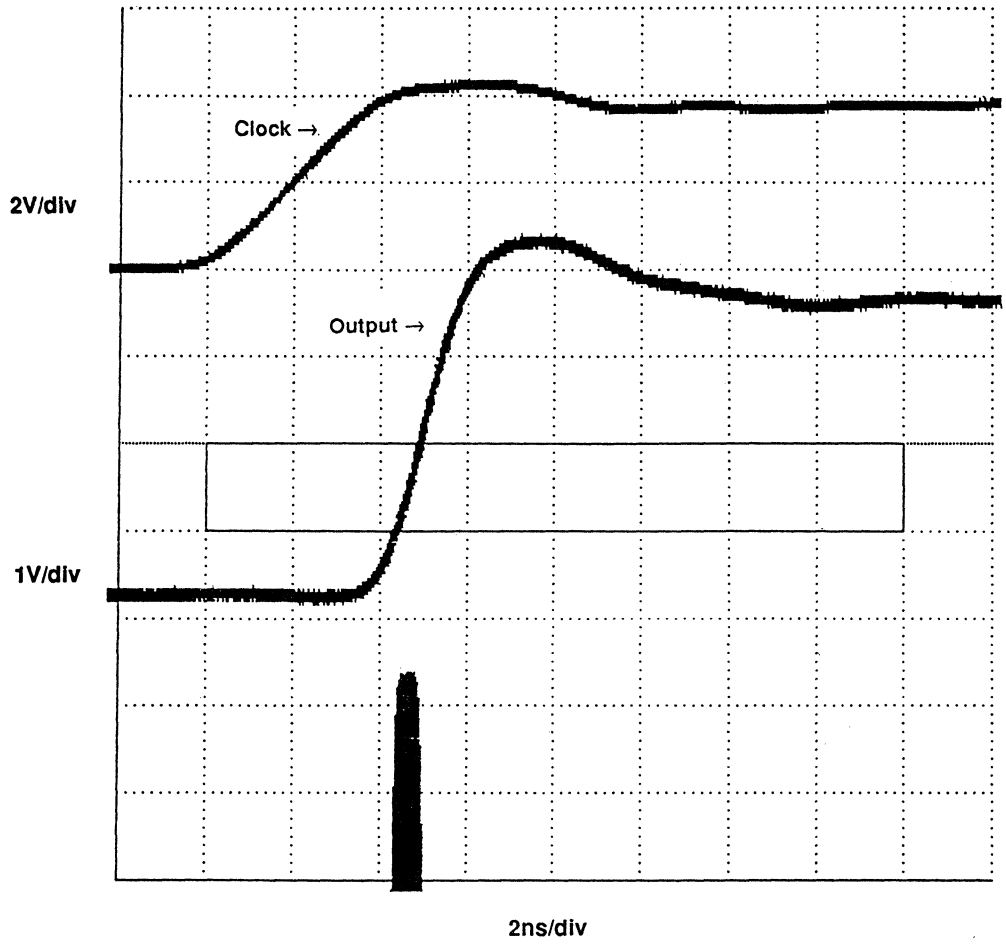


Plot 6. SN74AS74 Metastable Output

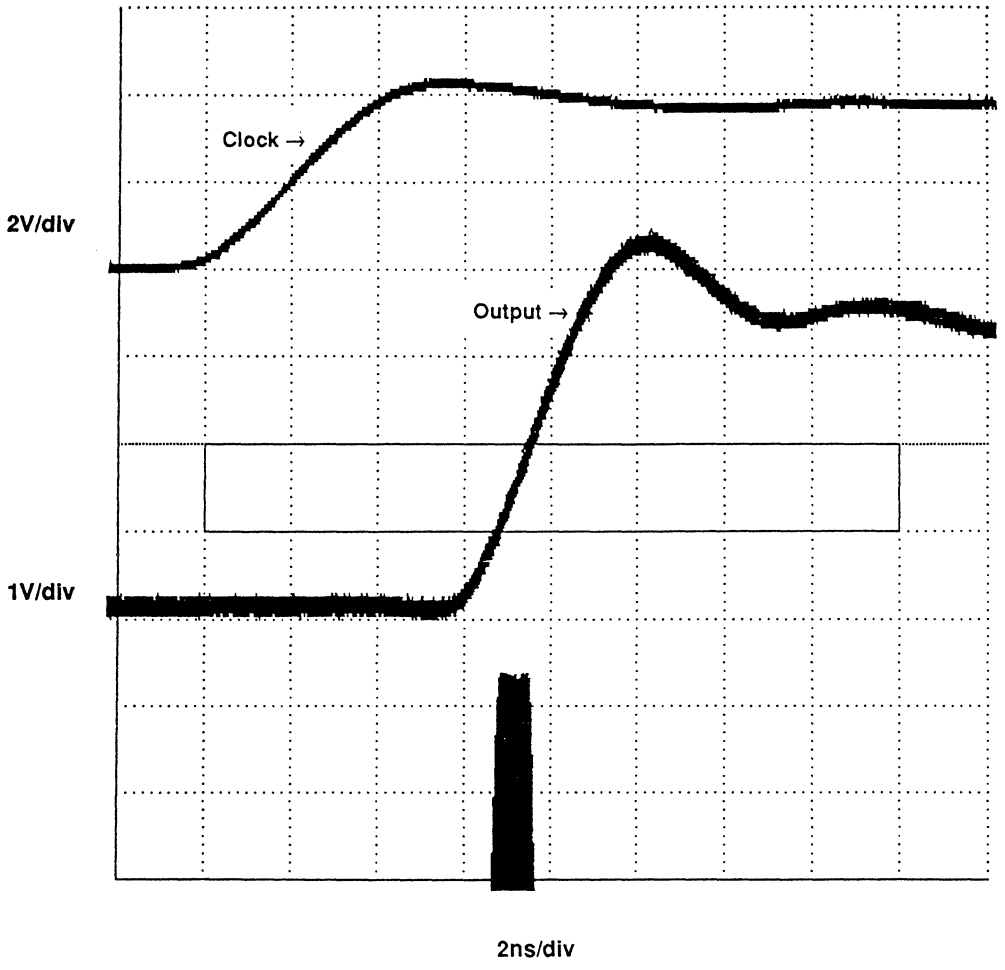
Part #	Manufacturer	Δo (ns)	k2 (1/ns²)
SN74AS74	TI	.91	3.5



Plot 7. Normal GAL16V8B-7 Transition



Plot 8. Normal PAL16R8-7 Transition



Plot 9. Normal SN74AS74 Transition

END

Latch-up Protection

INTRODUCTION

The Lattice GAL family has been developed using a high-performance E²CMOS process. CMOS processing was chosen for the GAL family to provide maximum AC performance with minimal power consumption. A drawback common to all CMOS technologies is the destructive agent, latch-up.

This brief defines the phenomenon of latch-up, how it manifests itself, and what techniques have been used to control it. Also described are three device features employed in the GAL family to eliminate the occurrence of latch-up as well as the results of an intensive investigation conducted to reveal the GAL family's tolerance to latch-up.

Latch-up is destructive bipolar device action that can potentially occur in any CMOS processed device. It is characterized by extreme runaway supply current and consequential smoking plastic packages. Latch-up is peculiar to CMOS technology, which integrates both P and N channel transistors on one chip.

In the doping profile of a CMOS inverter, parasitic bipolar (PNPN) silicon-controlled-rectifier (SCR) structures are formed. Figure 1 shows the process cross section of a CMOS inverter, as well as the bipolar components to the parasitic SCR structure. In steady-state conditions, the SCR structure remains off. Destruction results when stray current injects in to the base of either Q_1 or Q_2 in Figure 1. The current is amplified with regenerative feedback (assuming that the beta product of Q_1 and Q_2 is greater than unity), driving both Q_1 and Q_2 into saturation and effectively turning on the SCR structure between the device supply and ground. With the parasitic SCR on, the CMOS inverter quickly becomes a nonrecoverable short circuit; metal trace lines melt and the device becomes permanently damaged.

CAUSES OF LATCH-UP

It has been explained that parasitic bipolar SCR structures are inherent in CMOS processing. If triggered, the SCR forms a very low-impedance path from the device supply to the substrate, resulting in the destructive event. Two conditions are necessary for the SCR to turn on: The beta product of Q_1 and Q_2 must be greater than unity, which, although minimized, is usually the case; and a trigger current must be present. The cause of latch-up is best understood by examining the mechanisms that produce the initial injection current to trigger the SCR network. Figure 2 is a schematic of the parasitic bipolar network present in a CMOS inverter, where node "b" is the inverter output. It can be seen that two events might trigger latch-up: 1) the inverter output could overshoot the device supply, thereby turning on Q_3 and injecting current directly into the base of Q_2; and 2) the inverter output could undershoot the device ground, turning on Q_2 immediately. However, a third condition could also trigger latch-up; if the supply voltage to the P+ diffusion were to rise more quickly than the N-well bias, Q_1 could turn on. Within the device circuitry, overshoot and undershoot can be controlled by design. A problem area exists at the device

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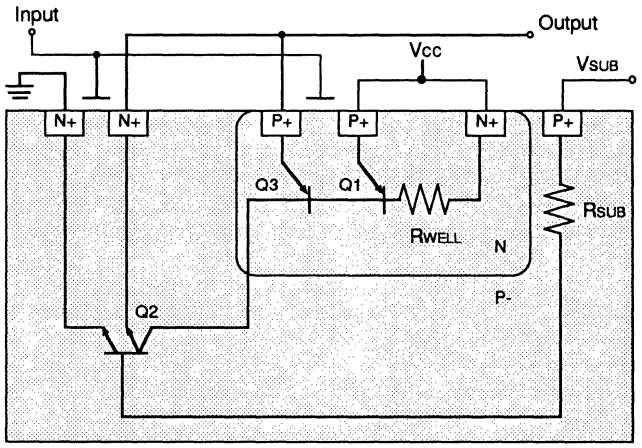


Figure 1. CMOS Inverter Cross-Section

inputs, outputs and I/Os because external conditions are not always perfect. Powering up can also be a potential problem because of unknown bias conditions that may arise.

With CMOS processing the possibility of latch-up is always present. The major causes of latch-up are understood and it is clear that if CMOS is to be used, solutions to latch-up will have to be created. As the technology evolves, solutions to latch-up are becoming more creative. Two of the more straightforward solutions are presented here.

One direct way to reduce the threat of latch-up is to inhibit Q_2 (Figure 1) from turning on. This has been accomplished by grounding the substrate and reducing the magnitude of Rsub through the use of wafers with a highly conductive epitaxial layer. While the technique is successful, the wafers are more expensive to manufacture, due to the extra processing required to form the epitaxial layers.

The extensive use of "guard rings" helps to collect stray currents which may inadvertently trigger an SCR structure. A disadvantage to heavy use of guard rings is the constraints placed on circuit design and topological layout, and the resulting increase in die size and cost.

THE LATCH-LOCK APPROACH

The intent of the GAL family was to implement cost-effective solutions to each major cause of latch-up. The goal was met through three device features.

The most susceptible areas for latch-up are the device inputs, outputs and I/Os. Extreme externally applied voltages may cause a P+N junction to forward-bias, leading to latch-up. The inputs, by design, are safe; but outputs and I/Os present a danger.

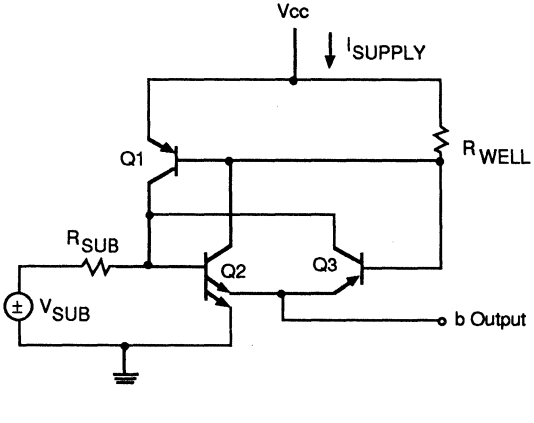


Figure 2. Parasitic SCR Schematic

To prevent latch-up by large positive swings on the device outputs or I/O pins, NMOS output drivers were used. This eliminates the possibility of turning on Q_3 (Figure 2) with an output bias in excess of the device supply voltage. Figure 3 contains the effective NMOS output driver and its switching characteristics. Note that the output does not fully reach the supply voltage, but still provides adequate V_{OH} margin for TTL compatibility.

To prevent negative swings on device output and I/O pins from forward-biasing the base-emitter junction of Q_2, a substrate- bias generator was employed. By producing a V_{sub} of approximately -2.5v, undershoot margin is increased to about -3V.

To insure that no undesired bias conditions occur with P+ diffusions, Lattice Semiconductor has developed proprietary Latch-Lock power-up circuitry, illustrated in Figure 4. In short, the drain of all P channel devices normally connected to the device supply is now connected to an alternate supply that powers up after the device N-wells have been biased and the substrate has reached its negative clamp value. This prevents any hazardous bias conditions from developing in the power-up sequence. After power-up is complete, the Latch-Lock circuitry becomes dormant until a full power-down has occurred; this eliminates the chance of an unwanted P channel power-down during device operation.

To determine the amount of latch-up immunity achieved with the three device features utilized in the GAL family, an intensive investigation was carried out. Each step was

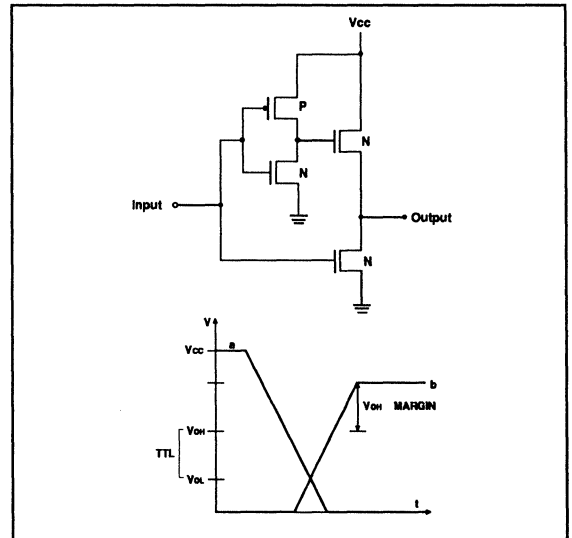


Figure 3. NMOS Output Driver

conducted at 25° and 100°C; inputs, outputs, and I/Os were sequentially forced to -8V and +12V while the device underwent fast and slow power-ups; devices were repeatedly "hot socket" switched with up to 7.0V.

Even under the extreme conditions specified, no instance of latch-up occurred. In an attempt to provoke latch-up, ± 50mA was forced into each output and I/O pin. The device output drivers were damaged in the battle, and still latch-up was not induced.

Based on the data, it is evident that the GAL family is completely immune to latch-up, even when subjected to a wide variety of extreme conditions, including current at inputs, outputs, and I/Os, power-supply rise time, hot-socket power-up and temperature.■

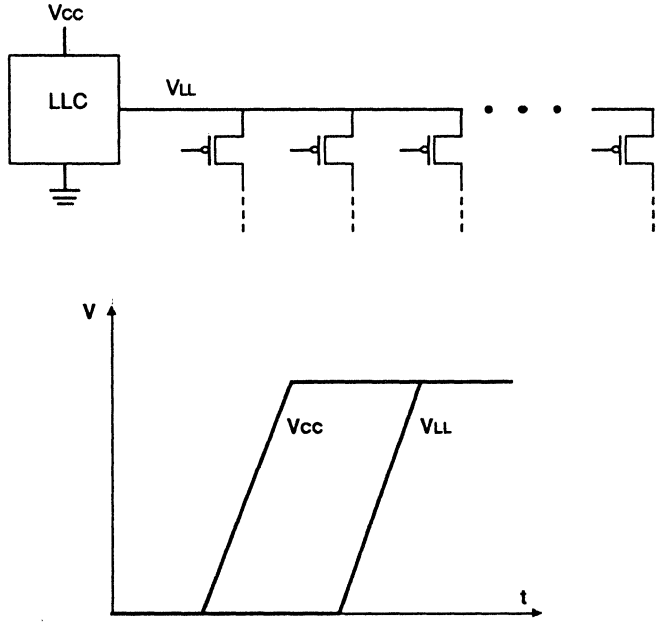


Figure 4. Latch-Lock Power-Up Circuitry

5

Section 1: Introduction to Generic Array Logic

Section 2: GAL Datasheets

Section 3: GAL Military Products

Section 4: Quality and Reliability

Section 5: Technical Notes

Section 6: Article Reprints

Section 7: General Information

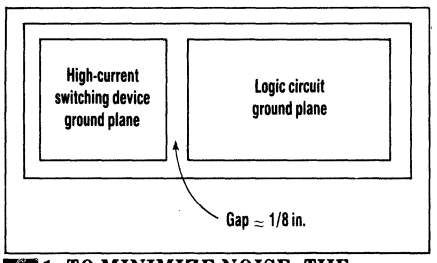
MAKE SURE THAT YOUR TURBO-CHARGED LOGIC SYSTEM WORKS BY PAYING AS MUCH ATTENTION TO PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES AS TO LOGIC DESIGN CONSIDERATIONS.

AVOID THE PITFALLS OF HIGH-SPEED LOGIC DESIGN

Modern high-speed systems demand modern high-speed logic families. Consequently, semiconductor houses have developed such product lines as ACT, FACT, and AS. But these systems also demand that the lay-out of their boards conform with the results of distributed-element theory, otherwise ringing, crosstalk, and other transmission-line phenomena render those systems inoperative. Meeting this second requirement necessitates something more than a new product introduction—it insists on a change in the way logic boards are engineered. The logic-systems designer and the board-layout designer must work hand-in-hand if a viable high-speed board or system is to be produced.

In the past, logic design and board layout were usually regarded as separate parts of the design process. First the system designer configured the logic, then the board engineer laid it out. That approach worked because slew rates were so low (0.3 to 0.5 V/ns) that crosstalk wasn't much of a problem; rise times were so long (4 to 6 ns) that ringing could settle down before a logic element could change state; and in general, the assumptions of lumped-element circuit theory usually worked out pretty well.

For systems designed with today's high-speed logic circuitry, those underlying assumptions no longer hold true. Today's slew rates are on the order of 2 to 3 V/ns, rise times are below 2 ns (frequently, below 1 ns), and transmission-line phenomena, such as ringing, can be a problem for trace



1. TO MINIMIZE NOISE, THE ground plane should be fragmented into separate areas for noisy high-current devices and for sensitive logic circuits. For best results, the number of signal lines that cross the gap between the fragments should be minimized.

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DESIGNING WITH HIGH-SPEED LOGIC

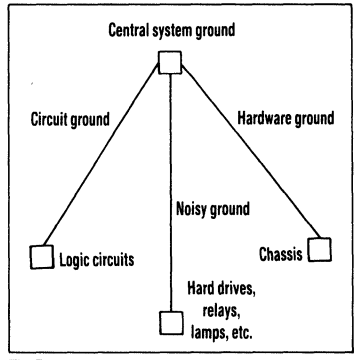
lengths as short as 7 in. As a result, logic designers must take certain steps:

- Use ground and power planes.
- Control conductor spacings to eliminate crosstalk.
- Make extensive use of decoupling capacitors.
- Pay attention to ac loading.
- Terminate lines properly to minimize reflections.

PLANE ADVICE

For high-speed logic, ground planes aren't simply suggested for reliable board performance—they are absolutely necessary. It's essential that one layer of the board be assigned for a ground plane and that it cover as large an area as possible. A solid ground plane lowers the ground-return-path impedance as well as the device-to-device ground pin impedance.

But a common ground plane for all of the circuitry in a system can cause problems by coupling noise from high-current switching devices into sensitive logic inputs. Therefore, the ground plane for such high-current devices as relays, lamps, motors, and hard drives should be separated from the logic ground. This can be accomplished by fragmenting the ground plane into discrete areas *(Fig. 1)*.



2. SEPARATE DEDICATED grounds should be supplied for the logic circuitry, noisy high-current devices, and the chassis. The three should come together at one point, the central system ground, which is usually located near the power supply.

But fragmentation causes problems of its own—it creates discontinuities in the characteristic impedance of any transmission line that crosses the separation between fragments. Therefore, for best results, boards should be laid out so that only two fragments are needed. The gap between those fragments should be kept as narrow as possible (an eighth of an inch works well in most applications), and the number of signal lines that cross the gap should be minimized. Designers should also bear in mind that through-holes and vias subtract from the effective area of the plane, increasing its effective impedance.

As with grounding, an entire layer of the board should be designated as a power plane. Even though it is at a different potential, the power plane should be implemented in accordance with the same concepts as the ground plane. Therefore, it should be fragmented when necessary to isolate noisy components from delicate logic circuits.

A WELL-GROUNDED SYSTEM

In addition to properly designed power and ground planes, high-speed logic systems require the establishment of a good, clean (low-

SIGNAL LINES BECOME TRANSMISSION LINES

For the transmission line model illustrated in the diagram, the rise time (t_R) is less than the line propagation delay (T_D). In other words, a complete TTL level transition will occur before the pulse is received at the receiving end of the line and reflections (ringing) will result. The voltage change at point A on the line is expressed in Eq. 1:

$\Delta V_A = \Delta V_{int} (Z_O / (R_O + Z_O))$

Where: V_{int} = internal voltage on the output of the driver;

R_O = output impedance of the driving gate;

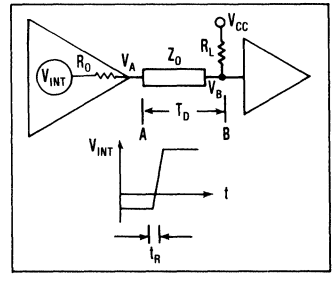
R_L = load impedance;

Z_O = the characteristic line impedance;

and V_A = the source voltage at the sending end of the line.

Because R_O is so small when compared to the line impedance, the change in voltage at point A (ΔV_A) will approximately equal the change in internal voltage (ΔV_{int}). This voltage transition propagates down the line and is seen at point B after the line propagation delay, T_D.

At point B, a portion of the wave will be reflected back towards point A in accordance with



the formula (Eq. 2):

Eq. 2

$\rho_L = (R_L - Z_O) / (R_L + Z_O)$

where ρ_L, called the voltage reflection coefficient (rho), is the ratio of the reflected voltage to the incident voltage.

After examining Eq. 2, it should be evident that $-1 \leq \rho \leq +1$. It should also be evident that there will be no reflected wave if $R_L = Z_O$—if the line is terminated in its characteristic impedance. Note that the reflected wave can, in principle, be as large as the incident voltage and of either positive or negative polarity.

This analysis holds true for the sending end of the line, as well as the receiving end. That is,

Eq. 3

$\rho_S = (R_O - Z_O) / (R_O + Z_O)$

DESIGNING WITH HIGH-SPEED LOGIC

noise) system ground for reliable performance. A clean system ground ensures less noise within the system, and thus ensures good, strong transistor margins. At least 10% of the ground connections on the pc card should be connected to the system ground to reduce card-to-ground impedance.

Like the ground and power planes of the individual boards, the overall grounding scheme should be fragmented with separate conductors provided for the various sections of the system. For example, all relays, lamps, hard drives, and other noise-generating devices should have their own separate ground path. The system's mechanical package (chassis, panels, and cabinet doors) should have a dedicated ground. And, of course, the logic circuitry should have a ground of its own.

Those three grounds should then come together at the central system ground point, which will usually be located near the power supply *(Fig. 2)*. This common-point grounding technique can also be very effective in reducing radiated interference (EMI and RFI).

TAMING CROSSTALK

Crosstalk—the undesirable coupling of a signal on one conductor to one on a nearby conductor—becomes an increasingly serious problem as slew rates go up. This signal coupling is made worse if the second trace has a high impedance or if the traces run parallel to one another for more than a few inches and are spaced less than 100 to 150 mils apart.

Crosstalk can be catastrophic to a logic board, sabotaging a conceptually flawless piece of logic design. For example, if a clock line and a data line run parallel to each other for more than several inches, and if the data line cross-couples or superimposes its signal onto the clock line, the device that the clock is driving may detect an illegal level transition.

Methods to reduce crosstalk are straightforward, though not particularly elegant. The coupling can be attenuated by separating the adjacent traces as much as possible. The trouble with this approach is that available board real estate often limits the possible separation to an inadequate amount.

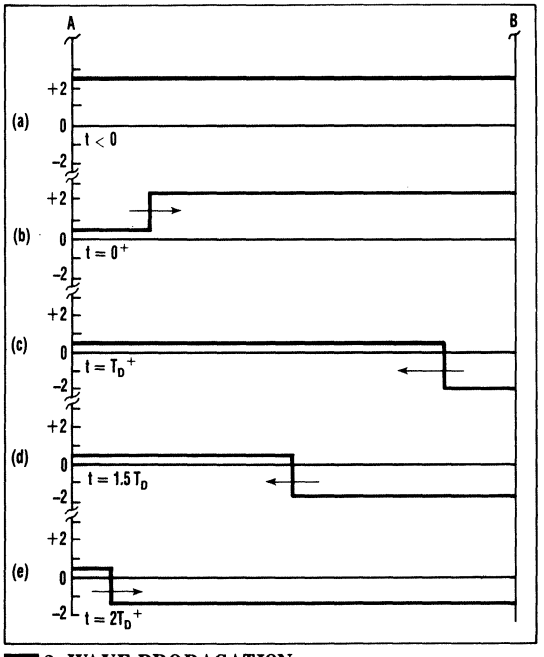
Ground striping, or shielding, is an effective way to reduce crosstalk and it makes better use of available board area. With ground striping, a ground trace (the stripe) is run between the two parallel traces to act as a shield. If ground striping is used, through holes to the ground plane should be placed every 1 to 1.5 inches along the ground strip to eliminate the possibility of inadvertently creating a stub or a high-frequency antenna.

Another step that can be taken to reduce crosstalk is to lower the impedance of those traces into which crosstalk is especially to be avoided. The lower the impedance that a trace presents, the harder it will be to cross-couple a signal into it.

Even with the use of power and ground planes on a pc board, decoupling capacitors must be used on the V_{CC} pins of every high-speed device. Those devices demand a nearly instantaneous change in current whenever they switch states. Because the power plane can't meet that demand, a high-quality decoupling capacitor is required, otherwise the switching will cause noise on the V_{CC} plane.

A 0.1-μF multilayer ceramic (MLC) or other RF quality (low-inductance) capacitor should be placed on every fast-slew-rate device as close to the V_{CC} pin as possible. The commercially available DIP sockets with built-in decoupling capacitors also work well in this application.

Most designers, when they think of loading at all, think in terms of dc loading—traditionally referred to as fan-out and fan-in. But that type of loading rarely presents a problem with today's state-of-the-art logic devices. Much more significant when designing with high-speed logic are input and output ac loading.

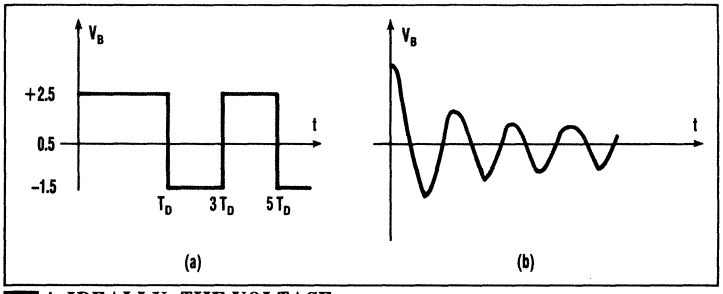


3. WAVE PROPAGATION along a transmission line occurs as follows: Prior to time zero, there is a steady-state voltage of 2.5 V dc on the line (a). At t = 0, the voltage at point A drops to 0.5 V, sending a negative pulse of -2 V toward point B (b). At t = T_D, that negative pulse is reflected from point B. It adds algebraically to the 0.5 V on the line and sends a -1.5-V pulse back toward point A (c). The reflections then continue as in (d) and (e).

INPUT CAPACITANCE

Because the input capacitance of a device impacts the overall performance of the logic circuit, it should be examined before a particular device is selected for a design. To ensure specified performance, the total load capacitance that a device drives—including the distributed ca-

DESIGNING WITH HIGH-SPEED LOGIC



4. IDEALLY, THE VOLTAGE at point B oscillates forever between +2.5 V and -1.5 V (a). In reality, it will be a damped ringing (b).

pacitance of the trace—shouldn't exceed the device's specified capacitive load. Most high-speed logic devices have a maximum loading of 50 pF. As a rule of thumb, the maximum load on any logic element should be no more than four to six devices for best speed/load performance. However, there are some high-slew-rate devices on the market that have higher output drive capabilities.

Beware Of Autorouter

The most common reason for not following the board-layout principles mentioned so far is having an autorouter do the layout. Autorouters do what they were designed to do very well: They place traces so as to make the most efficient use of the pc-board real estate. But most autorouters don't have the capability to determine which devices are high-speed and which are not. This is where the logic designer must step in and lay out sections, or islands, of high-speed logic by hand in order to avoid the pitfalls of designing with high-speed logic.

Transmission Lines

In addition to the common-sense layout considerations discussed so far, designers of high-speed systems must have at least a basic understanding of transmission lines and proper termination techniques *(see "Signal Lines Become Transmission Lines," p. 76)*. The reason: As frequencies go up, wavelengths come down to the point where they are of the same order as circuit-board dimensions. Once that happens, any connection between devices should be considered a transmission line. The lumped-element assumption is simply invalid above that point.

The most common consequence of failing to consider the distributed nature of a high-speed logic board is ringing, which is caused by multiple reflections from the ends of unterminated transmission lines. An unterminated line has no load impedance ($R_L = \infty$) and is therefore an impedance-mismatched line. The behavior of this line when connected to a device with a fast slew rate can be understood from the following example: Prior to time zero, there's a steady-state voltage of 2.5 V dc at all points on the line *(Fig. 3a)*. At $t = 0$, an initial TTL voltage transition from 2.5 V to 0.5 V occurs at point A *(Fig. 3b)*. Time T_D later, the signal reaches point B and is reflected by the load reflection coefficient, ρ_L.

The input impedance of the device at point B is very high with respect to Z_0; R_L can be approximated by infinity. By plugging into Eq. 2 from the box *(p. 76)*, the reflection coefficient approximately equals +1. In other words, the voltage reflected by the load is equal to the incident voltage *(Fig. 3c)*. The reflected wave passes back along the signal path toward point A *(Fig. 3d)*.

Repeating the calculations for the sending end of the line (point A), where $R_0 \simeq 0$, you get a value for the source reflection coefficient, ρ_S, of -1. In other words, there are reflections from the source as well as the load,, but the source reflects the inversion of the wave that is incident upon it *(Fig. 3e)*.

Looking just at the behavior of the signal at point B, the single-step volt-

RULES TO REMEMBER

The following ten rules summarize everything the logic designer needs to know when designing with high-speed CMOS.

1) Keep signal interconnections as short as possible.

2) Use a multilayer PCB.

3) Provide ground and power planes. Discontinuities in the planes should be avoided because reflections can occur from abrupt changes in the characteristic impedance.

4) Fragment the ground and power planes to supply separate sections for high-current switching devices.

5) Use decoupling capacitors on every high-speed logic device (0.1 μF MLC type) located as close to the V_{CC} pin as possible.

6) Provide the maximum possible spacing among all high-speed parallel signal leads.

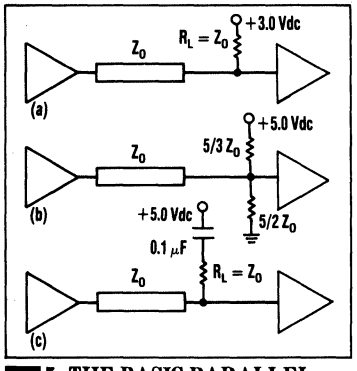
7) Terminate high-speed signal lines where $t_R < 2T_D$.

8) Beware of ac loading conditions within the design. Exceeding the manufacturer's recommended operating conditions, especially for capacitance, can cause problems.

9) When using parallel termination, put bends in all high-speed signal runs that go to more than one load. Use a termination load at the absolute end of the line.

10) Create islands of high-speed devices on the pc board. This simplifies board layout and ropes-off the high-speed areas.

DESIGNING WITH HIGH-SPEED LOGIC



5. THE BASIC PARALLEL termination scheme works well but requires a separate 3-V supply (a). The Thevenin equivalent eliminates the need for a separate supply, but dissipates extra power from the regular 5-V supply (b). The use of a capacitor cuts dc dissipation altogether while supplying ac termination (c).

age transition at t = 0 leads to an endlessly oscillating signal with a total voltage swing of 4.0 V—twice the original level transition. The voltage doubling comes about because the voltage at point B is the sum of the incident and reflected waves at that point *(Fig. 4a)*. Actually, because of the non-ideal nature of a real circuit board (finite input and output impedances, losses in the transmission lines, and so forth), ρ_L will be less than +1, and ρ_S will be greater than −1. As a result, the reflections will become successively smaller, causing the familiar damped ringing condition *(Fig. 4b)*.

If the ringing amplitude is large enough, it can cause the receiving device to see an illegal level transition and possibly result in spurious logic states occupying the logic design. In some cases, the amplitude of the ringing can actually be large enough to damage the input of the receiving device.

TERMINATE YOUR TROUBLES

The way to eliminate ringing on a transmission line is to terminate the line in its characteristic impedance at either the sending or receiving end. The most common way to terminate a line is with a parallel termination at the receiving end *(Fig. 5)*.

In the configuration *(Fig. 5a)*, $R_L = Z_0$ and R_L is pulled up to 3 V dc. In principle, R_L could be tied to ground, but TTL-compatible devices could not then supply the necessary drive.

Solving for ρ_L *(Eq. 2)*, it can be seen that $\rho_L = 0$. Terminating a line in its characteristic impedance results in a reflection coefficient of zero, which means that there will be no reflections or distortions on the line. Other than the time delay, T_D, the line will act as if it were a dc circuit. It's important to note that even though devices or gates may be placed at any location on the line, the terminating resistor should be placed at the end of the line. In no case should the line be split like a Tee to feed several devices in parallel *(Fig. 6a)*. Instead, it should be serpentined to feed them sequentially *(Fig. 6b)*.

The 3-V power source shown *(Fig. 5a)* appears at first to be a major drawback, but R_L and the power supply can be expressed as a Thevenin equivalent running off the system power supply of 5 V dc *(Fig. 5b)*. This variant works well, but the designer should bear in mind that it dissipates additional power.

REDUCING DISSIPATION

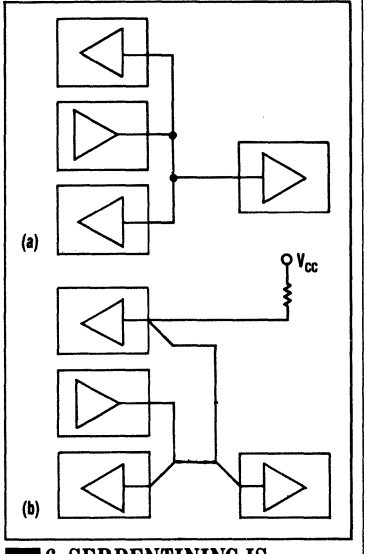
A solution that dissipates less power than either of the others uses a capacitor to cut the dc dissipation to zero *(Fig. 5c)*. The recommended capacitor is a 0.1-μF MLC type. Several manufacturers produce both capacitor-resistor and pull-up/pull-down termination packs. The pull-up/pull-down packs usually come in a single in-line package (SIP) with pins on 0.1-in. centers, while the capacitor-resistor combination comes in a standard 16-pin DIP. The most common SIP pull-up/pull-down resistor values are 220Ω/330Ω, 330Ω/470Ω combinations.

An alternative to a parallel termination at the receiving end is a series termination at the sending end *(Fig. 7)*. The idea behind serial termination is to make $\rho_S = 0$ and $\rho_L = +1$. To do so, R_L is made equal to infinity (left unterminated) and a series resistor is added at the source to make the overall source impedance equal to the characteristic impedance of the line—that is, $R_S + R_O = Z_{OL}$.

Making $R_S + R_O$ equal to Z_{OL}, of course, creates a voltage divider, which puts half of the signal amplitude across the line and half across the series combination of R_S and R_O. Therefore, with the series termination, the amplitude of the transmitted wave is half of what it would be without the termination.

Interestingly enough, the unterminated receiving end of the line precisely compensates for this halving of the amplitude. The reason is as follows: At the receiving end, the half-amplitude wave is received and a half-amplitude wave is reflected. But bear in mind that those are two separate waves whose amplitudes add at the point of reflection. As a result of this addition, the only thing seen at the receiving end of the line is a full-size pulse.

The main disadvantage of a series termination is that the receiving gate or gates must be at the end of the line—no distributed loading is possible. The obvious advantage of a series termination over a parallel one is that a series termination doesn't



6. SERPENTINING IS essential when terminating a line. Never split the line to feed parallel devices (a). Rather, feed them sequentially with a serpentined line (b).

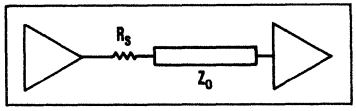
6

DESIGNING WITH HIGH-SPEED LOGIC

require any connection to a power supply.

Transmission-line effects must be taken into consideration whenever line propagation delays get up to the point where a signal transition can be completed before that signal can travel down a line, be reflected, and travel back to its starting point. In other words, lines must be terminated when,

$2T_D = T_R$.



7. THE SERIES termination needs no pull-up supply. Its main disadvantage is that it can't handle distributed loads.

CALCULATING DELAY

Taking 2 ns as a typical rise time for a state-of-the-art high-speed logic device, how long can a board trace get before its propagation delay gets to be 1-ns long? For a pc board with a continuous ground plane and a signal trace on the adjacent layer, the propagation delay depends on only one variable, the dielectric constant of the board material. That delay time is given by:

$$t_{PD} = 1.017\,(0.475\,e_R + 0.67)^{1/2}\ \text{ns/ft}$$

For a typical board constructed of FR4 material, e_R (the dielectric constant) is 4.7 to 4.9. If an average e_R of 4.8 is used in the equation, then t_{PD} turns out to be 1.75 ns/ft, which works out to 6.86 in./ns. As a rule of thumb, then, any line that is over 7 in. long should be considered a transmission line and approached accordingly.□

Jock Tomlinson, senior applications engineer at Lattice, holds a BSEE from Colorado State University.

Extending the 22V10 EPLD

An extendable device family allows gate and I/O counts to be boosted without major changes in board layout

The 22V10 device architecture is now one of the industry standards in programmable logic devices. The 22V10 owes its popularity to a number of architectural features that bring versatility and flexibility to system design. The Output Logic Macro-Cell (OLMC) is perhaps the most revolutionary feature of the 22V10 architecture. OLMCs eliminate such architectural constraints as insufficient product-term access, fixed output polarity, limited three-state control, and poor control of registered outputs. The OLMC at any device I/O pin is functionally identical to any other. Additionally, any I/O can be used as a feedback path into the AND array.

Asynchronous reset is another attractive feature of the 22V10. One reset signal is common to all registered OLMCs and operates independently of the dedicated clock input. This signal is taken from the AND array and may be generated via a product term. Registered OLMCs respond immediately to a reset signal. In addition, one preset signal is common to all registered OLMCs and operates on the arrival of a valid clock input. This signal is taken from the AND array and may be generated by a product term. Registered OLMCs respond only on the arrival of a valid clock input.

Along with a minimum of eight product terms per OLMC in all modes, two outputs have access to 10 product terms per OLMC in all modes, another two have access to 14 product terms, and the center two outputs have access to 16 product terms. Each OLMC's output driver has a unique enable/disable signal that is taken from the AND array and that may be generated via a product term. All OLMCs respond immediately to the arrival of a valid enable signal generated externally or internally.

The three members of Lattice's GAL22V10 series—the GAL18V10, GAL22V10, and GAL26CV12—are high-speed, EECMOS PLDs. Each is based on the standard 22V10 architecture; their differences involve the number of I/Os, pins, and product terms offered. The GAL18V10 is a 20-pin version of the 24-pin GAL22V10. It contains eight dedicated input pins (four less than the 22V10) and 10 I/O (the same as the 22V10). The 28-pin GAL26CV12 has two more dedicated input pins and two more I/O pins than the GAL22V10. The GAL26CV12 in a PLCC package requires no more space than many lower-density PLDs.

The EECMOS GAL18V10 and GAL26CV12 consume just 75 mA and 90 mA typical I_{CC}, respectively—50 percent less power than bipolar alternatives. The programmable AND arrays are proportional to the pin count of each device. The arrays are 96 × 36, 132 × 44, and 122 × 52 for the GAL18V10, GAL22V10, and GAL26CV12, respectively.

The first job that a designer has in selecting the right 22V10 device for a system is to evaluate the size and complexity of the design as well as system speed and power requirements. PLDs excel in applications that have a number of SSI parts with low gate counts and combinational logic that optimally fit into a single device.

The GAL18V10 features an equivalent gate count of 450 to 550 gates, along with eight to 18 inputs and one to 10 outputs. The GAL22V10's equivalent gate count is 550 to 750 gates; it offers 12 to 22 inputs and one to 10 outputs. The GAL26CV12 has an equivalent gate count of 650 to 850, 14 to 26 inputs, and one to 12 outputs. If a design has a fairly low gate count and relatively small I/O requirements, the GAL18V10 is the best choice. Should additional inputs be required without any additional output requirements, the best place to start is the GAL22V10. If gate count, input, and output requirements are large, the GAL26CV12 is recommended. For designs with larger requirements, some combination of the three devices will meet design needs.

The final stages of the evaluation cycle often reveal problems with a design. Typically, such problems include the omission of a critical input signal or a need for more output signals. Such adjustments are best accomplished by repatterning the fuse map of the PLD. This type of design fix is limited by the number of unused PLD pins available and by the flexibility of the PLD's internal fuse-map array. If the PLD has not been fully used, a new fuse-map pattern can often be implemented without any board-level redesign. If additional I/O is necessary, however, additional parts usually are needed.

The GAL22V10 family is well suited for situations in which greater overall complexity and lower power consumption must be achieved without a corresponding increase in device count or real estate use. With an extendable family, gate and I/O count can be boosted without major changes in board layout.

When designers are under pressure to produce a design quickly, the design cycle is much more chaotic. Many times, a designer will simply grab the closest part and use either single parts or multiple parts to build the circuit. When the final product has been in production for a few months, the manufacturing-engineering group then must come to grips with the challenge of cost reduction. In some cases, these cost-reduction efforts can also result in reliability gains and performance enhancements.

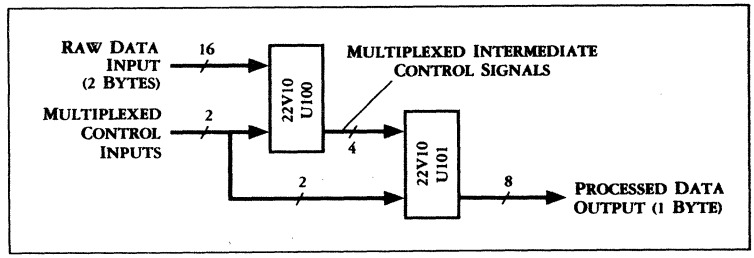


Figure 1. In this example, two 22V10 devices are needed to provide enough inputs and outputs for a state machine.

For example, suppose a designer, in a rush to build a state machine for control in a pipeline application, used two 22V10s to implement the function (Figure 1). The objective of the design is to take 16 data-input bits and two control bits to generate eight data-output bits. In the first device, 16 data inputs and two control inputs were used to generate four encoded outputs. Since the first device was output-bound, only four of the eight required data bits could be generated. The second device was used to take the four encoded outputs from the first device and the two control inputs to generate the required eight data output bits.

The above design can be implemented in a single 26-pin device (Figure 2). The 16 data-input bits and the two control bits are fed directly into the GAL26CV12, and the remaining two pins can be used for the required eight data-output bits. Not only does this approach offer the obvious advantage of reduced board space, it also saves more than 0.5 W of power and removes an entire package delay. Enough power reduction can mean power-supply cost savings and an indirect increase in board reliability. Performance enhancement results in an extension of the life of an already mature system.

■ A 10-Bit Counter Design

A second design example involves a standard 10-bit counter. A 10-bit counter can be used to provide location-by-location access of up to 1,024 addresses or to provide divide-by-two to divide-by-1,024 clock frequency reduction and distribution. A 10-bit counter can also be used to identify up to 1,024 sequential edge-identified events.

These counters generally are implemented in one of two ways—with multiple 20V8 devices or with a single 22V10 device. If a 22V10 is used, enough inherent flexibility remains for the implementation of asynchronous reset and synchronous preset functions. For a 10-bit counter built with a 22V10 that generates an output for every clock phase, which is appropriate for the implementation of a "watchdog" timer function for real-time activities, eight dedicated inputs remain unused. If that same counter were built with a 20-pin GAL18V10, four pins of real estate could be saved and power use cut by 0.5 W.

Suppose that same 10-bit counter is used to signal the "half-full" and "three-quarter full" points of a 1,024-location circular buffer. Two independent event codes will be needed to decode and generate single clock-width pulses at these two points in the buffer.

Such a part requires 12 outputs. Previously, multiple 22V10 devices or the combination of a 22V10 component and another PLD have been used for the task. Now, the part can be built with a single 28-pin GAL26CV12, yielding a power savings of about 1 W and eliminating one package delay. ■

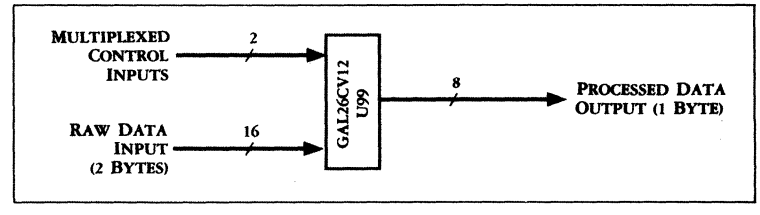


Figure 2. Here, a single 26CV12 replaces two 22V10s and reduces delays and power-supply requirements.

ELECTRONIC DESIGN EXCLUSIVE

In-circuit logic device can be reprogrammed on the fly

Compatible with 5-V systems, an EEPROM-based chip allows designers to update systems in situ, with 100% testing and observability.

Of the multitude of ways available for reconfiguring logic systems on circuit boards, none has ever proved entirely satisfactory. Changing dozens of DIP switches or jumper settings manually can be a nightmare. Electrically erasable or battery-backed memory can do the job at least in part, but the use of memory bits is limited in most cases to controlling signal flow in the parts of a system where speed is not critical.

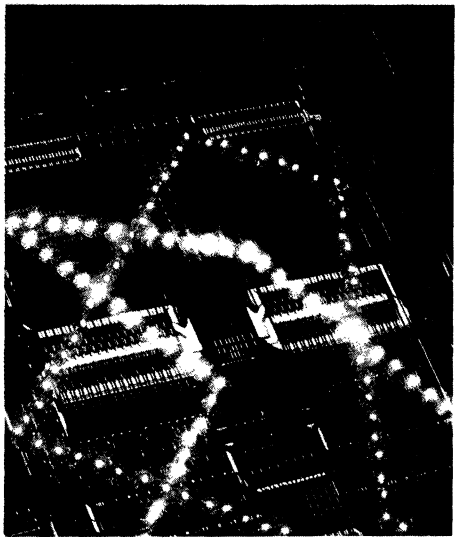
Memory bits do have their place in controlling such tasks as decoding I/O ports, enabling and disabling features, and selecting a memory bank, but those jobs are mutually exclusive: Designers have to decide which one they want to control through the use of memory.

The few logic devices now using UV EPROM cells cannot be reprogrammed without being removed from the system. Nor, if sealed in windowless plastic packages, are such chips 100% testable. Even with windows, they usually have to be removed from the board for erasing and reprogramming, because the 12- to 21-V programming voltage risks damage to other components on the board. Other difficulties can arise too with these techniques, such as mechanical switch failures, wire breaks or shorts, dead batteries, and mishaps that occur when technically unskilled users try their hand at reconfiguring or fixing circuitry.

A new 24-pin chip does away with all those pitfalls. By combining programmable logic circuits with 5-V electrically erasable CMOS memory, it opens up all kinds of options in reconfiguring a system. The ispGAL16Z8 not only is reprogrammable in circuit but also is 100% testable—a big plus. Propagation delays of a mere 25 to 35 ns mean that the reprogrammable device can be used in data paths where speed is critical, so that even the system's basic logic flow can be altered in an instant.

The chip is the first in a planned family of in-system reprogrammable devices, and its flexibility is limited only by the designer's imagination. Logic designers need not be restricted to that last etch on the board, and final testing no longer presents so many problems.

Because the new chip combines CMOS with electrically erasable floating-gate and high-speed logic, it runs at speeds associated with bipolar chips, but consumes significantly less power—450 mW maximum and 350 mW on standby—than do most bipolar chips. The 16Z8 is similar to the company's earlier programmable logic device, the 20-pin GAL16V8. Four additional pins in the 16Z8 control in-system programming and diagnostic testing (Fig. 1). A proprietary state-machine–based interface controller on the chip handles all programming and testing. It also makes possible, through the four pins, the in-system observability and controllability



that are such powerful diagnostic aids.

Like the 16V8, the new chip has a core consisting of a standard AND array plane and eight programmable output logic macrocells; it adds 5-V E^2CMOS programming circuitry. Each programmable output macrocell gives the designer five configuration options, among them output polarity (active high or active low), feedback, combinatorial logic, registered outputs and input selection. Either all the outputs are connected to one Output Enable signal, or separate product terms provide individual enabling controls.

The new chip also emulates all common 20-pin architectures similar to Monolithic Memories' programmable array logic. Its programming software and hardware support come through the standard PLD development packages. Because its fuse map is compatible with that of the older chip, the new chip accommodates the latter's software. (Data I/O is the first third-party vendor to offer updated programming; other companies are expected to follow suit shortly.)

SERIAL PORT SIMPLIFIES INTERFACE

The new chip can be programmed over a −55°C to −125°C operating range and can undergo at least 10,000 erase-write cycles. Given its 100% reprogrammability, yields of 100% in ac and dc parameters are guaranteed, as is a programming time of less than 1 second. The 5-V programming circuitry generates the necessary higher voltages internally and also shapes waveforms so that the device can be programmed through the four-pin interface without high-cost, high-voltage external hardware.

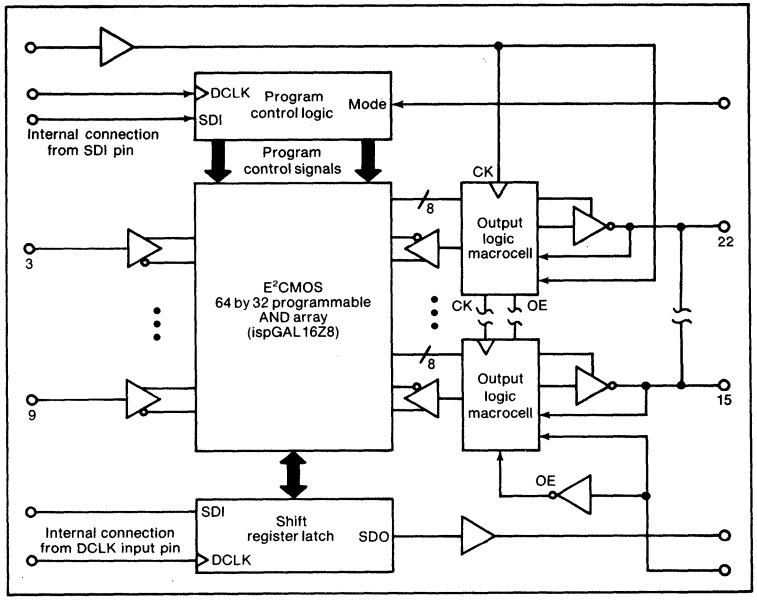
The four-pin interface controlling programming and diagnostics is compatible with Monolithic Memories' JEDEC-standard "diagnostics on chip." By eliminating multiplexed data paths, the interface optimizes data propagation. It has four basic functions: diagnostic preload, program shift, program read, and program write. The chip's state machine controls the sequence with information from three of the four signal pins: Serial Data In (SDI) for programming; Mode for loading; and Diagnostic Clock (DCLK) for diagnostics. The fourth pin, Serial Data Out (SDO), for data shifting, comes into play when the serial scan data has to be expanded into a loop (Fig. 2).

When the chip receives a Power on Reset signal, the state machine resets to the normal state to prevent unwanted writes at power-up. A user-controlled Reset signal makes the state machine move to the normal state from any state when the Mode pin is a logic 1, SDI is a logic 0, and DCLK has a rising edge.

The four interface signals are relatively simple to gen-

Typical write programming sequence

	Enter programming states from the normal state
Step 1	Mode is TTL high; SDI is TTL high; DCLK is clock Diagnostic: Preload state (just passing through)
Step 2	Mode is TTL high; SDI is TTL high; DCLK is clock Program: Shift state
Step 3	Mode is TTL low; SDI is address and data bits; DCLK is clock Program: Shift state (Load shift register latch with 82 data bits and 6 address bits) (Note: SDO data field is "don't care")
Step 4	Mode is TTL high; SDI is TTL high; DCLK is clock Program: Read state (just passing through)
Step 5	Mode is TTL high; SDI is TTL high; DCLK is clock Program: Write state (Write begins immediately upon entering Program: write state) (Time-out write pulse)
Step 6	Mode is TTL low; SDI is TTL high; DCLK is clock Program: Read state (End write)
Step 7	Mode is TTL low; SDI is "don't care"; clock is DCLK Program: Shift state (Read address; execution of verify; shift register latch is loaded)
Step 8	Mode is TTL low; SDI is next 88-bit word; clock is DCLK. Program: Shift state (Shift out 82 data bits and 6 address bits; observe SDO)
Step 9	Repeat steps 4–6 for each row address of verification



1. The 24-pin ispGAL16Z8 starts with an E^2CMOS programmable AND array at its core and eight output macrocells. Then it adds a serial diagnostic and programming port and 5-V programming circuitry.

erate, needing only the output ports of a standard single-chip microprocessor and a little support software. A typical serial scan programming-and-diagnostic control loop can take on a system with several devices (Fig. 3). In its normal state, the 16Z8 works like a standard PLD, remembering the last update to the E^2CMOS logic and functioning in the system as programmed. In the diagnos tic preload state, the chip latches the macrocells' presen condition and, with DCLK, lets diagnostic test informa tion move from SDI to SDO. SDI is loaded into the least significant output register on DCLK's rising edge. Most significant register data is shifted out through SDO. When the chip returns to normal, its outputs resume their preload state.

SHIFT, READ, AND WRITE

In the program shift state, one row of data in the array is shifted into SDI, with the appropriate array data moving first, followed by the row address field. To configure a device completely, each array location must be filled with the appropriate data. Any data already in the serial shift register is shifted out through SDO for cascading or for verifying a device.

In the program read state, one row of the array is transferred in parallel into the serial shift register, whose contents are transferred out of the selected row in the array. Returning the chip to the program shift state loads the shift register and lets the user verify the device. However, if the chip goes to the program write state, the register's data is programmed to the selected row in the array and its contents remain unchanged.

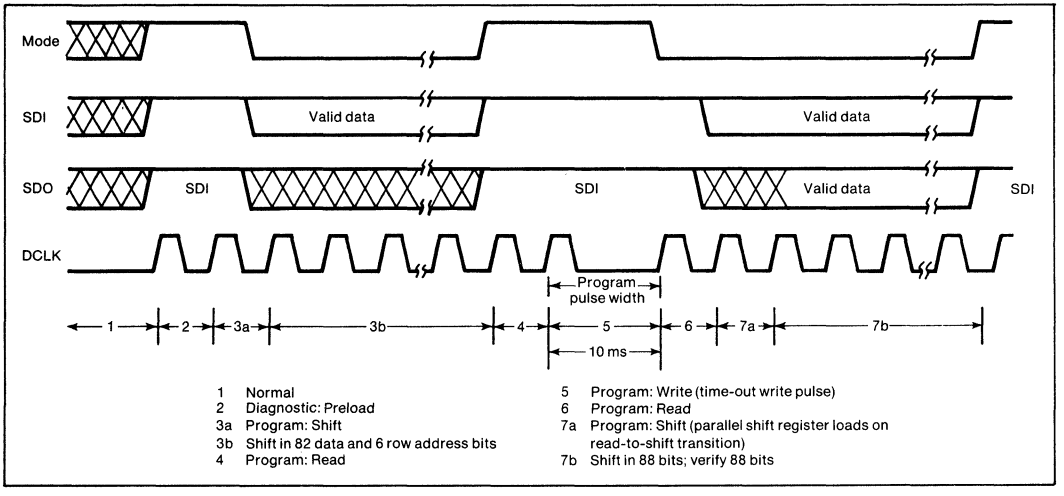
In the program write state, one row of the array is programmed with data from the serial shift register. Programming begins on one leading edge of the DCLK signal and ends on the next; the user must maintain the correct 10-ms programming timing (see the programming sequence, p. 95).

The chip's in-circuit reprogrammability makes possible the design and programming of generic hardware for specific applications. Small-volume system manufacturers can blend several lines of hardware into one, simply by updating the firmware. The fast system upgrades can even be predesigned into a system and enabled later by reprogramming.

ACHIEVING FLEXIBILITY

On-the-spot reprogramming maintains the integrity of a system's hardware, eliminating the need for field service or for returning the chip to the maker for upgrading or replacement. Upgrading can be done in the field by software delivered electronically or by mail, whichever is more convenient. Furthermore, the chip is programmed through the serial scan path, so that system diagnostics are easy to do, either locally or from a remote host system. Repair time and costs can be cut without significant impact on the system's cost or complexity. Since the chip's serial scan path is compatible with the ports in other commercial ICs, a complete system, including logic, can use these powerful and flexible diagnostic techniques.

Two design examples—a programmable two-output, 16-bit input selection decoder and a programmable output port—show off the 16Z8 chip's best points. Normally



2. During chip programming, just four lines transfer all data and perform diagnostics, ensuring that bit patterns are properly loaded.

a decoder's circuitry includes such standard logic as address comparators, DIP switches, and pull-up resistors. The pull-up resistors guarantee noise immunity at the comparator when a switch is off.

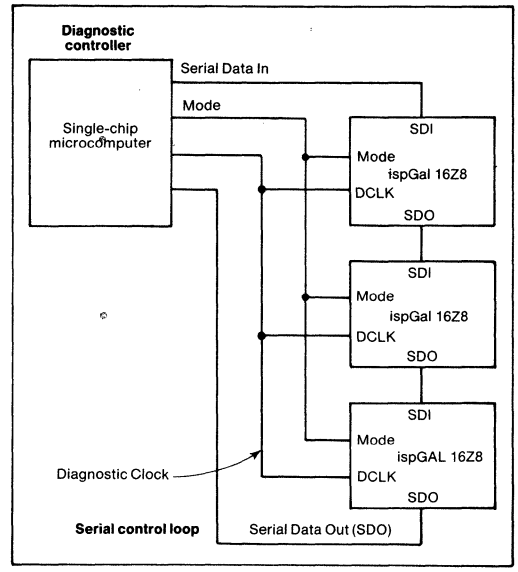
The decoder compares a 16-bit address from a microprocessor with a preset address held in the set of DIP switches. Decoding the two outputs requires four comparators, four octal DIP switches, and four octal resistor packs. In addition, the circuit needs 104 solder connections and 32 switch contacts, all subject to mechanical wear and tear.

A single 16Z8 can implement the same decoder. Switches controlling the address selection functions are internal and, in fact, are the product terms in the AND array. All programming occurs through the four-pin serial interface, and address selection updates are handled through reliable interactive software, rather than through a production-line assembler that uses a factory-standard DIP-switch programming pencil. Moreover, there are only 24 solder connections and no switch contacts, which substantially improves reliability and calls for a much smaller board area.

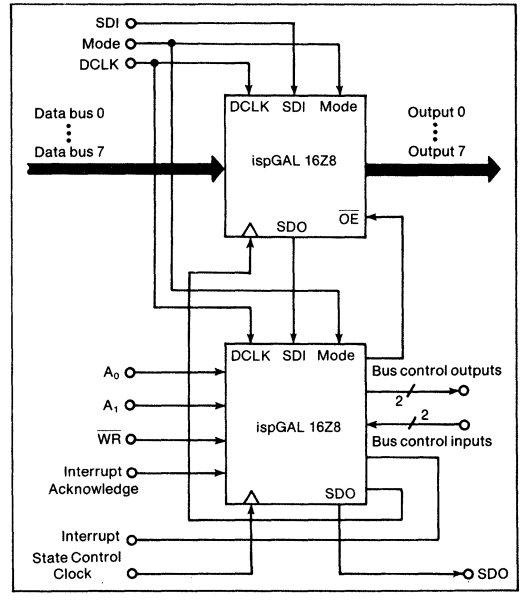
WORKING TOGETHER

The second application, a reconfigurable output port, gives systems wide flexibility and can be put together easily. In this setup, two chips work together, one for the output data path and the other for the microprocessor bus and output-port control paths (Fig. 4). The data path can be configured for registered, combinatorial, or latched outputs, and each output bit can be either active high or active low. Other Boolean logic manipulations are possible with the logic in the chip's AND array.

The control-path device handles the other chip's Clock and Output Enable signals, and its inherent logic can implement virtually any microprocessor or output port interface protocol. Interfaces may be synchronous or asynchronous, and each signal set up individually as a registered or combinatorial output, active high or active low. The interface can be programmed through the serial scan programming interface ICs. Thus a single interface is all that is necessary to tie into many different kinds of peripherals. □



3. Through the four-line serial port, several logic chips can tie into one diagnostic controller for board-level troubleshooting. Preloading the output registers affords rapid testing of programmable devices, since the logic-based circuit can be made to start at any desired state.



4. A programmable output port can be readily formed using two ispGAL16Z8s. The top one sets up the data path, the bottom one handles interface control and external handshaking. The output situation is very flexible; data can be configured in several ways.

Multiple factors define true cost of PLDs

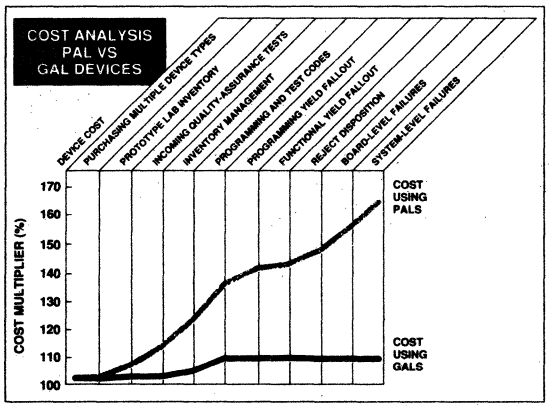
By DEAN SUHR

Designers using PLDs (programmable logic devices) for system design and manufacturing traditionally think of piece price as the key consideration in the PLD selection process. Thanks to recent advances in technology, however, the system cost of using PLDs is influenced by factors such as fabrication technology, device quality, reliability and yield.

System cost is quite different from the sum of the component costs. The price paid for a device or component represents only one part of the system cost of a PLD; the systems team also has to consider the costs hidden in the programming, handling, quality control, throughput and overhead that's necessary to get a "raw" PLD to a functional state on a board.

Because the true system cost of a PLD is the sum of the piece price and all of these hidden costs, and is spread over several functions and departments, it's often difficult to define and measure. In most companies, for example, purchasing and engineering define the parts list and acquire the parts. These departments are often under pressure to reduce absolute unit cost and to purchase the least-expensive part available.

But the profitability of both the product line and the company is based not on device acquisition cost but on total system cost. Buying the least-expensive part may not provide the lowest total system cost.



Programmability can play a significant role in the total cost of PLDs. The example above was taken from a system that used 100,000 bipolar PLDs per year. Moving to E²CMOS GALs can reduce total cost by up to 34 percent.

Hidden cost factors

To calculate the system cost of using a particular PLD type, vendor and technology, managers must also take into consideration the additional costs of purchasing overhead, inventory management, prototype inventory and quality assurance (QA). Purchasing overhead can add 2 percent to the actual device cost. As the number of inventory line items rises, the overhead needed to purchase those items increases. PLDs with generic architectures can minimize the number of different devices a company must purchase, and therefore reduce purchasing costs.

As much as 10 percent of a device's cost can be attributed to inventory management overhead, including shelf space, depreciation, count management, obsolete write-offs, and safety stock. Reducing inventory line items simplifies the management overhead, in turn cutting costs.

BY ELIMINATING YIELD AND HANDLING LOSS, IMPROVING QUALITY, AND SIMPLIFYING INVENTORY MANAGEMENT, DESIGNERS CAN CUT THE TRUE COST OF USING PLDS

PLDs are particularly adaptable to just-in-time (JIT) inventory management systems, which minimize inventory by increasing throughput. Using a JIT system constrains a company's flexibility because the company must carry fewer items. But adding PLDs to the inventory will let the same narrow range of products provide a wide variety of functions.

Macrocell-based PLDs also have increased the flexibility of companies that use them and reduced stocking requirements. In the past, designers using fixed-architecture PLDs had to keep in stock every PLD architecture required for a design. Macrocell-based devices, on the other hand, can be configured to emulate dozens of old architectures and many new configurations.

The macrocell used in E²CMOS generic array logic (GAL) devices goes one step further. These devices also offer 100 percent socket compatibility with older programmable array logic (PAL) architectures, so designers can simply substitute the GAL device for the old PLD architecture. No redesign is necessary. Existing JEDEC files and master devices can be used, reducing system cost.

No longer a simple calculation, the system cost of using programmable logic devices is affected by their fabrication technology, testability and impact on inventory management.

The cost of the prototype inventory also influences total system cost. Although engineering labs are stocked with devices for building and debugging prototypes, many companies meet engineering lab shortages by borrowing from manufacturing stock. This policy can shrink manufacturing inventories and, by doing so, can increase the system cost of the remaining manufacturing units by as much as 1 percent when units are ordered to restock the shelves.

All PLDs have a programmable element that determines their functionality and ac/dc performance. These programmable elements can be fabricated from metal-link fuses, programmable diodes or transistors, volatile static RAM cells, UV EPROM cells or EEPROM cells. Each of these technologies varies in programmability and has a different impact on device performance and reliability.

Each programmable element also offers a different erase capability. Metal-link and one-time-programmable devices, for instance, can't be erased. UV EPROM devices can be erased, but this process requires an expensive windowed package and takes 20 to 30 minutes. EEPROM devices offer instant erasability in as little as 50 ms. Technologies that aren't erasable or that have lengthy erase times constrain test flexibility and may add to the total system cost.

Finally, PLDs are usually subjected to a complete, electrical QA test upon receipt, which typically adds 7 percent to the device cost. This additional cost is based on test engineering and manufacturing resources, yield and equipment utilization. Manufacturers can avoid this additional expense without degrading device quality, by using E²CMOS devices. These devices are 100 percent pretested by the manufacturer, and require no incoming test. And their instant erasability lets IC manufacturers perform extensive tests at the manufacturing stage, prior to shipment to end-users.

Some companies, however, have extensive incoming QA operations that can't be eliminated. Reusable E²CMOS devices are ideal for these operations because they can be returned to manufacturing inventory after QA testing, instantly reprogrammed, and reused in production boards. This flexibility also lets QA engineers perform their inspection at any step in the process.

QA engineers can also simplify their testing by using generic-architecture, macrocell-based devices. These devices can be tested with one common test program and then configure in many ways during the programming operation. This step eliminates the generation and maintenance of multiple test programs and fixtures, one for each fixed architecture.

Analyzing the system cost

Managers can reduce these overhead costs to a formula based on a simple approach that assumes a percentage cost adder and yield factor for each operation: $Cost_n = Cost_{n-1} + (Cost_{n-1}/Yield_n)$. This formula is generic, so managers can tailor the factors to their specific environment and then analyze the actual system cost of using a particular PLD.

E²CMOS PLDs offer performance, quality, reliability and, most important, cost advantages over alternative solutions. By eliminating yield and handling loss, improving quality, and simplifying inventory management, designers can significantly reduce the true cost of using PLDs.

Dean Suhr is product marketing manager at Lattice Semiconductor, Hillsboro, OR.

The Factor of Ten rule

It's crucial that managers keep in mind the cost of detecting and repairing defective PLDs during manufacturing — and the importance of early detection. A common guideline for determining this cost is the Factor of Ten rule.

This rule states that the cost of detecting and repairing a defective PLD grows by a factor of ten at each subsequent stage in the manufacturing process. This dramatic growth rate is possible because other symptoms mask the PLD's faulty functionality as the device is buried deeper in the system.

The Factor of Ten rule implies that the earlier defective devices are caught, the lower the repair cost. If defects aren't found early, a very small yield loss can be greatly magnified by the quantity of devices on a board or in a system. Even a yield loss as small as 0.5 percent can result in a 5 percent system failure rate with only five PLDs per system. A loss of 0.5 percent translates to a defect rate of 5,000 ppm, a high defect rate.

Section 1: Introduction to Generic Array Logic

Section 2: GAL Datasheets

Section 3: GAL Military Products

Section 4: Quality and Reliability

Section 5: Technical Notes

Section 6: Article Reprints

Section 7: General Information

Development Tools

Lattice Semiconductor recommends that customers use only Lattice qualified programming equipment. Lattice guarantees 100% programming yield to customers using qualified programming tools. Below is a matrix that provides the third-party programmers which are qualified to program Lattice GAL devices.

Lattice works closely with third-party programming equipment manufacturers to ensure that customers achieve the highest programming yields and quality levels. Lattice's stringent qualification program includes an evaluation of algorithms, verification of timing and voltage levels, and a complete yield analysis.

For a current listing of Lattice qualified GAL programmers, please call Lattice's Literature Distribution Department (Tel: 503-693-0287; FAX: 503-681-3037) and request a GAL Qualified Programming Hardware List. This document contains information regarding programmer revision levels, adapters, and features.

LATTICE QUALIFED PROGRAMMERS (as of May 1991)

Vendor	Programmer	Lattice GAL Device Type									
		16V8A	16V8B	20V8A	20V8B	18V10	22V10	22V10B	26CV12	20RA10	6001
Data I/O	Unisite	■	■	■	■	■	■	■	■	■	■
	2900	■	■	■	■	■	■	■	■	■	■
	29B	■	■	■	■	■	■	■	■	■	■
	60A/H	■	■	■	■	■	■	■	❑	■	■
Logical Devices	Allpro 40	■	■	■	■	■	■	■	■	■	■
	PALPRO 2X	■	■	■	■	❑	■	❑	○	❑	❑
Stag	System 3000	■	■	■	■	■	■	■	■	■	■
	ZL30/A	■	■	■	■	■	■	■	■	■	■
System General	TURPRO-1	■	■	■	■	■	■	■	■	■	■
	SGUP-85A	■	■	■	■	■	■	■	■	■	■
	SGUP-85	■	■	■	■	■	■	■	■	■	■
SMS Microcomputer	Sprint Expert	■	■	■	■	■	■	■	■	■	■
	Sprint Plus	■	■	■	■	■	■	■	■	■	■
Digelec	Model 860	■	■	■	■	■	■	■	○	■	■
BP-Microsystems	PLD-1100	■	■	■	■	■	■	■	○	■	■
Prog. Logic Tech.	Logic Lab	■	■	■	■	■	■	■	■	■	■
Advin	Pilot-GL	■	■	■	■	■	■	■	■	■	■

■ = Programmer is qualified, refer to the GAL Qualified Programming Hardware list for additional information.
❑ = Programmer was not qualified as of 5/91. Contact Lattice or programmer vendor for latest information.
○ = Programmer does not support 28-pin devices.

LOGIC COMPILER SUPPORT (as of May 1991)

Vendor	Programmer	Lattice GAL Device Type						
		16V8A/B	20V8A/B	18V10	22V10/B	26CV12	20RA10	6001
Accel Tech.	Tango PLD	■	■	■	■	■	■	■
Data I/O	ABEL	■	■	■	■	■	■	■
ISDATA	LOG/iC	■	■	■	■	■	■	■
Logical Devices	CUPL	■	■	■	■	■	■	■
Minc	PLDesigner	■	■	■	■	■	■	■
OrCAD	OrCAD PLD	■	■	■	■	■	■	O
Omation	Schema-PLD	■	■	■	■	■	■	■

■ = Compiler supports GAL device type. Contact vendor or Lattice for the current revision level.
O = Contact vendor for support date.

PROGRAMMER/COMPILER VENDORS

Accel Technologies
6825 Flanders Dr.
San Diego, CA 92121
Phone: (619) 554-1000
FAX: (619) 554-1019

Advin Systems
1050-L Duane Ave
Sunnyvale, CA 94086
Phone: (408) 243-7000
Fax: (408) 736-2503

BP Microsystems
10681 Haddington
Suite #190
Houston, TX 77043
Tel: (713) 461-9430
Fax: (713) 461-7431
BBS: (713) 461-4958

Data I/O Corp.
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
Phone: (206) 881-6444
FAX: (206) 882-1043
In Europe contact:
Data I/O Corp.
Phone: +31 (0) 20-6622866
In Japan contact:
Data I/O Corp.
Phone: (03) 432-6991

Digitronics Israel Ltd.
25 Galgaley Haplada St.
Herzliya B 46722
Israel
Tel: 052-559615
fax: 052-555240
In the U.S. contact
Digelec
20144 Plummer St.
Chatsworth, CA 91311
Tel: (818) 701-9677
Fax: (818) 701-5040

ISDATA GmbH
Haid-und-Neu-Straße 7
7500 Karlsruhe 1
West Germany
Phone: 0721-693092
FAX: 0721-174263
In the U.S. contact
ISDATA Inc.
Phone: (408) 373-7359
FAX: (408) 373-3622

Logical Devices
1321 N.W. 65th Place.
Fort Lauderdale, FL 33309
Phone: (305) 974-0967
FAX: (305) 974-8531

Minc Incorporated
1575 York Rd.
Colorado Springs, CO 80918
Phone: (719) 590-1155
FAX: (719) 594-4708

Omation
801 Presidential
Richardson, TX 75081
Phone: (214) 231-5167
FAX: (214) 783-9072

OrCAD Systems Corp.
3175 N.W. Aloclek Dr.
Hillsboro, OR 97124
Phone: (503) 690-9881
FAX: (503) 690-9891

Programmable Logic Tech
P.O. Box 1567
Longmont, CO 80501
Tel: (303) 772-9059
Fax: (303) 772-5617

SMS Micro Systems
1M Morgenthal
D-8994 Hergatz
Scwarzenberg
W. Germany
In the U.S. contact:
Encore Technology Corp.
13720 Midway Suite 105
Dallas, TX 75244
Tel: (214) 233-2614
Fax: (214) 233-3122

Stag Microsystems
Martinfield
Welwyn Garden City
Hertz. AL7 15T
United Kingdom
Phone: 011-44-707-332148
FAX: 011-44-707-371503
In the U.S. contact:
Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
Phone: (408) 988-1118
FAX: (408) 988-1232

System General
3Fl., No. 6, Lane 4
Tun Hwa N. Rd.
P.O. Box: 53-591
Taipei, Taiwan R.O.C.
Phone: 886-2-7212613
FAX: 886-2-7212615
In the U.S. contact:
System General
244 S. Hillview Dr.
Milpitas, CA 95035
Phone: (408) 263-6667
FAX: (408) 262-9220

Copying PAL, EPLD & PEEL Patterns Into GAL Devices

INTRODUCTION

The generic/universal architectures of Lattice GAL devices are able to emulate a wide variety of PAL, EPLD and PEEL devices. GAL devices are direct functional and parametric replacements for most PLD device architectures. To use GAL devices in place of other PLD types, some conversion of the original device pattern may be needed. This conversion is not difficult, and can be accomplished at either the design or manufacturing level. The following sections describe several techniques available to convert PAL, EPLD and PEEL device patterns to Lattice GAL device patterns. The following table lists PLD devices that can be replaced by Lattice GAL devices.

CROSS PROGRAMMING: GAL16V8 AND GAL20V8

The GAL16V8 and GAL20V8 devices replace most standard 20-pin and 24-pin PAL devices. To simplify the conversion process, Lattice has worked with programmer hardware manufacturers to provide the ability to program GAL devices directly from existing PAL JEDEC files, or master PAL devices. Lattice qualified programmers can automatically configure the architecture of a GAL device to emulate the source PAL device.

To provide a conceptual framework for the conversion from PAL devices to GAL devices, a mythical device known as a RAL device was created. A RAL device is simply a GAL device configured to emulate a PAL. There is a one-to-one correspondence between the name of a PAL device and that of a RAL device. For example, a RAL16L8 is simply a GAL16L8 configured as a PAL16L8. Some programmers list the RAL device types as choices for cross-programming, while others specifically state that a cross-programming operation is to be performed using a PAL device type as the architecture type.

To program a GAL16V8 or GAL20V8 device from an existing PAL JEDEC file, simply select the appropriate device code (either RAL type, or PAL type to cross-program from), then download the PAL JEDEC file to the programmer. Insert the appropriate GAL device that can directly emulate the PAL device (according to the chart on the following page). The programmer will automatically configure the GAL device to emulate the PAL device during programming. The resulting GAL device is 100% compatible with the original PAL device.

A GAL device may also be programmed from a master PAL device by reading the pattern of the master PAL into the programmer memory, then selecting the appropriate RAL device or PAL type to cross-program from. The GAL device can then be programmed from the programmer memory.

CROSS PROGRAMMING: GAL22V10/GAL20RA10

The GAL22V10 and GAL20RA10 are direct replacements for bipolar PAL devices, and are JEDEC fuse map compatible with these industry standard devices. To program a GAL22V10 or GAL20RA10 device from an existing PAL JEDEC file, simply select the appropriate GAL device code, then download the PAL JEDEC file to the programmer. The resulting GAL device is 100% compatible with the original PAL.

GAL devices also may be programmed from Master PAL devices by reading the pattern of the Master PAL into the programmer memory, then selecting the appropriate GAL device code. The GAL device can then be programmed from the programmer memory.

The GAL22V10 and GAL20RA10 also can store a User Electronic Signature (see the datasheets on these devices for more information). To use this feature, the JEDEC file must contain this information. To add the signature data to the JEDEC map, use the PALtoGAL conversion utility (see next section) or recompile the source equations for a Lattice GAL device instead of a generic 22V10 type. Many programmers list two device types to differentiate between the two types of JEDEC files, and list both a GAL22V10 and a name such as GAL22V10UES or GAL22V10ES. Other programmers allow both types of JEDEC files to be accepted, and simply don't program the Signature fuses if they are not present in the file.

PALTOGAL CONVERSION UTILITY SOFTWARE

Lattice has created a software utility that will convert an existing PAL device JEDEC file to the appropriate GAL device JEDEC format. Called PALtoGAL, this software utility can be used to convert PAL device files to GAL device files, add or change the User Electronic Signature without changing device functionality, and reformat existing GAL JEDEC files for readability.

Since a few programmable logic devices have features that a GAL device cannot exactly emulate, the PALtoGAL utility will clearly describe the incompatibility but will not create an output file. GAL devices programmed using files converted by PALtoGAL will be 100% compatible with the original logic device. PALtoGAL is just another method of cross-programming, and should produce the same results as using a programmer. The advantage is that a full GAL device JEDEC map is created, meaning

that the appropriate GAL device may then be selected on the programmer, which may simplify the manufacturing flow.

A copy of the PALtoGAL conversion utility software can be obtained through your local Lattice representative, or by contacting the GAL Applications Hotline at 1-800-FASTGAL (327-8425) or (503) 693-0201. The software also may be downloaded from Lattice's Electronic Bulletin Board at (503) 693-0215; the file name is "PALTOGAL.EXE".

SOFTWARE COMPILER CONVERSION

If the equation source file is available for the PAL device, it can be converted by re-compiling using a suitable logic compiler that supports GAL devices. If there are any device incompatibilities (there shouldn't be in most cases), the compiler will describe the errors. The output of the compiler will be a GAL JEDEC file that can be used to program a GAL device directly. The resulting GAL device will be 100% functionally compatible with the original device.

Suitable logic compilers are listed in the Development Tools section. If additional questions arise, contact your compiler manufacturer or a Lattice Applications Engineer by calling the GAL Applications Hotline at 1-800-FASTGAL or (503) 693-0201.

COPYING PAL, EPLD AND PEEL PATTERNS INTO GAL DEVICES

	GAL16V8A/B	GAL20V8A/B	GAL18V10	GAL22V10/B	GAL26CV12	GAL20RA10
PAL10H8	●		⊛			
PAL10L8	●		⊛			
PAL10P8	●		⊛			
PAL12H6	●		⊛			
PAL12L6	●		⊛			
PAL12P6	●		⊛			
PAL14H4	●		⊛			
PAL14H8		●		⊛		
PAL14L4	●		⊛			
PAL14L8		●		⊛		
PAL14P4	●		⊛			
PAL14P8		●		⊛		
PAL16H2	●		⊛			
PAL16H6		●		⊛		
PAL16H8	●		⊛			
PAL16L2	●		⊛			
PAL16L6		●		⊛		
PAL16L8	●		⊛			
PAL16P2	●		⊛			
PAL16P6		●		⊛		
PAL16P8	●		⊛			
PAL16R4	●		⊛			
PAL16R6	●		⊛			
PAL16R8	●		⊛			
PAL16RP4	●		⊛			
PAL16RP6	●		⊛			
PAL16RP8	●		⊛			
PAL18H4		●		⊛		
PAL18L4		●		⊛		
PAL18P4		●		⊛		

	GAL16V8A/B	GAL20V8A/B	GAL18V10	GAL22V10/B	GAL26CV12	GAL20RA10
PAL18P8	○		⊛			
PAL18U8	○		⊛			
PAL20H2		●		⊛		
PAL20H8		●		⊛		
PAL20L2		●		⊛		
PAL20L8		●		⊛		
PAL20P8		●		⊛		
PAL20R4		●		⊛		
PAL20R6		●		⊛		
PAL20R8		●		⊛		
PAL20RP4		●		⊛		
PAL20RP6		●		⊛		
PAL20RP8		●		⊛		
PAL20RA10						●
PAL22V10				●		
PALCE16V8	●		⊛			
PALCE20V8		●		⊛		
PALCE22V10				●		
PALCE26V12					○	
PEEL18CV8	○		○			
EP320	○		⊛			
85C220	○		⊛			
85C224		○		⊛		
GAL16V8A/B			⊛			
GAL20V8A/B				⊛		

● Direct Replacement, with Cross Programming Availiable.
⊛ Direct Replacement, no Cross Programming Availiable.
○ Direct Replacement, with some Function Restrictions.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LATTICE PART #
ALTERA	EP310 EP320 EP330	GAL16V8A/B[1] or... GAL18V10
AMD	PAL10H8 PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	GAL16V8A/B
	PAL16L8 PAL16R4 PAL16R6 PAL16R8 PALC16L8 PALC16R4 PALC16R6 PALC16R8 AmPAL16L8 AmPAL16R4 AmPAL16R6 AmPAL16R8 PAL16P8 PAL16RP4 PAL16RP6 PAL16RP8	GAL16V8A/B
	PALCE16V8	GAL16V8A/B
	AmPAL18P8 PALC18U8	GAL16V8A/B[1] or... GAL18V10
	PAL14L8 PAL16L6 PAL18L4 PAL20L2	GAL20V8A/B
	PAL20L8 PAL20R4 PAL20R6 PAL20R8 AmPAL20RP4 AmPAL20RP6 AmPAL20RP8	GAL20V8A/B
	PALCE20V8	GAL20V8A/B
	PAL20RA10	GAL20RA10

MANUFACTURER	PART #	LATTICE PART #
AMD	AmPAL20RP10	GAL22V10/B
	PAL20S10 PAL20RS4 PAL20RS8 PAL20RS10	GAL22V10/B
	AmPAL20L10 PAL20L10 PAL20X4 PAL20X8 PAL20X10	GAL22V10/B[1]
	AmPAL22V10 PAL22V10 PALC22V10 PALCE22V10	GAL22V10/B
	PALCE24V10 PALCE26V12	GAL26CV12[1]
ATMEL	AT22V10	GAL22V10/B
CYPRESS	PALC16L8 PALC16R4 PALC16R6 PALC16R8	GAL16V8A/B
	PLDC18G8	GAL16V8A/B[1] or... GAL18V10
	PALC20CG10 PALC22V10 PAL22V10	GAL20V8A/B[1] or... GAL22V10/B
	PLD20RA10	GAL20RA10
HARRIS	HPL16LC8 HPL16RC4 HPL16RC6 HPL16RC8	GAL16V8A/B
ICT	PEEL18CV8	GAL16V8A/B[1] or... GAL18V10
	PEEL153 PEEL253	GAL16V8A/B[1] or... GAL18V10[1]
	PEEL20CG10 PEEL22CV10A	GAL20V8A/B[1] or... GAL22V10/B

1) Possible conversion but not 100% compatible to this device.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LATTICE PART #
INTEL	5C031 5C032 85C220	GAL16V8A/B[1] or... GAL18V10
	85C224	GAL20V8A/B[1] or... GAL22V10/B
NATIONAL	PAL10H8	GAL16V8A/B
	PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	GAL16V8A/B
	PAL16L8 PAL16R4 PAL16R6 PAL16R8	GAL16V8A/B
	GAL16V8 GAL16V8A	GAL16V8A/B
	GAL18V10	GAL18V10
	PAL14L8 PAL16L6 PAL18L4 PAL20L2	GAL20V8A/B
	PAL20L8 PAL20P8 PAL20R4 PAL20RP4 PAL20R6 PAL20RP6 PAL20R8 PAL20RP8	GAL20V8A/B
	PAL20RA10	GAL20RA10
	PAL20L10 PAL20X4 PAL20X8 PAL20X10	GAL22V10/B[1]
	GAL22V10	GAL22V10/B
	GAL26CV12	GAL26CV12
	GAL6001	GAL6001

MANUFACTURER	PART #	LATTICE PART #
RICOH	EPL10P8 EPL12P6 EPL14P4 EPL16P2	GAL16V8A/B
	EPL16P8 EPL16RP4 EPL16RP6 EPL16RP8	GAL16V8A/B
SAMSUNG	CPL16L8 CPL16R4 CPL16R6 CPL16R8	GAL16V8A/B
	CPL20L8 CPL20R4 CPL20R6 CPL20R8	GAL20V8A/B
	CPL22V10	GAL22V10/B
SGS-THOMSON	GAL16V8	GAL16V8A/B
	GAL20V8	GAL20V8A/B
	GAL39V18	GAL6001
	GAL16Z8	ispGAL16Z8
SIGNETICS	PLHS16L8 PLUS16L8 PLUS16R4 PLUS16R6 PLUS16R8	GAL16V8A/B
	PLHS18P8	GAL16V8A/B[1] or... GAL18V10
	PLS153 PHD16N8	GAL16V8A/B[1] or... GALI8V10[1]
	PLUS20L8 PLUS20R4 PLUS20R6 PLUS20R8	GAL20V8A/B
SPRAGUE	SPL14LC8 SPL16LC8 SPL16RC4 SPL16RC6 SPL16RC8	GAL16V8A/B

1) Possible conversion but not 100% compatible to this device.

MANUFACTURER	PART #	LATTICE PART #
SPRAGUE	SPL18LC4 SPL20LC2	GAL20V8A/B
	SPL20LC8 SPL20RC4 SPL20RC6 SPL20RC8	GAL20V8A/B
TI	TIBPAL16L8 TIBPAL16R4 TIBPAL16R6 TIBPAL16R8	GAL16V8A/B
	TICPAL16L8 TICPAL16R4 TICPAL16R6 TICPAL16R8	GAL16V8A/B GAL16V8A/B
	EP330 TIBPAD16N8	GAL16V8A/B[1] or... GAL18V10[1]
	TIBPAL20L8 TIBPAL20R4 TIBPAL20R6 TIBPAL20R8	GAL20V8A/B
	TIBPAL22V10 TICPAL22V10	GAL22V10/B

1) Possible conversion but not 100% compatible to this device.

Package Thermal Resistance

The following table provides information on the package thermal resistance of Lattice commercial and industrial grade devices. For information on the package thermal resistance of Lattice military grade devices, please refer to "MIL-M-38510, Appendix C".

Testing was performed per SEMI TEST METHOD G38-87: "Still and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of IC Packages" with devices mounted on a thermal test board conforming to SEMI SPECIFICATION G42-88: "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages".

Test Conditions
Power Dissipation = 0.5watts (IC chip reverse biased)
Ambient Air Velocity = Zero (still air)
Ambient Temperature = 65°C
Measuring Current = 3mA

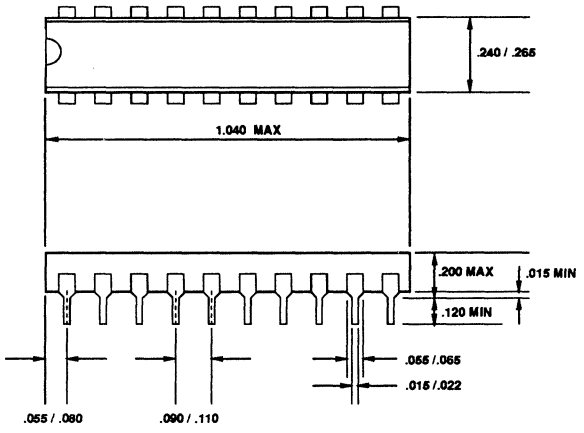
PACKAGE THERMAL RESISTANCE

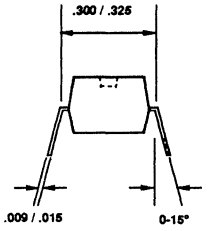
Commercial/Industrial Grade Devices

Package Type:	Device Type:	θ_{JA}	θ_{JC}
20-Pin Plastic DIP	GAL16V8A/B GAL18V10	59°C/W	39°C/W
24-Pin Plastic DIP	GAL20V8A/B GAL22V10/B GAL20RA10 GAL6001 ispGAL16Z8	57°C/W	36°C/W
28-Pin Plastic DIP	GAL26CV12	55°C/W	33°C/W
20-Pin Plastic LCC	GAL16V8A/B GAL18V10	46°C/W	32°C/W
28-Pin Plastic LCC	GAL20V8A/B GAL22V10/B GAL20RA10 GAL26CV12 GAL6001	45°C/W	29°C/W

20-Pin Plastic DIP

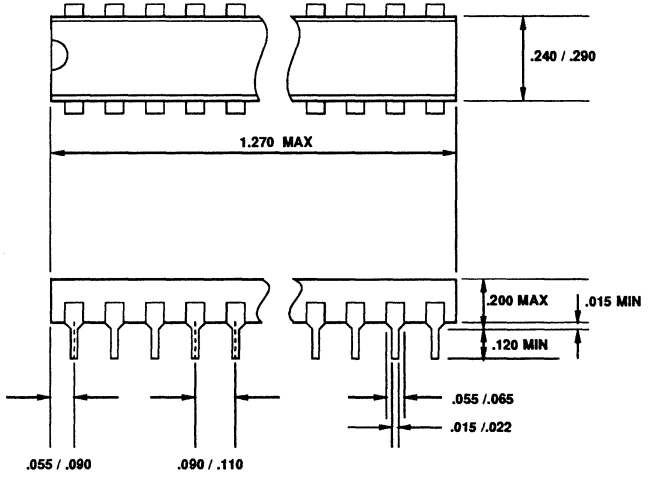
Dimensions in Inches MIN. / MAX.

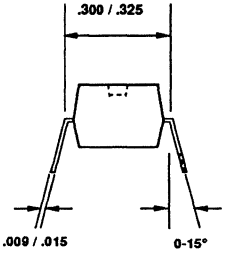




24-Pin Plastic DIP

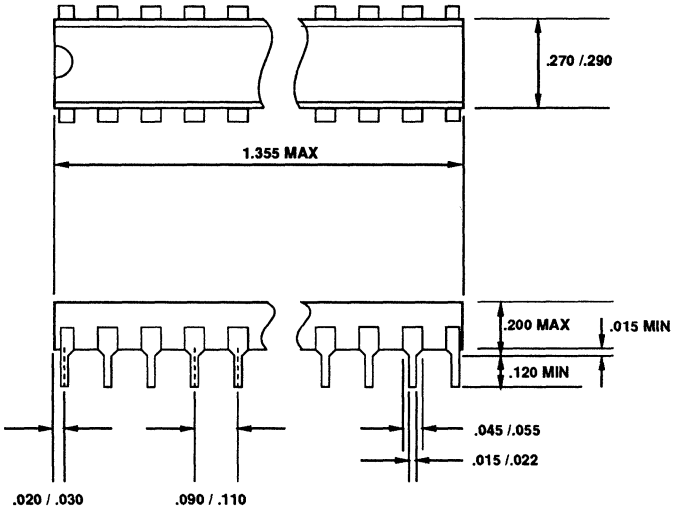
Dimensions in Inches MIN. / MAX.

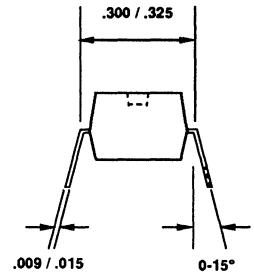




28-Pin Plastic DIP

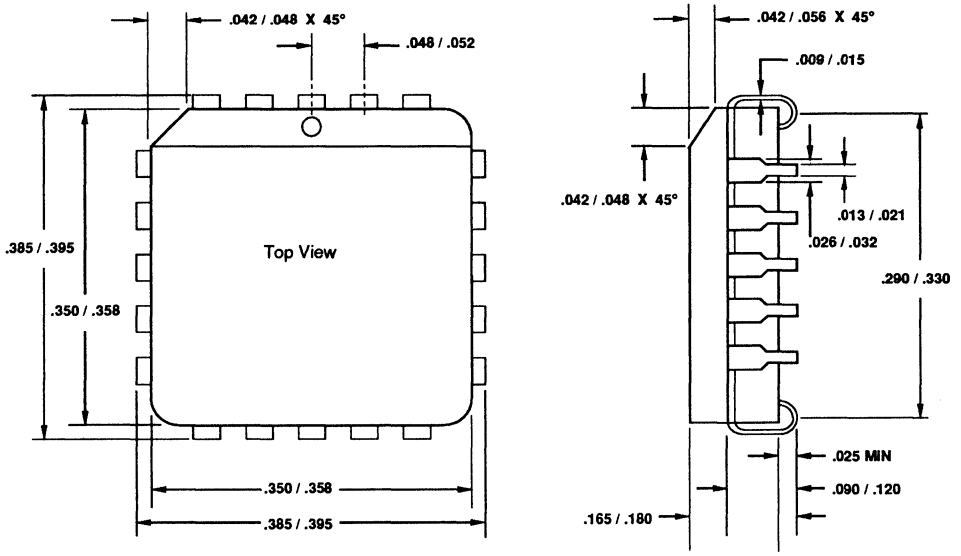
Dimensions in Inches MIN. / MAX.





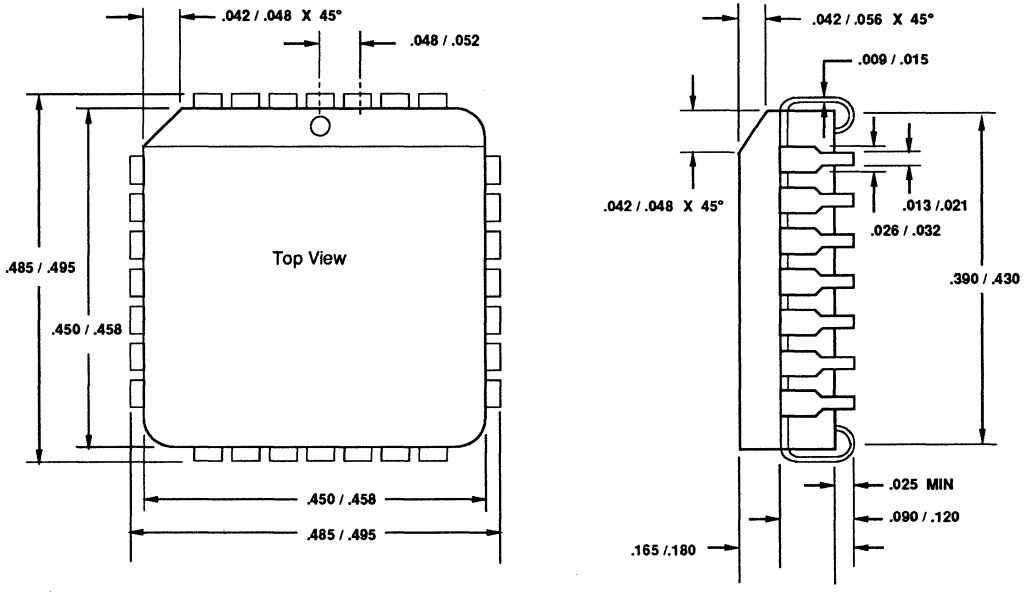
20-Pin PLCC Package

Dimensions in Inches MIN. / MAX.



28-Pin PLCC Package

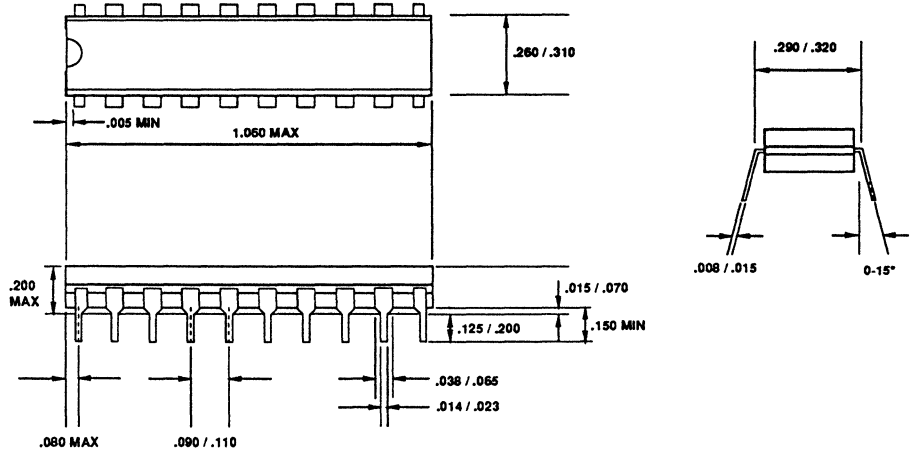
Dimensions in Inches MIN. / MAX.



7

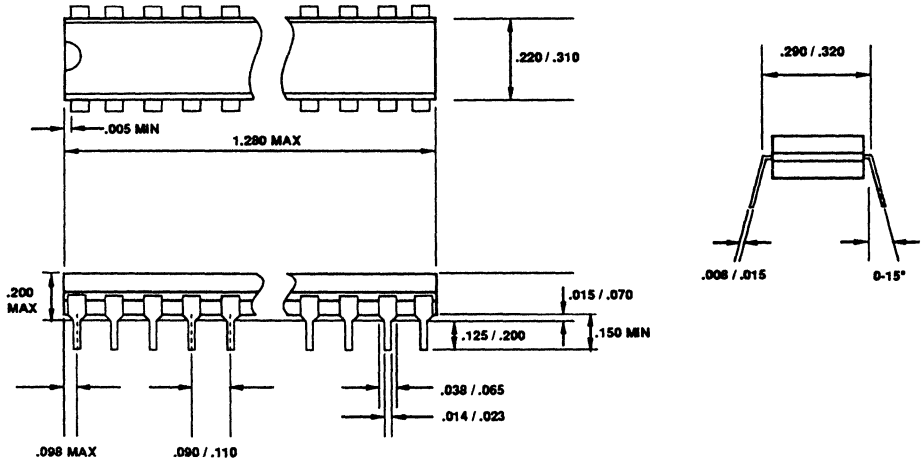
20-Pin (300 MIL) CERDIP

Dimensions in Inches MIN. / MAX.



24-Pin (300 MIL) CERDIP

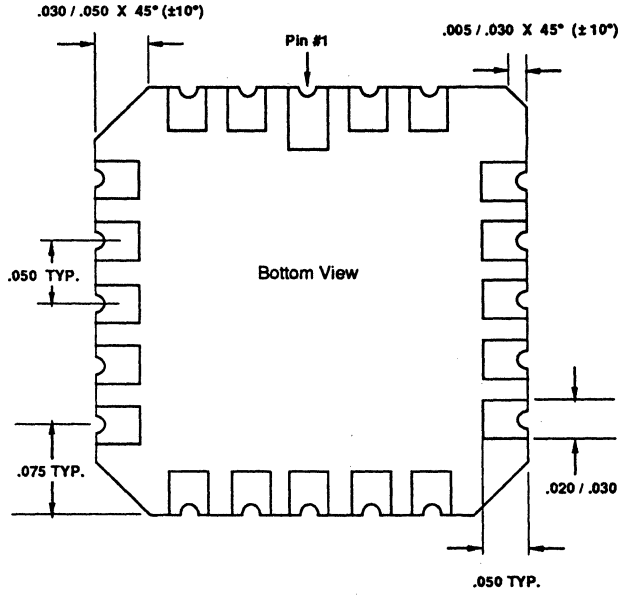
Dimensions in Inches MIN. / MAX.

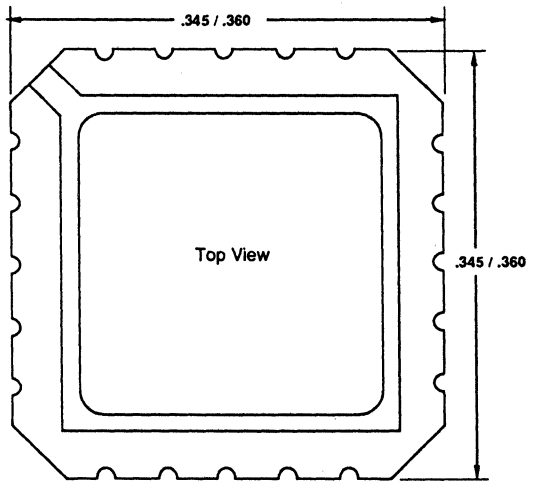


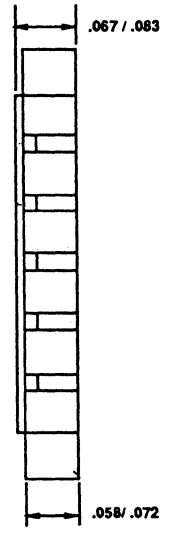
7

20-Pin LCC

Dimensions in Inches MIN. / MAX.

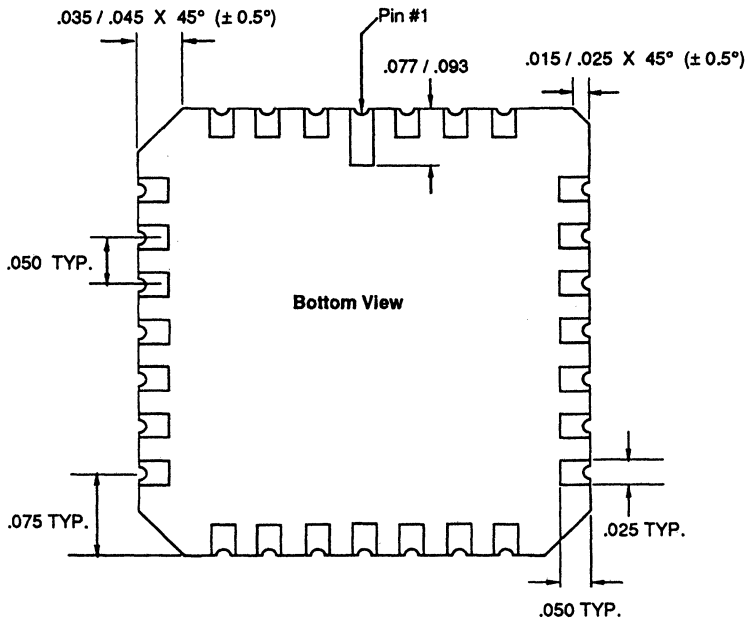


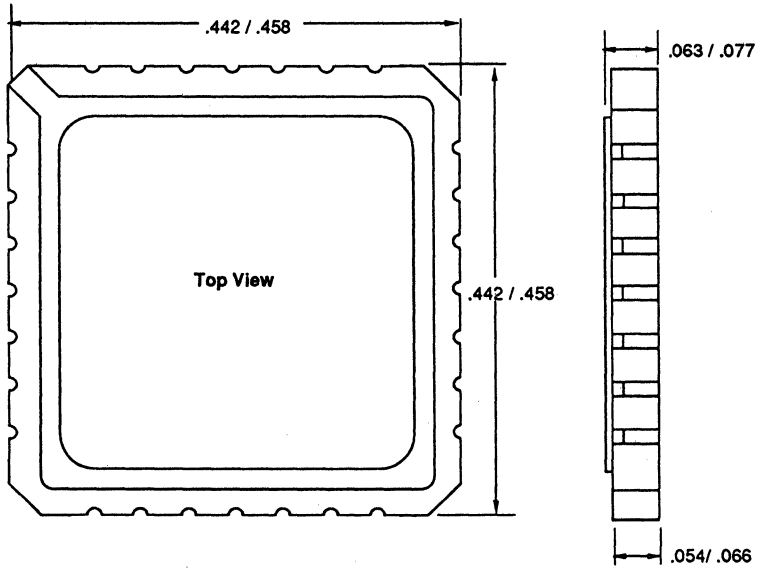




28-Pin LCC

Dimensions in Inches MIN. / MAX.





Tape and Reel Specifications

A tape-and-reel packing container is available for plastic leaded chip carriers to protect the product from mechanical/ electrical damage and to provide an efficient method for handling. Lattice's tape-and-reel containers are shipped in full compliance to Electronics Industry Association Standard EIA-RS481.

The tape-and-reel packing system consists of a pocketed carrier tape loaded with one device per pocket. A protective cover tape seals the carrier tape and holds the devices in the pockets. A full reel holds a maximum quantity of devices depending on the package size. Lattice requires ordering in full reel quantities. Once loaded, the tape is wound onto a plastic reel for labeling and packing.

Devices packaged in tape-and-reel containers must be factory programmed (pre-patterned). Custom marking of devices prior to mounting on tape-and-reel is available upon request. Contact your local Lattice sales office for more details on Lattice's tape-and reel packing system.

TAPE-AND-REEL QUANTITIES AND DIMENSIONS

Package	Pin Count	Carrier Tape Dimensions		Quantity Per 13 Inch Reel
		Width	Pitch	
PLCC	20-pin	16mm	12mm	1000
	28-pin	24mm	16mm	750

DIRECT SALES OFFICES

FRANCE
Lattice Semiconductor
Les Bureaux de Sèvres
72-78, Grand Rue
92310 Sèvres
France
TEL: 1-45 34 10 10
FAX: 1-46 26 71 36

GERMANY
Lattice Semiconductor
Stahlgruberring 12
8000 Munich 82
West Germany
TEL: (089) 42 01 107
FAX: (089) 422 731

JAPAN
Lattice Semiconductor
Peony Kikuchi 201
1-8-4, Botan
Koto-ku, Tokyo
Japan 135
TEL: 03-642-0621
FAX: 03-642-0629

NORTH AMERICA

CALIFORNIA
Lattice Semiconductor
1731 Technology Dr.
Suite 590
San Jose, CA 95110
TEL: (408) 441-0196
FAX: (408) 441-0739

Lattice Semiconductor
Carlsbad Pacific Ctr. One
701 Palomar Airport Rd.
3rd Floor
Carlsbad, CA 92009
TEL: (619) 931-4751
FAX: (619) 431-1821

GEORGIA
Lattice Semiconductor
3105 Medlock Bridge Rd.
Norcross, GA 30071
TEL: (404) 446-2930
FAX: (404) 416-7404

MASSACHUSETTS
Lattice Semiconductor
67 S. Bedford St.
Suite 400 West
Burlington, MA 01803
TEL: (617) 229-5819
FAX: (617) 272-3213

MINNESOTA
Lattice Semiconductor
13664 Hannibal Circle
Apple Valley, MN 55124
TEL: (612) 891-5200
FAX: (612) 891-5205

NEW JERSEY
Lattice Semiconductor
175-3C Fairfield Rd.
West Caldwell, NJ 07006
TEL: (201) 744-5908
FAX: (201) 509-9309

OREGON
Lattice Semiconductor
5555 N.E. Moore Ct.
Hillsboro, OR 97124
TEL: (503) 780-6771
FAX: (503) 681-3037

TEXAS
Lattice Semiconductor
100 Decker Ct. Ste. 280
Irving, TX 75062
TEL: (214) 650-1236
FAX: (214) 650-1237

NORTH AMERICAN SALES REPRESENTATIVES

ALABAMA
The Novus Group
2905 Westcorp Blvd. #120
Huntsville, AL 35805
(205) 534-0044

ARIZONA
Summit Sales
7802 E. Gray Rd. #600
Scottsdale, AZ 85260
(602) 998-4850

CALIFORNIA
Bager Electronics
17220 Newhope St. #209
Fountain Valley, CA 92708
(714) 957-3367

Bager Electronics
6324 Variel Ave. #314
Woodland Hills, CA 91367
(818) 712-0011

Criterion Sales
3350 Scott Blvd, Bldg.44
Santa Clara, CA 95054
(408) 988-6300

Earle Associates
7585 Ronson Rd. #200
San Diego, CA 92111
(619) 278-5441

COLORADO
Waugaman Associates
4800 Van Gordon
Wheat Ridge, CO 80033
(303) 423-1020

CONNECTICUT
Comp Rep Associates
117 Church St.
Yalesville, CT 06492
(203) 269-1145

FLORIDA
Sales Engineering Concepts
776 S. Military Trail
Deerfield Beach, FL 33442
(305) 426-4601

Sales Engineering Concepts
600 S. Norhtlake Blvd. #230
Altamonte Spgs, FL 32701
(407) 830-8444

GEORGIA
The Novus Group
6115A Oakbrook Pkwy.
Norcross, GA 30093
(404) 263-0320

ILLINOIS
Omni Electronics
328 E. Main
Barrington, IL 60010
(708) 381-9087

KANSAS
Stan Clothier Company
805 Clairborne
Olathe, Kansas 66062
(913) 829-0073

MARYLAND
Deltatronics
24048 Sugar Cane Ln.
Gaithersburg, MD 20882
(301) 253-0615

MASSACHUSETTS
Comp Rep Associates
100 Everett Street
Westwood, MA 02090
(617) 329-3454

MICHIGAN
Greiner & Associates
15324 E. Jefferson Ave.
Grosse Pointe Park, MI
48230
(313) 499-0188

MINNESOTA
Stan Clothier Company
10000 W. 76th St #D
Eden Prairie, MN 55344
(612) 944-3456

MISSOURI
Stan Clothier Company
3910 Old Highway 94 South
St. Charles, MO 63303
(314) 928-8078

North American Sales Representatives

NEW JERSEY
Technical Marketing Group
175-3C Fairfield Rd.
West Caldwell, NJ 07006
(201) 226-3300

NEW MEXICO
Summit Sales
2651 K Pan American N.E.
Albuquerque, NM 87107
(505) 345-5003

NEW YORK
Technical Marketing Group
20 Broad Hollow Rd.
Melville, NY 11747
(516) 351-8833

Tri-Tech Electronics
300 Main St.
E. Rochester, NY 14445
(716) 385-6500

Tri-Tech Electronics
14 Westview Dr.
Fishkill, NY 12524
(914) 897-5611

Tri-Tech Electronics
6836 E. Genesee St.
Fayetteville, NY 13066
(315) 446-2881

NORTH CAROLINA
The Novus Group
102L Commonwealth Ct.
Cary, NC 27511
(919) 460-7771

OHIO
Makin & Associates
3165 Lynwood Rd.
Cincinnati, OH 45208
(513) 871-2424

Makin & Associates
6400 Riverside Dr. Bldg. A
Dublin, OH 43017
(614) 793-9545

Makin & Associates
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