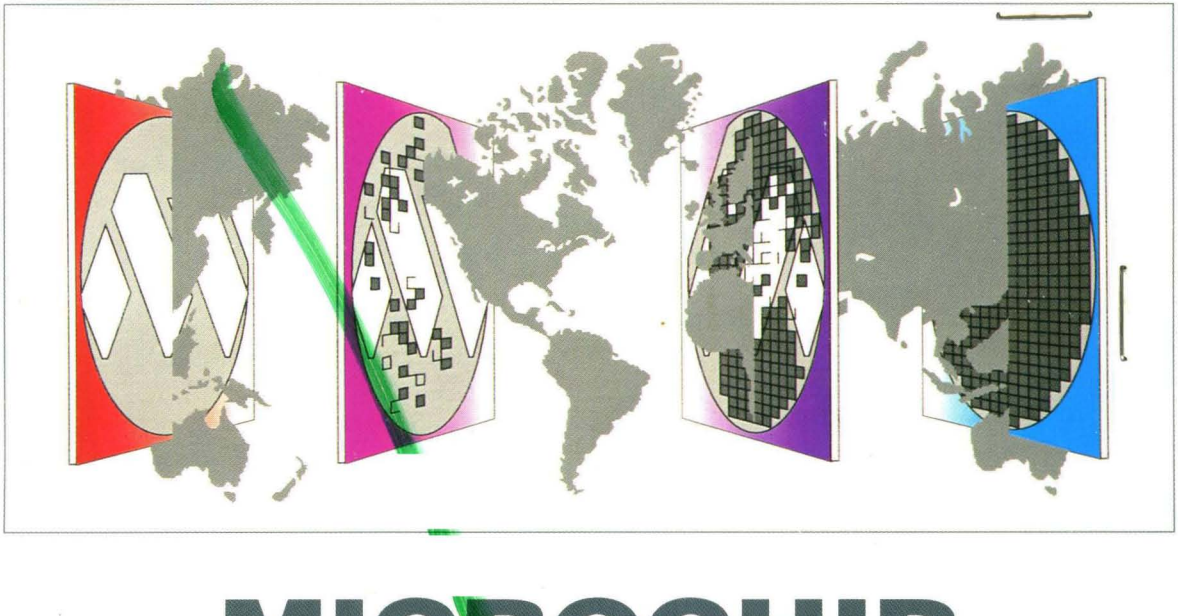


MICROCHIP DATA BOOK

Embedded Control VLSI Solutions

Microchip

Microchip Data Book

1992 Second Edition

SERVING A COMPLEX AND COMPETITIVE
WORLD WITH USER - PROGRAMMABLE
EMBEDDED CONTROL
SYSTEM SOLUTIONS

October 1992 / DS00018E

Table of Contents

Table of Contents

4

5

6

7

8

SERVING A COMPLEX AND COMPETITIVE WORLD WITH USER-PROGRAMMABLE EMBEDDED CONTROL SYSTEM SOLUTIONS

Motivated by customer requirements....

"Microchip Technology draws its impetus from the technology expectations of a large base of longstanding customers. Microchip is small enough to respond quickly with technology to serve our customers' needs. Moreover, as a fully integrated IC Manufacturer, Microchip deploys its panoply of resources to act timely and efficiently, and on a worldwide scale: Technology Development, Design, Wafer Fabrication, Assembly and Test, Quality, Reliability and Customer Support.

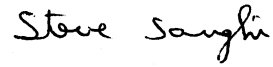
...and powered by continuous improvement...

"Worldwide competition leaves no room for divergence or mediocrity. Microchip Technology, committed to focus on and continuously improve all the aspects of its business, has a unique corporate culture. To improve performance, our employees are encouraged to analyze their methods continually. Personal empowerment expands the capability of personal responsibility to continually serve our customers better.

...riding and leading the wave of technological change.

"Our industry's life-line is innovation. The fast pace of technological change is inherent in our industry. Microchip Technology has accelerated the rate of change of its technology and products to leadership in providing user-programmable space-sensitive embedded control solutions.

"Change is our ally. Driving and managing customer-focused change is our winning strategy."



Steve Sanghi
President & Chief Executive Officer

MICROCHIP TECHNOLOGY INCORPORATED

Company Profile

HIGHLIGHTS

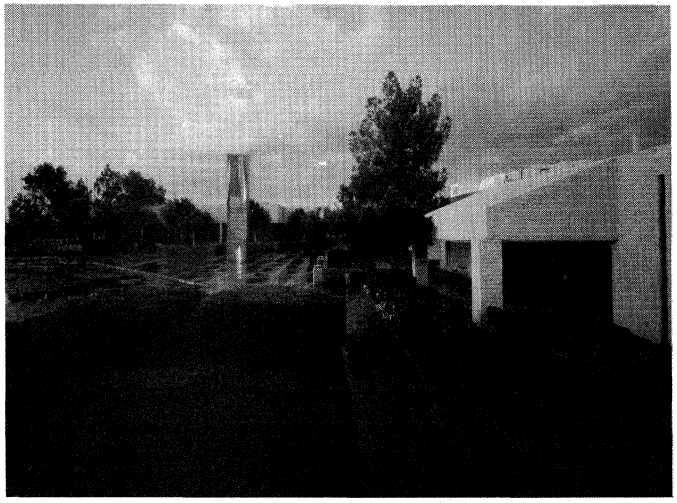
- Focused on user-programmable embedded control solutions
- Providing RISC 8-bit user-programmable microcontrollers and supporting logic products
- Providing Serial and Parallel EEPROMs and EPROMs
- A unique corporate culture dedicated to continuous improvement
- Research and development of high performance user-programmable products
- A history of innovation
- An experienced executive team focussed on innovation
- Quality without compromise
- Fully integrated manufacturing
- A global network of manufacturing and customer support facilities

BUSINESS SCOPE

Microchip Technology Inc. manufactures and markets a variety of VLSI CMOS semiconductor components to support the user-programmable embedded control market. In particular, the company specializes in highly integrated, user-programmable RISC microcontrollers and related non-volatile memory products to meet growing market requirements for high performance, yet economical embedded control capability in an increasing number of price-sensitive products. Microchip's products feature the industry's most economical OTP (one-time programmable) capability, along with the compact size, integrated functionality, ease of development and technical support so essential to timely and cost-effective product development by our customers.

MARKET FOCUS

Microchip targets selected markets where our advanced designs, progressive process technology and industry leading operating speeds enable us to deliver decidedly superior performance. The firm has positioned itself to maintain a dominant role as a supplier of high performance user-programmable microcontrollers and associated memory and logic products for embedded control applications.



Company headquarters in Chandler, Arizona: Executive Offices, R & D, and Wafer Fabrication occupy this campus.

GUIDING VALUES

Customers Are Our Focus

We establish successful customer partnerships by exceeding customer expectations for products, services and attitude. We earn our credibility through meeting commitments and producing quality products and services in a timely fashion. We believe each employee must effectively serve their internal customers in order for Microchip's external customers to be properly served.

Quality Comes First

We will perform correctly the first time, maintain customer satisfaction and measure our quality against requirements. We practice effective and standardized improvement methods, such as statistical process control to anticipate problems and implement root cause solutions. We believe that when quality comes first, reduced costs follow.

Continuous Improvement Is Essential

We utilize the concept of 'Vital Few" to establish our priorities. We concentrate our resources on continuously improving the Vital Few while empowering each employee to make continuous improvements in their area of responsibility. We strive for constructive and honest self-criticism to identify improvement opportunities.

Employees Are Our Greatest Strength

We design jobs and provide opportunities in a fashion which clearly promotes pride in work, integrity, trust, teamwork, creativity, employee involvement and development, fairness, and productivity. We base recognition, advancement and compensation on an employee's achievement of excellence in team and individual performance. We provide for employee health and welfare by offering a competitive, comprehensive employee benefits program.

Products And Technology Are Our Foundation

We commit to ongoing investments and advancements in the design and development of our manufacturing process, device circuit and system technologies, which provide innovative, reliable and cost-effective products to support current and future market opportunities.

Total Cycle Times Are Competitive

We focus resources to optimize cycle times to our customers by empowering employees to achieve efficient cycle times in their area of responsibility. We believe that cycle time reduction is achieved by streamlining processes through the systematic removal of barriers to productivity.

Safety Is Never Compromised

We place our concern for safety of our employees and community at the forefront of our decisions, policies and actions. Each employee is responsible for safety.

Profits Provide For Everything We Do

We strive to maintain competitive profits as they allow continued investments and future growth, and indicate the overall success of Microchip.

Communication Is Vital

We encourage open, honest, constructive, and ongoing communication in all company and community relationships to resolve issues, exchange information and share knowledge.

Suppliers, Representatives, And Distributors Are Our Partners

We maintain mutually beneficial partnerships with suppliers, representatives, and distributors who are an integral link in the achievement of our mission and guiding values.

Professional Ethics Are Practiced

We manage our business and treat customers, employees, shareholders, investors, suppliers, distributors, representatives, community and government in a manner that exemplifies our honesty, ethics and integrity. We recognize our responsibility to the community and are proud to serve as an equal opportunity employer.

PRODUCT FOCUS

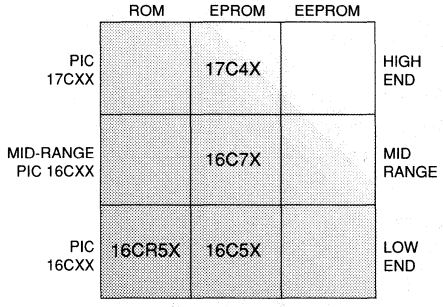
Microchip's product focus is user-programmable microcontrollers, nonvolatile memories and supporting logic. These product lines include PIC® microcontrollers, EEPROMs, and High Speed EPROMs in a broad range of technologies, speeds and packages.

Microchip is quick to capitalize on advances in one product line by incorporating those breakthroughs into other product families. Microchip targets selected markets where our advanced designs, progressive process technology and industry leading operating speeds enable us to deliver decidedly superior performance. The firm has recently positioned itself to play a dominant role as a supplier of high performance user-programmable microcontrollers and associated memory and logic products for embedded control applications.

MICROCONTROLLERS

PIC® Microcontrollers from Microchip combine high performance, low cost, and small package size. They offer the best price/performance ratio in the industry. Large numbers of these devices are used in automotive and cost-sensitive consumer products, such as remote controls and appliances, computer peripherals, data entry, office automation, automotive control systems, security, and telecom applications.

The widely accepted NMOS PIC16XX (over 75 million units shipped) and CMOS PIC16CXX and PIC17CXX series are the industry's only 8-bit microcontrollers using a high speed RISC architecture. Microchip pioneered the use of RISC architecture to obtain high speed and instruction efficiency. The CMOS PIC16CXX is in high volume production, with more than 25 million units shipped, and has achieved nearly five thousand design wins worldwide.



CMOS PIC Microcontroller Families

The PIC17CXX family is the world's highest performance 8-bit microcontroller. It continues PIC's high performance RISC architecture with an 8-bit data word and 16-bit instruction word, allowing expanded internal/external memory. The PIC17C42 incorporates advanced motor control peripherals allowing control of two single-phase motors with a single PIC17C42. High performance inter-controller communications can be implemented with the PIC17C42's 4-megabits-per-second serial I/O.

Future CMOS PIC product families will include advanced features, such as higher speed, additional I/O, sophisticated timers, embedded A/D, extended instruction/data memory, inter-processor communication, and ROM, EPROM and E²PROM memories.

DEVELOPMENT SYSTEMS

Both PIC16CXX and PIC17CXX families are supported by a range of user-friendly development systems including programmers, emulators and demonstration boards.

PICMASTER™ is an advanced real-time emulator system using the user friendly Windows® software environment. PICMASTER™ is a Microchip-designed universal emulator for both PIC16CXX and PIC17CXX families. PIC PRO II and PRO MASTER are advanced low cost programmers.

SOFTWARE SUPPORT

Both PIC families are supported by a selection of support software including assemblers, linker/loaders and libraries. The PIC16C5X family is also supported by a software simulator.

A full-featured compiler is under development to support both families.

Customers can obtain on-line updates on Microchip Development Systems and Support Software via the Electronic Bulletin Board System, "EBBS."

SERIAL EEPROMs

Microchip offers one of the broadest selections of CMOS Serial EEPROMs on the market for embedded control systems. Serial EEPROMs are available in variety of densities, operating voltages, bus interface protocols, operating temperature ranges and space saving packages. Device densities range from 1K bits up to 16K bits. In addition to 5V only operation, Microchip offers serials that read and write either at 2.5 or 2 volts. I²C™, Microwire™ and 4 wire bus interface protocols are standard. Devices come in three standard operating temperature ranges; commercial, industrial and automotive. Small footprint packages include: 8 pin DIP, 8 pin SOIC in JEDEC and EIAJ body widths and 14 pin SOIC. Other key features of the Serial EEPROM product line include: ESD protection greater than 4K volts and endurance of 100K cycles worst case and 1M typical.

Microchip is a high volume supplier of Serial EEPROMs to all the major markets worldwide, i.e. consumer, automotive, industrial, computer and communications. Microchip is developing leading edge unique serial EEPROMs.

PARALLEL EEPROMs

The CMOS EEPROM devices from Microchip are available in 4K, 16K, and 64K densities. The manufacturing process used for these EEPROMs ensures 10,000 to 100,000 write and erase cycles. Data retention is over 10 years. Short write times are less than 200 µsec. These EEPROMs work reliably under demanding conditions and operate efficiently at temperatures from -55 °C to +125 °C. Microchip's expertise in surface mount packaging supports our customers' needs in space-sensitive applications.

Typical applications include computer peripherals, engine control, pattern recognition and telecommunications.

EPROMs

Microchip's CMOS EPROM devices are produced in densities from 64K to 512K. High Speed EPROMs have access times as low as 55 nanoseconds. Typical applications include computer peripheral, military, instrumentation, and automotive devices. Microchip's expertise in Surface Mount Packaging led to the development of the Surface Mount OTP EPROM market where Microchip is the #1 supplier today. Microchip is also a leading supplier of low voltage EPROMs for battery powered applications.

MILITARY PRODUCTS

Microchip delivers military devices that conscientious engineers can use with confidence. Our 883C compliant parts cover all quality fronts: DESC standard military drawing approval, high speed performance and quick turn availability.

Microchip's military products include CMOS memories, CMOS/NMOS digital signal processors and microcontrollers - all highly reliable with fast access times and proven retention. Endurance is guaranteed in both dual in-line cerdip packages and leadless chip carriers.

OTHER MICROCHIP PRODUCTS

Other Microchip products, such as DSP products and Liquid Crystal Display Drivers, are mature products with proven track record and a large, repeat customer base. Microchip provides a wide package selection of single-chip DSPs that can be programmed for a wide variety of applications. Several variants of the industry standard 32010 and 320C10 are offered at speeds up to 25 MHz. The 320 DSP family is often found in commercial and military applications where medium and high performance parts are required.

RESEARCH AND DEVELOPMENT OF PERFORMANCE PRODUCTS

Microchip's research and development activities, include exploring new process technologies and products that have industry leadership potential. Particular emphasis is placed on products that can be put to work in high performance embedded control markets.

Equipment is continually updated to bring the most sophisticated process, CAD and testing on line. Cycle times for new technology development are continuously reduced to bring innovative new products to our customers.

FUTURE PRODUCTS AND TECHNOLOGY

New process technology is constantly being developed for EEPROM, High Speed EPROM, and microcontroller products. Advanced process technology modules are being developed that will be integrated into our present product lines to achieve a range of compatible processes. Current production technology utilizes dimensions down to 0.9 microns.

More advanced technologies are under development, as well as advanced CMOS RISC-based microcontroller and CMOS EEPROM products. Objective specifications for new products are developed by close cooperation with our many customer-partners worldwide.

FULLY INTEGRATED MANUFACTURING

Microchip delivers fast turnaround through total control over all phases of production. Design, product development, mask making, wafer fabrication, assembly and quality assurance testing are conducted at facilities owned and operated by Microchip. Our integrated approach to manufacturing along with rigorous use of advanced statistical process control, continuous improvement and implementation of root cause solutions to problems, has brought forth tight product consistency levels and high yields which enable Microchip to compete successfully in world markets. Microchip's unique approach to SPC provides customers with excellent costs, quality, reliability and on-time delivery.

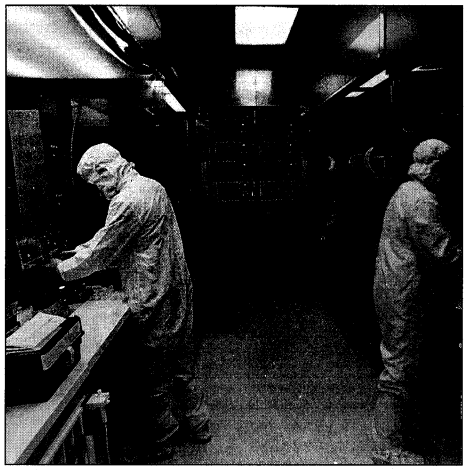
A GLOBAL NETWORK OF PLANTS AND FACILITIES

Microchip is a global competitor providing local service to the world's technology centers. The Company's focal point is the design and technology advancement facility in Chandler, Arizona. Most military and high performance parts emanate from here, along with front end wafer fabrication and electrical probing.

Microchip's assembly and test facility in Kaohsiung, Taiwan houses the technology and modern assembly methods necessary for plastic and ceramic packaging.

Sales and application offices are located in key cities throughout the Americas, Pacific Rim and Europe. Offices are staffed to meet the high quality expectations of our customers, and can be accessed for technical support, purchasing information and failure analysis.

CHANDLER, AZ FACILITY

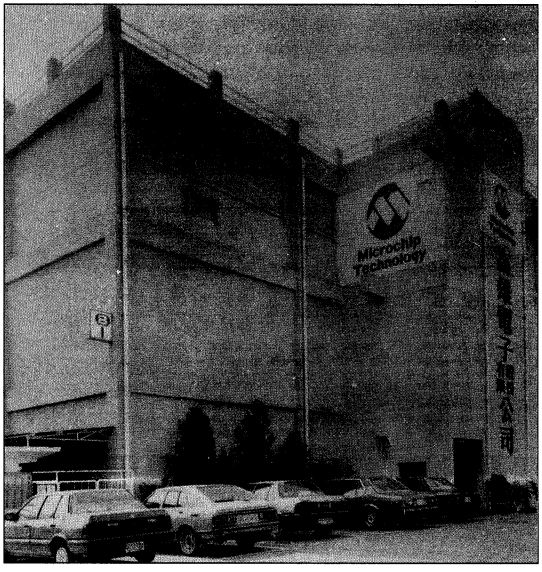


Chandler Wafer Fabrication: Diffusion Area

Chandler Wafer Fab: Sub-micron Alignment Area

TAIWAN FACILITY

Microchip Technology Taiwan, established in 1966, was the first semiconductor manufacturing company in the Kaohsiung export processing zone in south Taiwan.



Microchip's Kaohsiung plant has progressively developed into an assembly and test facility of the highest standards.

The plants' excellent track record and continuing efforts to achieve higher levels of quality and technological advancement has resulted in superior yields and fast turnaround.

QUALITY WITHOUT COMPROMISE

Product reliability is designed into Microchip products at the outset. Design margins are established to guarantee that every product can be easily produced, error-free and operates well beyond the tolerances of the manufacturing process.

All our quality assurance tests are run to tighter than customer specifications. Products are tested at least two machine tolerances higher than those specified by the customer.

Every new product is measured under accelerated stress testing. Qualification samples encompass the full range of processed tolerances at each step. Data sheets detailing these processes enable customers to reach accurate decisions based on known quantitative values.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at each process step. In-process controls are performed by operators in the wafer fabrication division and immediate corrective action is taken if they deem a process is out of our very tight SPC control limits. Products are also sampled weekly through a variety of carefully monitored stress and accelerated life tests.

Microchip's positive documentation control program assures the correct document is always available at the point of use.

CONTINUOUS IMPROVEMENT

Individuals in all departments analyze the methods employed in their positions and formulate plans to improve performance. This continuous improvement process is never completed. Screening efforts alone are never considered enough. In all areas of our business, everyone is expected to make continuous improvements to support their part of Microchip's unique culture.

FORMING A QUALITY ALLIANCE WITH CUSTOMERS

Microchip works in tandem with customers to establish mutual programs to improve the performance of our products in their systems. Microchip's quality and reliability support is extended through final shipment of our customer's products. Microchip's quality programs ensure that our products can be used with such confidence that a customer can implement improvement programs centered on us as a supplier.

SECTION 1
MICROCONTROLLER PRODUCT SPECIFICATIONS

Microchip

PIC®16C5X

EPROM-Based 8-Bit CMOS Microcontroller Series

1

FEATURES

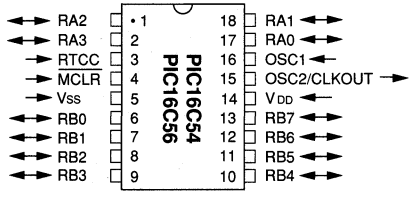
High Performance RISC-like CPU
- Only 33 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 12-bit wide instructions
- 8-bit wide data path
- 512 - 2K x 12 on-chip EPROM program memory
- 25 - 72 x 8 general purpose registers (SRAM)
- 7 special function hardware registers
- 2 level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features
- 12 - 20 I/O pins with individual direction control
- 8 bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power on reset
- Oscillator start-up timer
- Watchdog timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- EPROM fuse selectable oscillator options:
  - Low cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - High speed crystal/resonator: HS
  - Power saving low frequency crystal: LP

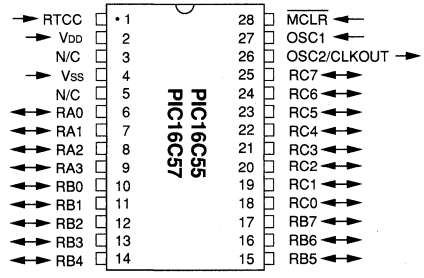
CMOS Technology
- Low power, high speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.5V to 6.25V
  - Industrial: 2.5V to 6.25V
  - Automotive: 2.5V to 6.0V
- Low power consumption
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 KHz
  - < 3 µA typical standby current @ 3V, 0°C to 70°C

FIGURE A - PIN CONFIGURATIONS

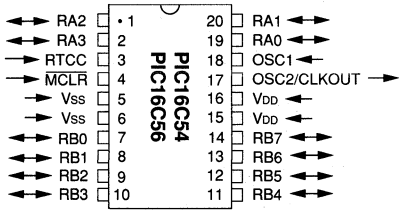
PDIP, SOIC, CERDIP Window



PDIP, SOIC, CERDIP Window



SSOP



SSOP

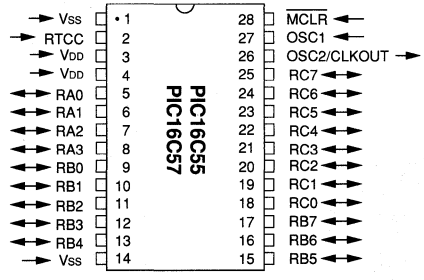


Table of Contents

Table of Figures

Table of Tables

1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family low cost, high performance, 8-bit, fully static, EPROM based CMOS microcontrollers. It employs a RISC-like architecture with only 33 single word/single cycle instructions to learn. All instructions are single cycle (200ns) except for program branches which take two cycles. The PIC16C5X delivers performance an order of magnitude higher than its competitors in similar price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special microcontroller like features that reduce system cost and power requirements. The power on reset and oscillator start up timer eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, watchdog timer and code protection features improves system cost, power and reliablity.

The UV-erasable cerdip-packaged versions are ideal for code development while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontroller while benefiting from the OTP flexibility.

The PIC16C5X products are supported by an assembler, a software simulator, an in-circuit emulator and a production quality programmer. All the tools are supported by IBM PC and compatible machines.

1.1 APPLICATIONS

The PIC16C5X series fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices, and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use, and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

TABLE 1.0.1 - OVERVIEW OF PIC16C5X DEVICES

Part #	EPROM	RAM*	I/O†	Package Options
PIC16C54	512 x 12	32 x 8	13	18L windowed CERDIP, 18L PDIP, 18L SOIC (300 mil), 20L SSOP
PIC16C55	512 x 12	32 x 8	21	28L windowed CERDIP, 28L PDIP (600 mil), 28L PDIP (300 mil), 28L SOIC (300 mil), 28L SSOP
PIC16C56	1K x 12	32 x 8	13	18L windowed CERDIP, 18L PDIP, 18L SOIC (300 mil), 20L SSOP
PIC16C57	2K x 12	80 x 8	21	28L windowed CERDIP, 28L PDIP (600 mil), 28L PDIP (300 mil), 28L SOIC (300 mil), 28L SSOP

* Including special function registers.
** The industrial versions and the HS version operates for V_{DD} range of 4.5 V to 5.5 V (see DC specs).
† Includes RTCC pin.

2.0 ARCHITECTURAL DESCRIPTION

2.1 Harvard Architecture

The PIC16C5X single-chip microcomputers are low-power, high-speed, full static CMOS devices containing EPROM, RAM, I/O, and a central processing unit on a single chip.

The architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8-bits wide while the program bus and program memory (EPROM) have a width of 12-bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. That means that, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the PIC16C5X series is given in Figure 2.1.1.

2.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 2.2.1.

FIGURE 2.1.1 - PIC16C5X SERIES BLOCK DIAGRAM

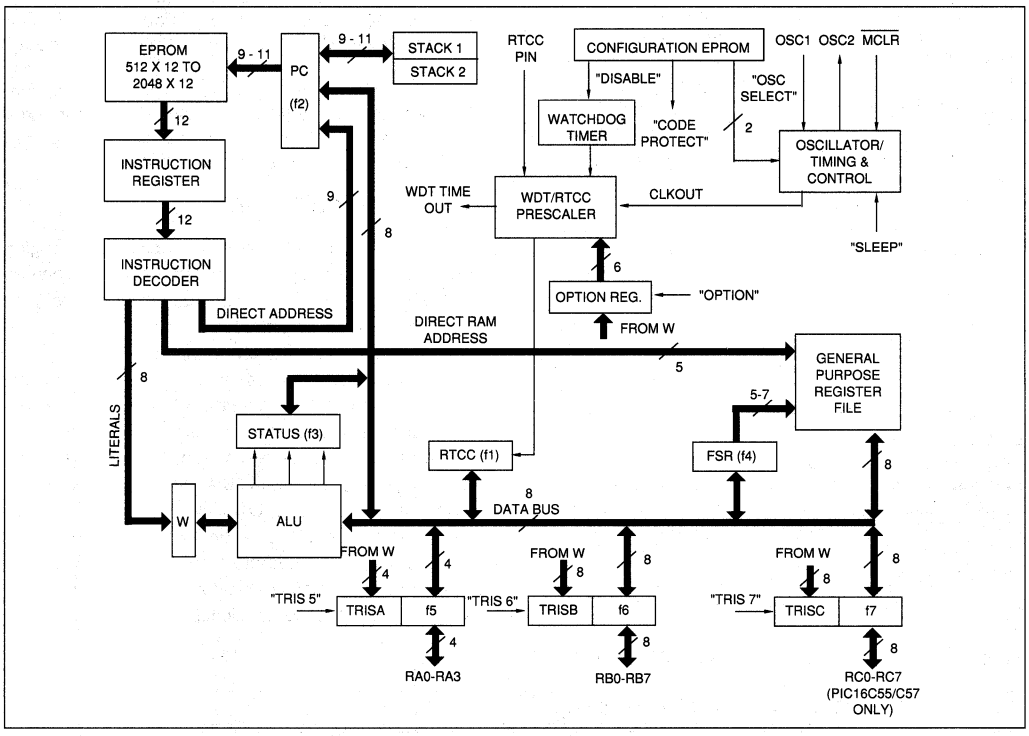


TABLE 2.1.1 - PIN FUNCTIONS

Name	Function
RA0 - RA3	I/O PORT A
RB0 - RB7	I/O PORT B
RC0 - RC7	I/O PORT C (C55/57 only)
RTCC	Real Time Clock/Counter
MCLR	Master Clear
OSC1	Oscillator (input)
OSC2/CLKOUT	Oscillator (output)
VDD	Power supply
VSS	Ground
N/C	No (internal) Connection

2.3 Data Register File

The 8-bit data bus connects two basic functional elements together: the Register File composed of up to 80 addressable 8-bit registers including the I/O Ports, and an 8-bit wide Arithmetic Logic Unit. The 32 bytes of RAM are directly addressable while a "banking" scheme, with banks of 16 bytes each, is employed to address larger data memories (Figure 4.2.1). Data can be addressed direct, or indirect using the file select register (f4). Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.

The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs), and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.

In addition, special purpose registers are used to control the I/O port configuration, and the prescaler options.

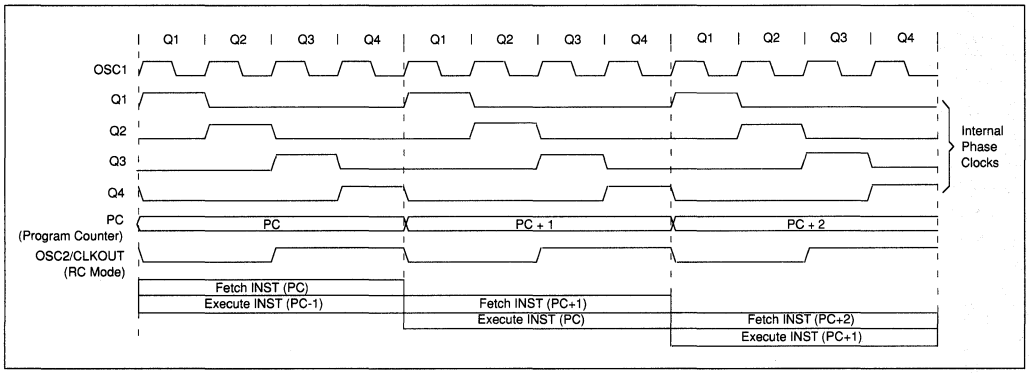
2.4 Arithmetic/Logic Unit (ALU)

The 8-bit wide ALU contains one temporary working register (W Register). It performs arithmetic and Boolean functions between data held in the W Register and any file register. It also does single operand operations on either the W register or any file register.

2.5 Program Memory

Up to 512 words of 12-bit wide on-chip program memory (EPROM) can be directly addressed. Larger program memories can be addressed by selecting one of up to four available pages with 512 words each (Figure 4.3.1). Sequencing of microinstructions is controlled via the

FIGURE 2.2.1 - CLOCKS/INSTRUCTION CYCLE



Program Counter (PC) which automatically increments to execute in-line programs. Program control operations, supporting direct, indirect, relative addressing modes, can be performed by Bit Test and Skip instructions, Call instructions, Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

3.0 PIC16C5X SERIES OVERVIEW

A wide variety of EPROM and RAM sizes, number of I/O pins, oscillator types, frequency ranges, and packaging options is available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C5X Product Identification System" on the back page of this data sheet to specify the correct part number.

3.1 UV Erasable Devices

Four different device versions, as listed in Table 3.1.1, are available to accommodate the different EPROM, RAM, and I/O configurations. These devices are optimal for prototype development and pilot series. The desired oscillator configuration is EPROM programmable as "RC", "XT", "HS" or "LP". An erased device is configured as "RC" type by default. Depending on the selected oscillator type and frequency, the operating supply voltage must be within the same range as a OTP/QTP part would be specified for.

The available PIC development tools "PICPRO™ and PICPRO™ II can program all PIC16C5X devices for prototyping and pilot series up to low-volume production.

3.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates. OTP devices have the oscillator type pre-configured by the factory, and they are tested only for this special configuration (including voltage and frequency ranges, current consumption). Table 3.2.1 gives an overview about devices available now and planned for future release.

The program EPROM is erased, allowing the user to write the application code into it. In addition, the watchdog timer can be disabled, and/or the code protection logic can be activated by programming special EPROM fuses. The sixteen special EPROM bits for ID code storage are also user programmable.

3.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices (see Table 3.2.1) but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

4.0 OPERATIONAL REGISTER FILES

4.1 f0 Indirect Data Addressing

This is not a physically implemented register. Addressing f0 calls for the contents of the File Select Register to be used to select a file register. f0 is useful as an indirect address pointer. For example, in the instruction ADDWF f0, W will add the contents of the register pointed to by the FSR (f4) to the content of the W Register and place the result in W.

If f0 itself is read through indirect addressing (i.e. FSR = 0h), then 00h is read. If f0 is written to via indirect addressing, the result will be a NOP.

4.2 f1 Real Time Clock/Counter Register (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin, or by the internal instruction cycle clock (CLKOUT=fosc/4). Figure 4.1.1 is a simplified block diagram of RTCC.

An 8-bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. OPTION register is a special register (not mapped in data memory) addressable using the 'OPTION' instruction. See section 7.5 for details. If the prescaler is assigned to the RTCC, instructions writing to f1 (e.g. CLRF 1, or BSF1,5, ...etc.) clear the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines, if f1 is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines, if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

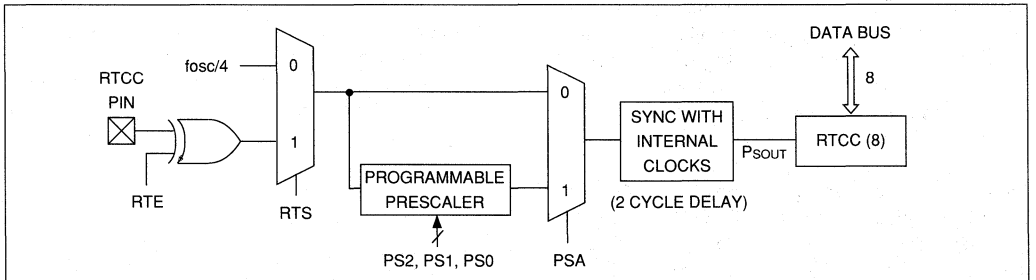
RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= Fosc/4). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. However, the RTCC pin must be tied to VDD or VSS, whatever is convenient, to prevent unintended entering of test modes and to reduce the current consumption in low power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), f1 keeps incrementing and just rolls over when the value "FFh" is reached. All increment pulses for f1 are delayed by two instruction cycles. After writing to f1, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before f1 is incremented. This is true for instructions that either write to or read-modify-write RTCC (e.g. MOVF f1, CLRF f1). For applications where RTCC needs to be tested for zero without affecting its count, use of MOVF f1, W instruction is recommended. Timing diagrams in Figure 4.2.2 show RTCC read, write and increment timing.

4.2.1 USING RTCC WITH EXTERNAL CLOCK

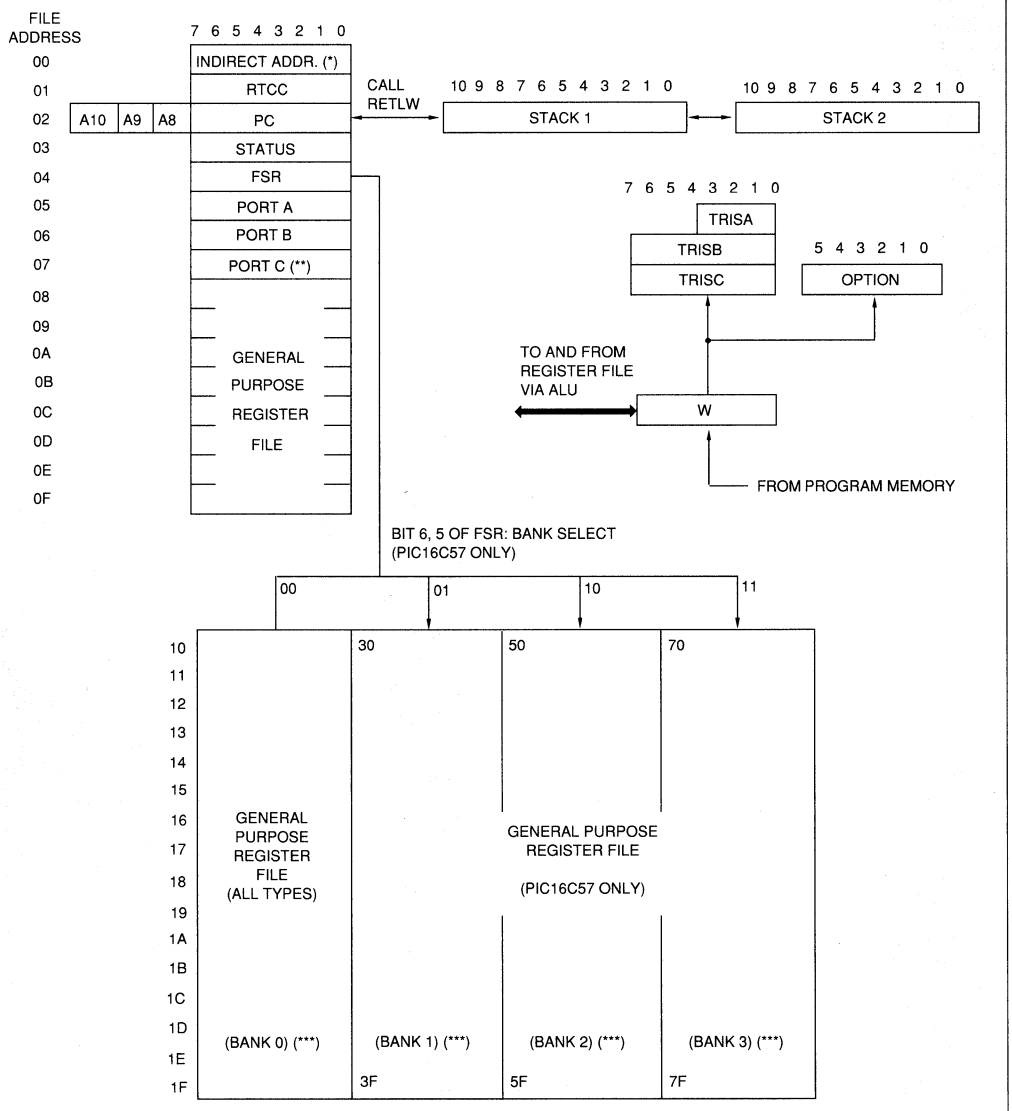
When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements.

FIGURE 4.1.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in option register.
2. The prescaler is shared with Watchdog Timer (see Figure 9.0.1).

FIGURE 4.2.1 - PIC16C5X DATA MEMORY MAP



(*) NOT A PHYSICALLY IMPLEMENTED REGISTER. SEE SECTION 4.0 OR DETAILS
(**) FILE f7 IS A GENERAL PURPOSE REGISTER ON THE PIC16C54/C56
(***) BANK 0 IS AVAILABLE ON ALL MICROCONTROLLERS WHILE BANK 1 TO BANK 3 ARE ONLY AVAILABLE ON THE PIC16C57. (SEE SECTION 4.6 FOR DETAILS)

Also there is some delay from the occurance of the external clock edge to the actual incrementing of RTCC. Referring to Figure 4.1.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 5) is the same as RTCC clock input and therefore the requirements are:

TRTH = RTCC high time ≥ 2tosc + 20 ns
TRTL = RTCC low time ≥ 2tosc + 20 ns

When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.
Then: PSOUT high time = PSOUT low time = $\frac{N.T_{RT}}{2}$
where TRT = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore $\frac{N.T_{RT}}{2}$ ≥ 2 tosc + 20 ns, or TRT ≥ $\frac{4\ tosc + 40\ ns}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10 ns is required. In summary, the RTCC input requirements are:

TRT = RTCC period ≥ (4 tosc + 40 ns)/N
TRTH = RTCC high time ≥ 10 ns
TRTL = RTCC low time ≥ 10 ns

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to Figure 4.2.3, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200 ns @ 20 MHz).

4.3 f2 Program Counter

The program counter generates the addresses for up to 2048 x 12 on-chip EPROM cells containing the program instruction words (Figure 4.3.1).

Depending on the device type, the program counter and its associated two-level hardware stack is 9 - 11-bits wide.

TABLE 4.3.1 - PROGRAM COUNTER STACK WIDTH

Part #	PC width	Stack width
PIC16C54/PIC16C55	9 bit	9 bit
PIC16C56	10 bit	10 bit
PIC16C57	11 bit	11 bit

The program counter is set to all "1"s upon a RESET condition. During program execution it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

FIGURE 4.2.2A - RTCC TIMING: INT CLOCK/NO PRESCALE

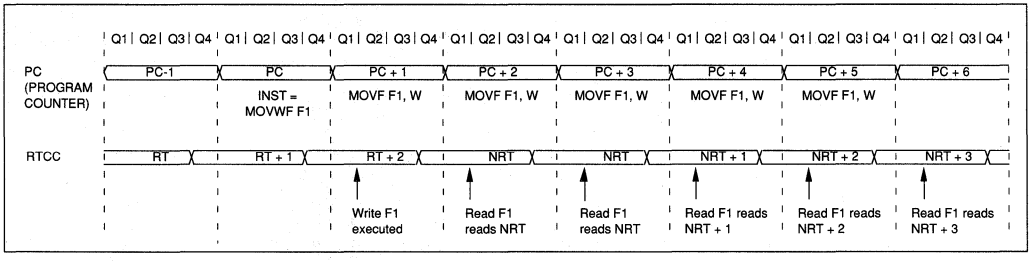
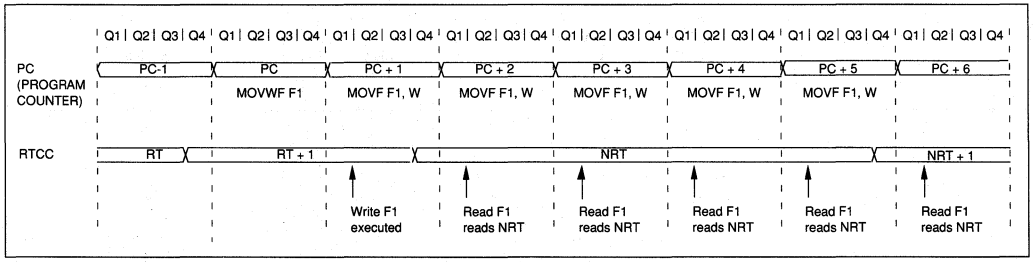


FIGURE 4.2.2B - RTCC TIMING: INT CLOCK/PRESCALE 1:2



a) "GOTO" instructions allow the direct loading of the lower 9 program counter bits (PC <8:0>). In case of PIC16C56/PIC16C57, the upper two bits of PC (PC<10:9>) are loaded with page select bits PA1, PA0 (bits 6,5 status register). Thus GOTO allows jump to any location on any page.

b) "CALL" instructions load the lower 8-bit of the PC directly while the ninth bit is cleared to "0". The PC value, incremented by one, will be pushed into the stack. In case of PIC16C56, PIC16C57, the upper two bits of PC (PC<10:9>) are loaded with Page Select bits PA1, PA0 (bits 6,5 status register).

c) "RETLW" instructions load the program counter with the top of stack contents.

d) If PC is the destination in any instruction (e.g. MOVWF 2, ADDWF 2, or BSF 2,5) then the computed 8-bit result will be loaded into the low 8-bits of program counter. The ninth bit of PC will be cleared. In case of PIC16C56/PIC16C57, PC<10:9> will be loaded with Page Select bits PA1, PA0 (bits 6,5 in status register).

It should be noted that because bit 8 (ninth bit) of PC is cleared in CALL instruction or any instruction which writes to the PC (e.g. MOVWF 2), all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

MORE ON PROGRAM MEMORY PAGE SELECT (PIC16C56/PIC16C57 ONLY):

Incrementing the program counter when it is pointing to the last address of a selected memory page is also possible and will cause the program to continue in the next higher page. However, the page pre-select bits in f3 will not be changed, and the next "GOTO", "CALL", "ADDWF 2", "MOVWF 2" instruction will return to the previous page, unless the page pre-select bits have been updated under program control. For example, a "NOP" at location "1FF" (page 0) increments the PC to "200" (page 1). A "GOTO xxx" at "200" will return the program to address "xxx" on page "0" (assuming that the page preselect bits in file register f3 are "0").
Upon a RESET condition, page 0 is pre-selected while the program counter addresses the last location in the last page. Thus, a "GOTO" instruction at this location will automatically cause the program to continue in page 0.

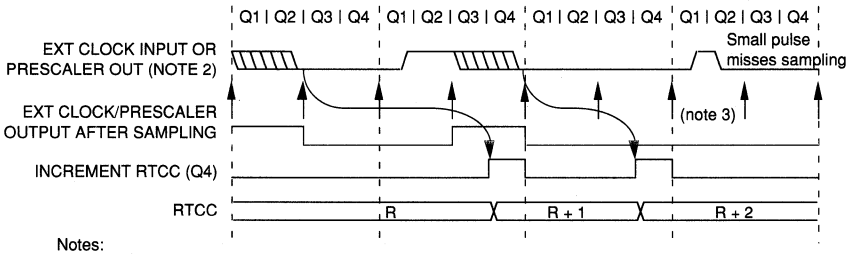
4.4 Stack

The PIC16C5X series employs a two level hardware push/pop stack (Figure 4.3.1).

CALL instructions push the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than 2 subsequent "CALL"s are executed, only the most recent two return addresses are stored.
For the PIC16C56 and PIC16C57, the page preselect bits of f3 will be loaded into the most significant bits of the program counter. The ninth bit is always cleared to "0" upon a CALL instruction. This means that subroutine entry addresses have to be located always within the lower half of a memory page (addresses 000-0FF, 200-2FF, 400-4FF, 600-6FF). However, as the stack has always the same width as the PC, subroutines can be called from anywhere in the program.

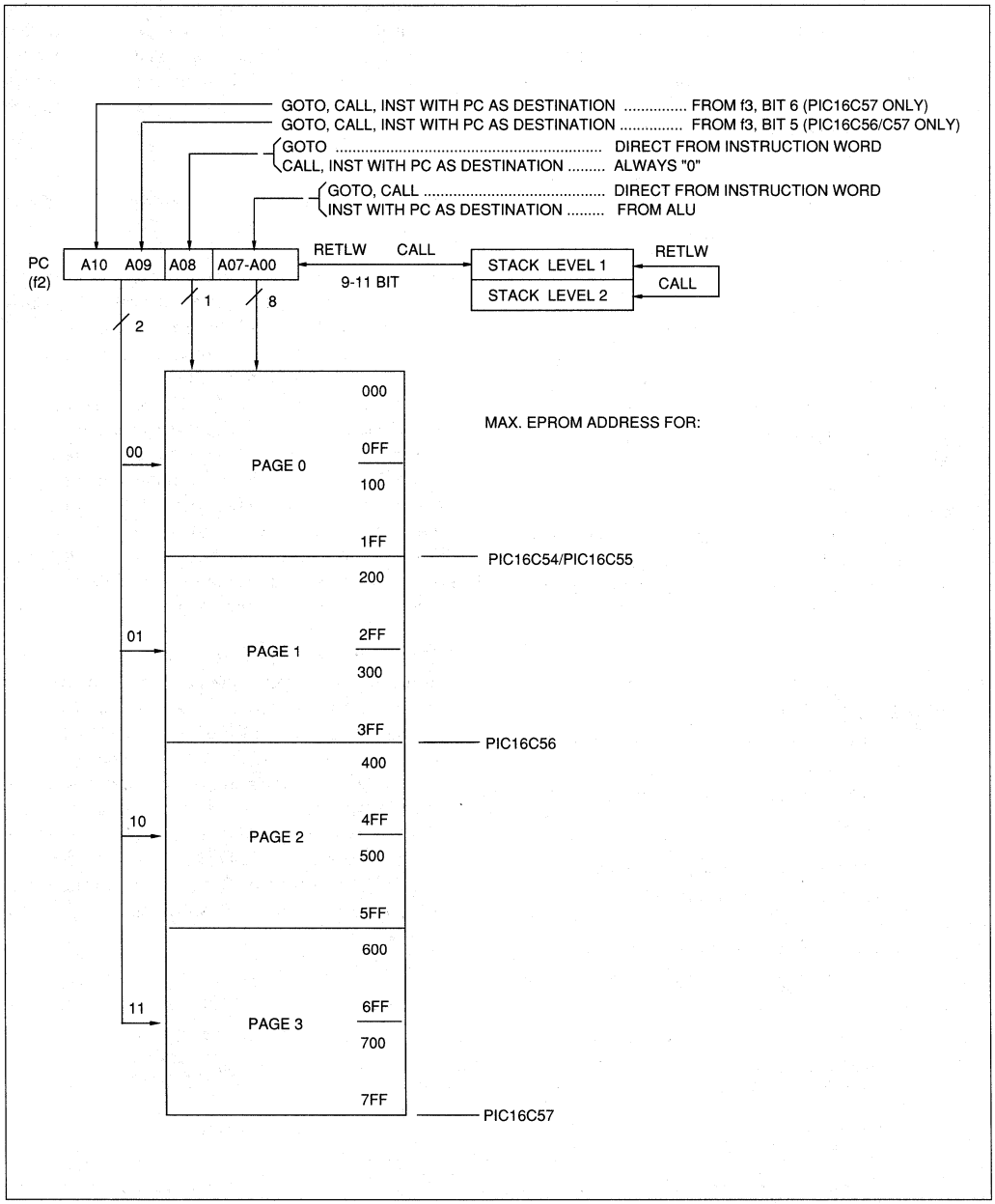
RETLW instructions load the contents of stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than 2 subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2. For the PIC16C56 and PIC16C57, the return will be always to the page from where the subroutine was called, regardless of the current setting of the page pre-select bits in file register f3. Note that the W register will be loaded with the literal value specified in the RETLW instruction. This is particularly useful for the implementation of "data" tables within the program memory.

FIGURE 4.2.3 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:
1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

FIGURE 4.3.1 - PROGRAM MEMORY ORGANIZATION



4.5 f3 Status Word Register

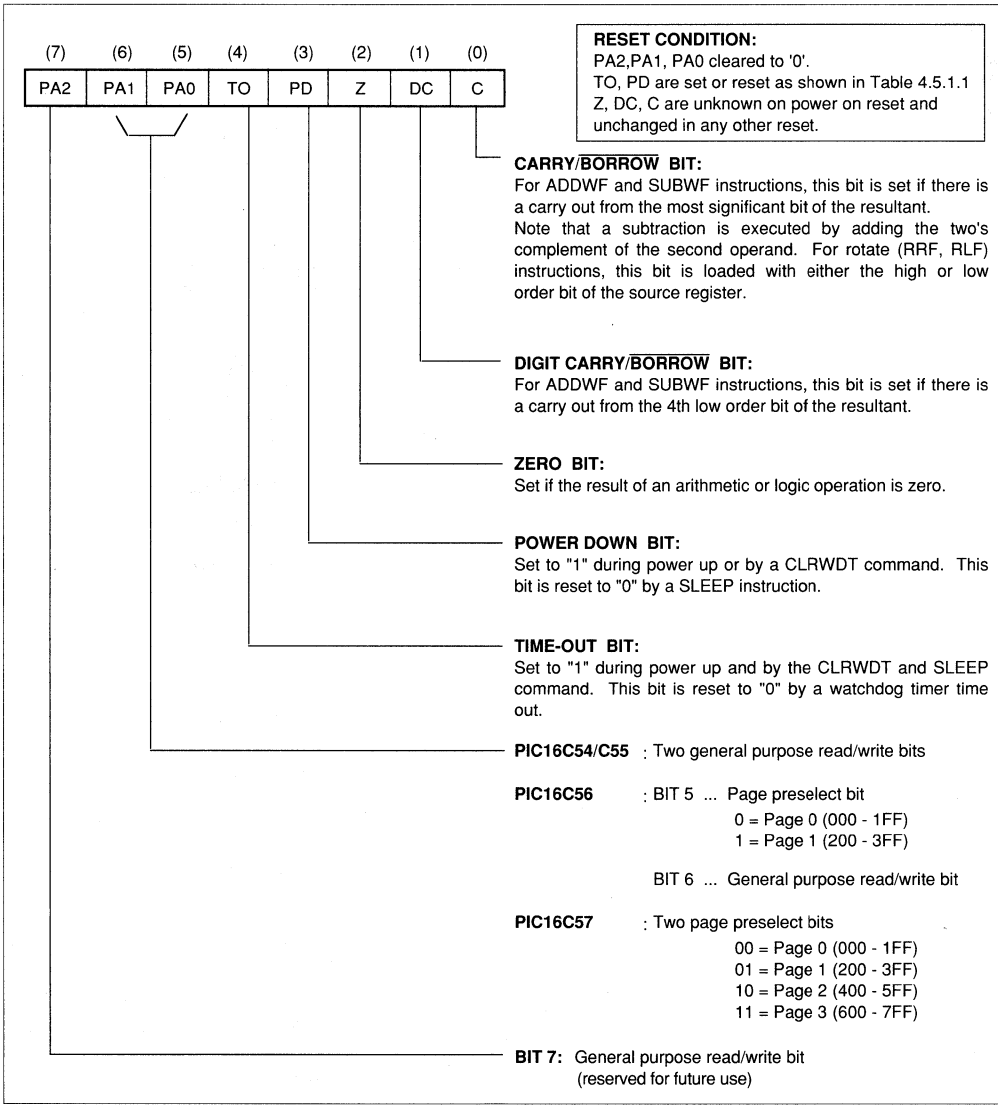
This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for larger program memories than 512 words (PIC16C56, PIC16C57).

The status register (f3) can be destination for any instruction like any other register. However, the status bits are set after the following write. Furthermore, TO and PD bits are not writable. Therefore, the result of an instruction with status register as destination may be different than intended. For example, CLRF f3 will clear all bits except for TO and PD and then set the Z bit and leave status register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the status registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see section "Instruction Set Summary" (Table 10.0.1).

FIGURE 4.5.1 - STATUS WORD REGISTER f3



4.5.1 CARRY/BORROW AND DIGIT CARRY/ BORROW BITS:

The Carry bit (C) is a carry out in addition operation (ADDWF) and a borrow out in subtract operation (SUBWF).
It is also affected by RRF and RLF instructions. The following examples explain carry/borrow bit operation:

```
;SUBWF Example #1
;
clrf   0x20    ;f(20h)=0
movlw  1       ;wreg=1
subwf  0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
               ;Carry=0: Result is negative
;
;SUBWF Example #2
movlw  0xFF    ;
movwf  0x20    ;f(20h)=FFh
clrw           ;wreg=0
subwf  0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
               ;Carry=1:Result is positive
;
```

The digit carry operates in the same way as the carry bit, i.e. it is a borrow in subtract operation.

4.5.2 TIME OUT AND POWER DOWN STATUS BITS (TO, PD)

The "TO" and "PD" bits in the status register f3 can be tested to determine if a RESET condition has been caused by a watchdog timer time-out, a power-up condition, or a wake-up from SLEEP by the watchdog timer or MCLR pin.
These status bits are only affected by events listed in Table 4.5.2.1.

TABLE 4.5.2.1 - EVENTS AFFECTING PD/ TO STATUS BITS

Event	TO	PD	Remarks
Power-up	1	1	
WDT Timeout	0	X	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT timeout will occur regardless of the status of the TO bit. A SLEEP instruction will be executed, regardless of the status of the PD bit. Table 4.5.2.2 reflects the status of PD and TO after the corresponding event.

TABLE 4.5.2.2 - PD/TO STATUS AFTER RESET

TO	PD	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	MCLR wake-up from SLEEP
1	1	Power-up
X	X	= Low pulse on MCLR input

Note: The PD and TO bit maintain their status (X) until an event of Table 4.5.2.1 occurs. A low-pulse on the MCLR input does not change the PD and TO status bits.

4.5.3 PROGRAM PAGE PRESELECT (PIC16C56, PIC16C57 ONLY)

Bits 5-6 of the STATUS register are defined as PAGE address bits PA0 - PA1, and are used to preselect a program memory page. When executing a GOTO, CALL, or an instruction with PC (f2) as destination (e.g. MOVWF 2), PA0 - PA1 are loaded into bit A9-A10 of the program counter, selecting one of the available program memory pages. The direct address specified in the instruction is only valid within this particular memory page.
RETLW instructions do not change the page preselect bits.
Upon a RESET condition, PA0-PA2 are cleared to "0"s.

4.6 f4 File Select Register (FSR)

PIC16C54/C55/C56

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling for file f0 in any of the file oriented instructions).
Bits 5-7 of the FSR are read-only and are always read as "one"s.
If no indirect addressing is used, the FSR can be used as a 5-bit wide general purpose register.

PIC16C57 ONLY

Bit 5 and 6 of the FSR select the current data memory bank (Figure 4.2.1).
The lower 16 bytes of each bank are physically identical and are always selected when bit 4 of the FSR (in case of indirect addressing) is "0", or bit 4 of the direct file register address of the currently executing instruction is "0" (e.g. MOVWF 08).
Only if bit 4 in the above mentioned cases is "1", bits 5 and 6 of the FSR select one of the four available register banks with 16 bytes each.
Bit 7 is read-only and is always read as "one."

5.0 I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. MOVF 6,W) always read the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB, TRISC) are all set to "ones."

The execution of a "TRIS f" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

5.1 f5 (Port A)

4-bit I/O register. Low order 4 bits only are used (RA0 - RA3). Bit 4 - 7 are unimplemented and read as "zeros."

5.2 f6 (Port B)

8-bit I/O register.

5.3 f7 (Port C)

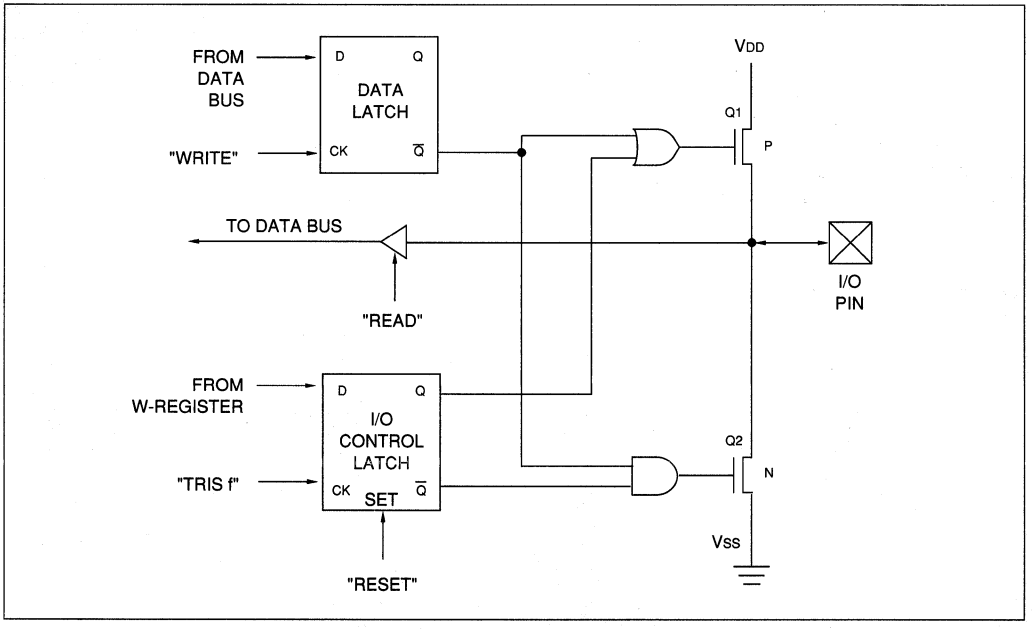
PIC16C55/C57: 8-bit I/O register.

PIC16C54/C56: General purpose register.

5.4 I/O INTERFACING

The equivalent circuit for an I/O port bit is shown in Figure 5.4.1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g. MOVF 6, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be set to zero. For use as an input, the corresponding TRIS bit must be "one". Any I/O pin can be programmed individually as input or output.

FIGURE 5.4.1 - EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



5.5 I/O PROGRAMMING CONSIDERATIONS

5.5.1 BIDIRECTIONAL I/O PORTS

a) Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of f6 (Port B) will cause all eight bits of f6 to be read into the CPU. Then the BSF operation takes place on bit 5 and f6 is re-output to the output latches. If another bit of f6 is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

b) A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.
For "wired-or" outputs (assuming negative logic), it is recommended to use external pull-up resistors on the corresponding pins. The pin should be left in high-impedance mode, unless a "0" has to be output. Thus, external devices can drive this pin "0" as well. "Wired-and" outputs can be realized in the same way, but with external pull-down resistors and only actively driving the "1" level from the PIC. The resistor values are user selectable, but should not force output currents above the specified limits (see DC Characteristics).

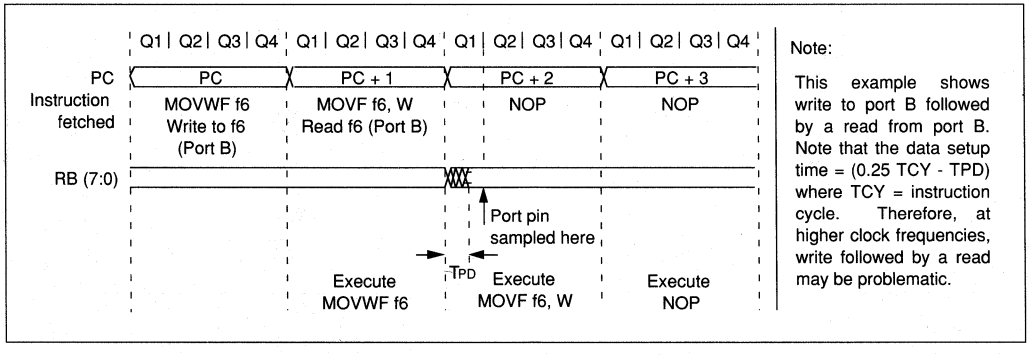
5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see figure 5.4.2.1). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

5.5.3 OPERATION IN NOISY ENVIRONMENT

In noisy application environments, such as keyboards which are exposed to ESD (Electro Static Discharge), register contents can get corrupted due to noise spikes. The on-chip watchdog timer will take care of all situations involving program sequence "lock-ups." However, if an I/O control register gets corrupted, the program sequence may still be executed properly although an input pin may have switched unintentionally to an output. In this case, the program would always read the same value on this pin. This may result, for example, in a keyboard "lock-up" situation without leading to a watchdog timer timeout. Thus, it is recommended to redefine all I/O pins in regular time intervals (inputs as well as outputs). The optimal strategy is to update the I/O control register every time before reading input data or writing output data .

FIGURE 5.5.2.1 - I/O PORT READ/WRITE TIMING



Note:

This example shows write to port B followed by a read from port B. Note that the data setup time = (0.25 TCY - TPD) where TCY = instruction cycle. Therefore, at higher clock frequencies, write followed by a read may be problematic.

6.0 GENERAL PURPOSE REGISTERS

PIC16C54/C55/C56:

f08h - f1Fh: are general purpose register files.

PIC16C57 only:

f08h - f0Fh: are general purpose register files which are always selected, independent of bank select.
f10h - f1Fh: general purpose register files in memory bank 0.
f20h - f2Fh: physically identical to f00 - f0F.
f30h - f3Fh: general purpose register files in memory bank 1.
f40h - f4Fh: physically identical to f00 - f0F.
f50h - f5Fh: general purpose register files in memory bank 2.
f60h - f6Fh: physically identical to f00 - f0.
f70h - f7Fh: general purpose register files in memory bank 3.

7.0 SPECIAL PURPOSE REGISTERS

7.1 W Working Register

Holds second operand in two operand instructions and/or supports the internal data transfer.

7.2 TRISA I/O Control Register For Port A (f5)

Only bits 0 - 3 are available. The corresponding I/O port (f5) is only 4-bit wide.

7.3 TRISB I/O Control Register For Port B (f6)

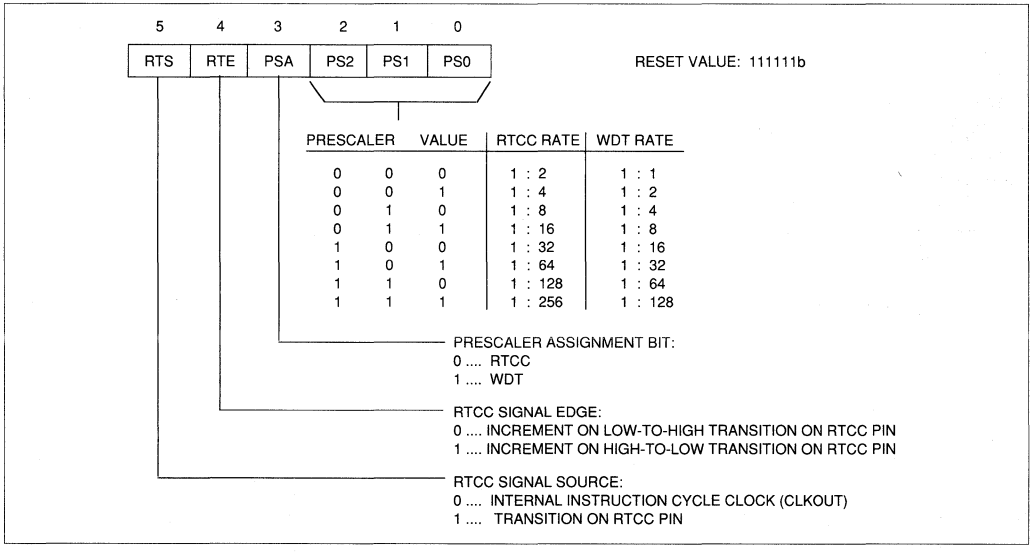
7.4 TRISC I/O Control Register For Port C (f7)

The I/O control registers will be loaded with the content of the W register by executing of the TRIS f instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of file register f5, f6, or f7 , respectively, out on the selected I/O pins.
These registers are "write-only" and are set to all "ones" upon a RESET condition.

7.5 OPTION Prescaler/RTCC Option Register

Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6 bit wide. By executing the "OPTION" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register is set to all "ones."

FIGURE 7.5.1 - OPTION REGISTER



8.0 RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the $\overline{MCLR}$ input "low", or by a Watchdog timer timeout. The device will stay in RESET as long as the oscillator start-up timer (OST) is active or the $\overline{MCLR}$ input is "low."
The oscillator start-up timer is activated as soon as $\overline{MCLR}$ input is sensed to be high. This implies that in case of power on reset with $\overline{MCLR}$ tied to V_{DD} the OST starts from power-up. In case of WDT time-out, it will start at the end of the time-out (since $\overline{MCLR}$ is high). In case of $\overline{MCLR}$ reset, the OST will start when $\overline{MCLR}$ goes high. The nominal OST time-out period is 18 ms. See section 13.0 for detailed information on OST and power on reset.

During a RESET condition the state of the PIC is defined as :

- The oscillator is running, or will be started (power-up or wake-up from SLEEP).
- All I/O port pins (RA0 - RA3, RB0 - RB7, RC0 - RC7) are put into the high-impedance state by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones" (1FFh in PIC16C54/55, 3FFh in PIC16C56 and 7FFh in PIC16C57).
- The OPTION register is set to all "ones".
- The Watchdog Timer and its prescaler are cleared.
- The upper three bits (page select bits) in the Status Register (f3) are cleared to "zero."
- "RC" devices only: The "CLKOUT" signal on the OSC2 pin is held at a"low" level.

9.0 PRESCALER

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the watchdog timer, respectively (Figure 9.0.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the watchdog timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the watchdog timer, and vice versa.
The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio.

When assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF 1, MOVWF 1, BSF 1,x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the watchdog timer.

9.1 Switching Prescaler Assignment

CHANGING PRESCALER FROM RTCC TO WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'  ; Select internal clock and select new
2. OPTION              ; prescaler value. If new prescale value
                       ; is = '000' or '001', then select any other
                       ; prescale value temporarily.
3. CLRF 1              ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'  ; Select WDT, do not change prescale
                       ; value.
5. OPTION              ;
6. CLRWDT              ; Clears WDT and prescaler.
7. MOVLW B'xxxx1xxx'   ; Select new prescale value.
8. OPTION              ;
```

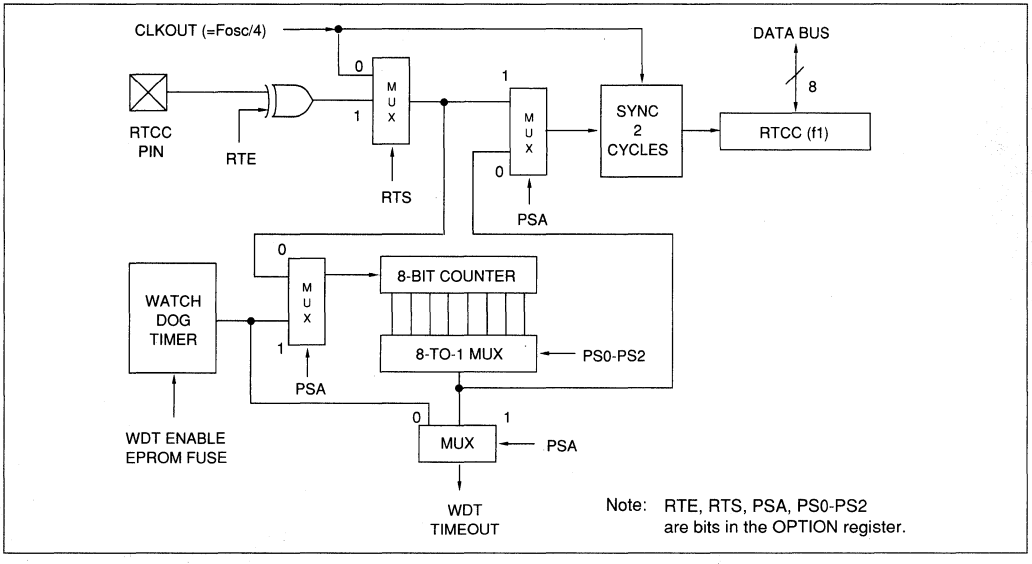
Step 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT              ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'  ; Select RTCC, new prescale value
                       ; and clock source
3. OPTION              ;
```

FIGURE 9.0.1 - BLOCK DIAGRAM RTCC/WDT PRESCALER



10.0 BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP CODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC instruction set summary in Table 10.0.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. For the PIC16C57, bit 5 and 6 in the FSR determine the selected register bank.
The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.
For literal and control operations, "k" represents an eight or nine bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 10.0.1

Note 1: The 9th bit of the program counter will be forced to a "zero" by any instruction that writes to the PC (f2) except for GOTO (e.g. CALL, MOVWF 2 etc.). See section 4.3 on page 8 for details.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF 6,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as output and is driven low by an external device, the data will be written back with a '0'.

Note 3: The instruction "TRIS f" , where f = 5,6, or 7 causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on file register f1 (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 10.0.1 - INSTRUCTION SET SUMMARY

BYTE -ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

d = 0 for destination W
d = 1 for destination f

Instruction-Binary	(Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0001 11df ffff	1Cf	Add W and f	**ADDWF**	**f, d**	W + f → d	C,DC,Z	1,2,4
0001 01df ffff	14f	AND W and f	**ANDWF**	**f, d**	W & f → d	Z	2,4
0000 011f ffff	06f	Clear f	**CLRF**	**f**	0 → f	Z	4
0000 0100 0000	040	Clear W	**CLRW**	**-**	0 → W	Z	
0010 01df ffff	24f	Complement f	**COMF**	**f, d**	$\bar{f}$ → d	Z	2,4
0000 11df ffff	0Cf	Decrement f	**DECF**	**f, d**	f -1 → d	Z	2,4
0010 11df ffff	2Cf	Decrement f,Skip if Zero	**DECFSZ**	**f, d**	f - 1 → d, skip if zero	None	2,4
0010 10df ffff	28f	Increment f	**INCF**	**f, d**	f + 1 → d	Z	2,4
0011 11df ffff	3Cf	Increment f,Skip if zero	**INCFSZ**	**f, d**	f + 1 → d, skip if zero	None	2,4
0001 00df ffff	10f	Inclusive OR W and f	**IORWF**	**f, d**	W v f → d	Z	2,4
0010 00df ffff	20f	Move f	**MOVF**	**f, d**	f → d	Z	2,4
0000 001f ffff	02f	Move W to f	**MOVWF**	**f**	W → f	None	1,4
0000 0000 0000	000	No Operation	**NOP**	**-**	-	None	
0011 01df ffff	34f	Rotate left f	**RLF**	**f, d**	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 00df ffff	30f	Rotate right f	**RRF**	**f, d**	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0000 10df ffff	08f	Subtract W from f	**SUBWF**	**f, d**	f - W → d [f + $\overline{W}$ + 1 → d]	C,DC,Z	1,2,4
0011 10df ffff	38f	Swap halves f	**SWAPF**	**f, d**	f(0-3) ↔ f(4-7) → d	None	2,4
0001 10df ffff	18f	Exclusive OR W and f	**XORWF**	**f, d**	W ⊕ f → d	Z	2,4

BIT- ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary	(Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0100 bbbf ffff	4bf	Bit Clear f	**BCF**	**f, b**	0 → f(b)	None	2,4
0101 bbbf ffff	5bf	Bit Set f	**BSF**	**f, b**	1 → f(b)	None	2,4
0110 bbbf ffff	6bf	Bit Test f,Skip if Clear	**BTFSC**	**f, b**	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff	7bf	Bit Test f, Skip if Set	**BTFSS**	**f, b**	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary	(Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
1110 kkkk kkkk	Ekk	AND Literal and W	**ANDLW**	**k**	k & W→ W	Z	
1001 kkkk kkkk	9kk	Call subroutine	**CALL**	**k**	PC + 1 → Stack, k → PC	None	1
0000 0000 0100	004	Clear Watchdog timer	**CLRWDT**	**-**	0 → WDT (and prescaler, if assigned)	TO, PD	
101k kkkk kkkk	Akk	Go To address (k is 9 bit)	**GOTO**	**k**	k → PC (9 bits)	None	
1101 kkkk kkkk	Dkk	Incl. OR Literal and W	**IORLW**	**k**	k v W → W	Z	
1100 kkkk kkkk	Ckk	Move Literal to W	**MOVLW**	**k**	k → W	None	
0000 0000 0010	002	Load OPTION register	**OPTION**	**-**	W → OPTION register	None	
1000 kkkk kkkk	8kk	Return,place Literal in W	**RETLW**	**k**	k → W, Stack → PC	None	
0000 0000 0011	003	Go into standby mode	**SLEEP**	**-**	0 → WDT, stop oscillator	TO, PD	
0000 0000 0fff	00f	Tristate port f	**TRIS**	**f**	W→ I/O control register f	None	3
1111 kkkk kkkk	Fkk	Excl. OR Literal and W	**XORLW**	**k**	k ⊕ W → W	Z	

Notes: See previous page

10.1 INSTRUCTION DESCRIPTION

ADDWF ADD W to f

Syntax: ADDWF f,d

Encoding:	0001	11df	ffff

Words: 1

Cycles: 1

Operation: (W + f) → d

Status bits: C, DC, Z

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

ANDLW AND Literal and W

Syntax: ANDLW k

Encoding:	1110	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .AND. k) → W

Status bits: Z

Description: The contents of W register are AND'ed with the eight bit literal "k". The result is placed in the W register.

ANDWF AND W with f

Syntax: ANDWF f,d

Encoding:	0001	01df	ffff

Words: 1

Cycles: 1

Operation: (W .AND. f) → d

Status bits: Z

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

BCF Bit Clear f

Syntax: BCF f,b

Encoding:	0100	bbbf	ffff

Words: 1

Cycles: 1

Operation: 0 → f(b)

Status bits: None

Description: Bit "b" in register "f" is reset to 0.

BSF Bit Set f

Syntax: BSF f,b

Encoding:	0101	bbbf	ffff

Words: 1

Cycles: 1

Operation: 1 → f(b)

Status bits: None

Description: Bit "b" in register "f" is set to 1.

BTFSC Bit Test, skip if Clear

Syntax: BTFSC f,b

Encoding:	0110	bbbf	ffff

Words: 1

Cycles: 1(2)

Operation: skip if f(b) = 0

Status bits: None

Description: If bit "b" in register "f" is "0" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

BTFSS Bit Test, skip if Set

Syntax: BTFSS f,b

Encoding:	0111	bbbf	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f(b) = 1

Status bits: None

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit "b" is "1", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

CALL Subroutine Call

Syntax: CALL k

Encoding:	1001	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC + 1 → TOS; k → PC<7:0>, '0' → PC<8>, PA2, PA1, PA0 → PC<11:9>;

Status bits: None

Description: Subroutine call. First, return address (PC + 1) is pushed into the stack. The eight bit value is loaded into PC bits <7:0>. PC bit 9 is cleared. PC <2:0> bits are loaded into PC <11:9>. CALL is a two cycle instruction.

CLRF Clear f and Clear d

Syntax: CLRF f,d

Encoding:	0000	011f	ffff

Words: 1

Cycles: 1

Operation: 00h → f, 00h → d

Status bits: None

Description: The contents of register "f" are set to 0. If "d" is 0 the contents of both data memory location "f" and W register are set to 0. If "d" is 1 the only contents of register "f" are set to 0.

CLRW Clear W Register

Syntax: CLRW

Encoding:	0000	0100	0000

Words: 1

Cycles: 1

Operation: 00h →W

Status bits: Z

Description: W registered is cleared. Zero bit (Z) is set.

CLRWDT Clear Watchdog Timer

Syntax: CLRWDT

Encoding:	0000	0000	0100

Words: 1

Cycles: 1

Operation: 00h →WDT, 0 → WDT prescaler,

Status bits: 1 → TO, 1 → PD

Description: CLRWDT instruction resets the watchdog timer.It also resets the prescaler of the WDT. Status bits TO and PD are set.

COMF Complement f

Syntax: COMF f,d

Encoding:	0010	01df	ffff

Words: 1

Cycles: 1

Operation: $\bar{f}$ → d

Status bits: Z

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

DECF Decrement f

Syntax: DECF f,d

Encoding:	0000	11df	ffff

Words: 1

Cycles: 1

Operation: (f-1) → d

Status bits: C, DC, Z

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

DECFSZ Decrement f, skip if 0

Syntax: DECFSZ f,d

Encoding:	0010	11df	ffff

Words: 1

Cycles: 1 (2)

Operation: (f - 1) → d; skip if result = 0

Status bits: None

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f". If the result is 0 the next instruction is skipped.

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

GOTO Unconditional Branch

Syntax: GOTO k

Encoding:	101k	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → PC<8:0>, PA2, PA1, PA0

→ PC<11:9>;

Status bits: None

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH <4:3>. GOTO is a two cycle instruction.

INCF Increment f

Syntax: INCF f,d

Encoding:	0010	10df	ffff

Words: 1

Cycles: 1

Operation: (f + 1) → d

Status bits: C, DC, Z

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

INCFSZ Increment f, skip if 0

Syntax: INCFSZ f,d

Encoding:

0011	11df	ffff

Words: 1

Cycles: 1 (2)

Operation: (f + 1) → d, skip if result = 0

Status bits: None

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f". If the result is 0 the next instruction is skipped.

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

IORLW Inclusive OR Literal with W

Syntax: IORLW k

Encoding:

1101	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .OR. k) → W

Status bits: Z

Description: The contents of the W register are OR'ed with the eight bit literal "k". The result is placed in the W register.

IORWF Inclusive OR W with f

Syntax: IORWF f,d

Encoding:

0001	00df	ffff

Words: 1

Cycles: 1

Operation: (W .OR. f) → d

Status bits: Z

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

MOVF Move f

Syntax: MOVF f,d

Encoding:

0010	00df	ffff

Words: 1

Cycles: 1

Operation: (f) → d

Status bits: Z

Description: The contents of register "f" are moved. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

MOVLW Move Literal to W

Syntax: MOVLW k

Encoding:

1100	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → W

Status bits: None

Description: The eight bit literal "k" is loaded into W register.

MOVWF Move W to f

Syntax: MOVWF f

Encoding:

0000	001f	ffff

Words: 1

Cycles: 1

Operation: W → f

Status bits: None

Description: Move data from W register to register "f".

NOP No Operation

Syntax: NOP

Encoding:

0000	0000	0000

Words: 1

Cycles: 1

Operation: No operation

Status bits: None

Description: No operation

OPTION Load Option Register

Syntax: OPTION

Encoding:

0000	0000	0010

Words: 1

Cycles: 1

Operation: W → OPTION;

Status bits: None

Description: The contents of the W register is loaded in the OPTION register.

RETLW Return Literal to W

Syntax: RETLW k

Encoding:	1000	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → W; TOS → PC;

Status bits: None

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

RLF Rotate Left f through Carry

Syntax: RLF f,d

Encoding:	0011	01df	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".

RRF Rotate Right f through Carry

Syntax: RRF f,d

Encoding:	0011	00df	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>, f<0> → C, C → d<7>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

SLEEP

Syntax: SLEEP

Encoding:	0000	0000	0011

Words: 1

Cycles: 1

Operation: 0 → PD, 1 → TO;
00h → WDT, 0 → WDT prescaler;

Status bits: TO, PD

Description: The power down status bit (PD) is cleared. Time-out status bit (TO) is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

SUBWF Subtract W from f

Syntax: SUBWF f,d

Encoding:	0000	10df	ffff

Words: 1

Cycles: 1

Operation: (f-W) → d

Status bits: C, DC, Z

```
;SUBWF Example #1
;
clrf   0x20    ;f(20h)=0
movlw  1       ;wreg=1
subwf  0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
               ;Carry=0; Result is negative
;
;SUBWF Example #2
;
movlw  0xFF    ;
movwf  0x20    ;f(20h)=FFh
clrw           ;wreg=0
subwf  0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
               ;Carry=1:Result is positive
;
```

Description: Subtract (2's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

SWAPF Swap f

Syntax: SWAPF f,d

Encoding:	0011	10df	ffff

Words: 1

Cycles: 1

Operation: f<0:3> → d<4:7>, f<4:7> → d<0:3>;

Status bits: None

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

TRIS Load TRIS Register

Syntax: TRIS f

Encoding:	0000	0000	0fff

Words: 1

Cycles: 1

Operation: W → TRIS register f;

Status bits: None

Description: TRIS register f (f = 5, 6 or 7) is loaded with the contents of the W register.

XORLW Exclusive OR literal with W

Syntax: XORLW k

Encoding:

1111	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .XOR. k) → W

Status bits: Z

Description: The contents of the W register are XOR'ed with the eight bit literal "k". The result is placed in the W register.

XORWF Exclusive OR W with f

Syntax: XORWF f,d

Encoding:

0001	10df	ffff

Words: 1

Cycles: 1

Operation: (W .XOR. f) → d

Status bits: Z

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

11.0 WATCHDOG TIMER (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming a "zero" into a special EPROM fuse which is not part of the normal program memory EPROM. The PIC development tools "PICMASTER™, PIC-PAK™", and "PICPRO™" provide special commands to program this fuse.

11.1 WDT Period

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit "TO" in file register f3 will be cleared upon a watchdog timer timeout.

The WDT period is a function of the supply voltage, operating temperature, and will also vary from unit to unit due to variations in the manufacturing process. Please refer to the graphs in section 18.0 and DC specs for more details.

11.2 WDT Programming Considerations

In a noisy application environment the OPTION register can get corrupted. The OPTION register should be updated at regular intervals.

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

12.0 OSCILLATOR CIRCUITS

12.1 Oscillator Types

The PIC16C5X series is available with 4 different oscillator options. On windowed devices, a particular oscillator circuit can be selected by programming the configuration EPROM accordingly. The PIC development tools (e.g. PICMASTER, PIC-PAK, PICPRO) provide special commands to select the desired oscillator configuration. On OTP and QTP devices, the oscillator configuration is programmed by the factory and the parts are tested only to the according specifications.

12.2 Crystal Oscillator

The PIC16C5X-XT, -HS, or LP needs a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Figure 12.2.1). XT = Standard crystal oscillator, HS = High speed crystal oscillator. The series resistor Rs may be required for the "HS" oscillator, especially at lower than 20 MHz oscillation frequency. It may also be required in XT mode with AT strip-cut type crystals to avoid overdriving.

12.3 RC Oscillator

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation to due tolerance of external R and C components used. Figure 12.3.1 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 kOhm, the

oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 5 kOhm and 100 kOhm.

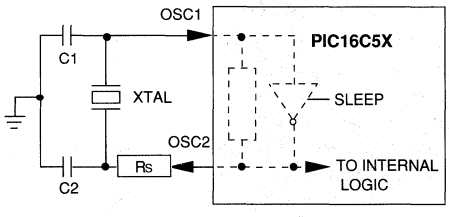
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See table in section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characteristics in section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 2.2.1 for timing).

FIGURE 12.2.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP TYPES ONLY)



Rs may be required in HS and XT modes for AT strip-cut crystals to avoid overdriving. See Tables 12.2.1 and 12.2.2 for recommended values of C1, C2 per oscillator type and frequency.

TABLE 12.2.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

FIGURE 12.2.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP TYPES ONLY)

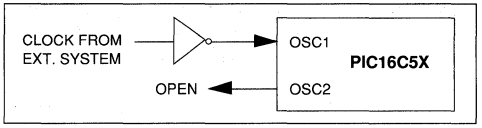


TABLE 12.2.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 12.3.1 - RC OSCILLATOR (RC TYPE ONLY)

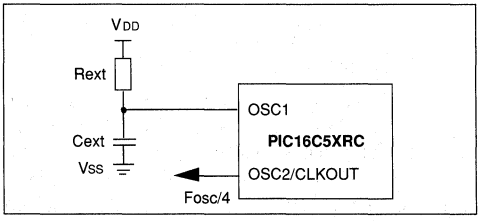
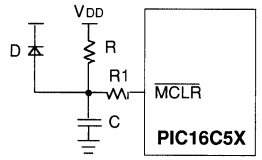


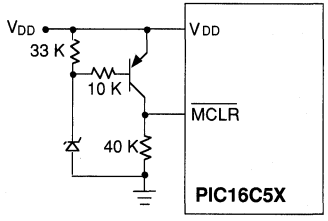
FIGURE 13.1.1 - EXTERNAL POWER ON RESET CIRCUIT



Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow or if a low frequency crystal oscillator is being used that need a long start-up time. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ must be observed to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on MCLR pin is 5 μA). A larger voltage drop will degrade VIH level on MCLR pin.
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

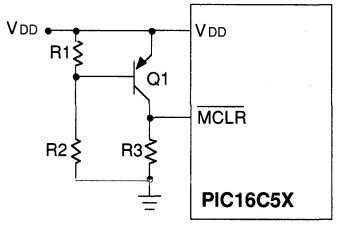
FIGURE 13.1.2 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 13.1.3 - BROWN OUT PROTECTION CIRCUIT



Notes:

1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$VDD \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

13.0 OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip oscillator start-up timer is provided which keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The OST will also be triggered upon a watchdog timer timeout. This is particularly important for applications using the WDT to awake the PIC16C5X from SLEEP mode automatically.

The OST is not adequate for low frequency crystals which require much longer than 18 ms to start up and stabilize.

13.1 Power On Reset (POR)

The PIC16C5X incorporates an on chip Power On Reset (POR) circuitry which provides internal chip reset for most power-up situations. To use this feature the user merely needs to tie MCLR pin to VDD. A simplified block diagram of the on-chip power on reset circuit is shown in Figure 13.1.4. The power on reset circuit and the oscillator start-up timer circuit are closely related. On power-up the reset latch is set and the start-up timer (see Figure 13.1.4) is reset. The start-up timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will reset the reset-latch and thus end the on-chip reset signal.

Figures 13.1.5 and 13.1.6 are two power-up situations with relatively fast rise time on VDD. In Figure 13.1.5, VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TOST ms after MCLR goes high. In Figure 13.1.6, the on chip power-on reset feature is being utilized (MCLR and VDD are tied together). The VDD is stable before the startup timer times out and there is no problem in getting a proper reset. Figure 13.1.7 depicts a potentially problematic situation where VDD rises too slowly. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is therefore not guaranteed to function correctly.

To summarize, the on chip power-on reset is guaranteed to work if the rate of rise of VDD is no slower than 0.05 V/ms. It is also necessary that the VDD starts from 0V. The on chip power on reset is also not adequate for low frequency crystals which require much longer than 18 ms to start up and stabilize. For such situations, we recommend that external RC circuits are used for longer power on reset.

FIGURE 13.1.4 - SIMPLIFIED POWER ON RESET BLOCK DIAGRAM

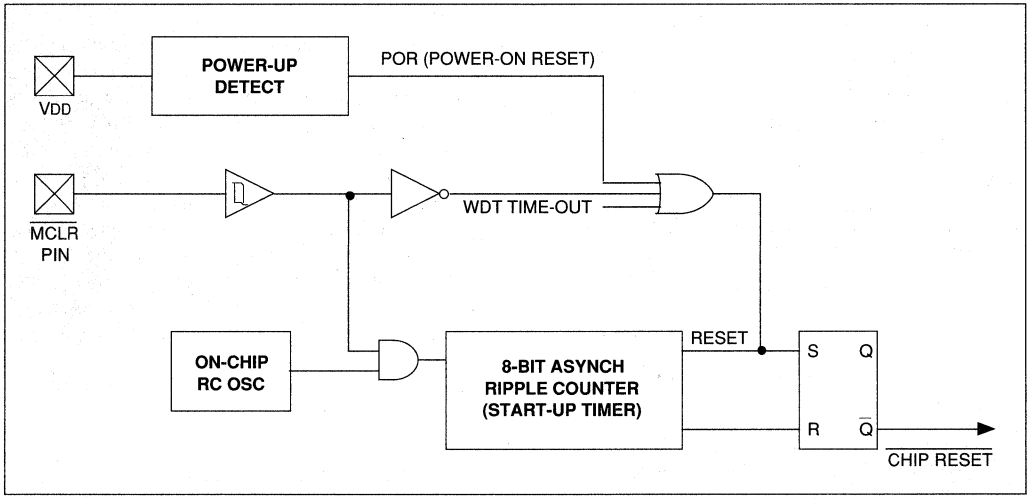
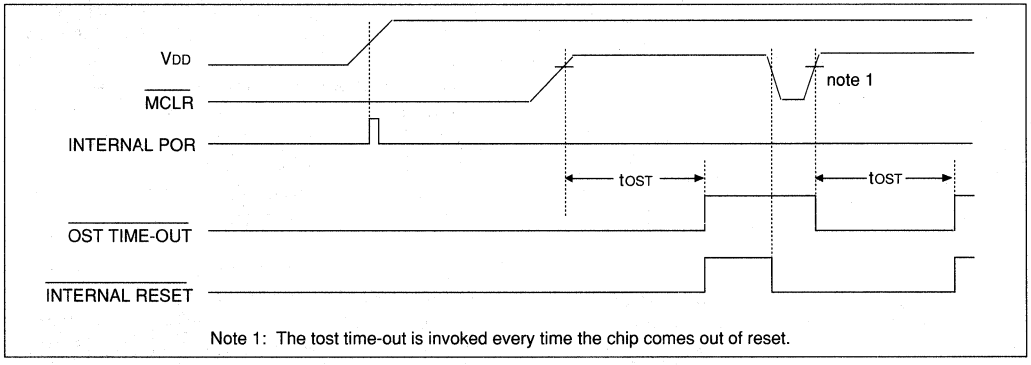


FIGURE 13.1.5 - USING EXTERNAL RESET INPUT



Note 1: The tost time-out is invoked every time the chip comes out of reset.

FIGURE 13.1.6 - USING ON-CHIP POR (FAST VDD RISE TIME)

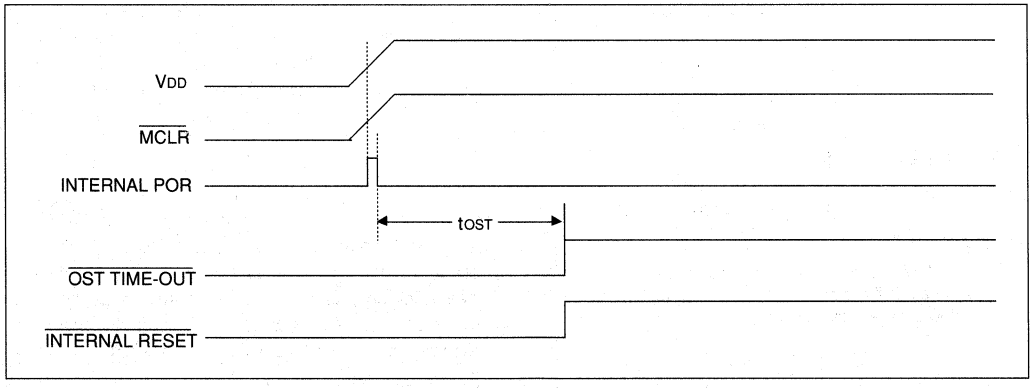
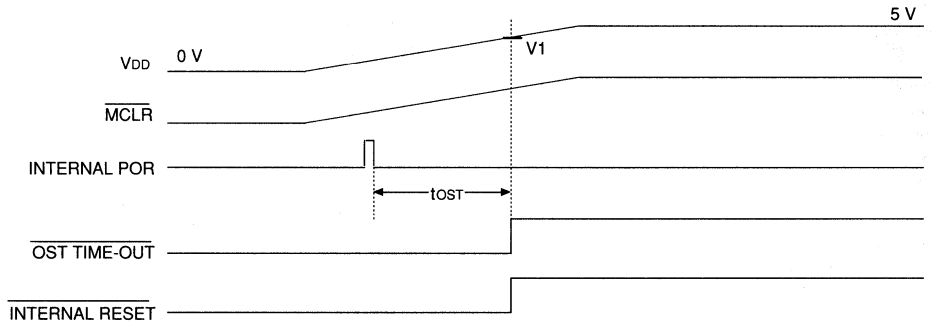


FIGURE 13.1.7 - USING ON-CHIP POR (SLOW VDD RISE TIME)



When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1≥ VDDMIN.

14.0 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the watchdog timer will be cleared but keeps running, the bit "PD" in the status register (f3) is cleared, the "TO" bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or VSS for lowest current consumption.

The MCLR pin must be at VIHMC.

14.1 Wake-Up

The device can be awakened by a watchdog timer timeout (if it is enabled) or an externally applied "low" pulse at the MCLR pin. In both cases the PIC will stay in RESET mode for one oscillator start-up timer period (triggered from rising edge on MCLR or WDT timeout) before normal program execution resumes.

The "PD" bit in the STATUS register, which is set to one during power on, but cleared by the "SLEEP" command, can be used to determine if the processor was powered up or awakened from the power down mode (Table 4.5.1.2). The TO bit in the Status register can be used to determine, if the "wake up" was caused by an external MCLR signal or a watchdog timer time out.

NOTE: Some applications may require external R/C networks on the MCLR pin in order to allow for oscillator startup times longer than one OST period. In this case, a WDT wake up from power down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the PIC will be in RESET only for the oscillator start-up timer period.

15.0 CONFIGURATION FUSES

The configuration EPROM consists of four EPROM fuses which are not part of the normal EPROM for program storage.

Two are for the selection of the oscillator type, one is the watchdog timer enable fuse, and one is the code protection fuse.

The PIC development tools (PICMASTER™, PICPAK-II™, PICPRO™, PICPRO II and PROMASTER) allow the setting of these with special commands.

OTP or QTP devices have the oscillator configuration programmed by the factory and the parts are tested accordingly. The packages are marked with the suffixes "XT", "RC", "HS" or "LP" following the part number to identify the oscillator type and operating range.

15.1 Customer ID Code

The PIC16C5X series has 16 special EPROM bits which are not part of the normal program memory. These bits are available to the user to store an Identifier (ID) code, checksum, or other informative data. They cannot be accessed during normal program execution. The PIC16C5X programmers (e.g. PICPRO or PICPRO II) provide special commands to read or write these ID bits.

15.2 Code Protection

The program code written into the EPROM can be protected by programming the code protection fuse with "0".
When code protected, the contents of the program EPROM cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 040h and above are protected against programming.
It is still possible to program locations 000h - 03Fh, the ID locations and the configuration fuses.
Note that the configuration fuses and the ID bits can still be read, even if the code protection logic is active.

15.2.1 VERIFYING A CODE-PROTECTED PIC

When code protected verifying any program memory location will read a scrambled output which looks like "00000000XXXX" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.
b. Next, blow its code protection fuse and then load its contents in a file.
c. Verify any code-protected PIC against this file.

16.0 ELECTRICAL CHARACTERISTICS

16.1 Absolute Maximum Ratings*

Ambient temperature under bias .....-55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to Vss
(except VDD and MCLR) .....-0.6V to VDD +0.6V
Voltage on VDD with respect to Vss .....0 to +9.5 V
Voltage on MCLR with respect to Vss
(Note 2) .....0 to +14 V
Total power Dissipation (Note 1) .....800 mW
Max. Current out of Vss pin .....150 mA
Max. Current into VDD pin .....50 mA
Max. Current into an input pin .....±500 µA
Max. Output Current sinked by any I/O pin.....25 mA
Max. Output Current sourced by any I/O pin .....20 mA
Max. Output Current sourced by a single
I/O port (Port A, B, or C) .....40 mA
Max. Output Current sinked by a single
I/O port (Port A, B, or C) 50mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = VDD \times \{IDD - \Sigma Ioh\} + \Sigma\{(VDD-Voh) \times Ioh\} + \Sigma(Vol \times Iol)$

2. Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the MCLR pin rather than pulling this pin directly to Vss.

TABLE 16.2 - PIN DESCRIPTIONS

Name	Function	Observation
RA0 - RA3	I/O PORT A	4 input/output lines.
RB0 - RB7	I/O PORT B	8 input/output lines.
RC0 - RC7	I/O PORT C	8 input/output lines, (PIC16C55/C57 only).
RTCC	Real Time Clock/Counter	Schmitt Trigger Input. Clock input to RTCC register. Must be tied to Vss or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption.
MCLR	Master Clear	Schmitt Trigger Input. A "Low" voltage on this input generates a RESET condition for the PIC16C5X microcontroller. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1	Oscillator (input)	"XT", "HS" and "LP" devices: Input terminal for crystal, ceramic resonator, or external clock generator. "RC" devices : Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	For "XT", "HS" and "LP" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
VDD	Power supply	
Vss	Ground	
N/C	No (internal) Connection	

16.3 DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (COMMERCIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature 0 ≤ TA ≤ +70°C, unless otherwise stated Operating voltage VDD = 3.0V to 5.5V unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
PIC16C5X-XT	VDDxt	3.0		6.25	V	Fosc = DC to 4 MHz
PIC16C5X-RC	VDDrc	3.0		6.25	V	Fosc = DC to 4 MHz
PIC16C5X-HS	VDDhs	4.5		5.5	V	Fosc = DC to 20 MHz
PIC16C5X-LP	VDDlp	2.5		6.25	V	Fosc = DC to 40 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on
Supply Current (Note 2)						
PIC16C5X-XT	IDDxt		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16C5X-RC (Note 5)	IDDrc		1.8	3.3	mA	Fosc = 4 MHz , VDD = 5.5V
PIC16C5X-HS	IDDhs1		4.8	10	mA	Fosc =10 MHz, VDD = 5.5V
	IDDhs2		9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V
PIC16C5X-LP	IDDlp		15	32	µA	Fosc = 32 KHz, VDD=3.0V, WDT disabled
Power Down Current (Note 4)						
PIC16C5X	IPD1		4	12	µA	VDD = 3.0V, WDT enabled
	IPD2		0.6	9	µA	VDD = 3.0V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.4 DC CHARACTERISTICS: PIC16C5XI-RC, XT, HS, LP (INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature -40 ≤ TA ≤ +85°C, unless otherwise stated Operating voltage VDD = 3.5V to 5.5V unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
PIC16C5X-XT	VDDxt	3.0		6.25	V	Fosc = DC to 4 MHz
PIC16C5X-RC	VDDrc	3.0		6.25	V	Fosc = DC to 4 MHz
PIC16C5X-HS	VDDhs	4.5		5.5	V	Fosc = DC to 20 MHz
PIC16C5X-LP	VDDlp	2.5		6.25	V	Fosc = DC to 40 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on reset
Supply Current (Note 2)						
PIC16C5X-XT	IDDxt		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16C5X-RC (Note 5)	IDDrc		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16C5X-HS	IDDhs1		4.8	10.0	mA	Fosc = 10 MHz, VDD = 5.5V
	IDDhs2		9.0	20.0	mA	Fosc = 20 MHz, VDD = 5.5V
PIC16C5X-LP	IDDlp		19	40	µA	Fosc = 32 KHz, VDD = 3.0V, WDT disabled
Power Down Current (Note 4)						
PIC16C5X	IPD1		5	14	µA	VDD = 3.0V, WDT enabled
	IPD2		0.8	12	µA	VDD = 3.0V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are:
OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.5 DC CHARACTERISTICS: PIC16C5XI-RC, XT, HS, LP (AUTOMOTIVE)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions Operating temperature -40 ≤ TA ≤ +125°C, unless otherwise stated Operating voltage VDD = 3.5V to 5.5V unless otherwise stated					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
PIC16C5X-XT	VDDxt	3.25		6.0	V	Fosc = DC to 4 MHz
PIC16C5X-RC	VDDrc	3.25		6.0	V	Fosc = DC to 4 MHz
PIC16C5X-HS	VDDhs	4.5		5.5	V	Fosc = DC to 16 MHz
PIC16C5X-LP	VDDlp	2.5		6.0	V	Fosc = DC to 40 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power on reset
Supply Current (Note 2)						
PIC16C5X-XT	IDDxt		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16C5X-RC (Note 5)	IDDrc		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V
PIC16C5X-HS	IDDhs1		4.8	10.0	mA	Fosc = 10 MHz, VDD = 5.5V
	IDDhs2		9.0	20.0	mA	Fosc = 16 MHz, VDD = 5.5V
PIC16C5X-LP	IDDlp		25	55	µA	Fosc = 32 KHz, VDD = 3.25V, WDT disabled
Power Down Current (Note 4)						
PIC16C5X	IPD1		5	22	µA	VDD = 3.25V, WDT enabled
	IPD2		0.8	18	µA	VDD = 3.25V, WDT disabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are:
OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: Does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.6 DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (COMMERCIAL) PIC16C5XI-RC, XT, HS, LP (INDUSTRIAL)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40 < TA < +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec tables 16.3 and 16.4

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt trigger)	VILMC	VSS		0.15 VDD	V	
RTCC (Schmitt trigger)	VILRT	VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)	VILOSC	VSS		0.15 VDD	V	PIC16C5XRC only (Note 5)
OSC1	VILOSC	VSS		0.3 VDD	V	PIC16C5X-XT, HS, LP
Input High Voltage						
I/O ports	VIH	0.45 VDD		VDD	V	For all VDD (Note 6)
	VIH	2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
	VIH	0.36 VDD		VDD	V	VDD > 5.5 V
$\overline{MCLR}$ (Schmitt trigger)	VIHMC	0.85 VDD		VDD	V	
RTCC (Schmitt trigger)	VIHRT	0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)	VIHOSC	0.85 VDD		VDD	V	PIC16C5X-RC only (Note 5)
OSC1	VIHOSC	0.7 VDD		VDD	V	PIC16C5X-XT, HS, LP
Input Leakage Current (Notes 3, 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$	IILMCL	-5			µA	VPIN = VSS + 0.25V
$\overline{MCLR}$	IILMCH		0.5	+5	µA	VPIN = VDD
RTCC	IILRT	-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1	IILOSC1	-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD , PIC16C5X-XT, HS, LP
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16C5X-RC)	VOL			0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16C5X-RC)	VOH	VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : For PIC16C5XRC devices, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

16.7 DC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (AUTOMOTIVE)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY		Standard Operating Conditions (unless otherwise stated) Operating temperature -40 < TA < +125°C Operating voltage VDD range as described in DC spec tables 16.3 and 16.4				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL	VSS		0.15 VDD	V	Pin at hi-impedance
MCLR (Schmitt trigger)	VILMC	VSS		0.15 VDD	V	
RTCC (Schmitt trigger)	VILRT	VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)	VILOSC	VSS		0.15 VDD	V	PIC16C5XRC only (Note 5)
OSC1	VILOSC	VSS		0.3 VDD	V	PIC16C5X-XT, HS, LP
Input High Voltage						
I/O ports	VIH	0.45 VDD		VDD	V	For all VDD (Note 6)
	VIH	2.0		VDD	V	4.0 V < VDD ≤ 5.5 V (Note 6)
	VIH	0.36 VDD		VDD	V	VDD > 5.5 V
MCLR (Schmitt trigger)	VIHMC	0.85 VDD		VDD	V	
RTCC (Schmitt trigger)	VIHRT	0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)	VIHOSC	0.85 VDD		VDD	V	PIC16C5X-RC only (Note 5)
OSC1	VIHOSC	0.7 VDD		VDD	V	PIC16C5X-XT, HS, LP
Input Leakage Current (Notes 3, 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR	IILMCL	-5			µA	VPIN = VSS + 0.25V
MCLR	IILMCH		0.5	+5	µA	VPIN = VDD
RTCC	IILRT	-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1	IILOSC1	-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD , PIC16C5X-XT, HS, LP
Output Low Voltage						
I/O Ports	VOL			0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16C5X-RC)	VOL			0.6	V	IOL = 1.6 mA, VDD = 4.5V
Output High Voltage						
I/O Ports (Note 4)	VOH	VDD-0.7			V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT (PIC16C5X-RC)	VOH	VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : For PIC16C5XRC devices, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

Note 6: The user may use better of the two specifications.

16.8 AC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (COMMERCIAL) PIC16C5XI-RC, XT, HS, LP (INDUSTRIAL) PIC16C5XI-RC, XT, HS, LP (AUTOMOTIVE)

AC CHARACTERISTICS	**Standard Operating Conditions (unless otherwise stated)** Operating temperature TA = -40°C to +85°C (industrial), TA = -40°C to +125°C (automotive) and 0°C ≤ TA ≤ +70°C (commercial) Operating voltage VDD range as described in DC spec tables 16.3 and 16.4					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
External CLOCKIN Frequency (Note 2)	FOSCRC	DC		4	MHz	RC mode
	FOSCXT	DC		4	MHz	XT mode
	FOSCHS1	DC		20	MHz	HS mode (Com/Ind)
	FOSCHS2	DC		16	MHz	HS mode (Automotive)
	FOSCLP	DC		40	KHz	LP mode
Oscillator Frequency (Note 2)	FOSCRC	DC		4	MHz	RC mode
	FOSCXT	0.1		4	MHz	XT mode
	FOSCHS1	4		20	MHz	HS mode (Com/Ind)
	FOSCHS2	4		16	MHz	HS mode (Automotive)
	FOSCLP	DC		40	KHz	LP mode
Instruction Cycle Time (Note 2)	TCYRC	1.0	4/FOSCRC	DC	µs	RC mode
	TCYXT	1.0	4/FOSCXT	DC	µs	XT mode
	TCYHS	0.2	4/FOSCHS	DC	µs	HS mode
	TCYLP	100	4/FOSCLP	DC	µs	LP mode
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
$\overline{MCLR}$ Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{T_{CY} + 40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	9*	18*	30*	ms	VDD = 5.0V
Oscillation Start-up Timer Period	TOST	9*	18*	30*	ms	VDD = 5.0V
I/O Timing						
I/O Pin Input Valid Before CLKOUT≠ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O Pin Input Hold After CLKOUT≠ (RC Mode)	TDH	0*			ns	
I/O Pin Output Valid After CLKOUTØ (RC Mode)	TPD			40*	ns	

* Guaranteed by characterization, but not tested.

(Notes on next page)

NOTES TO AC CHARACTERISTICS: PIC16C5X-RC, XT, HS, LP (COMMERCIAL) PIC16C5XI-RC, XT, HS, LP (INDUSTRIAL)

1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.
2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.
   All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. **When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.**
3. For a detailed explanation of RTCC input clock requirements see section 4.2.1.
4. Clock-in high-time is the duration for which clock input is at VIHOSC or higher.
   Clock-in low-time is the duration for which clock input is at VILOSC or lower.

16.9 Electrical Structure of Pins

FIGURE 16.9.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB, RC)

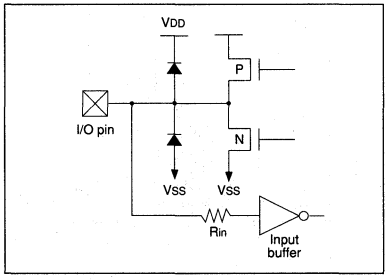
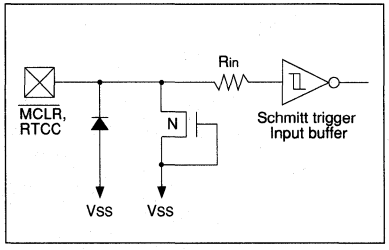


FIGURE 16.9.2 - ELECTRICAL STRUCTURE OF MCLR AND RTCC PINS



17.0 TIMING DIAGRAMS

FIGURE 17.0.1 - RTCC TIMING

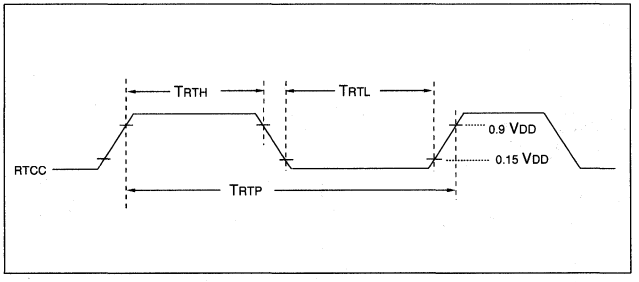
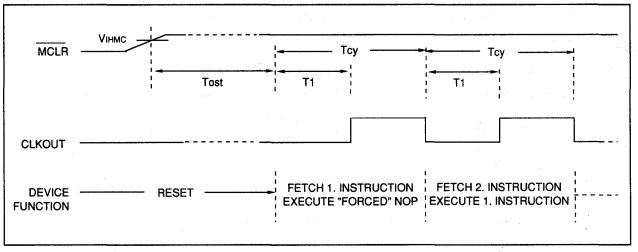
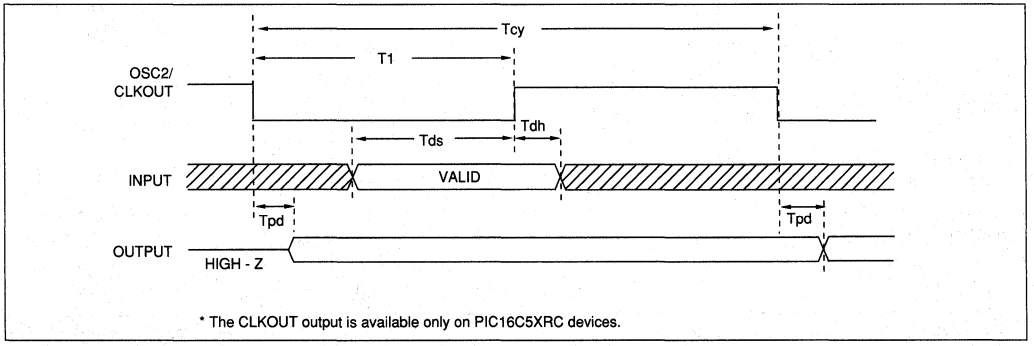


FIGURE 17.0.2 - OSCILLATOR START-UP TIMING (PIC16C5XRC)



Notes to figures 16.9.1 and 16.9.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

FIGURE 17.0.3 - INPUT/OUTPUT TIMING FOR I/O PORTS (PIC16C5XRC*)



* The CLKOUT output is available only on PIC16C5XRC devices.

18.0 DC & AC CHARACTERISTICS GRAPHS/TABLES:

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 18.0.1 - TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

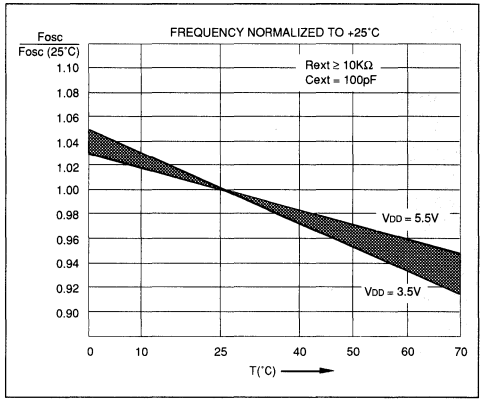


FIGURE 18.0.2 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

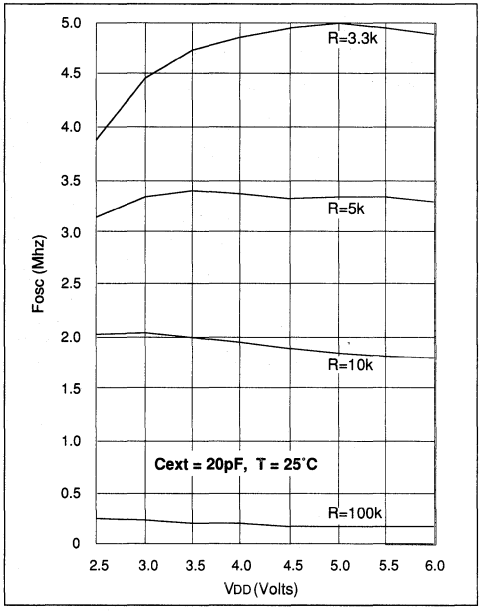


FIGURE 18.0.3 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

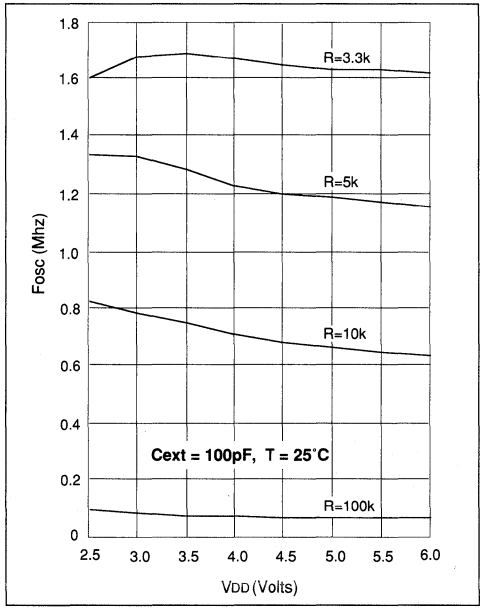


FIGURE 18.0.4 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

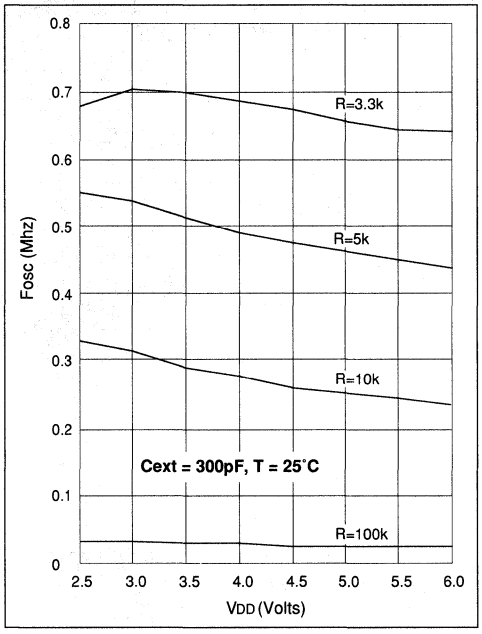


TABLE 18.0.1 - RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	3.3k	4.71 MHz	± 28%
	5k	3.31 MHz	± 25%
	10k	1.91 MHz	± 24%
	100k	207.76 KHz	± 39%
100pf	3.3k	1.65 MHz	± 18%
	5k	1.23 MHz	± 21%
	10k	711.54 KHz	± 18%
	100k	75.62 KHz	± 28%
300pf	3.3k	672.78 KHz	± 14%
	5k	489.49 KHz	± 13%
	10k	275.73 KHz	± 13%
	100k	28.12 KHz	± 23%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for full VDD range.

FIGURE 18.0.5 - TYPICAL Ipd vs VDD WATCHDOG DISABLED 25°C

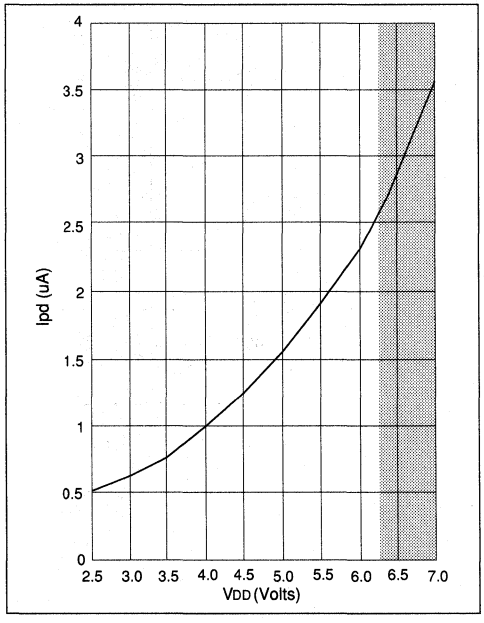
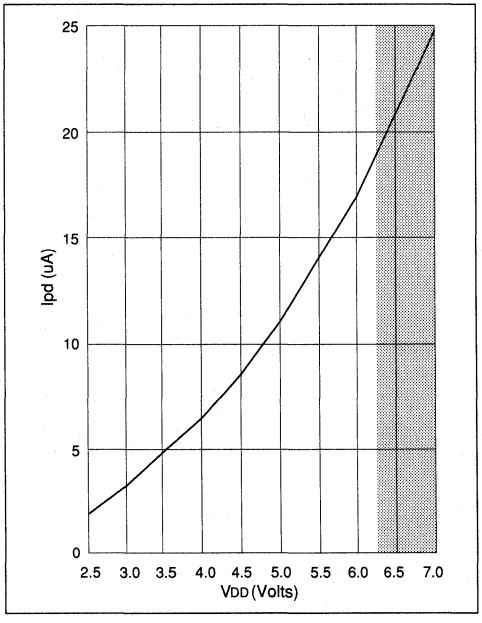


FIGURE 18.0.6 - TYPICAL Ipd vs VDD WATCHDOG ENABLED 25°C



Note: The gray shaded regions are outside the normal PIC operating range. Do not operate in these regions.

FIGURE 18.0.7 - MAXIMUM Ipd vs VDD WATCHDOG DISABLED

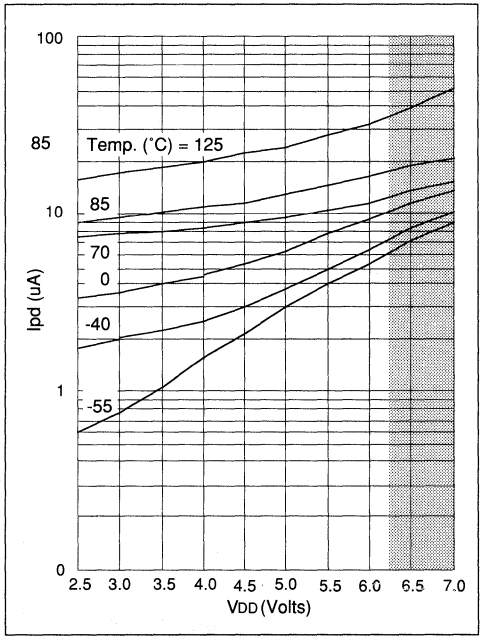
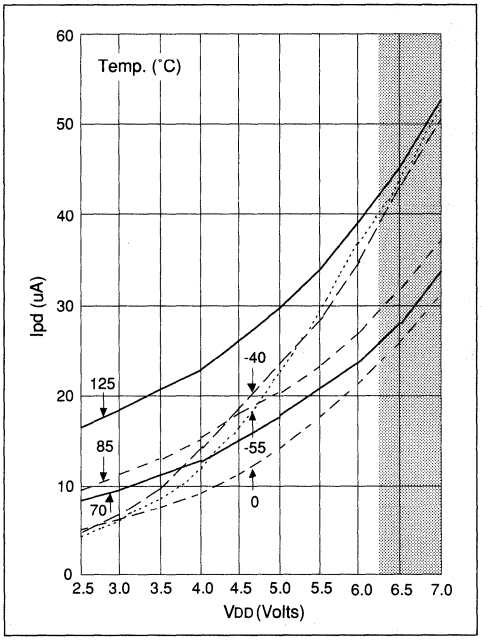


FIGURE 18.0.8 - MAXIMUM Ipd vs VDD WATCHDOG ENABLED*



* IPD, with watchdog timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the watchdog timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

Note: The gray shaded regions are outside the normal PIC operating range. Do not operate in these regions.

FIGURE 18.0.9 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs VDD

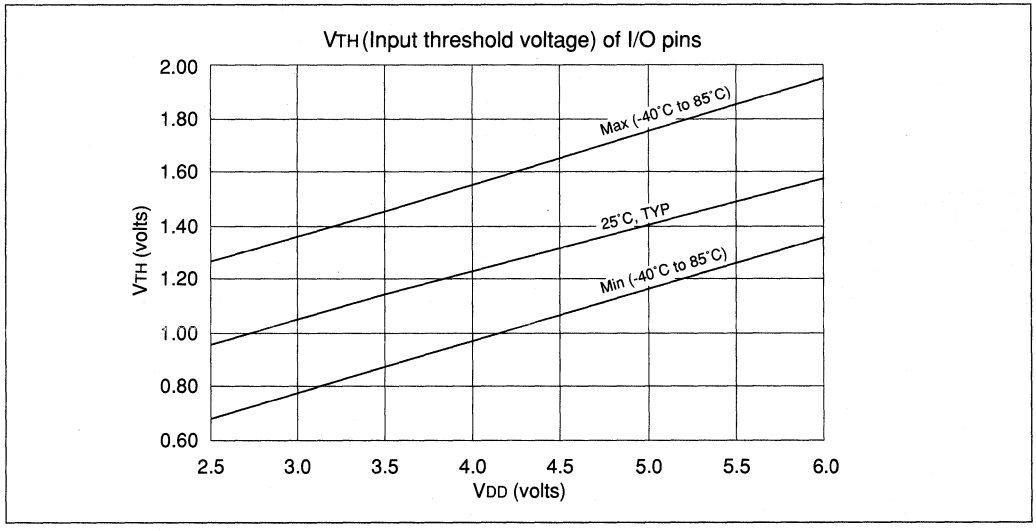
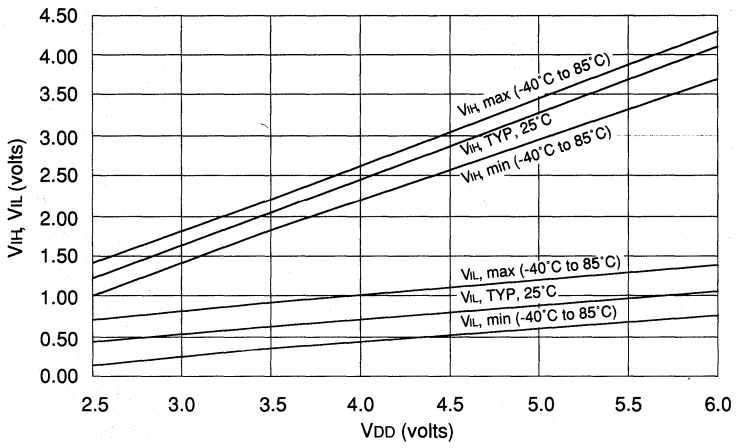


FIGURE 18.0.10 - V_{IH}, V_{IL} OF $\overline{MCLR}$, RTCC AND OSC1 (IN RC MODE) vs V_{DD}



Note: These input pins have Schmitt trigger input buffer.

FIGURE 18.0.11 - V_{TH} (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs V_{DD}

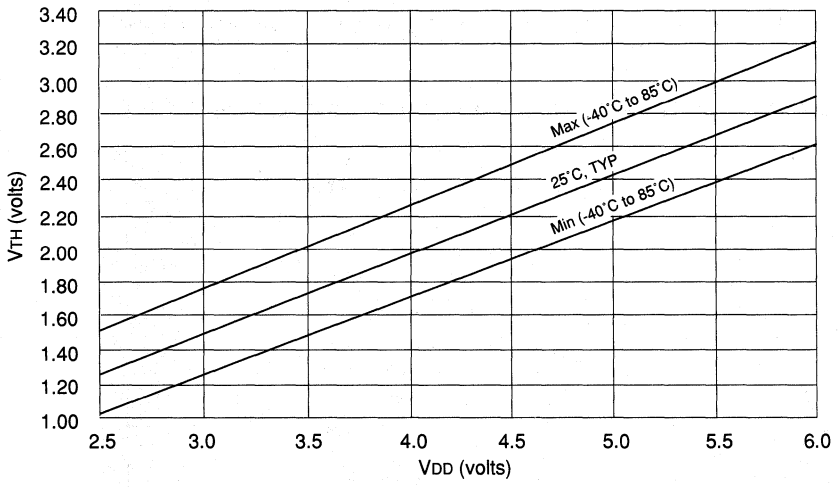


FIGURE 18.0.12 - TYPICAL IDD vs FREQ (EXT CLOCK, 25°C)

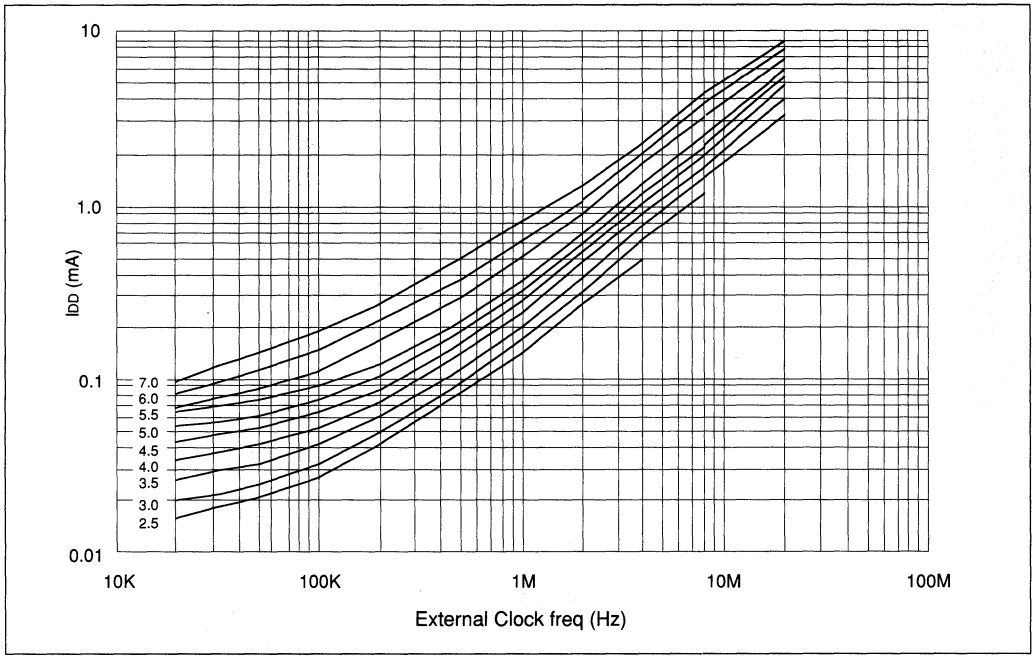


FIGURE 18.0.13 - MAXIMUM IDD vs FREQ (EXT CLOCK, -40° to +85°C)

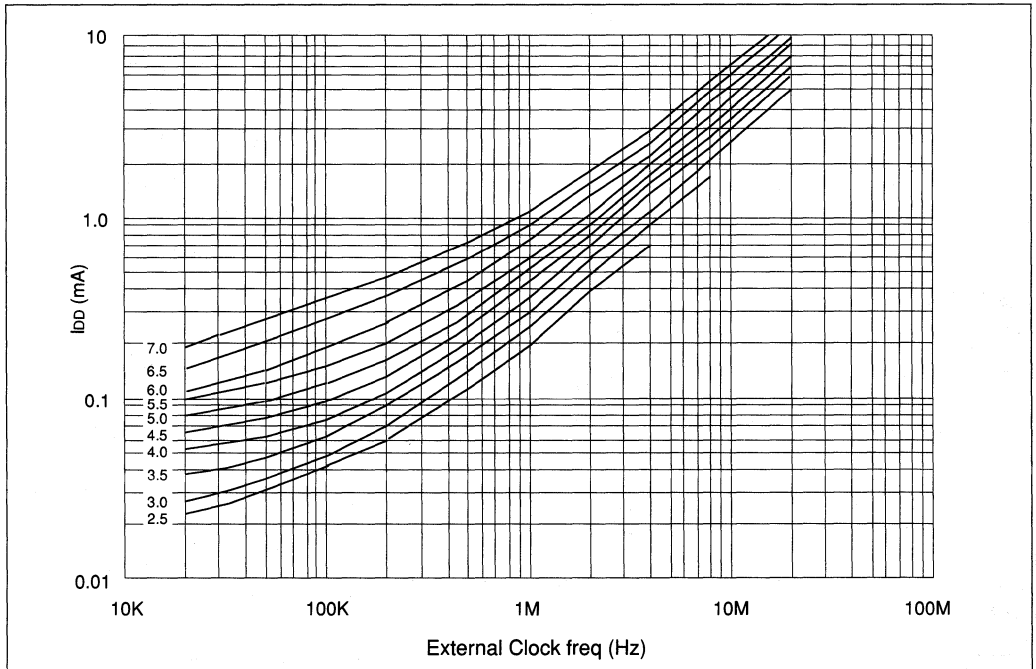


FIGURE 18.0.14 - MAXIMUM IDD vs FREQ (EXT CLOCK, -55° to +125°C)

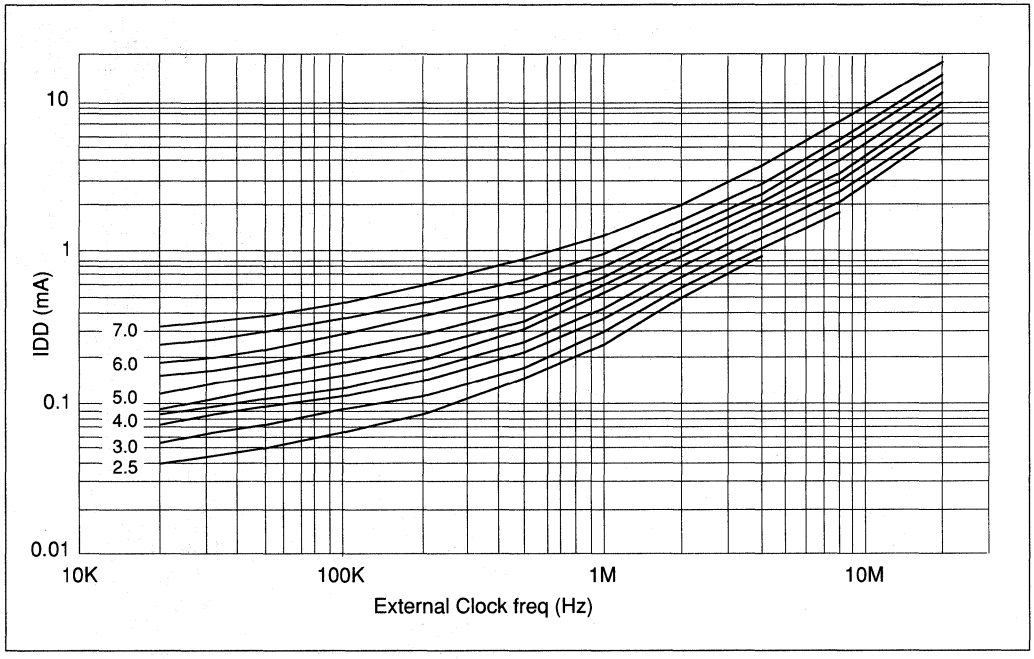


FIGURE 18.0.15 - WDT Timer Time-out Period vs VDD

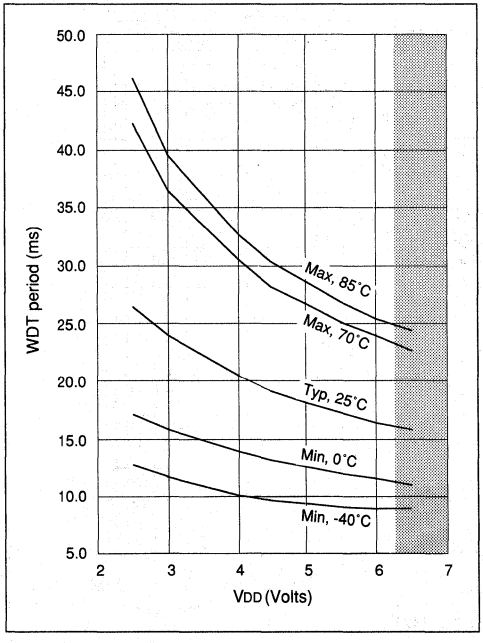
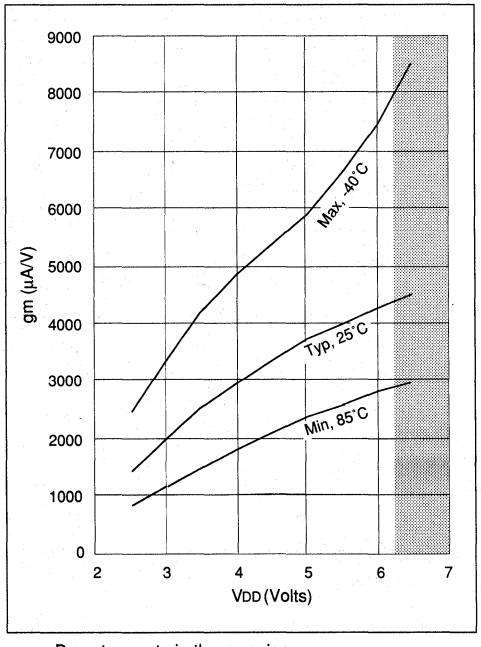


FIGURE 18.0.16 - Transconductance (gm) of HS Oscillator vs VDD



Note: The gray shaded regions are outside the normal PIC operating range. Do not operate in these regions.

FIGURE 18.0.17 - Transconductance (gm) of LP Oscillator vs VDD

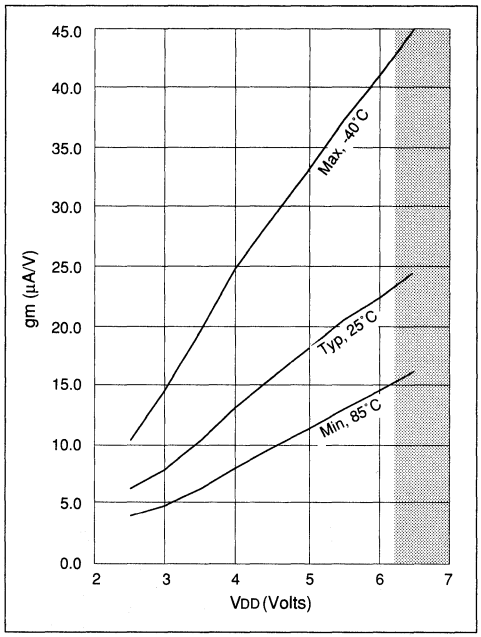
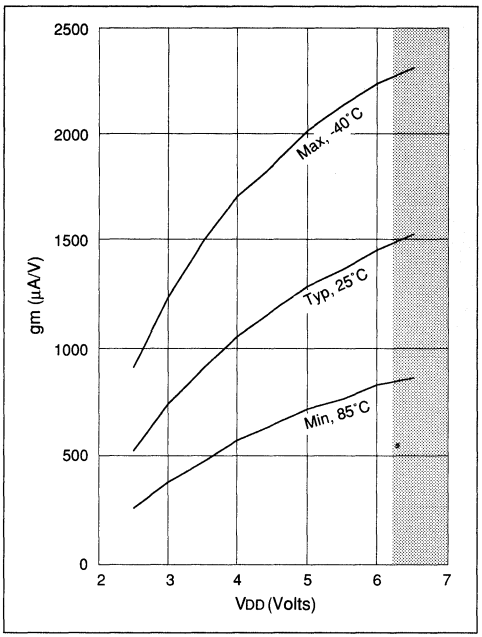


FIGURE 18.0.18 - Transconductance (gm) of XT Oscillator vs VDD



Note: The gray shaded regions are outside the normal PIC operating range. Do not operate in these regions.

FIGURE 18.0.19 - IOH vs VOH, VDD = 3V

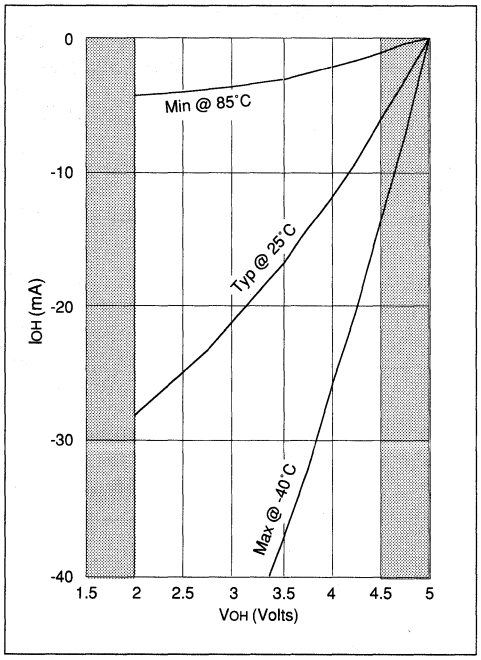


FIGURE 18.0.20 - IOH vs VOH, VDD = 5V

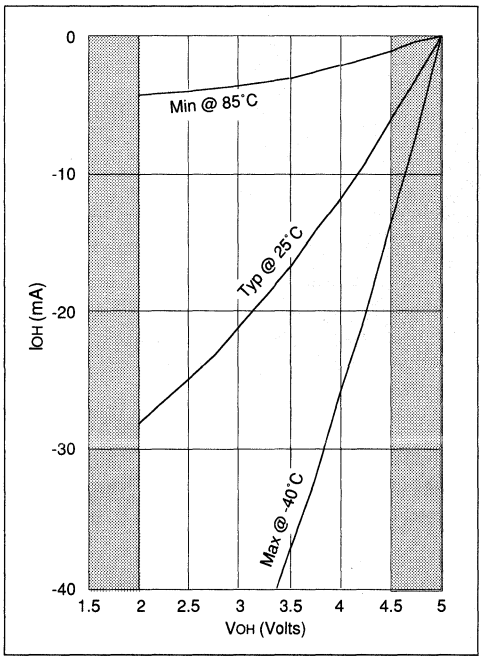


FIGURE 18.0.21 - IOL vs VOL, VDD = 3V

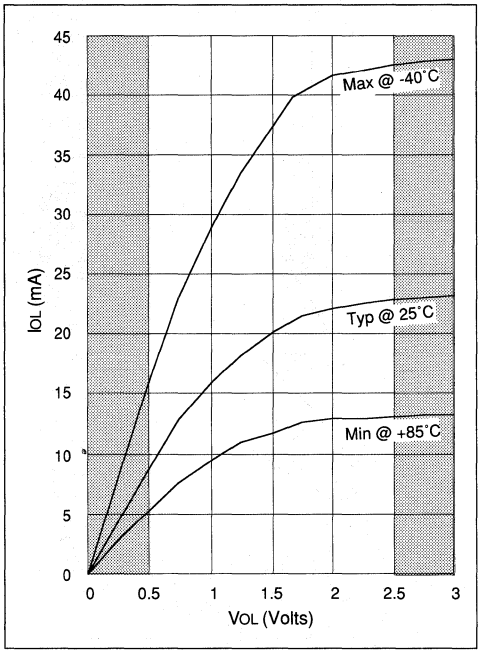
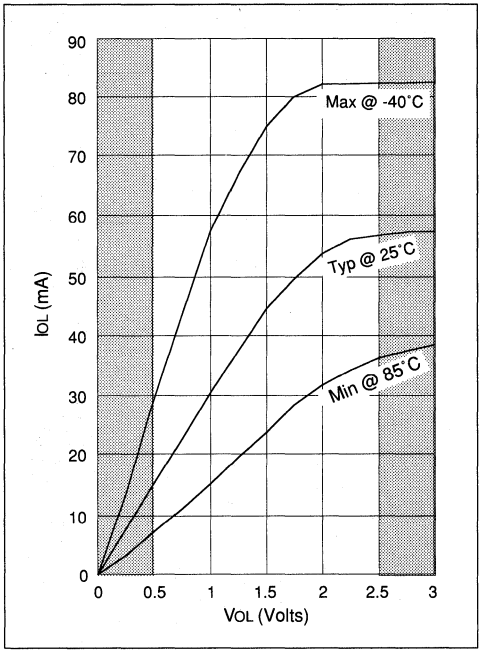


FIGURE 18.0.22 - IOL vs VOL, VDD = 5V



Note: The gray shaded regions are outside the normal PIC operating range. Do not operate in these regions.

TABLE 18.0.2 - INPUT CAPACITANCE FOR PIC16C54/56 *

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
RTCC	3.2	2.8

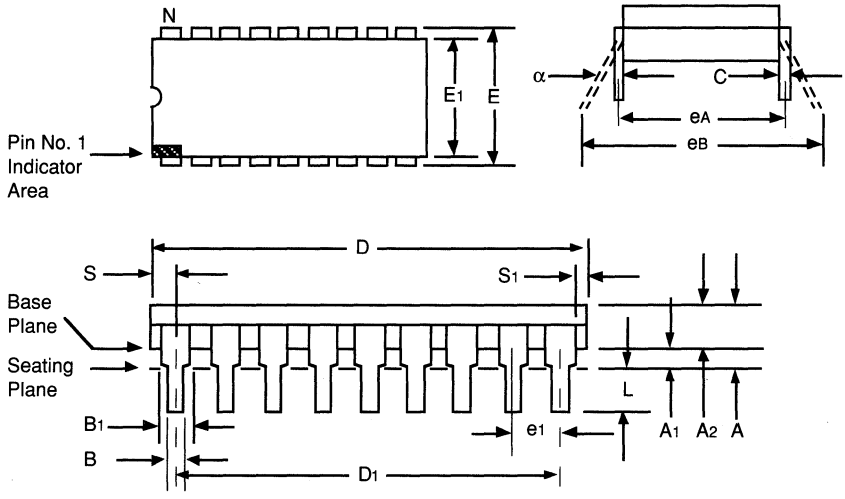
* All capacitance values are typical at 25°C and measured at 1 MHz. A part to part variation of ±25% (three standard deviations) should be taken into account.

TABLE 18.0.3 - INPUT CAPACITANCE FOR PIC16C55/57 *

Pin Name	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
MCLR	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
RTCC	4.5	3.5

19.0 PACKAGING DIAGRAMS AND DIMENSIONS

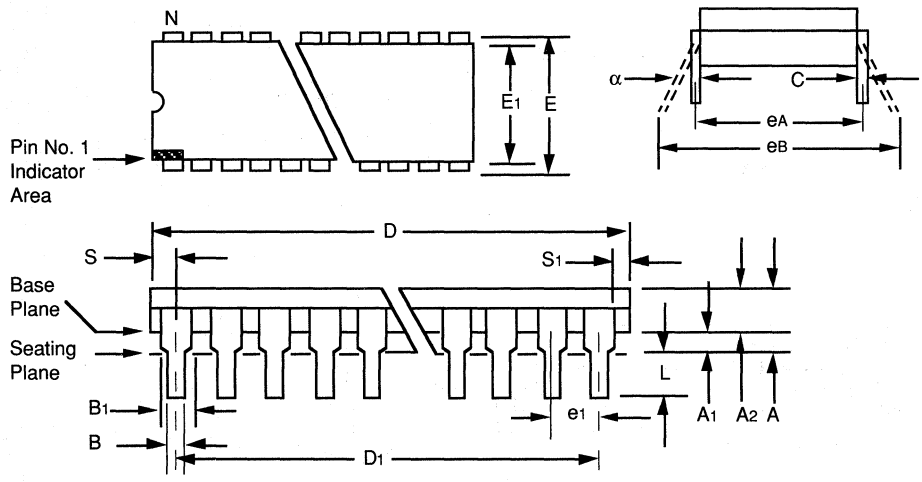
19.1 18-LEAD PLASTIC DUAL IN-LINE (300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.479	23.495		0.885	0.925	
D1	20.320	20.32	**Reference**	0.800	0.800	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

PACKAGING DIAGRAMS AND DIMENSIONS (CONT.)

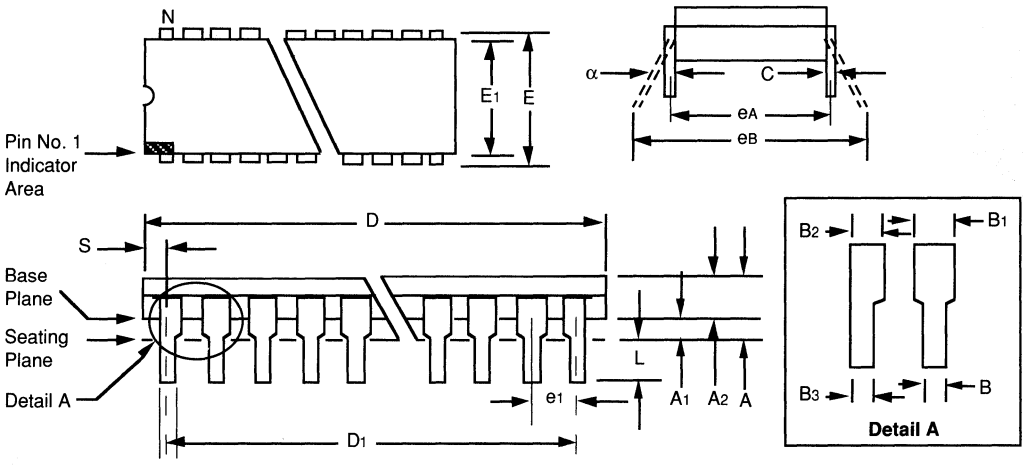
19.2 28-LEAD DUAL IN-LINE PLASTIC (600 mil)



Package Group: Plastic Dual-In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B1	1.270	1.778	**Typical**	0.050	0.070	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	35.560	37.084		1.400	1.460	
D1	33.020	33.020	**Reference**	1.300	1.300	**Reference**
E	15.240	15.875		0.600	0.625	
E1	12.827	13.970		0.505	0.550	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	28	28		28	28	
S	0.889	–		0.035	–	
S1	0.508	–		0.020	–	

PACKAGING DIAGRAMS AND DIMENSIONS (CONT.)

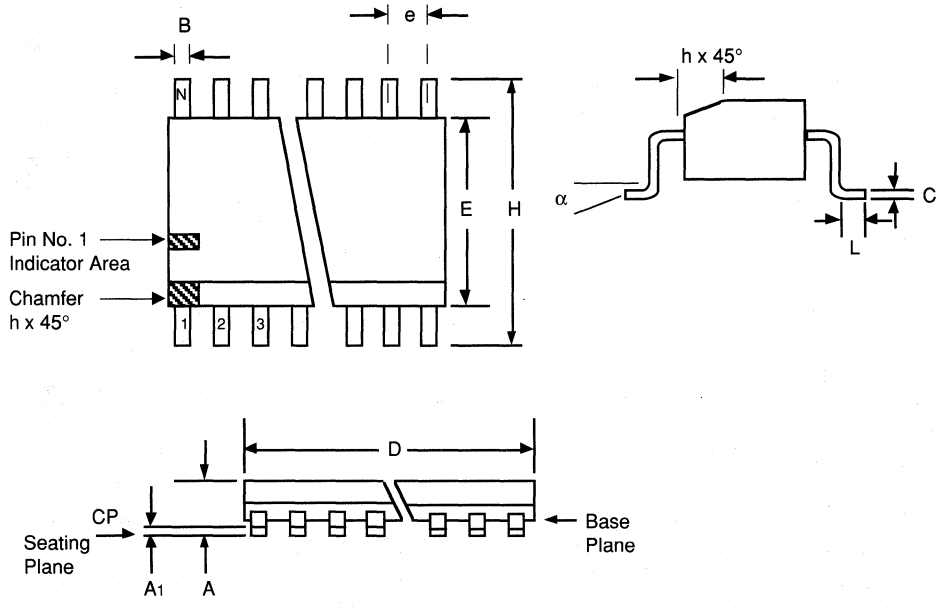
19.3 28-LEAD DUAL IN-LINE PLASTIC (300 mil)



Package Group: Plastic Dual-In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.63	4.57		.143	.180	
A1	.38	–		.015	–	
A2	3.25	3.65		.128	.140	
B	.41	.56		.016	.022	Typical
B1	1.02	1.65	Typical	.040	.065	
B2	.762	1.02	4 places	.030	.040	4 places
B3	.20	.51	4 places	.008	.020	4 places
C	.20	.33	Typical	.008	.013	Typical
D	34.16	35.43		1.345	1.395	
D1	33.02	33.02	Reference	1.300	1.300	Reference
E	7.87	8.38		.310	.330	
E1	7.1	7.52		.280	.296	
e1	2.54	2.54	Typical	.100	.100	Typical
eA	7.87	7.87	Reference	.310	.310	Reference
eB	8.64	9.65		.340	.380	
L	3.18	3.68		.125	.145	
N	28	-		28	-	
S	.58	1.22		.023	.048	

PACKAGING DIAGRAMS AND DIMENSIONS (CONT.)

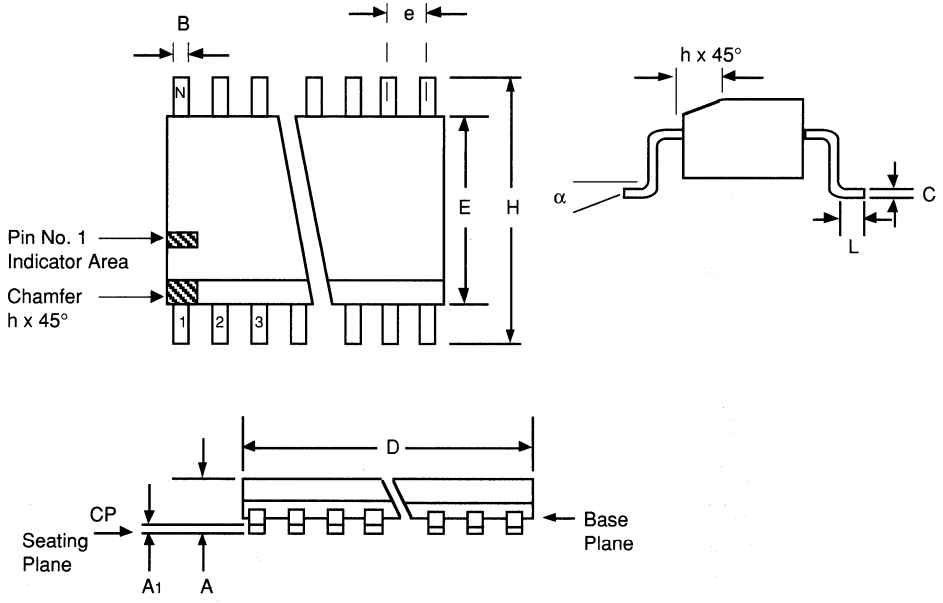
19.4 18-LEAD PLASTIC SURFACE MOUNT (SOIC - WIDE, 300 mil BODY)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A_1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	11.3538	11.7348		0.447	0.462	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	18	18		18	18	
CP	–	0.1016		–	0.004	

PACKAGE OUTLINES (CONT.)

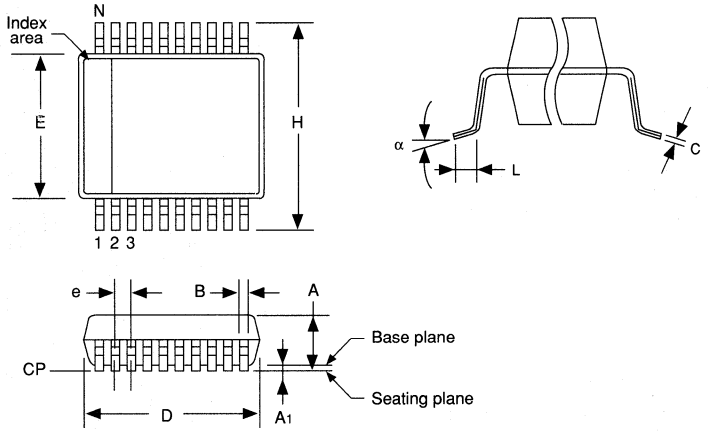
19.5 28-LEAD PLASTIC SURFACE MOUNT (SOIC - WIDE, 300 mil BODY)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A_1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	17.7038	18.0848		0.697	0.712	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	28	28		28	28	
CP	–	0.1016		–	0.004	

PACKAGE OUTLINES (CONT.)

19.6 20-LEAD PLASTIC SURFACE MOUNT (SSOP - .209 mil BODY 5.30 mm)



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.73	1.99		0.68	0.78	
A_1	0.05	0.21		0.002	0.008	
B	0.25	0.38		0.010	0.015	
C	0.13	0.22		0.005	0.009	
D	7.07	7.33		0.278	0.289	
E	5.20	5.38		0.205	0.212	
e	0.65	0.65	Typical	0.256	0.256	Typical
H	7.65	7.90		0.301	0.311	
L	0.55	0.95		0.022	0.037	
N	20	20		20	20	
CP	-	0.1016		-	0.004	

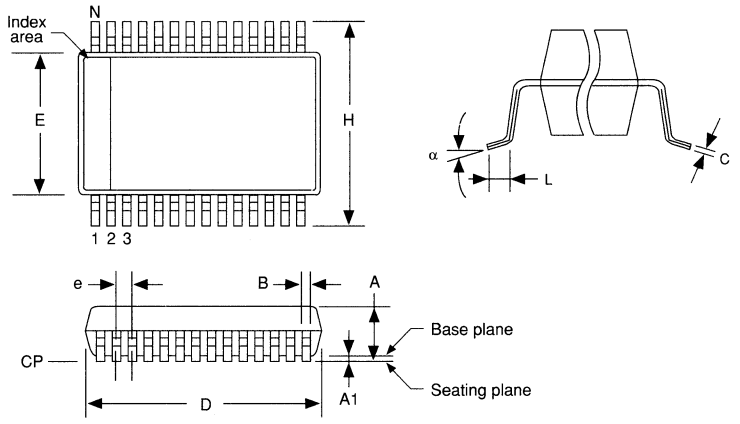
Symbol List for Shrink Small Outline Package Parameter	
Symbol	Description of Parameters
α	Angular spacing between min. and max. lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead positions
CP	Seating plane coplanarity

Notes: 1. Controlling parameter: mm.

2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .006 package ends and .010 on sides.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

PACKAGE OUTLINES (CONT.)

19.7 28-LEAD PLASTIC SURFACE MOUNT (SSOP - .209 mil BODY 5.30 mm)



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.73	1.99		0.68	0.78	
A_1	0.05	0.21		0.002	0.008	
B	0.25	0.38		0.010	0.015	
C	0.13	0.22		0.005	0.009	
D	10.07	10.33		0.397	0.407	
E	5.20	5.38		0.205	0.212	
e	0.65	0.65	**Typical**	0.256	0.256	**Typical**
H	7.65	7.90		0.301	0.311	
L	0.55	0.95		0.022	0.037	
N	28	28		28	28	
CP	-	0.1016		-	0.004	

Symbol List for Shrink Small Outline Package Parameter	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead positions
CP	Seating plane coplanarity

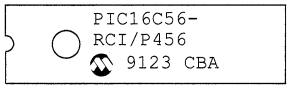
Notes: 1. Controlling parameter: mm.

2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .006 package ends and .010 on sides.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

19.8 PACKAGE MARKING INFORMATION

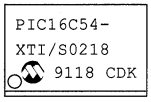
18L PDIP

Example

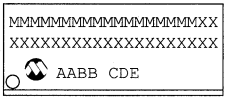


18L SOIC

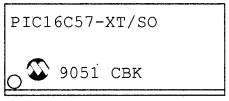
Example



28L SOIC

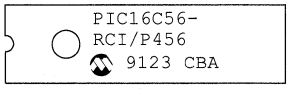


Example

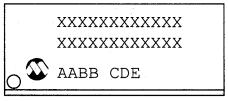


28L PDIP (.300 mil)

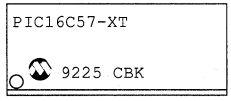
Example



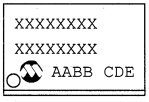
28L SSOP



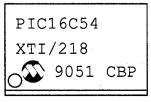
Example



20L SSOP



Example



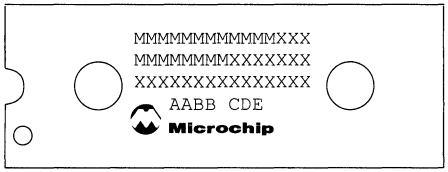
Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

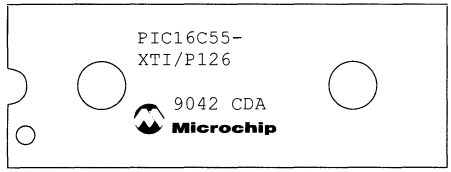
* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are incuded in QTP price.

19.8 PACKAGE MARKING INFORMATION (Cont.)

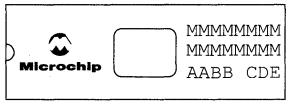
28L PDIP (.600 mil)



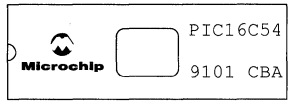
Example



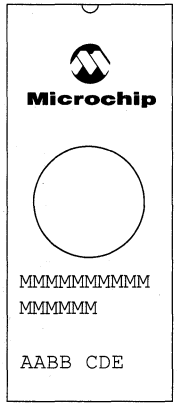
18L Cerdip



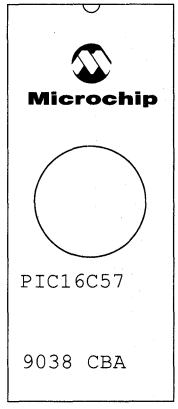
Example



28L Cerdip



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

20.0 DEVELOPMENT SUPPORT

Overview: The PIC16C5X family is supported by a variety of development tools:

- High Performance In-Circuit Emulator (PICMASTER)
- Low Cost Production Quality Programmer (PICPRO II)
- Microchip's Universal Production Quality Programmer (PRO MASTER)
- PC Based Assembler (PICALC)
- PC Based Simulator (PICSIM)

Microchip offers several bundled development tool systems for convenience and cost benefit to the customer. For PIC16C5X the following are available:

- PICPAK II: Assembler, Simulator, PICPRO II Programmer and windowed samples for development.
- PICMASTER-16: Assembler, Simulator, PICPRO II Programmer, PICMASTER emulator and windowed samples for development.

20.1 PICMASTER™: High Performance Universal In-Circuit Emulator System

The PICMASTER Universal In-Circuit Emulator System is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16CXX and PIC17CXX families. This system currently supports the PIC16CR54, PIC16C54, PIC16C55, PIC16C56 and PIC16C57, and PIC17C42 processors. PIC16C71 support is planned.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.0 environment, allowing the operator access to a wide range of supporting software and accessories.

Provided with the PICMASTER System is a high performance real-time In-Circuit Emulator, a programmer unit and a macro assembler program.

Coupled with the user's choice of text editor, the system is ready for development of products containing any of Microchip's microcontroller products.

A "Quick Start" PIC Product Sample Pak containing user programmable parts is included for additional convenience.

Microchip provides additional customer support to developers through an Electronic Bulletin Board System (EBBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS system.

20.1.1 Host System Requirements:

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to you the end user. To properly take advantages of these features, PICMASTER requires installation on a system having the following minimum configuration:

- PC AT compatible machine: 80286, 386SX, 386DX, or 80486 with ISA or EISA Bus.
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended).
- MSDOS / PCDOS version 3.1 or greater.
- Microsoft Windows® version 3.0 or greater operating in either standard or 386 enhanced mode).
- 1 Mbyte RAM (2 Mbytes recommended).
- One 5.25" floppy disk drive.
- Approximately 10 Mbytes of hard disk (1 Mbyte required for PICMASTER, remainder for Windows 3.X system).
- One 8-bit PC AT (ISA) I/O expansion slot (half size)
- Microsoft® mouse or compatible (highly recommended).

20.1.2 Emulator System Components:

The PICMASTER Emulator Universal System consists primarily of 4 major components:

- **Host-Interface Card:** The PC Host Interface Card connects the emulator system to an IBM PC compatible system. This high-speed parallel interface requires a single half-size standard AT / ISA slot in the host system. A 37-conductor cable connects the interface card to the external Emulator Control Pod.
- **Emulator Control Pod:** The Emulator Control Pod contains all emulation and control logic common to all microcontroller devices. Emulation memory, trace memory, event and cycle timers, and trace/breakpoint logic are contained here. The Pod controls and interfaces to an interchangeable target-specific emulator probe via a 14" precision ribbon cable.
- **Target-specific Emulator Probe:** A probe specific to microcontroller family to be emulated is installed on the ribbon cable coming from the control pod. This probe configures the universal system for emulation of a specific microcontroller.
- **PC Host Emulation Control Software:** Host software necessary to control and provide a working user interface is the last major component of the system. The emulation software runs in the Windows 3.X environment, and provides the user with full display, alter, and control of the system under emulation. The Control Software is also universal to all microcontroller families.

The Windows 3.X System is a multitasking operating system which will allows the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.X, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

Under Windows 3.X, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16Cxx processor and a PIC17Cxx processor).

FIGURE 20.1.1 - PICMASTER

FIGURE 20.1.2 - PICMASTER SYSTEM CONFIGURATION

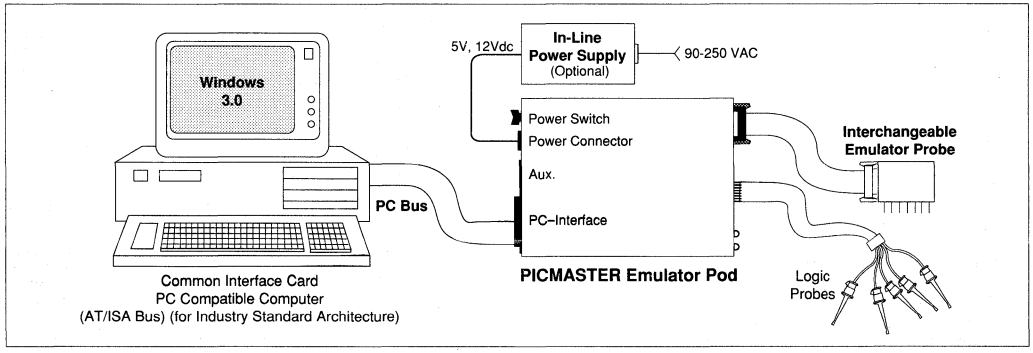
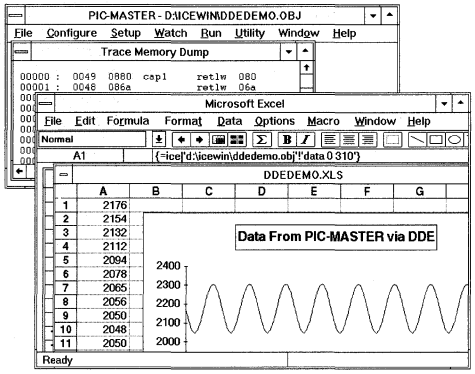


FIGURE 20.1.3 - PICMASTER TYPICAL SCREEN



20.2 PICPAK-II™ Development Kit

When real time or in-circuit emulation is not required for code development the PICPAK-II (PIC Applications Kit) offers the right solution. This very low cost PC hosted software development tool combines the power and versatility of the PICALC assembler and PICSIM simulator software tools to compile, execute, debug and analyze microcode in a PC hosted environment. Microcode debugging capability includes software trace, breakpoints, symbolic debug and stimulus file generation. An EPROM PIC Programmer (PICPRO II) and "Quick Start" PIC16C5X product sample PAK is included for final code verification.

20.3 PICALC Cross-Assembler

The PIC Cross Assembler PICALC is a PC hosted software development tool supporting the PIC16C5X CMOS series and PIC16C5X/7X NMOS series microcontrollers. PICALC offers a full featured Macro and Conditional assembly capability. It can also generate various object code formats including several Hex formats to support Microchip's proprietary development tools as well as third party tools. Also supports Hex (default), Decimal and Octal Source and listing formats. An assembler users manual is available for detailed support.

20.4 PICSIM™ Software Simulator

PICSIM is a software tool which allows for PIC16C5X code development in a PC host environment. The PICSIM software allows you to simulate the PIC16C5X series microcontroller products on an instruction level. On any given instruction, the user may examine or modify any of the data areas within the PIC or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. PICSIM uses two forms of symbolic debugging: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. PICSIM offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi project software development tool.

20.5 PICPRO™ II Programmer

PICPRO II is a production quality programmer with both stand-alone and PC based operation. The PICPRO II will program the entire family of PIC16C5X series of 8-bit microcontrollers. It can read, program, verify, and code protect parts without the need of a PC host. Its EEPROM memory holds programming data and parametric information even when power is removed making it ideal for duplicating PICs. It can also operate with a PC host and do complete read, program, verify, as in stand-alone mode with the additional features of program buffer editing, serialization of both code-protected and non code-protected parts. The PICPRO II comes with both 28 and 18 pin zero insertion force programming sockets on a removable socket module. Additional socket modules are available for the SOIC and PLCC packages. The PICPRO II conforms fully to Microchip's Programming Algorithm. Its programmable VCC and VPP supplies allow the PICPRO II to support PIC microcontrollers with various operating voltage ranges.

20.6 PRO MASTER™

The PRO MASTER programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MASTER has programmable VDD and VPP supplies which allows it to verify the PIC at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MASTER can read, verify or program a part. It can also set fuse configuration and code-protect in this mode. It's EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

In PC-hosted mode, the PRO MASTER connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is

possible where each part is programmed with a different serial number, sequential or random.

The PRO MASTER has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. It is planned that the PRO MASTER will support all current and future PIC16CXX and PIC17CXX processors. Currently socket modules are available for the PIC16C54, PIC16C55, PIC16C56, PIC16C57, PIC17C42 and the PIC16C71.

21.0 EPROM PROGRAMMING

21.1 Prototype Programmers

Microchip's proprietary PIC16C5X series Development System and PICPRO, were not designed for high volume production programming but were designed strictly to support engineering development level programming of PIC16C5X EPROM and OTP units. Microchip assumes no responsibility for the replacement of programming rejects when these development tools are used to support high volume production level programming.

21.2 Production Quality Programmers

Microchip's proprietary PICPRO II programmer can be used for reliable programming for production. High volume programming is also supported by production quality programmers from third party sources. See table 21.2.1.

Microchip assumes no responsibility for replacing defective units related to mechanical and/or electrical problems of any third party programming equipment or the improper use of such equipment.

Programming of the code protection bit (also called "security bit" or "security fuse") implies that the contents of the PIC16C5X EPROM can no longer be verified, thus making programming related failure analysis an impossibility.

Microchip warrants that PIC16C5X units will not exceed a programming failure rate of 1% of shipment quality. Programming related failures beyond this level can be returned for replacement, again, if the security bit has not been programmed.

21.3 Gang Programmers

Gang programmers are available from third party sources. See table 21.2.1.

21.4 Factory Programming

High volume factory programming (QTP) is an available service from Microchip Technology. A small price adder and minimum quantity requirements apply.

TABLE 21.2.1 LIST OF 3RD PARTY PROGRAMMERS*

Company	Model	Contact	Company	Model	Contact
ADVIN Systems, Inc.†	PILOT™-U40	408-984-8600 U.S.	HI-LO†	ALL-03	02 7640215 Taiwan
Application Solutions Ltd.	PIC Programmer	273 476608 U.K.	Link Computer Graphics†	CLK-3100	301-994-6669 U.S.
Baradine Products Ltd.	Micro-Burner™	604-988-9853 Canada	Logical Devices, Inc.	ALLPRO™-88	800-331-7766 U.S. 305-974-0967 U.S.
BP Microsystems	CP-1128™	800-225-2102 U.S. 713-461-4958 U.S.	Magic I/O	SPPIC	5957292 Taiwan
Citadel Products Ltd†	PC-82	44-819-511-848 U.K.	Maple Technology, Ltd	MQP-200	44-666-825-146 U.K.
Data I/O Corporation	Unisite™ with Site-48™ module	800-288-4065 U.S. 31(0) 6622866 Europe (03) 432-6991 Japan	Parallax, Inc.	PIC16C5X-PGM	916-721-6669 U.S.
			SMS	Sprint™ Expert	49-7522-4460 Germany
Elan Digital Systems Ltd.	EF-PER™ 5000 Series Gang Programmer	0489 579 799 U.K. (408) 946 3864 U.S.	Stag Microsystems†	PP39	44-707-332-148 U.K.
			Transdata	PGM16 PGM 16x8 Gang Programmer	(214) 980 2960

* As of July, 1992

† Product is available but Microchip has not evaluated it yet (as of July, 1992).

All trademarks shown in table 21.2.1 belong to their respective holders.

Notes:

Index

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices. For the *currently available code-combinations*, refer to previous page.

PART NO. - XX X /XX XXX

Pattern:	3-Digit Pattern Code for QTP (blank for OTP and Window Parts)		
Package:	P = PDIP	SS = SSOP (209 mil)	
	SO = 300 mil SOIC (Gull Wing Lead)	JW* = CERDIP Window	
	SP = 28L PDIP (300 mil)	S = Die in Waffle Pack	
Temperature Range:	- = 0° C to +70°C (T for tape/reel)		
	I = -40° C to +85°C (S for tape/reel)		
	E = -40°C to +125°C		
Oscillator Type:	RC XT HS LP		
Device:	PIC16C54 PIC16C55 PIC16C56 PIC16C57		

Examples:

a) PIC16C54 - XT/PXXX = "XT" oscillator, commercial temp., PDIP, QTP pattern

b) PIC16C55 - XTI/SO = "XT" oscillator, industrial temp., SOIC (OTP device)

c) PIC16C55 - JW = Commercial temp. CERDIP with WINDOW

d) PIC16C57-RCI/S = "RC oscillator", industrial temp., dice in waffle pack.

e) PIC16C54-LPE/SS = "LP oscillator", Automotive temp., SSOP package

Notes: * For UV-erasable devices, the oscillator type is RC by default (= erased device). The user can select XT, HS, or LP oscillators by programming the appropriate fuses.

PIC®16CR54

ROM-Based 8-Bit CMOS Microcontroller

FEATURES

High performance RISC-like CPU

- Only 33 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 12-bit wide instructions
- 8-bit wide data path
- 512 x 12 on-chip ROM program memory
- 25 x 8 general purpose registers (SRAM)
- 7 special function hardware registers
- 2 level deep hardware stack
- Direct, indirect and relative addressing modes

Peripheral features

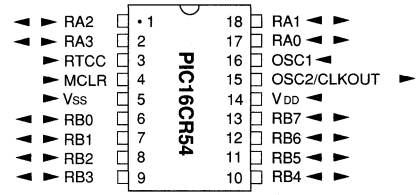
- 12 I/O pins with individual direction control
- 8 bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- Power on reset
- Oscillator start-up timer
- Watchdog timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security bit for code-protection
- Power saving SLEEP mode
- ROM mask selectable oscillator options:
  - Low cost RC oscillator: RC
  - Standard crystal/resonator: XT
  - High speed crystal/resonator: HS
  - Power saving low frequency crystal: LP

CMOS technology

- Low power, high speed CMOS ROM technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 6.25V
  - Industrial: 2.0V to 6.25V
- Low power consumption
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 KHz
  - < 1 µA typical standby current @ 3V

FIGURE A - PIN CONFIGURATION

PDIP, SOIC



OVERVIEW

PIC16CR54 is a fully compatible ROM-version of the PIC16C54 EPROM based microcontroller and a member of the PIC16C5X microcontroller family. The PIC16CR54 is a low cost, high performance, 8-bit, fully static CMOS microcontroller. It employs a RISC-like architecture with only 33 single word/single cycle instructions to learn. All instructions are single cycle (200ns) except in the case of program branches which take two cycles. The PIC16CR54 delivers performance an order of magnitude higher than its competitors in similar price category.The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression advantage over other 8-bit microcontrollers in its category. The easy to use and easy to remember instruction set reduces development time significantly.

The customer can also take full advantage of the UV-erasable PIC16C54 EPROM version for code development. The cost-effective One Time Programmable (OTP) version allows the customer to move in to production without committing to a final ROM code.

The PIC16CR54 is supported by an assembler, a software simulator and an in-circuit emulator. All the tools are supported by IBM PC and compatible machines.

Table of Contents

Table of Figures

Table of Tables

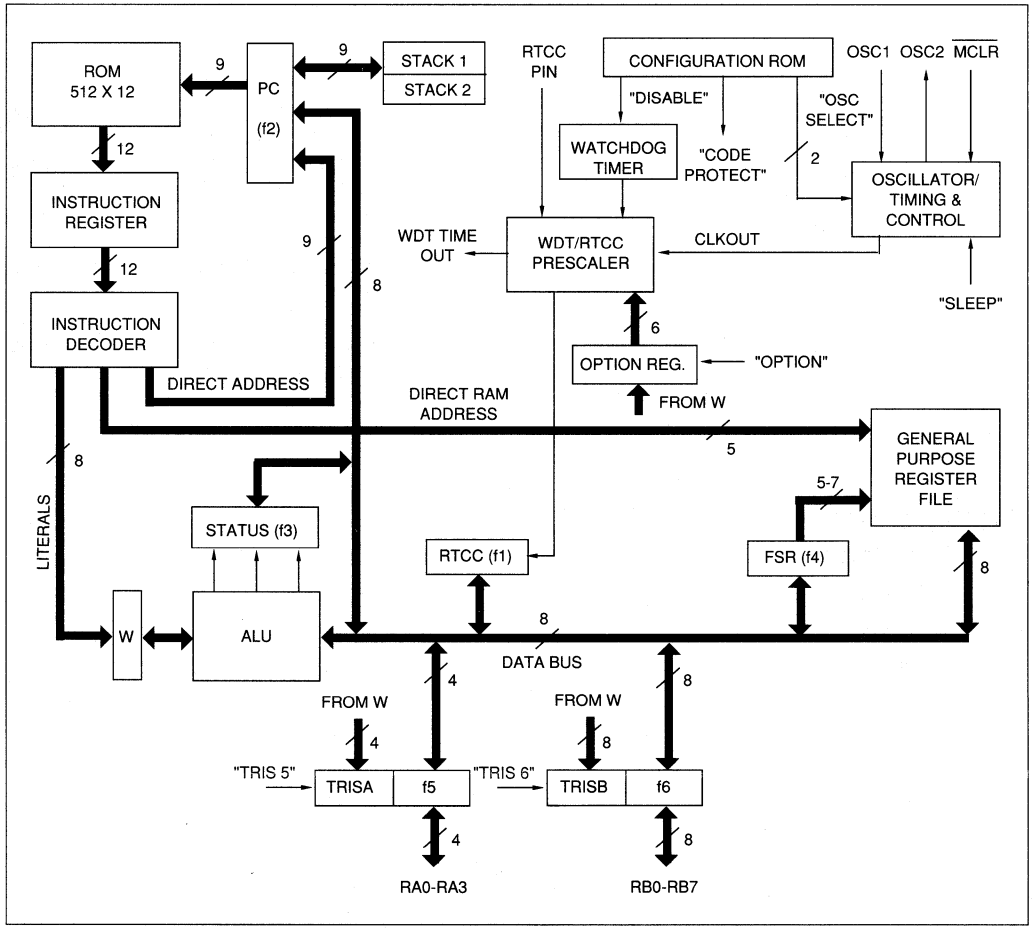
1.0 GENERAL DESCRIPTION

The Microchip Technology PIC16CR54 microcontroller is based on the proven architecture of the PIC16C5X product family. The PIC16CR54 is pin for pin compatible with the EPROM based PIC16C54, but it has the added advantage of an extended operating voltage (2.5V - 6.0V).

1.1 APPLICATIONS

The PIC16CR54 fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices, and telecommunications processors. The small footprint package for through hole or surface mounting make this microcontroller perfect for all applications with space limitations. Low cost, low power, high performance, ease of use, and I/O flexibility make the PIC16CR54 very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

FIGURE 2.1.1 - PIC16CR54 BLOCK DIAGRAM



2.0 ARCHITECTURAL DESCRIPTION

2.1 Harvard Architecture

The PIC16CR54 single-chip microcomputer is a low-power, high-speed, fully static CMOS device containing ROM, RAM, I/O, and a central processing unit on a single chip.

The architecture is based on a register file concept with separate bus and memories for data and instructions (Harvard architecture). The data bus and memory (RAM) are 8-bits wide while the program bus and program memory (ROM) have a width of 12-bits. This concept allows a simple yet powerful instruction set designed to emphasize bit, byte and register operations under high speed with overlapping instruction fetch and execution cycles. In other words, while one instruction is executed, the following instruction is already being read from the program memory. A block diagram of the PIC16CR54 is given in Figure 2.1.1.

TABLE 2.1.1 - PIN FUNCTION TABLE

Name	Function
RA0 - RA3	I/O PORT A
RB0 - RB7	I/O PORT B
RTCC	Real Time Clock/Counter
$\overline{MCLR}$	Master Clear
OSC1	Oscillator (input)
OSC2/CLKOUT	Oscillator (output)
V_{DD}	Power supply
V_{SS}	Ground

2.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 2.2.1.

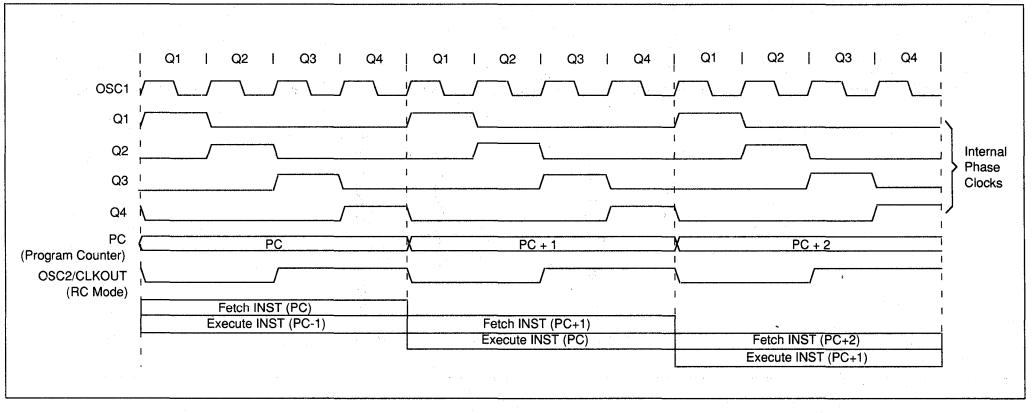
2.3 Data Register File

The 8-bit data bus connects two basic functional elements together: the Register File composed of 32 addressable 8-bit registers including the I/O Ports, and an 8-bit wide Arithmetic Logic Unit. The 32 bytes of RAM are directly addressable (Figure 2.3.1). Data can be addressed direct, or indirect using the file select register (f4). Immediate data addressing is supported by special "literal" instructions which load data from program memory into the W register.

The register file is divided into two functional groups: operational registers and general purpose registers. The operational registers include the Real Time Clock Counter (RTCC) register, the Program Counter (PC), the Status Register, the I/O registers (PORTs), and the File Select Register. The general purpose registers are used for data and control information under command of the instructions.

In addition, special purpose registers are used to control the I/O port configuration, and the prescaler options.

FIGURE 2.2.1 - CLOCKS/INSTRUCTION CYCLE



2.4 Arithmetic/Logic Unit (ALU)

The 8-bit wide ALU contains one temporary working register (W Register). It performs arithmetic and Boolean functions between data held in the W Register and any file register. It also does single operand operations on either the W register or any file register.

2.5 Program Memory

512 words of 12-bit wide on-chip read only program memory (ROM) can be directly addressed. Sequencing of instructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations, supporting direct, indirect, relative addressing modes, can be performed by Bit Test and Skip instructions, Call instructions, Jump instructions or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting.

3.0 PIC16CR54 OVERVIEW

A wide variety of oscillator types, frequency ranges, and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please refer to the part numbering system on the back page of this document.

To facilitate development and initial production phases, Microchip offers UV erasable EPROM version, One Time Programmable (OTP) version as well as Quick-Turnaround-Production (QTP) devices as described in the following sections. For more details on these, please refer to "PIC16C5X data-sheet" (DOC# DS30015) or contact your nearest sales office.

3.1 UV Erasable Device for Program Development

Microchip offers PIC16C54, the EPROM based version of the PIC16CR54 for program development. This device is optimal for prototype development and pilot series. The desired oscillator configuration is EPROM programmable as "RC", "XT", "HS" or "LP". An erased device is configured as "RC" type by default. The user should refer to the PIC16C5X data sheet for full electrical specification of these parts.

The available PIC development tools, "PICPRO™ and PICPRO™ II can program all PIC16C5X devices for prototyping and pilot series up to low-volume production.

3.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates. OTP devices are ideal for initial production runs. OTP devices have the oscillator type pre-configured by the factory.

3.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. QTP devices are also ideal for initial production. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

TABLE 3.0.1 - OVERVIEW OF PIC16CR54 DEVICES

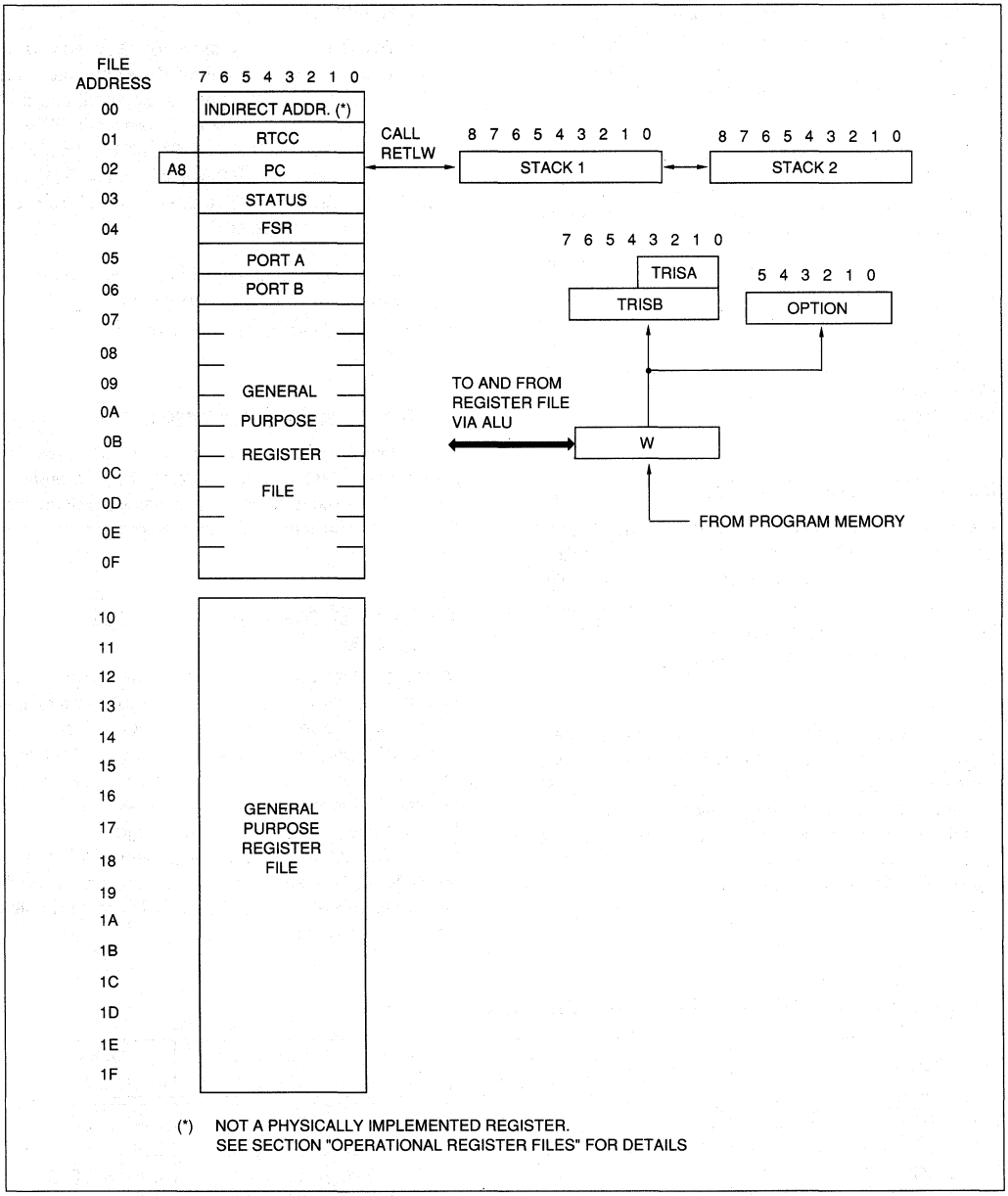
Part #	ROM	RAM*	I/O**	Supply Voltage	Osc. Type	Frequency Range***	Package Options
PIC16CR54RC	512 x 12	32 x 8	13	2.5 - 6.0 V	RC	DC - 4 MHz	DIP-18, SOIC-18
PIC16CR54XT	512 x 12	32 x 8	13	2.5 - 6.0 V	XTAL, Ext.	0.1 - 4 MHz	DIP-18, SOIC-18
PIC16CR54HS	512 x 12	32 x 8	13	4.5 - 5.5 V	XTAL, Ext.	4 - 20 MHz	DIP-18, SOIC-18
PIC16CR54LP	512 x 12	32 x 8	13	2.0 - 6.0 V	XTAL, Ext.	DC - 200 KHz	DIP-18, SOIC-18

* Including special function registers.

** Including RTCC pin.

*** All devices operate down to DC when external clock is applied.

FIGURE 2.3.1 - PIC16CR54 DATA MEMORY MAP



(*) NOT A PHYSICALLY IMPLEMENTED REGISTER.
SEE SECTION "OPERATIONAL REGISTER FILES" FOR DETAILS

4.0 OPERATIONAL REGISTER FILES

4.1 f0 Indirect Data Addressing

This is not a physically implemented register. Addressing f0 calls for the contents of the File Select Register to be used to select a file register. f0 is useful as an indirect address pointer. For example, in the instruction ADDWF f0, W will add the contents of the register pointed to by the FSR (f4) to the content of the W Register and place the result in W.

If f0 itself is read through indirect addressing (i.e. FSR = 0h), then 00h is read. If f0 is written to via indirect addressing, the result will be a NOP.

4.2 f1 Real Time Clock/Counter Register (RTCC)

This register can be loaded and read by the program as any other register. In addition, its contents can be incremented by an external signal edge applied to the RTCC pin, or by the internal instruction cycle clock (CLKOUT=fosc/4). Figure 4.2.1 is a simplified block diagram of RTCC.

An 8-bit prescaler can be assigned to the RTCC by writing the proper values to the PSA bit and the PS bits in the OPTION register. OPTION register is a special register (not mapped in data memory) addressable using the 'OPTION' instruction. See section 7.4 for details. If the prescaler is assigned to the RTCC, instructions writing to f1 (e.g. CLRF 1, or BSF1,5, ...etc.) clear the prescaler.

The bit "RTS" (RTCC signal Source) in the OPTION register determines, if f1 is incremented internally or externally.

RTS=1: The clock source for the RTCC or the prescaler, if assigned to it, is the signal on the RTCC pin. Bit 4 of the OPTION register (RTE) determines, if an increment occurs on the falling (RTE=1) or rising (RTE=0) edge of the signal presented to the RTCC pin.

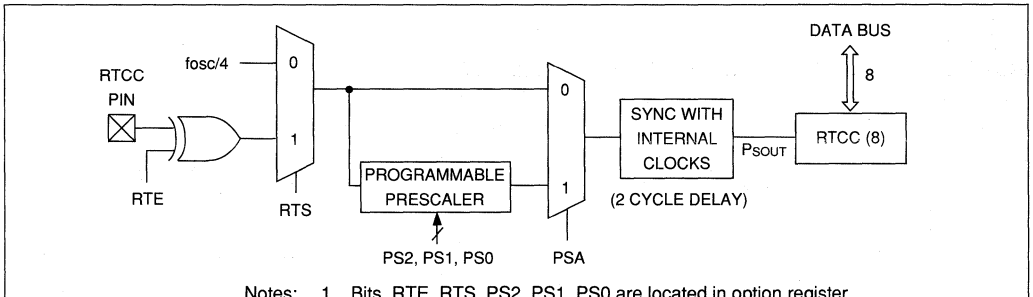
RTS=0: The RTCC register or its prescaler, respectively, will be incremented with the internal instruction clock (= Fosc/4). The "RTE" bit in the OPTION register and the RTCC pin are "don't care" in this case. However, the RTCC pin must be tied to VDD or VSS, whatever is convenient, to prevent unintended entering of test modes and to reduce the current consumption in low power applications.

As long as clocks are applied to the RTCC (from internal or external source, with or without prescaler), f1 keeps incrementing and just rolls over when the value "FFh" is reached. All increment pulses for f1 are delayed by two instruction cycles. After writing to f1, for example, no increment takes place for the following two instruction cycles. This is independent if internal or external clock source is selected. If a prescaler is assigned to the RTCC, the output of the prescaler will be delayed by two cycles before f1 is incremented. This is true for instructions that either write to or read-modify-write RTCC (e.g. MOVF f1, CLRF f1). For applications where RTCC needs to be tested for zero without affecting its count, use of MOVF f1, W instruction is recommended. Timing diagrams in Figure 4.2.2 show RTCC read, write and increment timing.

4.2.1 USING RTCC WITH EXTERNAL CLOCK

When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also there is some delay from the occurance of the

FIGURE 4.2.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in option register.
2. The prescaler is shared with Watchdog Timer (see Figure 9.0.1).

external clock edge to the actual incrementing of RTCC. Referring to Figure 4.2.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 4.2.2.1) is the same as RTCC clock input and therefore the requirements are:

TRTH = RTCC high time ≥ 2tosc + 20 ns
TRTL = RTCC low time ≥ 2tosc + 20 ns

When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.
Then: PSOUT high time = PSOUT low time = $\frac{N.T_{RT}}{2}$
where TRT = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore $\frac{N.T_{RT}}{2}$ ≥ 2 tosc + 20 ns, or TRT ≥ $\frac{4\ tosc + 40\ ns}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10 ns is required. In summary, the RTCC input requirements are:

TRT = RTCC period ≥ (4 tosc + 40 ns)/N
TRTH = RTCC high time ≥ 10 ns
TRTL = RTCC low time ≥ 10 ns

4.2.2 DELAY FROM EXTERNAL CLOCK EDGE

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to Figure 4.2.2.1, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±500 ns @ 8 MHz).

4.3 f2 Program Counter

The program counter generates the addresses for on-chip ROM containing the program instruction words (Figure 4.3.1).

The program counter is set to all "1"s upon a RESET condition. During program execution it is auto incremented with each instruction unless the result of that instruction changes the PC itself:

a) "GOTO" instructions allow the direct loading of the lower 9 program counter bits (PC <8:0>).
b) "CALL" instructions load the lower 8-bit of the PC directly while the ninth bit is cleared to "0". The PC value, incremented by one, will be pushed into the stack.
c) "RETLW" instructions load the program counter with the top of stack contents.

FIGURE 4.2.2A - RTCC TIMING: INT CLOCK/NO PRESCALE

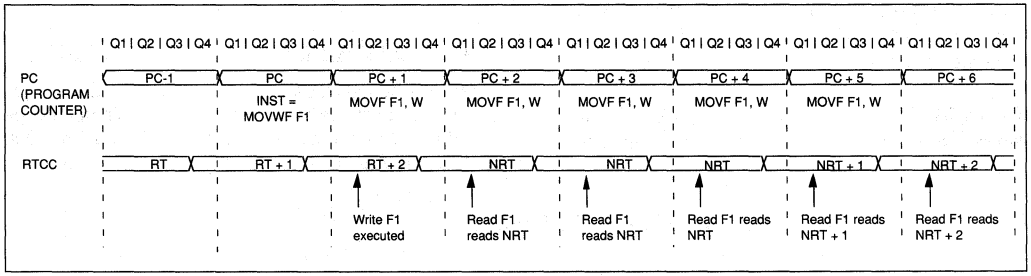
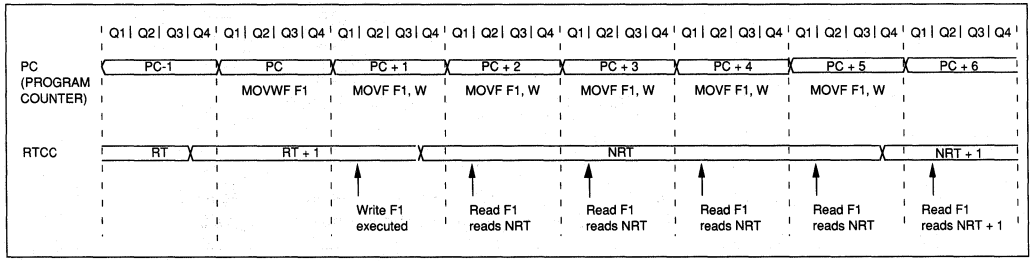


FIGURE 4.2.2B - RTCC TIMING: INT CLOCK/PRESCALE 1:2



d) If PC is the destination in any instruction (e.g. MOVWF 2, ADDWF 2, or BSF 2,5) then the computed 8-bit result will be loaded into the low 8-bits of program counter. The ninth bit of PC will be cleared.

It should be noted that because bit 8 (ninth bit) of PC is cleared in CALL instruction or any instruction which writes to the PC (e.g. MOVWF 2), all subroutine calls or computed jumps are limited to the first 256 locations of the program memory page (512 words long).

4.4 STACK

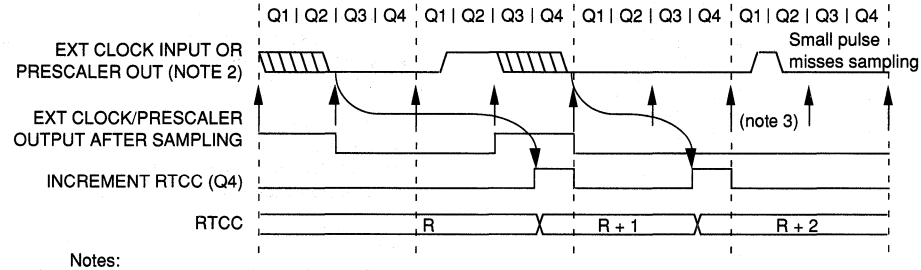
The PIC16CR54 has a two level (9 bit wide) hardware push/pop stack (Figure 4.3.1).

CALL instructions push the current program counter value, incremented by "1", into stack level 1. Stack level 1 is automatically pushed to level 2. If more than 2 subsequent "CALL"s are executed, only the most recent two return addresses are stored.

RETLW instructions load the contents of stack level 1 into the program counter while stack level 2 gets copied into level 1. If more than 2 subsequent "RETLW"s are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the RETLW instruction. This is particularly useful for the implementation of "data" tables within the program memory.

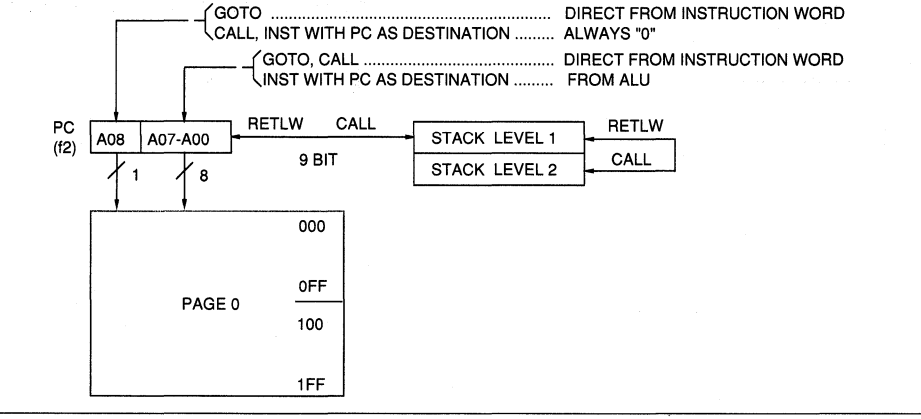
1

FIGURE 4.2.2.1 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:
1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

FIGURE 4.3.1 - PROGRAM MEMORY ORGANIZATION



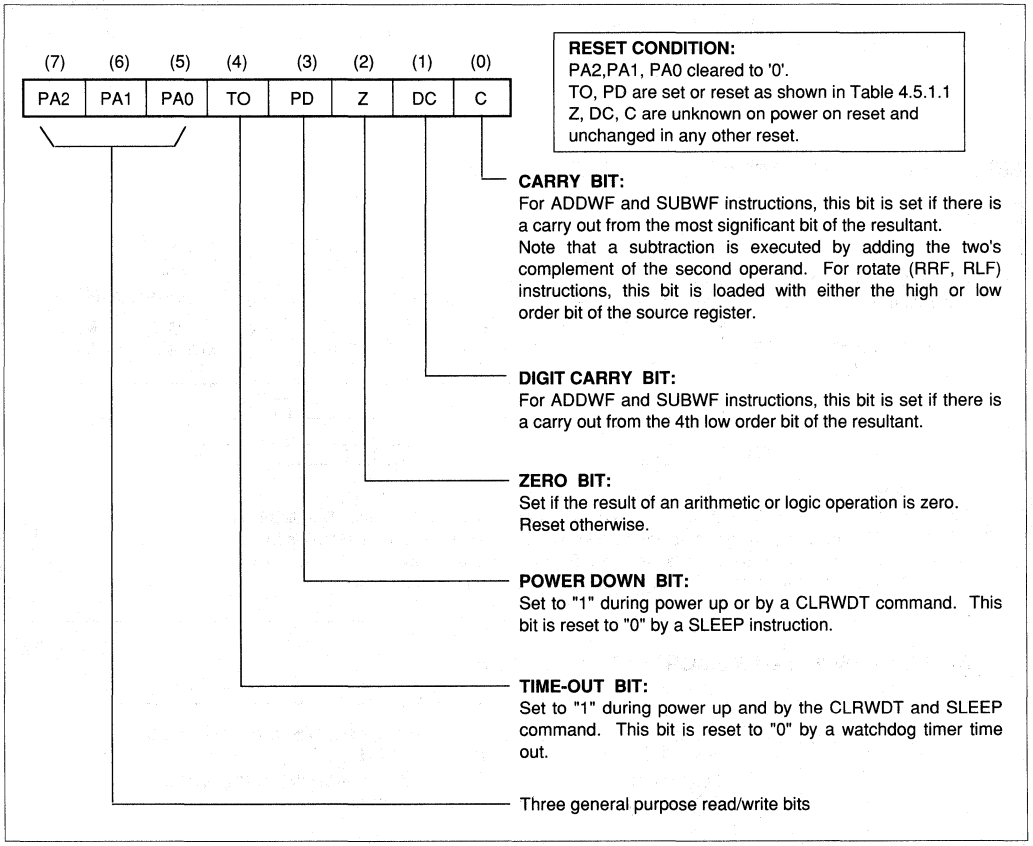
4.5 f3 Status Word Register

This register contains the arithmetic status of the ALU, and the RESET status.

The status register (f3) can be destination for any instruction like any other register. However, the status bits are set after the following write. Furthermore, TO and PD bits are not writable. Therefore, the result of an instruction with status register as destination may be different than intended. For example, CLRF f3 will clear all bits except for TO and PD and then set the Z bit and leave status register as 000XX100 (where X = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the status registers because these instructions do not affect any status bit.

FIGURE 4.5.1 - STATUS WORD REGISTER f3



4.5.1 TIME OUT AND POWER DOWN STATUS BITS (TO, PD)

The "TO" and "PD" bits in the status register f3 can be tested to determine if a RESET condition has been caused by a watchdog timer time-out, a power-up condition, or a wake-up from SLEEP by the watchdog timer or MCLR pin.
These status bits are only affected by events listed in Table 4.5.1.1.

TABLE 4.5.1.1 - EVENTS AFFECTING PD/TO STATUS BITS

Event	TO	PD	Remarks
Power-up	1	1	
WDT Timeout	0	X	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Note: A WDT timeout will occur regardless of the status of the TO bit. A SLEEP instruction will be executed, regardless of the status of the PD bit. Table 4.5.1.2 reflects the status of PD and TO after the corresponding event.

TABLE 4.5.1.2 - PD/TO STATUS AFTER RESET

TO	PD	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	MCLR wake-up from SLEEP
1	1	Power-up
X	X	= Low pulse on MCLR input

Note: The PD and TO bit maintain their status (X) until an event of Table 4.5.1.1 occurs. A low-pulse on the MCLR input does not change the PD and TO status bits.

4.6 f4 File Select Register (FSR)

Bits 0-4 select one of the 32 available file registers in the indirect addressing mode (that is, calling for file f0 in any of the file oriented instructions).
Bits 5-7 of the FSR are read-only and are always read as "one"s.
If no indirect addressing is used, the FSR can be used as a 5-bit wide general purpose register.

5.0 I/O REGISTERS (PORTS)

The I/O registers can be written and read under program control like any other register of the register file. However, "read" instructions (e.g. MOVF 6,W) always read the I/O pins, regardless if a pin is defined as "input" or "output." Upon a RESET condition, all I/O ports are defined as "input" (= high impedance mode) as the I/O control registers (TRISA, TRISB) are all set to "ones."

The execution of a "TRIS f" instruction with corresponding "zeros" in the W-register is necessary to define any of the I/O pins as output.

5.1 f5 (Port A)

4-bit I/O register. Low order 4 bits only are used (RA0 - RA3). Bit 4 - 7 are unimplemented and read as "zeros."

5.2 f6 (Port B)

8-bit I/O register.

5.3 I/O Interfacing

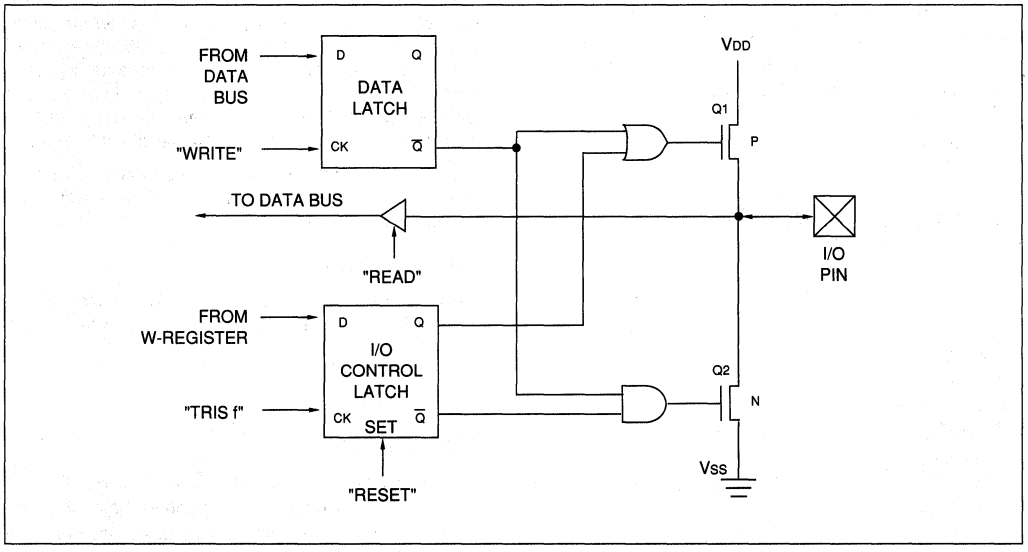
The equivalent circuit for an I/O port bit is shown in Figure 5.3.1. All ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g. MOVF 6, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB) must be set to zero. For use as an input, the corresponding TRIS bit must be "one". Any I/O pin can be programmed individually as input or output.

5.4 I/O Programming Considerations

5.4.1 BIDIRECTIONAL I/O PORTS

a) Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of f6 (Port B) will cause all eight bits of f6 to be read into the CPU. Then the BSF operation takes place on bit 5 and f6 is re-output to the output latches. If another bit of f6 is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

FIGURE 5.3.1 - EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



b) A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

For "wired-or" outputs (assuming negative logic), it is recommended to use external pull-up resistors on the corresponding pins. The pin should be left in high-impedance mode, unless a "0" has to be output. Thus, external devices can drive this pin "0" as well. "Wired-and" outputs can be realized in the same way, but with external pull-down resistors and only actively driving the "1" level from the PIC. The resistor values are user selectable, but should not force output currents above the specified limits (see DC Characteristics).

5.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

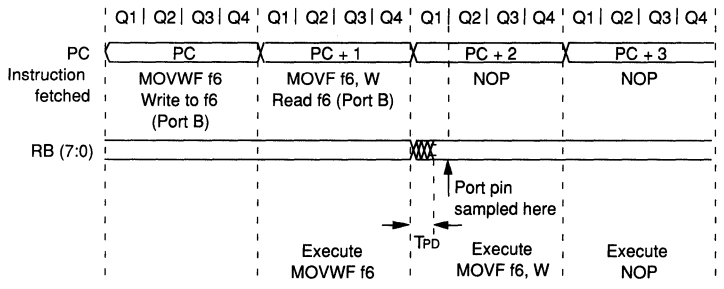
The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see figure 5.4.2.1).

Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

5.4.3 OPERATION IN NOISY ENVIRONMENT

In noisy application environments, such as keyboards which are exposed to ESD (Electro Static Discharge), register contents can get corrupted due to noise spikes. The on-chip watchdog timer will take care of all situations involving program sequence "lock-ups." However, if an I/O control register gets corrupted, the program sequence may still be executed properly although an input pin may have switched unintentionally to an output. In this case, the program would always read the same value on this pin. This may result, for example, in a keyboard "lock-up" situation without leading to a watchdog timer timeout. Thus, it is recommended that all I/O pins be redefined at regular time intervals (inputs as well as outputs). The optimal strategy is to update the I/O control register every time before reading input data or writing output data.

FIGURE 5.4.2.1 - I/O PORT READ/WRITE TIMING



Note:

This example shows write to port B followed by a read from port B. Note that the data setup time = (0.25 TCY - TPD) where TCY = instruction cycle. Therefore, at higher clock frequencies, write followed by a read may be problematic.

6.0 GENERAL PURPOSE REGISTERS

f07h - f1Fh: are general purpose register files.

7.0 SPECIAL PURPOSE REGISTERS

7.1 W Working Register

Holds second operand in two operand instructions and/or supports the internal data transfer.

7.2 TRISA I/O Control Register For Port A (f5)

Only bits 0 - 3 are available. The corresponding I/O port (f5) is only 4-bit wide.

7.3 TRISB I/O Control Register For Port B (f6)

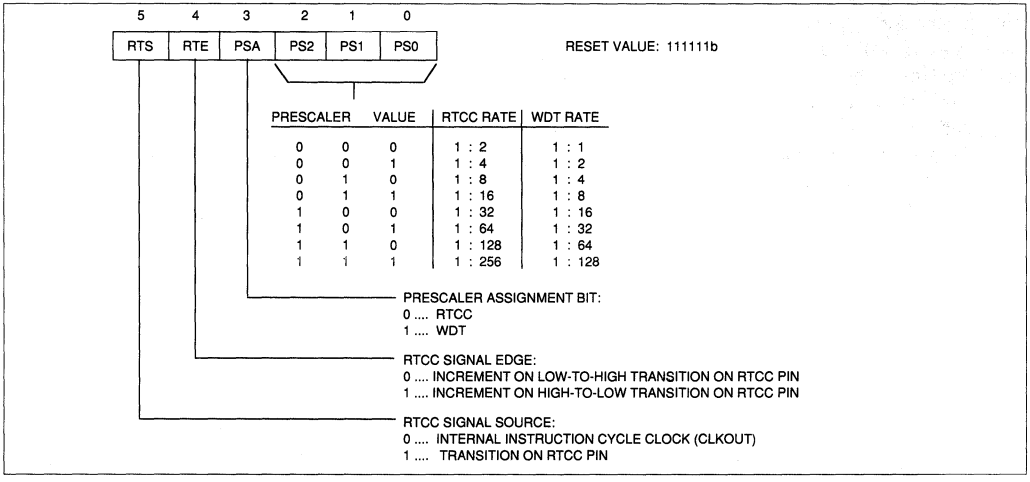
The I/O control registers will be loaded with the content of the W register by executing of the TRIS f instruction. A "1" in the I/O control register puts the corresponding I/O pin into a high impedance mode. A "0" puts the contents of file register f5 or f6, respectively, out on the selected I/O pins.

These registers are "write-only" and are set to all "ones" upon a RESET condition.

7.4 OPTION Prescaler/RTCC Option Register

Defines prescaler assignment (RTCC or WDT), prescaler value, signal source and signal edge for the RTCC. The OPTION register is "write-only" and is 6 bit wide. By executing the "OPTION" instruction, the contents of the "W" register will be transferred to the option register. Upon a RESET condition, the option register is set to all "ones."

FIGURE 7.4.1 - OPTION REGISTER



8.0 RESET CONDITION

A RESET condition can be caused by applying power to the chip (power-up), pulling the $\overline{MCLR}$ input "low", or by a Watchdog timer timeout. The device will stay in RESET as long as the oscillator start-up timer (OST) is active or the $\overline{MCLR}$ input is "low."
The oscillator start-up timer is activated as soon as $\overline{MCLR}$ input is sensed to be high. This implies that in case of power on reset with $\overline{MCLR}$ tied to V_{DD} the OST starts from power-up. In case of WDT time-out, it will start at the end of the time-out (since $\overline{MCLR}$ is high). In case of $\overline{MCLR}$ reset, the OST will start when $\overline{MCLR}$ goes high. The nominal OST time-out period is 18 ms. See section 13.0 for detailed information on OST and power on reset.

During a RESET condition the state of the PIC is defined as :

- The oscillator is running, or will be started (power-up or wake-up from SLEEP).
- All I/O port pins (RA0 - RA3, RB0 - RB7) are put into the high-impedance state by setting the "TRIS" registers to all "ones" (= input mode).
- The Program Counter is set to all "ones" (1FFh).
- The OPTION register is set to all "ones".
- The Watchdog Timer and its prescaler are cleared.
- The upper three bits (page select bits) in the Status Register (f3) are cleared to "zero."
- "RC" devices only: The "CLKOUT" signal on the OSC2 pin is held at a"low" level.

9.0 PRESCALER

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the watchdog timer, respectively (Figure 9.0.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the watchdog timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the watchdog timer, and vice versa.
The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio.

When assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF 1, MOVWF 1, BSF 1,x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the watchdog timer.

9.1 Switching Prescaler Assignment

CHANGING PRESCALER FROM RTCC TO WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'  ; Select internal clock and select new
2. OPTION              ; prescaler value. If new prescale value
                       ; is = '000' or '001', then select any other
                       ; prescale value temporarily.
3. CLRF 1              ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'  ; Select WDT, do not change prescale
                       ; value.
5. OPTION              ;
6. CLRWDT              ; Clears WDT and prescaler.
7. MOVLW B'xxxx1xxx'   ; Select new prescale value.
8. OPTION              ;
```

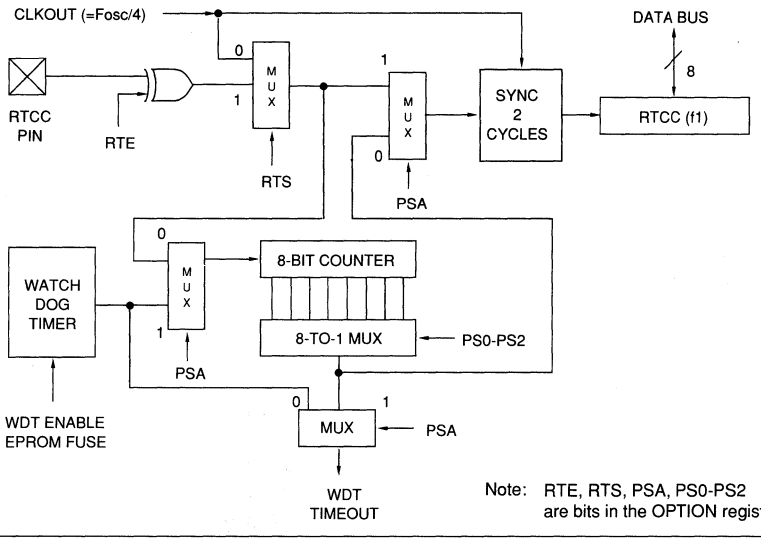
Step 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000'or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT              ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'  ; Select RTCC, new prescale value
                       ; and clock source
3. OPTION              ;
```

FIGURE 9.0.1 - BLOCK DIAGRAM RTCC/WDT PRESCALER



10.0 BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP CODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC instruction set summary in Table 10.0.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.
For literal and control operations, "k" represents an eight or nine bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 10.0.1

Note 1: The 9th bit of the program counter will be forced to a "zero" by any instruction that writes to the PC (f2) except for GOTO (e.g. CALL, MOVWF 2 etc.). See section 4.3 for details.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF 6,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as input, and it is driven low by an external device, the data latch will be written back with a '0'.

Note 3: The instruction "TRIS f", where f = 5 or 6 causes the contents of the W register to be written to the tristate latches of the specified file (port). A "one" forces the pin to a high impedance state and disables the output buffers.

Note 4: If this instruction is executed on file register f1 (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

TABLE 10.0.1 - INSTRUCTION SET SUMMARY

BYTE -ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4 - 0)
OPCODE	d	f(FILE #)

d = 0 for destination W
d = 1 for destination f

Instruction-Binary	(Hex)	Name	Mnemonic, Operands		Operation	Status Affected	Notes
0000 0000 0000	000	No Operation	**NOP**	-	-	None	
0000 001f ffff	02f	Move W to f	**MOVWF**	f	W → f	None	1,4
0000 0100 0000	040	Clear W	**CLRW**	-	0 → W	Z	
0000 011f ffff	06f	Clear f	**CLRF**	f	0 → f	Z	4
0000 10df ffff	08f	Subtract W from f	**SUBWF**	f, d	f - W → d [f + $\overline{W}$ + 1 → d]	C, DC, Z	1,2,4
0000 11df ffff	0Cf	Decrement f	**DECF**	f, d	f -1 → d	Z	2,4
0001 00df ffff	10f	Inclusive OR W and f	**IORWF**	f, d	W v f → d	Z	2,4
0001 01df ffff	14f	AND W and f	**ANDWF**	f, d	W & f → d	Z	2,4
0001 10df ffff	18f	Exclusive OR W and f	**XORWF**	f, d	W ⊕ f → d	Z	2,4
0001 11df ffff	1Cf	Add W and f	**ADDWF**	f, d	W + f → d	C, DC, Z	1,2,4
0010 00df ffff	20f	Move f	**MOVF**	f, d	f → d	Z	2,4
0010 01df ffff	24f	Complement f	**COMF**	f, d	$\bar{f}$ → d	Z	2,4
0010 10df ffff	28f	Increment f	**INCF**	f, d	f + 1 → d	Z	2,4
0010 11df ffff	2Cf	Decrement f,Skip if Zero	**DECFSZ**	f, d	f - 1 → d, skip if zero	None	2,4
0011 00df ffff	30f	Rotate right f	**RRF**	f, d	f(n) → d(n-1), C → d(7), f(0) → C	C	2,4
0011 01df ffff	34f	Rotate left f	**RLF**	f, d	f(n) → d(n+1), C → d(0), f(7) → C	C	2,4
0011 10df ffff	38f	Swap halves f	**SWAPF**	f, d	f(0-3) ↔ f(4-7) → d	None	2,4
0011 11df ffff	3Cf	Increment f,Skip if zero	**INCFSZ**	f, d	f + 1 → d, skip if zero	None	2,4

BIT- ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4 - 0)
OPCODE	b(BIT #)	f(FILE #)

Instruction-Binary	(Hex)	Name	Mnemonic,Operands		Operation	Status affected	Notes
0100 bbbf ffff	4bf	Bit Clear f	**BCF**	f, b	0 → f(b)	None	2,4
0101 bbbf ffff	5bf	Bit Set f	**BSF**	f, b	1 → f(b)	None	2,4
0110 bbbf ffff	6bf	Bit Test f,Skip if Clear	**BTFSC**	f, b	Test bit (b) in file (f): Skip if clear	None	
0111 bbbf ffff	7bf	Bit Test f, Skip if Set	**BTFSS**	f, b	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS

(11-8)	(7 - 0)
OPCODE	k (LITERAL)

Instruction-Binary	(Hex)	Name	Mnemonic,Operands		Operation	Status affected	Notes
0000 0000 0010	002	Load OPTION register	**OPTION**	-	W → OPTION register	None	
0000 0000 0011	003	Go into standby mode	**SLEEP**	-	0 → WDT, stop oscillator	TO, PD	
0000 0000 0100	004	Clear Watchdog timer	**CLRWDT**	-	0 → WDT (and prescaler, if assigned)	TO, PD	
0000 0000 0fff	00f	Tristate port f	**TRIS**	f	W→ I/O control register f	None	3
1000 kkkk kkkk	8kk	Return,place Literal in W	**RETLW**	k	k → W, Stack → PC	None	
1001 kkkk kkkk	9kk	Call subroutine	**CALL**	k	PC + 1 → Stack, k → PC	None	1
101k kkkk kkkk	Akk	Go To address (k is 9 bit)	**GOTO**	k	k → PC (9 bits)	None	
1100 kkkk kkkk	Ckk	Move Literal to W	**MOVLW**	k	k → W	None	
1101 kkkk kkkk	Dkk	Incl. OR Literal and W	**IORLW**	k	k v W → W	Z	
1110 kkkk kkkk	Ekk	AND Literal and W	**ANDLW**	k	k & W→ W	Z	
1111 kkkk kkkk	Fkk	Excl. OR Literal and W	**XORLW**	k	k ⊕ W → W	Z	

Notes: See previous page

11.0 WATCHDOG TIMER (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming a "zero" into a special ROM fuse which is not part of the normal program memory ROM. This masking bit, which is part of a configuration word can be specified by the customer.

11.1 WDT Period

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out period varies with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit "TO" in file register f3 will be cleared upon a watchdog timer timeout.

The WDT period is a function of the supply voltage, operating temperature, and will also vary from unit to unit due to variations in the manufacturing process. Please refer to graphs in section 18.0 and DC specs for more details.

11.2 WDT Programming Considerations:

In a noisy application environment the OPTION register can get corrupted. The OPTION register should be updated at regular intervals.

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

12.0 OSCILLATOR CIRCUITS

12.1 Oscillator Types

The PIC16CR54 series is available with 4 different oscillator options. Two bits in the configuration word select one of these four modes. The customer specifies the desired oscillator type along with the ROM pattern. The parts are tested for the specific oscillator type.

12.2 Crystal Oscillator

The PIC16CR54-XT, -HS, or LP needs a crystal or ceramic resonator connected to the OSC1 and OSC2 pins to establish oscillation (Figure 12.2.1). Note that the series resistor Rs is only required for the "HS" oscillator.

12.3 RC Oscillator

For timing insensitive applications the "RC" oscillator option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation to due tolerance of external R and C components used. Figure 12.3.1 shows how the R/C combination is connected to the PIC16CR54. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 5 kOhm and 100 kOhm.

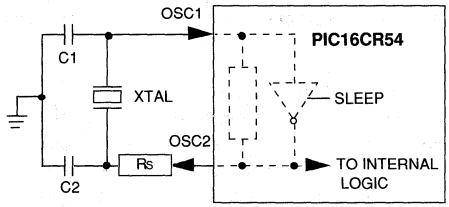
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See tables in section 18.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See graphs and tables in section 18.0 for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 2.2.1 for timing).

FIGURE 12.2.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP TYPES ONLY)



Rs is recommended for "HS" devices(100Ω < Rs < 1KΩ). RS may also be needed in XT mode for AT strip-out crystals to avoid overdriving. See Tables 12.2.1 and 12.2.2 for recommended values of C1, C2 and RS.

TABLE 12.2.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator frequencyf	Capacitor Range
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF
	20 MHz	0 - 20 pF

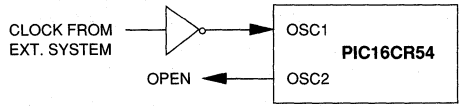
Higher capacitance increases stability of oscillation but also increases start-up time.

TABLE 12.2.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF
XT	200 KHz	15 - 50 pF	15 - 50 pF
	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Higher capacitance increases stability of oscillator but also increases start-up time. These values are for design guidance only. RS may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 12.2.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP TYPES ONLY)



Note: Load on OSC2 must not exceed 15 pF for external clock operation.

FIGURE 12.3.1 - RC OSCILLATOR (RC TYPE ONLY)

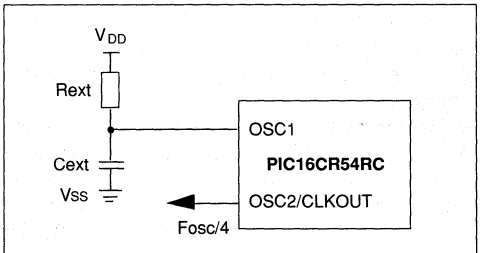
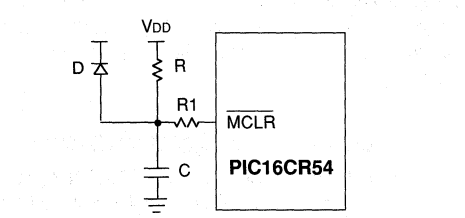


FIGURE 13.1.1 - EXTERNAL POWER ON RESET CIRCUIT



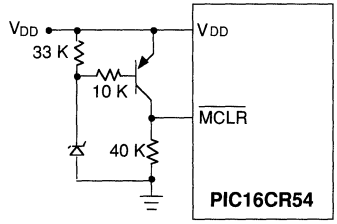
Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow or if a low frequency crystal oscillator is being used that need a long start-up time. The diode D helps discharge the capacitor quickly when VDD powers down.

2. R < 40 KΩ must be observed to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on MCLR pin is 5 μA). A larger than 0.2 V drop across R may cause a VIH level violation on MCLR pin.

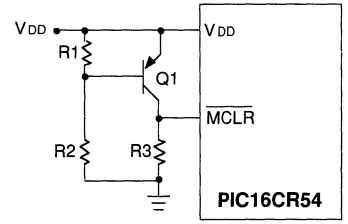
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

FIGURE 13.1.2 - BROWN OUT PROTECTION CIRCUIT



Notes:
1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 13.1.3 - BROWN OUT PROTECTION CIRCUIT



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$VDD \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

13.0 OSCILLATOR START-UP TIMER (OST)

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. An on-chip oscillator start-up timer is provided which keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR pin has reached a logic high (VIHMC) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.
The OST will also be triggered upon a watchdog timer timeout. This is particularly important for applications using the WDT to awake the PIC16CR54 from SLEEP mode automatically.
The OST is not adequate for low frequency crystals which require much longer than 18 ms to start up and stabilize.

13.1 Power On Reset (POR)

The PIC16CR54 incorporates an on chip Power On Reset (POR) circuitry which provides internal chip reset for most power-up situations. To use this feature the user merely needs to tie MCLR pin to VDD. A simplified block diagram of the on-chip power on reset circuit is shown in Figure 13.1.4. The power on reset circuit and the oscillator start-up timer circuit are closely related. On power-up the reset latch is set and the start-up timer (see Figure 13.1.4) is reset. The start-up timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will reset the reset-latch and thus end the on-chip reset signal.

Figures 13.1.5 and 13.1.6 are two power-up situations with relatively fast rise time on VDD. In Figure 13.1.5, VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset tOST ms after MCLR goes high. In Figure 13.1.6, the on chip power-on reset feature is being utilized (MCLR and VDD are tied together). The VDD is stable before the startup timer times out and there is no problem in getting a proper reset. Figure 13.1.7 depicts a potentially problematic situation where VDD rises too slowly. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is therefore not guaranteed to function correctly.

To summarize, the on chip power-on reset is guaranteed to work if the rate of rise of VDD is no slower than 0.05 V/ms. It is also necessary that the VDD starts from 0V. The on chip power on reset is also not adequate for low frequency crystals which require much longer than 18 ms to start up and stabilize. For such situations, we recommend that external RC circuits are used for longer power on reset.

FIGURE 13.1.4 - SIMPLIFIED POWER ON RESET BLOCK DIAGRAM

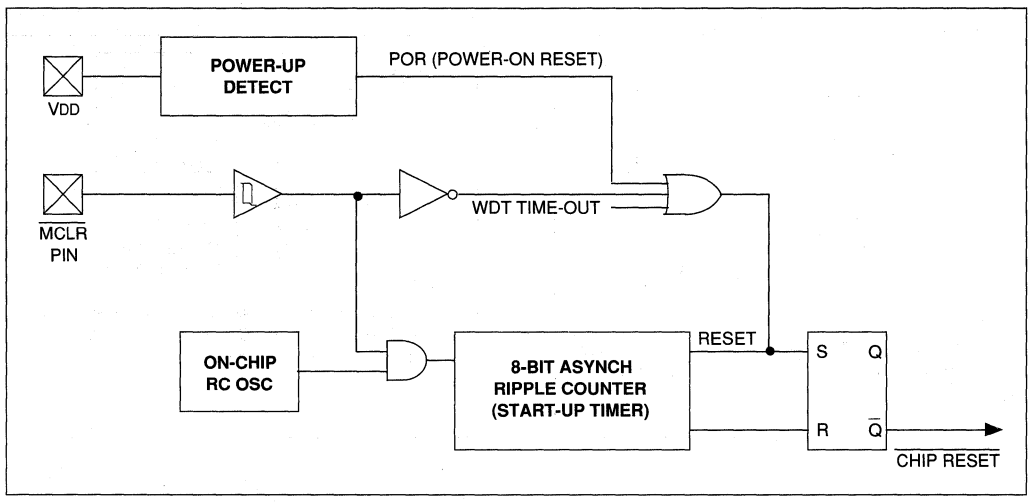


FIGURE 13.1.5 - USING EXTERNAL RESET INPUT

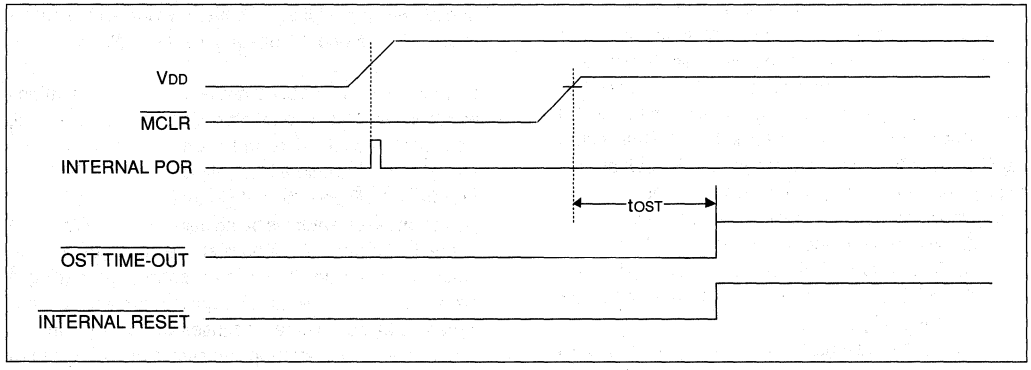


FIGURE 13.1.6 - USING ON-CHIP POR (FAST VDD RISE TIME)

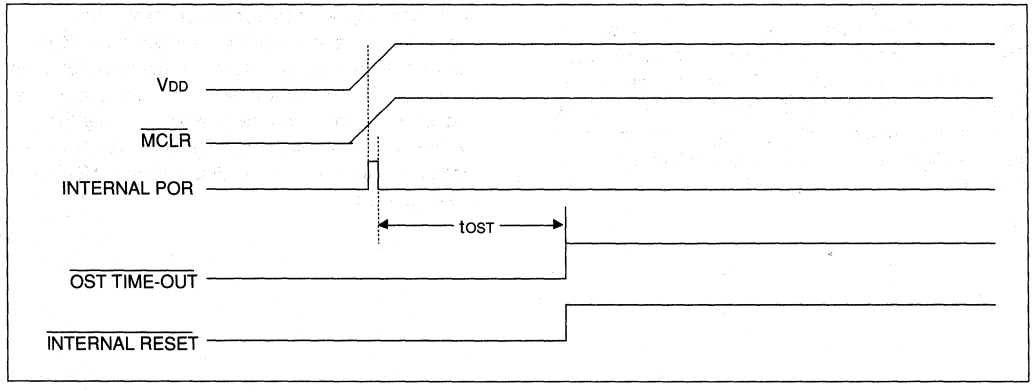
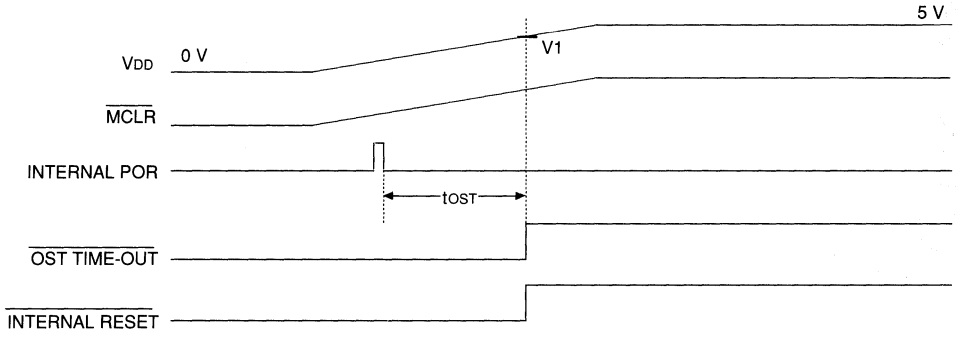


FIGURE 13.1.7 - USING ON-CHIP POR (SLOW VDD RISE TIME)



When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1≥ VDDMIN.

14.0 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the watchdog timer will be cleared but keeps running, the bit "PD" in the status register (f3) is cleared, the "TO" bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low or hi-impedence).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC pin should also be at VDD or VSS for lowest current consumption.

The MCLR pin must be at VIHMC.

14.1 Wake-Up

The device can be awakened by a watchdog timer timeout (if it is enabled) or an externally applied "low" pulse at the MCLR pin. In both cases the PIC will stay in RESET mode for one oscillator start-up timer period (triggered from rising edge on MCLR or WDT timeout) before normal program execution resumes.

The "PD" bit in the STATUS register, which is set to one during power on , but cleared by the "SLEEP" command, can be used to determine if the processor was powered up or awakened from the power down mode (Table 4.5.1.2). The TO bit in the Status register can be used to determine, if the "wake up" was caused by an external MCLR signal or a watchdog timer time out.

NOTE: Some applications may require external R/C networks on the MCLR pin in order to allow for oscillator startup times longer than one OST period. In this case, a WDT wake up from power down mode is not recommended, because a RESET generated by a WDT time out does not discharge the external capacitor, and the PIC will be in RESET only for the oscillator start-up timer period.

15.0 CONFIGURATION FUSES

The configuration word consists of four ROM fuses which are not part of the normal ROM program storage. Two are for the selection of the oscillator type, one is the watchdog timer enable fuse, and one is the code protection fuse.

The customer makes the selection for these and the parts are tested accordingly. The packages are marked with the suffixes "XT", "RC", "HS" or "LP" following the part number to identify the oscillator type and operating range.

15.1 Customer ID Code

The PIC16CR54 has 4 special ROM locations which are not part of the normal program memory. These locations are available to the user to store an Identifier (ID) code, checksum, or other informative data. They cannot be accessed during normal program execution but can be read out using any programmer that supports the PIC16C5X such as PICPRO or PICPRO II.

15.2 Code Protection

The code in the ROM can be protected by selecting the code protection fuse to be "0".
When code protected, the contents of the program ROM cannot be read out in a way that the program code can be reconstructed. The factory can verify every bit in a code protected ROM through a special ROM-verify test mode. In this test mode data is presented to the chip for every ROM location and a pass/fail bit at the end of the sequence indicates if the ROM matched the externally supplied pattern sequence. This mode does not output the ROM pattern and therefore does not compromise code security.

Another way to verify a code protected ROM without supplying the actual code is as follows:

When code protected, verifying any program memory location will read a scrambled output which looks like "00000000XXXX" (binary) where X is 1 or 0. To verify a code protected device, follow this procedure:

a. First, read in a code-protected device known to be good into a file. The data will look scrambled.
b. Verify any code-protected PIC against this file.

16.0 ELECTRICAL CHARACTERISTICS

16.1 Absolute Maximum Ratings*

Ambient temperature under bias .....-55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to VSS
(except VDD and MCLR) .....-0.6V to VDD +0.6V
Voltage on VDD with respect to VSS .....0 to +7.5 V
Voltage on MCLR with respect to VSS
(Note 2) .....0 to +14 V
Total power Dissipation (Note 1) .....800 mW
Max. Current out of VSS pin .....150 mA
Max. Current into VDD pin .....50 mA
Max. Current into an input pin .....±500 µA
Max. Output Current sinked by any I/O pin.....25 mA
Max. Output Current sourced by any I/O pin .....20 mA
Max. Output Current sourced by a single
I/O port (Port A or B) .....40 mA
Max. Output Current sinked by a single
I/O port (Port A or B) 50mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = VDD \times \{IDD - \sum Ioh\} + \sum\{(VDD-Voh) \times Ioh\} + \sum(Vol \times Iol)$
2. Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to VSS.

16.2 Pin Descriptions

Name	Function	Observation
RA0 - RA3	I/O PORT A	4 input/output lines.
RB0 - RB7	I/O PORT B	8 input/output lines.
RTCC	Real Time Clock/Counter	Schmitt Trigger Input. Clock input to RTCC register. Must be tied to VSS or VDD if not in use to avoid unintended entering of test modes and to reduce current consumption.
MCLR	Master Clear	Schmitt Trigger Input. A "Low" voltage on this input generates a RESET condition for the PIC16CR54 microcontroller. A rising voltage triggers the on-chip oscillator start-up timer which keeps the chip in RESET mode for about 18ms. This input must be tied directly, or via a pull-up resistor, to VDD.
OSC1	Oscillator (input)	"XT", "HS" and "LP" devices: Input terminal for crystal, ceramic resonator, or external clock generator. "RC" devices : Driver terminal for external RC combination to establish oscillation.
OSC2/CLKOUT	Oscillator (output)	For "XT", "HS" and "LP" devices: Output terminal for crystal and ceramic resonator. Do not connect any other load to this output. Leave open if external clock generator is used. For "RC" devices : A "CLKOUT" signal with a frequency of 1/4 Fosc1 is put out on this pin.
VDD	Power supply	
VSS	Ground	
N/C	No (internal) Connection	

16.3 DC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (COMMERCIAL) PIC16CR54-RC, XT, HS, LP (INDUSTRIAL)

DC CHARACTERISTICS, POWER SUPPLY PINS

Standard Operating Conditions

Operating temperature -40 ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Supply Voltage						
PIC16CR54-XT, RC	VDD	2.5		6.25	V	Fosc = DC to 4 MHz
PIC16CR54-HS	VDDhs	4.5		5.5	V	Fosc = DC to 20 MHz
PIC16CR54-LP	VDDlp	2.0		6.25	V	Fosc = DC to 200 KHz
RAM Data Retention Voltage (Note 3)	VDR		1.5		V	Device in SLEEP mode
VDD starting voltage to guarantee power on reset	VPOR		VSS		V	See section 13.1 for details on power-on-reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 13.1 for details on power-on-reset
Supply Current (Note 2)						
PIC16CR54-XT, RC (Note 5)	IDD1		2.0	3.6	mA	Fosc = 4 MHz, VDD = 6.0V
	IDD2		0.8	1.8	mA	Fosc = 4 MHz, VDD = 3.0V
	IDD3		90	350	µA	Fosc = 200 KHz, VDD = 2.5V
PIC16CR54-HS	IDDhs1		3.8	10	mA	Fosc = 8 MHz, VDD = 5.5V
	IDDhs2		9.0	20.0	mA	Fosc = 20 MHz, VDD = 5.5V
PIC16CR54-LP	IDDlp1		10.0	20.0	µA	Fosc = 32 KHz, VDD = 2.0V
	IDDlp2			70.0	µA	Fosc = 32 KHz, VDD = 6.0V
Power Down Current Commercial (Note 4)						
PIC16CR54	IPD1		1	6	µA	VDD = 2.5V, WDT disabled
	IPD2		2	8*	µA	VDD = 4.0V, WDT disabled
	IPD3		3	15	µA	VDD = 6.0V, WDT disabled
	IPD4		5	25	µA	VDD = 6.0V, WDT enabled
Power Down Current Industrial (Note 4)						
PIC16CR54	IPD1		1	8	µA	VDD = 2.5V, WDT disabled
	IPD2		2	10*	µA	VDD = 4.0V, WDT disabled
	IPD3		3	20*	µA	VDD = 4.0V, WDT enabled
	IPD4		3	18	µA	VDD = 6.0V, WDT disabled
	IPD5		5	45	µA	VDD = 6.0V, WDT enabled

* These parameters are based on characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
a) The test conditions for all IDD measurements in active operation mode are: OSC1= external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
b) For stand-by current measurements, the conditions are the same, except that the device is in SLEEP mode.

Note 3: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. It is measured in SLEEP with all I/O pins in hi-impedence state and connected to VDD or VSS.

Note 5: In RC mode does not include current through Rext. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

16.4 DC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (COMMERCIAL) PIC16CR54-RC, XT, HS, LP (INDUSTRIAL)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as in table 16.3 unless otherwise stated				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	VIL	VSS		0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt trigger)	VILMC	VSS		0.15 VDD	V	
RTCC (Schmitt trigger)	VILRT	VSS		0.15 VDD	V	
OSC1 (Schmitt trigger)	VILOSC	VSS		0.15 VDD	V	PIC16CR54RC only (Note 5)
OSC1	VILOSC	VSS		0.15 VDD	V	PIC16CR54-XT, HS, LP
Input High Voltage						
I/O ports	VIH	2.0		VDD	V	VDD = 3.0V to 5.5V (Note 6)
	VIH	0.6 VDD		VDD	V	Full VDD range (Note 6)
MCLR (Schmitt trigger)	VIHMC	0.85 VDD		VDD	V	
RTCC (Schmitt trigger)	VIHRT	0.85 VDD		VDD	V	
OSC1 (Schmitt trigger)	VIHOSC	0.85 VDD		VDD	V	PIC16CR54-RC only (Note 5)
OSC1	VIHOSC	0.85 VDD		VDD	V	PIC16CR54-XT, HS, LP
Input Leakage Current (Notes 3, 4)						**For VDD ≤ 5.5V**
I/O ports	IIL	-1		+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR	IILMCL	-5			µA	VPIN = VSS + 0.25V
MCLR	IILMCH		0.5	+5	µA	VPIN = VDD
RTCC	IILRT	-3	0.5	+5	µA	VSS ≤ VPIN ≤ VDD
OSC1	IILOSC1	-3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16CR54-XT, HS, LP
Output Low Voltage						
I/O Ports	VOL			0.5	V	IOL = 10 mA, VDD = 6.0V
OSC2/CLKOUT	VOL			0.5	V	IOL = 1.9 mA, VDD = 6.0V
Output High Voltage						
I/O Ports (Note 4, 5)	VOH	VDD-0.5V			V	IOH = -4.0 mA, VDD = 6.0V
OSC2/CLKOUT	VOH	VDD-0.5V			V	IOH = -0.8 mA, VDD = 6.0V

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : Total power dissipation as stated under absolute maximum ratings must not be exceeded.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

Note 5 : For PIC16CR54-RC devices, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16CR54 be driven with external clock in RC mode.

Note 6: The user may use the better of the two specs. TTL level is guaranteed in 3.0V to 5.5V range.

16.5 AC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (COMMERCIAL) PIC16CR54-RC, XT, HS, LP (INDUSTRIAL)

AC CHARACTERISTICS		Standard Operating Conditions (unless otherwise noted) Operating temperature $T_A \le -40°C \le +85°C$ for industrial and $0°C \le T_A \le +70°C$ for commercial Operating voltage V_{DD} range as in table 16.3 unless otherwise stated				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Oscillator Frequency (Note 2)	FOSCRC FOSCXT FOSCHS FOSCLP	DC 0.1 4		4.0 4 20 200	MHz MHz MHz KHz	RC mode, V_{DD} = 2.5 to 6.25V XT mode, V_{DD} = 2.5 to 6.25V HS mode, V_{DD} = 4.5 to 5.5V LP mode, V_{DD} = 2.0 to 6.25V
Instruction Cycle Time	TCY			4/Fosc		
External Clock in Timing (Note 4) Clock in High or Low Time XT oscillator type LP oscillator type HS oscillator type Clock in Rise or Fall Time XT oscillator type LP oscillator type HS oscillator type	 TCKHLXT TCKHLLP TCKHLHS TCKRFXT TCKRFLP TCKRFHS	 50* 2* 20* 25* 50* 25*		 	 ns µs ns ns ns ns	
RESET Timing MCLR Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler RTCC High Pulse Width RTCC Low Pulse Width	 TRTH TRTL	 0.5 TCY+ 20* 0.5 TCY+ 20*		 	 ns ns	 Note 3 Note 3
RTCC Input Timing, With Prescaler RTCC High Pulse Width RTCC Low Pulse Width RTCC Period	 TRTH TRTL TRTP	 10* 10* $\frac{T_{CY} + 40}{N}$ *		 	 ns ns ns	 Note 3 Note 3 Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	7*	18	30*	ms	VDD = 5V, -40°C to 85°C
Oscillation Start-up Timer Period	TOST	7*	18	30*	ms	VDD = 5V, -40°C to 85°C
I/O Timing I/O Pin Input Valid Before CLKOUT↑ (RC Mode) I/O Pin Input Hold After CLKOUT↑ (RC Mode) I/O Pin Output Valid After CLKOUT↓ (RC Mode)	 TDS TDH TPD	 0.25 TCY+ 30* 0* 		 40*	 ns ns ns	
Capacitive Loading Specs on Output Pins OSC2 All I/O pins	 COSC2 CIO	 	 	 15 50	 pF pF	 In XT, HS and LP modes when external clock is used to drive OSC1.

* Based on characterization, but not tested.

(Notes on next page)

NOTES TO AC CHARACTERISTICS: PIC16CR54-RC, XT, HS, LP (COMMERCIAL) PIC16CR54-RC, XT, HS, LP (INDUSTRIAL)

1. Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.
2. Instruction cycle period (Tcy) equals four times the input oscillator time base period.
   All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
   When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.
3. For a detailed explanation of RTCC input clock requirements see section 4.2.1.
4. Clock-in high time is the duration for which clock input is at VIHOSC or higher. Clock-in low time is the duration for which clock input is at VILOSC or lower.

16.6 Electrical Structure of Pins

FIGURE 16.6.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB)

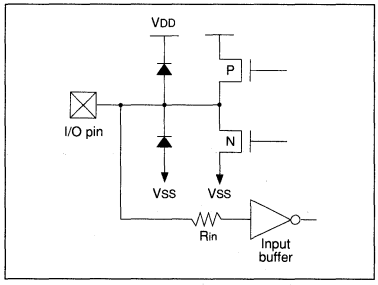
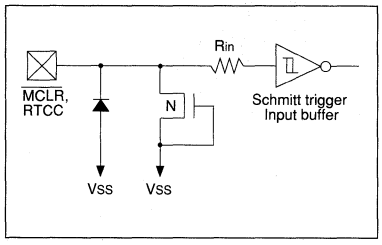


FIGURE 16.6.2 - ELECTRICAL STRUCTURE OF MCLR AND RTCC PINS



17.0 TIMING DIAGRAMS

FIGURE 17.0.1 - RTCC TIMING

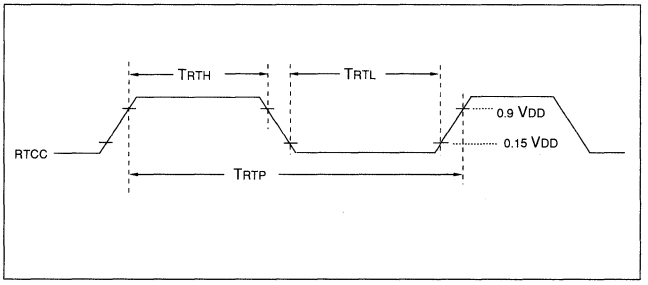
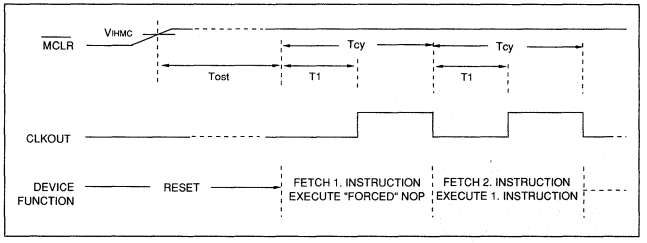
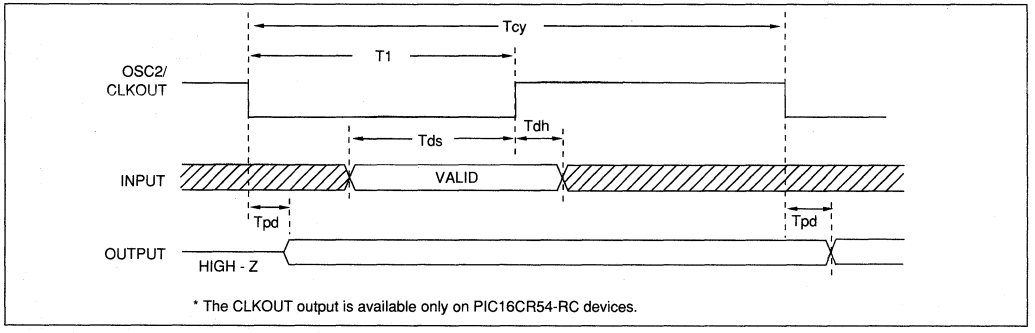


FIGURE 17.0.2 - OSCILLATOR START-UP TIMING (PIC16CR54RC)



Note to figures 16.6.1 and 16.6.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

FIGURE 17.0.3 - INPUT/OUTPUT TIMING FOR I/O PORTS (PIC16CR54RC*)



* The CLKOUT output is available only on PIC16CR54-RC devices.

18.0 DC & AC CHARACTERISTICS GRAPHS/TABLES:

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected from units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'max' and 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 18.0.1 - TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

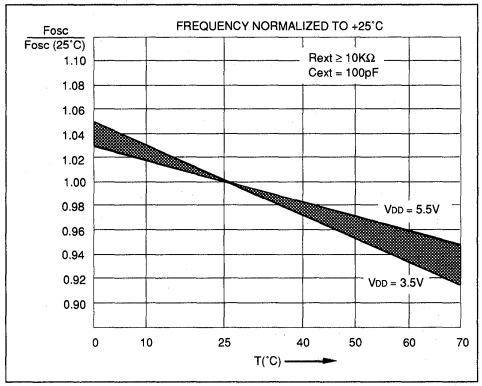


FIGURE 18.0.2 - TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

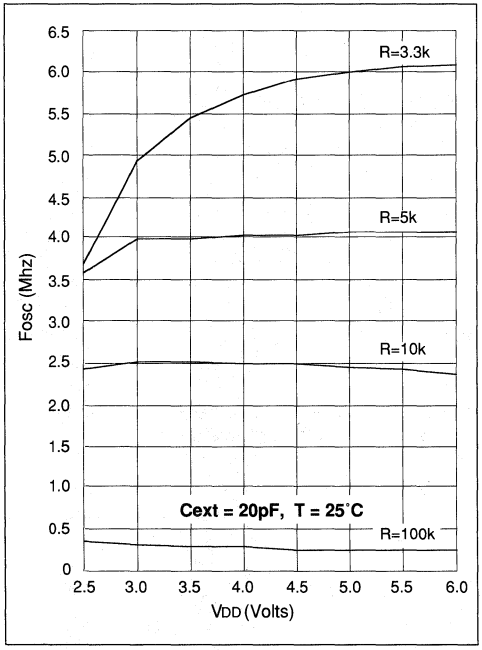


FIGURE 18.0.3 - TYPICAL RC OSCILLATOR FREQUENCY vs. VDD

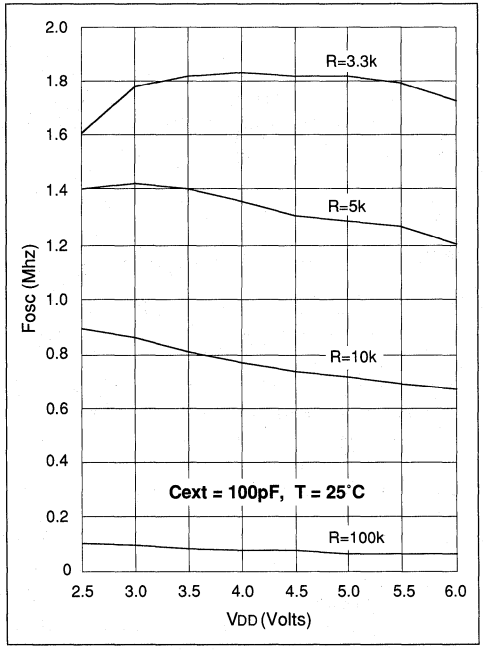


FIGURE 18.0.4 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

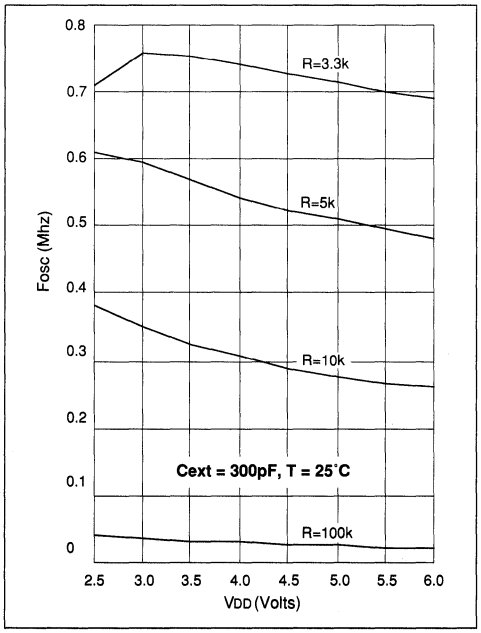


TABLE 18.0.1 - RC OSCILLATOR FREQUENCY VARIATION FROM UNIT TO UNIT

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	3.3k	6.02 Mhz	± 28%
	5k	4.06 Mhz	± 25%
	10k	2.47 Mhz	± 24%
	100k	261 Khz	± 39%
100pf	3.3k	1.82 Mhz	± 18%
	5k	1.28 Mhz	± 21%
	10k	715 Khz	± 18%
	100k	72.4 Khz	± 28%
300pf	3.3k	712.4 Khz	± 14%
	5k	508 Khz	± 13%
	10k	278 Khz	± 13%
	100k	28 Khz	± 23%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for full VDD range.

FIGURE 18.0.5 - TYPICAL IPD vs VDD WATCHDOG TIMER ENABLED 25°C

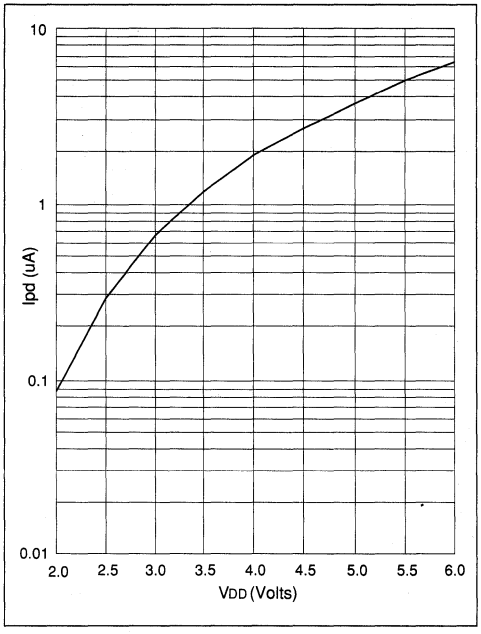


FIGURE 18.0.6 - MAXIMUM Ipd vs VDD WATCHDOG TIMER ENABLED

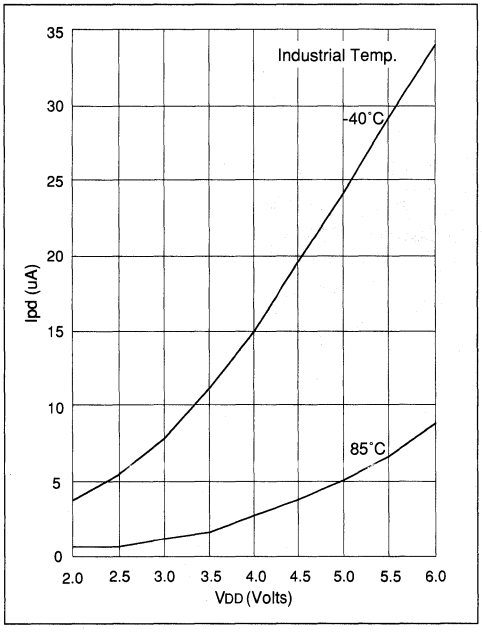


FIGURE 18.0.7 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs VDD

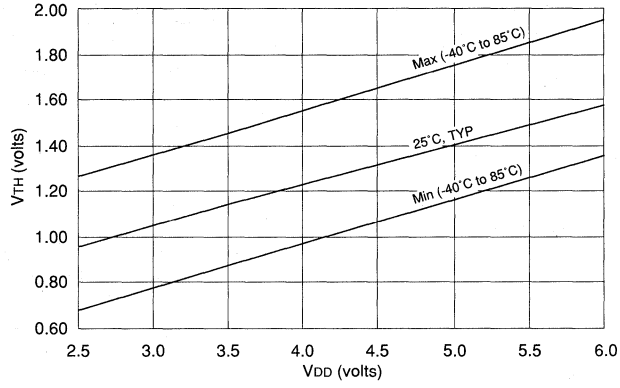
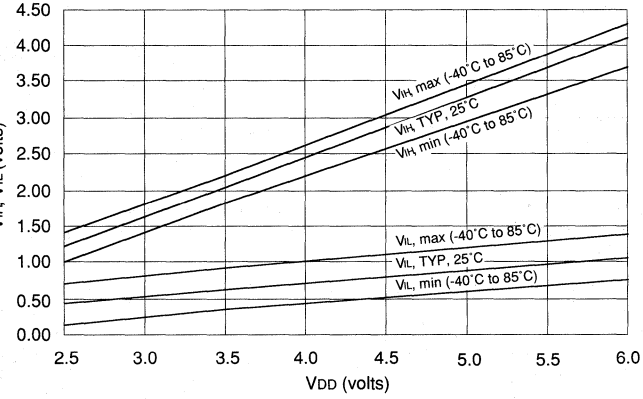


FIGURE 18.0.8 - VIH, VIL OF $\overline{MCLR}$, RTCC AND OSC1 (IN RC MODE) vs VDD



Note: These input pins have Schmitt trigger input buffer.

FIGURE 18.0.9 - VTH, (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs VDD

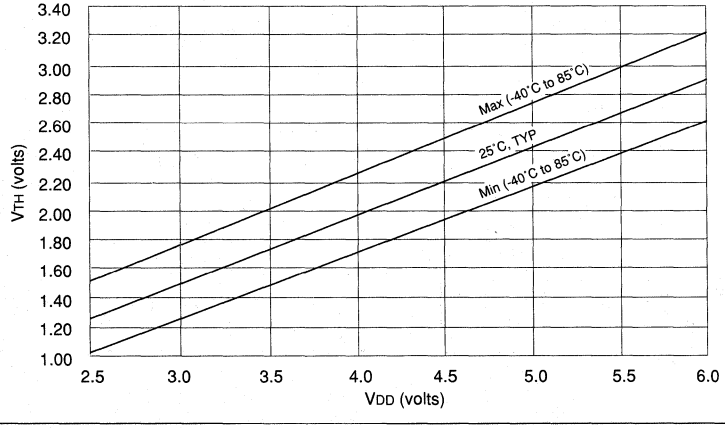


FIGURE 18.0.10 - TYPICAL IDD vs FREQ (EXT CLOCK, 25°C)

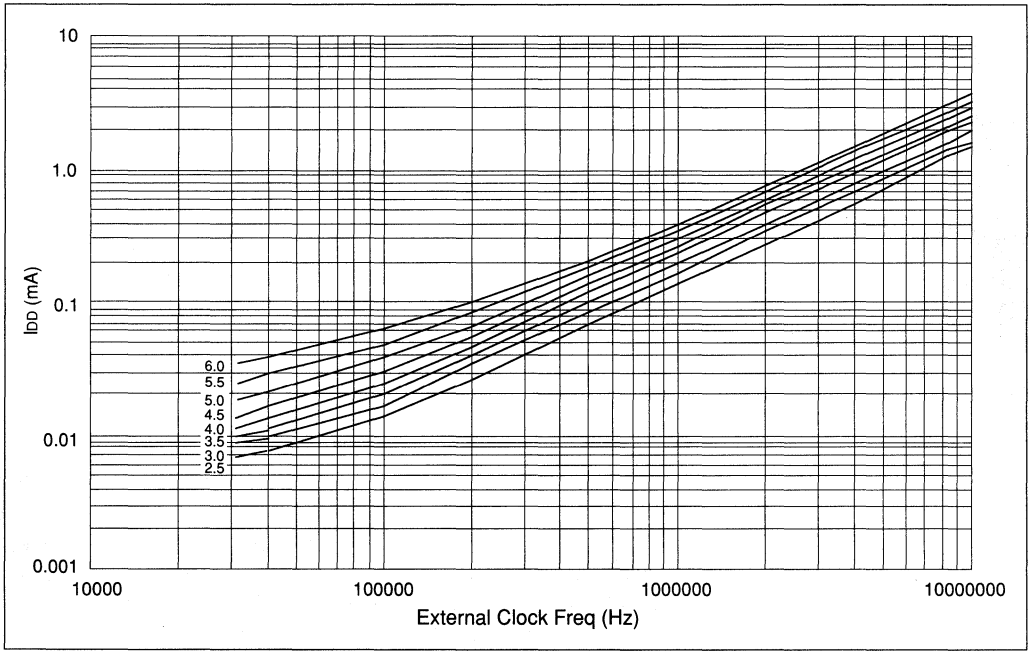


FIGURE 18.0.11 - MAXIMUM IDD vs FREQ (EXT CLOCK, -40°C TO +85°C)

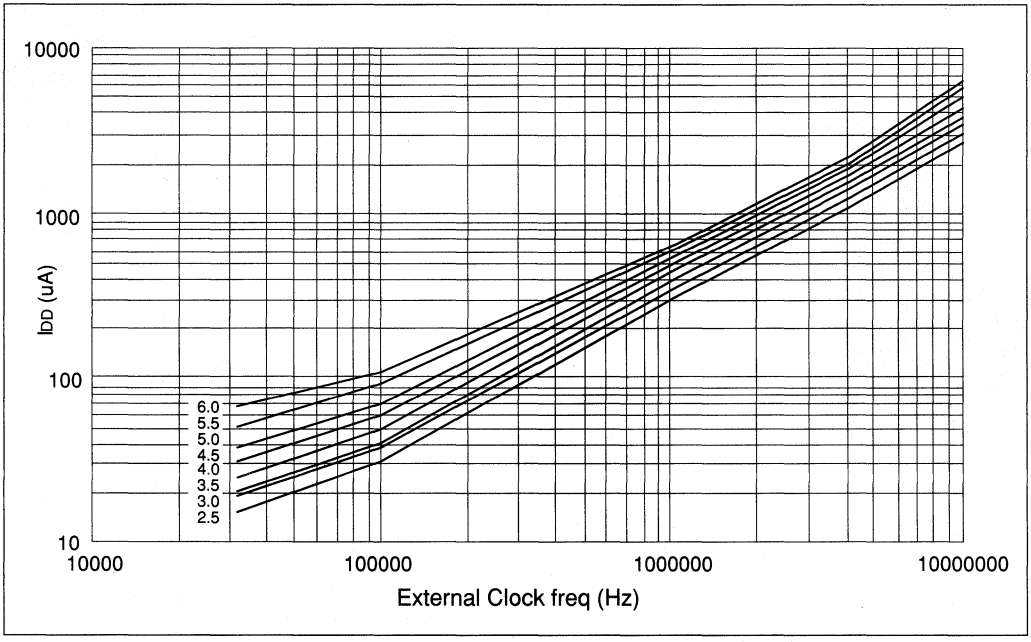


FIGURE 18.0.12 -WDT Timer Time-out Period vs VDD

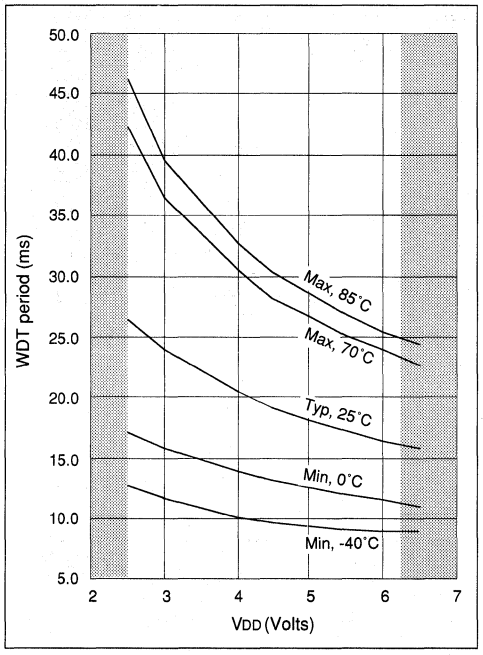


FIGURE 18.0.13 -Transconductance (gm) of HS Oscillator vs VDD

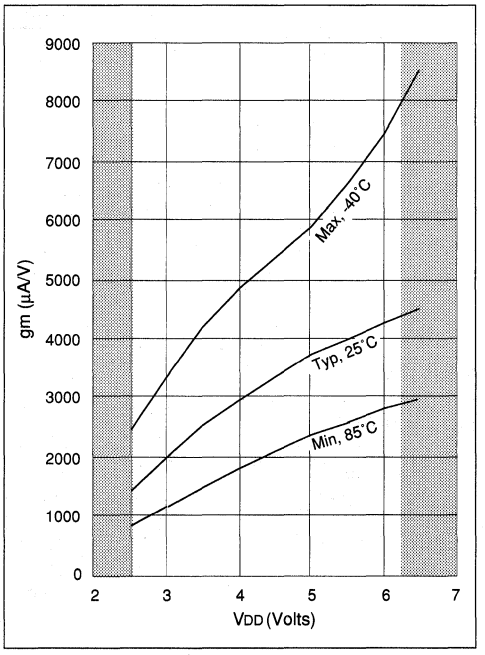


FIGURE 18.0.14 -Transconductance (gm) of LP Oscillator vs VDD

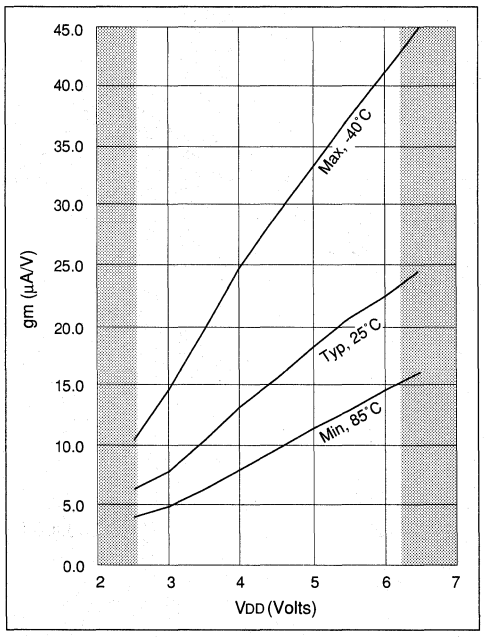
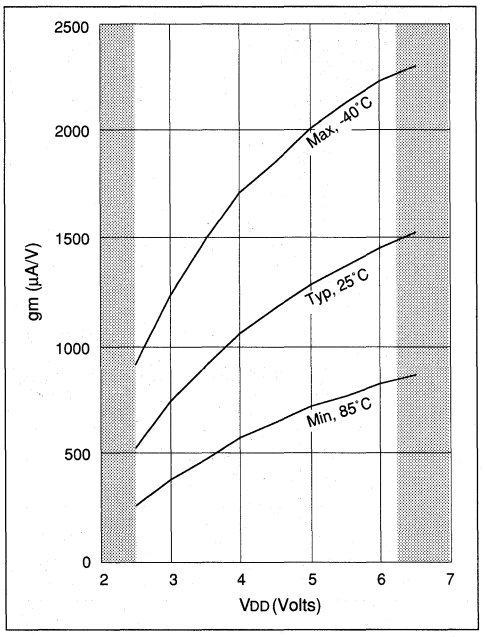


FIGURE 18.0.15 -Transconductance (gm) of XT Oscillator vs VDD



Note: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

FIGURE 18.0.16 - IOH vs VOH, VDD = 3V

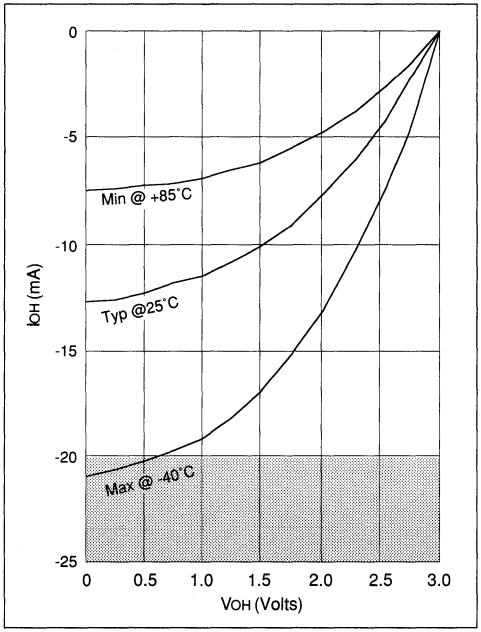


FIGURE 18.0.17 - IOH vs VOH, VDD = 5V

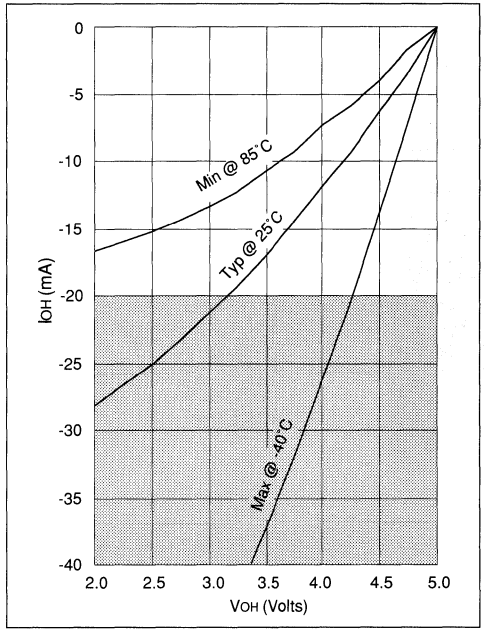


FIGURE 18.0.18 - IOL vs VOL, VDD = 3V

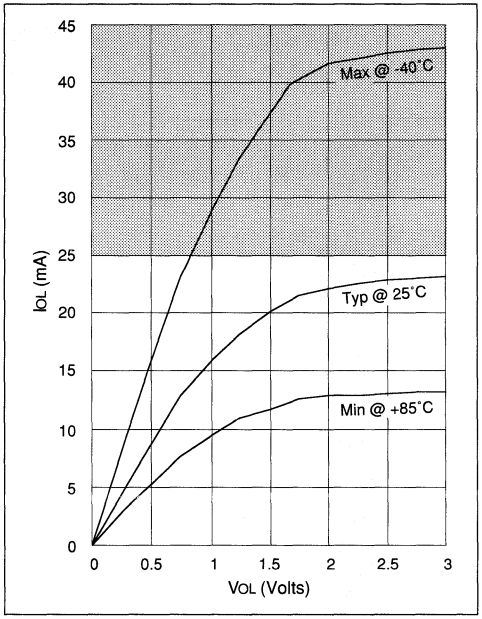
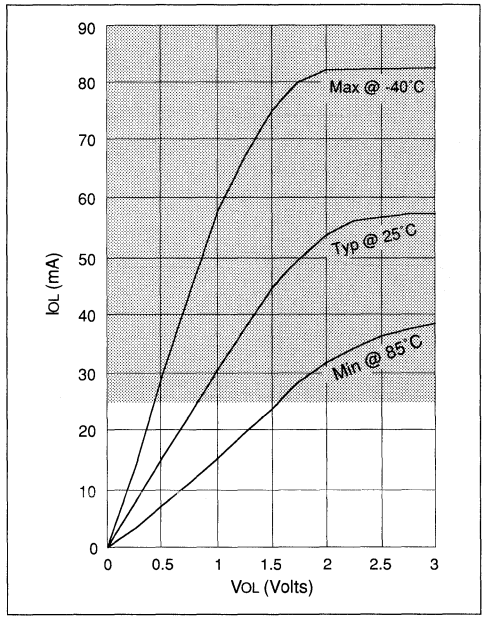


FIGURE 18.0.19 - IOL vs VOL, VDD = 5V



Note: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

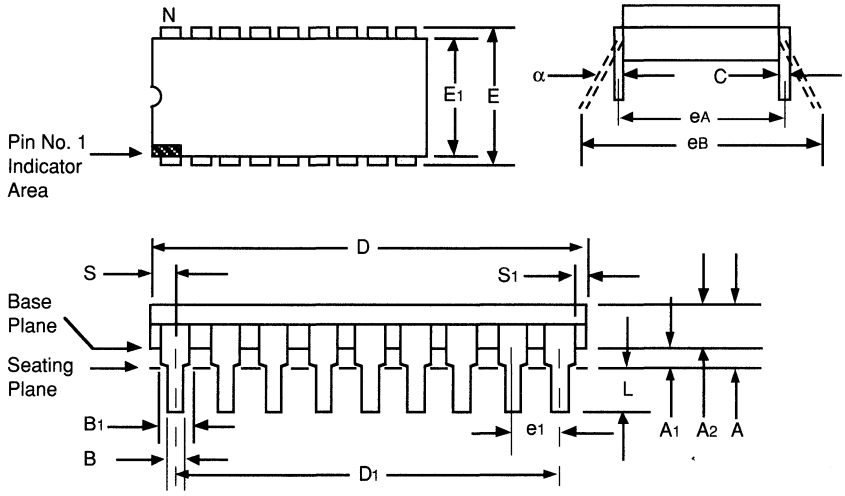
TABLE 18.0.2 - INPUT CAPACITANCE FOR PIC16CR54 *

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA, RB port	5.0	4.3
$\overline{\text{MCLR}}$	2.0	2.0
OSC1,OSC2/CLKOUT	4.0	3.5
RTCC	3.2	2.8

* All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

19.0 PACKAGING DIAGRAMS AND DIMENSIONS

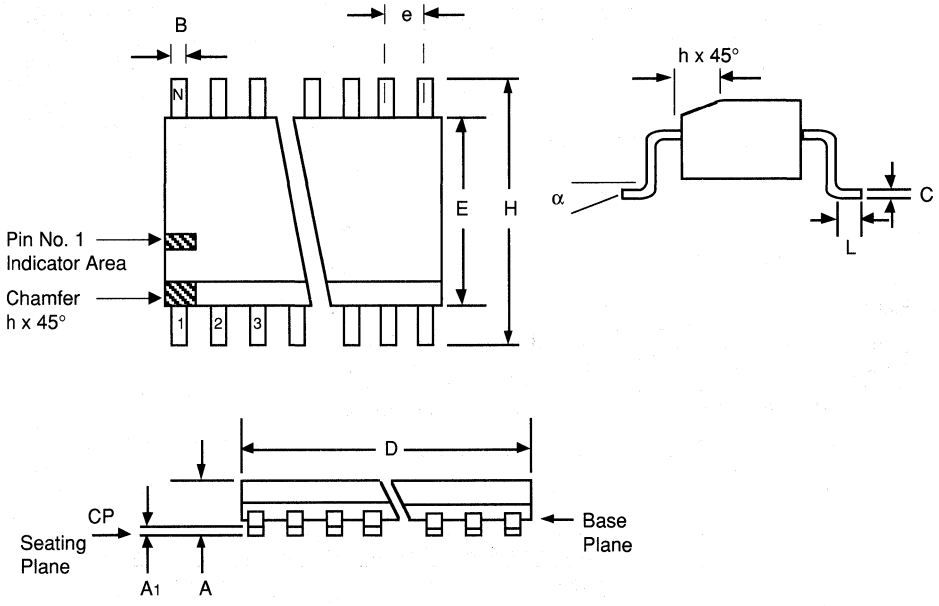
19.1 18-Lead Plastic Dual In-Line (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.479	23.495		0.885	0.925	
D1	20.320	20.32	**Reference**	0.800	0.800	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

PACKAGING DIAGRAMS AND DIMENSIONS (CONT.)

19.2 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)

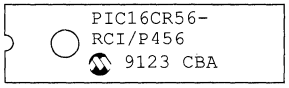


Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A_1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	11.3538	11.7348		0.447	0.462	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	18	18		18	18	
CP	–	0.1016		–	0.004	

19.3 Package Marking Information

18L PDIP

Example



18L SOIC

Example

Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

20.0 DEVELOPMENT SUPPORT

20.1 PICMASTER-16™: High Performance Universal In-Circuit Emulator System

The PICMASTER Universal In-Circuit Emulator System is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X and PIC17CXX families. This system currently supports the PIC16CR54, PIC16C54, PIC16C55, PIC16C56 and PIC16C57 at clock frequencies of 4 MHz and PIC17C42 at 16 MHz.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new microcontroller architectures with data and program memory paths to 16-bits.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.0 environment, allowing the operator access to a wide range of supporting software and accessories.

Provided with the PICMASTER System is a high performance real-time In-Circuit Emulator, a microcontroller EPROM programmer unit, a macro assembler program, and a simulator program. Sample programs are provided to help quickly familiarize the user with the development system and the PIC microcontroller line.

Coupled with the user's choice of text editor, the system is ready for development of products containing any of Microchip's microcontroller products.

A "Quick Start" PIC Product Sample Pak containing user programmable parts is included for additional convenience.

Microchip provides additional customer support to developers through an Electronic Bulletin Board System (EBBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS system.

20.1.1 Host System Requirements:

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.0 environment was chosen to best make these features available to you the end user. To properly take advantages of these features, PICMASTER requires installation on a system having the following minimum configuration:

- PC AT compatible machine: 80286, 386SX, 386DX, or 80486 with ISA or EISA Bus.
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended).
- MSDOS / PCDOS version 3.1 or greater.
- Microsoft Windows® version 3.0 or greater operating in either standard or 386 enhanced mode).
- 1 Mbyte RAM (2 Mbytes recommended).
- One 5.25" floppy disk drive.
- Approximately 10 Mbytes of hard disk (1 Mbyte required for PICMASTER, remainder for Windows 3.0 system).
- One 8-bit PC AT (ISA) I/O expansion slot (half size)
- Microsoft® mouse or compatible (highly recommended).

20.1.2 Emulator System Components:

The PICMASTER Emulator Universal System consists primarily of 4 major components:

- **Host-Interface Card:** The PC Host Interface Card connects the emulator system to an IBM PC compatible system. This high-speed parallel interface requires a single half-size standard AT / ISA slot in the host system. A 37-conductor cable connects the interface card to the external Emulator Control Pod.
- **Emulator Control Pod:** The Emulator Control Pod contains all emulation and control logic common to all microcontroller devices. Emulation memory, trace memory, event and cycle timers, and trace/breakpoint logic are contained here. The Pod controls and interfaces to an interchangeable target-specific emulator probe via a 14" precision ribbon cable.
- **Target-specific Emulator Probe:** A probe specific to microcontroller family to be emulated is installed on the ribbon cable coming from the control pod. This probe configures the universal system for emulation of a specific microcontroller. Currently, the 16C5x family, and the new PIC17C42 microcontrollers are supported. Future microcontroller probes will be available as they are released.
- **PC Host Emulation Control Software:** Host software necessary to control and provide a working user interface is the last major component of the system. The emulation software runs in the Windows 3.0 environment, and provides the user with full display, alter, and control of the system under emulation. The Control Software is also universal to all microcontroller families.

  The Windows 3.0 System is a multitasking operating system which will allows the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.0, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

Under Windows 3.0, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16C5x processor and a PIC17Cxx processor).

FIGURE 20.1.1 - PICMASTER-16

FIGURE 20.1.2 - PICMASTER-16 SYSTEM CONFIGURATION

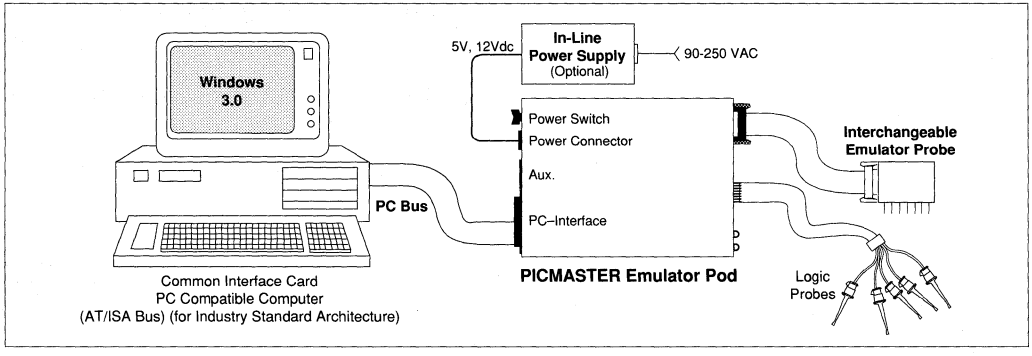
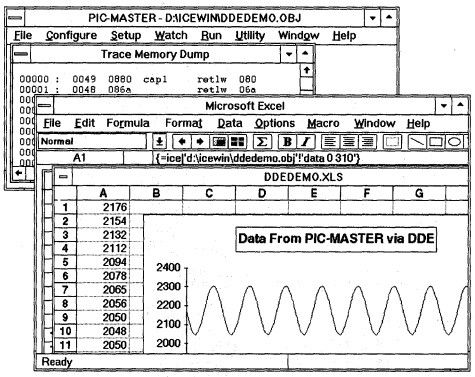


FIGURE 20.1.3 - PICMASTER-16 TYPICAL SCREEN



20.2 PICPAK-II™ Development Kit

When real time or in-circuit emulation is not required for code development the PICPAK-II (PIC Applications Kit) offers the right solution. This very low cost PC hosted software development tool combines the power and versatility of the PICALC assembler and PICSIM simulator software tools to compile, execute, debug and analyze microcode in a PC hosted environment. Microcode debugging capability includes software trace, breakpoints, symbolic debug and stimulus file generation. An EPROM PIC Programmer and "Quick Start" PIC16C5X product sample PAK is included for final code verification.

20.3 PICALC Cross-Assembler

The PIC Cross Assembler PICALC is a PC hosted software development tool supporting the PIC16C5X series microcontrollers. PICALC offers a full featured Macro and Conditional assembly capability. It can also generate various object code formats including several Hex formats to support Microchip's proprietary development tools as well as third party tools. Also supports Hex (default), Decimal and Octal Source and listing formats. An assembler users manual is available for detailed support.

20.4 PICSIM Software Simulator

PICSIM is a software tool which allows for PIC16C5X code development in a PC host environment. The PICSIM software allows you to simulate the PIC16C5X series microcontroller products on an instruction level. On any given instruction, the user may examine or modify any of the data areas within the PIC or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in single step, execute until break or in a trace mode. PICSIM uses two forms of symbolic debugging: an internal symbol table for disassembling opcodes and the displaying of source code from a listing file. PICSIM offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi project software development tool.

20.5 PICPRO-II Programmer

PICPRO II is a production quality programmer with both stand-alone and PC based operation. The PICPRO II will program the entire family of PIC16C5X series of 8-bit microcontrollers. It can read, program, verify, and code protect parts without the need of a PC host. Its EEPROM memory holds programming data and parametric information even when power is removed making it ideal for duplicating PICs. It can also operate with a PC host and do complete read, program, verify, as in stand-alone mode with the additional features of program buffer editing, serialization of both code-protected and non code-protected parts. The PICPRO II comes with both 28 and 18 pin zero insertion force programming sockets on a removable socket module. Additional socket modules are available for the SOIC and PLCC packages. The PICPRO II conforms fully to Microchip's Programming Algorithm. Its programmable V_{CC} and V_{PP} supplies allow the PICPRO II to support PIC microcontrollers with various operating voltage ranges. PICPRO II can read and verify the ROM code and configuration fuses for a non code-protected PIC16CR54.

20.6 ORDERING DEVELOPMENT TOOLS

The development tools are packaged as comprehensive systems for your convenience. Their description and planned availability dates are as follows:

System	Description	Available
PIC-PAK-II™	Includes: PICALC Assembler PICSIM, PICPRO II Simulator Programmer Manuals	Now
PICMASTER-16	Includes: PICALC Assembler PICPRO II Programmer PICALC Assembler PICSIM Simulator PIC16C5X Personality Module	Now
PICPRO II	Includes: PICPRO II Programmer DIP Socket Module Manuals	Now

21.0 CURRENT PRODUCT AVAILABILITY

The following selections are currently available (for the Part-Number coding, refer to the back page):

Oscillator Type	Temp/ Package	Descriptions
RC, XT, HS* or LP	/P	PDIP, 0°C to +70°C
RC, XT, HS* or LP	I/P	PDIP, -40°C to +85°C
RC, XT, HS* or LP	/SO	SOIC, 0°C to +70°C
RC, XT, HS* or LP	I/SO	SOIC, -40°C to +85°C

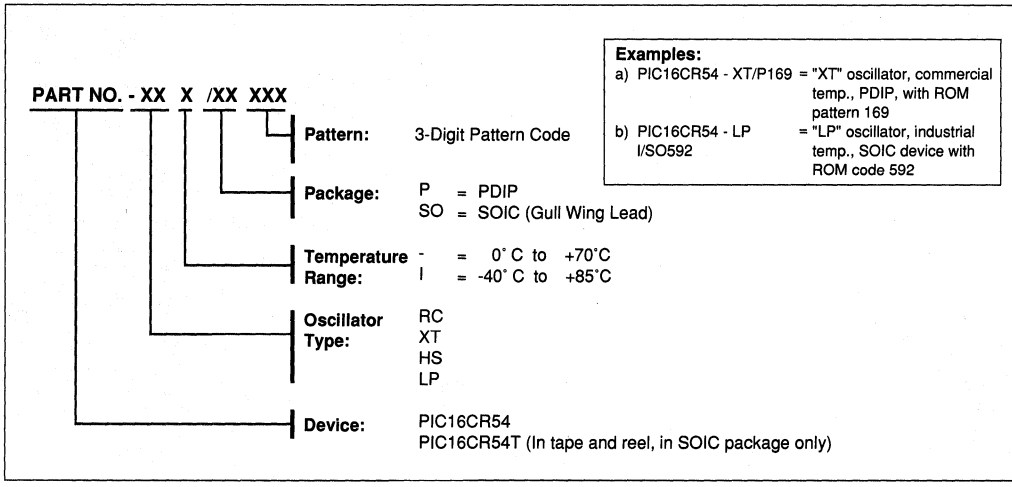
* Consult local sales office for availability of HS parts.

Notes

Index

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices. For the *currently available code-combinations*, refer to previous page.



Microchip

PIC®16C71

8-Bit CMOS EPROM Microcontroller with A/D Converter

1

FEATURES

High Performance RISC-like CPU

- Only 35 single word instructions to learn
- All single cycle instructions (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 14-bit wide instructions
- 8-bit wide data path
- 1024 x 14 on-chip EPROM program memory
- 36 x 8 general purpose registers (SRAM)
- 15 special function hardware registers
- 8 levels deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources: External INT pin, RTCC timer, A/D conversion completion and interrupt on change on four port B pins

Peripheral features

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 20 mA source max. per pin
- 8 bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- A/D converter module:
  - 4 analog inputs multiplexed into one A/D converter
  - Sample and hold
  - 20 µs conversion time/channel
  - 8-bit resolution with ±1 LSB accuracy
  - External reference input, V_{REF} ($V_{REF} \leq V_{DD}$)
  - Analog input range: V_{SS} to V_{REF}

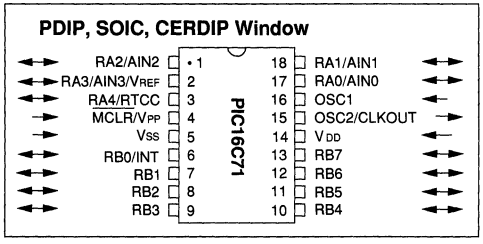
Special microcontroller features

- Power on reset
- Power up timer
- Oscillator start-up timer
- Watchdog timer (WDT) with its own on-chip RC oscillator for reliable operation
- Security EPROM fuse for code-protection
- Power saving SLEEP mode
- User selectable oscillator options:
  - RC oscillator: RC
  - Crystal/resonator: XT
  - High speed crystal/resonator: HS
  - Power saving low frequency crystal: LP
- Serial, In-System Programming (ISP) of EPROM program memory using only two pins

CMOS technology

- Low power, high speed CMOS EPROM technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 3.0V to 6.0V
  - Industrial: 3.0V to 6.0V
  - Automotive: 3.0V to 6.0V
- Low power consumption
  - < 2 mA @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 KHz (with A/D off)
  - < 1 µA typical standby current @ 3V

FIGURE A - PIN CONFIGURATION



INTRODUCTION

The PIC16C71 is a high performance, low cost, CMOS, fully static EPROM based 8-bit microcontroller with on-chip Analog to Digital converter.
It is the first member of a new and improved family of PIC16CXX microcontrollers (customers familiar with the PIC16C5X products may refer to Appendix A for a list of enhancements).
Its high performance is due to all single word instructions (14-bit wide) that are executed in single cycle (200 ns at 20 MHz clock) except for program-branches which take two cycles (400 ns).
The PIC16C71 has four interrupt sources and an eight level hardware stack.

The peripherals include an 8 bit timer/counter with 8 bit prescaler (effectively a 16 bit timer), 13 bi-directional I/O pins and an 8 bit A/D converter. The high current drive (25 mA max. sink, 20 mA max source) of the I/O pins help reduce external drivers and therefore, system cost.

The A/D converter has four channels, sample and hold, 8 bit resolution with ±1 LSB accuracy. Conversion time is typically 30 µs including sampling time.

The PIC16C71 product is supported by an assembler, an in-circuit emulator and a production quality programmer. All the tools are supported on IBM PC and compatible machines.

FIGURE B: PIC16C71 BLOCK DIAGRAM

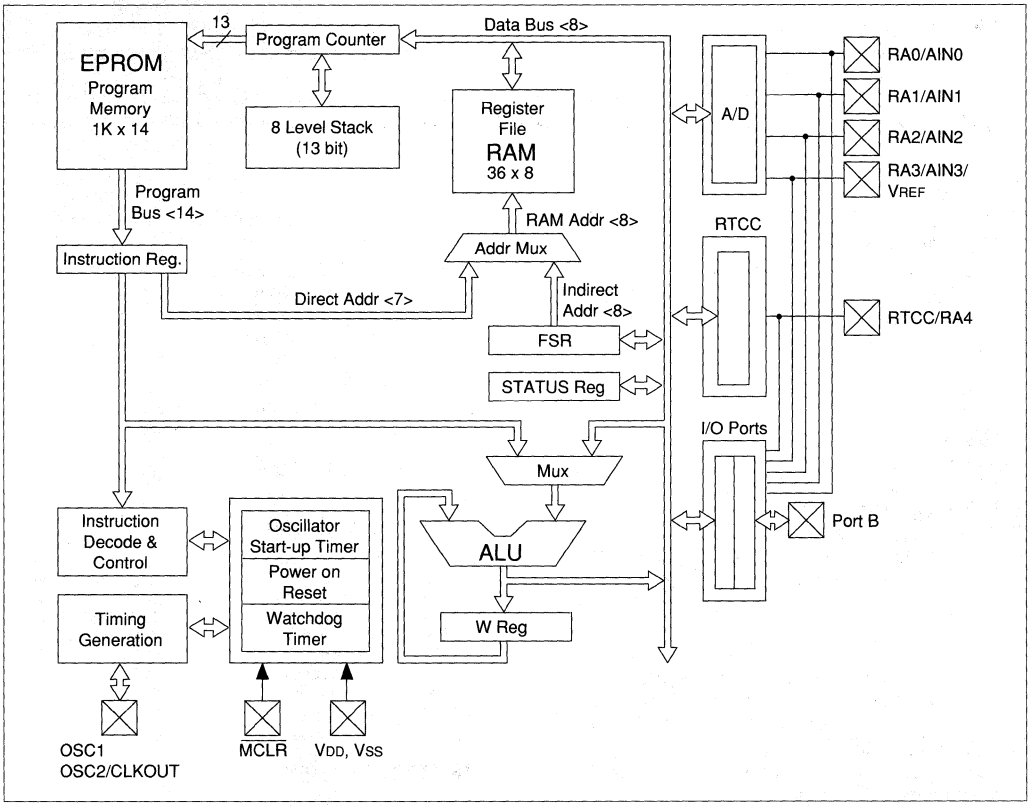


Table of Contents

Table of Figures

Table of Tables

Trademarks:

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PICMASTER, PICPAK, PICPRO and PRO MASTER are trademarks of Microchip Technology Incorporated.

IBM PC is a registered trademark of IBM Corporation.

MS DOS and Microsoft Windows are registered trademarks of Microsoft Corporation.

1.0 GENERAL DESCRIPTION

The PIC16C71 is a low cost, high performance, CMOS, fully static, EPROM-based 8-bit microcontroller with on-chip analog to digital converter. It employs an advanced RISC-like architecture. A reduced set of 35 instructions, all single word instructions (14-bit wide), all single cycle instructions (200ns) except for 2-cycle program branches, instruction pipe-lining, large register set and separate instruction and data memory (Harvard architecture) schemes are some of the architectural innovation used to achieve very high performance. The PIC16C71 typically achieves a 2:1 code compression and a 5:1 speed improvement over other 8 bit microcontrollers in its class.

The PIC16C71 is equipped with special features to reduce external components and thus reduce cost, enhance system reliability and reduce power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low cost solution and the LP oscillator minimizes power consumption. The SLEEP (power down) mode offers power saving. The user can wake up the chip from SLEEP through external interrupts and reset.

A highly reliable watchdog timer with its own on-chip RC oscillator provides protection against software malfunction.

The UV-erasable cerdip-packaged versions are ideal for code development while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontroller while benefiting from the OTP flexibility.

1.1 UPWARD COMPATIBILITY WITH PIC16C5X

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an improved version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of modifications. Code written for PIC16C5X can be easily ported to PIC16C71 (see Appendix B).

1.2 APPLICATIONS

The PIC16C71 fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, pointing devices, and telecom processors. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages for through hole or surface mounting make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use, and I/O flexibility makes the PIC16C71 very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, replacement of "glue" logic in larger systems, co-processor applications).

2.0 PIC16C71 DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information and tables in this section. When placing orders, please use the "PIC16C71 Product Identification System" on the back page of this data sheet to specify the correct part number.

2.1 UV Erasable Devices

The UV erasable version, offered in cerdip package is optimal for prototype development and pilot series.

The UV erasable version can be erased and reprogrammed to any of the oscillator modes etc. Microchip's PRO MASTER™ programmer supports programming of the PIC16C71.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages permit the user to program them once. In addition to the program memory, the oscillator fuses, configuration fuses and optionally, the ID locations must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C71 can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C71 uses a Harvard architecture, in which, program and data are accessed from separate memories. This improves bandwidth over traditional Von-Neuman architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. In PIC16C71, op-codes are 14-bit wide making it possible to have all single word instructions. A 14 bit wide program memory access bus fetches a 14 bit instruction in a single cycle. A two-stage pipeline

overlaps fetch and execution of instructions. Consequently, all instructions (35 in all) execute in a single cycle (200ns @ 20 MHz) except for program branches.

The PIC16C71 address 1K x 14 program memory space, all on-chip. Program execution is internal only (microcontroller mode).

The PIC16C71 can directly or indirectly address its 48 register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C71 has a fairly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C71 simple yet efficient. In addition, the learning curve is reduced significantly.

3.2 Clocking Scheme/Instruction Cycle

The clock input (from pin OSC1) is internally divided by four to generate four non overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, PC is incremented every Q1, instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3.2.1.

3.3 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" in PIC16C71 consists of Q1, Q2, Q3 and Q4. Instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction.

A fetch cycle begins with the program counter (PC) incrementing in Q1.

3.1 - PIC16C71 PINOUT DESCRIPTION

Pin name	Pin Type	Pin function	
		Normal operation	Serial In-System Programming (ISP) Mode
VDD	P	Power	Power
VSS	P	Ground	Ground
OSC1	I	Clock input/oscillator connection	-
OSC2/CLKOUT	I/O	Oscillator connection/CLKOUT output. It is CLKOUT in RC oscillator mode and oscillator connection in all other modes.	-
$\overline{MCLR}$/VPP	I/P	Master clear (external reset) input. Active low. It has Schmitt trigger input buffer.	Master clear/programming voltage (VPP) supply
RA4/RTCC	I/O	Open-drain output/input pin. It is also the clock input to RTCC timer/counter: Schmitt trigger input buffer	-
RA0/AIN0	I/O	Bidirectional I/O pin/Analog input channel 0. As digital input it has TTL input levels	-
RA1/AIN1	I/O	Bidirectional I/O pin/Analog input channel 1. As digital input it has TTL input levels	-
RA2/AIN2	I/O	Bidirectional I/O pin/Analog input channel 2. As digital input it has TTL input levels	-
RA3/AIN3/VREF	I/O	Bidirectional I/O pin/Analog input channel 3/Analog reference voltage input . As digital input it has TTL input levels	-
RB0/INT	I/O	Bidirectional I/O pin/External interrupt input. TTL input levels	-
RB1	I/O	Bidirectional I/O pin. TTL input levels	-
RB2	I/O	Bidirectional I/O pin. TTL input levels	-
RB3	I/O	Bidirectional I/O pin. TTL input levels	-
RB4	I/O	Bidirectional I/O pin. TTL input levels	-
RB5	I/O	Bidirectional I/O pin. TTL input levels	-
RB6	I/O	Bidirectional I/O pin. TTL input levels	Clock input
RB7	I/O	Bidirectional I/O pin. TTL input levels	Data input/output

Legend: I = input, O = output, I/O = input/output, P = power. -: Not used.

FIGURE 3.2.1 - CLOCK/INSTRUCTION CYCLE

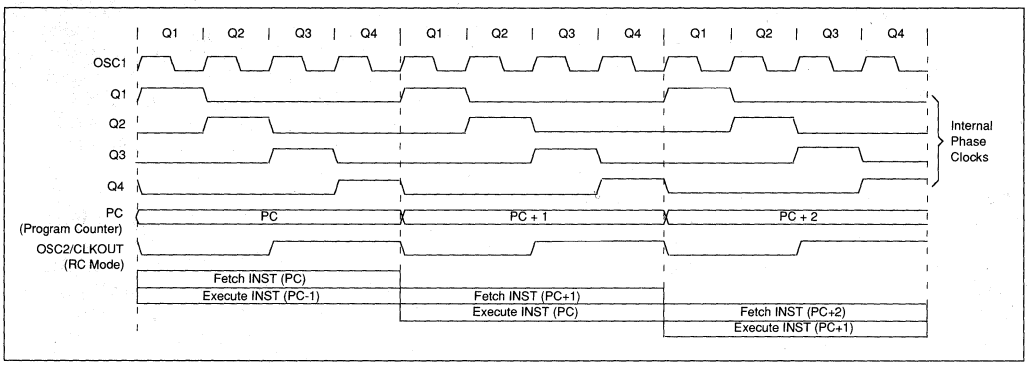


FIGURE 3.4.1 - PROGRAM MEMORY MAP AND STACK

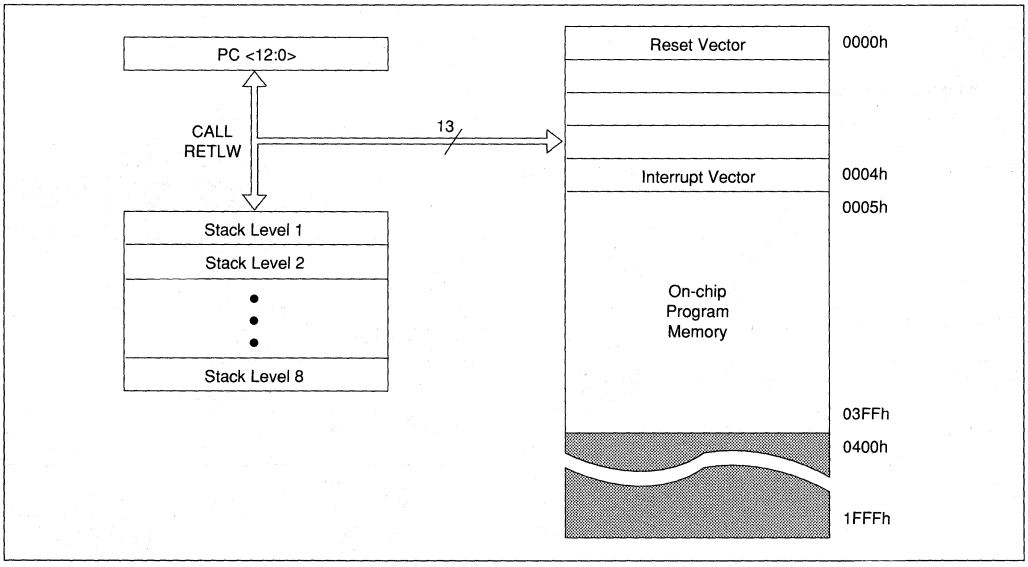
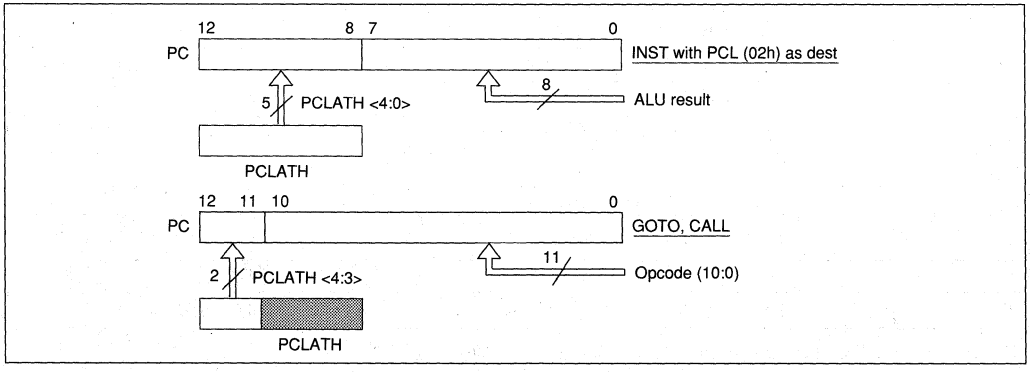


FIGURE 3.5.1 - LOADING OF PC IN DIFFERENT SITUATIONS



The fetched instruction is latched into the "Instruction Register (IR)" which is decoded and executed during Q2, Q3 and Q4. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

3.4 Program Memory Organization

The PIC16C71 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. In PIC16C71 only the first 1K x 14 (0000h - 03FFh) are physically implemented. Accessing a location above 3FFh will cause a wrap-around within the first 1K x 14 space. The reset vector is at 0000h and the interrupt vector is at 0004h.

3.5 Program Counter Module

The program counter (PC) is 13-bit wide. The low byte, PCL is a readable and writable register (02h). The high byte of the PC, PCH is not directly readable or writable. The high byte of the PC can be written through the PCLATH register (0Ah). When the PC is loaded with a new value during a CALL, GOTO or a write to PCL, the high bits of PC are loaded from PCLATH as shown in figure 3.5.1.

3.6 Stack

The PIC16C71 has an 8 deep x 13 bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is pushed in the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is popped in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH (0Ah) is not affected by a PUSH or a POP operation.

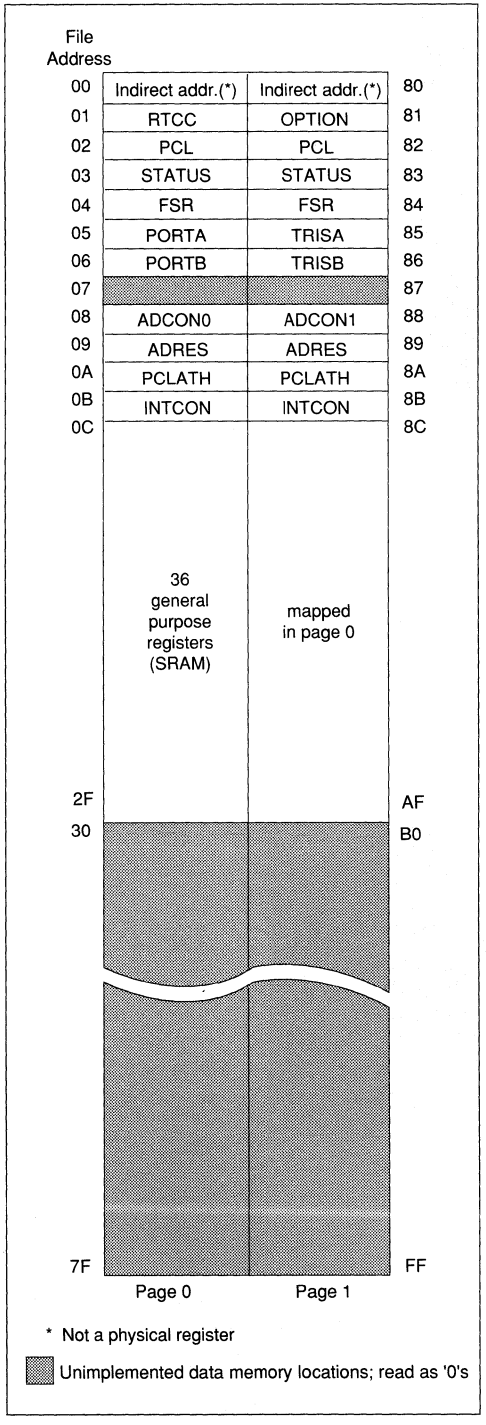
3.7 Register File Organization

The register file, in PIC16C71 is organized as 128 x 8. It is accessed either directly or indirectly through file select register FSR. It is also referred to as the data memory. There are several register file page select bits in the STATUS register allowing up to four pages. However, in the PIC16C71 data memory extends only up to 2Fh. The first 12 locations are used to map special function registers. Locations 0Ch - 2Fh are general purpose registers implemented as static RAM. Some special function registers are mapped in page 1. When in page 1, accessing locations 8Ch - AFh will access the RAM in page 0 (Figure 3.7.1).

3.8 Indirect Addressing Register

Indirect addressing is possible by using file address 00h. Any instruction using f0 as file register actually accesses data pointed to by the file select register, FSR (address 04h). Reading f0 itself indirectly will produce 00h. Writing to f0 indirectly results in a no-operation (although status bits may be affected).

FIGURE 3.7.1 - DATA MEMORY MAP



3.9 STATUS Register (f03)

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for data memory.

The status register (f03) can be destination for any instruction like any other register. However, the status bits are set following the write. Furthermore, TO and PD bits are not writable. Therefore, the result of an instruction with status register as destination may be different than intended. For example, CLRF f3 will clear all bits except for TO and PD and then set the Z bit and leave status register as 000UU100 (where U = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the status registers because these instructions do not affect any status bit.

For other instructions, affecting any status bits, see section "Instruction Set Summary" (Section 4.0)

3.9.1 CARRY/BORROW AND DIGIT CARRY/ BORROW BITS

The carry bit (C) is a carry out in addition operations (ADDWF, ADDLW) and a borrow out in subtract operations (SUBWF, SUBLW). The following examples explain operation of carry/borrow bit:

```
;SUBLW Example #1
;
MOVLW   0x01    ;wreg=1
SUBLW   0x02    ;wreg= 2-wreg = 2-1=1
                ;Carry=1: result is positive
;
;SUBLW Example #2
;
MOVLW   0x02    ;wreg=2
SUBLW   0x01    ;wreg=1-wreg=1-2=FFh
                ;Carry=0: Result is negative
;
;SUBWF Example #1
;
clrf    0x20    ;f(20h)=0
movlw   1       ;wreg=1
subwf   0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
                ;Carry=0:Result is negative
;
;SUBWF Example #2
movlw   0xFF    ;
movwf   0x20    ;f(20h)=FFh
clrw            ;wreg=0
subwf   0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
                ;Carry=1: Result is positive
;
```

The digit carry operates in the same way as the carry bit, i.e.: it is a borrow in subtract operations.

3.9.2 TIME OUT AND POWER DOWN STATUS BITS (TO, PD)

The "TO" and "PD" bits in the status register f03 can be tested to determine if a RESET condition has been caused by a watchdog timer time-out, a power-up condition, or a wake-up from SLEEP by the watchdog timer or $\overline{MCLR}$ pin.

These status bits are only affected by events listed in Table 3.9.1.1.

TABLE 3.9.2.1 - EVENTS AFFECTING PD/ TO STATUS BITS

Event	TO	PD	Remarks
Power-up	1	1	
WDT Timeout	0	U	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

U: unchanged

Note: A WDT timeout will occur regardless of the status of the TO bit. A SLEEP instruction will be executed, regardless of the status of the PD bit. Table 3.9.2.2 reflects the status of PD and TO after the corresponding event.

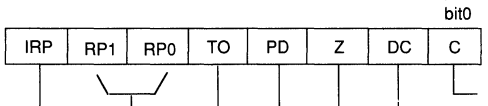
TABLE 3.9.2.2 - PD/TO STATUS AFTER RESET

TO	PD	RESET was caused by
0	0	WDT wake-up from SLEEP
0	1	WDT time-out (not during SLEEP)
1	0	$\overline{MCLR}$ wake-up from SLEEP
1	1	Power-up
U	U	$\overline{MCLR}$ reset during normal operation

U: unchanged

Note: The PD and TO bit maintain their status until an event of Table 3.9.2.1 occurs. A low-pulse on the $\overline{MCLR}$ input does not change the PD and TO status bits.

FIGURE 3.9.1 - STATUS REGISTER



ADDRESS:	03h
RESET CONDITION:	000??XXX
TO, PD are set or reset as shown in Table 3.9.2.1	

CARRY/$\overline{\text{BORROW}}$ BIT:
For ADDWF, SUBWF , ADDLW and SUBLW instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
Note that a subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

DIGIT CARRY/$\overline{\text{BORROW}}$ BIT:
For ADDWF, SUBWF , ADDLW and SUBLW instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

ZERO BIT:
Set if the result of an arithmetic or logic operation is zero.
Reset otherwise.

POWER DOWN BIT:
Set to "1" during power up or by a CLRWDT command. This bit is reset to "0" by a SLEEP instruction.

TIME-OUT BIT:
Set to "1" during power up and by the CLRWDT and SLEEP command. This bit is reset to "0" by a watchdog timer time out.

REGISTER PAGE SELECT BITS FOR DIRECT ADDRESSING:

RP1,0: 00 : page 0 (00h - 7Fh)
01 : page 1 (80h - FFh)
10 : page 2 (100h - 17Fh)
11 : page 3 (180h - 1FFh)

Each page is 128 bytes.
Only RP0 is useful in PIC16C71. Bit RP1 can be used as a general purpose read/write bit. However, this may affect upward compatibility with future products.

REGISTER PAGE SELECT BITS FOR INDIRECT ADDRESSING:

IRP: 0 : page 0,1 (00h - FFh)
1 : page 2,3 (100h - 1FFh)

This bit is effectively not used in the PIC16C71.
It may be used as a general purpose read/write bit. However, this may affect upward compatibility with future product.

3.10 Arithmetic and Logic Unit (ALU)

The ALU is 8 bit wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. In two-operand instructions, typically one operand is the working register (W register) or the accumulator. The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

3.11 W Register

The W register is an 8-bit working register (or accumulator) used for ALU operations. It is not an addressable register.

3.12 INTERRUPTS

The PIC16C71 has four sources of interrupt: external interrupt from RB0/INT pin, RTCC timer/counter overflow interrupt, end of conversion interrupt from A/D module, and interrupt on change on RB<7:4> pins. The interrupt control register (INTCON, addr 0Bh) records individual interrupt requests in flag bits. It also has individual and global mask bits. The only exception is A/D conversion completion interrupt flag (ADIF) which resides in ADCON register.

A global interrupt enable bit, GIE (bit 7, INTCON) enables (if = 1) all un-masked interrupts or disables (if = 0) all interrupts. Individual interrupts can be disabled through their corresponding mask bit in INTCON register. GIE is cleared on reset.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-

FIGURE 3.12.1 - INTERRUPT LOGIC

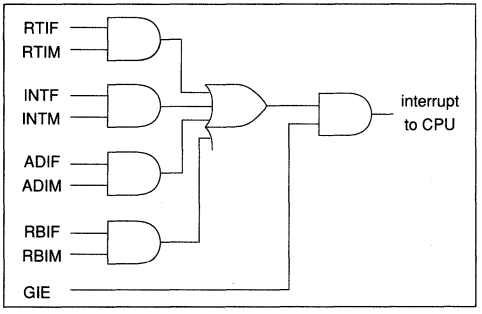
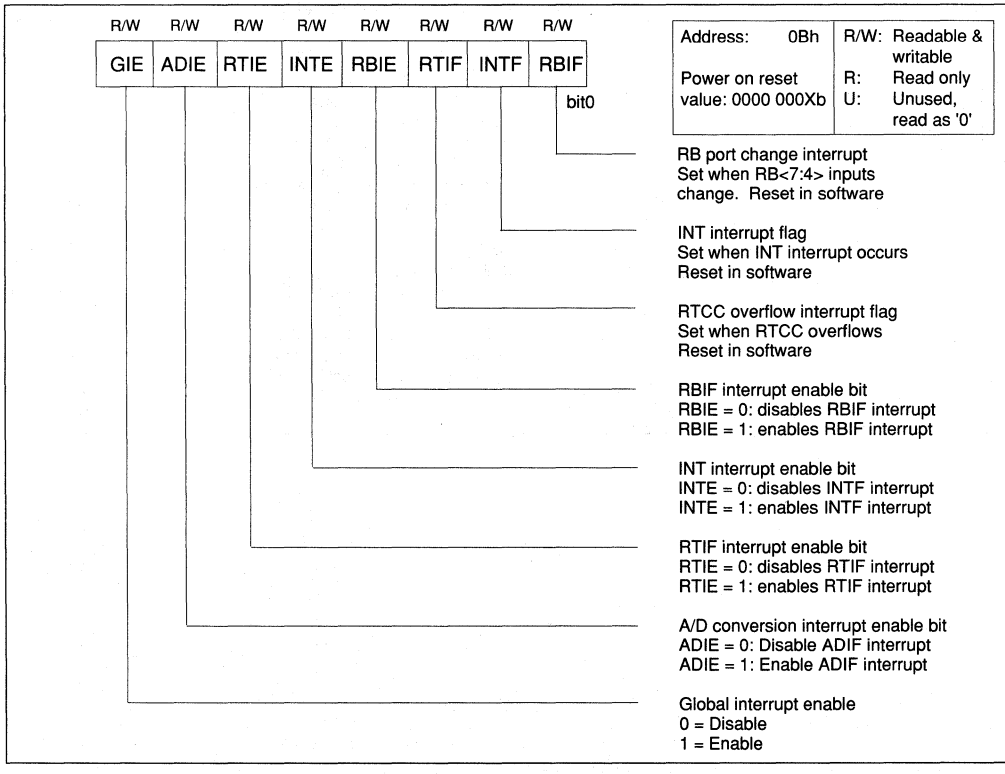


FIGURE 3.12.2 - INTCON REGISTER



enabling interrupts to avoid recursive interrupts. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

The "return from interrupt" instruction, RETFIE, exits interrupt routine as well as sets the GIE bit to re-enable interrupts.

3.12.1 INT Interrupt

External interrupt on RB0/INT pin is edge triggered: either rising (if INTEDG = 1, bit6 of OPTION register) or falling (if INTEDG = 0). When a valid edge appears on INT pin, INTF bit is set (bit1, INTCON register). This interrupt can be disabled by setting INTE control bit (bit4, INTCON) to '0'. INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake up the processor from SLEEP if INTE bit was set to '1' prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See section 5.5 for details on SLEEP.

3.12.2 RTCC Interrupt

RTCC interrupt is generated when the RTCC timer/counter overflows from FFh to 00h. It sets the RTIF bit (bit2, INTCON). The interrupt can be masked by setting RTIE bit (bit5, INTCON) to '0'. RTIF bit must be cleared in software in the RTCC interrupt service routine before re-enabling this interrupt. The RTCC interrupt can not wake the processor from SLEEP since the timer is shut off during SLEEP.

3.12.3 Port RB Interrupt

Port B has an interrupt on change feature on four of its pins, RB<7:4>. When configured as input, the inputs on these pins are compared with the old latched value in every instruction cycle. An active high output is generated on mismatch between the pin and the latch. The "mismatch" outputs of RB4, RB5, RB6 and RB7 are OR'ed together to generate the RBIF interrupt (latched in bit0, INTCON). Any pin configured as output is excluded from the comparison. This interrupt can wake the chip up from SLEEP. The user, in interrupt service routine can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing RBIM (bit3, INTCON) bit.

b) Read Port B. This will end mismatch condition. Next, clear RBIF bit.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression.

3.13 A/D INTERRUPT

The A/D converter sets the end of conversion interrupt flag, ADIF (bit1, ADCON) when a conversion is complete. The interrupt can be masked by setting ADIE bit (bit6, INTCON) to '0'. See section 6.6 for details on A/D interrupt.

4.0 INSTRUCTION SET SUMMARY

Each PIC instruction is a 14-bit word divided into an OP CODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC instruction set summary in Table 4.1 lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which file register is to be utilized by the instruction.

The destination designator specifies where the result of the operation is to be placed. If "d" is zero, the result is placed in the W register. If "d" is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.
For literal and control operations, "k" represents an eight or eleven bit constant or literal value.

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µsec. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µsec.

Notes to Table 4.1

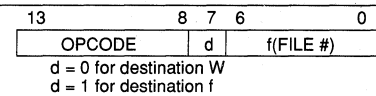
Note 1: The PIC16C71 has 35 instructions. Two additional instructions, TRIS and OPTION, are included only for compatibility with the PIC16C5X products. Their use in new code is strongly recommended against since TRIS and OPTION are made addressible registers, the user may simply write to them. These instructions may not be supported in future PIC16CXX products.

Note 2: When an I/O register is modified as a function of itself (e.g. MOVF 6,1), the value used will be that value present on the pins themselves. For example, if the data latch is "1" for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

Note 3: If this instruction is executed on file register f1 (and, where applicable, d=1), the prescaler will be cleared if assigned to the RTCC.

4.1 INSTRUCTION SET

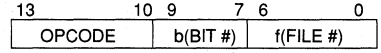
BYTE-ORIENTED FILE REGISTER OPERATIONS



d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Instruction-Binary	(Hex)	Name	Mnemonic, Operands		Operation	Status affected	Notes
00 0111 dfff ffff	07ff	Add W and f	**ADDWF**	**f, d**	W + f → d	C, DC, Z	2,3
00 0101 dfff ffff	05ff	AND W and f	**ANDWF**	**f, d**	W & f → d	Z	2,3
00 0001 1fff ffff	018f	Clear f	**CLRF**	**f**	0 → f	Z	3
00 0001 0XXX XXXX	0100	Clear W	**CLRW**	**-**	0 → W	Z	
00 1001 dfff ffff	09ff	Complement f	**COMF**	**f, d**	$\bar{f}$ → d	Z	2,3
00 0011 dfff ffff	03ff	Decrement f	**DECF**	**f, d**	f -1 → d	Z	2,3
00 1011 dfff ffff	0Bff	Decrement f,Skip if Zero	**DECFSZ**	**f, d**	f - 1 → d, skip if zero	None	2,3
00 1010 dfff ffff	0Aff	Increment f	**INCF**	**f, d**	f + 1 → d	Z	2,3
00 1111 dfff ffff	0Fff	Increment f,Skip if zero	**INCFSZ**	**f, d**	f + 1 → d, skip if zero	None	2,3
00 0100 dfff ffff	04ff	Inclusive OR W and f	**IORWF**	**f, d**	W v f → d	Z	2,3
00 1000 dfff ffff	08ff	Move f	**MOVF**	**f, d**	f → d	Z	2,3
00 0000 1fff ffff	008f	Move W to f	**MOVWF**	**f**	W → f	None	3
00 0000 0XX0 0000	0000	No Operation	**NOP**	**-**	-	None	
00 1101 dfff ffff	0Dff	Rotate left f	**RLF**	**f, d**	f(n)→d(n+1), C →d(0), f(7) →C	C	2,3
00 1100 dfff ffff	0Cff	Rotate right f	**RRF**	**f, d**	f(n)→d(n-1), C→d(7), f(0)→C	C	2,3
00 0010 dfff ffff	02ff	Subtract W from f	**SUBWF**	**f, d**	f - W → d [f + $\overline{W}$ + 1 → d]	C, DC, Z	2,3
00 1110 dfff ffff	0Eff	Swap halves f	**SWAPF**	**f, d**	f(0-3) ↔ f(4-7) → d	None	2,3
00 0110 dfff ffff	06ff	Exclusive OR W and f	**XORWF**	**f, d**	W ⊕ f → d	Z	2,3

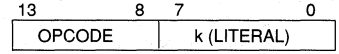
BIT-ORIENTED FILE REGISTER OPERATIONS



b = 3-bit bit address
f = 7-bit file register address

01 00bb bfff ffff	1bff	Bit Clear f	**BCF**	**f, b**	0 → f(b)	None	2,3
01 01bb bfff ffff	1bff	Bit Set f	**BSF**	**f, b**	1 → f(b)	None	2,3
01 10bb bfff ffff	1bff	Bit Test f,Skip if Clear	**BTFSC**	**f, b**	Test bit (b) in file (f): Skip if clear	None	
01 11bb bfff ffff	1bff	Bit Test f, Skip if Set	**BTFSS**	**f, b**	Test bit (b) in file (f): Skip if set	None	

LITERAL AND CONTROL OPERATIONS



k = 8-bit immediate value.

11 111X kkkk kkkk	3Ekk	Add literal to W	**ADDLW**	**k**	k + W → W	C,DC,Z	
11 1001 kkkk kkkk	39kk	AND Literal and W	**ANDLW**	**k**	k & W→ W	Z	
10 0kkk kkkk kkkk	2kkk	Call subroutine	**CALL**	**k**	PC + 1 → TOS, k → PC <10:0>, PCLATH <4:3> → PC <12:11>;	None	
00 0000 0110 0100	0064	Clear Watchdog timer	**CLRWDT**	**-**	0→WDT(and prescaler,if assigned)	TO, PD	
10 1kkk kkkk kkkk	2kkk	Go To address	**GOTO**	**k**	k → PC <10:0>, PCLATH <4:3> → PC <12:11>;	None	
11 1000 kkkk kkkk	38kk	Incl. OR Literal and W	**IORLW**	**k**	k v W → W	Z	
11 00XX kkkk kkkk	30kk	Move Literal to W	**MOVLW**	**k**	k → W	None	
00 0000 0000 1001	0009	Return from interrupt	**RETFIE**	**-**	TOS → PC, '1' → GIE	None	
11 01XX kkkk kkkk	34kk	Return, place literal in W	**RETLW**	**k**	k → W, TOS→ PC	None	
00 0000 0000 1000	0008	Return from subroutine	**RETURN**	**-**	TOS → PC	None	
00 0000 0110 0011	0063	Go into standby mode	**SLEEP**	**-**	0 → WDT, stop oscillator	TO, PD	
11 110X kkkk kkkk	3Ckk	Subtract W from literal	**SUBLW**	**k**	k - W → W	C,DC,Z	
11 1010 kkkk kkkk	3Akk	Excl. OR Literal and W	**XORLW**	**k**	k ⊕ W → W	Z	
00 0000 0110 0010	0062	Load OPTION register	**OPTION**	**-**	W → OPTION register	None	1
00 0000 0110 0fff	006f	Tristate port f	**TRIS**	**f**	W→ I/O control register f	None	1

X = 0 or 1. The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all software tools.
Notes: See previous page

4.2 INSTRUCTION DESCRIPTION

ADDLW Add Literal to W

Syntax: ADDLW k

Encoding:	11	111X	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W + k) → W

Status bits: C, DC, Z

Description: The contents of the W register are added to the eight bit literal "k" and the result is placed in the W register.

ADDWF ADD W to f

Syntax: ADDWF f,d

Encoding:	00	0111	dfff	ffff

Words: 1

Cycles: 1

Operation: (W + f) → d

Status bits: C, DC, Z

Description: Add the contents of the W register to register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

ANDLW AND Literal and W

Syntax: ANDLW k

Encoding:	11	1001	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .AND. k) → W

Status bits: Z

Description: The contents of W register are AND'ed with the eight bit literal "k". The result is placed in the W register.

ANDWF AND W with f

Syntax: ANDWF f,d

Encoding:	00	0101	dfff	ffff

Words: 1

Cycles: 1

Operation: (W .AND. f) → d

Status bits: Z

Description: AND the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

BCF Bit Clear f

Syntax: BCF f,b

Encoding:	01	00bb	bfff	ffff

Words: 1

Cycles: 1

Operation: 0 → f(b)

Status bits: None

Description: Bit "b" in register "f" is reset to 0.

BSF Bit Set f

Syntax: BSF f,b

Encoding:	01	01bb	bfff	ffff

Words: 1

Cycles: 1

Operation: 1 → f(b)

Status bits: None

Description: Bit "b" in register "f" is set to 1.

BTFSC Bit Test, skip if Clear

Syntax: BTFSC f,b

Encoding:	01	10bb	bfff	ffff

Words: 1

Cycles: 1(2)

Operation: skip if f(b) = 0

Status bits: None

Description: If bit "b" in register "f" is "0" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

BTFSS Bit Test, skip if Set

Syntax: BTFSS f,b

Encoding:	01	11bb	bfff	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f(b) = 1

Status bits: None

Description: If bit "b" in register "f" is "1" then the next instruction is skipped.

If bit "b" is "1", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

CALL Subroutine Call

Syntax: CALL k

Encoding:	10	0kkk	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC + 1 → TOS, k → PC<10:0>, PCLATH<4:3> → PC<12:11>;

Status bits: None

Description: Subroutine call. First, return address (PC + 1) is pushed into the stack. The eleven bit value is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH (f03). CALL is a two cycle instruction.

CLRF Clear f

Syntax: CLRF f

Encoding:	00	0001	1fff	ffff

Words: 1

Cycles: 1

Operation: 00h → f

Status bits: Z

Description: The contents of register "f" are set to 0.

CLRW Clear W Register

Syntax: CLRW

Encoding:	00	0001	0XXX	XXXX

Words: 1

Cycles: 1

Operation: 00h →W

Status bits: Z

Description: W registered is cleared. Zero bit (Z) is set.

CLRWDT Clear Watchdog Timer

Syntax: CLRWDT

Encoding:	00	0000	0110	0100

Words: 1

Cycles: 1

Operation: 00h →WDT, 0 → WDT prescaler,

Status bits: 1 → TO, 1 → PD

Description: CLRWDT instruction resets the watchdog timer.It also resets the prescaler of the WDT. Status bits TO and PD are set.

COMF Complement f

Syntax: COMF f,d

Encoding:	00	1001	dfff	ffff

Words: 1

Cycles: 1

Operation: $\bar{f}$ → d

Status bits: Z

Description: The contents of register "f" are complemented. If "d" is 0 the result is stored in W. If "d" is 1 the result is stored back in register "f".

DECF Decrement f

Syntax: DECF f,d

Encoding:	00	0011	dfff	ffff

Words: 1

Cycles: 1

Operation: (f-1) → d

Status bits: C, DC, Z

Description: Decrement register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

DECFSZ Decrement f, skip if 0

Syntax: DECFSZ f,d

Encoding:	00	1011	dfff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f - 1) → d; skip if result = 0

Status bits: None

Description: The contents of register "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

GOTO Unconditional Branch

Syntax: GOTO k

Encoding:	10	1kkk	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → PC<10:0>, PCLATH<4:3> → PC<12:11>

Status bits: None

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH <4:3>. GOTO is a two cycle instruction.

INCF Increment f

Syntax: INCF f,d

Encoding:

00	1010	dfff	ffff

Words: 1

Cycles: 1

Operation: (f + 1) → d

Status bits: C, DC, Z

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

INCFSZ Increment f, skip if 0

Syntax: INCFSZ f,d

Encoding:

00	1111	dfff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f + 1) → d, skip if result = 0

Status bits: None

Description: The contents of register "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

IORLW Inclusive OR Literal with W

Syntax: IORLW k

Encoding:

11	1000	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .OR. k) → W

Status bits: Z

Description: The contents of the W register are OR'ed with the eight bit literal "k". The result is placed in the W register.

IORWF Inclusive OR W with f

Syntax: IORWF f,d

Encoding:

00	0100	dfff	ffff

Words: 1

Cycles: 1

Operation: (W .OR. f) → d

Status bits: Z

Description: Inclusive OR the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

MOVLW Move Literal to W

Syntax: MOVLW k

Encoding:

11	00XX	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → W

Status bits: None

Description: The eight bit literal "k" is loaded into W register.

MOVF Move f

Syntax: MOVF f,d

Encoding:

00	1000	dfff	ffff

Words: 1

Cycles: 1

Operation: f → d

Status bits: Z

Description: The contents of register f is moved to destination d. If d=0, destination is W register. If d = 1, the destination is file register f itself. It is useful, however, to test a file register since status flag Z is affected.

MOVWF Move W to f

Syntax: MOVWF f

Encoding:

00	0000	1fff	ffff

Words: 1

Cycles: 1

Operation: W → f

Status bits: None

Description: Move data from W register to register "f".

NOP No Operation

Syntax: NOP

Encoding:

00	0000	0XX0	0000

Words: 1

Cycles: 1

Operation: No operation

Status bits: None

Description: No operation

OPTION Load Option Register

Syntax: OPTION

Encoding:	00	0000	0110	0010

Words: 1

Cycles: 1

Operation: W → OPTION;

Status bits: None

Description: The contents of the W register is loaded in the OPTION register. Refer to Fig. 6.5.1 for OPTION register settings.

This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it. To maintain upward compatibility with future PIC16CXX products, **do not use this instruction.**

RETFIE Return from Interrupt

Syntax: RETFIE

Encoding:	00	0000	0000	1001

Words: 1

Cycles: 2

Operation: TOS → PC, 1 → GIE;

Status bits: GLINTD

Description: Return from Interrupt. Stack is popped and Top of the Stack (TOS) is loaded in PC. Interrupts are enabled by setting the GIE bit. GIE is the global interrupt enable bit (bit 7, register INTCON). This is a two cycle instruction.

RETLW Return Literal to W

Syntax: RETLW k

Encoding:	11	01XX	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → W; TOS → PC;

Status bits: None

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

RETURN Return from Subroutine

Syntax: RETURN

Encoding:	00	0000	0000	1000

Words: 1

Cycles: 2

Operation: TOS → PC;

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

RLF Rotate Left f through Carry

Syntax: RLF f,d

Encoding:	00	1101	dfff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>, f<7> → C, C → d<0>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in register "f".

RRF Rotate Right f through Carry

Syntax: RRF f,d

Encoding:	00	1100	dfff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>, f<0> → C, C → d<7>;

Status bits: C

Description: The contents of register "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed back in register "f".

SLEEP

Syntax: SLEEP

Encoding:	00	0000	0110	0011

Words: 1

Cycles: 1

Operation: 0 → PD, 1 → TO;
00h → WDT, 0 → WDT prescaler;

Status bits: TO, PD

Description: The power down status bit (PD) is cleared. Time-out status bit (TO) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

SUBLW Subtract W from Literal

Syntax: SUBLW k

Encoding:	11	110X	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (k - W) → W

Status bits: C, DC, Z

Description: The W register is subtracted (2's complement method) from the eight bit literal "k". The result is placed in the W register.

```
Example
;SUBLW Example #1
;
MOVLW   0x01    ;wreg=1
SUBLW   0x02    ;wreg= 2-wreg = 2-1=1
                ;Carry=1: result is positive
;
;SUBLW Example #2
;
MOVLW   0x02    ;wreg=2
SUBLW   0x01    ;wreg=1-wreg=1-2=FFh
                ;Carry=0: Result is negative
```

SUBWF Subtract W from f

Syntax: SUBWF f,d

Encoding:	00	0010	dfff	ffff

Words: 1

Cycles: 1

Operation: (f-W) → d

Status bits: C, DC, Z

Description: Subtract (2's complement method) the W register from register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

```
Example:
;SUBWF Example #1
;
clrf    0x20    ;f(20h)=0
movlw   1       ;wreg=1
subwf   0x20    ;f(20h)=f(20h)-wreg=0-1=FFh
                ;Carry=0:Result is negative
;
;SUBWF Example #2
movlw   0xFF
movwf   0x20    ;f(20h)=FFh
clrw            ;wreg=0
subwf   0x20    ;f(20h)=f(20h)-wreg=FFh-0=FFh
                ;Carry=1: Result is positive
```

SWAPF Swap f

Syntax: SWAPF f,d

Encoding:	00	1110	dfff	ffff

Words: 1

Cycles: 1

Operation: f<0:3> → d<4:7>, f<4:7> → d<0:3>;

Status bits: None

Description: The upper and lower nibbles of register "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is placed in register "f".

TRIS Load TRIS Register

Syntax: TRIS f

Encoding:	00	0000	0110	0fff

Words: 1

Cycles: 1

Operation: W → I/O Control Register f

Status bits: None

Description: The I/O Control Register (or data direction register of the I/O port) is loaded with the contents of the W register.

The TRIS instruction configures an I/O port to either output or input (high-impedance). The valid values for "f" are 5 & 6 for PIC16C71.

This instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them. To maintain upward compatibility with future PIC16CXX products, **do not use this instruction**.

A '1' in the TRIS register configures the corresponding port pin as an input. A '0' in the TRIS register configures the corresponding port pin as an output.

```
Example:
MOVLW   0x0F
TRIS    6
```

I/O Port B (F6) is configured such that the 4 pins corresponding to the LSBs of Port B are inputs (h-impedance) and the other 4 pins are outputs.

XORLW Exclusive OR literal with W

Syntax: XORLW k

Encoding:	11	1010	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .XOR. k) → W

Status bits: Z

Description: The contents of the W register are XOR'ed with the eight bit literal "k". The result is placed in the W register.

XORWF Exclusive OR W with f

Syntax: XORWF f,d

Encoding:	00	0110	dfff	ffff

Words: 1

Cycles: 1

Operation: (W .XOR. f) → d

Status bits: Z

Description: Exclusive OR the contents of the W register with register "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in register "f".

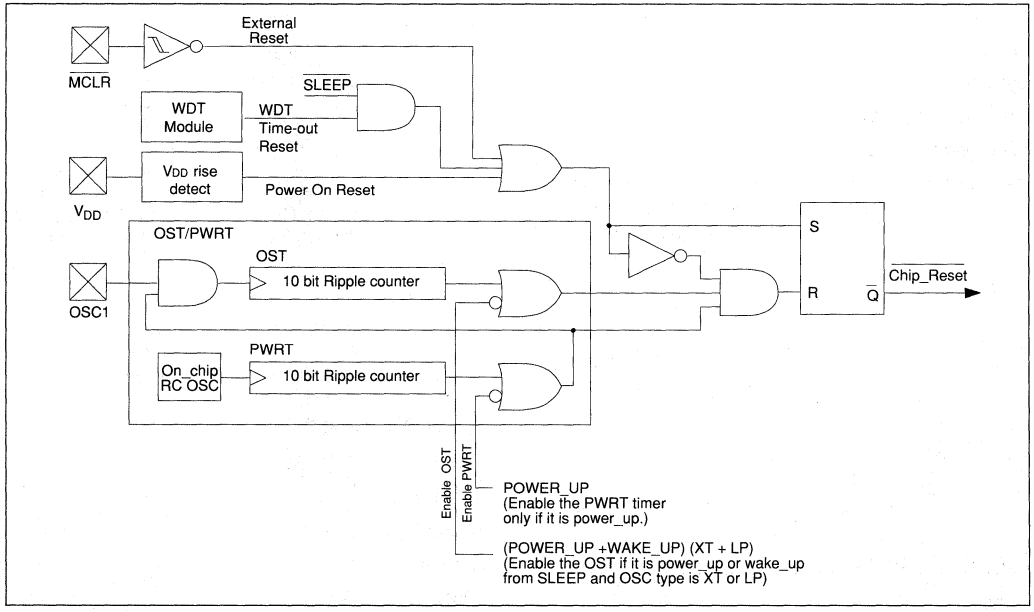
5.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors are special circuits to deal with the needs of real time applications. The PIC16C71 has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

The PIC16C71 has a watchdog timer which can be shut off only through EPROM fuses. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the oscillator start-up timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the power-up timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset, watchdog timer time-out or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of EPROM configuration bits (fuses) are used to select various options (section 5.6).

FIGURE 5.0.1 - SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



5.1 RESET

The PIC16C71 differentiates between various kinds of reset:

a) Power on reset (POR)

b) MCLR Reset during normal operation

c) MCLR reset during SLEEP

d) WDT time-out reset during normal operation

e) WDT time-out reset during SLEEP

Some registers are not reset in any way; they are unknown on POR and unchanged in any other reset. Most other registers are reset to "reset state" on power-on reset (POR), on MCLR or WDT reset during normal operation and on MCLR reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as resume of normal operation. There are a few exceptions to this. The PC is always reset to all 0's (0000h). Finally, TO and PD bits are set or cleared differently in different reset situations as indicated in section 3.8.1. These bits are used in software to determine the nature of reset. See Table 5.1.1 for a full description of reset states of all registers.

5.2 Power-on-reset (POR), Power-up-timer (PWRT) and Oscillator Start-up timer (OST)

Power-on-reset (POR): A power-on-reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V - 2.0V). To take advantage of the POR, just tie MCLR pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create power-on-reset.

TABLE 5.1.1 RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on reset (POR)	WDT time-out reset during normal operation	WDT time-out reset during SLEEP	MCLR reset during normal	MCLR reset during SLEEP	Wake-up through interrupt
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
INDIR	00h	-	-	-	-	-	-
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PC	02h	0000h	0000h	PC + 1	0000h	0000h	PC + 1
STATUS	03h	0001 1xxx	0000 1uuu	uuu0 0uuu	000u uuuu	000u 0uuu	uuu1 0uuu
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PORT A	05h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TRIS A	85h	---1 1111	---1 1111	---u uuuu	---1 1111	---1 1111	---u uuuu
TRIS B	86h	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111	uuuu uuuu
OPTION	81h	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111	uuuu uuuu
ADCON0	08h	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu
ADCON1	88h	---- --00	---- --00	---- --uu	---- --00	---- --00	---- --uu
ADRES	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu	0000 000u	0000 0000	uuuu uuuu*

Legend: - = unimplemented, reads as '0'
u = unchanged
x = unknown

* In the event of wake-up through interrupt, one or more of the interrupt flags will be set. Other bits in INTCON will remain unchanged.

The POR circuit does not produce internal reset when VDD declines (or goes through a brown-out).

Power-up Timer (PWRT): The power-up timer provides a fixed 72ms time-out on power-up only, from POR. The power-up timer operates on an internal RC oscillator. The chip is kept in reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration fuse, PWRTE can enable (if = 1) or disable (if = 0 or programmed) the power-up timer (section 5.6).

The power-up time delay will vary from chip to chip and due to VDD and temperature. See DC parameters for details.

Oscillator Start-up Timer (OST): The oscillator start-up timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This guarantees that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on power-on reset or wake-up from SLEEP.

Time-out Sequence: On power up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then TOST is activated. The total time-out will vary based on oscillator configuration and PWRTE fuse status. For example, in RC mode with PWRTE set to '0' (PWRT disabled), there will be no time-out at all. Figures 5.2.1 and 5.2.2 depict time-out sequences.

Since the time-outs occur from POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately. This is useful for testing purposes or to synchronize more than one PIC operating in conjunction.

TABLE 5.2.1 - TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power up		Wake up from SLEEP
	PWRTE = 1	PWRTE = 0	
XT, HS, LP	72 ms + 1024 tosc	1024 tosc	1024 tosc
RC	72 ms	-	-

FIGURE 5.2.1 TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): Case 1

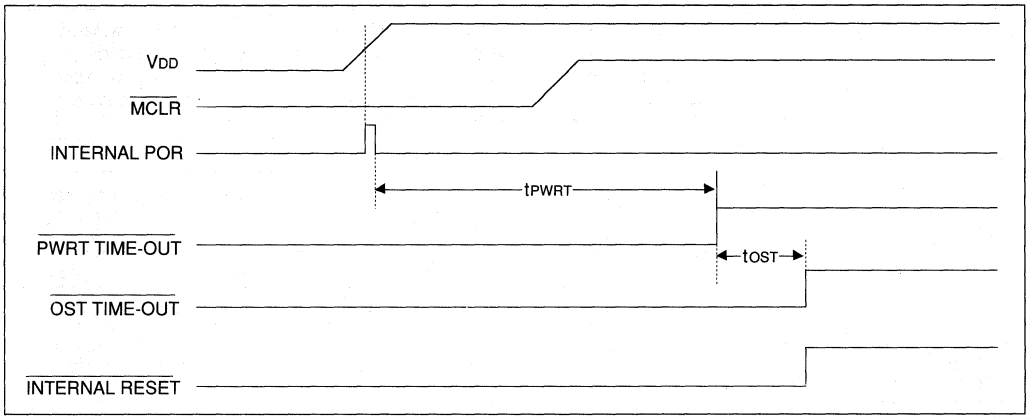


FIGURE 5.2.2 TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): Case 2

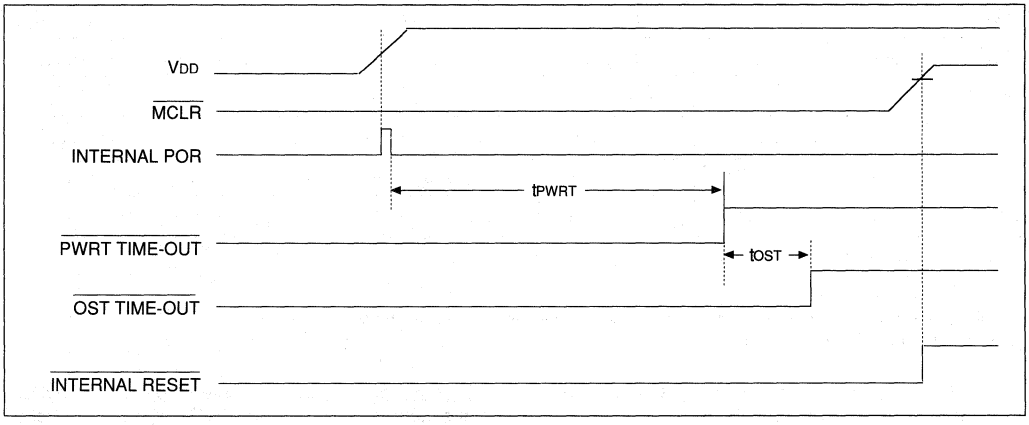


FIGURE 5.2.3 TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

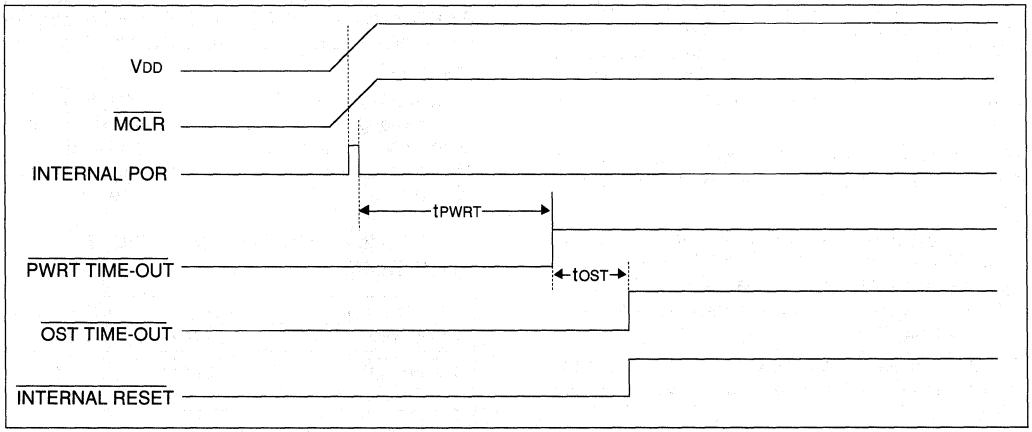
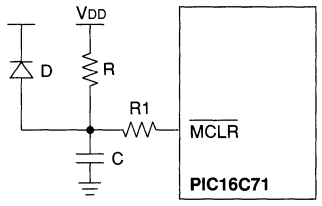


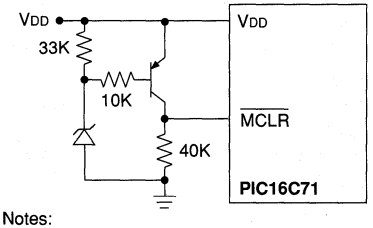
FIGURE 5.2.4 - EXTERNAL POWER ON RESET CIRCUIT



Notes:

1. External power on reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
2. R < 40 KΩ is recommended to make sure that voltage drop across R does not exceed 0.2 V (max leakage current spec on MCLR pin is 5 μA). A larger voltage drop will degrade VIH level on MCLR pin.
3. R1= 100Ω to 1KΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to ESD or EOS.

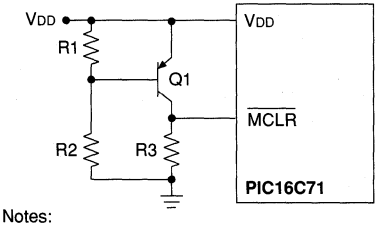
FIGURE 5.2.5 - BROWN OUT PROTECTION CIRCUIT 1



Notes:

1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 5.2.6 - BROWN OUT PROTECTION CIRCUIT 2



Notes:

1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$VDD \cdot \frac{R1}{R1 + R2} = 0.7\ V.$$

5.3 WATCHDOG TIMER (WDT)

The watchdog timer is realized as a free running on-chip RC oscillator which does not require any external components. That means that the WDT will run, even if the clock on the OSC1/OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. A WDT timeout generates a device RESET condition. The WDT can be permanently disabled by programming the configuration fuse WDTE as a '0' (section 5.6).

5.3.1 WDT Period

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.5 seconds can be realized.

The "CLRWDT" and "SLEEP" instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

The status bit "TO" in file register f3 will be cleared upon a watchdog timer timeout.

5.3.2 WDT Programming Considerations

In a noisy application environment the OPTION register can get corrupted. The OPTION register should be updated at regular intervals.

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT timeout occurs.

5.4 OSCILLATOR CONFIGURATIONS

5.4.1 Oscillator Types

The PIC16C71 can be operated in 4 different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes.

5.4.2 Crystal Oscillator

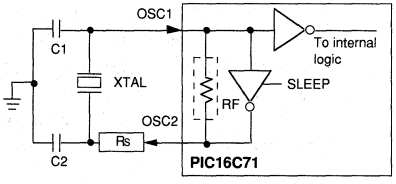
In XT, HS, or LP modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 5.4.1).

TABLE 5.4.1 - CAPACITOR SELECTION FOR CERAMIC RESONATORS

Oscillator Type	Resonator Frequency	Capacitor Range C1 = C2
XT	455 KHz	150 - 330 pF
	2.0 MHz	20 - 330 pF
	4.0 MHz	20 - 330 pF
HS	8.0 MHz	20 - 200 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

FIGURE 5.4.1 - CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



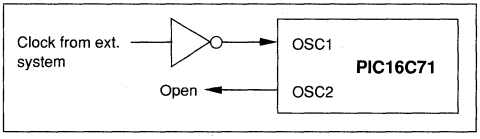
Rs is recommended for "HS" devices (100Ω < Rs < 1K). Rs may also be used in XT mode for AT strip-cut crystalg. See Tables 5.4.1 and 5.4.2 for recommended values of C1, C2 and Rs.

TABLE 5.4.2 - CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 KHz	15 pF	15 pF
	100 KHz	15 pF	15 pF
	200 KHz	0 - 15 pF	0 - 15 pF
XT	100 KHz	15 - 30 pF	200 - 300 pF
	200 KHz	15 - 30 pF	100 - 200 pF
	455 KHz	15 - 30 pF	15 - 100 pF
	1 MHz	15 - 30 pF	15 - 30 pF
	2 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

FIGURE 5.4.2 - EXTERNAL CLOCK INPUT OPERATION (HS, XT, or LP OSC CONFIGURATION)



5.4.3 RC Oscillator

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operation temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation to due tolerance of external R and C components used. Figure 5.4.3 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 kOhm, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g. 1 MOhm), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep Rext between 5 kOhm and 100 kOhm.

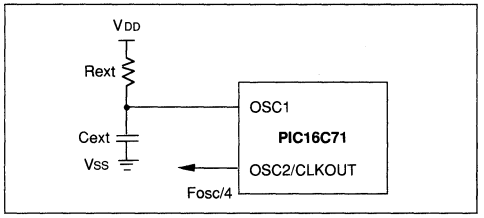
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See table in section 9.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See characteristics in section 9.0 for variation of oscillator frequency due to V_{DD} for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3.2.1 for timing).

FIGURE 5.4.3 - RC OSCILLATOR (RC TYPE ONLY)



5.5 POWER DOWN MODE (SLEEP)

The power down mode is entered by executing a SLEEP instruction.

If enabled, the watchdog timer will be cleared but keeps running, the bit "PD" in the status register (f03) is cleared, the "TO" bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP command was executed (driving high, low, or hi-impedance).

For lowest curent consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin. I/O pins that are in the High-Z mode should be pulled high or low externally to avoid switching currents caused by floating inputs. The RTCC input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PortB should be considered.

The $\overline{\text{MCLR}}$ pin must be at a logic high level (VIHMC).

It should be noted that a RESET generated by a WDT time out does not drive $\overline{\text{MCLR}}$ pin low.

5.5.1 Wake-up from SLEEP

The device can wake up from SLEEP through one of the following events:

a. External reset input on $\overline{\text{MCLR}}$ pin

b. Watchdog timer timeout reset (if WDT was enabled)

c. Interrupt from INT pin, RB port change or A/D converter.

The first event will cause a device reset. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device reset. PD bit, which is set on power-up is cleared when SLEEP is invoked. TO bit is cleared if WDT time-out occurred (and caused wake-up).

For the device to wake up through an interrupt, the corresponding interrupt mask bit must be enabled. On wake-up, the device will continue to execute code in-line if global interrupt was disabled (GIE = 0) or branch to interrupt service routine if GIE was enabled.

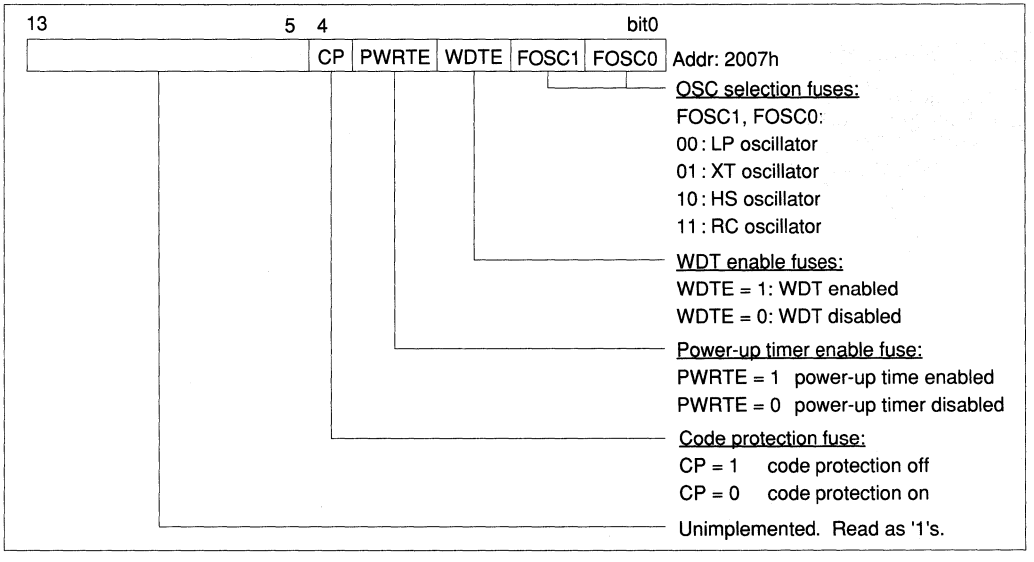
5.6 CONFIGURATION FUSES

The PIC16C71 has five configuration fuses which are EPROM bits. These fuses can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh). However, through a special mode, this location can be accessed during programming.

See description of fuses in figure 5.6.1.

FIGURE 5.6.1: CONFIGURATION WORD



5.7 ID LOCATIONS

The PIC16C71 has four ID locations (2000h - 2003h) mapped in the test program memory for storing code revision number, manufacturing information or other useful information. As with the configuration word, these locations are readable and writable through a programmer. They are not accessible during normal code execution.

If the chip is code protected, it is recommended that the user uses only the lower seven bits of the ID locations and program the higher seven bits as '1'. This way the ID locations will be readable even after code protection.

5.8 CODE PROTECTION

The code in the program memory can be protected by blowing the code protect fuse (CP).

When code protected, the contents of the program memory cannot be read out in a way that the program code can be reconstructed. In addition, all memory locations starting at 0040h and above are protected against programming.

It is still possible to program locations 0000h - 003Fh, the ID locations and the configuration fuses.

5.8.1 Verifying a Code-protected PIC

When code protected verifying any program memory location will read a scrambled output which looks like "0000000xxxxxxx" (binary) where X is 1 or 0. To verify a device after code protection, follow this procedure:

a. First, program and verify a good device without code protecting it.

b. Next, blow its code protection fuse and then load its contents in a file.

c. Verify any code-protected PIC against this file.

6.0 OVERVIEW OF PERIPHERALS

The PIC16C71 has 13 I/O pins organized as two I/O ports, PortA (5 bit) and PortB (8-bit). It has an 8-bit timer/counter (RTCC) with a programmable 8-bit prescaler and an analog to digital converter module. The A/D converter has up to four analog inputs, internal or external reference, 8 bit resolution and a typical 20µs conversion time.

6.1 PORTA

PortA is a 5 bit wide port with pins RA0 - RA4. Port pins RA<3:0> are bidirectional whereas RA4 has a open-collector output. PortA is file register 05h. Its corresponding direction control register TRISA is mapped in page 1 of register file at address 85h. TRISA is a five-bit wide register with bits <4:0>.

Pins RA<3:0> are multiplexed with analog input channels AIN3 - AIN0. Pin RA3 is further multiplexed with external reference voltage VREF for the ADC. Two bits in control register ADCON1 (file register 88h) are used to configure these pins as digital (i.e. port) or analog pins. When configured as analog inputs, these pins will read as '0's and the TRISA register bits will have no effect. Upon power-on reset, RA<3:0> are configured as analog inputs.

FIGURE 6.1.1 - BLOCK DIAGRAM OF RA0 - RA3 PINS

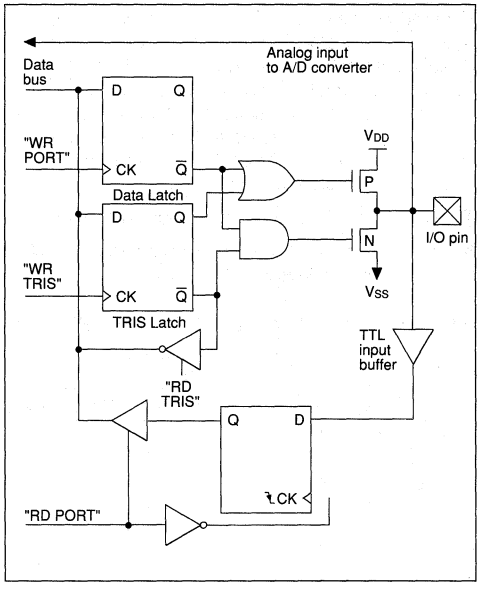


TABLE 6.1.1 - PORTA FUNCTIONS

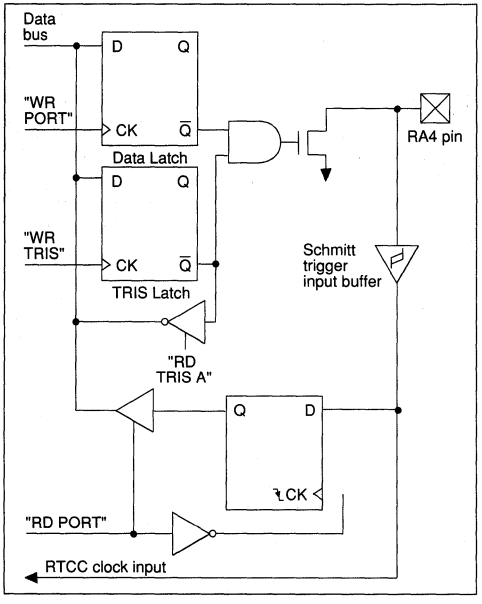
Port Pin	Bit	Pin Function	Alternate Function
RA0/AIN0	bit0	Input/output port. TTL input levels	Analog input channel 0
RA1/AIN1	bit1	Input/output port. TTL input levels	Analog input channel 1
RA2/AIN2	bit2	Input/output port. TTL input levels	Analog input channel 2
RA3/AIN3/VREF	bit3	Input/output port. TTL input levels	Analog input channel 3 or external reference voltage input (VREF)
RA4/RT	bit4	Input/output port. Output is open collector type. Input is Schmitt trigger type.	External clock input for RTCC timer/counter

TABLE 6.1.2 - SUMMARY OF PORTA REGISTERS

Register Name	Function	Address	Power-on Reset Value
PORTA	PortA pins when read PortA latch when written	05h	---X XXXX
TRISA	PortA data direction register	85h, PAGE1	---1 1111
ADCON1	A/D converter control register	88h, PAGE1	---- --00

Notes: 1: x = unknown, - = unimplemented, reads as a '0'.
2: For reset values of registers in other reset situations refer to table 5.1.1.

FIGURE 6.1.2 - BLOCK DIAGRAM OF RA4 PIN



6.2 PORTB

PortB is an 8-bit wide bidirectional port (file register address 06h). The corresponding data direction register is TRISB (address 86h). A '1' in TRISB sets the corresponding port pin as an input. Reading PortB register reads the status of the pins whereas writing to it will write to the port latch.

Each of the PortB pins has a weak internal pull-up (~250 µA typical). The weak pull-up is automatically turned off if the port pin is configured as an output. A single control bit RBPU (bit 7, OPTION register) can turn off (RBPU = 1) all the pull-ups. The pull-ups are disabled on power on reset.

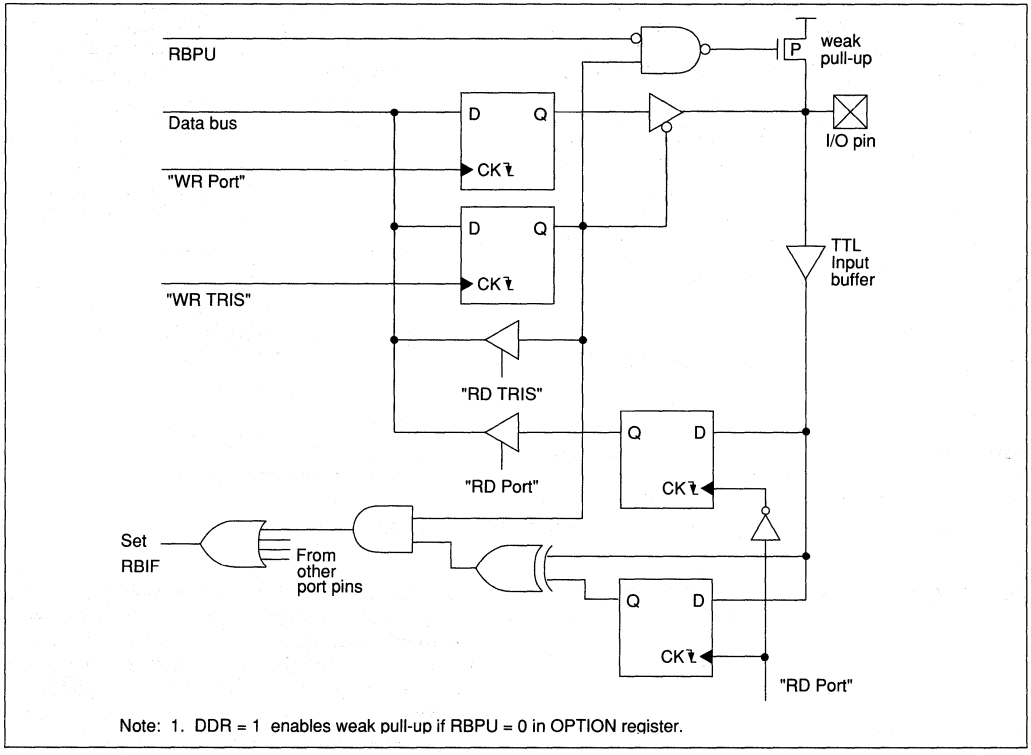
Port B has an interrupt on change feature on four of its pins, RB<7:4>. When configured as input, the inputs on these pins are sampled and latched every Q1. The new input is compared with the old latched value in every instruction cycle. An active high output is generated on mismatch between the pin and the latch. The "mismatch" outputs of RB4, RB5, RB6 and RB7 are OR'ed together to generate the RBIF interrupt (latched in bit0, INTCON). Any pin configured as output is excluded from the comparison. This interrupt can wake the chip up from SLEEP. The user, in interrupt service routine can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing RBIE (bit3, INTCON) bit.

b) Read Port B. This will end mismatch condition. Next, clear RBIF bit.

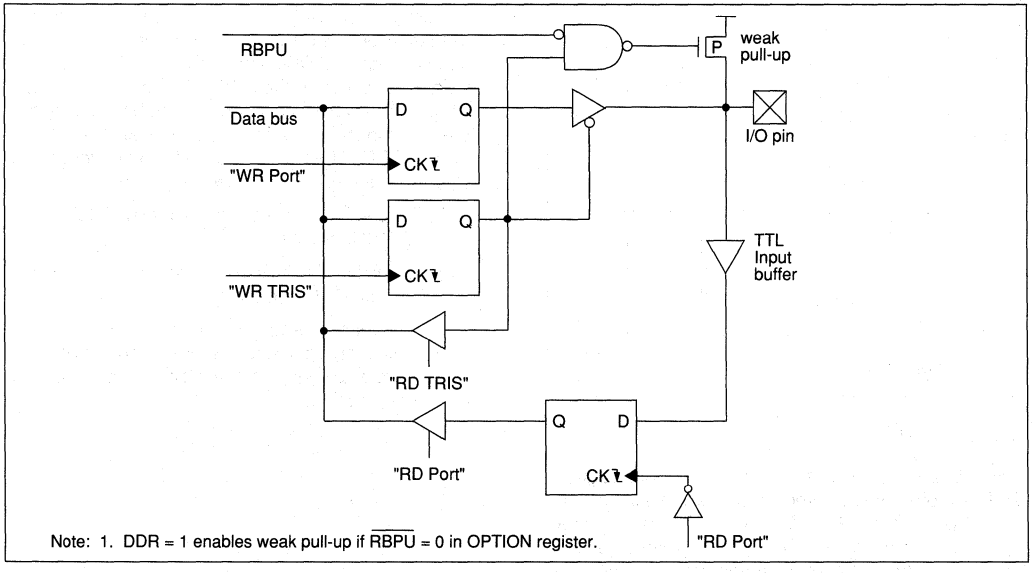
This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression.

FIGURE 6.2.1 - BLOCK DIAGRAM OF PORT PINS RB<7:4>



Note: 1. DDR = 1 enables weak pull-up if RBPU = 0 in OPTION register.

FIGURE 6.2.2 - BLOCK DIAGRAM OF PORT PINS RB<3:0>



Note: 1. DDR = 1 enables weak pull-up if $\overline{RBPU}$ = 0 in OPTION register.

Finally, port pin RB0 is multiplexed with external interrupt input INT.

TABLE 6.2.1 - PORTB FUNCTIONS

Port Pin	Bit	Pin Function	Alternate Function
RB0/INT	bit0	Input/output port pin. TTL input levels and internal software programmable weak pull-up	External interrupt input
RB1	bit1	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB2	bit2	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB3	bit3	Input/output port pin. TTL input levels and internal software programmable weak pull-up	-
RB4	bit4	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB5	bit5	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB6	bit6	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change
RB7	bit7	Input/output port pin. TTL input levels and internal software programmable weak pull-up	Interrupt on port change

TABLE 6.2.2 - SUMMARY OF PORTB REGISTERS

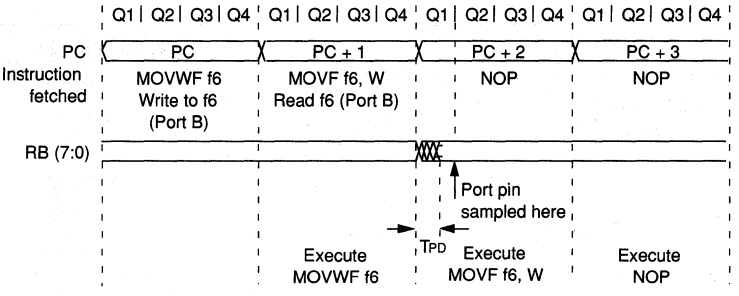
Register Name	Function	Address	Power-on Reset Value
PORTB	PortB pins when read PortB latch when written	06h	XXXX XXXX
TRISB	PortB data direction register	86h	1111 1111
OPTION	Weak pull-up on/off control ($\overline{\text{RBPU}}$ bit)	88h	1111 1111

6.3 I/O PROGRAMMING CONSIDERATIONS

6.3.1 BIDIRECTIONAL I/O PORTS

a) Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of f6 (Port B) will cause all eight bits of f6 to be read into the CPU. Then the BSF operation takes place on bit 5 and f6 is re-output to the output latches. If another bit of f6 is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit 0 is switched into output mode later on, the content of the data latch may now be unknown.

b) A pin actively outputting a "0" or "1" should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.
For "wired-or" outputs (assuming negative logic), it is recommended to use external pull-up resistors on the corresponding pins. The pin should be left in high-impedance mode, unless a "0" has to be output. Thus, external devices can drive this pin "0" as well. "Wired-and" outputs can be realized in the same way, but with external pull-down resistors and only actively driving the "1" level from the PIC. The resistor values are user selectable, but should not force output currents above the specified limits (see DC Characteristics).



Note:

This example shows write to port B followed by a read from port B. Note that the data setup time = (0.25 TCY - TPD) where TCY = instruction cycle. Therefore, at higher clock frequencies, write followed by a read may be problematic.

6.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (see figure 6.3.1). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or an other instruction not accessing this I/O port.

6.3.3 OPERATION IN NOISY ENVIRONMENT

In noisy application environments, such as keyboards which are exposed to ESD (Electro Static Discharge), register contents can get corrupted due to noise spikes. The on-chip watchdog timer will take care of all situations involving program sequence "lock-ups." However, if an I/O control register gets corrupted, the program sequence may still be executed properly although an input pin may have switched unintentionally to an output. In this case, the program would always read the same value on this pin. This may result, for example, in a keyboard "lock-up" situation without leading to a watchdog timer timeout. Thus, it is recommended to redefine all I/O pins in regular time intervals (inputs as well as outputs). The optimal strategy is to update the I/O control register every time before reading input data or writing output data .

6.4 Real Time Clock/Counter (RTCC)

The RTCC timer/counter has the following features:

- 8 bit timer/counter
- Readable and writable (file address 01h)
- 8 bit software programmable prescaler
- Internal or external clock select

Figure 6.4.1 is a simplified block diagram of the RTCC module.

Timer mode is selected by setting RTS bit to '0' (OPTION register). In timer mode, the RTCC will increment every instruction cycle (without prescaler). If RTCC (f01) is written, increment is inhibited for the following two cycles (see figures 6.4.2 and 6.4.3). The user can work around this by writing an adjusted value to the RTCC.

Counter mode is selected by setting RTS bit to '1' (OPTION register). In this mode RTCC will increment either on every rising or falling edge of pin RA4/RTCC. This is determined by control bit RTE (OPTION register). RTE = 0 selects rising edge. Restrictions on external clock input is discussed in detail in section 6.4.1.

The prescaler is shared between the RTCC and the watchdog timer. The prescaler assignment is controlled in software by control bit, PSA (OPTION register). PSA = 0 will assign the prescaler to RTCC. The prescaler is not readable or writable. When the prescaler is assigned to the RTCC, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.4.2 details the operation of the prescaler.

6.4.1 USING RTCC WITH EXTERNAL CLOCK

When external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements.

Also there is some delay from the occurance of the external clock edge to the actual incrementing of RTCC. Referring to Figure 6.4.1.1, the synchronization is done after the prescaler. The output of the prescaler is sampled twice in every instruction cycle to detect rising or falling edges. Therefore, it is necessary for PSOUT to be high for at least 2 tosc and low for at least 2 tosc where tosc = oscillator time period.

When no prescaler is used, PSOUT (Prescaler output, see Figure 5) is the same as RTCC clock input and therefore the requirements are:

TRTH = RTCC high time ≥ 2tosc + 20 ns
TRTL = RTCC low time ≥ 2tosc + 20 ns

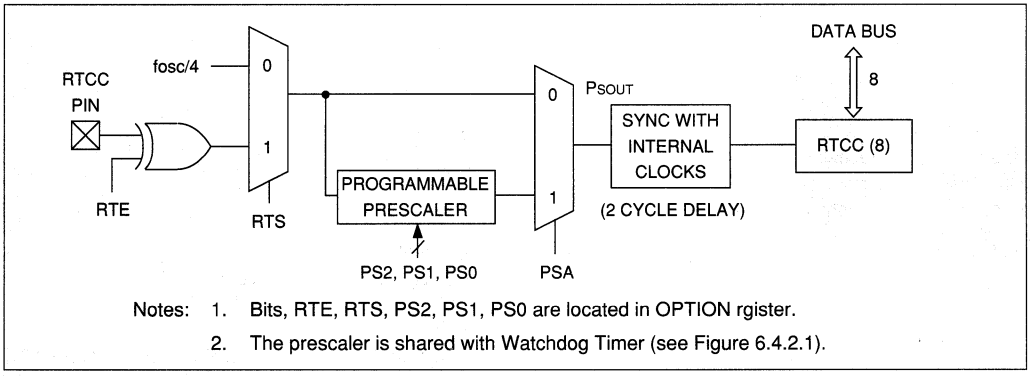
When prescaler is used, the RTCC input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical.
Then: PSOUT high time = PSOUT low time = $\frac{N.T_{RT}}{2}$
where TRT = RTCC input period and N = prescale value (2, 4, ..., 256). The requirement is, therefore $\frac{N.T_{RT}}{2} \geq 2$ tosc + 20 ns, or $T_{RT} \geq \frac{4 \text{ tosc} + 40 \text{ ns}}{N}$.

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on RTCC is too small then the pulse may not be detected, hence a minimum high or low time of 10 ns is required. In summary, the RTCC input requirements are:

TRT = RTCC period ≥ (4 tosc + 40 ns)/N
TRTH = RTCC high time ≥ 10 ns
TRTL = RTCC low time ≥ 10 ns

Delay from external clock edge: Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to Figure 6.4.1.1, the reader can see that this delay is between 3 tosc and 7 tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ±4 tosc (±200 ns @ 20 MHz).

FIGURE 6.4.1 - RTCC BLOCK DIAGRAM (SIMPLIFIED)



Notes: 1. Bits, RTE, RTS, PS2, PS1, PS0 are located in OPTION rgister.
2. The prescaler is shared with Watchdog Timer (see Figure 6.4.2.1).

FIGURE 6.4.2 - RTCC TIMING: INT CLOCK/NO PRESCALE

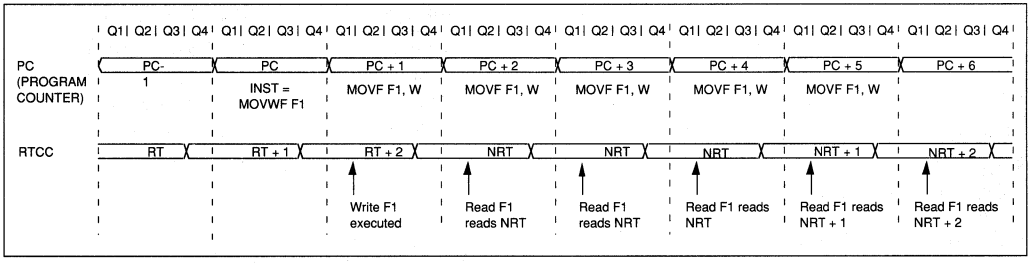


FIGURE 6.4.3 - RTCC TIMING: INT CLOCK/PRESCALE 1:2

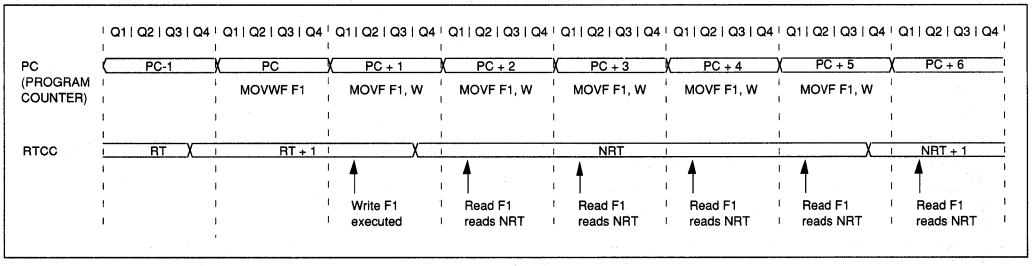
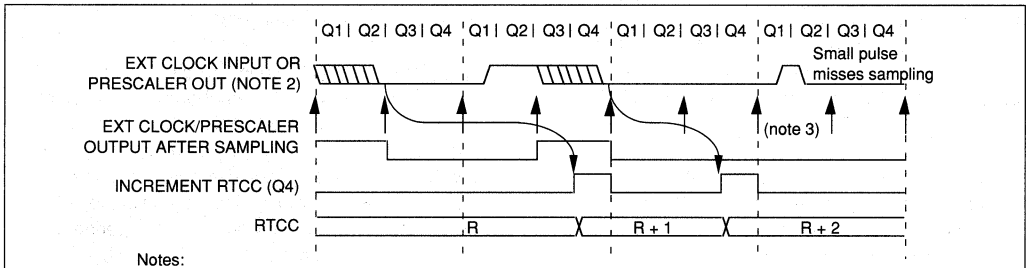


FIGURE 6.4.1.1 - RTCC TIMING WITH EXTERNAL CLOCK



Notes:
1. Delay from clock input change to RTCC increment is 3 tosc to 7 tosc. (Duration of Q = tosc). Therefore, the error in measuring the interval between two edges on RTCC input = ± 4 tosc max.
2. External clock if no prescaler selected, Prescaler output otherwise.
3. The arrows indicate the points in time where sampling occurs.

6.4.2 Prescaler

An 8-bit counter is available as a prescaler for the RTCC, or as a post-scaler for the watchdog timer, respectively (Figure 6.4.2.1). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the RTCC and the watchdog timer. Thus, a prescaler assignment for the RTCC means that there is no prescaler for the watchdog timer, and vice versa.

The PSA and PS0-PS2 bits in the OPTION register determine the prescaler assignment and pre-scale ratio. When assigned to the RTCC, all instructions writing to the RTCC (e.g. CLRF 1, MOVWF 1, BSF 1,x ....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the watchdog timer. The prescaler is not readable or writable.

6.4.2.1 SWITCHING PRESCALER ASSIGNMENT

Changing prescaler from RTCC to WDT

The prescaler assignment is fully under software control, i.e., it can be changed "on the fly" during program execution. To avoid an unintended device RESET, the following instruction sequence must be executed when changing the prescaler assignment from RTCC to WDT:

```
1. MOVLW  B'xx0x0xxx'  ; Select internal clock and select new
2. OPTION              ; prescaler value. If new prescale value
                       ; is = '000' or '001', then select any other
                       ; prescale value temporarily.
3. CLRF 1              ; Clear RTCC and prescaler.
4. MOVLW  B'xxxx1xxx'  ; Select WDT, do not change prescale
                       ; value.
5. OPTION              ;
6. CLRWDT              ; Clears WDT and prescaler.
7. MOVLW B'xxxx1xxx'   ; Select new prescale value.
8. OPTION              ;
```

Step 1 and 2 are only required if an external RTCC source is used. Steps 7 and 8 are necessary only if the desired prescale value is '000' or '001'.

CHANGING PRESCALER FROM WDT TO RTCC

To change prescaler from WDT to RTCC use the following sequence:

```
1. CLRWDT              ; Clear WDT and prescaler
2. MOVLW  B'xxxx0xxx'  ; Select RTCC, new prescale value
                       ; and clock source
3. OPTION              ;
```

6.5 OPTION REGISTER

The OPTION register (address 81h) is a readable and writable register which contains various control bits to configure the prescaler, the external INT interrupt, the RTCC and the weak pull-ups on PortB.

TABLE 6.4 - SUMMARY OF RTCC REGISTERS

Register Name	Function	Address	Power-on Reset Value
RTCC	Timer/counter register	01h	XXXX XXXX
OPTION	Configuration and prescaler assignment bits for RTCC	81h	1111 1111
INTCON	RTCC overflow interrupt flag and mask bits	0Bh	0000 000X

FIGURE 6.4.2.1 - BLOCK DIAGRAM OF THE RTCC/WDT PRESCALER

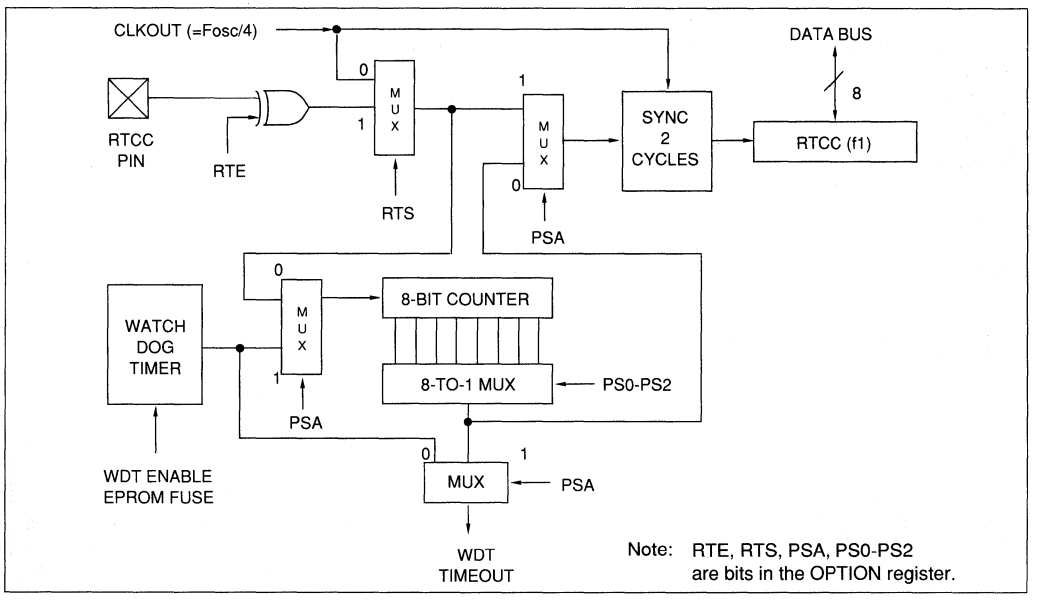
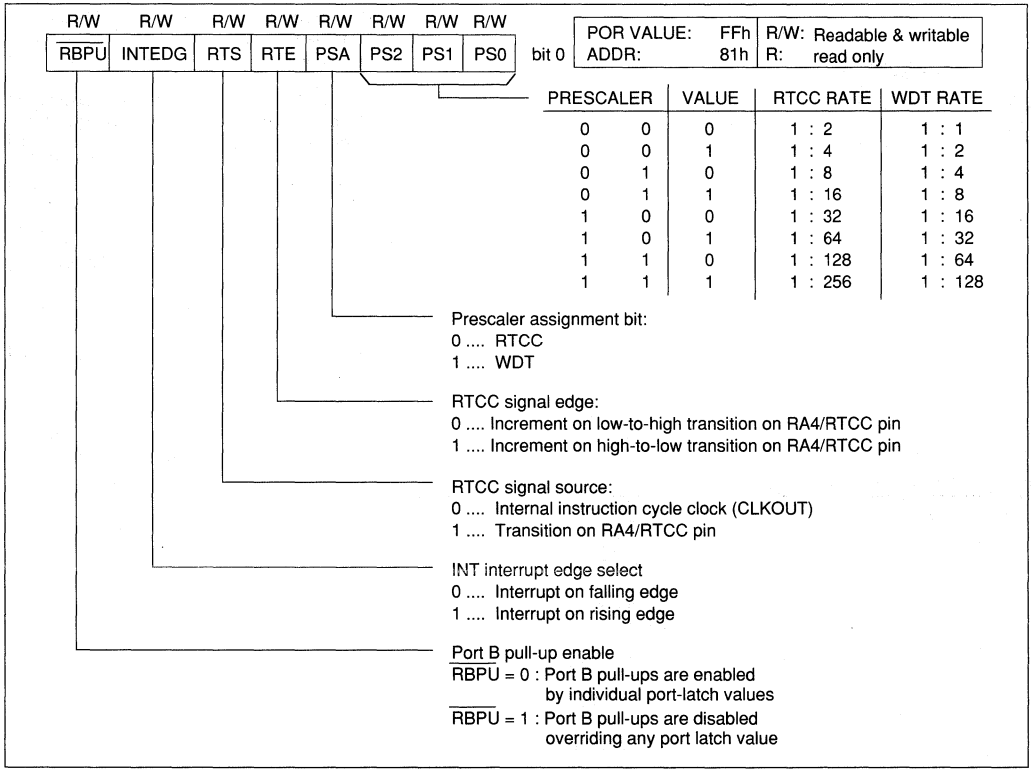


FIGURE 6.5.1 - OPTION REGISTER



6.6 A/D CONVERTER

The A/D converter module has four analog input channels multiplexed into one sample and hold and A/D converter. Reference voltage VREF can come externally from RA3/AIN3/VREF pin or internally from VDD. The converter itself is of successive approximation type and produces an 8-bit result in the ADRES register (address 09h). A conversion is initiated by setting a control bit (GO/DONE, ADCON register). Prior to conversion, the appropriate channel must be selected and enough time allowed for sampling to complete. The conversion time is a function of the oscillator cycle. The minimum conversion time required is 20 µs. At the end of conversion the GO/DONE bit is cleared and the A/D interrupt is activated. The overall accuracy (zero error, full scale error, integral error and quantization error) is less than ±1 LSB for VDD = 5.12V and VREF = VDD. The resolution and accuracy is less when VREF is less than VDD or for VDD less than 5.12V (see specifications for details).

FIGURE 6.6.1 - A/D CONTROL AND STATUS REGISTER (ADCON0, ADDRESS 08h)

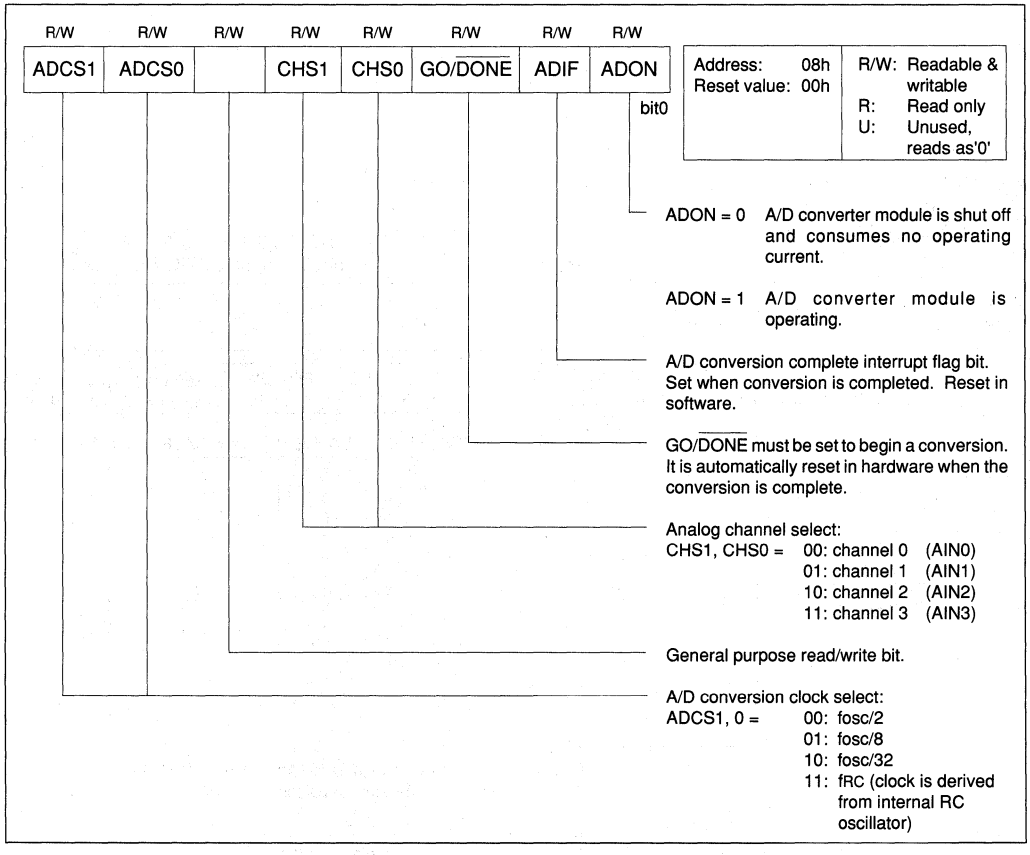


FIGURE 6.6.2 - A/D CONTROL REGISTER (ADCON1, ADDRESS 88h)

U	U	U	U	U	U	R/W	R/W
-	-	-	-	-	-	PCFG1	PCFG0

bit0

Address: 08h
POR value: 00h

R/W: Readable & writable
R: Read only
U: Unimplemented, reads as'0'

PCFG1, 0 configures the RA0-RA3 pins in various modes:

PCFG1, 0	RA0, RA1	RA2	RA3	VREF
0 0	analog inputs	analog input	analog input	VDD
0 1	analog inputs	analog input	ref input	RA3
1 0	analog inputs	digital input	digital input	VDD
1 1	digital inputs	digital input	digital input	-

6.6.1 A/D Clocking Scheme

The A/D converter operates on its own clock, tad, derived from either the OSC1 clock input or from its own on-chip RC oscillator as follows:

Control bit ADCS1, ADCS0	tad (must be > 2 µs)
00	2 tosc
01	8 tosc
10	32 tosc
11	tRC (2 µs-6 µs, 4 µs nominal)

The conversion time for each bit is tad. The total conversion time is 10tad. Selection must be made such that tad is at least 2 µs.

At low frequencies, the RC oscillator can be selected to maintain shorter conversion time. The RC oscillator frequency varies considerably with voltage, temperature and process parameters (2 µs to 6 µs period, nominally 4 µs).

6.6.2 A/D Operation during SLEEP

To reduce operating current all biasing circuits in the A/D block that consume DC current are shut off when ADON bit is a '0'. If a conversion is in progress using RC oscillator, it will be completed. The ADIF interrupt flag bit will be set and the chip will wake up if the ADIE interrupt enable bit is a '1'. Since, during SLEEP, the switching noise is eliminated, the conversion accuracy will be the maximum possible. This provides a means for getting accurate conversions while operating the processor at high clock rates.

If SLEEP is invoked during a conversion that uses OSC1 clock, the conversion will be aborted. The A/D converter will be shut off. The user must re-initialize the conversion, starting with resampling.

6.6.3 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 6.6.3.1. First, the user must configure the TRISA register such that the analog pins are configured as inputs. Second, since the analog pins are connected to digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore must be between VSS and VDD. If input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. To minimize the possibility of damage to the analog inputs due to latch-up a minimum source impedance of 500Ω is recommended. A maximum source impedance of 10KΩ is recommended for the analog sources. At this impedance, the maximum possible error caused by the leakage current is ±5 mV or ±0.25 LSB at VDD = VREF = 5V (10KΩ x 0.5 µA).

The other reason to limit the maximum source impedance is to be able to capture the analog input voltage on to the holding capacitor. The time constant to charge Chold is (see figure 6.6.3.1):

$= C_{hold}(R_{ic} + R_{SS} + R_S)$ where R_S = source impedance

$\approx 51.2\ pF\ (2K\Omega + R_S)$ $R_{ic} + R_{SS} \approx 2K\Omega$

$\approx 51.2\ pF \times 12K\Omega$ (assuming $R_S = 10K\Omega$)

$= 0.6144\ \mu s = T$

from the capacitive charging equation:

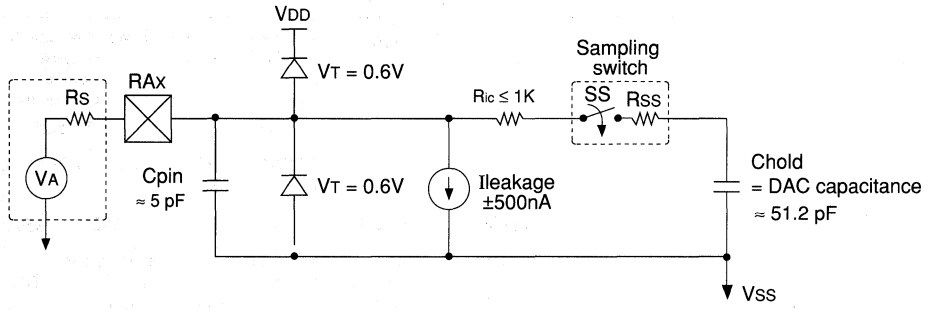
$V_{hold} = V_A(1-e^{-t/T})$

for 1/8 LSB error at VDD = 5V

$$e^{-t/T} = \frac{2.5\ mV}{5000\ mV}$$

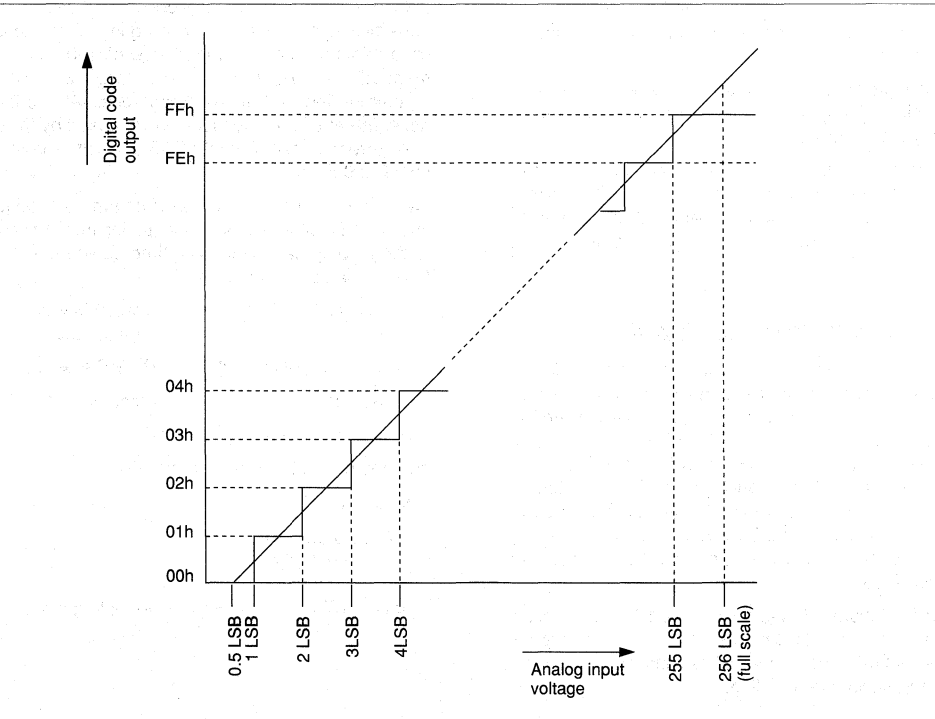
or $t \approx 7.6T = 4.67\mu s$ (required sampling time)

FIGURE 6.6.3.1 - ANALOG INPUT MODEL



Legend		
	Cpin	= input capacitance
	VT	= threshold voltage
	Ileakage	= leakage current at the pin due to various junctions
	Ric	= interconnect resistance
	RSS	= on resistance of the switch
	SS	= sampling switch
	Chold	= sample/hold capacitance (from DAC)
	RS	= source impedance of the analog input
	VA	= analog input voltage

FIGURE 6.6.5.1 - TRANSFER FUNCTION



External RC filter is sometimes added for anti-aliasing. Once again, the value of the R should be such that the total source impedance is kept under 10KΩ. Any external component connected to an analog input pin, such as a capacitor or a zener diode, should have very little leakage current.

6.6.4 Sample and Hold (S/H)

The sample and hold circuit consists of a sampling switch SS (figure 6.6.3.1) and the S/H capacitor whose value is typically 51 pF.

As long as ADON control bit is '1' (bit 0, ADCON 0) and a valid analog input channel is selected, the input will be continuously sampled. There is no command to start or stop sampling. When a conversion is started, sampling is ended and conversion begins on the voltage across the S/H capacitor. The sample and hold, therefore can be more accurately described as "track and hold".

After a conversion is completed, sampling begins after a delay of 2tad. (tad = A/D conversion clock). The user must keep this in mind when allowing for adequate sampling time.

6.6.5 Transfer Function

The ideal transfer function of the A/D converter is as follows: The first transition occurs when input voltage (VA) is 1 LSB (or full scale/256). Figure 6.6.5.1 shows the ideal transfer function.

6.6.6 SUMMARY OF A/D REGISTERS

Register name/bits	Function	Address
ADRES	A/D result register	09h
ADCON0	A/D control and status register	08h
ADCON1	A/D control register	88h
INTCON (bit ADIE)	Interrupt control register	0Bh

7.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Ambient temperature under bias .....-55 to+ 125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on any pin with respect to VSS
(except VDD and MCLR) .....-0.6V to VDD +0.6V
Voltage on VDD with respect to VSS .....0 to +7.5 V
Voltage on MCLR with respect to VSS
(Note 2) .....0 to +14 V
Total power Dissipation (Note 1) .....800 mW
Max. Current out of VSS pin .....150 mA
Max. Current into VDD pin .....100 mA
Max. Current into an input pin.....±500 nA
Max. Output Current sunk by any I/O pin .....25 mA
Max. Output Current sourced by any I/O pin .....20 mA
Max. Output Current sunk by I/O port A .....80 mA
Max. Output Current sunk by I/O port B .....150 mA
Max. Output Current sourced by I/O port A .....50 mA
Max. Output Current sourced by I/O port B .....100 mA

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or compliance to AC and DC parametric specifications at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Total power dissipation should not exceed 800 mW for the package. Power dissipation is calculated as follows:
$Pdis = VDD \times \{IDD - \Sigma Ioh\} + \Sigma\{(VDD-Voh) \times Ioh\} + \Sigma(Vol \times Iol)$

2. Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low' level to the MCLR pin rather than pulling this pin directly to VSS.

7.1 DC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, POWER SUPPLY PINS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ + 125°C for automotive,
-40°C ≤ TA ≤ + 85°C for industrial and
0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD = 4.0V to 6.0V

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Supply Voltage						
	VDD	4.0		6.0	V	XT, RC and LP osc configuration
	VDD	4.5		5.5	V	HS osc configuration
RAM Data Retention Voltage (Note 2)	VDR		1.5 *		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS *		V	See section 5.2 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 5.2 for details on power on reset
Supply Current (Note 3)						
	IDD1		1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V (Note 5)
	IDD2		35	70	µA	FOSC = 32 KHz, VDD = 4.0V, WDT disabled, LP osc config., A/D off (Note 6)
	IDD3		9	20	mA	FOSC = 20 MHz, VDD = 5.5V, HS osc configuration (PIC16C71-20)
Power Down Current (Note 4)						
	IPD1		7	28	µA	VDD = 4.0V, WDT enabled, -40°C to +125°C
	IPD2		1.0	14	µA	VDD = 4.0V, WDT disabled, 0°C to +70°C
	IPD3		1.0	16	µA	VDD = 4.0V, WDT disabled, -40°C to +85°C
	IPD4		1.0	20	µA	VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are guaranteed through characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

Note 6: For current contribution due to A/D module, see section 7.5.

7.2 DC CHARACTERISTICS: PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, POWER SUPPLY PINS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ + 125°C for automotive, -40°C ≤ TA ≤ + 85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD = 3.0V to 6.0V					
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Supply Voltage						
	VDD	3.0		6.0	V	XT, RC and LP osc configuration
	VDD	4.5		5.5	V	HS osc configuration
RAM Data Retention Voltage (Note 2)	VDR		1.5 *		V	Device in SLEEP mode
VDD start voltage to guarantee power on reset	VPOR		VSS *		V	See section 5.2 for details on power on reset
VDD rise rate to guarantee power on reset	SVDD	0.05*			V/ms	See section 5.2 for details on power on reset
Supply Current (Note 3)						
	IDD1		1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V (Note 5)
	IDD2		15	32	µA	FOSC = 32 KHz, VDD = 3.0V, WDT disabled, LP osc config., A/D off (Note 6)
Power Down Current (Note 4)						
	IPD1		5	20	µA	VDD = 3.0V, WDT enabled, -40°C to +125°C
	IPD2		0.6	9	µA	VDD = 3.0V, WDT disabled, 0°C to +70°C
	IPD3		0.6	12	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
	IPD4		0.6	16	µA	VDD = 3.0V, WDT disabled, -40°C to +125°C

* These parameters are guaranteed through characterization and are not tested.

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

Note 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, RT = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

Note 4: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedence state and tied to VDD and VSS.

Note 5: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula Ir = VDD/2Rext (mA) with Rext in kOhm.

Note 6: For current contribution due to A/D module, see section 7.5.

7.3 DC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

DC CHARACTERISTICS, ALL PINS EXCEPT POWER SUPPLY

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial
Operating voltage VDD range as described in DC spec table 7.1

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
Input Low Voltage						
I/O ports	VIL1	VSS		0.2 VDD	V	
MCLR, RTCC, OSC1 (in RC configuration)	VIL2	VSS		0.2 VDD	V	Note 2
OSC1 (in XT, HS and LP configuration)	VIL3	VSS		0.3 VDD	V	
Input High Voltage						
I/O ports	VIH1	2.0		VDD	V	VDD ≤ 5.5V
	VIH1	0.36 VDD				For entire VDD range
MCLR RTCC, OSC1 (in RC configuration)	VIH2	0.8 VDD		VDD	V	Note 2
OSC1 (XT, HS and LP configuration)	VIH3	0.7 VDD		VDD	V	
Input Leakage Current (Notes 3, 4)						
I/O port RB	IIL1			±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
I/O port RA	IIL2			±0.5	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR, RTCC	IIL3			±5	µA	VSS ≤ VPIN ≤ VDD
OSC1	IIL4			±5	µA	VSS ≤ VPIN ≤ VDD , XT, HS and LP osc configuration
Output Low Voltage						
I/O Ports	VOL1			0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
	VOL1			0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT	VOL2			0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)	VOL2			0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
Output High Voltage						
I/O Ports (Note 4)	VOH1	VDD-0.7			V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
	VOH1	VDD-0.7			V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
OSC2/CLKOUT	VOH2	VDD-0.7			V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
(RC osc configuration)	VOH2	VDD-0.7			V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C

Note 1: Data in the column labeled "Typical" is based on characterization results at 25 ° C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2 : In RC oscillator configuration, the OSC1 pin is a Schmitt trigger input. It is not recommended that the PIC16C71 be driven with external clock in RC mode.

Note 3 : The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 4 : Negative current is defined as coming out of the pin.

7.4 AC CHARACTERISTICS: PIC16C71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16C71-20 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE) PIC16LC71-04 (COMMERCIAL, INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS

* Guaranteed by characterization, but not tested.

(Notes on next page)

Standard Operating Conditions (unless otherwise stated)

Operating temperature -40°C ≤ TA ≤ +125°C for automotive,
-40 ≤ TA ≤ +85°C for industrial
and 0°C ≤ TA ≤ +70°C for commercial

Operating voltage VDD range as described in DC spec table 7.1

Characteristic	Sym	Min	Typ (Note 1)	Max	Units	Conditions
External CLOCKIN Frequency (Note 2)	FOSC	DC		4	MHz	XT and RC osc mode
	FOSC	DC		4	MHz	HS osc mode (PIC16C71-04, PIC16LC71-04)
	FOSC	DC		20	MHz	HS osc mode (PIC16C71-20)
	FOSC	DC		200	KHz	LP osc mode
Oscillator Frequency (Note 2)	FOSC	DC		4	MHz	RC osc mode
	FOSC	0.1		4	MHz	XT osc mode
	FOSC	1		4	MHz	HS osc mode (PIC16C71-04 PIC16LC71-04)
	FOSC	1		20	MHz	HS osc mode (PIC16C71-20)
	FOSC	DC		200	KHz	LP osc mode
Instruction Cycle Time (Note 2)	TCY	1.0	4/FOSC	DC	µs	
External Clock in Timing (Note 4)						
Clock in (OSC1) High or Low Time						
XT oscillator type	TCKHLXT	50*			ns	
LP oscillator type	TCKHLLP	2*			µs	
HS oscillator type	TCKHLHS	20*			ns	
Clock in (OSC1) Rise or Fall Time						
XT oscillator type	TCKRFXT	25*			ns	
LP oscillator type	TCKRFLP	50*			ns	
HS oscillator type	TCKRFHS	25*			ns	
RESET Timing						
MCLR Pulse Width (low)	TMCL	100*			ns	
RTCC Input Timing, No Prescaler						
RTCC High Pulse Width	TRTH	0.5 TCY+ 20*			ns	Note 3
RTCC Low Pulse Width	TRTL	0.5 TCY+ 20*			ns	Note 3
RTCC Input Timing, With Prescaler						
RTCC High Pulse Width	TRTH	10*			ns	Note 3
RTCC Low Pulse Width	TRTL	10*			ns	Note 3
RTCC Period	TRTP	$\frac{T_{CY} + 40}{N}$ *			ns	Note 3. Where N = prescale value (2,4, ..., 256)
Watchdog Timer Timeout Period (No Prescaler)	TWDT	7*	18*	33*	ms	VDD = 5V, -40°C to +125°C
Oscillation Start-up Timer Period	TOST		1024 tosc		ms	tosc = OSC1 period
Power up timer period	TPWRT	28*	72*	132*	ms	VDD = 5V, -40°C to +125°C
I/O Timing						
I/O Pin Input Valid Before CLKOUT≠ (RC Mode)	TDS	0.25 TCY+ 30*			ns	
I/O Pin Input Hold After CLKOUT≠ (RC Mode)	TDH	0*			ns	
I/O Pin Output Valid After CLKOUTØ (RC Mode)	TPD			40*	ns	
Capacitive Loading Specs on Output Pins						
OSC2 pin	COSC2			15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
All I/O pins	CIO			50	pF	

NOTES TO TABLE 7.4

Note 1: Data in the column labeled "Typical" is based on characterization results at 25°C. This data is for design guidance only and is not tested for, or guaranteed by Microchip Technology.

Note 2: Instruction cycle period (Tcy) equals four times the input oscillator time base period.
All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

Note 3: For a detailed explanation of RTCC input clock requirements see section 6.4.1.

Note 4: Clock-in high-time is the duration for which clock input is at VIHOSC or higher. Clock-in low-time is the duration for which clock input is at VIHOSC or lower.

7.5 A/D CONVERTER CHARACTERISTICS:

PIC16C71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)
PIC16C71-20 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)
PIC16LC71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS		Standard Conditions (unless otherwise stated) Operating temperature -40°C to +125°C for automotive, TA = -40°C to +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial, VDD = 5.12V				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Resolution	NR	-	-	8 Bits	-	VREF = VDD = 5.12V (Note 2)
Integral error	NINT	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Differential error	NDIF	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Full scale error	NFS	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Offset error	NOFF	-	-	less than ±1 LSB	-	VREF = VDD = 5.12V (Note 2)
Monotonicity	-	-	guaranteed	-	-	
Reference voltage	VREF	3.0 V	-	VDD + 0.3	V	
Analog input voltage	VAIN	VSS - 0.3	-	VREF	V	
Recommended impedance of analog voltage source	ZAIN	-	-	10.0	KΩ	
A/D clock period	tad	- - - 2.0	2tosc 8tosc 32tosc 4.0	- - - 6.0	- - - µs	ADCS1,0 = 00 (for tosc ≥ 1 µs) ADCS1,0 = 01 (for tosc ≥0.25 µs) ADSC1,0 = 10 (for tosc ≥ 62.5 ns) ADSC1,0 = 11 (RC oscillator source is selected)
Conversion time (not including S/H time)	TCNV	-	10tad	-	-	-
Sampling time	TSMP	5	-	-	µs	For 10KΩ source impedance, to guarantee less than 1/8 LSB sampling error. (Note 3)
A/D conversion current (VDD)	Iad	-	180	-	µA	Average current consumption when A/D is on (Note 4)
VREF input current (Note 5)	IREF	-	-	1 10	mA µA	During charging All other times

Note 1: All entries in the "typ" column are at 5V, 25°C unless otherwise stated.

Note 2: The error will be more for lower VREF and/or lower VDD.

Note 3: Sampling time may be less (or more) if source impedance is smaller (or higher). Also note that sampling begins after 2tad delay after a conversion is completed.

Note 4: When A/D is off, it will not consume any current other than minor leakage current. The power down current spec includes any such leakage from the A/D module.

Note 5: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

7.6 A/D CONVERTER CHARACTERISTICS: PIC16LC71-04 (COMMERCIAL/INDUSTRIAL, AUTOMOTIVE)

AC CHARACTERISTICS		Standard Conditions (unless otherwise stated) Operating temperature -40°C to +125°C for automotive, TA = -40°C to +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial, VDD = 3.0V				
Characteristic	**Sym**	**Min**	**Typ (Note 1)**	**Max**	**Units**	**Conditions**
Resolution	NR	-	-	8 Bits	-	VREF = VDD = 3.0V (Note 2)
Integral error	NINT	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Differential error	NDIF	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Full scale error	NFS	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Offset error	NOFF	-	-	less than ±2 LSB	-	VREF = VDD = 3.0V (Note 2)
Monotonicity	-	-	guaranteed	-	-	
Reference voltage	VREF	3.0 V	-	VDD + 0.3	V	
Analog input voltage	VAIN	VSS - 0.3	-	VREF	V	
Recommended impedance of analog voltage source	ZAIN	-	-	10.0	KΩ	
A/D clock period	tad	- - - 3.0	2tosc 8tosc 32tosc 6.0	- - - 9.0	- - - µs	ADCS1,0 = 00 (for tosc ≥ 1 µs) ADCS1,0 = 01 (for tosc ≥0.25 µs) ADSC1,0 = 10 (for tosc ≥ 62.5 ns) ADSC1,0 = 11 (RC oscillator source is selected)
Conversion time (not including S/H time)	TCNV	-	10tad	-	-	-
Sampling time	TSMP	5	-	-	µs	For 10KΩ source impedance, to guarantee less than 1/8 LSB sampling error. (Note 3)
A/D conversion current (VDD)	Iad	-	90	-	µA	Average current consumption when A/D is on (Note 4)
VREF input current (Note 5)	IREF	-	-	1 10	mA µA	During charging All other times

Note 1: All entries in the "typ" column are at 5V, 25°C unless otherwise stated.

Note 2: These specifications apply if VREF = 3.0V and if VDD ≥ 3.0V.

Note 3: Sampling time may be less (or more) if source impedance is smaller (or higher). Also note that sampling begins after 2tad delay after a conversion is completed.

Note 4: When A/D is off, it will not consume any current other than minor leakage current. The power down current spec includes any such leakage from the A/D module.

Note 5: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

7.6.1 Electrical Structure of Pins

FIGURE 7.6.1 - ELECTRICAL STRUCTURE OF I/O PINS (RA, RB)

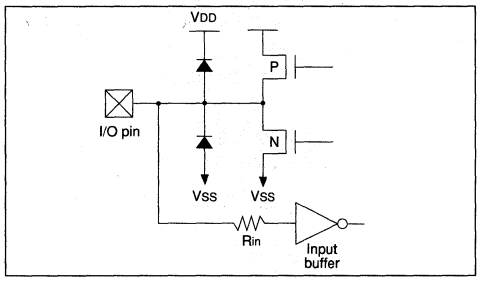
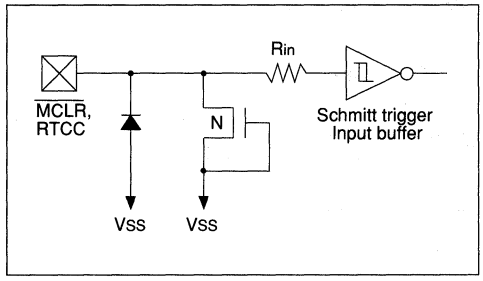


FIGURE 7.6.2 - ELECTRICAL STRUCTURE OF MCLR AND RTCC PINS



Notes to figures 7.6.1 and 7.6.2: The diodes and the grounded gate (or output driver) NMOS device are carefully designed to protect against ESD (Electrostatic discharge) and EOS (Electrical overstress). Rin is a small resistance to further protect the input buffer from ESD.

8.0 TIMING DIAGRAMS

FIGURE 8.0.1 - RTCC TIMING

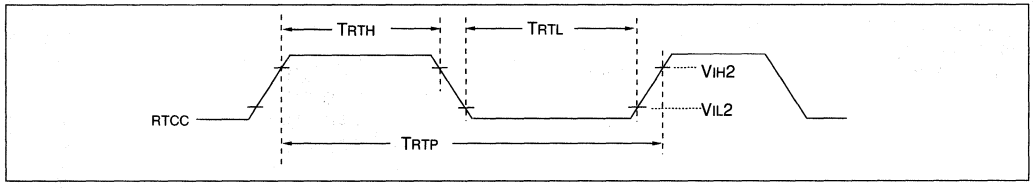


FIGURE 8.0.2 - OSCILLATOR START-UP TIMING (PIC16C71RC)

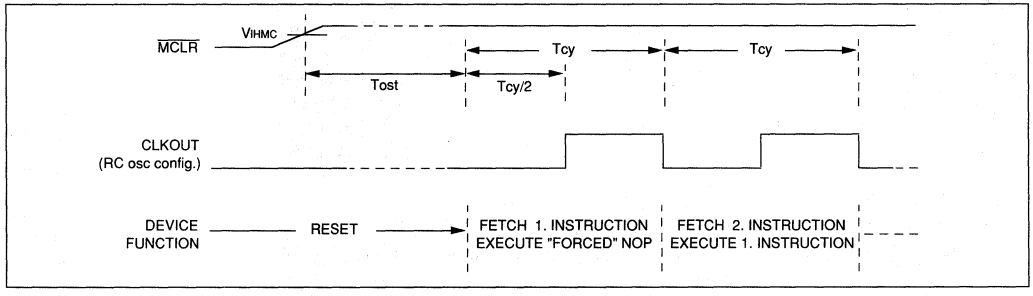
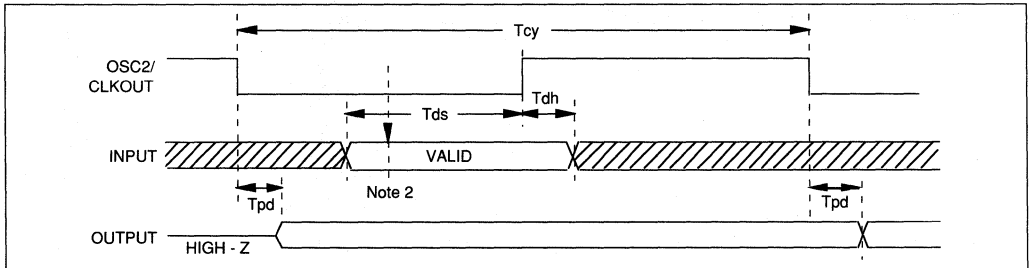


FIGURE 8.0.3 - INPUT/OUTPUT TIMING FOR I/O PORTS



Notes: 1. The CLKOUT output is available only in RC oscillator mode.
2. Internally, this is the point where input data is sampled. Since no timing edge is externally available, setup and hold times are specified with respect to the rising edge of CLKOUT.

9.0 DC & AC CHARACTERISTICS GRAPHS/TABLES:

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. **In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.**

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. 'Typical' represents the mean of the distribution while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

FIGURE 9.0.1 - TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

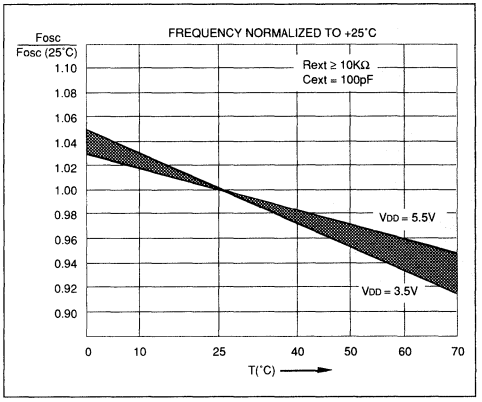


FIGURE 9.0.2 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

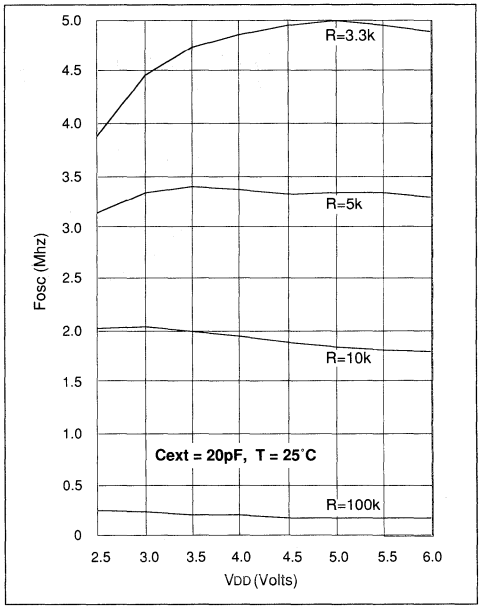
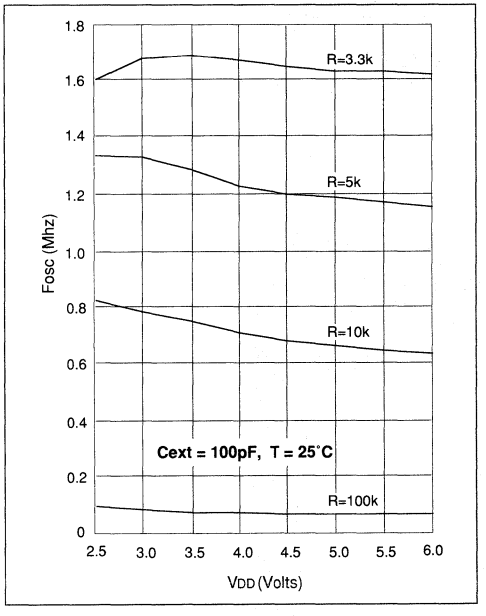


FIGURE 9.0.3 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD



Note: The gray shaded regions are outside normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.4 - TYPICAL RC OSCILLATOR FREQUENCY vs VDD

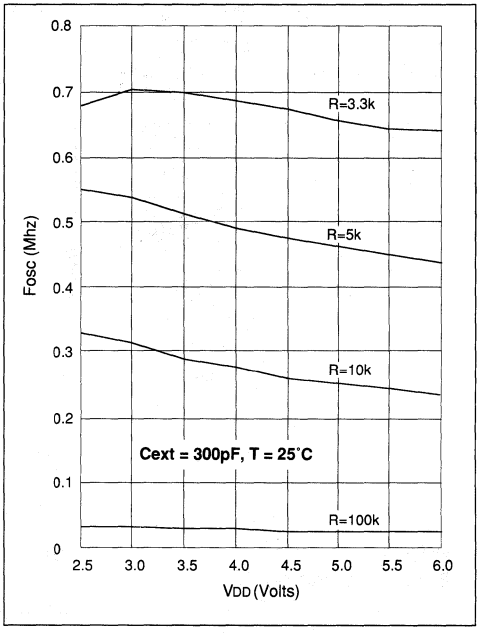


TABLE 9.0.1 - RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5V, 25°C	
20pf	3.3k	4.71 MHz	± 28%
	5k	3.31 MHz	± 25%
	10k	1.91 MHz	± 24%
	100k	207.76 KHz	± 39%
100pf	3.3k	1.65 MHz	± 18%
	5k	1.23 MHz	± 21%
	10k	711.54 KHz	± 18%
	100k	75.62 KHz	± 28%
300pf	3.3k	672.78 KHz	± 14%
	5k	489.49 KHz	± 13%
	10k	275.73 KHz	± 13%
	100k	28.12 KHz	± 23%

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for full VDD range.

FIGURE 9.0.5 - TYPICAL Ipd vs VDD WATCHDOG DISABLED 25°C

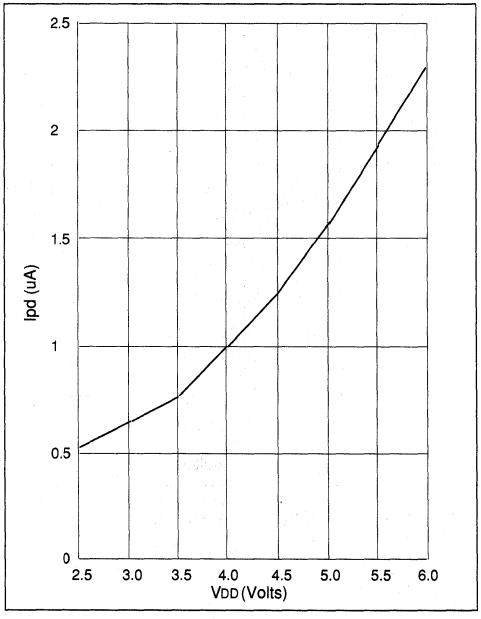
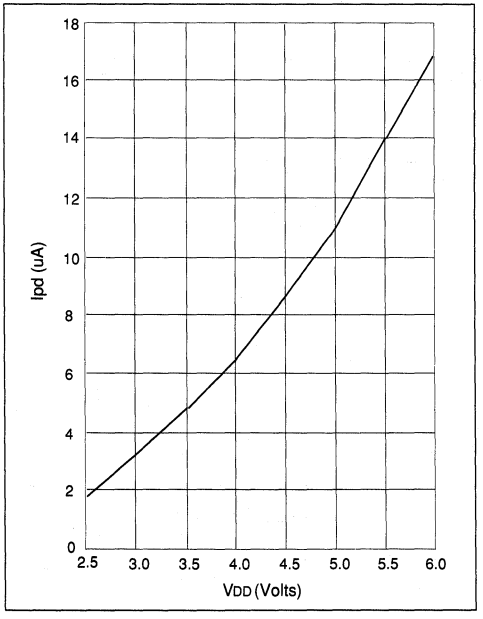


FIGURE 9.0.6 - TYPICAL Ipd vs VDD WATCHDOG ENABLED 25°C



Note 1: The gray shaded regions are outside normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.7 - MAXIMUM Ipd vs VDD WATCHDOG DISABLED

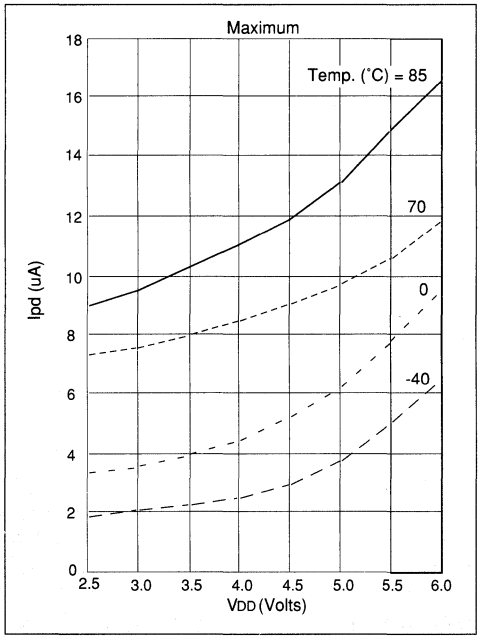
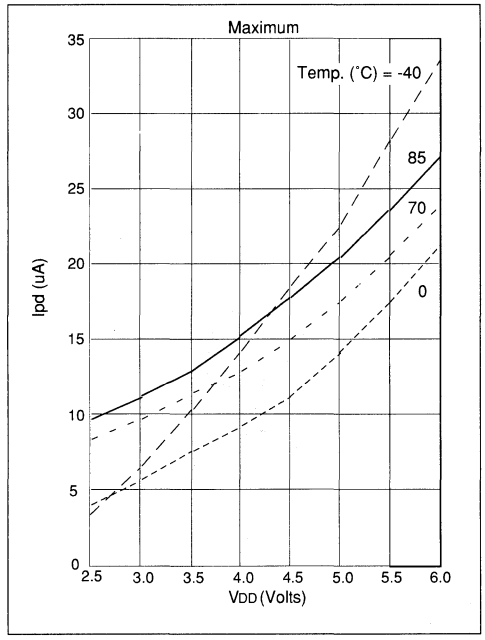


FIGURE 9.0.8 - MAXIMUM Ipd vs VDD WATCHDOG ENABLED*



* IPD, with watchdog timer enabled, has two components: The leakage current which increases with higher temperature and the operating current of the watchdog timer logic which increases with lower temperature. At -40°C, the latter dominates explaining the apparently anomalous behavior.

Note 1: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.9 - VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs VDD

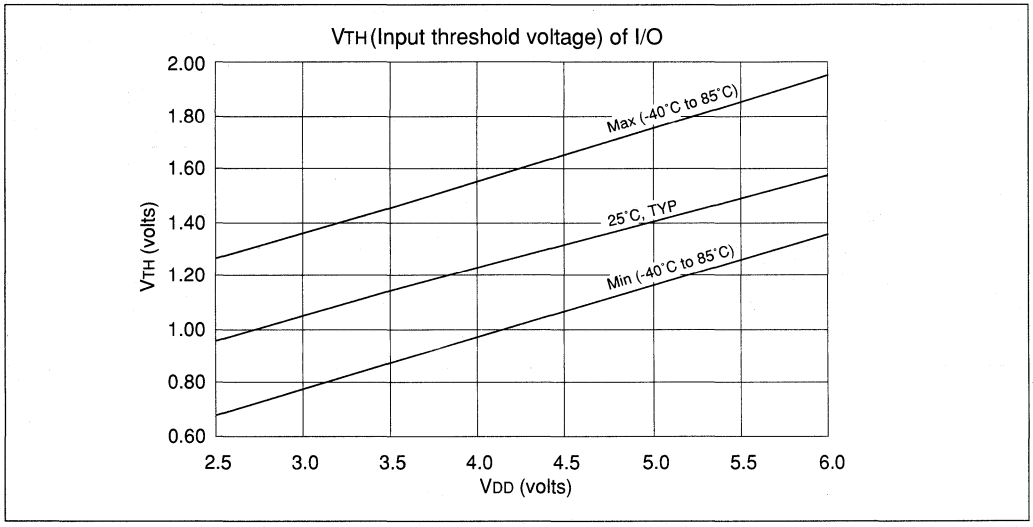
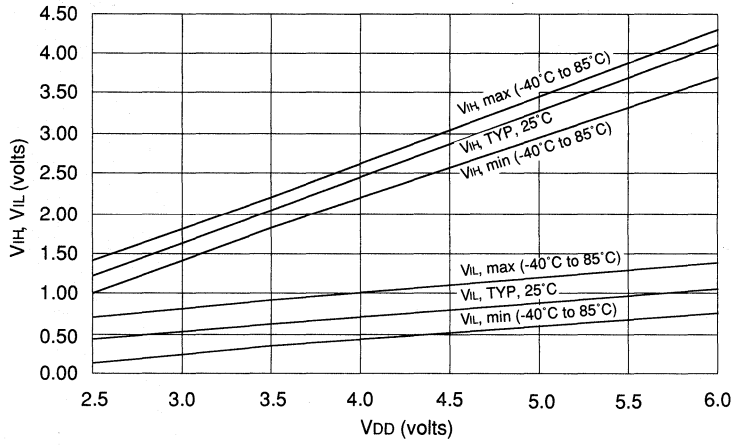
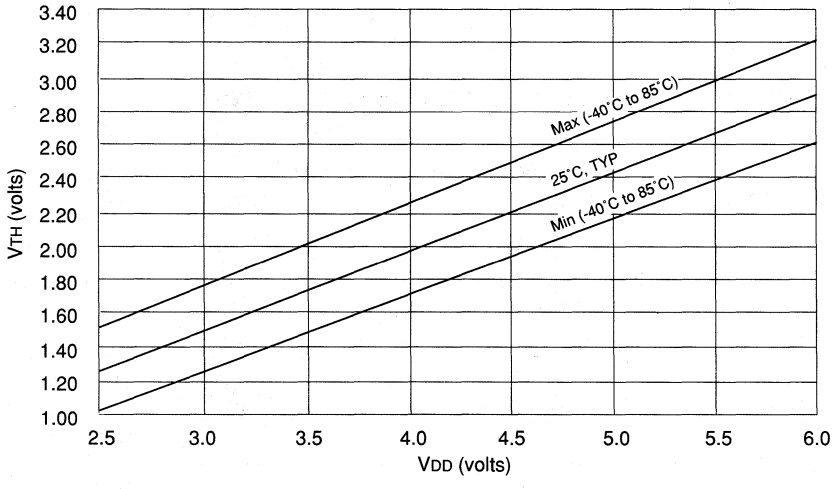


FIGURE 9.0.10 - VIH, VIL OF $\overline{\text{MCLR}}$, RTCC AND OSC1 (IN RC MODE) vs VDD



Note: These input pins have Schmitt trigger input buffer.

FIGURE 9.0.11 - VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs VDD



Note: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.12 - TYPICAL IDD vs FREQ (EXT CLOCK, 25°C)

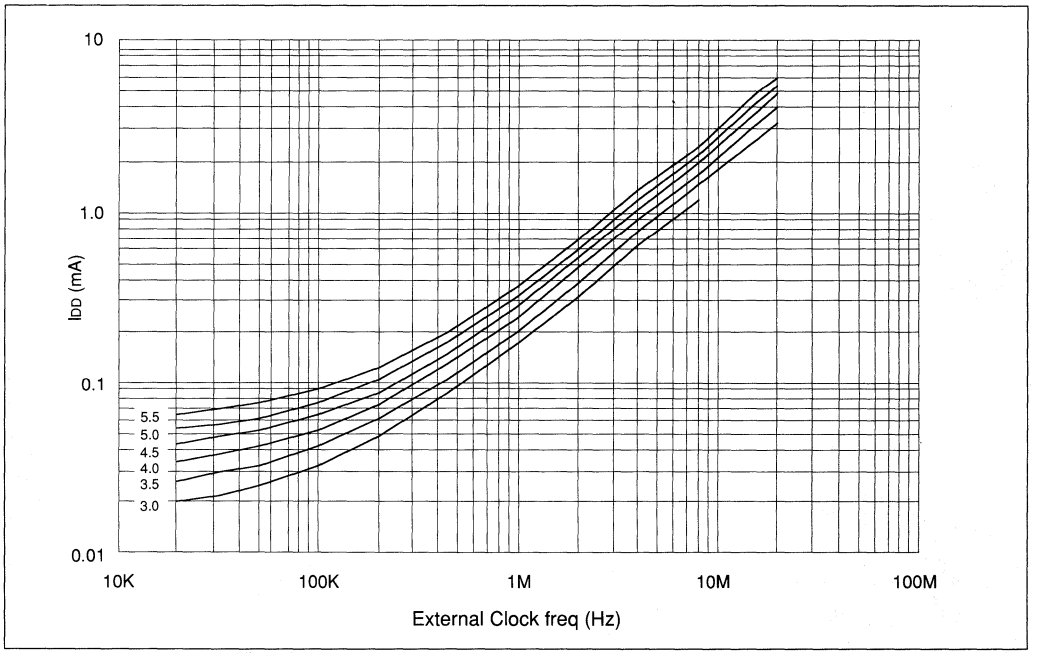


FIGURE 9.0.13 - MAXIMUM IDD vs FREQ (EXT CLOCK, -40° to +85°C)

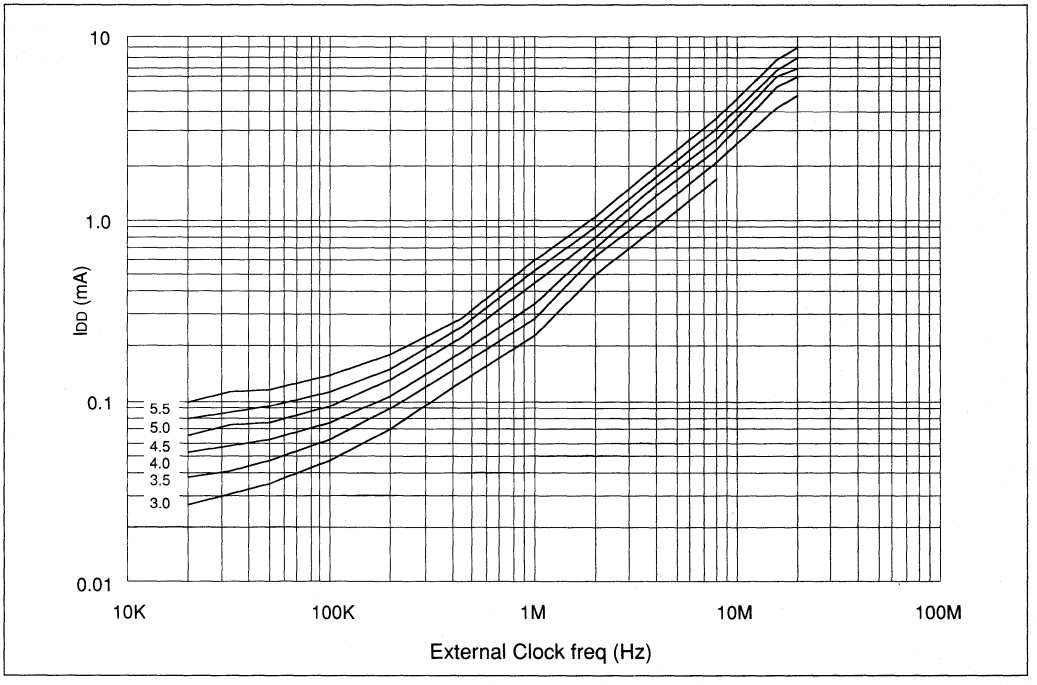


FIGURE 9.0.14 - WDT Timer Time-out Period vs VDD

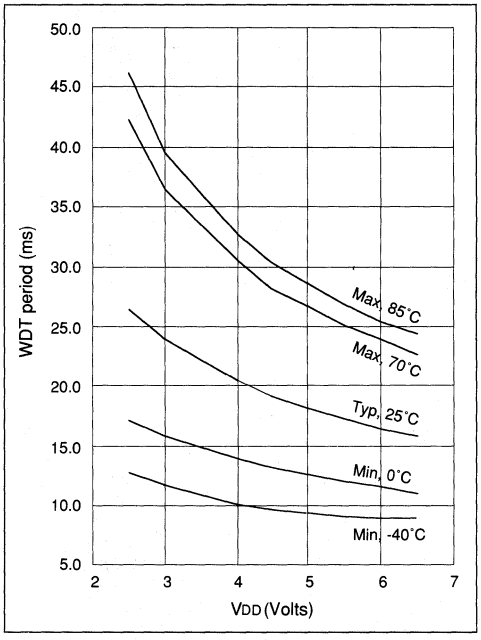


FIGURE 9.0.15 - Transconductance (gm) of HS Oscillator vs VDD

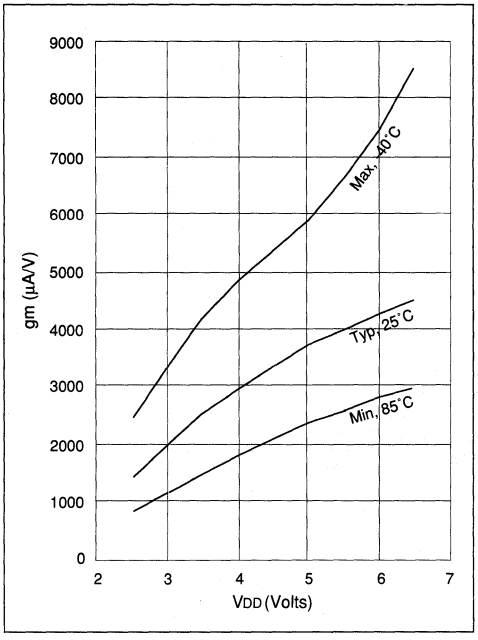


FIGURE 9.0.16 - Transconductance (gm) of LP Oscillator vs VDD

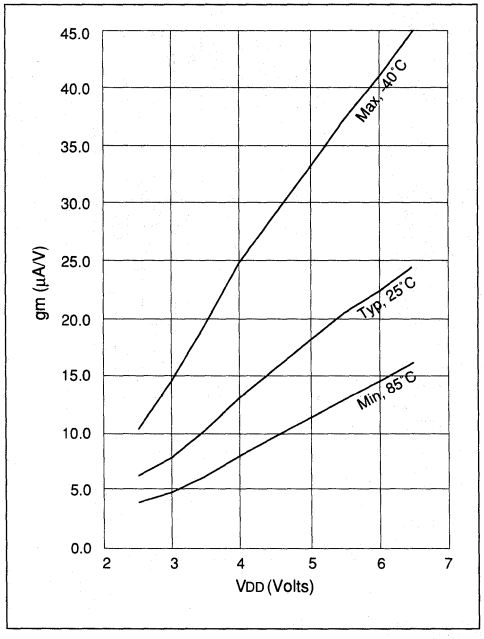
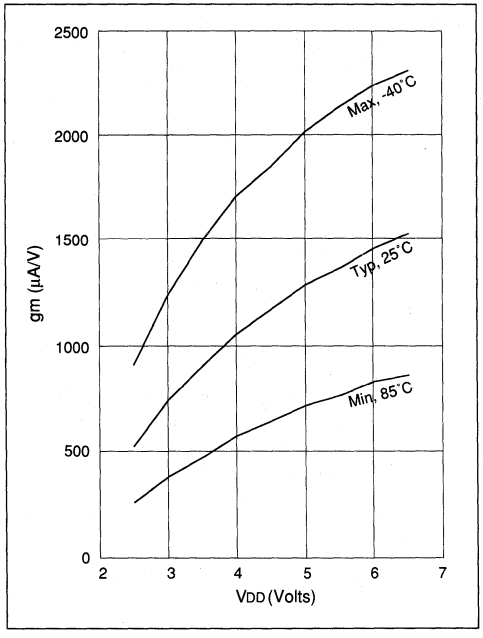


FIGURE 9.0.17 - Transconductance (gm) of XT Oscillator vs VDD



Note: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

FIGURE 9.0.18 - IOH vs VOH, VDD = 3V

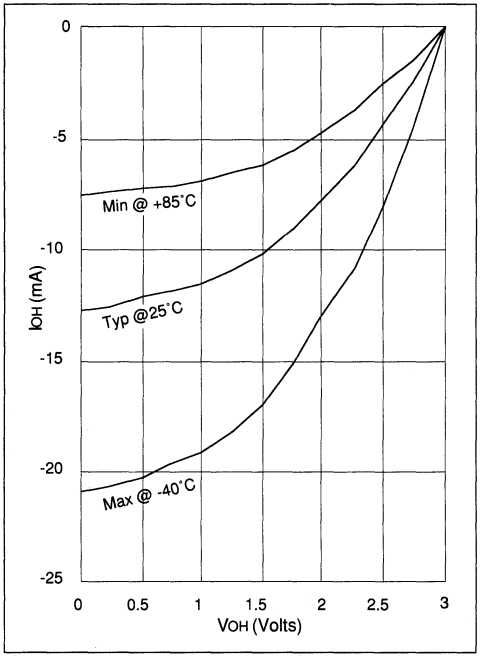


FIGURE 9.0.19 - IOH vs VOH, VDD = 5V

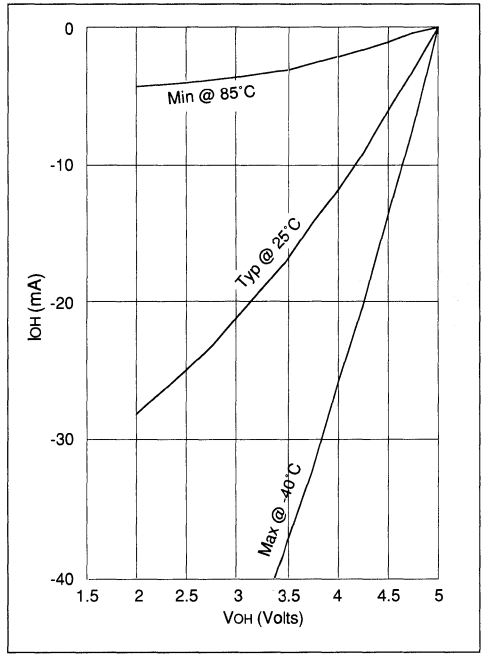


FIGURE 9.0.20 - IOL vs VOL, VDD = 3V

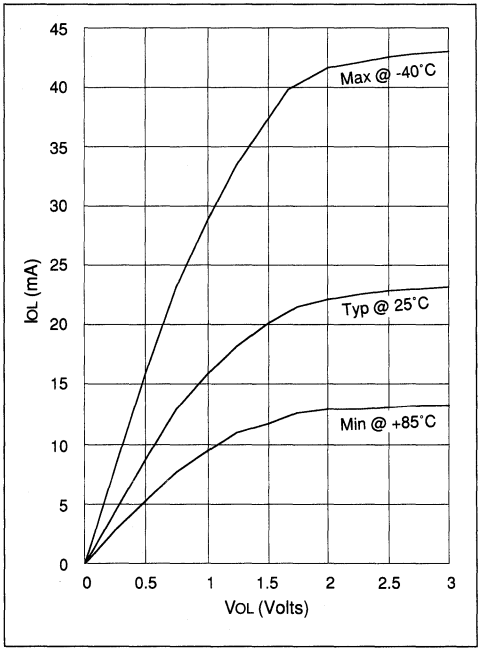
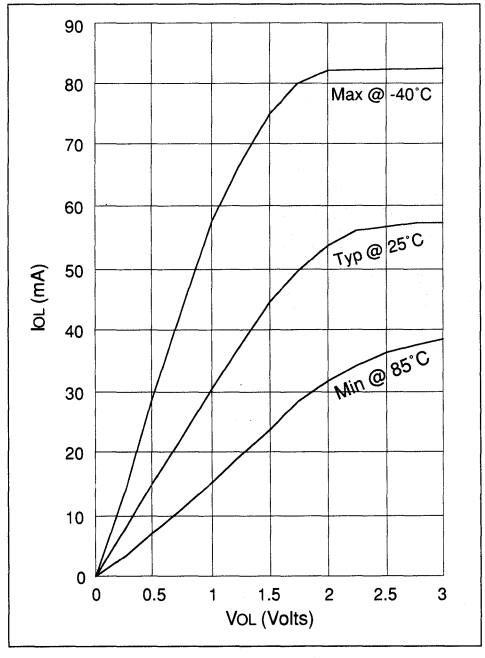


FIGURE 9.0.21 - IOL vs VOL, VDD = 5V



Note: The gray shaded regions are outside of the normal PIC operating range. Do not operate in these regions.

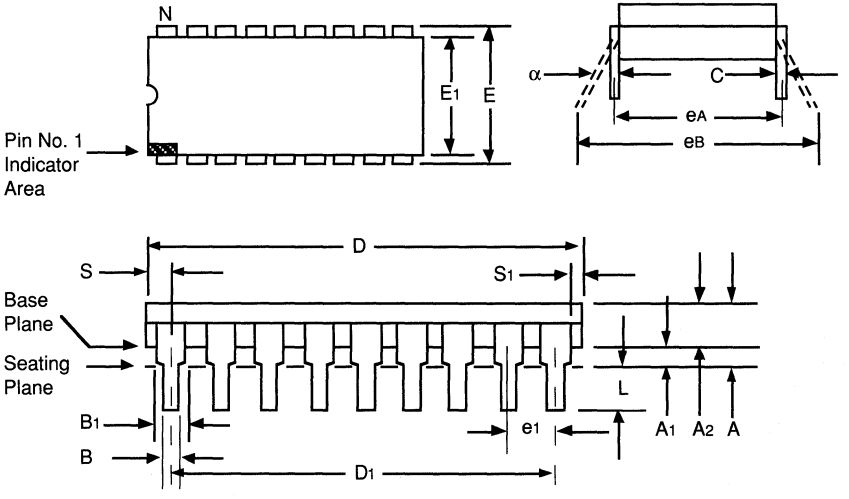
TABLE 9.0.2 - INPUT CAPACITANCE *

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
RTCC	3.2	2.8

* All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

10.0 PACKAGING DIAGRAMS AND DIMENSIONS

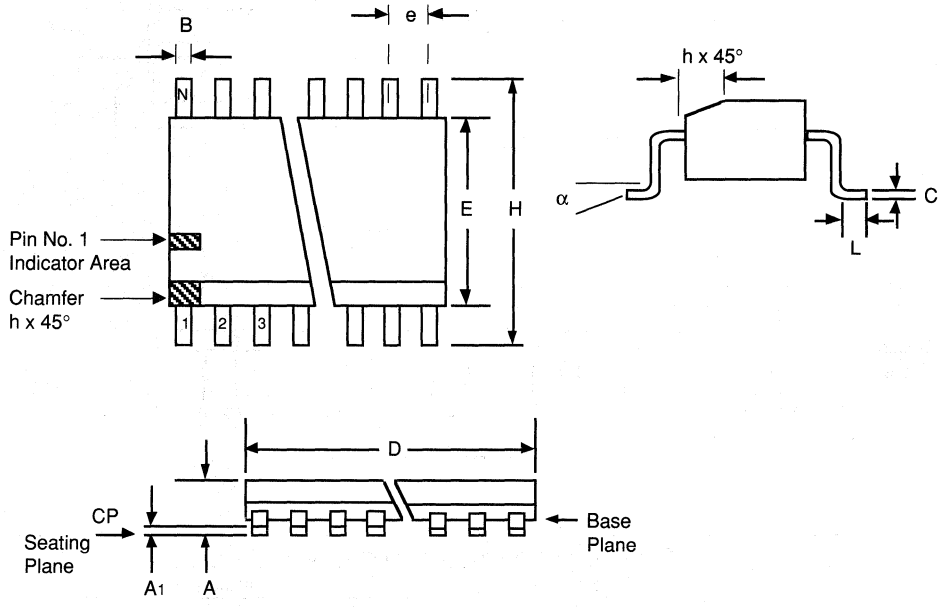
10.1 18-LEAD PLASTIC DUAL IN-LINE (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.479	23.495		0.885	0.925	
D1	20.320	20.32	**Reference**	0.800	0.800	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

PACKAGING DIAGRAMS AND DIMENSIONS (CONT.)

10.2 18-LEAD PLASTIC SURFACE MOUNT (SOIC - WIDE, 300 mil BODY)

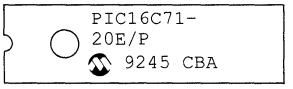


Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A_1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	11.3538	11.7348		0.447	0.462	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	18	18		18	18	
CP	–	0.1016		–	0.004	

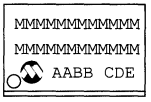
10.3 PACKAGE MARKING INFORMATION

18L PDIP

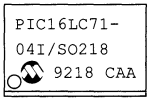
Example



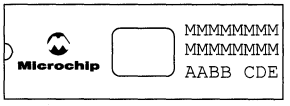
18L SOIC



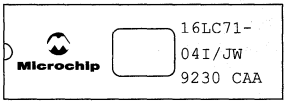
Example



18L Cerdip



Example



Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured. C = Chandler, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled.

Note: In the event the full Microchip part number can not be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev #, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

11.0 PROGRAMMING THE PIC16C71

The PIC16C71 is programmed using one of two methods, serial or parallel. The serial mode will allow the PIC16C71 to be programmed while in the users system using only five pins: VDD, VSS, MCLR/VPP, RB6 and RB7. This allows for increased design flexability. The parallel mode will provide faster programming as the data is loaded into the PIC16C71 with a greater throughput. Either mode may be selected at the start of the programming process. The parallel mode is intended for programmers. Only the "serial mode" is described here. You can get complete programming information in the PIC16C71 programming specification (DS30153).

11.1 Hardware Requirements

The PIC16C71 requires two programmable power supplies, one for VDD (4.5V to 5.5V) and one for VPP (VDD +4.5 to 14V). Both supplies should have a minimum resolution of 0.25V.

11.2 Programming Mode Entry

The programming mode for the PIC16C71 allows programming of user program memory, special locations used for ID, and the configuration fuses for the PIC16C71. This enters programming mode by raising MCLR/VPP from VIL to VIHH (high voltage) while keeping RB6 and RB7 pins at VIL.

11.3 User Program Memory Map

The user memory space extends from 0000h to 1FFFh (8K), of which 1K (0000h - 03FFh) is physically implemented. In actual implementation the on-chip user program memory is accessed by the lower 10 bits of the PC, with the upper 3 bits of the PC ignored. Therefore if the PC is greater than 3FFh, it will wrap around and address a location within the physically implemented memory.

In programming mode the program memory space extends from 0000h to 3FFFh, with the first half (0000h-1FFFh) being user program memory and the second half (2000h-3FFFh) being configuration memory. The PC will increment from 0000h to 1FFFh to 2000h to 3FFFh and wrap around to 2000h (not to 0000h). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program mode.

In the configuration memory space, 2000h-207Fh are utilized. When in configuration memory, as in the user memory, the 2000h-23FFh segment is repeatedly accessed as PC exceeds 23FFh.

11.4 Serial Program/Verify Operation

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled 6 times. Each command bit is latched on the falling edge of the clock with the least significant bit (lsb) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time of 100ns with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1us between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. Data is also input and output lsb first. Therefore, during a read operation the lsb will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the lsb will be latched on the falling edge of the second cycle. A minimum 1us delay is also specified between consecutive commands.

The commands that are available are:

11.4.1 Load Configuration

After receiving this command, the program counter (PC) will be set to 2000 hex. By then applying 16 cycles to the clock pin, the chip will load 14 bits in as the "data word", as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and configuration mode operation is shown in figure 11.3.1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking MCLR low (Vil).

11.4.2 Load Data

After receiving this command, the chip will load in 14 bits as a "data word" when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in figure 11.4.2.2.

11.4.3 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedence) after the 16th rising edge. A timing diagram of this command is shown in figure 11.4.3.1.

11.4.4 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in figure 11.4.4.1.

FIGURE 11.3.1 - PROGRAM MEMORY MAPPING

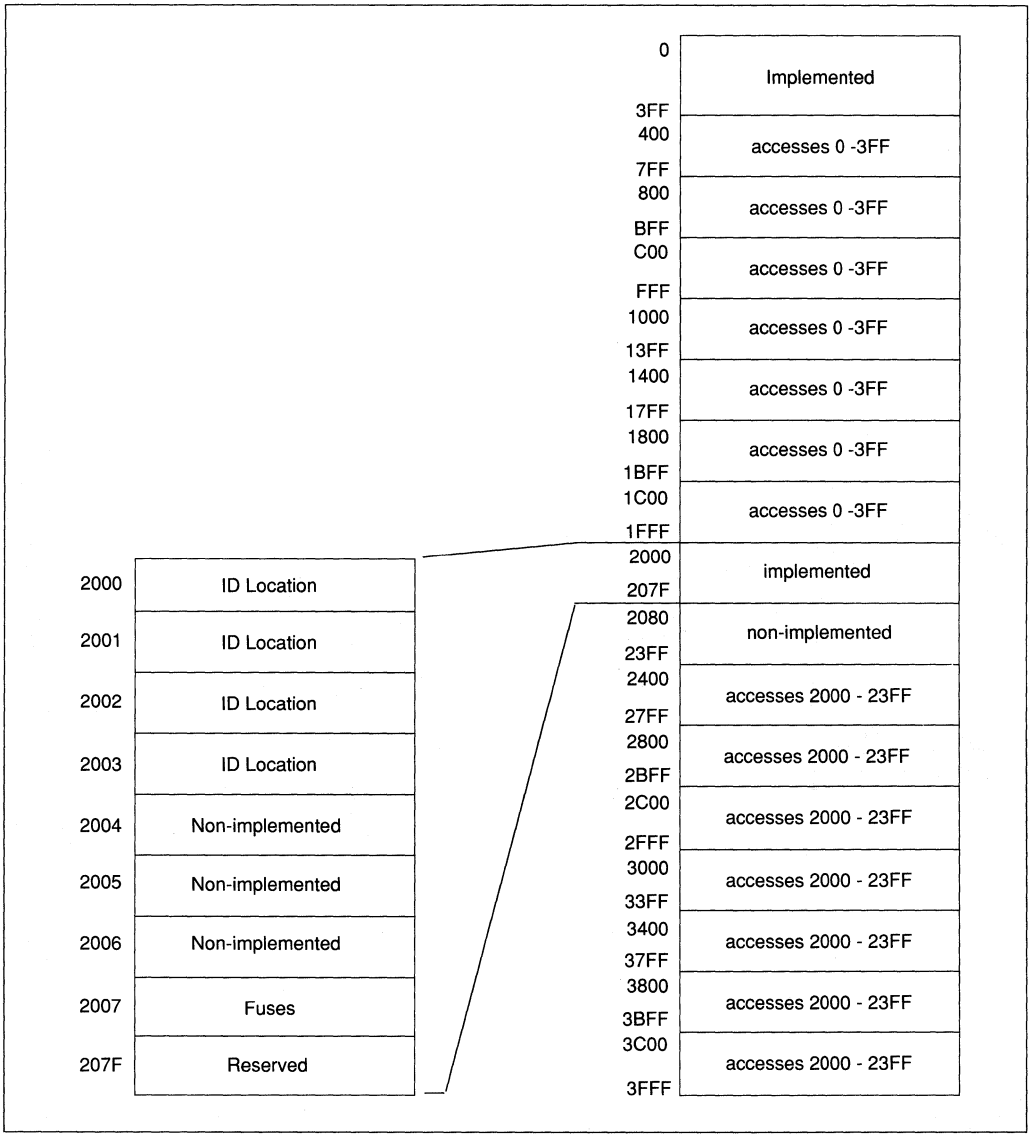


TABLE 11.4.1 - COMMAND MAPPING (SERIAL OPERATION)

Command	Mapping (msb ... lsb)	Data
Load Configuration	X X 0 0 0 X	0, data(14), 0
Load Data	X X 0 0 1 X	0, data(14), 0
Read Data	X X 0 1 0 X	0, data(14), 0
Increment Address	X X 0 1 1 X	
Begin programming	X X 1 0 0 X	
End Programming	X X 1 1 1 X	

FIGURE 11.4.2.2 - LOAD DATA COMMAND (SERIAL PROGRAM/VERIFY)

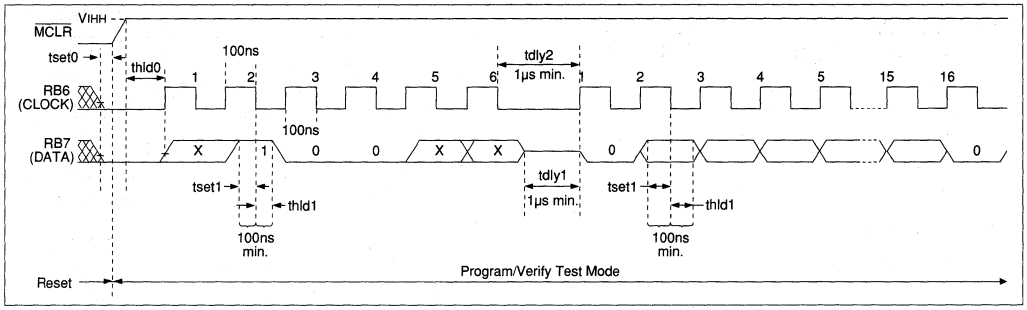


FIGURE 11.4.3.1 - READ DATA COMMAND (SERIAL PROGRAM/VERIFY)

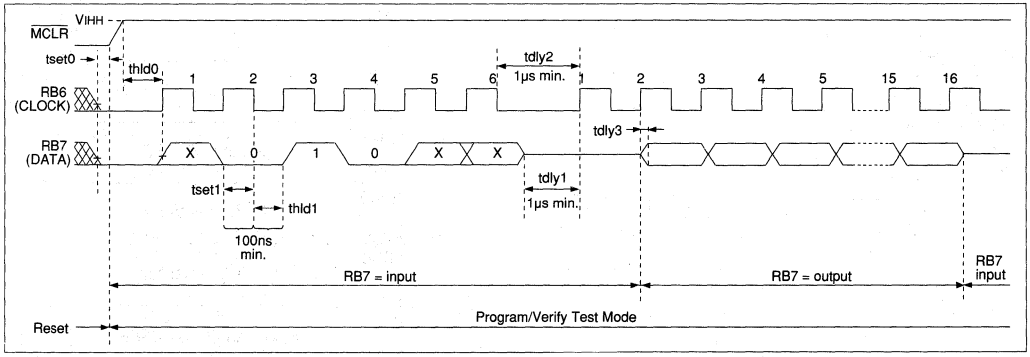
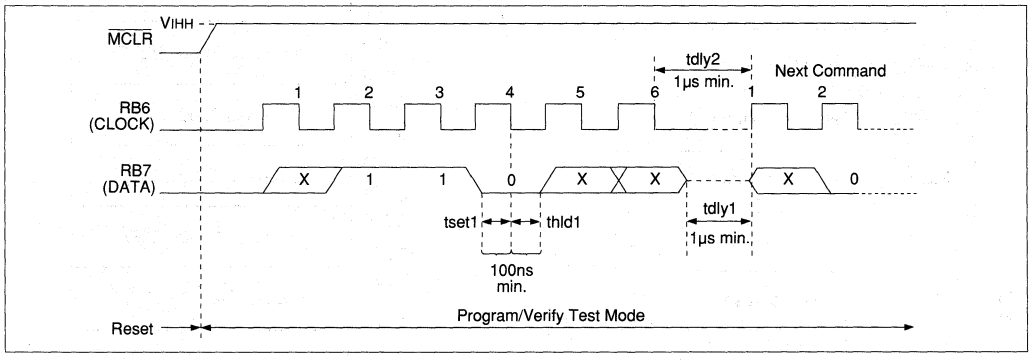


FIGURE 11.4.4.1 - INCREMENT ADDRESS COMMAND (SERIAL PROGRAM/VERIFY)



11.4.5 Begin Programming

A load command (load configuration or load data) must be given before the begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100 µs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

11.4.6 End Programming

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

All commands are transmitted lsb first. Data words are also transmitted lsb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1us is required between a command and a data word (or another command).

12.0 DEVELOPMENT SUPPORT

12.1 PICMASTER™: High Performance Universal In-Circuit Emulator System

The PICMASTER Universal In-Circuit Emulator System is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16CXX and PIC17CXX families. This system currently supports the PIC16CR54, PIC16C54, PIC16C55, PIC16C56 and PIC16C57, and PIC17C42 processors. PIC16C71 support is planned.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.0 environment, allowing the operator access to a wide range of supporting software and accessories.

Provided with the PICMASTER System is a high performance real-time In-Circuit Emulator, a programmer unit and a macro assembler program.

Coupled with the user's choice of text editor, the system is ready for development of products containing any of Microchip's microcontroller products.

A "Quick Start" PIC Product Sample Pak containing user programmable parts is included for additional convenience.

Microchip provides additional customer support to developers through an Electronic Bulletin Board System (EBBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS system.

12.1.1 Host System Requirements:

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to you the end user.

To properly take advantages of these features, PICMASTER requires installation on a system having the following minimum configuration:

- PC AT compatible machine: 80286, 386SX, 386DX, or 80486 with ISA or EISA Bus.
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended).
- MSDOS / PCDOS version 3.1 or greater.
- Microsoft Windows® version 3.0 or greater operating in either standard or 386 enhanced mode).
- 1 Mbyte RAM (2 Mbytes recommended).
- One 5.25" floppy disk drive.
- Approximately 10 Mbytes of hard disk (1 Mbyte required for PICMASTER, remainder for Windows 3.X system).
- One 8-bit PC AT (ISA) I/O expansion slot (half size)
- Microsoft® mouse or compatible (highly recommended).

12.1.2 Emulator System Components:

The PICMASTER Emulator Universal System consists primarily of 4 major components:

- **Host-Interface Card:** The PC Host Interface Card connects the emulator system to an IBM PC compatible system. This high-speed parallel interface requires a single half-size standard AT / ISA slot in the host system. A 37-conductor cable connects the interface card to the external Emulator Control Pod.
- **Emulator Control Pod:** The Emulator Control Pod contains all emulation and control logic common to all microcontroller devices. Emulation memory, trace memory, event and cycle timers, and trace/breakpoint logic are contained here. The Pod controls and interfaces to an interchangeable target-specific emulator probe via a 14" precision ribbon cable.
- **Target-specific Emulator Probe:** A probe specific to microcontroller family to be emulated is installed on the ribbon cable coming from the control pod. This probe configures the universal system for emulation of a specific microcontroller.
- **PC Host Emulation Control Software:** Host software necessary to control and provide a working user interface is the last major component of the system. The emulation software runs in the Windows 3.X environment, and provides the user with full display, alter, and control of the system under emulation. The Control Software is also universal to all microcontroller families.

The Windows 3.X System is a multitasking operating system which will allows the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.X, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

Under Windows 3.X, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16Cxx processor and a PIC17Cxx processor).

FIGURE 12.1.1 - PICMASTER

FIGURE 12.1.2 - PICMASTER SYSTEM CONFIGURATION

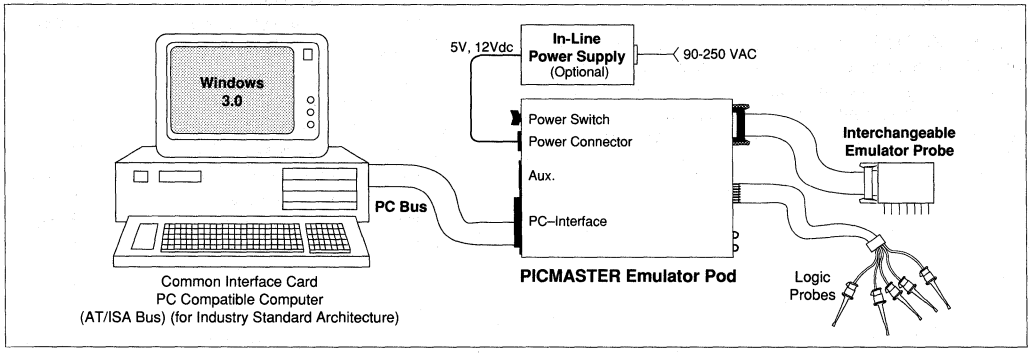
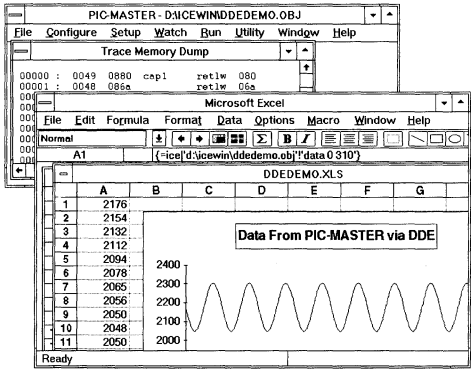


FIGURE 12.1.3 - PICMASTER TYPICAL SCREEN



12.2 PICALC Cross-Assembler

The PIC Cross Assembler PICALC is a PC hosted software development tool supporting the PIC16C5X series microcontrollers. PICALC offers a full featured Macro and Conditional assembly capability. It can also generate various object code formats including several Hex formats to support Microchip's proprietary development tools as well as third party tools. Also supports Hex (default), Decimal and Octal Source and listing formats. An assembler users manual is available for detailed support.

12.3 PRO MASTER™

The PRO MASTER programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MASTER has programmable VDD and VPP supplies which allows it to verify the PIC at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MASTER can read, verify or program a part. It can also set fuse configuration and code-protect in this mode. It's EEPROM memory holds data and parametric information even when powered down. It is ideal for low to moderate volume production.

In PC-hosted mode, the PRO MASTER connects to the PC via one of the COM (RS232) ports. A PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different serial number, sequential or random.

The PRO MASTER has a modular "programming socket module". Different socket modules are required for different processor types and/or package types. It is planned that the PRO MASTER will support all current and future PIC16CXX and PIC17CXX processors. Currently socket modules are available for the PIC16C54, PIC16C55, PIC16C56, PIC16C57, PIC17C42 and the PIC16C71.

APPENDIX A

The following are the list of modifications over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bit. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and register file (128 bytes now versus 32 bytes before).
2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from status register.
3. Data memory paging is redefined slightly. Status register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.

   Two instructions TRIS and OPTION are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressible.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers oscillator start-up timer (OST) and power-up timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PortB has weak pull-ups and interrupt on change feature.
13. RTCC pin is also a port pin (RA4) now.
14. Location 07h (PortC) is unimplemented and not a general purpose register.
15. FSR is made a full eight bit register.
16. "In system programming" is made possible. The user can program the PIC16C71 using only five pins: V_{DD}, V_{SS}, MCLR/V_{PP}, RB6 (clock) and RB7 (data in/out).

APPENDIX B

To convert code written for PIC16C5X to PIC16C71, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.
6. Note that location 07h is an unimplemented data memory location.

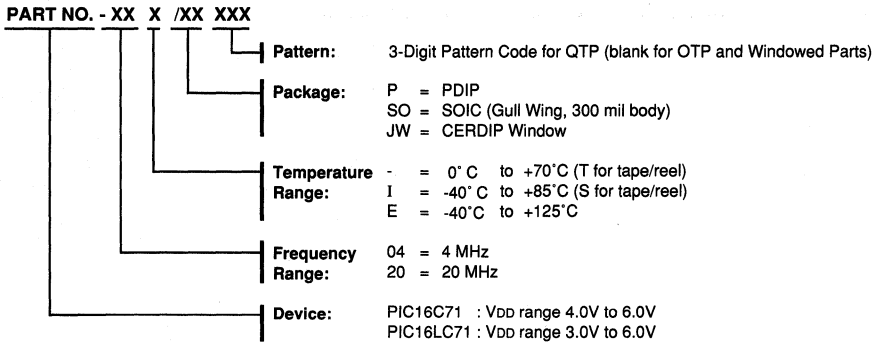
Notes:

Notes:

Notes:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices. For the *currently available code-combinations*, refer to previous page.



Examples:

a) PIC16C71 - 04/P301 = Commercial temp., PDIP package, 4 MHz, normal VDD limits, QTP pattern # 301
b) PIC16LC71I - 04/SO = Industrial temp., SOIC package, 4 MHz, extended VDD limits
c) PIC16C71E - 20/P = Automotive temp., PDIP package, 20 MHz, normal VDD limits

Microchip

PIC®17C42

High Performance 8-Bit CMOS EPROM Microcontroller

1

FEATURES

Powerful CPU

- Fully static design
- 8 bit wide data path
- 16 bit wide instructions
- All instructions are single word
- Most instructions are single cycle, a few are two cycle
- 250ns cycle time (at 16 MHz). 25 Mhz version is planned.
- 64K x 16 of addressable program memory space
- Direct, indirect (with auto increment and decrement), immediate and relative addressing
- Four modes of operation
  - Microcontroller mode
  - Secure microcontroller mode
  - Extended microcontroller mode (both internal and external program memory access)
  - Microprocessor mode (external only program memory access)

High level of Integration

- 2K x 16 on chip EPROM program memory
- 232 x 8 general purpose registers (SRAM)
- 48 special function registers
- 16 x 16 hardware stack
- 11 external/internal interrupts
- Up to 33 I/O pins
- Three 16-bit timer/counters
- Two 16-bit capture registers
- Two highs speed PWM outputs (10 bit, 15.6 KHz)
- Full featured serial port (USART) with baud rate generator

Special microcontroller features

- Watchdog timer with its own on-chip RC oscillator for reliable operation
- Power saving SLEEP mode
- On-chip power-up timer and power on reset saves external circuitry
- On-chip oscillator start-up timer
- Fuse selectable oscillator options: standard crystal oscillator, low frequency crystal oscillator, RC oscillator or external clocking
- Code protection feature to protect on-chip EPROM program memory

Package Options

- 40L cerdip window, 40L PDIP, 44L PLCC and 44L PQFP

PIC17C42 OVERVIEW

PIC17C42 is the first member of a high performance EPROM based 8-bit CMOS microcontroller family. The PIC17C42 integrates a powerful CPU (250 ns instruction cycle) with an array of peripheral resources making it ideal for complex real-time control applications.

Microchip's EPROM technology allows the user to test and develop code on windowed cerdip package version and move into production with the cost effective One Time Programmable (OTP) plastic DIP package version.

The PIC17C42 is fully supported by a host of software and hardware development tools. These include an assembler/linker, a low cost in-circuit emulator, a high performance in-circuit emulator, a programmer and a programmer/development board. A C compiler is planned. All tools are supported by PC AT and compatible platforms.

1.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC17C42 can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC17C42 uses a modified Harvard architecture, in which, program and data are accessed from separate memories. This improves bandwidth over traditional Von-Neuman architecture where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. In PIC17C42, opcodes are 16-bit wide making it possible to have all single word instructions. Full 16 bit wide program memory access bus fetches a 16 bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (55 in all) execute in a single cycle (250ns @ 16MHz) except for program branches and two special instructions that transfer data between program and data memory.

The PIC17C42 can address 64K x 16 program memory space. It integrates 2K x 16 EPROM program memory on-chip. Program execution can be internal only (microcontroller mode), external only (microprocessor mode) or both (extended microcontroller mode).

The PIC17C42 can directly or indirectly address 256 data memory locations (file registers). All special function registers including the program counter are mapped in the data memory. The PIC17C42 has a fairly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC17C42 simple yet efficient. In addition, the learning curve is reduced significantly.

FIGURE A: PIC17C42 BLOCK DIAGRAM

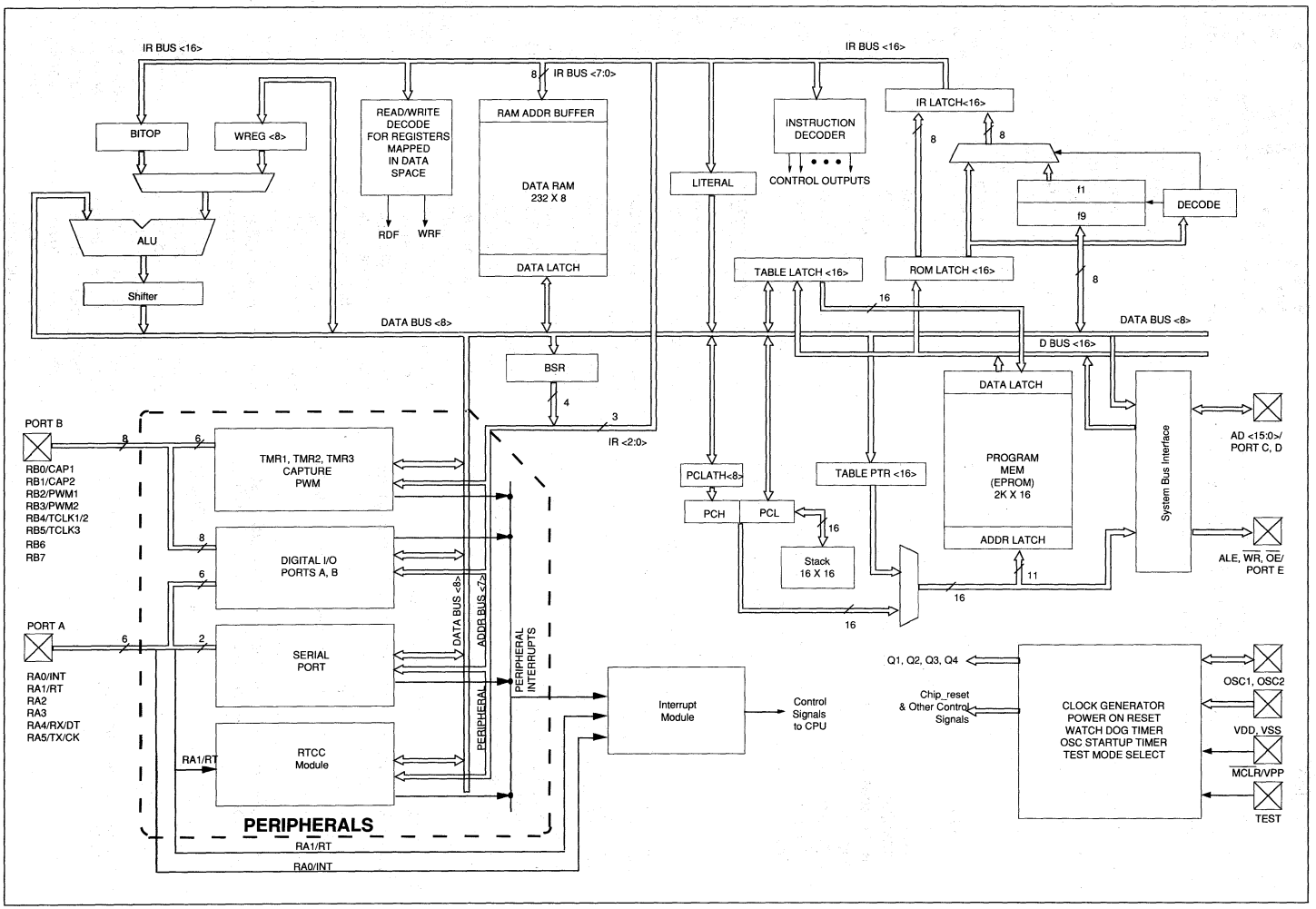
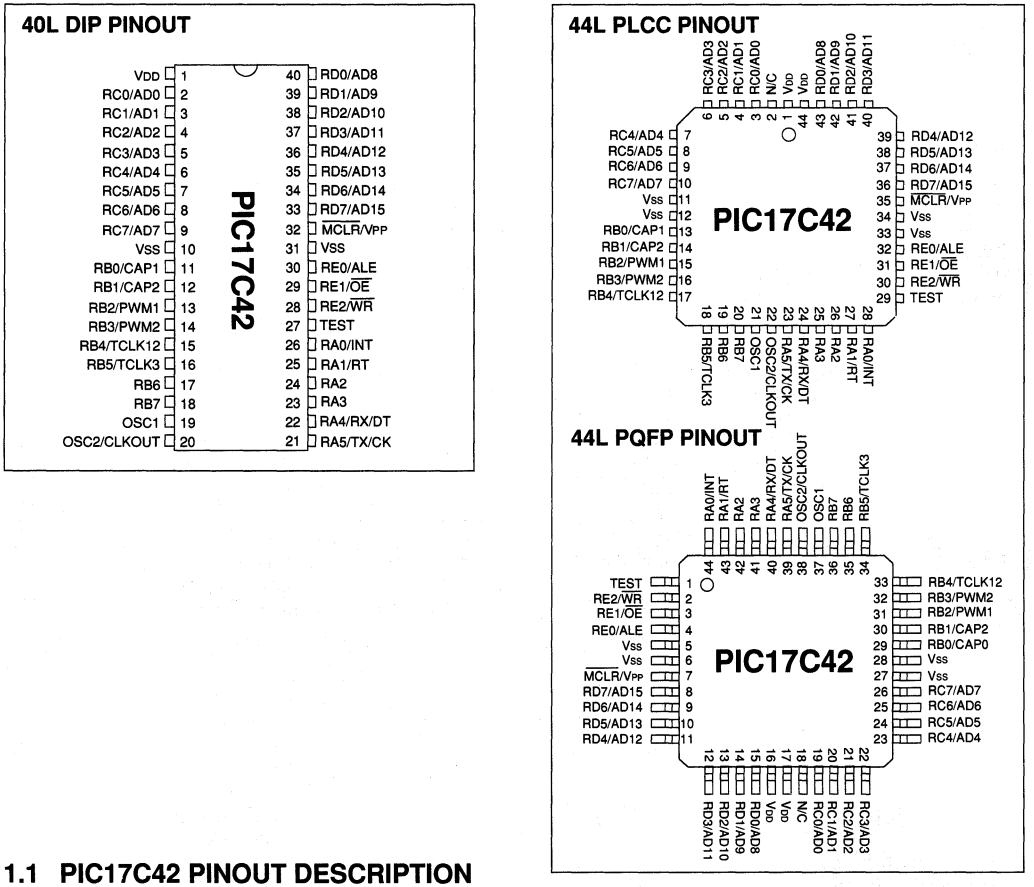


Table of Contents

Table of Figures

Table of Tables

FIGURE B: PIC17C42 PIN-OUT



1.1 PIC17C42 PINOUT DESCRIPTION

Pin Name	Pin Type	Number of Pins	Pin Function
MCLR/VPP	I/P	1	Master clear (reset) input. This is the active low reset input to the chip. During Programming mode, it is the programming voltage (VPP) input.
OSC1	I	1	Oscillator input in crystal/resonator or RC oscillator mode. External clock input in external clock mode.
OSC2/CLKOUT	O	1	Oscillator output. Connects to crystal or resonator in crystal oscillator mode. In RC oscillator or external clock modes OSC2 pin outputs CLKOUT which has one fourth the frequency of OSC1 and denotes the instruction cycle rate.
RA0/INT	I	1	Input only port pin (bit 0 of Port A) and also external interrupt input. Interrupt can be configured to be on positive or negative edge.
RA1/RT	I	1	Input only port pin (bit 1 of Port A) and also an external interrupt input. Interrupt can be configured to be on rising or falling edge. It is also the external clock input for the RTCC timer/counter.
RA2,RA3	I/O	2	High voltage, high current open drain input/output port pins.
RA4/RX/DT	I/O	1	Input only port pin (bit 4 of Port A). If the serial port is enabled, in full duplex asynchronous serial communication mode this is the receive pin. In half duplex synchronous serial communication mode it is data input (during receive) or data output (during transmit).
RA5/TX/CK	I/O	1	Input only port pin (bit 5 of Port A). If the serial port is enabled, in full duplex asynchronous serial communication mode it is the transmit pin. In half duplex synchronous communication mode, it is shift clock input (slave mode) or clock output (master mode).

(cont.)

Pin Name	Pin Type	Number of Pins	Pin Function
RB0/CAP1	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 0 of Port B). It is also the capture1 input pin.
RB1/CAP2	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 1 of Port B). It is also the capture2 input pin.
RB4/TCLK12	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 4 of Port B). It is also the external clock input to timer1 and timer2.
RB5/TCLK3	I/O	1	Port pin configurable as input or output in software, with Schmitt trigger input (bit 5, of Port B). It is also the external clock input to timer3.
RB6,RB7	I/O	2	Port pins configurable as input or output in software, with Schmitt trigger input (bits 6 and 7 of Port B).
RC7/AD7- RC0/AD0	I/O	8	Eight bit wide Port C with each pin software configurable as input or output. Input is TTL compatible (and not CMOS Schmitt trigger type). This is also the lower half of the 16 bit wide system bus in microprocessor mode or extended microcontroller mode. In multiplexed system bus configuration, these pins are address output as well as data input or output.
RD7/AD15- RD0/AD8	I/O	8	Eight bit wide Port D with each pin software configurable as input or output. Input is TTL compatible (and not CMOS Schmitt trigger type). This is also the upper byte of the 16 bit system bus in microprocessor mode or extended microprocessor mode or extended microcontroller mode. In multiplexed system bus configuration these pins are address output as well as data input or output.
RE0/ALE	I/O	1	Port pin configurable as input or output in software, with TTL compatible input (bit 0 of Port E). In microprocessor mode or extended microcomputer mode, it is the Address Latch Enable (ALE) output. Address should be latched on the falling edge of ALE output.
RE1/$\overline{OE}$	I/O	1	Port pin configurable as input or output in software, with TTL compatible input (bit 1 of Port E). In microprocessor or extended microcontroller mode, it is the Output Enable ($\overline{OE}$) control output (active low).
RE2/$\overline{WR}$	I/O	1	Port pin configurable as input or output in software, with TTL compatible input (bit 2 of Port E). In microprocessor or extended microcontroller mode, it is the Write Enable ($\overline{WR}$) control output (active low).
TEST	I	1	Test mode selection control input. Always tie to Vss for normal operation.
VDD	P	1	Power
Vss	P	2	Ground. Both pins must be connected to system ground.

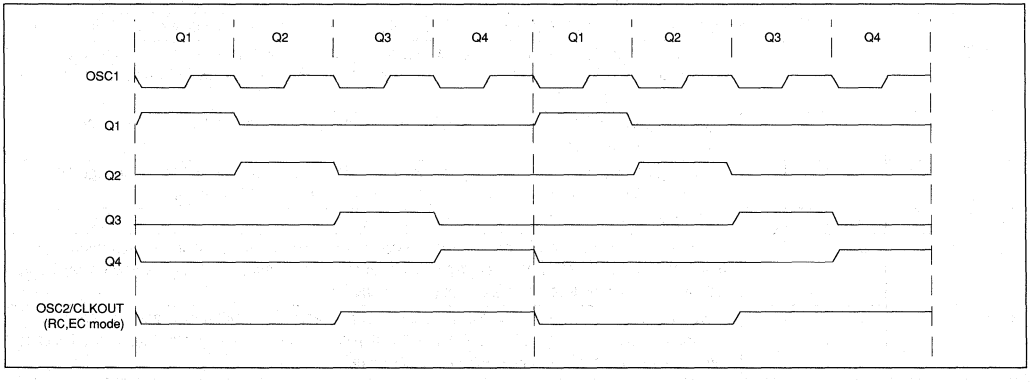
Legend: I = Input only; O = Output only; I/O = Input/output; P = Power.

1.2 INTERNAL CLOCKING SCHEME

Internally, the clock input to OSC1 pin is divided by four to generate four phases (Q1, Q2, Q3 and Q4) each with a frequency equal to fosc /4 and duty cycle of 25%. If EC (external clock) or RC oscillator mode is selected, the OSC2 pin provides a clock output, CLKOUT, which is high during Q3, Q4 and low during Q1, Q2.

As long as internal chip reset is active, the clock generator holds the chip in Q1 state. The CLKOUT pin is driven low (EC, RC mode).

FIGURE 1.2.1: INTERNAL CLOCKS



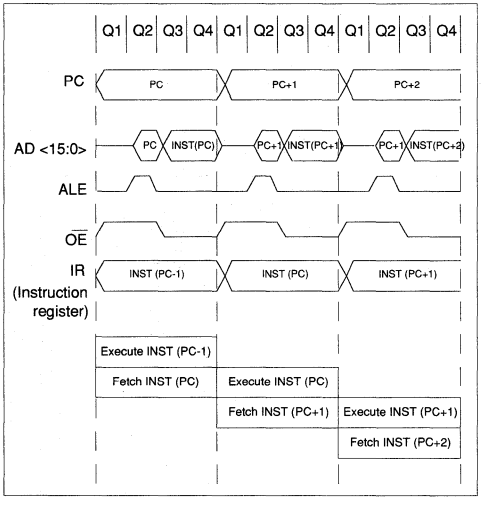
1.3 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" in PIC17C42 consists of Q1, Q2, Q3 and Q4. Instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction. Additionally, there are two instructions, TABLRD and TABLWT which take two or more cycles to complete. These are explained in more details 'Instruction Set' description.

A fetch cycle begins with the program counter (PC) incrementing in Q1. In external execution, the address is presented on pins AD15 - AD0 during Q2. The instruction is latched on the falling edge of Q4.

The fetched instruction is latched into the "Instruction Register (IR)" which is decoded in Q1 and executed during Q2, Q3 and Q4. Data memory is read during Q2 (operand read), ALU operations are done in Q3 and result is written back during Q4 (destination write).

FIGURE 1.3.1: INSTRUCTION FETCH/ EXECUTE PIPELINE



1.4 MEMORY ORGANIZATION

The PIC17C42 employs a Harvard architecture, i.e. it has separate program and data memory space. In addition, there is a hardware stack separate from both data and program space. The data space is 256 bytes in size. Most of the data space is implemented as static RAM (address 18h to FFh). Special function registers, implemented as individual hardware registers make up the rest of the data space. Refer to section 1.6 for more details. Data memory "address" and "data" buses are not brought outside the chip. So the data memory can not be expanded externally. The user can, however, create data segments in external program memory, use TABLWT and TABLRD instructions to move data between external program memory and the register file.

The program memory is 16 bits wide. It is addressed by the 16 bit program counter for instruction fetch. It is also addressed by the table pointer register (TBLPTR, also 16 bit wide) for data move to and from data space. Addressable program memory is 64K x 16. The PIC17C42 incorporates 2K x 16 EPROM program memory on chip.

1.5 DIFFERENT PROGRAM MEMORY ORGANIZATION

The PIC17C42 operates in on of four possible program memory configurations which are:

Microcontroller Mode: In this mode, only internal execution is allowed and therefore, only the on-chip 2K program memory is available. Any access to program memory beyond 2K reads 0000h (which is NOP). In addition to program memory, fuses, test memory, and boot memory (FE00h to FFFFh) are accessible.

Protected Microcontroller Mode: It is the same as microcontroller mode except that code protection is enabled. Refer to section 4.7 for details on code protection.

Extended Microcontroller Mode: In this mode, on chip program memory (0-2K) as well as external memory (2K - 64K) are available. Execution automatically switches to external if program memory address is greater than 07FFh. The fuses, test memory and the boot memory are not accessible in this mode.

Microprocessor Mode: In this mode the on-chip program memory is not used. The entire 64K program memory is mapped externally. The fuses, test memory and the boot memory are not accessible in this mode.

The different modes are selected by fuses FPMM0 and FPMM1. These fuses are mapped in the following program memory locations:

FPMM0: FE04h

FPMM1: FE06h

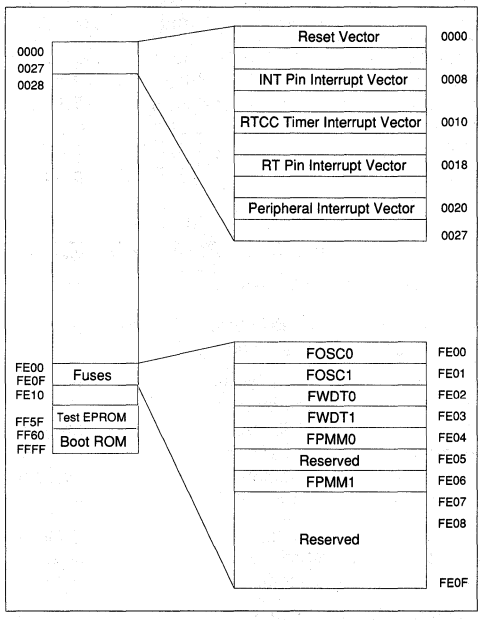
FPMM0	FPMM1	Mode
0	0	Microcontroller Mode (Code Protected)
0	1	Microcontroller Mode (Unprotected)
1	0	Extended Microcontroller Mode
1	1	Microprocessor Mode

Note: * 1 = fuse unprogrammed or erased,
0 = fuse programmed.

Refer to section 4.7 for information on code protection.

Test Memory, Boot Memory and Fuse Locations: Test memory space is used by the factory for testing purposes. The 'boot ROM' area holds programs used for programming and verification. The user need not be concerned about either of these. The fuse locations map configuration fuses used to select from various operating modes. The fuses are explained in detail, in section 4.8.

FIGURE 1.5.1: PROGRAM MEMORY MAP



1.5.1 External Program Memory interface

If external execution is selected, ports C, D and E are configured as a system bus for external program memory access. Ports D and C, together, constitute a 16 bit wide multiplexed address and data bus. The three bit E port outputs control signals ALE (Address Latch Enable), $\overline{OE}$ (Output Enable) and $\overline{WR}$ (Write Enable). An external memory access cycle is comprised of four oscillator cycles (from Q1 rising edge to Q1 rising edge). During Q2, a 16 bit address is presented on ports C and D (RD7 = MSB, RC0 = LSB) and ALE is asserted. The address output should be latched by the falling edge of ALE. In an instruction fetch or data read cycle, the $\overline{OE}$ is asserted during Q3 and Q4. The data is latched on the rising edge of $\overline{OE}$. One oscillator cycle separation between $\overline{OE}$ ↑ and address output guarantees adequate time for external memories to shut off their output drivers before address is driven on to the bus.

In a data write cycle (only during TABLWT instruction), following address output during Q2, data is driven onto the bus during Q3 and Q4. $\overline{WR}$ is asserted during Q4 and the data output is valid both on its falling and rising edge.

Figure 1.5.1.1 depicts read and write cycles and table 1.5.1.1 shows access time required of the external memory components. For complete timing information on the system bus, refer to AC characteristics section.

FIGURE 1.5.2: MEMORY MAP IN DIFFERENT MODES

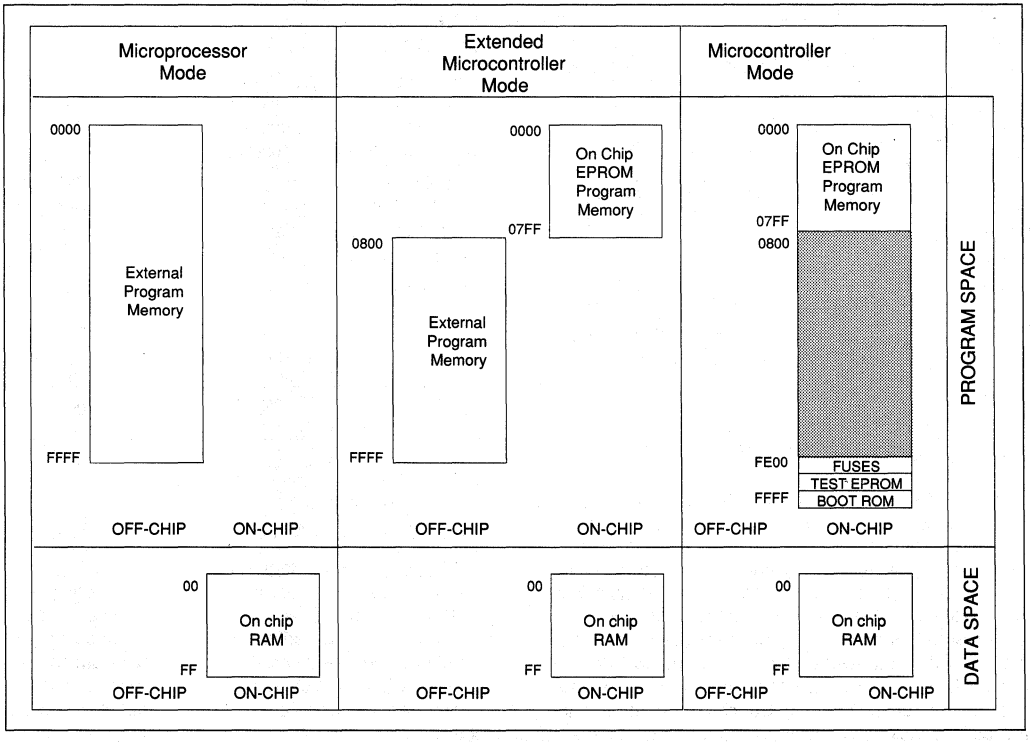


FIGURE 1.5.1.1: EXTERNAL PROGRAM MEMORY READ AND WRITE TIMINGS

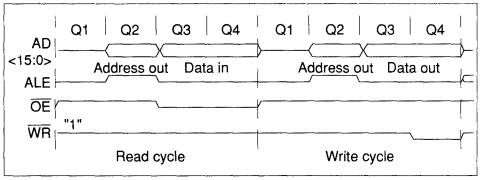


TABLE 1.5.1.2: ACCESS TIME REQUIREMENTS FOR EXTERNAL MEMORY

Osc frequency	Instruction cycle time (Tcy)	tacc	toe
8 MHz	500 ns	345 ns	115 ns
16 MHz	250 ns	157.5 ns	52.5 ns
20 MHz	200 ns	120 ns	40 ns
25 MHz	160 ns	90 ns	30 ns

Note: Estimated access time requirements. Exact number will be available after full characterization.

1.6 DATA MEMORY ORGANIZATION

Data memory in the PIC17C42 is organized as 256 x 8. It is accessed via an internal 8 bit data bus and an 8 bit data-memory-address-bus (derived from the instruction register). Data memory can be addressed via direct addressing mode or through indirect addressing mode using file select registers FSR0 or FSR1 as pointer registers.

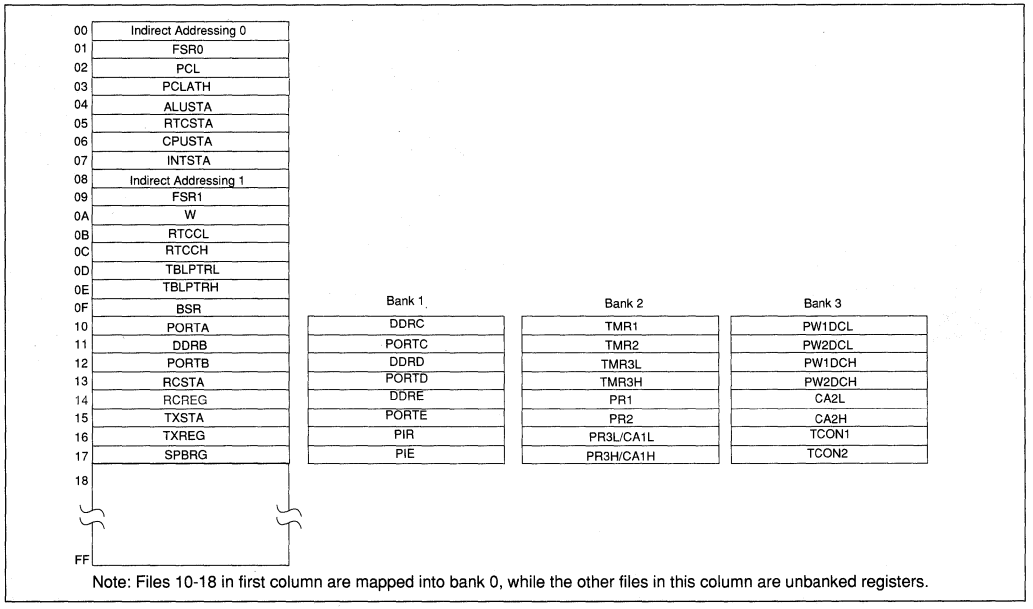
All special function registers (e.g. W, RTCC, Program Counter, Ports) are mapped in the data memory. The rest of the data memory is implemented as static RAM. A few special function registers such as Table Latches (TBLATH, TBLATL) are not mapped in data memory or any other memory space. Also not addressable are the watchdog timer and the stack pointer.

1.6.1 Organization of Special Function Registers

Figure 1.6.1 shows the data memory space in detail:

a. Address 00h:0Fh are mostly special function registers related to the CPU.
b. Address 10h:17h are 'peripheral registers' such as timer register or port data latch. Since there are many more peripheral registers than can be mapped into 8 address locations, a banking scheme is used. A bank select register, BSR (address 0Fh) is used to select one of many banks. Only the lower 4 bits of BSR are implemented in the PIC17C42, making it possible to address up to 16 banks.
c. Address locations 18h:1Fh are general purpose file registers implemented as part of the static RAM. However, these locations have the added privilege of being source or destination of a MOVPF or MOVFP instruction respectively.
d. Locations 20h:FFh are general purpose file registers implemented as static RAM.

FIGURE 1.6.1: DATA MEMORY MAP



Note: Files 10-18 in first column are mapped into bank 0, while the other files in this column are unbanked registers.

FIGURE 1.6.2: REGISTER FILE SUMMARY (PIC17C42)

Filename		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0	Value on power on reset	Value on all other reset (note3)	
UNBANKED:												
00	INDF0	Uses contents of F1 to address data memory (not a physical register)								00000000	00000000	
01	FSR0	Indirect data memory address pointer 0								XXXXXXXX	UUUUUUUU	
02	PCL	Low order 8 bits of PC								00000000	00000000	
03	PCLATH	Holding register for upper 8 bits of PC (Note 1)								XXXXXXXX	UUUUUUUU	Note 1
04	ALUSTA	FS3	FS2	FS1	FS0	OV	Z	DC	C	1111XXXX	1111UUUU	
05	RTCSTA	INTEDG	RTEDG	T/C	RTPS3	RTPS2	RTPS1	RTPS0	-	00000000	00000000	
06	CPUSTA	-	-	STKAV	GLINTD	TO	PD	-	-	00111100	0011??00	Note 2
07	INTSTA	PEIR	RTXIR	RTCIR	INTIR	PEIE	RTXIE	RTCIE	INTIE	00000000	00000000	
08	INDF1	Uses contents of F9 to address data memory (not a physical register)								00000000	00000000	
09	FSR1	Indirect data memory address pointer 1								XXXXXXXX	UUUUUUUU	
0A	W	W register								XXXXXXXX	UUUUUUUU	
0B	RTCCL	Real time clock counter LS byte								XXXXXXXX	UUUUUUUU	
0C	RTCCH	Real time clock counter MS byte								XXXXXXXX	UUUUUUUU	
0D	TBLPTRL	Low byte of program memory table pointer								XXXXXXXX	UUUUUUUU	
0E	TBLPTRH	High byte of program memory table pointer								XXXXXXXX	UUUUUUUU	
0F	BSR	Bank select register								00000000	00000000	
BANK0:												
10	PORTA	PUEB	-	RA5	RA4	RA3	RA2	RA1/RT	RA0/INT	00XXXXXX	00UUUUUU	
11	DDRB	Data Direction Register for Port B								11111111	11111111	
12	PORTB	Port B data latch								XXXXXXXX	UUUUUUUU	
13	RCSTA	SPEN	RC8/9	SREN	CREN	-	FERR	OERR	RCD8	0000000X	0000000U	
14	RCREG	Serial Port Receive Register								XXXXXXXX	UUUUUUUU	
15	TXSTA	CSRC	TX8/9	TXEN	SYNC	-	-	TRMT	TXD8	0000001X	0000001U	
16	TXREG	Serial Port Transmit Register								XXXXXXXX	UUUUUUUU	
17	SPBRG	Baud Rate Generator								XXXXXXXX	UUUUUUUU	
BANK1:												
10	DDRC	Data Direction Register for Port C								11111111	11111111	
11	PORTC	Port C data latch								XXXXXXXX	UUUUUUUU	
12	DDRD	Data Direction Register for Port D								11111111	11111111	
13	PORTD	Port D data latch								XXXXXXXX	UUUUUUUU	
14	DDRE	Data Direction Register for Port E								00000111	00000UUU	
15	PORTE	Port E data latch								00000XXX	00000UUU	
16	PIR	IRB	TM3IR	TM2IR	TM1IR	CA2IR	CA1IR	TBMT	RBFL	00000010	00000010	
17	PIE	IEB	TM3IE	TM2IE	TM1IE	CA2IE	CA1IE	TXIE	RCIE	00000000	00000000	
BANK2:												
10	TMR1	Timer1								XXXXXXXX	UUUUUUUU	
11	TMR2	Timer2								XXXXXXXX	UUUUUUUU	
12	TMR3L	Timer3 Low byte								XXXXXXXX	UUUUUUUU	
13	TMR3H	Timer3 High byte								XXXXXXXX	UUUUUUUU	
14	PR1	Timer1 Period Register								XXXXXXXX	UUUUUUUU	
15	PR2	Timer2 Period Register								XXXXXXXX	UUUUUUUU	
16	PR3L/CA1L	Timer3 Period Register, low byte/capture1 register, low byte								XXXXXXXX	UUUUUUUU	
17	PR3H/CA1H	Timer3 Period Register, High byte/capture1 register, high byte								XXXXXXXX	UUUUUUUU	
BANK3:												
10	PW1DCL	DC1	DC0	-	-	-	-	-	-	XX000000	UU000000	
11	PW2DCL	DC1	DC0	TM2PW2	-	-	-	-	-	XX000000	UU000000	
12	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	XXXXXXXX	UUUUUUUU	
13	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	XXXXXXXX	UUUUUUUU	
14	CA2L	Capture2 low byte								XXXXXXXX	UUUUUUUU	
15	CA2H	Capture2 high byte								XXXXXXXX	UUUUUUUU	
16	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	16/8	TMR3C	TMR2C	TMR1C	00000000	00000000	
17	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	00000000	00000000	

x = unknown
u = unchanged

Notes:

1: The upper byte of the program counter is not directly accessible. f03 is a holding register for PC<15:8> whose contents are updated from or transfered to the upper byte of the program counter.

2: The "TO" and PD" status bits in f06h are not affected by a "MCLR" reset. TO bit will be reset in the event of a WDT time-out reset.

3: Other (non power-up) resets include external reset through MCLR pin and watchdog timer timeout reset.

2.0 INSTRUCTION SET

The PIC17C42 instruction set consists of 55 instructions, each single word and 16 bit wide. Most instructions operate on a file register f and the working register W (accumulator). Depending on the instruction, the result may be directed to the file register, or the working register (W) or to both.

All instructions are executed in a single instruction cycle unless otherwise noted.

Any unused op-code is executed as a NOP.

The instruction set is highly orthogonal and is grouped into

- Data Move Operations
- Arithmetic and Logical Operations
- Bit Manipulation Operations
- Program Control Operations
- Special Control Operations

Data Move Instructions

Instruction Code Binary	Hex	mnemonic		Description	Function	Status bits Affected	Notes
011p pppp ffff ffff	6pff	MOVFP	f,p	Move f to p	f → p	None	4
1011 1000 kkkk kkkk	B8kk	MOVLB	k	Move literal to BSR	k → BSR	None	
010p pppp ffff ffff	4pff	MOVPF	p,f	Move p to f	p → f	Z	4
0000 0001 ffff ffff	01ff	MOVWF	f	Move W to f	W → f	None	
1010 10ti ffff ffff	A8ff	TABLRD	t,i,f	Read data from table latch into file f, then update table latch with 16-bit contents of memory location addressed by the table pointer.	TBLATH → f if t =1, TBLATL → f if t =0; Prog Mem (TBLPTR) → TBLAT; TBLPTR + 1 → TBLPTR if i =1;	None	8,10
1010 11ti ffff ffff	ACff	TABLWT	t,i,f	Write data from file f to table latch and then Write 16-bit table latch to program memory location addressed by table pointer. It also intitiates programming if on-chip EPROM program memory is addressed.	f → TBLATH if t =1, f →TBLATL if t =0; TBLAT → Prog Mem (TBLPTR); TBLPTR + 1 → TBLPTR if i =1	None	6
1010 00tx ffff ffff	A0ff	TLRD	t,f	Read data from table latch into file f (table latch unchanged).	TBLATH → f if t =1, TBLATL → f if t =0	None	
1010 01tx ffff ffff	A4ff	TLWT	t,f	Write data from file f into table latch.	f → TBLATH if t =1, f →TBLATL if t =0	None	

Arithmetic and Logical Instructions

Instruction Code Binary	Hex	mnemonic		Description	Function	Status bits Affected	Notes
1011 0001 kkkk kkkk	B1kk	ADDLW	k	Add literal to W	(W+k) → W	OV C DC Z	
0000 111d ffff ffff	0Eff	ADDWF	f,d	ADD W to f	(W+f) → d	OV C DC Z	
0001 000d ffff ffff	10ff	ADDWFC	f,d	ADD W and Carry to f	(W+f+C) → d	OV C DC Z	
1011 0101 kkkk kkkk	B5kk	ANDLW	k	AND literal and W	(W.AND.k) → W	Z	
0000 101d ffff ffff	0Aff	ANDWF	f,d	AND W with f	(W.AND.f) → d	Z	
0010 100d ffff ffff	28ff	CLRF	f,d	Clear f and Clear d	"00h" → f, "00h" → d	None	3
0001 001d ffff ffff	12ff	COMF	f,d	Complement f	$\overline{f}$ → d	Z	
0010 111d ffff ffff	2Eff	DAW	f,d	Dec. adjust W, store in f,d	W adjusted → f and d	C	3
0000 011d ffff ffff	06ff	DECF	f,d	Decrement f	(f-1)→ d	OV C DC Z	
0001 010d ffff ffff	14ff	INCF	f,d	Increment f	(f+1) → d	OV C DC Z	
1011 0011 kkkk kkkk	B3kk	IORLW	k	Inclusive OR literal with W	(W.OR.k) → W	Z	
0000 100d ffff ffff	08ff	IORWF	f,d	Inclusive OR W with f	(W.OR.f) → d	Z	
1011 0000 kkkk kkkk	B0kk	MOVLW	k	Move literal to W	$\underline{k}$ → W	None	
0010 110d ffff ffff	2Cff	NEGW	f,d	Negate W, store in f and d	$\overline{(W+1)}$ → f, $\overline{(W+1)}$ → d	OV C DC Z	1,3
0001 101d ffff ffff	1Aff	RLCF	f,d	Rotate left through Carry	f<n>→d<n+1>, f<7>→C, C→d<0>	C	
0010 001d ffff ffff	22ff	RLNCF	f,d	Rotate left (no Carry)	f<n>→ d<n+1>, f<7>→ d<0>	None	
0001 100d ffff ffff	18ff	RRCF	f,d	Rotate right through Carry	f<n>→d<n-1>, f<0>→C, C→d<7>	C	
0010 000d ffff ffff	20ff	RRNCF	f,d	Rotate right (no Carry)	f<n>→ d<n-1>, f<0>→ d<7>	None	
0010 101d ffff ffff	2Aff	SETF	f,d	Set f and Set d	"FFh" → f, "FFh"→ d	None	3
1011 0010 kkkk kkkk	B2kk	SUBLW	k	Subtract W from literal	(k-W) → W	OV C DC Z	
0000 010d ffff ffff	04ff	SUBWF	f,d	Subtract W from f	(f-W) → d	OV C DC Z	1
0000 001d ffff ffff	02ff	SUBWFB	f,d	Subtract W from f with borrow	(f-W-c)→ d	OV C DC Z	1
0001 110d ffff ffff	1Cff	SWAPF	f,d	Swap f	f<0:3> → d<4:7>, f<4:7> → d <0:3>	None	
1011 0100 kkkk kkkk	B4kk	XORLW	k	Exclusive OR literal with W	(W.XOR.k) → W	Z	
0000 110d ffff ffff	0Cff	XORWF	f,d	Exclusive OR W with f	(W.XOR.f) → d	Z	

Program Control Instructions

Instruction Code Binary	Hex	mnemonic		Description	Function	Status bits Affected	Notes
111k kkkk kkkk kkkk	Ekkk	CALL	k	Subroutine call (within 8K page boundary)	PC+1 → TOS, k → PC<12:0>; k<12:8> → f3<4:0>, PC<15:13> → f3<7:5>	None	8
0011 0001 ffff ffff	31ff	CPFSEQ	f	Compare f/W skip if f=W	f - W, skip if f = W	None	7
0011 0010 ffff ffff	32ff	CPFSGT	f	Compare f/W skip if f>W	f - W, skip if f > W	None	2,7
0011 0000 ffff ffff	30ff	CPFSLT	f	Compare f/W skip if f<W	f - W, skip if f < W	None	2,7
0001 011d ffff ffff	16ff	DECFSZ	f,d	Decrement f, skip if 0	(f-1) → d, skip if result =0	None	7
0010 011d ffff ffff	26ff	DCFSNZ	f,d	Decrement f skip if not 0	(f-1) → d, skip if not 0	None	7
110k kkkk kkkk kkkk	Ckkk	GOTO	k	Unconditional branch (within 8K page boundary)	k → PC<12:0>, k<12:8> → f3<4:0>, PC<15:13> → f3 <7:5>	None	8
0001 111d ffff ffff	1Eff	INCFSZ	f,d	Increment f skip if 0	(f+1) → d, skip if result 0	None	7
0010 010d ffff ffff	24ff	INFSNZ	f,d	Increment f skip if not 0	(f+1) → d, skip if not 0	None	7
1011 0111 kkkk kkkk	B7kk	LCALL	k	Long Call (anywhere in 64K range)	(PC+1) → TOS; (f3) → PCH; k → PCL	None	5,8
0000 0000 0000 0101	0005	RETFIE		Return from interrupt and enable interrupt	TOS → PC (f3 unchanged) "0" → GLINTD	GLINTD	8
1011 0110 kkkk kkkk	B6kk	RETLW	k	Return literal to W	k → W, TOS → PC, f3 unchanged	None	8
0000 0000 0000 0010	0002	RETURN		Return from subroutine	TOS→ PC (f3 unchanged)	None	8
0011 0011 ffff ffff	33ff	TSTFSZ	f	Test f skip if 0	skip if f = 0	None	7

Bit Handling Instructions

Instruction Code Binary	Hex	mnemonic		Description	Function	Status bits Affected	Notes
1000 1bbb ffff ffff	8bff	BCF	f,b	Bit clear f	0 → f(b)	None	4
1000 0bbb ffff ffff	8bff	BSF	f,b	Bit set f	1 → f(b)	None	4
1001 1bbb ffff ffff	9bff	BTFSC	f,b	Bit test, skip if clear	skip if f(b) = 0	None	4,7
1001 0bbb ffff ffff	9bff	BTFSS	f,b	Bit test, skip if set	skip if f(b) = 1	None	4,7
0011 1bbb ffff ffff	3bff	BTG	f,b	Bit Toggle f	$\overline{f(b)}$ → f(b)	None	4

Special control instructions

Instruction Code Binary	Hex	mnemonic	Description	Function	Status bits Affected	Notes
0000 0000 0000 0100	0004	CLRWDT	Clear watch dog timer	0 → WDT, 0 → WDT prescaler, 1 → $\overline{PD}$, 1 → $\overline{TO}$	$\overline{PD}$, $\overline{TO}$	
0000 0000 0000 0000	0000	NOP	No operation	None	None	
0000 0000 0000 0011	0003	SLEEP	Enter "sleep" mode	Stop oscillator,"power down" 0 → $\overline{WDT}$, 0 → $\overline{WDT}$ prescaler, 1 → $\overline{TO}$, 1 → $\overline{PD}$	$\overline{PD}$, $\overline{TO}$	

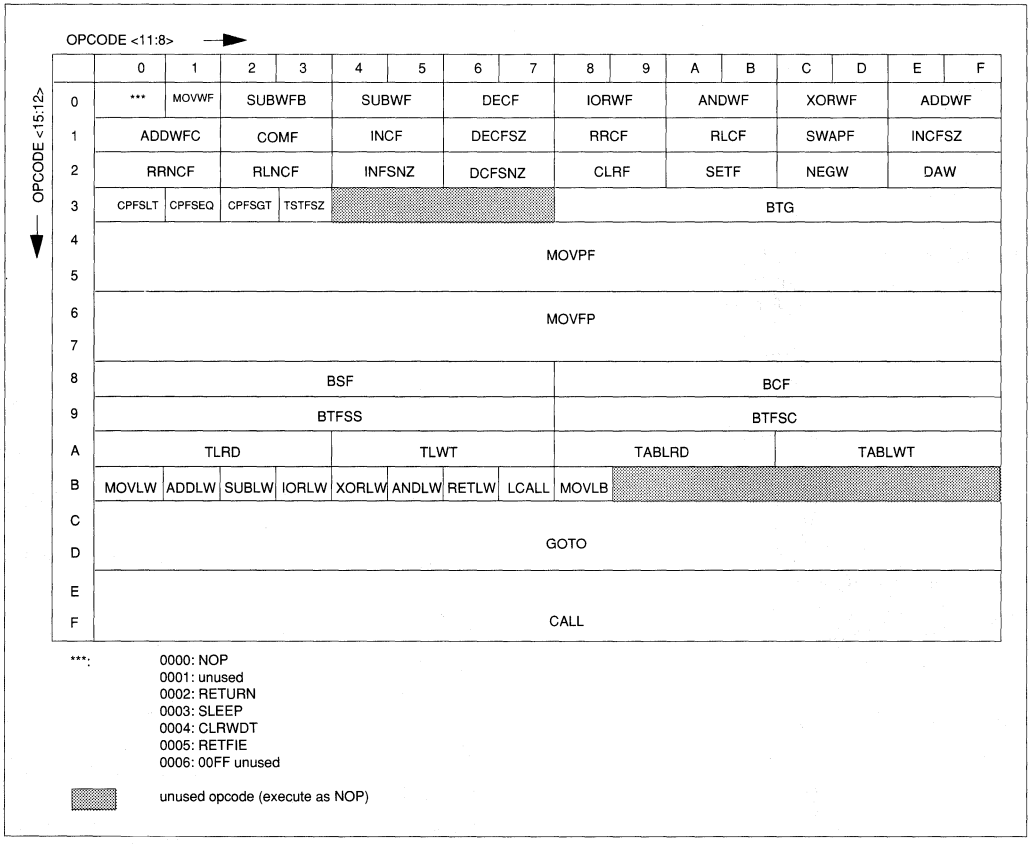
Legend:

f	register file address (00h to FFh)
p	peripheral register file address (00h to 1Fh)
b	bit address with in 8 bit file register
i	table pointer control i = 0: do not change i = 1: increment after instruction execution
t	table byte select t = 0: perform operation on lower byte t = 1: perform operation on upper byte
k	literal field (constant data)
x	don't care
d	destination select; d=0 store result in W (f0A) d=1 store result in file register 'f'
C,DC,Z,OV	ALU status bits Carry, Digit Carry, Zero, Overflow
$\overline{TO}$, $\overline{PD}$	CPU status bits Time-out and Power-down
GLINTD	GLobal Interrupt Disable bit (bit 4, CPUSTA)
W	W-register
PC	Program counter
TBLPTR	Table Pointer (16 bit)
TBLAT	Table Latch (16 bit) consists of high byte (TBLATH) and low byte (TBLATL)
TBLATL	Table latch low byte
TBLATH	Table latch high byte
WDT	Watchdog timer
BSR	Bank Select Register
TOS	Top of Stack

Notes:

1) 2's Complement method.
2) Unsigned arithmetic
3) If d=1, only the file is affected; If d=0, both W and the file are affected; If only W is required to be affected, then f=0Ah (File 0Ah) must be defined.
4) The HEX representation is not accurate. The value of the bit to be modified has to be incorporated into the third digit.
5) During an LCALL, the contents of file 03h are loaded into the MSB of the PC and kkkk kkkk is loaded into file 02h the LSB of the PC.
6) Multiple cycle instruction for EPROM programming when table pointer selects internal EPROM. The instruction is terminated by an interrupt event.
   When writing to external program memory, it is a two cycle instruction.
7) Two cycle instructions when condition is true, else single cycle instruction.
8) Two cycle instruction except for TABLRD to f02h (Program Counter low byte) in which case it takes 3 cycles.
9) A 'skip' means that instruction fetched during execution of current instruction is not executed. Instead a 'NOP' is executed.
10) Any instruction that writes to PCL (f02) is a two cycle instruction,
    execpt for TABLRD to f02 is a 3 cycle instruction.

FIGURE 2.0.1: INSTRUCTION DECODE MAP



2.1 SPECIAL FUNCTION REGISTERS AS SOURCE/DESTINATION

PIC17C42's orthogonal instruction set allows read and write of all file registers, including special function registers such as PC and status registers. There are some special situations the user should be aware of:

ALUSTA as destination (file 04h): If an instruction writes to ALUSTA, the Z, C, DC and OV bits may be set or reset as a result of the instruction and overwrite the original data bits written. For example, executing CLRF 04 will clear register 04, and then set Z bit leaving 00000100b first in the register.

PCL as source or destination (file 02h): Read, write or read-modify-write on PCL (f02) have the following results:

Read PCL (f02):	PCH → PCLATH; PCL → d
Write PCL (f02):	PCLATH → PCH; 8 bit destination value → PCL
Read-Modify-Write:	PCL → ALU operand PCLATH → PCH; 8 bit result → PCL

Where PCH = program counter high byte (not a addressable register), PCLATH = Program counter high holding latch (file f03), d = destination, W or f.

Bit Manipulation

All bit manipulation instructions are done by first reading the entire register, operating on the selected bit and writing the result back (read-modify-write). The user should keep this in mind when operating on special function registers, such as ports.

2.2 INSTRUCTION DESCRIPTION

ADDLW Add literal to W

Syntax: ADDLW k

Encoding:	1011	0001	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W + k) → W

Status bits: OV, C, DC, Z

Description: The contents of the W register are added to the eight bit literal "k" and the result is placed in the W register.

ADDWF ADD W to f

Syntax: ADDWF f,d

Encoding:	0000	111d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W + f) → d

Status bits: OV, C, DC, Z

Description: Add the contents of the W register to data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

ADDWFC ADD W and Carry to f

Syntax: ADDWFC f,d

Encoding:	0001	000d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W + f + C) → d

Status bits: OV, C, DC, Z

Description: Add the W register and the Carry Flag to data memory location "f". If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f".

ANDLW AND literal and W

Syntax: ANDLW k

Encoding:	1011	0101	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .AND. k) → W

Status bits: Z

Description: The contents of W register are AND'ed with the eight bit literal "k". The result is placed in the W register.

ANDWF AND W with f

Syntax: ANDWF f,d

Encoding:	0000	101d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W .AND. f) → d

Status bits: Z

Description: AND the W register with data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

BCF Bit Clear f

Syntax: BCF f,b

Encoding:	1000	1bbb	ffff	ffff

Words: 1

Cycles: 1

Operation: 0 → f(b)

Status bits: None

Description: Bit "b" in data memory location "f" is reset to 0.

BSF Bit Set f

Syntax: BSF f,b

Encoding:	1000	0bbb	ffff	ffff

Words: 1

Cycles: 1

Operation: 1 → f(b)

Status bits: None

Description: Bit "b" in data memory location "f" is set to 1.

BTFSC Bit test, skip if clear

Syntax: BTFSC f,b

Encoding:	1001	1bbb	ffff	ffff

Words: 1

Cycles: 1(2)

Operation: skip if f(b) = 0

Status bits: None

Description: If bit "b" in data memory location "f" is "0" then the next instruction is skipped.

If bit "b" is "0", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

BTFSS Bit test, skip if set

Syntax: BTFSS f,b

Encoding:	1001	0bbb	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f(b) = 1

Status bits: None

Description: If bit "b" in data memory location "f" is "1" then the next instruction is skipped.

If bit "b" is "1", the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

BTG Bit Toggle f

Syntax: BTG f,b

Encoding:	0011	1bbb	ffff	ffff

Words: 1

Cycles: 1

Operation: f(b) → f(b)

Status bits: None

Description: Bit "b" in data memory location "f" is inverted.

CALL Subroutine Call

Syntax: CALL k

Encoding:	111k	kkkk	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC + 1 → TOS, k → PC<12:0>, k<12:8> → PCLATH<4:0>; PC<15:13> →PCLATH<7:5>

Status bits: None

Description: Subroutine call within 8K page. First, return address (PC + 1) is pushed into the stack. The thirteen bit value is loaded into PC bits <12:0>. Then the upper eight bits of the PC is copied into PCLATH (f03). CALL is a two cycle instruction.

CLRF Clear f and Clear d

Syntax: CLRF f,d

Encoding:	0010	100d	ffff	ffff

Words: 1

Cycles: 1

Operation: 00h → f, 00h → d

Status bits: None

Description: The contents of data memory location "f" are set to 0. If "d" is 0 the contents of both data memory location "f" and W register are set to 0. If "d" is 1 the only contents of data memory location "f" are set to 0.

CLRWDT Clear Watchdog Timer

Syntax: CLRWDT

Encoding:	0000	0000	0000	1000

Words: 1

Cycles: 1

Operation: 00h →$\overline{\text{WDT}}$, 0 → $\overline{\text{WDT}}$ prescaler,

Status bits: 1 → TO, 1 → PD

Description: CLRWDT instruction resets the watchdog timer.It also resets the prescaler of the WDT. Status bits TO and PD are set.

COMF Complement f

Syntax: COMF f,d

Encoding:	0001	001d	ffff	ffff

Words: 1

Cycles: 1

Operation: f → d

Status bits: Z

Description: The contents of data memory location "f" are complemented.If "d" is 0 the result is stored in W. If "d" is 1 the result is stored in data memory location "f".

CPFSEQ Compare f with W, skip if f = W

Syntax: CPFSEQ f

Encoding:	0011	0001	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: f - W, skip if f = W

Status bits: None

Description: If the contents of data memory location "f" are equal to the contents of the W register, the next instruction is skipped.

If f = W then the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed instead making this a 2 cycle instruction.

CPFSGT Compare f with W, skip if f > W

Syntax: CPFSGT f

Encoding:

0011	0010	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: f - W, skip if f > W (unsigned comparison)

Status bits: None

Description: If the contents of data memory location "f" are greater than the contents of the W register, the next instruction is skipped. The subtraction is unsigned.

If f > W then the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this a 2 cycle instruction.

CPFSLT Compare f with W, skip if f< W

Syntax: CPFSLT f

Encoding:

0011	0000	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: f - W, skip if f < W (unsigned)

Status bits: None

Description: If the contents of data memory location "f" are less than the contents of the W register, the next instruction is skipped. The subtraction is unsigned.

If f < W then the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this a 2 cycle instruction.

DAW Decimal Adjust W Register

Syntax: DAW f,d

Encoding:

0010	111d	ffff	ffff

Words: 1

Cycles: 1

Operation: if [W<3:0> >9] .OR. [DC = 1] then W<3:0> + 6 → f<3:0>, d<3:0>; if [W<7:4> >9] .OR. [C = 1] then W<7:4> + 6 → f<7:4>, d<7:4>;

Status bits: C

Description: DAW adjusts the eight bit value in the W register resulting from the earlier addition of two variables (each in packed BCD format) and produces a correct packed BCD result. If "d" is 0 the result is placed in the W register and data memory location "f". If "d" is 1 the result is placed only in data memory location "f".

The Decimal Adjust Algorithm is as follows:

Step 1: If the lower nibble of W is greater then 9 or if the DC flag (Digit Carry) is set from previous operations, then 06h is added to W.

Step 2: If upper nibble is greater then 9 or if C flag (Carry) is set following Step 1 operation, 60h is added to W

The Carry flag may be set as a result of Step 1 or Step 2 operation.

DECF Decrement f

Syntax: DECF f,d

Encoding:

0000	011d	ffff	ffff

Words: 1

Cycles: 1

Operation: (f-1) → d

Status bits: OV, C, DC, Z

Description: Decrement data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

DECFSZ Decrement f, skip if 0

Syntax: DECFSZ f,d

Encoding:

0001	011d	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f - 1) → d; skip if result = 0

Status bits: None

Description: The contents of data memory location "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f". If the result is 0 the next instruction is skipped.

If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

DCFSNZ Decrement f, skip if not 0

Syntax: DCFSNZ f,d

Encoding:

0010	011d	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f-1) → d, skip if not 0

Status bits: None

Description: The contents of data memory location "f" are decremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f".

If the result is not 0, the next instruction, fetched during the current instruction execution is discarded. A NOP is executed instead making this a 2 cycle instruction.

GOTO Unconditional Branch

Syntax: GOTO k

Encoding:

110k	kkkk	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → PC<12:0>; k<12:8> → f3<4:0>, PC<15:13> → f3<7:5>

Status bits: None

Description: GOTO allows an unconditional branch anywhere within an 8K page boundary. The thirteen bit immediate value is loaded into PC bits <12:0>. Then the upper eight bits of PC are loaded into PCLATH (file 3). GOTO is always a two cycle instruction.

INCF Increment f

Syntax: INCF f,d

Encoding:

0001	010d	ffff	ffff

Words: 1

Cycles: 1

Operation: (f + 1) → d

Status bits: OV, C, DC, Z

Description: The contents of data memory location "f" are incremented. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is place in data memory location "f".

INCFSZ Increment f, skip if 0

Syntax: INCFSZ f,d

Encoding:

0001	111d	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: (f+1) → d, skip if result = 0

Status bits: None

Description: The contents of data memory location "f" are incremented. If "d" is 0 the result is placed in the W register.

If "d" is 1 the result is placed in data memory location "f". If the result is 0 the next instruction is skipped. If the result is 0 the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this the 2 cycle case.

INFSNZ Increment f, skip if not 0

Syntax: INFSNZ f,d

Encoding:

0010	010d	ffff	ffff

Words: 1

Cycles: 1(2)

Operation: (f+1) → d, skip if not 0

Status bits: None

Description: The contents of data memory location "f" are incremented. If "d" is 0 the result is placed in the W register.

If "d" is 1 the result is placed in data memory location "f". If the result is not 0 the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this a 2 cycle instruction.

IORLW Inclusive OR literal with W

Syntax: IORLW k

Encoding:

1011	0011	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .OR. k) → W

Status bits: Z

Description: The contents of the W register are inclusively OR'ed with the eight bit literal "k". The result is placed in the W register.

IORWF Inclusive OR W with f

Syntax: IORWF f,d

Encoding:

0000	100d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W .OR. f) → d

Status bits: Z

Description: Inclusive OR the W register with data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

LCALL Long Call

Syntax: LCALL k

Encoding:

1011	0111	kkkk	kkkk

Words: 1

Cycles: 2

Operation: PC+1 → TOS;
k → PCL, (PCLATH) → PCH

Status bits: None

Description: LCALL allows unconditional subroutine call to anywhere within the 64k program memory space. First, the return address (PC+1) is pushed onto the stack. A 16 bit destination address is then loaded into the program counter. The lower 8 bit of the destination address is embedded in the instruction. The upper 8 bit of PC is loaded from PC high holding latch, PCLATH. LCALL is a two cycle instruction.

Example:
```
MOVLW   56h       ; W = 56h
MOVPF   W,PCLATH  ; PCLATH = 56h
LCALL   3Ah       ; CALL 563Ah
```

MOVFP Move f to p

Syntax: MOVFP f,p

Encoding:

011p	pppp	ffff	ffff

Words: 1

Cycles: 1

Operation: f → p

Status bits: None

Description: Move data from data memory location "f" to data memory location "p". Location "f" can be anywhere in the 256 word data space (00h to FFh) while "p" can be 00h to 1Fh.

Either "p" or "f" can be the W register (a useful special situation).

MOVFP is particularly useful to transfer a data memory location to a peripheral register (such as the transmit buffer or an I/O port). Both "f" and "p" can be indirectly addressed.

MOVLB Move Literal to BSR

Syntax: MOVLB k

Encoding:

1011	1000	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → BSR

Status bits: None

Description: The constant is loaded in Bank Select Register (BSR, 0Fh). Only the low 4 bits of the Bank Select Register are physically implemented.

MOVLW Move Literal to W

Syntax: MOVLW k

Encoding:

1011	0000	kkkk	kkkk

Words: 1

Cycles: 1

Operation: k → W

Status bits: None

Description: The eight bit literal "k" is loaded into W register.

MOVPF Move p to f

Syntax: MOVPF p,f

Encoding:

010p	pppp	ffff	ffff

Words: 1

Cycles: 1

Operation: p → f

Status bits: Z

Description: Move data from data memory location "p" to data memory location "f". Location "f" can be anywhere in the 256 byte data space (00h to FFh) while "p" can be 00h to 1Fh.

Either "p" or "f" can be the W register (an useful special situation)

MOVPF is particularly useful for transferring a peripheral register (e.g. the timer or an I/O port) to a data memory location.

MOVWF Move W to f

Syntax: MOVWF f

Encoding:

0000	0001	ffff	ffff

Words: 1

Cycles: 1

Operation: W → f

Status bits: None

Description: Move data from W register to data memory location "f". Location "f" can be anywhere in the 256 word data space.

NEGW Negate W

Syntax: NEGW f,d

Encoding:

0010	110d	ffff	ffff

Words: 1

Cycles: 1

Operation: $\overline{W} + 1 \rightarrow f$; $\overline{W} + 1 \rightarrow d$

Status bit: OV, C, DC, Z

Description: The contents of the W register are negated using 2's complement. If "d" is 0 the result is placed in W register and data memory location "f". If "d" is 1 the result is placed only in data memory location "f".

NOP No Operation

Syntax: NOP

Encoding:

0000	0000	0000	0000

Words: 1

Cycles: 1

Operation: No operation

Status bits: None

Description: No operation

RETFIE Return from Interrupt

Syntax: RETFIE

Encoding:

0000	0000	0000	0101

Words: 1

Cycles: 2

Operation: TOS → PC, 0 → GLINTD;
PCLATH (f3) is unchanged

Status bits: GLINTD

Description: Return from Interrupt. Stack is popped and Top of the Stack (TOS) is loaded in PC. Interrupts are enabled by clearing GLINTD bit. GLINTD is global interrupt disable bit (bit 4, register CPUSTA). This is a two cycle instruction.

RETLW Return Literal to W

Syntax: RETLW k

Encoding:

1011	0110	kkkk	kkkk

Words: 1

Cycles: 2

Operation: k → W; TOS → PC;
PCLATH (f03) is unchanged

Status bits: None

Description: The W register is loaded with the eight bit literal "k". The program counter is loaded from the top of the stack (the return address). The high address latch (PCLATH) remains unchanged. This is a two cycle instruction.

RETURN Return from Subroutine

Syntax: RETURN

Encoding:

0000	0000	0000	0010

Words: 1

Cycles: 2

Operation: TOS → PC;
PCLATH (f3) is unchanged

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

RLCF Rotate Left f through Carry

Syntax: RLCF f,d

Encoding:

0001	101d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>; f<7> → C; C → d<0>

Status bits: C

Description: The contents of data memory location "f" are rotated one bit to the left through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is stored back in data memory location "f".

RLNCF Rotate Left f (no carry)

Syntax: RLNCF f,d

Encoding:

0010	001d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n+1>; f<7> → d<0>

Status bits: None

Description: The contents of data memory location "f" are rotated one bit to the left. If "d" is 0 the result is placed in the W register . If "d" is 1 the result is stored back in data memory location "f".

RRCF Rotate Right f through Carry

Syntax: RRCF f,d

Encoding:

0001	100d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>; f<0> → C; C → d<7>

Status bits: C

Description: The contents of data memory location "f" are rotated one bit to the right through the Carry Flag. If "d" is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f".

RRNCF Rotate Right f (no carry)

Syntax: RRNCF f,d

Encoding:

0010	000d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<n> → d<n-1>; f<0> → d<7>

Status bits: None

Description: The contents of data memory location "f" are rotated one bit to the right. If "d"is 0 the result is placed in the W register. If "d" is 1 the result is placed in data memory location "f".

SETF Set f and Set d

Syntax: SETF f,d

Encoding:

0010	101d	ffff	ffff

Words: 1

Cycles: 1

Operation: FFh → f, FFh → d

Status bits: None

Description: If "d" is 0 both the data memory location "f" and W register are set to FFh. If "d" is 1 the only the data memory location "f" is set to FFh.

SLEEP

Syntax: SLEEP

Encoding:

0000	0000	0000	0011

Words: 1

Cycles: 1

Operation: 0 → $\overline{PD}$; 1 → $\overline{TO}$
00h → WDT; 0 → WDT prescaler

Status bits: $\overline{TO}$, $\overline{PD}$

Description: The power down status bit ($\overline{PD}$) is cleared. Time-out status bit ($\overline{TO}$) is set. Watchdog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP mode for more details.

SUBLW Subtract W from literal

Syntax: SUBLW k

Encoding:

1011	0010	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (k - W) → W

Status bits: OV, C, DC, Z

Description: The contents of the W register are subtracted from the eight bit literal "k". The result is placed in the W register.

SUBWF Subtract W from f

Syntax: SUBWF f,d

Encoding:

0000	010d	ffff	ffff

Words: 1

Cycles: 1

Operation: (f-W) → d

Status bits: OV,C, DC, Z

Description: Subtract (2's complement method) the W register from data memory location"f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored back in data memory location "f".

SUBWFB Subtract W from f with Borrow

Syntax: SUBWFB f,d

Encoding:	0000	001d	ffff	ffff

Words: 1

Cycles: 1

Operation: (f-W-C) → d

Status bits: OV, C, DC, Z

Description: Subtract (2's complement method) the W register and the carry flag (borrow) from data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

SWAPF Swap f

Syntax: SWAPF f,d

Encoding:	0001	110d	ffff	ffff

Words: 1

Cycles: 1

Operation: f<0:3> → d<4:7>, f<4:7> → d<0:3>

Status bits: None

Description: The upper and lower nibbles of data memory location "f" are exchanged. If "d" is 0 the result is placed in W register. If "d" is 1 the result is place in data memory location "f".

TABLRD Table Read

Syntax: TABLRD t,i,f

Encoding:	1010	10ti	ffff	ffff

Words: 1

Cycles: 2 (3 cycle if f = 02h [PC])

Operation: If t = 1 then TBLATH → f
else if t = 0 TBLATL → f;
Prog Mem (TBLPTR) → TBLAT;
if i = 1 then TBLPTR + 1 → TBLPTR

Status bits: None

Description: First, either the low byte (if t = 0) or the high byte (if t = 1) of the table latch (TBLAT) is moved to register file "f".

Then the contents of the program memory location pointed to by the 16 bit Table Pointer (TBLPTR) is loaded into the 16 bit Table Latch (TBLAT). Finally table pointer is incremented if i = 1.

Example:

```
MOVLW   12h         ;
MOVPF   W, TBLPTRH  ;
MOVLW   34h         ;
MOVPF   W,TBLPTRL   ; TBLPTR = 1234h
TABLRD  0, 1, 50h   ; TBLAT = Prog Mem
                    ; (1234h)
                    ; TBLPTR = 1235h
TLRD    0, 50h      ; low byte → 50h
TABLRD  1,1, 51h    ; high byte → 51h
                    ; TBLAT = Prog Mem
                    ; (1235h)
                    ; TB1.PTR = 1236h
TLRD    0, 52h      ; low byte → 52h
TLRD    1, 53h      ; high byte → 53h
```

TABLWT Table write

Syntax: TABLWT t, i, f

Encoding:	1010	11ti	ffff	ffff

Words: 1

Cycles: 2 (Many if write is to on-chip EPROM program memory)

Operation: if t = 0 then f → TBLATL
else if t = 1 then f → TBLATH;
TBLAT → Prog Mem (TBLPTR);
if i = 1 then TBLPTR + 1 → TBLPTR;

Description: First, contents of file register f is loaded in the low byte (if t = 0) or high byte (if t = 1) of Table Latch, TBLAT.

If TBLPTR points to external program memory location then the contents of TBLAT is written to it and the instruction takes 2 cycles.

If TBLPTR points to an internal EPROM location, then an EPROM write (program) sequence is initiated. It is terminated when an interrupt is received.

If the Global Interrupt Disable bit (GLINTD) is set, the interrupt will complete the TABLWT, but no interrupt sequence will be invoked. If GLINTD = 0, then interrupt will be acknowledged following the TABLWT.

For an interrupt to end programming, its corresponding mask bit must enable the interrupt. If the terminating interrupt is INTIR, RTCIR or RTXIR, the flag bit is automatically cleared. The clearing takes place for both short and long table writes. The user can protect against accidental clearing of an interrupt flag due to a TABLWT instruction by masking off the above mentioned interrupts before doing table write operations.

$\overline{MCLR}/V_{PP}$ pin must be at programming voltage for successful programming. If $\overline{MCLR}/V_{PP} = V_{CC}$ then the programming sequence will be executed, but will not be successful (although the location may be disturbed).

TLRD Table Latch Read

Syntax: TLRD t,f

Encoding:

1010	00tx	ffff	ffff

x= don't care

Words: 1

Cycles: 1

Operation: if (t = 0) thenTBLATL → f else if (t = 1) then TBLATH → f

Status bits: None

Description: Read data from high byte (t = 1) or low byte (t = 0) of 16 bit Table Latch into file register "f". Table Latch is unaffected.

This instruction is used in conjunction with TABLRD to transfer data from program memory to data memory.

TLWT Table Latch Write

Syntax: TLWT t,f

Encoding:

1010	01tx	ffff	ffff

x= don't care

Words: 1

Cycles: 1

Operation: if (t = 0) then f → TBLATL else if (t = 1) then f → TBLATH

Status bits: None

Description: Data from file register f is written into the low byte (t = 0) or thehigh byte(t = 1) of the 16 bit Table Latch.

This instruction is used in conjunction with TABLWT, to transfer data from data memory to program memory.

TSTFSZ Test f, skip if 0

Syntax: TSTFSZ f

Encoding:

0011	0011	ffff	ffff

Words: 1

Cycles: 1 (2)

Operation: skip if f = 0

Status bits: None

Description: If the contents of data memory location "f" are 0 then the next instruction is skipped.

If "f" = 0, the next instruction, fetched during the current instruction execution, is discarded. A NOP is executed instead making this a 2 cycle instruction.

XORLW Exclusive OR literal with W

Syntax: XORLW k

Encoding:

1011	0100	kkkk	kkkk

Words: 1

Cycles: 1

Operation: (W .XOR. k) → W

Status bits: Z

Description: The contents of the W register are XOR'ed with the eight bit literal "k". The result is placed in the W register.

XORWF Exclusive OR W with f

Syntax: XORWF f,d

Encoding:

0000	110d	ffff	ffff

Words: 1

Cycles: 1

Operation: (W .XOR. f) → d

Status bits: Z

Description: Exclusive OR the contents of the W register with data memory location "f". If "d" is 0 the result is stored in the W register. If "d" is 1 the result is stored in data memory location "f".

3.0 HARDWARE DESCRIPTION OF THE CPU

3.1 INDIRECT ADDRESSING REGISTERS (FILES 00h & 08h)

These two register locations (not physically implemented) are used to implement indirect addressing of data memory space. An instruction using file address of 0 or 8 actually accesses the data memory location pointed to by the corresponding FSR register (file 1 or file 9). If file 00h (or file 08h) itself is read indirectly via an FSR, all zeroes are read. Similarly, if file 00h (or file 08h) is written to indirectly, the operation will be equivalent to a NOP.

Single cycle data transfers within the entire data space are possible with MOVFP and MOVPF instructions, when "p" is specified as "00h" and "f" as "08h", or vice versa.

3.2 FILE SELECT REGISTERS (FSR0 AND FSR1, FILES 01h AND 09h)

These two registers are 8 bit wide indirect address pointers for data memory. They can be auto-incremented, auto-decremented or left unchanged after each access as determined by the 4 control bits in the status register "ALUSTA" (File 04h bits 7:4). See figure 3.8.1.

3.3 TABLE POINTER (TBLPTRL FILES AND TBLPTRH, FILES ODh AND OEh)

File registers 0Dh and 0Eh form a 16 bit pointer to address the 64K program memory space. The table pointer is used by instructions TABLWT and TABLRD.

The TABLRD and the TABLWT instructions allow transfer of data between program and data space. The table pointer serves as the 16 bit address of the data word within the program memory.

3.4 TABLE LATCH (TBLATH, TBLATL)

The table latch (TBLAT) is a 16 bit register, consisting of TBLATH and TBLATL refer to the high and low bytes of the register. It is not mapped into data or program memory. The table latch is used as a temporary holding latch during data transfer between program and data memory (see descriptions of instructions TABLRD, TABLWR, TLRD and TLWR).

3.5 PROGRAM COUNTER MODULE

The program counter (PC) is a 16 bit register. PCL, the low byte of the PC, is mapped in the data memory (file 02h). PCL is readable and writable just as any other register. PCH is the high byte of the PC and is not directly addressable since PCH is not mapped in data or program memory. An 8 bit register PCLATH (PC high latch) is used as a holding latch for the high byte of the PC. PCLATH is mapped into data memory (file 03h). The user can read or write PCH through PCLATH.

The 16 bit wide PC is incremented after each instruction fetch during Q1 unless modified by GOTO, CALL, LCALL, RETURN, RETLW, or RETFIE instruction or interrupt response or due to destination write to PCL by an instruction. "Skip"s are equivalent to incrementing the PC twice.

The operations of the PC and PCLATH for different instructions are as follows:

a) LCALL:

PCLATH → PCH , IR<7:0> → PCL (PCL is loaded with 8 bit destinaton address embedded in the instruction. PCLATH is unchanged.

b) CALL, GOTO:

A 13 bit destination address is provided in the instruction
IR<12:0> → PC <12:0>
PC<15:13> → PCLATH<7:5>

c) Read f03 (Any instruction that reads PCL):

PCL → data bus → ALU or destination
PCH → PCLATH

d) Write f03 (Any instruction that writes to PCL):

8 bit data → data bus → PCL
PCLATH → PCH

e) Read-Modify-Write (Any instruction that does a read-write-modify operation on f02, such as ADDWF f02)

Read: PCL → data bus → ALU
Write: 8 bit result → data bus → PCL
PCLATH → PCH

Note that read-modify-write only affects the PCL with the result. PCH is loaded with PCLATH. Thus, ADDWF f02, for example will result in a jump within the current page. If PC = 03F0h, W = 30h and PCLATH = 03h before instruction, PC = 0320h after the instruction. To accomplish a true 16 bit computed jump, the user needs to compute the 16 bit destination address, write the high byte to PCLATH and then write the low value to PCL.

The following PC related operations do not change f03h:

a) LCALL, RETLW, RETURN, RETFIE instructions,
b) Interrupt vector is forced onto the PC,
c) Read-modify-write instructions (e.g. BSF 02) on f02h.

3.6 STACK

The PIC17C42 has a 16 word x 16 bit hardware stack which is not part of data or program space. The PC is pushed onto the stack if CALL or LCALL instructions are executed or if an interrupt is responded to by branching to the corresponding interrupt vector. The stack is POPed

into the PC if a RETURN, RETLW or RETFIE instruction is executed. The top of the stack is not addressable in any other way.

3.6.1 Stack Available Status Bit (Bit 5, CPUSTA)

STKAVL is a read only status bit that indicates any stack overflow error. STKAVL is set to '1' on reset and stays '1' unless the following situation occurs:

If stack is full: i.e. there are 16 entries in the stack the STKAVL is set to '0'. If, the stack is popped (by RETURN, RETLW or RETFIE instruction) then STKAVL is set to '1' again indicating 'stack availability'.

If, however, a push takes place instead (due to CALL, LCALL or interrupt), then stack overflow occurs. In this event the first entry is lost and STKAVL is permanently cleared to '0'. Under this condition, the only way STKAVL will set to '1' is via reset.

STKAVL usage caution: If the stack is empty, a POP (due to RETURN, RETLW or RETFIE)followed by a PUSH, will permanently clear STKAVL to '0 '.

For a description of CPUSTA register, see figure 4.5.1.

3.6.2 Using the STKAVL bit

One way to use the STKAVL bit is to test it at the beginning of every subroutine or interrupt service routine. If STKAVL = 0, then all stack locations are used (and presumably no error has occurred yet). In such case, interrupts must be disabled in the subroutine. Also, no subroutine calls must be made unless software stack management is invoked.

3.7 INTERRUPT LOGIC

The PIC17C42 has 11 interrupt sources that are mapped into 4 interrupt vectors. The interrupt logic is controlled by the INTSTA register and the global interrupt disable bit (GLINTD) in CPUSTA register, file f06h. See figure 4.5.1 for a description of CPUSTA register. Four hardwired vectors allow fast interrupt response time. Worst case latency is 3 instruction cycles when only one interrupt at a time is being serviced. Interrupt nesting to multiple levels is possible by enabling interrupts within the service routine. When an interrupt occurs, the current PC value is pushed onto the stack and the vector corresponding to the interrupt source is loaded into the PC.

3.7.1 Interrupt Flag and Mask Bits

Each interrupt has a request flag bit and a mask bit associated with it. The registers that hold these bits are INTSTA (file 07h), PIR (Bank 1, file 16h) and PIE (Bank 1, file 17h). See table 3.7.1 for details.

Interrupt flag bits INTIR, RTCIR or RTXIR are cleared automatically in hardware. PEIR is not cleared automatically since it is not a latched bit. PEIR is simply the OR of all the individual peripheral interrupt flag bits such as IRB, TM3IR, etc. Therefore if PEIR is the source of the interrupt, the user must clear, in software, the actual peripheral interrupt flag bit. The global interrupt disable bit, GLINTD, is set, in any case, preventing any further interrupt. To enable interrupts from the service routine the user must clear GLINTD. The user, must first clear the current interrupt flag bit to prevent recursive vectoring to the same service routine.

The TABLWT instruction, in a long write situation (i.e. writing to on-chip EPROM location) must be terminated with an interrupt. On completion, TABLWT clears the interrupt flag in the same exact fashion as an interrupt response, i.e. INTIR, RTCIR or RTXIR flag will be cleared if responsible for ending the TABLWT.

3.7.2 Peripheral interrupts

All peripherals use the same interrupt vector, 0020h. The individual peripheral interrupt request bits are "ORed" together. When multiple peripheral interrupt sources are enabled, the priorities have to be determined by software. Each peripheral has its own interrupt enable and request bit(s). In addition, the PEIE (Peripheral Interrupt Enable) bit acts as a global enable bit for all peripheral interrupts. There is a common peripheral interrupt request status bit (PEIR, bit 7, register INTSTA)which is a logical OR of all the individual peripheral interrupt request flags. This is a read only status bit useful for quickly determining if any peripheral request is outstanding.

3.7.1 TABLE OF INTERRUPTS

Interrupt flag	Flag location bit, Register	Interrupt mask bit	Mask bit location bit , Register	Interrupt Source	Priority	Vectors to
INTIR	bit 4,INTSTA	INTIE	bit 0, INTSTA	External interrupt on INT pin	Highest priority	0008h
RTCIR	bit 5,INTSTA	RTCIE	bit 1, INTSTA	RTCC overflow interrupt	2nd priority	0010h
RTXIR	bit 6, INTSTA	RTXIE	bit 2, INTSTA	External interrupt on RT pin	3rd priority	0018h
PEIR	bit 7, INTSTA	PEIE	bit 3, INTSTA	Any peripheral interrupt	Lowest priority	0020h
IRB	bit 7, PIR	IEB	bit 7, PIE	Port B input change interrupt	lowest priority	0020h
TM3IR	bit 6, PIR	TM3IE	bit 6, PIE	Timer/Counter3 interrupt	(All these	
TM2IR	bit 5, PIR	TM2IE	bit 5, PIE	Timer/Counter2 interrupt	peripheral	
TM1IR	bit 4, PIR	TM1IE	bit 4, PIE	Timer/Counter1 interrupt	interrupts are	
CA2IR	bit 3, PIR	CA2IE	bit 3, PIE	Capture1 interrupt	OR'ed together	
CA1IR	bit 2, PIR	CA1IE	bit 2, PIE	Capture2 interrupt	to generate	
TBMT	bit 1, PIR	TXIE	bit 1, PIE	Serial port transmit interrupt	PEIR)	
RBFL	bit 0, PIR	RCIE	bit 0, PIE	Serial port receive interrupt		

FIGURE 3.7.1.1: REGISTER INTSTA

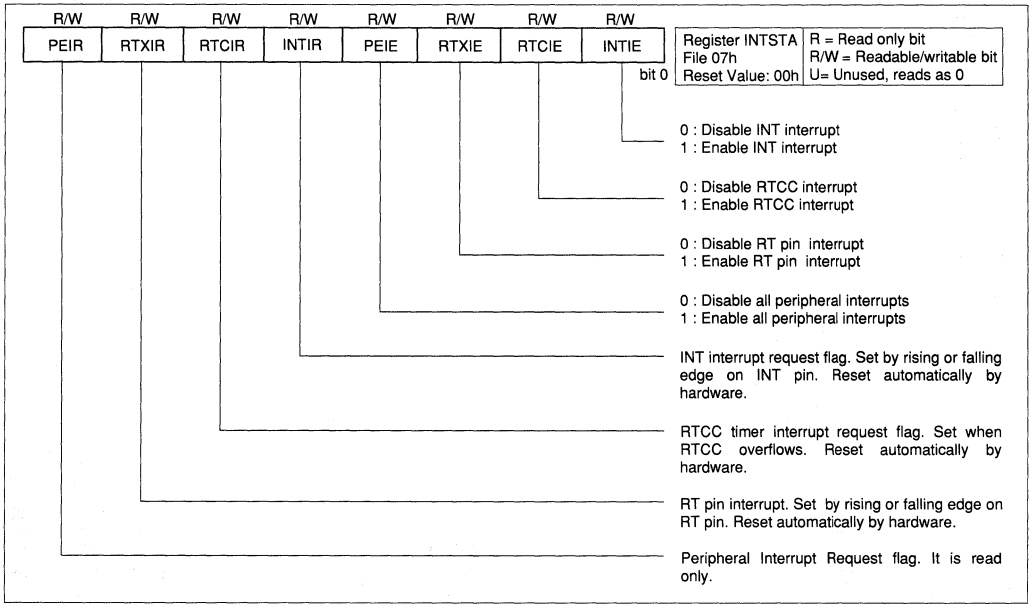


FIGURE 3.7.1.2: PIR (PERIPHERAL INTERRUPT REQUEST) REGISTER

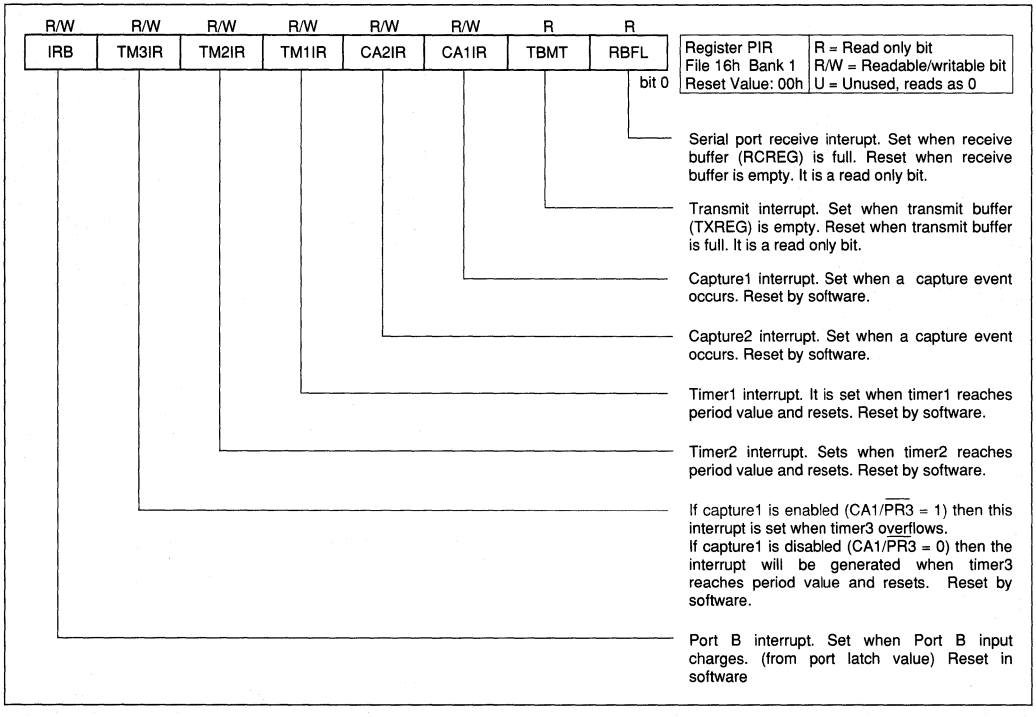
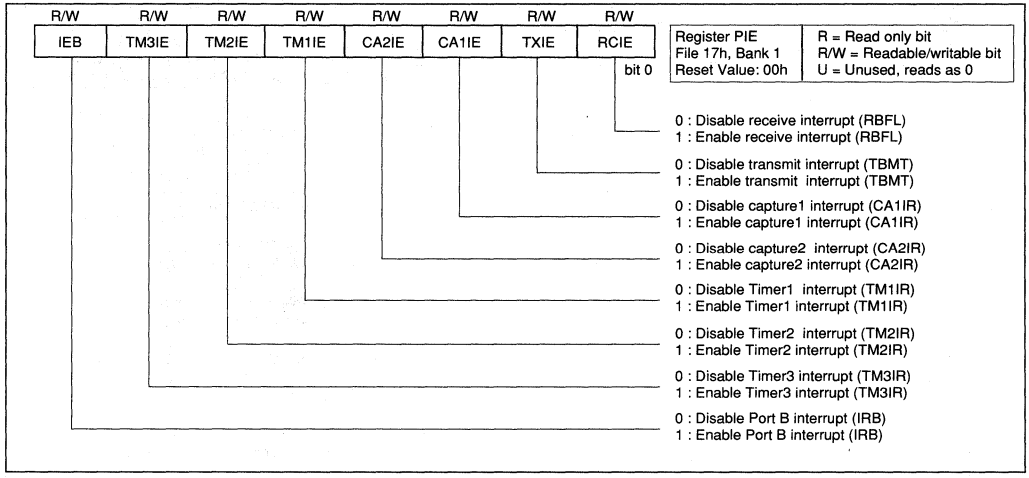


FIGURE 3.7.1.3: PIE (PERIPHERAL INTERRUPT ENABLE) REGISTER



3.7.3 INT and RT External Interrupts

INT and RT external interrupts can be positive or negative edge triggered, selectable in software. INT interrupt is generated on falling edge if INTEDG = 0 or on rising edge if INTEDG = '1'. Similarly, setting bit RTEDG = '0' will generate RT pin interrupt on falling edge whereas RTEDG = '1' will trigger RT interrupt on rising edge. The timing requirements on INT and RT inputs are as follows:

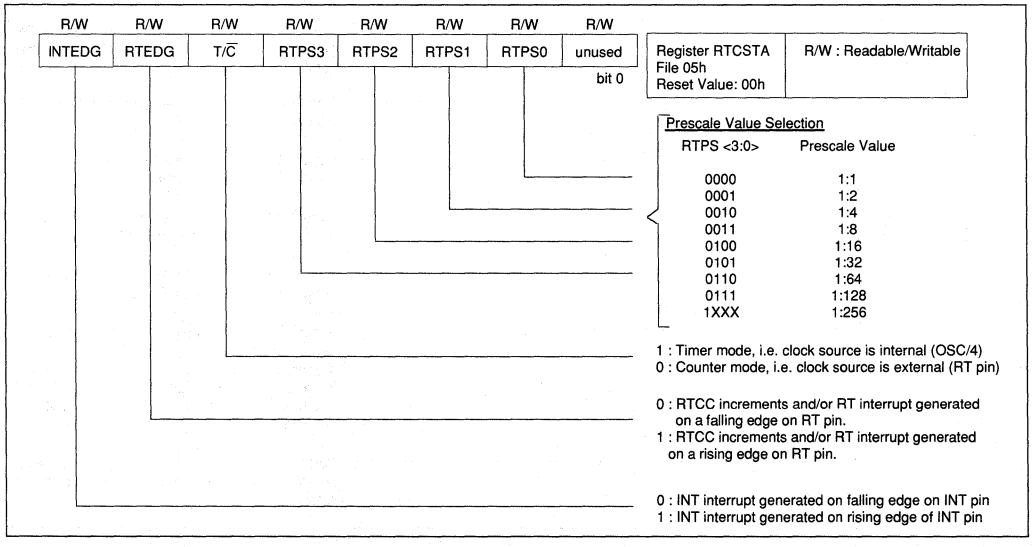
t_{INTH} = t_{RTIH} = INT or RT high time ≥ 25ns

t_{INTL} = t_{RTIL} = INT or RT low time ≥ 25ns

Please note that changing edge selection for INT or RT pin may generate a false interrupt. The user should clear the INTIR or the RTXIR bit after changing edge setting.

See RTCSTA (register file 05h) for bit allocation.

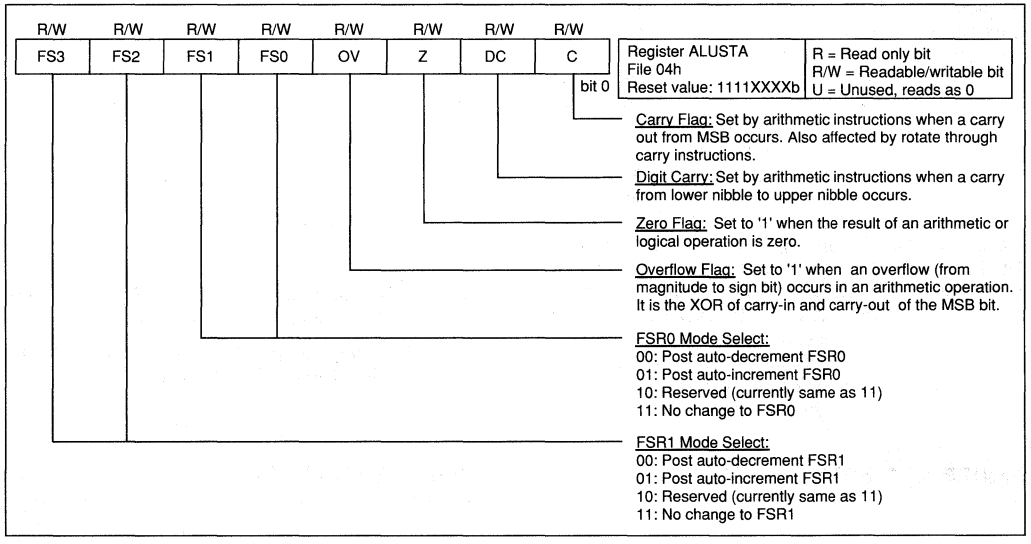
FIGURE 3.7.3.1: RTCSTA: RTCC STATUS/CONTROL REGISTER



3.8 ALU

The Arithmetic and Logic Unit of the PIC17C42 is capable of carrying out arithmetic or logical operations on two operands or a single operand. All single operand instructions operate either on the W register or a file register. For two operand instructions, one of the operands is the W register and the other one is either a file register or an 8 bit immediate constant.

FIGURE 3.8.1: ALUSTA (ALU STATUS) REGISTER



4.0 SPECIAL FEATURES OF THE CPU

What sets apart a microcontroller from other processors the most are special circuits to deal with the needs of real time applications. The PIC17C42 has a host of such features intended to maximize system reliability, minimize cost through elimination of costly external components, provide power saving operating modes and offer code protection.

The PIC17C42 has a watchdog timer which can be shut off only through EPROM fuses. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the oscillator start-up timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the power-up timer (PWRT), which provides a fixed delay of 80 ms nominal on power up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on chip, most applications need no external reset circuitry. The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset, watchdog timer time-out or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LF (low frequency) crystal/resonator option saves power. A set of EPROM configuration bits (fuses) are used to select various options. Additional EPROM fuses are included for code-security.

4.1 RESET

The reset logic resets the complete PIC17C42 circuitry as follows:

- Oscillator buffer is enabled (i.e. oscillator is restarted if waking up from SLEEP through reset).
- Program Counter is reset to 0000h.
- All registers are reset as described in Table 1.6.2.
- Watchdog timer & its prescaler are cleared.
- Internal phase clock generator is held in Q1 state. If external execution is selected, ALE output is held low while $\overline{OE}$ and $\overline{WR}$ outputs are driven high.
- I/O ports B, C, D and E are configured as inputs. In case of port B, the weak pull-ups are activated. Ports RA2 and RA3 revert to high impedance state.

There are three events which can cause a device reset.

a) Power On Reset :VDD rise is detected (1.2V - 2.0V range)

b) External reset: "Low" level on the $\overline{MCLR}$ input

c) WDT reset: Watchdog timer Time out

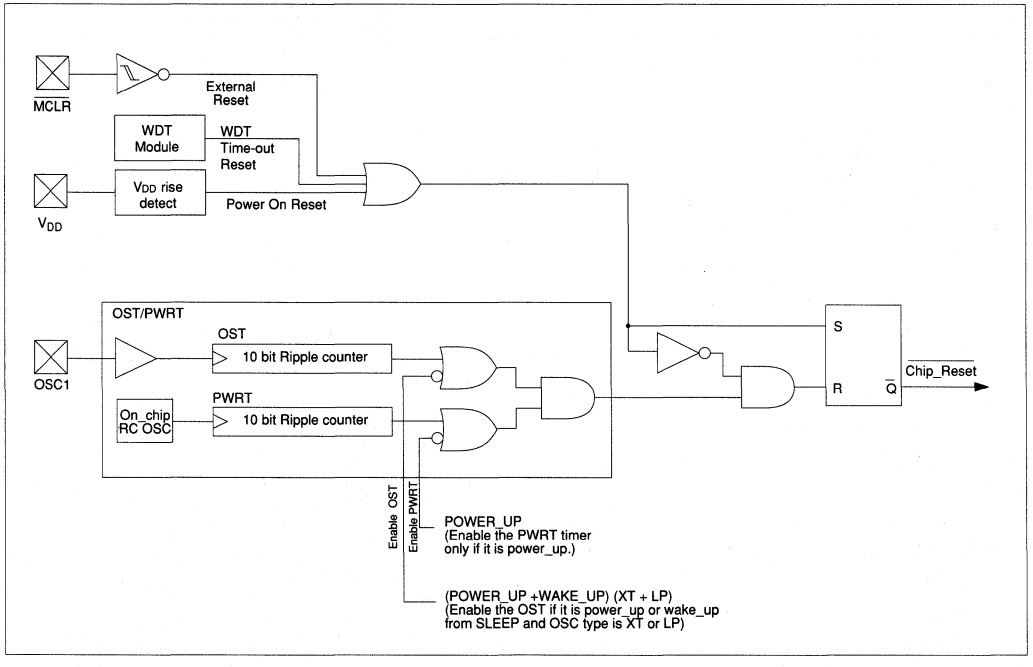
The RESET condition is maintained as long as

a) the $\overline{MCLR}$ input is "low"

b) $\overline{MCLR}$ has gone high but the Power-up timer (PWRT) is active, (i.e. has not timed out)

c) $\overline{MCLR}$ has gone high but the oscillator start-up timer (OST) is active (i.e. has not timed out)

FIGURE 4.1.1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



4.2. OSCILLATOR

The PIC17C42 can accept an external clock input on OSC1 pin or will run off external crystal or ceramic resonator connected between OSC1 and OSC2 pins. It also has an RC oscillator mode in which an external R and C combination can be connected to OSC1 pin. The choice is made by EPROM fuses FOSC1 and FOSC0. These fuses are mapped in program memory locations FE01h and FE00h respectively. Refer to section 4.8 for details on the fuses.

TABLE 4.2.1: OSCILLATOR OPTIONS

Fosc1, Fosc0 Fuses	Mode	OSC1 Pin Function	OSC2 Pin Function	Freq. Range
11	EC: External Clock input	External clock input	CLKOUT output	DC-16Mhz
01	RC: RC oscillator mode	External RC oscillator connection	CLKOUT output	DC-4Mhz
10	XT: Crystal oscillator mode	Crystal connection	Crystal connection	0.2-16Mhz
00	LF: Low frequency crystal oscillator mode	Crystal connection	Crystal connection	32-200Khz

Note: 0 implies a programmed fuse.

4.2.1 EC: External Clock Input Mode:

The OSC1 input can be driven by CMOS drivers (figure 4.2.1A). In this mode, the OSC1 pin is a high impedance CMOS input. The OSC2 pin outputs CLKOUT (frequency = fosc/4). See Figure 1.2.1 for timing of CLKOUT.

4.2.2 RC: RC Oscillator Mode:

An external R and C combination can be connected to OSC1 pin (figure 4.2.1B). The RC oscillator mode provides a very cost effective solution. However, the frequency of oscillation will vary with Vcc, temperature and from chip to chip due to process variation. It is, therefore, not the right choice for timing sensitive applications where accurate oscillator frequency is desired. The OSC2 pin, in this mode, outputs CLKOUT (freq. = fosc/4). See Figure 1.2.1 for timing of CLKOUT.

4.2.3 XT: Crystal Oscillator Mode:

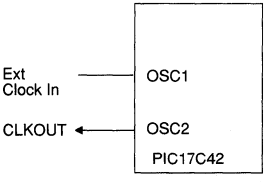
In this mode a crystal or a ceramic resonator can be connected across OSC1 and OSC2. (figure 4.2.1C). The crystal must be of fundamental mode. If an overtone mode crystal is used (which is common above 20 MHz) then a tank circuit must be used to attenuate the gain at fundamental frequency (figure 4.2.1D)

4.2.4 LF: Low Frequency Crystal Oscillator Mode:

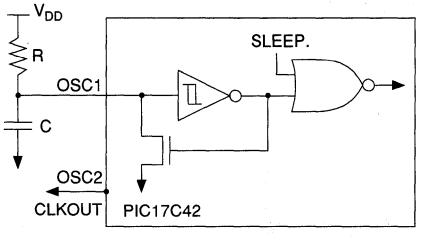
This is same as the XT mode, (figure 4.2.1E) except that it is suitable for crystals of frequency range 32 KHz to 200 KHz.

FIGURE 4.2.1: DIFFERENT OSCILLATOR/ CLOCKIN OPTIONS

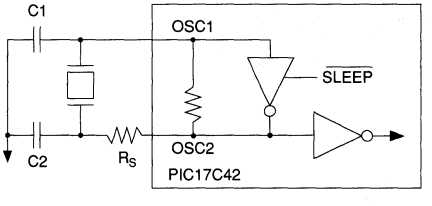
4.2.1A EXTERNAL CLOCK



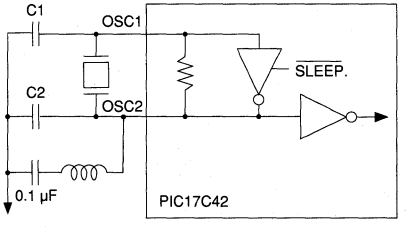
4.2.1B RC OSCILLATOR MODE



4.2.1C XT CRYSTAL OSCILLATOR MODE



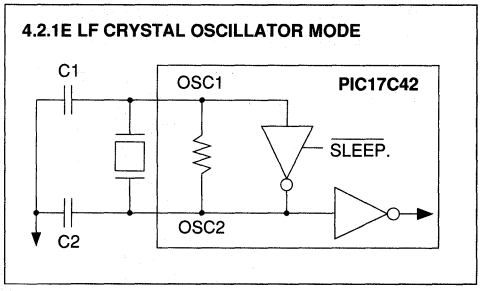
4.2.1D XT CRYSTAL OSCILLATOR MODE (OVERTONE CRYSTALS)



To Filter the fundamental frequency

$$\frac{1}{LC2} = (2\pi f)^2$$

Where f= tank circuit resonant frequency.This should be midway between the fundamental and the 3rd overtone frequencies of the crystal.



4.3 OSCILLATOR START-UP TIMER (OST)

The OST provides a 1024 oscillator period delay on power-up and on wake up from SLEEP. This delay is provided by a 10 bit ripple counter. On power-up, the delay begins from the rising edge of MCLR. On wake-up from SLEEP the time-out is counted from the time the wake-up event occurs. Since the OST counts oscillator signal on OSC1 pin, the counter only starts counting when amplitude on OSC1 pin reaches a certain acceptable limit. The OST time-out allows the crystal oscillator (or resonator) to stabilize before the chip is taken out of reset. The circuit will function with crystals of any frequency. This time-out is not invoked in RC oscillator mode or external clock (EC) mode.

4.4 POWER-UP TIMER (PWRT) AND POWER-ON RESET (POR)

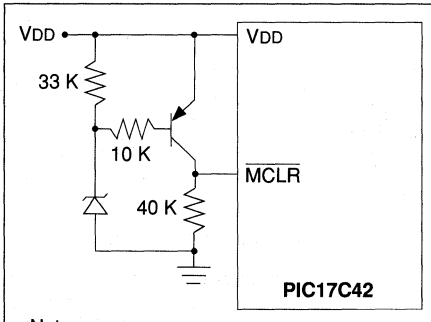
The function of the PWRT timer is to provide a fixed 80 ms (typical) delay only on power-up. This is provided by a 10 bit ripple counter whose input clock comes from an on chip RC oscillator. The time-out is counted from the rising edge of MCLR. The purpose of this time-out is to allow the VDD supply to reach acceptable level before the part is taken out of reset.

An internal Power-on Reset pulse (POR) is generated when a VDD rise is detected during initial power-up of the chip. (when VDD = 1.2V to 2.0V nominally). The POR signal resets internal registers as described in table 1.6.2. The user should note that the on-chip circuitry does not generate an internal reset when VDD goes down, i.e., it does not provide brown out protection. Figure 4.4.1 and 4.4.2 shows possible external brown-out protection circuits. Also VDD must come up from VSS (nominal) for a POR signal to be generated. The PWRT timer and OST timer guarantee proper power-on reset without external components. This is done by simply tying the MCLR pin to VDD (figure 4.4.4). As VDD comes up, POR is generated and MCLR is sensed as '1' inside the chip, both OST and PWRT timers begin time-out. The 80 ms (nominal) delay of the PWRT allows VDD to rise above VDD min. spec. If the rise time of VDD is much slower such that at the end of the time-out VDD has not reached an acceptable level (as in figure 4.4.6) then external RC delay must be added on MCLR pin.

The following table shows the time-outs for different oscillator types.

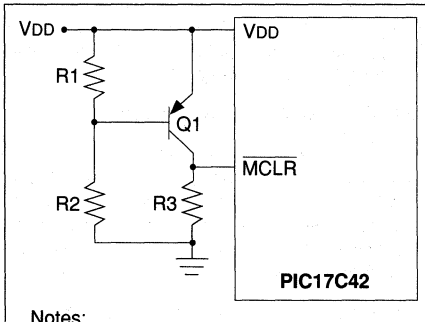
Oscillator Type	Power-up	Wake-up from SLEEP
EC	80 ms	—
RC	80 ms	—
XT	Greater of 80 ms and 1024 tosc	1024 tosc
LP	Greater of 80 ms and 1024 tosc	1024 tosc

FIGURE 4.4.1: BROWN OUT PROTECTION CIRCUIT



Notes:
1. This circuit will activate reset when VDD goes below (VZ + 0.7 V) where VZ = Zener voltage.

FIGURE 4.4.2: BROWN OUT PROTECTION CIRCUIT



Notes:
1. This brown circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7\ V$$

FIGURE 4.4.3: EXTERNAL RESET PULSE

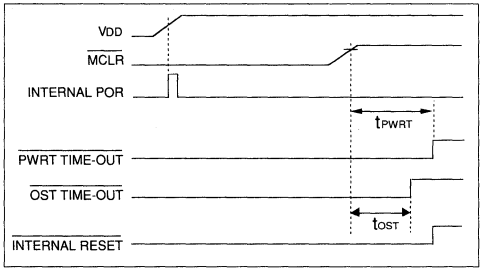


FIGURE 4.4.4: USING ON-CHIP POR

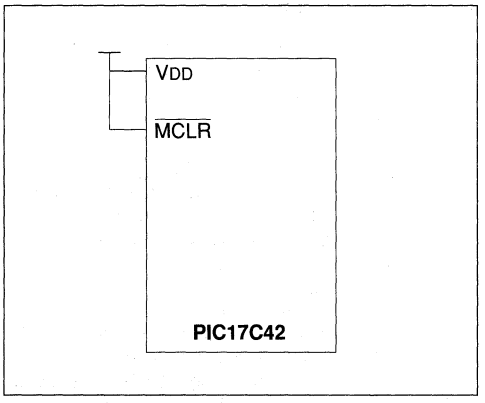
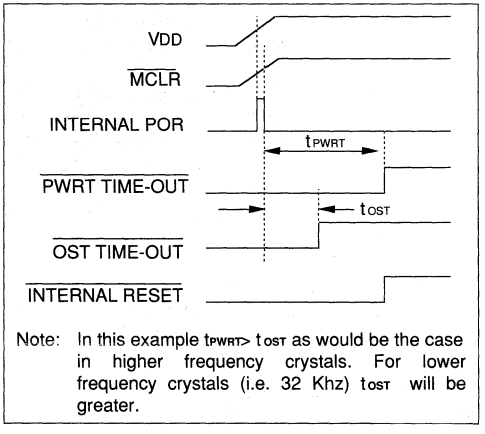
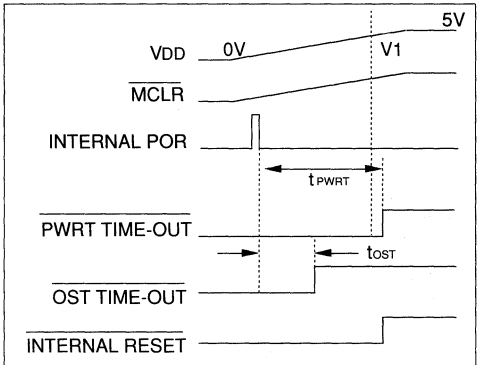


FIGURE 4.4.5: INTERNAL RESET (VDD AND MCLR TIED TOGETHER)



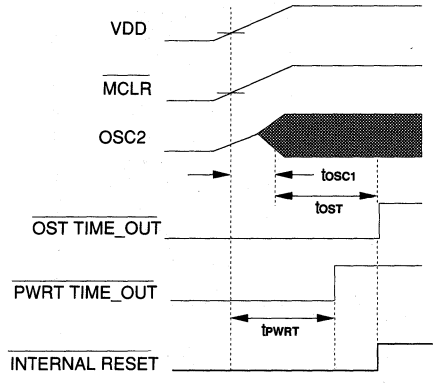
Note: In this example $t_{PWRT} > t_{OST}$ as would be the case in higher frequency crystals. For lower frequency crystals (i.e. 32 Khz) t_{OST} will be greater.

FIGURE 4.4.6: INTERNAL RESET (VDD AND MCLR TIED TOGETHER): SLOW VDD RISE TIME



Note: In this example $t_{PWRT} > t_{OST}$ as would be the case in higher frequency crystals. For lower frequency crystals (i.e. 32 Khz) t_{OST} will be greater.

FIGURE 4.4.7: OST START UP TIMING DETAILS



This figure shows in greater detail the timings involved with the oscillator start-up timer. In this example the low frequency crystal start-up time is larger than power-up time (t_{PWRT}).

t_{OSC1} = time for the crystal oscillator to reach oscillation level detectable by the oscillator start-up timer (OST)

t_{OST} = 1024 t osc

4.5 SLEEP MODE

The full static design of the PIC17C42 makes it possible to put the part in a power saving SLEEP (or power down) mode in which all on chip clocks are stopped.

The SLEEP mode, entered by executing a SLEEP instruction, shuts down the oscillator, sets $\overline{TO}$ (bit3, CPUSTA), clears $\overline{PD}$ (bit2, CPUSTA), the watchdog timer and its prescaler. In XT or LP mode, both OSC1 and OSC2 are placed into high-impedance state. In EC and RC modes, OSC1 pin is placed in high-impedance state while OSC2 is driven low. No clocks are presented to the internal logic even when an external clock is present on the OSC1 pin. The chip will remain in a completely static condition with the following exceptions:

a) If the watchdog timer is enabled, it will keep running and will consequently wake up the chip on time-out.
b) Signal edges on the RT pin (rising or falling whichever is defined to be the active edge by the RTEDG control bit) will increment the RTCC prescaler (an asynchronous ripple counter) if an external clock source is selected for RTCC. The RTCC itself will not increment.
c) Any external interrupt event, such as RT, INT, capture1 or capture2 interrupt will wake the processor provided the corresponding interrupt mask bit was enabled when entering SLEEP mode. If global interrupt disable is off (GLINTD=0) then the chip will jump to corresponding interrupt vector on wake-up. Otherwise the chip will wake up and resume executing without responding to the interrupt (i.e. will not branch to interrupt vector).
d) Any peripheral operating independent of the internal processor clock can change its status due to external events. Specifically, the serial port receive shift register will shift in data in synchronous slave (external clock) mode.

Besides the on-chip oscillator, any circuitry that consumes current is turned off in SLEEP mode. This includes the entire EPROM and, in particular, the EPROM fuses. The only fuses that will remain active are the WDT fuses (FWDT0, FWDT1). If minimal SLEEP current is desired, the user should consider turning off the watchdog timer. Since fuses consume current in '1' state. Turning WDT off not only saves the operating current it requires, but also saves fuse current due to FWDT1 or FWDT0 fuses. All I/O pins maintain their status during SLEEP.

4.5.1 Wake-up from SLEEP

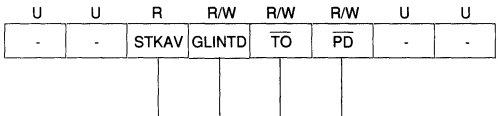
Once the chip has entered the SLEEP mode it can only be awakened by one of the following events:

a) Bringing V_{DD} down to zero and back up to operational level will induce a power on reset and wake up the chip.
b) Applying a "low" level on $\overline{MCLR}$ pin
c) A watchdog timer time-out (WDT must be enabled). "TO" status bit will be cleared in this case.
d) The following interrupts can wake up the processor from SLEEP:
   1. External interrupt on RT pin
   2. External interrupt on INT pin
   3. Capture1 interrupt, due to a capture event on the RB0/CAP1 pin. The prescaler on the capture input will operate during SLEEP. The actual capture of the timer value will occur when execution resumes after wake-up (which is therefore, not meaningful).
   4. Capture2 interrupt.
   5. Input change on Port B interrupt
   6. Synchronous slave mode transmission interrupt: If synchronous transmission is in progress (using external clock) at the time the processor is put to SLEEP, a TBMT interrupt will be generated at the end of the transmission and wake the chip up.
   7. Synchronous slave mode reception interrupt: If synchronous reception is enabled (CREN = 1) before the chip goes into SLEEP, then RBFL interrupt will be set at the end of a reception (if a receive word came during SLEEP) which will wake the chip up.

If GLINTD = 0, the normal interrupt response takes place. If GLINTD = 1, the chip will resume execution starting with the instruction following the SLEEP instruction. It will not vector to interrupt service routine.

If selected oscillator type is XT or LP then the oscillator start-up timer (OST) is activated on wake-up. This will mean that the timer will keep the part in reset for 1024 tosc. The user needs to take this into account when considering interrupt response time coming out of SLEEP.

FIGURE 4.5.1: CPUSTA REGISTER



Register: CPUSTA	R = Read only
File 06h	R/W = Readable/Writable bit
Power-on-Reset Value: 00111100b	U = Unimplemented, reads as '0'

Power-down status bit.
$\overline{PD}$ = 0 indicates that the chip was in power-down (SLEEP mode).
$\overline{PD}$ is set to '1' on power-on reset.
It is cleared when a SLEEP instruction is executed.
It is unaffected otherwise. The user should look at this coming out of reset to determine how the reset was caused (Table 4.5.1.1).

Time-out status bit.
$\overline{TO}$ = 0 indicates WDT time-out. $\overline{TO}$ is set on power-on reset.
It is cleared when WDT times out. It is unaffected otherwise.
The user should look at this coming out of reset to determine how the reset was caused (Table 4.5.1.1).

Global Interrupt Disable bit.
GLINTD = 0: Enables all interrupts. For an interrupt to be enabled, its individual enable bit must also be a '1'.

GLINTD = 1: Disables all interrupts.

Stack available bit.
STKAVL = 2 indicates stack is available.
STAKVL = 0 indicates stack is full or a stack-error may have occured.
See section 3.6.1 for a detailed description.

TABLE 4.5.1.1: WAKE -UP AND RESET FUNCTION TABLE

Event	Chip Status before event	Chip function after event					Notes
		PC	Oscillator Circuit	OST	$\overline{TO}$	$\overline{PD}$	
Power on reset	Don't care	0000	on	yes	1	1	
$\overline{MCLR}$ reset	Normal operation	0000	on	no	u	u	
$\overline{SLEEP}$ instruction	Normal operation	N+1	off	no	1	0	
$\overline{MCLR}$ wake-up	SLEEP	0000	on	yes(2)	u	u	
WDT time-out	Normal operation	0000	on	no	0	u	
WDT wake-up	SLEEP	0000	on	yes(2)	0	u	
Interrupt	Normal operation	Vector	on	no	u	u	
Interrupt wake-up	SLEEP,GLINTD=0	1. N+1 2.Vector	on	yes(2)	u	u	1
Interrupt wake-up	SLEEP,GLINTD=1	1. N+1 2. N+2	on	yes(2)	u	u	1

Legend

PC Program Counter contents after the event
$\overline{TO}$ Time Out status bit after the event
$\overline{PD}$ Power Down status bit after the event
N Address of SLEEP instruction
U No change takes place

Notes

Note 1: The instruction at "N+1" executed, after wake up. Step 2 depends on the status of the GLINTD bit at the time of the event. If GLINTD was "0", the program will vector to the interrupt routine.

Note 2: OST timer is activated only in XT and LP oscillator modes. (Sec. 4.4)

4.5.2 Interrupt/SLEEP Interaction

If an interrupt occurs during the very cycle a SLEEP instruction is fetched, it will be recognized in the following cycle (which is the execution cycle of the SLEEP instruction) preventing the processor from going into SLEEP. The SLEEP instruction will effectively execute as a single cycle NOP. The $\overline{PD}$ bit will not be cleared.

4.5.3 Minimizing Current Consumption in SLEEP Mode

The SLEEP mode is designed to reduce power consumption. To minimize current drawn during SLEEP mode, the user should turn-off output drivers that are sourcing or sinking current, if it is practical. Weak pull-ups on port-pins should be turned off, if possible. All inputs should be either at V_{SS} or at V_{DD} (or as close to rail as possible). An intermediate voltage on an input pin causes the input buffer to draw a significant amount of current.

4.6 WATCHDOG TIMER

The PIC17C42 has an on chip watchdog timer whose function is to recover from software malfunction. The watchdog timer is an 8 bit asynchronous ripple counter with an 8 bit prescaler (also an asynchronous ripple counter). The watchdog timer always runs off its own internal RC oscillator. The watchdog timer is not readable or writable. It is not mapped in data or program memory space. Two EPROM fuses provide four operating options for the watchdog timer:

FWDT1, FWDT0	WDT Clock Input Source	WDT Function Input Clock	WDT Period
1 0	RC osc	WDT runs with prescale = 256	4.6 sec
0 1	RC osc	WDT runs with prescale = 64	1.15 sec
1 1	RC osc	WDT runs with prescale = 1	18 ms
0 0	OSC/4	WDT runs as a regular timer with prescale = 256	65536 Tcy

Note: 0 implies a programmed fuse.

Fuses FWDT1 abd FWDT0 are mapped in program memory locations FE03h and FE02h respectively. See section 4.8 for details on how to program fuses.

The watchdog timer and its prescaler are reset and the time-out bit, TO (bit3, CPUSTA) set to '1' if:

a. A CLRWDT instruction is executed.
b. A SLEEP instruction is executed.
c. A power on reset occurs.

Under normal circumstances, the user program is expected to clear the watchdog timer on a regular interval. If the program fails to do so, the WDT will overflow and reset the chip. The watchdog timer and its prescaler are physically the same as the power-up timer (PWRT). They simply perform different roles in and outside reset condition.

4.6.1 WDT as a Regular Timer

Setting fuses FWDT1 and FWDT0 as 0's will configure the WDT as a simple timer. In this mode the timer increments on internal OSC/4 clock with a prescale of 256 (i.e. increments at OSC freq/1024 rate). On overflow TO bit is cleared, but the chip is not reset. In this mode the WDT is stopped during SLEEP. The TO bit is set when a CLRWDT instruction is executed.

4.7 CODE PROTECTION AND WRITE PROTECTION

The code in the user EPROM may be protected from piracy by selecting "code protected Microcontroller mode." This is done by blowing fuses FPMM1 and FPMM0 to "0". A TABLRD instruction, executed from the test EPROM attempting to read user EPROM will read encrypted data. However, if the instruction is executed from an address less than 2K (i.e. from user EPROM), it will read un-encrypted data.

Further, any TABLWT instruction executed from the test EPROM and attempting to write to the user EPROM, will not result in programming of the destination. However, the instruction will still need to be terminated by an interrupt condition and the table latches will still be written. A TABLWT instruction, executed from an address less than 2K can program any user EPROM location regardless of code protection.

The above measures essentially prevent read, verify or programming of any user EPROM location from outside.

4.8 CONFIGURATION FUSES

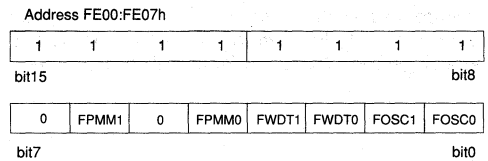
Configuration fuses are EPROM bits that can be programmed (reads '0') or left unprogrammed (reads '1') to select between options (e.g. operating modes). For simplicity of programming they are mapped into program memory. This also makes it possible to read the fuse values (only in microcontroller modes). Each fuse is assigned one program memory location. In erased condition a fuse will read as a '1'. To program (or "blow") a fuse, the user needs to write to the fuse address using a TABLWT instruction. Regardless of the data, a TABLWT to a fuse location will bow the fuse. The fuses and their addresses are shown in table 4.8.1.

Reading configuration fuses: Reading any fuse location in the address range FE00:FE07h will read all eight fuse values in the lower byte and all 1's in the upper byte. Fuse located at FE00h will show up in bit 0 and so on. The fuse locations are accessible only in microcontroller and secure microcontroller modes. In microprocessor and extended microcontroller modes, this section of the program memory is mapped external (see figure 1.5.2) making the fuse locations inaccessible.

TABLE 4.8.1: CONFIGURATION FUSES

Fuse	Address	Function
FOSC0	FE00h	FOSC1, FOSC0 :
FOSC1	FE01h	00 : LP oscillator mode 01 : RC oscillator mode 10 : XT oscillator mode 11 : EC (external clock mode)
FWDT0	FE02h	FWDT1, FWDT0 :
FWDT1	FE03h	10 : WDT prescale is 256 01 : WDT prescale is 64 11 : WDT prescale is 1 00 : WDT is a normal timer
FPMM0	FE04h	FPMM1, FPMM0 :
FPMM1	FE06h	00 : Microcontroller mode (code protected) 10 : Microcontroller mode 01 : Extended microcontroller mode 11 : Microprocessor mode

FIGURE 4.8.1: READING FUSE LOCATION



5.0 OVERVIEW OF PERIPHERALS

An array of sophisticated, high speed peripherals are incorporated on chip to meet the demands of real time applications. All peripherals are highly intelligent and have their own interrupts and error handling to free up the CPU as much as possible. There are three 16 bit timer/counters one of which can be split into two eight bit timers creating up to four timer/counter resources. Two high speed captures are provided for efficient interface to shaft encoders and other high speed pulse train sources. Two high speed pulse-width-modulation (PWM) outputs with up to 10 bit resolution make it possible to control a motor through power drivers. There are two external and several internal interrupt sources. The capture pins can be used as interrupt pins making it possible to have up to four external interrupts. Finally, there are 33 I/O pins most of which can be configured as inputs or outputs in software. A number of the I/O pins are multiplexed with peripheral functions or the system bus. In microcontroller mode 23 I/O pin are un-multiplexed.

5.1 THE BANK SELECT REGISTER (BSR, ADDRESS 0Fh)

All the peripheral registers are mapped into the data memory space. In order to accommodate the large number of registers in the 256 byte data memory space without taking away from the general purpose data RAM, a banking scheme has been used. A segment of the data memory, from address 10h to address 17h, is banked. A bank select register (BSR, address 0Fh) selects the currently active "peripheral bank". Effort has been made to group the peripheral registers of related functionality in one bank. However, it will still be necessary to switch from bank to bank in order to address all peripherals related to a single task. To alleviate this problem, a single cycle instruction, MOVLB (move literal value to BSR) is incorporated in the instruction set. In the PIC17C42 only the low four bits of the BSR are physically implemented, making it possible to address up to sixteen banks. Only four banks are actually used (see data memory map in figure 1.6.1).

6.0 DIGITAL I/O PORTS

The PIC17C42 has five ports A, B, C, D and E. Together these add up to 33 port pins. Most port pins have an associated data direction bit which configures it as input (DDR bit='1') or output (DDR bit='0'). When a port pin is read as an input, the value on the pin (and not the data latch) is read.

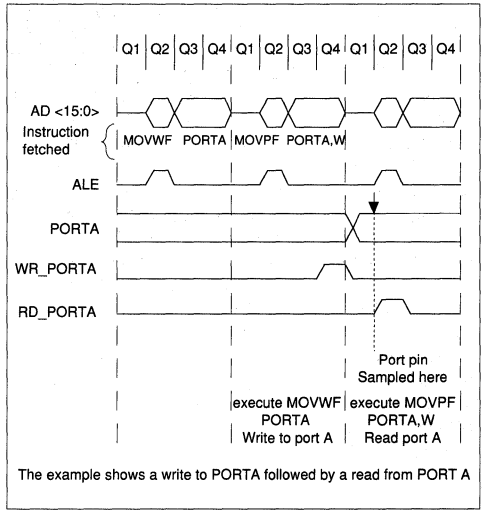
Most port pins are multiplexed with the system bus or peripheral functions. These pins are configured as port pins or peripheral inputs/outputs by control bits in corresponding peripheral registers. Once a port pin is selected for an alternate function, it's direction will be determined by the peripheral logic which will force the DDR bit to the required state.

Ports A, B, C, D and E and their associated DDR registers are mapped into the data-memory. Ports C, D and E multiplex with the system bus (AD <15:0>, ALE, $\overline{WR}$ and $\overline{OE}$).

6.1 PORT A

File 10h in Bank 0 is PORTA, a 6 bit port. There is no Data Direction Register associated with this port. Port A is multiplexed with peripheral functions as described in table 6.1.1. See figure 6.1.1 for block diagram of Port A and 6.0.1 for read/write timing.

FIGURE 6.0.1: I/O PORT READ AND WRITE TIMING



The example shows a write to PORTA followed by a read from PORT A

TABLE 6.1.1 : PORT A FUNCTIONS

Port Pin	Bit	Pin function	Alternate function
RA0/INT	bit 0	Input only (Schmitt Trigger) port pin	INT external interrupt input
RA1/RT	bit 1	Input only (Schmitt Trigger) port pin	RT external interrupt input. It is also the external clock input for the RTCC timer/counter.
RA2, RA3	bit 2,3	Input/output pins with Schmitt Trigger input and open-drain output. To use either of these two pins as an input, the user must write a '1' to the port data latch. If used as an output, external pull-up resistor must be provided. These pins can be pulled up to voltages higher than Vcc. Also, these two port pins provide higher current sink capability (See DC specs for details).	None
RA4/RX/DT	bit 4	Input only (Schmitt Trigger) port pin	If the SPEN bit (bit 7, RCSTA) is a '1' then this pin is configured by the serial port. In SYNC mode: It is data input or output (DT) In ASYNC mode: It is receive data input (RX).
RA5/TX/CK	bit 5	Input only (Schmitt Trigger) port pin	If the SPEN (bit 7, RCSTA) bit is a '1' then this pin is controlled by the serial port. In SYNC mode: It is either clock input (slave mode) or the clock output (master mode) in ASYNC mode: It is the transmit data output (TX).
	bit 6	This bit is unimplemented and reads as '0'.	
	bit 7	No pin associated	This is a control bit ($\overline{PUEB}$) for Port B. No port pin is associated with this bit. $\overline{PUEB}$=0 enables weak pull-ups on Port B.

6.1.1 Using RA2, RA3 Pins as Output

PortA does not have an associated data direction register. When using them as outputs, read-modify-write instructions (such as BCF, BSF, BTF) are not recommended on PortA, since a read will read the port pins but a write will write to the port data latch. Such an operation may inadvertantly cause RA2, RA3 to switch from output to input or vice-versa.

FIGURE 6.1.1: PORT A BLOCK DIAGRAMS

FIGURE 6.1.1A

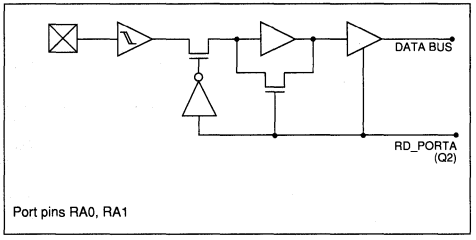


FIGURE 6.1.1B

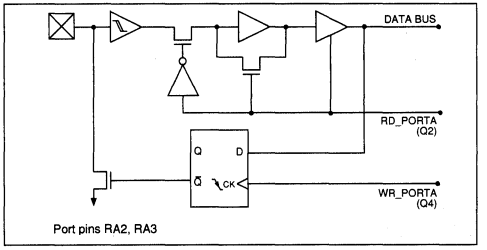
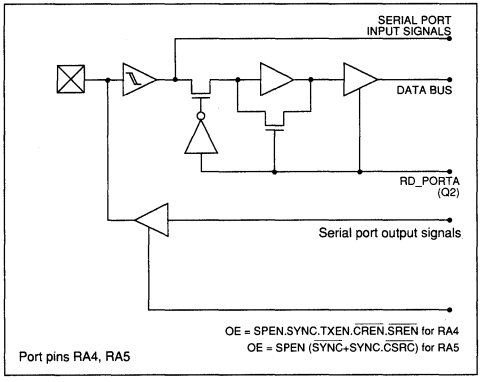


FIGURE 6.1.1C



6.1.2 SUMMARY OF PORT A REGISTERS

Register Name	Function	Address	Reset Value
PORTA	Port A pins when read, Port A latch when written (RA2/RA3 only)	Bank 0, File10h	00XXXXXb
RTCSTA	RTCC status/control register (configures RA0/INT & RA1/RT pins)	File 05h	0000000b
RCSTA	Serial port receive status/control register (configures RA4/RX/DT and RA5/TX/CK pins)	Bank0, File 13h	000000Xb

6.2 PORT B

Port B is an eight bit wide bidirectional port. It is mapped in Bank0, File 12h. Writing to this address writes to the port latch while reading it will read the port pins. An eight bit data direction register (DDRB, Bank 0, File 11h) configures each port pin as an input or output. A '0' in the 'DDR' register configures the port as an output. Each port pin also has a software configurable weak pull-up (~100 µA typical). A control bit $\overline{\text{PUEB}}$ (bit 7, Bank 0, File 10h, Register PORTA) can enable ($\overline{\text{PUEB}}$ = '0') or disable ($\overline{\text{PUEB}}$ = '1') the pull-ups. The weak pull-up is turned off for any pin configured as output.

Most of the pins of Port B are multiplexed with peripheral functions. Table 6.2.1 describes their alternate functions. When a pin is redefined to be a port pin from a peripheral pin, its data direction bit may be left in an unknown state. The user will need to re-initialize the DDR bit properly. See figures 6.2.1 and 6.2.2 for block diagrams of port B and figure 6.0.1 for read/write timing.

Port B also has an "interrupt on change" feature. When configured as input, its output data latch can be used as a compare latch. An active high output is generated on mismatch between the pin and the latch. The "mismatch" outputs of all the input pins are OR-ed together to generate the IRB interrupt. All the output pins are excluded from the comparison. Thus, an interrupt is generated when the port input changes. This interrupt can wake the chip up from SLEEP mode.

The interrupt is latched in the IRB bit (bit 7, Register PIR, Bank1, File 16h). IRB is readable and writable by the CPU. The user, in the interrupt service routine, can clear the interrupt in one of two ways:

a) Disable the interrupt by clearing the corresponding interrupt enable bit, IEB.

b) Read PortB and write back the pin value to the data latch. This will end mismatch condition and therefore the mismatch output. Next, the user must clear bit IRB.

TABLE 6.2.1: PORT B FUNCTIONS

Port Pin	Bit	Pin Function	Alternate Function
RB0/CAP1	bit 0	Input/Output port pin with Schmitt Trigger input	CAP1: Capture1 input
RB1/CAP2	bit 1	Input/Output port pin with Schmitt Trigger input	CAP2: Capture2 input
RB2/PWM1	bit 2	Input/Output port pin with Schmitt Trigger input	PWM1 output. This pin is configured as the PWM1 output if control bit PWM1ON (bit 4, Register TCON2, Bank 3, File 17h) is set to '1'.
RB3/PWM2	bit 3	Input/Output port pin with Schmitt Trigger input	PWM2 output. This pin is configured as the PWM2 output if the control bit PWM2ON (bit 5, Register TCON2, Bank 3, File 17h) is '1'
RB4/TCLK12	bit 4	Input/Output port pin with Schmitt Trigger input	TCLK12: external clock input for timer1 and timer2
RB5/TCLK3	bit 5	Input/Output port pin with Schmitt Trigger input	TCLK3: external clock input for timer3
RB6	bit 6	Input/Output port pin with Schmitt Trigger input	
RB7	bit 7	Input/Output port pin with Schmitt Trigger input	

FIGURE 6.2.1: PORT B BLOCK DIAGRAM

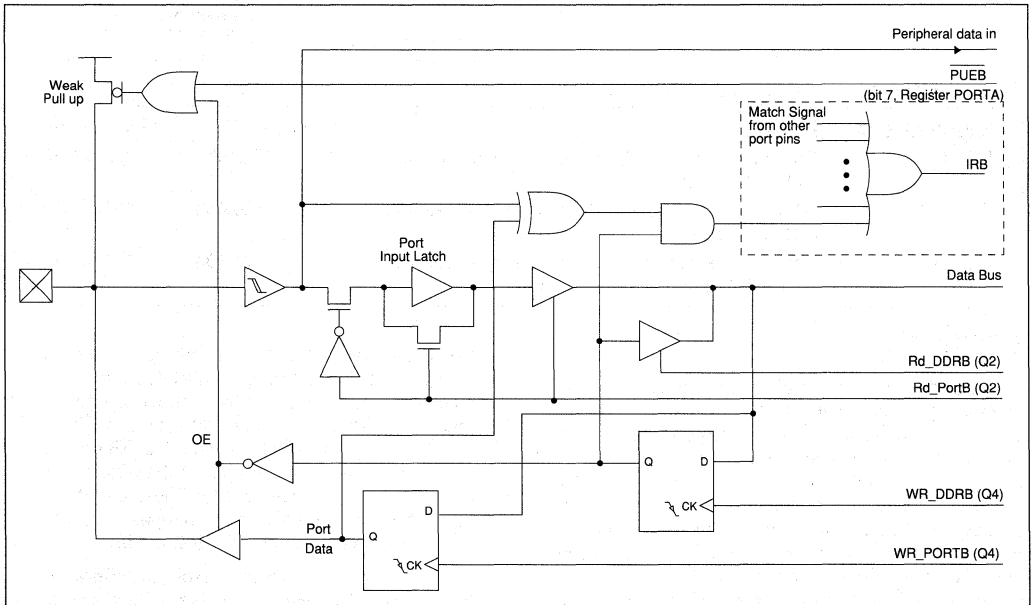
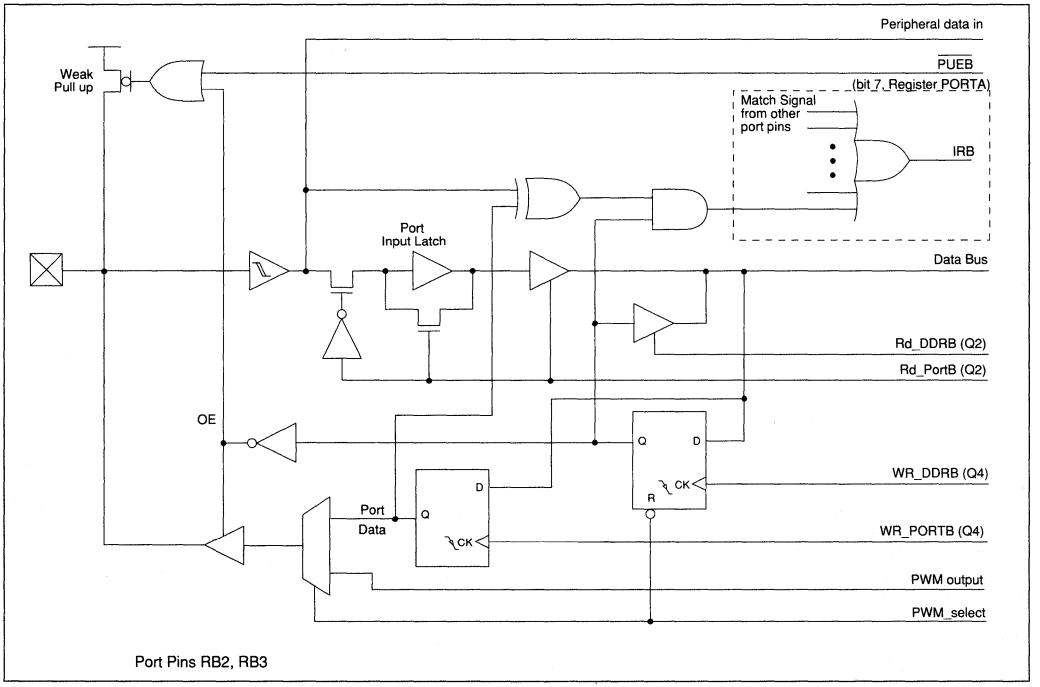


FIGURE 6.2.2: PORT B BLOCK DIAGRAM



6.2.1 SUMMARY OF PORT B REGISTERS

Register Name	Function	Address	Reset Value
PORTB	Port B pins when read Port B latch when written	Bank 0, File 12h	XXXXXXXXb
DDRB	Port B data direction register	Bank 0, File 11h	11111111b
PORTA (bit $\overline{PUEB}$)	Port A data/ $\overline{PUEB}$ bit	Bank 0, File 10h	00XXXXXXb
PIR (bit IRB)	Peripheral interrupt register	Bank 1, File 16h	00000010b
PIE (bit IEB)	Peripheral interrupt enable register	Bank 1, File 17h	00000000b
INTSTA (bit PEIE)	Interrupt status register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU status register	File 06h	0011XX00b
TCON2	Timer/PWM/capture control registers	Bank 3, File 17h	00000000b

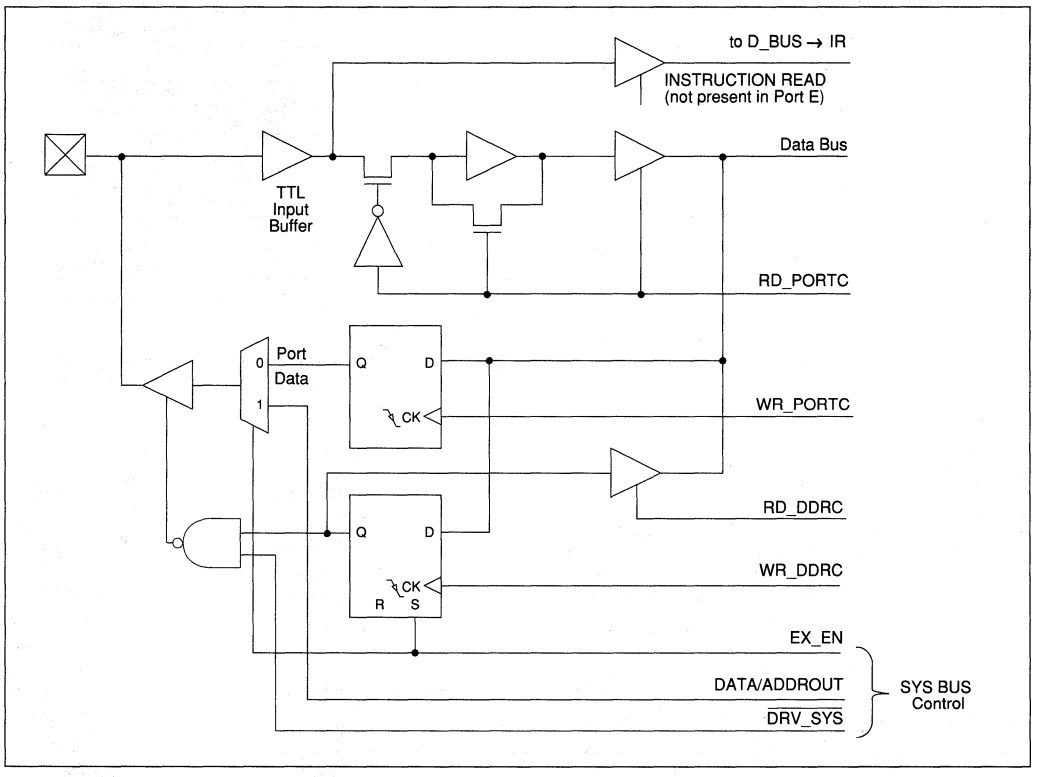
6.3 PORT C

Port C is an eight bit wide bidirection port mapped in File 11h, Bank 1. The corresponding data direction register DDRC (file 10h, Bank 1) can configure each pin as an input (if DDRC bit is '1') or output (if DDRC bit is '0'). This port is multiplexed with AD<7:0>, the lower byte of the Address/Data bus. Bit 0 of Port C is AD<0>. See figure 6.3.1 for block diagram of Port C and figure 6.0.1 for read/write timing.

6.3.1 SUMMARY OF PORT C REGISTERS

Register Name	Function	Address	Reset Value
PORTC	Port C pins when read Port C latch when written	Bank 1, File 11h	XXXXXXXXb
DDRC	Port C data direction register	Bank 1, File 10h	11111111b
INTSTA (bit PEIE)	Interrupt status register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU status register	File 06h	0011XX00b

FIGURE 6.3.1: BLOCK DIAGRAM OF PORTS C, D AND E



6.4 PORT D

Port D is an eight bit wide bidirection port mapped in File 13h, Bank 1. The corresponding data direction register DDRD (file 12h, Bank 1) can configure each pin as an input (if DDRD bit is '1') or output (if DDRD bit is '0'). This port is multiplexed with AD<15.8>, the higher byte of the Address/Data bus. Bit 0 of Port D is AD<8>. See figure 6.3.1 for block diagram of Port C and figure 6.0.1 for read/write timing.

6.5 PORT E

PORTE is a 3 bit wide bidirectional port mapped in data memory (file 15h, Bank1). The corresponding Data Direction Register, DDRE, is mapped at file 14h, Bank 1. Each port pin can be configured as an input (DDRE bit = '1') or an output (DDRE bit = '0'). Only the three lowest significant bits are physically implemented in 17C42. The unimplemented bits read as '0'. See Figure 6.3.1 for block diagram of Port E and Figure 6.0.1 for read/write timing. Port E is multiplexed with control outputs ALE, WR and OE in external execution mode.

FIGURE 6.4.1: SUMMARY OF PORT D REGISTERS

Register Name	Function	Address	Reset Value
PORTD	Port D pins when read Port D latch when written	Bank 1, File 13h	XXXXXXXXb
DDRD	Port D data direction register	Bank 1, File 12h	11111111b

6.5.1 SUMMARY OF PORT E REGISTERS

Register Name	Function	Address	Reset Value
PORT E	Port E pins when read Port E latch when written	Bank 1, File15h	00000XXXb
DDRE	Port E data direction register	Bank 1, File14h	00000111b

TABLE 6.5.1 PORT E FUNCTIONS

Port Pin	Bit	Pin Function	System Bus Function (External execution)
RE0/ALE	bit 0	Input/output port. TTL input buffer.	ALE output
RE1/$\overline{OE}$	bit 1	Input/output port. TTL input buffer.	$\overline{OE}$ output
RE2/$\overline{WR}$	bit 2	Input/output port. TTL input buffer.	$\overline{WR}$ output

7.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

The serial port can operate either a full-duplex asynchronous mode or in a half-duplex clocked synchronous mode. Synchronous mode uses a bi-directional data pin and a bi-directional clock pin. In synchronous mode, the clock can be either internal (master mode) or external (slave mode). In asynchronous mode, the clock is always derived internally. A dedicated 8 bit Baud Rate Generator (BRG) is used for internal clock generation. In both modes, receiver and transmitter are double buffered, 8 or 9 data bits are supported and separate transmit and receive interrupts are available.

7.1 ASYNCHRONOUS MODE

The asynchronous mode is selected by setting the SYNC bit to '0' in the TXSTA register. Furthermore, SPEN bit (Serial Port Enable, bit 7, Register RCSTA, Bank 0) has to be set to enable RA4 and RA5 as serial port pins. SPEN=0 will configure these pins as port pins. In asynchronous mode the RX pin receives data and the TX pin transmits data in a full duplex mode. Data is transmitted and received least significant bit first. Both receive and transmit operate on the same internally generated clock which is derived from the Baud Rate Generator (Register SPBRG, Bank 0, File 17h). Data on the RX pin is sampled on the 7th, 8th and 9th pulses of a 16X (16 times the baud clock) internal clock. A majority of these three bits decide whether a one or a zero was received. In addition to the 8 or 9 data bits, one start bit and one stop bit are sent. Parity is not supported directly in hardware, but can easily be implemented in software. Asynchronous mode operation is stopped during SLEEP.

7.1.1 Asynchronous Mode Transmission

Once asynchronous mode is selected (SYNC=0, bit 4 Register TXSTA) and serial port outputs are enabled (SPEN=1, bit 7, Register RCSTA) transmission can be enabled by setting TXEN bit to '1' (bit 5, TXSTA register). Actual transmission will begin when a word is written to the transmit buffer register (TXREG, bank0, file 16h) and the Baud Rate Generator produces a shift clock (figure 7.1.1.1). A start bit is sent out first (logic '0'), followed by 8 or 9 data bits and a stop bit (logic '1'). Transmitted data appears on RA5/TX/CK pin. Transmission can also be started by first writing a word to the TXREG and then setting TXEN to '1'.

The transmit register (TXREG) is double buffered. As the user writes to TXREG, the data is transferred from the buffer to the transmit shift register (TSR), thus freeing up the buffer register. An interrupt is pending as long as TXREG is empty. Indicating that the transmit buffer register (TXREG) is free to accept another word. This interrupt request is bit 1 (TBMT) of PIR (peripheral interrupt request register; Bank 1, file 16h) register. This interrupt can be enabled or disabled by bit 1 (TXIE) of PIE (peripheral interrupt enable; Bank 1, file 17h) register. TXIE=1 enables the interrupt. Regardless of TXIE, the TBMT bit will always show the status of the TXREG buffer (can not be affected in software) and can be used as a status bit. The interrupt request bit (TBMT) is read only. Therefore, to avoid unwanted interrupts (say, at the end of a transmission) the user will need to mask off this interrupt.

In addition to TXIE bit, two other bits will affect the transmit interrupt. They are: PEIE (bit3, INTSTA register, file 07h) that enables (if='1') or disables (if='0') all peripheral interrupts, and GLINTD (Global Interrupt Disable, bit 4, CPUSTA register, file 06h) bit that disables all interrupts if set to '1'.

While TBMT (Transmit Buffer Empty) indicates the status of the transmit buffer register, another bit TRMT (bit1, register TXSTA) indicates the status of the transmit shift register. It is a read only bit. TRMT=1 implies transmit shift register is empty. The user can determine exactly when transmission is completed by polling this bit. TRMT is set after stop bit is sent out.

CREN or SREN bits do not affect asynchronous transmission. Clearing TXEN during transmission aborts transmission, reverts TX pin to hi-impedance and resets the transmitter.

FIGURE 7.1.1.1: ASYNCHRONOUS TRANSMISSION

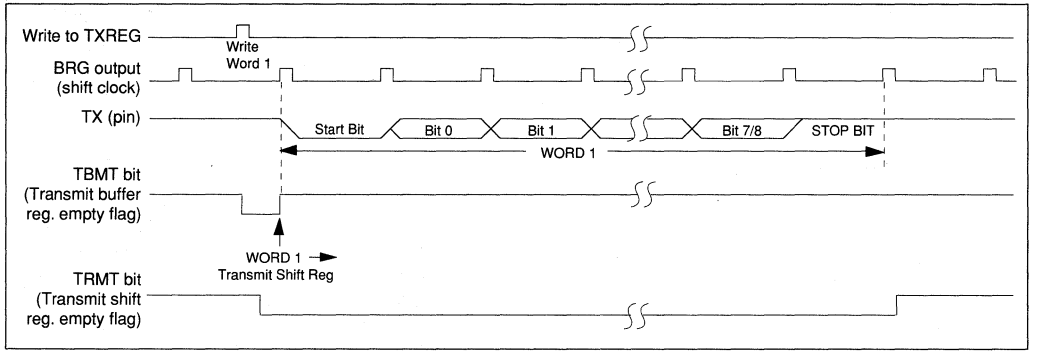
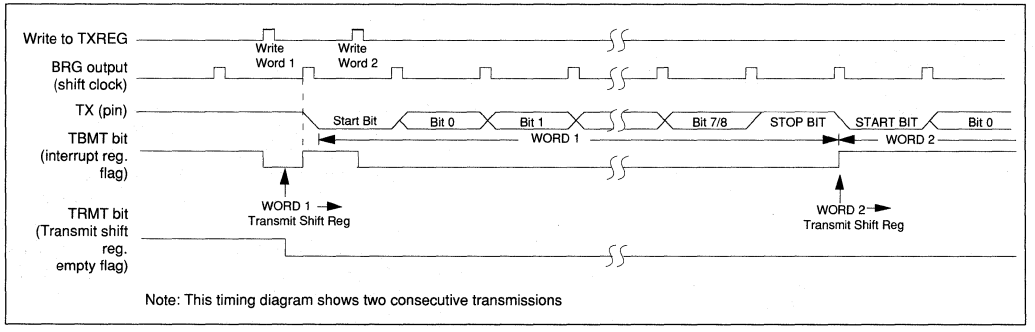


FIGURE 7.1.1.2: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions

If 9 bit transmission is selected (TX8/9=1, bit 6, register TXSTA) the 9th bit should be written to TXD8 (bit0, TXSTA). This bit is double buffered as well. The 9th bit must be written before writing the data word to TXREG, since the latter triggers the transfer of the entire word to the transmit shift register.

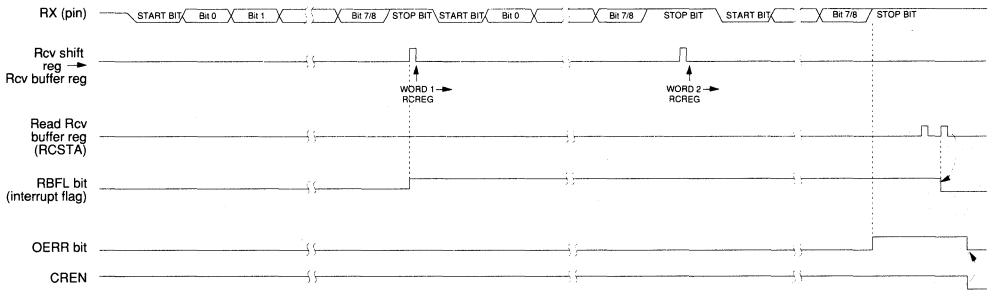
7.1.2 Asynchronous Mode Reception

Data is received on RA4/RX/DT pin. Reception is enabled by setting the CREN bit (bit4, register RCSTA) to '1'. The SREN bit (bit5, RCSTA) has no function in asynchronous mode. Reception begins when a start-bit is detected on RX pin. The Baud Rate Generator internally generates a 16x clock. Every incoming bit is sampled on the 7th, 8th and the 9th time slot and a majority detection is done to determine the value of the bit. After sampling the stop bit (i.e. halfway through stop bit), the received data is transferred to the receive buffer register (RCREG) if the buffer register is empty. The RCREG is actually a two word deep FIFO. Therefore, it is possible to receive two words, transfer them to RCREG and begin receiving the 3rd word in the receive shift register (RSR). If at the time of reception of the last bit of the 3rd word, the RCREG has still not been read (and therefore is holding two words) then the receiver control logic will set the overrun error bit, OERR (bit1, register RCREG). In case of overrun, the word in the shift register is lost (i.e. it can not be read). The RCREG can be read twice to retrieve the first two words. The user will need to clear OERR by resetting the receiver (by clearing CREN). Clearing OERR is essential since once the overflow flag is set, the receiver simply stops transferring RSR to RCREG.

The framing error bit, FERR (bit 2, Register RCSTA) and the 9th receive bit, RCD8 (bit 0, RCSTA) are buffered the same way as the receive data. Reading RCREG will load the RCD8 and FERR bits with new values. The user, therefore, must read the RCSTA register before reading the received data (RCREG) in order to obtain FERR and 9th data bit information. If the RCREG is read first, then the status register RCSTA will be loaded with new status information and the old information will be lost. The framing error bit, FERR, is set if the stop bit is detected to be a '0'.

A receive interrupt flag RBFL, is set (bit0, register PIR) when the receive shift register content is shifted to the receive buffer register. This interrupt can be enabled or disabled via the RCIE (Receive interrupt enable) bit (bit0, register PIE). RCIE=1 will enable the interrupt. The RBFL (receive buffer full interrupt flag) bit is a read only bit and is cleared when the receive buffer is read. However, if the receive shift register is full, it will transfer its contents to the receive buffer register and the RBFL

FIGURE 7.1.2.1: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows 3 words appear on RX input. The RCREG (Receive buffer) is read after the 3rd word, therefore causing the OERR (overrun) bit to set.

bit will be set again. To enable receive interrupt, the Peripheral Interrupt Enable bit, PEIE (bit3, INTSTA register, file 07h). must be set and the Global Interrupt Disable bit, GLINTD (bit4, CPUSTA register, file 06h), must be cleared.

7.2 SYNCHRONOUS MODE

The synchronous mode is selected by setting the SYNC bit (bit4, TXSTA register) to a '1'. In addition, the SPEN bit (bit7, RCSTA register) must be set to a '1' to configure the RA5/TX/CK and RA4/RX/DT pins as CK (synchronous clock) and DT (sync data) pins respectively. Synchronous mode is half duplex with the DT pin as data input during reception and data output during transmission. The CK pin is clock output if internal clock option (master mode) is selected by setting the CSRC (bit7, TXSTA register) bit to a '1'. If CSRC='0' then the CK pin is clock input (synchronous slave mode).

As in asynchronous mode, 8 or 9 data bits are transmitted or received. No start or stop bits are sent or received.

7.2.1 Synchronous Mode Transmission

Once the sync mode is selected (SYNC='1') and the serial port is enabled (SPEN='1', register RCSTA), transmission is enabled by setting the TXEN (transmit enable, bit5, TXSTA register) bit to a '1'. This will configure the TX pin as an output. Actual transmission will begin when a word is written to the transmit buffer register (TXREG). The transmitter is double buffered. If the transmit shift register (TSR) is empty then the word will be transferred from TXREG to TSR. The first data bit will be shifted out at the next available rising edge of the clock. Data out is stable around the falling edge of the sync clock. Transmission can also be started by first writing a data word to TXREG and then setting TXEN='1'. This method may be advantageous when slow baud rates are selected, since the Baud Rate Generator is kept under reset when TXEN=CREN=SREN=0. Setting the TXEN bit will start the BRG, creating a shift clock immediately.

The TBMT interrupt (bit1, PIR register) is pending whenever the transmit buffer is empty and ready to accept another word. The interrupt has a corresponding mask bit (TXIE, bit1, Register PIE). TXIE='1' enables the transmit interrupt while TXIE='0' disables it. Regardless of TXIE, TBMT will always show the status of the TXREG (not affected by software) and can be used as a status bit. To enable the transmit interrupt, Peripheral Interrupt Enable, PEIE (bit3, INTSTA register, file 07h) bit must be set and Global Interrupt Disable, GLINTD (bit4, CPUSTA register, file 06h) bit must be cleared.

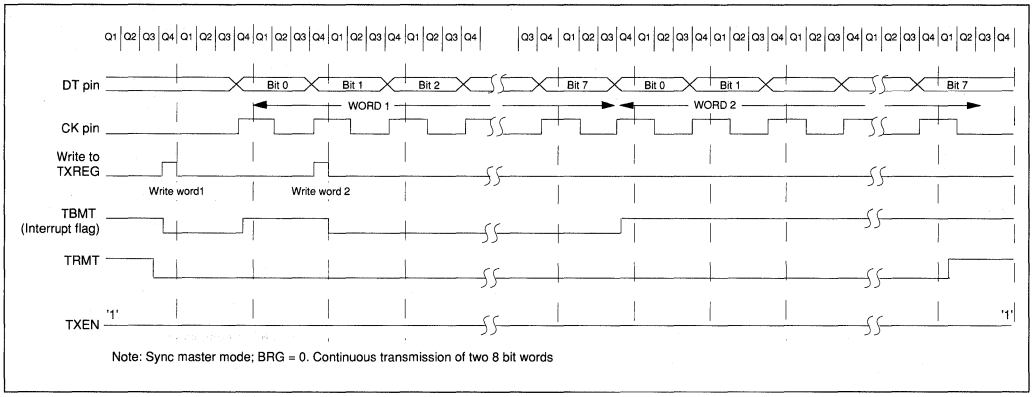
While TBMT (Transmit Buffer Empty) indicates the status of the transmit buffer register, another bit TRMT (bit1, register TXSTA), indicates the status of the transmit shift register. It is a read only status bit. TRMT=1 implies that the transmit shift register is empty. The user can determine exactly when transmission is over by polling this bit. TRMT is set after the last bit is sent out.

If 9 bit transmission is selected, the 9th bit should be written to bit TXD8 (bit0, TXSTA). This bit is also double buffered. The 9th bit must be written prior to writing the data word to TXREG, since a write to the TXREG triggers the transfer of the entire word to the transmit shift register.

In sync master mode, the CK pin will output clocks only during actual transmission (figure 7.2.1.1). In sync slave mode clock input may be present on the pin at all times.

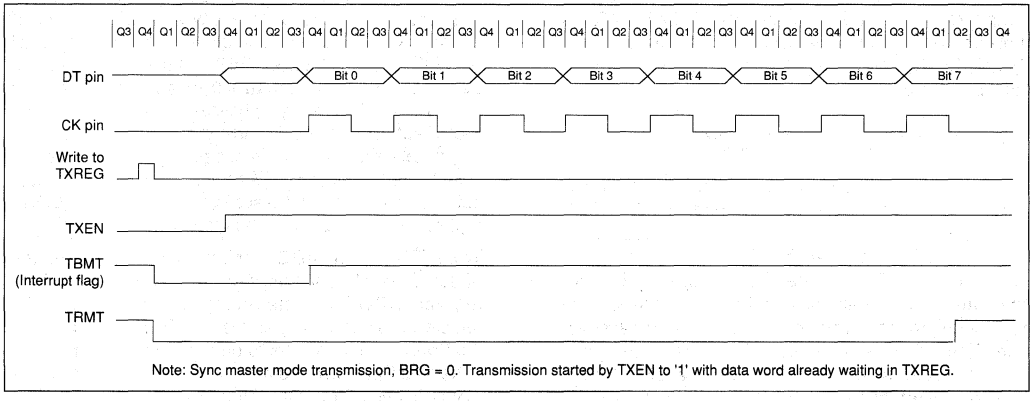
If TXEN is cleared during transmission of a word, transmission will be aborted and the DT and CK pins will revert to hi-impedance. If either the CREN or the SREN bit is set to a '1', transmission is also aborted and the DT pin will go into hi-impedance state (for reception). The CK pin will remain an output if CSRC=1 (internal clock). The transmitter logic, although disconnected from the pins, is not reset. The user must clear the TXEN bit to reset the transmitter. This is particularly important if the SREN was set to a '1' to interrupt an ongoing transmission. In this case, after reception of a single word, the SREN bit will reset and the serial port will revert back to transmit mode (since TXEN is still set). This means the DT pin will turn around and start driving. To avoid this, TXEN should be cleared.

FIGURE 7.2.1.1: SYNCHRONOUS TRANSMISSION



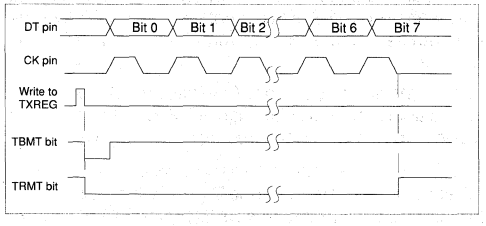
Note: Sync master mode; BRG = 0. Continuous transmission of two 8 bit words

FIGURE 7.2.1.2: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



Note: Sync master mode transmission, BRG = 0. Transmission started by TXEN to '1' with data word already waiting in TXREG.

FIGURE 7.2.1.3: SYNCHRONOUS TRANSMISSION (SLAVE)



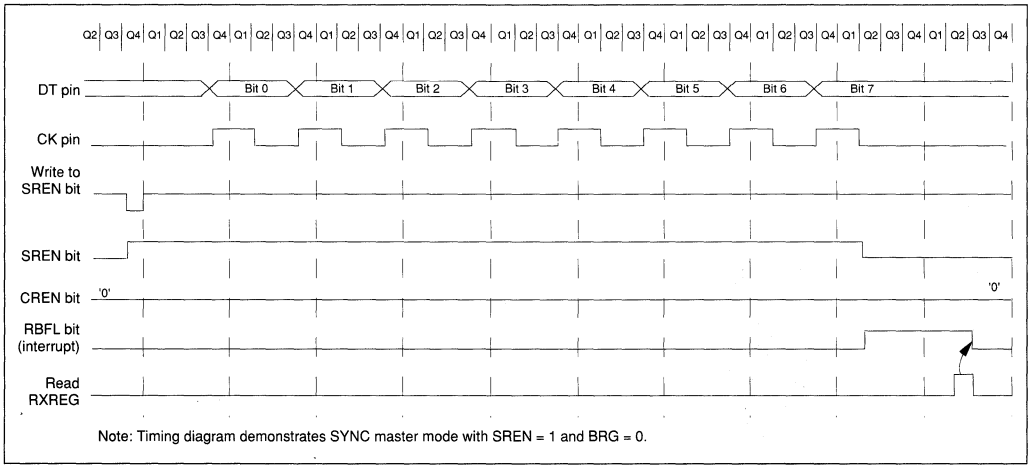
7.2.2 Synchronous Mode Reception

Data is sampled on the DT pin on the falling edge of the clock. Reception is enabled by either setting the SREN bit (Single Receive Enable, bit5, RCSTA register) or the CREN bit (Continuous Receive Enable, bit4, RCSTA register). If SREN is set, one word is received after which SREN is reset in hardware. If the CREN bit is set, words are received continuously (and read off by the CPU presumably) until CREN is reset by software. If both CREN and SREN are set, then CREN will take precedence.

After a word is received completely, it is transferred from the receive shift register (RSR) to the receive buffer register (RCREG) thus freeing up the RSR to receive the next word. With CREN=1, it is possible to receive consecutive data words without any discontinuity in between. This makes it possible to receive data words of larger size, e.g. 16 bit. In synchronous slave mode the SREN bit is a don't care.

The RCREG is actually a two word deep FIFO. Therefore, it is possible to receive two words, transfer them to RCREG and begin receiving the 3rd word in the receive shift register (RSR). If, at the time of reception of the last bit of the 3rd word, the RCREG has still not been read (and therefore is holding two words) then the receiver control logic will set the overrun error bit, OERR (bit1, register RCSTA). In case of an overrun, the word in the shift register is lost (i.e. it can not be read). The RCREG can be read twice to retrieve the first two words. The user will need to clear OERR by resetting the receiver (by clearing CREN). Clearing OERR is essential since once overflow flag is set the receiver simply stops transferring RSR to RCREG.

FIGURE 7.2.2.1: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates SYNC master mode with SREN = 1 and BRG = 0.

An interrupt is issued when RSR transfers a data word to receive buffer register, RCREG, indicating that RCREG is full. The interrupt flag (RBFL, bit0, register PIR) can be masked by interrupt mask bit RCIE (Receive interrupt enable, bit0, register PIE). RCIE=1 enables the receive interrupt.

The 9th bit of the received word is loaded into RCD8 (bit0, RCSTA). This bit is buffered the same way as the receive data. Reading the RCREG register will load the new 9th bit. Therefore, the user must read the RCSTA register before reading the received data word from RCREG.

7.2.3 Synchronous Slave Mode/SLEEP Mode Interaction:

When the part is put into SLEEP mode, all on chip phase clocks are stopped (part is held in Q1 state; see SLEEP section for details). In SLEEP, synchronous slave mode operation is possible because this mode uses external clock.

SLEEP/sync slave receive: If receive is enabled (SREN = '1') prior to invoking SLEEP mode, then a word may be received during SLEEP and at the completion of such reception the RSR will be transferred to RCREG (assuming it is empty). Simultaneously a receive interrupt will be generated which will wake the chip up, provided this interrupt was enabled (by setting RCIE = PEIE = '1'). If GLINTD = '0', then additionally the interrupt will be responded to by jumping to interrupt vector 0020h. If the receive interrupt is disabled, prior to invoking SLEEP mode, then words are received during SLEEP without waking up the processor. Overflow bit will be set if three words are received.

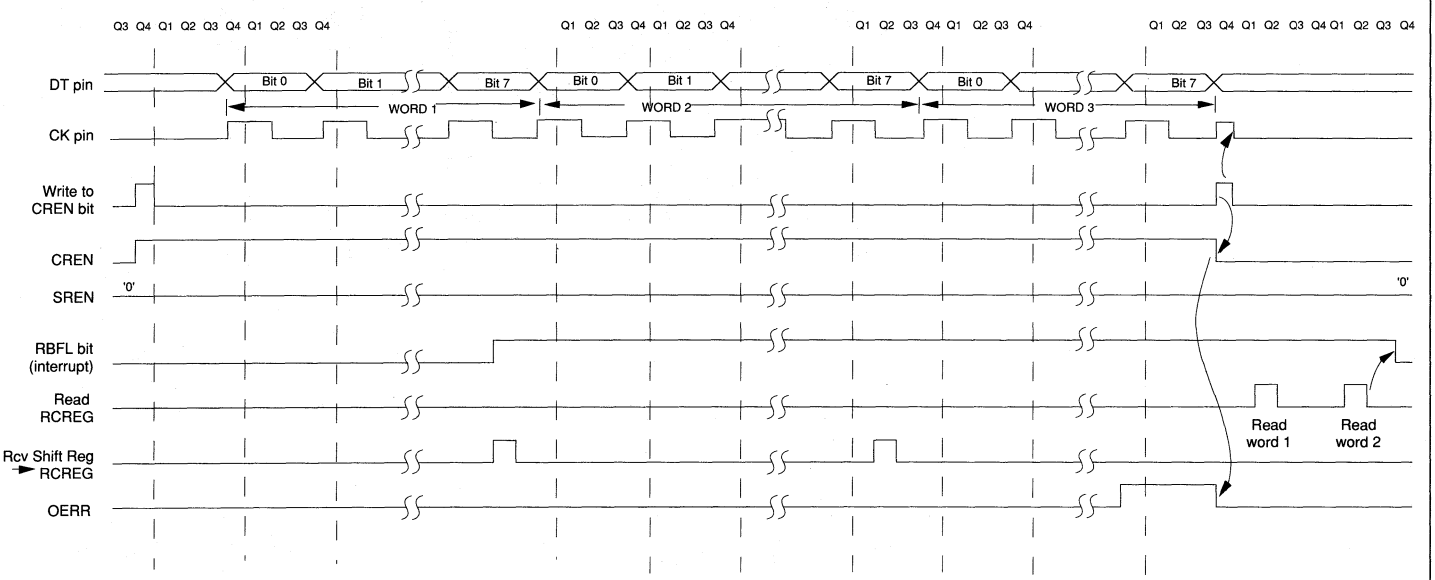
SLEEP/sync slave transmit: If two words are written to TXREG and then the chip is put into SLEEP the following sequence of events will occur. The first word will immediately transfer to the TSR. The second word will remain in TXREG. Transmit interrupt (TBMT) will stay inactive (low). As the first word is shifted out, the second word will transfer from TXREG to TSR and the transmit interrupt (TBMT) will be raised again. This will wake up the chip provided the interrupt was not masked (i.e. TXIE = PEIE = '1'). If GLINTD = 0, then branch to interrupt vector 0020h will take place as well.

7.3 BAUD RATE GENERATOR

The serial port is equipped with a dedicated 8 bit Baud Rate Generator (SPBRG, bank0, file 17h). The SPBRG register is readable and writable. The SPBRG register controls the period of a free running 8 bit timer. In synchronous mode the baud rate is fosc/4(x+1) where fosc = oscillator or clock-in frequency and x = value written to SPBRG register. In asynchronous mode the baud rate is fosc/64(x+1). Tables 7.3.1 and 7.3.2 show baud rate values for different SPBRG value and clock-in frequency. SPBRG is unknown following power-on reset.

Writing a value to the SPBRG clears the timer. This guarantees that the timer does not go through an overflow cycle, before outputting the appropriate baud rate.

FIGURE 7.2.2.2: SYNCHRONOUS MASTER MODE RECEPTION, CREN



Note : Synchronous master mode reception with CREN. Overflow occurs after two words have been received and reception of the 3rd word is almost complete. Resetting CREN resets the receiver, including the OERR bit. The two words are read which then clears the RBFL flag. The 3rd word is lost.

TABLE 7.3.1: BAUD RATES FOR SYNCHRONOUS MODE

BAUD RATE (K)	fosc = 20MHZ KBAUD	%ERROR	SPBRG value (decimal)	16MHZ KBAUD	%ERROR	SPBRG value (decimal)	10MHZ KBAUD	%ERROR	SPBRG value (decimal)	7.15909MHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	NA	-	-	NA	-	-	NA	-	-
9.6	NA	-	-	NA	-	-	9.766	+1.73	255	9.622	+0.23	185
19.2	19.53	+1.73	255	19.23	+0.16	207	19.23	+0.16	129	19.24	+0.23	92
76.8	76.92	+0.16	64	76.92	+0.16	51	75.76	-1.36	32	77.82	+1.32	22
96	96.15	+0.16	51	95.24	-0.79	41	96.15	+0.16	25	94.20	-1.88	18
300	294.1	-1.96	16	307.69	+2.56	12	312.5	+4.17	7	298.3	-0.57	5
500	500	0	9	500	0	7	500	0	4	NA	-	-
HIGH	5000	-	0	4000	-	0	2500	-	0	1789.8	-	0
LOW	19.53	-	255	15.625	-	255	9.766	-	255	6.991	-	255

BAUD RATE (K)	fosc = 5.0688MHZ KBAUD	%ERROR	SPBRG value (decimal)	3.579545MHZ KBAUD	%ERROR	SPBRG value (decimal)	1MHZ KBAUD	%ERROR	SPBRG value (decimal)	32.768KHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	0.303	+1.14	26
1.2	NA	-	-	NA	-	-	1.202	+0.16	207	1.170	-2.48	6
2.4	NA	-	-	NA	-	-	2.404	+0.16	103	NA	-	-
9.6	9.6	0	131	9.622	+0.23	92	9.615	+0.16	25	NA	-	-
19.2	19.2	0	65	19.04	-0.83	46	19.24	+0.16	12	NA	-	-
76.8	79.2	+3.13	15	74.57	-2.90	11	83.34	+8.51	2	NA	-	-
96	97.48	+1.54	12	99.43	+3.57	8	NA	-	-	NA	-	-
300	316.8	+5.60	3	298.3	-0.57	2	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	1267	-	0	894.9	-	0	250	-	0	8.192	-	0
LOW	4.950	-	255	3.496	-	255	0.9766	-	255	0.032	-	255

TABLE 7.3.2: BAUD RATES FOR ASYNCHRONOUS MODE

BAUD RATE (K)	fosc = 20MHZ KBAUD	%ERROR	SPBRG value (decimal)	16MHZ KBAUD	%ERROR	SPBRG value (decimal)	10MHZ KBAUD	%ERROR	SPBRG value (decimal)	7.15909MHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129	1.203	+0.23	92
2.4	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64	2.380	-0.83	46
9.6	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15	9.322	-2.90	11
19.2	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5
76.8	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1	NA	-	-
96	104.2	+8.51	2	NA	-	-	NA	-	-	NA	-	-
300	312.5	+4.17	0	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	312.5	-	0	250	-	0	156.3	-	0	111.9	-	0
LOW	1.221	-	255	0.977	-	255	0.6104	-	255	0.437	-	255

BAUD RATE (K)	fosc = 5.0688MHZ KBAUD	%ERROR	SPBRG value (decimal)	3.579545MHZ KBAUD	%ERROR	SPBRG value (decimal)	1MHZ KBAUD	%ERROR	SPBRG value (decimal)	32.768KHZ KBAUD	%ERROR	SPBRG value (decimal)
0.3	0.31	+3.13	255	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	1
1.2	1.2	0	65	1.190	-0.83	46	1.202	+0.16	12	NA	-	-
2.4	2.4	0	32	2.432	+1.32	22	2.232	-6.99	6	NA	-	-
9.6	9.9	+3.13	7	9.322	-2.90	5	NA	-	-	NA	-	-
19.2	19.8	+3.13	3	18.64	-2.90	2	NA	-	-	NA	-	-
76.8	79.2	+3.13	0	NA	-	-	NA	-	-	NA	-	-
96	NA	-	-	NA	-	-	NA	-	-	NA	-	-
300	NA	-	-	NA	-	-	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	79.2	-	0	55.93	-	0	15.63	-	0	0.512	-	0
LOW	0.3094	-	255	0.2185	-	255	0.0610	-	255	0.0020	-	255

7.4. SERIAL PORT REGISTERS

7.4.1 Summary of Serial Port Registers

Register Name	Function	Address	Reset Value
RCSTA	Receive status/control register	Bank 0, File 13h	0000000Xb
RCREG	Receive buffer register	Bank 0, File 14h	XXXXXXXXb
TXSTA	Transmit status/control register	Bank 0, File 15h	0000001Xb
TXREG	Transmit buffer register	Bank 0, File 16h	XXXXXXXXb
SPBRG	Baud Rate Generator	Bank 0, File 17h	XXXXXXXXb
PIR	Peripheral interrupt flag register	Bank 1, File 16h	00000010b
PIE	Peripheral interrupt enable register	Bank 1, File 17h	00000000b
INTSTA	Interrupt status register	File 07h	00000000b
CPUSTA	CPU status register	File 06h	0011XX00b

FIGURE 7.4.1.1 RCSTA: RECEIVE STATUS & CONTROL REGISTER

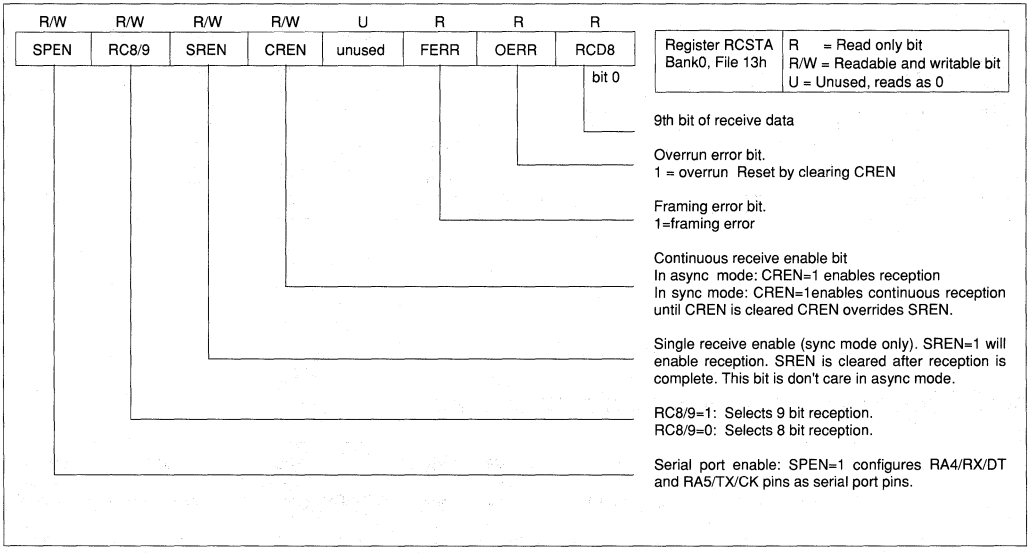
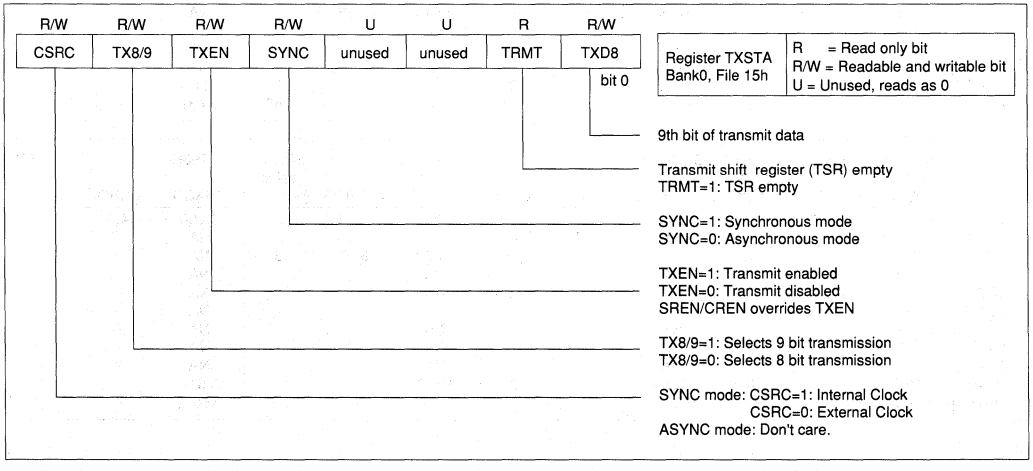


FIGURE 7.4.1.2 TXSTA: TRANSMIT STATUS & CONTROL REGISTER



7.5 SUMMARY OF SERIAL PORT PINS

The serial port uses two pins, RA4/RX/DT and RA5/TX/CK. If SPEN bit (bit 7, RCSTA) is set then these pins are controlled by the serial port. If SPEN=0, then they are configured as input only port pins. **(Both pins have Schmitt Trigger input buffer.)**

Pin Name	SPEN = 0	SPEN = 1		
		SYNC Master Mode	SYNC Slave Mode	ASYNC Mode
RA4/RX/DT	input only port pin	DT: Data in/out Data output if TXEN=1 and CREN=0 and SREN=0, Hi-impedance input otherwise		RX: Receive input, Always hi-impedance input.
RA5/TX/CK	input only port pin	CK: clock output Always a driven output	CK: clock input Always hi-impedance input	TX: Transmit Driven output if TXEN=1. Hi-impedance input if TXEN=0

8.0 TIMER/COUNTERS: OVERVIEW

The PIC17C42 has a rich set of timer/counters: Two 8 bit timer counters (also configurable as one sixteen bit timer/counter) and two 16 bit timer/counters. These can be configured as:

-Two 16 bit + two 8 bit timer/counters

-Three 16 bit timer/counters

A brief overview of these timer/counters is as follows:

RTCC <16>: RTCC <16> is a 16 bit timer/counter consisting of two 8 bit sections (RTCCH <8>, RTCCL<8>). It has a programmable 8 bit prescaler. RTCC can increment off internal clock (OSC/4) or external clock input on the RT pin. RTCC generates an interrupt on overflow.

TMR1 <8>, TMR2 <8>: These are two 8 bit timer/counters. They each have an eight bit period register (PR1 and PR2 respectively) and an interrupt. In counter mode, their clock comes from pin TCLK12 (shared between the two timer/counters). They can be configured as a 16 bit timer/counter with interrupt and a 16 bit period register.

TMR3 <16>: Timer3 is a 16 bit timer/counter consisting of two 8 bit sections TMR3H <8> and TMR3L <8>. It has a 16 bit period register (PR3H <8>, PR3L <8>), an interrupt and an external clock source (pin TCLK3) in counter mode.

8.1 ROLE OF THE TIMER/COUNTERS

The timer/counters are general purpose. However, they have special usage. RTCC is physically part of the 'core'. It is planned that future variations of the PIC17CXX family will include this timer. Therefore, time dependent code, e.g. real time operating system or clock/calender type software can be written using RTCC and ported to future PIC17CXX family members.

TMR3 is also used for 16 bit capture function as is described in capture section. Timers TMR1 and TMR2 can be used as time bases for PWM1 and PWM2 outputs respectively. Alternately, TMR1 can run both PWM outputs and thus free up TMR2 to be a general purpose timer.

These timers are not needed to do the following functions: Watchdog timer (it's a separate timer); Baud Rate generation for serial communication (serial port has its own 8 bit Baud Rate Generator).

8.2 RTCC MODULE

The RTCC (Real time clock/counter) module consists of a 16 bit timer/counter, RTCC (high byte RTCCH, file 0Ch and low byte RTCCL, file 0Bh), an 8 bit prescaler, and the RT pin as the source of external clock signal. The control bits for this module are in register RTCSTA (File 05h).

FIGURE 8.2.1.1: RTCC MODULE BLOCK DIAGRAM

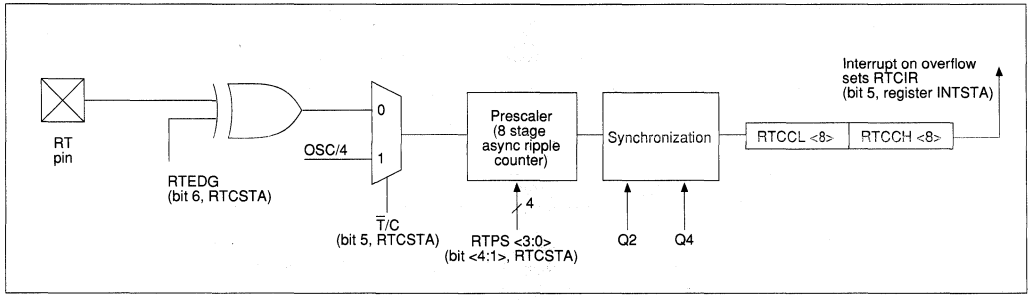
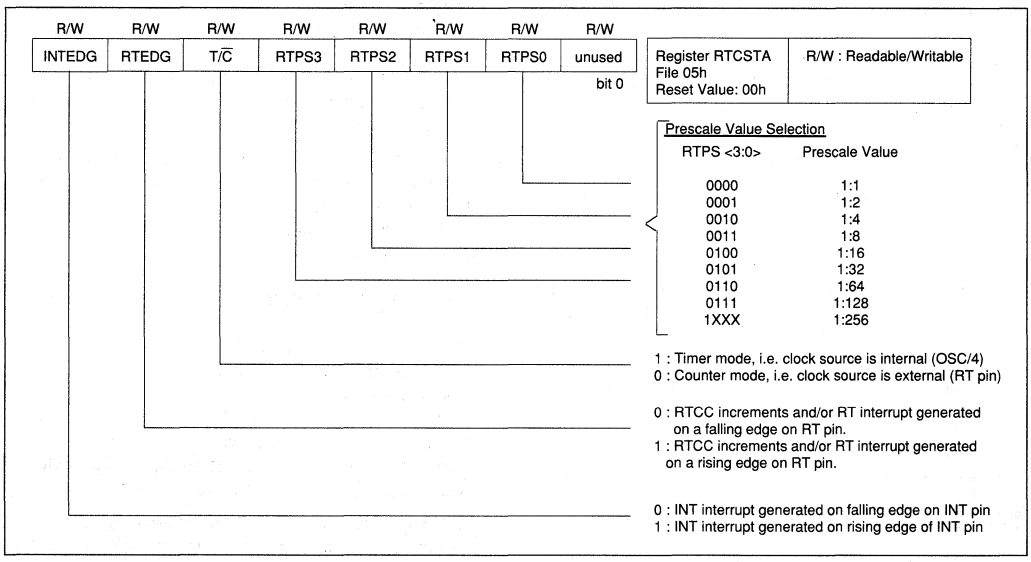


FIGURE 8.2.1.2: RTCSTA: RTCC STATUS/CONTROL REGISTER



8.2.1 RTCC Operation

RTCC increments either on internal clock, OSC/4 (if T/$\overline{C}$ = '1' in RTCSTA) or on external clock (counter mode) on RT pin (if bit T/$\overline{C}$ = '0' in RTCSTA). If external clock is chosen, increment can occur on either the rising edge (RTEDG = '1' is RTCSTA register) or the falling edge (RTEDG = '0' is RTCSTA register). The prescaler can be programmed to introduce a prescale of 1:1 to 1:256 in either timer or counter mode. The timers increment from 0000h to FFFFh and roll over to 0000h. On overflow, the RTCC interrupt request flag, RTCIR (bit 5, register INTSTA), is set. The RTCC interrupt can be masked off by clearing the corresponding interrupt mask bit, RTCIE (bit 1, INTSTA). The interrupt request flag, RTCIR, must be cleared in software.

8.2.2 Read/Write Consideration for RTCC

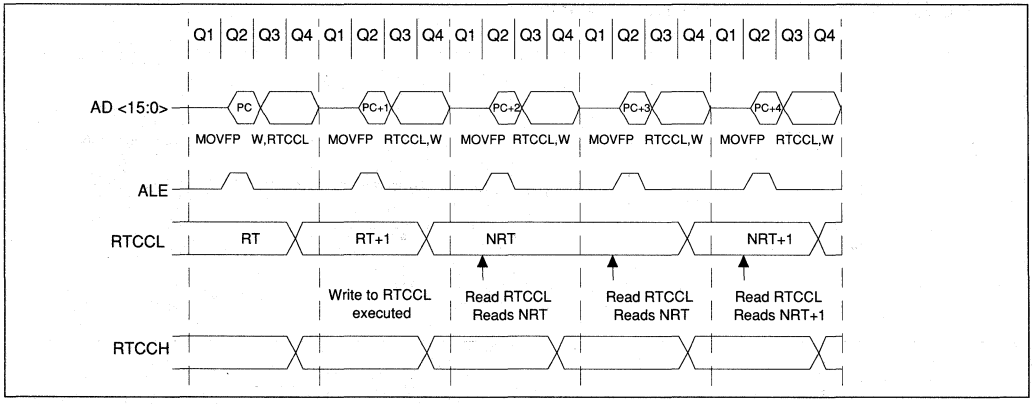
Although the RTCC is a 16 bit timer/counter, only 8 bits at a time can be read or written. This could create a problem unless care is taken.

Reading 16 bit value: One problem in reading the entire 16 bit value is that after reading the low (or high) byte it may change from FFh to 00h. This can be handled in software as follows:

```
movpf   rtccl, tmplo   ;read lo rtcc
movpf   rtcch, tmphi   ;read hi rtcc
movfp   tmplo, wreg    ;tmplo → wreg
cpfslt  rtccl, wreg    ;rtccl < wreg?
retfie                 ;no then return
movpf   rtccl, tmplo   ;read lo rtcc
movpf   rtcch, tmphi   ;read hi rtcc
retfie                 return
```

Interrupt must be disabled during this subroutine.

FIGURE 8.2.2.1: RTCC TIMING: WRITE HIGH OR LOW BYTE



Writing a 16 bit value to the RTCC: Since writing to either RTCCL or RTCCH will effectively inhibit increment of that half of the RTCC in the next cycle (following write), but not inhibit increment of the other half, the user must write to RTCCL first and RTCCH next in two consecutive instructions, as shown below:

```
BSF     CPUSTA, GLINTD      ; Disable interrupt
MOVFP   RAM_L, RTCCL        ;
MOVFP   RAM_H, RTCCH        ;
BCF     CPUSTA, GLINTD      ; Done, enable interrupt
```

Interrupt must be disabled. The user should note that a write to RTCCL or RTCCH will reset the prescaler.

8.2.3 External Clock Considerations

When the external clock input is used for RTCC, it is synchronized with the internal phase clocks. Therefore, the external clock input must meet certain requirements. Also, there is some delay from the occurrence of the external clock edge to the incrementing of RTCC. Referring to Figure 8.2.3.1, the synchronization is done after the prescaler. The output of the prescaler (PSOUT) is sampled twice in every instruction cycle to detect a rising or a falling edge. Therefore, it is necessary for PSOUT to be high for at least 2tosc or low for at least 2tosc where tosc= oscillator time period.

When no prescaler is used (i.e. prescale is 1:1) : PSOUT is the same as the RTCC clock input and therefore the requirements are:

T_{RTH} = RA1/RT high time ≥ 2tosc + 20 ns

T_{RTL} = RA1/RT low time ≥ 2 tosc + 20 ns

When prescaler is used: the RA1/RT input is divided by the asynchronous ripple counter-type prescaler and so the prescaler output is symmetrical. The requirements are then:

PSOUT high time = PSOUT low time = $\frac{N \cdot T_{RT}}{2}$

where T_{RT} = RA1/RT input period and

N = prescale value (2, 4, ..., 256).

Therefore $\frac{N \cdot T_{RT}}{2} \geq$ 2tosc + 20 ns, or $T_{RT} \geq \frac{4\,tosc + 40\,ns}{N}$

The user will notice that no requirement on RTCC high time or low time is specified. However, if the high time or low time on the RTCC input is too small then the pulse may not be detected, hence a minimum high or low time of 10 ns is required, In summary, the RTCC input requirements are:

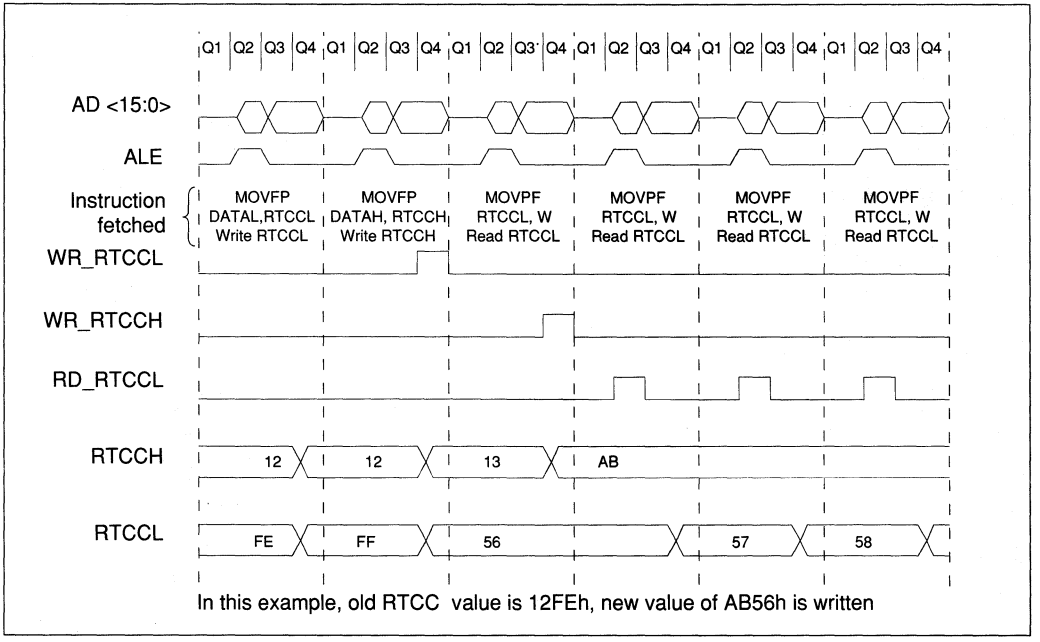
T_{RT} = RA1/RT period ≥ (4tosc + 40 ns)/N

T_{RTH} = RA1/RT high time ≥ 10 ns

T_{RTL} = RTCC low time ≥ 10 ns

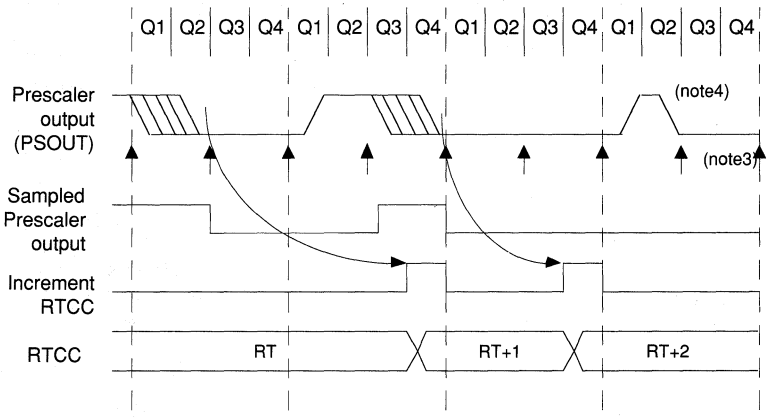
Delay from external clock edge: since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the RTCC is actually incremented. Referring to figure 8.2.3.1, the reader can see that this delay is between 3tosc and 7tosc. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within ± 4tosc (± 250 ns @16 MHz).

FIGURE 8.2.2.2: RTCC READ/WRITE IN TIMER MODE



In this example, old RTCC value is 12FEh, new value of AB56h is written

FIGURE 8.2.3.1: RTCC TIMING WITH EXTERNAL CLOCK



Note1: The RTCC increments on falling edges in this example
Note2: The delay from the RT edge to the RTCC increment is 3tosc-7tosc. Therefore, error in measuring the interval between two edges is ± 4tosc.
Note3: ↑ = PSOUT is sampled here.
Note4: The PSOUT high time is too small and is missed by the sampling circuit.

8.2.4 Summary of RTCC Registers

Register Name	Function	Address	Reset Value
RTCCL	RTCC Timer/Counter low byte	File 0Bh	XXXXXXXXb
RTCCH	RTCC Timer/Counter high byte	File 0Ch	XXXXXXXXb
RTCSTA	RTCC Status/Control	File 05h	00000000b
INTSTA	Interrupt Status Register	File 07h	00000000b
CPUSTA	CPU Status Register	File 06h	0011XX00b

8.3 TIMER1 & TIMER2

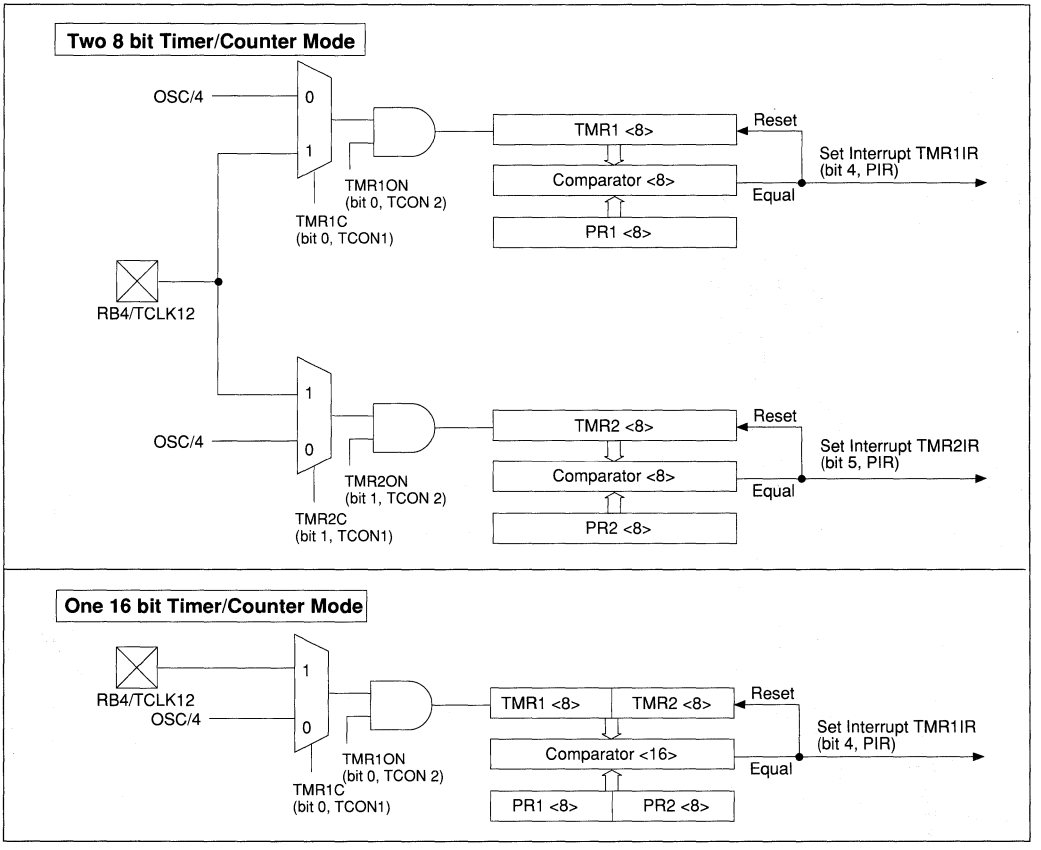
Timer 1 (TMR1, Bank 2, File 10h) and Timer 2 (TMR2, Bank 2, File 11h) are two 8 bit incrementing timer/counters, each with a period register (PR1, Bank 2, File 14h and PR2, Bank 2, File 15h respectively) and separate overflow interrupt. They can operate as timers (increment on internal OSC/4 clock) or as counters (increment on falling edge of external clock on pin TCLK12). They can operate as two 8 bit timer/counters or as a single 16 bit timer counter. TMR1 and TMR2 are also used as the time base for the PWM (pulse width modulation) module.

8.3.1 Timer1, Timer2 in 8 Bit Mode

8 bit mode is selected by setting 16/$\overline{8}$ (bit 3, register TCON1) to '0'. In this mode, TMR1 will be configured as a timer if control bit TMR1C (bit 0, register TCON1) is '0' and increment once every instruction cycle (OSC/4). Setting bit TMR1C = '1' will configure TMR1 as a counter. As a counter, TMR1 will increment on every negative edge on pin TCLK12. Since TCLK12 input is synchronized with internal phase clocks, it has to satisfy certain requirements. TCLK12 must be high for at least (0.5Tcy + 20)ns and low for at least (0.5Tcy + 20)ns where Tcy = 4tosc. TMR1 increments from 00h until it is equal to PR1 and then resets to 00h at the next increment cycle. An interrupt is generated when reset occurs which is latched in bit TM1IR (TMR1 Interrupt Request Flag, bit 4, PIR). This bit can be masked off by setting bit TM1IE (TMR1 Interrupt Enable) to '0'. In order for the TM1IR interrupt to be recognized, the Peripheral Interrupt Enable bit (PEIE, bit 3, register INTSTA) must be set to a '1' and the Global Interrupt Disable bit, GLINTD, must be '0'. TMR1 must be enabled by setting bit TMR1ON (bit 0, register TCON2) to a '1' and can be stopped any time by clearing bit TMR1ON to '0'. TMR1 and PR1 are both readable and writable registers.

TMR2, in 8 bit mode is identical in functionality as TMR1. The corresponding control bits for TMR2 are TMR2C (bit 1, TCON1), TM2IR (Timer 2 Interrupt-Request Flag, bit 5, PIR), TM2IE (Timer 2 Interrupt Enable Flag, bit 5, PIE) and TMR2ON (bit 1, TCON2). In counter mode, TMR2 also increments on falling edge on TCLK12 pin.

FIGURE 8.3.1.1: TIMER1/TIMER2 BLOCK DIAGRAM



8.3.2 Timer1 & Timer2 in 16 Bit Mode

16 bit mode is selected by setting bit 16/$\overline{8}$ (bit 3, register TCON1) to '1'. In this mode TMR1 and TMR2 concatenate to form one 16 bit timer/counter (TMR2 = high byte). Timer mode is selected by setting TMR1C (bit0, register TCON1) to '0' where it increments once every instruction cycle (OSC/4). Counter mode is selected if TMR1C bit = '1' and it increments on every negative edge on pin TCLK12. Input clock on TCLK12 must have a high time ≥ (0.5Tcy + 20)ns and a low time ≥ (0.5Tcy + 20)ns where Tcy = 4tosc. The 16 bit timer increments until it matches the 16 bit value in PR1, PR2 (PR2 = high byte) and then resets back to 0000h. An interrupt is generated at this time which is latched into the TM1IR bit (bit 4, PIR). In 16 bit mode, control bit TMR1C controls the entire 16 bit timer and bit TMR2C is a don't care. The TMR2ON bit must be always set to '1' in 16 bit mode. TMR1ON bit controls the entire 16-bit timer.

8.3.3 External Clock Input for Timer1, Timer2

When configured as a counter, TMR1 or TMR2 increments on the falling edge of clock input TCLK12. However, this input is sampled and synchronized by the internal phase clocks twice every instruction cycle. Therefore, the external clock must meet the following requirements:

TCLK12 high time ≥ 0.5 Tcy + 20 ns
TCLK12 low time ≥ 0.5 Tcy + 20 ns

There is a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. The delay is between 2tosc and 6tosc, where tosc = oscillator period. See Figure 8.3.3.1 for a timing diagram.

FIGURE 8.3.1.2: TMR1, TMR2, TMR3 TIMING IN TIMER MODE

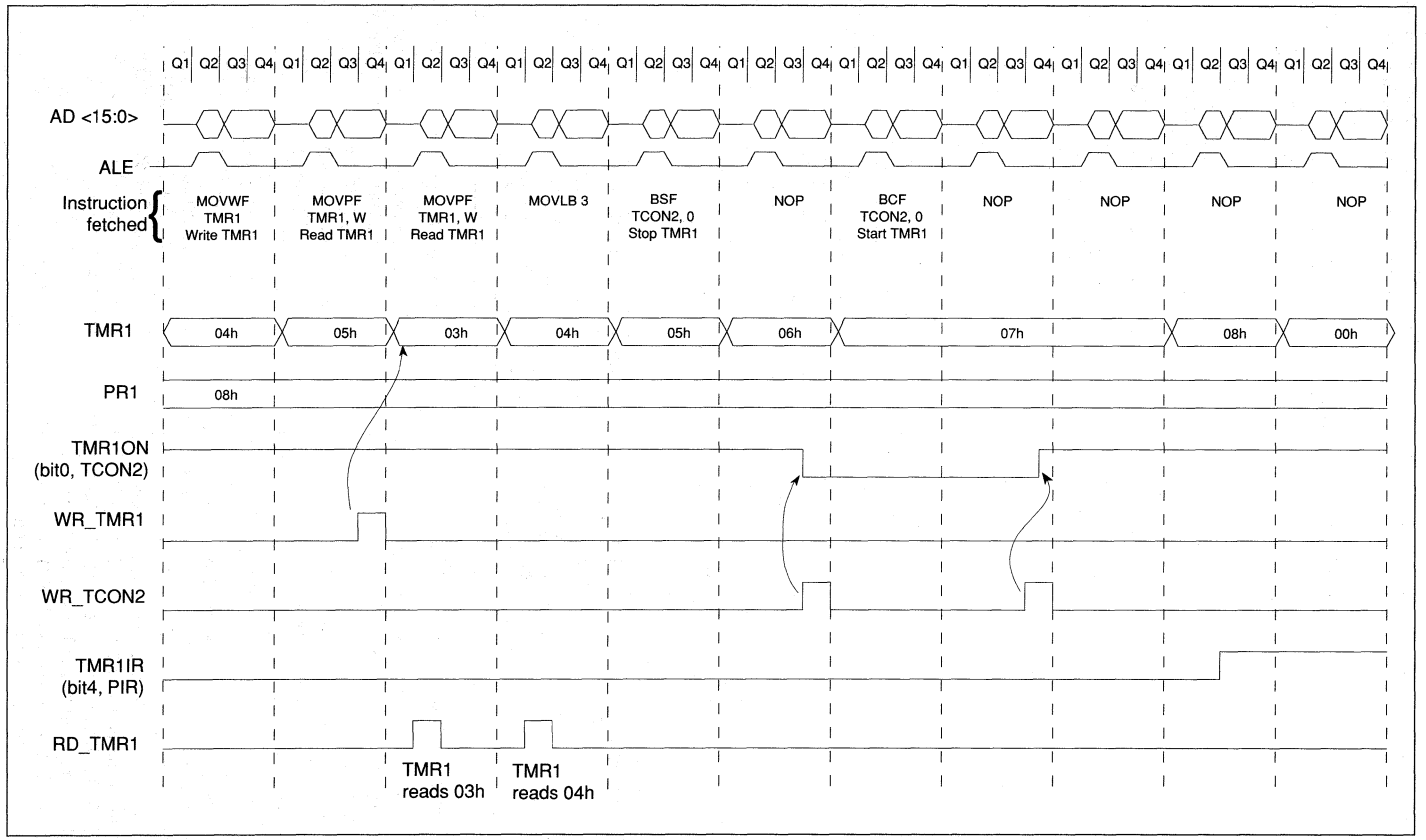


FIGURE 8.3.1.3: TIMER/CAPTURE/PWM CONTROL REGISTER 1 (TCON1)

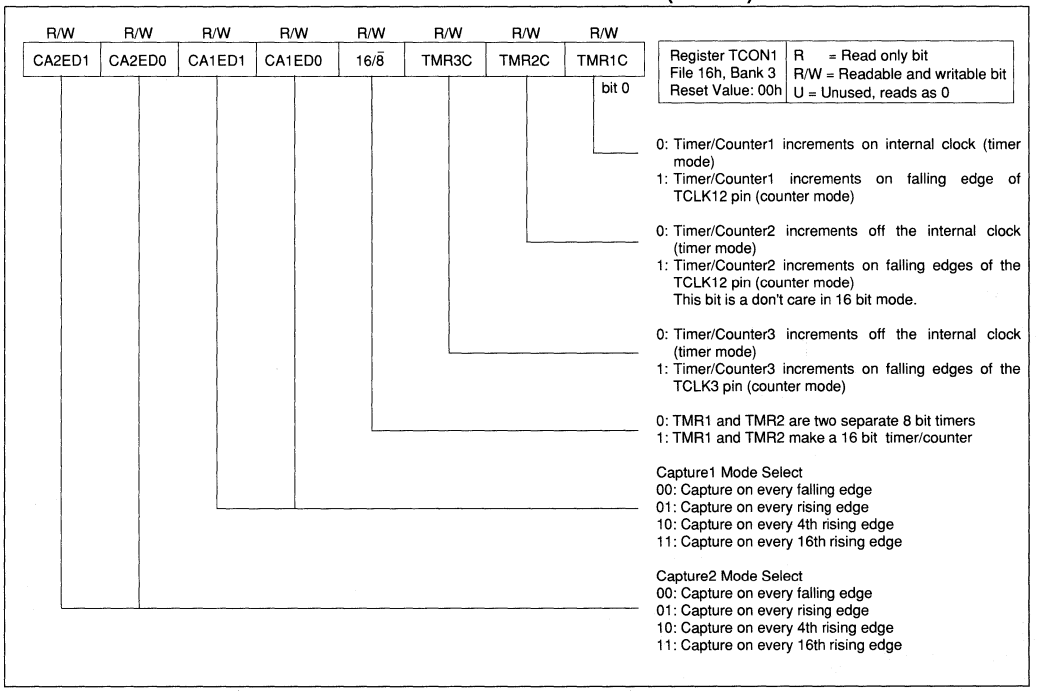
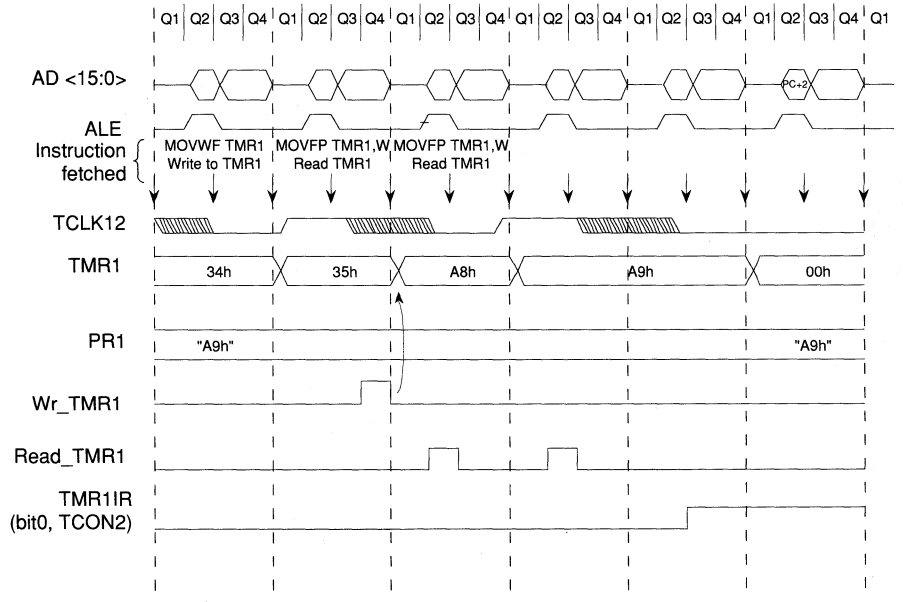
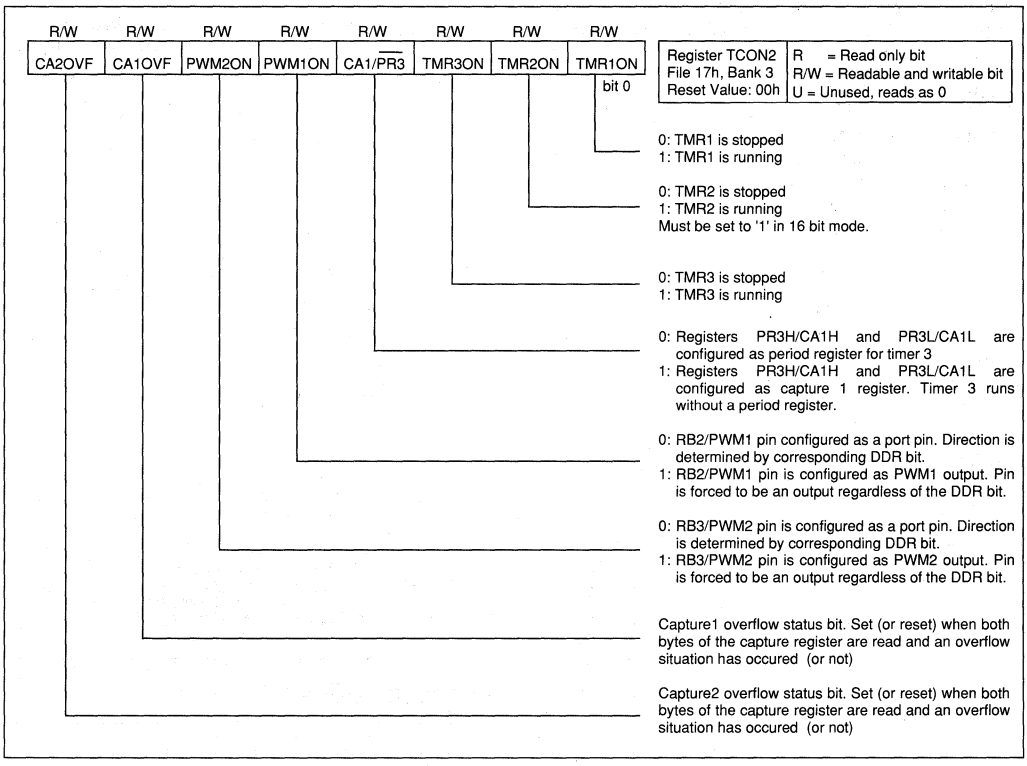


FIGURE 8.3.3.1: TMR1, TMR2 AND TMR3 IN EXTERNAL CLOCK MODE



Notes: TCLK12 is sampled in Q2 and Q4. ↓ indicates a sampling point.
The latency from TCLK12 ↓ to timer increment is between 2 tosc and 6 tosc.

FIGURE 8.3.3.2: TIMER/CAPTURE/PWM CONTROL REGISTER 2 (TCON2)



8.3.4 Summary of Timer1, Timer2 Registers

Register Name	Function	Address	Reset Value
TMR1	Timer/Counter1	Bank 2, File 10h	XXXXXXXXb
TMR2	Timer/Counter2	Bank 2, File 11h	XXXXXXXXb
PR1	Period Register1	Bank 2, File 14h	XXXXXXXXb
PR2	Period Register2	Bank 2, File 15h	XXXXXXXXb
TCON1	Timer Control Register1	Bank 3, File 16h	00000000b
TCON2	Timer Control Register2	Bank 3, File 17h	00000000b
PIR	Peripheral Interrupt Register	Bank 1, File 16h	00000010b
PIE	Peripheral Interrupt Enable	Bank 1, File 17h	00000000b
INTSTA (bit PEIE)	Interrupt Status Register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU Status Register	File 06h	0011XX00b

8.4 TIMER/COUNTER 3

TMR3 is a 16 bit timer/counter consisting of TMR3L (file 12, Bank 2) as the low byte of the timer and TMR3H (file 13, Bank 2) as the high byte of the timer. It has an associated 16 bit period register consisting of PR3L/CA1L (file 16, Bank 2), the low byte, and PR3H/CA1H (file 17, Bank 2), the high byte. Timer3 is a timer if TMR3C = 0 (bit 2, Register TCON1) in which case it increments every instruction cycle (OSC/4). If TMR3C = 1, the timer 3 acts as a counter and increments on every falling edge of TCLK3 pin input. In either mode, TMR3 increments if TMR3ON = 1 (bit 2, Register TCON2) and stops if TMR3ON = 0. TMR3 has two modes of operation: depending on bit CA1/$\overline{PR3}$ (bit 3, Register TCON2) the period register can be configured as a period or a capture register (Refer to section 9.0 for details on capture operation).

Period register mode, CA1/$\overline{PR3}$ = 0: In this mode registers PR3H/CA1H and PR3L/CA1L constitute a 16 bit period register. The timer increments until it equals the

period register and then resets to 0000h. Timer3 interrupt (TM3IR, bit 6, Register PIR) request flag is set at this point. This interrupt can be disabled by setting timer3 mask bit (TM3IE, bit 6, Register PIE) to '0'. TM3IR must be cleared in software.

Capture1 register mode, CA1/$\overline{PR3}$ = 1: In this mode the PR3H/CA1H and PR3L/CA1L constitute a 16 bit capture register. The timer operates without a period register and increments from 0000h to FFFFh and rolls over to 0000h. A timer3 interrupt (TM3IR, bit 6, Register PIR) is generated on overflow. The TM3IR interrupt flag must be cleared in software.

8.4.1 External Clock Input for Timer3

Timer3 increments on the falling edges of the clock input on TCLK3 pin. However, this input is sampled and synchronized by the internal phases, twice every instruction cycle. Therefore, the external clock input must meet the following requirements:

TCLK3 high time ≥ 0.5Tcy + 20 ns

TCLK3 low time ≥ 0.5Tcy + 20 ns

There is a delay from the time an edge occurs on TCLK3 to the time the timer3 is actually incremented. This delay is between 2 tosc and 6tosc, where tosc = oscillator period. See Figure 8.3.3.1 for a timing diagram.

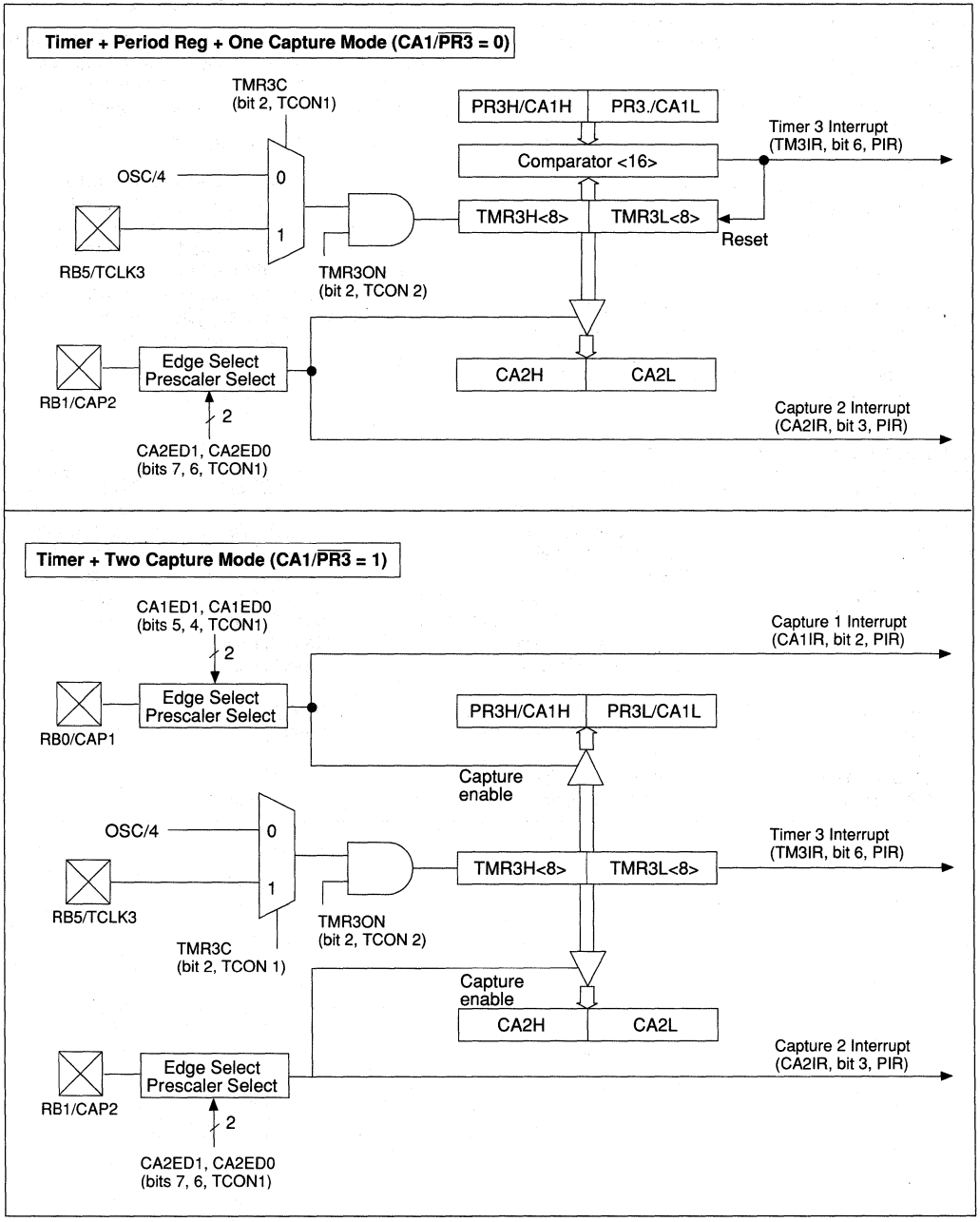
8.4.2 Reading/Writing Timer3

Since timer3 is a 16 bit timer and only 8 bits at a time can be read or written, the user should be careful about reading and writing when the timer is running. The safe and easy thing to do is to stop the timer, perform any read or write operation, and then restart timer3 (using the TMR3ON bit). If, however, it is necessary to keep timer3 free-running then certain suggested methods must be followed for reading and writing the timer. See section 8.2.3 for details.

8.4.3 Summary of Timer3 Registers

Register Name	Function	Address	Reset Value
TMR3L	Timer/Counter3 low byte	Bank 2, File 12h	XXXXXXXXb
TMR3H	Timer/Counter3 high byte	Bank 2, File 13h	XXXXXXXXb
CA2L	Capture2 low byte	Bank 3, File 14h	XXXXXXXXb
CA2H	Capture2 high byte	Bank 3, File 15h	XXXXXXXXb
PR3L/CA1L	Period Register3 low/capture 1 low	Bank 2, File 16h	XXXXXXXXb
PR3H/CA1H	Period Register3 high/capture 1 high	Bank 2, File 17h	XXXXXXXXb
TCON1	Timer Control Register1	Bank 3, File 16h	00000000b
TCON2	Timer Control Register2	Bank 3, File 17h	00000000b
PIR	Peripheral Interrupt Register	Bank 1, File 16h	00000010b
PIE	Peripheral Interrupt Enable	Bank 1, File 17h	00000000b
INTSTA (bit PEIE)	Interrupt Status Register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU Status Register	File 06h	0011XX00b

FIGURE 8.4.1.1: TIMER3/CAPTURE MODULE BLOCK DIAGRAM



9.0 CAPTURE MODULE

The PIC17C42 has two 16 bit capture registers that capture the 16-bit value of timer/counter3 (TMR3) when events are detected on capture pins. There are two capture pins (RB0/CAP1 and RB1/CAP2), one for each capture register. The capture pins are multiplexed with port B pins. An event can be a rising edge, a falling edge, 4 rising edges or 16 rising edges on the pin. Each capture register has an interrupt request flag associated with it which is set when a capture is made. The capture module is truly part of the timer/counter3/capture block. Refer to Figure 8.4.1.1 for a block diagram. The capture module can operate in one of two modes described below.

9.1 ONE CAPTURE + TIMER/ COUNTER3 + PERIOD REGISTER MODE

This mode is selected if control bit CA1/$\overline{PR3}$ = 0 (bit 3, register TCON2). In this mode, the capture1 register, consisting of high byte (PR3H/CA1H, File 17, Bank 2) and low byte (PR3L/CA1L, File 16, Bank 2), is configured as the period control register for TMR3. Capture1 is disabled in this mode, and the corresponding interrupt bit CA1IR (bit 2, PIR) is never set. Timer/counter3 increments until it equals the value in the period register and then resets to 0000h. See Section 8.4 for details of TMR3 operation in this mode.

Capture2 is active in this mode. Control bits CA2ED1 and CA2ED0 (bits 7 & 6, Register TCON1) determine the event on which capture will occur. CA2ED1, CA2ED0 = 00 enables capture on every falling edge, 01 = capture on every rising edge, 10 = capture every 4th rising edge and 11 = capture every 16th rising edge. When a capture takes place, an interrupt is latched into CA2IR (capture 2 interrupt flag, bit 3, PIR). This interrupt can be enabled by setting the corresponding mask bit CA2IE (bit 3, PIE) to '1'. Also, peripheral interrupt enable bit PEIE (bit 3, INSTA) must be a '1' and the Global Interrupt Disable bit (GLINTD, bit 4, CPUSTA), should be '0' for the interrupt to be acknowledged. The CA2IR interrupt flag needs to be cleared in software.

When the capture prescale select is changed, the prescaler is not reset. Therefore, the first capture after such a change will be ambiguous. It, however, sets the basis for the next capture. The prescaler is reset upon chip reset.

The capture pin RB1/CAP2 is a multiplexed pin. When used as a port pin, capture2 is not disabled. However, the user can simply disable the capture2 interrupt by setting CA2IE = '0'. If RB1/CAP2 is used as an output pin, some interesting possibilities arise. The user can activate a capture by writing to the port pin which may be useful during development phase to emulate a capture interrupt.

The input on capture pin, RB1/CAP2, is synchronized internally to internal phase clocks. This imposes certain restrictions on the input waveform. The minimum high time (T_{CPH}) and the minimum low time (T_{CPL}) on the capture input needs to be greater or equal to 10ns. The period (T_{CAP}) must be >2Tcy/N where N = prescale value (1, 4, 16) and where Tcy = one instruction cycle time (= 4tosc).

Capture2 Overflow

The overflow status flag bit is double buffered. The master bit is set to '1' if one captured word is already residing in the capture2 register and another 'event' has occurred on RB1/CA2 pin. The new event will not transfer the timer3 value to the capture register, protecting the previous unread capture value. When the user reads both the high and the low bytes (in any order) of the capture2 register, the master overflow bit is transferred to the slave overflow bit (CA2OVF, bit 7, TCON2) and then the master bit is reset. The user can then read TCON2 to determine the value of CA2OVF.

The recommended sequence to read capture registers and overflow is as follows:

```
MOVLB   3                   ; Select Bank 3
MOVPF   CA2L, LO_BYTE       ; Read capture2 low byte,
                            ; store in LO_BYTE
MOVPF   CA2H, HI_BYTE       ; Read capture2 high byte,
                            ; store in HI_BYTE
MOVPF   TCON2, STAT_VAL     ; Read TCON2 into file
                            ; STAT_VAL
```

9.2 TWO CAPTURE + TIMER/ COUNTER3 MODE

This mode is selected by setting CA1/$\overline{PR3}$ = 1 (bit 3, register TCON2). In this mode the timer (TMR3) runs without a period register and increments from 0000h to FFFFh and rolls over to 0000h. For details on TMR3 operation see section 8.4 Registers PR3H/CA1H (file 17h, Bank 2) and PR2L/CA1L (file 16h, Bank 2) make a 16 bit capture register (Capture1). It captures events on pin RB0/CAP1. Capture mode is set by control bits CA1ED1 and CA1ED0 (bit 5 & 4, Register TCON1). A capture1 interrupt is latched into the CA1IR (bit 2, PIR). The corresponding interrupt mask bit is CA1IE (bit 2, PIE). The capture1 overflow status bit is CA1OVF (bit 6, TCON2). Otherwise, capture1 operates identically to capture2. Capture2 operation is same as in the previous mode.

9.3 SUMMARY OF CAPTURE REGISTERS

Register Name	Function	Address	Reset Value
PR3L/CA1L	Period Register 3 low/capture 1 low	Bank 2, File 16h	XXXXXXXXb
PR3H/CA1H	Period Register 3 high/capture 1 low	Bank 2, File 17h	XXXXXXXXb
CA2L	Capture2 register low	Bank 3, File 14h	XXXXXXXXb
CA2H	Capture2 register high	Bank 3, File 15h	XXXXXXXXb
TMR3L	Timer/Counter 3 low	Bank 2, File 12h	XXXXXXXXb
TMR3H	Timer/Counter 3 high	Bank 2, File 13h	XXXXXXXXb
TCON1	Timer Control Register 1	Bank 3, File 16h	00000000b
TCON2	Timer Control Register 2	Bank 3, File 17h	00000000b
PIR	Peripheral Interrupt Register	Bank 1, File 16h	00000010b
PIE	Peripheral Interrupt Enable	Bank 1, File17h	00000000b
INTSTA (bit PEIE)	Interrupt Status Register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU Status Register	File 06h	0011XX00b

10.0 PULSE WIDTH MODULATION (PWM) OUTPUTS

The PIC17C42 provides two high speed pulse-width modulation outputs on pins RB2/PWM1 and RB3/PWM2. Each PWM output has a maximum resolution of 10 bits. At 10 bit resolution, the PWM output frequency is 15.6 KHz (@ 16 MHz clock) and at 8 bit resolution the PWM output frequency is 62.5 KHz.

The user needs to set the PWM1ON control bit (bit 4, register TCON2) to enable the PWM1 output. Once the PWM1ON bit = '1', the RB2/PWM1 pin is configured as PWM1 output and forced as an output irrespective of the data direction bit. If PWM1ON = '0', then the pin behaves as a port pin and its direction is controlled by its data direction bit (bit2, DDRB). Similarly, the PWM2ON bit controls the configuration of the RB3/PWM2 pin.

The period of the PWM1 output is determined by timer1 (TMR1) and its period register (PR1). The period of the PWM2 output is determined by timer1 if control bit TM2PW2 = '0' (bit 5, register PW2DCL) or by timer2 if TM2PW2 = '1'.

Thus the PWM periods are:

t_{PWM1P} = period of PWM1 = [(PR1) + 1] x 4 tosc

t_{PWM2P} = period of PWM2 = [(PR1) + 1] x 4 tosc

or [(PR2) + 1] x 4 tosc

The duty cycle of PWM1 is determined by the 10 bit value DC1<9:0>. The upper 8 bits are from register PW1DCH (file 12, Bank 3) and the lower 2 bits are in register PW1DCL<1:0> (file 10, Bank 3). The PWM1 high time is as follows:

t_{PWM1H} = PWM1 high time = (DC1) x tosc

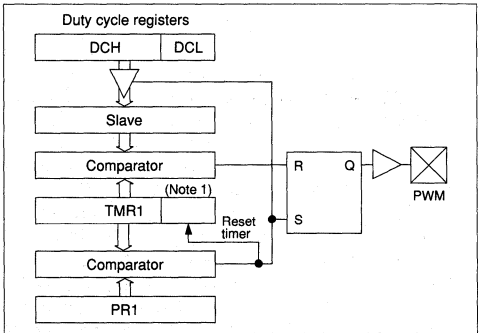
where DC1 represents the 10 bit value from PW1DCH, PW1DCL concatenated.

If DC1 = 0, then the duty cycle is zero. If t_{PWM1H} is equal to or higher than t_{PWM1P} then the duty cycle is 100%.

Similarly, PWM2 high time, t_{PWM2H} = (DC2) x tosc.

The duty cycle registers for both PWM outputs are double buffered. When the user writes to these registers they are stored in master latches. When TMR1 (or TMR2) overflows, and a new PWM period begins the master latch values are transferred to the slave latches.

FIGURE 10.0.1 - SIMPLIFIED PWM BLOCK DIAGRAM



Notes: 1. 8-bit timer is concatenated with 2-bit internal Q clock time to create 10-bit time base.
2. Timer1 is used in this example.

Using external clock for PWM will also cause jitter in the 'duty cycle' as well as the 'period' of the PWM output. This is because external TCLK12 input is synchronized internally (sampled once per instruction cycle). Therefore, from the time TCLK12 changes to the time timer increments will vary by as much as Tcy (one instruction cycle). Therefore, both the high time and the period of the PWM output will have a jitter of ±Tcy, unless the external clock is in sync with the processor clock. The latter is the case when TCLK12 input itself is generated by the PIC17C42 (e.g. one PWM output is feedback as TCLK12).

In general therefore, when using external clock reference for PWM, its frequency should be much smaller compared to fosc.

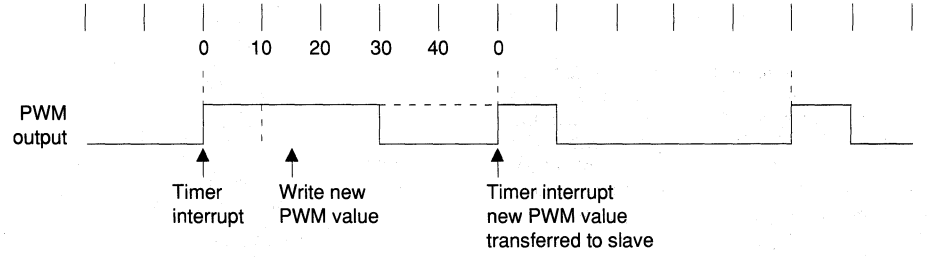
PWM interrupts: The PWM module makes use of timer1 or timer2 interrupts. A timer interrupt is generated when TMR1 or TMR2 equals its period register and is reset to zero. This interrupt, also marks the beginning of a PWM cycle. The user can write new duty cycle values before the next interrupt. The timer1 interrupt is latched into the TM1IR bit (bit4, PIR) and the timer2 interrupt is latched into the TM2IR bit (bit 5, PIR). These flags need to be cleared in software.

Using External clock: Timer1 or timer2, when used as the PWM time base, may be run off external clock only if the PWM output is being generated with 8 bit resolution or less. In this case, the PW1DCL and the PW2DCL registers must be kept at '0'. Any other value will distort the PWM output. Internal clock can be used for all resolutions. The user should also note that the maximum attainable frequency is lower. Since the maximum possible external clock input frequency for a timer is 1/(Tc + 40) ns, (see AC specs) the PWM frequency at 8 bit resolution can be, at most, 13.47 KHz (@ 16 MHz osc clock).

Timer selection for PWM2: While PWM1 always runs based on TMR1, PWM2 can run off timer1 (if bit TM2PW2 = 0, bit 5, Register PW2DCL) or timer2 (if TM2PW2 = 1). Running two different PWM outputs on two different timers allow different PWM period.

Running both PWMs off timer1 allows the best utilization of resources. If frees timer2 to operate as an 8 bit timer/counter. Timer1 and timer2 can not be used as a 16 bit timer if either PWM is being used.

FIGURE 10.0.2 - PWM OUTPUT



Notes: 1. The dotted line shows PWM output if duty cycle registers are not double buffered. If the new duty cycle value is written after the timer has passed that value, then the PWM does not reset at all during the current cycle causing a "glitch".

2. In this example, PWM period = 50. Old duty cycle value is 30. New duty cycle value is 10.

Figure 10.0.1 shows a simplified block diagram of the PWM module. The duty cycle register is double buffered for a glitch free operation. Figure 10.0.2 shows how a glitch could occur if duty cycle registers are not double buffered.

Operating on duty cycle registers: For PW1DCH, PW1DCL, PW2DCH and PW2DCL registers, a write operation writes to the "master latches" while a read operation reads the "slave latches". As a result, the user may not read back what was just written to the duty cycle registers.

The user should also avoid any "read-modify-write" operations on these registers, such as: ADDWF PW1DCH, may not work as intended.

10.1 SUMMARY OF PWM REGISTERS

Register Name	Function	Address	Reset Value
TMR1	Timer/Counter 1	Bank 2, File 10h	xxxxxxxxb
TMR2	Timer/Counter 2	Bank 2, File 11h	xxxxxxxxb
PR1	Period Register 1	Bank 2, File 14h	xxxxxxxxb
PR2	Period Register 2	Bank 2, File 15h	xxxxxxxxb
TCON1	Timer/Capture/PWM Control Register 1	Bank 3, File 16h	00000000b
TCON2	Timer/Capture/PWM Control Register 2	Bank 3, File 17h	00000000b
PW1DCL	PWM1 duty cycle, lower 2 bits	Bank 3, File 10h	xx000000b
PW1DCH	PWM1 duty cycle, upper 8 bits	Bank 3, File 12h	xxxxxxxxb
PW2DCL	PWM2 duty cycle, lower 2 bits	Bank 3, File 11h	xx000000b
PW2DCH	PWM2 duty cycle, upper 8 bits	Bank 3, File 13h	xxxxxxxxb
PIR	Peripheral Interrupt Register	Bank 1, File 16h	00000010b
PIE	Peripheral Interrupt Enable	Bank 1, File 17h	00000000b
INTSTA (bit PEIE)	Interrupt Status Register	File 07h	00000000b
CPUSTA (bit GLINTD)	CPU Status Register	File 06h	0011xx00b

11.0 DEVELOPMENT SUPPORT

The PIC17C42 is supported with a full range of development tools as well as several support programs. These tools and support programs help the user design the PIC17C42 into his or her system easily and quickly. The user can take advantage of the variety of tools from evaluation stage to complex design debug phase. Time to market is significantly reduced by the easy-to-use, PC based tools. All the available and planned tools and programs are described in this section.

11.1 PICASM-17 : PIC17C42 CROSS ASSEMBLER:

The PICASM-17 is a powerful two pass relocatable assembler with advanced MACRO capabilities, high level construct support and source line debug support. It runs on any PC compatible platform. A host of assembler directives support conditional assembly, data area definition and initialization, outputting customized error messages, formatting listing file etc. Advanced MACRO processing capabilities include nesting of macros, conditional macro expansion and parameterized macros. High level constructs such as WHILE and IF-THEN-ELSE permit readable and efficient code writing. ANSI-C style expressions and #define support further makes the assembler more like a high level language.

11.2 PICPAK-17™ : PIC17C42 EVALUATION/DEVELOPMENT/ PROGRAMMER KIT

The PICPAK-17 is a very low cost development kit containing an Evaluation/Development/Programmer PCB, PC-based assembler, and documentation. The EDP board operates in one of three modes:

a) Programmer mode: In this mode the PIC17C42 programs itself from two external 27C64 EPROMs. The user simply programs the EPROMs with the desired code using any standard EPROM programmer.

b) External execution mode: In this mode the PIC17C42 executes out of two external 8K x 8 EPROMs or SRAMs. The user may also plug in a ROM emulator instead of using EPROMs.

c) Internal execution mode: In this mode the PIC17C42 executes from its own internal memory. The external memories are disconnected.

The development board has a solder-less bread-board area with most PIC17C42 signals brought out for easy prototyping and evaluation. Only a single 5V supply is required for the board. Additionally, there is a PIC16C57 microcontroller, which primarily controls the mode selection but is also capable of providing complex stimuli to the PIC17C42 such as stream of capture, timer clock or interrupt pulses, asynchronous data stream or synchronous data stream. Various stimuli are easily selected through DIP switch settings.

11.3 PRO MASTER™ PROGRAMMER

The PRO MASTER programmer is a production quality programmer capable of operating in stand alone mode as well as PC-hosted mode.

The PRO MASTER has programmable VDD and VPP supplies which allows it to verify the PIC at VDD min and VDD max for maximum reliability . It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand alone mode the PRO MASTER can read, verify or program a part. It can also set fuse configuration and code-protect in this mode. It's EEPROM memory holds data and parametric information even when powered down. It is ideal for duplicating a large number PIC17C42 for production.

In PC-hosted mode, the PRO MASTER connects to the PC via one of the COM (RS232) ports. PC based user-interface software makes using the programmer simple and efficient. The user interface is full-screen and menu-based. Full screen display and editing of data, easy selection of fuse configuration and part type, easy selection of VDD min, VDD max and VPP levels, load and store to and from disk files (intel hex format) are some of the features of the software. Essential commands such as read, verify, program, blank check can be issued from the screen. Additionally, serial programming support is possible where each part is programmed with a different

11.4 PICMASTER™-17: HIGH PERFORMANCE UNIVERSAL IN-CIRCUIT EMULATOR SYSTEM

The PICMASTER Universal In-Circuit Emulator System is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X and PIC17CXX families. This system currently supports the PIC16C54, PIC16C55, PIC16C56, PIC16C57 and PIC17C42 processors.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new PIC16CXX and PIC17CXX microcontrollers.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.1 environment, allowing the operator access to a wide range of supporting software and accessories.

Provided with the PICMASTER System is a high performance real-time In-Circuit Emulator, a microcontroller EPROM programmer unit, a macro assembler program, and a simulator program. Sample programs are provided to help quickly familiarize the user with the development system and the PIC microcontroller line.

Coupled with the user's choice of text editor, the system is ready for development of products containing any of Microchip's microcontroller products.

A "Quick Start" PIC Product Sample Pak containing user programmable parts is included for additional convenience.

Microchip provides additional customer support to developers through an electronic Bulletin Board System (EBBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS system.

11.4.1 Host System Requirements:

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.1 environment was chosen to best make these features available to you the end user. To properly take advantages of these features, PICMASTER requires installation on a system having the following minimum configuration:

- PC AT compatible machine: 80286, 386SX, 386DX, or 80486 with ISA or EISA Bus.
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended).
- MSDOS / PCDOS version 3.1 or greater.
- Microsoft Windows® version 3.0 or greater operating in either standard or 386 enhanced mode).
- 1 Mbyte RAM (2 Mbytes recommended).
- One 5.25" floppy disk drive.
- Approximately 10 Mbytes of hard disk (1 Mbyte required for PICMASTER, remainder for Windows 3.0 system).
- One 8-bit PC AT (ISA) I/O expansion slot (half size)
- Microsoft® mouse or compatible (highly recommended).

11.4.2 Emulator System Components:

The PICMASTER Emulator Universal System consists primarily of 4 major components:

- **Host-Interface Card:** The PC Host Interface Card connects the emulator system to an IBM PC compatible system. This high-speed parallel interface requires a single half-size standard AT / ISA slot in the host system. A 37-conductor cable connects the interface card to the external Emulator Control Pod.
- **Emulator Control Pod:** The Emulator Control Pod contains all emulation and control logic common to all microcontroller devices. Emulation memory, trace memory, event and cycle timers, and trace/breakpoint logic are contained here. The Pod controls and interfaces to an interchangeable target-specific emulator probe via a 14" precision ribbon cable.
- **Target-specific Emulator Probe:** A probe specific to microcontroller family to be emulated is installed on the ribbon cable coming from the control pod. This probe configures the universal system for emulation of a specific microcontroller. Currently, the 16C5x family, and the new PIC17C42 microcontrollers are supported. Future microcontroller probes will be available as they are released.

- **PC Host Emulation Control Software:** Host software necessary to control and provide a working user interface is the last major component of the system. The emulation software runs in the Windows 3.0 environment, and provides the user with full display, alter, and control of the system under emulation. The Control Software is also universal to all microcontroller families.
  The Windows 3.1 System is a multitasking operating system which will allows the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.1, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.
Under Windows 3.1, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16C5x processor and a PIC17Cxx processor).

FIGURE 11.4.1: PICMASTER-17 DEVELOPMENT SYSTEM

FIGURE 11.4.2: PICMASTER-17 DEVELOPMENT SYSTEM BLOCK DIAGRAM

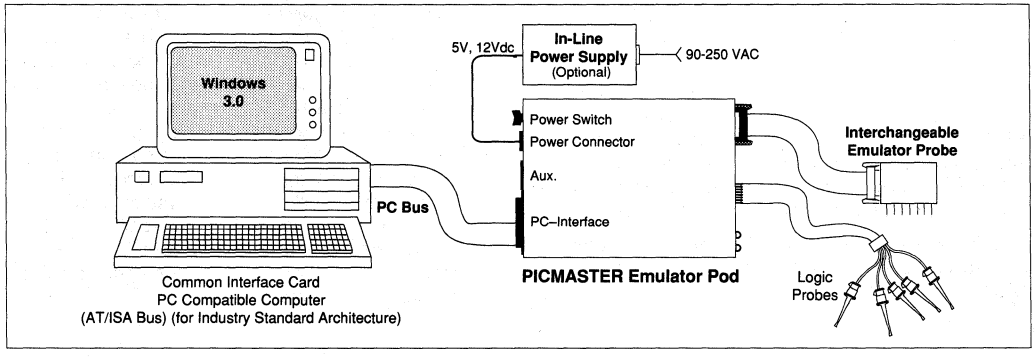
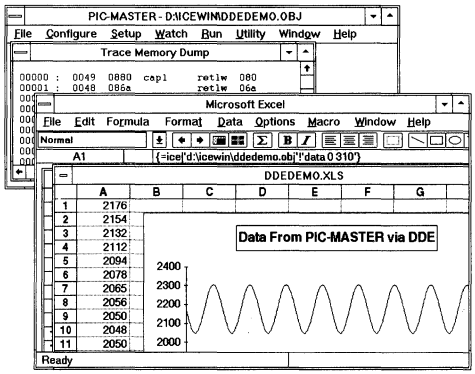


FIGURE 11.4.3: SAMPLE SCREEN LAYOUT FOR PICMASTER-17



11.5 ORDERING DEVELOPMENT TOOLS

The development tools are packaged as comprehensive systems for your convenience. Their description and planned availability dates are as follows:

System	Description	Available
PICPAK-17	Includes: PICASM-17 PIC EDP-17 manuals	Now
PICMASTER-17	Includes: PICASM-17 PRO MASTER PICMASTER PIC17C42 personality module manuals	Now
PRO MASTER™	Includes: PRO MASTER programmer DIP socket module manuals	Now

11.6 APPLICATION AND TECHNICAL SUPPORT

Microchip Technology has a number of sales offices in U.S., Europe, and Asia with highly trained Field Applications Engineers to give you prompt, hands on technical support. Please refer to the back cover page for the sales office and its number nearest to you. In addition, factory technical staff will be glad to help you over the phone (602-963-7373, Chandler, AZ, U.S.A). Application notes and software routines are being made available to give you a jump-start in your system development. These are usually available in printed as well as electronic format.

11.7 PROGRAMMING SUPPORT

The OTP microcontroller provides excellent time-to-market. It offers quick development, over-night code changes and easy to manage inventory. To support your programming needs Microchip offers various options.

11.7.1 Prototype Programming

Prototype programming can be done either using the low cost PICPAK-17 board or the PRO MASTER production quality programmer.

11.7.2 Production Volume Programming

High volume programming for production can be done using the PRO MASTER programmer. Microchip is working with industry leading programming companies to support the PIC17C42 on their programmers. Our low end 8-bit microcontroller family, the PIC16CXX, is now supported by DATA I/O, Logical Devices, BP Microsystems, Baradine and Stag most of which support handlers. Microchip is working to develop a similar level of support for the PIC17CXX family of products.

11.7.3 Factory Programming

High volume factory programming (QTP) is an available service from Microchip Technology. A small price adder and a minimum quantity requirement apply.

11.7.4 Distributor Programming Support

Some of our distributors will support your programming needs. Please contact your distributor for price and volume requirements.

12.0 ELECTRICAL CHARACTERISTICS

12.1 ABSOLUTE MAXIMUM RATINGS

Maximum temperatures

Ambient temperature under bias ..... –55°C to 125°C
Storage temperature ..... –65°C to 150°C

Maximum voltages

V_{DD} to V_{SS} ..... 0V to +7.5V
$\overline{MCLR}$ to V_{SS} ..... –0.6V to 12V
RA2 and RA3 to V_{SS} ..... –0.6V to 12V
Any pin with respect to V_{SS} ..... –0.6V to V_{DD} +0.6V (except V_{DD}, $\overline{MCLR}$, RA2, RA3)

Maximum currents

Into V_{DD} pin(s) total ..... 150 mA
Out of all V_{SS} pins total ..... 150 mA
Into any pin when configured as output (except RA2, RA3) ..... 35 mA

Into RA2, RA3 when configured as output ..... 60 mA
Out of any pin when configured as output ..... 20 mA
Into any pin when configured as input ..... ±500 µA

Maximum power dissipation

Total power dissipation 1W

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. **This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied.** Exposure to maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Total power dissipation should not exceed 1 W for the package. Power dissipation is calculated as follows:

   $Pdis = V_{DD} \times \{I_{DD} - \Sigma\ Ioh\} + \Sigma\ \{(V_{DD}-Voh) \times Ioh\} + \Sigma(Vol \times Iol)$

2. Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

12.2 DC CHARACTERISTICS

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Conditions
Supply voltages and currents						
Supply Voltage	VDD	4.5	5.0	5.5	V	
Supply Current (note 1)	IDD1	-	3	6	mA	VDD=5.5V,freq=4MHz
	IDD2	-	95	-	uA	VDD=4.5V,freq=32KHz
	IDD3	-	6	12	mA	VDD=5.5V,freq=8MHz
	IDD4	-	11	24	mA	VDD=5.5V,freq=16MHz
Standby current (notes 2,3)	IDDS1	-	30	50	uA	VDD=4.5V,WDT on
	IDDS2	-	60	100	uA	VDD=5.5V,WDT on
	IDDS3	-	15	25	uA	VDD=4.5V, WDT off
	IDDS4	-	30	50	µA	VDD=5.5V,WDT off
Programming voltage	VPP	11.5	11.75	12.0	V	
Input voltage levels & hysterisis						
All inputs except C, D and E	Vil1	-	-	0.2 VDD	V	
ports (Schmitt trigger inputs)	Vih1	0.8 VDD	-	-	V	
including OSC1 (EC, RC modes)	Vhys1	0.15 VDD*	-	-	V	
Ports C, D and E (TTL input)	Vil2	-	-	0.8	V	
	Vih2	2.0	-	-	V	
OSC1 (XT, LF modes)	Vil3	-	-	0.2VDD		
	Vih3	0.8 VDD	-	-		
Input leakage current						
All pins except MCLR,RA2,RA3	Iil1	-	-	±1	uA	VSS ≤ VPIN ≤VDD (note 4)
MCLR pin	Iil2	-	-	±2	uA	VSS≤VMCLR≤VDD
RA2,RA3 pin	Iil3	-	-	±2	uA	VSS ≤ VRA2, VRA3≤12V
MCLR pin	Iil4	-	-	10	uA	VMCLR = VPP(note 5)
Pin capacitance						
All pins except MCLR, VDD, VSS	Cin	-	10*	-	pF	
MCLR	Cmclr	-	20*	-	pF	
Output voltage levels						
RA2,RA3 (open collector)	Voh1	-	-	12.0	V	(note 6)
	Vol1	-	-	3.0	V	Iol1= 60 mA, VDD = 5.5V
PORT C, D & E (TTL)	Voh2	2.4	-	-	V	Ioh2 = -6 mA, VDD = 4.5V
	Vol2	-	-	0.4	V	Iol2 = 6 mA, VDD = 4.5V
OSC2/CLKOUT (RC & EC modes)	Voh3	2.4	-	-	V	Ioh3 = -5 mA, VDD = 4.5V
	Vol3	-	-	0.4	V	Iol3 = 3 mA, VDD = 4.5V
All Outputs except OSC2	Voh4	0.9 VDD	-	-	V	Ioh4 = -2 mA
(including C, D and E ports)	Vol4	-	-	0.1 VDD	V	Iol4 = 4 mA
Weak pull-up current (PortB)	Ipu	60	100	250	uA	Pull-up active, VPIN = VSS
RAM retention voltage	Vram	1.5*	-	-	V	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
*: Guaranteed by characterization and not tested.
**: Guaranteed by Design.

NOTE 1: Supply current is measured with PIC17C42 executing code (from internal test EPROM which is same as microcomputer mode) with all port pins configured as input and forced to VDD or VSS. External clock (rail to rail) is used. The user should note the following:
a) The code executed from test memory attempts to exercise the chip to make more realistic measurements of IDD (rather than in reset). However, depending on user's code, the current will vary.
b) The user needs to add the current consumed by output drivers driving external capacitive or resistive load. For capacitive loads, this can be estimated for an individual output pin as: (C_L·VDD) f where C_L = total capacitive load, f = average frequency with which the pin switches.

The current due to external capacitance load switching is most significant during external execution.

c) The current consumed by the oscillator circuit needs to be considered as well. This will be especially significant for RC oscillator, where the current through the external pull up resistor can be estimated as: VDD/(2·R)

NOTE 2: Standby current is measured under the following conditions: Part in SLEEP, $\overline{MCLR}$ = VDD. OSC1 and OSC2 pins driven or left floating (makes no difference). All port pins configured as input and tied to VSS or VDD. Standby current is not affected by oscillator type.

NOTE 3: WDT off implies fuses FWDT1 = FWDT0 = 0 which configures the WDT as a normal timer that shuts off during SLEEP. WDT on implies that the WDT is configured as a watchdog timer (FWDT1, FWDT0 = 01, 10 or 11) which continues to run during SLEEP.

NOTE 4: With any weak pull-up disabled.

NOTE 5: When not programming

NOTE 6: RA2 and RA3 are open collector outputs that will pull-up to externally applied voltage (through resistor pull-ups). Maximum allowable VOH = 12V.

12.3 AC CHARACTERISTICS

12.3.1 AC Characteristics: OSC/Reset/System bus

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
Input clock and oscillator frequencies						
Oscillator frequency	Fosclf	DC	-	200	KHz	LF osc mode
	Foscxt	0.2	-	16	MHz	XT osc mode
RC mode frequency	Foscrc	DC	-	4	MHz	RC osc mode
Recommended limits:	R	2	-	50	Kohm	
	C	20	-	1000	pF	
External clock in frequency	Fextck	DC	-	16	MHz	EC mode (external clock)
Instruction cycle time	Tcy	-	4/Fosc	-	ns	Fosc = osc/clock-in frequency
Clock-in (OSC1) high or low time	TckHL	15*			ns	For external clock input in XT, LF or EC mode.
Clock-in (OSC1) rise or fall time	TckRF			15*	ns	For external clock input in XT, LF or EC mode.
Reset timing						
$\overline{MCLR}$ pulse width	tmcL	100*	-	-	ns	
$\overline{MCLR}$ ↓ to AD<15:0> high impedance	tmcL2adZ	-	-	50*	ns	
WDT, OST, PWRT and POR timings						
WDT period	twdt	-	20*	-	ms	Prescale = 1
Power up timer period	tPWRT	-	80*	-	ms	
Oscillator start-up timer (OST) period	tOST	-	1024 tOSC**	-	ns	tOSC = oscillator period
VDD rise time for POR to function properly	tVDDR	-	-	80*	ms	Time for VDD to rise from 0V to 4.5V (Note 1)
VDD start voltage to guarantee power on reset	VPOR	-	Vss*	-	V	See section 4.4 for details
System bus timings						
Address out valid to ALE ↓ (address setup time)	tadV2alL	0.25 Tcy-30	-	-	ns	with 100 pF load on all address/data and control (ALE,$\overline{OE}$,$\overline{WR}$) pins.
ALE ↓ to address out invalid (address hold time)	talL2adI	5	-	-	ns	
AD <15:0> high impedance to $\overline{OE}$↓	tadZ2oeL	0	-	-	ns	
$\overline{OE}$↑ to AD<15:0> driven	toeH2adD	0.25 Tcy-15	-	-	ns	
Data in valid before $\overline{OE}$↑ (data setup time)	tadV2oeH	30	-	-	ns	
$\overline{OE}$↑ to data in invalid (data hold time)	toeH2adI	0	-	-	ns	
Data out valid to $\overline{WR}$↓ (data setup time)	tadV2wrL	0.25 Tcy-40	-	-	ns	
$\overline{WR}$↑ to data out invalid (data hold time)	twrH2adI	5	-	-	ns	
ALE pulse width	talH	-	0.25 Tcy**	-	ns	
OE pulse width	toeL	0.5 Tcy-25**	-	-	ns	
$\overline{WR}$ pulse width	twrL	-	0.25 Tcy**	-	ns	
$\overline{ALE}$ ↑ to ALE ↑ (cycle time)	talH2alH	-	Tcy**	-	ns	
Capacitive load on output pins						
OSC2	Cload1	-	-	25	pF	(note 2)
ALE, $\overline{WR}$, $\overline{OE}$ and AD<15:0>	Cload2	-	-	100	pF	(note 3)
All other pins, including C, D, E ports (when used as port)	Cload3	-	-	50	pF	(note 3)

See footnotes on next page.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
*: Guaranteed by characterization
**: Guaranteed by design
NOTE 1: VDD must start from 0V for Power on reset to function properly. VDD rise time can be longer but then external POR circuitry will be required.
NOTE 2: In EC and RC oscillator modes when OSC2 pin is outputting CLKOUT, or in XT or LP mode when external clock is driven into OSC1 pin.
NOTE 3: All AC specs are valid for these capacitive loadings

12.3.2 AC Characteristics: Serial Port

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
SYNC XMIT (MASTER & SLAVE)						
Clock high to data out valid	tckH2dtV	-	-	50	ns	
Clock out rise time and fall time (Master Mode)	tckrf	-	-	25	ns	
Data out rise time and fall time	tdtrf	-	-	25	ns	
SYNC RCV (MASTER & SLAVE)						
Data in valid before CK ↓ (DT setup time)	tdtV2ckL	15	-	-	ns	
Data in invalid after CD ↓ (DT hold time)	tckL2dtl	15	-	-	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

12.3.3 AC Characteristics: I/O Port

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
CLKOUT ↑ to Port out valid	tckH2rxV	-	-	0.5Tcy+20	ns	note 1
Port A, B, C, D, E in valid before CLKOUT ↑ (RC and EC mode)	trxV2ckH	0.25 Tcy+25	-	-	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
NOTE 1: Timings are valid for a maximum of 50pF total capacitive load on the port pins, and CLKOUT pin.

12.3.4 AC Characteristics: RTCC & INT

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
RTCC in ext clock, prescale = 1						
RT clock input high time	trtH1	0.5 Tcy+20**	-	-	ns	
RT clock input low time	trtL1	0.5 Tcy+20**	-	-	ns	
RTCC in ext clock, prescale > 1						
RT clock input high time	trtH2	10*	-	-	ns	
RT clock input low time	trtH2	10*	-	-	ns	
RT clock input period	trtP	-	$\frac{Tcy+40^{**}}{N}$	-	ns	N = prescale value (2,4,8,....,256)
RT and INT interrupt input						
RT and INT input high time	triH	25*	-	-	ns	
RT and INT input low time	triL	25*	-	-	ns	

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

* Guaranteed by characterization

** Guaranteed by design and characterization

12.3.5 AC Characteristics: Timer1, Timer2, Timer3, Capture and PWM

Operating Conditions: 4.5V ≤VDD ≤5.5V, -40°C ≤TA ≤85°C unless otherwise stated.

Characteristic	Symbol	Min	Typ†	Max	Unit	Comments
Timer1, Timer2, Timer3						
Input clock high time on pins TCLK12, TCLK3	tcH	0.5Tcy+20**	-	-	ns	
Input clock low time on pins TCLK12, TCLK3	tcL	0.5Tcy+20**	-	-	ns	
Capture1, Capture2						
Input high time on RB0/CAP1, RB1/CAP2	tcpH	10*	-	-	ns	
Input low time on RB0/CAP1, RB1/CAP2	tcpL	10*	-	-	ns	
Input period on RB0/CAP1, RB1/CAP2	tcpL	$\frac{2\ Tcy\ **}{N}$	-	-	ns	where N=capture prescale (1, 4, 16)

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

* Guaranteed by characterization

12.3.6 AC TEST LOAD AND TIMING CONDITIONS

FIGURE 12.3.6.1 INPUT LEVEL CONDITIONS

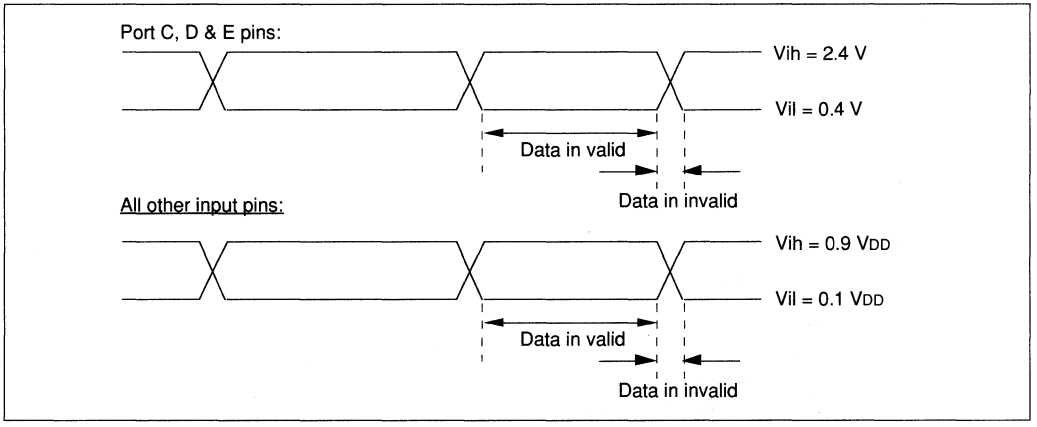


FIGURE 12.3.6.2 OUTPUT LEVEL CONDITIONS

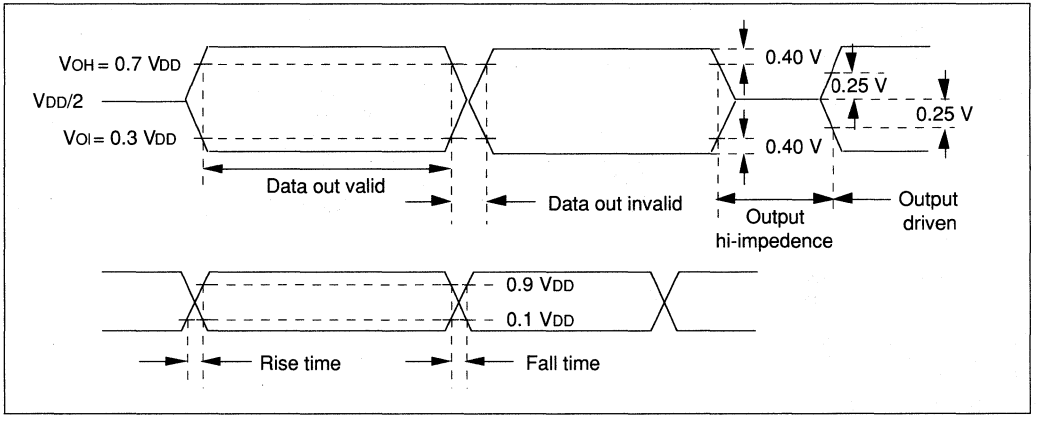
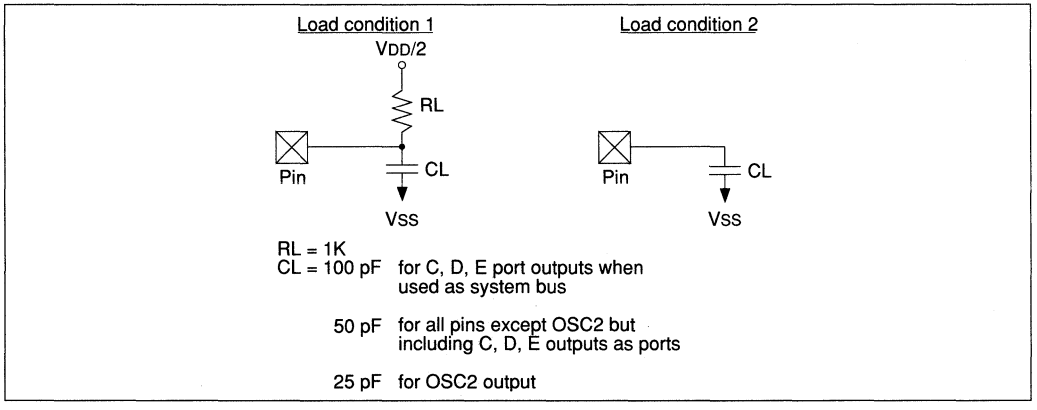
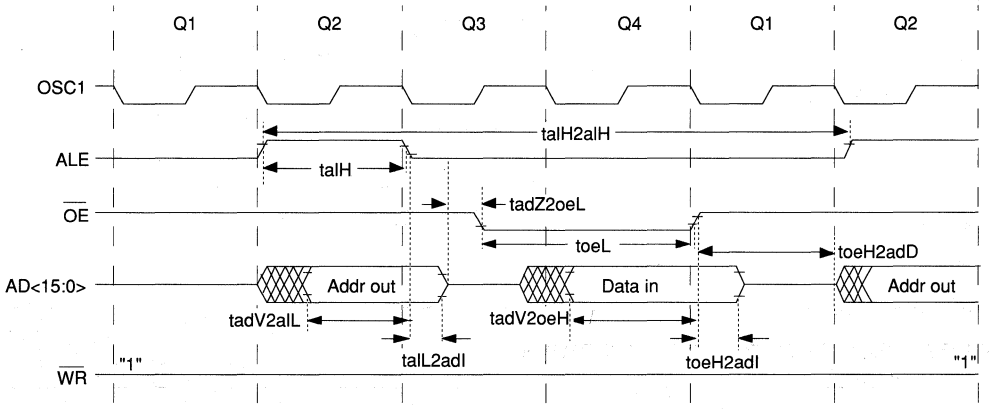


FIGURE 12.3.6.3 LOAD CONDITIONS



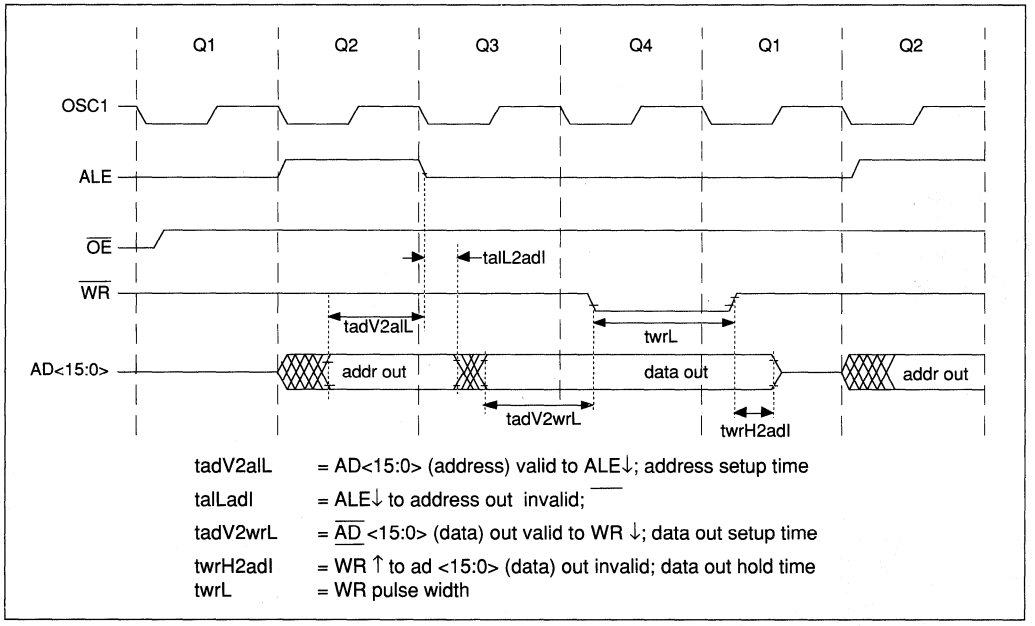
12.4 TIMING DIAGRAMS

FIGURE 12.4.1: TIMING DIAGRAM - EXTERNAL PROGRAM MEMORY READ



tadV2alL	= AD <15:0> (address) valid to ALE Ø; address setup time
talL2adl	= ALE Ø to AD<15:0> (address) invalid; address hold time
tadZ2oeL	= AD <15:0> high impedance to $\overline{OE}$ Ø
toeH2adD	= $\overline{OE}$ ≠ to AD <15:0> driven (address out)
tadV2oeH	= AD <15:0> (data) valid to $\overline{OE}$ ≠; data setup time
toeH2adl	= $\overline{OE}$ ≠ to AD <15:0> (data) invalid; data hold time
talH	= ALE pulse width
toeL	= $\overline{OE}$ pulse width
talH2alH	= ALE ≠ to ALE ≠; bus cycle period

FIGURE 12.4.2: TIMING DIAGRAM - EXTERNAL PROGRAM MEMORY WRITE



tadV2alL = AD<15:0> (address) valid to ALE↓; address setup time
talLadl = ALE↓ to address out invalid;
tadV2wrL = AD <15:0> (data) out valid to WR ↓; data out setup time
twrH2adl = WR ↑ to ad <15:0> (data) out invalid; data out hold time
twrL = WR pulse width

FIGURE 12.4.3: TIMING DIAGRAM - INTERRUPT TIMING

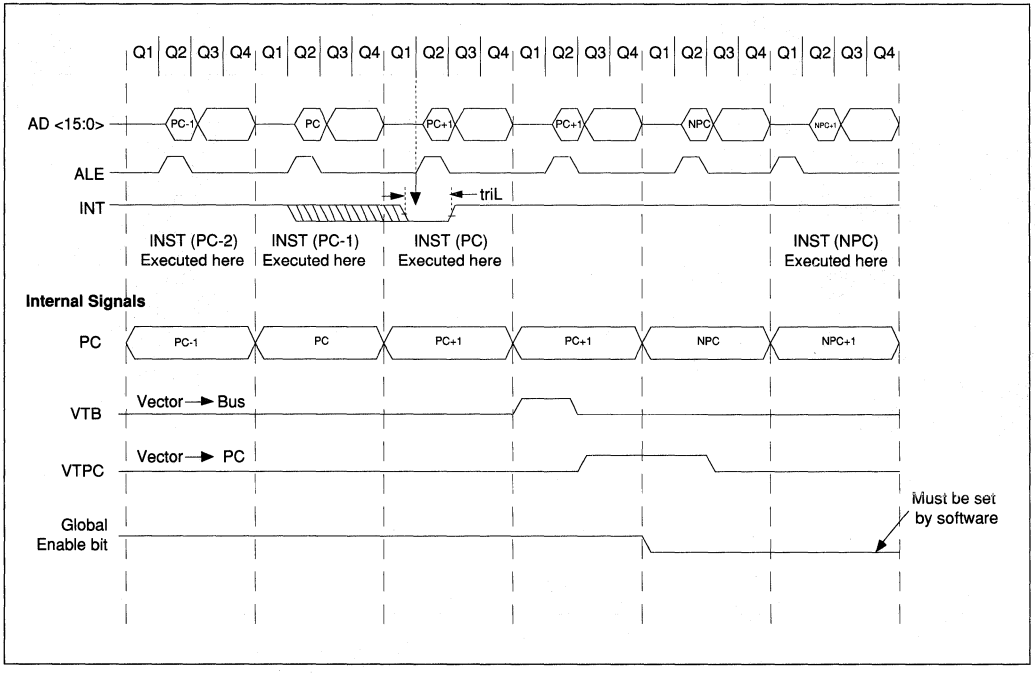


FIGURE 12.4.4: RESET TIMING

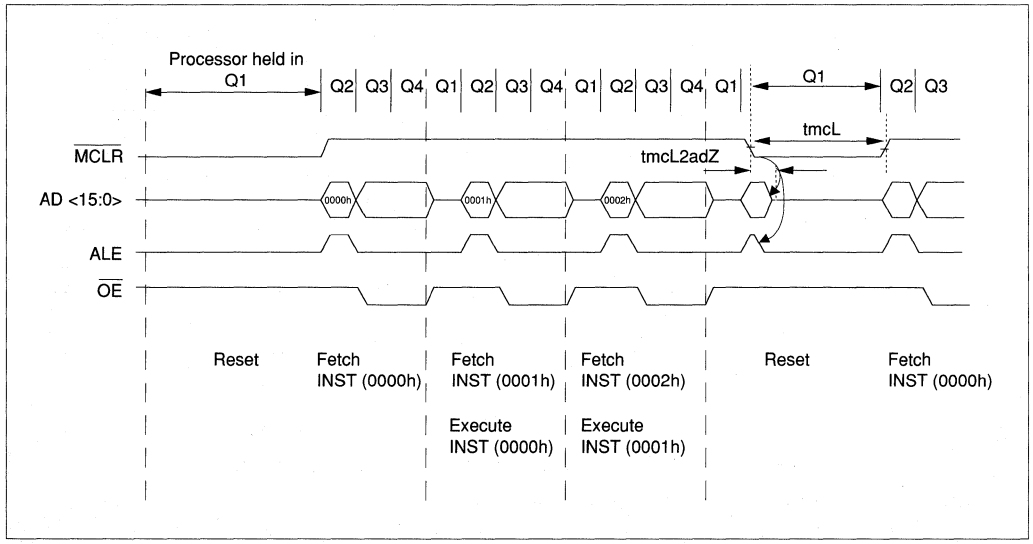


FIGURE 12.4.5: TABLRD TIMING

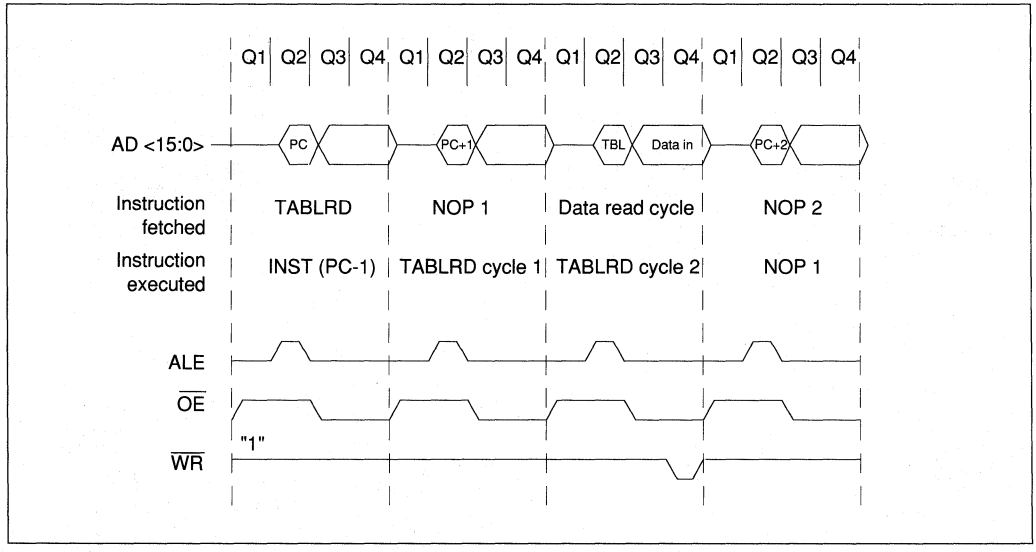


FIGURE 12.4.6: TABLRD TIMING (CONSECUTIVE TABLRD INSTRUCTIONS)

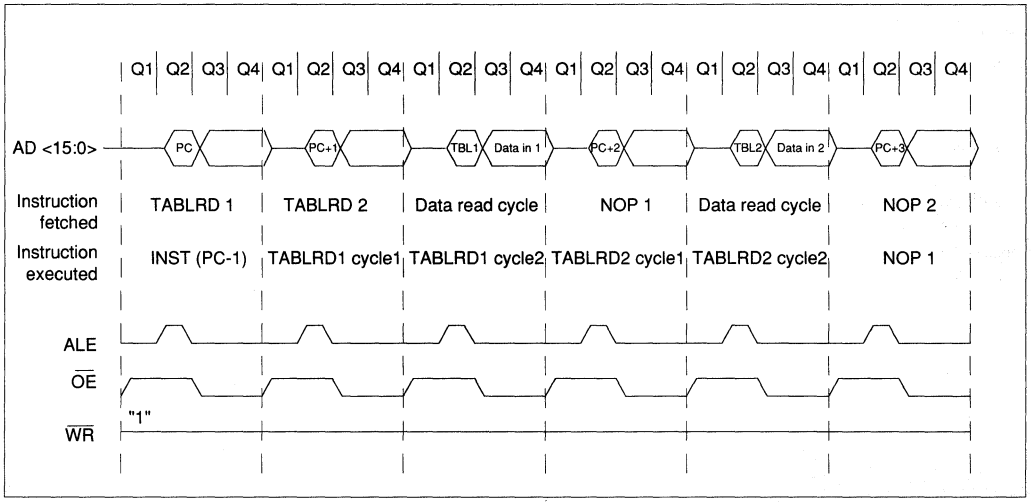


FIGURE 12.4.7: TABLWT TIMING

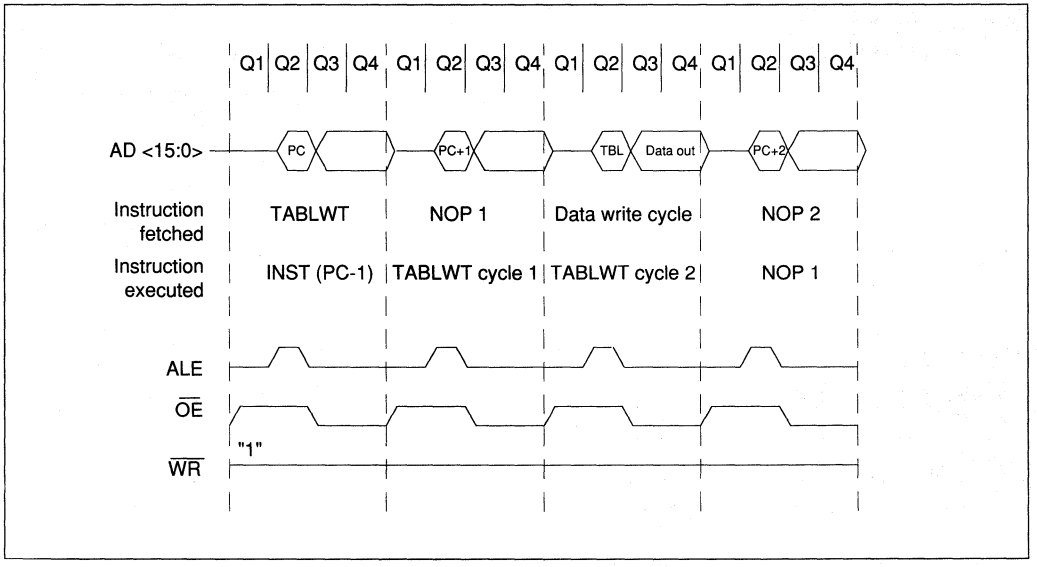


FIGURE 12.4.8: TABLWT TIMING (CONSECUTIVE TABLWT INSTRUCTIONS)

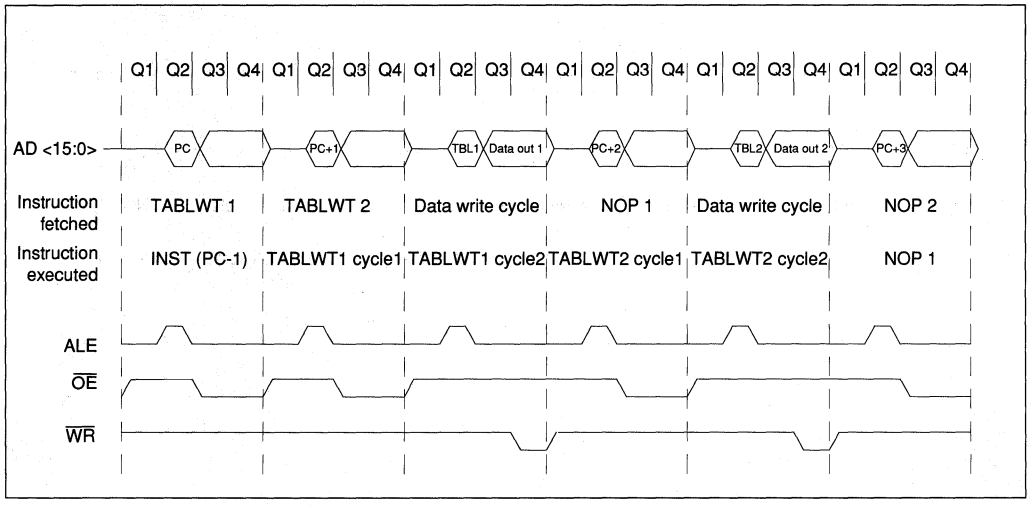
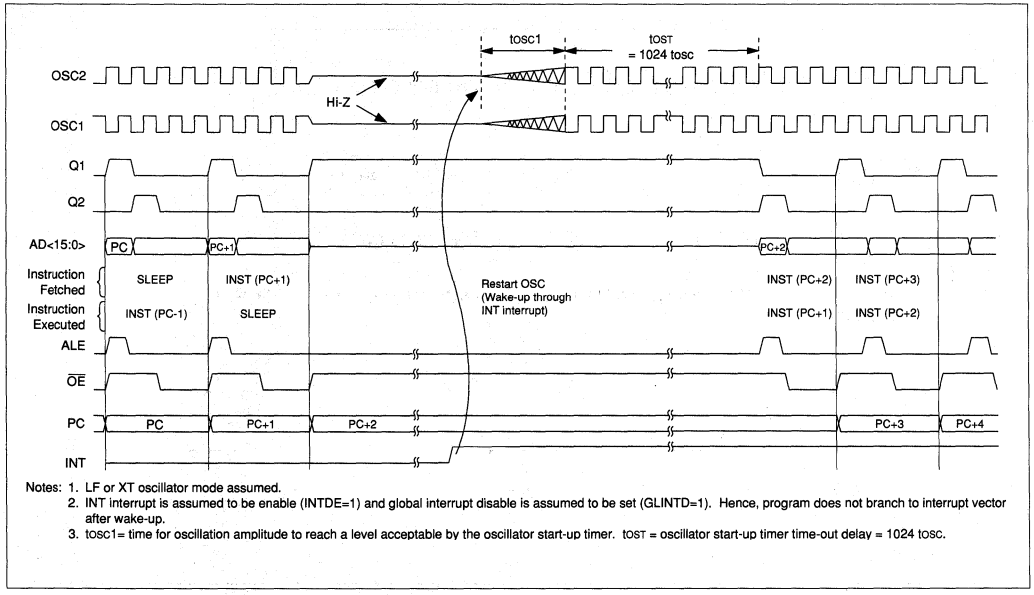
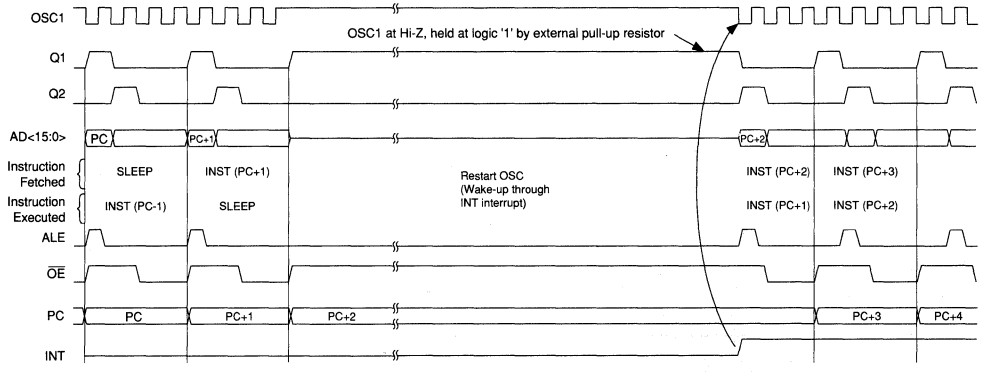


FIGURE 12.4.9: SLEEP/WAKE-UP THROUGH INT (LF, XT MODES)



Notes: 1. LF or XT oscillator mode assumed.
2. INT interrupt is assumed to be enable (INTDE=1) and global interrupt disable is assumed to be set (GLINTD=1). Hence, program does not branch to interrupt vector after wake-up.
3. tOSC1= time for oscillation amplitude to reach a level acceptable by the oscillator start-up timer. tOST = oscillator start-up timer time-out delay = 1024 tOSC.

FIGURE 12.4.10: SLEEP/WAKE-UP THROUGH INT (RC MODE)



Notes: 1. RC oscillator mode assumed.
2. INT interrupt is assumed to be enable (INTDE=1) and global interrupt disable is assumed to be set (GLINTD=1). Hence, program does not branch to interrupt vector after wake-up.
3. tosc1= time for oscillation amplitude to reach a level acceptable by the oscillator start-up timer. tost = oscillator start-up timer time-out delay = 1024 tosc.

FIGURE 12.4.11 SYNCHRONOUS TRANSMISSION (MASTER/SLAVE)

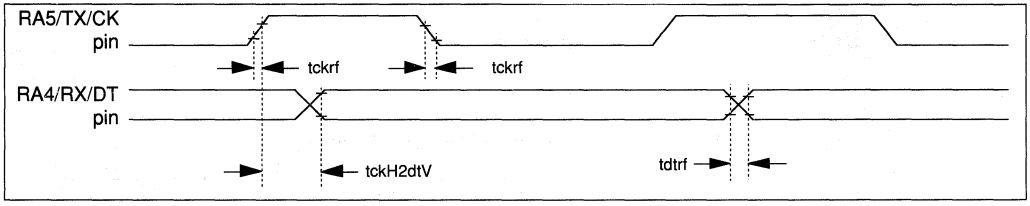


FIGURE 12.4.12 SYNCHRONOUS RECEIVE (MASTER/SLAVE)

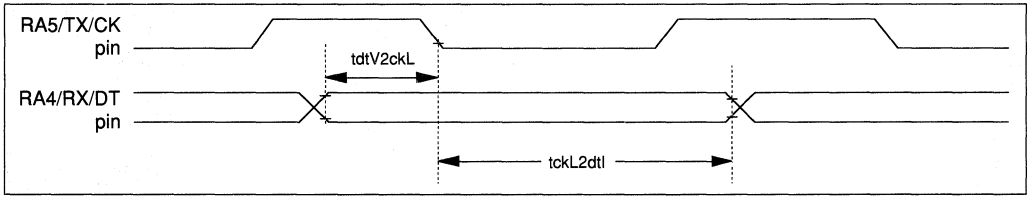
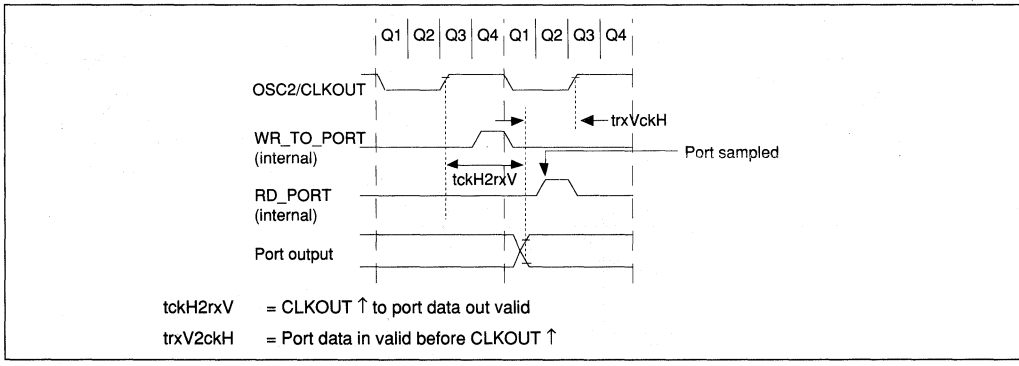
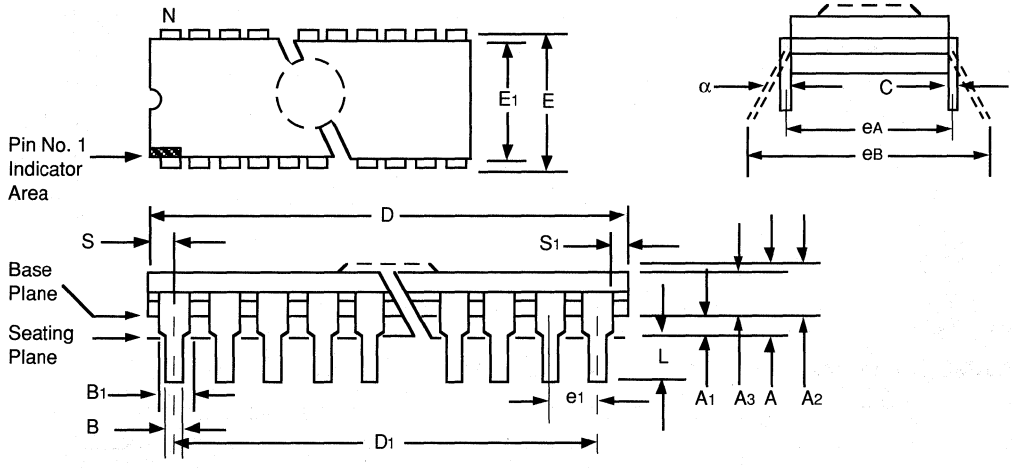


FIGURE 12.4.13: I/O PORT INPUT/OUTPUT TIMING (PORTA, PORTB)



13.0 PACKAGING INFORMATION

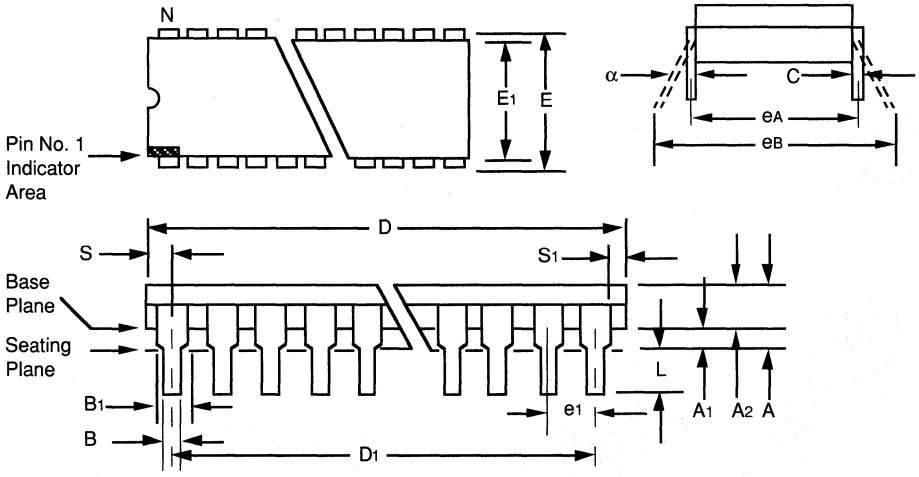
13.1 PACKAGE TYPE: 40-LEAD CERAMIC CERDIP DUAL IN-LINE WITH WINDOW (.600 MIL)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699	**Ref. A3**	0.150	0.185	**Ref. A3**
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	**Reference**	1.900	1.900	**Reference**
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	14.986	16.002	**Reference**	0.590	0.630	**Reference**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

13.0 PACKAGING INFORMATION (CONT.)

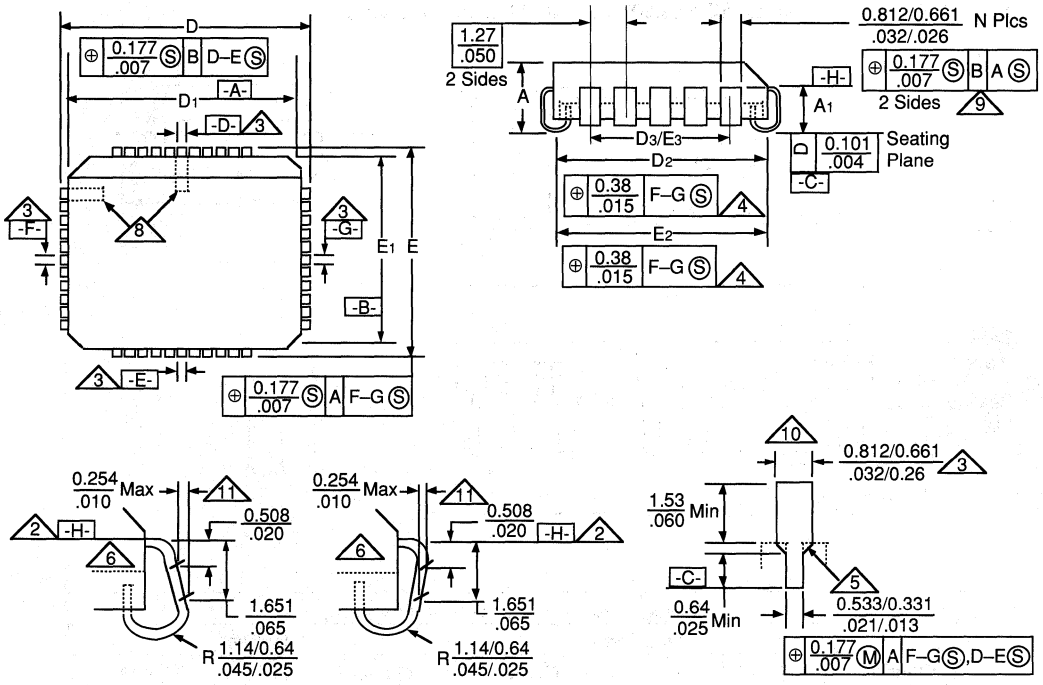
13.2 PACKAGE TYPE: 40-LEAD PLASTIC DUAL IN-LINE (.600 MIL)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min		Notes	Min	Max	Notes
α	0°			0°	10°	
A	–			–	0.200	
A1	0.381			0.015	–	
A2	3.175			0.125	0.160	
B	0.356			0.014	0.022	
B1	1.270		**Typical**	0.050	0.070	**Typical**
C	0.2032		**Typical**	0.008	0.015	**Typical**
D	51.181			2.015	2.055	
D1	48.260		**Reference**	1.900	1.900	**Reference**
E	15.240			0.600	0.625	
E1	13.462			0.530	0.550	
e1	2.489		**Typical**	0.098	0.102	**Typical**
eA	15.240		**Reference**	0.600	0.600	**Reference**
eB	15.240			0.600	0.680	
L	2.921			0.115	0.145	
N	40			40	40	
S	1.270			0.050	–	
S1	0.508			0.020	–	

13.0 PACKAGING INFORMATION (CONT.)

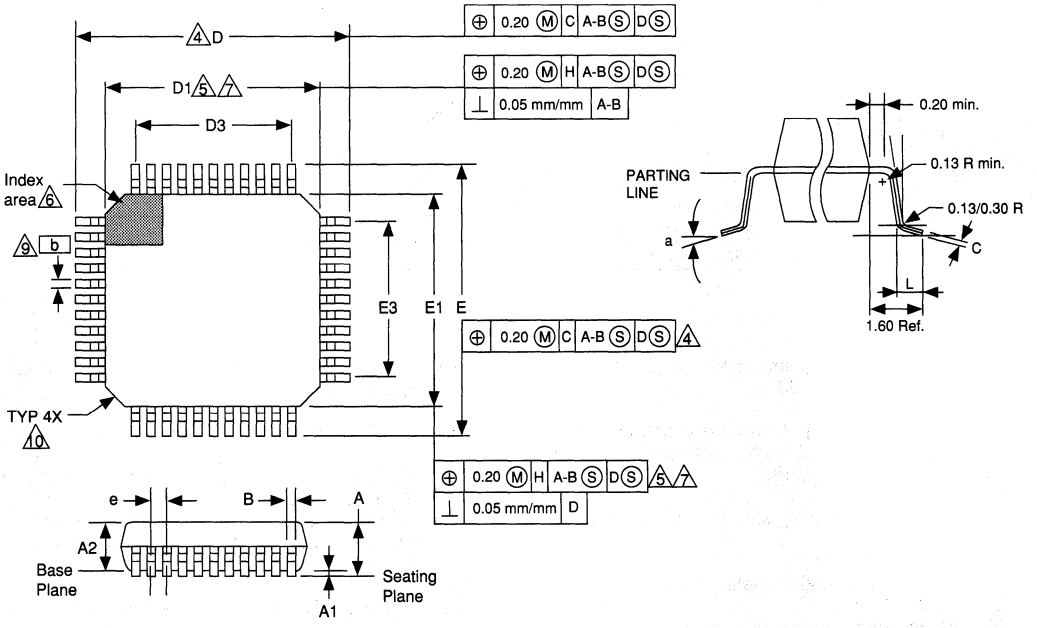
13.3 PACKAGE TYPE: 44-LEAD PLASTIC LEADED CHIP CARRIER (SQUARE)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	17.399	17.653		0.685	0.695	
D1	16.510	16.662		0.650	0.656	
D2	15.494	16.002		0.610	0.630	
D3	12.700	12.700	Reference	0.500	0.500	Reference
E	17.399	17.653		0.685	0.695	
E1	16.510	16.662		0.650	0.656	
E2	15.494	16.002		0.610	0.630	
E3	12.700	12.700	Reference	0.500	0.500	Reference
N	44	44		44	44	
CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

13.0 PACKAGING INFORMATION (CONT.)

13.4 PACKAGE TYPE: 44-LEAD METRIC PLASTIC QUAD FINE PITCH (MQFP 10X10MM BODY 1.6/.015MM LEAD FORM)



Package Group: Plastic MQFP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°		0°	7°	
A	2.00	2.35		0.0787	0.0925	
A_1	0.05	0.25		0.0019	0.0098	
A_2	1.95	2.10		0.768	0.0827	
b	0.30	0.45	Typical	0.0118	0.0177	Typical
C	0.15	0.18		.006	.007	
D	12.95	13.45		0.510	0.530	
D_1	9.90	10.10		0.390	0.398	
D_3	8.00	8.00	Reference	0.315	0.315	Reference
E	12.95	13.45		0.510	0.530	
E_1	9.90	10.10		0.390	0.398	
E_3	8.00	8.00	Reference	.315	.315	Reference
e	0.80	0.80		.0314	.0314	
L	0.65	0.95		.0256	.0374	
N	44	44		44	44	
CP	0.102			.004		

(Notes on following page)

Symbol List for Metric Plastic Quad Flat Pack Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body
b	Width of terminals
C	Thickness of terminals
D_1/E_1	Largest overall package parameter including leads
D/E	Largest overall package parameter including leads
D_3/E_3	Center of end lead to center of end lead
e	Linear spacing of true minimum lead position center line to center line
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead positions
CP	Seating plane coplanarity

Notes

1. All dimensioning and tolerancing conform to ANSI Y14, BM-1582.
2. Datum Plane -H- is located at bottom of hold parting line and coincident with bottom of lead, where lead exits body.
3. Datums A-B and -D- to be determined at Datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include hold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 do not include hold mismatch and are determined at Datum Plane -H-.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. These dimensions to be determined at Datum plane -H-.
8. All dimensions in millimeters.
9. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.
10. Exact shape of this feature is optional.
11. N is the number of leads.
12. Controlling parameters: milimeters
13. All packages are gull wing lead form.

Notes:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

PART NO - XXX/X XXX

	PATTERN:	3-Digit Pattern code for QTP (blank for OTP and windowed parts)
	PACKAGE:	P = PDIP JW = Cerdip window L = PLCC PQ = MQFP (Metric PQFP)
	TEMPERATURE RANGE:	Blank = 0°C to + 70°C I = -40°C to + 85°C
	SPEED:	16 = 16 Mhz
	DEVICE:	PIC17C42

SECTION 2
DEVELOPMENT SYSTEMS

PICMASTER™-16 System

PICMASTER Universal In-Circuit Emulator System

2

SYSTEM FEATURES

General:

- Complete Hi-Performance PC-based MSDOS Microcontroller Development System for the PIC16C5x family and PIC17C42 (future release).
- For use on PC compatible 286, 386, and 486 machines under Microsoft Windows® 3.X environment.
- Assembler Software, Emulator System, and EPROM Programmer unit, sample kit, and demonstration hardware and software provide a complete microcontroller product development environment.

Emulator System:

- Hi-Performance In-Circuit Emulation of Microchip Microcontrollers.
- Real-time instruction emulation.
- Single and Multiple instruction step execution.
- Program Memory emulation and memory mapping capability up to 64K words. Instruction execution can be mapped into either emulation memory or user prototype memory.
- Real-time trace memory capture of 40 bits of information for each instruction cycle in an 8Kx40 trace buffer. Trace region can range from 0 to 64K in any address combinations.
- Real-time trace data can be captured and displayed without halting emulation.
- Unlimited number of hardware breakpoints can be set anywhere in the program memory.
- External Break with "AND"/"OR" capability with internal breakpoints.
- Multiprocessor emulation capability. Up to eight PICMASTER emulators can be synchronized on a single PC, for multi-processor development.
- Extended 48-bit cycle counter.
- Trigger Output available on any range of addresses.
- Full Symbolic Debug Capability. Symbolic display and alter of all register files, special purpose registers, stack registers, and bank registers.
- Selectable Internal Emulator Clock or User Target (Prototype) System Clock.
- User selectable internal or external Power Supply (provided).

EPROM Programmer System:

- PICPRO-II EPROM Programmer unit for all current PIC16C5x products.
- Operates as a Stand-alone Unit or in Conjunction with a PC Compatible host system.
- Performs READ, PROGRAM, and VERIFY functions in Stand-alone mode. Uses Non-Volatile Program Memory (EEPROM).
- PC Host Software provides file display and editing, file transfer to and from programmer unit, device serialization, and program voltage calibration.

Macro Assembler:

- Provides translation of Assembler source code to object code for the PIC family of microcontrollers.
- Macro-assembly and conditional assembly capability.
- Produces Object files, Listing files, Symbol files, and special files required for symbolic debug with the PICMASTER Emulator System.
- Binary / Hex output formats: INHX8S, INHX8M, INHX16, and PICMASTER.

SYSTEM DESCRIPTION

The PICMASTER Universal In-Circuit Emulator System is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X and PIC17CXX families. This introductory system currently supports the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 at clock frequencies of 4 MHz and PIC17C42 at 16 MHz.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new microcontroller architectures with data and program memory paths to 16-bits.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows® 3.X environment, allowing the operator access to a wide range of supporting software and accessories.

Provided with the PICMASTER System is a high performance real-time In-Circuit Emulator, a microcontroller EPROM programmer unit, a macro assembler program, and a simulator program. Sample programs are provided to help quickly familiarize the user with the development system and the PIC microcontroller line.

Coupled with the user's choice of text editor, the system is ready for development of products containing any of Microchip's microcontroller products.

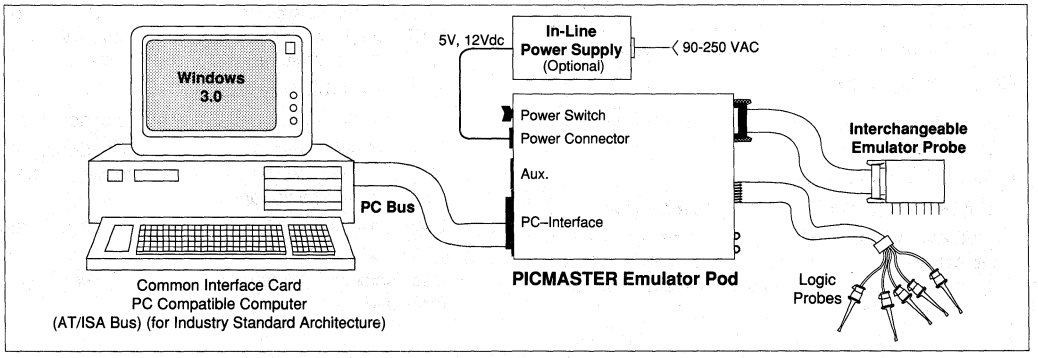
A "Quick Start" PIC Product Sample Pak containing user programmable parts is included for additional convenience.

Microchip provides additional customer support to developers through an electronic Bulletin Board System (BBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS system.

Host System Requirements:

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to you the end user. To properly take advantages of these features, PICMASTER requires installation on a system having the following minimum configuration:

- PC AT compatible machine: 80286, 386SX, 386DX, or 80486 with ISA or EISA Bus.
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended).
- MSDOS / PCDOS version 3.1 or greater.
- Microsoft Windows® version 3.0 or greater operating in either standard or 386 enhanced mode).
- 1 Mbyte RAM (2 Mbytes recommended).
- One 5.25" floppy disk drive.
- Approximately 10 Mbytes of hard disk (1 Mbyte required for PICMASTER, remainder for Windows 3.X system).
- One 8-bit PC AT (ISA) I/O expansion slot (half size)
- Microsoft® mouse or compatible (highly recommended).



Emulator System Components:

The PICMASTER Emulator Universal System consists primarily of 4 major components:

- **Host-Interface Card:** The PC Host Interface Card connects the emulator system to a PC compatible system. This high-speed parallel interface requires a single half-size standard AT / ISA slot in the host system. A 37-conductor cable connects the interface card to the external Emulator Control Pod.
- **Emulator Control Pod:** The Emulator Control Pod contains all emulation and control logic common to all microcontroller devices. Emulation memory, trace memory, event and cycle timers, and trace/breakpoint logic are contained here. The Pod controls and interfaces to an interchangeable target-specific emulator probe via a 14" precision ribbon cable.
- **Target-specific Emulator Probe:** A probe specific to microcontroller family to be emulated is installed on the ribbon cable coming from the control pod. This probe configures the universal system for emulation of a specific microcontroller. Currently, the 16C5x family, and the new PIC17C42 microcontrollers are supported. Future microcontroller probes will be available as they are released.
- **PC Host Emulation Control Software:** Host software necessary to control and provide a working user interface is the last major component of the system. The emulation software runs in the Windows 3.X environment, and provides the user with full display, alter, and control of the system under emulation. The Control Software is also universal to all microcontroller families.

  The Windows 3.X System is a multitasking operating system which will allows the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

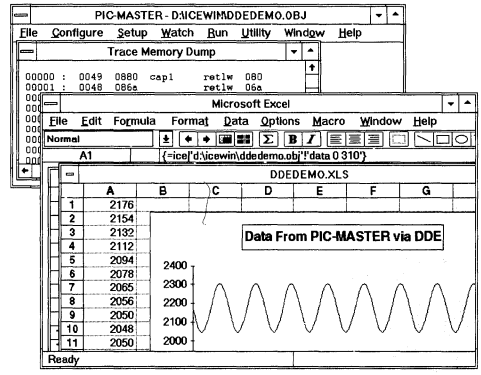
  PICMASTER emulation can operate in one window, while a text editor is running in a second window. Dynamic Data Exchange (DDE), a feature of Windows 3.X, will be available in this and future versions of the software. DDE allows data to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

  Under Windows 3.X, up to eight PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16C5x processor and a PIC17Cxx processor).

PICPRO-II EPROM Programmer:

The PICPRO-II Programmer system included in the PICMASTER Development System provides the product developer with the ability to program (transfer) the developer's software into PIC EPROM microcontrollers.

The programmer unit comes complete with accessories for use with a PC host computer. Supplied are interface cables and connectors to a standard PC parallel printer port (LPT), a wall mount power supply unit, and host operating software.



The PICPRO-II Programmer will work in either stand-alone mode, or in PC host connected mode. Connected to a PC host, many more features are available to the user.

STAND-ALONE MODE

Stand-alone mode is useful in situations where a PC may not be available or even required, such as in the field or in a lab production environment. In stand-alone mode the following programming functions are available:

VERIFY

VERIFY preforms two functions. For a programmed part, the device in the programming socket will be compared to the program data stored in internal EEPROM. If the data and fuse settings are correct, VERIFIED will be displayed. VERIFY will also confirm that erased parts are blank. A device in the socket will display ERASED if all programmable locations are blank.

PROGRAM

In stand-alone mode, devices inserted into the programmer socket will be programmed with data currently stored in EEPROM memory. Pressing the PROGRAM key will cause the unit to program and verify both the program memory and the device fuses. If all program successfully, PGM OKAY will be displayed.

READ

A pre-programmed device placed in the programmer socket can be read into the programmer unit by pressing the READ key. Program and fuse data will be read and stored into internal EEPROM. Various options exist with the READ function.

PC HOST CONNECT MODE

When the PICPRO-II is connected to a host PC system, many more options and conveniences are available to the user. Host mode allows full interactive control over the PICPRO-II unit. A full screen, user-friendly software program is provided to fully assist the user.

As in stand-alone mode, parts may be Read, Programmed, Blank checked, and Verified. Also, all fuses and ID locations may be specified. In addition, other features available in host-mode are:

Editing

A large screen buffer editing facility allows the user to change and program location in either hexadecimal or ASCII (text) modes. Complete program and fuse data can be loaded and saved to DOS disk files. Files generated by the Assembler program are directly loadable into programmer memory.

VDD and VPP Adjust

The programming environment voltage settings of VDD max, VDD min, and VPP can be set and altered only on PC host mode. The voltage settings allow the user to program the part in the environment that the part will be used. The part will be programmed at VDD max and verified at VDD min. VPP is the programming voltage.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBER	DESCRIPTION
EM167001	**Complete PICMASTER-16 System with 100 volt PICPRO-II Power Supply (1)**
EM167002	**Complete PICMASTER-16 System with 110 volt PICPRO-II Power Supply (2)**
EM167003	**Complete PICMASTER-16 System with 220 volt PICPRO-II Power Supply (3)**
EM167004	**Complete PICMASTER-16 System with 240 volt PICPRO-II Power Supply (4)**
EM167010	**Complete PICMASTER-16 System without PICPRO-II Programmer**

Notes:
(1) Used primarily in Japan
(2) Used primarily in North, Central, and South America, Taiwan and Korea
(3) Used primarily in Continental Europe, Hong Kong, Singapore and Scandinavia
(4) Used primarily in England, Ireland, Scotland and R.O.C. (China)

PICMASTER-17™ System

PICMASTER PIC®17CXX In-Circuit Emulator System

SYSTEM FEATURES

General:

- The PICMASTER-17 Development System is designed by Microchip Technology Incorporated and manufactured in the U.S.A.
- Complete Hi-Performance PC-based MSDOS Microcontroller Development System for the PIC17Cxx family.
- For use on PC compatible 286, 386, and 486 machines under the Windows™ 3.X environment.
- Assembler Software, Emulator System, and EPROM Programmer unit, sample kit, and EDP demonstration board and software provide a complete microcontroller product development environment.

Emulator System:

- Universal In-Circuit Emulation pod supports emulation of PIC17CXX family. It can easily support other PIC microcontroller products with the purchase of a low cost personality probe kit.
- Real-time emulation to 16 Mhz.
- Single and Multiple instruction step execution.
- Program Memory emulation and memory mapping capability up to 64K words. Instruction execution can be mapped into either emulation memory or user prototype memory.
- Real-time trace memory capture of 40 bits of information for each instruction cycle in an 8Kx40 trace buffer. Trace region can range from 0 to 64K in any address combinations.
- Real-time trace data can be captured and displayed without halting emulation.
- Unlimited number of hardware breakpoints can be set anywhere in the program memory.
- External Break with "AND"/"OR" capability with internal breakpoints.
- Multiprocessor emulation capability. Two or more PICMASTER emulators can be synchronized on a single PC for multi-processor development.
- Extended 48-bit cycle counter.
- Trigger Output available on any range of addresses.
- Full Symbolic Debug Capability. Symbolic display and alter of all register files, special purpose registers, stack, and bank registers.
- Selectable Internal Emulator Clock or User Target (Prototype) System Clock.
- User selectable internal or external Power Supply (provided).

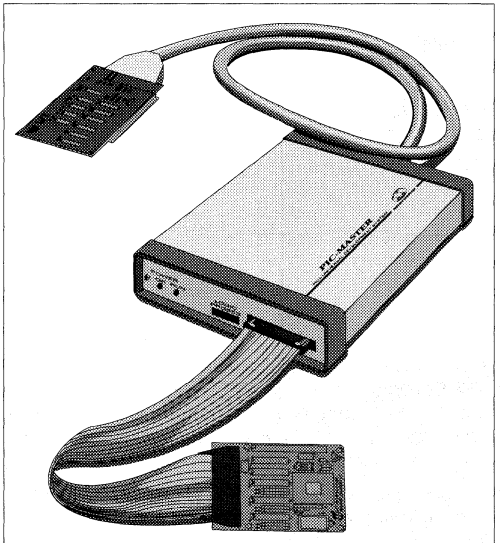


FIGURE 1: PICMASTER EMULATOR SYSTEM

EPROM Programmer System:

- PRO MASTER™ EPROM Programmer unit for all Microchip PIC CMOS microcontrollers.
- Operates as a Standalone Unit or in Conjunction with a PC Compatible host system.
- Performs READ, PROGRAM, and VERIFY functions in Standalone mode.
- PC Host Software provides file display and editing, file transfer to and from programmer unit, device serialization, and program voltage calibration.

Macro Assembler:

- PICASM-17 provides macro-assembly and conditional assembly capability.
- Provides translation of Assembler source code to object code for the PIC family of microcontrollers.
- Produces Object files, Listing files, Symbol files, and special files required for symbolic debug with the PICMASTER Emulator System.
- Binary / Hex output formats: INHX8S, INHX8M, INHX32.

SYSTEM DESCRIPTION

The PICMASTER Universal In-Circuit Emulator System provides the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC16C5X and PIC17CXX families. The system currently supports the PIC16C54, PIC16C55, PIC16C56, PIC16C57 and PIC17C42.

The PICMASTER-17 System is configured to support the PIC17C42 and related 17Cxx family members. Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new microcontroller architectures with data and program memory paths to 16-bits.

The Emulator System is designed to operate on low-cost PC compatible machines ranging from 80286-AT class ISA-bus systems through the new 80486 EISA-bus machines. The development software runs in the Microsoft Windows 3.X™ environment, allowing the operator access to a wide range of supporting software and accessories.

Provided with the PICMASTER System is a high performance real-time In-Circuit Emulator, a microcontroller EPROM programmer unit, and a macro assembler program. Sample programs are provided to help quickly familiarize the user with the development system and the PIC microcontroller line.

Coupled with the user's choice of text editor, the system is ready for development of products containing any of Microchip's microcontroller products.

A "Quick Start" PIC Product Sample Pak containing user programmable parts is included for additional convenience.

Microchip provides additional customer support to developers through an electronic Bulletin Board System (BBS). Customers have access to the latest updates in software as well as application source code examples.

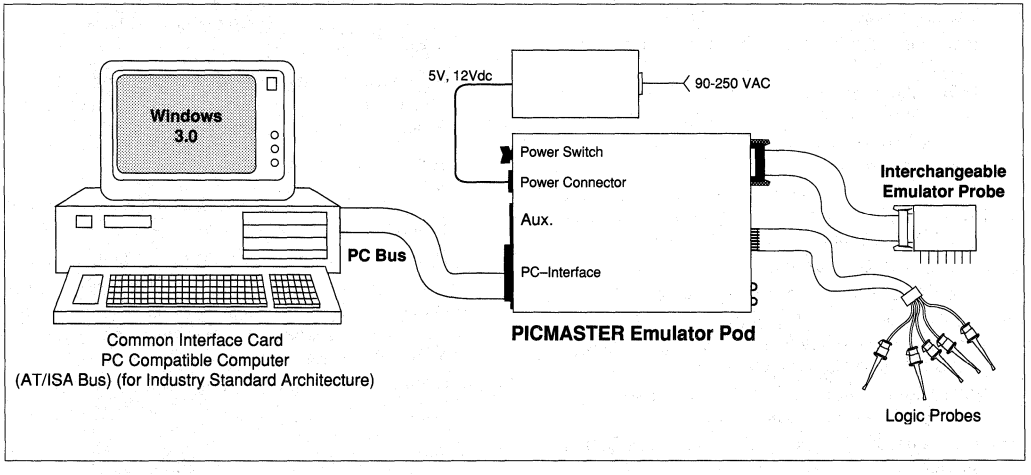
Consult your local sales representative for information on accessing Microchip Technology's Bulletin Board System (BBS).

Host System Requirements

The PICMASTER has been designed as a real-time emulation system with advanced features generally found on more expensive development tools. The AT platform and Windows 3.X environment was chosen to best make these features available to you the end user. To properly take advantages of these features, PICMASTER requires installation on a system having the following minimum configuration:

- PC AT compatible machine: 80286, 386SX, 386DX, or 80486 with ISA or EISA Bus
- EGA, VGA, 8514/A, Hercules graphic card (EGA or higher recommended).
- MSDOS / PCDOS version 3.1 or greater.
- Microsoft Windows version 3.0 or greater operating in either standard or 386 enhanced mode).
- 1 Mbyte RAM (2 Mbytes recommended).
- One 5.25" floppy disk drive.
- Approximately 10 Mbytes of hard disk (1 Mbyte required for PICMASTER, remainder for Windows 3.0 system)
- One 8-bit PC AT (ISA) I/O expansion slot (half size)
- Microsoft mouse or compatible (highly recommended).

Emulator System Components



The PICMASTER Emulator Universal System consists primarily of 4 major components:

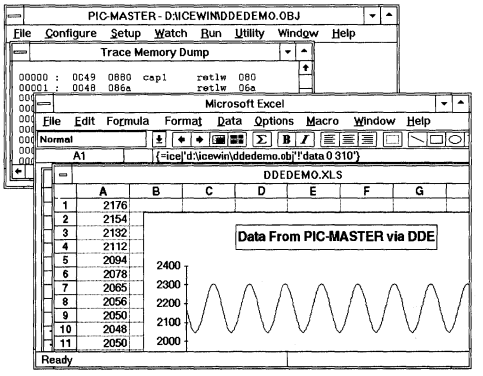
- **Host-Interface Card:** The PC Host Interface Card connects the emulator system to a PC compatible system. This high-speed parallel interface requires a single half-size standard AT / ISA slot in the host system. A 37-conductor cable connects the interface card to the external Emulator Control Pod.
- **Emulator Control Pod:** The Emulator Control Pod contains all emulation and control logic common to all Microchip CMOS microcontroller devices. Emulation memory, trace memory, event and cycle timers, and trace/breakpoint logic are contained here. The Pod controls and interfaces to an interchangeable target-specific emulator probe via a 14" precision ribbon cable.
- **Target-specific Emulator Probe:** A probe specific to microcontroller family to be emulated is installed on the ribbon cable coming from the control pod. This probe configures the universal system for emulation of a specific microcontroller. Currently, the PIC16C5x family, and the new PIC17C42 microcontrollers are supported. Future microcontroller probes will be available as they are released.
- **PC Host Emulation Control Software:** Host software necessary to control and provide a working user interface is the last major component of the system. The emulation software runs in the Windows 3.X environment, and provides the user with full display, alter, and control of the system under emulation. The Control Software is also universal to all microcontroller families.

  The Windows 3.X System is a multitasking operating system which allows the developer to take full advantage of the many powerful features and functions of the PICMASTER system.

  PICMASTER emulation can operate in one window, while a text editor is running in a second window. PICMASTER supports the window feature Dynamic data Exchange (DDE). DDE allows data and commands to be dynamically transferred between two or more Windows programs. With this feature, data collected with PICMASTER can be automatically transferred to a spreadsheet or database program for further analysis.

  Under Windows 3.X, two or more PICMASTER emulators can run simultaneously on the same PC making development of multi-microcontroller systems possible (e.g., a system containing a PIC16C5x controller and a PIC17Cxx controller) or two or more of the same controller family.

This allows data collected by PICMASTER to be automatically transferred to spreadsheets, data bases, or other analytic tools for further evaluation. DDE also allows automated control of PICMASTER which in turn allows development of automated test suites, life testing and production testers.



PRO MASTER EPROM Programmer

The PRO MASTER Programmer system included in the PICMASTER Development System provides the product developer with the ability to program (transfer) the developer's software into PIC EPROM microcontrollers.

The programmer unit comes complete with accessories for use with a PC host computer. Supplied are interface cables and connectors to a standard PC serial port COM 1-4, power supply cable, and host operating software.

The PRO MASTER Programmer will work in either stand-alone mode, or in PC host connected mode. Connected to a PC host, many more features are available to the user as explained below.

STAND-ALONE MODE

Stand-alone mode is useful in situations where a PC may not be available or even required, such as in the field or in a lab production environment. In stand-alone mode the following programming functions are available:

VERIFY

VERIFY preforms two functions. For a programmed part, the device in the programming socket will be compared to the program data stored in internal EEPROM. If the data and fuse settings are correct, VERIFIED will be displayed. VERIFY will also confirm that erased parts are blank. A device in the socket will display ERASED if all programmable locations are blank.

PROGRAM

In stand-alone mode, devices inserted into the programmer socket will be programmed with data currently stored in memory. Pressing the PROGRAM key will cause the unit to program and verify both the program memory and the device fuses. If all program successfully, PGM OKAY will be displayed.

READ

A pre-programmed device placed in the programmer socket can be read into the programmer unit by pressing the READ key. Program and fuse data will be read and stored into internal memory. Various options exist with the READ function.

PC HOST CONNECT MODE

When the PRO MASTER is connected to a host PC system, many more options and conveniences are available to the user such as serialized code programming. Host mode allows full interactive control over the PRO MASTER unit. A full screen, user-friendly software program is provided to assist the user.

As in stand-alone mode, parts may be Read, Programmed, Blank checked, and Verified. Also, all fuses and ID locations may be specified. Other features available in host-mode are:

Editing

A large screen buffer editing facility allows the user to change and program location in hexadecimal mode. Complete program and fuse data can be loaded and saved to DOS disk files. Files generated by the Assembler program are directly loadable into programmer memory.

VDD and VPP Adjust

The programming environment voltage settings of VDD max, VDD min, and VPP can be set and altered only on PC host mode. The voltage settings allow the user to program the part in the environment that the part will be used. The part will be programmed at VDD max and verified at VDD min. VPP is the programming voltage.

SALES AND SUPPORT - To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBER	DESCRIPTION
EM177001	PICMASTER PIC17CXX In-Circuit Emulator System
EM177004	PICMASTER-17 System without PRO MASTER Programmer

PICPAK-II™ System

PIC®16C5x Low-Cost Microcontroller Development System

SYSTEM FEATURES

EPROM Programmer System

- PICPRO-II™ EPROM Programmer unit for the PIC16C5X Microcontroller family.
- Operates as a Stand-alone Unit or in Conjunction with a PC Compatible host system.
- READS, PROGRAMS, and VERIFIES in Stand-alone mode.
- Non-Volatile Program Memory for stand-alone or field use where PC is not available.
- PC Host Software provides file display and editing, and transfer to and from Programmer unit.

PICALC Macro Assembler

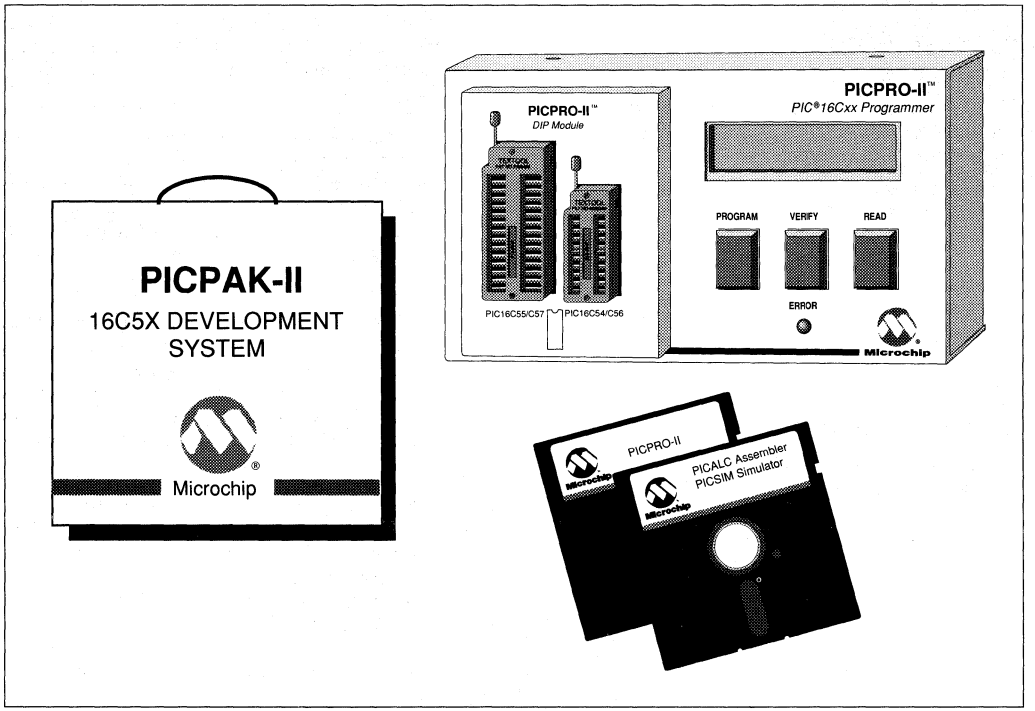
- Provides translation of Assembler source code to object code for all PIC microcontrollers.
- Macro-Assembly capability.
- Provides Object files, Listing files, Symbol files, and special files required for symbolic debug with the PIC Emulator System.
- Output formats: INHX8S, INHX8M and INHX16.

PICSIM Simulator

- Instruction-level Simulator of the PIC16C5x microcontroller product family.
- For PC compatible systems running the MSDOS operating system.
- Full screen simulation user interface.
- Symbolic debugging capability.
- I/O stimulus input capability.

"Quick Start" Sample Kit

- Provides the User / Developer with a sample kit of PIC parts for initial prototype use.



SYSTEM DESCRIPTION

The PICPAK-II Development System provides the product development engineer with an alternative low-cost introductory microcontroller design tool set for the PIC16C5X family where full real-time emulation is not required. The equipment in the PICPAK-II system operates on any PC compatible machine running the MSDOS/PCDOS operating system.

Provided in the System is an MSDOS-based Software Simulator program (PICSIM), a microcontroller EPROM programmer unit (PICPRO-II), and a macro assembler program (PICALC).

Sample software programs to be run on the simulator are provided to help the user to quickly become familiar with the development system and the PIC microcontroller line.

The user need only provide his or her own preferred text editor and the system is ready for development of end products using the PIC16C54, 16C55, 16C56, or 16C57 microcontrollers.

A "Quick Start" PIC16C5X Product Sample Pak containing user programmable parts is included for additional convenience.

Microchip provides additional customer support to developers through an electronic Bulletin Board System (BBS). Customers have access to the latest updates in software as well as application source code examples. Consult your local sales representative for information on accessing the BBS.

PICPRO-II EPROM Programmer

The PICPRO-II Programmer system included in the PICPAK-II Development System provides the product developer with the ability to program user software into PIC16C5x EPROM microcontrollers.

The programmer unit comes complete with accessories to be used with the PC host computer. Supplied are interface cables and connectors to a standard PC parallel printer port (LPT), a wall mount power supply unit, and host operating software (PP2.EXE).

The PICPRO-II Programmer will work in either stand-alone mode, or in PC host connected mode. Connected to a PC host, many more features are available to the user.

STAND-ALONE MODE

Stand-alone mode is useful in situations where a PC may not be available or even required, such as in the field or in a lab production environment. In stand-alone mode the following programming functions are available:

VERIFY

VERIFY performs two functions. For a programmed part, the device in the programming socket will be compared to the program data stored in internal EEPROM. If the data and fuse settings are correct, VERIFIED will be displayed. VERIFY will also confirm that erased parts are blank. A device in the socket will display ERASED if all programmable locations are blank.

PROGRAM

In stand-alone mode, devices inserted into the programmer socket will be programmed with data currently stored in EEPROM memory. Pressing the PROGRAM key will cause the unit to program and verify both the program memory and the device fuses. If all program successfully, PGM OKAY will be displayed.

READ

A pre-programmed device placed in the programmer socket can be read into the programmer unit by pressing the READ key. Program and fuse data will be read and stored into internal EEPROM. Various options exist with the READ function.

PC HOST CONNECT MODE

When the PICPRO-II is connected to a host PC system, many more options and conveniences are available to the user. Host mode allows full interactive control over the PICPRO-II unit. A full screen, user-friendly software program (PP2.EXE) is provided to fully assist the user.

As in stand-alone mode, parts may be Read, Programmed, Blank checked, and Verified. Also, all fuses and ID locations may be specified. In addition, other features available in host-mode are:

Editing

A large screen buffer editing facility allows the user to change and program location in either hexadecimal or ASCII (text) modes. Complete program and fuse data can be loaded and saved to DOS disk files. Files generated by the PICALC Assembler program are directly loadable into programmer memory.

VDD and VPP

The programming environment voltage settings of VDD max, VDD min, and VPP can be set and altered only on PC host mode. The voltage settings allow the user to program the part in the environment that the part will be used. The part will be programmed at VDD max and verified at VDD min. VPP is the programming voltage.

Parts Serialization

In PC host mode, the user can select up to 8 locations to be programmed with a serial number or random security code. Provisions for setting the address ranges, and starting serial numbers are provided. The serial number can use either incrementing serialization, or a random number sequence. Serialization is also permitted with parts already code-protected in the first 64 locations. This allows end user customization while keeping proprietary, the program software code.

PICPRO-II SPECIFICATIONS

Device Types	**PIC16C54, 16C55, 16C56, 16C57 (oscillators: RC, XT, HS, LP)**
Capacity	**Program and fuse information for one device to 2Kx12 (stored in non-volatile EEPROM).**
Enclosure	**6.5"L x 3.75"x 1.25" epoxy coated aluminum, rubber feet**
Weight	**14 oz.**
Power	**±20 to 35VDC. External AC/DC power supply included. Lab power cord with standard banana jacks.**
Display	**8 character LCD**
Interface	**Host PC Printer Port (auto-seeking of LPT1-LPT4 port)**
Adapters	**18 and 28 Pin ZIF DIP (standard) 18 and 28 lead SOIC (optional)**
Software	**PP2.EXE provided on 5.25" MSDOS 360K diskette.**
Accessories	**DB25-RJ11 adapter for host PC, RJ11 cable to PICPRO-II, User Manual.**

PICSIM Simulator

The PICSIM Simulator program provides the developer with an instruction and limited I/O simulator software program for debugging PIC16C5x assembler code.

The simulator is meant for use with smaller projects not requiring precise more extensive development equipment. Since the PIC16C5x architecture is essentially a single tasking microcontroller without interrupts, many applications can be developed by using a simulator program alone.

The PICSIM Simulator has the following features to assist in the debugging of software/firmware for the user:

Program Load/Save

Commands exist to load assembled object file programs into simulation memory. Conversely, programs may be saved from program simulation memory back to the PC disk.

Display & Alter

Provisions are made to display and alter Program Memory, Register Files, and status register bits. Also simulator information such as cycle times, elapsed time, and step count can be displayed.

Disassembler

Program memory can be disassembled showing both hexadecimal data and instruction mnemonics for specified address ranges.

Utilitiy Functions

Various utility functions exist which assist the user in operating the simulator. Memory and registers can be cleared by command. Memory can be searched to find occurances of instructions, register use, and ASCII data.

Symbolic Debugging

The simulator provides for symbolic referencing to aid and simplify debugging. The symbol table may be displayed. New symbols defined and unwanted symbols deleted.

Execution and Trace

During program execution, address ranges, registers, register contents, and others can be traced.

Breakpoints

The user may specify up to 512 breakpoints at any one time.

SALES AND SUPPORT

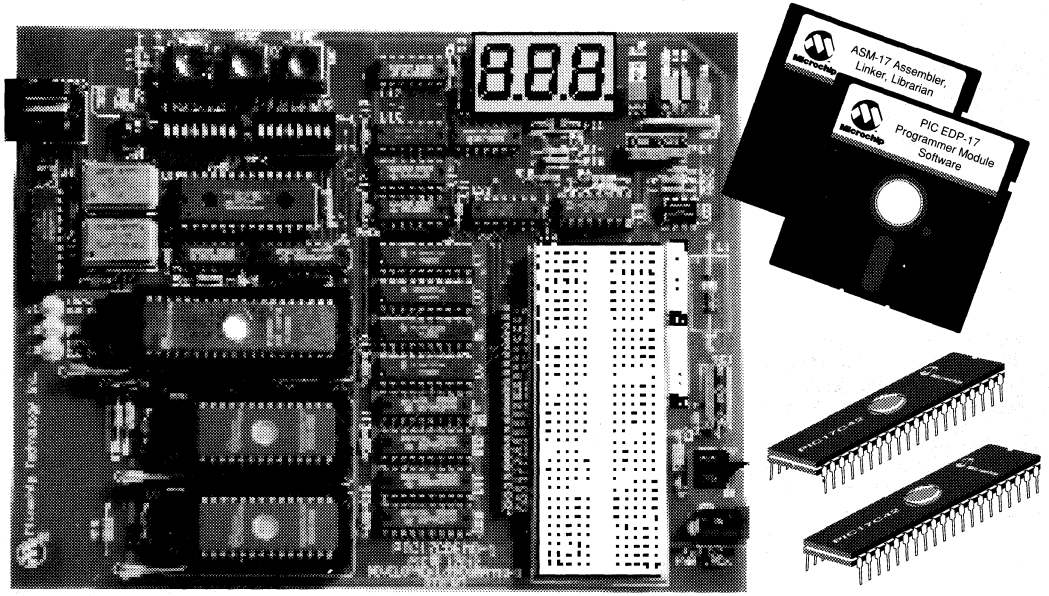
To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBER	DESCRIPTION
DV165001	**Programmer/Applications Kit with 100V Power Supply (1)**
DV165002	**Programmer/Applications Kit with 110V Power Supply (2)**
DV165003	**Programmer/Applications Kit with 220V Power Supply (3)**
DV165004	**Programmer/Applications Kit with 240V Power Supply (4)**
AC164009	**Optional 18 and 28-Lead SOIC Adapter**

Notes: (1) Used primarily in Japan
(2) Used primarily in North, Central and South America, Taiwan and Korea
(3) Used primarily in Continental Europe, Hong Kong, Singapore and Scandinavia
(4) Used primarily in England, Ireland, Scotland and R.O.C. (China)

PICPAK-17™ System

PIC®17C42 Evaluation / Development / Programmer Kit



SYSTEM FEATURES

- Low-cost Evaluation, Development, Demonstration, and Programmer Kit for the PIC17C42 Microcontroller.
- Provides a method for the design engineer to rapidly evaluate, learn, and experiment with the Microchip PIC17C42 Microcontroller.
- The PICEDP-17 Board provides for three execution modes of the PIC17C42:
  - Microcontroller mode using internal program memory only.
  - Extended Microcomputer mode using both internal memory and external memory.
  - Microprocessor mode using external memory only.
- On-board programming capability for the PIC17C42. Microcontroller self-programs from socketed external memory devices.
- 3 digit seven-segment LED display for use by the PIC17C42 application.
- PIC17C42 signals are available to the prototyping solderless terminal block. PIC17C42 I/O lines RA, RB, RC, RD, and RE available at terminal block.
- RS232 Port can be connected to PIC17C42 serial port (Rx, Tx, CTS, RTS, DSR lines supported).
- Socketed PIC16C57 microcontroller generates RESET and PROGRAM signals, and provides I/O stimulus to PIC17C42.
- Requires a single +5VDC power supply. Lab cable included.
- PC based software included: PICASM-17 Macro Assembler, I/O stimulus, and demonstration software with source code available.
- "Quick Start" Sample Chip Kit included: PIC17C42 and 27C64 UV-erasable parts. Fully assembled and ready to use.
- Documentation: PIC17C42 datasheet, full schematics, Assembler manual, and applications booklet.

INTRODUCTION

The PICPAK-17 is a low-cost development tool for use with Microchip's PIC17C42 microcontroller. It comes complete with the PIC EDP-17 Evaluation/Demonstration/Programmer board, lab power cable, PIC "Quick Start" Sample product kit, PICASM-17 Assembler software, documentation, and source code for demonstration programs. The kit allows the user to quickly familiarize and experiment with the PIC17C42 chip.

The EDP-17 board allows the PIC17C42 to execute code from either two external 8-bit wide EPROMs, or to execute in microcomputer (single-chip) mode from its own internal EPROM program memory. In addition, the system provides a **PROGRAMMING MODE**, in which the PIC17C42 can program its own internal on-chip memory by reading data from two external EPROMs. The system is ideal for evaluation and quick prototyping of simple applications.

The user writes and assembles source code on any PC compatible machine. A standard EPROM programmer is used to place the PIC17C42 binary code into two standard 27C64 8-bit EPROMs. The user can then execute and verify the code in external execution mode. Once verified, the code can be programmed into the PIC17C42 with the push of a button. Finally, the user's application can tried stand-alone with the PIC17C42 executing from its own internal memory.

An on board, pre-programmed PIC16C57 co-processor provides a variety of stimulus signals to the PIC17C42 allowing the user to exercise the serial port, timer, capture registers, and other peripheral functions. For convenience, a solderless breadboard with easy access to all PIC17C42 signals is provided for quick prototyping.

OPERATION

On power-up or after system RESET the PIC17C42 is put into one of three modes based on a DIP switch setting:

- External execution mode (EXTEX) in which the PIC17C42 executes from external memory.
- Internal execution mode (INTEX) where the PIC17C42 operates in the microcontroller mode and executes from internal memory.
- Programming mode (PROGRAM) in which the PIC17C42 programs its own internal EPROM and its configuration fuses (auto-programming).

On power-up or after a system RESET the PIC16C57 senses the mode select switches and generates the appropriate sequence of startup signals to the PIC17C42. LED's indicate which modes are selected. The PIC16C57 also controls data buffers and latches associated with the programming and external execution modes.

Programming mode (PROGRAM) operation

In this mode the PIC17C42 reads the two external EPROMs, RAM memory, or ROM emulator, one word at a time, and programs the corresponding location in its on-chip EPROM. Programming status LED's indicate progress of the programming activity.

External execution mode (EXTEX) operation

In this mode, the PIC17C42 executes code from the two external 8-bit wide memories. The user can use 27HC64 or compatible EPROMs, 21256 or compatible SRAMs or 28HC64 EEPROMs. To use this mode, the user must configure the PIC17C42 in microprocessor or extended microcontroller mode.

In external execution mode the PIC17C42 is connected to the 3-digit LED display which may be used to communicate with a terminal. Selected pins of the PIC17C42 pins are connected to the PIC16C57 for stimulus input

Reset control

Two reset switches are provided for either a complete system reset or a PIC17C42 reset. The system reset switch resets the PIC16C57 which in turn issues the proper reset signals to the PIC17C42 depending on the mode control switch settings. The **RESET 17C42** key may be used to reset the PIC17C42 at any time.

Clock circuitry

Two crystal clock oscillators are provided on the system. The 1 MHz oscillator (Y2) provides the clock source for the PIC16C57. In the external and internal execution modes the 10 MHz oscillator (Y1) provides the clock source for the PIC17C42. Optionally, the crystal oscillators can be removed and an external clock source can be provided using turrets J1 and J3 for their PIC17C42 and the PIC17C57 respectively.

Display module

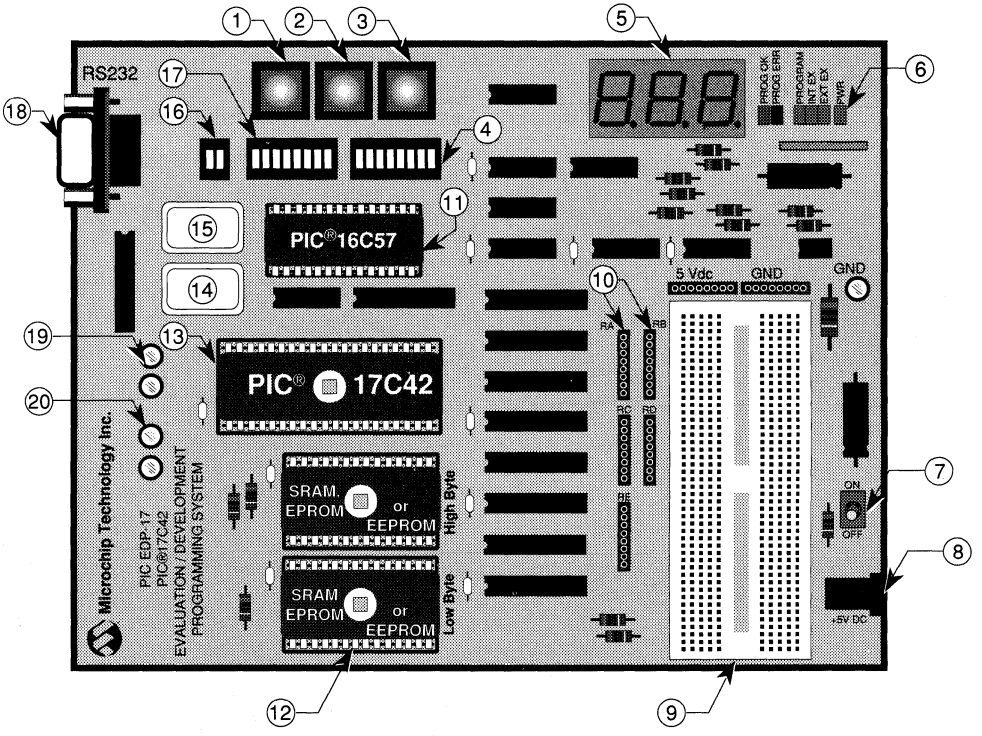
A three-digit seven-segment display module is provided on board for use by the application's program. RB5, RB6 and RB7 outputs of the PIC17C42 controls the clock, data and enable outputs to the display.

PIC 17C42 Demonstration Software

- **DEMO1.ASM:** Displays hex digits "0" through "F" on LED display at 1 second intervals.
- **DEMO2.ASM:** Displays digits "000" through "255" on LED display.
- **DEMO3.ASM:** Configures and exercises PIC 17C42 serial port in full duplex mode. Transmits a preset pattern of data at a one second interval. Displays incoming data on the LED display.
- **Subroutines:** Binary to BCD, Serial port RX, Serial port TX, Delays (10 msec, 1 second), Hex to 7-segment convert, 7-segment display.

PIC 16C57 Demonstration Software

- **Stimulus to PIC17C42:** Serial async, serial sync, baud rate generation, interrupt pulses, timer clock generation, capture pulse generation.
- Control of PIC17C42 PROGRAM modes.
- Control of PIC17C42 RESET & EXECUTE modes.



PIC EDP-17 DEMONSTRATION / EVALUATION / PROGRAMMER BOARD FUNCTIONS

1	Event trigger switch to PIC17C42. Causes the PIC16C57 microcontroller to generate the stimulus event selected by #17.	11	Provides RESET and stimulus signals to PIC17C42. PIC16C57 microcontroller firmware can be re-programmed by the end user.
2	PIC17C42 microcontroller RESET switch.	12	PIC17C42 external memory sockets (2). For external program execution, or for programming of internal EPROM from external devices.
3	System RESET switch.	13	PIC17C42 device (socketed).
4	Fuse setting for PIC17C42 programming.	14	PIC17C42 crystal, 10 Mhz. (socketed).
5	7-segment LED display for PIC17C42.	15	PIC16C57 crystal, 1 Mhz. (socketed).
6	PROGRAM, EXECUTION, and POWER status LED indicators.	16	PIC17C42 Execution mode switch (EXT, INT, or PROGRAM).
7	ON / OFF power switch.	17	PIC16C57 I/O stimulus mode selection.
8	Lab +5VDC power supply jack (male).	18	RS232 DB9 connector to PIC17C42.
9	Solderless prototype board area (1.25" x 3.5").	19	External clock oscillator input for PIC17C42.
10	PIC17C42 I/O & Bus lines (RA,RB,RC,RD,RE).	20	External clock oscillator input for PIC16C57.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBER	DESCRIPTION
DV173001	PICPAK-17 PIC17C42 Evaluation / Demonstation / Programmer System.

PICPRO-II™

PIC®16C5x Microcontroller EPROM Programmer Unit

SYSTEM FEATURES

EPROM Programmer System

- PICPRO-II EPROM Programmer unit for the PIC16C5X Microcontroller family.
- Operates as a Stand-alone Unit or in Conjunction with a PC Compatible host system.
- READS, PROGRAMS, and VERIFIES in Stand-alone mode.
- Non-Volatile Program Memory for stand-alone or field use where PC is not available.
- PC Host Software provides file display and editing, and transfer to and from Programmer unit.

SYSTEM DESCRIPTION

PICPRO-II EPROM Programmer

The PICPRO-II Programmer system provides the product developer with the ability to program user software into PIC 16C5x EPROM microcontrollers.

The programmer unit comes complete with accessories to be used with the PC host computer. Supplied are interface cables and connectors to a standard PC parallel printer port (LPT), a wall mount power supply unit, and host operating software (PP2.EXE).

The PICPRO-II Programmer will work in either stand-alone mode, or in PC host connected mode. Connected to a PC host, many more features are available to the user.

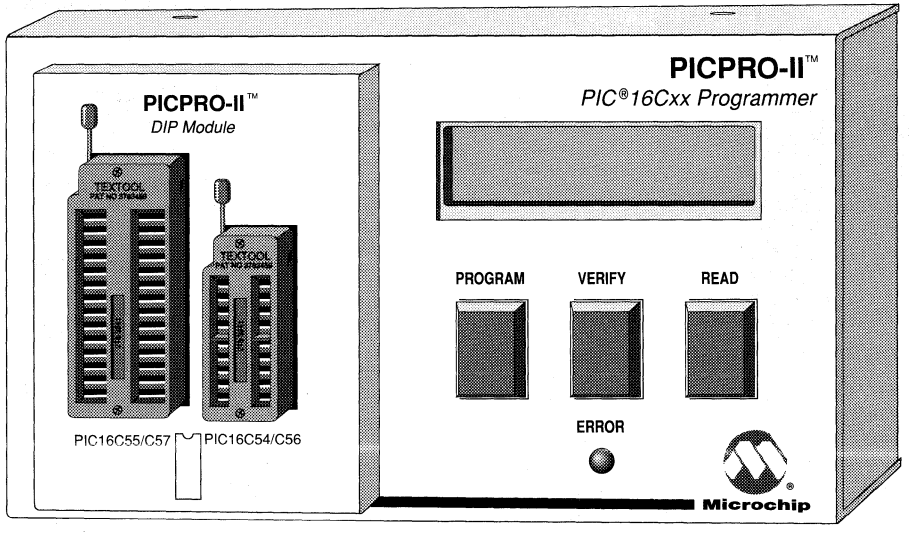


FIGURE 1: PICPRO-II UNIT WITH DIP ADAPTER

STAND-ALONE MODE

Stand-alone mode is useful in situations where a PC may not be available or even required, such as in the field or in a lab production environment. In stand-alone mode the following programming functions are available:

VERIFY

VERIFY performs two functions. For a programmed part, the device in the programming socket will be compared to the program data stored in internal EEPROM. If the data and fuse settings are correct, VERIFIED will be displayed. VERIFY will also confirm that erased parts are blank. A device in the socket will display ERASED if all programmable locations are blank.

PROGRAM

In stand-alone mode, devices inserted into the programmer socket will be programmed with data currently stored in EEPROM memory. Pressing the PROGRAM key will cause the unit to program and verify both the program memory and the device fuses. If all program successfully, PGM OKAY will be displayed.

READ

A pre-programmed device placed in the programmer socket can be read into the programmer unit by pressing the READ key. Program and fuse data will be read and stored into internal EEPROM. Various options exist with the READ function.

PC HOST CONNECT MODE

When the PICPRO-II is connected to a host PC system, many more options and conveniences are available to the user. Host mode allows full interactive control over the PICPRO-II unit. A full screen, user-friendly software program (PP2.EXE) is provided to fully assist the user.

As in stand-alone mode, parts may be Read, Programmed, Blank checked, and Verified. Also, all fuses and ID locations may be specified. In addition, other features available in host-mode are:

Editing

A large screen buffer editing facility allows the user to change and program location in either hexadecimal or ASCII (text) modes. Complete program and fuse data can be loaded and saved to DOS disk files. Files generated by the PICALC™ Assembler program are directly loadable into programmer memory.

VDD and VPP

The programming environment voltage settings of VDD max, VDD min, and VPP can be set and altered only on PC host mode. The voltage settings allow the user to program the part in the environment that the part will be used. The part will be programmed at VDD max and verified at VDD min. VPP is the programming voltage.

Parts Serialization

In PC host mode, the user can select up to 8 locations to be programmed with a serial number or random security code. Provisions for setting the address ranges, and starting serial numbers are provided. The serial number can use either incrementing serialization, or a random number sequence. Serialization is also permitted with parts already code-protected in the first 64 locations. This allows end user customization while keeping proprietary, the program software code.

PICPRO-II SPECIFICATIONS

Device Types	**PIC16C54, 16C55, 16C56, 16C57 (oscillators: RC, XT, HS, LP)**
Capacity	**Program and fuse information for one device to 2Kx12 (stored in non-volatile EEPROM).**
Enclosure	**6.5"L x 3.75"x 1.25" epoxy coated aluminum, rubber feet**
Weight	**14 oz.**
Power	**±20 to 35VDC. External AC/DC power supply included. Lab power cord with standard banana jacks.**
Display	**8 character LCD**
Interface	**Host PC Printer Port (auto-seeking of LPT1-LPT4 port)**
Adapters	**18 and 28 Pin ZIF DIP (standard) 18 and 28 lead SOIC (optional)**
Software	**PP2.EXE provided on 5.25" MSDOS 360K diskette.**
Accessories	**DB25-RJ11 adapter for host PC, RJ11 cable to PICPRO-II, User Manual.**

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

PART NUMBERS	DESCRIPTIONS
PG165001	Programmer Kit with 100 volt power supply (Note 1)
PG165002	Programmer Kit with 110 volt power supply (Note 2)
PG165003	Programmer Kit with 220 volt power supply (Note 3)
PG165004	Programmer Kit with 240 volt power supply (Note 4)
AC164009	Optional 18 and 28 - lead SOIC adapter

NOTES:
1) Used primarily in Japan
2) Used primarily in North, Central and South America, Taiwan and Korea
3) Used primarily in continental Europe, Hong Kong, Singapore and Scandinavia
4) Used primarily in England, Ireland, Scotland and R.O.C. (China)

Notes:

PRO MASTER ™

CMOS PIC® Microcontroller Programmer Unit

SYSTEM FEATURES

EPROM Programmer System

- PRO MASTER Programmer unit for the PIC16CXX, PIC17CXX Microcontroller family.
- Operates as a Stand-alone Unit or in Conjunction with a PC Compatible host system.
- READS, PROGRAMS, and VERIFIES in Stand-alone mode.
- PC Host Software provides file display and editing, and transfer to and from Programmer unit
- Communication Via RS-232

SYSTEM DESCRIPTION

PRO MASTER Programmer

The PRO MASTER Programmer system provides the product developer with the ability to program user software into PIC16CXX, PIC17CXX CMOS microcontrollers.

The programmer unit comes complete with accessories to be used with the PC host computer. Supplied are interface cables and connectors to a standard PC serial port, a universal input power supply unit, and host operating software.

The PRO MASTER Programmer will work in either stand-alone mode, or in PC host connected mode. Connected to a PC host, many more features are available to the user.

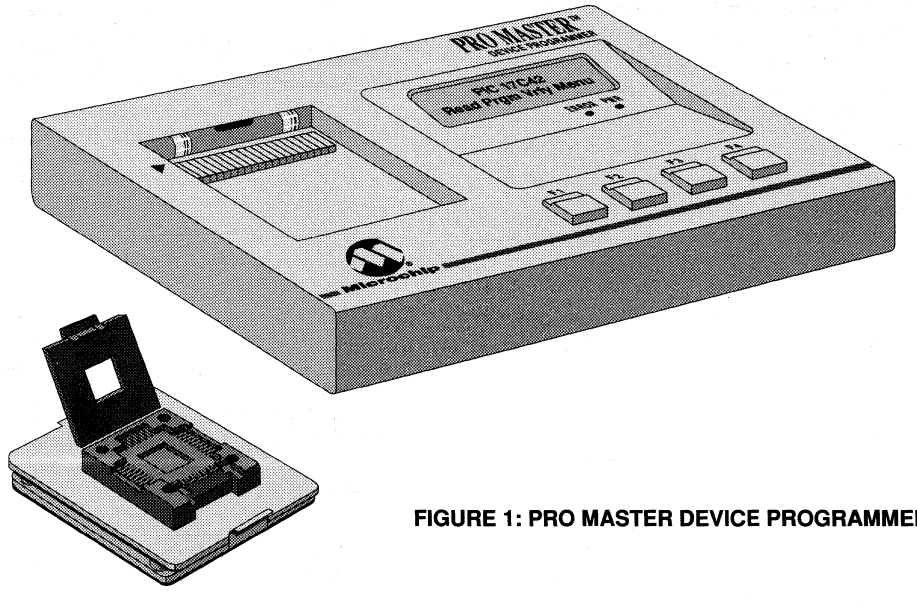


FIGURE 1: PRO MASTER DEVICE PROGRAMMER

STAND-ALONE MODE

Stand-alone mode is useful in situations where a PC may not be available or even required, such as in the field or in a lab production environment. In stand-alone mode the following programming functions are available:

VERIFY

VERIFY performs two functions. For a programmed part, the device in the programming socket will be compared to the program data stored in internal memory. If the data and fuse settings are correct, VERIFIED will be displayed. VERIFY will also confirm that erased parts are blank. A device in the socket will display ERASED if all programmable locations are blank.

PROGRAM

In stand-alone mode, devices inserted into the programmer socket will be programmed with data currently stored in memory. Pressing the PROGRAM key will cause the unit to program and verify both the program memory and the device fuses. If all program successfully, PGM OKAY will be displayed.

READ

A pre-programmed device placed in the programmer socket can be read into the programmer unit by pressing the READ key. Program and fuse data will be read and stored into internal memory. Various options exist with the READ function.

PC HOST CONNECT MODE

The PRO MASTER provides a very user friendly user interface which allows complete control over the programming session.

The PRO MASTER host software is a DOS windowed environment with full mouse support to allow the user to point and click when entering commands.

The Host Software communicates with the PRO MASTER via the serial port of the PC. Any of the four (COM 1-4) ports may be used. The communication is done at 19200baud to insure fast throughput. Communication will be established with the PRO MASTER Device Programmer prior to any transfers taking place.

Serialization is done by generating a serialization file, and then using that file to serialize locations in the PIC microcontroller. Once a serialization file is generated, it may be used over different programming sessions. Serial numbers are automatically marked as used when a PIC is programmed successfully with that serial number.

Complete control over the programming environment is also provided. Control over the programming and verify voltage of Vdd insures that the PIC will perform in the desired environment. Programming (Vpp) voltage is also adjustable to insure complete compatibility with future programming algorithms.

PRO MASTER™ SPECIFICATIONS

Device Types	**PIC16C54, 16C55, 16C56, 16C57, PIC16C71, PIC17C42**
Capacity	**Program and fuse information for one device to 32Kx16 .**
Enclosure	**9.0"L x 6.5"x 1.5" epoxy coated aluminum, rubber feet**
Weight	**16 oz.**
Power	**±5V@ 500 mA. External AC/DC power supply included.**
Display	**20 character x 2 line LCD**
Interface	**Host PC Serial Port (COM 1-4)**
Adapters	**Support current package types.**
Software	**DOS executable provided on disk.**
Accessories	**DB9-DB8 Serial Port Cable for host PC, User Manual.**

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the listed sales offices.

SOCKET PART NUMBER	DESCRIPTION
AC164001	PIC16C54 thru C57 18 & 28 LD PDIP Socket Module
AC164002	PIC16C54 thru C57 18 & 28 LD SOIC Socket Module (future release)
AC164004	PIC16C71 18 Lead PDIP Socket Module
AC164005	PIC16C71 18 Lead SOIC Socket Module
AC174001	PIC17C42 40 Lead PDIP Socket Module
AC174002	PIC17C42 44 Lead PLCC Socket Module (future release)
AC174003	PIC17C42 44 Lead QFP Socket Module (future release)

PROGRAMMER PART NUMBER	DESCRIPTION
PG007001	Programmer Kit as described above
PG007002	Programmer Kit without power supply

(Target Socket Module must be specified, see notes)

Note: Only one socket module is included with shipment of Pro Master Programmer. Socket module must be specified at time of order entry. Order by using individual socket module part number above. Additional socket modules may be purchased separately.

SECTION 3
SERIAL EEPROM PRODUCT SPECIFICATIONS

Microchip

24C01A

1K (128 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Organized as one block of 128 bytes (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention >40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

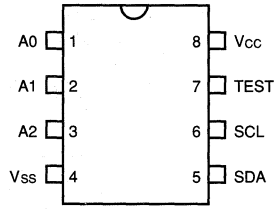
DESCRIPTION

The Microchip Technology Inc 24C01A is a 1K bit Electrically Erasable PROM. The device is organized as 128 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Up to eight 24C01As may be connected to the two wire bus. The 24C01A is available in the standard 8-pin DIP and a surface mount SOIC package.

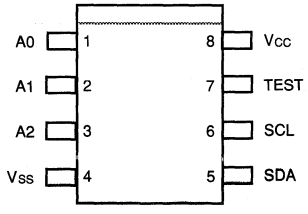
3

PIN CONFIGURATION

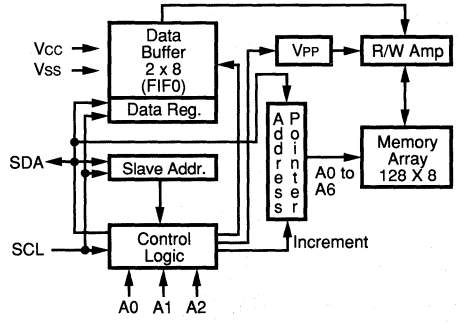
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss ..... -0.3 V to +7 V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .... +300°C
ESD protection on all pins ..... 4 kV

***Notice**: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Test	Tie to Vcc or Vss
Vcc	+5 V Power Supply

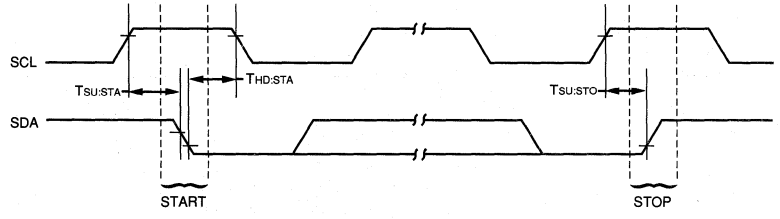
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = 0°C to 70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = (I) and (E)
read cycle	ICCR		750	µA	Vcc = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

BUS TIMING START/STOP

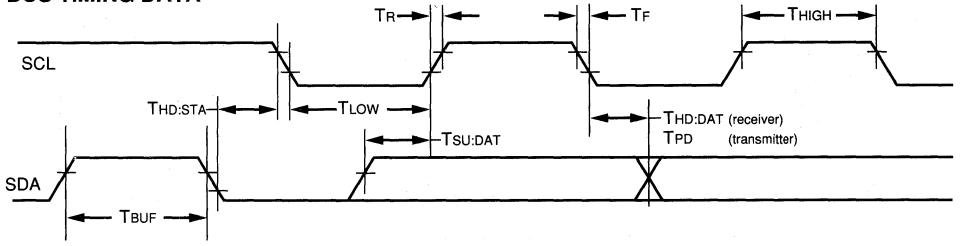


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written
Endurance	---	100,000			E/W Cycles	

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C01A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C01As can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus but require different device codes than the 24C01A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

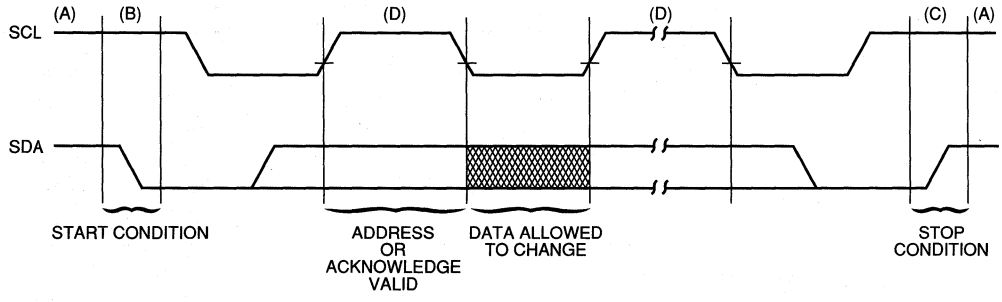
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C01A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

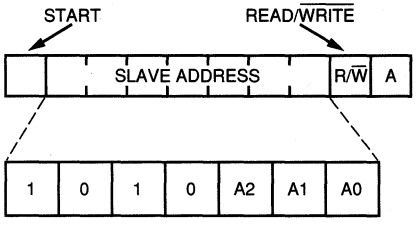
The chip address inputs A0, A1 and A2 of each 24C01A must be externally connected to either Vcc or ground (Vss), assigning to each 24C01A a unique 3-bit address. Up to eight 24C01As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 24C01A.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C01A, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 24C01A. (See Figure 2.)

The 24C01A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 24C01A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C01A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01A. The most significant bit of the word address is a "Do Not Care" value for the 24C01A. After receiving the acknowledge of the 24C01A, the master device transmits the data word to be written into the addressed memory location. The 24C01A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C01A. (See Figure 3).

PAGE PROGRAM MODE

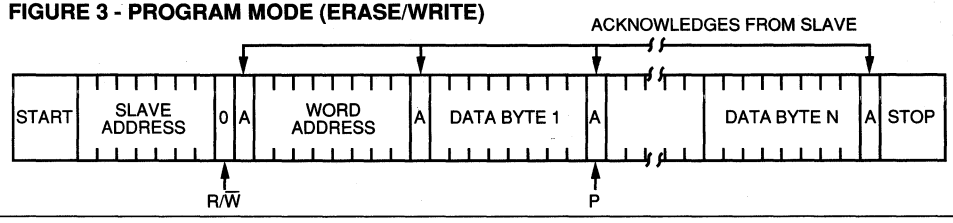
To program the 24C01A, the master sends addresses and data to the 24C01A which is the slave, (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C01A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (One do not care bit and seven address bits.) The 24C01A will generate an acknowledge after every 8-bits received and store them consecutively in a 2-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 24C01A will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 24C01A.

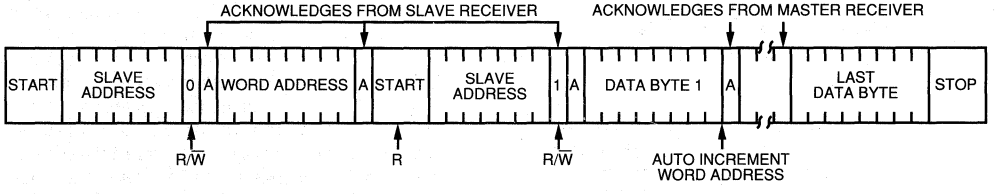
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 24C01A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

In all modes, the address pointer will automatically increment from the end of the memory block (128 byte) back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C01As can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

Test

Must be connected to either Vss or Vcc.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C01A page is 2 bytes long.

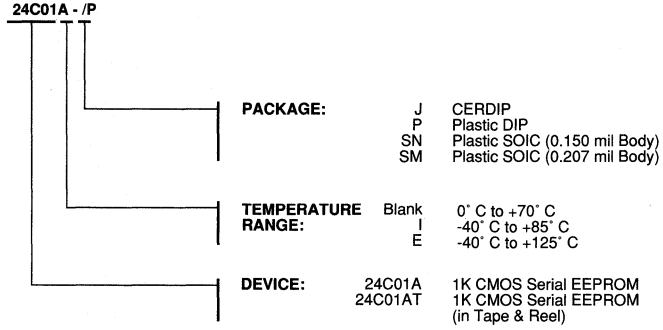
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C01A has only one block (128 bytes).

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

24C02A

2K (256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Organized as one block of 256 bytes (256 x 8)
- Hardware write protect for upper 1K (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention >40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

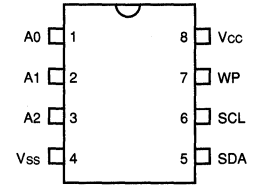
DESCRIPTION

The Microchip Technology Inc. 24C02A is a 2K bit Electrically Erasable PROM. The device is organized as 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature allows a write protection for the upper 1K (128 x 8). The 24C02A also has a page-write capability for up to 2 bytes of data. Up to eight 24C02As may be connected to the two wire bus. The 24C02A is available in the standard 8-pin DIP and a surface mount SOIC package.

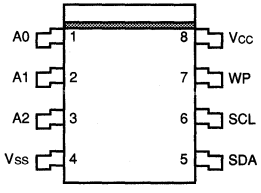
3

PIN CONFIGURATION

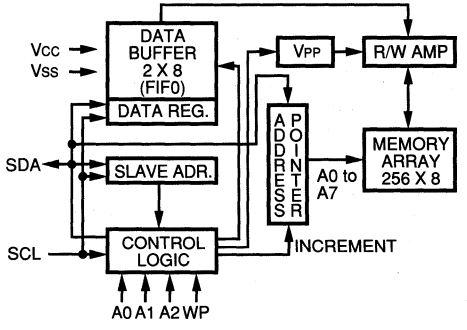
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+5 V Power Supply

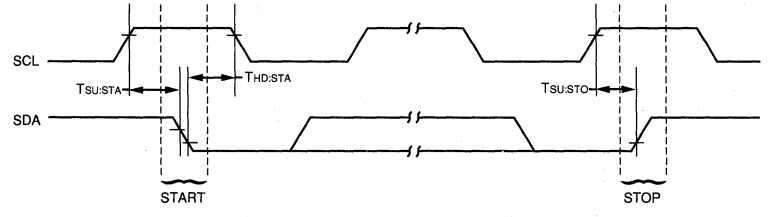
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) TAMB = 25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = 0°C to 70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = (I) and (E)
read cycle	ICCR		750	µA	Vcc = 5 V, Tamb = (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

BUS TIMING START/STOP

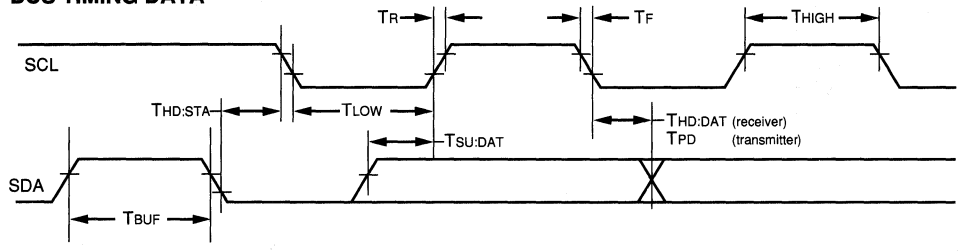


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written
Endurance	---	100,000			E/W Cycles	

Note 1: As transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C02A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C02A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C02As can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 24C02A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a STARTcondition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

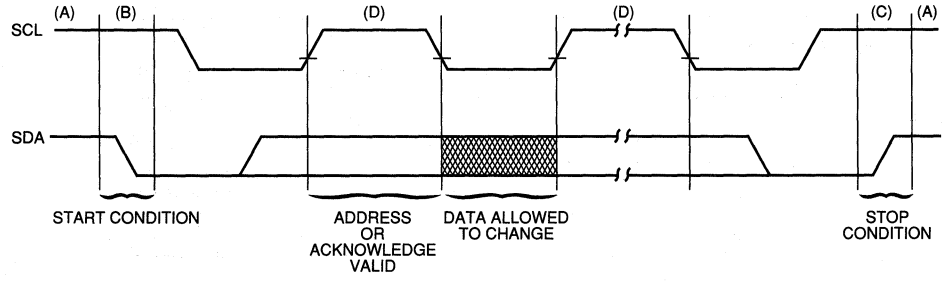
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C02A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

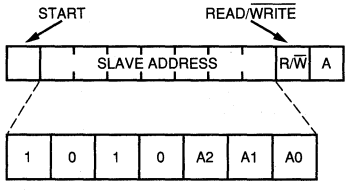
The chip address inputs A0, A1 and A2 of each 24C02A must be externally connected to either Vcc or ground (Vss), assigning to each 24C02A a unique 3-bit address. Up to eight 24C02As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 24C02A.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C02A, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 24C02A. (See Figure 2.)

The 24C02A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 24C02A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C02A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C02A. After receiving the acknowledge of the 24C02A, the master device transmits the data word to be written into the addressed memory location. The 24C02A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C02A. (See Figure 3.)

PAGE PROGRAM MODE

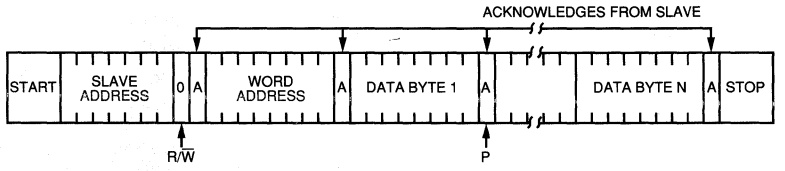
To program the 24C02A, the master sends addresses and data to the 24C02A which is the slave. (See Figure 3.) This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C02A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 24C02A will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 24C02A will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the 24C02A is connected to Vcc (+5 V). The 24C02A will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C02A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

READ MODE

This mode illustrates master device reading data from the 24C02A.

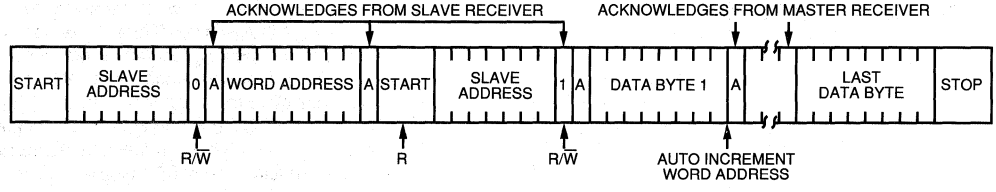
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: although this is a read mode the address pointer must be written to.) During this period the 24C02A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will automatically increment from the end of the memory block (256 byte) back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24C02As can be connected to the bus. These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP Write Protection

This pin must be connected to either Vss or Vcc.

If tied to Vcc, PROGRAM operations onto the upper half of memory (addresses 080—0FF) will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000—0FF).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C02A page is 2 bytes long.

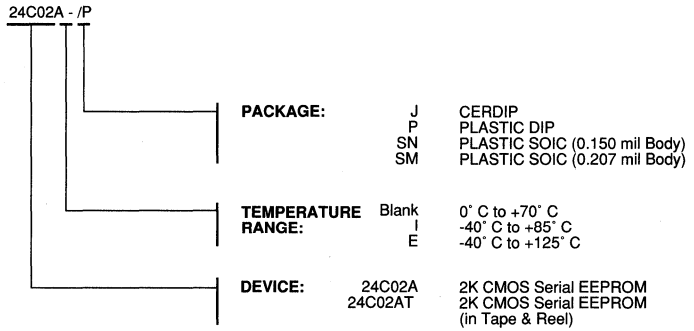
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C02A has only one block (256 bytes).

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

24C04A

4K (512 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Organized as two blocks of 256 bytes (2 x 256 x 8)
- Hardware write protect for upper block
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 1ms write cycle time for single byte
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention >40 years
- 8-pin DIP/SOIC packages
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

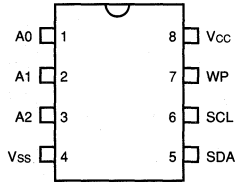
DESCRIPTION

The Microchip Technology Inc. 24C04A is a 4K bit Electrically Erasable PROM. The device is organized as two blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature allows a write protection for the upper 256 byte block. The 24C04A also has a page-write capability for up to 8 bytes of data. Up to four 24C04As may be connected to the two wire bus. The 24C04A is available in the standard 8-pin DIP and 8-pin surface mount SOIC package.

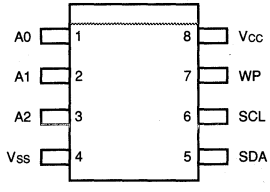
3

PIN CONFIGURATION

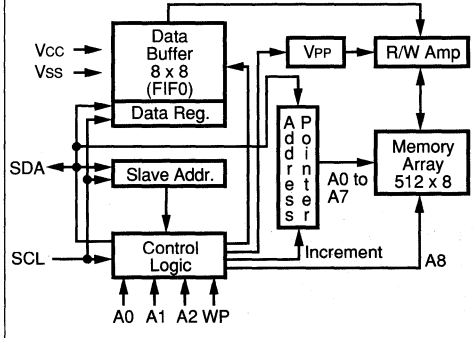
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

***Notice**: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0	No Function, Must be connected to Vcc or Vss
A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+5 V Power Supply

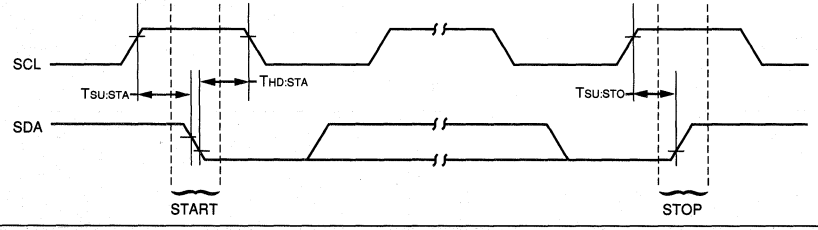
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive: (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = (I) and (E)
read cycle	ICCR		750	µA	Vcc = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles

BUS TIMING START/STOP

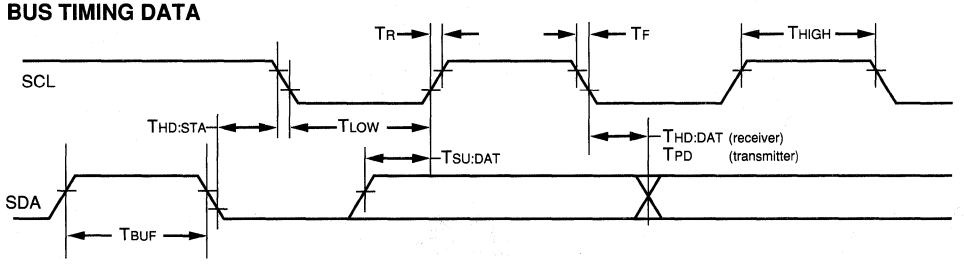


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written
Endurance	---	100,000			E/W Cycles	

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C04A works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 24C04As can be connected to the bus, selected by the A1 and A2 chip address inputs. A0 must be tied to Vcc or Vss. Other devices can be connected to the bus but require different device codes than the 24C04A (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

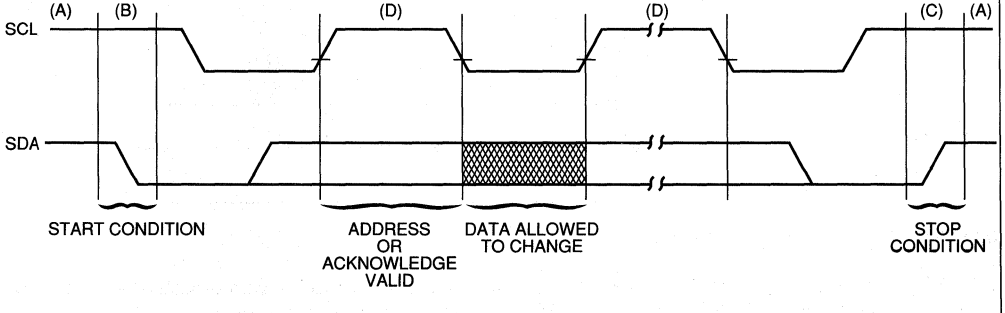
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

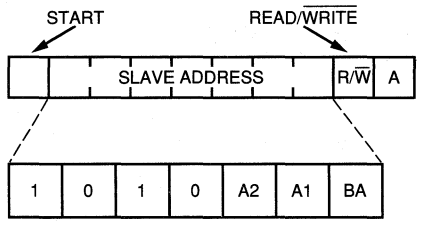
The chip address inputs A1 and A2 of each 24C04A must be externally connected to either Vcc or ground (Vss), assigning to each 24C04A a unique2-bit address. Up to four 24C04As may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 24C04A. A0 is not used and must be connected to either Vcc or Vss.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C04A, followed by the chip address bits A1 and A2. The seventh bit of that byte (BA) is used to select the upper block (addresses 100—1FF) or the lower block (addresses 000—0FF) of the 24C04A.

The eighth bit of slave address determines if the master device wants to read or write to the 24C04A. (See Figure 2.)

The 24C04A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C04A.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C04A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C04A. After receiving the acknowledge of the 24C04A, the master device transmits the data word to be written into the addressed memory location. The 24C04A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C04A. (See Figure 3.)

PAGE PROGRAM MODE

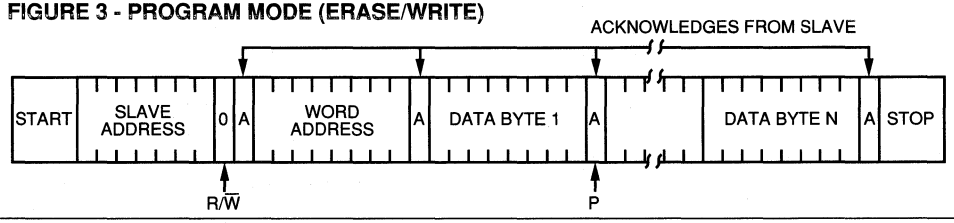
To program the 24C04A, the master sends addresses and data to the 24C04A which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C04A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The BA bit transmitted with the slave address is the ninth bit of the address pointer.) The 24C04A will generate an acknowledge after every 8-bits received and store them consecutively in an 8-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 8 bytes are transmitted by the master, the 24C04A will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to eight) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the 24C04A is connected to Vcc (+5 V). The 24C04A will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted.

READ MODE

This mode illustrates master device reading data from the 24C04A.

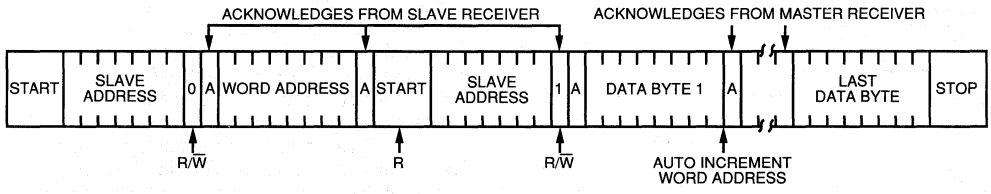
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 24C04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will not increment through a block (256 byte) boundary, but will rotate back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0

This pin must be connected to either Vcc or Vss.

A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four 24C04As can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP Write Protection

This pin must be connected to either Vcc or Vss.

If tied to Vcc, PROGRAM operations onto the upper memory block (addresses 100—1FF) will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000—1FF).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C04A page is 8 bytes long.

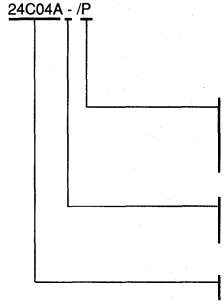
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C04A has two blocks, 256 bytes each.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



PACKAGE:	J	CERDIP
	P	PLASTIC DIP
	SN	PLASTIC SOIC (0.150 mil Body)
	SM	PLASTIC SOIC (0.207 mil Body)
TEMPERATURE RANGE:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
DEVICE:	24C04A	4K CMOS Serial EEPROM
	24C04AT	4K CMOS Serial EEPROM (in Tape and Reel)

Microchip

24C16

16K (8 x 256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Single supply with programming operation down to 4.5 volts
- Low power CMOS technology
  - — 2 mA active current typical
  - — 100 µA standby current at 5.5 V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000 V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP or 14 pin SOIC package
- Available for extended temperature ranges
  - — Commercial: 0°C to + 70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

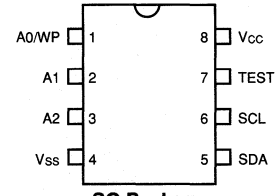
DESCRIPTION

The Microchip Technology Inc. 24C16 is a 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 24C16 also has a page-write capability for up to 16 bytes of data. The 24C16 is available in the standard 8-pin DIP and a 14-pin surface mount SOIC package.

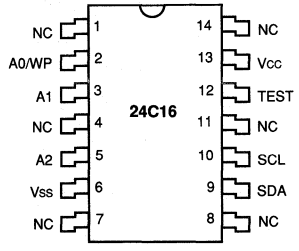
3

PIN CONFIGURATION

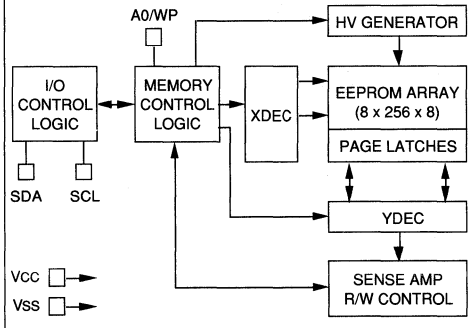
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +6.25 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0/WP	Write Protect Input
A1, A2	Grounded for Normal Operation
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
TEST	Grounded for Normal Operation
Vcc	+5.0 V Power Supply
NC	No Connection

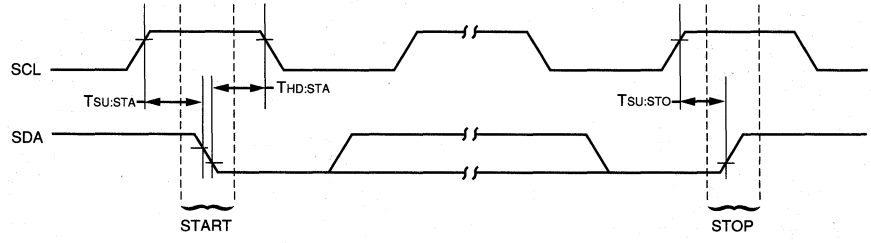
DC CHARACTERISTICS

Vcc = +5.0 V ± 10%
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
A0/WP, SCL and SDA pins: High level input voltage	VIH	.7 Vcc		V	
Low level input voltage	VIL		.3 Vcc	V	
Low level output voltage	VOL		.40	V	IOL = 3.2 mA Vcc = 2.5 V
Input leakage current	ILI	-10	10	µA	VIN = .1 V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		10	pF	Vcc = 5.0 V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICCO		3	mA	Vcc = 5.5 V SCL = 100 KHz
Standby current	ICCS		100	µA	Vcc = 5.5 V SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



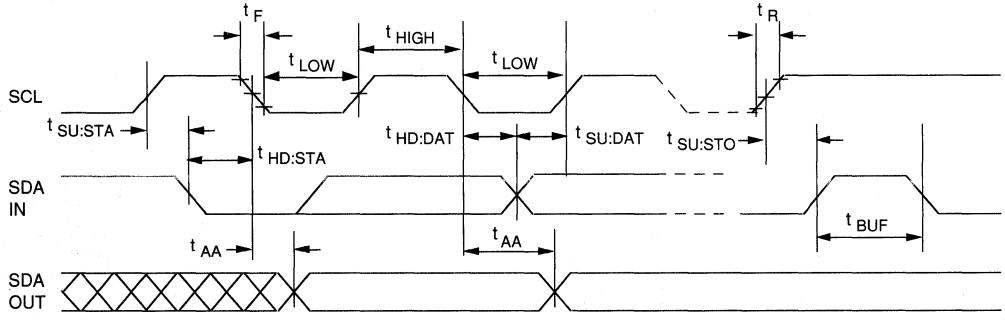
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
STOP condition hold time	THD:STO	4000			ns	
STOP condition setup time	TSU:STO	4700			ns	
Output valid from clock	TAA	300		3500	ns	See Note 1
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Write cycle time	TWR		2	10	ms	Byte or Page mode See Note 2
Endurance	---	100,000			E/W Cycles	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: When writing data to the 24C16, an automatic internal erase then write cycle is executed.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24C16 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C16 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a STARTcondition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

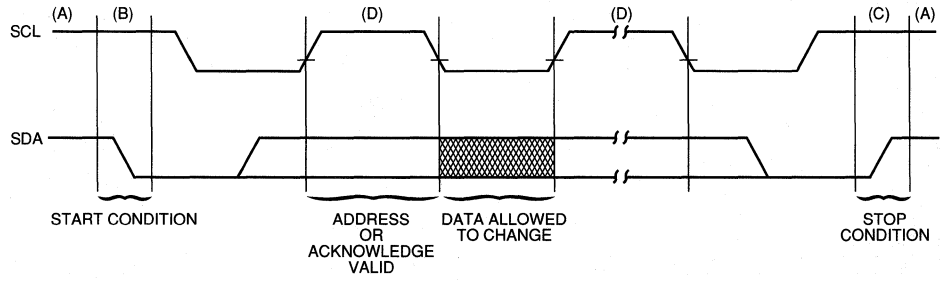
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C16 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

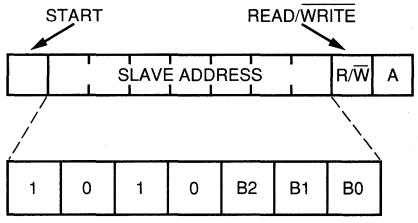
Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24C16 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24C16 per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24C16 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24C16 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start conditionl from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C16. After receiving another acknowledge signal from the 24C16 the master device will transmit the data word to be written into the addressed memory location. The 24C16 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C16 will not generate acknowledge signals. (See Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24C16 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24C16 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (See Figure 4).

FIGURE 3 - BYTE WRITE

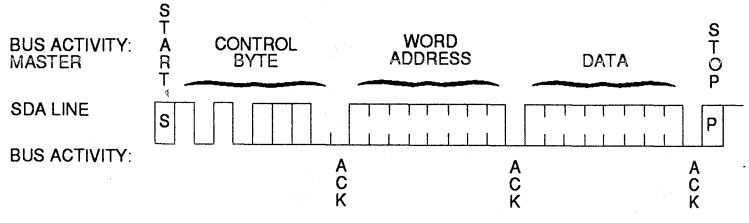


FIGURE 4 - PAGE WRITE

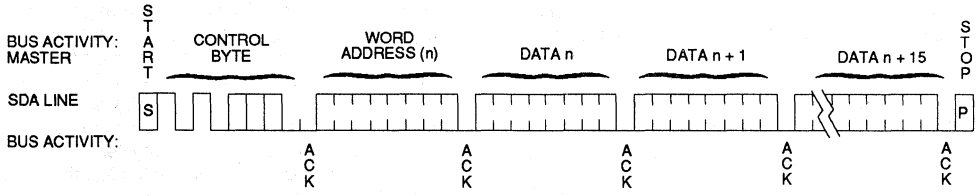


FIGURE 5 - CURRENT ADDRESS READ

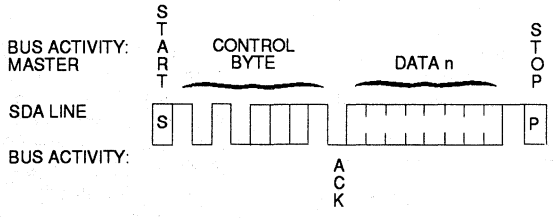


FIGURE 6 - RANDOM READ

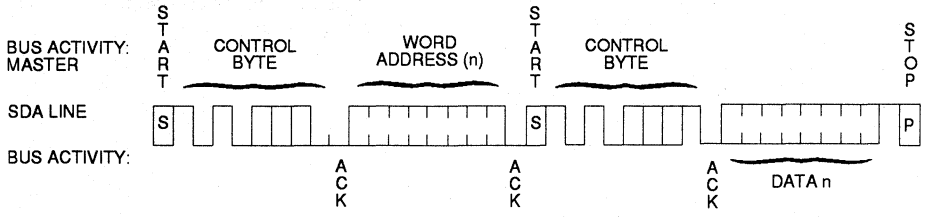
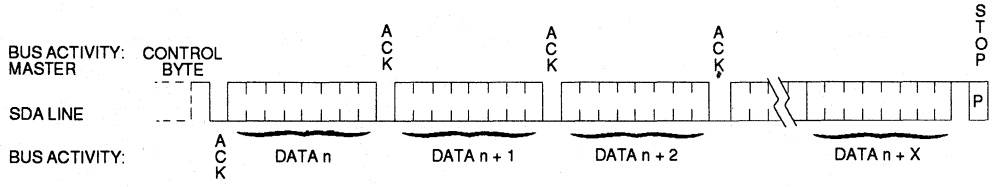


FIGURE 7 - SEQUENTIAL READ



WRITE PROTECTION

The 24C16 can be used as a serial ROM when WP pin is connected to Vcc (+5V). Programming will be inhibited and the entire memory (2K bytes) will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24C16 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C16 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C16 discontinues transmission. (See Figure 5).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C16 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C16 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C16 discontinues transmission. (See Figure 6).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C16 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C16 to transmit the next sequentially addressed 8 bit word. (See Figure 7).

To provide sequential reads the 24C16 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

A0/WP Write Protect Input

This pin must be connected to either Vss or Vcc.

If tied to Vcc, WRITE operations are inhibited. The entire 2K bytes memory will be write-protected. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

This feature allows the user to use the 24C16 as a serial ROM when WP is enabled (tied to Vcc).

A1, A2 Chip Address Inputs

The A1 and A2 inputs are unused by the 24C16. They must be connected to Vss to insure proper device operation.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

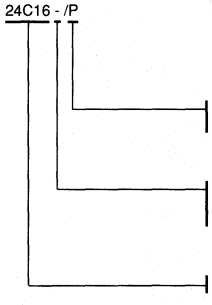
TEST

This pin must be connected to Vss.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



PACKAGE:	P	PLASTIC DIP
	SL	PLASTIC SOIC (0.150 mil Body)
TEMPERATURE RANGE:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
DEVICE:	24C16	16K CMOS Serial EEPROM
	24C16T	16K CMOS Serial EEPROM (in Tape and Reel Form)

Microchip

24LC01

1K (128 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Single supply with operation down to 2.5 volts
- Low power CMOS technology
  - 2 mA active current typical
  - 100 µA standby current at 5.5 V
  - 30 µA standby current at 3.0 V
- Organized as a single block of 128 bytes (128 x 8)
- Two wire serial interface bus
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Factory programming (QTP) available
- ESD protection > 4,000 V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP or SOIC package
- Available for extended temperature ranges
  - Commercial: 0°C to + 70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

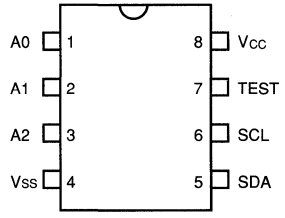
DESCRIPTION

The Microchip Technology Inc. 24LC01 is a 1K bit Electrically Erasable PROM. The device is organized as a single block of 128 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 30 µA and 3 mA respectively. The 24LC01 also has a page-write capability for up to 8 bytes of data. Up to eight 24LC01s may be connected to the two wire bus. The 24LC01 is available in the standard 8-pin DIP and an 8-pin surface mount SOIC package.

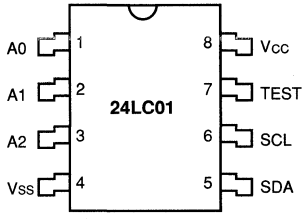
3

PIN CONFIGURATION

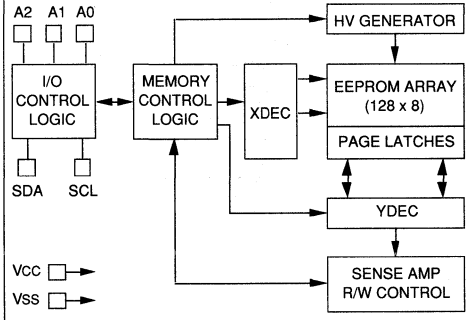
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +6.25 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Test	No Function. Grounded for normal operation
Vcc	+2.5 V to 5.5 V Power Supply

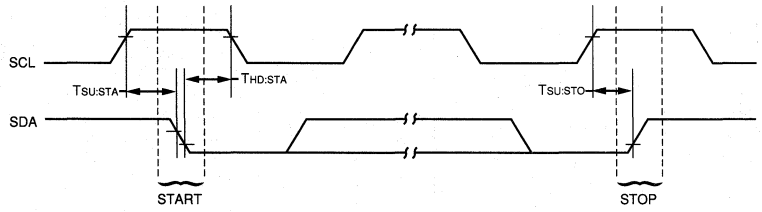
DC CHARACTERISTICS

Vcc = +2.5 V to +5.5 V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
A0, A1, A2, SCL and SDA pins: High level input voltage	VIH	.7 Vcc		V	
Low level input voltage	VIL		.3 Vcc	V	
Low level output voltage	VOL		.40	V	IOL = 3.2 mA Vcc = 2.5 V
Input leakage current	ILI	-10	10	µA	VIN = .1 V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		10	pF	Vcc = 5.0 V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICCO		3	mA	Vcc = 5.5 V SCL = 100 KHz
Standby current	ICCS		100	µA	Vcc = 5.5 V SDA = SCL = Vcc
			30	µA	Vcc = 3.0 V SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

BUS TIMING START/STOP



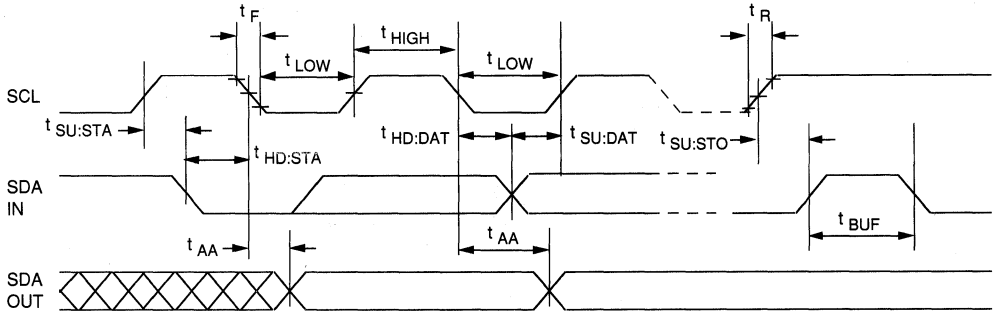
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
STOP condition hold time	THD:STO	4000			ns	
STOP condition setup time	TSU:STO	4700			ns	
Output valid from clock	TAA	300		3500	ns	See Note 1
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Write cycle time	TWR		2	10	ms	Byte or Page mode See Note 2
Endurance	---	100,000			E/W Cycles	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: When writing data to the 24LC01, an automatic internal erase then write cycle is executed.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC01 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC01 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24LC01s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 24LC01 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a STARTcondition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

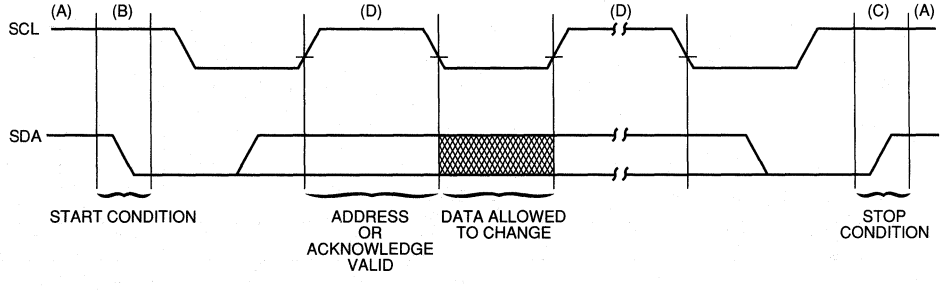
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC01 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

Slave Address

The chip address inputs A0, A1 and A2 of each 24LC01 must be externally connected to either Vcc or ground (Vss), assigning to each 24LC01 a unique 3-bit address. Up to eight 24LC01s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 24LC01.

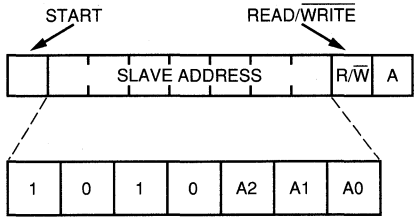
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24LC01, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC01. (See Figure 2.)

The 24LC01 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	Chip Address	1
Write	1010	Chip Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start signal from the master, the device code (4 bits), the chip address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC01. After receiving another acknowledge signal from the 24LC01 the master device will transmit the data word to be written into the addressed memory location. The 24LC01 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC01 will not generate acknowledge signals. (See Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC01 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC01 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (See Figure 4).

FIGURE 3 - BYTE WRITE

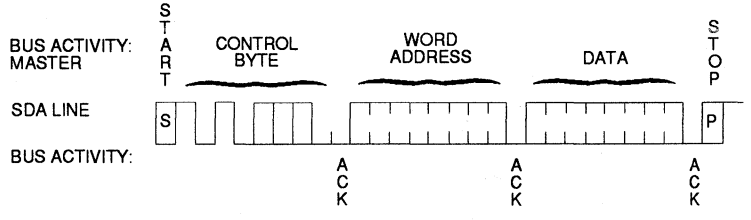


FIGURE 4 - PAGE WRITE

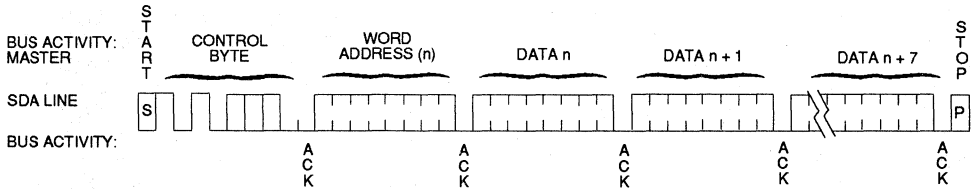


FIGURE 5 - CURRENT ADDRESS READ

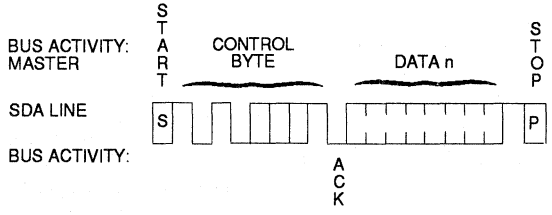


FIGURE 6 - RANDOM READ

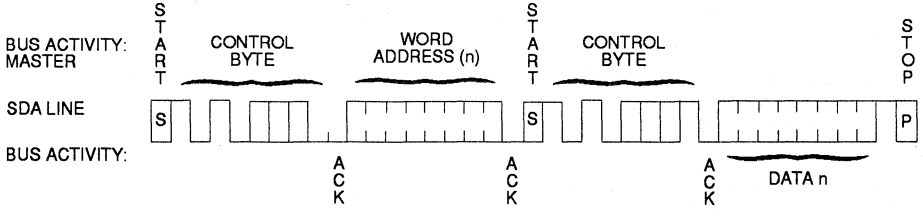
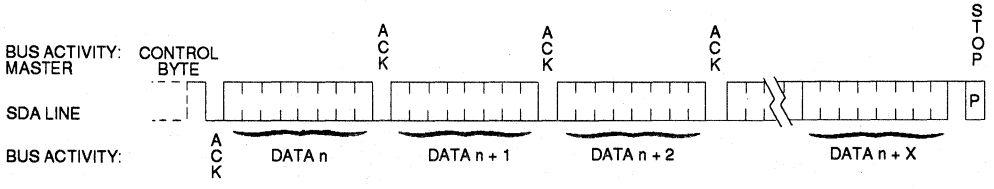


FIGURE 7 - SEQUENTIAL READ



READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC01 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to one, the 24LC01 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01 discontinues transmission. (See Figure 5).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC01 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one. The 24LC01 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01 discontinues transmission. (See Figure 6).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC01 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC01 to transmit the next sequentially addressed 8 bit word. (See Figure 7).

To provide sequential reads the 24LC01 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24LC01 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24LC01s can be connected to the bus. These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

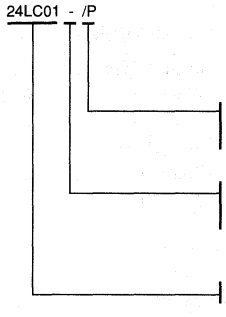
Test

This pin must be connected to Vss for normal operation.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



PACKAGE:	P	PLASTIC DIP
	SN	PLASTIC SOIC (150 mil Body)
	SM	PLASTIC SOIC (207 mil Body)
TEMPERATURE RANGE:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
DEVICE:	24LC01	1K CMOS Serial EEPROM
	24LC01T	1K CMOS Serial EEPROM (in Tape and Reel Form)

Microchip

24LC02

2K (256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Single supply with operation down to 2.5 volts
- Low power CMOS technology
  - 2 mA active current typical
  - 100 μA standby current at 5.5 V
  - 30 μA standby current at 3.0 V
- Organized as a single block of 256 bytes (256 x 8)
- Two wire serial interface bus
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Factory programming (QTP) available
- ESD protection > 4,000 V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP or SOIC package
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

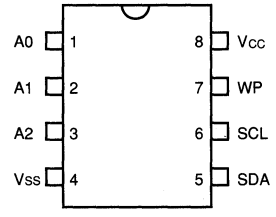
DESCRIPTION

The Microchip Technology Inc. 24LC02 is a 2K bit Electrically Erasable PROM. The device is organized as a single block of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 30 μA and 3 mA respectively. The 24LC02 also has a page-write capability for up to 8 bytes of data. Up to eight 24LC02s may be connected to the two wire bus. The 24LC02 is available in the standard 8-pin DIP and an 8-pin surface mount SOIC package.

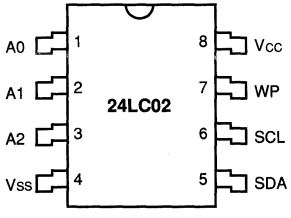
3

PIN CONFIGURATION

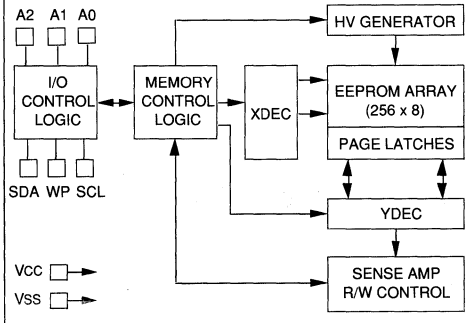
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +6.25 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5 V to 5.5 V Power Supply

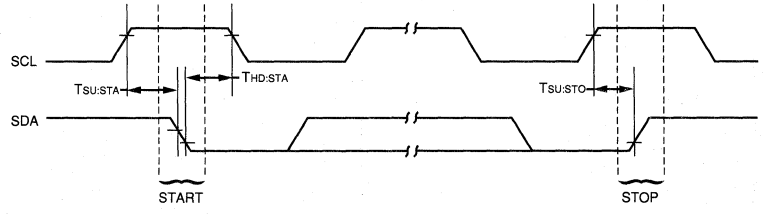
DC CHARACTERISTICS

Vcc = +2.5 V to +5.5 V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
A0, A1, A2, WP, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc		V	
Low level input voltage	VIL		.3 Vcc	V	
Low level output voltage	VOL		.40	V	IOL = 3.2 mA Vcc = 2.5 V
Input leakage current	ILI	-10	10	µA	VIN = .1 V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		10	pF	Vcc = 5.0 V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICCO		3	mA	Vcc = 5.5 V SCL = 100 KHz
Standby current	ICCS		30	µA	Vcc = 3.0 V SDA = SCL = Vcc
			100	µA	Vcc = 5.5 V SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

BUS TIMING START/STOP



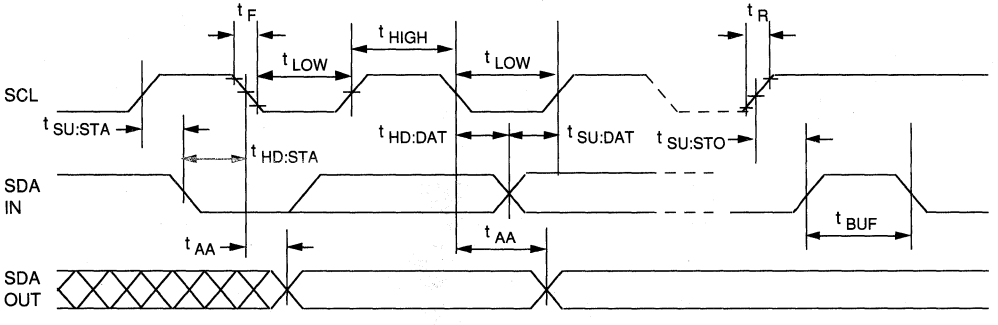
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
STOP condition hold time	THD:STO	4000			ns	
STOP condition setup time	TSU:STO	4700			ns	
Output valid from clock	TAA	300		3500	ns	See Note 1
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Write cycle time	TWR		2	10	ms	Byte or Page mode See Note 2
Endurance	---	100,000			E/W Cycles	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: When writing data to the 24LC02, an automatic internal erase then write cycle is executed.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC02 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC02 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24LC02s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 24LC02 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a STARTcondition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

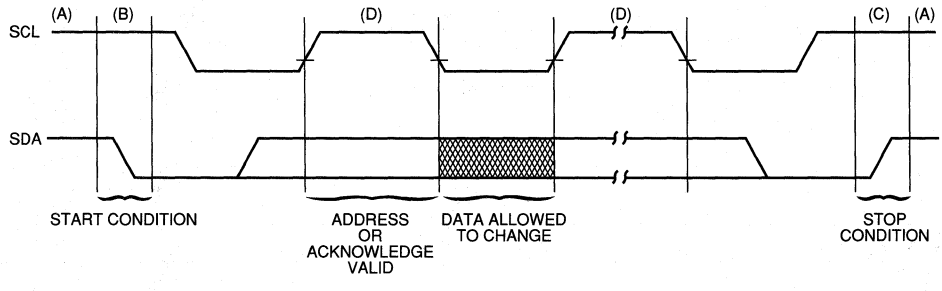
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC02 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

Slave Address

The chip address inputs A0, A1 and A2 of each 24LC02 must be externally connected to either Vcc or ground (Vss), assigning to each 24LC02 a unique 3-bit address. Up to eight 24LC02s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 24LC02.

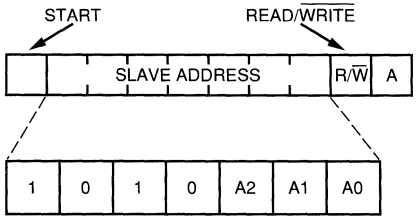
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24LC02, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC02. (See Figure 2.)

The 24LC02 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	Chip Address	1
Write	1010	Chip Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start signal from the master, the device code (4 bits), the chip address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC02. After receiving another acknowledge signal from the 24LC02 the master device will transmit the data word to be written into the addressed memory location. The 24LC02 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC02 will not generate acknowledge signals. (See Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC02 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC02 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (See Figure 4).

FIGURE 3 - BYTE WRITE

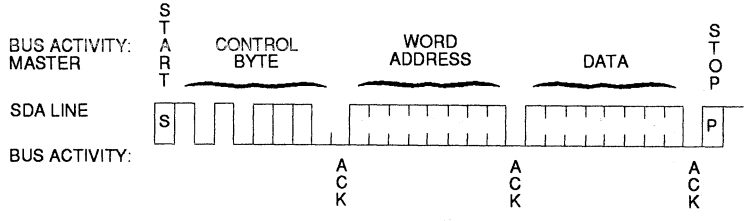


FIGURE 4 - PAGE WRITE

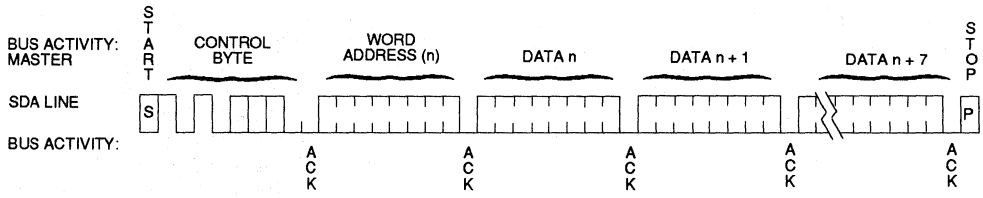


FIGURE 5 - CURRENT ADDRESS READ

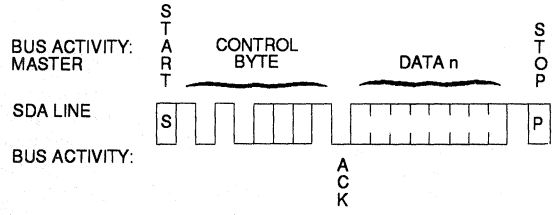


FIGURE 6 - RANDOM READ

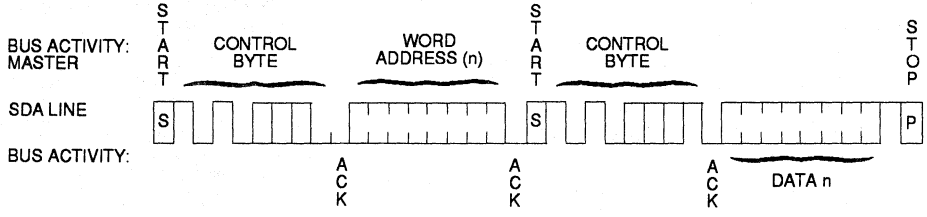
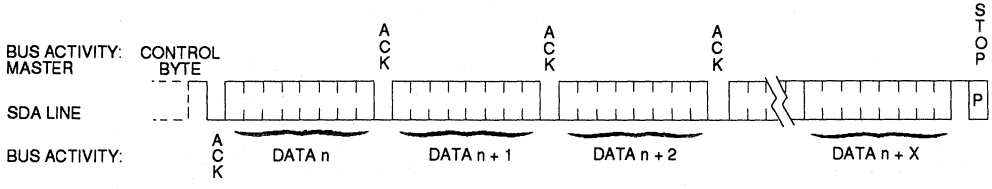


FIGURE 7 - SEQUENTIAL READ



READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC02 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to one, the 24LC02 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC02 discontinues transmission. (See Figure 5).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC02 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one. The 24LC02 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC02 discontinues transmission. (See Figure 6).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC02 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC02 to transmit the next sequentially addressed 8 bit word. (See Figure 7).

To provide sequential reads the 24LC02 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24LC02 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24LC02s can be connected to the bus. These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

WP Write Protect Input

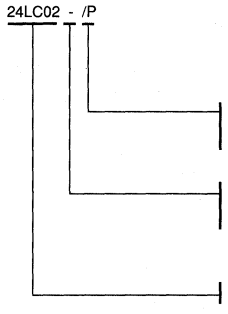
This pin can be connected to either Vss or Vcc. If tied to Vcc, WRITE operations are inhibited. The entire 256 bytes memory will be write-protected. Read operations are possible.

If tied to Vss, normal memory operation is enabled. (Read/write the entire memory 000-0FF).

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



PACKAGE:	P	PLASTIC DIP
	SN	PLASTIC SOIC (150 mil Body)
	SM	PLASTIC SOIC (207 mil Body)
TEMPERATURE RANGE:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
DEVICE:	24LC02	2K CMOS Serial EEPROM
	24LC02T	2K CMOS Serial EEPROM (in Tape and Reel Form)

Microchip

24LC04

4K (512 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Single supply with operation down to 2.5 volts
- Low power CMOS technology
  - 2 mA active current typical
  - 100 µA standby current at 5.5 V
  - 30 µA standby current at 3.0 V
- Organized as 2 blocks of 256 bytes (2 x 256 x 8)
- Two wire serial interface bus
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000 V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP or 14 pin SOIC package
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

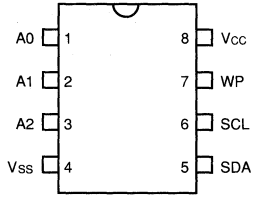
DESCRIPTION

The Microchip Technology Inc. 24LC04 is a 4K bit Electronically Erasable PROM. The device is organized as 2 blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 30 µA and 3 mA respectively. The 24LC04 also has a page-write capability for up to 16 bytes of data. The 24LC04 is available in the standard 8-pin DIP and a 14-pin surface mount SOIC package.

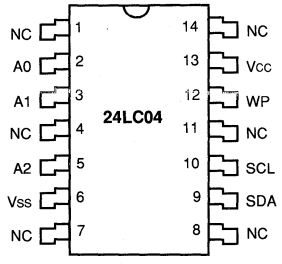
3

PIN CONFIGURATION

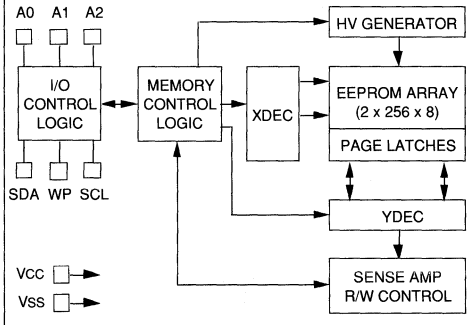
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +6.25 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0	Not Used. Must be tied to Vss.
A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5 V to 5.5 V Power Supply
NC	No Connection

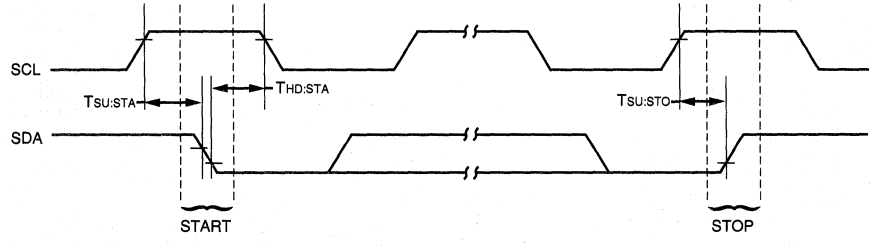
DC CHARACTERISTICS

Vcc = +2.5 V to +5.5 V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
A1, A2, WP, SCL and SDA pins: High level input voltage	VIH	.7 Vcc		V	
Low level input voltage	VIL		.3 Vcc	V	
Low level output voltage	VOL		.40	V	IOL = 3.2 mA Vcc = 2.5 V
Input leakage current	ILI	-10	10	µA	VIN = .1 V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		10	pF	Vcc = 5.0 V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICCO		3	mA	Vcc = 5.5 V SCL = 100 KHz
Standby current	ICCS		30	µA	Vcc = 3.0 V SDA = SCL = Vcc
			100	µA	Vcc = 5.5 V SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

BUS TIMING START/STOP



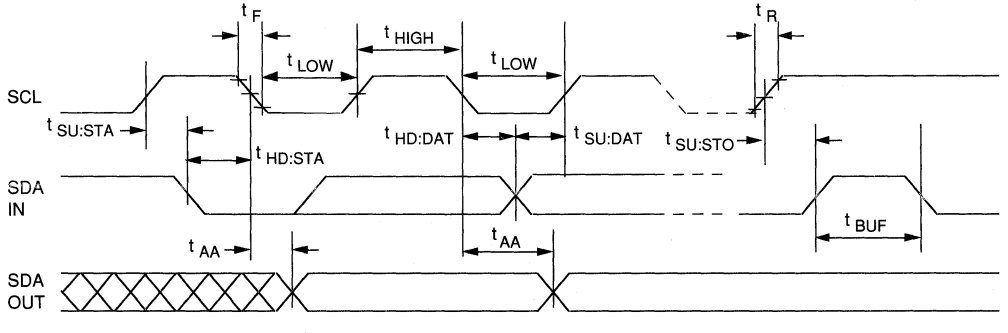
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
STOP condition hold time	THD:STO	4000			ns	
STOP condition setup time	TSU:STO	4700			ns	
Output valid from clock	TAA	300		3500	ns	See Note 1
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Write cycle time	TWR		2	10	ms	Byte or Page mode See Note 2
Endurance	---	100,000			E/W Cycles	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: When writing data to the 24LC04, an automatic internal erase then write cycle is executed.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC04 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC04 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a STARTcondition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

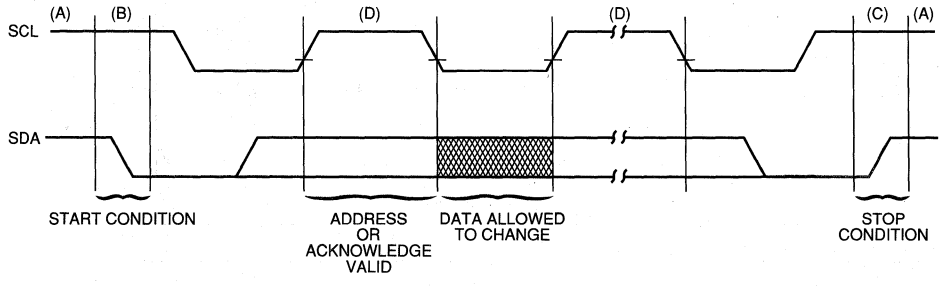
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC04 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

Slave Address

The chip address inputs A1 and A2 of each 24LC04 must be externally connected to either Vcc or ground (Vss), assigning to each 24LC04 a unique 2-bit address. Up to four 24LC04s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 24LC04.

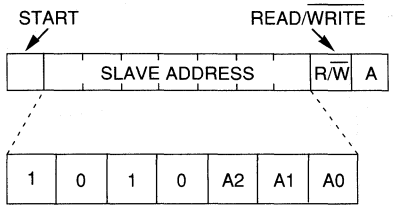
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24LC04, followed by the chip address bits (A1, A2) and the block select bit (A0).

The eighth bit of slave address determines if the master device wants to read or write to the 24LC04. (See Figure 2).

The 24LC04 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip/Block Select	R/$\overline{W}$
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0

FIGURE 2 - CONTROL BYTE ALLOCATION



A0 is the block select bit to select the upper or lower 256-byte block.

A1, A2 are chip address bits.

WRITE OPERATION

Byte Write

Following the start condition from the master, the device code (4 bits), the chip address (2 bits), the block select bit, and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC04. After receiving another acknowledge signal from the 24LC04 the master device will transmit the data word to be written into the addressed memory location. The 24LC04 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC04 will not generate acknowledge signals. (See Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC04 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24LC04 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (See Figure 4).

FIGURE 3 - BYTE WRITE

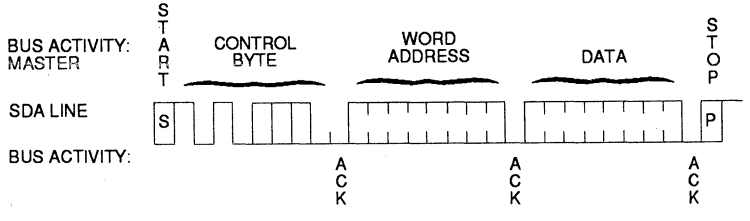


FIGURE 4 - PAGE WRITE

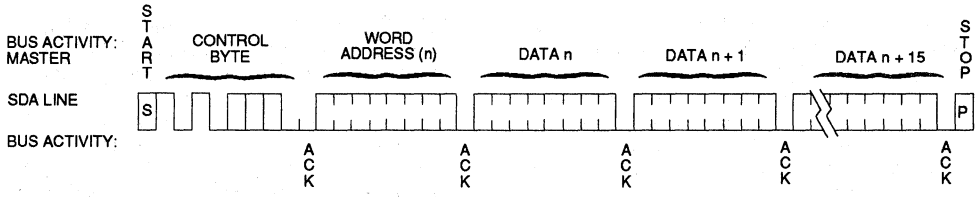


FIGURE 5 - CURRENT ADDRESS READ

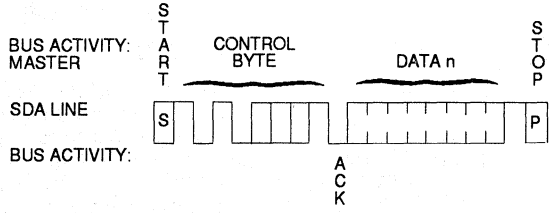


FIGURE 6 - RANDOM READ

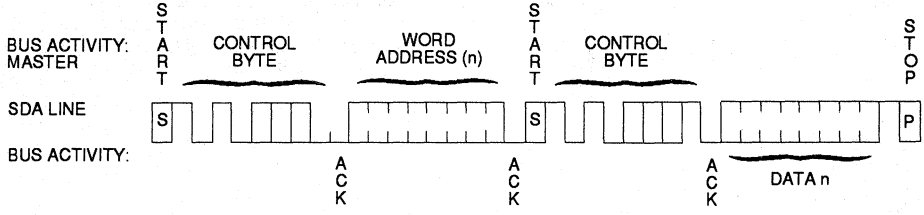
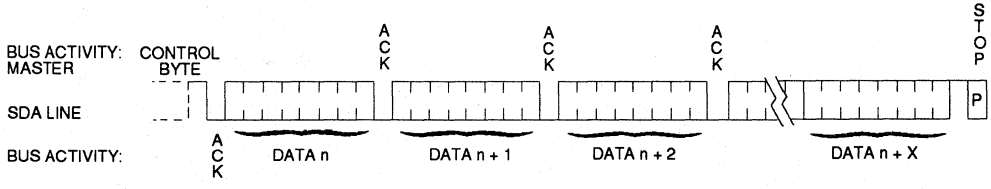


FIGURE 7 - SEQUENTIAL READ



WRITE PROTECTION

The 24LC04 can be used as a serial ROM when WP pin is connected to Vcc (+5V). Programming will be inhibited and the entire memory (512 bytes) will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC04 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC04 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04 discontinues transmission. (See Figure 5).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC04 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one. The 24LC04 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04 discontinues transmission. (See Figure 6).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC04 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC04 to transmit the next sequentially addressed 8 bit word. (See Figure 7).

To provide sequential reads the 24LC04 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24LC04 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

WP Write Protect Input

This pin must be connected to either Vss or Vcc.

If tied to Vcc, WRITE operations are inhibited. The entire 512 bytes memory will be write-protected. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-1FF).

This feature allows the user to use the 24LC04 as a serial ROM when WP is enabled (tied to Vcc).

A0 (Test Pin)

Unused by the 24LC04 during operation. Must be tied to Vss for normal operation.

A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. Up to four 24LC04s can be connected to the bus. These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

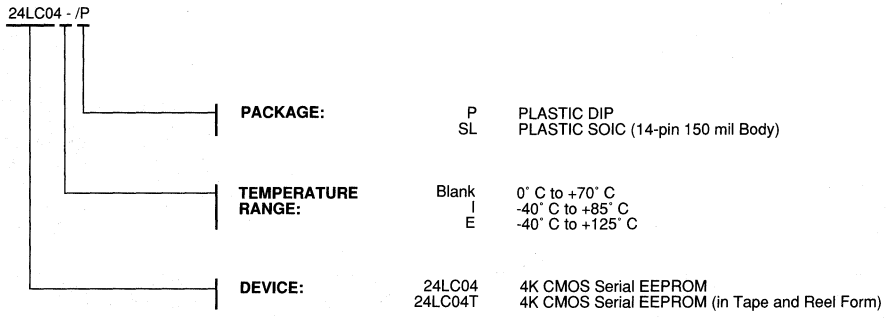
SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

24LC16

16K (8 x 256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Single supply with operation down to 2.5 volts
- Low power CMOS technology
  - — 2 mA active current typical
  - — 100 µA standby current at 5.5 V
  - — 30 µA standby current at 2.5 V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000 V
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8 pin DIP or 14 pin SOIC package
- Available for extended temperature ranges
  - — Commercial: 0°C to + 70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

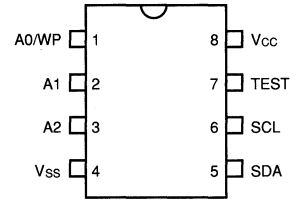
DESCRIPTION

The Microchip Technology Inc. 24LC16 is a 16K bit Electronically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 30 µA and 3 mA respectively. The 24LC16 also has a page-write capability for up to 16 bytes of data. The 24LC16 is available in the standard 8-pin DIP and a 14-pin surface mount SOIC package.

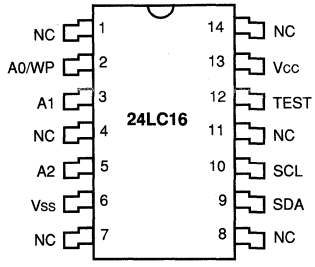
3

PIN CONFIGURATION

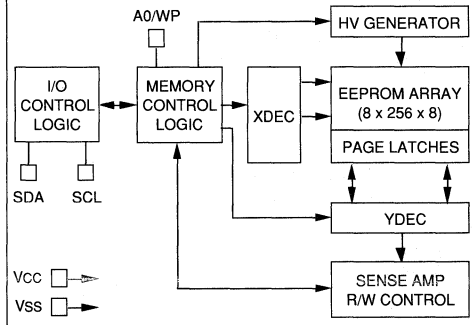
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. V_{SS} .....-0.3 V to +6.25 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0/WP	Write Protect Input
A1, A2	Grounded for Normal Operation
V_{SS}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
TEST	Grounded for Normal Operation
V_{CC}	+2.5 V to 5.5 V Power Supply
NC	No Connection

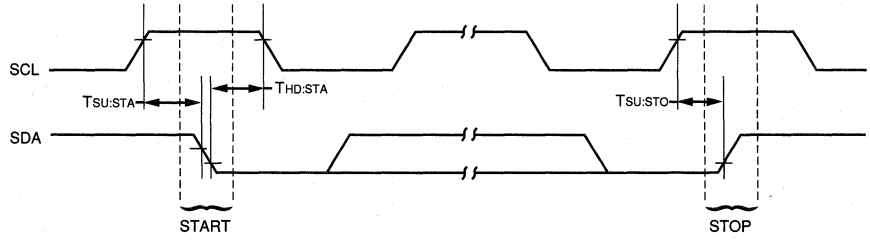
DC CHARACTERISTICS

V_{CC} = +2.5 V to +5.5 V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
A0/WP, SCL and SDA pins: High level input voltage	V_{IH}	.7 V_{CC}		V	
Low level input voltage	V_{IL}		.3 V_{CC}	V	
Low level output voltage	V_{OL}		.40	V	I_{OL} = 3.2 mA V_{CC} = 2.5 V
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = .1 V to 5.5 V
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = .1 V to 5.5 V
Internal capacitance (all inputs/outputs)	C_{INT}		10	pF	V_{CC} = 5.0 V (Note 1) Tamb = 25°C, F_{CLK} = 1 MHz
Operating current	I_{CCO}		3	mA	V_{CC} = 5.5 V SCL = 100 KHz
Standby current	I_{CCS}		30	µA	V_{CC} = 2.5 V SDA = SCL = V_{CC}
			100	µA	V_{CC} = 5.5 V SDA = SCL = V_{CC}

Note 1: This parameter is periodically sampled and not 100% tested.

BUS TIMING START/STOP



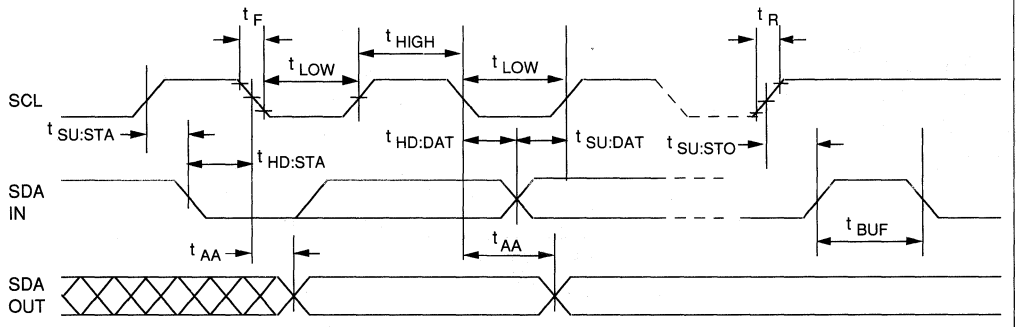
AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
STOP condition hold time	THD:STO	4000			ns	
STOP condition setup time	TSU:STO	4700			ns	
Output valid from clock	TAA	300		3500	ns	See Note 1
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Write cycle time	TWR		2	10	ms	Byte or Page mode
Endurance	---	100,000			E/W Cycles	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: When writing data to the 24LC16, an automatic internal erase then write cycle is executed.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 24LC16 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC16 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a STARTcondition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

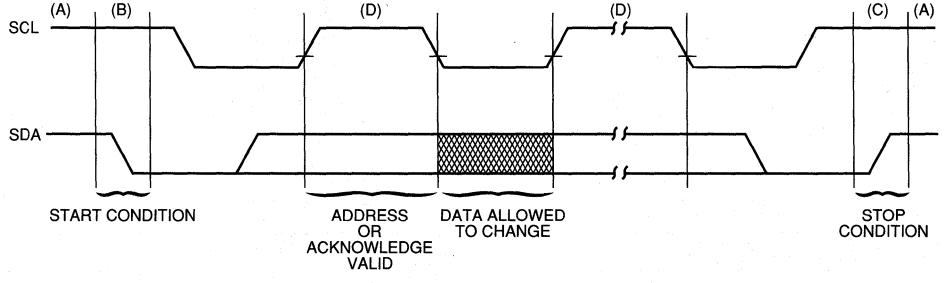
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC16 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



BUS CHARACTERISTICS

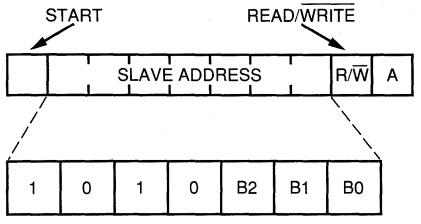
Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC16 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24LC16 per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC16 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24LC16 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 2 - CONTROL BYTE ALLOCATION



WRITE OPERATION

Byte Write

Following the start conditionl from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC16. After receiving another acknowledge signal from the 24LC16 the master device will transmit the data word to be written into the addressed memory location. The 24LC16 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC16 will not generate acknowledge signals. (See Figure 3).

Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC16 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24LC16 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (See Figure 4).

FIGURE 3 - BYTE WRITE

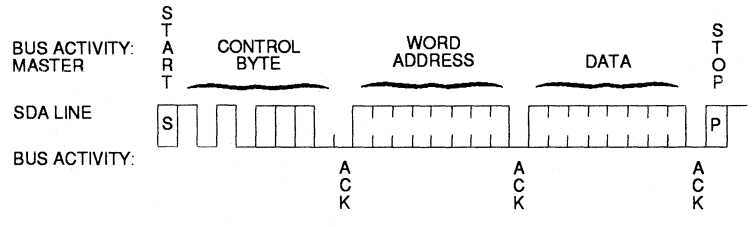


FIGURE 4 - PAGE WRITE

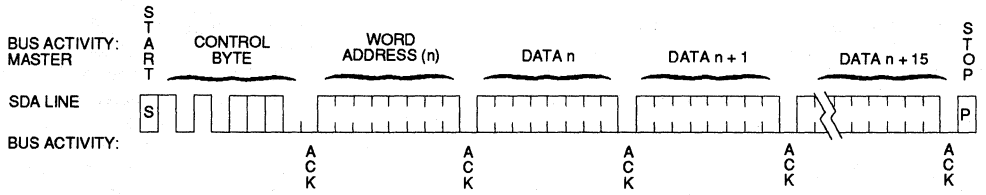


FIGURE 5 - CURRENT ADDRESS READ

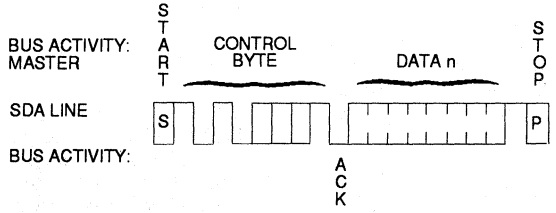


FIGURE 6 - RANDOM READ

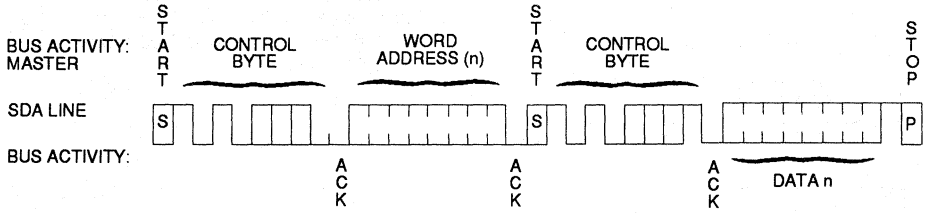
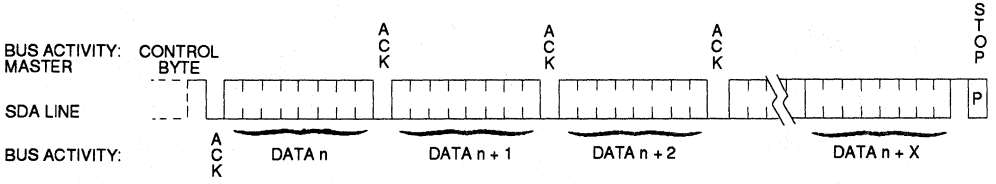


FIGURE 7 - SEQUENTIAL READ



WRITE PROTECTION

The 24LC16 can be used as a serial ROM when WP pin is connected to Vcc (+5V). Programming will be inhibited and the entire memory (2K bytes) will be write-protected.

READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The 24LC16 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC16 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16 discontinues transmission. (See Figure 5).

Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC16 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC16 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16 discontinues transmission. (See Figure 6).

Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC16 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC16 to transmit the next sequentially addressed 8 bit word. (See Figure 7).

To provide sequential reads the 24LC16 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

Noise Protection

The 24LC16 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

PIN DESCRIPTIONS

A0/WP Write Protect Input

This pin must be connected to either Vss or Vcc.

If tied to Vcc, WRITE operations are inhibited. The entire 2K bytes memory will be write-protected. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

This feature allows the user to use the 24LC16 as a serial ROM when WP is enabled (tied to Vcc).

A1, A2 Chip Address Inputs

The A1 and A2 inputs are unused by the 24LC16. They must be connected to Vss to insure proper device operation.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

TEST

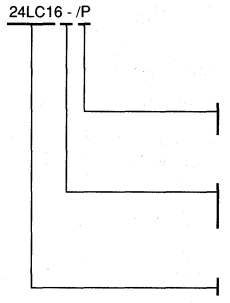
This pin must be connected to Vss.

3

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



PACKAGE:	P	PLASTIC DIP
	SL	PLASTIC SOIC (150 mil Body)
TEMPERATURE RANGE:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
DEVICE:	24LC16	16K CMOS Serial EEPROM
	24LC16T	16K CMOS Serial EEPROM (in Tape and Reel Form)

Microchip

59C11

1K (128 x 8 or 64 x 16) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Pin selectable memory organization
  — 128 x 8 or 64 x 16 bit organization
- Single 5 volt only operation
- Self timed WRITE, ERAL and WRAL cycles
- Automatic erase before WRITE
- RDY/$\overline{BSY}$ status information during WRITE
- Power on/off data protection circuitry
- 100,000 ERASE/WRITE cycles
- Data Retention > 40 Years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  — Commercial: 0°C to +70°C
  — Industrial: -40°C to +85°C
  — Automotive: -40°C to +125°C

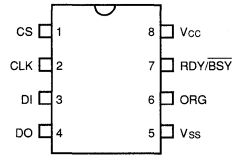
DESCRIPTION

The Microchip Technology Inc. 59C11 is a 1K bit Electrically Erasable PROM. The device is configured as 128 x 8 or 64 x 16, selectable externally by means of the control pin ORG. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 59C11 is available in the standard 8-pin DIP and a surface mount SOIC package.

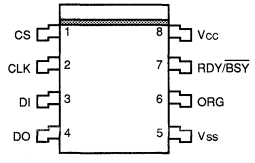
3

PIN CONFIGURATION

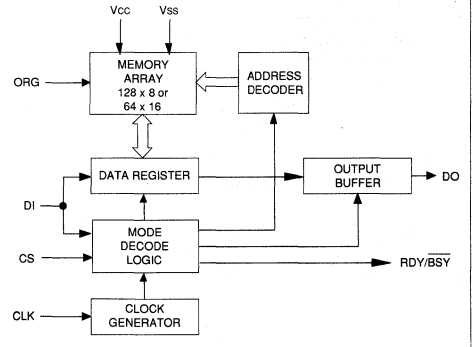
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS ..... -0.3 V to +7.0 V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
VSS	Ground
ORG	Memory Array Organization
RDY/BSY	Ready/Busy Status
VCC	+5 V Power Supply

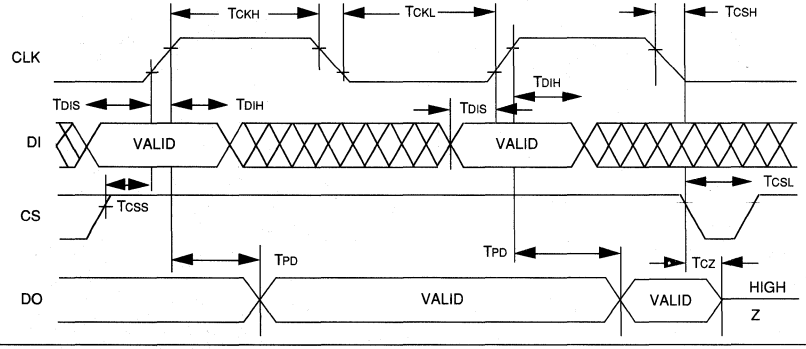
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = –40°C to +85°C
Automotive: Tamb = –40°C to +125°C (Note 3)

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	VCC + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to VCC (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0V (Note 2) Tamb = 25°C, f = 1 MHz
Operating current (all modes)	ICC0		4	mA	FCLK = 1 MHz, VCC =5.5 V
Standby current	ICCS		100	µA	CS = 0 V, VCC = 5.5 V

Note 1: Internal resister pull-up at Pin 6. Active output at Pin 7.
Note 2: This parameter is periodically sampled and not 100% tested.
Note 3: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCS	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
RDY/$\overline{\text{BSY}}$ delay time	TRBD		400	ns	
Program cycle time (Auto Erase & Write)	TWC		1 15	ms ms	for 8-bit mode for ERAL and WRAL in 8/16-bit modes

3

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a WRITE cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a WRITE cycle, the device will go into standby mode as soon as the WRITE cycle is completed.

CS must be LOW for 100 ns (TCSL) minimum between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 59C11. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock high time (TCKH) and clock low time (TCKL)). This gives freedom in preparing opcode, address and data for the controlling master.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto erase/write) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). When that limit has been reached, CLK and DI become "Don't Care" inputs until CS is brought LOW for at least chip select low time (TCSL) and brought HIGH again and a WRITE cycle (if any) is completed.

Data In (DI)

Data In is used to clock in START bit, opcode, address and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK). This output is in HIGH–Z mode except if data is clocked out as a result of a READ instruction.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is output after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during WRITE cycles.

Organization (ORG)

This input selects the memory array organization. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64 x 16 organization. In applications subject to electrical noise, it is recommended that this pin not be left floating, but tied either high or low.

Ready/Busy (RDY/$\overline{BSY}$)

Pin 7 provides RDY/$\overline{BSY}$ status information. RDY/BSY is low if the device is performing a WRITE, ERAL, or WRAL operation. When it is HIGH the internal, self-timed WRITE, ERAL or WRAL operation has been completed and the device is ready to receive a new instruction.

DATA PROTECTION

During power-up, all modes of operation are inhibited until Vcc has reached a level of between 2.8 V and 4.5 V. During power-down, the source data protection circuitry acts to inhibit all modes when VCC has fallen below the voltage range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, EWEN instruction must be performed before any WRITE, ERAL or WRAL instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

INSTRUCTION SET — **64 X 16 MODE, ORG=1**

Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A5 A4 A3 A2 A1 A0	—	D15 – D0	27
WRITE	1	X 1 X X	A5 A4 A3 A2 A1 A0	D15 – D0	High-Z	27
EWEN	1	0 0 1 1	X X X X X X	—	High-Z	11
EWDS	1	0 0 0 0	X X X X X X	—	High-Z	11
ERAL	1	0 0 1 0	X X X X X X	—	High-Z	11
WRAL	1	0 0 0 1	X X X X X X	D15 – D0	High-Z	27

128 X 8 MODE, ORG=0

Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A6 A5 A4 A3 A2 A1 A0	—	D7 – D0	20
WRITE	1	X 1 X X	A6 A5 A4 A3 A2 A1 A0	D7 – D0	High-Z	20
EWEN	1	0 0 1 1	X X X X X X X	—	High-Z	12
EWDS	1	0 0 0 0	X X X X X X X	—	High-Z	12
ERAL	1	0 0 1 0	X X X X X X X	—	High-Z	12
WRAL	1	0 0 0 1	X X X X X X X	D7 – D0	High-Z	20

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both High with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition) without resulting in any device operation (READ, WRITE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e. clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

Note: CS must go LOW between consecutive instructions.

DI/DO Pins

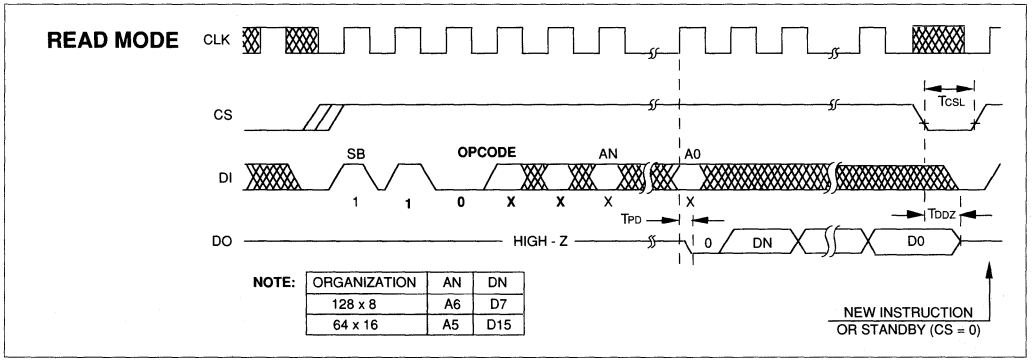
It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 8- or 16-bit output string. The output data changes during the high state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 is a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the negative edge of CS, whichever occurs first. D0 remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15 or D7) is always output first, followed by the lower significant bits (D14 - D0 or D6 - D0).



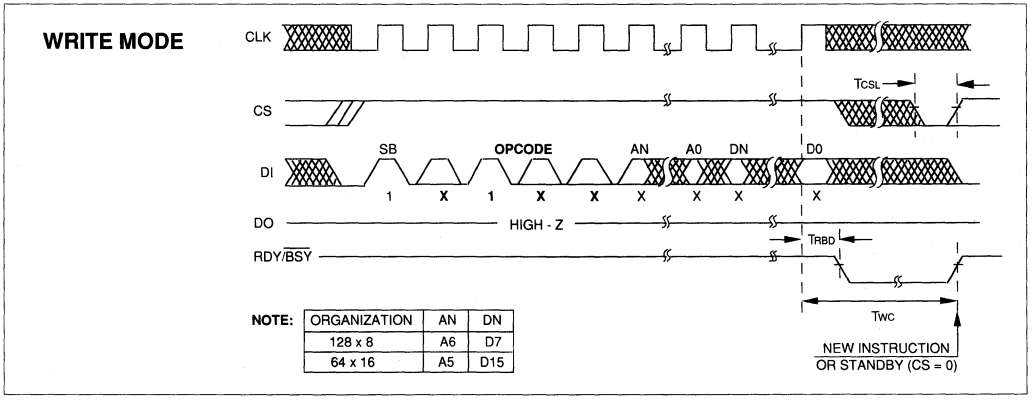
NOTE:

ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

WRITE

The WRITE instruction is followed by 8 or 16 bits of data which are written into the specified address. The most significant data bit (D15 or D7) has to be clocked in first followed by the lower significant data bits (D14 – D0 or D6 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic erase cycle on the specified address before the data are written. The WRITE cycle is completely self timed and commences automatically after the rising edge of the CLK signal for the last data bit (D0).

The WRITE cycle takes 1 ms max for 8-bit mode and 2 ms max for 16-bit mode.



NOTE:

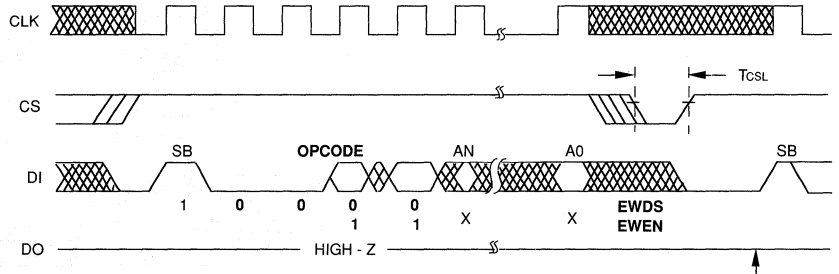
ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

ERASE/WRITE Enable/Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, EWEN instruction has to be performed before any WRITE, ERAL, or WRAL instruction is executed by the device.

For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.

ERASE/WRITE ENABLE AND DISABLE



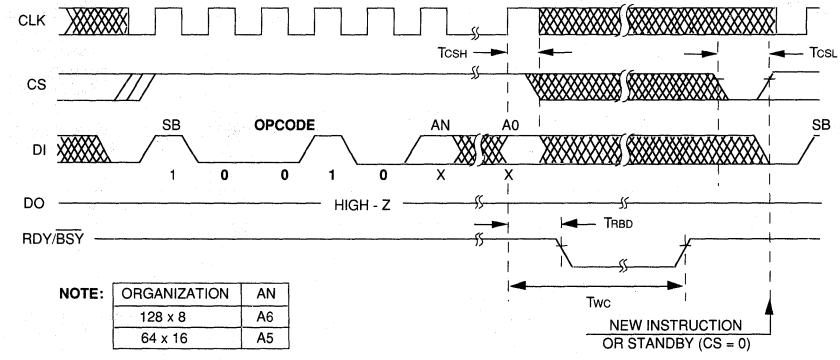
NOTE:

ORGANIZATION	AN
128 x 8	A6
64 x 16	A5

ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the rising edge of the CLK signal for the last dummy address bit. ERAL takes 15 ms max.

ERASE ALL (CHIP ERASE)



NOTE:

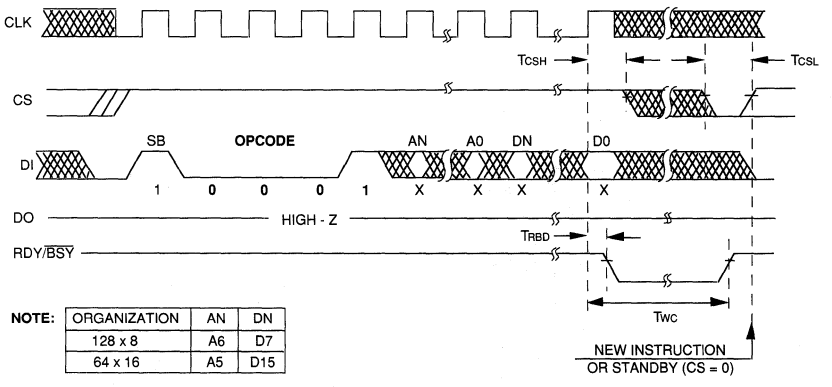
ORGANIZATION	AN
128 x 8	A6
64 x 16	A5

WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms max.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases. The WRAL instruction is used for testing and/or device initialization.

WRITE ALL



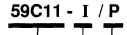
NOTE:

ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Package:	J	CERDIP
	P	Plastic DIP
	SN	Plastic SOIC (0.150 mil Body)
	SM	Plastic SOIC (0.207 mil Body)
Temperature Range:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
Device:	59C11	1K CMOS Serial EEPROM
	59C11T	1K CMOS Serial EEPROM (in Tape & Reel)

Microchip

85C72

1K (128 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Organized as one block of 128 bytes (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

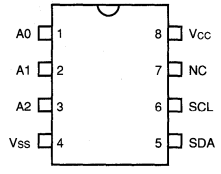
DESCRIPTION

The Microchip Technology Inc. 85C72 is a 1K bit Electrically Erasable PROM. The device is organized as 128 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. Up to eight 85C72s may be connected to the two wire bus. The 85C72 is available in the standard 8-pin DIP and a surface mount SOIC package.

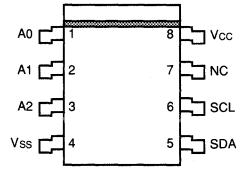
3

PIN CONFIGURATION

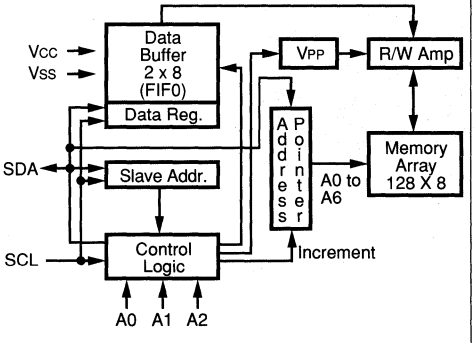
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4.0 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NC	No Connect
VCC	+5 V Power Supply

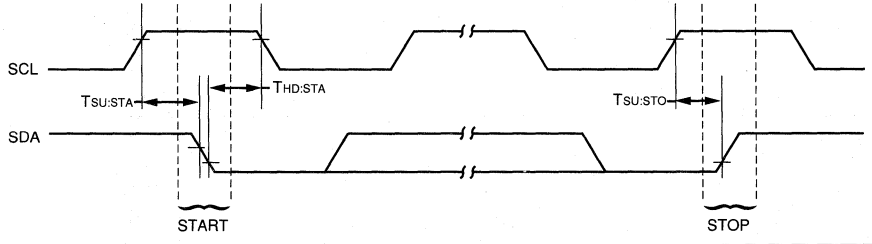
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, VCC = 5 V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, VCC = 5 V, Tamb = (I) and (E)
Read cycle	ICCR		750	µA	VCC = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = VCC = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

BUS TIMING START/STOP

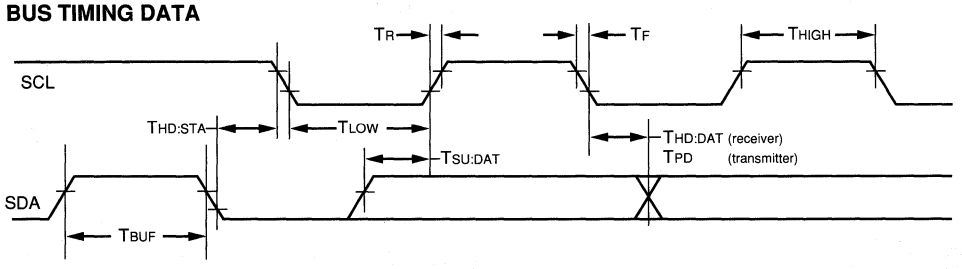


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C72 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the start and STOP conditions, while the 85C72 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 85C72s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 85C72 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

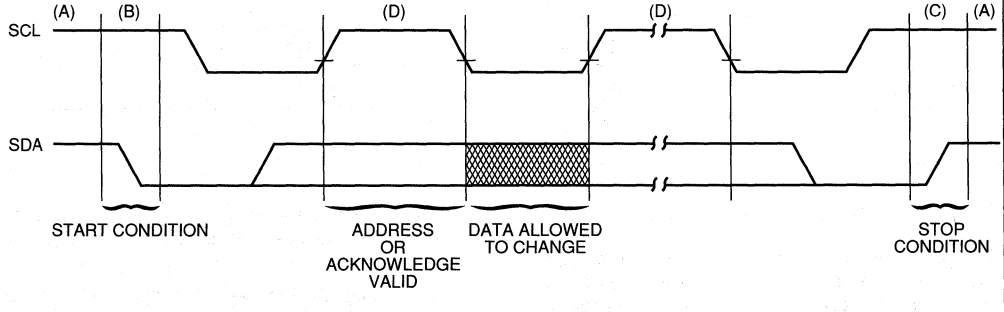
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C72 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

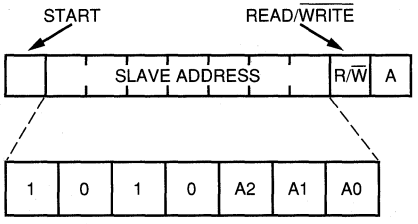
The chip address inputs A0, A1 and A2 of each 85C72 must be externally connected to either Vcc or ground (Vss), assigning to each 85C72 a unique 3-bit address. Up to eight 85C72s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 85C72.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C72, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 85C72. (See Figure 2.)

The 85C72 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 85C72.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C72 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C72. The most significant bit of the word address is a "Do Not Care" value for the 85C72. After receiving the acknowledge of the 85C72, the master device transmits the data word to be written into the addressed memory location. The 85C72 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C72. (See Figure 3.)

PAGE PROGRAM MODE

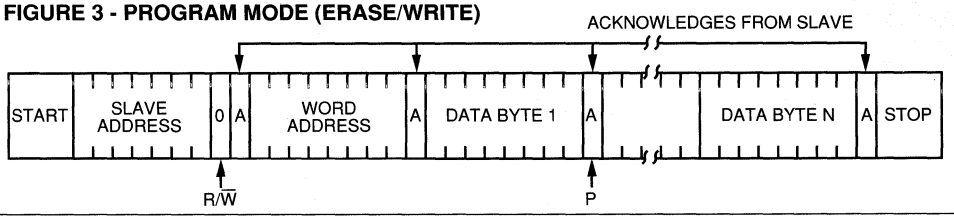
To program the 85C72, the master sends addresses and data to the 85C72 which is the slave. (See Figure 3.) This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C72, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (One " Do Not Care" bit and seven address bits.) The 85C72 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C72 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 85C72.

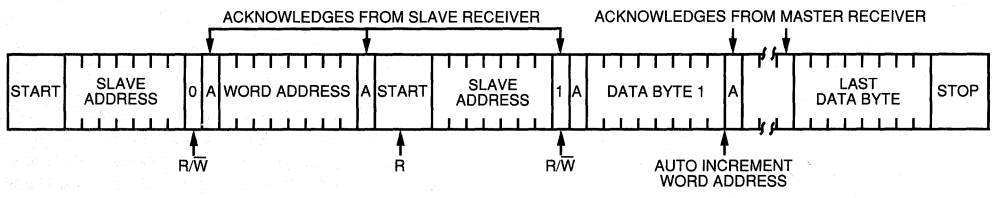
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode the address pointer must be written to.) During this period the 85C72 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

In all modes, the address pointer will automatically increment from the end of the memory block (128 bytes) back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 85C72s can be connected to the bus.

These inputs must be connected to either V_{SS} or V_{CC}.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NC No Connect

This pin can be left open or used as a tie point.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C72 page is 2 bytes long.

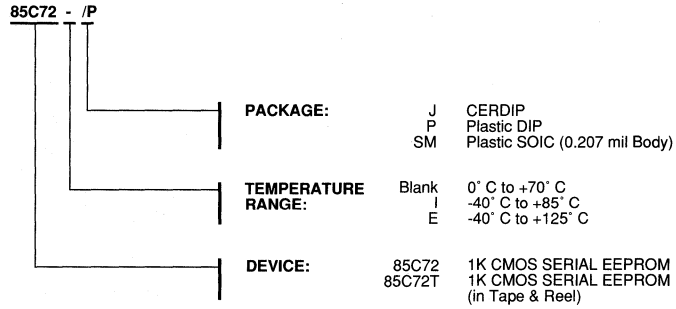
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 85C72 has only one block (128 bytes).

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

85C82

2K (256 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Organized as one block of 256 bytes (256 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 2 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

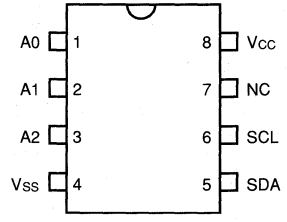
DESCRIPTION

The Microchip Technology Inc. 85C82 is a 2K bit Electrically Erasable PROM. The device is organized as 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C82 also has a page-write capability for up to 2 bytes of data. Up to eight 85C82s may be connected to the two wire bus. The 85C82 is available in standard 8-pin DIP and surface mount SOIC package.

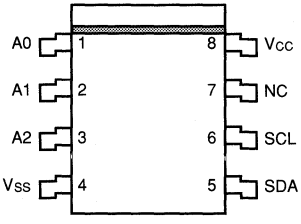
3

PIN CONFIGURATION

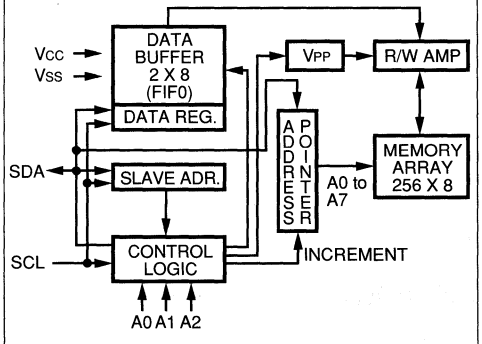
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data Input/Output
SCL	Serial Clock
NC	No Connect
Vcc	+5 V Power Supply

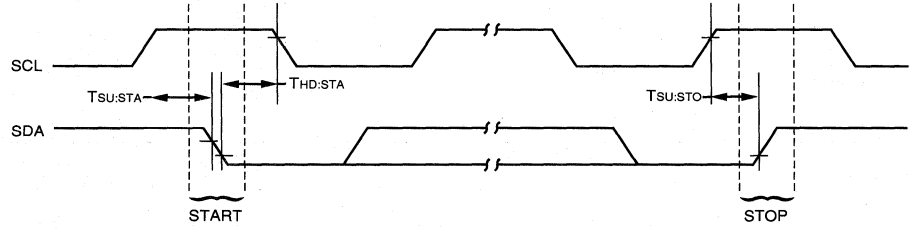
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A0, A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = (I) and (E)
read cycle	ICCR		750	µA	Vcc = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V(no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles

BUS TIMING START/STOP

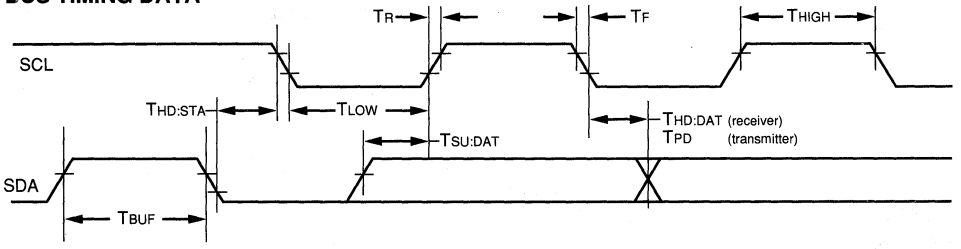


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C82 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C82 works as slave. Both, master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Up to eight 85C82s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 85C82 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

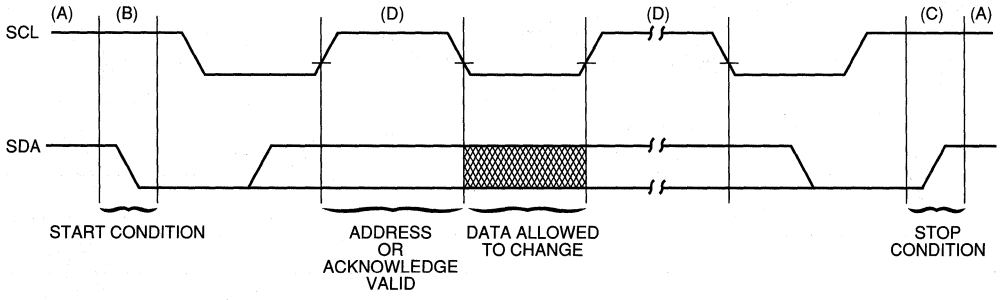
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C82 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

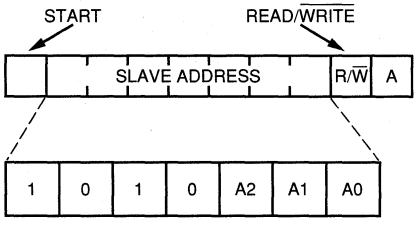
The chip address inputs A0, A1 and A2 of each 85C82 must be externally connected to either Vcc or ground (Vss), assigning to each 85C82 a unique 3-bit address. Up to eight 85C82s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 85C82.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C82, followed by the chip address bits A0, A1 and A2.

The eighth bit of slave address determines if the master device wants to read or write to the 85C82. (See Figure 2.)

The 85C82 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 85C82.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C82 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C82. After receiving the acknowledge of the 85C82, the master device transmits the data word to be written into the addressed memory location. The 85C82 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C82. (See Figure 3.)

PAGE PROGRAM MODE

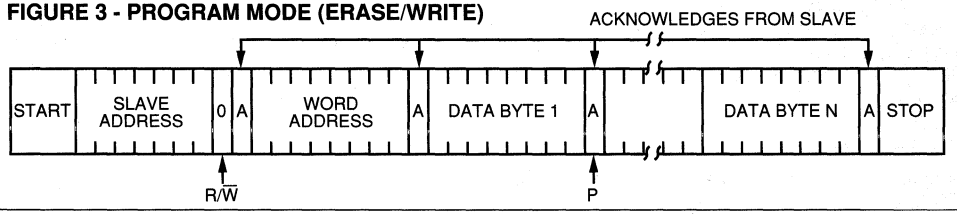
To program the 85C82, the master sends addresses and data to the 85C82 which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C82, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 85C82 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a stop condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C82 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 85C82.

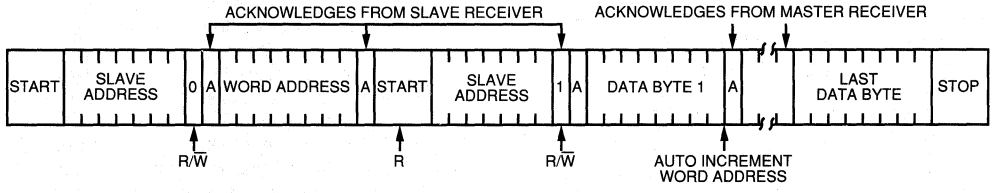
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 85C82 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

Note: In all modes, the address pointer will automatically increment from the end of the memory block (256 byte) back to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 85C82s can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal. For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NC No Connect

This pin can be left open or used as a tie point.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C82 page is 2 bytes long.

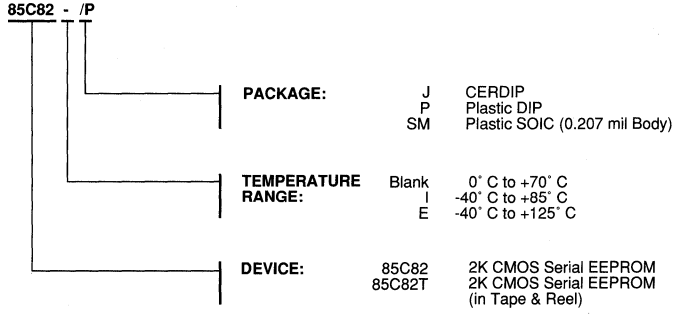
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 85C82 has only one block (256 bytes).

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

85C92

4K (512 x 8) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- Organized as two blocks of 256 bytes (2 x 256 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 1ms write cycle time for single byte
- 100,000 erase/write cycles
- Data retention >40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  —Commercial: 0°C to +70°C
  —Industrial: -40°C to +85°C
  —Automotive: -40°C to +125°C

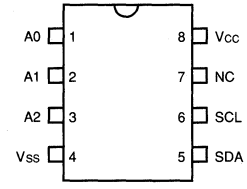
DESCRIPTION

The Microchip Technology Inc. 85C92 is a 4K bit Electrically Erasable PROM. The device is organized as two blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C92 also has a page-write capability for up to 8 bytes of data. Up to four 85C92s may be connected to the two wire bus. The 85C92 is available in the standard 8-pin DIP and a surface mount SOIC package.

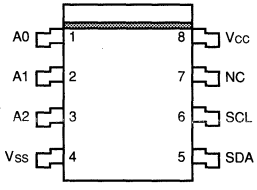
3

PIN CONFIGURATION

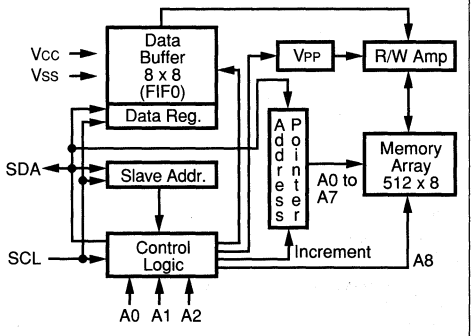
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0	No function. Must be connected to Vcc or Vss
A1, A2	Chip address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
NC	No Connect
Vcc	+5 V Power Supply

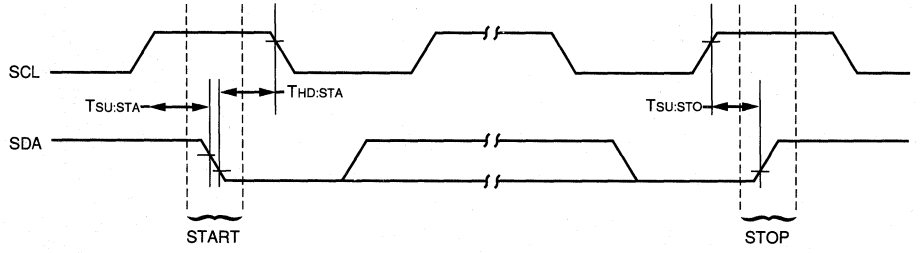
DC CHARACTERISTICS

Vcc = + 5 V (±10%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C (Note 2)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA only)
A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7.0	pF	VIN/VOUT = 0 V (Note 1) TAMB = 25°C, f = 1 MHz
Operating current	ICCO		3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5 V, Tamb = (I) and (E)
read cycle	ICCR		750	µA	Vcc = 5 V, Tamb= (C), (I) and (E)
Standby current	ICCS		100	µA	SDA = SCL = Vcc = 5 V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

BUS TIMING START/STOP

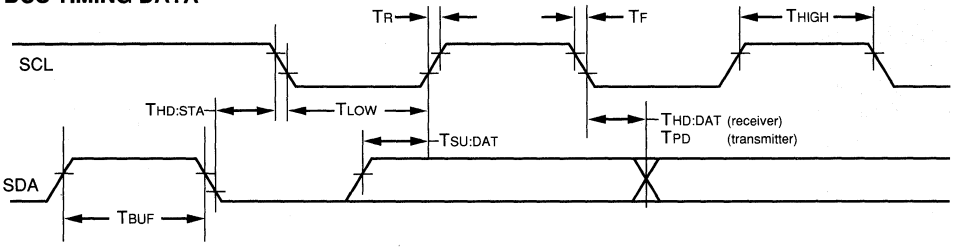


AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK			100	kHz	
Clock high time	THIGH	4000			ns	
Clock low time	TLOW	4700			ns	
SDA and SCL rise time	TR			1000	ns	
SDA and SCL fall time	TF			300	ns	
START condition hold time	THD:STA	4000			ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700			ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0			ns	
Data input setup time	TSU:DAT	250			ns	
Data output delay time	TPD	300		3500	ns	See Note 1
STOP condition setup time	TSU:STO	4700			ns	
Bus free time	TBUF	4700			ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI			100	ns	
Program cycle time	TWC		.7N	N	ms	Byte or Page mode N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (min 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

BUS TIMING DATA



FUNCTIONAL DESCRIPTION

The 85C92 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C92 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to four 85C92s can be connected to the bus, selected by the A1 and A2 chip address inputs. A0 must be tied to VCC or VSS. Other devices can be connected to the bus but require different device codes than the 85C92 (refer to section Slave Address).

BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

Bus not Busy (A)

Both data and clock lines remain HIGH.

Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.
The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

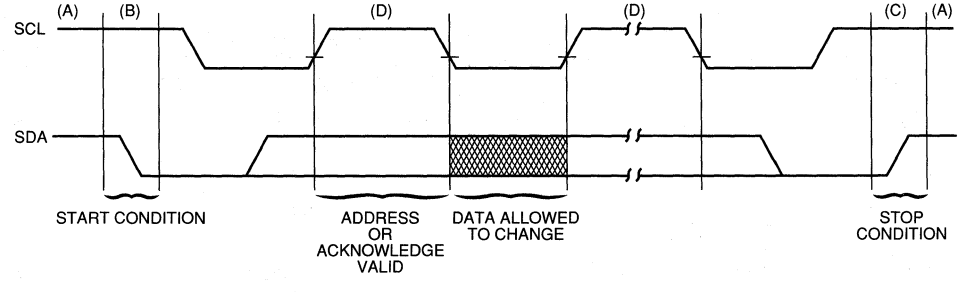
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C92 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS



SLAVE ADDRESS

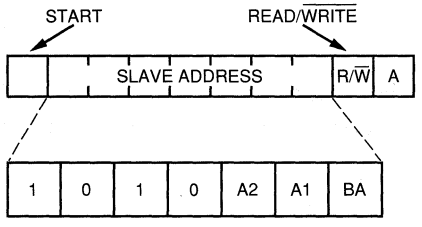
The chip address inputs A1 and A2 of each 85C92 must be externally connected to either Vcc or ground (Vss), assigning to each 85C92 a unique 2-bit address. Up to four 85C92s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A1 and A2 of the slave address to the corresponding hardwired logic levels of the selected 85C92. A0 is not used and must be connected to either Vcc or Vss.

After generating a start condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C92, followed by the chip address bits A1 and A2. The seventh bit of that byte (BA) is used to select the upper block (addresses 100—1FF) or the lower block (addresses 000—0FF) of the 85C92.

The eighth bit of slave address determines if the master device wants to read or write to the 85C92. (See Figure 2.)

The 85C92 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 2 - SLAVE ADDRESS ALLOCATION



BYTE PROGRAM MODE

In this mode the master sends addresses and one data byte to the 85C92.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/W bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C92 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C92. After receiving the acknowledge of the 85C92, the master device transmits the data word to be written into the addressed memory location. The 85C92 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C92. (See Figure 3.)

PAGE PROGRAM MODE

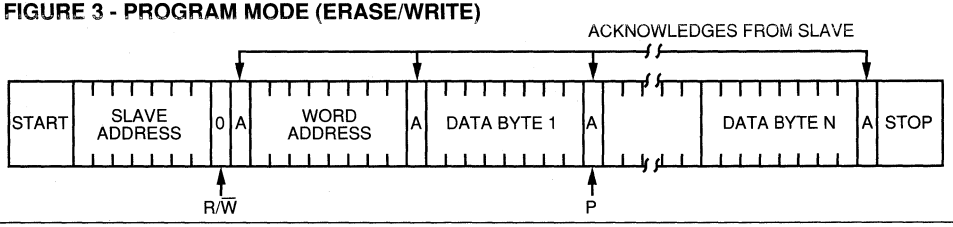
To program the 85C92, the master sends addresses and data to the 85C92 which is the slave (see Figure 3). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/W bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C92, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The BA bit transmitted with the slave address is the ninth bit of the address pointer.) The 85C92 will generate an acknowledge after every 8 bits received and store them consecutively in an 8-byte RAM until a STOP condition is detected which initiates the internal programming cycle. If more than 8 bytes are transmitted by the master, the 85C92 will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 3), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to 8) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8).

FIGURE 3 - PROGRAM MODE (ERASE/WRITE)



READ MODE

This mode illustrates master device reading data from the 85C92.

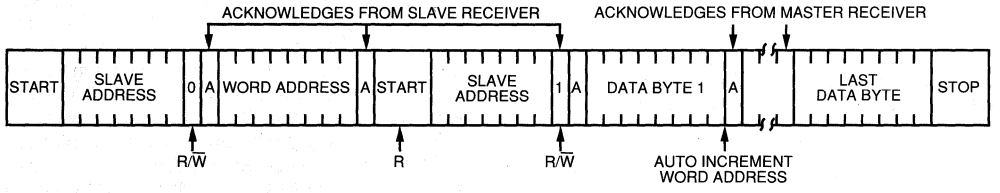
As can be seen from Figure 4, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to.) During this period the 85C92 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 4 and save time transmitting the slave and word addresses.

In all modes, the address pointer will not increment through a block (256 byte) boundary but will wrap around to the first location in that block.

FIGURE 4 - READ MODE



PIN DESCRIPTION

A0

This pin must be connected to either Vcc or Vss.

A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four 85C92s can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

NC No Connect

This pin can be left open or used as a tie point.

Notes:

1) A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C92 page is 8 bytes long.

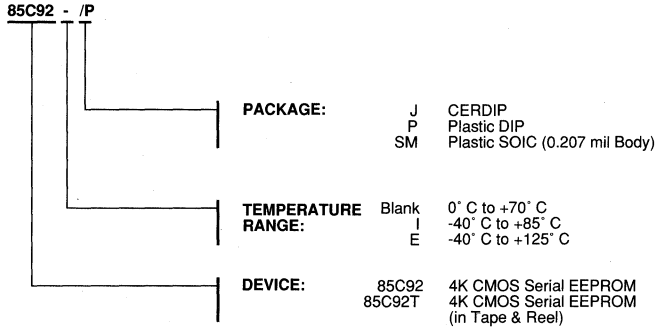
2) A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 85C92 has two blocks, 256 bytes each.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

93C06

256 Bits (16 X 16) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- 16 x 16 bit memory organization
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- 1,000,000 ERASE/WRITE cycles (typical)
- Data Retention > 40 Years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

DESCRIPTION

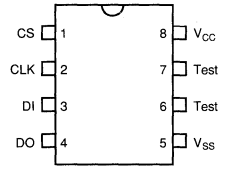
The Microchip Technology Inc. 93C06 is a 256 bit serial Electrically Erasable PROM. The device memory is configured as 16 x 16 bits. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 93C06 is available in the standard 8-pin DIP and a surface mount SOIC package.

3

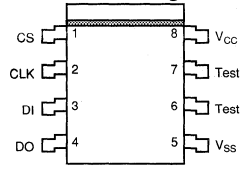
NOT RECOMMENDED FOR NEW DESIGNS

PIN CONFIGURATION

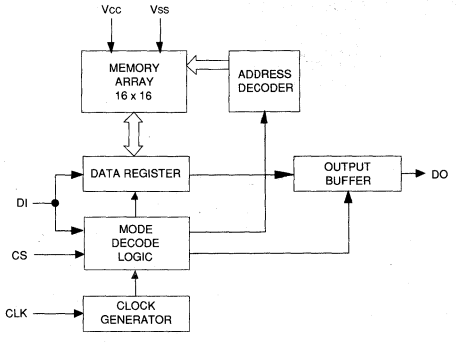
DIP Package



SO Package



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS ..... -0.3 V to +7.0 V
Storage temperature ..... -65°C to +150°C
Ambient temperature with
power applied ..... -65°C to +125°C
Soldering termperature of leads (10 seconds) ... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
VSS	Ground
Test	Recommend tie to VSS or VCC
VCC	+5 V Power Supply

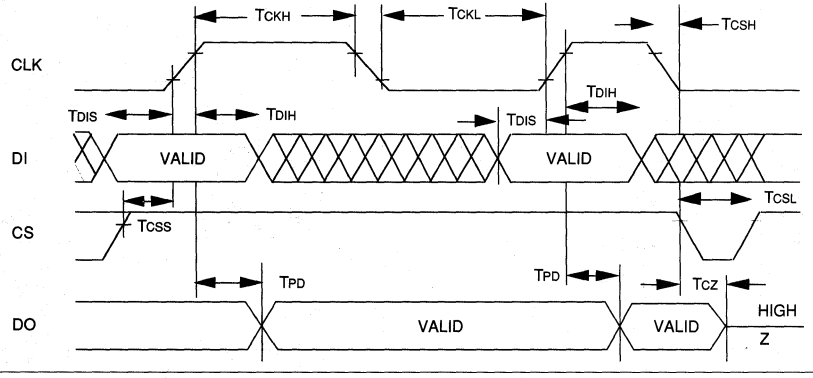
DC CHARACTERISTICS

VCC = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Automotive: Tamb = -40°C to +125°C (Note 3)

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	VCC + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to VCC (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V (Note 2) Tamb = +25°C, F = 1 MHz
Operating current (all modes)	ICC0		4	mA	FCLK = 1 MHz, VCC = 5.5 V
Standby current	ICCS		100	µA	CS = VSS, VCC = 5.5 V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.
Note 3: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = Low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time (Auto Erase & Write)	TWC		2 15	ms ms	for ERAL and WRAL
Erase cycle time	TEC		1	ms	
Endurance	---	100,000		E/W Cycles	

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C06. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e,. auto ERASE/WRITE) cycle.

After detection of a START condition, the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become "Don't Care" inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a Start bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select LOW time (TCSL) from the falling edge of the CLK which clocked in the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during ERASE and WRITE cycles if the READY/BUSY status information is output by the 93C06.

INSTRUCTION SET

Instruction	Start BIT	Opcode OP1	Opcode OP2	Address						Number of Data In	Data Out	Req. CLK Cycles
READ	1	1	0	0	0	A3	A2	A1	A0	—	D15 – D0	25
WRITE	1	0	1	0	0	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{BSY}$)	25
ERASE	1	1	1	0	0	A3	A2	A1	A0	—	(RDY/$\overline{BSY}$)	9
EWEN	1	0	0	1	1	X	X	X	X	—	High-Z	9
EWDS	1	0	0	0	0	X	X	X	X	—	High-Z	9
ERAL	1	0	0	1	0	X	X	X	X	—	(RDY/$\overline{BSY}$)	9
WRAL	1	0	0	0	1	X	X	X	X	D15 – D0	(RDY/$\overline{BSY}$)	25

FUNCTIONAL DESCRIPTION

START Condition

The start bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is High, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new START condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection and Noise Immunity

During power-up, all modes of operation are inhibited until Vcc has reached a level of between 2.8 Vand 4.5 V.

During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below the range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE, or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

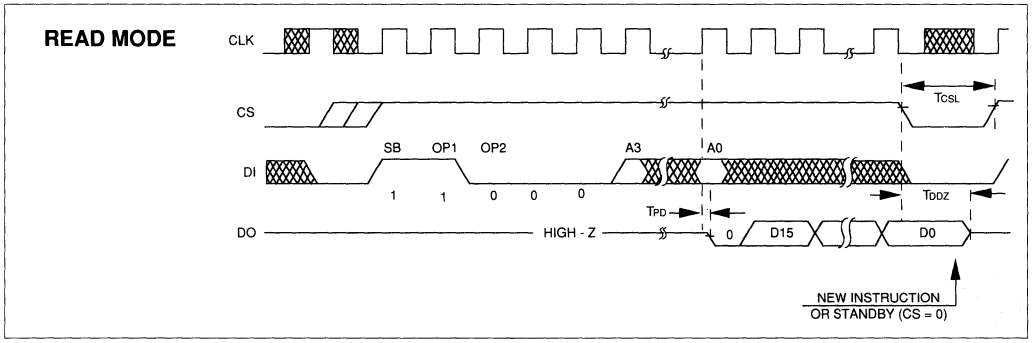
READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the high state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a "1".

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the negative edge of CS, whichever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

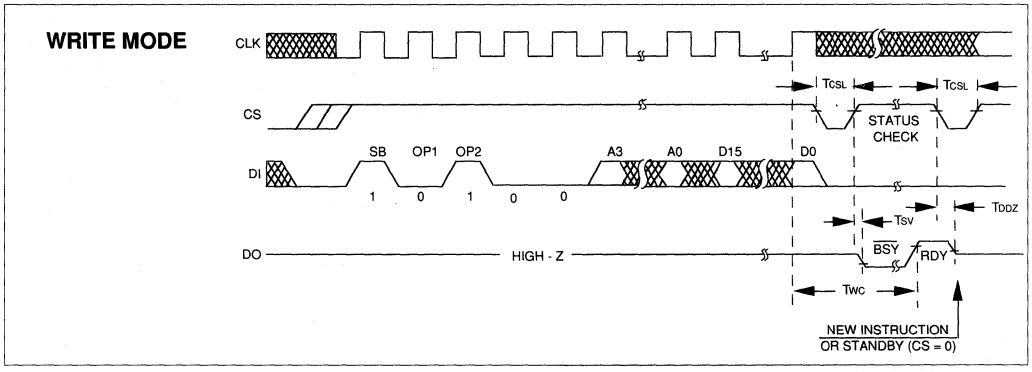
The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).



WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first, followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the rising edge of the CLK signal for the last data bit (D0).

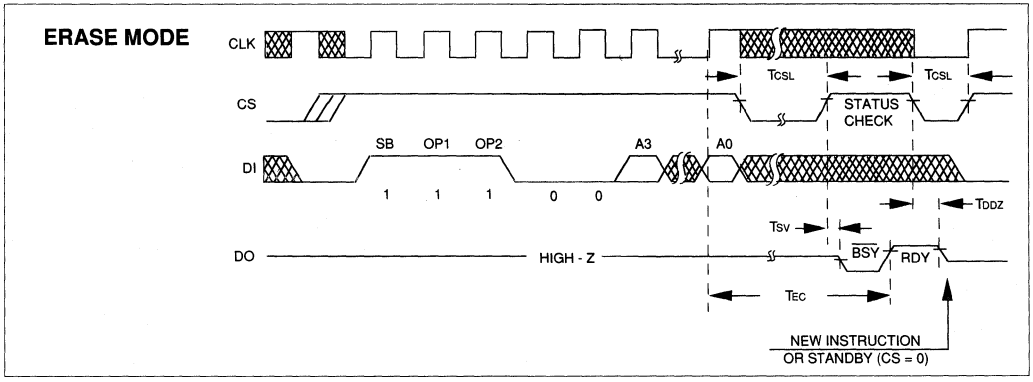
The WRITE cycle takes 2 ms max.



ERASE Mode

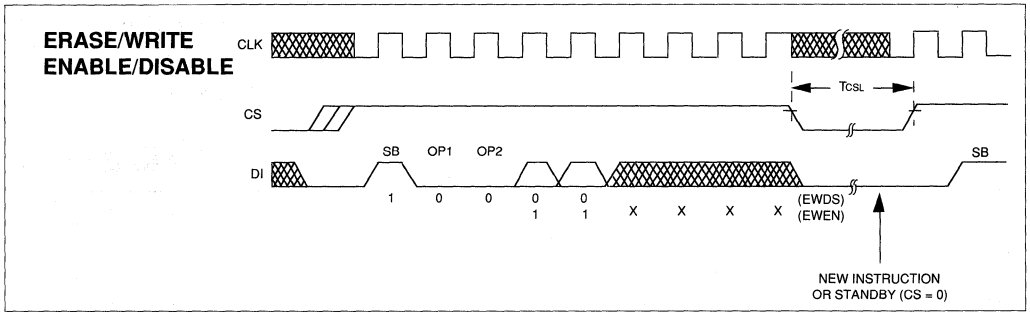
The ERASE instruction forces all the data bits of the specified address to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

The ERASE cycle takes 1 ms max.



ERASE/WRITE Enable/Disable (EWEN, EWDS)

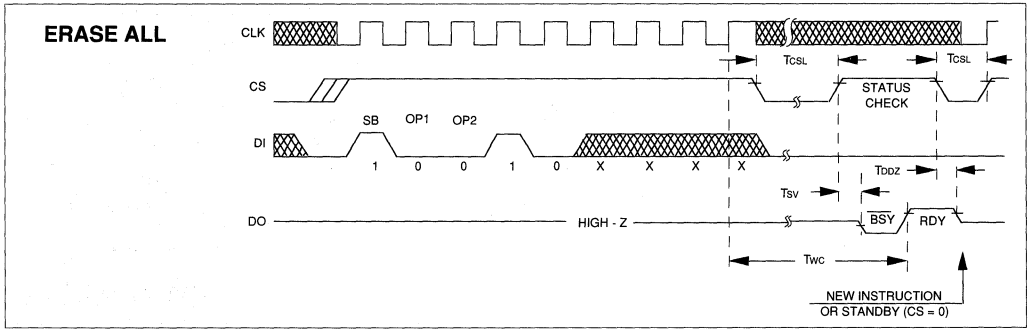
The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.



ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms max.

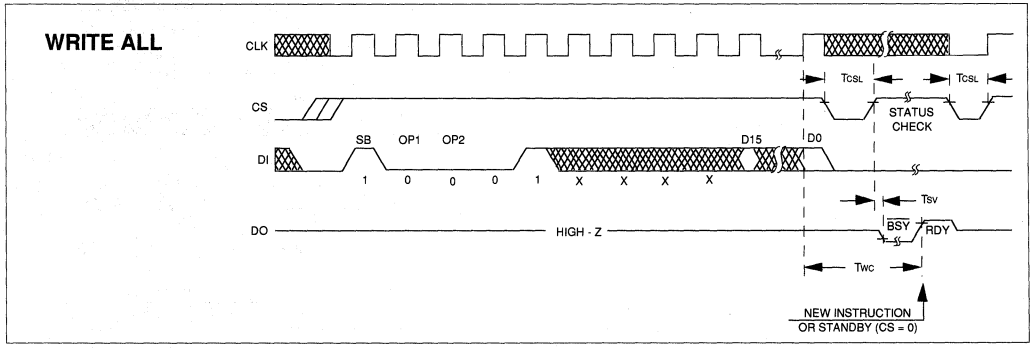


WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms max.

Note: The WRAL does not include an automatic erase cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

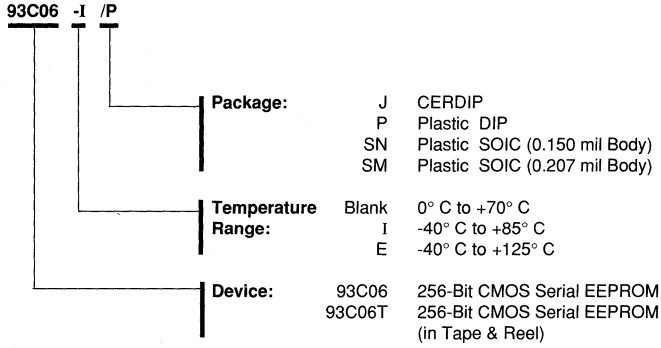


NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

93C46

1K (64 X 16) CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- 64 x 16 bit memory organization
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- 1,000,000 ERASE/WRITE cycles (typical)
- Data Retention > 40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  — Commercial: 0°C to +70°C
  — Industrial: -40°C to +85°C
  — Automotive: -40°C to +125°C

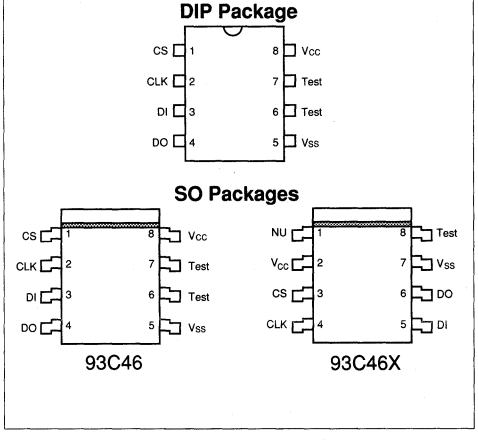
DESCRIPTION

The Microchip Technology Inc. 93C46 is a 1K bit serial Electrically Erasable PROM. The device memory is configured as 64 x 16 bits. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 93C46 is available in the standard 8-pin DIP and a surface mount SOIC package. The 93C46X comes as SOIC only.

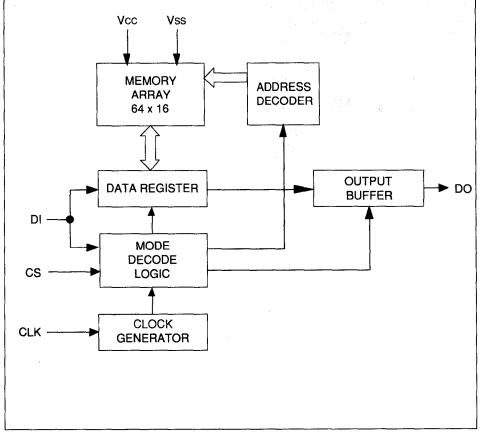
3

NOT RECOMMENDED FOR NEW DESIGNS

PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7.0 V
Storage temperature .....-65°C to +150°C
Ambient temperature with
power applied .....-65°C to +125C
Soldering termperature of leads (10 seconds) ... +300°C
ESD protection on all pins .....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
Vss	Ground
Test	Recommend tie to Vss or Vcc
Vcc	+5 V Power Supply

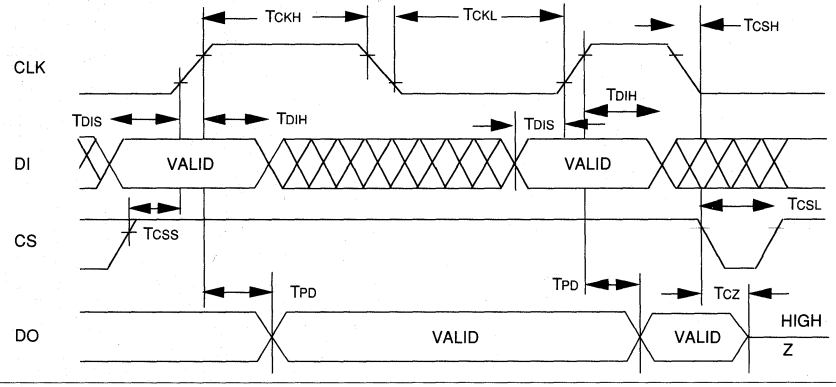
DC CHARACTERISTICS

Vcc = +5 V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = –40°C to +85°C
Automotive: Tamb = –40°C to +125°C (Note 3)

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc (Note 1)
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc (Note 1)
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V (Note 2) Tamb = +25°C, f = 1 MHz
Operating current (all modes)	ICC0		4	mA	FCLK = 1 MHz, Vcc = 5.5 V
Standby current	ICCS		100	µA	CS = 0 V, Vcc = 5.5 V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.
Note 3: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

SYNCHRONOUS DATA TIMING



AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	
Chip select hold time	TCSH	0		ns	
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	
Data input hold time	TDIH	100		ns	
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time (Auto Erase & Write)	TWC		2 15	ms ms	for ERAL and WRAL
Erase cycle time	TEC		1	ms	
Endurance	---	100,000		E/W Cycles	

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C46. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but STARTcondition has not been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., autoERASE/WRITE) cycle.

After detection of a start condition, the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become "Don't Care" inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) from the falling edge of the CLK which clocked in the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during Erase and Write cycles if the READY/$\overline{\text{BUSY}}$ status information is outputted by the 93C46.

INSTRUCTION SET

Instruction	Start BIT	Opcode OP1	Opcode OP2	Address						Number of Data In	Data Out	Req. CLK Cycles
READ	1	1	0	A5	A4	A3	A2	A1	A0	—	D15 – D0	25
WRITE	1	0	1	A5	A4	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{\text{BSY}}$)	25
ERASE	1	1	1	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	9
EWEN	1	0	0	1	1	X	X	X	X	—	High-Z	9
EWDS	1	0	0	0	0	X	X	X	X	—	High-Z	9
ERAL	1	0	0	1	0	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	9
WRAL	1	0	0	0	1	X	X	X	X	D15 – D0	(RDY/$\overline{\text{BSY}}$)	25

FUNCTIONAL DESCRIPTION

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 Vand 4.5 V. During power-down, the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the range of 2.8 V to 4.5 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

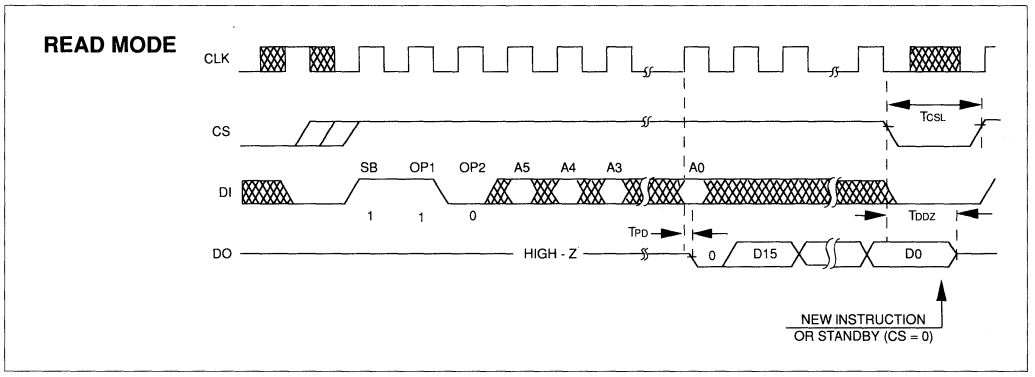
READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output T_{PD} after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, which ever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

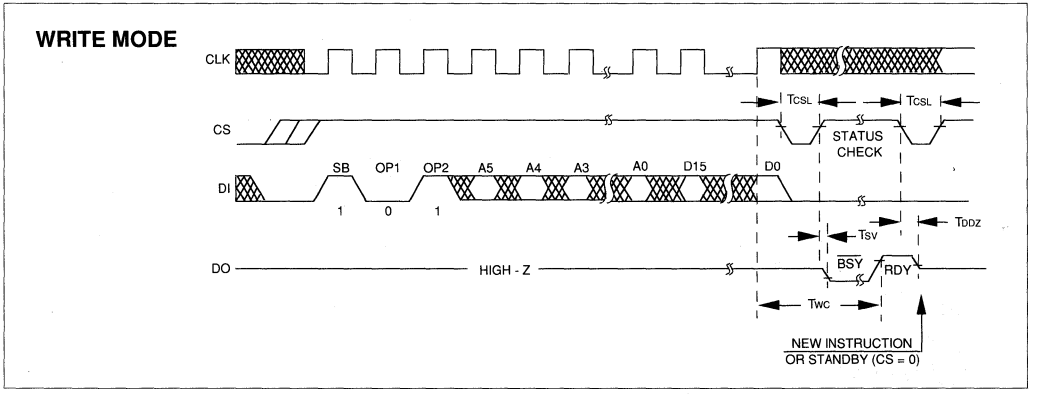
The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).



WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first, followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the rising edge of the CLK for the last data bit (D0).

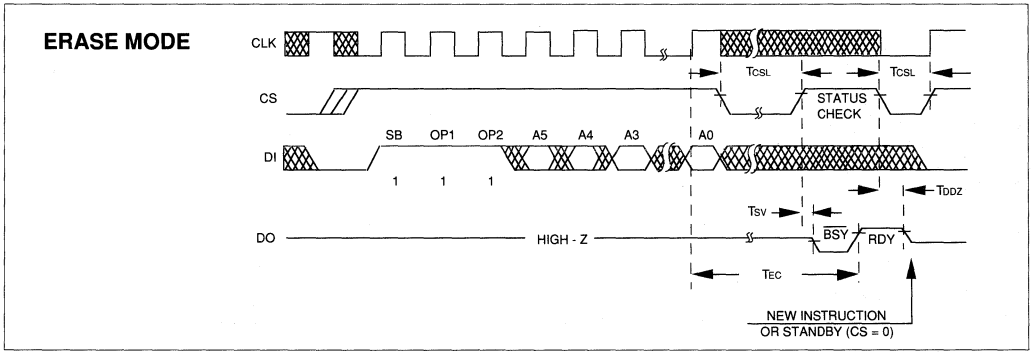
The WRITE cycle takes 2 ms max.



ERASE Mode

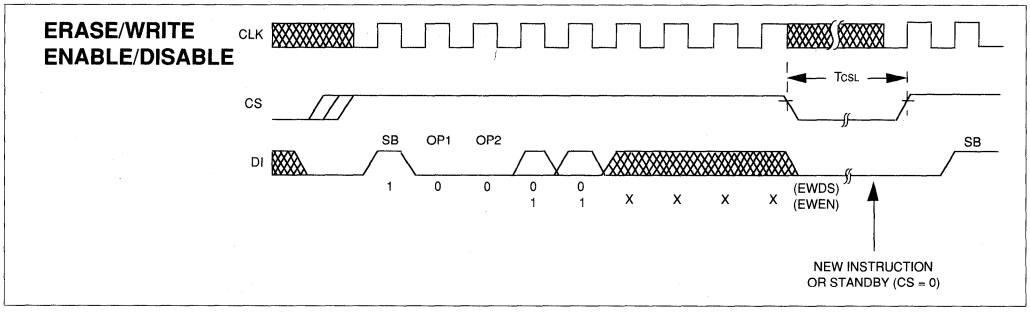
The ERASE instruction forces all the data bits of the specified address to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

The ERASE cycle takes 1 ms max.



ERASE/WRITE Enable/Disable (EWEN, EWDS)

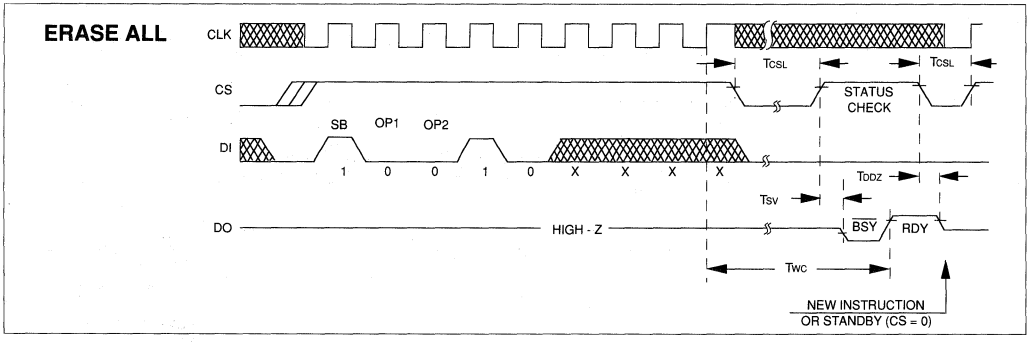
The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.



ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms max.

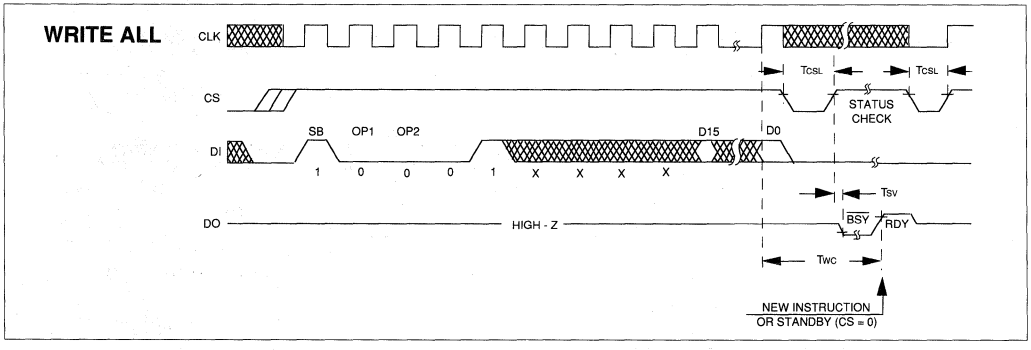


WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the rising edge of the CLK for the last data bit (DO). WRAL takes 15 ms max.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

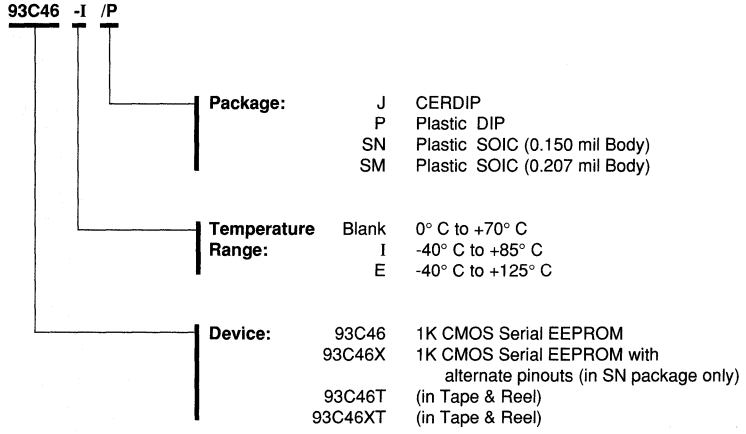


NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

93C56

2K CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- ORG pin selectable memory organization 256 x 8 or 128 x 16 bit organization
- Single 5 volts only operation
- Max clock at 2MHz
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC packages (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - — Commercial: 0°C to +70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

DESCRIPTION

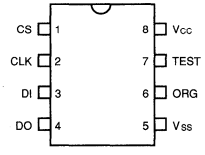
The Microchip Technology Inc. 93C56 is a 2K bit serial Electrically Erasable PROM. The device memory is configured as 256 x 8 or 128 x 16 bits depending on the ORG pin configuration. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 93C56 is available in the standard 8-pin DIP and 8-pin surface mount SOIC package.

3

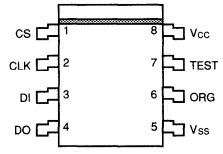
NOT RECOMMENDED FOR NEW DESIGNS

PIN CONFIGURATION

DIP Package

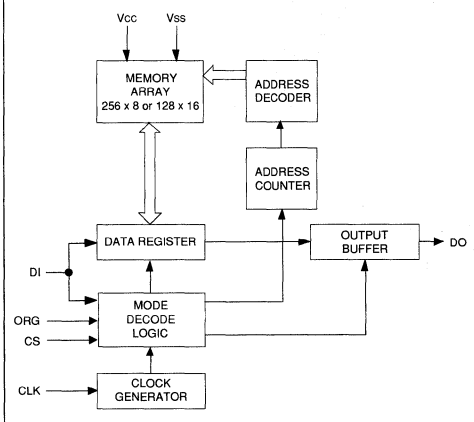


SO Package



93C56

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to +7.0 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....3 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
ORG	Memory Array Organization
Test	Connect to VSS or VCC
VCC	Power Supply +5 V

DC AND AC ELECTRICAL CHARACTERISTICS

VCC = +5 V (+10%/-20%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C
(Note 2) Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
VCC detector threshold	VTH	2.3	4.0	V	
High level input voltage	VIH	2.0	VCC + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 2.1 mA
Input leakage current	ILI		10	µA	VIN = 0 V to VCC
Output leakage current	ILO		10	µA	VOUT = 0 V to VCC
Output capacitance	COUT		7	pF	VIN/VOUT = 0 V; Note 1
Input capacitance	CIN		7	pF	VIN/VOUT = 0 V; Note 1
Operating current (all modes)	ICCO		4	mA	FCLK = 2 MHz; VCC = 5.5 V
Standby current	ICCS		130	µA	CS = 0 V; VCC = 5.5 V; x 8 org
			100	µA	CS = 0 V; VCC = 5.5 V; x 16 org
Endurance	---	100,000		E/W Cycles	
Clock frequency	FCLK		2	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	Relative to CLK
Chip select hold time	TCSH	0		ns	Relative to CLK
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	Relative to CLK
Data input hold time	TDIH	100		ns	Relative to CLK
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time	TCZ		100	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time	TWC		1	ms	(x 8 organization)
(auto ERASE & WRITE)			2	ms	(x 16 organization)
	TEC		15	ms	ERAL & WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz. It is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

INSTRUCTION SET FOR 93C56

ORG = 1 (x 16 organization)						
Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{\text{BSY}}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

ORG = 0 (x 8 organization)						
Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{\text{BSY}}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

FUNCTIONAL DESCRIPTION

The 93C56 can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the (x16) organization. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CLK.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached a level of between 2.3 V and 4.0 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below the range of 2.3 V to 4.0 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93C56 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data changes, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 1 ms per byte max.

WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 1 ms per byte max.

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1". The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL).

The ERAL cycle takes 15 ms max.

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is comnpletely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does not include an automatic ERASE cycle for the device. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL).

The WRAL cycle takes 15 ms max.

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C56. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (T_{CKH}) and clock LOW time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (T_{CSL}) and an ERASE or WRITE operation has been initiated.

Organization (ORG)

When ORG is connected to V_{CC}, the (x16) memory organization is selected. When ORG is tied to V_{SS}, the (x8) memory organization is selected. When ORG is left floating, an internal pullup device will select the device in (x16) organization.

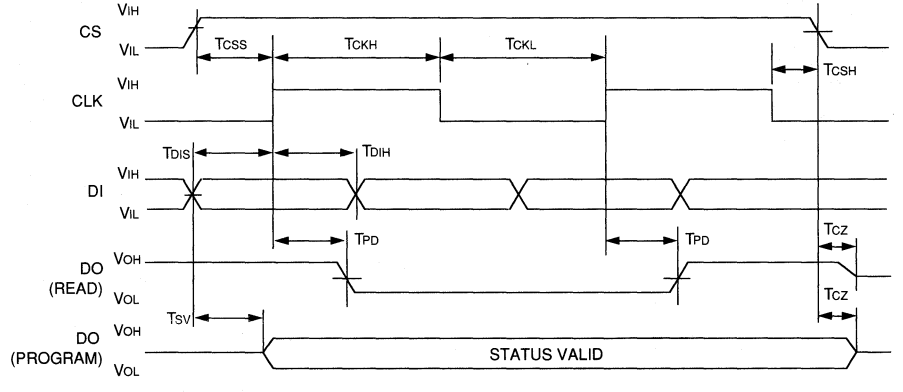
Test

This pin is used for test mode only. It is recommended to connect to V_{CC} or V_{SS} for normal operation.

3

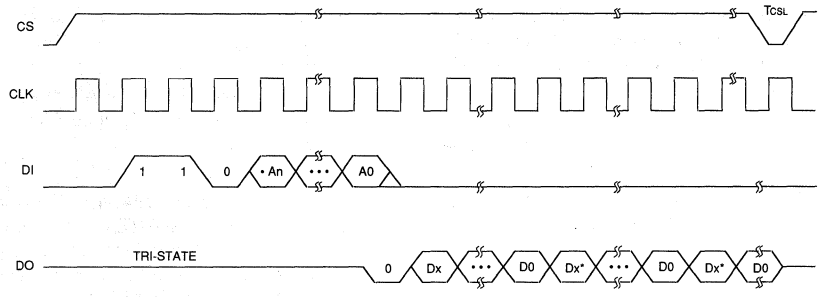
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



TIMING DIAGRAMS (Cont.)

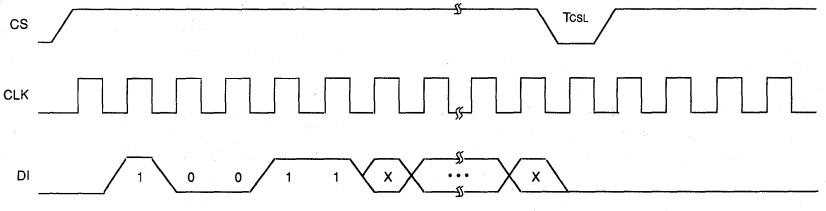
READ



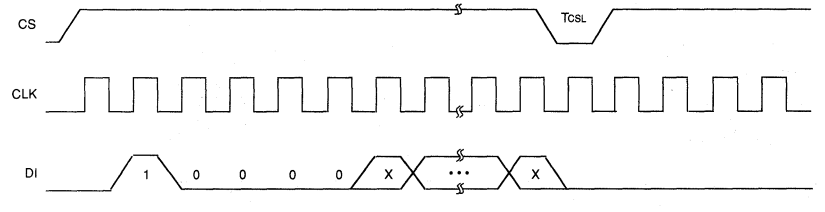
- Address bit A7 becomes a "don't care" (x16 mode).
- Address bit A8 becomes a "don't care" (x8 mode).
- * The memory automatically cycles to the next register.

	(x16)	(x8)
An	A7	A8
Dx	D15	D7

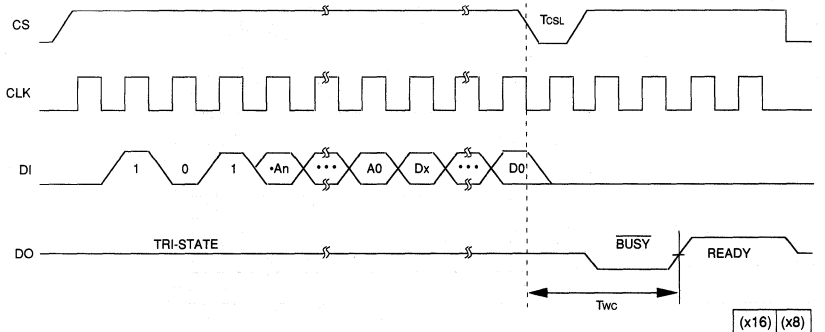
EWEN



EWDS



WRITE

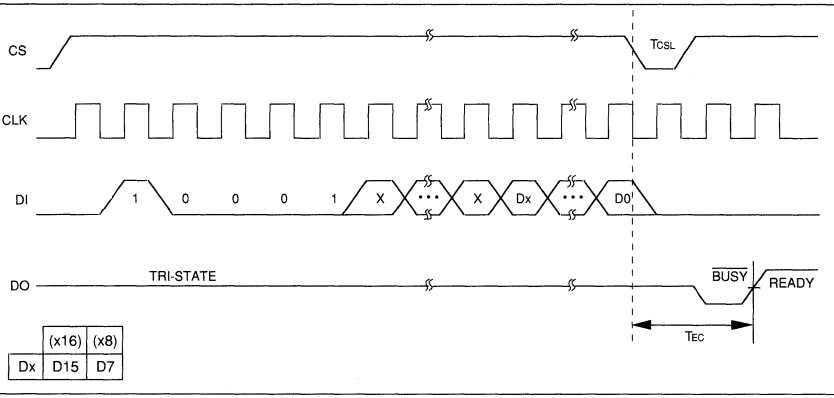


- Address bit A7 becomes a "don't care" (x16 mode).
- Address bit A8 becomes a "don't care" (x8 mode).

	(x16)	(x8)
An	A7	A8
Dx	D15	D7

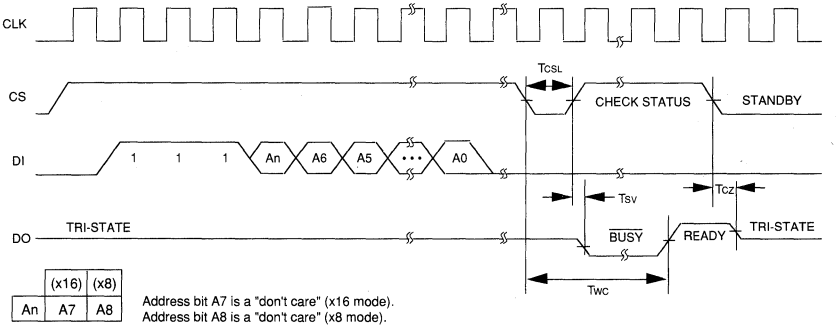
TIMING DIAGRAMS (Cont.)

WRAL



	(x16)	(x8)
Dx	D15	D7

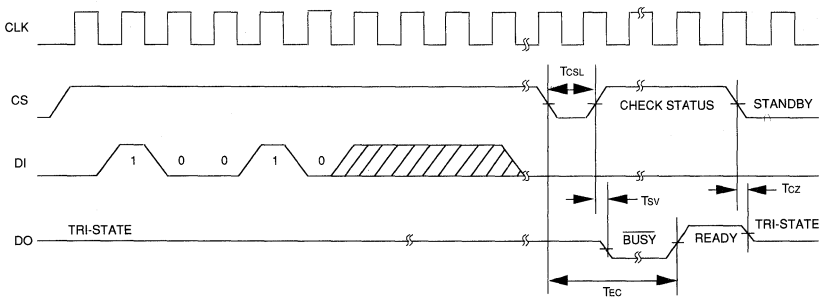
ERASE



	(x16)	(x8)
An	A7	A8

Address bit A7 is a "don't care" (x16 mode).
Address bit A8 is a "don't care" (x8 mode).

ERAL



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93C56 - /P

PACKAGE:		P	PLASTIC DIP
		SN	PLASTIC SOIC (0.150 mil Body)
		SM	PLASTIC SOIC (0.207 mil Body)
TEMPERATURE RANGE:		Blank	0° C to +70° C
		I	-40° C to +85° C
		E	-40° C to +125° C
DEVICE:		93C56	2K CMOS Serial EEPROM
		93C56T	2K CMOS Serial EEPROM (in Tape and Reel Form)

Microchip

93C66

4K CMOS Serial Electrically Erasable PROM

FEATURES

- Low power CMOS technology
- ORG pin selectable memory organization
- Single 5 volts only operation
- Max clock at 2MHz
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC
  (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - — Commercial: 0°C to + 70°C
  - — Industrial: -40°C to +85°C
  - — Automotive: -40°C to +125°C

DESCRIPTION

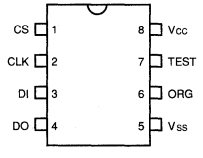
The Microchip Technology Inc. 93C66 is a 4K bit serial Electrically Erasable PROM. The device memory is configured as 512 x 8 or 256 x 16 bits depending on the ORG pin configuration. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications. The 93C66 is available in the standard 8-pin DIP and 8-pin surface mount SOIC package.

3

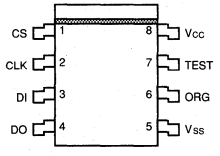
NOT RECOMMENDED FOR NEW DESIGNS

PIN CONFIGURATION

DIP Package

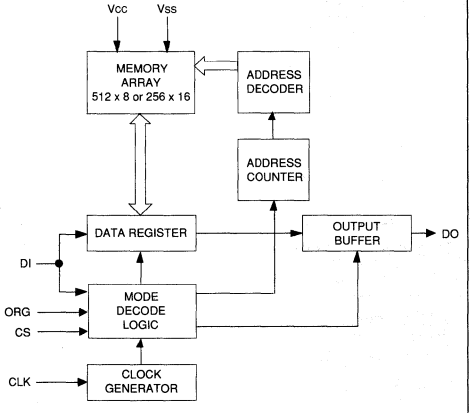


SO Package



93C66

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3 V to +7.0 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....3 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Array Organization
Test	Connect to Vss or Vcc
Vcc	Power Supply +5 V

DC AND AC ELECTRICAL CHARACTERISTICS

Vcc = +5 V (+10%/-20%)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C
(Note 2) Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
Vcc detector threshold	VTH	2.3	4.0	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL		0.4	V	IOL = 2.1 mA
Input leakage current	ILI		10	µA	VIN = 0 V to Vcc
Output leakage current	ILO		10	µA	VOUT = 0 V to Vcc
Output capacitance	COUT		7	pF	VIN/VOUT = 0 V; Note 1
Input capacitance	CIN		7	pF	VIN/VOUT = 0 V; Note 1
Operating current (all modes)	ICCO		4	mA	FCLK = 2 MHz; Vcc = 5.5 V
Standby current	ICCS		130	µA	CS = 0 V; Vcc = 5.5 V; x 8 org
			100	µA	CS = 0 V; Vcc = 5.5 V; x 16 org
Endurance	---	100,000		E/W Cycles	
Clock frequency	FCLK		2	MHz	
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	Relative to CLK
Chip select hold time	TCSH	0		ns	Relative to CLK
Chip select low time	TCSL	100		ns	
Data input setup time	TDIS	100		ns	Relative to CLK
Data input hold time	TDIH	100		ns	Relative to CLK
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time	TCZ		100	ns	CL = 100 pF
Status valid time	TSV		100	ns	CL = 100 pF
Program cycle time	TWC		1	ms	(x 8 organization)
(auto ERASE & WRITE)			2	ms	(x 16 organization)
	TEC		15	ms	ERAL & WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz. It is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

INSTRUCTION SET FOR 93C66

ORG = 1 (x 16 organization)						
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**Req. CLK Cycles**
READ	1	10	A7 - A0	—	D15 - D0	27
EWEN	1	00	11XXXXXX	—	High-Z	11
ERASE	1	11	A7 - A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	10XXXXXX	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 - A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	01XXXXXX	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	00XXXXXX	—	High-Z	11

ORG = 0 (x 8 organization)						
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**Req. CLK Cycles**
READ	1	10	A8 - A0	—	D7 - D0	20
EWEN	1	00	11XXXXXXX	—	High-Z	12
ERASE	1	11	A8 - A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	10XXXXXXX	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	A8 - A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	01XXXXXXX	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	00XXXXXXX	—	High-Z	12

3

FUNCTIONAL DESCRIPTION

The 93C66 can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the (x16) organization. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CLK.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached a level of between 2.3 V and 4.0 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below the range of 2.3 V to 4.0 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93C66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data changes, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 1 ms per byte max.

WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 1 ms per byte max.

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1". The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL).

The ERAL cycle takes 15 ms max.

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is comnpletely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does not include an automatic ERASE cycle for the device. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL).

The WRAL cycle takes 15 ms max.

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C66. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (T_{CKH}) and clock LOW time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (T_{CSL}) and an ERASE or WRITE operation has been initiated.

Organization (ORG)

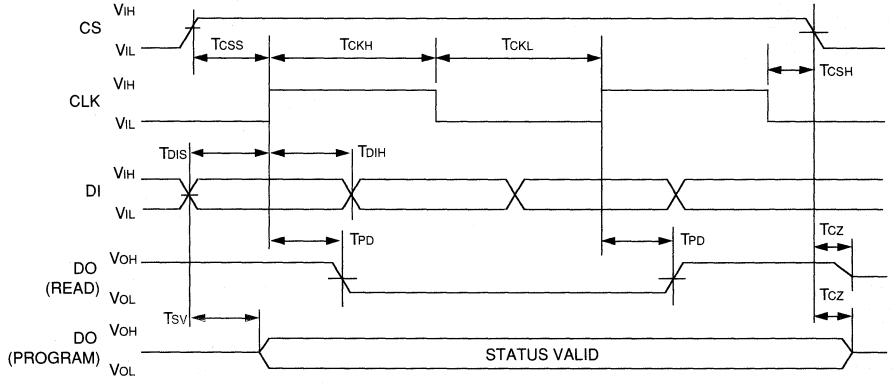
When ORG is connected to V_{CC}, the (x16) memory organization is selected. When ORG is tied to V_{SS}, the (x8) memory organization is selected. When ORG is left floating, an internal pullup device will select the device in (x16) organization.

Test

This pin is used for test mode only. It is recommended to connect to V_{CC} or V_{SS} for normal operation.

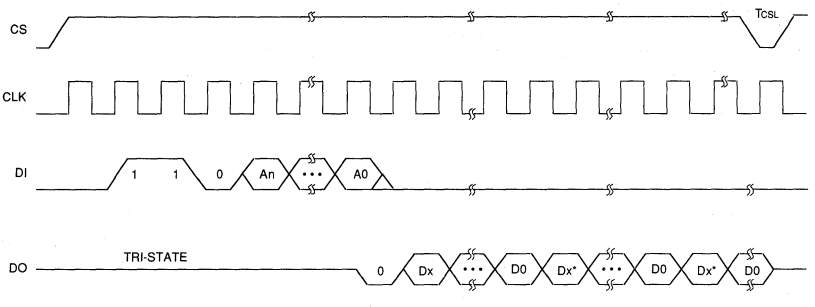
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



TIMING DIAGRAMS (Cont.)

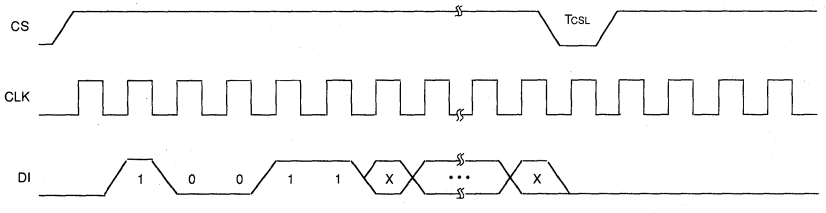
READ



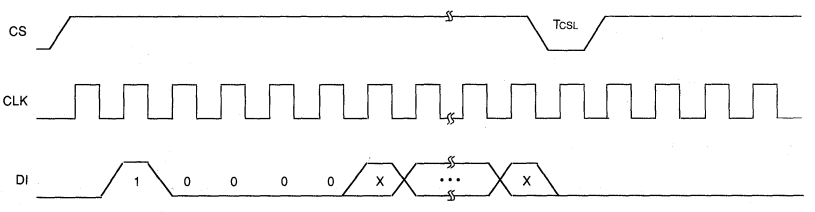
* The memory automatically cycles to the next register.

	(x16)	(x8)
An	A7	A8
Dx	D15	D7

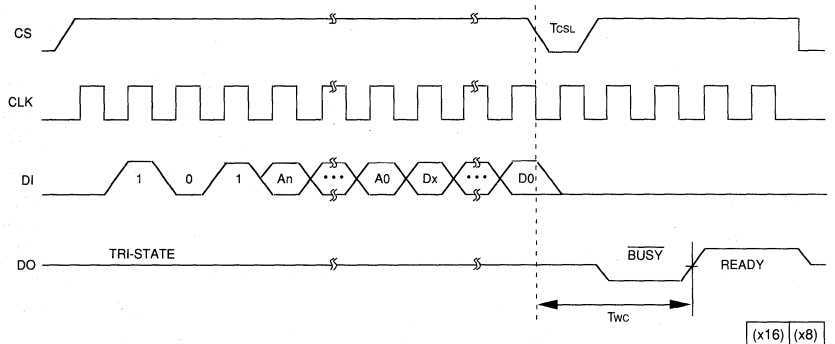
EWEN



EWDS



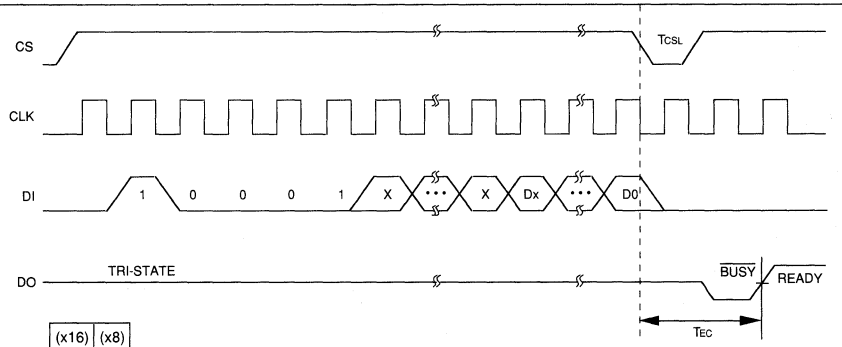
WRITE



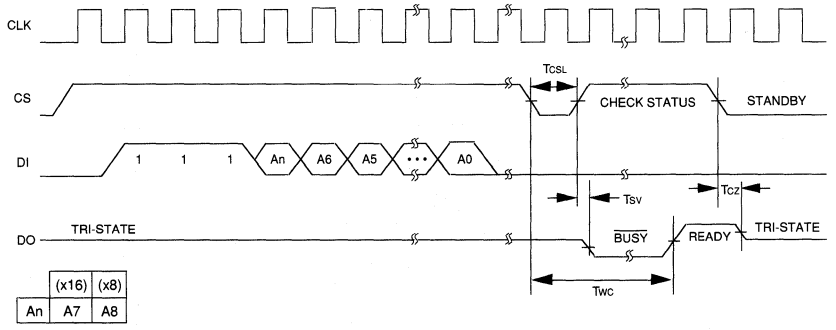
	(x16)	(x8)
An	A7	A8
Dx	D15	D7

TIMING DIAGRAMS (Cont.)

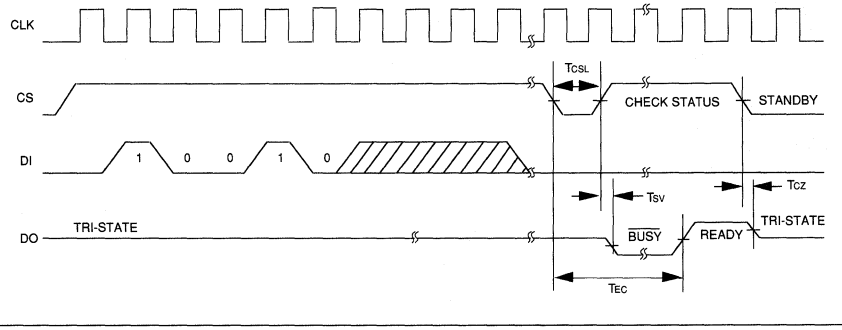
WRAL



ERASE



ERAL



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93C66 - /P

PACKAGE:	P	PLASTIC DIP
	SN	PLASTIC SOIC (0.150 mil Body)
	SM	PLASTIC SOIC (0.207 mil Body)
TEMPERATURE RANGE:	Blank	0° C to +70° C
	I	-40° C to +85° C
	E	-40° C to +125° C
DEVICE:	93C66	4K CMOS Serial EEPROM
	93C66T	4K CMOS Serial EEPROM (in Tape and Reel Form)

93LC46/56/66

CMOS Serial Electrically Erasable PROM

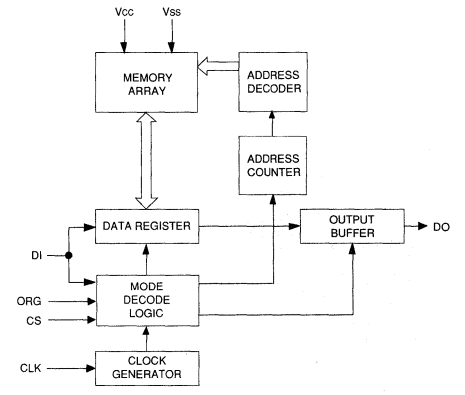
FEATURES

- Single supply with programming operation down to 2.0 volts
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current (typical) at 3.0 V
- ORG pin selectable memory configuration
  128x8 or 64x16 bit organization (93LC46)
  256x8 or 128x16 bit organization (93LC56)
  512 x 8 or 256 x 16 bit organization (93LC66)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- 1,000,000 ERASE/WRITE cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC package (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C (93LC56/66)

DESCRIPTION

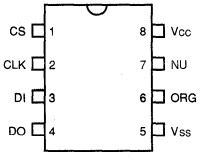
The Microchip Technology Inc. 93LC46/56/66 are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93LC Series is available in standard 8-pin DIP and 8/14-pin surface mount SOIC packages. The 93LC46X/56X/66Xare offered in "SN" package only.

BLOCK DIAGRAM

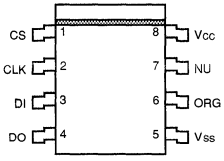


PIN CONFIGURATION

DIP Package

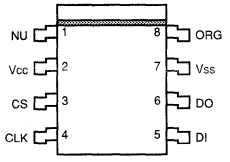


93LC46
93LC56
93LC66

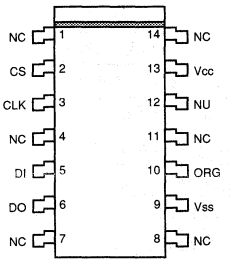


93LC46
93LC56
93LC66

SO Packages



93LC46X
93LC56X
93LC66X



93LC56
93LC66

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss .....-0.3V to +7.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Configuration
NU	Not Utilized
Vcc	Power Supply

DC AND AC ELECTRICAL CHARACTERISTICS

Vcc = +2.0V to +6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
High level input voltage	VIH	0.7 Vcc		V	
Low level input voltage	VIL		0.3 Vcc	V	
Low level output voltage	VOL1		0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2		0.2	V	IOL =10 µA
High level output voltage	VOH1	2.4		V	IOH = -400 µA
	VOH2	Vcc-0.2		V	IOH = -10 µA
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to Vcc
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V (Note 1 & 3) Tamb = +25°C, FCLK = 1 MHz
Operating current (read mode)	ICCO		1	mA	FCLK = 2 MHz; Vcc = 6.0V
			500	µA	FCLK = 1 MHz; Vcc = 3.0V
Standby current	ICCS		100	µA	CLK = CS = 0V; Vcc = 5.5V
			30	µA	CLK = CS = 0V; Vcc = 3.0V
Endurance	—	100,000		E/W Cycles	
Clock frequency	FCLK		2	MHz	Vcc > 4.5V
			1	MHz	Vcc < 4.5V
Clock high time	TCKH	250		ns	
Clock low time	TCKL	250		ns	
Chip select setup time	TCSS	50		ns	Relative to CLK
Chip select hold time	TCSH	0		ns	Relative to CLK
Chip select low time	TCSL	250		ns	
Data input setup time	TDIS	100		ns	Relative to CLK
Data input hold time	TDIH	100		ns	Relative to CLK
Data output delay time	TPD		400	ns	CL = 100 pF
Data output disable time	TCZ		100	ns	CL = 100 pF (Note 3)
Status valid time	TSV		500	ns	CL = 100 pF
Program cycle time	TWC		10	ms	ERASE/WRITE mode (Note 2)
	TEC		20	ms	ERAL mode
	TWL		40	ms	WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
Note 2: Typical program cycle time is 4 ms per word.
Note 3: This parameter is periodically sampled and not 100% tested.

INSTRUCTION SET FOR 93LC46: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	9
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{BSY}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/$\overline{BSY}$)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

INSTRUCTION SET FOR 93LC46: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{BSY}$)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

INSTRUCTION SET FOR 93LC56: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

INSTRUCTION SET FOR 93LC56: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

INSTRUCTION SET FOR 93LC66: ORG = 1 (x 16 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 - A0	—	D15 - D0	27
EWEN	1	00	11XXXXX	—	High-Z	11
ERASE	1	11	A7 - A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	10XXXXX	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 - A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	01XXXXX	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	00XXXXX	—	High-Z	11

INSTRUCTION SET FOR 93LC66: ORG = 0 (x 8 organization)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 - A0	—	D7 - D0	20
EWEN	1	00	11XXXXXXX	—	High-Z	12
ERASE	1	11	A8 - A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	10XXXXXXX	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	A8 - A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	01XXXXXXX	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	00XXXXXXX	—	High-Z	12

3

FUNCTIONAL DESCRIPTION

When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

ERASE/WRITE ENABLE AND DISABLE

The 93LC46/56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word.

WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.
The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word.

ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at VCC = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The ERAL cycle takes 20 ms max (8 ms typical).

WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at VCC = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 40 ms max (16 ms typical).

PIN DESCRIPTION

Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LCX66. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

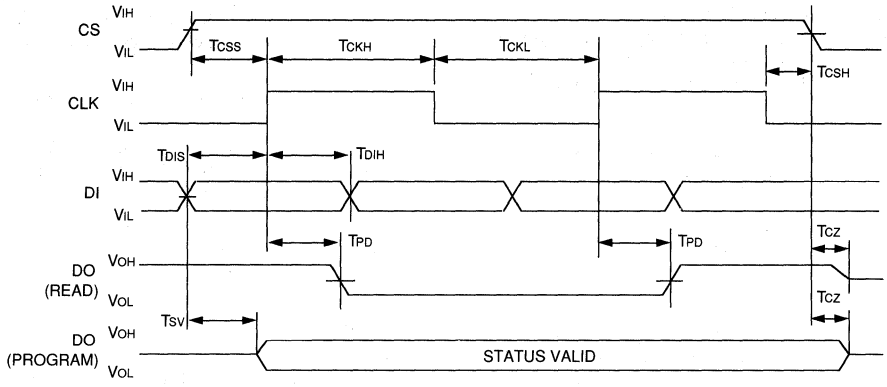
Organization (ORG)

93LC46/56/66:

When ORG is connected to VCC or floated, the (x16) memory organization is selected. When ORG is tied to VSS, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1 MHZ or less.

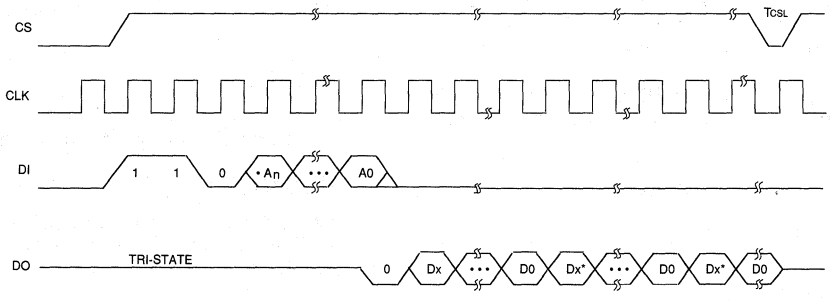
TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING

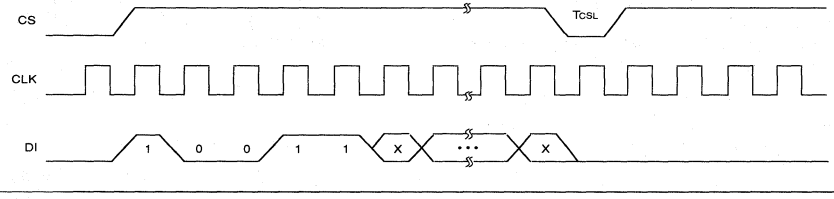


- The memory automatically cycles to the next register.

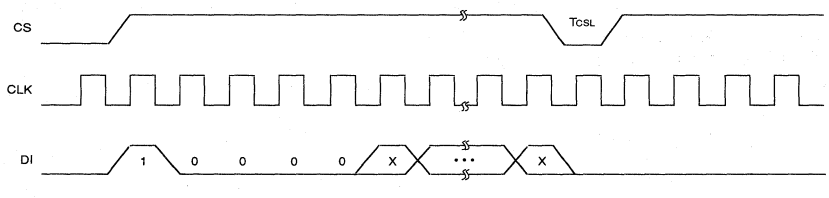
READ



EWEN

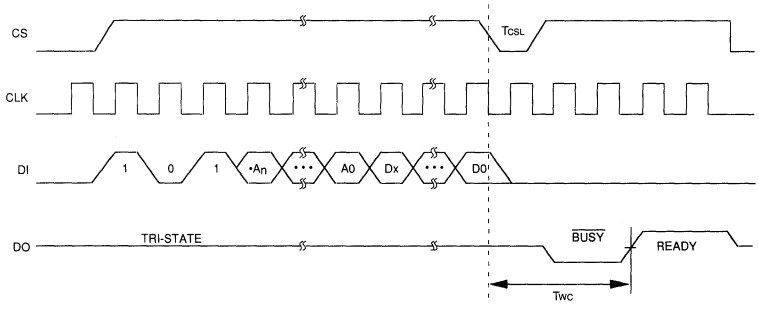


EWDS

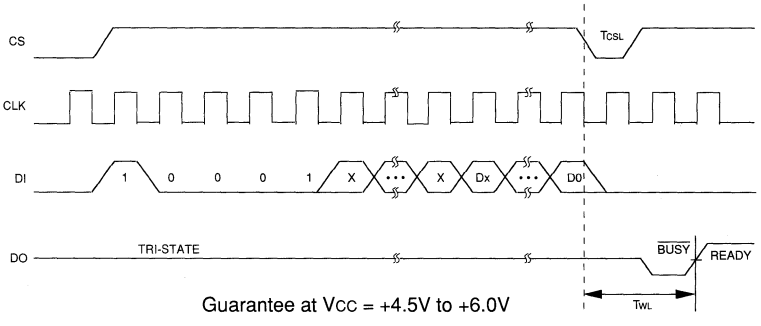


TIMING DIAGRAMS (Cont.)

WRITE

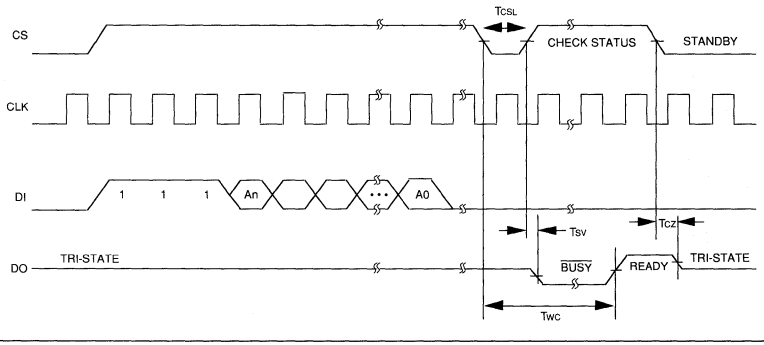


WRAL

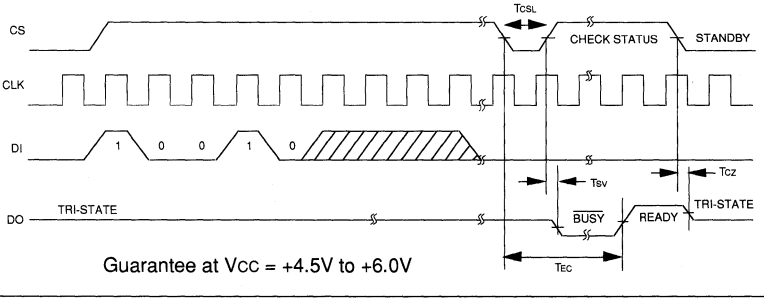


Guarantee at VCC = +4.5V to +6.0V

ERASE



ERAL



Guarantee at VCC = +4.5V to +6.0V

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

93LC46/56/66 - /P

PACKAGE:

P	PLASTIC DIP
SN	PLASTIC SOIC (150 mil Body) 8-Lead
SM	PLASTIC SOIC (207 mil Body) 8-Lead
SL	PLASTIC SOIC (150 mil Body) 14-Lead (93LC56/66)

TEMPERATURE RANGE:

Blank	0° C to +70° C
I	-40° C to +85° C
E	-40° C to +85° C

DEVICE TYPE:

Configuration	(x16) or (x8)
CMOS Serial EEPROM	93LC46/56/66
CMOS Serial EEPROM in alternate pinouts (SN package only)	93LC46X/56X/66X
CMOS Serial EEPROM (in Tape & Reel)	93LC46T/56T/66T
CMOS Serial EEPROM (in Tape & Reel)	93LC46XT/56XT/66XT

93LCS56 Product Brief

2K CMOS Serial Electrically Erasable PROM

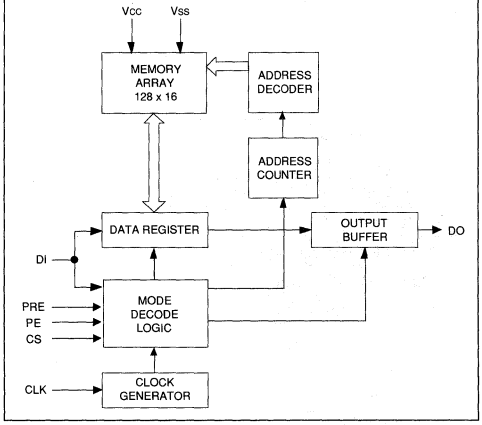
FEATURES

- Single supply with programming operation down to 2.5 volts
- Low power CMOS technology
  - 2 mA active current
  - 100 µA standby current at 5.5 V
  - 30 µA standby current at 3.0 V
- Organized as 128 x 16 bits
- Software write protection of user defined memory space
- Self timed erase and write cycles
- Automatic ERAL before WRAL
- Power on/off data protection
- Industry standard 3-wire serial I/O
- Device status signal during E/W
- Sequential READ function
- 1,000,000 E/W cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC packages
- Commercial: 0°C to +70°C
- Industrial: 40°C to +85°C

DESCRIPTION

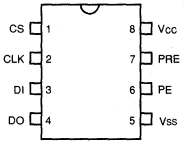
The Microchip Technology Inc. 93LCS56 is a 2048 bit low voltage serial Electrically Erasable PROM. The 2K bit memory is configured as 128 x 16 bits. A write protect register is included in order to provide a user defined region of write protected memory. All memory locations greater than or equal to the address placed in the write protect register will be protected from any attempted write or erase operation. It is also possible to protect the address in the write protect register permanently by using a one time only instruction (PRDS). Any attempt to alter data in a register whose address is equal to or greater than the address stored in the protect register will be aborted. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications.

BLOCK DIAGRAM

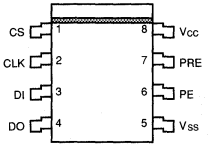


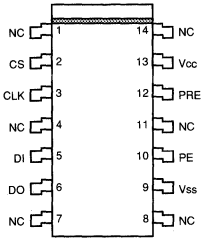
PIN CONFIGURATION

DIP Package



SO Packages





ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss.....-0.3V to Vcc +0.3V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
PE	Program Enable
PRE	Protect Register Enable
Vcc	Power Supply

DC AND AC ELECTRICAL CHARACTERISTICS

Vcc = +2.5 V to + 5.5
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C
(Note 2) Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
High level input voltage	VIH	0.7 Vcc		V	
Low level input voltage	VIL		0.3 Vcc	V	
Low level output voltage	VOL		0.4	V	IOL = 2.1 mA; Vcc = 2.0 V
High level output voltage	VOH	0.7 Vcc		V	IOH = -400 µA 5.5 V
Input leakage current	ILI	-10	10	µA	VIN = 0.1 V to 5.5 V
Output leakage current	ILO	-10	10	µA	VOUT = 0.1 V to 5.5 V
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V; Note 1 Tamb = +25°C, FCLK = 1 MHz
Operating current (read mode)	ICCO		2	mA	FCLK = 2 MHz; Vcc = 5.5 V
			1	µA	FCLK = 1 MHz; Vcc = 3.0 V
Standby current	ICCS		100	µA	CS = CLK = 0 V; Vcc = 5.5 V
			30	µA	CS = CLK = 0 V; Vcc = 3.0 V
Clock frequency	FCLK		2	MHz	Vcc > 4.5V
			1	MHz	Vcc < 4.5V
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	Relative to CLK
Chip select hold time	TCSH	0		ns	Relative to CLK
Chip select low time	TCSL	250		ns	
PRE setup time	TPRES	100		ns	Relative to CLK
PE setup time	TPES	100		ns	Relative to CLK
PRE hold time	TPREH	0		ns	Relative to CLK
PE hold time	TPEH	500		ns	Relative to CLK
Data input setup time	TDIS	100		ns	Relative to CLK
Data input hold time	TDIH	100		ns	Relative to CLK
Data output delay time	TPD		500	ns	CL = 100 pF
Data output disable time	TCZ		100	ns	CL = 100 pF
Status valid time	TSV		500	ns	CL = 100 pF
Program cycle time	TWC		10	ms	ERASE/WRITE mode (Note 3)
	TEC		20	ms	ERAL mode
	TWL		40	ms	WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz. It is periodically sampled and not 100% tested.
Note 2: Endurance at temperature greater than 85°C is rated at 10,000 erase/write cycles (minimum).
Note 3: Typical program cycle time is 2 ms per word.

93LCS66 Product Brief

4K CMOS Serial Electrically Erasable PROM

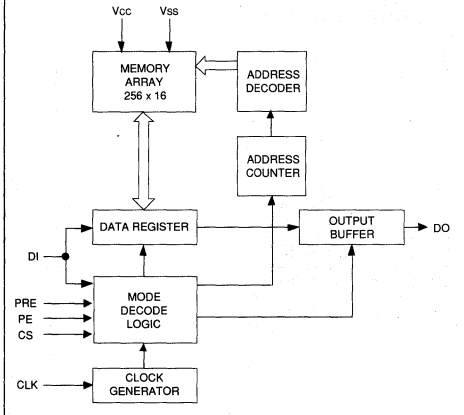
FEATURES

- Single supply with programming operation down to 2.0 volts
- Low power CMOS technology
  - 2 mA active current
  - 100 µA standby current at 5.5 V
  - 30 µA standby current at 3.0 V
- Organized as 256 x 16 bits
- Software write protection of user defined memory space
- Self timed erase and write cycles
- Automatic ERAL before WRAL
- Power on/off data protection
- Industry standard 3-wire serial I/O
- Device status signal during E/W
- Sequential READ function
- 1,000,000 E/W cycles (typical)
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC packages
- Commercial: 0°C to 70°C
- Industrial: -40°C to 85°C

DESCRIPTION

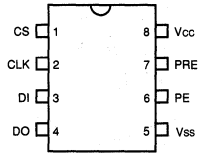
The Microchip Technology Inc. 93LCS66 is a 4096 bit low voltage serial Electrically Erasable PROM. The 4K bit memory is configured as 256 x 16 bits. A write protect register is included in order to provide a user defined region of write protected memory. All memory locations greater than or equal to the address placed in the write protect register will be protected from any attempted write or erase operation. It is also possible to protect the address in the write protect register permanently by using a one time only instruction (PRDS). Any attempt to alter data in a register whose address is equal to or greater than the address stored in the protect register will be aborted. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications.

BLOCK DIAGRAM

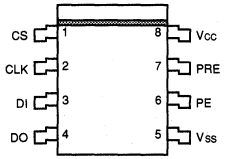


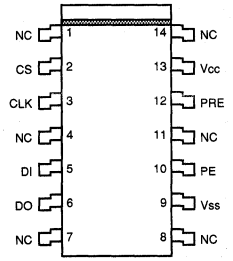
PIN CONFIGURATION

DIP Package



SO Packages





ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. VSS .....-0.3 V to VCC +0.3V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
PE	Program Enable
PRE	Protect Register Enable
VCC	Power Supply

DC AND AC ELECTRICAL CHARACTERISTICS

VCC = +2.5 V to +5.5 V (93LCS66)
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) : Tamb = -40°C to +85°C
(Note 2) Automotive (E): Tamb = -40°C to +125°C

Parameter	Symbol	Min	Max	Units	Conditions
High level input voltage	VIH	0.7 VCC		V	
Low level input voltage	VIL		0.3 VCC	V	
Low level output voltage	VOL		0.4	V	IOL = 2.1 mA; VCC = 2.0 V
High level output voltage	VOH	0.7 VCC		V	IOH = -400 µA
Input leakage current	ILI	-10	10	µA	VIN = 0.1 V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = 0.1 V to VCC
Internal capacitance (all inputs/outputs)	CINT		7	pF	VIN/VOUT = 0 V; Note 1 Tamb = +25°C, FCLK = 1 MHz
Operating current (read mode)	ICCO		2 1	mA µA	FCLK = 2 MHz; VCC = 5.5 V FCLK = 1 MHz; VCC = 3.0 V
Standby current	ICCS		100 30	µA µA	CS = CLK = 0 V; VCC = 6.0 V CS = CLK = 0 V; VCC = 3.0 V
Clock frequency	FCLK		2 1	MHz MHz	VCC > 4.5V VCC < 4.5V
Clock high time	TCKH	500		ns	
Clock low time	TCKL	500		ns	
Chip select setup time	TCSS	50		ns	Relative to CLK
Chip select hold time	TCSH	0		ns	Relative to CLK
Chip select low time	TCSL	250		ns	
PRE setup time	TPRES	100		ns	Relative to CLK
PE setup time	TPES	100		ns	Relative to CLK
PRE hold time	TPREH	0		ns	Relative to CLK
PE hold time	TPEH	500		ns	Relative to CLK
Data input setup time	TDIS	100		ns	Relative to CLK
Data input hold time	TDIH	100		ns	Relative to CLK
Data output delay time	TPD		500	ns	CL = 100 pF
Data output disable time	TCZ		100	ns	CL = 100 pF
Status valid time	TSV		500	ns	CL = 100 pF
Program cycle time	TWC		10	ms	ERASE/WRITE mode (Note 3)
	TEC		15	ms	ERAL mode
	TWL		30	ms	WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz. It is periodically sampled and not 100% tested.
Note 2: Endurance at temperature greater than 85°C is rated at 10,000 erase/write cycles (minimum).
Note 3: Typical program cycle time is 2 ms per word.

SECTION 4
EEPROM PRODUCT SPECIFICATIONS

Microchip

28C04A

4K (512 x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast Read Access Time—150ns Maximum
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100µA Standby
- Fast Byte Write Time—200µs or 1ms
- Data Retention >10 years
- High Endurance 10^4 Erase/Write Cycles
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- 5-Volt-Only Operation
- Organized 512x8 JEDEC standard pinout
  - —24 Pin Dual-In-Line Package
  - —32 Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Automotive: -40° C to 125° C

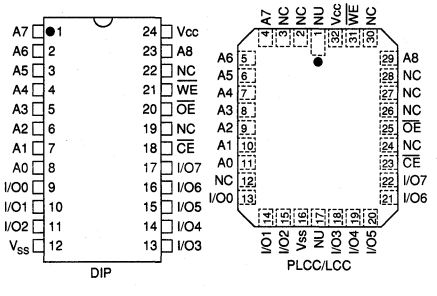
DESCRIPTION

The Microchip Technology Inc 28C04A is a CMOS 4K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C04A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C04A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

4

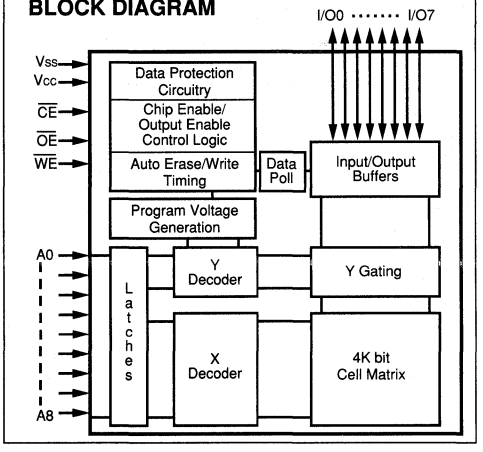
PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A8	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V
Output Voltage w.r.t. Vss .....-0.6V to Vcc+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied .....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

Vcc = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C
Automotive (E): Tamb= -40° C to 125° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0° C to 70° C) $\overline{CE}$ = VIH (-40° C to 125° C) CE = Vcc-0.3 to Vcc+1

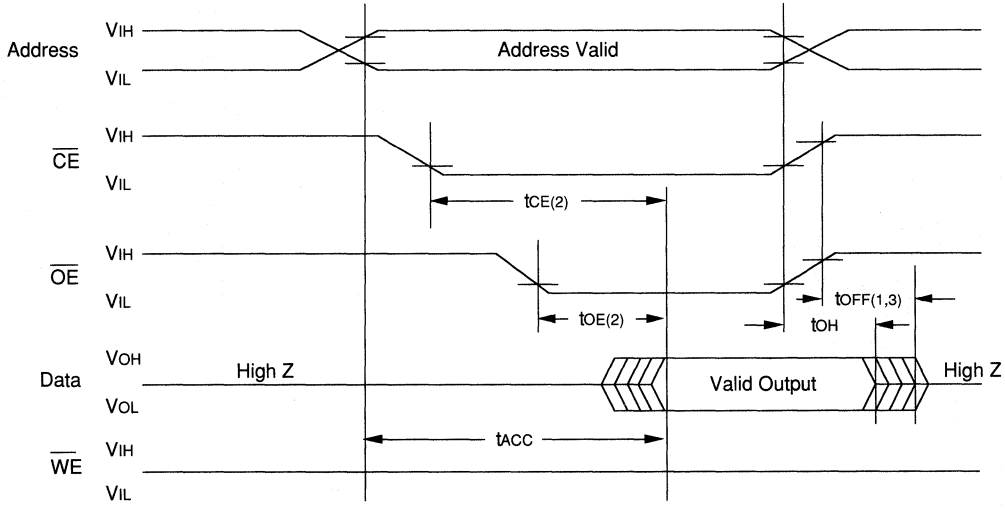
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C
Automotive (E): Tamb= -40° C to 125° C

Parameter	Sym	28C04A-15		28C04A-20		28C04A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

4

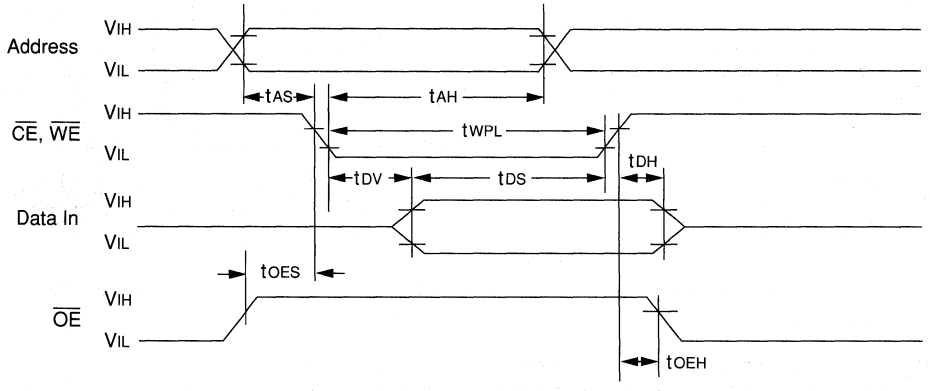
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C
Automotive (E): Tamb = -40° C to 125° C

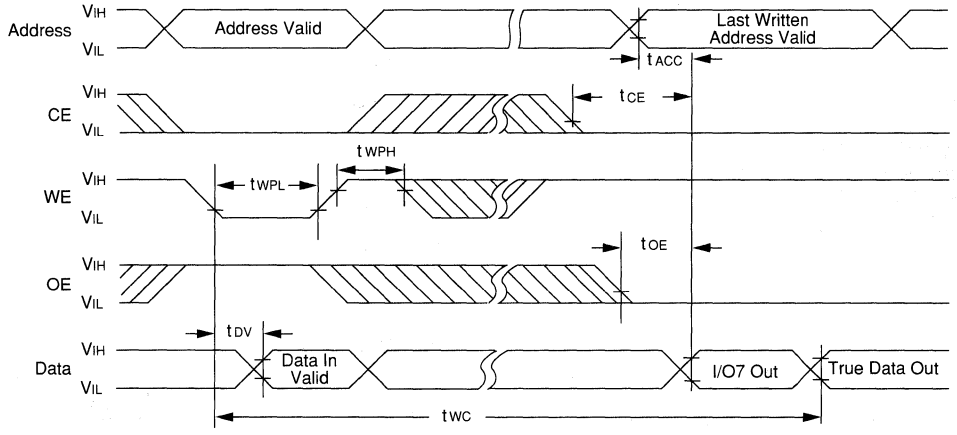
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C04A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C04AF)	t_{WC}		200	µs	100µs typical

Note: (1) A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, wichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of WE or CE, whichever occurs first.

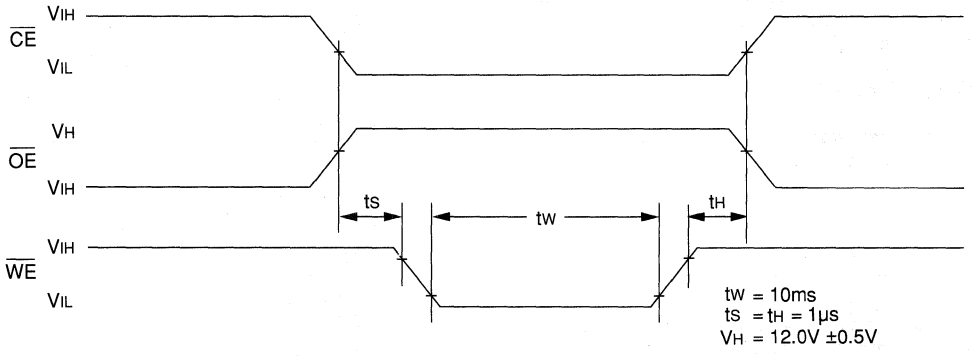
PROGRAMMING
Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



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DEVICE OPERATION

The Microchip Technology Inc 28C04A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

Read Mode

The 28C04A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 28C04A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

Write Mode

The 28C04A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

Data Polling

The 28C04A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Optional Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C04AF - 15 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier (LCC)
	L	Plastic Leaded Chip Carrier (PLCC))
	P	Plastic DIP
Temperature Range:	Blank	0° C to 70° C
	I	-40° C to 85° C
	E	-40° C to 125° C
Access Time:	15	150 nsec
	20	200 nsec
	25	250 nsec
Option:	-	= twc = 1ms
	F	= twc = 200µs
Device:	4K	(512 x 8) CMOS EEPROM

Microchip

28C16A

16K (2K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast Read Access Time—150ns Maximum
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100µA Standby
- Fast Byte Write Time—200µs or 1ms
- Data Retention >10 years
- High Endurance 10^4 Erase/Write Cycles
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- $\overline{\text{Data}}$ polling
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - —24 Pin Dual-In-Line Package
  - —32-Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Automotive: -40° C to 125° C

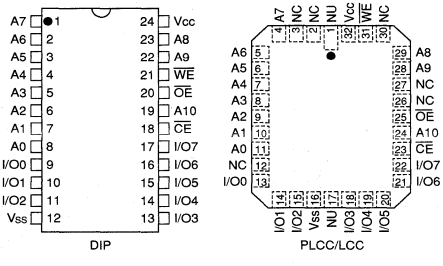
DESCRIPTION

The Microchip Technology Inc 28C16A is a CMOS 16K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C16A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C16A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

4

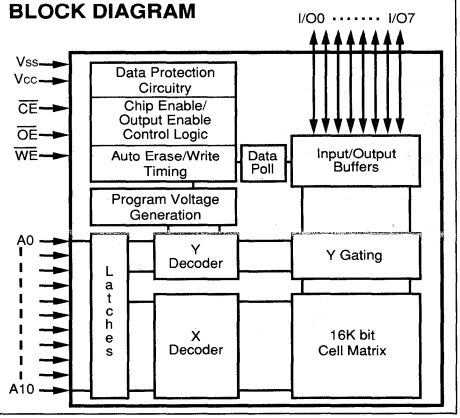
PIN CONFIGURATION

Top View



●Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
VCC	+5V Power Supply
VSS	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

VCC and input voltages w.r.t. VSS .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. VSS .....-0.6V to +13.5V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output Voltage w.r.t. VSS .....-0.6V to VCC+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied .....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C
Automotive (E): Tamb= -40° C to 125° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to VCC+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V to VCC+0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) VCC = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0° C to 70° C) $\overline{CE}$ = VIH (-40° C to 125° C) $\overline{CE}$ = VCC-0.3 to VCC+1

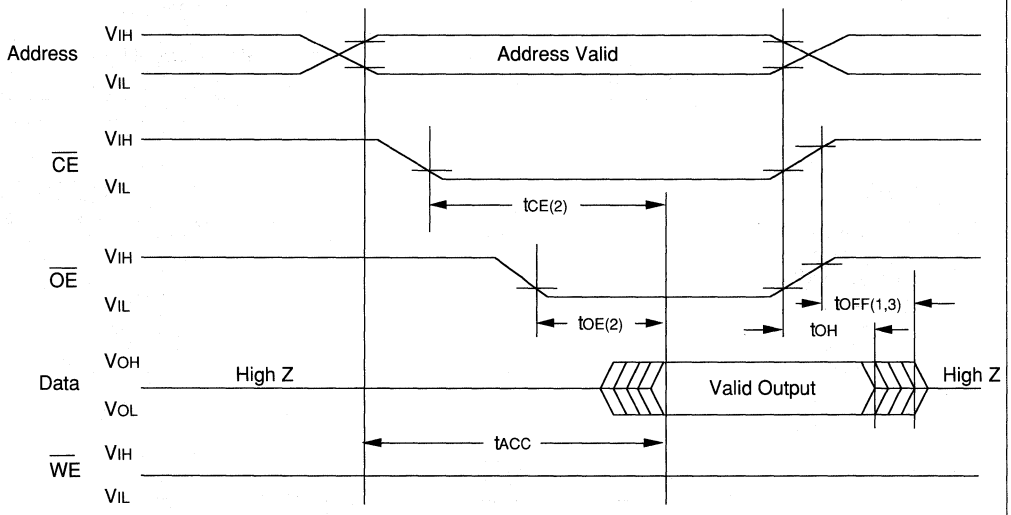
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C
Automotive (E): Tamb= -40° C to 125° C

Parameter	Sym	28C16A-15		28C16A-20		28C16A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

4

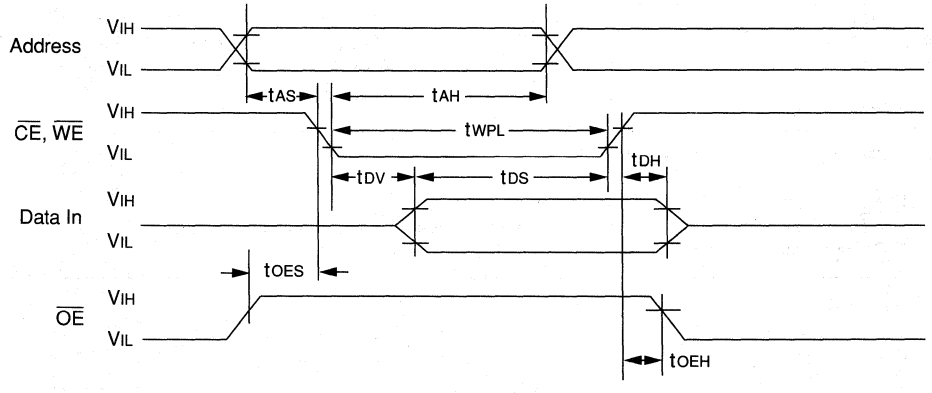
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C
Automotive (E): Tamb = -40° C to 125° C

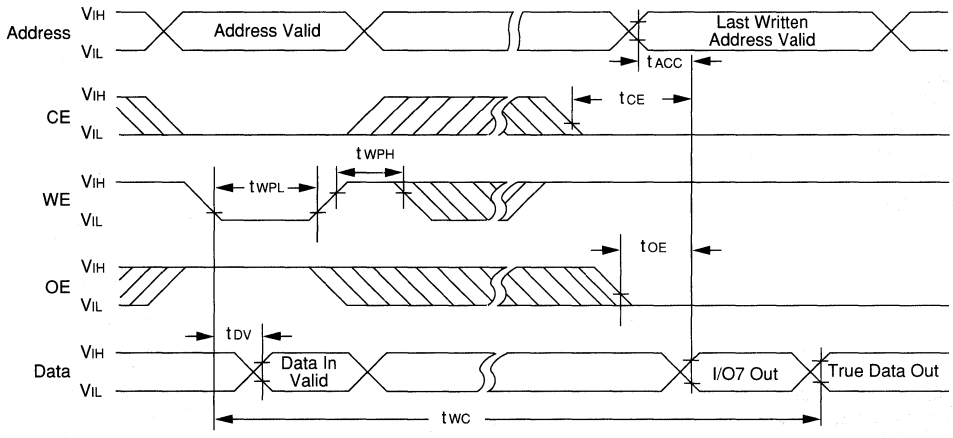
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C16A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C16AF)	t_{WC}		200	µs	100µs typical

Note: (1) A write cycle can be initiated by $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of WE or CE, whichever occurs first.

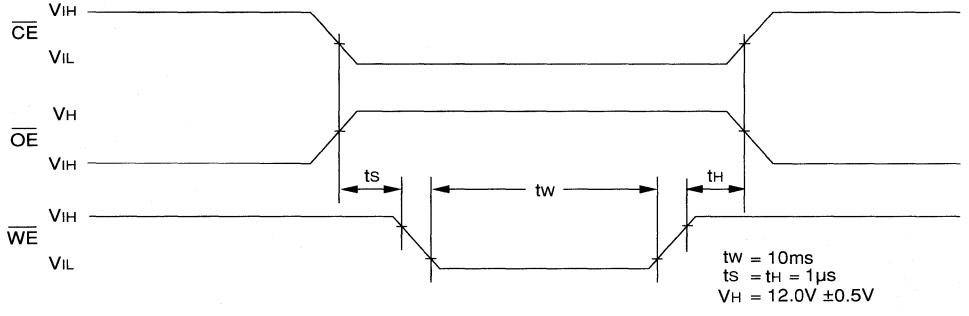
PROGRAMMING
Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C16A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

Read Mode

The 28C16A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C16A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

Write Mode

The 28C16A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

Data Polling

The 28C16A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Optional Chip Clear

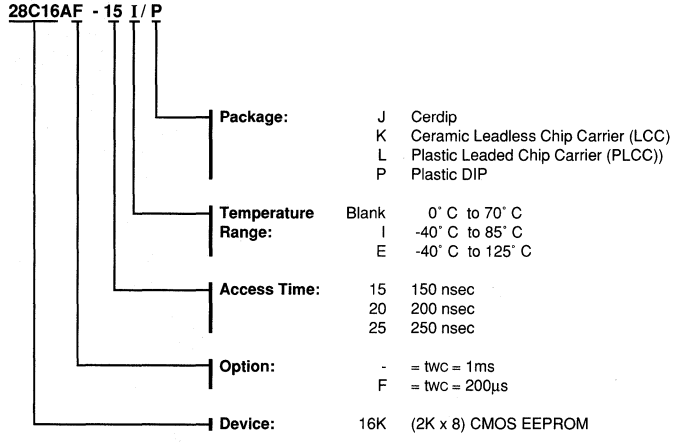
All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



28C17A

16K (2K x 8) CMOS Electrically Erasable PROM

FEATURES

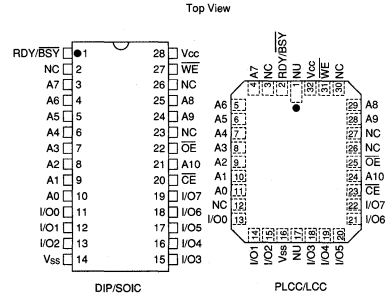
- Fast Read Access Time—150ns Maximum
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100µA Standby
- Fast Byte Write Time—200µs or 1ms
- Data Retention >10 years
- High Endurance 10^4 Erase/Write Cycles
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - —28 Pin Dual-In-Line Package
  - —32-Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Automotive: -40° C to 125° C

DESCRIPTION

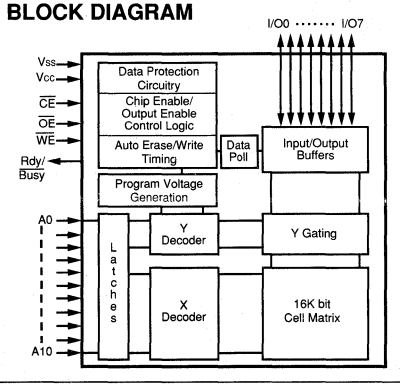
The Microchip Technology Inc 28C17A is a CMOS 16K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C17A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

4

PIN CONFIGURATION



BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
VCC	+5V Power Supply
VSS	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

VCC and input voltages w.r.t. VSS .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. VSS .....-0.6V to +13.5V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output Voltage w.r.t. VSS .....-0.6V to VCC+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied.....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C
Automotive (E): Tamb= -40° C to 125° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN= -0.1V to VCC+1
Input Capacitance		CIN		10	pF	VIN= 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH= -400µA IOL= 2.1mA
Output Leakage		ILO	-10	10	µA	VOUT= -0.1V to VCC+0.1V
Output Capacitance		COUT		12	pF	VIN= 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) VCC = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0° C to 70° C) $\overline{CE}$ = VIH (-40° C to 125° C) $\overline{CE}$ = VCC-0.3 to VCC+1

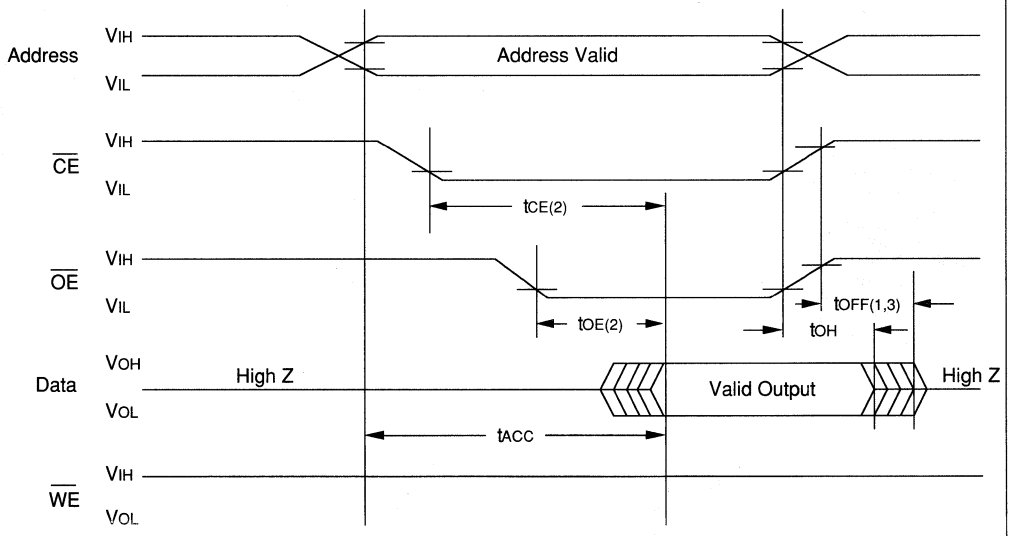
Note: (1) AC power supply current above 5 MHz: 1 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C
Automotive (E): Tamb = -40° C to 125° C

Parameter	Sym	28C17A-15		28C17A-20		28C17A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

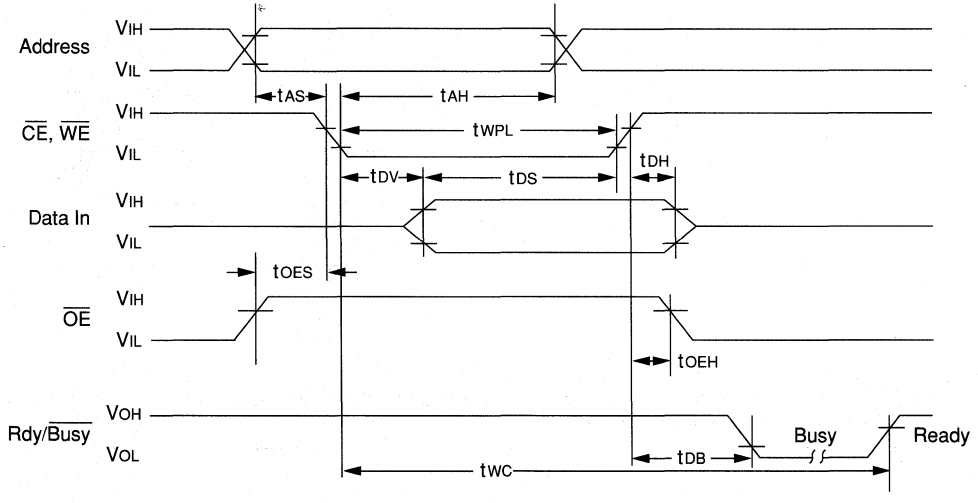
BYTE WRITE AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C
Automotive (E): Tamb = -40° C to 125° C

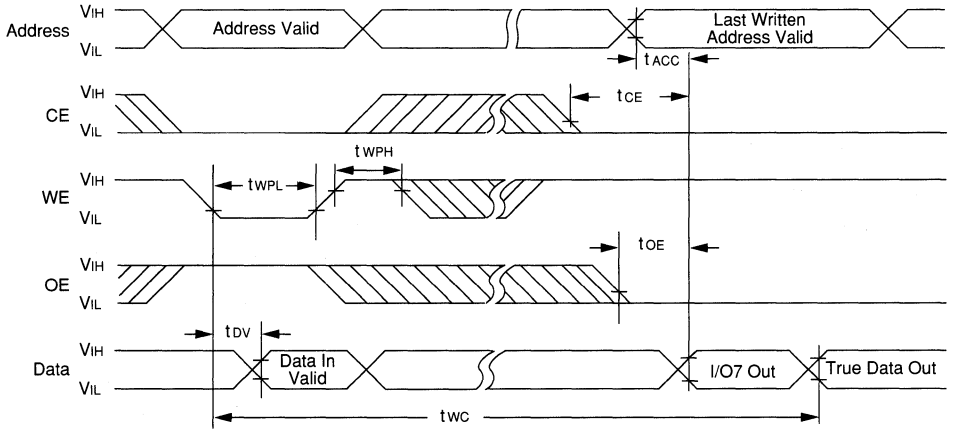
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Time to Device Busy	t_{DB}	2	50	ns	
Write Cycle Time (28C17A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C17AF)	t_{WC}		200	µs	100µs typical

Note: (1) A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, wichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of WE or CE, whichever occurs first.

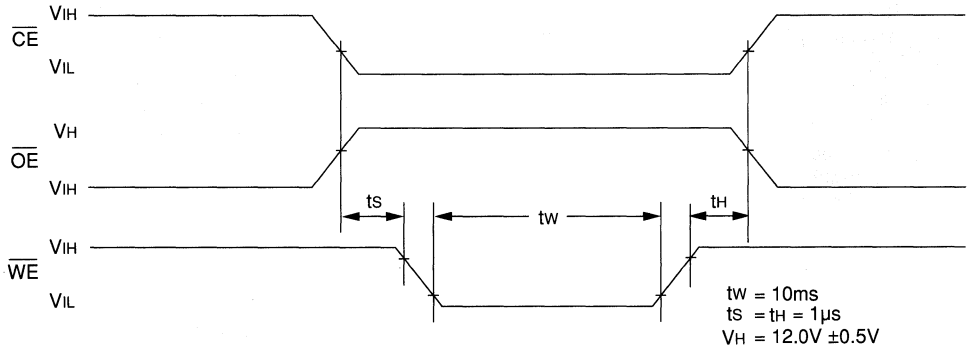
PROGRAMMING Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C17A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.
(2) X = Any TTL level.

Read Mode

The 28C17A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C17A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

Write Mode

The 28C17A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C17A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C17A has completed writing and is ready to accept another cycle.

$\overline{Data}$ Polling

The 28C17A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Optional Chip Clear

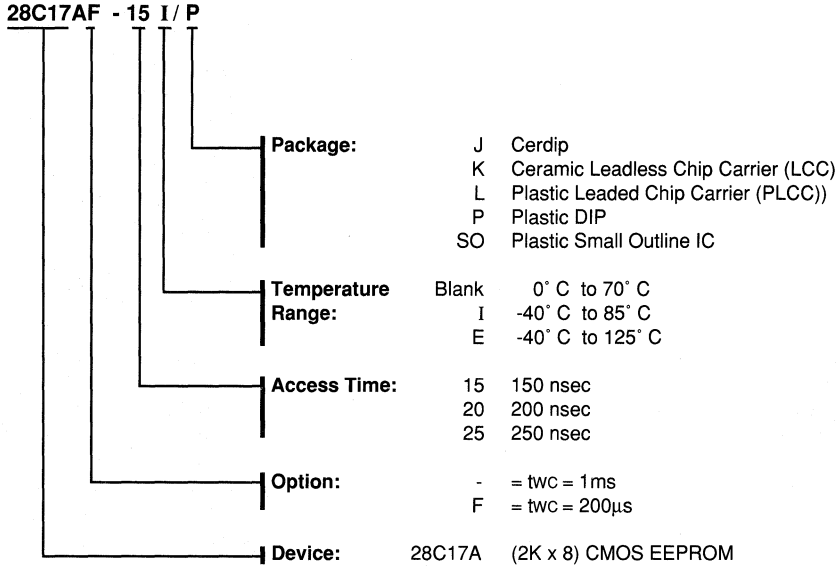
All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

28C64A

64K (8K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast Read Access Time—150ns Maximum
- CMOS Technology for Low Power Dissipation
  - —30mA Active
  - —100µA Standby
- Fast Byte Write Time—200µs or 1ms
- Data Retention >10 years
- High Endurance 10^4 Erase/Write Cycles
- Automatic Write Operation
  - —Internal Control Timer
  - —Auto-Clear Before Write Operation
  - —On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
  - —Vcc Detector
  - —Pulse Filter
  - —Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 8Kx8 JEDEC Standard Pinout
  - —28 Pin Dual-In-Line Package
  - —32-Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Automotive: -40° C to 125° C

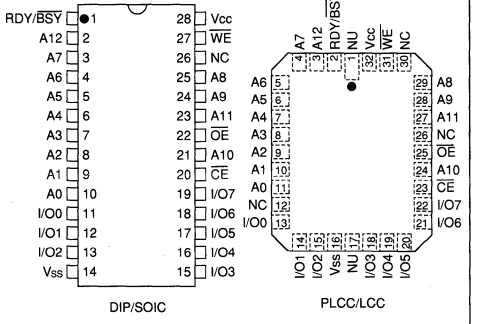
DESCRIPTION

The Microchip Technology Inc 28C64A is a CMOS 64K non-volatile electrically Erasable and Programmable Read Only Memory. The 28C64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

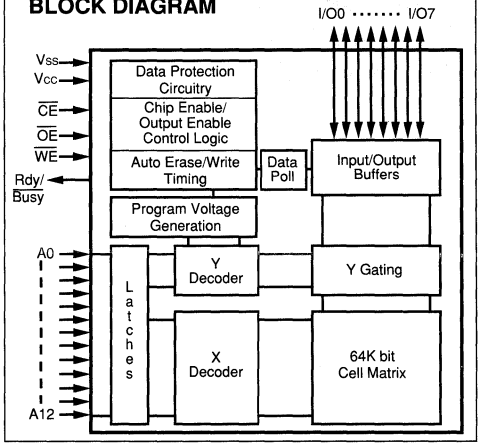
4

PIN CONFIGURATION

Top View



BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

V_{CC} and input voltages w.r.t. V_{SS} .....-0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. V_{SS} .....-0.6V to +13.5V
Voltage on A9 w.r.t. V_{SS} .....-0.6V to +13.5V
Output Voltage w.r.t. V_{SS} .....-0.6V to V_{CC}+0.6V
Storage temperature .....-65° C to 125° C
Ambient temp. with power applied.....-50° C to 95° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ / WRITE OPERATION
DC Characteristics

V_{CC} = +5V ±10%
Commercial (C): Tamb= 0° C to 70° C
Industrial (I): Tamb= -40° C to 85° C

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN}= -0.1V to V_{CC}+1
Input Capacitance		C_{IN}		10	pF	V_{IN} = 0V; Tamb = 25° C; f = 1 MHz
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
Output Leakage		I_{LO}	-10	10	µA	V_{OUT}= -0.1V to V_{CC}+0.1V
Output Capacitance		C_{OUT}		12	pF	V_{IN} = 0V; Tamb = 25° C; f = 1 MHz
Power Suppy Current, Active	TTL input	I_{CC}		30	mA	f = 5 MHz (Note 1) V_{CC} = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	$I_{CC(S)TTL}$ $I_{CC(S)TTL}$ $I_{CC(S)CMOS}$		2 3 100	mA mA µA	$\overline{CE}$ = V_{IH} (0° C to 70° C) $\overline{CE}$ = V_{IH} (-40° C to 85° C) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1

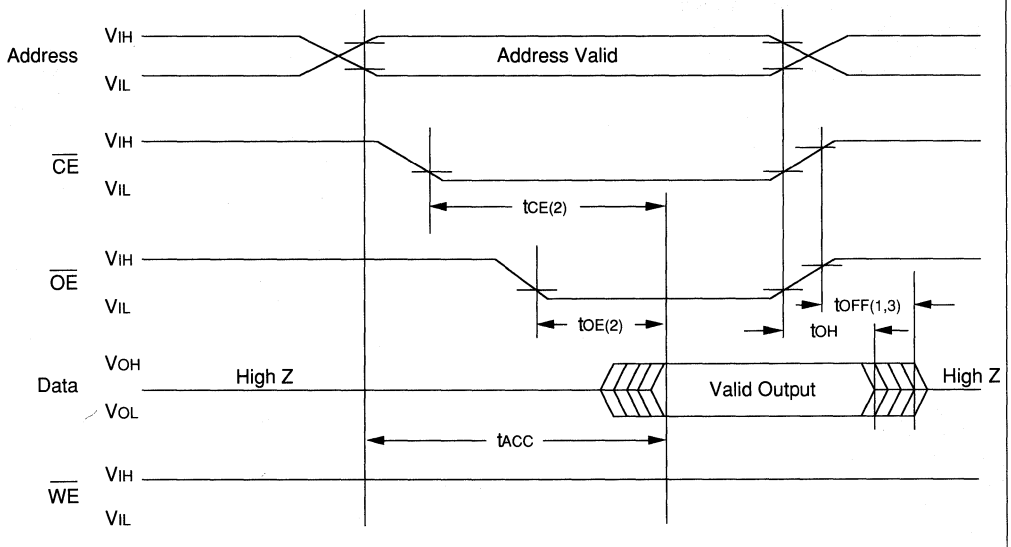
Note: (1) AC power supply current above 5 MHz: 2 mA/MHz

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

Parameter	Sym	28C64A-15		28C64A-20		28C64A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0		0		0		ns	

READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

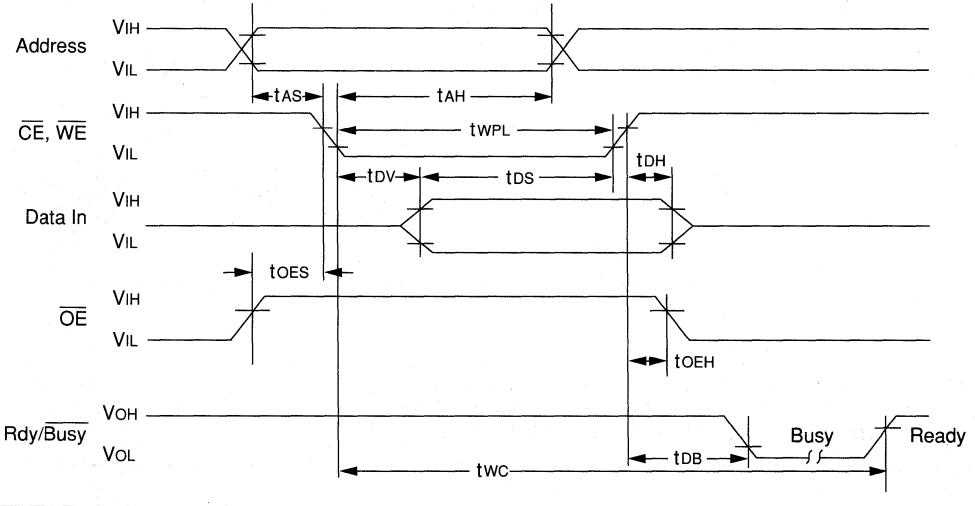
BYTE WRITE
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise/Fall Times: 20 nsec
Ambient Temperature: Commercial (C): Tamb = 0° C to 70° C
Industrial (I): Tamb = -40° C to 85° C

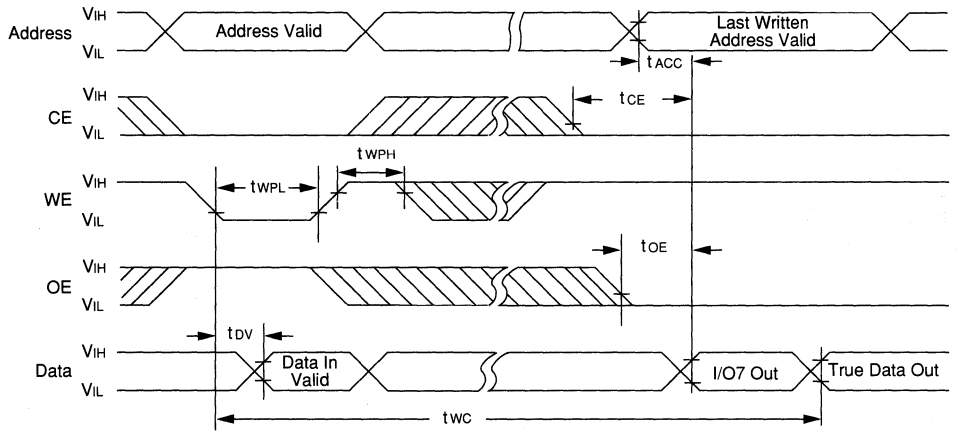
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Time to Device Busy	t_{DB}	-	50	ns	
Write Cycle Time (28C64A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C64AF)	t_{WC}		200	µs	100µs typical

Note: (1) A write cycle can be initiated $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
(2) Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

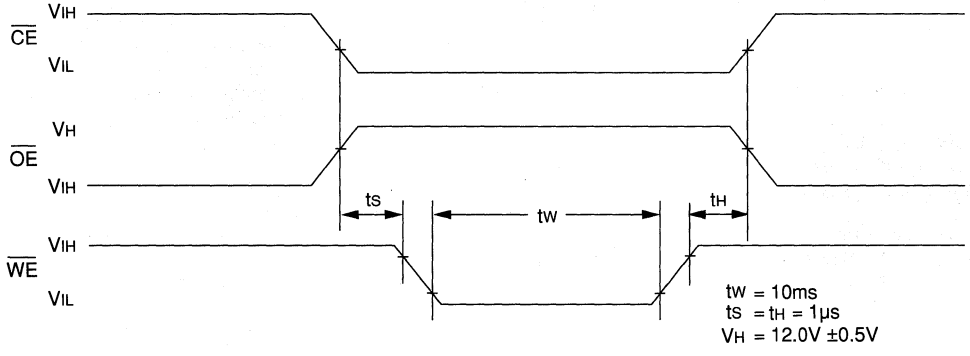
PROGRAMMING
Waveforms



$\overline{\text{DATA}}$ POLLING Waveforms



CHIP CLEAR Waveforms



SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

DEVICE OPERATION

The Microchip Technology Inc 28C64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.
(2) X = Any TTL level.

Read Mode

The 28C64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

Standby Mode

The 28C64A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

Write Mode

The 28C64A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C64A has completed writing and is ready to accept another cycle.

$\overline{Data}$ Polling

The 28C64A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 1FE0 to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

Optional Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES:

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

28C64AF - 15 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier (LCC)
	L	Plastic Leaded Chip Carrier (PLCC))
	P	Plastic DIP
	SO	Plastic Small Outline IC
Temperature Range:	Blank	0° C to 70° C
	I	-40° C to 85° C
	E	-40° C to 125°C
Access Time:	15	150 nsec
	20	200 nsec
	25	250 nsec
Option:	-	= twc = 1ms
	F	= twc = 200µs
	X	Pin 1 NC (Pin 2 PLCC), twc = 1ms
Device:	64K	(8K x 8) CMOS EEPROM

SECTION 5
EPROM PRODUCT SPECIFICATIONS

27C64

64K (8K x 8) CMOS EPROM

FEATURES

- High speed performance
  —120ns maximum access time
- CMOS Technology for low power consumption
  —20mA Active current
  —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin Chip carrier (leadless or plastic)
  —28-pin SOIC package
  —28-pin TSOP package
  —Tape and reel
- Available for extended temperature ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C
  —Automotive: -40° C to 125° C

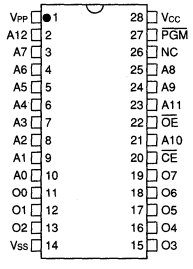
DESCRIPTION

The Microchip Technology Inc 27C64 is a CMOS 64K bit (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

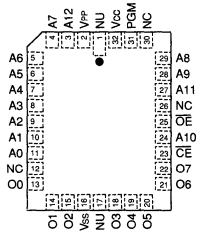
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. U.V. erasable versions are also available.

5

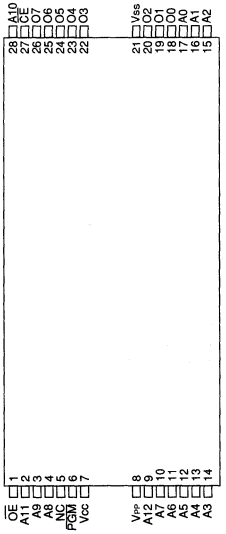
PIN CONFIGURATIONS
Top View



DIP/SOIC



PLCC/LCC



TSOP

PIN FUNCTION TABLE	
Name	**Function**
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN= 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH= -400µA IOL= 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT= 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN= 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT= 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL= -0.1 to 0.8 V; VIH= 2.0 to VCC; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

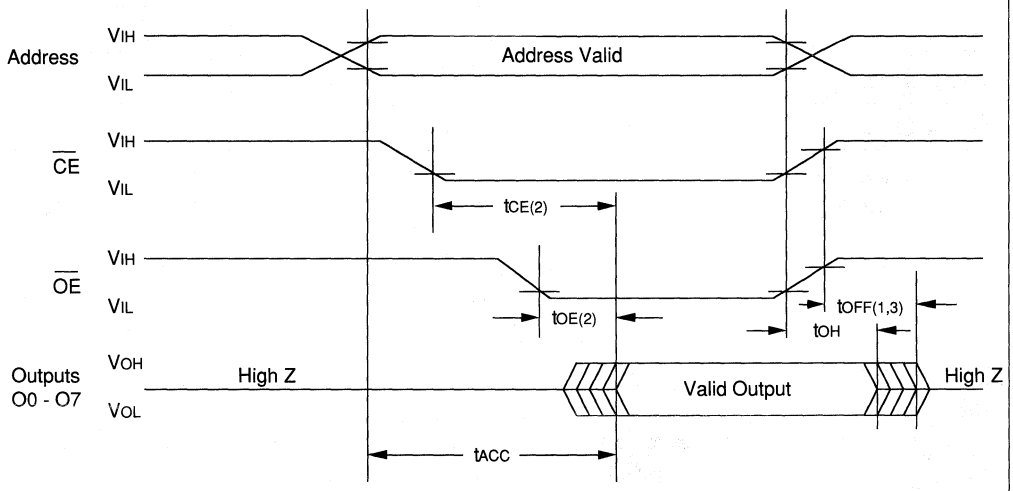
* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 8mA up to maximum frequency.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100 pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Sym	27C64-12		27C64-15		27C64-17		27C64-20		27C64-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		120		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		120		150		170		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		65		70		70		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0		0		0		0		0		ns	

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

5

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		20	mA	Note 1
V_{PP} Current,program		I_{PP2}		25	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

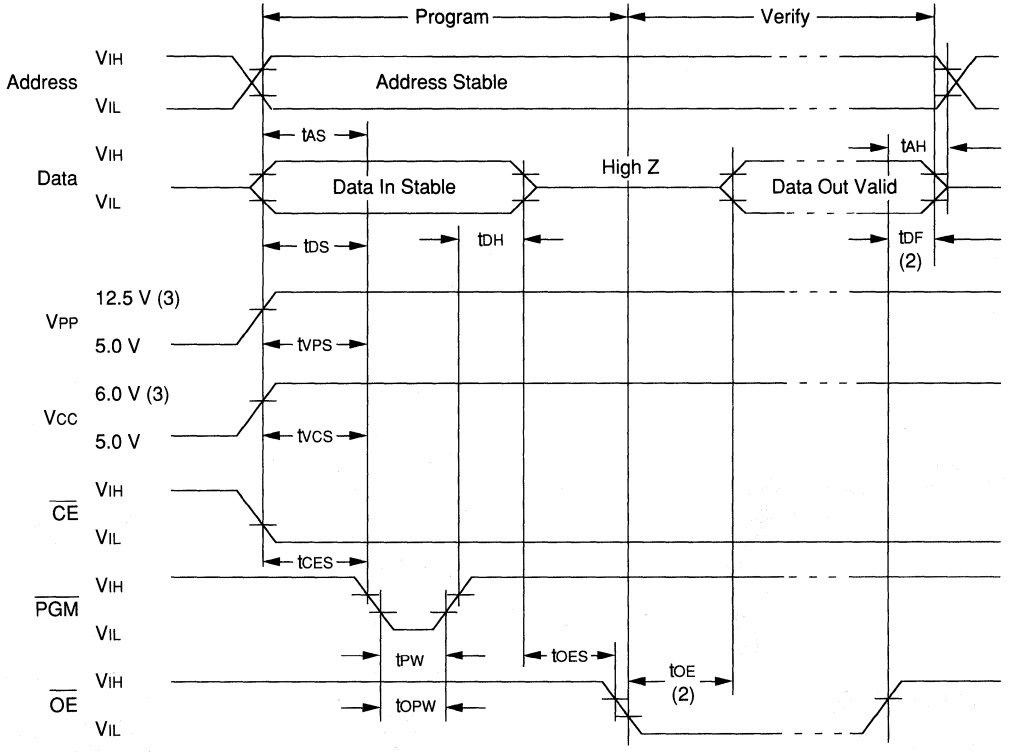
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms (1)



Notes: (1) The input timing reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.0 V ±0.25 V, $V_{PP} = V_H$ = 12.5 V ±0.25 V for fast programming algorithm and V_{CC} = 6.5 V ±0.25 V, $V_{PP} = V_H$ = 13.0 V ±0.25 V for Express algorithm.

5

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

Standby Mode

The standby mode is defined when the $\overline{CE}$ and $\overline{PGM}$ pins are both high (V_{IH}).

When these conditions are met, the supply current will drop from 20mA to 100µA.

Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm² for approximately 20 minutes.

Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to the proper voltage,
b) V_{PP} is brought to the proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

Identity Mode

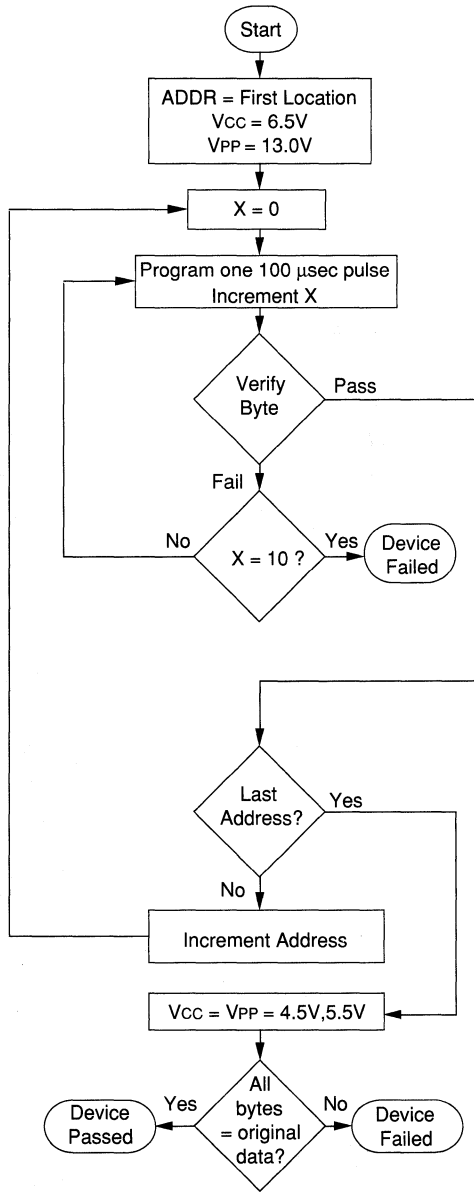
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	0	0	0	0	0	0	1	0	02

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C64 - 25 I / K

Package:		J	Cerdip
		K	Ceramic Leadless Chip Carrier
		L	Plastic Leaded Chip Carrier
		P	Plastic DIP
		SO	Plastic SOIC
		TS	Plastic TSOP
Temperature Range:		-	0° C to 70° C
		I	-40° C to 85° C
		E	-40° C to 125° C
Access Time:		12	120 nsec
		15	150 nsec
		17	170 nsec
		20	200 nsec
		25	250 nsec
Device:		27C64	64K (8K x 8) CMOS EPROM

Microchip

27C128

128K (16K x 8) CMOS EPROM

FEATURES

- High speed performance
  - —120ns Maximum access time
- CMOS Technology for low power consumption
  - —20mA Active current
  - —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 16K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32-pin Chip carrier (leadless or plastic)
  - —28-pin SOIC package
  - —28-pin TSOP package
  - —Tape and reel
- Available for extended temperature ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Automotive: -40° C to 125° C

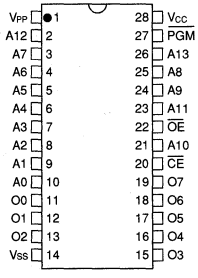
DESCRIPTION

The Microchip Technology Inc 27C128 is a CMOS 128K bit (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

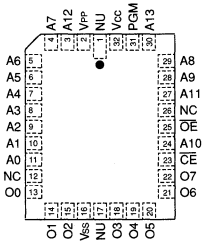
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

5

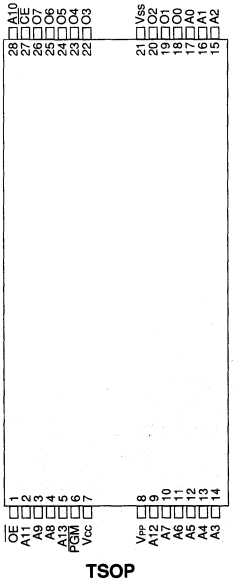
PIN CONFIGURATIONS
Top View



DIP/SOIC



PLCC/LCC



TSOP

PIN FUNCTION TABLE	
Name	**Function**
A0 - A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC + 1V
Storage temperature ..... -65° C to 150° C
Ambient temp. with power applied ..... -65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V; Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

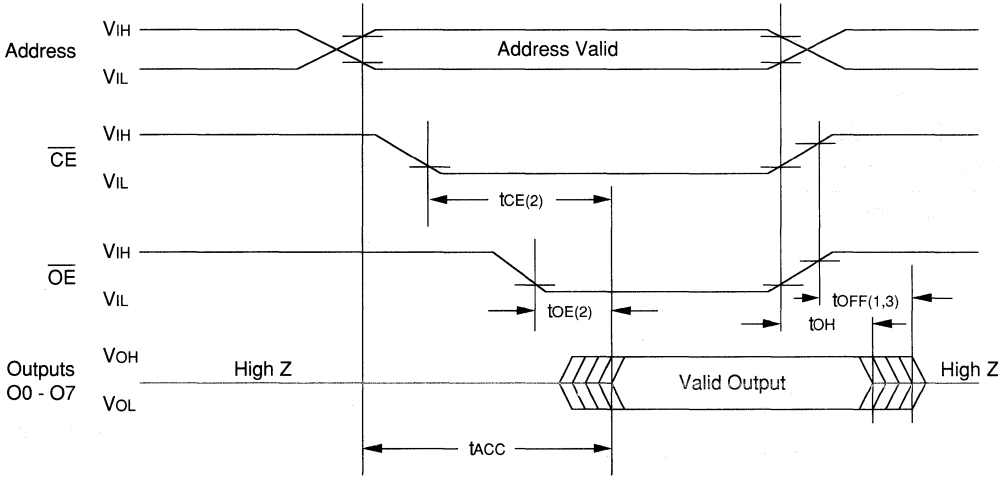
* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 8mA up to maximum frequency.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Sym	27C128-12		27C128-15		27C128-17		27C128-20		27C128-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		120		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		120		150		170		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		65		70		70		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0		0		0		0		0		ns	

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

5

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		20	mA	Note 1
V_{PP} Current,program		I_{PP2}		25	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

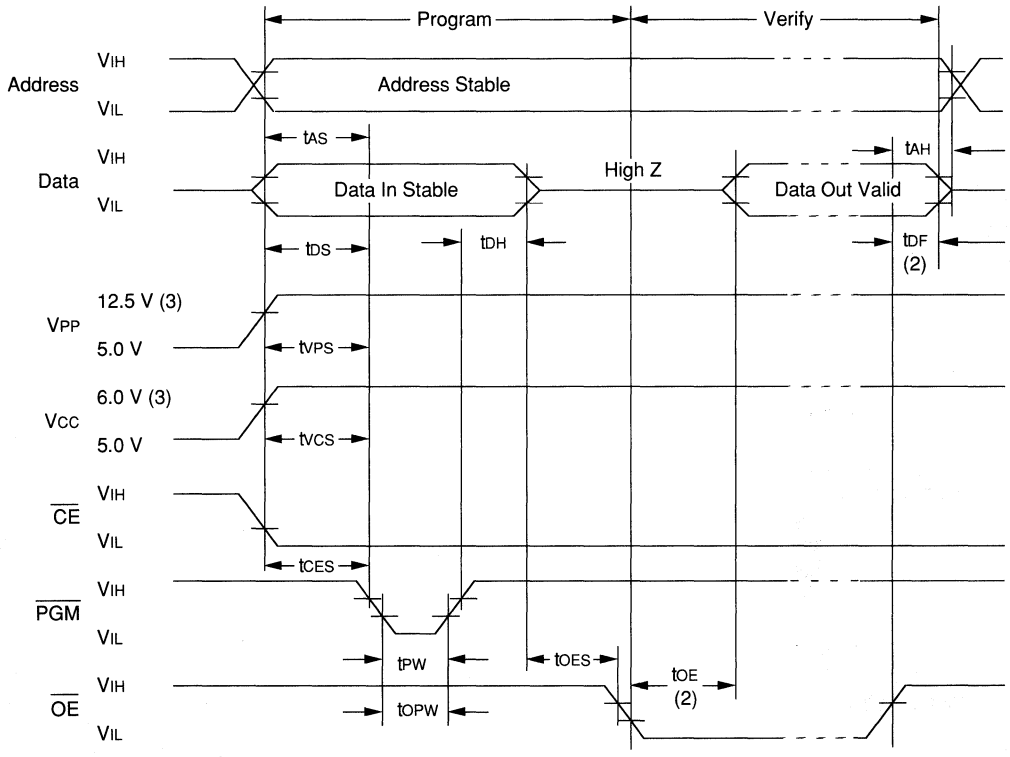
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms (1)



Notes: (1) The input timing reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.0 V ±0.25 V, V_{PP} = V_H = 12.5 V ±0.25 V for fast programming algorithm.

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MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

Standby Mode

The standby mode is defined when the $\overline{CE}$ and $\overline{PGM}$ pins are both high (V_{IH}).

When these conditions are met, the supply current will drop from 20mA to 100µA.

Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm² for approximately 20 minutes.

Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to the proper voltage,
b) V_{PP} is brought to the proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

Identity Mode

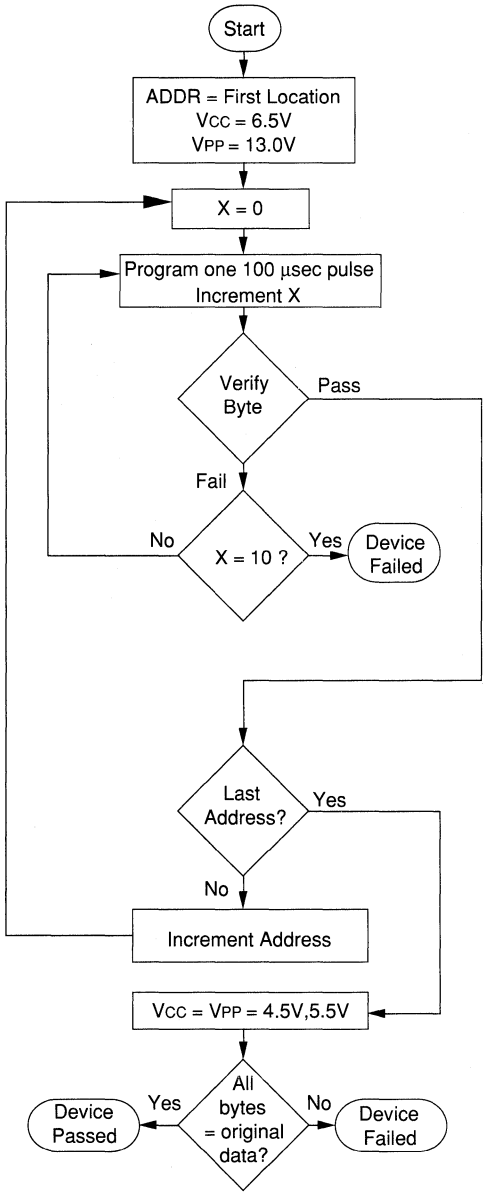
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	0	0	1	1	83

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C128 - 25 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Plastic TSOP
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
	E	-40° C to 125° C
Access Time:	12	120 nsec
	15	150 nsec
	17	170 nsec
	20	200 nsec
	25	250 nsec
Device:	27C128	128K (16K x 8) CMOS EPROM

Microchip

27C256

256K (32K x 8) CMOS EPROM

FEATURES

- High speed performance
  —90ns maximum access time
- CMOS Technology for low power consumption
  —20mA Active current
  —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin Chip carrier (leadless or plastic)
  —28-pin SOIC package
  —28-pin TSOP
  —Tape and reel
- Available for extended temperature ranges:
  —Commercial: 0° C to +70° C
  —Industrial: -40° C to +85° C
  —Automotive: -40° C to +125° C

DESCRIPTION

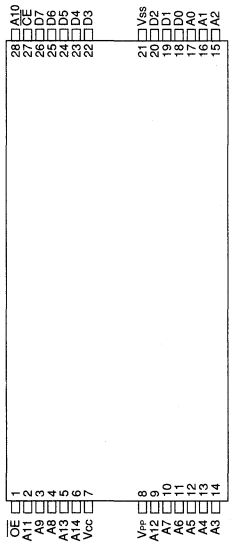
The Microchip Technology Inc 27C256 is a CMOS 256K bit (electrically) Programmable Read Only Memory. The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

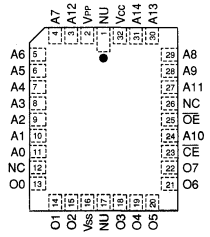
5

PIN CONFIGURATIONS

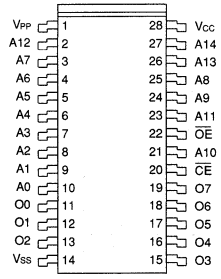
Top View



TSOP



PLCC/LCC



DIP/SOIC

PIN FUNCTION TABLE	
Name	**Function**
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC + 1.0V
Storage temperature ..... -65° C to 150° C
Ambient temp. with power applied ..... -65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current	all	Read Mode	IPP		100	µA	VPP = 5.5V
VPP Read Voltage	all	Read Mode	VPP	VCC-0.7	VCC	V	Note 2

* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 5mA up to maximum frequency.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

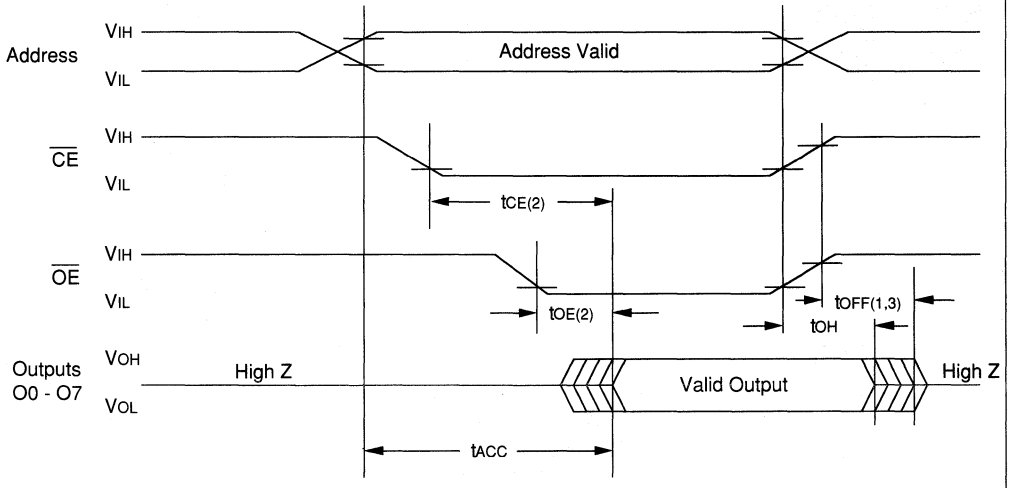
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Sym	27C256-90*		27C256-10*		27C256-12		27C256-15		27C256-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		90		100		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		90		100		120		150		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		40		45		55		65		75	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0		0		0		0		0		ns	

* -10, -90 AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 1.5V and V_{OL}= 1.5V
Output Load: 1 TLL Load + 30pF

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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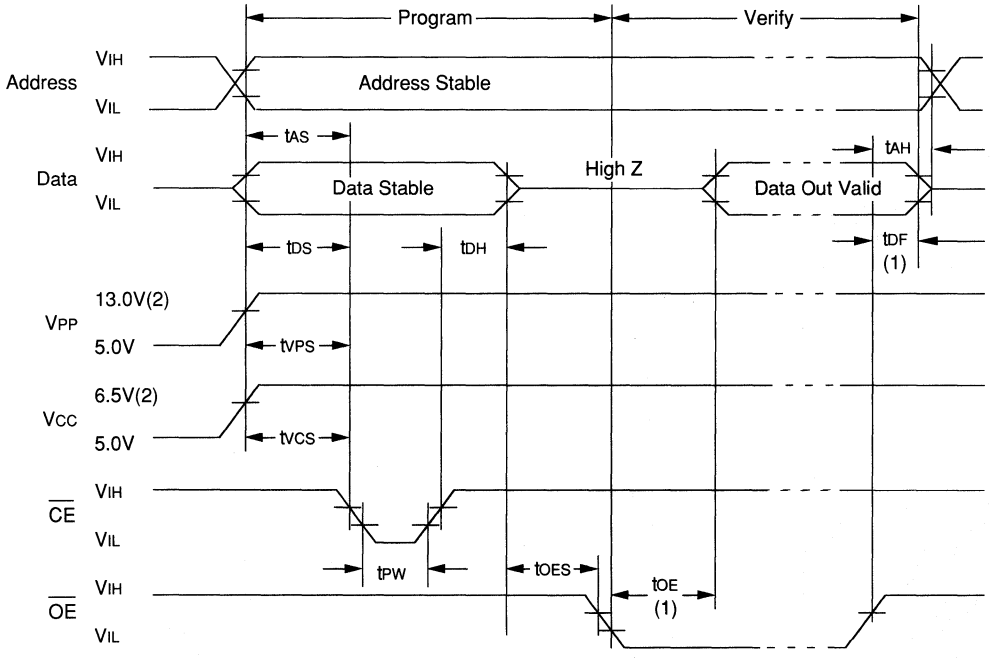
PROGRAMMING **DC Characteristics**		Ambient Temperature: Tamb = 25° C ±5° C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		20	mA	Note 1
V_{PP} Current, program		I_{PP2}		25	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING **AC Characteristics** for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V Output Load: 1 TTL Load + 100 pF Ambient Temperature: Tamb = 25° C ±5° C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5 V ±0.25 V, VPP = VH = 13.0 V ±0.25 V for express algorithm

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MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these condition are met, the supply current will drop from 20mA to 100μA.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and a program is not defined.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000μW/cm^2 for approximately 20 minutes.

Programming Mode

The express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) The $\overline{OE}$ pin is high and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) The $\overline{CE}$ pin is high and
d) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

Identity Mode

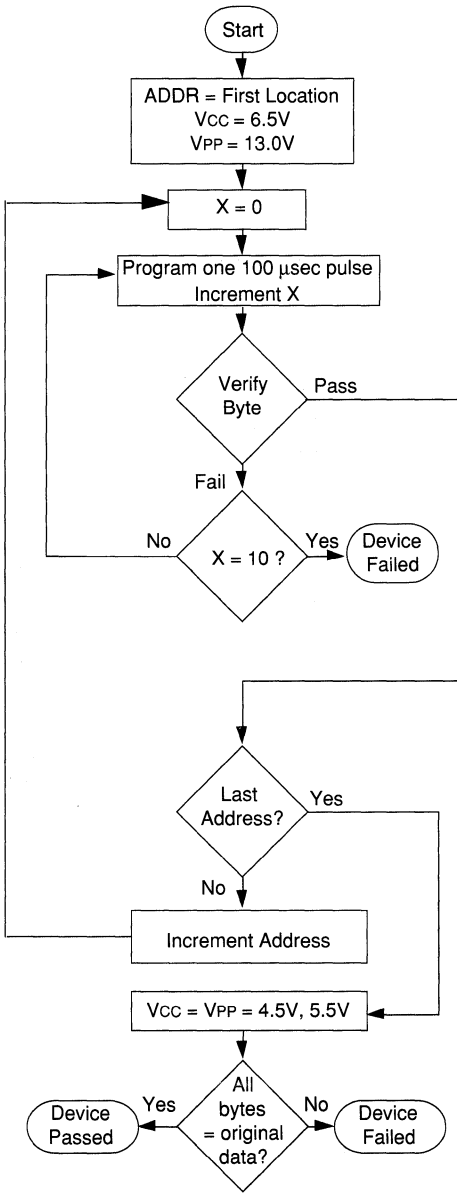
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C256 - 25 I / TS

Package:	J	CERDIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	TSOP
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
	E	-40° C to 125° C
Access Time:	90	90 nsec
	10	100 nsec
	12	120 nsec
	15	150 nsec
	20	200 nsec
Device:	27C256	256K (32K x 8) CMOS EPROM

Microchip

27C512

512K (64K x 8) CMOS EPROM

FEATURES

- High speed performance
  - —90ns access time available
- CMOS Technology for low power consumption
  - —35mA Active current
  - —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- High speed express programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32-pin Chip carrier (leadless or plastic)
  - —28-pin SOIC package
  - —28-pin TSOP
  - —Tape and reel
- Available for extended temperature ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Automotive: -40° C to 125° C

DESCRIPTION

The Microchip Technology Inc 27C512 is a CMOS 512K bit (electrically) Programmable Read Only Memory. The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexability in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape or reel packaging is also available for PLCC or SOIC packages. U.V. erasable versions are also available.

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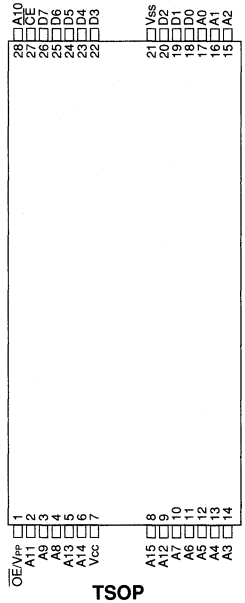
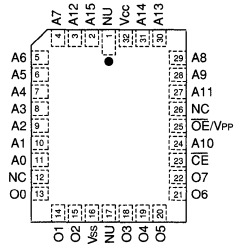
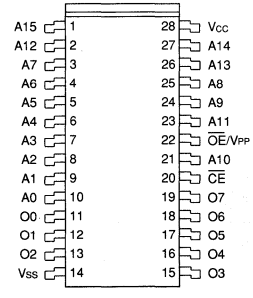
PIN CONFIGURATIONS
Top View



TSOP



PLCC/LCC



DIP/SOIC

PIN FUNCTION TABLE	
Name	**Function**
A0 - A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/ Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC + 1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN= 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT= 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT= 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC ICC		35 45	mA mA	VCC = 5.5V f = 1MHz; $\overline{OE}$/VPP= $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC;
Power Supply Current, Standby	S X S	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 2mA/MHz.

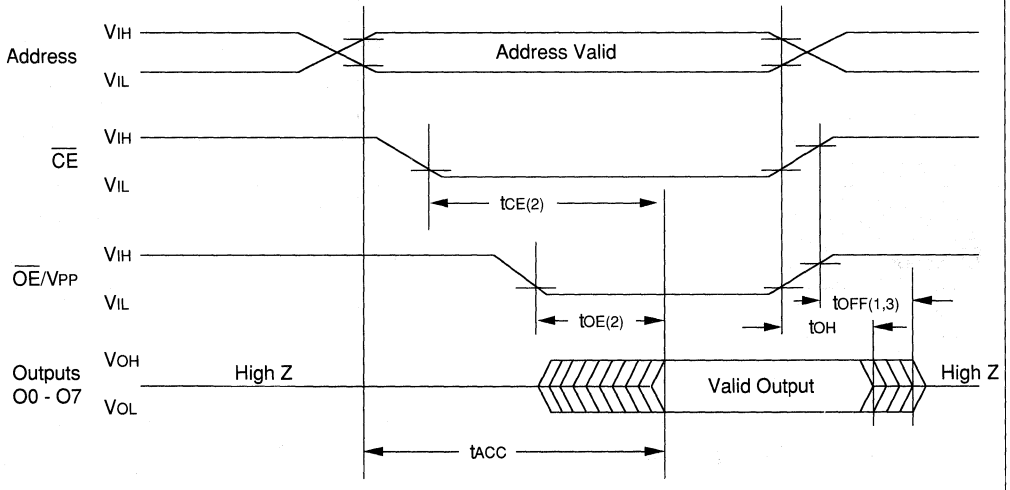
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 2.0V and V_{OL} = 0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Sym	27C512-90*		27C512-10*		27C512-12		27C512-15		27C512-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		90		100		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$/VPP = VIL
$\overline{CE}$ to Output Delay	tCE		90		100		120		150		200	ns	$\overline{OE}$/VPP = VIL
$\overline{OE}$ to Output Delay	tOE		40		45		55		65		75	ns	$\overline{CE}$ = VIL
$\overline{OE}$ to Output High Impedance	tOFF	0	35	0	35	0	40	0	45	0	55	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$/VPP, whichever occured first	tOH	0		0		0		0		0		ns	

* -10, -90 AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30pF

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$/VPP or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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PROGRAMMING
DC Characteristics

Ambient Temperature: 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions (See Note 1)
Input Voltages	Logic "1"	V_{IH}	2.0	V_{CC}+1	V	
	Logic "0"	V_{IL}	-0.1	0.8	V	
Input Current (all inputs)		I_{IL}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1"	V_{OH}	2.4		V	I_{OH} = -400µA
	Logic "0"	V_{OL}		0.45	V	I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		35	mA	
$\overline{OE}/V_{PP}$ Current, program		I_{PP2}		25	mA	$\overline{CE}$ = V_{IL}
A9 Product Identification		V_{ID}	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before the V_{PP} voltage on $\overline{OE}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{OE}/V_{PP}$.

PROGRAMMING
AC Characteristics

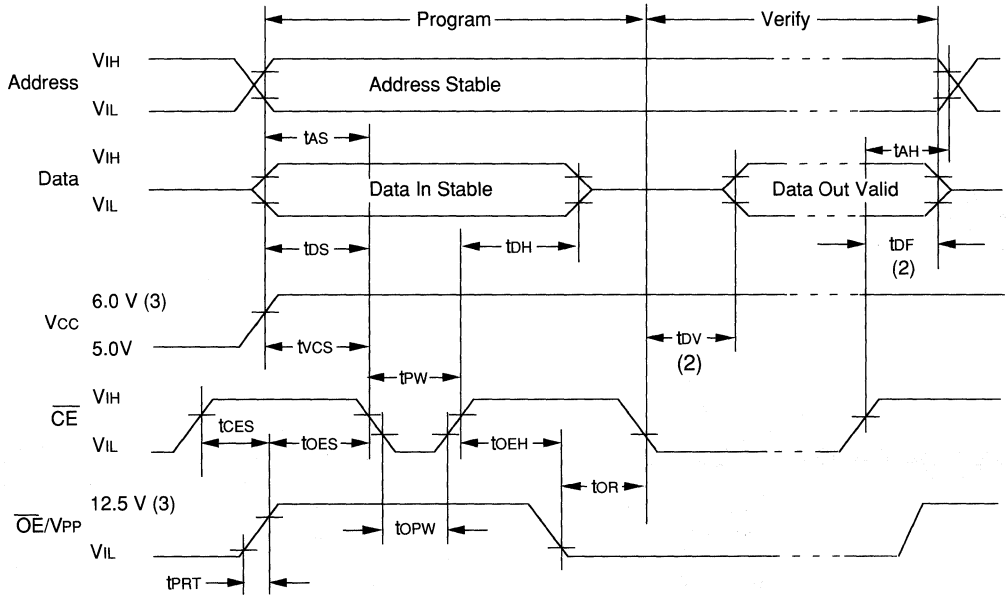
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Output Load: 1 TTL Load + 100pF
Ambient Temperature: 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
$\overline{OE}$ Hold Time	t_{OEH}	2		µs	
$\overline{OE}$ Recovery Time	t_{OR}	2		µs	
$\overline{OE}/V_{PP}$ Rise Time During Programming	t_{PRT}	50		ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ± 5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms (1)



Notes: (1) The input timing reference level is 0.8 V for VIL and 2.0 V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) VCC = 6.0 V ±0.25 V, VPP = VH = 12.5 V ±0.5 V for fast programming algorithm.

5

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$/VPP	A9	O0 - O7
Read	VIL	VIL	X	DOUT
Program	VIL	VH	X	DIN
Program Verify	VIL	VIL	X	DOUT
Program Inhibit	VIH	VH	X	High Z
Standby	VIH	X	X	High Z
Output Disable	VIL	VIH	X	High Z
Identity	VIL	VIL	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$/VPP pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay (tOE) from the falling edge of $\overline{OE}$/VPP.

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified.

When this condition is met, the supply current will drop from 35mA to 100μA.

Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in multiple bus microprcessor systems and the outputs go to high impedance when:

• the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"'s state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000μW/cm^2 for approximately 20 minutes.

Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

Identity Mode

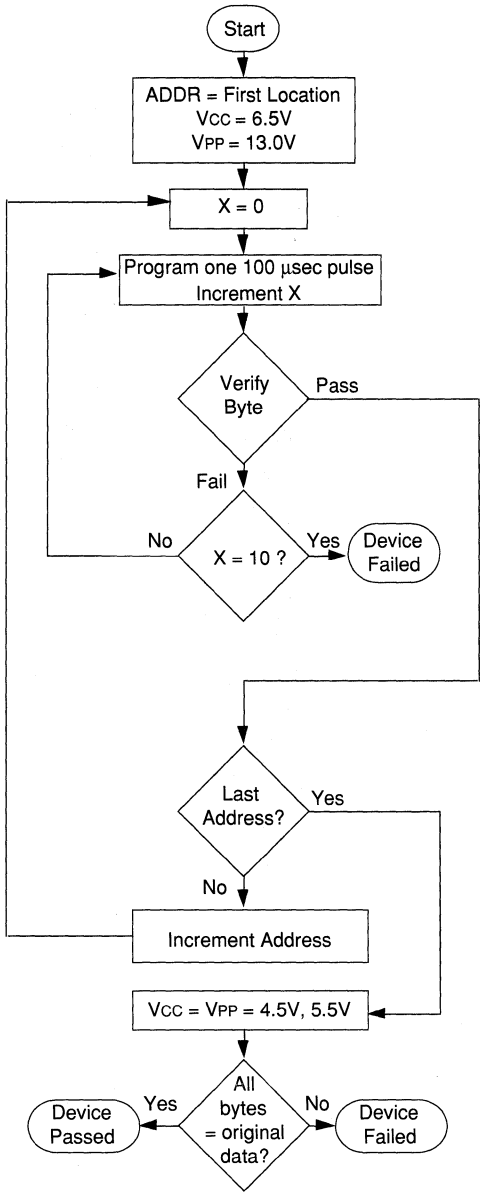
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	1	1	0	1	0D

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C512 - 25 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	TSOP
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
	E	-40° C to 125° C
Access Time:	90	90 nsec
	10	100 nsec
	12	120 nsec
	15	150 nsec
	20	200 nsec
Device:	27C512	512K (64K x 8) CMOS EPROM

27HC1616

256K (16K x 16) High Speed CMOS UV Erasable PROM

FEATURES

- 16 bit configuration
- High speed performance
  —55ns Maximum access time
- CMOS Technology for low power consumption
  —90mA Active current
  —50mA Standby current
- WordWide architecture offers space saving over Bytewide memories
- Organized 16K x 16: JEDEC standard pinouts
  —40-Pin ceramic dual in line package
  —44-Pin ceramic leadless chip carrier
- Extended temperature ranges available:
  —Commercial: 0°C to +70°C

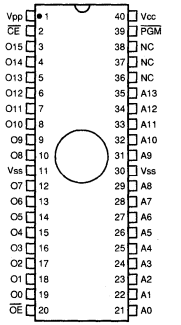
DESCRIPTION

The Microchip Technology Inc. 27HC1616 is a CMOS 16K x 16 (256K) Programmable Read Only Memory. The device operates at Bipolar PROM speeds but uses far less current than any Bipolar PROM. The 27HC1616 is an excellent choice for any application requiring blazing speeds and low power consumption. The word wide (16 bit) architecture can replace two 8 bit EPROMS in any 16 bit application saving valuable printed circuit space and components costs. Typical applications for the 27HC1616 include automotive systems control, high speed modems, digital signal processing, or any application that uses the 80386, 68030, 29000, etc. high performance microprocessors.

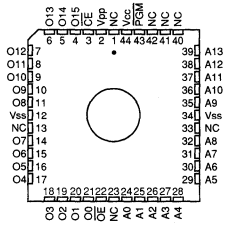
5

PIN CONFIGURATION

Top View

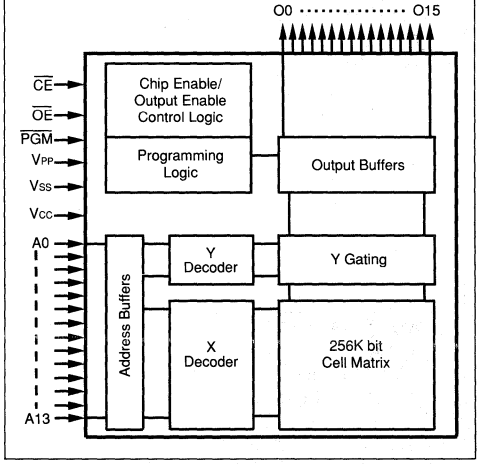


DIP



LCC

BLOCK DIAGRAM



PIN FUNCTION TABLE	
Name	**Function**
A0 - A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O15	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V
Temperature under bias ..... -65°C to 125° C
Storage temperature ..... -65°C to 150° C
ESD protection on all pins 2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN= -0.1 to VCC + 1.0V
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 2mA IOL = 8mA
Output Leakage	all		ILO	-10	10	µA	VOUT= -0.1 to VCC + 0.1V
Input Capacitance	all		CIN		6	pF	VIN= 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT= 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	all	TTL input	ICC		90	mA	VCC = 5.5V; VPP = VCC f = 2MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH= 2.0 to VCC; Note 1
Power Supply Current, Standby	S,X		ICC(S)		50	mA	
PP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: S = Standard Temp; X = Industrial Temp Range;
Notes: (1) AC Power component above 2MHz: 2mA/MHz.
(2) VCC must be applied simultaneously or before VPP and be removed simultaneously or after VPP.

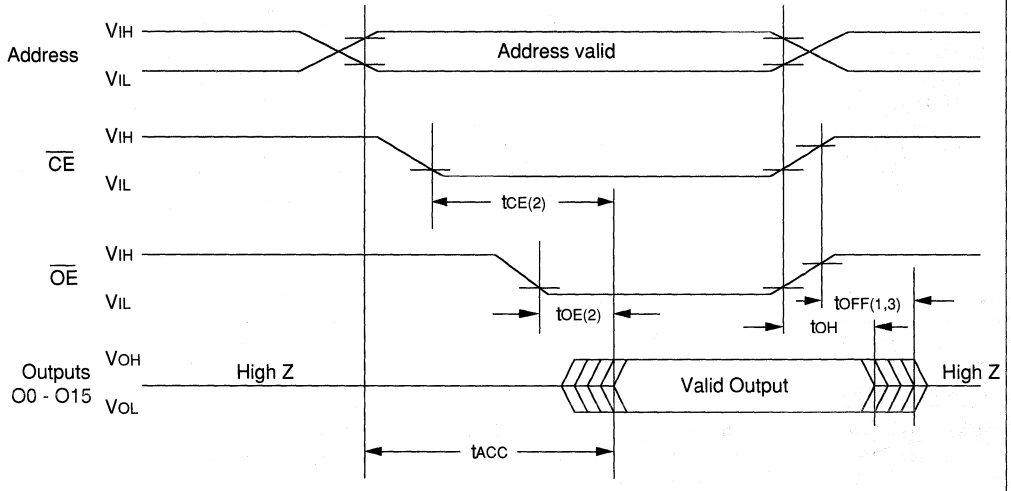
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0 V and V_{IL} = 0.0 V; V_{OH} = V_{OL} = 1.5 V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb= 0° C to 70° C

Parameter	Part*	Sym	27HC1616-55		27HC1616-70		Units	Conditions
			Min	Max	Min	Max		
Address to Output Delay	all	tACC		55		70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	all	tCE2		35		45	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	tOE		30		35	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	all	tOFF	0	20	0	25	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	all	tOH	0		0		ns	

* Parts: S = Standard Power; L = Low Power

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

5

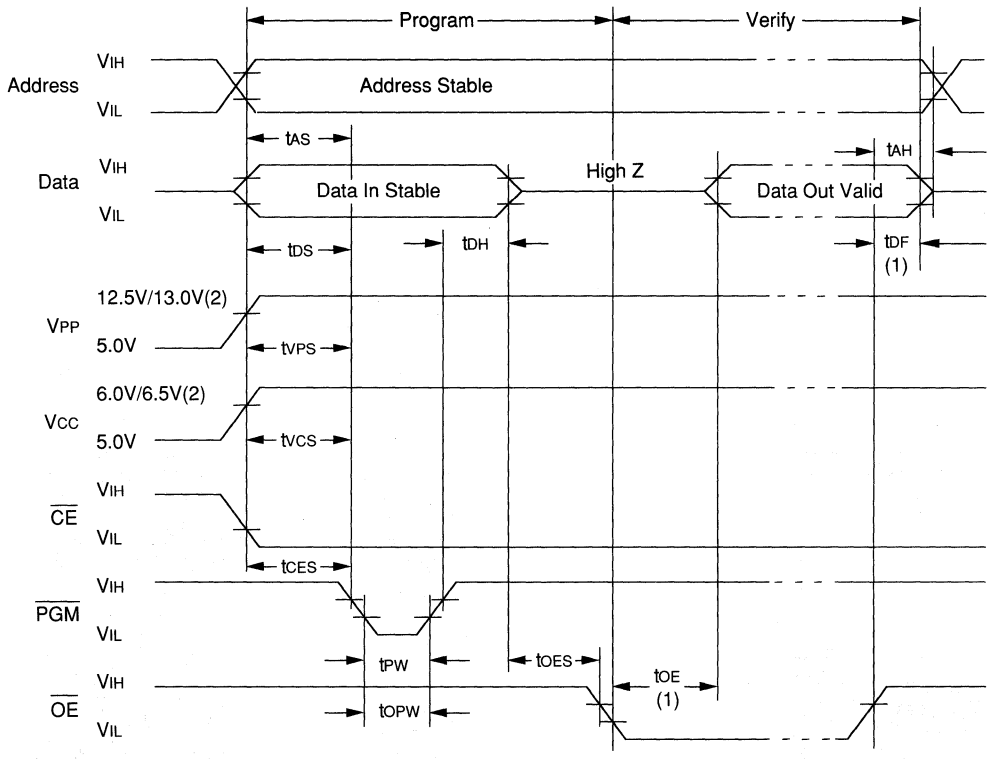
PROGRAMMING DC Characteristics	Ambient Temperature: 25° C ±5° C For V_{PP} and V_{CC} Voltages refer to Programming Algorithms					
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = -.1V to V_{CC} + 1.0V
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 2mA I_{OL} = 8mA
V_{CC} Current, program & verify		I_{CC}		90	mA	Note 1
V_{PP} Current,program		I_{PP}		50	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING AC Characteristics for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V and V_{OL} = 0.8V Ambient Temperature: 25° C ±5° C For V_{PP} and V_{CC} Voltages, refer to Programming Algorithms				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accomodated by the programmer
(2) V_{CC} = 6.0V ±0.25V, V_{PP} = V_H = 12.5V ±0.5V for fast programming algorithm
V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express algorithm

FUNCTIONAL DESCRIPTION

The 27HC1616 has the following functional modes:

—Operation: The 27HC1616 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC1616 must be programmed. Both a program and program/verify procedure is available. It can be programmed using the Fast or Express algorithm; however, the Express algorithm is recommended.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

For the general characteristics in these operation and programming modes, refer to the table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A9	O0 - O15
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	X	D_{out}
Program	V_{IL}	V_{IH}	V_{IL}	V_H	X	D_{in}
Program Verify	V_{IH}	V_{IL}	V_{IH}	V_H	X	D_{out}
Program Inhibit	V_{IH}	X	X	V_H	X	High Z
Standby	V_{IH}	X	X	V_{CC}	X	High Z
Output Disable	X	V_{IH}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_H	Identity Code

X = Don't Care
V_H = 12.0 ±0.5V

5

OPERATION

Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC1616's memory data is accessed when

—the chip is enabled by setting the $\overline{CE}$ pin low.
—the data is gated to the output pins by setting the $\overline{OE}$ pin low.

For Read operations on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). A faster $\overline{CE}$ access time (t_{CE}) is available on the standard part to provide the additional time for decoding the $\overline{CE}$ signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$.

Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not defined. When these conditions are met, the supply current will drop from 90mA to 50mA.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

Programming/Verification

The 27HC1616 has to be programmed, and afterward the programmed information verified. Before these operations, the Identity Code can be read to properly set up automated equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

Programming Algorithm

The "Express" algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100µsec each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure 2.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ pin is pulsed low.

Since the erase state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A13, and the data is presented to pins O0 - O15. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{OE}$ line is low
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ line is high.

Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{PGM}$ needs to be under separate control to each device. By pulsing the $\overline{PGM}$ line low on a particular device, that device will be programmed, and all other devices with corresponding $\overline{PGM}$ or $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin →	Input	Output*							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	1	1	97

*Code subject to change.
Note: O15 - O8 are 00 for the manufacturer and device type code.

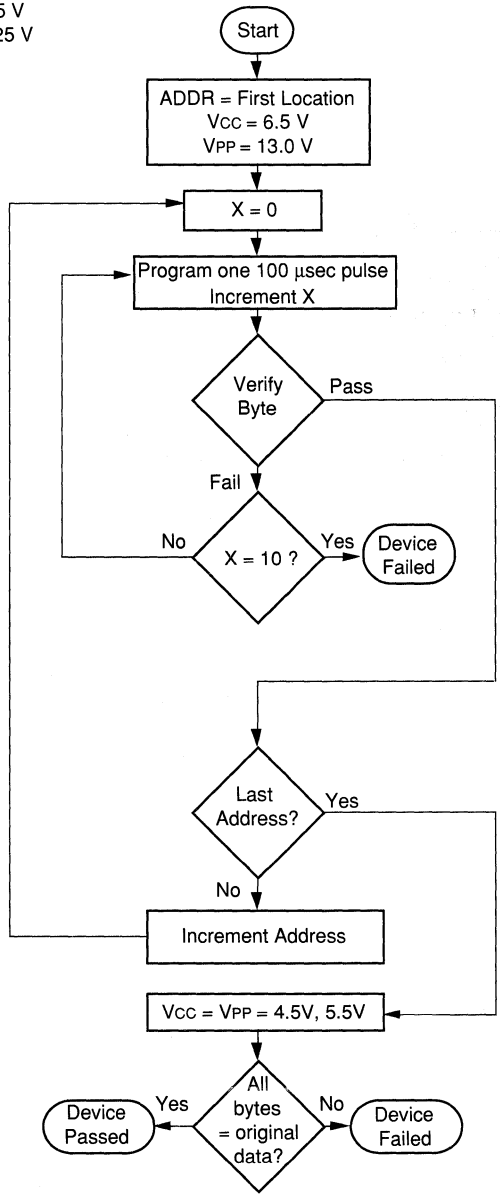
Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537Å with an intensity of 12,000µW/cm² at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25 V
V_{PP} = 13.0 ±0.25 V



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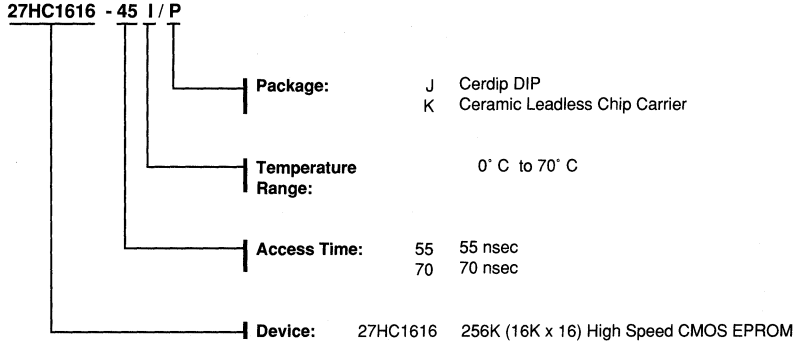
SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



Microchip

27HC256

256K (32K x 8) High Speed CMOS EPROM

FEATURES

- High speed performance
  —55ns access time available
- CMOS technology for low power consumption
  —55mA active current
  —100μA standby current (low power option)
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Organized in 32K x 8 - JEDEC Standard Pinouts
  —28-pin Dual-in-line and SOIC package
  —32-pin Chip carrier (leadless or plastic)
- Extended temperature ranges available:
  —Commercial: 0° C to +70° C
  —Industrial: -40° C to +85° C
  —Automotive: -40° C to +125° C

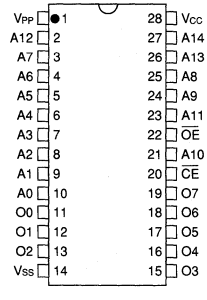
DESCRIPTION

The Microchip Technology Inc 27HC256 is a CMOS 256K bit (electrically) Programmable Read Only Memory. The device is organized into 32K words of 8 bit each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further reduction in the standby power requirement to 100μA. The 27HC256 is configured in a standard 256K EPROM pinout which allows an easy upgrade for present 27C256 users. A complete family of packages are offered to provide the utmost flexibility. The 27HC256 allows high performance microprocessors to run at full speed without the need of wait states. CMOS design and processing makes this part suitable for applications where reliability and reduced power consumption are essential.

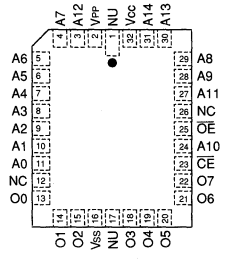
5

PIN CONFIGURATIONS

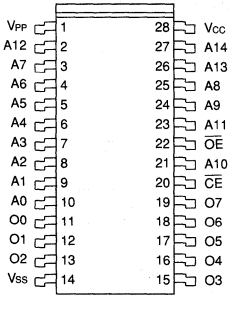
TOP VIEW



DIP



PLCC/LCC



SOIC

PIN FUNCTION TABLE	
Name	**Function**
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS
Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC +1.0V
Temperature under bias .....-65° C to 125° C
Storage temperature .....-65° C to 150° C
Maximum exposure to UV 7258Wsec/cm²
ESD protection on all pins 2.0kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%

Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C
Automotive: Tamb= -40° C to 125° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = -0.1V to VCC +1.0V
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -4mA IOL = 16mA
Output Leakage	all		ILO	-10	10	µA	VOUT = -0.1V to VCC +0.1V
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb = 25°C; f = 1MHz
Power Suppy Current, Active	S,L X	TTL input TTL input	ICC1 ICC2		55 65	mA mA	VCC = 5.5V; VPP = VCC f = 2MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S SX		ICC(S)1		35 40	mA mA	
Power Supply Current, Standby	L LX L, LX	TTL input TTL input CMOS input	ICC(S)2		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC -0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: S = Standard Power; L = Low Power; X = Industrial and Automotive Temp. Ranges;
Notes: (1) AC Power component above 2 MHz: 3mA/MHz for standard part; 5 mA/MHz for extended temperature range part.
(2) VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP.

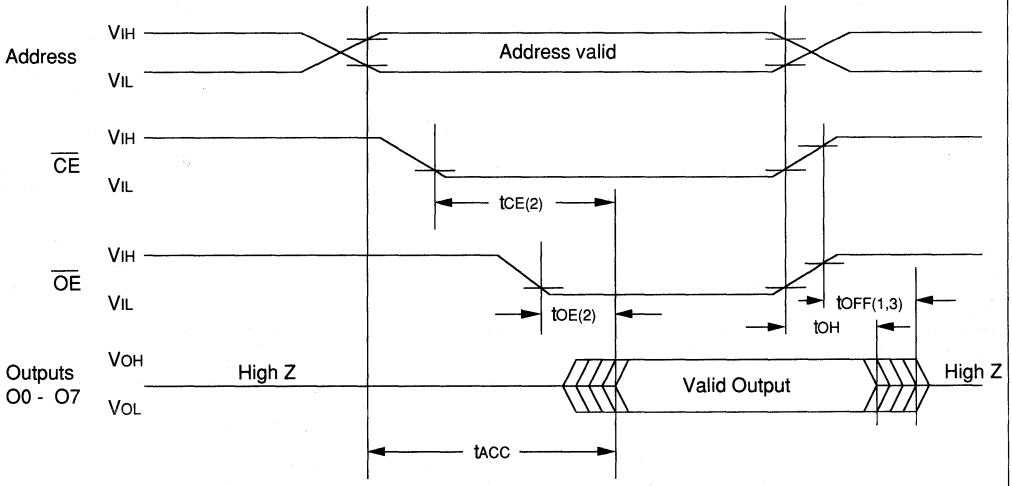
READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C
Automotive: Tamb = -40° C to 125° C

Parameter	Part*	Sym	27HC256-55**		27HC256-70		27HC256-90***		Units	Conditions
			Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	tACC		55		70		90	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	L S	tCE1 tCE2		55 45		70 45		90 50	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	tOE		30		35		40	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to O/P High Impedance	all	tOFF	0	25	0	30	0	35	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	tOH	0		0		0		ns	

* Parts: S = Standard Power; L = Low Power
** 27HC256-55 is only available in commercial temperature range
*** SOIC package only

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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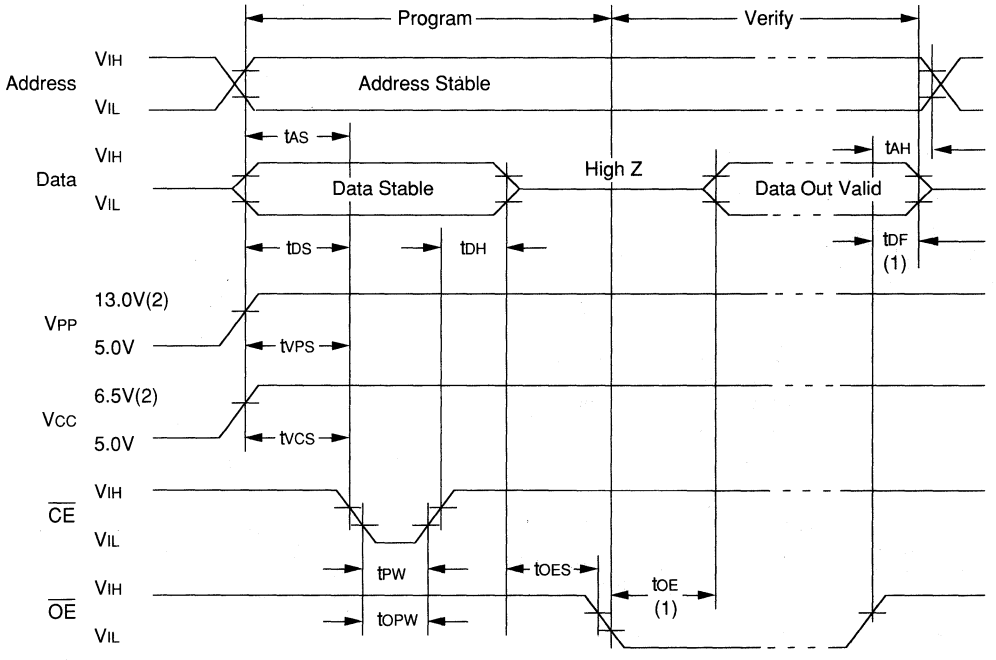
PROGRAMMING **DC Characteristics**		Ambient Temperature: Tamb = 25° C ±5° C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V				
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = OV to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -4mA I_{OL} = 16mA
V_{CC} Current, program & verify		I_{CC}		55	mA	
V_{PP} Current, program		I_{PP}		30	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

PROGRAMMING **AC Characteristics** for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Ambient Temperature: Tamb = 25° C ±5° C V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100 µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer
(2) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express algorithm

FUNCTIONAL DESCRIPTION

The 27HC256 has the following functional modes:

—Operation: The 27HC256 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.

—Programming: To receive its permanent data, the 27HC256 must be programmed. Both a program and program/verify procedure is available. It can be programmed with the "Express" algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

Operation Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	A9	O0 - O7
Read	V_{IL}	V_{IL}	V_{CC}	X	D_{OUT}
Program	V_{IL}	V_{IH}	V_H	X	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_H	X	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	V_{CC}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{CC}	V_H	Identity Code

X = Don't Care

Operation

- Read
- Standby
- Output Disable

For the general characteristics in these operation modes, refer to the table above.

Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC256's memory data is accessed when

— the chip is enabled by setting the $\overline{CE}$ pin low.
— the data is gated to the output pins by setting the $\overline{OE}$ pin low.

For Read operations on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). A faster $\overline{CE}$ access time (t_{CE}) is available on the standard part to provide the additional time for decoding the $\overline{CE}$ signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$.

Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and a program mode is not defined. When these conditions are met, the supply current will drop from 55mA to 100µA on the low power part, and to 35mA on the standard part.

Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

Programming Algorithms

The Express algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100µsec each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure1.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low

Since the erase state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A14, and the data is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low

Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{CE}$ needs to be under seperate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed, and all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type	V_{IH}	1	0	0	1	0	1	0	0	94

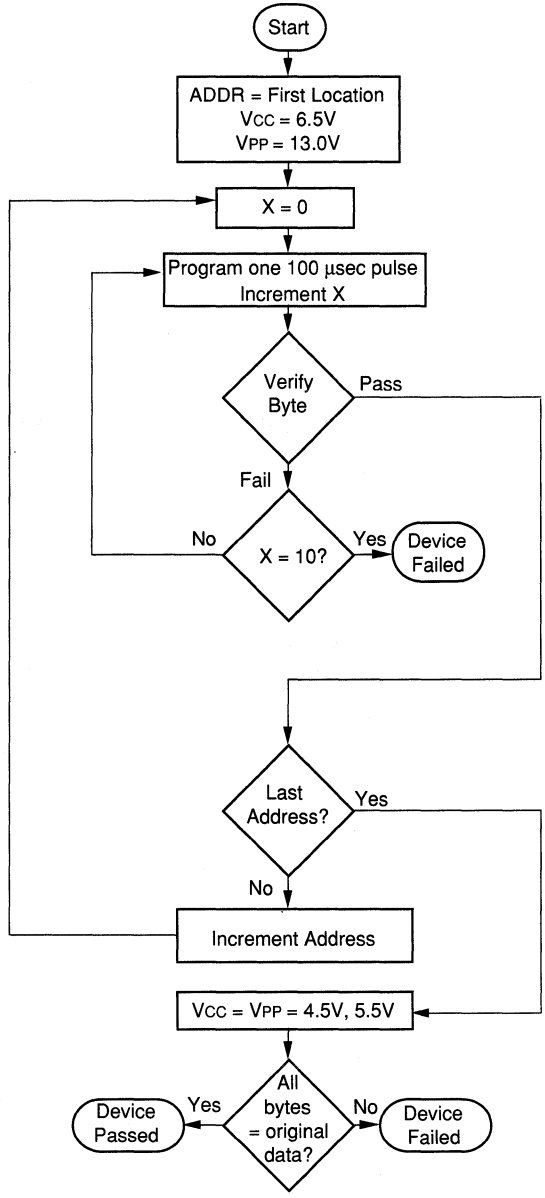
Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state when exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537 Å with an intensity of 12,000µW/cm² at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

PROGRAMMING - Figure 1
Express Algorithm

Conditions:
T_{amb} = 25+/-5C
V_{CC} = 6.5+/-0.25V
V_{PP} = 13.0+/-0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing, or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27HC256 L - 55 I / SO

Package:		J	Cerdip DIP
		K	Ceramic Leadless Chip Carrier
		L	PLCC
		P	Plastic DIP
		SO	Plastic SOIC
Temperature Range:		-	0° C to +70° C
		I	-40° C to +85° C
		E	-40° C to + 125° C
Access Time:		55	55 nsec
		70	70 nsec
		90	90 nsec (SOIC only) AWD/WTD
Power Type:		-	Standard Power
		L	Low Power
Device:	27HC256		256K (32K x 8) High Speed EPROM

27LV256

256K (32K x 8) Low Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  —200ns maximum access time at 3.0V
- CMOS Technology for low power consumption
  —8mA Active current at 3.0V
  —20mA Active current at 5.5V
  —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin PLCC package
  —28-pin SOIC package
  —28-pin TSOP package
  —Tape and reel
- Available for extended temperature ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C

DESCRIPTION

The Microchip Technology Inc. 27LV256 is a low voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 32K x 8 (32K-Byte) non-volatile memory product. The 27LV256 consumes only 8mA maximum of active current during a 3.0 volt read operation, thereby improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMS can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200ns at 3.0 volts. This device allows systems designers the ability to use low voltage non-volatile memory with todays low voltage microprocessors and peripherals in battery powered applications.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

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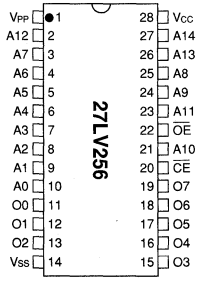
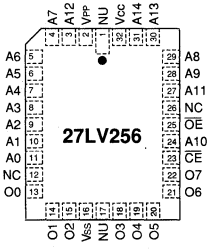
PIN CONFIGURATIONS

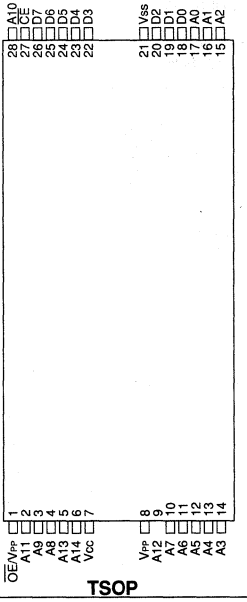
Top View



DIP/SOIC



PLCC/LCC



TSOP

PIN FUNCTION TABLE	
Name	**Function**
A0 - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V or +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC + 1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10% or 3.0V where indicated
Commercial: Tamb= 0° C to 70° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		20 8 @ 3.0V 25 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)		1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

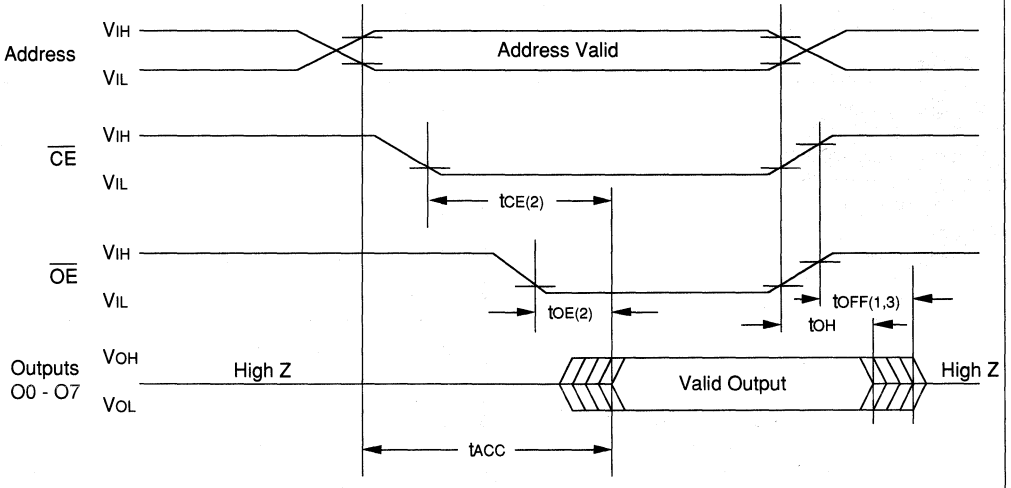
S = Standard Power; X = Extended Temp. Range;
(1) AC Power component above 1MHz: 5mA up to maximum frequency.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C

Parameter	Sym	27LV256-20		27LV256-25		27LV256-30		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		200		250		300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		200		250		300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		100		125		125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0		0		0		ns	

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		20	mA	Note 1
V_{PP} Current, program		I_{PP2}		25	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

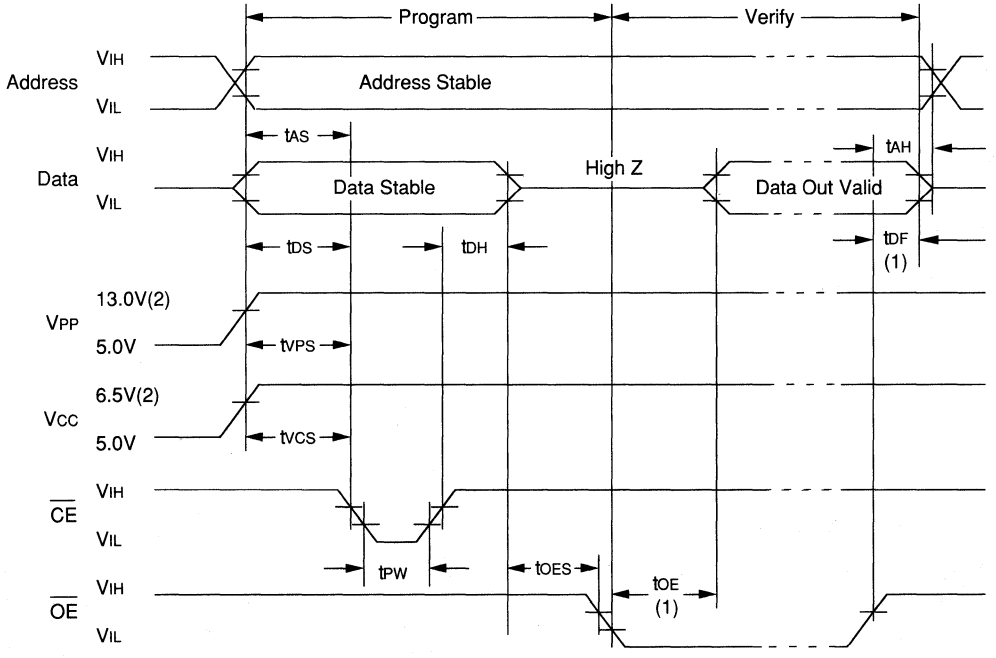
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Ambient Temperature: Tamb = 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, V_{PP} = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For express algorithm, initial programming width tolerance is 100µsec ±5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5 V ±0.25 V, VPP = VH = 13.0 V ±0.25 V for express algorithm

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MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high.

Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) The $\overline{OE}$ pin is high and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) The $\overline{CE}$ pin is high and
d) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

Identity Mode

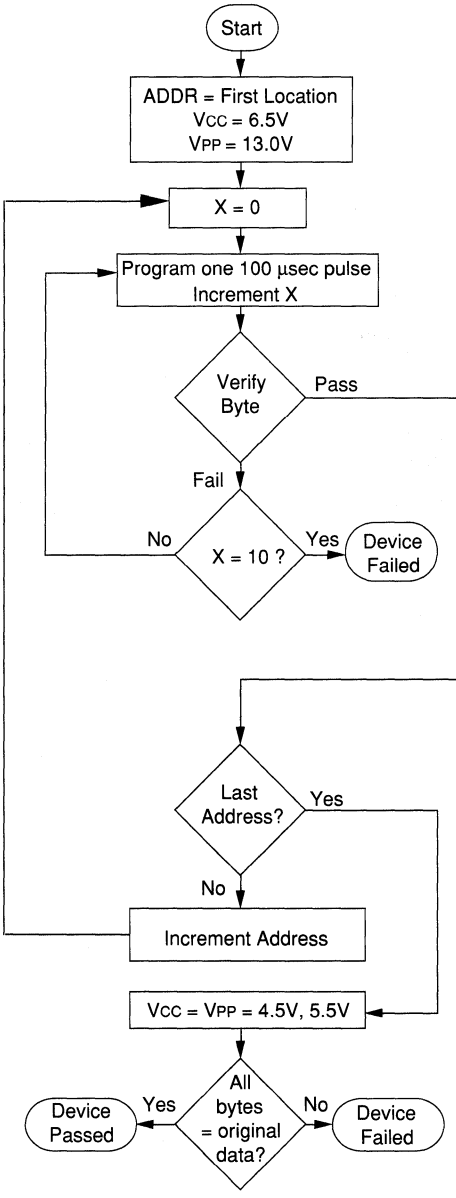
In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27LV256 - 25 I / P

Package:	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	J	Ceramic DIP
	K	Ceramic Leadless Chip Carrier
	TS	Plastic Thin Small Outline (TSOP)
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
Access Time:	20	200 nsec
	25	250 nsec
	30	300 nsec
Device:	27LV256	256K (32K x 8) Low Voltage CMOS EPROM

Microchip

27LV512

512K (64K x 8) Low Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  —200ns maximum access time at 3.0V
- CMOS Technology for low power consumption
  —12mA Active current at 3.0V
  —35mA Active current at 5.5V
  —100μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin PLCC package
  —28-pin SOIC package
  —28-pin TSOP package
  —Tape and reel
- Available for extended temperature ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C

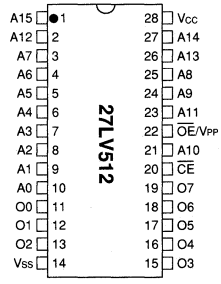
DESCRIPTION

The Microchip Technology Inc. 27LV512 is a low voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 64K x 8 (64K-Byte) non-volatile memory product. The 27LV512 consumes only 12mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMS can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200ns at 3.0 volts. This device allows systems designers the ability to use low voltage non-volatile memory with todays low voltage microprocessors and peripherals in battery powered applications.

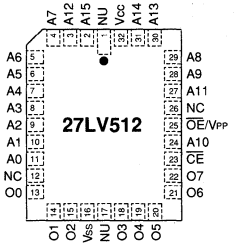
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

5

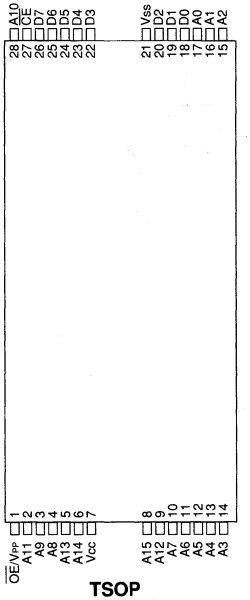
PIN CONFIGURATIONS
Top View



DIP/SOIC



PLCC/LCC



TSOP

PIN FUNCTION TABLE	
Name	**Function**
A0 - A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/ Programming Voltage
O0 - O7	Data Output
VCC	+3.0V To +5.5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC + 1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10% or 3.0V where indicated
Commercial: Tamb= 0° C to 70° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		35 12 @ 3.0V 45 12 @ 3.0V	mA mA mA mA	VCC = 5.5V f = 1MHz; $\overline{OE}$/VPP= $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC;
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

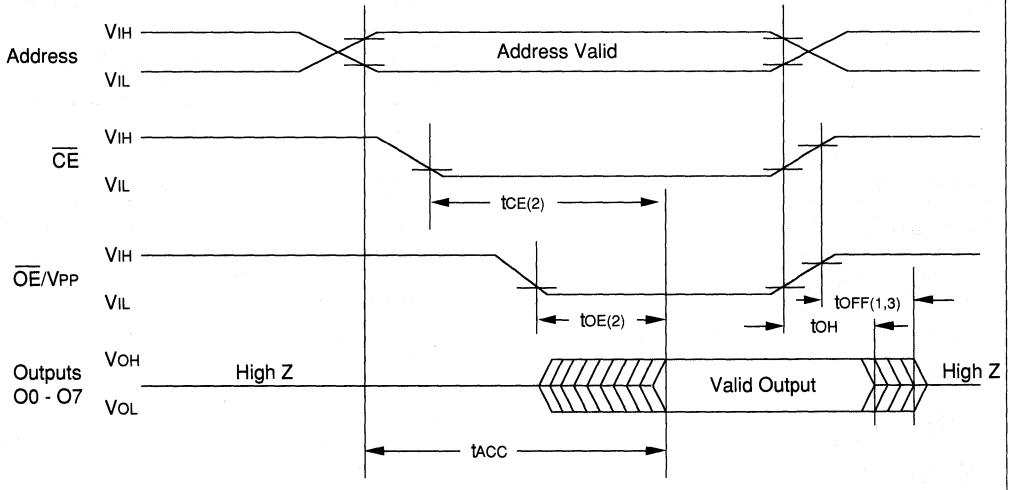
* Parts: S = Standard Power; X = Extended Temp. Range;
Notes: (1) AC Power component above 1MHz: 2mA/MHz.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C

Parameter	Sym	27LV512-20		27LV512-25		27LV512-30		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		200		250		300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		200		250		300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		90		100		125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0		0		0		ns	

READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$/VPP or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

5

PROGRAMMING
DC Characteristics

Ambient Temperature: 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Current (all inputs)		I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400µA I_{OL} = 2.1mA
V_{CC} Current, program & verify		I_{CC2}		35	mA	
$\overline{OE}/V_{PP}$ Current,program		I_{PP2}		25	mA	$\overline{CE}$ = V_{IL}
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before the V_{PP} voltage on $\overline{OE}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{OE}/V_{PP}$.

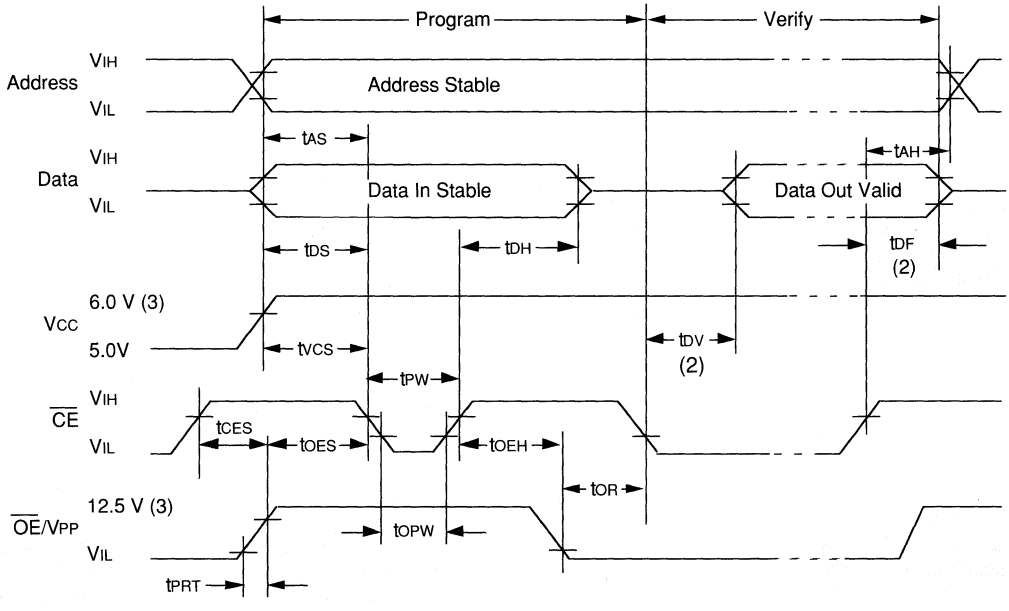
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V
Ambient Temperature: 25° C ±5° C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
$\overline{OE}$ Hold Time	t_{OEH}	2		µs	
$\overline{OE}$ Recovery Time	t_{OR}	2		µs	
$\overline{OE}/V_{PP}$ Rise Time During Programming	t_{PRT}	50		ns	

Notes: (1) For Express algorithm, initial programming width tolerance is 100µsec ± 5%.
(2) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms (1)



Notes: (1) The input timing reference level is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.0 V ±0.25 V, V_{PP} = V_H = 12.5 V ±0.5 V for fast programming algorithm.

5

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A9	O0 - O7
Read	V_{IL}	V_{IL}	X	D_{OUT}
Program	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	X	High Z
Output Disable	V_{IL}	V_{IH}	X	High Z
Identity	V_{IL}	V_{IL}	V_H	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}/V_{PP}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}/V_{PP}$.

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified.

Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus contention in microprocessor based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when:

• the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

Identity Mode

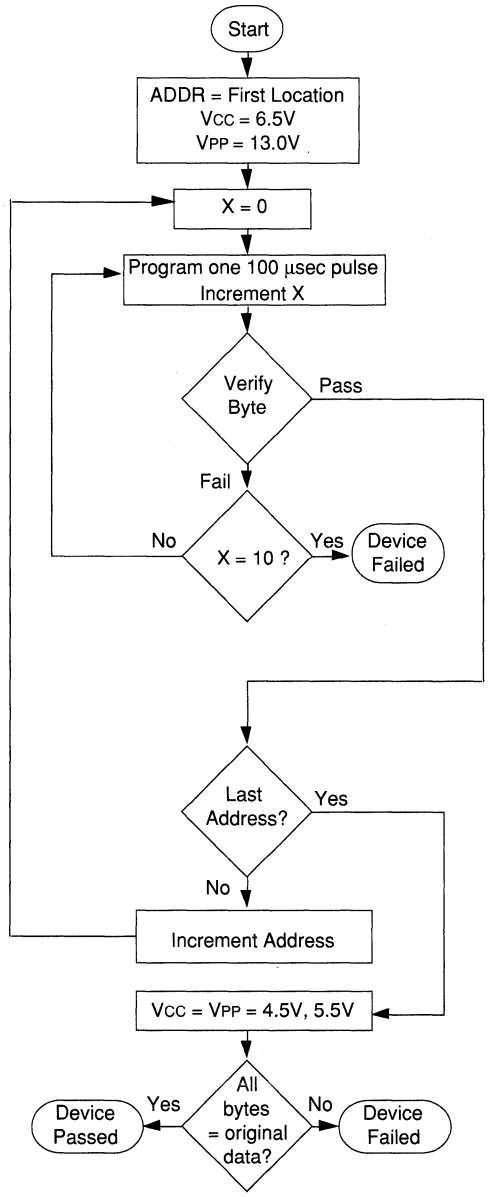
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	1	1	0	1	0D

* Code subject to change.

PROGRAMMING - FIGURE 1
EXPRESS ALGORITHM

Conditions:
T_{amb} = 25° C ±5° C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27LV512 - 25 I / P

Package:	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	J	Ceramic DIP
	K	Ceramic Leadless Chip Carrier
	TS	Plastic Thin Small Outline (TSOP)
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
Access Time:	20	200 nsec
	25	250 nsec
	30	300 nsec
Device:	27LV512	512K (64K x 8) Low Voltage CMOS EPROM

27CXXX EPROM FAMILY PROGRAMMING ALGORITHM

Overview

Microchip Technology Inc. supports three programming algorithms for its CMOS EPROM Family. The selection of an algorithm is an important consideration and will impact the programming time, programming yield and programming margins of the EPROM. **The Express algorithm is the preferred algorithm for all Microchip OTP and windowed EPROMs.**

Fast Programming Algorithm

This is the old industry standard programming algorithm with up to 25 1-msec programming pulses and a three times overprogramming pulse. It is a very stable algorithm to use, with its major draw back being an increase in throughput time especially at the larger densities. The Fast Programming algorithm is no longer recommended for todays programmable memory devices.

Rapid Pulse Programming Algorithm

The Rapid Pulse algorithm provides an alternative to the Fast algorithm. The slight increase in VCC and VPP during programming allows the use of a narrower 100 usec programming pulse and the removal of the overprogramming pulse associated with the Fast Programming. This translates into a decrease in programming times of nearly 40 to 1 and an increase in throughput of nearly 10 to 1. (Throughput is heavily influenced by the machine cycle time of the programmer during the pre-programming blank check, and the post-programming verification. It also varies from programmer to programmer.)

Express Programming Algorithm

The Express algorithm is an improvement on the Rapid Pulse algorithm. While it exhibits the same excellent throughput as the Rapid Pulse algorithm, its advantage lies in the additional increase in VPP and VCC applied during programming. The higher VPP and VCC voltages provide additional charge to the floating gate during programming. After each programming pulse, the cell is verified against a VCC of 6.5 V. This verification step with a higher VCC level ensures an improvement in programming margins.

Algorithm Selection

The optimization of programmer throughput is a concern to all EPROM users in a production environment. A major contributor to increasing throughput is shorter programming times. The Express algorithm has been developed to minimize programming times. In addition, sufficient programming margins must be developed to insure EPROM functionality over the full range of voltage and temperature variations. The higher Vcc and Vpp voltages generate this increased margin and provide additional guardband against the effects of aging hardware.

Programming Times (sec)			
Memory Size	**Fast**	**Rapid**	**Express**
64K	32.8	0.819	0.819
128K	65.6	1.64	1.64
256K	131.2	3.28	3.28
512K	262.4	6.55	6.55

Note: Actual throughput time depends on the machine cycle time of the programmer during pre-programming blank check, and the post-programming verification.

Microchip Programming Algorithm Recommendations

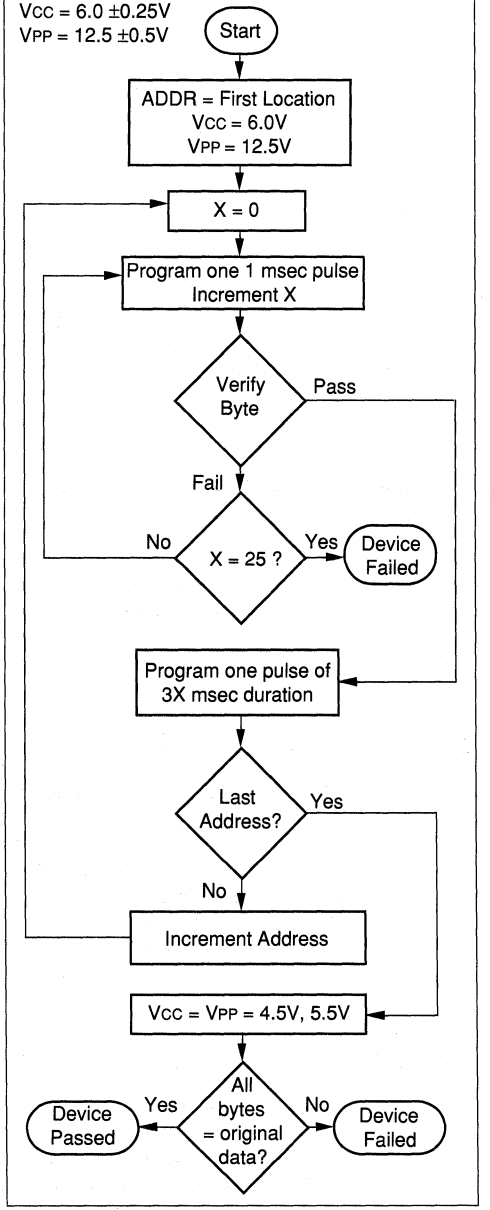
Microchip recommends that the Express algorithm be used on all commercial/industrial EPROMs (when available).

The Fast Programming algorithm should be your second choice for the 64K and the 128K EPROMs, with Rapid Pulse being the second choice for the 256K and 512K EPROMs. The remaining algorithm should be your third choice. This recommendation is based on the maximization of programmer throughput and cell margins. At the smaller density (when Express is not available) the increased margins supplied by the Fast Programming far outweigh the small increase in throughput of Rapid Pulse. As you increase density, programming throughput becomes the dominant criteria.

Data I/O Family Code and Pin-Outs*				
Device	**Size**	**Fast**	**Rapid**	**Express**
27C64	64K	93/33	5C/33	115/033
27C128	128K	93/51	5C/51	115/051
27C256	256K	93/32	5C/32	115/032
27HC256	256K	93/32	5C/32	115/032
27HC1616	256K	-	-	191/1A2
27C512	512K	4B/A4	5E/A4	116/0A4
27LV256	256K	93/32	5C/32	115/032
27LV512	512K	4B/A4	5E/A4	116/0A4

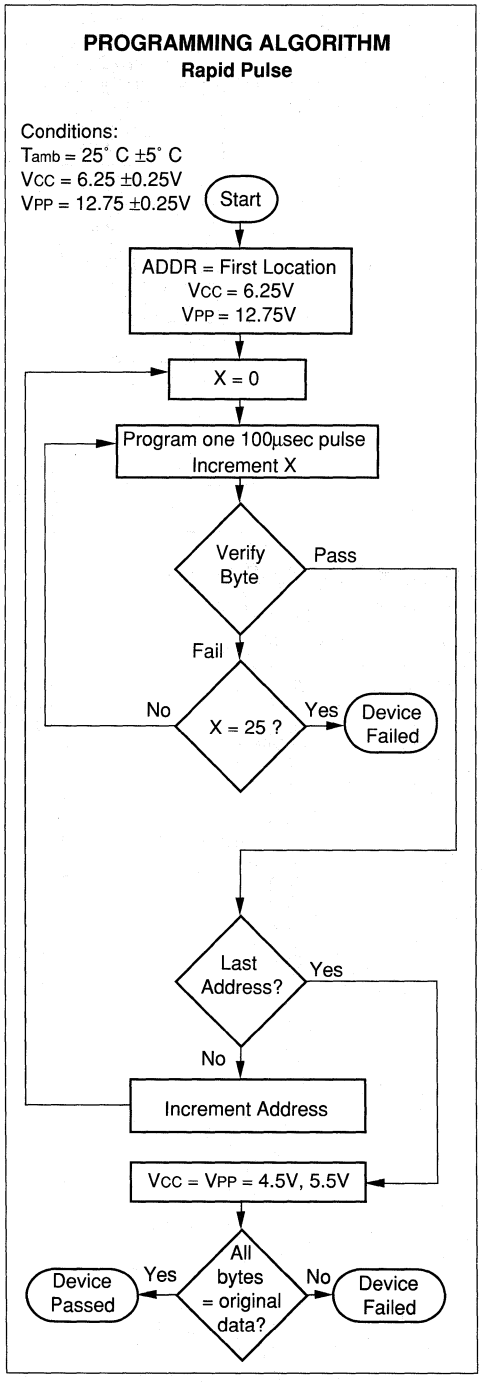
* DIP Packages

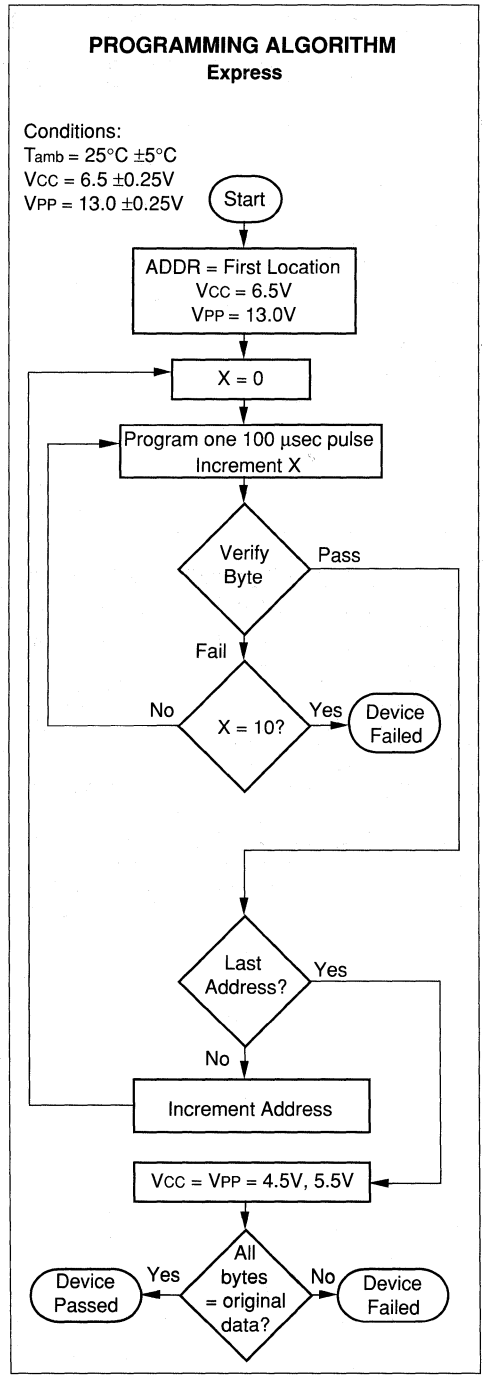
PROGRAMMING ALGORITHM
Fast Algorithm



LOGICAL DEVICES PROGRAMMERS				
	Gang-Pro "S", Model II	**Gang-Pro 8+**	**All Pro 40/88**	**All-Pro 88 x R**
27C64	V 1.0	V 1.1	V 2.1 Ex	V 1.0 Ex
27C128	V 1.0	V 1.1	V 2.1 Ex	V 1.0 Ex
27C256	V 1.0	V 1.1	V 2.1 Ex	V 1.0 Ex
27C512	V 1.0	V 1.1	V 2.1 Ex	V 1.0 Ex
27HC256	V 1.0 Express	V 1.1	V 1.48 Fast	V 1.0 Fast
27HC1616	By Request	By Request		
27LV256	By Request	By Request		
27LV512	By Request	By Request		

STAG PROGRAMMERS												
	Device Code	**39M101**	**40M100**	**40M101**	**41M100**	**41M101**	**42M100**	**42M101**	**ZM2000**	**ZM2500**	**ZM3000**	**1040/84**
27C64	02DA	V9.0	V5.0	V6.0	V9.0	V6.0	V3.0	V6.0	v36	v9.0	v12.1	28 stEPROM
27C128	02DB	9.0	5.0	6.0	9.0	6.0	3.0	6.0	20-38	9.0	12/1	28 stEPROM
27C256	02DC	9.0	3.02	6.0	9.0	6.0	1.02	6.0	20-38	9.0	12.1	28 stEPROM
27C512	02DD	9.0	4.0	6.0	9.0	6.0	2.0	6.0	20-30	9.0	12.1	28 stEPROM
27HC256	02DC	9.0	3.02	6.0	9.0	6.0	1.02	6.0	20-38	9.0	12.1	28 stEPROM
27HC1616	—	—	—	—	—	—	—	—	—	—	—	40 stEPROM
27LV256	02DC	9.0	3.02	6.0	9.0	6.0	1.02	6.0	20-38	9.0	12.1	28 stEPROM
27LV512	02DD	9.0	4.0	6.0	9.0	6.0	2.0	6.0	20-30	9.0	12.1	28 stEPROM





SECTION 6
LOGIC PRODUCTS

Microchip

AY0438

32-Segment CMOS LCD Driver

FEATURES

- Drives up to 32 LCD segments of arbitrary configuration
- CMOS process for: wide supply voltage range, low power operation, high noise immunity, wide temperature range
- CMOS, NMOS and TTL-compatible inputs
- Electrostatic discharge protection on all pins
- Cascadable
- On-chip oscillator
- Requires only three control lines
- Can be used to drive relays, solenoids, print head drives, etc.

APPLICATIONS

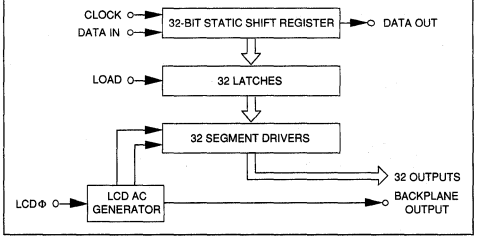
- Industrial displays
- Consumer product displays
- Telecom product displays
- Automotive dashboard displays

DESCRIPTION

The AY0438 is a CMOS LSI circuit that drives a liquid crystal display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.

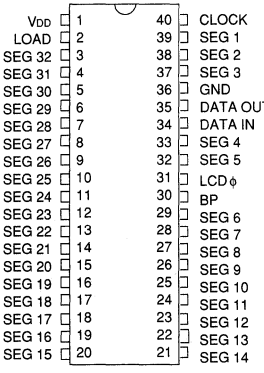
The AY0438 can drive any standard or custom parallel drive LCD display, whether it be field effect or dynamic scattering; 7-, 9-, 14-, or 16-segment characters; decimals; leading + or -; or special symbols. Several AY0438 devices can be cascaded. The AC frequency of the LCD waveforms can either be supplied by the user or generated by attaching a capacitor to the LCD input, which controls the frequency of an internal oscillator.

BLOCK DIAGRAM

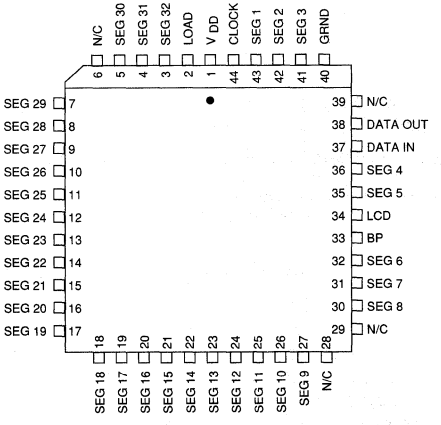


PIN CONFIGURATION
40 LEAD DUAL INLINE

Top View



44 PLCC



The device also acts as a versatile peripheral, able to drive displays, motors, relays, and solenoids within its output limitations.

The AY0438 is available in 40 lead dual-in-line ceramic and plastic packages. Unpackaged dice are also available.

6

PIN DESCRIPTION

Pin #	Name	Direction	Description
1	VDD	-	Supply voltage
2	Load	Input	Latch data from registers
3-29, 32, 33, 37-39	Seg 1-32	Output	Direct drive outputs
30	BP	Output	Backplane drive output
31	LCDΦ	Input	Backplane drive input
34	Data In	Input	Data input to shift register
35	Data Out	Output	Data output from shift register
36	Vss	Ground	Ground
40	Clock	Input	System clock input

FIGURE 1 TIMING DIAGRAM

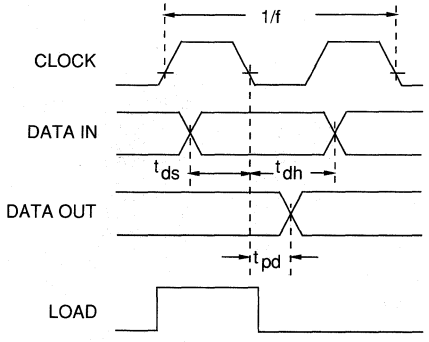
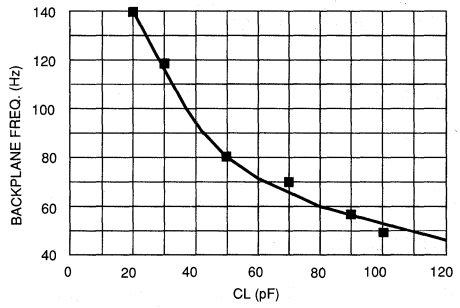


FIGURE 2 OSCILLATOR FREQUENCY GRAPH (TYPICAL @ 25°C)



OPERATING NOTES

1. The shift register loads, shifts, and outputs on the falling edge of the clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A logic 1 on Load causes a parallel load of the data in the shift register into latches that control the segment drivers.
4. If LCDΦ is driven, it is in phase with the backplane output.
5. To cascade units, either connect backplane of one circuit to LCDΦ of all other circuits (thus one capacitor provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. If the former is chosen, tie just one backplane to the LCD and use a different backplane output to drive the LCDΦ inputs. The data can be loaded to all circuits in parallel or else Data Out can be connected to Data In to form a long serial shift register.

6 The supply voltage of the AY0438 is equal to half the peak driving voltage of the LCD.

7. The LCDΦ pin can be used in two modes, driven or oscillating. If LCDΦ is driven, the circuit will sense this condition and pass the LCDΦ input to the backplane output. If the LCDΦ pin is allowed to oscillate, its frequency is inversely proportional to capacitance and the LCD drivingwaveforms have a frequency 2^8 slower than the oscillator itself. The relationship is shown graphically (see Figure 2). The frequency is nearly independent of supply voltage. If LCDΦ is oscillating, it is important to keep coupling capacitance to backplane and segments as low as possible. Similarly, it is recommended that the load capacitance on LCDΦ be as large as is practical.
8. There are two obvious signal races to be avoided in this circuit, (1) changing Data In when the clock is falling, and (2) changing Load when the clock is falling.
9. The number of a segment corresponds to how many pulses have occurred since its data was present at the input. For example, the data on SEG 17 was input 17 clock pulses earlier.
10. It is acceptable to tie the load line high. In this case the latches are transparent. Also, remote control would only require two signal lines, clock and Data In.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} ..... -0.3V to +12V
Inputs (CLK, Data In, Load) ..... V_{CC} to V_{DD} +0.3V
LCDΦ Input ..... -0.3V to V_{DD} +0.3V
Power Dissipation 250mW
Storage Temperature ..... -65°C to +125°C
Operating Temperature Industrial ..... -40°C to +85°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

V_{DD} = +5V unless otherwise noted
T_A = -40°C to +85°C

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	+3.0	-	+8.5	V	
Supply Current	I_{DD}	-	25	60	µA	LCDΦ OSC < 15 kHz
		-	13	30	µA	LCDΦ OSC < 100Hz
Input High Level	V_{IH}	0.5V_{DD}	-	V_{DD}	V	
Input Low Level Clock,	V_{IL1}	0	-	0.1 V_{DD}	V	3.0V ≤ V_{DD} ≤ 8.5V
Data,	V_{IL2}	0	-	0.1 V_{DD}	V	3.0V ≤ V_{DD} ≤ 8.5V
Input Leakage Current Load	I_L	-	0.01	±10	µA	V_{IN} = 0V and +5.0V
Input Capacitance	C_I	-	-	5.0	pF	V_{DD} = +5.0V
Segment Output Voltage	V_{OH}	0.8V_{DD}	-	V_{DD}	V	I_{OH} = -100µA
	V_{OL}	0	-	0.1V_{DD}	V	I_{OL} = 100µA
LCDΦ Input High Level	V_{IN}	0.9V_{DD}	-	V_{DD}	V	
LCDΦ Input Low Level	V_{IL}	0	-	0.1V_{DD}	V	
LCDΦ Input Leakage Current Level	I_L	-	-	10	µA	V_{IN} = 0V and +5.0V V_{DD} = +5.0V

AC CHARACTERISTICS

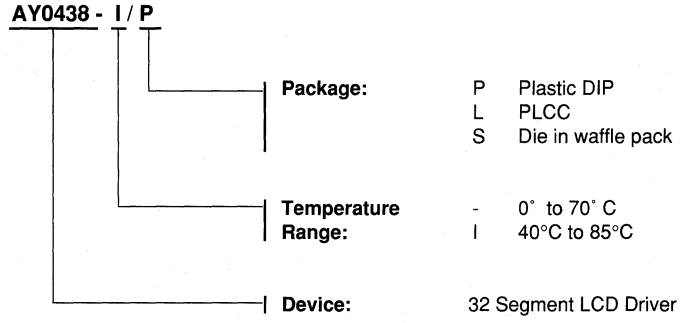
Characteristics	Sym	Min	Typ	Max	Units	Conditions
Clock Rate	f	DC	-	1.5	MHz	50% duty cycle
Data Set-up Time	t_{ds}	150	-	-	nsec	Data change to Clk falling edge
Data Hold Time	t_{dh}	50	-	-	nsec	
Load Pulse Width	t_{pw}	175	-	-	nsec	
Data Out Prop. Delay	t_{pd}	-	-	500	nsec	C_L = 55pF

6

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



DSP Product Portfolio

COMMERCIAL DSP (0° TO 70°)

CMOS DSP - COMMERCIAL (0° TO 70°)				
Microchip Part Number	**Speed (MHz) / TI Part Number**	**Maximum Instruction Cycle Time (ns)**	**Internal Mask ROM Version Available**	**Package**
DSP320C10-32/P	15.0 to 32.8	122	X	40L Plastic DIP
DSP320C10-32/L	15.0 to 32.8	122	X	44L PLCC
DSP320C10-25/P	15.0 to 25.6/ TMS320C10NL-25	156	X	40L Plastic DIP
DSP320C10-25/L	15.0 to 25.6/ TMS320C10FNL-25	156	X	44L PLCC
DSP320C10/P	6.7 to 20.5/ TMS320C10NL	195	X	40L Plastic DIP
DSP320C10/L	6.7 to 20.5/ TMS320C10FNL	195	X	44L PLCC
DSP320C10-14/P	6.7 to 14.4/ TMS320C10NL-14	277	X	40L Plastic DIP
DSP320C10-14/L	6.7 to 14.4	277	X	44L PLCC

INDUSTRIAL DSP (-45° TO +85°C)

CMOS DSP - INDUSTRIAL (-45° TO +85°C)				
Microchip Part Number	**Speed (MHz) / TI Part Number**	**Maximum Instruction Cycle Time (ns)**	**Internal Mas ROM Version Available**	**Package**
DSP320C10-32I/P	15.0 to 32.8	122	X	40L Plastic DIP
DSP320C10-32I/L	15.0 to 32.8	122	X	44L PLCC
DSP320C10-25I/P	15.0 to 25.6/ TMS320C10NA-25	156	X	40L Plastic DIP
DSP320C10-25I/L	15.0 to 25.6/ TMS320C10FNA-25	156	X	44L PLCC
DSP320C10I/P	6.7 to 20.5/ TMS320C10NA	195	X	40L Plastic DIP
DSP320C10I/L	6.7 to 20.5/ TMS320C10FNA	195	X	44L PLCC

MILITARY DSP (-55° TO +110°C)

Please refer to the "MILITARY DATA BOOK"

CMOS DSP - MILITARY (-55° TO +125°C)

Microchip	DESC SMD Part Number	Speed (MHz) Part Number Number	Maximum TI Part Cycle Time (ns)	Package Instruction	Lead Finish	Internal Masked ROM Version
DSP320C10-B/QA	5962-8763301QA	6.7 to 20.5 SMJ320C10JDM	195	40L Ceramic Side-Braze	Solder	-
DSP320C10-B/QC	5692-8763301QC	6.7 to 20.5	195	40L Ceramic Side-Braze	Gold	-
DSP320C10-B/UA	5962-8763301XA	6.7 to 20.5 SMJ320C10FDM	195	44 Terminal LCC	Solder	-
DSP320C10-B/UC	5692-8763301XC	6.7 to 20.5	195	44 Terminal LCC	Gold	-
DSP320C10-25B/QA	5962-8763302QA	15.0 to 25.6	156	40L Ceramic Side-Braze	Solder	-
DSP320C10-25B/QC	5962-8763302QC	15.0 to 25.6	156	40L Ceramic Side-Braze	Gold	-
DSP320C10-25B/UA	5692-8763302XA	15.0 to 25.6	156	44 Terminal LCC	Solder	-
DSP320C10-25B/UC	5962-8763302XC	15.0 to 25.6	156	44 Terminal LCC	Gold	-
DSP320CF10-25B/QA	5962-8763305QA	6.7 to 25.6	156	40L Ceramic Side-Braze	Solder	-
DSP320CF10-25B/QC	5962-8763305QC	6.7 to 25.6	156	40L Ceramic Side-Braze	Gold	-
DSP320CF10-25B/UA	5962-8763305XA	6.7 to 25.6	156	44 Terminal LCC	Solder	-
DSP320CF10-25B/UC	5962-8763305XC	6.7 to 25.6	156	44 Terminal LCC	Gold	-
DSP320CM10-B/QA	5962-8763303QA X	6.7 to 20.5	195	40L Ceramic Side-Braze	Solder	-
DSP320CM10-B/QC	5962-8763303QC	6.7 to 20.5	195	40L Ceramic Side-Braze	Gold	X
DSP320CM10-B/UA	5962-8763303XA X	6.7 to 20.5	195	44 Terminal LCC	Solder	-
DSP320CM10-B/UC	5962-8763303XC	6.7 to 20.5	195	44 Terminal LCC	Gold	X
DSP320CM10-25B/QA	5962-8763304QA X	15.0 to 25.6	156	40L Ceramic Side-Braze	Solder	-
DSP320CM10-25B/QC	5962-8763304QC	15.0 to 25.6	156	40L Ceramic Side-Braze	Gold	X
DSP320CM10-25B/UA	5962-8763304XA X	15.0 to 25.6	156	44 Terminal LCC	Solder	-
DSP320CM10-25B/UC	5962-8763304XC	15.0 to 25.6	156	44 Terminal LCC	Gold	X

PART NUMBERS - MILITARY (see next page for Commercial and Industrial Parts)

DSP320x10 - 32 I / Q A

Lead Finish:		A	Solder Dip
		C	Gold
Case Outline:		Q	44 Pin Side Braze DIL
		U	40 Terminal LCC
Screening Level*:		B	MIL-STD-883C Compliant (-55° C to 125° C)
Frequency:		-	20.5 MHz
		25	25.6 MHz
Device:	DSP32010		NMOS DSP
	DSP320C10		CMOS DSP
	DSP320CF10		CMOS DSP, 6.7 to 25.6 MHz
	DSP320C10		CMOS DSP, ROM Version

***Note:** 32010 = TE (Thermally Enhanced LCC); 320C10 = NTE (Non-Thermally Enhanced LCC)

PART NUMBERS - DESC SMD

5xx2 87633 30x Q A

Lead Finish:		A	Solder Dip
		C	Gold
Case Outline*:		X	Ceramic Dual-in-line (28 lead)
		Q	Ceramic Side Braze DIL(40 lead)
		Z	Flat pack
Version:		301	6.7 to 20.5 MHz
		302	15.0 to 25.6 MHz
		303	6.7 to 20.5 MHz, ROM Version
		304	15.0 to 25.6 MHz, ROM Version
		305	6.7 to 25.6 MHz
Device:		5962	CMOS DSP
		5692	NMOS DSP

***Note:** The Case Outline Code is used for order entry only and will not be marked on device

NOTES:

DSP320C10

CMOS Digital Signal Processor

FEATURES

- 122ns instruction cycle
- 144 word on-chip data RAM
- ROM-less version — DSP320C10
- 1.5K word on-chip program ROM—DSP320CM10
- External memory expansion to a total of 4K words at full speed
- 16-bit instruction/data word
- 32-bit ALU/Accumulator
- 16 x 16-bit multiply in 122ns
- 0 to 15-bit barrel shifter
- Eight input and eight output channels
- 16-bit bidirectional data bus with a 65Mbps transfer rate
- Interrupt with a full context save
- Signed two's complement fixed-point arithmetic
- CMOS technology
- Single 5 volt supply
- Four versions available:

—DSP320C10-14	14.4MHz Clock
—DSP320C10	20.5MHz Clock
—DSP320C10-25	25.6MHz Clock
—DSP320C10-32	32.8MHz Clock

DESCRIPTION

The DSP320C10 is the first low power CMOS member of the Microchip Technology DSP320 family of digital signal processors, designed to support a wide range of high-speed or numeric-intensive applications. This device is a CMOS pin-for-pin compatible version of the industry standard DSP32010 digital signal processor.

The processor has been enhanced to make the Data RAM static with respect to the Reset. Also, the address hold time has been improved to a non-negative value.

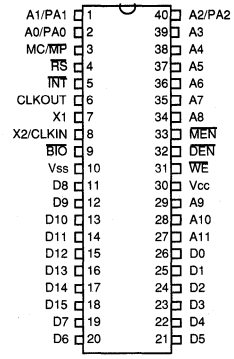
This 16/32 bit single-chip microcomputer combines the flexibility of a high-speed controller with the numerical capability of an array processor thereby offering an inexpensive alternative to multichip bit-slice processors. The DSP320 family contains MOS microcomputers capable of executing eight million instructions per second. This high throughput is the result of the comprehensive, efficient, and easily programmed instruction set and of the highly pipelined architecture. Special instructions have been incorporated to speed the execution of digital signal processing (DSP) algorithms.

The DSP320 family's unique versatility and power give the design engineer solutions to a variety of complicated applications. In addition, these microcomputers are capable of providing the multiple functions often required for a single application. For example, the DSP320 family can enable an industrial robot to synthesize and recognize speech, sense objects with radar or optical intelligence, and perform mechanical operations through digital servo loop computations.

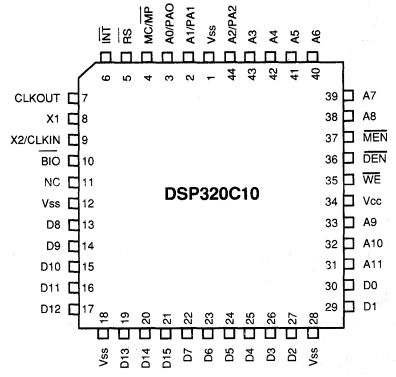
PIN CONFIGURATION

Top View

40 LEAD DIP



44 PIN PLCC



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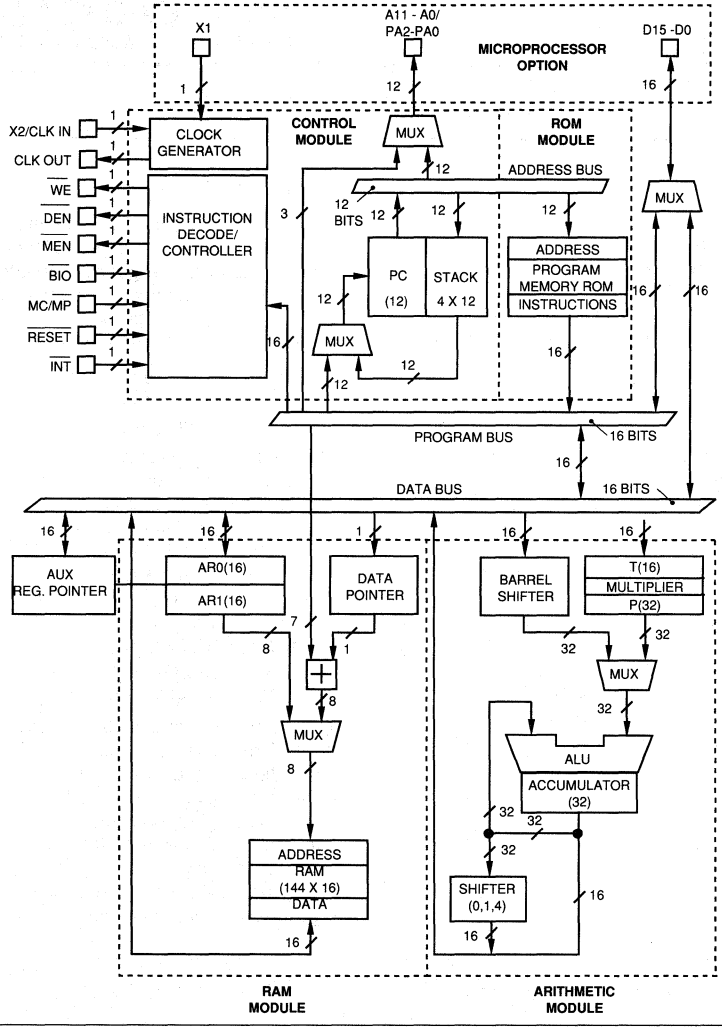
DSP320C10 BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	I/O	Definition	Name	I/O	Definition
A11-A0/ PA2-PA0	OUT	External address bus. I/O port address multiplexed over PA2-PA0.	MC/$\overline{MP}$	IN	Memory mode select: High selects microcomputer, low selects microprocessor mode.
$\overline{BIO}$	IN	External polling input for bit test and jump operations.	$\overline{MEN}$	OUT	Memory enable indicates that D15-D0 will accept external memory instruction.
CLKOUT	OUT	System clock output, 1/4 crystal CLKIN frequency.	$\overline{RS}$	IN	Reset used to initialize device.
			VCC	IN	Power.
D15-D0	I/O	16-bit data bus.	VSS	IN	Ground.
$\overline{DEN}$	OUT	Data enable indicates the processor accepting input data on D15-D0.	$\overline{WE}$	OUT	Write enable indicates valid data on D15-DO.
			X1	IN	Crystal input.
$\overline{INT}$	IN	Interrupt.	X2/CLKIN	IN	Crystal input or external clock input.

ARCHITECTURE

The DSP320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of the instruction fetch and execution. The DSP320 family's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

The DSP320C10 utilizes hardware to implement functions that other processors typically perform in software. For example, this device contains a hardware multiplier to perform a multiplication in a single 122ns cycle. There is also a hardware barrel shifter for shifting data on its way into the ALU. Finally, extra hardware has been included so that auxiliary registers, which provide indirect data RAM addresses, can be configured in an auto increment/decrement mode for single-cycle manipulation of data tables. This hardware-intensive approach gives the design engineer the type of power previously unavailable on a single chip.

32-bit ALU/Accumulator

The DSP320C10 contains a 32-bit ALU and accumulator that support double-precision arithmetic. The ALU operates on 16-bit words taken from the data RAM or derived from immediate instructions. Besides the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller.

Shifters

A barrel shifter is available for left-shifting data 0 to 15 places before it is loaded into, subtracted from, or added to the accumulator. This shifter extends the high-order bit of the data word and zero-fills the low-order bits for two's complement arithmetic A second shifter left-shifts the upper half of the accumulator 0, 1, or 4 places while it is being stored in the data RAM. Both shifters are very useful for scaling and bit extraction.

16 x 16-bit Parallel Multiplier

The DSP320C10's multiplier performs a 16 x 16-bit, two's complement multiplication in one 122ns instruction cycle. The 16-bit T Register temporarily stores the multiplicand; the P Register stores the 32-bit result. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the DSP320C10 to perform such fundamental operations as convolution, correlation, and filtering at a very high rate.

Program Memory Expansion

The DSP320C10 is equipped with a 1536-word ROM which can be mask-programmed at the factory with a customer's program. It can also execute from an additional 2560 words of off-chip program memory at full speed. This memory expansion capability is especially useful for those situations where a customer has a number of different applications that share the same subroutines. In this case, the common subroutines can be stored on-chip while the application specific code is stored off-chip.

The DSP 320C10 can operate in either of the following memory modes via the MC/$\overline{MP}$ pin:

Microcomputer Mode (MC)—Instruction addresses 0-1535 fetched from on-chip ROM. Those with addresses 1536-4095 fetched from off-chip memory at full speed.

Microprocessor Mode ($\overline{MP}$)—Full speed execution from all 4096 off-chip instruction addresses.

The ability of the DSP320C10 to execute at full speed from off-chip memory provides important benefits:

- Easier prototyping and development work than is possible with a device that can address only on-chip ROM
- Purchase of a standard off-the-shelf product rather than a semi-custom mask-programmed device
- Ease of updating code
- Execution from external RAM
- Downloading of code from another microprocessor
- Use of off-chip RAM to expand data storage capability

Input/Output

The DSP320C10's 16-bit parallel data bus can be utilized to perform I/O functions at burst rates of 65 million bits per second. Available for interfacing to peripheral devices are 128 input and 128 output bits consisting of eight 16-bit multiplexed input ports and eight 16-bit multiplexed output ports. In addition, a polling input for bit test and jump operations (BIO) and an interrupt pin ($\overline{INT}$) have been incorporated for multi-tasking.

Interrupts and Subroutines

The DSP320C10 contains a four-level hardware stack for saving the contents of the program counter during interrupts and subroutine calls. Instructions are available for saving the DSP320C10's complete context. The instructions, PUSH stack from accumulator, and POP stack to accumulator permit a level of nesting restricted only by the amount of available RAM. The interrupts used in the DSP320C10 are maskable.

INSTRUCTION SET

The DSP320C10's comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general purpose operations, such as high-speed control. The instruction set, explained in Tables 1 and 2, consists primarily of single-cycle single-word instructions, permitting execution rates of up to eight million instructions per second. Only infrequently used branch and I/O instructions are multicycle.

The DSP320C10 also contains a number of instructions that shift data as part of an arithmetic operation. These all execute in a single cycle and are very useful for scaling data in parallel with other operations.

Three main addressing modes are available with the DSP320C10 instruction set: direct, indirect, and immediate addressing.

Direct Addressing

In direct addressing, seven bits of the instruction word concatenated with the data page pointer form the data memory address. This implements a paging scheme in which the first page contains 128 words and the second page contains 16 words. In a typical application, infrequently accessed variables, such as those used for servicing an interrupt, are stored on the second page. The instruction format for direct addressing is shown below.

15 14 13 12 11 10 9 8	7	6 5 4 3 2 1 0
OPCODE	0	DMA

Bit 7 = 0 defines direct addressing mode. The opcode is contained in bits 15 through 8. Bits 6 through 0 contain data memory address.

The seven bits of the data memory address (DMA) field can directly address up to 128 words (1 page) of data memory. Use of the data memory page pointer is required to address the full 144 words of data memory.

Direct addressing can be used with all instructions requiring data operands except for the immediate operand instructions.

Indirect Addressing

Indirect addressing forms the data memory from the least significant eight bits of one of two auxiliary registers, AR0 and AR1. The auxiliary register pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. The instruction format for indirect addressing is as follows:

15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
OPCODE	1	0	INC	DEC	NAR	0	0	ARP

Bit7 = 1 defines indirect addressing mode. The opcode is contained in bits 15 through 8. Bits 7 through 0 contain indirect addressing control bits.

Bit 3 and bit 0 control the Auxiliary Register Pointer (ARP). If bit 3 = 0, then the content of bit 0 is loaded into the ARP. If bit 3 = 1, then content of ARP remain unchanged. ARP = 0 defines the contents of AR0 as memory address. ARP = 1 defines the contents of AR1 as memory address.

Bit 5 and bit 4 control the auxiliary registers. If bit 5 = 1, then the ARP defines which auxiliary register is to be incremented by 1. If bit 4 = 1, then the ARP defines which auxiliary register is to be decremented by 1. If bit 5 or bit 4 are zero, then neither auxiliary register is incremented or decremented. Bits 6, 2 and 1 are reserved and should always be programmed to zero.

Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

Immediate Addressing

The DSP320C10 instruction set contains special "immediate" instructions. These instructions derive data from part of the instruction word rather than from the data RAM. Some very useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

INSTRUCTION SET SUMMARY

TABLE 1 - INSTRUCTION SYMBOLS

Symbol	Meaning
ACC	Accumulator
D	Data memory address field
I	Addressing mode bit
K	Immediate operand field
PA	3-bit port address field
R	1-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

TABLE 2 - ACCUMULATOR INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS	Absolute value of accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0
ADD	Add to accumulator with shift	1	1	0	0	0	0	←		S	→	I	←			D			→
ADDH	Add to high-order accumulator bits	1	1	0	1	1	0	0	0	0	0	I	←			D			→
ADDS	Add to accumulator with no sign extension	1	1	0	1	1	0	0	0	0	1	I	←			D			→
AND	AND with accumulator	1	1	0	1	1	1	1	0	0	1	I	←			D			→
LAC	Load accumulator with shift	1	1	0	0	1	0	←		S	→	I	←			D			→
LACK	Load accumulator immediate	1	1	0	1	1	1	1	1	1	0	←				K			→
OR	OR with accumulator	1	1	0	1	1	1	1	0	1	0	I	←			D			→
SACH	Store high-order accumulator bits with shift	1	1	0	1	0	1	1	←	X	→	I	←			D			→
SACL	Store low-order accumulator bits	1	1	0	1	0	1	0	0	0	0	I	←			D			→
SUB	Subtract from accumulator with shift	1	1	0	0	0	1	←		S	→	I	←			D			→
SUBC	Conditional subtract (for divide)	1	1	0	1	1	0	0	1	0	0	I	←			D			→
SUBH	Subtract from high-order	1	1	0	1	1	0	0	0	1	0	I	←			D			→
SUBS	Subtract from accumulator with no sign extension	1	1	0	1	1	0	0	0	1	1	I	←			D			→
XOR	Exclusive OR with accumulator	1	1	0	1	1	1	1	0	0	0	I	←			D			→
ZAC	Zero accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	1
ZALH	Zero accumulator and load high-order bits	1	1	0	1	1	0	0	1	0	1	I	←			D			→
ZALS	Zero accumulator and load low-order bits with no sign extension	1	1	0	1	1	0	0	1	1	0	I	←			D			→

6

INSTRUCTION SET SUMMARY (CONT.)

TABLE 2 (CONT.) - AUXILIARY REGISTER AND DATA PAGE POINTER INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAR	Load auxiliary register	1	1	0	0	1	1	1	0	0	R	I	←			D	→		
LARK	Load auxiliary register immediate	1	1	0	1	1	1	0	0	0	R	←				K	→		
LARP	Load auxiliary register pointer immediate	1	1	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	K
LDP	Load data memory page pointer	1	1	0	1	1	0	1	1	1	1	I	←			D	→		
LDPK	Load data memory page pointer immediate	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	K
MAR	Modify auxiliary register and pointer	1	1	0	1	1	0	1	0	0	0	I	←			D	→		
SAR	Store auxiliary register	1	1	0	0	1	1	0	0	0	R	I	←			D	→		

TABLE 2 (CONT.) - BRANCH INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	Branch unconditionally	2	2	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BANZ	Branch on auxiliary register not zero	2	2	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BGEZ	Branch if accumulator ≥ 0	2	2	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BGZ	Branch if accumulator > 0	2	2	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BIOZ	Branch on $\overline{BIO}$ = 0	2	2	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BLEZ	Branch if accumulator ≤ 0	2	2	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BLZ	Branch if accumulator < 0	2	2	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BNZ	Branch if accumulator ≠ 0	2	2	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BV	Branch on overflow	2	2	1	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
BZ	Branch if accumulator = 0	2	2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
CALA	Call subroutine from accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0
CALL	Call subroutine immediately	2	2	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	←			BRANCH ADDRESS					→			
RET	Return from subroutine or interrupt routine	2	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1

INSTRUCTION SET SUMMARY (CONT.)

TABLE 2 (CONT.) - T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APAC	Add P register to accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1
LT	Load T register	1	1	0	1	1	0	1	0	1	0	I	←			D			→
LTA	LTA combines LT and APAC into one instruction	1	1	0	1	1	0	1	1	0	0	I	←			D			→
LTD	LTD combines LT, APAC, and DMOV into one instruction	1	1	0	1	1	0	1	0	1	1	I	←			D			→
MPY	Multiply with T register, store product in P register	1	1	0	1	1	0	1	1	0	1	I	←			D			→
MPYK	Multiply T register with immediate operand; store product in P register	1	1	1	0	0	←						K						→
PAC	Load accumulator from P register	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	1	0
SPAC	Subtract P register from accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0

TABLE 2 (CONT.) - CONTROL INSTRUCTIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DINT	Disable interrupt	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0
LST	Load status register	1	1	0	1	1	1	1	0	1	1	I	←			D			→
NOP	No operation	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
POP	POP stack to accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	0	1
PUSH	PUSH stack from accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	1	1	1	0	0
ROVM	Reset overflow mode	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1
SOVM	Set overflow mode	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1
SST	Store status register	1	1	0	1	1	1	1	1	0	0	I	←			D			→

TABLE 2 (CONT.) - I/O AND DATA MEMORY OPERATIONS

Mnemonic	Description	Number of Cycles	Number of Words	OpCode - Instruction Register 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMOV	Copy contents of data memory	1	1	0	1	1	0	1	0	0	1	I	←			D			→
IN	Input data from port	2	1	0	1	0	0	0	←	PA	→	I	←			D			→
OUT	Output data to port	2	1	0	1	0	0	1	←	PA	→	I	←			D			→
TBLR	Table read from program memory to data RAM	3	1	0	1	1	0	0	1	1	1	I	←			D			→
TBLW	Table write from data RAM to program (external only)	3	1	0	1	1	1	1	1	0	1	I	←			D			→

6

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Over specified temperature range (unless otherwise noted)**

Supply voltage, V_{CC} ..... -0.3V to 7V
All input voltages ..... -0.3V to 7V
Output voltage ..... -0.3V to 7V

Continuous power dissipation:

DSP320C10 (0° to +70°C) 0.3W
DSP320C10I (-40° to +85°C) 0.36W
DSP320C10-25 (0° to +70°C) 0.35W
DSP320C10I-25 (-40° to +85°C) 0.4W

Air temperature range above operating device:

– Commercial ..... 0° C to 70° C
– Industrial ..... -40° C to 85° C

Storage Temperature Range ..... -55° C to 150° C
Junction Temperature (TJ) ..... 165° C

**Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

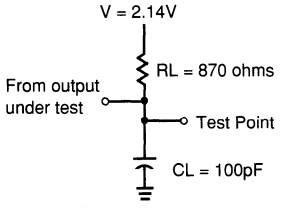
DC CHARACTERISTICS

*V_{CC} = 5V, TA = 25° C

Characteristics	DSP320C10			DSP320C10-14			DSP320C10-25			DSP320C10-32			Unit	Conditions
	Min	Nom*	Max	Min	Nom*	Max	Min	Nom*	Max	Min	Nom*	Max		
Supply voltage, V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V	
Supply voltage, V_{SS}	—	0	—	—	0	—	—	0	—	—	0	—	V	
High-level input voltage, V_{IH}														
- All inputs except CLKIN	2.0	—	—	2.0	—	—	2.0	—	—	2.0	—	—	V	
- CLKIN	.65Vcc	—	—	.65Vcc	—	—	.65Vcc	—	—	.65Vcc	—	—	V	
Low-level input voltage, V_{IL} (all inputs)	—	—	0.8	—	—	0.8	—	—	0.8	—	—	0.8	V	
High-level output voltage V_{OH}	Vcc-.4	—	—	Vcc-.4	—	—	Vcc-.4	—	—	Vcc-.4	—	—	V	I_{OH} = 20µA
	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V	I_{OH} = 300µA
Low-level output voltage, V_{OL}	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V	I_{OL} = 2mA
Off-state output current, I_{OZ}	—	—	20	—	—	20	—	—	20	—	—	20	µA	V_{CC} = 5.5V
	—	—	-20	—	—	-20	—	—	-20	—	—	-20	µA	V_O = V_{CC} - .4V
Input current, I_I	—	—	±50	—	—	±50	—	—	±50	—	—	±50	µA	
Supply current, I_{CC} (tested w/clocks running & part in reset)	—	—	50	—	—	50	—	—	55	—	—	65	mA	V_{CC} = 5.5V
Input capacitance, C_I														f = 1MHz, all other pins 0V
- Data bus	—	25	—	—	25	—	—	25	—	—	25	—	pF	
- All others	—	15	—	—	15	—	—	15	—	—	15	—	pF	
Output capacitance, C_O														
- Data bus	—	25	—	—	25	—	—	25	—	—	25	—	pF	
- All others	—	10	—	—	10	—	—	10	—	—	10	—	pF	

PARAMETER MEASUREMENT INFORMATION

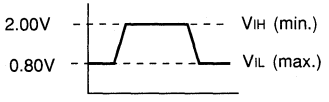
FIGURE 2 - TEST LOAD CIRCUIT



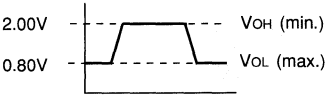
TTL Load Condition

FIGURE 3 - AC TIMING VOLTAGE REFERENCE LEVELS

a. Inputs, TTL compatible



b. Outputs, TTL compatible



6

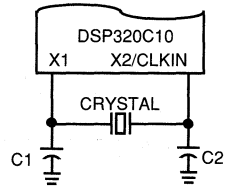
CLOCK

The DSP320C10 can use either its internal oscillator or an external frequency source for a clock.

INTERNAL CLOCK OPTION

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (See Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency.

FIGURE 1 - INTERNAL CLOCK OPTION



The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1mW, and be specified at a load capacitance of 20pF.

EXTERNAL CLOCK OPTION

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected.

The external frequency injected must conform to the specifications listed in the table below.

CLOCK FREQUENCIES

Characteristics	Sym	Min	Nom	Max	Unit	Temperature Range Conditions
DSP320C10 Crystal frequency	fx	6.7	—	20.5	MHz	I, C
DSP320C10-14 Crystal frequency	fx	6.7	—	14.4	MHz	I, C
DSP320C10-25 Crystal frequency	fx	6.7	—	25.6	MHz	I, C
DSP320C10-32 Crystal frequency	fx	6.7	—	32.8	MHz	I, C
C1,C2		—	10	—	pf	I, C

CLOCK (CONT.)

CLOCK AC CHARACTERISTICS

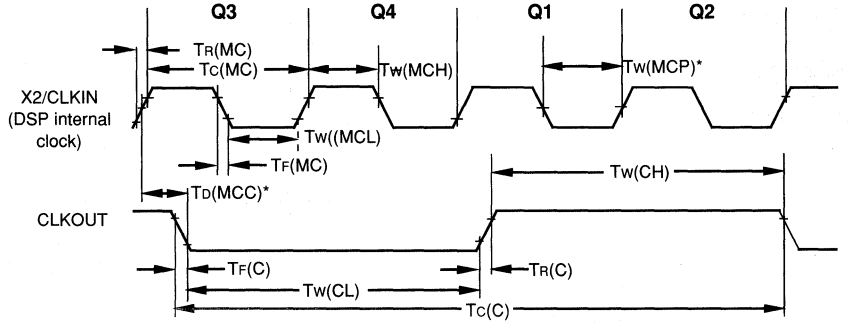
Timing requirements/Switching Characteristics over Recommended Operating Conditions

T_A (Commercial) = 0° to 70° C
T_A (Industrial) = -40° to 85° C
V_{CC} = 5V + 10%, V_{SS} = 0V

		DSP320C10			DSP320C10-14			DSP320C10-25			DSP320C10-32				
Characteristics	**Sym**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Unit**	**Conditions**
Master clk cycle time	$T_{C(MC)}$	48.78	—	150	69.50	—	150	39	—	150	30.5	—	150	ns	Note 1
Rise time mast. clk in.	$T_{R(MC)}$	—	5	10*	—	5	10*	—	4	8*	—	3	6*	ns	
Fall time mast. clk in.	$T_{F(MC)}$	—	5	10*	—	5	10*	—	4	8*	—	3	6*	ns	
Pulse dur. mast. clk low, Tc(MC) = 70ns	$T_{W(MCL)}$	14*	20	—	14*	20	—	12*	16	—	8*	12	—	ns	
Pulse dur. mast clk high, Tc(MC) = 70ns	$T_{W(MCH)}$	14*	20	—	14*	20	—	12*	16	—	8*	12	—	ns	
Pulse dur. mast clk	$T_{W(MCP)}$	0.4$T_{C(C)}$*	—	0.6$T_{C(C)}$*	0.4$T_{C(C)}$*	—	0.6$T_{C(C)}$*	0.45$T_{C(C)}$*	—	0.55$T_{C(C)}$*	0.45$T_{C(C)}$*	—	0.55$T_{C(C)}$*	ns	
CLKOUT cycle time	$T_{C(C)}$	195.12	—	—	277.80	—	—	156	—	—	122	—	—	ns	
CLKOUT rise time	$T_{R(C)}$	—	10	—	—	10	—	—	10	—	—	4	—	ns	
CLKOUT fall time	$T_{F(C)}$	—	8	—	—	8	—	—	8	—	—	7	—	ns	
Pls. dur., CLKOUT low	$T_{W(CL)}$	—	92	—	—	131	—	—	74	—	—	57	—	ns	See Fig 2
Pls. dur., CLKOUT high	$T_{W(CH)}$	—	90	—	—	129	—	—	72	—	—	54	—	ns	
Delay time to CLKIN↑ to CLKOUT↓ (Note 2)	$T_{D(MCC)}$	10	—	60	10	—	60	10	—	50	10	—	50	ns	

Note: (1) TC(C) is the cycle time of CLKOUT. i.e., 4*TC(MC) (4 times CLKIN cycle time if an external oscillator is used)
(2) **These values were derived from characterization data and are not tested or guaranteed.*

CLOCK TIMING



* TD(MCC) and TW(MCP) are referenced to an intermediate level of 1.5 volts on the CLKIN waveform.
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

6

MEMORY AND PERIPHERAL INTERFACE TIMING

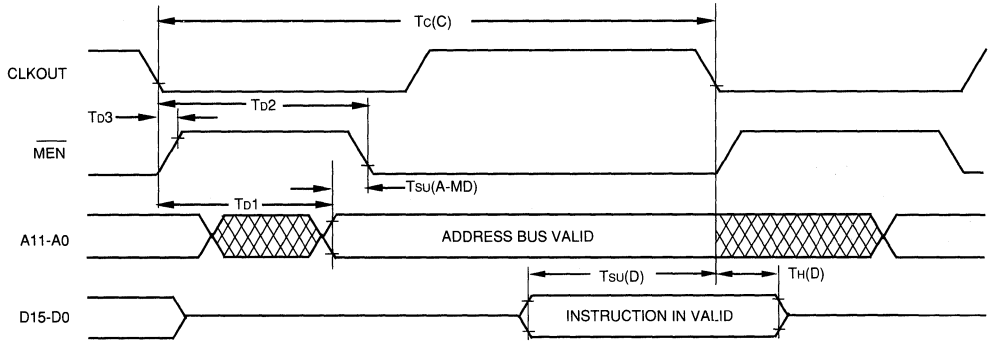
MEMORY AND PERIPHERAL INTERFACE - AC CHARACTERISTICS
Over recommended operating conditions

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Delay time CLKOUT↓ to address bus valid (see note)	Td1	10*	—	38	ns	See Figure 2
Delay time CLKOUT↓ to $\overline{MEN}$↓	Td2	1/4Tc(C) -5*	—	1/4Tc(C) +12	ns	
Delay time CLKOUT↓ to $\overline{MEN}$↑	Td3	-8*	—	12	ns	
Delay time CLKOUT↓ to $\overline{DEN}$↓	Td4	1/4Tc(C) -5*	—	1/4Tc(C) +12	ns	
Delay time CLKOUT↓ to $\overline{DEN}$↑	Td5	-8*	—	12	ns	
Delay time CLKOUT↓ to $\overline{WE}$↓	Td6	1/2Tc(C) -5*	—	1/2Tc(C) +12	ns	
Delay time CLKOUT↓ to $\overline{WE}$↑	Td7	-8*	—	12	ns	
Delay time CLKOUT↓ to data bus OUT valid	Td8	—	—	1/4Tc(C) +40	ns	
Time after CLKOUT↓ that data bus starts to be driven	Td9	1/4Tc(C) - 5*	—	—	ns	
Time after CLKOUT↓ that data bus stops being driven	Td10	—	—	1/4Tc(C) +30*	ns	
Data bus OUT valid after CLKOUT↓	Tv	1/4Tc(C) - 10	—	—	ns	
Delay time $\overline{DEN}$↑, $\overline{MEN}$↑ and $\overline{WE}$↑ from $\overline{RS}$↓	Td11	-	—	Tc(C) + 50*	ns	
Setup time data bus valid prior to CLKOUT↓	Tsu(D)	38	—	—	ns	
Hold time data bus held valid after CLKOUT↓	Th(D)	0	—	—	ns	
Address bus setup time prior to $\overline{MEN}$↓ or $\overline{DEN}$↓	Tsu (A-MD)	1/4Tc(C) -35	—	—	ns	
Address bus hold after $\overline{WE}$↑, $\overline{MEN}$↑ or $\overline{DEN}$↑	Th(A-WMD)	5	—	—	ns	
Address bus setup time prior to $\overline{WE}$↓	Tsu(A-WE)	1/2Tc(C) -34	—	—	ns	
Data bus setup time prior to $\overline{WE}$↓	Tsu(D-WE)	1/4Tc(C) -32	—	—	ns	
Data bus hold after $\overline{WE}$↑	Th(D-WE)	1/4Tc(C) -18	—	—	ns	
External memory access time	Tacc	—	—	Tc(C) - 69	ns	
External memory output enable time	Toe	—	—	3/4 Tc(C) - 40	ns	

*These values were derived from characterization data and are not tested.
Note: 1. Address bus will be valid upon $\overline{WE}$↑, $\overline{DEN}$↑, or $\overline{MEN}$↑.
2. Data may be removed from the data bus upon $\overline{MEN}$↑ or $\overline{DEN}$↑ preceding CLKOUT↓

MEMORY AND PERIPHERAL INTERFACE TIMING (CONT.)

MEMORY READ TIMING DIAGRAM

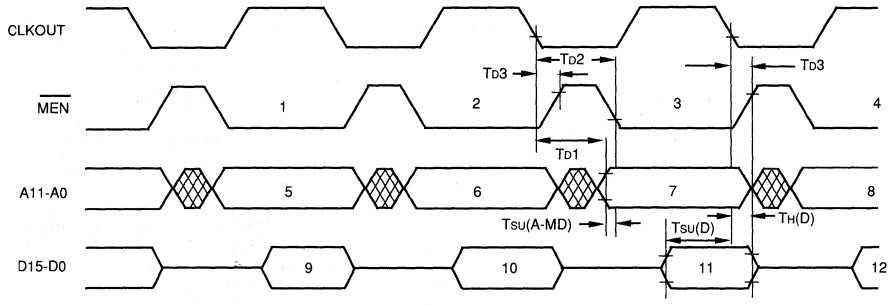


Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

6

INSTRUCTION TIMING DIAGRAMS (CONT.)

TBLR INSTRUCTION TIMING DIAGRAM

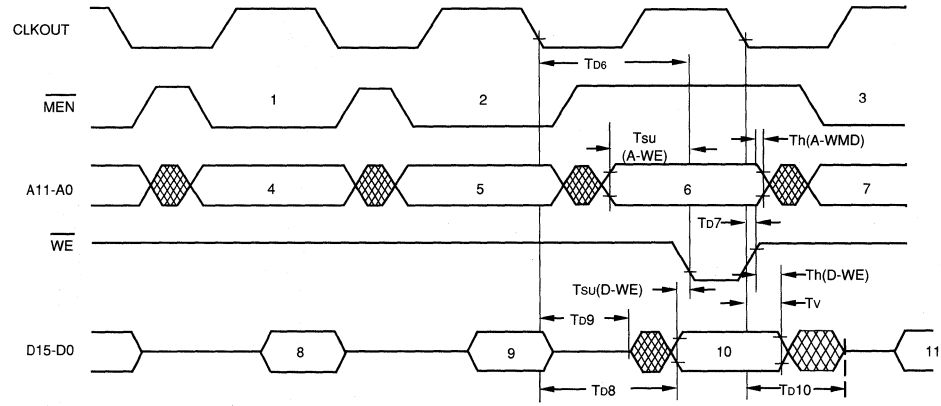


Legend:

1. TBLR INSTRUCTION PREFETCH
2. DUMMY PREFETCH
3. DATA FETCH
4. NEXT INSTRUCTION PREFETCH
5. ADDRESS BUS VALID
6. ADDRESS BUS VALID
7. ADDRESS BUS VALID
8. ADDRESS BUS VALID
9. INSTRUCTION IN VALID
10. INSTRUCTION IN VALID
11. DATA IN VALID
12. INSTRUCTION IN VALID

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

TBLW INSTRUCTION TIMING DIAGRAM



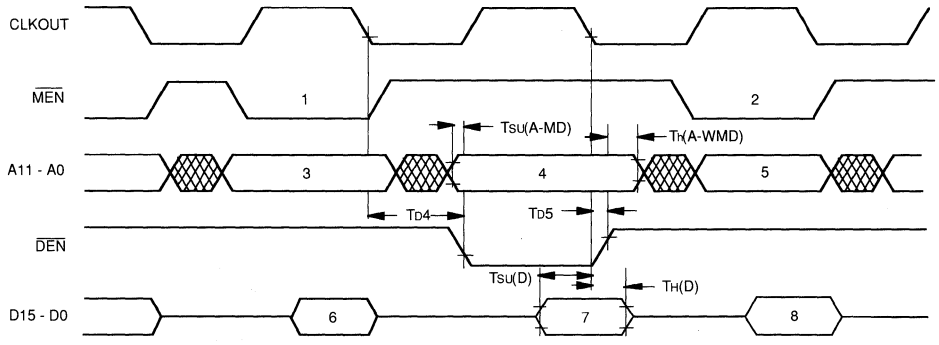
Legend:

1. TBLW INSTRUCTION PREFETCH
2. DUMMY PREFETCH
3. NEXT INSTRUCTION PREFETCH
4. ADDRESS BUS VALID
5. ADDRESS BUS VALID
6. ADDRESS BUS VALID
7. ADDRESS BUS VALID
8. INSTRUCTION IN VALID
9. INSTRUCTION IN VALID
10. DATA OUT VALID
11. INSTRUCTION IN VALID

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

INSTRUCTION TIMING DIAGRAMS (CONT.)

IN INSTRUCTION TIMING DIAGRAM

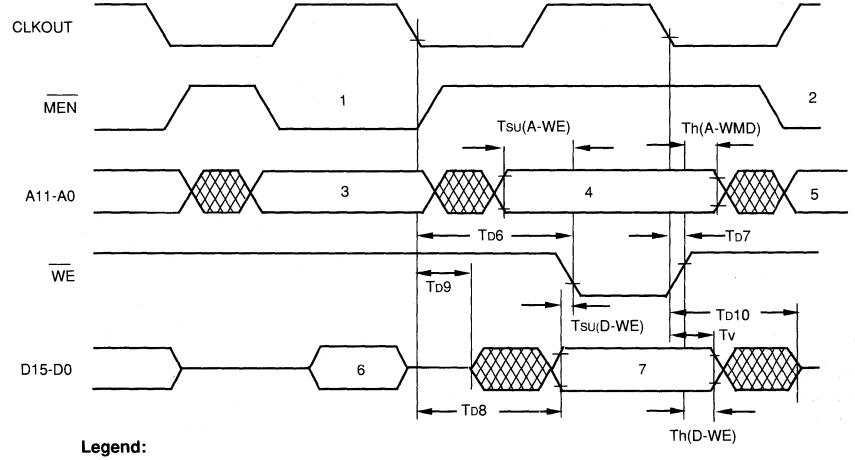


Legend:

1. IN INSTRUCTION PREFETCH
2. NEXT INSTRUCTION PREFETCH
3. ADDRESS BUS VALID
4. PERIPHERAL ADDRESS VALID
5. ADDRESS BUS VALID
6. INSTRUCTION IN VALID
7. DATA IN VALID
8. INSTRUCTION IN VALID

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

OUT INSTRUCTION TIMING DIAGRAM



Legend:

1. OUT INSTRUCTION PREFETCH
2. NEXT INSTRUCTION PREFETCH
3. ADDRESS BUS VALID
4. PERIPHERAL ADDRESS VALID
5. ADDRESS BUS VALID
6. INSTRUCTION IN VALID
7. DATA OUT VALID

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

6

RESET (RS) TIMING

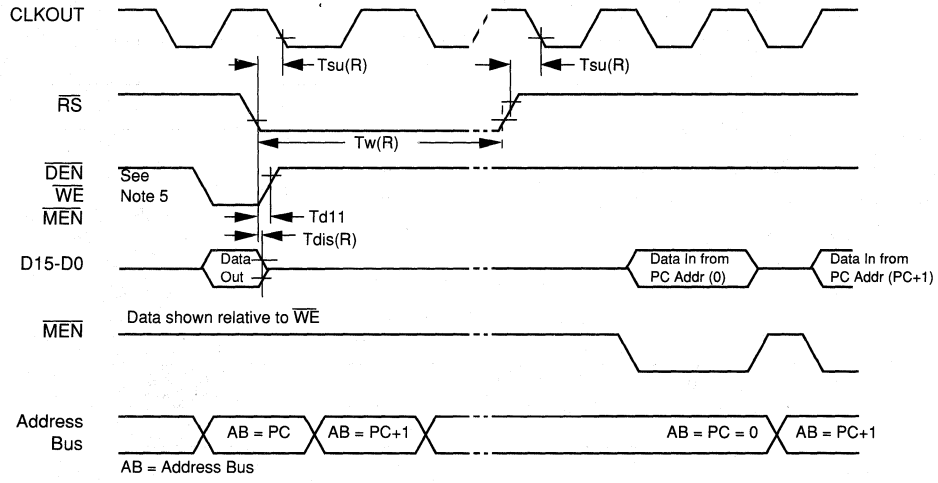
RESET TIMING AC CHARACTERISTICS

Timing requirements over recommended operating conditions

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
Reset ($\overline{RS}$) setup time prior to CLKOUT. See notes 1-4. DSP320C10-32	Tsu(R)	38	—	—	ns	See Figure 2
$\overline{RS}$ pulse duration	Tw(R)	5Tc(C)	—	—	ns	
Delay time $\overline{DEN}\uparrow$, $\overline{WE}\uparrow$, and $\overline{MEN}\uparrow$ from $\overline{RS}\downarrow$	Td11	—	—	Tc(C) + 50*	ns	
Data bus disable time after $\overline{RS}$	Tdis(R)	—	—	3/4Tc(C) + 120*	ns	

Note: RS can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.
*These values were derived from characterization data and are not tested.

FIGURE 4 - RESET TIMING



Notes:

1. $\overline{RS}$ forces $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ high and tristates data bus DO through D15. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from $\overline{RS}\downarrow$.
2. $\overline{RS}$ must be maintained for a minimum of five clock cycles.
3. Resumption of normal program will commence after one complete CLK cycle from $\overline{RS}\uparrow$.
4. Due to the synchronizing action on $\overline{RS}$, time to execute the function can vary dependent upon when $\overline{RS}\uparrow$ or $\overline{RS}\downarrow$ occur in the CLK cycle.
5. Diagram shown is for definition purpose only. $\overline{DEN}$, $\overline{WE}$, and $\overline{MEN}$ are mutually exclusive.
6. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
7. During a write cycle, $\overline{RS}$ may produce an invalid write address.

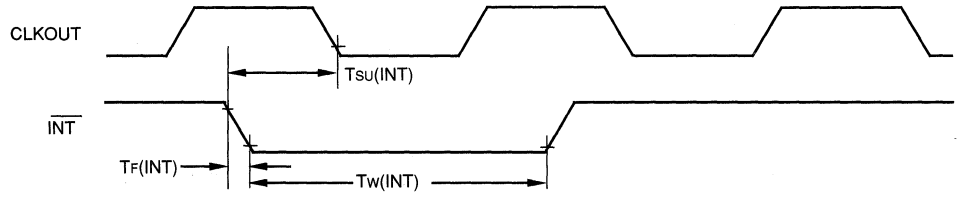
INTERRUPT (INT) TIMING

INTERRUPT TIMING AC CHARACTERISTICS

Timing requirements over recommended operating conditions * These values are not tested

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
Fall time $\overline{INT}$	$T_f(INT)$	—	—	15*	ns	
Pulse duration $\overline{INT}$	$T_w(INT)$	$T_c(C)$	—	—	ns	
Setup time $\overline{INT}\downarrow$ before CLKOUT$\downarrow$	$T_{su}(INT)$	38	—	—	ns	

INTERRUPT TIMING DIAGRAM



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

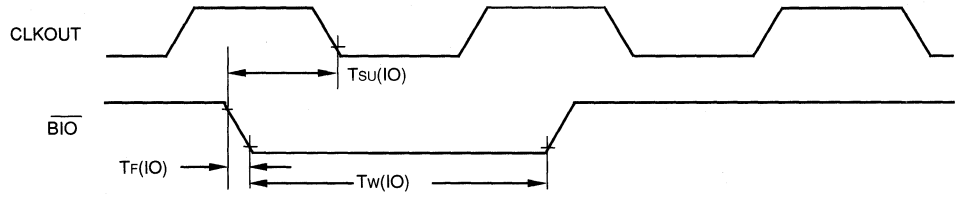
I/O (BIO) TIMING

I/O (BIO) AC CHARACTERISTICS

Timing requirements over recommended operating conditions * These values are not tested

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
Fall time $\overline{BIO}$	$T_f(IO)$	—	—	15*	ns	
Pulse duration $\overline{BIO}$	$T_w(IO)$	$T_c(C)$	—	—	ns	
Setup time $\overline{BIO}\downarrow$ before CLKOUT$\downarrow$	$T_{su}(IO)$	38	—	—	ns	

I/O (BIO) TIMING DIAGRAM



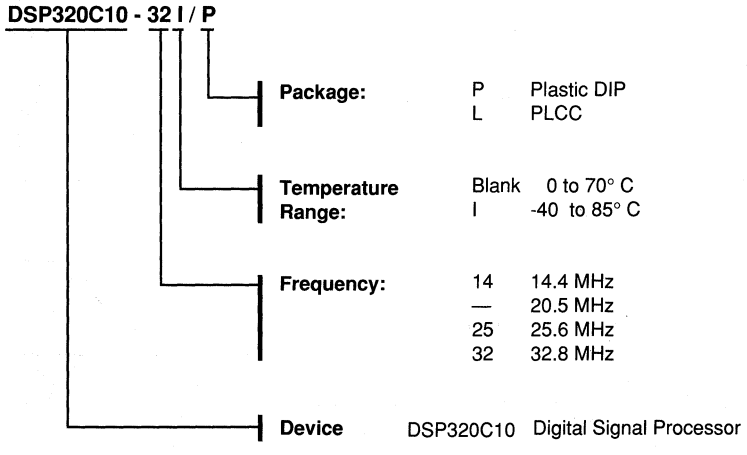
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

6

SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



SECTION 7
QUALITY AND RELIABILITY

Microchip

Quality Without Compromise

A CORPORATE COMMITMENT

Raising the quality level of Microchip's products and services is a performance alliance built with customers and suppliers.

Total quality improvement and quality awareness is powered by company-wide participation.

Meeting a customer's expectations is where quality commitment begins. The resolve to continuously improve never ends.

THE CHALLENGE OF COMPLEXITY

Integrating an Ideal

Microchip's quality programs and business plan are vertically integrated and touch all levels of the company. From the top down, the President and CEO actively leads programs to ensure continuous improvement is a perpetual process. Quality teams work from the bottom up to improve performance at every department level. Incorporating quality improvement objectives into the business plan creates a unity of purpose and mandates that the two merge as one measurement.

Determination to be the Best

Through statistical management and the use of statistical tools, a framework is built for becoming a continuously improving supplier. These programs are the foundation for success.

PROCESS TECHNOLOGY

All the products manufactured at Microchip make use of a common N-Well CMOS baseline process to which modules are added in order to create the specific functions required by the product (EEPROM, Microcontroller, Logic and EPROM).

The baseline process, which has been in Manufacturing for the last 5 years, uses minimum dimensions of 2μm, 360Å gate oxide thickness, N^+ doped polysilicon gates and arsenic implanted source-drain diffusions for the N-channel devices.

A more advanced process uses minimum dimensions of 1μm, 250Å gate oxide thickness, polycide gate and LDD junction for the N-channel devices. A double level metal modules can be added to both processes.

All of these devices utilize a proprietary passivation suitable for a wide variety of package types. Microchip's processes have been developed with manufacturability, predictability, and reliability as their primary goals.

EEPROM

Microchip's CMOS floating gate EEPROM technology produces a non-volatile memory cell by storing or removing charge from the floating gate. Charge is transferred bidirectionally to the floating gate by Fowler-Nordheim tunneling through a sub-10 nm oxide over the drain of the transistor. This technology produces a memory cell with a typical endurance of > 10^6 cycles.

EPROM

This technology uses a non-volatile memory cell which stores charge on a self aligned floating gate. Electrons are provided to the floating gate via hot electron injection from the drain depletion region. Each byte can typically be programmed in 100 microseconds, and can retain that data for more than 10 years with unlimited reads. Programming is done off-line using an EPROM programmer. This technology is available in a wide variety of plastic packages for one time programming (OTP), or in windowed packages. Block erasing is accomplished with a high intensity UV source through the package window. Windowed parts can be erased and reprogrammed more than 100 times.

Microcontroller and Logic

Logic products are built on both of Microchip's common processes and their derivatives. These products have process modules for production of ROM, Analog, EPROM, and EEPROM in addition to basic logic circuitry.

QUALITY

Design for Quality and Reliability

Product reliability is designed into all Microchip processes and products. Design margins are established to guarantee every product can be produced economically, error-free and within the tolerances of the manufacturing process. Design committee members representing manufacturing, engineering, quality and product divisions ensure that exacting standards are met for each specific product.

Documentation and Procurement Specifications

Microchip's documentation control program assures the correct and current document always is available at the point of use. Active documents are revision coded and serialized. Procurement specifications bear the same requirements. These document control procedures, which are common in the industry for military and high reliability products, are employed by Microchip, system wide.

In Line Controls and Process Assessment

Product integrity is assured by sampling and inspection plans performed in line. This enables Microchip to control and improve product quality levels as product moves through the manufacturing operation. Microchip's acceptance sampling plans in assembly emphasize the attempt to eliminate defective product as it is discovered. Acceptance and sampling plans are based on proprietary low fraction defective (<1000ppm) quality statistics.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at selected process steps. In-process controls are performed by operators in the wafer fabrication and assembly operations. Operators take immediate corrective action if a process step is out of its control limit. Through these in-line controls the true capability of a process is generated. (See Appendix A - Controls)

Control of Customer Quality is attained through a statistical program based on minimum defect capability levels. These levels are defined as the error levels associated with the circuit design and science limitations of the chemistry and physics of processing.

Material controls prevent defective piece parts from getting into the line. Microchip's assembly material control sample plan is typical of the emphasis placed on safeguards. (See Appendix B - Material Controls).

Testing for Margin

Microchip conducts a product's initial test under stringent requirements. All quality assurance tests are run to tighter limits than customer specifications. As part of an outgoing quality assurance program, most products are tested at least two machine tolerances tighter than those limits specified by the customer. Margin testing accounts for normal tolerances of any particular test system and provides the assurance that Microchip's products meet a customer's specifications.

Variation from Expectation

Microchip works to make variation from target as small as possible. The better process is the one that holds the narrowest dispersion. Presently Microchip uses electrical screens to help eliminate short term failures. The long term program of total quality improvement emphasizes continuous improvement.

Individuals in all departments are encouraged to analyze the methods employed at their positions and formulate plans to improve performance. Because a customer could receive part of every mistake, definitive programs are continuously formulated at all working levels, designed to eliminate mistakes and contain error.

Outgoing Quality

Quality Control samples all outgoing product from Microchip final testing. These samples measure in line defect levels after screens have been applied. Root cause analysis follows, initiating technical change to effect continuous improvement.

RELIABILITY

Process Qualification

No priority is more important than the one where processes under which Microchip products are built operate without fail. Engineers labor under strict guidelines to ensure tests of sample lots are precise and reliable. Exacting internal specifications demand every product used to qualify a process endure an accelerated life test. Microcontrollers, EPROMs, EEPROMs, and Logic Products are stressed beyond normal use limits when undergoing high temperature reverse bias, operating life, and retention bake tests.

Package Qualification

Package qualification measures a component's ability to withstand extreme thermal and mechanical stress. All products are stressed to military or high level industrial specifications to ensure reliability.

Ongoing Sampling of Key Reliability Variables

Microchip conducts accelerated mechanical tests, operating life tests and memory retention tests to explore the many ways failures might occur. Data gleaned from continuous testing is used to identify potential reliability problems and for defining action courses to improve product. Microchip's reliability knowledge is shared with customers. This data is available for use in customer's own quality and reliability improvement programs.

RELIABILITY CONCEPTS

Definition

Reliability is the probability of a system or circuit performing its predefined function adequately under specific conditions for a given period of time. Thus, the reliability of a microcircuit is a function of both stress conditions and the time of operation.

The reliability (or probability of survival) range runs from 0 (no chance of survival) to 1 (no chance of failure). Current microelectronic circuits are manufactured and controlled to such tight specifications that reliability figures for the total operation time approaching 1 (i.e., 0.9999) are common. As a result, the complement of reliability, or the failure probability, is more often quoted in current literature.

The failure rate is the rate at which failures occur on units surviving to a specific number of hours of operation. Failure rates per unit circuit-hour would generally be very small. To avoid reporting such small numbers, failure rates have been defined for greater circuit-hours. One thousand circuit-hours is defined as one circuit operating for one thousand hours, or 1,000 circuits operating for 1 hour, etc. The numbers of circuit-hours is the number of circuits multiplied by the number of operation hours for each circuit.

Two methods to define failure rate are commonly used:

* Percent failures per thousand circuit-hours
* Absolute failures per 10^9 circuit-hours, or FITs.

Note that a failure rate of 0.0001%/1000 hours and 1 FIT are equivalent numbers.

Bathtub Curve: Failure Rate Over Time

The generic representational graph of failure rate vs. time takes the shape of a bathtub curve. (Figure 1).

The early failure rate (infant mortality) period starts from initial operation (time T_0) and decreases as time goes on.

Time T_1 signifies the end of the infant mortality period. The next phase of the curve occurs between time T_1 and T_2. This long period of time is distinguished by a nearly constant and very low failure rate. After T_2 is passed, the failure rate starts to increase slowly. This last phase of failure rate vs. time is known as the wear-out period.

Temperature Dependency

In order to establish failure rates in a reasonable time, it is necessary to accelerate the incidence of the failure modes. Higher environmental stress levels than those encountered under normal conditions are needed. The accelerating parameter most employed is junction temperature, although voltage and humidity, for example, are also used. Higher temperatures are capable of accelerating many common failure modes dramatically.

Arrhenius Equation

A number of mathematical models were developed to quantify the relationship between accelerated failure rates and increased junction temperatures. The one model most commonly used employs the Arrhenius Equation. It is as follows:

$$AF = e^x, \text{ where } x = \frac{E_A}{K}\left[\frac{1}{T_N} - \frac{1}{T_A}\right]$$

AF = Acceleration Factor (non-dimensional)

e = 2.718281828 ... (non-dimensional constant)

E_A = Activation energy level (electron volts)

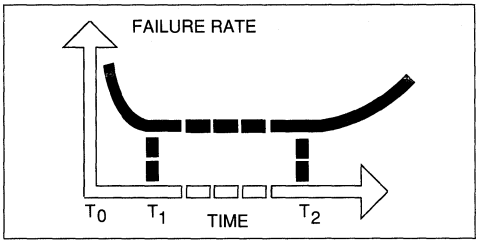
k = Boltzmann's constant = 8.6172×10^{-5} (electron-volts/degree Kelvin)

T_N = Normal junction temperature (degrees Kelvin)

T_A = Accelerated junction temperature (degrees Kelvin)

Thus, the time to achieve a certain probability of failure at time T_1 under temperature T_N can be compressed to T_1 divided by AF at the accelerated temperature, T_A. Note

FIGURE 1: BATHTUB CURVE



7

Activation Energy Level

AF, the dependent variable of the Arrhenius Equation is a function of several variables. T_N and T_A are specified for the situation under consideration. E_A is a function of the particular mode of failure, and can be viewed as the minimum energy required for a particular failure to occur.

Activation energy levels in semiconductors generally are in the 0.3 - 1.1 electron-volt range. Each failure mode has its own activation energy. Some typical examples are:

FAILURE MECHANISM	E_A (eV)
Oxide/Dielectric Defects	0.3
Chemical, Galvanic, or Electrolytic	0.3
Corrosion Silicon Defect	0.5
Electromigration	0.5 to 0.7
Broken Bonds	0.7
Lifted Die	0.7
Surface Related Contamination	1.0
Lifted Bonds (Au-Al Interface)	1.0
Charge Injection	1.3
Floating Gate Charge Loss	0.6
Hot Electron Trapping	-.06
Tunnel Dielectric Breakdown	0.13

A compromise value of 0.6 electron-volts is often used when there are no specific a priori facts relating to the failure modes being accelerated.

There is however, a continuous reliability program at Microchip structured to validate E_A values in use and to categorize new failure mechanisms.

RELIABILITY TESTS

Operating Life Test

The Operating Life Test is run under dynamic bias conditions where inputs are clocked and outputs are loaded in the same way as a typical application. The test is conducted at high temperature to accelerate the failure mechanisms. The normal temperature for the test is +125°C for 1,000 hours. Readouts occur at 24, 168, 500 and 1,000 hours. Early hour failures are usually associated with manufacturing defects or otherwise marginal material. Longer term failures are typically caused by metal migration, ionic contamination, and oxide breakdowns.

High Temperature Reverse Bias (HTRB)

Microchip employs the High Temperature Reverse Bias test to accelerate charge gain onto the floating gate due to oxide defects or accelerate threshold shifts due to ionic contamination. The test is conducted by putting the device into a special test mode whereby 7.0 volts is applied to all poly 2 structures with source, drain and substrate held at ground. The test is conducted at +150°C and is normally conducted for 1,000 hours with readouts at 24, 168, 500 and 1,000 hours.

Retention Bake

The Retention Bake Test is performed to accelerate data loss on floating gate devices. The test consists of unbiased baking at elevated temperature. Usually the test lasts for 1,000 hours at +150°C. The failure mechanism that is accelerated is charge leakage from a stored element.

Endurance Cycling

Endurance Cycling establishes the number of times a device can be programmed and erased. Normally the test is conducted at rated temperature conditions and is followed by a retention bake.

Temperature Cycle

The Temperature Cycle test simulates stresses which occur to systems during power up/power down sequences. The test is intended to reveal any deficiencies resulting from thermal expansion mismatch of the die/package structure. Normally the test is conducted by cycling between -65°C and +150°C in an air ambient. Duration for the test is typically 500 cycles for both plastic and ceramic packages. Endpoint criteria are both electrical and visual/mechanical.

Thermal Shock

The Thermal Shock test is similar to the Temperature Cycle test except that the ambient during cycling is liquid-to-liquid. This stimulates rapid thermal environmental changes. The mechanisms accelerated are identical to those in the Temperature Cycle test except that the Thermal Shock test is a more accelerated test with temperatures normally +125°C to -55°C. The number of cycles are 500 for qualification testing.

Autoclave

The autoclave test determines the survivability of devices in molded plastic packages to a hot, humid environment. The test exposes unbiased, plastic packaged devices to saturated steam at 121°C and 15 pounds per square inch (one atmosphere) gauge pressure. The 168 or more hours of testing allows moisture to penetrate to the die surface. Chemical corrosion of the die metallization may occur if ionic contaminants are present and the die surface protection is deficient or damaged. Charge leaks from floating devices usually happen before a corrosion mechanism develops.

RELIABILITY TESTS (CONT.)

Temperature Humidity Test

The Temperature Humidity test determines the survivability of devices in molded plastic packages functioning in a hot, humid environment. By convention, test conditions are 85°C with 85% relative humidity. The parts are biased to lend themselves to electrochemical corrosion. The duration of the test is usually 1,000 hours or more. The test checks the adequacy of the die surface protection and the plastic's lack of ionic impurities. The applied bias may be 5 volts on alternating pins or set up for minimum power to reduce internal heating and consequent moisture evaporation on the device. Similar to the Autoclave test, charge loss on floating gate devices is a principle failure mechanism.

QUALIFICATION CATEGORIES

Qualification is required for new design, major changes in old design, process or material when either wafer fabrication or package assembly operations are affected. Qualification applies to the following changes:

I. New technology

II. Start-up of Fab or Assembly

III. Transfer of fab or assembly to another location

IV. Major process changes:

- A. Process scaling (shrink conversion)
- B. Change in vendor or material source
- C. New equipment that affects reliability

V. New device configurations:

- A. New structures
- B. New packaging material
- C. Design rule changes
- D. Existing package revision (dimensional or layout)

QUALIFICATION PROGRAMS

Qualifications guarantee changes to or new processes and technologies are properly evaluated for reliability performance.

Reliability Monitoring

Microchip's reliability monitoring program is a comprehensive effort to measure the reliability of all process families with strict regularity. The program strives to improve performance through failure analysis and corrective action. Numerous screening procedures are used and estimates of product life and expected failure rates are provided.

Typical tests and frequencies include:

- Quarterly Die Monitor on selected product for -
  - Dynamic Life
  - Retention Bake
  - Endurance
  - HTRB
- Periodic (weekly, monthly and quarterly) package monitors to evaluate:
  - Mechanical stresses
  - Alignment
  - Temperature and moisture stresses
  - Corrosion resistance
  - Marking permanency

7

APPENDIX A - IN LINE CONTROLS

CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced
			Quality	Prod	MIL-STD
Die Visual	Reject defectives 100% rescreen per LTPD	10% sample LTPD 10	- X	X -	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One slice per lot	X	-	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	4X/Lot/Machine LTPD 15	X	-	N/A
Wire Bond	Machine Shut Down	1% AQL each 1/2 shift	X	-	MIL-STD-883C Method 2010
Post Wire Bond	Reject defectives 100% rescreen per LTPD	LTPD 15	X	-	MIL-STD-883C Method 2010
Mold Press	Machine Shut Down	One sample /4 hrs	X	-	N/A
Die Plating	Reject defectives 100% rescreen per LTPD	Every 4 hrs LTPD 10	X	-	N/A
Trim and Form	Reject defectives 100% rescreen per LTPD	Once/ 2 hrs LTPD 10	X	-	N/A
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	- X	X -	MIL-STD-883C Method 2010, Method 2016

CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced
			Quality	Prod	MIL-STD
Die Visual	Reject defectives 100% rescreen per LTPD	10% LTPD 10	- X	X -	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One slice per lot	X	-	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	Non-destruct each 2 hrs destruct each shift	X	-	MIL-STD-883C Method 2010
Wire Bond	Machine Shut Down	4X/shift/machine	X	-	MIL-STD-883C Method 2010
Preseal Visual	Reject defectives 100% rescreen per LTPD	100% LTPD 15	- X	X -	MIL-STD-883C Method 2010
Package Seal	Machine Shut Down	LTPD 15	X	-	N/A
Environmental Stress Centrifuge Temp Cycle	Machine Shut Down	LTPD 5 84(0) 84(0)	X	-	MIL-STD-883C Method 2001 Method 1010
Fine Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	-	MIL-STD-883C Method 1014
Gross Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	-	MIL-STD-883C Method 1014
Lead Trim	Reject defectives 100% rescreen per LTPD	100% LTPD 2	- X	X -	MIL-STD-883C Method 2009
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	- X	X -	MIL-STD-883C Method 2010, Method 2016

7

APPENDIX B - MATERIAL CONTROLS PACKAGE

MATERIALS CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced
			Quality	Prod	MIL-STD
Lead Frame	Reject defectives 100% rescreen per LTPD	Visual, LTPD 2 Functional, LTPD 10 and material spec	X	-	N/A
Die Attach Epoxy	Reject	Functional, LTPD 15 and material spec	X	-	N/A
Gold Wire	Reject	Per material spec	X	-	N/A
Molding Compound	Reject	Spiral flow, 3X/lot Functional, 1X/lot and material spec	X	-	N/A

MATERIALS CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced
			Quality	Prod	MIL-STD
Base/Lead Frame	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	-	MIL-M-38510
Package	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 Plating, LTPD 10 and material spec	X	-	MIL-M-38510
Preform	Reject	Visual, LTPD 10 Functional, LTPD 15	X	-	MIL-M-38510
Bond Wire	Reject	Per material spec 2 spools/lot	X	-	MIL-M-38510
Lid	Reject	Visual, LTPD 7 Functional, LTPD 10 and material spec	X	-	MIL-M-38510

Microchip

Plastic Package Reliability

OVERVIEW

Microchip Technology Plastic products provide competitive leadership in quality and reliability, with demonstrated performance of less than 250 FITs (Failures in Time) operating life. The designed-in reliability of Microchip Technology Plastic package products are supported by ongoing reliability data monitors. This document presents current data for your use - to provide you with results you can count on.

The test descriptions included in this document explain Microchip Technology's quality and reliability system, and the product data demonstrate its results.

The customer's quality requirements are Microchip Technology's top priority: Ongoing customer feedback and device performance monitoring drive Microchip Technology's manufacturing and design process, leading to continuing improvements in the long-term quality and reliability.

PRODUCT SCOPE

The subjects of this Product Reliability Bulletin are the Plastic Packages of Microchip Technology's Product Families: Microcontrollers, Serial and Parallel EEPROMs and EPROMs.

RELIABILITY DATA

Microchip Technology's products in plastic packages were produced to offer the customer the flexibility of using plastic devices as a direct substitution for ceramic package products. Failure Rate Predictions/Operating Life data for plastic package products at 125°C prove to be equivalent to the data of ceramic, opening the way for package substitution for cost savings.

FAILURE RATE CALCULATION

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip Technology agree closely with those published in the literature. For complex CMOS devices in production at Microchip Technology, an activation energy of 0.6 eV has been shown to be most representative of typical failures on operating life. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

The plastic product families have an early failure rate (infant mortality) of less than .04%/1,000 hrs. and thus, a production burn-in should not be necessary. For all products shown, the early life failure rates are reported separate from long term life.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink, or air flow by convection is used.

Plastic Package Reliability

Environment	Typical Failure Mechanism
Operating Life	Process parameter drift/shift Metal electromigration Internal leakage path Lifted bond/ball bond chip-out
Temperature Cycle	Lifted bond/ball chip-out Cracked die or surface cracks Bond pad corrosion
Biased-Humidity	Internal circuit corrosion
Autoclave	Inter-pin leakage Charge loss
High Temp. Bake	Charge loss
High Temp. Reverse Bias	Charge gain, Parameter drift/shift

DEFINITIONS

FIT (Failure In Time): Expresses the estimated field failure rate in number of failures per billion power-on device-hours. 100 FITS equals 0.01% fail per 1,000 device-hours.

Operating Life Test: The device is dynamically exercised at a high ambient temperature (usually 125°C) to quickly simulate field life. Derating from high temperature, an ambient use condition failure rate can be calculated.

Temperature Cycle: The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 15 minutes, 150°C for 15 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

Biased-Humidity: Moisture and bias are used to accelerate corrosion-type failures in plastic packages. The conditions include 85°C ambient temperature with 85% relative humidity. Typical bias voltage is +5 volts and ground on alternating pins.

Autoclave (pressure cooker): Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Thermal Shock: Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media.

Retention Bake: A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM.

High Temperature Reverse Bias (HTRB): A special test mode which subjects the entire EPROM array to a high gate voltage with drain, source and substrate grounded. It is used to measure charge gain and/or threshold shifts.

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system ensures that released products are designed, processed, packaged and tested to meet both design functionality and strict reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability.

DESIGN AND DEVELOPMENT → QUALIFICATION → RELIABILITY CONTROL

Specify:
- Design objectives/specifications
- Testability goals
- Reliability requirements
- Process/packaging requirements
- Design guidelines

Design:
- Functional models
- Logic design & verification
- Circuit design & verification
- Layout design & verification
- Prototype verification
- Performance characterization

Develop (as required):
- Wafer fabrication processes
- Package/packaging technology

Confirm design objectives using qualification tests:
- Operating life, 125°C ambient
- Temp-cycle, -65°/150°C
- Thermal shock, -65°/150°C
- ESD resistance, ± 2000 V
- Latch-up (CMOS devices)
- Biased-humidity, 85°C/85%
- Autoclave (pressure cooker) retention bake
- HTRB

Assure Outgoing Quality Level:
- Design release document
- Baseline wafer fabrication process
- Baseline assembly process
- Qualification release
- Enter device to specification system
- Wafer-level reliability controls
- Assembly reliability controls
- Early failure rate sampling
- Reliability monitoring
- Statistical process control feedback
- Audit specifications
- Analyze returned failures
- Requalify devices as needed for major changes such as ESD resistance enhancement, cost reduction/die shrink, process improvement, and new package types.

RELIABILITY DATA SUMMARY

Introduction

This section provides a reliability summary of Microchip Technology's plastic product. Included is plastic packaging information and reliability data obtained to date for all product families.

Plastic Package Characteristics

Plastic packaging utilized for the product families uses a silver filled epoxy adhesive for die attach. Bonding technology is gold wire thermosonic bonding. The lead frame pedestal and finger tips are silver plated. The epoxy molding compound used is a Shinetsu compound KMC-140-3 which meets the safety rating requirements of UL94 V-O. External lead finish is electroplated tin/lead 90/10 percent. The package code table below lists the plastic packages covered by the reliability data in this document.

As part of an on going product improvement program, Microchip Technology will apply its Quality and Reliability process in evaluating the latest developments in plastic packaging technology, and implement the highest reliability materials and assembly techniques.

PLASTIC PACKAGE IDENTIFICATION CODES

Package Description	Identification Code
Plastic Leadless Chip Carrier	L
Plastic Dual In Line (600)	P
Plastic Dual In Line (300)	SP
Plastic SOIC (.150)	SL/SN
Plastic SOIC (.207)	SM
Plastic SOIC (.300)	SO
Plastic TSOP (8 x 20mm)	TS

ELECTRICAL CHARACTERISTICS

Microchip Technology's product packaged in plastic are tested to the same electrical characteristics as devices assembled in Cerdip packages. This testing covers the full commercial range of 0-70°C. Performance characteristics are the same as for Cerdip packaging.

QUALITY/RELIABILITY TESTING RESULTS

Reliability and programming tests were performed on all devices in plastic packages. Data from these qualification tests are displayed throughout this document.

PROGRAMMABILITY

Programmability is measured by sample data taken from production lots. Devices are programmed with a Diagonal FF which exercises 98% of the EPROM cell array. This rigorous patterning combined with Microchip Technology Express programming algorithm greatly enhances the ability to meet specific customer applications. Large volume beta site programming results for plastic EPROMs indicate an expected yield far exceeding 99%, using Express programming, under normal production conditions.

PROGRAMMABILITY DATA (12 MONTH PERIOD)

Time Period	No. of Sample Units	No. of Non-Programmable Units	Fraction Defective
1989	10019	258	.026
1990	26025	326	.013

Note: Derated to typical customer programming, the defective fraction should be 0.006.

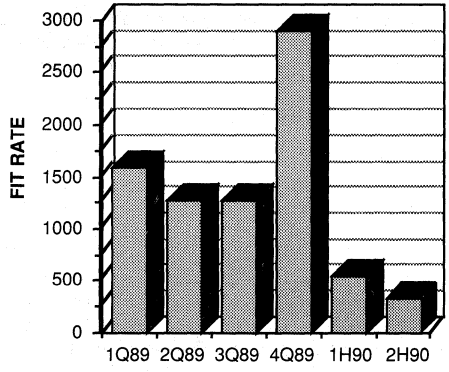
7

HIGH TEMPERATURE (125°C) DYNAMIC LIFE TEST

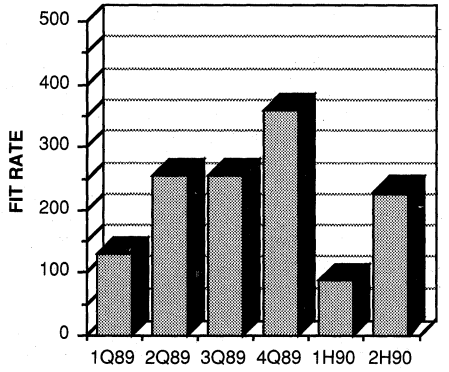
Graph set for EEPROM, PIC and EPROM for all conditions

High temperature dynamic life testing accelerates random failure modes which would occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems.

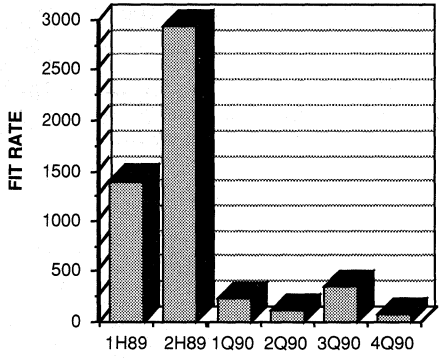
EEPROM DYNAMIC LIFE
INFANT MORTALITY



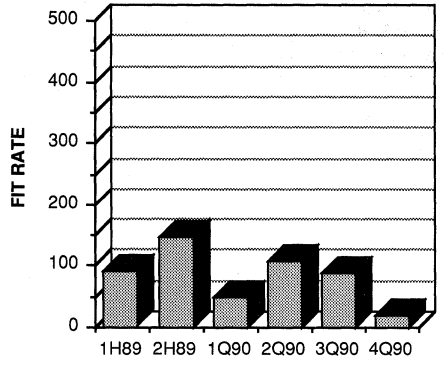
EEPROM DYNAMIC LIFE
LONG TERM MORTALITY



CMOS PIC DYNAMIC LIFE
INFANT MORTALITY



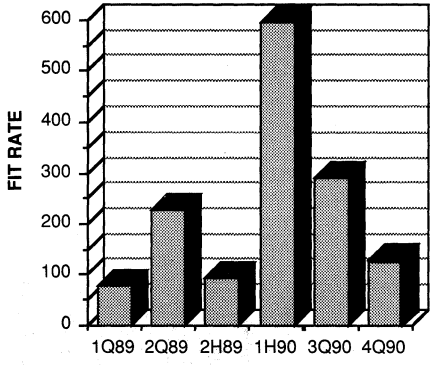
CMOS PIC DYNAMIC LIFE
LONG TERM MORTALITY



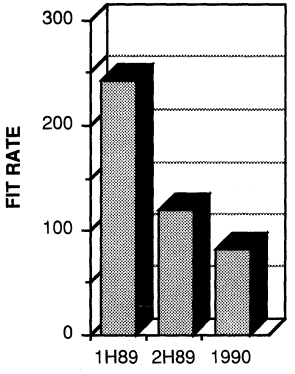
HIGH TEMPERATURE REVERSE BIAS (150°C/7 VOLTS)

Microchip Technology Inc.'s applicable products are designed for enhanced reliability by having a special test mode which allows all gates on the array to be simultaneously placed at a high voltage stress level in reference to the rest of the circuitry. This test is used to create a high voltage stress on the memory oxide. An additional acceleration of three times is gained from a higher than industry standard 7V level. This is calculated into the failure rates below. Failures which will be detected with this type of stress are: pin holes in the oxide, thin oxide layers, and charge gain failures.

CMOS PIC HTRB
INFANT MORTALITY



CMOS PIC HTRB
LONG TERM MORTALITY



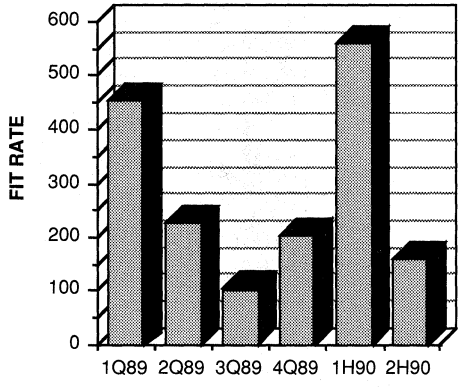
7

DATA RETENTION BAKE

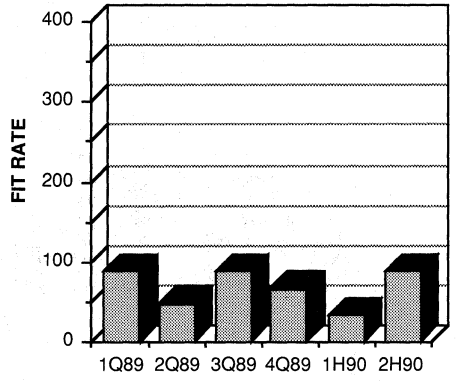
Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in loss of data. In order to detect this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell.

This added screen for detecting infant mortality charge allows Microchip Technology Inc.'s plastic product to duplicate the excellent data retention characteristics of the ceramic packages.

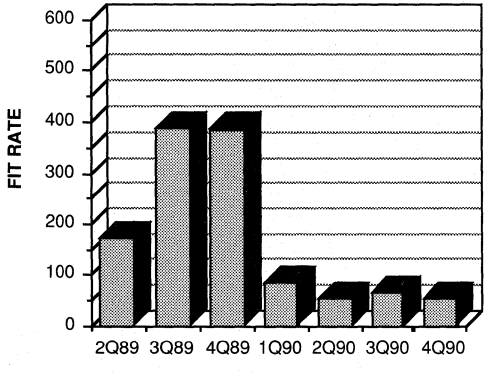
EEPROM RETENTION BAKE INFANT MORTALITY



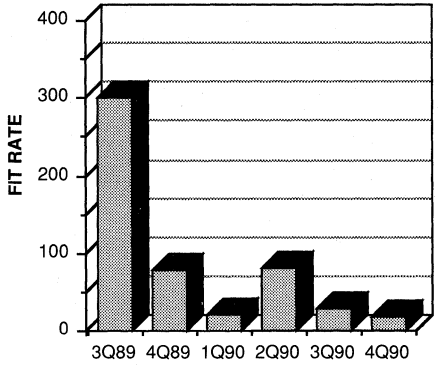
EEPROM RETENTION BAKE LONG TERM MORTALITY



CMOS PIC RETENTION BAKE INFANT MORTALITY



CMOS PIC RETENTION BAKE LONG TERM MORTALITY



Note:

Representation of reliability data typically shows calendar quarter grouping along the x-axis. This provides the equal time interval normally expected for graphical presentation. However, Chi-square statistics demand equivalent device-hours for fair interval comparison. Such data grouping assures that relatively small sample sizes do not indicate unrepresentative FIT rates. When both conditions cannot easily be met, equivalent device hours typically are chosen. For this reason, half and full year time intervals are occasionally included in addition to our standard use of calendar quarters. Even so, all peaks shown in the trend data are results of low device hours.

PRODUCT RELIABILITY DATA

CMOS PIC								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	60% CL @ 55°C
16C57	DLT	0/358	1/358	0/305	-	1	162624	297
16C56	DLT	0/205	0/205	0/153	0/153	0	162960	134
16C55	DLT	4/2464	7/2460	0/1642	2/1009	13	1473624	237
16C54	DLT	2/3001	3/2999	0/2366	1/1416	6	2012520	87
16C57	HTRB	0/55	0/52	-	-	0	8808	294
16C56	HTRB	0/166	2/166	2/164	1/162	5	164640	108
16C55	HTRB	0/914	13/914	5/491	1/125	19	381528	153
16C54	HTRB	6/689	3/683	3/225	-	12	190488	202
16C57	BAKE	0/52	0/52	-	-	0	8736	890
16C56	BAKE	0/189	0/189	0/189	-	0	95256	82
16C55	BAKE	0/2178	0/2178	0/931	0/81	2	719544	37
16C54	BAKE	0/2054	1/2054	0/1616	2/135	3	1056888	34
EEPROM								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	60% CL @ 55°C
24C01/02	DLT	1/1305	2/1304	0/394	0/394	3	550056	181
24C04	DLT	0/854	6/854	1/256	0/255	7	358008	560
93C46/59C11	DLT	0/897	0/897	0/225	0/225	0	339696	64
24C01/02	BAKE	0/442	1/442	0/306	0/229	1	292488	59
24C04	BAKE	4/305	2/301	0/154	0/154	6	180024	347
93C46/59C11	BAKE	0/540	0/540	0/225	0/225	0	279720	28
EPROM								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	60% CL @ 55°C
27C64	DLT	0/1354	3/1354	0/339	0/261	3	496,524	202
27C128	DLT	1/2203	3/2202	0/392	1/315	5	659,400	229
27C256	DLT	0/4966	17/4966	1/1615	1/1570	19	2,189,604	228
27C512	DLT	2/2801	11/2799	3/991	3/684	19	1,143,576	437
27C64	HTRB	0/1175	4/1175	0/135	1/135	5	309624	58
27C128	HTRB	4/2236	11/2232	1/390	2/389	18	698,880	80
27C256	HTRB	3/3981	29/3978	2/764	2/762	36	1,302,504	83
27C512	HTRB	1/1667	17/1666	3/684	2/605	23	809,760	87
27C64	BAKE	0/863	3/863	0/135	1/135	4	567,912	78
27C128	BAKE	4/1664	5/1660	1/390	2/389	12	1,220,580	95
27C256	BAKE	29/6853	16/3076	1/687	2/686	48	2,331,504	184
27C512	BAKE	9/2706	8/1371	2/673	4/455	23	1,278,156	166

Operation Legend: DLT - Dynamic Life Test
Bake - Retention Bake
HTRB - High Temperature Reverse Bias

Notes:

SECTION 8
PACKAGING

COMMERCIAL AND INDUSTRIAL PARTS

Part Number Suffix Designations:

XXXXXXXXXX - XX X / XX XXX

ROM Code or Special Requirements

Case Outline

D	=	Ceramic Side Brazed Dual In-Line
J	=	Cerdip (with window if EPROM) - all product except Microcontrollers
JL	=	Ceramic Leaded Chip Carrier (CLCC)
JN	=	Cerdip, no window
JW	=	Cerdip, windowed - for Microcontrollers only
K	=	LCC (Ceramic Leadless Chip Carrier)
L	=	PLCC (Plastic Leaded Chip Carrier)
P	=	Plastic Dual In-Line
PQ	=	Metric Quad Flat Pack Plastic
PT	=	Thin Quad Flat Pack Plastic
S	=	Die in Waffle Pack
SF	=	Sawn Probed Wafer on Film
SJ	=	Skinny Cerdip
SL	=	14-Lead Small Outline Narrow Plastic Gull Wing (150 mil Body)
SM	=	Small Outline Medium Plastic Gull Wing (207 mil Body)
SN	=	8-Lead Small Outline Narrow Plastic Gull Wing (150 mil Body)
SO	=	Small Outline Wide Plastic Gull Wing (300 mil Body)
SP	=	Skinny Plastic Dual In-Line
SS	=	Shrink Small Outline Plastic (5.3mm .208 Body)
ST	=	Thin Shrink Small Outline Plastic
SW	=	Small Outline Large Plastic Gull Wing (330 mil Body)
TS	=	Thin Small Outline Plastic Gull Wing Type I (8 x 20mm)
W	=	Die in Wafer Form

Process Temperature

Blank	=	0°C to +70°C
I	=	-40°C to +85°C
H	=	-40°C to +110°C
E	=	-40°C to +125°C

Speed (EPROM / High Density EEPROM)		**Frequency** (DSP)		**Crystal Designation** (PIC16C5X)	
-55	= 55 ns	Blank	= 20.5 MHz	LP	= 4 µs
-70	= 70 ns	-14	= 14.4 MHz	RC	= 1 µs
-90	= 90 ns	-25	= 25.6 MHz	XT	= 1 µs
-10	= 100 ns	-32	= 32.8 MHz	-10	= 400 ns
-12	= 120 ns			HS	= 200 ns
-15	= 150 ns	(PIC16CX)			
-17	= 170 ns	-04	= 4 MHz		
-20	= 200 ns	-16	= 16 MHz		
-25	= 250 ns	-20	= 20 MHz		

Device Type (Up To 10 Digits)

8

TABLE OF CONTENTS

SECTION 1: HERMETIC

8

TABLE OF CONTENTS (Cont'd)

SECTION 2: PLASTIC

8

Packaging Diagrams and Parameters

Ceramic Side Brazed Dual In-line Family

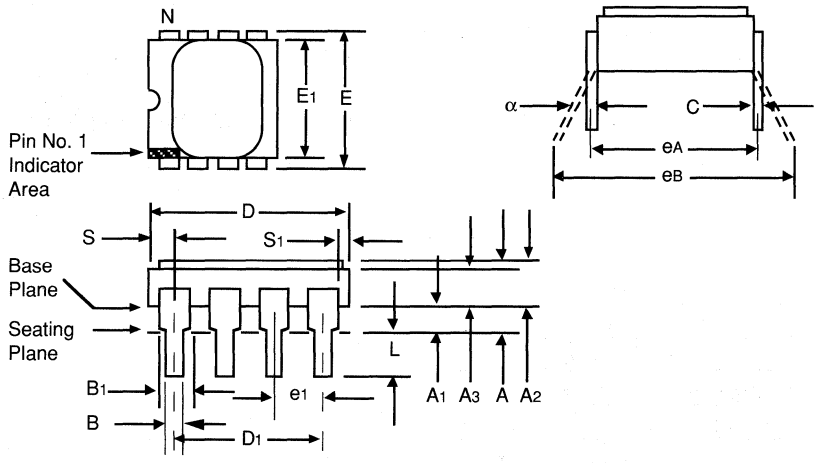
Symbol List for Ceramic Side Brazed Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_1	Body width parameters not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially useable lead positions
S	Distance from true position center line of No. 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:
1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.

8

Packaging Diagrams and Parameters

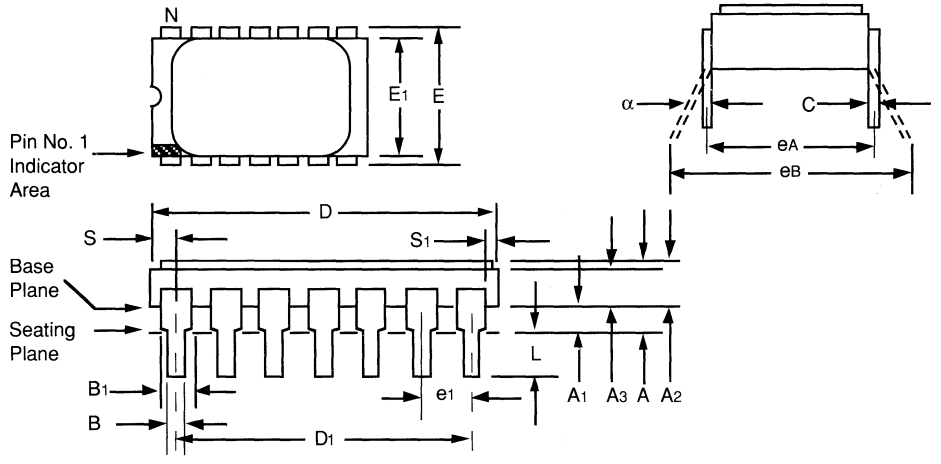
Package Type: 8-Lead Ceramic Side Brazed Dual In-line (.300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	3.937		0.130	0.155	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	**Typical**	0.054	0.054	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	13.0048	13.4112		0.512	0.528	
D1	7.4168	7.8232	**Reference**	0.292	0.308	**Reference**
E	7.5692	8.2296		0.298	0.324	
E1	7.112	7.620		0.280	0.300	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.620	9.652		0.300	0.380	
L	3.302	3.810		0.130	.150	
N	8	8		8	8	
S	2.540	3.048		0.100	0.120	
S1	0.127	–		.005	–	

Packaging Diagrams and Parameters

Package Type: 14-Lead Ceramic Side Brazed Dual In-line (.300 mil)

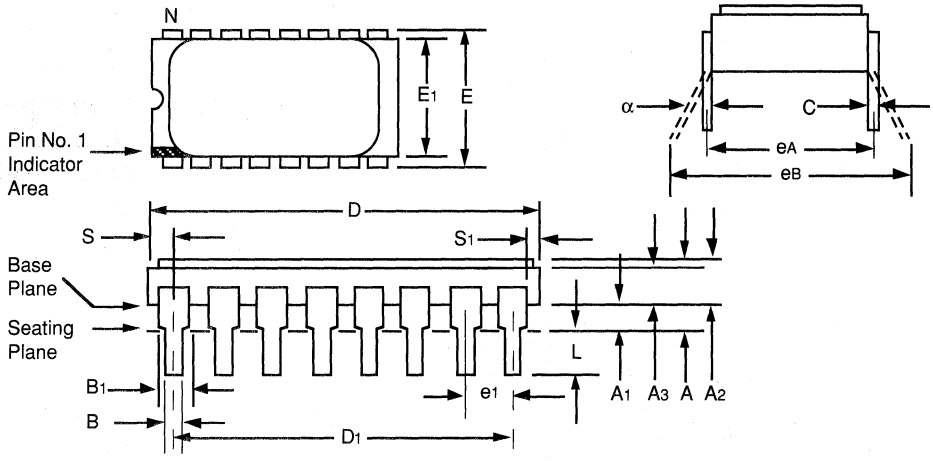


Package Group: Ceramic Side Brazed Dual In-line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.2032	0.3048	Typical	0.008	0.012	Typical
D	18.796	19.2278		0.740	0.757	
D1	15.0368	15.4432	Reference	0.592	0.608	Reference
E	7.620	8.382		0.300	0.330	
E1	7.0612	7.5692		0.278	0.298	
e1	2.3622	2.7432	Typical	0.093	0.108	Typical
eA	7.366	7.874	Reference	0.290	0.310	Reference
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	14	14		14	14	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

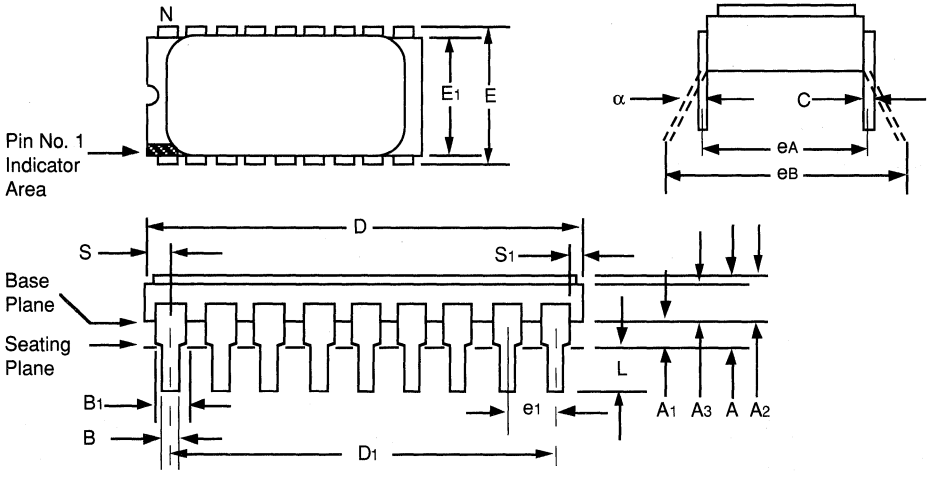
Package Type: 16-Lead Ceramic Side Brazed Dual In-line (.300 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	**Typical**	0.054	0.054	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	19.812	20.574		0.780	0.810	
D1	17.653	17.907	**Reference**	0.695	0.705	**Reference**
E	7.620	8.382		0.300	0.330	
E1	7.1628	7.4676		0.282	0.294	
e1	2.413	2.667	**Typical**	0.095	0.105	**Typical**
eA	7.366	7.874	**Reference**	0.290	0.310	**Reference**
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	16	16		16	16	
S	–	2.032		–	0.080	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 18-Lead Ceramic Side Brazed Dual In-line (.300 mil)

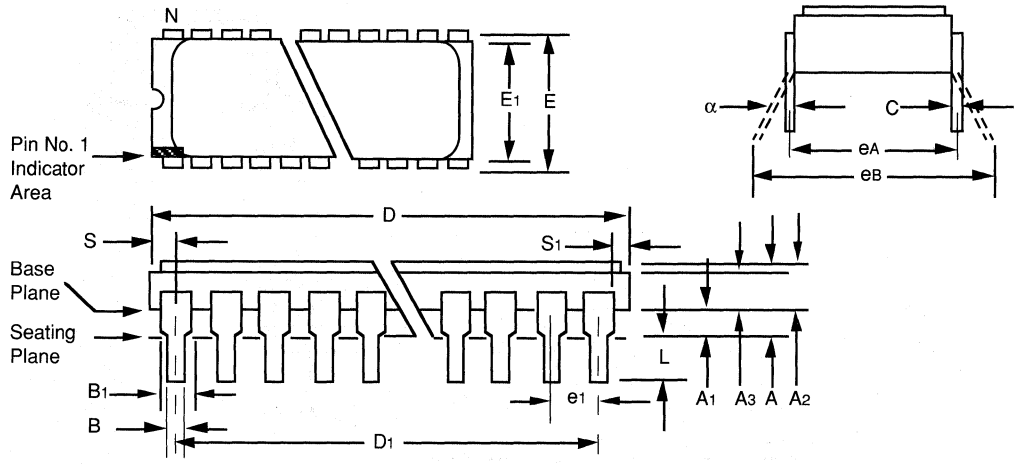


Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.4064	0.508		0.016	0.020	
B1	1.3716	1.3716	**Typical**	0.054	0.054	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	22.352	23.114		0.880	0.910	
D1	20.193	20.447	**Reference**	0.795	0.805	**Reference**
E	7.620	8.382		0.300	0.330	
E1	7.0612	7.5692		0.278	0.298	
e1	2.413	2.667	**Typical**	0.095	0.105	**Typical**
eA	7.366	7.874	**Reference**	0.290	0.310	**Reference**
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	18	18		18	18	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

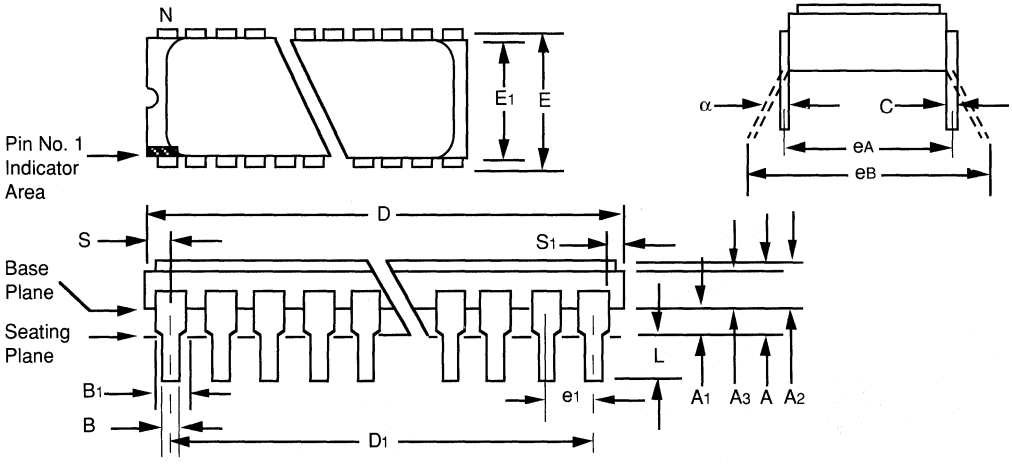
Package Type: 22-Lead Ceramic Side Brazed Dual In-line (.400 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.667	4.064		0.105	0.160	
A1	0.7112	1.2192		0.028	0.048	
A2	2.032	3.302		0.080	0.130	
A3	1.778	2.921		0.070	0.115	
B	0.4318	0.5842		0.017	0.023	
B1	1.016	1.016	**Typical**	0.040	0.040	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	27.1526	27.8638		1.069	1.091	
D1	25.2968	25.6032	**Reference**	0.992	1.008	**Reference**
E	10.160	10.922		0.400	0.430	
E1	9.7282	9.9822		0.383	0.393	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	9.906	10.414	**Reference**	0.390	0.410	**Reference**
eB	10.160	12.192		0.400	0.480	
L	3.175	4.191		0.125	0.165	
N	22	22		22	22	
S	–	2.032		–	0.080	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 24-Lead Ceramic Side Brazed Dual In-line (.600 mil)

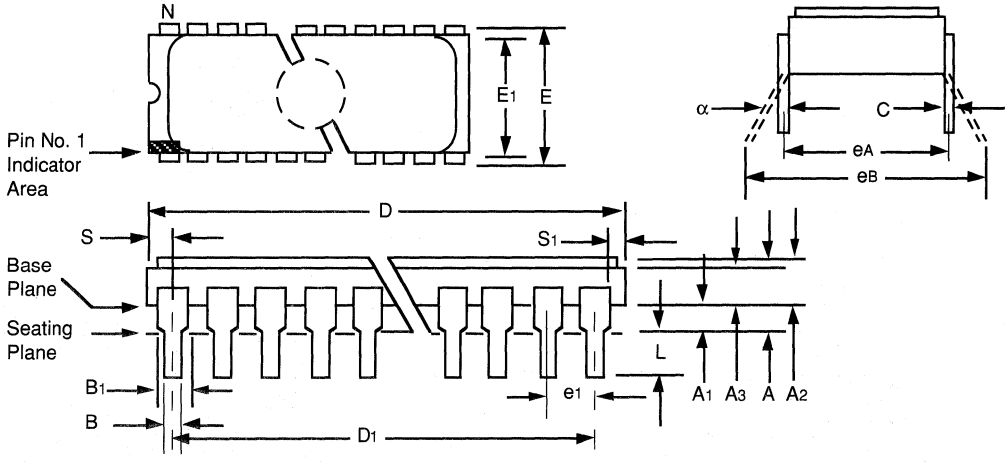


Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	30.1752	30.7848		1.188	1.212	
D1	27.7368	28.1432	**Reference**	1.092	1.108	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.7828	14.9352		0.582	0.588	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	14.986	15.748	**Reference**	0.590	0.620	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	24	24		24	24	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

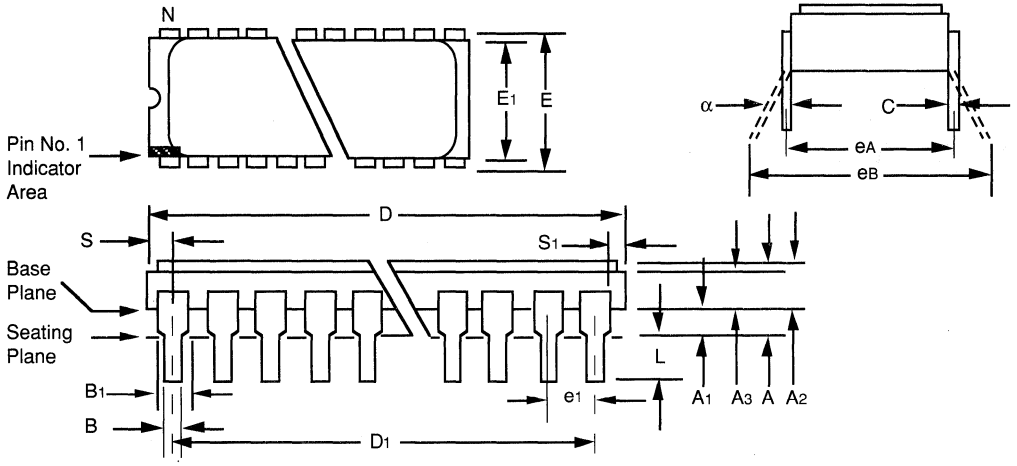
Package Type: 24-Lead Ceramic Side Brazed Dual In-line with Window (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	30.1752	30.7848		1.188	1.212	
D1	27.7368	28.1432	**Reference**	1.092	1.108	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.7828	14.9352		0.582	0.588	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	14.986	15.748	**Reference**	0.590	0.620	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	24	24		24	24	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Side Brazed Dual In-line (.600 mil)

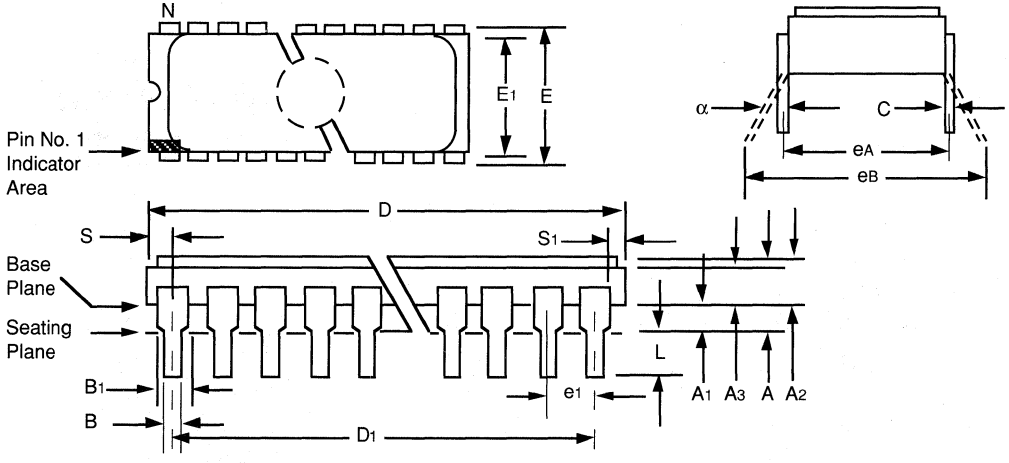


Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.064		0.120	0.160	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4572	0.508		0.018	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	35.2044	35.9156		1.386	1.414	
D1	32.8168	33.2232	**Reference**	1.292	1.308	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.7828	15.1892		0.582	0.598	
e1	2.4892	2.5908	**Typical**	0.098	0.102	**Typical**
eA	14.986	15.494	**Reference**	0.590	0.610	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

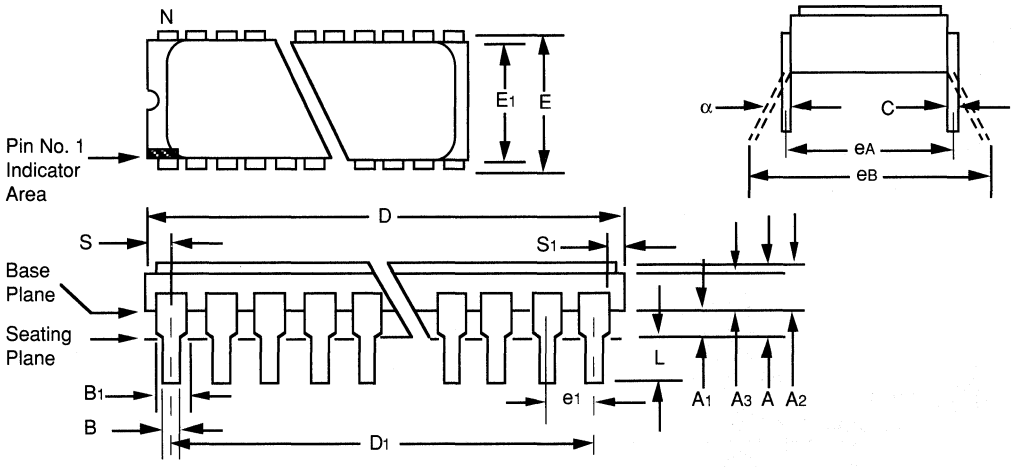
Package Type: 28-Lead Ceramic Side Brazed Dual In-line with Window (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.064		0.120	0.160	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.4572	0.508		0.018	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	35.2044	35.9156		1.386	1.414	
D1	32.8168	33.2232	**Reference**	1.292	1.308	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.7828	15.1892		0.582	0.598	
e1	2.4892	2.5908	**Typical**	0.098	0.102	**Typical**
eA	14.986	15.494	**Reference**	0.590	0.610	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 40-Lead Ceramic Side Brazed Dual In-line (.600 mil)

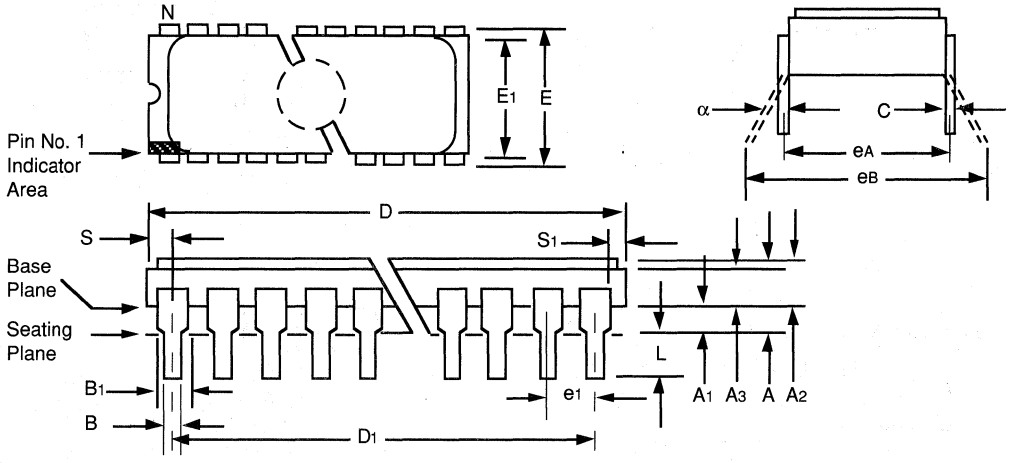


Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		.072	.088	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	50.546	51.308		1.990	2.020	
D1	48.056	48.463	**Reference**	1.892	1.908	**Reference**
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	40	40		40	40	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

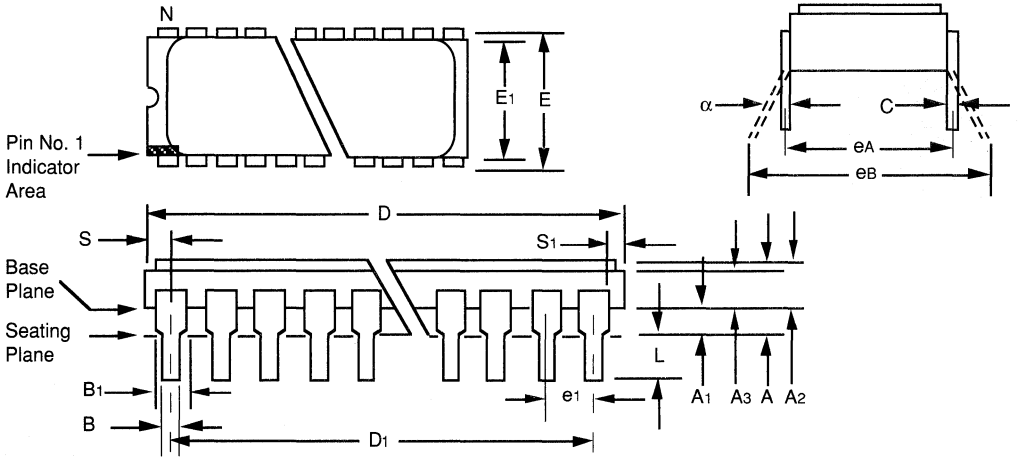
Package Type: 40-Lead Ceramic Side Brazed Dual In-line with Window (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		.072	.088	
B	0.4064	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	50.546	51.308		1.990	2.020	
D1	48.056	48.463	**Reference**	1.892	1.908	**Reference**
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	40	40		40	40	
S	–	2.4892		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 48-Lead Ceramic Side Brazed Dual In-line (.600 mil)



Package Group: Ceramic Side Brazed Dual In-line (CER)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A_1	1.016	1.524		0.040	0.060	
A_2	2.032	2.921		0.080	0.115	
A_3	1.829	2.235		0.072	0.088	
B	0.4064	0.508		0.016	0.020	
B_1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2286	0.3048	**Typical**	0.009	0.012	**Typical**
D	60.3504	61.5696		2.376	2.424	
D_1	58.2168	58.6232	**Reference**	2.292	2.308	**Reference**
E	15.240	16.256		0.600	0.640	
E_1	14.478	15.748		0.570	0.620	
e_1	2.3368	2.7432	**Typical**	0.092	0.108	**Typical**
e_A	15.240	15.290	**Reference**	0.600	0.600	**Reference**
e_B	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	48	48		48	48	
S	–	2.4892		–	0.100	
S_1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

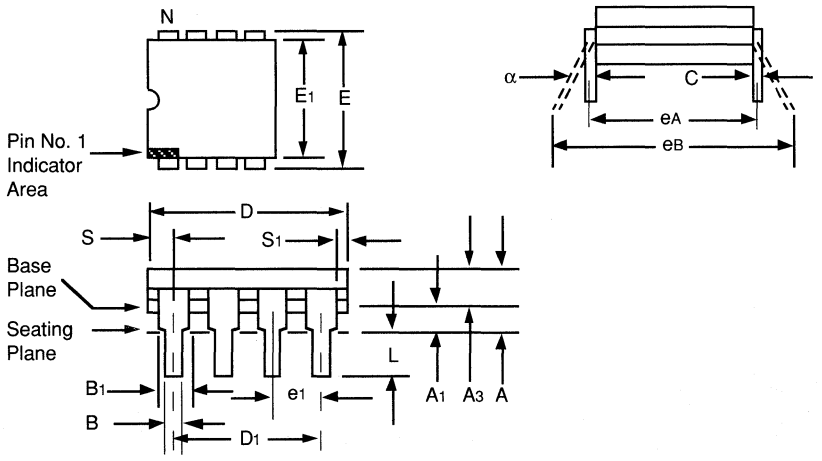
Ceramic Cerdip Dual In-line Family

Symbol List for Ceramic Cerdip Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body (lid)
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body (lid)
A_3	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_1	Body width parameters not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially useable lead positions
S	Distance from true position center line of No. 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:
1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.

Packaging Diagrams and Parameters

Package Type: 8-Lead Cerdip Dual In-line (.300 mil)

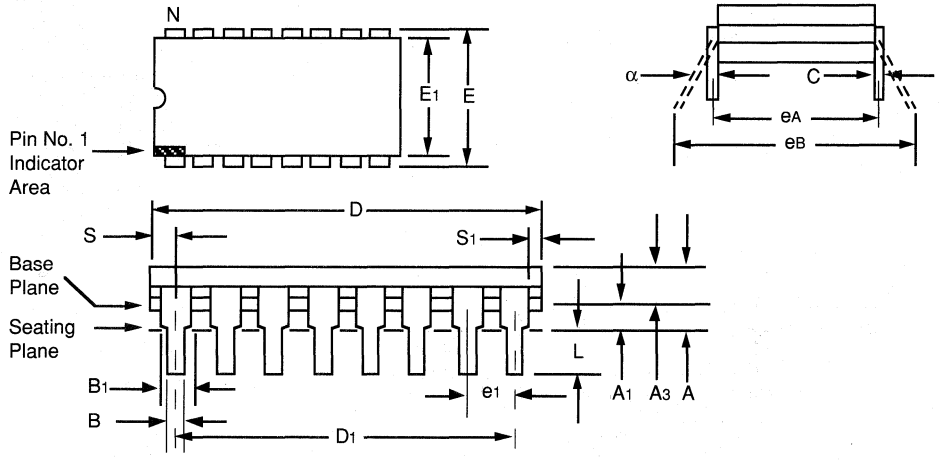


Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	9.398	10.287		0.370	0.405	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	7.620	8.255		0.300	0.325	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Referemce	0.290	0.320	Reference
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	8	8		8	8	
S	5.08	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

8

Packaging Diagrams and Parameters

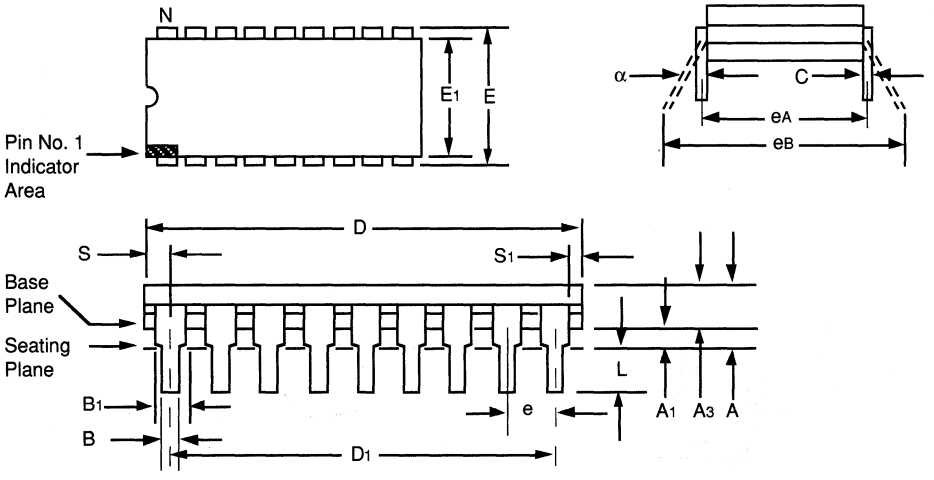
Package Type: 16-Lead Ceramic Cerdip Dual In-line (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.191	5.080		0.165	0.200	
A_1	0.381	1.524		0.015	0.060	
A_2	—	—	**Ref. A_3**	—	—	**Ref. A_3**
A_3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B_1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	19.050	20.320		0.750	0.800	
D_1	17.780	17.780	**Reference**	0.700	0.700	**Reference**
E	7.493	8.255		0.295	0.325	
E_1	5.588	7.874		0.220	0.310	
e_1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
e_A	7.366	8.128	**Reference**	0.290	0.320	**Reference**
e_B	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	16	16		16	16	
S	5.08	1.397		0.020	0.055	
S_1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

Package Type: 18-Lead Ceramic Cerdip Dual In-line (.300 mil)

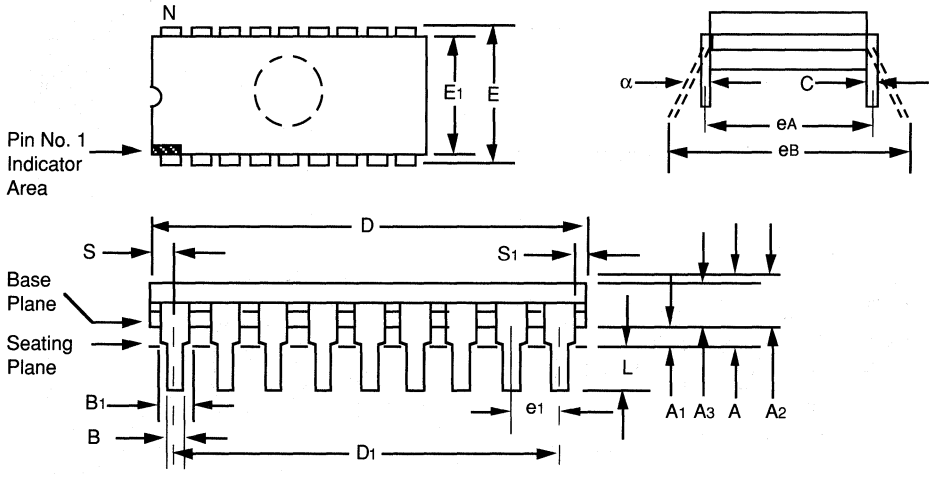


Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.524		0.015	0.070	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.180	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Reference	0.290	0.320	Reference
eB	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	5.08	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

8

Packaging Diagrams and Parameters

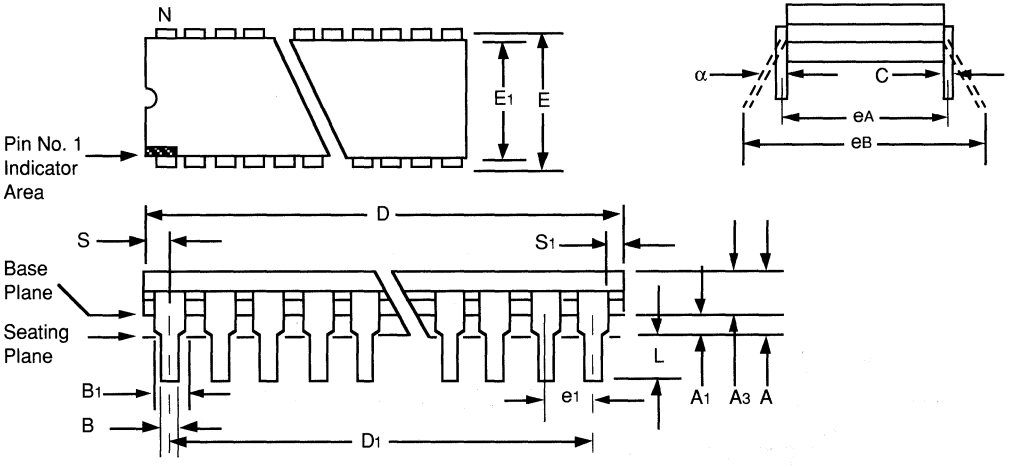
Package Type: 18-Lead Cerdip Dual In-line with Window (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.524		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.180	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	**Reference**	0.800	0.800	**Reference**
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	7.366	8.128	**Reference**	0.290	0.320	**Reference**
eB	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	5.08	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

Package Type: 22-Lead Ceramic Cerdip Dual In-line (.400 mil)

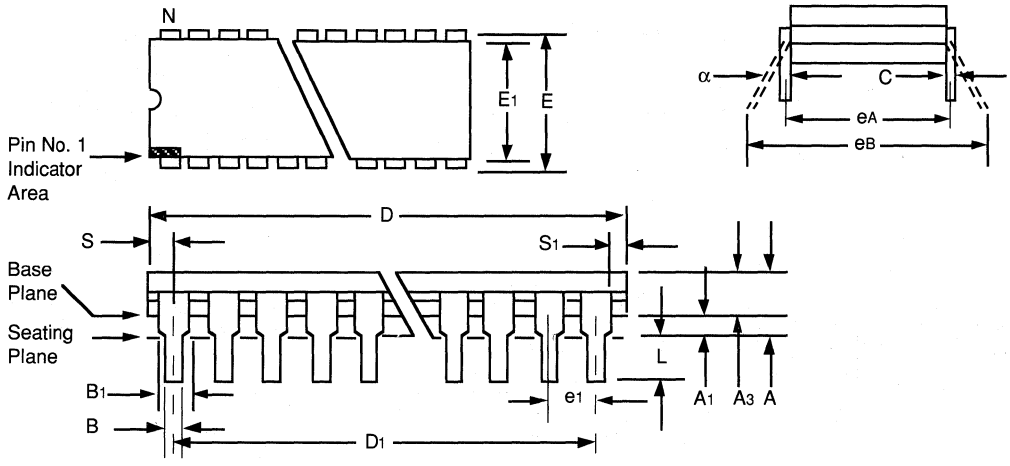


Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.524		0.015	0.070	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.180	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	26.670	27.940		1.050	1.100	
D1	25.400	25.400	Reference	1.000	1.000	Reference
E	10.160	10.922		0.400	0.430	
E1	8.890	10.414		0.350	0.410	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	9.906	10.668	Reference	0.390	0.420	Reference
eB	10.160	12.700		0.400	0.500	
L	3.175	3.810		0.125	0.150	
N	18	18		22	22	
S	—	1.270		—	0.050	
S1	0.127	1.270		0.005	0.050	

8

Packaging Diagrams and Parameters

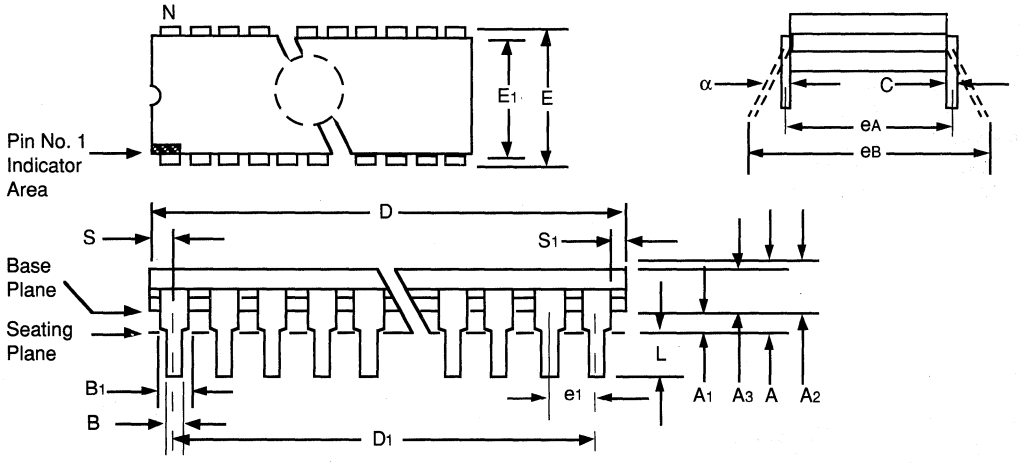
Package Type: 24-Lead Ceramic Cerdip Dual In-line (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.894		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Reference	0.290	0.320	Reference
eB	7.62	11.43		0.300	0.450	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

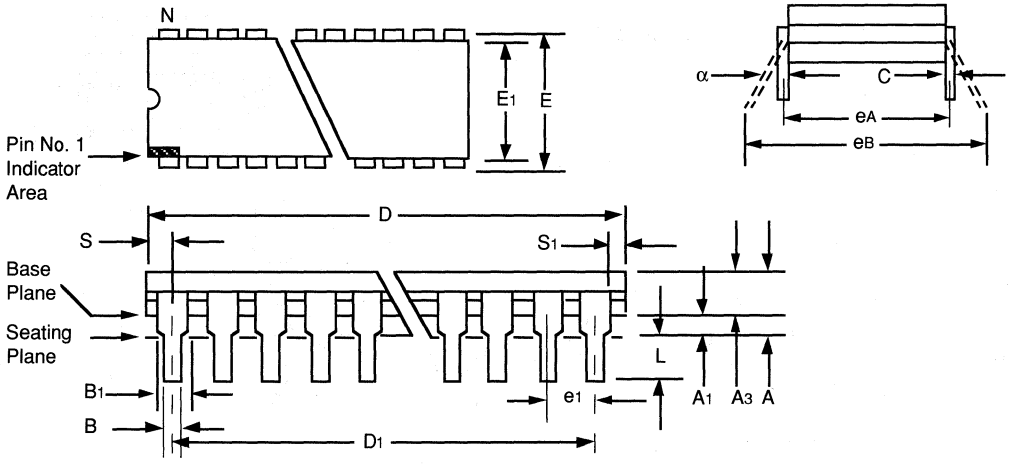
Package Type: 24-Lead Ceramic Cerdip Dual In-line with Window (.300 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	**Reference**	1.100	1.100	**Reference**
E	7.62	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	7.366	8.128	**Reference**	0.290	0.320	**Reference**
eB	7.62	11.43		0.300	0.450	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

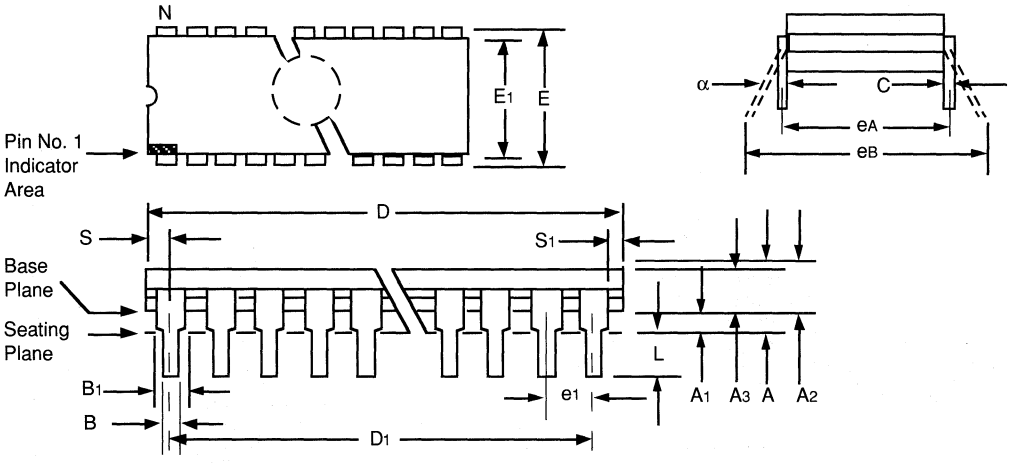
Package Type: 24-Lead Ceramic Cerdip Dual In-line (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.524		0.015	0.075	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	15.748	Reference	0.590	0.620	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.127	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Package Type: 24-Lead Ceramic Cerdip Dual In-line with Window (.600 mil)

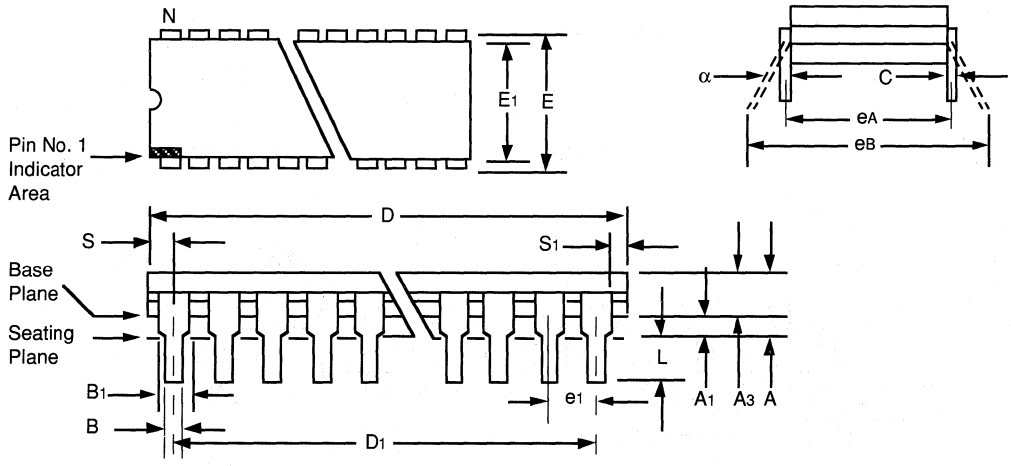


Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.524		0.015	0.075	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	**Reference**	1.100	1.100	**Reference**
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	14.986	15.748	**Reference**	0.590	0.620	**Reference**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.127	1.778		0.015	0.070	

8

Packaging Diagrams and Parameters

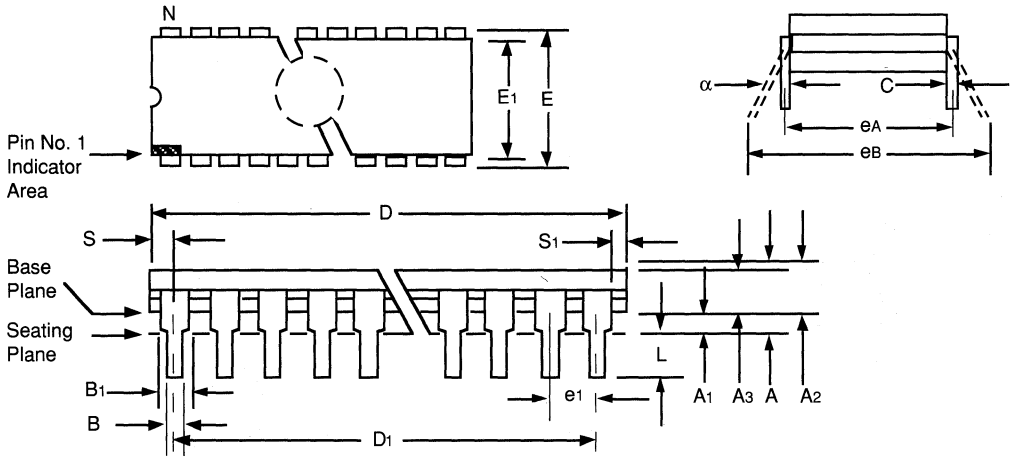
Package Type: 28-Lead Ceramic Cerdip Dual In-line (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	36.195	36.195		1.425	1.475	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	8.128	Reference	0.590	0.620	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	28	28		28	28	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Cerdip Dual In-line with Window (.600 mil)

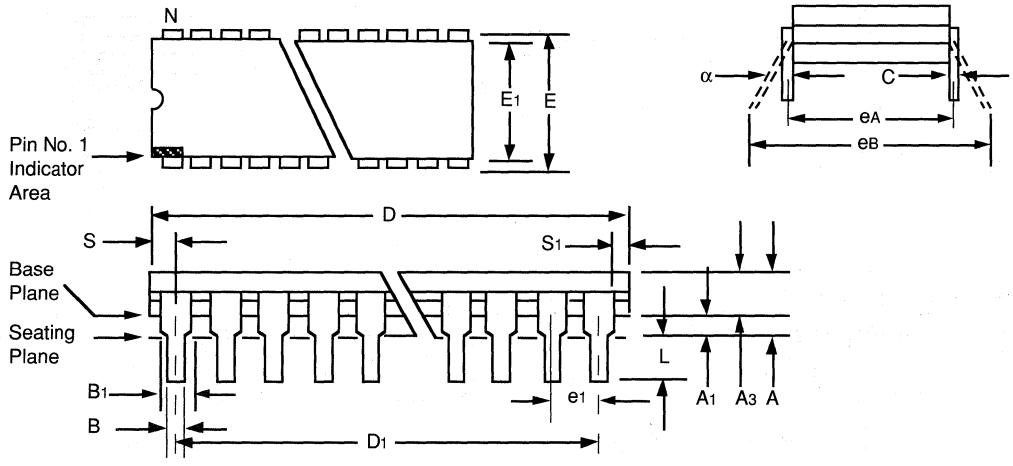


Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	36.195	36.195		1.425	1.475	
D1	33.020	33.020	**Reference**	1.300	1.300	**Reference**
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	14.986	8.128	**Reference**	0.590	0.620	**Reference**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	28	28		28	28	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

8

Packaging Diagrams and Parameters

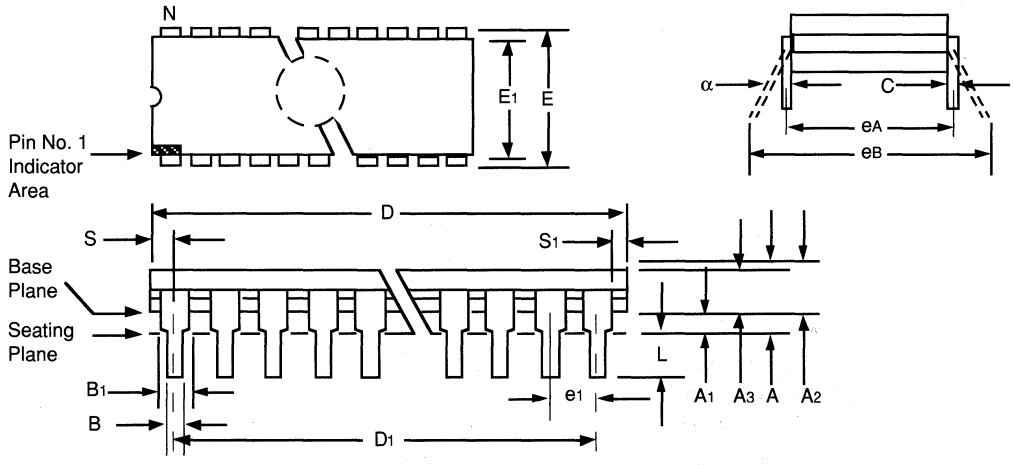
Package Type: 40-Lead Ceramic Cerdip Dual In-line (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	–	–	Ref. A3	–	–	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	16.002	Reference	0.590	0.630	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Package Type: 40-Lead Ceramic Cerdip Dual In-line with Window (.600 mil)



Package Group: Ceramic Cerdip Dual In-line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699	**Ref. A3**	0.150	0.185	**Ref. A3**
A3	3.810	4.445		0.150	0.175	
B	0.356	0.584		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	**Reference**	1.900	1.900	**Reference**
E	15.240	15875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	14.986	16.002	**Reference**	0.590	0.630	**Reference**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

8

Packaging Diagrams and Parameters

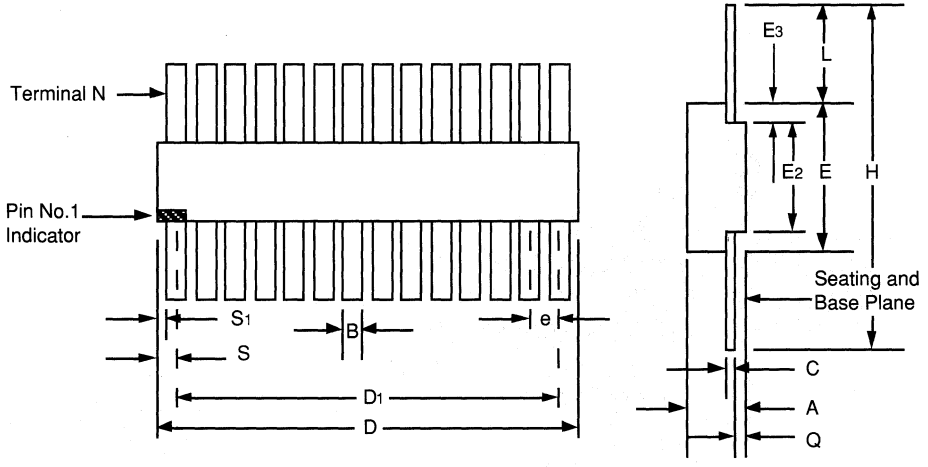
Ceramic Flatpack Family

Symbol List for Ceramic Flatpack Package Parameters	
Symbol	**Description of Parameters**
A	Distance between seating plane to highest point of body (lid)
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_2, E_3	Body width parameters not including leads
e	Linear spacing between center lines of body standoffs (terminal leads)
H	Other package width parameter
L	Distance from package body to end of lead
N	Total number of potentially useable lead positions
Q	Distance between seating plane and lead
S	Distance from true position center line of No. 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:
1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameters "B" and "C" are nominal.

Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Flatpack



Package Group: Ceramic Flatpack (CFPK)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.286	3.302		0.090	0.130	
B	0.381	0.4826		0.015	0.019	Typical
C	0.0762	0.1524		0.003	0.006	Typical
D	17.780	18.796		0.700	0.740	
D1	16.307	16.713		0.642	0.658	Reference
E	9.652	10.668		0.380	0.420	
E2	9.756	–		0.180	–	
E3	0.762	–		0.030	–	
e	1.270	1.270	BSC	0.050	0.050	Typical
H	22.352	29.464		0.880	1.160	
L	6.350	9.398		0.250	0.370	
N	28	28		28	28	
Q	0.660	1.143		0.026	0.045	
S	0.889	1.016		0.035	0.040	
S1	0.254	0.381		0.010	0.015	

Packaging Diagrams and Parameters

Ceramic Leadless Chip Carrier Family

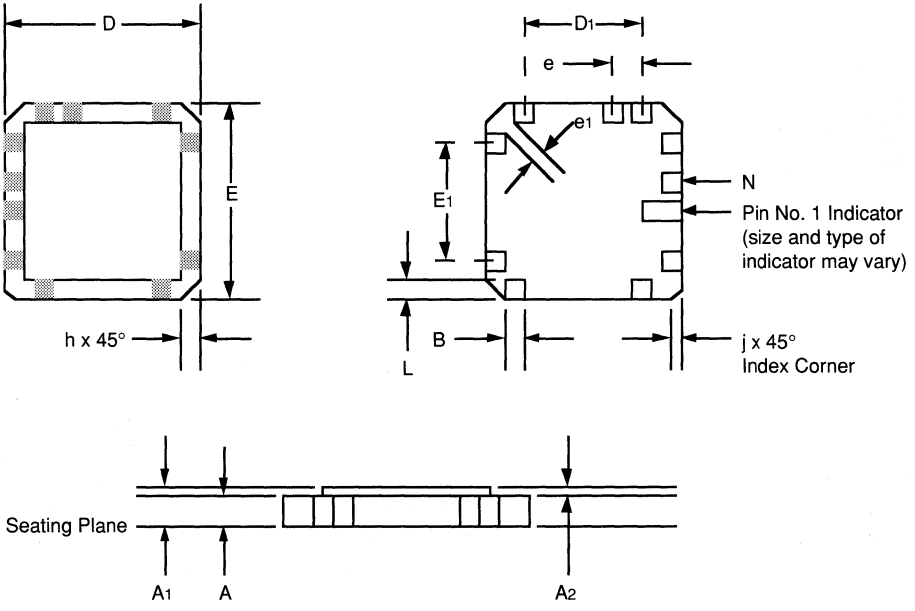
Symbol List for Ceramic Leadless Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Thickness of base body
A_1	Total package height
A_2	Distance from base body to highest point of body (lid)
B	Width of terminal lead pin
D	Largest overall package dimension of length
D_1, E_1	Body length dimension - end lead center to end lead center
E	Largest overall package dimension of width
e	Linear spacing
e_1	Linear spacing between edges of true lead positions (of corner terminal lead pads) lead corner to lead corner
h	Depth of major index feature
j	Width of minor index feature
L	Distance from package edge to end of effective pad
N	Total number of potentially useable lead positions

Notes:

1. Controlling dimension: inches.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by PC board hole size.
4. Dimension "B" is nominal.
5. Corner configuration optional.

Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Leadless Chip Carrier

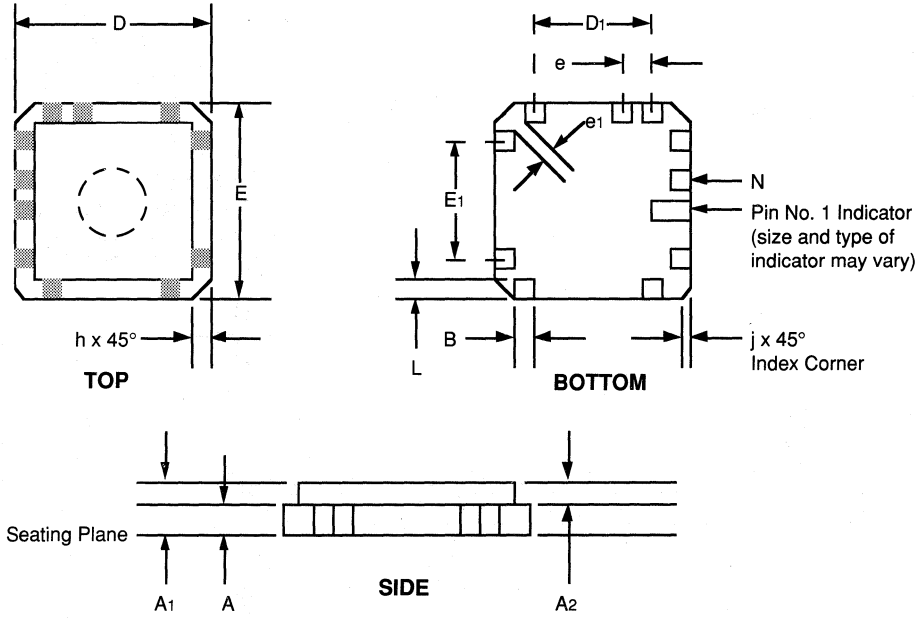


Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	1.651	2.540		0.065	0.100	
A2	0.254	0.381		0.010	0.015	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	11.2268	11.684		0.442	0.460	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.684		0.442	0.460	
E1	7.620	7.620	Reference	0.300	0.300	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	28	28		28	28	

8

Packaging Diagrams and Parameters

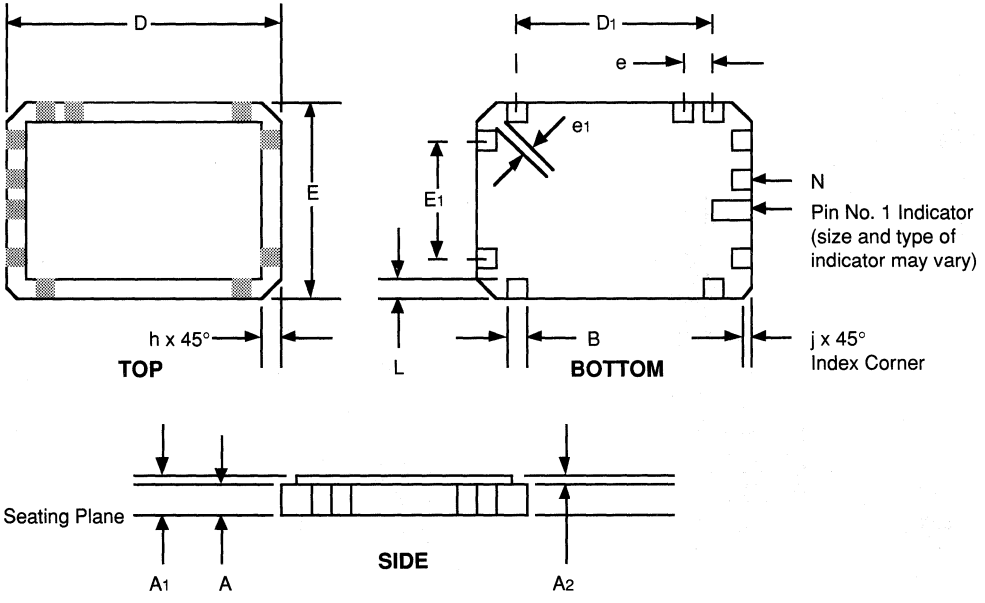
Package Type: 28-Lead Ceramic Leadless Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.100	
A2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	11.2268	11.684		0.442	0.460	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.684		0.442	0.460	
E1	7.620	7.620	Reference	0.300	0.300	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	28	28		28	28	

Packaging Diagrams and Parameters

Package Type: 32-Lead Ceramic Leadless Chip Carrier

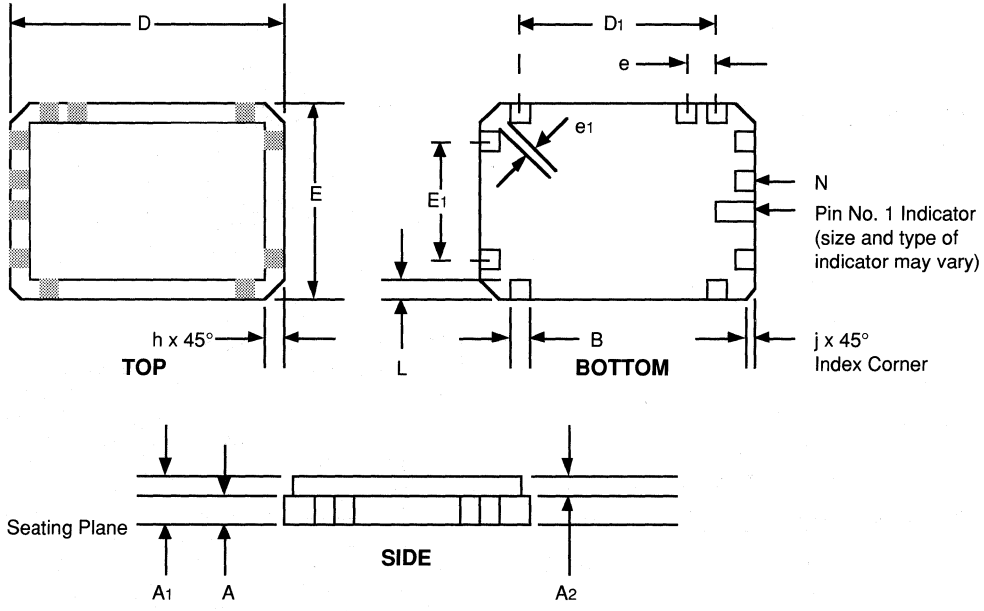


Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.54	3.048		0.100	0.120	
A2	0.254	0.381		0.010	0.015	
B	0.635	0.7112	Typical	0.025	0.026	Typical
D	13.716	14.224		0.540	0.560	
D1	9.98	10.34	Reference	0.393	0.407	Reference
E	11.2268	11.684		0.442	0.458	
E1	7.442	7.80	Reference	0.293	0.307	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

8

Packaging Diagrams and Parameters

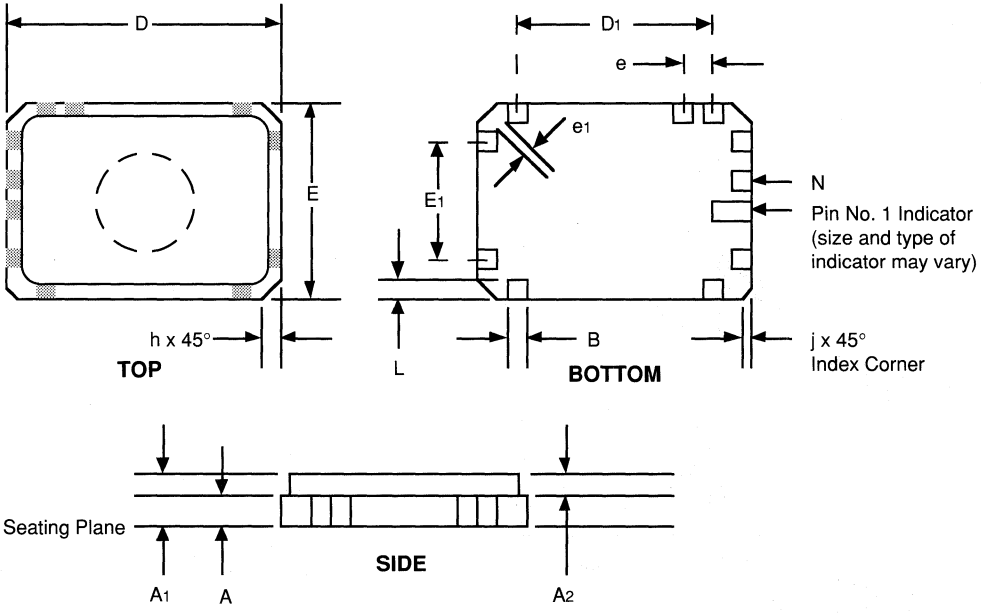
Package Type: 32-Lead Ceramic Leadless Chip Carrier - FRIT



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.635	1.143		0.025	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.6332		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

Package Type: 32-Lead Ceramic Leadless Chip Carrier with Window

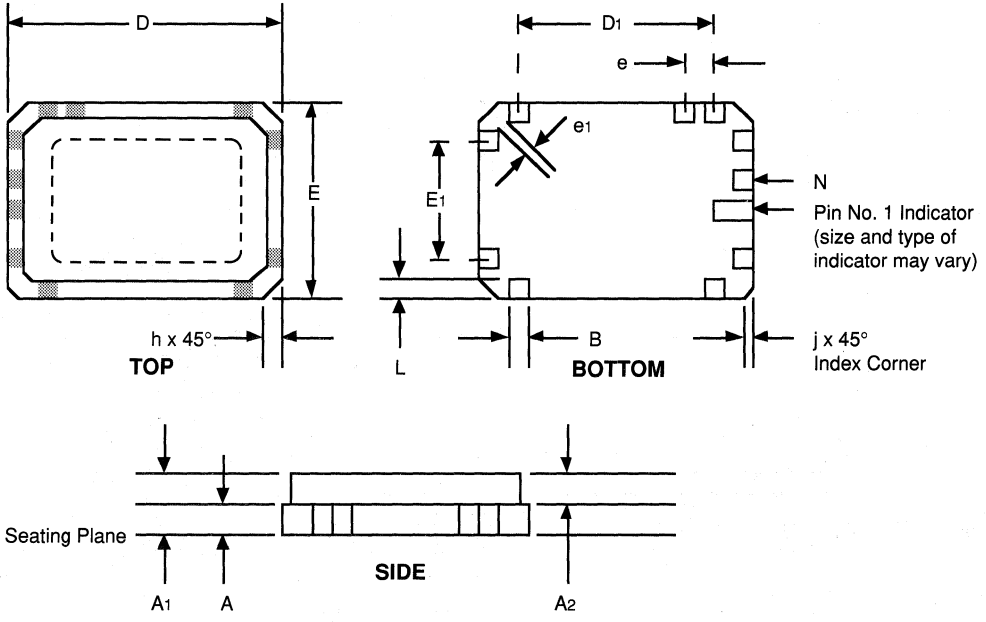


Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.6332		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	1.02	1.02	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

8

Packaging Diagrams and Parameters

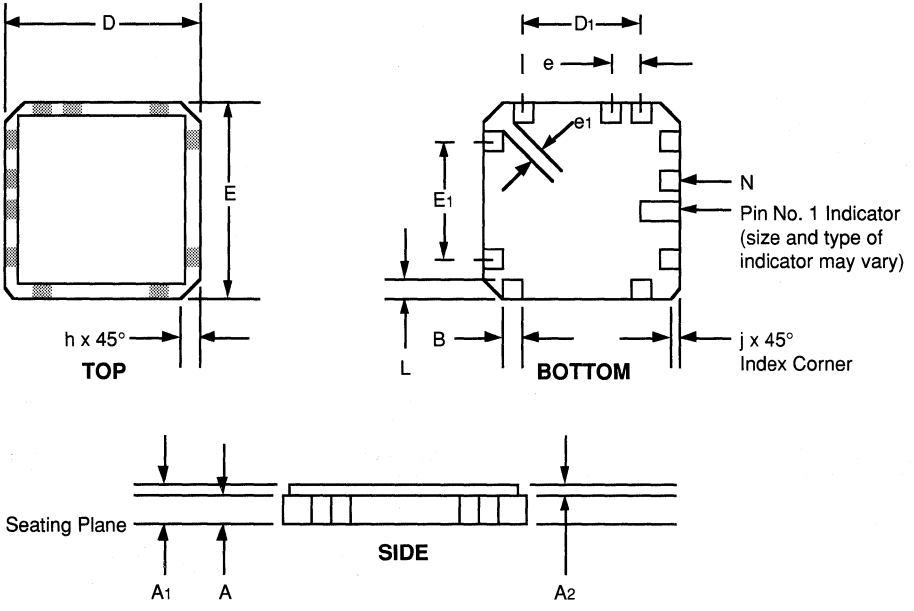
Package Type: 32-Lead Ceramic Leadless FRIT-Seal Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.889	1.143		0.035	0.045	
B	0.5588	0.7112	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.2268	11.6332		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

Package Type: 44-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.37	2.082		0.054	0.082	
A1	1.778	3.048		0.070	0.120	
A2	0.254	1.143		0.010	0.045	
B	0.584	0.7112	Typical	0.023	0.028	Typical
D	16.256	16.8148		0.640	0.662	
D1	12.700	12.700	Reference	0.500	0.500	Reference
E	16.256	16.8148		0.640	0.662	
E1	12.700	12.700	Reference	0.500	0.500	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.38	–	Typical	0.015	–	Typical
h	1.02	1.02	Reference	0.040	0.040	Reference
j	0.51	0.51	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	44	44		44	44	

Packaging Diagrams and Parameters

Ceramic Leaded Chip Carrier Family

Symbol List for Ceramic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance from seating plane to highest point of body
A_1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D_1/E_1	Body dimension
D_2/E_2	Footprint
D_3/E_3	Footprint
LT	Lead thickness
N	Total number of potentially useable lead positions
N_d	Total number of leads on short side (rectangular)
N_e	Total number of leads on long side (rectangular)

Notes:

1 All dimensions and tolerances conform to ANSI Y14.5M-1982.

2 Datum plane -H- located at top of parting line and coincident with top of lead. Where lead exits body.

3 Datums D–E and F–G to be determined where center leads exit body at datum plane -H-.

4 To be determined at seating plane -C-.

5 Transition is optional.

6 Square: Details of pin 1 identifier are optional but must be located within one of the two zones indicated.
Rectangle: Details of pin 1 identifier are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.

7 Location to datums -A- and -B- to be determined at plane -H-.

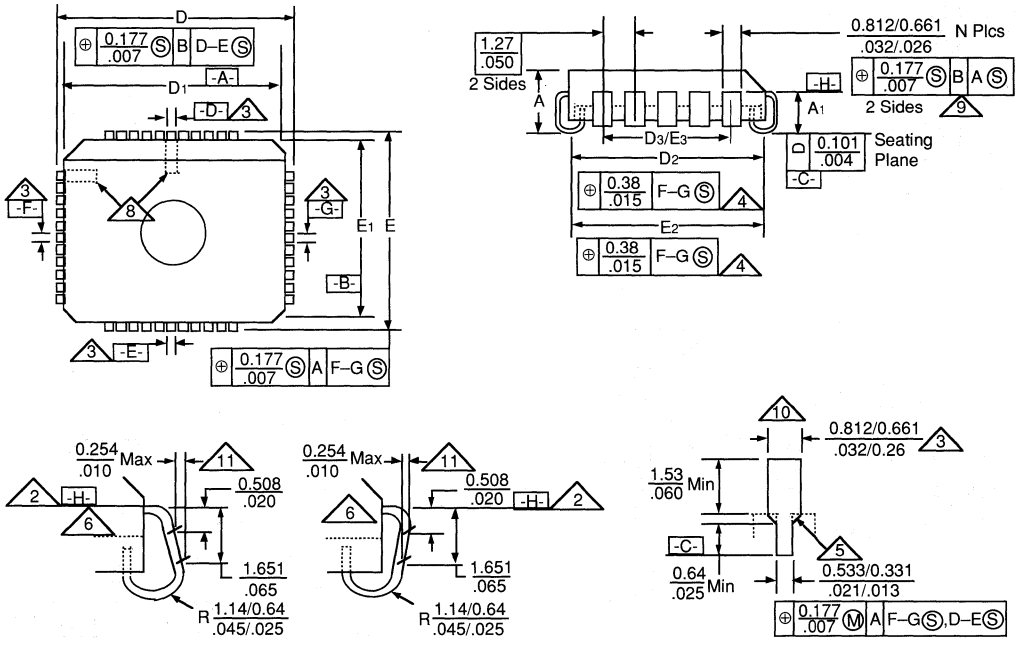
8 All dimensions and tolerances include lead trim offset and lead finish.

9 These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.

10 Controlling dimension: inches.

Packaging Diagrams and Parameters

Package Type: 68-Lead Ceramic Leaded Chip Carrier (Window)

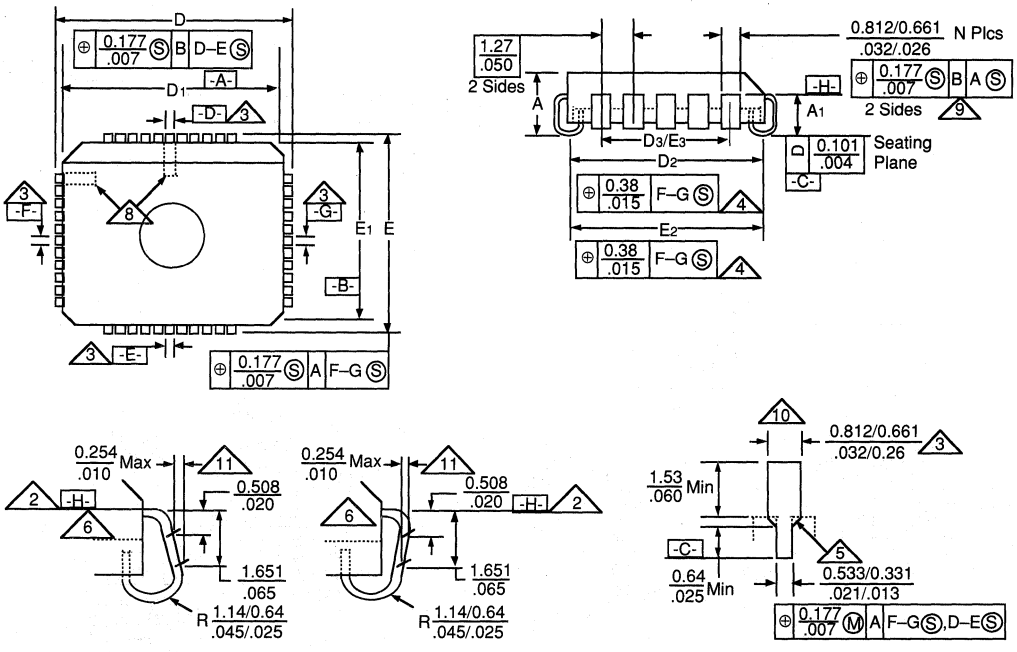


Package Group: Ceramic Leaded Chip Carrier (CLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		.165	.185	
A1	2.286	3.048		.090	.120	
D	24.968	25.222		.983	.993	
D1	23.977	24.333		.944	.958	
D2	22.860	23.876		.900	.940	
D3	20.320	-	Reference	.800	-	Reference
E	24.968	25.222		.983	.993	
E1	23.977	24.333		.944	.958	
E2	22.860	23.876		.900	.940	
E3	20.320	-	Reference	.800	-	Reference
N	68	-		68	-	
CP	-	.1016		-	.004	
LT	.1524	.2032		.006	.008	

8

Packaging Diagrams and Parameters

Package Type: 84-Lead Ceramic Leaded Chip Carrier (Window)



Package Group: Ceramic Leaded Chip Carrier (CLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		.165	.185	
A1	2.286	3.048		.090	.120	
D	30.048	30.353		1.183	1.195	
D1	28.829	29.591		1.135	1.165	
D2	27.940	28.956		1.100	1.140	
D3	25.400	-	Reference	1.000	-	Reference
E	30.048	30.353		1.183	1.195	
E1	28.829	29.591		1.135	1.165	
E2	27.940	28.956		1.100	1.140	
E3	25.400	-	Reference	1.000	-	Reference
N	84	-		84	-	
CP	-	.1016		-	.004	
LT	.1524	.2032		.006	.008	

Packaging Diagrams and Parameters

Plastic Dual In-line Family

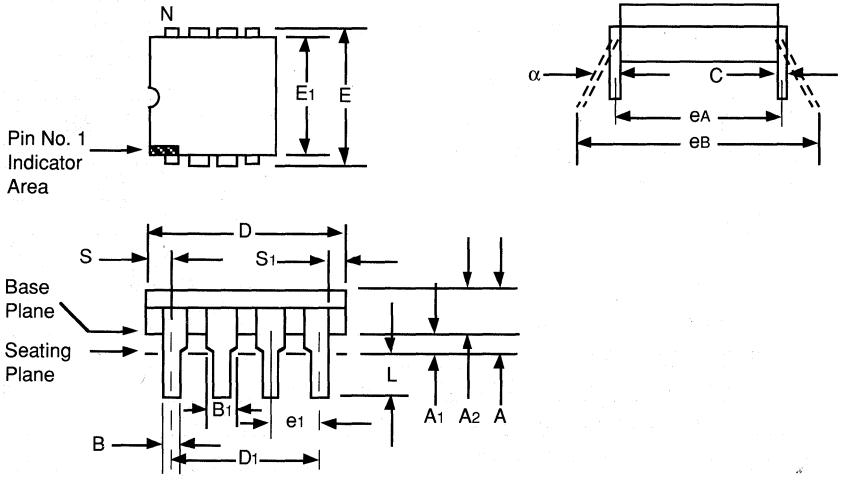
Symbol List for Plastic Dual In-line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
A_2	Base body thickness
B	Width of terminal leads
B_1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D_1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E_1	Body width parameters not including leads
e_A	Linear spacing of true minimum lead position center line to center line
e_B	Linear spacing between true lead position outside of lead to outside of lead
e_1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially useable lead positions
S	Distance from true position center line of No. 1 lead to the extremity of the body
S_1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B_1" is nominal.
5. Details of pin No. 1 identifier are optional.
6. Parameters "D + E_1" do not include mold flash/protrusions. Mold flash or protrusions shall not exceed .010 inches.

Packaging Diagrams and Parameters

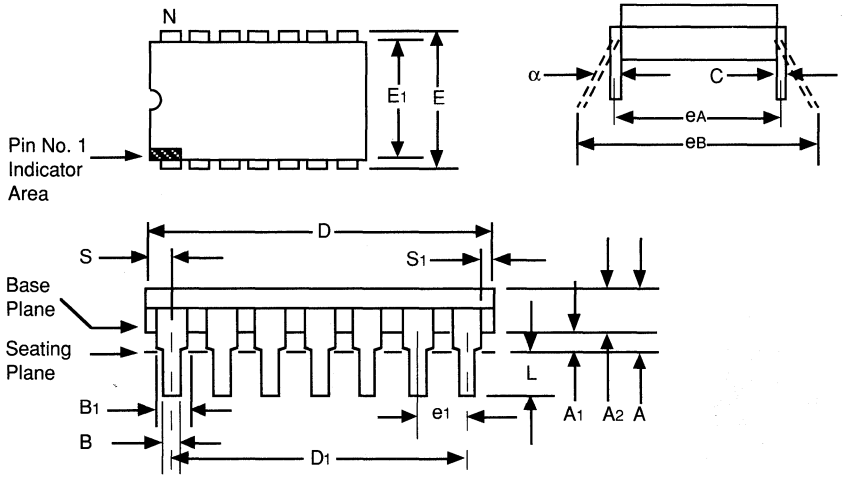
Package Type: 8-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A_1	0.381	–		0.015	–	
A_2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B_1	1.397	1.651		0.055	0.065	
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	9.017	10.922		0.355	0.430	
D_1	7.620	7.620	**Reference**	0.300	0.300	**Reference**
E	7.620	8.255		0.300	0.325	
E_1	6.096	7.112		0.240	0.280	
e_1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
e_A	7.620	7.620	**Reference**	0.300	0.300	**Reference**
e_B	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	8	8		8	8	
S	0.889	–		0.035	–	
S_1	0.254	–		0.010	–	

Packaging Diagrams and Parameters

Package Type: 14-Lead Plastic Dual In-line (.300 mil)

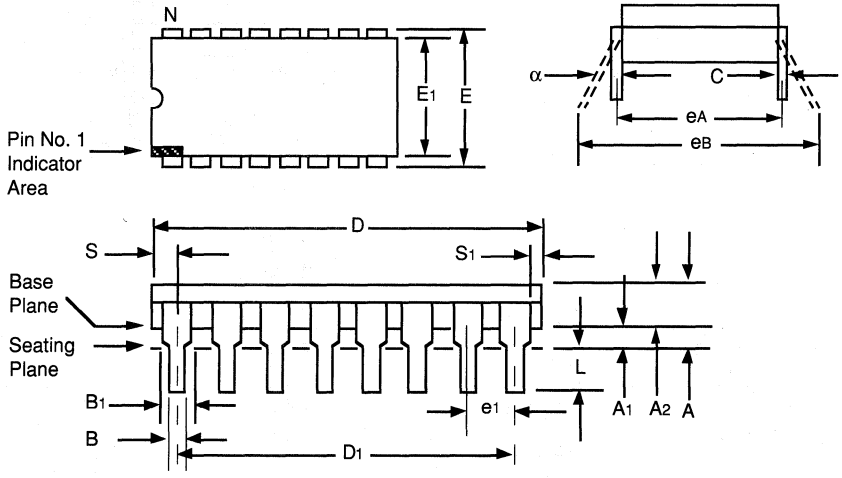


Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	18.415	19.431		0.725	0.765	
D1	15.240	15.240	**Reference**	0.600	0.600	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.4892	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	14	14		14	14	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

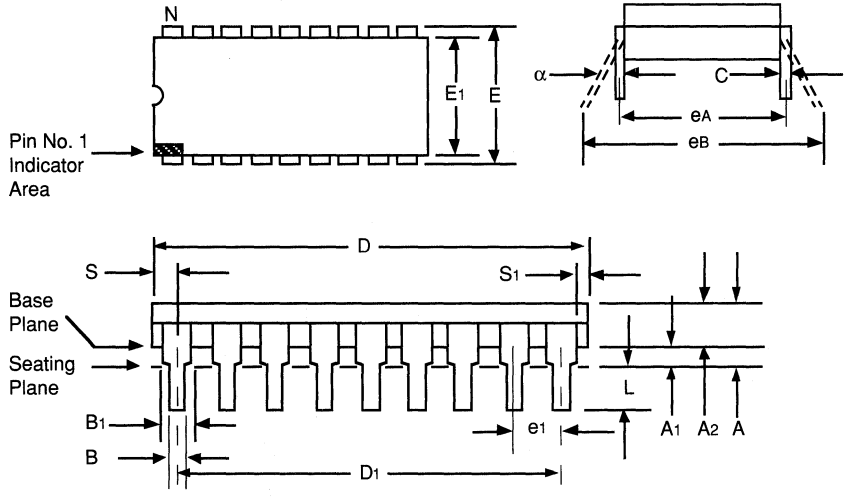
Package Type: 16-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	18.923	19.939		0.745	0.785	
D1	17.780	17.780	**Reference**	0.700	0.700	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.0480	3.556		0.120	0.140	
N	16	16		16	16	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 18-Lead Plastic Dual In-line (.300 mil)

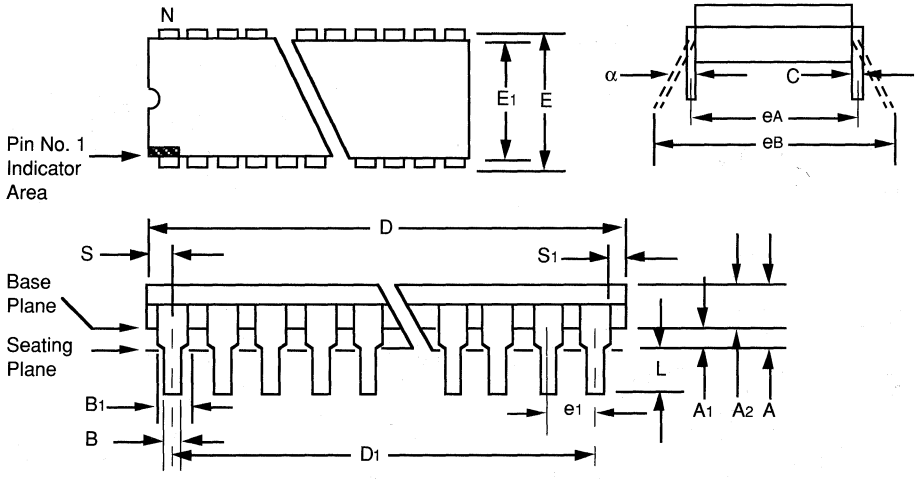


Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	Typical	0.060	0.060	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.479	23.495		0.885	0.925	
D1	20.320	20.32	Reference	0.800	0.800	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

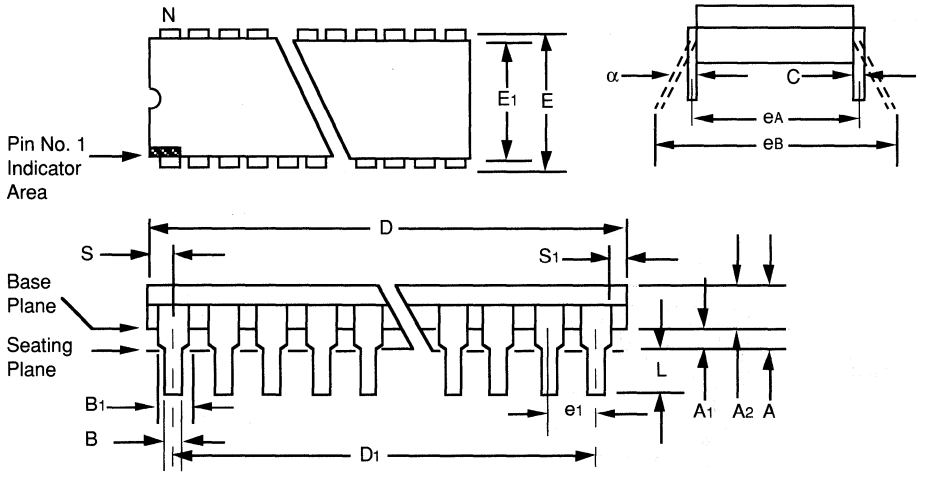
Package Type: 22-Lead Plastic Dual In-line (.400 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	.180		–	.180	
A1	0.381	–		0.015	–	
A2	3.175	3.810		0.125	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	26.670	28.448		1.050	1.120	
D1	25.400	25.400	**Reference**	1.000	1.000	**Reference**
E	9.906	10.795		0.390	0.425	
E1	8.382	9.398		0.330	0.370	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	10.160	10.160	**Reference**	0.400	0.400	**Reference**
eB	10.160	12.192		0.400	0.480	
L	3.048	3.556		0.120	0.140	
N	22	22		22	22	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 24-Lead Plastic Dual In-line (.600 mil)

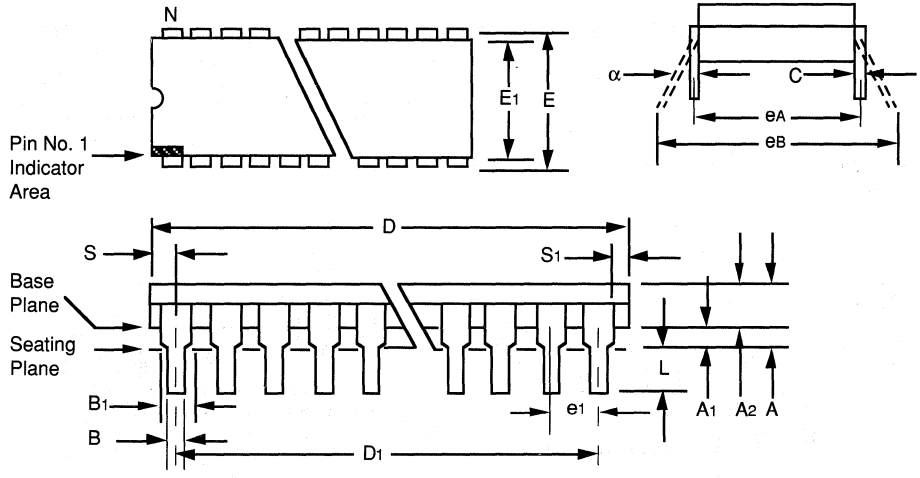


Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	30.353	32.385		1.195	1.275	
D1	27.940	27.940	**Reference**	1.100	1.100	**Reference**
E	15.240	15.875		0.600	0.625	
E1	12.827	14.224		0.505	0.560	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	15.494	17.272		0.610	0.680	
L	3.048	3.556		0.120	0.140	
N	24	24		24	24	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

8

Packaging Diagrams and Parameters

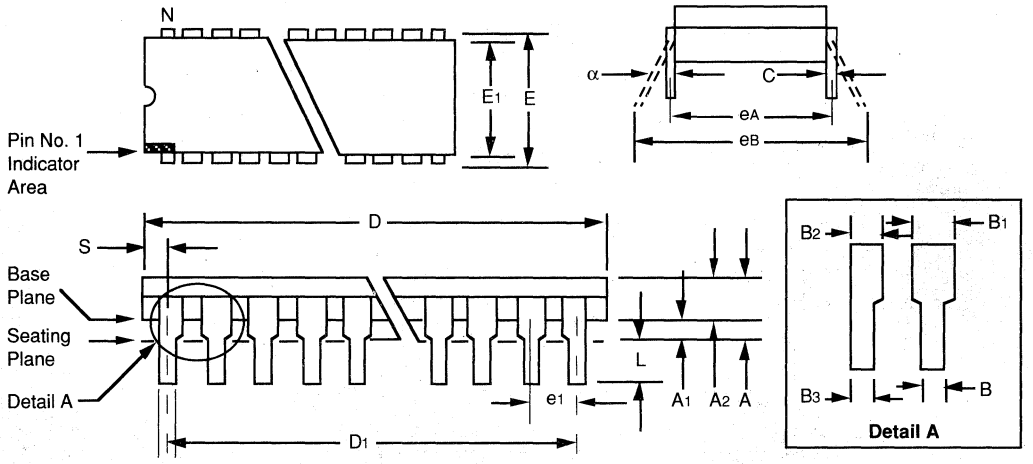
Package Type: 24-Lead Plastic Dual In-line (.300 mil)



Package Group: Plastic Dual In-line Package (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.356	0.559		0.014	0.022	
B1	1.524	1.524	**Typical**	0.060	0.060	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	31.242	32.258		1.230	1.270	
D1	27.940	27.940	**Reference**	1.100	1.100	**Reference**
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	24	24		24	24	
S	0.889	–		0.035	–	
S1	0.381	–		0.015	–	

Packaging Diagrams and Parameters

Package Type: 28-Lead Dual In-line Plastic (.300 mil)

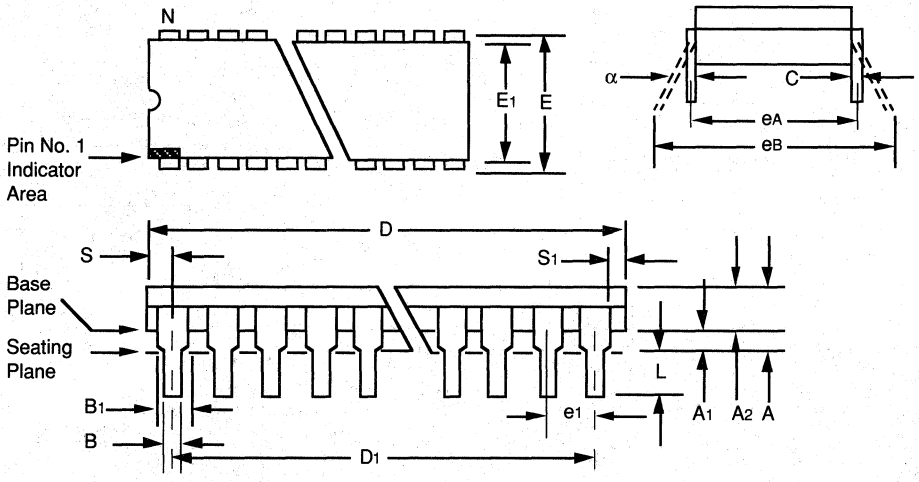


Package Group: Plastic Dual-In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.63	4.57		.143	.180	
A1	.38	–		.015	–	
A2	3.25	3.65		.128	.140	
B	.41	.56		.016	.022	Typical
B1	1.02	1.65	Typical	.040	.065	
B2	.762	1.02	4 places	.030	.040	4 places
B3	.20	.51	4 places	.008	.020	4 places
C	.20	.33	Typical	.008	.013	Typical
D	34.16	35.43		1.345	1.395	
D1	33.02	33.02	Reference	1.300	1.300	Reference
E	7.87	8.38		.310	.330	
E1	7.1	7.52		.280	.296	
e1	2.54	2.54	Typical	.100	.100	Typical
eA	7.87	7.87	Reference	.310	.310	Reference
eB	8.64	9.65		.340	.380	
L	3.18	3.68		.125	.145	
N	28	-		28	-	
S	.58	1.22		.023	.048	

8

Packaging Diagrams and Parameters

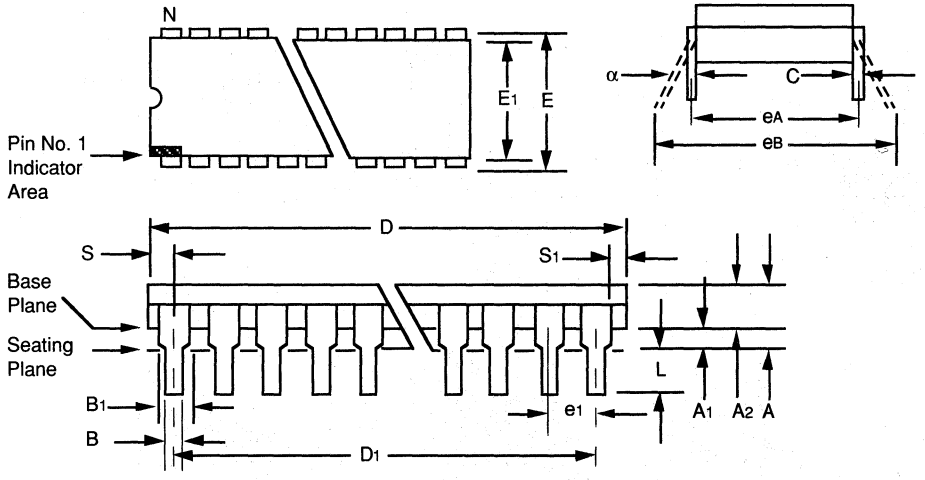
Package Type: 28-Lead Dual In-line Plastic (.600 mil)



Package Group: Plastic Dual-In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B1	1.270	1.778	Typical	0.050	0.070	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	35.560	37.084		1.400	1.460	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15.875		0.600	0.625	
E1	12.827	13.970		0.505	0.550	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	28	28		28	28	
S	0.889	–		0.035	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

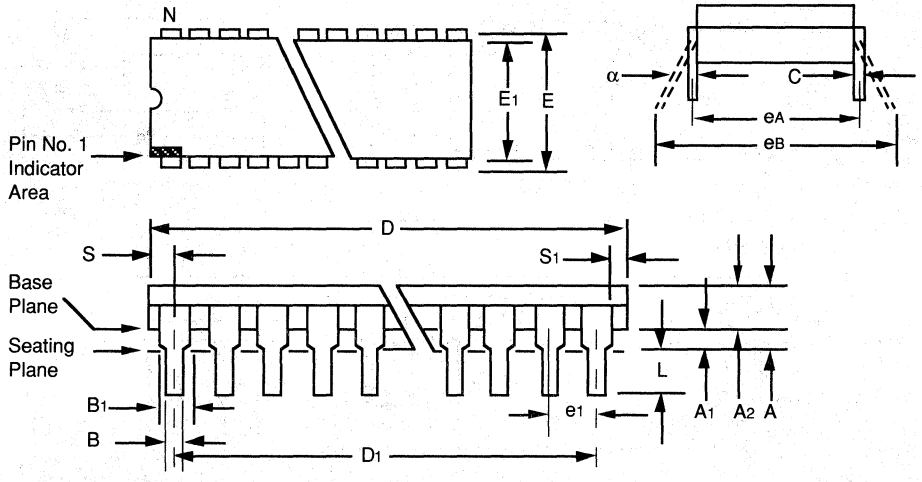
Package Type: 40-Lead Plastic Dual In-line (.600 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.381	–		0.015	–	
A2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B1	1.270	1.778	Typical	0.050	0.070	Typical
C	0.2032	0.381	Typical	0.008	0.015	Typical
D	51.181	52.197		2.015	2.055	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	13.462	13.970		0.530	0.550	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	40	40		40	40	
S	1.270	–		0.050	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

Package Type: 48-Lead Plastic Dual In-line (.600 mil)



Package Group: Plastic Dual In-line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A_1	0.381	–		0.015	–	
A_2	3.175	4.064		0.125	0.160	
B	0.356	0.559		0.014	0.022	
B_1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.2032	0.381	**Typical**	0.008	0.015	**Typical**
D	61.468	62.230		2.420	2.450	
D_1	58.420	58.420	**Reference**	2.300	2.300	**Reference**
E	15.240	15.875		0.600	0.625	
E_1	13.716	14.224		0.540	0.560	
e_1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
e_A	15.240	15.240	**Reference**	0.600	0.600	**Reference**
e_B	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	48	48		48	48	
S	1.270	–		0.050	–	
S_1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

Plastic Leaded Chip Carrier Family

Symbol List for Plastic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance from seating plane to highest point of body
A1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D1/E1	Plastic body dimension
D2/E2	Footprint
D3/E3	Footprint
LT	Lead thickness
N	Total number of potentially useable lead positions
Nd	Total number of leads on short side (rectangular)
Ne	Total number of leads on long side (rectangular)

Notes:

1 All dimensions and tolerances conform to ANSI Y14.5M-1982.
2 Datum plane -H- located at top of mold parting line and coincident with top of lead. Where lead exits plastic body.
3 Datums D–E and F–G to be determined where center leads exit plastic body at datum plane -H-.
4 To be determined at seating plane -C-.
5 Transition is optional.
6 Plastic body details between leads are optional.
7 Dimensions D1 and E1 do not include mold protru sion. Allowable mold protrusion is .254 mm/.010 in. per side. Dimensions D and E include mold mismatch and are dtermined at parting line.
8 Square: Details of pin 1 identifier are optional but must be located within one of the two zones indicated.
Rectangle: Details of pin 1 identifier are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.
9 Location to datums -A- and -B- to be determined at plane -H-.
10 All dimensions and tolerances include lead trim offset and lead finish.
11 These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
12 Controlling dimension: inches.

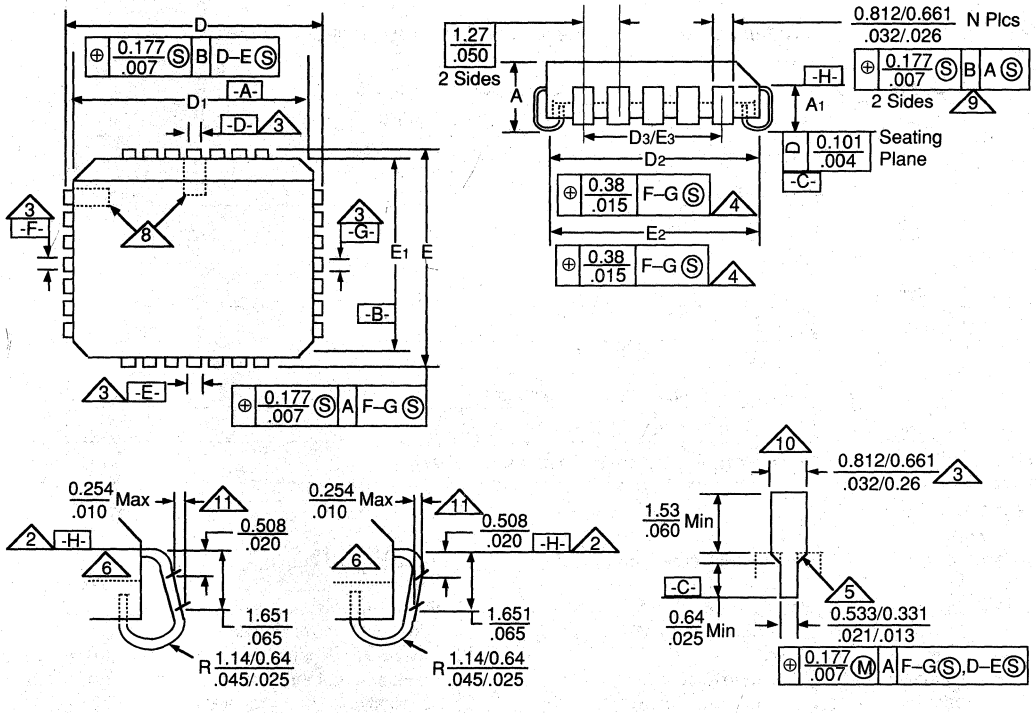
X Sum of dam bar protrusions to be 0.17 (.007) max per lead.

Y Feature is not required, but is optional at

8

Packaging Diagrams and Parameters

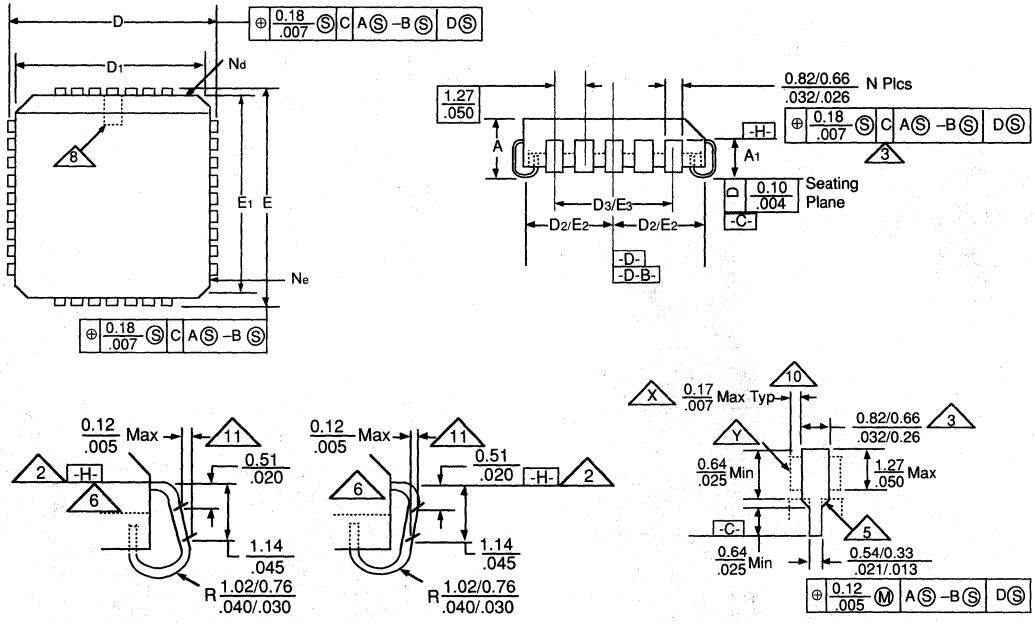
Package Type: 28-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	12.319	12.573		0.485	0.495	
D1	11.430	11.582		0.450	0.456	
D2	10.414	10.922		0.410	0.430	
D3	7.620	7.620	Reference	0.300	0.300	Reference
E	12.319	12.573		0.485	0.495	
E1	11.430	11.582		0.450	0.456	
E2	10.414	10.922		0.410	0.430	
E3	7.620	7.620	Reference	0.300	0.300	Reference
N	28	28		28	28	
CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

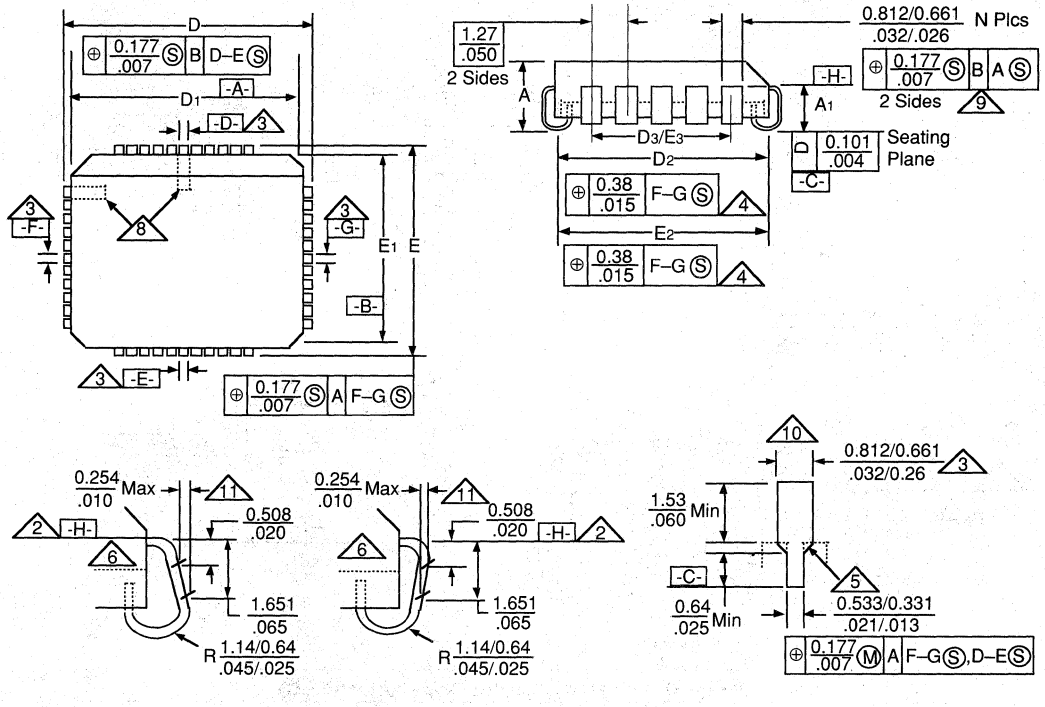
Package Type: 32-Lead Plastic Leaded Chip Carrier (Rectangle)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.048	3.556		0.120	0.140	
A1	1.905	2.413		0.075	0.095	
D	12.319	12.573		0.485	0.495	
D1	11.35	11.506		0.447	0.453	
D2	4.826	5.334		0.190	0.210	
D3	7.620	7.620	Reference	0.300	0.300	Reference
E	14.859	15.113		0.585	0.595	
E1	13.893	14.046		0.547	0.553	
E2	6.096	6.858		0.240	0.270	
E3	10.160	10.160	Reference	0.400	0.400	Reference
N	32	32		32	32	
Nd	7	7		7	7	
Ne	9	9		9	9	
CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

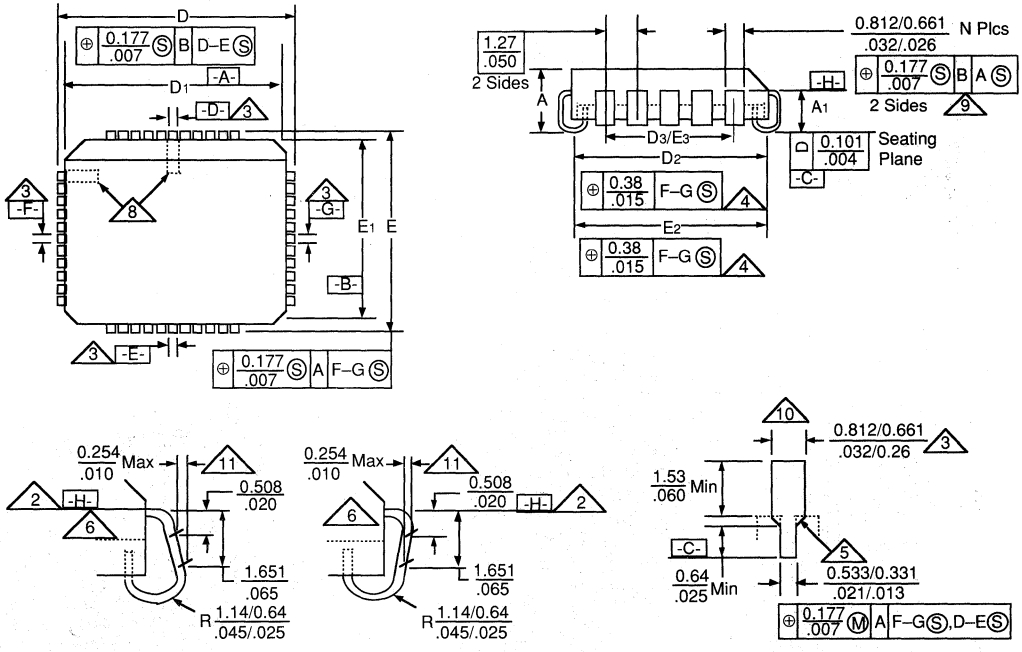
Package Type: 44-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	17.399	17.653		0.685	0.695	
D1	16.510	16.662		0.650	0.656	
D2	15.494	16.002		0.610	0.630	
D3	12.700	12.700	Reference	0.500	0.500	Reference
E	17.399	17.653		0.685	0.695	
E1	16.510	16.662		0.650	0.656	
E2	15.494	16.002		0.610	0.630	
E3	12.700	12.700	Reference	0.500	0.500	Reference
N	44	44		44	44	
CP	–	0.1016		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

Package Type: 68-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		.165	.185	
A1	2.286	2.794		.090	.110	
D	25.019	25.273		.985	.995	
D1	24.130	24.333		.950	.958	
D2	22.860	23.622		.900	.930	
D3	20.320	-	Reference	.800	-	Reference
E	25.019	25.273		.985	.995	
E1	24.130	24.333		.950	.958	
E2	22.860	23.622		.900	.930	
E3	20.320	-	Reference	.800	-	Reference
N	68	-		68	-	
CP	-	.1016		-	.004	
LT	.2032	.254		0.008	0.010	

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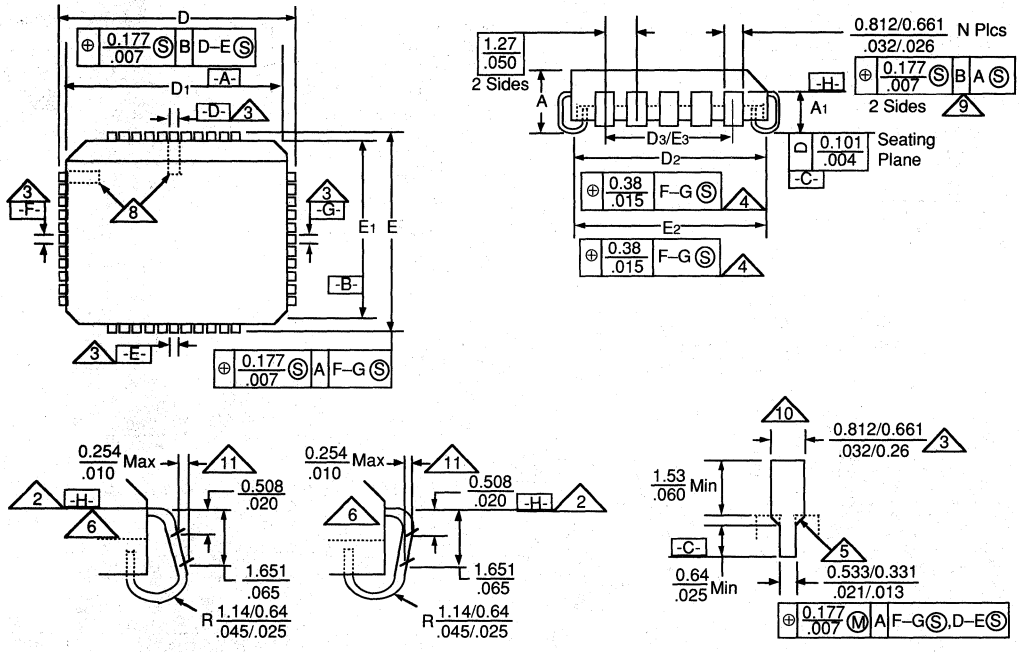
Packaging Diagrams and Parameters

Package Type: 84-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		.165	.185	
A1	2.286	2.794		.090	.110	
D	30.099	30.353		1.185	1.195	
D1	29.210	29.413		1.150	1.158	
D2	27.940	28.702		1.100	1.130	
D3	25.400	-	Reference	1.000	-	Reference
E	30.099	30.353		1.185	1.195	
E1	29.210	29.413		1.150	1.158	
E2	27.940	28.702		1.100	1.130	
E3	25.400	-	Reference	1.000	-	Reference
N	84	-		84	-	
CP	-	.1016		-	.004	
LT	.2032	.254		.008	.010	

Packaging Diagrams and Parameters

Plastic Small Outline Family

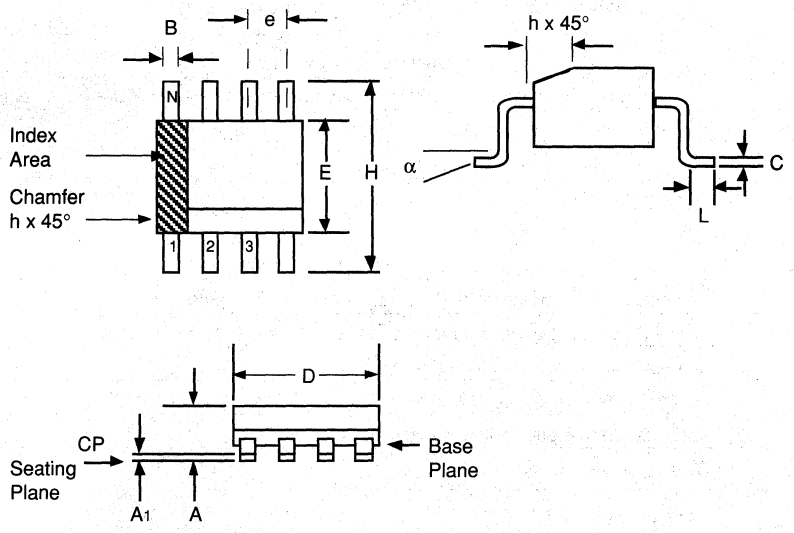
Symbol List for Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spaciing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead postions
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: inches.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .006 package ends and .010 on sides.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

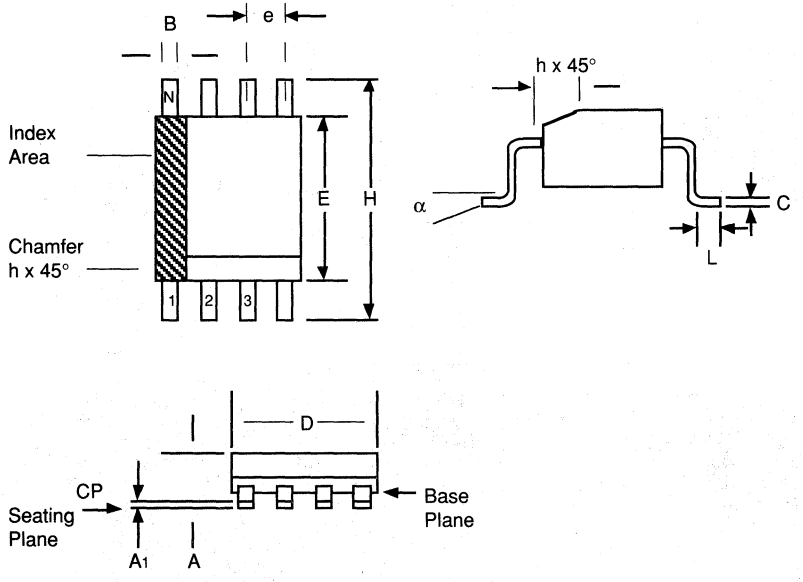
Package Type: 8-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SN)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.3716	1.7272		0.054	0.068	
A1	0.1016	0.2489		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.2489		0.0075	0.0098	
D	4.8006	4.9784		0.189	0.196	
E	3.810	3.9878		0.150	0.157	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	5.8166	6.1976		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
N	8	8		8	8	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

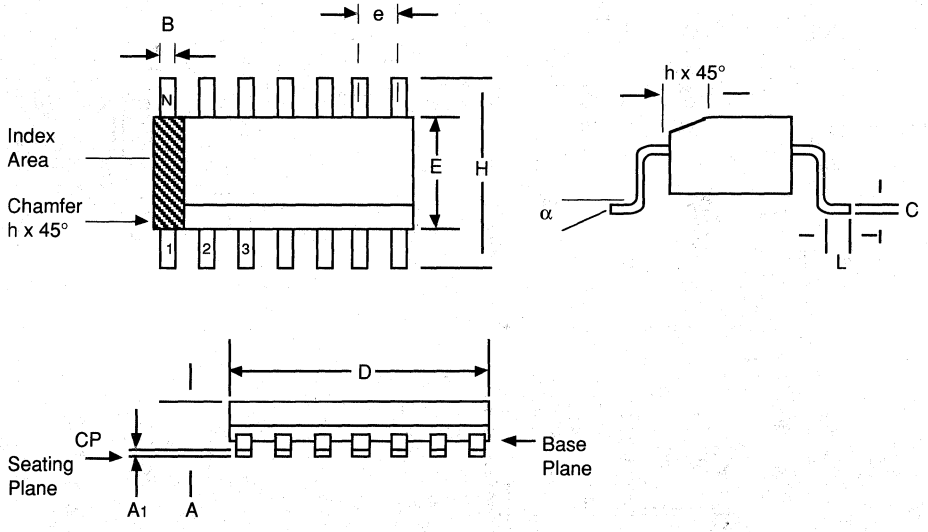
Package Type: 8-Lead Plastic Surface Mount (SOIC - Medium, 200 mil Body)



Package Group: Plastic SOIC (SM)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.778	2.032		0.070	0.080	
A1	0.1016	0.2489		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.2489		0.0075	0.0098	
D	5.08	5.334		0.200	0.210	
E	5.156	5.410		0.203	0.213	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	7.62	8.382		0.300	0.330	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
N	14	14		14	14	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

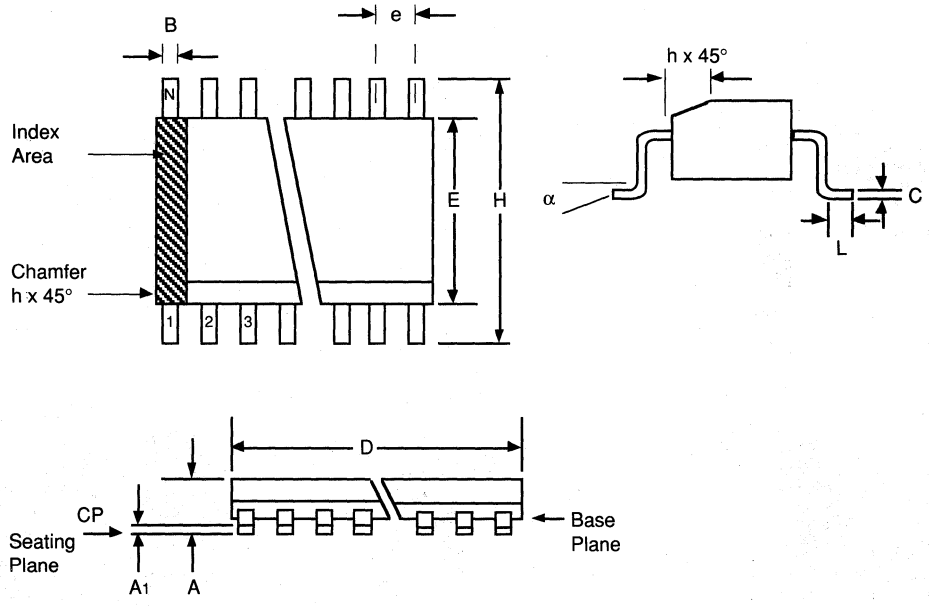
Package Type: 14-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SL)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.3716	1.7272		0.054	0.068	
A1	0.1016	0.2489		0.004	0.0098	
B	0.3556	0.4826		0.014	0.019	
C	0.1905	0.2489		0.0075	0.0098	
D	9.830	9.982		0.387	0.393	
E	3.810	3.9878		0.150	0.157	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	5.8166	6.1976		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	14	14		16	16	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

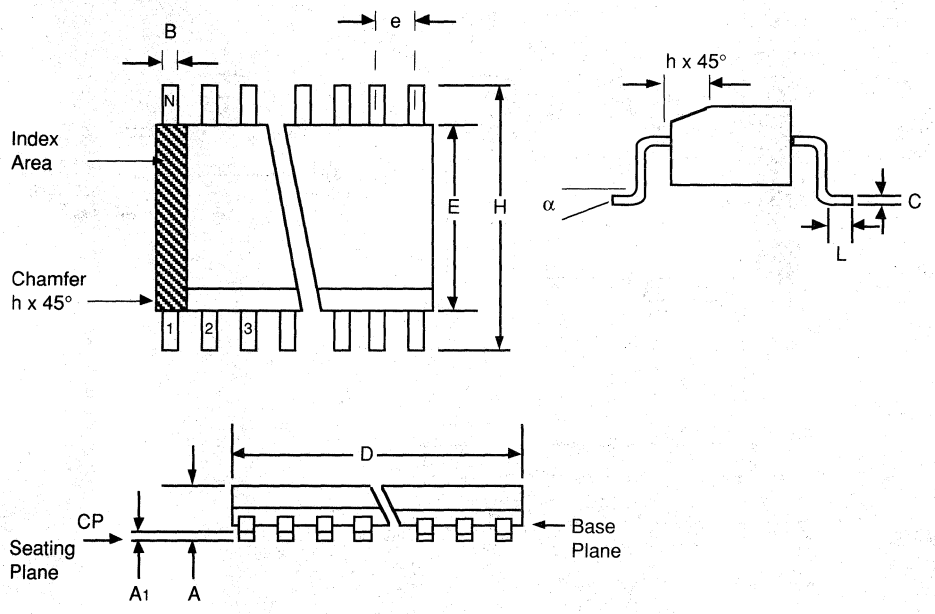
Package Type: 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A_1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	11.3538	11.7348		0.447	0.462	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	18	18		18	18	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

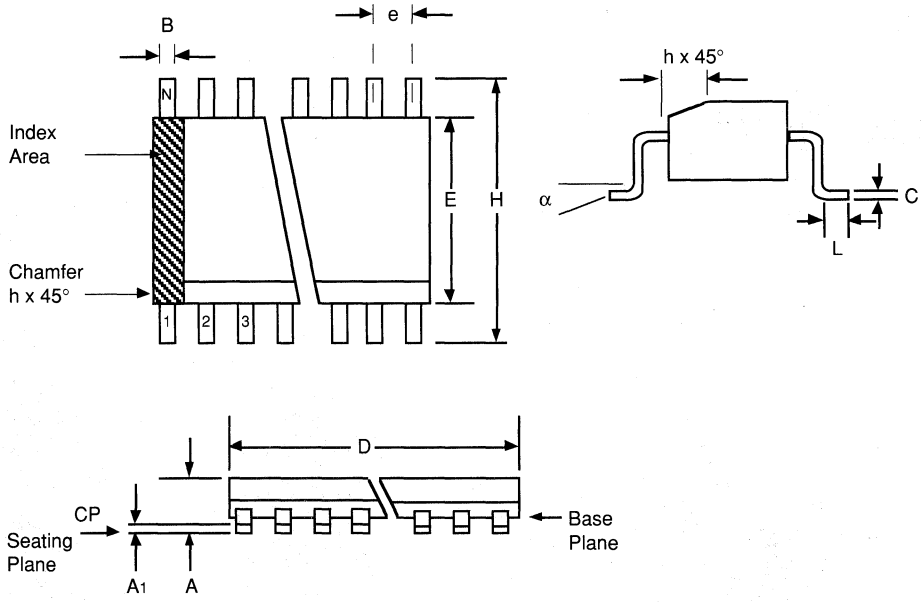
Package Type: 24-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	15.2146	15.5956		0.599	0.614	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	24	24		24	24	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)

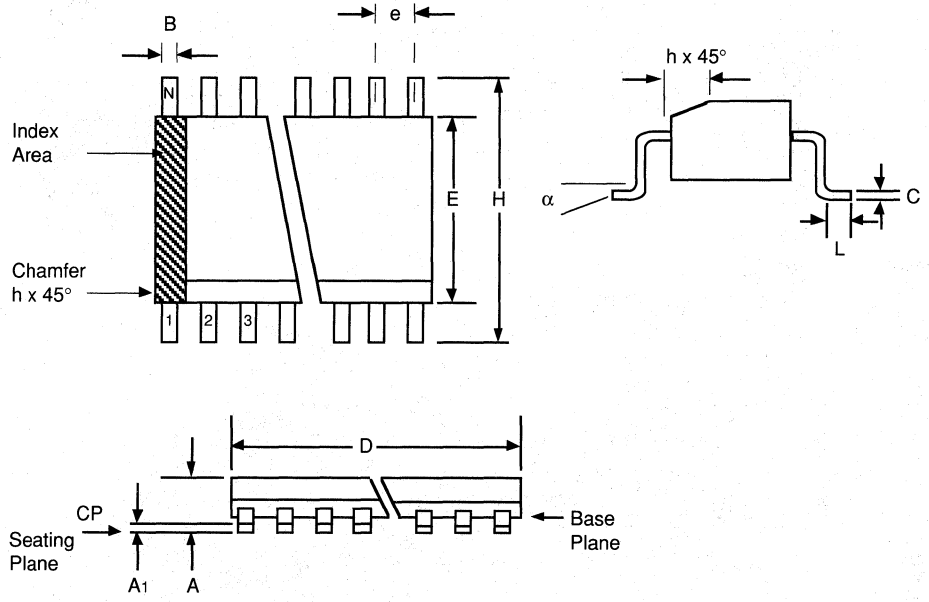


Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.3622	2.6416		0.093	0.104	
A1	0.1016	0.2997		0.004	0.0118	
B	0.3556	0.4826		0.014	0.019	
C	0.2413	0.3175		0.0095	0.0125	
D	17.7038	18.0848		0.697	0.712	
E	7.4168	7.5946		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.0076	10.6426		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.4064	1.143		0.016	0.045	
N	28	28		28	28	
CP	–	0.1016		–	0.004	

8

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (SOIC - Wide, 330 mil Body)



Package Group: Plastic SOIC (SW)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	2.286	2.642		.090	.104	
A1	0.102	0.279		.004	.011	
B	0.356	0.508		.014	.020	
C	0.228	0.305		.009	.012	
D	17.780	18.085		.700	.712	
E	8.636	8.890		.340	.350	
e	1.27	1.27	Typical	.050	.050	Typical
H	11.760	12.116		.463	.477	
h	0.254	0.736		.010	.029	
L	0.508	1.067		.020	.042	
N	28	28		28	28	
CP	–	0.1016		–	0.004	

Packaging Diagrams and Parameters

Plastic Shrink Small Outline Family

Symbol List for Shrink Small Outline Package Parameter	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead positions
CP	Seating plane coplanarity

Notes: 1. Controlling parameter: mm.

2. All packages are gull wing lead form.

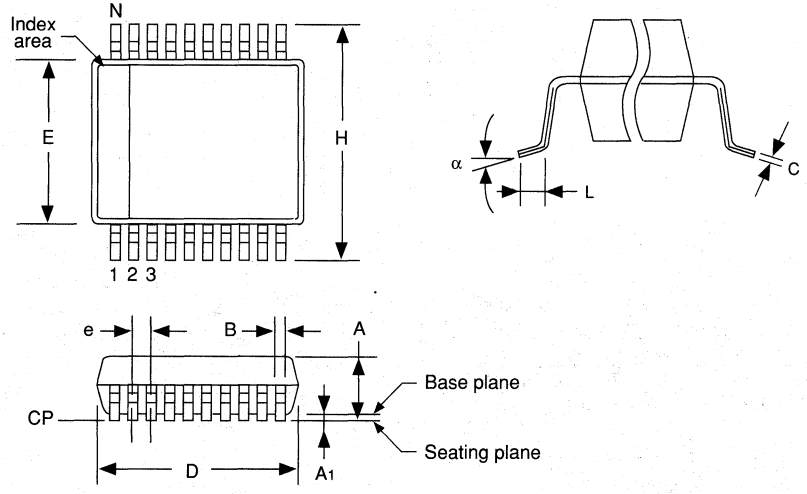
3. "D" and "E" are reference datums and do not include mold flash or protrusions.
Mold flash or protrusions shall not exceed 0.15mm .006 package ends and .010" on sides.

4. A .25mm visual index feature must be located within the crosshatched area to indicate pin 1 position.

5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

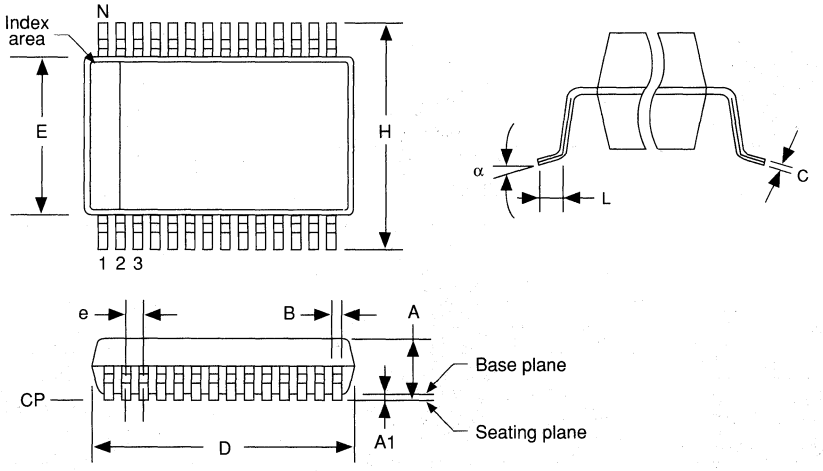
Package Type: 20-Lead Plastic Surface Mount (SSOP - .209 mil Body 5.30mm)



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.73	1.99		0.68	0.78	
A_1	0.05	0.21		0.002	0.008	
B	0.25	0.38		0.010	0.015	
C	0.13	0.22		0.005	0.009	
D	7.07	7.33		0.278	0.289	
E	5.20	5.38		0.205	0.212	
e	0.65	0.65	Typical	0.256	0.256	Typical
H	7.65	7.90		0.301	0.311	
L	0.55	0.95		0.022	0.037	
N	20	20		20	20	
CP	-	0.1016		-	0.004	

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (SSOP - .209 mil Body 5.30mm)



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.73	1.99		0.68	0.78	
A_1	0.05	0.21		0.002	0.008	
B	0.25	0.38		0.010	0.015	
C	0.13	0.22		0.005	0.009	
D	10.07	10.33		0.397	0.407	
E	5.20	5.38		0.205	0.212	
e	0.65	0.65	Typical	0.256	0.256	Typical
H	7.65	7.90		0.301	0.311	
L	0.55	0.95		0.022	0.037	
N	28	28		28	28	
CP	-	0.1016		-	0.004	

8

Packaging Diagrams and Parameters

Plastic Thin Small Outline Family

Symbol List for Thin Small Outline Package Parameter	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead positions
CP	Seating plane coplanarity

Notes: 1. Controlling parameter: inches.

2. All packages are gull wing lead form.

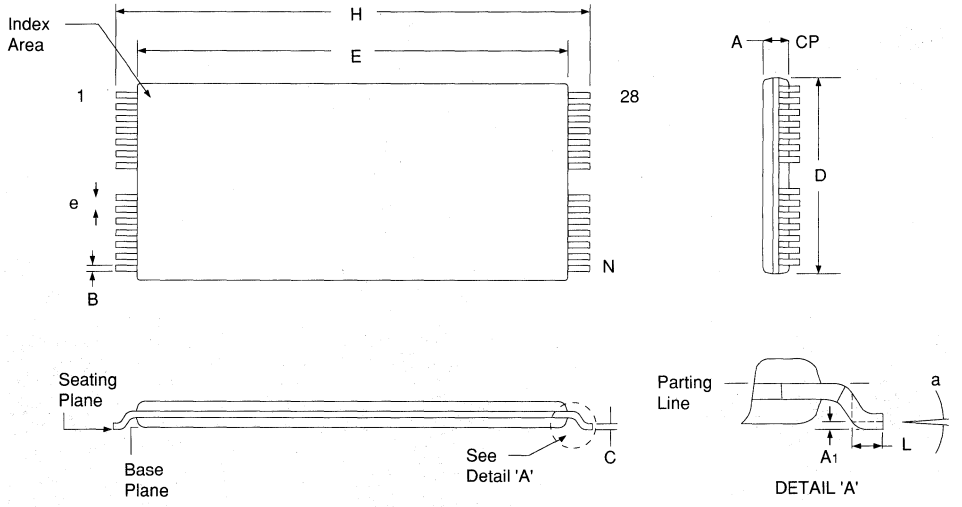
3. "D" and "E" are reference datums and do not include mold flash or protrusions.
Mold flash or protrusions shall not exceed .005 per side.

4. A visual index feature must be located within the crosshatched area to indicate pin 1 position.

5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (TSOP 8 x 20mm)

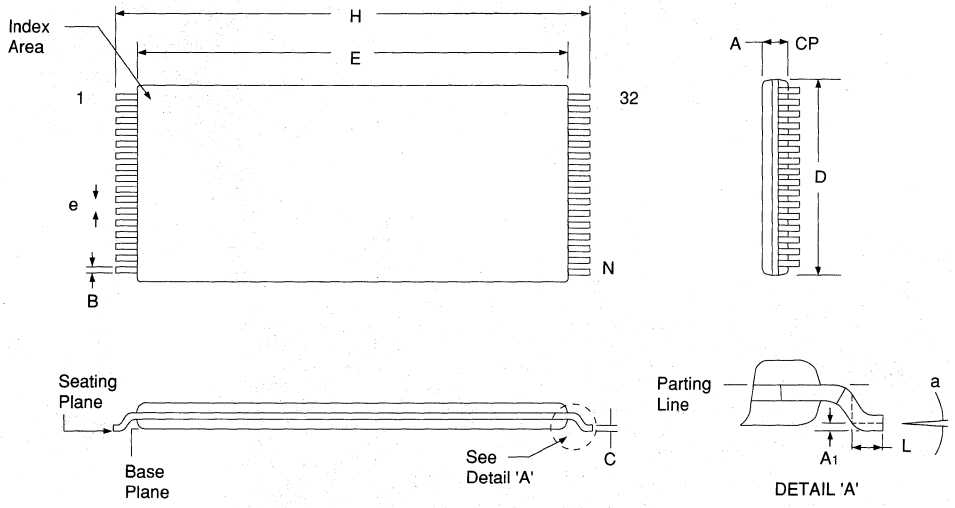


Package Group: Plastic TSOP (TS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	-	1.20		-	.047	
A_1	0.00	0.15		.000	.006	
B	0.15	0.25		.006	.010	
C	0.10	0.20		.004	.008	
D	7.90	8.20		.307	.323	
E	18.30	18.50		.720	.728	
e	.50	-	Typical	.020	-	Typical
H	19.80	20.20		.780	.795	
	-	-		-	-	
L	0.40	0.60		.016	.024	
N	28	28		28	28	
CP	-	0.102		-	.004	

8

Packaging Diagrams and Parameters

Package Type: 32-Lead Plastic Surface Mount (TSOP 8 x 20mm)



Package Group: Plastic TSOP (TS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	-	1.20		-	.047	
A_1	0.00	0.15		.000	.006	
B	0.15	0.25		.006	.010	
C	0.10	0.20		.004	.008	
D	7.90	8.20		.307	.323	
E	18.30	18.50		.720	.728	
e	.50	-	Typical	.020	-	Typical
H	19.80	20.20		.780	.795	
	-	-		-	-	
L	0.40	0.60		.016	.024	
N	28	28		28	28	
CP	-	0.102		-	.004	

Packaging Diagrams and Parameters

Plastic Metric Flat Pack Family

Symbol List for Metric Plastic Quad Flat Pack Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min and max lead positions measured at the guage plane
A	Distance between seating plane to highest point of body
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body
b	Width of terminals
C	Thickness of terminals
D_1/E_1	Largest overall package parameter including leads
D/E	Largest overall package parameter including leads
D_3/E_3	Center of end lead to center of end lead
e	Linear spacing of true minimum lead position center line to center line
L	Length of terminal for soldering to a substrate
N	Total number of potentially useable lead positions
CP	Seating plane coplanarity

Notes

1. All dimensioning and tolerancing conform to ANSI Y14, BM-1582.
2. Datum Plane -H- is located at bottom of hold parting line and coincident with bottom of lead, where lead exits body.
3. Datums A-B and -D- to be determined at Datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include hold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 do not include hold mismatch and are determined at Datum Plane -H-.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. These dimensions to be determined at Datum plane -H-.
8. All dimensions in millimeters.
9. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.
10. Exact shape of this feature is optional.
11. N is the number of leads.
12. Controlling parameters: milimeters
13. All packages are gull wing lead form.

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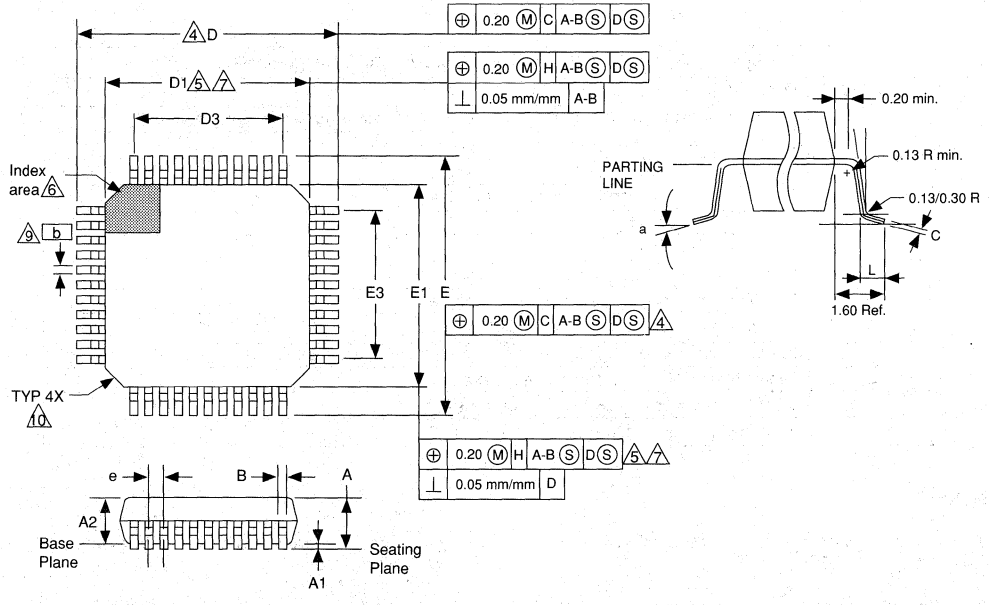
Packaging Diagrams and Parameters

Package Type: 44-Lead Plastic Surface Mount (MQFP 10x10mm Body 1.6/0.5mm Lead Form)



Package Group: Plastic MQFP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°		0°	7°	
A	2.00	2.35		0.0787	0.0925	
A_1	0.05	0.25		0.0019	0.0098	
A_2	1.95	2.10		0.768	0.0827	
b	0.30	0.45	Typical	0.0118	0.0177	Typical
C	0.15	0.18		.006	.007	
D	12.95	13.45		0.510	0.530	
D_1	9.90	10.10		0.390	0.398	
D_3	8.00	8.00	Reference	0.315	0.315	Reference
E	12.95	13.45		0.510	0.530	
E_1	9.90	10.10		0.390	0.398	
E_3	8.00	8.00	Reference	.315	.315	Reference
e	0.80	0.80		.0314	.0314	
L	0.65	0.95		.0256	.0374	
N	44	44		44	44	
CP	0.102			.004		

APPENDIX
OFFICE LOCATIONS

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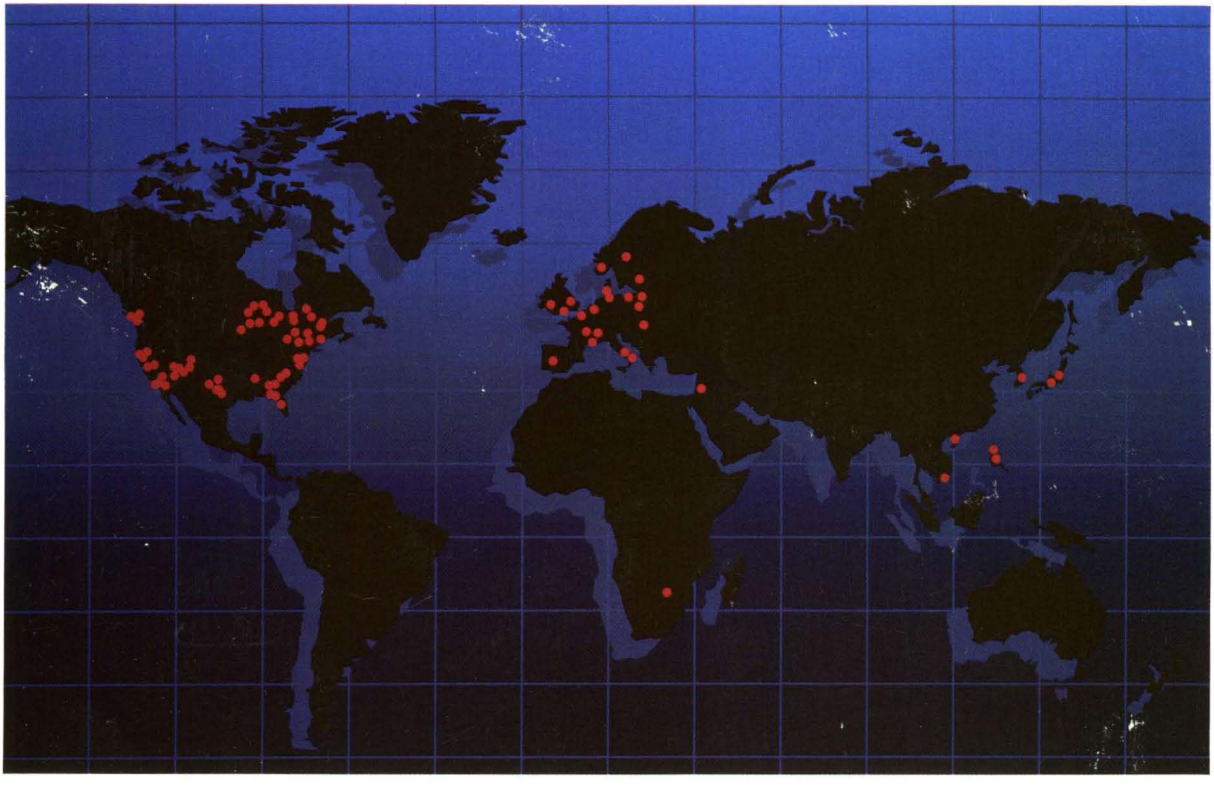

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