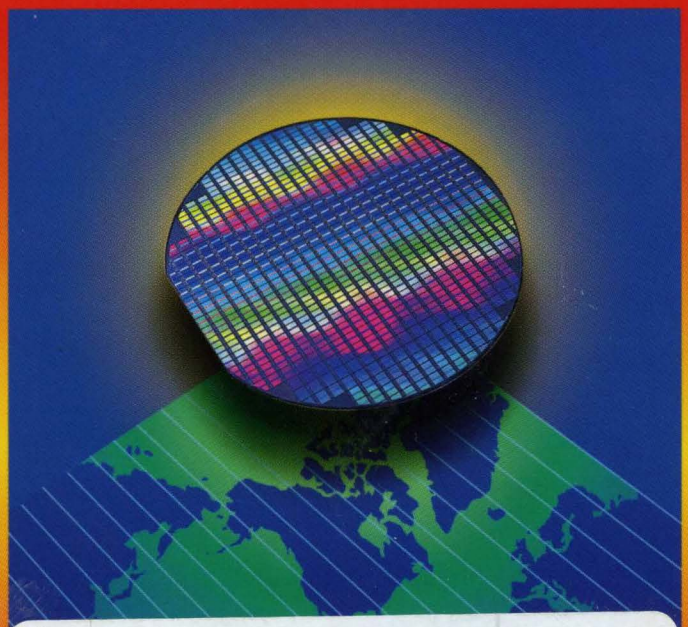
NON-VOLATILE MEMORY
PRODUCTS DATA BOOK

1995
1996

MICROCHIP

NON-VOLATILE MEMORY PRODUCTS DATA BOOK



THE EMERGING WORLD STANDARD™

1995/1996

MICROCHIP

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Microchip Non-Volatile Memory Products Data Book

1995/1996 Edition

SERVING A COMPLEX AND COMPETITIVE WORLD WITH FIELD-PROGRAMMABLE EMBEDDED CONTROL SYSTEM SOLUTIONS

May 1995 /DS00157A

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Marking	Description
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Preliminary	This is preliminary information on new products in production but not yet fully characterized. The specifications in these data sheets are subject to change without notice. Before you finalize your design, please ensure that you have the most current revision of the data sheet by contacting your Microchip sales office, representative or distributor.
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MICROCHIP

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SECTION 1
MICROCHIP TECHNOLOGY INC. COMPANY PROFILE

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Microchip Technology Inc.

Company Profile

INTRODUCTION TO *THE EMBEDDED CONTROL SOLUTIONS COMPANY*™

Microchip Technology's mission is to offer leadership semiconductor products for embedded control system applications. To do this we have focused our technology, engineering, manufacturing and marketing resources on two synergistic product lines: 8-bit PIC16/17 microcontrollers and Serial EEPROMS. These product lines provide the solutions to many of the problems facing designers of embedded control systems.

We publish the Microchip *Data Book* and *Embedded Control Handbook* to assist our customers, existing and new, in their efforts to design and produce state-of-the-art embedded control systems.

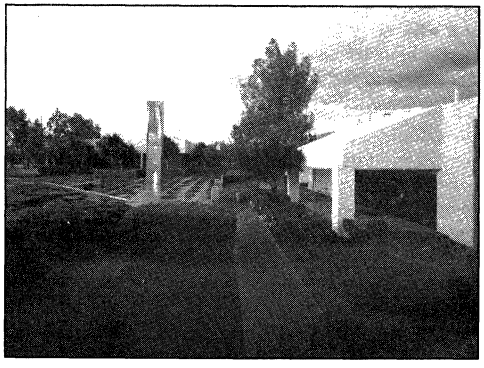
HIGHLIGHTS

Inside Microchip Technology you'll find:

- A focus on providing high-performance, cost-effective, field-programmable embedded control solutions
- An experienced executive team focused on innovation and committed to listening to our customers
- 8-bit RISC field-programmable microcontrollers and supporting logic products
- Serial and Parallel EEPROMs and EPROMs
- A variety of end-user Application-Specific Standard Products
- Fully integrated manufacturing capabilities
- A global network of manufacturing and customer support facilities
- A unique corporate culture dedicated to continuous improvement
- Distributor network support worldwide including certified distribution FAEs

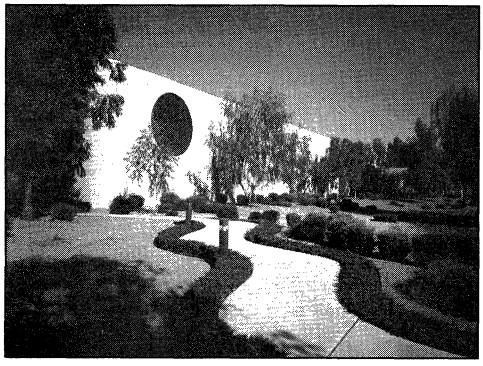
BUSINESS SCOPE

Microchip Technology Inc. manufactures and markets a variety of VLSI CMOS semiconductor components to support the market for cost-effective embedded control solutions. In particular, the company specializes in highly integrated, field-programmable RISC microcontrollers, application-specific standard products and related non-volatile memory products to meet growing market requirements for high performance, yet economical embedded control capability in products. Microchip's products feature the industry's most economical OTP (one-time programmable), reprogrammable EEPROM and ROM capability, along with the compact size, integrated functionality, ease of development and technical support so essential to timely and cost-effective product development by our customers.



Chandler, Arizona:

Company headquarters near Phoenix, Arizona; executive offices, R & D and wafer fabrication occupy this 142,000-square-foot facility. An additional 100,000 square foot adjacent facility is under construction with completion expected in mid-1995.



Tempe, Arizona:

Microchip's 170,000-square-foot wafer fabrication facility provides increased manufacturing capacity today and for the future.

MICROCHIP

- Mission Statement -

Microchip Technology Incorporated is a leading supplier of field-programmable embedded control solutions by providing RISC microcontrollers and related non-volatile memory products. In order to contribute to the ongoing success of customers, shareholders and employees, our mission is to focus resources on high value, high quality products and to continuously improve all aspects of our business, providing a competitive return on investment.

- Guiding Values -

Customers Are Our Focus: We establish successful customer partnerships by exceeding customer expectations for products, services and attitude. We start by listening to our customers, earning our credibility by producing quality products, delivering comprehensive services and meeting commitments. We believe each employee must effectively serve their internal customers in order for Microchip's external customers to be properly served.

Quality Comes First: We will perform correctly the first time, maintain customer satisfaction and measure our quality against requirements. We practice effective and standardized improvement methods, such as statistical process control to anticipate problems and implement root cause solutions. We believe that when quality comes first, reduced costs follow.

Continuous Improvement Is Essential: We utilize the concept of "Vital Few" to establish our priorities. We concentrate our resources on continuously improving the Vital Few while empowering each employee to make continuous improvements in their area of responsibility. We strive for constructive and honest self-criticism to identify improvement opportunities.

Employees Are Our Greatest Strength: We design jobs and provide opportunities promoting employee teamwork, productivity, creativity, pride in work, trust, integrity, fairness, involvement, development and empowerment. We base recognition, advancement and compensation on an employee's achievement of excellence in team and individual performance. We provide for employee health and welfare by offering competitive and comprehensive employee benefits.

Products And Technology Are Our Foundation: We make ongoing investments and advancements in the design and development of our manufacturing process, device, circuit, system and software technologies to provide timely, innovative, reliable and cost effective products to support current and future market opportunities.

Total Cycle Times Are Optimized: We focus resources to optimize cycle times to our internal and external customers by empowering employees to achieve efficient cycle times in their area of responsibility. We believe that cycle time reduction is achieved by streamlining processes through the systematic removal of barriers to productivity.

Safety Is Never Compromised: We place our concern for safety of our employees and community at the forefront of our decisions, policies and actions. Each employee is responsible for safety.

Profits And Growth Provide For Everything We Do: We strive to generate and maintain competitive rates of company profits and growth as they allow continued investment for the future, enhanced employee opportunity and represent the overall success of Microchip.

Communication Is Vital: We encourage appropriate, honest, constructive, and ongoing communication in company, customer and community relationships to resolve issues, exchange information and share knowledge.

Suppliers, Representatives, And Distributors Are Our Partners: We strive to maintain professional and mutually beneficial partnerships with suppliers, representatives, and distributors who are an integral link in the achievement of our mission and guiding values.

Professional Ethics Are Practiced: We manage our business and treat customers, employees, shareholders, investors, suppliers, distributors, representatives, community and government in a manner that exemplifies our honesty, ethics and integrity. We recognize our responsibility to the community and are proud to serve as an equal opportunity employer.

MARKET FOCUS

Microchip targets selected markets where our advanced designs, progressive process technology and industry-leading product performance enable us to deliver decidedly superior performance. The company has positioned itself to maintain a dominant role as a supplier of high-performance, field-programmable microcontrollers and associated memory and logic products for embedded control applications which are found throughout the consumer, automotive, telecommunication, office automation and industrial control markets.

FULLY INTEGRATED MANUFACTURING

Microchip delivers fast turnaround and consistent quality through total control over all phases of production. Research and development, design, mask making, wafer fabrication, and the major part of assembly and quality assurance testing are conducted at facilities wholly-owned and operated by Microchip. Our integrated approach to manufacturing along with rigorous use of advanced statistical process control (SPC) and a continuous improvement culture has resulted in high and consistent yields which have positioned Microchip as a quality leader in its global markets. Microchip's unique approach to SPC provides customers with excellent costs, quality, reliability and on-time delivery.

A GLOBAL NETWORK OF PLANTS AND FACILITIES

Microchip is a global competitor providing local service to the world's technology centers. The Company's focal point is its design and technology advancement facility in Chandler, Arizona. Product and technology development is located here, along with front-end wafer fabrication and wafer probe and sort.

In 1994, Microchip purchased a second wafer fabrication facility in Tempe, Arizona – thirteen miles from its Chandler, Arizona, headquarters. The additional 170,000 square foot facility is meeting production requirements beyond those which could be produced in Microchip's Chandler wafer facility. Assembly and test facilities predominantly located in Kaohsiung, Taiwan, and Bangkok, Thailand, house the technology and assembly and test equipment necessary for modern plastic and ceramic packaging.

Sales and application offices are located in key cities throughout the Americas, Asia/Pacific, Japan and Europe. Offices are staffed to meet the high quality expectations of our customers, and can be accessed for technical and business support.

EMBEDDED CONTROL OVERVIEW

Unlike "processor" applications such as personal computers and workstations, the computing or controlling elements of embedded control applications are buried inside the application. The user of the product is only concerned with the very top-level user interface (such as keypads, displays and high-level commands). Very rarely does an end-user know (or care to know) the embedded controller inside (unlike the conscientious PC users, who are intimately familiar not only with the processor type, but also its clock speed, DMA capabilities and so on).

It is, however, most vital for designers of embedded control products to select the most suitable controller and companion devices. Embedded control products are found in all market segments: consumer, commercial, PC peripherals, automotive, telecommunications (including fast-emerging personal telecommunication products) and industrial. Most often embedded control products must meet special requirements: cost-effectiveness, low power, small footprint and a high level of system integration.

Typically, most embedded control systems are designed around a microcontroller which integrates on-chip program memory, data memory (RAM) and various peripheral functions, such as timers and serial communication. In addition, these systems also usually require Serial EEPROM memories, display drivers, keypads, small displays, etc.

Microchip Technology has established itself as a leading supplier of field-programmable embedded control solutions. The combination of high-performance microcontrollers from the PIC17CXX, PIC16CXX and PIC16C5X families, along with industry leading nonvolatile memory products provides the basis for this leadership.

Microchip is committed to continuous innovation and improvement in design, manufacturing and technical support to provide the best possible embedded control solutions to you.

MICROCONTROLLERS

PIC16/17 microcontrollers from Microchip combine high performance, low cost and small package size, offering the best price/performance ratio in the industry. Over 200 million of these devices have been used in cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

PIC16/17 MICROCONTROLLER OVERVIEW AND ROADMAP

Microchip offers three families of 8-bit microcontrollers to best fit your needs:

- PIC16C5X: Base-Line 8-bit Family
- PIC16CXX: Mid-Range 8-bit Family
- PIC17CXX: High-End 8-bit Family

All families offer One-Time-Programmable, low-voltage and low-power options, as well as various packaging options. Selected members are available in ROM and reprogrammable versions.

The widely-accepted PIC16C5X, PIC16CXX and PIC17CXX families are the industry's only 8-bit microcontrollers using a high-speed RISC architecture. Microchip pioneered the use of RISC architecture to obtain high speed and instruction efficiency.

PIC16C5X: BASE-LINE FAMILY

PIC16C5X is the well established base-line family offering the most cost-effective solution. This PIC16C5X products have a 12-bit wide instruction set and are currently offered in 18-, 20- or 28-pin packages. In SOIC and SSOP packaging options, these are the smallest footprint controllers. Low-voltage operation down to 2.0V makes this family ideal for battery operated applications.

The PIC16C5X base-line family is in high-volume production, shipping in the range of one million units per week, and has achieved more than twenty-five thousand design wins worldwide.

PIC16CXX: MID-RANGE FAMILY

PIC16CXX mid-range family offers a wide-range of options, from 18-pin to 44-pin packages as well as low to high level of peripheral integration. This family has a 14-bit wide instruction set, interrupt handling capability and deeper 8-level hardware stack. The PIC16CXX family provides the performance and versatility to meet the requirements of more demanding, yet cost-sensitive, mid-range 8-bit applications.

The PIC16CXX mid-range family is rapidly gaining acceptance with several of its members introduced: PIC16C61, PIC16C62, PIC16C63, PIC16C64, PIC16C65, PIC16C620, PIC16C621, PIC16C622, PIC16C71, PIC16C73, PIC16C74 and PIC16C84.

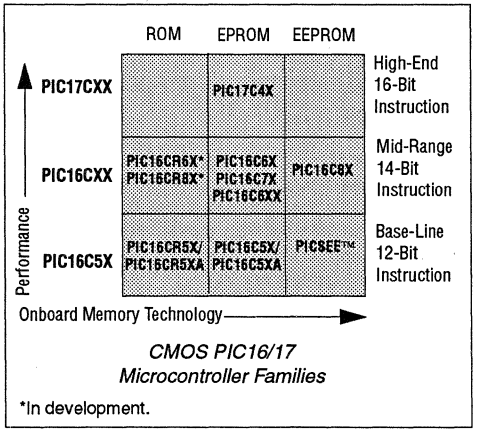
PIC17CXX: HIGH-END FAMILY

The PIC17CXX high-performance family offers the world's fastest execution performance of any 8-bit microcontroller family in the industry. The PIC17CXX family extends the PIC16/17 microcontroller's high-performance RISC architecture with a 16-bit instruction word, enhanced instruction set and powerful vectored interrupt handling capabilities. A powerful array of precise on-chip peripheral features provide the performance for the most demanding 8-bit applications.

Currently, two members of the PIC17CXX family have been announced. A third member will be available soon.

Current PIC16/17 microcontroller product families include advanced features such as sophisticated timers, embedded Analog-to-Digital Converter, extended instruction/data memory, inter-processor communication (I^2C™ bus, SPI and USARTs) and ROM, RAM, EPROM and EEPROM memories.

Both PIC16CXX and PIC17CXX families are supported by user-friendly development systems including assembler, software simulator, C Compiler, fuzzy logic development software, programmers and in-circuit emulators.



CMOS PIC16/17 Microcontroller Families

*In development.

FIGURE 1: PIC16/17 MICROCONTROLLER MIGRATION PATH

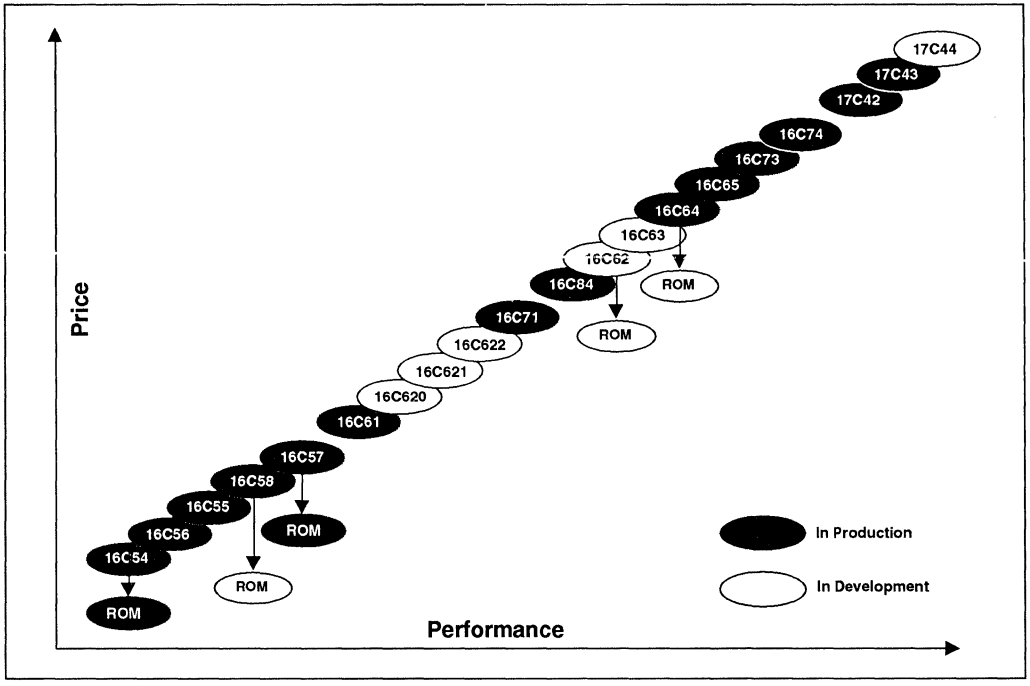


FIGURE 2: PIC16/17 SYNERGISTIC DEVELOPMENT TOOLS

Development Tool	Name	PIC16C5X	PIC16CXX	PIC17CXX
Assembler	MPASM	✔	✔	✔
Software Simulator	MPSIM	✔	✔	✔
C Compiler*	MP-C	✔	✔	✔
Entry Level Development Kit	PICSTART®	✔	✔	Planned
Universal Programmer	PRO MATE™	✔	✔	✔
Universal In-Circuit Emulator	PICMASTER®	✔	✔	✔
Fuzzy Logic Development Tool	fuzzyTECH®-MP	✔	✔	✔

* Available from Byte Craft Limited in Canada.

PIC16/17 NAMING CONVENTION

The PIC16/17 architecture offers users a wide range of cost/performance options of any 8-bit microcontroller family. In order to identify the families, the following naming conventions have been applied to the PIC16/17 microcontrollers.

TABLE 1: PIC16/17 NAMING CONVENTION

Family		Architectural Features	Name	Technology	Products
PIC16C5X	Base-Line 8-bit Microcontroller Family	• 12-bit wide instruction set • DC - 20 MHz clock speed • 200 ns instruction cycle	PIC16C5X PIC16C5XA (Note 1)	OTP program memory, digital only	PIC16C54 PIC16C54A PIC16C55 PIC16C56 PIC16C57 PIC16C58A
			PIC16CR5X PIC16CR5XA (Note 1)	ROM program memory, digital only	PIC16CR54 PIC16CR57A PIC16CR58A
PIC16CXX	Mid-Range 8-bit Microcontroller Family	• 14-bit wide instruction set • Internal/external interrupts • DC - 20 MHz clock speed (Note 3) • 200 ns instruction cycle (@ 20 MHz)	PIC16C6X	OTP program memory, digital	PIC16C61 PIC16C62 PIC16C63 PIC16C64 PIC16C65
			PIC16CR6X	ROM program memory, digital only	Planned
			PIC16C62X	OTP program memory with comparators	PIC16C620 PIC16C621 PIC16C622
			PIC16C7X	OTP program memory, with analog functions (e.g. A/D)	PIC16C71 PIC16C73 PIC16C74
			PIC16C8X	EEPROM program and data memory	PIC16C84
			PIC16CR8X	ROM program and EEPROM data memory	Planned
PIC17CXX	HIgh-End 8-bit Microcontroller Family	• 16-bit wide instruction set • Internal/external interrupts • DC - 25 MHz clock speed • 160 ns instruction cycle	PIC17C4X	OTP program memory, digital only	PIC17C42 PIC17C43 PIC17C44
			PIC17CR4X	ROM program memory, digital only	Planned

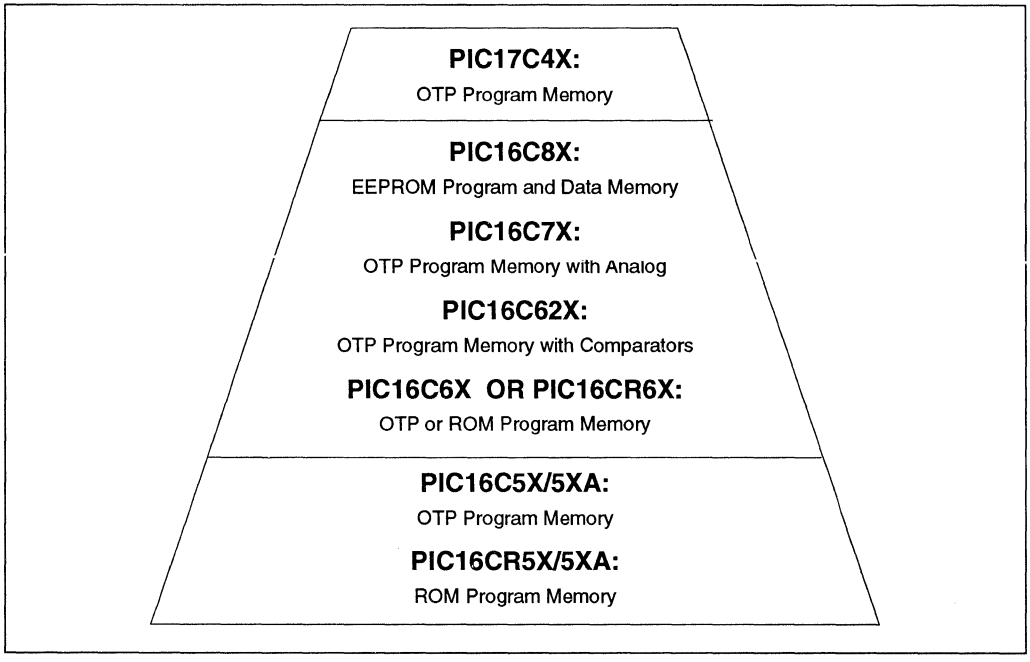
Note 1: "A" designates a more advanced process technology, generally offering customers the benefits of lower power, higher speed, etc. (example: PIC16C54, PIC16C54A). Sometimes it designates additional functions such as the addition of Brown-out detect.

Note 2: The numbering system within each family is not necessarily significant.

Note 3: The maximum clock speed for some devices is less than 20 MHz.

Please check with your local Microchip distributor, sales representative or sales office for the latest product information.

FIGURE 3: PIC16/17 8-BIT MCU FAMILY



THE ADVANTAGE OF FIELD PROGRAMMABILITY

The PIC16/17 microcontroller family provides a unique combination of a high-performance RISC processor with cost-effective One-Time-Programmable (OTP) technology. Cost-effective OTP provides many benefits to the user at prices which can be comparable to competing ROM solutions. The benefits include: 1) quick time-to-market, 2) ease of code changes, 3) ability to provide adaptable solutions to end-customer requirements, 4) ability to meet upside potential via inventory positions at Microchip or worldwide distribution, 5) reduced scrappage in manufacturing, 6) reduced inventory in manufacturing, and 7) reduced work-in-process liability.

For most manufacturers, getting the product to market quickly has become the number one goal as global markets have become more competitive. Time-to-market puts pressure on all functions within the manufacturing process: development, purchasing, production, and marketing and sales. Field-programmable OTP technology streamlines the process for all stages in the product life cycle.

In the early product development stages, a programmable microcontroller allows much of the functionality to be implemented in software which can be modified more easily than hardware-only solutions.

In the manufacturing stage, the compression of the product life cycle curve puts pressure on the management of inventory and manufacturing cycle times. Minimizing inventory reduces the ability to meet upside demand. Using a traditional ROM-based microcontroller limits the ability to respond to the market with product enhancements or semi-customized products for specific customers. Using the standard OTP-based PIC16/17 microcontroller solves all these issues. Inventory can be managed effectively by using the same device in several systems. Costs can be reduced due to volume purchasing. Upsides can be met from either safety stock, directly from Microchip, or local distributors who regularly inventory all the PIC16/17 microcontroller devices. A sudden decline in demand means no work-in-process ROM-based inventory and any excess safety stock can be consumed by the other products using the same standard device.

OTP is the 'Flexible Manufacturing' technology of the microcontroller world. As competition intensifies, the demand for customer-specific products increases. Having the ability to change (for example, the appearance of LCD displays or add extra features in a timely manner) can be a key competitive advantage. Programming the OTP device on the manufacturing floor allows easy customizing and internal tracking of the devices for each specific customer. Customization can significantly increase the overall product life cycle to provide better return on investment and help minimize the threat of competition.

DEVELOPMENT SYSTEMS

Microchip is committed to providing useful and innovative solutions to your embedded system designs. Among the support products offered are the PICMASTER® real-time universal in-circuit emulator running under Windows™ environment. PICMASTER is designed to provide product development engineers with an optimized design tool for developing target applications. This universal in-circuit emulator provides a complete microcontroller design tool set for all microcontrollers in the PIC16C5X, PIC16CXX and PIC17CXX families. PRO MATE™, the full-featured device programmer, enables you to quickly and easily program user software into PIC16C5X, PIC16CXX and PIC17CXX CMOS microcontrollers. The PRO MATE operates as a stand-alone unit or in conjunction with a PC compatible host system. The PICSTART® development kit, a low-cost development system for the PIC16C5X/16CXX families of microcontrollers, includes an assembler for code development, a simulator for debug and a development programmer board. PICSEEKIT and PICSEESTART provide product development engineers with a cost-effective and timely design tool solution for the MTA8XXXX family of ASSP products.

The Serial EEPROM Designer's Kit includes everything necessary to read, write, erase or program special features of any Microchip Serial EEPROM products including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

The TrueGauge™ development tool supports system development with the MTA11200 TrueGauge Intelligent Battery Management IC.

SOFTWARE SUPPORT

Microchip's PIC16/17 microcontrollers families are supported by an assembler, compiler, software simulator and fuzzy logic development software. MPASM is a universal macro assembler supporting Microchip's entire product line of microcontrollers. MPSIM, a discrete event software simulator, is designed to imitate operation of PIC16C5X, PIC16CXX and PIC17CXX microcontrollers. It allows the user to debug software that will use any of these microcontrollers.

A full-featured C Compiler and Fuzzy Logic support are also available for all three microcontroller families.

Microchip endeavors at all times to provide the best service and responsiveness possible to its customers. The Microchip Systems Bulletin Board Service (BBS) is one service to facilitate this process. It's a multi-faceted tool that can provide you with information on a number of different topics. Special Interest Groups available through the BBS can provide you with the opportunity to discuss issues and topics of interest with others that share your interest or questions. The BBS is regularly used to distribute technical information, application notes source codes, errata sheets, bug reports, interim patches for Microchip systems products and user contributed files for distribution.

APPLICATION-SPECIFIC STANDARD PRODUCTS (ASSPs)

Microchip's Application-Specific Standard Products (ASSP) provide value-added embedded control solutions by combining PIC16/17 microcontroller architecture, non-volatile memory and innovative software technology for vertical applications. These products incorporate technology that offers a complete solution that is both unique to the customer and standard in manufacture to Microchip. In addition, Microchip ASSPs reduce or remove the barriers for customers to use Microchip solutions in their products through the use of software embedded in secure OTP- or ROM-based microcontrollers. The family is packaged to provide the highest integration to the customer at the best overall system cost.

The MTA11200 family is the most accurate and most integrated battery management and charging solution available today. The TrueGauge family incorporates Microchip/SPAN patented technology which digitally integrates battery charge and discharge current to provide an accurate (>97% typical) state of charge indication. The family operates with NiCd and NiMH and lead acid battery packs from 3 VDC to 25 VDC. These products are ideal for portable PC, cellular phone and portable consumer product applications.

The MTA14000 programmable Intelligent Battery Management IC allows engineers to design intelligent controllers for smart batteries, battery chargers, battery status monitoring, uninterruptible power supplies, HVAC and other data acquisition and processing required for managing energy. The MTA14000's programmable 4K words of program memory and 192 bytes of RAM allows it to support any battery technology including Li Ion, NiMH, NiCd, Pb acid, Zinc Air. In addition, the products I^2C port enables any system OEM, battery pack VAR and battery manufacturer to design, build and market SBD-compliant products supporting the System Management Bus™ standard.

The MTE1122 Energy Management Controller combines Microchip's proprietary PIC16/17 8-bit RISC microcontroller technology with a unique, patent pending power management firmware algorithm in a single package. This device, by monitoring and controlling the supply requirements into an AC induction motor, effectively reduces the power consumed by the motor. The MTE1122 is available in both plastic DIP and space-saving SOIC packages, and operates over commercial and industrial ranges.

Ease-of-use, low voltage and low cost make the MTA41XXX mouse and trackball MCU firmware solutions ideal for implementing new designs for both PCs and Apple® computers. The products in the MTA41XXX family are 18-lead, low-power CMOS microcontroller ICs combined with application-specific software. By adding a few external components, the user can easily realize a complete mouse or trackball system.

The MTA8XXXX PICSEE™ family of cost-effective system solutions integrates PIC16/17 microcontrollers with EEPROM technology. These PICSEE devices are ideally suited for automotive security, keyless entry, remote control, data acquisition and telecommunication applications. The combined product assembly techniques provide the user the highest performance solution in a compact and cost-effective package.

Future ASSP products will include advanced features such as mixed analog and digital capability as well as an ever broadening family of turnkey software solutions for the embedded control market.

SERIAL EEPROM OVERVIEW

Microchip offers one of the broadest selections of CMOS Serial EEPROMs on the market for embedded control systems. Serial EEPROMs are available in a variety of densities, operating voltages, bus interface protocols, operating temperature ranges and space saving packages.

Densities:

Currently range from 1K to 64K with higher density devices in development.

Bus Interface Protocols:

All major protocols are covered: 2-wire, 3-wire and 4-wire.

Operating Voltages:

In addition to standard 5V devices there are two low voltage families. The "LC" devices operate down to 2.5V, while the breakthrough "AA" family operates, in both read and write mode, down to 1.8V, making these devices highly suitable for alkaline and NiCad battery powered applications.

Temperature Ranges:

Like all Microchip devices, Serial EEPROMs are offered in Commercial (0°C to 70°C), Industrial (-40°C to 85°C) and Automotive (-40°C to 125°C) operating temperature ranges.

Packages:

The focus is on small packages. Small footprint packages include: 8-lead DIP, 8-lead SOIC in JEDEC and EIAJ body widths, and 14-lead SOIC. The SOIC comes in two body widths; 150 mil and 207 mil.

In February 1995, Microchip announced its 10 million Erase/Write cycle guarantee - an endurance breakthrough unmatched by its competitors. The Company has also developed the world's first 64K Smart Serial EEPROM which provided four times the speed, four times the memory and four times the features of any competitive 2-wire Serial EEPROM. Device densities range from 256 bits up to 64K bits. Another first is the 24LC21, the only single chip DDC1/DDC2™-compatible solution for plug-and-play video monitors.

Microchip is a high-volume supplier of Serial EEPROMs to all the major markets worldwide including consumer, automotive, industrial, computer and communications. To date, more than 300 million units have been produced. Microchip continues to develop new Serial EEPROM solutions for embedded control applications.

Microchip's erase/write cycle endurance is among the best in the world, and only Microchip offers unique and powerful development tools such as the Total Endurance disk. This mathematical software model is an innovative tool used by system designers to optimize Serial EEPROM performance and reliability within the application.

PARALLEL EEPROM OVERVIEW

CMOS Parallel EEPROM devices from Microchip are available in 4K, 16K and 64K densities. The manufacturing process used for these EEPROMs ensures 10,000 to 100,000 write and erase cycles typical. Data retention is more than 10 years. Fast write times are less than 200 µs. These EEPROMs work reliably under demanding conditions and operate efficiently at temperatures from –40°C to +85°C. Microchip's expertise in advanced SOIC, TSOP and VSOP surface mount packaging supports our customers' needs in space-sensitive applications.

Typical applications include computer peripherals, engine control, pattern recognition and telecommunications.

OTP EPROM OVERVIEW

Microchip's CMOS EPROM devices are produced in densities from 64K to 512K. High-speed EPROMs have access times as low as 55 ns. Typical applications include computer peripherals, instrumentation and automotive devices. Microchip's expertise in surface mount Packaging on SOIC, TSOP and VSOP packages led to the development of the Surface Mount one-time-programmable (OTP) EPROM market where Microchip is a leading supplier today. Microchip is also a leading supplier of low-voltage EPROMs for battery powered applications.

EASE OF PRODUCTION UTILIZING QUICK TURN PROGRAMMING (QTP) AND SERIALIZED QUICK TURN PROGRAMMING (SQTP℠)

Recognizing the needs of high-volume manufacturing operations, Microchip has developed two programming methodologies which make the OTP products as easy to use in manufacturing as they are efficient in the system development stage.

Quick Turn Programming allows factory programming of OTP product prior to delivery to the system manufacturing operation. PIC16/17, EPROM and Serial EEPROM products can be automatically programmed with the users program during the final stages of the test operation at Microchip's assembly and test operations in Philippine Islands, Taiwan and Thailand. This low-cost programming step allows the elimination of programming during system manufacturing and essentially allows the user to treat the PIC16/17 and memory products as custom ROM products. With one- to four-week lead times on QTP product, the user no longer needs to plan for the extended ROM masking lead times and masking charges associated with custom ROM products. This capability, combined with the off-the-shelf availability of standard OTP product, ensures the user of product availability and the ability to reduce his time-to-market once product development has been completed.

Unique in the 8-bit microcontroller market is Microchip's ability to enhance the QTP capability with Serialized Quick Turn Programming (SQTP). SQTP allows for the programming of devices with unique, random or serialized identification codes. As each PIC16/17 device is programmed with the customers program code, a portion of the program memory space can be programmed with a unique code, accessible from normal program memory, which will allow the user to provide each device with a unique identification. This capability is ideal for embedded systems applications where the transmission of key codes or identification of the device as a node within a network are essential. Taking advantage of this capability allows the system designer to eliminate the requirement for expensive off-chip code implementation using DIP switches or nonvolatile memory components. The SQTP offering, pioneered by Microchip, provides the embedded systems designer with a low cost means of putting a unique and custom device into every system or node.

FUTURE PRODUCTS AND TECHNOLOGY

New process technology is constantly being developed for microcontroller, ASSP, EEPROM and high-speed EPROM products. Advanced process technology modules and products are being developed that will be integrated into present product lines to continue to achieve a range of compatible processes. Current production technology utilizes lithography dimensions down to 0.9 microns.

Microchip's current research and development activities focus on the design of new microcontroller and specialty memory products, ASSPs, new development systems, and software and application-specific software libraries. The Company is also developing new design and process technology to achieve further cost reductions and performance improvements in existing products.

As of September 1994, Microchip owned 15 U.S. patents and three foreign patents, expiring on various dates beginning in the year 2001 and ending in the year 2011, and had an additional 20 U.S. patent applications and six foreign patent applications pending. The Company intends to continue to seek, and expand its efforts to acquire, patents on its inventions used in its products and manufacturing processes.

Equipment is continually updated to bring the most sophisticated process, CAD and testing tools online. Cycle times for new technology development are continuously reduced by using in-house mask generation, a high-speed pilot line within the manufacturing facility and continuously improving methodologies.

More advanced technologies are under development, as well as advanced CMOS RISC-based microcontroller, ASSP and CMOS EEPROM and EPROM products. Objective specifications for new products are developed by listening to our customers and by close cooperation with our many customer-partners worldwide.

SECTION 2
NON-VOLATILE MEMORY PRODUCT SELECTION AND CROSS REFERENCE GUIDES

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Serial EEPROM Selection Guide

CMOS SERIAL EEPROMS

I²C™ Serial EEPROMs

Device	Compatibility	Density/ Organization	Page Buffer	Write Speed	Max Clock Freq.	Endur-ance	Temp Range	# Pins	Package Types	Operating Voltage
24AA01	Industry	1K bits (128 x 8)	8 bytes	10 ms	400 KHz	10M	C	8	P,SN,SM	1.8V - 5.5V
24AA02	Industry	2K bits (256 x 8)	8 bytes	10 ms	400 KHz	1M*	C	8	P,SN,SM	1.8V - 5.5V
24AA04	Industry	4K bits (512 x 8)	16 bytes	10 ms	400 KHz	1M*	C	8,14	P,SN,SM,SL	1.8V - 5.5V
24AA08	Industry	8K bits (1K x 8)	16 bytes	10 ms	400 KHz	1M*	C	8,14	P,SN,SM,SL	1.8V - 5.5V
24AA16	Industry	16K bits (2K x 8)	16 bytes	10 ms	400 KHz	10M	C	8,14	P,SN,SL	1.8V - 5.5V
24AA164	Atmel, Xicor	16K bits (2K x 8)	16 bytes	10 ms	400 KHz	10M	C	8	P,SN	1.8V - 5.5V
24AA32	Sole Source	2K bits (4K x 8)	64 bytes	5 ms/pg	100 kHz	10M/100K	C	8	P,SM	1.8V - 5.5V
24LC01B	Industry	1K bits (128 x 8)	8 bytes	10 ms	400 KHz	10M	C,I	8	P,SN,SM	2.5V - 5.5V
24LC02B	Industry	2K bits (256 x 8)	8 bytes	10 ms	400 KHz	1M*	C,I	8	P,SN,SM	2.5V - 5.5V
24LC04B	Industry	4K bits (512 x 8)	16 bytes	10 ms	400 KHz	1M*	C,I	8,14	P,SN,SM,SL	2.5V - 5.5V
24LC08B	Industry	8K bits (1K x 8)	16 bytes	10 ms	400 KHz	1M*	C,I	8,14	P,SN,SM,SL	2.5V - 5.5V
24LC16B	Industry	16K bits (2K x 8)	16 bytes	10 ms	400 KHz	10M	C,I	8,14	P,SN,SL	2.5V - 5.5V
24LC164	Atmel, Xicor	16K bits (2K x 8)	16 bytes	10 ms	400 KHz	10M	C,I	8	P,SN	2.5V - 5.5V
24LC32	Sole Source	32K bits (4K x 8)	64 bytes	5 ms/pg	400 KHz	10M/100K	C,I	8	P,SM	2.5V - 6.0V
24C01A	Industry	1K bits (128 x 8)	2 bytes	1 ms/byte	100 KHz	1M	C,I,E	8	P,SN,SM	4.5V - 5.5V
24C02A	Industry	2K bits (128 x 8)	2 bytes	1 ms/byte	100 KHz	1M	C,I,E	8	P,SN,SM	4.5V - 5.5V
24C04A	Industry	4K bits (512 x 8)	8 bytes	1 ms/byte	100 KHz	1M	C,I,E	8,14	P,SN,SM,SL	4.5V - 5.5V
24C08B	Industry	8K bits (1K x 8)	16 bytes	10 ms	100 KHz	1M	E	8,14	P,SL,SN	4.5V - 5.5V
24C16B	Industry	16K bits (2K x 8)	16 bytes	10 ms	100 KHz	1M	E	8,14	P,SL,SN	4.5V - 5.5V
24C32	Sole Source	32K bits (4K x 8)	64 bytes	5 ms/pg	400 KHz	10M/100K	C,I	8	P,SM	4.5V - 5.0V
85C72	Philips	1K bits (128 x 8)	2 bytes	1 ms/byte	100 KHz	1M	C,I,E	8	J,P,SM	4.5V - 5.5V
85C82	Philips	2K bits (256 x 8)	2 bytes	1 ms/byte	100 KHz	1M	C,I,E	8	J,P,SM	4.5V - 5.5V
85C92	Philips	4K bits (512 x 8)	8 bytes	1 ms/byte	100 KHz	1M	C,I,E	8,14	P,J,SM,SL	4.5V - 5.5V

*Future: 10M

SERIAL EEPROMS

Microwire™ Serial EEPROMs

Device	Compatibility	Density/ Organization	Page Buffer	Write Speed	Max Clock Freq.	Endurance	Temp Range	# Pins	Package Types	Operating Voltage
93AA46	Atmel	1K bits (x8 or x16)	N/A	10 ms	2 MHz	1M*	C	8	P,SN,SM	1.8V - 5.5V
93AA56	Atmel	2K bits (x8 or x16)	N/A	10 ms	2 MHz	10M	C	8	P,SN,SM	1.8V - 5.5V
93AA66	Atmel	4K bits (x8 or x16)	N/A	10 ms	2 MHz	10M	C	8	P,SN,SM	1.8V - 5.5V
93LC46	Industry	1K bits (x8 or x16)	N/A	10 ms	2 MHz	1M*	C,I	8	P,SN,SM	2.0V - 6.0V
93LC56	Industry	2K bits (x8 or x16)	N/A	10 ms	2 MHz	10M	C,I	8,14	P,SN,SM,SL	2.0V - 6.0V
93LC66	Industry	4K bits (x8 or x16)	N/A	10 ms	2 MHz	10M	C,I	8,14	P,SN,SM,SL	2.0V - 6.0V
93LC46B	National	1K bits (64 x 16)	N/A	10 ms	2 MHz	1M*	C,I	8	P,SN,SM	2.0V - 6.0V
93LC56B	National	2K bits (128 x 16)	N/A	10 ms	2 MHz	10M	C,I	8	P,SN,SM	2.0V - 6.0V
93LC66B	National	4K bits (256 x 16)	N/A	10 ms	2 MHz	10M	C,I	8	P,SN,SM	2.0V - 6.0V
93C06	Industry	256 bits (16 x16)	N/A	1 ms/byte	1 MHz	1M	C,I,E	8	P,SN,SM	4.5V - 5.5V
93C46	Industry	1K bits (64 x 16)	N/A	1 ms/byte	1 MHz	1M	C,I,E	8	P,SN,SM	4.5V - 5.5V
93C56	Industry	2K bits (x8 or x16)	N/A	1 ms/byte	2 MHz	1M	C,I,E	8,14	P,SN,SM,SL	4.5V - 5.5V
93C66	Industry	4K bits (x8 or x16)	N/A	1 ms/byte	2 MHz	1M	C,I,E	8,14	P,SN,SM,SL	4.5V - 5.5V

*Future: 10M

Specialty Serial EEPROMs

Device	Compatibility	Density/ Organization	Page Buffer	Write Speed	Max Clock Freq.	Endurance	Temp Range	# Pins	Package Types	Operating Voltage
24AA174	Sole Source	16K bits (2K x 8) +16 bytes	16 bytes	10 ms	400 KHz	10M	C	8	P,SN	1.8V - 5.5V
24LC174	Sole Source	16K bits (2K x 8) +16 bytes	16 bytes	10 ms	400 KHz	10M	C,I	8	P,SN	2.5V - 5.5V
24LC21	Sole Source	1K bits (128 x 8)	8 bytes	10 ms	400 kHz	1M*	C,I	8	P,SN	2.5V - 5.5V
24AA65	Sole Source	64K bits (4K x 8)	64 bytes	5 ms/pg	100 KHz	10M/100K	C	8	P,SM	1.8V - 5.5V
24LC65	Sole Source	64K bits (4K x 8)	64 bytes	5 ms/pg	400 KHz	10M/100K	C,I	8	P,SM	2.5V - 6.0V
24C65	Sole Source	64K bits (4K x 8)	64 bytes	5 ms/pg	400 KHz	10M/100K	C,I	8	P,SM	4.5 - 5.5V
59C11	Industry	1K bits (x8 or x16)	N/A	1 ms/byte	1 MHz	1M	C,I,E	8	P,SN,SM	4.5V - 5.5V
93LCS56	National	2K bits (128 x 16)	N/A	10 ms	2 MHz	1M	C,I	8,14	P,SN,SM,SL	2.5V - 6.0V
93LCS66	National	4K bits (256 x 16)	N/A	10 ms	2 MHz	1M	C,I	8,14	P,SN,SM,SL	2.5V - 6.0V

*Future: 10M

Legend:

P = Plastic Dip
SN = 150°" 8ld SOIC
S = Dice in Wafflepack
J = Ceramic DIP
SM = .207" 8ld SOIC
L = PLCC
SL = .150" 14ld SOIC
W = Dice in Wafer Form
VS = 28ld VSOP (8x13.4mm)
K = Ceramic LCC
SO = .300" 28ld SOIC
STS = 28ld TSOP (8x20mm)

Note 1: Not All Combinations Of Speed/temperature Range/package/etc. Are Available. Consult Factory For Specific Part Information.

SERIAL EEPROM

Serial EEPROM Cross Reference Guide

The purpose of this document is to provide a quick way to determine the closest Microchip equivalent to Serial EEPROMs produced by other manufacturers. The cross reference section is broken down by manufacturer and lists all parts from that manufacturer, and the comparable Microchip part number. There is also a listing of manufacturer's part numbering schemes to assist in determining the specifications of a particular part.

There are subtle differences from manufacturer to manufacturer and device to device, so Microchip recommends consulting the respective manufacturer's gadabout for specific details.

Microchip provides a wide selection of Serial EEPROM devices, both from a density and a packaging standpoint, as well as several different protocols. If you are interested in a part that is not listed in this book, please refer to the Microchip data book, or contact your local distributor or sales representative for assistance.

The manufacturers* included in this document are as follows:

AKM	Oki
Atmel	Philips
Catalyst	Samsung
Exel	SGS-Thomson
ISSI	Siemens
Microchip	Xicor
Mitsubishi	
National	

FIGURE 1: MICROCHIP SERIAL EEPROM PART NUMBER GUIDE

XX XX XX XX X / XX

Package	W	=	Die in wafer form
	S	=	Die in waffle pack
	P	=	PDIP
	SM	=	Small outline .207 mil
	SN	=	Small outline .150 mil
	SL	=	14-lead small outline .150 mil
	J	=	CERDIP
Process Temperature	Blank	=	0°C to +70°C
	I	=	-40°C to +125°C
	E	=	-40°C to +125°C
Special Options			
Memory	01	1K	128 x 8
	02	2K	256 x 8
	04	4K	512 x 8
	08	8K	1K x 8
	16	16K	2K x 8
	32	32K	4K x 8
	65	64K	8K x 8
	11	1K	128K x 8 or 64 x 16
	72	1K	128 x 8
	82	2K	256 x 8
	92	4K	512 x 8
	06	256 Bit	16 x 16
	46	1K	64 x 16/128 x 8
	56	2K	256 x 8/128 x 16
	66	4K	512 x 8/256 x 16
Process Technology	C	–	CMOS
	LC	–	Low Voltage (2.5V) CMOS
	AA	–	1.8 Volt
Part Number Designator	24	–	2-wire
	59	–	4-wire
	85	–	2-wire
	93	–	3-wire

*The above trademarks are property of their respective companies.

SERIAL EEPROM

Manufacturer	Part Number	Closest Microchip Equivalent	Size
AKM	AK93C45	93C46	1K
AKM	AK93C45L	93C46	1K
AKM	AK93C55	93LC56	2K
AKM	AK93C55L	93AA56	2K
AKM	AK93C57	93LC56	2K
AKM	AK6420	93LC56	2K
AKM	AK93C65	93LC66	4K
AKM	AK93C65L	93AA66	4K
AKM	AK93C67	93LC66	4K
AKM	AK6420	93LC66	4K
ATMEL	AT24C01A	24LC01B/ 24C01A	1K
ATMEL	AT24C01A-2.7	24LC01B	1K
ATMEL	AT24C01A-2.5	24LC01B	1K
ATMEL	AT24C01A-1.8	24AA01	1K
ATMEL	AT59C11	59C11	1K
ATMEL	AT59C11-2.7	59C11	1K
ATMEL	AT59C11-2.5	59C11	1K
ATMEL	AT59C11-1.8	59C11	1K
ATMEL	AT93C46	93C46	1K
ATMEL	AT93C46-2.7	93LC46	1K
ATMEL	AT93C46-2.5	93LC46	1K
ATMEL	AT93C46-1.8	93LC46	1K
ATMEL	AT93C56	93C56	2K
ATMEL	AT93C56-2.7	93LC56	2K
ATMEL	AT93C56-2.5	93LC56	2K
ATMEL	AT93C56-1.8	93AA56	2K
ATMEL	AT93C57	93C56	2K
ATMEL	AT93C57-2.7	93LC56	2K
ATMEL	AT93C57-2.5	93LC56	2K
ATMEL	AT93C57-1.7	93AA56	2K
ATMEL	AT24C02	24C02/ 24LC02B	2K
ATMEL	AT24C02-2.7	24LC02B	2K
ATMEL	AT24C02-2.5	24LC02B	2K
ATMEL	AT24C02-1.8	24AA02	2K
ATMEL	AT93C66	93C66	4K
ATMEL	AT93C66-2.7	93LC66	4K
ATMEL	AT93C66-2.5	93LC66	4K
ATMEL	AT93C66-1.8	93AA66	4K
ATMEL	AT24C04	24C04/ 24LC04B	4K
ATMEL	AT24C04-2.7	24LC04B	4K
ATMEL	AT24C04-2.5	24LC04B	4K
ATMEL	AT24C04-1.8	24AA04	4K
ATMEL	AT24C08	24LC08B	8K
ATMEL	AT24C08-2.7	24LC08B	8K
ATMEL	AT24C08-2.5	24LC08B	8K
ATMEL	AT24C08-1.8	24AA08	8K
ATMEL	AT24C16	24LC16B	16K
ATMEL	AT24C16-2.7	24LC16B	16K
ATMEL	AT24C16-2.5	24LC16B	16K
ATMEL	AT24C16-1.8	24AA16	16K
ATMEL	AT24C164	24LC164	16K
ATMEL	AT24C164-2.7	24LC164	16K
ATMEL	AT24C164-2.5	24LC164	16K
ATMEL	AT24C164-1.8	24AA164	16K
ATMEL	AT24C64	24C65*	64K
ATMEL	AT24C64-2.7	24C65*	64K
ATMEL	AT24C642.5	24C65*	64K

Manufacturer	Part Number	Closest Microchip Equivalent	Size
ATMEL	AT24C64-1.8	24C65*	64K
ATMEL	AT24C32	24C32*	32K
ATMEL	AT24C32-2.7	24C32*	32K
ATMEL	AT24C32-2.5	24C32*	32K
ATMEL	AT24C32-1.8	24C32*	32K
Catalyst	CAT59C11/I/A/AI/H	59C11	1K
Catalyst	CAT33C101C/I	93LC46	1K
Catalyst	CAT33C101	93LC46	1K
Catalyst	CAT93C46/I/H	93LC46	1K
Catalyst	CAT93C46AI/H	93LC46	1K
Catalyst	CAT35C102H/I	93C56	2K
Catalyst	CAT93C56/I	93C56	2K
Catalyst	CAT93LC56/I	93LC56	2K
Catalyst	CAT24C02/I	24C02B/ 24LC02B	2K
Catalyst	CAT24LC02/I	24LC02B	2K
Catalyst	CAT24C04.1	24C04A/ 24LC04B	4K
Catalyst	CAT24LC04.1	24LC04B	4K
Catalyst	CAT35C104/H/I	93C66	4K
Catalyst	CAT33C104	93LC66	4K
Catalyst	CAT35C704/I	93C66	4K
Catalyst	CAT33C704/I	93LC66	4K
Catalyst	CAT35C80	93C66	4K
Catalyst	CAT33C80	93LC66	4K
Catalyst	CAT24C08	24LC08B	8K
Catalyst	CAT24LC08	24LC08B	8K
Catalyst	CAT24C16	24LC16B	16K
Catalyst	CAT24LC16	24LC16B	16K
Exel	XL93LC06	93C06	256bit
Exel	XL24C01A	24C01A/ 24LC01B	1K
Exel	XL24C01-2.5	24LC01B	1K
Exel	XL93CCSLC46	93C46	1K
Exel	XL93CCSLC46-3	93LC46	1K
Exel	XL24C01A-3	24LC01B	1K
Exel	XL24C02	24C02A/ 24LC02B	2K
Exel	XL24C02-3	24LC02B	2K
Exel	XL93C56,LC56	93C56/ LC56	2K
Exel	XL24C01-2.5	24LC01B	2K
Exel	XL93LC56-3	93LC56	2K
Exel	XL93C66,LC66	93C66/ 93LC66	4K
Exel	XL93C66-3,LC66-3	93LC66	4K
Exel	XL24C04	24C04A/ 24LC04B	4K
Exel	XL24C04-3	24LC04B	4K
Exel	XL24C04-2.5	24LC04B	4K
Exel	XL24C16	24LC16B	16K
Exel	XL24C16-3	24LC16B	16K
ISSI	IS93C46	93C46	1K
ISSI	IS93C46-3	93LC46	1K
ISSI	IS93C56	93C56	2K
ISSI	IS93C66	93C66	4K
National	NM93C06	93C06	256bit
National	NM93C46	93C46	1K
National	NM93C46LZ	93AA46	1K
National	NM93C56	93C56	2K

*Not 100% compatible.

Manufacturer	Part Number	Closest Microchip Equivalent	Size
National	NM93C56LZ	93AA56	2K
National	NM93CS56	93LCS56	2K
National	NM93CS56L	93LCS56	2K
National	NM24C02	24C02A/	2K
National	NM24C02L	24LC02B	2K
National	NM24C03	24C02A	2K
National	NM24C03L	24LC02B	2K
National	NM93C66	93C66	4K
National	NM93CS66	93LCS66	4K
National	NM93C66L	93LC66	4K
National	NM93CS66L	93LCS66	4K
National	NM93C66LZ	93AA66	4K
National	NM24C04	24C04A/ 24LC04B	4K
National	NM24C04L	24LC04B	4K
National	NM24C05L	24LC04B	4K
National	NM24C08	24LC08B	8K
National	NM24C08L	24LC08B	8K
National	NM24C09	24LC08B	8K
National	NM24C09L	24LC08B	8K
National	NM24C16	24LC16B	16K
National	NM24C16L	24LC16B	16K
National	NM24C17	24LC16B	16K
National	NM24C17L	24LC16B	16K
Oki	MSM16812	93C56	2K
Philips-Signetics	PCA8581	24C01A	1K
Philips-Signetics	PCF8582C2	85C82	2K
Philips-Signetics	PCD8582D2	85C82	2K
Philips-Signetics	PCF8582F2	85C82	2K
Philips-Signetics	PCF8594C-2	24AA04	4K
Philips-Signetics	PCD8594D-2	24LC04B	4K
Philips-Signetics	PCF8598C-2	24LC08B	8K
Philips-Signetics	PCD8598D-2	24LC08B	8K
Philips-Signetics	PCD85898F-2	24LC08B	8K
Samsung	KM93C06	93C06256bit	
Samsung	KM93C07	93C06256bit	
Samsung	KM93C46	93C46	1K
Samsung	KM94C46V	93C46	1K
Samsung	KM93C56	93C56	2K
Samsung	KM93CS56	93LCS56	2K
Samsung	KM93C56V	93AA56	2K
Samsung	KM93C57	93C56	2K
Samsung	KM93C57V	93AA56	2K
Samsung	KM93C66	93C66	4K
Samsung	KM93CS66	93LCS66	4K
Samsung	KM93C66V	93AA66	4K
Samsung	KM93C67	93C66	4K
Samsung	KM93C67V	93AA66	4K
SEEQ	2913A	93C46	1K
SEEQ	2913C	93C46	1K
SEEQ	2914A	93C46	1K
SEEQ	2919G	93C46	1K
SEEQ	2922A	93LC56	2K
SEEQ	2929G	93LC56	2K
SEEQ	2934A	93LC66	4K
SEEQ	2929G	93LC66	4K
SGS-Thomson	ST93C06	93C06	256bit
SGS-Thomson	ST24C01	24LC01B	1K
SGS-Thomson	ST93C46A	93C46	1K
SGS-Thomson	ST93C46T	93C46	1K
SGS-Thomson	ST93C46	93LC46	1K
SGS-Thomson	ST24W01	24LC01B	1K
SGS-Thomson	ST25W01	24LC01B	1K
SGS-Thomson	ST93C56	93C56	2K
SGS-Thomson	ST93CS56	93LCS56	2K
SGS-Thomson	ST93CS57	93LCS56	2K
SGS-Thomson	ST24C02A	24LC02B	2K
SGS-Thomson	ST24C02C	24LC02B	2K
SGS-Thomson	ST24W02C	24LC02B	2K
SGS-Thomson	ST25C02A	24LC02B	2K
SGS-Thomson	ST25W02C	24LC02B	2K
SGS-Thomson	ST93CS66	93LCS66	4K
SGS-Thomson	ST93CS67	93LCS66	4K
SGS-Thomson	ST24C04	24C04A 24LC04B/	4K
SGS-Thomson	ST24C04C	24LC04B	4K
SGS-Thomson	ST24W04C	24LC04B	4K
SGS-Thomson	ST25C04	24LC04B	4K
SGS-Thomson	ST25C0RC	24LC04B	4K
SGS-Thomson	ST25W04C	24LC04B	4K
SGS-Thomson	ST24C08	24LC08B	8K
SGS-Thomson	ST24C08C	24LC08B	8K
SGS-Thomson	ST25CO8C	24LC08B	8K
SGS-Thomson	ST24C16C	24LC16B	16K
SGS-Thomson	ST24E16C	24LC16B	16K
SGS-Thomson	ST25C16C	24LC16B	16K
SGS-Thomson	ST25E16C	24LC16B	16K
SGS-Thomson	ST24E32D	24LC32*	32K
SGS-Thomson	ST25E32D	24LC32*	32K
SGS-Thomson	ST24E64D	24LC65*	64K
SGS-Thomson	ST25E64D	24LC65*	64K
Siemens	SDA2516-2	24C01A/ 24LC01B	1K
Siemens	SDA2526-2	24C02A/ 24LC02B	2K
Siemens	SDA2546	24C04A/ 24LC04B	4K
Siemens	SDA2586	24LC08B	8K
Xicor	X24C01A	24LC01B	1K
Xicor	X2402	24C02A	2K
Xicor	X24C02	24LC02B	2K
Xicor	X2404	24C04A/ 24LC04B	4K
Xicor	X24C04	24LC04B	4K
Xicor	X24C08	24LC08B	8K
Xicor	X24C16	24LC16B	16K
Xicor	X24164	24LC164	16K
Xicor	X24645	24LC65*	64K

*Not 100% compatible.

COMPETITIVE PART NUMBER BREAKDOWN

FIGURE 2: ATMEL

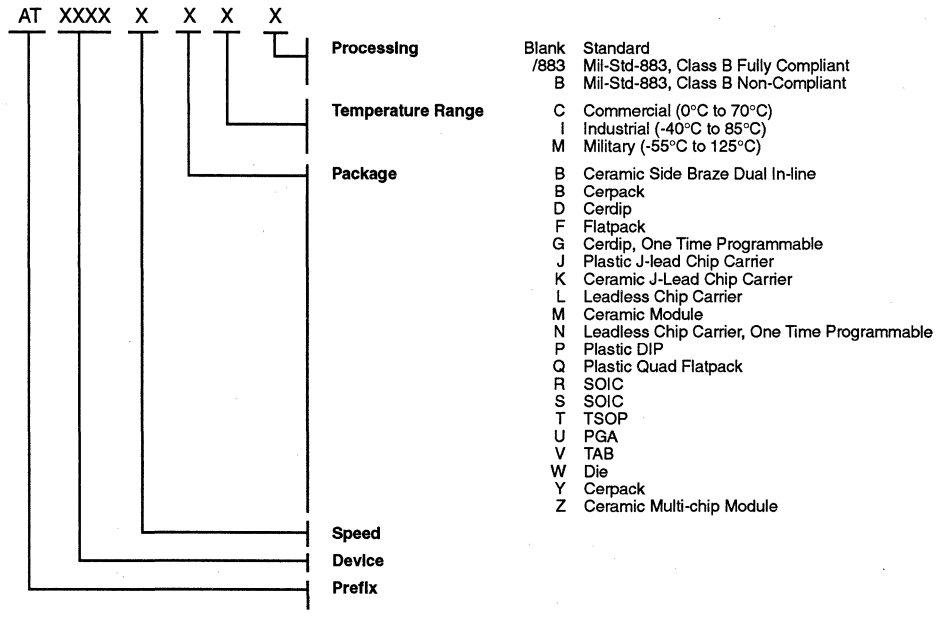


FIGURE 3: CATALYST SEMICONDUCTOR

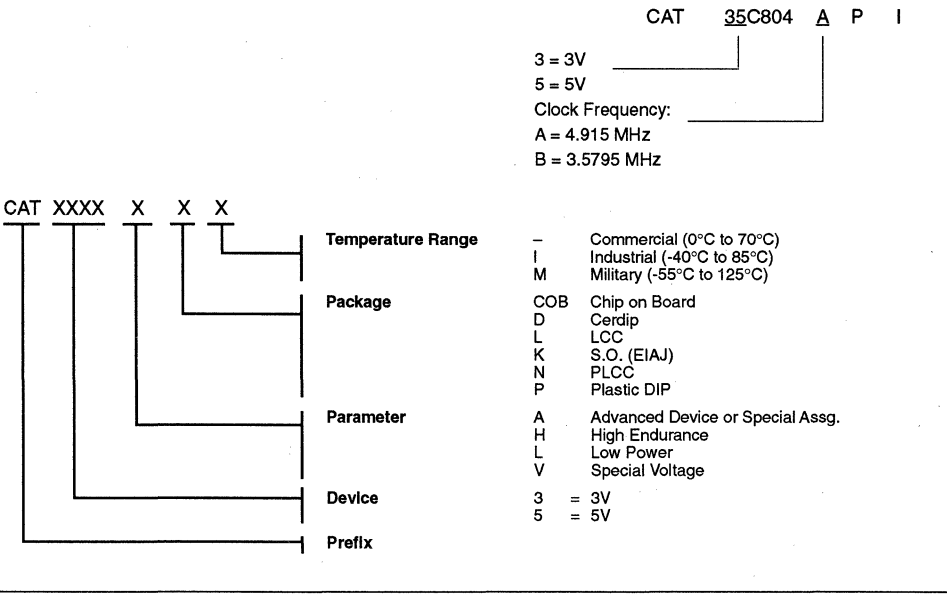


FIGURE 4: EXEL

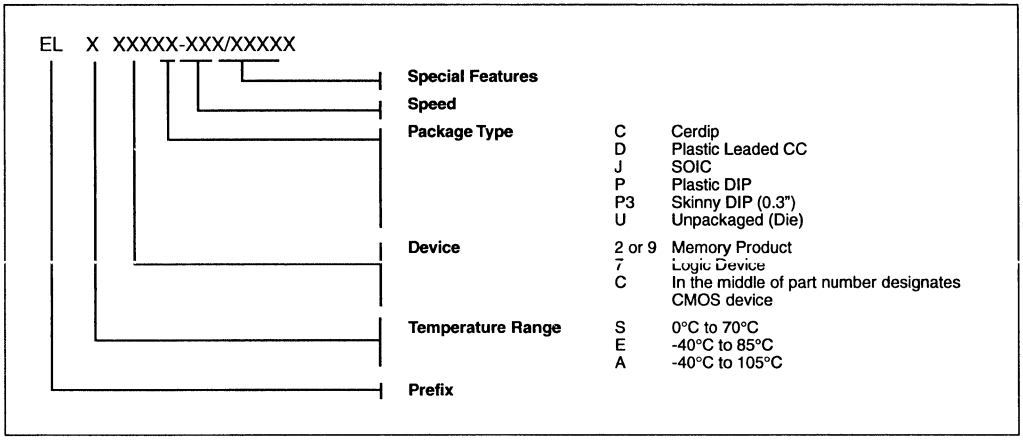


FIGURE 5: NATIONAL SEMICONDUCTOR CORPORATION

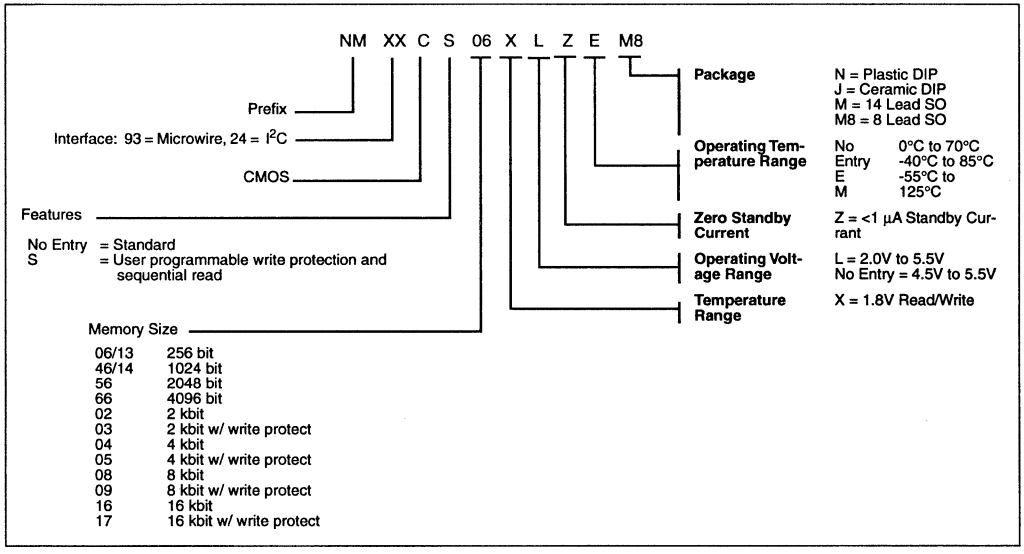


FIGURE 6: PHILIPS

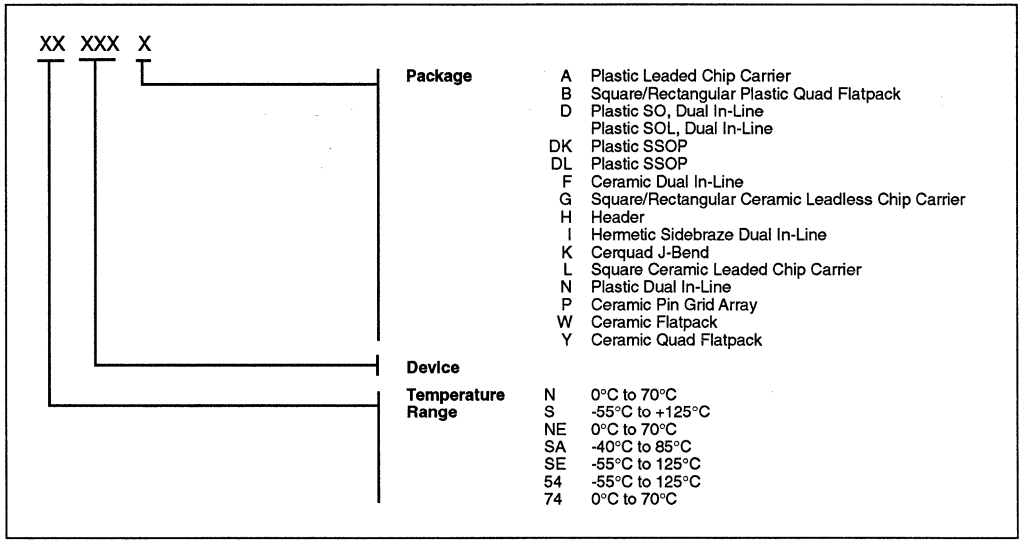


FIGURE 7: SAMSUNG

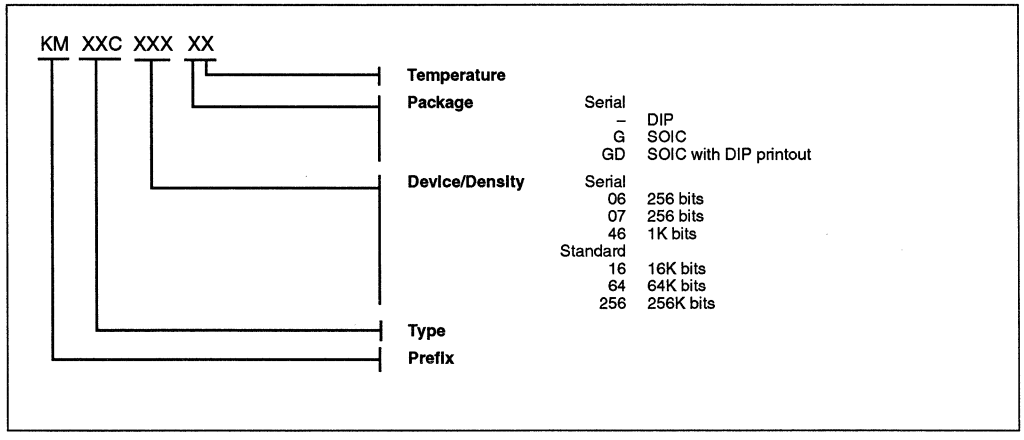


FIGURE 8: SEEQ

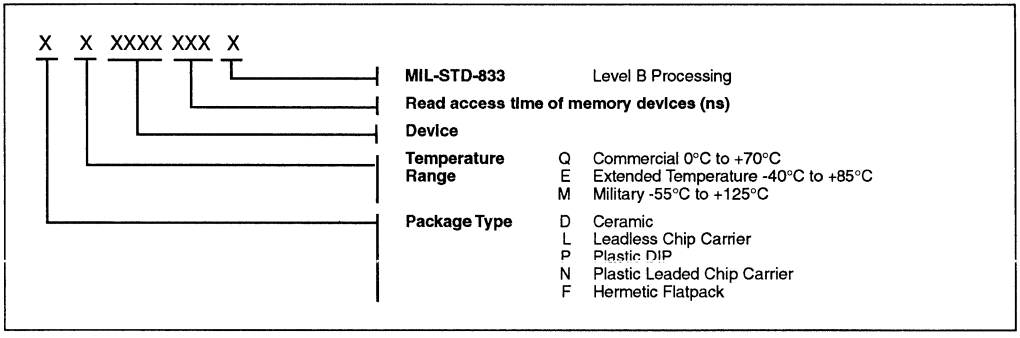


FIGURE 9: SGS-THOMSON

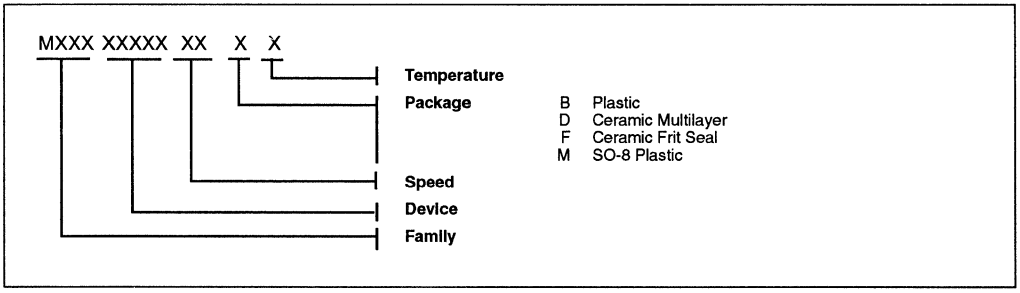
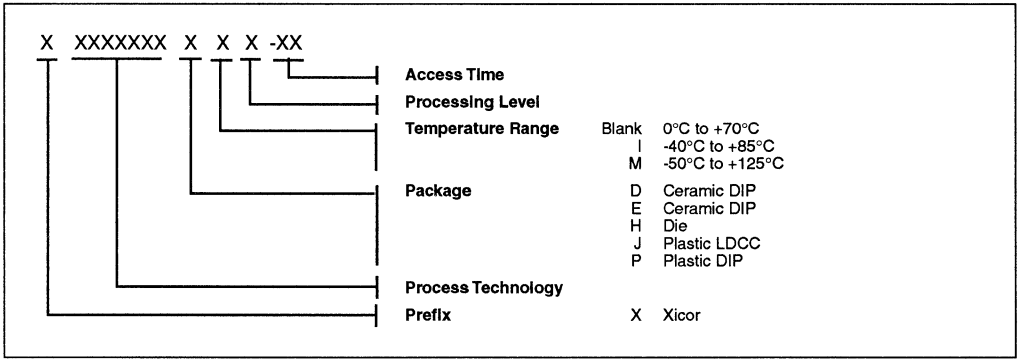


FIGURE 10: SIEMENS - NOT AVAILABLE

FIGURE 11: XICOR



NOTES

PARALLEL EEPROMS

Parallel EEPROM Selection Guide

CMOS PARALLEL EEPROMS

Device	Density/ Organization	Access Time (ns)	Icc (Active/ Standby)	Byte Write Time	Endurance (cycles) *	Temp Range	# Pins	Package Types	Operating Voltage
28C04A	4K bits (512 x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	24,32	P,J,L	4.5V - 5.5V
28C16A	16K bits (2K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	24,28,32	P,J,TS,VS,L	4.5V - 5.5V
28C17A	16K bits (2K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V
28C64A	64K bits (8K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V
28C64AX	64K bits (8K x 8)	150/200/250	30 mA/100 µA	1 ms	10K	C,I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V
28C04AF	4K bits (512 x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C,I	24,32	P,J,L	4.5V - 5.5V
28C16AF	16K bits (2K x 8)	150/200/250	30 mA/100 uA	200 µs	10K	C,I	24,28,32	P,J,TS,VS,L	4.5V - 5.5V
28C17AF	16K bits (2K x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C,I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V
28C64AF	64K bits (8K x 8)	150/200/250	30 mA/100 µA	200 µs	10K	C,I	28,32	P,J,SO,TS,VS,L	4.5V - 5.5V

PACKAGES

P = Plastic DIP
SN = .150" 8 lead SOIC
S = Dice in Wafflepack
J = Ceramic DIP
SM = .207" 8 lead SOIC
L = PLCC
SL = .150" 14 lead SOIC
W = Dice in Wafer Form
VS = 28 lead VSOP (8x13.4mm)
K = Ceramic LCC
SO = .300" 28 lead SOIC
TS = 28lead TSOP (8x20mm)

* Endurance is guaranteed to 10K cycles at extended (-40°C to +125°C) temperature.

Note 1: NOT ALL COMBINATIONS OF SPEED/TEMPERATURE RANGE/PACKAGE/ETC. ARE AVAILABLE. CONSULT FACTORY FOR SPECIFIC PART INFORMATION

NOTES

EPROM Selection Guide

CMOS Parallel EPROMs

Part Number	QTP Avail.	Size	Org	Access Time (ns)	Supply Voltage	Package	Temp. Range	Standby Current
27C64	Yes	64K	8K x 8	120-250	+5V	J,K,L,P,SO,TS	C,I	2mA/100µA
27C128	Yes	128K	16K x 8	120-250	+5V	J,K,L,P,SO	C,I	2mA/100µA
27C256	Yes	256K	32K x 8	90-200	+5V	J,K,L,P,SO,TS,VS	C,I,E	2mA/100µA
27C512A	Yes	512K	64K x 8	70-150	+5V	J,K,L,P,SO,TS,VS	C,I,E	2mA/30µA
27LV64	Yes	64K	8K x 8	200-300	+3V to +5V	J,K,L,P,SO,TS	C,I	1mA/100µA
27LV256	Yes	256K	32K x 8	200-300	+3V to +5V	J,K,L,P,SO,TS,VS	C,I	1mA/100µA
27LV512	Yes	512K	64K x 8	200-300	+3V to +5V	J,K,L,P,SO,TS,VS	C,I	1mA/100µA
27HC256	No	256K	32K x 8	55-90	+5V	J,K,L,P,SO,TS,VS	C,I,E	35mA
27HC256L	No	256K	32K x 8	90	+5V	J,K,L,P,SO,TS,VS	C,I	2mA/100µA
27HC1616	No	256K	16K x16	55-70	+5V	40J, 44K	C,I	50mA

CMOS Serial EPROM

Part Number	QTP Avail.	Size	Org.	Max. Clock Freq.	Supply Voltage	Package	Temperature Range
37LV36	Yes	36K	1134x32	60-200	+3V to +5V	P, SN, L	C,I
37LV65	Yes	64K	2048x32	60-200	+3V to +5V	P, SN, L	C,I
37LV128	Yes	128K	4096x32	60-200	+3V to +5V	P, SN, L	C,I

PACKAGES

P = Plastic DIP J = Ceramic DIP L = PLCC K = Ceramic LCC

SN = .150" 8ld SOIC W = Dice in Wafer Form SO = .300" 28ld SOIC

S = Dice in Wafflepack VS = 28ld VSOP (8x13.4mm) TS = 28ld TSOP (8x20mm)

Note: Not all combinations of speed/temperature range/package/etc. are available. Consult factory for specific part information.

NOTES

EPROM Cross Reference Guide

INTRODUCTION

The purpose of this document is to provide a quick way to determine which EPROM parts are mechanical and electrical equivalents to Microchip devices. There is also a listing of manufacturer's part numbering schemes to assist in determining the specifications of a particular part. The cross reference section is broken down by manufacturer and lists all parts from that manufacturer, and the plug compatible Microchip part number.

The one exception to plug compatibility listed in this cross-reference concerns the 28 pin SOIC package. Microchip, along with other manufacturers, make this part in a .300" (JEDEC Standard) width. There are other manufacturers that produce this device in a .330" (EIAJ Standard) wide package. In many cases, the PCB can be laid out to accommodate both versions. The devices that are offered in the .330" package are listed in this reference with an asterisk.

Microchip provides a wide selection of EPROM devices, both from a density and a packaging standpoint. If you are interested in a part that is not listed in this book, please refer to the Microchip data book, or contact your local distributor or sales representative for assistance.

Legend:		
AMD®	=	Advanced Micro Devices
T.I.	=	Texas Instruments
SGS	=	ST® SGS-Thomson
Intel®	=	Intel Corporation
Toshiba®	=	Toshiba Corporation
National®	=	National Semiconductor® Corporation
Hitachi®	=	Hitachi Corporation
Atmel®	=	Atmel Corporation

The information contained in this publication regarding competitor devices was obtained from the respective EPROM manufacturer's latest available published technical information and may be subject to updates

1.0 CROSS REFERENCE OF MICROCHIP EPROM PRODUCTS TO THE COMPETITION

Hitachi Part Number	Description	Microchip Part Number	
HN27C256AG-10	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
HN27C256HP-10	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
HN27C256FP-10T*	OTP 256K EPROM,100NS	SOIC 28	**27C256-10/SO**
HN27C256AG-12	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
HN27C256AG-15	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
HN27C256FP-25T/-30T*	OTP 256K EPROM,200NS	SOIC 28	**27C256-20/SO**
HN27512G-25/-30	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
HN27512P-25/-30	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
HN27C256HG-70/-85	UV 256K HS EPROM,70NS	CERDIP 28	**27HC256-70/J**
HN27C256HP-70/-85	OTP 256K HS EPROM,70NS	PDIP 28	**27HC256-70/P**
HN27C256HFP-85T*	OTP 256K HS EPROM,70NS	SOIC 28	**27HC256-70/SO**

AMD Part Number	Description	Microchip Part Number	
Am27C64-120DC	UV 64K EPROM,120NS	CERDIP 28	**27C64-12/J**
Am27C64-120LC	UV 64K EPROM,120NS	LCC 32	**27C64-12/K**
Am27C64-120JC	OTP 64K EPROM,120NS	PLCC 32	**27C64-12/L**
Am27C64-120PC	OTP 64K EPROM,120NS	PDIP 28	**27C64-12/P**
Am27C64-150DC	UV 64K EPROM,150NS	CERDIP 28	**27C64-15/J**
Am27C64-150LC	UV 64K EPROM,150NS	LCC 32	**27C64-15/K**
Am27C64-150JC	OTP 64K EPROM,150NS	PLCC 32	**27C64-15/L**
Am27C64-150PC	OTP 64K EPROM,150NS	PDIP 28	**27C64-15/P**
Am27C64-200DC	UV 64K EPROM,200NS	CERDIP 28	**27C64-20/J**
Am27C64-200LC	UV 64K EPROM,200NS	LCC 32	**27C64-20/K**
Am27C64-200JC	OTP 64K EPROM,200NS	PLCC 32	**27C64-20/L**
Am27C64-200PC	OTP 64K EPROM,200NS	PDIP 28	**27C64-20/P**
Am27C64-250DC	UV 64K EPROM,250NS	CERDIP 28	**27C64-25/J**
Am27C64-250LC	UV 64K EPROM,250NS	LCC 32	**27C64-25/K**
Am27C64-250JC	OTP 64K EPROM,250NS	PLCC 32	**27C64-25/L**
Am27C64-250PC	OTP 64K EPROM,250NS	PDIP 28	**27C64-25/P**
Am27C64-120DI	UV 64K EPROM,120NS,IND	CERDIP 28	**27C64-12I/J**
Am27C64-150DI	UV 64K EPROM,150NS,IND	CERDIP 28	**27C64-15I/J**
Am27C64-150LI	UV 64K EPROM,150NS,IND	LCC 32	**27C64-15I/K**
Am27C64-150JI	OTP 64K EPROM,150NS,IND	PLCC 32	**27C64-15I/L**
Am27C64-150PI	OTP 64K EPROM,150NS,IND	PDIP 28	**27C64-15I/P**
Am27C64-200DI	UV 64K EPROM,200NS,IND	CERDIP 28	**27C64-20I/J**
Am27C64-200LI	UV 64K EPROM,200NS,IND	LCC 32	**27C64-20I/K**
Am27C64-200JI	OTP 64K EPROM,200NS,IND	PLCC 32	**27C64-20I/L**
Am27C64-200PI	OTP 64K EPROM,200NS,IND	PDIP 28	**27C64-20I/P**
Am27C64-250DI	UV 64K EPROM,250NS,IND	CERDIP 28	**27C64-25I/J**
Am27C64-250LI	UV 64K EPROM,250NS,IND	LCC 32	**27C64-25I/K**
Am27C64-250JI	OTP 64K EPROM,250NS,IND	PLCC 32	**27C64-25I/L**
Am27C64-250PI	OTP 64K EPROM,250NS,IND	PDIP 28	**27C64-25I/P**
Am27C128-120DC	UV 128K EPROM,120NS	CERDIP 28	**27C128-12/J**

AMD Part Number	Description	Microchip Part Number	
Am27C128-120LC	UV 128K EPROM,120NS	LCC 32	**27C128-12/K**
Am27C128-120JC	OTP 128K EPROM,120NS	PLCC 32	**27C128-12/L**
Am27C128-120PC	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**
Am27C128-150DC	UV 128K EPROM,150NS	CERDIP 28	**27C128-15/J**
Am27C128-150LC	UV 128K EPROM,150NS	LCC 32	**27C128-15/K**
Am27C128-150JC	OTP 128K EPROM,150NS	PLCC 32	**27C128-15/L**
Am27C128-150PC	OTP 128K EPROM,150NS	PDIP 28	**27C128-15/P**
Am27C128-200DC	UV 128K EPROM.200NS	CERDIP 28	**27C128-20/J**
Am27C128-200LC	UV 128K EPROM,200NS	LCC 32	**27C128-20/K**
Am27C128-200JC	OTP 128K EPROM,200NS	PLCC 32	**27C128-20/L**
Am27C128-200PC	OTP 128K EPROM,200NS	PDIP 28	**27C128-20/P**
Am27C128-250DC	UV 128K EPROM,250NS	CERDIP 28	**27C128-25/J**
Am27C128-250LC	UV 128K EPROM,250NS	LCC 32	**27C128-25/K**
Am27C128-250JC	OTP 128K EPROM,250NS	PLCC 32	**27C128-25/L**
Am27C128-250PC	OTP 128K EPROM,250NS	PDIP 28	**27C128-25/P**
Am27C128-120DI	UV 128K EPROM,120NS,IND	CERDIP 28	**27C128-12I/J**
Am27C128-150DI	UV 128K EPROM,150NS,IND	CERDIP 28	**27C128-15I/J**
Am27C128-150LI	UV 128K EPROM,150NS,IND	LCC 32	**27C128-15I/K**
Am27C128-150JI	OTP 128K EPROM,150NS,IND	PLCC 32	**27C128-15I/L**
Am27C128-150PI	OTP 128K EPROM,150NS,IND	PDIP 28	**27C128-15I/P**
Am27C128-200DI	UV 128K EPROM,200NS,IND	CERDIP 28	**27C128-20I/J**
Am27C128-200LI	UV 128K EPROM,200NS,IND	LCC 32	**27C128-20I/K**
Am27C128-200JI	OTP 128K EPROM,200NS,IND	PLCC 32	**27C128-20I/L**
Am27C128-200PI	OTP 128K EPROM,200NS,IND	PDIP 28	**27C128-20I/P**
Am27C128-250DI	UV 128K EPROM,250NS,IND	CERDIP 28	**27C128-25I/J**
Am27C128-250LI	UV 128K EPROM,250NS,IND	LCC 32	**27C128-25I/K**
Am27C128-250JI	OTP 128K EPROM,250NS,IND	PLCC 32	**27C128-25I/L**
Am27C128-250PI	OTP 128K EPROM,250NS,IND	PDIP 28	**27C128-25I/P**
Am27C256-90DC	UV 256K EPROM,90NS	CERDIP 28	**27C256-90/J**
Am27C256-90LC	OTP 256K EPROM,90NS	PLCC 32	**27C256-90/L**
Am27C256-90JC	OTP 256K EPROM,90NS	PDIP 28	**27C256-90/P**
Am27C256-90PC	OTP 256K EPROM,90NS	SOIC 28	**27C256-90/SO**
Am27C256-100DC	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
Am27C256-100LC	UV 256K EPROM,100NS	LCC 32	**27C256-10/K**
Am27C256-100JC	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
Am27C256-100PC	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
Am27C256-120DC	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
Am27C256-120LC	UV 256K EPROM,120NS	LCC 32	**27C256-12/K**
Am27C256-120JC	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
Am27C256-120PC	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
Am27C256-150DC	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
Am27C256-150LC	UV 256K EPROM,150NS	LCC 32	**27C256-15/K**
Am27C256-150JC	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
Am27C256-150PC	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
Am27C256-200DC	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
Am27C256-200LC	UV 256K EPROM,200NS	LCC 32	**27C256-20/K**

AMD Part Number	Description	Microchip Part Number	
Am27C256-200JC	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
Am27C256-200PC	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
Am27C256-100DI	UV 256K EPROM,100NS,IND	CERDIP 28	**27C256-10I/J**
Am27C256-100LI	UV 256K EPROM,100NS,IND	LCC 32	**27C256-10I/K**
Am27C256-100JI	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256-10I/L**
Am27C256-100PI	OTP 256K EPROM,100NS,IND	PDIP 28	**27C256-10I/P**
Am27C256-120DI	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
Am27C256-120LI	UV 256K EPROM,120NS,IND	LCC 32	**27C256-12I/K**
Am27C256-120JI	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
Am27C256-120PI	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
Am27C256-150DI	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
Am27C256-150LI	UV 256K EPROM,150NS,IND	LCC 32	**27C256-15I/K**
Am27C256-150JI	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
Am27C256-150PI	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
Am27C256-200DI	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
Am27C256-200LI	UV 256K EPROM,200NS,IND	LCC 32	**27C256-20I/K**
Am27C256-200JI	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
Am27C256-200PI	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
Am27C512-90DC	UV 512K EPROM,90NS	CERDIP 28	**27C512-90/J**
Am27C512-90LC	UV 512K EPROM,90NS	LCC 32	**27C512-90/K**
Am27C512-90JC	OTP 512K EPROM,90NS	PLCC 32	**27C512-90/L**
Am27C512-90PC	OTP 512K EPROM,90NS	PDIP 28	**27C512-90/P**
Am27C512-120DC	UV 512K EPROM,120NS	CERDIP 28	**27C512-12/J**
Am27C512-120LC	UV 512K EPROM,120NS	LCC 32	**27C512-12/K**
Am27C512-120JC	OTP 512K EPROM,120NS	PLCC 32	**27C512-12/L**
Am27C512-120PC	OTP 512K EPROM,120NS	PDIP 28	**27C512-12/P**
Am27C512-150DC	UV 512K EPROM,150NS	CERDIP 28	**27C512-15/J**
Am27C512-150LC	UV 512K EPROM,150NS	LCC 32	**27C512-15/K**
Am27C512-150JC	OTP 512K EPROM,150NS	PLCC 32	**27C512-15/L**
Am27C512-150PC	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
Am27C512-200DC	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
Am27C512-200LC	UV 512K EPROM,200NS	LCC 32	**27C512-20/K**
Am27C512-200JC	OTP 512K EPROM,200NS	PLCC 32	**27C512-20/L**
Am27C512-200PC	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
Am27C512-120DI	UV 512K EPROM,120NS,IND	CERDIP 28	**27C512-12I/J**
Am27C512-120LI	UV 512K EPROM,120NS,IND	LCC 32	**27C512-12I/K**
Am27C512-120JI	OTP 512K EPROM,120NS,IND	PLCC 32	**27C512-12I/L**
Am27C512-120PI	OTP 512K EPROM,120NS,IND	PDIP 28	**27C512-12I/P**
Am27C512-150DI	UV 512K EPROM,150NS,IND	CERDIP 28	**27C512-15I/J**
Am27C512-150LI	UV 512K EPROM,150NS,IND	LCC 32	**27C512-15I/K**
Am27C512-150JI	OTP 512K EPROM,150NS,IND	PLCC 32	**27C512-15I/L**
Am27C512-150PI	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
Am27C512-200DI	UV 512K EPROM,200NS,IND	CERDIP 28	**27C512-20I/J**
Am27C512-200LI	UV 512K EPROM,200NS,IND	LCC 32	**27C512-20I/K**
Am27C512-200JI	OTP 512K EPROM,200NS,IND	PLCC 32	**27C512-20I/L**
Am27C512-200PI	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**

AMD Part Number	Description	Microchip Part Number	
Am27C512-75DI	UV 512K EPROM,70NS	CERDIP 28	**27C512A-70/J**
Am27C512-75LI	UV 512K EPROM,70NS	LCC 32	**27C512A-70/K**
Am27C512-90DC	UV 512K EPROM,90NS	CERDIP 28	**27C512A-90/J**
Am27C512-90LC	UV 512K EPROM,90NS	LCC 32	**27C512A-90/K**
Am27C512-90JC	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
Am27C512-90PC	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
Am27C512-120DC	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
Am27C512-120LC	UV 512K EPROM,120NS	LCC 32	**27C512A-12/K**
Am27C512-120JC	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
Am27C512-120PC	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
Am27C512-150DC	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
Am27C512-150LC	UV 512K EPROM,150NS	LCC 32	**27C512A-15/K**
Am27C512-150JC	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
Am27C512-150PC	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
Am27C512-200DC	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**
Am27C512-200LC	UV 512K EPROM,200NS	LCC 32	**27C512A-20/K**
Am27C512-200JC	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
Am27C512-200PC	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**
Am27HC256-55DC	UV 256K HS EPROM,55NS	CERDIP 28	**27HC256-55/J**
Am27HC256-55LC	UV 256K HS EPROM,55NS	LCC 32	**27HC256-55/K**
Am27HC256-55JC	OTP 256K HS EPROM,55NS	PLCC 32	**27HC256-55/L**
Am27HC256-55PC	OTP 256K HS EPROM,55NS	PDIP 28	**27HC256-55/P**
Am27HC256-70DC	UV 256K HS EPROM,70NS	CERDIP 28	**27HC256-70/J**
Am27HC256-70LC	UV 256K HS EPROM,70NS	LCC 32	**27HC256-70/K**
Am27HC256-70JC	OTP 256K HS EPROM,70NS	PLCC 32	**27HC256-70/L**
Am27HC256-70PC	OTP 256K HS EPROM,70NS	PDIP 28	**27HC256-70/P**
Am27HC256-55DI	UV 256K HS EPROM,55NS,IND	CERDIP 28	**27HC256-55I/J**
Am27HC256-55JI	OTP 256K HS EPROM,55NS,IND	PLCC 32	**27HC256-55I/L**
Am27HC256-55PI	OTP 256K HS EPROM,55NS,IND	PDIP 28	**27HC256-55I/P**
Am27HC256-70DI	UV 256K HS EPROM,70NS,IND	CERDIP 28	**27HC256-70I/J**
Am27HC256-70LI	UV 256K HS EPROM,70NS,IND	LCC 32	**27HC256-70I/K**
Am27HC256-70JI	OTP 256K HS EPROM,70NS,IND	PLCC 32	**27HC256-70I/L**
Am27HC256-70PI	OTP 256K HS EPROM,70NS,IND	PDIP 28	**27HC256-70I/P**

TI Part Number	Description	Microchip Part Number	
TMS27C128-12JL	UV 128K EPROM,120NS	CERDIP 28	**27C128-12/J**
TMS27PC128-12FML	OTP 128K EPROM,120NS	PLCC 32	**27C128-12/L**
TMS27PC128-12NL	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**
TMS27C128-15JL	UV 128K EPROM,150NS	CERDIP 28	**27C128-15/J**
TMS27PC128-15FML	OTP 128K EPROM,150NS	PLCC 32	**27C128-15/L**
TMS27PC128-15NL	OTP 128K EPROM,150NS	PDIP 28	**27C128-15/P**
TMS27C128-20JL	UV 128K EPROM,200NS	CERDIP 28	**27C128-20/J**
TMS27PC128-20FML	OTP 128K EPROM,200NS	PLCC 32	**27C128-20/L**
TMS27PC128-20NL	OTP 128K EPROM,200NS	PDIP 28	**27C128-20/P**
TMS27C128-25JL	UV 128K EPROM,250NS	CERDIP 28	**27C128-25/J**
TMS27PC128-25FML	OTP 128K EPROM,250NS	PLCC 32	**27C128-25/L**

TI Part Number	Description	Microchip Part Number	
TMS27PC128-25NL	OTP 128K EPROM,250NS	PDIP 28	**27C128-25/P**
TMS27C128-15JE	UV 128K EPROM,150NS,IND	CERDIP 28	**27C128-15I/J**
TMS27PC128-15FME	OTP 128K EPROM,150NS,IND	PLCC 32	**27C128-15I/L**
TMS27PC128-15NE	OTP 128K EPROM,150NS,IND	PDIP 28	**27C128-15I/P**
TMS27C128-20JE	UV 128K EPROM,200NS,IND	CERDIP 28	**27C128-20I/J**
TMS27PC128-20FME	OTP 128K EPROM,200NS,IND	PLCC 32	**27C128-20I/L**
TMS27PC128-20NE	OTP 128K EPROM,200NS,IND	PDIP 28	**27C128-20I/P**
TMS27C128-25JE	UV 128K EPROM,250NS,IND	CERDIP 28	**27C128-25I/J**
TMS27PC128-25FME	OTP 128K EPROM,250NS,IND	PLCC 32	**27C128-25I/L**
TMS27PC128-25NE	OTP 128K EPROM,250NS,IND	PDIP 28	**27C128-25I/P**
TMS27C256-10JL	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
TMS27PC256-10FML	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
TMS27PC256-10NL	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
TMS27C256-12JL	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
TMS27PC256-12FML	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
TMS27PC256-12NL	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
TMS27C256-15JL	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
TMS27PC256-15FML	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
TMS27PC256-15NL	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
TMS27C256-20JL	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
TMS27PC256-20FML	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
TMS27PC256-20NL	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
TMS27C256-10JE	UV 256K EPROM,100NS,IND	CERDIP 28	**27C256-10I/J**
TMS27PC256-10FME	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256-10I/L**
TMS27PC256-10NE	OTP 256K EPROM,100NS,IND	PDIP 28	**27C256-10I/P**
TMS27C256-12JE	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
TMS27PC256-12FME	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
TMS27PC256-12NE	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
TMS27C256-15JE	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
TMS27PC256-15FME	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
TMS27PC256-15NE	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
TMS27C256-20JE	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
TMS27PC256-20FME	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
TMS27PC256-20NE	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
TMS27C512-10JL	UV 512K EPROM,100NS	CERDIP 28	**27C512-10/J**
TMS27PC512-10FML	OTP 512K EPROM,100NS	PLCC 32	**27C512-10/L**
TMS27PC512-10NL	OTP 512K EPROM,100NS	PDIP 28	**27C512-10/P**
TMS27C512-12JL	UV 512K EPROM,120NS	CERDIP 28	**27C512-12/J**
TMS27PC512-12FML	OTP 512K EPROM,120NS	PLCC 32	**27C512-12/L**
TMS27PC512-12NL	OTP 512K EPROM,120NS	PDIP 28	**27C512-12/P**
TMS27C512-15JL	UV 512K EPROM,150NS	CERDIP 28	**27C512-15/J**
TMS27PC512-15FML	OTP 512K EPROM,150NS	PLCC 32	**27C512-15/L**
TMS27PC512-15NL	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
TMS27C512-20JL	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
TMS27PC512-20FML	OTP 512K EPROM,200NS	PLCC 32	**27C512-20/L**
TMS27PC512-20NL	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**

TI Part Number	Description	Microchip Part Number	
TMS27C512-10JE	UV 512K EPROM,100NS,IND	CERDIP 28	**27C512-10I/J**
TMS27PC512-10FME	OTP 512K EPROM,100NS,IND	PLCC 32	**27C512-10I/L**
TMS27PC512-10NE	OTP 512K EPROM,100NS,IND	PDIP 28	**27C512-10I/P**
TMS27C512-12JE	UV 512K EPROM,120NS,IND	CERDIP 28	**27C512-12I/J**
TMS27PC512-12FME	OTP 512K EPROM,120NS,IND	PLCC 32	**27C512-12I/L**
TMS27PC512-12NE	OTP 512K EPROM,120NS,IND	PDIP 28	**27C512-12I/P**
TMS27C512-15JE	UV 512K EPROM,150NS,IND	CERDIP 28	**27C512-15I/J**
TMS27PC512-15FME	OTP 512K EPROM,150NS,IND	PLCC 32	**27C512-15I/L**
TMS27PC512-15NE	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
TMS27C512-20JE	UV 512K EPROM,200NS,IND	CERDIP 28	**27C512-20I/J**
TMS27PC512-20FME	OTP 512K EPROM,200NS,IND	PLCC 32	**27C512-20I/L**
TMS27PC512-20NE	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**
TMS27C512-80JL	UV 512K EPROM,70NS	CERDIP 28	**27C512A-70/J**
TMS27PC512-80FML	OTP 512K EPROM,70NS	PLCC 32	**27C512A-70/L**
TMS27PC512-80NL	OTP 512K EPROM,70NS	PDIP 28	**27C512A-70/P**
TMS27C512-10JL	UV 512K EPROM,90NS	CERDIP 28	**27C512A-90/J**
TMS27PC512-10FML	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
TMS27PC512-10NL	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
TMS27C512-12JL	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
TMS27PC512-12FML	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
TMS27PC512-12NL	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
TMS27C512-15JL	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
TMS27PC512-15FML	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
TMS27PC512-15NL	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
TMS27C512-20JL	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**
TMS27PC512-20FML	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
TMS27PC512-20NL	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**

SGS Part Number	Description	Microchip Part Number	
M27C64A-15F1	UV 64K EPROM,150NS	CERDIP 28	**27C64-15/J**
M27C64A-15C1	OTP 64K EPROM,150NS	PLCC 32	**27C64-15/L**
M27C64A-15C1TR	OTP 64K EPROM,150NS	PLCC 32	**27C64T-15/L**
M27C64A-20F1	UV 64K EPROM,200NS	CERDIP 28	**27C64-20/J**
M27C64A-20C1	OTP 64K EPROM,200NS	PLCC 32	**27C64-20/L**
M27C64A-20C1TR	OTP 64K EPROM,200NS	PLCC 32	**27C64T-20/L**
M27C64A-25F1	UV 64K EPROM,250NS	CERDIP 28	**27C64-25/J**
M27C64A-25C1	OTP 64K EPROM,250NS	PLCC 32	**27C64-25/L**
M27C64A-25C1TR	OTP 64K EPROM,250NS	PLCC 32	**27C64T-25/L**
M27C64A-15F6	UV 64K EPROM,150NS,IND	CERDIP 28	**27C64-15I/J**
M27C64A-15C6	OTP 64K EPROM,150NS,IND	PLCC 32	**27C64-15I/L**
M27C64A-15C6TR	OTP 64K EPROM,150NS,IND	PLCC 32	**27C64T-15I/L**
M27C64A-20F6	UV 64K EPROM,200NS,IND	CERDIP 28	**27C64-20I/J**
M27C64A-20C6	OTP 64K EPROM,200NS,IND	PLCC 32	**27C64-20I/L**
M27C64A-20C6TR	OTP 64K EPROM,200NS,IND	PLCC 32	**27C64T-20I/L**
M27C64A-25F6	UV 64K EPROM,250NS,IND	CERDIP 28	**27C64-25I/J**
M27C64A-25C6	OTP 64K EPROM,250NS,IND	PLCC 32	**27C64-25I/L**

SGS Part Number	Description	Microchip Part Number	
M27C64A-25C6TR	OTP 64K EPROM,250NS,IND	PLCC 32	**27C64T-25I/L**
M27C128A-12F1	UV 128K EPROM,120NS	CERDIP 28	**27C128-12/J**
M27C128A-12C1	OTP 128K EPROM,120NS	PLCC 32	**27C128-12/L**
M27C128A-15F1	UV 128K EPROM,150NS	CERDIP 28	**27C128-15/J**
M27C128A-15C1	OTP 128K EPROM,150NS	PLCC 32	**27C128-15/L**
M27C128A-20F1	UV 128K EPROM,200NS	CERDIP 28	**27C128-20/J**
M27C128A-20C1	OTP 128K EPROM,200NS	PLCC 32	**27C128-20/L**
M27C128A-12F6	UV 128K EPROM,120NS,IND	CERDIP 28	**27C128-12I/J**
M27C128A-15F6	UV 128K EPROM,150NS,IND	CERDIP 28	**27C128-15I/J**
M27C128A-15C6	OTP 128K EPROM,150NS,IND	PLCC 32	**27C128-15I/L**
M27C128A-20F6	UV 128K EPROM,200NS,IND	CERDIP 28	**27C128-20I/J**
M27C128A-20C6	OTP 128K EPROM,200NS,IND	PLCC 32	**27C128-20I/L**
M27C256B-90F1	UV 256K EPROM,90NS	CERDIP 28	**27C256-90/J**
M27C256B-90C1	OTP 256K EPROM,90NS	PLCC 32	**27C256-90/L**
M27C256B-90B1	OTP 256K EPROM,90NS	PDIP 28	**27C256-90/P**
M27C256B-90C1	OTP 256K EPROM,90NS	PLCC 32	**27C256T-90/L**
M27C256B-10F1	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
M27C256B-10C1	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
M27C256B-10B1	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
M27C256B-10N1	OTP 256K EPROM,100NS	VSOP 28	**27C256-10/VS**
M27C256B-10C1	OTP 256K EPROM,100NS	PLCC 32	**27C256T-10/L**
M27C256B-12F1	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
M27C256B-12C1	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
M27C256B-12B1	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
M27C256B-12M1*	OTP 256K EPROM,120NS	SOIC 28	**27C256-12/SO**
M27C256B-12N1	OTP 256K EPROM,120NS	VSOP 28	**27C256-12/VS**
M27C256B-12C1	OTP 256K EPROM,120NS	PLCC 32	**27C256T-12/L**
M27C256B-15F1	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
M27C256B-15C1	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
M27C256B-15B1	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
M27C256B-15M1*	OTP 256K EPROM,150NS	SOIC 28	**27C256-15/SO**
M27C256B-15N1	OTP 256K EPROM,150NS	VSOP 28	**27C256-15/VS**
M27C256B-15C1	OTP 256K EPROM,150NS	PLCC 32	**27C256T-15/L**
M27C256B-20F1	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
M27C256B-20C1	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
M27C256B-20B1	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
M27C256B-20M1*	OTP 256K EPROM,200NS	SOIC 28	**27C256-20/SO**
M27C256B-20C1	OTP 256K EPROM,200NS	PLCC 32	**27C256T-20/L**
M27C256B-10F6	UV 256K EPROM,100NS,IND	CERDIP 28	**27C256-10I/J**
M27C256B-10C6	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256-10I/L**
M27C256B-10B6	OTP 256K EPROM,100NS,IND	PDIP 28	**27C256-10I/P**
M27C256B-10C6	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256T-10I/L**
M27C256B-12F6	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
M27C256B-12C6	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
M27C256B-12B6	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
M27C256B-12C6	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256T-12I/L**

SGS Part Number	Description	Microchip Part Number	
M27C256B-15F6	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
M27C256B-15C6	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
M27C256B-15B6	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
M27C256B-15C6	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256T-15I/L**
M27C256B-20F6	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
M27C256B-20C6	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
M27C256B-20B6	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
M27C256B-20C6	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256T-20I/L**
M27C512-90F1	UV 512K EPROM,90NS	CERDIP 28	**27C512-90/J**
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	**27C512-90/L**
M27C512-90B1	OTP 512K EPROM,90NS	PDIP 28	**27C512-90/P**
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	**27C512T-90/L**
M27C512-10F1	UV 512K EPROM,100NS	CERDIP 28	**27C512-10/J**
M27C512-10C1	OTP 512K EPROM,100NS	PLCC 32	**27C512-10/L**
M27C512-10B1	OTP 512K EPROM,100NS	PDIP 28	**27C512-10/P**
M27C512-10C1	OTP 512K EPROM,100NS	PLCC 32	**27C512T-10/L**
M27C512-12F1	UV 512K EPROM,120NS	CERDIP 28	**27C512-12/J**
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	**27C512-12/L**
M27C512-12B1	OTP 512K EPROM,120NS	PDIP 28	**27C512-12/P**
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	**27C512T-12/L**
M27C512-15F1	UV 512K EPROM,150NS	CERDIP 28	**27C512-15/J**
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	**27C512-15/L**
M27C512-15B1	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	**27C512T-15/L**
M27C512-20F1	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	**27C512-20/L**
M27C512-20B1	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	**27C512T-20/L**
M27C512-10F6	UV 512K EPROM,100NS,IND	CERDIP 28	**27C512-10I/J**
M27C512-10C6	OTP 512K EPROM,100NS,IND	PLCC 32	**27C512-10I/L**
M27C512-10B6	OTP 512K EPROM,100NS,IND	PDIP 28	**27C512-10I/P**
M27C512-10C6	OTP 512K EPROM,100NS,IND	PLCC 32	**27C512T-10I/L**
M27C512-12F6	UV 512K EPROM,120NS,IND	CERDIP 28	**27C512-12I/J**
M27C512-12C6	OTP 512K EPROM,120NS,IND	PLCC 32	**27C512-12I/L**
M27C512-12B6	OTP 512K EPROM,120NS,IND	PDIP 28	**27C512-12I/P**
M27C512-12C6	OTP 512K EPROM,120NS,IND	PLCC 32	**27C512T-12I/L**
M27C512-15F6	UV 512K EPROM,150NS,IND	CERDIP 28	**27C512-15I/J**
M27C512-15C6	OTP 512K EPROM,150NS,IND	PLCC 32	**27C512-15I/L**
M27C512-15B6	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
M27C512-15C6	OTP 512K EPROM,150NS,IND	PLCC 32	**27C512T-15I/L**
M27C512-20F6	UV 512K EPROM,200NS,IND	CERDIP 28	**27C512-20I/J**
M27C512-20C6	OTP 512K EPROM,200NS,IND	PLCC 32	**27C512-20I/L**
M27C512-20B6	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**
M27C512-20C6	OTP 512K EPROM,200NS,IND	PLCC 32	**27C512T-20I/L**
M27C512-80F1	UV 512K EPROM,70NS	CERDIP 28	**27C512A-70/J**
M27C512-80C1	OTP 512K EPROM,70NS	PLCC 32	**27C512A-70/L**

SGS Part Number	Description	Microchip Part Number	
M27C512-80B1	OTP 512K EPROM,70NS	PDIP 28	**27C512A-70/P**
M27C512-80C1	OTP 512K EPROM,70NS	PLCC 32	**27C512AT-70/L**
M27C512-90F1	UV 512K EPROM,90NS	CERDIP 28	**27C512A-90/J**
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
M27C512-90B1	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
M27C512-90C1	OTP 512K EPROM,90NS	PLCC 32	**27C512AT-90/L**
M27C512-12F1	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
M27C512-12B1	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
M27C512-12C1	OTP 512K EPROM,120NS	PLCC 32	**27C512AT-12/L**
M27C512-15F1	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
M27C512-15B1	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
M27C512-15C1	OTP 512K EPROM,150NS	PLCC 32	**27C512AT-15/L**
M27C512-20F1	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
M27C512-20B1	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**
M27C512-20C1	OTP 512K EPROM,200NS	PLCC 32	**27C512AT-20/L**
M27V512-200K1	OTP 512K EPROM,3V,200NS	PLCC 32	**27LV512-20/L**
M27V512-250K1	OTP 512K EPROM,3V,250NS	PLCC 32	**27LV512-25/L**
M27V512-300K1	OTP 512K EPROM,3V,300NS	PLCC 32	**27LV512-30/L**
M27V512-200K6	OTP 512K EPROM,3V,200NS,IND	PLCC 32	**27LV512-20I/L**
M27V512-250K6	OTP 512K EPROM,3V,250NS,IND	PLCC 32	**27LV512-25I/L**
M27V512-300K6	OTP 512K EPROM,3V,300NS,IND	PLCC 32	**27LV512-30I/L**
27C64A-1Q	UV 64K EPROM,150NS	CERDIP 28	**27C64-15/J**
27C64A-20Q	UV 64K EPROM,200NS	CERDIP 28	**27C64-20/J**
27C64A-25Q	UV 64K EPROM,250NS	CERDIP 28	**27C64-25/J**
27C64A-1T	UV 64K EPROM,150NS,IND	CERDIP 28	**27C64-15I/J**
27C64A-20T	UV 64K EPROM,200NS,IND	CERDIP 28	**27C64-20I/J**
27C64A-25Q	UV 64K EPROM,250NS,IND	CERDIP 28	**27C64-25I/J**
27128A-1Q	UV 128K EPROM,150NS	CERDIP 28	**27C128-15/J**
27128A-20Q	UV 128K EPROM,200NS	CERDIP 28	**27C128-20/J**
27128A-25Q	UV 128K EPROM,250NS	CERDIP 28	**27C128-25/J**
27128A-1T	UV 128K EPROM,150NS,IND	CERDIP 28	**27C128-15I/J**
27128A-20T	UV 128K EPROM,200NS,IND	CERDIP 28	**27C128-20I/J**
27128A-25T	UV 128K EPROM,250NS,IND	CERDIP 28	**27C128-25I/J**
27C256-120V10Q	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
N27C256-120V10Q	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
P27C256-120V10Q	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
27C256-150V10Q	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
N27C256-150V10Q	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
P27C256-150V10Q	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
27C256-200V10Q	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
N27C256-200V10Q	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
P27C256-200V10Q	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
27C256-120V10T	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**

SGS Part Number	Description	Microchip Part Number	
N27C256-120V10T	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
P27C256-120V10T	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
27C256-150V10T	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
N27C256-150V10T	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
P27C256-150V10T	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
27C256-200V10T	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
N27C256-200V10T	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
P27C256-200V10T	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
27C512-120V10Q	UV 512K EPROM,120NS	CERDIP 28	**27C512-12/J**
27C512-150V10Q	UV 512K EPROM,150NS	CERDIP 28	**27C512-15/J**
27C512-200V10Q	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
27C512-120V10T	UV 512K EPROM,120NS,IND	CERDIP 28	**27C512-12I/J**
27C512-150V10T	UV 512K EPROM,150NS,IND	CERDIP 28	**27C512-15I/J**
27C512-200V10T	UV 512K EPROM,200NS,IND	CERDIP 28	**27C512-20I/J**
27C512-120V10Q	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
27C512-150V10Q	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
27C512-200V10Q	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**

Toshiba Part Number	Description	Microchip Part Number	
TC57256AD-12/-120	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
TC57256AD-15/-150	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
TC57256AD-20	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
TC54256AP-15	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
TC54256AF-20*	OTP 256K EPROM,150NS,IND	SOIC 28	**27C256-15I/SO**
TC57512AD-15	UV 512K EPROM,150NS	LCC 32	**27C512-15/K**
TC54512AP-15	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
TC54512AF-15*	OTP 512K EPROM,150NS	SOIC 28	**27C512-15/SO**
TC57512AD-20	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
TC54512AP-20	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
TC54512AF-20*	OTP 512K EPROM,200NS	SOIC 28	**27C512-20/SO**
TC54512AP-17	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
TC54512AP-20	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**
TC57H256D-70/-85	UV 256K HS EPROM,70NS	CERDIP 28	**27HC256-70/J**

National Part Number	Description	Microchip Part Number	
NM27C64Q150	UV 64K EPROM,150NS	CERDIP 28	**27C64-15/J**
NM27C64N150	OTP 64K EPROM,150NS	PDIP 28	**27C64-15/P**
NM27C64Q200	UV 64K EPROM,200NS	CERDIP 28	**27C64-20/J**
NM27C64N200	OTP 64K EPROM,200NS	PDIP 28	**27C64-20/P**
NM27C64QE150	UV 64K EPROM,150NS,IND	CERDIP 28	**27C64-15I/J**
NM27C64NE150	OTP 64K EPROM,150NS,IND	PDIP 28	**27C64-15I/P**
NM27C128Q150	UV 128K EPROM,120NS	CERDIP 28	**27C128-12/J**
NM27C128N150	OTP 128K EPROM,120NS	PDIP 28	**27C128-12/P**
NM27C128Q200	UV 128K EPROM,200NS	CERDIP 28	**27C128-20/J**
NM27C128N200	OTP 128K EPROM,200NS	PDIP 28	**27C128-20/P**
NM27C128QE150	UV 128K EPROM,150NS,IND	CERDIP 28	**27C128-15I/J**

National Part Number	Description	Microchip Part Number	
NM27C128NE150	OTP 128K EPROM,150NS,IND	PDIP 28	**27C128-15I/P**
NM27C256Q100	UV 256K EPROM,100NS	CERDIP 28	**27C256-10/J**
NM27C256V100	OTP 256K EPROM,100NS	PLCC 32	**27C256-10/L**
NM27C256N100	OTP 256K EPROM,100NS	PDIP 28	**27C256-10/P**
NM27C256Q120	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
NM27C256V120	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
NM27C256N120	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
NM27C256Q150	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
NM27C256V150	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
NM27C256N150	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
NM27C256Q200	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
NM27C256V200	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
NM27C256N200	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
NM27C256QE100	UV 256K EPROM,100NS,IND	CERDIP 28	**27C256-10I/J**
NM27C256VE100	OTP 256K EPROM,100NS,IND	PLCC 32	**27C256-10I/L**
NM27C256NE100	OTP 256K EPROM,100NS,IND	PDIP 28	**27C256-10I/P**
NM27C256QE120	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
NM27C256VE120	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
NM27C256NE120	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
NM27C256QE150	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
NM27C256VE150	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
NM27C256NE150	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
NM27C256QE200	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
NM27C256VE200	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
NM27C256NE200	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
NM27C512Q120	UV 512K EPROM,120NS	CERDIP 28	**27C512-12/J**
NM27C512V120	OTP 512K EPROM,120NS	PLCC 32	**27C512-12/L**
NM27C512N120	OTP 512K EPROM,120NS	PDIP 28	**27C512-12/P**
NM27C512Q150	UV 512K EPROM,150NS	CERDIP 28	**27C512-15/J**
NM27C512V150	OTP 512K EPROM,150NS	PLCC 32	**27C512-15/L**
NM27C512N150	OTP 512K EPROM,150NS	PDIP 28	**27C512-15/P**
NM27C512Q200	UV 512K EPROM,200NS	CERDIP 28	**27C512-20/J**
NM27C512V200	OTP 512K EPROM,200NS	PLCC 32	**27C512-20/L**
NM27C512N200	OTP 512K EPROM,200NS	PDIP 28	**27C512-20/P**
NM27C512QE120	UV 512K EPROM,120NS,IND	CERDIP 28	**27C512-12I/J**
NM27C512VE120	OTP 512K EPROM,120NS,IND	PLCC 32	**27C512-12I/L**
NM27C512NE120	OTP 512K EPROM,120NS,IND	PDIP 28	**27C512-12I/P**
NM27C512QE150	UV 512K EPROM,150NS,IND	CERDIP 28	**27C512-15I/J**
NM27C512VE150	OTP 512K EPROM,150NS,IND	PLCC 32	**27C512-15I/L**
NM27C512NE150	OTP 512K EPROM,150NS,IND	PDIP 28	**27C512-15I/P**
NM27C512QE200	UV 512K EPROM,200NS,IND	CERDIP 28	**27C512-20I/J**
NM27C512VE200	OTP 512K EPROM,200NS,IND	PLCC 32	**27C512-20I/L**
NM27C512NE200	OTP 512K EPROM,200NS,IND	PDIP 28	**27C512-20I/P**
NM27C512Q120	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
NM27C512V120	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
NM27C512N120	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**

National Part Number	Description	Microchip Part Number	
NM27C512Q150	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
NM27C512V150	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
NM27C512N150	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
NM27C512Q200	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**
NM27C512V200	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
NM27C512N200	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**

Atmel Part Number	Description	Microchip Part Number	
AT27C256R-90DC	UV 256K EPROM,90NS	CERDIP 28	**27C256-90/J**
AT27C256R-90JC	OTP 256K EPROM,90NS	PLCC 32	**27C256-90/L**
AT27C256R-90PC	OTP 256K EPROM,90NS	PDIP 28	**27C256-90/P**
AT27C256R-90RC*	OTP 256K EPROM,90NS	SOIC 28	**27C256-90/SO**
AT27C256R-90TC	OTP 256K EPROM,90NS	VSOP 28	**27C256-90/VS**
AT27C256R-12DC	UV 256K EPROM,120NS	CERDIP 28	**27C256-12/J**
AT27C256R-12LC	UV 256K EPROM,120NS	LCC 32	**27C256-12/K**
AT27C256R-12JC	OTP 256K EPROM,120NS	PLCC 32	**27C256-12/L**
AT27C256R-12PC	OTP 256K EPROM,120NS	PDIP 28	**27C256-12/P**
AT27C256R-12RC*	OTP 256K EPROM,120NS	SOIC 28	**27C256-12/SO**
AT27C256R-12TC	OTP 256K EPROM,120NS	VSOP 28	**27C256-12/VS**
AT27C256R-15DC	UV 256K EPROM,150NS	CERDIP 28	**27C256-15/J**
AT27C256R-15LC	UV 256K EPROM,150NS	LCC 32	**27C256-15/K**
AT27C256R-15JC	OTP 256K EPROM,150NS	PLCC 32	**27C256-15/L**
AT27C256R-15PC	OTP 256K EPROM,150NS	PDIP 28	**27C256-15/P**
AT27C256R-15RC*	OTP 256K EPROM,150NS	SOIC 28	**27C256-15/SO**
AT27C256R-15TC	OTP 256K EPROM,150NS	VSOP 28	**27C256-15/VS**
AT27C256R-20DC	UV 256K EPROM,200NS	CERDIP 28	**27C256-20/J**
AT27C256R-20LC	UV 256K EPROM,200NS	LCC 32	**27C256-20/K**
AT27C256R-20JC	OTP 256K EPROM,200NS	PLCC 32	**27C256-20/L**
AT27C256R-20PC	OTP 256K EPROM,200NS	PDIP 28	**27C256-20/P**
AT27C256R-20RC*	OTP 256K EPROM,200NS	SOIC 28	**27C256-20/SO**
AT27C256R-20TC	OTP 256K EPROM,200NS	VSOP 28	**27C256-20/VS**
AT27C256R-12DI	UV 256K EPROM,120NS,IND	CERDIP 28	**27C256-12I/J**
AT27C256R-12LI	UV 256K EPROM,120NS,IND	LCC 32	**27C256-12I/K**
AT27C256R-12JI	OTP 256K EPROM,120NS,IND	PLCC 32	**27C256-12I/L**
AT27C256R-12PI	OTP 256K EPROM,120NS,IND	PDIP 28	**27C256-12I/P**
AT27C256R-12RI*	OTP 256K EPROM,120NS,IND	SOIC 28	**27C256-12I/SO**
AT27C256R-15DI	UV 256K EPROM,150NS,IND	CERDIP 28	**27C256-15I/J**
AT27C256R-15LI	UV 256K EPROM,150NS,IND	LCC 32	**27C256-15I/K**
AT27C256R-15JI	OTP 256K EPROM,150NS,IND	PLCC 32	**27C256-15I/L**
AT27C256R-15PI	OTP 256K EPROM,150NS,IND	PDIP 28	**27C256-15I/P**
AT27C256R-15RI*	OTP 256K EPROM,150NS,IND	SOIC 28	**27C256-15I/SO**
AT27C256R-20DI	UV 256K EPROM,200NS,IND	CERDIP 28	**27C256-20I/J**
AT27C256R-20LI	UV 256K EPROM,200NS,IND	LCC 32	**27C256-20I/K**
AT27C256R-20JI	OTP 256K EPROM,200NS,IND	PLCC 32	**27C256-20I/L**
AT27C256R-20PI	OTP 256K EPROM,200NS,IND	PDIP 28	**27C256-20I/P**
AT27C256R-20RI*	OTP 256K EPROM,200NS,IND	SOIC 28	**27C256-20I/SO**

Atmel Part Number	Description	Microchip Part Number	
AT27C512R-90DC	UV 512K EPROM,90NS	CERDIP 28	**27C512A-90/J**
AT27C512R-90LC	UV 512K EPROM,90NS	LCC 32	**27C512A-90/K**
AT27C512R-90JC	OTP 512K EPROM,90NS	PLCC 32	**27C512A-90/L**
AT27C512R-90PC	OTP 512K EPROM,90NS	PDIP 28	**27C512A-90/P**
AT27C512R-90RC*	OTP 512K EPROM,90NS	SOIC 28	**27C512A-90/SO**
AT27C512R-90TC	OTP 512K EPROM,90NS	VSOP 28	**27C512A-90/VS**
AT27C512R-12DC	UV 512K EPROM,120NS	CERDIP 28	**27C512A-12/J**
AT27C512R-12LC	UV 512K EPROM,120NS	LCC 32	**27C512A-12/K**
AT27C512R-12JC	OTP 512K EPROM,120NS	PLCC 32	**27C512A-12/L**
AT27C512R-12PC	OTP 512K EPROM,120NS	PDIP 28	**27C512A-12/P**
AT27C512R-12RC*	OTP 512K EPROM,120NS	SOIC 28	**27C512A-12/SO**
AT27C512R-12TC	OTP 512K EPROM,120NS	VSOP 28	**27C512A-12/VS**
AT27C512R-15DC	UV 512K EPROM,150NS	CERDIP 28	**27C512A-15/J**
AT27C512R-15LC	UV 512K EPROM,150NS	LCC 32	**27C512A-15/K**
AT27C512R-15JC	OTP 512K EPROM,150NS	PLCC 32	**27C512A-15/L**
AT27C512R-15PC	OTP 512K EPROM,150NS	PDIP 28	**27C512A-15/P**
AT27C512R-15RC*	OTP 512K EPROM,150NS	SOIC 28	**27C512A-15/SO**
AT27C512R-15TC	OTP 512K EPROM,150NS	VSOP 28	**27C512A-15/VS**
AT27C512R-20DC	UV 512K EPROM,200NS	CERDIP 28	**27C512A-20/J**
AT27C512R-20LC	UV 512K EPROM,200NS	LCC 32	**27C512A-20/K**
AT27C512R-20JC	OTP 512K EPROM,200NS	PLCC 32	**27C512A-20/L**
AT27C512R-20PC	OTP 512K EPROM,200NS	PDIP 28	**27C512A-20/P**
AT27C512R-20RC*	OTP 512K EPROM,200NS	SOIC 28	**27C512A-20/SO**
AT27HC256R-55DC	UV 256K HS EPROM,55NS	CERDIP 28	**27HC256-55/J**
AT27HC256R-55LC	UV 256K HS EPROM,55NS	LCC 32	**27HC256-55/K**
AT27HC256R-70DC	UV 256K HS EPROM,70NS	CERDIP 28	**27HC256-70/J**
AT27HC256R-70LC	UV 256K HS EPROM,70NS	LCC 32	**27HC256-70/K**
AT27HC256R-70JC	OTP 256K HS EPROM,70NS	PLCC 32	**27HC256-70/L**
AT27HC256R-70PC	OTP 256K HS EPROM,70NS	PDIP 28	**27HC256-70/P**
AT27HC256R-90DC	UV 256K HS EPROM,90NS	CERDIP 28	**27HC256-90/J**
AT27HC256R-90LC	UV 256K HS EPROM,90NS	LCC 32	**27HC256-90/K**
AT27HC256R-90JC	OTP 256K HS EPROM,90NS	PLCC 32	**27HC256-90/L**
AT27HC256R-90PC	OTP 256K HS EPROM,90NS	PDIP 28	**27HC256-90/P**
AT27HC256R-55DI	UV 256K HS EPROM,55NS,IND	CERDIP 28	**27HC256-55I/J**
AT27HC256R-55LI	OTP 256K HS EPROM,55NS,IND	PLCC 32	**27HC256-55I/L**
AT27HC256R-70DI	UV 256K HS EPROM,70NS,IND	CERDIP 28	**27HC256-70I/J**
AT27HC256R-70LI	UV 256K HS EPROM,70NS,IND	LCC 32	**27HC256-70I/K**
AT27HC256R-70JI	OTP 256K HS EPROM,70NS,IND	PLCC 32	**27HC256-70I/L**
AT27HC256R-70PI	OTP 256K HS EPROM,70NS,IND	PDIP 28	**27HC256-70I/P**
AT27LV256R-20DC	OTP 256K EPROM,3V,200NS	CERDIP 28	**27LV256-20/J**
AT27LV256R-20LC	OTP 256K EPROM,3V,200NS	LCC 32	**27LV256-20/K**
AT27LV256R-20JC	OTP 256K EPROM,3V,200NS	PLCC 32	**27LV256-20/L**
AT27LV256R-20PC	OTP 256K EPROM,3V,200NS	PDIP 28	**27LV256-20/P**
AT27LV256R-20RC*	OTP 256K EPROM,3V,200NS	SOIC 28	**27LV256-20/SO**
AT27LV256R-20TC	OTP 256K EPROM,3V,200NS	VSOP 28	**27LV256-20/VS**
AT27LV256R-25DC	OTP 256K EPROM,3V,250NS	CERDIP 28	**27LV256-25/J**

Atmel Part Number	Description	Microchip Part Number	
AT27LV256R-25LC	OTP 256K EPROM,3V,250NS	LCC 32	**27LV256-25/K**
AT27LV256R-25JC	OTP 256K EPROM,3V,250NS	PLCC 32	**27LV256-25/L**
AT27LV256R-25PC	OTP 256K EPROM,3V,250NS	PDIP 28	**27LV256-25/P**
AT27LV256R-25RC*	OTP 256K EPROM,3V,250NS	SOIC 28	**27LV256-25/SO**
AT27LV256R-25TC	OTP 256K EPROM,3V,250NS	VSOP 28	**27LV256-25/VS**
AT27LV256R-20DI	OTP 256K EPROM,3V,200NS,IND	CERDIP 28	**27LV256-20I/J**
AT27LV256R-20LI	OTP 256K EPROM,3V,200NS,IND	LCC 32	**27LV256-20I/K**
AT27LV256R-25DI	OTP 256K EPROM,3V,250NS,IND	CERDIP 28	**27LV256-25I/J**
AT27LV256R-25LI	OTP 256K EPROM,3V,250NS,IND	LCC 32	**27LV256-25I/K**
AT27LV512R-20DC	OTP 512K EPROM,3V,200NS	CERDIP 28	**27LV512-20/J**
AT27LV512R-20LC	OTP 512K EPROM,3V,200NS	LCC 32	**27LV512-20/K**
AT27LV512R-20JC	OTP 512K EPROM,3V,200NS	PLCC 32	**27LV512-20/L**
AT27LV512R-20PC	OTP 512K EPROM,3V,200NS	PDIP 28	**27LV512-20/P**
AT27LV512R-20RC*	OTP 512K EPROM,3V,200NS	SOIC 28	**27LV512-20/SO**
AT27LV512R-20TC	OTP 512K EPROM,3V,200NS	VSOP 28	**27LV512-20/VS**
AT27LV512R-25DC	OTP 512K EPROM,3V,250NS	CERDIP 28	**27LV512-25/J**
AT27LV512R-25LC	OTP 512K EPROM,3V,250NS	LCC 32	**27LV512-25/K**
AT27LV512R-25JC	OTP 512K EPROM,3V,250NS	PLCC 32	**27LV512-25/L**
AT27LV512R-25PC	OTP 512K EPROM,3V,250NS	PDIP 28	**27LV512-25/P**
AT27LV512R-25RC*	OTP 512K EPROM,3V,250NS	SOIC 28	**27LV512-25/SO**
AT27LV512R-25TC	OTP 512K EPROM,3V,250NS	VSOP 28	**27LV512-25/VS**
AT27LV512R-20DI	OTP 512K EPROM,3V,200NS,IND	CERDIP 28	**27LV512-20I/J**
AT27LV512R-20LI	OTP 512K EPROM,3V,200NS,IND	LCC 32	**27LV512-20I/K**
AT27LV512R-25DI	OTP 512K EPROM,3V,250NS,IND	CERDIP 28	**27LV512-25I/J**
AT27LV512R-25LI	OTP 512K EPROM,3V,250NS,IND	LCC 32	**27LV512-25I/K**

FIGURE 1-1: ADVANCED MICRO DEVICES

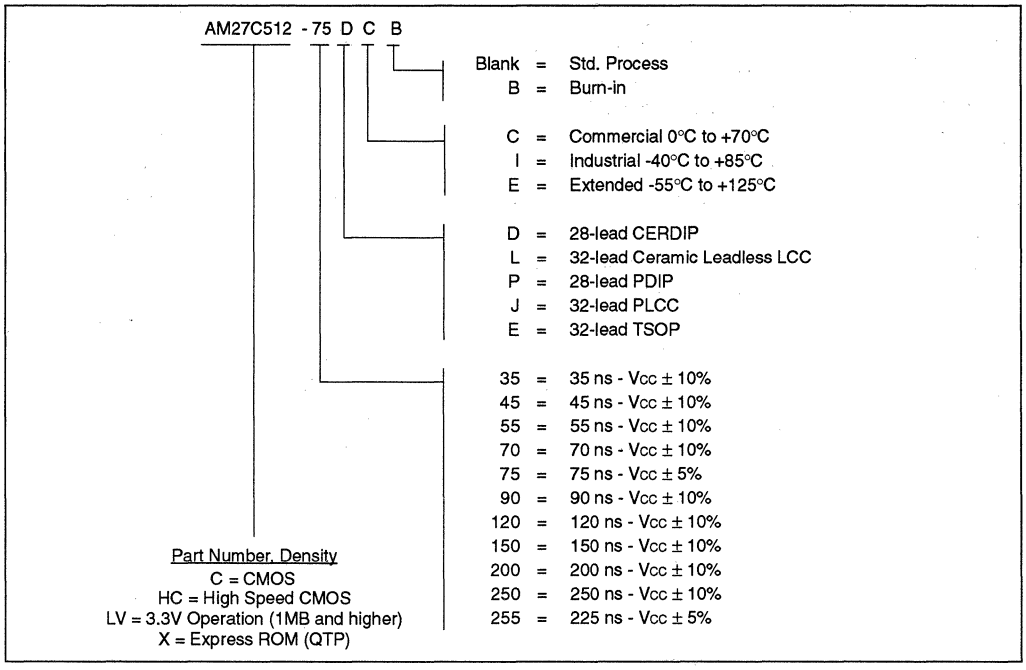


FIGURE 1-2: TEXAS INSTRUMENTS

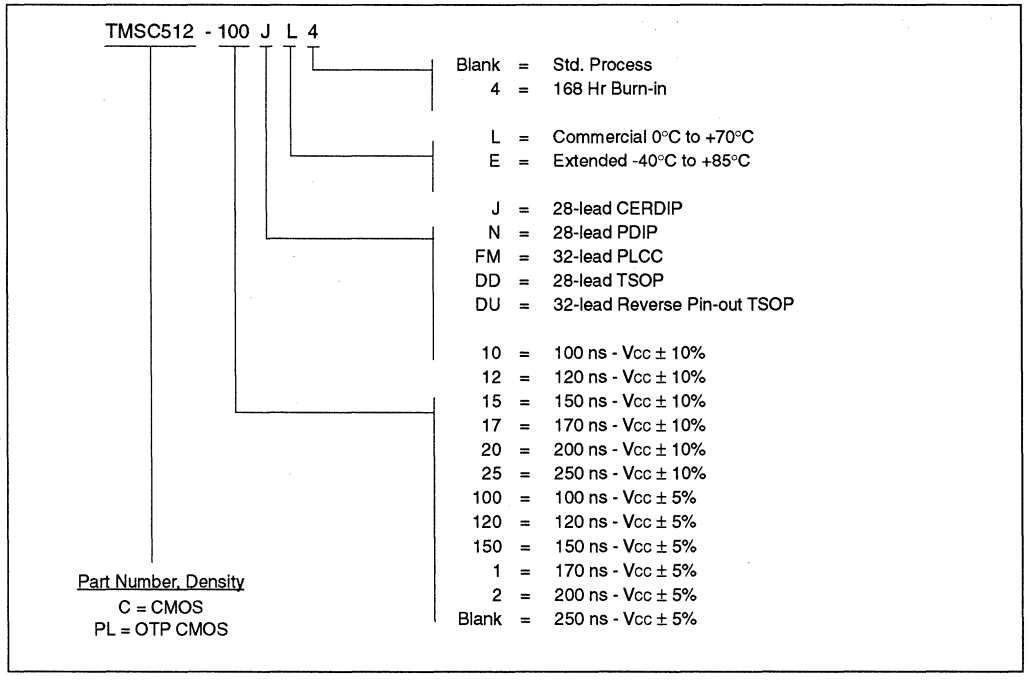


FIGURE 1-3: SGS-THOMSON

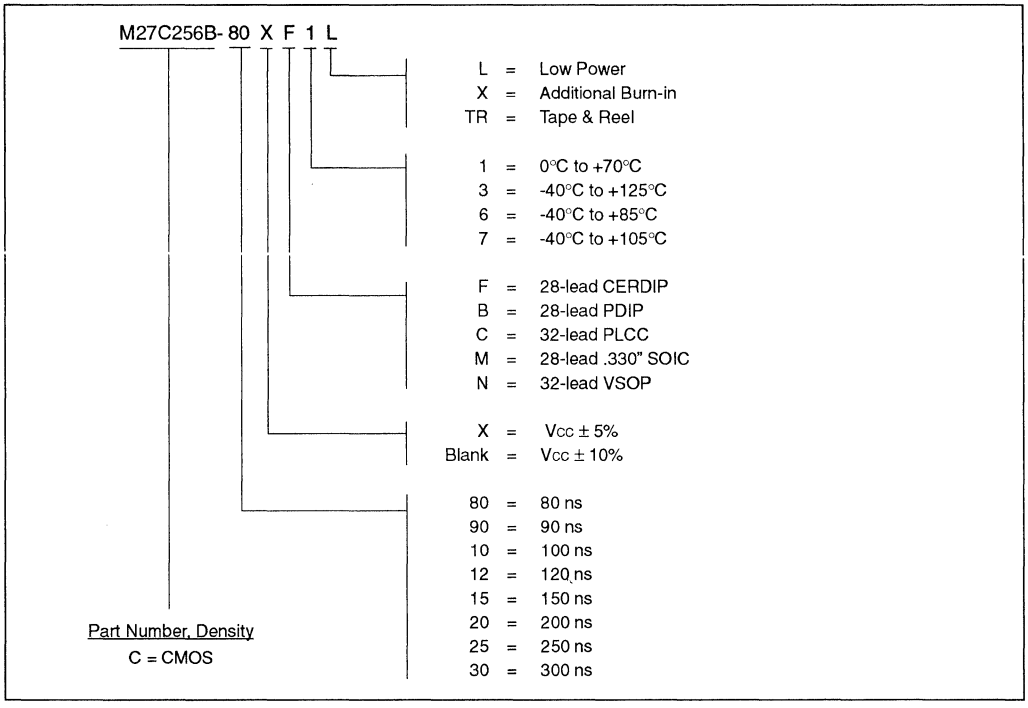


FIGURE 1-4: INTEL CORPORATION

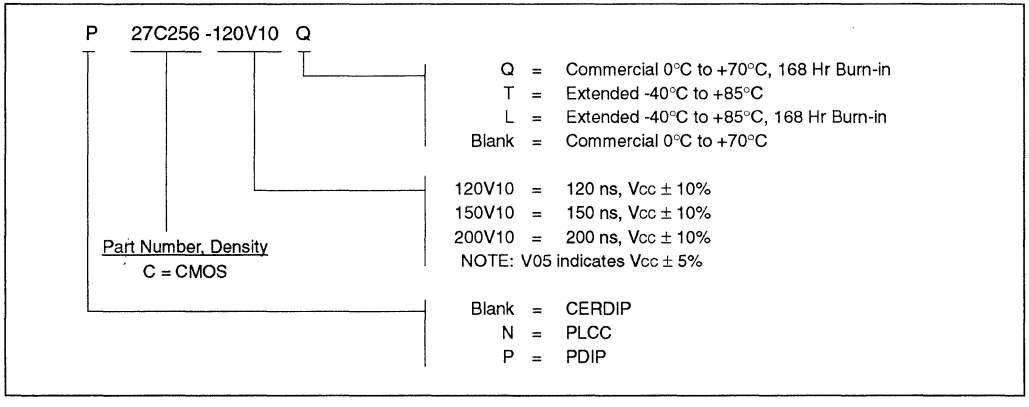


FIGURE 1-5: TOSHIBA CORPORATION

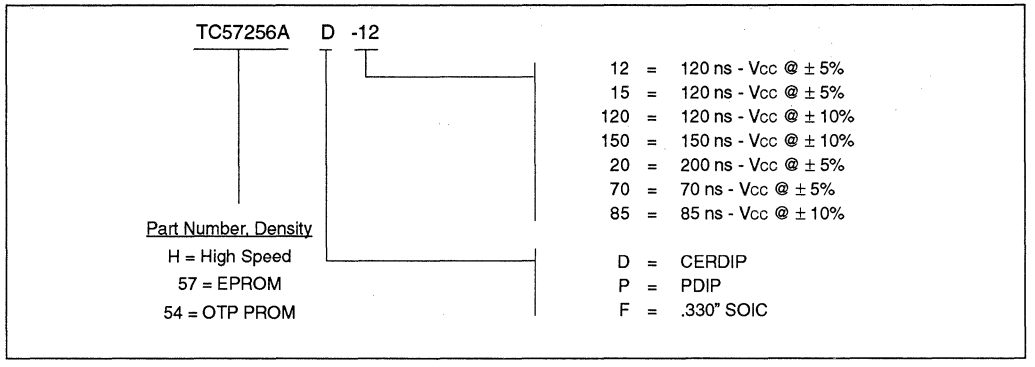


FIGURE 1-6: NATIONAL SEMICONDUCTOR CORPORATION

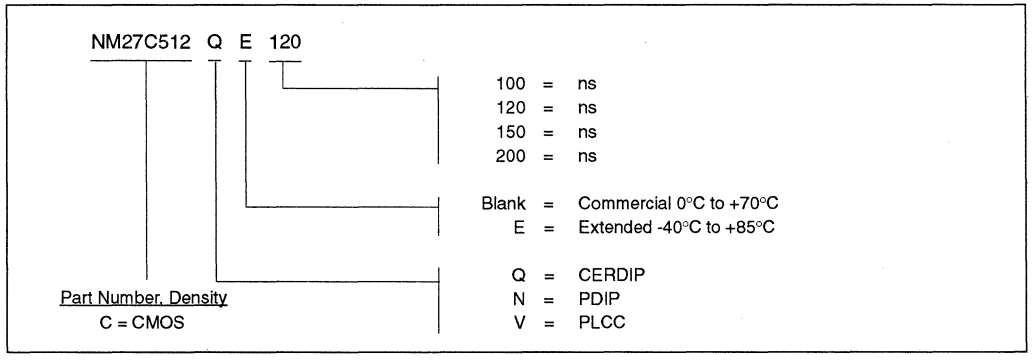


FIGURE 1-7: HITACHI CORPORATION

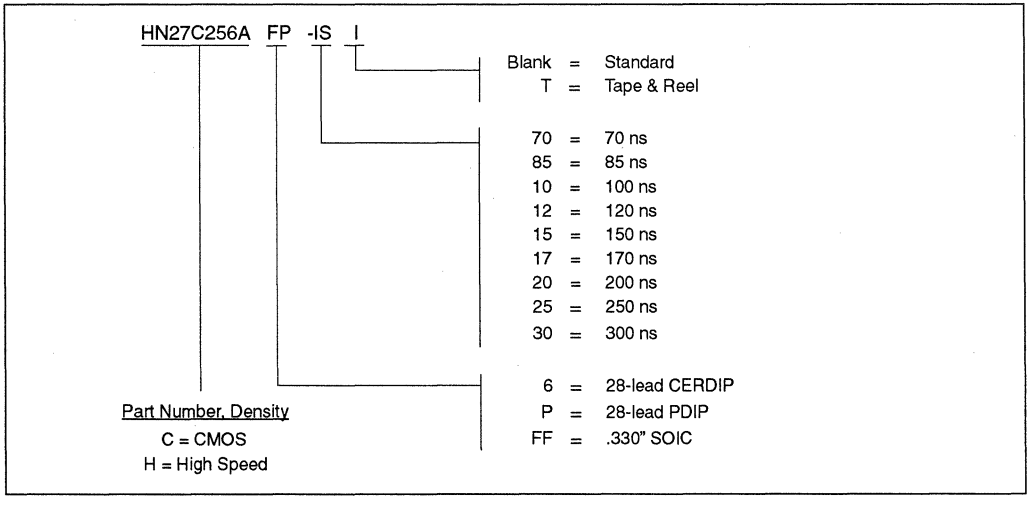


FIGURE 1-8: ATMEL CORPORATION

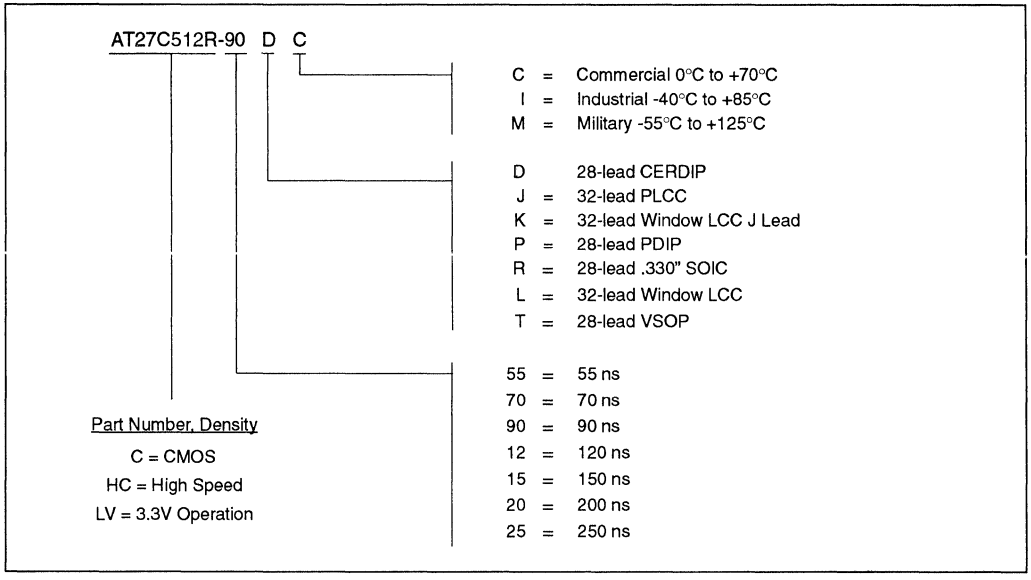
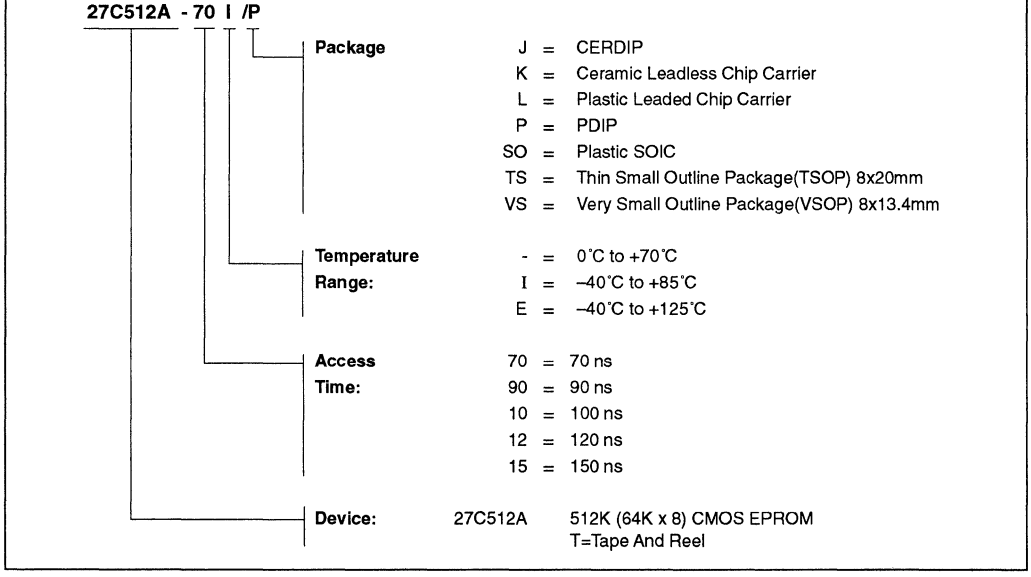


FIGURE 1-9: MICROCHIP TECHNOLOGY INCORPORATED



NOTES

MICROCHIP

SECTION 3
I^2C^{TM} SERIAL EEPROM PRODUCT SPECIFICATIONS

3

24AA01/02	1K/2K 1.8V CMOS Serial EEPROMs	3-1
24AA04/08	4K/8K 1.8V CMOS Serial EEPROMs	3-11
24AA16	16K 1.8V CMOS Serial EEPROM	3-21
24AA164	16K 1.8V Cascadable CMOS Serial EEPROM	3-31
24AA32	32K 1.8V CMOS Serial EEPROM	3-41
24LC01B/02B	1K/2K 2.5V CMOS Serial EEPROMs	3-53
24LC04B/08B	4K/8K 2.5V CMOS Serial EEPROMs	3-63
24LC16B	16K 2.5V CMOS Serial EEPROM	3-73
24LC164	16K 2.5V Cascadable CMOS Serial EEPROM	3-83
24LC32	32K 2.5V CMOS Serial EEPROM	3-93
24C01A/02A/04A	1K/2K/4K 5.0V CMOS Serial EEPROMs	3-105
24C08B/16B	8K/16K 5.0V E-Temperature Serial EEPROMs	3-115
24C32	32K 5.0V CMOS Serial EEPROM	3-125
85C72/82/92	1K/2K/4K 5.0V CMOS Serial EEPROM	3-137

MICROCHIP

24AA01/02

1K/2K 1.8V CMOS Serial EEPROMs

FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 3 µA standby current typical at 1.8V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 3,000V
- **10,000,000 ERASE/WRITE cycles guaranteed on 24AA01**
- **1,000,000 ERASE/WRITE cycles guaranteed on 24AA02***
- Data retention > 40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C

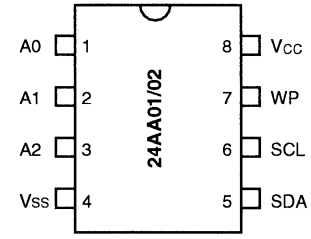
DESCRIPTION

The Microchip Technology Inc. 24AA01 and 24AA02 are 1K bit and 2K bit Electrically Erasable PROMs. The devices are organized as a single block of 128 x 8 bit or 256 x 8 bit memory with a two wire serial interface. Low-voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA, respectively. The 24AA01 and 24AA02 also have page-write capability for up to 8 bytes of data. The 24AA01 and 24AA02 are available in the standard 8-pin DIP and 8-pin surface mount SOIC packages.

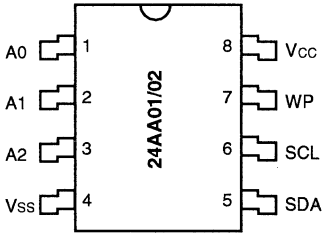
*Future: 10,000,000 E/W cycles guaranteed

PACKAGE TYPE

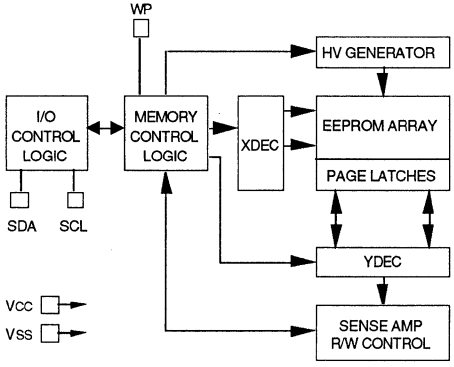
DIP



SOIC



BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}.....7.0V
All inputs and outputs w.r.t. V_{SS} .... -0.6V to V_{CC} +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins .....≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
V_{SS}	Ground
SDA	Serial Address/Data/I/O
SCL	Serial Clock
WP	Write Protect Input
V_{CC}	+1.8V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

		V_{CC} = +1.8V to +5.5V Commercial (C): Tamb = 0°C to +70°C				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:						
High level input voltage	V_{IH}	.7 V_{CC}	—	—	V	
Low level input voltage	V_{IL}	—	—	.3 V_{CC}	V	
Hysteresis of Schmitt trigger inputs	V_{HYS}	.05 V_{DD}	—	—	V	Note 1
Low level output voltage	V_{OL}	—	—	.40	V	I_{OL} = 3.0 mA, V_{CC} = 1.8V
Input leakage current	I_{LI}	-10	—	10	µA	V_{IN} = .1V to 5.5V
Output leakage current	I_{LO}	-10	—	10	µA	V_{OUT} = .1V to 5.5V
Internal capacitance (all inputs/outputs)	C_{INT}	—	—	10	pF	V_{CC} = 5.0V (Note 1) Tamb = 25°C, F_{CLK} = 1 MHz
Operating current	I_{CC} Write	—	—	3	mA	V_{CC} = 5.5V, SCL = 400 kHz
		—	.5	—	mA	V_{CC} = 1.8V, SCL = 100 kHz
	I_{CC} Read	—	—	1	mA	V_{CC} = 5.5V, SCL = 400 kHz
		—	.05	—	mA	V_{CC} = 1.8V, SCL = 100 kHz
Standby current	I_{CCS}	—	—	100	µA	V_{CC} = 5.5V, SDA = SCL = V_{CC}
		—	—	30	µA	V_{CC} = 3.0V, SDA = SCL = V_{CC}
		—	3	—	µA	V_{CC} = 1.8V, SDA = SCL = V_{CC}

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

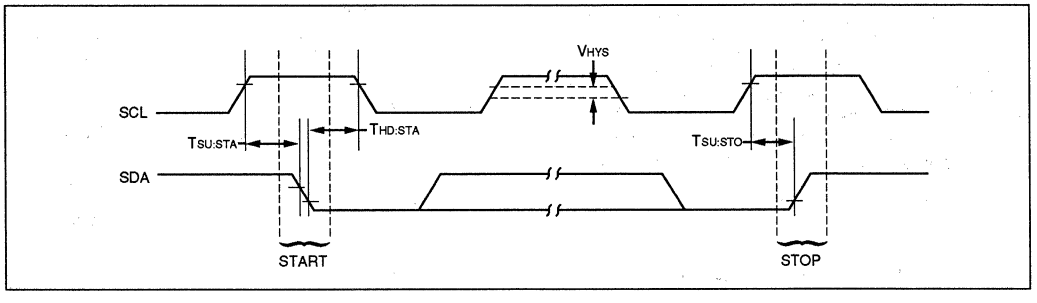


TABLE 1-3: AC CHARACTERISTICS

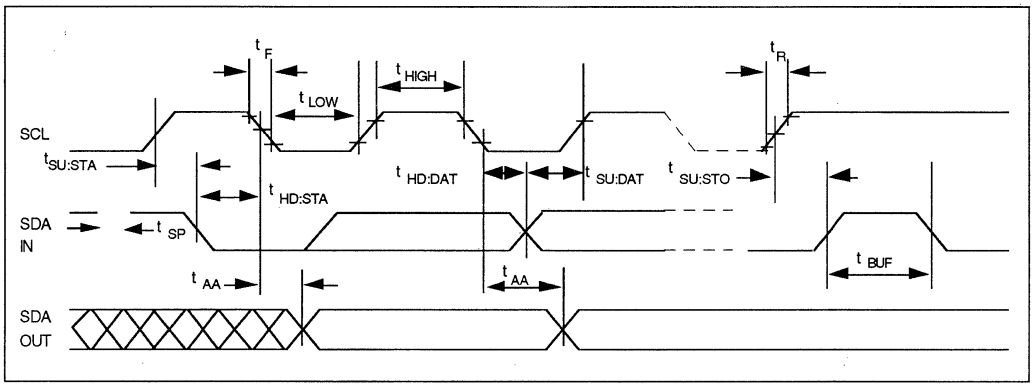
Parameter	Symbol	Standard Mode		Vcc = 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	Note 1
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA01/02 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA01/02 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

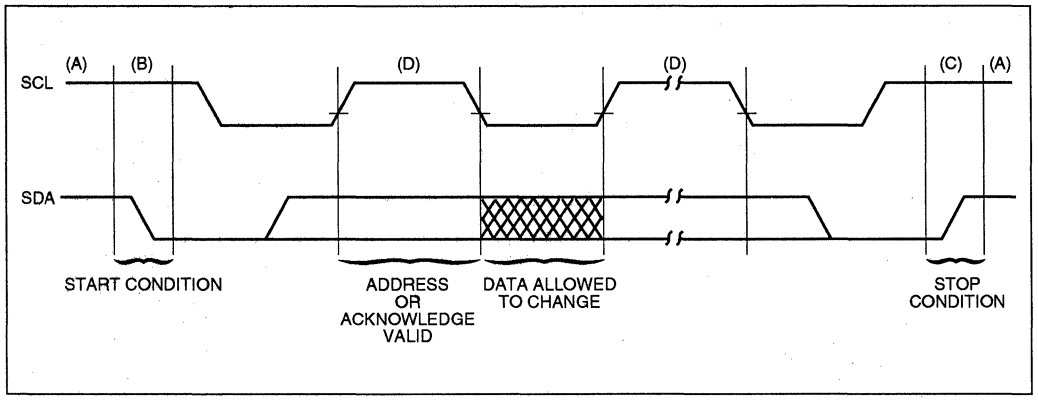
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA01/02 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Slave Address

The 24AA01/02 are software-compatible with older devices such as 24C01A, 24C02A, 24LC01, and 24LC02. A single 24AA02 can be used in place of two 24LC01's, for example, without any modifications to software. The "chip select" portion of the control byte becomes a don't care.

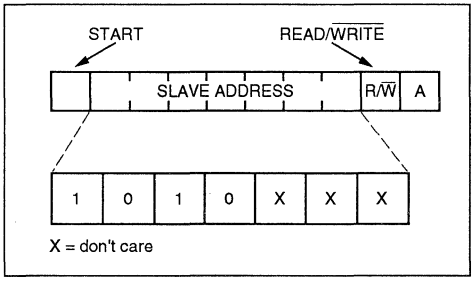
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24AA01/02, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24AA01/02 (see Figure 4-1).

The 24AA01/02 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

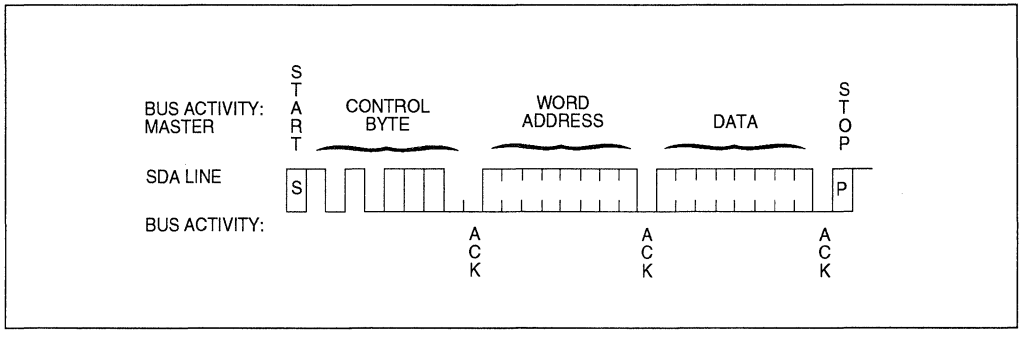
5.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA01/02. After receiving another acknowledge signal from the 24AA01/02 the master device will transmit the data word to be written into the addressed memory location. The 24AA01/02 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA01/02 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA01/02 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24AA01/02 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

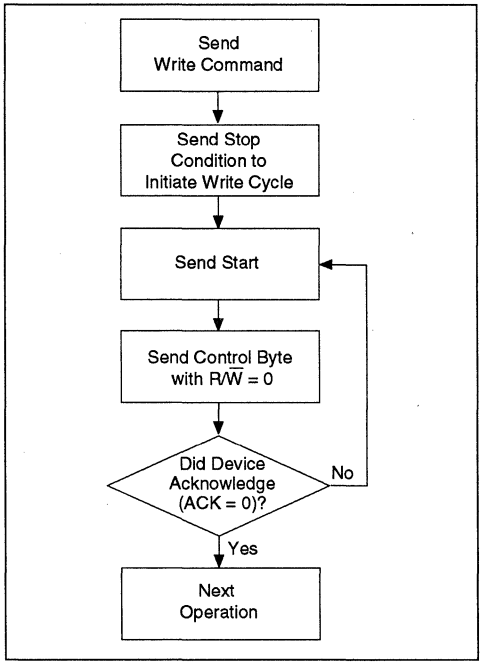
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24AA01/02 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the $R/\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24AA01/02 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with $R/\overline{W}$ bit set to one, the 24AA01/02 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA01/02 discontinues transmission (see Figure 8-2).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA01/02 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the $R/\overline{W}$ bit set to a one. The 24AA01/02 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA01/02 discontinues transmission (see Figure 8-3).

FIGURE 8-1: PAGE WRITE

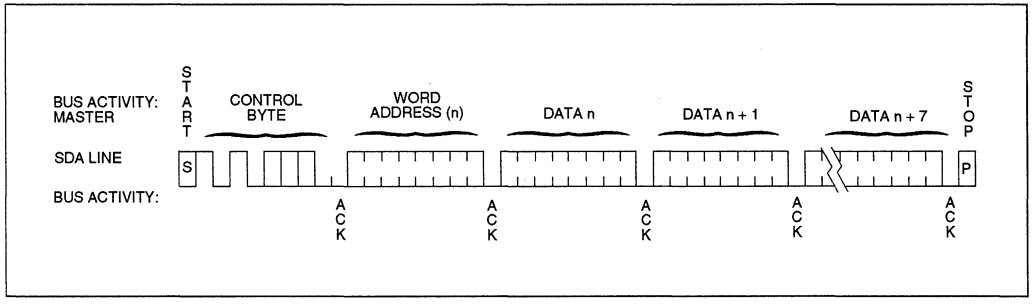


FIGURE 8-2: CURRENT ADDRESS READ

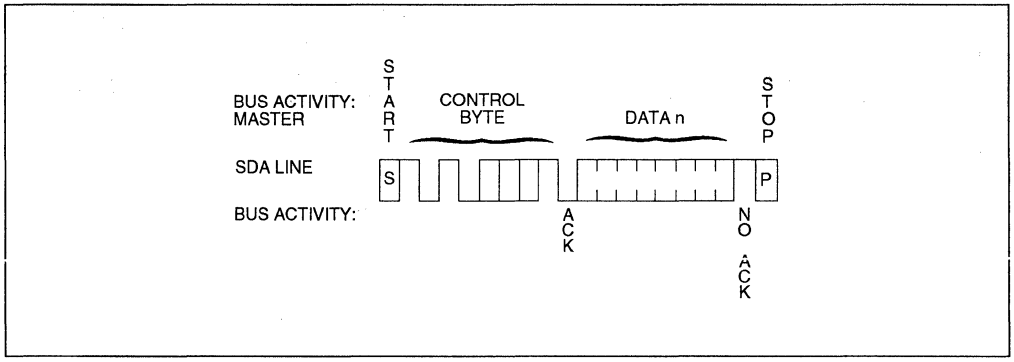
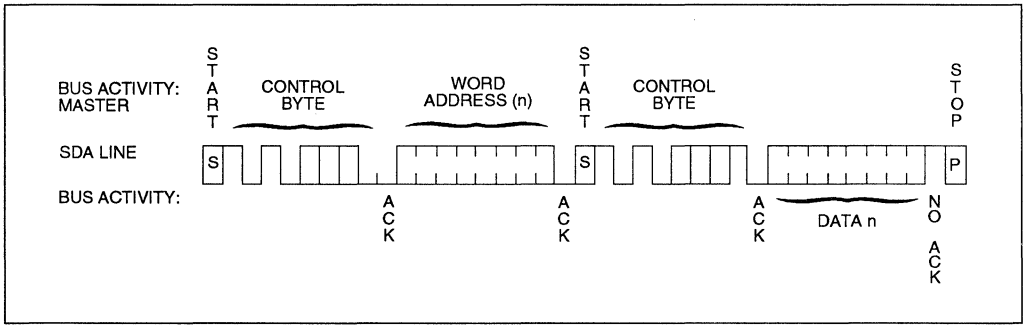


FIGURE 8-3: RANDOM READ



3

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA01/02 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA01/02 to transmit the next sequentially addressed 8 bit word (see Figure 9-1).

To provide sequential reads the 24AA01/02 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24AA01/02 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1K for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

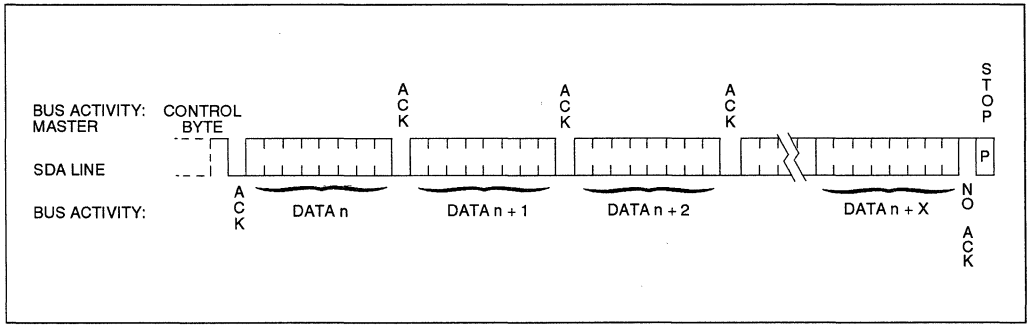
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA01/02 as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are not used by the 24AA01/02. They may be left floating or tied to either Vss or Vcc.

FIGURE 9-1: SEQUENTIAL READ



NOTES

24AA01/02 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24AA01/02 - /P

Package:	P	=	Plastic DIP (300 mil Body), 8-lead
	SN	=	Plastic SOIC (150 mil Body), 8-lead
	SM	=	Plastic SOIC (207 mil Body), 8-lead
Temperature Range:	Blank	=	0°C to +70°C
Device:	24AA01		1.8V, 1K CMOS Serial EEPROM
	24AA01T		1.8V, 1K CMOS Serial EEPROM (Tape and Reel)
	24AA02		1.8V, 2K CMOS Serial EEPROM
	24AA02T		1.8V, 2K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24AA04/08

4K/8K 1.8V CMOS Serial EEPROMs

FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 3 µA standby current typical at 1.8V
- Organized as 2 or 4 blocks of 256 bytes (2 x 256 x 8) or (4 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **1,000,000 ERASE/WRITE cycles guaranteed***
- Data retention > 40 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C

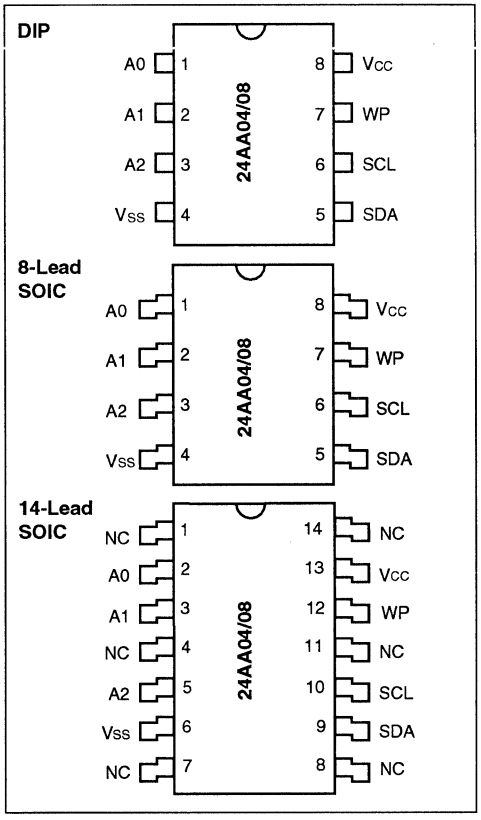
DESCRIPTION

The Microchip Technology Inc. 24AA04/08 is a 4K bit or 8K bit Electrically Erasable PROM. The device is organized as 2 or 4 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA respectively. The 24AA04/08 also has a page-write capability for up to 16 bytes of data. The 24AA04/08 is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

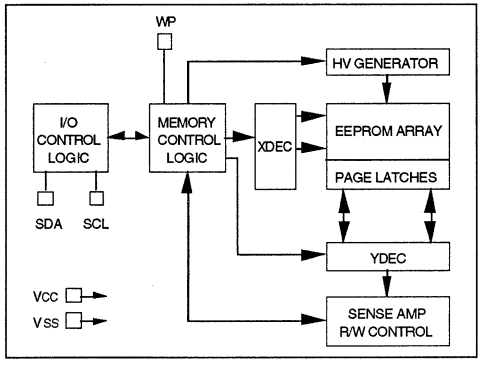
*Future: 10,000,000 E/W cycles guaranteed

I²C is a trademark of Philips Corporation

PACKAGE TYPE



BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS ... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

				VCC = +1.8V to +5.5V Commercial (C): Tamb = 0°C to +70°C		
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:						
High level input voltage	VIH	.7 VCC	—	—	V	
Low Level input voltage	VIL	—	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	—	V	Note 1
Low level output voltage	VOL	—	—	.40	V	IOL = 3.0 mA, VCC = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	—	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC WRITE	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
		—	.05	—	mA	VCC = 1.8V, SCL = 100 kHz
	ICC READ	—	—	1	mA	VCC = 5.5V, SCL = 400 kHz
		—	.05	—	mA	VCC = 1.8V, SCL = 100 kHz
Standby current	ICCS	—		100	µA	VCC = 5.5V, SDA=SCL=VCC
		—		30	µA	VCC = 3.0V, SDA=SCL=VCC
		—	3	—	µA	VCC = 1.8V, SDA=SCL=VCC

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

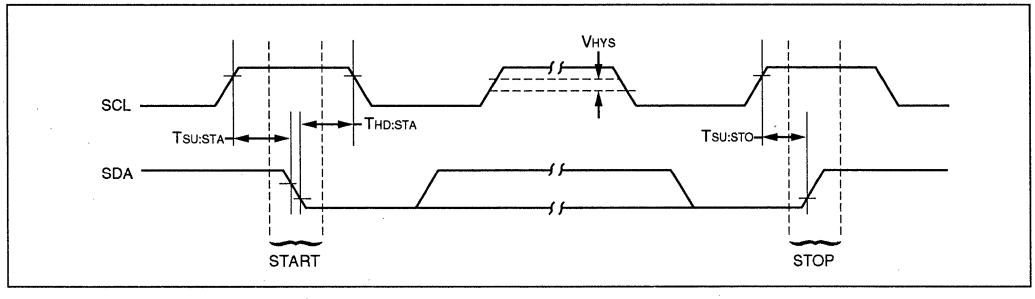
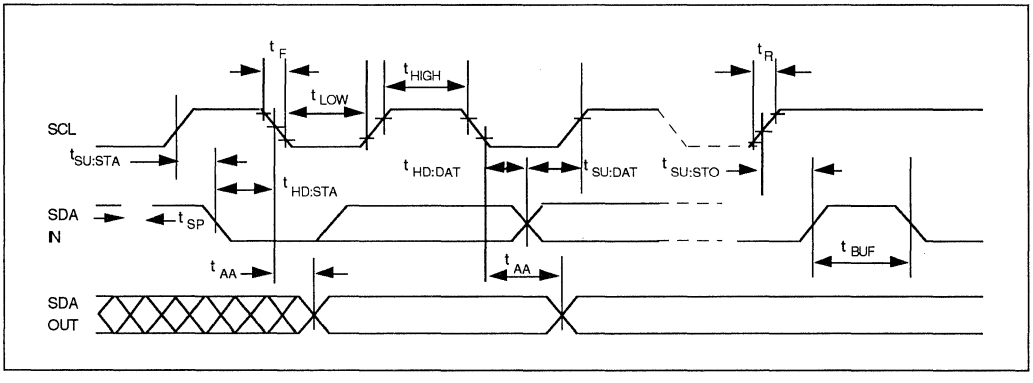


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		Vcc = 4.5-5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA04/08 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA04/08 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

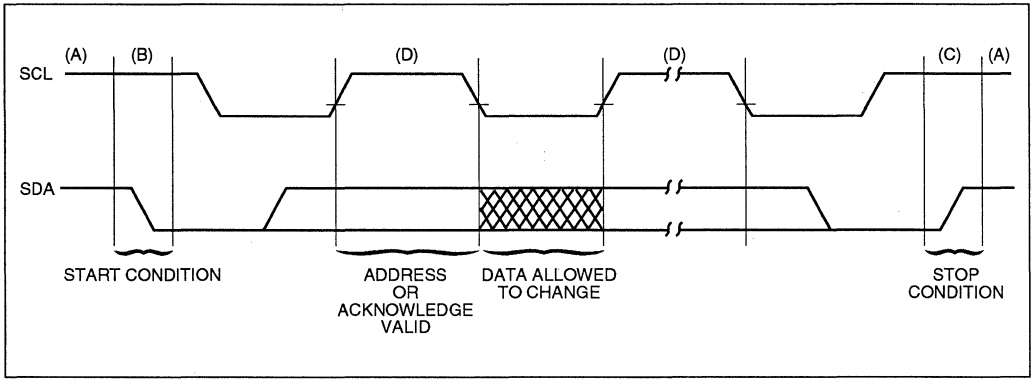
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA04/08 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

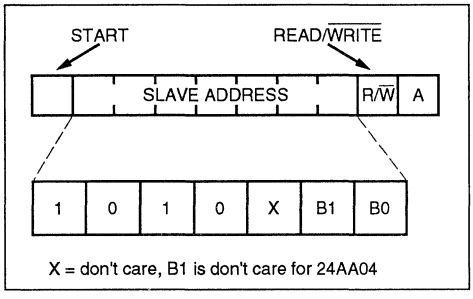
4.1 Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24AA04/08 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). B2 is a don't care for both the 24AA04 and 24AA08; B1 is a don't care for the 24AA04. They are used by the master device to select which of the two or four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA04/08 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA04/08 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

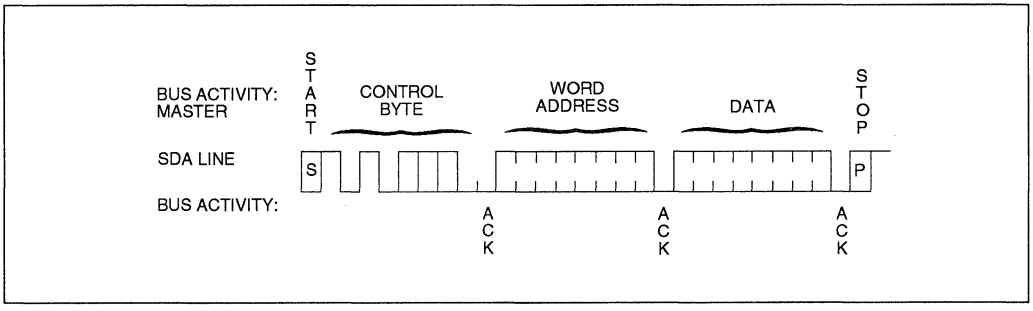
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA04/08. After receiving another acknowledge signal from the 24AA04/08 the master device will transmit the data word to be written into the addressed memory location. The 24AA04/08 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA04/08 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word ad dress and the first data byte are transmitted to the 24AA04/08 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24AA04/08 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

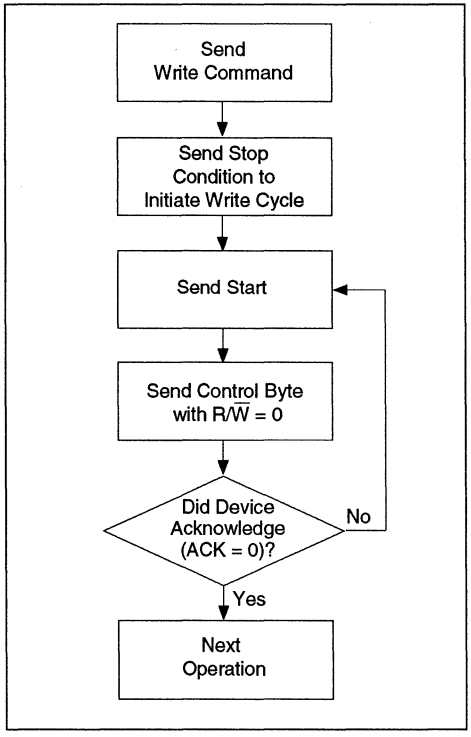
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24AA04/08 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24AA04/08 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA04/08 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA04/08 discontinues transmission (see Figure 8-2).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA04/08 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA04/08 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA04/08 discontinues transmission (see Figure 8-3).

FIGURE 8-1: PAGE WRITE

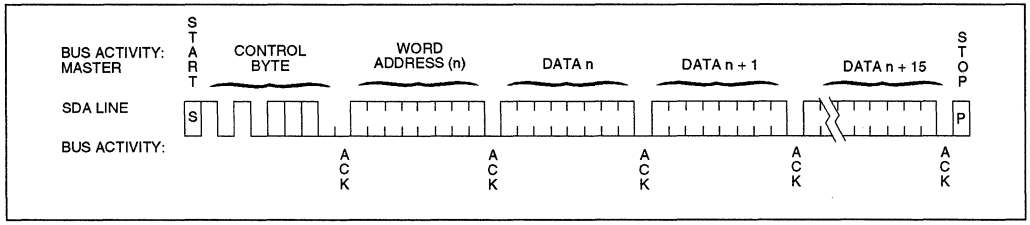


FIGURE 8-2: CURRENT ADDRESS READ

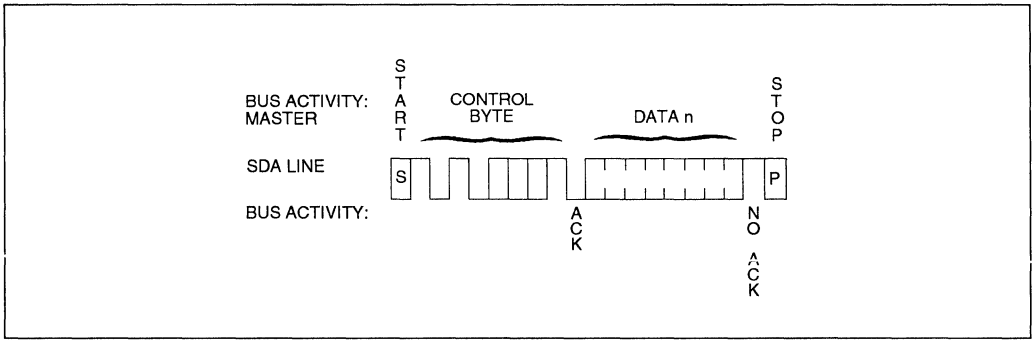
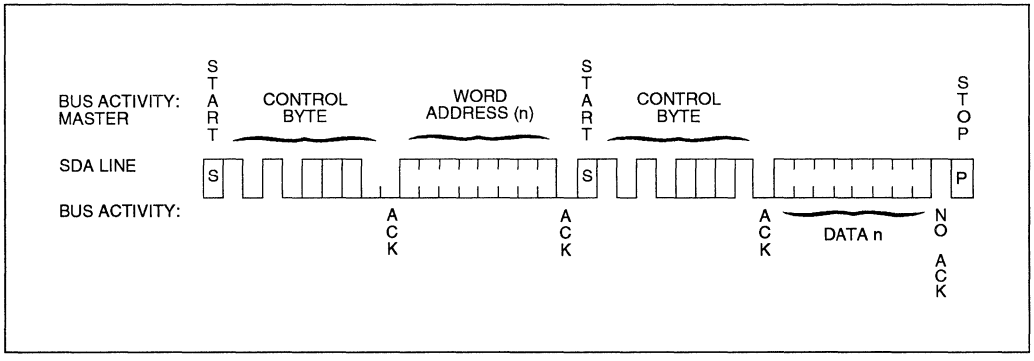


FIGURE 8-3: RANDOM READ



3

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA04/08 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA04/08 to transmit the next sequentially addressed 8 bit word (see Figure 9-1).

To provide sequential reads the 24AA04/08 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24AA04/08 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10Ω for 100 kHz, 1Ω for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

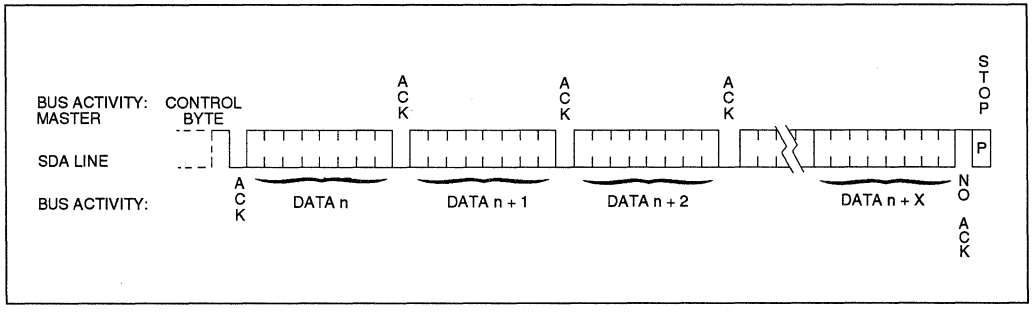
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA04/08 as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are not used by the 24AA04/08. They may be left floating or tied to either Vss or Vcc.

FIGURE 9-1: SEQUENTIAL READ



NOTES

24AA04/08 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24AA04/08 - /P

Package:	P	=	Plastic DIP (300 mil Body), 8-lead
	SL	=	Plastic SOIC (150 mil Body), 14-lead
	SN	=	Plastic SOIC (150 mil Body), 8-lead
	SM	=	Plastic SOIC (207 mil Body), 8-lead
Temperature Range:	Blank	=	0°C to +70°C
Device:	24AA04		1.8V, 4K CMOS Serial EEPROM
	24AA04T		1.8V, 4K CMOS Serial EEPROM (Tape and Reel)
	24AA08		1.8V, 8K CMOS Serial EEPROM
	24AA08T		1.8V, 8K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24AA16

16K 1.8V CMOS Serial EEPROM

FEATURES

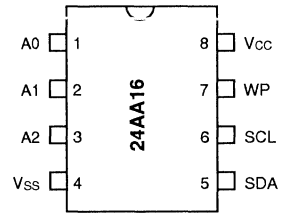
- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 3 µA standby current typical at 1.8V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **10,000,000 ERASE/WRITE cycles guaranteed**
- Data retention > 40 years
- 8 pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C

DESCRIPTION

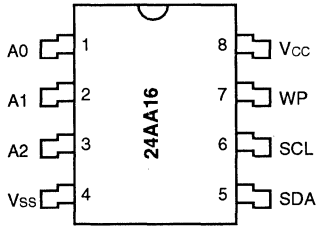
The Microchip Technology Inc. 24AA16 is a 1.8 volt 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 1.8 volts with standby and active currents of only 3 µA and 1 mA, respectively. The 24AA16 also has a page-write capability for up to 16 bytes of data. The 24AA16 is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

PACKAGE TYPE

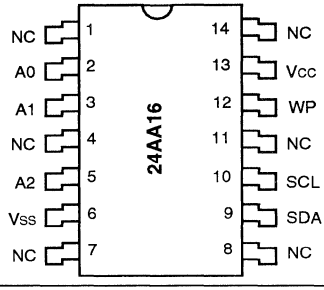
DIP



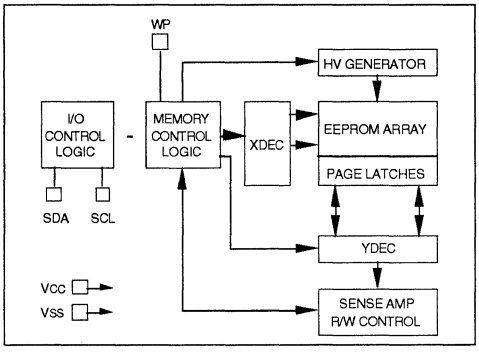
8-lead SOIC



14-lead SOIC



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V

All inputs and outputs w.r.t. Vss.....-0.6V to Vcc +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+1.8V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

		Vcc = 1.8V to +5.5V Commercial (C): Tamb = 0°C to +70°C				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:						
High level input voltage	VIH	.7 Vcc		—	V	
Low level input voltage	VIL	—		.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc		—	V	Note 1
Low level output voltage	VOL	—		.40	V	IOL = 3.0 mA, Vcc = 1.8V
Input leakage current	ILI	-10		10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10		10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs	CINT	—		10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc Write	—	—	3	mA	Vcc = 5.5V, SCL = 400 kHz
		—	.05	—	mA	Vcc = 1.8V, SCL = 100 kHz
	Icc Read	—	—	1	mA	Vcc = 5.5V, SCL = 400 kHz
		—	.05	—	mA	Vcc = 1.8V, SCL = 100 kHz
Standby current	Iccs	—	—	100	µA	Vcc = 5.5V, SDA=SCL=Vcc
		—	—	30	µA	Vcc = 3.0V, SDA=SCL=Vcc
		—	3	—	µA	Vcc = 1.8V, SDA=SCL=Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

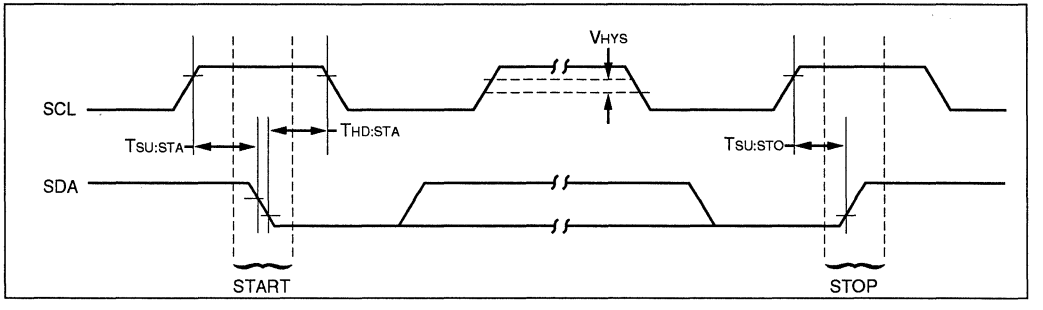


TABLE 1-3: AC CHARACTERISTICS

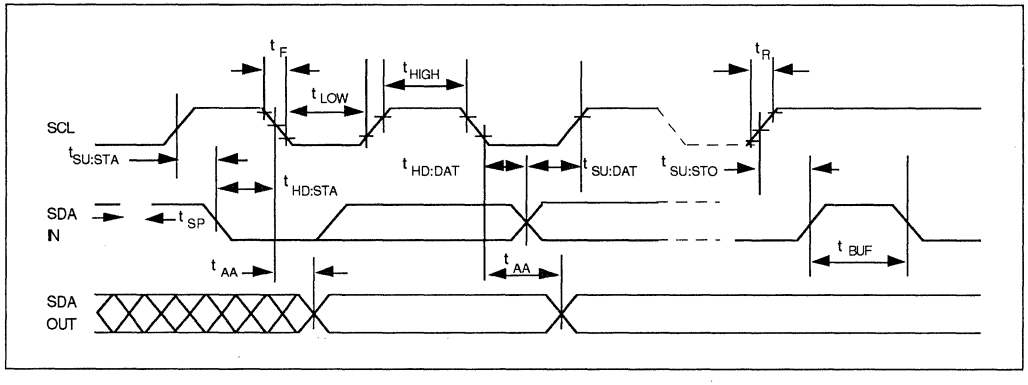
Parameter	Symbol	STANDARD MODE		Vcc = 4.5-5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from V_{IH} min to V_{IL} max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions

Note 2: Not 100% tested. C_B = total capacitance of one bus line in pF.

Note 3: The combined T_{SP} and V_{HYS} =specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a T_I specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA16 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA16 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

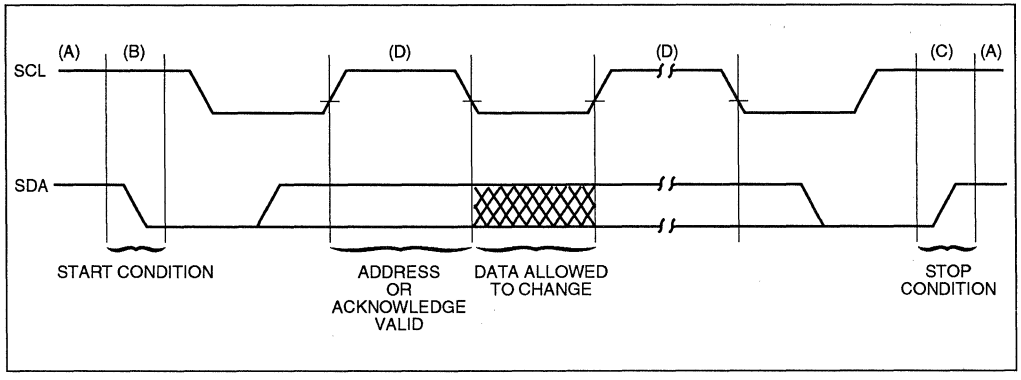
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA16 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

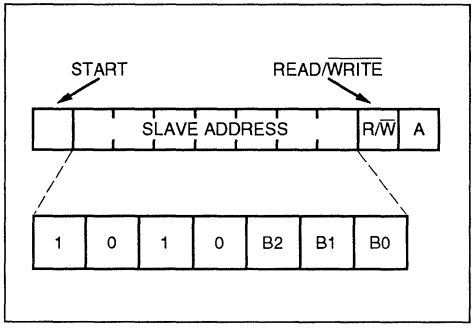
4.1 Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24AA16 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24AA16 per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA16 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA16 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

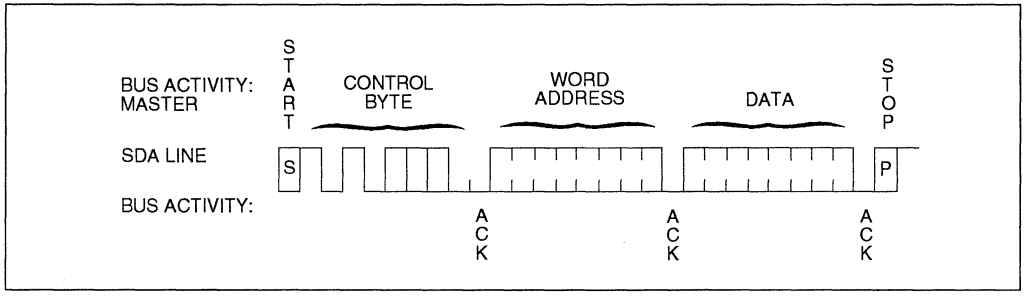
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA16. After receiving another acknowledge signal from the 24AA16 the master device will transmit the data word to be written into the addressed memory location. The 24AA16 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA16 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA16 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24AA16 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

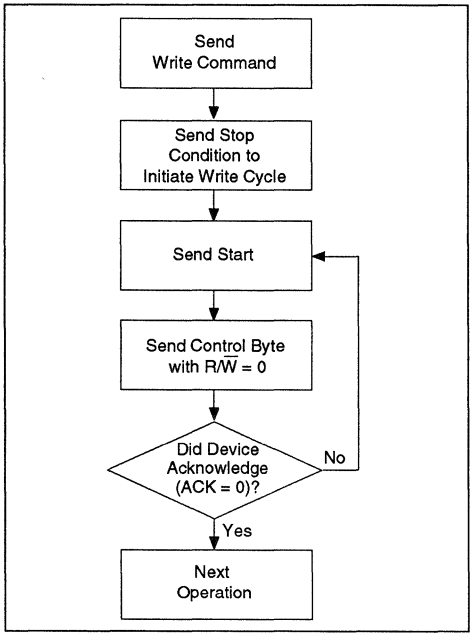
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24AA16 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24AA16 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA16 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA16 discontinues transmission (see Figure 8-2).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA16 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA16 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA16 discontinues transmission (see Figure 8-3).

FIGURE 8-1: PAGE WRITE

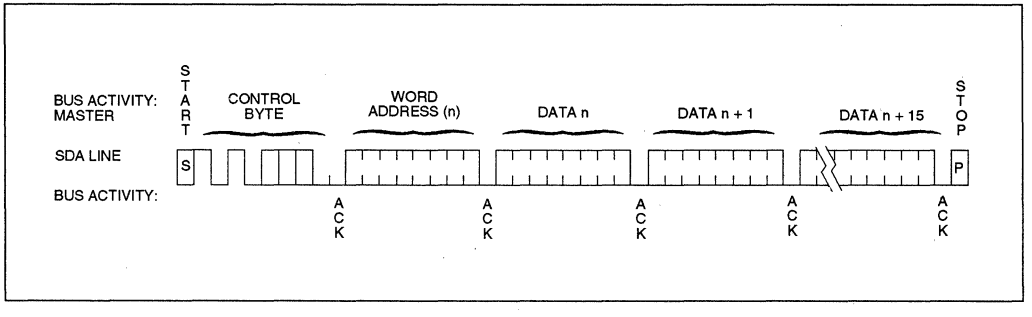


FIGURE 8-2: CURRENT ADDRESS READ

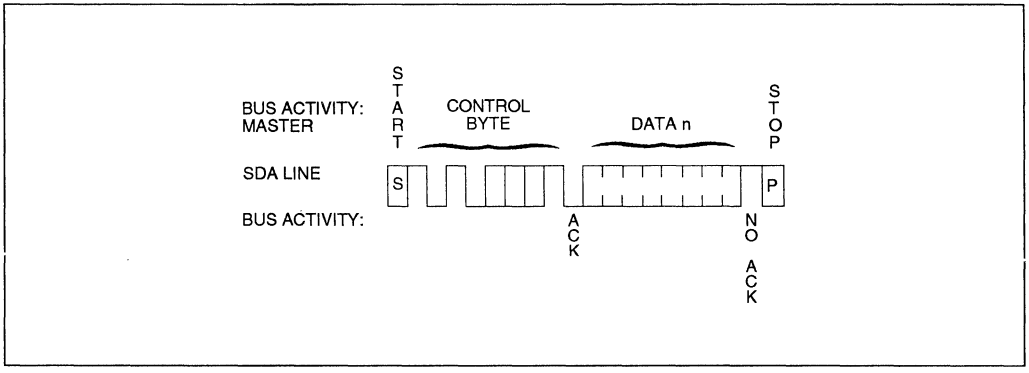
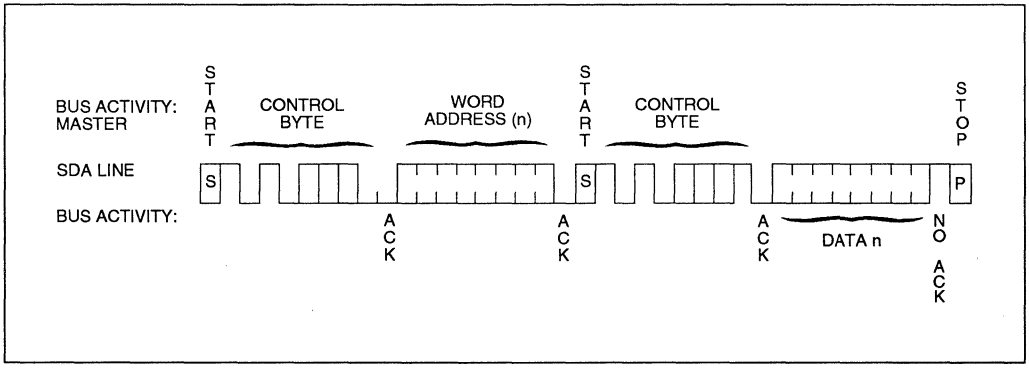


FIGURE 8-3: RANDOM READ



8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA16 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA16 to transmit the next sequentially addressed 8 bit word (see Figure 9-1).

To provide sequential reads the 24AA16 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24AA16 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz) from 24LC04B/08B.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

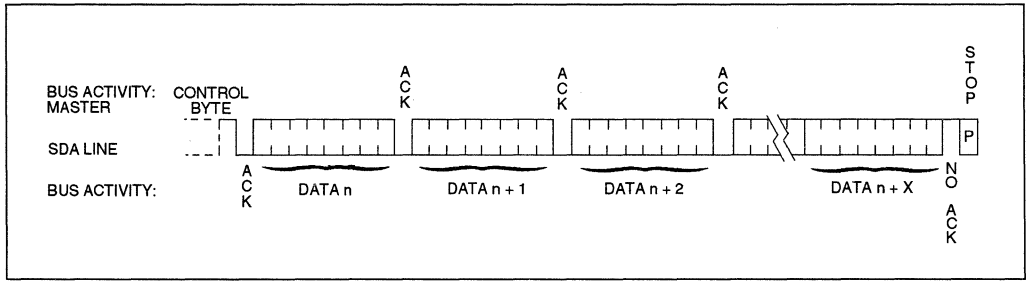
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA16 as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are not used by the 24AA16. They may be left floating or tied to either Vss or Vcc.

FIGURE 9-1: SEQUENTIAL READ



NOTES

24AA16 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24AA16 - /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	Blank =	0°C to +70°C
Device:	24AA16	1.8V, 16K CMOS Serial EEPROM
	24AA16T	1.8V, 16K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

24AA164

16K 1.8V Cascadable CMOS Serial EEPROM

FEATURES

- Single supply with operation down to 1.8V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **10,000,000 ERASE/WRITE cycles guaranteed**
- Data retention > 40 years
- 8 pin DIP, 8-lead SOIC packages
- Available for commercial temperature range
  - Commercial: 0°C to +70°C

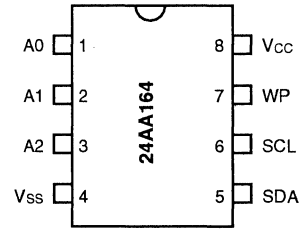
DESCRIPTION

The Microchip Technology Inc. 24AA164 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 1.8 volts (end-of-life voltage for most popular battery technologies) with standby and active currents of only 5 µA and 1 mA respectively. The 24AA164 also has a page-write capability for up to 16 bytes of data. The 24AA164 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

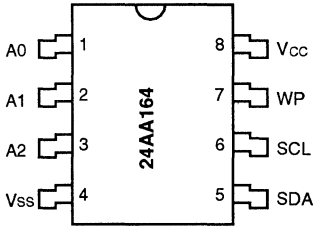
The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPE

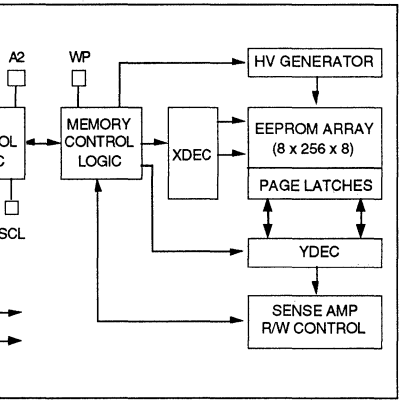
DIP



8-lead SOIC



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V

All inputs and outputs w.r.t. VSS.....-0.3V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 5.5V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

		VCC= 1.8V to +5.5V Commercial (C): Tamb = 0°C to +70°C			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	VCC = 3.0V, SDA=SCL=VCC VCC = 5.5V, SDA=SCL=VCC

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

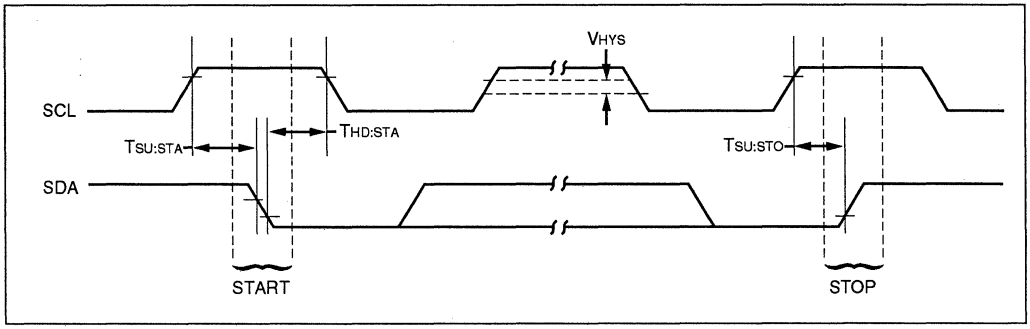
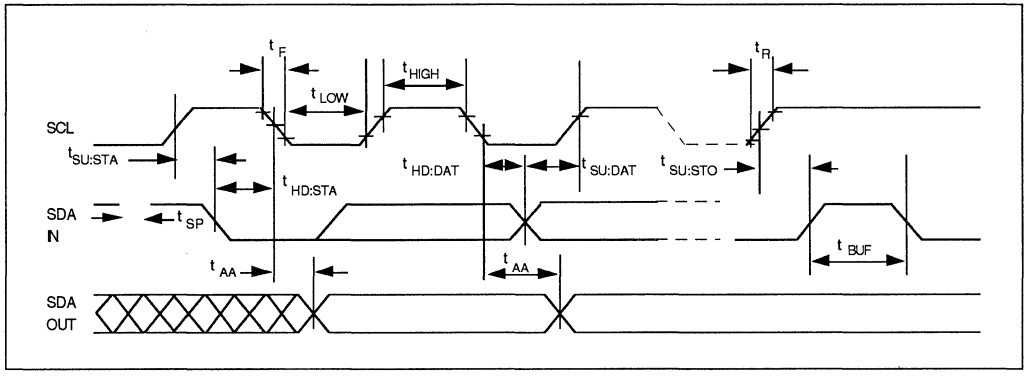


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		V_{CC} = 4.5-5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from V_{IH} min to V_{IL} max	TOF	—	250	—	250	ns	Note 2, $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 2: Not 100% tested. C_B = total capacitance of one bus line in pF.
Note 3: The combined TSP and VHYS =specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA164 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA164 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

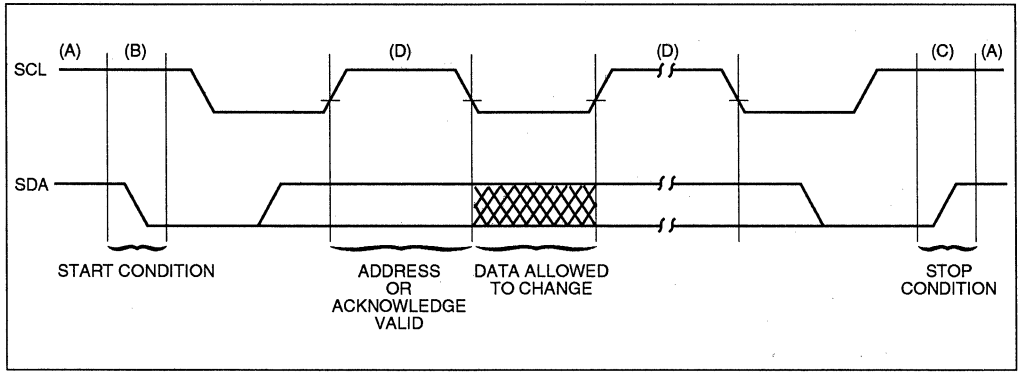
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA164 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA164) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation

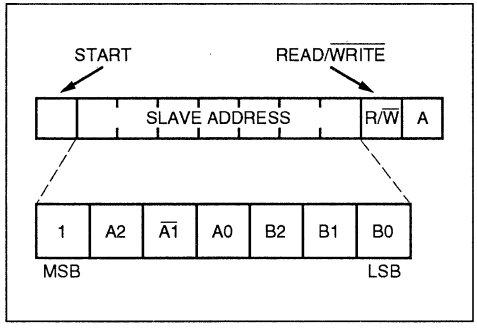
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA164 looks for the slave address for the device selected. Depending on the state of the R/$\overline{W}$ bit, the 24AA164 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1 A2 $\overline{A1}$ A0	Block Address	1
Write	1 A2 $\overline{A1}$ A0	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

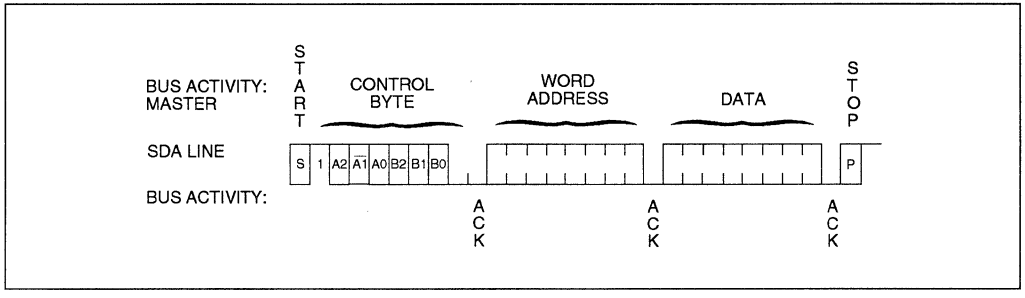
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA164. After receiving another acknowledge signal from the 24AA164 the master device will transmit the data word to be written into the addressed memory location. The 24AA164 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA164 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA164 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24AA164 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

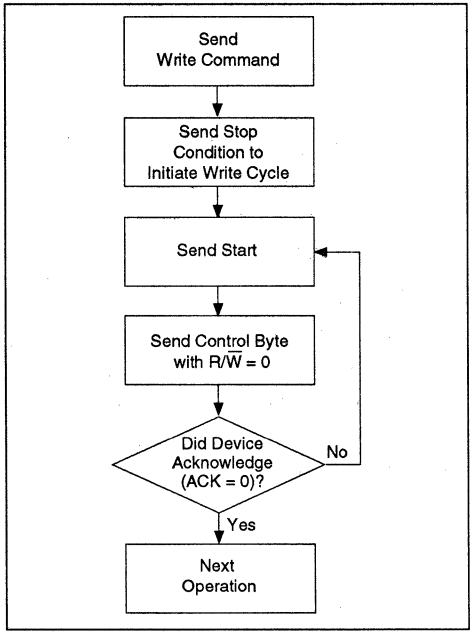
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24AA164 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

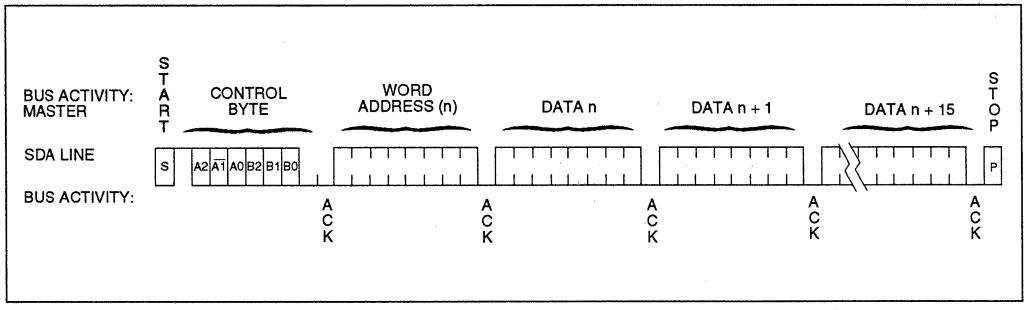
8.1 Current Address Read

The 24AA164 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA164 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA164 discontinues transmission (see Figure 9-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA164 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA164 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA164 discontinues transmission (see Figure 9-2).

FIGURE 8-1: PAGE WRITE



8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA164 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA164 to transmit the next sequentially addressed 8 bit word (see Figure 9-3).

To provide sequential reads the 24AA164 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

8.4 Noise Protection

The 24AA164 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA164 as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are used to configure the proper chip address in multiple-chip applications (more than one 24AA164 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note: The level on A1 is compared to the inverse of the slave address.

Up to eight 24AA164s may be connected to the same bus. These pins must be connected to either Vss or Vcc.

FIGURE 9-1: CURRENT ADDRESS READ

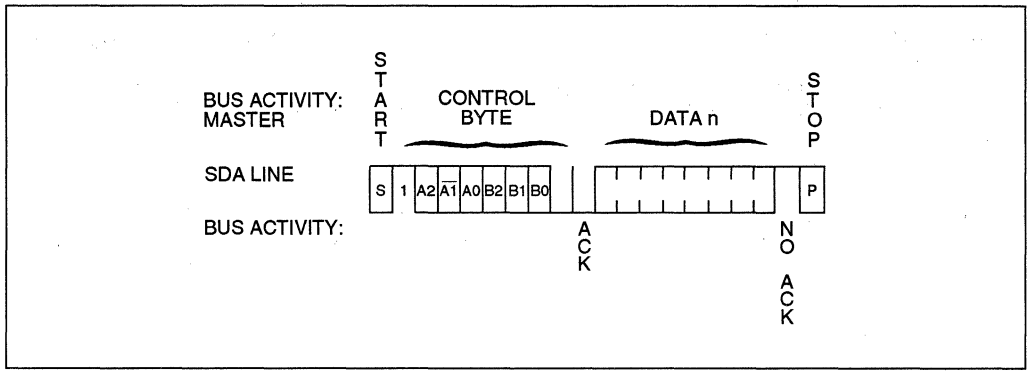


FIGURE 9-2: RANDOM READ

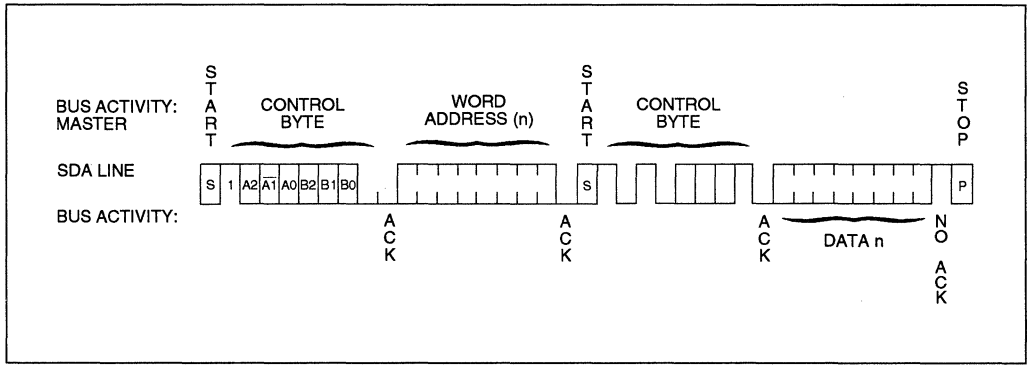
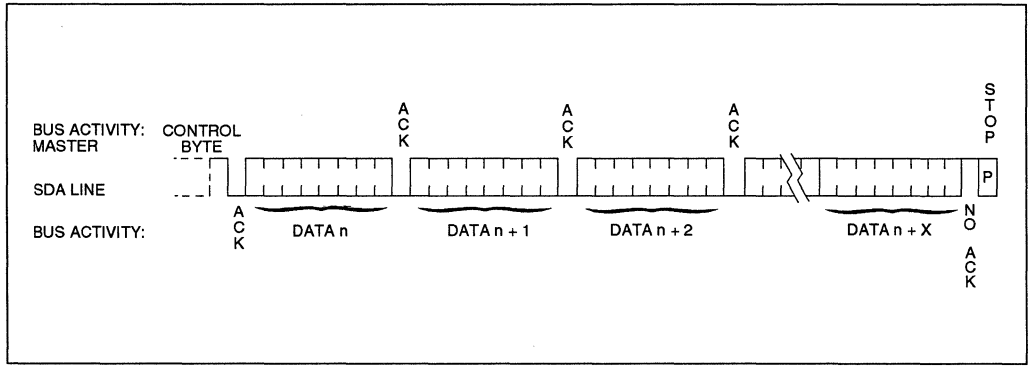


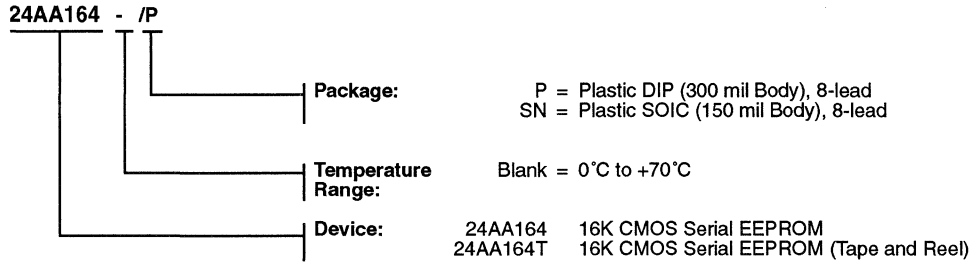
FIGURE 9-3: SEQUENTIAL READ



NOTES

24AA164 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24AA32

32K 1.8V CMOS Serial EEPROM

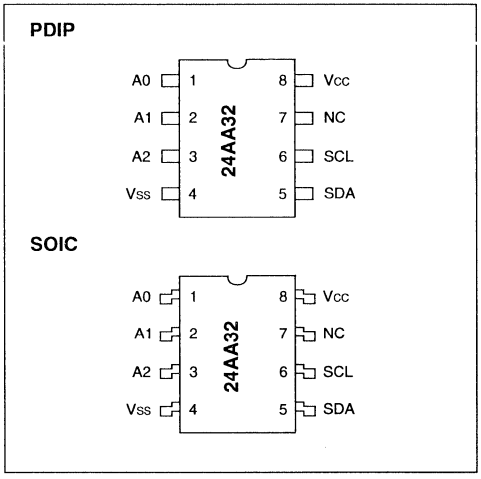
FEATURES

- Voltage operating range: 1.8V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
  - Including 100 kHz (1.8V) and 400 kHz (5V) modes
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - **10,000,000 ERASE/WRITE (E/W) cycles guaranteed for High Endurance Block**
  - **100,000 E/W cycles guaranteed for Standard Endurance Block**
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Factory programming (QTP) available
- Up to 8 devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C

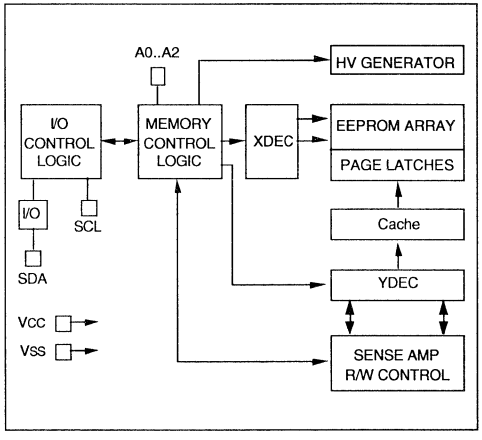
DESCRIPTION

The Microchip Technology Inc. 24AA32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (1.8V to 6.0V). This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24AA32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24AA32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to 8 - 24AA32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/low voltage, non-volatile code and data applications. The 24AA32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

PACKAGE TYPE



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V

All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTIONS

Name	Function
A0..A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+1.8V to 6.0V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			Vcc = +1.8V to 6.0V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V Note 1 Tamb = 25°C, Fclk = 1 MHz
Operating current	Icc Write Icc Read	— —	3 150	mA µA	Vcc = 6.0V, SCL = 400 kHz Vcc = 6.0V, SCL = 400 kHz
Standby current	ICCS	—	50 2	µA µA	Vcc = 5.0V, SCL = SDA = Vcc Note 1 Vcc = 1.8V, SCL = SDA = Vcc Note1

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

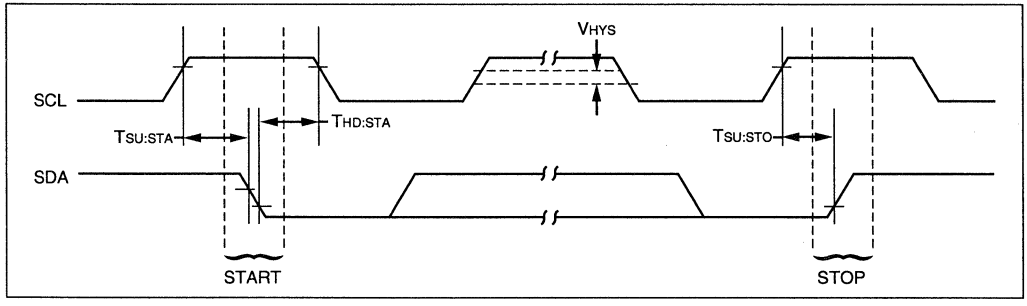


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	VCF = 1.8V-6.0V STD. MODE		V = 4.5 - 6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

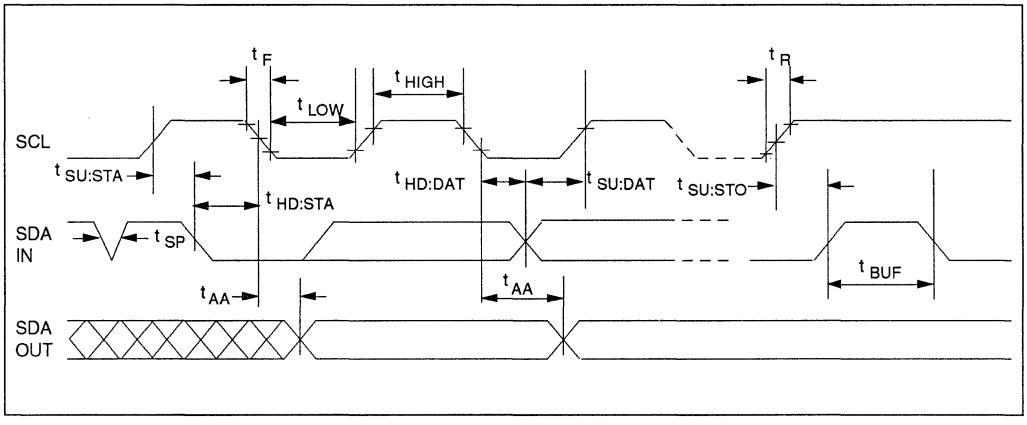
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (See Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

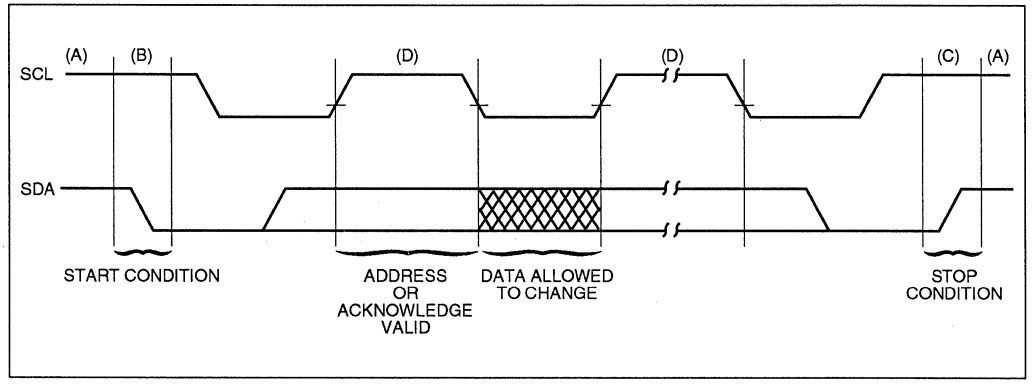
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA32) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation (Figure 4-1)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24AA32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 4-2). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

Following the start condition, the 24AA32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA32 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION

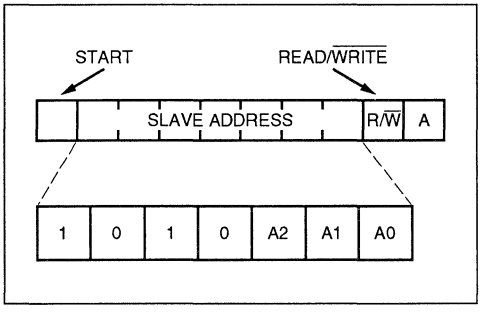
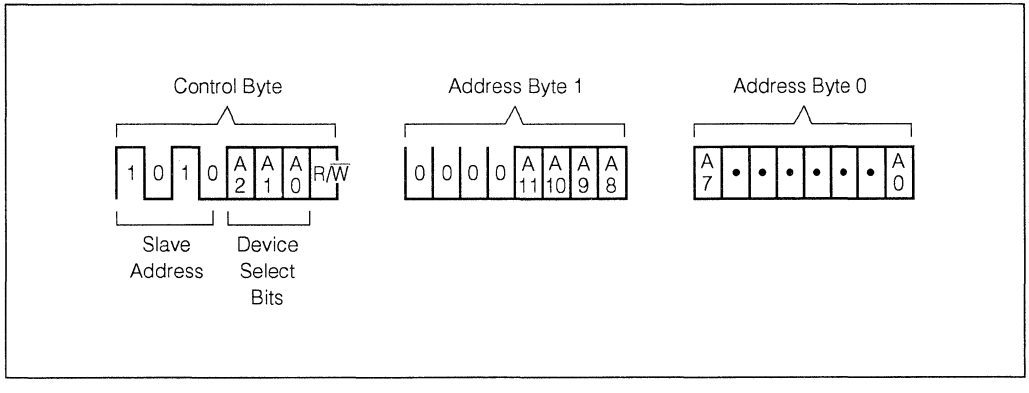


FIGURE 4-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



5.0 WRITE OPERATION

5.1 Split Endurance

The 24AA32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 10,000,000 E/W cycles guaranteed. The remainder of the array, 28K bits, is rated at 100,000 E/W cycles guaranteed. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

5.2 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24AA32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24AA32 the master device will transmit the data word to be written into the addressed memory location.

The 24AA32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA32 will not generate acknowledge signals (see Figure 5-1).

5.3 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24AA32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 5-2).

FIGURE 5-1: BYTE WRITE

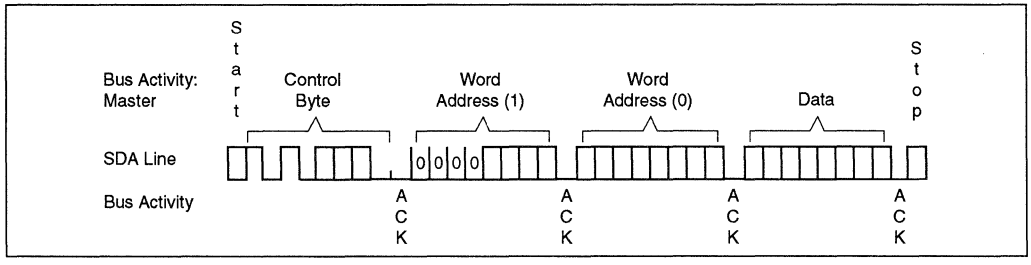
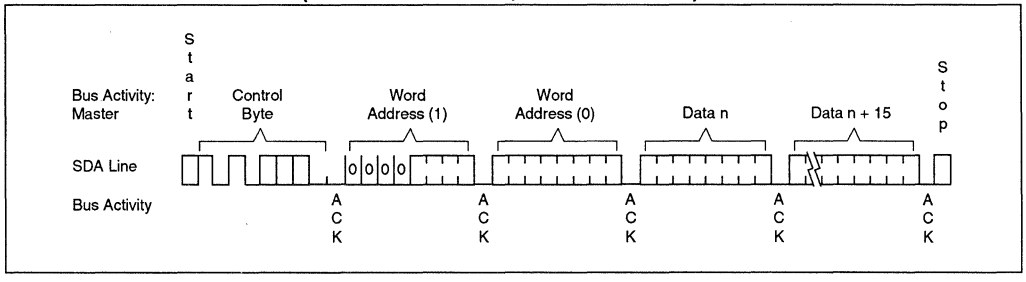


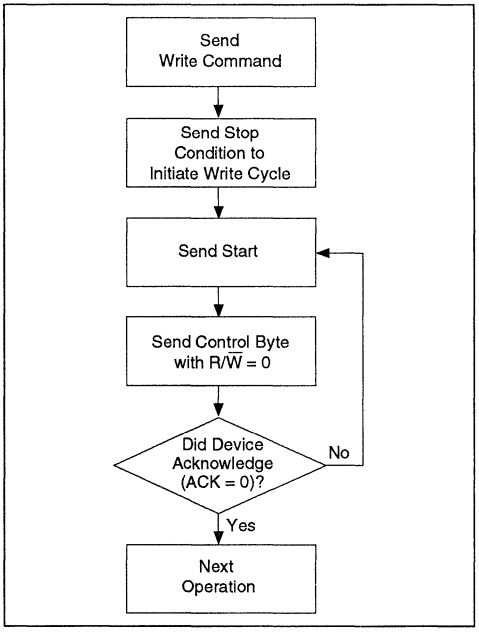
FIGURE 5-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 8-1)



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

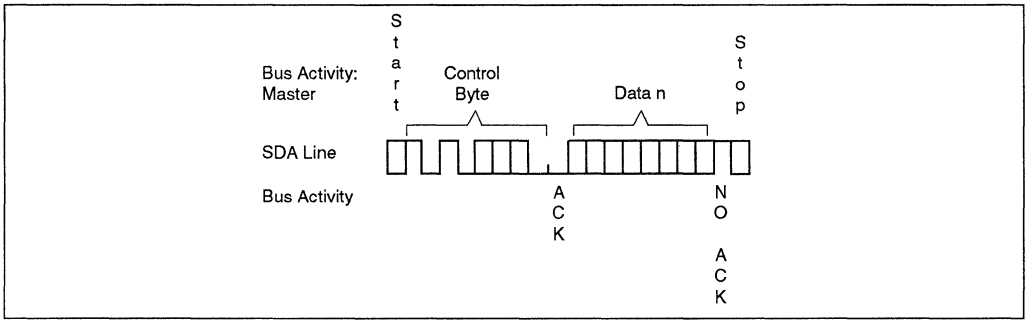
7.1 Current Address Read

The 24AA32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA32 discontinues transmission (see Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA32 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24AA32 to discontinue transmission (see Figure 7-2).

FIGURE 7-1: CURRENT ADDRESS READ



7.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24AA32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

7.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24AA32 to transmit the next sequentially addressed 8 bit word (see Figure 7-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24AA32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

7.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

FIGURE 7-2: RANDOM READ

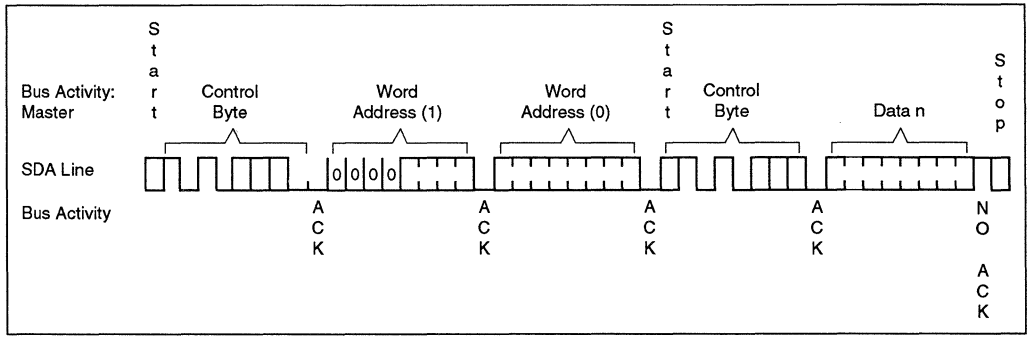
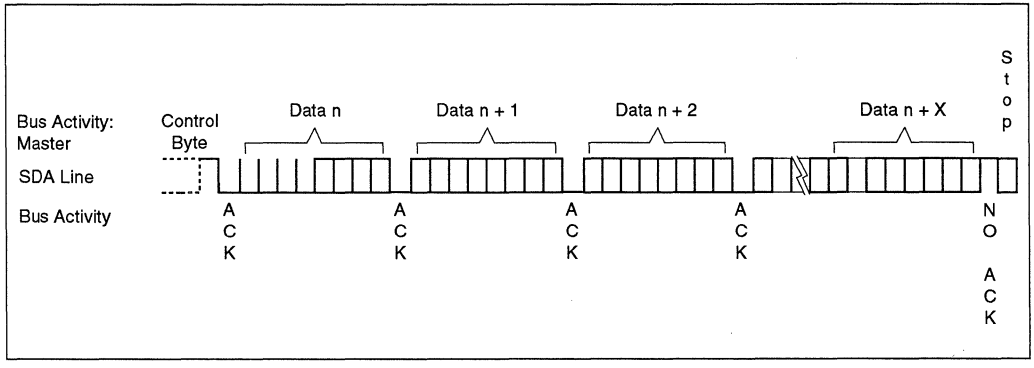


FIGURE 7-3: SEQUENTIAL READ



7.6 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.7 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 5-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.8 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 8-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.9 Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24AA32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figure 4-2).

8.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 8-1: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

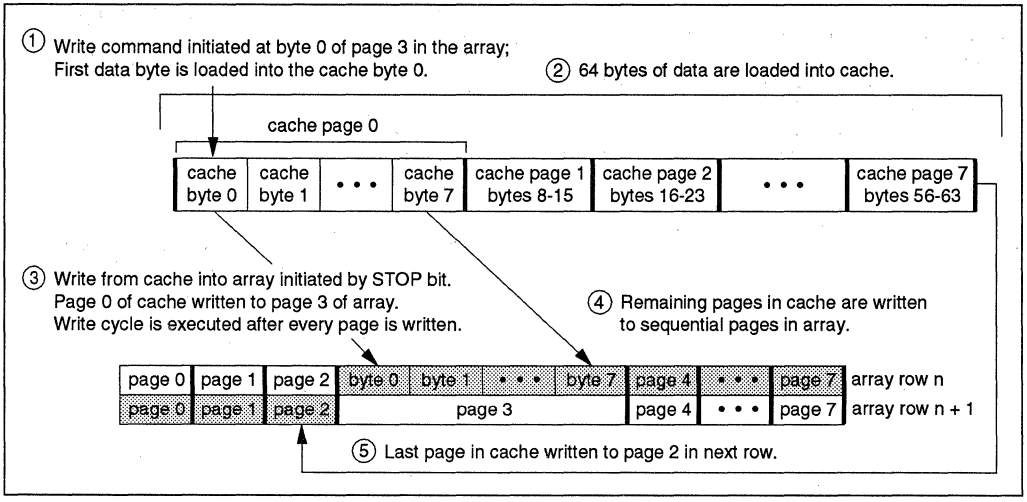
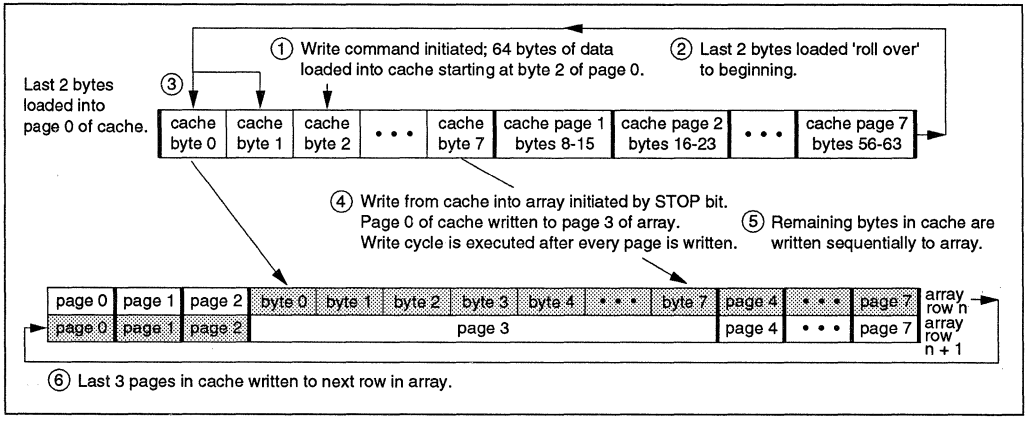


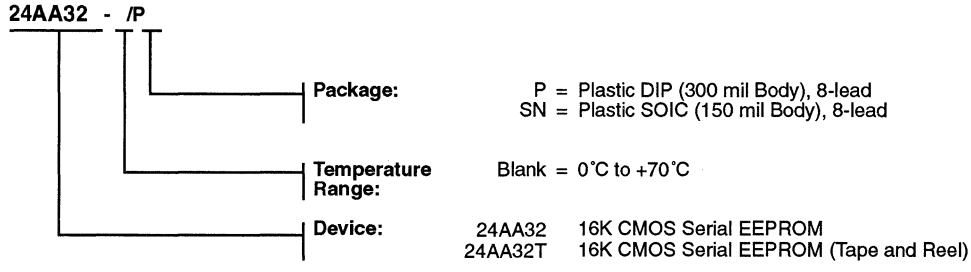
FIGURE 8-2: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



NOTES

24AA32 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24LC01B/02B

1K/2K 2.5V CMOS Serial EEPROMs

FEATURES

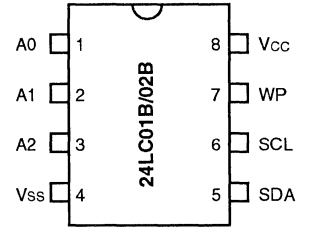
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- Two wire serial interface bus, I²C™ compatible
- 100kHz (2.5V) and 400kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 3,000V
- **10,000,000 ERASE/WRITE cycles guaranteed on 24LC01B**
- **1,000,000 E/W cycles guaranteed on 24LC02B***
- Data retention > 40 years
- 8 pin DIP or SOIC package
- Available for extended temperature ranges
  - Commercial 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

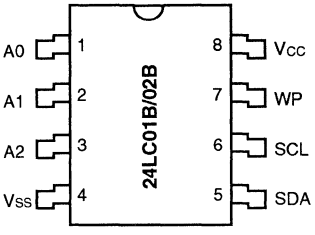
The Microchip Technology Inc. 24LC01B and 24LC02B are 1K bit and 2K bit Electrically Erasable PROMs. The devices are organized as a single block of 128 x 8 bit or 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with a standby and active currents of only 5 µA and 1 mA respectively. The 24LC01B and 24LC02B also have page-write capability for up to 8 bytes of data. The 24LC01B and 24LC02B are available in the standard 8-pin DIP and an 8-pin surface mount SOIC package.

PACKAGE TYPE

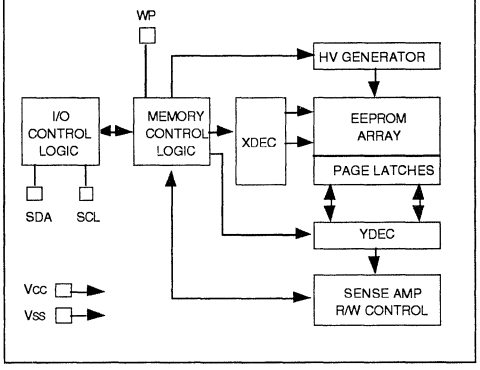
DIP



SOIC



BLOCK DIAGRAM



*Future: 10,000,000 E/W cycles guaranteed.

I²C is a trademark of Phillips Corporation

1.0 ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC.....7.0V

All inputs and outputs w.r.t. VSS .... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

	VCC = +2.5V to +5.5V		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
WP, SCL and SDA pins: High level input voltage	VIH	.7 VCC		V	
Low level input voltage	VIL		.3 VCC	V	
Hysteresis of Schmidt trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL		.40	V	IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to 5.5V
Output leakage current	ILO	-10	10	µA	VOUT = .1V to 5.5V
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	VCC = 5.5V, SCL = 400 kHz
	ICC Read	—	1	mA	
Standby current	ICCS	—	30	µA	VCC = 3.0V, SDA = SCL = VCC
			100	µA	VCC = 5.5V, SDA = SCL = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

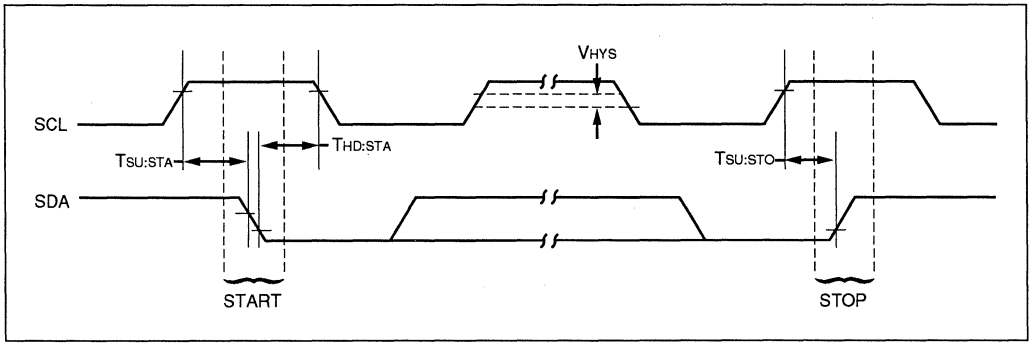
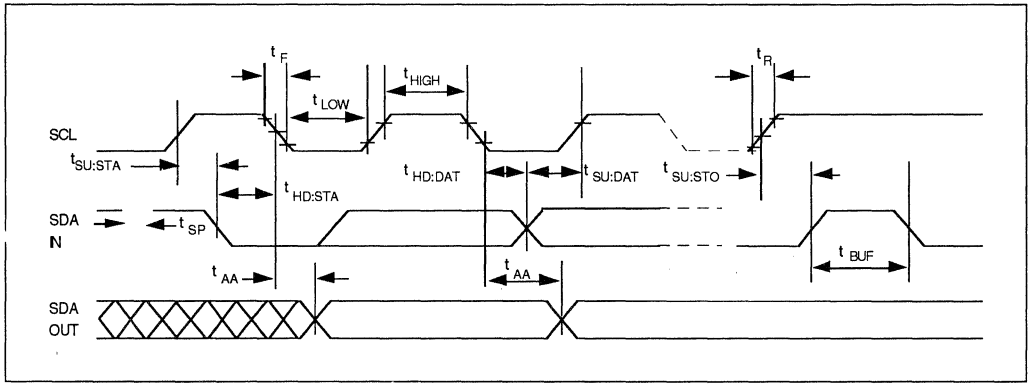


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	Note 1
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC01B/02B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC01B/02B works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

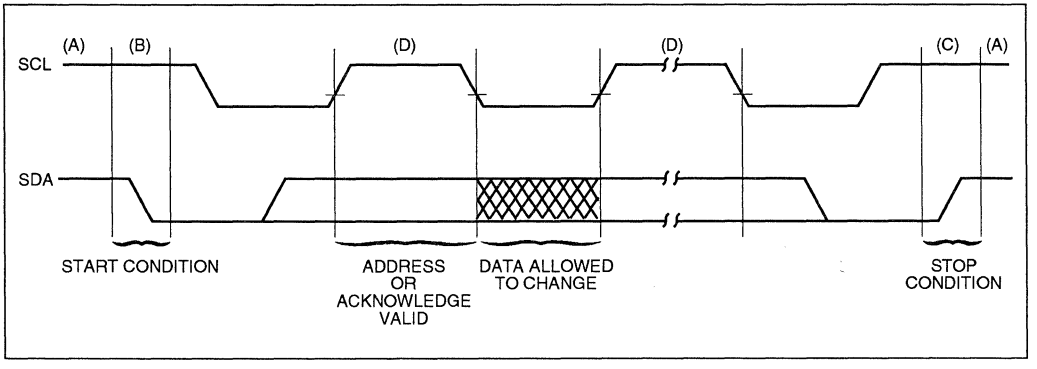
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC01B/02B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Slave Address

The 24LC01B/02B are software-compatible with older devices such as 24C01A, 24C02A, 24LC01, and 24LC02. A single 24LC02B can be used in place of two 24LC01's, for example, without any modifications to software. The "chip select" portion of the control byte becomes a don't care.

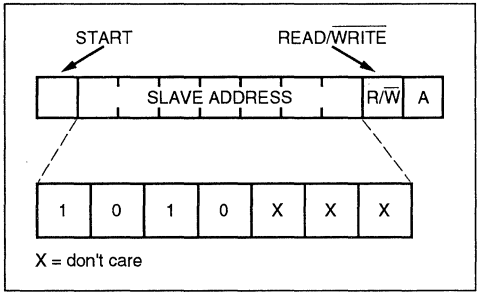
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24LC01B/02B, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC01B/02B (see Figure 4-1).

The 24LC01B/02B monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

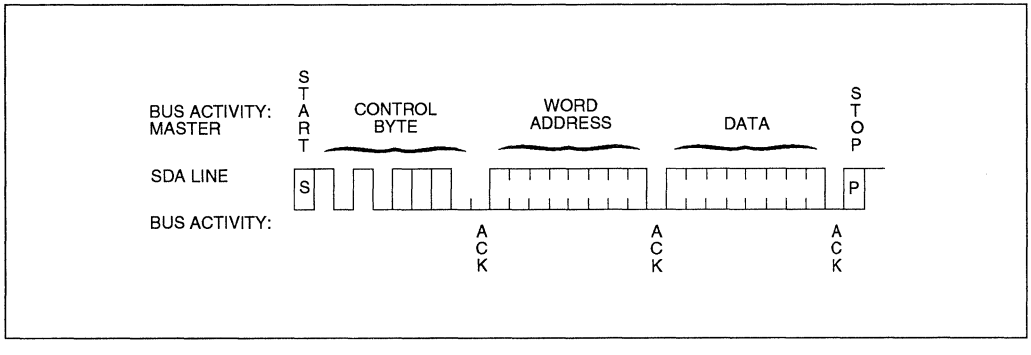
5.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC01B/02B. After receiving another acknowledge signal from the 24LC01B/02B the master device will transmit the data word to be written into the addressed memory location. The 24LC01B/02B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC01B/02B will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC01B/02B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC01B/02B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

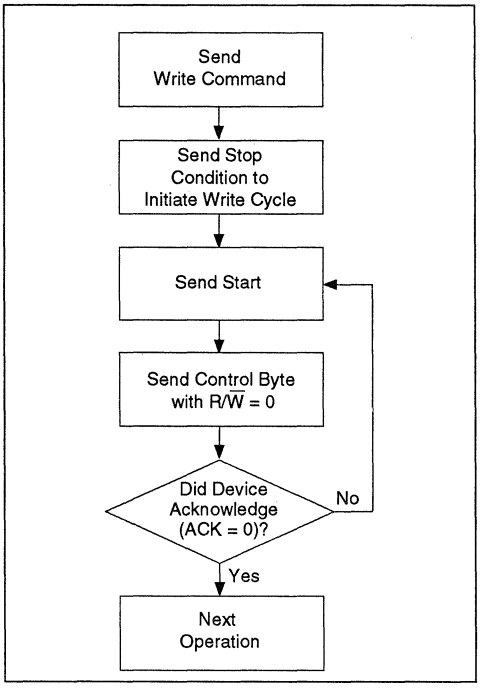
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24LC01B/02B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24LC01B/02B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC01B/02B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B/02B discontinues transmission (see Figure 8-2).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC01B/02B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC01B/02B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B/02B discontinues transmission (see Figure 8-3).

FIGURE 8-1: PAGE WRITE

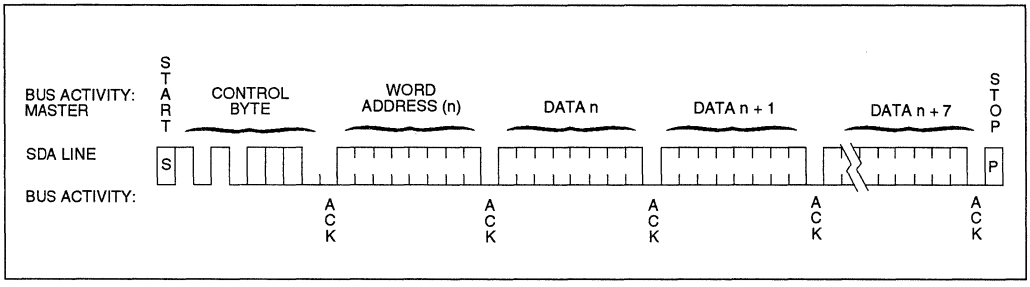


FIGURE 8-2: CURRENT ADDRESS READ

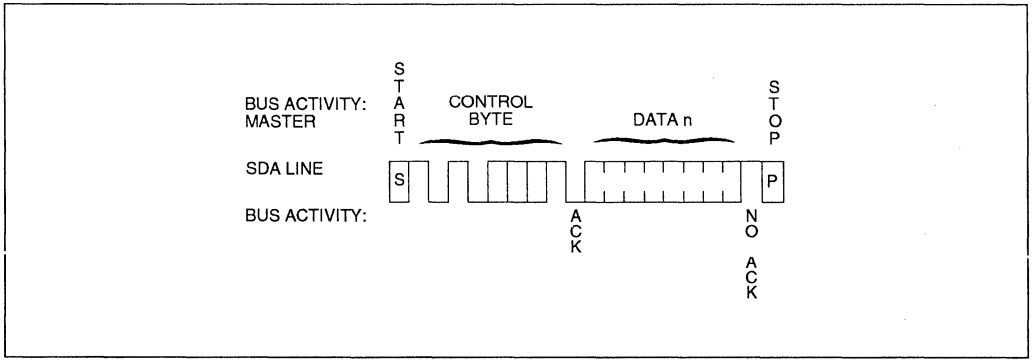
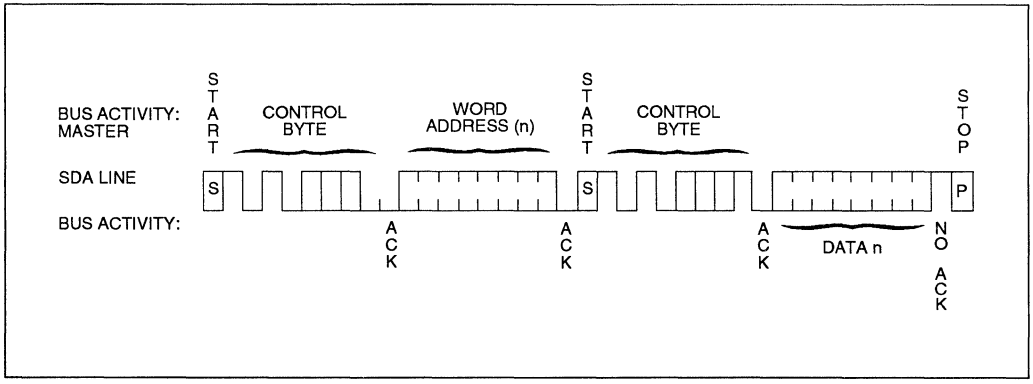


FIGURE 8-3: RANDOM READ



3

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC01B/02B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC01B/02B to transmit the next sequentially addressed 8 bit word (see Figure 9-1).

To provide sequential reads the 24LC01B/02B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24LC01B/02B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

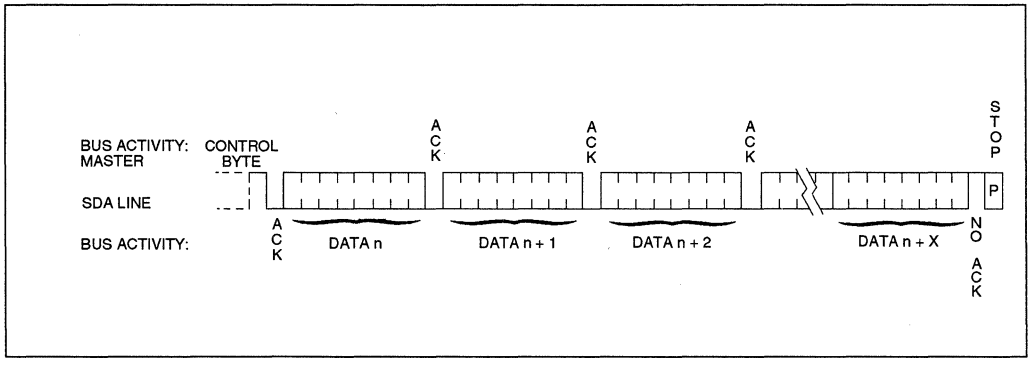
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC01B/02B as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are not used by the 24LC01B/02B. They may be left floating or tied to either Vss or Vcc.

FIGURE 9-1: SEQUENTIAL READ



NOTES

24LC01B/02B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC01B - /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body)
	SM =	Plastic SOIC (207 mil Body)
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Device:	24LC01B	1K CMOS Serial EEPROM
	24LC01BT	1K CMOS Serial EEPROM (Tape and Reel)
	24LC02B	2K CMOS Serial EEPROM
	24LC02BT	2K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24LC04B/08B

4K/8K 2.5V CMOS Serial EEPROMs

FEATURES

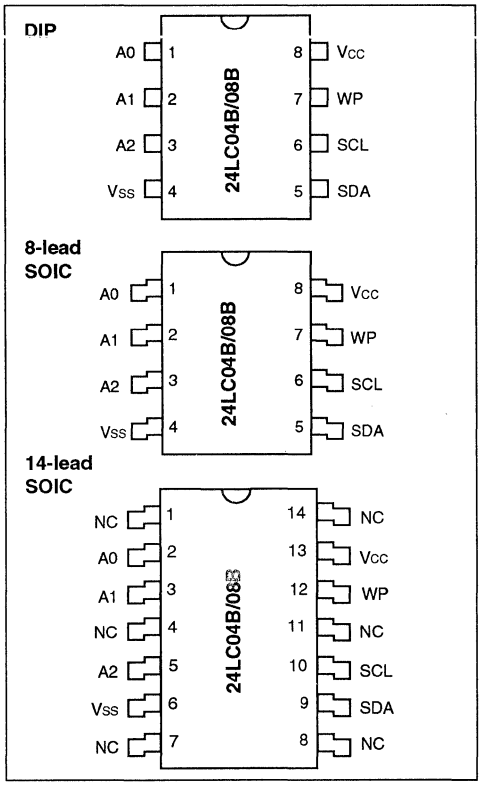
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as two or four blocks of 256 bytes (2 x 256 x 8) and (4 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **1,000,000 ERASE/WRITE cycles guaranteed***
- Data retention > 40 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

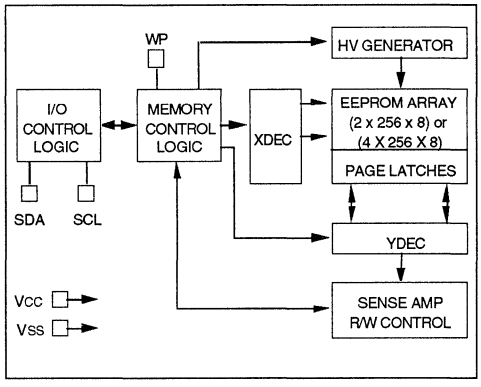
The Microchip Technology Inc. 24LC04B/08B is a 4K- or 8K-bit Electrically Erasable PROM. The device is organized as two or four blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC04B/08B also has a page-write capability for up to 16 bytes of data. The 24LC04B/08B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

*Future: 10,000,000 E/W cycles guaranteed

PACKAGE TYPE



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS ... -0.3V to VCC + 1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

					VCC = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C
Parameter	**Symbol**	**Min**	**Max**	**Units**	
WP, SCL and SDA pins: High level input voltage Low level input voltage Hysteresis of Schmitt trigger inputs Low level output voltage	 VIH VIL VHYS VOL	 .7 VCC — .05 VCC —	 — .3 VCC — .40	 V V V V	 Note 1 IOL = 3.0mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE ICC READ	— —	3 1	mA mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	VCC = 3.0V, SDA = SCL = VCC VCC = 5.5V, SDA = SCL = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

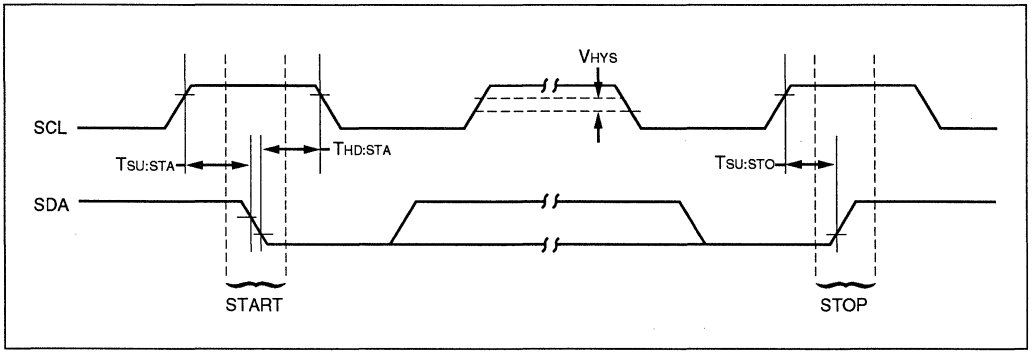


TABLE 1-3: AC CHARACTERISTICS

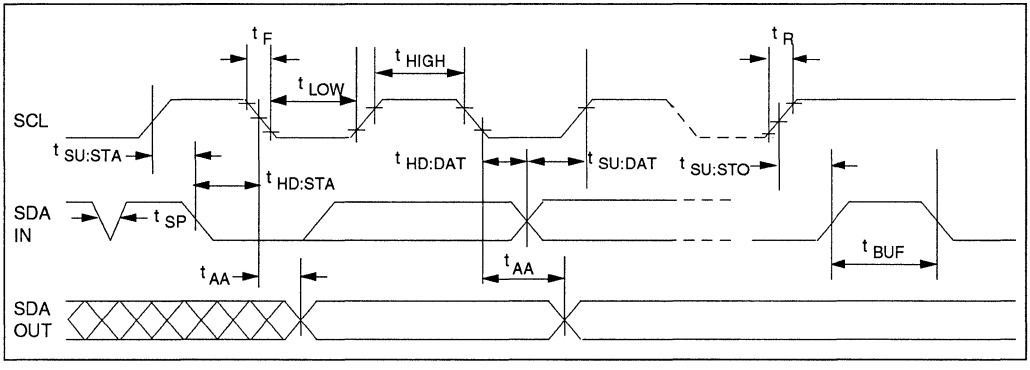
Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC04B/08B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC04B/08B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

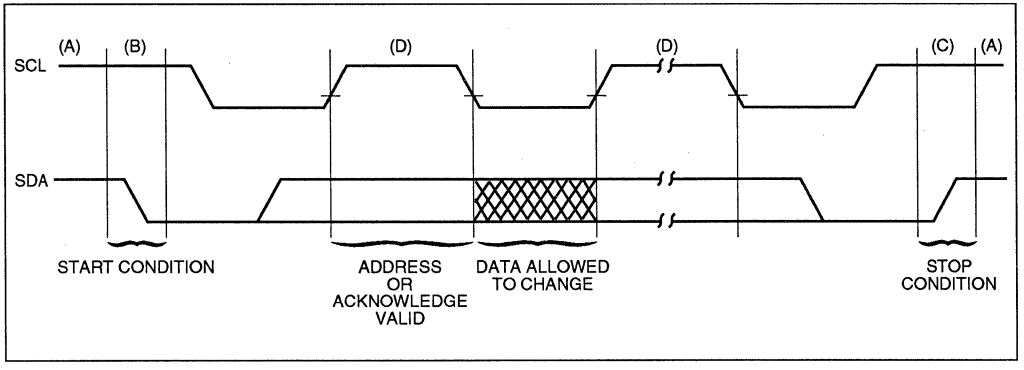
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC04B/08B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

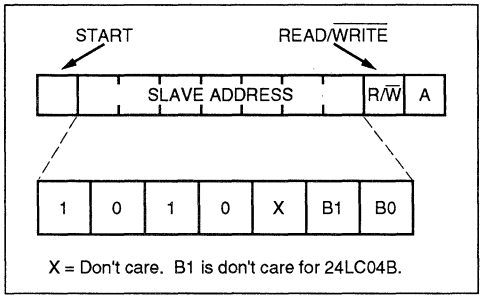
4.1 Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC04B/08B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). B2 is a don't care for both the 24LC04B and 24LC08B; B1 is a don't care for the 24LC04B. They are used by the master device to select which of the two or four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC04B/08B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24LC04B/08B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

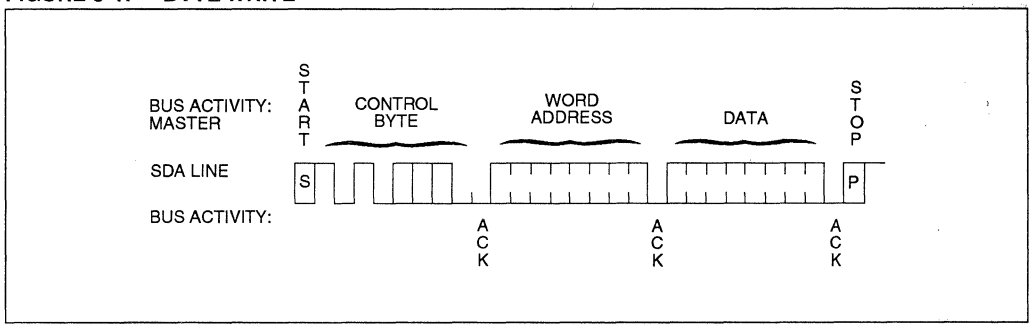
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC04B/08B. After receiving another acknowledge signal from the 24LC04B/08B the master device will transmit the data word to be written into the addressed memory location. The 24LC04B/08B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC04B/08B will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC04B/08B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24LC04B/08B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

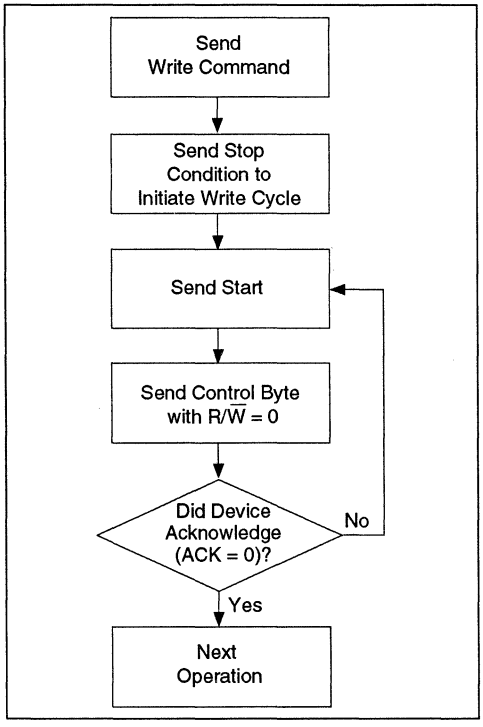
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24LC04B/08B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24LC04B/08B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC04B/08B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04B/08B discontinues transmission (see Figure 8-2).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC04B/08B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC04B/08B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04B/08B discontinues transmission (see Figure 8-3).

FIGURE 8-1: PAGE WRITE

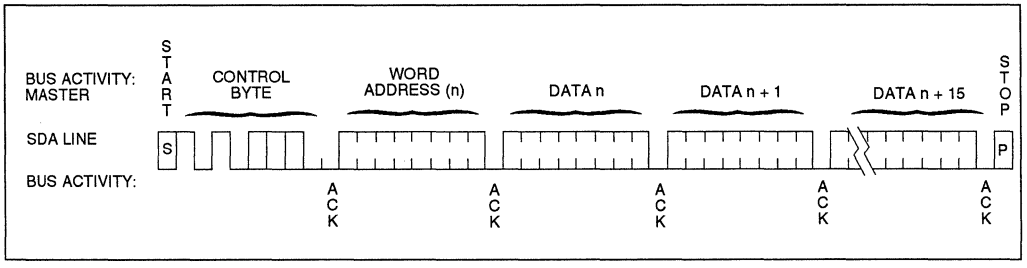


FIGURE 8-2: CURRENT ADDRESS READ

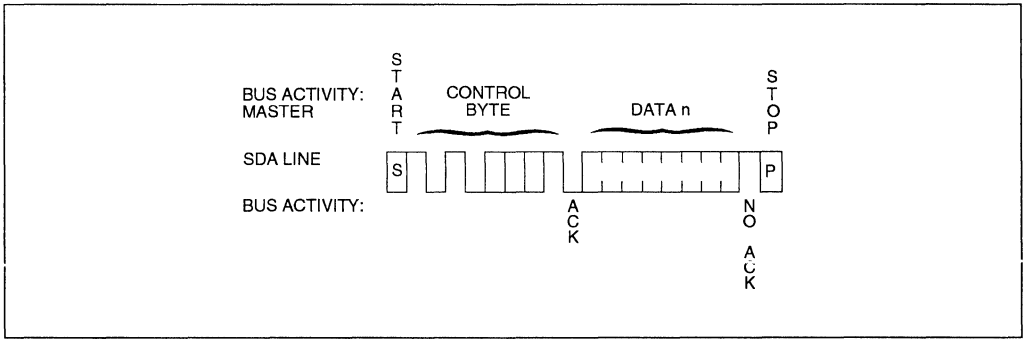
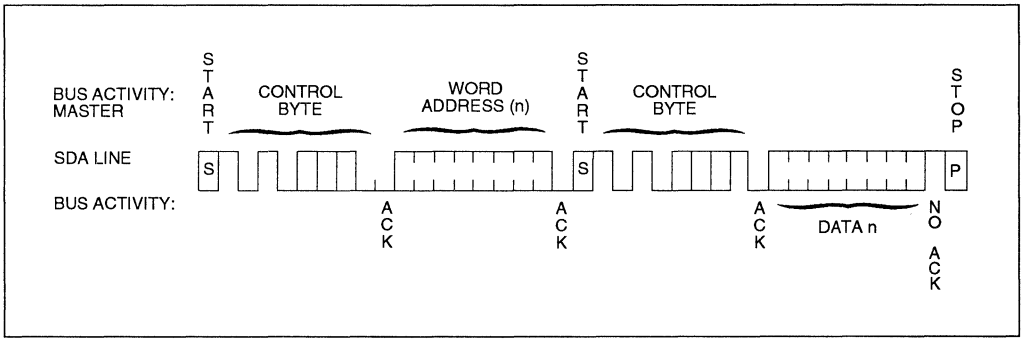


FIGURE 8-3: RANDOM READ



3

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC04B/08B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC04B/08B to transmit the next sequentially addressed 8 bit word (see Figure 9-1).

To provide sequential reads the 24LC04B/08B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24LC04B/08B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

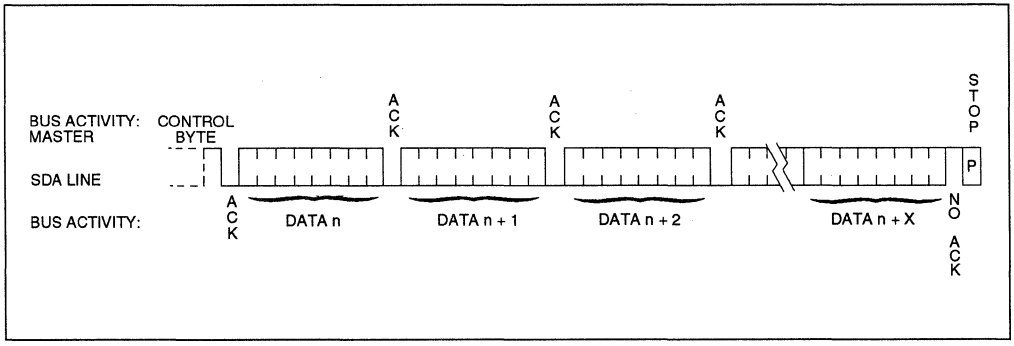
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC04B/08B as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are not used by the 24LC04B/08B. They may be left floating or tied to either Vss or Vcc.

FIGURE 9-1: SEQUENTIAL READ



NOTES

24LC04B/08B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC04B - /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SM =	Plastic SOIC (207 mil Body), 8-lead
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Device:	24LC04B	4K CMOS Serial EEPROM
	24LC04BT	4K CMOS Serial EEPROM (Tape and Reel)
	24LC04B	8K CMOS Serial EEPROM
	24LC04BT	8K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24LC16B

16K 2.5V CMOS Serial EEPROM

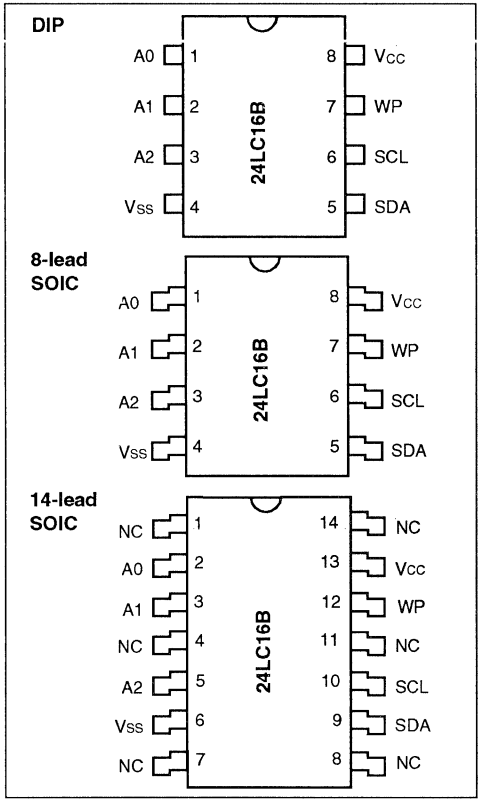
FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **10,000,000 ERASE/WRITE cycles guaranteed**
- Data retention > 40 years
- 8 pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

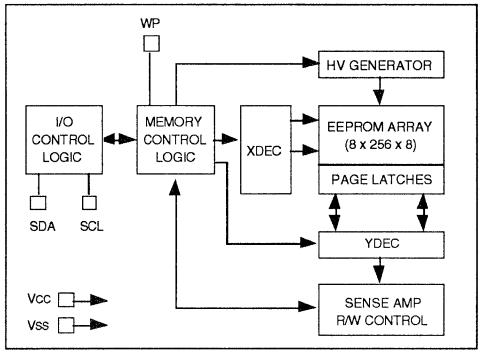
DESCRIPTION

The Microchip Technology Inc. 24LC16B is a 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC16B also has a page-write capability for up to 16 bytes of data. The 24LC16B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

PACKAGE TYPE



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .... -0.3V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

		Vcc = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins: High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, FCLK = 1MHz
Operating current	ICC write ICC read	— —	3 1	mA mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	Vcc = 3.0V, SDA = SCL = Vcc Vcc = 5.5V, SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

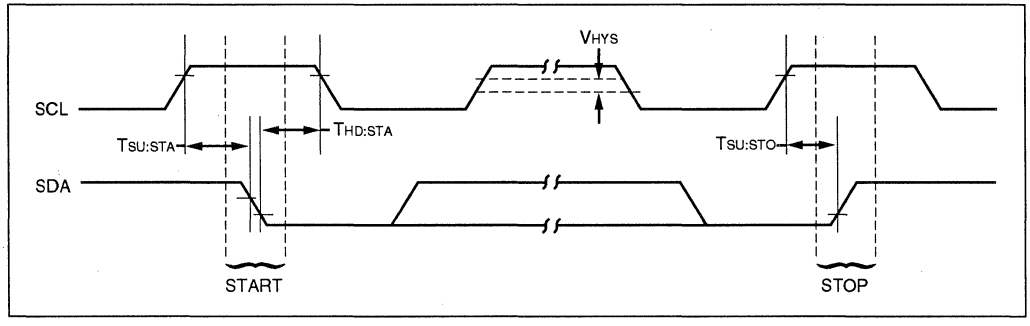


TABLE 1-3: AC CHARACTERISTICS

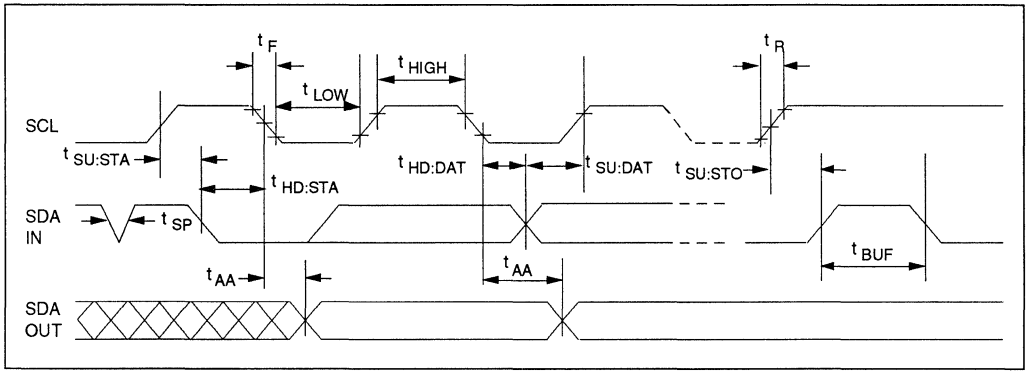
Parameter	Symbol	STANDARD MODE		Vcc = 4.5V - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC16B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC16B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

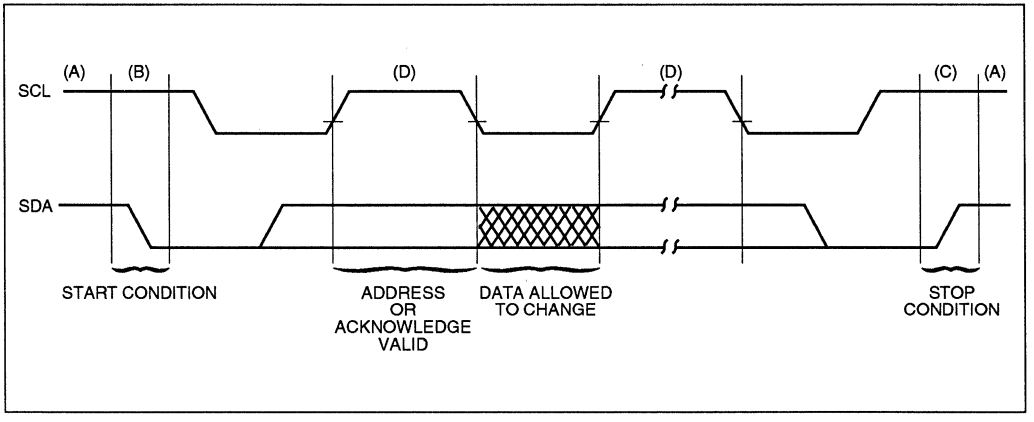
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC16B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC16B) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

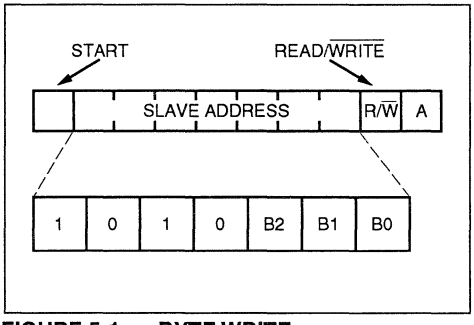
4.1 Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC16B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24LC16B per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC16B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC16B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

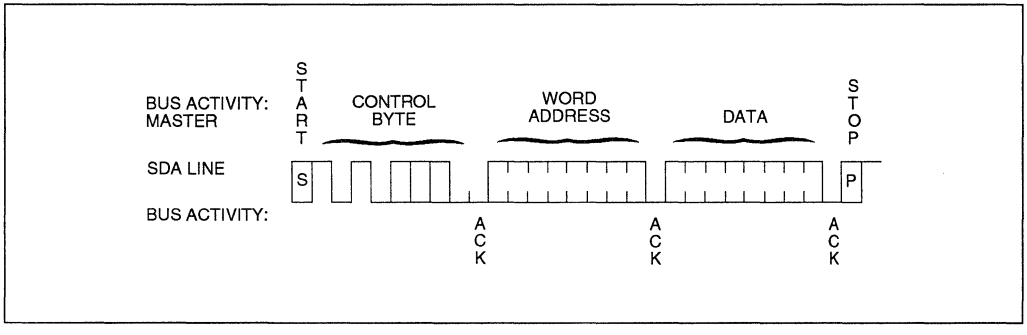
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC16B. After receiving another acknowledge signal from the 24LC16B the master device will transmit the data word to be written into the addressed memory location. The 24LC16B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC16B will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC16B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24LC16B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

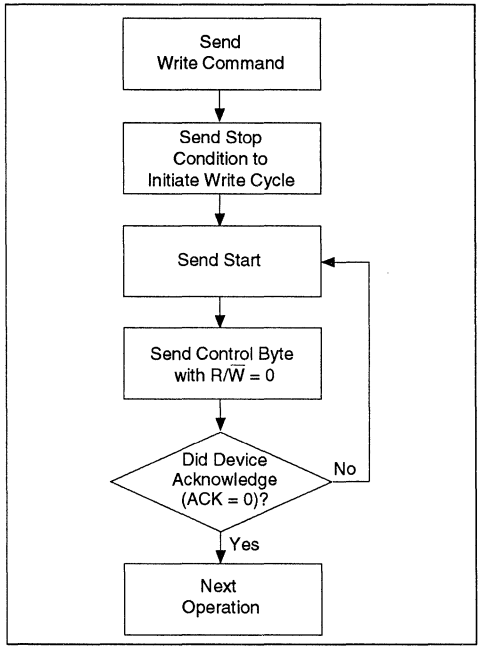
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24LC16B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24LC16B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC16B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16B discontinues transmission (see Figure 8-2).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC16B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC16B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC16B discontinues transmission (see Figure 8-3).

FIGURE 8-1: PAGE WRITE

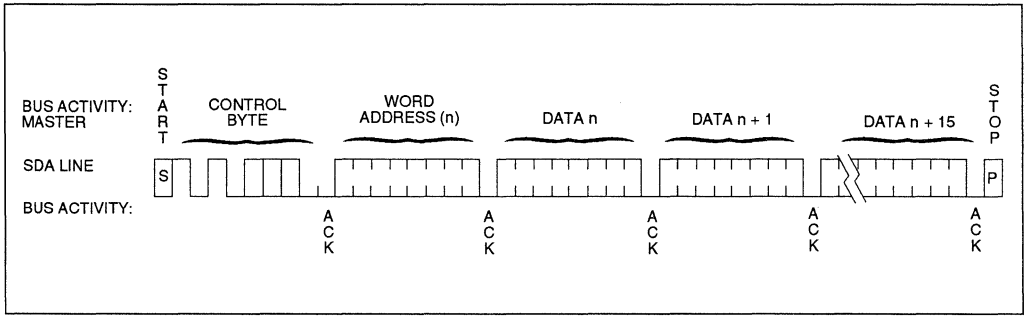


FIGURE 8-2: CURRENT ADDRESS READ

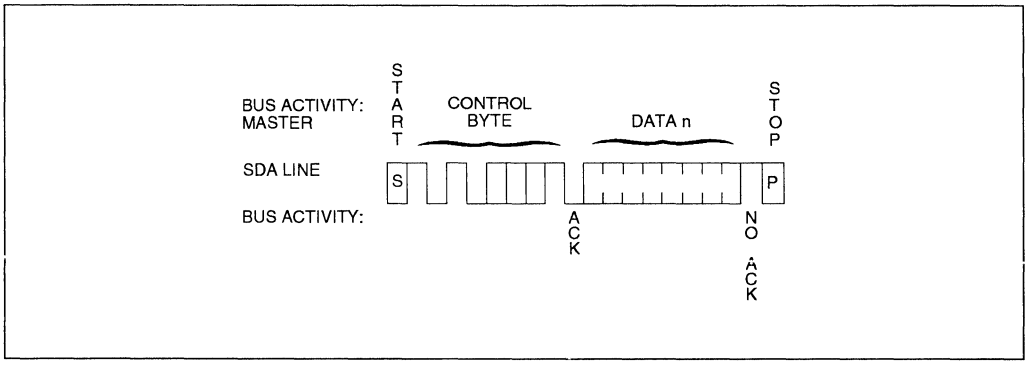
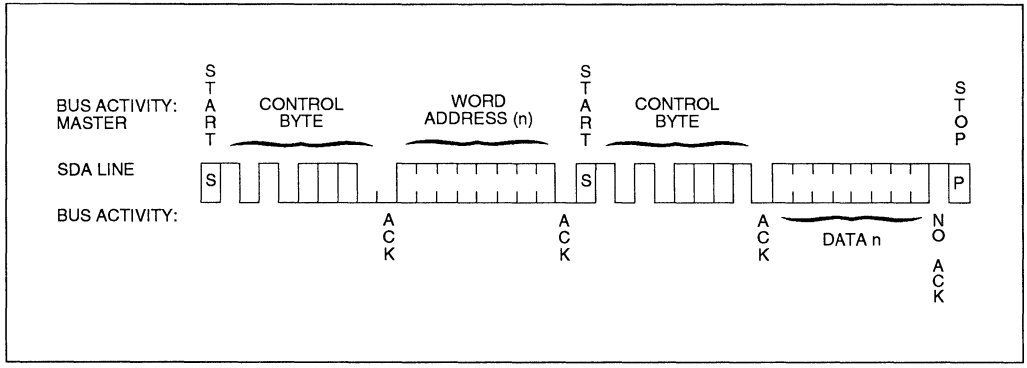


FIGURE 8-3: RANDOM READ



8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC16B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC16B to transmit the next sequentially addressed 8 bit word (see Figure 9-1).

To provide sequential reads the 24LC16B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24LC16B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss normal memory operation is enabled (read/write the entire memory 000-7FF).

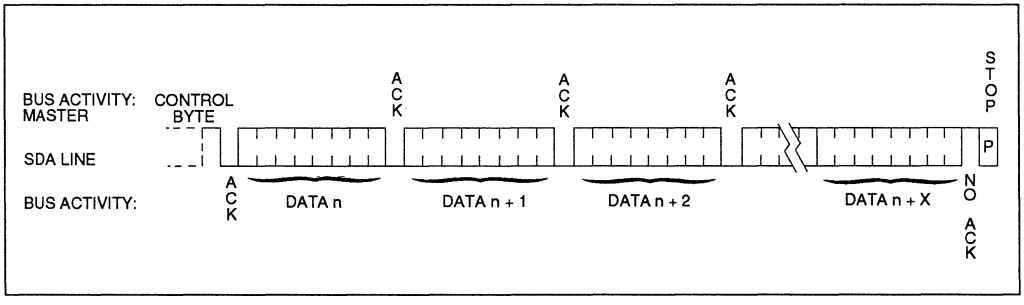
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC16B as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are not used by the 24LC16B. They may be left floating or tied to either Vss or Vcc.

FIGURE 9-1: SEQUENTIAL READ



NOTES

24LC16B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC16B - /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SM =	Plastic SOIC (207 mil Body), 8-lead
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Device:	24LC16B	16K CMOS Serial EEPROM
	24LC16BT	16K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24LC164

16K 2.5V Cascadable CMOS Serial EEPROM

FEATURES

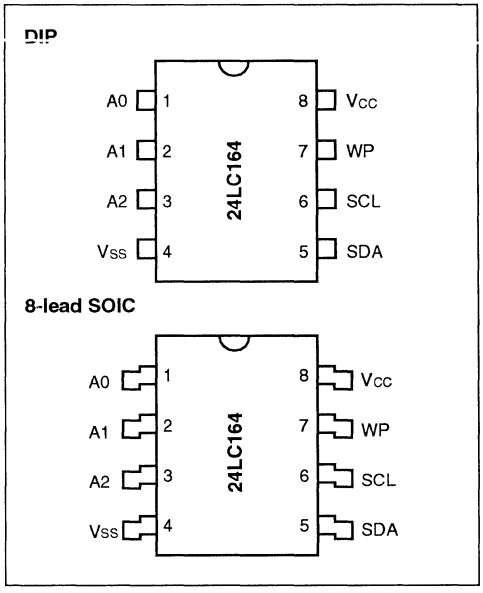
- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **10,000,000 ERASE/WRITE cycles guaranteed**
- Data retention > 40 years
- 8 pin DIP, 8-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

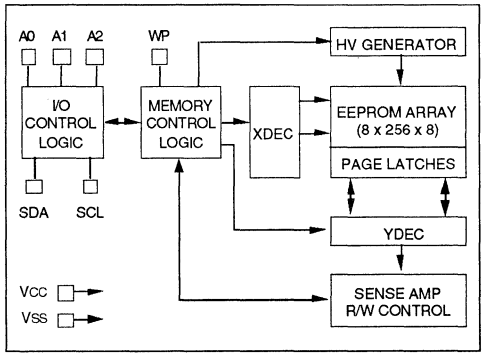
The Microchip Technology Inc. 24LC164 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC164 also has a page-write capability for up to 16 bytes of data. The 24LC164 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPE



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss .... -0.3V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5V to 5.5V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

			Vcc = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins: High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, FCLK = 1MHz
Operating current	Icc Write Icc Read	— —	3 1	mA mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	Iccs	— —	30 100	µA µA	Vcc = 3.0V, SDA = SCL = Vcc Vcc = 5.5V, SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

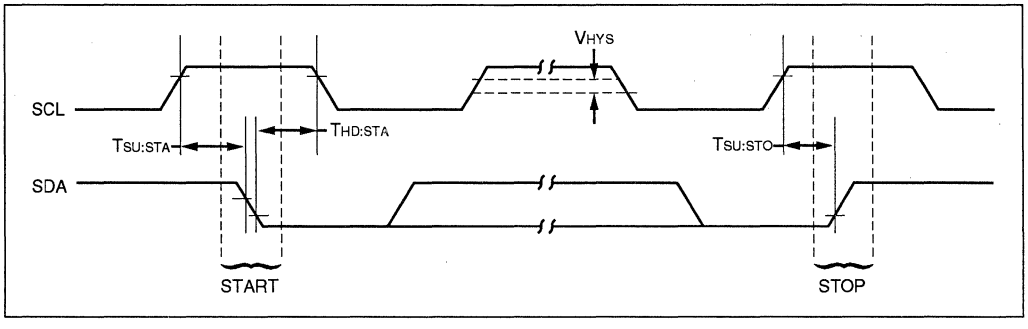
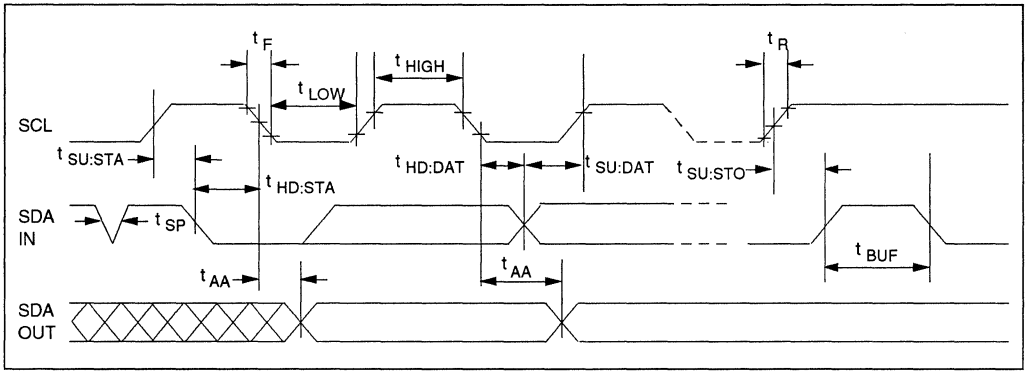


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	STANDARD MODE		Vcc = 4.5V - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	—	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC164 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC164 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

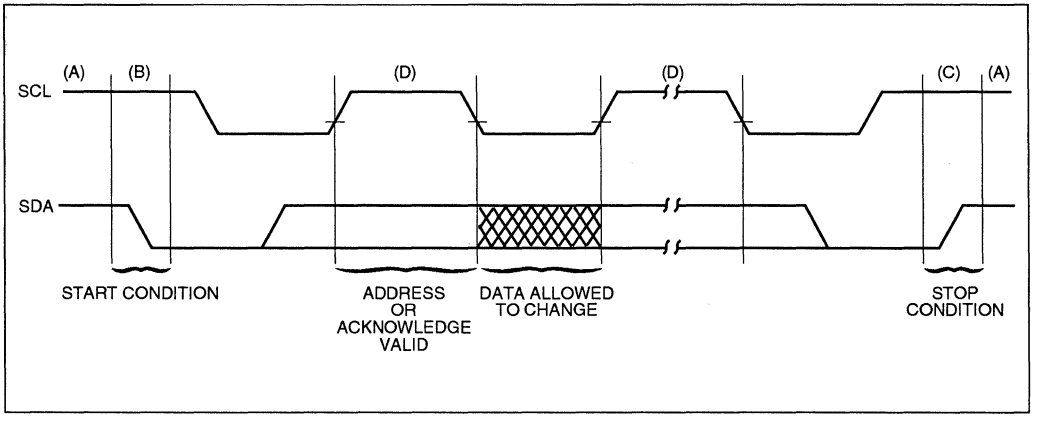
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC164 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC164) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation

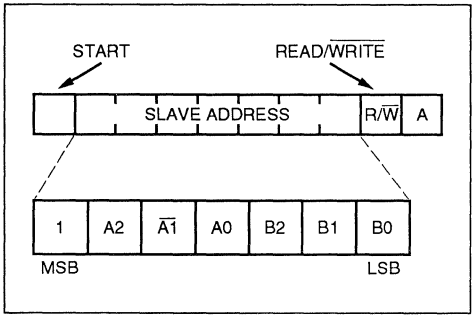
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC164 looks for the slave address for the device selected. Depending on the state of the R/$\overline{W}$ bit, the 24LC164 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1 A2 $\overline{A1}$ A0	Block Address	1
Write	1 A2 $\overline{A1}$ A0	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

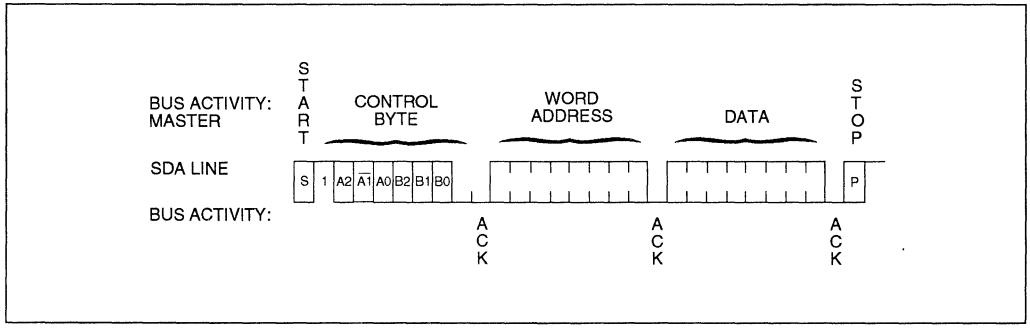
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC164. After receiving another acknowledge signal from the 24LC164 the master device will transmit the data word to be written into the addressed memory location. The 24LC164 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC164 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC164 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24LC164 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

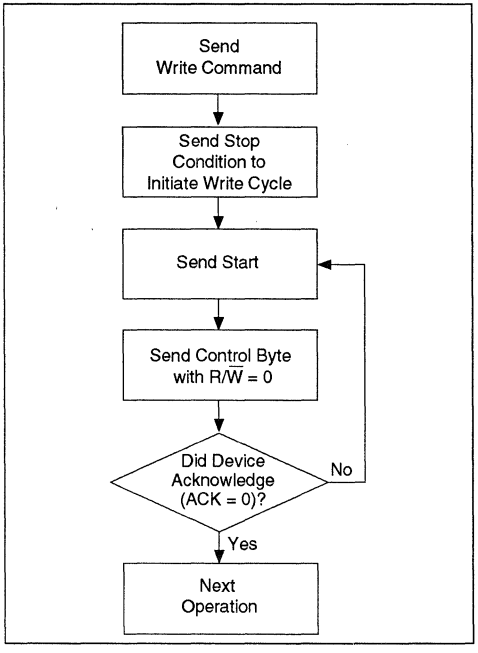
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24LC164 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

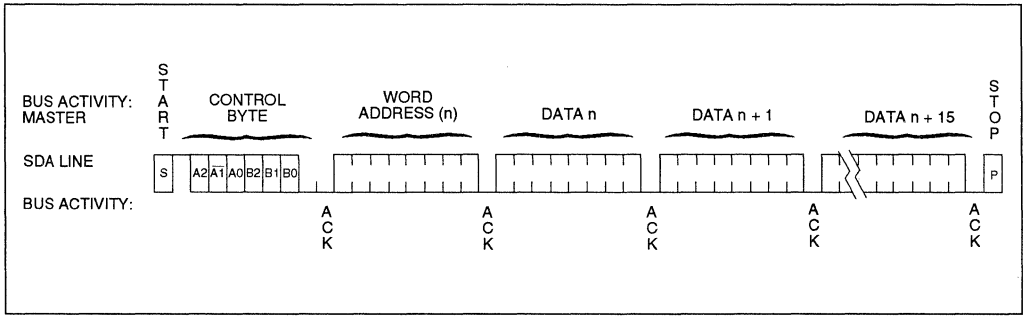
8.1 Current Address Read

The 24LC164 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC164 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC164 discontinues transmission (see Figure 9-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC164 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC164 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC164 discontinues transmission (see Figure 9-2).

FIGURE 8-1: PAGE WRITE



8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC164 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC164 to transmit the next sequentially addressed 8 bit word (see Figure 9-3).

To provide sequential reads the 24LC164 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

8.4 Noise Protection

The 24LC164 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC164 as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are used to configure the proper chip address in multiple-chip applications (more than one 24LC164 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note: The level on A1 is compared to the inverse of the slave address.

Up to eight 24LC164s may be connected to the same bus. These pins must be connected to either Vss or Vcc.

FIGURE 9-1: CURRENT ADDRESS READ

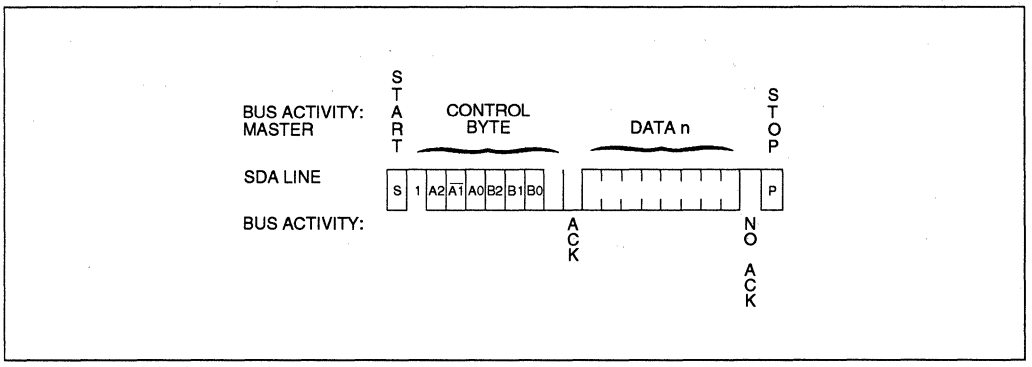


FIGURE 9-2: RANDOM READ

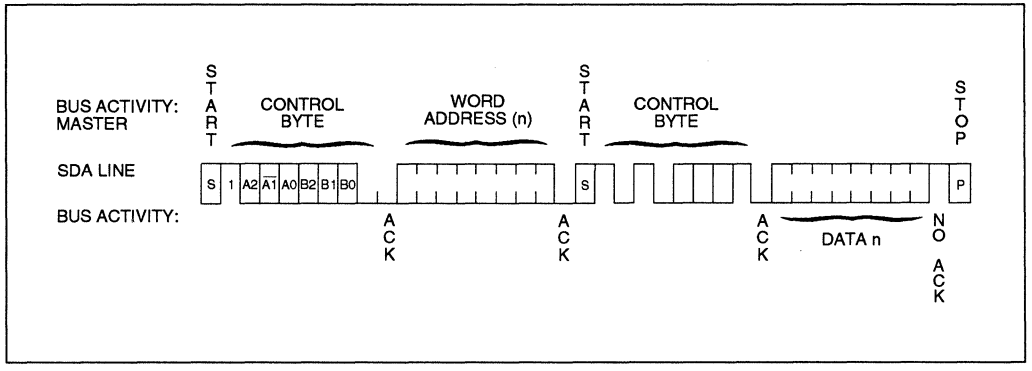
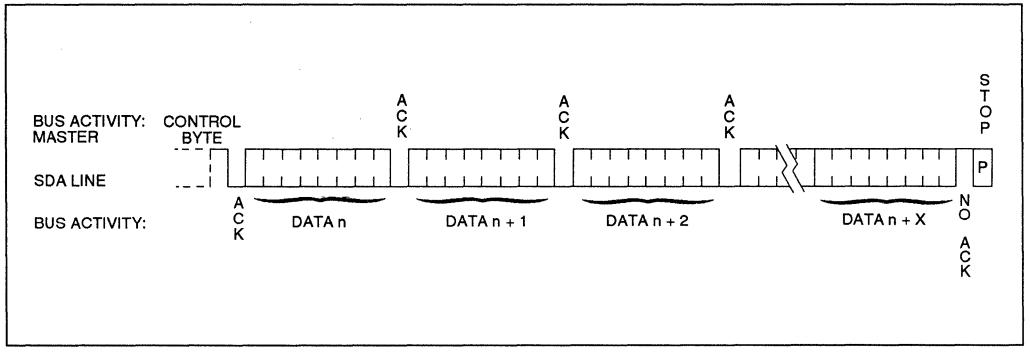


FIGURE 9-3: SEQUENTIAL READ



NOTES

24LC164 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC164 - /P

Package:		P =	Plastic DIP (300 mil Body), 8-lead
		SN =	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:		Blank =	0°C to +70°C
		I =	-40°C to +85°C
Device:	24LC164		16K CMOS Serial EEPROM
	24LC164T		16K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

24LC32

32K 2.5V CMOS Serial EEPROM

FEATURES

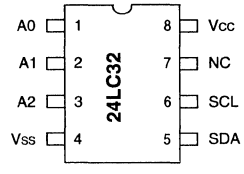
- Voltage operating range: 2.5V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
  - Including 100 kHz (2.5V) and 400 kHz (5V) modes
- Self-timed ERASE and WRITE cycles
- Power on/off data protection circuitry
- Endurance:
  - **10,000,000 ERASE/WRITE cycles guaranteed for High Endurance Block**
  - **100,000 E/W cycles guaranteed for Standard Endurance Block**
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Factory programming (QTP) available
- Up to 8 devices may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

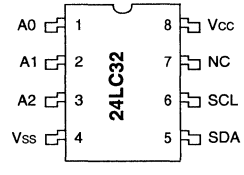
The Microchip Technology Inc. 24LC32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 6.0V). This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24LC32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24LC32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to 8 - 24LC32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology and broad voltage range make this device ideal for low-power/low voltage, non-volatile code and data applications. The 24LC32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

PACKAGE TYPE

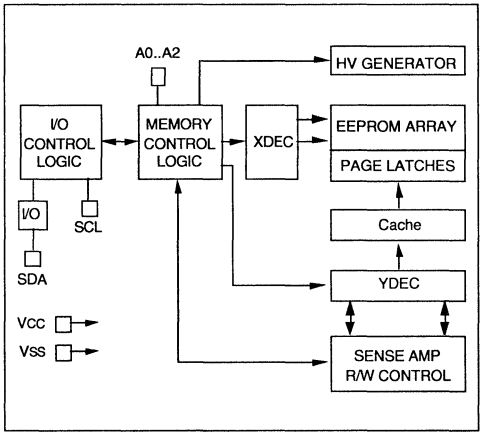
PDIP



SOIC



BLOCK DIAGRAM



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3

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTIONS

Name	Function
A0..A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+2.5V to 6.0V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

		VCC = +2.5V to 6.0V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC Write ICC Read	— —	3 150	mA µA	VCC = 6.0V, SCL = 400 kHz VCC = 6.0V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.0V, SCL = SDA = VCC Note 1

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

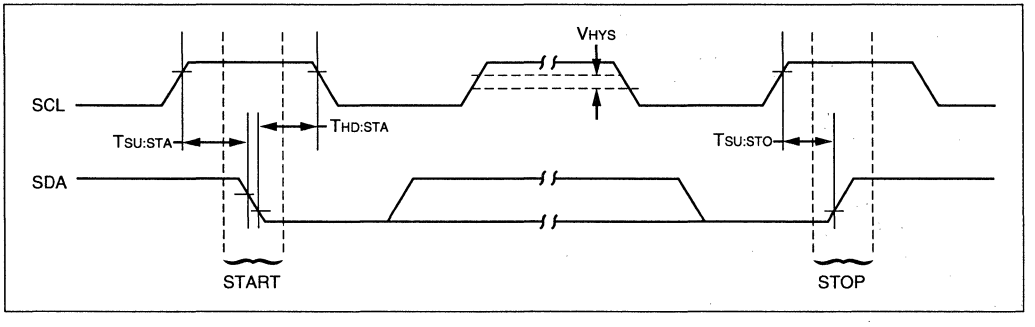


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	VCF = 2.5V-6.0V STD. MODE		V = 4.5 - 6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

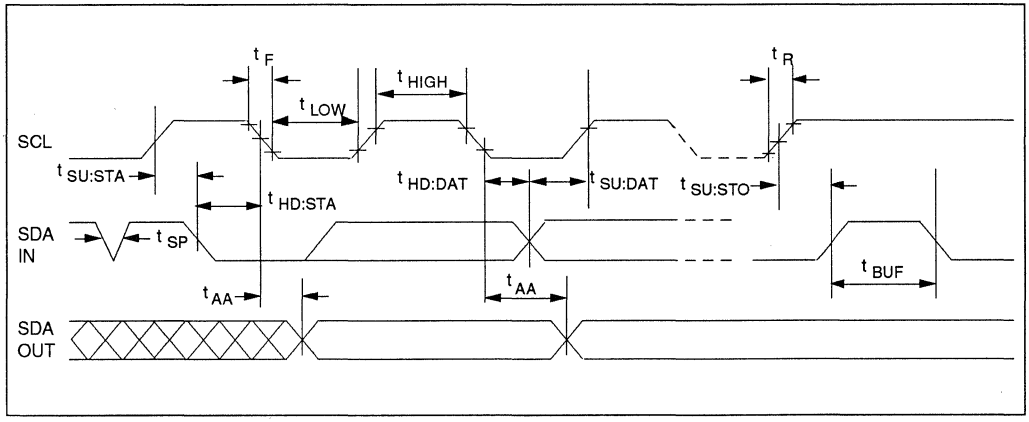
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (See Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

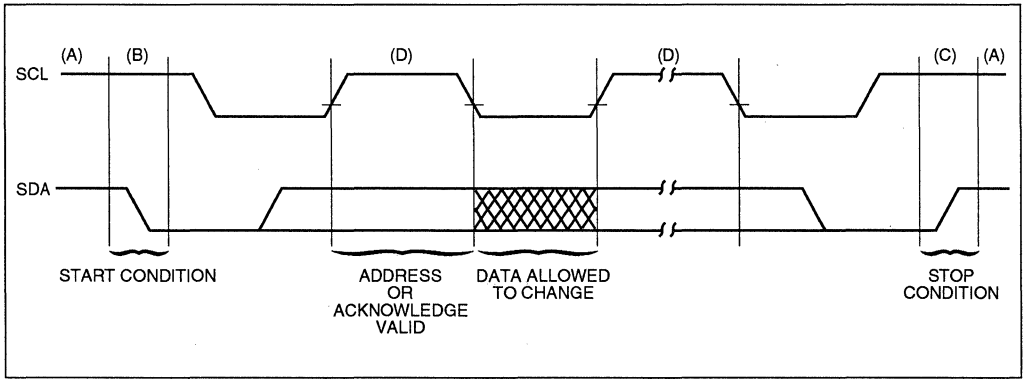
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC32) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation (Figure 4-1)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24LC32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 4-2). Because only A11...A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first.

Following the start condition, the 24LC32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC32 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

3

FIGURE 4-1: CONTROL BYTE ALLOCATION

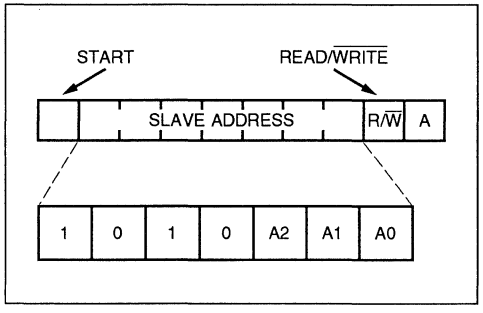
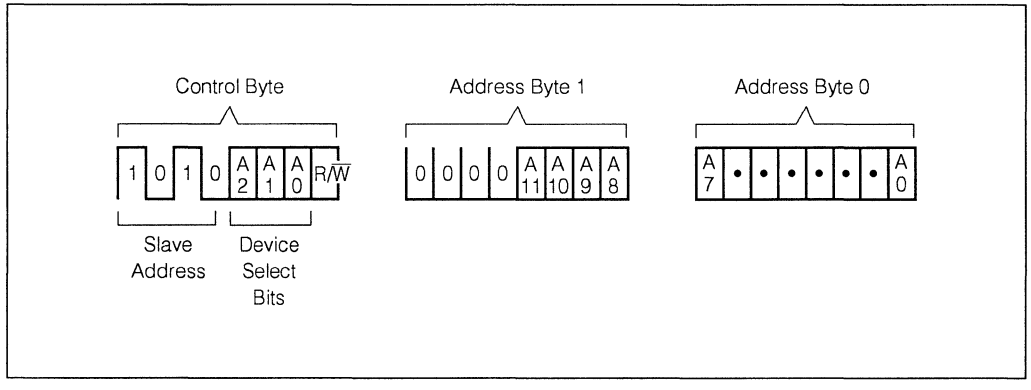


FIGURE 4-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



5.0 WRITE OPERATION

5.1 Split Endurance

The 24LC32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 10,000,000 E/W cycles guaranteed. The remainder of the array, 28K bits, is rated at 100,000 E/W cycles guaranteed. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

5.2 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24LC32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24LC32 the master device will transmit the data word to be written into the addressed memory location.

The 24LC32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC32 will not generate acknowledge signals (see Figure 5-1).

5.3 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24LC32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 5-2).

FIGURE 5-1: BYTE WRITE

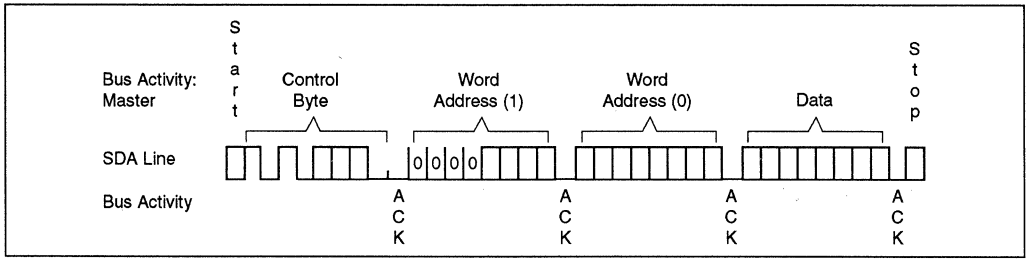
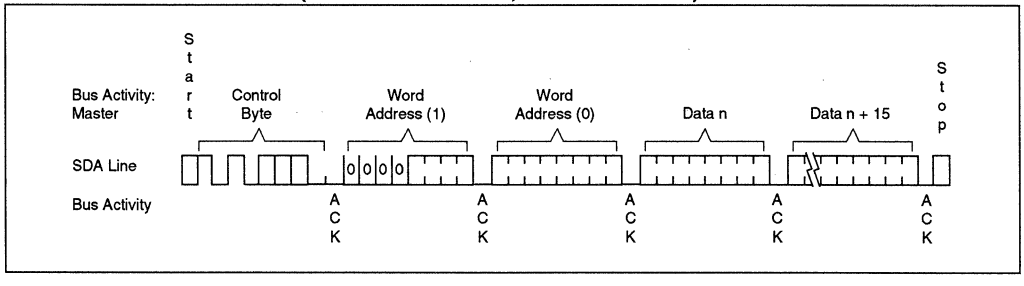


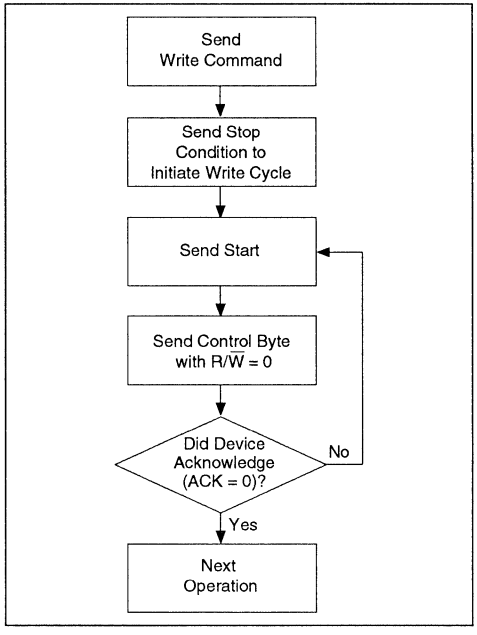
FIGURE 5-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 8-1)



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

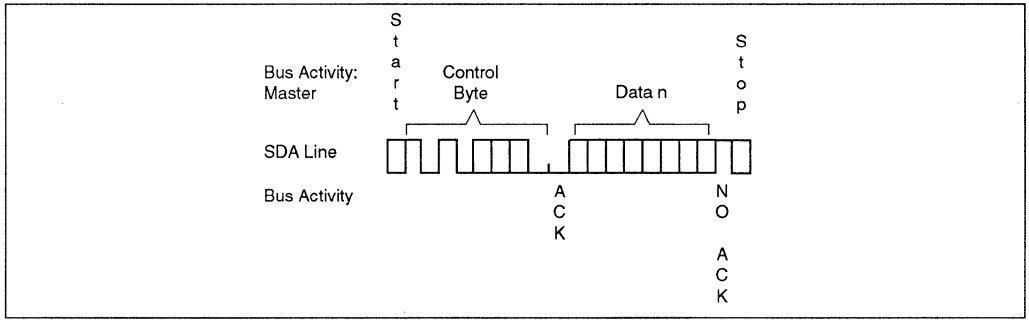
7.1 Current Address Read

The 24LC32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC32 discontinues transmission (see Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC32 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24LC32 to discontinue transmission (see Figure 7-2).

FIGURE 7-1: CURRENT ADDRESS READ



7.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24LC32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

7.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24LC32 to transmit the next sequentially addressed 8 bit word (see Figure 7-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24LC32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

7.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

FIGURE 7-2: RANDOM READ

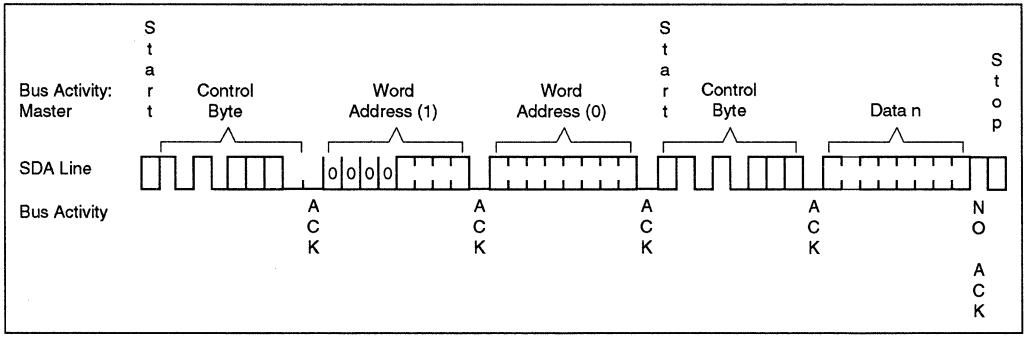
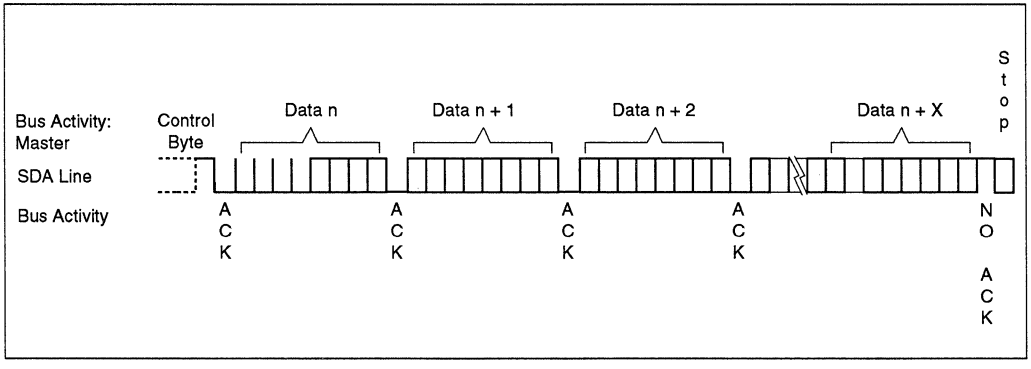


FIGURE 7-3: SEQUENTIAL READ



7.6 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.7 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 5-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.8 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 8-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.9 Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24LC32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figure 4-2).

8.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz)

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 8-1: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

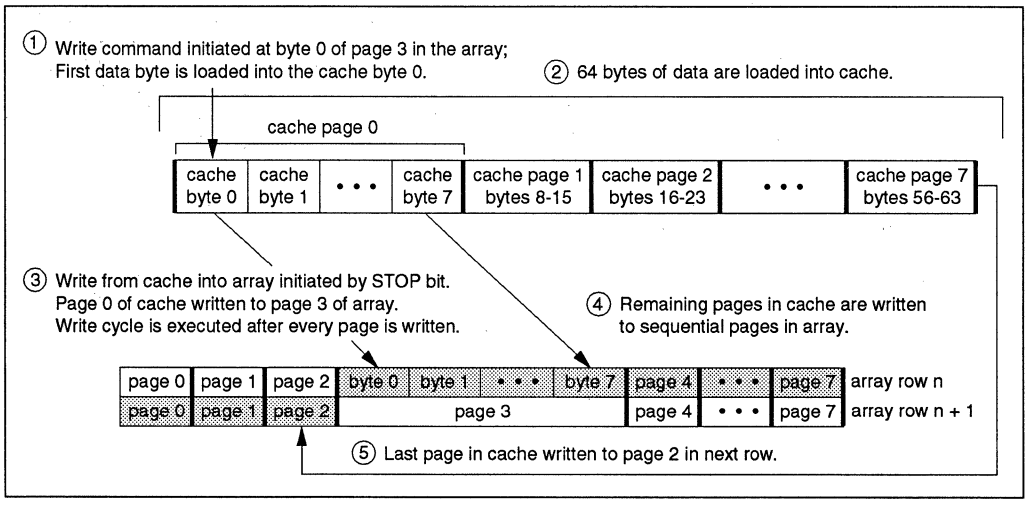
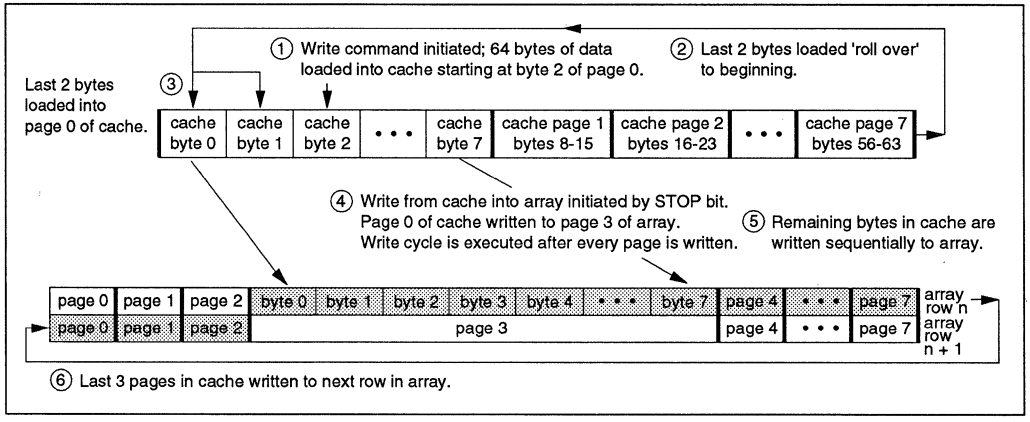


FIGURE 8-2: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



NOTES

24LC32 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC32 - /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SM =	Plastic SOIC (207 mil Body, EIAJ standard)
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Device:	24LC32	32K CMOS Serial EEPROM (100 kHz, 400 kHz)
	24LC32T	32K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24C01A/02A/04A

1K/2K/4K 5.0V CMOS Serial EEPROMs

FEATURES

- Low power CMOS technology
- Hardware write protect
- Two wire serial interface bus, I²C™ compatible
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer
- 1ms write cycle time for single byte
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data retention >40 years
- 8-pin DIP/SOIC packages
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

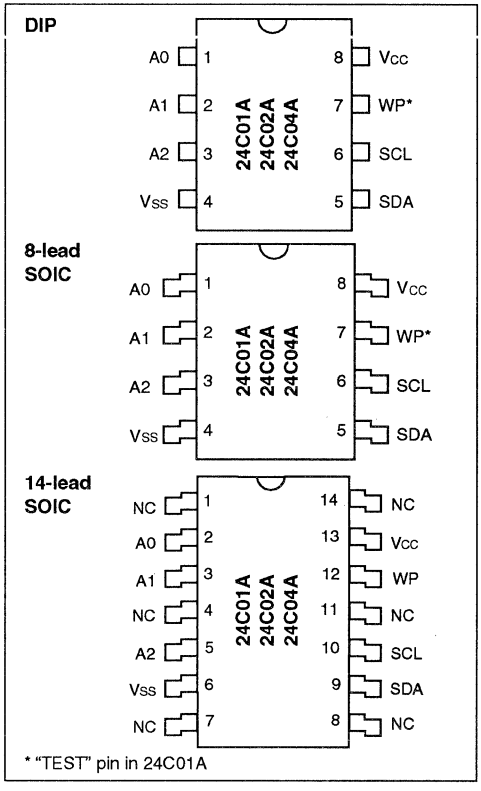
DESCRIPTION

The Microchip Technology Inc. 24C01A/02A/04A is a 1K/2K/4K bit Electrically Erasable PROM. The device is organized as shown, with a standard two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. A special feature in the 24C02A and 24C04A provides hardware write protection for the upper half of the block. The 24C01A and 24C02A have a page write capability of two bytes and the 24C04A has a page length of eight bytes. Up to eight 24C01A or 24C02A devices and up to four 24C04A devices may be connected to the same two wire bus.

This device offers fast (1ms) byte write and extended (-40°C to 125°C) temperature operation. It is recommended that all other applications use Microchip's 24LCXXB.

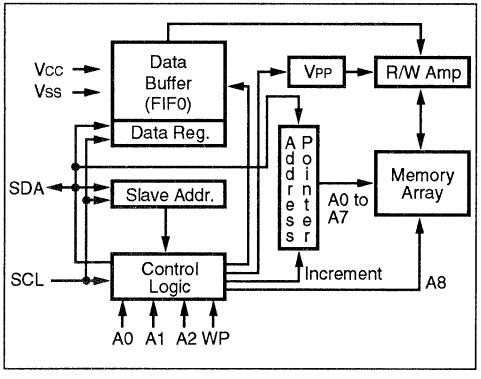
	24C01A	24C02A	24C04A
Organization	128 x 8	258 x 8	2 x 256 x 8
Write Protect	None	080-0FF	100-1FF
Page Write Buffer	2 Bytes	2 Bytes	8 Bytes

PACKAGE TYPE



* "TEST" pin in 24C01A

BLOCK DIAGRAM



I²C is a trademark of Phillips Corporation

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V

All inputs and outputs w.r.t. Vss .... -0.6V to Vcc +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0	No Function for 24C04A only, Must be connected to Vcc or Vss
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
TEST	(24C01A only) Vcc or Vss
WP	Write Protect Input
Vcc	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

Vcc = +5V (±10%)		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to +125°C			
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL		Vcc x 0.3	V	
Low level output voltage	VOL	-0.3	0.4	V	IOL = 3.2 mA (SDA only)
A1 & A2 pins:					
High level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI	—	10	µA	VIN = 0V to Vcc
Output leakage current	ILO	—	10	µA	VOUT = 0V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	7.0	pF	VIN/VOUT = 0V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	Icc Write	—	3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = 0°C to +70°C
	Icc Write	—	4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = (I) and (E)
	Icc Read	—	750	µA	Vcc = 5V, Tamb= (C), (I) and (E)
Standby current	Iccs	—	100	µA	SDA=SCL=Vcc=5V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

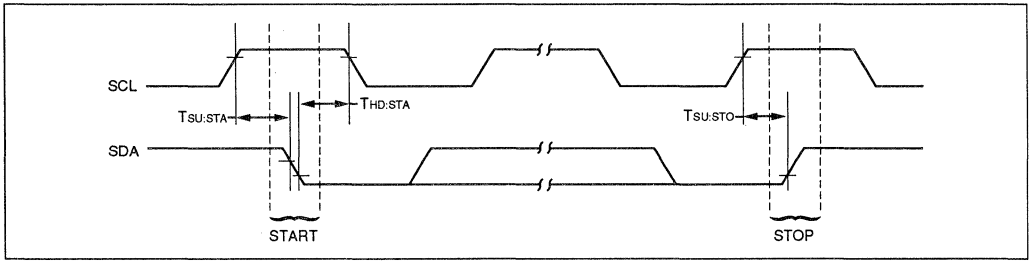
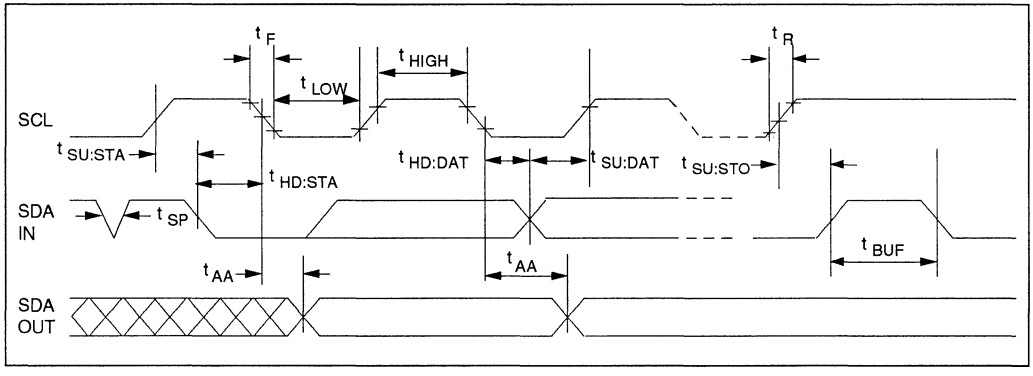


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min.	Typ	Max.	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	THIGH	4000	—	—	ns	
Clock low time	TLOW	4700	—	—	ns	
SDA and SCL rise time	TR	—	—	1000	ns	
SDA and SCL fall time	TF	—	—	300	ns	
START condition hold time	THD:STA	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	—	ns	
Data input setup time	TSU:DAT	250	—	—	ns	
Data output delay time	TAA	300	—	3500		Note 1
STOP condition setup time	TSU:STO	4700	—	—	ns	
Bus free time	TBUF	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI	—	—	100	ns	
Program cycle time	TWC	—	.4	1	ms	Byte mode
			.4N	N	ms	Page mode, N=# of bytes

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24C01A/02A/04A supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C01A/02A/04A works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

Up to eight 24C01/24c02s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Up to four 24C04As can be connected to the bus, selected by A1 and A2 chip address inputs. A0 must be tied to Vcc or Vss for the 24C04A. Other devices can be connected to the bus but require different device codes than the 24C01A/02A/04A (refer to section Slave Address).

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

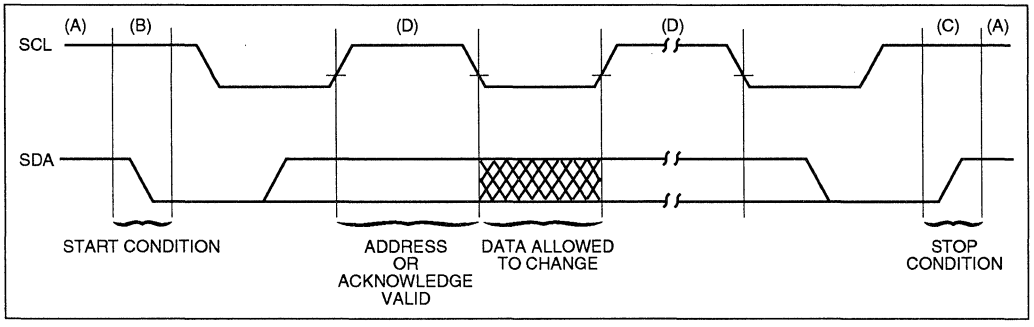
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C01A/02A/04A does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



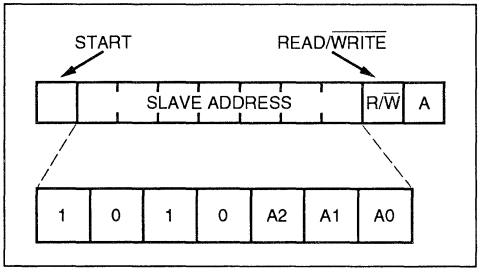
4.0 SLAVE ADDRESS

The chip address inputs A0, A1 and A2 of each 24C01A/02A/04A must be externally connected to either Vcc or ground (Vss), assigning to each 24C01A/02A/04A a unique address. A0 is not used on the 24C04A and must be connected to either Vcc or Vss. Up to eight 24C01A or 24C02A devices and up to four 24C04A devices may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the slave address to the corresponding hard-wired logic levels of the selected 24C01A/02A/04A. After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C01A/02A/04A, followed by the chip address bits A0, A1 and A2. In the 24C04A, the seventh bit of that byte (A0) is used to select the upper block (addresses 100—1FF) or the lower block (addresses 000—0FF) of the array.

The eighth bit of slave address determines if the master device wants to read or write to the 24C01A/02A/04A (see Figure 4-1).

The 24C01A/02A/04A monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 4-1: SLAVE ADDRESS ALLOCATION



5.0 BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 24C01A/02A/04A.

Following the START signal from the master, the device code (4-bits), the slave address (3-bits), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 24C01A/02A/04A that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01A/02A/04A. After receiving the acknowledge of the 24C01A/02A/04A, the master device transmits the data word to be written into the addressed memory location. The 24C01A/02A/04A acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 24C01A/02A/04A (see Figure 6-1).

6.0 PAGE PROGRAM MODE

To program the 24C01A/02A/04A, the master sends addresses and data to the 24C01A/02A/04A which is the slave (see Figure 6-1 and Figure 6-2). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 24C01A/02A/04A, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. (The A0 bit transmitted with the slave address is the ninth bit of the address pointer for the 24C04A). The 24C01A/02A/04A will generate an acknowledge after every 8-bits received and store them consecutively in a RAM buffer until a STOP condition is detected. This STOP condition initiates the internal programming cycle. The RAM buffer is 2 bytes for the 24C01A/02A and 8 bytes for the 24C04A. If more than 2 bytes are transmitted by the master to the 24C01A/02A, the device will not acknowledge the data transfer and the sequence will be aborted. If more than 8 bytes are transmitted by the master to the 24C04A, it will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address registers bottom 3 bits to increment while the upper 5 bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 6-1), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received data bytes in the page buffer will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 8 for 24C04A, 2 for 24C01A/02A).

3

FIGURE 6-1: BYTE WRITE

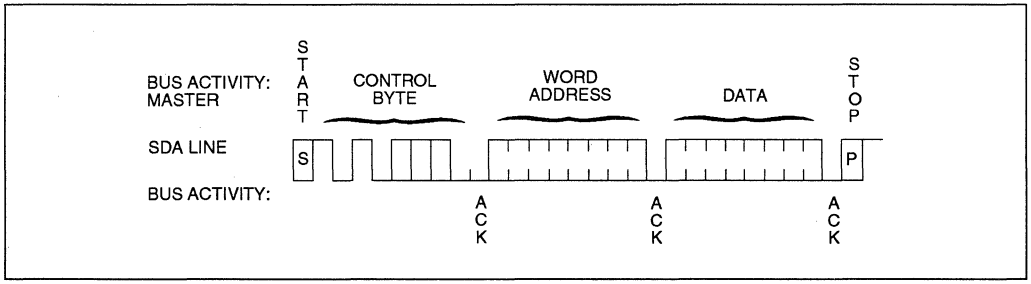
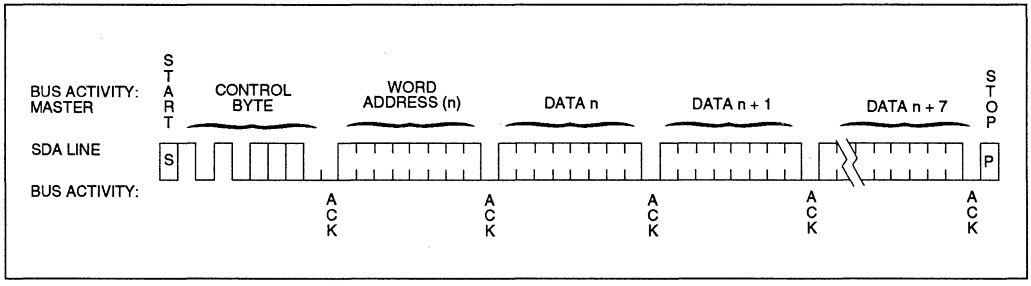


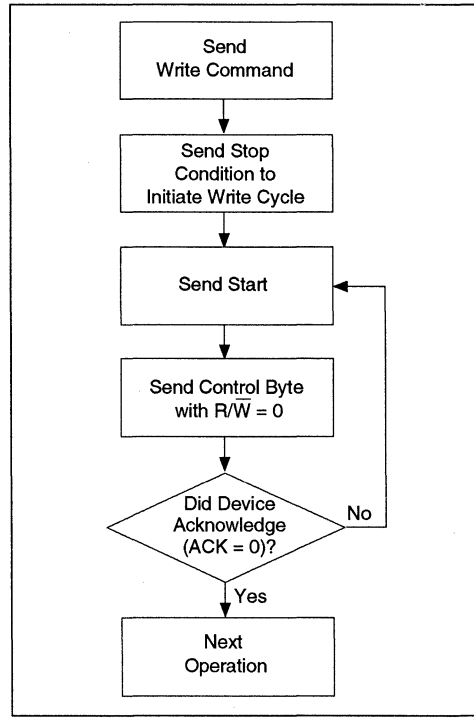
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the 24C02A or 24C04A is connected to VCC (+5V). The device will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the 24C02A/04A will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the STOP condition is asserted. Polarity of the WP pin has no effect on the 24C01A.

9.0 READ MODE

This mode illustrates master device reading data from the 24C01A/02A/04A.

As can be seen from Figure 9-2 and Figure 9-3, the master first sets up the slave and word addresses by doing a write. (Note: Although this is a read mode, the address pointer must be written to). During this period the 24C01A/02A/04A generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This auto-increment sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note 1: If the master knows where the address pointer is, it can begin the read sequence at the current address (see Figure 9-1) and save time transmitting the slave and word addresses.

Note 2: In all modes, the address pointer will not increment through a block (256 byte) boundary, but will rotate back to the first location in that block.

3

FIGURE 9-1: CURRENT ADDRESS READ

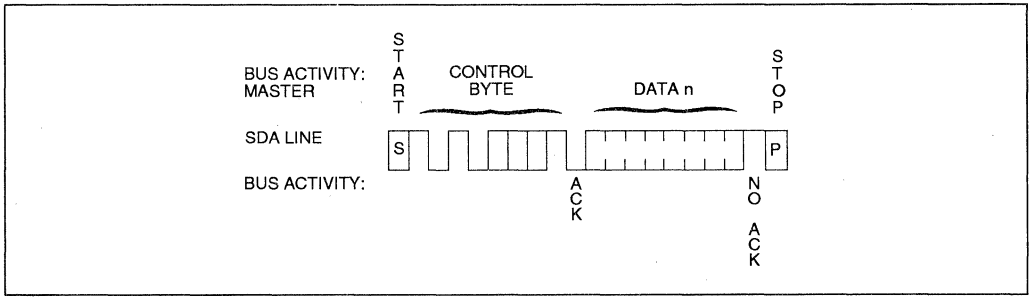


FIGURE 9-2: RANDOM READ

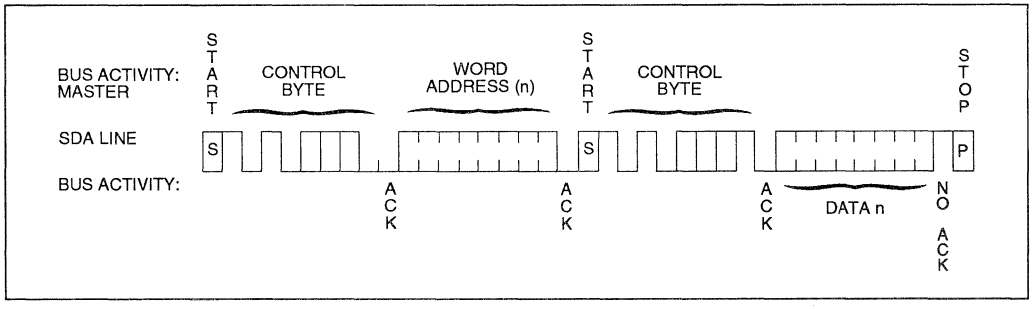
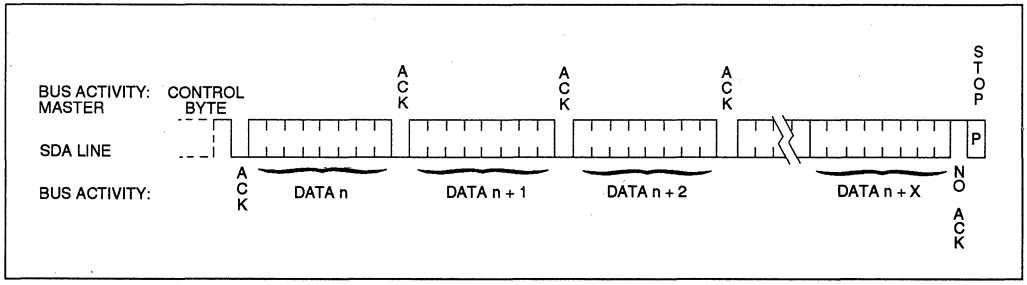


FIGURE 9-3: SEQUENTIAL READ



10.0 PIN DESCRIPTION

10.1 A0, A1, A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. For 24C04 A0 is no function.

Up to eight 24C01A/02A's or up to four 24C04A's can be connected to the bus.

These inputs must be connected to either Vss or Vcc.

10.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10KΩ).

For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

10.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

10.4 WP Write Protection

This pin must be connected to either Vcc or Vss for 24C02A or 24C04A. It has no effect on 24C01A.

If tied to Vcc, PROGRAM operations onto the upper memory block will not be executed. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Note 1: A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 24C04A page is 8 bytes long; the 24C01A/02A page is 2 bytes long.

Note 2: A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will however, wrap around from the end of a block to the first location in the same block. The 24C04A has two blocks, 256 bytes each. The 24C01A and 24C02A each have only one block.

NOTES

24C01A/02A/04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24C01A - /P

Package:	J	= CERDIP
	P	= Plastic DIP
	SN	= Plastic SOIC (150 mil Body), 8-lead, 24C01A/02A only
	SM	= Plastic SOIC (207 mil Body), 8-lead
	SL	= Plastic SOIC (150 mil Body), 14-lead, 24C04A only
Temperature Range:	Blank	= 0°C to +70°C
	I	= -40°C to +85°C
	E	= -40°C to +125°C
Device:	24C01A	1K CMOS Serial EEPROM
	24C01AT	1K CMOS Serial EEPROM (Tape and Reel)
	24C02A	2K CMOS Serial EEPROM
	24C02AT	2K CMOS Serial EEPROM (Tape and Reel)
	24C04A	4K CMOS Serial EEPROM
	24C04AT	4K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24C08B/16B

8K/16K 5.0V E-Temperature Serial EEPROMs

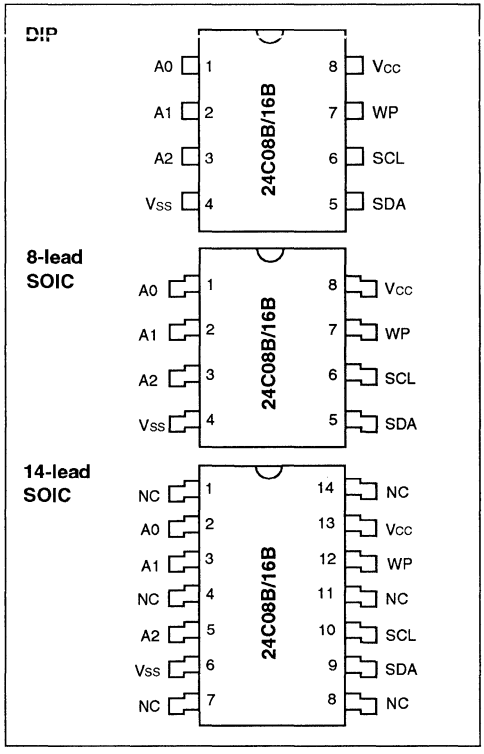
FEATURES

- Single supply with operation from 4.5-5.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as 4 or 8 blocks of 256 bytes (4 x 256 x 8) or (8 x 256 x 8)
- Two wire serial interface bus, I²C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data retention > 40 years
- 8 pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature range
  - Automotive: -40°C to +125°C

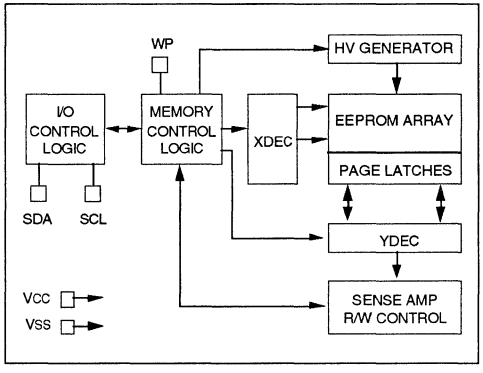
DESCRIPTION

The Microchip Technology Inc. 24C08B/16B is an 8K/16K bit Electrically Erasable PROM intended for use in extended/automotive temperature ranges. The device is organized as 4 or 8 blocks of 256 x 8 bit memory with a two wire serial interface. The 24C08B/16B also has a page-write capability for up to 16 bytes of data. The 24C08B/16B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.

PACKAGE TYPE



BLOCK DIAGRAM



I²C is a trademark of Phillips Corporation.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V

All inputs and outputs w.r.t. Vss .... -0.6V to Vcc +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+4.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			Vcc = +4.5V to +5.5V Automotive (E): Tamb = -40°C to +125°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins: High level input voltage	VIH	.7 Vcc	—	V	
Low Level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, Vcc=4.5V
Input leakage current	ILI	-10	10	µA	VIN =.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, FCLK=1 MHz
Operating current	ICC write ICC read	— —	3 1	mA mA	Vcc = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	100	µA	Vcc = 5.5V, SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

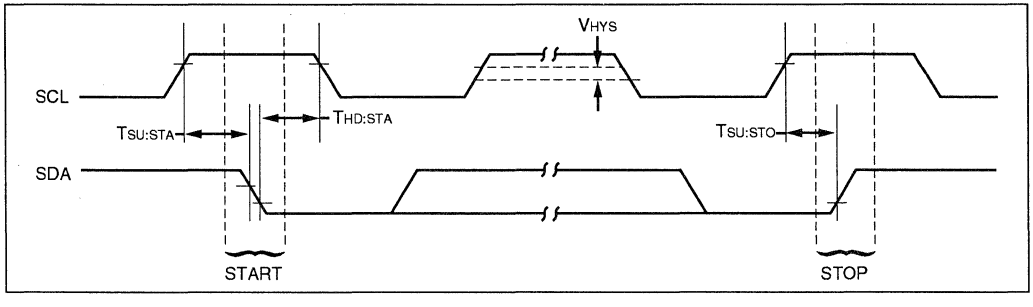
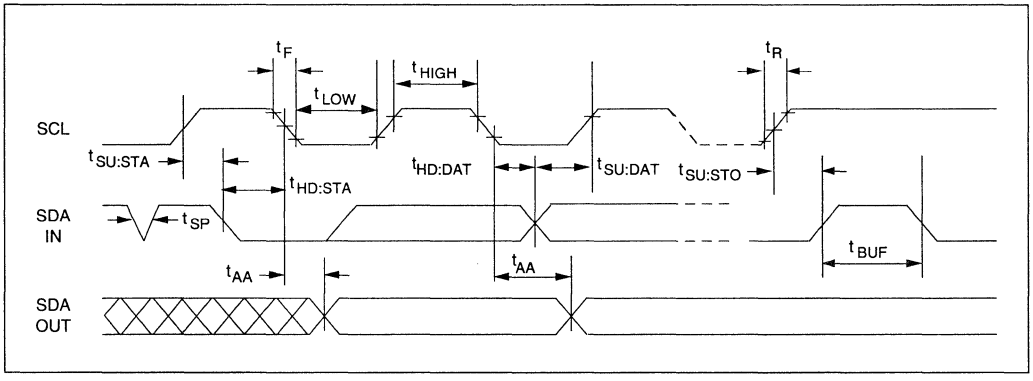


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Remarks
Clock frequency	FCLK	0	100	kHz	
Clock high time	THIGH	4000	—	ns	
Clock low time	TLOW	4700	—	ns	
SDA and SCL rise time	TR	—	1000	ns	Note 2
SDA and SCL fall time	TF	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	ns	
Data input setup time	TSU:DAT	250	—	ns	
STOP condition setup time	TSU:STO	4000	—	ns	
Output valid from clock	TAA	—	3500	ns	Note 1
Bus free time	TBUF	4700	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	ns	Note 3
Write cycle time	TWR	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24C08B/16B supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C08B/16B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

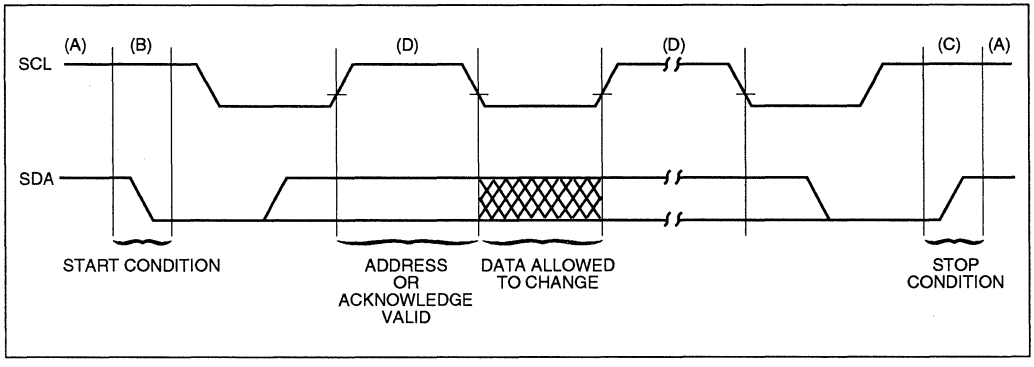
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C08B/16B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C08B/16B) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

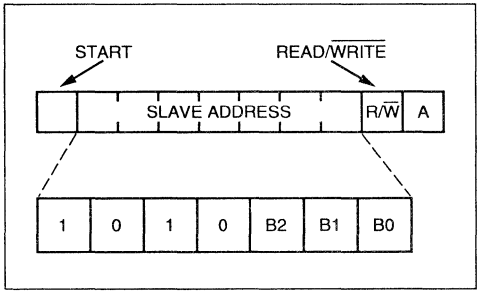
4.1 Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24C08B/16B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24C08B/16B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C08B/16B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

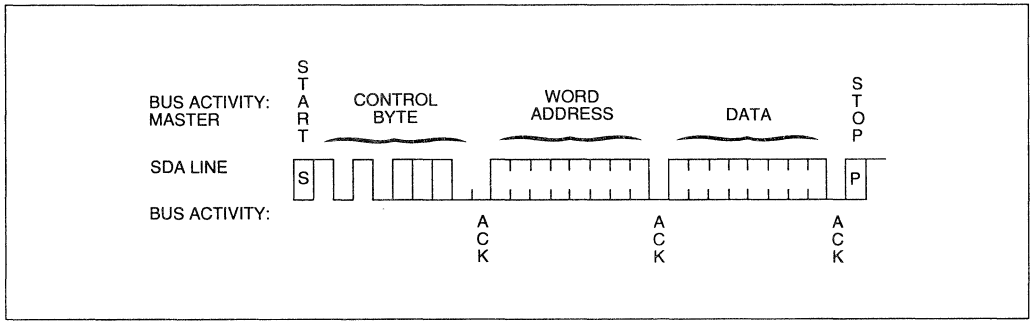
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C08B/16B. After receiving another acknowledge signal from the 24C08B/16B the master device will transmit the data word to be written into the addressed memory location. The 24C08B/16B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C08B/16B will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C08B/16B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24C08B/16B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

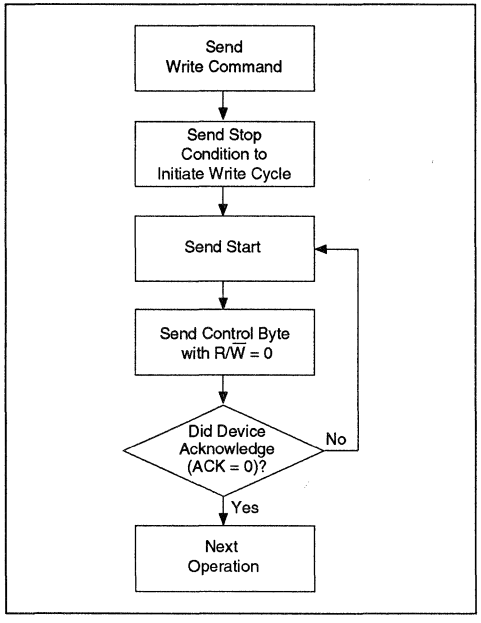
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24C08B/16B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24C08B/16B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C08B/16B issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C08B/16B discontinues transmission (see Figure 8-2).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C08B/16B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C08B/16B will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C08B/16B discontinues transmission (see Figure 8-3).

FIGURE 8-1: PAGE WRITE

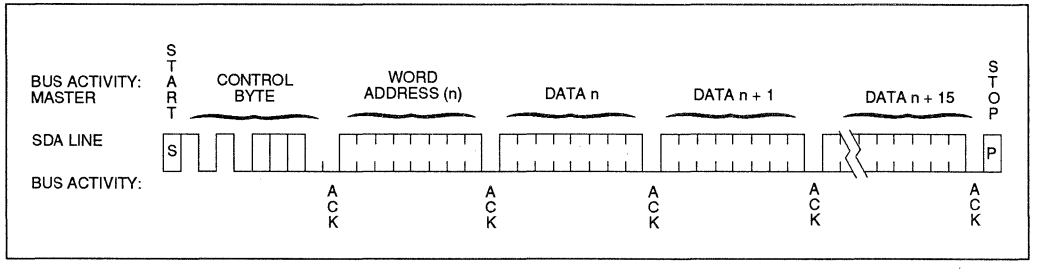


FIGURE 8-2: CURRENT ADDRESS READ

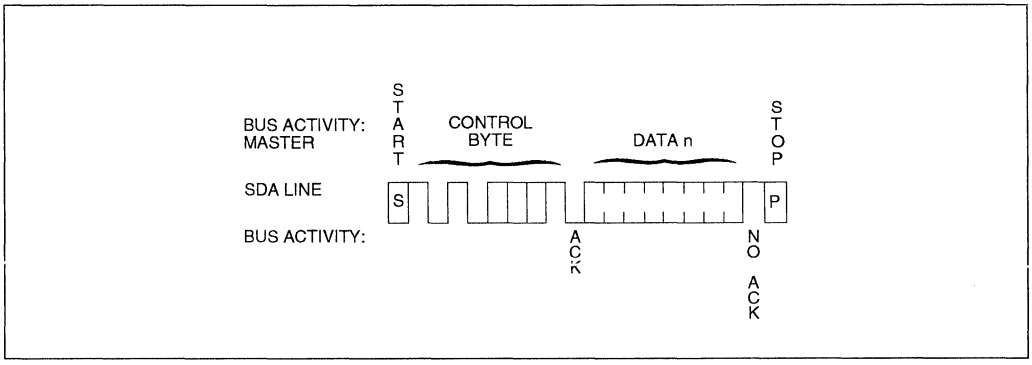
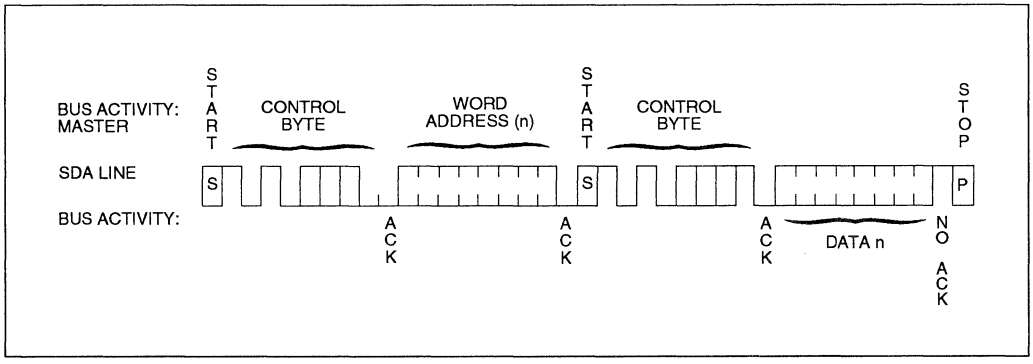


FIGURE 8-3: RANDOM READ



3

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C08B/16B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C08B/16B to transmit the next sequentially addressed 8 bit word (see Figure 9-1).

To provide sequential reads the 24C08B/16B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

8.4 Noise Protection

The 24C08B/16B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10Ω).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

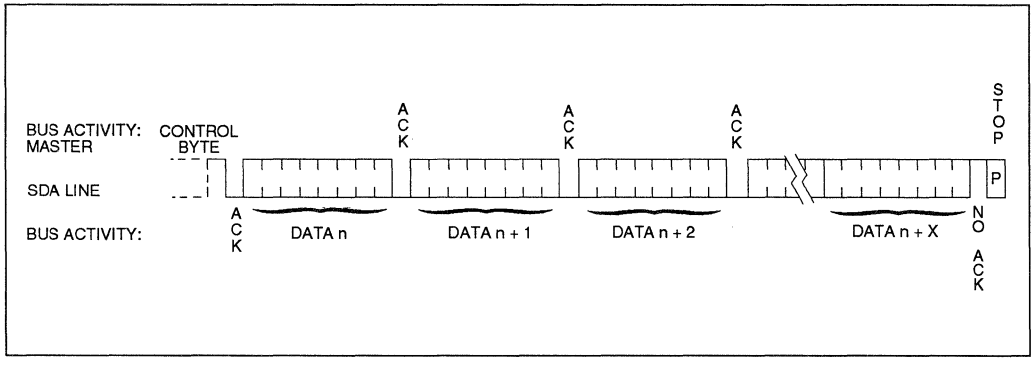
If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24C08B/16B as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are not used by the 24C08B/16B. They may be left floating or tied to either Vss or Vcc.

FIGURE 9-1: SEQUENTIAL READ



NOTES

24C08B/16B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24CXXB - /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	E =	-40°C to +125°C
Device:	24C16B	16K CMOS Serial EEPROM
	24C16BT	16K CMOS Serial EEPROM (Tape and Reel)
	24C08B	8K CMOS Serial EEPROM
	24C08BT	8K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

24C32

32K 5.0V CMOS Serial EEPROM

FEATURES

- Voltage operating range: 4.5V to 5.5V
  - Peak write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 1 µA typical
- Industry standard two-wire bus protocol, I²C™ compatible
  - Including 100 kHz and 400 kHz modes
- Self-timed write cycle (including auto-erase)
- Power on/off data protection circuitry
- Endurance:
  - **10,000,000 ERASE/WRITE cycles guaranteed for High Endurance Block**
  - **100,000 E/W cycles guaranteed for Standard Endurance Block**
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Factory programming (QTP) available
- Up to 8 chips may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

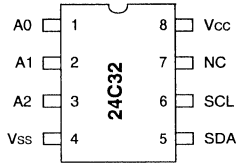
DESCRIPTION

The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to 8 - 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24C32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

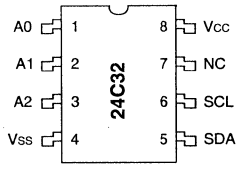
I²C is a trademark of Philips Corporation

PACKAGE TYPE

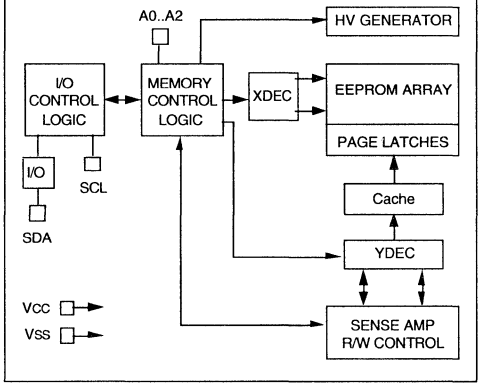
PDIP



SOIC



BLOCK DIAGRAM



3

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0..A2	User Configurable Chip Selects
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
VCC	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 VCC	—	V	
Low level input voltage	VIL	—	.3 VCC	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V TO VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE ICC Read	— —	3 150	mA µA	VCC = 5.5V, SCL = 400 kHz VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.5V, SCL = SDA = VCC Note 1

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

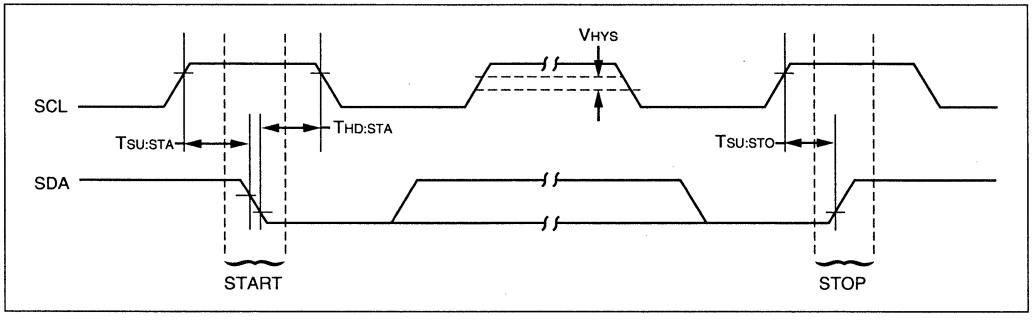
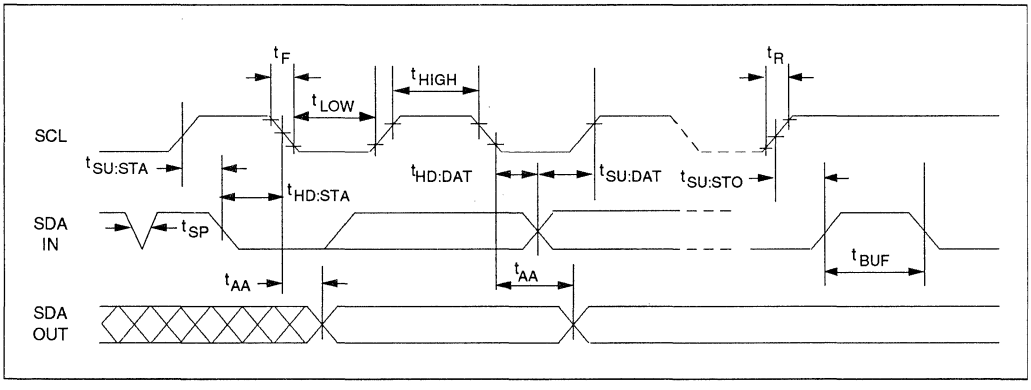


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 4.5V - 5.5V STD. MODE		Vcc = 4.5V - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.
Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.
Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24C32 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C32 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

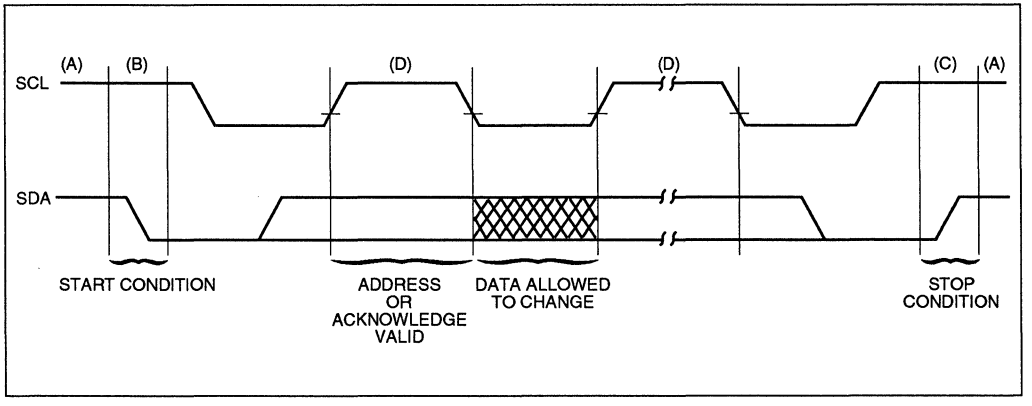
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C32 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C32) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation (Figure 4-1)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code; for the 24C32 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 4-2). Because only A11..A0 are used, the upper four address bits must be zeros. The most significant bit of the most significant byte of the address is transferred first. Following the start condition, the 24C32 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C32 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION

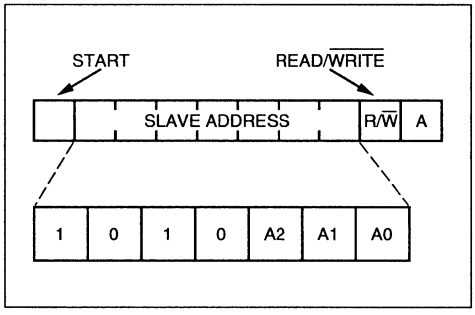
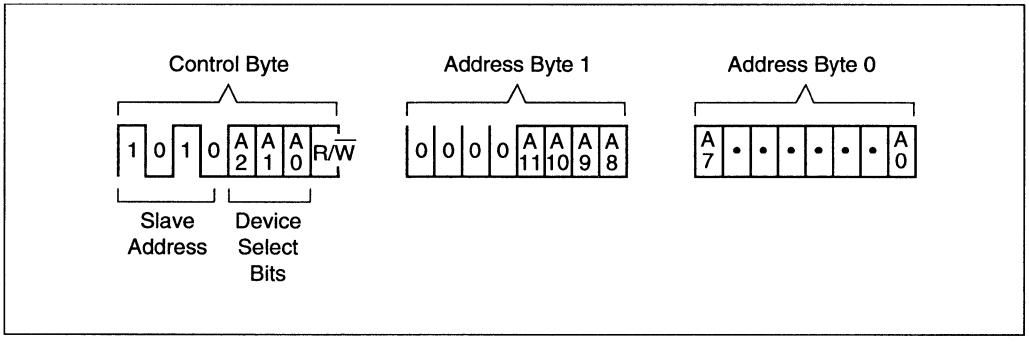


FIGURE 4-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



4.2 WRITE OPERATION

4.3 Split Endurance

The 24C32 is organized as a continuous 32K block of memory. However, the first 4K, starting at address 000, is rated at 10,000,000 E/W cycles guaranteed. The remainder of the array, 28K bits, is rated at 100K E/W cycles guaranteed. This feature is helpful in applications in which some data change frequently, while a majority of the data change infrequently. One example would be a cellular telephone in which last-number redial and microcontroller scratch pad require a high-endurance block, while speed dials and lookup tables change infrequently and so require only a standard endurance rating.

4.4 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24C32. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24C32 the master device will transmit the data word to be written into the addressed memory location. The 24C32 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C32 will not generate acknowledge signals (see Figure 4-3).

4.5 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C32 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24C32. They will be written from cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once a stop condition is received, an internal write cycle will begin. The 64-byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 4-4).

FIGURE 4-3: BYTE WRITE

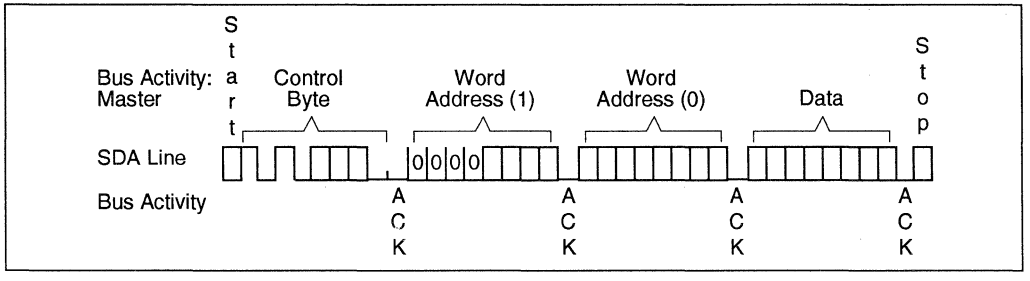
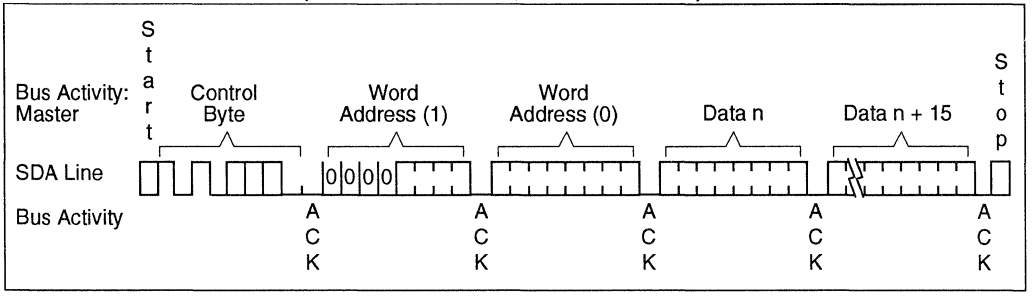


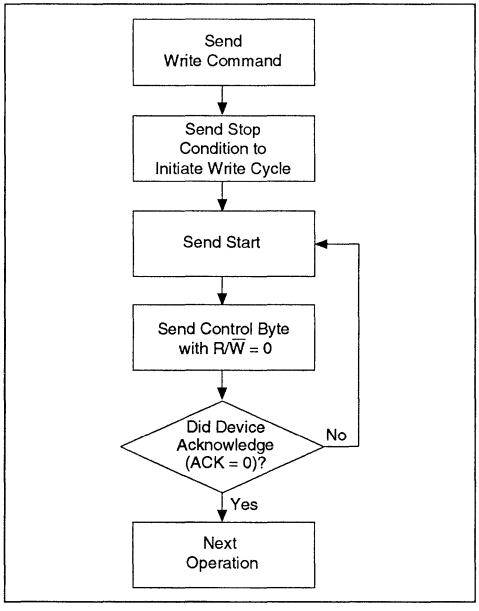
FIGURE 4-4: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 6-3)



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

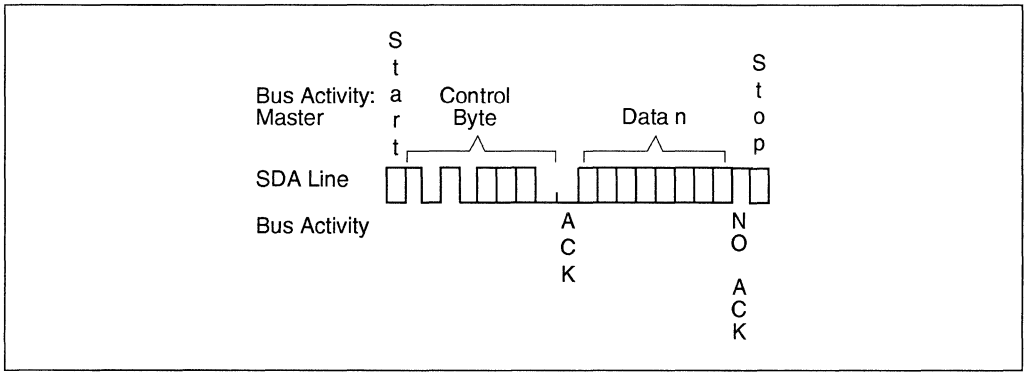
6.1 Current Address Read

The 24C32 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C32 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C32 discontinues transmission (see Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C32 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C32 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24C32 to discontinue transmission (see Figure 6-2).

FIGURE 6-1: CURRENT ADDRESS READ



6.3 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 256K bits by adding up to eight 24C32's on the same bus. In this case, software can use A0 of the control byte as address bit A12, A1 as address bit A13, and A2 as address bit A14.

6.4 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C32 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24C32 to transmit the next sequentially addressed 8 bit word. (See Figure 6-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24C32 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The address pointer, however, will not roll over from address 07FF to address 0000. It will roll from 07FF to unused memory space.

6.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to ensure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

FIGURE 6-2: RANDOM READ

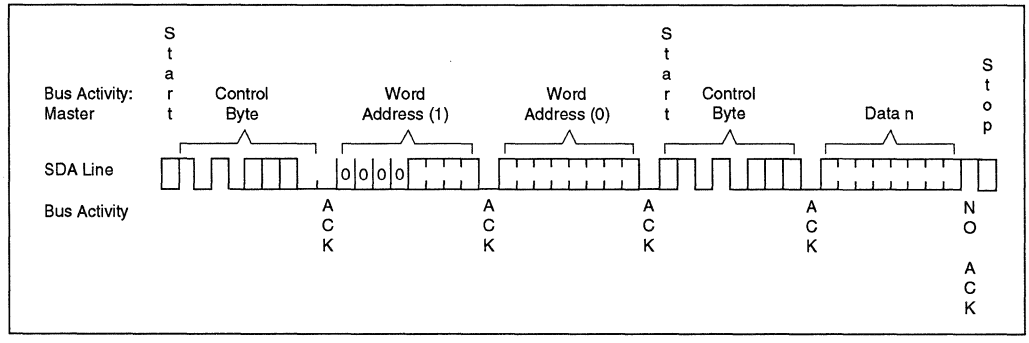
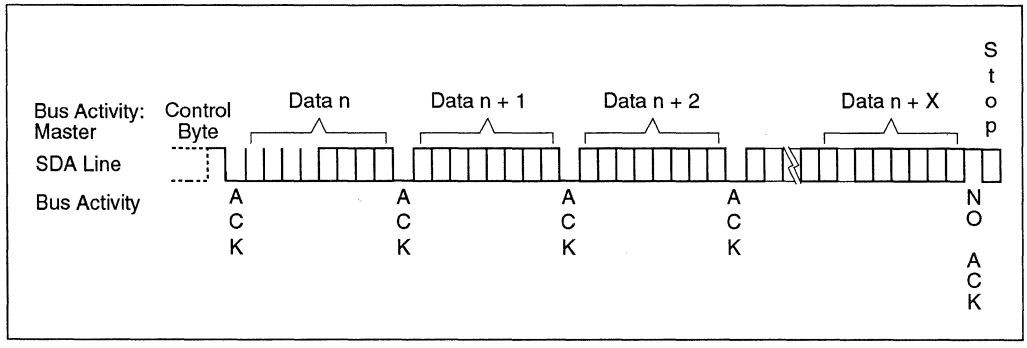


FIGURE 6-3: SEQUENTIAL READ



7.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

7.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 8-1) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

7.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 8-2, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

7.3 Power Management

This design incorporates a power standby mode when the device is not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, ie. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

8.0 PIN DESCRIPTIONS

8.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24C32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figure 4-2).

8.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

FIGURE 8-1: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

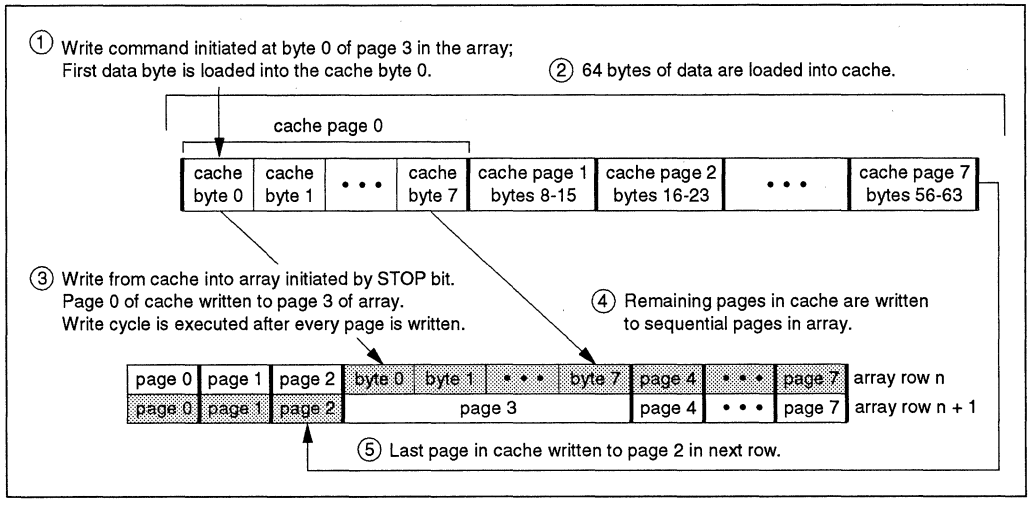
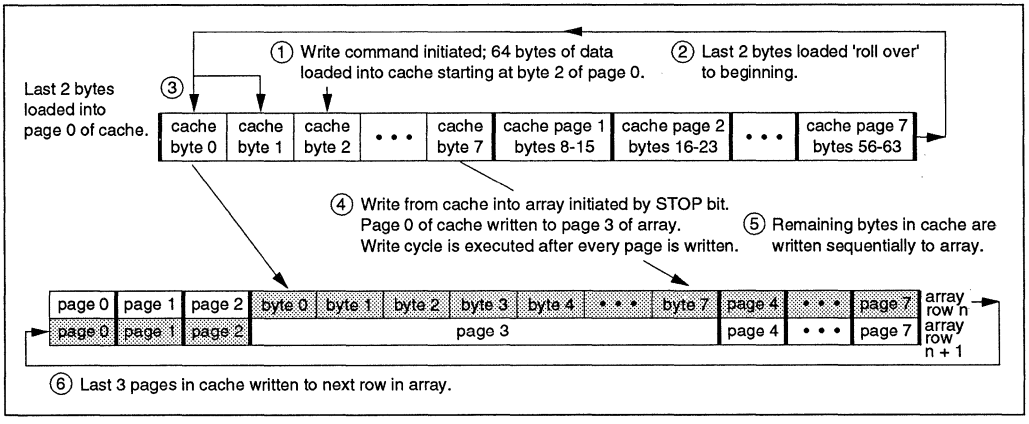


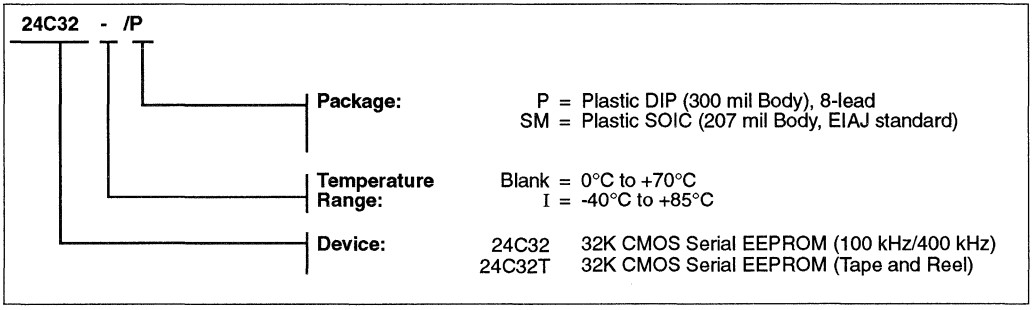
FIGURE 8-2: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY



NOTES

24C32 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

85C72/82/92

1K/2K/4K 5.0V CMOS Serial EEPROM

FEATURES

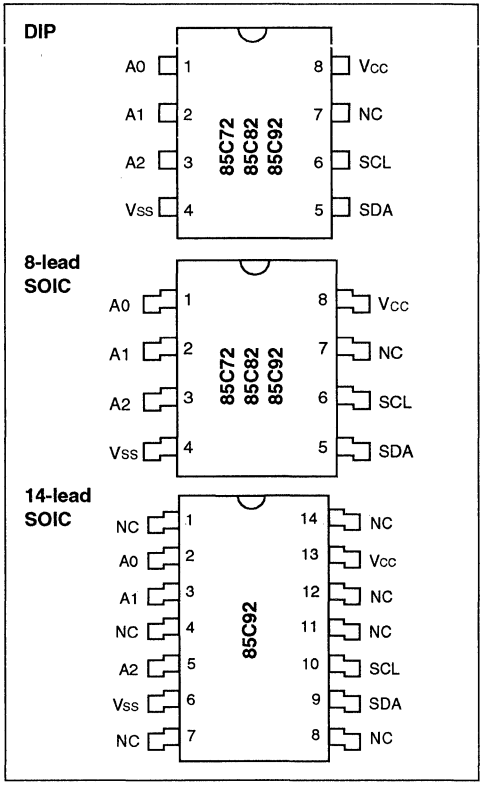
- Low power CMOS technology
- Two wire serial interface bus, I²C™ compatible
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer
- 1ms write cycle time for single byte
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data retention >40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

	85C72	85C82	85C92
Organization	128 x 8	256 x 8	2 x 256 x 8
Page Write Buffer	2 Bytes	2 Bytes	8 Bytes

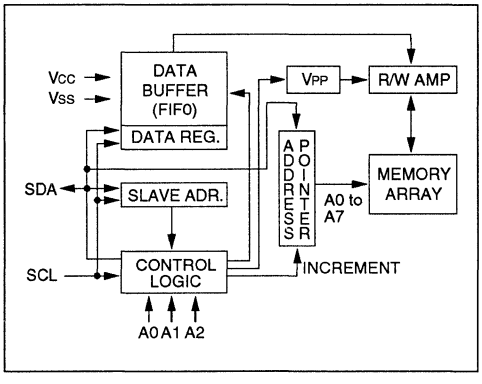
DESCRIPTION

The Microchip Technology Inc. 85C72/82/92 is a 1K/2K/4K bit Electrically Erasable PROM. The device is organized as shown with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C72/82/92 also has a page-write capability for up to 8 bytes of data (see chart). Up to eight 85C72/82/92s may be connected to the two wire bus. The 85C72/82/92 is available in standard 8-pin DIP and surface mount SOIC packages.

PACKAGE TYPE



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V

All inputs and outputs w.r.t. Vss ... -0.6V to Vcc +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
Vss	Ground
SDA	Serial Address/Data Input/Output
SCL	Serial Clock
NC	No Connect
Vcc	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

Vcc = +5V (10%)			Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to 125°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Vcc detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	Vcc x 0.7	Vcc + 1	V	
Low level input voltage	VIL	-0.3	Vcc x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA Only)
A0, A1 & A2 pins:					
HIgh level input voltage	VIH	Vcc - 0.5	Vcc + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI	—	10	µA	VIN = 0V TO Vcc
Output leakage current	ILO	—	10	µA	VOUT = 0V TO Vcc
Internal capacitance (all inputs/outputs)	CINT	—	7.0	pF	VIN/VOUT = 0V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO	—	3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, Vcc = 5V, Tamb = (I) and (E)
read cycle	ICCR	—	750	µA	Vcc = 5V, Tamb = (C), (I) and (E)
Standby current	ICCS	—	100	µA	SDA=SCL=Vcc=5V (no PROGRAM active)

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

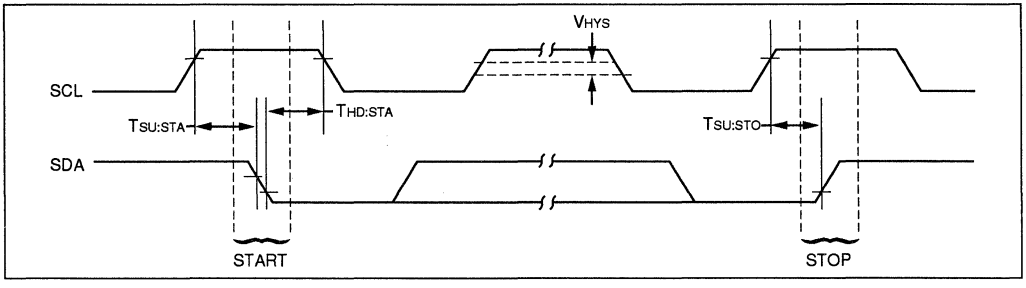
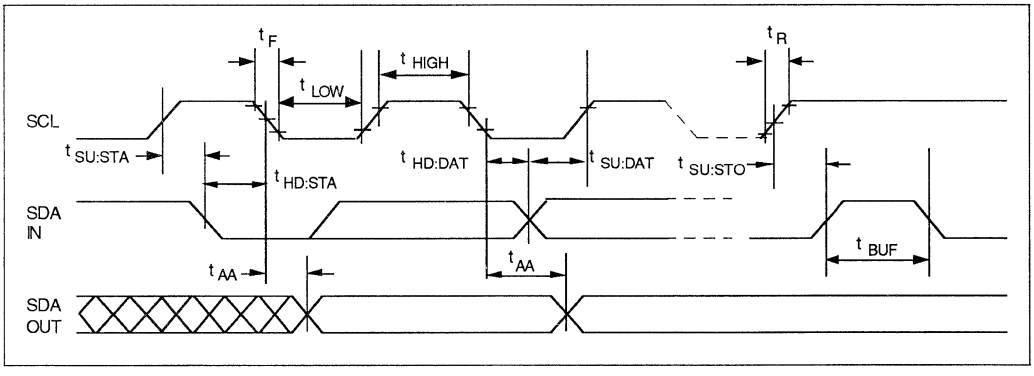


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	THIGH	4000	—	—	ns	
Clock low time	TLOW	4700	—	—	ns	
SDA and SCL rise time	TR	—	—	1000	ns	
SDA and SCL fall time	TF	—	—	300	ns	
START condition hold time	THD:STA	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	—	ns	
Data input setup time	TSU:DAT	250	—	—	ns	
Data output delay time	TPD	300	—	3500	ns	Note 1
STOP condition setup time	TSU:STO	4700	—	—	ns	
Bus free time	TBUF	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI	—	—	100	ns	
Program cycle time	TWC	—	.4 .4N	1 N	ms ms	Byte Mode Page Mode, N = # of bytes to be written

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 85C72/82/92 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C72/82/92 works as slave. Both, master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Up to eight 85C72/82/92s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 85C72/82/92 (refer to section Slave Address).

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

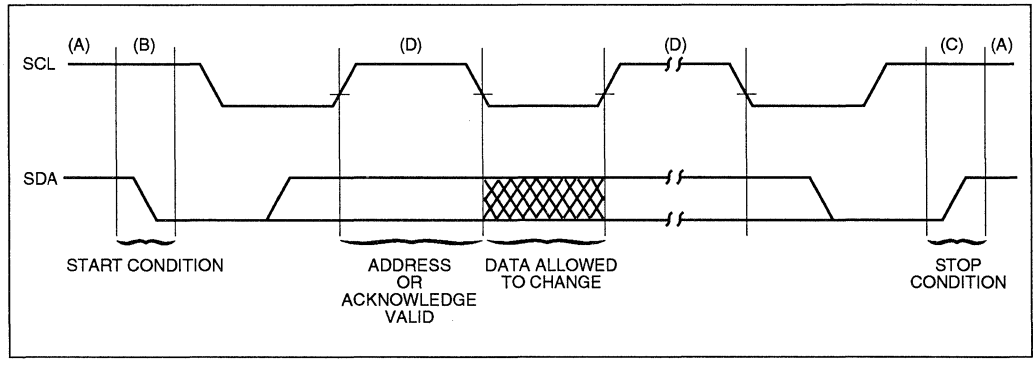
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C72/82/92 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case the slave must leave the data line HIGH to enable the master to generate the STOP condition

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 SLAVE ADDRESS

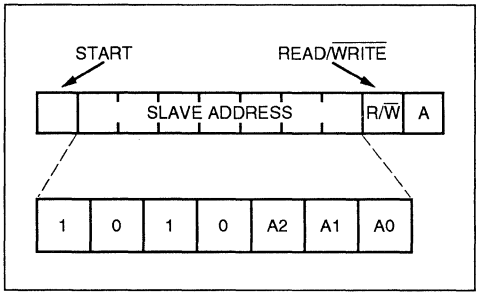
The chip address inputs A0, A1 and A2 of each 85C72/82/92 must be externally connected to either Vcc or ground (Vss), assigning to each 85C72/82/92 a unique 3-bit address. Up to eight 85C72/82/92s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 85C72/82/92.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C72/82/92, followed by the chip address bits A0, A1 and A2. In the 85C92 the seventh bit of that byte (BA) is used to select the upper block (addresses 100 - 1FF) or the lower block (000 - FFF) of the array.

The eighth bit of slave address determines if the master device wants to read or write to the 85C72/82/92 (see Figure 4-1).

The 85C72/82/92 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 4-1: SLAVE ADDRESS ALLOCATION



5.0 BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 85C72/82/92.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C72/82/92 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C72/82/92. After receiving the acknowledge of the 85C72/82/92, the master device transmits the data word to be written into the addressed memory location. The 85C72/82/92 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C72/82/92 (see Figure 6-1).

6.0 PAGE PROGRAM MODE

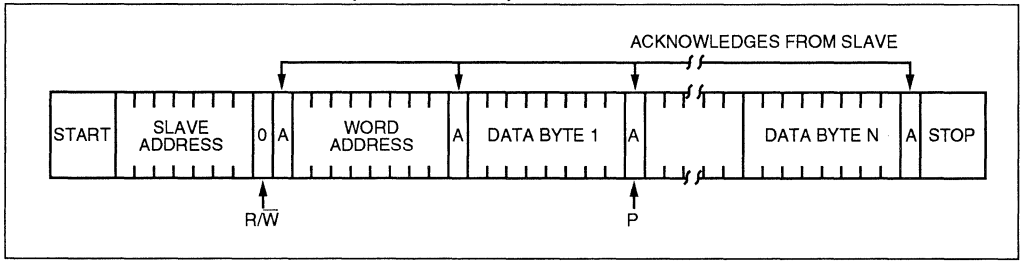
To program the 85C72/82/92, the master sends addresses and data to the 85C72/82/92 which is the slave (see Figure 6-1). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C72/82/92, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 85C72/82/92 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a stop condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C72/82/92 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 6-1), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

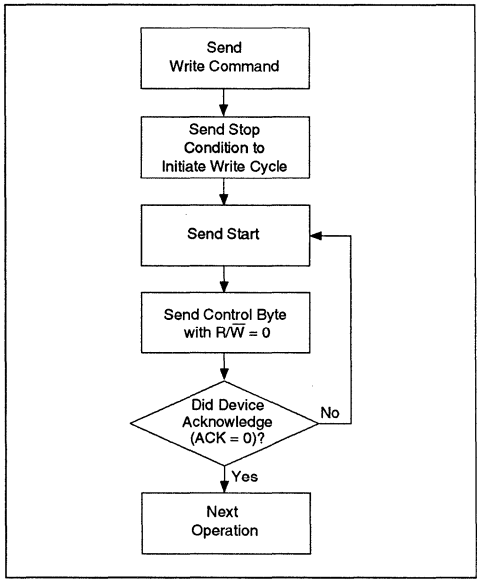
FIGURE 6-1: PROGRAM MODE (ERASE/WRITE)



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ MODE

This mode illustrates master device reading data from the 85C72/82/92.

As can be seen from Figure 8-1, the master first sets up the slave and word addresses by doing a write.

Note: Although this is a read mode, the address pointer must be written to.

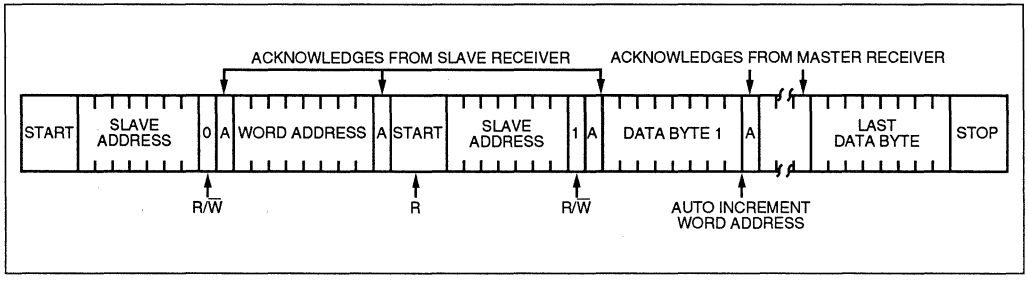
During this period the 85C72/82/92 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note 1: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 8-1 and save time transmitting the slave and word addresses.

Note 2: In all modes, the address pointer will automatically increment from the end of the memory block (256 byte) back to the first location in that block.

FIGURE 8-1: READ MODE



9.0 PIN DESCRIPTION

9.1 A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. For 85C92, A0 is no function.

Up to eight 85C72/82s or four 85C92s can be connected to the bus.

These inputs must be connected to either VSS or VCC.

9.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KW). For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

9.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.4 NC No Connect

This pin can be left open or used as a tie point.

Note 1: A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C72/82 page is 2 bytes long and the 85C92 page is 8 bytes long.

Note 2: A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will, however, wrap around from the end of a block to the first location in the same block. The 85C72/82 has only one block (256 bytes), while the 85C92 has two blocks of 256 bytes each.

85C72/82/92 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

85C82 - /P

Package:	J =	CERDIP (300 mil Body), 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead
	SM =	Plastic SOIC (207 mil Body), 8-lead
	SL =	Plastic SOIC 14-lead (85C92 only)
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
	E =	-40°C to +125°C

Device:	85C72	1K CMOS Serial EEPROM
	85C72T	1K CMOS Serial EEPROM (Tape and Reel)
	85C82	2K CMOS Serial EEPROM
	85C82	2K CMOS Serial EEPROM (Tape and Reel)
	85C92	4K CMOS Serial EEPROM
	85C92T	4K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

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1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
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MICROCHIP

SECTION 4
MICROWIRE™ SERIAL EEPROM PRODUCT SPECIFICATIONS

4

93AA46/56/66	1K/2K/4K 1.8V CMOS Serial EEPROM	4-1
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93AA46/56/66

1K/2K/4K 1.8V CMOS Serial EEPROM

FEATURES

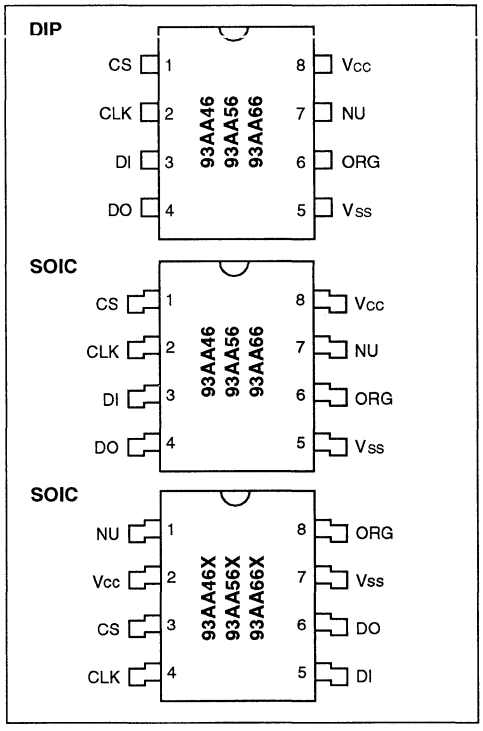
- Single supply with programming operation down to 1.8V
- Low power CMOS technology
  - 70 µA typical active READ current at 1.8V
  - 2 µA typical standby current at 1.8V
- ORG pin selectable memory configuration
  - 128 x 8 or 64 x 16 bit organization (93AA46)
  - 256 x 8 or 128 x 16 bit organization (93AA56)
  - 512 x 8 or 256 x 16 bit organization (93AA66)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- **10,000,000 ERASE/WRITE cycles guaranteed on 93AA56 and 93AA66**
- **1,000,000 E/W cycles guaranteed on 93AA46***
- Data retention > 40 years
- 8-pin PDIP/SOIC (SOIC in JEDEC and EIAJ standards)

DESCRIPTION

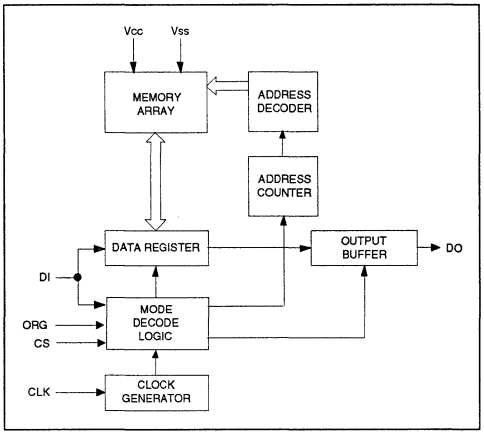
The Microchip Technology Inc. 93AA46/56/66 are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93AA Series is available in standard 8-pin DIP and surface mount SOIC packages. The rotated pin-out 93AA46X/56X/66X are offered in the "SN" package only.

*Future: 10,000,000 cycles guaranteed

PACKAGE TYPE



BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings

VCC 7.0V
All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
ORG	Memory Configuration
NU	Not Utilized
VCC	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

			VCC = +1.8V to +5.5V		Commercial (C): Tamb = 0°C to +70°C	
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
High level input voltage	VIH1	2.0	—	VCC+1	V	VCC ≥ 2.5V
	VIH2	0.7 VCC	—	VCC+1	V	VCC < 2.5V
Low level input voltage	VIL1	-0.3	—	0.8	V	VCC ≥ 2.5V
	VIL2	-0.3	—	0.2 VCC	V	VCC < 2.5V
Low level output voltage	VOL1	—	—	0.4	V	IOL = 2.1 mA; VCC = 4.5V
	VOL2	—	—	0.2	V	IOL = 100µA; VCC = 1.8V
High level output voltage	VOH1	2.4	—	—	V	IOH = -400 µA; VCC = 4.5V
	VOH2	VCC-0.2	—	—	V	IOH = -100 µA; VCC = 1.8V
Input leakage current	ILI	-10	—	10	µA	VIN = 0.1V to VCC
Output leakage current	ILO	-10	—	10	µA	VOUT = 0.1V to VCC
Intenal capacitance (all inputs/outputs)	CINT	—	—	7	pF	VIN/VOUT = 0V (Note 1 & 2) Tamb = +25°C, FCLK = 1 MHz
Operating current	ICC write	—	—	3	mA	FCLK=2 MHz; VCC=5.5V (Note 2)
	ICC read	—	—	1	mA	FCLK = 2 MHz; VCC = 5.5V
				500	µA	FCLK = 1 MHz; VCC = 3.0V
			70		µA	FCLK = 1 MHz; VCC = 1.8V
Standby current	ICCS			100	µA	CLK = CS = 0V; VCC = 5.5V
				30	µA	CLK = CS = 0V; VCC = 3.0V
			2		µA	CLK = CS = 0V; VCC = 1.8V
Clock frequency	FCLK				MHz	VCC ≥ 4.5V
				2	MHz	VCC < 4.5V
Clock high time	TCKH	250		1	ns	
Clock low time	TCKL	250			ns	
Chip select setup time	TCSS	50			ns	Relative to CLK
Chip select hold time	TCSH	0			ns	Relative to CLK
Chip select low time	TCSL	250			ns	
Data input setup time	TDIS	100			ns	Relative to CLK
Data input hold time	TDIH	100			ns	Relative to CLK
Data output delay time	TPD			400	ns	CL = 100 pF
Data output disable time	TCZ			100	ns	CL = 100 pF (Note 2)
Status valid time	TSV			500	ns	CL = 100 pF
Program cycle time	TWC		4	10	ms	ERASE/WRITE mode
	TEC		8	15	ms	ERAL mode (Vcc = 5V ± 10%)
	TWL		16	30	ms	WRAL mode (Vcc = 5V ± 10%)

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
Note 2: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: INSTRUCTION SET FOR 93AA46: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	9
ERAL	1	00	1 0 X X X X	—	(RDY/BSY)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/BSY)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

TABLE 1-4: INSTRUCTION SET FOR 93AA46: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	10
ERAL	1	00	1 0 X X X X X	—	(RDY/BSY)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/BSY)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

TABLE 1-5: INSTRUCTION SET FOR 93AA56: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	11
ERAL	1	00	1 0 X X X X X	—	(RDY/BSY)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-6: INSTRUCTION SET FOR 93AA56: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/BSY)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

TABLE 1-7: INSTRUCTION SET FOR 93AA66: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/BSY)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/BSY)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/BSY)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-8: INSTRUCTION SET FOR 93AA66: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/BSY)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/BSY)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/BSY)	20
WRAL	1	00	0 1 X X X X X X X	D7 - D0	(RDY/BSY)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

3.0 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

4.0 ERASE/WRITE ENABLE AND DISABLE

The 93AA46/56/66 power up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

5.0 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word typical.

6.0 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word typical.

7.0 ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at 5V ± 10%.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete.

The ERAL cycle takes (8 ms typical).

8.0 WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at 5V ± 10%.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 16 ms typical.

9.0 PIN DESCRIPTION

9.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

9.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93AAXX. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

9.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

9.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

9.5 Organization (ORG)

When ORG is connected to VCC, the (x16) memory organization is selected. When ORG is tied to VSS, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1MHz or less for the (x16) memory organization. For clock speeds greater than 1 MHz, ORG must be tied to VCC or VSS.

FIGURE 9-1: SYNCHRONOUS DATA TIMING

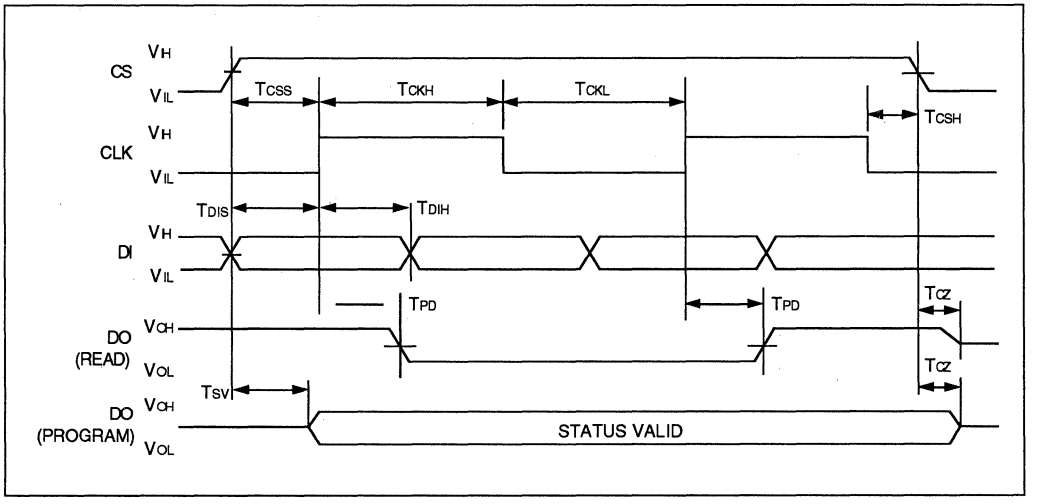
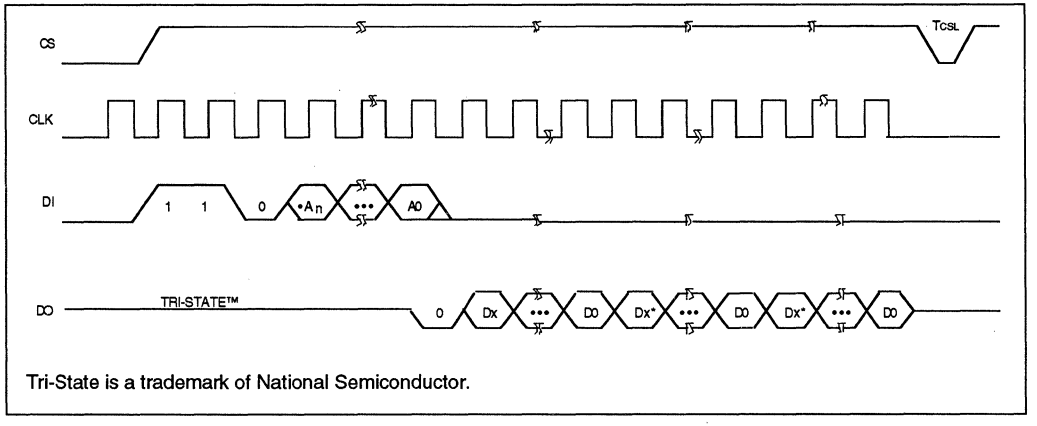


FIGURE 9-2: READ TIMING



Tri-State is a trademark of National Semiconductor.

FIGURE 9-3: EWEN TIMING

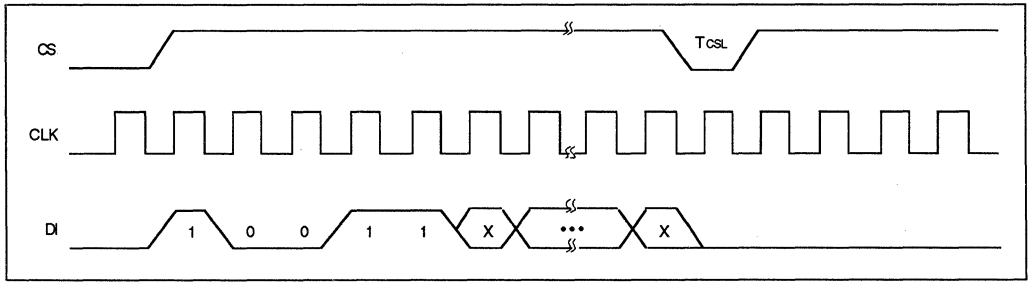


FIGURE 9-4: EWDS TIMING

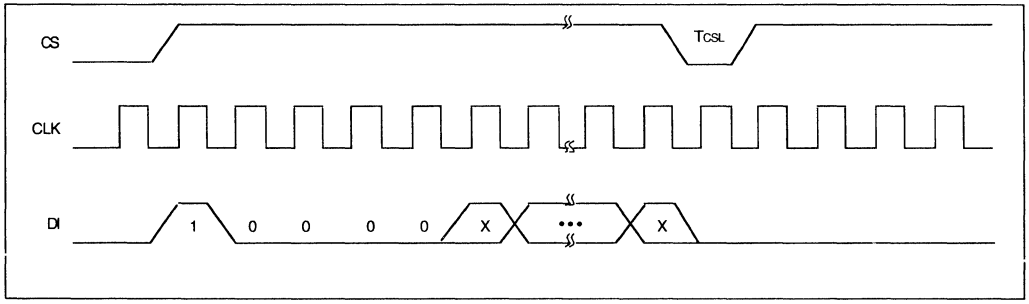


FIGURE 9-5: WRITE TIMING

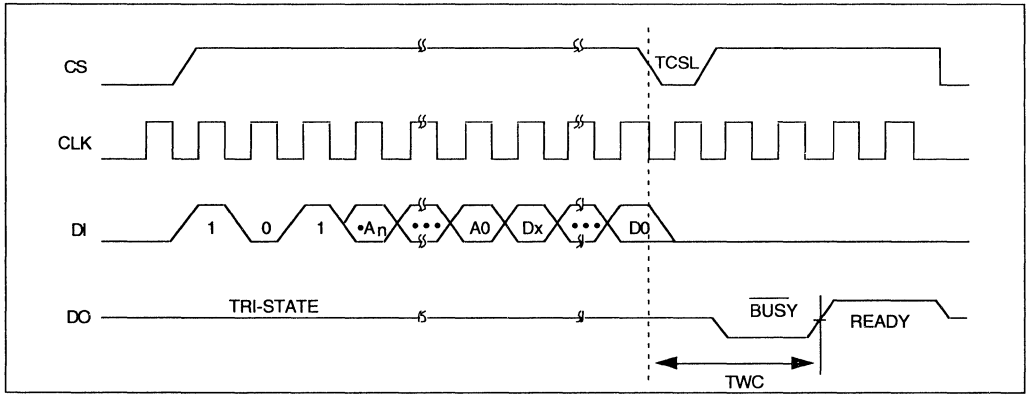


FIGURE 9-6: WRAL TIMING

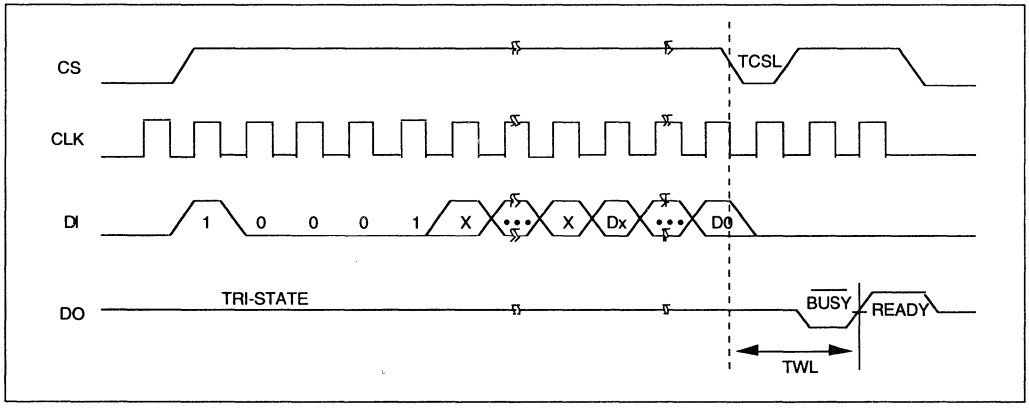


FIGURE 9-7: ERASE TIMING

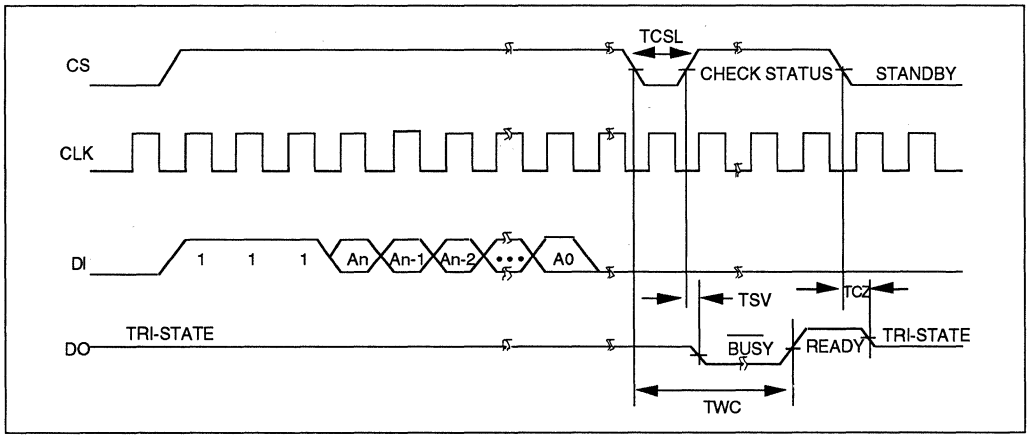
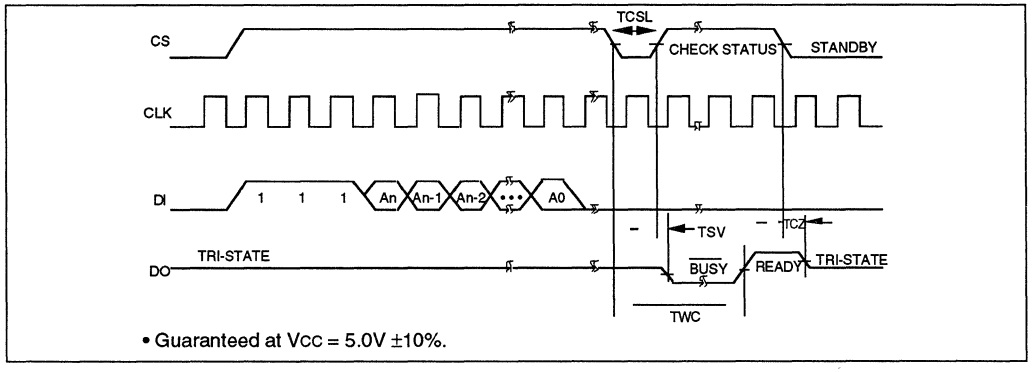


FIGURE 9-8: ERAL TIMING



• Guaranteed at V_{CC} = 5.0V ±10%.

NOTES

93AA46/56/66 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93AA46/56/66 - /P

Package:

P = Plastic DIP (300 mil Body), 8-lead
SN = Plastic SOIC (150 mil Body), 8-lead
SM = Plastic SOIC (207 mil Body), 8-lead (93AA46/56/66)

Temperature Range:

Blank = 0°C to +70°C

Device:

(x16) or (x8)	Configuration
93AA46/56/66	CMOS Serial EEPROM
93AA46/56/66X	CMOS Serial EEPROM in alternate pinouts (SN package only)
93AA46T/56T/66T	CMOS Serial EEPROM (Tape and Reel)
93AA46XT/56XT/66XT	CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

93LC46/56/66

1K/2K/4K 2.0V CMOS Serial EEPROM

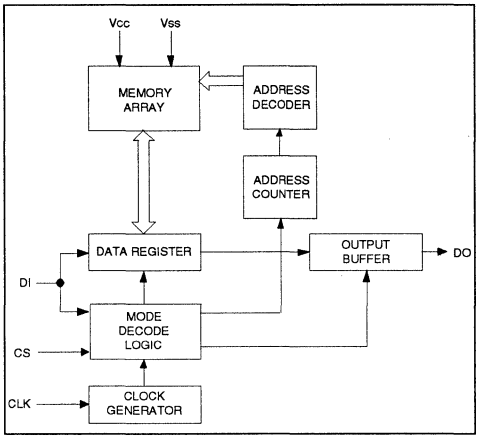
FEATURES

- Single supply with programming operation down to 2.0V (Commercial only)
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current (typical) at 3.0V
- ORG pin selectable memory configuration
  - 128 x 8 or 64 x 16 bit organization (93LC46)
  - 256 x 8 or 128 x 16 bit organization (93LC56)
  - 512 x 8 or 256 x 16 bit organization (93LC66)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- **10,000,000 ERASE/WRITE cycles guaranteed on 93LC56 and 93LC66**
- **1,000,000 E/W cycles guaranteed on 93LC46***
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC package (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - Commercial: 0°Cto +70°C
  - Industrial: -40°C to +85°C

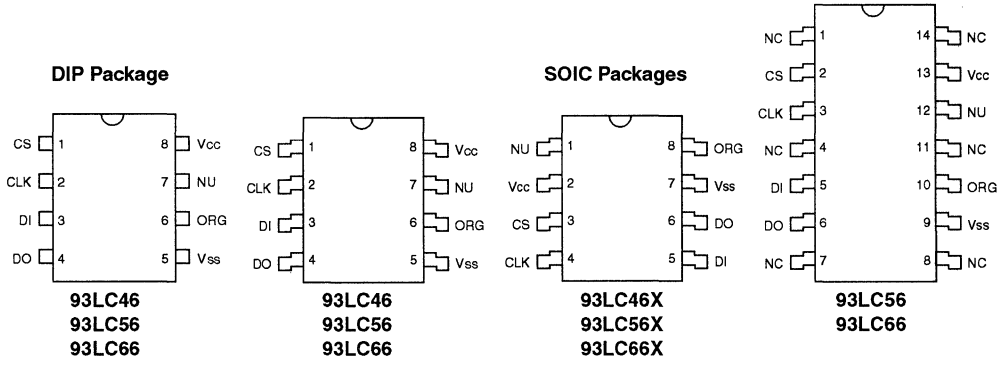
DESCRIPTION

The Microchip Technology Inc. 93LC46/56/66 are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x8 or x16 bits depending on the ORG pin setup. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93LC Series is available in standard 8-pin DIP and 8/14-pin surface mount SOIC packages. The 93LC46X/56X/66X are offered in "SN" package only.

BLOCK DIAGRAM



PACKAGE TYPE



**Future: 10,000,000 E/W cycles guaranteed

1.0 ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss ....-0.6V to Vcc +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Configuration
NU	Not Utilized
NC	No Connect
Vcc	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

	Commercial Vcc = +2.0V to +6.0V (C): Tamb = 0°C to +70°C Industrial Vcc = +2.5V to +6.0V (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
High level input voltage	VIH1	2.0	Vcc +1	V	Vcc ≥ 2.5V
	VIH2	0.7 Vcc	Vcc +1	V	Vcc < 2.5V
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.5V
	VIL2	-0.3	0.2 Vcc	V	Vcc < 2.5V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL =100 µA; Vcc = Vcc Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100 µA; Vcc = Vcc Min.
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	7	pF	VIN/VOUT = 0 V (Note 1 & 3) Tamb = +25°C, FCLK = 1 MHz
Operating current	Icc write	—	3	mA	FCLK = 2 MHz; Vcc = 6.0V (Note 3)
	Icc read	—	1 500	mA µA	FCLK = 2 MHz; Vcc = 6.0V FCLK = 1 MHz; Vcc = 3.0V
Standby current	Iccs	—	100 30	µA µA	CLK = CS = 0V; Vcc = 6.0V CLK = CS = 0V; Vcc = 3.0V
Clock frequency	FCLK	—	2 1	MHz MHz	Vcc ≥ 4.5V Vcc < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF (Note 3)
Status valid time	TSV	—	500	ns	CL = 100 pF
Program cycle time	TWC	—	10	ms	ERASE/WRITE mode (Note 2)
	TEC	—	15	ms	ERAL mode
	TWL	—	30	ms	WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
Note 2: Typical program cycle time is 4 ms per word.
Note 3: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: INSTRUCTION SET FOR 93LC46: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	9
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{BSY}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/$\overline{BSY}$)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

TABLE 1-4: INSTRUCTION SET FOR 93LC46: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	18
EWEN	1	00	1 1 X X X X X	—	High-Z	10
ERASE	1	11	A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	10
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{BSY}$)	10
WRITE	1	01	A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	18
WRAL	1	00	0 1 X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	18
EWDS	1	00	0 0 X X X X X	—	High-Z	10

TABLE 1-5: INSTRUCTION SET FOR 93LC56: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X	—	High-Z	11

TABLE 1-6: INSTRUCTION SET FOR 93LC56: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

TABLE 1-7: INSTRUCTION SET FOR 93LC66: ORG = 1 (X 16 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X	—	High-Z	11

TABLE 1-8: INSTRUCTION SET FOR 93LC66: ORG = 0 (X 8 ORGANIZATION)

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X	D7 - D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X	—	High-Z	12

4

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the READY/$\overline{\text{BUSY}}$ status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

3.0 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

4.0 ERASE/WRITE ENABLE AND DISABLE

The 93LC46/56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

5.0 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word (Typical).

6.0 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word (Typical).

7.0 ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete.

The ERAL cycle takes 15 ms maximum (8 ms typical).

8.0 WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at Vcc = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 30 ms maximum (16 ms typical).

9.0 PIN DESCRIPTION

9.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

9.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LCXX. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

9.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

9.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

9.5 Organization (ORG)

When ORG is connected to Vcc or floated, the (x16) memory organization is selected. When ORG is tied to VSS, the (x8) memory organization is selected. ORG can only be floated for clock speeds of 1 MHz or less for the (X16) memory organization. For clock speeds greater than 1 MHz, ORG must be tied to Vcc or VSS.

FIGURE 9-1: SYNCHRONOUS DATA TIMING

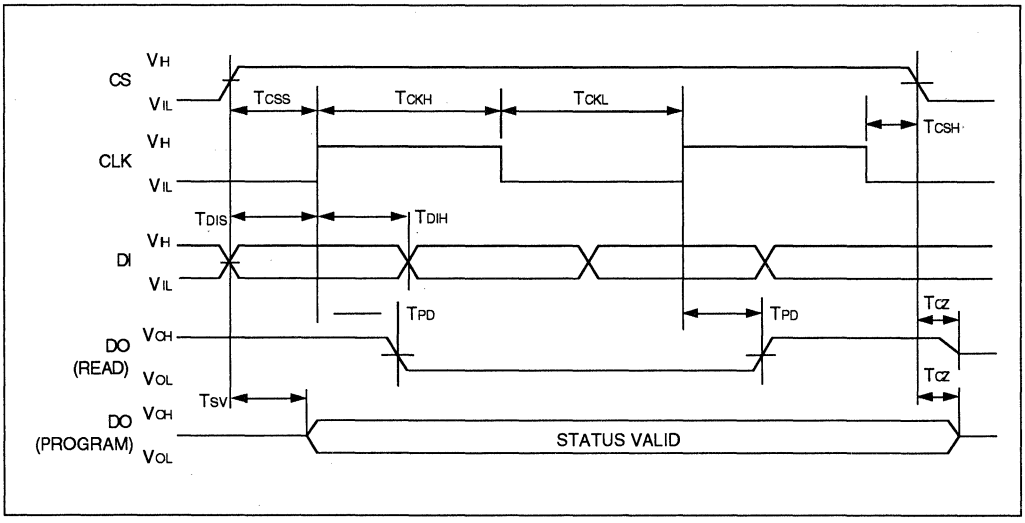


FIGURE 9-2: READ TIMING

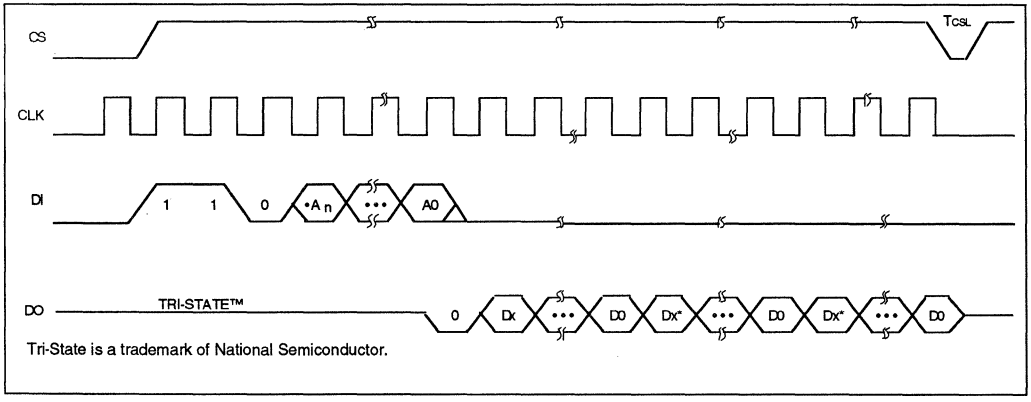


FIGURE 9-3: EWEN TIMING

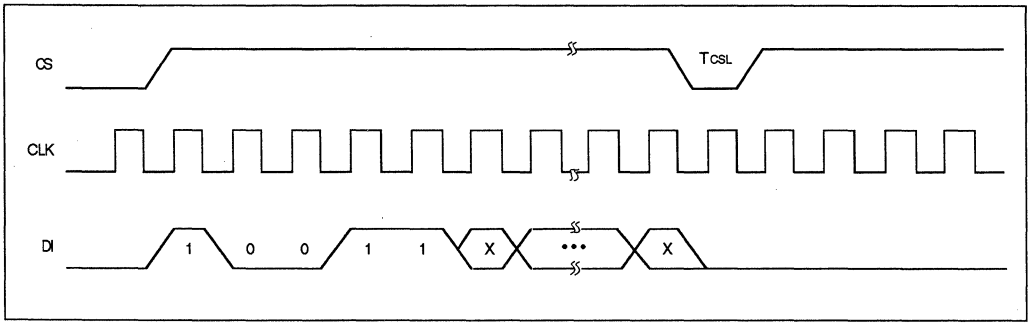


FIGURE 9-4: EWDS TIMING

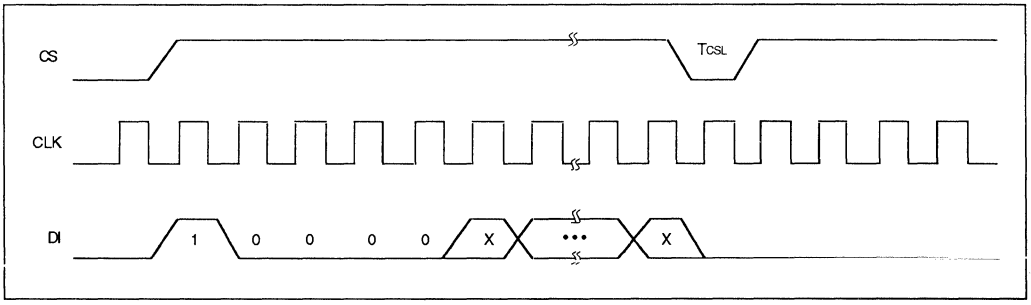


FIGURE 9-5: WRITE TIMING

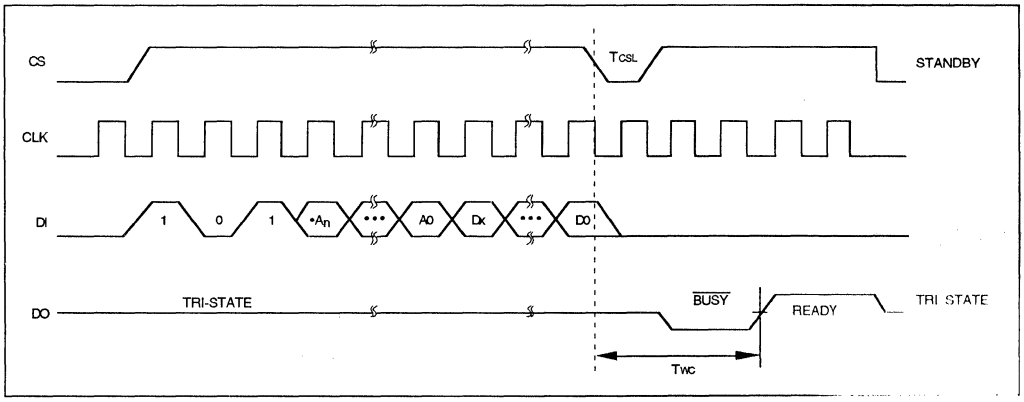
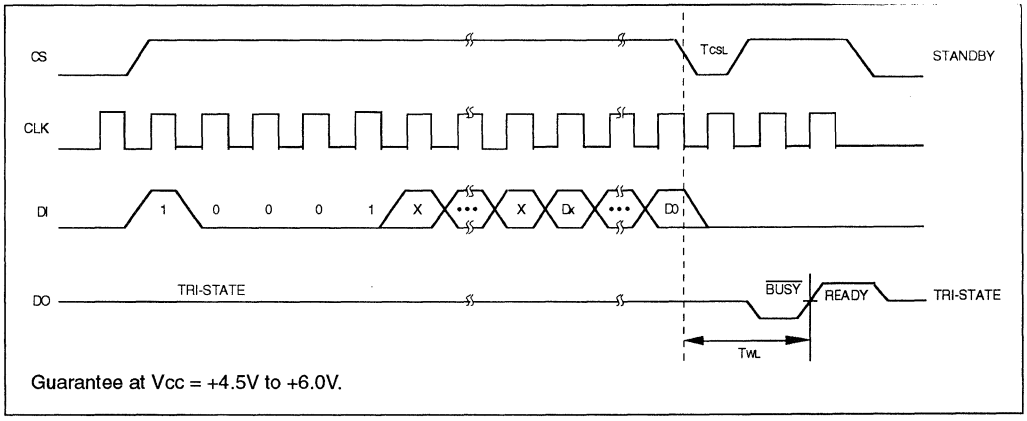


FIGURE 9-6: WRAL TIMING



Guarantee at Vcc = +4.5V to +6.0V.

4

FIGURE 9-7: ERASE TIMING

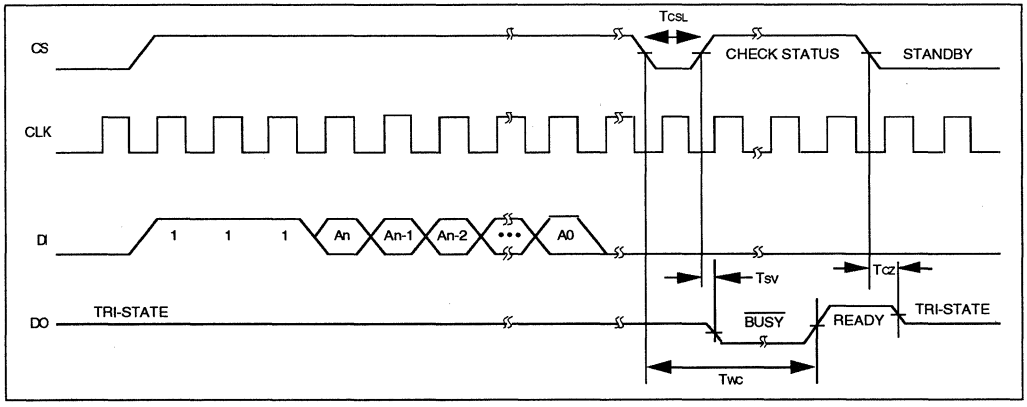
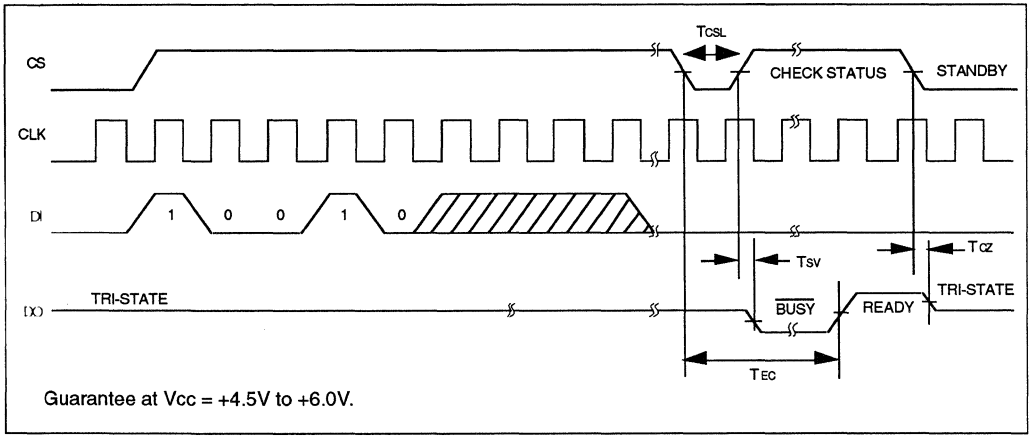


FIGURE 9-8: ERAL TIMING



Guarantee at Vcc = +4.5V to +6.0V.

NOTES

93LC46/56/66 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93LC46/56/66 - /P

Package:
- P = Plastic DIP (300 mil Body), 8-lead
- SN = Plastic SOIC (150 mil Body), 8-lead
- SM = Plastic SOIC (207 mil Body), 8-lead
- SL = Plastic SOIC (150 mil Body), 14-lead

Temperature Range:
- Blank = 0°C to +70°C
- I = -40°C to +85°C

Device:

	Configuration
93LC46/56/66	CMOS Serial EEPROM
93LC56/X/66X	CMOS Serial EEPROM in alternate pinouts (SN package only)
93LC46T/56T/66T	CMOS Serial EEPROM (Tape and Reel)
93LC56XT/66XT	CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

93LC46B/56B/66B

1K/2K/4K 2.0V CMOS Serial EEPROM

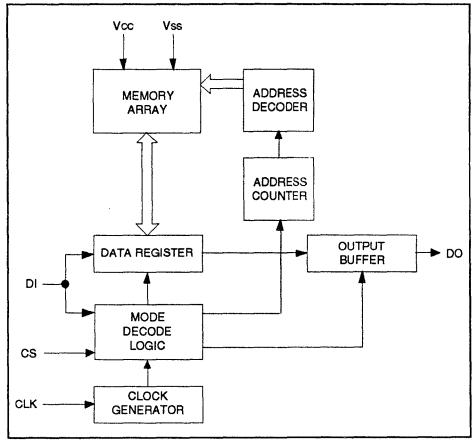
FEATURES

- Single supply with programming operation down to 2.0V (Commercial only)
- Low power CMOS technology
  - 1 mA active current typical
  - 5 μA standby current (typical) at 3.0V
- x16 bit organization
- 64x16 (93LC46B)
- 128x16 (93LC56B)
- 256x16 (93LC66B)
- Self-timed ERASE and WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- **10,000,000 ERASE/WRITE cycles guaranteed on 93LC56B and 93LC66B**
- **1,000,000 E/W cycles guaranteed on 93LC46B***
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC package (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

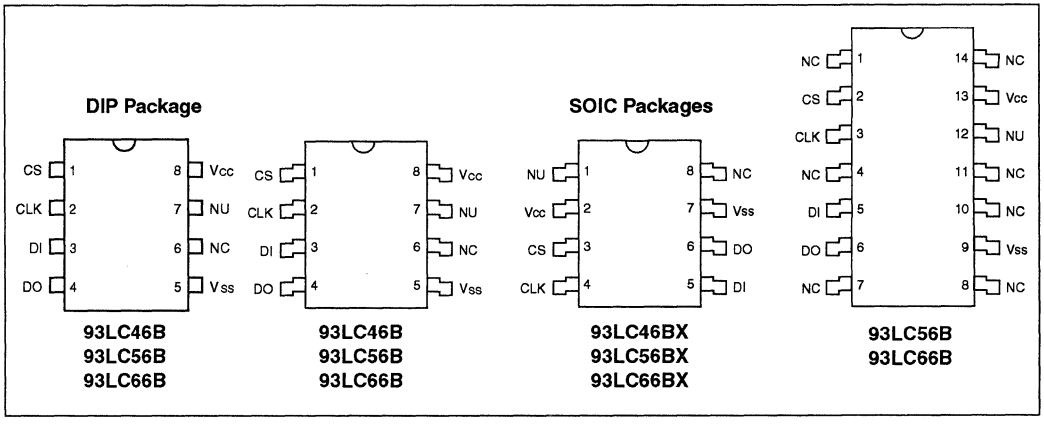
DESCRIPTION

The Microchip Technology Inc. 93LC46B/56B/66B are 1K, 2K and 4K low voltage serial Electrically Erasable PROMs. The device memory is configured as x16. Advanced CMOS technology makes these devices ideal for low power non-volatile memory applications. The 93LC Series is available in standard 8-pin DIP and 8/14-pin surface mount SOIC packages.

BLOCK DIAGRAM



PACKAGE TYPE



**Future: 10,000,000 E/W cycles guaranteed

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss ... -0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
NC	No Connect
NU	Not Utilized
Vcc	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

	Commercial Industrial	(C): Vcc = +2.0V to +6.0V (I): Vcc = +2.5V to +6.0V			(C): Tamb = 0°C to +70°C (I): Tamb = -40°C to +85°C
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
High level input voltage	VIH1	2.0	Vcc + 1	V	Vcc ≥ 2.5V
	VIH2	0.7 Vcc	Vcc + 1	V	Vcc < 2.5V
Low level input voltage	VIL1	-0.3	0.8	V	Vcc ≥ 2.5V
	VIL2	-0.3	0.2 Vcc	V	Vcc < 2.5V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; Vcc = 4.5V
	VOL2	—	0.2	V	IOL = 100 µA; Vcc = Vcc Min.
High level output voltage	VOH1	2.4	—	V	IOH = -400 µA; Vcc = 4.5V
	VOH2	Vcc-0.2	—	V	IOH = -100 µA; Vcc = Vcc Min.
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = 0.1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	7	pF	VIN/VOUT = 0 V (Note 1 & 3) Tamb = +25°C, FCLK = 1 MHz
Operating current	Icc write	—	3	mA	FCLK = 2 MHz; Vcc = 6.0V (Note 3)
	Icc read	—	1 500	mA µA	FCLK = 2 MHz; Vcc = 6.0V FCLK = 1 MHz; Vcc = 3.0V
Standby current	Iccs	—	100 30	µA µA	CLK = CS = 0V; Vcc = 6.0V CLK = CS = 0V; Vcc = 3.0V
Clock frequency	FCLK	—	2 1	MHz MHz	Vcc ≥ 4.5V Vcc < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	Tcss	500	—	ns	Relative to CLK
Chip select hold time	Tcsh	0	—	ns	Relative to CLK
Chip select low time	Tcsl	250	—	ns	
Data input setup time	Tdis	100	—	ns	Relative to CLK
Data input hold time	Tdih	100	—	ns	Relative to CLK
Data output delay time	Tpd	—	400	ns	CL= 100 pF
Data output disable time	Tcz	—	100	ns	CL = 100 pF (Note 3)
Status valid time	Tsv	—	500	ns	CL= 100 pF
Program cycle time	Twc	—	10	ms	ERASE/WRITE mode (Note 2)
	Tec	—	15	ms	ERAL mode
	Twl	—	30	ms	WRAL mode

Note 1: This parameter is tested at tamb = 25°C and FCLK = 1 MHz.
Note 2: Typical program cycle time is 4 ms per word.
Note 3: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: INSTRUCTION SET FOR 93LC46B

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
EWEN	1	00	1 1 X X X X	—	High-Z	9
ERASE	1	11	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	9
ERAL	1	00	1 0 X X X X	—	(RDY/$\overline{BSY}$)	9
WRITE	1	01	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	25
WRAL	1	00	0 1 X X X X	D15 - D0	(RDY/$\overline{BSY}$)	25
EWDS	1	00	0 0 X X X X	—	High-Z	9

TABLE 1-4: INSTRUCTION SET FOR 93LC56B

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

TABLE 1-5: INSTRUCTION SET FOR 93LC66B

Instruction	SB	Opcode	Address	Data In	Data Out	Req. CLK Cycles
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

4

2.0 FUNCTIONAL DESCRIPTION

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until V_{CC} has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when V_{CC} has fallen below 1.4V at nominal conditions.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

3.0 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (T_{PD}). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

4.0 ERASE/WRITE ENABLE AND DISABLE

The 93LC46B/56B/66B powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or V_{CC} is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

5.0 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 4 ms per word (Typical).

6.0 WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 4 ms per word (Typical).

7.0 ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at VCC = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete.

The ERAL cycle takes 15 ms maximum (8 ms typical).

8.0 WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at VCC = +4.5V to +6.0V.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 30 ms maximum (16 ms typical).

9.0 PIN DESCRIPTION

9.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

9.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LCXXB. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

9.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

9.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

FIGURE 9-1: SYNCHRONOUS DATA TIMING

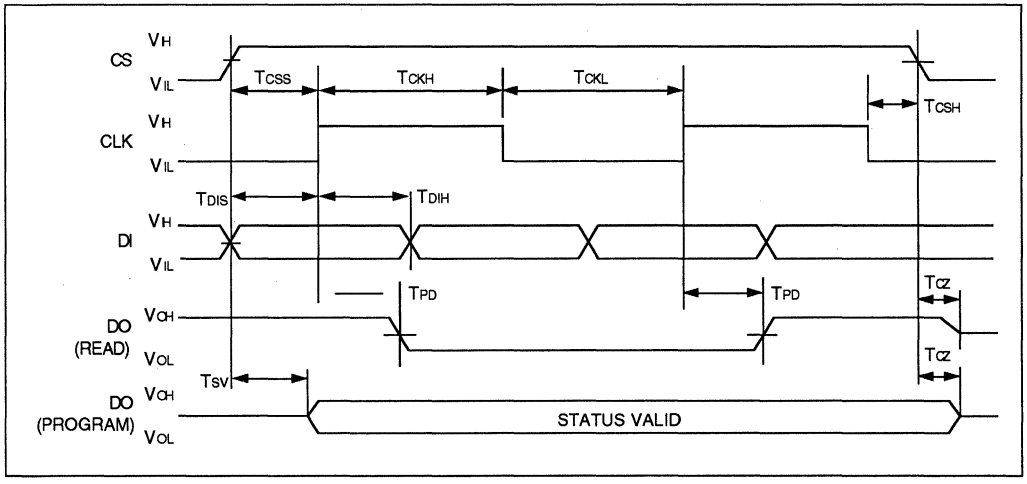


FIGURE 9-2: READ TIMING

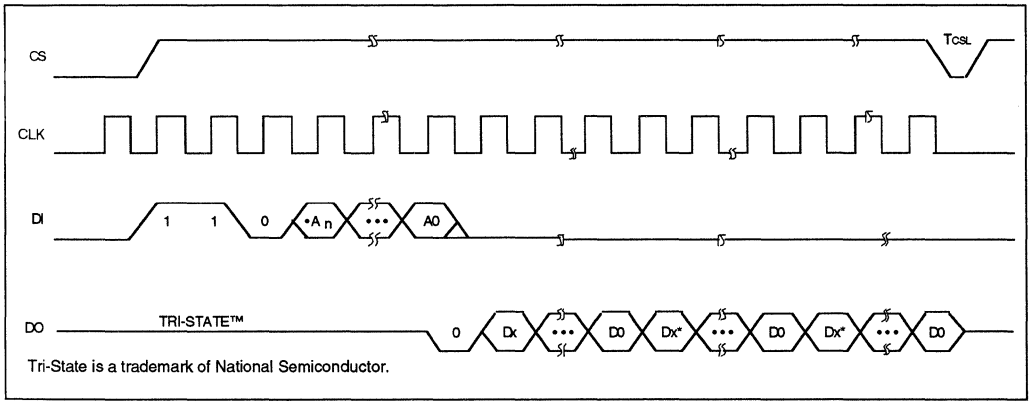


FIGURE 9-3: EWEN TIMING

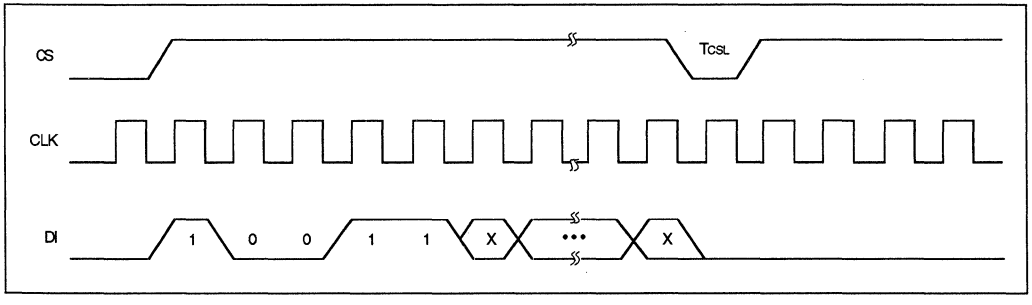


FIGURE 9-4: EWDS TIMING

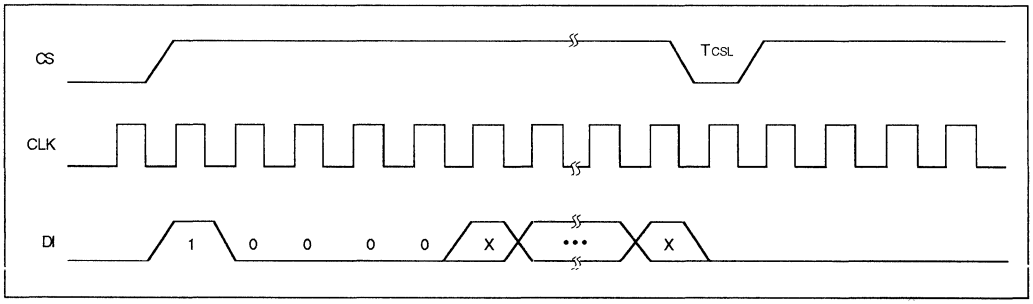


FIGURE 9-5: WRITE TIMING

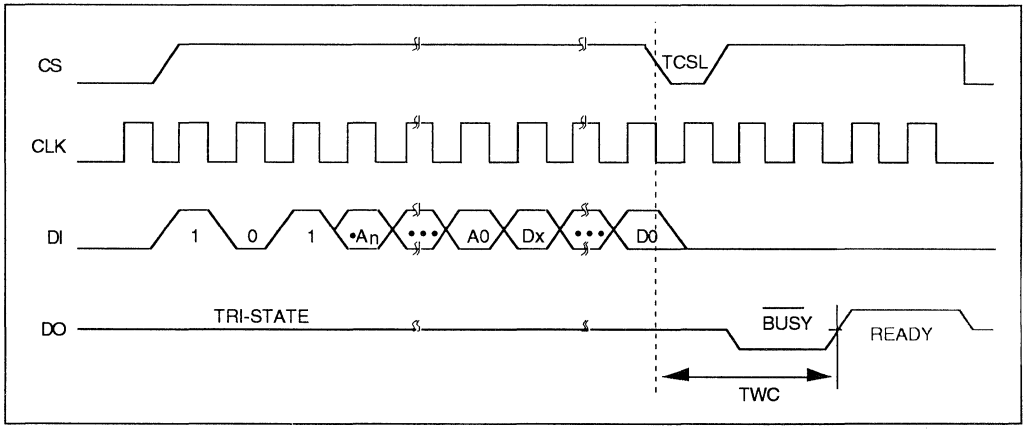
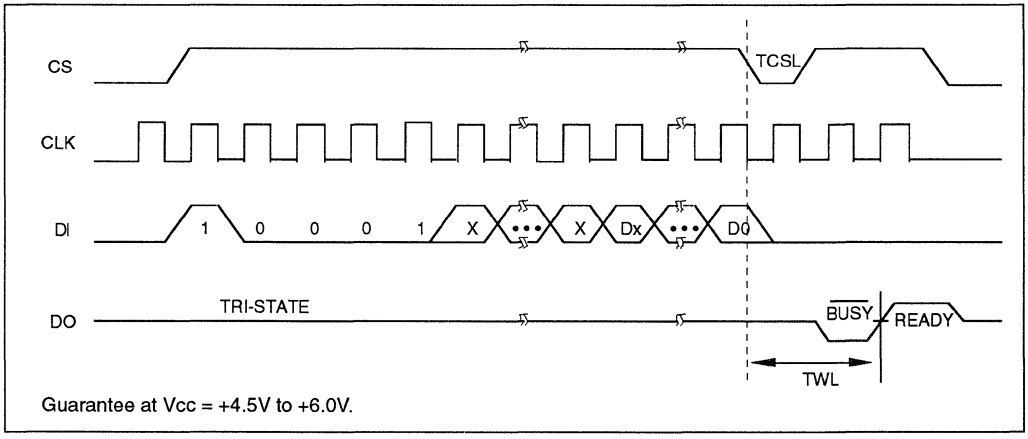


FIGURE 9-6: WRAL TIMING



Guarantee at Vcc = +4.5V to +6.0V.

FIGURE 9-7: ERASE TIMING

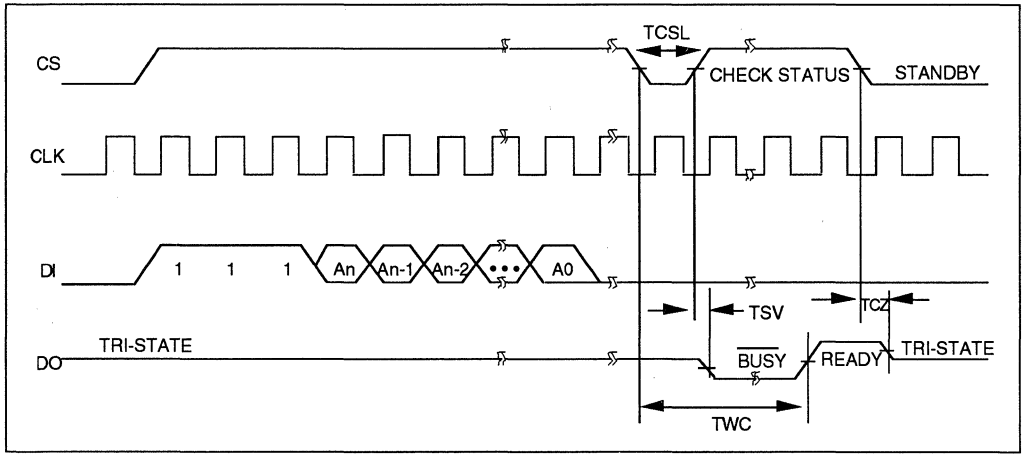
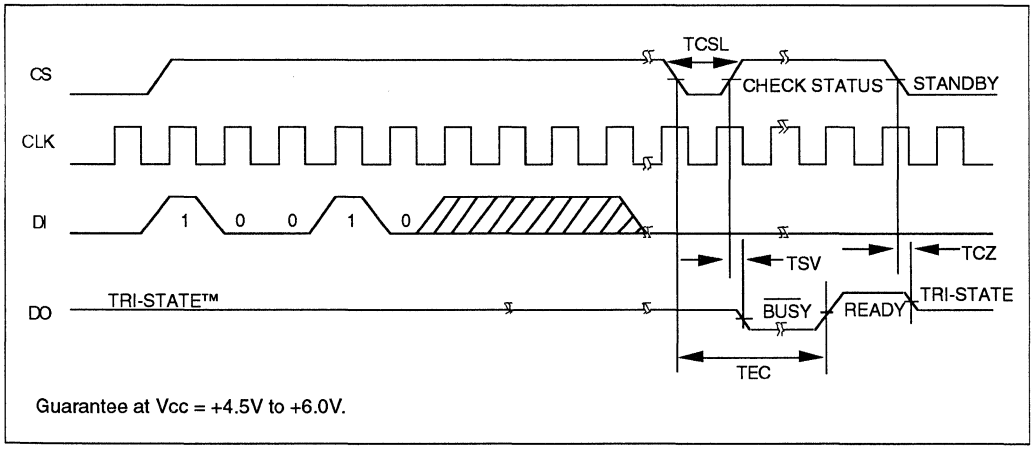


FIGURE 9-8: ERAL TIMING



Guarantee at Vcc = +4.5V to +6.0V.

NOTES

93LC46B/56B/66B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93LC46B/56B/66B - /P

Package:
P = Plastic DIP (300 mil Body), 8-lead
SN = Plastic SOIC (150 mil Body), 8-lead
SM = Plastic SOIC (207 mil Body), 8-lead
SL = Plastic SOIC (150 mil Body), 14-lead (93LC56B/93LC66B)

Temperature Range:
Blank = 0°C to +70°C
I = -40°C to +85°C

Device:

	Configuration
93LC46B/56B/66B	CMOS Serial EEPROM
93LC46BX/56BX/66BX	CMOS Serial EEPROM in alternate pinouts (SN package only)
93LC46BT/56BT/66BT	CMOS Serial EEPROM (Tape and Reel)
93LC46BXT/56BXT/66BXT	CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

93C06/46

256 Bit/1K 5.0V CMOS Serial EEPROM

FEATURES

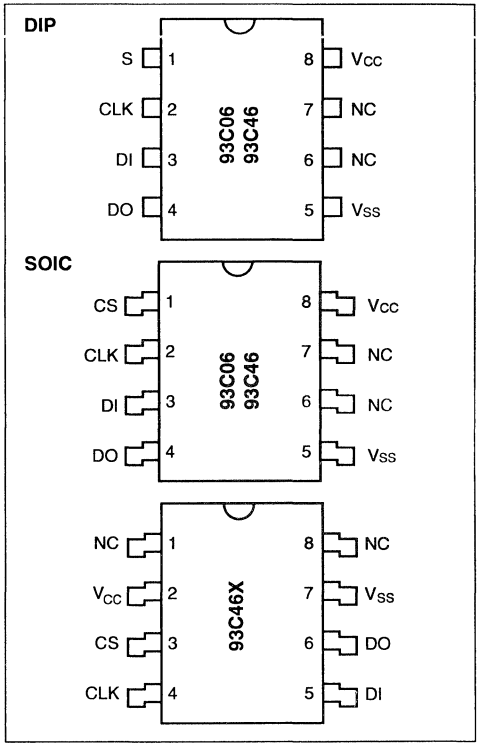
- Low power CMOS technology
- 16 bit memory organization
  - 6 x 16 bit organization (93C06)
  - 64 x 16 bit organization (93C46)
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data Retention > 40 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C
- 2 ms program cycle time

DESCRIPTION

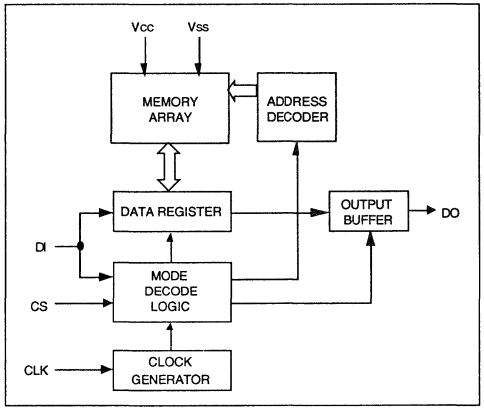
The Microchip Technology Inc. 93C06/46 family of Serial Electrically Erasable PROMs are configured in a x16 organization. Advanced CMOS technology makes these devices ideal for low-power non-volatile memory applications. The 93C06/46 is available in the standard 8-pin DIP and surface mount SOIC packages. The 93C46X comes as SOIC only.

These devices offer fast (1 ms) byte write and extended (-40°C to +125°C) temperature operation. It is recommended that all other applications use Microchip's 93LC46.

PACKAGE TYPE



BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC 7.0V

All inputs and outputs w.r.t. VSS.....-0.6V to VCC +1.0V

Storage temperature.....-65°C to +150°C

Ambient temperature with power applied . -65°C to +125C

Soldering temperature of leads (10 seconds).....+300°C

ESD protection on all pins ..... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
VSS	Ground
NC	No Connect; No Internal Connection
VCC	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

VCC = +5V (±10%)			Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Automotive: Tamb = -40°C to +125°C (Note 3)		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
VCC detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	VCC + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4	—	V	IOH = -400 µA
Low level output voltage	VOL	—	0.4	V	IOL = 3.2 mA
Input leakage current	ILI	—	10	µA	VIN = 0V to VCC (Note 1)
Output leakage current	ILO	—	10	µA	VOUT = 0V to VCC (Note 1)
Internal capacitance (all inputs/outputs)	CINT	—	7	pF	VIN/VOUT = 0V (Note 2) Tamb = +25°C, f = 1 MHz
Operating current (all modes)	ICC write	—	4	mA	FCLK = 1 MHz, VCC = 5.5V
Standby current	ICCS	—	100	µA	CS = 0V, VCC = 5.5V

Note 1: Internal resistor pull-up at Pin 6.
Note 2: This parameter is periodically sampled and not 100% tested.
Note 3: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

FIGURE 1-1: SYNCHRONOUS DATA TIMING

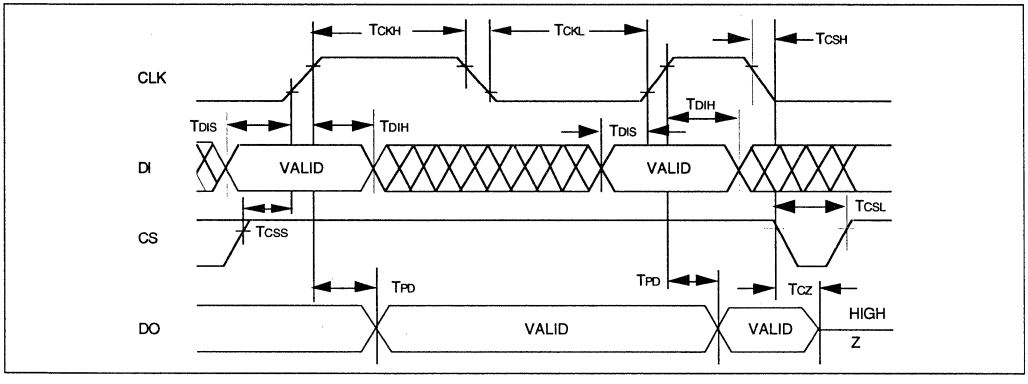


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500	—	ns	
Clock low time	TCKL	500	—	ns	
Chip select setup time	TCSS	50	—	ns	
Chip select6 hold time	TCSH	0	—	ns	
Chip select low time	TCSL	100	—	ns	
Data input setup time	TDIS	100	—	ns	
Data input hold time	TDIH	100	—	ns	
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
Status valid time	TSV	—	100	ns	CL = 100 pF
Program cycle time (Auto Erase and Write)	TWC	—	2 15	ms ms	For ERAL and WRAL
Erase cycle time	TEC	—	1	ms	

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C06/46. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status. (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition, the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become "Don't Care" inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

2.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) from the falling edge of the CLK which clocked in the last DI bit (D0 for WRITE, A0 for ERASE) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is outputted after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during Erase and Write cycles if the READY/$\overline{\text{BUSY}}$ status information is outputted by the 93C06/46.

INSTRUCTION SET - 93C06

Instruction	Start BIT	Opcode OP1 OP2	Address	Number of Data In	Data Out	Req. CLK Cycles
READ	1	1 0	0 0 A3 A2 A1 A0	—	D15 - D0	25
WRITE	1	0 1	0 0 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
ERASE	1	1 1	0 0 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	9
EWEN	1	0 0	1 1 X X X X	—	High-Z	9
EWDS	1	0 0	0 0 X X X X	—	High-Z	9
ERAL	1	0 0	1 0 X X X X	—	(RDY/$\overline{\text{BSY}}$)	9
WRAL	1	0 0	0 1 X X X X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25

INSTRUCTION SET - 93C46

Instruction	Start BIT	Opcode OP1 OP2	Address	Number of Data In	Data Out	Req. CLK Cycles
READ	1	1 0	A5 A4 A3 A2 A1 A0	—	D15 - D0	25
WRITE	1	0 1	A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
ERASE	1	1 1	A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{\text{BSY}}$)	9
EWEN	1	0 0	1 1 X X X X	—	High-Z	9
EWDS	1	0 0	0 0 X X X X	—	High-Z	9
ERAL	1	0 0	1 0 X X X X	—	(RDY/$\overline{\text{BSY}}$)	9
WRAL	1	0 0	0 1 X X X X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25

3.0 FUNCTIONAL DESCRIPTION

3.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

3.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

3.3 Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached 2.8V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.8V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

3.4 READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 16-bit output string. The output data changes during the HIGH state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 has been a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the low going edge of CS, which ever occurs first.

DO remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15) is always output first, followed by the lower significant bits (D14 - D0).

3.5 WRITE Mode

The WRITE instruction is followed by 16 bits of data which are written into the specified address. The most significant data bit (D15) has to be clocked in first, followed by the lower significant data bits (D14 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic ERASE cycle on the specified address before the data are written. The WRITE cycle is completely self-timed and commences automatically after the rising edge of the CLK for the last data bit (D0).

The WRITE cycle takes 2 ms maximum.

FIGURE 3-1: READ MODE

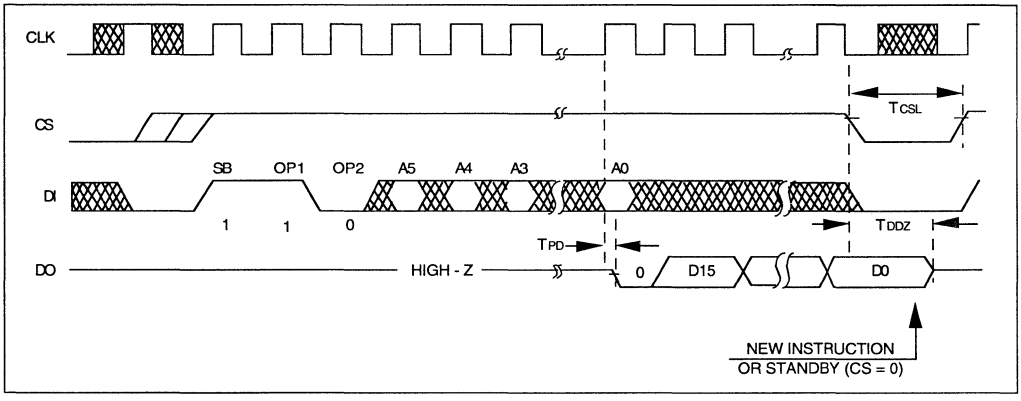
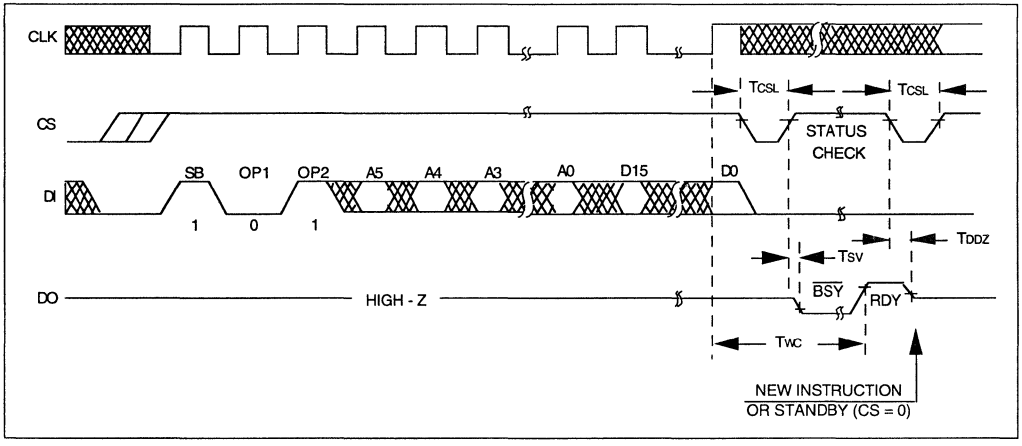


FIGURE 3-2: WRITE MODE

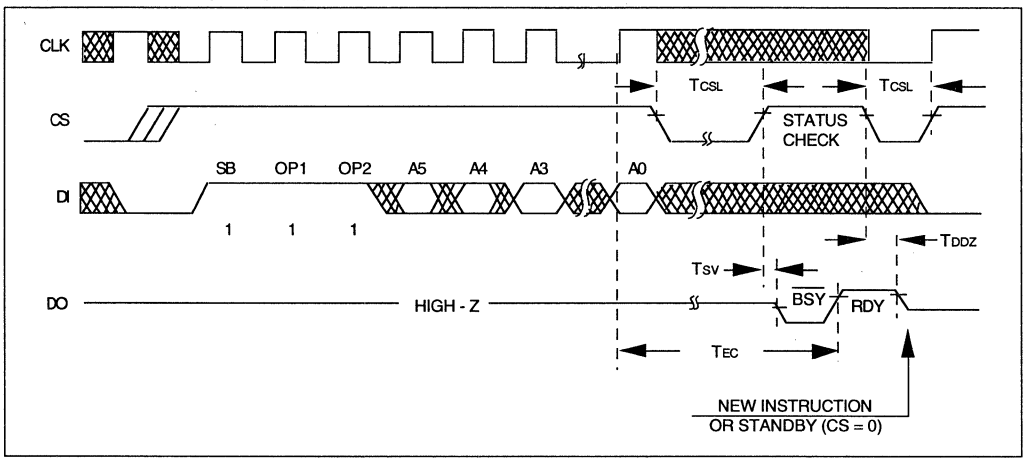


3.6 ERASE Mode

The ERASE instruction forces all the data bits of the specified address to logical "1s". The ERASE cycle is completely self-timed and commences automatically after the last address bit has been clocked in.

The ERASE cycle takes 1 ms maximum.

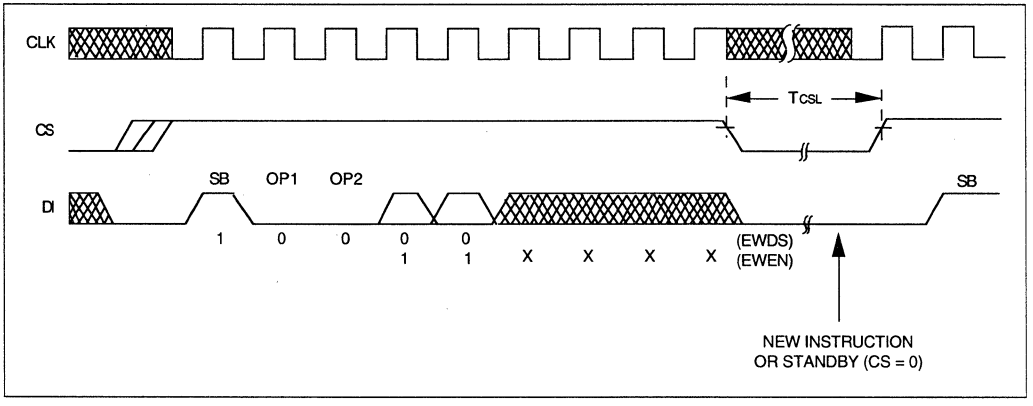
FIGURE 3-3: ERASE MODE



3.7 ERASE/WRITE Enable/Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, an EWEN instruction has to be performed before any ERASE, WRITE, ERAL, WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.

FIGURE 3-4: ERASE/WRITE ENABLE/DISABLE

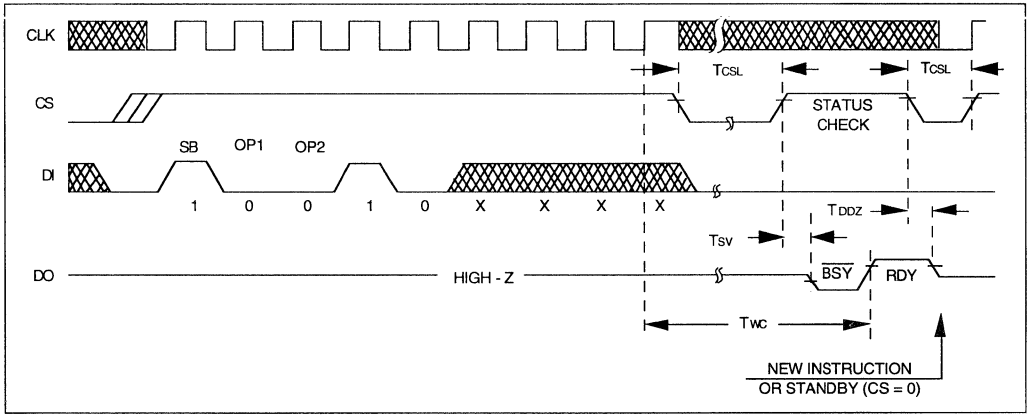


3.8 ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the last dummy address bit has been clocked in.

ERAL takes 15 ms maximum.

FIGURE 3-5: ERASE ALL



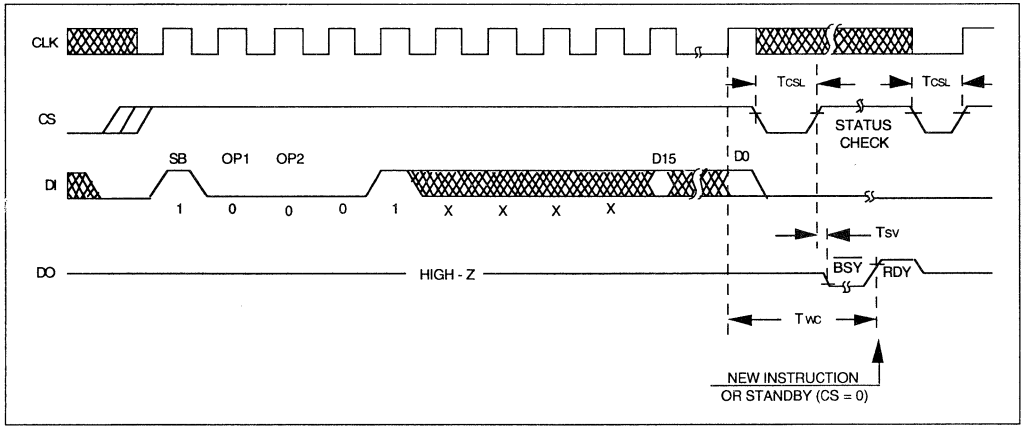
3.9 WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the rising edge of the CLK for the last data bit (DO). WRAL takes 15 ms maximum.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The WRAL instruction is used for testing and/or device initialization.

FIGURE 3-6: WRITE ALL



93C06/46 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93C06/46 - /P

Package:

J	=	CERDIP (300 mil Body)
P	=	Plastic DIP (300 mil Body)
SN	=	Plastic SOIC (150 mil Body)
SM	=	Plastic SOIC (207 mil Body)

Temperature Range:

Blank	=	0°C to +70°C
I	=	-40°C to +85°C
E	=	-40°C to +125°C

Device:

	Configuration
93C06	256 bit CMOS Serial EEPROM
93C46	1K CMOS Serial EEPROM
93C46X	1K CMOS Serial EEPROM in alternate pinouts (SN package only)
93C06T	CMOS Serial EEPROM (Tape and Reel)
93C46T	CMOS Serial EEPROM (Tape and Reel)
93C46XT	CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1.Your local Microchip sales office

2.The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277

3.The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

93C56/66

2K/4K 5.0V CMOS Serial EEPROM

FEATURES

- Low power CMOS technology
- ORG pin selectable memory organization
  - 256 x 8 or 128 x 16 bit organization (93C56)
  - 512 x 8 or 256 x 16 bit organization (93C66)
- Single 5 volts only operation
- Max clock at 2 MHz
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device status signal during ERASE/WRITE cycles
- Sequential READ function
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data retention > 40 years
- 8-pin PDIP/SOIC packages (SOIC in JEDEC and EIAJ standards)
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C
- 1 ms byte write time

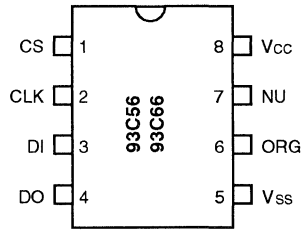
DESCRIPTION

The Microchip Technology Inc. 93C56/66 family of Serial EEPROMs are configurable to either x16 or x8 organization. The ORG pin is used to select the desired configuration. Advanced CMOS technology makes this device ideal for low-power non-volatile memory applications. The 93C56/66 are available in the standard 8-pin DIP and 8-pin surface mount SOIC package.

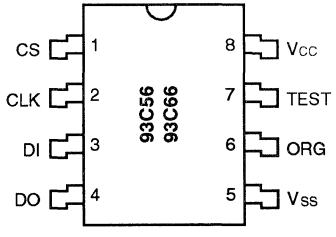
This device offers fast (1 ms) byte write and extended (-40°C to +125°C) temperature operation. It is recommended that all other applications use Microchip's 93LC56/93LC66.

PACKAGE TYPE

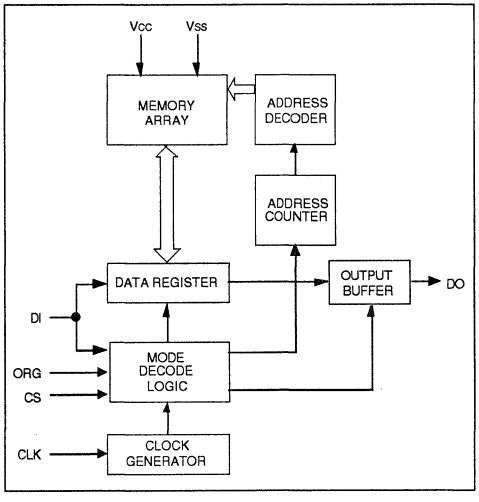
DIP



SOIC



BLOCK DIAGRAM



4

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V
All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins.....3 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
ORG	Memory Array Organization
Test	Connect to Vss or Vcc
Vcc	Power Supply +5V

TABLE 1-2: DC CHARACTERISTICS

	Commercial (C): Tamb = 0°C to +70°C Vcc = +5V (±10%) Industrial (I): Tamb = -40°C to +85°C Vcc = +5V (±10%) Automotive (E): Tamb = -40°C to +125°C Vcc = +5V (±10%) (Note 2)				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Vcc detector threshold	VTH	2.3	4.5	V	
High level input voltage	VIH	2.0	Vcc + 1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4		V	IOH = -400 µA
Low level output voltage	VOL	—	0.4	V	IOL = 2.1 mA
Input leakage current	ILI	—	10	µA	VIN = 0V to Vcc
Output leakage current	ILO	—	10	µA	VOUT = 0V to Vcc
Output capacitance	COUT	—	7	pF	VIN/VOUT = 0V; Note 1
Input capacitance	CIN	—	7	pF	VIN/VOUT = 0V; Note 1
Operating current (all modes)	Icc write	—	4	mA	Fclk = 2 MHz; Vcc = 5.5V
Standby current	ICCS	—	130	µA	Cs = 0V; Vcc = 5.5V; x 8 org
	—	—	100	µA	CS = 0V; Vcc = 5.5V; x 16 org
Clock frequency	FCLK		2	MHz	
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	100	—	ns	
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time	TCZ	—	100	ns	CL = 100 pF
Status valid time	TSV	—	100	ns	CL = 100 pF
Program cycle time	TWC	—	1	ms	(x 8 organization)
(auto ERASE and WRITE)		—	2	ms	(x16 organization)
	TEC	—	15	ms	ERAL & WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz. It is periodically sampled and not 100% tested.
Note 2: For operation above 85°C, endurance is rated at 10,000 ERASE/WRITE cycles.

TABLE 1-3: INSTRUCTION SET FOR 93C56

ORG = 1 (x 16 organization)						
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**Req. CLK Cycles**
READ	1	10	X A6 A5 A4 A3 A2 A1 A0	—	D15 - D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	X A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	X A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15 - D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

ORG = 0 (x 8 organization)						
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**Req. CLK Cycles**
READ	1	10	X A7 A6 A5 A4 A3 A2 A1 A0	—	D7 - D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	X A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	X A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7- D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

TABLE 1-4: INSTRUCTION SET FOR 93C66

ORG = 1 (x 16 organization)						
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**Req. CLK Cycles**
READ	1	10	A7 A6 A5 A4 A3 A2 A1 A0	—	D15-D0	27
EWEN	1	00	1 1 X X X X X X	—	High-Z	11
ERASE	1	11	A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	11
ERAL	1	00	1 0 X X X X X X	—	(RDY/$\overline{BSY}$)	11
WRITE	1	01	A7 A6 A5 A4 A3 A2 A1 A0	D15 - D0	(RDY/$\overline{BSY}$)	27
WRAL	1	00	0 1 X X X X X X	D15- D0	(RDY/$\overline{BSY}$)	27
EWDS	1	00	0 0 X X X X X X	—	High-Z	11

ORG = 0 (x 8 organization)						
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**Req. CLK Cycles**
READ	1	10	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	D7-D0	20
EWEN	1	00	1 1 X X X X X X X	—	High-Z	12
ERASE	1	11	A8 A7 A6 A5 A4 A3 A2 A1 A0	—	(RDY/$\overline{BSY}$)	12
ERAL	1	00	1 0 X X X X X X X	—	(RDY/$\overline{BSY}$)	12
WRITE	1	01	A8 A7 A6 A5 A4 A3 A2 A1 A0	D7 - D0	(RDY/$\overline{BSY}$)	20
WRAL	1	00	0 1 X X X X X X X	D7- D0	(RDY/$\overline{BSY}$)	20
EWDS	1	00	0 0 X X X X X X X	—	High-Z	12

4

2.0 FUNCTIONAL DESCRIPTION

The 93C56/66 family can be organized x16 or x8. When the ORG pin is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the (x16) organization. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CLK.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all modes of operation are inhibited until Vcc has reached 2.3 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.3 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

3.0 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit (x16 organization) or 8 bit (x8 organization) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

4.0 ERASE/WRITE ENABLE AND DISABLE

The 93C56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data changes, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

5.0 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction.

The ERASE cycle takes 1 ms per byte maximum.

6.0 WRITE

The WRITE instruction is followed by 16 bits (or by 8 bits) of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the READY/BUSY status of the device if CS is brought high after a minimum of 100 ns (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at

the specified address has been written with the data specified and the device is ready for another instruction.

The WRITE cycle takes 1 ms per byte maximum.

7.0 ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1". The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL) and before the entire write cycle is complete.

The ERAL cycle takes 15 ms maximum.

8.0 WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does not include an automatic ERASE cycle for the device. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 100 ns low (TCSL).

The WRAL cycle takes 15 ms maximum.

9.0 PIN DESCRIPTION

9.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 100 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

9.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93C56/66. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note: CS must go LOW between consecutive instructions.

9.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

9.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after being LOW for minimum chip select LOW time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

9.5 Organization (ORG)

When ORG is connected to VCC, the (x16) memory organization is selected. When ORG is tied to VSS, the (x8) memory organization is selected. When ORG is left floating, an internal pullup device will select the device in (x16) organization.

9.6 Test

This pin is used for test mode only. It is recommended to connect to VCC or VSS for normal operation.

FIGURE 9-1: SYNCHRONOUS DATA TIMING

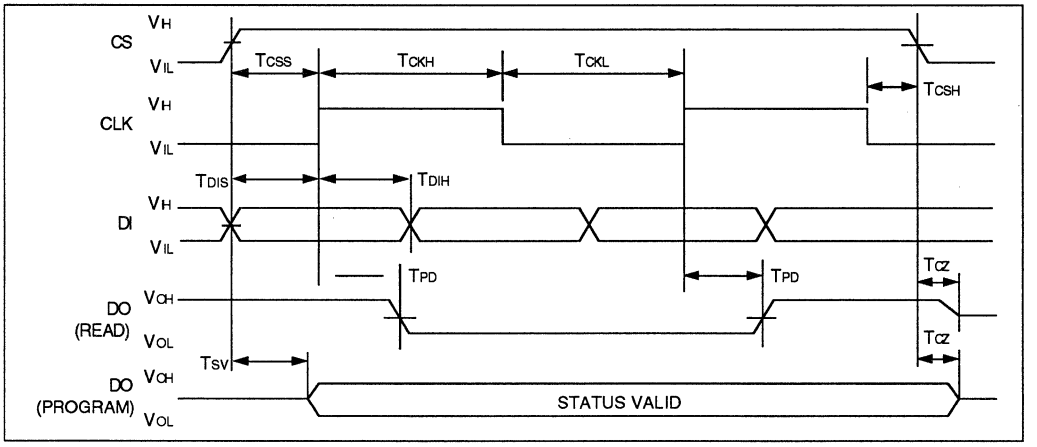
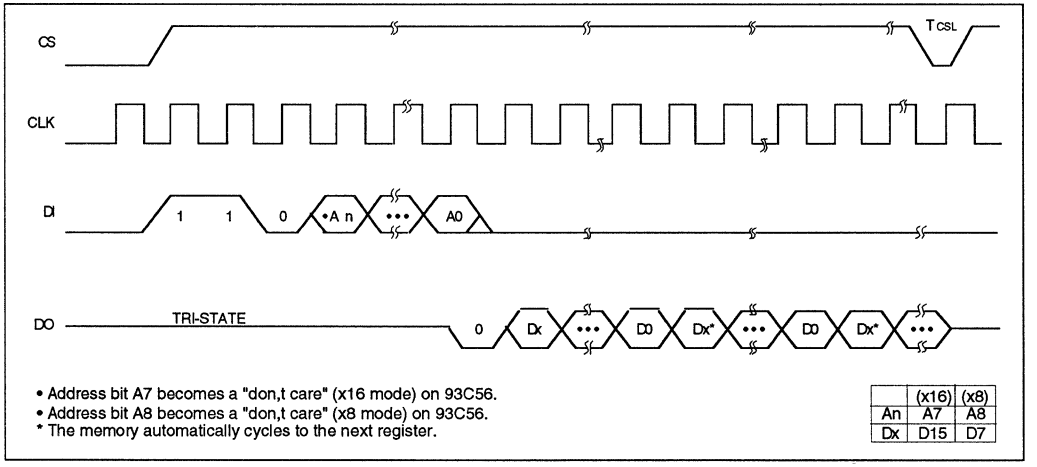


FIGURE 9-2: READ TIMING



• Address bit A7 becomes a "don,t care" (x16 mode) on 93C56.
• Address bit A8 becomes a "don,t care" (x8 mode) on 93C56.
* The memory automatically cycles to the next register.

	(x16)	(x8)
An	A7	A8
Dx	D15	D7

FIGURE 9-3: EWEN TIMING

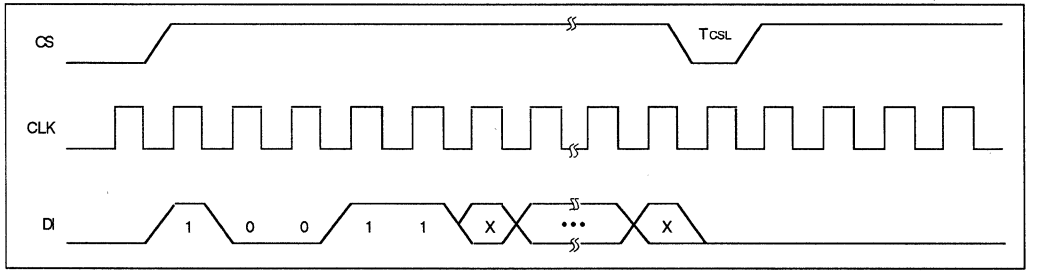


FIGURE 9-4: EWDS TIMING

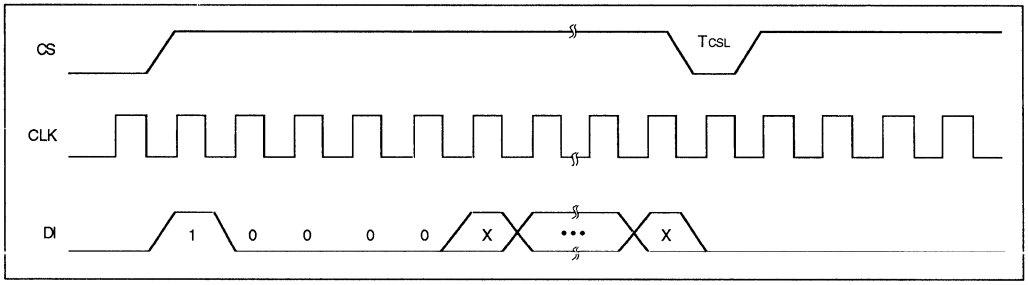
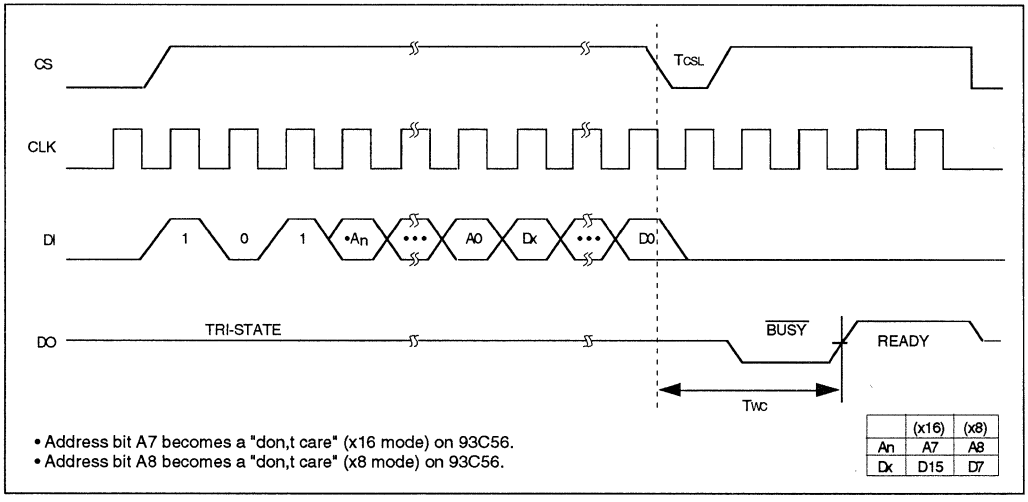


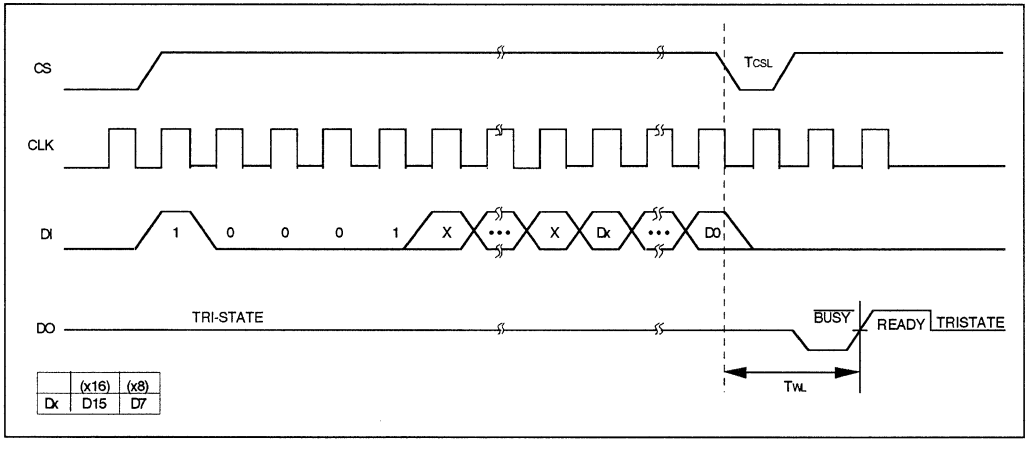
FIGURE 9-5: WRITE TIMING



• Address bit A7 becomes a "don,t care" (x16 mode) on 93C56.
• Address bit A8 becomes a "don,t care" (x8 mode) on 93C56.

	(x16)	(x8)
An	A7	A8
Dx	D15	D7

FIGURE 9-6: WRAL TIMING



	(x16)	(x8)
Dx	D15	D7

FIGURE 9-7: ERASE TIMING

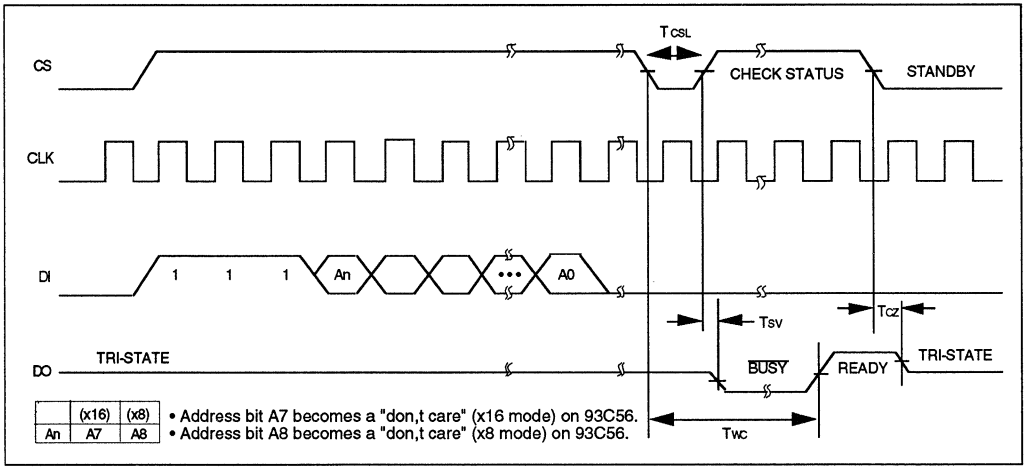
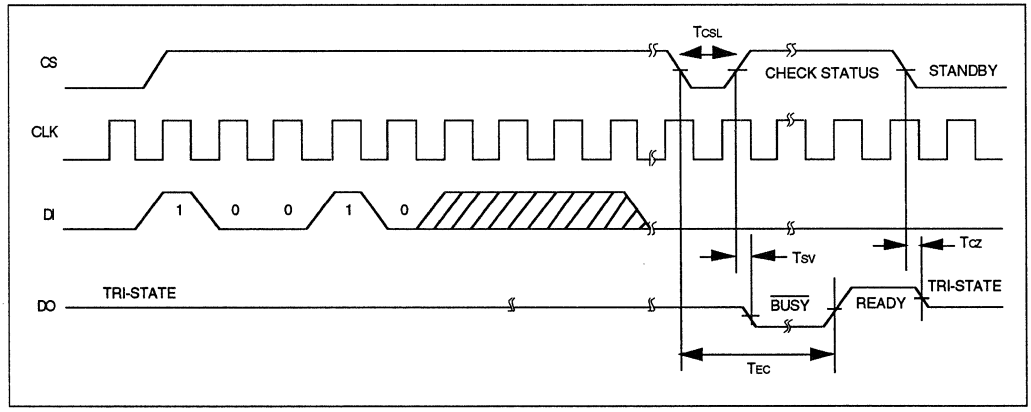


FIGURE 9-8: ERAL TIMING



NOTES

93C56/66 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93C56/66 - /P

Package:	P	=	Plastic DIP (300 mil Body)
	SN	=	Plastic SOIC (150 mil Body)
	SM	=	Plastic SOIC (207 mil Body)
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Device:	93C56		2K CMOS Serial EEPROM
	93C56T		2K CMOS Serial EEPROM (Tape and Reel)
	93C66		4K CMOS Serial EEPROM
	93C66T		4K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

SECTION 5
SPECIALTY SERIAL EEPROM PRODUCT SPECIFICATIONS

24AA174	16K 1.8V Cascadable CMOS Serial EEPROM with OTP Security Page	5-1
24LC174	16K 2.5V Cascadable CMOS Serial EEPROM with OTP Security Page	5-11
24LC21	1K 2.5V Dual Mode CMOS Serial EEPROM	5-21
24AA65	64K 1.8V CMOS Smart Serial™ EEPROM	5-33
24LC65	64K 2.5V CMOS Smart Serial™ EEPROM	5-45
24C65	64K 5.0V CMOS Smart Serial™ EEPROM	5-57
59C11	1K 5.0V CMOS Serial EEPROM	5-69
93LCS56/66	2K/4K 2.5V CMOS Serial EEPROM with Software Write Protect	5-77

24AA174

16K 1.8V Cascadable CMOS Serial EEPROM with OTP Security Page

FEATURES

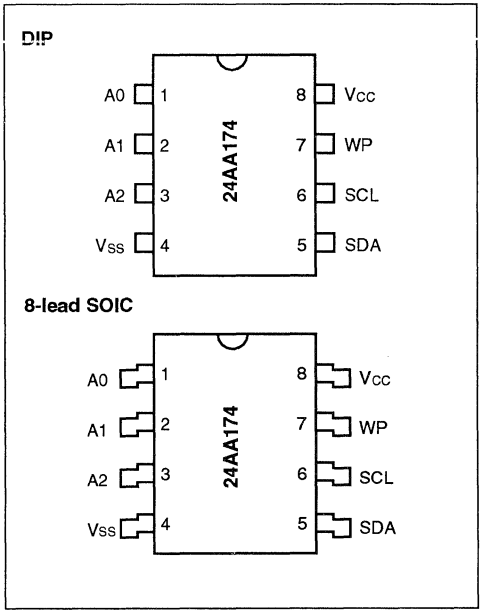
- Single supply with operation down to 1.8V
- 16 Bytes OTP Secure Memory
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus, I^2C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (1.8V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **10,000,000 ERASE/WRITE cycles guaranteed**
- Data retention > 40 years
- 8 pin DIP, 8-lead SOIC packages
- Available for commercial temperature range
  - Commercial: 0°C to +70°C

DESCRIPTION

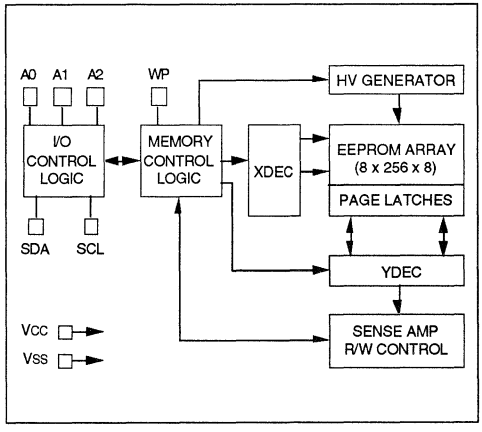
The Microchip Technology Inc. 24AA174 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface and provides a specially addressed OTP (one-time programmable) 16 byte security block. Low voltage design permits operation down to 1.8 volts (end-of-life voltage for most popular battery technologies) with standby and active currents of only 5 µA and 1 mA respectively. The 24AA174 also has a page-write capability for up to 16 bytes of data. The 24AA174 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPE



BLOCK DIAGRAM



5

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.3V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
VCC	+1.8V to 5.5V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

VCC = +1.8V to 5.5V Commercial (C): Tamb = 0°C to +70°C					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins: High level input voltage Low level input voltage Hysteresis of Schmitt trigger inputs Low level output voltage	 VIH VIL VHYS VOL	 .7 VCC — .05 VCC —	 — .3 VCC — .40	 V V V V	 Note 1 IOL = 3.0 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Input capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note1) Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	VCC = 3.0V, SDA = SCL = VCC VCC = 5.5V, SDA = SCL = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

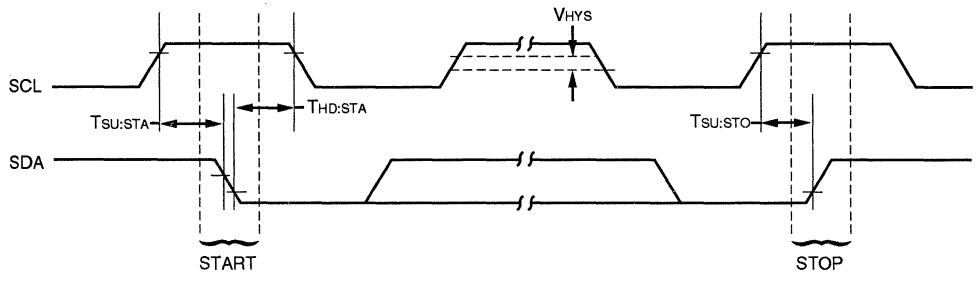
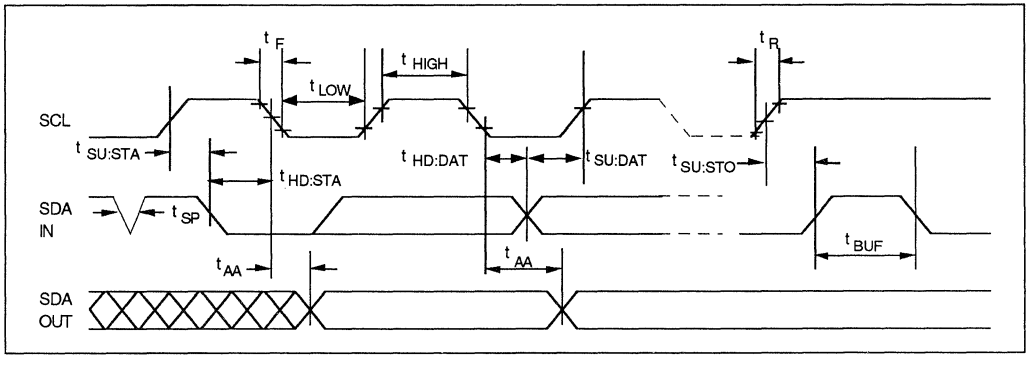


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		V cc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000		300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	—	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	100,000	—	100,000	—	E/W Cycles	

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA174 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA174 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

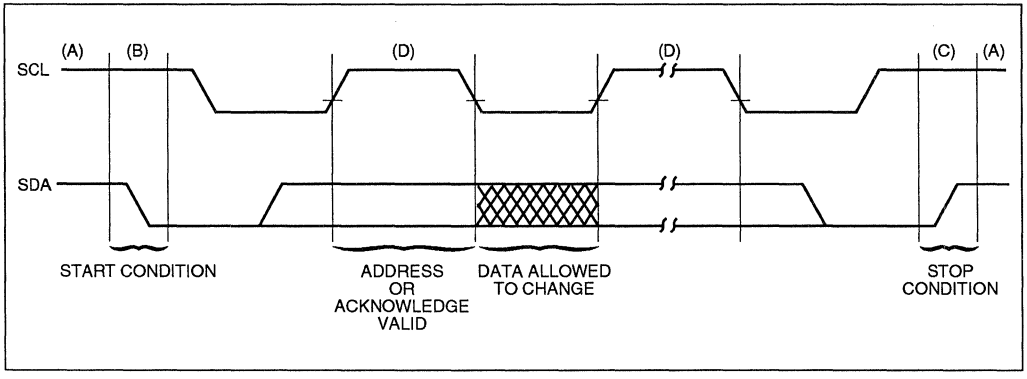
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA174 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA174) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation

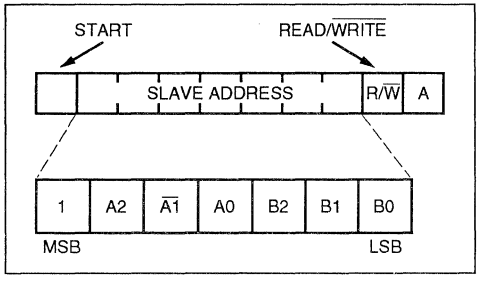
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24AA174 looks for the slave address for the device selected. Depending on the state of the R/$\overline{W}$ bit, the 24AA174 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1 A2 $\overline{A1}$ A0	Block Address	1
Write	1 A2 $\overline{A1}$ A0	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

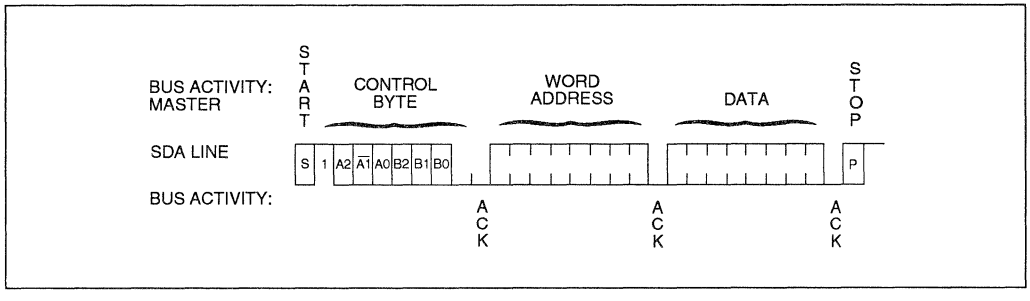
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA174. After receiving another acknowledge signal from the 24AA174 the master device will transmit the data word to be written into the addressed memory location. The 24AA174 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA174 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA174 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24AA174 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

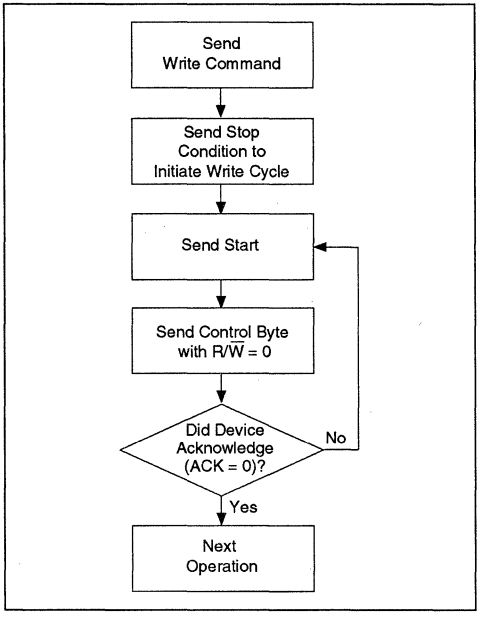
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24AA174 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

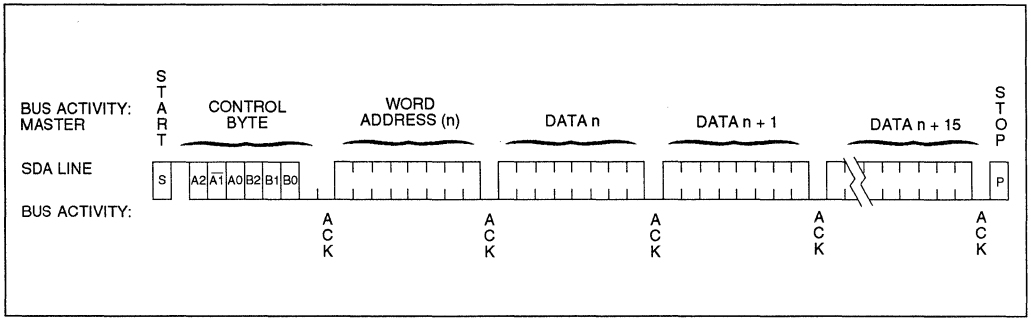
8.1 Current Address Read

The 24AA174 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA174 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA174 discontinues transmission (see Figure 9-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA174 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA174 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA174 discontinues transmission (see Figure 9-2).

FIGURE 8-1: PAGE WRITE



8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA174 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24AA174 to transmit the next sequentially addressed 8 bit word (see Figure 9-3).

To provide sequential reads the 24AA174 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

8.4 Noise Protection

The 24AA174 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24AA174 as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are used to configure the proper chip address in multiple-chip applications (more than one 24AA174 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note: The level on A1 is compared to the inverse of the slave address.

Up to eight 24AA174s may be connected to the same bus. These pins must be connected to either Vss or Vcc.

9.5 Security Access Control

The security row is enabled by sending the control sequence with the I^2C slave address of 0110. Bit 0 of the control byte must be set to a 1 for a READ OPERATION or a 0 for the OTP WRITE OPERATION. The SECURITY ACCESS DATA is always read starting at byte 0 for N bytes up to and including byte 15. (See Figure 8-1).

9.6 Security Access Write

The S.A.W. data is written to the device using a normal page write following the proper control access sequence. Upon receiving the final stop bit, the internal write sequence will commence. At the completion of the internal write sequence a fuse will be set disabling the write function for the 16 byte security page.

9.7 Security Access Read

The security access read is accomplished by executing the normal read sequences, following the security access control sequence with bit 0 set to a 1. The security page read starts at data byte 0.

5

FIGURE 9-1: CURRENT ADDRESS READ

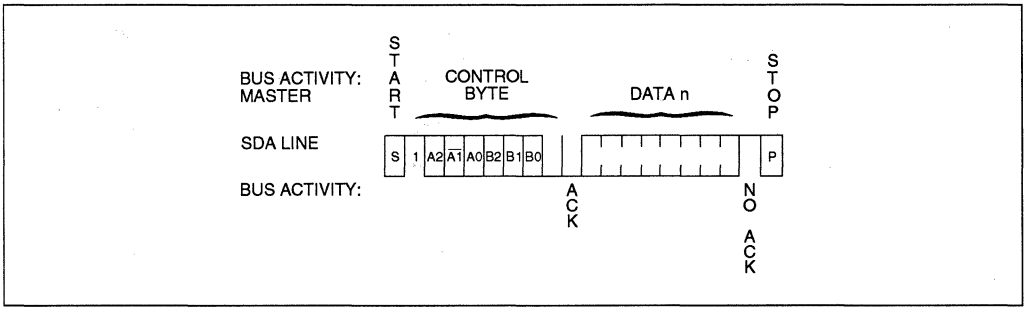


FIGURE 9-2: RANDOM READ

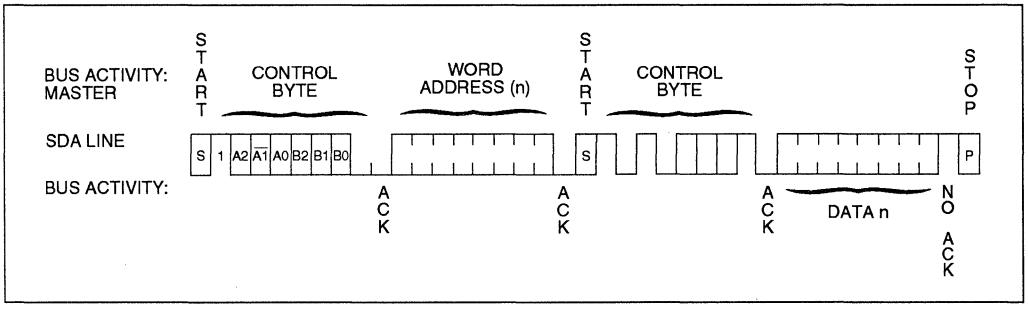


FIGURE 9-3: SEQUENTIAL READ

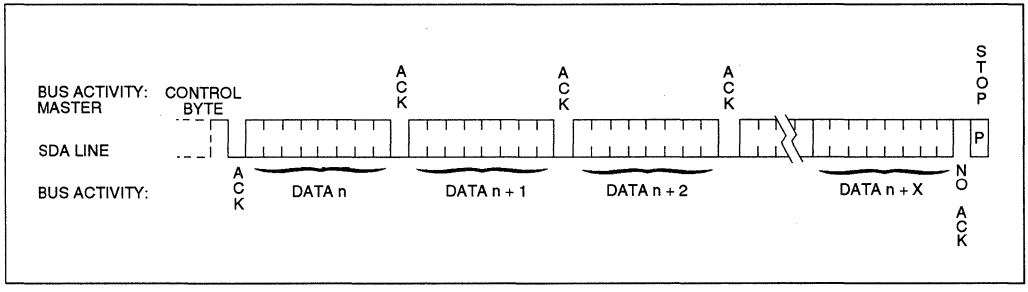


FIGURE 9-4: SECURITY CONTROL BYTE ALLOCATION

Operation	Control Code	MBZ	R/$\overline{W}$
Read	0110	000	1
Write	0110	000	0

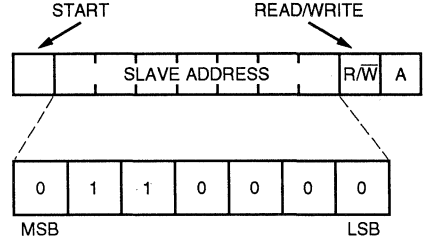


FIGURE 9-5: SECURITY PAGE READ

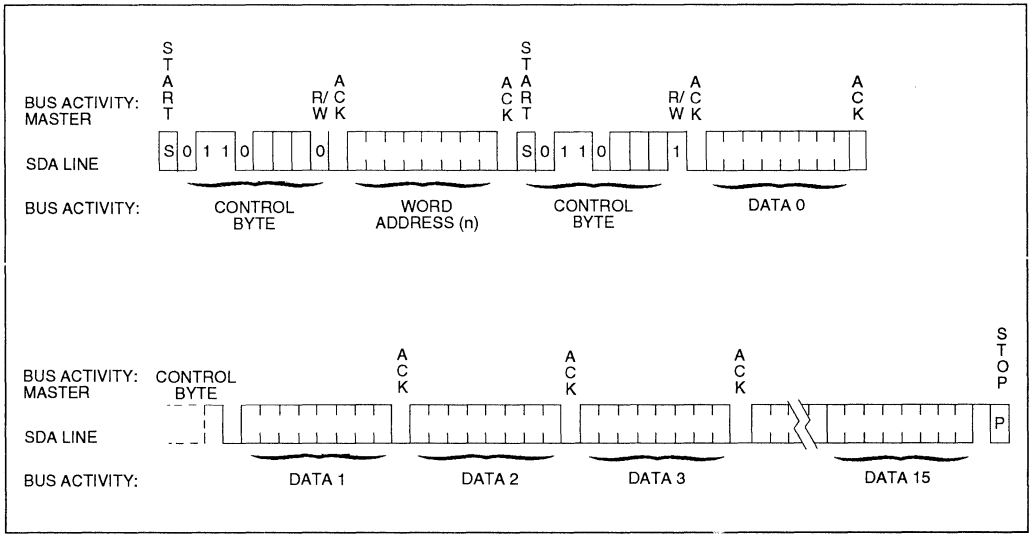
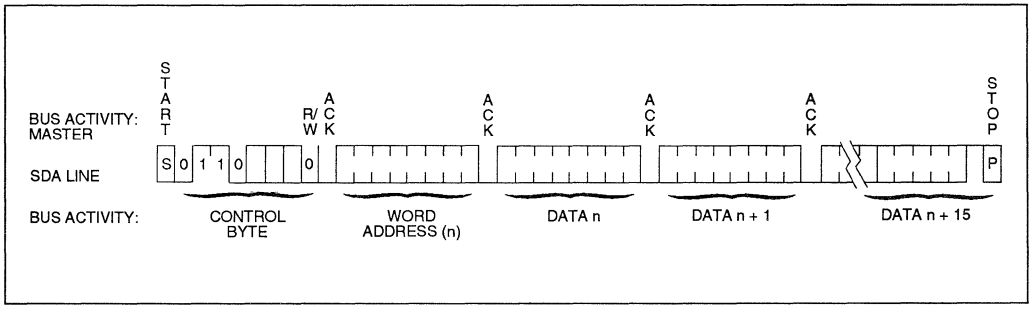


FIGURE 9-6: SECURITY PAGE WRITE



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24AA174 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24AA174 - /P

Package:		P =	Plastic DIP (300 mil Body), 8-lead
		SN =	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:		Blank =	0°C to +70°C
Device:	24AA174		16K CMOS Serial EEPROM
	24AA174T		16K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

24LC174

16K 2.5V Cascadable CMOS Serial EEPROM with OTP Security Page

FEATURES

- Single supply with operation down to 2.5V
- 16 Bytes OTP Secure Memory
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus, I^2C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- **10,000,000 ERASE/WRITE cycles guaranteed**
- Data retention > 40 years
- 8 pin DIP, 8-lead SOIC packages
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

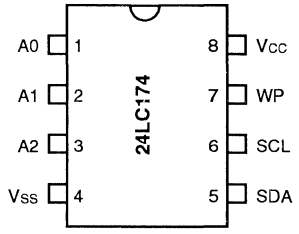
DESCRIPTION

The Microchip Technology Inc. 24LC174 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface and provides a specially addressed OTP (one-time programmable) 16 byte security block. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 µA and 1 mA respectively. The 24LC174 also has a page-write capability for up to 16 bytes of data. The 24LC174 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

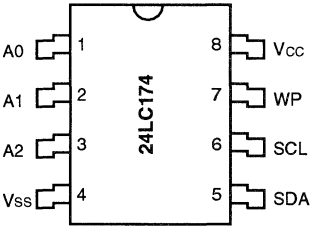
The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPE

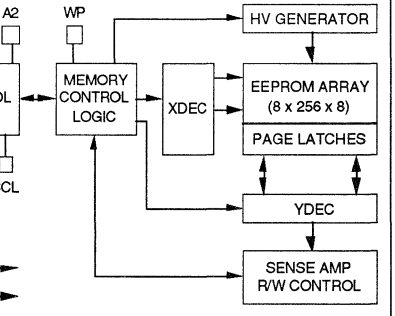
DIP



8-lead SOIC



BLOCK DIAGRAM



5

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V
All inputs and outputs w.r.t. Vss ..... -0.3V to Vcc +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5V to 5.5V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

	Vcc = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
WP, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA, Vcc = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Input capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note1), Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc Write	—	3	mA	Vcc = 5.5V, SCL = 400 kHz
	Icc Read	—	1	mA	
Standby current	Iccs	—	30	µA	Vcc = 3.0V, SDA = SCL = Vcc
		—	100	µA	Vcc = 5.5V, SDA = SCL = Vcc

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

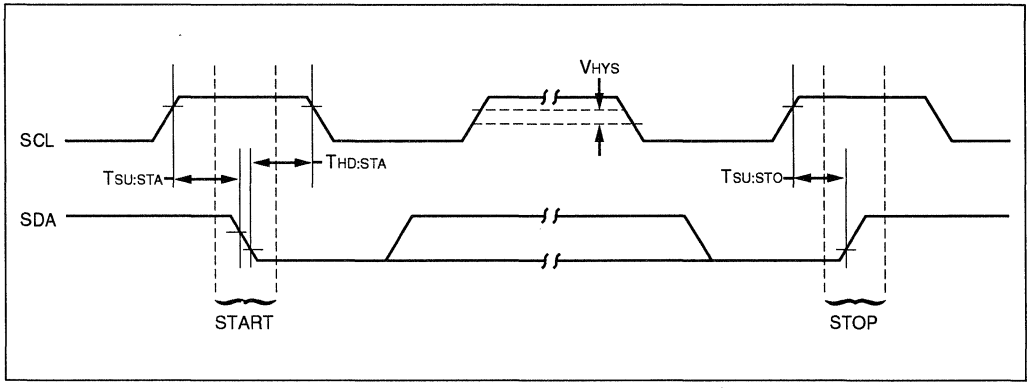
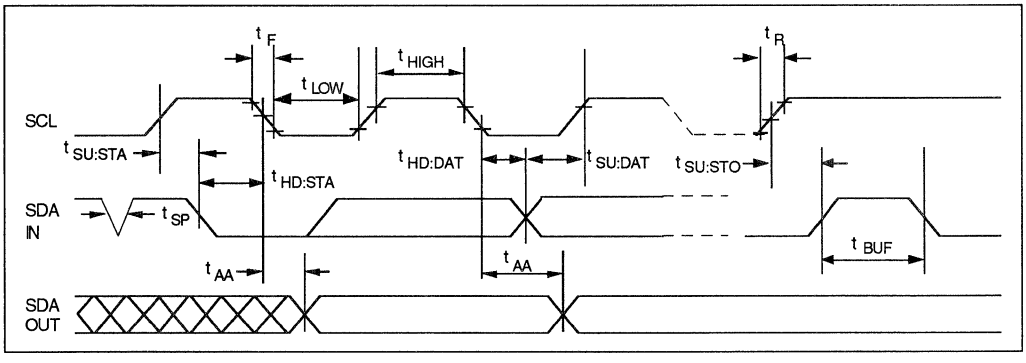


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		V cc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	—	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC174 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC174 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

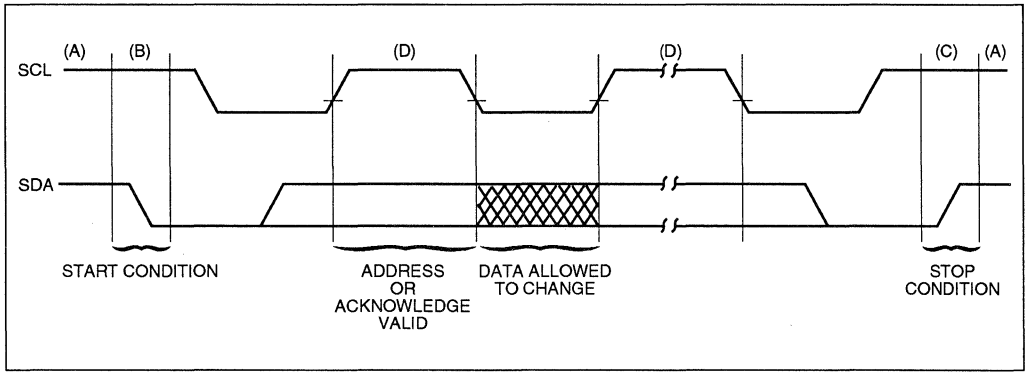
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC174 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC174) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation

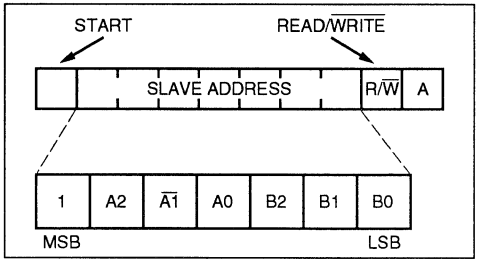
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC174 looks for the slave address for the device selected. Depending on the state of the R/$\overline{W}$ bit, the 24LC174 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1 A2 $\overline{A1}$ A0	Block Address	1
Write	1 A2 $\overline{A1}$ A0	Block Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

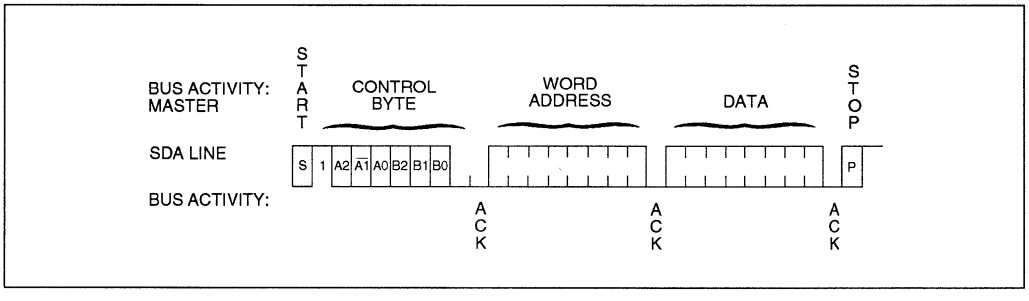
5.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC174. After receiving another acknowledge signal from the 24LC174 the master device will transmit the data word to be written into the addressed memory location. The 24LC174 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC174 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC174 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24LC174 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 8-1).

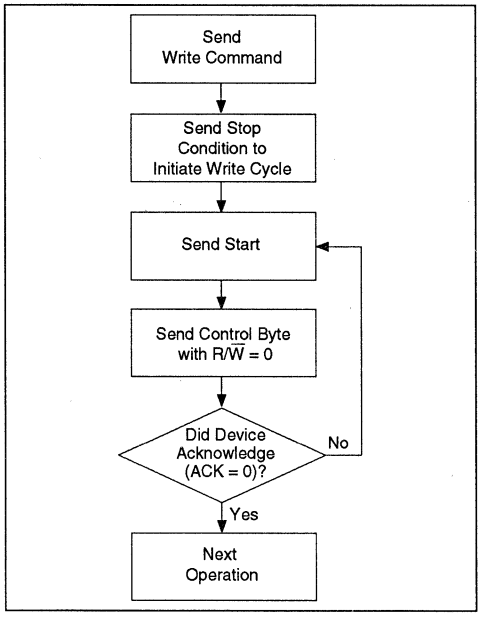
FIGURE 5-1: BYTE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 WRITE PROTECTION

The 24LC174 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

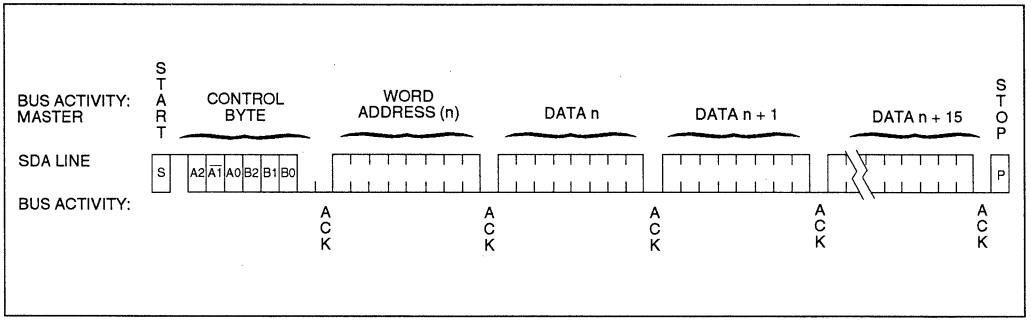
8.1 Current Address Read

The 24LC174 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC174 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC174 discontinues transmission (see Figure 9-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC174 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC174 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC174 discontinues transmission (see Figure 9-2).

FIGURE 8-1: PAGE WRITE



8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC174 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC174 to transmit the next sequentially addressed 8 bit word (see Figure 9-3).

To provide sequential reads the 24LC174 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

8.4 Noise Protection

The 24LC174 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

9.0 PIN DESCRIPTIONS

9.1 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC174 as a serial ROM when WP is enabled (tied to Vcc).

9.4 A0, A1, A2

These pins are used to configure the proper chip address in multiple-chip applications (more than one 24LC174 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note: The level on A1 is compared to the inverse of the slave address.

Up to eight 24LC174s may be connected to the same bus. These pins must be connected to either Vss or Vcc.

9.5 Security Access Control

The security row is enabled by sending the control sequence with the I^2C slave address of 0110. Bit 0 of the control byte must be set to a 1 for a READ OPERATION or a 0 for the OTP WRITE OPERATION. The SECURITY ACCESS DATA is always read starting at byte 0 for N bytes up to and including byte 15. (See Figure 9-3).

9.6 Security Access Write

The S.A.W. data is written to the device using a normal page write following the proper control access sequence. Upon receiving the final stop bit, the internal write sequence will commence. At the completion of the internal write sequence a fuse will be set disabling the write function for the 16 byte security page.

9.7 Security Access Read

The security access read is accomplished by executing the normal read sequences, following the security access control sequence with bit 0 set to a 1. The security page read starts at data byte 0.

5

FIGURE 9-1: CURRENT ADDRESS READ

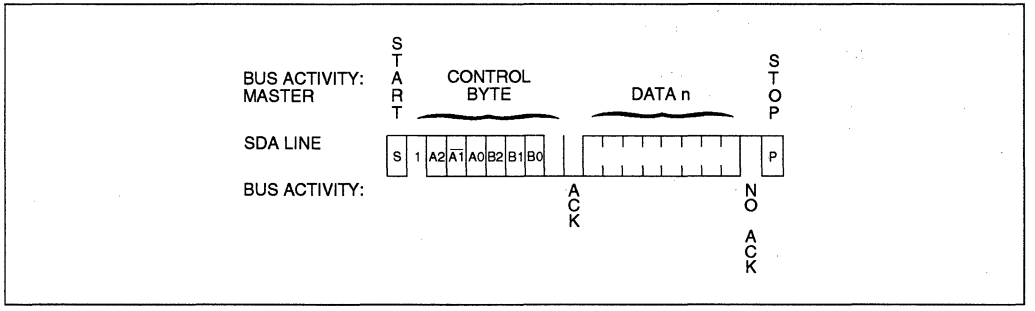


FIGURE 9-2: RANDOM READ

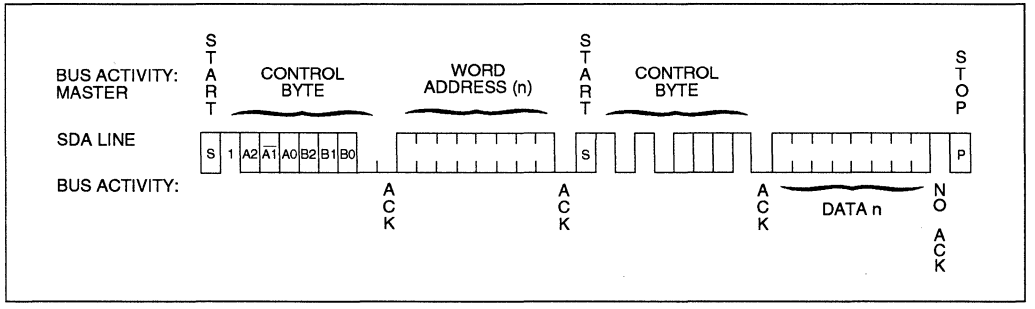


FIGURE 9-3: SEQUENTIAL READ

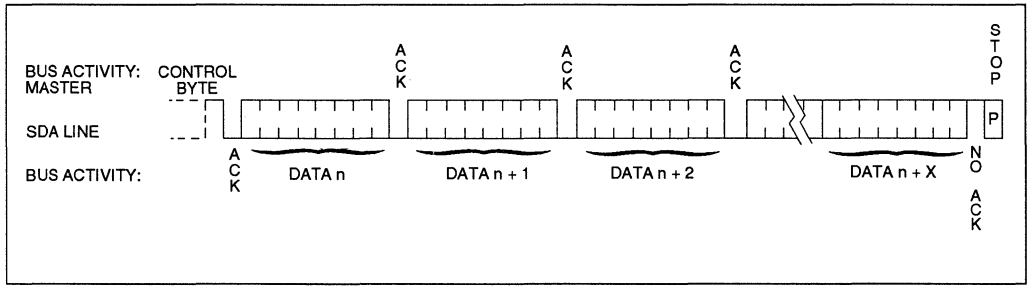


FIGURE 9-4: SECURITY CONTROL BYTE ALLOCATION

Operation	Control Code	MBZ	R/$\overline{W}$
Read	0110	000	1
Write	0110	000	0

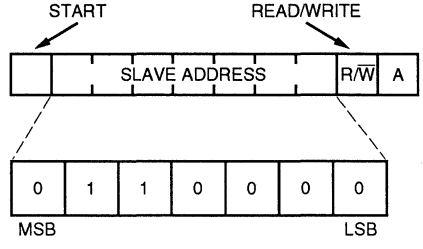


FIGURE 9-5: SECURITY PAGE READ

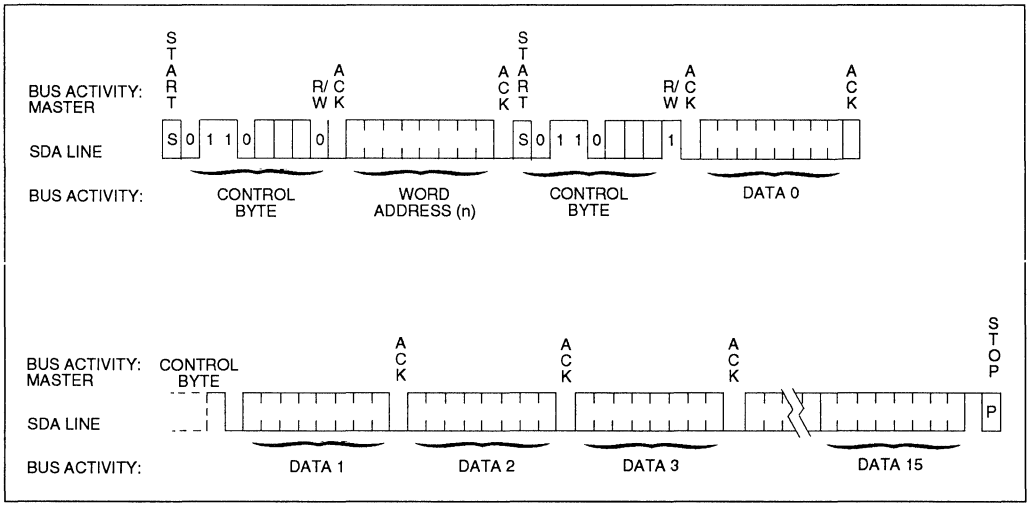
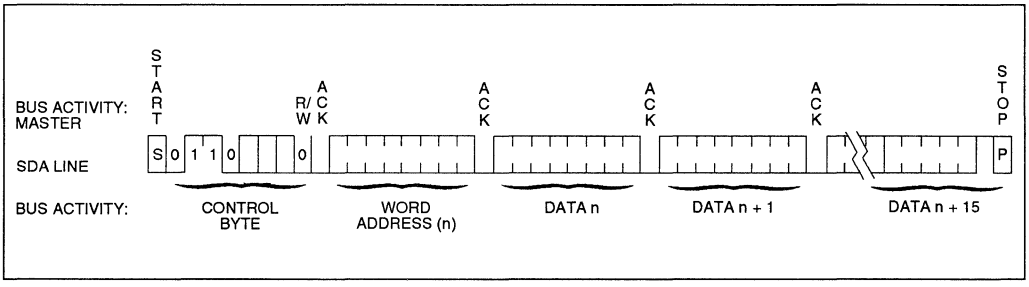


FIGURE 9-6: SECURITY PAGE WRITE



5

24LC174 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC174 - /P

Package:	P	=	Plastic DIP (300 mil Body), 8-lead
	SN	=	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
Device:	24LC174		16K CMOS Serial EEPROM
	24LC174T		16K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

24LC21

1K 2.5V Dual Mode CMOS Serial EEPROM

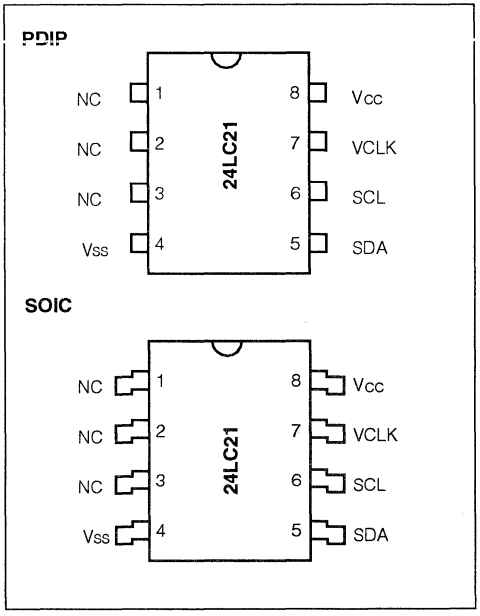
FEATURES

- Single supply with operation down to 2.5V
- Completely implements DDC1™/DDC2™ interface for monitor identification
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Two wire serial interface bus, I²C™ compatible
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Factory programming (QTP) available
- **1,000,000 erase/write cycles guaranteed***
- Data retention > 40 years
- 8 pin PDIP and SOIC package
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

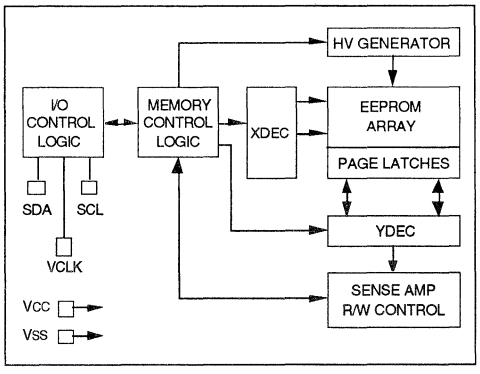
DESCRIPTION

The Microchip Technology Inc. 24LC21 is a 128 x 8 bit Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit Only Mode and Bi-Directional Mode. Upon power-up, the device will be in the Transmit Only Mode, sending a serial bit stream of the entire memory array contents, clocked by the VCLK pin. A valid high to low transition on the SCL pin will cause the device to enter the Bi-Directional Mode, with byte selectable read/write capability of the memory array. The 24LC21 is available in a standard 8-pin PDIP and SOIC package in both commercial and industrial temperature ranges.

PACKAGE TYPE



BLOCK DIAGRAM



*Future: 10,000,000 E/W cycles guaranteed

DDC is a trademark of the Video Electronics Standards Association.
I²C is a trademark of Philips Corporation.

5

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
VSS	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bi-Directional Mode)
VCLK	Serial Clock (Transmit-Only Mode)
VCC	+2.5V to 5.5V Power Supply
NC	No Connection

TABLE 1-2: DC CHARACTERISTICS

	VCC = +2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
SCL and SDA pins: High level input voltage Low level input voltage	 VIH VIL	 .7 VCC —	 — .3 VCC	 V V	
Input levels on VCLK pin: High level input voltage Low level input voltage	 VIH VIL	 2.0 —	 .8 .2 VCC	 V V	 VCC ≥ 2.7V (Note 1) VCC < 2.7V (Note 1)
Hysteresis of Schmitt trigger inputs	VHYS	.05 VCC	—	V	Note 1
Low level output voltage	VOL1	—	.4	V	IOL = 3 mA, VCC = 2.5V (Note 1)
Low level output voltage	VOL2	—	.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = .1V to VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Input capacitance (all inputs/outputs)	CINT	—	10	pF	VCC = 5.0V (Note1), Tamb = 25°C, FCLK = 1 MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	VCC = 3.0V, SDA = SCL = VCC VCC = 5.5V, SDA = SCL = VCC

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		Vcc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 2
SDA and SCL fall time	TF	—	300	—	300	ns	Note 2
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	Note 1
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 1
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + .1 CB	250	ns	Note 2, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	500	—	500	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
Mode transition time	TVHZ	—	500	—	500	ns	
Transmit-Only power up time	TVPU	0	—	0	—	ns	

Note 1: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: Not 100% tested. CB = total capacitance of one bus line in pF.

Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

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2.0 FUNCTIONAL DESCRIPTION

The 24LC21 operates in two modes, the Transmit-Only Mode and the Bi-Directional Mode. There is a separate two wire protocol to support each mode, each having a separate clock input and sharing a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the Bi-Directional Mode. The only way to switch the device back to the Transmit-Only Mode is to remove power from the device.

2.1 Transmit-Only Mode

The device will power up in the Transmit-Only Mode. This mode supports a unidirectional two wire protocol for transmission of the contents of the memory array. This device requires that it be initialized prior to valid data being sent in the Transmit-Only Mode (see Initialization Procedure, below). In this mode, data is transmitted on the SDA pin in 8 bit bytes, each followed by a ninth, null bit (see Figure 2-1). The clock source for the Transmit-Only Mode is provided on the VCLK pin, and a data bit is output on the rising edge on this pin. The eight bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The Bi-Directional Mode Clock (SCL) pin must be held high for the device to remain in the Transmit-Only Mode.

2.2 Initialization Procedure

After Vcc has stabilized, the device will be in the Transmit-Only Mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal sychronization. During this period, the SDA pin will be in a high impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power up at an indeterminate byte address. (See Figure 2-2).

FIGURE 2-1: TRANSMIT ONLY MODE

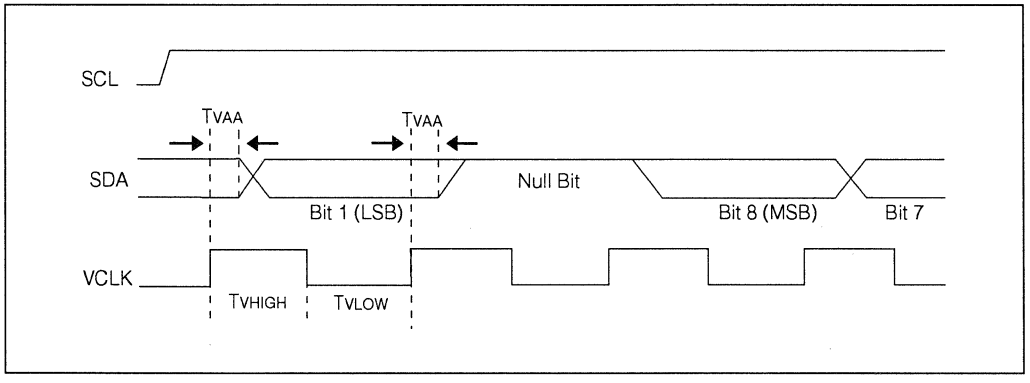
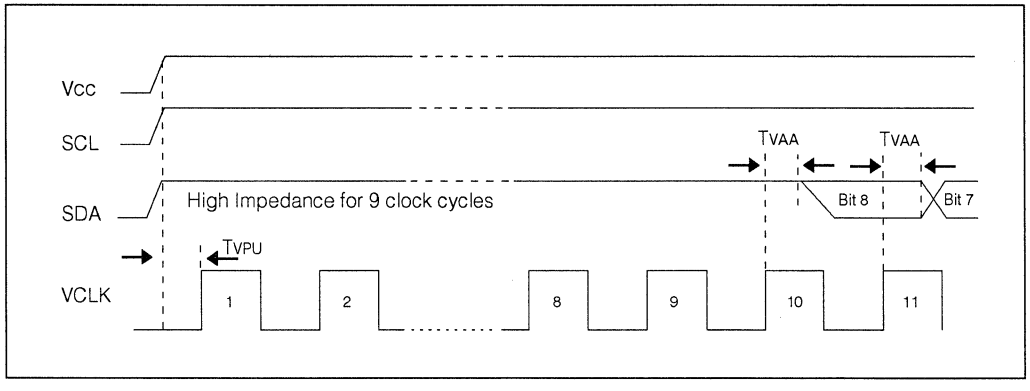


FIGURE 2-2: DEVICE INITIALIZATION



3.0 BI-DIRECTIONAL MODE

The 24LC21 can be switched into the Bi-Directional Mode (see Figure 3-1) by applying a valid high to low transition on the Bi-Directional Mode Clock (SCL). When the device has been switched into the Bi-Directional Mode, the VCLK input is disregarded, with the exception that a logic high level is required to enable write capability. This mode supports a two wire bi-directional data transmission protocol. In this protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the Bi-Directional Mode Clock (SCL), controls access to the bus and generates the START and STOP conditions, while the 24LC21 acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.1 Bi-Directional Mode Bus Characteristics

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-2).

3.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

3.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

5

FIGURE 3-1: MODE TRANSITION

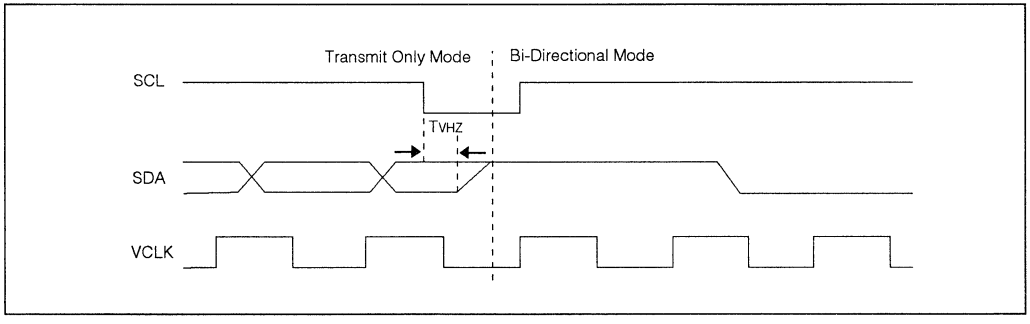
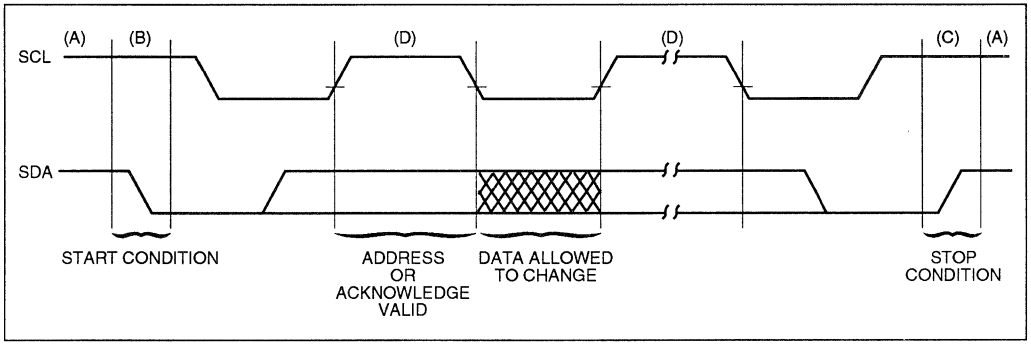


FIGURE 3-2: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last eight will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

3.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC21 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-3: BUS TIMING START/STOP

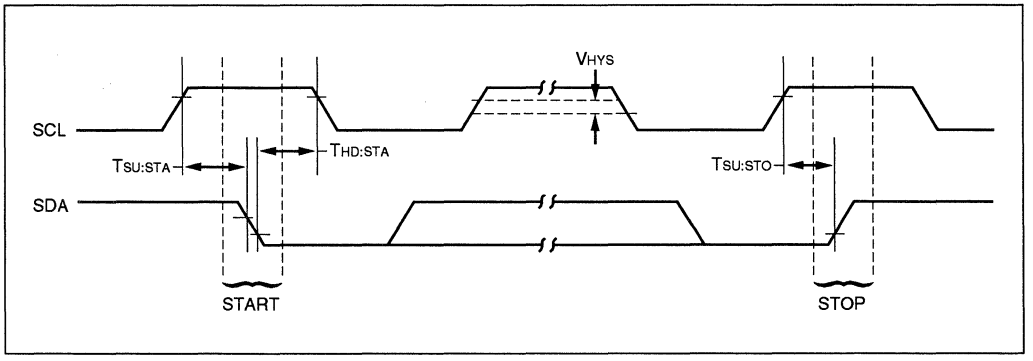
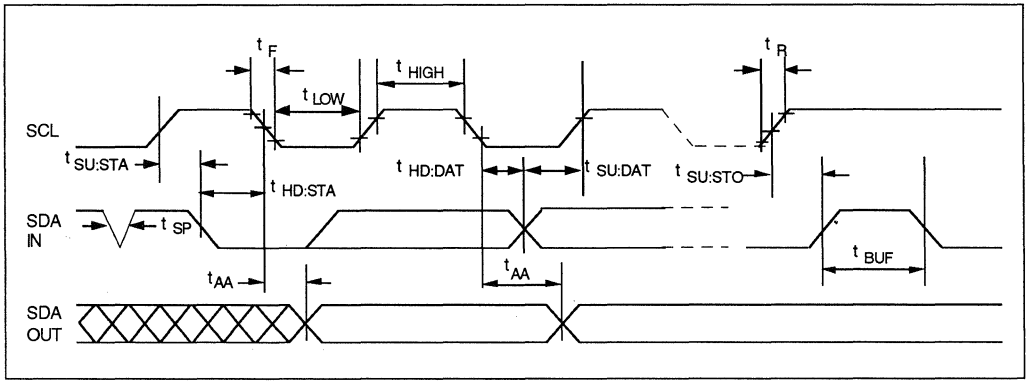


FIGURE 3-4: BUS TIMING DATA



3.1.6 SLAVE ADDRESS

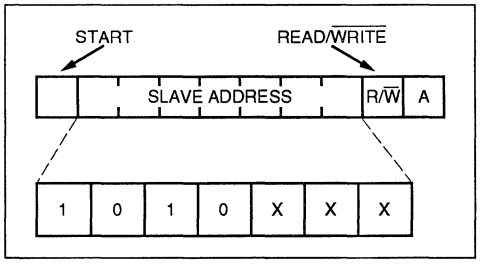
After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (1010) for the 24LC21, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC21 (see Figure 3-5).

The 24LC21 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 3-5: CONTROL BYTE ALLOCATION



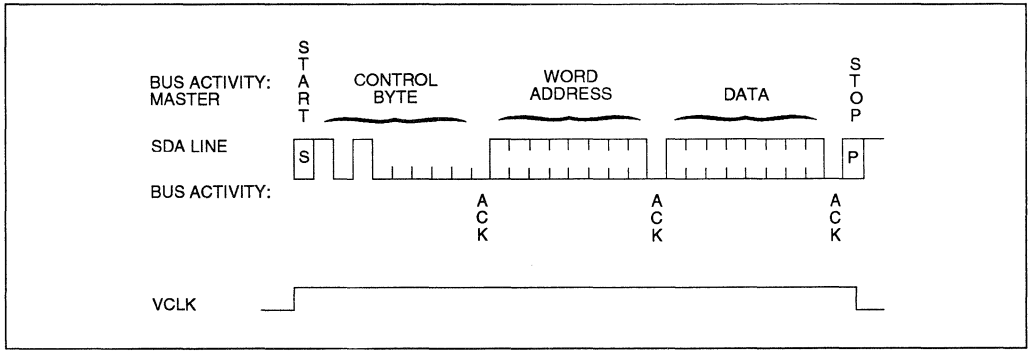
4.0 WRITE OPERATION

4.1 Byte Write

Following the start signal from the master, the slave address (4 bits), the don't care bits (3 bits) and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC21. After receiving another acknowledge signal from the 24LC21 the master device will transmit the data word to be written into the addressed memory location. The 24LC21 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC21 will not generate acknowledge signals (see Figure 4-1).

It is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

FIGURE 4-1: BYTE WRITE



4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC21 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the 24LC21 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (see Figure 5-2).

It is required that VCLK be held at a logic high level in order to program the device. This applies to byte write and page write operation. Note that VCLK can go low while the device is in its self-timed program operation and not affect programming.

5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for the flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW

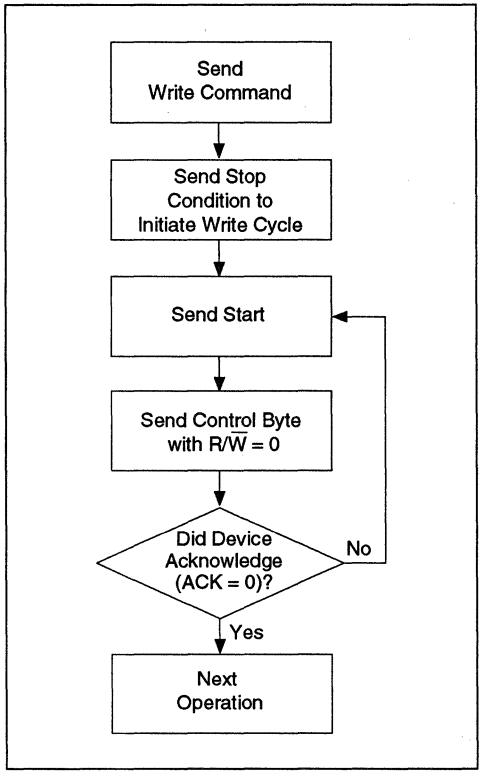
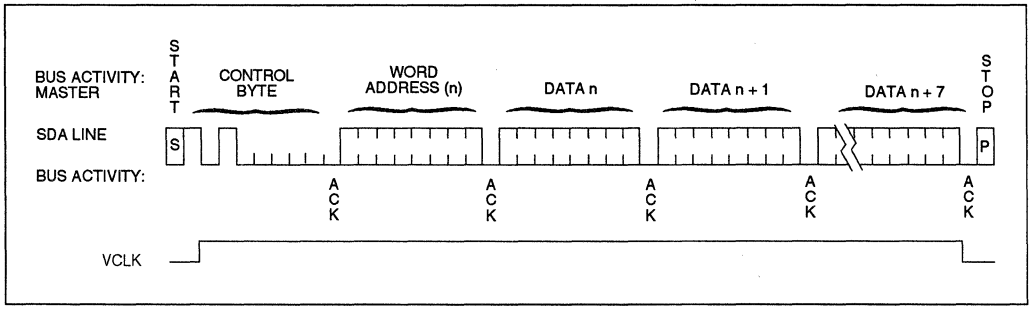


FIGURE 5-2: PAGE WRITE



6.0 WRITE PROTECTION

When using the 24LC21 in the Bi-Directional Mode, the VCLK pin operates as the write protect control pin. Setting VCLK high allows normal write operations, while setting VCLK low prevents writing to any location in the array. Connecting the VCLK pin to VSS would allow the 24LC21 to operate as a serial ROM, although this configuration would prevent using the device in the Transmit-Only Mode.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

7.1 Current Address Read

The 24LC21 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC21 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC21 discontinues transmission (see Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC21 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC21 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC21 discontinues transmission (see Figure 7-2).

5

FIGURE 7-1: CURRENT ADDRESS READ

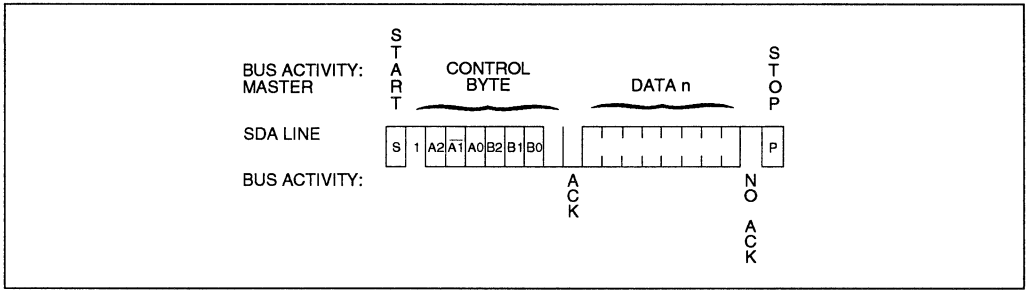
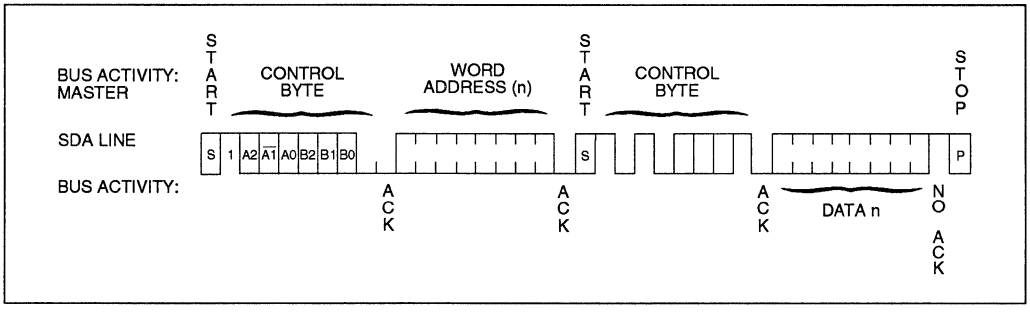


FIGURE 7-2: RANDOM READ



7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC21 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC21 to transmit the next sequentially addressed 8 bit word (see Figure 8-1).

To provide sequential reads the 24LC21 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC21 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

8.0 PIN DESCRIPTIONS

8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the Bi-Directional Mode. In the Transmit-Only Mode, which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer in the Bi-Directional Mode, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

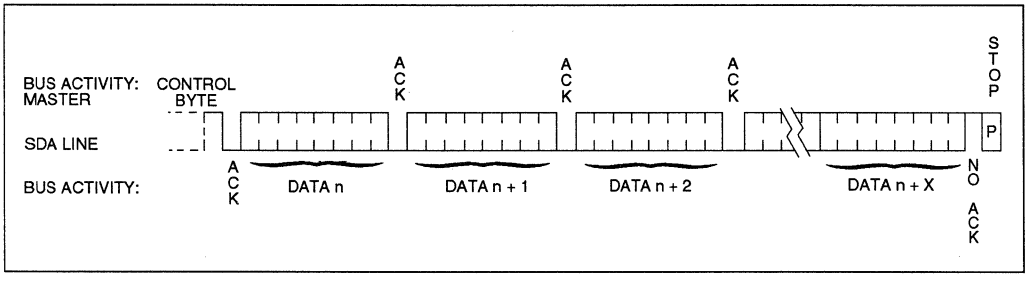
8.2 SCL

This pin is the clock input for the Bi-Directional Mode, and is used to synchronize data transfer to and from the device. It is also used as the signaling input to switch the device from the Transmit Only Mode to the Bi-Directional Mode. It must remain high for the chip to continue operation in the Transmit Only Mode.

8.3 VCLK

This pin is the clock input for the Transmit Only Mode. In the Transmit Only Mode, each bit is clocked out on the rising edge of this signal. In the Bi-Directional Mode, a high logic level is required on this pin to enable write capability.

FIGURE 8-1: SEQUENTIAL READ



NOTES

24LC21 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC21 - /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Device:	24LC21	Dual Mode Serial EEPROM
	24LC21T	Dual Mode Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

24AA65

64K 1.8V CMOS Smart Serial™ EEPROM

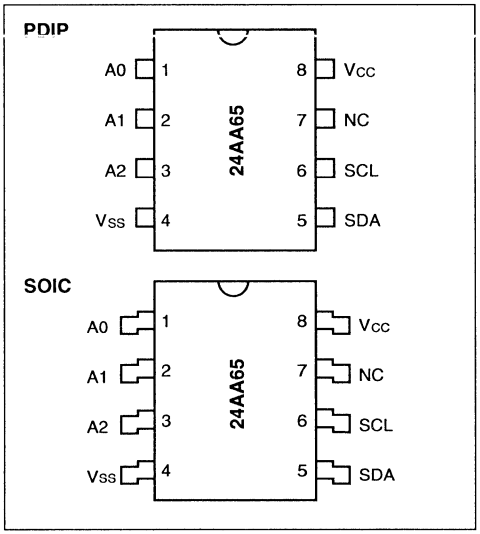
FEATURES

- Voltage operating range: 1.8V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA typical
- Industry standard two wire bus protocol I²C™ compatible
- Including 100 kHz (1.8V) and 400 kHz (5.0V) Modes
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE (E) and WRITE (W) cycles
- Power on/off data protection circuitry
- Endurance:
  - **10,000,000 E/W cycles guaranteed for a High Endurance Block**
  - **100,000 E/W cycles guaranteed for a Standard Endurance Block**
- 8 byte page, or byte modes available
- 1 page x 8 line input cache for fast write loads
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
- 2 ms typical write cycle time, byte or page
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory

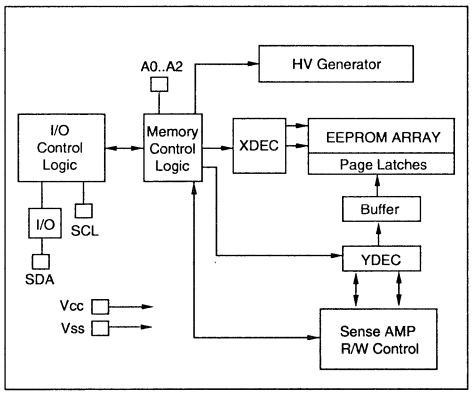
DESCRIPTION

The Microchip Technology Inc. 24AA65 is a "smart" 8K x 8 Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. It is capable of operation down to 1.8V, the end-of-life voltage for 2 "AA" battery cells for most popular battery technologies.The 24AA65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 100,000 ERASE/WRITE (E/W) cycles guaranteed. The 24AA65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K blocks.

PACKAGE TYPE



BLOCK DIAGRAM



Functional address lines allow the connection of up to eight 24LC65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24AA65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

I²C is a trademark of Philips Corporation. Smart Serial is a trademark of Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc 7.0V

All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V

Storage temperature ..... -65°C to+150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0.. A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+1.8V to 6.0V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			Vcc = +1.8V to +6.0V Commercial(C): Tamb = 0°C to +70°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating Current	Icc Write	—	3	mA	Vcc = 6.0V, SCL = 400 kHz
	Icc Read	—	150	µA	Vcc = 6.0V, SCL = 400 kHz
Standby current		—	5	µA	Vcc = 5.0V, SCL = SDA = Vcc Note 1
			2	µA	Vcc = 1.8V, SCL = SDA = Vcc Note 1

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

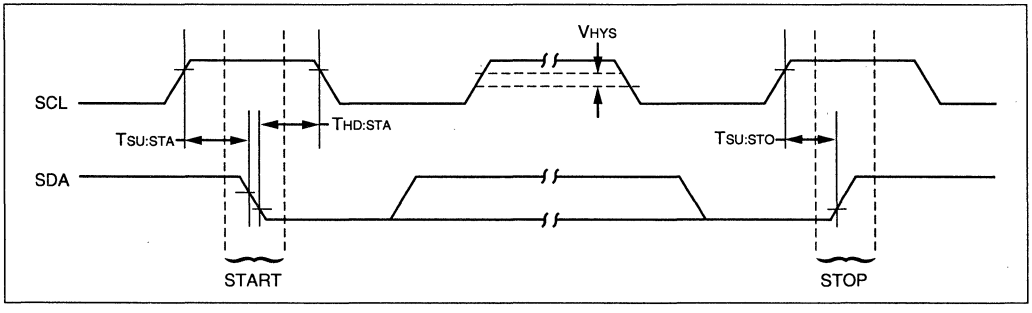
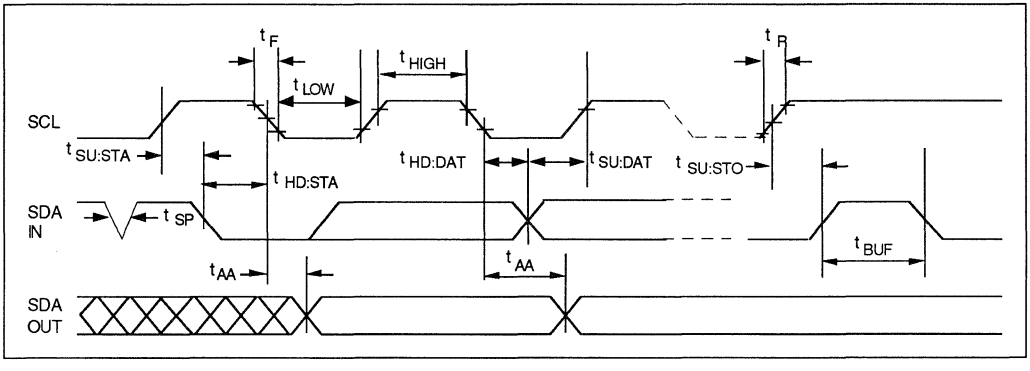


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 1.8V - 6.0V STD. MODE		Vcc = 4.5V - 6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time fro VIH min to VIL max	TOF	—	250	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/ page	Note 4

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.
Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.
Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24AA65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24AA65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

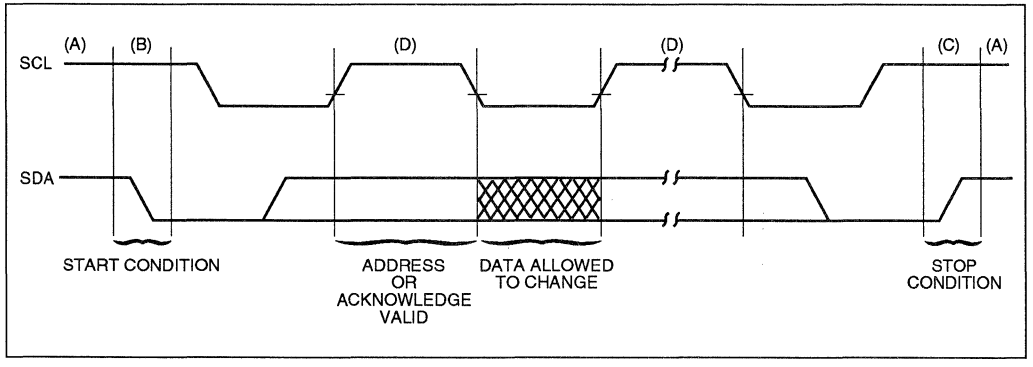
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24AA65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24AA65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



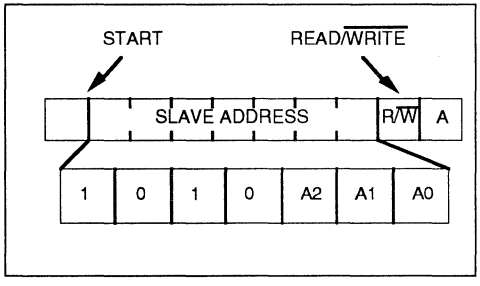
4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation (Figure 4-1)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24AA65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 5-1). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24AA65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24AA65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24AA65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

5.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24AA65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24AA65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24AA65 the master device will transmit the data word to be written into the addressed memory location. The 24AA65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24AA65 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24AA65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 5-2).

FIGURE 5-1: BYTE WRITE

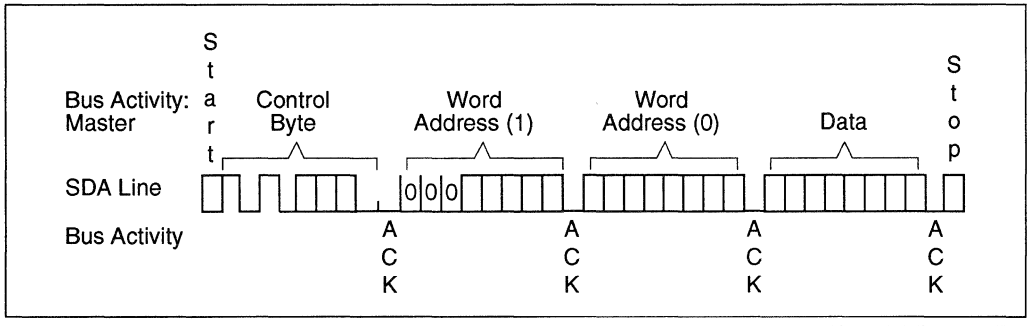


FIGURE 5-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 9-2)

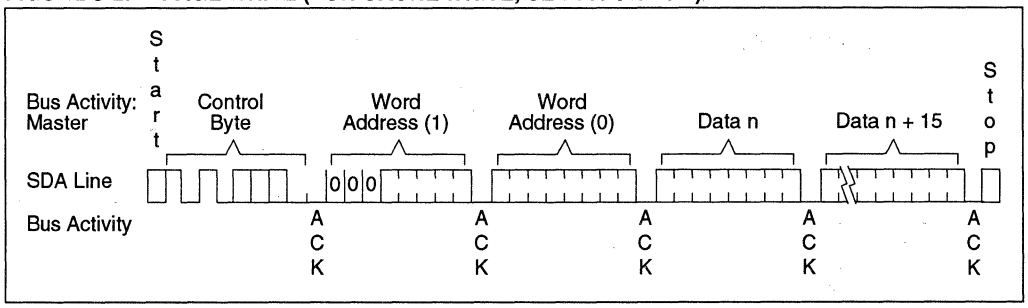


FIGURE 5-3: CURRENT ADDRESS READ

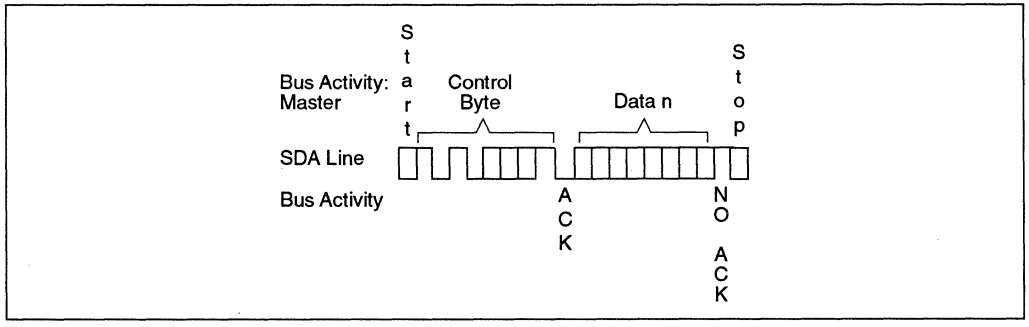


FIGURE 5-4: RANDOM READ

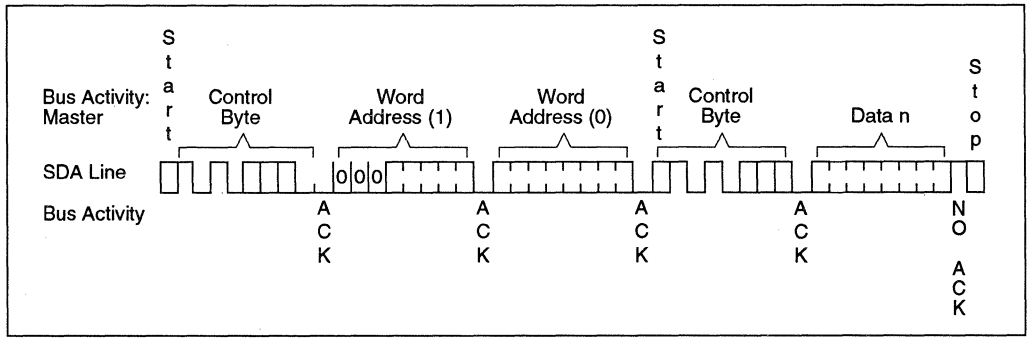
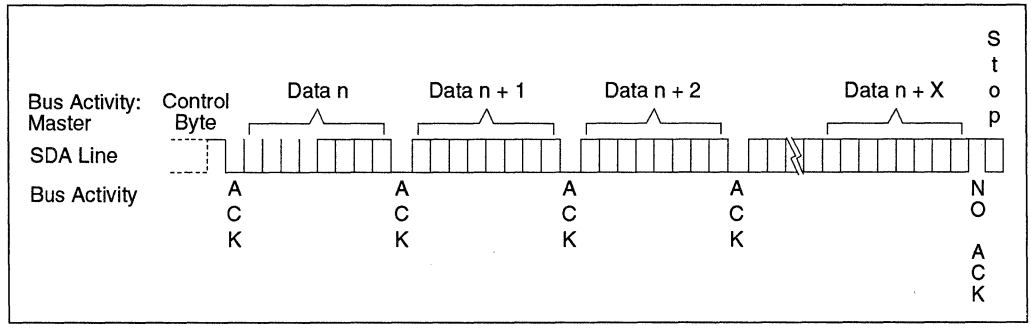


FIGURE 5-5: SEQUENTIAL READ



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

6.1 Current Address Read

The 24AA65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24AA65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24AA65 discontinues transmission (see Figure 5-3).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24AA65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24AA65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24AA65 to discontinue transmission (see Figure 5-4).

6.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24AA65 to transmit the next sequentially addressed 8 bit word (see Figure 5-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24AA65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

6.4 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24LC65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

6.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 kHz (Fast Mode) compatibility.

6.6 High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance. This block will be capable of 10,000,000 ERASE/WRITE cycles (see Figure 9-1).

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

6.7 Security Options

The 24AA65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. If the security option is invoked with 0 blocks protected, then all portions of the array will be unprotected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (see Figure 9-1). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/HE) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

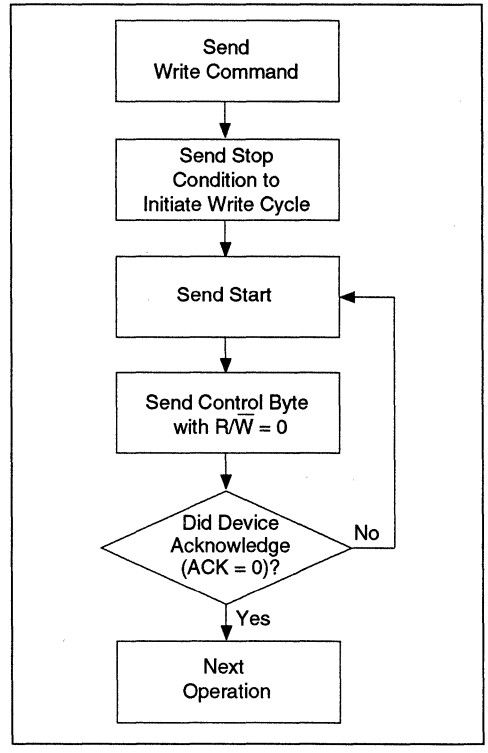
6.8 Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (see Figure 9-1).

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

8.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 9-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

8.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 9-3, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

8.3 Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

9.0 PIN DESCRIPTIONS

9.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24AA65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figure 4-1 and Figure 9-1).

9.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to VCC (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

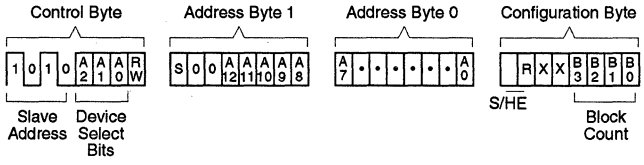
For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.3 SCL Serial Clock

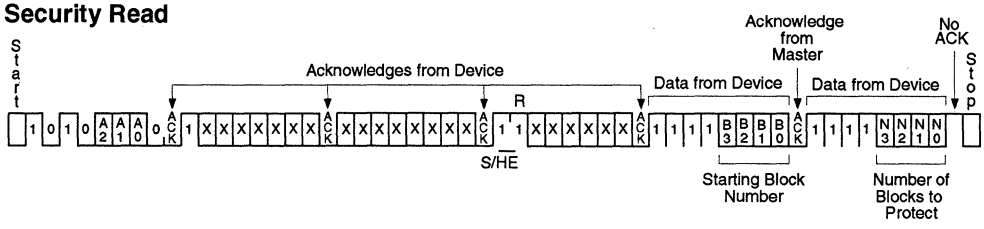
This input is used to synchronize the data transfer from and to the device.

5

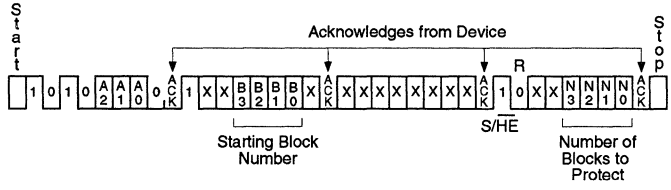
FIGURE 9-1: CONTROL SEQUENCE BIT ASSIGNMENTS



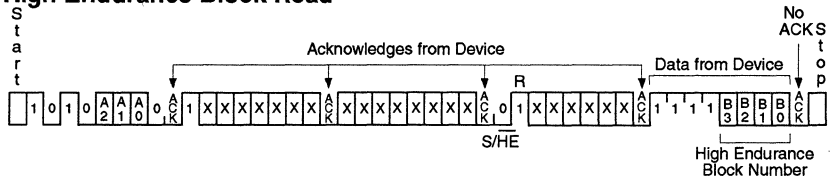
Security Read



Security Write



High Endurance Block Read



High Endurance Block Write

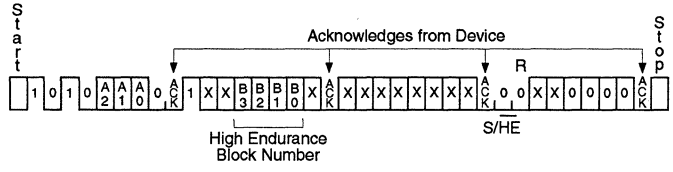


FIGURE 9-2: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

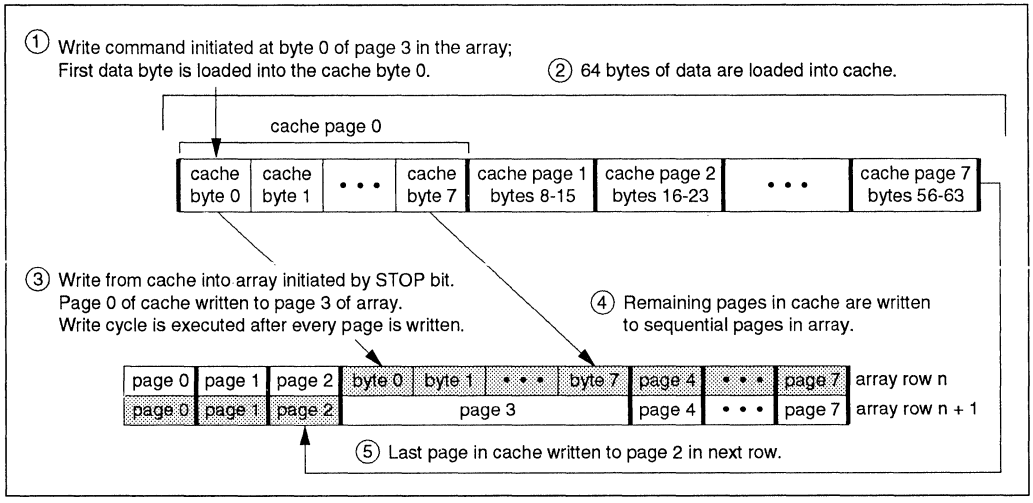
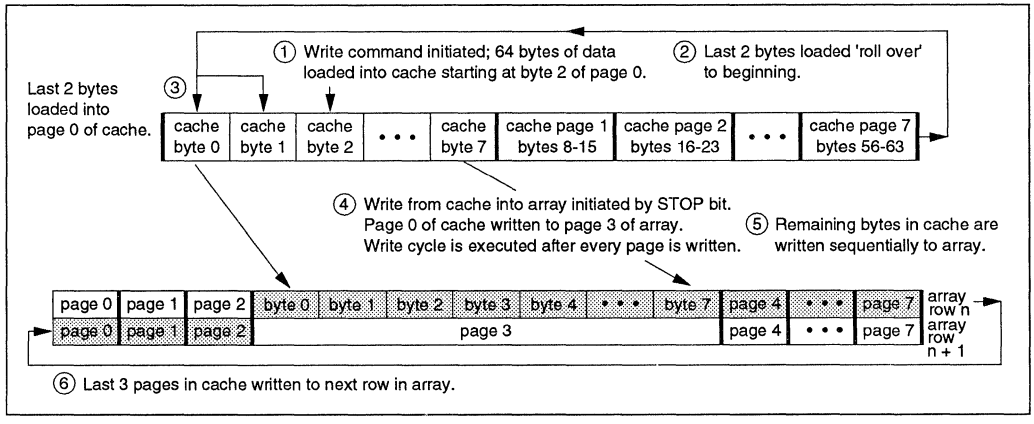


FIGURE 9-3: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



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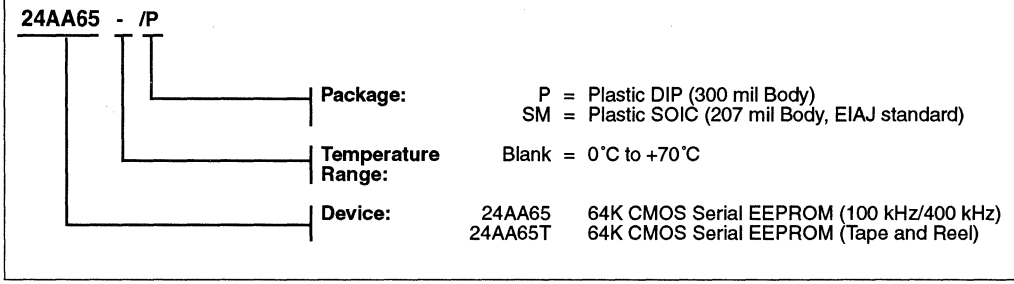
24AA65 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

24LC65

64K 2.5V CMOS Smart Serial™ EEPROM

FEATURES

- Voltage operating range: 2.5V to 6.0V
  - Peak write current 3 mA at 6.0V
  - Maximum read current 150 µA at 6.0V
  - Standby current 1 µA typical
- Industry standard two wire bus protocol I²C™ compatible
  - Including 100 kHz (2.5V) and 400 kHz (5.0V) Modes
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE (E) and WRITE (W) cycles
- Power on/off data protection circuitry
- Endurance:
  - **10,000,000 E/W cycles guaranteed for a High Endurance Block**
  - **100,000 E/W cycles guaranteed for a Standard Endurance Block**

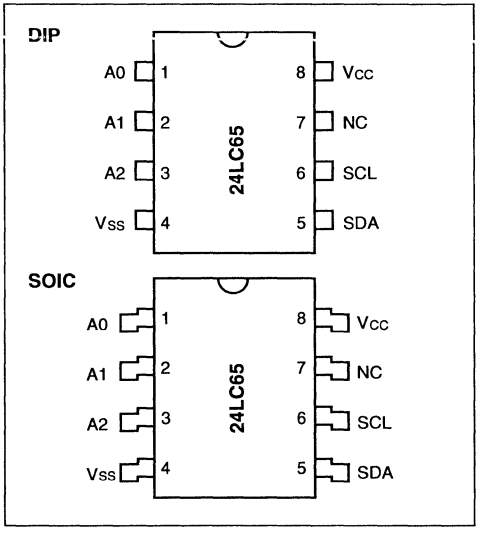
8 byte page, or byte modes available
1 page x 8 line input cache for fast write loads
Electrostatic discharge protection > 4000V
Data retention > 40 years
8-pin PDIP/SOIC packages
Temperature ranges:
- Commercial: 0°C to +70°C
- Industrial: -40°C to +85°C

- 2 ms typical write cycle time, byte or page
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory

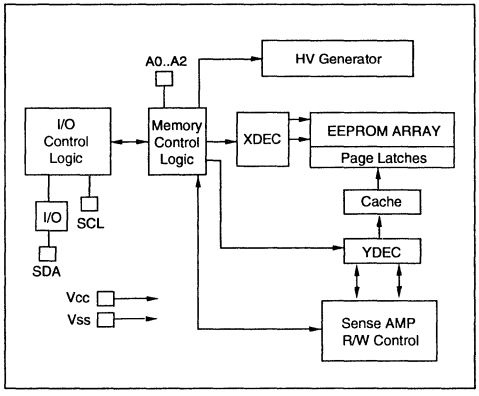
DESCRIPTION

The Microchip Technology Inc. 24LC65 is a "smart" 8K x 8 Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24LC65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 100,000 ERASE/WRITE (E/W) cycles guaranteed. The 24LC65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to fifteen 4K

PACKAGE TYPE



BLOCK DIAGRAM



blocks. Functional address lines allow the connection of up to eight 24LC65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24LC65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

I²C is a trademark of Philips Corporation.
Smart Serial is a trademark of Microchip Technology Inc.

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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V

All inputs and outputs w.r.t. Vss .....-0.6V to Vcc +1.0V

Storage temperature ..... -65°C to+150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0..A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data/I/O
SCL	Serial Clock
Vcc	+2.5V to 6.0V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

					Vcc = +2.5V to +6.0V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C
Parameter	**Sym**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE	—	3	mA	Vcc = 6.0V, SCL = 400 kHz
	ICC Read	—	150	µA	Vcc = 6.0V, SCL = 400 kHz
Standby current	ICCS	—	50	µA	Vcc = 5.0V, SCL = SDA = Vcc Note 1

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

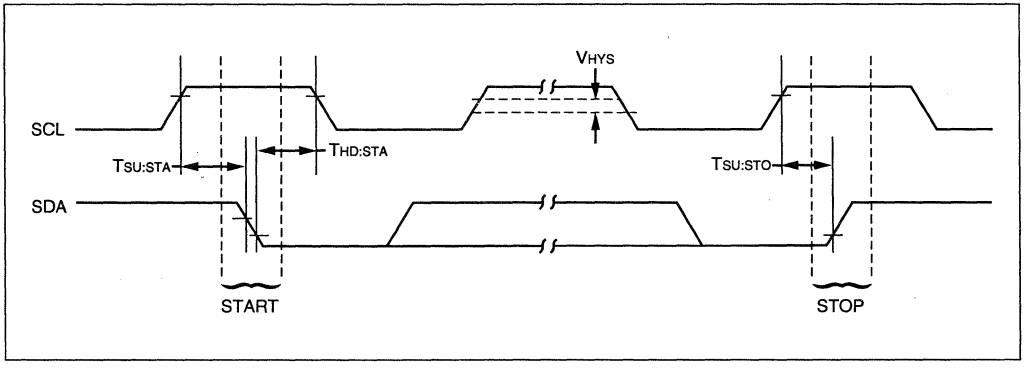
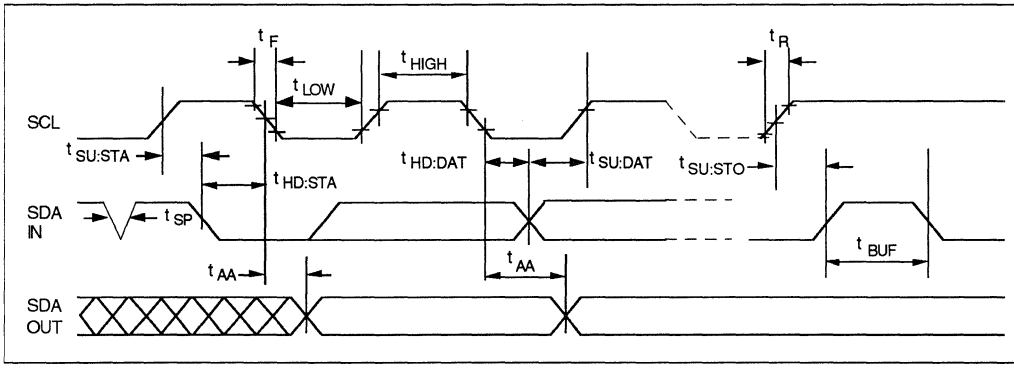


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 2.5V-6.0V STD. MODE		Vcc = 4.5-6.0V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	0	100	0	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	—	300	ns	Note 1
START condition setup time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	Note 2
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	N/A	N/A	0	50	ns	Note 3
Write cycle time	TWR	—	5	—	5	ms/page	Note 4

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.
Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.
Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

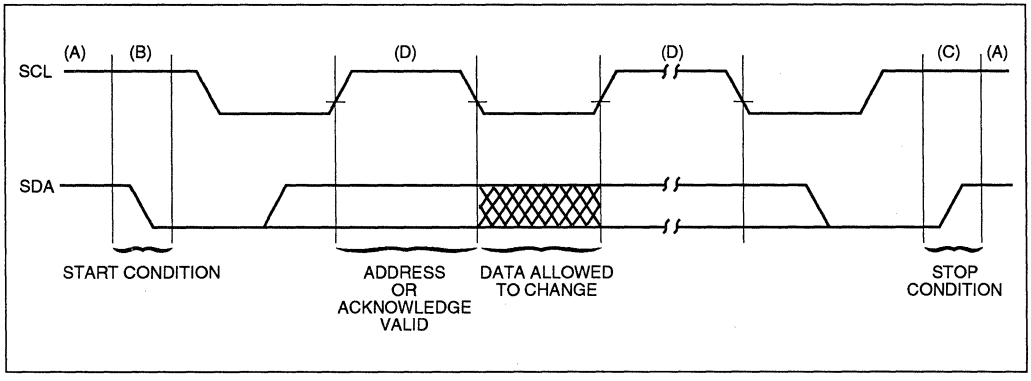
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



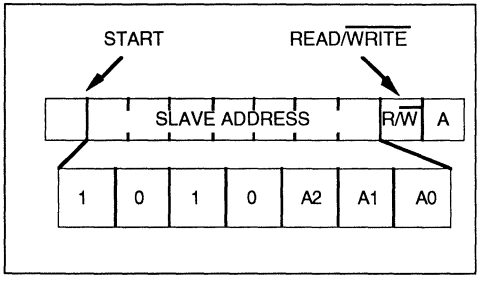
4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation (Figure 4-1)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24LC65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 5-1). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24LC65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24LC65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24LC65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

5.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24LC65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24LC65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24LC65 the master device will transmit the data word to be written into the addressed memory location. The 24LC65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC65 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24LC65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 5-2).

FIGURE 5-1: BYTE WRITE

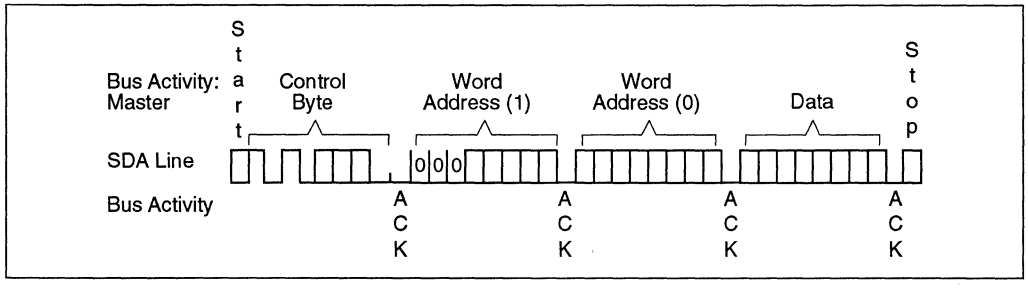


FIGURE 5-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 9-2)

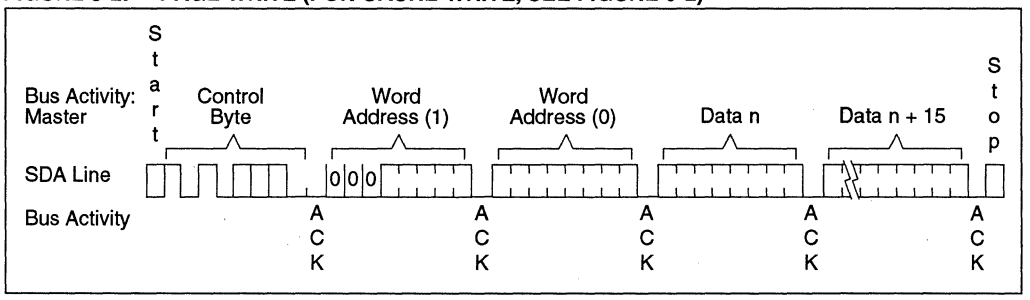


FIGURE 5-3: CURRENT ADDRESS READ

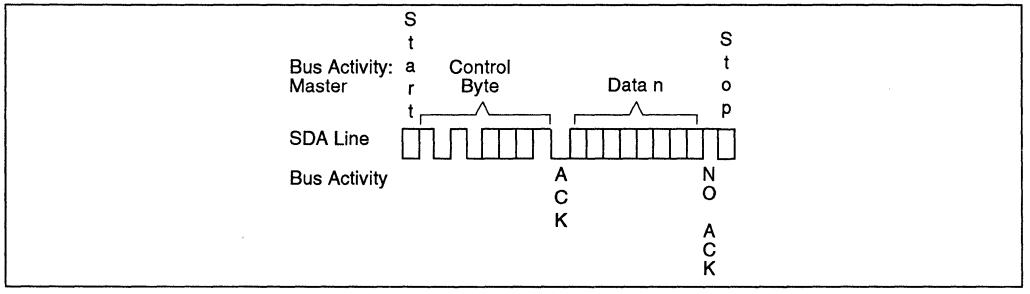


FIGURE 5-4: RANDOM READ

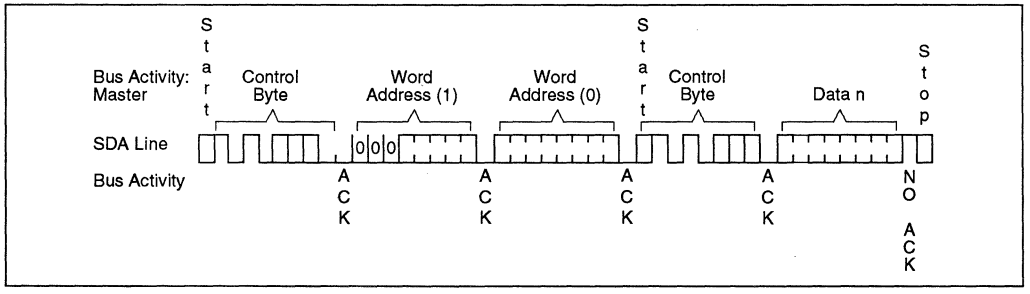
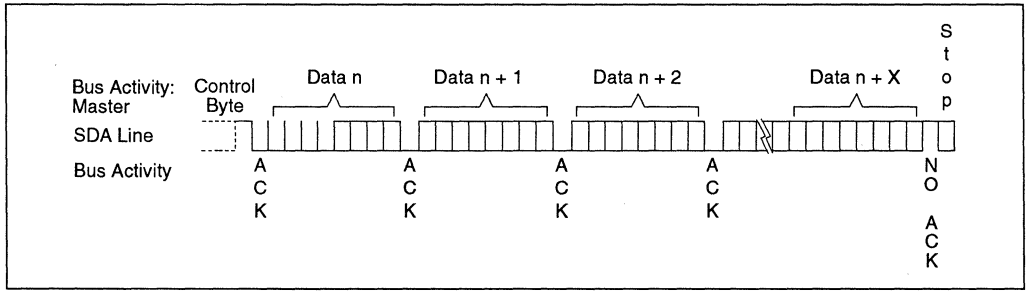


FIGURE 5-5: SEQUENTIAL READ



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

6.1 Current Address Read

The 24LC65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC65 discontinues transmission (see Figure 5-3).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24LC65 to discontinue transmission (see Figure 5-4).

6.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24LC65 to transmit the next sequentially addressed 8 bit word (see Figure 5-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24LC65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

6.4 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24LC65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

6.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

6.6 High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance. This block will be capable of 10,000,000 ERASE/WRITE cycles typical (see Figure 9-1).

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

5

6.7 Security Options

The 24LC65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. If the security option is invoked with 0 blocks protected, then all portions of the array will be unprotected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (see Figure 9-1). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/HE) set high and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

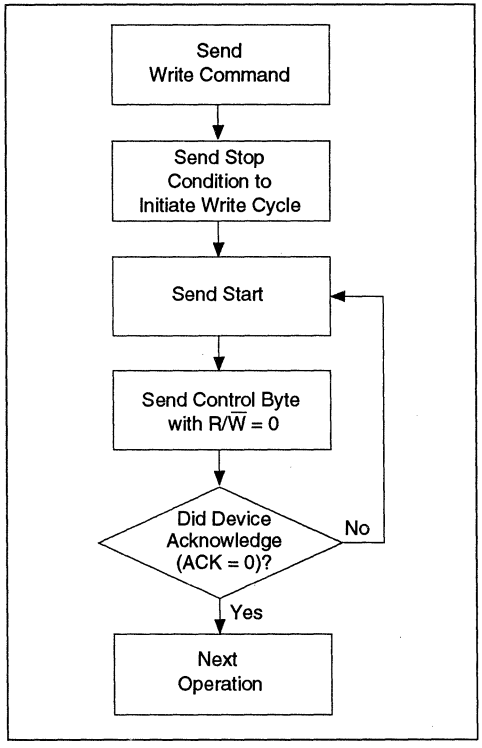
6.8 Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (see Figure 9-1).

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

8.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 9-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

8.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 9-3, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

8.3 Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates VDD monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The VDD monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

9.0 PIN DESCRIPTIONS

9.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24LC65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figure 4-1 and Figure 9-1).

9.2 SDA Serial Address/Data Input/Output

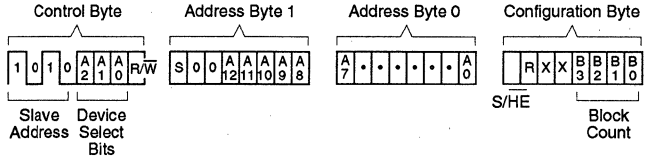
This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

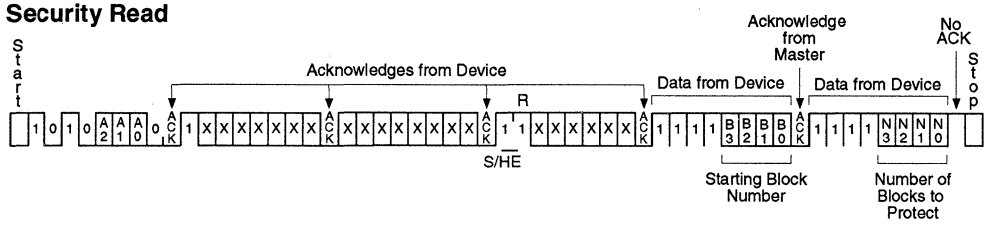
9.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

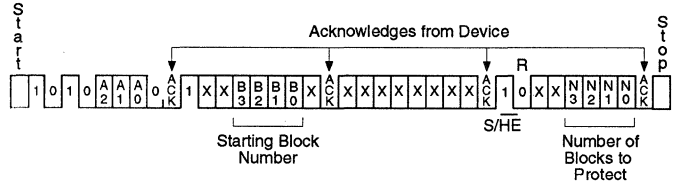
FIGURE 9-1: CONTROL SEQUENCE BIT ASSIGNMENTS



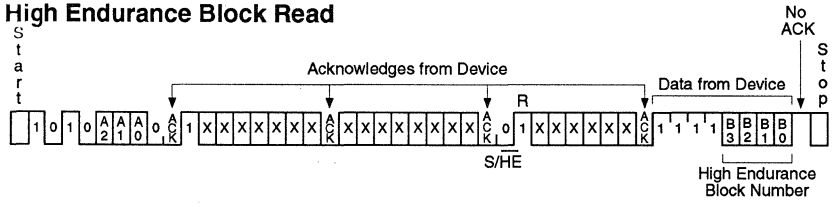
Security Read



Security Write



High Endurance Block Read



High Endurance Block Write

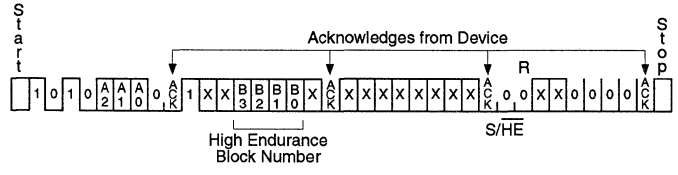


FIGURE 9-2: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

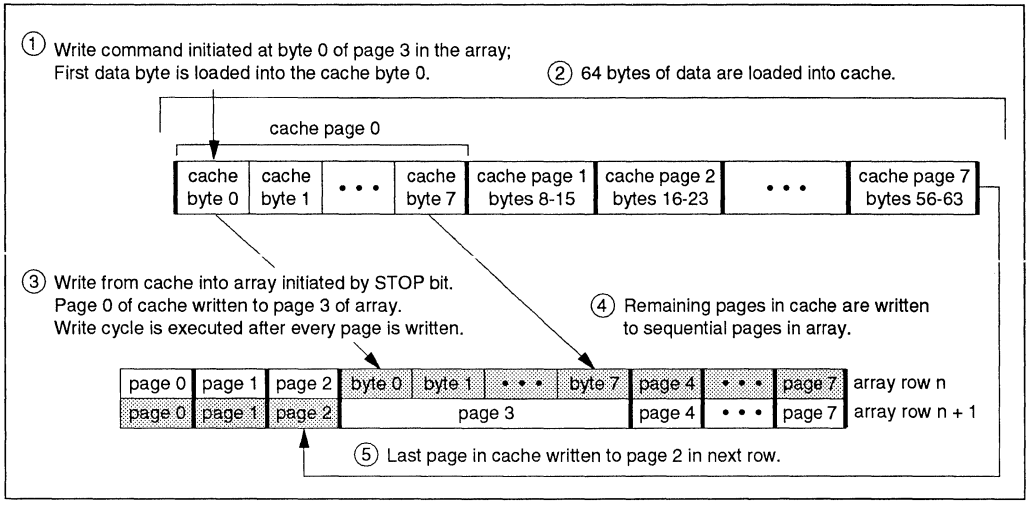
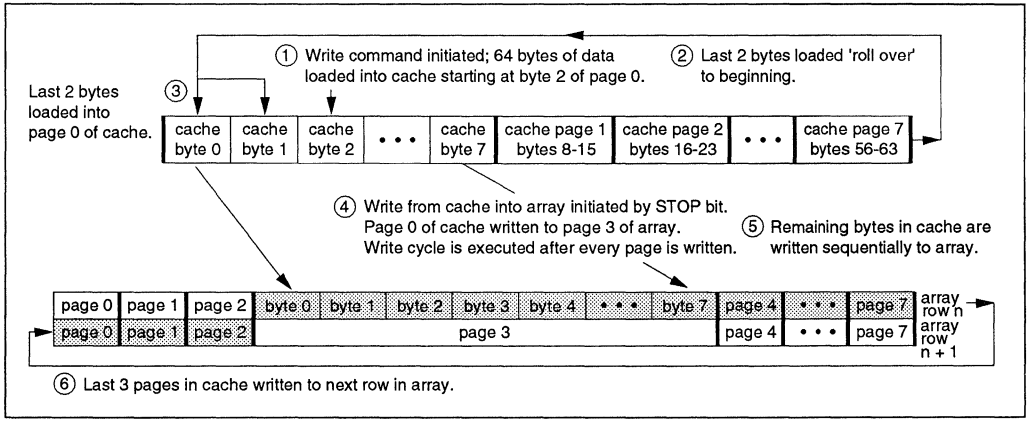


FIGURE 9-3: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



5

24LC65 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC65 - /P

Package:	P	=	Plastic DIP (300 mil Body)
	SM	=	Plastic SOIC (207 mil Body, EIAJ standard)
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
Device:	24LC65		64K CMOS Serial EEPROM (100 kHz/400kHz)
	24LC65T		64K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

24C65

64K 5.0V CMOS Smart Serial™ EEPROM

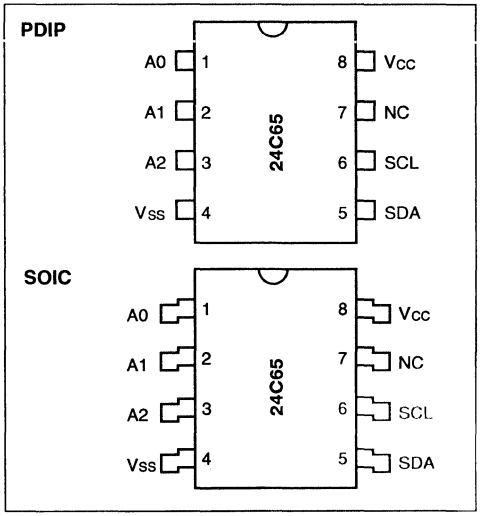
FEATURES

- Voltage operating range: 4.5V to 5.5V
  - Peak write current 3 mA at 5.5V
  - Maximum read current 150 µA at 5.5V
  - Standby current 1 µA typical
- Industry standard two wire bus protocol, I²C™ compatible
  - Including 400 KHz Mode
- Programmable block security options
- Programmable endurance options
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- Self-timed ERASE (E) and WRITE (W) cycles
- Power on/off data protection circuitry
- Endurance:
  - **10,000,000 E/W cycles guaranteed for High Endurance Block**
  - **100,000 E/W cycles guaranteed for a Standard Endurance Block**
- 8 byte page, or byte modes available
- 1 page x 8 line input cache for fast write loads
- Electrostatic discharge protection > 4000V
- Data retention > 40 years
- 8-pin PDIP/SOIC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- 2 ms typical write cycle time, byte or page
- Up to 8 devices may be connected to the same bus for up to 512K bits total memory

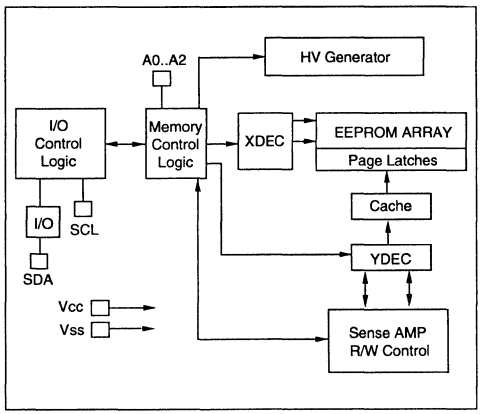
DESCRIPTION

The Microchip Technology Inc. 24C65 is a "smart" 8K x 8 Serial Electrically Erasable PROM (EEPROM). This device has been developed for advanced, low power applications such as personal communications, and provides the systems designer with flexibility through the use of many new user-programmable features. The 24C65 offers a relocatable 4K bit block of ultra-high-endurance memory for data that changes frequently. The remainder of the array, or 60K bits, is rated at 100,000 ERASE/WRITE (E/W) cycles guaranteed. The 24C65 features an input cache for fast write loads with a capacity of eight pages, or 64 bytes. This device also features programmable security options for E/W protection of critical data and/or code of up to

PIN CONFIGURATIONS



BLOCK DIAGRAM



fifteen 4K blocks. Functional address lines allow the connection of up to eight 24C65's on the same bus for up to 512K bits contiguous EEPROM memory. Advanced CMOS technology makes this device ideal for low-power nonvolatile code and data applications. The 24C65 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

I²C is a trademark of Philips Corporation
Smart Serial is a trademark of Microchip Technology, Inc.

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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc.....7.0V

All inputs and outputs w.r.t. Vss .... -0.6V to Vcc +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins .....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0..A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

TABLE 1-2: DC CHARACTERISTICS

			Vcc = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40° to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	Note 1
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V to Vcc
Output leakage current	ILO	-10	10	µA	VOUT = .1V to Vcc
Internal capacitance (all inputs/outputs)	CINT	—	10	pF	Vcc = 5.0V (Note 1) Tamb = 25°C, FCLK = 1 MHz
Operating current	Icc Write	—	3	mA	Vcc = 5.5V, SCL = 400 kHz
	Icc Read	—	150	µA	Vcc = 5.5V, SCL = 400 kHz
Standby current	Iccs	—	5	µA	Vcc = 5.5V, SCL = SDA =Vcc Note 1

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

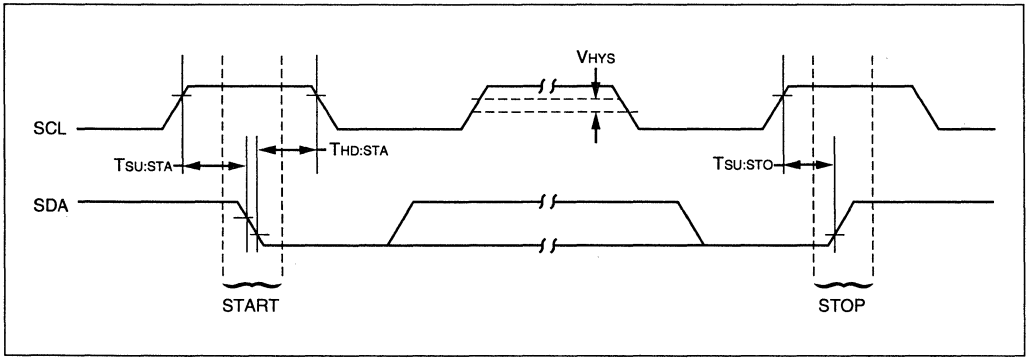
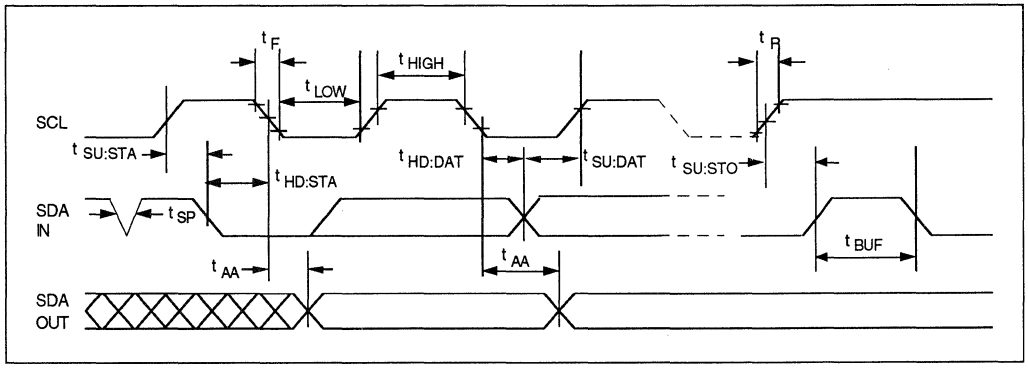


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 4.5V-5.5V		Units	Remarks
		Min	Max		
Clock frequency	FCLK	0	400	kHz	
Clock high time	THIGH	600	—	ns	
Clock low time	TLOW	1300	—	ns	
SDA and SCL rise time	TR	—	300	ns	Note 1
SDA and SCL fall time	TF	—	300	ns	Note 1
START condition hold time	THD:STA	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	ns	
Data input setup time	TSU:DAT	100	—	ns	
STOP condition setup time	TSU:STO	600	—	ns	
Output valid from clock	TAA	—	900	ns	Note 2
Bus free time	TBUF	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	20 +0.1 CB	250	ns	Note 1, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	0	50	ns	Note 3
Write cycle time	TWR	—	5	ms/page	Note 4

Note 1: Not 100 percent tested. CB = total capacitance of one bus line in pF.
Note 2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
Note 3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.
Note 4: The times shown are for a single page of 8 bytes. Multiply by the number of pages loaded into the write cache for total time.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24C65 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C65 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (SeeFigure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device.

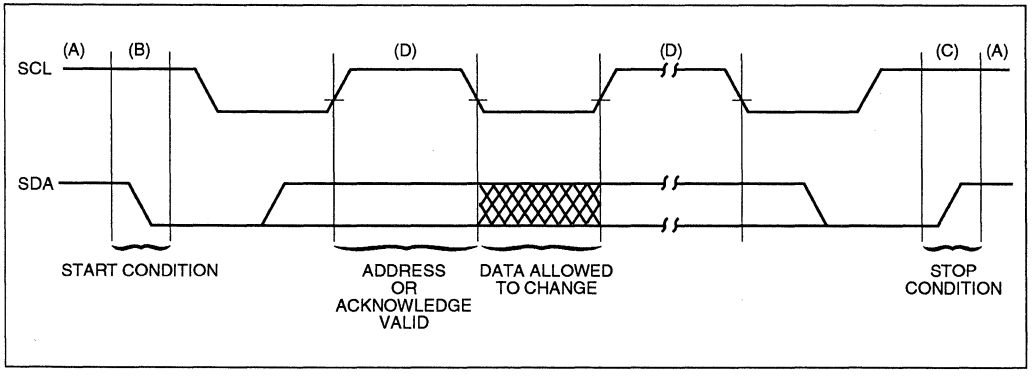
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C65 does not generate any acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C65) must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



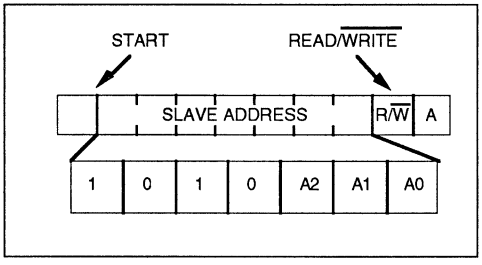
4.0 BUS CHARACTERISTICS

4.1 Device Addressing and Operation (Figure 4-1)

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24C65 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of the eight devices are to be accessed. These bits are in effect the three most significant bits of the word address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, when set to a zero a write operation is selected. The next two bytes received define the address of the first data byte (see Figure 5-1). Because only A12..A0 are used, the upper three address bits must be zeros. The most significant bit of the most significant byte is transferred first. Following the start condition, the 24C65 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a 1010 code and appropriate device select bits, the slave device (24C65) outputs an acknowledge signal on the SDA line. Depending upon the state of the R/$\overline{W}$ bit, the 24C65 will select a read or write operation.

Operation	Control Code	Device Select	R/$\overline{W}$
Read	1010	Device Address	1
Write	1010	Device Address	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

5.1 Byte Write

Following the start condition from the master, the control code (four bits), the device select (three bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver (24C65) that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the high-order byte of the word address and will be written into the address pointer of the 24C65. The next byte is the least significant address byte. After receiving another acknowledge signal from the 24C65 the master device will transmit the data word to be written into the addressed memory location. The 24C65 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C65 will not generate acknowledge signals (see Figure 5-1).

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C65 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight pages of eight data bytes each (64 bytes total) which are temporarily stored in the on-chip page cache of the 24C65. They will be written from the cache into the EEPROM array after the master has transmitted a stop condition. After the receipt of each word, the six lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remain constant. If the master should transmit more than eight bytes prior to generating the stop condition (writing across a page boundary), the address counter (lower three bits) will roll over and the pointer will be incremented to point to the next line in the cache. This can continue to occur up to eight times or until the cache is full, at which time a stop condition should be generated by the master. If a stop condition is not received, the cache pointer will roll over to the first line (byte 0) of the cache, and any further data received will overwrite previously captured data. The stop condition can be sent at any time during the transfer. As with the byte write operation, once the stop condition is received an internal write cycle will begin. The 64 byte cache will continue to capture data until a stop condition occurs or the operation is aborted (see Figure 5-2).

FIGURE 5-1: BYTE WRITE

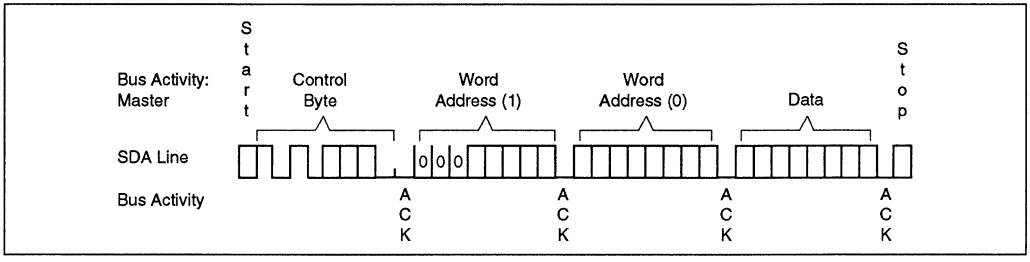


FIGURE 5-2: PAGE WRITE (FOR CACHE WRITE, SEE FIGURE 9-2)

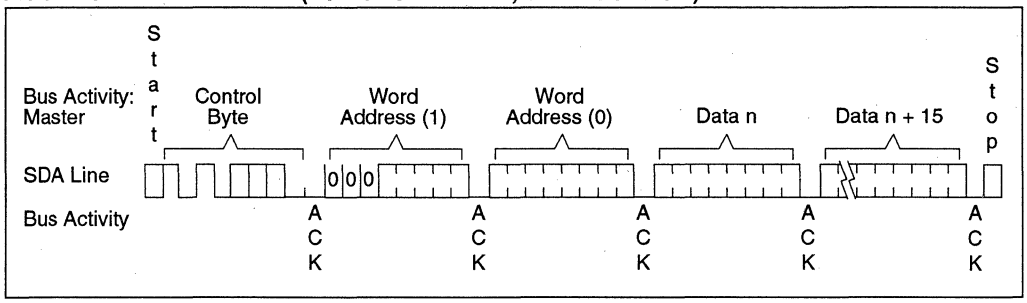


FIGURE 5-3: CURRENT ADDRESS READ

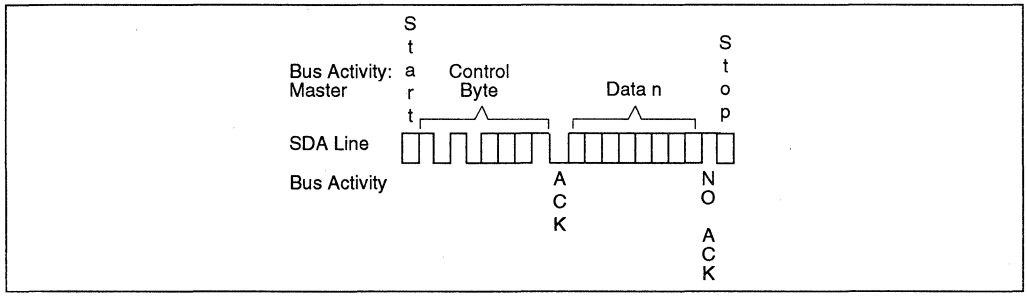


FIGURE 5-4: RANDOM READ

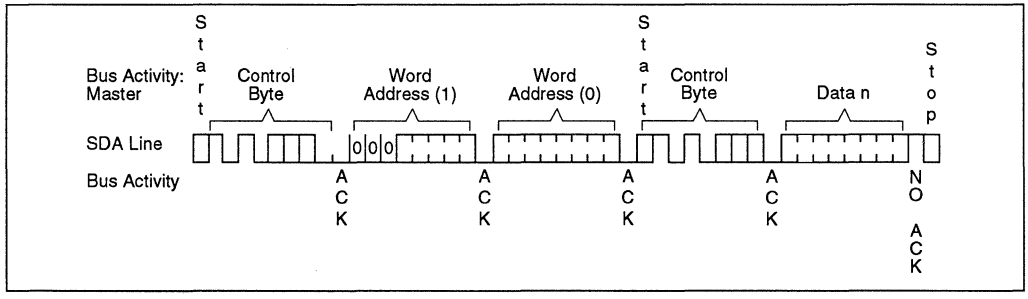
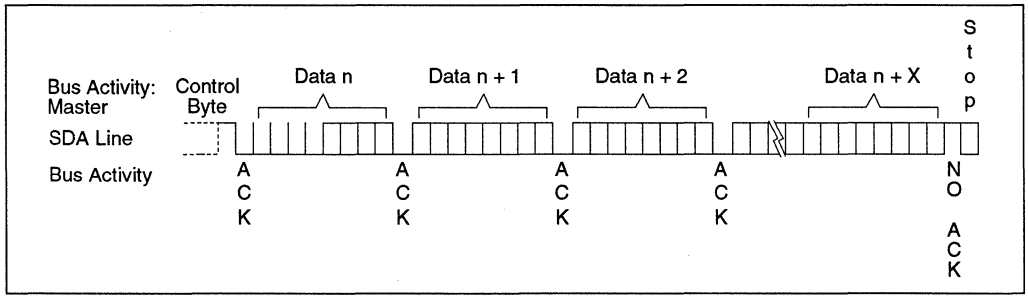


FIGURE 5-5: SEQUENTIAL READ



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

6.1 Current Address Read

The 24C65 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n (n is any legal address), the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C65 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C65 discontinues transmission (see Figure 5-3).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C65 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C65 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition which causes the 24C65 to discontinue transmission (see Figure 5-4).

6.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C65 transmits the first data byte, the master issues an acknowledge as opposed to the stop condition used in a random read. This acknowledge directs the 24C65 to transmit the next sequentially addressed 8 bit word (see Figure 5-5). Following the final byte transmitted to the master, the master will NOT generate an acknowledge but will generate a stop condition.

To provide sequential reads the 24C65 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

6.4 Contiguous Addressing Across Multiple Devices

The device select bits A2, A1, A0 can be used to expand the contiguous address space for up to 512K bits by adding up to eight 24C65's on the same bus. In this case, software can use A0 of the control byte as address bit A13, A1 as address bit A14, and A2 as address bit A15.

6.5 Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus. All I/O lines incorporate Schmitt triggers for 400 KHz (Fast Mode) compatibility.

6.6 High Endurance Block

The location of the high-endurance block within the memory map is programmed by setting the leading bit 7 (S/$\overline{HE}$) of the configuration byte to 0. The upper bits of the address loaded in this command will determine which 4K block within the memory map will be set to high endurance (see Figure 9-1). This block will be capable of 10,000,000 erase/write cycles.

Note: The High Endurance Block cannot be changed after the security option has been set. If the H.E. block is not programmed by the user, the default location is the highest block of memory.

6.7 Security Options

The 24C65 has a sophisticated mechanism for write-protecting portions of the array. This write protect function is programmable and allows the user to protect 0-15 contiguous 4K blocks. The user sets the security option by sending to the device the starting block number for the protected region and the number of blocks to be protected. If the security option is invoked with 0 blocks protected, then all portions of the array will be unprotected. All parts will come from the factory in the default configuration with the starting block number set to 15 and the number of protected blocks set to zero. THE SECURITY OPTION CAN BE SET ONLY ONCE.

To invoke the security option, a write command is sent to the device with the leading bit (bit 7) of the first address byte set to a 1 (see Figure 9-1). Bits 1-4 of the first address byte define the starting block number for the protected region. For example, if the starting block number is to be set to 5, the first address byte would be 1XX0101X. Bits 0, 5 and 6 of the first address byte are disregarded by the device and can be either high or low. The device will acknowledge after the first address byte. A byte of don't care bits is then sent by the master, with the device acknowledging afterwards. The third byte sent to the device has bit 7 (S/$\overline{HE}$) set high

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and bit 6 (R) set low. Bits 4 and 5 are don't cares and bits 0-3 define the number of blocks to be write protected. For example, if three blocks are to be protected, the third byte would be 10XX0011. After the third byte is sent to the device, it will acknowledge and a STOP bit is then sent by the master to complete the command.

During a normal write sequence, if an attempt is made to write to a protected address, no data will be written and the device will not report an error or abort the command. If a write command is attempted across a secure boundary, unprotected addresses will be written and protected addresses will not.

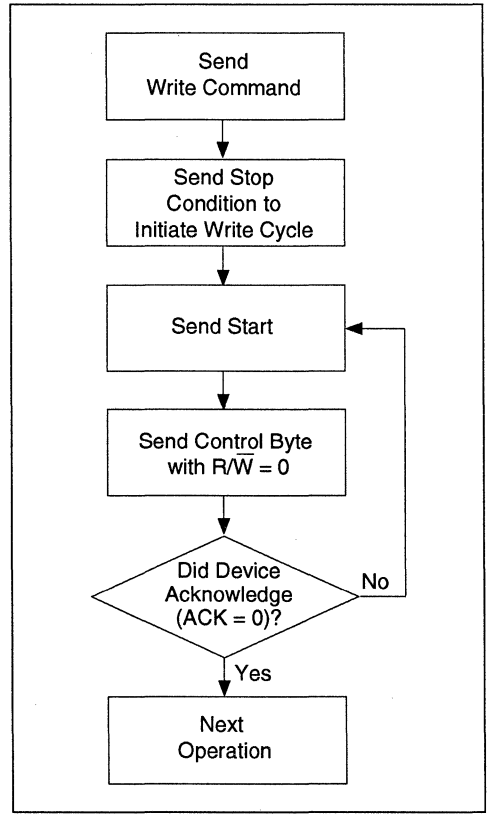
6.8 Security Configuration Read

The status of the secure portion of memory can be read by using the same technique as programming this option except the READ bit (bit 6) of the configuration byte is set to a one. After the configuration byte is sent, the device will acknowledge and then send two bytes of data to the master just as in a normal read sequence. The master must acknowledge the first byte and not acknowledge the second, and then send a stop bit to end the sequence. The upper four bits of both of these bytes will always be read as '1's. The lower four bits of the first byte contains the starting secure block. The lower four bits of the second byte contains the number of secure blocks. The default starting secure block is fifteen and the default number of secure blocks is zero (see Figure 9-1).

7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 PAGE CACHE AND ARRAY MAPPING

The cache is a 64 byte (8 pages x 8 bytes) FIFO buffer. The cache allows the loading of up to 64 bytes of data before the write cycle is actually begun, effectively providing a 64-byte burst write at the maximum bus rate. Whenever a write command is initiated, the cache starts loading and will continue to load until a stop bit is received to start the internal write cycle. The total length of the write cycle will depend on how many pages are loaded into the cache before the stop bit is given. Maximum cycle time for each page is 5 ms. Even if a page is only partially loaded, it will still require the same cycle time as a full page. If more than 64 bytes of data are loaded before the stop bit is given, the address pointer will 'wrap around' to the beginning of cache page 0 and existing bytes in the cache will be overwritten. The device will not respond to any commands while the write cycle is in progress.

8.1 Cache Write Starting at a Page Boundary

If a write command begins at a page boundary (address bits A2, A1 and A0 are zero), then all data loaded into the cache will be written to the array in sequential addresses. This includes writing across a 4K block boundary. In the example shown below, (see Figure 9-2) a write command is initiated starting at byte 0 of page 3 with a fully loaded cache (64 bytes). The first byte in the cache is written to byte 0 of page 3 (of the array), with the remaining pages in the cache written to sequential pages in the array. A write cycle is executed after each page is written. Since the write begins at page 3 and 8 pages are loaded into the cache, the last 3 pages of the cache are written to the next row in the array.

8.2 Cache Write Starting at a Non-Page Boundary

When a write command is initiated that does not begin at a page boundary (i.e., address bits A2, A1 and A0 are not all zero), it is important to note how the data is loaded into the cache, and how the data in the cache is written to the array. When a write command begins, the first byte loaded into the cache is always loaded into page 0. The byte within page 0 of the cache where the load begins is determined by the three least significant address bits (A2, A1, A0) that were sent as part of the write command. If the write command does not start at byte 0 of a page and the cache is fully loaded, then the last byte(s) loaded into the cache will roll around to page 0 of the cache and fill the remaining empty bytes. If more than 64 bytes of data are loaded into the cache, data already loaded will be overwritten. In the example shown in Figure 9-3, a write command has been initiated starting at byte 2 of page 3 in the array with a fully loaded cache of 64 bytes. Since the cache started loading at byte 2, the last two bytes loaded into the cache will 'roll over' and be loaded into the first two bytes of page 0 (of the cache). When the stop bit is sent, page 0 of the cache is written to page 3 of the array. The remaining pages in the cache are then loaded sequentially to the array. A write cycle is executed after each page is written. If a partially loaded page in the cache remains when the STOP bit is sent, only the bytes that have been loaded will be written to the array.

8.3 Power Management

The design incorporates a power standby mode when not in use and automatically powers off after the normal termination of any operation when a stop bit is received and all internal functions are complete. This includes any error conditions, i.e. not receiving an acknowledge or stop condition per the two-wire bus specification. The device also incorporates V_{DD} monitor circuitry to prevent inadvertent writes (data corruption) during low-voltage conditions. The V_{DD} monitor circuitry is powered off when the device is in standby mode in order to further reduce power consumption.

9.0 PIN DESCRIPTIONS

9.1 A0, A1, A2 Chip Address Inputs

The A0..A2 inputs are used by the 24C65 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, A0) in the control byte (see Figure 4-1 and Figure 9-1).

9.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to V_{CC} (typical 10KΩ for 100 KHz, 1KΩ for 400 KHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

9.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

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FIGURE 9-1: CONTROL SEQUENCE BIT ASSIGNMENTS

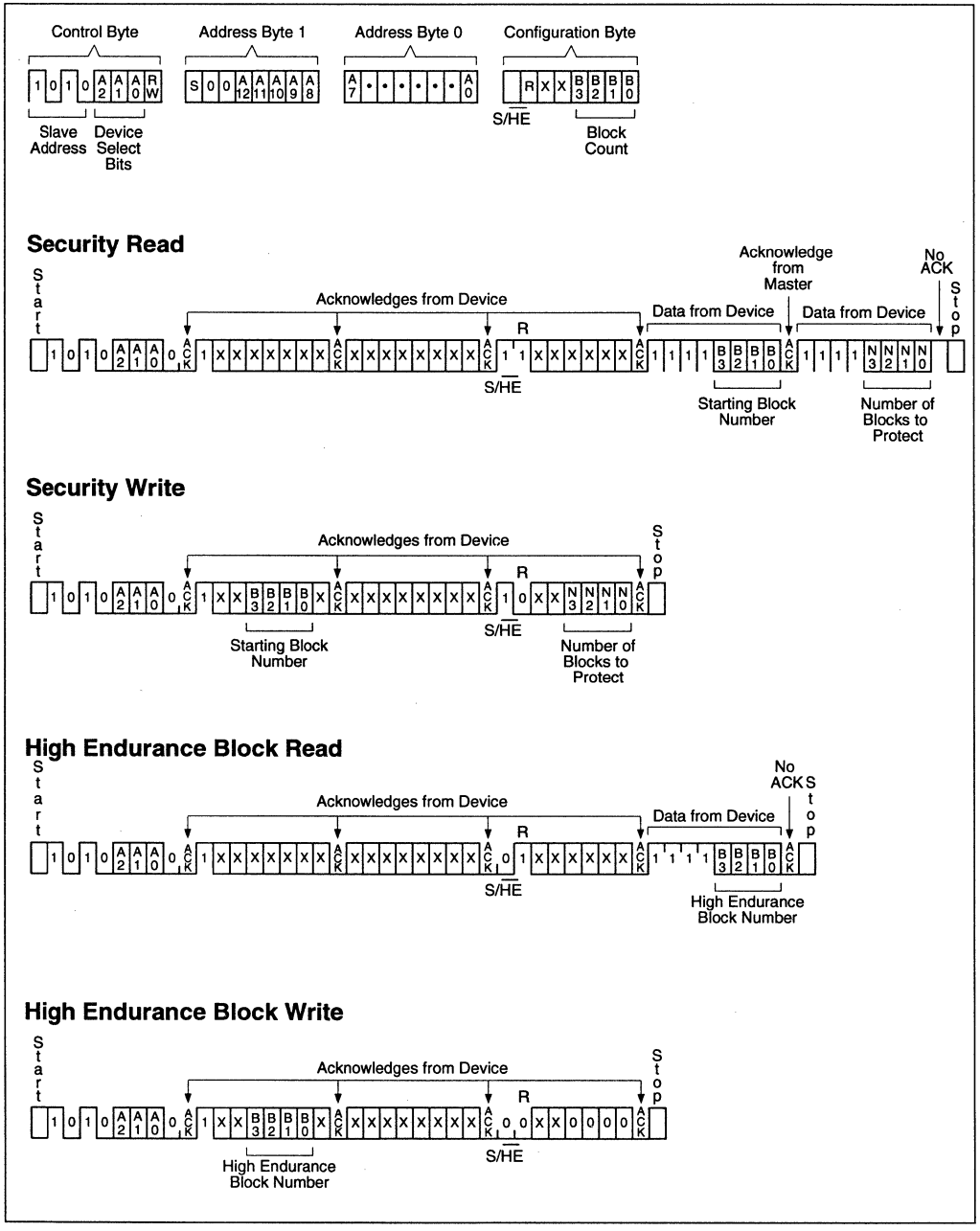


FIGURE 9-2: CACHE WRITE TO THE ARRAY STARTING AT A PAGE BOUNDARY

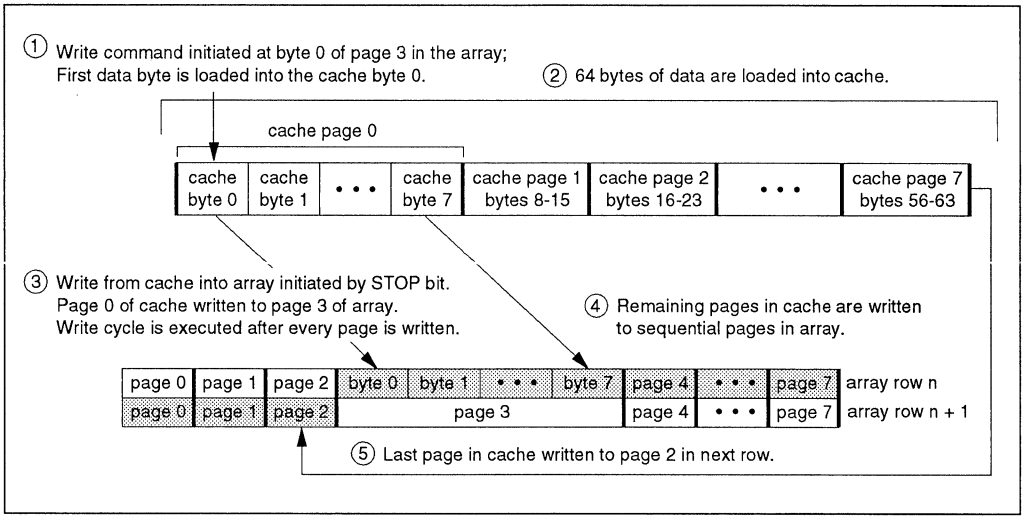
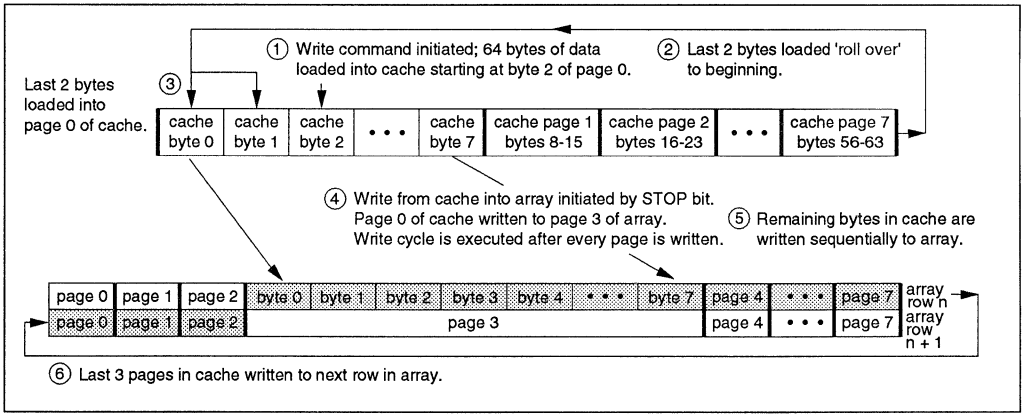


FIGURE 9-3: CACHE WRITE TO THE ARRAY STARTING AT A NON-PAGE BOUNDARY



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24C65 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24C65 - /P

Package:	P =	Plastic DIP (300 mil Body)
	SM =	Plastic SOIC (207 mil Body, EIAJ standard)
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Device:	24C65	64K CMOS Serial EEPROM (100 kHz/400kHz)
	24C65T	64K CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

59C11

1K 5.0V CMOS Serial EEPROM

FEATURES

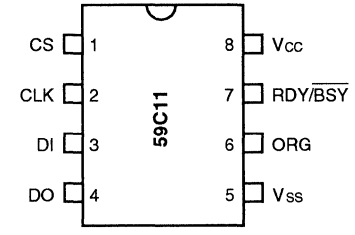
- Low power CMOS technology
- Pin selectable memory organization
  - 128 x 8 or 64 x 16 bit organization
- Single 5 volt only operation
- Self timed WRITE, ERAL and WRAL cycles
- Automatic erase before WRITE
- RDY/$\overline{BSY}$ status information during WRITE
- Power on/off data protection circuitry
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data Retention > 40 Years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

DESCRIPTION

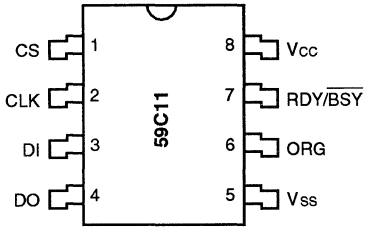
The Microchip Technology Inc. 59C11 is a 1K bit Electrically Erasable PROM. The device is configured as 128 x 8 or 64 x 16, selectable externally by means of the control pin ORG. Advanced CMOS technology makes this device ideal for low power nonvolatile memory applications. The 59C11 is available in the standard 8-pin DIP and a surface mount SOIC package.

PACKAGE TYPE

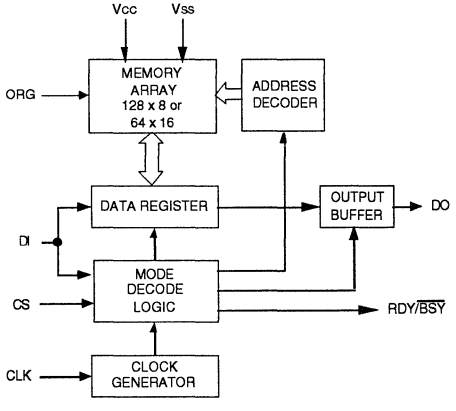
DIP



SOIC



BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V

All inputs and outputs w.r.t. VSS .... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temperature with power applied..... -65°C to +125°C

Soldering temperature of leads (10 seconds) .. +300°C

ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
VSS	Ground
ORG	Memory Array Organization
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Status
VCC	+5V Power SUpply

TABLE 1-2: DC CHARACTERISTICS

VCC = +5V (±10%)			Commercial: Tamb = 0°C to 70°C Industrial: Tamb = -40°C to +85°C Automotive: Tamb = -40°C to 125°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
VCC detector threshold	VTH	2.8	4.5	V	
High level input voltage	VIH	2.0	Vcc+1	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH	2.4	—	V	IOH = -400 µA
Low level output voltage	VOL	—	0.4	V	IOL = 3.2 mA
Input leakage current	ILI	—	10	µA	VIN = 0V to VCC (Note 1)
Output leakage current	ILO	—	10	µA	VOUT = 0V to VCC (Note 1)
Internal capacitance (all inputs/outputs)	CINT	—	7	pF	VIN/VOUT = 0V (Note 2) Tamb = 25°C, f = 1 MHz
Operating current (all modes)	ICC write	—	4	mA	FCLK = 1 MHz, VCC = 5.5V
Standby current	ICCS	—	100	µA	CS = 0V, VCC = 5.5V

Note 1: Internal resister pull-up at Pin 6. Active output at Pin 7.

Note 2: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: SYNCHRONOUS DATA TIMING

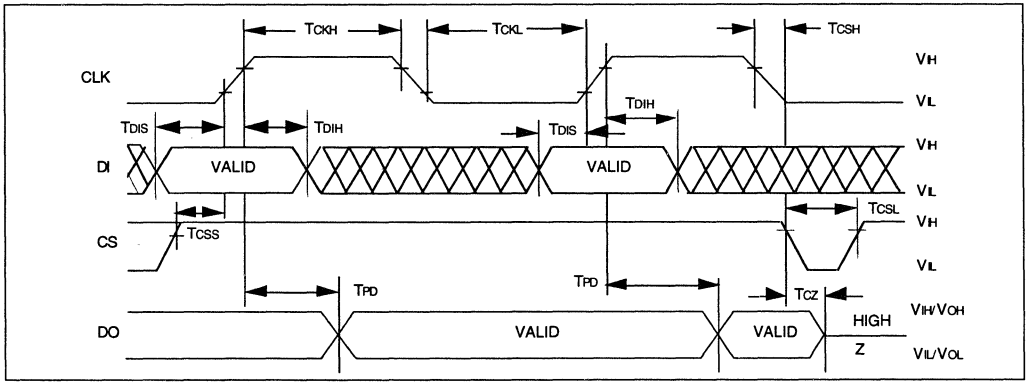


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500	—	ns	
Clock low time	TCKL	500	—	ns	
Chip select setup time	TCSS	50	—	ns	
Chip select hold time	TCSH	0	—	ns	
Chip select low time	TCS	100	—	ns	
Data input setup time	TDIS	100	—	ns	
Data input hold time	TDIH	100	—	ns	
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
RDY/$\overline{BSY}$ delay time	TRBD	—	400	ns	
Program cycle time (Auto Erase and Write)	Twc	—	1 15	ms ms	for 8-bit mode for ERAL and WRAL in 8/16-bit modes

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a WRITE cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a WRITE cycle, the device will go into standby mode as soon as the WRITE cycle is completed.

CS must be LOW for 100 ns (TCSL) minimum between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 59C11. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock high time (TCKH) and clock low time (TCKL)). This gives freedom in preparing opcode, address and data for the controlling master.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto erase/write) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). When that limit has been reached, CLK and DI become "Don't Care" inputs until CS is brought LOW for at least chip select low time (TCSL) and brought HIGH again and a WRITE cycle (if any) is completed.

2.3 Data In (DI)

Data In is used to clock in START bit, opcode, address and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK). This output is in HIGH–Z mode except if data is clocked out as a result of a READ instruction.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is output after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during WRITE cycles.

5

2.5 Organization (ORG)

This input selects the memory array organization. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization. In applications subject to electrical noise, it is recommended that this pin not be left floating, but tied either high or low.

2.6 Ready/Busy (RDY/$\overline{BSY}$)

Pin 7 provides RDY/$\overline{BSY}$ status information. RDY/BSY is low if the device is performing a WRITE, ERAL, or WRAL operation. When it is HIGH the internal, self-timed WRITE, ERAL or WRAL operation has been completed and the device is ready to receive a new instruction.

3.0 DATA PROTECTION

During power-up, all modes of operation are inhibited until Vcc has reached a level of 2.8 V. During power-down, the source data protection circuitry acts to inhibit all modes when Vcc has fallen below 2.8 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, EWEN instruction must be performed before any WRITE, ERAL or WRAL instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

TABLE 3-1: INSTRUCTION SET

6 X 16 MODE, ORG = 1						
Instruction	**Start Bit**	**Opcode**	**Address**	**Data In**	**Data Out**	**Number of Req. CLK CYcles**
READ	1	1 0 X X	A5 A4 A3 A2 A1 A0	—	D15-D0	27
WRITE	1	X 1 X X	A5 A4 A3 A2 A1 A0	D15-D0	High-Z	27
EWEN	1	0 0 1 1	X X X X X X	—	High-Z	11
EWDS	1	0 0 0 0	X X X X X X	—	High-Z	11
ERAL	1	0 0 1 0	X X X X X X	—	High-Z	11
WRAL	1	0 0 0 1	X X X X X X	D15-D0	High-Z	27
128 X 8 MODE, ORG = 0						
Instruction	**Start Bit**	**Opcode**	**Address**	**Data In**	**Data Out**	**Number of Req. CLK CYcles**
READ	1	1 0 X X	A6 A5 A4 A3 A2 A1 A0	—	D7-D0	20
WRITE	1	X 1 X X	A6 A5 A4 A3 A2 A1 A0	D7-D0	High-Z	20
EWEN	1	0 0 1 1	X X X X X X X	—	High-Z	12
EWDS	1	0 0 0 0	X X X X X X X	—	High-Z	12
ERAL	1	0 0 1 0	X X X X X X X	—	High-Z	12
WRAL	1	0 0 0 1	X X X X X X X	D7-D0	High-Z	20

4.0 FUNCTIONAL DESCRIPTION

4.1 START Condition

The START bit is detected by the device if CS and DI are both High with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition) without resulting in any device operation (READ, WRITE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e. clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

Note: CS must go LOW between consecutive instructions.

4.2 DI/DO Pins

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero"

that precedes the READ operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

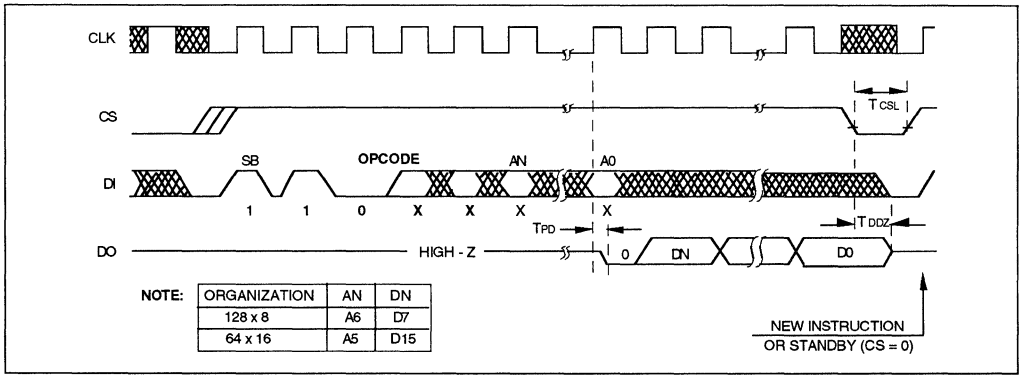
4.3 READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 8- or 16-bit output string. The output data changes during the high state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 is a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the negative edge of CS, whichever occurs first. D0 remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15 or D7) is always output first, followed by the lower significant bits (D14 - D0 or D6 - D0).

FIGURE 4-1: READ MODE



NOTE:

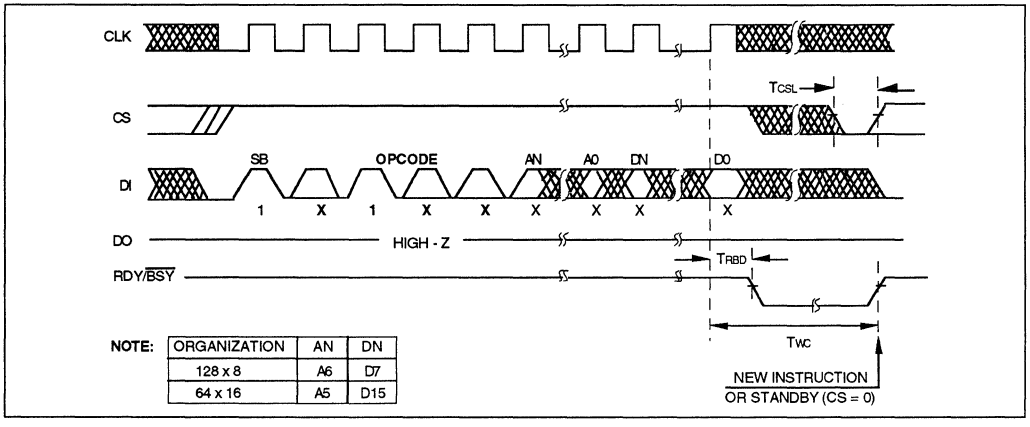
ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

4.4 WRITE

The WRITE instruction is followed by 8 or 16 bits of data which are written into the specified address. The most significant data bit (D15 or D7) has to be clocked in first followed by the lower significant data bits (D14 – D0 or D6 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic erase cycle on the specified address before the data are written. The WRITE cycle is completely self timed and commences automatically after the rising edge of the CLK signal for the last data bit (D0).

The WRITE cycle takes 1 ms maximum for 8-bit mode and 2 ms maximum for 16-bit mode.

FIGURE 4-2: WRITE MODE



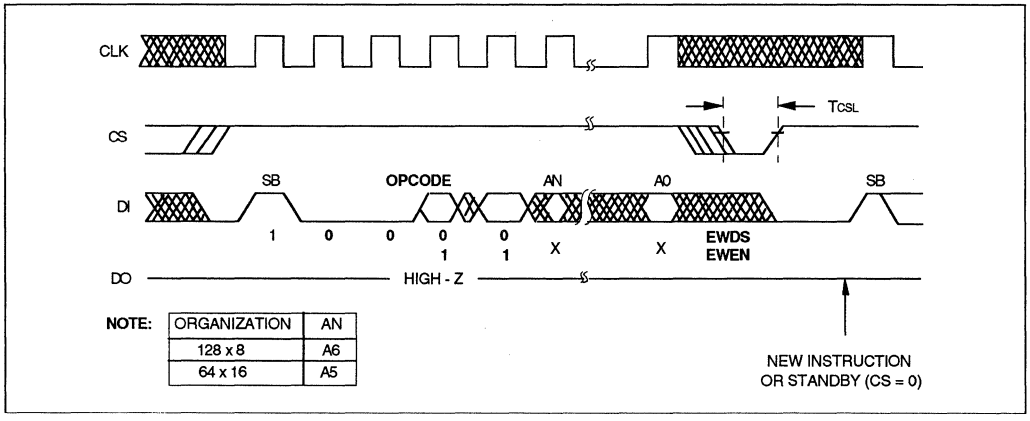
NOTE:

ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

4.5 ERASE/WRITE Enable/Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, EWEN instruction has to be performed before any WRITE, ERAL, or WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.

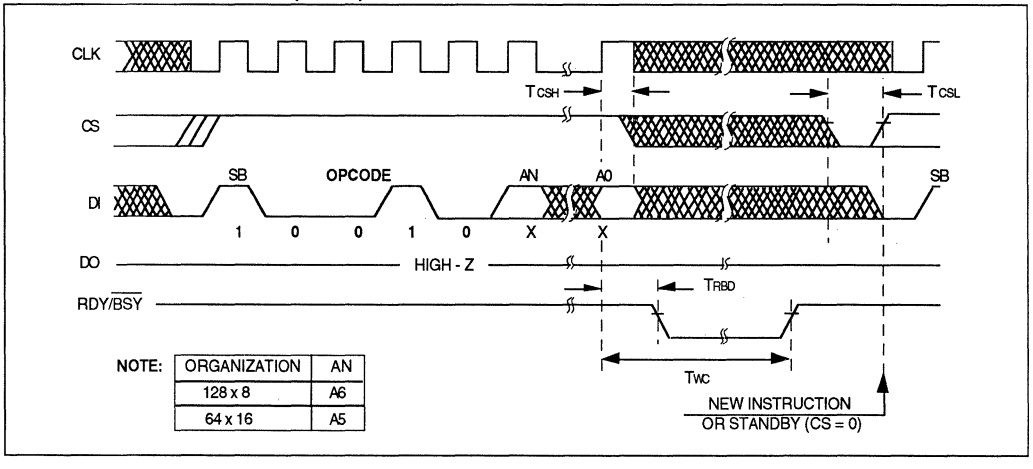
FIGURE 4-3: ERASE/WRITE ENABLE AND DISABLE



4.6 ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the rising edge of the CLK signal for the last dummy address bit. ERAL takes 15 ms maximum.

FIGURE 4-4: ERASE ALL (ERAL)

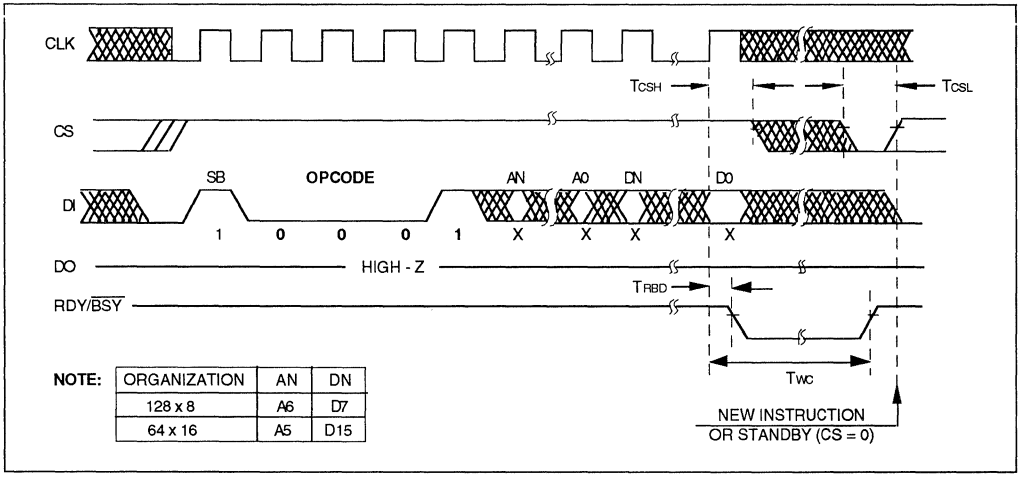


4.7 WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms maximum.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases. The WRAL instruction is used for testing and/or device initialization.

FIGURE 4-5: WRITE ALL



NOTE:

ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

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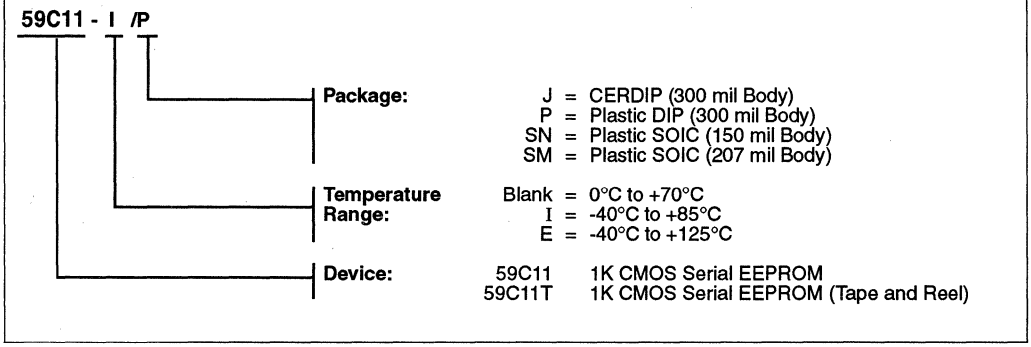
59C11 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

93LCS56/66

2K/4K 2.5V CMOS Serial EEPROM with Software Write Protect

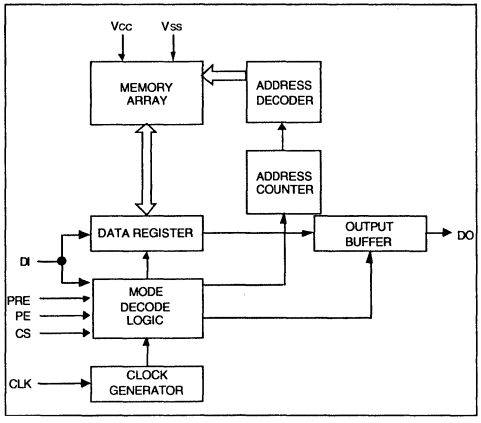
FEATURES

- Single supply with programming operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 5 µA standby current (typical) at 3.0V
- x16 memory organization
  - 128x16 (93LCS56)
  - 256x16 (93LCS66)
- Software write protection of user defined memory space
- Self timed erase and write cycles
- Automatic ERAL before WRAL
- Power on/off data protection
- Industry standard 3-wire serial I/O
- Device status signal during E/W
- Sequential READ function
- **1,000,000 E/W cycles guaranteed**
- Data retention > 40 years
- 8-pin PDIP/SOIC and 14-pin SOIC packages
- Commercial: 0°C to +70°C
- Industrial: -40°C to +85°C

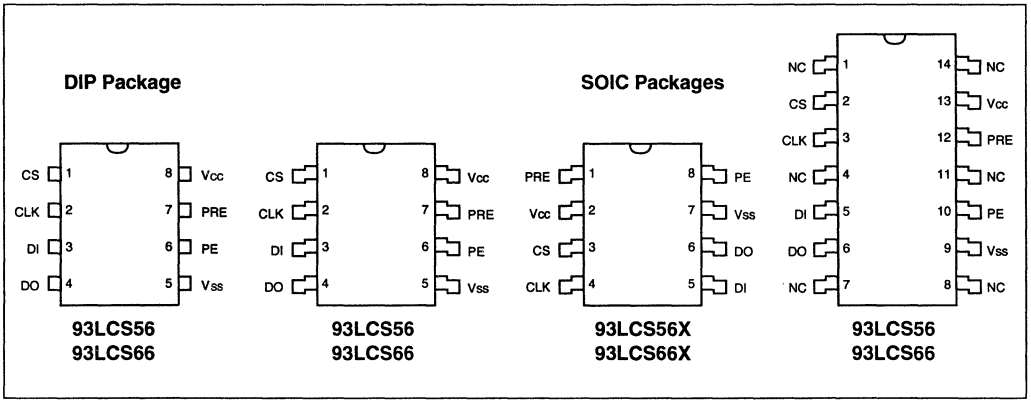
DESCRIPTION

The Microchip Technology Inc. 93LCS56/66 are low voltage Serial Electrically Erasable PROMs with memory capacities of 2K bits/4K bits respectively. A write protect register is included in order to provide a user defined region of write protected memory. All memory locations greater than or equal to the address placed in the write protect register will be protected from any attempted write or erase operation. It is also possible to protect the address in the write protect register permanently by using a one time only instruction (PRDS). Any attempt to alter data in a register whose address is equal to or greater than the address stored in the protect register will be aborted. Advanced CMOS technology makes this device ideal for low power non-volatile memory applications.

BLOCK DIAGRAM



PACKAGE TYPE



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .... -0.6V to VCC +1.0V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) .. +300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VSS	Ground
PE	Program Enable
PRE	Protect Register Enable
VCC	Power Supply

TABLE 1-2: DC AND AC ELECTRICAL CHARACTERISTICS

VCC = +2.5V to +6.0V
Commercial(C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min	Max	Units	Conditions
High level input voltage	VIH1	2.0	VCC +1	V	VCC ≥ 2.5V
	VIH2	0.7 VCC	VCC +1	V	VCC < 2.5V
Low level input voltage	VIL1	-0.3	0.8	V	VCC ≥ 2.5V
	VIL	-0.3	0.2 VCC	V	VCC < 2.5V
Low level output voltage	VOL1	—	0.4	V	IOL = 2.1 mA; VCC = 4.5V
	VOL2	—	0.2	V	IOL = 100 µA; VCC = 2.5V
High level output voltage	VOH1	2.4	—	V	IOH = -400µA; VCC = 4.5V
	VOH2	VCC-0.2	—	V	IOH = -100µA; VCC = 2.5V
Input leakage current	ILI	-10	10	µA	VIN = 0.1V to VCC
Output leakage current Internal capacitance	ILO CINT	-10 —	10 7	µA pF	VOUT = 0.1V to VCC VIN/VOUT = 0V (Note 1 & 3)
(all inputs/outputs)					Tamb = +25°C; FCLK = 1 MHz
Operating current	ICC Write	—	3	mA	FCLK = 2 MHz; VCC = 3.0V (Note 3)
	ICC Read	—	1 500	mA µA	FCLK = 2 MHz; VCC = 6.0V FCLK = 1 MHz; VCC = 3.0V
Standby current	ICCS	—	100 30	µA µA	CLK = CS = 0V; VCC = 6.0V CLK = CS = 0V; VCC = 3.0V
Clock frequency	FCLK	—	2 1	MHz MHz	VCC ≥ 4.5V VCC < 4.5V
Clock high time	TCKH	250	—	ns	
Clock low time	TCKL	250	—	ns	
Chip select setup time	TCSS	50	—	ns	Relative to CLK
Chip select hold time	TCSH	0	—	ns	Relative to CLK
Chip select low time	TCSL	250	—	ns	
PRE setup time	TPRES	100	—	ns	Relative to CLK
PE setup time	TPES	100	—	ns	Relative to CLK
PRE hold time	TPREH	0	—	ns	Relative to CLK
PE hold time	TPEH	500	—	ns	Relative to CLK
Data input setup time	TDIS	100	—	ns	Relative to CLK
Data input hold time	TDIH	100	—	ns	Relative to CLK
Data output delay time	TPD	—	400	ns	CL=100 pF

			Vcc = +2.5V to +6.0V Commercial(C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Data output disable time	TCZ	—	100	ns	CL=100 pF (Note 3)
Status valid time	TSV		500	ns	CL=100 pF
Program cycle time	TWC		10	ms	ERASE/WRITE mode (Note 2)
	TEC		15	ms	ERAL mode
	TWL		30	ms	WRAL mode

Note 1: This parameter is tested at Tamb = 25°C and FCLK = 1 MHz.
Note 2: Typical program cycle time is 4 ms per word.
Note 3: This parameter is periodically sampled and not 100% tested.

TABLE 1-3: INSTRUCTION SET FOR 93LCS56*/66

93LCS56/66 (x 16 organization)								
Instruction	**SB**	**Opcode**	**Address**	**Data In**	**Data Out**	**PRE**	**PE**	**Comments**
READ	1	10	A7 - A0*	—	D15-D0	0	X	Reads data stored in memory, starting at specified address.
EWEN	1	00	11XXXXXX	—	High-Z	0	1	Erase/Write Enable must precede all programming modes.
ERASE	1	11	A7 - A0*	—	(RDY/$\overline{BSY}$)		1	Erase data at specified address location if address is unprotected.
ERAL	1	00	10XXXXXX	—	(RDY/$\overline{BSY}$)	0	1	Erase all registers to "FF". Valid only when Protect Register is cleared.
WRITE	1	01	A7 - A0*	D15 - D0	(RDY/$\overline{BSY}$)	0	1	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15 - D0	(RDY/$\overline{BSY}$)	0	1	Writes all registers. Valid only when Protect Register is cleared.
EWDS	1	00	00XXXXXX	—	High-Z	0	X	Erase/Write Disable deactivates all programming instructions.
PRREAD	1	10	XXXXXXXX	—	A7-A0	1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX	—	High-Z	1	1	Must immediately precede PRCLEAR, PRWRITE and PRDS instructions.
PRCLEAR	1	11	11111111	—	(RDY/$\overline{BSY}$)	1	1	Clears the Protect Register such that all data are NOT write-protected.
PRWRITE	1	01	A7 - A0*	—	(RDY/$\overline{BSY}$)	1	1	Programs address into Protect Register. Thereafter, memory addresses greater than or equal to the address in Protect Register are write-protected.
PRDS	1	00	00000000	—	(RDY/$\overline{BSY}$)	1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

*Address A7 bit is a "don't card" on 93LCS56.

5

2.0 FUNCTIONAL DESCRIPTION

The 93LCS56/66 is organized as 128/256 registers by 16 bits. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a high-Z state except when reading data from the device, or when checking the ready/busy status during a programming operation. The ready/busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. The DO will enter the high-Z state on the falling edge of the CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both HIGH with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, WRAL, PRREAD, PREN, PRCLEAR, PRWRITE, and PRDS). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e., clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

2.2 DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic HIGH level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all programming modes of operation are inhibited until Vcc has reached a level greater than 1.4V. During power-down, the source data protection circuitry acts to inhibit all programming modes when Vcc has fallen below 1.4V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed.

3.0 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 16 bit output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

4.0 ERASE/WRITE ENABLE AND DISABLE

The 93LCS56/66 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. The PE pin MUST be held "high" while loading the EWEN instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device. To protect against accidental data disturb, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

5.0 ERASE

The ERASE instruction forces all data bits of the specified address to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle. The PE pin MUST be latched "high" during loading the ERASE instruction but becomes a "don't care" after loading the instruction.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been erased and the device is ready for another instruction. ERASE instruction is valid if specified address is unprotected.

The ERASE cycle takes 4 ms per word typical.

6.0 WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. After the last data bit is put on the DI pin, CS must be brought low before the next rising edge of the CLK clock. This falling edge of CS initiates the self-timed auto-erase and programming cycle. The PE pin MUST be latched "high" while loading the WRITE instruction but becomes a "don't care" thereafter.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns (TCSL) and before the entire write cycle is complete. DO at logical "0" indicates that programming is still in progress. DO at logical "1" indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction. WRITE instruction is valid only if specified address is unprotected.

The WRITE cycle takes 4 ms per word typical.

7.0 ERASE ALL

The ERAL instruction will erase the entire memory array to the logical "1". The ERAL cycle is identical to the ERASE cycle except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. PE pin MUST be held "high" while loading the instruction but becomes "don't care" thereafter. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ERAL instruction is guaranteed at VCC = 4.5 to 6V and valid only when Protect Register is cleared.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL) and before the entire write cycle is complete.

The ERAL cycle takes 15 ms maximum (8 ms typical).

8.0 WRITE ALL

The WRAL instruction will write the entire memory array with the data specified in the command. The WRAL cycle is completely self-timed and commences at the falling edge of the CS. PE pin MUST be held "high" while loading the instruction but becomes "don't care" thereafter. Clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status. The WRAL instruction is guaranteed at VCC = 4.5 to 6V and valid only when Protect Register is cleared.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

The WRAL cycle takes 30 ms maximum (16 ms typical).

Note: In order to execute either READ, EWEN, ERAL, WRITE, WRAL, or EWDS instructions, the Protect Register Enable (PRE) pin must be held LOW.

9.0 PROTECT REGISTER READ

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin MUST be held HIGH when loading the instruction and remains HIGH until CS goes LOW. A dummy zero bit precedes the 8-bit output string. The output data bits in the memory Protect Register will toggle on the rising edge of the CLK as in the READ mode.

10.0 PROTECT REGISTER ENABLE

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the device must be in the EWEN mode. Both PRE and PE pins MUST be held "high" while loading the instruction. The PREN instruction MUST immediately precede a PRCLEAR, PRWRITE, or PRDS instruction.

11.0 PROTECT REGISTER CLEAR

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables all registers for programming instructions such as ERASE, ERAL, WRITE, and WRAL. The PRE and PE pin MUST be held HIGH when loading the instruction. Thereafter, PRE and PE pins become "don't care". A PREN instruction must immediately precede a PRCLEAR instruction.

12.0 PROTECT REGISTER WRITE

The Protect Register Write (PRWRITE) instruction writes into the Protect Register the address of the first register to be protected. After this instruction is executed, all registers whose memory addresses are greater than or equal to the address pointer specified in the Protect register are protected from any programming instructions. Note that a PREN instruction must be executed before a PRWRITE instruction and, the Protect Register must be cleared (by a PRCLEAR instruction) before executing the PRWRITE instruction. The PRE and PE pins MUST be held HIGH while loading PRWRITE instruction. After the instruction is loaded, they become "don't care".

13.0 PROTECT REGISTER DISABLE

The Protect Register Disable (PRDS) instruction is a ONE TIME ONLY instruction to permanently set the address specified in the Protect Register. Any attempts to change the address pointer will be aborted. The PRE and PE pins MUST be held HIGH while loading PRDS instruction. After the instruction is loaded, they become "don't care". Note that a PREN instruction must be executed before a PRDS instruction.

14.0 PIN DESCRIPTION

14.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a programming cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

CS must be LOW for 250 ns minimum (TCSL) between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

14.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93LCS56/66. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime with respect to clock HIGH time (TCKH) and clock LOW time (TCKL). This gives the controlling master freedom in preparing opcode, address, and data.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a start condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). CLK and DI then become don't care inputs waiting for a new start condition to be detected.

Note:	CS must go LOW between consecutive instructions.

14.3 Data In (DI)

Data In is used to clock in a START bit, opcode, address, and data synchronously with the CLK input.

14.4 Data Out (DO)

Data Out is used in the READ and PRREAD mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought HIGH after held LOW for minimum chip select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The status signal is not available on DO, if CS is held LOW or HIGH during the entire WRITE or ERASE cycle. In all other cases DO is in the HIGH-Z mode. If status is checked after the WRITE/ERASE cycle, a pull-up resistor on DO is required to read the READY signal.

14.5 Program Enable (PE)

This pin should be held HIGH in the programming mode or when executing the Protect Register programming instructions.

14.6 Protect Register Enable (PRE)

This pin should be held HIGH when executing all Protect Register instructions. Otherwise, it must be held LOW for normal operations.

FIGURE 14-1: SYNCHRONOUS DATA TIMING

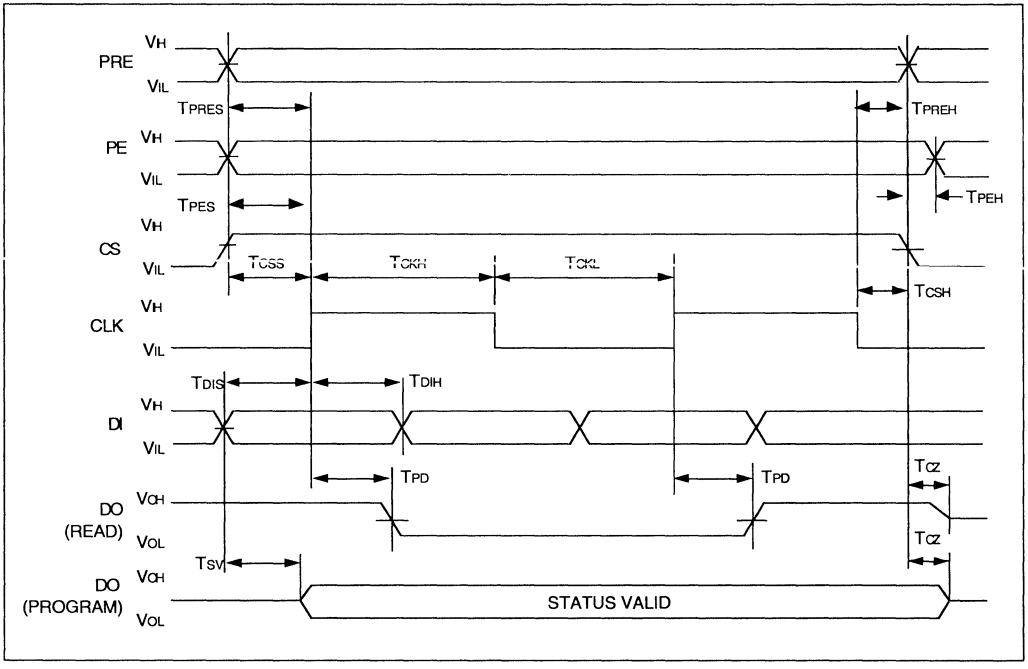
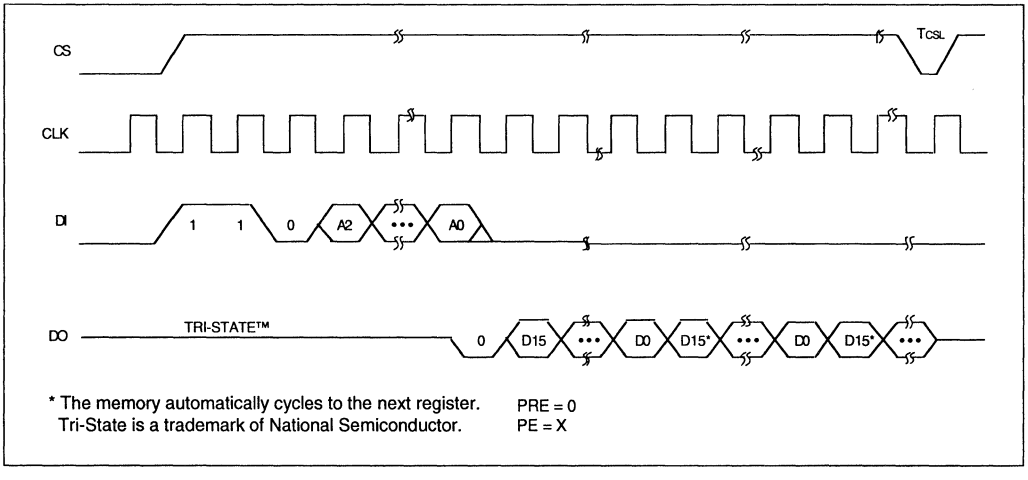


FIGURE 14-2: READ TIMING



* The memory automatically cycles to the next register. PRE = 0
Tri-State is a trademark of National Semiconductor. PE = X

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FIGURE 14-3: EWEN TIMING

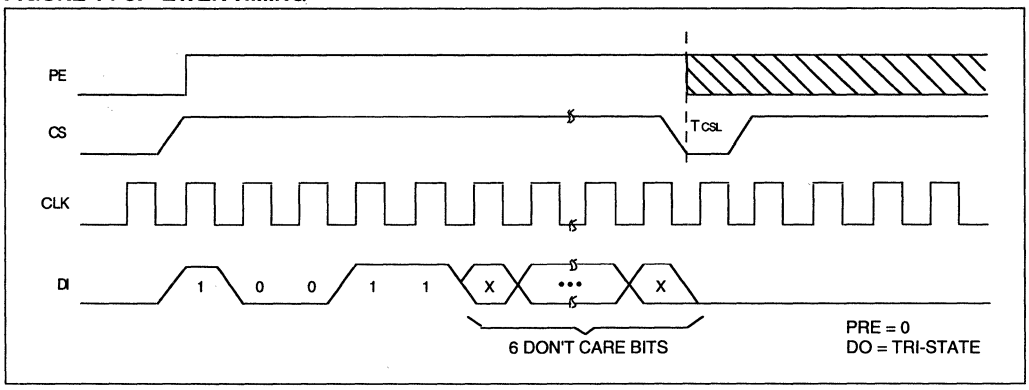

FIGURE 14-4: EWDS TIMING

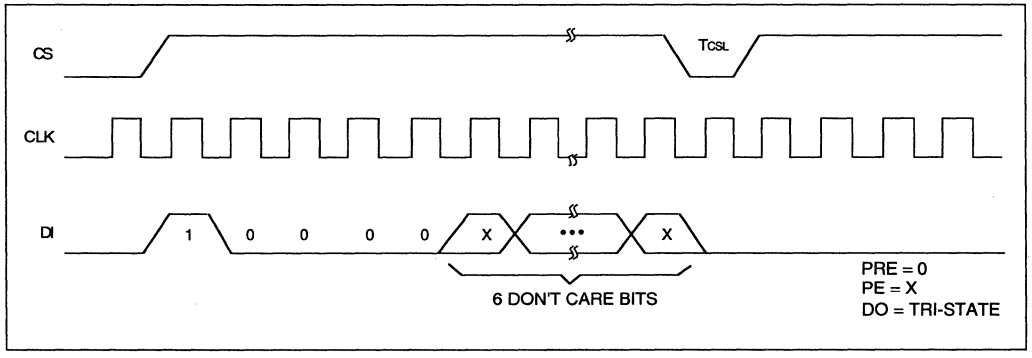

FIGURE 14-5: WRITE TIMING

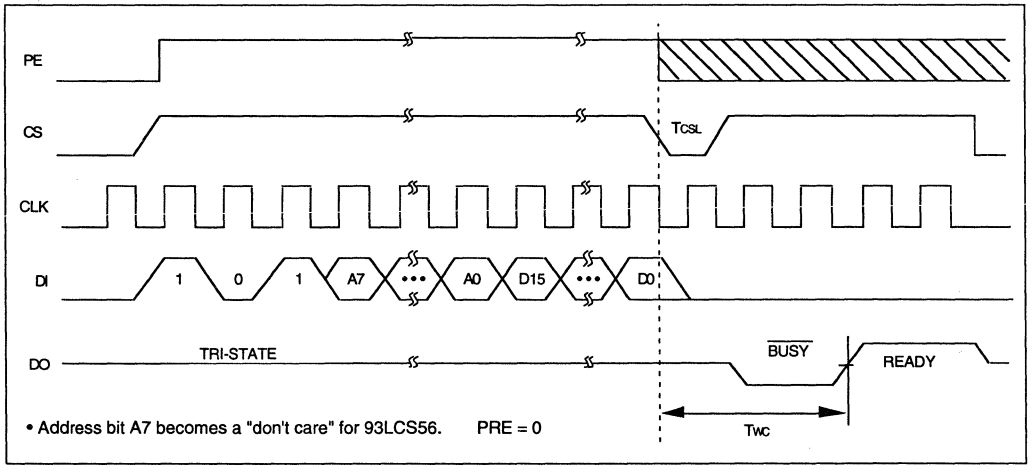

FIGURE 14-6: WRAL TIMING

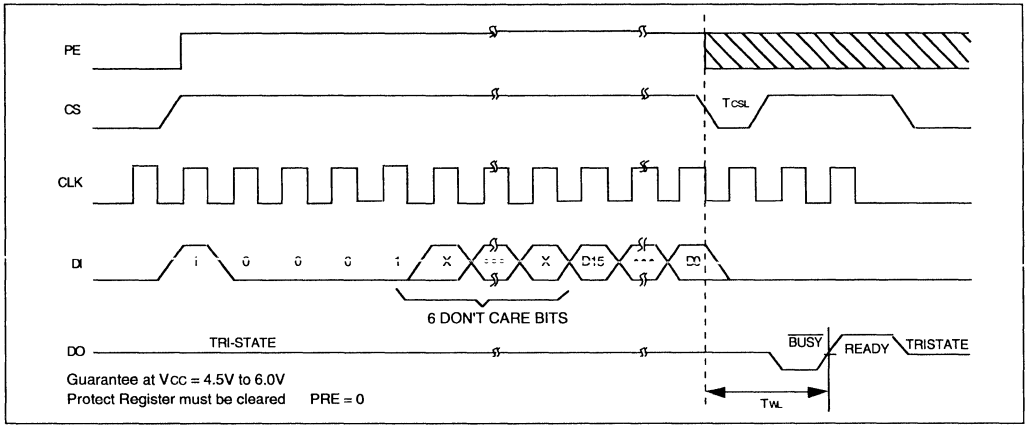

FIGURE 14-7: ERASE TIMING

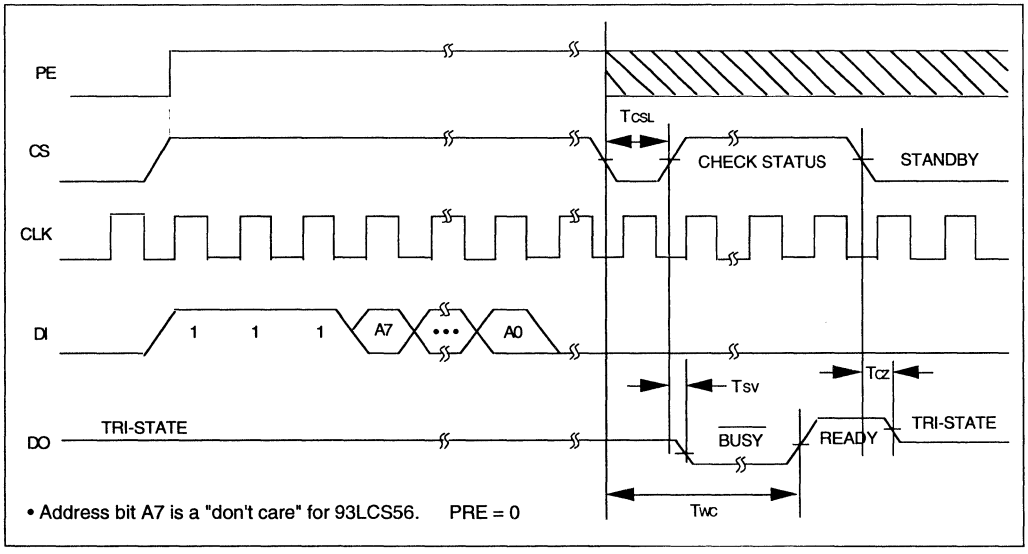

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FIGURE 14-8: ERAL TIMING

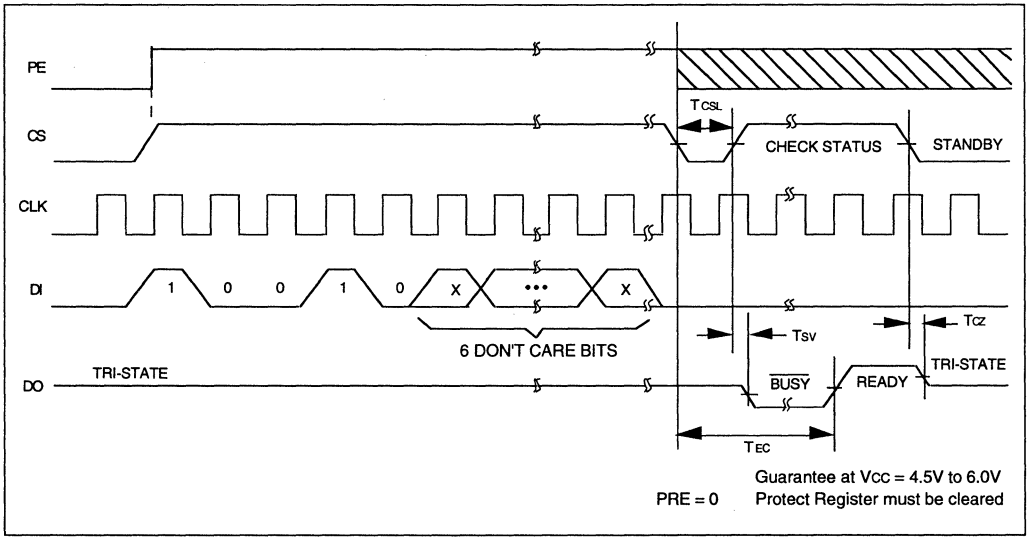

FIGURE 14-9: PRREAD TIMING

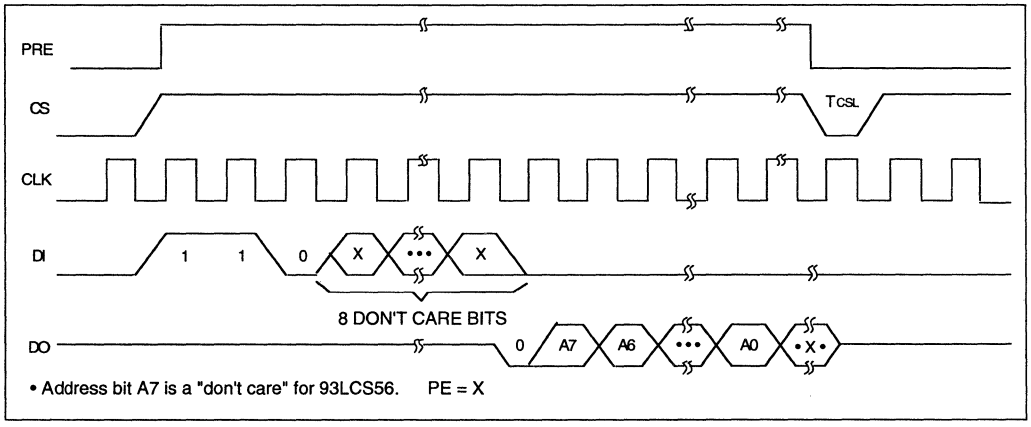

FIGURE 14-10: PREN TIMING

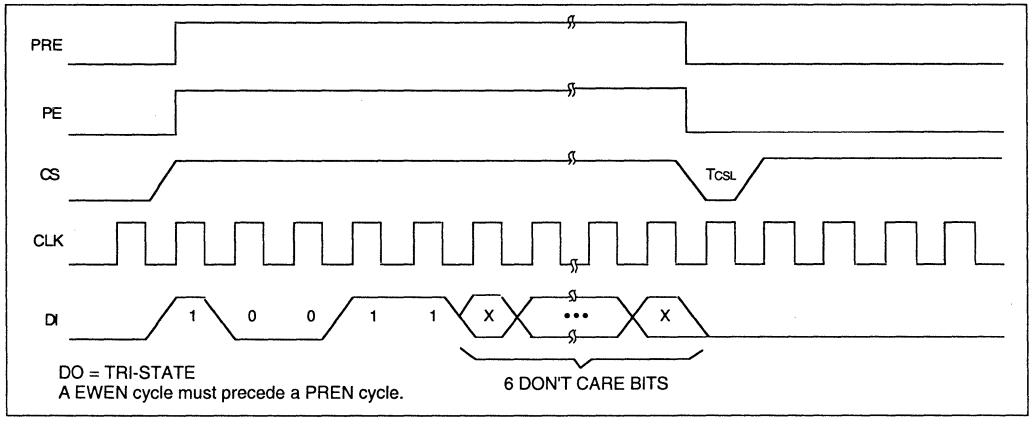

FIGURE 14-11: PRCLEAR TIMING

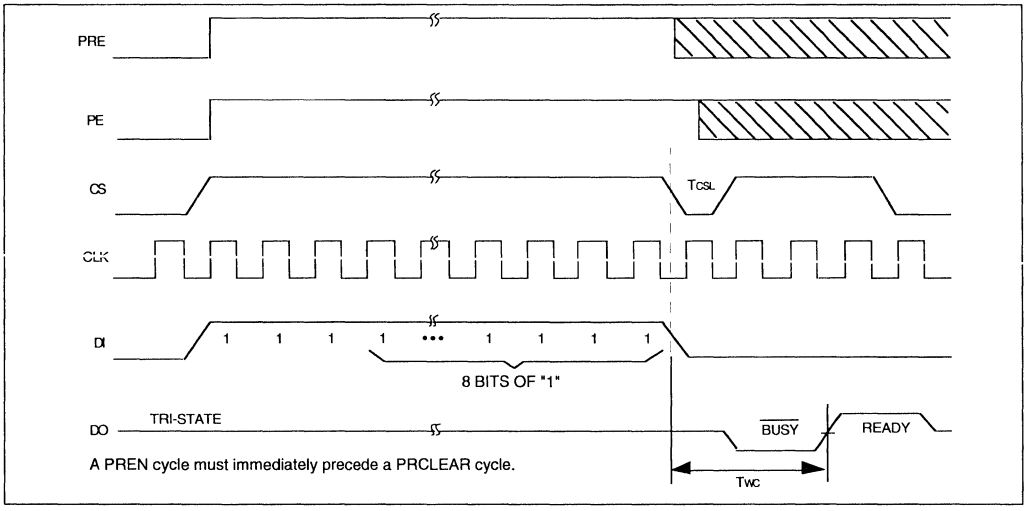

FIGURE 14-12: PRWRITE TIMING

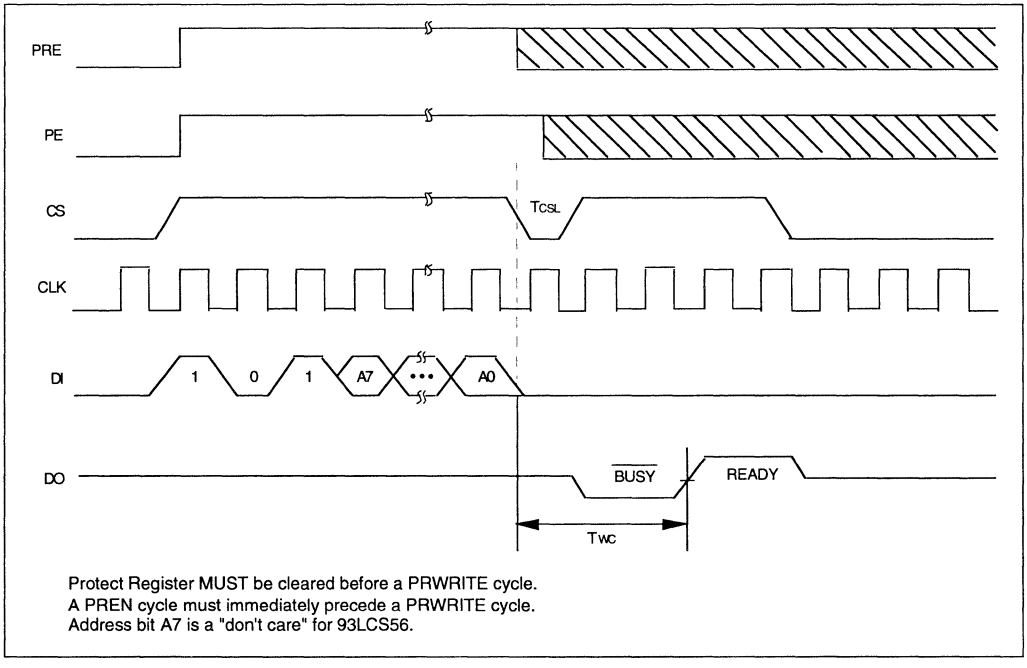

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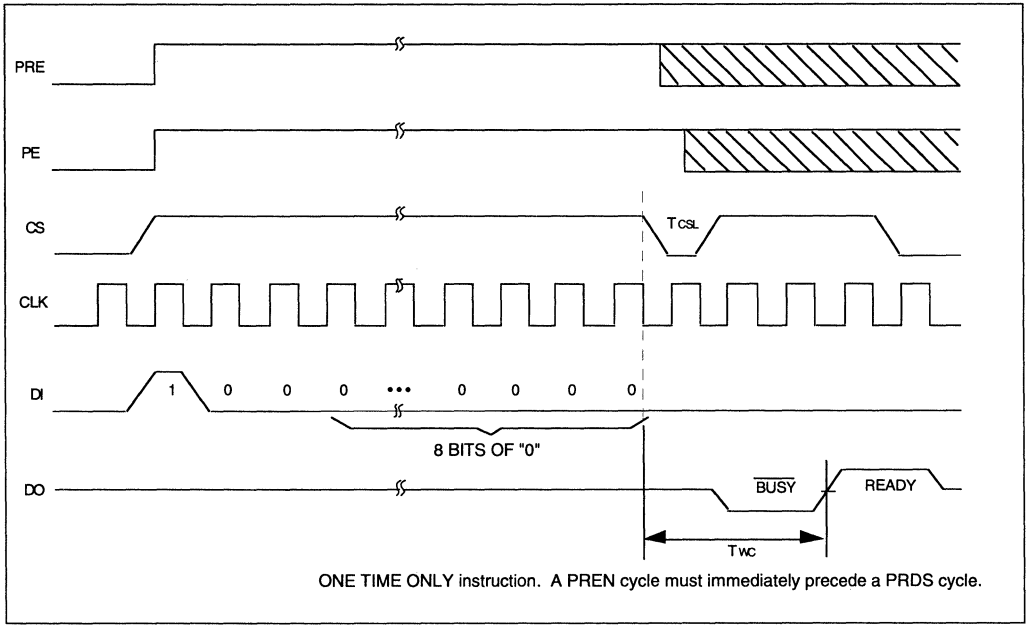
FIGURE 14-13: PRDS TIMING



ONE TIME ONLY instruction. A PREN cycle must immediately precede a PRDS cycle.

NOTES

93LCS56/66 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

93LCS56/66 - /P

Package:
P = Plastic DIP (300 mil Body), 8-lead
SN = Plastic SOIC (150 mil Body), 8-lead
SM = Plastic SOIC (207 mil Body), 8-lead
SL = Plastic SOIC (150 mil Body), 14-lead

Temperature Range:
Blank = 0°C to +70°C
I = -40°C to +85°C

Device:

	Configuration
93LCS56/66	CMOS Serial EEPROM
93LCS56X/66X	CMOS Serial EEPROM in alternate pinouts (SN package only)
93LCS56T/66T	CMOS Serial EEPROM (Tape and Reel)
93LCS56XT/66XT	CMOS Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

SECTION 6
PARALLEL EEPROM
PRODUCT SPECIFICATIONS

28C04A	4K (512 x 8) CMOS EEPROM	6-1
28C16A	16K (2K x 8) CMOS EEPROM	6-9
28C17A	16K (2K x 8) CMOS EEPROM	6-17
28C64A	64K (8K x 8) CMOS EEPROM	6-25

MICROCHIP

28C04A

4K (512 x 8) CMOS EEPROM

FEATURES

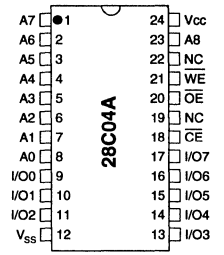
- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >10 years
- Endurance - Minimum 10^4 Erase/Write Cycles
  - Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- 5-Volt-Only Operation
- Organized 512x8 JEDEC standard pinout
  - 24-pin Dual-In-Line Package
  - 32-pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

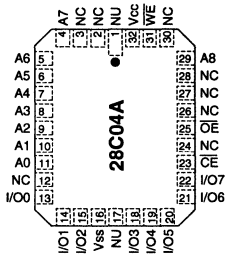
The Microchip Technology Inc. 28C04A is a CMOS 4K non-volatile electrically Erasable and Programmable Read Only Memory (EEPROM). The 28C04A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C04A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPE

DIP

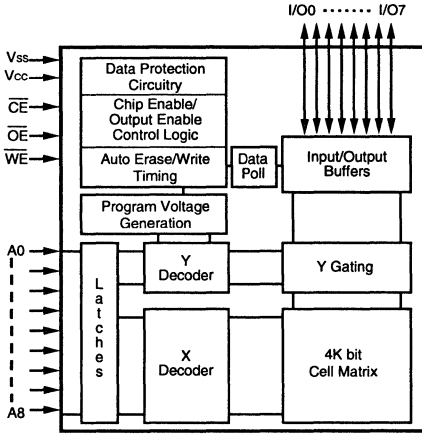


PLCC



• Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM



6

1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss .....-0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss.....-0.6V to +13.5V

Output Voltage w.r.t. Vss.....-0.6V to Vcc+0.6V

Storage temperature .....-65°C to +125°C

Ambient temp. with power applied .....-50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A8	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

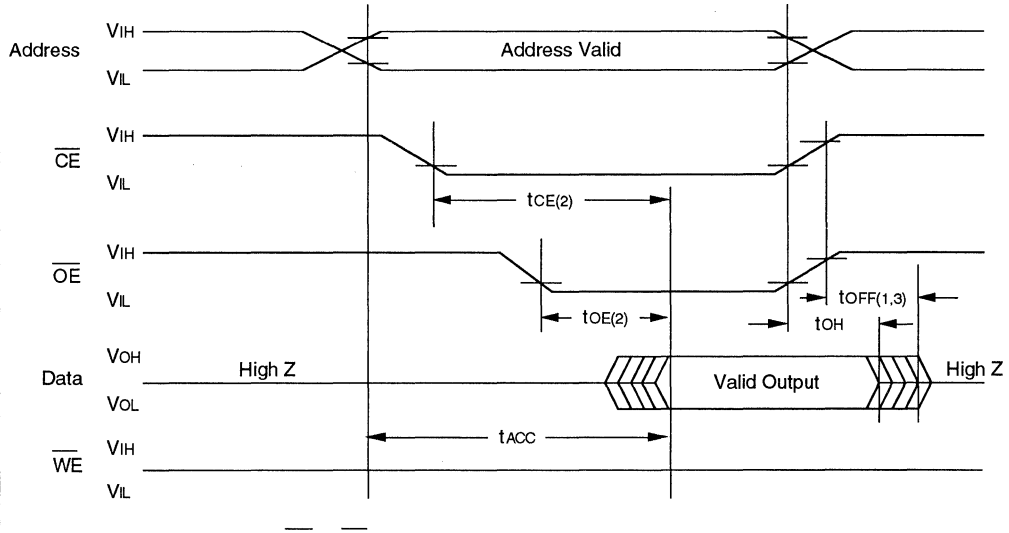
			Vcc = +5V ±10% Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic '1' Logic '0'	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance		CIN		10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage		ILO	-10	10	µA	VOUT = -0.1V TO Vcc + 0.1V
Output Capacitance		COUT		12	pF	VIN = 0V; TAMB = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC		30	mA	f = 5 MHz (Note 1) Vcc = 5.5V
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc+1

Note 1: AC power supply current above 5 MHz; 1 mA/MHz

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C									
Parameter	**Sym**	**28C04A-15**		**28C04A-20**		**28C04A-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}		150		200		250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		150		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		70		80		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ to $\overline{OE}$ High Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0		0		0		ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

FIGURE 1-2: BYTE WRITE AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100 pF	
Input Rise/Fall Times:	20 nsec	
Ambient Temperature:	Commercial (C): Tamb= 0°C to 70°C	
	Industrial (I): Tamb= -40°C to 85°C	

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10		ns	
Address Hold Time	t_{AH}	50		ns	
Data Set-Up Time	t_{DS}	50		ns	
Data Hold Time	t_{DH}	10		ns	
Write Pulse Width	t_{WPL}	100		ns	Note 1
Write Pulse High Time	t_{WPH}	50		ns	
$\overline{OE}$ Hold Time	t_{OEH}	10		ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10		ns	
Data Valid Time	t_{DV}		1000	ns	Note 2
Write Cycle Time (28C04A)	t_{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C04AF)	t_{WC}		200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

Note 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-3: PROGRAMMING WAVEFORMS

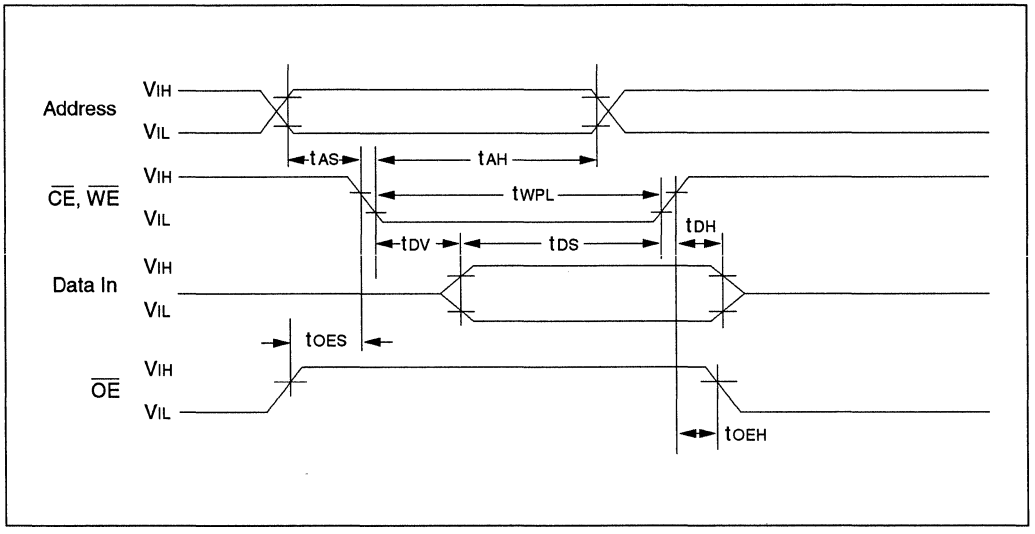


FIGURE 1-4: $\overline{\text{DATA}}$ POLLING WAVEFORMS

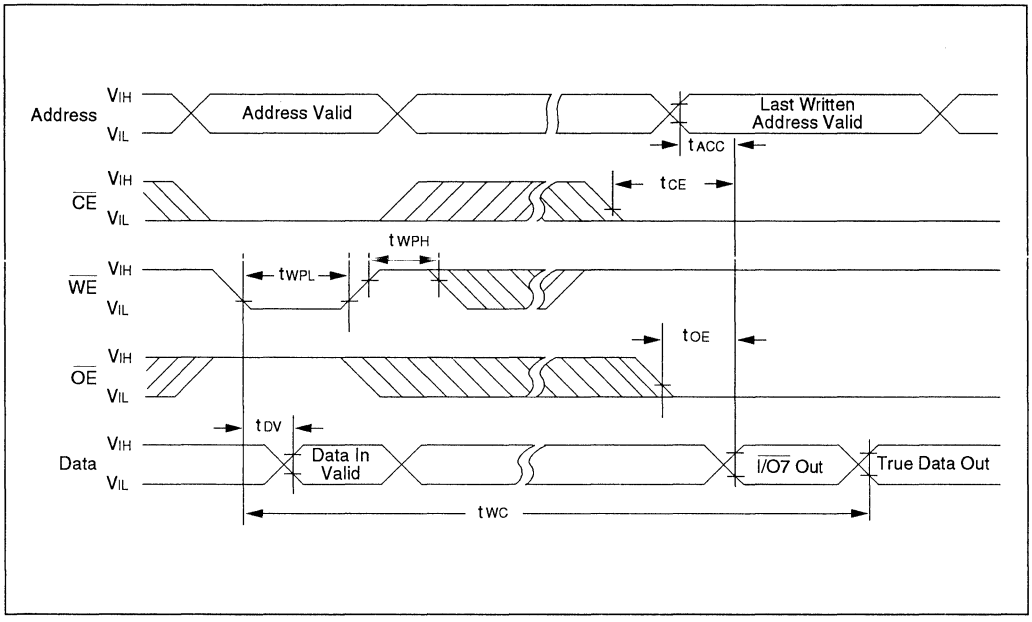
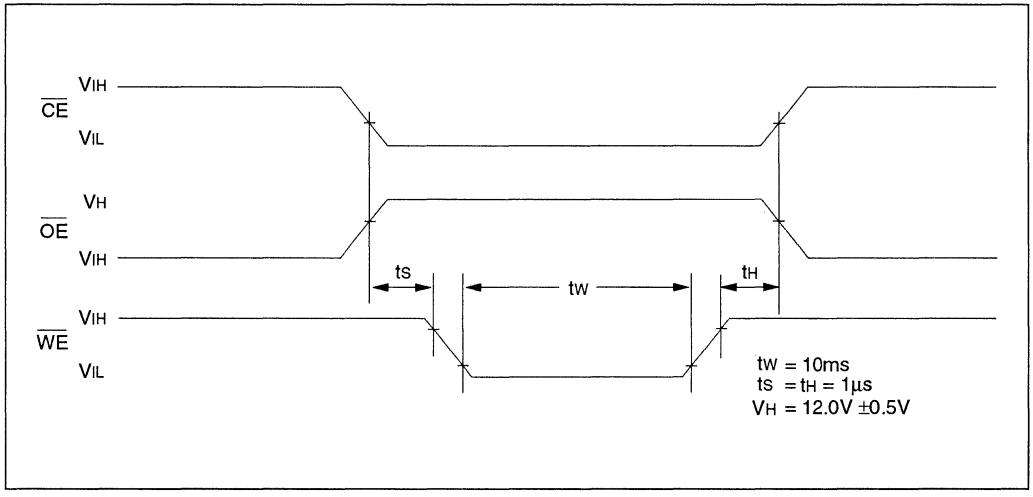


FIGURE 1-5: CHIP CLEAR WAVEFORMS



6

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C04A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{IE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

2.1 Read Mode

The 28C04A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

2.2 Standby Mode

The 28C04A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

2.4 Write Mode

The 28C04A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

2.5 Data Polling

The 28C04A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

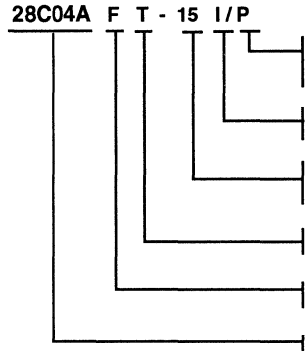
2.6 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

NOTES

28C04A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Package:	J	= CERDIP
	L	= Plastic Leaded Chip Carrier (PLCC)
	P	= Plastic DIP
Temperature Range:	Blank	= 0°C to +70°C
	I	= -40°C to +85°C
Access Time:	15	150 ns
	20	200 ns
	25	250 ns
Shipping:	Blank	Tube
	T	Tape and Reel "L" only.
Option:	–	= twc = 1ms
	F	= twc = 200 µs
Device:	28C04A	512 x 8 CMOS EEPROM

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

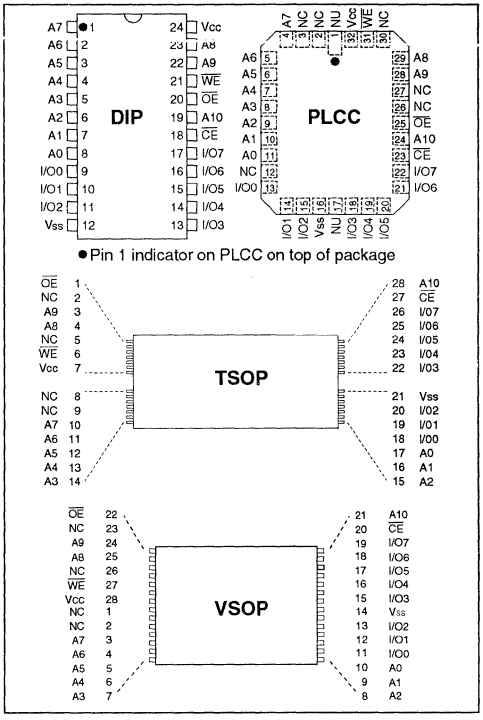
28C16A

16K (2K x 8) CMOS EEPROM

FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >10 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ polling
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
- 24-pin Dual-In-Line Package
- 32-pin Chip Carrier (Leadless or Plastic)
- 28-pin Thin Small Outline Package (TSOP) 8x20mm
- 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

PACKAGE TYPE

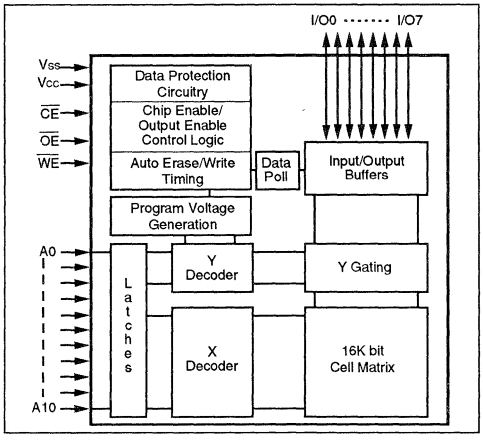


● Pin 1 indicator on PLCC on top of package

DESCRIPTION

The Microchip Technology Inc. 28C16A is a CMOS 16K non-volatile electrically Erasable PROM. The 28C16A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when a write cycle is complete, the 28C16A uses $\overline{\text{Data}}$ polling. $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

BLOCK DIAGRAM



6

1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss ..... -0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss ..... -0.6V to +13.5V

Voltage on A9 w.r.t. Vss ..... -0.6V to +13.5V

Output Voltage w.r.t. Vss ..... -0.6V to Vcc+0.6V

Storage temperature ..... -65°C to +125°C

Ambient temp. with power applied ..... -50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

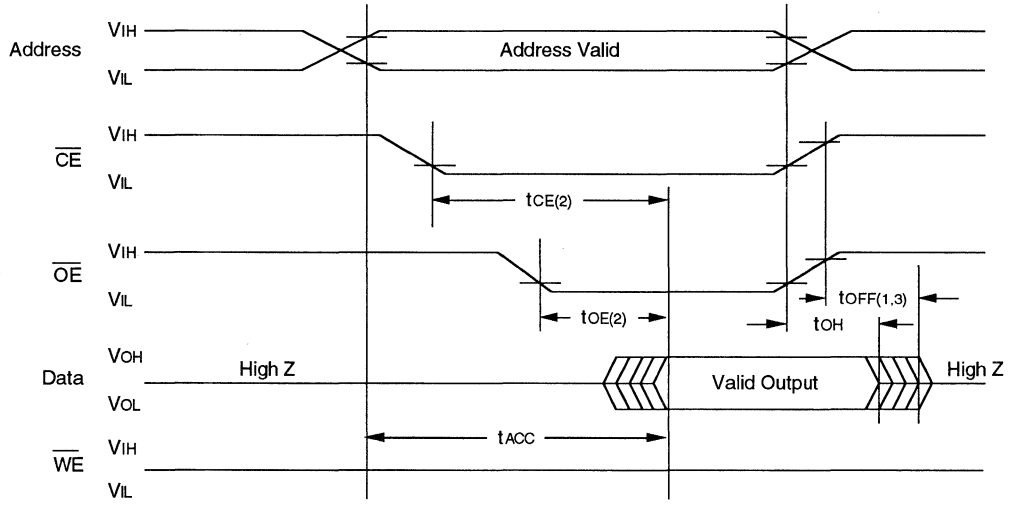
			Vcc = +5V ±10% Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic '1' Logic '0;	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to Vcc+1
Input Capacitance	—	CIN	—	10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1 mA
Output Leakage	—	ILO	-10	10	µA	VOUT = -0.1V to Vcc+0.1V
Output Capacitance	—	COUT	—	12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc+1

Note 1: AC power supply current above 5 MHz; 1 mA/MHz

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; Vol = 0.8V Output Load: 1 TTL Load + 100pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): Tamb = 0°C to +70°0°C Industrial (I): Tamb = -40°C to +85°C									
Parameter	**Sym**	**28C16A-15**		**28C16A-20**		**28C16A-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

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FIGURE 1-2: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise/Fall Times:	20 ns			
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C			
		Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	10	—	ns	
Address Hold Time	tAH	50	—	ns	
Data Set-Up Time	tDS	50	—	ns	
Data Hold Time	tDH	10	—	ns	
Write Pulse Width	tWPL	100	—	ns	Note 1
Write Pulse High Time	tWPH	50	—	ns	
$\overline{OE}$ Hold Time	tOEH	10	—	ns	
$\overline{OE}$ Set-Up Time	tOES	10	—	ns	
Data Valid Time	tDV	—	1000	ns	Note 2
Write Cycle Time (28C16A)	tWC	—	1	ms	0.5 ms typical
Write Cycle Time (28C16AF)	tWC	—	200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

Note 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until tDH after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-3: PROGRAMMING WAVEFORMS

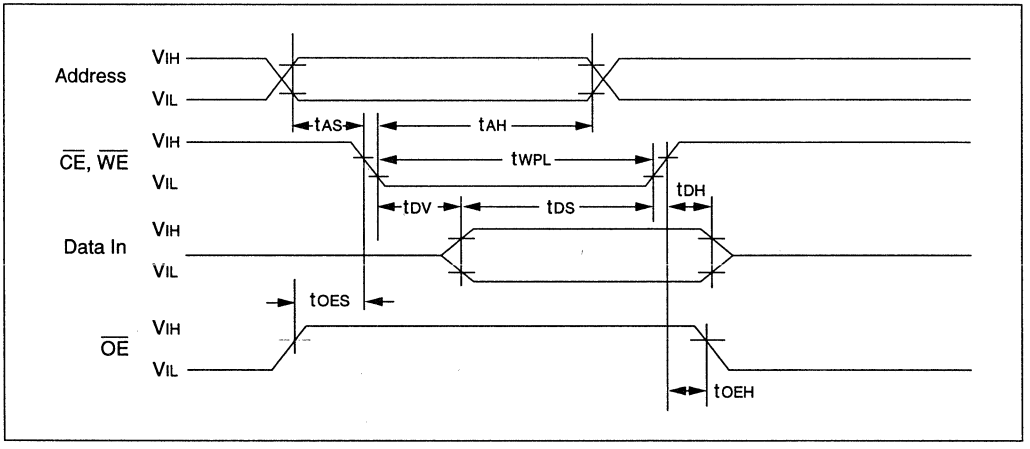


FIGURE 1-4: $\overline{\text{DATA}}$ POLLING WAVEFORMS

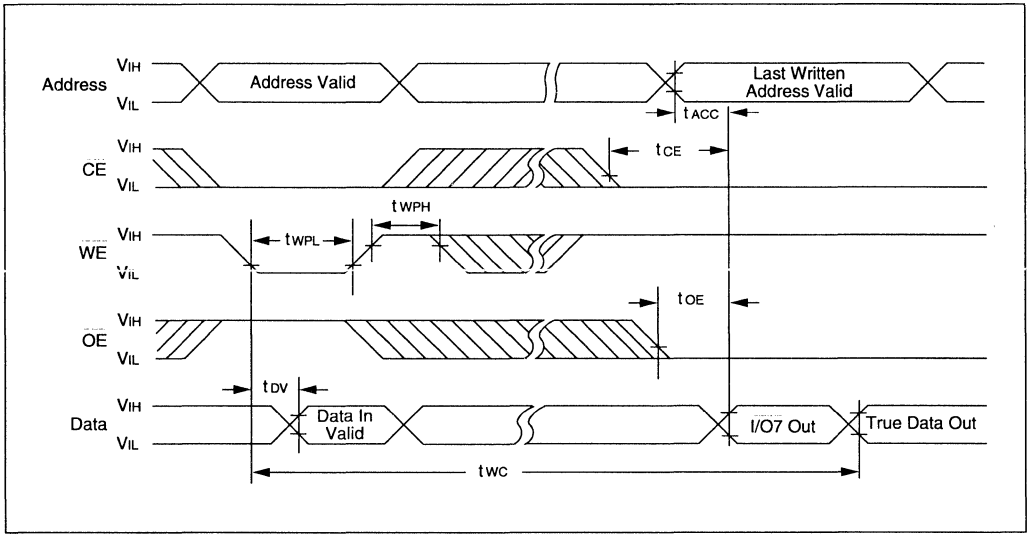


FIGURE 1-5: CHIP CLEAR WAVEFORMS

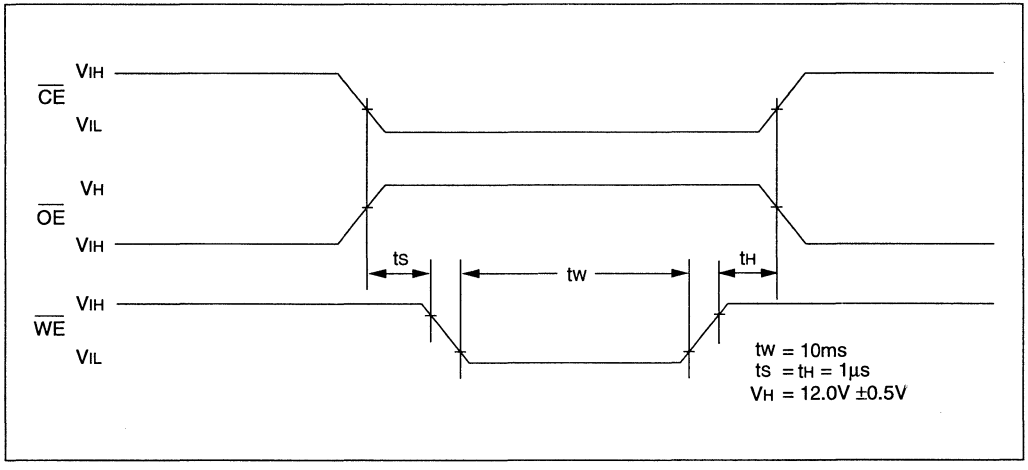


TABLE 1-4: SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In
Note 1: VH = 12.0V±0.5V		* Pulsed per programming waveforms.				

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C16A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

2.1 Read Mode

The 28C16A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

2.2 Standby Mode

The 28C16A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

2.4 Write Mode

The 28C16A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

2.5 $\overline{\text{Data}}$ Polling

The 28C16A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

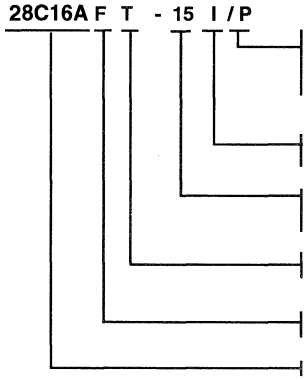
2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES

28C16A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Package:	J =	CERDIP
	L =	Plastic Leaded Chip Carrier (PLCC)
	P =	Plastic DIP
	TS =	Thin Small Outline Package (TSOP) 8x20mm
	VS =	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
Access Time:	15	150 ns
	20	200 ns
	25	250 ns
Shipping:	Blank	Tube
	T	Tape and Reel "L" only.
Option:	– =	twc = 1ms
	F =	twc = 200 µs
Device:	28C16A	2K x 8 CMOS EEPROM

Sales and Support

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2.The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277

3.The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

28C17A

16K (2K x 8) CMOS EEPROM

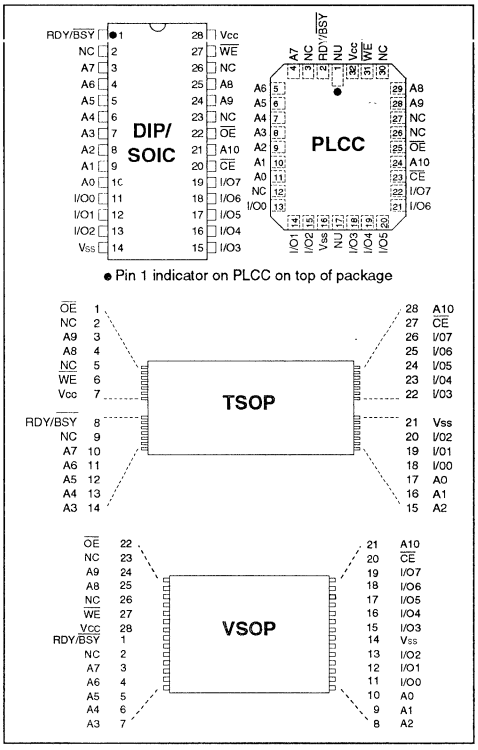
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >10 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling; Ready/$\overline{\text{Busy}}$
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 2Kx8 JEDEC Standard Pinout
  - 28 Pin Dual-In-Line Package
  - 32-Pin Chip Carrier (Leadless or Plastic)
  - 28-Pin Thin Small Outline Package (TSOP) 8x20mm
  - 28-Pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

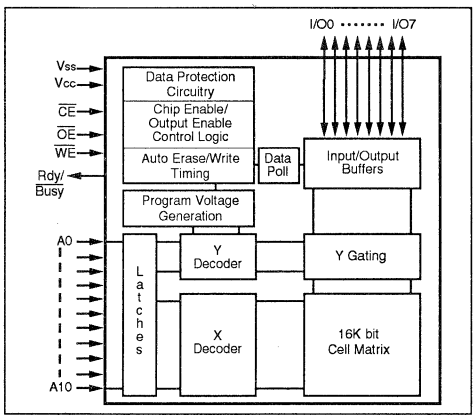
DESCRIPTION

The Microchip Technology Inc. 28C17A is a CMOS 16K non-volatile electrically Erasable PROM. The 28C17A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/$\overline{\text{Busy}}$ output or using $\overline{\text{Data}}$ polling. The Ready/$\overline{\text{Busy}}$ pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPE



BLOCK DIAGRAM



6

1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss.....-0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V

Voltage on A9 w.r.t. Vss .....-0.6V to +13.5V

Output Voltage w.r.t. Vss..... -0.6V to Vcc+0.6V

Storage temperature .....-65°C to +125°C

Ambient temp. with power applied .....-50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A10	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

				Vcc = +5V ±10% Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic '1' Logic '0'	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to Vcc +1
Input Capacitance	—	CIN	—	10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	—	ILO	-10	10	µA	VOUT = -0.1V to Vcc +0.1V
Output Capacitance	—	COUT	—	12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	ICC	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V;
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc +1

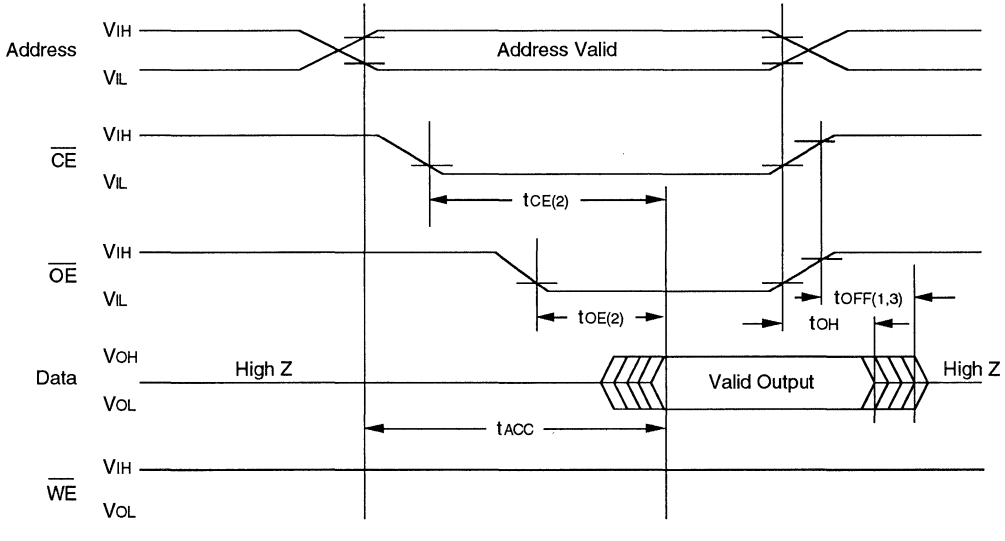
Note 1: AC power supply current above 5MHz: 1mA/MHz

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100 pF	
Input Rise and Fall Times:	20 ns	
Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C	
	Industrial (I): Tamb = -40°C to +85°C	

Parameter	Symbol	28C17A-15		28C17A-20		28C17A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V			
	Output Load:	1 TTL Load + 100 pF			
	Input Rise/Fall Times:	20 ns			
	Ambient Temperature:	Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	10	—	ns	
Address Hold Time	t_{AH}	50	—	ns	
Data Set-Up Time	t_{DS}	50	—	ns	
Data Hold Time	t_{DH}	10	—	ns	
Write Pulse Width	t_{WPL}	100	—	ns	Note 1
Write Pulse High Time	t_{WPH}	50	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	10	—	ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10	—	ns	
Data Valid Time	t_{DV}	—	1000	ns	Note 2
Time to Device Busy	t_{DB}	2	50	ns	
Write Cycle Time (28C17A)	t_{WC}	—	1	ms	0.5 ms typical
Write Cycle Time (28C17AF)	t_{WC}	—	200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first

Note 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

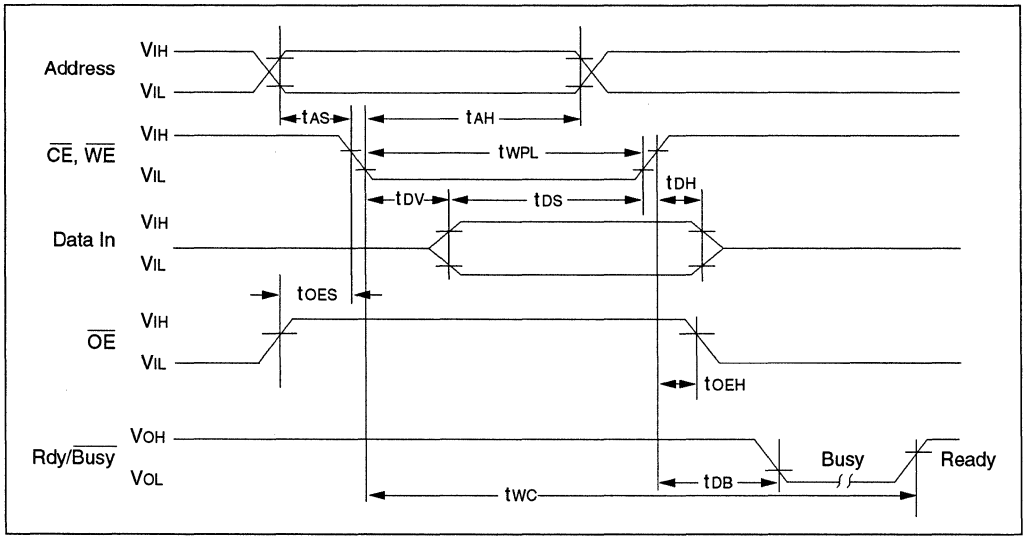


FIGURE 1-3: DATA POLLING WAVEFORMS

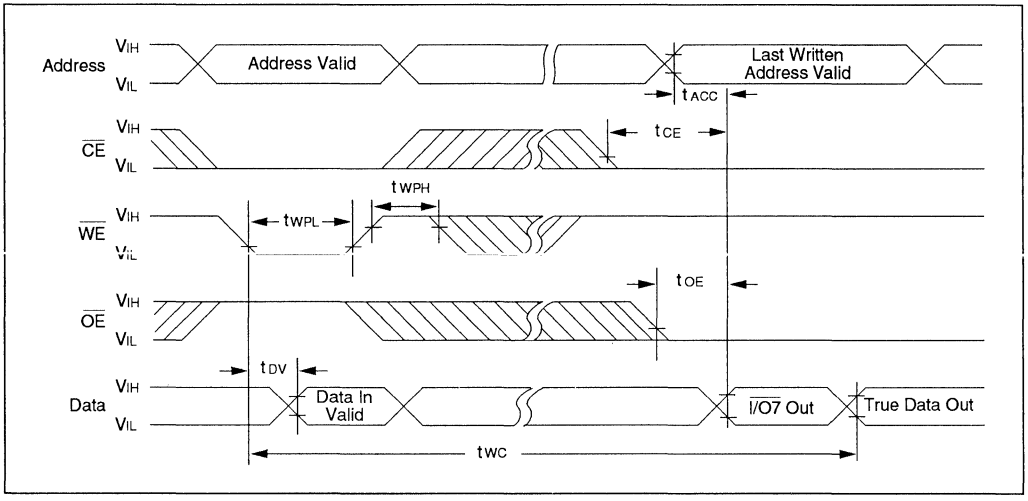


FIGURE 1-4: CHIP CLEAR WAVEFORMS

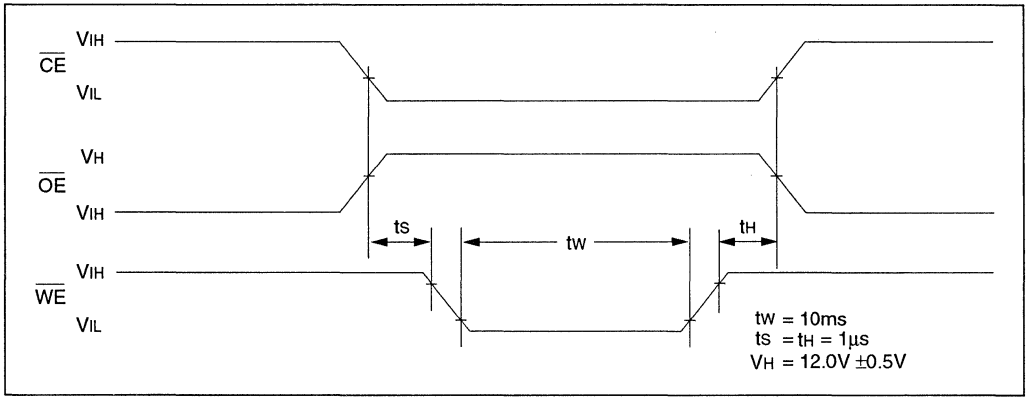


TABLE 1-5: SUPPLEMENTARY CONTROL

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	Vcc	I/Oi
Chip Clear	VIL	VH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note 1: VH = 12.0V ±0.5V * Pulsed per programming waveforms.

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C17A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$ (1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note 1: Open drain output.
Note 2: X = Any TTL level.

2.1 Read Mode

The 28C17A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{OE}$, assuming that CE has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

2.2 Standby Mode

The 28C17A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

2.4 Write Mode

The 28C17A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C17A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C17A has completed writing and is ready to accept another cycle.

2.5 $\overline{Data}$ Polling

The 28C17A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7EO to 7FF, the additional bytes can be written to or read from in the same manner as the regular memory array.

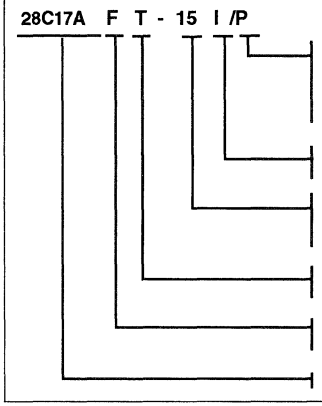
2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

NOTES

28C17A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



Package:	J	= CERDIP
	L	= Plastic Leaded Chip Carrier (PLCC)
	P	= Plastic DIP
	TS	= Thin Small Outline Package (TSOP) 8x20mm
	VS	= Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	Blank	= 0°C to +70°C
	I	= -40°C to +85°C
Access Time:	15	150 ns
	20	200 ns
	25	250 ns
Shipping:	Blank	Tube
	T	Tape and Reel "L" and "SO"
Option:	–	= twc = 1ms
	F	= twc = 200 µs
Device:	28C17A	2K x 8 CMOS EEPROM

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2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

28C64A

64K (8K x 8) CMOS EEPROM

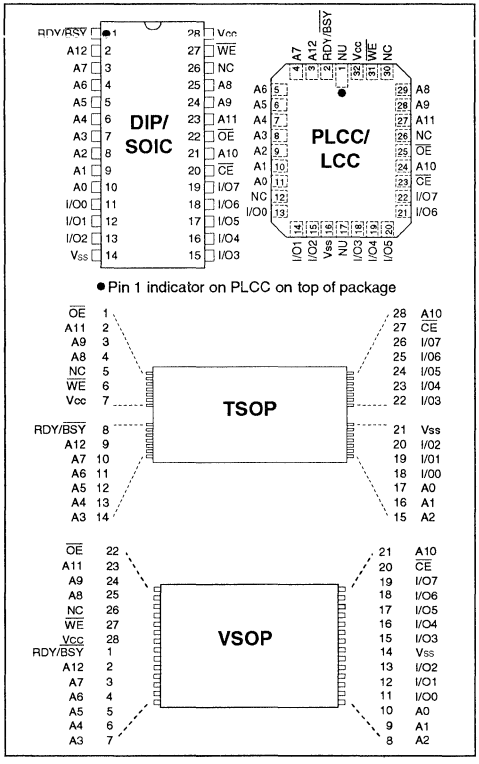
FEATURES

- Fast Read Access Time—150 ns
- CMOS Technology for Low Power Dissipation
  - 30 mA Active
  - 100 µA Standby
- Fast Byte Write Time—200 µs or 1 ms
- Data Retention >10 years
- High Endurance - Minimum 10^4 Erase/Write Cycles
- Automatic Write Operation
  - Internal Control Timer
  - Auto-Clear Before Write Operation
  - On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Ready/$\overline{\text{Busy}}$
- Chip Clear Operation
- Enhanced Data Protection
  - Vcc Detector
  - Pulse Filter
  - Write Inhibit
- Electronic Signature for Device Identification
- 5-Volt-Only Operation
- Organized 8Kx8 JEDEC Standard Pinout
  - 28-pin Dual-In-Line Package
  - 32-pin Chip Carrier (Leadless or Plastic)
  - 28-pin Thin Small Outline Package (TSOP) 8x20mm
  - 28-pin Very Small Outline Package (VSOP) 8x13.4mm
- Available for Extended Temperature Ranges:
  - Commercial: 0°C to +70°C

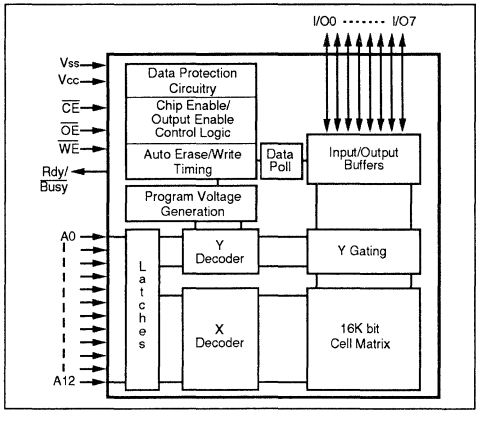
DESCRIPTION

The Microchip Technology Inc. 28C64A is a CMOS 64K non-volatile electrically Erasable PROM. The 28C64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/$\overline{\text{Busy}}$ output or using $\overline{\text{Data}}$ polling. The Ready/$\overline{\text{Busy}}$ pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, $\overline{\text{Data}}$ polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications

PACKAGE TYPE



BLOCK DIAGRAM



6

1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

Vcc and input voltages w.r.t. Vss.....-0.6V to + 6.25V

Voltage on $\overline{OE}$ w.r.t. Vss .....-0.6V to +13.5V

Voltage on A9 w.r.t. Vss .....-0.6V to +13.5V

Output Voltage w.r.t. Vss..... -0.6V to Vcc+0.6V

Storage temperature .....-65°C to +125°C

Ambient temp. with power applied .....-50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
Vcc	+5V Power Supply
Vss	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTIC

				Vcc = +5V ±10% Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Status**	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
Input Voltages	Logic '1' Logic '0'	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to Vcc +1
Input Capacitance	—	CIN	—	10	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz (Note 2)
Output Voltages	Logic '1' Logic '0'	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	—	ILO	-10	10	µA	VOUT = -0.1V to Vcc +0.1V
Output Capacitance	—	COUT	—	12	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz (Note 2)
Power Supply Current, Active	TTL input	ICC	—	30	mA	f = 5 MHz (Note 1) Vcc = 5.5V
Power Supply Current, Standby	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	—	2 3 100	mA mA µA	$\overline{CE}$ = VIH (0°C to +70°C) $\overline{CE}$ = VIH (-40°C to +85°C) $\overline{CE}$ = Vcc-0.3 to Vcc +1

Note 1: AC power supply current above 5MHz: 2mA/MHz.
Note 2: Not 100% tested.

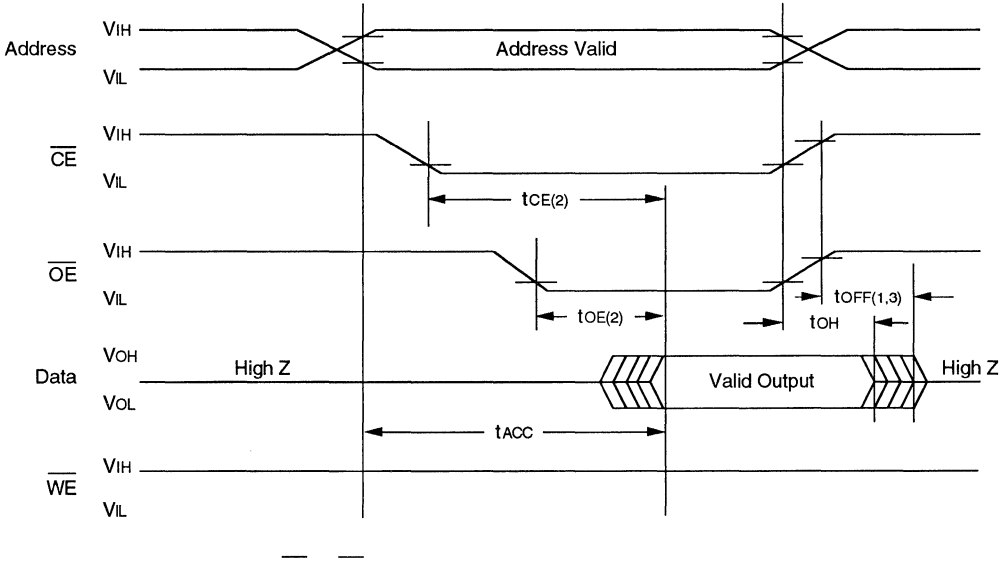
TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100 pF	
Input Rise and Fall Times:	20 ns	
Ambient Temperature:	Commercial (C):	Tamb = 0°C to +70°C
	Industrial (I):	Tamb = -40°C to +85°C

Parameter	Symbol	28C64A-15		28C64A-20		28C64A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	150	—	200	—	250	ns	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	70	—	80	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ High to Output Float	t_{OFF}	0	50	0	55	0	70	ns	Note 1
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first.	t_{OH}	0	—	0	—	0	—	ns	Note 1

Note 1: Not 100% tested.

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested

TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

	AC Testing Waveform:		V_{IH} = 2.4V; V_{IL} = 0.45V; V_{OH} = 2.0V; V_{OL} = 0.8V		
	Output Load:		1 TTL Load + 100 pF		
	Input Rise/Fall Times:		20 ns		
	Ambient Temperature:		Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	10	—	ns	
Address Hold Time	t_{AH}	50	—	ns	
Data Set-Up Time	t_{DS}	50	—	ns	
Data Hold Time	t_{DH}	10	—	ns	
Write Pulse Width	t_{WPL}	100	—	ns	Note 1
Write Pulse High Time	t_{WPH}	50	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	10	—	ns	
$\overline{OE}$ Set-Up Time	t_{OES}	10	—	ns	
Data Valid Time	t_{DV}	—	1000	ns	Note 2
Time to Device Busy	t_{DB}	2	50	ns	
Write Cycle Time (28C64A)	t_{WC}	—	1	ms	0.5 ms typical
Write Cycle Time (28C64AF)	t_{WC}	—	200	µs	100 µs typical

Note 1: A write cycle can be initiated be $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data is latched on the positive edge $\overline{WE}$, whichever occurs first.

Note 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS

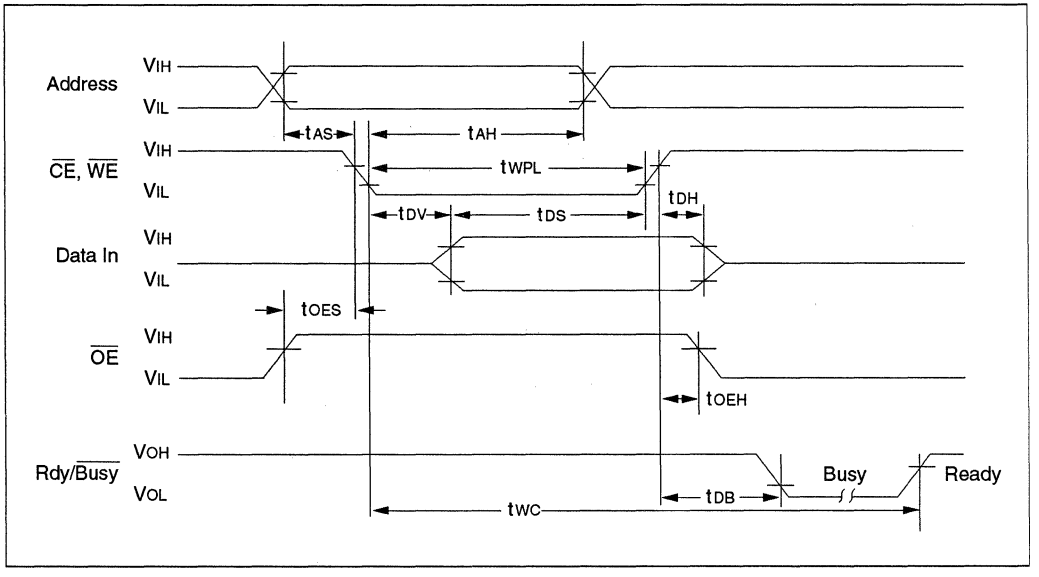


FIGURE 1-3: $\overline{\text{DATA}}$ POLLING WAVEFORMS

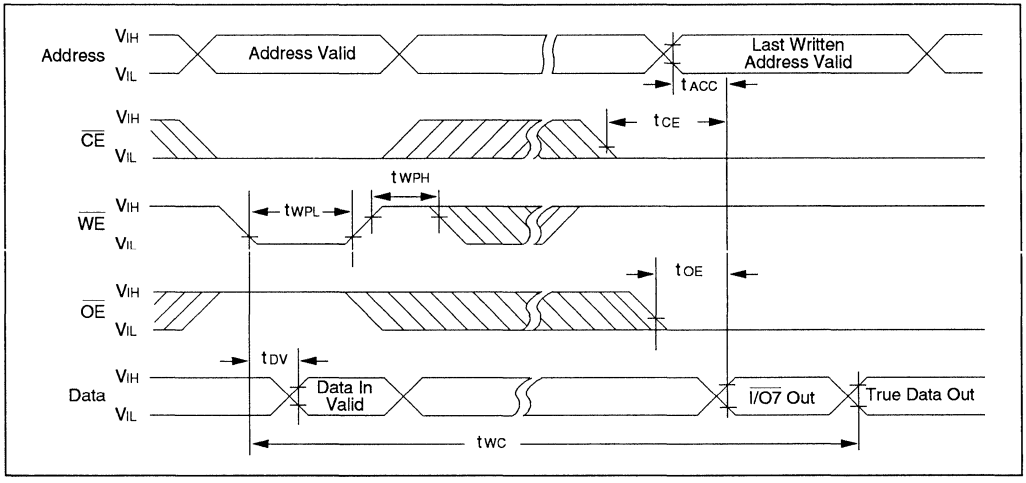


FIGURE 1-4: CHIP CLEAR WAVEFORMS

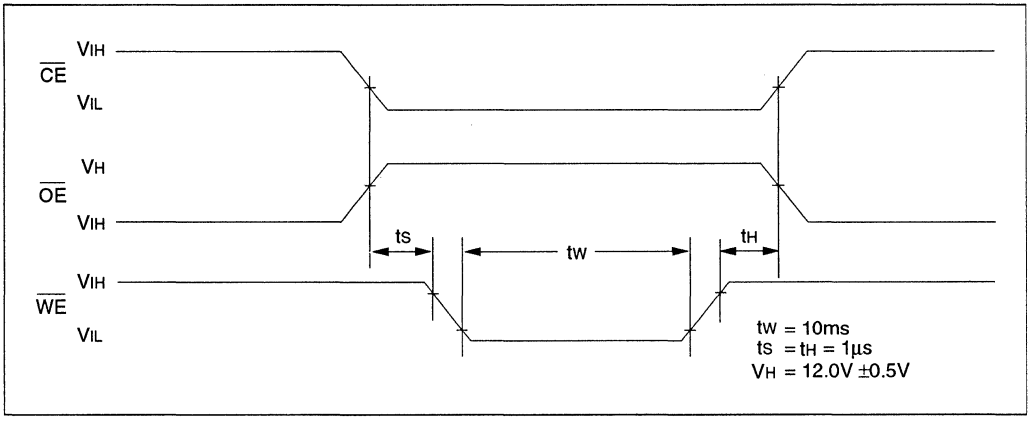


TABLE 1-5: SUPPLEMENTARY CONTROL

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A9	Vcc	I/Oi
Chip Clear	VIL	VIH	VIL	X	Vcc	
Extra Row Read	VIL	VIL	VIH	A9 = VH	Vcc	Data Out
Extra Row Write	*	VIH	*	A9 = VH	Vcc	Data In

Note: VH = 12.0V±0.5V. *Pulsed per programming waveforms.

6

2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$ (1)
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note 1: Open drain output.
Note 2: X = Any TTL level.

2.1 Read Mode

The 28C64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the output tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC-tOE.

2.2 Standby Mode

The 28C64A is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal VCC detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when VCC is less than the VCC detect circuit trip.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (VCC).

2.4 Write Mode

The 28C64A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C64A has completed writing and is ready to accept another cycle.

2.5 $\overline{Data}$ Polling

The 28C64A features $\overline{Data}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminable). After completion of the write cycle, true data is available. $\overline{Data}$ polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

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2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data, except for the extra row.

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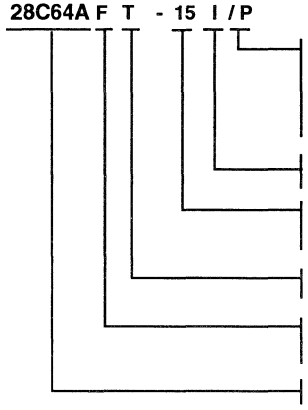

Package:	J	=	CERDIP
	L	=	Plastic Leaded Chip Carrier (PLCC)
	P	=	Plastic DIP
	SO	=	Plastic Small Outline IC
	TS	=	Thin Small Outline Package (TSOP) 8x20mm
	VS	=	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
Access Time:	15		150 ns
	20		200 ns
	25		250 ns
Shipping:	Blank		Tube
	T		Tape and Reel "L" and "SO"
Option:	–	=	twc = 1ms
	F	=	twc = 200 µs
Device:	28C64A		8K x 8 CMOS EEPROM

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2.The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277

3.The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

MICROCHIP

SECTION 7
EPROM
PRODUCT SPECIFICATIONS

27C64	64K (8K x 8) CMOS EPROM	7-1
27LV64	64K (8K x 8) Low-Voltage CMOS EPROM	7-9
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MICROCHIP

27C64

64K (8K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 120 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin Chip carrier (leadless or plastic)
  - 28-pin SOIC package
  - 28-pin TSOP package
  - Tape and reel
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

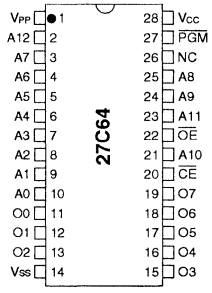
DESCRIPTION

The Microchip Technology Inc. 27C64 is a CMOS 64K bit (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

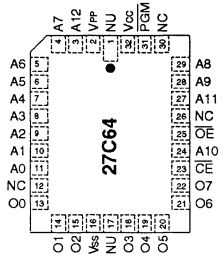
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

PACKAGE TYPE

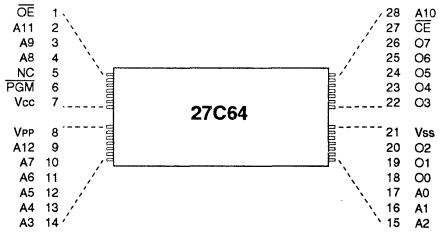
DIP/SOIC



PLCC/LCC



TSOP



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to + 7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S) — —	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ± 0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: C=Commercial Temperature Range; I =Industrial Temperature Range

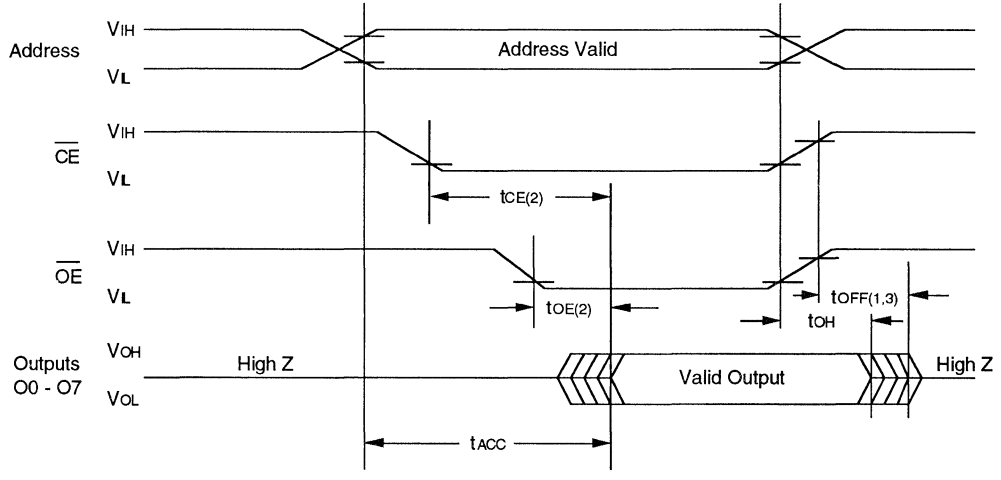
Note 1: Typical active current increases .5 mA per MHz up to operating frequency for all temperature ranges.

Note 2: VCC must be applied before VPP, and be removed simultaneously or after VPP.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C												
Parameter	**Sym**	**27C64-12**		**27C64-15**		**27C64-17**		**27C64-20**		**27C64-25**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	tACC	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Note 1: tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Note 2: $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE.
Note 3: This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic"1" Logic"0"	V_{OH} V_{OL}	2.4 —	— 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

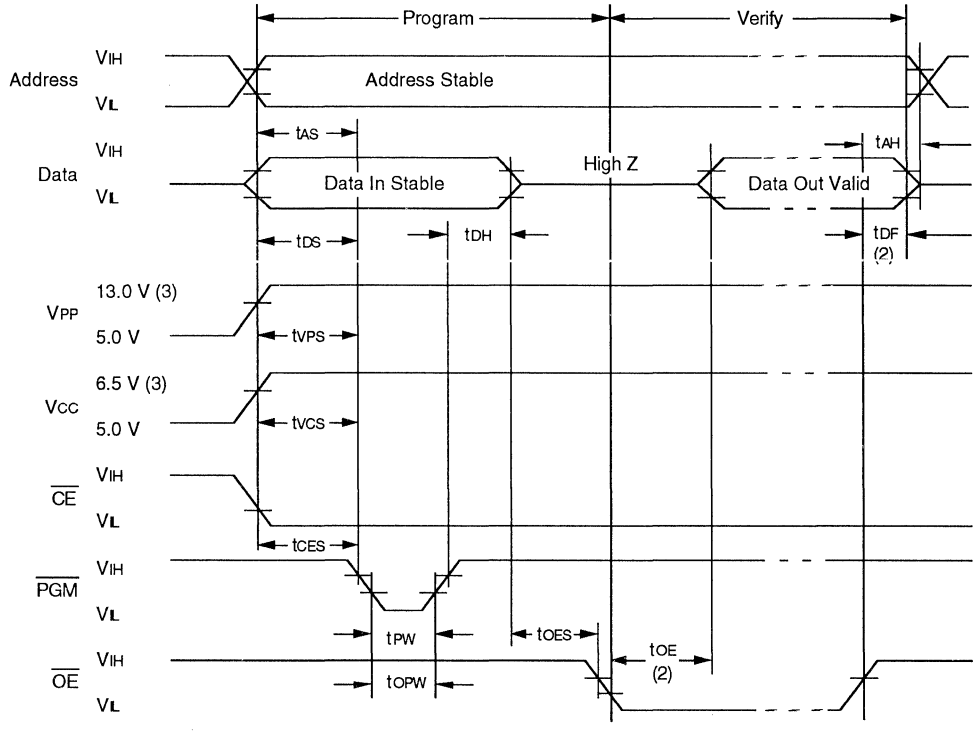
Note 1: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH}=2.4V and V_{IL}=0.45V; V_{OH}=2.0V; V_{OL}=0.8V Ambient Temperature: Tamb=25°C ±5°C V_{CC}= 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5 V ±0.25 V, V_{PP} = V_H = 13.0 V ±0.25 V for Express algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) VPP is brought to the proper VH level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) VPP is at the proper VH level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

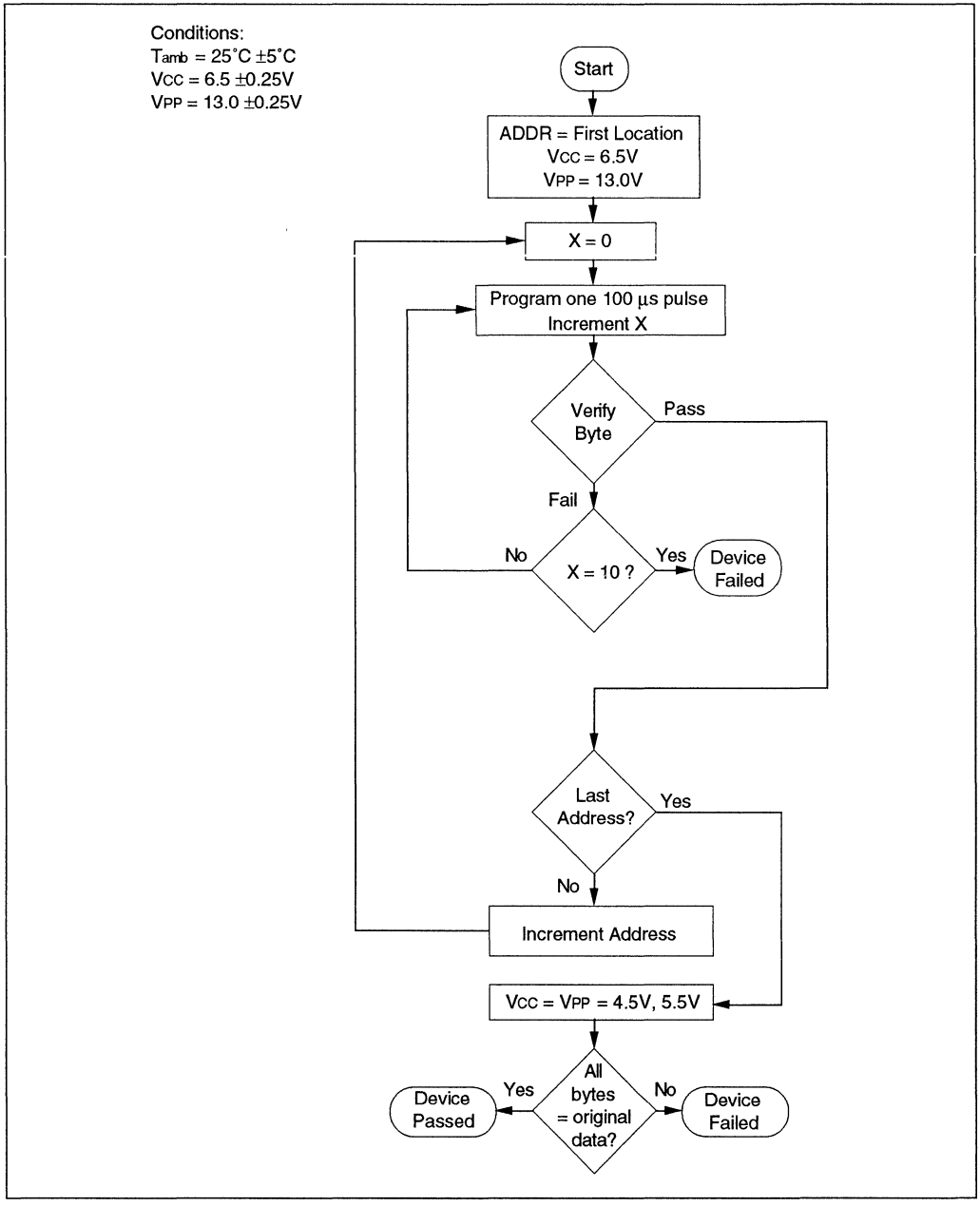
1.9 Identity Mode

In this mode, specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	0	0	1	0	02

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C64 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27C64 - 25 I /K

Package:	J	CERDIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package (TSOP) 8X13.4mm
Temperature Range:	-	0°C to +70°C
	I	–40°C to +85°C
Access Time:	12	120 ns
	15	150 ns
	17	170 ns
	20	200 ns
	25	250 ns
Device:	27C64	64K (8K x 8) CMOS EPROM

MICROCHIP

27LV64

64K (8K x 8) Low-Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  - 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  - 8 mA active current at 3.0V
  - 20 mA active current at 5.5V
  - 100 µA standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 8K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin Chip carrier (leadless or plastic)
  - 28-pin SOIC package
  - 28-pin TSOP package
  - Tape and reel
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

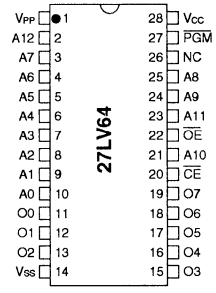
DESCRIPTION

The Microchip Technology Inc. 27LV64 is a low-voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as 8K x 8 (8K-Byte) non-volatile memory product. The 27LV64 consumes only 8mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMs can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0V.This device allows system designers the ability to use low voltage non-volatile memory with today's low voltage microprocessors and peripherals in battery powered applications.

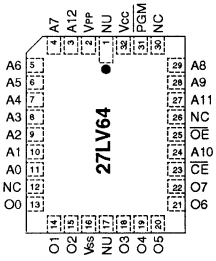
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPE

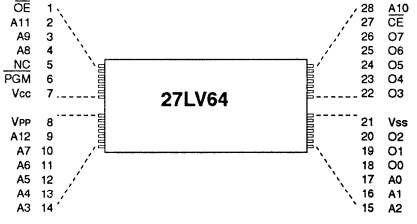
DIP/SOIC



PLCC/LCC



TSOP



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to + 7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Or +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = 3.0V to 5.5V unless otherwise specified
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 @ 5.0V 8 @ 3.0V 25 @ 5.0V 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)	—	1 @ 3.0V 2@ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$ = VCC ± 0.2V

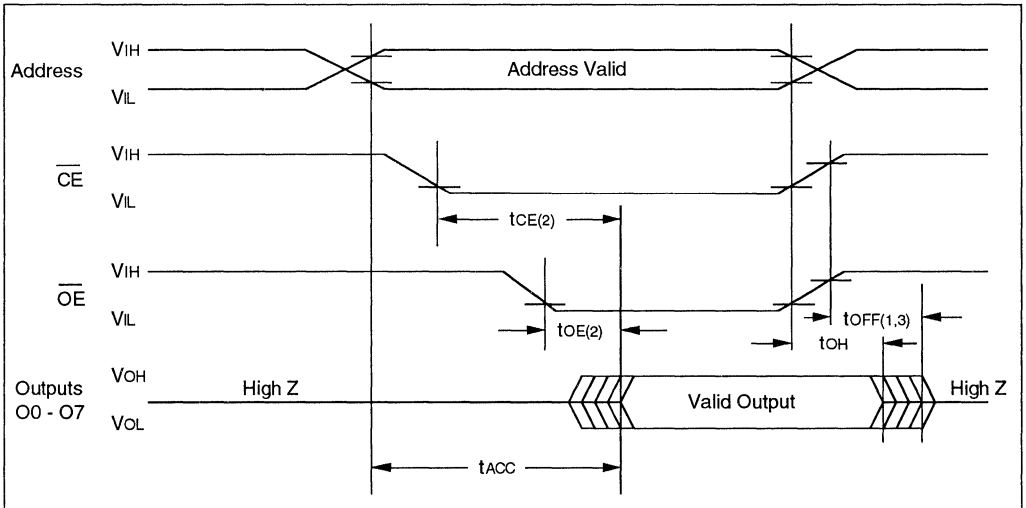
* Parts: C=Commercial Temperature Range; I=Industrial Temperature Range

Note 1: Typical active current increases .5 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C								
Parameter	**Sym**	**27LV64-20**		**27LV64-25**		**27LV64-30**		**Units**	**Conditions**
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	100	—	125	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	IPP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

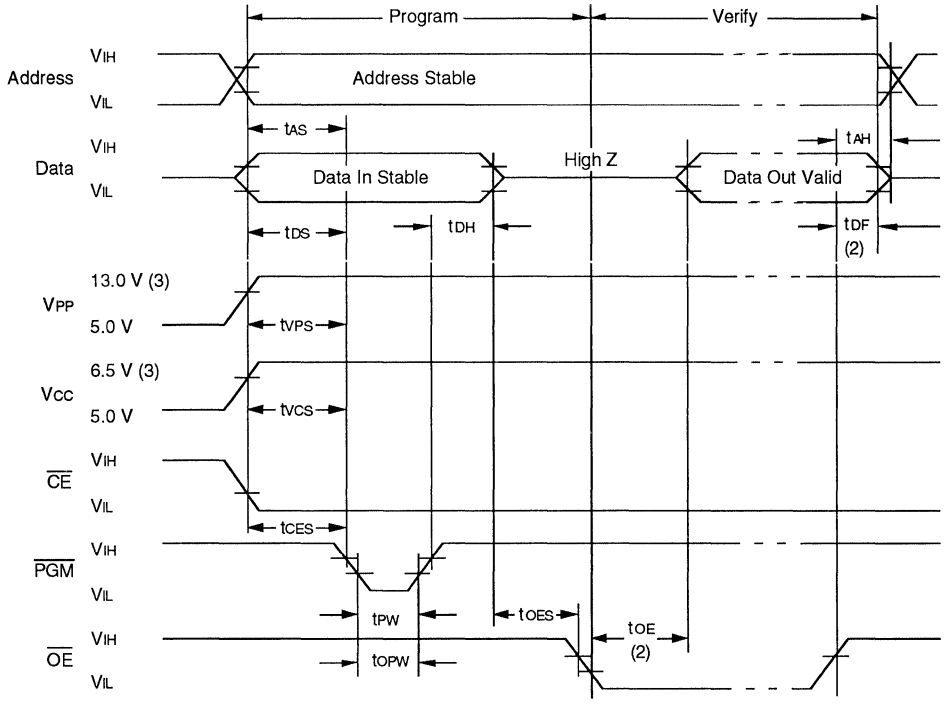
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Ambient Temperature: Tamb=25°C ± 5°C VCC= 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE		100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference is 0.8V for VIL and 2.0V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) Vcc = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for Express algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	Vcc	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	Vcc	X	High Z
Output Disable	VIL	VIH	VIH	Vcc	X	High Z
Identity	VIL	VIL	VIH	Vcc	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) V_{CC} is brought to the proper voltage,
b) V_{PP} is brought to the proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

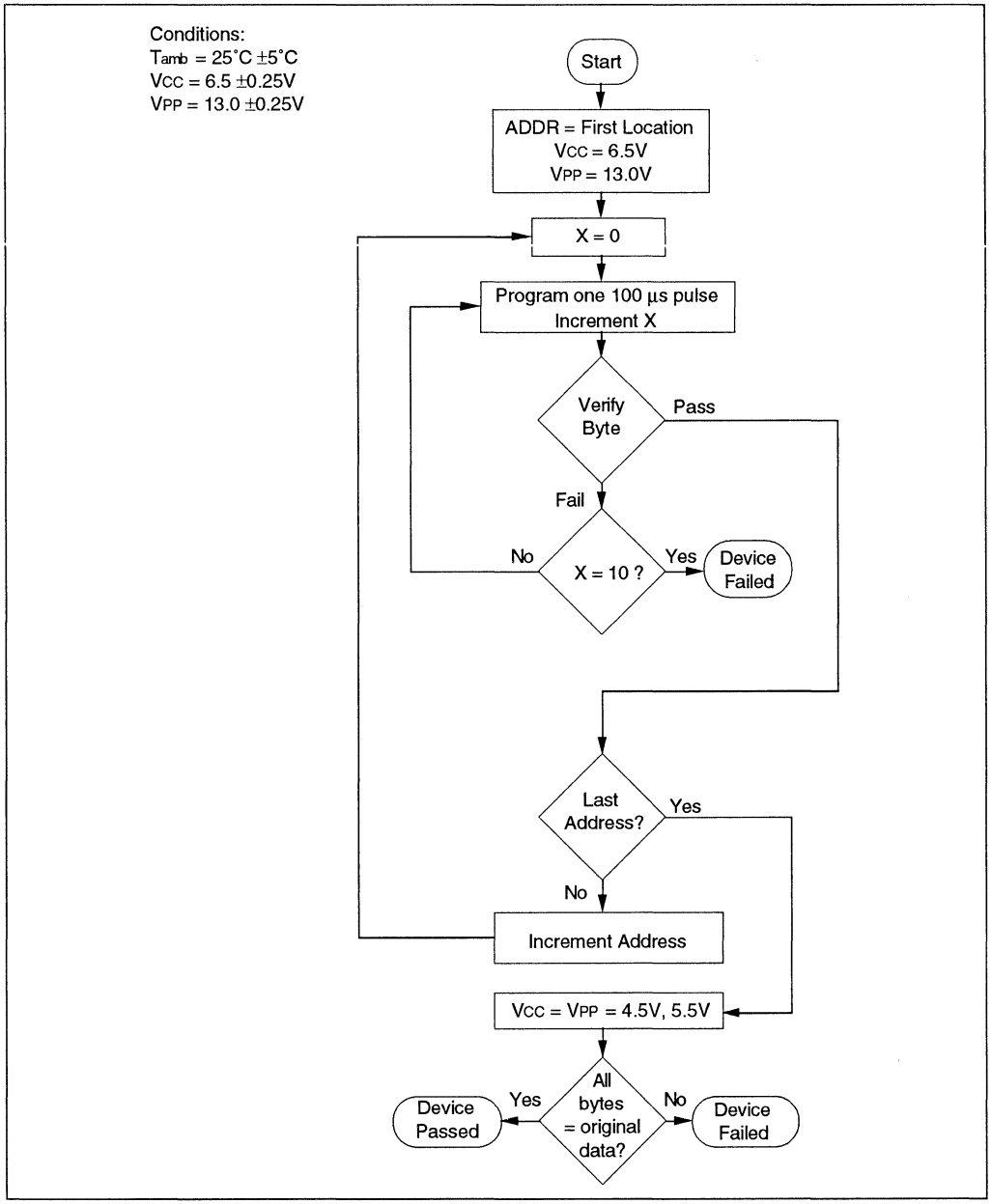
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	0	0	0	0	0	0	1	0	02

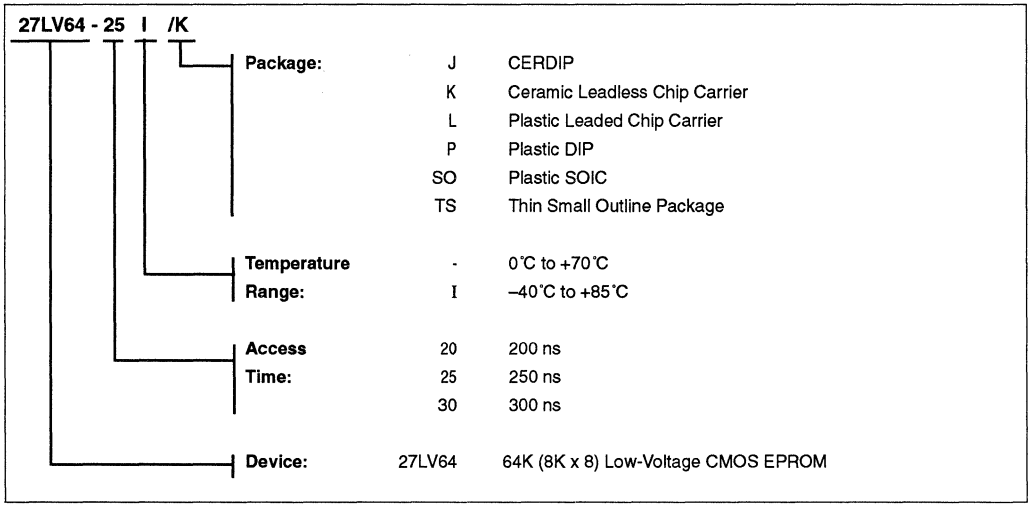
* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27LV64 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

27C128

128K (16K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 120 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 16K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin Chip carrier (leadless or plastic)
  - 28-pin SOIC package
  - 28-pin TSOP package
  - Tape and reel
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

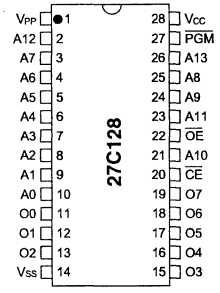
DESCRIPTION

The Microchip Technology Inc. 27C128 is a CMOS 128K bit (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

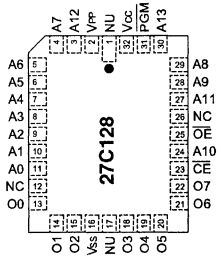
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

PACKAGE TYPE

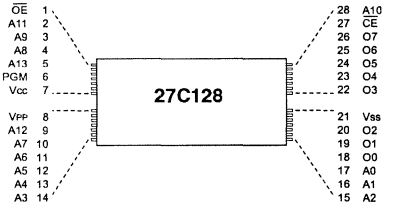
DIP/SOIC



PLCC/LCC



TSOP



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = VCC ± 0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

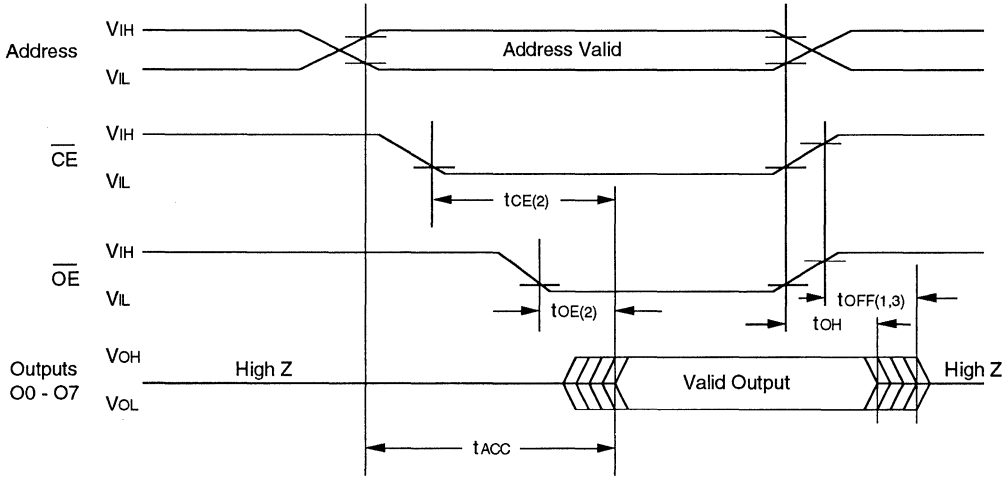
Note 2: VCC must be applied before VPP, and be removed simultaneously or after VPP.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100 pF	
Input Rise and Fall Times:	10 ns	
Ambient Temperature:	Commercial:	Tamb = 0°C to +70°C
	Industrial:	Tamb = -40°C to +85°C
	Extended (Automotive):	Tamb = -40°C to +125°C

Parameter	Sym	27C128-12		27C128-15		27C128-17		27C128-20		27C128-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$=$\overline{OE}$=V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$=V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}$=V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t_{OH}	0	—	0	—	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = 13.0V ± 0.25V						
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	IPP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

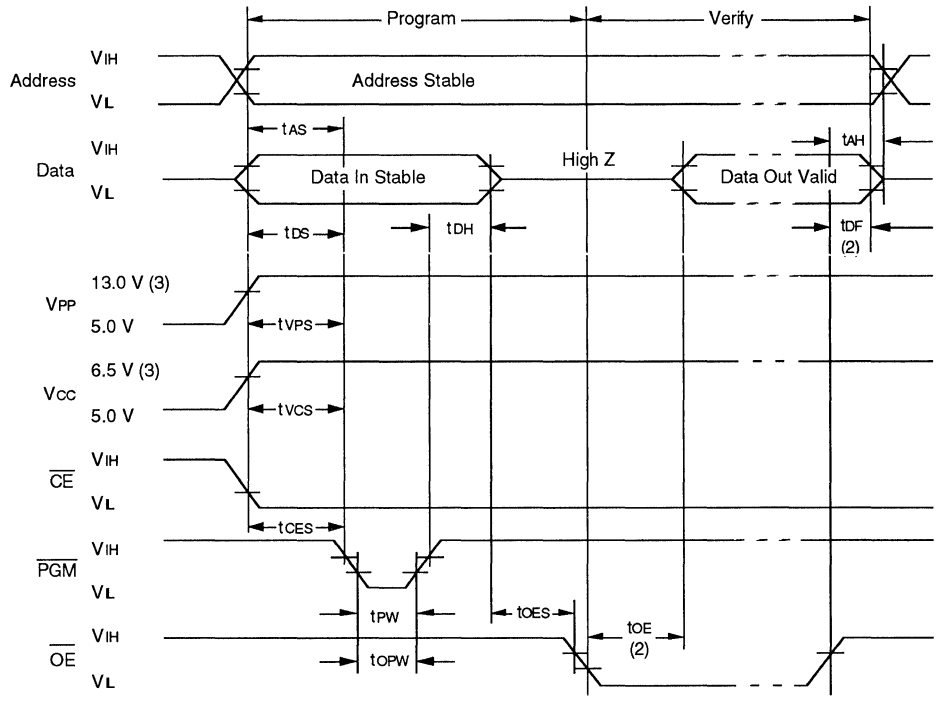
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Ambient Temperature: Tamb=25°C± 5°C VCC= 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference is 0.8V for VIL and 2.0V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for Express algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) VPP is brought to the proper VH level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A13 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) VPP is at the proper VH level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

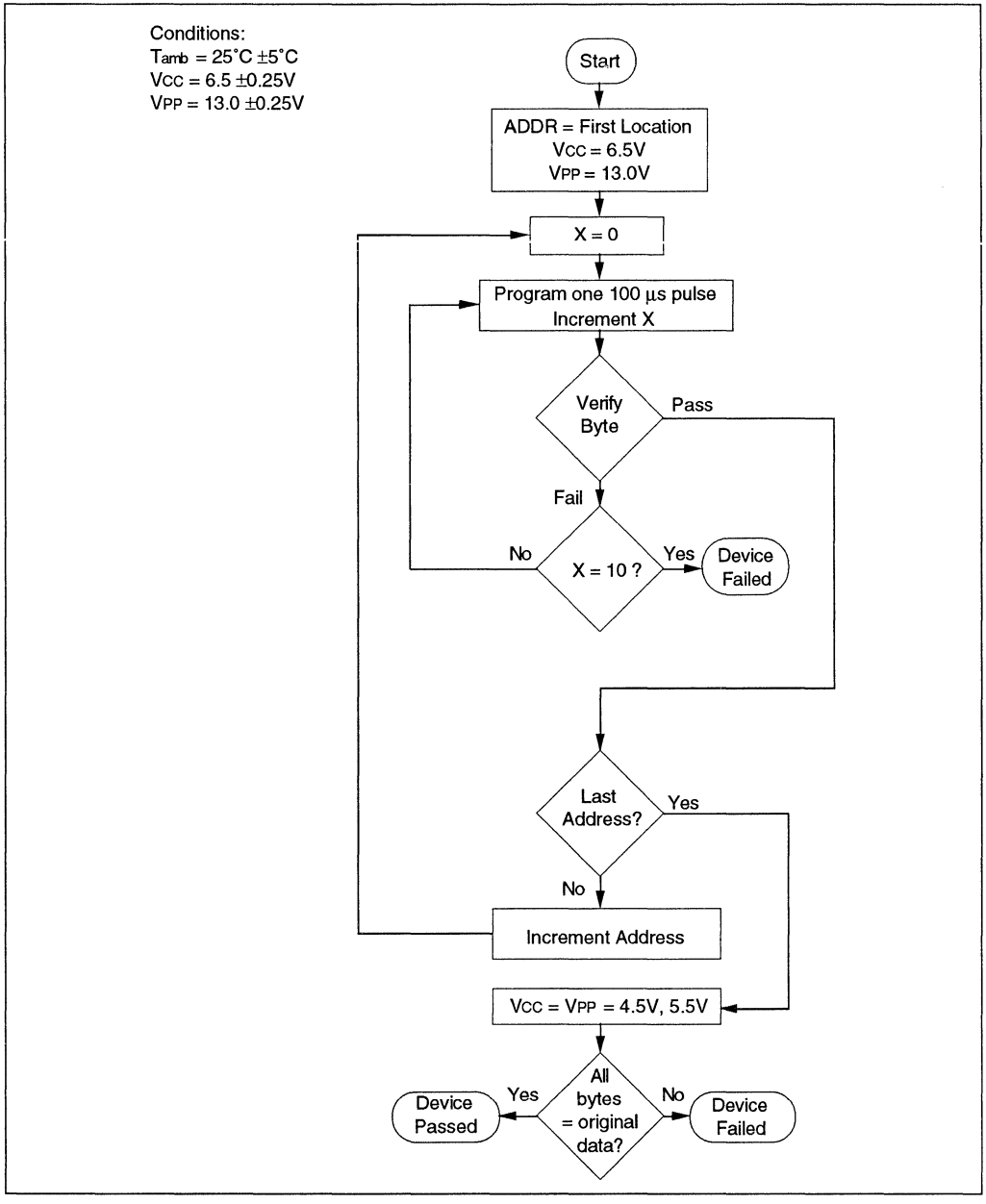
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	0	0	1	1	83

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C128 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27C128 - 25 I /P

Package:	J	CERDIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package (TSOP) 8X13.4mm
Temperature Range:	-	0°C to +70°C
	I	–40°C to +85°C
	E	–40°C to +125°C
Access Time:	12	120 ns
	15	150 ns
	17	170 ns
	20	200 ns
	25	250 ns
Device:	27C128	128K (16K x 8) CMOS EPROM

MICROCHIP

27C256

256K (32K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 90 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin Chip carrier (leadless or plastic)
  - 28-pin SOIC package
  - 28-pin Thin Small Outline Package (TSOP)
  - 28-pin Very Small Outline Package (VSOP)
  - Tape and reel
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

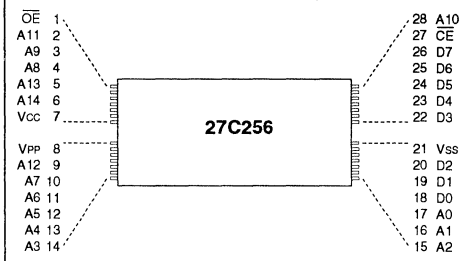
DESCRIPTION

The Microchip Technology Inc. 27C256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

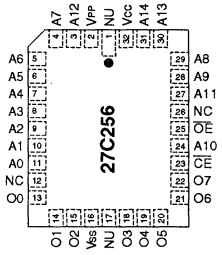
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

PACKAGE TYPE

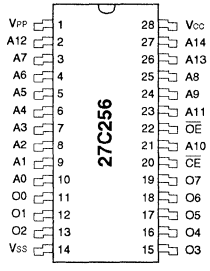
TSOP



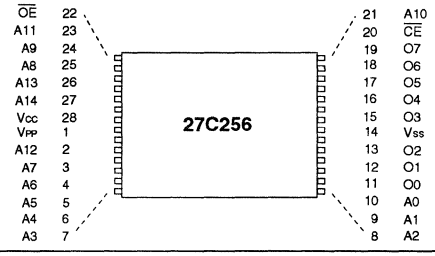
PLCC/LCC



DIP/SOIC



VSOP



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} and input voltages w.r.t. V_{SS} ..... -0.6V to +7.25V

V_{PP} voltage w.r.t. V_{SS} during programming ..... -0.6V to +14.0V

Voltage on A9 w.r.t. V_{SS} ..... -0.6V to +13.5V

Output voltage w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage
O0 - O7	Data Output
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

V_{CC} = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.5	V_{CC}+1 0.8	V V	
Input Leakage	all	—	I_{LI}	-10	10	µA	V_{IN} = 0 to V_{CC}
Output Voltages	all	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
Output Leakage	all	—	I_{LO}	-10	10	µA	V_{OUT} = 0V to V_{CC}
Input Capacitance	all	—	C_{IN}	—	6	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C_{OUT}	—	12	pF	V_{OUT} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	I_{CC1} I_{CC2}	— —	20 25	mA mA	V_{CC} = 5.5V; V_{PP} = V_{CC} f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = V_{IL}; I_{OUT} = 0 mA; V_{IL} = -0.1 to 0.8V; V_{IH} = 2.0 to V_{CC}; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	$I_{CC(S)}$	—	2 3 100	mA mA µA	 $\overline{CE}$ = V_{CC} ± 0.2V
I_{PP} Read Current V_{PP} Read Voltage	all all	Read Mode Read Mode	I_{PP} V_{PP}	 V_{CC}-0.7	100 V_{CC}	µA V	V_{PP} = 5.5V Note 2

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

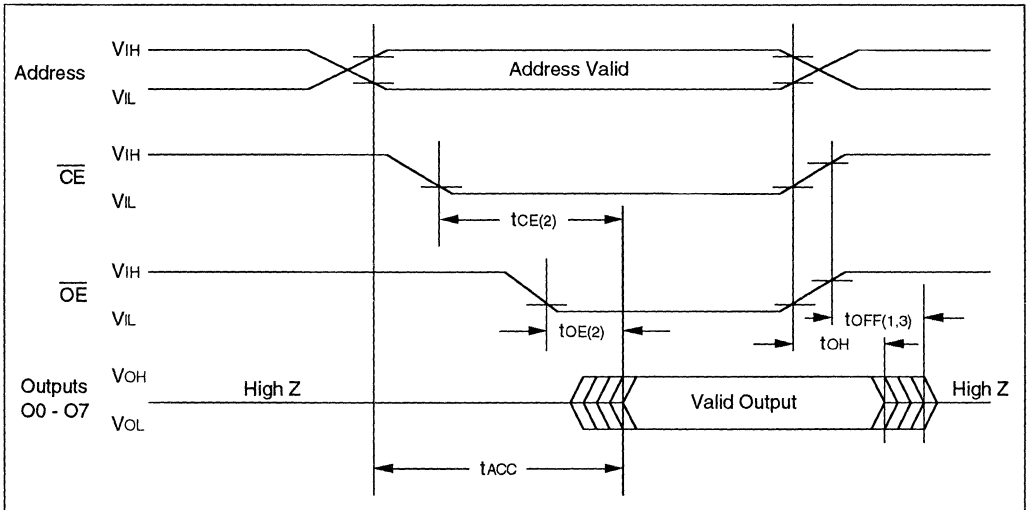
Note 2: V_{CC} must be applied before V_{PP}, and be removed simultaneously or after V_{PP}.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Automotive: Tamb = -40°C to +125°C													
Parameter	Sym	27C256-90*		27C256-10*		27C256-12		27C256-15		27C256-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE}$=$\overline{OE}$ =V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	40	—	45	—	55	—	65	—	75	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

* -10, -90 AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30pF

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

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TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic"1" Logic"0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

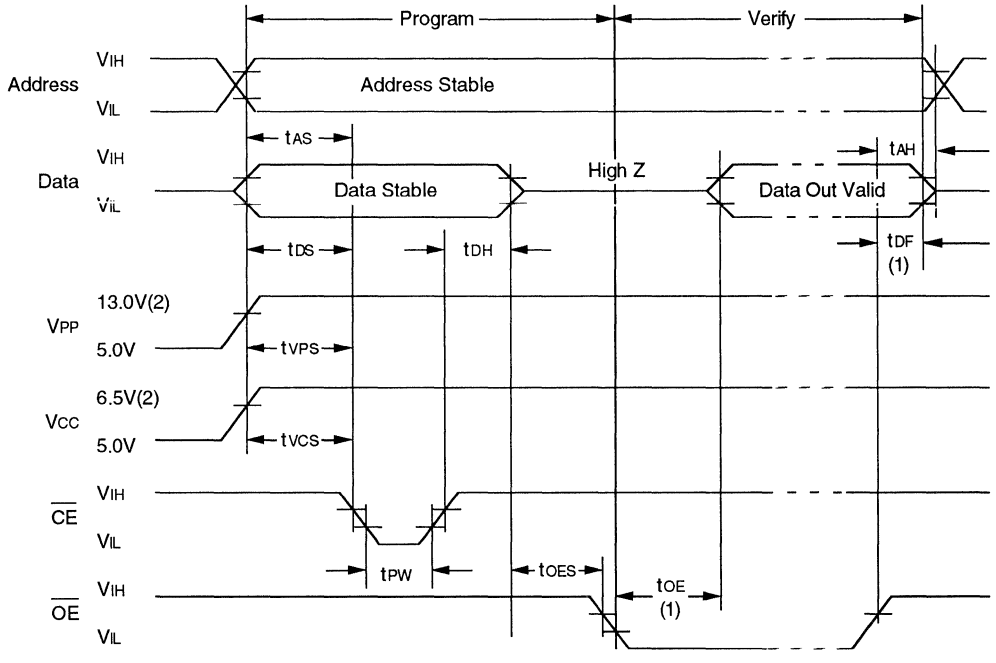
Note 1: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH}=2.4V and V_{IL}=0.45V; V_{OH}=2.0V; V_{OL}=0.8V Output Load: 1 TTL Load + 100pF Ambient Temperature: Tamb=25°C ± 5°C V_{CC}= 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
V_{PP} Set-Up Time	t_{VPS}	2	—	µs	
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5 V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	OE	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when:

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and the program mode is not defined.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) VPP is brought to the proper VH level,
c) the $\overline{OE}$ pin is high, and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) VPP is at the proper VH level,
c) the $\overline{CE}$ line is high, and
d) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

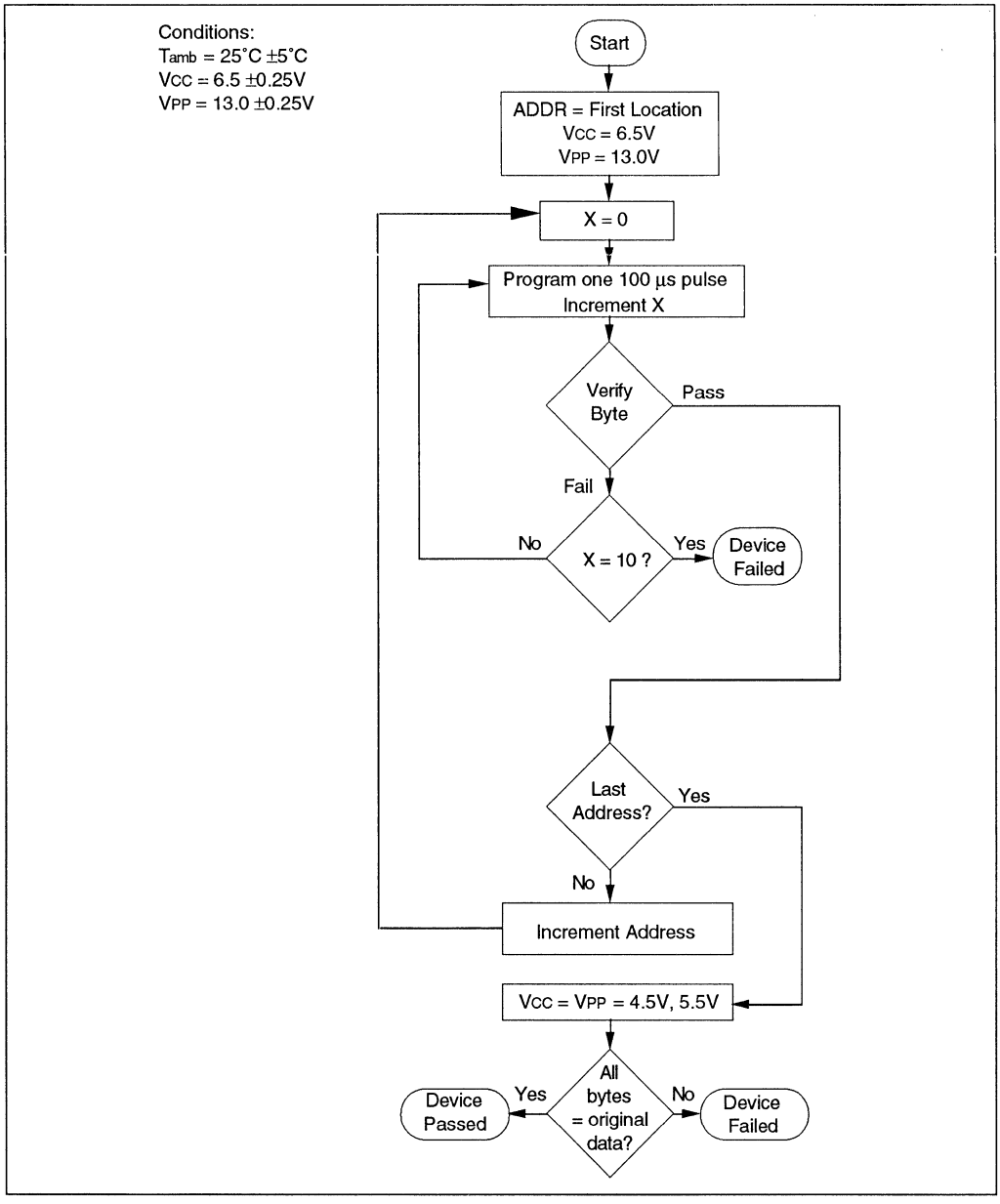
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	1	1	0	0	8C

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C256 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27C256 - 90 I /TS

Package:	J		CERDIP
	K		Ceramic Leadless Chip Carrier
	L		Plastic Leaded Chip Carrier
	P		Plastic DIP
	SO		Plastic SOIC
	TS		Thin Small Outline Package (TSOP) 8x20mm
	VS		Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	-		0°C to +70°C
	I		–40°C to +85°C
	E		–40°C to +125°C
Access Time:	90		90 ns
	10		100 ns
	12		120 ns
	15		150 ns
	20		200 ns
Device		27C256	256K (32K x 8) CMOS EPROM

27HC256

256K (32K x 8) High-Speed CMOS EPROM

FEATURES

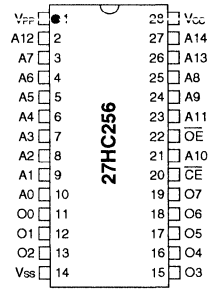
- High speed performance
  - 55 ns access time available
- CMOS Technology for low power consumption
  - 55 mA Active current
  - 100 µA Standby current
- OTP (one time programming) available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line and SOIC package
  - 32-pin Chip carrier (leadless or plastic)
  - 28-pin Very Small Outline Package (VSOP)
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

DESCRIPTION

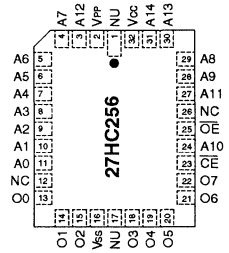
The Microchip Technology Inc. 27HC256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words of 8 bits each. Advanced CMOS technology allows bipolar speed with a significant reduction in power. A low power option (L) allows further reduction in the standby power requirement to 100 µA The 27HC256 is configured in a standard 256K EPROM pinout which allows an easy upgrade for present 27C256 users. A complete family of packages are offered to provide the utmost flexibility. The 27HC256 allows high performance microprocessors to run at full speed without the need of wait states. CMOS design and processing makes this part suitable for applications where high reliability and reduced power consumption are essential.

PACKAGE TYPE

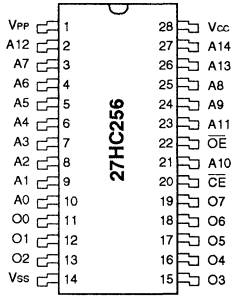
DIP



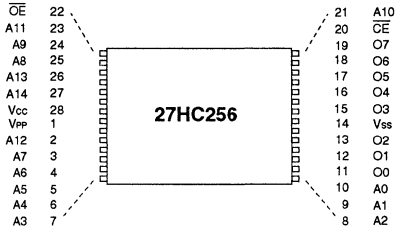
PLCC/LCC



SOIC



VSOP



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} and input voltages w.r.t. V_{SS} ..... -0.6V to +7.25V

V_{PP} voltage w.r.t. V_{SS} during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. V_{SS} ..... -0.6V to +13.5V

Output voltage w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V

Temperature under bias ..... -65°C to +125°C

Storage temperature ..... -65°C to +150°C

Maximum exposure to UV ..... 7258Wsec/cm^2

ESD protection on all pins ..... 2 KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage
O0 - O7	Data Output
V_{CC}	+5V
V_{SS}	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

V_{CC} = +5V ±10%
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	all		I_{LI}	-10	10	µA	V_{IN} = -0.1V to V_{CC} +1.0V
Output Voltages	all	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -4 µA I_{OL} = 16 mA
Output Leakage	all	—	I_{LO}	-10	10	µA	V_{OUT} = -0.1V to V_{CC} +0.1V
Input Capacitance	all	—	C_{IN}	—	6	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C_{OUT}	—	12	pF	V_{OUT} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	I_{CC1} I_{CC2}	— —	55 65	mA mA	V_{CC} = 5.5V; V_{PP} = V_{CC} f = 2 MHz; $\overline{OE}$ = $\overline{CE}$ = V_{IL}; I_{OUT} = 0 mA; V_{IL} = -0.1 to 0.8V; V_{IH} = 2.0 to V_{CC}; Note 1
Power Supply Current, Standby, Std	C I,E	— —	$I_{CC(S)1}$	—	35 40	mA mA	
Power Supply Current, Standby, "L" version (low power)	C I,E I,E	TTL input TTL input CMOS input	$I_{CC(S)2}$	—	2 3 100	mA mA µA	 $\overline{CE}$ = V_{CC} ± 0.2V
I_{PP} Read Current V_{PP} Read Voltage	all all	Read Mode Read Mode	I_{PP} V_{PP}	V_{CC} -0.7	100 V_{CC}	µA V	V_{PP} = 5.5V Note 2

* Parts: C=Commercial Temperature Range; L = Low Power; I, E=Industrial and Extended Temperature Ranges

Note 1: Active current increases 3 mA per MHz for Commercial part or 5mA per MHz for Industrial or Extended temperature parts up to operating frequency.

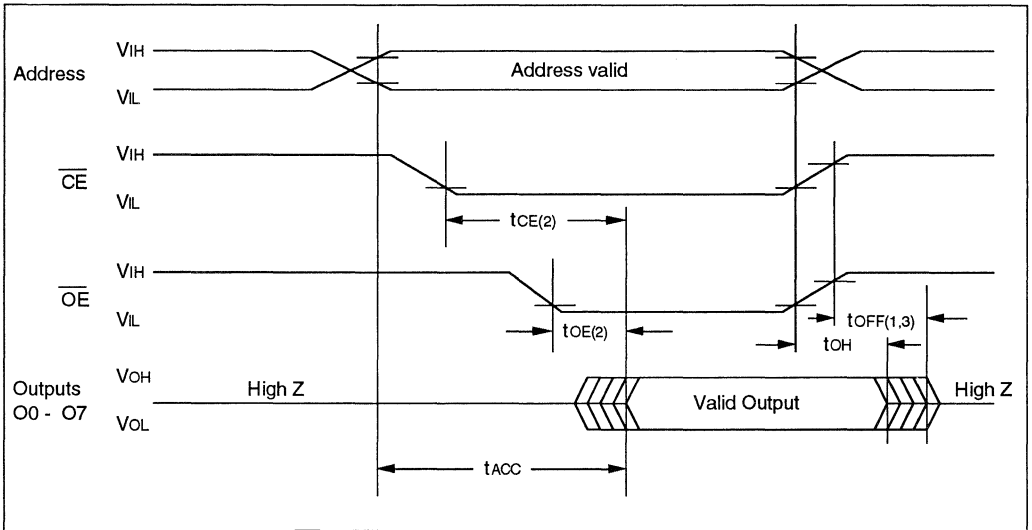
Note 2: V_{CC} must be applied simultaneously or before V_{PP}, and be removed simultaneously or after V_{PP}.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V Output Load: 1 TTL Load + 30 pF Input Rise and Fall Times: 5 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Extended (Automotive): Tamb = -40°C to +125°C										
Parameter	**Part***	**Sym**	**27HC256-55**		**27HC256-70**		**27HC256-90**		**Units**	**Conditions**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	all	t_{ACC}	—	55	—	70	—	90	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	L S	t_{CE1} t_{CE2}	—	55 45	—	70 45	—	90 50	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	t_{OE}	—	30	—	35	—	40	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	25	0	30	0	35	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	t_{OH}	0	—	0	—	0	—	ns	

* Parts: S = Standard Power; L = Low Power

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4 —	— 0.45	V V	IOH = -4 mA IOL = 16 mA
VCC Current, program & verify	—	ICC	—	55	mA	
VPP Current, program	—	IPP	—	30	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

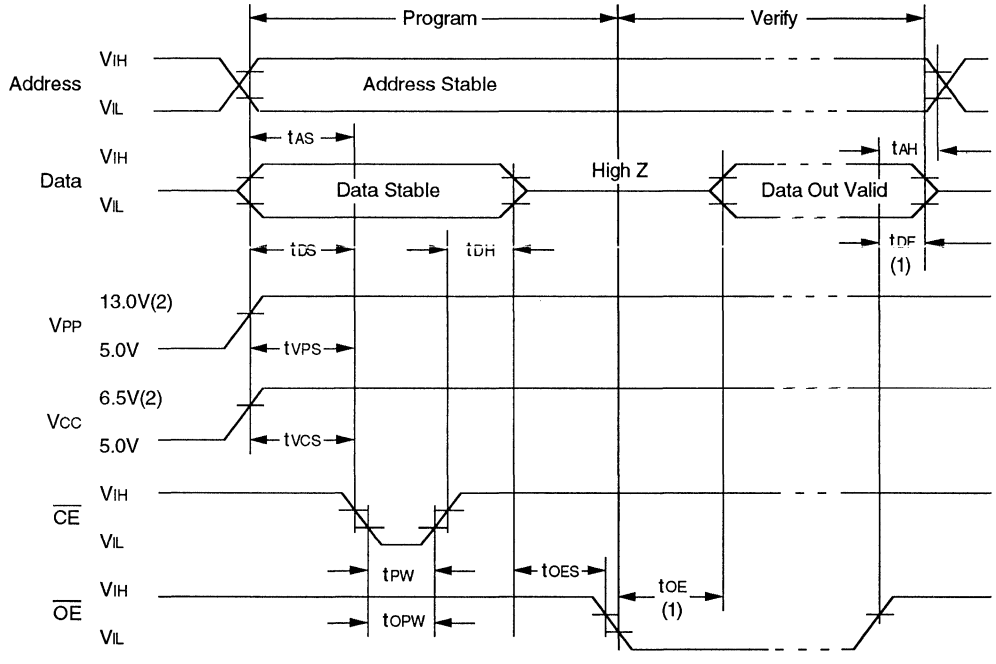
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Ambient Temperature: Tamb=25°C ± 5°C VCC= 6.5V ± 0.25V, VPP =13.0V ± 0.25V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

2.0 FUNCTIONAL DESCRIPTION

The 27HC256 has the following functional modes:

- Operation: The 27HC256 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.
- Programming: To receive its permanent data, the 27HC256 must be programmed. Both a program and program/verify procedure are available. It can be programmed with the "Express" algorithm.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

2.1 Operations

- Read
- Standby
- Output Disable

For the general characteristics in these operation modes, refer to the table above.

2.2 Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC256's memory data is accessed when

- the chip is enabled by setting the $\overline{CE}$ pin low.
- the data is gated to the output pins by setting the $\overline{OE}$ pin low

For Read operations on the Low Power version, once the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). A faster $\overline{CE}$ access time (t_{CE}) is available on the standard part to provide the additional time for decoding the $\overline{CE}$ signal. Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$

2.3 Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and a program mode is not defined. When these conditions are met, the supply current will drop from 55 mA to 100 µA on the low power part, and to 35 mA on the standard part.

2.4 Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

2.5 Programming Algorithms

The Express algorithm has been developed to improve programming throughput times in a production environment. Up to 10 pulses of 100 µs each are applied until the byte is verified. No over-programming is required. A flowchart of this algorithm is shown in Figure 2-1.

The programming mode is entered when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low

Since the erased state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A14, and the data is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

2.6 Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper VH level
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is high, an
d) the $\overline{OE}$ line is low.

2.7 Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed, and all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

2.8 Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

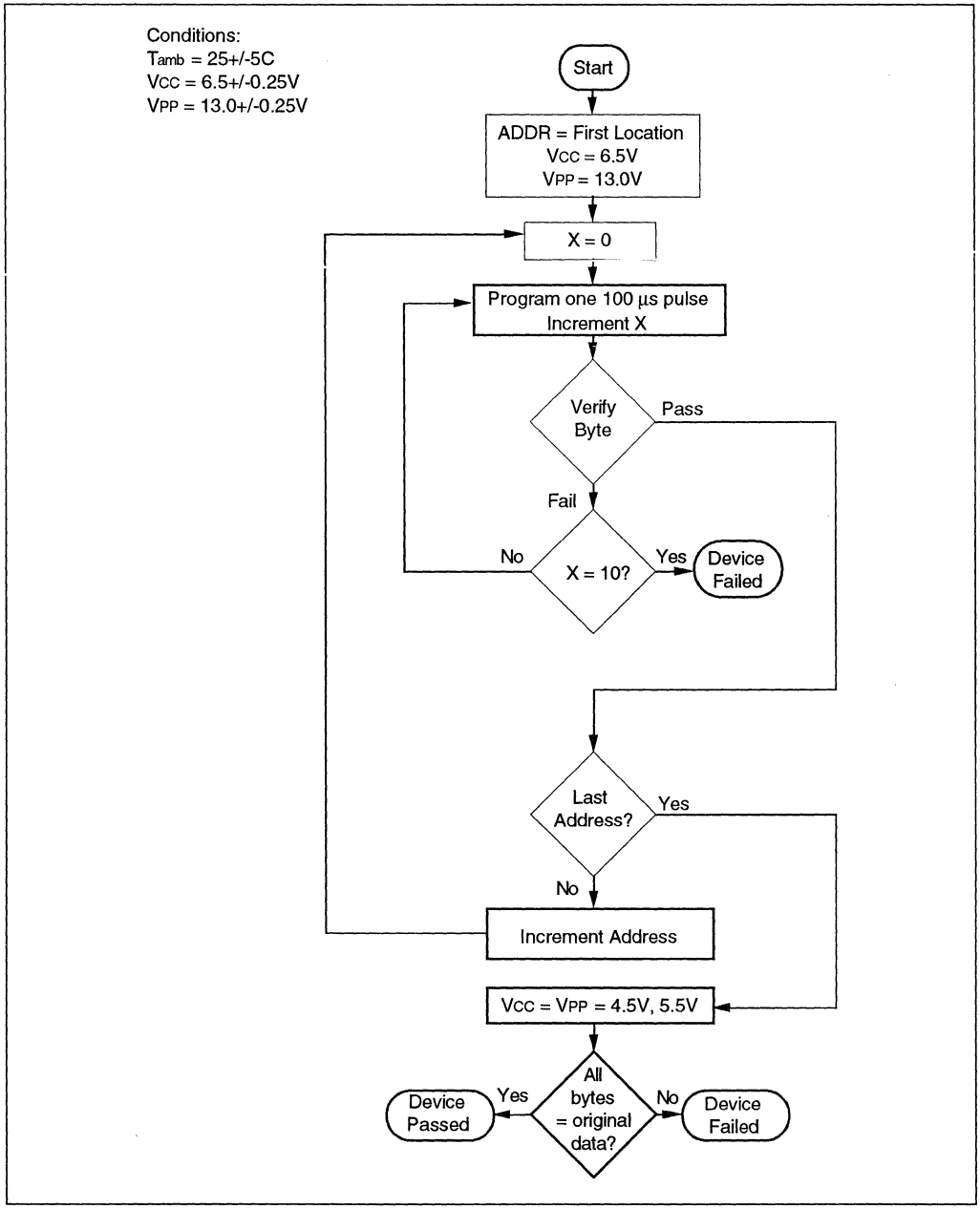
Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	0	0	94

2.9 Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state when exposed to ultraviolet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537 Å with an intensity of 12,000µW/cm^2 at 1". The erasure time at that distance is about 15 to 20 min.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

FIGURE 2-1: PROGRAMMING EXPRESS ALGORITHM



7

27HC256 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27HC256 L - 55 I /SO

Package:	J	CERDIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	VS	Very Small Outline Package (VSOP) 8x13.4mm
Temperature Range:	-	0°C to +70°C
	I	–40°C to +85°C
	E	–40°C to +125°C
Access Time:	55	55 ns
	70	70 ns
	90	90 ns (SOIC only)
Power Type:	-	Standard Power
	L	Low Power
Device:	27HC256	256K (32K x 8) High-Speed EPROM

MICROCHIP

27LV256

256K (32K x 8) Low-Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  - 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  - 8 mA Active current at 3.0V
  - 20 mA Active current at 5.5V
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC package
  - 28-pin SOIC package
  - 28-pin VSOP package
  - Tape and reel
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

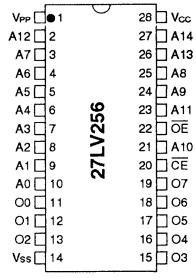
DESCRIPTION

The Microchip Technology Inc. 27LV256 is a low voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 32K x 8 (32K-Byte) non-volatile memory product. The 27LV256 consumes only 8 mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low voltage applications where conventional 5.0 volt only EPROMS can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0V. This device allows systems designers the ability to use low voltage non-volatile memory with today's' low voltage microprocessors and peripherals in battery powered applications.

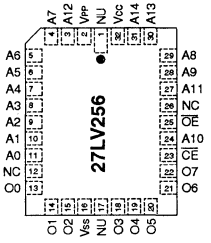
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPE

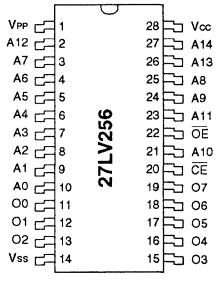
PDIP



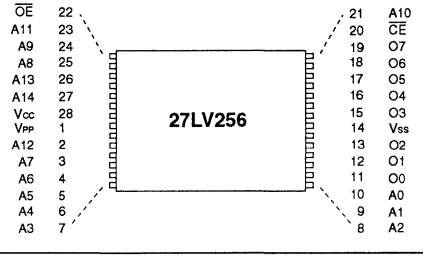
PLCC



SOIC



VSOP



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V or +3V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V ±10% or 3.0V where indicated
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	20 @ 5.0V 8 @ 3.0V 25 @ 5.0V 10 @ 3.0V	mA mA mA mA	VCC = 5.5V; VPP = VCC f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)	—	1 @ 3.0V 2 @ 3.0V 100 @ 3.0V	mA mA µA	 $\overline{CE}$=VCC ± 0.2V

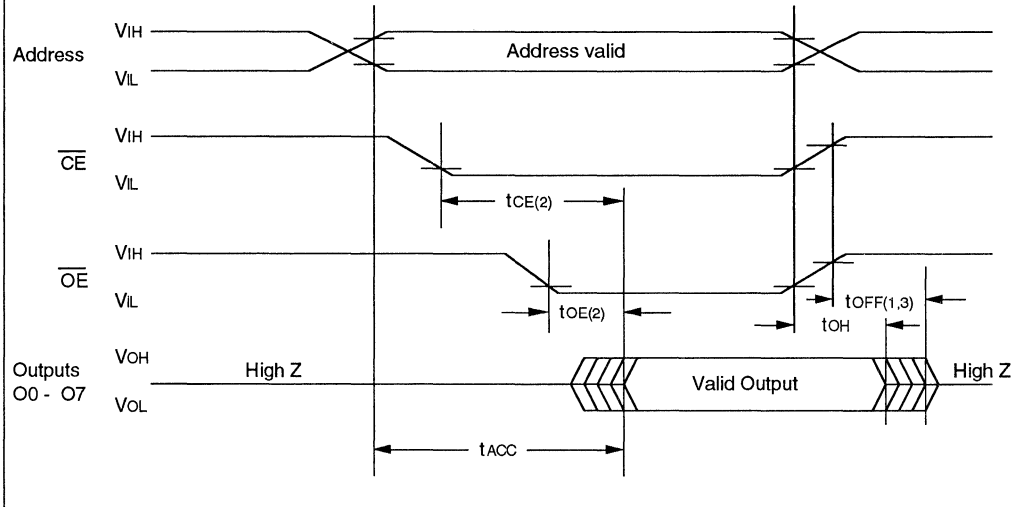
* Parts: C=Commercial Temperature Range
I =Industrial Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C									
Parameter	**Sym**	**27HC256-20**		**27HC256-25**		**27HC256-30**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	100	—	125	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, VPP = 13.0V ± 0.25V			
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic"1" Logic"0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	20	mA	Note 1
VPP Current, program	—	IPP2	—	25	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

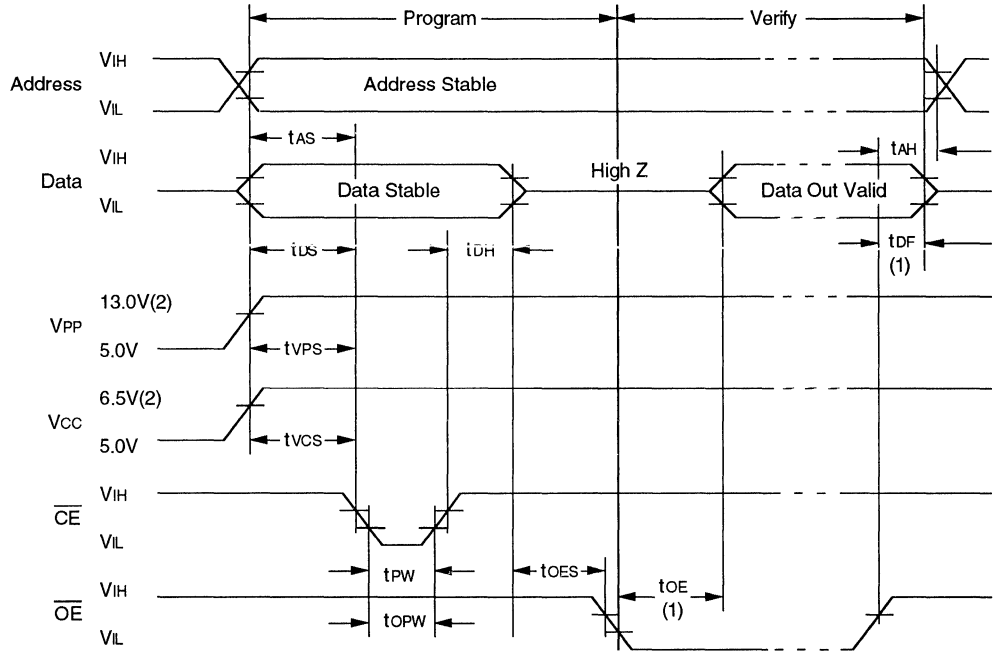
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Output Load: 1 TLL Load + 100pF Ambient Temperature: Tamb=25°C±5°C VCC= 6.5V ± 0.25V, VPP =13.0V ± 0.25V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when:

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined. Output Disable

1.4 Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and program mode is not defined.

1.5 Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No over-programming is required. A flowchart of the express algorithm is shown in Figure 1.

Programming takes place when:

a) V_{CC} is brought to the proper voltage
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

1.6 Verify

After the array has been programmed it must be verified to ensure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{CE}$ pin is high
d) the $\overline{OE}$ line is low

1.7 Inhibit

When Programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed, and all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

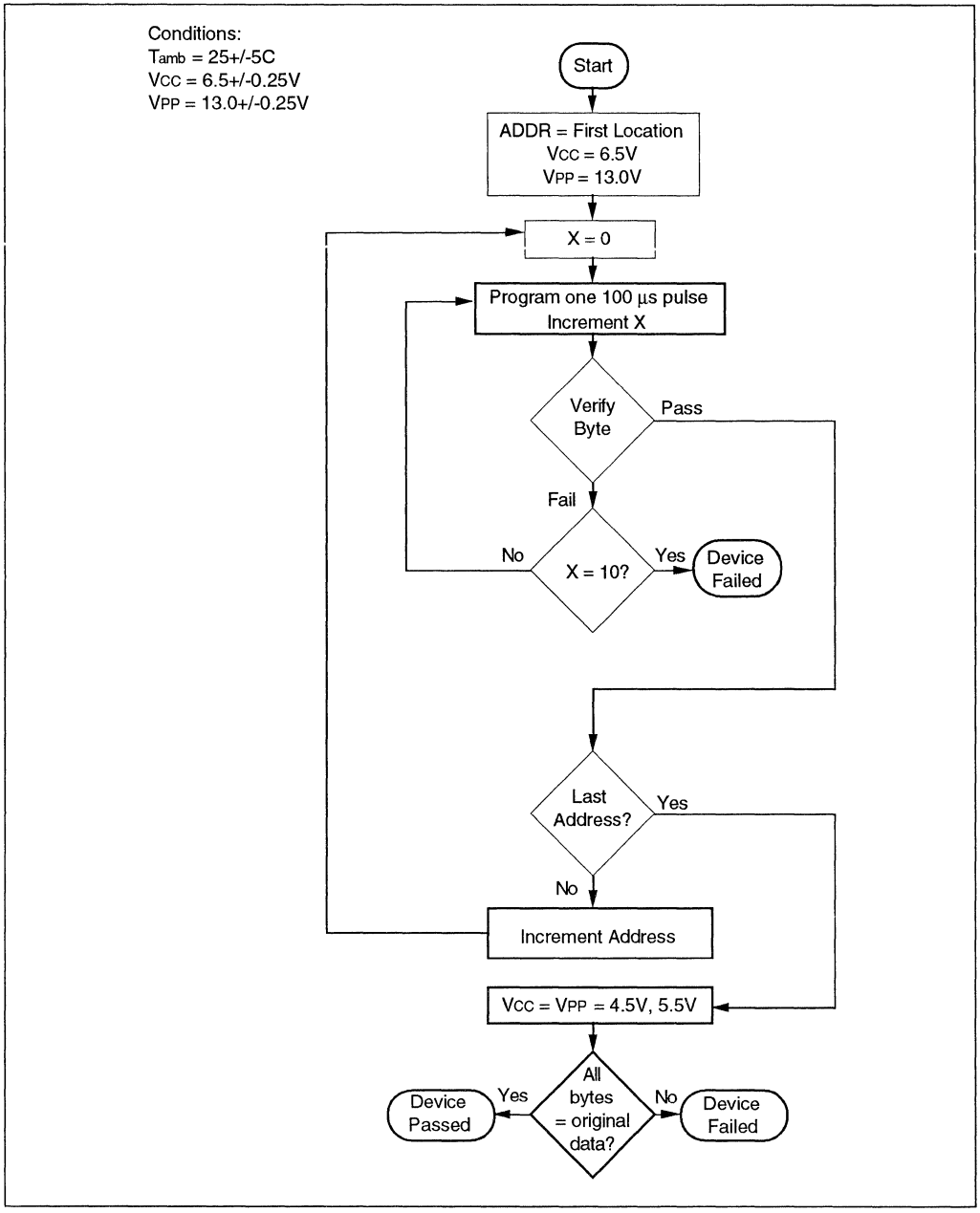
1.8 Identity Mode

In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27LV256 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27LV256 - 25 I /P

Package:	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	VS	Very Small Outline Package (VSOP) 8X13.4mm
Temperature Range:	-	0°C to +70°C
	I	–40°C to +85°C
Access Time:	20	200 ns
	25	250 ns
	30	300 ns (SOIC only)
Device:	27LV256	256K (32K x 8) Low-Voltage CMOS EPROM

MICROCHIP

27HC1616

256K (16K x 16) High-Speed CMOS EPROM

FEATURES

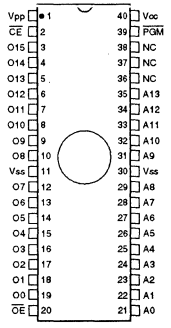
- 16 bit configuration
- High speed performance
  - 55 ns access time available
- CMOS Technology for low power consumption
  - 90 mA Active current
  - 50 mA Standby current
- Worldwide architecture offers space saving over Bytewide memories
- Organized 16K x 16: JEDEC standard pinouts
  - 40-Pin ceramic dual in line package
  - 44-Pin ceramic leadless chip carrier
- Temperature range available:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

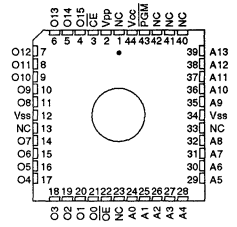
The Microchip Technology Inc. 27HC1616 is a CMOS 16K x 16 (256K) Programmable Read Only Memory. The device operates at Bipolar PROM speeds but uses far less current than any Bipolar PROM. The 27HC1616 is an excellent choice for any application requiring blazing speeds and low power consumption. The word wide (16 bit) architecture can replace two 8 bit EPROMS in any 16 bit application saving valuable printed circuit space and components costs. Typical applications for the 27HC1616 include automotive systems control, high speed modems, digital signal processing, or any application that uses the 80386, 68030, 29000, etc. high performance microprocessors.

PACKAGE TYPE

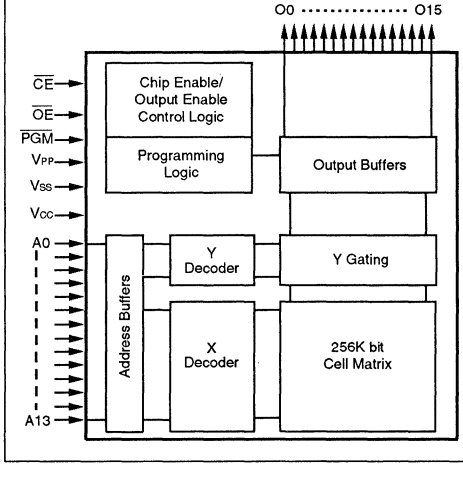
DIP



LCC



BLOCK DIAGRAM



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Temperature under bias ..... -65°C to +125°C

Storage temperature ..... -65°C to +150°C

ESD protection on all pins ..... 2 KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
VPP	Programming Voltage
O0 - O15	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V ±10%
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = -0.1 to VCC + 1.0V
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 2 mA IOL = 8 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = -0.1V to VCC + 0.1V
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	all	TTL input	ICC	—	90	mA	VCC = 5.5V; VPP = VCC f = 2 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	all	—	ICC	—	50	mA	
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

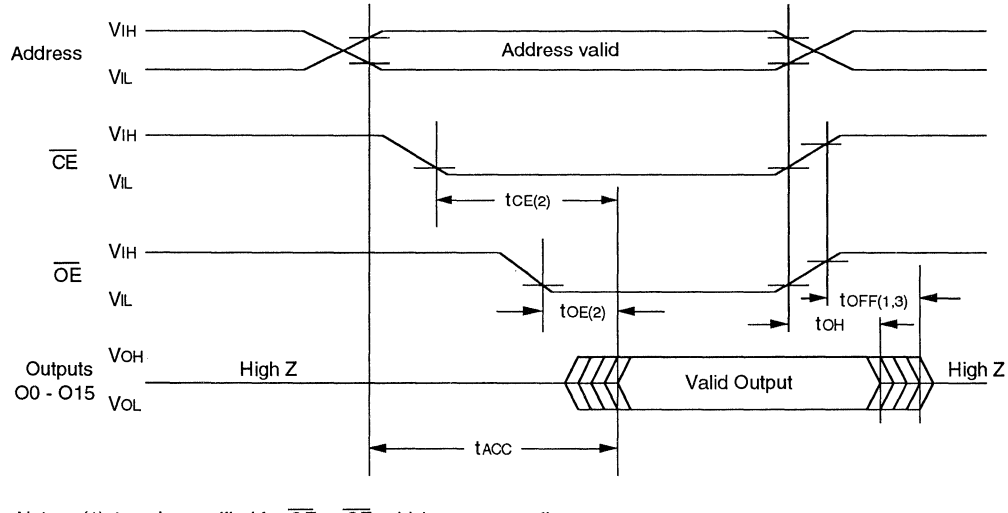
Note 1: Active current increases 2 mA per MHz up to operating frequency.
Note 2: VCC must be supplied simultaneously or before VPP and be removed simultaneously or after VPP.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 ns
Ambient Temperature: Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part	Sym	27HC1616-55		27HC1616-70		Units	Conditions
			Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}	—	55	—	70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	all	t_{CE2}	—	35	—	45	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	t_{OE}	—	30	—	35	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	20	0	25	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	t_{OH}	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

7

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

			Ambient Temperature: Tamb = 25°C ± 5°C For VPP and VCC Voltages refer to Programming Algorithm			
Parameter	**Status**	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to VCC + 1.0V
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4 —	 0.45	V V	IOH = -2 mA IOL = 8 mA
VCC Current, program & verify	—	ICC	—	90	mA	Note 1
VPP Current, program	—	IPP	—	50	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

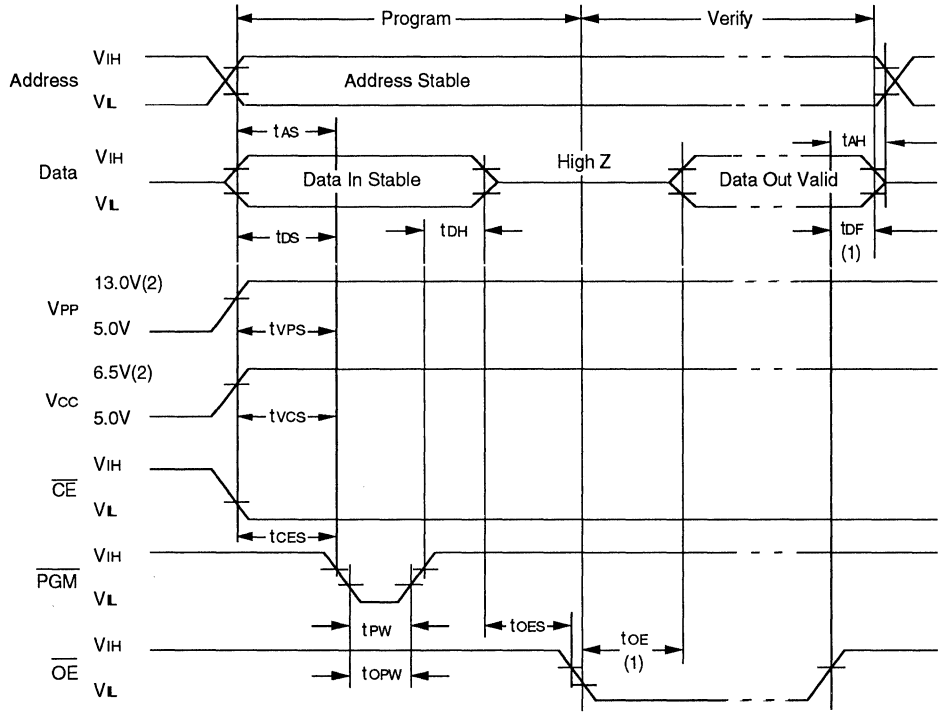
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V, VIL=0.45V; VOH=2.0V and VOL=0.8V Ambient Temperature: Tamb=25°C±5°C For VPP and VCC Voltages, refer to Programming Algorithm				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accomodated by the programmer
(2) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIH	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	X	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care
V_H = 12.0 ± 0.5V

2.0 FUNCTIONAL DESCRIPTION

The 27HC1616 has the following functional modes:

- Operation: The 27HC1616 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.
- Programming: To receive its permanent data, the 27HC1616 must be programmed. Both a program and program/verify procedure is available. The Express programming algorithm is recommended.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

For the general characteristics in these operation and programming modes, refer to the table.

3.0 OPERATION

3.1 Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC1616's memory data is accessed when

- the chip is enabled by setting the $\overline{CE}$ pin low
- the data is gated to the output pins by setting the $\overline{OE}$ pin low

3.2 Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not defined. When these conditions are met, the supply current will drop from 90 mA to 50 mA.

3.3 Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

3.4 Programming/Verification

The 27HC1616 has to be programmed, and afterward the programmed information verified. Before these operations, the Identity Code can be read to properly set up automated equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

3.5 Programming Algorithm

The "Express" algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100 µs each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure 3-1.

Programming takes place when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low
e) the $\overline{PGM}$ pin is pulsed low

Since the erased state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A13, and the data is presented to pins O0 - O15. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

3.6 Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{OE}$ line is low
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ line is high.

3.7 Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{PGM}$ needs to be under separate control to each device. By pulsing the $\overline{PGM}$ line low on a particular device, that device will be programmed, and all other devices with corresponding $\overline{PGM}$ or $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

3.8 Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin →	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	1	1	97

* Code subject to change

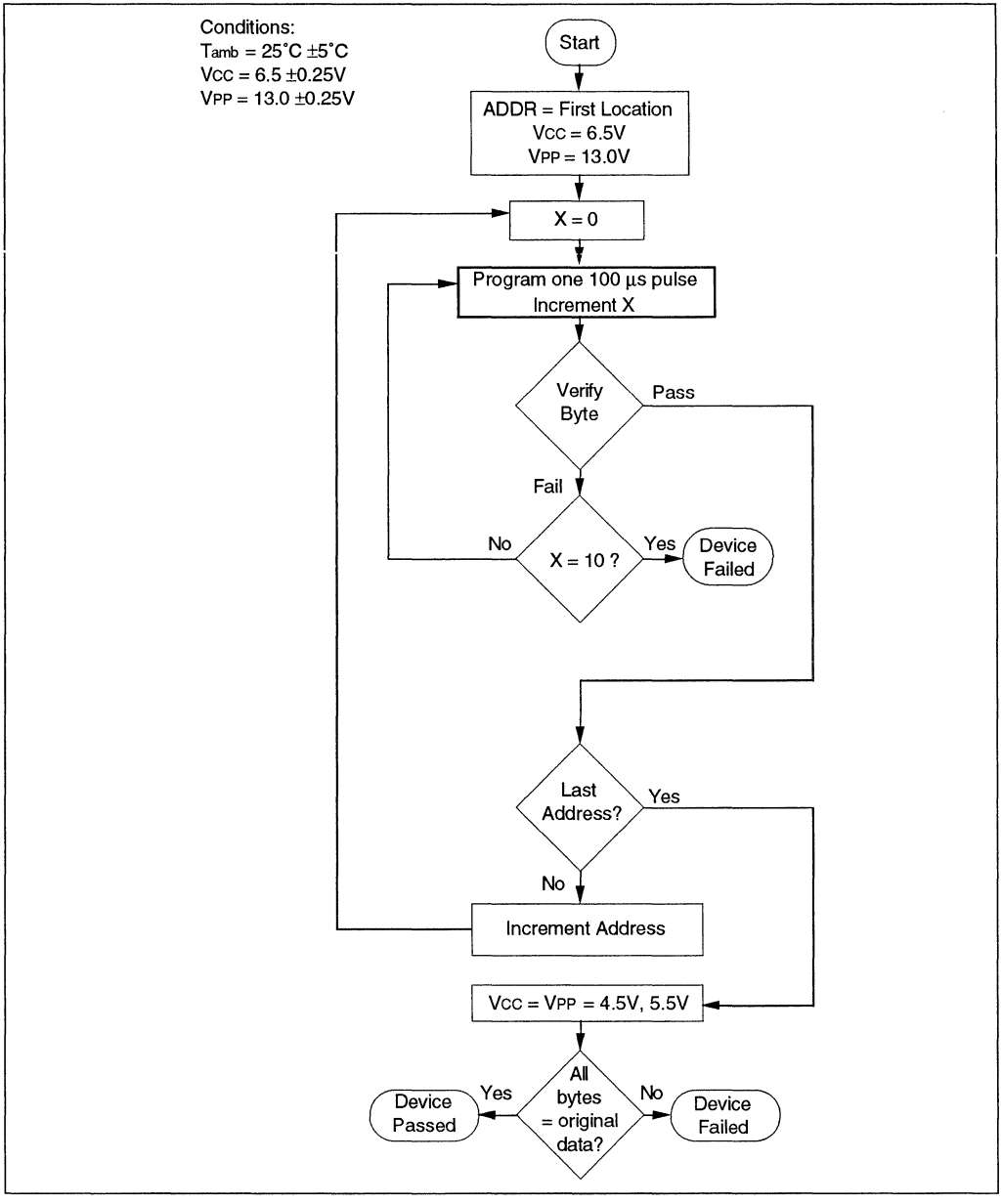
Note 1: O15 - O8 are 00 for the manufacturer and device type code.

3.9 Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537Å with an intensity of 12,000µW/cm^2 at 1". The erasure time at that distance is about 15 to 20 minutes.

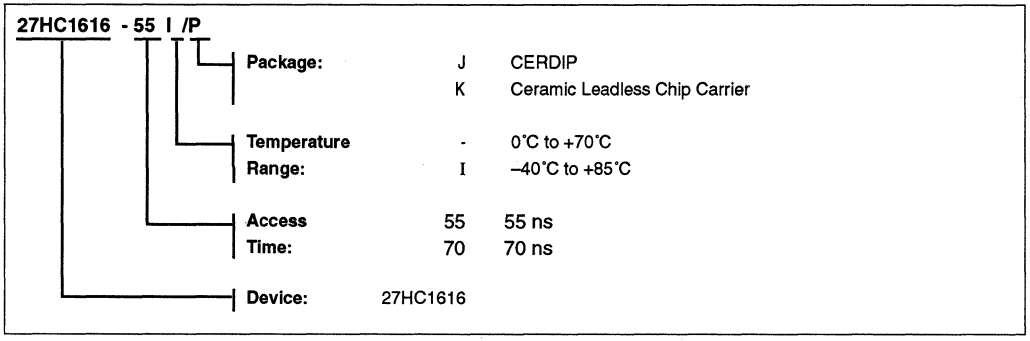
Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

FIGURE 3-1: PROGRAMMING EXPRESS ALGORITHM



27HC1616 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



MICROCHIP

27C512A

512K (64K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 70 ns access time available
- CMOS Technology for low power consumption
  - 25 mA Active current
  - 30 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- High speed express programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin Chip carrier (leadless or plastic)
  - 28-pin SOIC package
  - 28-pin TSOP package
  - 28-pin VSOP package
  - Tape and reel
- Available for the following temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

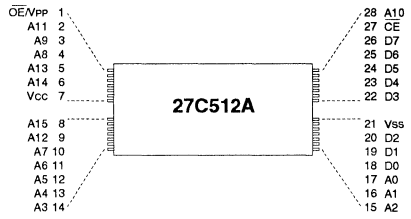
DESCRIPTION

The Microchip Technology Inc. 27C512A is a CMOS 512K bit electrically Programmable Read Only Memory (EPROM). The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 70 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

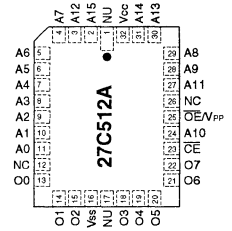
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape or reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

PACKAGE TYPE

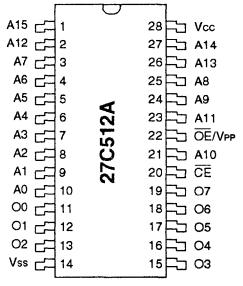
TSOP



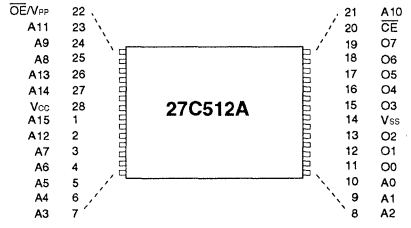
PLCC/LCC



DIP/SOIC



VSOP



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V ±10%
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	ICC ICC	— —	25 35	mA mA	VCC = 5.5V f = 1 MHz; $\overline{OE}$/VPP = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	1 2 30	— — —	mA mA µA	 $\overline{CE}$ = VCC±0.2V

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

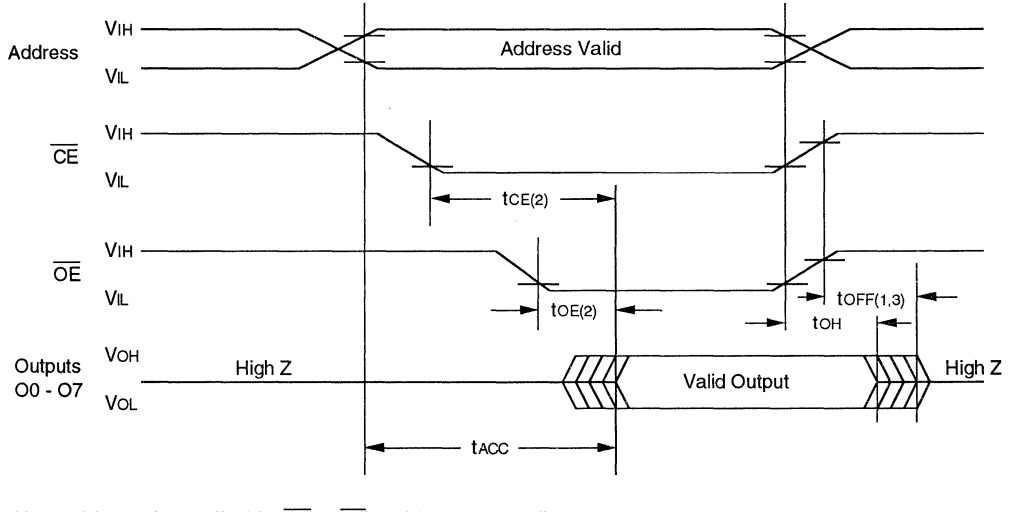
TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 2.0V and V_{OL} = 0.8V	
Output Load:	1 TTL Load + 100 pF	
Input Rise and Fall Times:	10 ns	
Ambient Temperature:	Commercial:	Tamb = 0°C to +70°C
	Industrial:	Tamb = -40°C to +85°C
	Extended (Automotive):	Tamb = -40°C to +125°C

Parameter	Sym	27C512-70*		27C512-90*		27C512-10*		27C512-12		27C512-15		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	70	—	90	—	100	—	120	—	150	ns	$\overline{CE}$ = $\overline{OE}$/ V_{PP} = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	70	—	90	—	100	—	120	—	150	ns	$\overline{OE}$/V_{PP} = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	30	—	40	—	40	—	50	—	60	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to Output High Impedance	t_{OFF}	0	30	0	35	0	35	0	40	0	45	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$/ V_{PP}, whichever occurred first	t_{OH}	0	0	0	—	0	—	0	—	0	—	ns	

*70/90/10 AC Testing Waveforms: V_{IH} = 3.0V and V_{IL} = 0V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, $\overline{OE}$/VPP = VH = 13.0V ± 0.25V						
Parameter	**Status**	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions (See Note 1)**
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4 —	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	35	mA	$\overline{CE}$ = VIL
$\overline{OE}$/VPP Current, program	—	IPP2	—	25	mA	
A9 Product Identification	—	VID	11.5	12.5	V	

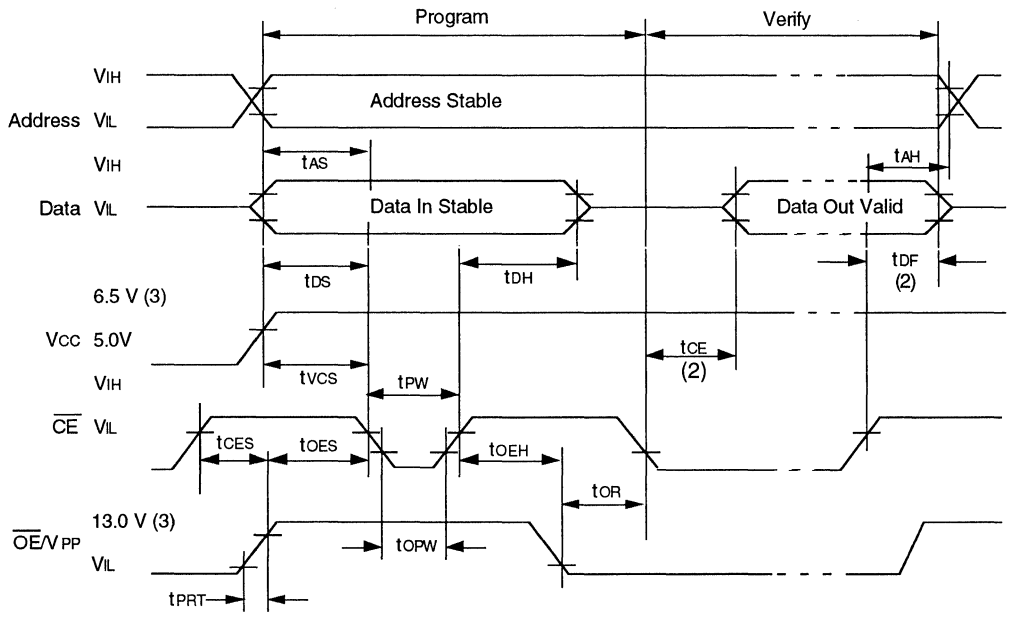
Note 1: VCC must be applied simultaneously or before VPP voltage on $\overline{OE}$/VPP and removed simultaneously or after the VPP voltage on $\overline{OE}$/VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Ambient Temperature: 25°C ±5°C VCC = 6.5V ± 0.25V, $\overline{OE}$/VPP = VH = 13.0V ± 0.25 V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
$\overline{OE}$ Hold Time	tOEH	2	—	µs	
$\overline{OE}$ Recovery Time	tOR	2	—	µs	
$\overline{OE}$ /VPP Rise Time During Programming	tPRT	50	—	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference level is 0.8V for VIL and 2.0V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.5V for express programming algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$/VPP	A9	O0 - O7
Read	VIL	VIL	X	DOUT
Program	VIL	VH	X	DIN
Program Verify	VIL	VIL	X	DOUT
Program Inhibit	VIH	VH	X	High Z
Standby	VIH	X	X	High Z
Output Disable	VIL	VIH	X	High Z
Identity	VIL	VIL	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the CE pin is low to power up (enable) the chip
b) the OE/VPP pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay (tOE) from the falling edge of $\overline{OE}$/VPP.

1.3 Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not identified.

When this conditions are met, the supply current will drop from 25 mA to 30 μA.

1.4 Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in multiple bus microprocessor systems and the outputs go to high impedance when:

- the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

1.5 Erase Mode (UV Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1's" state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 mW/cm^2 for approximately 40 minutes.

1.6 Programming Mode

The Express algorithm must be used for best results. It has been developed to improve programming yields and throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

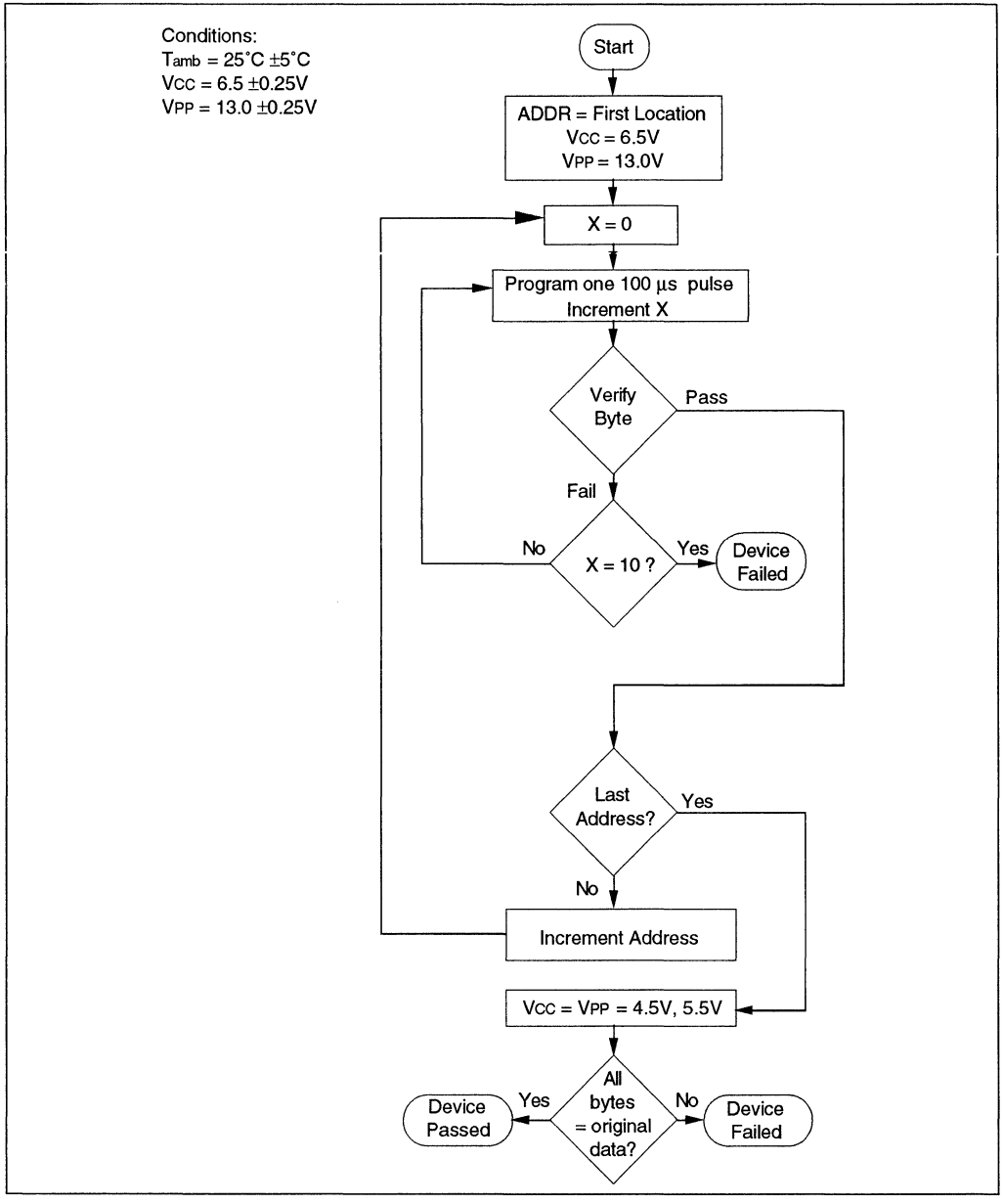
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	1	1	0	0	0D

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C512A Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27C512A - 70 I /P

Package:	J	CERDIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	TS	Thin Small Outline Package(TSOP) 8x20mm
	VS	Very Small Outline Package(VSOP) 8x13.4mm
Temperature Range:	-	0°C to +70°C
	I	–40°C to +85°C
	E	–40°C to +125°C
Access Time:	70	70 ns
	90	90 ns
	10	100 ns
	12	120 ns
	15	150 ns
Device:	27C512A	512K (64K x 8) CMOS EPROM

MICROCHIP

27LV512

512K (64K x 8) Low-Voltage CMOS EPROM

FEATURES

- Wide voltage range 3.0V to 5.5V
- High speed performance
  - 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
  - 12 mA Active current at 3.0V
  - 35 mA Active current at 5.5V
  - 100 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC package
  - 28-pin SOIC package
  - 28-pin TSOP package
  - 28-pin VSOP package
  - Tape and reel
- Available for the following temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

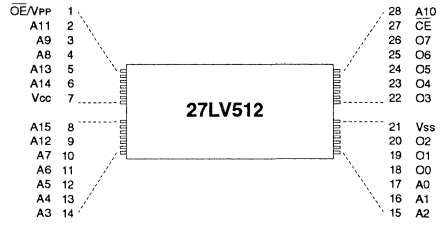
DESCRIPTION

The Microchip Technology Inc. 27LV512 is a low-voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 64K x 8 (64K-Byte) non-volatile memory product. The 27LV512 consumes only 12 mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low-voltage applications where conventional 5.0 volt only EPROMs can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0 volts. This device allows systems designers the ability to use low voltage non-volatile memory with today's low-voltage microprocessors and peripherals in battery powered applications.

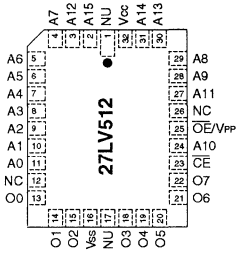
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPE

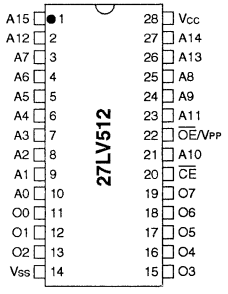
TSOP



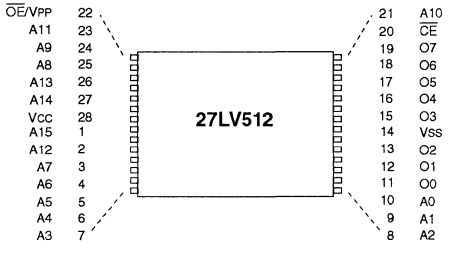
PLCC/LCC



DIP/SOIC



VSOP



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V

Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V

Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/Programming Voltage
O0 - O7	Data Output
VCC	+3.0V To +5.5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = 3.0V to 5.5V unless otherwise specified
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I	TTL input TTL input	ICC1 ICC2	— —	35@5.0V 12@3.0V 45@5.0V 12@3.0V	mA mA mA mA	VCC = 5.5V f = 1 MHz; $\overline{OE}$/VPP = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	C I all	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS	— — —	1@3.0V 2@3.0V 100@3.0V	mA mA µA	 $\overline{CE}$ = VCC ± 0.2V

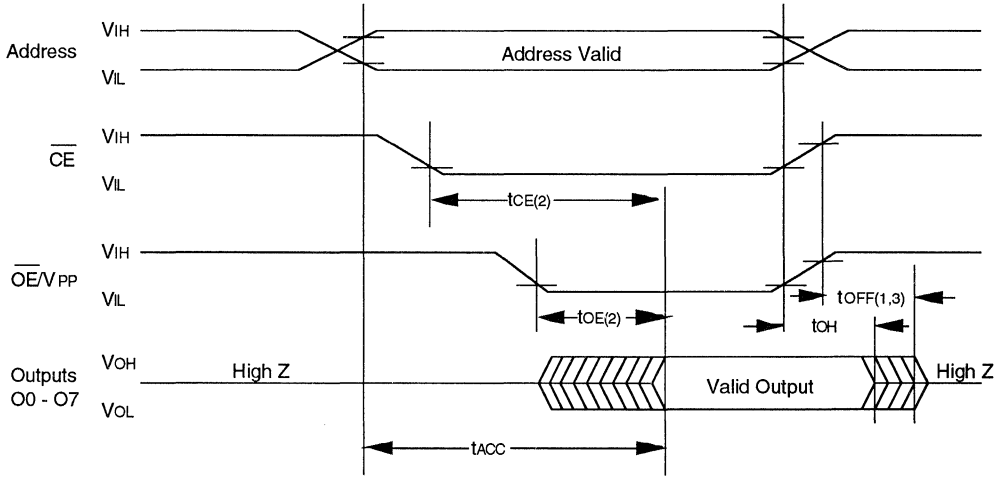
* Parts: C=Commercial Temperature Range; I=Industrial Temperature Range

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

	AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V and V_{OL} = 0.8V Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C								
Parameter	**Sym**	**27LV512-20**		**27LV512-25**		**27LV512-30**		**Units**	**Conditions**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**		
Address to Output Delay	t_{ACC}	—	200	—	250	—	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	200	—	250	—	300	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	90	—	100	—	125	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

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TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C VCC = 6.5V ± 0.25V, $\overline{OE}$/VPP = VH = 13.0V ± 0.25V						
Parameter	**Status**	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions (See Note 1)**
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4 —	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
VCC Current, program & verify	—	ICC2	—	35	mA	
$\overline{OE}$/VPP Current, program	—	IPP2	—	25	mA	$\overline{CE}$ = VIL
A9 Product Identification	—	VID	11.5	12.5	V	

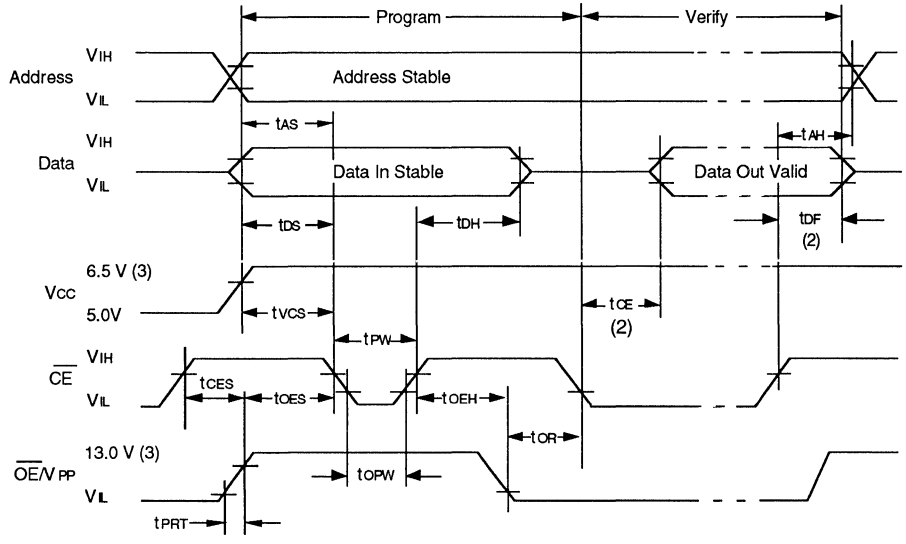
Note 1: VCC must be applied simultaneously or before VPP voltage on $\overline{OE}$/VPP and removed simultaneously or after the VPP voltage on $\overline{OE}$/VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V Ambient Temperature: Tamb=25°C ± 5°C VCC = 6.5V ± 0.25V, $\overline{OE}$/VPP = VH = 13.0V ± 0.25 V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
$\overline{OE}$ Hold Time	tOEH	2	—	µs	
$\overline{OE}$ Recovery Time	tOR	2	—	µs	
$\overline{OE}$/VPP Rise Time During Programming	tPRT	50	—	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express programming algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A9	O0 - O7
Read	V_{IL}	V_{IL}	X	D_{OUT}
Program	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	X	High Z
Output Disable	V_{IL}	V_{IH}	X	High Z
Identity	V_{IL}	V_{IL}	V_H	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}/V_{PP}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}/V_{PP}$.

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified.

1.4 Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in microprocessor based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when:

- the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

1.5 Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

1.6 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

1.7 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

1.8 Identity Mode

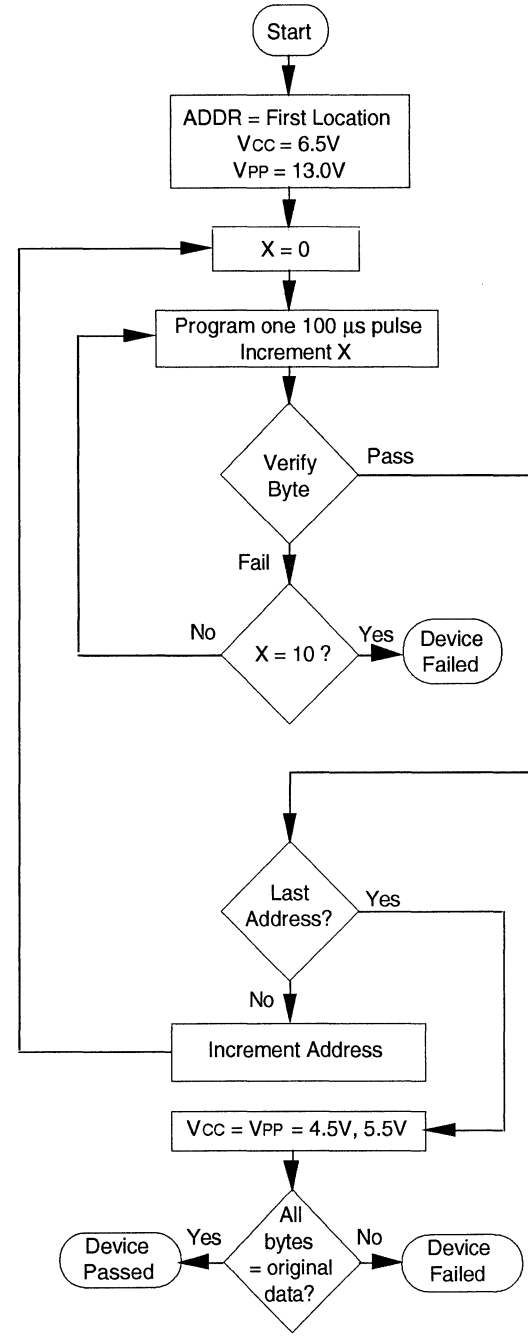
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	1	1	0	1	0D

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM

Conditions:
T_{amb} = 25°C ±5°C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



7

27LV512 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27LV512 - 25 I /P

Package:	L	Plastic Leaded Chip Carrier
	P	Plastic DIP
	SO	Plastic SOIC
	J	Ceramic DIP
	K	Ceramic Leaded Chip Carrier
	TS	Thin Small Outline Package(TSOP) 8x20mm
	VS	Very Small Outline Package(VSOP) 8x13.4mm
Temperature Range:	-	0°C to +70°C
	I	–40°C to +85°C
Access Time:	20	200 ns
	25	250 ns
	30	300 ns
Device:	27LV512	512K (64K x 8) Low-Voltage CMOS EPROM

37LV36/65/128

36K, 64K and 128K Serial EPROM Family

FEATURES

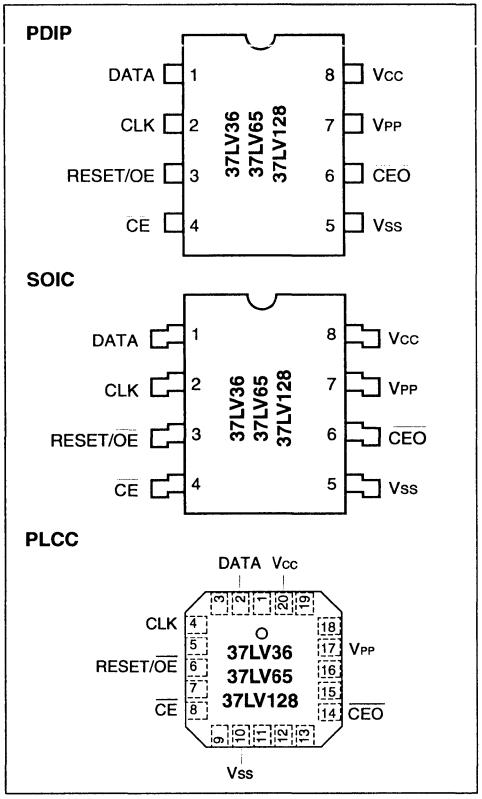
- Operationally equivalent to Xilinx® XC1700 family
- Wide voltage range 3.0 V to 6.0 V
- Maximum read current 10 mA at 5.0 V
- Standby current 100 µA typical
- Industry standard Synchronous Serial Interface/ 1 bit per rising edge of clock
- Full Static Operation
- Sequential Read/Program
- Cascadable Output Enable
- 10 MHz Maximum Clock Rate @ 5.0 Vdc
- Programmable Polarity on Hardware Reset
- Programming with industry standard EPROM programmers
- Electrostatic discharge protection > 4,000 volts
- 8-pin PDIP/SOIC and 20-pin PLCC packages
- Temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

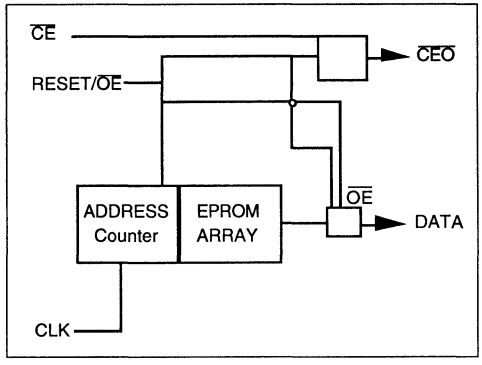
The Microchip Technology Inc. 37LV36/65/128 is a family of Serial OTP EPROM devices organized internally in a x32 configuration. The family also features a cascadable option for increased memory storage where needed. The 37LV36/65/128 is suitable for many applications in which look-up table information storage is desirable and provides full static operation in the 3.0V to 6.0V Vcc range. The devices also support the industry standard serial interface to the popular RAM-based Field Programmable Gate Arrays (FPGA). Advanced CMOS technology makes this an ideal bootstrap solution for today's high speed SRAM-based FPGAs. The 37LV36/65/128 family is available in the standard 8-pin plastic DIP, 8-pin SOIC and 20-pin PLCC packages.

Device	Bits	Programming Word
37LV36	36,288	1134 x 32
37LV65	65,536	2048 x 32
37LV128	131,072	4096 x 32

PACKAGE TYPE



BLOCK DIAGRAM



Xilinx is a registered trademark of Xilinx Corporation.

7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS ..... -0.6V to +0.6V

VPP voltage w.r.t. VSS during programming ..... -0.6V to +14.0V

Output voltage w.r.t. VSS ..... -0.6V to VCC +0.6V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

Soldering temperature of leads (10 sec.) ..... +300°C

ESD protection on all pins ..... ≥ 4 kV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function	8	20
DATA	Data I/O	1	2
CLK	Clock Input	2	4
RESET/$\overline{OE}$	Reset Input and Output Enable	3	6
$\overline{CE}$	Chip Enable Input	4	8
VSS	Ground	5	10
$\overline{CEO}$	Chip Enable Output	6	14
VPP	Programming Voltage Supply	7	17
VCC	+3.0V to 6.0V Power Supply	8	20
Not Labeled	Not utilized, not connected		

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +3.0 to 6.0V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Units	Conditions
DATA, $\overline{CE}$, $\overline{CEO}$ and Reset pins:					
High level input voltage	VIH	2.0	VCC	V	
Low level input voltage	VIL	-0.3	0.8	V	
High level output voltage	VOH1	3.86		V	IOH = -4 mA VCC ≥ 4.5V
	VOH2	2.4			IOH = -4 mA VCC ≥ 3.0V
Low level output voltage	VOL	—	.32	V	IOL = 4.0 mA
Input Leakage	ILI	-10	10	µA	VIN = .1V to VCC
Output Leakage	ILO	-10	10	µA	VOUT = .1V to VCC
Input Capacitance (all inputs/outputs)	CINT	—	6	pF	VCC = 5.0V (Note 1) Tamb = 25°C; FCLK = 1 MHz
Operating Current	ICC Read	—	10	mA	VCC = 6.0V, CLK = 10 MHz
		—	2	mA	VCC = 3.6V, CLK = 2.5 MHz Outputs open
Standby Current	ICCS	—	100	µA	VCC = 6.0V, CE = 5.8V
			50	µA	VCC = 3.6V, CE = 3.4V

Note 1: This parameter is initially characterized and not 100% tested.

2.0 DATA

2.1 Data I/O

Three-state DATA output for reading and input during programming.

3.0 CLK

3.1 Clock Input

Used to increment the internal address and bit counters for reading and programming.

4.0 RESET/$\overline{OE}$

4.1 Reset Input and Output Enable

A LOW level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A HIGH level on RESET/$\overline{OE}$ resets both the address and bit counters. In the 37LVXXX, the logic polarity of this input is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. This document describes the pin as RESET/$\overline{OE}$ although the opposite polarity is also possible. This option is defined and set at device program time.

5.0 $\overline{CE}$

5.1 Chip Enable Input

$\overline{CE}$ is used for device selection. A LOW level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A HIGH level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode.

6.0 $\overline{CEO}$

6.1 Chip Enable Output

This signal is asserted LOW on the clock cycle following the last bit read from the memory. It will stay LOW as long as $\overline{CE}$ and $\overline{OE}$ are both LOW. It will then follow $\overline{CE}$ until $\overline{OE}$ goes HIGH. Thereafter, $\overline{CEO}$ will stay HIGH until the entire EPROM is read again. This pin also used to sense the status of RESET polarity when Programming Mode is entered.

7.0 VPP

7.1 Programming Voltage Supply

Used to enter programming mode (+13 volts) and to program the memory (+13 volts). Must be connected directly to Vcc for normal Read operation. No overshoot above +14 volts is permitted.

8.0 CASCADING SERIAL EPROMS

Cascading Serial EPROMs provide additional memory for multiple FPGAs configured as a daisy-chain, or for future applications requiring larger configuration memories.

When the last bit from the first Serial EPROM is read, the next clock signal to the Serial EPROM asserts its $\overline{CEO}$ output LOW and disables its DATA line. The second Serial EPROM recognizes the LOW level on its $\overline{CE}$ input and enables its DATA output.

When configuration is complete, the address counters of all cascaded Serial EPROMs are reset if RESET goes LOW forcing the RESET/$\overline{OE}$ on each Serial EPROM to go HIGH. If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground.

Additional logic may be required if cascaded memories are so large that the rippled chip enable is not fast enough to activate successive Serial EPROMs.

9.0 STANDBY MODE

The 37LVXXX enters a low-power Standby Mode whenever $\overline{CE}$ is HIGH. In Standby Mode, the Serial EPROM consumes less than 100 µA of current. The output will remain in a high-impedance state regardless of the state of the $\overline{OE}$ input.

10.0 PROGRAMMING MODE

Programming Mode is entered by holding V_{PP} HIGH (+13 volts) for two clock edges and then holding V_{PP} = V_{DD} for one clock edge. Programming mode is exited by driving a LOW on both $\overline{CE}$ and $\overline{OE}$ and then removing power from the device. Figures 4 through 7 show the programming algorithm.

11.0 37LVXXX RESET POLARITY

The 37LVXXX lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{OE}$/RESET. Any third-party commercial programmer should prompt the user for the desired reset polarity.

The programming of the overflow word should be handled transparently by the EPROM programmer; it is mentioned here as supplemental information only.

The polarity is programmed into the first overflow word location, maximum address+1. 00000000 in these locations makes the reset active LOW, FFFFFFFF in these locations makes the reset active HIGH. The default condition is RESET active HIGH.

7

FIGURE 11-1: READ CHARACTERISTICS TIMING

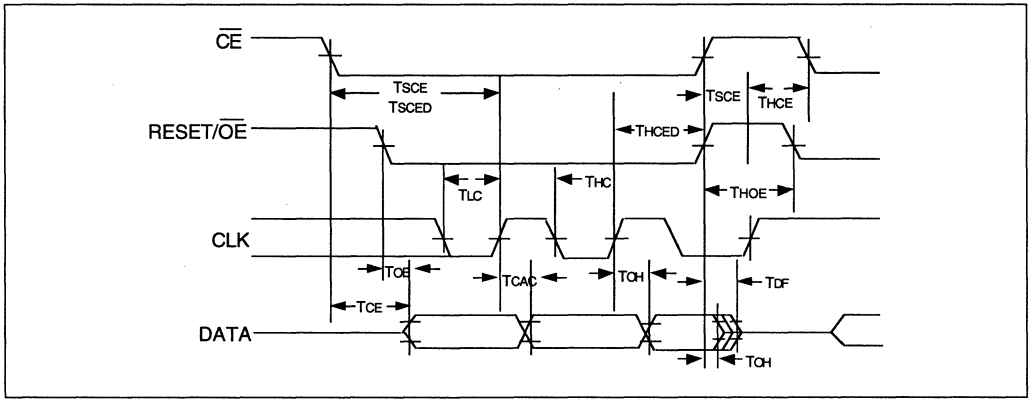


TABLE 11-1: READ CHARACTERISTICS

		AC Testing Waveform: V_{IL} = 0.2V; V_{IH} = 2.8V AC Test Load: 50 pF V_{OL} = V_{OL_MAX}; V_{OH} = V_{OH_MIN}					
Symbol	**Parameter**	**Limits 3.0V ≤ Vcc ≤ 6.0V**		**Limits 4.5V ≤ Vcc ≤ 6.0V**		**Units**	**Conditions**
		Min.	**Max.**	**Min.**	**Max.**		
T_{OE}	$\overline{OE}$ to Data Delay	—	45	—	45	ns	
T_{CE}	$\overline{CE}$ to Data Delay	—	60	—	50	ns	
T_{CAC}	CLK to Data Delay	—	200	—	60	ns	
T_{OH}	Data Hold from $\overline{CE}$, $\overline{OE}$ or CLK	0	—	0	—	ns	
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay	—	50	—	50	ns	Notes 1, 2
T_{LC}	CLK Low Time	100	—	25	—	ns	
T_{HC}	CLK High Time	100	—	25	—	ns	
T_{SCE}	$\overline{CE}$ Set up Time to CLK (to guarantee proper counting)	40	—	25	—	ns	Note 1
T_{SCED}	$\overline{CE}$ setup time to CLK (to guarantee proper DATA read)	100	—	80	—	ns	
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0	—	0	—	ns	Note 1
T_{HCED}	$\overline{CE}$ hold time to CLK (to guarantee proper DATA read)	50	—	0	—	ns	
T_{HCE}	$\overline{OE}$ High Time (Guarantees counters are Reset)	100		20	—	ns	
CLK max	Clock Frequency	—	2.5	—	10	MHz	

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: Float delays are measured with output pulled through 1kΩ to V_{LOAD} = Vcc/2.

FIGURE 11-2: READ CHARACTERISTICS AT END OF ARRAY TIMING

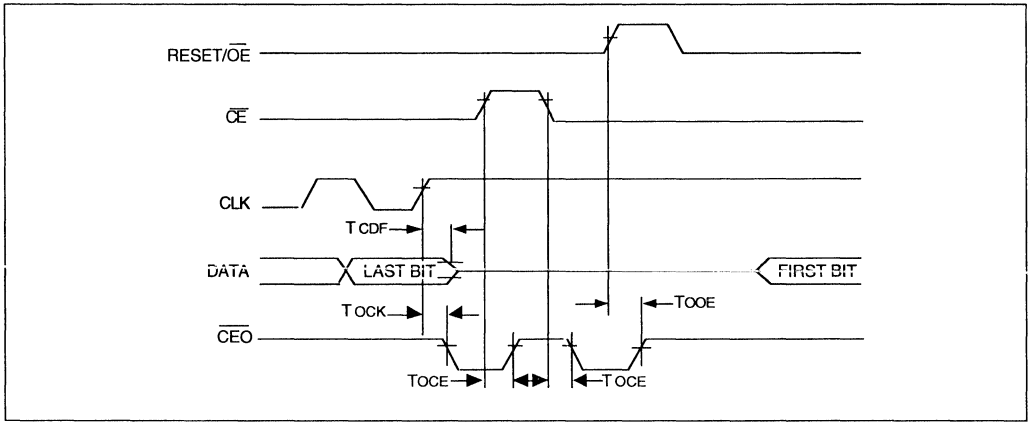


TABLE 11-2: READ CHARACTERISTICS AT END OF ARRAY

		AC Testing Waveform: V_{IL} = 0.2V; V_{IH} = 2.8V AC Test Load: 50 pF V_{OL} = V_{OL}_MAX; V_{OH} = V_{OH}_MIN					
Symbol	**Parameter**	**Limits 3.0V ≤ Vcc ≤ 6.0V**		**Limits 4.5V ≤ Vcc ≤ 6.0V**		**Units**	**Conditions**
		Min.	**Max.**	**Min.**	**Max.**		
TCDF	CLK to Data Float Delay	—	50	—	50	ns	Notes 1, 2
TOCK	CLK to $\overline{CEO}$ Delay	—	65	—	40	ns	
TOCE	$\overline{CE}$ to $\overline{CEO}$ Delay	—	45	—	40	ns	
TOOE	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay	—	45	—	40	ns	

Note 1: This parameter is periodically sampled and not 100% tested.
Note 2: Float delays are measured with output pulled through 1kΩ to V_{LOAD} = Vcc/2.

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TABLE 11-3: PIN ASSIGNMENTS IN THE PROGRAMMING MODE

DIP/SOIC Pin	PLCC Pin	Name	I/O	Description
1	2	DATA	I/O	The rising edge of the clock shifts a data word in or out of the EPROM one bit at a time.
2	4	CLK	I	Clock Input. Used to increment the internal address/word counter for reading and programming operation.
3	6	RESET/$\overline{OE}$	I	The rising edge of CLK shifts a data word into the EPROM when $\overline{CE}$ and $\overline{OE}$ are HIGH; it shifts a data word out of the EPROM when $\overline{CE}$ is LOW and $\overline{OE}$ is HIGH. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held HIGH and $\overline{OE}$ is held LOW. Note 1: Any modified polarity of the RESET/$\overline{OE}$ pin is ignored in the programming mode.
4	8	$\overline{CE}$	I	The rising edge of CLK shifts a data word into the EPROM when $\overline{CE}$ and $\overline{OE}$ are HIGH; it shifts a data word out of the EPROM when $\overline{CE}$ is LOW and $\overline{OE}$ is HIGH. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held HIGH and $\overline{OE}$ is held LOW.
5	10	VSS		Ground pin.
6	14	$\overline{CEO}$	O	The polarity of the RESET/$\overline{OE}$ pin can be read by sensing the $\overline{CEO}$ pin. Note 1: The polarity of the RESET/$\overline{OE}$ pin is ignored while in the Programming Mode. In final verification, this pin must be monitored to go LOW one clock cycle after the last data bit has been read.
7	17	VPP		Programming Voltage Supply. Programming Mode is entered by holding $\overline{CE}$ and $\overline{OE}$ HIGH and VPP at VPP1 for two rising clock edges and then lowering VPP to VPP2 for one more rising clock edge. A word is programmed by strobing the device with VPP for the duration TPGM. VPP must be tied to VCC for normal read operation.
8	20	VCC		+5 V power supply input.

TABLE 11-4: DC PROGRAMMING SPECIFICATIONS

Symbol	Parameter Ambient Temperature: Tamb = 25°C ±5°C	Limits		Units
		Min.	Max.	
VCCP	Supply voltage during programming	5.0	6.0	V
VIL	Low-level input voltage	0.0	0.5	V
VIH	High-level input voltage	2.4	VCC	V
VOL	Low-level output voltage	—	0.4	V
VOH	High-level output voltage	3.7	—	V
VPP1	Programming voltage*	12.5	13.5	V
VPP2	Programming Mode access voltage	VCCP	VCCP+1	V
IPPP	Supply current in Programming Mode	—	100	mA
IL	Input or output leakage current	-10	10	µA
VCCL	First pass Low-level supply voltage for final verification	2.8	3.0	V
VCCH	Second pass High-level supply voltage for final verification	7.0	7.2	V

* No overshoot is permitted on this signal. VPP must not be allowed to exceed 14 volts.

TABLE 11-5: AC PROGRAMMING SPECIFICATIONS (SEE NOTE 2)

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
TRPP	10% to 90% Rise Time of VPP	1		µs	Note 1
TFPP	90% to 10% Fall Time of VPP	1		µs	Note 1
TPGM	VPP Programming Pulse Width	.50	1.05	ms	
TSVC	VPP Setup to CLK for Entering Programming Mode	100		ns	Note 1
TSVCE	$\overline{CE}$ Setup to CLK for Entering Programming Mode	100		ns	Note 1
TSVOE	$\overline{OE}$ Setup to CLK for Entering Programming Mode	100		ns	Note 1
THVC	VPP Hold from CLK for Entering Programming Mode	300		ns	Note 1
TSDP	Data Setup to CLK for Programming	50		ns	
THDP	Data Hold from CLK for Programming	0		ns	
TLCE	$\overline{CE}$ Low time to clear data latches	100		ns	
TSCC	$\overline{CE}$ Setup to CLK for Programming/Verifying	100		ns	
TSIC	$\overline{OE}$ Setup to CLK for Incrementing Address Counter	100		ns	
THIC	$\overline{OE}$ Hold from CLK for Incrementing Address Counter	0		ns	
THOV	$\overline{OE}$ Hold from VPP	200		ns	Note 1
TPCAC	CLK to Data Valid		400	ns	
TPOH	Data Hold from CLK	0		ns	
TPCE	$\overline{CE}$ Low to Data Valid		250	ns	

Note 1: This parameter is periodically sampled and not 100% tested.

Note 2: While in Programming Mode, $\overline{CE}$ should only be changed while $\overline{OE}$ is HIGH and has been HIGH for 200 ns and $\overline{OE}$ should only be changed while $\overline{CE}$ is HIGH and has been HIGH for 200 ns.

FIGURE 11-3: ENTER AND EXIT PROGRAMMING MODES

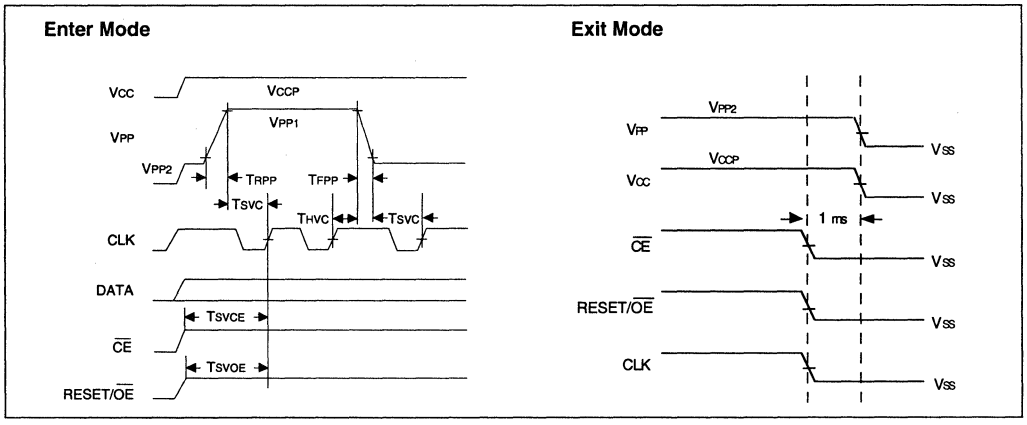


FIGURE 11-4: PROGRAMMING CYCLE OVERVIEW (NO VERIFY UNTIL ENTIRE ARRAY IS PROGRAMMED.)

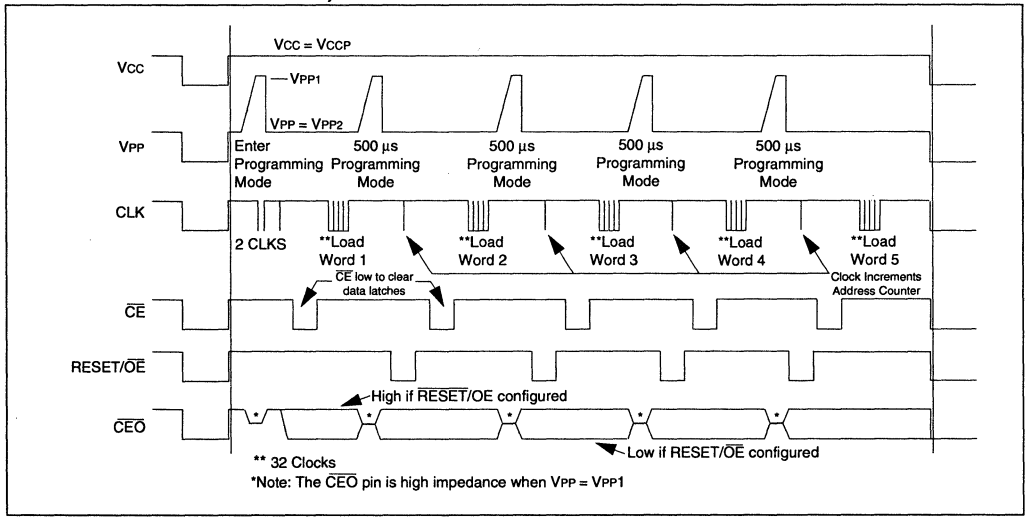


FIGURE 11-5: DETAILS OF PROGRAM CYCLE

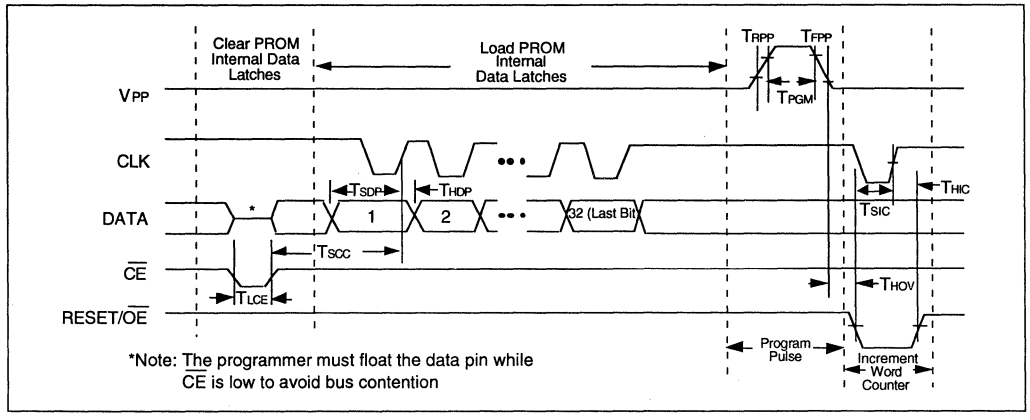


FIGURE 11-6: READ MANUFACTURER AND DEVICE ID OVERVIEW

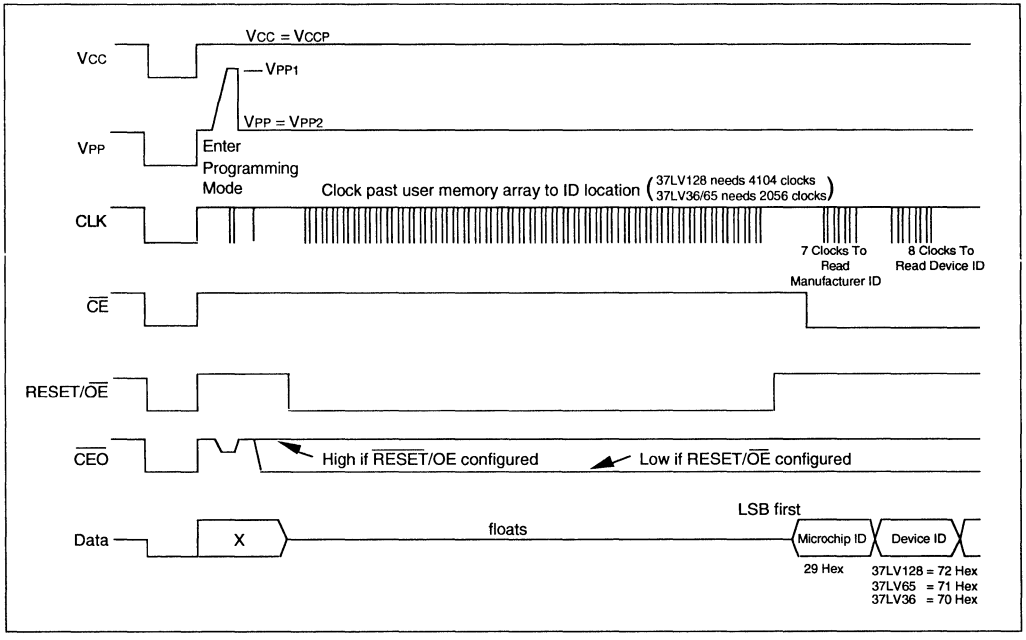


FIGURE 11-7: DETAILS OF READ MANUFACTURER AND DEVICE ID

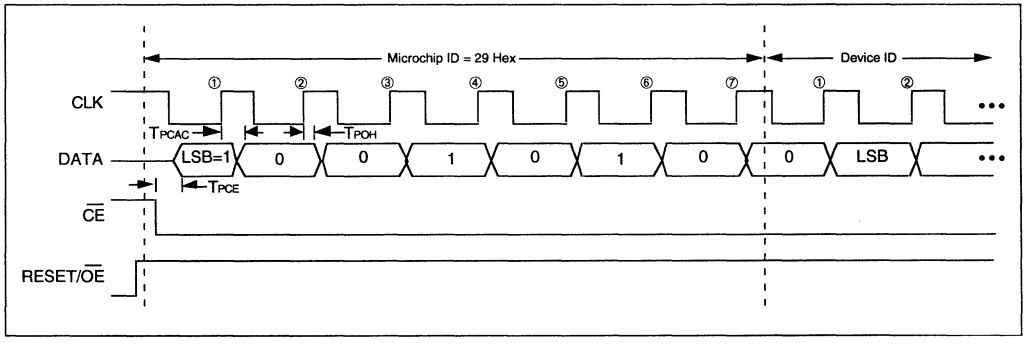
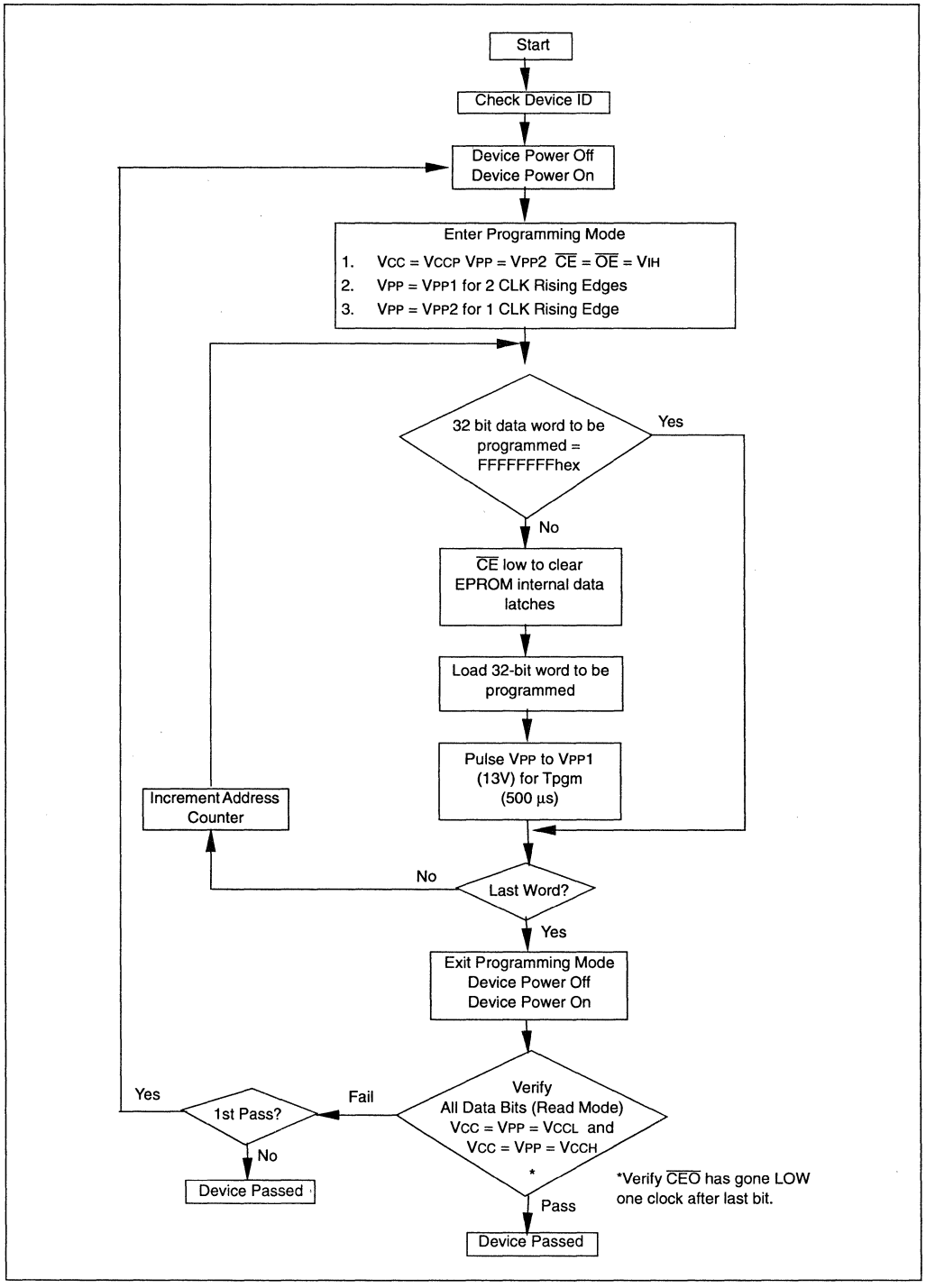


FIGURE 11-8: 37LVXXX PROGRAMMING SPECIFICATIONS



NOTES

37LV36/65/128 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

37LVXXX - X X X

Package:		P	Plastic DIP, 8 lead
		SN	Plastic SOIC (150 mil Body), 8 lead
		L	Plastic Leaded Chip Carrier (PLCC), 20 lead
Temperature Range:		Blank	0°C to +70°C
		I	–40°C to +85°C
Shipping:		Blank	Tube
		T	Tape and Reel
Device:		37LV128	128K Serial EPROM
		37LV65	64K Serial EPROM
		37LV36	36K Serial EPROM

EPROM Programming Guide

All Microchip EPROMs should be programmed using the Express algorithm (shown on reverse side). Other algorithms can cause high programming fallout and even retention failures due to undue stress on the chips. This list will be updated as information becomes available. Programmer models and revisions shown are subject to change by the manufacturers at any time.

Manufacturer	Model	Software Rev	Status
DATA I/O	S1000	24 or 25	Verified Express
DATA I/O	29B	24	Verified Express
DATA I/O	288	1.0	Vendor specifies Express
DATA I/O	2900	1.1, 1.2, 1.7	Vendor specifies Express
DATA I/O	3900	1.0, 1.4	Vendor specifies Express
DATA I/O	Autosite	1.0, 1.5	Vendor specifies Express
DATA I/O	Unisite	3.0, 3.1, 3.2	Vendor specifies Express
STAG	PP42	8.0	Verified close to Express, but user must manually select double-voltage verify
STAG	PP39		Same
ELAN	5000/932 Turbo	6.02V1	Vendor specifies Express
ELAN	5000/932	5.05V1	Vendor specifies Express
EPRO	Model 124		User-programmable to Express
LOGIC DEVICES	AllPro 88, 40	2.2	Express AND Low Voltage Support No Express support for Windows version (Exar)
LOGIC DEVICES	GangPro 8+	1.1	Vendor specifies Express on latest release
LOGIC DEVICES	GangPro S		Fast, Rapid only
LOGIC DEVICES	GangPro S,	1.0	Vendor specifies Express on latest release
LOGIC DEVICES	Husky		Fast, Rapid only
BYTEK	Multitrk-4000		Vendor specifies Express on latest release
BP MICROSYSTEMS	1148,1200	3.06	Vendor specifies Express on latest release.

ADAPTERS

PLCC-to-DIP

Emulation Technology
32-28-01-P600

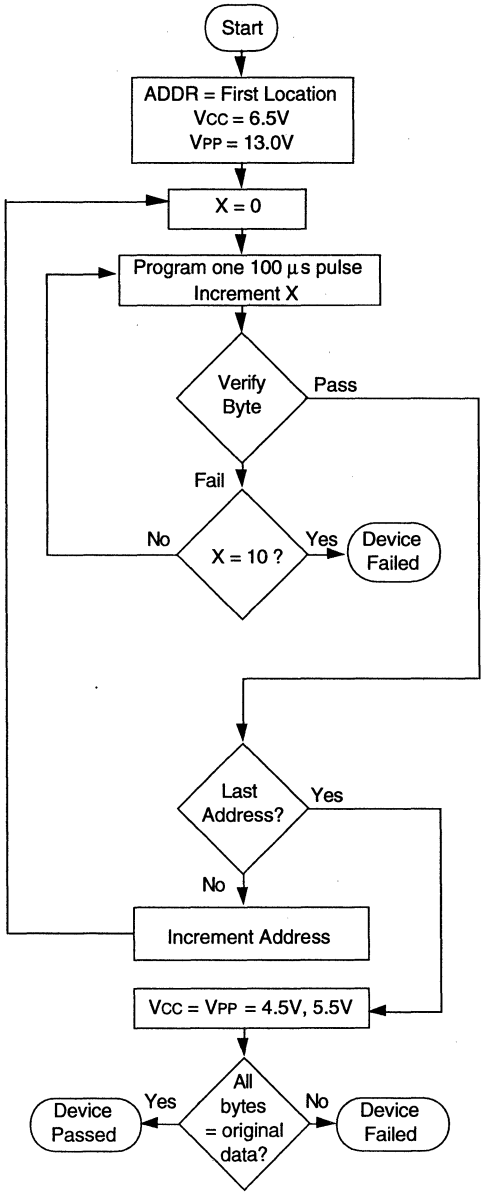
TSOP-to-DIP

Emulation Technology
AS-32-28-02TS-6ENP-GANG-S

Emulation Technology
Phone 408-982-0660, FAX 408-982-0664

EXPRESS ALGORITHM

Conditions:
T_{amb} = 25°C ±5°C
V_{CC} = 6.5 ±0.25V
V_{PP} = 13.0 ±0.25V



SECTION 8
DEVELOPMENT SYSTEMS

Microchip BBS	Microchip Bulletin Board Service	8-1
Total Endurance™	Microchip Serial EEPROM Endurance Model	8-3
Designer's Kit	Microchip Serial EEPROM Designer's Kit	8-5

MICROCHIP BBS

Microchip Bulletin Board Service

Get current information and help on Microchip's Bulletin Board Service (BBS)! Microchip wants to provide you with the most responsive service possible. To accomplish this, the systems team monitors the BBS, posting the latest component data and software tool updates, providing technical help and embedded systems insights, and discussing how Microchip products provide project solutions. Extend your technical groups staff with microcontroller and memory experts through Microchip's BBS communication channel.

SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information And Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits. The Hot Line Numbers are: 1-800-755-2345 for U.S. and most of Canada, and 1-602-786-7302 for the rest of the world.

These phone numbers are also listed on the "Important Information" sheet that is shipped with all development systems. The hot line message is updated whenever a new software version is added to the Microchip BBS, or when a new upgrade kit becomes available.

CONNECTING TO MICROCHIP

Connect worldwide to the Microchip BBS using the CompuServe® communications network. In most cases, a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore, **you do not need CompuServe membership to join Microchip's BBS.**

There is **no charge** for connecting to the BBS, except for a toll charge to the CompuServe access number, where applicable. You do not need to be a CompuServe member to take advantage of this connection (you never actually log in to CompuServe).

The procedure to connect will vary slightly from country to country. Please check with your local CompuServe agent for details if you have a problem. CompuServe service allow multiple users at baud rates up to 14400 bps.

The following connect procedure applies in most locations.

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
2. Dial your local CompuServe access number.
3. Depress **<Enter↵>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.
4. Type +, depress **<Enter↵>** and `Host Name:` will appear.
5. Type **MCHIPBBS**, depress **<Enter↵>** and you will be connected to the Microchip BBS.

In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600-14400 baud connection. After the system responds with `Host Name:`, type **NETWORK**, depress **<Enter↵>** and follow CompuServe's directions.

For voice information (or calling from overseas), you may call (614) 457-1550 for your local CompuServe number.

USING THE BULLETIN BOARD

The bulletin board is a multifaceted tool. It can provide you with information on a number of different topics.

- Special Interest Groups
- Files
- Mail
- Bug Lists

Special Interest Groups

Special Interest Groups, or SIGs as they are commonly referred to, provide you with the opportunity to discuss issues and topics of interest with others that share your interest or questions. SIGs may provide you with information not available by any other method because of the broad background of the PIC16/17 user community.

There are SIGs for most Microchip systems, including:

- MPASM
- PICMASTER®
- PRO MATE™
- Utilities
- Bugs
- PICSTART®
- MPSIM
- TRUE GAUGE™
- *fuzzy*TECH®-MP
- ASSP
- MTE1122

These groups are monitored by the Microchip staff.

8

Files

Microchip regularly uses the Microchip BBS to distribute technical information, application notes, source code, errata sheets, bug reports, and interim patches for Microchip systems software products. Users can contribute files for distribution on the BBS. For each SIG, a moderator monitors, scans, and approves or disapproves files submitted to the SIG. No executable files are accepted from the user community in general to limit the spread of computer viruses.

Mail

The BBS can be used to distribute mail to other users of the service. This is one way to get answers to your questions and problems from the Microchip staff, as well as keeping in touch with fellow Microchip users worldwide.

Consider mailing the moderator of your SIG, or the SYSOP, if you have ideas or questions about Microchip products, or the operation of the BBS.

Note:	The SIGs provide you with the opportunity to discuss issues and exchange ideas. Technical support and urgent questions should be referred to your local distributor, sales representative or FAE. They are your first level of support.

Software Releases

Software products released by Microchip are referred to by version numbers. Version numbers use the form:

```
xx.yy.zz <status>
```

Where `xx` is the major release number, `yy` is the minor number, and `zz` is the intermediate number. The `status` field displays one of the following categories:

- Alpha
- Intermediate
- Beta
- Released

Production releases are numbered with major, and minor version numbers like:

```
3.04 Released
```

Alpha, Beta and Intermediate releases are numbered with the major, minor and intermediate numbers:

```
3.04.01 Alpha
```

Alpha Release

Alpha designated software is engineering software that has not been submitted to any quality assurance testing. In general, this grade of software is intended for software development team access only, but may be sent to selected individuals for conceptual evaluation.

Intermediate Release

Intermediate released software represents changes to a released software system and is designated as such by adding an intermediate number to the version number. Intermediate changes are represented by:

- Bug Fixes
- Special Releases
- Feature Experiments

Intermediate released software does not represent our most tested and stable software. Typically, it will not have been subject to a thorough and rigorous test suite, unlike production released versions. Therefore, users should use these versions with care, and only in cases where the features provided by an intermediate release are required.

Intermediate releases are primarily available through the BBS.

Beta Release

Preproduction software is designated as Beta. Beta software is sent to Applications Engineers and Consultants, FAEs, and select customers. The Beta Test period is limited to a few weeks. Software that passes Beta testing without having significant flaws, will be production released. Flawed software will be evaluated, repaired, and updated with a new revision number for a subsequent Beta trial.

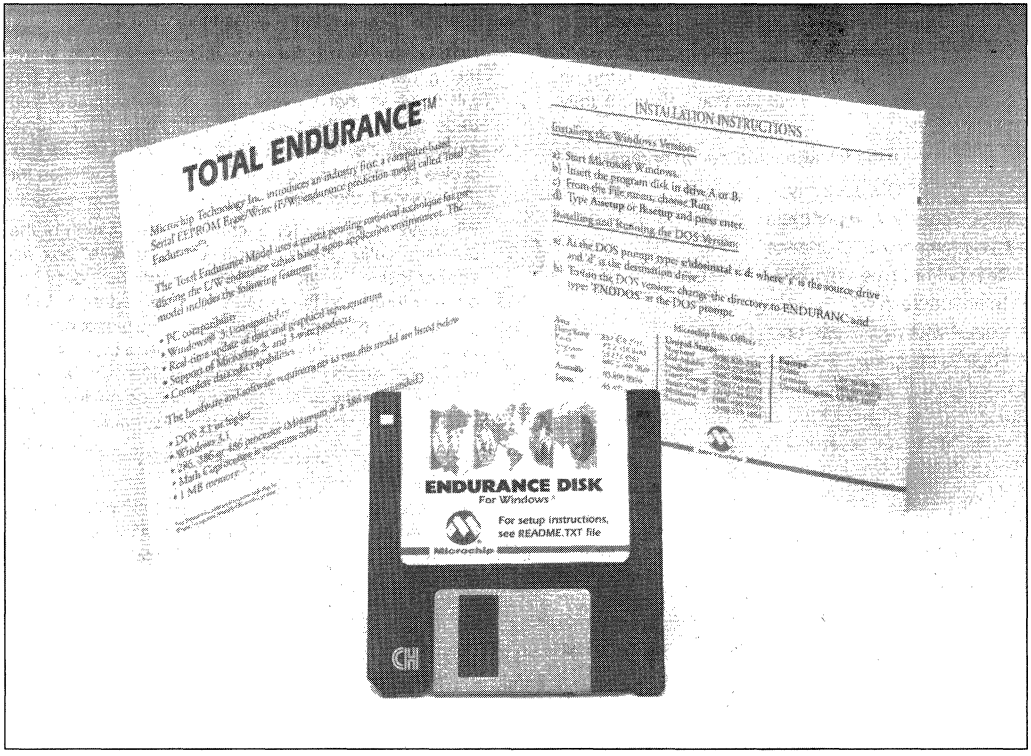
Production Release

Production released software is software shipped with tool products. Example products are PRO MATE, PICSTART®, and PICMASTER. The Major number is advanced when significant feature enhancements are made to the product. The minor version number is advanced for maintenance fixes and minor enhancements. Production released software represents Microchip's most stable and thoroughly tested software.

There will always be a period of time when the Production Released software is not reflected by products being shipped until stocks are rotated. You should always check the BBS for the current production release.

MICROCHIP TOTAL ENDURANCE™

Microchip Serial EEPROM Endurance Model



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FEATURES

- IBM® PC compatibility
- Windows™ 3.1 or DOS 3.1 compatibility
- Automatic or manual recalculation
- Real-time update of data
- Full-screen or windowed graphical view
- Hypertext on-screen help
- Key or slide-bar entry of parameters
- On-screen editing of parameters
- Single-click copy of plot to clipboard
- Numeric export to delimited text file
- On-disk Endurance Tutorial

SYSTEM REQUIREMENTS

- DOS 3.1 or higher
- Windows 3.1
- 1MB memory
- 386 or 486 processor recommended
- Math coprocessor recommended

DEVICE SUPPORT

- Microchip 2-wire 24CXX/24LCXXB/24AAXX/ 85CXX
- Microchip 3-wire 93CXX/93LCXX/93AAXX Series
- Microchip 4-wire 59C11

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Windows is a trademark of Microsoft Corp.

Total Endurance™

DESCRIPTION

Microchip's revolutionary Total Endurance Model provides electronic systems designers with unprecedented visibility into Serial EEPROM-based applications. This advanced software model (with a very friendly user interface) eliminates time and guesswork from Serial EEPROM-based designs by accurately predicting the device's performance and reliability within a user-defined application environment. Design trade-off analysis which formerly consumed days or weeks can now be performed in minutes...with a level of accuracy that delivers a truly robust design.

Users may input the following application parameters:

- Serial EEPROM device type
- Bytes to be written per cycle
- Cycling mode - byte or page
- Data pattern type - random or worst-case
- Temperature in °C
- Erase/Write cycles per day
- Application lifetime or target PPM level

The model will respond with FIT rate, PPM level, application life and a plot of the PPM level vs. number of cycles. The model is available in both DOS and Windows versions.

BACKGROUND

Microchip's research into the Erase/Write endurance of Serial EEPROMs has resulted in the conclusion that endurance depends upon three primary effects: the physical properties of the EEPROM cell, the internal error-correction technology employed, and the application environment. EEPROM endurance specified as a "typical" value in device data sheets must therefore be evaluated on a case-by-case basis, taking into account the manner in which the device will be used in the application. The Microchip Total Endurance software applies the user-defined application parameters to a complex mathematical model in order to emulate the EEPROM's performance and reliability in the system.

USING THE MODEL

The user has simply to choose a Microchip Serial EEPROM device from the device-list menu and begin entering the application parameters. The entire process can take literally seconds to complete, and the model will output the PPM level and FIT rate of the device vs. the number of Erase/Write cycles. If the user has specified an application lifetime, the model will output PPM and FIT rates at that point in time. Alternately, the user may input a desired PPM level and the model will calculate the application lifetime which will result in that survival rate. The user may then trade-off any of the parameters (device type, voltage, application life, temperature, # of bytes per cycle, # of cycles per day etc.) to arrive at an optimal solution for the intended application.

Whenever a parameter is changed, calculation of the ppm/application life is automatic. An "update" box will appear inside the graph to indicate that new data has been entered and the graph should be redrawn. A single click in the "draw" box will redraw the plot of ppm vs. cycles; a click in the "Resize" box will take the plot to full-screen display for a closer view. The plot data can be saved to a file or the plot itself can be copied to the clipboard to be pasted into another application.

ACCURACY OF THE MODEL

The accuracy of the Microchip Total Endurance model has been verified against test data to within ten percent of the actual values. However, Microchip makes no warranty as to its accuracy or applicability of the information to any given application. It is intended to be used as a guide to aid designers of Serial EEPROM-based systems in performing trade-off analysis and developing robust and reliable designs.

Order Information:

Description	Part Number
Total Endurance Software Disk	SW242001

MICROCHIP

DESIGNER'S KIT

Microchip Serial EEPROM Designer's Kit

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FEATURES

- Includes everything necessary to begin developing Serial EEPROM-based applications
- Microchip *Total Endurance*™ software model
- Microchip *SEEVAL*™ evaluation and programming board
- Microchip *SEEVAL* software
- Microchip Serial EEPROM handbook
- Microchip Serial EEPROM sample pack
- RS-232 serial cable
- Power supply

SYSTEM REQUIREMENTS

- DOS 3.1 or higher
- Windows™ 3.1
- VGA monitor
- 386 or 486 processor recommended
- Math coprocessor recommended

DEVICE SUPPORT

- Microchip 2-wire 24CXX/24LCXXB/85CXX
- Microchip *Smart Serial*™ 24XX65
- Microchip 3-wire 93CXX/93LCXX series
- Microchip 4-wire 59C11

Total Endurance, SEEVAL and Smart Serial are trademarks of Microchip Technology Inc.
IBM PC is a registered trademark of IBM Corp.
Windows is a trademark of Microsoft Corp.

Designer's Kit

DESCRIPTION

Now designers of Serial EEPROM-based applications can enjoy the increased productivity, reduced time to market, and the ability to create a rock-solid design that only a well-thought-out development system can provide. Microchip's new Serial EEPROM Designer's Kit includes everything necessary to quickly develop a robust and reliable Serial EEPROM-based design and greatly reduce the time required for system integration and hardware/software debug.

The **Total Endurance software model** enables designers to quickly choose the best Serial EEPROM for the specific application and perform trade-off analysis with voltage, temperature, write cycle and other system parameters in order to achieve the desired Erase/Write endurance (specific ppm rate) or product lifetime. Total Endurance is the new standard of excellence in understanding and predicting the Erase/Write endurance of Serial EEPROMs. An on-line endurance tutorial is included, along with hypertext help files.

Microchip's **SEEVAL Serial EEPROM evaluation and programming system** will accept any Microchip Serial EEPROM in DIP package and enable the designer or system integrator to read, write, or erase any byte or the entire array. SEEVAL also provides the following advanced features to aid in system integration and debug:

- Program special user functions like *Smart Serial* configurations
- Hexadecimal display of array contents
- Pre-set or user-defined repeating patterns
- User-configurable functions like continuous read/write, programmable delay, etc.
- Upload/download files between the Serial EEPROM and disk

Another industry first, the **Microchip Serial EEPROM Handbook** provides a plethora of information crucial to the designers of Serial EEPROM-based systems. Along with data sheets on Microchip Serial EEPROMs, this resource provides application notes regarding Erase/Write endurance, interfacing with different protocols and many, many others. A cross-reference and selector guide are also included, plus article reprints and qualification reports on Microchip Serial EEPROMs.

USING SEEVAL AND TOTAL ENDURANCE

Both software packages can be loaded from Windows by choosing FILE RUN and entering SETUP.EXE from the Program Manager. The applications will install themselves; then a double mouse-click will start either application. The first step in either program is to select a device from the device list.

In Total Endurance, the user has simply to choose a Microchip Serial EEPROM device from the device-list menu and begin entering the application parameters. The entire process can take literally seconds to complete, and the model will output the PPM level and FIT rate of the device vs. the number of Erase/Write cycles. If the user has specified an application lifetime, the model will output PPM and FIT rates at that point in time. Alternately, the user may input a desired PPM level and the model will calculate the application lifetime which will result in that survival rate. The user may then trade-off any of the parameters (device type, voltage, application life, temperature, # of bytes per cycle, # of cycles per day etc.) to arrive at an optimal solution for the intended application.

Whenever a parameter is changed, calculation of the ppm/application life is automatic. An "update" box will appear inside the graph to indicate that new data has been entered and the graph should be redrawn. A single click in the "draw" box will redraw the plot of ppm vs. cycles; a click in the "Resize" box will take the plot to full-screen display for a closer view. The plot data can be saved to a file or the plot itself can be copied to the clipboard to be pasted into another application.

In **SEEVAL**, the user may choose to load a file from disk to program the Serial EEPROM, or read data from the EEPROM and save it to disk. The screen displays the contents of a software buffer. The buffer may be manipulated before programming data to the Serial EEPROM, or data can be written to the Serial EEPROM directly on-line. An area of memory can be highlighted (selected) and programmed with a predefined pattern or user-specified pattern. Alternately, the entire device can be programmed with any repeating pattern.

Both SEEVAL and Total Endurance allow the user to save any configuration as default. This configuration (device and application settings) will then automatically load at boot time.

Order Information:

Description	Part Number
SErial EEPROM Designer's Kit	DV243001

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MICROCHIP

PIC16/17

Shortform Catalog to PIC16/17 8-Bit Microcontrollers

The following shortform catalog section will provide an overview to Microchip Technology Inc.'s PIC16/17 8-bit, RISC-based microcontrollers and development systems. This includes: PIC16C5X base-line, PIC16CXX mid-range and PIC17CXX high-end performance product families with complementary emulator systems and development tools.

For detailed information on PIC16/17 microcontroller and development systems, please refer to the ***Microchip PIC16/17 8-Bit Microcontroller Data Book.*** (A copy can be obtained by calling your local Microchip sales office.)

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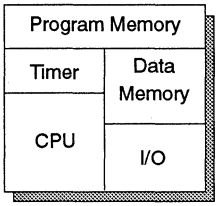
PIC16C5X 8-BIT MICROCONTROLLER FAMILY: BASE-LINE COST EFFECTIVENESS

For many consumer, automotive and commercial applications, the PIC16C5X family of CMOS microcontrollers offers the best combination of low-cost, low-power, small-footprint and speed operation with the versatile field programmable EPROM program memory. This advanced OTP technology provides the designer/manufacturer with a new level of cost savings and affordable versatility uncommon in today's microcontroller market.

- Low cost, Low power
- Small-footprint
- Versatile Field Programmable EPROM
- Most cost-effective OTP solution
- RISC-like Harvard architecture
- 33 12-bit wide instructions
- Highly efficient, easy-to-learn set of program instructions
- Single cycle instruction execution
- Single word instructions result in more compact software code
- Instruction execution rates as fast as 200 ns per instruction

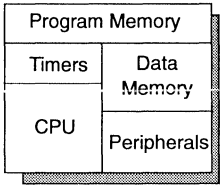
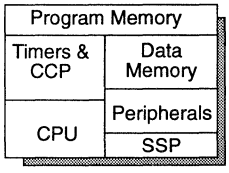
PIC16C5X development is supported by user-friendly, Windows™-based PICMASTER®-16D universal development platform and the low-cost PICSTART®-16B1. Software support includes assembler (MPASM), simulator (MPSIM), C Compiler and fuzzy logic development software (*fuzzy*TECH-MP®).

Part Number	Package	Features
PIC16C54	18-Lead	• 512 x 12 EPROM • 25 bytes general purpose RAM • 12 bidirectional I/O lines • RTCC timer/counter • Watchdog timer • Fuse selectable oscillator configurations: RC, XT, LP, HS for EPROM-based devices • DC through 20MHz clock • DC to 200ns instruction cycle • Wide operating voltage • Sleep Mode • Three temperature ranges (0°C to +70°C, -40°C to +85°C, and -40°C to +125°C) • Packaging available: 18-Lead PDIP, CERDIP (Windowed), SOIC and 20-pin SSOP
PIC16C54A	18 Lead	Same as PIC16C54 but with extended operating voltage range and lower operating current.
PIC16CR54	18 Lead	Same as PIC16C54 but with ROM program memory in place of EPROM.
PIC16C55	28 Lead	Same as PIC16C54 but with additional 8-bit I/O port (20 I/O).
PIC16C56	18 Lead	All the features of PIC16C54 but with 1024 x 12-bit words of EPROM program memory.
PIC16C57	28 Lead	All features of the PIC16C55 but with 72 bytes of RAM registers and 2048 x 12-bit words of EPROM program memory.
PIC16CR57A	28 Lead	Same as PIC16C57 but with ROM program memory, extended operating voltage range, and lower operating currents.
PIC16C58A	18 Lead	All features of the PIC16C57 but with one less 8-bit I/O port (12 I/O).
PIC16CR58A*	18 Lead	Same as PIC16C58A but with ROM program memory, extended operating voltage range and lower operating currents.



*Please check with your local Microchip sales support for more information.

PIC16CXX 8-BIT MICROCONTROLLER FAMILY: MID-RANGE PIC16C6X

Function/Description	Part Number	Package	Features
The PIC16CXX family of 8-bit microcontrollers provides the advantages of the enhanced CPU core along with a more powerful array of peripheral features designed to meet the demands of today's mid-range 8-bit embedded control applications. The enhanced CPU core includes enhancements such as multiple interrupt sources, 8 level deep hardware stack and 14-bit wide instruction words. • Higher level of peripheral integration • Upward compatible from PIC16C5X base-line family • Versatile field-programmable EPROM • Cost effective OTP user programmability • RISC-like Harvard Architecture • 35 single word instructions • Multiple Interrupt Sources • Deeper hardware stack • Low power consumption • Small footprint package options • Fast execution throughput • Fuse selectable oscillator options: RC, XT, LP, HS • Three temperature ranges: (0°C to +70°C, -40°C to +85°C and -40°C to +125°C) The PIC16CXX family is supported by user-friendly, yet powerful development tools such as the Windows-based PICMASTER in-circuit emulator. The PICSTART-16C provides a low cost entry level tool to evaluate and begin code development for PIC16CXX devices. Fuzzy Logic Development Tools and a C-Compiler as well as a host of other third party hardware and software tools are also available to support the PIC16CXX family.	**PIC16C61** 	18-Lead	• 1K x 14 EPROM program memory • 36 bytes general purpose RAM • 8-level deep hardware stack • 13 bidirectional I/O lines • 3 interrupt sources including wake-up on change of port • Timer resources include 8-bit real-time clock/counter with 8-bit programmable prescaler • Operating frequencies: DC to 20MHz, low power/voltage option • Packaging options: 18-Lead PDIP, CERDIP (Windowed), 18-lead SOIC for surface mount applications
	PIC16C62 **IN DEVELOPMENT** Contact your local Microchip Sales Office for more information		• 2K x 14 EPROM program memory • 128 bytes general purpose RAM • 22 I/O with individual direction control • Capture/Compare/PWM module • I^2C™ and 3-wire SPI compatible • 8 internal and external interrupt sources • 16-bit timer/counter: two 8-bit timer/counters with prescaler one with post scaler • Operating frequencies: DC to 20MHz, low-power, low-voltage option • Packaging options: 28-lead PDIP, CERDIP and SSOP
	PIC16C64 	40/44 Lead	• 2K x 14 EPROM program memory • 128 bytes general purpose RAM • 33 I/O with individual direction control • Capture/Compare/PWM module • Parallel slave port • I^2C™ and 3-wire SPI compatible Synchronous Serial Port (SSP) • 8 internal and external interrupt sources • 16-bit timer/counter: two 8-bit timer/counters with prescaler one with post scaler • Operating frequencies: DC to 20MHz, low-power, low-voltage option • Packaging options: 40-lead PDIP, CERDIP (Windowed), and 44-lead PLCC, QFP

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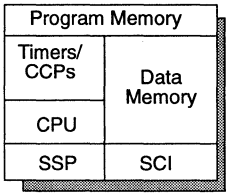
PIC16CXX 8-BIT MICROCONTROLLER FAMILY: MID-RANGE PIC16C6X

Function/Description	Part Number	Package	Features
	PIC16C65	40/44 Lead	• 4K x 14 EPROM program memory • 192 bytes general purpose RAM • 33 I/O pins with individual direction control • 12 external and internal interrupt sources • 2 Capture/Compare/PWM modules • Synchronous Serial Port (SSP) that is I^2C and 3-wire SPI compatible • Serial Communications Interface (SCI) provides USART functions • Parallel slave port • 3 counter/timers, one can be incremented during Sleep Mode via external clock • Operating Frequencies: DC to 20MHz, low power, low voltage option • Three temperature ranges: Commercial, Industrial, and Automotive • Packaging options: 40-lead PDIP and CERDIP (Windowed), 44-lead PLCC, 44-lead QFP



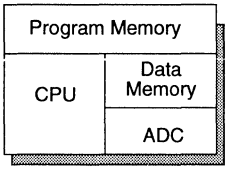
PIC16CXX 8-BIT MICROCONTROLLER FAMILY: MID-RANGE PIC16C62X

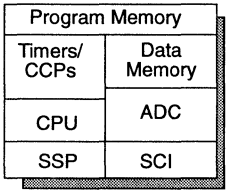
Function/Description	Part Number	Package	Features
	PIC16C620		• 512 x 14 EPROM program memory • 80 bytes general purpose RAM • 4 external and internal interrupt sources • 16 I/O pins with individual direction control • Analog comparator module with two comparators • 8-bit timer/counter with 8-bit programmable prescaler • Packaging options: 18-lead PDIP and CERDIP (Windowed), 20-lead SSOP
	PIC16C621		Same as the PIC16C620 except: • 1K x 14 EPROM program memory • 80 bytes general purpose RAM
	PIC16C622		Same as the PIC16C620 except: • 2K x 14 EPROM program memory • 128 bytes general purpose RAM

IN DEVELOPMENT
Contact your local Microchip Sales Office for more information

PIC16CXX 8-BIT MICROCONTROLLER FAMILY: MID-RANGE PIC16C7X

Function/Description	Part Number	Package	Features
	PIC16C71	18-Lead	• 1K x 14 EPROM program memory • 36 bytes general purpose RAM • 8-bit, 4-channel A/D converter with sample and hold, accuracy of ±1 LSB, 20µs conversion time • 13 I/O pins with individual direction control • 4 internal/external interrupt sources • 8-bit timer/counter with programmable prescaler • Operating frequencies: DC to 20MHz • 4 user selectable oscillator options • Packaging options: 18-pin PDIP and SOIC
	PIC16C73	28 Lead	• 4K x 14 EPROM program memory • 192 bytes general purpose RAM • 22 I/O pins with individual direction control • 11 external and internal interrupt sources • 2 Capture/Compare/PWM modules • 8-bit, 8-channel A/D converter • Synchronous Serial Port (SSP) that is I^2C and 3-wire SPI compatible • Serial Communications Interface (SCI) provides USART functions • Parallel slave port • 3 counter/timers, one can be incremented during Sleep Mode via external clock • Operating Frequencies: DC to 20 MHz, low power, low voltage option • Three temperature ranges: Commercial, Industrial, and Automotive • Packaging options: 28-lead PDIP (300 mil), CERDIP (Windowed) and SOIC





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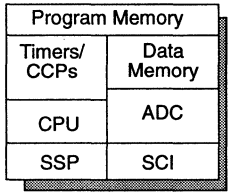
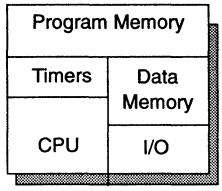
PIC16CXX 8-BIT MICROCONTROLLER FAMILY: MID-RANGE PIC16C7X

Function/Description	Part Number	Package	Features
	PIC16C74	40/44 Lead	• 4K x 14 EPROM program memory • 192 bytes general purpose RAM • 33 I/O pins with individual direction control • 12 external and internal interrupt sources • 2 Capture/Compare/PWM modules • 8-bit, 8-channel A/D converter • Synchronous Serial Port (SSP) that is I^2C and 3-wire SPI compatible • Serial Communications Interface (SCI) provides USART functions • Parallel slave port • 3 counter/timers, one can be incremented during Sleep Mode via external clock • Operating Frequencies: DC to 20MHz, low power, low voltage option • Three temperature ranges: Commercial, Industrial, and Automotive • Packaging options: 40-lead PDIP and CERDIP (Windowed), 44-lead PLCC, 44-lead QFP

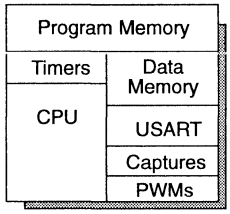


PIC16CXX 8-BIT MICROCONTROLLER FAMILY: REPROGRAMMABLE PIC16C8X

Function/Description	Part Number	Package	Features
	PIC16C84	18-Lead	• Unique 1K x 14 EEPROM program memory • 64 bytes EEPROM data memory • 36 bytes general purpose RAM • EEPROM program memory can be serially programmed in the application circuit • 13 I/O pins with individual direction control • 4 internal/external interrupt sources • 8-bit timer/counter with programmable prescaler • Operating frequencies: DC to 10MHz • Packaging options: 18-pin PDIP and SOIC



PIC17CXX 8-BIT MICROCONTROLLER FAMILY: HIGH-PERFORMANCE PIC17C4X*

Function/Description	Part Number	Package	Features
For high-end applications, the PIC17CXX family of CMOS microcontrollers offers the industry's highest performance 8-bit microcontroller, powerful on-chip peripherals, OTP user flexibility, and world class development tools, all at competitive pricing. • Unique RISC/Harvard architecture • Long 16-bit Instruction Word • Single-cycle/single-word instruction execution for extremely fast execution throughput and compact software code • Instruction set includes enhanced capabilities such as easy and fast utilization of large look-up tables, and the ability to move data in a single instruction cycle • Powerful vectored interrupt handling • Watchdog Timer and Sleep Mode features effectively address the requirements of real-time embedded control applications The PIC17C42 has 55 instructions, and the PIC17C43 and PIC17C44 have 58 instructions including single-cycle hardware multiply. PIC17CXX development is supported by user-friendly, Windows-based PICMASTER-17 Universal Development platform. Software support includes assembler (MPASM), simulator (MPSIM), C-Compiler and fuzzy logic tools.	**PIC17C42** 	40/44 Lead	• 2K x 16 EPROM program memory • 232 bytes general purpose RAM • Can function as stand-alone microcontroller or address up to 64K word external Program Memory • Instruction set includes 55 instructions • 2 fast PWM outputs: 97.6kHz at 8-bit resolution; 24.3kHz at 10-bit resolution (at 25MHz) • Two Capture Inputs with prescaler with 160ns resolution • Full featured USART (SCI) with baud rate generator • 33 I/O pins with individual direction control • Three 16-bit counter/timers which can be configured as two 16-bit and two 8-bit counter/timer • 11 internal and external interrupt sources • 4 fuse selectable oscillator options • Operating frequencies: DC to 25MHz • Temperature range: Commercial and Industrial • Packaging options: 40-Lead PDIP, 40-lead CERDIP (Windowed), 44-lead QFP, 44-lead PLCC
	PIC17C43	40/44 Lead	Same as the PIC17C42 except: • 4K x 16 EPROM program memory • 454 bytes general purpose RAM • 58 instruction includes two hardware multiply instructions
	PIC17C44	40/44 Lead	Same as the PIC17C42 except: • 8K X 16 EPROM program memory • 454 bytes general purpose RAM • 58 instruction includes two hardware multiply instructions

*Additional products are in development. Contact your local sales support for more information.

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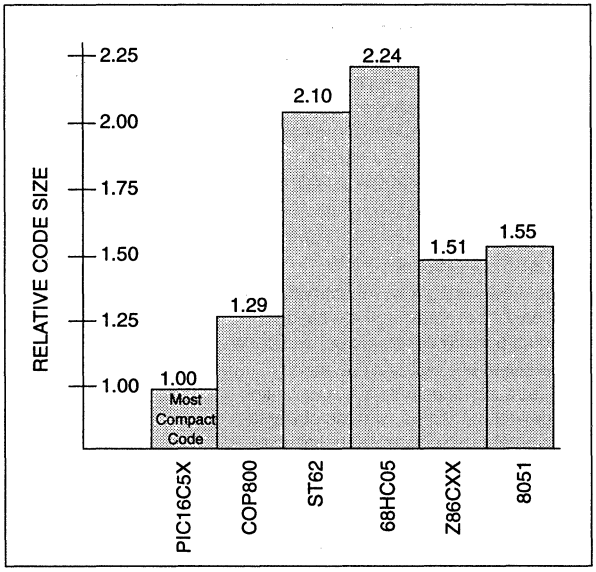
MICROCONTROLLER CODE COMPACTION COMPARISON

With its 12-bit wide program word size, Microchip's PIC16C5X microcontroller demonstrates a code compaction advantage over competing architectures. The table on the right summarizes code sizes for different MCUs. The overall relative code size number is an average of the individual relative code sizes. In this example, 1.5X is the average.

The PIC16C5X MCU exceeds this average in most comparisons because its 12-bit wide instruction word executes instructions in a single cycle. By comparison, all competing architectures have 8-bit program word size, and do not achieve maximum code compaction efficiency.

With its 16-bit wide instruction word, the PIC17CXX microcontroller family produces even greater code compaction over other microcontroller families.



MICROCONTROLLER EMULATOR SYSTEMS

Function/Description		Model Name/ Part Number	Features
CMOS PIC16C5X In-Circuit Emulator System	**PICMASTER®-16D** is a complete high-performance in-circuit emulator system for the **PIC16C5X microcontroller family.** The PICMASTER-16D system operates on PC-compatible 386 and 486 machines under Microsoft Windows 3.X allowing access to a wide range of supporting software and accessories. This universal system also includes the universal PRO MATE programmer. The complete PICMASTER-16D development system supports other PIC16/17 microcontrollers with a simple, low-cost active probe card change.	**PICMASTER-16D** EM167015 (includes PRO MATE) EM167016 (without PRO MATE)	• Emulator system • PROBE-16D PIC16C5X Probe Kit (20MHz) • MPASM macro assembler • MPSIM software simulator • PRO MATE programmer • PICDEM-1 Demo Board • Product sample kit • Demonstration software • Complete system documentation

MICROCONTROLLER EMULATOR SYSTEMS

Function/Description		Model Name/ Part Number	Features
CMOS PIC16C71 In-Circuit Emulator System	**PICMASTER-16B** is the same complete high-performance emulator system as described for PICMASTER-16D but it **supports the PIC16C71** microcontroller products. Includes the PIC16C71 active probe card and the PIC16C71 programming socket.	**PICMASTER-16B** EM167011 (includes PRO MATE) EM167012 (without PRO MATE)	• Emulator system • PROBE-16B PIC16C71 Probe Kit (10MHz) • MPASM macro assembler • MPSIM software simulator • PRO MATE programmer • PICDEM-1 Demo Board • Product sample kit • Demonstration software • Complete system documentation
CMOS PIC16C84 In-Circuit Emulator System	**PICMASTER-16C** is the same complete high-performance emulator system as described for PICMASTER-16D but it **supports the PIC16C84** microcontroller products. Includes the PIC16C84 active probe card and the PIC16C84 programming socket.	**PICMASTER-16C** EM167013 (includes PRO MATE) EM167014 (without PRO MATE)	• Emulator system • PROBE-16C PIC16C84 Probe Kit (10MHz) • MPASM macro assembler • MPSIM software simulator • PRO MATE programmer • PICDEM-1 Demo Board • Product sample kit • Demonstration software • Complete system documentation
CMOS PIC16C64 In-Circuit Emulator System	**PICMASTER-16E** is the same complete high-performance emulator system as described for PICMASTER-16D but it **supports the PIC16C64** microcontroller products. Includes the PIC16C64 active probe card and the PIC16C64 programming socket.	**PICMASTER-16E** EM167017 (includes PRO MATE) EM167018 (without PRO MATE)	• Emulator system • PROBE-16E PIC16C64 Probe Kit (10MHz) • MPASM macro assembler • MPSIM software simulator • PRO MATE programmer • PICDEM-2 Demo Board • Product sample kit • Demonstration software • Complete system documentation
CMOS PIC16C65/73/74 In-Circuit Emulator System	**PICMASTER-16F** is the same complete high-performance emulator system as described for PICMASTER-16D but it **supports the PIC16C65/73/74** microcontroller products. Includes PIC16C65/73/74 active probe card and PIC16C65/73/74 programming socket.	**PICMASTER-16F** EM167019 (includes PRO MATE) EM167020 (without PRO MATE)	• Emulator system • PROBE-16F PIC16C65/73/74 Probe Kit (10MHz) • MPASM macro assembler • MPSIM software simulator • PRO MATE programmer • PICDEM-2 Demo Board • Product sample kit • Demonstration software • Complete system documentation

MICROCONTROLLER EMULATOR SYSTEMS

Function/Description		Model Name/ Part Number	Features
CMOS PIC16C61 In-Circuit Emulator System	**PICMASTER-16G** is the same complete high-performance emulator system as described for PICMASTER-16D but it **supports the PIC16C61** microcontroller products. Includes the PIC16C61 active probe card and the PIC16C61 programming socket.	**PICMASTER-16G** EM167021 (includes PRO MATE) EM167022 (without PRO MATE)	• Emulator system • PIC16C61 Probe Kit (10MHz) • MPASM macro assembler • MPSIM software simulator • PRO MATE programmer • Demo Board • Product sample kit • Demonstration software • Complete system documentation
PIC16C62X	**PICMASTER-16H** is the same complete high-performance emulator system as described for PICMASTER-16D but it **supports the PIC16C62X** microcontroller products. Includes the PIC16C62X active probe card and the PIC16C62X programming socket.	**PICMASTER-16H** EM167023 (includes PRO MATE) EM167024 (includes PRO MATE)	• Emulator system • PIC16C620, PIC16C621, PIC16C622 Probe Kit (10MHz) • MPASM macro assembler • MPSIM software simulator • PRO MATE programmer • Demo Board • Product sample kit • Demonstration software • Complete system documentation
CMOS PIC17C42 In-Circuit Emulator System	**PICMASTER-17** is the same complete high-performance emulator system as described for PICMASTER-16D but it **supports the PIC17C42** microcontroller products. Includes the PIC17C42 active probe card and the PIC17C42 programming socket.	**PICMASTER-17** EM177001 (includes PRO MATE) EM177004 (without PRO MATE)	• Emulator system • PIC17C42 Probe Kit (16MHz) • MPASM macro assembler • MPSIM software simulator • PRO MATE programmer • Demo Board • Product sample kit • Demonstration software • Complete system documentation

MICROCONTROLLER DEVELOPMENT TOOLS

Function/Description		Model Name/ Part Number	Package
Universal Microchip Device Programmer	**PRO MATE™** is a universal programmer for the entire PIC16C5X, PIC16CXX and PIC17CXX microcontroller families. It includes Microchip MPSIM (simulator) and MPASM (assembler) software. It operates either as a stand-alone unit or in conjunction with a PC host system. PC host software provides file display and editing, and transfer to and from the programming unit.	**PRO MATE** DV007001	• Programs all PIC16C5X, PIC16CXX and PIC17CXX microcontroller family members • Operates in stand-alone and PC host mode • Reads, programs and verifies in stand-alone mode • MPASM PIC16/17 assembler software • MPSIM PIC16CXX simulator software
CMOS PIC16CXX Development Kit	**PICSTART®-16B1** is a very low-cost entry-level development system for the PIC16C5X family of microcontrollers including PIC16C71 and PIC16C84. It is a PC hosted system which includes an assembler for code development, a simulator for debug and a development programmer board.	**PICSTART-16B1** DV163003	• MPASM macro assembler • MPSIM software simulator • Development programmer board • Product sample kit • Power supply • RS-232 Cable • Complete system documentation
CMOS PIC16C64/65/73/74 Development Kit	**PICSTART-16C** is a very low-cost entry-level development system for the PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. It is a PC hosted system which includes an assembler for code development, a simulator for debug and a development programmer board.	**PICSTART-16C** DV163002	• MPASM macro assembler • MPSIM software simulator • Development programmer board • Product sample kit • Power supply • RS-232 Cable • Complete system documentation
Fuzzy Logic Development	***fuzzy*TECH®-MP** fuzzy logic development tool supports all PIC16/17 microcontrollers. It comes in two versions – an introductory Explorer version for designers to gain a comprehensive working knowledge of fuzzy logic system design, and a full-featured edition for implementing more complex systems. Both versions come with Microchip ***fuzzy*LAB™** Demonstration Board to give hands-on experience with fuzzy logic systems implementation.	***fuzzy*TECH** DV005001 (-MP Explorer) DV005002 (-MP Edition)	• *fuzzy*TECH software • *fuzzy*LAB Demonstration Board • RS-232 Cable • PIC16CXX production sample • Universal power supply • Complete system documentation • Hardware protection key (on full-featured edition only)

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MICROCONTROLLER DEVELOPMENT TOOLS

Function/Description		Model Name/ Part Number	Package
CMOS PIC16/17 Microcontroller Assembler	**MPASM** is a fully-featured macro-assembler supporting the PIC16C5X, PIC16CXX and PIC17C4X microcontroller product families.	**MPASM** SW005002	• Fully-featured macro assembler • Conditional assembly • Several source and listing formats • Generates various object code formats
CMOS PIC16CXX Microcontroller Simulator	**MPSIM** is a discrete event simulator designed to imitate operation of PIC16C5X, PIC16CXX and PIC17C4X microcontroller product families. It allows the user to debug software that will use any of these microcontrollers.	**MPSIM** SW005002	• Program load and save • Display and alter • Disassembler • Symbolic debug • Execution trace and breakpoints
CMOS PIC16CXX Microcontroller Compiler (Available from Byte Craft Limited, 519-888-6911)	The MP-C Code Development Systems is a complete C Compiler and integrated development environment for Microchip's PIC16/17 family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.	**MP-C**	• Provides Object, Listing, Symbol and special files required for debugging with other Microchip development systems • Supports interrupt routines • Checks source against target hardware definitions • Generates efficient, tight object code • Includes a linker and built-in macro assembler • "C" enhancements specific to the PIC16/17 families' instruction sets • Output formats: INHX8S, INHX8M and INHX32

OTHER LOGIC PRODUCTS - LCD DRIVER

Function	Description	Part Number	Temp. Range	Supply Voltage	Package	Features
Static LCD Driver	Drives up to 32 segments	**AY0438**	-40°C to +85°C	+3.0V to +8.5V	40-Lead DIP 44-Lead PLCC	Static LCD Driver. Cascadable to drive larger number of segments. Serial, clocked data in.

Shortform Catalog to Application-Specific Standard Products

The following shortform catalog will provide an overview to Microchip Technology Inc.'s application-specific standard products including the TrueGauge™ Intelligent Battery Management Family, PC pointing device family, energy management controller, PICSEE 8-bit microcontrollers and development systems.

For further information on application-specific standard products, please refer to individual product data sheets. (Copies can be obtained by calling your local Microchip sales office.)

TRUEGAUGE™ INTELLIGENT BATTERY MANAGEMENT

Function/Description		Part Number	Package	Features
Integrated Battery Capacity Monitoring and Charge Controller	The **MTA11200 TrueGauge Battery "Fuel Gauge" and Charge Controller IC** is a simple full-featured solution to battery monitoring and charging. It is designed to operate with either NiCd, NiMH or lead acid battery packs. The MTA11200 digitally integrates battery charge and discharge current to determine the battery state of charge. The MTA11200 is ideally suited for use in portable computers, portable video equipment, cellular phones, and other products relying on rechargeable battery technology. It excels in applications where an accurate "fuel gauge" is desired to prevent interruption in use, or data loss due to insufficient battery power.	**MTA11200**	28 Lead	• Low-cost • Operates with NiCd, NiMH or lead acid battery pack • From 3.0 volts to 25VDC • Real-time RS-232 interface provides battery data on remaining capacity, total capacity, battery voltage, current and temperature • Five levels of overcharge protection • Automatic measurement of battery capacity and request of condition cycles • Logs battery information such as number of charge cycles, over temperature, under temperature, and over voltage conditions
Programmable Intelligent Battery I.C.	The **MTA14000** is a high performance mixed-signal microcontroller based on Microchip's powerful 8-bit RISC core that enables real-time measurement and processing of battery parameters including voltage, charge current, discharge current, temperature, and total number of cycles. It supports 4096 words of program memory, 192 bytes of RAM, 11 interrupts, 38 special function hardware registers and eight levels of hardware stack. The MTA14000 is ideally suited for use in smart battery controllers, battery chargers, uninterruptable power supply controllers, smart sensors, HVAC controllers and data acquisition.	**MTA14000**	28 Lead	• RISC core • 35 single word instructions • Fully code compatible with Microchip's standard PIC16/17 microcontroller family • 4K Program Memory, 192 bytes RAM, 11 interrupts, eight levels of stack • 8-channel analog-to-digital converter with programmable resolution up to 16 bits • Two 3-decade digital-to-analog converters • Multiple power down controls for analog circuits • Synchronous Serial Port compatible with I^2C™, ACCESS.bus™, System Management Bus • I/O pins with individual direction control allowing for support of any other communications interface such as RS-232 and one-wire

TRUEGAUGE™ DEVELOPMENT TOOLS

Function/Description		Part Number	Features
TrueGauge Development Tool	The **MTA11200 TrueGauge Intelligent Battery Management IC** is support by a user friendly tool for system development. The DV114001 operates under Microsoft Windows™. This development tool enables the management of all phases of product development including inception, debugging and maintenance. System design verification can be accomplished before a hardware prototype needs to be built, thus reducing time and cost. The user interface provides a graphically-oriented development environment. The data logging feature saves measured data into a file that can be imported to Excel®.	**DV114001**	The TrueGauge development tool is a tool for system development under Windows. The development tool kit contains the following: • NiCd battery with TrueGauge module • NiMH battery with TrueGauge module • Stand-alone TrueGauge module • Charger/Discharger Interface Board • Universal power supply with power cord • PC Interface Cable with DB9-DB25 converter • Design/Verification software on a 3.5" diskette • MTA11200 and 24LC01B product samples • MTA11200 data sheet • *TrueGauge Development Tool User's Guide*

PC POINTING DEVICES

Function/Description		Part Number	Package	Features
Mouse Controller	The **MTA41XXX** Mouse Controllers are the heart of a simple, low-cost mouse or trackball solution. The MTA41XXX family supports all Apple® Computer and IBM® PC-compatible formats.	**MTA41300**	18 Lead	Low-cost mouse controller with support for IBM PS/2®-compliant or Microsoft® serial-format-compatible.* The MTA41300 controller supports 2-button mouse or trackball operation. Packaging is available in 300 mil wide PDIP and SOIC
		MTA41110	18 Lead	Low-cost, low power mouse controller with complete support for IBM PS/2 interface format. Like the MTA41300, the MTA41110 controller supports 2-button mouse or trackball operation, but unique software features of the MTA41110 allow for direct input from optical encoders without the need for external comparators. LED strobing is also supported by the MTA41110 for low-power applications.
		MTA41120	18 Lead	Same as MTA41110 except offers complete support for Apple Computer ADB™ interface.

* The code in this product was not developed or licensed by Microsoft Corporation.

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ENERGY MANAGEMENT DEVICES

Function/Description		Part Number	Package	Features
Energy Management Controller	The **MTE1122** Energy Management Controller combines Microchip's proprietary PIC16/17 8-bit RISC microcontroller technology with a unique, patent pending power management firmware algorithm in a single package. This device, by monitoring and controlling the supply requirements into an AC induction motor, effectively reduces the power consumed by the motor. The MTE1122 is available in both plastic DIP and space-saving SOIC packages, and operates over commercial and industrial ranges.	**MTE1122**	18 Lead	• Low cost • Reduces power consumption of AC induction motors • Protects against brownouts and power surges

PICSEE FAMILY OF MICROCONTROLLERS WITH SERIAL EEPROM

Function/Description		Part Number	Package	Features
8-Bit Microcontroller with Serial EEPROM	The **PICSEE**™ offers the unique combination of an EPROM-based microcontroller and a Serial EEPROM in a single package. The MTA81010 is a multi-chip module that integrates a PIC16C54 low-cost, high-performance, 8-bit, fully-static, EPROM-based CMOS microcontroller with a 24LC01B 1024-bit Serial EEPROM configured 128K x 8. The integration of these two popular chips into a single package reduces system cost, board area and inventory.	**MTA81010**	28 Lead	• 512 x 12 EPROM • 1K EEPROM • 32 bytes of RAM registers • 12 bidirectional I/O lines • RTCC timer/counter • Free running watchdog timer and load protection fuse • EEPROM is configured as 8-byte page • Maximum write time 10ms • 100K erase write cycles minimum • 400KHz clock, hardware write-protect • Available in the oscillator configurations RC, XT, LP • Frequency range: from 25KHz through 4MHz down to 2.5 volt operation • Temperature ranges: 0°C to +70°C, –40°C to +85°C, and –40°C to +125°C • Packaging: available in 600 mil wide PDIP, CERDIP (Windowed), SSOP and 300 mil wide SOIC
		MTA85XXX	20 Lead SSOP	• 512 or 2048 x 12 on-chip EPROM • 1K or 2K EEPROM • 25 or 72 x 8 general purpose registers (SRAM) • 7 special function hardware registers • 12 I/O pins with individual direction control • 8-bit real time clock/counter (RTCC) with 8-bit programmable prescaler • Clock frequencies available: 4MHz, 10MHz

PICSEE FAMILY DEVELOPMENT TOOLS

	Function/Description	Part Number	Package	Features
PICSEE Development Kit	**PICSEESTART** is a very low-cost entry-level development system for the PICSEE microcontroller. It is a combination of the PICSEE Adapter Kit and the PIC-START-16B1 Development Kit.	**DV813001 PICSEESTART-81A**	28 Lead	• PICSEE Adapter Kit • PICSTART-16B1 • Product sample kit • Complete system documentation
		DV853001 PICSEESTART-85A	20 Lead	• PICSEE Adapter Kit • PICSTART-16B1 • Product sample kit • Complete system documentation

PICSEE FAMILY PROGRAMMERS

	Function/Description	Part Number	Package	Features
PICSEEKIT	The **PICSEEKITs** are programmer adapters for use in conjunction with PRO MATE or PICSTART programmers. Included is the in-circuit emulation adapter board for the PICMASTER-16A.	**AC812001 PICSEEKIT-81A**	28 Lead	Supports programming of all PDIP, SOIC and JW MTA81010 devices.
		AC814003	28 Lead	Programming adapter sockets for DIP and SOIC devices.
		AC852001 PICSEEKIT-85A	20 Lead	MTA85XXX programming adapter and emulation kit.
		AC854001	20 Lead	20-lead SSOP programming adapter socket.

SECTION 10
QUALITY, RELIABILITY AND ENDURANCE

Product Quality 10-1
Product Reliability 10-9
EEPROM Endurance 10-15

MICROCHIP

Product Quality

A CORPORATE COMMITMENT

Microchip Technology Inc. has evolved a culture where a commitment to quality is an integral part. By empowering every employee to be responsible for the quality of their work, the entire corporation is involved in the quality process. This interaction creates an environment for continuous improvement throughout the organization. The benefits of the system are then not only enhanced product quality and reliability but also product services.

THE CHALLENGE OF COMPLEXITY

Integrating an Ideal

Microchip's quality programs and business plan are vertically integrated and touch all levels of the company. From the top down, the President and CEO actively lead programs to ensure continuous improvement is a perpetual process. Improvement and cross functional teams work to enhance performance at every department level. Incorporating the improvement objectives into the business plan creates a unity of purpose and mandates that the two merge as one measurement.

Determination to be the Best

A fundamental concept at Microchip is the commitment to continuous improvement. All areas are constantly looking for ways to improve every aspect of the company. This has allowed products and processes to become world class in quality and reliability. These programs are the foundation for success.

PROCESS TECHNOLOGY

All the products manufactured at Microchip make use of a common N-Well CMOS baseline process to which modules are added in order to create the specific functions required by the product (EEPROM, Microcontroller, Logic and EPROM).

The baseline process, which has been in Manufacturing for the last 8 years, uses minimum dimensions of 1.5µm, 360Å gate oxide thickness, N+ doped polysilicon gates and arsenic implanted source-drain diffusions for the N-channel devices.

A more advanced process uses minimum dimensions of 1µm, 250Å gate oxide thickness, polycide gate and LDD junction for the N-channel devices. A double level metal module can be added to both processes.

All of these devices utilize a proprietary passivation suitable for a wide variety of package types. Microchip's processes have been developed with reliability and manufacturability as their primary goals.

EEPROM

Microchip's CMOS floating gate EEPROM technology produces a non-volatile memory cell by storing or removing charge from the floating gate. Charge is transferred bidirectionally to the floating gate by Fowler-Nordheim tunneling through a sub-10 nm oxide over the drain of the transistor. This technology produces a memory cell with a typical endurance of $> 10^7$ cycles and greater than 40 years of data retention. (See EEPROM application note for details).

EPROM

This technology uses a non-volatile memory cell which stores charge on a self aligned floating gate. Electrons are provided to the floating gate via hot electron injection from the drain depletion region. Each byte can typically be programmed in 100 microseconds, and can retain that data for more than 10 years with unlimited reads. Block erasing is accomplished with a high intensity UV source through the package window. Windowed parts can be erased and reprogrammed more than 100 times.

Microcontroller and Logic

Logic products are built on a variety of Microchip's processes and their derivatives. These products have process modules for production of controllers that feature ROM, Analog, EPROM, and EEPROM. By utilizing the standard processing modules, the designs meld these technologies and their flexibility while maintaining the high quality and reliability standards expected.

QUALITY

Design for Quality and Reliability

Product reliability is designed into all Microchip processes and products. Design margins are established to guarantee every product can be produced economically, error-free and within the tolerances of the manufacturing process. Product Introduction Teams representing manufacturing, engineering, quality and product divisions ensure that exacting standards are met for each specific product.

Documentation and Procurement Specifications

Microchip's documentation control program assures the correct and current document always is available at the point of use. Active documents are revision coded and serialized. Procurement specifications bear the same requirements. These document control procedures, which are common in the industry for military and high reliability products, are employed by Microchip, system wide.

In Line Controls and Process Assessment

Product integrity is assured by sampling and inspection plans performed in-line. This enables Microchip to control and improve product quality levels as product moves through the manufacturing operation. Microchip's acceptance sampling plans in assembly emphasize the attempt to eliminate defective product as it is discovered. Acceptance and sampling plans are based on proprietary low fraction defective (<1000ppm) quality statistics.

To determine whether a process is within normal manufacturing variation, statistical techniques are put to work at selected process steps. In-process controls are performed by operators in the wafer fabrication and assembly operations. Operators take immediate corrective action if a process step is out of its control limit. Through these in-line controls the true capability of a process is generated. (See Appendix A:In Line Controls)

Control of Customer Quality is attained through a statistical program based on minimum defect capability levels. These levels are defined as the error levels associated with the circuit design and science limitations of the chemistry and physics of processing.

Material controls prevent defective piece parts from getting into the line. Microchip's assembly material control sample plan is typical of the emphasis placed on safeguards. (See Appendix B:Material Controls Package).

Testing for Margin

Microchip conducts a product's initial test under stringent requirements. All quality assurance tests are run to tighter limits than customer specifications. As part of an outgoing quality assurance program, products are tested at least two machine tolerances tighter than those limits specified by the customer on every parameter. Margin testing accounts for normal tolerances of any particular test system and provides the assurance that Microchip's products meet a customer's specifications.

Variation from Expectation

Microchip works to make variation from target as small as possible. The better process is the one that holds the narrowest dispersion. Processes are targeted to maintain Cpk's of >1.5 and currently have typical values of >2.0. Higher process capability values are continually strived for indicating that better process control is being obtained.

Outgoing Quality

Quality Control samples all outgoing product from final testing. These samples measure in-line defect levels after screens have been applied. Root cause analysis follows, initiating technical change to effect continuous improvement.

Programmability Yield

Using programmable devices adds a complexity to the Quality Level interpretation. It is not unlikely that some programmable devices will not program. The programmability yield is dependent on (but not limited to): programmers, technology, array size, and handling.

Any device that does not program properly will not be used in the end system. Therefore, programmability yields should not be used to calculate AQLs.

For convenience, Microchip offers programming services for certain devices. This service is an advantage to the customer since it not only eliminates programmability rejects, but also reduces the handling of the parts. See the individual data sheets for details on our Quick-Turnaround-Production (QTP) service.

RELIABILITY

Process Qualification

No priority is more important than the one where processes under which Microchip products are built operate without fail. All products are stressed beyond normal use limits when undergoing high temperature operating life and retention bake tests. This is done to ensure that the devices meet the strictest reliability guidelines and will maintain industry low failure rates.

Package Qualification

Package qualification measures a component's ability to withstand extreme thermal and mechanical stresses. All products are stressed to high level industrial specifications to ensure reliability.

Ongoing Sampling of Key Reliability Variables

Microchip conducts accelerated mechanical tests, operating life tests and memory retention tests to explore the many ways failures might occur. Data obtained from continuous testing is used to identify potential reliability problems and for defining action courses to improve product. Microchip's reliability knowledge is shared with customers. This data is available for use in customer's own quality and reliability improvement programs and is published in regular quarterly and yearly reports.

RELIABILITY CONCEPTS

Definition

Reliability is the probability of a system or circuit performing its predefined function adequately under specific conditions for a given period of time. Thus, the reliability of a microcircuit is a function of both stress conditions and the time of operation.

The reliability (or probability of survival) range runs from 0 (no chance of survival) to 1 (no chance of failure). Current microelectronic circuits are manufactured and controlled to such tight specifications that reliability figures for the total operation time approaching 1 (i.e., 0.9999) are common. As a result, the complement of reliability, or the failure probability, is more often quoted in current literature.

The failure rate is the rate at which failures occur on units surviving to a specific number of hours of operation. Failure rates per unit circuit-hour would generally be very small. To avoid reporting such small numbers, failure rates have been defined for greater circuit-hours. One thousand circuit-hours is defined as one circuit operating for one thousand hours, or 1,000 circuits operating for 1 hour, etc. The numbers of circuit-hours is the number of circuits multiplied by the number of operation hours for each circuit.

Two methods to define failure rate are commonly used:

- Percent failures per thousand circuit-hours
- Absolute failures per billion circuit-hours, or FITs.

Note that a failure rate of 0.0001%/1000 hours and 1 FIT are equivalent numbers.

Bathtub Curve: Failure Rate Over Time

The generic representational graph of failure rate vs. time takes the shape of a bathtub curve. (See Figure 1).

The early failure rate (infant mortality) period starts from initial operation (time T0) and decreases as time goes on.

Time T1 signifies the end of the infant mortality period. The next phase of the curve occurs between time T1 and T2. This long period of time is distinguished by a nearly constant and very low failure rate. After T2 is passed, the failure rate starts to increase slowly. This last phase of failure rate vs. time is known as the wear-out period.

Temperature Dependency

In order to establish failure rates in a reasonable time, it is necessary to accelerate the incidence of the failure modes. Higher environmental stress levels than those encountered under normal conditions are needed. The accelerating parameter most employed is junction temperature, although voltage and humidity, for example, are also used. Higher temperatures are capable of accelerating many common failure modes dramatically.

Arrhenius Equation

A number of mathematical models were developed to quantify the relationship between accelerated failure rates and increased junction temperatures. The one model most commonly used employs the Arrhenius Equation. It is as follows:

$$AF = e^{x}, \text{ where } x = \frac{E_A}{K}\left[\frac{1}{T_N} - \frac{1}{T_A}\right]$$

AF = Acceleration Factor (non-dimensional)

e = 2.718281828... (non-dimensional constant)

E_A = Activation energy level (electron volts)

k = Boltzmann's constant = 8.6172 x 10-5 (electron-volts/degree Kelvin)

T_N = Normal junction temperature (degrees Kelvin)

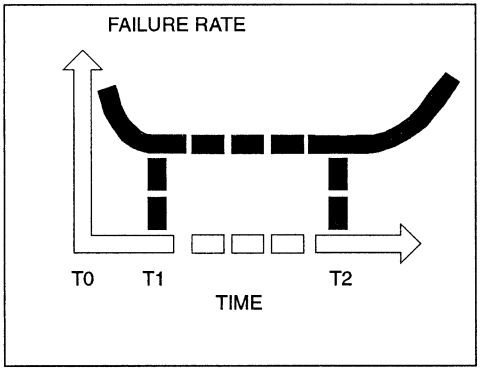
T_A = Accelerated junction temperature (degrees Kelvin)

Thus, the time to achieve a certain probability of failure at time T1 under temperature TN can be compressed to T1 divided by AF at the accelerated temperature, TA.

Note that for true acceleration, the acceleration factor AF is independent of the probability of the fail point specified.

AF, the dependent variable of the Arrhenius Equation is a function of several variables. TN and TA are specified for the situation under consideration. EA is a function of the particular mode of failure, and is determined by experimental evaluation.

FIGURE 1: BATHTUB CURVE



Activation Energy Level

Activation energy levels in semiconductors generally are in the 0.3 - 1.1 electron-volt range. Each failure mode has its own activation energy. Some typical examples are:

FAILURE MECHANISM	EA (eV)
Oxide/Dielectric Breakdown	0.3
Electromigration	0.5 to 0.7
Surface Related Contamination	1.0
Intermetallics	1.0
Floating Gate Charge Loss	0.6 to 1.2
Hot Electron Trapping	-.1
Charge Trapping	0.12

A compromise value of 0.6 electron-volts is often used when there is no specific information relating to the failure modes being accelerated.

RELIABILITY TESTS

Operating Life Test

The Operating Life Test is run under dynamic bias conditions where inputs are clocked. The test is conducted at high temperature to accelerate the failure mechanisms. The normal temperature for the test is +125°C for 1,000 hours. Readouts occur at 168 and 1,000 hours. Early hour failures are usually associated with manufacturing defects or otherwise marginal material.

Retention Bake

The Retention Bake Test is performed to accelerate data loss on floating gate devices. The test consists of unbiased baking at elevated temperature. Usually the test lasts for 1,000 hours at +150°C. The failure mechanism that is accelerated is charge leakage from a stored element.

Endurance Cycling

Endurance Cycling establishes the number of times a device can be programmed and erased. Normally the test is conducted at rated temperature conditions and is followed by retention bake. The standard cycling at Microchip is done at 85°C using a page cycle mode and is followed by a bake of both a checkerboard and an inverse checkerboard of 48 hours at 150°C.

Temperature Cycle

The Temperature Cycle test simulates stresses which occur to systems during power up/power down sequences. The test is intended to reveal any deficiencies resulting from thermal expansion mismatch of the die/package structure. Normally the test is conducted by cycling between -65°C and +150°C in an air ambient. Duration for the test is typically 500 cycles for both plastic and ceramic packages. Endpoint criteria are both electrical and visual/mechanical.

Thermal Shock

The Thermal Shock test is similar to the Temperature Cycle test except that the ambient during cycling is liquid-to-liquid. This stimulates rapid thermal environmental changes. The mechanisms accelerated are identical to those in the Temperature Cycle test except that the Thermal Shock test is a more accelerated test with temperatures normally +125°C to -55°C. The number of cycles are 500 for qualification testing.

Autoclave

The autoclave test determines the survivability of devices in molded plastic packages to a hot, humid environment. The test exposes unbiased, plastic packaged devices to saturated steam at 121°C and 15 pounds per square inch (one atmosphere) gauge pressure. The 168 or more hours of testing allows moisture to penetrate into the die. Chemical corrosion of the die metallization may occur if ionic contaminants are present and the die surface protection is deficient or damaged. Charge leaks from floating devices usually happen before a corrosion mechanism develops.

Temperature Humidity Test

The Temperature Humidity test determines the survivability of devices in molded plastic packages functioning in a hot, humid environment. By convention, test conditions are 85°C with 85% relative humidity. The parts are biased to lend themselves to electrochemical corrosion. The duration of the test is usually 1,000 hours or more. The test checks the adequacy of the die surface protection and the plastic's lack of ionic impurities. The applied bias is 5 volts on alternating pins or set up for minimum power to reduce internal heating and consequent moisture evaporation on the device. Similar to the Autoclave test, charge loss on floating gate devices is a principle failure mechanism.

HAST

The Highly Accelerated Stress Test is similar to the Temperature Humidity Test but with more stringent temperature exposure. Devices are subjected to 130°C with 85% relative humidity and an alternating bias of 5 volts and ground on device pins. The duration of the test is 168 hours. This tests for ionic contamination and corrosion, but floating gate devices may also fail for charge loss, due to the high temperature.

QUALIFICATION CATEGORIES

In general, qualification is required for new design, major changes in old design, process or material when either wafer fabrication or package assembly operations are affected. Cross functional teams which include reliability develop new products for introduction. In other areas, Microchip utilizes the concept of a Change Control Board which meets regularly to establish which criteria is to be used for all specific proposed changes. This board is made up of representative leaders of various groups and departments throughout Microchip to insure all concerns are heard early during the process.

QUALIFICATION PROGRAMS

Qualifications guarantee changes to or new processes and technologies are properly evaluated for reliability performance.

Reliability Monitoring

Microchip's reliability monitoring program is a comprehensive effort to measure the reliability of all process families with strict regularity. The program strives to improve performance through failure analysis and corrective action. Numerous screening procedures are used and estimates of product life and expected failure rates are provided.

Typical tests and frequencies include:

- Die Monitor on selected product for -
  - Dynamic Life
  - Retention Bake
  - Endurance
- Periodic (weekly, monthly and quarterly) package monitors to evaluate:
  - Mechanical stresses
  - Alignment
  - Temperature and moisture stresses
  - Corrosion resistance
  - Marking permanency

APPENDIX A: IN LINE CONTROLS

TABLE 1: CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Die Visual	Reject defectives 100% rescreen per LTPD	10% sample LTPD 10	— X	X —	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	—	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	4X/Lot/Machine LTPD 15	X	—	N/A
Wire Bond	Machine Shut Down	1% AQL each 1/2 shift	X	—	MIL-STD-883C Method 2010
Post Wire Bond	Reject defectives 100% rescreen per LTPD	LTPD 15	X	—	MIL-STD-883C Method 2010
Mold Press	Machine Shut Down	One sample /4 hrs	X	—	N/A
Die Plating	Reject defectives 100% rescreen per LTPD	Every 4 hrs LTPD 10	X	—	N/A
Trim and Form	Reject defectives 100% rescreen per LTPD	Once/ 2 hrs LTPD 10	X	—	N/A
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2010, Method 2016

TABLE 2: CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Die Visual	Reject defectives 100% rescreen per LTPD	10% LTPD 10	— X	X —	MIL-STD-883C Method 2010
Wafer Saw	Machine Shut Down	One kerf per lot	X	—	MIL-STD-883C Method 2010
Die Attach	Machine Shut Down	Non-destruct each 2 hrs destruct each shift	X	—	MIL-STD-883C Method 2010
Wire Bond	Machine Shut Down	4X/shift/machine	X	—	MIL-STD-883C Method 2010
Preseal Visual	Reject defectives 100% rescreen per LTPD	100% LTPD 15	— X	X —	MIL-STD-883C Method 2010
Package Seal	Machine Shut Down	LTPD 15	X	—	N/A
Environmental Stress Centrifuge Temp Cycle	Machine Shut Down	LTPD 5 84(0) 84(0)	X	—	MIL-STD-883C Method 2001 Method 1010
Fine Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	—	MIL-STD-883C Method 1014
Gross Leak	Reject defectives 100% rescreen per LTPD	LTPD 5	X	—	MIL-STD-883C Method 1014
Lead Trim	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2009
External Visual and Documentation Verification	Reject defectives 100% rescreen per LTPD	100% LTPD 2	— X	X —	MIL-STD-883C Method 2010, Method 2016

APPENDIX B: MATERIAL CONTROLS PACKAGE

TABLE 3: MATERIALS CONTROLS - PLASTIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Lead Frame	Reject defectives 100% rescreen per LTPD	Visual, LTPD 2 Functional, LTPD 10 and material spec	X	—	N/A
Die Attach Epoxy	Reject	Functional, LTPD 15 and material spec	X	—	N/A
Gold Wire	Reject	Per material spec	X	—	N/A
Molding Compound	Reject	Spiral flow, 3X/lot Functional, 1X/lot and material spec	X	—	N/A

TABLE 4: MATERIALS CONTROLS - CERAMIC PACKAGE ASSEMBLY

Operation	Action	Sample Plan	Responsibility		Referenced MIL-STD
			Quality	Prod	
Base/Lead Frame	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	—	MIL-M-38510
Package	Reject 100% rescreen per LTPD	Visual, LTPD 10 Functional, LTPD 10 Bake test, LTPD 15 Dimensions, LTPD 50 and material spec	X	—	MIL-M-38510
Preform	Reject	Visual, LTPD 10 Functional, LTPD 15	X	—	MIL-M-38510
Bond Wire	Reject	Per material spec 2 spools/lot	X	—	MIL-M-38510
Lid	Reject	Visual, LTPD 7 Functional, LTPD 10 and material spec	X	—	MIL-M-38510

MICROCHIP

Product Reliability

OVERVIEW

Microchip Technology Inc.'s products provide competitive leadership in quality and reliability, with demonstrated performance of less than 100 FITs (Failures in Time) operating life for most products. The designed-in reliability of Microchip's products are supported by ongoing reliability data monitors. This document presents current data for your use - to provide you with results you can count on.

The test descriptions included in this document explain Microchip's quality and reliability system. The product data demonstrates its results.

The customer's quality requirements are Microchip's top priority. Ongoing customer feedback and device performance monitoring drive Microchip, leading to continuing improvements in the long-term quality and reliability.

FAILURE RATE CALCULATION

Extended field life is simulated by using high ambient temperature. In the semiconductor technology, high temperatures dramatically accelerate the mechanisms leading to component failure. Using performance results at different temperatures, an activation energy is determined using the Arrhenius equation. For each type of failure mechanism, the activation energy expresses the degree to which temperature increases the failure rate.

The activation energy values determined by Microchip Technology agree closely with those published in the literature. For complex CMOS devices in production at Microchip Technology, an activation energy of 0.6 eV has been shown to be representative of typical failures on operating life. This activation energy also applies to some of our retention bake failures, though most are 1.2eV. By definition, failure is reached when a device no longer meets the data sheet specifications as a direct result of the reliability test environment to which it was exposed. Common failure modes for CMOS integrated circuits are identified for each test environment.

To establish a field failure rate, the acceleration factor is applied to the device operating hours observed at high temperature stress and extrapolated to a failure rate at 55°C ambient temperature in still air.

The actual failure rate experienced could be considerably less than that calculated if lower device temperatures occur in the application board, such as would be the case if a fan, a heat sink, or air flow by convection is used.

Environment	Typical Failure Mechanism
Operating Life	Process parameter drift/shift Metal electromigration Internal leakage path Lifted bond/ball bond chip-out
Temperature Cycle	Lifted bond/ball chip-out Cracked die or surface cracks Bond pad corrosion
Biased-Humidity	Internal circuit corrosion
Autoclave	Inter-pin leakage Charge loss
High Temp. Bake	Charge loss
High Temp. Reverse Bias	Charge gain, Parameter drift/shift

DEFINITIONS

FIT (Failure In Time): Expresses the estimated field failure rate in number of failures per billion power-on device-hours. 100 FITS equals 0.01% fail per 1,000 device-hours.

Operating Life Test: The device is dynamically exercised at a high ambient temperature (usually 125°C) to quickly simulate field life. Derating from high temperature, an ambient use condition failure rate can be calculated.

Temperature Cycle: The devices are exposed to severe extremes of temperature in an alternating fashion (-65°C for 15 minutes, 150°C for 15 minutes per cycle). Package strength, bond quality and consistency of assembly process are stressed using this environment.

Biased-Humidity: Moisture and bias are used to accelerate corrosion-type failures in plastic packages. The conditions include 85°C ambient temperature with 85% relative humidity. Typical bias voltage is +5 volts and ground on alternating pins.

Autoclave (pressure cooker): Using a pressure of one atmosphere above atmospheric pressure, plastic packaged devices are exposed to moisture at 121°C. The pressure forces moisture permeation of the package and accelerates related failure mechanisms, if present, on the device.

Thermal Shock: Exposes devices to extreme temperatures from -55°C to +125°C by alternate immersion in liquid media.

Retention Bake: A 150°C temperature stress is used to accelerate charge loss in the memory cell and measure the data retention on the EPROM and EEPROM portions of the circuitry.

HAST: Moisture, extreme heat and bias are used to accelerate corrosion and contamination in plastic packages. The conditions are 130°C and 85% relative humidity. Typical bias voltage is +5 Volts and ground on alternating pins.

RELIABILITY CONTROL SYSTEM

A comprehensive qualification system ensures that released products are designed, processed, packaged and tested to meet both design functionality and strict reliability objectives. Once qualified, a reliability monitor system ensures that wafer fabrication and assembly process performance is stable over time. A set of baseline specifications is maintained that states which changes require requalification. These process changes can only be made after successful demonstration of reliability performance. This system results in reliable field performance, while enabling the smooth phase-in of improved designs and product capability.

RELIABILITY DATA SUMMARY

Introduction

This section provides a reliability summary of Microchip Technology's product. Included is reliability data and packaging information obtained over the recent past.

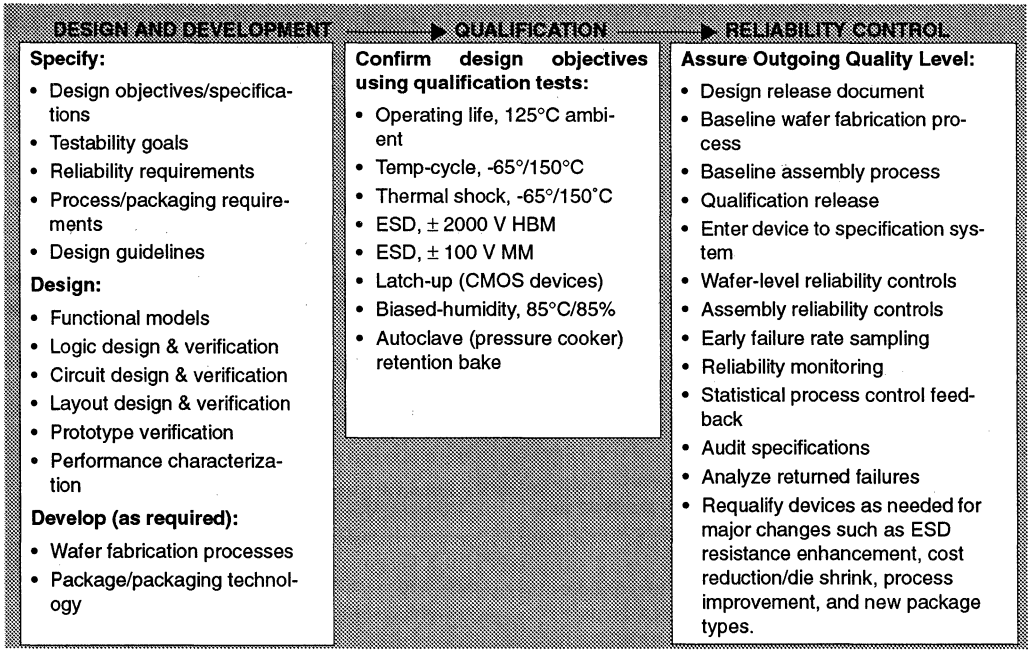
Plastic Package Characteristics and Codes

As part of an on going product program, Microchip Technology will apply its Quality and Reliability process in evaluating the latest developments in plastic packaging technology, and implement the highest reliability materials and assembly techniques. The plastic packages that are currently available from Microchip are listed in the table below.

Package Description Identification Code

Package Description	Identification Code
Plastic Leadless Chip Carrier	L
Plastic Dual In Line (600)	P
Plastic Dual In Line (300)	SP
Plastic SOIC (.150)	SL/SN
Plastic SOIC (.207)	SM
Plastic SOIC (.300)	SO
Plastic TSOP (8 x 20mm)	TS
Plastic SSOP (.207)	SS

FIGURE 1: RELIABILITY CONTROL SYSTEM DIAGRAM



HIGH TEMPERATURE (125°C) DYNAMIC LIFE TEST

Graph set for EEPROM, PIC16/17 and EPROM for all conditions

High temperature dynamic life testing accelerates random failure modes which would occur in user applications. Voltage bias and address signals are used to exercise the device in a manner similar to user systems.

FIGURE 2: EEPROM DYNAMIC LIFE

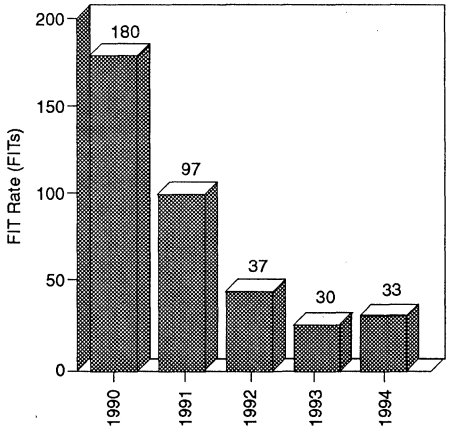


FIGURE 3: EPROM DYNAMIC LIFE

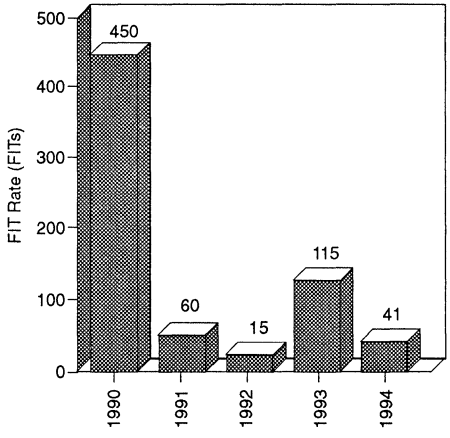
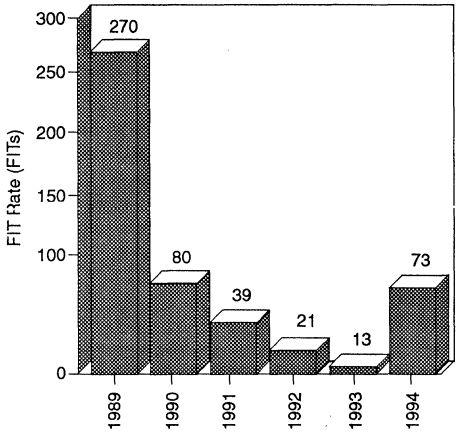


FIGURE 4: PIC16/17 MICROCONTROLLER DYNAMIC LIFE



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DATA RETENTION BAKE

Data storage in applicable devices is done by developing a charge on the floating gate structure in the memory cell. Charge loss in this cell structure results in a conversion of zeroes to ones. In order to evaluate the level of this type of failure, devices are subjected to a 150°C bake. This bake accelerates charge loss in the memory cell and 1000 hours at 150°C is equivalent to approximately 13.5 years in the field at 55°C.

FIGURE 5: EEPROM RETENTION BAKE

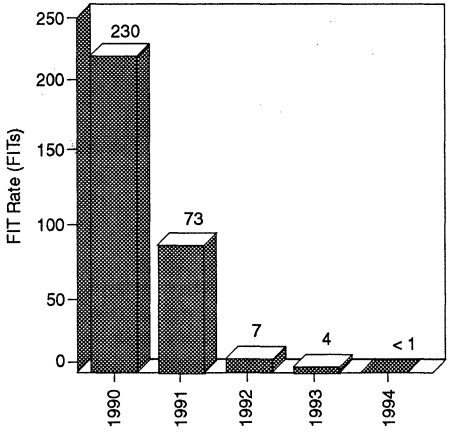


FIGURE 6: EPROM RETENTION BAKE

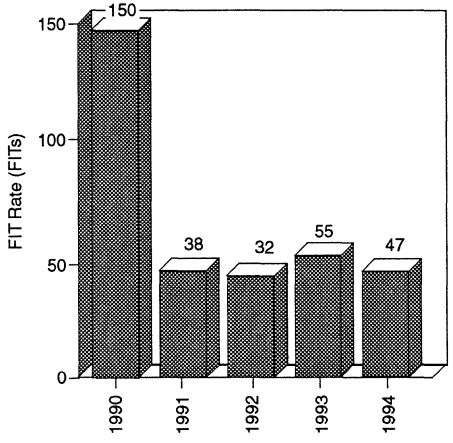
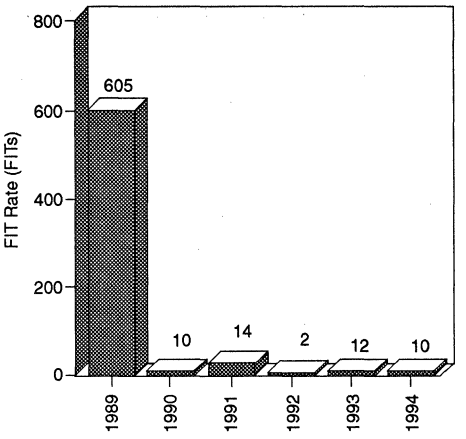


FIGURE 7: PIC16/17 MICROCONTROLLER RETENTION BAKE



NOTE: Representation of reliability data typically shows calendar year grouping along the x-axis, except for 1993 which includes only first, second and third quarters. This provides the equal time interval normally expected for graphical presentation. However, Chi-square statistics demand equivalent device-hours for fair interval comparison. Such data grouping assures that relatively small sample sizes do not indicate unrepresentative FIT rates.

BIASED 85°/85% R.H.

Microchip Technology evaluates plastic encapsulated devices ability to withstand high temperature, high humidity environments while under electrical bias. This is done by utilizing the industry standard test method known as 85/85. This stress is designed to create corrosion of the metal or internal device leakage if ionic contaminants are present but also may cause charge loss in memory cells.

Operating Hours				
Package	**24**	**168**	**504**	**1008**
PDIP	0/5152	2/5152	2/5150	4/5148
PLCC	0/3909	5/3909	2/3904	3/3902
SOIC	0/4827	5/4827	1/4694	0/4693
TSOP	0/377	0/377	0/377	0/377

PCT (AUTOCLAVE)

Originally, this test was designed to evaluate corrosion of bond pads due to penetrating moisture combining with contaminant residue on the metal surface. The corrosion failure rate for this test has become nearly zero and a new failure mode has surfaced. This is memory cell charge loss due to moisture penetration along the floating gate allowing a conduction path for removal of stored charge. This moisture path is between the seal of the metal and the passivation which can then be traced to the substrate near the edge of the floating gate. This failure type is the primary mode in the data provided.

Operating Hours		
Package	**24**	**168**
PDIP	0/10199	5/10199
PLCC	0/4978	4/4978
SOIC	0/8764	7/8764
TSOP	0/234	2/234

TEMPERATURE CYCLING

This thermal tests evaluates air to air rapid temperature change evaluating built in material stresses. This is a worst case simulation of system power up/ power down and is based on stringent military packaging requirements.

Operating Results			
Package	**15 Cycles**	**100 Cycles**	**500 Cycles**
PDIP	0/3112	3/2514	3/2054
PLCC	0/1413	0/1275	1/907
SOIC	0/1895	0/1665	0/837
TSOP	0/234	0/96	0/96
SSOP	0/240	0/194	0/94
VSOP	0/46	0/0	0/0

THERMAL SHOCK

Thermal shock is the most extreme case of temperature cycling by using liquid immersion for the technique to change the device environment. This accelerates any stress related failures with the rapidly changing gradient. After the temperature stressing a constant force centrifuge test is also preformed prior to final electrical testing to further uncover any defects that may have occurred under stress.

Operating Results			
Package	**15 Cycles**	**100 Cycles**	**500 Cycles**
PDIP	0/5700	2/3386	0/2682
PLCC	0/2365	2/1487	7/1292
SOIC	0/3422	0/2332	0/2056
TSOP	0/330	0/234	0/96
SSOP	0/234	0/140	0/94
VSOP	0/46	0/46	0/0

HAST (130°/85% R.H.)

Highly Accelerated Stress Testing evaluates plastic encapsulated devices' ability to withstand extreme high temperature, high humidity environments while under electrical bias. This is done by a new method known as HAST. This stress is designed to create corrosion of the metal or internal device leakage if ionic contaminants are present but also may cause charge loss in memory cells.

Operating Results		
Package	**48 Hours**	**168 Hours**
PDIP	1/3707	1/2030
PLCC	2/1542	0/1170
SOIC	5/2784	3/2779

PRODUCT RELIABILITY DATA

CMOS PIC16/17								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	FITS 60% CL@55°C
PIC16C57	DLT	0/11648	11/11648	0/5316	0/5316	11	6,422,304	47
PIC16C56	DLT	0/9192	1/9192	1/3672	1/3671	3	4,628,736	22
PIC16C55	DLT	0/9215	1/9215	1/4562	2/4561	4	5,380,200	23
PIC16C54	DLT	1/13424	1/13423	3/7334	1/7331	6	8,415,792	21
PC16C84	DLT	0/1305	0/1305	0/1023	1/1023	1	1,078,560	45
PIC16C57	BAKE	0/13092	0/13092	1/2788	0/2787	1	4,541,376	4
PIC16C56	BAKE	0/11136	2/11136	0/2280	0/2280	2	3,786,048	7
PIC16C55	BAKE	0/9887	1/9887	1/2823	1/2822	3	4,032,336	9
PIC16C54	BAKE	0/15938	2/15938	1/4689	0/4688	3	6,616,344	5
PIC16C84	BAKE	0/485	0/485	0/485	0/485	0	488,880	< 1
EEPROM								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	FITS 60% CL@55°C
24CXX	DLT	0/18597	1/18597	2/5735	4/5733	7	7,941,696	25
93CXX	DLT	2/6993	4/6991	0/2601	0/2601	6	3,359,664	52
24LCXX	DLT	0/15164	3/15164	2/8427	3/8425	8	9,626,232	24
93LCXX	DLT	0/7771	5/7771	3/3188	2/3185	10	3,983,448	69
28C16	DLT	0/2681	2/2681	0/1071	0/1071	2	1,350,048	55
28C64	DLT	1/5800	4/5799	0/2586	0/2586	5	3,146,640	48
24CXX	BAKE	2/14345	1/14343	1/3600	2/3599	6	5,433,960	< 1
93CXX	BAKE	0/6320	0/6320	0/1425	0/1425	0	2,258,760	< 1
24LCXX	BAKE	0/11842	0/11842	0/5004	1/5004	1	6,192,816	< 1
93LCXX	BAKE	0/6969	0/6969	0/3192	0/3192	0	3,852,072	< 1
28C16	BAKE	1/3840	2/3839	2/797	1/795	6	1,314,600	< 1
28C64	BAKE	0/3942	26/3942	1/1144	1/1143	28	1,623,216	1
EPROM								
		Operating Hours						
Device	Operation	24	168	504	1008	Fails	Device Hours	FITS 60% CL@55°C
27HC256	DLT	0/2316	1/2316	1/1166	0/1165	2	1,368,528	54
27C256	DLT	1/9666	4/9665	0/2028	0/2028	5	3,327,408	45
27C512	DLT	0/3658	4/3658	0/1260	0/1260	4	1,672,944	75
27HC256	BAKE	0/2656	5/2656	1/627	0/626	6	972,888	64
27C256	BAKE	2/9905	3/9903	0/2478	1/2478	6	3,745,560	17
27C512	BAKE	2/3334	16/3332	1/570	2/569	21	1,038,912	188

Operation Legend: DLT - Dynamic Life Test (125°C) Bake -Retention Bake (150°C)

EEPROM Endurance

INTRODUCTION

A unique feature of non-volatile memory devices is the dual requirement both to change and to maintain data states. It is this combination of requirements that provides the contrasting nature that defines the complexities involved in change and maintaining such change. Anything that enhances the physics to allow a data state change in contrast degrades the retention of that change. It also holds that any retention enhancements inhibit the data changing capabilities. A balance must be struck between the combinations to achieve the field requirements of customer applications.

Erase/Write cycling has many variables which greatly effect the lifetime of the device. To accurately make comparisons between specifications and the actual requirements, or any other comparisons, these factors must be well understood and taken into account.

TECHNOLOGY OVERVIEW

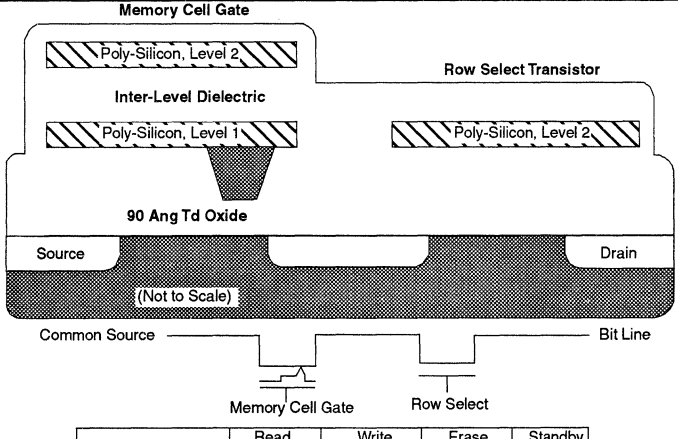
Silicon Technology

The basic technology employed by Microchip Technology for EEPROM's is a FLOTOX structure as drawn below. This is a an industry standard architecture base which has been enhanced by Microchip to provide improvements to the quality and reliability of the devices produced.

Circuit Technology

These cells are then structured in either an 8 or 16 bit word organization for data storage with between 32 words (256 byte device) and 8K words (64K device) using standard binary decoding schemes found industry wide on memory devices. Data can then be transmitted either into the device for storage or read from the device when needed along a single DATA pin, (I^2C bus) or a dual Data in/Data out configuration (3-wire bus). The device has no restriction on the number of read cycles that can be processed per byte without damage but the storage process does have finite limitations.

Currently two different schemes of error correction are being utilized on Microchip EEPROM's. The 24CXX, 93CXX, 85CXX, 59CXX and 28CXX device types utilize a modified Hamming code redundancy scheme with four parity bits per eight bit byte. This has been the industry standard correction scheme for enhancement of cycling lifetimes by eliminating single bit per word errors. An alternative approach has been developed utilizing an AND cell concept of redundant memory cells. This further enhances the write/erase lifetime over the Hamming code and has been implemented on the 24LCXX and 93LCXX circuits.



	Read	Write	Erase	Standby
Bit Line	1.6 volts	18.0 volts	0.0 volts	0.0 volts
Row Select Gate	5.0 volts	20.0 volts	20.0 volts	0.0 volts
Memory Cell Gate	5.0 volts	0.0 volts	20.0 volts	0.0 volts
Common Source	0.0 volts	Float	0.0 volts	0.0 volts

10

Reliability Endurance

The endurance failure rate curve for the Microchip devices is presented in the standard form for this curve from EEPROM FLOTOX manufacturers. Microchip does write/erase cycle all EEPROM devices prior to shipment to remove the infant mortality endurance failures from the population. This characteristic curve, with two failure increase sections, is shown below for reference. Both sections have single bits failing as the dominant mechanism.

The first of the failure increase sections is usually related to breakdown of oxides from latent oxide defects that are inherent to any process. These oxides have reached a time dependent dielectric breakdown condition and permanently rupture. This generally characterizes the first 200K write/erase cycles under any conditions. The second curve is the standard trap up of electrons within the tunnel dielectric which closes the write/erase threshold window until the device no longer adequately programs or erases.

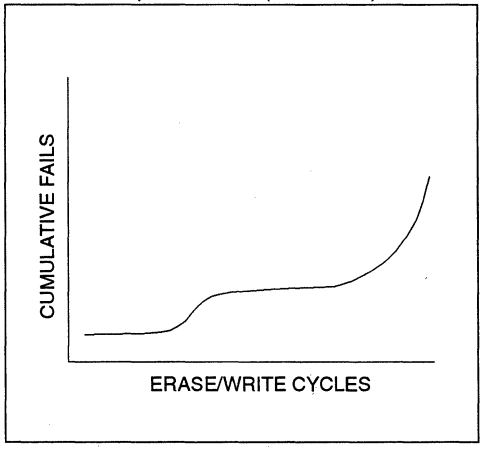
This curve depends on multiple parameters, but the trap up failure increase portion often does not occur until ten million write/erase cycles or greater.

The first failures from endurance cycling and the long term end of life failures are due to different mechanisms.

The failures from 200K to 500K cycles have historically been attributed to "fast trap up" around the industry. Analysis at Microchip has shown that these failures are not actually trap up but oxide breakdown in nature. They most often manifest themselves as single bit charge loss or charge pump failure, both due to the formation of a conductive path within the gate oxide layer.

These oxide breakdown failures can be related to defects of three types of categories.

Type 1 is a residual chemical stain left behind on the wafer after processing due to an inadequate rinse. These are very difficult to physically detect and are best inferred from a pattern of bits (a bit cluster) that fail.



Type 2 is a physical defect which can be found upon microscopic or SEM analysis resulting in the failure. This is most often a particle, polysilicon nodule or metal short.

Type 3 is a physical defect with low activation energy that cannot be detected until end of life evaluation because of it's change in state (subsequent consumption) during latter processing steps.

The end of life mechanism is called "oxide trap up". This is where the tunnel dielectric oxide layer loses it's ability to pass charge and begins to retain some portion of the charge that it passes to the floating gate. These excess electrons within the oxide act as a charge shield, resulting in insufficient charge movement while significantly raising the voltage required to continue transmitting a constant charge level. Since the programming voltage is not adjustable this results in less charge movement for either the write or erase state. These states, whether charged negatively or charged positively, approach a central point and become indistinguishable to the detection circuitry of the device. This results in a failure to read the correct pattern, (impossible to distinguish between a programmed one and a programmed zero) beginning with the extreme voltage values of the operating specification.

Microchip strives to offer the lowest failure rate for both early life and wearout fails. Early fails in Microchip products are in the PPM range, and wearout does not set in most applications until after ten million cycles.

MEASUREMENT OF CYCLING

Microchip Technology defines a device lifetime in the strictest sense, that is, stated lifetime has to exhibit the truest correlation to customer results. All units shipped from Microchip have Error Correction circuitry engaged for customer use. Error Correction amends any one error per byte for Hamming and one error per bit for AND cell which allows the device to read correct data. An endurance failure is determined when any one bit is not capable of being correctly written and maintained in that state indefinitely.

The device lifetime is defined when a specified percentage of devices, (Microchip currently uses a cumulative 2.5 percent), have a customer detectable error under worst case operating conditions.

Ongoing monitors are acquired from every wafer lot of material manufactured for shipment. Samples are subjected to byte cycling of a checkerboard pattern at 85°C in rapid succession to the specified number of guaranteed cycles. These units then are baked in both checkerboard and inverse checkerboard forms and electrically tested to ensure that data sheet requirements are met. This data is accumulated on a monthly basis and reviewed to measure both results of continuous improvement programs and conformance against the device standards.

ENDURANCE VARIABLES

a) **Temperature:** Within the FLOTOX technology, temperature has an inverse effect on the endurance of a EEPROM device. The activation energy of these cycling failures is approximately 0.15 eV. The long term trap up portion of the curve is worsened by temperature to a greater extent than the early fails due to the difficult failure mechanisms that are activated.

b) **Delay between cycles:** This has been reported in the industry as having an enhanced effect on the lifetime of EEPROM devices. For some technologies this does have a positive effect, however, this is not strictly the case for FLOTOX manufacturers. While the second failure rate increase period (associated with end of life) may be impacted by this due to a decreased rate of electron trapping, the first failure rate is actually not impacted by this variable.

c) **Write timing:** The decrease in write time to the device correlates directly with write/erase cycling failure rate of the device. This shorter pulse reduces the cell time at voltage which then provides an enhanced life prior to the occurrence of a time dependent oxide breakdown. It also passes fewer electrons through the oxide providing less potential trapping possibilities while maintaining adequate margins for the written state.
Please note that the rise time of the signal, which the customer does not have control over is also a dominant effect.

d) **Vcc voltage:** The higher voltages generate higher fields within the device. This causes more stress which is offset by the operational increase of internal timers and actually shortens the write time of the device.

Lower voltages this has the opposite effects on the individual parameters except in cycles obviously where the write timer is externally controlled. This overall effect is minor compared to the others in magnitude on the failure rate curve and is variable over the customer operating range with a maximum at V_{CC}=5.5 Volts.

e) **Pattern effect:** The pattern that is programmed in the device does play a first order role in the overall lifetime. The act of programming a nonvolatile memory inflicts damage on the device that cannot be repaired. This damage is the result of exposure to high electric fields which over a period of time either breakdown or trap up the effected oxide causing failures. The act of writing a cell from a one to a zero provides the maximum amount of stress by exercising the charge pump and passing electrons through the tunnel dielectric. (Please note that to write a zero even from a zero state causes an automatic byte erase prior to the write converting the bit to a one and returning it to it's original state!) Conversely writing a one from a one then passes no charge through the cell and therefore does no damage to the cell but does stress the charge pump.

From an array standpoint, this would allow a checkerboard/ inverse checkerboard patterned device to endure twice the number of write cycles that an all zero patterned device would last. In general this appears to be approximately correct but does neglect the charge pump and other peripheral wearout mechanisms.

f) **Cycling mode:** Three modes exist in Microchip devices that are primarily used for endurance evaluations. The byte write mode (one single byte written at a time) is the standard mode used by the customer in the field. A second technique exists called block mode which exercises all the cells of the array simultaneously. The lifetime expectations are approximately ten times as long for these block cycled devices as equivalently cycled byte cycled circuits based on experimental findings. This effect has been traced back to the rise time of the programming signal at the memory cell. The faster this voltage rise occurs, the more damage occurs and the shorter the lifetime. The block mode has a much slower rise time given the entire array being utilized provides a much larger resistive/capacitive load which slows the signal rise ultimately resulting in the greater lifetime. Please note that the page mode which can be utilized by the customers falls between the block and byte modes with respect to failure rate. Page mode offers the best balance of endurance and write cycle times.

g) **Array Size:** This effect is a direct result of how fast most devices will fail due to a single bit not working simply due to the number of bits involved. This is not exactly double the failure rate with a doubling of the memory size since some circuits fail within the charge pump or decoding circuitry sections and are therefore not directly related to array size.

FIELD RESULTS

Microchip Technology, after significant experimentation, has developed a model of the Endurance failure rates as a function of all the variables listed above. This model is available to the customer in the form of a diskette called Total Endurance™. This allows the customer to bypass confusing information and conditions other than their application and directly predict the failures seen in their application conditions within a few percent. This also allows the customer to adjust operating parameters and immediately evaluate the impact on the results of the final system. Results for a typical application (obtained from the Total Endurance model are listed at right for reference).

Device	Application Life	Cum Percent
24C02A	10 years	154 PPM
24C04A	10 years	172 PPM
93C46	10 years	136 PPM
24LC02B	10 years	108 PPM
24LC04B	10 years	131 PPM
24LC16B	10 years	668 PPM
93LC46B	10 years	374 PPM
93LC56B	10 years	108 PPM
24LC65HE	10 years	131 PPM
24LC65SE	10 years	4061 PPM

Typical conditions used are 25°C, Byte mode operation with 24 cycles per day, V_{CC} = 4.5 Volts with a random pattern writing one quarter of the array at each occasion. The failure rates quoted are the expected failure rate at the end of the application life using an unlimited number of read cycles. For more information on Endurance, it is recommended that the user obtain a copy of Total Endurance.

SECTION 11
PACKAGING INFORMATION

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PACKAGING

Commercial/Industrial Outlines and Parameters

PART NUMBER SUFFIX DESIGNATIONS:

XXXXXXXXXX - XX X/XX XXX

Examples:

27C256T - 15I/J
PIC16C54 - RCI/SO

QTP, SQTP, or ROM Code or Special Requirements

Case Outline

D = Ceramic
J = CERDIP (with window if EPROM) - all products except Microcontrollers
K = LCC (Ceramic Leadless Chip Carrier, not thermally enhanced)
L = PLCC (Plastic Leaded Chip Carrier)
P = Plastic DIP
S = Die in Waffle Pack
W = Die in Wafer Form
CB = COB (Chip-on-Board)
JN = CERDIP, no window - for Microcontrollers only
JW = CERDIP, windowed - for Microcontrollers only
PQ = Plastic Quad Flat Pack (PQFP) - Metric
SJ = Skinny CERDIP
SL = 14-Lead Small Outline 150 mil
SM = 8-Lead Small Outline 207 mil
SN = 8-Lead Small Outline 150 mil
SO = Small Outline 300 mil
SP = Skinny Plastic Carrier
SS = Shrink Small Outline Package
TS = Thin Small Outline (TSOP) 8 mm x 20 mm
VS = Very Small Outline (VSOP) 8 mm x 13.4 mm

Process Temperature

Blank = 0°C to +70°C
I = -40°C to +85°C
E = -40°C to +125°C

Speed (EPROM/High Density EEPROM)

-55 = 55 ns
-70 = 70 ns
-90 = 90 ns
-10 = 100 ns
-12 = 120 ns
-15 = 150 ns
-17 = 170 ns
-20 = 200 ns
-25 = 250 ns
-30 = 300 ns

Crystal Frequency Designator for PIC16/17 Microcontrollers

LP = Low Power Crystal
RC = Resistor Capacitor
XT = Standard Crystal/Resonator
HS = High Speed Crystal
-04 = 4 MHz
-10 = 10 MHz
-16 = 16 MHz
-20 = 20 MHz
-25 = 25 MHz

OPTION

- = twc = 1 ms
F = twc = 200 µs
X = Rotated pinout
T = Tape and Reel

Device Type (Up to 10 Digits)

C = Indicates CMOS
LC = Indicates Low Power CMOS
AA = 1.8V
LV = Low Voltage
HC = High Speed
LCS = Low Power Security

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MICROCHIP

Packaging Diagrams and Parameters

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Packaging Diagrams and Parameters

Ceramic Side Brazed Dual In-Line Family

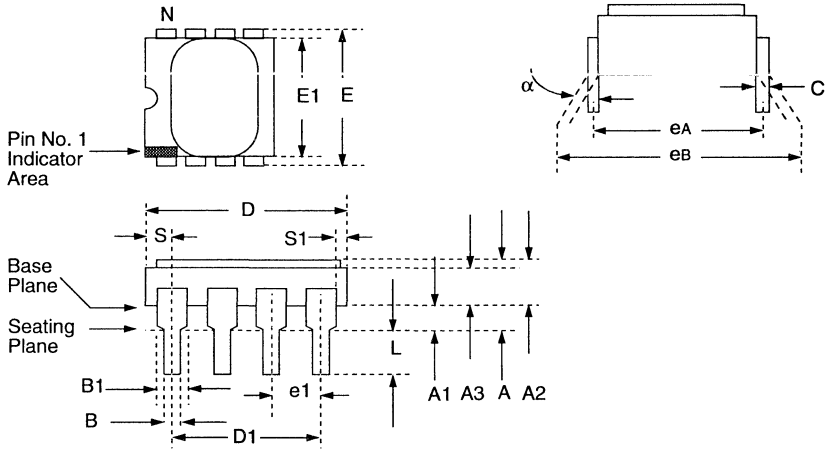
Symbol List for Ceramic Side Brazed Dual In-Line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body (lid)
A1	Distance between seating plane and base plane
A2	Distance from base plane to highest point of body (lid)
A3	Base body thickness
B	Width of terminal leads
B1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E1	Body width parameters not including leads
eA	Linear spacing of true minimum lead position center line to center line
eB	Linear spacing between true lead position outside of lead to outside of lead
e1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially usable lead positions
S	Distance from true position center line of Number 1 lead to the extremity of the body
S1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B1" is nominal.

Packaging Diagrams and Parameters

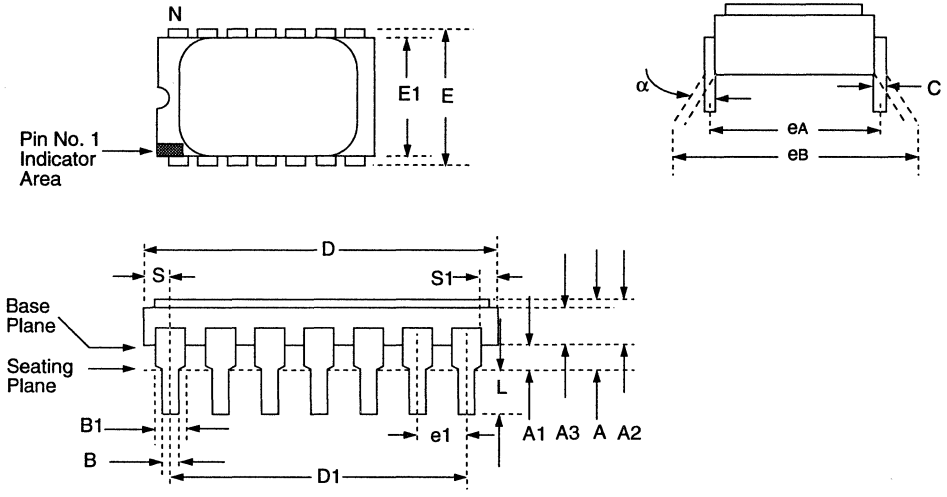
Package Type: 8-Lead Ceramic Side Brazed Dual In-Line (300 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	3.937		0.130	0.155	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.406	0.508		0.016	0.020	
B1	1.371	1.371	**Typical**	0.054	0.054	**Typical**
C	0.228	0.305	**Typical**	0.009	0.012	**Typical**
D	13.004	13.412		0.512	0.528	
D1	7.416	7.824	**Reference**	0.292	0.308	**Reference**
E	7.569	8.230		0.298	0.324	
E1	7.112	7.620		0.280	0.300	
e1	2.540	2.540	**Typical**	0.100	0.100	**Typical**
eA	7.620	7.620	**Reference**	0.300	0.300	**Reference**
eB	7.620	9.652		0.300	0.380	
L	3.302	3.810		0.130	0.150	
N	8	8		8	8	
S	2.540	3.048		0.100	0.120	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

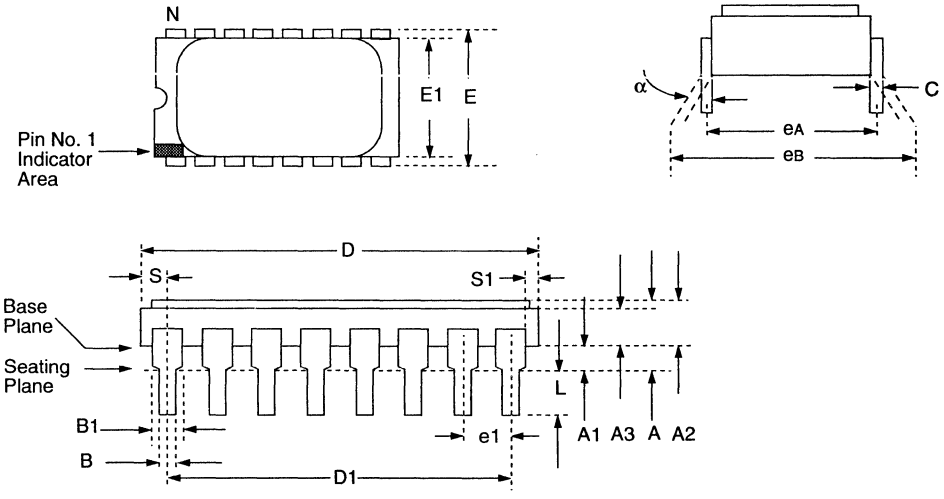
Package Type: 14-Lead Ceramic Side Brazed Dual In-line (300 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.406	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.203	0.305	Typical	0.008	0.012	Typical
D	18.796	19.228		0.740	0.757	
D1	15.036	15.444	Reference	0.592	0.608	Reference
E	7.620	8.382		0.300	0.330	
E1	7.061	7.570		0.278	0.298	
e1	2.362	2.744	Typical	0.093	0.108	Typical
eA	7.366	7.874	Reference	0.290	0.310	Reference
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	14	14		14	14	
S	–	2.490		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

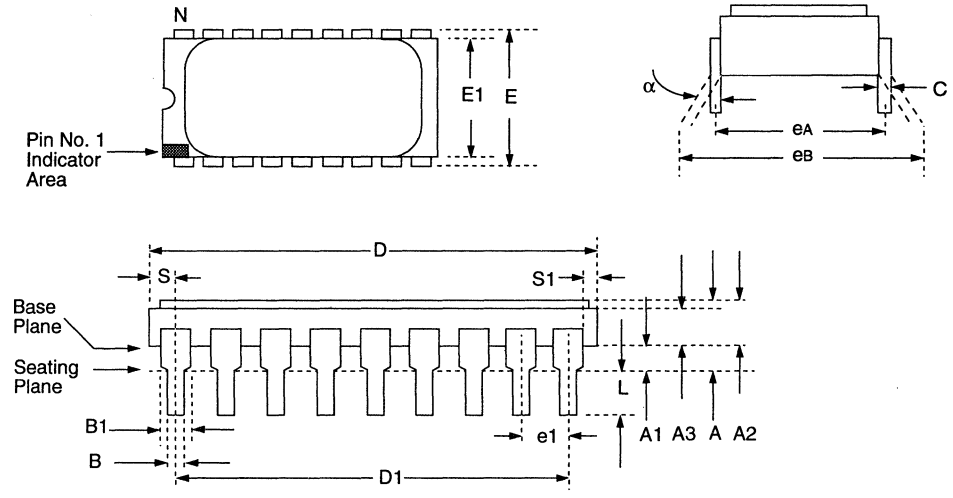
Package Type: 16-Lead Ceramic Side Brazed Dual In-line (300 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.406	0.508		0.016	0.020	
B1	1.371	1.371	Typical	0.054	0.054	Typical
C	0.228	0.305	Typical	0.009	0.012	Typical
D	19.812	20.574		0.780	0.810	
D1	17.653	17.907	Reference	0.695	0.705	Reference
E	7.620	8.382		0.300	0.330	
E1	7.162	7.470		0.282	0.294	
e1	2.413	2.667	Typical	0.095	0.105	Typical
eA	7.366	7.874	Reference	0.290	0.310	Reference
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	16	16		16	16	
S	–	2.032		–	0.080	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

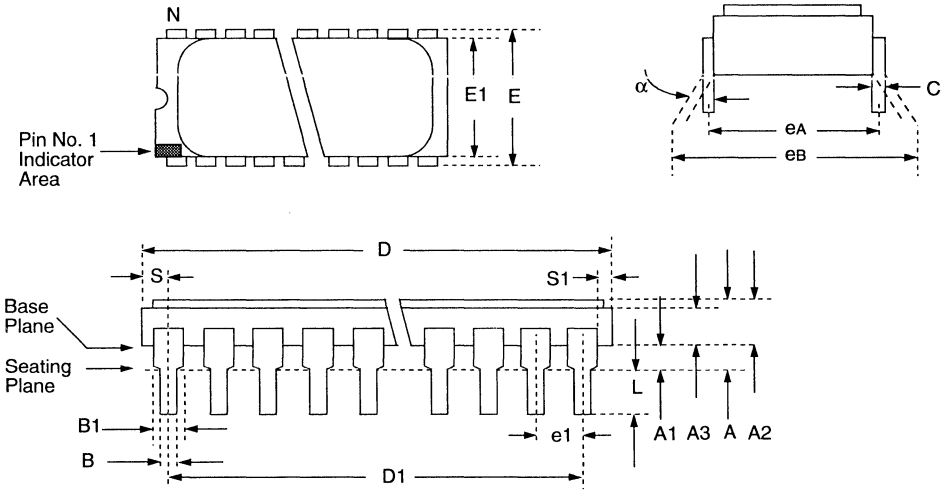
Package Type: 18-Lead Ceramic Side Brazed Dual In-line (300 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.302	4.064		0.130	0.160	
A1	0.635	1.143		0.025	0.045	
A2	2.032	2.794		0.080	0.110	
A3	1.778	2.413		0.070	0.095	
B	0.406	0.508		0.016	0.020	
B1	1.371	1.371	Typical	0.054	0.054	Typical
C	0.228	0.305	Typical	0.009	0.012	Typical
D	22.352	23.114		0.880	0.910	
D1	20.193	20.447	Reference	0.795	0.805	Reference
E	7.620	8.382		0.300	0.330	
E1	7.061	7.570		0.278	0.298	
e1	2.413	2.667	Typical	0.095	0.105	Typical
eA	7.366	7.874	Reference	0.290	0.310	Reference
eB	7.620	9.652		0.300	0.380	
L	3.175	4.191		0.125	0.165	
N	18	18		18	18	
S	–	2.490		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

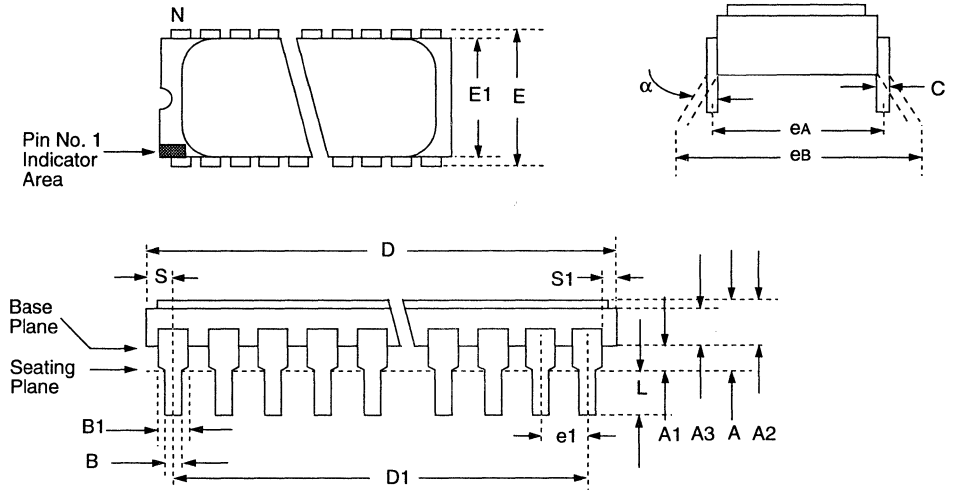
Package Type: 22-Lead Ceramic Side Brazed Dual In-line (400 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	2.667	4.064		0.105	0.160	
A1	0.711	1.220		0.028	0.048	
A2	2.032	3.302		0.080	0.130	
A3	1.778	2.921		0.070	0.115	
B	0.431	0.585		0.017	0.023	
B1	1.016	1.016	**Typical**	0.040	0.040	**Typical**
C	0.228	0.305	**Typical**	0.009	0.012	**Typical**
D	27.152	27.864		1.069	1.091	
D1	25.296	25.604	**Reference**	0.992	1.008	**Reference**
E	10.160	10.922		0.400	0.430	
E1	9.728	9.983		0.383	0.393	
e1	2.336	2.744	**Typical**	0.092	0.108	**Typical**
eA	9.906	10.414	**Reference**	0.390	0.410	**Reference**
eB	10.160	12.192		0.400	0.480	
L	3.175	4.191		0.125	0.165	
N	22	22		22	22	
S	–	2.032		–	0.080	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

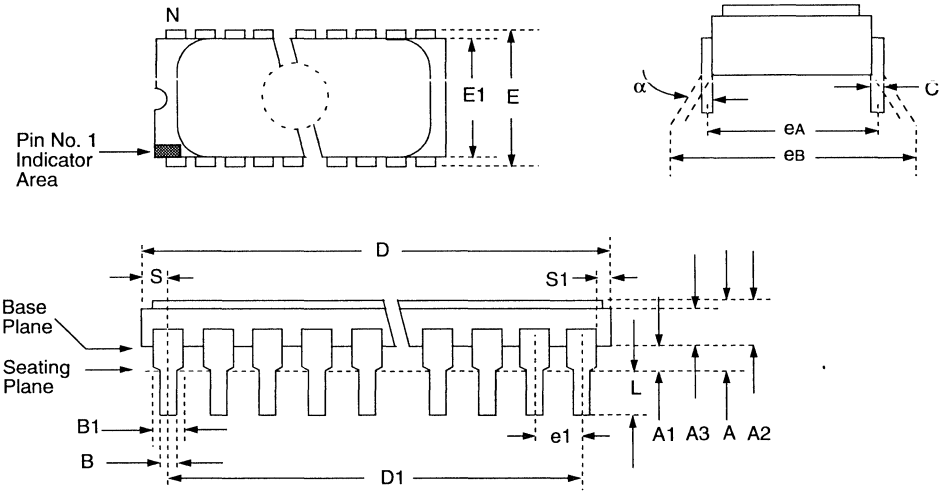
Package Type: 24-Lead Ceramic Side Brazed Dual In-line (600 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.406	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.228	0.305	Typical	0.009	0.012	Typical
D	30.175	30.745	*	1.188	1.212	
D1	27.736	28.144	Reference	1.092	1.108	Reference
E	14.986	16.002		0.590	0.630	
E1	14.782	14.936		0.582	0.588	
e1	2.336	2.744	Typical	0.092	0.108	Typical
eA	14.986	15.748	Reference	0.590	0.620	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	24	24		24	24	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

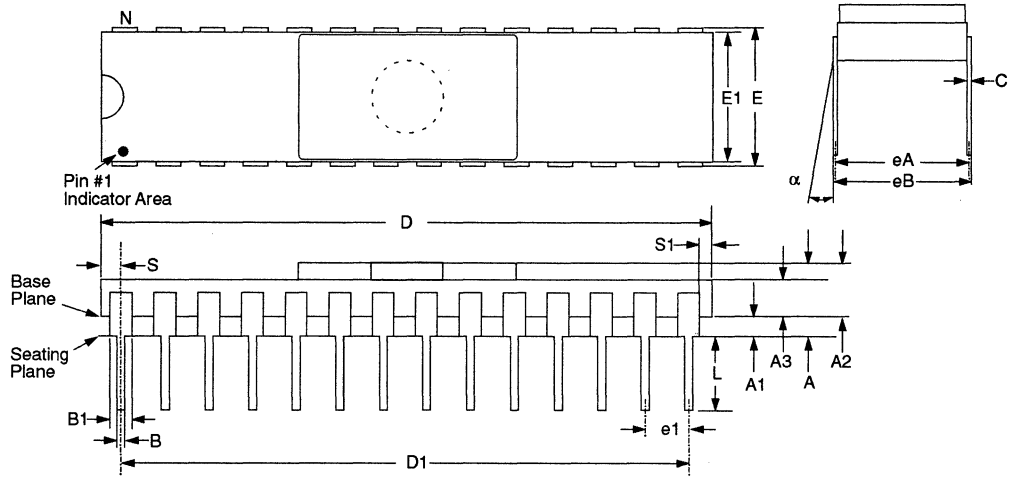
Package Type: 24-Lead Ceramic Side Brazed Dual In-line with Window (600 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.406	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.228	0.305	Typical	0.009	0.012	Typical
D	30.175	30.785		1.188	1.212	
D1	27.736	28.144	Reference	1.092	1.108	Reference
E	14.986	16.002		0.590	0.630	
E1	14.782	14.936		0.582	0.588	
e1	2.336	2.744	Typical	0.092	0.108	Typical
eA	14.986	15.748	Reference	0.590	0.620	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	24	24		24	24	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

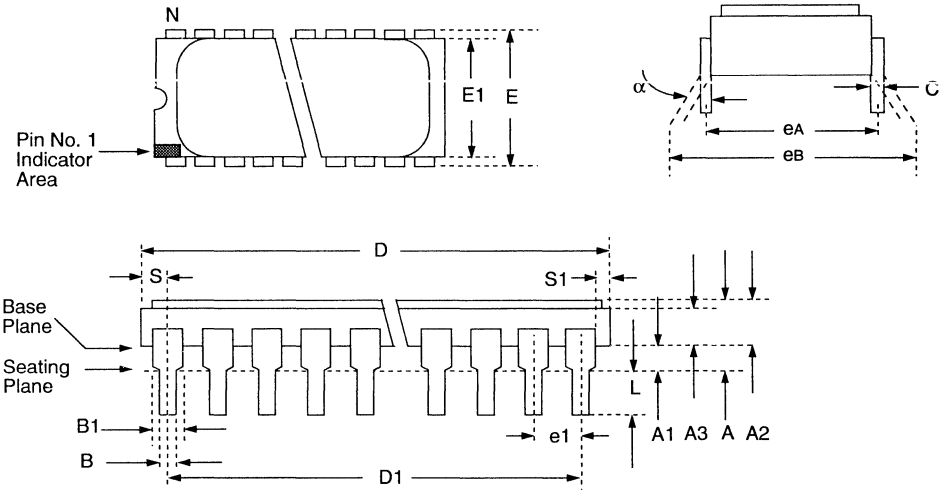
Package Type: 28-Lead Ceramic Side Brazed Dual In-Line with Window (300 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.937	5.030		0.155	0.198	
A1	1.016	1.524		0.040	0.060	
A2	2.921	3.506		0.115	0.138	
A3	1.930	2.388		0.076	0.094	
B	0.406	0.508		0.016	0.020	
B1	1.219	1.321	Typical	0.048	0.052	
C	0.228	0.305	Typical	0.009	0.012	
D	35.204	35.916		1.386	1.414	
D1	32.893	33.147	Reference	1.295	1.305	
E	7.620	8.128		0.300	0.320	
E1	7.366	7.620		0.290	0.300	
e1	2.413	2.667	Typical	0.095	0.105	
eA	7.366	7.874	Reference	0.290	0.310	
eB	7.594	8.179		0.299	0.322	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	1.143	1.397		0.045	0.055	
S1	0.533	0.737		0.021	0.029	

Packaging Diagrams and Parameters

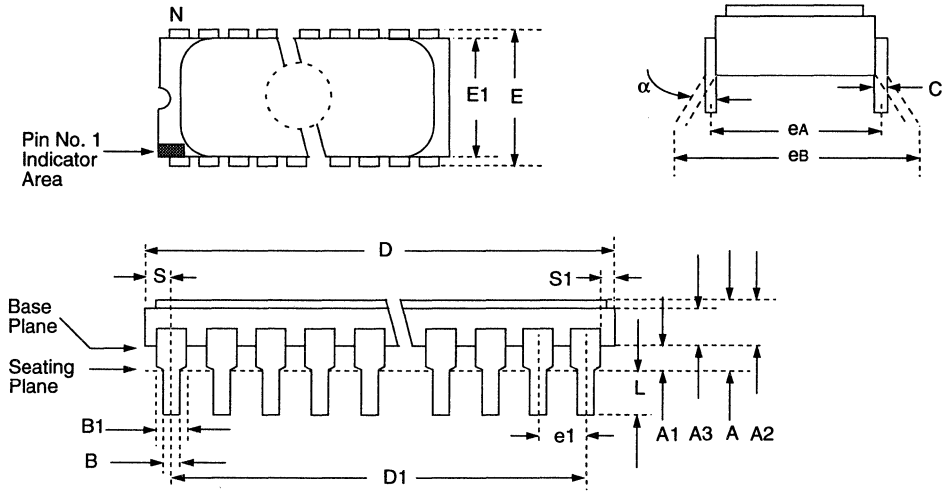
Package Type: 28-Lead Ceramic Side Brazed Dual In-line (600 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.064		0.120	0.160	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.457	0.508		0.018	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.228	0.305	**Typical**	0.009	0.012	**Typical**
D	35.204	35.916		1.386	1.414	
D1	32.816	33.224	**Reference**	1.292	1.308	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.782	15.190		0.582	0.598	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	14.986	15.494	**Reference**	0.590	0.610	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

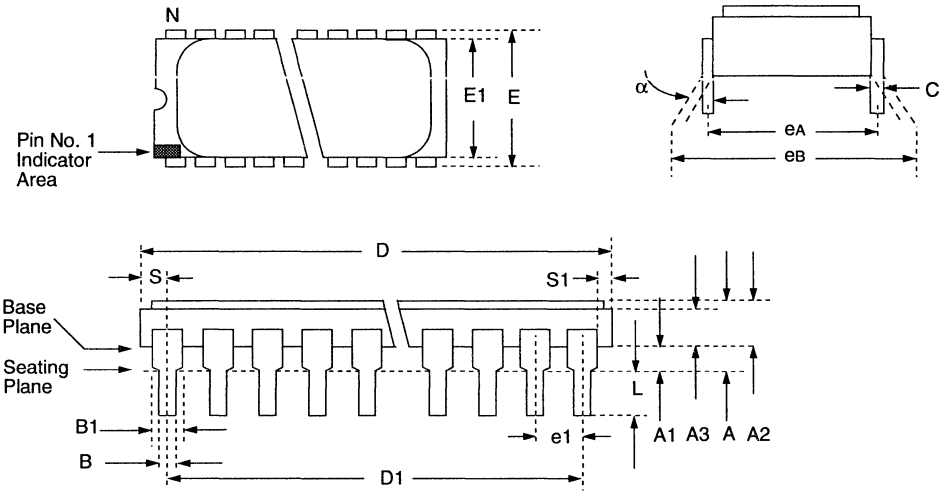
Package Type: 28-Lead Ceramic Side Brazed Dual In-line with Window (600 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.064		0.120	0.160	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.778	2.540		0.070	0.100	
B	0.457	0.508		0.018	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.228	0.305	**Typical**	0.009	0.012	**Typical**
D	35.204	35.916		1.386	1.414	
D1	32.816	33.224	**Reference**	1.292	1.308	**Reference**
E	14.986	16.002		0.590	0.630	
E1	14.782	15.190		0.582	0.598	
e1	2.489	2.591	**Typical**	0.098	0.102	**Typical**
eA	14.986	15.494	**Reference**	0.590	0.610	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	28	28		28	28	
S	–	2.540		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

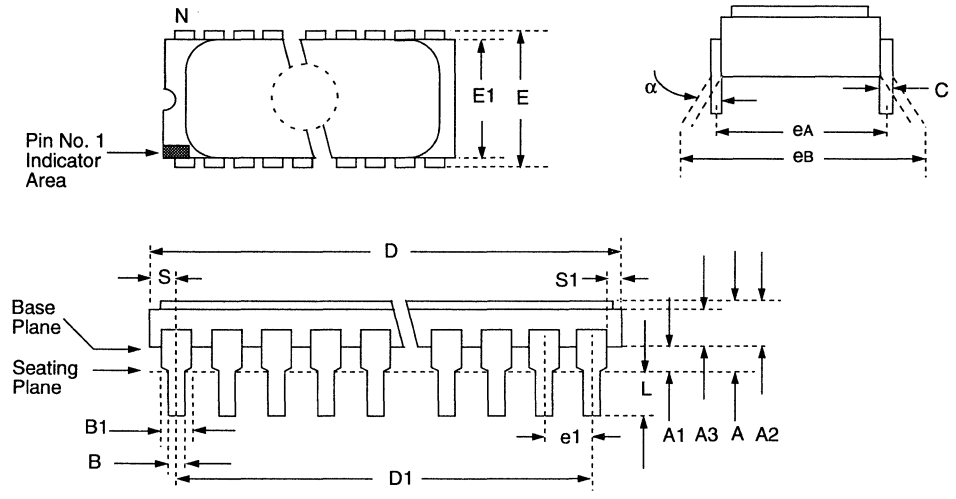
Package Type: 40-Lead Ceramic Side Brazed Dual In-line (600 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		0.072	0.088	
B	0.406	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.228	0.305	**Typical**	0.009	0.012	**Typical**
D	50.546	51.308		1.990	2.020	
D1	48.056	48.463	**Reference**	1.892	1.908	**Reference**
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.336	2.744	**Typical**	0.092	0.108	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	40	40		40	40	
S	–	2.490		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

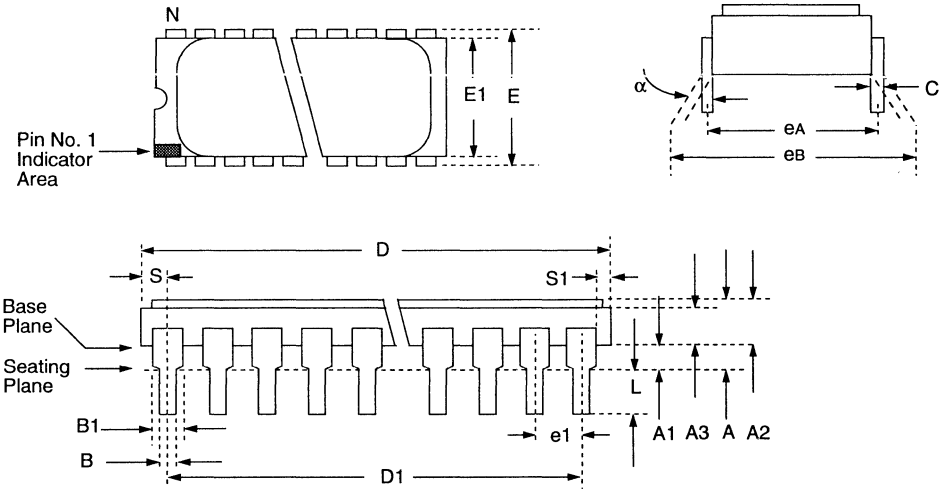
Package Type: 40-Lead Ceramic Side Brazed Dual In-line with Window (600 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		0.072	0.088	
B	0.406	0.508		0.016	0.020	
B1	1.270	1.270	**Typical**	0.050	0.050	**Typical**
C	0.228	0.305	**Typical**	0.009	0.012	**Typical**
D	50.546	51.308		1.990	2.020	
D1	48.056	48.463	**Reference**	1.892	1.908	**Reference**
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.336	2.744	**Typical**	0.092	0.108	**Typical**
eA	15.240	15.240	**Reference**	0.600	0.600	**Reference**
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	40	40		40	40	
S	–	2.490		–	0.098	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Package Type: 48-Lead Ceramic Side Brazed Dual In-line (600 mil)



Package Group: Ceramic Side Brazed Dual In-Line (CER)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.048	4.445		0.120	0.175	
A1	1.016	1.524		0.040	0.060	
A2	2.032	2.921		0.080	0.115	
A3	1.829	2.235		0.072	0.088	
B	0.406	0.508		0.016	0.020	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.228	0.305	Typical	0.009	0.012	Typical
D	60.350	61.570		2.376	2.424	
D1	58.216	58.624	Reference	2.292	2.308	Reference
E	15.240	16.256		0.600	0.640	
E1	14.478	15.748		0.570	0.620	
e1	2.336	2.744	Typical	0.092	0.108	Typical
eA	15.240	15.290	Reference	0.600	0.600	Reference
eB	14.986	16.256		0.590	0.640	
L	3.302	4.064		0.130	0.160	
N	48	48		48	48	
S	–	2.490		–	0.100	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

Ceramic CERDIP Dual In-Line Family

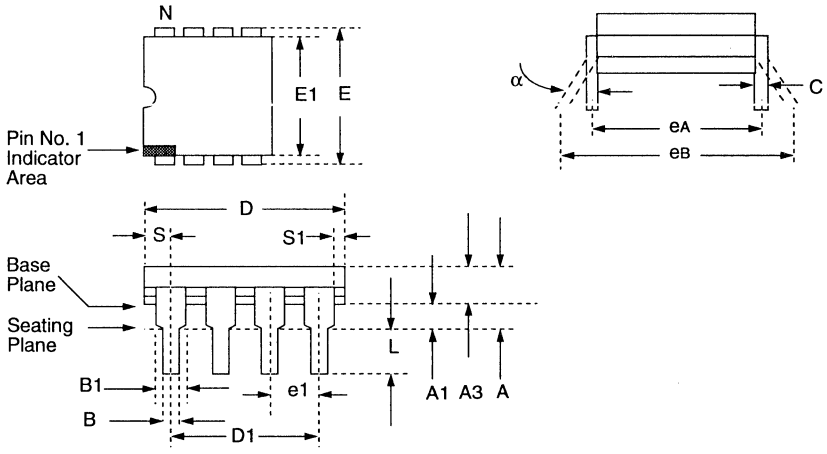
Symbol List for Ceramic CERDIP Dual In-Line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body (lid)
A1	Distance between seating plane and base plane
A2	Distance from base plane to highest point of body (lid)
A3	Base body thickness
B	Width of terminal leads
B1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E1	Body width parameters not including leads
eA	Linear spacing of true minimum lead position center line to center line
eB	Linear spacing between true lead position outside of lead to outside of lead
e1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially usable lead positions
S	Distance from true position center line of Number 1 lead to the extremity of the body
S1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B1" is nominal.

Packaging Diagrams and Parameters

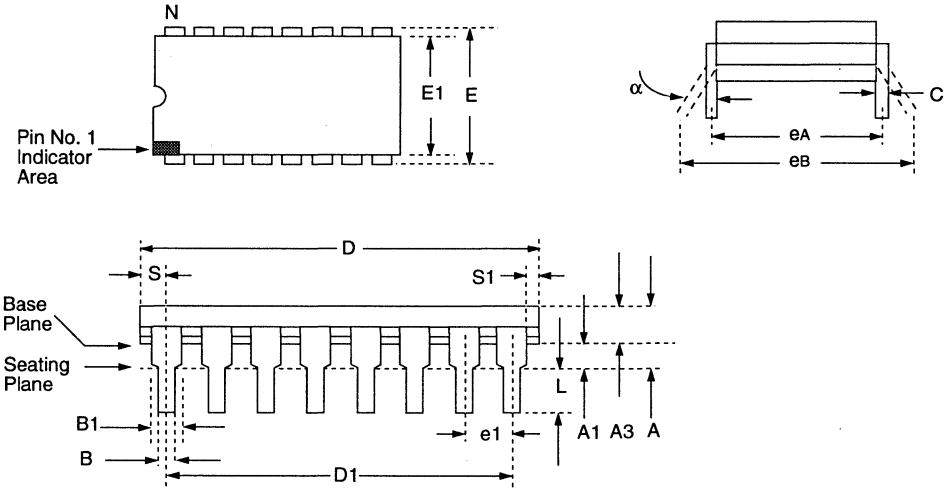
Package Type: 8-Lead Ceramic CERDIP Dual In-line (300 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	9.398	10.287		0.370	0.405	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	7.620	8.255		0.300	0.325	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Reference	0.290	0.320	Reference
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	8	8		8	8	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

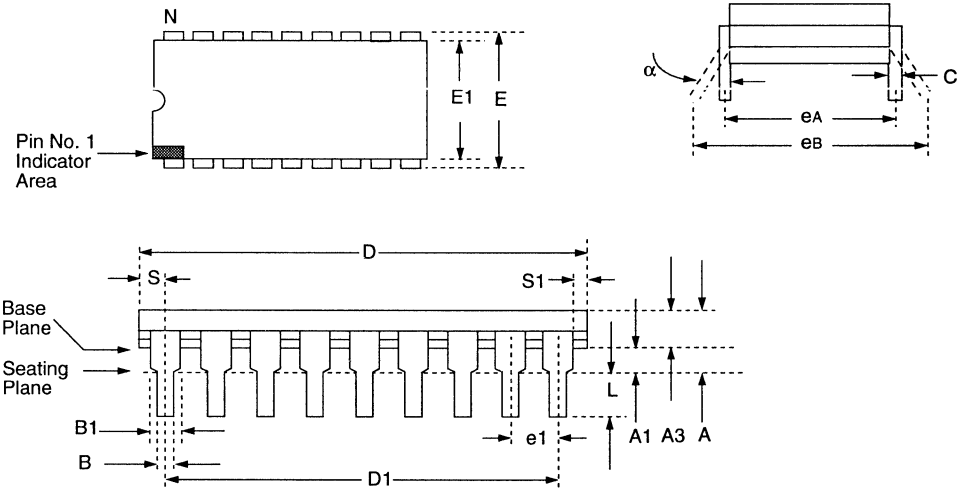
Package Type: 16-Lead Ceramic CERDIP Dual In-line (300 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.191	5.080		0.165	0.200	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	19.050	20.320		0.750	0.800	
D1	17.780	17.780	Reference	0.700	0.700	Reference
E	7.493	8.255		0.295	0.325	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.366	8.128	Reference	0.290	0.320	Reference
eB	7.62	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	16	16		16	16	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

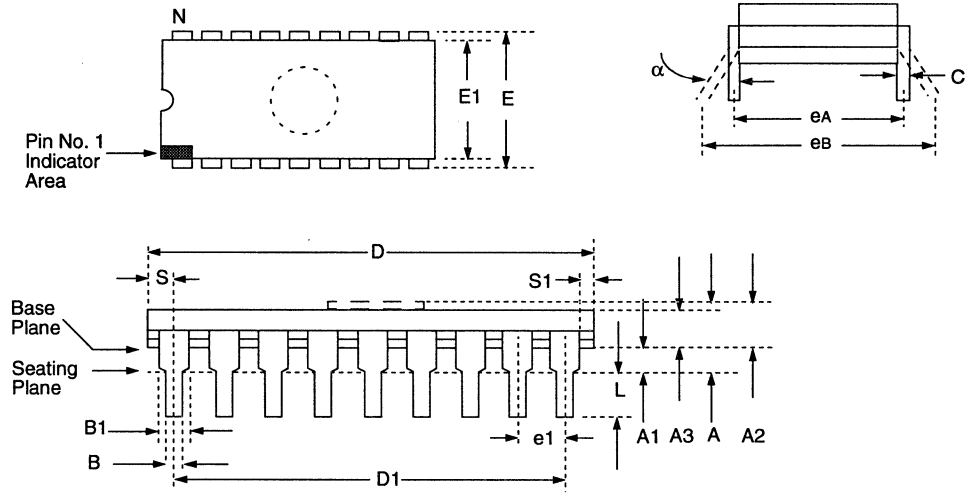
Package Type: 18-Lead Ceramic CERDIP Dual In-line (300 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.778		0.015	0.070	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540		0.100	0.100	
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.620	10.160	Reference	0.300	0.400	Reference
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

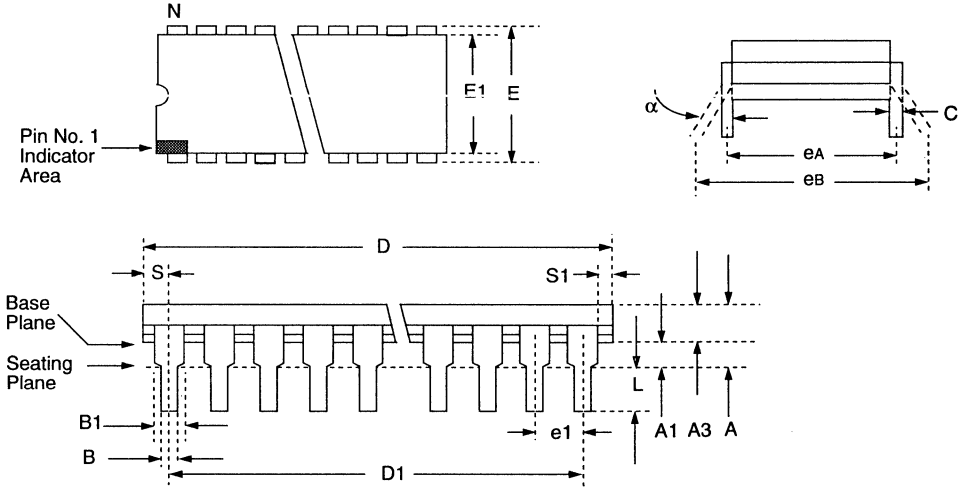
Package Type: 18-Lead Ceramic CERDIP Dual In-line with Window (300 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.080		—	0.200	
A1	0.381	1.7780		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.352	23.622		0.880	0.930	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.620	10.160		0.300	0.400	
L	3.175	3.810		0.125	0.150	
N	18	18		18	18	
S	0.508	1.397		0.020	0.055	
S1	0.381	1.270		0.015	0.050	

Packaging Diagrams and Parameters

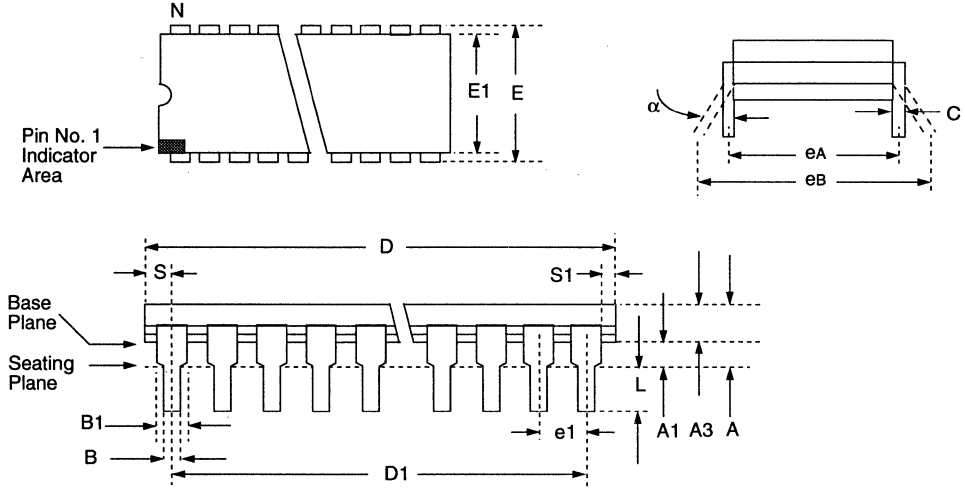
Package Type: 22-Lead Ceramic CERDIP Dual In-line (400 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.778		0.015	0.070	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	26.670	27.940		1.050	1.100	
D1	25.400	25.400	Reference	1.000	1.000	Reference
E	10.160	10.922		0.400	0.430	
E1	8.890	10.414		0.350	0.410	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	9.906	10.668	Typical	0.390	0.420	Typical
eB	10.160	12.700		0.400	0.500	
L	3.175	3.810		0.125	0.150	
N	18	18		22	22	
S	—	1.270		—	0.050	
S1	0.127	1.270		0.005	0.050	

Packaging Diagrams and Parameters

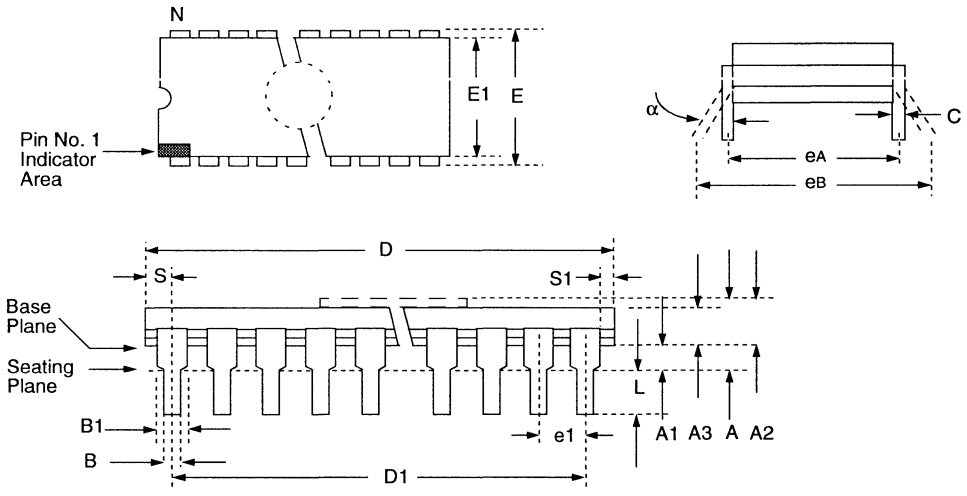
Package Type: 24-Lead Ceramic CERDIP Dual In-line (300 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.620	11.430		0.300	0.450	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

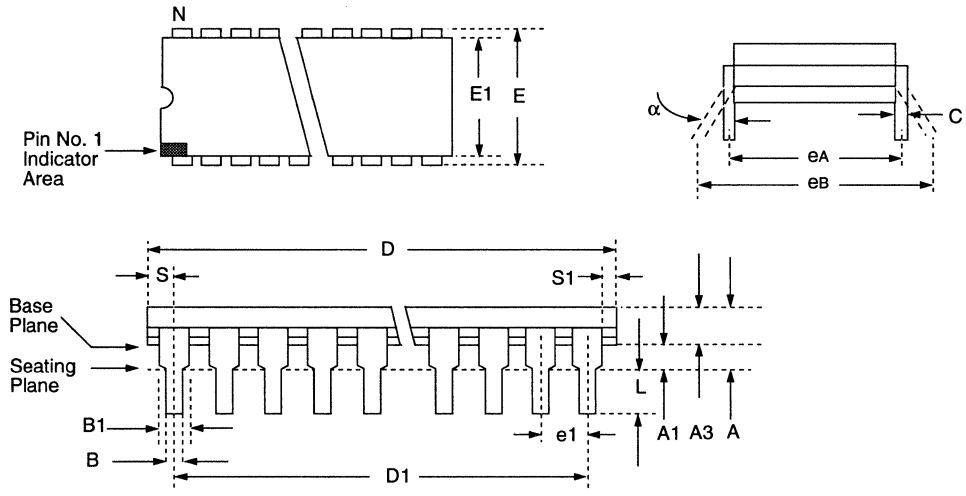
Package Type: 24-Lead Ceramic CERDIP Dual In-line with Window (300 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.382		0.300	0.330	
E1	5.588	7.874		0.220	0.310	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	7.366	8.128	Typical	0.290	0.320	Typical
eB	7.620	11.430		0.300	0.450	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

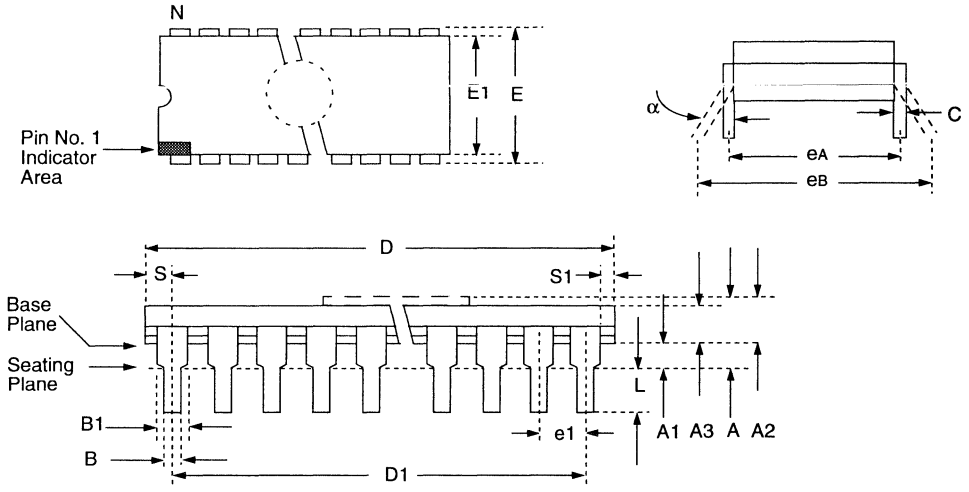
Package Type: 24-Lead Ceramic CERDIP Dual In-line (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	15.748	Typical	0.590	0.620	Typical
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

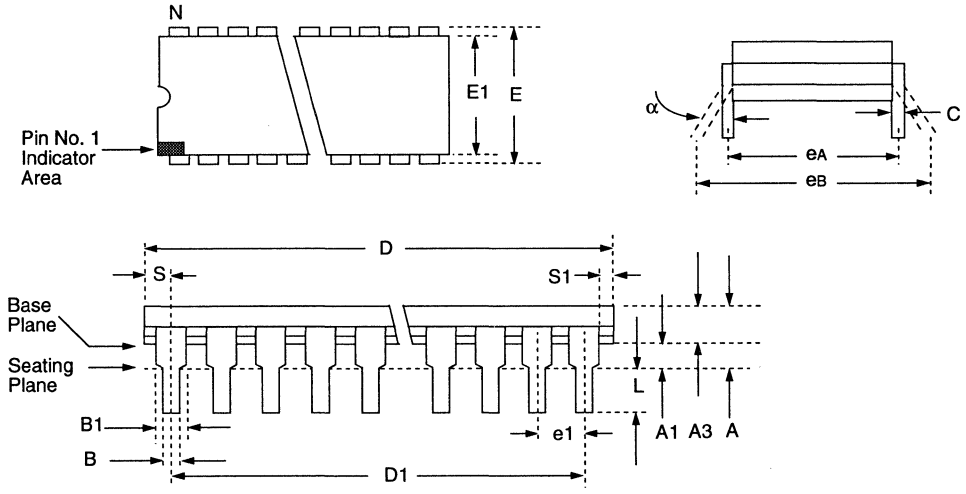
Package Type: 24-Lead Ceramic CERDIP Dual In-line with Window (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.715		—	0.225	
A1	0.381	1.905		0.015	0.075	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	**Typical**	0.050	0.065	**Typical**
C	0.203	0.381	**Typical**	0.008	0.015	**Typical**
D	31.115	32.385		1.225	1.275	
D1	27.940	27.940	**Reference**	1.100	1.100	**Reference**
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	**Reference**	0.100	0.100	**Reference**
eA	14.986	15.748	**Typical**	0.590	0.620	**Typical**
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	24	24		24	24	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

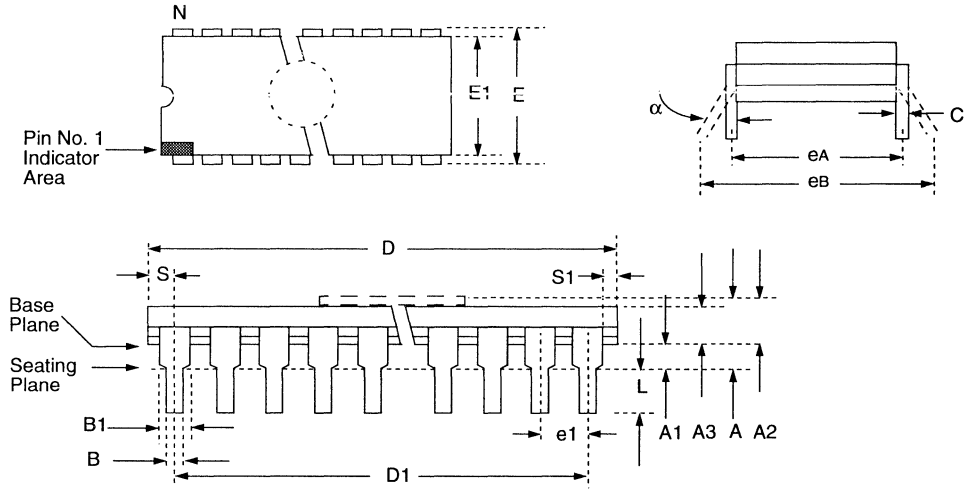
Package Type: 28-Lead Ceramic CERDIP Dual In-line (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	—	—	Ref. A3	—	—	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	36.195	37.465		1.425	1.475	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	15.748	Typical	0.590	0.620	Typical
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	28	28		28	28	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

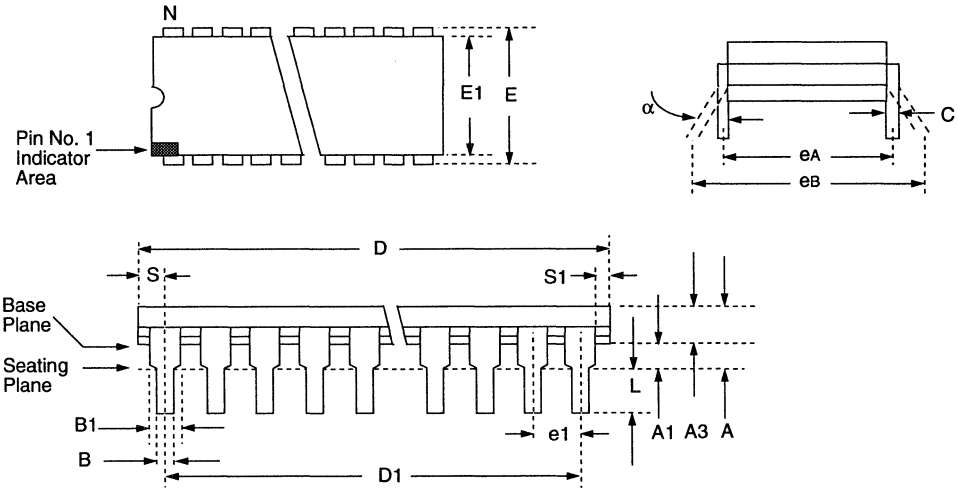
Package Type: 28-Lead Ceramic CERDIP Dual In-line with Window (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	5.461		—	0.215	
A1	0.381	1.524		0.015	0.060	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	36.195	37.465		1.425	1.475	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	15.748	Reference	0.590	0.620	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	28	28		28	28	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

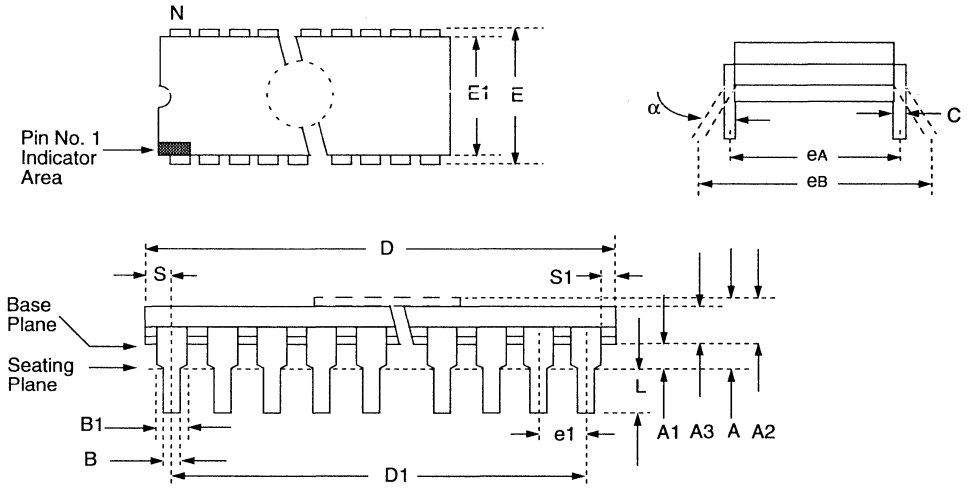
Package Type: 40-Lead Ceramic CERDIP Dual In-line (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	–	–	Ref. A3	–	–	Ref. A3
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	14.986	16.002	Reference	0.590	0.630	Reference
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Package Type: 40-Lead Ceramic CERDIP Dual In-line with Window (600 mil)



Package Group: Ceramic CERDIP Dual In-Line (CDP)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	4.318	5.715		0.170	0.225	
A1	0.381	1.778		0.015	0.070	
A2	3.810	4.699		0.150	0.185	
A3	3.810	4.445		0.150	0.175	
B	0.355	0.585		0.014	0.023	
B1	1.270	1.651	Typical	0.050	0.065	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.435	52.705		2.025	2.075	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	12.954	15.240		0.510	0.600	
e1	2.540	2.540	Reference	0.100	0.100	Reference
eA	14.986	16.002	Typical	0.590	0.630	Typical
eB	15.240	18.034		0.600	0.710	
L	3.175	3.810		0.125	0.150	
N	40	40		40	40	
S	1.016	2.286		0.040	0.090	
S1	0.381	1.778		0.015	0.070	

Packaging Diagrams and Parameters

Ceramic Flatpack Family

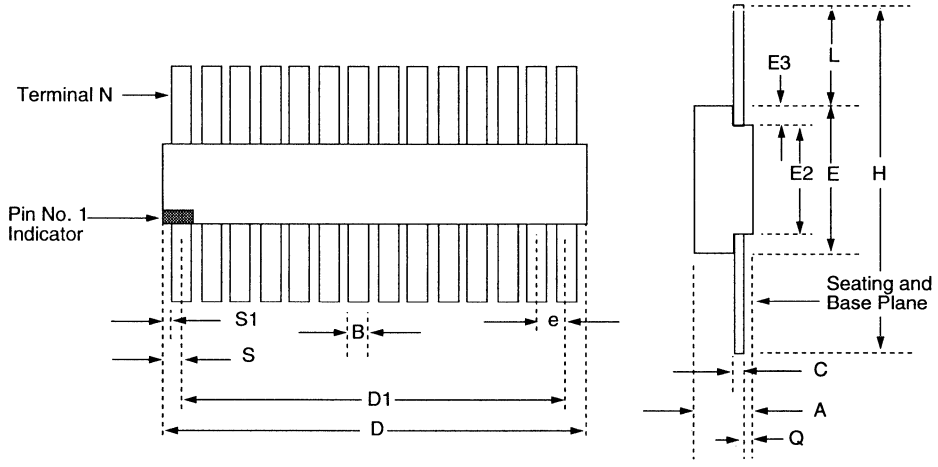
Symbol List for Ceramic Flatpack Package Parameters	
Symbol	**Description of Parameters**
A	Distance between seating plane to highest point of body (lid)
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package parameter of length
D1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E2, E3	Body width parameters not including leads
e	Linear spacing between center lines of body standoffs (terminal leads)
H	Other package width parameter
L	Distance from seating plane to end of lead
N	Total number of potentially usable lead positions
Q	Distance between seating plane and lead
S	Distance from true position center line of Number 1 lead to the extremity of the body
S1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameters "B" and "C" are nominal.

Packaging Diagrams and Parameters

Package Type: 28-Lead Ceramic Flatpack



Package Group: Ceramic Flatpack (CFPK)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.286	3.302		0.090	0.130	
B	0.381	0.482		0.015	0.019	**Typical**
C	0.076	0.153		0.003	0.006	**Typical**
D	17.780	18.796		0.700	0.740	
D1	16.306	16.714		0.642	0.658	**Reference**
E	9.652	10.668		0.380	0.420	
E2	4.572	–		0.180	–	
E3	0.762	–		0.030	–	
e	1.270	1.270	**BSC**	0.050	0.050	**Typical**
H	22.352	29.464		0.880	1.160	
L	6.350	9.398		0.250	0.370	
N	28	28		28	28	
Q	0.660	1.143		0.026	0.045	
S	0.889	1.016		0.035	0.040	
S1	0.254	0.381		0.010	0.015	

Packaging Diagrams and Parameters

Ceramic Leadless Chip Carrier Family

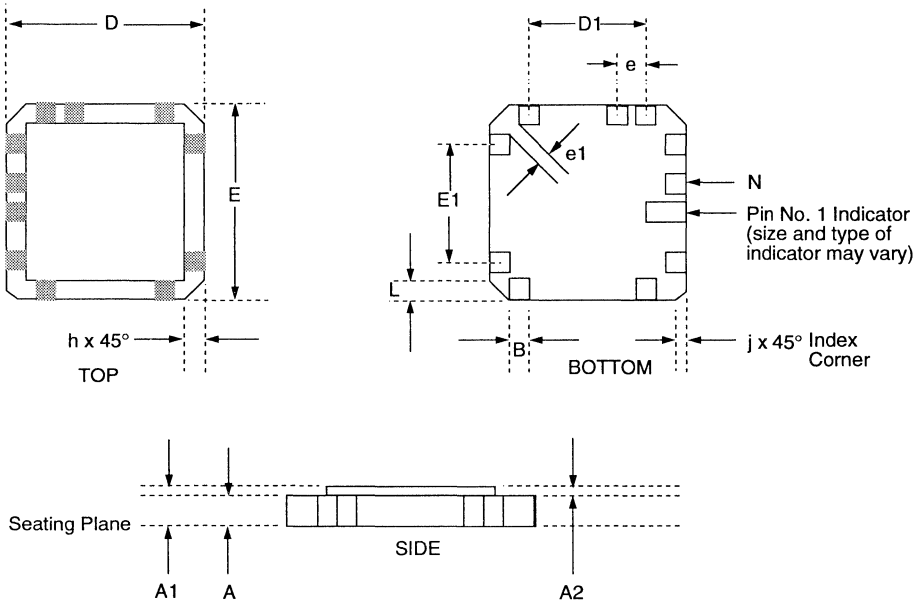
Symbol List for Ceramic Leadless Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Thickness of base body
A1	Total package height
A2	Distance from base body to highest point of body (lid)
B	Width of terminal lead pin
D	Largest overall package parameter of length
D1, E1	Body length dimension - end lead center to end lead center
E	Largest overall package dimension of width
e	Linear spacing
e1	Linear spacing between edges of true lead positions (of corner terminal lead pads) lead corner to lead corner
h	Depth of major index feature
j	Width of minor index feature
L	Distance from package edge to end of effective pad
N	Total number of potentially usable lead positions

Notes:

1. Controlling dimension: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by PC board hole size.
4. Parameter "B" is nominal.
5. Corner configuration optional.

Packaging Diagrams and Parameters

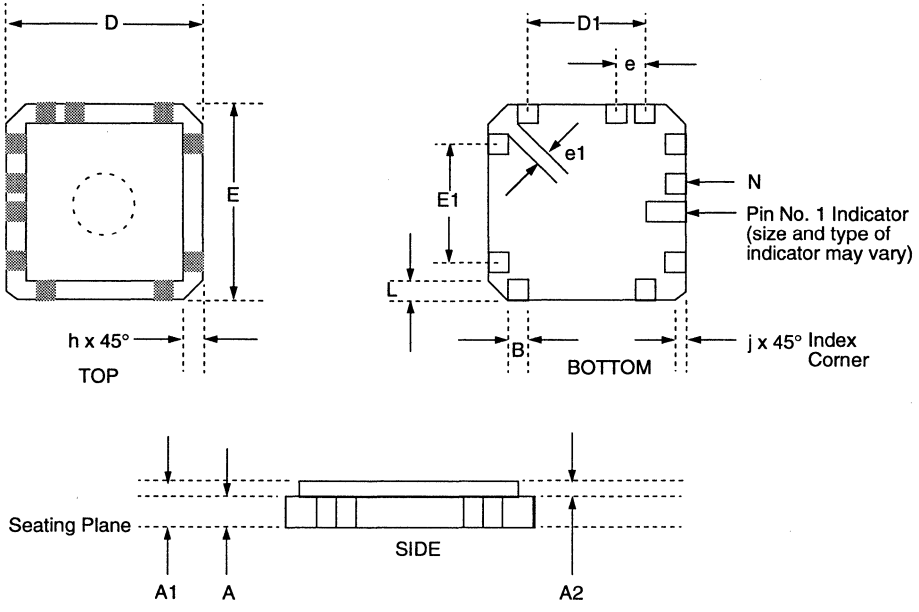
Package Type: 28-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	1.651	2.540		0.065	0.100	
A2	0.254	0.381		0.010	0.015	
B	0.558	0.712	Typical	0.022	0.028	Typical
D	11.226	11.684		0.442	0.460	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.226	11.684		0.442	0.460	
E1	7.620	7.620	Typical	0.300	0.300	Typical
e	1.270	1.270	Reference	0.050	0.050	Reference
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	28	28		28	28	

Packaging Diagrams and Parameters

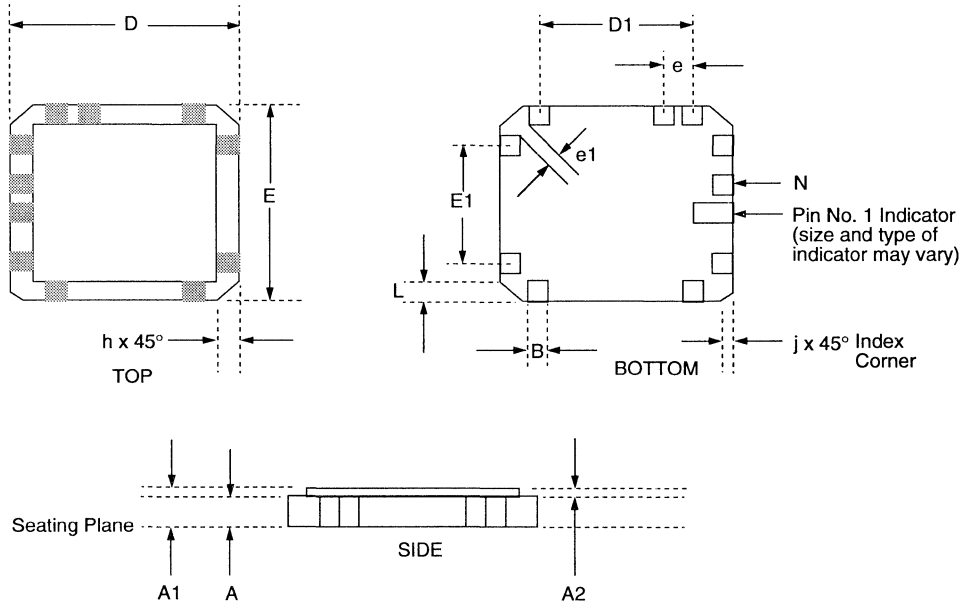
Package Type: 28-Lead Ceramic Leadless Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	2.540		0.090	0.100	
A2	0.889	1.143		0.035	0.045	
B	0.558	0.712	Typical	0.022	0.028	Typical
D	11.226	11.684		0.442	0.460	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.226	11.684		0.442	0.460	
E1	7.620	7.620	Reference	0.300	0.300	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	28	28		28	28	

Packaging Diagrams and Parameters

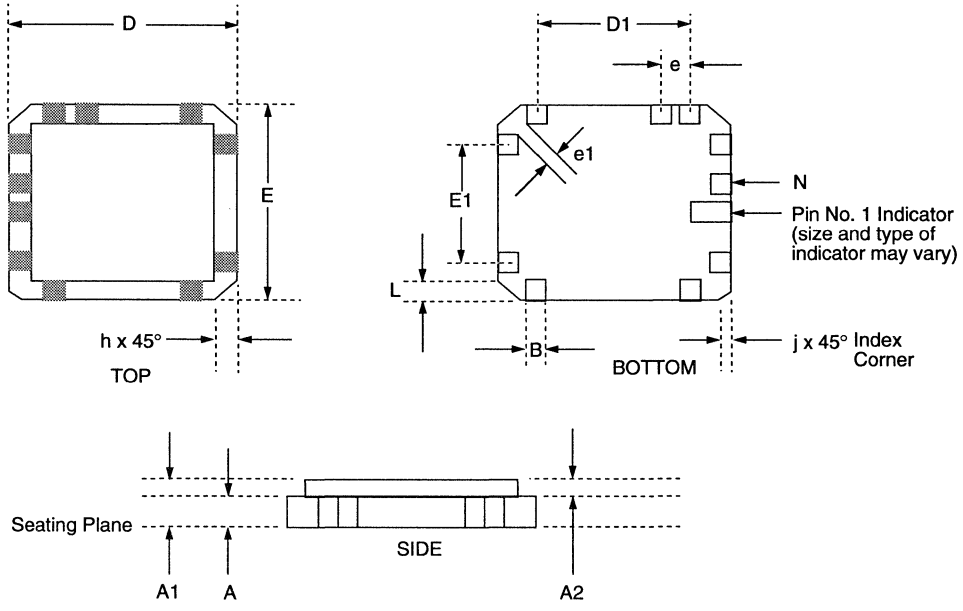
Package Type: 32-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.540	3.048		0.100	0.120	
A2	0.254	0.381		0.010	0.015	
B	0.635	0.661	Typical	0.025	0.026	Typical
D	13.716	14.224		0.540	0.560	
D1	9.982	10.338	Reference	0.393	0.407	Reference
E	11.226	11.634		0.442	0.458	
E1	7.442	7.798	Reference	0.293	0.307	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

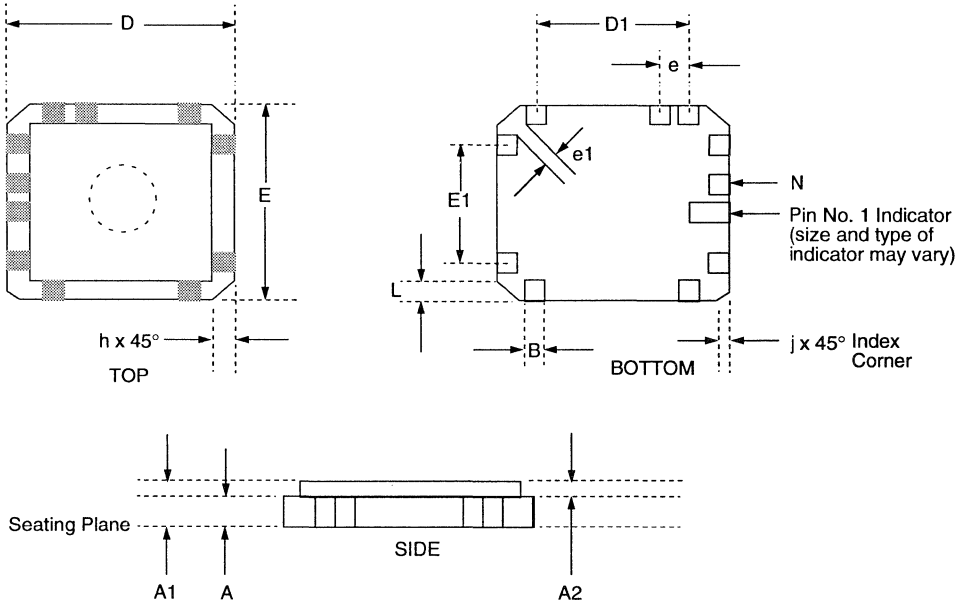
Package Type: 32-Lead Ceramic Leadless Chip Carrier - FRIT



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.635	1.143		0.025	0.045	
B	0.558	0.712	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.226	11.634		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Reference	0.050	0.050	Reference
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

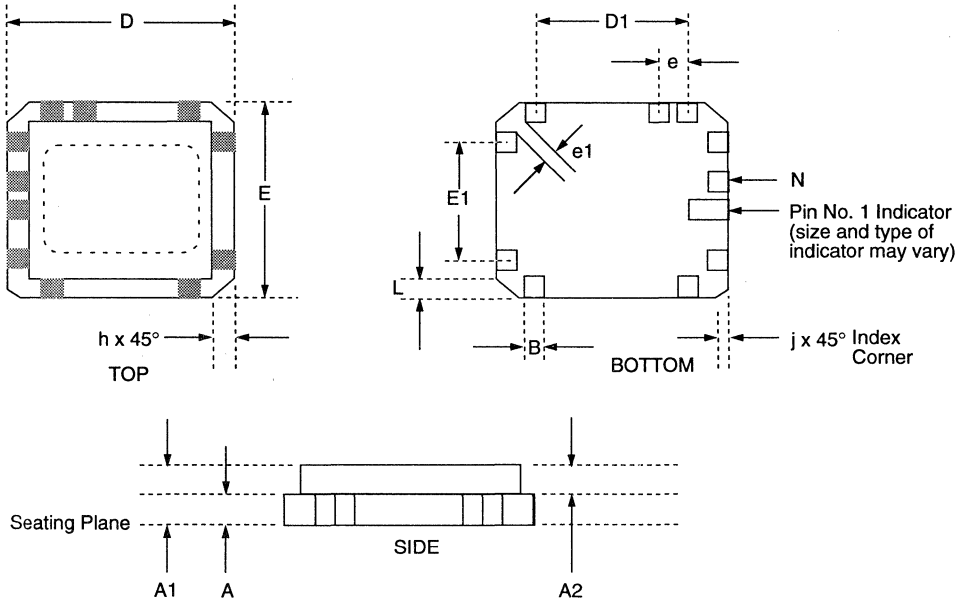
Package Type: 32-Lead Ceramic Leadless Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.889	1.143		0.035	0.045	
B	0.558	0.712	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.226	11.634		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Reference	0.050	0.050	Reference
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

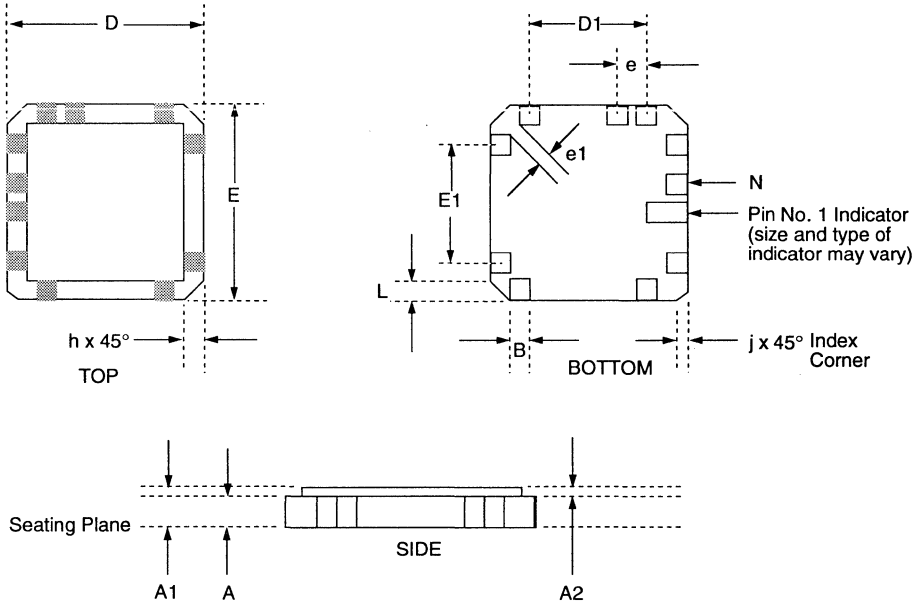
Package Type: 32-Lead Ceramic Leadless FRIT-Seal Chip Carrier with Window



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.397	2.159		0.055	0.085	
A1	2.286	3.302		0.090	0.130	
A2	0.889	1.143		0.035	0.045	
B	0.558	0.712	Typical	0.022	0.028	Typical
D	13.716	14.224		0.540	0.560	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	11.226	11.634		0.442	0.458	
E1	10.160	10.160	Reference	0.400	0.400	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	32	32		32	32	

Packaging Diagrams and Parameters

Package Type: 44-Lead Ceramic Leadless Chip Carrier



Package Group: Ceramic Leadless Chip Carrier (LCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.371	2.083		0.054	0.082	
A1	1.778	3.048		0.070	0.120	
A2	0.254	1.143		0.010	0.045	
B	0.584	0.712	Typical	0.023	0.028	Typical
D	16.256	16.815		0.640	0.662	
D1	12.700	12.700	Reference	0.500	0.500	Reference
E	16.256	16.815		0.640	0.662	
E1	12.700	12.700	Reference	0.500	0.500	Reference
e	1.270	1.270	Typical	0.050	0.050	Typical
e1	0.381	–	Typical	0.015	–	Typical
h	1.016	1.016	Reference	0.040	0.040	Reference
j	0.508	0.508	Reference	0.020	0.020	Reference
L	1.143	1.397	Typical	0.045	0.055	Typical
N	44	44		44	44	

Packaging Diagrams and Parameters

Ceramic Leaded Chip Carrier Family

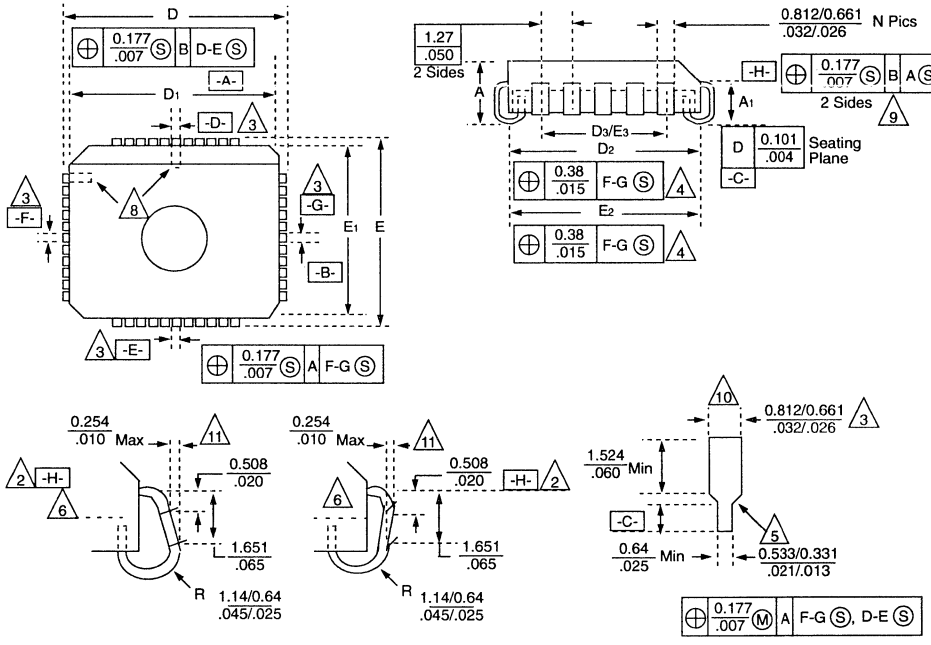
Symbol List for Ceramic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance between seating plane to highest point of body
A1	Distance from lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D1/E1	Body dimension
D2/E2	Footprint
D3/E3	Footprint
LT	Lead thickness
N	Total number of potentially usable lead positions
Nd	Total number of leads on short side (rectangular)
Ne	Total number of leads on long side (rectangular)

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane -H- located at top of parting line and coincident with top of lead. Where lead exits body.
3. Datums D-E and F-G to be determined where center leads exit body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Transition is optional.
6. Square: Details of pin1 identifier are optional but must be located within one of the two zones indicated. If the number of terminals on a side is odd terminal 1 is the center terminal.
   Rectangle: Details of pin1 are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.
7. Location to datums -A- and -B- to be determined at plane -H-.
8. All dimensions and tolerances include lead trim offset and lead finish.
9. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
10. Controlling dimension: inches.

Packaging Diagrams and Parameters

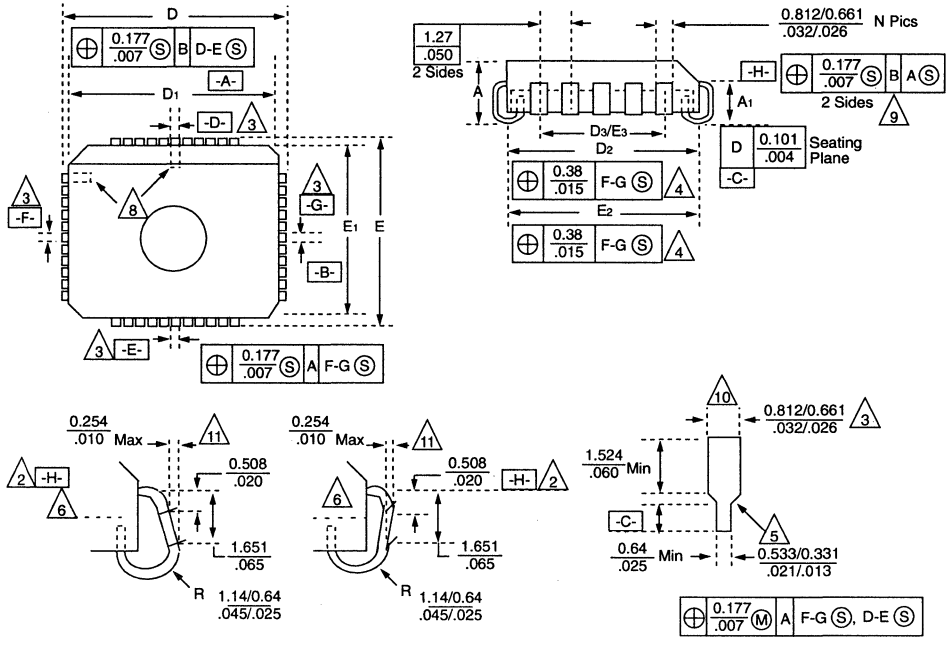
Package Type: 68-Lead Ceramic Leaded Chip Carrier (Window)



Package Group: Ceramic Leaded Chip Carrier (CLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		0.165	0.185	
A1	2.286	3.048		0.090	0.120	
D	24.968	25.222		0.983	0.993	
D1	23.977	24.333		0.944	0.958	
D2	22.860	23.876		0.900	0.940	
D3	20.320	-	Reference	0.800	-	Reference
E	24.968	25.222		0.983	0.993	
E1	23.977	24.333		0.944	0.958	
E2	22.860	23.876		0.900	0.940	
E3	20.320	-	Reference	0.800	-	Reference
N	68	-		68	-	
CP	-	0.102		-	0.004	
LT	0.152	0.204		0.006	0.008	

Packaging Diagrams and Parameters

Package Type: 84-Lead Ceramic Leaded Chip Carrier (Window)



Package Group: Ceramic Leaded Chip Carrier (CLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		0.165	0.185	
A1	2.286	3.048		0.090	0.120	
D	30.048	30.353		1.183	1.195	
D1	28.829	29.591		1.135	1.165	
D2	27.940	28.956		1.100	1.140	
D3	25.400	-	Reference	1.000	-	Reference
E	30.048	30.353		1.183	1.195	
E1	28.829	29.591		1.135	1.165	
E2	27.940	28.956		1.100	1.140	
E3	25.400	-	Reference	1.000	-	Reference
N	84	-		84	-	
CP	-	0.102		-	0.004	
LT	0.152	0.204		0.006	0.008	

Packaging Diagrams and Parameters

Plastic Dual In-Line Family

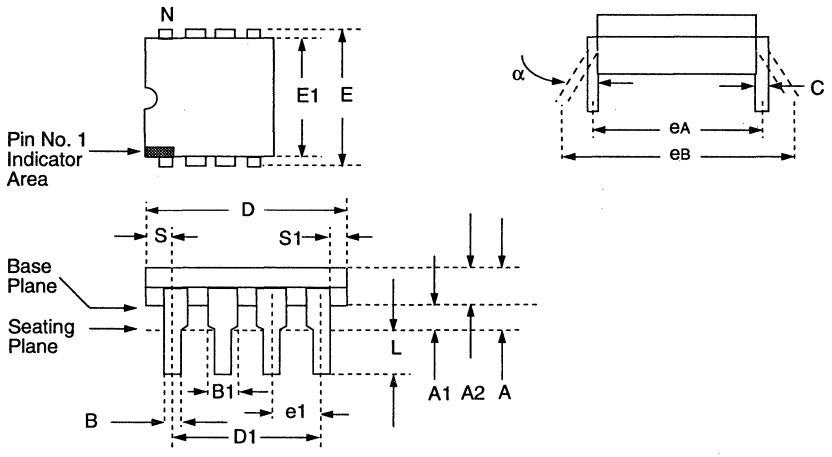
Symbol List for Plastic In-Line Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
A2	Base body thickness
B	Width of terminal leads
B1	Width of terminal lead shoulder which locate seating plane (standoff geometry optional)
C	Thickness of terminal leads
D	Largest overall package parameter of length
D1	Body length parameter - end lead center to end lead center
E	Largest overall package width parameter outside of lead
E1	Body width parameters not including leads
eA	Linear spacing of true minimum lead position center line to center line
eB	Linear spacing between true lead position outside of lead to outside of lead
e1	Linear spacing between center lines of body standoffs (terminal leads)
L	Distance from seating plane to end of lead
N	Total number of potentially usable lead positions
S	Distance from true position center line of Number 1 lead to the extremity of the body
S1	Distance from other end lead edge positions to the extremity of the body

Notes:

1. Controlling parameter: inches.
2. Parameter "e1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by board hole size.
4. Parameter "B1" is nominal.
5. Details of pin Number 1 identifier are optional.
6. Parameters "D + E1" do not include mold flash/protrusions.
   Mold flash or protrusions shall not exceed .010 inches.

Packaging Diagrams and Parameters

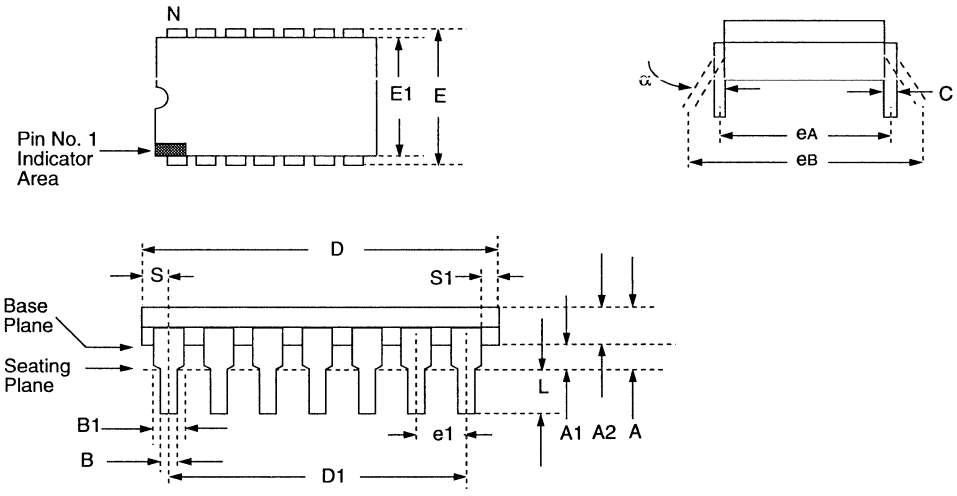
Package Type: 8-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.397	1.651		0.055	0.065	
C	0.203	0.381	Typical	0.008	0.015	Typical
D	9.017	10.922		0.355	0.430	
D1	7.620	7.620	Reference	0.300	0.300	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	8	8		8	8	
S	0.889	–		0.035	–	
S1	0.254	–		0.010	–	

Packaging Diagrams and Parameters

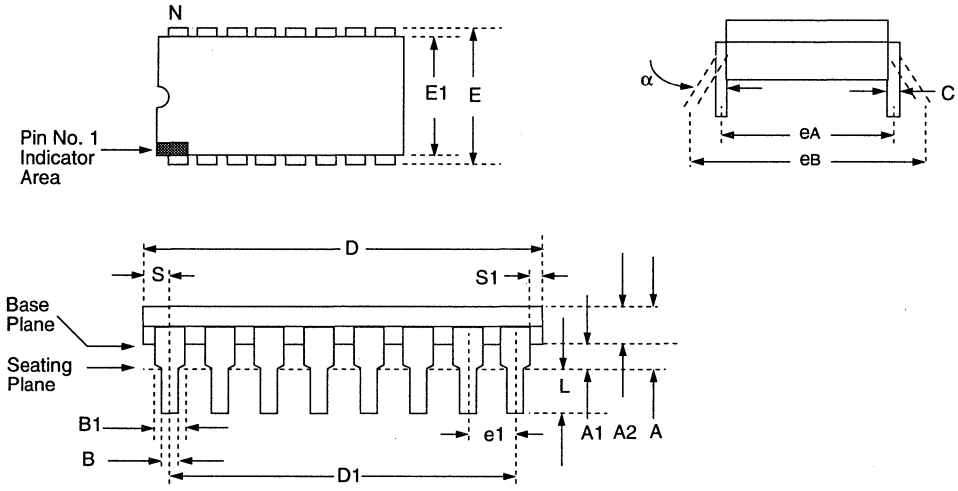
Package Type: 14-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.203	0.381	Typical	0.008	0.015	Typical
D	18.415	19.431		0.725	0.765	
D1	15.240	15.240	Reference	0.600	0.600	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	14	14		14	14	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

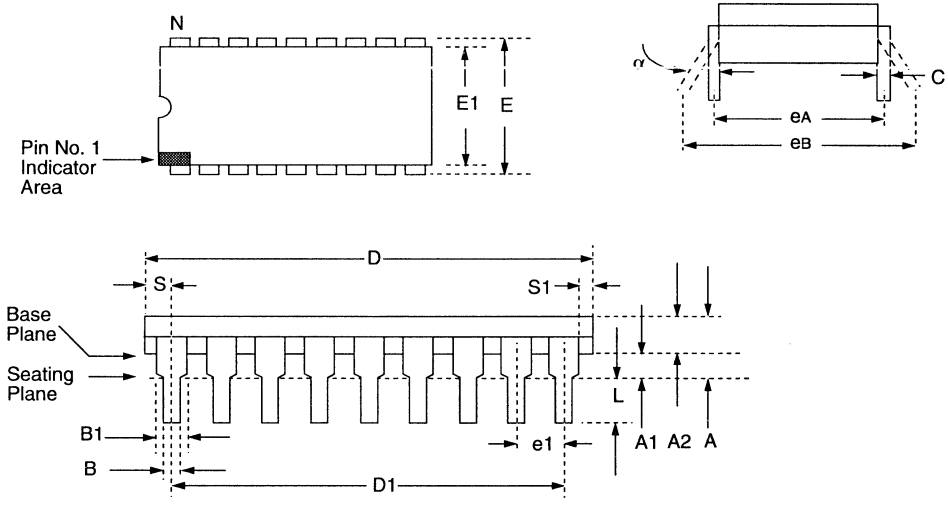
Package Type: 16-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.203	0.381	Typical	0.008	0.015	Typical
D	18.923	19.939		0.745	0.785	
D1	17.780	17.780	Reference	0.700	0.700	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	16	16		16	16	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

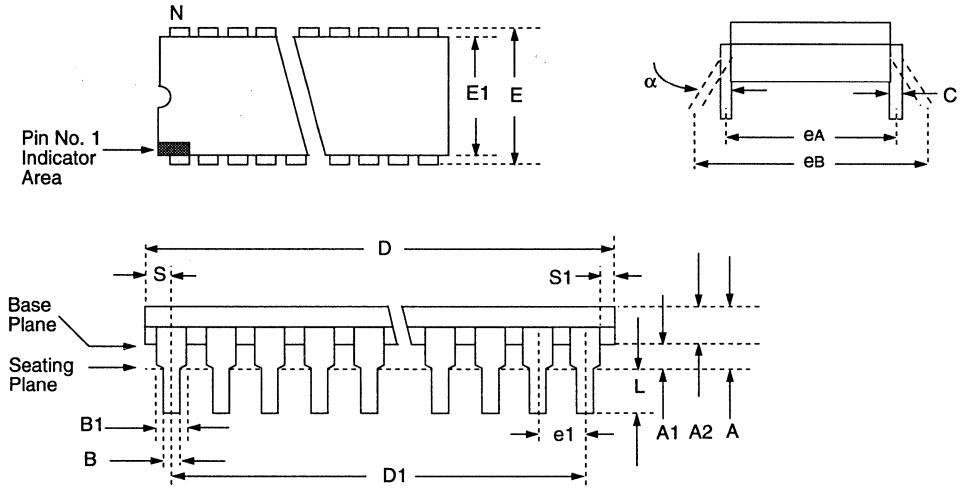
Package Type: 18-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.479	23.495		0.885	0.925	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

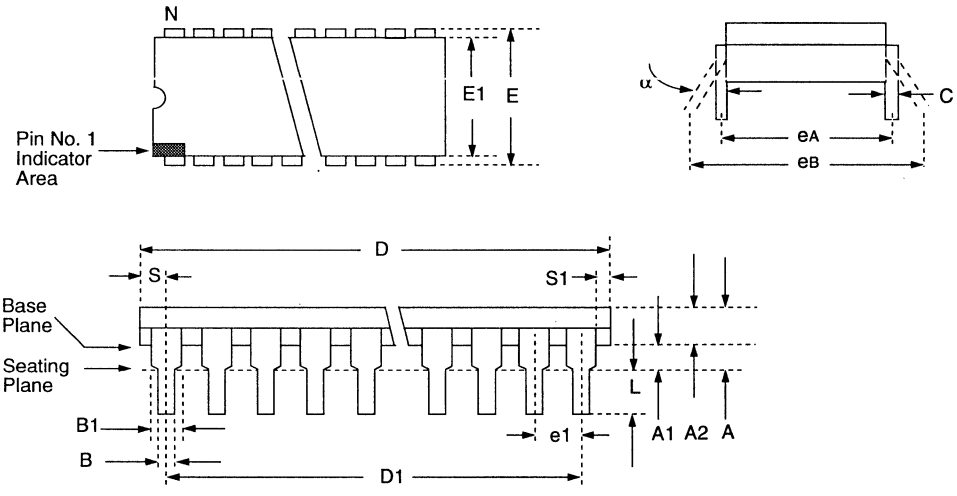
Package Type: 22-Lead Plastic Dual In-line (400 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.572		–	0.180	
A1	0.381	–		0.015	–	
A2	3.175	3.810		0.125	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.203	0.381	Typical	0.008	0.015	Typical
D	26.670	28.448		1.050	1.120	
D1	25.400	25.400	Reference	1.000	1.000	Reference
E	9.906	10.795		0.390	0.425	
E1	8.382	9.398		0.330	0.370	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	10.160	10.160	Reference	0.400	0.400	Reference
eB	10.160	12.192		0.400	0.480	
L	3.048	3.556		0.120	0.140	
N	22	22		22	22	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

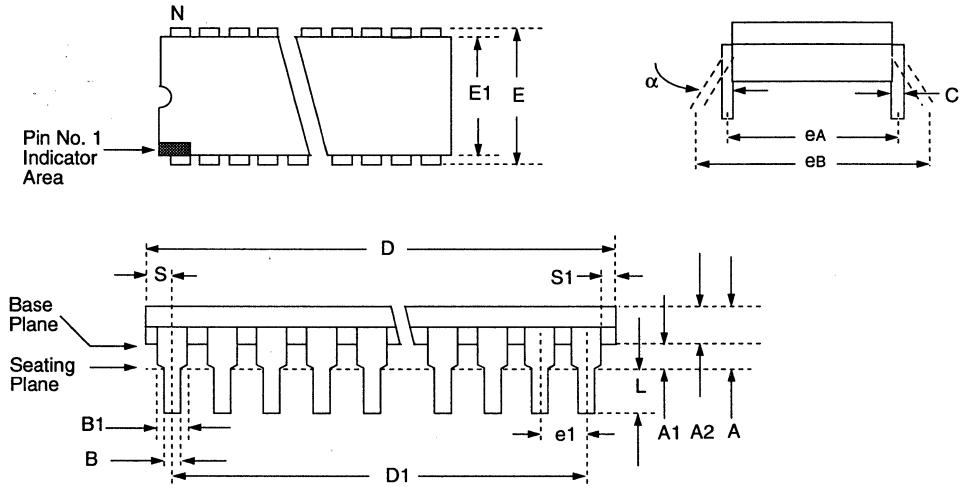
Package Type: 24-Lead Plastic Dual In-line (600 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	30.353	32.385		1.195	1.275	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	15.240	15.875		0.600	0.625	
E1	12.827	14.224		0.505	0.560	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.494	17.272		0.610	0.680	
L	3.048	3.556		0.120	0.140	
N	24	24		24	24	
S	0.889	–		0.035	–	
S1	0.127	–		0.005	–	

Packaging Diagrams and Parameters

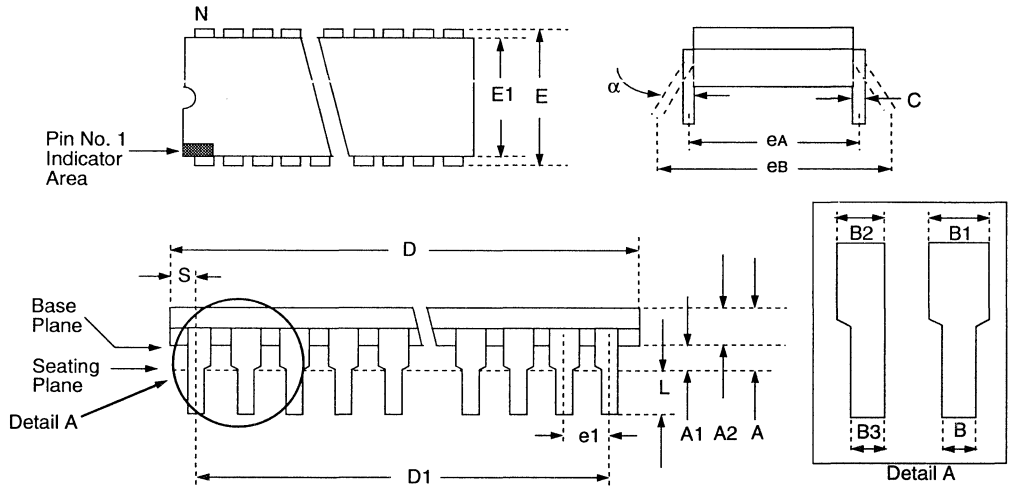
Package Type: 24-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	4.064		–	0.160	
A1	0.381	–		0.015	–	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	Typical	0.060	0.060	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	31.242	32.258		1.230	1.270	
D1	27.940	27.940	Reference	1.100	1.100	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	24	24		24	24	
S	0.889	–		0.035	–	
S1	0.381	–		0.015	–	

Packaging Diagrams and Parameters

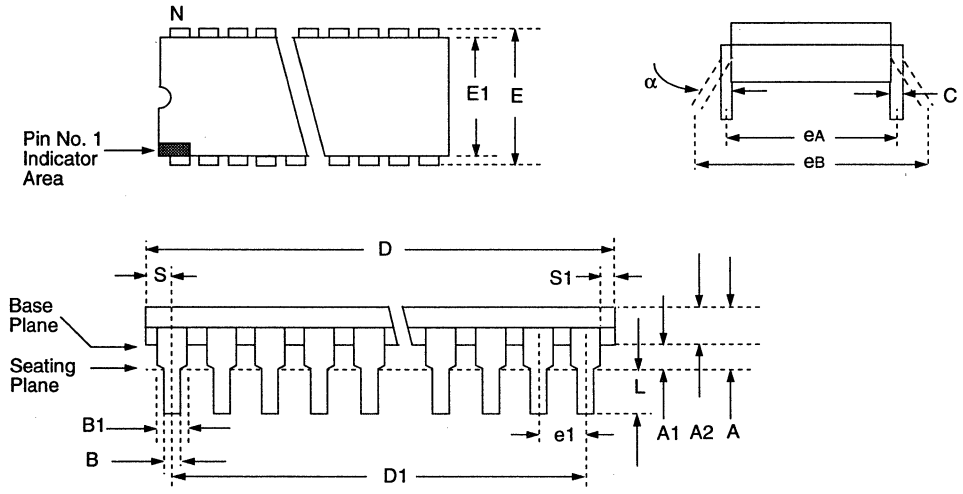
Package Type: 28-Lead Plastic Dual In-line (300 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	3.632	4.572		0.143	0.180	
A1	0.381	–		0.015	–	
A2	3.175	3.556		0.125	0.140	
B	0.406	0.559		0.016	0.022	
B1	1.016	1.651	Typical	0.040	0.065	Typical
B2	0.762	1.016	4 places	0.030	0.040	4 places
B3	0.203	0.508	4 places	0.008	0.020	4 places
C	0.203	0.331	Typical	0.008	0.013	Typical
D	34.163	35.179		1.385	1.395	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	7.874	8.382		0.310	0.330	
E1	7.112	7.493		0.280	0.295	
e1	2.540	2.540	Typical	0.100	0.100	Typical
eA	7.874	7.874	Reference	0.310	0.310	Reference
eB	8.128	9.652		0.320	0.380	
L	3.175	3.683		0.125	0.145	
N	28	-		28	-	
S	0.584	1.220		0.023	0.048	

Packaging Diagrams and Parameters

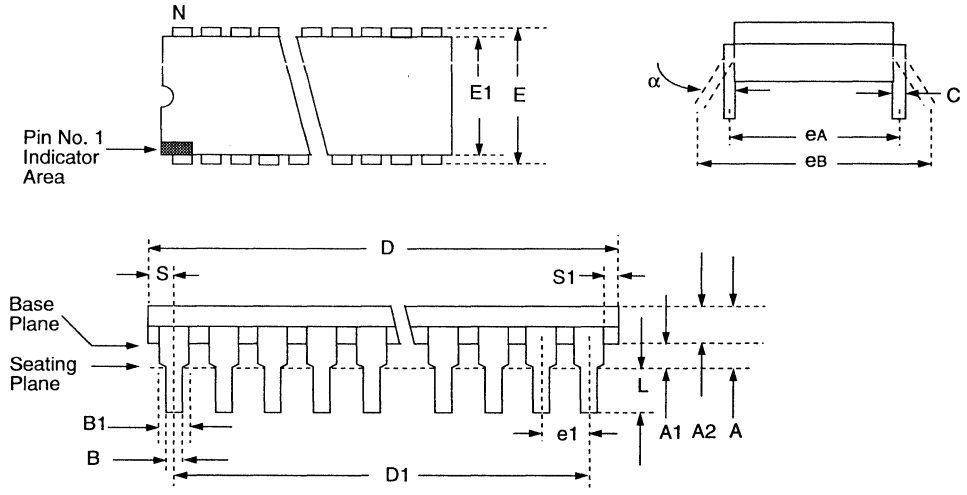
Package Type: 28-Lead Plastic Dual In-line (600 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.508	–		0.020	–	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.778	Typical	0.050	0.070	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	35.052	37.084		1.380	1.460	
D1	33.020	33.020	Reference	1.300	1.300	Reference
E	15.240	15.875		0.600	0.625	
E1	12.827	13.970		0.505	0.550	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	28	28		28	28	
S	0.889	–		0.035	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

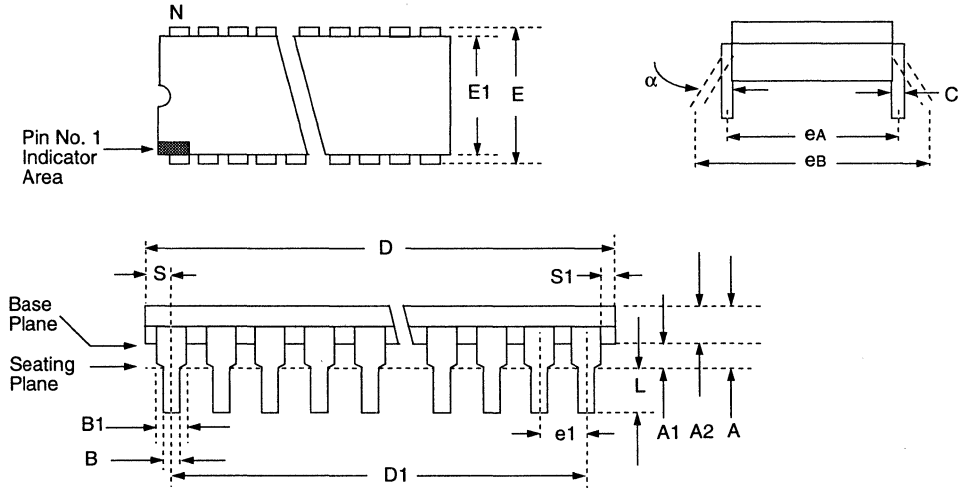
Package Type: 40-Lead Plastic Dual In-line (600 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.381	–		0.015	–	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.778	Typical	0.050	0.070	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	51.181	52.197		2.015	2.055	
D1	48.260	48.260	Reference	1.900	1.900	Reference
E	15.240	15.875		0.600	0.625	
E1	13.462	13.970		0.530	0.550	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	40	40		40	40	
S	1.270	–		0.050	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

Package Type: 48-Lead Plastic Dual In-line (600 mil)



Package Group: Plastic Dual In-Line (PLA)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	–	5.080		–	0.200	
A1	0.381	–		0.015	–	
A2	3.175	4.064		0.125	0.160	
B	0.355	0.559		0.014	0.022	
B1	1.270	1.270	Typical	0.050	0.050	Typical
C	0.203	0.381	Typical	0.008	0.015	Typical
D	61.468	62.230		2.420	2.450	
D1	58.420	58.420	Reference	2.300	2.300	Reference
E	15.240	15.875		0.600	0.625	
E1	13.716	14.224		0.540	0.560	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	15.240	15.240	Reference	0.600	0.600	Reference
eB	15.240	17.272		0.600	0.680	
L	2.921	3.683		0.115	0.145	
N	48	48		48	48	
S	1.270	–		0.050	–	
S1	0.508	–		0.020	–	

Packaging Diagrams and Parameters

Plastic Leaded Chip Carrier Family

Symbol List for Plastic Leaded Chip Carrier Package Parameters	
Symbol	**Description of Parameters**
A	Distance between seating plane to highest point of body
A1	Distance between lead shoulder to seating plane
CP	Seating plane coplanarity
D/E	Outside dimension
D1/E1	Plastic body dimension
D2/E2	Footprint
D3/E3	Footprint
LT	Lead thickness
N	Total number of potentially usable lead positions
Nd	Total number of leads on short side (rectangular)
Ne	Total number of leads on long side (rectangular)

Notes:

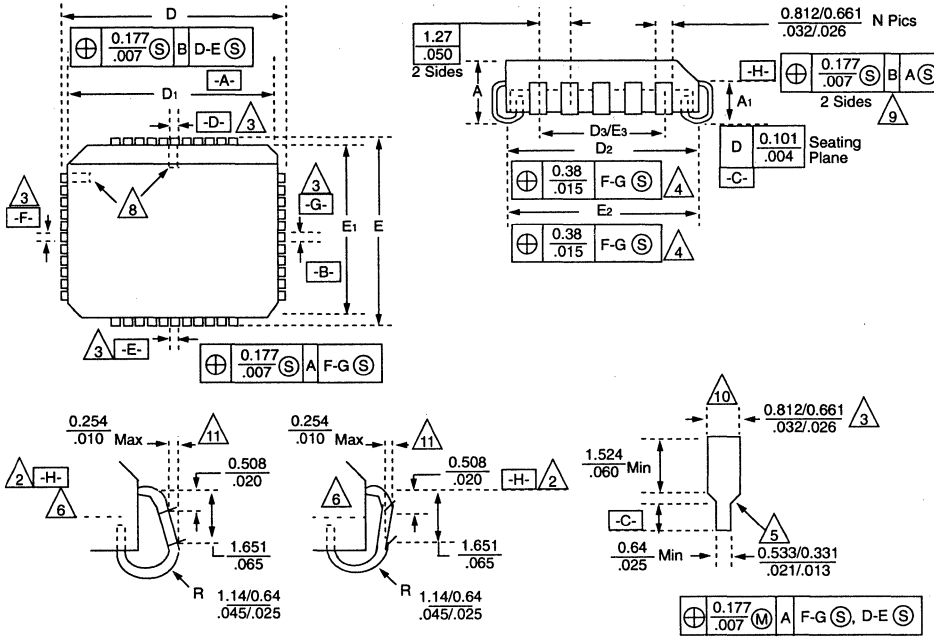
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane -H- located at top of mold parting line and coincident with top of lead where lead exits plastic body.
3. Datums D-E and F-G to be determined where center leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Transition is optional.
6. Plastic body details between leads are optional.
7. Dimension D1 and E1 do not include mold protrusion. Allowable mold protrusion is .254mm/.010in. per side. Dimensions D and E include mold mismatch and are determined at parting line.
8. Square: Details of pin 1 identifier are optional but must be located within one of the two zones indicated. Rectangle: Details of pin 1 identifier are optional but must be located within zone indicated. If the number of terminals on a side is odd, terminal 1 is the center terminal.
9. Location of datums -A- and -B- to be determined at plane -H-.
10. All dimensions and tolerances include lead trim offset and lead finish.
11. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
12. Controlling dimension: inches.

X. Sum of dambar protrusions to be 0.17 (.007) max. per lead.

Y. Feature is not required, but is optional at manufacturer's discretion.

Packaging Diagrams and Parameters

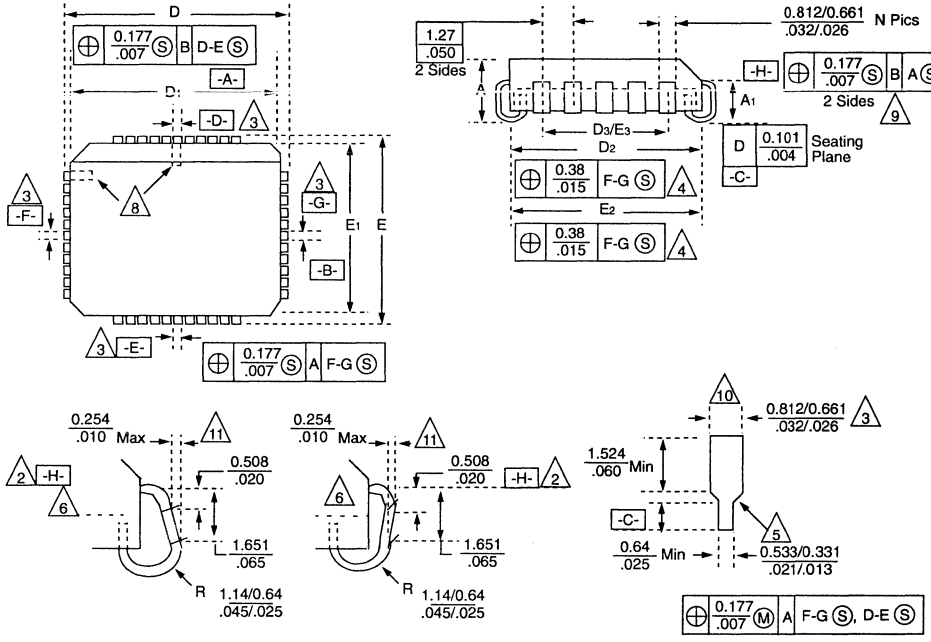
Package Type: 28-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	12.319	12.573		0.485	0.495	
D1	11.430	11.583		0.450	0.456	
D2	10.414	10.922		0.410	0.430	
D3	7.620	7.620	Reference	0.300	0.300	Reference
E	12.319	12.573		0.485	0.495	
E1	11.430	11.583		0.450	0.456	
E2	10.414	10.922		0.410	0.430	
E3	7.620	7.620	Reference	0.300	0.300	Reference
N	28	28		28	28	
CP	–	0.102		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

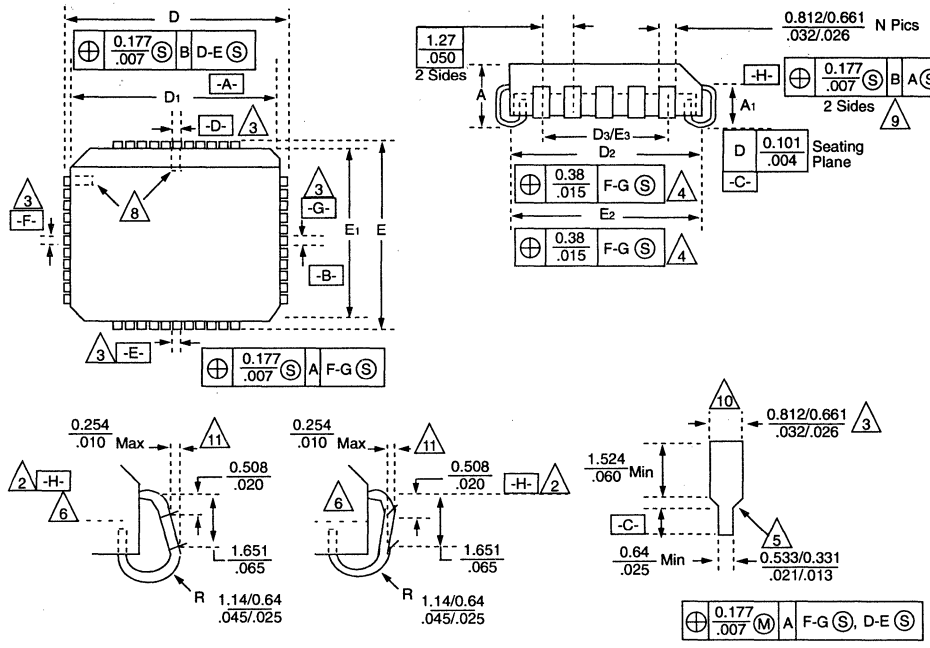
Package Type: 32-Lead Plastic Leaded Chip Carrier (Rectangle)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.048	3.556		0.120	0.140	
A1	1.905	2.413		0.075	0.095	
D	12.319	12.573		0.485	0.495	
D1	11.353	11.507		0.447	0.453	
D2	9.310	10.780		0.380	0.440	
D3	7.620	7.620	Reference	0.300	0.300	Reference
E	14.859	15.113		0.585	0.595	
E1	13.893	14.047		0.547	0.553	
E2	11.760	13.230		0.480	0.540	
E3	10.160	10.160	Reference	0.400	0.400	Reference
N	32	32		32	32	
Nd	7	7		7	7	
Ne	9	9		9	9	
CP	–	0.102		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

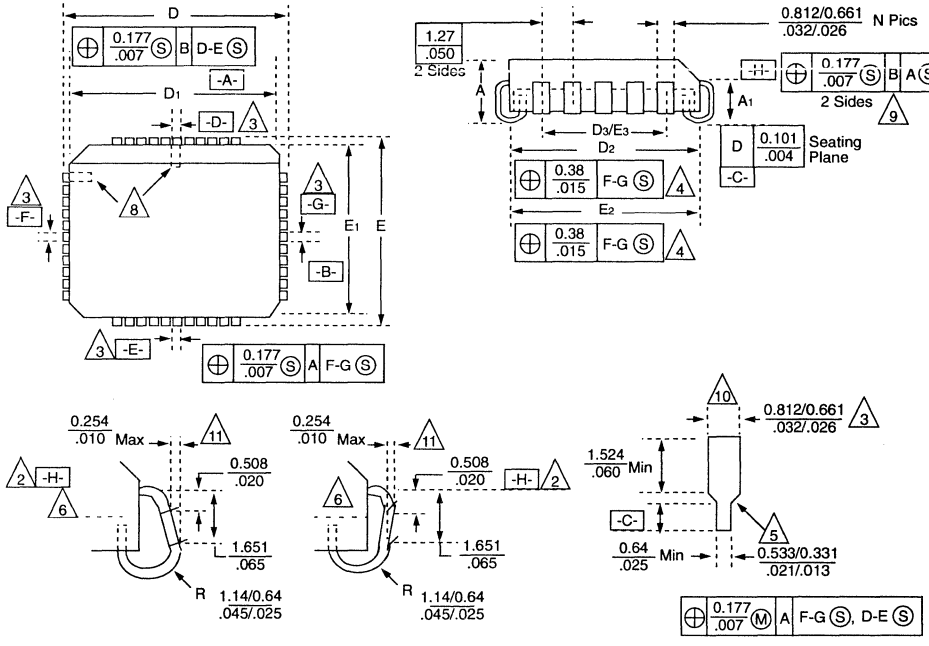
Package Type: 44-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.572		0.165	0.180	
A1	2.413	2.921		0.095	0.115	
D	17.399	17.653		0.685	0.695	
D1	16.510	16.663		0.650	0.656	
D2	15.494	16.002		0.610	0.630	
D3	12.700	12.700	Reference	0.500	0.500	Reference
E	17.399	17.653		0.685	0.695	
E1	16.510	16.663		0.650	0.656	
E2	15.494	16.002		0.610	0.630	
E3	12.700	12.700	Reference	0.500	0.500	Reference
N	44	44		44	44	
CP	–	0.102		–	0.004	
LT	0.203	0.381		0.008	0.015	

Packaging Diagrams and Parameters

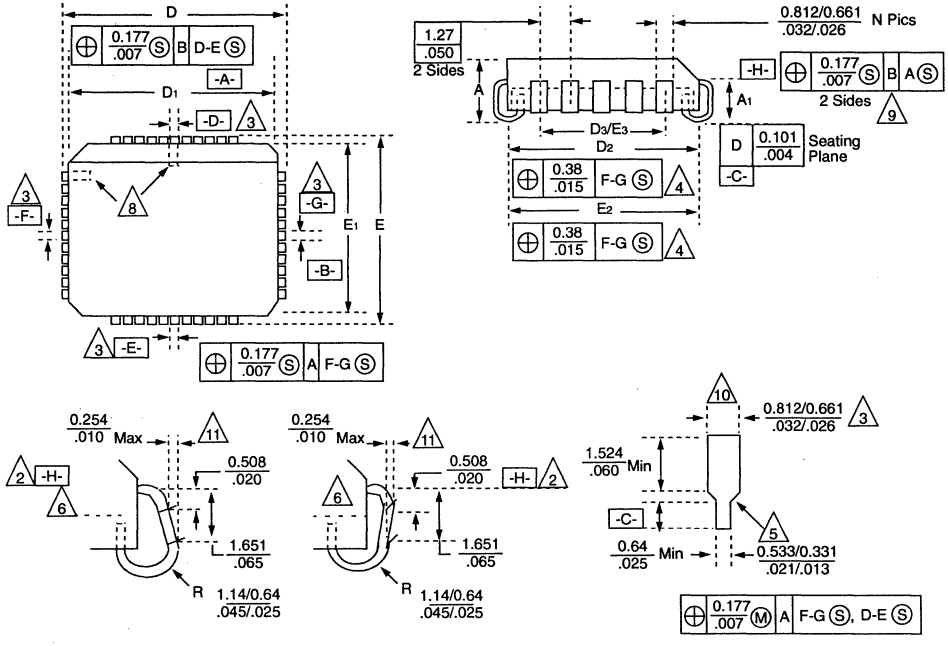
Package Type: 68-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		0.165	0.185	
A1	2.286	2.794		0.090	0.110	
D	25.019	25.273		0.985	0.995	
D1	24.130	24.334		0.950	0.958	
D2	22.860	23.622		0.900	0.930	
D3	20.320	-	Reference	0.800	-	Reference
E	25.019	25.273		0.985	0.995	
E1	24.130	24.334		0.950	0.958	
E2	22.860	23.622		0.900	0.930	
E3	20.320	-	Reference	0.800	-	Reference
N	68	-		68	-	
CP	-	0.102		-	0.004	
LT	0.203	0.254		0.008	0.010	

Packaging Diagrams and Parameters

Package Type: 84-Lead Plastic Leaded Chip Carrier (Square)



Package Group: Plastic Leaded Chip Carrier (PLCC)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.191	4.699		0.165	0.185	
A1	2.286	2.794		0.090	0.110	
D	30.099	30.353		1.185	1.195	
D1	29.210	29.414		1.150	1.158	
D2	27.940	28.702		1.100	1.130	
D3	25.400	-	Reference	1.000	-	Reference
E	30.099	30.353		1.185	1.195	
E1	29.210	29.414		1.150	1.158	
E2	27.940	28.702		1.100	1.130	
E3	25.400	-	Reference	1.000	-	Reference
N	84	-		84	-	
CP	-	0.102		-	0.004	
LT	0.203	0.254		0.008	0.010	

Packaging Diagrams and Parameters

Plastic Small Outline Family

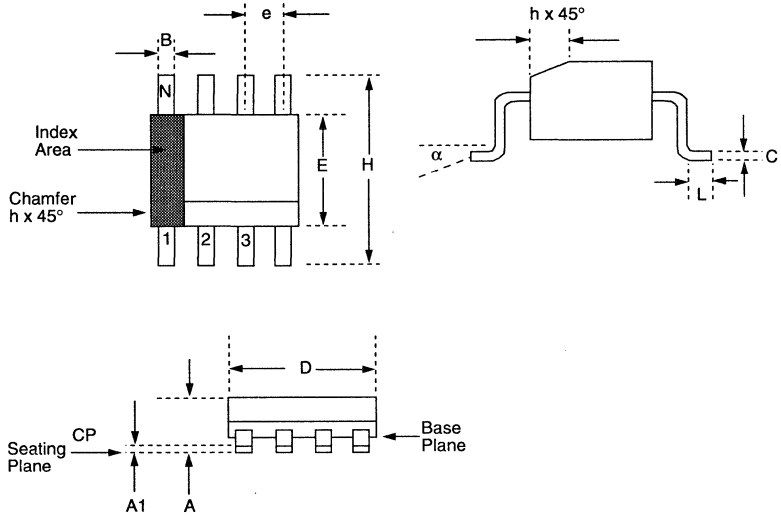
Symbol List for Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially usable lead positions
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: inches.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .006 package ends and .010 on sides.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area to indicate pin1 position.
5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

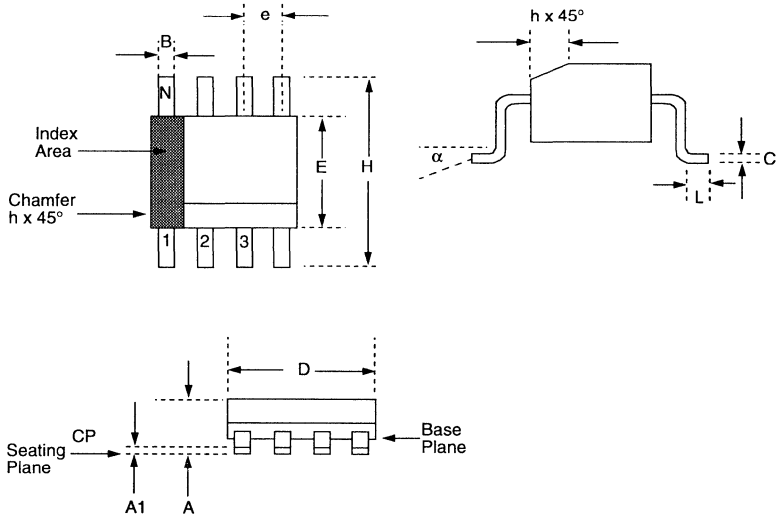
Package Type: 8-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SN)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.371	1.728		0.054	0.068	
A1	0.101	0.249		0.004	0.010	
B	0.355	0.483		0.014	0.019	
C	0.190	0.249		0.007	0.010	
D	4.800	4.979		0.189	0.196	
E	3.810	3.988		0.150	0.157	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	5.816	6.198		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
N	8	8		8	8	
CP	–	0.102		–	0.004	

Packaging Diagrams and Parameters

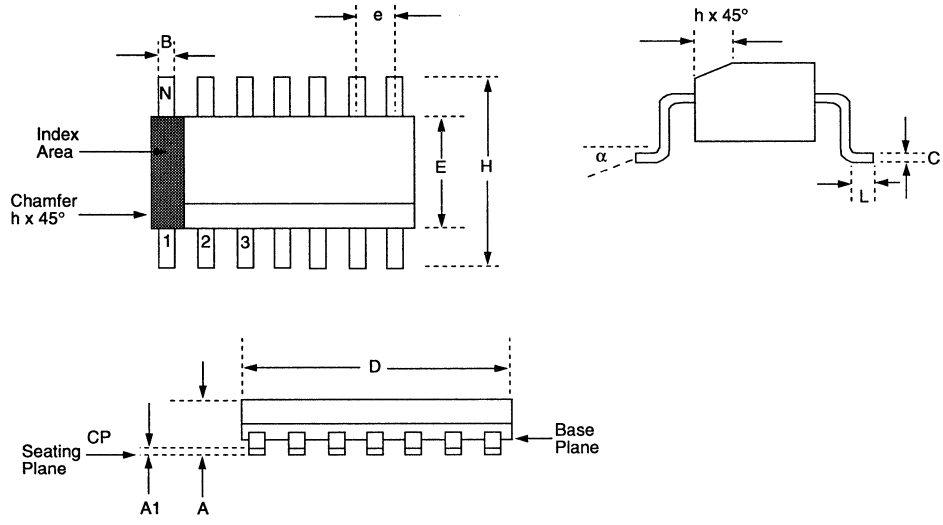
Package Type: 8-Lead Plastic Surface Mount (SOIC - Medium, 200 mil Body)



Package Group: Plastic SOIC (SM)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.778	2.032		0.070	0.080	
A1	0.101	0.249		0.004	0.010	
B	0.355	0.483		0.014	0.019	
C	0.190	0.249		0.007	0.010	
D	5.080	5.334		0.200	0.210	
E	5.156	5.411		0.203	0.213	
e	1.270	1.270	Reference	0.050	0.050	Reference
H*	7.670	8.103		0.302	0.319	
h	0.381	0.762		0.015	0.030	
L	0.508	1.016		0.020	0.040	
N	14	14		14	14	
CP	–	0.102		–	0.004	

Packaging Diagrams and Parameters

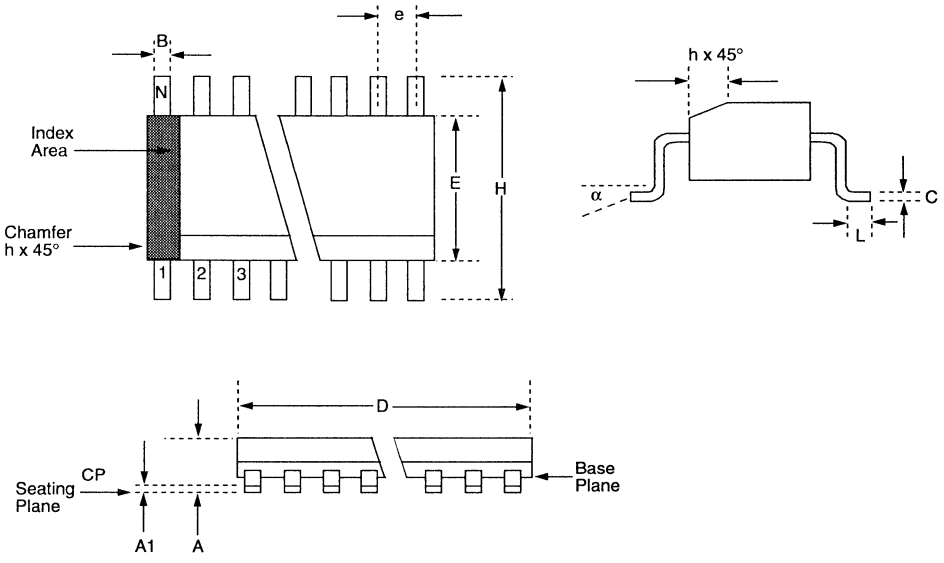
Package Type: 14-Lead Plastic Surface Mount (SOIC - Narrow, 150 mil Body)



Package Group: Plastic SOIC (SL)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.371	1.728		0.054	0.068	
A1	0.101	0.249		0.004	0.010	
B	0.355	0.483		0.014	0.019	
C	0.190	0.249		0.008	0.010	
D	8.559	9.983		0.337	0.393	
E	3.810	3.988		0.150	0.157	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	5.816	6.198		0.229	0.244	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	14	14		16	16	
CP	–	0.102		–	0.004	

Packaging Diagrams and Parameters

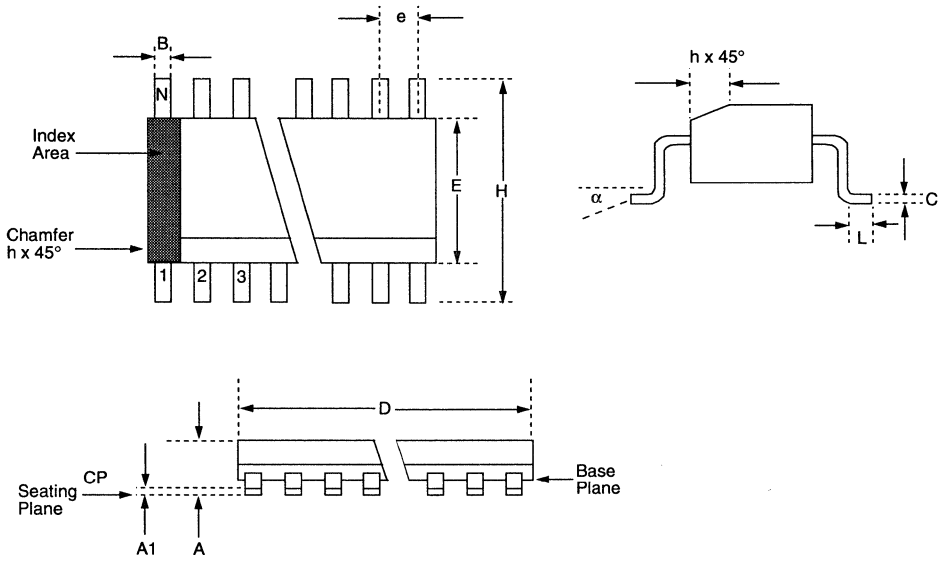
Package Type: 18-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	11.353	11.735		0.447	0.462	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	18	18		18	18	
CP	–	0.102		–	0.004	

Packaging Diagrams and Parameters

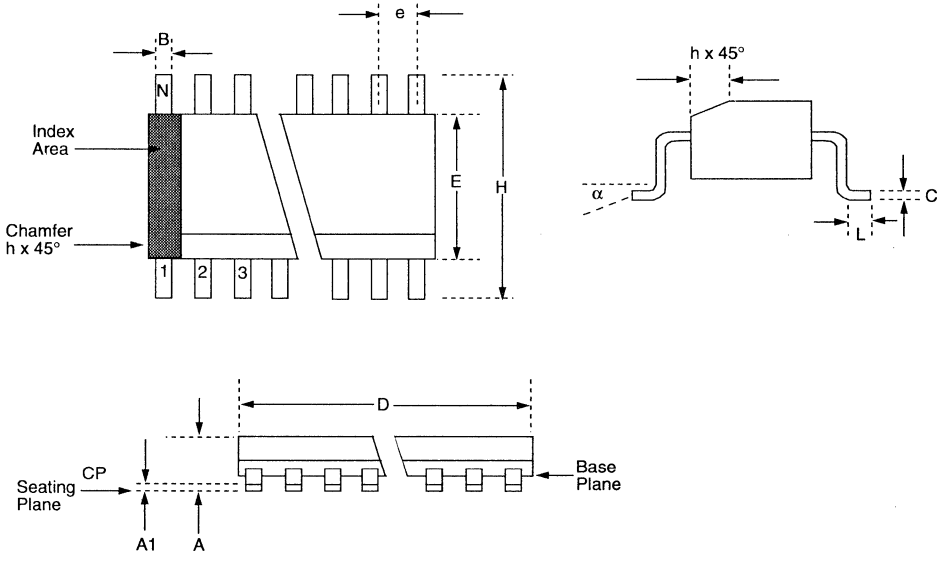
Package Type: 24-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	15.214	15.596		0.599	0.614	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	24	24		24	24	
CP	–	0.102		–	0.004	

Packaging Diagrams and Parameters

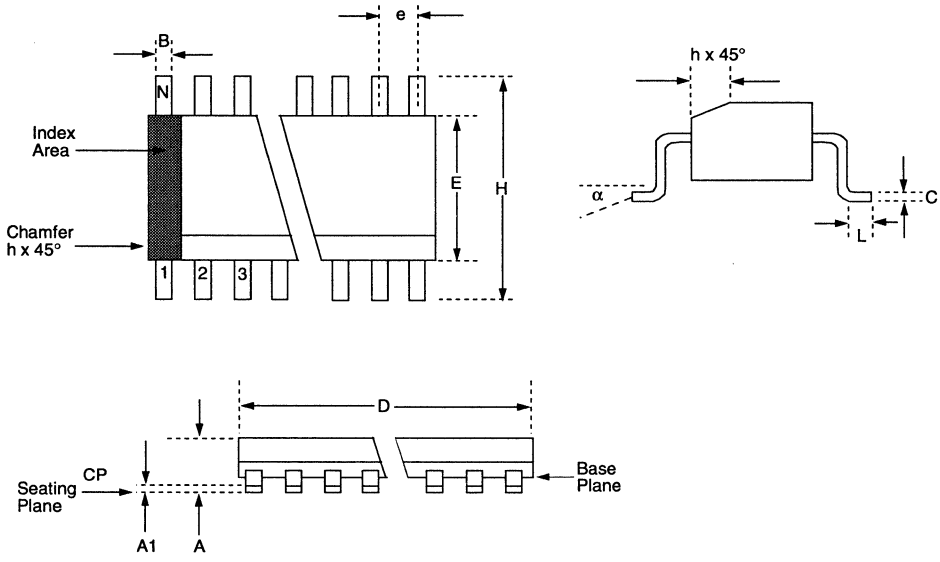
Package Type: 28-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body)



Package Group: Plastic SOIC (SO)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	17.703	18.085		0.697	0.712	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	Typical	0.050	0.050	Typical
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	28	28		28	28	
CP	–	0.102		–	0.004	

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (SOIC - Wide, 330 mil Body)



Package Group: Plastic SOIC (SW)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	2.286	2.642		0.090	0.104	
A1	0.101	0.280		0.004	0.011	
B	0.355	0.508		0.014	0.020	
C	0.228	0.305		0.009	0.012	
D	17.780	18.085		0.700	0.712	
E	8.636	8.890		0.340	0.350	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	11.760	12.116		0.463	0.477	
h	0.254	0.737		0.010	0.029	
L	0.508	1.067		0.020	0.042	
N	28	28		28	28	
CP	–	0.102		–	0.004	

Packaging Diagrams and Parameters

Plastic Shrink Small Outline Family

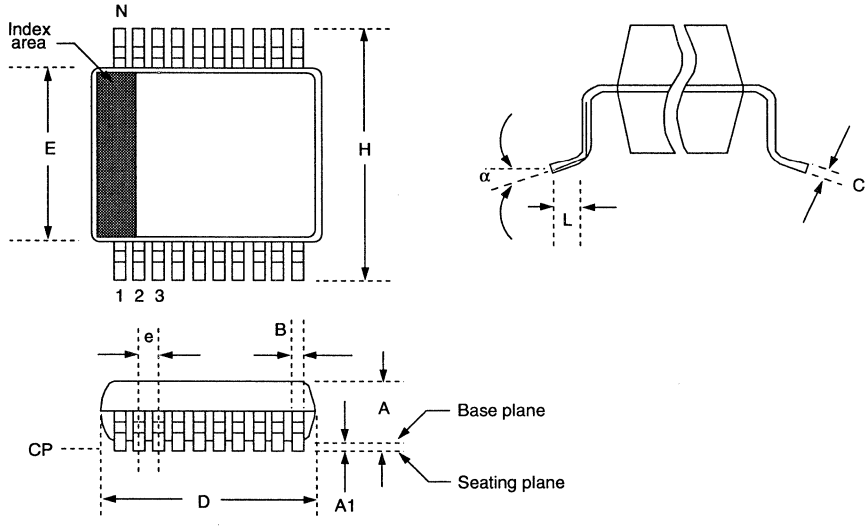
Symbol List for Shrink Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially usable lead positions
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: mm.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .015mm .006 package ends and .010" on sides.
4. A .25mm visual index feature must be located within the shaded area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

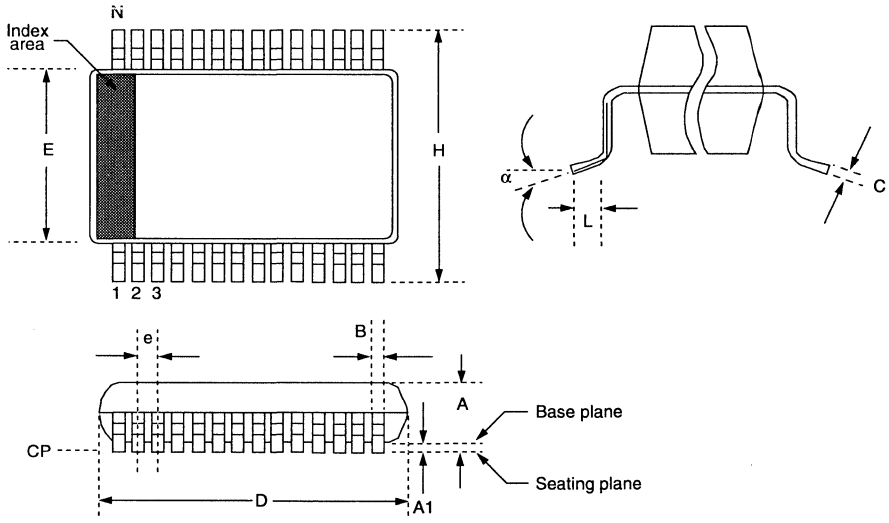
Package Type: 20-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm)



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	7.070	7.330		0.278	0.289	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	Reference	0.026	0.026	Reference
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
N	20	20		20	20	
CP	-	0.102		-	0.004	

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm)



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	10.070	10.330		0.396	0.407	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	Reference	0.026	0.026	Reference
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
N	28	28		28	28	
CP	-	0.102		-	0.004	

Packaging Diagrams and Parameters

Plastic Thin Small Outline and Very Small Outline Families (TSOP, VSOP)

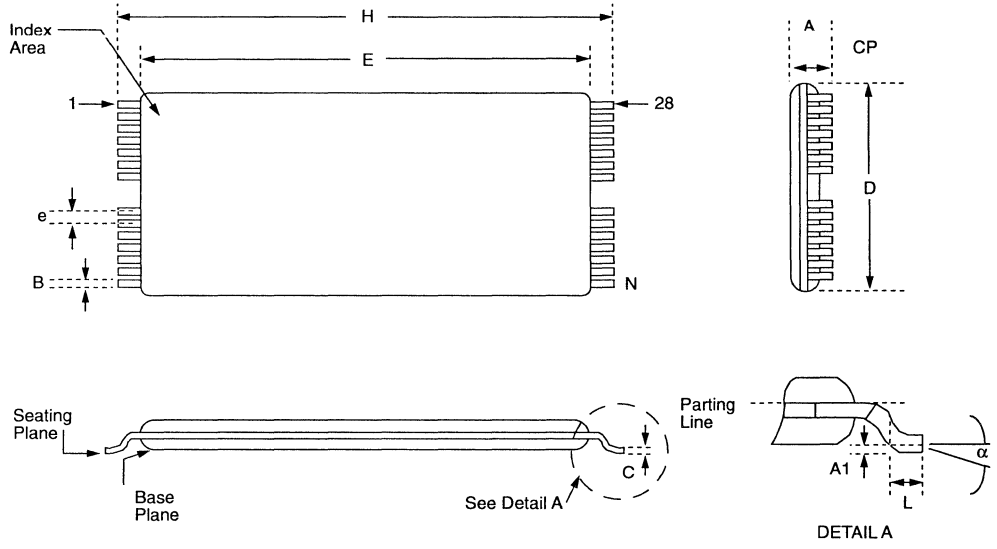
Symbol List for Thin Small Outline Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
B	Width of terminals
C	Thickness of terminals
D	Largest overall package parameter of length
E	Largest overall package width parameter not including leads
e	Linear spacing of true minimum lead position center line to center line
H	Largest overall package dimension of width
L	Length of terminal for soldering to a substrate
N	Total number of potentially usable lead positions
CP	Seating plane coplanarity

Notes:

1. Controlling parameter: inches.
2. All packages are gull wing lead form.
3. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005 per side.
4. A visual index feature must be located within the crosshatched area to indicate pin 1 position.
5. Terminal numbers are shown for reference.

Packaging Diagrams and Parameters

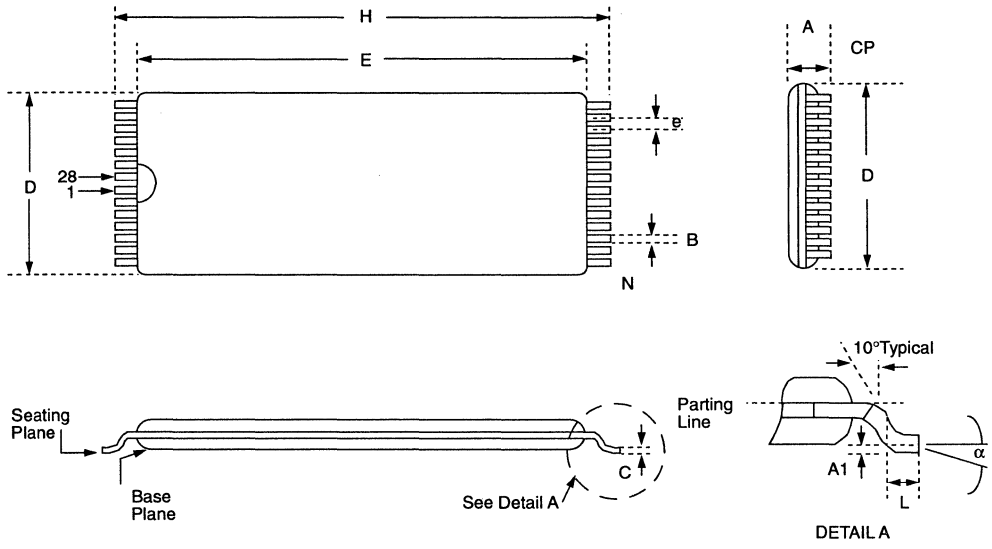
Package Type: 28-Lead Plastic Surface Mount (TSOP 8 x 20 mm)



Package Group: Plastic TSOP (TS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	-	1.190		-	0.047	
A1	0.050	0.150		0.002	0.006	
B	0.150	0.250		0.006	0.010	
C	0.100	0.200		0.004	0.008	
D	7.800	8.200		0.307	0.323	
E	18.290	18.490		0.720	0.728	
e	0.510	-	Reference	0.020	-	Reference
H	19.810	20.190		0.780	0.795	
L	0.410	0.610		0.016	0.024	
N	28	28		28	28	
CP	-	0.102		-	0.004	

Packaging Diagrams and Parameters

Package Type: 28-Lead Plastic Surface Mount (VSOP 8 x 13.4 mm))



Package Group: Plastic VSOP (VS)						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0	8°		0	8°	
A	1.000	1.250		0.039	0.049	
A1	0.000	0.200		0.000	0.008	
B	0.150	0.300		0.006	0.012	
C	0.130	0.220		0.005	0.009	
D	7.900	8.100		0.311	0.319	
E	11.700	11.900		0.460	0.468	
e	0.550	-	Reference	0.022	-	Reference
H	13.100	13.700		0.516	0.539	
N	28	28		28	28	
L	0.300	0.700		0.012	0.027	
CP	-	0.102		-	0.004	

Packaging Diagrams and Parameters

Plastic Metric Quad Flatpack Family (MQFP)

Symbol List for Metric Plastic Quad Flatpack Package Parameters	
Symbol	**Description of Parameters**
α	Angular spacing between min. and max. lead positions measured at the gauge plane
A	Distance between seating plane to highest point of body
A1	Distance between seating plane and base plane
A2	Distance from base plane to highest point of body
b	Width of terminals
C	Thickness of terminals
D1/E1	Largest overall package parameter including leads
D/E	Largest overall package parameter including leads
D3/E3	Center of end lead to center of end lead
e	Linear spacing of true minimum lead position center line to center line
L	Length of terminal for soldering to a substrate
N	Total number of potentially usable lead positions
CP	Seating plane coplanarity

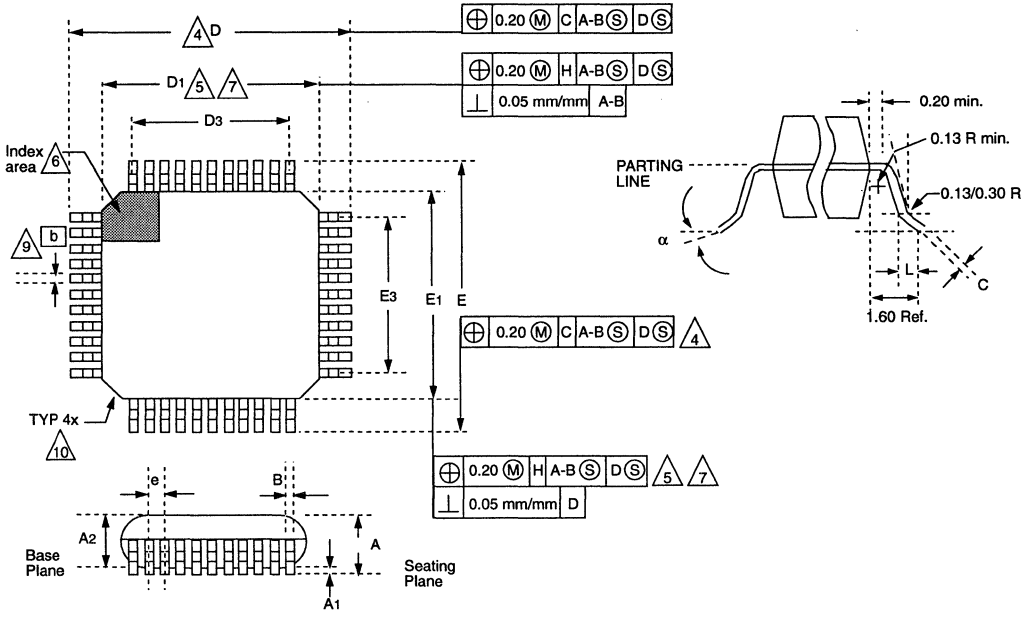
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane -H- is located at bottom of mold parting line and coincident with bottom of lead, where lead exits body.
3. Datums A-B and -D- to be determined at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimension D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25mm per side. Dimensions D1 and E1 do not include mold mismatch and are determined at datum plane -H-.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. These dimensions to be determined at datum plane -H-.
8. All dimensions are in millimeters.
9. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.
10. Exact shape of this feature is optional.
11. N is the number of leads.
12. Controlling parameter: millimeters.
13. All packages are gull wing lead form.

11

Packaging Diagrams and Parameters

Package Type: 44-Lead Plastic Surface Mount (MQFP 10x10 mm Body 1.6/0.15 mm Lead Form))



Package Group: Plastic MQFP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	7°		0°	7°	
A	2.000	2.350		0.078	0.093	
A1	0.050	0.250		0.002	0.010	
A2	1.950	2.100		0.768	0.083	
b	0.300	0.450	Typical	0.011	0.018	Typical
C	0.150	0.180		0.006	0.007	
D	12.950	13.450		0.510	0.530	
D1	9.900	10.100		0.390	0.398	
D3	8.000	8.000	Reference	0.315	0.315	Reference
E	12.950	13.450		0.510	0.530	
E1	9.900	10.100		0.390	0.398	
E3	8.000	8.000	Reference	0.315	0.315	Reference
e	0.800	0.800		0.031	0.032	
L	0.730	1.030		0.028	0.041	
N	44	44		44	44	
CP	0.102	–		0.004	–	

SECTION 12
OFFICE LOCATIONS

Factory Representatives
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Distributors
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Factory Sales 12-21

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