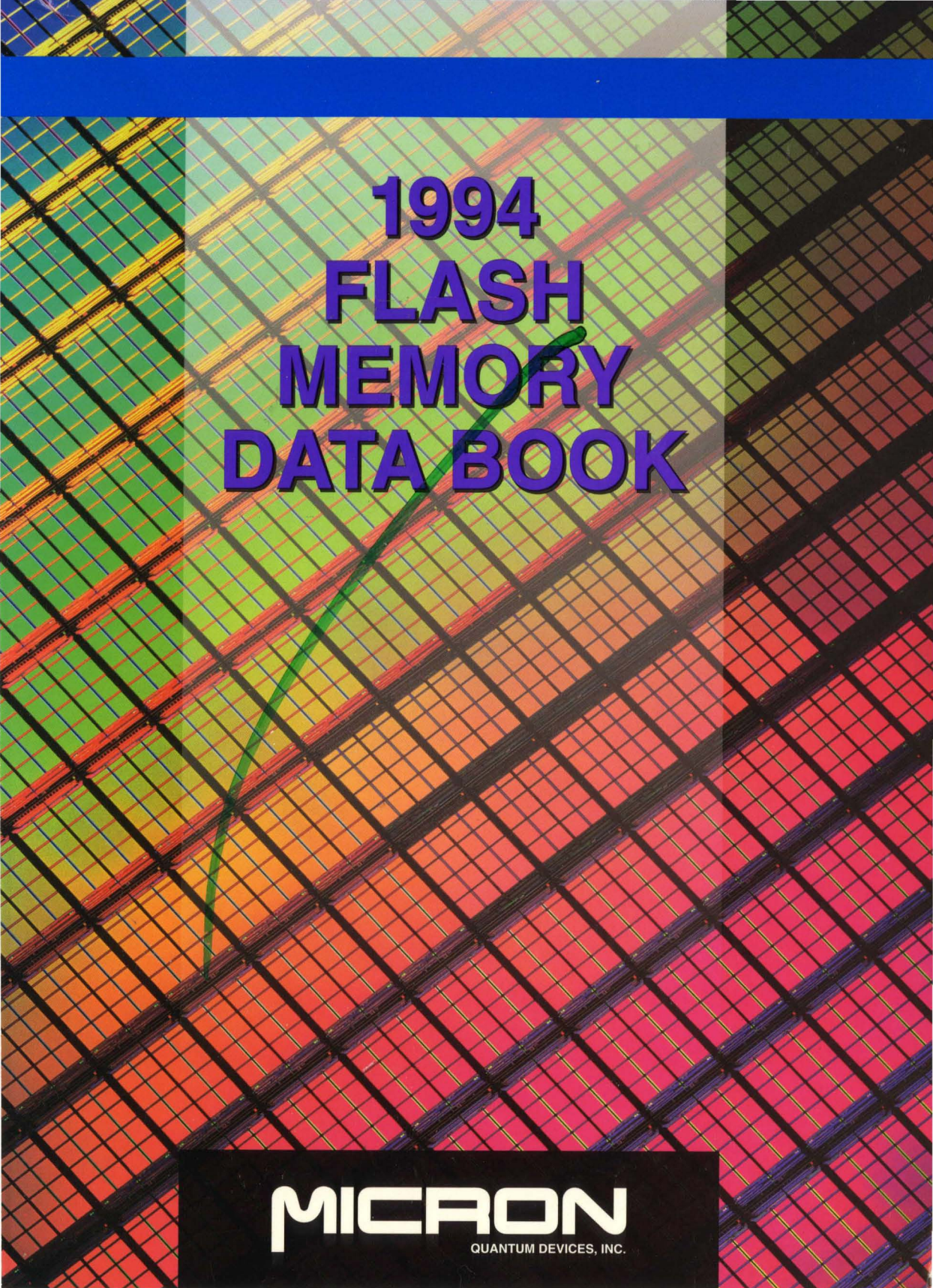
1994
FLASH
MEMORY
DATA BOOK
MICRON
QUANTUM DEVICES, INC.

MICRON
QUANTUM DEVICES, INC.

5/12 VOLT FLASH MEMORY 1

3.3/12 VOLT FLASH MEMORY 2

PACKAGE INFORMATION 3

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MICRON
QUANTUM DEVICES, INC.

FLASH MEMORY DATA BOOK

Micron Quantum Devices' products are marketed worldwide by Micron Semiconductor, Inc. For additional information contact:

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ABOUT THE COVER:

Front — A wafer of Micron Quantum Devices' 4 Meg Boot Block Flash memory.

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The Micron Team

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Micron Quantum Devices, Inc. and its parent company, Micron Semiconductor, Inc., bring quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds and smallest die sizes. And we establish delivery standards based on customer expectations, including JIT programs, made possible by ever-increasing product reliability.

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ABOUT THIS BOOK

CONTENT

The 1994 *Flash Memory Data Book* from Micron Quantum Devices, Inc. provides specifications on Micron's Flash memory products.

SECTION ORGANIZATION

Micron Quantum Devices' 1994 *Flash Memory Data Book* contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The *Data Book* is organized into four sections:

- **Sections 1–2:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 3:** Packaging information.
- **Section 4:** Sales information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by density and second by bus width. For example, the 5 Volt Flash Memory section begins with 2 Meg products: first the 256K x 8 data sheet followed by 128K x 16 data sheet and all other configurations in order of ascending density. Next come the 4 Meg products, followed by 8 Meg, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either Advance, Preliminary or Final. In addition, new product data sheets that are new additions are designated with a "New" indicator in the tab area of each page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron Quantum Devices product literature, or to order additional copies of this publication, contact

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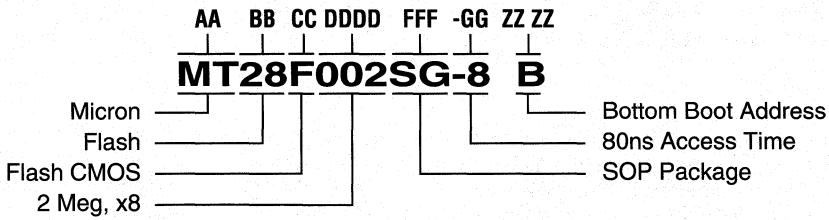
DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
Advance	This data sheet contains initial descriptions of products still under development.
Preliminary	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
New	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the data book.

NOTE: Micron Quantum Devices' *Flash Memory Data Book* uses acronyms to refer to certain industry-standard-setting bodies. These are defined below:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council
JEIDA—Japanese Electronics Industry Development Association
PCMCIA—Personal Computer Memory Card International Association

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

Flash 28
DRAM 4
TPDRAM 43
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
Flash CMOS ..... F
Low Voltage Flash CMOS ..... LF

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

Flash ..... Density, Configuration
DRAM ..... Width, Density
TPDRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Density, Width

E – DEVICE VERSIONS

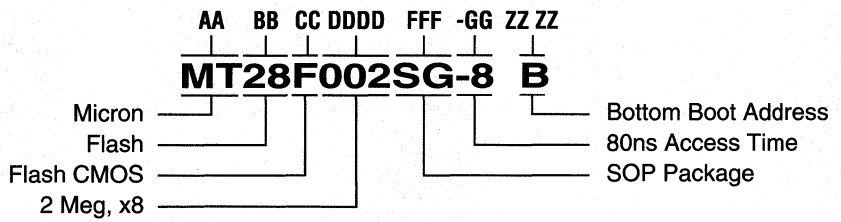
(Alphabetic characters only; located between D and F when required.)

JEDEC Test Mode (4 Meg DRAM) ..... J
Errata on Base Part ..... Q

FFF – PACKAGE CODES

PLASTIC
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type I) ..... VG
TSOP (Type I, Reversed) ..... XG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Flash	
Bottom Boot	B
Top Boot	T
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

5/12 VOLT FLASH MEMORY

		PAGE
MT28F002	256K x 8	BB, AUTO 1-1
MT28F200	128K x 16/256K x 8	BB, AUTO 1-25
MT28F004	512K x 8	BB, AUTO 1-49
MT28F400	256K x 16/512K x 8	BB, AUTO 1-73
MT28F008	1 Meg x 8	SB, AUTO, DPD 1-97

BB ..... Boot Block
SB ..... Symmetric Block
AUTO ..... Automated W/E Algorithm
DPD ..... Deep Power Down

3.3/12 VOLT FLASH MEMORY

		PAGE
MT28LF002	256K x 8	BB, AUTO 2-1
MT28LF200	128K x 16/256K x 8	BB, AUTO 2-3
MT28LF004	512K x 8	BB, AUTO 2-5
MT28LF400	256K x 16/512K x 8	BB, AUTO 2-7
MT28LF008	1 Meg x 8	SB, AUTO, DPD 2-31

BB ..... Boot Block
SB ..... Symmetric Block
AUTO ..... Automated W/E Algorithm
DPD ..... Deep Power Down

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28F004	5V/12 Flash Memory	1-49
28F008	5V/12 Flash Memory	1-97
28F200	5V/12 Flash Memory	1-25
28F400	5V/12 Flash Memory	1-73
28LF002	3.3V/12 Flash Memory	2-1
28LF004	3.3V/12 Flash Memory	2-5
28LF008	3.3V/12 Flash Memory	2-31
28LF200	3.3V/12 Flash Memory	2-3
28LF400	3.3V/12 Flash Memory	2-7

5/12 VOLT FLASH MEMORY PRODUCT SELECTION GUIDE

Memory Configuration	Features/ Options	Part Number	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins		Page
				Standby	Active	SOP	TSOP	
256K x 8	BB, AUTO	MT28F002	60, 80, 100	100µA	60mA	-	40	1-1
128K x 16/ 256K x 8	BB, AUTO	MT28F200	60, 80, 100	100µA	60mA	44	56	1-25
512K x 8	BB, AUTO	MT28F004	60, 80, 100	100µA	60mA	-	40	1-49
256K x 16/ 512K x 8	BB, AUTO	MT28F400	60, 80, 100	100µA	60mA	44	56	1-73
1 Meg x 8	SB, AUTO, DPD	MT28F008	80, 90, 100	100µA	50mA	44	40	1-97

BB = Boot Block, AUTO = Automated W/E Algorithm, SB = Symmetric Block, DPD = Deep Power Down

3.3/12 VOLT FLASH MEMORY PRODUCT SELECTION GUIDE

Memory Configuration	Features/ Options	Part Number	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins		Page
				Standby	Active	SOP	TSOP	
256K x 8	BB, AUTO	MT28LF002	90, 100, 120	120µA	30mA	-	40	2-1
128K x 16/ 256K x 8	BB, AUTO	MT28LF200	90, 100, 120	120µA	30mA	44	56	2-3
512K x 8	BB, AUTO	MT28LF004	90, 100, 120	120µA	30mA	-	40	2-5
256K x 16/ 512K x 8	BB, AUTO	MT28LF400	90, 100, 120	120µA	30mA	44	56	2-7
1 Meg x 8	SB, AUTO, DPD	MT28LF008	100, 150	120µA	30mA	44	40	2-31

BB = Boot Block, AUTO = Automated W/E Algorithm, SB = Symmetric Block, DPD = Deep Power Down

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5/12 VOLT FLASH MEMORY 1

3.3/12 VOLT FLASH MEMORY 2

PACKAGE INFORMATION 3

SALES INFORMATION 4

5/12 VOLT FLASH MEMORY PRODUCT SELECTION GUIDE

Memory Configuration	Features/ Options	Part Number	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins		Page
				Standby	Active	SOP	TSOP	
256K x 8	BB, AUTO	MT28F002	60, 80, 100	100µA	60mA	-	40	1-1
128K x 16/ 256K x 8	BB, AUTO	MT28F200	60, 80, 100	100µA	60mA	44	56	1-25
512K x 8	BB, AUTO	MT28F004	60, 80, 100	100µA	60mA	-	40	1-49
256K x 16/ 512K x 8	BB, AUTO	MT28F400	60, 80, 100	100µA	60mA	44	56	1-73
1 Meg x 8	SB, AUTO, DPD	MT28F008	80, 90, 100	100µA	50mA	44	40	1-97

BB = Boot Block, AUTO = Automated W/E Algorithm, SB = Symmetric Block, DPD = Deep Power Down

NEW ■ 5/12 VOLT FLASH MEMORY

FLASH MEMORY 256K x 8

5V/12V, BOOT BLOCK

FEATURES

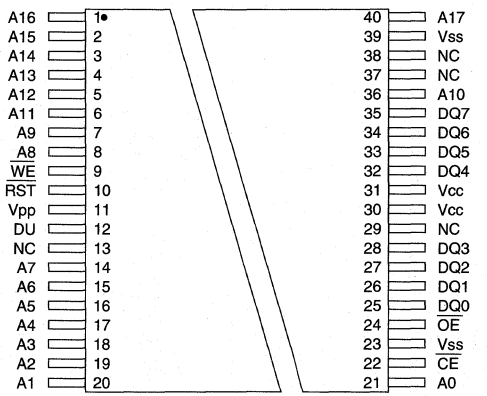
- Five erase blocks:
  - 16KB boot block (protected)
  - Two 8KB parameter blocks
  - One 96KB memory block
  - One 128KB memory block
- Low power: 100µA standby; 60mA active, MAX
- 5V±10% read; 12V±5% write/erase
- Address access times: 60ns, 80ns, 100ns
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 80ns access - 8
  - 100ns access -10
- Boot-Block Starting Address
  - Top (3FFFFH) T
  - Bottom (00000H) B
- Package
  - Plastic TSOP Type 1 (10 x 20mm) VG
- Part Number Example: MT28F002VG-8T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(FB-1)



GENERAL DESCRIPTION

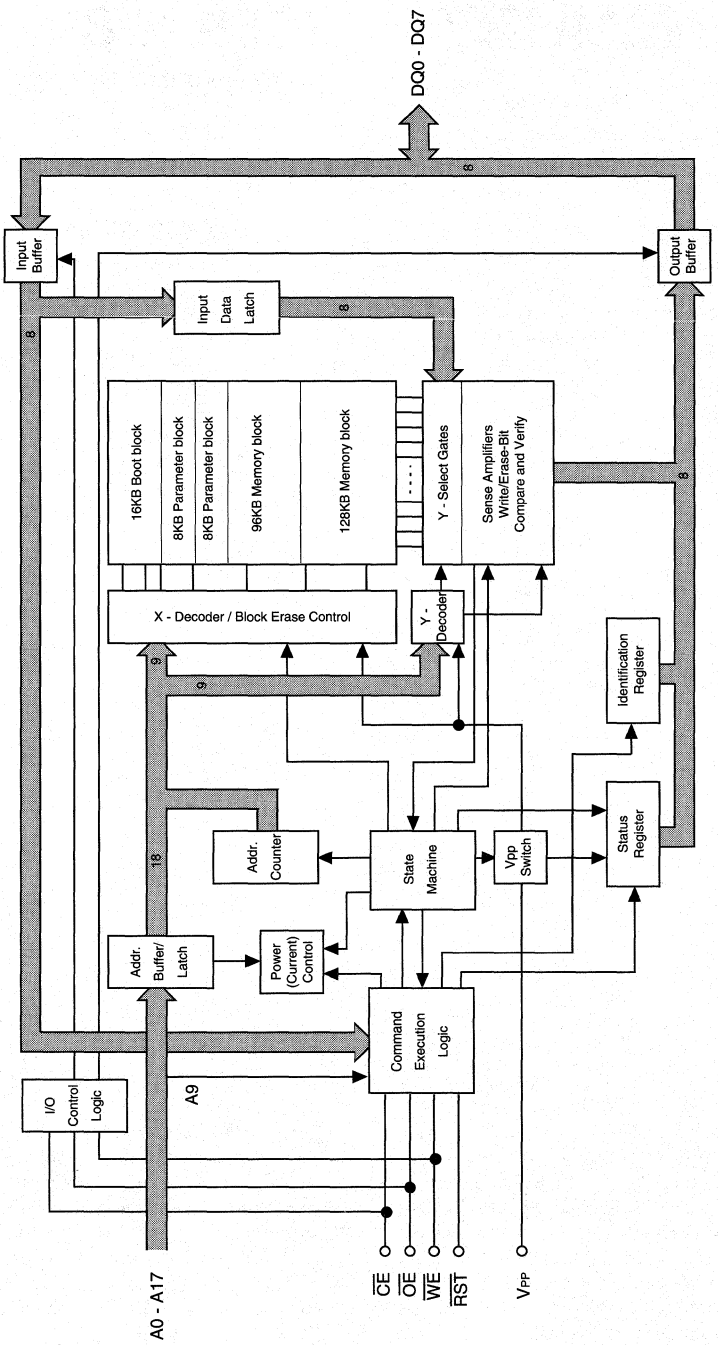
The MT28F002 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 2,097,152 bits organized as 262,144 by 8 bits. It is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F002 is organized into five separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F002 features a hardware-protected boot-block. Writing or erasing the boot block requires a super-voltage on the $\overline{RST}$ pin in addition to executing the normal write or block erase sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density, and are written-to and erased with no additional super-voltage required.

To read the array, the byte address is issued with $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH. Valid data is output until the next address is issued or until $\overline{CE}$ or $\overline{OE}$ go HIGH.

NEW ■ 5/12 VOLT FLASH MEMORY

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
9	$\overline{WE}$	Input	Write Enable: Determines if a given cycle is a write cycle. If $\overline{WE}$ = LOW when $V_{PP} < V_{PPH}$, the cycle is a write (command input) to the Command Execution Logic (CEL). If $\overline{WE}$ = LOW when $V_{PP} = V_{PPH}$, the cycle is a WRITE to one of the sectors or an ERASE CONFIRM.
22	$\overline{CE}$	Input	Chip Enable: Activates the device when LOW. When $\overline{CE}$ is HIGH, the device is disabled and goes into standby power mode.
10	$\overline{RST}$	Input	Reset: Clears the status register, sets the Internal State Machine (ISM) to the array read mode, and places the device in standby mode when LOW. All inputs, including $\overline{CE}$, are "don't care," and all outputs are High-Z. Also used to unlock boot block when brought to V_{HH} (boot-block unlock voltage; 12V). Must be held HIGH during all other modes of operation.
24	$\overline{OE}$	Input	Output Enable: Enables data output buffers.
21, 20, 19, 18, 17, 16, 15, 14, 8, 7, 36, 6, 5, 4, 3, 2, 1, 40	A0-A17	Input	Address Inputs: Selects a unique byte out of the 262,144 available.
25, 26, 27, 28, 32, 33, 34, 35	DQ0-DQ7	Input/ Output	Data I/O: Data output pins during any read operation, or data input pins during a WRITE. Used to input commands to the CEL for a command input.
13, 29, 37, 38	NC	-	No Connect: These pins may be driven or left unconnected.
12	DU	-	Don't Use: This pin must be left unconnected in the system.
11	V_{PP}	Supply	Write/Erase Supply Voltage: During a WRITE or ERASE CONFIRM, $V_{PP} = V_{PPH}$ (12V). V_{PP} = "don't care" during all other operations.
30, 31	V_{CC}	Supply	Power Supply: +5V ±10%
23, 39	V_{SS}	Supply	Ground

TRUTH TABLE [1]

FUNCTION	$\overline{RST}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A9	V_{PP}	DQ0-DQ7
Standby	H	H	X	X	X	X	X	High-Z
RESET	L	X	X	X	X	X	X	High-Z
READING								
Read	H	L	L	H	X	X	X	Data-Out
Output Disable	H	L	H	H	X	X	X	High-Z
WRITE/ERASE [2]								
ERASE SETUP	H	L	H	L	X	X	X	20H
ERASE CONFIRM [3]	H	L	H	L	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	10H/40H
WRITE [4]	H	L	H	L	X	X	V_{PPH}	Data-In
READ ARRAY	H	L	H	L	X	X	X	FFH
WRITE/ERASE (BOOT BLOCK) [2, 5]								
ERASE SETUP	H	L	H	L	X	X	X	20H
ERASE CONFIRM [3]	V_{HH}	L	H	L	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	10H/40H
WRITE [4]	V_{HH}	L	H	L	X	X	V_{PPH}	Data-In
READ ARRAY	H	L	H	L	X	X	X	FFH
DEVICE IDENTIFICATION [6, 7]								
Manufacturer (8-bit)	H	L	L	H	L	V_{ID}	X	2CH
Device (top boot)	H	L	L	H	H	V_{ID}	X	B6H
Device (bottom boot)	H	L	L	H	H	V_{ID}	X	B7H

NOTE: 1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. V_{PPH} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. V_{HH} = 12V.
6. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
7. A1-A8, A10-A17 = V_{IL}.

FUNCTIONAL DESCRIPTION

The MT28F002 Flash memory incorporates a number of features to make it ideally suited for system firmware.

The memory array is segmented into individual erase blocks. Each block may be erased without affecting data stored in other blocks. These memory blocks are read, written and erased by issuing commands to the Command Execution Logic (CEL). The CEL controls the operation of the Internal State Machine (ISM) that completely controls all write, block erase, and verify operations. This state machine protects each memory location from overerasure and optimizes each memory location for maximum data retention. In addition, the ISM greatly simplifies the control necessary for writing the device in-system or in an external programmer.

The Functional Description provides detailed information on the operation of the MT28F002, and is organized into these sections:

- Overview
- Memory Architecture
- Output (Read) Operations
- Input Operations
- Command Set
- ISM Status Register
- Command Execution
- Error Handling
- Write/Erase Cycle Endurance
- Power Usage
- Powerup

OVERVIEW

FIVE INDEPENDENTLY ERASABLE MEMORY BLOCKS

The MT28F002 is organized into five independently erasable memory blocks that allow portions of the memory to be erased without affecting the rest of the memory data. A special boot block is hardware-protected against inadvertent erasure or writes by a super-voltage pin. The voltage on this pin is required in addition to the 12V on the V_{PP} pin. The remaining blocks require only the 12V V_{PP} to be present in order to be changed.

HARDWARE-PROTECTED BOOT-BLOCK

This block of the memory array can be erased or written only when the $\overline{RST}$ pin is taken to V_{HH}. Designing a system so that the processor or control logic is unable to apply 12V to this pin will ensure data integrity in this memory block. This provides additional security for the core firmware during in-system firmware updates, should an unintentional power fluctuation or system reset occur. The MT28F002 is available in two versions; the MT28F002T addresses the boot block starting from 3FFFFH, and the MT28F002B addresses the boot block starting from 00000H.

INTERNAL STATE MACHINE (ISM)

Block erase and write timing are simplified by using an ISM to control all erase and write algorithms in the memory array. The ISM ensures protection against overerasure and optimizes write margin to each cell.

During write operations the ISM automatically increments and monitors write attempts, verifies write margin on each memory cell, and updates the ISM status register. When a block erase is performed the ISM automatically overwrites the entire addressed block (eliminates overerasure), increments and monitors erase attempts, and sets bits in the ISM status register.

ISM STATUS REGISTER

The ISM status register allows an external processor to monitor the status of the ISM during write and erase operations. Two bits of the 8-bit status register are set and cleared entirely by the ISM. These bits indicate whether the ISM is busy with an erase or write task, and when an erase has been suspended. Additional error information is set in the other three bits: valid programming voltage, write error, and erase error.

COMMAND EXECUTION LOGIC (CEL)

The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the read path (i.e. memory array, ID register, or status register). Commands may be issued to the CEL while the ISM is active. However, there are restrictions on what commands are allowed in this condition. See the Command Execution section for more detail.

MEMORY ARCHITECTURE

The MT28F002 memory array architecture is designed to allow sections to be erased without disturbing the rest of the array. The array is divided into five addressable "blocks" that are of varying size and independently erasable. By erasing in blocks, rather than the entire array, the total device endurance is enhanced, as is system flexibility. Only the erase function is block oriented. All read and write operations are done on a random byte basis.

The boot block is protected from unintentional erase or write with a hardware protection circuit that requires a super-voltage be applied before erasure is commenced. The boot block is intended for the core firmware required for basic system functionality. The remaining four blocks do not require this super-voltage before being written or erased.

BOOT BLOCK

The hardware-protected boot-block provides extra security for the most sensitive portions of the firmware. This 16KB block may only be erased or written when the $\overline{RST}$ pin is at the specified boot block unlock voltage (V_{HH}) of 12V. When performing erase or write cycles to this block, $\overline{RST}$ must be held at the unlock voltage (V_{HH}) until the erase or write is completed. As for any erase or write operations, the V_{PP} pin must be at V_{PPH} when writing to the boot block.

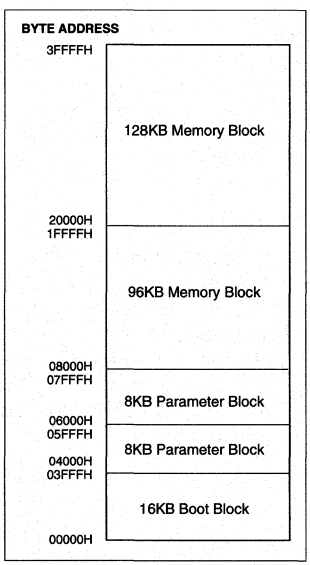
The MT28F002 is available in two configurations, top or bottom boot-block. The MT28F002T top boot-block version supports processors of the x86 variety. The MT28F002B bottom boot-block version is intended for 680X0 and RISC applications. Figure 1 illustrates the memory address maps associated with these two versions.

PARAMETER BLOCKS

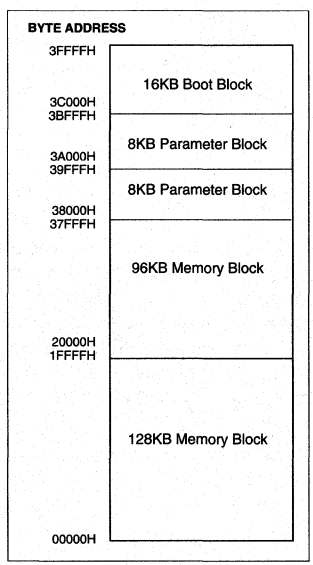
The two 8KB parameter blocks are used for storage of less sensitive and more frequently changing system parameters and also may include configuration or diagnostic coding. These blocks are enabled for erasure when the V_{PP} pin is at V_{PPH}. No super-voltage unlock is required.

GENERAL MEMORY BLOCKS

The two remaining blocks are general memory blocks and do not require a super-voltage on $\overline{RST}$ to be erased or written. These blocks are intended for code storage, or ROM-resident applications or operating systems that require in-system update capability.



Bottom Boot - MT28F002VG-xxB



Top Boot - MT28F002VG-xxT

Figure 1
MEMORY ADDRESS MAPS

OUTPUT (READ) OPERATIONS

The MT28F002 features three different types of reads. Depending on the current mode of the device, a read operation will produce data from the memory array, status register, or device identification register. In each of these three cases, the $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$ inputs are controlled in a similar manner to perform a read. However, several differences exist, and are described in the following section. Moving between modes to perform a specific read will be covered in the Command Execution section.

MEMORY ARRAY

To read the memory array, $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. Valid data will be output on the DQ pins once these conditions have been met and a valid address is given. Valid data will remain on the DQ pins until the address changes, or $\overline{OE}$ or $\overline{CE}$ go HIGH, whichever occurs first. The DQ pins will continue to output new data after each address transition, as long as $\overline{OE}$ and $\overline{CE}$ remain LOW.

After powerup or RESET, the device will automatically be in the array read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

STATUS REGISTER

Performing a read of the status register requires the same input sequencing as when reading the array, except that the address inputs are "don't care." Data from the status register is latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last. If the contents of the status register change during a read of the status register, either $\overline{OE}$ or $\overline{CE}$ may be toggled while the other is held LOW to update the output.

Following a write or erase, the device automatically enters the status register read mode. In addition, a read during a write or erase will produce the status register contents on DQ0-DQ7. When in the erase suspend mode, a read operation will produce the status register contents until another command is issued. While in certain other modes, READ STATUS REGISTER may be given to return to the status register read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

IDENTIFICATION REGISTER

A read of the two 8-bit device identification registers requires the same input sequencing as when reading the array. $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. A0 is used to decode between the two bytes of the device ID register; all other address inputs are "don't care." When A0 is LOW, the manufacturer ID is output, and when A0 is HIGH, the device ID is output.

To get to the identification register read mode, READ IDENTIFICATION may be issued while in certain other modes. In addition, the identification register read mode can be reached by applying a super-voltage (V_{ID}) to the A9 pin. Using this method, the ID register can be read while in any mode. Once A9 is returned to V_{IL} or V_{IH}, the device will return to the previous mode.

INPUT OPERATIONS

The DQ pins are used to either input data to the array or input a command to the CEL. A command input issues an 8-bit command to the CEL. Commands may be issued to control operation of the part. A WRITE is used to input data to the memory array. The following section describes both types of inputs. More information describing how to use the two types of inputs to write the device is provided in the Command Execution section.

COMMANDS

To perform a command input, $\overline{OE}$ must be HIGH, and $\overline{CE}$ and $\overline{WE}$ must be LOW. A0-A17 are not used for command inputs, except during an ERASE CONFIRM (described in a later section). The 8-bit command is input on DQ0-DQ7. The command is latched on the rising edge of $\overline{CE}$ ($\overline{CE}$ controlled) or $\overline{WE}$ ($\overline{WE}$ controlled), whichever occurs first.

MEMORY ARRAY

A write to the memory array sets the desired bits to logic 0's, but cannot change a given bit to a logic 1 from a logic 0. Setting any bits to a logic 1 requires that the entire block be erased. To perform a WRITE, $\overline{OE}$ must be HIGH, $\overline{CE}$ and $\overline{WE}$ must be LOW, and V_{PP} must be set to V_{PPH}. Writing to the boot block also requires that the $\overline{RST}$ pin be at V_{HH}. A0-A17 provide the address to be written, while the data to be written to the array is input on the DQ pins. The data and addresses are latched on the rising edge of $\overline{CE}$ ($\overline{CE}$-controlled) or $\overline{WE}$ ($\overline{WE}$-controlled), whichever occurs first. A WRITE must be preceeded by WRITE SETUP. Detail on how to input data to the array will be covered in the Write Sequence section.

COMMAND SET

To simplify writing of the memory blocks, the MT28F002 incorporates an ISM that controls all internal algorithms for the write and erase cycles. An 8-bit command set is used to control the device. Detail on how to sequence commands is provided in the Command Execution section. Table 1 lists the valid commands.

Table 1
COMMAND SET

COMMAND	HEX CODE	DESCRIPTION
RESERVED	00H	This command and all unlisted commands are invalid, and should not be called. These commands are reserved to allow for future feature enhancements.
READ ARRAY	FFH	Must be issued after any other command cycle before the array can be read. It is not necessary to issue this command after powerup or reset.
IDENTIFY DEVICE	90H	Allows the device and manufacturer ID to be read. A0 is used to decode between the manufacturer ID (A0=LOW) and device ID (A0=HIGH).
READ STATUS REGISTER	70H	Allows the status register to be read. Please refer to Table 2 for more information on the status register bits.
CLEAR STATUS REGISTER	50H	Clears status register bits 3 through 5, which cannot be cleared by the ISM.
ERASE SETUP	20H	The first command given in the two cycle erase sequence. The erase will not be completed unless followed by the ERASE CONFIRM command.
ERASE CONFIRM/RESUME	D0H	The second command given in the two cycle erase sequence. Must follow an ERASE SETUP command to be valid. Also used during an ERASE SUSPEND to resume the erase.
WRITE SETUP	40H or 10H	The first command given in the two cycle write sequence. The write data and address are given in the following cycle to complete the write.
ERASE SUSPEND	B0H	Halts the erase and puts device into the erase suspend mode. When in this mode only READ STATUS REGISTER, READ ARRAY and ERASE RESUME commands may be executed.

ISM STATUS REGISTER

The 8-bit ISM status register (see Table 2) is polled to check for write or erase completion or any related errors. During or following a write, erase, or erase suspend, a read operation will output the status register contents on DQ0 - DQ7 without prior command. While reading the status register contents, the outputs will not be updated if there is a change in the ISM status unless $\overline{OE}$ or $\overline{CE}$ is toggled. If the device is not in the write, erase, erase suspend, or status register read mode, READ STATUS REGISTER (70H) can be issued to view the status register contents.

All of the defined bits are set by the ISM, but only the ISM and erase suspend status bits are reset by the ISM. The erase, write and VPP status bits must be cleared using CLEAR STATUS REGISTER. If the VPP status bit (SR3) is set, the CEL will not allow further write or erase operations until the status register is cleared. This allows the user to choose when to poll and clear the status register. For example, the host system may perform multiple byte write operations before checking the status register, instead of checking after each individual write. Asserting the $\overline{RST}$ signal or powering down the device are other methods to clear the status register.

Table 2
STATUS REGISTER

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	ISM STATUS 1 = Ready 0 = Busy	The ISMS bit displays the active status of the state machine when performing write or block erase. The controlling logic polls this bit to determine when the erase and write status bits are valid.
SR6	ERASE SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed	Issuing an ERASE SUSPEND places the ISM in the suspend mode and sets this and the ISMS bit to "1." The ESS bit will remain "1" until an ERASE RESUME is issued.
SR5	ERASE STATUS 1 = Block erase error 0 = Successful block erase	ES is set to "1" after the maximum amount of erase cycles are executed by the ISM without a successful verify. ES is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR4	WRITE STATUS 1 = Write error 0 = Successful write	WS is set to "1" after the maximum amount of write cycles are executed by the ISM without a successful verify. WS is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR3	VPP STATUS 1 = No VPP voltage detected 0 = VPP present	VPPS detects the presence of a VPP voltage. It does not monitor VPP continously nor does it indicate a valid VPP voltage. The VPP pin is sampled for 12V after WRITE or ERASE CONFIRM is given. Must be cleared by CLEAR STATUS REGISTER or after a RESET.
SR0-2	RESERVED	Reserved for future use.

COMMAND EXECUTION

Commands are issued to bring the device into different operational modes. Each mode has specific operations that can be performed while in that mode. Several modes require a sequence of commands to be written before they are reached. The following section describes the properties of each mode and Table 3 lists all command sequences required to perform the desired operation.

READ ARRAY

The array read mode is the initial state of the device upon powerup, and is also entered after a RESET. If the device is in any other mode, READ ARRAY (FFH) must be given to return to the array read mode. Unlike the WRITE SETUP (40H), READ ARRAY does not need to be given before each individual read access.

IDENTIFY DEVICE

The 8-bit device identification may be read using one of two methods. IDENTIFY DEVICE (90H) may be written to the CEL to enter the identify device mode. While in this mode, any read will produce the device identification when A0 is HIGH and manufacturer identification when A0 is LOW. The device will remain in this mode until another command is given.

WRITE SEQUENCE

Two consecutive cycles are needed to input data to the array. WRITE SETUP (40H or 10H) is given in the first cycle. The next cycle is the WRITE, during which the write address and data are issued, and V_{PP} brought to V_{PPH}. Writing to the boot block also requires that the $\overline{RST}$ pin be brought to V_{HH} at the same time V_{PP} is brought to V_{PPH}. The ISM will now begin to write the byte. The desired bits within the byte will be set to logic 0. V_{PP} must be held at V_{PPH} until the write is completed (SR7 = 1). When writing to the boot block, $\overline{RST}$ must be held at V_{HH} until the ISM status bit (SR7) is set.

While the ISM executes the write, the ISM status bit (SR7) will be at 0, and the device will not respond to any commands. However, any read operation will produce the status register contents on DQ0-DQ7. When the ISM status bit (SR7) is set, the write has been completed, and the device will go into the status register read mode until another command is given.

Table 3
COMMAND SEQUENCES

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE			2ND CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY	1	Write	X	FFH				1
IDENTIFY DEVICE	3	Write	X	90H	Read	IA	ID	2, 3
READ STATUS REGISTER	2	Write	X	70H	Read	X	SRD	4
CLEAR STATUS REGISTER	1	Write	X	50H				
ERASE SETUP/CONFIRM	2	Write	X	20H	Write	BA	D0H	5
ERASE SUSPEND/RESUME	2	Write	X	B0H	Write	X	D0H	
WRITE SETUP/WRITE	2	Write	X	40H	Write	WA	WD	6
ALTERNATE WRITE	2	Write	X	10H	Write	WA	WD	6

NOTE:
1. Must follow WRITE or ERASE CONFIRM commands to the CEL in order to enable flash array read cycles.
2. IA = Identify address; 00H for manufacturer ID, 01H for device ID.
3. ID = Indentify data.
4. SRD = Status Register Data.
5. BA = Block address.
6. WA = Address to be written, WD = Data to be written to WA.

After the ISM has initiated the write, it cannot be aborted except by a RESET or by powering-down the part. Doing either during a write will corrupt the data being written. If only the WRITE SETUP command has been given, the write may be nullified by performing a null WRITE. To execute a null WRITE, FFH must be written . Once the ISM status bit (SR7) has been set, the device will be in the status register read mode until another command is issued.

ERASE SEQUENCE

Executing an erase sequence will set all bits within a block to logic 1. The command sequence necessary to execute an erase is similar to that of a write. To provide added security against accidental block erasure, two consecutive command cycles are required to initiate an erase of a block. In the first cycle, addresses are "don't care," and ERASE SETUP (20H) is given. In the second cycle, V_{PP} must be brought to V_{PPH}, an address within the block to be erased is issued, and ERASE CONFIRM (D0H) is given. If ERASE CONFIRM is not given, the ISM and erase status bits (SR7 and SR5) will be set, and the device will return to the array read mode.

At this time, the ISM will start the erase of the block. Any read operation will output the status register contents on DQ0-DQ7. V_{PP} must be held at V_{PPH} until the erase is completed (SR7 = 1). Once the erase is completed, the device will be in the status register read mode until another command is issued. Erasing the boot block also requires that the $\overline{RST}$ pin be set to V_{HH} at the same time V_{PP} is set to V_{PPH}.

ERASE SUSPENSION

The only command that may be issued while an erase is in progress is ERASE SUSPEND. This command allows other commands to be executed while pausing the erase in progress. Once the device has reached the erase suspend mode, the erase suspend status bit (SR6) will be set. The device may now be given a READ ARRAY, ERASE RESUME, or READ STATUS REGISTER. After the READ ARRAY command has been issued, any location not within the block being erased may be read. If the ERASE RESUME command is issued before SR6 has been set, the device will immediately proceed with the erase in progress. During the suspend mode V_{PP} must be held at V_{PPH}.

ERROR HANDLING

After the ISM status bit (SR7) has been set, the V_{PP} (SR3), write (SR4), and erase (SR5) status bits may be checked. If one or a combination of these three bits has been set, then an error has occurred. The ISM cannot reset these three bits. To clear these bits, the CLEAR STATUS REGISTER command (50H) must be given. If the V_{PP} status bit (SR3) is set, further write or erase operations cannot resume until the status register is cleared. Table 4 lists the combination of errors.

Table 4
STATUS REGISTER ERROR DECODE[1]

STATUS BITS			
SR5	SR4	SR3	ERROR DESCRIPTION
0	0	0	No errors
0	0	1	V_{PP} voltage error
0	1	0	Write error
0	1	1	Write error, V_{PP} voltage not valid at time of WRITE
1	0	0	Erase error
1	0	1	Erase error, V_{PP} voltage not valid at time of ERASE CONFIRM
1	1	0	Command sequencing error
1	1	1	Command sequencing error, programming voltage error

NOTE: 1. SR3 - SR5 must be cleared using CLEAR STATUS REGISTER.

WRITE/ERASE CYCLE ENDURANCE

The MT28F002 is designed and fabricated to meet advanced firmware storage requirements. To ensure this level of reliability, V_{PP} must be at 12V ±5% during write or erase cycles. Operation outside these limits may reduce the number of erase cycles that can be performed on the device. For further information on write and erase cycle endurance, refer to the Micron *Flash Reliability Monitor*.

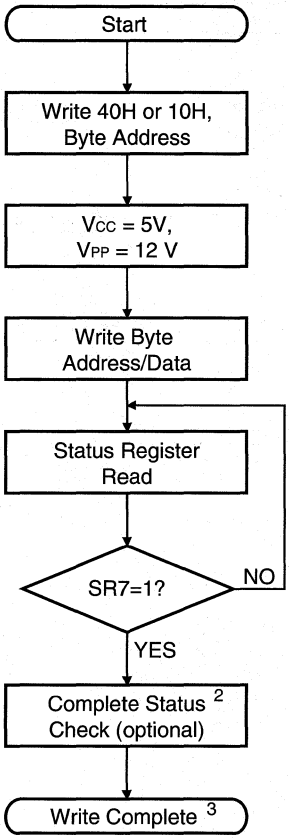
POWER USAGE

The MT28F002 offers several power saving features that may be utilized in the array read mode to conserve power. With $\overline{CE}$ LOW, the device will enter idle current mode when not being accessed. In this mode, the maximum I_{CC} current is 3mA. When $\overline{CE}$ is HIGH, the device will enter standby mode. In this mode, maximum I_{CC} current is 100µA. If $\overline{CE}$ is brought HIGH during an erase or write, the ISM will continue to operate, and the device will consume the respective active power until the write or erase is completed.

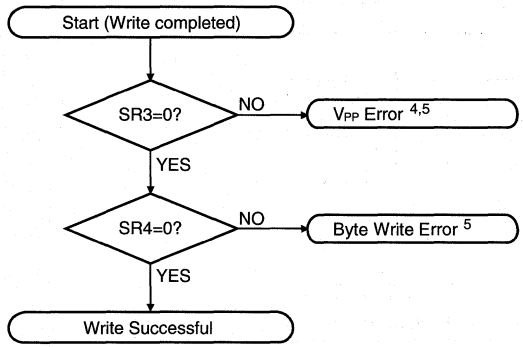
POWERUP

During a powerup, it is not necessary to sequence V_{CC} and V_{PP}. The likelihood of unwanted write or erase operations is minimized, since two consecutive cycles are required to execute either operation. However, $\overline{CE}$ or $\overline{WE}$ may be held HIGH, or $\overline{RST}$ can be held LOW during powerup for additional protection against unwanted write or erase operations. After a powerup or RESET, the status register is reset, and the device will enter the array read mode.

SELF-TIMED WRITE SEQUENCE[1]

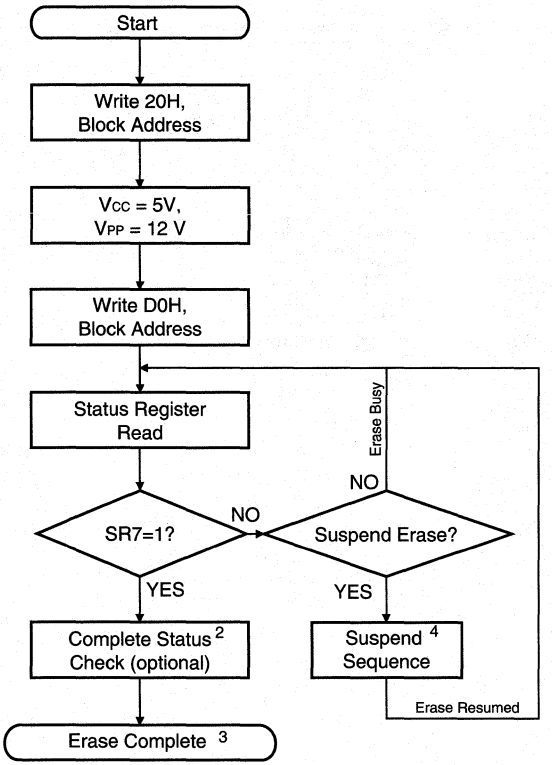


COMPLETE WRITE STATUS-CHECK SEQUENCE

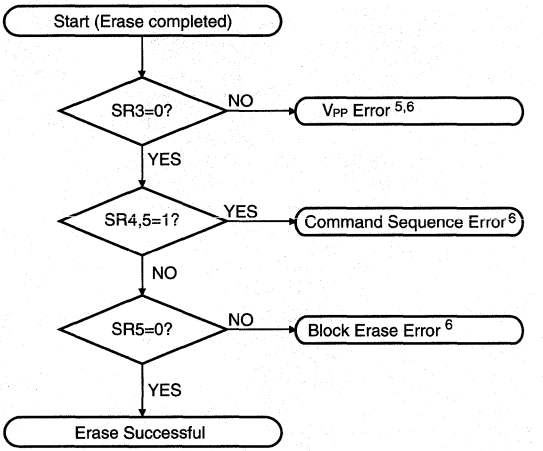


NOTE:
1. Sequence may be repeated for multiple writes.
2. Complete status check is not required. However, if SR3 = 1, further writes are inhibited until the status register is cleared.
3. Device will be in status register read mode. To return to the array read mode, the FFH command must be issued.
4. If SR3 is set during a write or erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
5. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

SELF-TIMED BLOCK ERASE SEQUENCE[1]

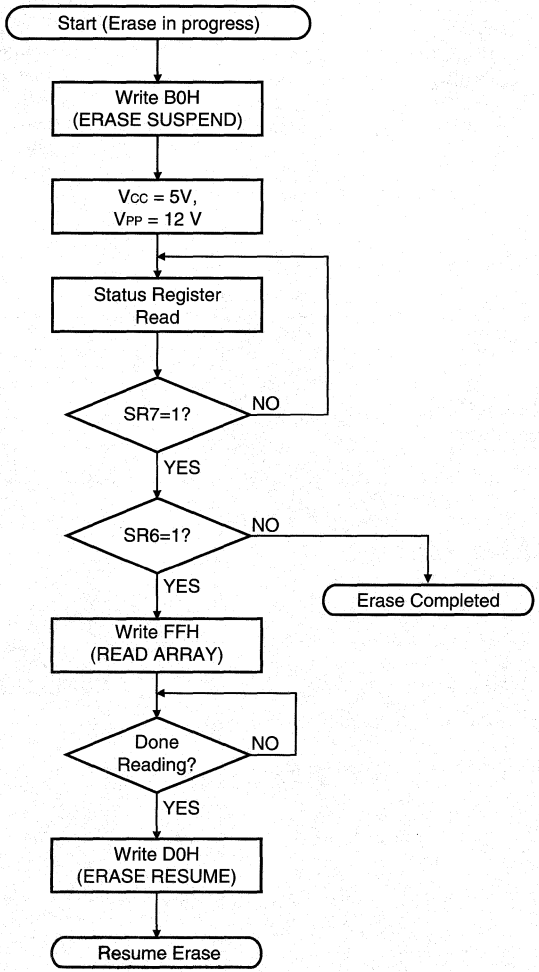


COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



NOTE:
1. Sequence may be repeated to erase multiple blocks.
2. Complete status check is not required. However, if SR3 = 1, further erases are inhibited until the status register is cleared.
3. To return to the array read mode, the FFH command must be issued.
4. Refer to the erase suspend flowchart for more information.
5. If SR3 is set during a write or erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
6. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

ERASE SUSPEND/RESUME SEQUENCE



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -0.5V to +7V
Input Voltage Relative to Vss ..... -0.5V to +7V**
V_{PP} Voltage Relative to Vss ..... -0.5V to +12.6V†
$\overline{RST}$/Pin A9 Voltage Relative to Vss .... -0.5V to +13.5V**,†
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Input and I/O pins may transition to -2.0V for < 20ns and Vcc +2.0V for < 20ns.
†Voltage may pulse to 14.0V ≤ 20ns.

RECOMMENDED DC OPERATING CONDITIONS

(0°C≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-0.5	0.8	V	1
Device Identification Voltage, A9	VID	11.4	13.0	V	1

DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS Output High Voltage (IOH = - 2.5 mA)	VOH	2.4		V	1
Output Low Voltage (IOL = 5.8 mA)	VOL		0.45	V	
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.4V ≤ A9 ≤ 13.0 = VID)	IID		500	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled; 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	

CAPACITANCE

(T_A = 25°C; Vcc = 5V ±10%; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	CI	8	pF	
Output Capacitance	CO	12	pF	

NOTE: 1. All voltages referenced to Vss.

READ AND STANDBY CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
READ CURRENT: TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}); $\overline{RST}$ = V_{IH}	I_{CC1}	60	mA	2, 3
READ CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 10 MHz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V); $\overline{RST}$ = V_{IH}	I_{CC2}	55	mA	2, 3
READ CURRENT: V_{PP} SUPPLY (V_{PP} > V_{CC})	I_{PP1}	200	µA	
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RST}$ = V_{IH}, or $\overline{RST}$ = V_{IL}; other inputs = V_{IL} or V_{IH})	I_{CC3}	1.5	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RST}$ = V_{CC} - 0.2V; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V)	I_{CC4}	100	µA	
STANDBY CURRENT: V_{PP} SUPPLY (V_{PP} ≤ V_{CC})	I_{PP2}	±15	µA	
IDLE CURRENT: TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 0 Hz; Other inputs = V_{IL} or V_{IH}; $\overline{RST}$ = V_{IH}; read array mode)	I_{CC5}	3	mA	
IDLE CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 0 Hz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V; $\overline{RST}$ = V_{IH}; READ ARRAY)	I_{CC6}	3	mA	

WRITE/ERASE CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
WRITE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC7}	65	mA	
WRITE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP3}	40	mA	
ERASE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC8}	30	mA	
ERASE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP4}	30	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%; erase suspended)	I_{CC9}	10	mA	4
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%; erase suspended)	I_{PP5}	200	µA	

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 10\%$)

AC CHARACTERISTICS		-6		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	70		80		100		ns	6
Access time from $\overline{CE}$	^tACE		70		80		100	ns	5,6
Access time from $\overline{OE}$	^tAOE		35		40		50	ns	5,6
Access time from address	^tAA		70		80		100	ns	6
$\overline{RST}$ HIGH to output valid delay	^tRWH		300		300		300	ns	6
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		25		30		40	ns	6
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		0		0		ns	6

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 5\%$)

AC CHARACTERISTICS		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	60		ns	7
Access time from $\overline{CE}$	^tACE		60	ns	5,7
Access time from $\overline{OE}$	^tAOE		30	ns	5,7
Access time from address	^tAA		60	ns	7
$\overline{RST}$ HIGH to output valid delay	^tRWH		300	ns	7
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		20	ns	7
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		ns	7

AC TEST CONDITION–1

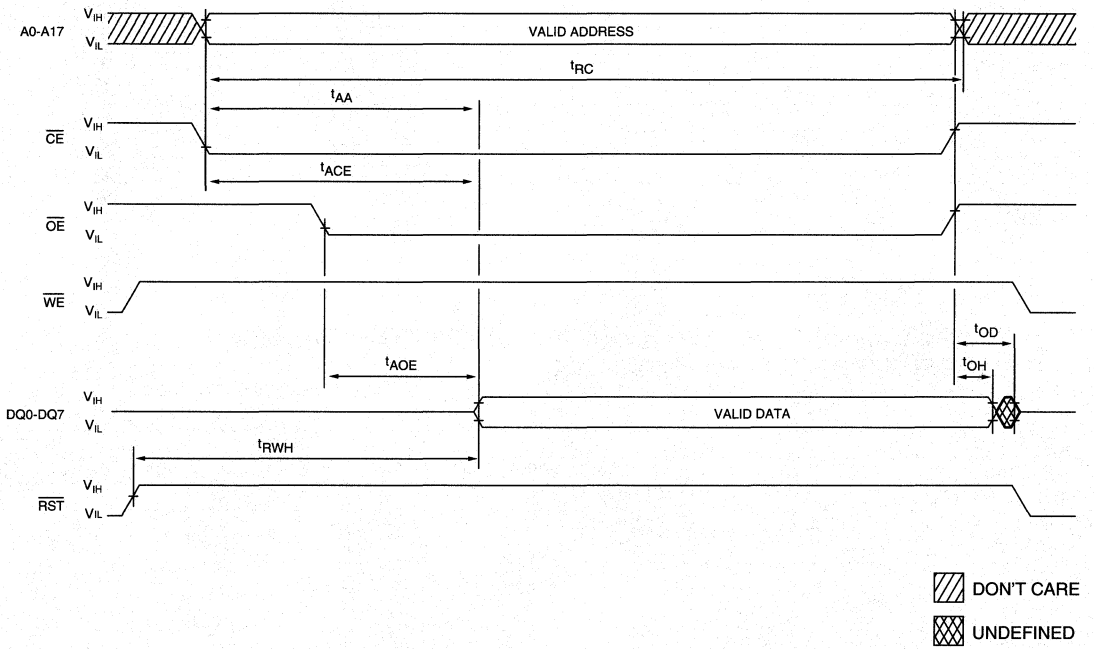
Input pulse levels	0.4 to 2.4V
Input rise and fall times	<10ns
Input timing reference level	0.8 V and 2.0 V
Output timing reference level	0.8 V and 2.0 V
Output load	1 TTL gate and C_L = 100 pF

AC TEST CONDITION–2

Input pulse levels	0.0 to 3.0V
Input rise and fall times	<10ns
Input timing reference level	1.5 V
Output timing reference level	1.5 V
Output load	1 TTL gate and C_L = 30 pF

NOTE:
1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on cycle rates.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Parameter is specified when device is not accessed. Actual current draw will be I_{CC9} plus read current if a read is executed while in erase suspend mode.
5. $\overline{OE}$ may be delayed by ^tACE minus ^tAOE after $\overline{CE}$ falls before ^tACE is affected.
6. Measurements tested under AC Test Condition-1.
7. Measurements tested under AC Test Condition-2.

READ CYCLE



RECOMMENDED DC WRITE/ERASE CONDITIONS

($0°C \le T_A \le +70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
V_{PP} voltage during normal operation	V_{PPL}	0.0	6.5	V	
V_{PP} voltage during erase/write operation	V_{PPH}	11.4	12.6	V	
Boot block unlock voltage	V_{HH}	11.4	13.0	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT: $\overline{RST}$ INPUT ($11.4 \le \overline{RST} \le 13.0V = V_{HH}$)	I_{HH}		500	µA	

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	70		80		100		ns	1
$\overline{WE}$ HIGH pulse width	^tWPH	20		20		30		ns	1
$\overline{CE}$ HIGH pulse width	^tCPH	20		20		30		ns	1

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	60		ns	2
$\overline{WE}$ HIGH pulse width	^tWPH	10		ns	2
$\overline{CE}$ HIGH pulse width	^tCPH	10		ns	2

NOTE: 1. Measurements tested under AC Test Condition-1.
2. Measurements tested under AC Test Condition-2.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{WE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10% or ±5%)

AC CHARACTERISTICS		-6, -8, -10			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{WE}$ HIGH	^tAS	50		ns	
Address hold time from $\overline{WE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{WE}$ HIGH	^tDS	50		ns	
Data hold time from $\overline{WE}$ HIGH	^tDH	0		ns	
$\overline{CE}$ setup time to $\overline{WE}$ LOW	^tCS	0		ns	
$\overline{CE}$ hold time from $\overline{WE}$ HIGH	^tCH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	100		ns	1
$\overline{WE}$ pulse width	^tWP	50		ns	
$\overline{RST}$ HIGH to $\overline{WE}$ LOW delay	^tRS	220		ns	
$\overline{RST}$ V_{HH} setup time to $\overline{WE}$ HIGH	^tRHS	100		ns	2
Write duration	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		100	ns	3

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{CE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10% or ±5%)

AC CHARACTERISTICS		-6, -8, -10			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{CE}$ HIGH	^tAS	50		ns	
Address hold time from $\overline{CE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{CE}$ HIGH	^tDS	50		ns	
Data hold time from $\overline{CE}$ HIGH	^tDH	0		ns	
$\overline{WE}$ setup time to $\overline{CE}$ LOW	^tWS	0		ns	
$\overline{WE}$ hold time from $\overline{CE}$ HIGH	^tWH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	100		ns	1
$\overline{CE}$ pulse width	^tCP	50		ns	
$\overline{RST}$ HIGH to $\overline{CE}$ LOW delay	^tRS	220		ns	
$\overline{RST}$ V_{HH} setup time to $\overline{CE}$ HIGH	^tRHS	100		ns	2
Write duration	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1, 2
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		100	ns	2

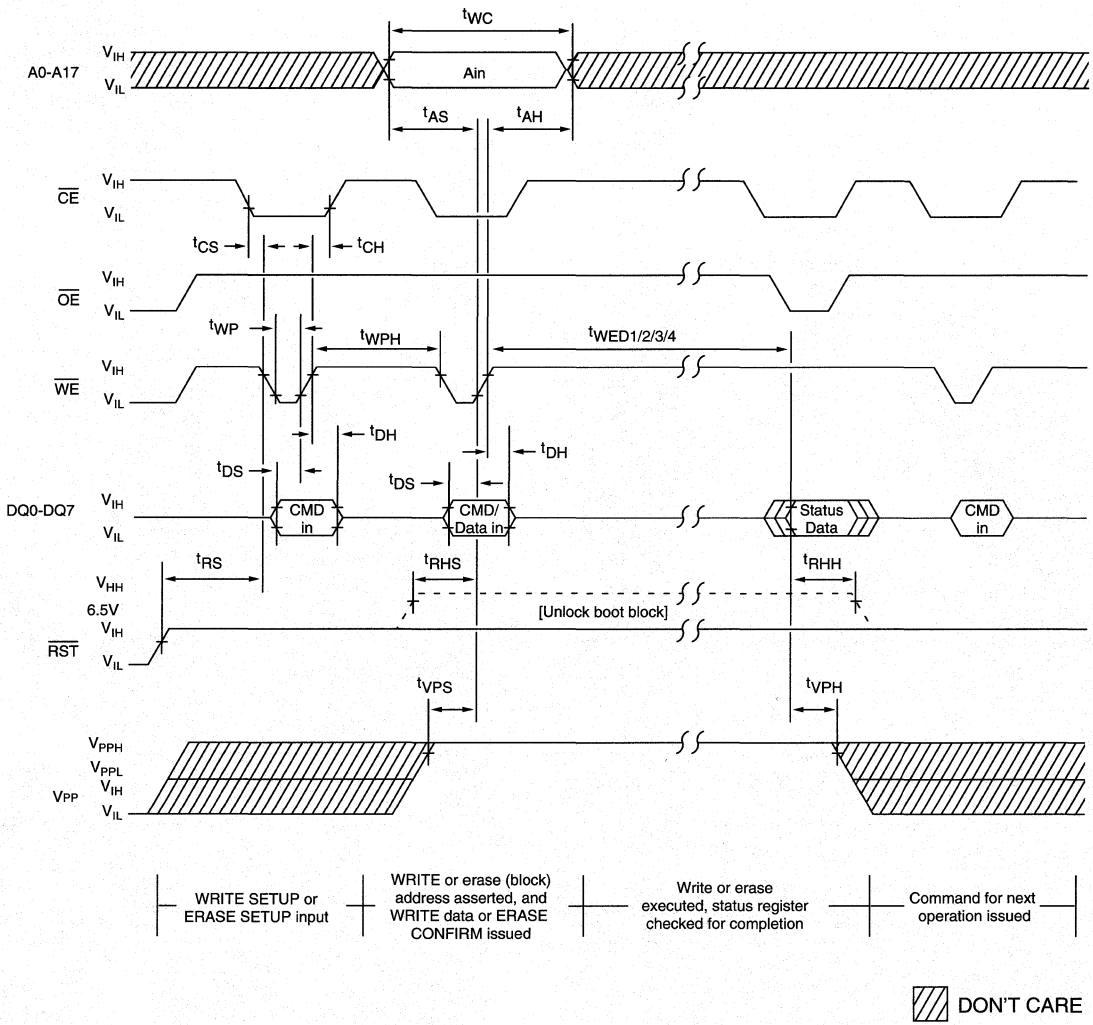
NOTE: 1. Write/erase times are measured to valid status register data (SR7=1).
2. $\overline{RST}$ should be held at V_{HH} until boot-block write or erase is complete.
3. ^tREL is required to relock boot block after write or erase to boot block.

WRITE AND ERASE DURATION CHARACTERISTICS

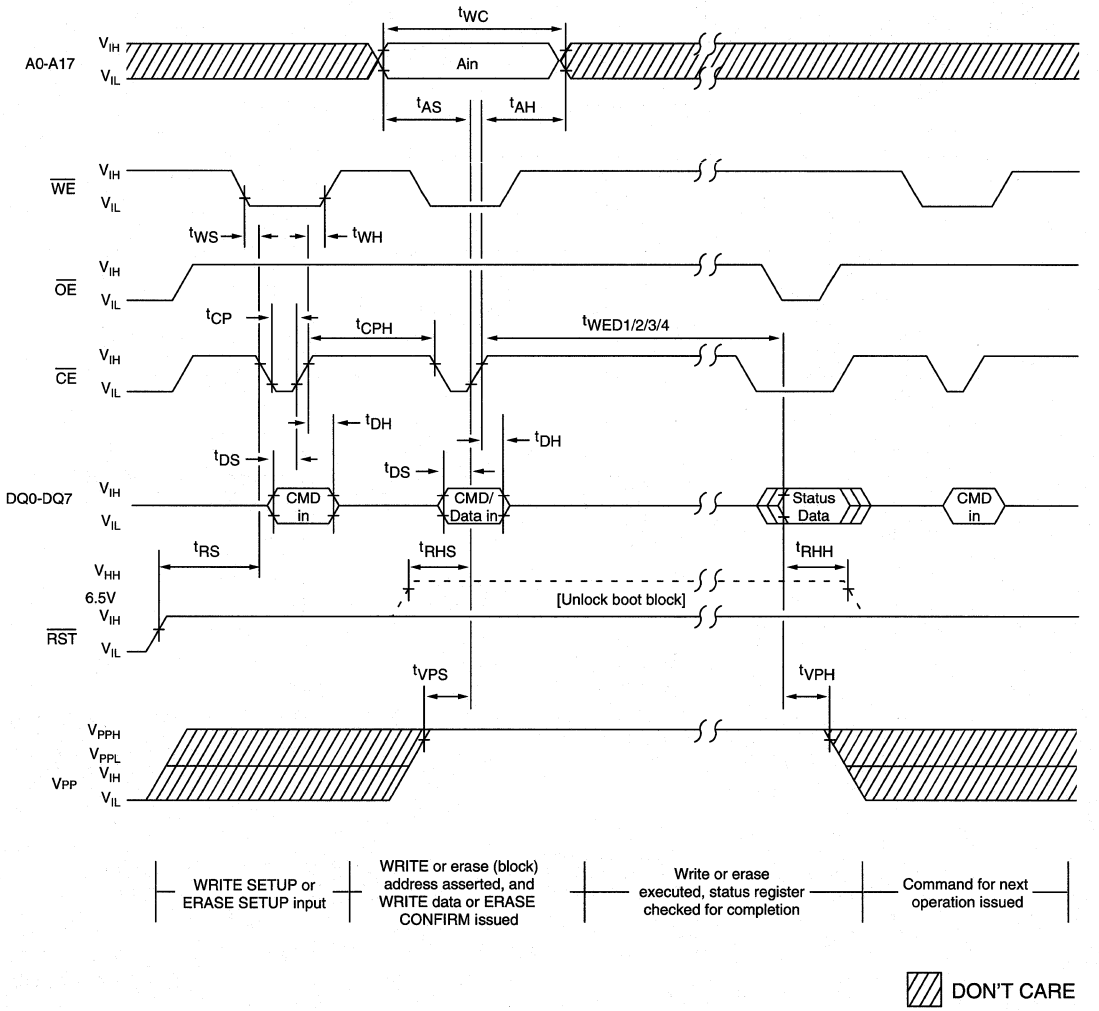
PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Boot/parameter block erase time		1.0	7.0	s	1
Main block erase time		2.5	14.0	s	1
Main block write time		1.0	4.0	s	1, 2

NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.

ERASE/WRITE CYCLE
$\overline{WE}$-CONTROLLED WRITE/ERASE



ERASE/WRITE CYCLE
$\overline{CE}$-CONTROLLED WRITE/ERASE



NEW 5/12 VOLT FLASH MEMORY

FLASH MEMORY

128K x 16, 256K x 8

5V/12V, BOOT BLOCK

FEATURES

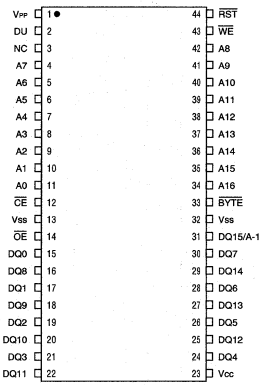
- Five erase blocks:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - One 96KB/48K-word memory block
  - One 128KB/64K-word memory block
- Low power: 100µA standby; 60mA active, MAX
- 5V±10% read; 12V±5% write/erase
- Address access times: 60ns, 80ns, 100ns
- Selectable organizations: 131,072 x 16 or 262,144 x 8
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm
- Byte- or word-wide write
- TSOP packaging option

OPTIONS — MARKING

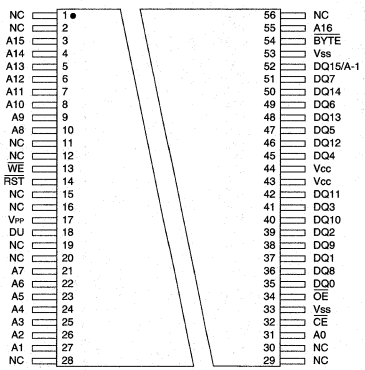
- Timing
  - 60ns access - 6
  - 80ns access - 8
  - 100ns access -10
- Boot-Block Starting Address
  - Top (1FFFFH) T
  - Bottom (00000H) B
- Packages
  - Plastic SOP (600 mil) SG
  - Plastic TSOP Type 1 (14 x 20mm) VG
- Part Number Example: MT28F200SG-8T

PIN ASSIGNMENT (Top View)

44-Pin SOP (FA-1)



56-Pin TSOP Type I (FB-2)



GENERAL DESCRIPTION

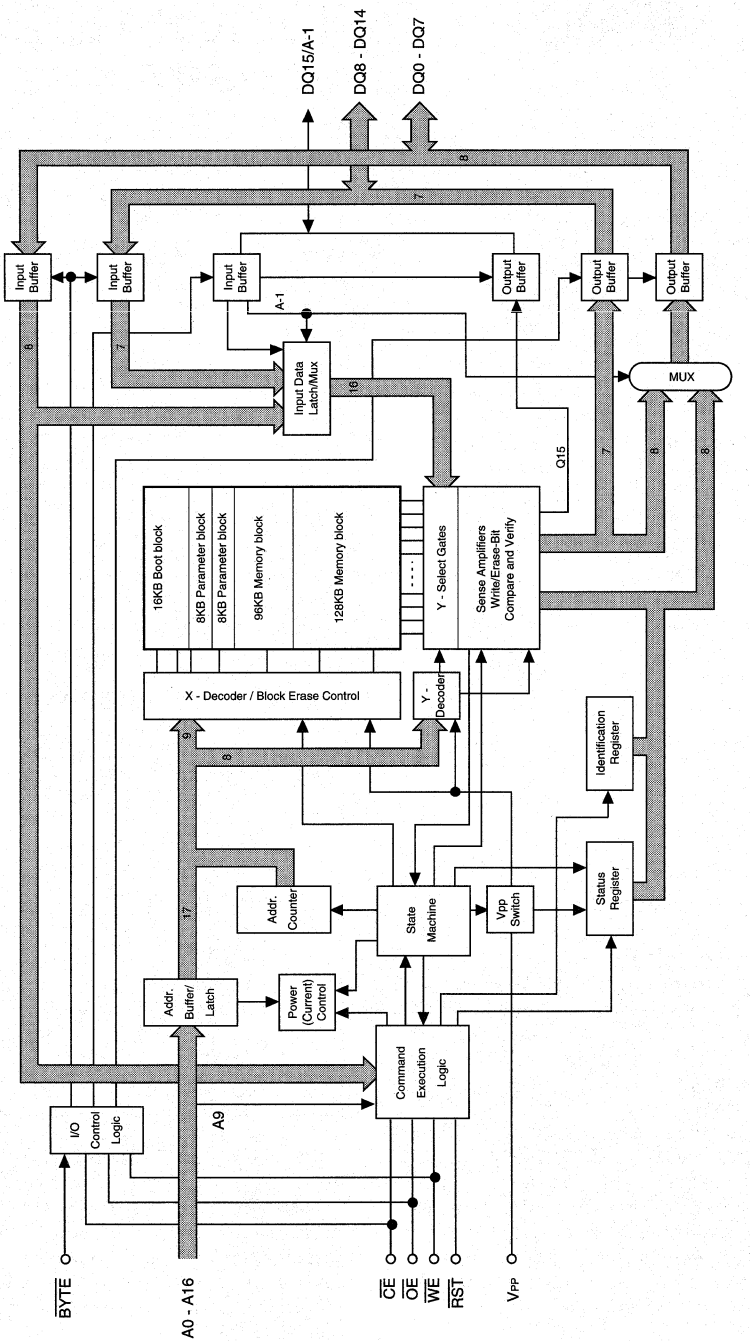
The MT28F200 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 2,097,152 bits organized as 131,072 words by 16 bits or 262,144 words by 8 bits. It is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F200 is organized into five separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F200 features a hardware-protected boot-block. Writing or erasing the boot block requires a super-voltage on the $\overline{RST}$ pin in addition to executing the normal write or erase sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density, and are written-to and erased with no additional super-voltage required.

The byte or word address is issued to read the memory array with $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH. Valid data is output until the next address is issued. The $\overline{BYTE}$ pin is used to switch the data path between 8 bits wide and 16 bits wide. When $\overline{BYTE}$ is LOW, the dual-use pin DQ15/A-1 becomes the lowest order address bit (A-1). When $\overline{BYTE}$ is HIGH, the DQ15/A-1 pin becomes the most significant data bit (DQ15).

NEW ■ 5/12 VOLT FLASH MEMORY

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
43	13	$\overline{WE}$	Input	Write Enable: Determines if a given cycle is a write cycle. If $\overline{WE}$ = LOW when $V_{PP} < V_{PPH}$, the cycle is a write (command input) to the Command Execution Logic (CEL). If $\overline{WE}$ = LOW when $V_{PP} = V_{PPH}$, the cycle is a WRITE to one of the sectors or an ERASE CONFIRM.
12	32	$\overline{CE}$	Input	Chip Enable: Activates the device when LOW. When $\overline{CE}$ is HIGH, the device is disabled and goes into standby power mode.
44	14	$\overline{RST}$	Input	Reset: Clears the status register, sets the Internal State Machine (ISM) to the array read mode, and places the device in standby mode when LOW. All inputs, including $\overline{CE}$, are "don't care," and all outputs are High-Z. Also used to unlock boot block when brought to V_{HH} (boot-block unlock voltage; 12V). Must be held HIGH during all other modes of operation.
14	34	$\overline{OE}$	Input	Output Enable: Enables data output buffers.
33	54	$\overline{BYTE}$	Input	Byte Enable: If $\overline{BYTE}$=HIGH the upper byte is active through DQ8-DQ15. If $\overline{BYTE}$=LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34	31, 27, 26, 25, 24, 23, 22, 21, 10, 9, 8, 7, 6, 5, 4, 3, 55	A0-A16	Input	Address Inputs: Selects a unique, 16-bit word out of the 131,072 available. The DQ15/A-1 input becomes the lowest order address when $\overline{BYTE}$=LOW to allow for selection of an 8-bit byte from 262,144 available.
31	52	DQ15/A-1	Input/ Output	Data I/O: MSB of data when $\overline{BYTE}$ = HIGH. Address Input: LSB of address input when $\overline{BYTE}$ = LOW during read or write operation. Not used during erase or read device ID.
15, 17, 19, 21, 24, 26, 28, 30	35, 37, 39, 41, 45, 47, 49, 51	DQ0-DQ7	Input/ Output	Data I/O: Data output pins during any read operation, or data input pins during a WRITE. Used to input commands to the CEL or a command input.
16, 18, 20, 22, 25, 27, 29	36, 38, 40, 42, 46, 48, 50	DQ8-DQ14	Input/ Output	Data I/O: Data output pins during any read operation or data input pins during a WRITE when $\overline{BYTE}$ = HIGH. High-Z when $\overline{BYTE}$ is LOW.
3	1, 2, 11, 12, 15, 16, 19, 20, 28, 29, 30, 56	NC	-	No Connect: These pins may be driven or left unconnected.
2	18	DU	-	Don't Use: This pin must be left unconnected in the system.
1	17	V_{PP}	Supply	Write/Erase Supply Voltage: During a WRITE or ERASE CONFIRM, $V_{PP} = V_{PPH}$ (12V). V_{PP} = "don't care" during all other operations.
23	43, 44	V_{CC}	Supply	Power Supply: +5V ±10%
13, 32	33, 53	V_{SS}	Supply	Ground

TRUTH TABLE [1]

FUNCTION	$\overline{RST}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READING											
16-bit Read	H	L	L	H	H	X	X	X	Data-Out	Data-Out	Data-Out
8-bit Read	H	L	L	H	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE [2, 3]											
ERASE SETUP	H	L	H	L	X	X	X	X	20H	X	X
ERASE CONFIRM [4]	H	L	H	L	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H	X	X
16-bit WRITE [5]	H	L	H	L	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
8-bit WRITE [5]	H	L	H	L	L	X	X	V_{PPH}	Data-In	High-Z	A-1
READ ARRAY	H	L	H	L	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK) [2, 3, 6]											
ERASE SETUP	H	L	H	L	X	X	X	X	20H	X	X
ERASE CONFIRM [4]	V_{HH}	L	H	L	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H	X	X
16-bit WRITE [5]	V_{HH}	L	H	L	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
8-bit WRITE [5]	V_{HH}	L	H	L	L	X	X	V_{PPH}	Data-In	High-Z	A-1
READ ARRAY	H	L	H	L	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION [7, 8]											
Manufacturer (16-bit) [2]	H	L	L	H	H	L	V_{ID}	X	2CH	00H	-
Manufacturer (8-bit)	H	L	L	H	L	L	V_{ID}	X	2CH	High-Z	X
Device (16-bit, top boot) [2]	H	L	L	H	H	H	V_{ID}	X	B4H	22H	-
Device (8-bit, top boot)	H	L	L	H	L	H	V_{ID}	X	B4H	High-Z	X
Device (16-bit, bottom boot) [2]	H	L	L	H	H	H	V_{ID}	X	B5H	22H	-
Device (8-bit, bottom boot)	H	L	L	H	L	H	V_{ID}	X	B5H	High-Z	X

NOTE:
1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. Value reflects DQ8-DQ15.
3. V_{PPH} = 12V.
4. Operation must be preceded by ERASE SETUP command.
5. Operation must be preceded by WRITE SETUP command.
6. V_{HH} = 12V.
7. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
8. A1-A8, A10-A16 = V_{IL}.

FUNCTIONAL DESCRIPTION

The MT28F200 Flash memory incorporates a number of features to make it ideally suited for system firmware.

The memory array is segmented into individual erase blocks. Each block may be erased without affecting data stored in other blocks. These memory blocks are read, written and erased by issuing commands to the Command Execution Logic (CEL). The CEL controls the operation of the Internal State Machine (ISM) that completely controls all write, block erase, and verify operations. This state machine protects each memory location from over-erasure and optimizes each memory location for maximum data retention. In addition, the ISM greatly simplifies the control necessary for writing the device in-system or in an external programmer.

The Functional Description provides detailed information on the operation of the MT28F200, and is organized into these sections:

- Overview
- Memory Architecture
- Output (Read) Operations
- Input Operations
- Command Set
- ISM Status Register
- Command Execution
- Error Handling
- Write/Erase Cycle Endurance
- Power Usage
- Powerup

OVERVIEW

FIVE INDEPENDENTLY ERASABLE MEMORY BLOCKS

The MT28F200 is organized into five independently erasable memory blocks that allow portions of the memory to be erased without affecting the rest of the memory data. A special boot block is hardware-protected against inadvertent erasure or writes by a super-voltage pin. The voltage on this pin is required in addition to the 12V on the V_{PP} pin. The remaining blocks require only the 12V V_{PP} to be present in order to be changed.

HARDWARE-PROTECTED BOOT-BLOCK

This block of the memory array can be erased or written only when the $\overline{RST}$ pin is taken to V_{HH}. Designing a system so that the processor or control logic is unable to apply 12V to this pin will ensure data integrity in this memory block. This provides additional security for the core firmware during in-system firmware updates, should an unintentional power fluctuation or system reset occur. The MT28F200 is available in two versions; the MT28F200T addresses the boot block starting from 1FFFFH, and the MT28F200B addresses the boot block starting from 00000H.

CONFIGURABLE BUS SIZE

The MT28F200T/B allows dynamic selection of an 8-bit (256K x 8) or 16-bit (128K x 16) data bus for reading and writing the memory. The $\overline{BYTE}$ pin is used to select the bus width. When in the x16 configuration, control data is read or written only on the lower 8 bits (DQ0-DQ7).

Data written to the memory array utilize all active data pins for the selected configuration. When the x8 configuration is selected, data is written in byte form; when in the x16 configuration, data is written in the word form.

INTERNAL STATE MACHINE (ISM)

Block erase and byte/word write timing are simplified by using an ISM to control all erase and write algorithms in the memory array. The ISM ensures protection against overerasure and optimizes write margin to each cell.

During write operations the ISM automatically increments and monitors write attempts, verifies write margin on each memory cell, and updates the ISM status register. When block erase is performed the ISM automatically overwrites the entire addressed block (eliminates over erasure), increments and monitors erase attempts, and sets bits in the ISM status register.

ISM STATUS REGISTER

The ISM status register allows an external processor to monitor the status of the ISM during write and erase operations. Two bits of the 8-bit status register are set and cleared entirely by the ISM. These bits indicate whether the ISM is busy with an erase or write task, and when an erase has been suspended. Additional error information is set in the other three bits: valid programming voltage, write error, and erase error.

COMMAND EXECUTION LOGIC (CEL)

The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the read path (i.e. memory array, ID register, or status register). Commands may be issued to the CEL while the ISM is active. However, there are restrictions on what commands are allowed in this condition. See the Command Execution section for more detail.

MEMORY ARCHITECTURE

The MT28F200 memory array architecture is designed to allow sections to be erased without disturbing the rest of the array. The array is divided into five addressable "blocks" that are of varying size and independently erasable. By erasing in blocks, rather than the entire array, the total device endurance is enhanced, as is system flexibility. Only the erase function is block oriented. All read and write operations are done on a random word- or byte-basis.

The boot block is protected from unintentional erase or write with a hardware protection circuit that requires a super-voltage be applied before erasure is commenced. The boot block is intended for the core firmware required for basic system functionality. The remaining four blocks do not require this super-voltage before being written or erased.

BOOT BLOCK

The hardware-protected boot-block provides extra security for the most sensitive portions of the firmware. This 16KB block may only be erased or written when the $\overline{RST}$ pin is at the specified boot block unlock voltage (V_{HH}) of 12V. When performing erase or write cycles to this block, $\overline{RST}$ must be held at the unlock voltage (V_{HH}) until the erase or write is completed. As for any erase or write operations, the V_{PP} pin must be at V_{PPH} when writing to the boot block.

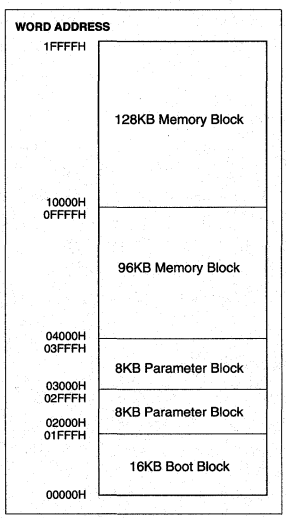
The MT28F200 is available in two configurations, top or bottom boot-block. The MT28F200T top boot-block version supports processors of the x86 variety. The MT28F200B bottom boot-block version is intended for 680X0 and RISC applications. Figure 1 illustrates the memory address maps associated with these two versions.

PARAMETER BLOCKS

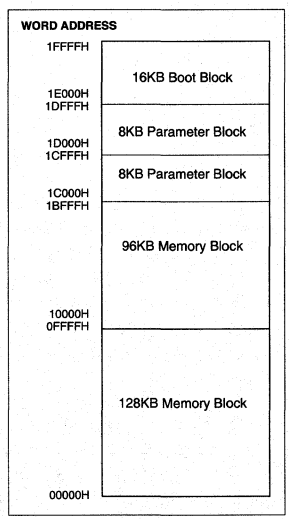
The two 8KB parameter blocks are used for storage of less sensitive and more frequently changing system parameters and also may include configuration or diagnostic coding. These blocks are enabled for erasure when the V_{PP} pin is at V_{PPH}. No super-voltage unlock is required.

GENERAL MEMORY BLOCKS

The two remaining blocks are general memory blocks and do not require a super-voltage on $\overline{RST}$ to be erased or written. These blocks are intended for code storage, or ROM-resident applications or operating systems that require in-system update capability.



Bottom Boot - MT28F200xx-xxB



Top Boot - MT28F200xx-xxT

Figure 1
MEMORY ADDRESS MAPS

OUTPUT (READ) OPERATIONS

The MT28F200 features three different types of reads. Depending on the current mode of the device, a read operation will produce data from the memory array, status register, or device identification register. In each of these three cases, the $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$ inputs are controlled in a similar manner to perform a read. However, several differences exist, and are described in the following section. Moving between modes to perform a specific read will be covered in the Command Execution section.

MEMORY ARRAY

To read the memory array, $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. Valid data will be output on the DQ pins once these conditions have been met and a valid address is given. Valid data will remain on the DQ pins until the address changes, or $\overline{OE}$ or $\overline{CE}$ go HIGH, whichever occurs first. The DQ pins will continue to output new data after each address transition, as long as $\overline{OE}$ and $\overline{CE}$ remain LOW.

The MT28F200 features dynamically sizable bus widths. When configured as 128K x 16 ($\overline{BYTE}$ is HIGH), data will be output on DQ0-DQ15. To configure the memory array as a 256K x 8, $\overline{BYTE}$ must be LOW. DQ8 - DQ14 are now "High-Z," and all data is output on DQ0-DQ7. The DQ15/A-1 pin now becomes the lowest order address input, so that 262,144 locations can be read.

After powerup or RESET, the device will automatically be in the array read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

STATUS REGISTER

Performing a read of the status register requires the same input sequencing as when reading the array, except that the address inputs are "don't care." The status register contents are always output on DQ0-DQ7, regardless of the condition of $\overline{BYTE}$. DQ8-DQ15 are LOW when $\overline{BYTE}$ is HIGH, and DQ8-DQ14 are High-Z when $\overline{BYTE}$ is LOW. Data from the status register is latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last. If the contents of the status register change during a read of the status register, either $\overline{OE}$ or $\overline{CE}$ may be toggled while the other is held LOW to update the output.

Following a write or erase, the device automatically enters the status register read mode. In addition, a read during a write or erase will produce the status register contents on DQ0-DQ7. When in the erase suspend mode, a read operation will produce the status register contents until another command is issued. While in certain other modes, the READ STATUS REGISTER command may be given to return to the status register read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

IDENTIFICATION REGISTER

A read of the two 8-bit device identification registers requires the same input sequencing as when reading the array. $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. However, ID register data is output only on DQ0-DQ7, regardless of the condition of $\overline{BYTE}$. A0 is used to decode between the two bytes of the device ID register; all other address inputs are "don't care." When A0 is LOW, the manufacturer ID is output, and when A0 is HIGH, the device ID is output. DQ8-DQ15 are "High-Z" when $\overline{BYTE}$ is LOW. When $\overline{BYTE}$ is HIGH, DQ8-DQ15 is 00H when the manufacturer ID is read, and 22H when the device ID is read.

To get to the identification register read mode, READ IDENTIFICATION command may be issued while in certain other modes. In addition, the identification register read mode can be reached by applying a super-voltage (V_{ID}) to the A9 pin. Using this method, the ID register can be read while in any mode. Once A9 is returned to V_{IL} or V_{IH}, the device will return to the previous mode.

INPUT OPERATIONS

The DQ pins are used to either input data to the array or input a command to the CEL. A command input issues an 8-bit command to the CEL. Commands may be issued to control operation of the part. A WRITE is used to input data to the memory array. The following section describes both types of inputs. More information describing how to use the two types of inputs to write the device is provided in the Command Execution section.

COMMANDS

To perform a command input, $\overline{OE}$ must be HIGH, and $\overline{CE}$ and $\overline{WE}$ must be LOW. A0-A16 are not used for command inputs, except during an ERASE CONFIRM (described in a later section). The 8-bit command is input on DQ0-DQ7, while DQ8-DQ15 are "don't care." The command is latched on the rising edge of $\overline{CE}$ ($\overline{CE}$ controlled) or $\overline{WE}$ ($\overline{WE}$ controlled), whichever occurs first. The condition of $\overline{BYTE}$ has no effect on a command input.

MEMORY ARRAY

A write to the memory array sets the desired bits to logic 0's, but cannot change a given bit to a logic 1 from a logic 0. Setting any bits to a logic 1 requires that the entire block be erased. To perform a WRITE, $\overline{OE}$ must be HIGH, $\overline{CE}$ and $\overline{WE}$ must be LOW, and V_{PP} must be set to V_{PPH}. Writing to

the boot block also requires that the $\overline{RST}$ pin be at V_{HH}. A0-A16 provide the address to be written, while the data to be written to the array is input on the DQ pins. The data and addresses are latched on the rising edge of $\overline{CE}$ ($\overline{CE}$-controlled) or $\overline{WE}$ ($\overline{WE}$-controlled), whichever occurs first. A WRITE must be preceeded by a WRITE SETUP command. Detail on how to input data to the array will be covered in the Write Sequence section.

Dynamic bus sizing applies to writes as it does for reads. When $\overline{BYTE}$ is LOW (BYTE mode), data is input on DQ0-DQ7, DQ8-DQ14 are "High-Z," and DQ15 becomes the lowest order address input. To WRITE in x16 (WORD) mode, $\overline{BYTE}$ is HIGH, and data is input on DQ0-DQ15.

COMMAND SET

To simplify writing of the memory blocks, the MT28F200 incorporates an ISM that controls all internal algorithms for the write and erase cycles. An 8-bit command set is used to control the device. Detail on how to sequence commands is provided in the Command Execution section. Table 1 lists the valid commands.

Table 1
COMMAND SET

COMMAND	HEX CODE	DESCRIPTION
RESERVED	00H	This command and all unlisted commands are invalid, and should not be called. These commands are reserved to allow for future feature enhancements.
READ ARRAY	FFH	Must be issued after any other command cycle before the array can be read. It is not necessary to issue this command after powerup or reset.
IDENTIFY DEVICE	90H	Allows the device and manufacturer ID to be read. A0 is used to decode between the manufacturer ID (A0=LOW) and device ID (A0=HIGH).
READ STATUS REGISTER	70H	Allows the status register to be read. Please refer to Table 2 for more information on the status register bits.
CLEAR STATUS REGISTER	50H	Clears status register bits 3 through 5, which cannot be cleared by the ISM.
ERASE SETUP	20H	The first command given in the two cycle erase sequence. The erase will not be completed unless followed by ERASE CONFIRM.
ERASE CONFIRM/RESUME	D0H	The second command given in the two cycle erase sequence. Must follow an ERASE SETUP command to be valid. Also used during an ERASE SUSPEND to resume the erase.
WRITE SETUP	40H or 10H	The first command given in the two cycle write sequence. The write data and address are given in the following cycle to complete the write.
ERASE SUSPEND	B0H	Halts the erase and puts device into the erase suspend mode. When in this mode only READ STATUS REGISTER, READ ARRAY, and ERASE RESUME commands may be executed.

ISM STATUS REGISTER

The 8-bit ISM status register (see Table 2) is polled to check for write or erase completion or any related errors. During or following a write, erase, or erase suspend, a read operation will output the status register contents on DQ0 - DQ7 without prior command. While reading the status register contents, the outputs will not be updated if there is a change in the ISM status unless $\overline{OE}$ or $\overline{CE}$ is toggled. If the device is not in the write, erase, erase suspend, or status register read mode, READ STATUS REGISTER (70H) can be issued to view the status register contents.

All of the defined bits are set by the ISM, but only the ISM and erase suspend status bits are reset by the ISM. The erase, write, and VPP status bits must be cleared using CLEAR STATUS REGISTER. If the VPP status bit (SR3) is set, the CEL will not allow further write or erase operations until the status register is cleared. This allows the user to choose when to poll and clear the status register. For example, the host system may perform multiple byte write operations before checking the status register, instead of checking after each individual write. Asserting the $\overline{RST}$ signal or powering down the device are other methods to clear the status register.

Table 2
STATUS REGISTER

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	ISM STATUS 1 = Ready 0 = Busy	The ISMS bit displays the active status of the state machine when performing write or block erase. The controlling logic polls this bit to determine when the erase and write status bits are valid.
SR6	ERASE SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed	Issuing an ERASE SUSPEND places the ISM in the suspend mode and sets this and the ISMS bit to "1." The ESS bit will remain "1" until an ERASE RESUME is issued.
SR5	ERASE STATUS 1 = Block erase error 0 = Successful block erase	ES is set to "1" after the maximum amount of erase cycles are executed by the ISM without a successful verify. ES is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR4	WRITE STATUS 1 = Write (word/byte) error 0 = Successful word/byte write	WS is set to "1" after the maximum amount of write cycles are executed by the ISM without a successful verify. WS is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR3	VPP STATUS 1 = No VPP voltage detected 0 = VPP present	VPPS detects the presence of a VPP voltage. It does not monitor VPP continously nor does it indicate a valid VPP voltage. The VPP pin is sampled for 12V after WRITE or ERASE CONFIRM is given. Must be cleared by CLEAR STATUS REGISTER or after a RESET.
SR0-2	RESERVED	Reserved for future use.

COMMAND EXECUTION

Commands are issued to bring the device into different operational modes. Each mode has specific operations that can be performed while in that mode. Several modes require a sequence of commands to be written before they are reached. The following section describes the properties of each mode and Table 3 lists all command sequences required to perform the desired operation.

READ ARRAY

The array read mode is the initial state of the device upon powerup, and is also entered after a RESET. If the device is in any other mode, READ ARRAY (FFH) must be given to return to the array read mode. Unlike the WRITE SETUP command (40H), READ ARRAY does not need to be given before each individual read access.

IDENTIFY DEVICE

The 8-bit device identification may be read using one of two methods. IDENTIFY DEVICE (90H) may be written to the CEL to enter the identify device mode. While in this mode, any read will produce the device identification when A0 is HIGH and manufacturer identification when A0 is LOW. The device will remain in this mode until another command is given.

WRITE SEQUENCE

Two consecutive cycles are needed to input data to the array. WRITE SETUP (40H or 10H) is given in the first cycle.The next cycle is the WRITE, during which the write address and data are issued, and V_{PP} brought to V_{PPH}. Writing to the boot block also requires that the $\overline{RST}$ pin be brought to V_{HH} at the same time V_{PP} is brought to V_{PPH}. The ISM will now begin to write the word or byte. The desired bits within the word will be set to logic 0. V_{PP} must be held at V_{PPH} until the write is completed (SR7 = 1). When writing to the boot block, $\overline{RST}$ must be held at V_{HH} until the ISM status bit (SR7) is set.

While the ISM executes the write, the ISM status bit (SR7) will be at 0, and the device will not respond to any commands. However, any read operation will produce the status register contents on DQ0-DQ7. When the ISM status bit (SR7) is set, the write has been completed, and the device will go into the status register read mode until another command is given.

Table 3
COMMAND SEQUENCES

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE			2ND CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY	1	Write	X	FFH				1
IDENTIFY DEVICE	3	Write	X	90H	Read	IA	ID	2, 3
READ STATUS REGISTER	2	Write	X	70H	Read	X	SRD	4
CLEAR STATUS REGISTER	1	Write	X	50H				
ERASE SETUP/CONFIRM	2	Write	X	20H	Write	BA	D0H	5
ERASE SUSPEND/RESUME	2	Write	X	B0H	Write	X	D0H	
WRITE SETUP/WRITE	2	Write	X	40H	Write	WA	WD	6
ALTERNATE WORD /BYTE WRITE	2	Write	X	10H	Write	WA	WD	6

NOTE:
1. Must follow WRITE or ERASE CONFIRM commands to the CEL in order to enable flash array read cycles.
2. IA = Identify address; 00H for manufacturer ID, 01H for device ID.
3. ID = Indentify data.
4. SRD = Status Register Data.
5. BA = Block address.
6. WA = Address to be written, WD = Data to be written to WA.

After the ISM has initiated the write, it cannot be aborted except by a RESET or by powering-down the part. Doing either during a write will corrupt the data being written. If only the WRITE SETUP command has been given, the write may be nullified by performing a null WRITE. To execute a null WRITE, FFH must be written when $\overline{BYTE}$ is LOW, or FFFFH must be written when $\overline{BYTE}$ is HIGH. Once the ISM status bit (SR7) has been set, the device will be in the status register read mode until another command is issued.

ERASE SEQUENCE

Executing an erase sequence will set all bits within a block to logic 1. The command sequence necessary to execute an erase is similar to that of a write. To provide added security against accidental block erasure, two consecutive command cycles are required to initiate an erase of a block. In the first cycle, addresses are "don't care," and ERASE SETUP (20H) is given. In the second cycle, V_{PP} must be brought to V_{PPH}, an address within the block to be erased is issued, and ERASE CONFIRM (D0H) is given. If ERASE CONFIRM is not given, the ISM and erase status bits (SR7 and SR5) will be set, and the device will return to the array read mode.

At this time, the ISM will start the erase of the block. Any read operation will output the status register contents on DQ0-DQ7. V_{PP} must be held at V_{PPH} until the erase is completed (SR7 = 1). Once the erase is completed, the device will be in the status register read mode until another command is issued. Erasing to the boot block also requires that the $\overline{RST}$ pin be set to V_{HH} at the same time V_{PP} is set to V_{PPH}.

ERASE SUSPENSION

The only command that may be issued while an erase is in progress is ERASE SUSPEND. This command allows other commands to be executed while pausing the erase in progress. Once the device has reached the erase suspend mode, the erase suspend status bit (SR6) will be set. The device may now be given a READ ARRAY, ERASE RESUME, or READ STATUS REGISTER. After READ ARRAY has been issued, any location not within the block being erased may be read. If ERASE RESUME is issued before SR6 has been set, the device will immediately proceed with the erase in progress. During the suspend mode V_{PP} must be held at V_{PPH}.

ERROR HANDLING

After the ISM status bit (SR7) has been set, the V_{PP} (SR3), write (SR4), and erase (SR5) status bits may be checked. If one or a combination of these three bits has been set, then an error has occurred. The ISM cannot reset these three bits. To clear these bits, CLEAR STATUS REGISTER (50H) must be given. If the V_{PP} status bit (SR3) is set, further write or erase operations cannot resume until the status register is cleared. Table 4 lists the combination of errors.

Table 4
STATUS REGISTER ERROR DECODE[1]

STATUS BITS			
SR5	SR4	SR3	ERROR DESCRIPTION
0	0	0	No errors
0	0	1	V_{PP} voltage error
0	1	0	Write error
0	1	1	Write error, V_{PP} voltage not valid at time of WRITE
1	0	0	Erase error
1	0	1	Erase error, V_{PP} voltage not valid at time of ERASE CONFIRM
1	1	0	Command sequencing error
1	1	1	Command sequencing error, programming voltage error

NOTE: 1. SR3 - SR5 must be cleared using CLEAR STATUS REGISTER.

WRITE/ERASE CYCLE ENDURANCE

The MT28F200 is designed and fabricated to meet advanced firmware storage requirements. To ensure this level of reliability, V_{PP} must be at 12V ±5% during write or erase cycles. Operation outside these limits may reduce the number of erase cycles that can be performed on the device. For further information on write and erase cycle endurance, refer to the Micron *Flash Reliability Monitor*.

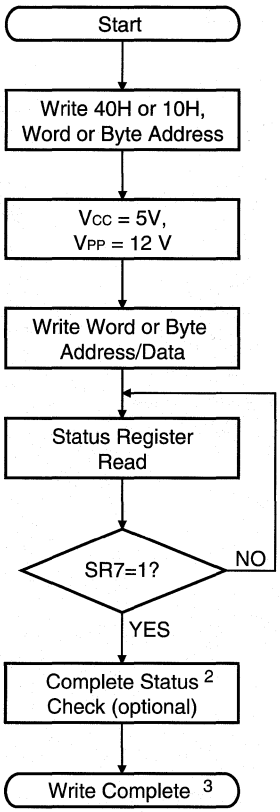
POWER USAGE

The MT28F200 offers several power saving features that may be utilized in the array read mode to conserve power. With $\overline{CE}$ LOW, the device will enter idle current mode when not being accessed. In this mode, the maximum I_{CC} current is 3mA. When $\overline{CE}$ is HIGH, the device will enter standby mode. In this mode, maximum I_{CC} current is 100µA. If $\overline{CE}$ is brought HIGH during an erase or write, the ISM will continue to operate, and the device will consume the respective active power until the write or erase is completed.

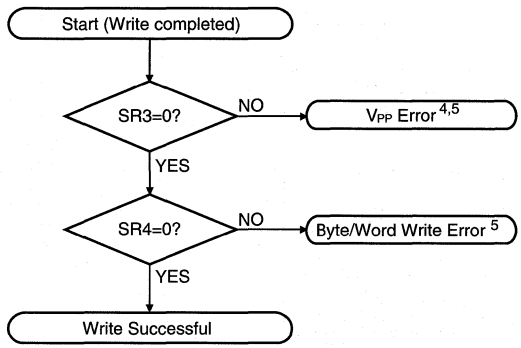
POWERUP

During a powerup, it is not necessary to sequence V_{CC} and V_{PP}. The likelihood of unwanted write or erase operations is minimized, since two consecutive cycles are required to execute either operation. However, $\overline{CE}$ or $\overline{WE}$ may be held HIGH, or $\overline{RST}$ can be held LOW during powerup for additional protection against unwanted write or erase operations. After a powerup or RESET, the status register is reset, and the device will enter the array read mode.

SELF-TIMED WRITE SEQUENCE (Word or Byte Write)[1]

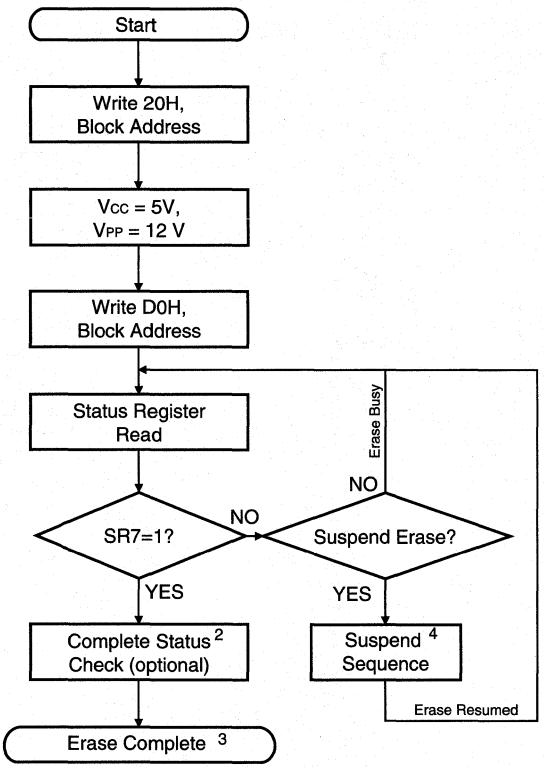


COMPLETE WRITE STATUS-CHECK SEQUENCE

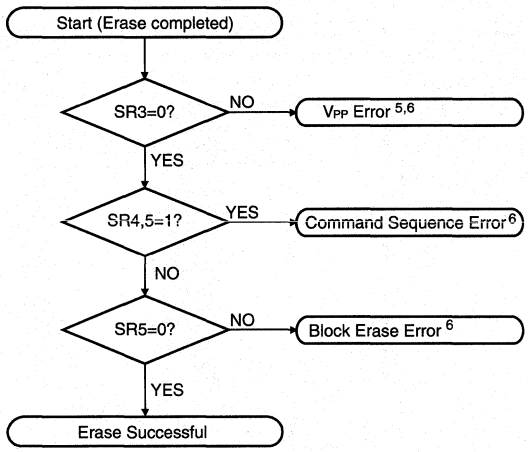


NOTE:
1. Sequence may be repeated for multiple byte or word writes.
2. Complete status check is not required. However, if SR3 = 1, further writes are inhibited until the status register is cleared.
3. Device will be in status register read mode. To return to the array read mode, the FFH command must be issued.
4. If SR3 is set during a write or erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
5. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

SELF-TIMED BLOCK ERASE SEQUENCE[1]

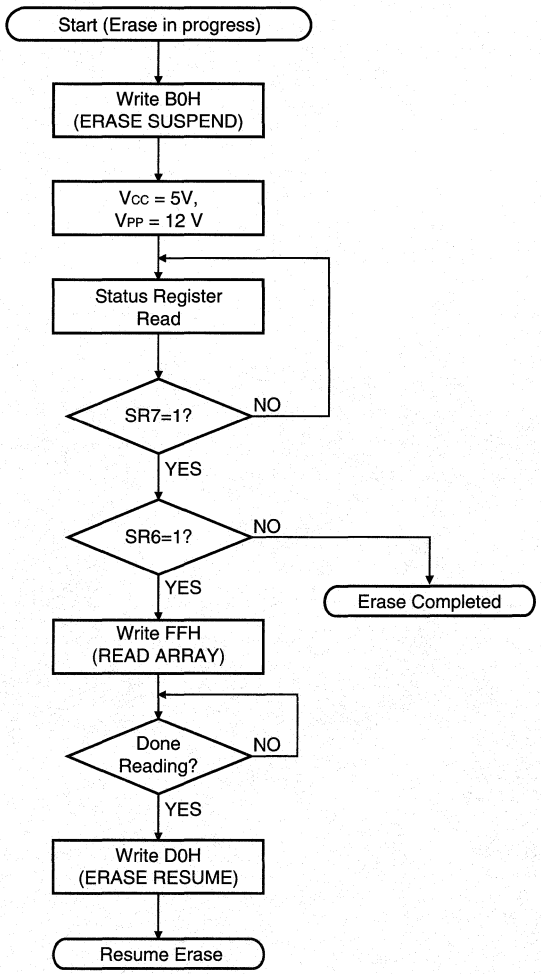


COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



NOTE:
1. Sequence may be repeated to erase multiple blocks.
2. Complete status check is not required. However, if SR3 = 1, further erases are inhibited until the status register is cleared.
3. To return to the array read mode, the FFH command must be issued.
4. Refer to the erase suspend flowchart for more information.
5. If SR3 is set during a write or erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
6. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

ERASE SUSPEND/RESUME SEQUENCE



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -0.5V to +7V
Input Voltage Relative to Vss ..... -0.5V to +7V**
VPP Voltage Relative to Vss ..... -0.5V to +12.6V†
$\overline{RST}$/Pin A9 Voltage Relative to Vss .... -0.5V to +13.5V**,†
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Input and I/O pins may transition to -2.0V for < 20ns and Vcc +2.0V for < 20ns.
†Voltage may pulse to 14.0V ≤ 20ns.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-0.5	0.8	V	1
Device Identification Voltage, A9	VID	11.4	13.0	V	1

DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS Output High Voltage (IOH = - 2.5 mA)	VOH	2.4		V	1
Output Low Voltage (IOL = 5.8 mA)	VOL		0.45	V	
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.4V ≤ A9 ≤ 13.0 = VID)	IID		500	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled; 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	

CAPACITANCE

(T_A = 25°C; Vcc = 5V ±10%; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	CI	8	pF	
Output Capacitance	CO	12	pF	

NOTE: 1. All voltages referenced to Vss.

READ AND STANDBY CURRENT DRAIN

($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
READ CURRENT: WORD-WIDE, TTL INPUT LEVELS ($\overline{CE} = V_{IL}$; f = 10 MHz; Other inputs = V_{IL} or V_{IH}); $\overline{RST} = V_{IH}$	I_{CC1}	60	mA	2, 3
READ CURRENT: WORD-WIDE, CMOS INPUT LEVELS ($\overline{CE} \le 0.2V$; f = 10 MHz; Other inputs$\le$ 0.2V, or $\ge V_{CC}$-0.2V); $\overline{RST} = V_{IH}$	I_{CC2}	55	mA	2, 3
READ CURRENT: BYTE-WIDE, TTL INPUT LEVELS ($\overline{CE} = V_{IL}$; f = 10 MHz; Other inputs = V_{IL} or V_{IH}); $\overline{RST} = V_{IH}$	I_{CC3}	60	mA	2, 3
READ CURRENT: BYTE-WIDE, CMOS INPUT LEVELS ($\overline{CE} \le 0.2V$; f = 10 MHz; Other inputs $\le$ 0.2V, or $\ge V_{CC}$-0.2V); $\overline{RST} = V_{IH}$	I_{CC4}	55	mA	2, 3
READ CURRENT: V_{PP} SUPPLY ($V_{PP} > V_{CC}$)	I_{PP1}	200	µA	
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current ($\overline{CE} = \overline{RST} = V_{IH}$, or $\overline{RST} = V_{IL}$; other inputs = V_{IL} or V_{IH})	I_{CC5}	1.5	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current ($\overline{CE} = \overline{RST} = V_{CC}$ - 0.2V; Other inputs $\le$ 0.2V, or $\ge V_{CC}$-0.2V)	I_{CC6}	100	µA	
STANDBY CURRENT: V_{PP} SUPPLY ($V_{PP} \le V_{CC}$)	I_{PP2}	±15	µA	
IDLE CURRENT: TTL INPUT LEVELS ($\overline{CE} = V_{IL}$; f = 0 Hz; Other inputs = V_{IL} or V_{IH}; $\overline{RST} = V_{IH}$; array read mode)	I_{CC7}	3	mA	
IDLE CURRENT: CMOS INPUT LEVELS ($\overline{CE} \le 0.2V$; f = 0 Hz; Other inputs $\le$ 0.2V, or $\ge V_{CC}$-0.2V; $\overline{RST} = V_{IH}$; READ ARRAY)	I_{CC8}	3	mA	

WRITE/ERASE CURRENT DRAIN

($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
WORD-WRITE CURRENT: V_{CC} SUPPLY ($V_{PP} = 12V \pm 5\%$)	I_{CC9}	65	mA	
WORD-WRITE CURRENT: V_{PP} SUPPLY ($V_{PP} = 12V \pm 5\%$)	I_{PP3}	40	mA	
BYTE-WRITE CURRENT: V_{CC} SUPPLY ($V_{PP} = 12V \pm 5\%$)	I_{CC10}	65	mA	
BYTE-WRITE CURRENT: V_{PP} SUPPLY ($V_{PP} = 12V \pm 5\%$)	I_{PP4}	30	mA	
ERASE CURRENT: V_{CC} SUPPLY ($V_{PP} = 12V \pm 5\%$)	I_{CC11}	30	mA	
ERASE CURRENT: V_{PP} SUPPLY ($V_{PP} = 12V \pm 5\%$)	I_{PP5}	30	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY ($V_{PP} = 12V \pm 5\%$; erase suspended)	I_{CC12}	10	mA	4
ERASE SUSPEND CURRENT: V_{PP} SUPPLY ($V_{PP} = 12V \pm 5\%$; erase suspended)	I_{PP6}	200	µA	

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	70		80		100		ns	6
Access time from $\overline{CE}$	^tACE		70		80		100	ns	5,6
Access time from $\overline{OE}$	^tAOE		35		40		50	ns	5,6
Access time from address	^tAA		70		80		100	ns	6
$\overline{RST}$ HIGH to output valid delay	^tRWH		300		300		300	ns	6
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		25		30		40	ns	6
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		0		0		ns	6

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	60		ns	7
Access time from $\overline{CE}$	^tACE		60	ns	5,7
Access time from $\overline{OE}$	^tAOE		30	ns	5,7
Access time from address	^tAA		60	ns	7
$\overline{RST}$ HIGH to output valid delay	^tRWH		300	ns	7
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		20	ns	7
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		ns	7

AC TEST CONDITION–1

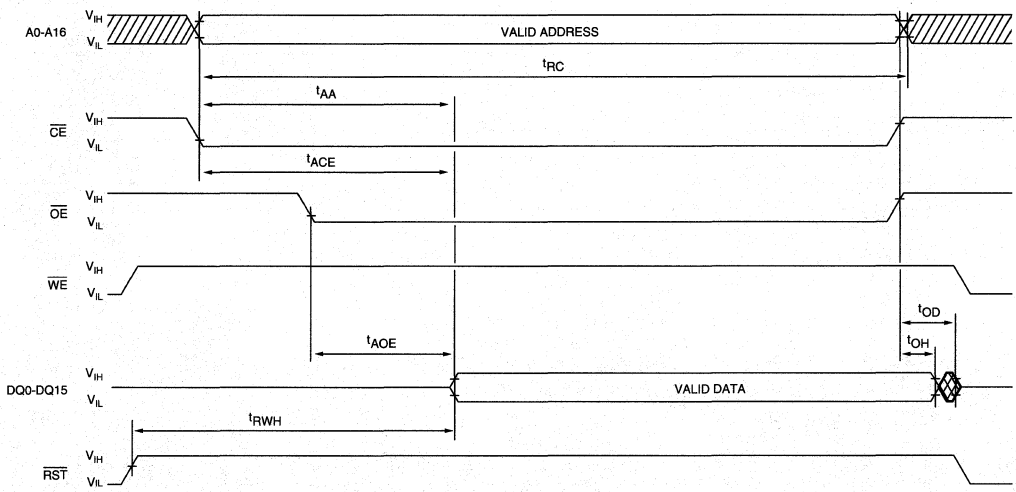
Input pulse levels	0.4 to 2.4V
Input rise and fall times	<10ns
Input timing reference level	0.8 V and 2.0 V
Output timing reference level	0.8 V and 2.0 V
Output load	1 TTL gate and C_L = 100 pF

AC TEST CONDITION–2

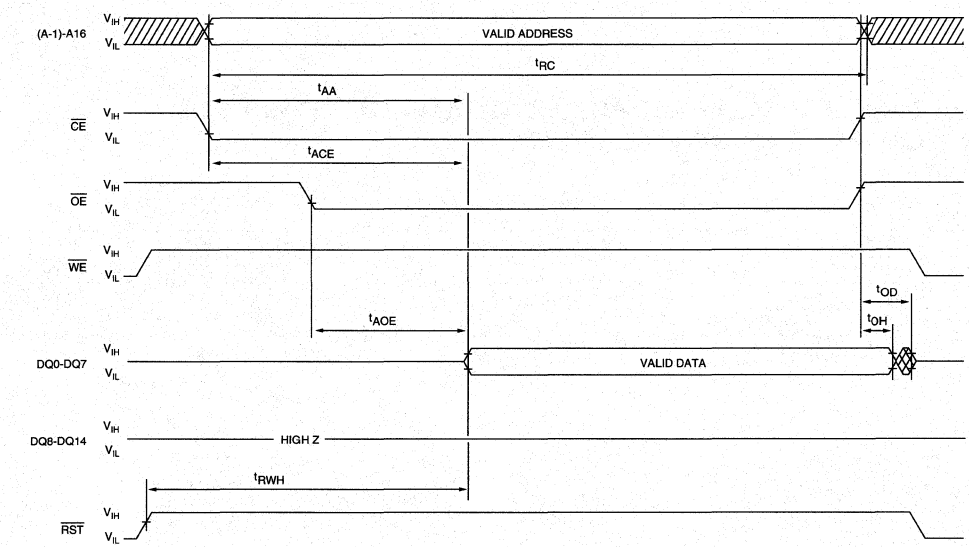
Input pulse levels	0.0 to 3.0V
Input rise and fall times	<10ns
Input timing reference level	1.5 V
Output timing reference level	1.5 V
Output load	1 TTL gate and C_L = 30 pF

NOTE:
1. All voltages referenced to Vss.
2. Icc is dependent on cycle rates.
3. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Parameter is specified when device is not accessed. Actual current draw will be Icc12 plus read current if a read is executed while in erase suspend mode.
5. $\overline{OE}$ may be delayed by ^tACE minus ^tAOE after $\overline{CE}$ falls before ^tACE is affected.
6. Measurements tested under AC Test Conditions-1.
7. Measurements tested under AC Test Conditions-2.

WORD-WIDE READ CYCLE [1]



BYTE-WIDE READ CYCLE [2]



DON'T CARE

UNDEFINED

NOTE: 1. $\overline{BYTE}$ = HIGH
2. $\overline{BYTE}$ = LOW

RECOMMENDED DC WRITE/ERASE CONDITIONS

($0°C \leq T_A \leq +70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
V_{PP} voltage during normal operation	V_{PPL}	0.0	6.5	V	
V_{PP} voltage during erase/write operation	V_{PPH}	11.4	12.6	V	
Boot block unlock voltage	V_{HH}	11.5	13.0	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT: $\overline{RST}$ INPUT ($11.4 \leq \overline{RST} \leq 13.0V = V_{HH}$)	I_{HH}		500	µA	

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	70		80		100		ns	1
$\overline{WE}$ HIGH pulse width	^tWPH	20		20		30		ns	1
$\overline{CE}$ HIGH pulse width	^tCPH	20		20		30		ns	1

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	60		ns	2
$\overline{WE}$ HIGH pulse width	^tWPH	10		ns	2
$\overline{CE}$ HIGH pulse width	^tCPH	10		ns	2

NOTE: 1. Measurements tested under AC Test Conditions-1.
2. Measurements tested under AC Test Conditions-2.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{WE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10% or ±5%)

AC CHARACTERISTICS		-6, -8, -10			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{WE}$ HIGH	^tAS	50		ns	
Address hold time from $\overline{WE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{WE}$ HIGH	^tDS	50		ns	
Data hold time from $\overline{WE}$ HIGH	^tDH	0		ns	
$\overline{CE}$ setup time to $\overline{WE}$ LOW	^tCS	0		ns	
$\overline{CE}$ hold time from $\overline{WE}$ HIGH	^tCH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	100		ns	1
$\overline{WE}$ pulse width	^tWP	50		ns	
$\overline{RST}$ HIGH to $\overline{WE}$ LOW delay	^tRS	220		ns	
$\overline{RST}$ V_{HH} setup time to $\overline{WE}$ HIGH	^tRHS	100		ns	2
Write duration (word or byte write)	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		100	ns	3

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{CE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10% or ±5%)

AC CHARACTERISTICS		-6, -8, -10			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{CE}$ HIGH	^tAS	50		ns	
Address hold time from $\overline{CE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{CE}$ HIGH	^tDS	50		ns	
Data hold time from $\overline{CE}$ HIGH	^tDH	0		ns	
$\overline{WE}$ setup time to $\overline{CE}$ LOW	^tWS	0		ns	
$\overline{WE}$ hold time from $\overline{CE}$ HIGH	^tWH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	100		ns	1
$\overline{CE}$ pulse width	^tCP	50		ns	
$\overline{RST}$ HIGH to $\overline{CE}$ LOW delay	^tRS	220		ns	
$\overline{RST}$ V_{HH} setup time to $\overline{CE}$ HIGH	^tRHS	100		ns	2
WRITE duration (word or byte write)	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1, 2
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		100	ns	2

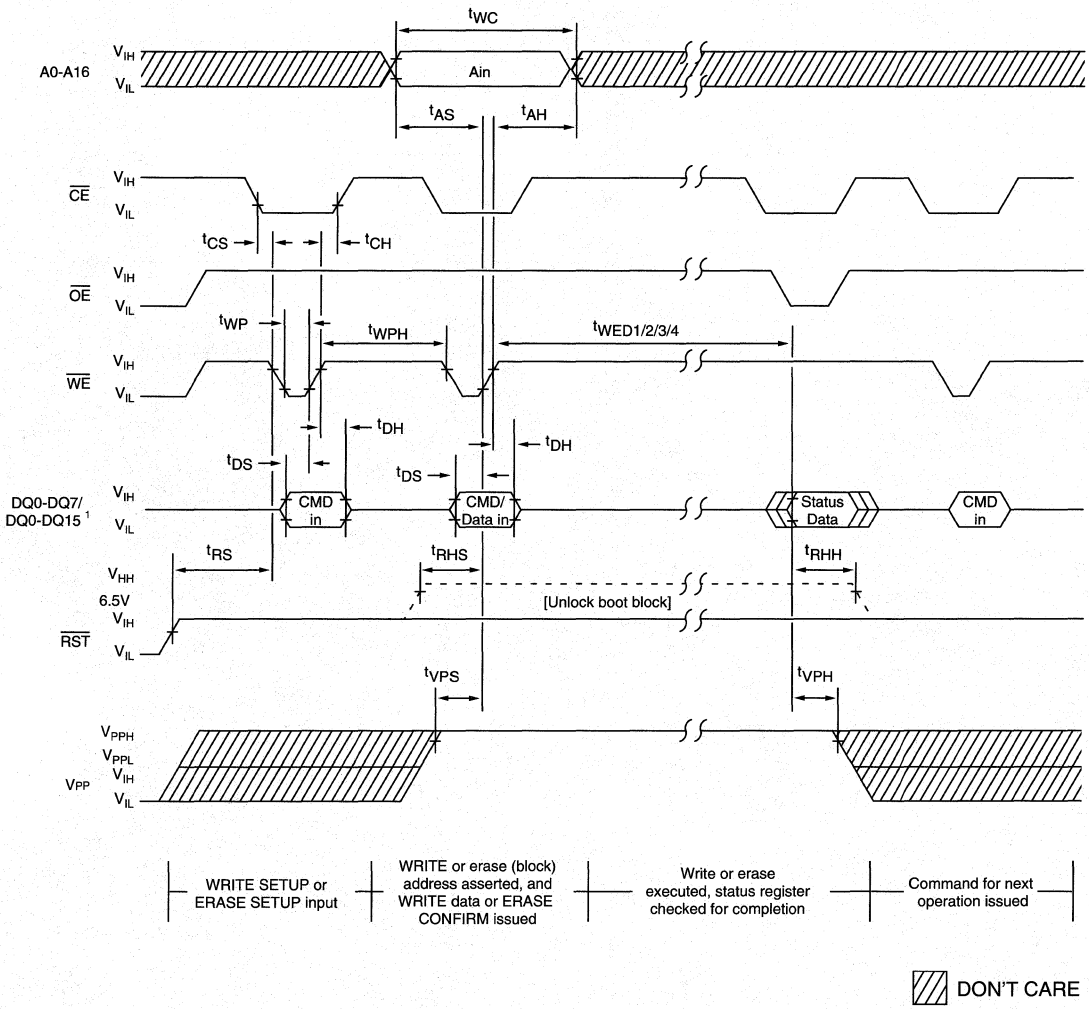
NOTE: 1. Write/erase times are measured to valid status register data (SR7=1).
2. $\overline{RST}$ should be held at V_{HH} until boot-block write or erase is complete.
3. ^tREL is required to relock boot block after write or erase to boot block.

WORD/BYTE WRITE AND ERASE DURATION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Boot/parameter block erase time		1.0	7.0	s	1
Main block erase time		2.5	14.0	s	1
Main block byte write time		1.0	4.0	s	1, 2
Main block word write time		0.5	2.0	s	1, 2

NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.

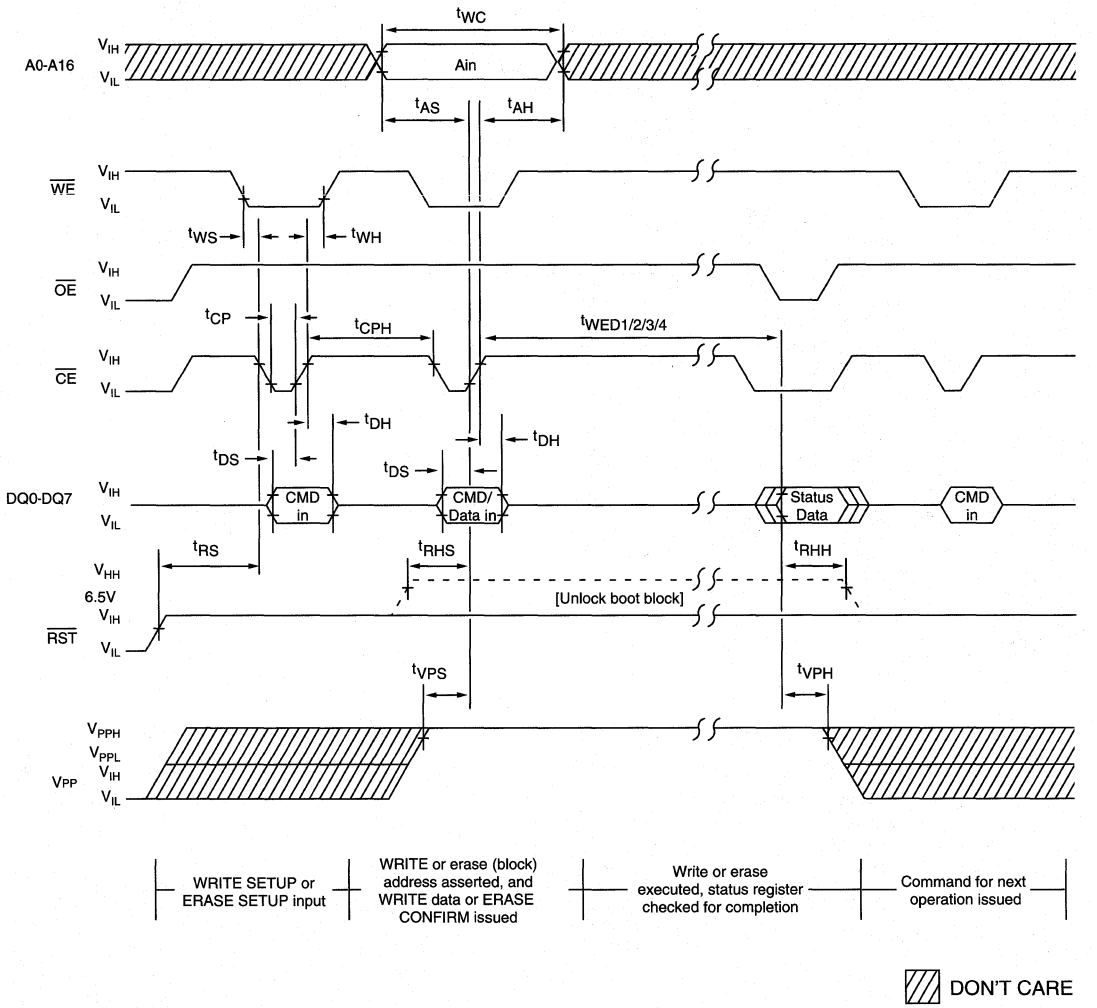
ERASE/WRITE CYCLE
$\overline{WE}$-CONTROLLED WRITE/ERASE



NOTE: 1. If $\overline{BYTE}$ is LOW, DATA and COMMAND are 8-bit. If $\overline{BYTE}$ is HIGH, DATA is 16-bit and COMMAND is 8-bit.

NEW ■ 5/12 VOLT FLASH MEMORY

ERASE/WRITE CYCLE
$\overline{CE}$-CONTROLLED WRITE/ERASE



NOTE: 1. If $\overline{BYTE}$ is LOW, DATA and COMMAND are 8-bit. If $\overline{BYTE}$ is HIGH, DATA is 16-bit and COMMAND is 8-bit.

NEW ■ 5/12 VOLT FLASH MEMORY

FLASH MEMORY 512K x 8

5V/12V, BOOT BLOCK

FEATURES

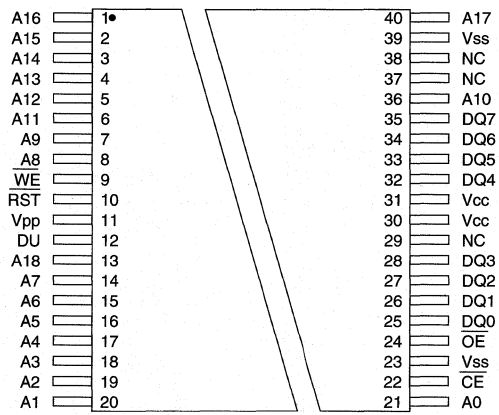
- Seven erase blocks:
  - 16KB boot block (protected)
  - Two 8KB parameter blocks
  - Four general memory blocks
- Low power: 100µA standby; 60mA active, MAX
- 5V±10% read; 12V±5% write/erase
- Address access times: 60ns, 80ns, 100ns
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm

OPTIONS MARKING

- Timing
  - 60ns access - 6
  - 80ns access - 8
  - 100ns access -10
- Boot-Block Starting Address
  - Top (7FFFFH) T
  - Bottom (00000H) B
- Packages
  - Plastic TSOP Type 1 (10 x 20mm) VG
- Part Number Example: MT28F004VG-8T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(FB-1)



GENERAL DESCRIPTION

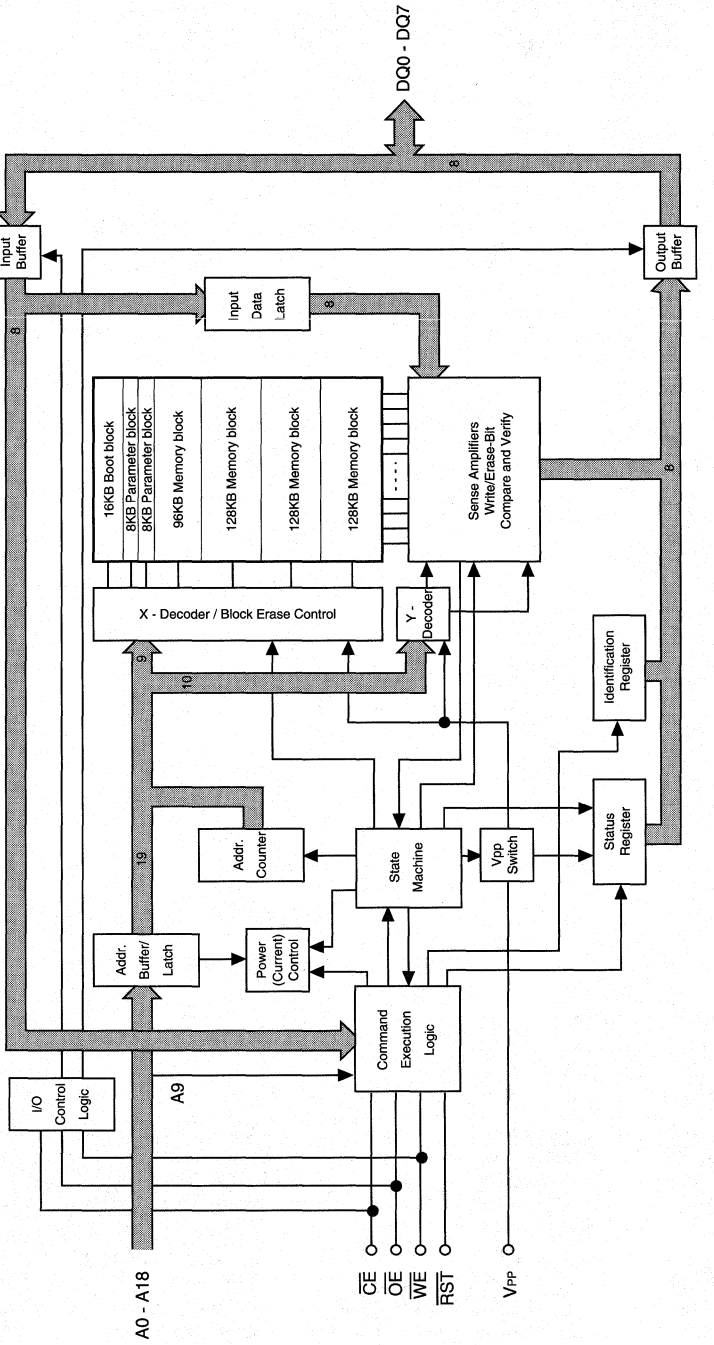
The MT28F004 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 4,194,304 bits organized as 524,288 words by 8 bits. It is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F004 is organized into seven separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F004 features a hardware-protected boot-block. Writing or erasing the boot block requires a super-voltage on the $\overline{RST}$ pin in addition to executing the normal write or block erase sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density, and are written-to and erased with no additional super-voltage required.

The byte address is issued to read the memory array with $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH. Valid data is output until the next address is issued or $\overline{CE}$ or $\overline{OE}$ go HIGH.

NEW ■ 5/12 VOLT FLASH MEMORY

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
9	$\overline{WE}$	Input	Write Enable: Determines if a given cycle is a write cycle. If $\overline{WE}$ = LOW when $V_{PP} < V_{PPH}$, the cycle is a WRITE (command input) to the Command Execution Logic (CEL). If $\overline{WE}$ = LOW when $V_{PP} = V_{PPH}$, the cycle is a WRITE to one of the sectors or an ERASE CONFIRM.
22	$\overline{CE}$	Input	Chip Enable: Activates the device when LOW. When $\overline{CE}$ is HIGH, the device is disabled and goes into standby power mode.
10	$\overline{RST}$	Input	Reset: Clears the status register, sets the Internal State Machine (ISM) to the array read mode, and places the device in standby mode when LOW. All inputs, including $\overline{CE}$, are "don't care", and all outputs are High-Z. Also used to unlock boot block when brought to V_{HH} (boot-block unlock voltage; 12V). Must be held HIGH during all other modes of operation.
24	$\overline{OE}$	Input	Output Enable: Enables data output buffers.
21,20,19,18, 17, 16, 15, 14, 8, 7, 36, 6, 5, 4, 3, 2, 1, 40, 13	A0-A18	Input	Address Inputs: Selects a unique byte out of the 524,288 available.
25, 26, 27, 28, 32, 33, 34, 35	DQ0-DQ7	Input/ Output	Data I/O: Data output pins during any read operation, or data input pins during a WRITE. Used to input commands to the CEL for a command input.
29, 37, 38	NC	-	No Connect: These pins may be driven or left unconnected.
11	V_{PP}	Supply	Write/Erase Supply Voltage: During a WRITE or ERASE CONFIRM, $V_{PP} = V_{PPH}$ (12V). V_{PP} = "don't care" during all other operations.
30, 31	Vcc	Supply	Power Supply: +5V ±10%
23, 39	Vss	Supply	Ground

TRUTH TABLE [1]

FUNCTION	$\overline{RST}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A9	V_{PP}	DQ0-DQ7
Standby	H	H	X	X	X	X	X	High-Z
RESET	L	X	X	X	X	X	X	High-Z
READING								
Read	H	L	L	H	X	X	X	Data-Out
Output Disable	H	L	H	H	X	X	X	High-Z
WRITE/ERASE [2]								
ERASE SETUP	H	L	H	L	X	X	X	20H
ERASE CONFIRM [3]	H	L	H	L	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	10H/40H
WRITE [4]	H	L	H	L	X	X	V_{PPH}	Data-In
READ ARRAY	H	L	H	L	X	X	X	FFH
WRITE/ERASE (BOOT BLOCK) [2, 5]								
ERASE SETUP	H	L	H	L	X	X	X	20H
ERASE CONFIRM [3]	V_{HH}	L	H	L	X	X	V_{PPH}	D0H
WRITE SETUP	H	L	H	L	X	X	X	10H/40H
WRITE [4]	V_{HH}	L	H	L	X	X	V_{PPH}	Data-In
READ ARRAY	H	L	H	L	X	X	X	FFH
DEVICE IDENTIFICATION [6, 7]								
Manufacturer (8-bit)	H	L	L	H	L	V_{ID}	X	2CH
Device (top boot)	H	L	L	H	H	V_{ID}	X	B2H
Device (bottom boot)	H	L	L	H	H	V_{ID}	X	B3H

NOTE: 1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. V_{PPH} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. V_{HH} = 12V.
6. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
7. A1-A8, A10-A18 = V_{IL}.

FUNCTIONAL DESCRIPTION

The MT28F004 Flash memory incorporates a number of features to make it ideally suited for system firmware.

The memory array is segmented into individual erase blocks. Each block may be erased without affecting data stored in other blocks. These memory blocks are read, written and erased by issuing commands to the Command Execution Logic (CEL). The CEL controls the operation of the Internal State Machine (ISM) that completely controls all write, block erase, and verify operations. This state machine protects each memory location from overerasure and optimizes each memory location for maximum data retention. In addition, the ISM greatly simplifies the control necessary for writing the device in-system or in an external programmer.

The Functional Description provides detailed information on the operation of the MT28F004, and is organized into these sections:

- Overview
- Memory Architecture
- Output (Read) Operations
- Input Operations
- Command Set
- ISM Status Register
- Command Execution
- Error Handling
- Write/Erase Cycle Endurance
- Power Usage
- Powerup

OVERVIEW

SEVEN INDEPENDENTLY ERASABLE MEMORY BLOCKS

The MT28F004 is organized into seven independently erasable memory blocks that allow portions of the memory to be erased without affecting the rest of the memory data. A special boot block is hardware-protected against inadvertent erasure or writes by a super-voltage pin. The voltage on this pin is required in addition to the 12V on the V_{PP} pin. The remaining blocks require only the 12V V_{PP} to be present in order to be changed.

HARDWARE-PROTECTED BOOT-BLOCK

This block of the memory array can be erased or written only when the $\overline{RST}$ pin is taken to V_{HH}. Designing a system so that the processor or control logic is unable to apply 12V to this pin will ensure data integrity in this memory block. This provides additional security for the core firmware during in-system firmware updates, should an unintentional power fluctuation or system reset occur. The MT28F004 is available in two versions; the MT28F004T addresses the boot block starting from 7FFFFH, and the MT28F004B addresses the boot block starting from 00000H.

INTERNAL STATE MACHINE (ISM)

Block erase and write timing are simplified by using an ISM to control all erase and write algorithms in the memory array. The ISM ensures protection against overerasure and optimizes write margin to each cell.

During write operations the ISM automatically increments and monitors write attempts, verifies write margin on each memory cell, and updates the ISM status register. When a block erase is performed the ISM automatically overwrites the entire addressed block (eliminates overerasure), increments and monitors erase attempts, and sets bits in the ISM status register.

ISM STATUS REGISTER

The ISM status register allows an external processor to monitor the status of the ISM during write and erase operations. Two bits of the 8-bit status register are set and cleared entirely by the ISM. These bits indicate whether the ISM is busy with an erase or write task, and when an erase has been suspended. Additional error information is set in the other three bits: valid programming voltage, write error, and erase error.

COMMAND EXECUTION LOGIC (CEL)

The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the read path (i.e. memory array, ID register, or status register). Commands may be issued to the CEL while the ISM is active. However, there are restrictions on what commands are allowed in this condition. See the Command Execution section for more detail.

MEMORY ARCHITECTURE

The MT28F004 memory array architecture is designed to allow sections to be erased without disturbing the rest of the array. The array is divided into seven addressable "blocks" that are of varying size and independently erasable. By erasing in blocks, rather than the entire array, the total device endurance is enhanced, as is system flexibility. Only the erase function is block oriented. All read and write operations are done on a random byte basis.

The boot block is protected from unintentional erase or write with a hardware protection circuit that requires a super-voltage be applied before erasure is commenced. The boot block is intended for the core firmware required for basic system functionality. The remaining six blocks do not require this super-voltage before being written or erased.

BOOT BLOCK

The hardware-protected boot-block provides extra security for the most sensitive portions of the firmware. This 16KB block may only be erased or written when the $\overline{RST}$ pin is at the specified boot block unlock voltage (V_{HH}) of 12V. When performing erase or write cycles to this block, $\overline{RST}$ must be held at the unlock voltage (V_{HH}) until the erase or write is completed. As for any erase or write operations, the V_{PP} pin must be at V_{PPH} when writing to the boot block.

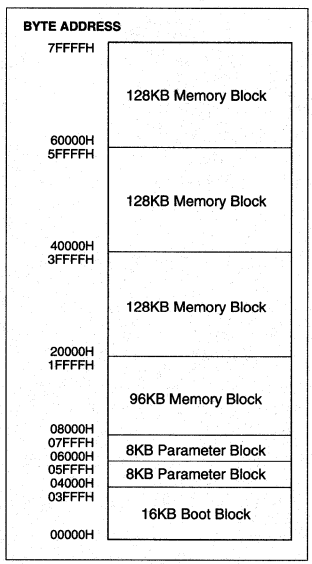
The MT28F004 is available in two configurations, top or bottom boot-block. The MT28F004T top boot-block version supports processors of the x86 variety. The MT28F004B bottom boot-block version is intended for 680X0 and RISC applications. Figure 1 illustrates the memory address maps associated with these two versions.

PARAMETER BLOCKS

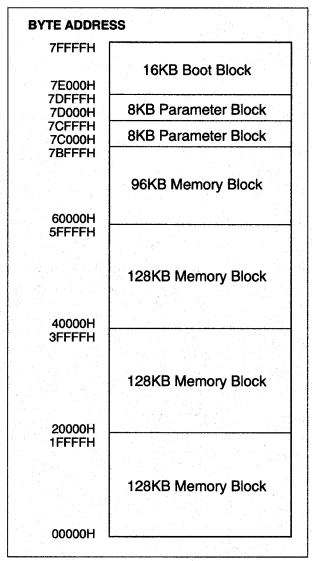
The two 8KB parameter blocks are used for storage of less sensitive and more frequently changing system parameters and also may include configuration or diagnostic coding. These blocks are enabled for erasure when the V_{PP} pin is at V_{PPH}. No super-voltage unlock is required.

GENERAL MEMORY BLOCKS

The four remaining blocks are general memory blocks and do not require a super-voltage on $\overline{RST}$ to be erased or written. These blocks are intended for code storage, or ROM-resident applications or operating systems that require in-system update capability.



Bottom Boot - MT28F004VG-xxB



Top Boot - MT28F004VG-xxT

Figure 1
MEMORY ADDRESS MAPS

OUTPUT (READ) OPERATIONS

The MT28F004 features three different types of reads. Depending on the current mode of the device, a read operation will produce data from the memory array, status register, or device identification register. In each of these three cases, the $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$ inputs are controlled in a similar manner to perform a read. However, several differences exist, and are described in the following section. Moving between modes to perform a specific read will be covered in the Command Execution section.

MEMORY ARRAY

To read the memory array, $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. Valid data will be output on the DQ pins once these conditions have been met and a valid address is given. Valid data will remain on the DQ pins until the address changes, or $\overline{OE}$ or $\overline{CE}$ go HIGH, whichever occurs first. The DQ pins will continue to output new data after each address transition, as long as $\overline{OE}$ and $\overline{CE}$ remain LOW.

After powerup or RESET, the device will automatically be in the array read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

STATUS REGISTER

Performing a read of the status register requires the same input sequencing as when reading the array, except that the address inputs are "don't care." Data from the status register is latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last. If the contents of the status register change during a read of the status register, either $\overline{OE}$ or $\overline{CE}$ may be toggled while the other is held LOW to update the output.

Following a write or erase, the device automatically enters the status register read mode. In addition, a read during a write or erase will produce the status register contents on DQ0-DQ7. When in the erase suspend mode, a read operation will produce the status register contents until another command is issued. While in certain other modes, READ STATUS REGISTER may be given to return to the status register read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

IDENTIFICATION REGISTER

A read of the two 8-bit device identification registers requires the same input sequencing as when reading the array. $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. A0 is used to decode between the two bytes of the device ID register; all other address inputs are "don't care." When A0 is LOW, the manufacturer ID is output, and when A0 is HIGH, the device ID is output.

To get to the identification register read mode, READ IDENTIFICATION may be issued while in certain other modes. In addition, the identification register read mode can be reached by applying a super-voltage (V_{ID}) to the A9 pin. Using this method, the ID register can be read while in any mode. Once A9 is returned to V_{IL} or V_{IH}, the device will return to the previous mode.

INPUT OPERATIONS

The DQ pins are used to either input data to the array or input a command to the CEL. A command input issues an 8-bit command to the CEL. Commands may be issued to control operation of the part. A WRITE is used to input data to the memory array. The following section describes both types of inputs. More information describing how to use the two types of inputs to write the device is provided in the Command Execution section.

COMMANDS

To perform a command input, $\overline{OE}$ must be HIGH, and $\overline{CE}$ and $\overline{WE}$ must be LOW. A0-A18 are not used for command inputs, except during an ERASE CONFIRM (described in a later section). The 8-bit command is input on DQ0-DQ7. The command is latched on the rising edge of $\overline{CE}$ ($\overline{CE}$ controlled) or $\overline{WE}$ ($\overline{WE}$ controlled), whichever occurs first.

MEMORY ARRAY

A write to the memory array sets the desired bits to logic 0's, but cannot change a given bit to a logic 1 from a logic 0. Setting any bits to a logic 1 requires that the entire block be erased. To perform a WRITE, $\overline{OE}$ must be HIGH, $\overline{CE}$ and $\overline{WE}$ must be LOW, and V_{PP} must be set to V_{PPH}. Writing to the boot block also requires that the $\overline{RST}$ pin be at V_{HH}. A0-A18 provide the address to be written, while the data to be written to the array is input on the DQ pins. The data and addresses are latched on the rising edge of $\overline{CE}$ ($\overline{CE}$-controlled) or $\overline{WE}$ ($\overline{WE}$-controlled), whichever occurs first. A WRITE must be preceeded by a WRITE SETUP. Detail on how to input data to the array will be covered in the Write Sequence section.

COMMAND SET

To simplify writing of the memory blocks, the MT28F004 incorporates an ISM that controls all internal algorithms for the write and erase cycles. An 8-bit command set is used to control the device. Detail on how to sequence commands is provided in the Command Execution section. Table 1 lists the valid commands.

Table 1
COMMAND SET

COMMAND	HEX CODE	DESCRIPTION
RESERVED	00H	This command and all unlisted commands are invalid, and should not be called. These commands are reserved to allow for future feature enhancements.
READ ARRAY	FFH	Must be issued after any other command cycle before the array can be read. It is not necessary to issue this command after powerup or reset.
IDENTIFY DEVICE	90H	Allows the device and manufacturer ID to be read. A0 is used to decode between the manufacturer ID (A0=LOW) and device ID (A0=HIGH).
READ STATUS REGISTER	70H	Allows the status register to be read. Please refer to Table 2 for more information on the status register bits.
CLEAR STATUS REGISTER	50H	Clears status register bits 3 through 5, which cannot be cleared by the ISM.
ERASE SETUP	20H	The first command given in the two cycle erase sequence. The erase will not be completed unless followed by the ERASE CONFIRM command.
ERASE CONFIRM/RESUME	D0H	The second command given in the two cycle erase sequence. Must follow an ERASE SETUP command to be valid. Also used during an ERASE SUSPEND to resume the erase.
WRITE SETUP	40H or 10H	The first command given in the two cycle write sequence. The write data and address are given in the following cycle to complete the write.
ERASE SUSPEND	B0H	Halts the erase and puts device into the erase suspend mode. When in this mode only READ STATUS REGISTER, READ ARRAY, and ERASE RESUME commands may be executed.

ISM STATUS REGISTER

The 8-bit ISM status register (see Table 2) is polled to check for write or erase completion or any related errors. During or following a write, erase, or erase suspend, a read operation will output the status register contents on DQ0 - DQ7 without prior command. While reading the status register contents, the outputs will not be updated if there is a change in the ISM status unless $\overline{OE}$ or $\overline{CE}$ is toggled. If the device is not in the write, erase, erase suspend, or status register read mode, READ STATUS REGISTER (70H) can be issued to view the status register contents.

All of the defined bits are set by the ISM, but only the ISM and erase suspend status bits are reset by the ISM. The erase, write, and VPP status bits must be cleared using CLEAR STATUS REGISTER. If the VPP status bit (SR3) is set, the CEL will not allow further write or erase operations until the status register is cleared. This allows the user to choose when to poll and clear the status register. For example, the host system may perform multiple byte write operations before checking the status register, instead of checking after each individual write. Asserting the $\overline{RST}$ signal or powering down the device are other methods to clear the status register.

Table 2
STATUS REGISTER

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	ISM STATUS 1 = Ready	The ISMS bit displays the active status of the state machine when performing write or erase. The controlling logic polls this bit to determine when the erase and write status bits are valid.
SR6	ERASE SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed	Issuing an ERASE SUSPEND places the ISM in the suspend mode and sets this and the ISMS bit to "1." The ESS bit will remain "1" until an ERASE RESUME is issued.
SR5	ERASE STATUS 1 = Block erase error 0 = Successful block erase	ES is set to "1" after the maximum amount of erase cycles are executed by the ISM without a successful verify. ES is only cleared by CLEAR STATUS REGISTER or after a RESET.
SR4	WRITE STATUS 1 = Write error 0 = Successful write	WS is set to "1" after the maximum amount of write cycles are executed by the ISM without a successful verify. WS is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR3	VPP STATUS 1 = No VPP voltage detected 0 = VPP present	VPPS detects the presence of a VPP voltage. It does not monitor VPP continously nor does it indicate a valid VPP voltage. The VPP pin is sampled for 12V after WRITE or ERASE CONFIRM is given. Must be cleared by CLEAR STATUS REGISTER or after a RESET.
SR0-2	RESERVED	Reserved for future use

COMMAND EXECUTION

Commands are issued to bring the device into different operational modes. Each mode has specific operations that can be performed while in that mode. Several modes require a sequence of commands to be written before they are reached. The following section describes the properties of each mode and Table 3 lists all command sequences required to perform the desired operation.

READ ARRAY

The array read mode is the initial state of the device upon powerup, and is also entered after a RESET. If the device is in any other mode, READ ARRAY (FFH) must be given to return to the array read mode. Unlike WRITE SETUP (40H), READ ARRAY does not need to be given before each individual read access.

IDENTIFY DEVICE

The 8-bit device identification may be read using one of two methods. IDENTIFY DEVICE (90H) may be written to the CEL to enter the IDENTIFY DEVICE mode. While in this mode, any read will produce the device identification when A0 is HIGH and manufacturer identification when A0 is LOW. The device will remain in this mode until another command is given.

WRITE SEQUENCE

Two consecutive cycles are needed to input data to the array. WRITE SETUP (40H or 10H) is given in the first cycle. The next cycle is the WRITE, during which the write address and data are issued, and V_{PP} brought to V_{PPH}. Writing to the boot block also requires that the $\overline{RST}$ pin be brought to V_{HH} at the same time V_{PP} is brought to V_{PPH}. The ISM will now begin to write the byte. The desired bits within the byte will be set to logic 0. V_{PP} must be held at V_{PPH} until the write is completed (SR7 = 1). When writing to the boot block, $\overline{RST}$ must be held at V_{HH} until the ISM status bit (SR7) is set.

While the ISM executes the write, the ISM status bit (SR7) will be at 0, and the device will not respond to any commands. However, any read operation will produce the status register contents on DQ0-DQ7. When the ISM status bit (SR7) is set, the write has been completed, and the device will go into the status register read mode until another command is given.

Table 3
COMMAND SEQUENCES

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE			2ND CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY	1	Write	X	FFH				1
IDENTIFY DEVICE	3	Write	X	90H	Read	IA	ID	2, 3
READ STATUS REGISTER	2	Write	X	70H	Read	X	SRD	4
CLEAR STATUS REGISTER	1	Write	X	50H				
ERASE SETUP/CONFIRM	2	Write	X	20H	Write	BA	D0H	5
ERASE SUSPEND/RESUME	2	Write	X	B0H	Write	X	D0H	
WRITE SETUP/WRITE	2	Write	X	40H	Write	WA	WD	6
ALTERNATE WRITE	2	Write	X	10H	Write	WA	WD	6

NOTE:
1. Must follow WRITE or ERASE CONFIRM commands to the CEL in order to enable flash array read cycles.
2. IA = Identify address; 00H for manufacturer ID, 01H for device ID.
3. ID = Indentify data.
4. SRD = Status Register Data.
5. BA = Block address.
6. WA = Address to be written, WD = Data to be written to WA.

After the ISM has initiated the write, it cannot be aborted except by a RESET or by powering-down the part. Doing either during a write will corrupt the data being written. If only the WRITE SETUP command has been given, the write may be nullified by performing a null WRITE. To execute a null WRITE, FFH must be written. Once the ISM status bit (SR7) has been set, the device will be in the status register read mode until another command is issued.

ERASE SEQUENCE

Executing an erase sequence will set all bits within a block to logic 1. The command sequence necessary to execute an erase is similar to that of a write. To provide added security against accidental block erasure, two consecutive command cycles are required to initiate an ERASE of a block. In the first cycle, addresses are "don't care," and ERASE SETUP (20H) is given. In the second cycle, V_{PP} must be brought to V_{PPH}, an address within the block to be erased is issued, and ERASE CONFIRM (D0H) is given. If ERASE CONFIRM is not given, the ISM and erase status bits (SR7 and SR5) will be set, and the device will return to the array read mode.

At this time, the ISM will start the erase of the block. Any read operation will output the status register contents on DQ0-DQ7. V_{PP} must be held at V_{PPH} until the erase is completed (SR7 = 1). Once the erase is completed, the device will be in the status register read mode until another command is issued. Erasing the boot block also requires that the $\overline{RST}$ pin be set to V_{HH} at the same time V_{PP} is set to V_{PPH}.

ERASE SUSPENSION

The only command that may be issued while an erase is in progress is ERASE SUSPEND. This command allows other commands to be executed while pausing the erase in progress. Once the device has reached the erase suspend mode, the erase suspend status bit (SR6) will be set. The device may now be given a READ ARRAY, ERASE RESUME, or READ STATUS REGISTER. After the READ ARRAY command has been issued, any location not within the block being erased may be read. If the ERASE RESUME command is issued before SR6 has been set, the device will immediately proceed with the erase in progress. During the suspend mode V_{PP} must be held at V_{PPH}.

ERROR HANDLING

After the ISM status bit (SR7) has been set, the V_{PP} (SR3), write (SR4), and erase (SR5) status bits may be checked. If one or a combination of these three bits has been set, then an error has occurred. The ISM cannot reset these three bits. To clear these bits, the CLEAR STATUS REGISTER command (50H) must be given. If the V_{PP} status bit (SR3) is set, further write or erase operations cannot resume until the status register is cleared. Table 4 lists the combination of errors.

Table 4
STATUS REGISTER ERROR DECODE[1]

STATUS BITS			
SR5	SR4	SR3	ERROR DESCRIPTION
0	0	0	No errors
0	0	1	V_{PP} voltage error
0	1	0	Write error
0	1	1	Write error, V_{PP} voltage not valid at time of WRITE
1	0	0	Erase error
1	0	1	Erase error, V_{PP} voltage not valid at time of ERASE CONFIRM
1	1	0	Command sequencing error
1	1	1	Command sequencing error, programming voltage error

NOTE: 1. SR3 - SR5 must be cleared using CLEAR STATUS REGISTER.

WRITE/ERASE CYCLE ENDURANCE

The MT28F004 is designed and fabricated to meet advanced firmware storage requirements. To ensure this level of reliability, V_{PP} must be at 12V ±5% during write or erase cycles. Operation outside these limits may reduce the number of erase cycles that can be performed on the device. For further information on write and erase cycle endurance, refer to the Micron *Flash Reliability Monitor*.

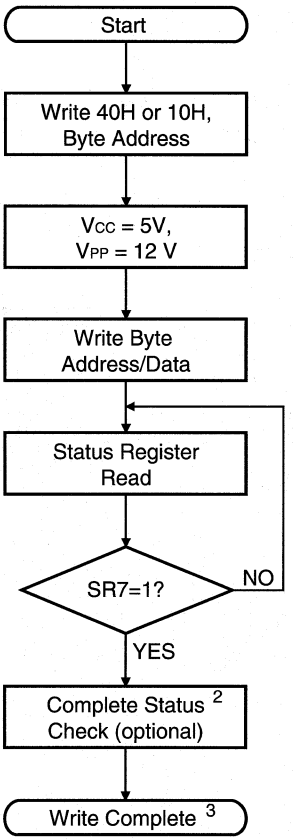
POWER USAGE

The MT28F004 offers several power saving features that may be utilized in the array read mode to conserve power. With $\overline{CE}$ LOW, the device will enter idle current mode when not being accessed. In this mode, the maximum I_{CC} current is 3mA. When $\overline{CE}$ is HIGH, the device will enter standby mode. In this mode, maximum I_{CC} current is 100µA. If $\overline{CE}$ is brought HIGH during an erase or write, the ISM will continue to operate, and the device will consume the respective active power until the write or erase is completed.

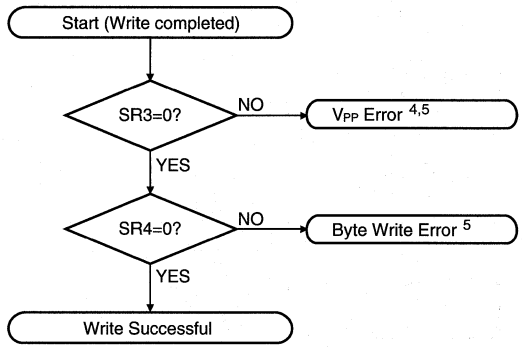
POWERUP

During a powerup, it is not necessary to sequence V_{CC} and V_{PP}. The likelihood of unwanted write or erase operations is minimized, since two consecutive cycles are required to execute either operation. However, $\overline{CE}$ or $\overline{WE}$ may be held HIGH, or $\overline{RST}$ can be held LOW during powerup for additional protection against unwanted write or erase operations. After a powerup or RESET, the status register is reset, and the device will enter the array read mode.

SELF-TIMED WRITE SEQUENCE[1]

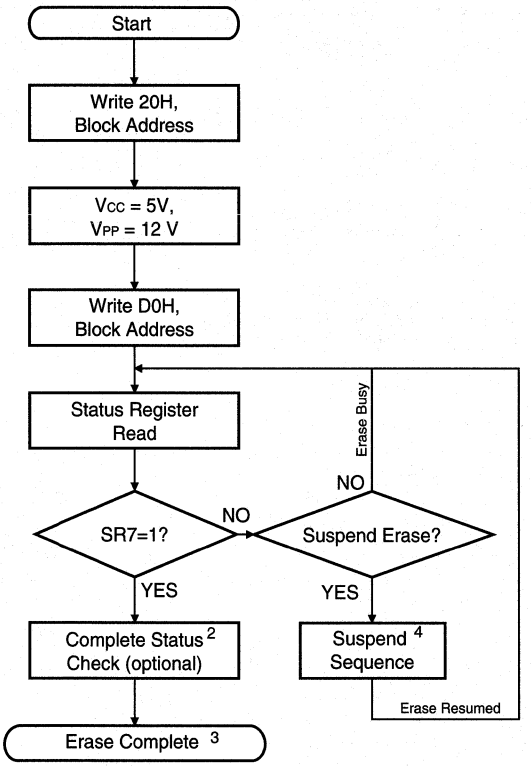


COMPLETE WRITE STATUS-CHECK SEQUENCE

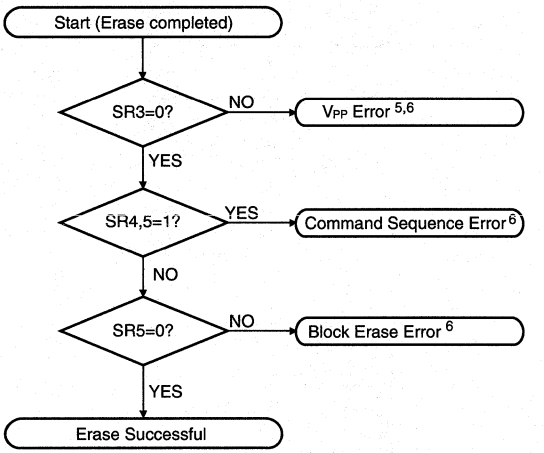


NOTE:
1. Sequence may be repeated for multiple writes.
2. Complete status check is not required. However, if SR3 = 1, further writes are inhibited until the status register is cleared.
3. Device will be in status register read mode. To return to the array read mode, the FFH command must be issued.
4. If SR3 is set during a write or block erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
5. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

SELF-TIMED BLOCK ERASE SEQUENCE[1]

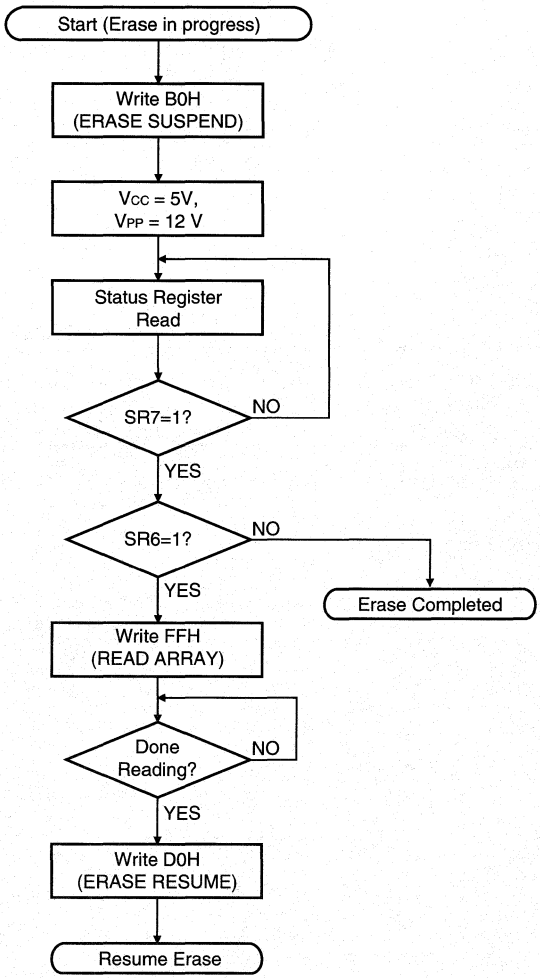


COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



NOTE:
1. Sequence may be repeated to erase multiple blocks.
2. Complete status check is not required. However, if SR3 = 1, further erases are inhibited until the status register is cleared.
3. To return to the array read mode, the FFH command must be issued.
4. Refer to the ERASE SUSPEND flowchart for more information.
5. If SR3 is set during a write or block erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
6. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

ERASE SUSPEND/RESUME SEQUENCE



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -0.5V to +7V
Input Voltage Relative to Vss ..... -0.5V to +7V**
VPP Voltage Relative to Vss ..... -0.5V to +12.6V†
$\overline{RST}$/Pin A9 Voltage Relative to Vss .... -0.5V to +13.5V**,†
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Input and I/O pins may transition to -2.0V for < 20ns and Vcc +2.0V for < 20ns.
†Voltage may pulse to 14.0V ≤ 20ns.

RECOMMENDED DC OPERATING CONDITIONS

(0°C≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-0.5	0.8	V	1
Device Identification Voltage, A9	VID	11.4	13.0	V	1

DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS Output High Voltage (IOH = - 2.5 mA)	VOH	2.4		V	1
Output Low Voltage (IOL = 5.8 mA)	VOL		0.45	V	
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.4V ≤ A9 ≤ 13.0 = VID)	IID		500	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled; 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	

CAPACITANCE

(T_A = 25°C; Vcc = 5V ±10%; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	CI	8	pF	
Output Capacitance	CO	12	pF	

NOTE: 1. All voltages referenced to Vss.

READ AND STANDBY CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
READ CURRENT: TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}); $\overline{RST}$ = V_{IH}	I_{CC1}	60	mA	2, 3
READ CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 10 MHz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V); $\overline{RST}$ = V_{IH}	I_{CC2}	55	mA	2, 3
READ CURRENT: V_{PP} SUPPLY (V_{PP} > V_{CC})	I_{PP1}	200	µA	
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RST}$ = V_{IH}, or $\overline{RST}$ = V_{IL}; other inputs = V_{IL} or V_{IH})	I_{CC3}	1.5	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RST}$ = V_{CC} - 0.2V; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V)	I_{CC4}	100	µA	
STANDBY CURRENT: V_{PP} SUPPLY (V_{PP} ≤ V_{CC})	I_{PP2}	±10	µA	
IDLE CURRENT: TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 0 Hz; Other inputs = V_{IL} or V_{IH}; $\overline{RST}$ = V_{IH}; array read mode)	I_{CC5}	3	mA	
IDLE CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 0 Hz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V; $\overline{RST}$ = V_{IH}; READ ARRAY)	I_{CC6}	3	mA	

WRITE/ERASE CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
WRITE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC7}	60	mA	
WRITE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP3}	30	mA	
ERASE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC8}	30	mA	
ERASE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP4}	30	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%; erase suspended)	I_{CC9}	10	mA	4
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%; erase suspended)	I_{PP5}	200	µA	

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	70		80		100		ns	6
Access time from $\overline{CE}$	^tACE		70		80		100	ns	5,6
Access time from $\overline{OE}$	^tAOE		35		40		50	ns	5,6
Access time from address	^tAA		70		80		100	ns	6
$\overline{RST}$ HIGH to output valid delay	^tRWH		300		300		300	ns	6
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		25		30		40	ns	6
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		0		0		ns	6

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	60		ns	7
Access time from $\overline{CE}$	^tACE		60	ns	5,7
Access time from $\overline{OE}$	^tAOE		30	ns	5,7
Access time from address	^tAA		60	ns	7
$\overline{RST}$ HIGH to output valid delay	^tRWH		300	ns	7
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		20	ns	7
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		ns	7

AC TEST CONDITION–1

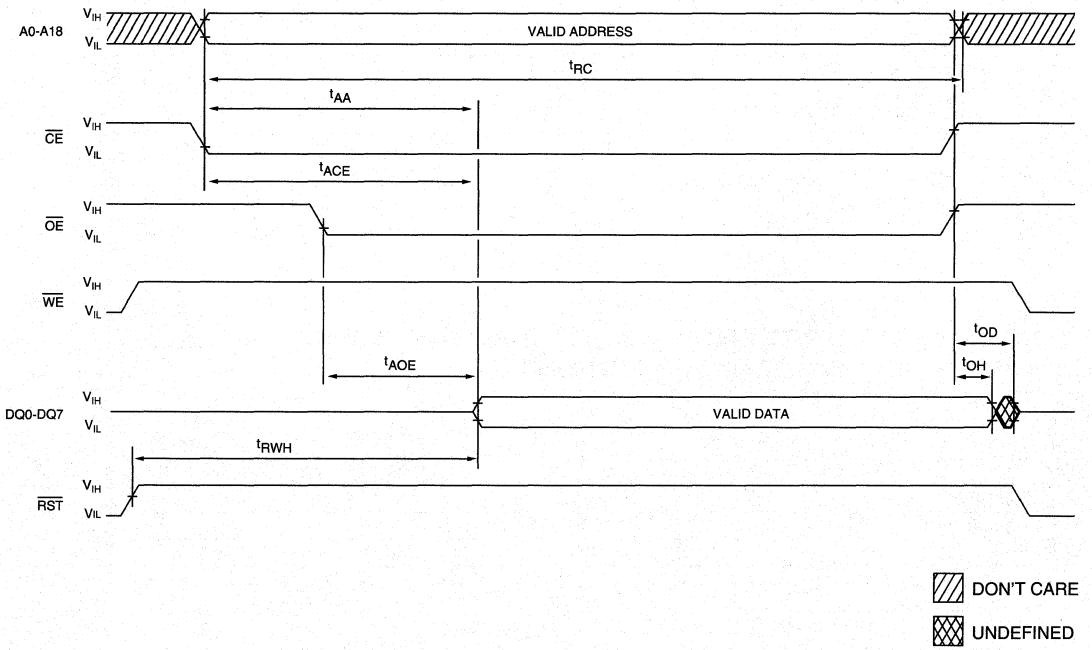
Input pulse levels	0.4 to 2.4V
Input rise and fall times	<10ns
Input timing reference level	0.8 V and 2.0 V
Output timing reference level	0.8 V and 2.0 V
Output load	1 TTL gate and C_L = 100 pF

AC TEST CONDITION–2

Input pulse levels	0.0 to 3.0V
Input rise and fall times	<10ns
Input timing reference level	1.5 V
Output timing reference level	1.5 V
Output load	1 TTL gate and C_L = 30 pF

NOTE:
1. All voltages referenced to Vss.
2. Icc is dependent on cycle rates.
3. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Parameter is specified when device is not accessed. Actual current draw will be Icc9 plus read current if a read is executed while in erase suspend mode.
5. $\overline{OE}$ may be delayed by ^tACE minus ^tAOE after $\overline{CE}$ falls before ^tACE is affected.
6. Measurements tested under AC Test Conditions-1.
7. Measurements tested under AC Test Conditions-2.

READ CYCLE



RECOMMENDED DC WRITE/ERASE CONDITIONS

($0°C \le T_A \le +70°C$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
V_{PP} voltage during normal operation	V_{PPL}	0.0	6.5	V	
V_{PP} voltage during erase/write operation	V_{PPH}	11.4	12.6	V	
Boot block unlock voltage	V_{HH}	11.4	13.0	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT: $\overline{RST}$ INPUT ($11.4 \le \overline{RST} \le 13.0V = V_{HH}$)	I_{HH}		500	µA	

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	70		80		100		ns	1
$\overline{WE}$ HIGH pulse width	^tWPH	20		20		30		ns	1
$\overline{CE}$ HIGH pulse width	^tCPH	20		20		30		ns	1

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	60		ns	2
$\overline{WE}$ HIGH pulse width	^tWPH	10		ns	2
$\overline{CE}$ HIGH pulse width	^tCPH	10		ns	2

NOTE: 1. Measurements tested under AC Test Conditions-1.
2. Measurements tested under AC Test Conditions-2.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{WE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10% or ±5%)

AC CHARACTERISTICS		-6, -8, -10			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{WE}$ HIGH	^tAS	50		ns	
Address hold time from $\overline{WE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{WE}$ HIGH	^tDS	50		ns	
Data hold time from $\overline{WE}$ HIGH	^tDH	0		ns	
$\overline{CE}$ setup time to $\overline{WE}$ LOW	^tCS	0		ns	
$\overline{CE}$ hold time from $\overline{WE}$ HIGH	^tCH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	100		ns	1
$\overline{WE}$ pulse width	^tWP	50		ns	
$\overline{RST}$ HIGH to $\overline{WE}$ LOW delay	^tRS	220		ns	
$\overline{RST}$ V_{HH} setup time to $\overline{WE}$ HIGH	^tRHS	100		ns	2
Write duration	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		100	ns	3

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{CE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10% or ±5%)

AC CHARACTERISTICS		-6, -8, -10			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{CE}$ HIGH	^tAS	50		ns	
Address hold time from $\overline{CE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{CE}$ HIGH	^tDS	50		ns	
Data hold time from $\overline{CE}$ HIGH	^tDH	0		ns	
$\overline{WE}$ setup time to $\overline{CE}$ LOW	^tWS	0		ns	
$\overline{WE}$ hold time from $\overline{CE}$ HIGH	^tWH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	100		ns	1
$\overline{CE}$ pulse width	^tCP	50		ns	
$\overline{RST}$ HIGH to $\overline{CE}$ LOW delay	^tRS	220		ns	
$\overline{RST}$ V_{HH} setup time to $\overline{CE}$ HIGH	^tRHS	100		ns	2
Write duration	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1, 2
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		100	ns	2

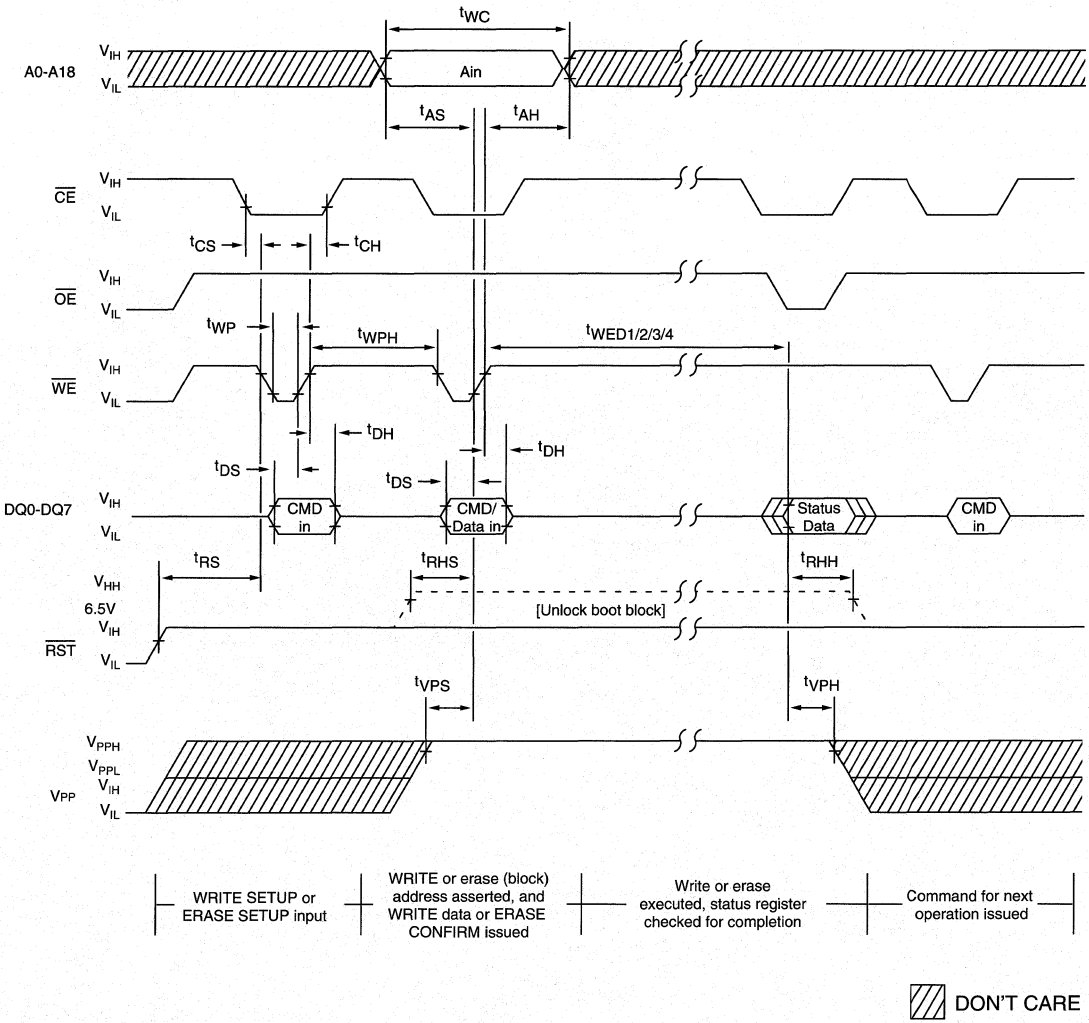
NOTE: 1. Write/erase times are measured to valid status register data (SR7=1).
2. $\overline{RST}$ should be held at V_{HH} until boot-block write or erase is complete.
3. ^tREL is required to relock boot block after write or erase to boot block.

WRITE AND ERASE DURATION CHARACTERISTICS

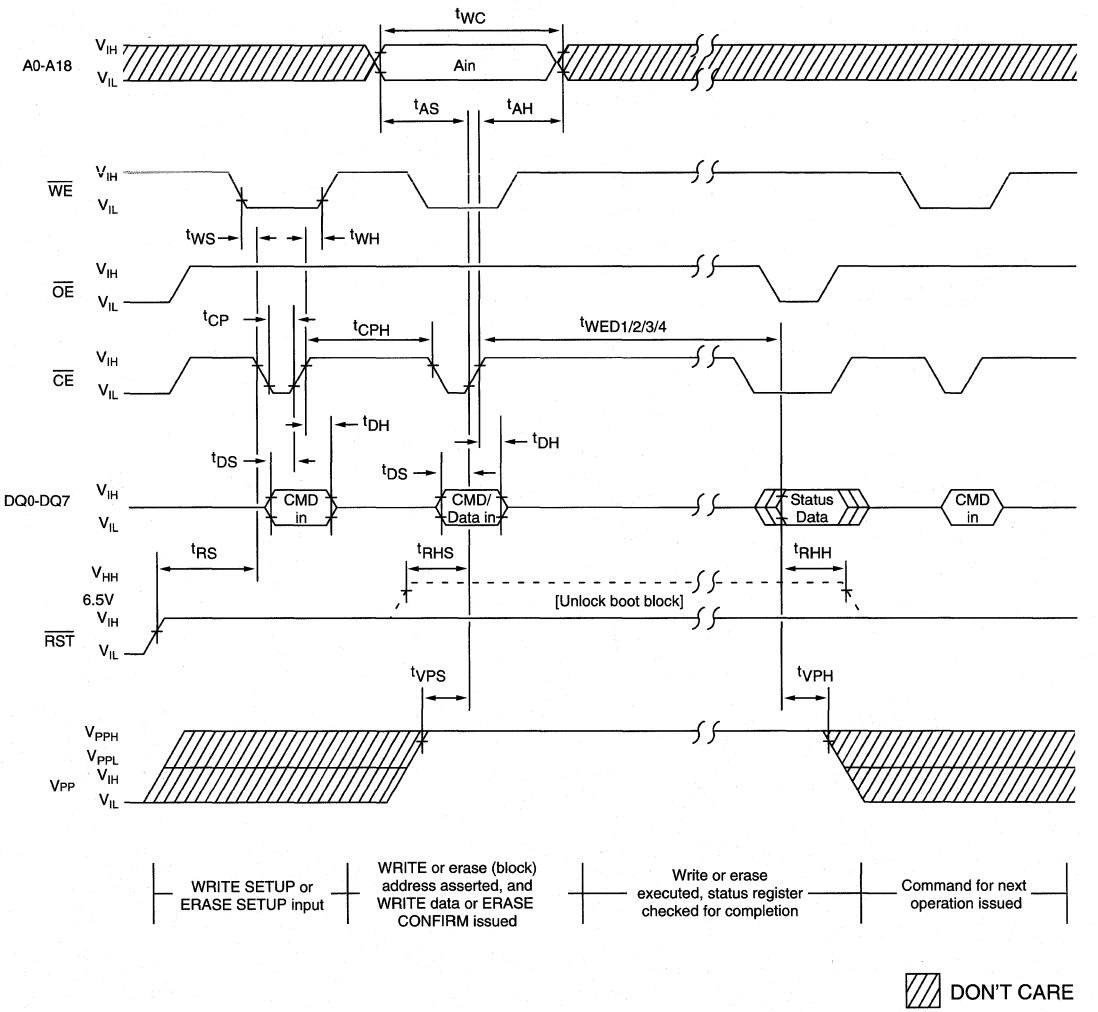
PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Boot/parameter block erase time		1.0	7.0	s	1
Main block erase time		2.5	14.0	s	1
Main block write time		1.0	4.0	s	1, 2

NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.

ERASE/WRITE CYCLE
$\overline{WE}$-CONTROLLED WRITE/ERASE



ERASE/WRITE CYCLE
$\overline{CE}$-CONTROLLED WRITE/ERASE



NEW 5/12 VOLT FLASH MEMORY

FLASH MEMORY

256K x 16, 512K x 8

5V/12V, BOOT BLOCK

FEATURES

- Seven erase blocks:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Four general memory blocks
- Low power: 100µA standby; 60mA active, MAX
- 5V±10% read; 12V±5% write/erase
- Address access times: 60ns, 80ns, 100ns
- Selectable organizations: 262,144 x 16 or 524,288 x 8
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm
- Byte- or word-wide write
- TSOP packaging option

OPTIONS

	MARKING
• Timing	
60ns access	- 6
80ns access	- 8
100ns access	-10
• Boot-Block Starting Address	
Top (3FFFFH)	T
Bottom (00000H)	B
• Packages	
Plastic SOP (600 mil)	SG
Plastic TSOP Type 1 (14 x 20mm)	VG

- Part Number Example: MT28F400SG-8T

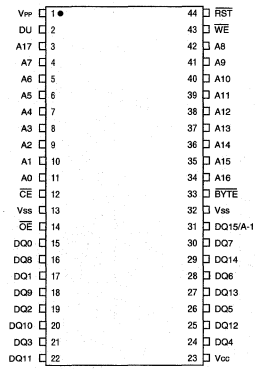
GENERAL DESCRIPTION

The MT28F400 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 4,194,304 bits organized as 262,144 words by 16 bits or 524,288 words by 8 bits. It is fabricated with Micron's advanced CMOS floating-gate process.

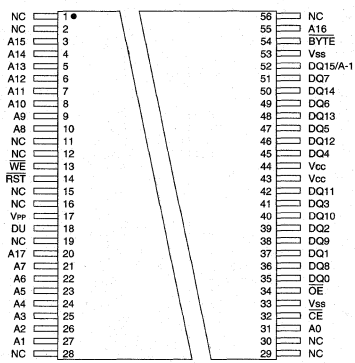
The MT28F400 is organized into seven separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F400 features a hardware-protected boot-block. Writing or erasing the boot block requires a super-voltage on the $\overline{RST}$ pin in addition to executing the normal write or erase sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density, and are written-to and erased with no additional super-voltage required.

PIN ASSIGNMENT (Top View)

44-Pin SOP (FA-1)

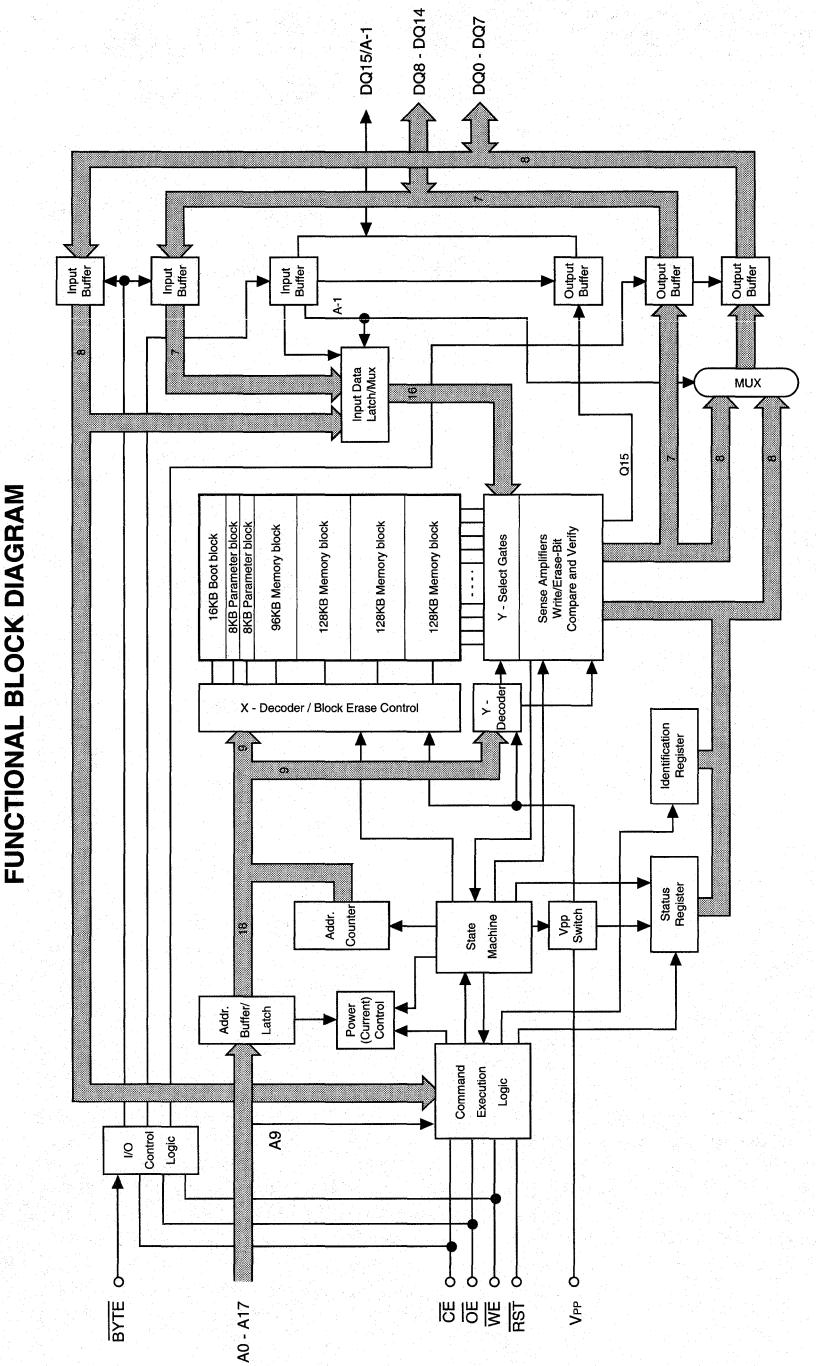


56-Pin TSOP Type I (FB-2)



The byte or word address is issued to read the memory array with $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH. Valid data is output until the next address is issued. The $\overline{BYTE}$ pin is used to switch the data path between 8 bits wide and 16 bits wide. When $\overline{BYTE}$ is LOW, the dual-use pin DQ15/A-1 becomes the lowest order address bit (A-1). When $\overline{BYTE}$ is HIGH, the DQ15/A-1 pin becomes the most significant data bit (DQ15).

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
43	13	$\overline{WE}$	Input	Write Enable: Determines if a given cycle is a write cycle. If $\overline{WE}$ = LOW when $V_{PP} < V_{PPH}$, the cycle is a write to the Command Execution Logic (CEL). If $\overline{WE}$ = LOW when $V_{PP} = V_{PPH}$, the cycle is a WRITE to one of the sectors or an ERASE CONFIRM.
12	32	$\overline{CE}$	Input	Chip Enable: Activates the device when LOW. When $\overline{CE}$ is HIGH, the device is disabled and goes into standby power mode.
44	14	$\overline{RST}$	Input	Reset: Clears the status register, sets the Internal State Machine (ISM) to the array read mode, and places the device in standby mode when LOW. All inputs, including $\overline{CE}$, are "don't care," and all outputs are High-Z. Also used to unlock boot block when brought to V_{HH} (boot-block unlock voltage; 12V). Must be held HIGH during all other modes of operation.
14	34	$\overline{OE}$	Input	Output Enable: Enables data output buffers.
33	54	$\overline{BYTE}$	Input	Byte Enable: If $\overline{BYTE}$=HIGH the upper byte is active through DQ8-DQ15. If $\overline{BYTE}$=LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34, 3	31, 27, 26, 25, 24, 23, 22, 21, 10, 9, 8, 7, 6, 5, 4, 3, 55, 20	A0-A17	Input	Address Inputs: Selects a unique, 16-bit word out of the 262,144 available. The DQ15/A-1 input becomes the lowest order address when $\overline{BYTE}$=LOW to allow for selection of an 8-bit byte from 524,288 available.
31	52	DQ15/A-1	Input/ Output	Data I/O: MSB of data when $\overline{BYTE}$ = HIGH. Address Input: LSB of address input when $\overline{BYTE}$ = LOW during read or write operation. Not used during erase or read device ID.
15, 17, 19, 21, 24, 26, 28, 30	35, 37, 39, 41, 45, 47, 49, 51	DQ0-DQ7	Input/ Output	Data I/O: Data output pins during any read operation, or data input pins during a WRITE. Used to input commands to the CEL or a command input.
16, 18, 20, 22, 25, 27, 29	36, 38, 40, 42, 46, 48, 50	DQ8-DQ14	Input/ Output	Data I/O: Data output pins during any read operation or data input pins during a WRITE when $\overline{BYTE}$ = HIGH. High-Z when $\overline{BYTE}$ is LOW.
	1, 2, 11, 12, 15, 16, 19, 28, 29, 30, 56	NC	-	No Connect: These pins may be driven or left unconnected.
2	18	DU	-	Don't Use: This pin must be left unconnected in the system.
1	17	V_{PP}	Supply	Write/Erase Supply Voltage: During a WRITE or ERASE CONFIRM, $V_{PP} = V_{PPH}$ (12V). V_{PP} = "don't care" during all other operations.
23	43, 44	Vcc	Supply	Power Supply: +5V ±10%
13, 32	33, 53	Vss	Supply	Ground

TRUTH TABLE [1]

FUNCTION	$\overline{RST}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READING											
16-bit Read	H	L	L	H	H	X	X	X	Data-Out	Data-Out	Data-Out
8-bit Read	H	L	L	H	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE [2]											
ERASE SETUP	H	L	H	L	X	X	X	X	20H	X	X
ERASE CONFIRM [3]	H	L	H	L	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H	X	X
16-bit WRITE [4]	H	L	H	L	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
8-bit WRITE [4]	H	L	H	L	L	X	X	V_{PPH}	Data-In	High-Z	A-1
READ ARRAY	H	L	H	L	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK) [2, 5]											
ERASE SETUP	H	L	H	L	X	X	X	X	20H	X	X
ERASE CONFIRM [3]	V_{HH}	L	H	L	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H	X	X
16-bit WRITE [4]	V_{HH}	L	H	L	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
8-bit WRITE [4]	V_{HH}	L	H	L	L	X	X	V_{PPH}	Data-In	High-Z	A-1
READ ARRAY	H	L	H	L	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION [6, 7]											
Manufacturer (16-bit) [8]	H	L	L	H	H	L	V_{ID}	X	2CH	00H	-
Manufacturer (8-bit)	H	L	L	H	L	L	V_{ID}	X	2CH	High-Z	X
Device (16-bit, top boot) [8]	H	L	L	H	H	H	V_{ID}	X	B0H	44H	-
Device (8-bit, top boot)	H	L	L	H	L	H	V_{ID}	X	B0H	High-Z	X
Device (16-bit, bottom boot) [8]	H	L	L	H	H	H	V_{ID}	X	B1H	44H	-
Device (8-bit, bottom boot)	H	L	L	H	L	H	V_{ID}	X	B1H	High-Z	X

NOTE:
1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. V_{PPH} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. V_{HH} = 12V.
6. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE Command.
7. A1-A8, A10-A17 = V_{IL}.
8. Value reflects DQ8-DQ15.

FUNCTIONAL DESCRIPTION

The MT28F400 Flash memory incorporates a number of features to make it ideally suited for system firmware.

The memory array is segmented into individual erase blocks. Each block may be erased without affecting data stored in other blocks. These memory blocks are read, written and erased by issuing commands to the Command Execution Logic (CEL). The CEL controls the operation of the Internal State Machine (ISM) that completely controls all write, block erase, and verify operations. This state machine protects each memory location from over-erasure and optimizes each memory location for maximum data retention. In addition, the ISM greatly simplifies the control necessary for writing the device in-system or in an external programmer.

The Functional Description provides detailed information on the operation of the MT28F400, and is organized into these sections:

- Overview
- Memory Architecture
- Output (Read) Operations
- Input Operations
- Command Set
- ISM Status Register
- Command Execution
- Error Handling
- Write/Erase Cycle Endurance
- Power Usage
- Powerup

OVERVIEW

SEVEN INDEPENDENTLY ERASABLE MEMORY BLOCKS

The MT28F400 is organized into seven independently erasable memory blocks that allow portions of the memory to be erased without affecting the rest of the memory data. A special boot block is hardware-protected against inadvertent erasure or writes by a super-voltage pin. The voltage on this pin is required in addition to the 12V on the V_{PP} pin. The remaining blocks require only the 12V V_{PP} to be present in order to be changed.

HARDWARE-PROTECTED BOOT-BLOCK

This block of the memory array can be erased or written only when the $\overline{RST}$ pin is taken to V_{HH}. Designing a system so that the processor or control logic is unable to apply 12V to this pin will ensure data integrity in this memory block. This provides additional security for the core firmware during in-system firmware updates, should an unintentional power fluctuation or system reset occur. The MT28F400 is available in two versions; the MT28F400T addresses the boot block starting from 3FFFFH, and the MT28F400B addresses the boot block starting from 00000H.

CONFIGURABLE BUS SIZE

The MT28F400T/B allows dynamic selection of an 8-bit (512K x 8) or 16-bit (256K x 16) data bus for reading and writing the memory. The $\overline{BYTE}$ pin is used to select the bus width. When in the x16 configuration, control data is read or written only on the lower 8 bits (DQ0-DQ7).

Data written to the memory array utilize all active data pins for the selected configuration. When the x8 configuration is selected, data is written in byte form; when in the x16 configuration, data is written in the word form.

INTERNAL STATE MACHINE (ISM)

Block erase and byte/word write timing are simplified by using an ISM to control all erase and write algorithms in the memory array. The ISM ensures protection against overerasure and optimizes write margin to each cell.

During write operations the ISM automatically increments and monitors write attempts, verifies write margin on each memory cell, and updates the ISM status register. When block erase is performed the ISM automatically overwrites the entire addressed block (eliminates over-erasure), increments and monitors erase attempts, and sets bits in the ISM status register.

ISM STATUS REGISTER

The ISM status register allows an external processor to monitor the status of the ISM during write and erase operations. Two bits of the 8-bit status register are set and cleared entirely by the ISM. These bits indicate whether the ISM is busy with an erase or write task, and when an erase has been suspended. Additional error information is set in the other three bits: valid programming voltage, write error, and erase error.

COMMAND EXECUTION LOGIC (CEL)

The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the read path (i.e. memory array, ID register, or status register). Commands may be issued to the CEL while the ISM is active. However, there are restrictions on what commands are allowed in this condition. See the Command Execution section for more detail.

MEMORY ARCHITECTURE

The MT28F400 memory array architecture is designed to allow sections to be erased without disturbing the rest of the array. The array is divided into seven addressable "blocks" that are of varying size and independently erasable. By erasing in blocks, rather than the entire array, the total device endurance is enhanced, as is system flexibility. Only the erase function is block oriented. All read and write operations are done on a random word- or byte-basis.

The boot block is protected from unintentional erase or write with a hardware protection circuit that requires a super-voltage be applied before erasure is commenced. The boot block is intended for the core firmware required for basic system functionality. The remaining six blocks do not require this super-voltage before being written or erased.

BOOT BLOCK

The hardware-protected boot-block provides extra security for the most sensitive portions of the firmware. This 16KB block may only be erased or written when the $\overline{RST}$ pin is at the specified boot block unlock voltage (V_{HH}) of 12V. When performing erase or write cycles to this block, $\overline{RST}$ must be held at the unlock voltage (V_{HH}) until the erase or write is completed. As for any erase or write operations, the V_{PP} pin must be at V_{PPH} when writing to the boot block.

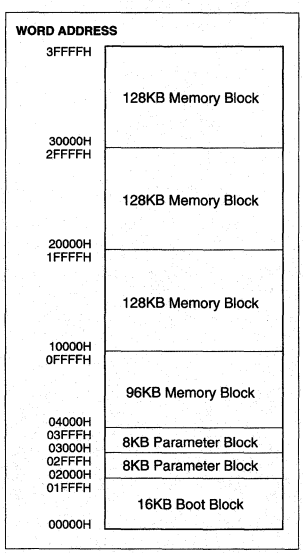
The MT28F400 is available in two configurations, top or bottom boot-block. The MT28F400T top boot-block version supports processors of the x86 variety. The MT28F400B bottom boot-block version is intended for 680X0 and RISC applications. Figure 1 illustrates the memory address maps associated with these two versions.

PARAMETER BLOCKS

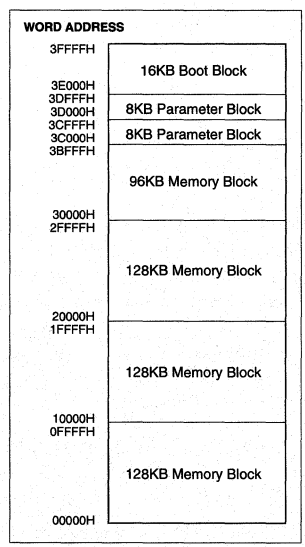
The two 8KB parameter blocks are used for storage of less sensitive and more frequently changing system parameters and also may include configuration or diagnostic coding. These blocks are enabled for erasure when the V_{PP} pin is at V_{PPH}. No super-voltage unlock is required.

GENERAL MEMORY BLOCKS

The four remaining blocks are general memory blocks and do not require a super-voltage on $\overline{RST}$ to be erased or written. These blocks are intended for code storage, or ROM-resident applications or operating systems that require in-system update capability.



Bottom Boot - MT28F400xx-xxB



Top Boot - MT28F400xx-xxT

Figure 1
MEMORY ADDRESS MAPS

OUTPUT (READ) OPERATIONS

The MT28F400 features three different types of reads. Depending on the current mode of the device, a read operation will produce data from the memory array, status register, or device identification register. In each of these three cases, the $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$ inputs are controlled in a similar manner to perform a read. However, several differences exist, and are described in the following section. Moving between modes to perform a specific read will be covered in the Command Execution section.

MEMORY ARRAY

To read the memory array, $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. Valid data will be output on the DQ pins once these conditions have been met and a valid address is given. Valid data will remain on the DQ pins until the address changes, or $\overline{OE}$ or $\overline{CE}$ go HIGH, whichever occurs first. The DQ pins will continue to output new data after each address transition, as long as $\overline{OE}$ and $\overline{CE}$ remain LOW.

The MT28F400 features dynamically sizable bus widths. When configured as 256K x 16 ($\overline{BYTE}$ is HIGH), data will be output on DQ0-DQ15. To configure the memory array as a 512K x 8, $\overline{BYTE}$ must be LOW. DQ8 - DQ14 are now "High-Z," and all data is output on DQ0-DQ7. The DQ15/A-1 pin now becomes the lowest order address input, so that 512,288 locations can be read.

After powerup or RESET, the device will automatically be in the array read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

STATUS REGISTER

Performing a read of the status register requires the same input sequencing as when reading the array, except that the address inputs are "don't care." The status register contents are always output on DQ0-DQ7, regardless of the condition of $\overline{BYTE}$. DQ8-DQ15 are LOW when $\overline{BYTE}$ is HIGH, and DQ8-DQ14 are High-Z when $\overline{BYTE}$ is LOW. Data from the status register is latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last. If the contents of the status register change during a read of the status register, either $\overline{OE}$ or $\overline{CE}$ may be toggled while the other is held LOW to update the output.

Following a write or erase, the device automatically enters the status register read mode. In addition, a read during a write or erase will produce the status register contents on DQ0-DQ7. When in the erase suspend mode, a read operation will produce the status register contents until another command is issued. While in certain other modes, READ STATUS REGISTER may be given to return to the status register read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

IDENTIFICATION REGISTER

A read of the two 8-bit device identification registers requires the same input sequencing as when reading the array. $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. However, ID register data is output only on DQ0-DQ7, regardless of the condition of $\overline{BYTE}$. A0 is used to decode between the two bytes of the device ID register; all other address inputs are "don't care." When A0 is LOW, the manufacturer ID is output, and when A0 is HIGH, the device ID is output. DQ8-DQ15 are "High-Z" when $\overline{BYTE}$ is LOW. When $\overline{BYTE}$ is HIGH, DQ8-DQ15 is 00H when the manufacturer ID is read, and 44H when the device is read.

To get to the identification register read mode, READ IDENTIFICATION may be issued while in certain other modes. In addition, the identification register read mode can be reached by applying a super-voltage (V_{ID}) to the A9 pin. Using this method, the ID register can be read while in any mode. Once A9 is returned to V_{IL} or V_{IH}, the device will return to the previous mode.

INPUT OPERATIONS

The DQ pins are used to either input data to the array or input a command to the CEL. A command input issues an 8-bit command to the CEL. Commands may be issued to control operation of the part. A WRITE is used to input data to the memory array. The following section describes both types of inputs. More information describing how to use the two types of inputs to write the device is provided in the Command Execution section.

COMMANDS

To perform a command input, $\overline{OE}$ must be HIGH, and $\overline{CE}$ and $\overline{WE}$ must be LOW. A0-A17 are not used for command inputs, except during an ERASE CONFIRM (described in a later section). The 8-bit command is input on DQ0-DQ7, while DQ8-DQ15 are "don't care." The command is latched on the rising edge of $\overline{CE}$ ($\overline{CE}$ controlled) or $\overline{WE}$ ($\overline{WE}$ controlled), whichever occurs first. The condition of $\overline{BYTE}$ has no effect on a command input.

MEMORY ARRAY

A write to the memory array sets the desired bits to logic 0's, but cannot change a given bit to a logic 1 from a logic 0. Setting any bits to a logic 1 requires that the entire block be erased. To perform a WRITE, $\overline{OE}$ must be HIGH, $\overline{CE}$ and $\overline{WE}$ must be LOW, and V_{PP} must be set to V_{PPH}. Writing to

the boot block also requires that the $\overline{RST}$ pin be at V_{HH}. A0-A17 provide the address to be written, while the data to be written to the array is input on the DQ pins. The data and addresses are latched on the rising edge of $\overline{CE}$ ($\overline{CE}$-controlled) or $\overline{WE}$ ($\overline{WE}$-controlled), whichever occurs first. A WRITE must be preceeded by a WRITE SETUP command. Detail on how to input data to the array will be covered in the Write Sequence section.

Dynamic bus sizing applies to writes as it does for reads. When $\overline{BYTE}$ is LOW (BYTE mode), data is input on DQ0-DQ7, DQ8-DQ14 are "High-Z," and DQ15 becomes the lowest order address input. To WRITE in x16 (WORD) mode, $\overline{BYTE}$ is HIGH, and data is input on DQ0-DQ15.

COMMAND SET

To simplify writing of the memory blocks, the MT28F400 incorporates an ISM that controls all internal algorithms for the write and erase cycles. An 8-bit command set is used to control the device. Detail on how to sequence commands is provided in the Command Execution section. Table 1 lists the valid commands.

Table 1
COMMAND SET

COMMAND	HEX CODE	DESCRIPTION
RESERVED	00H	This command and all unlisted commands are invalid, and should not be called. These commands are reserved to allow for future feature enhancements.
READ ARRAY	FFH	Must be issued after any other command cycle before the array can be read. It is not necessary to issue this command after powerup or reset.
IDENTIFY DEVICE	90H	Allows the device and manufacturer ID to be read. A0 is used to decode between the manufacturer ID (A0=LOW) and device ID (A0=HIGH).
READ STATUS REGISTER	70H	Allows the status register to be read. Please refer to Table 2 for more information on the status register bits.
CLEAR STATUS REGISTER	50H	Clears status register bits 3 through 5, which cannot be cleared by the ISM.
ERASE SETUP	20H	The first command given in the two cycle erase sequence. The erase will not be completed unless followed by ERASE CONFIRM.
ERASE CONFIRM/RESUME	D0H	The second command given in the two cycle erase sequence. Must follow an ERASE SETUP command to be valid. Also used during an ERASE SUSPEND to resume the erase.
WRITE SETUP	40H or 10H	The first command given in the two cycle write sequence. The write data and address are given in the following cycle to complete the write.
ERASE SUSPEND	B0H	Halts the erase and puts device into the erase suspend mode. When in this mode only READ STATUS REGISTER, READ ARRAY, and ERASE RESUME commands may be executed.

ISM STATUS REGISTER

The 8-bit ISM status register (see Table 2) is polled to check for write or erase completion or any related errors. During or following a write, erase, or erase suspend, a read operation will output the status register contents on DQ0 - DQ7 without prior command. While reading the status register contents, the outputs will not be updated if there is a change in the ISM status unless $\overline{OE}$ or $\overline{CE}$ is toggled. If the device is not in the write, erase, erase suspend, or status register read mode, READ STATUS REGISTER (70H) can be issued to view the status register contents.

All of the defined bits are set by the ISM, but only the ISM and erase suspend status bits are reset by the ISM. The erase, write, and VPP status bits must be cleared using CLEAR STATUS REGISTER. If the VPP status bit (SR3) is set, the CEL will not allow further write or erase operations until the status register is cleared. This allows the user to choose when to poll and clear the status register. For example, the host system may perform multiple byte write operations before checking the status register, instead of checking after each individual write. Asserting the $\overline{RST}$ signal or powering down the device are other methods to clear the status register.

Table 2
STATUS REGISTER

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	ISM STATUS 1 = Ready 0 = Busy	The ISMS bit displays the active status of the state machine when performing write or block erase. The controlling logic polls this bit to determine when the erase and write status bits are valid.
SR6	ERASE SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed	Issuing an ERASE SUSPEND places the ISM in the suspend mode and sets this and the ISMS bit to "1." The ESS bit will remain "1" until an ERASE RESUME is issued.
SR5	ERASE STATUS 1 = Block erase error 0 = Successful block erase	ES is set to "1" after the maximum amount of erase cycles are executed by the ISM without a successful verify. ES is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR4	WRITE STATUS 1 = Write (word/byte) error 0 = Successful word/byte write	WS is set to "1" after the maximum amount of write cycles are executed by the ISM without a successful verify. WS is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR3	VPP STATUS 1 = No VPP voltage detected 0 = VPP present	VPPS detects the presence of a VPP voltage. It does not monitor VPP continously nor does it indicate a valid VPP voltage. The VPP pin is sampled for 12V after WRITE or ERASE CONFIRM is given. Must be cleared by CLEAR STATUS REGISTER or after a RESET.
SR0-2	RESERVED	Reserved for future use

COMMAND EXECUTION

Commands are issued to bring the device into different operational modes. Each mode has specific operations that can be performed while in that mode. Several modes require a sequence of commands to be written before they are reached. The following section describes the properties of each mode and Table 3 lists all command sequences required to perform the desired operation.

READ ARRAY

The array read mode is the initial state of the device upon powerup, and is also entered after a RESET. If the device is in any other mode, READ ARRAY (FFH) must be given to return to the array read mode. Unlike the WRITE SETUP command (40H), READ ARRAY does not need to be given before each individual read access.

IDENTIFY DEVICE

The 8-bit device identification may be read using one of two methods. IDENTIFY DEVICE (90H) may be written to the CEL to enter the identify device mode. While in this mode, any read will produce the device identification when A0 is HIGH and manufacturer identification when A0 is LOW. The device will remain in this mode until another command is given.

WRITE SEQUENCE

Two consecutive cycles are needed to input data to the array. WRITE SETUP (40H or 10H) is given in the first cycle. The next cycle is the WRITE, during which the write address and data are issued, and V_{PP} brought to V_{PPH}. Writing to the boot block also requires that the $\overline{RST}$ pin be brought to V_{HH} at the same time V_{PP} is brought to V_{PPH}. The ISM will now begin to write the word or byte. The desired bits within the word will be set to logic 0. V_{PP} must be held at V_{PPH} until the write is completed (SR7 = 1). When writing to the boot block, $\overline{RST}$ must be held at V_{HH} until the ISM status bit (SR7) is set.

While the ISM executes the write, the ISM status bit (SR7) will be at 0, and the device will not respond to any commands. However, any read operation will produce the status register contents on DQ0-DQ7. When the ISM status bit (SR7) is set, the write has been completed, and the device will go into the status register read mode until another command is given.

Table 3
COMMAND SEQUENCES

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE			2ND CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY	1	Write	X	FFH				1
IDENTIFY DEVICE	3	Write	X	90H	Read	IA	ID	2, 3
READ STATUS REGISTER	2	Write	X	70H	Read	X	SRD	4
CLEAR STATUS REGISTER	1	Write	X	50H				
ERASE SETUP/CONFIRM	2	Write	X	20H	Write	BA	D0H	5
ERASE SUSPEND/RESUME	2	Write	X	B0H	Write	X	D0H	
WRITE SETUP/WRITE	2	Write	X	40H	Write	WA	WD	6
ALTERNATE WORD /BYTE WRITE	2	Write	X	10H	Write	WA	WD	6

NOTE:
1. Must follow WRITE or ERASE CONFIRM commands to the CEL in order to enable flash array read cycles.
2. IA = Identify address; 00H for manufacturer ID, 01H for device ID.
3. ID = Indentify data.
4. SRD = Status Register Data.
5. BA = Block address.
6. WA = Address to be written, WD = Data to be written to WA.

After the ISM has initiated the write, it cannot be aborted except by a RESET or by powering-down the part. Doing either during a write will corrupt the data being written. If only the WRITE SETUP command has been given, the write may be nullified by performing a null WRITE. To execute a null WRITE, FFH must be written when $\overline{BYTE}$ is LOW, or FFFFH must be written when $\overline{BYTE}$ is HIGH. Once the ISM status bit (SR7) has been set, the device will be in the status register read mode until another command is issued.

ERASE SEQUENCE

Executing an erase sequence will set all bits within a block to logic 1. The command sequence necessary to execute an erase is similar to that of a write. To provide added security against accidental block erasure, two consecutive command cycles are required to initiate an erase of a block. In the first cycle, addresses are "don't care," and ERASE SETUP (20H) is given. In the second cycle, V_{PP} must be brought to V_{PPH}, an address within the block to be erased is issued, and ERASE CONFIRM (D0H) is given. If ERASE CONFIRM is not given, the ISM and erase status bits (SR7 and SR5) will be set, and the device will return to the array read mode.

At this time, the ISM will start the erase of the block. Any read operation will output the status register contents on DQ0-DQ7. V_{PP} must be held at V_{PPH} until the erase is completed (SR7 = 1). Once the erase is completed, the device will be in the status register read mode until another command is issued. Erasing to the boot block also requires that the $\overline{RST}$ pin be set to V_{HH} at the same time V_{PP} is set to V_{PPH}.

ERASE SUSPENSION

The only command that may be issued while an erase is in progress is ERASE SUSPEND. This command allows other commands to be executed while pausing the erase in progress. Once the device has reached the erase suspend mode, the erase suspend status bit (SR6) will be set. The device may now be given a READ ARRAY, ERASE RESUME, or READ STATUS REGISTER command. After READ ARRAY has been issued, any location not within the block being erased may be read. If ERASE RESUME is issued before SR6 has been set, the device will immediately proceed with the erase in progress. During the suspend mode V_{PP} must be held at V_{PPH}.

ERROR HANDLING

After the ISM status bit (SR7) has been set, the V_{PP} (SR3), write (SR4), and erase (SR5) status bits may be checked. If one or a combination of these three bits has been set, then an error has occurred. The ISM cannot reset these three bits. To clear these bits, CLEAR STATUS REGISTER (50H) must be given. If the V_{PP} status bit (SR3) is set, further write or erase operations cannot resume until the status register is cleared. Table 4 lists the combination of errors.

Table 4
STATUS REGISTER ERROR DECODE[1]

STATUS BITS			
SR5	SR4	SR3	ERROR DESCRIPTION
0	0	0	No errors
0	0	1	V_{PP} voltage error
0	1	0	Write error
0	1	1	Write error, V_{PP} voltage not valid at time of WRITE
1	0	0	Erase error
1	0	1	Erase error, V_{PP} voltage not valid at time of ERASE CONFIRM
1	1	0	Command sequencing error
1	1	1	Command sequencing error, programming voltage error

NOTE: 1. SR3 - SR5 must be cleared using CLEAR STATUS REGISTER.

WRITE/ERASE CYCLE ENDURANCE

The MT28F400 is designed and fabricated to meet advanced firmware storage requirements. To ensure this level of reliability, V_{PP} must be at 12V ±5% during write or erase cycles. Operation outside these limits may reduce the number of erase cycles that can be performed on the device. For further information on write and erase cycle endurance, refer to the Micron *Flash Reliability Monitor*.

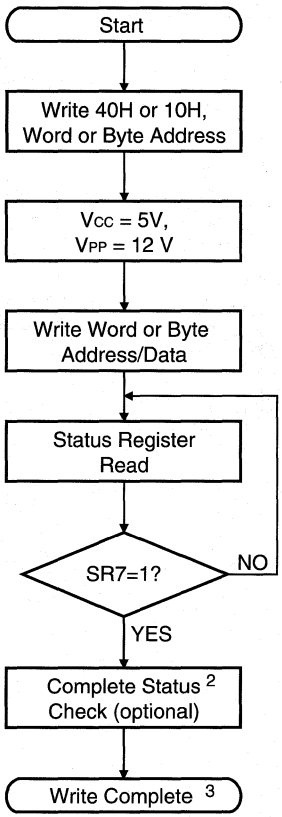
POWER USAGE

The MT28F400 offers several power saving features that may be utilized in the array read mode to conserve power. With $\overline{CE}$ LOW, the device will enter idle current mode when not being accessed. In this mode, the maximum I_{CC} current is 3mA. When $\overline{CE}$ is HIGH, the device will enter standby mode. In this mode, maximum I_{CC} current is 100µA. If $\overline{CE}$ is brought HIGH during an erase or write, the ISM will continue to operate, and the device will consume the respective active power until the write or erase is completed.

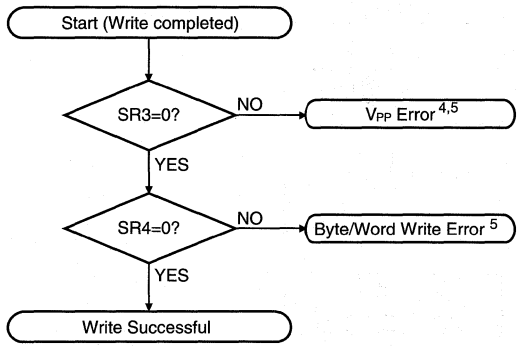
POWERUP

During a powerup, it is not necessary to sequence V_{CC} and V_{PP}. The likelihood of unwanted write or erase operations is minimized, since two consecutive cycles are required to execute either operation. However, $\overline{CE}$ or $\overline{WE}$ may be held HIGH, or $\overline{RST}$ can be held LOW during powerup for additional protection against unwanted write or erase operations. After a powerup or RESET, the status register is reset, and the device will enter the array read mode.

SELF-TIMED WRITE SEQUENCE (Word or Byte Write)[1]

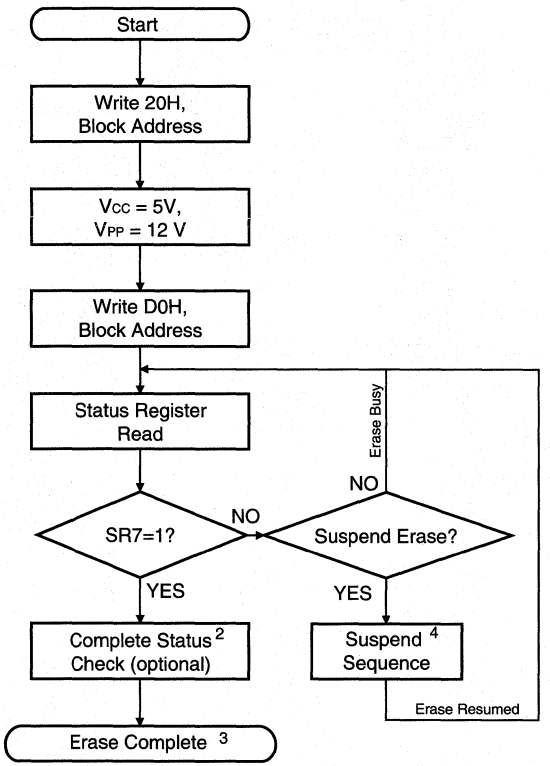


COMPLETE WRITE STATUS-CHECK SEQUENCE

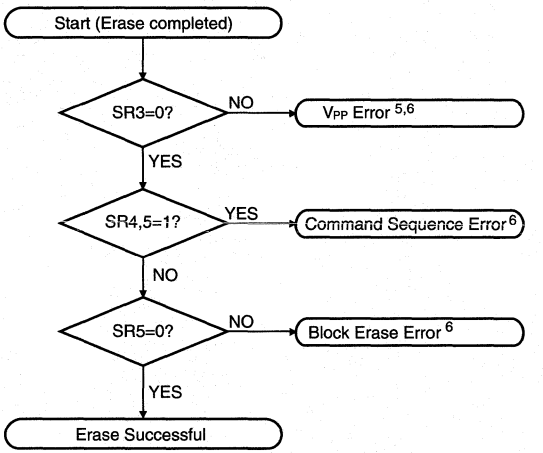


NOTE:
1. Sequence may be repeated for multiple byte or word writes.
2. Complete status check is not required. However, if SR3 = 1, further writes are inhibited until the status register is cleared.
3. Device will be in status register read mode. To return to the array read mode, the FFH command must be issued.
4. If SR3 is set during a write or block erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
5. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

SELF-TIMED BLOCK ERASE SEQUENCE[1]

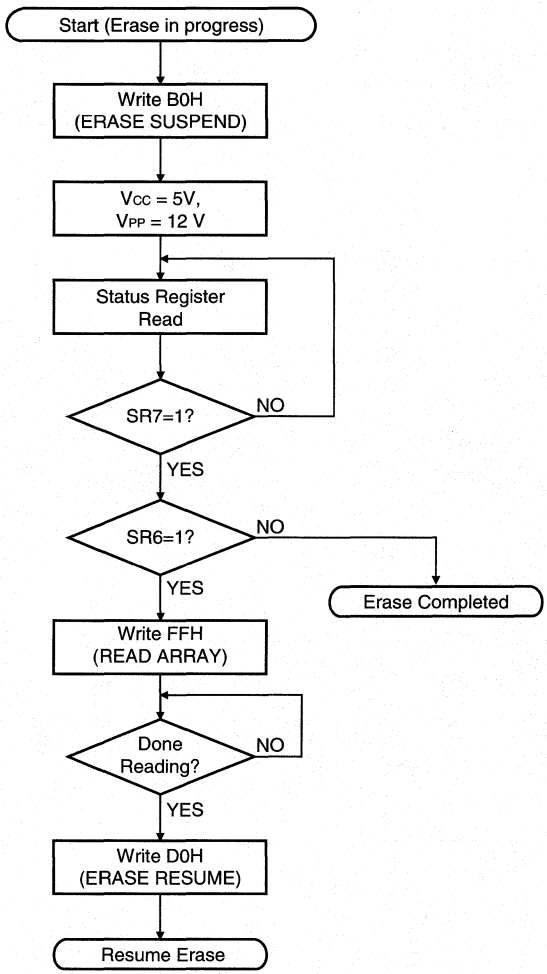


COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



NOTE:
1. Sequence may be repeated to erase multiple blocks.
2. Complete status check is not required. However, if SR3 = 1, further erases are inhibited until the status register is cleared.
3. To return to the array read mode, the FFH command must be issued.
4. Refer to the ERASE SUSPEND flowchart for more information.
5. If SR3 is set during a write or block erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
6. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

ERASE SUSPEND/RESUME SEQUENCE



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -0.5V to +7V
Input Voltage Relative to Vss ..... -0.5V to +7V**
V_{PP} Voltage Relative to Vss ..... -0.5V to +12.6V†
$\overline{RST}$/Pin A9 Voltage Relative to Vss .... -0.5V to +13.5V**,†
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Input and I/O pins may transition to -2.0V for < 20ns and Vcc +2.0V for < 20ns.
†Voltage may pulse to 14.0V ≤ 20ns.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	1
Device Identification Voltage, A9	V_{ID}	11.4	13.0	V	1

DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS Output High Voltage (I_{OH} = - 2.5 mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OL} = 5.8 mA)	V_{OL}		0.45	V	
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ Vcc); all other pins not under test = 0V	I_L	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.5V ≤ A9 ≤ 13.0 = V_{ID})	I_{ID}		500	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled; 0V ≤ V_{OUT} ≤ Vcc)	I_{OZ}	-10	10	µA	

CAPACITANCE

(T_A = 25°C; Vcc = 5V ±10%; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_I	8	pF	
Output Capacitance	C_O	12	pF	

NOTE: 1. All voltages referenced to Vss.

READ AND STANDBY CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
READ CURRENT: WORD-WIDE, TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}); $\overline{RST}$ = V_{IH}	I_{CC1}	60	mA	2, 3
READ CURRENT: WORD-WIDE, CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 10 MHz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V); $\overline{RST}$ = V_{IH}	I_{CC2}	55	mA	2, 3
READ CURRENT: BYTE-WIDE, TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}); $\overline{RST}$ = V_{IH}	I_{CC3}	60	mA	2, 3
READ CURRENT: BYTE-WIDE, CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 10 MHz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V); $\overline{RST}$ = V_{IH}	I_{CC4}	55	mA	2, 3
READ CURRENT: V_{PP} SUPPLY (V_{PP} > V_{CC})	I_{PP1}	200	µA	
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RST}$ = V_{IH}, or $\overline{RST}$ = V_{IL}; other inputs = V_{IL} or V_{IH})	I_{CC5}	1.5	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RST}$ = V_{CC} - 0.2V; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V)	I_{CC6}	100	µA	
STANDBY CURRENT: V_{PP} SUPPLY (V_{PP} ≤ V_{CC})	I_{PP2}	±15	µA	
IDLE CURRENT: TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 0 Hz; Other inputs = V_{IL} or V_{IH}; $\overline{RST}$ = V_{IH}; array read mode)	I_{CC7}	3	mA	
IDLE CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 0 Hz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V; $\overline{RST}$ = V_{IH}; READ ARRAY)	I_{CC8}	3	mA	

WRITE/ERASE CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
WORD-WRITE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC9}	65	mA	
WORD-WRITE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP3}	40	mA	
BYTE-WRITE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC10}	65	mA	
BYTE-WRITE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP4}	30	mA	
ERASE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC11}	30	mA	
ERASE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP5}	30	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%; erase suspended)	I_{CC12}	10	mA	4
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%; erase suspended)	I_{PP6}	200	µA	

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	70		80		100		ns	6
Access time from $\overline{CE}$	^tACE		70		80		100	ns	5,6
Access time from $\overline{OE}$	^tAOE		35		40		50	ns	5,6
Access time from address	^tAA		70		80		100	ns	6
$\overline{RST}$ HIGH to output valid delay	^tRWH		300		300		300	ns	6
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		25		30		40	ns	6
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		0		0		ns	6

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; Vcc = 5V ±5%)

AC CHARACTERISTICS		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	60		ns	7
Access time from $\overline{CE}$	^tACE		60	ns	5,7
Access time from $\overline{OE}$	^tAOE		30	ns	5,7
Access time from address	^tAA		60	ns	7
$\overline{RST}$ HIGH to output valid delay	^tRWH		300	ns	7
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		20	ns	7
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		ns	7

AC TEST CONDITION–1

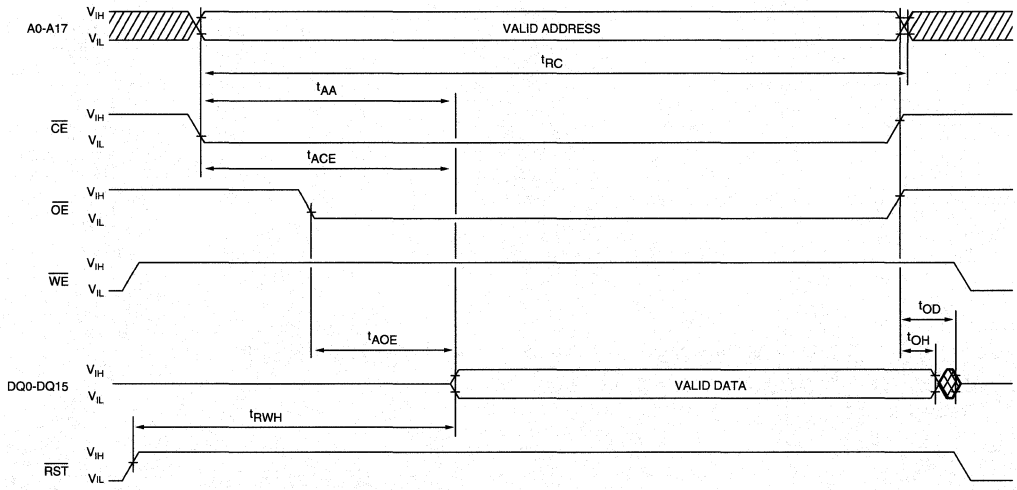
Input pulse levels	0.4 to 2.4V
Input rise and fall times	<10ns
Input timing reference level	0.8 V and 2.0 V
Output timing reference level	0.8 V and 2.0 V
Output load	1 TTL gate and C_L = 100 pF

AC TEST CONDITION–2

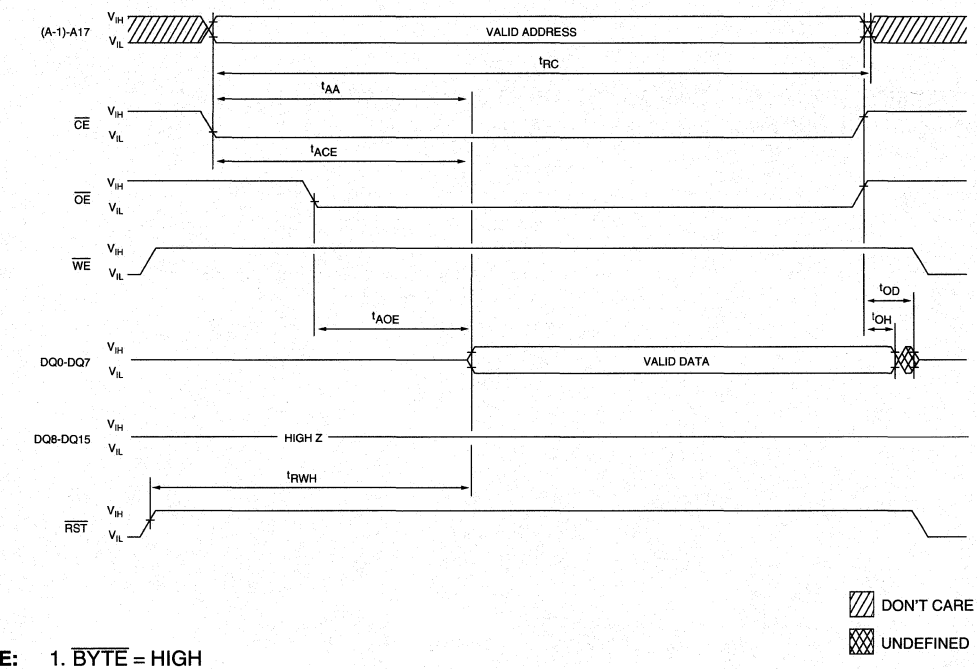
Input pulse levels	0.0 to 3.0V
Input rise and fall times	<10ns
Input timing reference level	1.5 V
Output timing reference level	1.5 V
Output load	1 TTL gate and C_L = 30 pF

NOTE:
1. All voltages referenced to Vss.
2. Icc is dependent on cycle rates.
3. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Parameter is specified when device is not accessed. Actual current draw will be Icc12 plus read current if a read is executed while in erase suspend mode.
5. $\overline{OE}$ may be delayed by ^tACE minus ^tAOE after $\overline{CE}$ falls before ^tACE is affected.
6. Measurements tested under AC Test Conditions-1.
7. Measurements tested under AC pTest Conditions-2.

WORD-WIDE READ CYCLE [1]



BYTE-WIDE READ CYCLE [2]



NOTE: 1. $\overline{BYTE}$ = HIGH
2. $\overline{BYTE}$ = LOW

RECOMMENDED DC WRITE/ERASE CONDITIONS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
V_{PP} voltage during normal operation	V_{PPL}	0.0	6.5	V	
V_{PP} voltage during erase/write operation	V_{PPH}	11.4	12.6	V	
Boot block unlock voltage	V_{HH}	11.4	13.0	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT: $\overline{RST}$ INPUT ($11.4 \le \overline{RST} \le 13.0V = V_{HH}$)	I_{HH}		500	µA	

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	70		80		100		ns	1
$\overline{WE}$ HIGH pulse width	^tWPH	20		20		30		ns	1
$\overline{CE}$ HIGH pulse width	^tCPH	20		20		30		ns	1

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±5%)

AC CHARACTERISTICS		-6			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	60		ns	2
$\overline{WE}$ HIGH pulse width	^tWPH	10		ns	2
$\overline{CE}$ HIGH pulse width	^tCPH	10		ns	2

NOTE: 1. Measurements tested under AC Test Conditions-1.
2. Measurements tested under AC Test Conditions-2.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{WE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10% or ±5%)

AC CHARACTERISTICS		-6, -8, -10			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{WE}$ HIGH	^tAS	50		ns	
Address hold time from $\overline{WE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{WE}$ HIGH	^tDS	50		ns	
Data hold time from $\overline{WE}$ HIGH	^tDH	0		ns	
$\overline{CE}$ setup time to $\overline{WE}$ LOW	^tCS	0		ns	
$\overline{CE}$ hold time from $\overline{WE}$ HIGH	^tCH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	100		ns	1
$\overline{WE}$ pulse width	^tWP	50		ns	
$\overline{RST}$ HIGH to $\overline{WE}$ LOW delay	^tRS	220		ns	
$\overline{RST}$ V_{HH} setup time to $\overline{WE}$ HIGH	^tRHS	100		ns	2
Write duration (word or byte write)	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		100	ns	3

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{CE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ±10% or ±5%)

AC CHARACTERISTICS		-6, -8, -10			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{CE}$ HIGH	^tAS	50		ns	
Address hold time from $\overline{CE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{CE}$ HIGH	^tDS	50		ns	
Data hold time from $\overline{CE}$ HIGH	^tDH	0		ns	
$\overline{WE}$ setup time to $\overline{CE}$ LOW	^tWS	0		ns	
$\overline{WE}$ hold time from $\overline{CE}$ HIGH	^tWH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	100		ns	1
$\overline{CE}$ pulse width	^tCP	50		ns	
$\overline{RST}$ HIGH to $\overline{CE}$ LOW delay	^tRS	220		ns	
$\overline{RST}$ V_{HH} setup time to $\overline{CE}$ HIGH	^tRHS	100		ns	2
Write duration (word or byte write)	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1, 2
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		100	ns	2

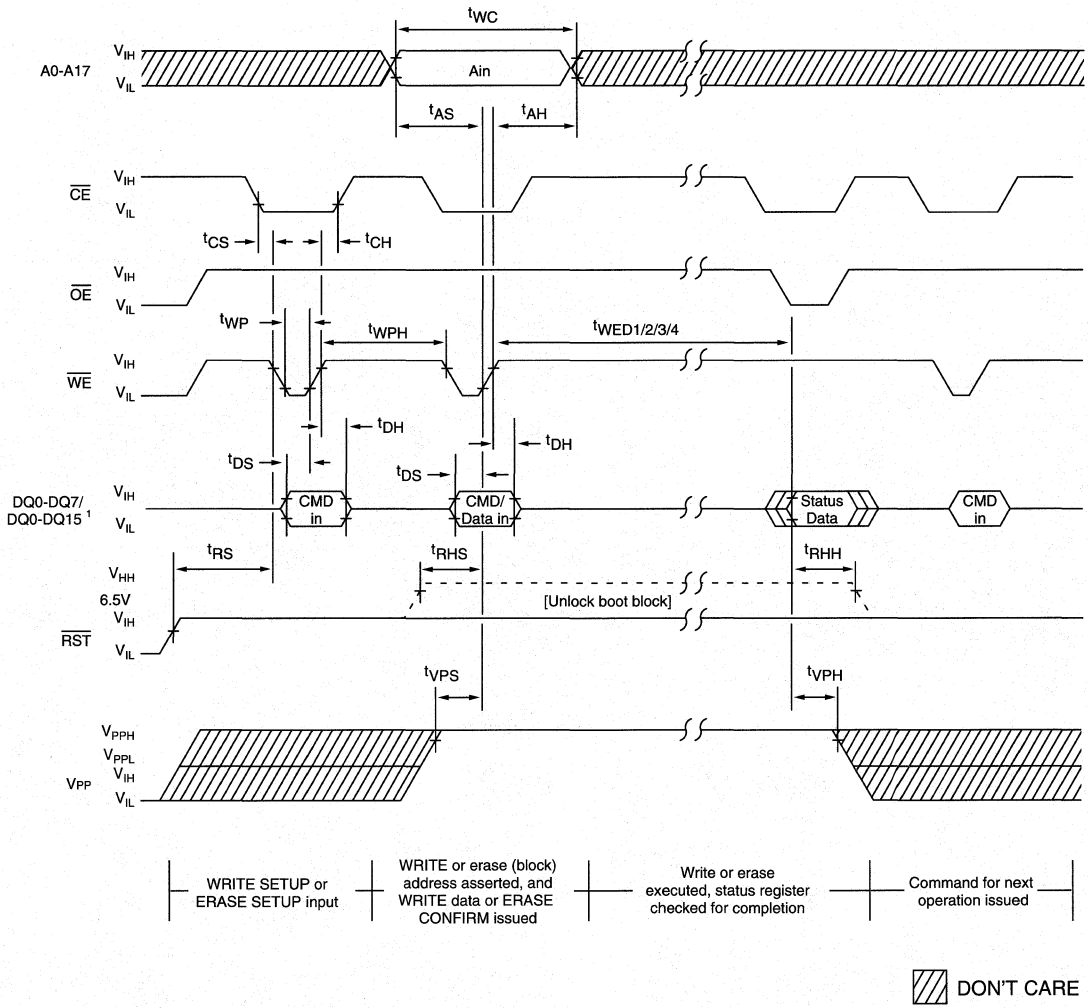
NOTE: 1. Write/erase times are measured to valid status register data (SR7=1).
2. $\overline{RST}$ should be held at V_{HH} until boot-block write or erase is complete.
3. ^tREL is required to relock boot block after write or erase to boot block.

WORD/BYTE WRITE AND ERASE DURATION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Boot/parameter block erase time		1.0	7.0	s	1
Main block erase time		2.5	14.0	s	1
Main block byte write time		1.0	4.0	s	1, 2
Main block word write time		0.5	2.0	s	1, 2

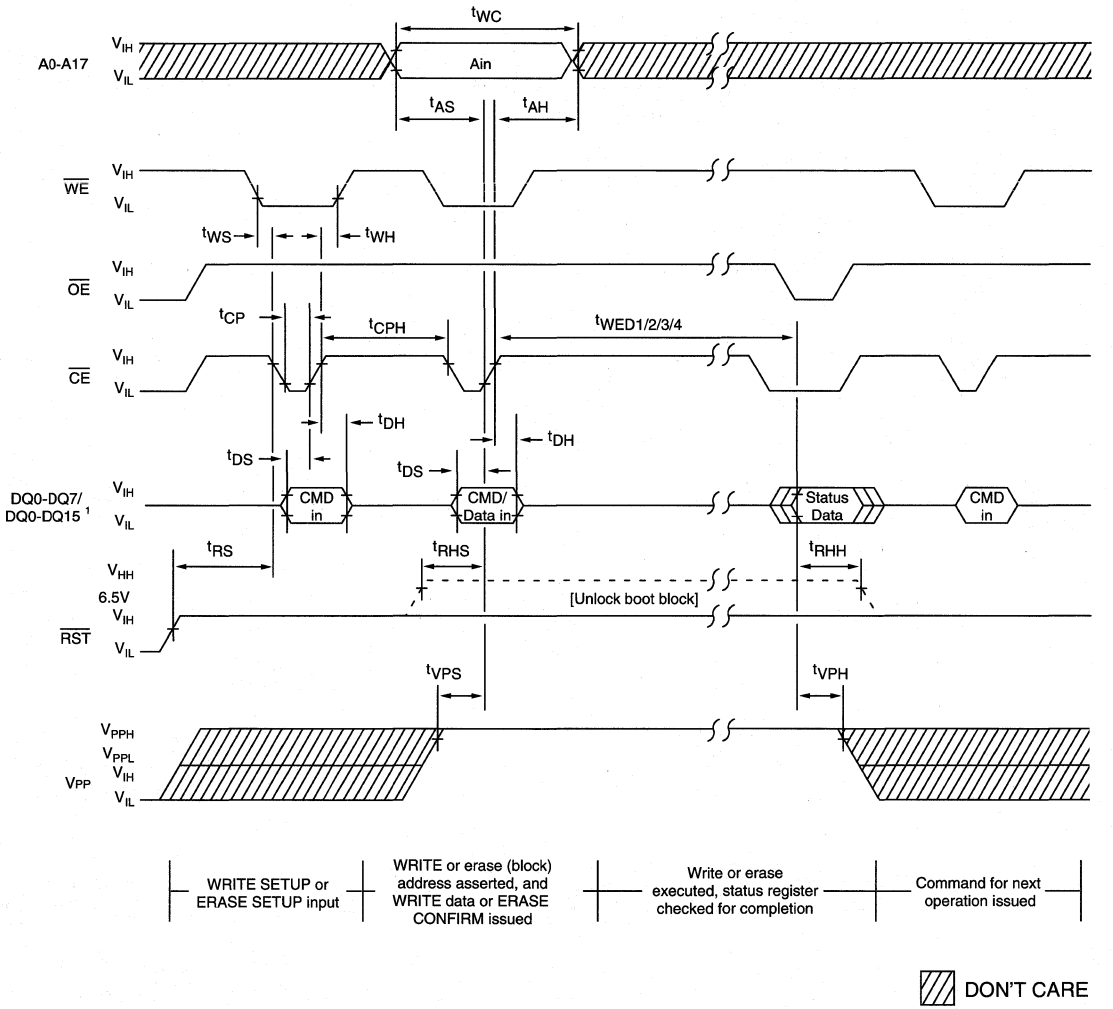
NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.

ERASE/WRITE CYCLE
$\overline{WE}$-CONTROLLED WRITE/ERASE



NOTE: 1. If $\overline{BYTE}$ is LOW, DATA and COMMAND are 8-bit. If $\overline{BYTE}$ is HIGH, DATA is 16-bit and COMMAND is 8-bit.

ERASE/WRITE CYCLE
$\overline{CE}$-CONTROLLED WRITE/ERASE



NOTE: 1. If $\overline{BYTE}$ is LOW, DATA and COMMAND are 8-bit. If $\overline{BYTE}$ is HIGH, DATA is 16-bit and COMMAND is 8-bit.

NEW ■ 5/12 VOLT FLASH MEMORY

FLASH MEMORY 1 MEG x 8

5V/12V, SYMMETRIC BLOCK

FEATURES

- Sixteen 64KB erase blocks
- Low power: 100µA standby; 50mA active, MAX
- 5V±10% read; 12V±5% write/erase
- Address access times: 80ns, 90ns, 100ns
- Industry-standard pinouts
- READY/$\overline{\text{BUSY}}$ (R/$\overline{\text{B}}$) output and status register write/erase polling
- High-performance CMOS floating-gate process
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm
- TSOP Packaging option

OPTIONS MARKING

- Timing
  - 80ns access - 8
  - 90ns access - 9
  - 100ns access -10
- Packages
  - Plastic SOP (600 mil) SG
  - Plastic TSOP Type 1 (10 x 20mm) VG
- Part Number Example: MT28F008VG-8

GENERAL DESCRIPTION

The MT28F008 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 8,388,608 bits organized as 1,048,576 words by 8 bits. It is fabricated with Micron's advanced CMOS floating-gate process.

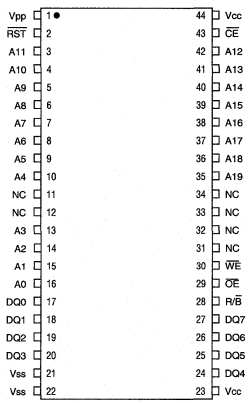
The MT28F008 is organized into 16 separately erasable 64KB blocks. Data is read and written on a random access basis, and erased in blocks. To write or erase the device, a super-voltage must be applied to the V_{PP} pin. This provides the necessary voltage and current required to write or erase the cells, and provides additional security against accidental erasure or overwrite. The internal state machine executes all write and erase algorithms to the memory array.

In addition to status register polling, the MT28F008 provides a READY/$\overline{\text{BUSY}}$ (R/$\overline{\text{B}}$) output to indicate write and erase completion. Operations are executed by issuing commands from an industry standard command set.

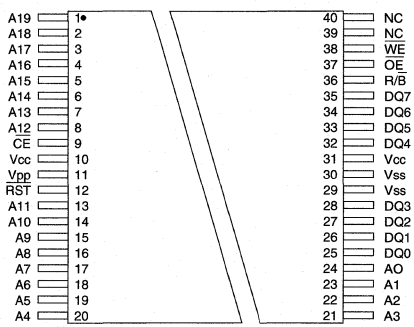
To read the array, the byte address is issued with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ LOW and $\overline{\text{WE}}$ HIGH. Valid data is output until the next address is issued or until $\overline{\text{CE}}$ or $\overline{\text{OE}}$ go HIGH.

PIN ASSIGNMENT (Top View)

44-Pin SOP
(FA-1)



40-Pin TSOP Type I
(FB-1)



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QUANTUM DEVICES, INC.

5/12 VOLT FLASH MEMORY 1

3.3/12 VOLT FLASH MEMORY 2

PACKAGE INFORMATION 3

SALES INFORMATION 4

3.3/12 VOLT FLASH MEMORY PRODUCT SELECTION GUIDE

Memory Configuration	Features/ Options	Part Number	Access Time (ns)	Typical Power Dissipation		Package/Number of Pins		Page
				Standby	Active	SOP	TSOP	
256K x 8	BB, AUTO	MT28LF002	90, 100, 120	120µA	30mA	-	40	2-1
128K x 16/ 256K x 8	BB, AUTO	MT28LF200	90, 100, 120	120µA	30mA	44	56	2-3
512K x 8	BB, AUTO	MT28LF004	90, 100, 120	120µA	30mA	-	40	2-5
256K x 16/ 512K x 8	BB, AUTO	MT28LF400	90, 100, 120	120µA	30mA	44	56	2-7
1 Meg x 8	SB, AUTO, DPD	MT28LF008	100, 150	120µA	30mA	44	40	2-31

BB = Boot Block, AUTO = Automated W/E Algorithm, SB = Symmetric Block, DPD = Deep Power Down

NEW ■ 3.3/12 VOLT FLASH MEMORY

FLASH MEMORY 256K x 8

3.3V/12V, BOOT BLOCK

FEATURES

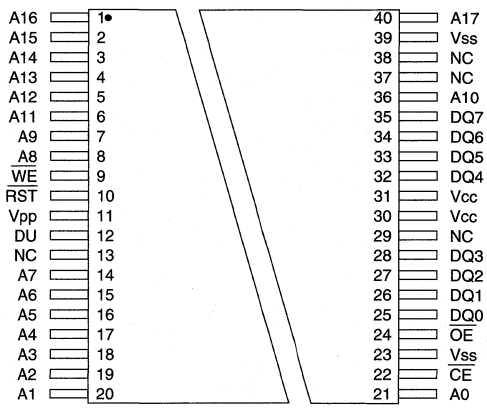
- Five erase blocks:
  - 16KB boot block (protected)
  - Two 8KB parameter blocks
  - One 96KB memory block
  - One 128KB memory block
- Low power: 120µA standby; 30mA active, MAX
- 3.3V±0.3V read; 12V±5% write/erase
- Address access time: 90ns, 100ns, 120ns
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm
- TSOP packaging

OPTIONS MARKING

- Timing
  - 90ns access - 9
  - 100ns access -10
  - 120ns access -12
- Boot-Block Starting Address
  - Top (3FFFFH) T
  - Bottom (00000H) B
- Packages
  - Plastic TSOP Type 1 (10 x 20mm) VG
- Part Number Example: MT28LF002VG-9T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(FB-1)



GENERAL DESCRIPTION

The MT28LF002 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 2,097,152 bits organized as 262,144 words by 8 bits. It is fabricated with Micron's advanced 3.3V CMOS floating-gate process.

The MT28LF002 is organized into five separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28LF002 features a hardware-protected boot-block. Writing or erasing the boot block requires a super-voltage on the $\overline{RST}$ pin in addition to executing the normal write or erase sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density, and are written-to and erased with no additional super-voltage required.

To read the array, the byte address is issued with $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH. Valid data is output until the next address is issued or until $\overline{CE}$ or $\overline{OE}$ go HIGH.

NEW

FLASH MEMORY

128K x 16, 256K x 8

3.3V/12V, BOOT BLOCK

3.3/12 VOLT FLASH MEMORY

FEATURES

- Five erase blocks:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - One 96KB/48K-word memory block
  - One 128KB/64K-word memory block

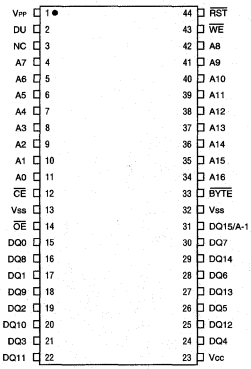
  Low power: 120µA standby; 30mA active, MAX
- 3.3V±0.3V read; 12V±5% write/erase
- Address access time: 90ns, 100ns, 120ns
- Selectable organizations: 131,072 x 16 or 262,144 x 8
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm
- Byte- or word-wide write
- TSOP packaging option

OPTIONS / MARKING

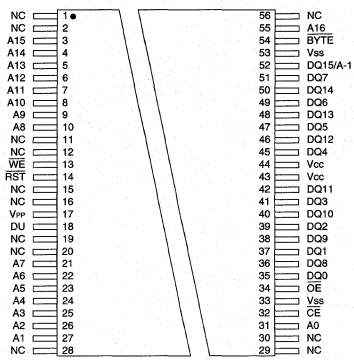
- Timing
  - 90ns access - 9
  - 100ns access -10
  - 120ns access -12
- Boot-Block Starting Address
  - Top (1FFFFH) T
  - Bottom (00000H) B
- Packages
  - Plastic SOP (600 mil) SG
  - Plastic TSOP Type 1 (14 x 20mm) VG
- Part Number Example: MT28LF200SG-9T

PIN ASSIGNMENT (Top View)

44-Pin SOP (FA-1)



56-Pin TSOP Type I (FB-2)



GENERAL DESCRIPTION

The MT28LF200 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 2,097,152 bits organized as 131,072 words by 16 bits or 262,144 words by 8 bits. It is fabricated with Micron's advanced 3.3V CMOS floating-gate process.

The MT28LF200 is organized into five separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28LF200 features a hardware-protected boot-block. Writing or erasing the boot block requires a super-voltage on the $\overline{RST}$ pin in addition to executing the normal write or erase sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density, and are written-to and erased with no additional super-voltage required.

The byte or word address is issued to read the memory array with $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH. Valid data is output until the next address is issued. The $\overline{BYTE}$ pin is used to switch the data path between 8 bits wide and 16 bits wide. When $\overline{BYTE}$ is LOW, the dual-use pin DQ15/A-1 becomes the lowest order address bit (A-1). When $\overline{BYTE}$ is HIGH, the DQ15/A-1 pin becomes the most significant data bit (DQ15).

NEW

3.3/12 VOLT FLASH MEMORY

FLASH MEMORY 512K x 8

3.3V/12V, BOOT BLOCK

FEATURES

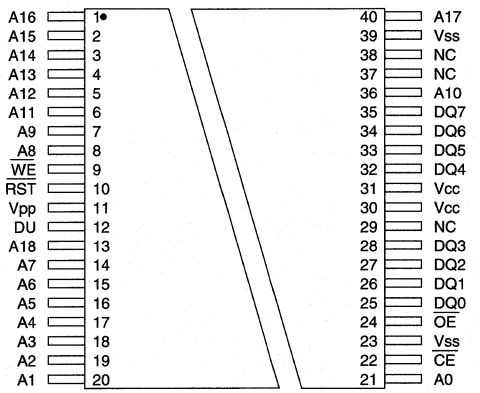
- Seven erase blocks:
  - 16KB boot block (protected)
  - Two 8KB parameter blocks
  - One 96KB memory blocks
- Low power: 120µA standby; 30mA active, MAX
- 3.3V±0.3V read; 12V±5% write/erase
- Address access time: 90ns, 100ns, 120ns
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm
- TSOP packaging

OPTIONS MARKING

- Timing
  - 90ns access - 9
  - 100ns access -10
  - 120ns access -12
- Boot-Block Starting Address
  - Top (7FFFFH) T
  - Bottom (00000H) B
- Packages
  - Plastic TSOP Type 1 (10 x 20mm) VG
- Part Number Example: MT28LF004VG-9T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I
(FB-1)



GENERAL DESCRIPTION

The MT28LF004 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 4,194,304 bits organized as 524,288 words by 8 bits. It is fabricated with Micron's advanced 3.3V CMOS floating-gate process.

The MT28LF004 is organized into seven separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28LF004 features a hardware-protected boot-block. Writing or erasing the boot block requires a super-voltage on the $\overline{RST}$ pin in addition to executing the normal write or erase sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density, and are written-to and erased with no additional super-voltage required.

To read the array, the byte address is issued with $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH. Valid data is output until the next address is issued or until $\overline{CE}$ or $\overline{OE}$ go HIGH.

NEW

3.3/12 VOLT FLASH MEMORY

FLASH MEMORY

256K x 16, 512K x 8

3.3V/12V, BOOT BLOCK

FEATURES

- Seven erase blocks:
  - 16KB/8K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Four general memory blocks
- Low power: 120µA standby; 30mA active, MAX
- 3.3V±0.3V read; 12V±5% write/erase
- Address access time: 90ns, 100ns, 120ns
- Selectable organizations: 262,144 x 16 or 524,288 x 8
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm
- Byte- or word-wide write
- TSOP packaging option

OPTIONS / MARKING

- Timing
  - 90ns access - 9
  - 100ns access -10
  - 120ns access -12
- Boot-Block Starting Address
  - Top (3FFFFH) T
  - Bottom (00000H) B
- Packages
  - Plastic SOP (600 mil) SG
  - Plastic TSOP Type 1 (14 x 20mm) VG
- Part Number Example: MT28LF400SG-9T

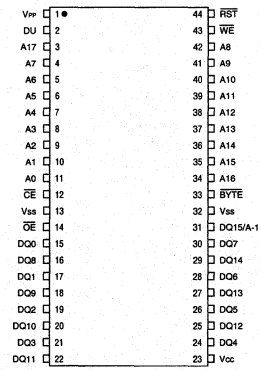
GENERAL DESCRIPTION

The MT28LF400 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 4,194,304 bits organized as 262,144 words by 16 bits or 524,288 words by 8 bits. It is fabricated with Micron's advanced CMOS floating-gate process.

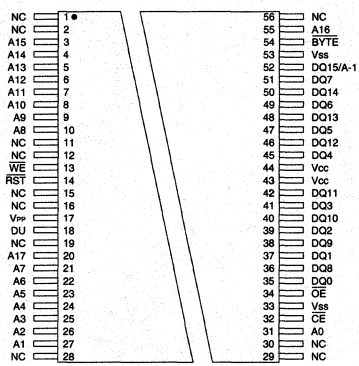
The MT28LF400 is organized into seven separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28LF400 features a hardware-protected boot-block. Writing or erasing the boot block requires a super-voltage on the $\overline{RST}$ pin in addition to executing the normal write or erase sequences. This block may be used to store code implemented in low-level system recovery. The remaining blocks vary in density, and are written-to and erased with no additional super-voltage required.

PIN ASSIGNMENT (Top View)

44-Pin SOP (FA-1)



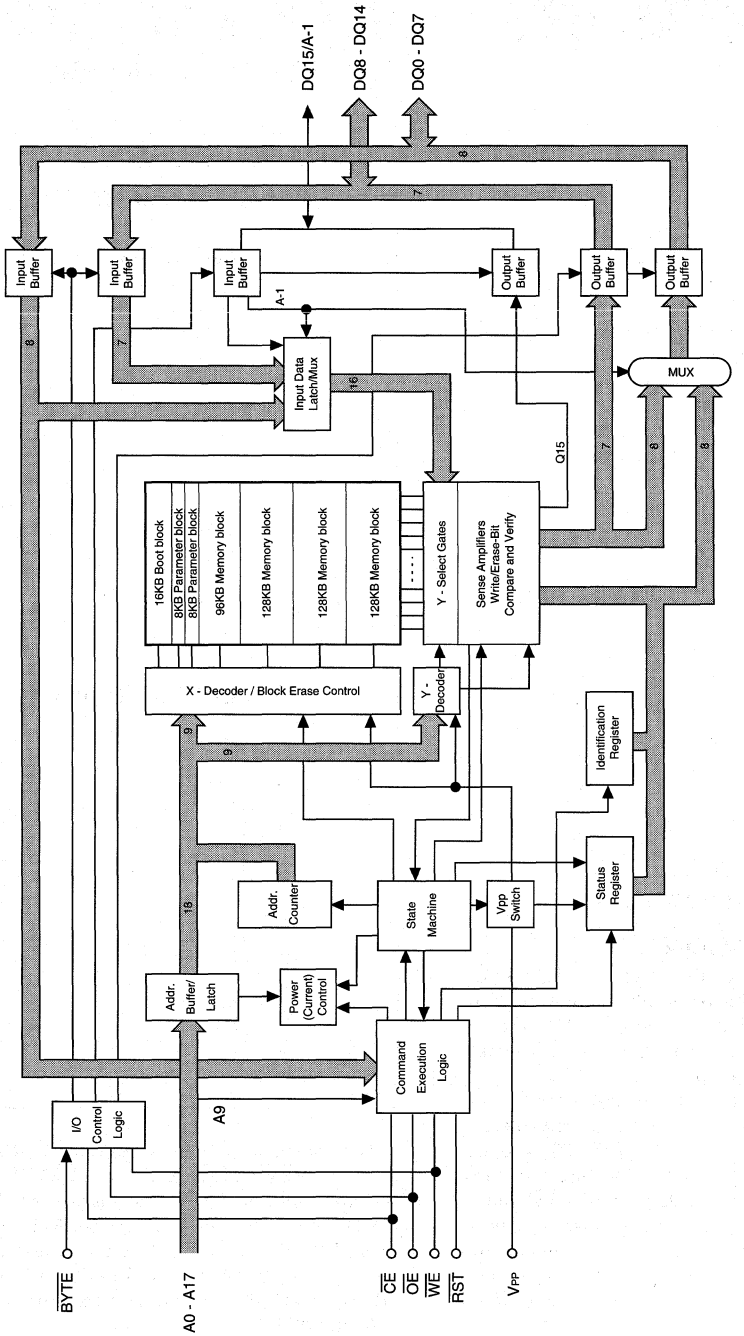
56-Pin TSOP Type I (FB-2)



The byte or word address is issued to read the memory array with $\overline{CE}$ and $\overline{OE}$ LOW and $\overline{WE}$ HIGH. Valid data is output until the next address is issued. The $\overline{BYTE}$ pin is used to switch the data path between 8 bits wide and 16 bits wide. When $\overline{BYTE}$ is LOW, the dual-use pin DQ15/A-1 becomes the lowest order address bit (A-1). When $\overline{BYTE}$ is HIGH, the DQ15/A-1 pin becomes the most significant data bit (DQ15).

NEW 3.3/12 VOLT FLASH MEMORY

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
43	13	$\overline{WE}$	Input	Write Enable: Determines if a given cycle is a write cycle. If $\overline{WE}$ = LOW when $V_{PP} < V_{PPH}$, the cycle is a write to the Command Execution Logic (CEL). If $\overline{WE}$ = LOW when $V_{PP} = V_{PPH}$, the cycle is a WRITE to one of the sectors or an ERASE CONFIRM.
12	32	$\overline{CE}$	Input	Chip Enable: Activates the device when LOW. When $\overline{CE}$ is HIGH, the device is disabled and goes into standby power mode.
44	14	$\overline{RST}$	Input	Reset: Clears the status register, sets the Internal State Machine (ISM) to the array read mode, and places the device in standby mode when LOW. All inputs, including $\overline{CE}$, are "don't care," and all outputs are High-Z. Also used to unlock boot block when brought to V_{HH} (boot-block unlock voltage; 12V). Must be held HIGH during all other modes of operation.
14	34	$\overline{OE}$	Input	Output Enable: Enables data output buffers.
33	54	$\overline{BYTE}$	Input	Byte Enable: If $\overline{BYTE}$=HIGH the upper byte is active through DQ8-DQ15. If $\overline{BYTE}$=LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34, 3	31, 27, 26, 25, 24, 23, 22, 21, 10, 9, 8, 7, 6, 5, 4, 3, 55, 20	A0-A17	Input	Address Inputs: Selects a unique, 16-bit word out of the 262,144 available. The DQ15/A-1 input becomes the lowest order address when $\overline{BYTE}$=LOW to allow for selection of an 8-bit byte from 524,288 available.
31	52	DQ15/A-1	Input/ Output	Data I/O: MSB of data when $\overline{BYTE}$ = HIGH. Address Input: LSB of address input when $\overline{BYTE}$ = LOW during read or write operation. Not used during erase or read device ID.
15, 17, 19, 21, 24, 26, 28, 30	35, 37, 39, 41, 45, 47, 49, 51	DQ0-DQ7	Input/ Output	Data I/O: Data output pins during any read operation, or data input pins during a WRITE. Used to input commands to the CEL for a command input.
16, 18, 20, 22, 25, 27, 29	36, 38, 40, 42, 46, 48, 50	DQ8-DQ14	Input/ Output	Data I/O: Data output pins during any read operation or data input pins during a WRITE when $\overline{BYTE}$ = HIGH. High-Z when $\overline{BYTE}$ is LOW.
	1, 2, 11, 12, 15, 16, 19, 28, 29, 30, 56	NC	-	No Connect: These pins may be driven or left unconnected.
2	18	DU	-	Don't Use: This pin must be left unconnected in the system.
1	17	V_{PP}	Supply	Write/Erase Supply Voltage: During a WRITE or ERASE CONFIRM, $V_{PP} = V_{PPH}$ (12V). V_{PP} = "don't care" during all other operations.
23	43, 44	Vcc	Supply	Power Supply: +3.3V ±0.3V
13, 32	33, 53	Vss	Supply	Ground

TRUTH TABLE [1]

FUNCTION	$\overline{RST}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READING											
16-bit Read	H	L	L	H	H	X	X	X	Data-Out	Data-Out	Data-Out
8-bit Read	H	L	L	H	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE [2]											
ERASE SETUP	H	L	H	L	X	X	X	X	20H	X	X
ERASE CONFIRM [3]	H	L	H	L	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H	X	X
16-bit WRITE [4]	H	L	H	L	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
8-bit WRITE [4]	H	L	H	L	L	X	X	V_{PPH}	Data-In	High-Z	A-1
READ ARRAY	H	L	H	L	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK) [2, 5]											
ERASE SETUP	H	L	H	L	X	X	X	X	20H	X	X
ERASE CONFIRM [3]	V_{HH}	L	H	L	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	10H/40H	X	X
16-bit WRITE [4]	V_{HH}	L	H	L	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
8-bit WRITE [4]	V_{HH}	L	H	L	L	X	X	V_{PPH}	Data-In	High-Z	A-1
READ ARRAY	H	L	H	L	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION [6, 7]											
Manufacturer (16-bit) [8]	H	L	L	H	H	L	V_{ID}	X	2CH	00H	-
Manufacturer (8-bit)	H	L	L	H	L	L	V_{ID}	X	2CH	High-Z	X
Device (16-bit, top boot) [8]	H	L	L	H	H	H	V_{ID}	X	30H	44H	-
Device (8-bit, top boot)	H	L	L	H	L	H	V_{ID}	X	30H	High-Z	X
Device (16-bit, bottom boot) [8]	H	L	L	H	H	H	V_{ID}	X	31H	44H	-
Device (8-bit, bottom boot)	H	L	L	H	L	H	V_{ID}	X	31H	High-Z	X

NOTE:
1. L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}.
2. V_{PPH} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. V_{HH} = 12V.
6. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
7. A1-A8, A10-A17 = V_{IL}.
8. Value reflects DQ8-DQ15.

FUNCTIONAL DESCRIPTION

The MT28LF400 Flash memory incorporates a number of features to make it ideally suited for system firmware.

The memory array is segmented into individual erase blocks. Each block may be erased without affecting data stored in other blocks. These memory blocks are read, written and erased by issuing commands to the Command Execution Logic (CEL). The CEL controls the operation of the Internal State Machine (ISM) that completely controls all write, block erase, and verify operations. This state machine protects each memory location from overerasure and optimizes each memory location for maximum data retention. In addition, the ISM greatly simplifies the control necessary for writing the device in-system or in an external programmer.

The Functional Description provides detailed information on the operation of the MT28LF400, and is organized into these sections:

- Overview
- Memory Architecture
- Output (Read) Operations
- Input Operations
- Command Set
- ISM Status Register
- Command Execution
- Error Handling
- Write/Erase Cycle Endurance
- Power Usage
- Powerup

OVERVIEW

SEVEN INDEPENDENTLY ERASABLE MEMORY BLOCKS

The MT28LF400 is organized into seven independently erasable memory blocks that allow portions of the memory to be erased without affecting the rest of the memory data. A special boot block is hardware-protected against inadvertent erasure or writes by a super-voltage pin. The voltage on this pin is required in addition to the 12V on the V_{PP} pin. The remaining blocks require only the 12V V_{PP} to be present in order to be changed.

HARDWARE-PROTECTED BOOT-BLOCK

This block of the memory array can be erased or written only when the $\overline{RST}$ pin is taken to V_{HH}. Designing a system so that the processor or control logic is unable to apply 12V to this pin will ensure data integrity in this memory block. This provides additional security for the core firmware during in-system firmware updates, should an unintentional power fluctuation or system reset occur. The MT28LF400 is available in two versions; the MT28LF400T addresses the boot block starting from 3FFFFH, and the MT28LF400B addresses the boot block starting from 00000H.

CONFIGURABLE BUS SIZE

The MT28LF400T/B allows dynamic selection of an eight-bit (512K x 8) or 16-bit (256K x 16) data bus for reading and writing the memory. The $\overline{BYTE}$ pin is used to select the bus width. When in the x16 configuration, control data is read or written only on the lower eight bits (DQ0-DQ7).

Data written to the memory array utilize all active data pins for the selected configuration. When the x8 configuration is selected, data is written in byte form; when in the x16 configuration, data is written in the word form.

INTERNAL STATE MACHINE (ISM)

Block erase and byte/word write timing are simplified by using an ISM to control all erase and write algorithms in the memory array. The ISM ensures protection against overerasure and optimizes write margin to each cell.

During write operations the ISM automatically increments and monitors write attempts, verifies write margin on each memory cell, and updates the ISM status register. When block erase is performed the ISM automatically overwrites the entire addressed block (eliminates overerasure), increments and monitors erase attempts, and sets bits in the ISM status register.

ISM STATUS REGISTER

The ISM status register allows an external processor to monitor the status of the ISM during write and erase operations. Two bits of the 8-bit status register are set and cleared entirely by the ISM. These bits indicate whether the ISM is busy with an erase or write task, and when an erase has been suspended. Additional error information is set in the other three bits: valid programming voltage, write error, and erase error.

COMMAND EXECUTION LOGIC (CEL)

The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the read path (i.e. memory array, ID register, or status register). Commands may be issued to the CEL while the ISM is active. However, there are restrictions on what commands are allowed in this condition. See the Command Execution section for more detail.

MEMORY ARCHITECTURE

The MT28LF400 memory array architecture is designed to allow sections to be erased without disturbing the rest of the array. The array is divided into seven addressable "blocks" that are of varying size and independently erasable. By erasing in blocks, rather than the entire array, the total device endurance is enhanced, as is system flexibility. Only the erase function is block oriented. All read and write operations are done on a random word- or byte-basis.

The boot block is protected from unintentional erase or write with a hardware protection circuit that requires a super-voltage be applied before erasure is commenced. The boot block is intended for the core firmware required for basic system functionality. The remaining six blocks do not require this super-voltage before being written or erased.

BOOT BLOCK

The hardware-protected boot-block provides extra security for the most sensitive portions of the firmware. This 16KB block may only be erased or written when the $\overline{RST}$ pin is at the specified boot block unlock voltage (V_{HH}) of 12V. When performing erase or write cycles to this block, $\overline{RST}$ must be held at the unlock voltage (V_{HH}) until the erase or write is completed. As for any erase or write operations, the V_{PP} pin must be at V_{PPH} when writing to the boot block.

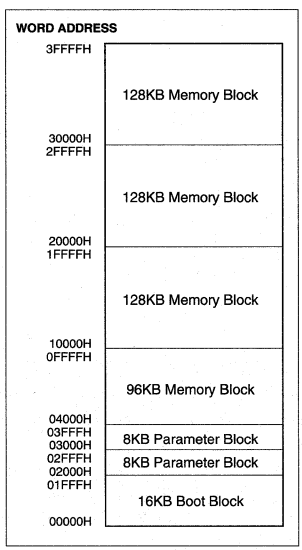
The MT28LF400 is available in two configurations, top or bottom boot-block. The MT28LF400T top boot-block version supports processors of the x86 variety. The MT28LF400B bottom boot-block version is intended for 680X0 and RISC applications. Figure 1 illustrates the memory address maps associated with these two versions.

PARAMETER BLOCKS

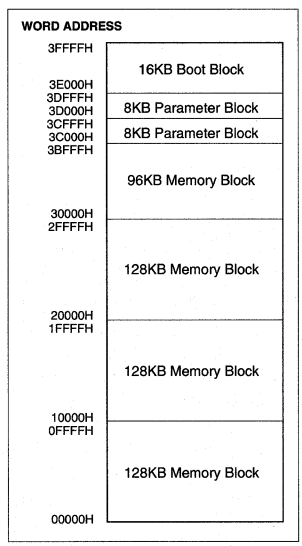
The two 8KB parameter blocks are used for storage of less sensitive and more frequently changing system parameters and also may include configuration or diagnostic coding. These blocks are enabled for erasure when the V_{PP} pin is at V_{PPH}. No super-voltage unlock is required.

GENERAL MEMORY BLOCKS

The four remaining blocks are general memory blocks and do not require a super-voltage on $\overline{RST}$ to be erased or written. These blocks are intended for code storage, or ROM-resident applications or operating systems that require in-system update capability.



Bottom Boot - MT28LF400xx-xxB



Top Boot - MT28LF400xx-xxT

Figure 1
MEMORY ADDRESS MAPS

OUTPUT (READ) OPERATIONS

The MT28LF400 features three different types of reads. Depending on the current mode of the device, a read operation will produce data from the memory array, status register, or device identification register. In each of these three cases, the $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$ inputs are controlled in a similar manner to perform a read. However, several differences exist, and are described in the following section. Moving between modes to perform a specific read will be covered in the Command Execution section.

MEMORY ARRAY

To read the memory array, $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. Valid data will be output on the DQ pins once these conditions have been met and a valid address is given. Valid data will remain on the DQ pins until the address changes, or $\overline{OE}$ or $\overline{CE}$ go HIGH, whichever occurs first. The DQ pins will continue to output new data after each address transition, as long as $\overline{OE}$ and $\overline{CE}$ remain LOW.

The MT28LF400 features dynamically sizable bus widths. When configured as 256K x 16 ($\overline{BYTE}$ is HIGH), data will be output on DQ0-DQ15. To configure the memory array as a 512K x 8, $\overline{BYTE}$ must be LOW. DQ8 - DQ14 are now "High-Z," and all data is output on DQ0-DQ7. The DQ15/A-1 pin now becomes the lowest order address input, so that 512,288 locations can be read.

After powerup or RESET, the device will automatically be in the array read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

STATUS REGISTER

Performing a read of the status register requires the same input sequencing as when reading the array, except that the address inputs are "don't care." The status register contents are always output on DQ0-DQ7, regardless of the condition of $\overline{BYTE}$. DQ8-DQ15 are LOW when $\overline{BYTE}$ is HIGH, and DQ8-DQ14 are High-Z when $\overline{BYTE}$ is LOW. Data from the status register is latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last. If the contents of the status register change during a read of the status register, either $\overline{OE}$ or $\overline{CE}$ may be toggled while the other is held LOW to update the output.

Following a write or erase, the device automatically enters the status register read mode. In addition, a read during a write or erase will produce the status register contents on DQ0-DQ7. When in the erase suspend mode, a read operation will produce the status register contents until another command is issued. While in certain other modes, READ STATUS REGISTER may be given to return to the status register read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

IDENTIFICATION REGISTER

A read of the two 8-bit device identification registers requires the same input sequencing as when reading the array. $\overline{WE}$ must be HIGH, and $\overline{OE}$ and $\overline{CE}$ must be LOW. However, ID register data is output only on DQ0-DQ7, regardless of the condition of $\overline{BYTE}$. A0 is used to decode between the two bytes of the device ID register; all other address inputs are "don't care." When A0 is LOW, the manufacturer ID is output, and when A0 is HIGH, the device ID is output. DQ8-DQ15 are "High-Z" when $\overline{BYTE}$ is LOW. When $\overline{BYTE}$ is HIGH, DQ8-DQ15 is 00H when the manufacturer ID is read, and 44H when the device is read.

To get to the read identification register mode, the READ IDENTIFICATION command may be issued while in certain other modes. In addition, the read identification register mode can be reached by applying a super-voltage (V_{ID}) to the A9 pin. Using this method, the ID register can be read while in any mode. Once A9 is returned to V_{IL} or V_{IH}, the device will return to the previous mode.

INPUT OPERATIONS

The DQ pins are used to either input data to the array or input a command to the CEL. A command input issues an 8-bit command to the CEL. Commands may be issued to control operation of the part. A WRITE is used to input data to the memory array. The following section describes both types of inputs. More information describing how to use the two types of inputs to write the device is provided in the Command Execution section.

COMMANDS

To perform a command input, $\overline{OE}$ must be HIGH, and $\overline{CE}$ and $\overline{WE}$ must be LOW. A0-A17 are not used for command inputs, except during an ERASE CONFIRM (described in a later section). The 8-bit command is input on DQ0-DQ7, while DQ8-DQ15 are "don't care." The command is latched on the rising edge of $\overline{CE}$ ($\overline{CE}$ controlled) or $\overline{WE}$ ($\overline{WE}$ controlled), whichever occurs first. The condition of $\overline{BYTE}$ has no effect on a command input.

MEMORY ARRAY

A write to the memory array sets the desired bits to logic 0's, but cannot change a given bit to a logic 1 from a logic 0. Setting any bits to a logic 1 requires that the entire block be erased. To perform a WRITE, $\overline{OE}$ must be HIGH, $\overline{CE}$ and $\overline{WE}$ must be LOW, and V_{PP} must be set to V_{PPH}. Writing to

the boot block also requires that the $\overline{RST}$ pin be at V_{HH}. A0-A17 provide the address to be written, while the data to be written to the array is input on the DQ pins. The data and addresses are latched on the rising edge of $\overline{CE}$ ($\overline{CE}$-controlled) or $\overline{WE}$ ($\overline{WE}$-controlled), whichever occurs first. A WRITE must be preceeded by a WRITE SETUP command. Detail on how to input data to the array will be covered in the Write Sequence section.

Dynamic bus sizing applies to writes as it does for reads. When $\overline{BYTE}$ is LOW (BYTE mode), data is input on DQ0-DQ7, DQ8-DQ14 are "High-Z," and DQ15 becomes the lowest order address input. To WRITE in x16 (WORD) mode, $\overline{BYTE}$ is HIGH, and data is input on DQ0-DQ15.

COMMAND SET

To simplify writing of the memory blocks, the MT28LF400 incorporates an ISM that controls all internal algorithms for the write and erase cycles. An 8-bit command set is used to control the device. Detail on how to sequence commands is provided in the Command Execution section. Table 1 lists the valid commands.

Table 1
COMMAND SET

COMMAND	HEX CODE	DESCRIPTION
RESERVED	00H	This command and all unlisted commands are invalid, and should not be called. These commands are reserved to allow for future feature enhancements.
READ ARRAY	FFH	Must be issued after any other command cycle before the array can be read. It is not necessary to issue this command after powerup or reset.
IDENTIFY DEVICE	90H	Allows the device and manufacturer ID to be read. A0 is used to decode between the manufacturer ID (A0=LOW) and device ID (A0=HIGH).
READ STATUS REGISTER	70H	Allows the status register to be read. Please refer to Table 2 for more information on the status register bits.
CLEAR STATUS REGISTER	50H	Clears status register bits 3 through 5, which cannot be cleared by the ISM.
ERASE SETUP	20H	The first command given in the two cycle erase sequence. The erase will not be completed unless followed by ERASE CONFIRM.
ERASE CONFIRM/RESUME	D0H	The second command given in the two cycle erase sequence. Must follow an ERASE SETUP command to be valid. Also used during an ERASE SUSPEND to resume the erase.
WRITE SETUP	40H or 10H	The first command given in the two cycle write sequence. The write data and address are given in the following cycle to complete the write.
ERASE SUSPEND	B0H	Halts the erase and puts device into the erase suspend mode. When in this mode only READ STATUS REGISTER, READ ARRAY and ERASE RESUME may be executed.

ISM STATUS REGISTER

The 8-bit ISM status register (see Table 2) is polled to check for write or erase completion or any related errors. During or following a write, erase, or erase suspend, a read operation will output the status register contents on DQ0 - DQ7 without prior command. While reading the status register contents, the outputs will not be updated if there is a change in the ISM status unless $\overline{OE}$ or $\overline{CE}$ is toggled. If the device is not in the write, erase, erase suspend, or status register read mode, READ STATUS REGISTER (70H) can be issued to view the status register contents.

All of the defined bits are set by the ISM, but only the ISM and erase suspend status bits are reset by the ISM. The erase, write, and VPP status bits must be cleared using CLEAR STATUS REGISTER. If the VPP status bit (SR3) is set, the CEL will not allow further write or erase operations until the status register is cleared. This allows the user to choose when to poll and clear the status register. For example, the host system may perform multiple byte write operations before checking the status register, instead of checking after each individual write. Asserting the $\overline{RST}$ signal or powering down the device are other methods to clear the status register.

Table 2
STATUS REGISTER

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	ISM STATUS 1 = Ready 0 = Busy	The ISMS bit displays the active status of the state machine when performing write or block erase. The controlling logic polls this bit to determine when the erase and write status bits are valid.
SR6	ERASE SUSPEND STATUS 1 = Erase Suspended 0 = Erase in Progress/Completed	Issuing an ERASE SUSPEND places the ISM in the suspend mode and sets this and the ISMS bit to "1." The ESS bit will remain "1" until an ERASE RESUME is issued.
SR5	ERASE STATUS 1 = Block erase error 0 = Successful block erase	ES is set to "1" after the maximum amount of erase cycles are executed by the ISM without a successful verify. ES is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR4	WRITE STATUS 1 = Write (word/byte) error 0 = Successful word/byte write	WS is set to "1" after the maximum amount of write cycles are executed by the ISM without a successful verify. WS is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR3	VPP STATUS 1 = No VPP voltage detected 0 = VPP present	VPPS detects the presence of a VPP voltage. It does not monitor VPP continously nor does it indicate a valid VPP voltage. The VPP pin is sampled for 12V after WRITE or ERASE CONFIRM is given. Must be cleared by CLEAR STATUS REGISTER or after a RESET.
SR0-2	RESERVED	Reserved for future use

COMMAND EXECUTION

Commands are issued to bring the device into different operational modes. Each mode has specific operations that can be performed while in that mode. Several modes require a sequence of commands to be written before they are reached. The following section describes the properties of each mode and Table 3 lists all command sequences required to perform the desired operation.

READ ARRAY

The array read mode is the initial state of the device upon powerup, and is also entered after a RESET. If the device is in any other mode, READ ARRAY (FFH) must be given to return to the array read mode. Unlike the WRITE SETUP command (40H), READ ARRAY does not need to be given before each individual read access.

IDENTIFY DEVICE

The 8-bit device identification may be read using one of two methods. IDENTIFY DEVICE (90H) may be written to the CEL to enter the identify device mode. While in this mode, any read will produce the device identification when A0 is HIGH and manufacturer identification when A0 is LOW. The device will remain in this mode until another command is given.

WRITE SEQUENCE

Two consecutive cycles are needed to input data to the array. WRITE SETUP (40H or 10H) is given in the first cycle. The next cycle is the WRITE, during which the write address and data are issued, and V_{PP} brought to V_{PPH}. Writing to the boot block also requires that the $\overline{RST}$ pin be brought to V_{HH} at the same time V_{PP} is brought to V_{PPH}. The ISM will now begin to write the word or byte. The desired bits within the word will be set to logic 0. V_{PP} must be held at V_{PPH} until the write is completed (SR7 = 1). When writing to the boot block, $\overline{RST}$ must be held at V_{HH} until the ISM status bit (SR7) is set.

While the ISM executes the write, the ISM status bit (SR7) will be at 0, and the device will not respond to any commands. However, any read operation will produce the status register contents on DQ0-DQ7. When the ISM status bit (SR7) is set, the write has been completed, and the device will go into the status register read mode until another command is given.

Table 3
COMMAND SEQUENCES

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE			2ND CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY	1	Write	X	FFH				1
IDENTIFY DEVICE	3	Write	X	90H	Read	IA	ID	2, 3
READ STATUS REGISTER	2	Write	X	70H	Read	X	SRD	4
CLEAR STATUS REGISTER	1	Write	X	50H				
ERASE SETUP/CONFIRM	2	Write	X	20H	Write	BA	D0H	5
ERASE SUSPEND/RESUME	2	Write	X	B0H	Write	X	D0H	
WRITE SETUP/WRITE	2	Write	X	40H	Write	WA	WD	6
ALTERNATE WORD /BYTE WRITE	2	Write	X	10H	Write	WA	WD	6

NOTE:
1. Must follow WRITE or ERASE CONFIRM commands to the CEL in order to enable flash array read cycles.
2. IA = Identify address; 00H for manufacturer ID, 01H for device ID.
3. ID = Indentify data.
4. SRD = Status Register Data.
5. BA = Block address.
6. WA = Address to be written, WD = Data to be written to WA.

After the ISM has initiated the write, it cannot be aborted except by a RESET or by powering-down the part. Doing either during a write will corrupt the data being written. If only the WRITE SETUP command has been given, the write may be nullified by performing a null WRITE. To execute a null WRITE, FFH must be written when $\overline{BYTE}$ is LOW, or FFFFH must be written when $\overline{BYTE}$ is HIGH. Once the ISM status bit (SR7) has been set, the device will be in the status register read mode until another command is issued.

ERASE SEQUENCE

Executing an erase sequence will set all bits within a block to logic 1. The command sequence necessary to execute an erase is similar to that of a write. To provide added security against accidental block erasure, two consecutive command cycles are required to initiate an erase of a block. In the first cycle, addresses are "don't care," and ERASE SETUP (20H) is given. In the second cycle, V_{PP} must be brought to V_{PPH}, an address within the block to be erased is issued, and ERASE CONFIRM (D0H) is given. If ERASE CONFIRM is not given, the ISM and erase status bits (SR7 and SR5) will be set, and the device will return to the array read mode.

At this time, the ISM will start the erase of the block. Any read operation will output the status register contents on DQ0-DQ7. V_{PP} must be held at V_{PPH} until the erase is completed (SR7 = 1). Once the erase is completed, the device will be in the status register read mode until another command is issued. Erasing to the boot block also requires that the $\overline{RST}$ pin be set to V_{HH} at the same time V_{PP} is set to V_{PPH}.

ERASE SUSPENSION

The only command that may be issued while an erase is in progress is ERASE SUSPEND. This command allows other commands to be executed while pausing the erase in progress. Once the device has reached the erase suspend mode, the erase suspend status bit (SR6) will be set. The device may now be given a READ ARRAY, ERASE RESUME, or READ STATUS REGISTER command. After READ ARRAY has been issued, any location not within the block being erased may be read. If ERASE RESUME is issued before SR6 has been set, the device will immediately proceed with the erase in progress. During the suspend mode V_{PP} must be held at V_{PPH}.

ERROR HANDLING

After the ISM status bit (SR7) has been set, the V_{PP} (SR3), write (SR4), and erase (SR5) status bits may be checked. If one or a combination of these three bits has been set, then an error has occurred. The ISM cannot reset these three bits. To clear these bits, CLEAR STATUS REGISTER (50H) must be given. If the V_{PP} status bit (SR3) is set, further write or erase operations cannot resume until the status register is cleared. Table 4 lists the combination of errors.

Table 4
STATUS REGISTER ERROR DECODE[1]

STATUS BITS			
SR5	SR4	SR3	ERROR DESCRIPTION
0	0	0	No errors
0	0	1	V_{PP} voltage error
0	1	0	Write error
0	1	1	Write error, V_{PP} voltage not valid at time of WRITE
1	0	0	Erase error
1	0	1	Erase error, V_{PP} voltage not valid at time of ERASE CONFIRM
1	1	0	Command sequencing error
1	1	1	Command sequencing error, programming voltage error

NOTE: 1. SR3 - SR5 must be cleared using CLEAR STATUS REGISTER.

WRITE/ERASE CYCLE ENDURANCE

The MT28LF400 is designed and fabricated to meet advanced firmware storage requirements. To ensure this level of reliability, V_{PP} must be at 12V ±5% during write or erase cycles. Operation outside these limits may reduce the number of erase cycles that can be performed on the device. For further information on write and erase cycle endurance, refer to the Micron *Flash Reliability Monitor*.

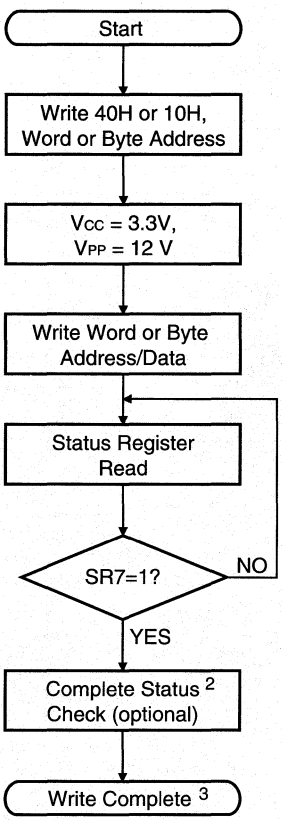
POWER USAGE

The MT28LF400 offers several power saving features that may be utilized in the array read mode to conserve power. With $\overline{CE}$ LOW, the device will enter idle current mode when not being accessed. In this mode, the maximum I_{CC} current is 2mA. When $\overline{CE}$ is HIGH, the device will enter standby mode. In this mode, maximum I_{CC} current is 120µA. If $\overline{CE}$ is brought HIGH during an erase or write, the ISM will continue to operate, and the device will consume the respective active power until the write or erase is completed.

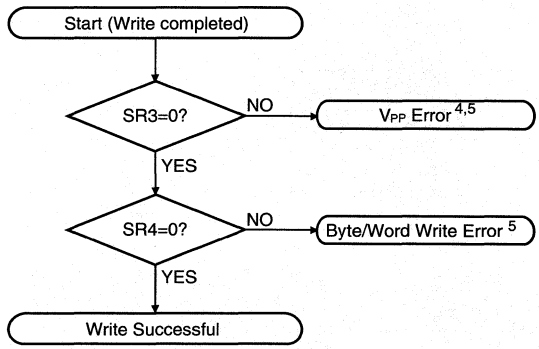
POWERUP

During a powerup, it is not necessary to sequence V_{CC} and V_{PP}. The likelihood of unwanted write or erase operations is minimized, since two consecutive cycles are required to execute either operation. However, $\overline{CE}$ or $\overline{WE}$ may be held HIGH, or $\overline{RST}$ can be held LOW during powerup for additional protection against unwanted write or erase operations. After a powerup or RESET, the status register is reset, and the device will enter the array read mode.

SELF-TIMED WRITE SEQUENCE (Word or Byte Write)[1]



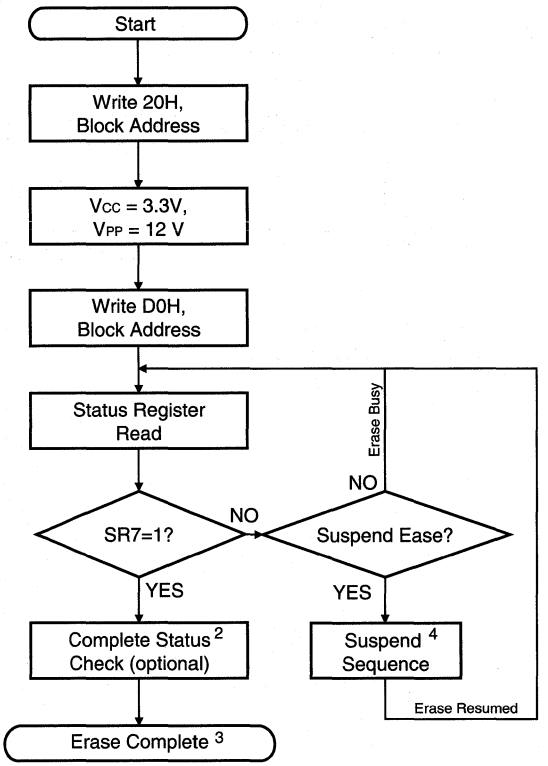
COMPLETE WRITE STATUS-CHECK SEQUENCE



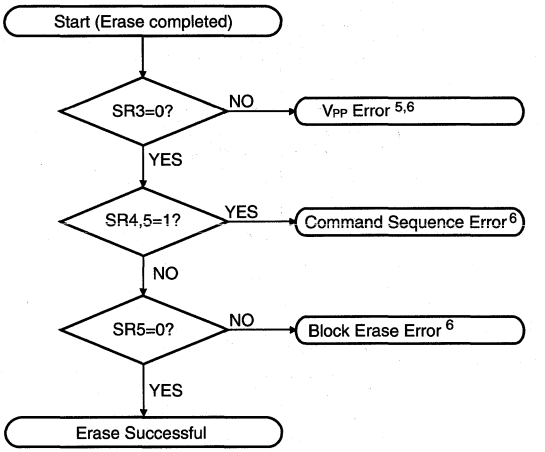
NOTE:
1. Sequence may be repeated for multiple byte or word writes.
2. Complete status check is not required. However, if SR3 = 1, further writes are inhibited until the status register is cleared.
3. Device will be in status register read mode. To return to the array read mode, the FFH command must be issued.
4. If SR3 is set during a write or block erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
5. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

NEW ■ 3.3/12 VOLT FLASH MEMORY

SELF-TIMED BLOCK ERASE SEQUENCE[1]

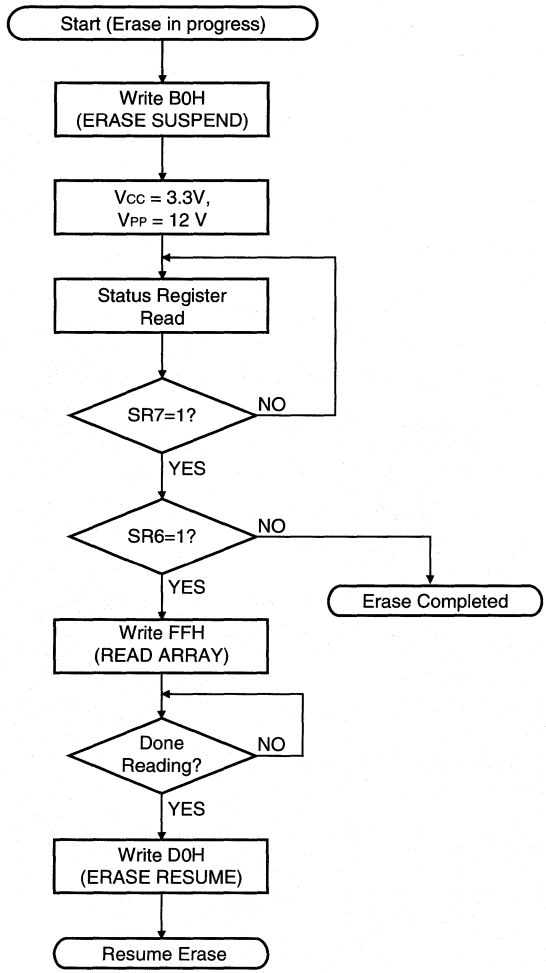


COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



NOTE:
1. Sequence may be repeated to erase multiple blocks.
2. Complete status check is not required. However, if SR3 = 1, further erases are inhibited until the status register is cleared.
3. To return to the array read mode, the FFH command must be issued.
4. Refer to the ERASE SUSPEND flowchart for more information.
5. If SR3 is set during a write or block erase attempt, CLEAR STATUS REGISTER must be issued before further write or erase operations are allowed by the CEL.
6. Status register bits 3 - 5 must be cleared using CLEAR STATUS REGISTER.

ERASE SUSPEND/RESUME SEQUENCE



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -2.0V to +4.6V
Input Voltage Relative to Vss ..... -0.5V to +4.6V**
VPP Voltage Relative to Vss ..... -0.5V to +12.6V†
$\overline{RST}$/Pin A9 Voltage Relative to Vss .... -0.5V to +13.5V**,†
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Input and I/O pins may transition to -2.0V for < 20ns and Vcc +2.0V for < 20ns.

†Voltage may pulse to 14.0V ≤ 20ns.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	1
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-0.5	0.6	V	1
Device Identification Voltage, A9	VID	11.4	13.0	V	1

DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C; Vcc = 3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS Output High Voltage (IOH = - 2.0 mA)	VOH	2.4		V	1
Output Low Voltage (IOL = 2.0 mA)	VOL		0.40	V	
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	IL	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.4V ≤ A9 ≤ 13.0 = VID)	IID		500	µA	
OUTPUT LEAKAGE CURRENT (Dout is disabled; 0V ≤ VOUT ≤ Vcc)	IOZ	-10	10	µA	

CAPACITANCE

(T_A = 25°C; Vcc = 3.3V ±0.3V; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	CI	8	pF	
Output Capacitance	CO	12	pF	

NOTE: 1. All voltages referenced to Vss.

READ AND STANDBY CURRENT DRAIN

($0°C \le T_A \le +70°C$; V_{CC} = 3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
READ CURRENT: WORD-WIDE, TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 8 MHz; Other inputs = V_{IL} or V_{IH}); $\overline{RST}$ = V_{IH}	I_{CC1}	30	mA	2, 3
READ CURRENT: WORD-WIDE, CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 8 MHz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V); $\overline{RST}$ = V_{IH}	I_{CC2}	30	mA	2, 3
READ CURRENT: BYTE-WIDE, TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 8 MHz; Other inputs = V_{IL} or V_{IH}); $\overline{RST}$ = V_{IH}	I_{CC3}	30	mA	2, 3
READ CURRENT: BYTE-WIDE, CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 8 MHz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V); $\overline{RST}$ = V_{IH}	I_{CC4}	30	mA	2, 3
READ CURRENT: V_{PP} SUPPLY (V_{PP} > V_{CC})	I_{PP1}	200	µA	
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RST}$ = V_{IH}, or $\overline{RST}$ = V_{IL}; other inputs = V_{IL} or V_{IH})	I_{CC5}	120	µA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RST}$ = V_{CC} - 0.2V; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V)	I_{CC6}	120	µA	
STANDBY CURRENT: V_{PP} SUPPLY (V_{PP} ≤ V_{CC})	I_{PP2}	±15	µA	
IDLE CURRENT: TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; f = 0 Hz; Other inputs = V_{IL} or V_{IH}; $\overline{RST}$ = V_{IH}; array read mode)	I_{CC7}	2	mA	
IDLE CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 0 Hz; Other inputs ≤ 0.2V, or ≥ V_{CC}-0.2V; $\overline{RST}$ = V_{IH}; READ ARRAY)	I_{CC8}	2	mA	

WRITE/ERASE CURRENT DRAIN

($0°C \le T_A \le +70°C$; V_{CC} = 3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
WORD-WRITE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC9}	30	mA	
WORD-WRITE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP3}	40	mA	
BYTE-WRITE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC10}	30	mA	
BYTE-WRITE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP4}	30	mA	
ERASE CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%)	I_{CC11}	20	mA	
ERASE CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%)	I_{PP5}	30	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (V_{PP} = 12V ±5%; erase suspended)	I_{CC12}	6	mA	4
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (V_{PP} = 12V ±5%; erase suspended)	I_{PP6}	200	µA	

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$; $V_{CC} = 3.3V \pm 0.3V$)

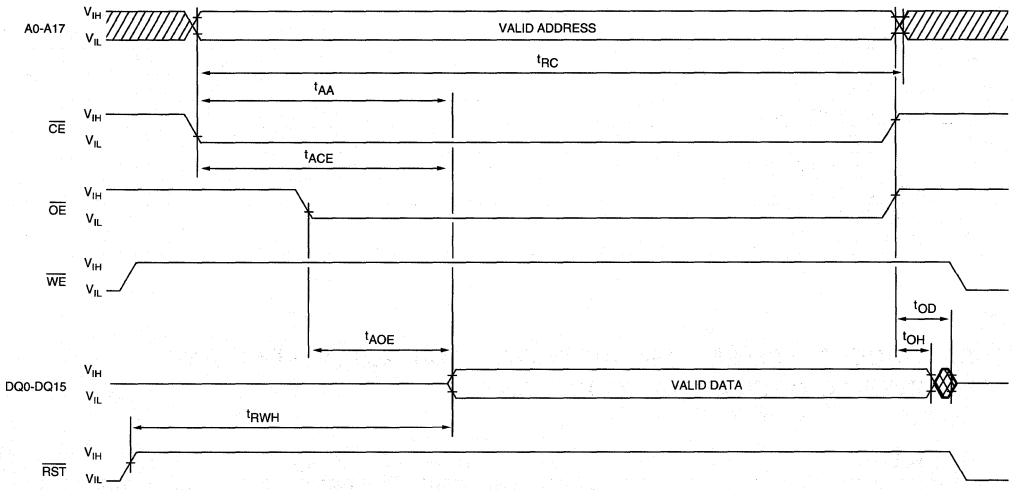
AC CHARACTERISTICS		-9		-10		-12			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read cycle time	^tRC	90		100		120		ns	
Access time from $\overline{CE}$	^tACE		90		100		120	ns	5
Access time from $\overline{OE}$	^tAOE		45		50		60	ns	5
Access time from address	^tAA		90		100		120	ns	
$\overline{RST}$ HIGH to output valid delay	^tRWH		600		600		600	ns	
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		35		40		45	ns	
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		0		0		ns	

AC TEST CONDITION

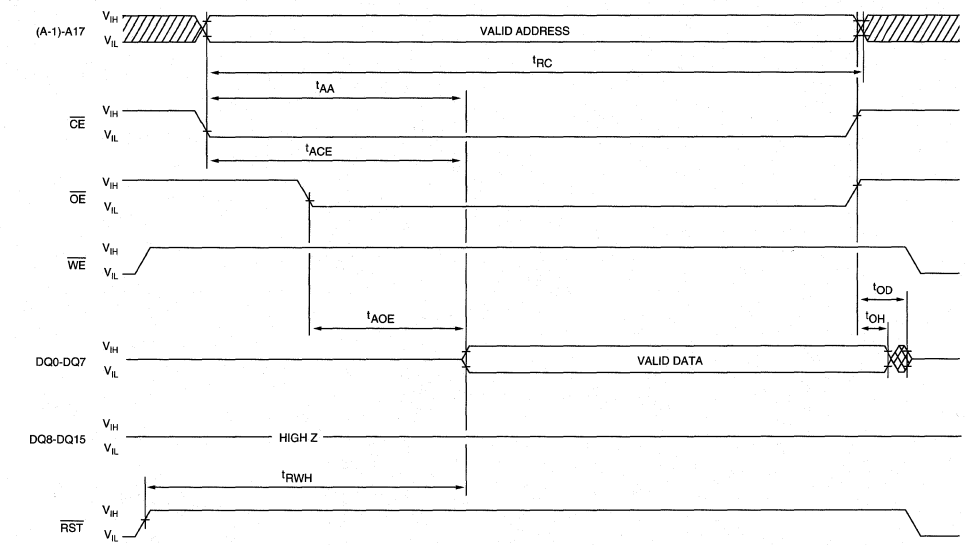
Input pulse levels	0.0 to 3.0V
Input rise and fall times	<10ns
Input timing reference level	1.5 V
Output timing reference level	1.5 V
Output load	1 TTL gate and $C_L = 50$ pF

NOTE:
1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on cycle rates.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Parameter is specified when device is not accessed. Actual current draw will be $I_{CC}12$ plus read current if a read is executed while in erase suspend mode.
5. $\overline{OE}$ may be delayed by ^tACE minus ^tAOE after $\overline{CE}$ falls before ^tACE is affected.

WORD-WIDE READ CYCLE [1]



BYTE-WIDE READ CYCLE [2]



DON'T CARE

UNDEFINED

NOTE: 1. $\overline{BYTE}$ = HIGH
2. $\overline{BYTE}$ = LOW

RECOMMENDED DC WRITE/ERASE CONDITIONS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
V_{PP} voltage during normal operation	V_{PPL}	0.0	4.1	V	
V_{PP} voltage during erase/write operation	V_{PPH}	11.4	12.6	V	
Boot block unlock voltage	V_{HH}	11.4	13.0	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.6	V	
INPUT LEAKAGE CURRENT: $\overline{RST}$ INPUT ($11.4 \le \overline{RST} \le 13.0V = V_{HH}$)	I_{HH}		500	µA	

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{CC} = 3.3V ±0.3V)

AC CHARACTERISTICS		-9		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WRITE cycle time	^tWC	90		100		120		ns	
$\overline{WE}$ HIGH pulse width	^tWPH	30		30		40		ns	
$\overline{CE}$ HIGH pulse width	^tCPH	30		30		40		ns	

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{WE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 3.3V ±0.3V)

AC CHARACTERISTICS		-9 , -10, -12			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{WE}$ HIGH	^tAS	95		ns	
Address hold time from $\overline{WE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{WE}$ HIGH	^tDS	100		ns	
Data hold time from $\overline{WE}$ HIGH	^tDH	0		ns	
$\overline{CE}$ setup time to $\overline{WE}$ LOW	^tCS	0		ns	
$\overline{CE}$ hold time from $\overline{WE}$ HIGH	^tCH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	200		ns	1
$\overline{WE}$ pulse width	^tWP	100		ns	
$\overline{RST}$ HIGH to $\overline{WE}$ LOW delay	^tRS	1		µs	
$\overline{RST}$ V_{HH} setup time to $\overline{WE}$ HIGH	^tRHS	200		ns	2
Write duration (word or byte write)	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		200	ns	3

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: $\overline{CE}$ CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = 3.3V ±0.3V)

AC CHARACTERISTICS		-9 , -10, -12			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to $\overline{CE}$ HIGH	^tAS	95		ns	
Address hold time from $\overline{CE}$ HIGH	^tAH	10		ns	
Data setup time to $\overline{CE}$ HIGH	^tDS	100		ns	
Data hold time from $\overline{CE}$ HIGH	^tDH	0		ns	
$\overline{WE}$ setup time to $\overline{CE}$ LOW	^tWS	0		ns	
$\overline{WE}$ hold time from $\overline{CE}$ HIGH	^tWH	10		ns	
V_{PP} setup time to $\overline{WE}$ HIGH	^tVPS	200		ns	1
$\overline{CE}$ pulse width	^tCP	100		ns	
$\overline{RST}$ HIGH to $\overline{CE}$ LOW delay	^tRS	1		µs	
$\overline{RST}$ V_{HH} setup time to $\overline{CE}$ HIGH	^tRHS	200		ns	2
Write duration (word or byte write)	$^tWED1$	6		µs	1
Boot-block erase duration	$^tWED2$	300		ms	1, 2
Parameter block erase duration	$^tWED3$	300		ms	1
Main block erase duration	$^tWED4$	600		ms	1
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
$\overline{RST}$ at V_{HH} hold time from Status Data valid	^tRHH	0		ns	2
Boot block relock delay time	^tREL		200	ns	2

NOTE: 1. Write/erase times are measured to valid status register data (SR7=1).
2. $\overline{RST}$ should be held at V_{HH} until boot-block write or erase is complete.
3. ^tREL is required to relock boot block after write or erase to boot block.

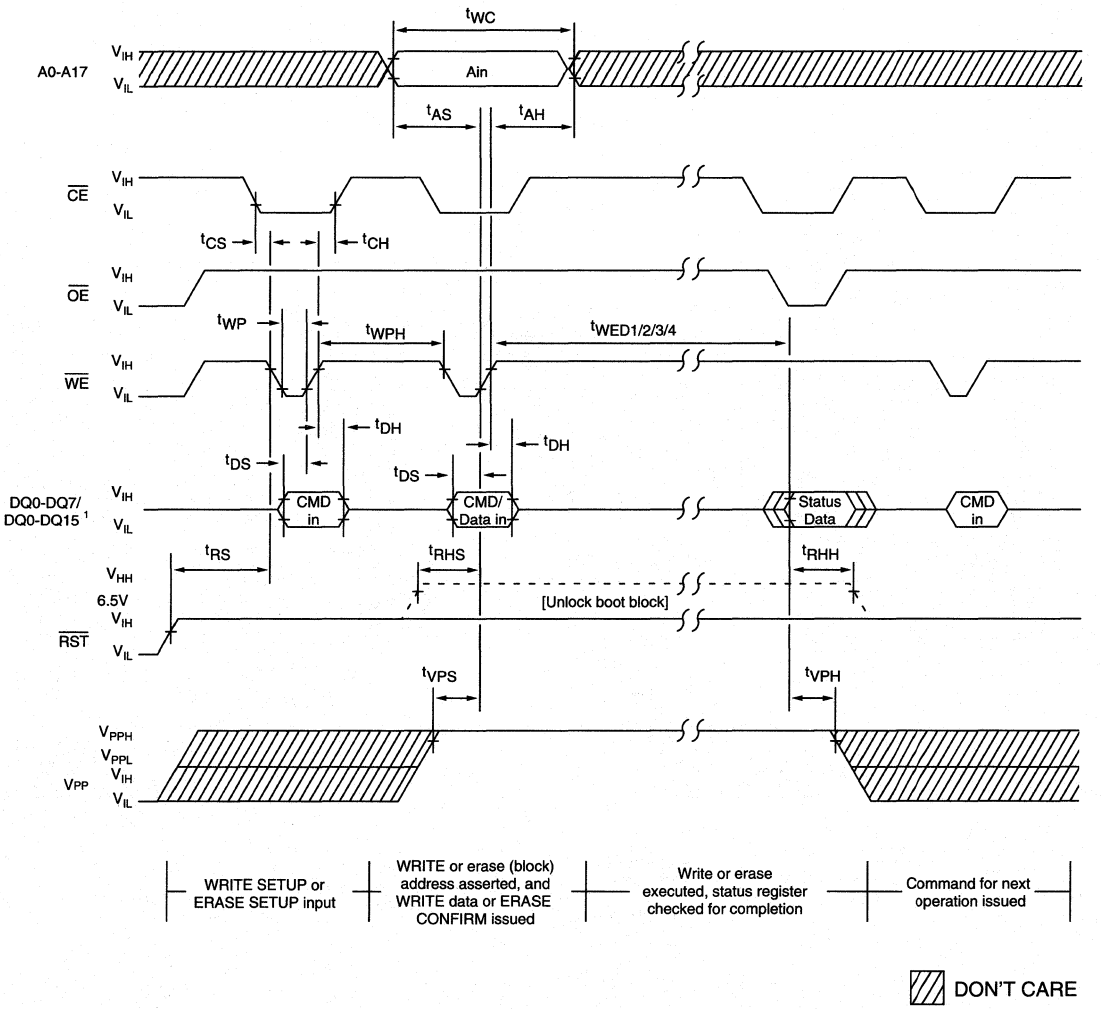
WORD/BYTE WRITE AND ERASE DURATION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Boot/parameter block erase time		2.0	8.0	s	1
Main block erase time		3.5	18.0	s	1
Main block byte write time		1.5	5.5	s	1, 2
Main block word write time		0.8	2.5	s	1, 2

NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.

NEW ■ 3.3/12 VOLT FLASH MEMORY

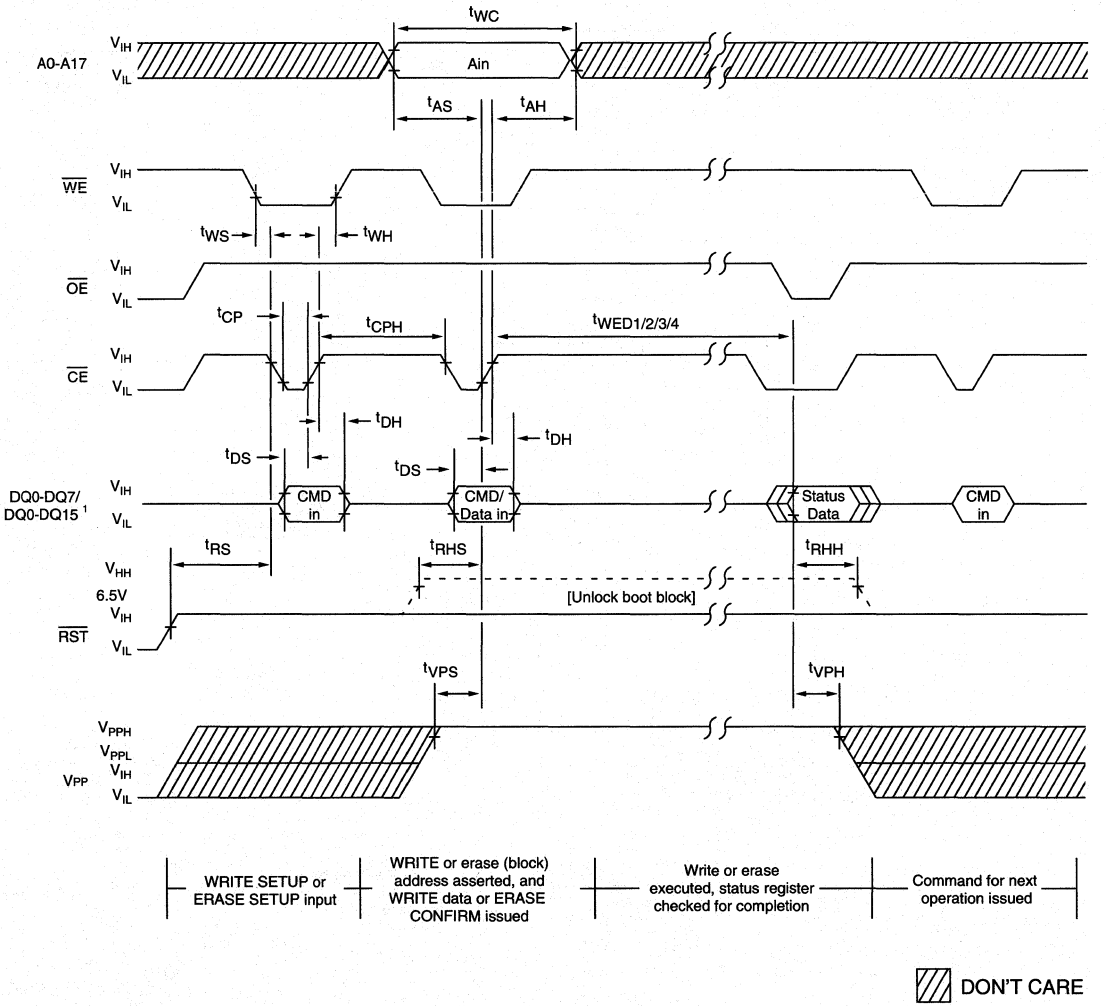
ERASE/WRITE CYCLE
WE-CONTROLLED WRITE/ERASE



NOTE: 1. If $\overline{BYTE}$ is LOW, DATA and COMMAND are 8-bit. If $\overline{BYTE}$ is HIGH, DATA is 16-bit and COMMAND is 8-bit.

NEW ■ 3.3/12 VOLT FLASH MEMORY

ERASE/WRITE CYCLE
$\overline{CE}$-CONTROLLED WRITE/ERASE



NOTE: 1. If $\overline{BYTE}$ is LOW, DATA and COMMAND are 8-bit. If $\overline{BYTE}$ is HIGH, DATA is 16-bit and COMMAND is 8-bit.

NEW ■ 3.3/12 VOLT FLASH MEMORY

FLASH MEMORY 1 MEG x 8

3.3V/12V, SYMMETRIC BLOCK

FEATURES

- Sixteen 64KB blocks
- Low power: 120µA standby; 30mA active, MAX
- 3.3V±0.3V read; 12V±5% write/erase
- Address access time: 100ns and 150ns
- Industry-standard pinouts
- READY/$\overline{\text{BUSY}}$ (R/$\overline{\text{B}}$) output and status register write/erase polling
- High-performance CMOS floating-gate process
- Inputs and outputs are fully TTL-compatible
- Three-state outputs
- Automated write and erase algorithm
- TSOP Packaging option

OPTIONS MARKING

- Timing
  - 100ns access -10
  - 150ns access -15
- Packages
  - Plastic SOP (600 mil) SG
  - Plastic TSOP Type 1 (10 x 20mm) VG
- Part Number Example: MT28LF008VG-10

GENERAL DESCRIPTION

The MT28LF008 is a nonvolatile, electrically block-erasable (FLASH), programmable read-only memory containing 8,388,608 bits organized as 1,048,576 words by 8 bits. It is fabricated with Micron's advanced 3.3V CMOS floating-gate process.

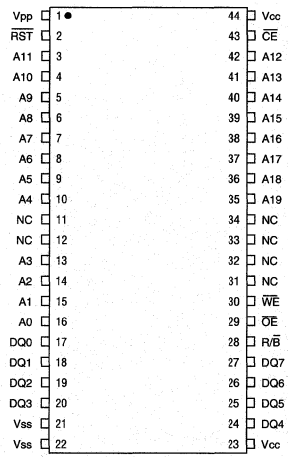
The MT28LF008 is organized into 16 separately erasable 64KB blocks. Data is read and written on a random access basis, and erased in blocks. To write or erase the device, a super-voltage must be applied to the V_{PP} pin. This provides the necessary voltage and current required to write or erase the cells, and provides additional security against accidental erasure or overwrite. The internal state machine executes all write and erase algorithms and timing to the memory array.

In addition to status register polling, the MT28LF008 provides a READY/$\overline{\text{BUSY}}$ (R/$\overline{\text{B}}$) output to indicate write and erase completion. Operations are executed by issuing commands from an industry standard command set.

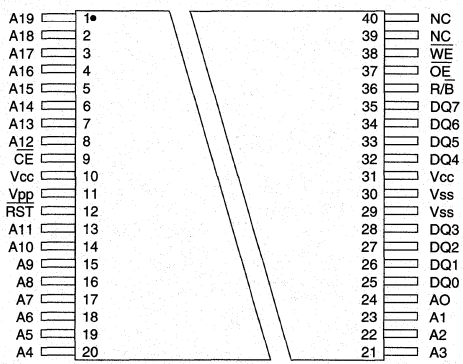
To read the array, the byte address is issued with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ LOW and $\overline{\text{WE}}$ HIGH. Valid data is output until the next address is issued or until $\overline{\text{CE}}$ or $\overline{\text{OE}}$ go HIGH.

PIN ASSIGNMENT (Top View)

44-Pin SOP
(FA-1)



40-Pin TSOP Type I
(FB-1)



MICRON
QUANTUM DEVICES, INC.

5/12 VOLT FLASH MEMORY 1

3.3/12 VOLT FLASH MEMORY 2

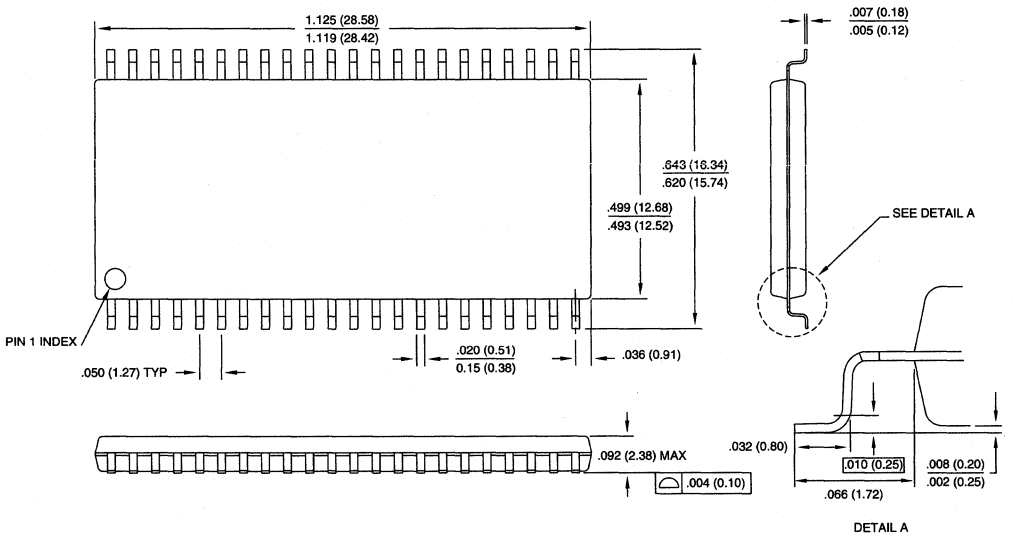
PACKAGE INFORMATION 3

SALES INFORMATION 4

PACKAGE TYPE	PIN COUNT	PAGE
PLASTIC SOP	44	3-2
PLASTIC TSOP	40	3-3
	56	3-4

44-PIN PLASTIC SOP (600 mil)

FA-1

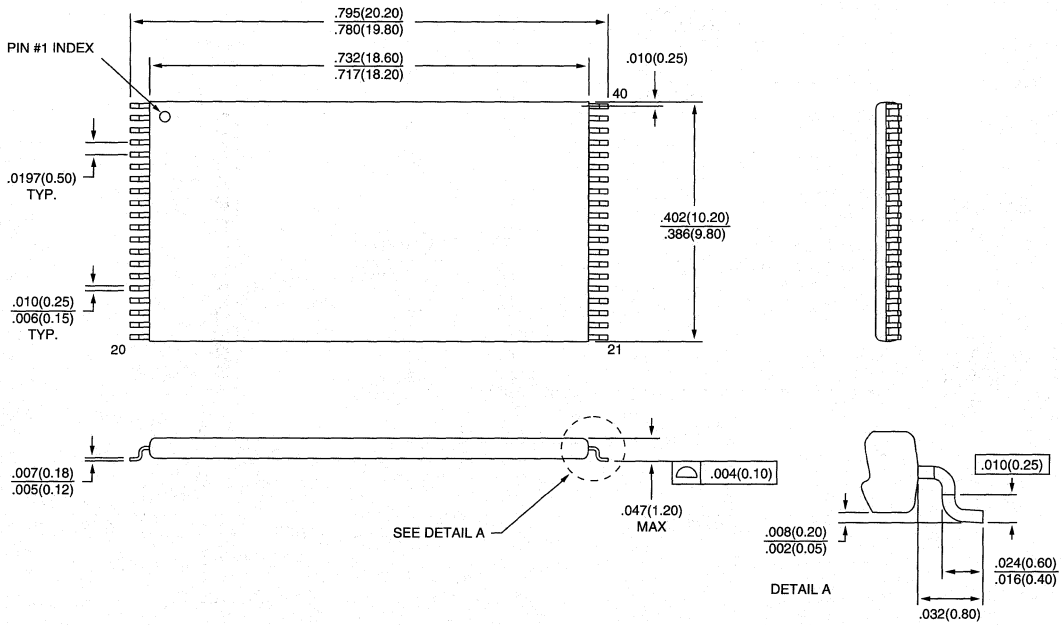


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

40-PIN PLASTIC TSOP (10mm x 20mm)

FB-1

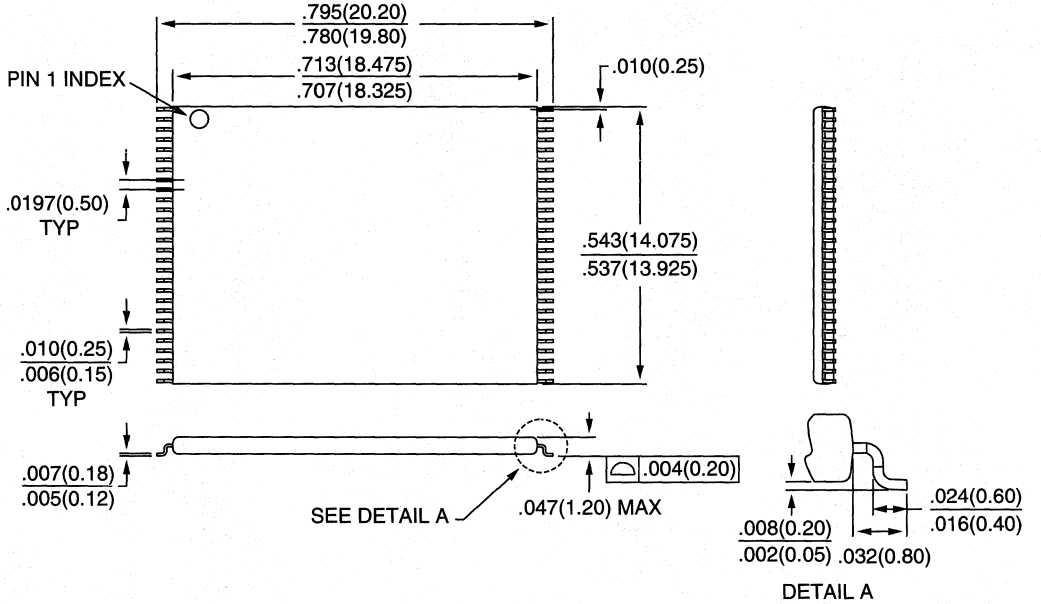


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

56-PIN PLASTIC TSOP (14mm x 20mm)

FB-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

MICRON
QUANTUM DEVICES, INC.

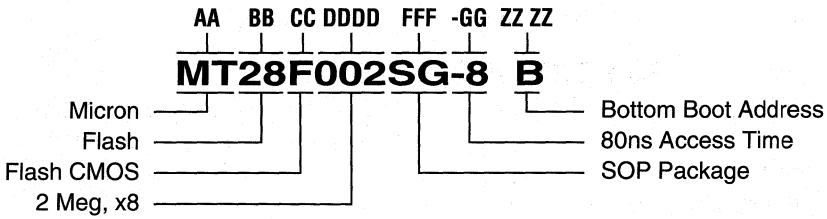
5/12 VOLT FLASH MEMORY 1

3.3/12 VOLT FLASH MEMORY 2

PACKAGE INFORMATION 3

SALES INFORMATION 4

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Micron Product ..... MT

BB – PRODUCT FAMILY
Flash 28
DRAM 4
TPDRAM 43
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY
CMOS C
Low Voltage CMOS LC
Flash CMOS ..... F
Low Voltage Flash CMOS ..... LF

DDDD – DEVICE NUMBER
(Can be modified to indicate variations)

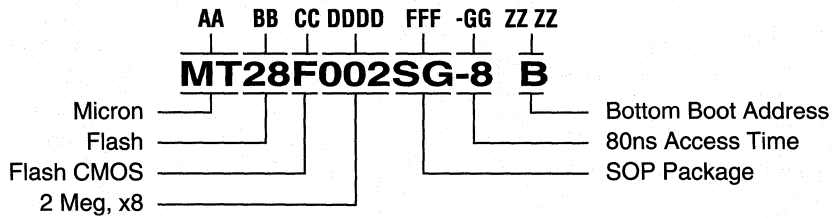
Flash ..... Density, Configuration
DRAM ..... Width, Density
TPDRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Density, Width

E – DEVICE VERSIONS
(Alphabetic characters only; located between D and F when required.)

JEDEC Test Mode (4 Meg DRAM) ..... J
Errata on Base Part ..... Q

FFF – PACKAGE CODES
PLASTIC
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type I) ..... VG
TSOP (Type I, Reversed) ..... XG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-50 (SRAM only)	50ns
-53	53ns
-55	55ns
-70 (SRAM only)	70ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Flash	
Bottom Boot	B
Top Boot	T
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

ORDER INFORMATION*

Each Micron Quantum Devices component family is manufactured and quality controlled in the U.S.A. at Micron Semiconductor's modern Boise, Idaho, facility employing our low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron System Integration's exclusive AMBYX intelligent burn-in and test system.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributor nearest you. Micron's policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

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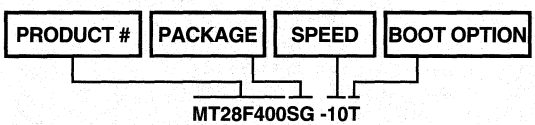
Micron DataFax: 208-368-5802
Customer Comment Line:
800-932-4992 (U.S.A.)
01-208-368-3410 (Intl.)

ORDER EXAMPLES

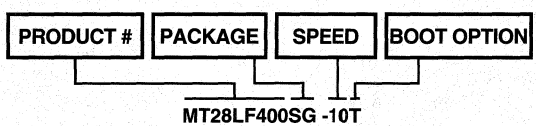
5 VOLT FLASH MEMORY

256K x 16, 512K x 8, 5V, 100ns in Plastic SOP



3.3 VOLT FLASH MEMORY

256K x 16, 512K x 8, 3.3VV, 100ns in Plastic SOP



*For more detailed information, refer to the product numbering charts on pages 4-1 through 4-2.

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