MITSUBISHI SEMICONDUCTORS 1987

BIPOLAR DIGITAL ICs
M54000 SERIES

DATA BOOK

MITSUBISHI ELECTRIC

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BIPOLAR DIGITAL ICs
M54000 SERIES

54564 2-229

54585 2-276

DATA BOOK

MITSUBISHI ELECTRIC

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BIPOLAR PROMS

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M54730AP,S				50			—	
M54731AP,S-1	256-Bit (32×8) Field Programmable Read Only Memory	B,S,TTL	350	30	32×8	16P4 16S1	—	2—385
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M54731AP,S				50			—	
M54700AP,S-1	1024-Bit (256×4) Field Programmable Read Only Memory	B,S,TTL	400	30	256×4	16P4 16S1	93417	2—381
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M54700AP,S				50				
M54701AP,S-1	1024-Bit (256×4) Field Programmable Read Only Memory	B,S,TTL	400	30	256×4	16P4 16S1	93427	2—381
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M54701AP,S				50				
M54740AP,S-1	4096-Bit (1024×4) Field Programmable Read Only Memory	B,S,TTL	600	30	1024×4	18P4 18S1	93452	2—389
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M54740AP,S				50				
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M54741AP,S				50				

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Type No.	Circuit Function	Typical Electrical Characteristics (T_a=25℃)				Package Outline	Interchange-able products	Page
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M54543L	Bi-Directional Motor Driver with Brake Function	12	24	1200	300	9P9	BA6209	2—184
M54543AL	Bi-Directional Motor Driver with Brake Function and Thermal Shut Down Function	12	10	1200	300	9P9	—	2—187
M54544L	Bi-Directional Motor Driver with Brake Function	12	21	1200	300	9P9	—	2—190
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M54547P	Bi-Directional Motor Driver with OP Amp and Transister Array	12	4	600	150	16P4	—	2—202
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Type No	Circuit Function	Typical Electrical Characteristics(T_a=25℃)				Package Outline	Interchangeable products	Page
		Supply Voltage (V)	Supply Current (mW)	Rush Current (mA)	Constant Current (mA)			
M54641L	Bi-Directional Motor Driver with Brake Function	10	7.5	800	150	8P5	—	2—346
M54642L	Bi-Directional Motor Driver with Brake Function	10	7.5	800	150	10P5	—	2—349
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M54648AL	Bi-Directional Motor Driver with Motor Speed Control	16	30	3000	600	12P9B	—	2—367
M54649L	Dual Bi-Directional Motor Driver with Brake Function and Thermal Shut Down Function	12	19	1600	600	10P5	BA6238A BA6248	2—370

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Type No.	Circuit Function	Typical Electrical Characteristics(T_a=25℃)				Package Outline	Interchangeable products	Page
		Supply Voltage (V)	Low-level Output Current (mA)	High-level Output Current (mA)	Output with-Stand Voltage (V)			
M54640P	Stepper Motor Driver	45	20	800	45	16P4	PBL3717	2—340
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TRANSISTOR ARRAYS

Type No.	Circuit Function	Typical Electrical Characteristics(T_a=25℃)				Package Outline	Interchangeable products	Page
		Input Voltage (V)	Input Current (mW)	Collector Withstand Voltage (V)	Collector Current duty ratio (mA/%)			
M54512L	4-Unit 50mA Transistor Array	11	2	20	50/100	8P5	—	2—106
M54513P	8-Unit 50mA Transistor Array	2.5	0.7	40	50/100	18P4	—	2—108
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M54515P	7-Unit 16mA Transistor Array	0.75	1	17	16/100	16P4	—	2—112
M54516P	5-Unit 500mA Darlington Transistor Array	8	0.4	25	400/25	14P4	LB1288	2—114
M54517P	7-Unit 400mA Darlington Transistor Array	8	0.4	25	400/15	16P4	TD12605	2—117
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M54521P	5-Unit 500mA Darlington Transistor Array	1.35	1	30	400/20	14P4	IR3403	2—123
M54522P	8-Unit 400mA Darlington Transistor Array with Clamp Diode	8	0.4	40	400/15	18P4	—	2—126
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M54524P	7-Unit 500mA Darlington Transistor Array with Clamp Diode	1.4	1	50	400/15	16P4	ULN2001A	2—132
M54525P	7-Unit 500mA Darlington Transistor Array with Clamp Diode	17	0.9	50	400/15	16P4	ULN2002A	2—135
M54526P	7-Unit 500mA Darlington Transistor Array with Clamp Diode	8	0.9	50	400/15	16P4	ULN2004A	2—138
M54527P	6-Unit 150mA Darlington Transistor Array with Clamp Diode	7	0.3	40	150/90	14P4	LB1274	2—141

TRANSISTOR ARRAYS (Continued)

Type No	Circuit Function	Typical Electrical Characteristics (T_a=25℃)				Package Outline	Interchangeable products	Page
		Input Voltage (V)	Input Current (mW)	Collector Withstand Voltage (V)	Collector Current duty ratio (mA/%)			
M54528P	7-Unit 150mA Darlington Transistor Array with Clamp Diode	7	0.3	40	150/80	16P4	LB1275	2—143
M54529P	5-Unit 320mA Transistor Array with Strobe	7	0.3	20	320/60	14P4	—	2—145
M54529AP	5-Unit 320mA Transistor Array with Strobe	3.5	0.05	20	320/60	14P4	—	2—148
M54530P	7-Unit 400mA Darlington Transistor Array with Clamp Diode	8	0.4	40	400/15	16P4	IR2411	2—151
M54531P	7-Unit 400mA Darlington Transistor Array with Clamp Diode	9	0.4	40	400/15	16P4	IR2410	2—154
M54532P	4-Unit 1.5A Darlington Transistor Array with Clamp Diode	3	5	50	1250/10	16P4	ULN2064A	2—157
M54533P	6-Unit 320mA Transistor Array with Clamp Diode and Strobe	7	0.3	20	320/50	16P4	—	2—160
M54534P	6-Unit 320mA Transistor Array with Clamp Diode and Strobe	3.2	0.5	20	320/50	16P4	IR2425	2—163
M54535P	7-Unit 150mA Transistor Array with Clamp Diode and Strobe	7	0.3	V_{CC}	150/85	18P4	LB1260	2—166
M54536P	7-Unit 150mA Transistor Array with Clamp Diode and Strobe	3.2	0.7	V_{CC}	150/85	18P4	—	2—169
M54537P	7-Unit 350mA Transistor Array	3.2	0.8	20	350/60	16P4	—	2—172
M54538P	7-Unit 350mA Transistor Array and Motor Driver	3.2	0.8	20	350/45	18P4	—	2—175
M54539P	6-Unit 700mA Transistor Array with Clamp Diode	3.2	0.8	20	*700/40	16P4	IR2420	2—178
M54560P	7-Unit 150mA Source Type Darlington Transistor Array with Clamp Diode	V_S—5V	—0.2	40	—150/75	16P4	—	2—217
M54561P	7-Unit 300mA Source Type Darlington Transistor Array with Clamp Diode	V_S—3.5V	—0.15	40	—300/20	16P4	—	2—220
M54562P	8-Unit 500mA Source Type Darlington Transistor Array with Clamp Diode	4	0.35	50	—400/15	18P4	UDN2982A	2—223
M54563P	8-Unit 500mA Source Type Darlington Transistor Array with Clamp Diode	2.4	0.4	50	—400/15	18P4	UDN2981A	2—226
M54564P	8-Unit 500mA Source Type Darlington Transistor Array	4	0.35	50	—400/15	18P4	—	2—229
M54565P	8-Unit 50mA Transistor Array ("L" Active Input)	V_{CC}—0.75	—0.2	20	50/100	18P4	—	2—232
M54566P	7-Unit 400mA Darlington Transistor Array ("L" Active Input)	V_{CC}—3	—0.3	50	400/15	16P4	TD62304	2—234
M54567P	4-Unit 1.5A Darlington Transistor Array with Clamp Diode	V_{CC}—3.5	—0.3	50	1250/10	16P4	TD62308AP	2—237
M54568L	4-Unit 30mA PNP Transistor Array	V_{CC}—0.8	—2	30	—30/100	10P5	—	2—240
M54569P	8-Unit 30mA PNP Transistor Array	V_{CC}—0.8	—2	30	—30/100	18P4	—	2—242
M54571P	6-Unit 350mA Transistor Array and Motor Driver	9	2	43	350/20	20P4	—	2—246
M54574P	4-Unit 700mA Transistor Array with Clamp Diode	9	3	43	350/20	16P4	—	2—253
M54575P	8-Unit 150mA Transistor Array with Clamp Diode and Strobe	9	3	43	350/20	20P4	—	2—255
M54576P, FP	7-Unit 30mA Transistor Array ("L" Active Input)	3	0.06	30	50/100	16P4 16P2	—	2—257
M54577P, FP	7-Unit 30mA Transistor Array	3	0.06	30	50/100	16P4 16P2	—	2—259

TRANSISTOR ARRAYS (Continued)

Type No	Circuit Function	Typical Electrical Characteristics (T_a=25℃)				Package Outline	Interchangeable products	Page
		Input Voltage (V)	Input Current (mA)	Collector Withstand Voltage (V)	Collector Current duty ratio (mA/%)			
M54578P	6-Unit 700mA Transistor Array with Clamp Diode and Strobe	3.5	0.5	20	*700/40	16P4	—	2—261
M54580P	7-Unit 150mA Source Type Darlington Transistor Array	Vs—3.5	—0.3	50	—150/80	16P4	—	2—264
M54581P	8-Unit 500mA Source Type Darlington Transistor Array with Clamp Diode	Vs—3.6	—0.3	50	—400/15	18P4	UDN2580A	2—267
M54583P	8-Unit 400mA Darlington Transistor Array	V_{CC}—3.6	—0.3	50	350/10	18P4	—	2—270
M54584P	8-Unit 350mA Transistor Array	3	0.8	20	250/50	18P4	—	2—273
M54585P	8-Unit 500mA Darlington Transistor Array with Clamp Diode	3.85	0.9	50	400/6	18P4	ULN2803A	2—276
M54586P	8-Unit 500mA Source Type Darlington Transistor Array	Vs—3.6	—0.3	50	—300/8	18P4	—	2—279
M54590P	8-Unit High Voltage 500mA Darlington Transistor Array with Clamp Diode	3.85	1	80	400/10	18P4	ULN2823A	2—282
M54591P	8-Unit High Voltage 500mA Darlington Transistor Array with Clamp Diode	1.4	1	80	400/10	18P4	ULN2821A	2—285
M54592P	8-Unit High Voltage 500mA Darlington Transistor Array with Clamp Diode	1.7	0.9	80	400/10	18P4	ULN2824A	2—288
M54593P	8-Unit High Voltage 500mA Darlington Transistor Array with Clamp Diode	8	0.9	80	400/10	18P4	ULN2824A	2—291
M54594P	4-Unit High Voltage 1.5A Darlington Transistor Array with Clamp Diode	3	5	80	1250/4	16P4	ULN2064B	2—294
M54595P	4-Unit 1.5A Darlington Transistor Array with Clamp Diode	8	5	80	1250/4	16P4	ULN2067B	2—297
M54596P	4-Unit High Voltage 1.5A Darlington Transistor Array with Clamp Diode	V_{CC}—3.5	—0.3	80	1250/4	16P4	TD62308BP	2—300
M54597P	8-Unit High Voltage 500mA Source Type Darlington Transistor Array	4	0.35	80	—350/8	18P4	UDN2984A	2—303
M54598P	8-Unit High Voltage 500mA Source Type Darlington Transistor Array	2.4	0.4	80	—350/8	18P4	UDN2983A	2—306
M54660P	8-Unit High Voltage 500mA Source Type Darlington Transistor Array	Vs—3.6	—0.3	80	—350/8	18P4	UDN2580A1	2—375
M54661P	4-Unit High Voltage 1.5A Darlington Transistor Array with Clamp Diode	V_{CC}—3.6	—0.3	80	1250/4	16P4	LB1205	2—378

* : Synchronous operation of 3 circuits

DISPLAY DECODER/DRIVERS

Type No	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃)				Package Outline	Interchangeable products	Page
			Power dissipation (mW)	Low-level Output Current (mA)	High-level Output Current (mA)	Output Withstand Voltage (V)			
M54405P	4-Bit Binary-to-Seven-Segment Decoder/Driver	TTL	300	16	0.25	15	16P4	—	2—42
M54406P	BCD-to-Seven-Segment Decoder/Driver	TTL	265	20	0.2	15	16P4	—	2—46
M54940P/FP	8-Digit Fluorescent Display Driver for Microcomputer	I^2L	150	—	—10	35	30P4B/ 32P2W-A	—	2—479
M54844P	8-Digit Fluorescent Display Driver for Microcomputer	I^2L	120	—	—10	33	28P4	—	2—424
M54847AP	2-Digit BCD-to-Seven-Segment Decoder/Driver	I^2L	75	—	—10	25	30P4B	—	2—428
M54480P	RGB Decoder	ECL	650	30	—	5.5	24P4	—	2—91

CURRENT DRIVER/PERIPHERAL DRIVERS

Type No	Circuit Function	Typical Electrical Characteristics(V_{CC}=5V, T_a=25℃)				Package Outline	Interchangeable products	Page
		Power* dissipation (mW)	Low-level Output Current (mW)	Output Withstand Voltage (V)	Propagation time (ns)			
M54502P	Dual AND Gate with Drive Transistor	430	300	30	—	14P4	—	2—96
M54503P	Quadruple Current Driver	390	100	30	—	14P4	—	2—100
M54504P	Dual NAND Gate with Drive Transistor	360	300	30	—	14P4	SN75450N	2—102
M54600P	Dual Peripheral Positive AND Driver	150	300	30	20	14P4	SN75450BN	2—309
M54601P	Dual Peripheral Positive AND Driver	150	300	30	18	8P4	SN75451BP	2—315
M54602P	Dual Peripheral Positive NAND Driver	170	300	30	25	8P4	SN75452BP	2—318
M54603P	Dual Peripheral Positive OR Driver	155	300	30	17	8P4	SN75453BP	2—321
M54604P	Dual Peripheral Positive NOR Driver	185	300	30	26	8P4	SN75454BP	2—324
M54605P	Dual Peripheral Positive NAND Driver	170	300	30	28	14P4	—	2—327

* : I_{OL}=0

HIGH SPEED DIVIDERS

Type No.	Circuit Function	Typical Characteristics(T_a=25℃)				Package Outline	Interchangeable products	Page
		Supply Voltage (V)	Count Frequency (MHz)	Input Sensitivity (dBm)	Output			
M54455L	1/4, 1/8, 1/40 High Speed Divider	5.0	30~130	200	Open Collector	8P5	—	2—58
M54459L	1/20, 1/100 High Speed Divider	5.0	30~130	180	Open Collector	8P5	—	2—60
M54460L	1/10, 1/100 High Speed Divider	5.0 or 3.0	30~130	180	Open Collector	8P5	—	2—62
M54466L	1/10, 1/11 High Speed Divider with ECL Output	5.0	30~300	400	ECL	8P5	—	2—64
M54468AL	1/256 High Speed Divider with ECL Output	5.0	80~1100	400	ECL	8P5	TD6108	2—68
M54471P/L ★★	1/64 High Speed Divider with ECL Output	5.0	80~1250	400	ECL	8P4,8P5		2—70
M54472L	1/64 High Speed Divider with ECL Output	5.0	80~1100	400	ECL	8P5	TD6107	2—72
M54473P/L	1/256 High Speed Divider with TTL Output	5.0	80~1250	400	TTL	8P4,8P5	TD6111	2—74
M54475P	1/64, 1/65, 1/128, 1/129 2-Modulus High Speed Divider with ECL Output	5.0	700~1000	400	ECL	8P4	μPB566C	2—76
M54477P/L M54477AP	1/128, 1/136 2-Modulus High Speed Divider with ECL Output	5.0	80~1000	100	ECL	8P5 8P4	μPB562AC	2—80 2—83
M54478P	1/256 High Speed Divider with ECL Output	5.0	80~860	50	ECL	8P4	SP4683	2—86
M54479P ★★	1/64 High Speed Divider	5.0	700~1900	200	ECL	10P2-C		2—88

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PLL FREQUENCY SYNTHESIZERS

Type No.	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃) Supply Voltage (V)	Power dissipation (mW)	Output Withstand Voltage (V)	Operation Frequency (MHz)	Package Outline	Interchangeable products	Page
M54927P	PLL Frequency Synthesizer for Digital Tuning Systems	ECL/I^2L	5	150	6	120	16P4	—	2—454
M54928P	PLL Frequency Synthesizer for Digital Tuning Systems	ECL/I^2L	5	150	6	120	22P4	—	2—463
M54929P	PLL Frequency Synthesizer for Amateur Radios	ECL/I^2L	5	300	6	300	16P4		2—472
M54956P	PLL Frequency Synthesizer for Personal Radios	ECL/I^2L	5	200	6	1000	16P4	—	2—484
M54959P	PLL Frequency Synthesizer for Personal Radios	ECL/I^2L	5	100	6	500	16P4	—	2—492
M54965ASP ★★	Serial Input PLL Frequency Synthesizer for VTR	ECL/I^2L	5	350	6	1000	20P4B		2—499
M54967ASP ★★	Serial Input PLL Frequency Synthesizer for VTR	ECL/I^2L	5	350	6	1000	20P4B		2—504
M54968ASP ★★	Serial Input PLL Frequency Synthesizer for VTR	ECL/I^2L	5	350	6	1000	20P4B		2—509

TUNER BAND SWITCHES

Type No.	Circuit Function	Typical Electrical Characteristics (T_a=25℃) Supply Voltage (V)	Low-level Output Current (mA)	High-level Output Current (mA)	Output Withstand Voltage (V)	Package Outline	Interchangeable products	Page
M54570L	Tuner Band Decoder/Driver	12	—	−35	24	8P5	—	2—244
M54572L	Tuner Band Decoder/Driver	12	30	−30	24	8P5	—	2—249
M54573L	Tuner Band Decoder/Driver	12	30	−30	24	8P5	—	2—251

FREQUENCY COUNTERS

Type No.	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃) Power dissipation (mW)	Receive band	Output Form	Package Outline	Interchangeable products	Page
M54820P	Frequency Counter with 5-Digit LED Driver	I^2L	200	SW	Dynamic lamp	24P4	—	2—412

CHANNEL SELECTORS

Type No.	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃) Supply Voltage (V)	Power dissipation (mW)	Low-level Input Current (mA)	Output Withstand Voltage (V)	Low-level Output Current (mA)	Package Outline	Interchangeable products	Page
M54832P	8-Channel Selector	I^2L	4.5	18	—	12	20	16P4	—	2—416
M54833P	8-Channel Selector with Clock Out	I^2L	4.5	18	—	12	20	16P4	—	2—418
M54834P	14-Channel Selector	I^2L	5	40	—	12	25	22P4	—	2—421

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FREQUENCY DIVIDER/OSCILLATORS

Type No	Circuit Function	Circuit Family	Power dissipation (mW)	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃)			Package Outline	Interchangeable products	Page
				Count Frequency (MHz)	Count	Preset Pin			
M54812L	1/4, 1/8, 1/32 Divider/Oscillator	I^2L	85*	1～4	↓	—	8P5	—	2—404
M54813L	1/4, 1/16, 1/32 Divider/Oscillator	I^2L	85*	1～4	↓	—	8P5	—	2—406
M54816P	14-Stage Divider/Oscillator	I^2L	60	0.5～4.2	↓	—	14P4	—	2—408
M54819L	Presettable Divider	I^2L	27	0～0.8	↓	Available	8P5	—	2—410

* : Max Value

↑ : Indicates the count when "Low" changes to "High" ↓ : Indicates the count when "High" changes to "Low"

LATCHED DRIVERS

Type No	Circuit Function	Supply Voltage (V)	Output Current (mA)	Output Withstand Voltage(V)	Supply Current (mA) (V_{CC}=5V, T_a=25℃)	Package Outline	Interchangeable products	Page
M54970P	9-Bit Serial-Input, Latched Divider	4.5～5.5	300	20	90	18P4	—	2—514
M54972P	Bi-CMOS 8-Bit Serial-Input, Latched Divider	4～6	300	30	6*	16P4	—	2—521
M54973P	Bi-CMOS 8-Bit Parallel-Input Latched Divider	4～6	300	30	10*	22P4	—	2—526
M54974P	Bi-CMOS 12-Bit Serial-Input, Latched Divider	4～6	400	30	10*	28P4B-A	—	2—531
M54975P	Bi-CMOS 8-Bit Serial-Input, Latched Divider	4～6	300	30	1.2*	16P4	UCN4820A	2—537
M54976P	Bi-CMOS 8-Bit Parallel-Input, Latched Divider	4～6	300	30	1.2*	22P4	UCN4801A	2—542
M54977P	Bi-CMOS 12-Bit Serial-Input, Latched Divider	4～6	200	30	1*	20P4	—	2—547

* : Per 1 Output ON

TELEPHONES

Type No	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃)				Package Outline	Interchangeable products	Page
			Power dissipation (mW)	Supply voltage (V)	Output withstand voltage(V)	Output Current (mA)			
M54193P/AP/BP	Telephone Tone Ringer	TTL	50	300	45	±5	8P4	—	2—35

TAPE CONTROLLERS

Type No	Circuit Function	Circuit Family	Typical Electrical Characteristics (T_a=25℃)				Package Outline	Interchangeable products	Page
			Supply Voltage (V)	Power dissipation (mW)	Output Withstand Voltage (V)	Output Current (mA)			
M54410P	Key Controller for Tape Deck	TTL	5	270	7	10	16P4	—	2—49
M54886P	System Controller for Tape Deck	I^2L	5	50	6	30	16P4	—	2—431
M54418P	Tape Selector	TTL	8～23	300	23	3	16P4	—	2—53

INDEX BY FUNCTION

REGISTER, LATCHES

Type No	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃)						Package Outline	Interchangeable products	Page
			Power dissipation (mW)	Shift frequency (MHz)	Clock	Set up Time (ns)	Holding Time (ns)	Transfer Time (ns)			
M54403P	5-Bit Right-Shift Left-Shift Register with Reset	TTL	510	0~10	↓	30	0	35	16P4	—	2—39

↑ : Indicates the count when "Low" changes to "High". ↓ : Indicates the count when "High" changes to "Low"

LEVEL DETECTORS

Type No.	Circuit Function	Typical Electrical Characteristics (T_a=25℃)				Package Outline	Interchangeable products	Page
		Supply Voltage (V)	Circuit current (mA)	Input Sensitivity (mV)	Output Current (mA)			
M54101P	Level Detector	12~16	9	—	40	14P4	—	2—3
M54121L	Earth Leakage Current Detector	14~18	2	20	1	8P5	—	2—7
M54122L	Earth Leakage Current Detector	12(Min)	0.4	13	0.2	8P5	—	2—11
M54123L	Earth Leakage Current Detector	12(Min)	0.4	6.1	0.2	8P5	—	2—17
M54124L	Earth Leakage Current Detector	12(Min)	0.5	6.5	0.2	8P5	—	2—23
M54125P	Earth Leakage Current Detector	12(Min)	0.7	6.5	0.2	10P2-C	—	2—29

MISCELLANEOUSS

Type No	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃)					Package Outline	Interchangeable products	Page
			Supply Voltage (V)	Power dissipation (mW)	Low-level Input Current (mA)	Output Withstand Voltage (V)	Low-level Output Current (mA)			
M54844P	8-Digit Fluorescent Display Driver For Microcomputer	I^2L	3.5~9	30	−0.2	9	10	28P4	—	2—424
M54910P	F2F Magnetic Stripe Enocording Card Reder	I^2L	4.5~9.5	100	0.1	6	16	16P4	—	2—440
M54914FP	F2F Magnetic Stripe Enocording Card Reder	Bi-CMOS	4~6	5	0.0001	5	5	20P2	—	2—447
M54801P	FM Diversity Receive Controller	I^2L	4.5~7	210	—	—	10	22P4	—	2—393

TIMER/COUNTERS

Type No.	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃)				Pacage Outline	Interchangeable products	Page
			Power dissipation (mW)	Count Frequency (MHz)	Preset range	Count range			
M54811P	Presettable Timer/Counter with 7 Segment LED Driver	I^2L	400*	0~0.1	BCD 00~99	BCD 00~99	24P4	—	2—400

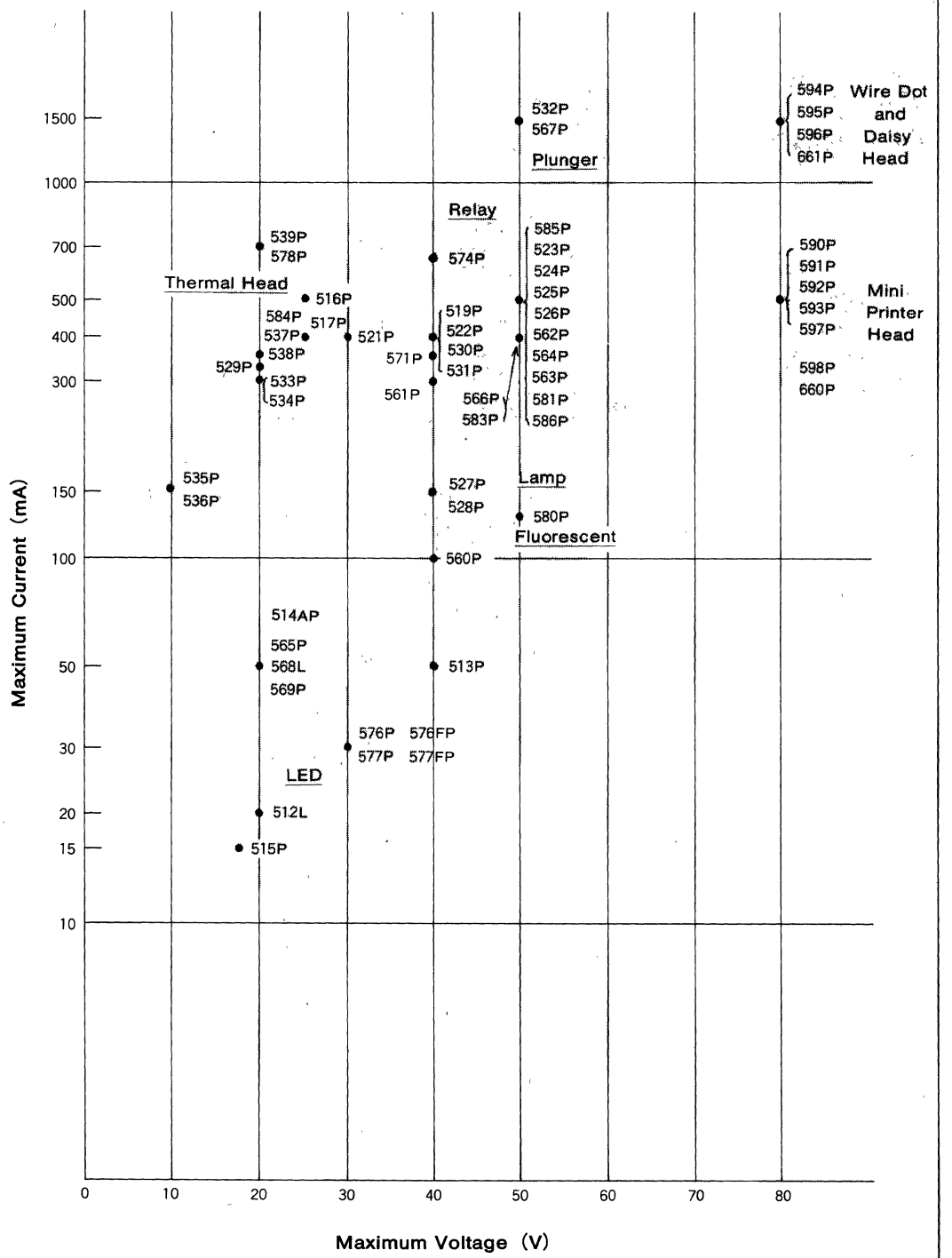
* : Worst Value

OTHERS

Type No	Circuit Function	Circuit Family	Typical Electrical Characteristics (V_{CC}=5V, T_a=25℃)					Package Outline	Interchangeable products	Page
			Supply Voltage (V)	Power dissipation (mW)	Low-level Input Current (mA)	Output Withstand Voltage (V)	Low-level Output Current (mA)			
M54610P	8-Bit Parallel Data Interface For Printer	I^2L LSTTL	5	35	−0.4	5.5	8	42P4B	—	2—332

REFERENCE BY CURRENT VS. VOLTAGE CHARACTERISTICS

REFERENCE BY CURRENT VS. VOLTAGE CHARACTERISTICS



MITSUBISHI ELECTRIC

QUICK REFERENCE

No.	I/O Type		Type Number				
	Input	Output					
1	"H" Active	Current (Sink)	4	M54512L	M54594P	M54532P	M54595P
			5	M54516P		M54521P	
				M54529P		M54529AP	
			6	M54527P		M54533P	
				M54534P		M54539P	
				M54571P		M54578P	
			7	M54514AP		M54515P	
				M54517P		M54519P	
				M54523P		M54524P	
				M54525P		M54526P	
				M54528P		M54530P	
				M54531P		M54535P	
				M54536P		M54537P	
				M54538P		M54577P	
				M54577FP			
			8	M54513P	M54522P	M54584P	M54585P
				M54590P	M54591P	M54592P	M54593P
2	"H" Active	Current (Source)	8	M54562P	M54597P	M54563P	
				M54564P	M54598P		
3	"L" Active	Current (Sink)	4	M54567P	M54596P	M54661P	M54574P
			7	M54566P	M54576P	M54576FP	
			8	M54565P		M54583P	M54575P
4	"L" Active	Current (Source)	4	M54568L			
			7	M54560P		M54561P	
				M54580P			
			8	M54569P		M54581P	
				M54586P		M54660P	

ORDERING INFORMATION

FOR MITSUBISHI ORIGINAL PRODUCTS

Example : **M 5 45 14 A P**

M : indicates the product is a Mitsubishi Electric integrated circuit.

5 : industrial/consumer
(Operating ambient temperature range is −20~+75℃, standard)

9 : High-reliability type

A single or two-digit alphanumeric code indicates circuit type and series name.

0	: CMOS
1~2	: Linear circuit
3	: TTL
10~19	: Linear circuit
20~29	: Linear circuit
32~33	: TTL (equivalent to the TI SN74 family)
41~47	: TTL and others
48~49	: IIL
84	: CMOS
85	: p-channel silicon gate MOS
86	: p-channel aluminum gate MOS
87	: n-channel silicon gate MOS
88	: p-channel aluminum gate ED-MOS
89	: COMS
S0~S2	: Schottky TTL (equivalent to the TI SN74S family)

This group consists of a two- or three-digit serial number to indicate the type of circuit within the series.

Consists of a single letter which indicates the difference of outer appearance or some part of the device specifications as listed below.

(1) For linear circuits, this is one letter of the alphabet, chosen in alphabetical order but not including I or O, which is used to flag devices for which parts of the specifications differ.

(2) For devices with identical specifications having only pin-bending direction differences, an R is assigned to this group following group (5)

(3) When this group designation is not required, the next group is shifted to the left to follow group (5) immediately.

Package style

K	: Low melting point glass sealed ceramic-type package
L, **SL**, **TL**	: Plastic molded SIP (Single In-line Package)
P, **SP**	: Plastic molded DIP (Dual In-line Package)
FP, **GP**	: Plastic molded FLAT package
S	: Metal-sealed ceramic

ORDERING INFORMATION

FOR SECOND SOURCE PRODUCTS

Example: **M 5 K 4164 S - 2**

- **M** : Mitsubishi integrated prefix
- Temperature range
  - **5** : Standard industrial/commercial (0 to 70/75℃ or −20 to 85℃)
  - **9** : High reliability
- Series designation of original source using 1 or 2 alphabetical characters.
  - **A** : Advanced Micro Devices
  - **C** : Motorola's MC series
  - **E** : Signetics
  - **F** : Fairchild
  - **G** : General Instrument's series
  - **K** : Mostek's MK series
  - **L** : Intel's series
  - **N** : National Semiconductor
  - **R** : Raytheon
  - **T** : Texas Instrument's
  - **W** : Western Digital's series
- Circuit function identification code of the original source type name.
- Package style
  - **K** : Glass-sealed ceramic
  - **P** : Molded plastic
  - **S** : Metal-sealed ceramic
- Electrical characteristic identification code using 1 or 2 digits.

PACKAGE CODE

Package style may be specified by using the following simplified alphanumeric code.

Example: **30 P 4 B**

- Number of pins
- Package structure
  - **K** : Low-melting-point glass sealed ceramic
  - **P** : Molded plastic
  - **S** : Metal-sealed ceramic
- Package outline

0 : Chip carrier	**4** : DIP/Shrink DIP	**8** : PGA
1 : DIP	**5** : SIP, ZIP	**9** : SIP
2 : SOP	**6** : QFP	

- Auxiliary outline code

SYMBOLOGY

Symbol	Parameter Definition	
BV_{CBO}	Collector-base breakdown voltage when the emitter is open	
BV_{CER}	Collector-emitter breakdown voltage when the specified resistor is connected between the base and the emitter	
BV_{CES}	Collector-emitter breakdown voltage when the base and emitter are shorted together	
BV_D	Diode breakdown voltage	The breakdown voltage of the diode
BV_{EBO}	Emitter-base breakdown voltage when the collector is open	
BV_I	Input breakdown voltage	The breakdown voltage of the input
BV_O	Output breakdown voltage	The breakdown voltage of the output
C_I	Input capacitance	Capacitance between the input and the ground terminals
C_L	Load capacitance	Externally connected load capacitance
C_O	Output capacitance	Capacitance between the output and the ground terminals
f_{max}	Maximum clock frequency	Maximum input repetition frequency for normal IC operation
F_I	Fan-in	Number of similar inputs
F_O	Fan-out	Number of similar ICs which can be driven by an output
G_V	Voltage gain	Ratio of the output voltage to extremely small changes of the input voltage
H	Indicates the high logic level	Used in voltage and current suffixes to indicate the high potential level
h_{FE}	Current amplification factor	
I	Indicates current or input	Currents flowing into ICs are taken to be positive and those flowing out as negative
I_{AS}	Total outflow current	
I_{CC}	Supply current	The current flowing into the V_{CC} supply terminal of a circuit
I_{CCL}	Low-level supply current	V_{CC} current when the inputs are such that the output is low
I_{CCH}	High-level supply current	V_{CC} current when the inputs are such that the output is high
I_F	Forward current	Forward diode current
I_I	Input current at maximum voltage	The input current flowing when maximum voltage is applied to the IC input pins
I_{IH}	High-level input current	The current flowing into an input when a specified high voltage is applied
I_{IL}	Low-level input current	The current flowing out of an input when a specified low voltage is applied
I_{OH}	High-level output current	Current flowing in the load when the output is high or current flowing when a high level is applied
I_{OL}	Low-level output current	The current flowing into an output which is in the low state
I_{OS}	Short-circuit output current	The current flowing out of an output which is in the high state when that output is short circuit to ground
I_{OZ}	Off-state output current	The current that flows when the output is in the 3-state condition
I_R	Reverse current	The current that flows when a reverse voltage is applied
I_S	Supply current	The current flowing into the IC from the V_S terminal
I_T	Threshold current	Current which lows when the threshold voltage is applied to the input
I_{T+}	Positive threshold current	Current which flows when the positive threshold voltage is applied to the input
I_{T-}	Negative threshold current	Current which flows when the negative threshold voltage is applied to the input
L	Indicates the low logic level	Used in voltage and current suffixes to indicate the low potential level
O	Indicates output	
Pd	Power dissipation	Product of the supply voltage and the supply current
PRR	Pulse repetition rate	The rate of repetition of an applied pulse train
R_I	Input resistance	The resistance expressed by V_I/I_I
r_I	Input resistance	The resistance expressed by $\Delta V_I/\Delta I_I$
T_a	Operating free-air temperature	The temperature of the environment surrounding an IC
t_f	Fall time	Time required to fall from the high to the low logic level
t_h	Hold time	The required hold time for a specified input after an input has changed
T_{opr}	Operating temperature	The ambient temperature range for normal IC operation
t_{pd}	Propagation delay time	Amount of time required from a change of input signal until the corresponding change in output, expressed as the average propagation time
t_{PHL}	Propagation delay time, high-to low-level output	Amount of time required from a change of input signal until the output changes from high to low
t_{PHZ}	Output disable time from High-level	Amount of time required from a change of input signal until the output changes from high to high-impedance
t_{PLH}	Propagation delay time low-to high-level output	Amount of time required from a change of input signal until the output changes from low to high
t_{PLZ}	Output disable time from Low level	Amount of time required from a change of input signal until the output changes from low to high-impedance
t_{PW}	Pulse width	

SYMBOLOGY

Symbol	Parameter Definition	
t_{PZH}	Output enable time to a High level	Amount of time required from a change of input signal until the output changes from high-impedance to high
t_{PZL}	Output enable time to a Low level	Amount of time required from a change of input signal until the output changes from high-impedance to low
t_r	Rise time	Time required to rise from the low to the high logic level
T_{stg}	Storage temperature	The range of surrounding stroage temparature for an IC
t_{su}	Setup time	The required hold time for other inputs before a paricular input may be changed
t_{THL}	High-to low-level output transition time	The time required for the output to change from high level to low level
t_{TLH}	Low-to high-level output transition time	The time required for the output to change from low level to high level
t_{WR}	Write recovery time	The period between the end of a write pulse and the beginning of the next cycle
V_{CC}	Supply voltage	The voltage of power supply voltage over which the device is quaranted to operate within the specified limits
V_{CE}	Collector-emitter voltage	
$V_{CE(sat)}$	Collector-emitter saturation voltage	
V_F	Forward voltage	Forwared voltage applied to a diode
V_I	Input voltage	Voltage applied to an input
V_{IC}	Input clamp diode voltage	The forward voltage applied to an input clamping diode
V_{IE}	Input emitter-emitter voltage	The emitter-to-emitter voltage for a multi-emitter transistor input
V_{IH}	High-level input voltage	The range of input voltages that represents a logic high in the system
V_{IL}	Low-level input voltage	The range of input voltages that represents a logic low in the system
V_O	Output voltage	Voltage applied to or apperaring at an output
V_{OH}	High-level output voltage	Voltage at an output in the high-state
V_{OL}	Low-level output voltage	Voltage at an output in the low state
V_{OO}	Output offset voltage	The collector-emitter voltage when the collector current is 0
V_P	Pulse amplitude	The differance between the low level and high levelof a pulse
V_R	Reverse voltage	The high voltage applied to an output
V_S	Supply voltage	The voltage applied to the V_S pin
V_T	Threshold voltage	The input voltage beyond at which the output changes
V_{T+}	Positive-going threshold voltage	The threshold voltage at which the output changes when the input is changing from low to high
V_{T-}	Negative-going threshold voltage	The threshold voltage at which the output changes when the input is changing from low to low
Z_O	Output impedance	The load impedance which should be connected to such devices as pulse generators

QUALITY ASSURANCE AND RELIABILITY

1 INTRODUCTION

IC & LSI have made rapid technical progress in electrical performances of high integration, high speed, and sophisticated functionality. And now they have got boundless wider applications in electronic systems and electrical appliances.

To meet the above trend of expanding utilization of IC & LSI, Mitsubishi considers that it is extremely important to supply stable quality and high reliable products to customers.

Mitsubishi Electric places great emphasis on quality as a basic policy "Quality First", and has striven always to improve quality and reliability.

Mitsubishi has already developed the Quality Assurance System covering design, manufacturing, inventory and delivery for IC & LSI, and has supplied highly reliable products to customers for many years. The following articles describe the Quality Assurance System and examples of reliability control for Mitsubishi Bipolar Digital ICs.

2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System places emphasis on built-in reliability in designing and built-in quality in manufacturing. The System from development to delivery is summarized in Figure 1.

2.1 Quality Assurance in Designing

The following steps are applied in designing stage for new product.

(1) Setting of perfomance, quality and reliability target for new product.
(2) Discussion of performance and quality for circuit design, device structure, process, material and package.
(3) Verification of design by CAD system to meet standardized design rule.
(4) Functional evaluation for bread-board device to confirm electrical performance.
(5) Reliability evaluation for TEG (Test Element Group) chip to detect basic failure mode and investigate failure machanism.
(6) Reliability test (In-house qualification) for new product to confirm quality and reliability target.
(7) Decision of pre-production from the standpoint of performance, reliability, production flow/conditions, production capability, delivery and etc.

2.2 Quality Assurance in Manufacturing

The quality assurance in manufacturing are performed as follows.

(1) Environment control such as temperature, humidity and dust as well as deionized water and utility gases.
(2) Maintenance and calibration control for automatized manufacturing equipments, automatic testing equipments, and measuring instruments.
(3) Material control such as silicon wafer, lead frame, packaging material, mask and chemicals.
(4) In-process inspections in wafer-fabrication, assembly and testing.
(5) 100% final inspection of electrical characteristics, visual inspection and burn-in, if necessary.
(6) Quality assurance test
-Electrical characteristics and visual inspection, lot by lot sampling
-Environment and endurance test, periodical sampling.
(7) Inventory and shipping control, such as storage environment, date code identification, handling and ESD (Electro Static Discharge) preventive procedure.

2.3 Reliability Test

To verify the reliability of a product as described in the Mitsubishi Quality Assurance System, reliability tests are performed at three different stages of new product development, pre-production, and mass-production.

At the development of new product the reliability test plan is fixed corresponding to quality and reliability target of each product, respectively. The test plan includes in-house qualification test, and TEG evaluation, if necessary. TEG chips are designed and prepared for new device structure, new process and new material.

After the proto-type product has passed the in-house qualification test, the product advances to the pre-production. In the pre-production stage. The specific reliability tests are programmed and performed again to verify the quality of pre-production product.

In the mass production, the reliability tests are performed periodically to confirm the quality of mass production product according to quality assurance test program.

Table 1 shows an example of reliability test program for plastic encapsulated IC & LSI.

Table 1 TYPICAL RELIABILITY TEST PROGRAM FOR PLASTIC ENCAPSULATED IC & LSI

Group	Test	Test condition
1	Solderability	230℃, 5sec. Rosin flux
2	Soldering heat	260℃, 10sec
	Thermal shock	−55℃, 125℃, 15cycles
	Temperature cycling	−65℃, 150℃, 100cycles
3	Lead fatigue	250gr, 90°, 2arcs
4	Shock	1500G, 0.5msec.
	Vibration	20G, 100~2000Hz X, Y, Z direction 4min./cycle, 4cycles/direction
	Constant acceleration	20000G, Y direction, 1min.
5	Operation life	T_a=Toprmax, $V_{CC} \leqq$ Vccmax 1000hours
6	High temperature storage life	T_a=150℃, 1000hours
7	High temperature and high humidity bias	85℃, 85%, 1000hours
	Pressure cooker	121℃, 100%, 100hours

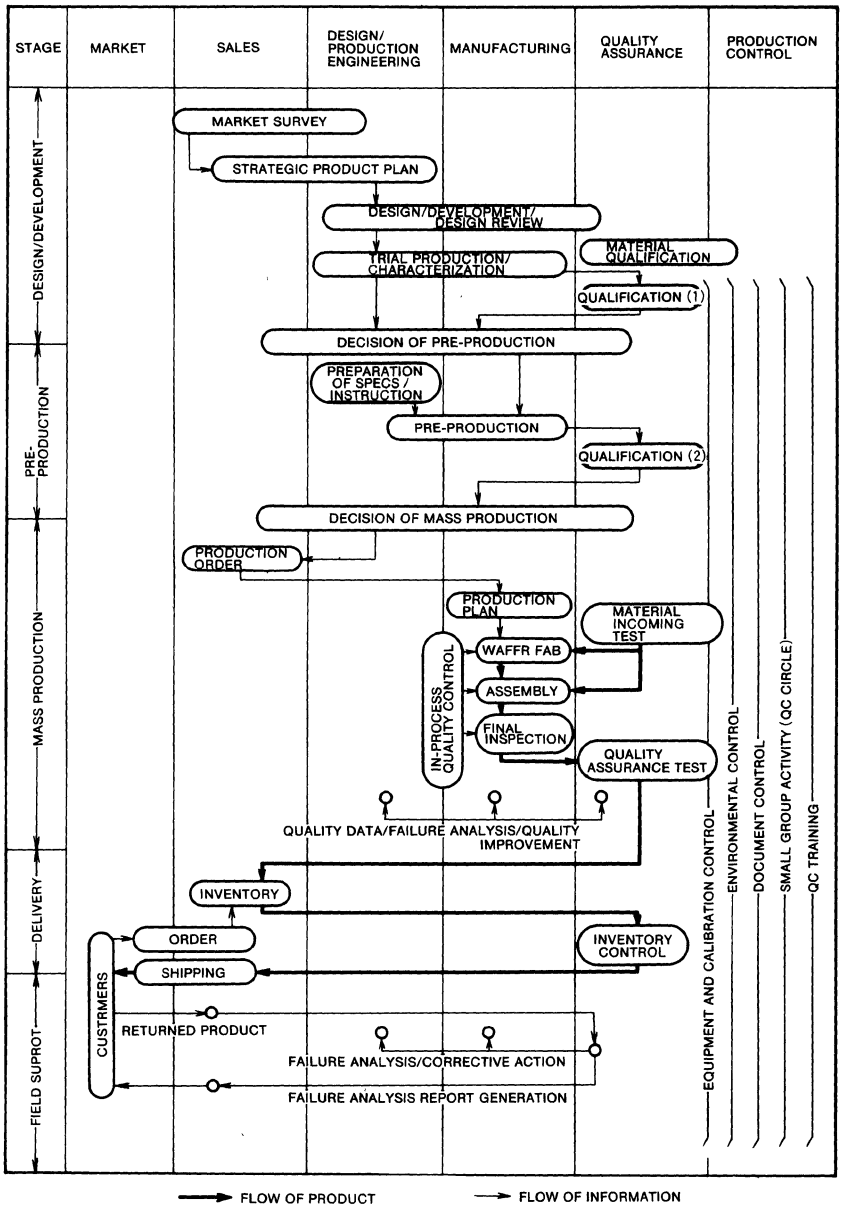


Fig.1 FLOW CHART OF QUALITY ASSURANCE SYSTEM

2.4 Returned Product Control

When failure analysis is requested by a customer, the failed devices are returned to Mitsubishi Electric via the sales office of Mitsubishi using the form of "Analysis Request of Returned Product"

Mitsubishi provides various failure analysis equipments to analyze the returned product. A failure analysis report is generated to the customer upon completion of the analysis. Failure analysis result enforces to take corrective action for the design, fabrication, assembly or testing of the product to improve reliability and realize lower failure rate.

Figure 2 shows the procedure of returned product control from customer.

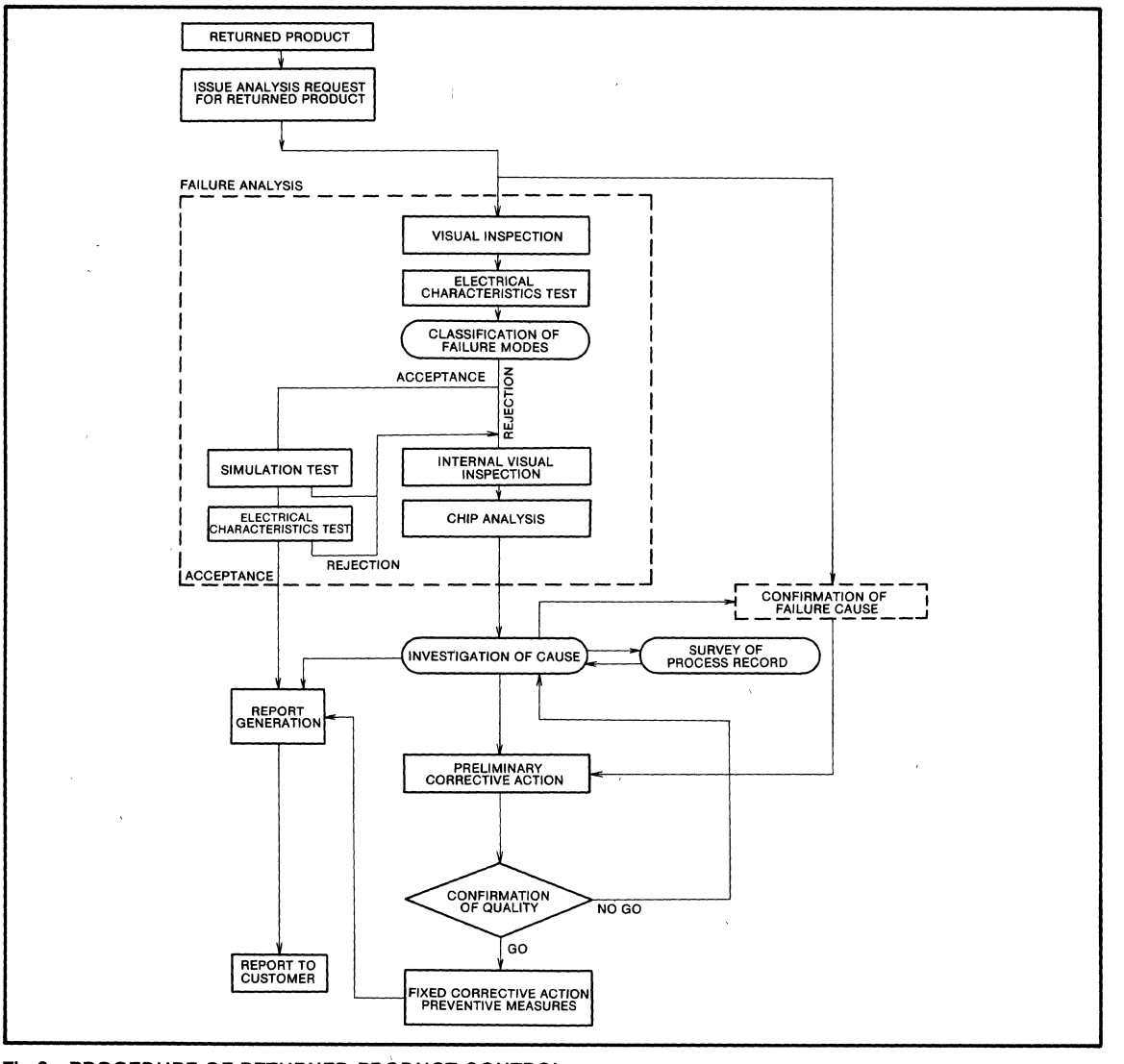


Fig.2 PROCEDURE OF RETURNED PRODUCT CONTROL

3 RELIABILITY TEST RESULTS

The reliability test results for Mitsubishi Bipolar Digital ICs are shown in Table 2, Table 3 and Table 4.

Table 2 shows the result of endurance tests of steady-state operation life and high temperature storage life test for representative types of Bipolar Digital ICs, Transistor Array, High Speed Divider, Motor Driver Peripheral Driver, Latched Driver, Programmable ROM and PLL Frequency Synthesizer. From Table 2, the combined failure rate of Mitsubishi Bipolar Digital ICs is calculated 0.070% /1000hours (60% confidence level) at maximum rating of operating condition.

Table 3 shows the result of environment test of temperature cycling, high temperature/high humidity and pressure cooker test for the same type of products as of endurance tests.

Table 4 shows the results of mechanical tests for representative products of various package types.

Table 2 ENDURANCE TEST RESULTS

Circuit Function	Type Number	Steady-State Operation Life: Test Conditions T_a(℃)	Steady-State Operation Life: Test Conditions V_{CC}/V_O(Volts)	Steady-State Operation Life: Number of Samples	Steady-State Operation Life: Device Hours	Steady-State Operation Life: Number of Failures	High Temperature Storage Life: Test Condition T_a(℃)	High Temperature Storage Life: Number of Samples	High Temperature Storage Life: Device Hours	High Temperature Storage Life: Number of Failures
Transistor Array	M54519P	75	40	40	40,000	0	150	44	44,000	0
	M54523P		50	44	88,000	0		22	22,000	0
	M54594P		80	44	88,000	0		22	22,000	0
High Speed Divider	M54473L	75	5.5	44	44,000	0	150	22	22,000	0
	M54477P			44	88,000	0		22	22,000	0
Moter Driver	M54543L	75	15	44	44,000	0	150	22	22,000	0
	M54548AL		16	44	44,000	0		22	22,000	0
Peripheral Driver	M54601P	125	5.25	38	38,000	0	150	22	22,000	0
Latched Driver	M54975P	75	6	44	44,000	0	150	22	22,000	0
	M54977P			80	160,000	0		22	22,000	0
Programmable ROM	M54700AP	125	5.25	114	342,000	0	150	22	22,000	0
	M54741AP			76	228,000	0		22	22,000	0
PLL Frequency Synthesizer	M54929P	75	5.5	44	44,000	0	150	22	22,000	0

Table 3 ENVIRONMENTAL TEST RESULTS

Application	Type Number	Soldering Heat Thermal Shock Temperature Cycling: Number of Samples	Soldering Heat Thermal Shock Temperature Cycling: Number of Cycles	Soldering Heat Thermal Shock Temperature Cycling: Number of Failures	High Temperature/High Humidity Bias: Number of Samples	High Temperature/High Humidity Bias: V_{CC}/V_O (Volts)	High Temperature/High Humidity Bias: Number of Failures	Pressure Cooker: Number of Samples	Pressure Cooker: Duration (hours)	Pressure Cooker: Number of Failures
Test Condition		260℃, 10sec −55℃, 125℃, 15cycles −65℃, 150℃, 100~300cycles			85℃, 85% 1000hours			121℃, 100%RH 240~500hours		
Transistor Array	M54519P	22	100	0	22	40	0	22	240	0
	M54523P	22	100	0	22	50	0	22	240	0
	M54594P	22	300	0	44	80	0	22	500	0
High Speed Divider	M54473L	44	300	0	22	5.5	0	22	240	0
	M54477P	22	300	0	22			44	500	0
Moter Driver	M54543L	22	100	0	22	15	0	22	240	0
	M54548AL	22	100	0	22	16	0	44	500	0
Peripheral Driver	M54601P	38	300	0	38	5.25	0	38	500	0
Latched Driver	M54975P	44	100	0	22	6	0	44	240	0
	M54977P	44	100	0	44		0	44	240	0
Programmable ROM	M54700AP	38	300	0	38	5.25	0	38	500	0
	M54741AP	38	300	0	38		0	38	500	0
PLL Frequency Synthesizer	M54929P	22	300	0	22	5.5	0	22	240	0

Table 4 MECHANICAL TEST RESULTS

Package Pin Count	Type Number	Solderability: Number of Samples	Solderability: Number of Failures	Lead Fatigue: Number of Samples	Lead Fatigue: Number of Failures	Shock Vibration Constant Acceleration: Number of Samples	Shock Vibration Constant Acceleration: Number of Failures
Test Condition		See Table 1		See Table 1		See Table 1	
8P5	M54473L	22	0	15	0	22	0
9P9	M54543L	22	0	15	0	22	0
16P4	M54519P	22	0	15	0	22	0
24P4	M54820P	22	0	15	0	22	0

4 FAILURE ANALYSIS

Accelerated reliability tests are applied to observe failures casued by temperature, voltage, humidity, current, mechanical stress and those combined stresses on chips and packages.

Examples of typical failure modes are shown below.

(1) Wire Bonding Failure by Thermal Stress

Figure 3, Figure 4 and Figure 5 are example of a failure occurred by temperature storage test of 225℃ , 1000hours.

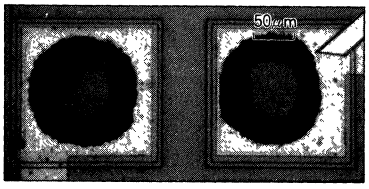


Fig.3 Micrograph of lifted Au ball trace on Al bonding pad

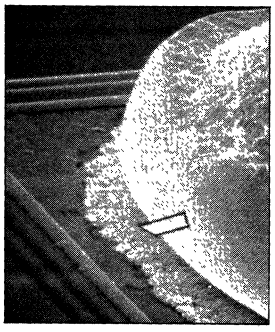


Fig.4 Au-Al plague formation on bonding pad

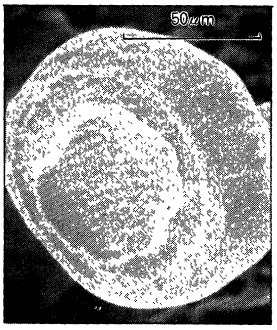


Fig.5 Lifted Au wire ball base

Au-Al intermetallic formation so-called "Purple plague" by thermal overstress makes Au wire lift off from aluminum metallization. The activation energy of this failure mode is estimated approximately 1.0eV and no failure has been observed so far in practical uses.

(2) Aluminum Corrosion Failure by Temperature/Humidity Stress.

Figure 6, Figure 7 and Figure 8 are an example of corroded failure of aluminum metallization of plastic encapsulated IC after accelerated temperature/humidity storage test (pressure cooker test) of 121℃, 100%RH, 1000hours duration.

Aluminum bonding pad is dissolved by penetrated water from plastic package, and chlorine concentration is observed on corroded aluminum bonding pad as shown in Figure 8.

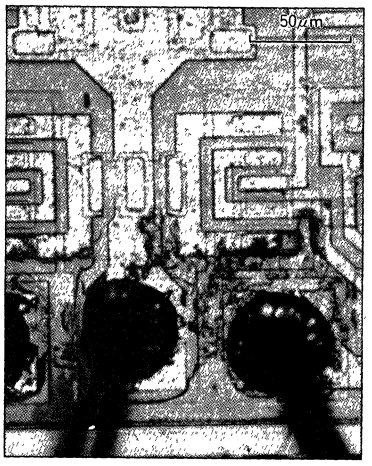


Fig.6 Micrograph of corroded Aluminum metallization

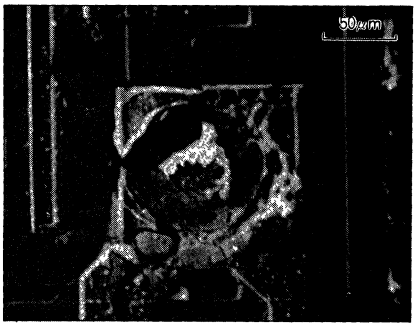


Fig.7 Enlarged micrograph of corroded Aluminum bonding pad

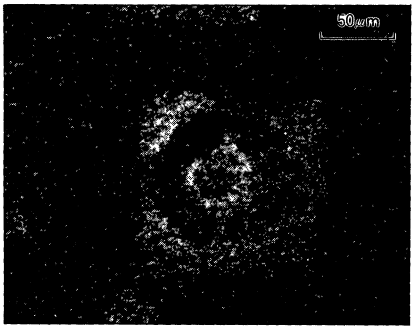


Fig.8 Cl distribution on corroded Aluminum bonding pad

(3) Destructive Failure by Electrical Overstress
Surge voltage marginal tests have been performed to reproduce the electrical overstress failure in field uses. Figure 9 and Figure 10 are an example of failure observed by surge voltage test. The trace of destruction is verified as the aluminum bridge by X ray micro analysis.

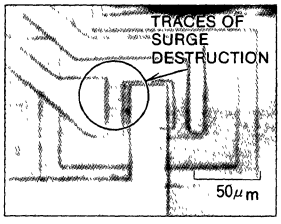


Fig.9
Micrograph of surge voltage destruction

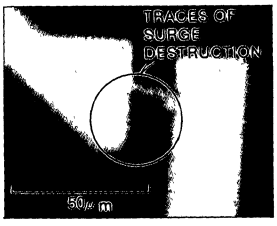


Fig.10
Aluminum trace of destructive spot

(4) Aluminum Electromigration
Figure 11 shows an open circuit of aluminum metallization in high current density region caused by accelerated operation life test. This failure is due to aluminum electromigration. Voids and hillock have been formed in aluminum metallization by high current density operation.

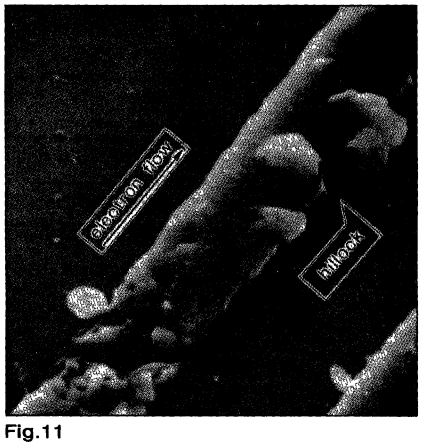


Fig.11
Voids and hillocks formation by Aluminum electromigration

5 SUMMARY

The Mitsubishi quality assurance system and examples of reliability control have been discussed. Customer's interest and requirement for high reliable IC & LSI are increasing significantly. To satisfy customer's expectancy. Mitsubishi as an IC vendor, would like to make perpetual efforts in the following areas.

(1) Emphasis on built-in reliability at design stage and reliability evaluation to investigate latent failure modes and acceleration factors.
(2) Execution of periodical endurance, environment and mechanical test to verify reliability target and realize higher reliability.
(3) Focus on development of advanced failure analysis techniques. Detail failure analysis, intensive corrective action, and quick response to customer's analysis request.
(4) Collection of customer's quality data in qualification, incoming inspection, production and field use to improve PPM, fraction defective and FIT, failure rate.

Mitsubishi would highly appreciate if the customer would provide quality and reliability data of incoming inspection or field failure rate essential to verify and improve the quality/reliability of IC & LSI.

1. INTRODUCTION

LSTTL and TTL devices are designed for low power dissipation, high speed, and a high fan-out. In addition, since the DC noise margin is large and the output impedance is low, these devices are strongly designed against AC noise on the output pins. Use of these ICs permits the construction of IC-based systems which are more effective and offer higher stability and reliability. Note that in general, ICs have a small logic amplitude and accompanying the advances in switching speed, there are problems related to noise, mounting, and wiring which have a great effect on system design. Precautions to be taken with respect to these matters are explained below.

2. TREATMENT OF ICs

2-1 Supply Voltage

The absolute maximum rating value of the supply voltage indicates the permissible value with respect to surge voltages added beyond the standard operating conditions and spike voltages generated in an excessive condition. When supply voltages above this value are continually applied, excessive current will flow due to such causes as breakdown of the internal elements of the IC. The element may generate heat and be destroyed or the internal wiring may melt, and the function of the IC cannot be guaranteed. Therefore, be sure to use supply voltages within the values designated in the recommended operating conditions (e.g., V_{CC}=5V±10% or ±5%).

2-2 Ambient Temperature

The ambient temperature is broadly classified into operating ambient temperature and storage temperature. Operating ambient temperature (T_{opr}) is generally divided into the public use field at 0 to 75℃ or −20 to +75℃ and the military use field at −55 to +125℃. Mitsubishi guarantees the electrical characteristics in the range of T_{opr}=0 to 75℃ or −20 to +75℃. Therefore, it is necessary to pay careful attention at the time of system design that use is in this range. Next, the storage temperature (T_{stg}) indicates the ambient temperature range at which changes or deterioration of characteristics does not occur when the IC is stored in a non-operating condition. Mitsubishi guarantees devices over the range of −55 to +125℃ or −65 to +150℃. These storage temperatures have been decided taking into account that the IC will be built into a machine and the conditions under which the IC will be shipped (especially air freight). Careful attention must be paid to these temperatures, since, if they are exceeded, the IC may be destroyed or its reliability may drop markedly.

2-3 Treatment Of Unused Inputs

(1) Method in which unused input pins are gathered together and connected to other driven inputs within the same gate (Fig. 1. (a))

In this case, since the inputs are always high or low level, the noise margin is not worsened and the junction capacitance between the base and emitters of the multiemitter transistor of the input acts a speed-up capacitor to provide high-speed operation. It is also good practice to make connections to nearby pins and so wiring is simple. Note that since there is an increase in the high-level output current of the output of the gate of the previous stage, it is necessary to pay attention to the fan-out of the gate of the previous stage. With the exception of this point, this is the very best method.

(2) Method in which connections are made to the IC power supply (Fig. 1 (b))

The unused inputs become completely reverse biased and this is the best method with respect to the noise margin.

In this method, the inputs connected to the power supply become grounded in terms of AC and whenever the voltage level of the drive inputs changes, the junction capacitance of the inputs connected to the power supply is charged and discharged and the operating speed is slowed down by several percent. There is also the fear of the inputs being destroyed by power supply spikes and so it is desirable to avoid using this method. However, when connections are made from the power supply to the input pins via a resistor, such connections strongly resist power supply noise for which this method is the best.

(3) Method in which connections are made to a power supply of approximately 3 to 3.5V (Fig. 1 (c))

The voltage applied to the inputs can be adjusted to the minimum necessary value, but there will still be the proiblems encountered in section (2) with respect to operating speed and wiring complexities.

(4) Method in which the input leads are left open (Fig. 1 (d) and (e))

This is the simplest method, but while the potential of the open inputs is a value close to the threshold voltage of the inpus and the base-emitter forward voltage, especially when the other driven inpus are high level, careful attention must be paid to noise on these open inputs because of the threshold potential.

When the drive inputs are kept at low level for a long period (several tens of seconds), the charge that has gathered in the capacitance of the open inputs will be discharged by the reverse-direction resistance (extremely high) of the emitter-base junction. Next, when the drive inputs have become high level, the capacitance of the open inputs becomes high level while charging and as a result, the operating speed is slowed down somewhat. One practice that should be avoided is leaving the unused inputs (including the set/reset pins of flip-flops) in a wired condition without applying a determined voltage since the wiring will act as an antenna and the inputs will be susceptible to even small amounts of noise as a result.

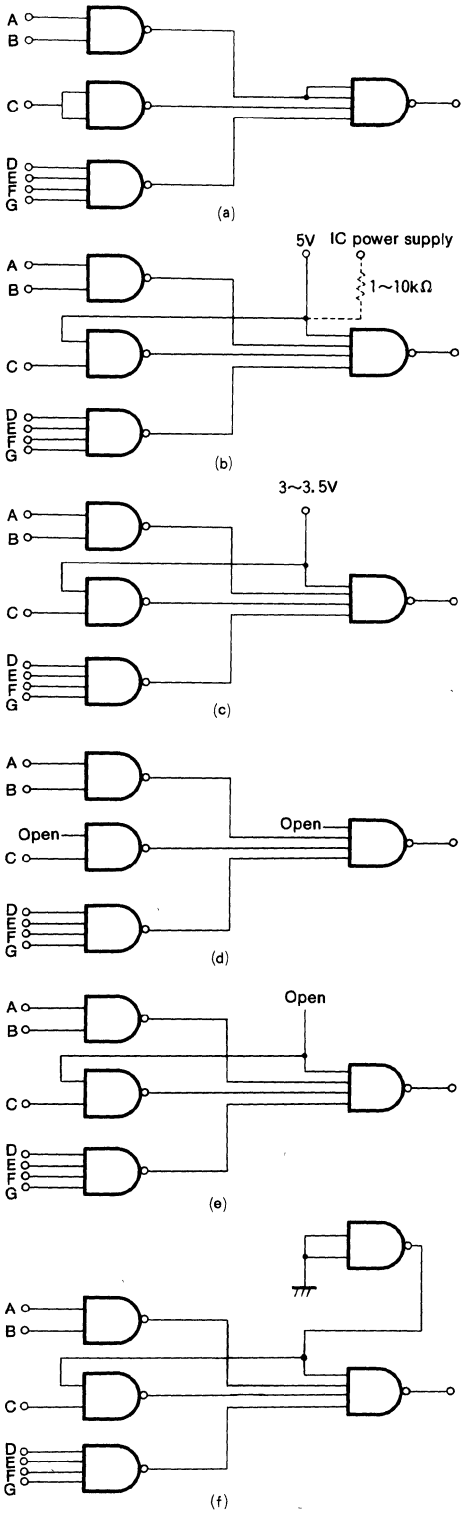


Fig.1 Methods of Processing Input Pins

(5) Method in which connections are made to the output pin of the gate (Fig. 1 (f))

In this method, when using one NAND gate for example, the gate input is grounded and the output is always maintained at high level; this output pin is connected to the unused input pins. In this instance, output voltage V_{OH} is about 2.4 to 3.5V in normal TTL, a value which is lower than the power supply value of section (2) above. Incomparison with section (2), the accumulated charge in the input capacitance is held to a minimum, and the switching characteristics and noise margin will be under the same conditions as the input pins used in the basic gate. There will not be the problem of the absolute maximum rating value of the input voltage (5.5V for TTL) which occurred section (2), and excepting the wiring complexities and the requirement of extra ICs, this is the best method.

2-4 Abnormal Oscillations

This oscillation phenomenon is often seen in ICs with current sources. For example, when an input waveform with a rise time of over 1 us is input to the gate, the output undergoes an oscillation of several tens of MHz. When the rise time is slow, this oscillation occurs because of the long input application time in the vicinity of the threshold voltage. To prevent this oscillation, set the rise (fall) time of the input waveform to less than 1 us. Furthermore, it is necessary to insert a waveform shaping circuit to the input and correct the rise (fall) time.

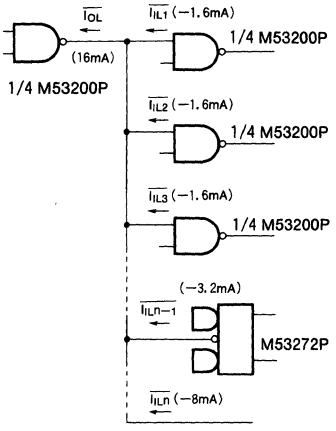
2-5 The Problem Of Output Load Capacitance

Induction noise on the transmission line is generally removed by inserting a capacitor at the output of the IC or between the transmission line and ground. This capacitor is charged when the output is high level and is discharged through the output transistor when the output is low level. Note that when the capacitor is very large, excessive current will flow momentarily and cause deterioration of the IC. The selection of this capacitor does have a relationship with the period of the output of the IC, but in general a value of less than 0.1μF is used. A commonly used method for preventing the deteriorization of the IC is to insert a small (protection) resistor in series between the output and the capacitor.

2-6 Relationship Between The Clock And The Data

The relationship between the trigger time of the clock input and the data is specified for flip-flops or counters and shift registers made up of flip-flops. That is, the setup time (t_{su}) and the hold time (t_h) are shown in the recommended operating conditions. Attention must be paid to these variables since erroneous operation will occur if the IC is used outside of this range.

When the output level of the driver is "L"



16−(1.6+1.6+1.6+3.2)=8mA drivable

Drivable Conditions

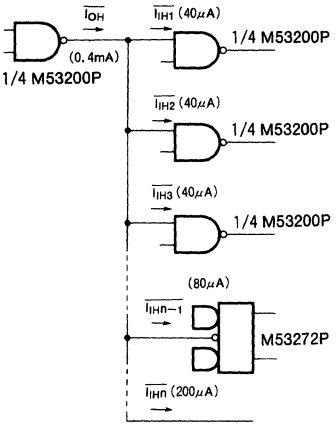
1. When the input currents of each of the load circuits differ

$$|\overline{I_{OL}}| \geqq \sum_{i=1}^{n} |\overline{I_{IL1}}| \quad (1)$$

2. When the input currents of each of the load circuits is the same

$$|\overline{I_{OL}}| \geqq F_O |\overline{I_{IL}}| \quad (3)$$

When the output level of the driver is "H"



400−(40+40+40+80)=200μA drivable

Drivable Conditions

1. When the input currents of each of the load circuits differ

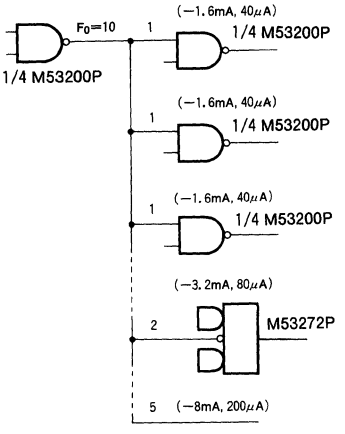
$$|\overline{I_{OL}}| \geqq \sum_{i=1}^{n} |\overline{I_{IH1}}| \quad (2)$$

2. When the input currents of each of the load circuits is the same

$$|\overline{I_{OH}}| \geqq F_O |\overline{I_{IH}}| \quad (4)$$

Fig.2 Calculation of the Number of Loads by Input/Output Currents

When the output level of the driver is "L"



10−(1+1+1+2)=5 drisable

Drivable Conditions

$F_O \geqq$ Total sum of the input load coefficients (5)

Fig.3 Calculation of the Number of Loads by Input Load Coefficients

3. PRECAUTIONS TO BE TAKEN FOR SYSTEM DESIGN

3-1 Method Of Calculating Fan-out

The number of loads that can be driven by the circuit are within the specified value range of the circuit output voltage, V_{OL} and V_{OH}, and are found from the relationship between the output current of the drive circuit, I_{OL} and I_{OH}, and the input current of the load circuit, I_{IL} and I_{IH}. The value can be found from the relationship formulae shown in formula (1) and formula (2), and if the number of loads within this range is satisfactory based on these formulae, driving of the ICs is possible. (See Fig. 2.)

$|\overline{I_{OL}}| \geqq \sum_{i=1}^{n} |\overline{I_{IH1}}|$ (When the output level of the drive circuit is low level) ·····(1)

$|\overline{I_{OH}}| \geqq \sum_{i=1}^{n} |\overline{I_{IH1}}|$ (When the output level of the drive circuit is high level) ·····(2)

Here, if the load circuits are all identical circuits or they have the same input current characteristics, and the number of loads is defined as F_{OH} when the output is high level and as F_{OL} when the output is low level, formula (1) and formula (2) will be as follows:

$|I_{OL}| \geqq F_{OL} |I_{IL}|$ ·····(3)

$|I_{OH}| \geqq F_{OH} |I_{IH}|$ ·····(4)

F_{OL} and F_{OH} each have equivalent cases as well as differences. Generally, in terms of system design, the worst-case value is used for the number of fan-outs F_O. In this way, when the input currents of each of the load circuits are the same, the number of loads can be easily found from formula (3) and formula (4). In actuality, there are a large number of cases where the input currents differ depending on the circuit, and the calculation of the number of loads must be found from formula (1) and formula (2) and becomes extermely complex.

In the M53200P series, input load coefficients and fan-out F_O values are used so that such complex circuit connection relationships can be hadled simply. As a result, the calculation of the number of loads has been greatly simplified by only performing addition and subtraction of the input load coefficients and the fan-out F_O as shown in Fig. 3.

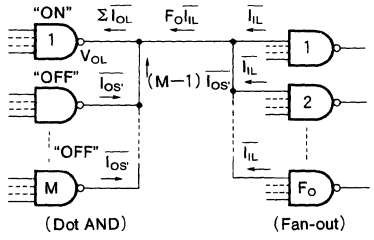
The input load coefficient may be described by setting the maximum value of the basic input current of the basic gate circuit to 1 and comparing the maximum value of the input current of the other circuits such as flip-flops. This value expresses the number of input loads of the circuit. In the case where the fan-out F_O drives circuits of input load coefficient 1, the number of circuits that can be driven is indicated and the value has the same significance as the F_O mentioned in formula (3) and formula (4).

In the case of the TTL M53200P series, the basic currnet is $I_{IL} = -1.6$mA and $I_{IH} = 40\mu$A, which is set as input load coefficient 1.

3-2 And Ties

In this instnace, the output pins of the circuits are simply connected together and the operation of the AND function can be accomplished. This type of connection is called a "wired AND", "dot AND," or "AND tie."

When making AND ties, attention should be paid to the following matters as explained in the example of Fig. 4. From among the several AND-tied (M) circuits, when only one of the circuits is in the "ON" state (output low level) and the remaining circuits are all in the "OFF" state (output high level), (in terms of AND tie circuit function this combination is the worst-case conditin for a circuit in the "ON" state) current will flow into the output pin of this circuit in the "ON" state. The currents that flow will not only be input current $F_O \cdot \overline{I_{IL}}$ of the fan-out F_O section connected as a load, but also the total sum $(M-1) \cdot \overline{I_{OS'}}$ of currents $\overline{I_{OS'}}$ close to each of output short currents $\overline{I_{OS}}$ from all circuits (M-1) that are in the "OFF" state from among the circuits connected as an AND tie.



From the diagram $\Sigma\overline{I_{OL}}=(M-1)\cdot\overline{I_{OS'}}+F_O\cdot\overline{I_{IL}}$

From the specifications $\Sigma\overline{I_{OL}}\leqq\overline{I_{OL}}$

Therefore $F_O\leqq\dfrac{\overline{I_{OL}}-(M-1)\cdot\overline{I_{OS'}}}{\overline{I_{IL}}}$

Here $\overline{I_{OS'}}=\dfrac{\overline{V_{CC}}-\overline{V_{OL}}}{R_C}$

Fig.4 Relationship Between AND Tie Connections Fan-outs

Because of this the load currents $\overline{I_{OL}}$ of the AND-tied circuit will become a current greater than the specified value. $\overline{I_{OL}}$ is expressed in calculation formla (5).

$$\Sigma\overline{I_{OL}}=(M-1)\cdot\overline{I_{OS'}}+F_O\cdot I_{IL} \quad \cdots\cdots(5)$$

When finding from this formula the number of fan-outs F_O that can be driven in the case of AND ties, it is necessary that $\overline{I_{OL}}$ is smaller than the specified value $\overline{I_{OL}}$ and so we get.

$$\Sigma\overline{I_{OL}}\leqq\overline{I_{OL}} \quad \cdots\cdots(6)$$

and from formula (5) and formula (6) we get

$$F_O\leqq\frac{\overline{I_{OL}}-(M-1)\cdot\overline{I_{OS'}}}{I_{IL}} \quad \cdots\cdots(7)$$

However, $\overline{I_{OS'}}=\dfrac{\overline{V_{CC}}-\overline{V_{OL}}}{R_C}$

which is smaller than the general fan-out $F_O\leqq I_{OL}/I_{IL}$.

Accordingly, in the case of making AND ties, it is necessary to use reduced number of fan-outs from the AND ties. In addition, when all of the AND-tied circuits are in the "OFF" state, the collector load resistors R_C of the circuits will be in a parallel condition and the combined resistance will be 1/M. This has the role of pulling up output voltage V_{OH}; however, examination of the "OFF" state is not necessry.

3-3 Selection Of Load Resistors For And Ties

When using AND-tied open collector gates or when using the collector gates independently, the maximum load resistance ($R_{L(max)}$) and the minimum load resistance ($R_{L(min)}$) is found in order to guarantee the fan-out and values are taken from within this range. The general formula used to find R_L is shown below:

$$R_L=\frac{V_{RL}}{I_{RL}}$$

provided that V_{RL} is the voltage drop across R_L Unit (V) and I_{RL} is the currnet flowing through R_L Unit (A)

The maximum load resistance ($R_{L(max)}$) is found when the outputs are all in the high-level state. For example, when the number of fan-outs is expressed as M and the number making up AND ties is expressed as N, (Fig. 5)

$V_{RL}=V_{CC}-V_{OH}$

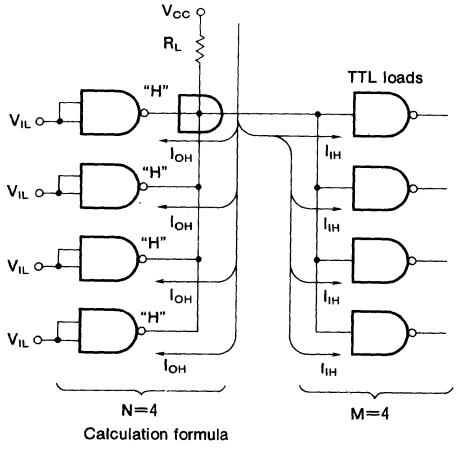
and according to $I_{RL}=M\cdot I_{IH}+N\cdot I_{OH}$

$$R_{L(max)}=\frac{V_{CC}-V_{OH}}{M\cdot I_{IH}+N\cdot I_{OH}}$$

The minimum load resistance ($R_{L(min)}$) is found when one of the outputs is in the low-level state and is expressed by the following formula:

$$R_{L(min)}=\frac{V_{CC}-V_{OL}}{I_{OL(max)}-N\cdot|I_{IL}|}$$

Table 1 is compounded from these formulae.



Calculation formula

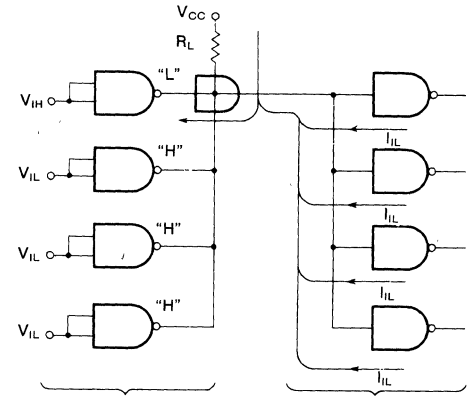
$$R_{L(max)}=\frac{V_{CC}-V_{OH}}{M\cdot I_{IH}+N\cdot I_{OH}}$$

Example $V_{CC}=5V$, M=4, N=4

When $I_{OH}=250\mu A$, $I_{IH}=40\mu A$

$$R_{L(max)}=\frac{5-2.4}{0.00016+0.001}=2241\,\Omega$$

Fig.5 Worst-case Conditions for Finding $R_{L(max)}$



Calculation formula

$$R_{L(min)}=\frac{V_{CC}-V_{OL}}{I_{OL(max)}-M\cdot|I_{IL}|}$$

Example V_{CC}=5V, M=4, $I_{OL(max)}$=16mA

When I_{OL}=1.6mA

$$R_{L(min)}=\frac{5-2.4}{0.0016+0.0064}=479\Omega$$

Fig.6 Worst-case Conditionp for Finding $R_{L(min)}$

4. PROBLEMS RELATED TO MOUNTING AND WIRING

4-1 Oscillations Due To Wiring Impedance

This oscillation phenomenon is caused by the oscillation due to the slow rise (fall) time of the input voltage mentioned in section 2-4. Approximately $I_{OS}/2$ flows in the output, and a loop can be made via the base resistor of the input transistor of the IC by means of voltage fluctuations from the power supply and the wiring impedance. This is how the oscillation is formed. The oscillation frequency at this time is about 25 to 50MHz. A preventive method is to be cautious of the voltage fluctuations from the common impedance of the power supply and insert a bypass capacitor at the card unit so that the oscillation can be reduced.

4-2 Crosstalk Between Lines

When using single wires and twisted wires in the transmission line, crosstalk is roughly proportional to line length for each kind of wire up to line lengths of about 1m and induction noise will increase. In this range, reducing the capacitance between the signal line and the noise line will prevent the crosstalk. Compared to single wires, twisted wires reduce the induction noise voltage to about one half value. When line lengths exceed 1m, lines other than twisted lines will become saturated. Especially when single lines become longer than 2m, positive pulses of 4V are superposed on the high level. Caution is required in this regard since there is a greater possiblity of destroying the input section of the IC.

4-3 Wiring Precautions

One of the first precautions in wiring design is to insert a ground line between signal line and signal line and it is effective to establish a large ground line on one side. Also, the basics of wiring is to have narrow print strips, wide intervals, and short line lengths.

4-3-1 Supply Voltage

The supply vlotage is within the range of $V_{CC}=5V\pm5\%$ designated in the recommended operating conditions and the power supply fluctuation rate and ripple are low.

Especially when using high-speen TTL, noise is generated by current spike voltage and since the capacitance of the power supply is increased, it is necessary to lower the impedance of the power supply and supply line.

The measures to be taken of course deal with the power supply itself. Insert steel titanate type capacitors (0.01 to 0.1μF) having excellent high-frequency characteristics between the supply line and ground at suitable intervals (5 to 10 packages of IC) and lower the impedance with respect to high frequencies.

4-3-2 Ground Line

Noise is generated by the common impedance of the ground line, and when the ground line is grounded at a multiple points, voltage is induced by the external electromagnetic field and there are many such cases where this leads to noise. Measures to be taken for the ground line are to use an exclusive ground plate and to completely separate it from the grounds of other power systems and electronic device systems. In addition, reduce the impedance of the ground line, and use a one-circuit one-ground system for the ground lines of each of the circuits.

4-4 Rationalization Of Transmission Impedance

Generally, a value of about 50 ohms is appropriate, but when there is a lot of electromagnetic induction, it is desirable to transmit at high level even though the impedance may become a little high.

4-5 Measures Against External Noise Interference

4-5-1 Noise Due to Electromagnetic Induction

This noise occurs when a magnetic field generated by current flowing in a noise-generatig circuit crosses a signal circuit. Measures that may be taken:

(1) Twist together the return wires of the circuit that is the souce of noise and cancel the magetic field being generated.
(2) Twist together the return wires of the signal circuit and induce the voltages in the same direction to cause cancellation.
(3) Increase the distance between the noise-generating circuit and the signal circuit.
(4) Establish a suitable magnetic shield between the two circuits.
(5) Shorten the length of interfering wiring.

4-5-2 Noise Due to Static Induction

This noise is generated when the noise-generating cirucit and the signal are separated by some induction material and the voltage levels differ. Measures to be taken:

(1) Increase the distance between the wires.
(2) Reduce the dialectric constant between the wires.
(3) Reduce the diameter and length of the wires.
(4) Reduce the potential difference between the wires.
(5) Establish a static shield.

4-5-3 Noise Due to Common Impedance

When the signal circuit and the circuit of the source of noise are joined by the common impedance of the ground line, a voltage is generated in the ground line by the current flowing in the noise source and this becomes the noise signal. In addition, when the ground line is grounded at multiple points, a closed circuit is formed mutually between the ground lines, and when a voltage is induced within this loop by the changes in the external magnetic field, this voltage may become the noise signal. Measures to be taken include:

(1) Completely separate the grounding system of the signal circuit from the power line grounding system of other electrical devices.
(2) Reduce the impedance of the ground line.
(3) Use the one-circuit one-ground method for the ground lines of each of the circuits.

Table 1 Selection of Load Resistors for AND Tie Connections

(V_{CC}=5V) (Unit : Ω)

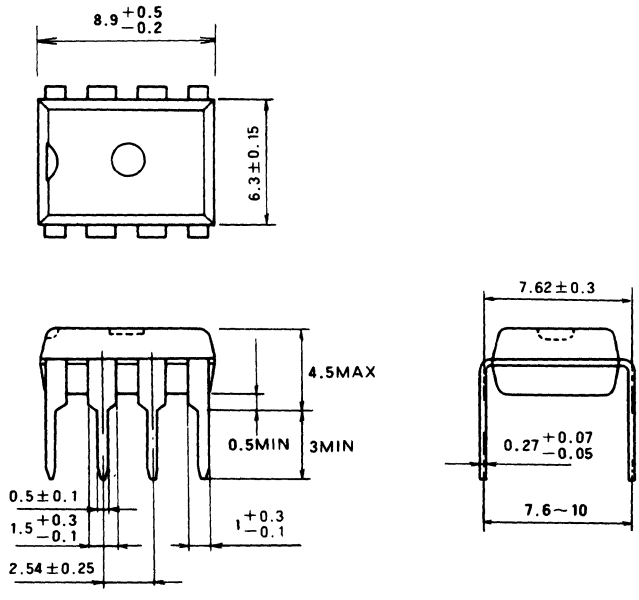
Fan-out number (M)	Number of AND tie outputs (N)							
	1	2	3	4	5	6	7	1~7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	×	×	1437
9	4262	3023	×	×	×	×	×	2875
10	4000	×	×	×	×	×	×	4000*
	R_L(max)							R_L(min)

× : Avoid this combination
* : When M=10, R_L(min)=∞, but R_L=4000Ω is recommended for reason of guaranteeing the high level, etc

PACKAGE OUTLINES

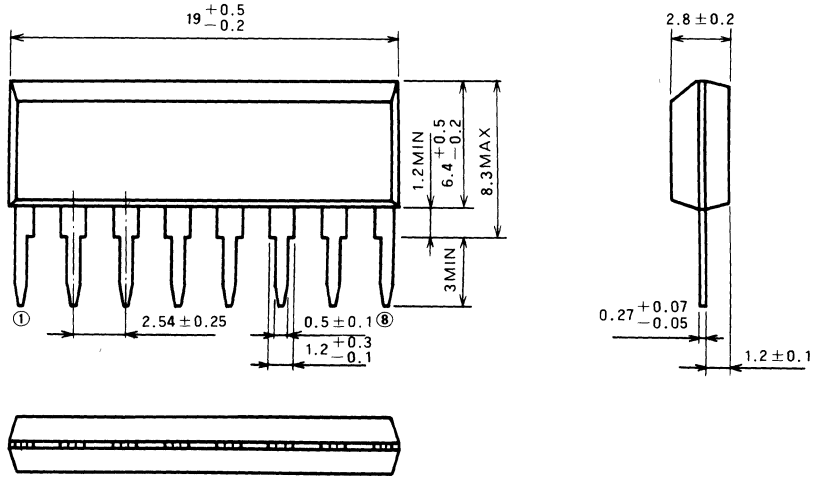
TYPE 8P4 8-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 8P5 8-PIN MOLDED PLASTIC SIP

Dimension in mm

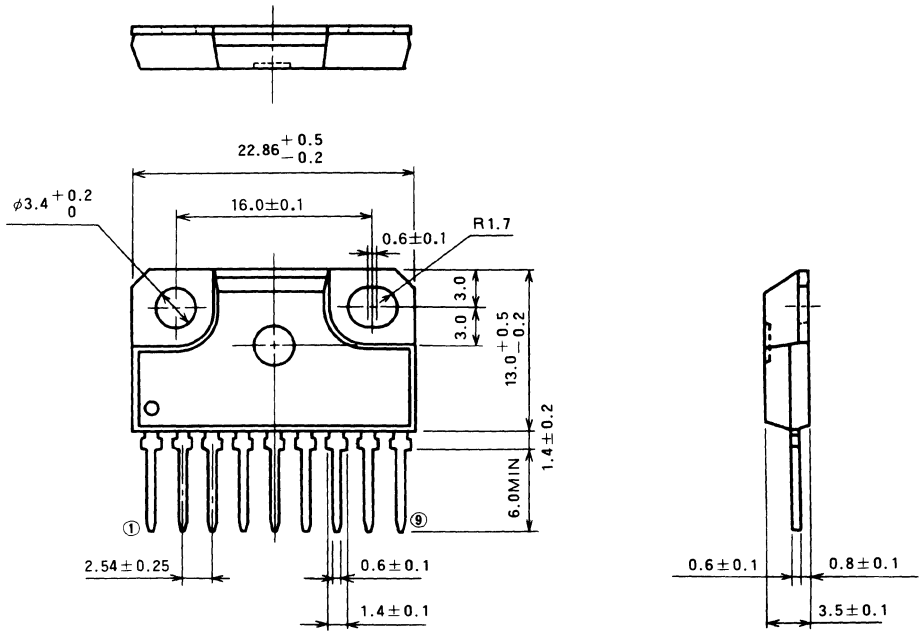


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

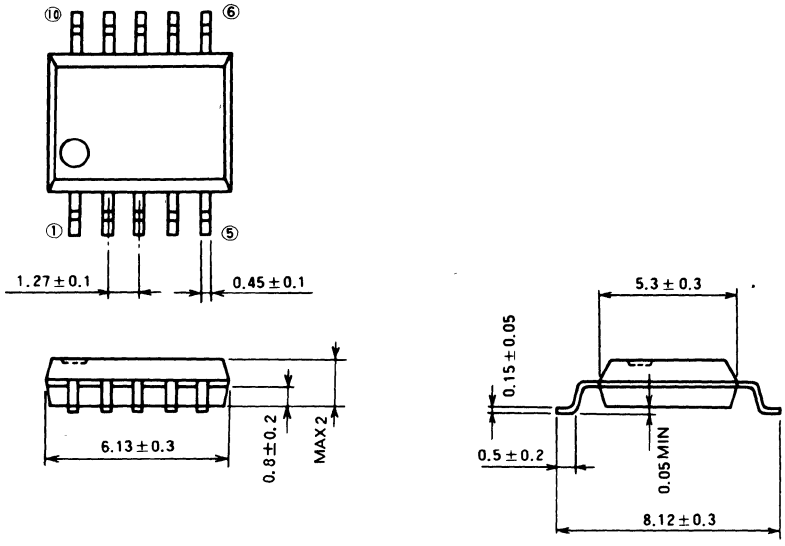
TYPE 9P9 9-PIN MOLDED PLASTIC SIP

Dimension in mm



TYPE 10P2-C 10-PIN MOLDED PLASTIC FLAT

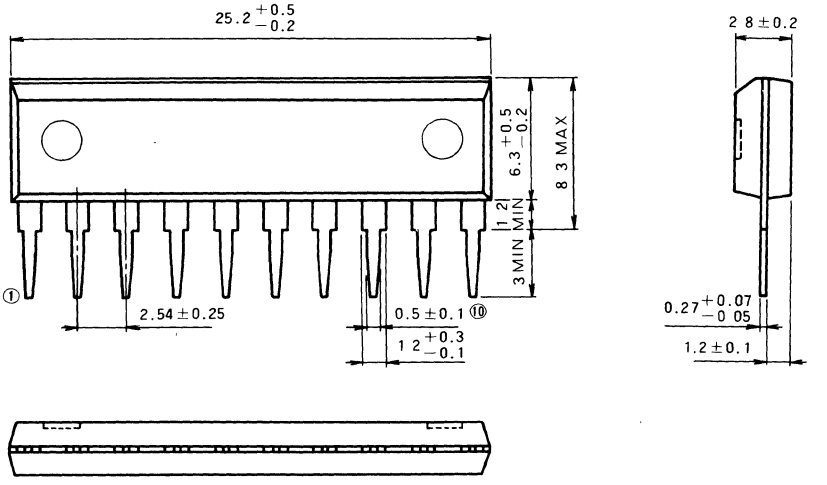
Dimension in mm



PACKAGE OUTLINES

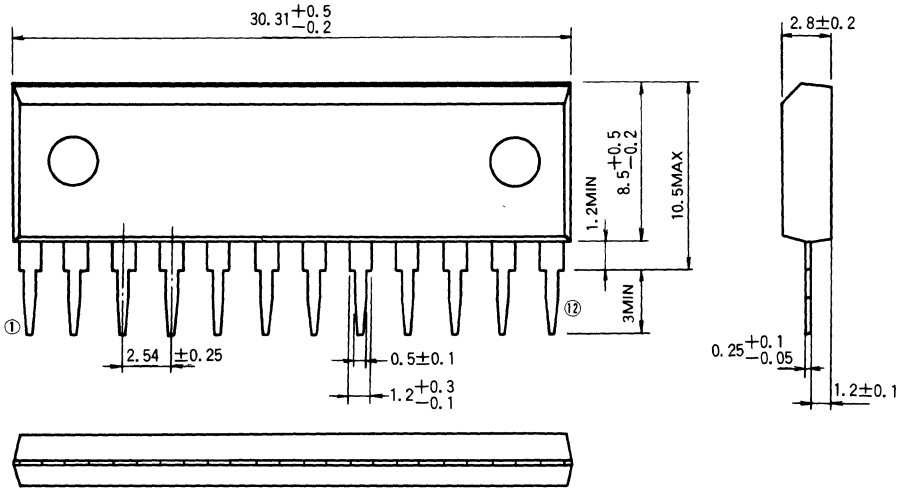
TYPE 10P5 10-PIN MOLDED PLASTIC SIP

Dimension in mm



TYPE 12P5 12-PIN MOLDED PLASTIC SIP

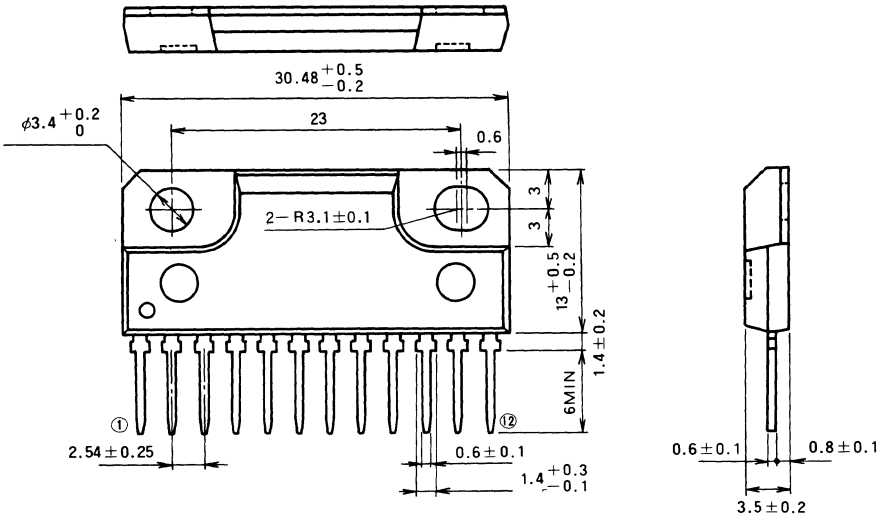
Dimension in mm



MITSUBISHI ELECTRIC

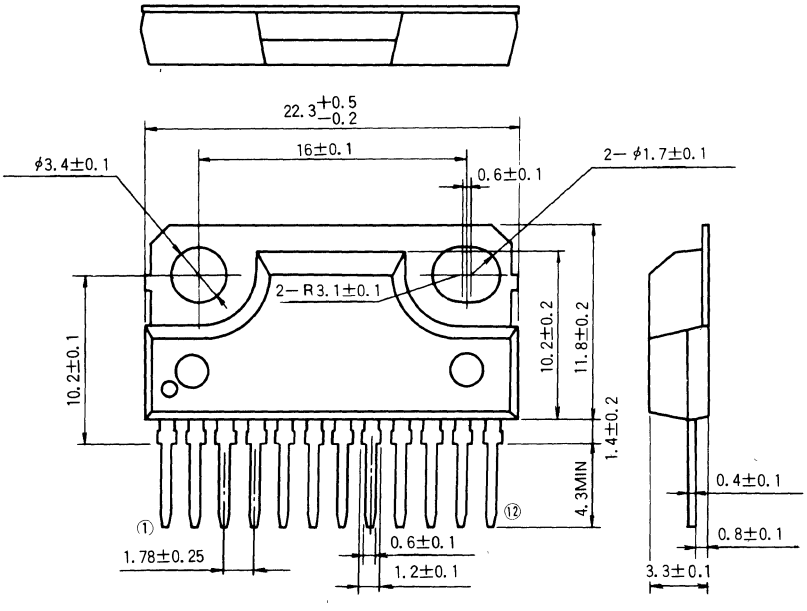
TYPE 12P9 12-PIN MOLDED PLASTIC SIP

Dimension in mm



TYPE 12P9B 12-PIN MOLDED PLASTIC SIP(SHRINK)

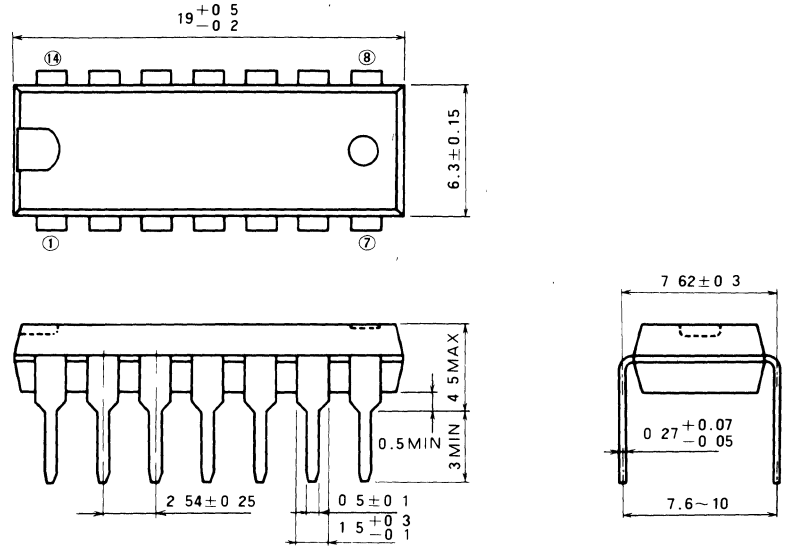
Dimension in mm



PACKAGE OUTLINES

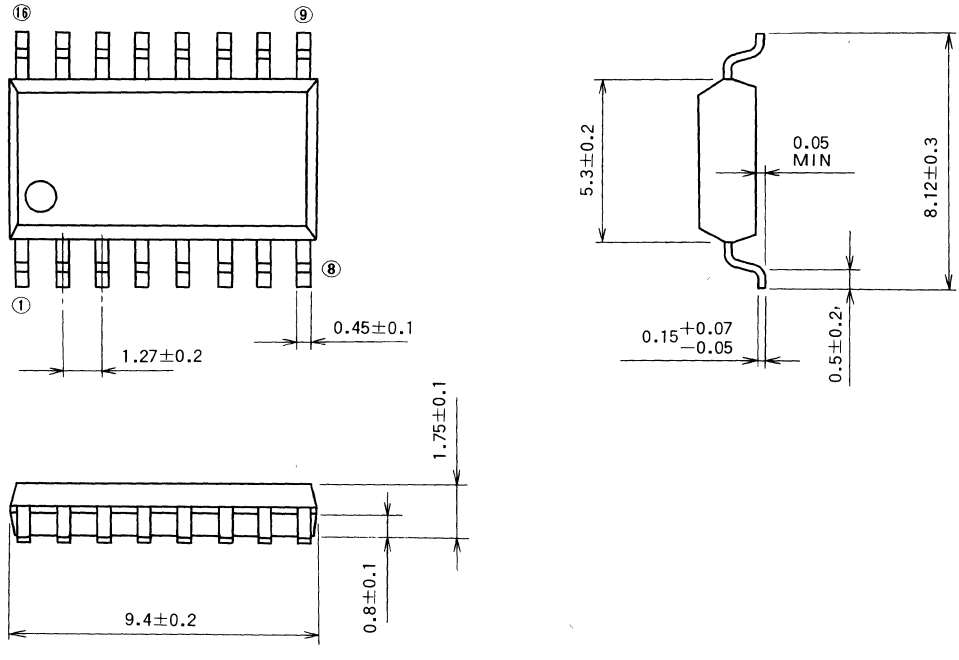
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P2 16-PIN MOLDED PLASTIC FLAT

Dimension in mm

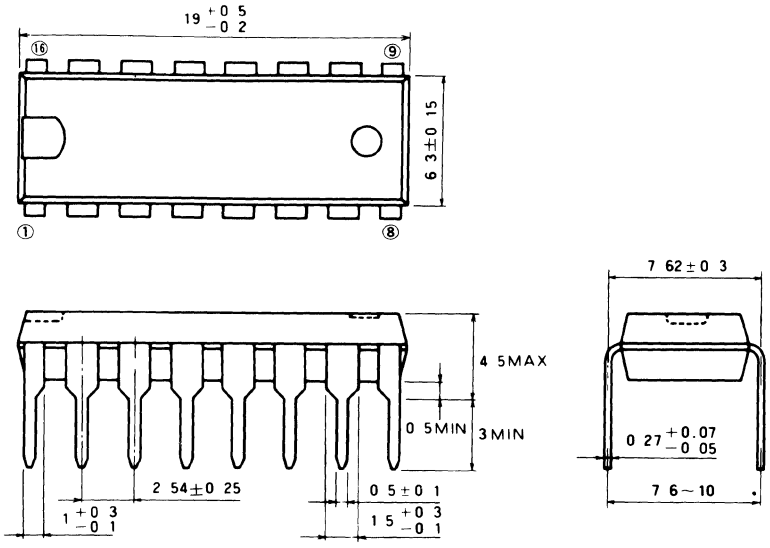


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

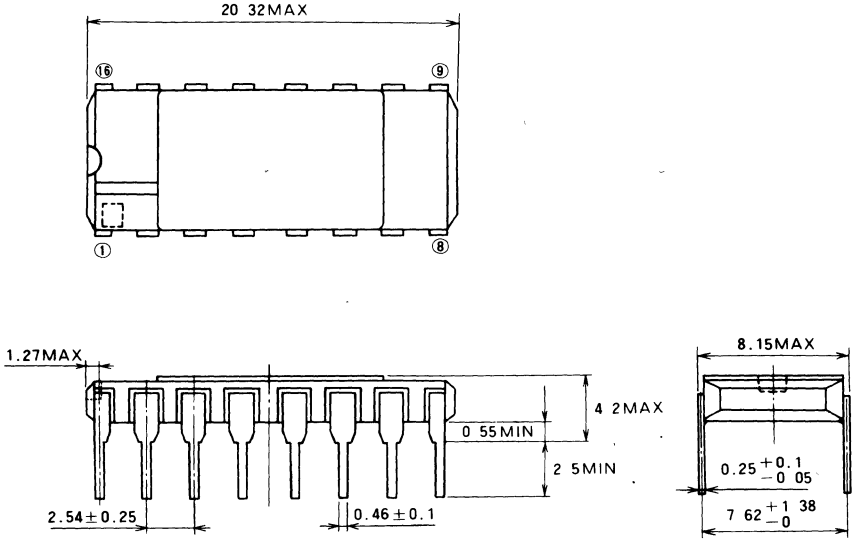
TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16S1 16-PIN METAL-SEALED CERAMIC DIP

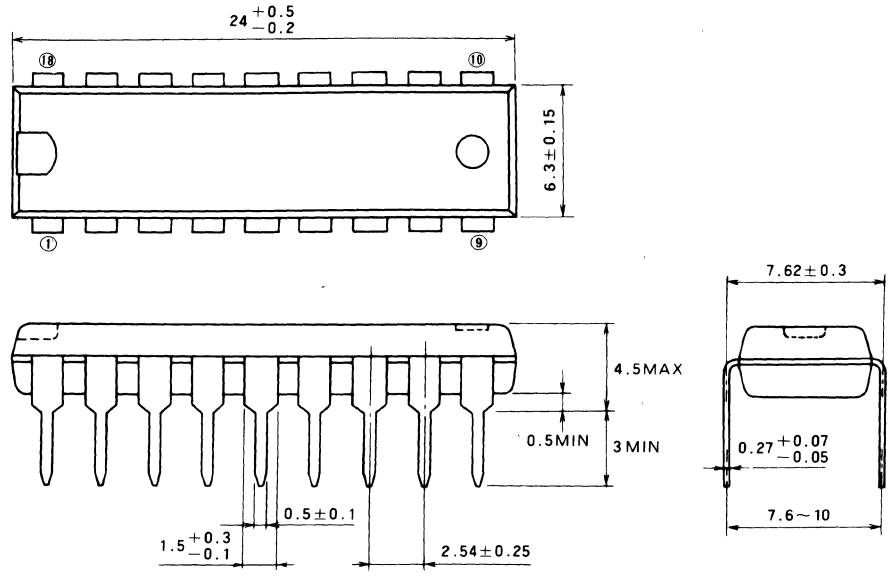
Dimension in mm



PACKAGE OUTLINES

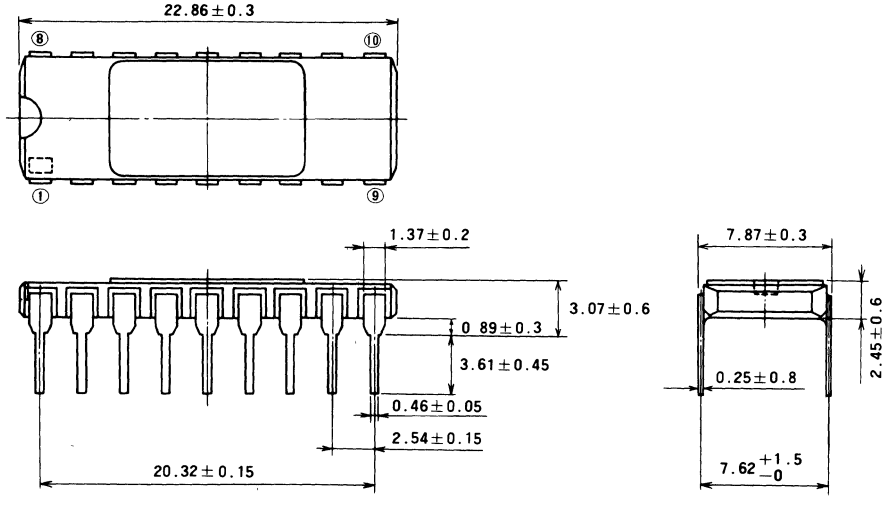
TYPE 18P4 18-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 18S1 18-PIN METAL-SEALED CERAMIC DIP

Dimension in mm

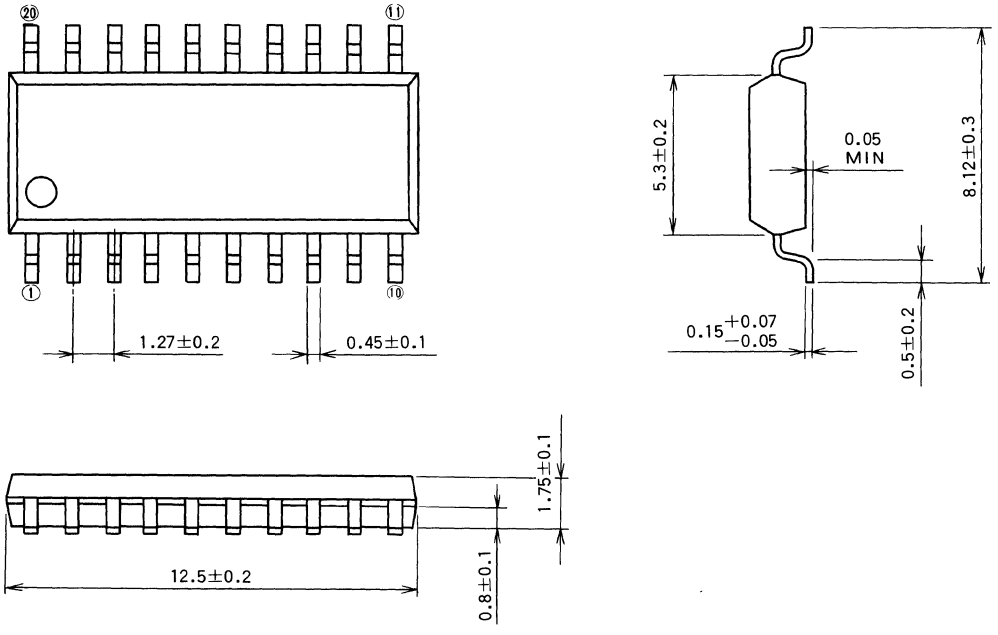


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

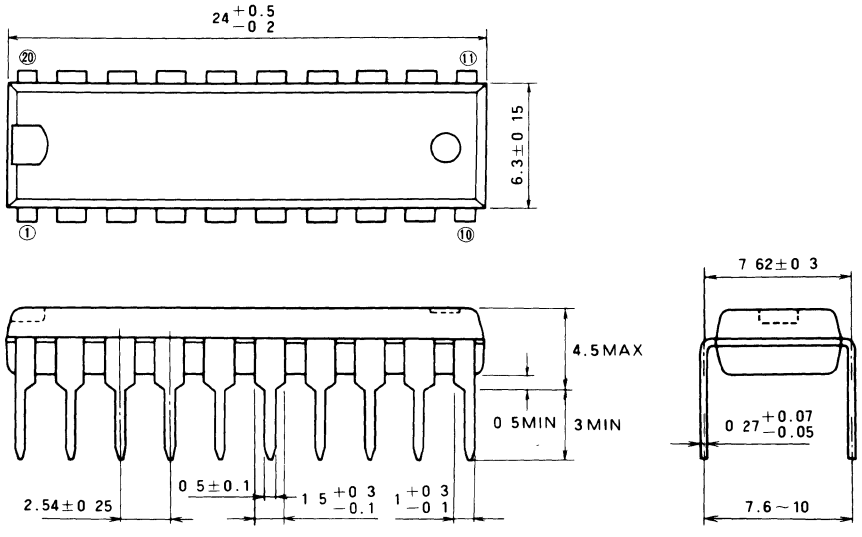
TYPE 20P2 20-PIN MOLDED PLASTIC FLAT

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIP

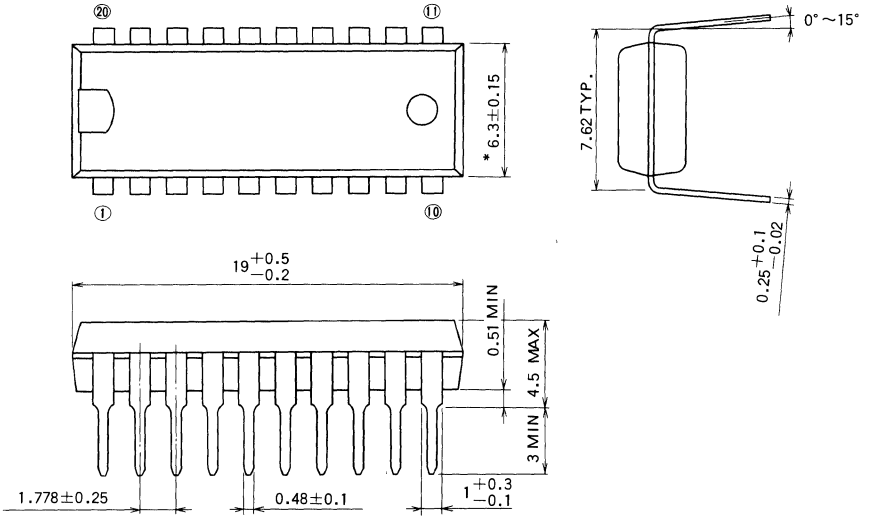
Dimension in mm



PACKAGE OUTLINES

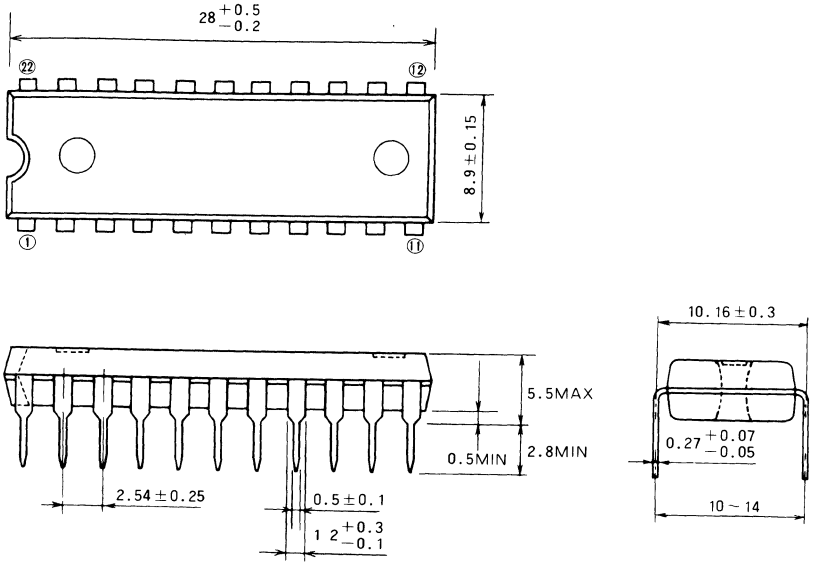
TYPE 20P4B 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 22P4 22-PIN MOLDED PLASTIC DIP

Dimension in mm

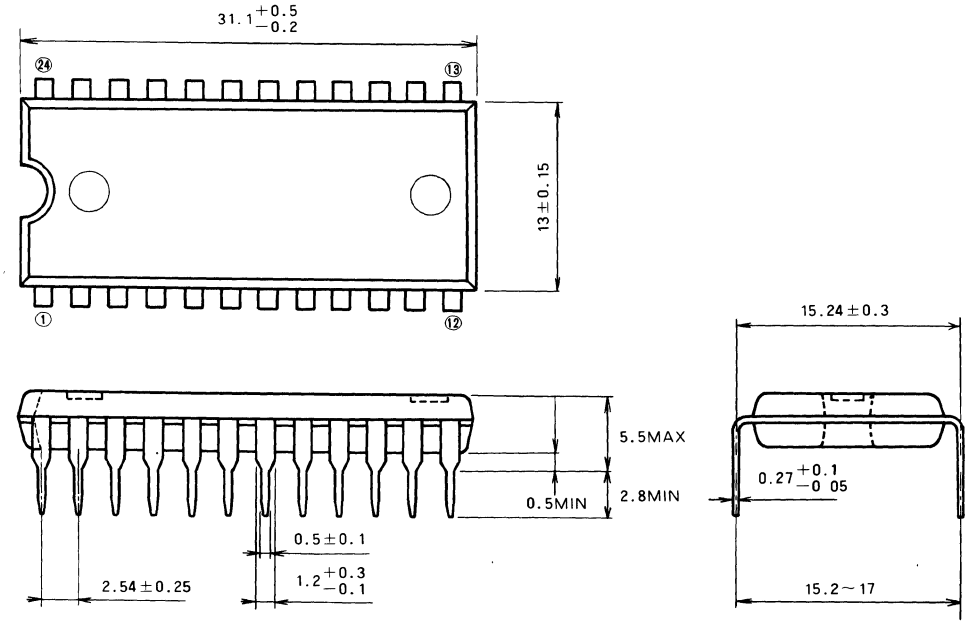


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

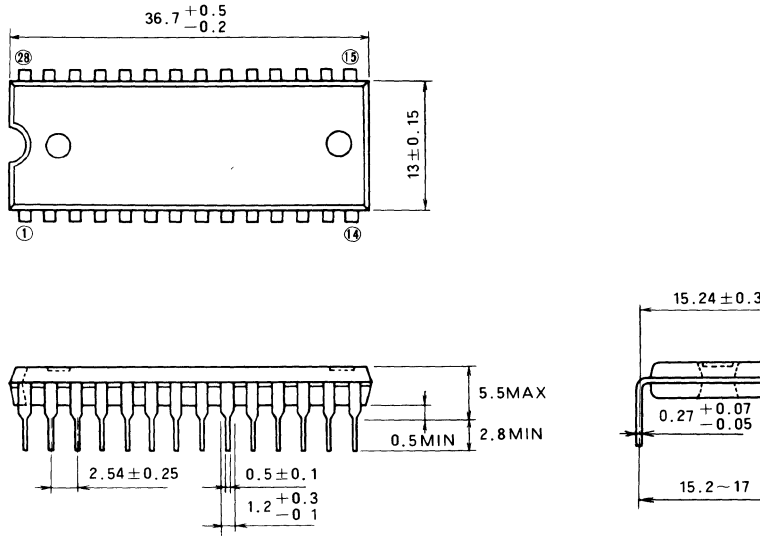
TYPE 24P4 24-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 28P4 28-PIN MOLDED PLASTIC DIP

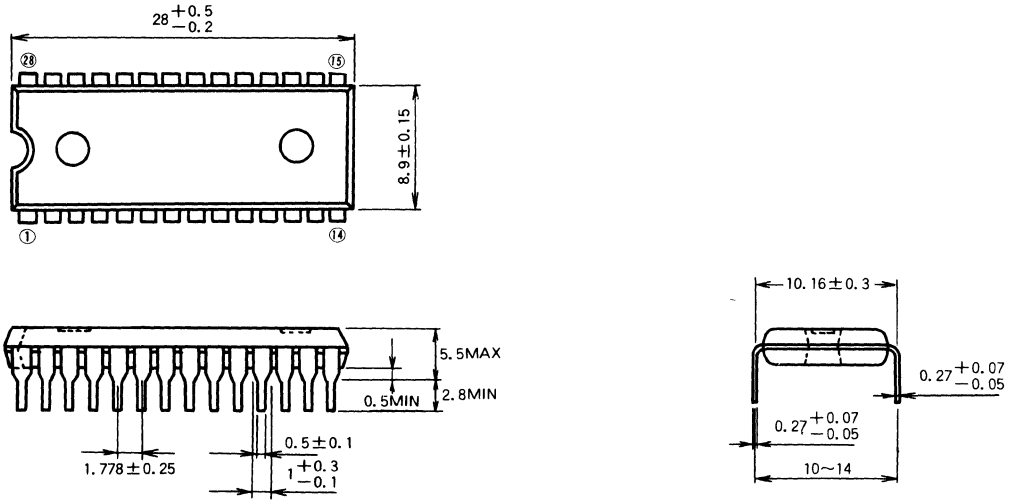
Dimension in mm



PACKAGE OUTLINES

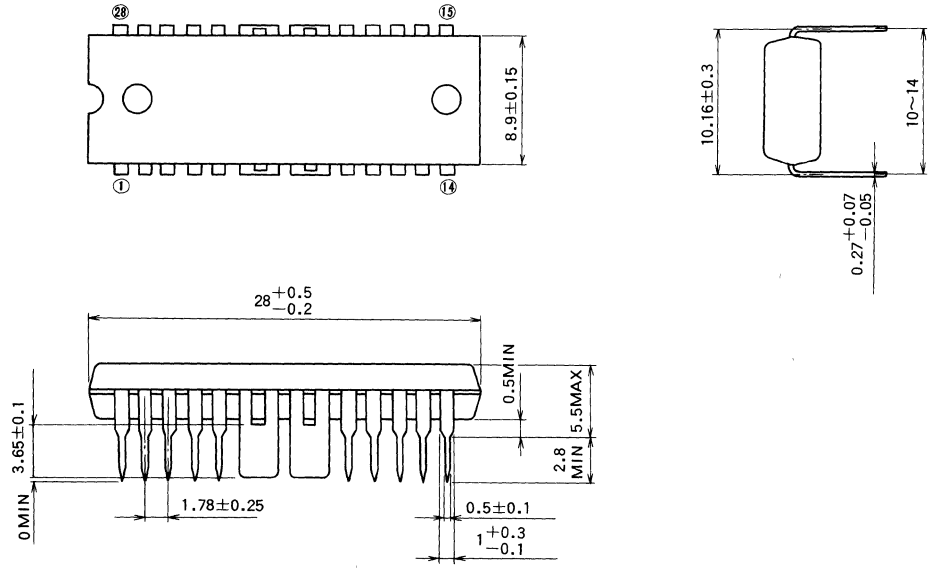
TYPE 28P4B 28-PIN MOLDED PLASTIC DIP(LEAD PITCH 1.778mm)

Dimension in mm



TYPE 28P4B-A 28-PIN PLASTIC DIP (SHRINK)

Dimension in mm

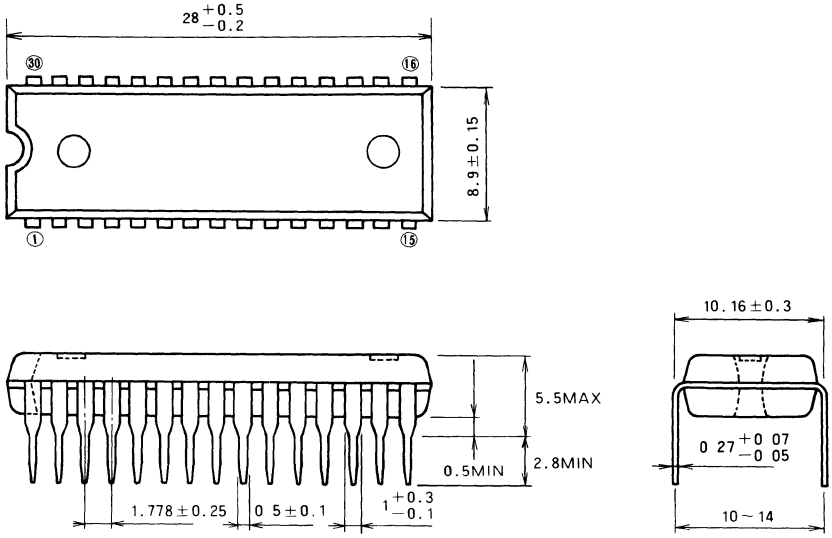


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

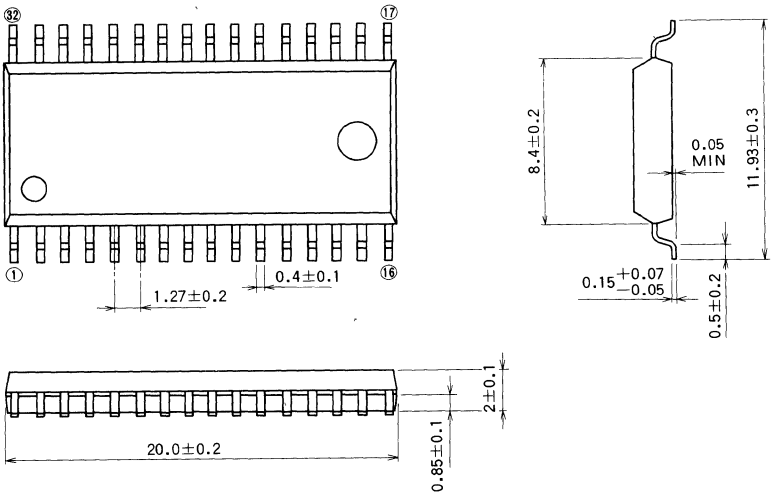
TYPE 30P4B 30-PIN MOLDED PLASTIC DIP(SHRINK)

Dimension in mm



TYPE 32P2W-A 32-PIN MOLDED PLASTIC FLAT

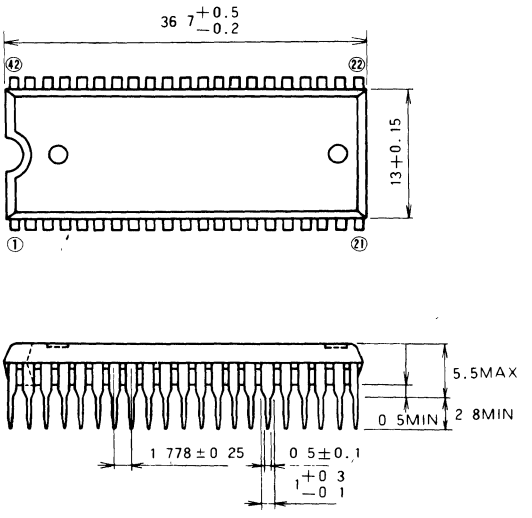
Dimension in mm



PACKAGE OUTLINES

TYPE 42P4B 42-PIN MOLDED PLASTIC DIP(SHRINK)

Dimension in mm



DATA SHEETS

2

M54101P

LEVEL DETECTOR

DESCRIPTION

The M54101P is a semiconductor integrated circuit containing a differential amplifier and Schmitt circuit suitable for temperature control.

FEATURES

- Suitable for high precision temperature control circuits
- High output current, high breakdown voltage (I_O=40mA, V_O=30V)
- Wide operating temperature range (T_a=−20～+75℃)

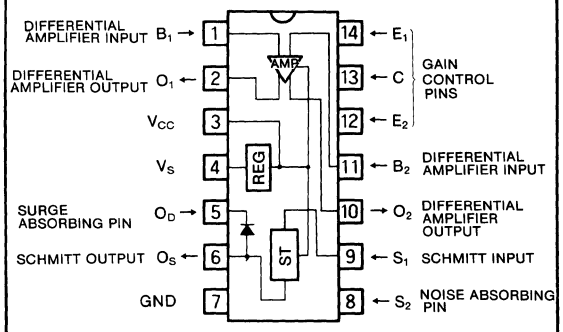
APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

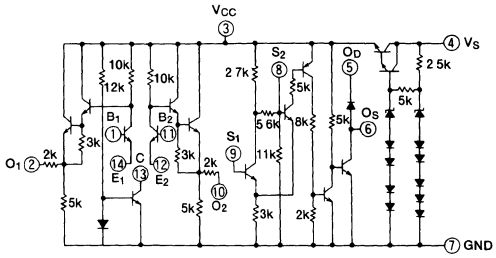
Designed for detecting minute changes in voltage and current, this IC is especially suitable for temperature control circuits using thermistors as sensors. Besides containing the differential amplifier and Schmitt circuit necessary for a control IC, it also employs a constant voltage circuit enabling usage of a 12～16V power supply source. Being an open collector, output O_S can be used to drive a relay or a lamp. Further, in the output O_S circuit is a diode limiter which can be used in case of relay overload.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC



Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_S	Supply voltage		20	V
V_I	Input voltage		V_{CC} (Note 1)	V
V_{ID}	Differential input voltage (Note 2)		±5	V
V_O	Output voltage	"H" level state	30	V
I_O	Output current	"L" level state	50	mA
V_R	Reverse voltage		30	V
P_d	Power dissipation		500	mW
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

Note 1 : V_{CC} is value of voltage at pin 3.
2 : Voltage difference between inputs B_1 and B_2

RECOMMENDED OPERATING CONDITIONS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		12	14	16	V
V_O	Output voltage	"H" level state			V_S	V
I_{OL}	"L" level output current	V_{OL} = 0.6V			40	mA
I_{AS}	Total output current (Note 3)				−4	mA

Note 3 : This is the total of all output current (excluding pins 4, 7).

ELECTRICAL CHARACTERISTICS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Temp (℃)	Limits			Unit	Test circuit
					Min	Typ*	Max		
V_{CC}	Supply voltage	I_{CC} = −2mA V_{B1} = V_{B2} = 1.6V 12, 13, 14 Connected	V_S = 12V		7.8		9.6	V	1
			V_S = 16V						
Reg_1	Regulation 1 (Note 4)	I_{CC} = −2mA, V_{B1} = V_{B2} = 1.6V 12, 13, 14 Connected		425			0.22	V	1
Reg_2	Regulation 2 (Note 4)	V_S = 14V, V_{B1} = V_{B2} = 1.6V 12, 13, 14 Connected		25			0.22	V	1
I_{IN}	Input bias current	V_{B1} = V_{B2} = 1.6V 12, 13, 14 Connected	V_{CC} = 8.7V				17	μA	2
			V_{CC} = 9.6V				20		
V_{OO}	Output offset voltage (Note 5)	V_{B1} = V_{B2} = 1.6V 12, 13, 14 Connected	V_{CC} = 8.7V				0.5	V	3
			V_{CC} = 9.6V				0.55		
G_V	Voltage gain (Note 5)	V_{B1} = 1.65V V_{B2} = 1.6V 12, 13, 14 Connected	V_{CC} = 8.7V	−20	3.95		5.55	V	3
				25	3.75		5.15		
				75	3.35		4.95		
			V_{CC} = 7.8V	−20	3.25				
				25	3.15				
				75	2.85				
			V_{CC} = 9.6V	−20			6.25		
				25			5.75		
				75			5.45		
G_V	Voltage gain (Note 5)	V_{B1} = 1.6V V_{B2} = 1.65V 12, 13, 14 Connected	V_{CC} = 8.7V	−20	3.95		5.55	V	3
				25	3.75		5.15		
				75	3.35		4.95		
			V_{CC} = 7.8V	−20	3.25				
				25	3.15				
				75	2.85				
			V_{CC} = 9.6V	−20			6.25		
				25			5.75		
				75			5.45		
V_{T+}	Positive-going threshold voltage	V_{CC} = 8.7V		−20	3.75		4.45	V	4
				25	3.8		4.4		
				75	3.75		4.45		
		V_{CC} = 7.8V		−20	3.3				
				25	3.35				
				75	3.3				
		V_{CC} = 9.6V		−20			4.9		
				25			4.85		
				75			4.9		

Continue to next page

ELECTRICAL CHARACTERISTICS (continued)

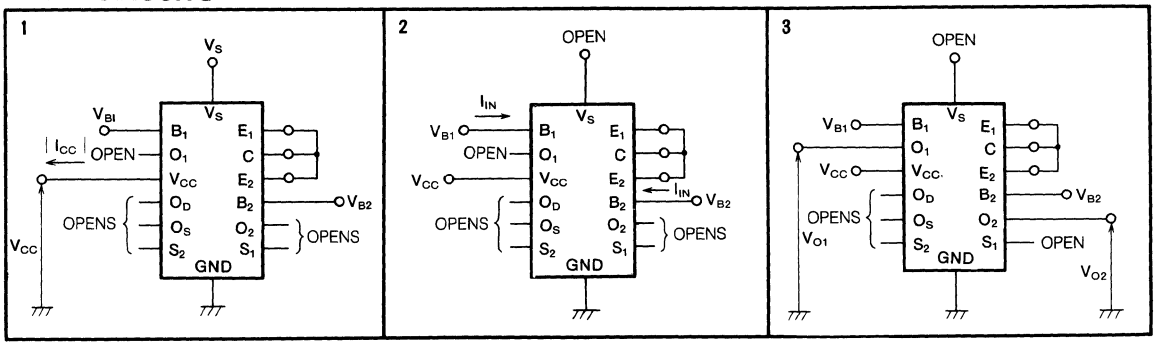
Symbol	Parameter	Test conditions	Temp (°C)	Limits			Unit	Test circuit
				Min	Typ*	Max		
V_{T-}	Negative-going threshold voltage	V_{CC} = 8.7V	−20	3.15		3.85	V	5
			25	3.2		3.8		
			75	3.15		3.85		
		V_{CC} = 7.8V	−20	2.75				
			25	2.8				
			75	2.75				
		V_{CC} = 9.6V	−20			4.25		
			25			4.2		
			75			4.25		
I_{T+}	"V_{T+}" input current	V_{CC} = 8.7V	−20	180			μA	4
			25	100				
			75	80				
		V_{CC} = 9.6V	−20	200				
			25	110				
			75	90				
I_{OH}	"H" level output current	V_{SI} = 3.2V, V_{CC} = 9.6V, V_{OH} = 16V				250	μA	5
V_{OL}	"L" level output current	V_{SI} = 4.5V, V_{CC} = 7.8V, I_{OL} = 40mA			0.3	0.6	V	4
V_O	Output voltage	V_{SI} = 3.2V, V_{CC} = 8.7V, I_O = 1mA		30			V	6
V_R	Reverse voltage	V_{OS} = 0V, I_R = 1mA		30			V	7
V_F	Forward voltage	V_{OD} = 0V, I_F = 20mA	25			1.2	V	7
I_S	Supply current	V_{B1} = V_{B2} = 1.6V, V_S = 16V 12, 13, 14 Connected	25			13	mA	8

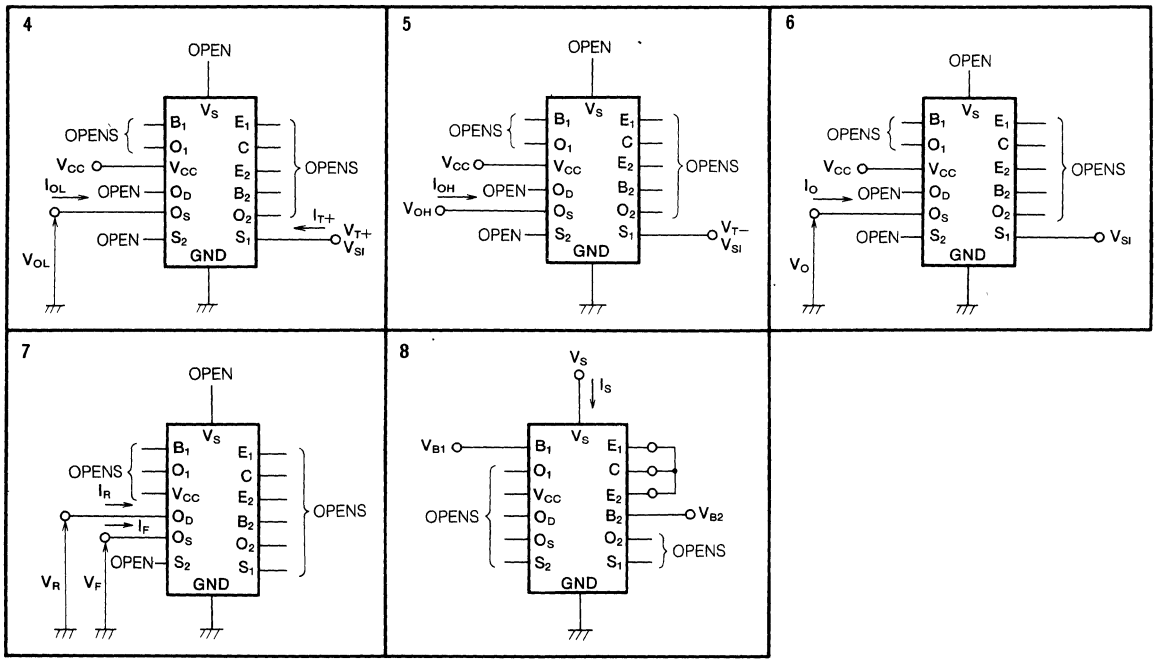
* : A typical value is at T_a=25°C.

Note 4 : Conditions of Regulation 1 and Regulation 2 are set as follows.
Reg 1 = V_{CC1} (V_{CC} when V_{CC} = 16V) − V_{CC2} (V_{CC} When V_S = 12V)
Reg 2 = V_{CC1} (V_{CC} when I_L = circuit current+2mA) − V_{CC2} (V_{CC} when I_L = circuit current+6mA)

5 : All parameters are set at $|V_{01}-V_{02}|$.

TEST CIRCUITS





APPLICATION EXAMPLES

Basic ON/OFF thermo-circuit

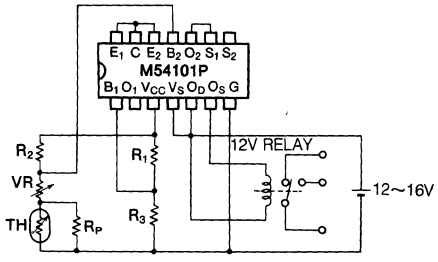


Fig.1 CIRCUIT

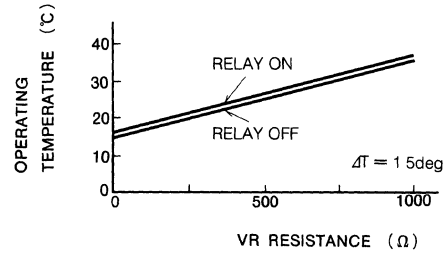


Fig.2 EXAMPLE CHARACTERISTICS

The differential amplifier connections B_1 and B_2 are biased through the bridge consisting of R_1, R_2, R_3, R_P, temperature level setting variable resistor V_R, and thermistor TH. Figure 2 shows the special characteristics of an air-conditioner room-thermal circuit employing a NTC thermistor. Hysteresis temperature ΔT varies according to value of resistance inserted between pins $E_1 \cdot C$ and $E_2 \cdot C$.

MITSUBISHI ELECTRIC

M54121L

EARTH LEAKAGE CURRENT DETECTOR

DESCRIPTION

M54121L is a semiconductor integrated circuit functioning as a highspeed ground fault circuit interrupter-amplifier.

FEATURES

- Easily meets JIS C 8371 specifications
- Excellent input current sensitivity to temperature characteristics
- Need for few externally connected components makes unit economical
- Highly resistant to noise and surges
- Low power dissipation (P_d=32mW)
- High input sensitivity (20mV at normal usage)
- Has high packaging density for an 8 pin SIL
- Wide operating temperature range (T_a=−20~75℃)

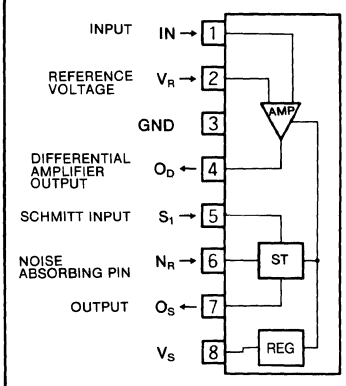
APPLICATION

For use in high-speed ground fault circuit interrupters, ground fault circuit interrupter alarms, and other relay applications.

FUNCTIONAL DESCRIPTION

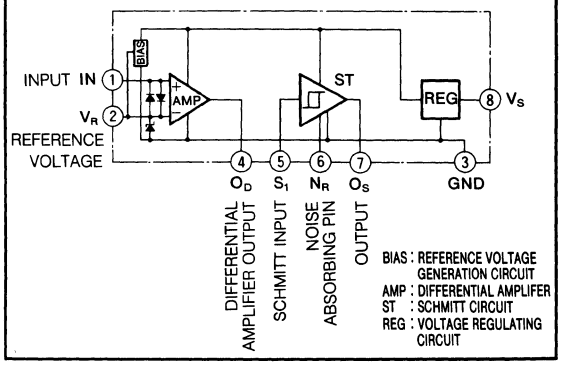
For use in a ground fault circuit interrupter amplifiers, this integrated circuit includes a differential amplifier circuit, a Schmitt circuit, and a constant voltage circuit. It is connected to the secondary of a zero current-transformer, which detects current leakage in the input side of the differential amplifier. The output signal of the differential amplifier is integrated in an externally mounted capacitor. Having been delayed, long enough to satisfy the characteristics specified by JIS C 8371 for high-speed type ground fault circuit interrupters, the signal is fed to the Schmitt circuit. As long as input voltage remains below the preset level Schmitt circuit output is maintained at "L" level. When a current leakage larger than the preset amount is detected, the output becomes "H" level and the thyristor, located on the Schmitt circuit output, is driven.

PIN CONFIGURATION (TOP VIEW)



Outline 8P5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_S	Supply voltage		20	V
I_{IN}	IN current	Between IN−V_R	60	mA
I_{IN}	IN current	Between IN−GND	30	mA
I_{IN}	IN current	Between V_R−IN	−60	mA
I_{VR}	V_R current	Between V_R−IN	60	mA
I_{VR}	V_R current	Between V_R−GND	30	mA
I_{VR}	V_R current	Between IN−V_R	−60	mA
I_{SI}	S_I Input current		10	mA
P_d	Power dissipation		200	mW
T_{opr}	Operating temperature		−20~+75	℃
T_{stg}	Storage temperature		−55~+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	yp	Max	
V_S	Supply voltage	14	16	18	V

ELECTRICAL CHARACTERISTICS (T_a = −20∼+75℃, unless otherwise noted)

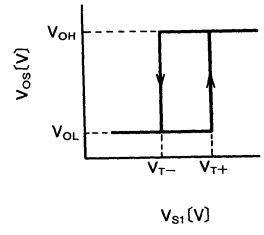
Symbol	Parameter	Test conditions	Temp (℃)	Limits			Unit	Test circuit
				Min	Typ*	Max		
V_{ODL}	"L" saturated output voltage	V_S = 18V, V_{IN} = 3.21V, V_R = 3.25V	−20			1.4	V	1
		V_S = 18V, V_{IN} = 2.96V, V_R = 3V	25			1.4		
		V_S = 18V, V_{IN} = 2.66V, V_R = 2.7V	75			1.4		
V_{OD1}	Differential amplifier output voltage 1	V_S = 16V, $V_I - V_R$ = 30mV	−20	3.3		5.8	V	2
			25	3		5.3		
			75	2.5		5		
V_{OD2}	Differential amplifier output voltage 2	V_S = 16V, $V_I - V_R$ = 60mV	−20	6.2		8	V	2
			25	6.1		7.7		
			75	5.7		7.5		
V_{OD3}	Differential amplifier output voltage 3	V_S = 16V, V_R = 3V, V_{IN} = 3.16V	−20	7.2		9.2	V	1
			25	7.8		9.6		
			75	8.2		10.2		
V_{T+}	Positive-going threshold voltage (Note 1)	V_S = 16V	−20	1.52		2.2	V	3
			25	1.35		1.95		
			75	1.05		1.73		
V_{T-}	Negative-going threshold voltage (Note 1)	V_S = 16V	−20	0.3		1.2	V	3
			25	0.2		1		
			75	0.05		0.95		
I_{T+}	"V_{T+}" input current (Note 1)	V_S = 16V	25	5			μA	3
I_O	Output current	V_S = 14V, V_{S1} = 2V, V_O = 0.8V	−20	−0.7			mA	3
			25	−0.6				
			75	−0.35				
V_{IC}	Input clamp diode voltage	V_S = 16V, I_{IC} = 20mA		4.3		6.7	V	4
V_{IDC}	Differential clamping voltage	I_{IDC} = 50mA		0.4		2.1	V	5
I_S	Supply current	V_S = 16V, $V_R - V_I$ Connected	25		2	3	mA	6
V_{S1}	S1 voltage	V_S = 16V, I_{SI} = 5mA	25	4.6		6.6	V	7

* : A Typical value is at T_a = 25℃

Note 1 : V_{T+}, V_{T-} are the voltages expressed in the chart at the right

2 : When testing each parameter be sure to insert a 0.01μF capacitor between V_R (pin 2) and GND (pin 3).

3 : A 3.9kΩ resistor is connected between pin IN and other pin V_I



TEST CIRCUITS

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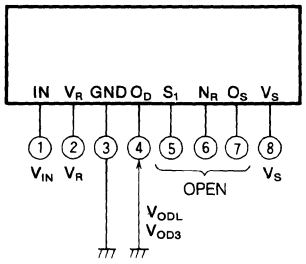

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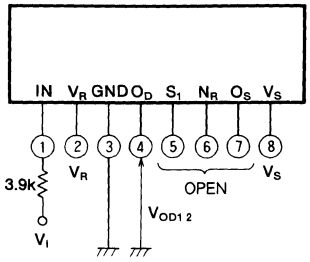

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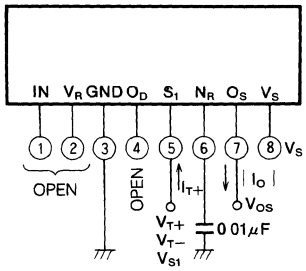

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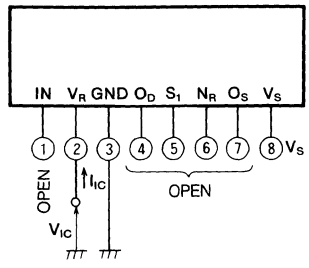

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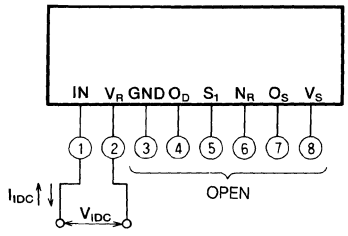

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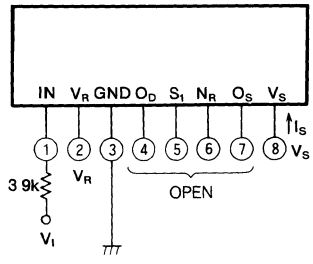

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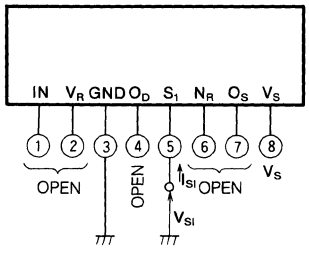
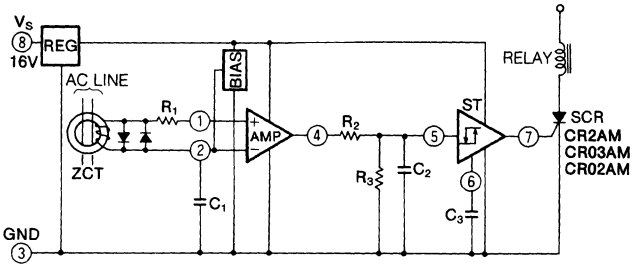


Note : All resistor units are in ohms.

APPLICATION EXAMPLE

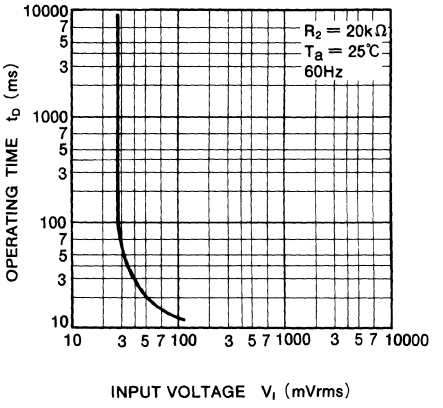
● HIGH-SPEED TYPE GROUND FAULT CIRCUIT INTERRUPTER UTILIZING THE M54121L



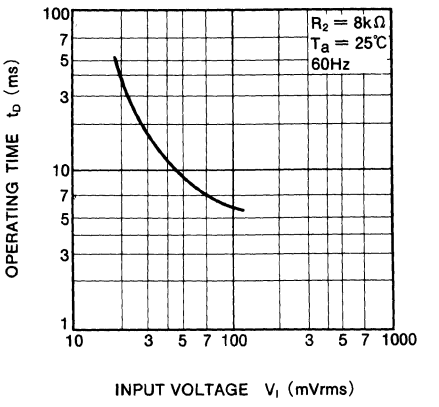
$R_1 = 3.9k\Omega$, $R_3 = 39k\Omega$, $C_1 = 0.01\mu F$, $C_2 = 1\mu F$, $C_3 = 1\mu F$

TYPICAL CHARACTERISTICS

OPERATING TIME VS INPUT VOLTAGE



OPERATING TIME VS INPUT VOLTAGE



MITSUBISHI ELECTRIC

M54122L

EARTH LEAKAGE CURRENT DETECTOR

DESCRIPTION

M54122L is a semiconductor integrated circuit with amplifier for a high-speed earth leakage circuit breaker.

FEATURES

- Suitable for JIS C 8371
- Good temperature characteristics of input sensitivity current
- High input sensitivity (V_T=13.5mV Typ.)
- Low external component count
- High noise and surge-proof
- Low power dissipation (P_d = 5mW Typ.) and may be used both as 100V and 200V.
- High mounting density by SIL package with 8 pins
- Wide temperature range (T_a=−20∼+80℃)

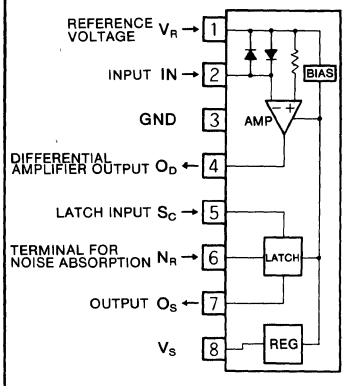
APPLICATION

High speed earth leakage circuit breaker

FUNCTION

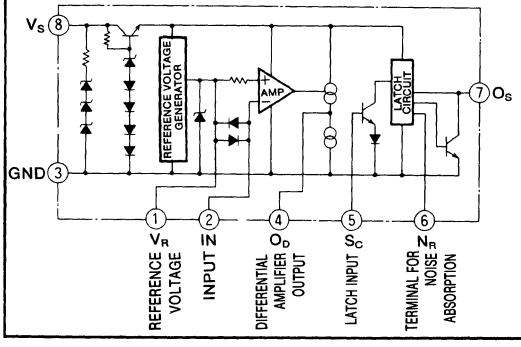
The M54122L circuit for the amplifying parts of earth leakage circuit breaker consists of differential amplifier, latch circuit and voltage regulator. It is connected to the secondary side of the zero-current transformer (ZCT) which detects leakage current in the both input of the differential amplifier. Signals amplified by differential amplifier are integrated by an external capacitor, and connects to the input terminal of latch circuit with output suitable for the characteristics of high-speed earth leakage circuit breaker. Latch circuit keeps low in the output till the input voltage reaches the fixed level, and output becomes high when the leakage current more than fixed flows. It drives a thyristor connected to the output terminal of latch circuit.

PIN CONFIGURATION (TOP VIEW)



Outline 8P5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+80℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
I_S	Supply current		8	mA
I_{VR}	V_R terminal current	Between V_R−IN (Note 1)	250	mA
		Between V_R−GND	30	
		Between IN−V_R (Note 1)	−250	
I_{IN}	I_{IN} terminal current	Between IN−V_R (Note 1)	250	mA
		Between IN−GND	30	
		Between V_R−IN (Note 1)	−250	
I_{SC}	S_C terminal current		5	mA
P_d	Power dissipation		200	mW
T_{opr}	Operating temperature		−20∼+80	℃
Tstg	Storage temperature		−55∼+125	℃

Note 1 : Current value between V_R and IN, and between IN and V_R is less than 1ms in the pulse width, and duty cycle is less than 12% In applying AC current continuously, it is 100mArms in the off-state.

Remarks : GND terminal (pin 3) of the circuit is a basis of all the voltages except differential input clamp voltage of DC electrical characteristics, and direction of current is plus (no signal) in flowing into the circuit and is minus (−signal) in flowing out of it Maximum value and minimum one are shown as absolute value Please don't apply voltage whose standard is GND terminal in V_R and IN pin

RECOMMENDED OPERATING CONDITIONS (T_a = −20∼+80℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_S	Supply voltage when latch circuit is off-state	12			V
C_{VS}	External capacitor between V_S and GND	1			μF
C_{OS}	External capacitor between O_S and GND			1	μF

ELECTRICAL CHARACTERISTICS (T_a = −20∼+80℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Temp. (℃)	Limits			Unit	Test circuit
					Min	Typ*	Max		
I_{S1}	Supply current	V_S=12V, V_R-V_I=30mV		−20			580	μA	1
				25		400	530		1
				80			480		1
V_T	Trip voltage	V_S=16V, V_R-V_I (Note 2)		−20∼+80	10	13.5	17	mV_{rms}	2
I_{TD1}	Timing current 1	V_S=16V, V_R-V_I=30mV, V_{OD}=1.2V		25	−12		−30	μA	3
I_{TD2}	Timing current 2	V_S=16V, short circuit between V_R and V_I V_{OD}=0.8V		25	17		37	μA	4
I_O	Output current	V_{SC}=1.4V V_{OS}=0.8V	I_{S1}=580μA	−20	−200			μA	5
			I_{S1}=530μA	25	−100				5
			I_{S1}=480μA	80	−75				5
$V_{SC"ON"}$	S_C on voltage (Note 3)	V_S=16V		25	0.7		1.4	V	6
$I_{SC"ON"}$	S_C input current	V_S=12V		25			5	μA	7
I_{OSL}	Output low-level current	V_S=12V, V_{OSL}=0.2V		−20∼+80	200			μA	8
V_{IC}	Input clamp voltage	V_S=12V, I_{IC}=20mA		−20∼+80	4.3		6.7	V	9
V_{IDC}	Differential input clamp voltage	I_{IDC}=100mA		−20∼+80	0.4		2	V	10
V_{SM}	Maximum current voltage	I_{SM}=7mA		25	20		28	V	11
I_{S2}	Supply current 2 (Note 4)	V_R-V_I V_{OS}=0.6V (Note 5)		−20∼+80			900	μA	12
$V_{S"OFF"}$	Latch circuit is off-state supply voltage (Note 6)			25	0.5			V	13
T_{ON}	Operational time (Note 7)	V_S=16V, V_R-V_I=0.3V		25	2		4	ms	14

* : Typical values are at T_a = 25℃.

Note 2 : When standard value of voltage (60Hz) between V_R and V_I is minimum, and output O_S is low-level, or when standard value of voltage (60Hz) between V_R and V_I is maximum, and output O_S is high-level, it is considered as a good one.

3 : When standard value of voltage $V_{SC"ON"}$ is minimum, and output O_S is low-level, or when standard value of voltage $V_{SC"ON"}$ is maximum, and output O_S is high-level, it is considered as a good one.

4 : Supply current 2 is necessary to keep high in output O_S.

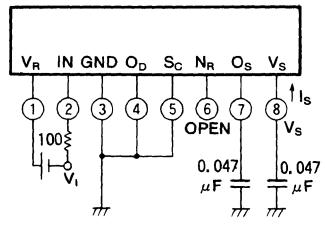
5 : After applying 30mV between V_R and V_I and shorting between them, it is considered as a good one if standard value of I_{GT} flows out of output O_S.

6 : After supply voltage applies 12V and output O_S is high-level, it is considered as a good one in the standard value of supply voltage and in the low-level of output O_S

7 : Operating time is a time from applying fixed input till operating latch circuit in 0.047μF between O_D and GND.

TEST CIRCUIT

1



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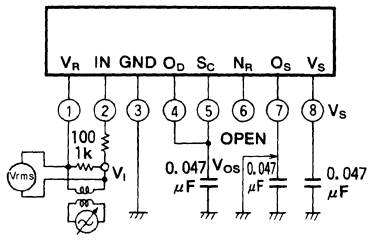

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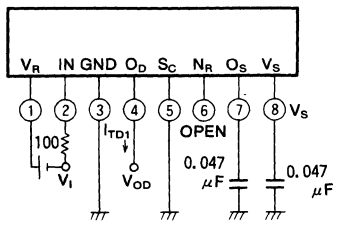

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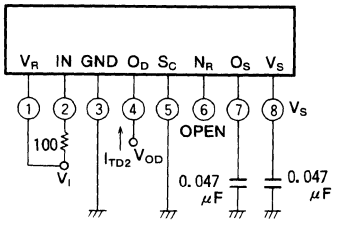

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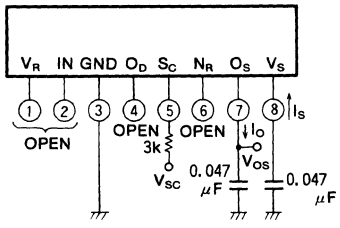

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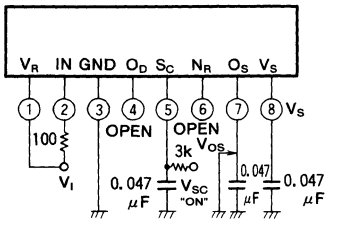

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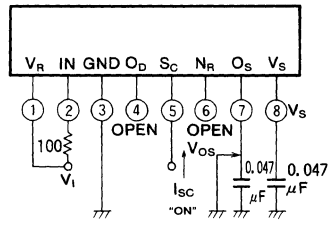

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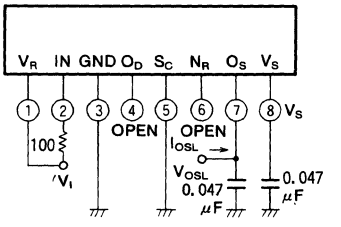

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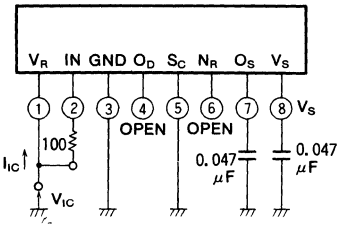

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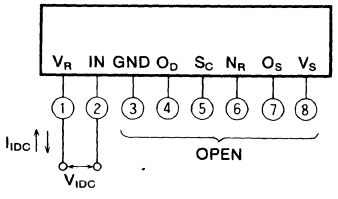

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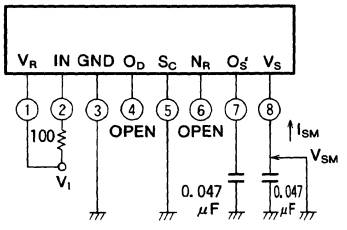

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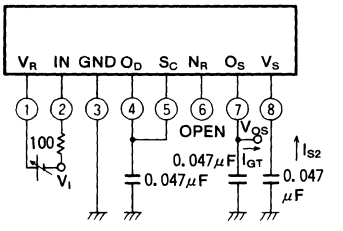

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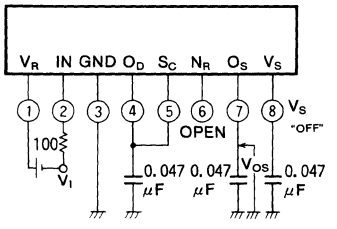

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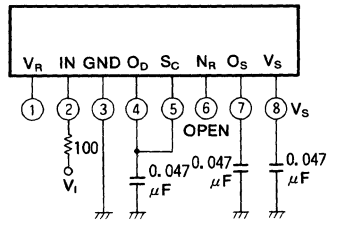
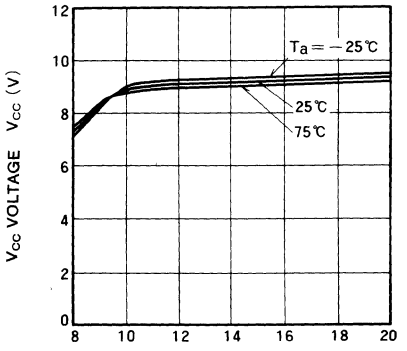


Note : The unit of resistance is ohm
Please insurt 0 01μF between pin 1 and pin 3 in test.

TYPICAL CHARACTERISTICS

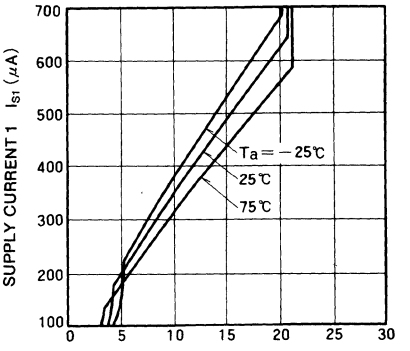
V_{CC} VOLTAGE VS SUPPLY VOLTAGE



SUPPLY VOLTAGE V_S (V)

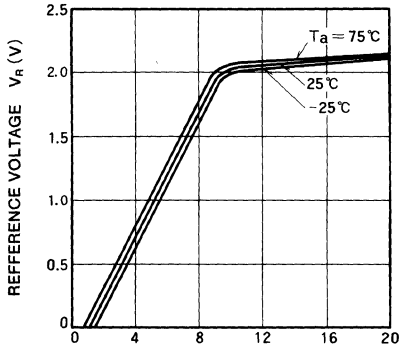
V_{CC} voltage generates by the constant voltage circuit in IC
This is measured not by M54122L but by a special element

SUPPLY CURRENT 1 VS SUPPLY VOLTAGE



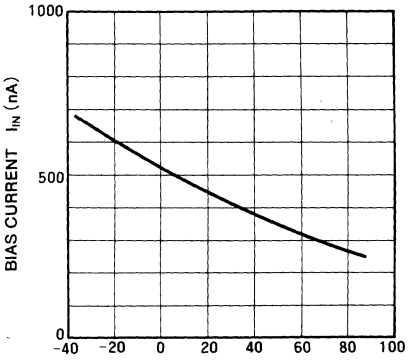
SUPPLY VOLTAGE V_S (V)

REFFERENCE VOLTAGE VS SUPPLY VOLTAGE



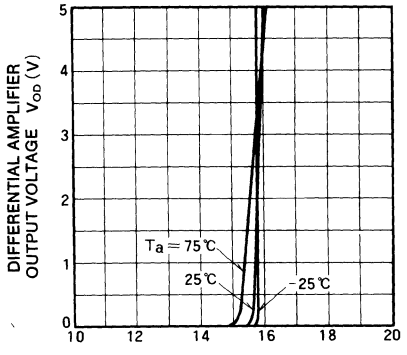
SUPPLY VOLTAGE V_S (V)

BIAS CURRENT VS AMBIENT TEMPERATURE



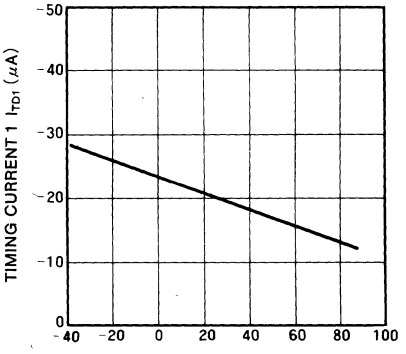
AMBIENT TEMPERATURE T_a (℃)

DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE VS DIFFERENTIAL INPUT VOLTAGE



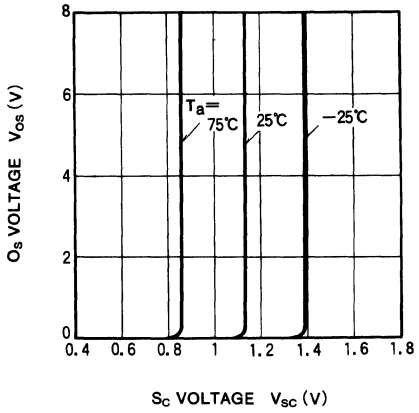
DIFFERENTIAL INPUT VOLTAGE $\Delta V_I = V_R - V_{IN}$ (mV)

TIMING CURRENT VS AMBIENT TEMPERATURE

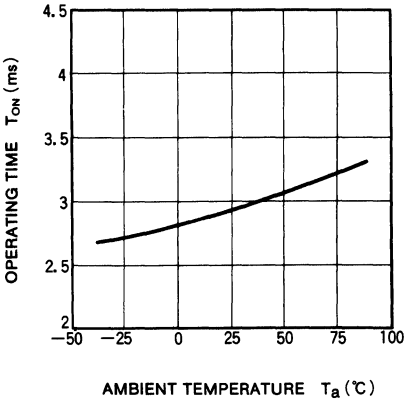


AMBIENT TEMPERATURE T_a (℃)

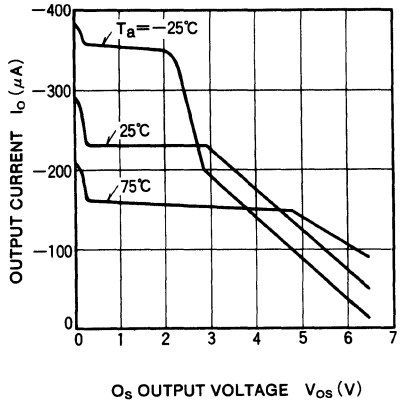
O_S VOLTAGE VS S_C VOLTAGE



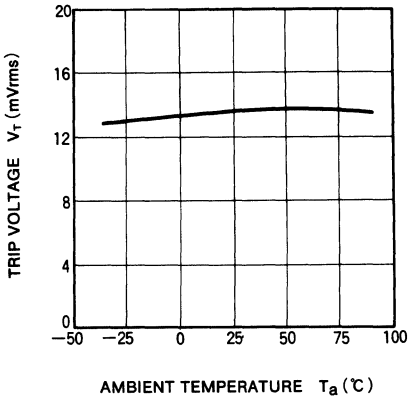
OPERATING TIME VS AMBIENT TEMPERATURE



OUTPUT CURRENT VS O_S OUTPUT VOLTAGE

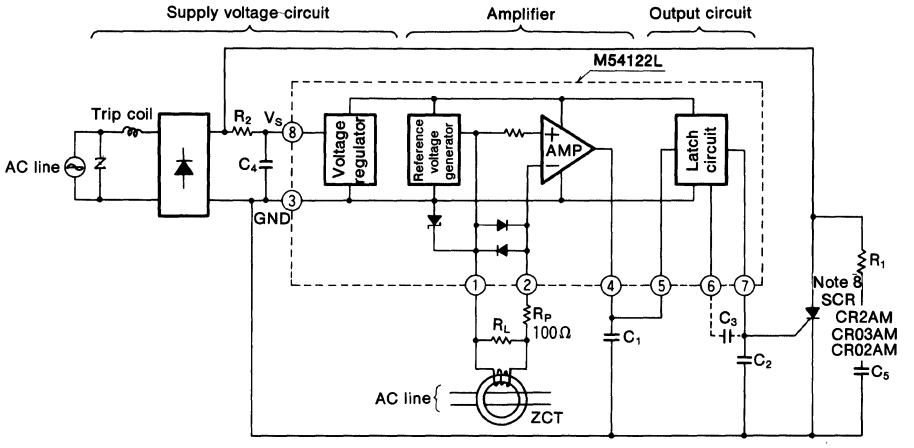


TRIP VOLTAGE VS AMBIENT TEMPERATURE



APPLIED EXAMPLE

● HIGH-SPEED EARTH LEAKAGE CIRCUIT BREAKER WITH M54122L



Note 8 : Gate current must be selected.
Please select voltage resistance by AC supply voltage.

Supply voltage circuit is connected as a previous diagram. Please decide constants R_1, R_2, C_4, and C_5 of a filter in order to keep at least 12V in V_S, when normal supply current flows.

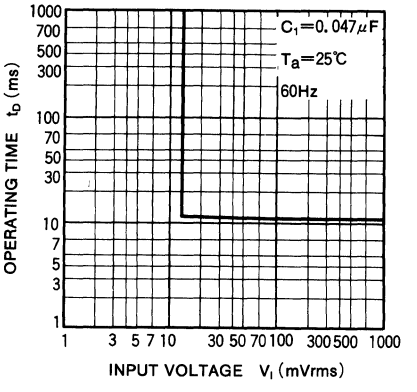
In this case, please connect C_4 (more than $1\mu F$) and C_2 (less than $1\mu F$). ZCT and load resistance R_L of ZCT are connected between input pin 1 and 2. In this case protective resistance ($R_P = 100\,\Omega$) must be insurted. Sensitivity current is regulated by R_L, and output of amplifier shows in pin 4. External capacitor C_1 between pin 4 and GND is used for noise removal.

When large current is grounded in the primary side (AC line) of ZCT, the wave form in the secondary side of ZCT is distorted and some signals doesn't appear in the output of amplifier. So please connect a varistor or a diode (2 pcs.) to ZCT in parallel.

Latch circuit is used to inspect the output level of amplifier and to supply gate current on the external SCR. When input pin becomes more than 1.1V (Typ.), latch circuit operates and supply gate current in the gate of SCR connected to the output pin 7.

Pin 6 can be used in the open state, but please connect capacitor (about $0.047\mu F$) between pin 6 and pin 7.

OPERATING TIME VS INPUT VOLTAGE



MITSUBISHI ELECTRIC

M54123L

EARTH LEAKAGE CURRENT DETECTOR

DESCRIPTION

M54123L is a semiconductor integrated circuit with amplifier for a high-speed earth leakage circuit breaker.

FEATURES

- Suitable for JIS C 8371
- Good temperature characteristics of input sensitivity current
- High input sensitivity (V_T=6.1mV Typ.)
- Low external component count
- High noise and surge-proof
- Low power dissipation (P_d = 5mW Typ.) and may be used both as 100V and 200V.
- High mounting density by SIL package with 8 pins
- Wide temperature range (T_a=−20∼+80℃)

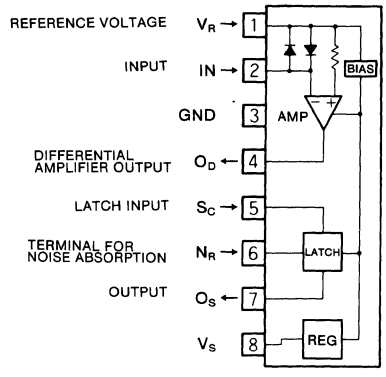
APPLICATION

High speed earth leakage circuit breaker

FUNCTION

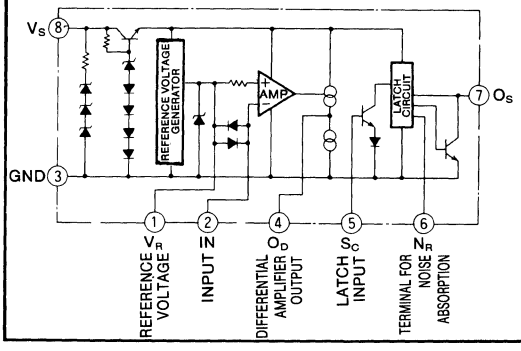
The M54123L circuit for the amplifying parts of earth leakage circuit breaker consists of differential amplifier, latch circuit and voltage regulator. It is connected to the secondary side of the zero-current transformer (ZCT) which detects leakage current in the both input of the differential amplifier. Signals amplified by differential amplifier are integrated by an external capacitor, and connects to the input terminal of latch circuit with output suitable for the characteristics of high-speed earth leakage circuit breaker. Latch circuit keeps low in the output till the input voltage reaches the fixed level, and output becomes high when the leakage current more than fixed flows. It drives a thyristor connected to the output terminal of latch circuit.

PIN CONFIGURATION (TOP VIEW)



Outline 8P5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+80℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
I_S	Supply current		8	mA
I_{VR}	V_R terminal current	Between V_R−IN (Note 1)	250	mA
		Between V_R−GND	30	
		Between IN−V_R (Note 1)	−250	
I_{IN}	I_{IN} terminal current	Between IN−V_R (Note 1)	250	mA
		Between IN−GND	30	
		Between V_R−IN (Note 1)	−250	
I_{SC}	S_C terminal current		5	mA
P_d	Power dissipation		200	mW
T_{opr}	Operating temperature		−20∼+80	℃
T_{stg}	Storage temperature		−55∼+125	℃

Note 1 : Current value between V_R and IN, and between IN and V_R is less than 1ms in the pulse width, and duty cycle is less than 12% In applying AC current continuously, it is 100mArms in the off-state

Remarks : GND terminal (pin 3) of the circuit is a basis of all the voltages except differential input clamp voltage of DC electrical characteristics, and direction of current is plus (no signal) in flowing into the circuit and is minus (−signal) in flowing out of it Maximum value and minimum one are shown as absolute value Please don't apply voltage whose standard is GND terminal in V_R and IN pin

RECOMMENDED OPERATING CONDITIONS (T_a = −20∼+80℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_S	Supply voltage when latch circuit is off-state.	12			V
C_{VS}	External capacitor between V_S and GND	1			μF
C_{OS}	External capacitor between O_S and GND			1	μF

ELECTRICAL CHARACTERISTICS (T_a = −20∼+80℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Temp. (℃)	Limits Min	Limits Typ*	Limits Max	Unit	Test circuit
I_{S1}	Supply current	V_S=12V, V_R−V_I=30mV		−20			580	μA	1
				25		400	530		1
				80			480		1
V_T	Trip voltage	V_S=16V, V_R−V_I (Note 2)		−20∼+80	4	6.1	9	mV_{rms}	2
I_{TD1}	Timing current 1	V_S=16V, V_R−V_I=30mV, V_{OD}=1.2V		25	−12		−30	μA	3
I_{TD2}	Timing current 2	V_S=16V, short circuit between V_R and V_I V_{OD}=0.8V		25	17		37	μA	4
I_O	Output current	V_{SC}=1.4V V_{OS}=0.8V	I_{S1}=580μA	−20	−200			μA	5
			I_{S1}=530μA	25	−100				5
			I_{S1}=480μA	80	−75				5
$V_{SC"ON"}$	S_C on voltage (Note 3)	V_S=16V		25	0.7		1.4	V	6
$I_{SC"ON"}$	S_C input current	V_S=12V		25			5	μA	7
I_{OSL}	Output low-level current	V_S=12V, V_{OSL}=0.2V		−20∼+80	200			μA	8
V_{IC}	Input clamp voltage	V_S=12V, I_{IC}=20mA		−20∼+80	4.3		6.7	V	9
V_{IDC}	Differential input clamp voltage	I_{IDC}=100mA		−20∼+80	0.4		2	V	10
V_{SM}	Maximum current voltage	I_{SM}=7mA		25	20		28	V	11
I_{S2}	Supply current 2 (Note 4)	V_R—V_I V_{OS}=0.6V (Note 5)		−20∼+80			900	μA	12
$V_{S"OFF"}$	Latch circuit is off-state supply voltage. (Note 6)			25	0.5			V	13
T_{ON}	Operational time (Note 7)	V_S=16V, V_R−V_I=0.3V		25	2		4	ms	14

* : Typical values are at T_a = 25℃.

Note 2 : When standard value of voltage (60Hz) between V_R and V_I is minimum, and output O_S is low-level, or when standard value of voltage (60Hz) between V_R and V_I is maximum, and output O_S is high-level, it is considered as a good one

3 : When standard value of voltage $V_{SC"ON"}$ is minimum, and output O_S is low-level, or when standard value of voltage $V_{SC"ON"}$ is maximum, and output O_S is high-level, it is considered as a good one.

4 : Supply current 2 is necessary to keep high in output O_S

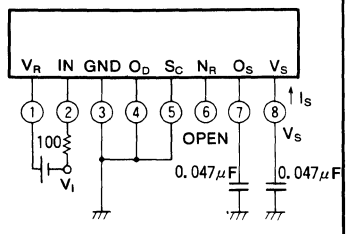
5 : After applying 30mV between V_R and V_I and shorting between them, it is considered as a good one if standard value of I_{GT} flows out of output O_S.

6 : After supply voltage applies 12V and output O_S is high-level, it is considered as a good one in the standard value of supply voltage and in the low-level of output O_S

7 : Operating time is a time from applying fixed input till operating latch circuit in 0.047μF between O_D and GND.

TEST CIRCUIT

1



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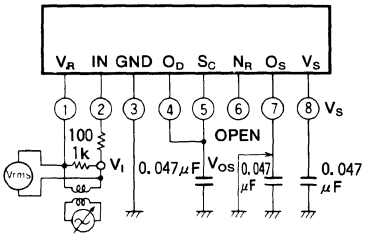

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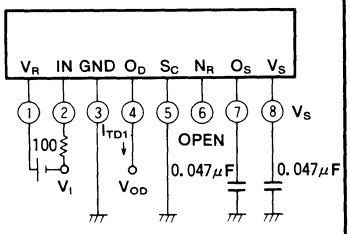

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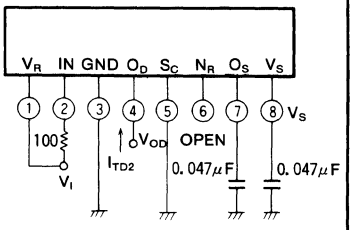

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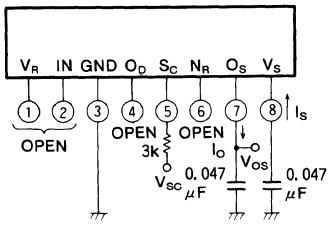

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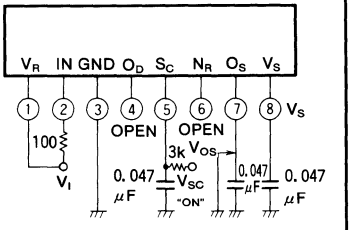

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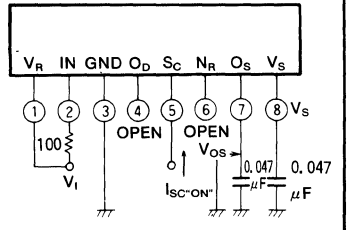

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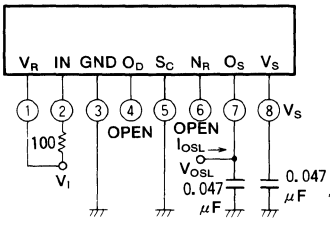

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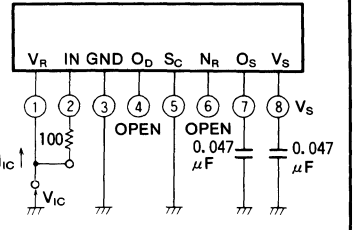

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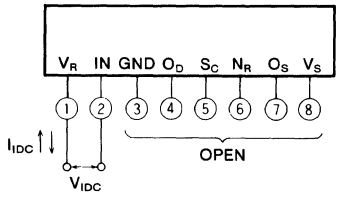

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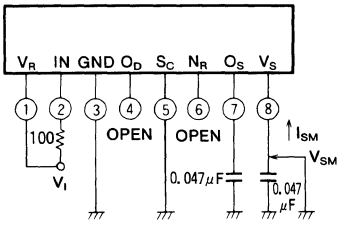

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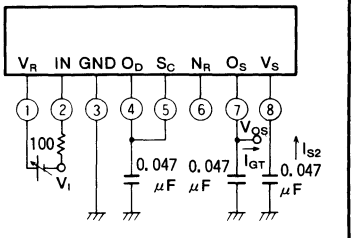

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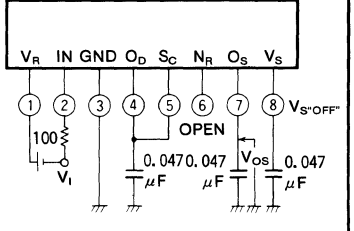

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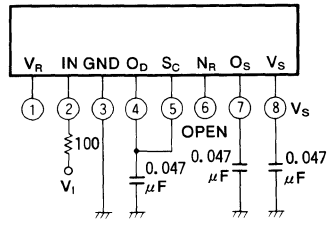
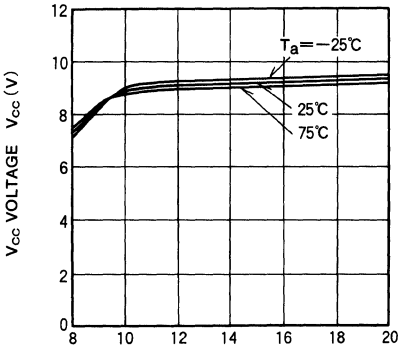


Note : The unit of resistance is ohm
Please insurt 0 01μF between pin 1 and pin 3 in test.

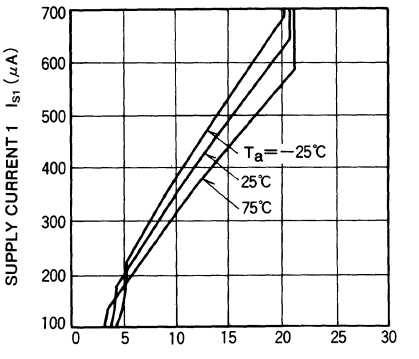
TYPICAL CHARACTERISTICS

V_{CC} VOLTAGE VS SUPPLY VOLTAGE

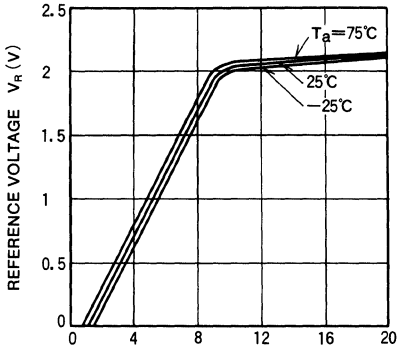


V_{CC} voltage generates by the constant voltage circuit in IC.
This is measured not by M54122L but by a special element

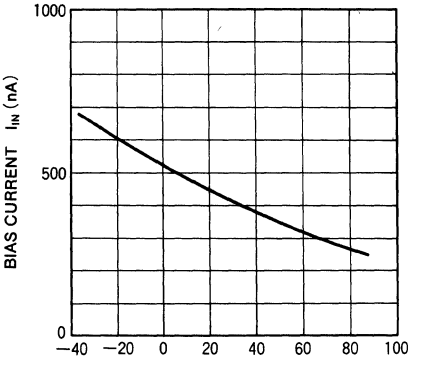
SUPPLY CURRENT 1 VS SUPPLY VOLTAGE



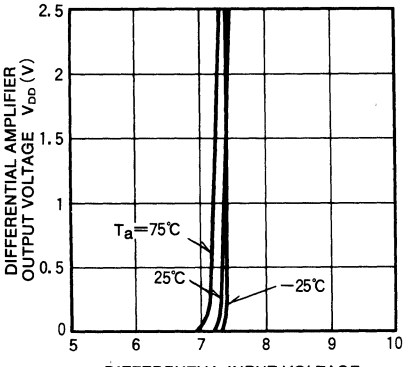
REFERENCE VOLTAGE VS SUPPLY VOLTAGE



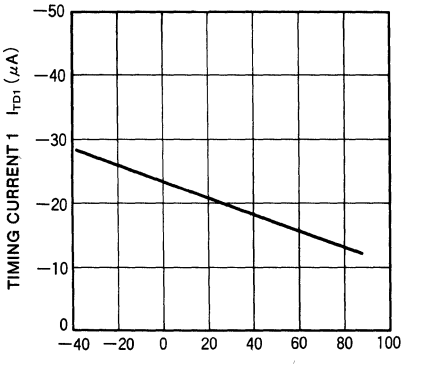
BIAS CURRENT VS AMBIENT TEMPERATURE



DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE VS DIFFERENTIAL INPUT VOLTAGE

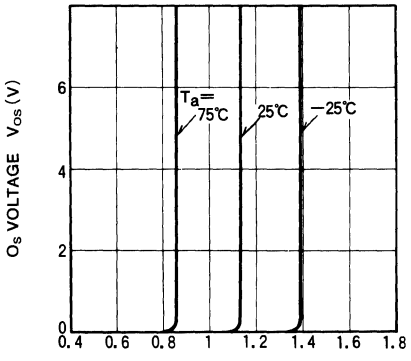


TIMING CURRENT VS AMBIENT TEMPERATURE

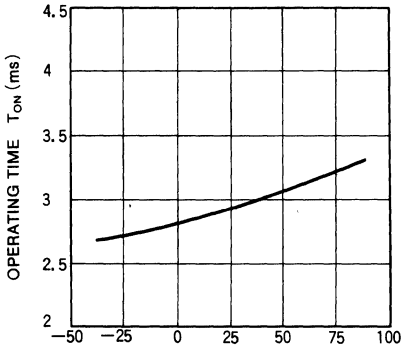


MITSUBISHI ELECTRIC

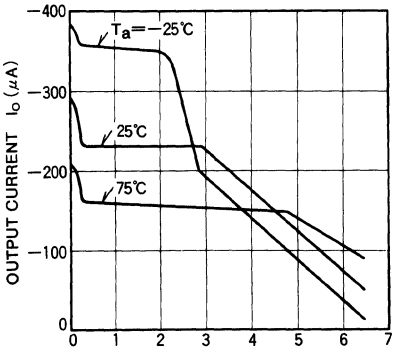
O_S VOLTAGE VS S_C VOLTAGE



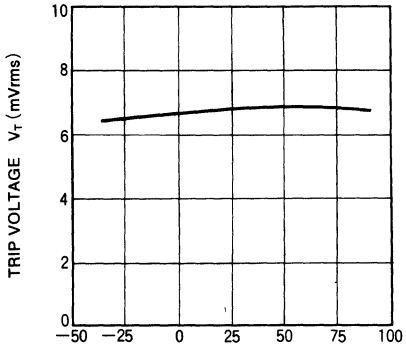
OPERATING TIME VS AMBIENT TEMPERATURE



OUTPUT CURRENT VS O_S OUTPUT VOLTAGE

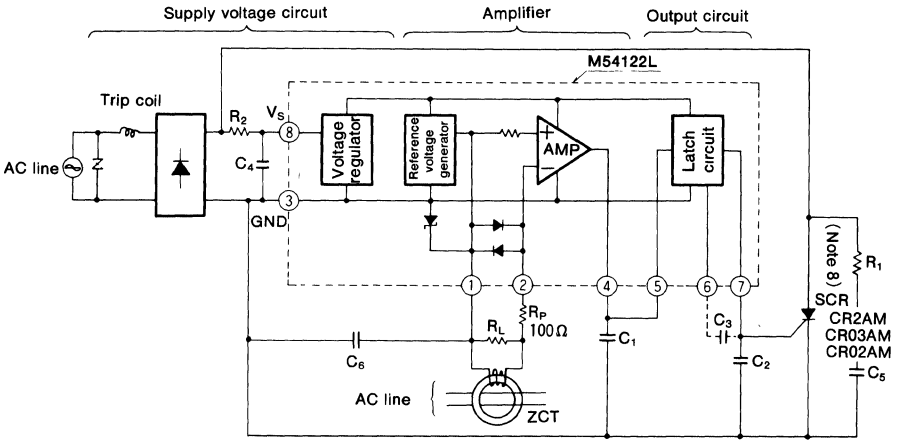


TRIP VOLTAGE VS AMBIENT TEMPERATURE



APPLIED EXAMPLE

● HIGH-SPEED EARTH LEAKAGE CIRCUIT BREAKER WITH M54122L



Note 8 : Gate current must be selected.
Please select voltage resistance by AC supply voltage

Supply voltage circuit is connected as a previous diagram. Please decide constants R_1, R_2, C_4, and C_5 of a filter in order to keep at least 12V in V_S, when normal supply current flows.

In this case, please connect C_4 (more than 1μF) and C_2 (less than 1μF). ZCT and load resistance R_L of ZCT are connected between input pin 1 and 2. In this case protective resistance (R_P = 100 Ω) must be insurted. Sensitivity current is regulated by R_L, and output of amplifier shows in pin 4. External capacitor C_1 between pin 4 and GND is used for noise removal.

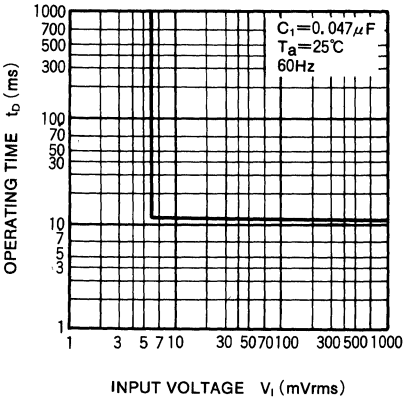
When large current is grounded in the primary side (AC line) of ZCT, the wave form in the secondary side of ZCT is distorted and some signals doesn't appear in the output of amplifier. So please connect a varistor or a diode (2 pcs.) to ZCT in parallel.

Latch circuit is used to inspect the output level of amplifier and to supply gate current on the external SCR. When input pin becomes more than 1.1V (Typ.), latch circuit operates and supply gate current in the gate of SCR connected to the output pin 7.

Pin 6 can be used in the open state, but please connect capacitor (about 0.047μF) between pin 6 and pin 7.

Capacitor C_6 between pin 1 and GND is used to remove noise and is about 0.047μF.

OPERATING TIME VS INPUT VOLTAGE



MITSUBISHI ELECTRIC

M54124L

EARTH LEAKAGE CURRENT DETECTOR

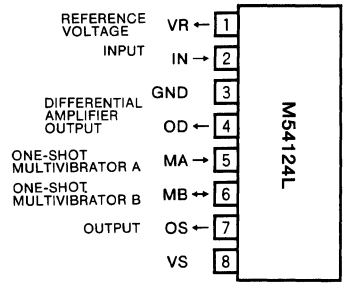
DESCRIPTION

The M54124L is a semiconductor integrated circuit consisting of an amplifier for a high-speed earth-leakage circuit breaker.

FEATURES

- Satisfies JIS C 8371
- Temperature-stable input current threshold
- High-input sensitivity (V_T=6.5mV)
- Low external component count
- Highly resistant to noise and power surges
- Low power dissipation (P_d= 5 mW typ)
- Can be used at 100V and 200V
- High-density mounting eight-pin SIL pacage
- Wide operating temperature range (T_a=−20∼+80℃)

PIN CONFIGURATION (TOP VIEW)



Outline 8P5

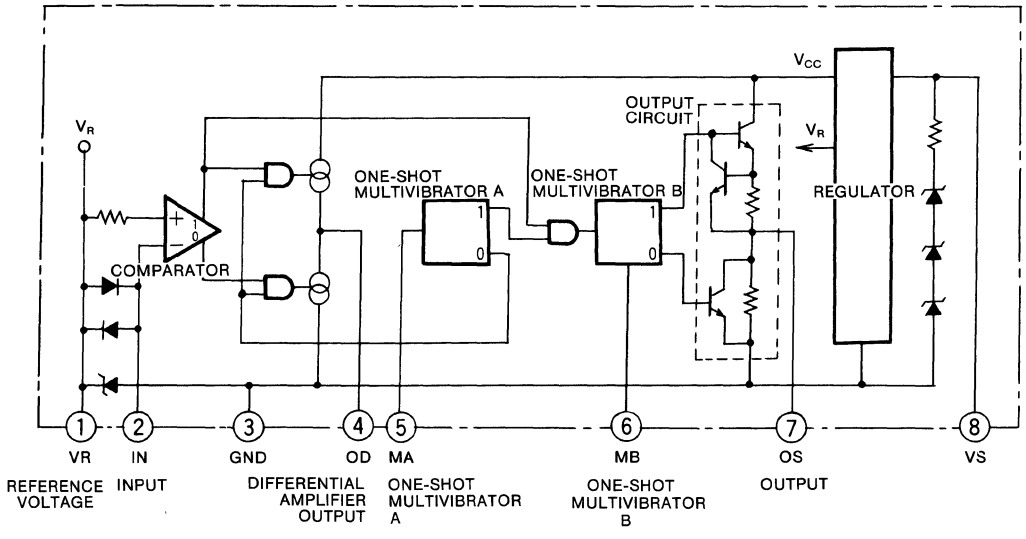
APPLICATION

High-speed earth-leakage circuit breakers

FUNCTION

The M54124L is a semiconductor integrated circuit for use in the amplifier section of earth-leakage circuit breakers. It consists of a differential amplifier, one-shot circuit, output circuit and voltage regulator. It is connected to the secondary side of the zero-current transformer, ZCT, and detects leakage current in both inputs of the differential amplifier. Signals amplified by the differential amplifier are integrated by an external capacitor, and applied to the input pin of a one-shot multivibrator circuit having time-delay characteristics that are suitable for high-speed earth-leakage circuit breakers (such as specified in JIS C 8371). The one-shot multivibrator circuit normally maintains a low output. When the input current (earth-leakage) exceeds a specified level, a one-shot high pulse is output to turn on an externally connected thyristor.

BLOCK DIAGRAM

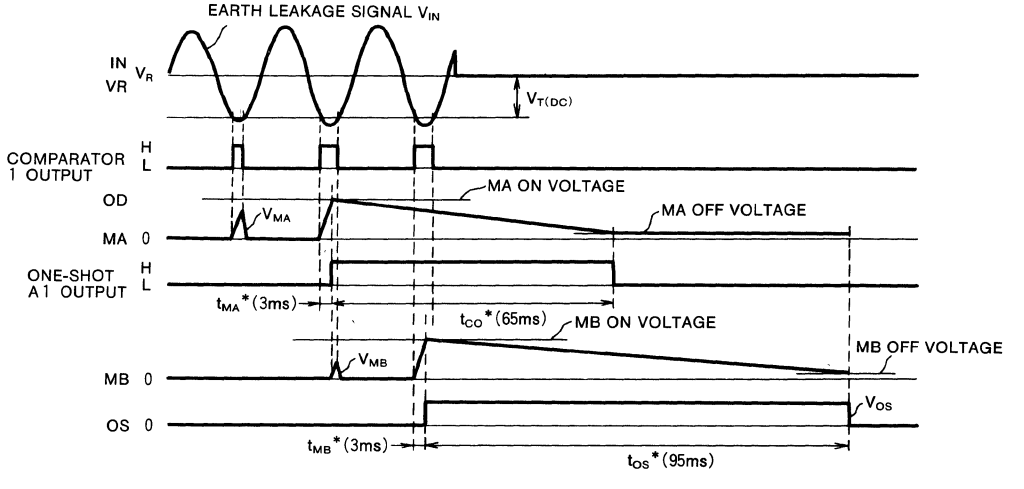


OPERATION

Discussion refers to the block diagram, application example, and operational waveform diagram.

- When an earth leakage current appears on the primary side of zero-current transformer ZCT, leakage signal voltage V_{IN} appears on the secondary side and is input at IN with VR as the reference.
- In the half cycle when V_{IN} is negative, capacitor C_{MA} connected to pin MA charges until V_{IN} reaches the trip voltage V_T (DC). If voltage V_{MA} at pin MA does not reach the MA threshold voltage, capacitor C_{MA} discharges immediately at a current greater than the charge current, when the charging current phase is completed. When V_{MA} reaches the MA threshold voltage, capacitor C_{MA} discharges at a small current for a period time t_{CO} during which the output of one-shot multivibrator A is high.
- During t_{CO}, the same operation takes place again at capacitor C_{MB}, causing one-shot multivibrator B to trigger current pulse of duration t_{OS} at output pin OS.
- Earth leakage currents are detected when the amplitude of input voltage V_{IN} exceeds the trip voltage V_T (DC) for longer than the input detection time t_{MA}.
- The output current is used to turn on the thyristor that opens the breaker contacts.

WAVEFORM DIAGRAM



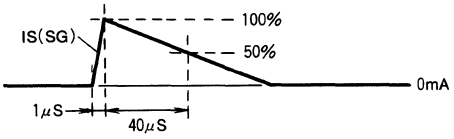
* t_{MA} : MA input detection time
t_{CO} : MA detector on time
t_{MB} : MB input detection time
t_{OS} : OS output pulse width (MB detector on time)

Note. The values in the parentheses are typical values for reference only.

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+80℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
I_S	Supply voltage		8	mA
$I_{S(SG)}$	Supply surge current	(Note 1)	12	mA
I_{IN}	Input current	Between IN and VR (Note 2)	−250∼+250	mA
I_{IG}	Input pin current	Between VR and GND, and between IN and GND	30	mA
V_{OD}	OD applied voltage	When external voltage is applied	6	V
I_{MA}	MA input current	When external voltage is applied	4	mA
V_{OS}	OS applied voltage	When external voltage is applied	6	V
P_d	Power dissipation		200	mW
T_{opr}	Operating temperature		−20∼+80	℃
T_{str}	Storage temperature		−55∼+125	℃

Note 1 : The surge waveform The waveform of surge current $I_{S(SG)}$ is shown on the left It is applied less than once per minute



Note 2 : Applies to currents between IN and VR with pulse widths less than 1 ms and duty cycles less than 12% If AC current is applied, the current limit is 100mArms when the IC supply power is off

Remark : Circuit voltage at GND pin is 0 V Current flowing into the circuit is positive (no sign) and the current flowing out from the circuit is negative (negative sign), unless otherwise noted Maximum values of rated and specified values are shown in absolute values

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+80℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_S	Supply voltage when output is off	12			V
C_{VS}	Capacitance between VS and GND	1			μF
C_{OS}	Capacitance between OS and GND			1	μF
C_{MA}	Capacitance between MA and GND		0.1		μF
C_{MB}	Capacitance between MB and GND		0.1		μF
R_{IN}	External resistor at IN		100		Ω

ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V, T_a=−20∼+80℃, unless otherwise noted)

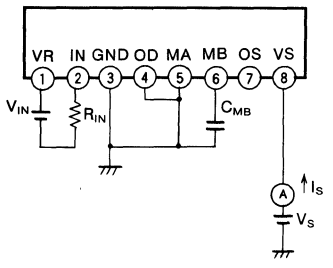
Symbol	Parameter	Test condition	Temperature (℃)	Limits			Unit	Test circuit
				Min	Typ	Max		
I_S	Supply current	V_S=12V, V_{IN}=−15mV				800	μA	1
V_T	Trip voltage	V_S=16V, V_{IN} : 60Hz sine wave		4		9	mVrms	2
I_{ODL}	OD sink current	V_S=16V, V_{IN}=0mV, V_{OD}=4V	25	120		240	μA	3
I_{ODH}	OD source current	V_S=16V, V_{IN}=−15mV, V_{OD}=4V	25	−75		−150	μA	3
V_{MAH}	MA on voltage	V_S=16V, V_{IN}=−15mA	25	2.8		3.4	V	4
V_{MAL}	MA off voltage	V_S=16V, V_{IN}=−15mA	25	0.8		1.2	V	4
I_{MBL}	MB sink current	V_S=16V, V_{IN}=0mA, V_{MB}=1.6V	25	120		240	μA	5
I_{MBH}	MB source current	V_S=16V, V_{IN}=−15mA, V_{MB}=1.6V	25	−75		−150	μA	5
I_{OSL}	OS sink current	V_S=16V, V_{IN}=0mA, V_{OS}=0.2V		200			μA	6
I_{OSH}	OS source current	V_S=12V, V_{IN}=−15mA, V_{OS}=1.6V	−20	−200			μA	6
			+25	−100				
			+80	−75				
V_{SM}	VS maximum current voltage	I_S=7mA	25	20		30	V	7
V_{INC}	IN, VR input clamp voltage	V_S : open, I_{IN}=±100mA	25	±0.4		±2.0	V	8
V_{RCL}	VR clamp voltage	V_S=16V, I_{VR}=20mA	25	4.4		6.6	V	9
t_{MA}	MA input detection time	V_S=16V		1.7		4.0	ms	10
t_{CO}	MA detector on time	V_S=16V		40		100	ms	10
t_{MB}	MB input detection time	V_S=16V		1.7		4.0	ms	11
t_{OS}	OS input detection time	V_S=16V		60		150	ms	11

Note V_{IN} is the input voltage with V_R as reference V_{IN} is applied to IN through resistor R_{IN}

TEST CIRCUIT

(C_{MA}=0.1μF, C_{MB}=0.1μF, R_{IN}=100Ω, Diode are equivalent to MD234, unless otherwise noted)

1



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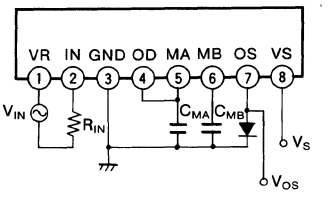
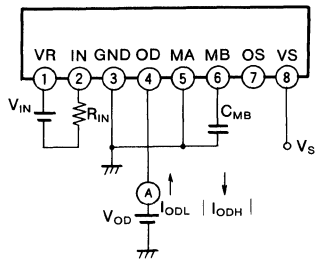


※ V_T is the value of V_{IN} at which OS turns on (V_{OS}>0.4V) as V_{IN} is increased gradually

3



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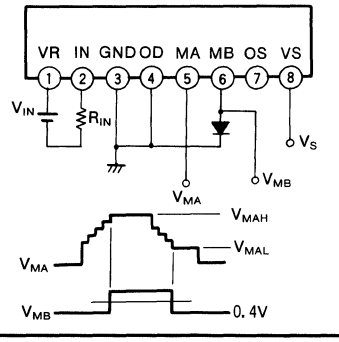

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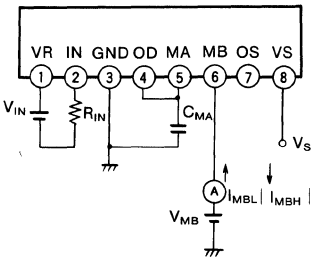

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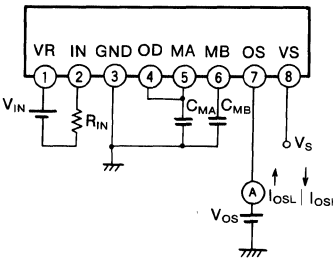

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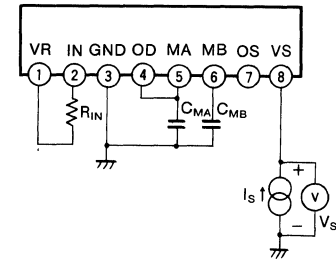

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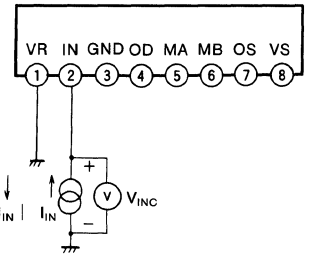

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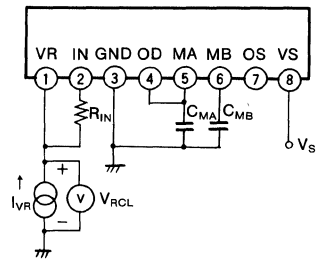

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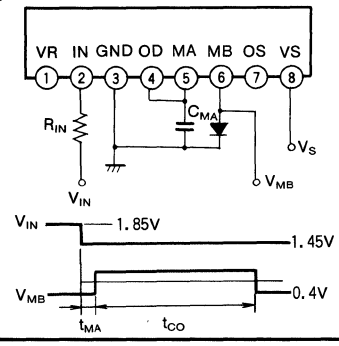

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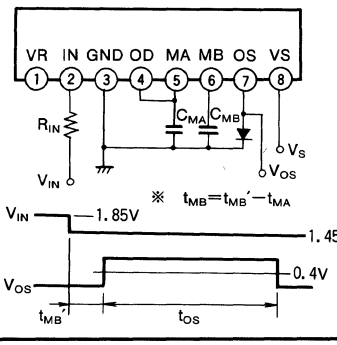
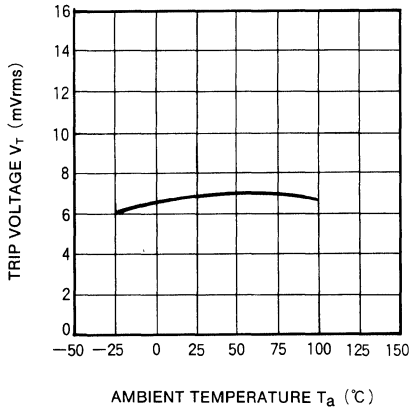


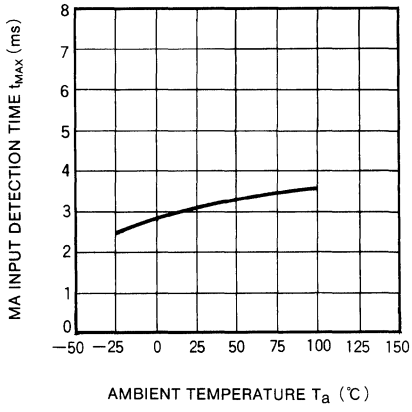
MITSUBISHI ELECTRIC

TYPICAL CHRACTERISTICS

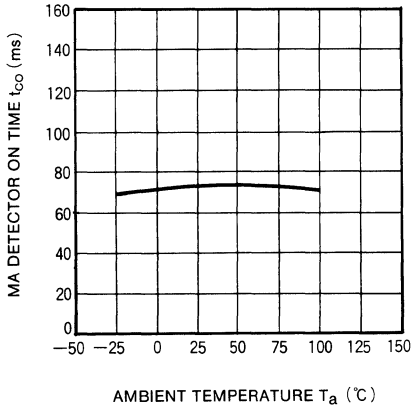
TRIP VOLTAGE VS AMBIENT TEMPERATURE



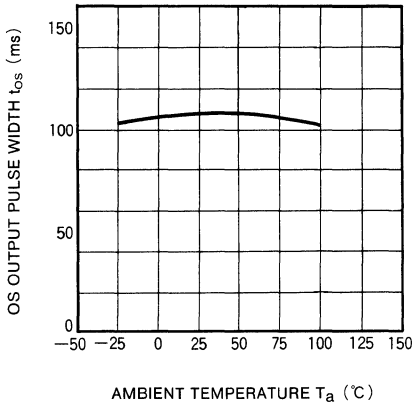
MA INPUT DETECTION TIME VS AMBIENT TEMPERATURE



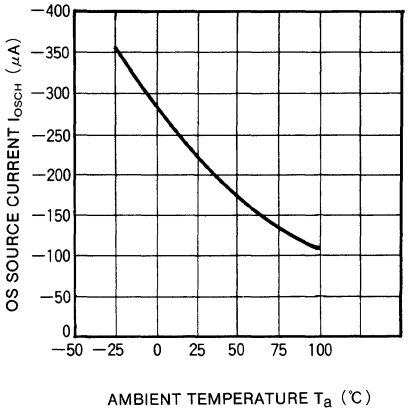
MA DETECTOR ON TIME VS AMBIENT TEMPERATURE



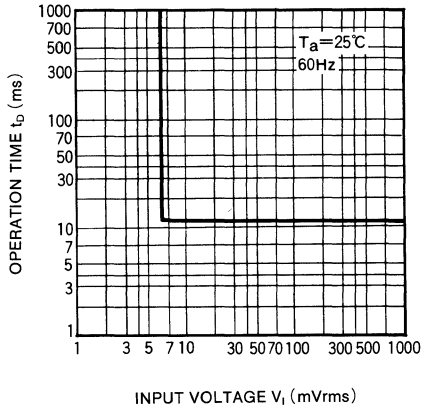
OS OUTPUT PULSE WIDTH VS AMBIENT TEMPERATURE



OS SOURCE CURRENT VS AMBIENT TEMPERATURE

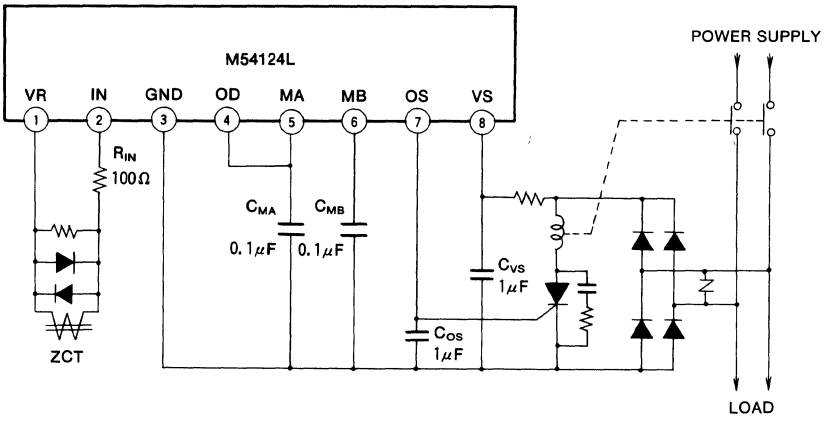


OPERATION TIME VS INPUT VOLTAGE



APPLICATION EXAMPLE

• A high-speed earth-leakage circuit breaker using the M54124L



M54125P

EARTH LEAKAGE CURRENT DETECTOR

DESCRIPTION

The M54125P is a semiconductor integrated circuit consisting of an amplifier for high-speed earth leakage circuit breaker.

FEATURES

- Satisfies JIS C 8371
- Temperature-stable input current trigger threshold (V_{LKT} =9mV)
- Capable of detecting a lost phase on the neutral line
- Economical, low external component count
- Highly resistant to noise and power surges
- Wide operating temperature range (T_a=−20∼+80℃)

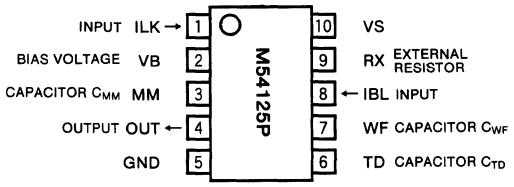
APPLICATION

High-speed earth-leakage circuit breakers

FUNCTION

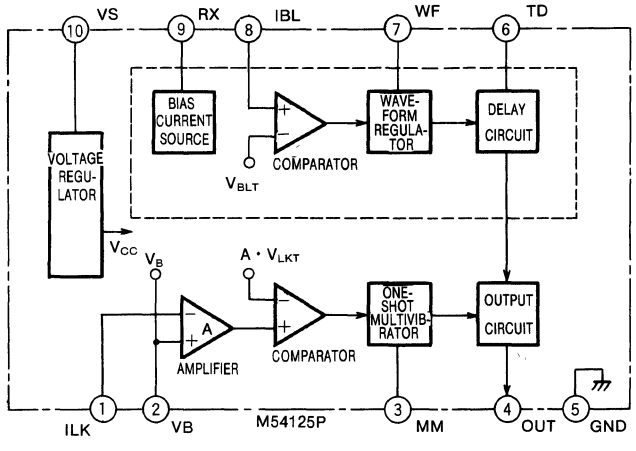
The M54125P is a semiconductor integrated circuit for use in the amplifier section of earth-leakage circuit breakers. It consists of a differential amplifier, one-shot circuit, output circuit, current regulator, waveform regulator and delay circuit. The following description refers to the block diagram, application example, and operational waveforms.

PIN CONFIGURATION (TOP VIEW)



Outline 10P2-C

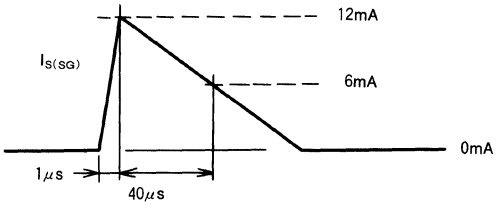
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+80℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
I_S	Supply voltage	Average supply current frequency per cycle	0∼6	mA
$I_{S(SG)}$	Supply surge current	(Note 1)	0∼12	mA
ΔV_{ILK}	ILK Input voltage	Pin VB serves as the voltage reference.	−1.8∼+1.8	V
V_{IBL}	IBL Input voltage		−0.3∼6	V
V_{OUT}	OUT applied voltage	When external voltage is applied	−0.3∼4	V
P_d	Power dissipation		160	mW
Topr	Operating temperature		−20∼+80	℃
Tstg	Storage temperature		−55∼+125	℃

Note 1 : The surge current waveform $I_{S(SG)}$ is shown below It is applied less than once per minute



RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+80℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage	When output OUT is OFF	12			V
I_S	Supply current	Average power supply current per cycle			5.6	mA
C_{MM}	External capacitor MM			0.22		μF
C_{WF}	External capacitor WF			1		μF
C_{TD}	External capacitor TD			6.8		μF
R_X	External resistor R_X			27		kΩ

Handling of unused pins when the abnormal voltage detection function is not used

- Pin 9 R_X must be left open
- Pin 6 TD must be shorted to GND
- Pin 7 WF and pin 8 IBL may be left open or shorted to GND

LEAKAGE DETECTION FUNCTION

When leakage current current Ig appears on the primary side of zero-current transformer, ZCT, leakage signal voltage V_{ILK} appears on the secodary side and is input at ILK with bias VB as the reference. In the half cycle when V_{ILK} is negative, capacitor C_{MM} connected to MM charges until V_{ILK} reaches the DC trip voltage.

If the voltage at MM does not reach the MM positive threshold voltage, when the charging phase is completed, capacitor C_{MM} discharges at a small current. The output OUT is reset to the off state (in which output current flows in) when V_{MM} descends to the MM negative threshold voltage.

Earth-leakage currents are detected when the amplitude of input voltage V_{ILK} exceeds the DC trip voltage V_{LKT} for longer than the detection time t_{MM}. The output OUT turns on for time t_{OUT}. The output current is used to turn on the thyristor that opens the breaker contacts.

ABNORMAL VOLTAGE DETECTION FUNCTION

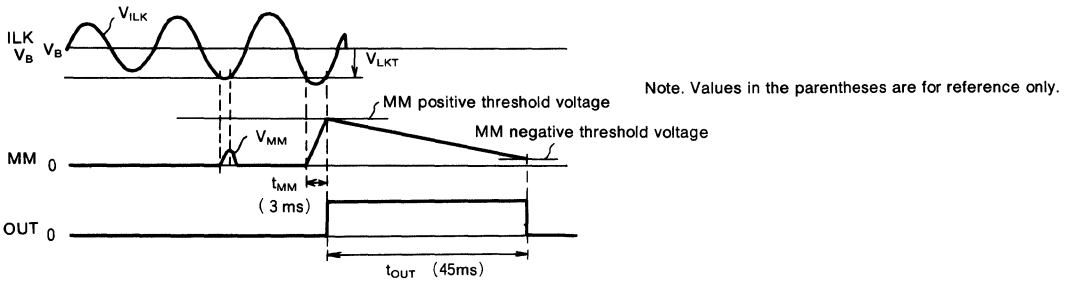
Normally V_{IBL}, fixed amplitude AC supply that has been rectified and divided by a resistor, is input to abnormal voltage input IBL. When a fault occurs in the neutral line N, successive peaks of V_{IBL} become alternately small and large, with the levels determined by the load on the AC power lines A and B.

When the amplitude of V_{IBL} exceeds the abnormal voltage trip voltage V_{BLT}, capacitor C_{WF} connected to pin WF discharges. After the discharge shase is completed, charging begins again.) When voltage V_{WF} at WF drops below the WF threshold voltage, capacitor C_{TD} at TD charges, and after delay time t_{TD}, when voltage V_{TD} at TD reaches the TD threshold voltage, output OUT turns on, activating the circuit breaker. To avoid misoperation due to the effect of repeated one-shot noise that brings V_{IBL} above V_{BLT}, the voltage drops to the initial value only after time t_{WF}.

This abnomal voltage detection circuit is enabled only when an external resistor R_X is connected to pin R_X to enable the current flow.

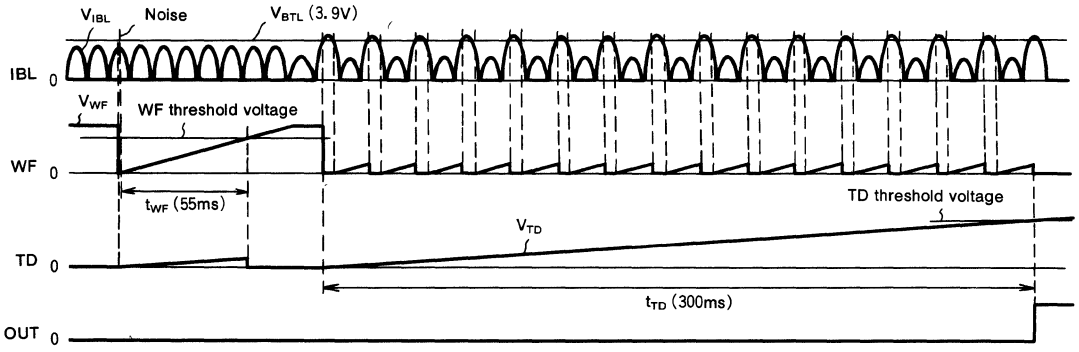
WAVEFORM DIAGRAM

1) Voltage waveform when earth leakage is detected.



Note. Values in the parentheses are for reference only.

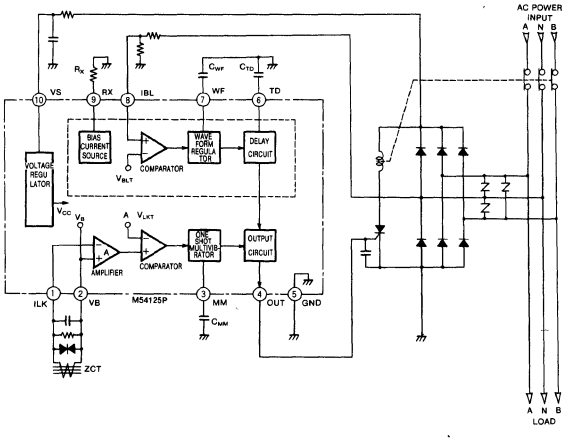
2) Voltage waveform when abnormal voltage is detected.



ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V, T_a=−20∼+80℃, unless otherwise noted)

Symbol	Parameter		Test condition	Temperature (℃)	Limits			Unit	Test circuit
					Min	Typ	Max		
I_{S1}	Supply current 1	Pin VS	V_S=12V, ΔV_{ILK}= 0 mV Out : "OFF"				0.7	mA	1
I_{S2}	Supply current 2	Pin VS	V_S=16V, ΔV_{ILK}=−15mV Out : "ON"				1.2	mA	1
V_{LKT}	Trip voltage	Pins ILK and VB	V_S=16V, V_{LKT} : 60Hz Test circuit 3		4		9	mVrms	
I_{MM+}	Sink current	Pin MM	V_S=16V, ΔV_{ILK}= 0 mV V_{MM}=0.8V	25	170		370	μA	4
I_{MM-}	Source current	Pin MM	V_S=16V, ΔV_{ILK}=−15mV V_{MM}=0.8V	25	−110		−250	μA	4
t_{MM}	Detect inhibit time	Pin MM	V_S=16V		1.7		4	ms	10
I_{OU+}	Sink current	Pin OUT	V_S=16V, ΔV_{ILK}= 0 mV V_{OUT}=0.2V		150			μA	5
I_{OU-}	Source current	Pin OUT	V_S=16V, ΔV_{ILK}=−15mV V_{OUT}=0.8V	−20	−200			μA	5
				25	−100				
				80	−70				
t_{OUT}	Output pulse width	Pin OUT	V_S=16V		25		100	ms	10
V_{SM}	Maximum current voltage	Pin VS	I_S=3.5mA	25	20		26	V	6
I_{S3}	Supply current 3	Pin VS	V_S=12V, V_{ILK} : 0 mV V_{IBL}= 0 V, OUT : "OFF" Test circuit 2				1	mA	
I_{S4}	Supply current 4	Pin VS	V_S=12V, V_{ILK} : −15mV V_{IBL}=12V, OUT : "ON" Test circuit 2				1.4	mA	
V_{BLT}	Trip voltage	Pin IBL	V_S=16V		3.6		4.1	V	7
I_{IBL}	Input current	Pin IBL	V_S=16V, V_{IBL}=4.5V Test circuit 7	25			0.8	μA	
I_{WF+}	Sink current	Pin WF	V_S=16V, V_{IBL}=4.5V V_{WF}=0.5V	25	1			mA	8
I_{WF-}	Source current	Pin WF	V_S=16V, V_{IBL}= 0 V V_{WF}=0.5V	25	−22		−30	μA	8
t_{WF}	Recovery time	Pin WF	V_S=16V		35		70	ms	11
I_{TD+}	Sink current	Pin TD	V_S=16V, V_{IBL}= 0 V V_{TD}=0.5V	25	1			mA	9
I_{TD-}	Source current	Pin TD	V_S=16V, V_{IBL}=4.5V V_{TD}=0.5V	25	−22		−30	μA	9
t_{DT}	Delay time	Pin TD	V_S=16V		200		420	ms	12

APPLICATION EXAMPLE

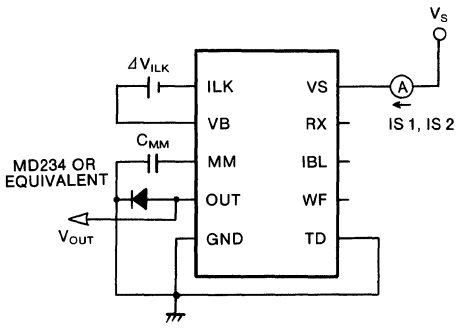


MITSUBISHI ELECTRIC

TEST CIRCUIT

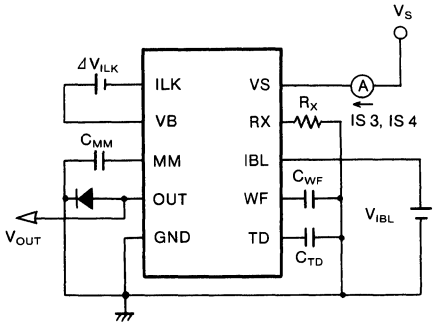
(C_{MM}=0.22μF, CTD=6.8μF, R_X=27kΩ, unless oterwise noted)

1 • IS 1, IS 2 Measurement



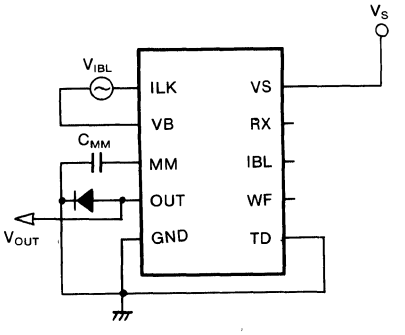
* : IS 2 is the value after OUT turns on (V_{OUT}>0.5V).

2 • IS 3, IS 4 Measurement



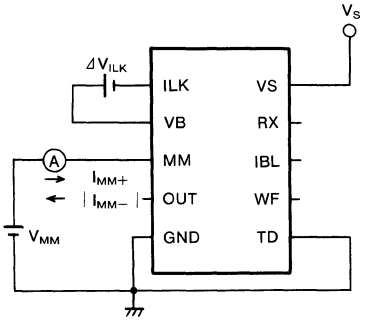
* : IS 4 is the value after OUT turns on

3 • V_{LKT}

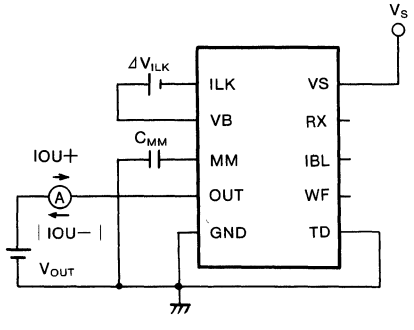


* : V_{LKT} is the value of V_{IBL} when OUT turns on as V_{IBL} is gradually increased

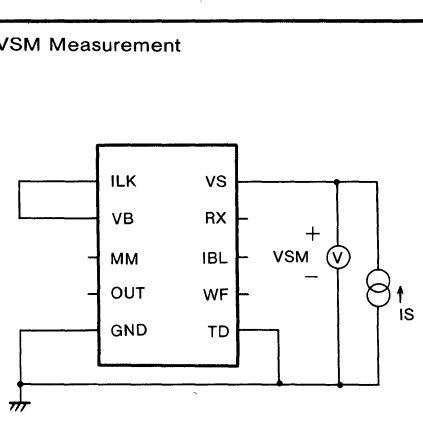
4 • I_{MM+}, I_{MM-} Measurement



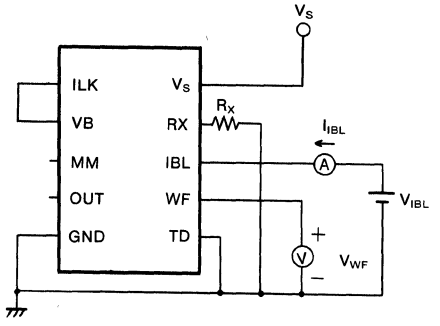
5 • IOU+, IOU− Measurement



6 • VSM Measurement

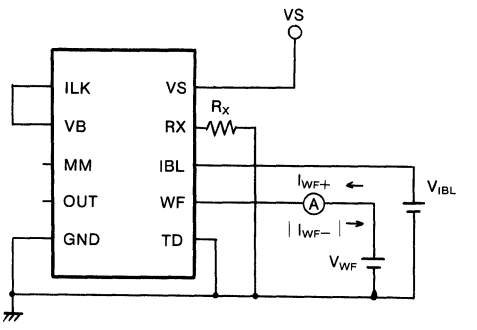


7 • V_{BLT}, I_{IBL} Measurement

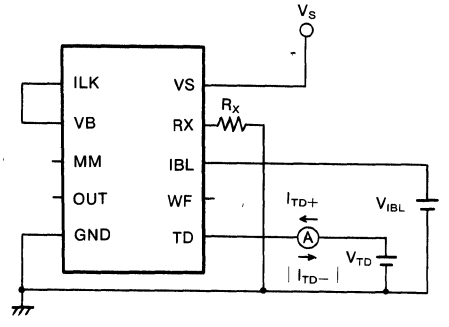


* : V_{BLT} is the value of V_{IBL} when VF=0.5V

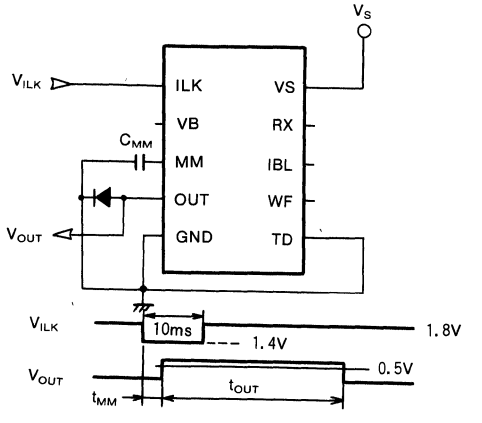
8 • I_{WF+}, I_{WF-} Measurement



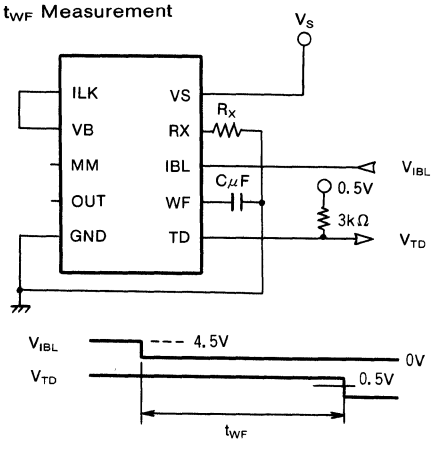
9 • I_{TD+}, I_{TD-} Measurement



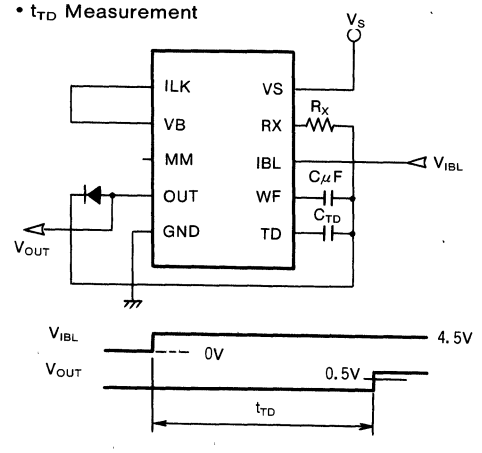
10 • t_{MM}, t_{OUT} Measurement



11 • t_{WF} Measurement



12 • t_{TD} Measurement



MITSUBISHI ELECTRIC

M54193P/AP/BP

TELEPHON TONE RINGER

DESCRIPTION

The M54193P/AP/BP is a semiconductor integrated circuit consisting of a tone ringer for telephone handsets. The device withstands a maximum input voltage of 50V and is capable of $45V_{P-P}$ output.

FEATURES

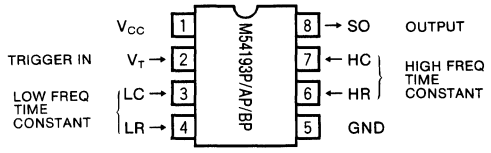
- Output voltage $45V_{P-P}$
- Built-in anti-resonance circuit
- Variable oscillation frequency
- Built-in circuit prevents misoperation due to power supply noise
- Built-in output compulsory turn off function, by means of drop voltagd detection circuit. (M54193P/M54193AP)

(When V_{CC} is less than V_{OFF} *, output is compulsoily set to "L" level, therefore tone cut off is improved
* : V_{OFF}=26V at M54193
V_{OFF}=18.5V at M54193)

APPLICATION

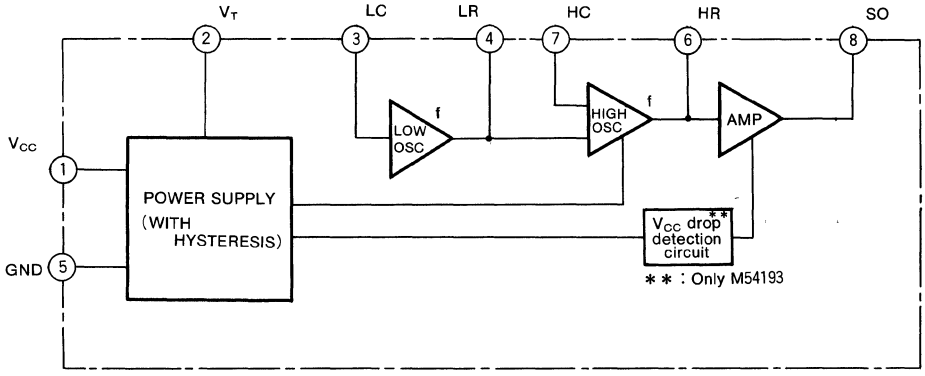
Analog telephone handsets

PIN CONFIGURATION (TOP VIEW)



Outline 8P4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		50	V
I_{SO}	Output current		±10	mA
P_d	Power dissipation	T_a=25℃	625	mW
		T_a=75℃	300	
Topr	Ambient operating temperature		−25∼+75	℃
Tstg	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

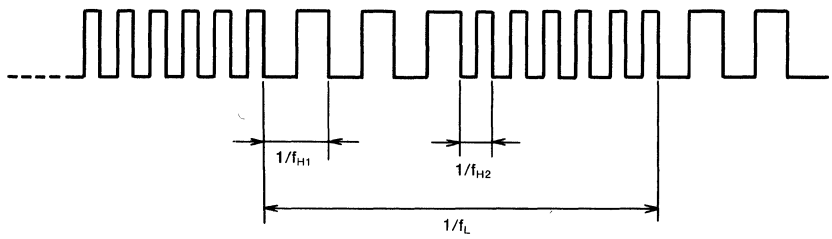
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage				50	V
I_{SO}	SO output current				±5	mA
C_L	External capacitor for low OSC		3900	56000	470000	pF
R_L	External resister for low OSC		100	1000	1800	kΩ
C_H	External capacitor for high OSC		1000	3900	6800	pF
R_H	External resister for high OSC		100	330	1800	kΩ

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Operating voltage				50	V
V_{si}	Startup voltage	(Note 1)	17	20	23	V
V_{sus}	Sustaing voltage	(Note 2)	10	12	16	V
I_{si}	Startup current	V_{CC}=V_{SI}	2.3	3.3	4.8	mA
I_{sus}	Operation sustaing current	V_{CC}=V_{sus}	0.7	1.1	1.6	mA
V_{TR}	Trigger voltage			10		V
V_O	Output voltage	V_{CC}=V_{sus}∼V_{OFF} M54193P, M54193AP			1.8	V
		V_{CC}=V_{OFF}∼50V M54193P, M54193AP	V_{CC}−5	V_{CC}−2	V_{CC}−1	
		V_{CC}=V_{sus}∼V_{OFF} M54193BP	V_{CC}−5	V_{CC}−2	V_{CC}−1	
f_O	Oscillator frequency accuracy	V_{CC}=25V C_L=56000pF, R_L=100kΩ C_H=3900pF, R_H=330kΩ	−7		+7	%
I_{CC}	Supply current	V_{CC}=50V	1.6	2.4	3.2	mA
V_{OFF}	Output compulsion off voltage	M54193P	24	26	28	V
		M54193AP	16.5	18.5	20.5	
V_{ON}	Output on voltage	M54193P	25	27	29	V
		M54193AP	18	20	22	

Note 1 : The startup voltage is the supply voltage at which the tone ringer initiates oscillation.
2 : The sustaining voltage is the supply voltage required to sustain the oscillation

SO OUTPUT WAVEFORM



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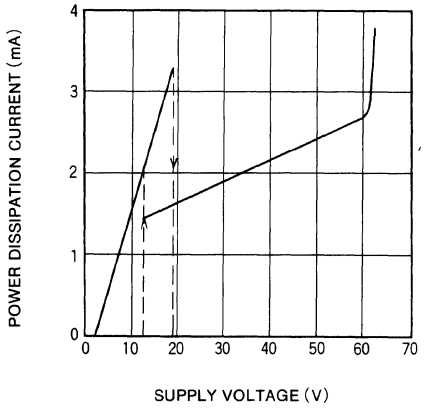
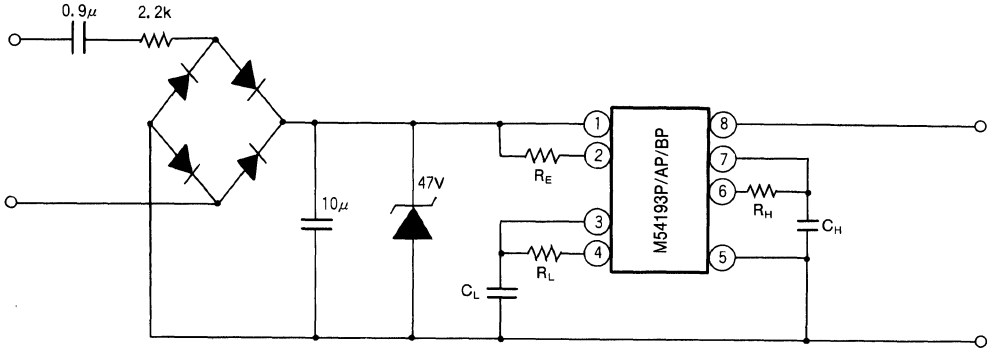
TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE VS POWER DISSIPATION CURRENT



APPLICATION EXAMPLE



OSCILLATOR FREQUENCY SETTING

$$f_L = \frac{1}{1.657 \cdot C_L \cdot R_L} \text{ (Hz)}$$

$$f_{H1} = \frac{1}{1.515 \cdot C_H R_H} \text{ (Hz)}$$

$$f_{H2} = 1.24 f_{H1} \text{ (Hz)}$$

The oscillator frequencies f_L, f_{H1}, f_{H2} are determined by the above equations

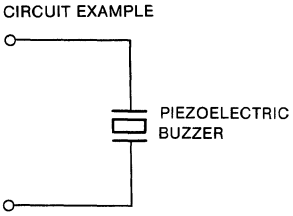
(Example) R_L=1000kΩ R_H=330kΩ

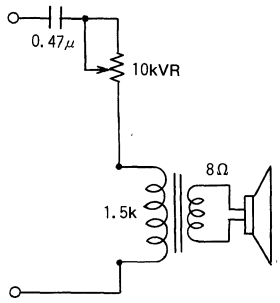
C_L=56000pF C_H=3900pF

$f_L \fallingdotseq 10.8$Hz $f_{H1} \fallingdotseq 513$Hz

$f_{H2} \fallingdotseq 636$Hz

OUTPUT CIRCUIT EXAMPLE





USE OF TRIGGER IN (PIN 2)

Normally TRIGGER IN is left open, but it can be used to inhibit oscillation or alter the startup voltage (V_{Si}).
When the M54193P is oscillating ($V_{SUS} < V_{CC} < 30V$), it can be stopped by connecting pin 2 to potential V_I through resistance R_I. (V_{SUS} is the startup voltage.)

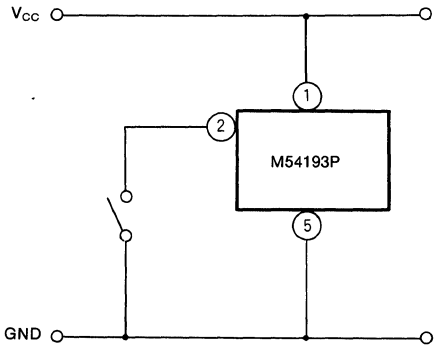
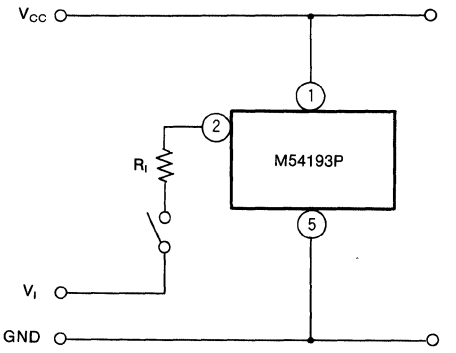


Fig 1



$0 \leqq V_I \leqq 0.5V$
$0 \leqq R_I \leqq 20k\Omega$

Fig 2

When $V_{SUS} < V_{CC} < V_{Si}$, the oscillation of the M54193P can be initiated by I_E ($10\mu A < I_E < 1$ mA) from pin 2.
(V_{Si} is the startup voltage.)
To start the oscillation at a lower voltage than the startup voltage, pin 2 is connected to V_{CC} through R_E as shown in Fig. 3.
R_E must satisfy the condition :

$$10k\Omega < R_E < \frac{(Vsi-10)}{10} (M\Omega)$$

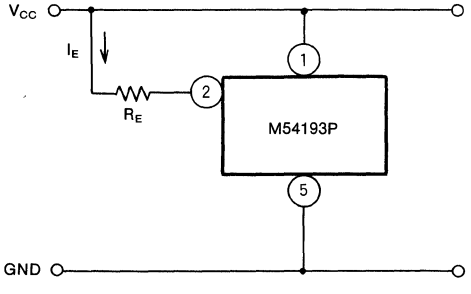


Fig 3

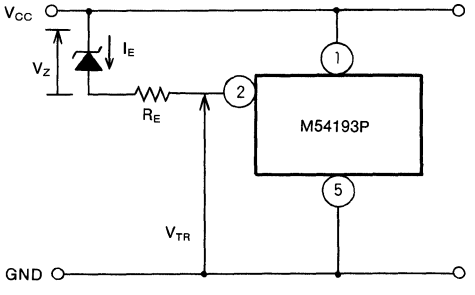


Fig. 4

Use of a Zener diode can alter V_{Si}, in which case, V_{Si} is determined by :
$V_{Si} = V_{TR} + V_Z + 10R_E$ (R_E : MΩ)

M54403P

5-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER WITH RESET

DESCRIPTION

The M54403P is a semiconductor integrated circuit containing a 5-bit serial/parallel input serial/parallel output reversible shift register.

FEATURES

- Serial/parallel input——serial/parallel output
- Depending on external connections shift left function possible
- Mode control input provided

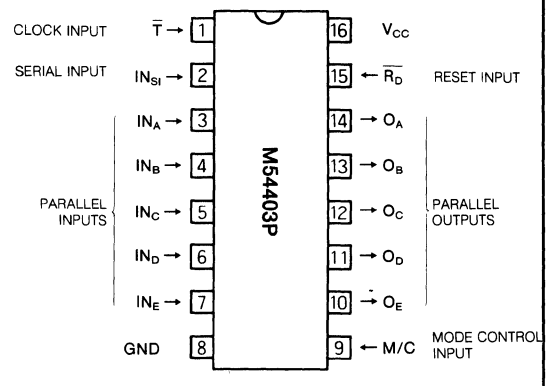
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

This 5-bit shift register consists of 5 R-S-T flip-flops. It functions as either a serial-in/serial (parallel)-out or a parallel-in/parallel-out register depending on the condition of mode control input (M/C). When mode control input (M/C) is maintained in "L" with serial datum applied to serial input (IN_{SI}), it functions as a right-shift register and data can be read from outputs ($O_A \sim O_E$). Mode control input (M/C) maintained in "H", parallel data applied to parallel input ($IN_A \sim IN_E$), one bit of clock pulse is applied to clock input ($\overline{T}$), and then the parallel data appear at the outputs ($O_A \sim O_E$). Set mode control input in "H", apply serial datum to IN_E, connect O_E and IN_D, O_D and IN_C, O_C and IN_B, O_B and IN_A respectively, and it functions as a left-shift register.

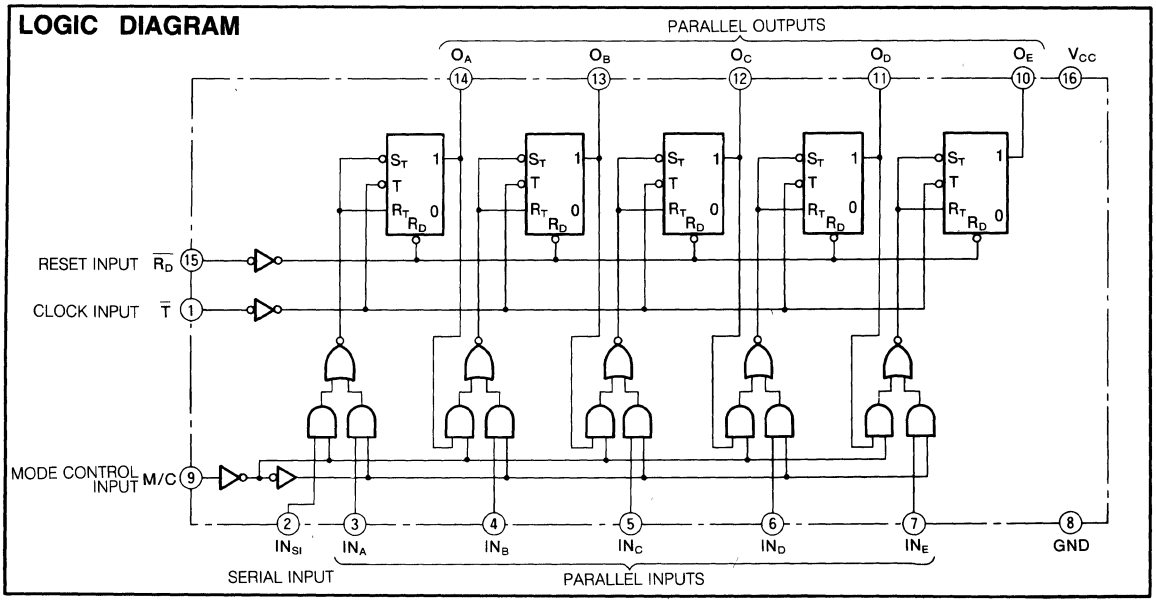
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

When clock input ($\overline{T}$) changes from "H" to "L", data are shifted one bit or parallel data are read. When reset input ($\overline{R_D}$) is "L", all outputs ($O_A \sim O_E$) are set "L" irrespective of other input signals.

LOGIC DIAGRAM



5-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER WITH RESET

FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{R_D}$	M/C	$\overline{T}$	IN_{SI}	IN_A	IN_B	IN_C	IN_D	IN_E	O_A	O_B	O_C	O_D	O_E
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	↑	H	X	X	X	X	X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	L	↑	L	X	X	X	X	X	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	↑	X	a	b	c	d	e	a	b	c	d	e

X : Irrelevant (any input, including transition).
↑ : Transition from "L" to "H".
Q_{A0}, Q_{B0}, etc. : The level of Q_A, Q_B, etc. respectively, before the ↑ transtion of the clock
a, b, c, d, e : The level of steady-state input at inputs A, B, C, D, or E, respectively.

ABSOLUTE MAXIMUM RATINGS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage	High-Level output	V_{CC}	V
P_d	Power dissipation		800	mW
T_{opr}	Operating temperature		0~75	℃
Tstg	Storage temperature		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
F_O	Fan out			10	—
$f_{max(\overline{T})}$	Maximum clock frequency (clock input ($\overline{T}$))	0		10	MHz

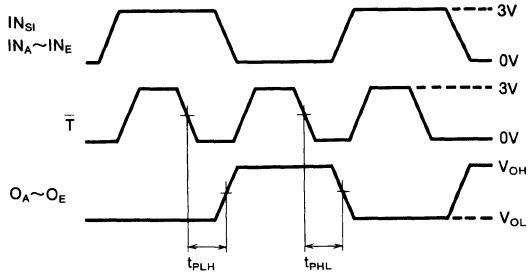
ELECTRICAL CHARACTERISTICS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −12mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V I_{OH} = −400μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current	V_{CC} = 5.25V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−1.6	mA
I_{OS}	Short-circuit output current	V_{CC} = 5.25V, V_I = 4.5V, V_I = 0V, V_O = 0V		−18		−57	mA
I_{CC}	Supply current	V_{CC} = 5.25V, V_I = 4.5V, V_I = 0V				102	mA

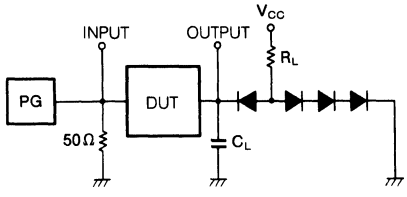
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF, R_L = 400Ω (Note 1)	10			MHz
t_{PHL}	High-to-low-level and Low-to-high-level propagation delay from clock input $\overline{T}$, to outputs O_A through O_E				35	ns
t_{PLH}					35	ns

TIMING DIAGRAM (Reference level = 1 5V)



Note 1 : Test circuit



1 The pulse generator (PG) characteristics ($\overline{T}$) · $t_r \leqq 10ns$, $t_f \leqq 10ns$, PRR = 1MHz, $t_{PW} \geqq 15ns$, $V = 3V_{P-P}$, $Z_O = 50\Omega$
The pulse generator (PG) characteristics (IN) . $t_r \leqq 10ns$, $t_f \leqq 10ns$, PRR = 500kHz, $t_{PW} \geqq 20ns$, $V = 3V_{P-P}$, $Z_O = 50\Omega$.
2. All diodes used are high-speed switching diodes ($t_{rr} \leqq 4ns$).
3. C_L includes probe and jig capacitance

M54405P

4-BIT BINARY-TO-SEVEN-SEGMENT DECODER/DRIVER

DESCRIPTION

The M54405P is a semiconductor integrated circuit with a 4-bit binary-to-seven-segment decoder/driver. It contains a TTL open collector output driver.

FEATURES

- High output breakdown voltage (V_O=15V)
- Output current (I_O=16mA)
- Displays 16 characters (0, 1~9, A, b, C, d, E, F)
- Zero-suppression input/output ($\overline{RBI}$, $\overline{BI/RBO}$)
- Lamp-test ($\overline{LT}$) provided

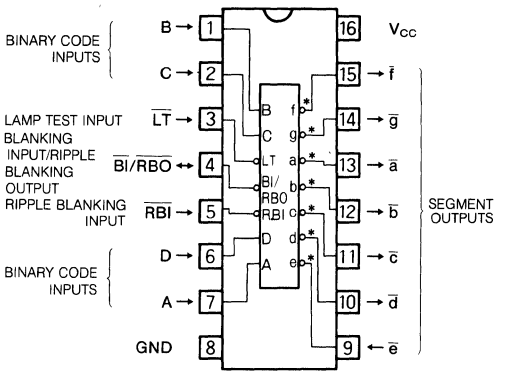
APPLICATION

General-purpose industrial and consumer electronic digital equipment.

FUNCTION

The M54405P is a 4-bit binary-to-7-segment decoder/driver which can directly drive a mosaic type of display tube. In particular, it features English alphabet indication when numbers 10~15 are applied to inputs A, B, C and D in 4-bit pure binary code. The circuitry employs a TTL configuration and open collector outputs (15V breakdown voltage, 16mA load current, active low) are used in the output stage so that a display tube can be lighted directly. Auxiliary inputs include the lamp test input ($\overline{LT}$) which lights all the segments, regardless of the status of the inputs, the blanking input ($\overline{BI/RBO}$) that blanks the segments, and the ripple blanking input ($\overline{RBI}$) which blanks the segments only with a decimal "0" and which can be used for zero masking.

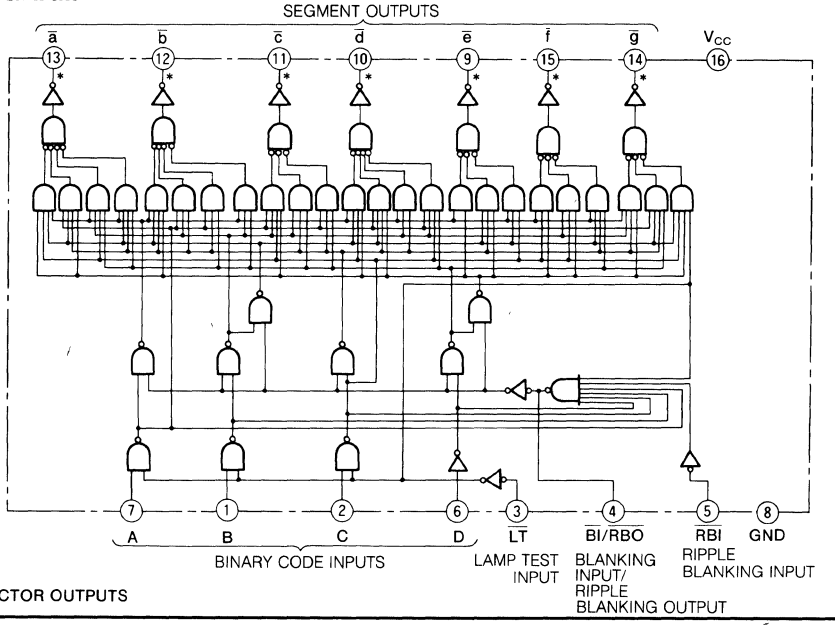
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

* : OPEN COLLECTOR OUTPUTS

LOGIC DIAGRAM



* : OPEN COLLECTOR OUTPUTS

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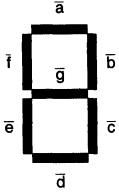
FUNCTION TABLE

Decimal number of function	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$		$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	Note
0	H	H	L	L	L	L		H	L	L	L	L	L	L	H	1
1	H	X	L	L	L	H		H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L		H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H		H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L		H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H		H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L		H	L	H	L	L	L	L	L	
7	H	X	L	H	H	H		H	L	L	L	H	H	L	H	
8	H	X	H	L	L	L		H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H		H	L	L	L	L	H	L	L	
10	H	X	H	L	H	L		H	L	L	L	H	L	L	L	
11	H	X	H	L	H	H		H	H	H	L	L	L	L	L	
12	H	X	H	H	L	L		H	L	H	H	L	L	L	H	
13	H	X	H	H	L	H		H	H	L	L	L	L	H	L	
14	H	X	H	H	H	L		H	L	H	H	L	L	L	L	
15	H	X	H	H	H	H		H	L	H	H	H	L	L	L	
Blanking	X	X	X	X	X	X	L		H	H	H	H	H	H	H	2
Ripple blanking	H	L	L	L	L	L		L	H	H	H	H	H	H	H	3
Lamp test	L	X	X	X	X	X		H	L	L	L	L	L	L	L	4

Note 1 : $\overline{LT}$ is normally kept high
$\overline{RBI}$ should be kept open or high with a decimal 0 output.
2 : When $\overline{BI}$ is low, all the segment outputs are set high regardless of the status of the other inputs.
3 : When $\overline{RBI}$, A, B, C, D are low, all the segment outputs are set high and $\overline{BI/RBO}$ is set low.
4 : When $\overline{LT}$ is low, all the segment outputs are set low.
5 : X Irrelevant.

DEFINITION OF SEGMENTS



SEGMENT IDENTIFICATION

Hexadecimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F

ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
I_O	Output current	Output high	1	mA
P_d	Power dissipation		500	mW
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_O	Output breakdown voltage	Outputs $\overline{a}$∼$\overline{g}$			15	V
I_{OL}	Low-level state output current	Outputs $\overline{a}$∼$\overline{g}$			16	mA
F_O	Fan out	Outputs $\overline{BI/RBO}$			5	—

ELECTRICAL CHARACTERISTICS (T_a = −20~+70℃, unless otherwise noted)

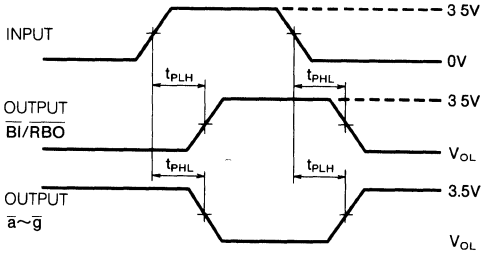
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −12mA			−1.5	V
I_{OH}	High-level output current ($\bar{a}$~$\bar{g}$)	V_{CC} = 5.25V, V_{IH} = 2V, V_{IL} = 0.8V V_{OH} = 15V			250	μA
V_{OH}	High-level output voltage ($\overline{BI}/\overline{RBO}$)	V_{CC} = 4.75V, I_{OH} = −0.2mA	2.4	3.3		V
V_{OL}	Low-level output voltage ($\bar{a}$~$\bar{g}$)	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA		0.22	0.4	V
V_{OL}	Low-level output voltage ($\overline{BI}/\overline{RBO}$)	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V I_{OL} = 8mA		0.22	0.4	V
I_{IH}	High-level input current (except $\overline{BI}/\overline{RBO}$)	V_{CC} = 5.25V, V_I = 2.4V			40	μA
I_{IL}	Low-level input current (except $\overline{BI}/\overline{RBO}$)	V_{CC} = 5.25V, V_I = 0.4V			−1.6	mA
I_{IL}	Low-level current ($\overline{BI}/\overline{RBO}$)	V_{CC} = 5.25V, V_I = 0.4V			−4.2	mA
I_{OS}	Output short-circuit current ($\overline{BI}/\overline{RBO}$)	V_{CC} = 5.25V			−4	mA
I_{CC}	Supply current	V_{CC} = 5.25V			90	mA

* : A typical value at T_a = 25℃

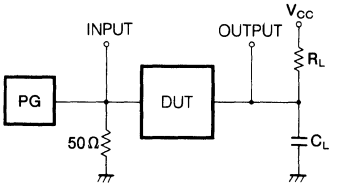
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}(A-$\bar{a}$)	Output low-to-high, high-to-low propagation time,	C_L = 15pF, R_L = 280Ω			130	ns
t_{PHL}(A-$\bar{a}$)	from input A, $\overline{RBI}$ to outputs $\bar{a}$ thru $\bar{g}$				130	ns

TIMING DIAGRAM (Reference level = 1.5V)



Note 6 : TEST CIRCUIT

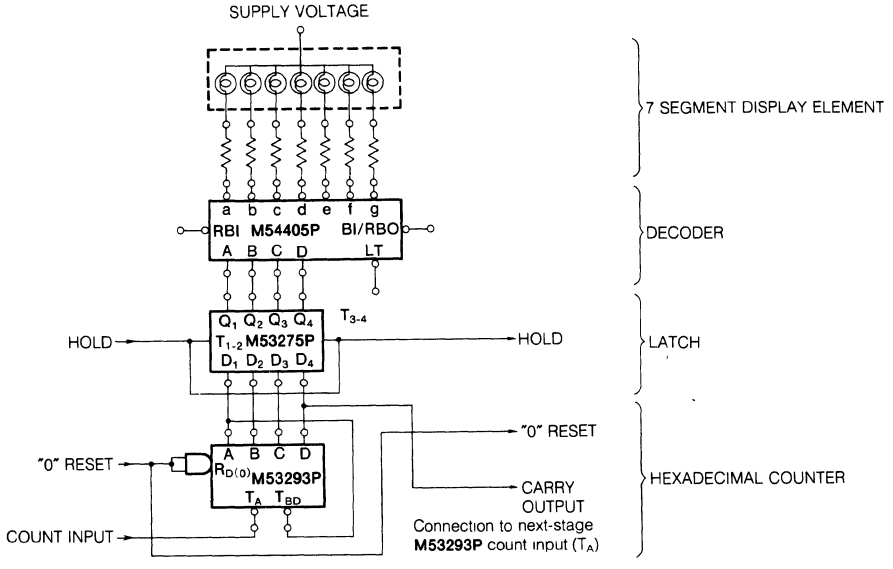


1. The pulse generator (PG) characteristics $t_r \leqq 10ns$, $t_f \leqq 10ns$, PRR = 1MHz, t_{PW} = 500ns, $V_P = 3.5V_{P-P}$, Z_O = 50Ω
2. C_L includes probe and jig capacitance.

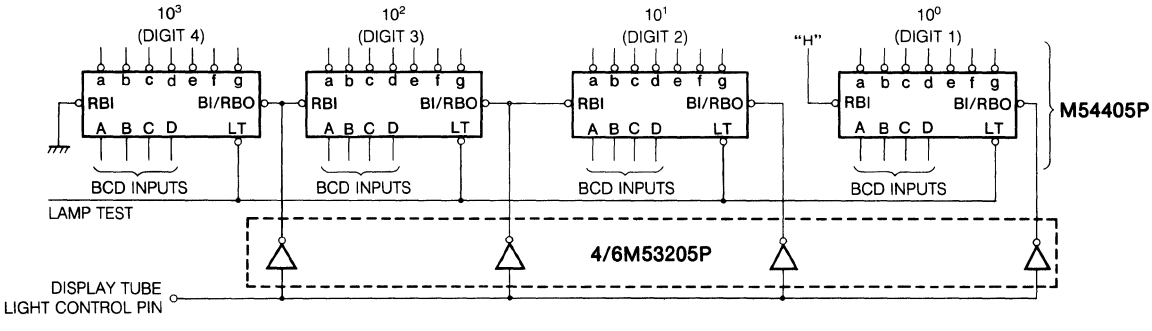
MITSUBISHI ELECTRIC

APPLICATION EXAMPLES

7-SEGMENT DISPLAY DRIVE CIRCUIT



ZERO SUPPRESSION AND LIGHT CONTROL



M54406P

BCD-TO-SEVEN-SEGMENT DECODER/DRIVER

DESCRIPTION

The M54406P is a semiconductor integrated circuit with a BCD-7-segment decoder/driver. It contains a TTL open collector output driver.

FEATURES

- High output breakdown voltage (V_O=15V)
- Output current (I_O=20mA)
- Characters 6, 7, 9 light a, f, d respectively.
- Zero-suppression input ($\overline{RBI}$) and input/output ($\overline{BI}$/$\overline{RBO}$) provided
- Lamp test ($\overline{LT}$) provided

APPLICATION

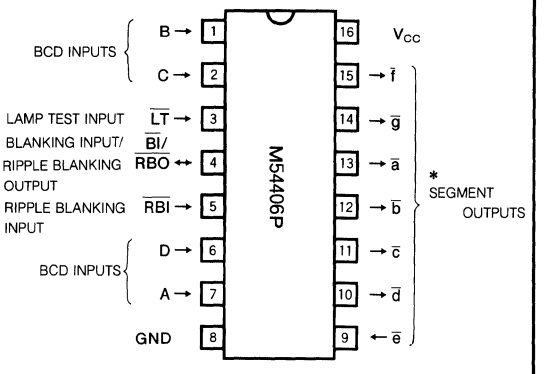
General-purpose industrial and consumer electronic digital equipment.

FUNCTION

When the BCD code is applied to the BCD inputs (A, B, C, D), the outputs ($\overline{a}$~$\overline{g}$) are set low in accordance with the numerical value and, by connecting 7-segment display devices to each of the outputs, it is possible to display the characters given in the section "Displayed Characters." Open collector outputs are used for outputs ($\overline{a}$~$\overline{g}$) and, since the breakdown voltage is equal to or greater than 15V and the low-level output current is 20mA, it is possible to drive directly a 7-segment LED used for anode-common numerical display.

It is possible to blank unnecessary high-order zeroes from significant numbers by setting the highest order input ($\overline{RBI}$) low and connecting the output ($\overline{BI}$/$\overline{RBO}$) to the next order input ($\overline{RBI}$) for each digit.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

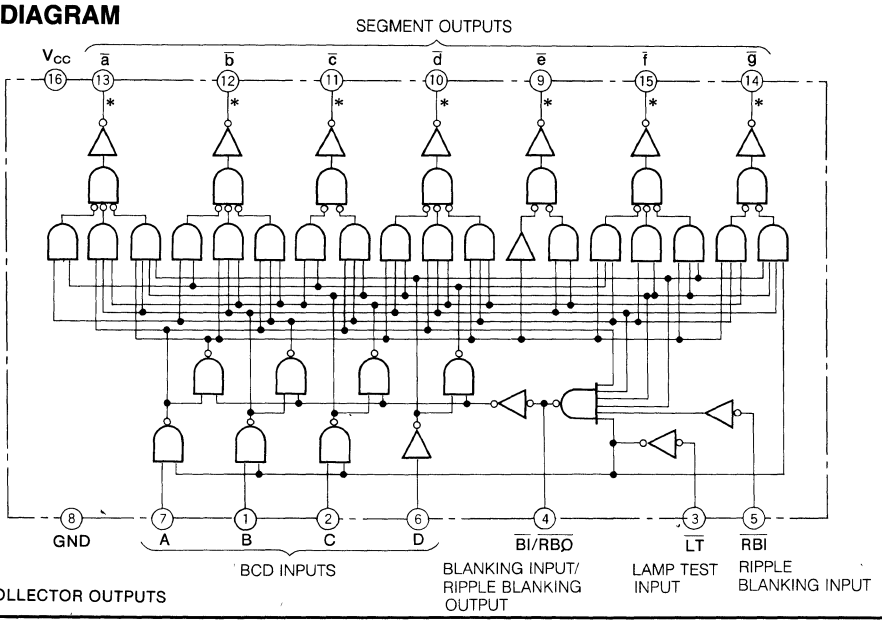
* : OPEN COLLECTOR OUTPUTS

When the blanking input ($\overline{BI}$/$\overline{RBO}$) is set low, the outputs ($\overline{a}$~$\overline{g}$) are set high regardless of the other inputs and the display device is extinguished.

The outputs ($\overline{a}$~$\overline{g}$) are set low, regardless of the inputs ($\overline{BI}$/$\overline{RBO}$, A, B, C, D), by setting the lamp test input ($\overline{LT}$) low, and the display device can be lighted and each segment tested.

Apart from numerals 6, 7 and 9, the M54406P is identical to the M53247P in terms of electrical characteristics and pin connections. For the application example, refer to the M53247P.

LOGIC DIAGRAM



* : OPEN COLLECTOR OUTPUTS

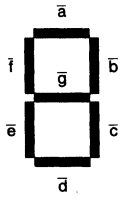
MITSUBISHI ELECTRIC

FUNCTION TABLE

Decimal number of function	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI}/\overline{RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	Note
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	1
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	L	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	L	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	L	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
Blanking	X	X	X	X	X	X	L	H	H	H	H	H	H	H	2
Ripple blanking	H	L	L	L	L	L	L	H	H	H	H	H	H	H	3
Lamp test	L	X	X	X	X	X	H	L	L	L	L	L	L	L	4

Note 1 : $\overline{LT}$ is normally kept high.
$\overline{RBI}$ is kept open or high with a decimal 0 output.
2 : When $\overline{BI}$ is low, all the segment outputs are high irrespective of the status of the other inputs
3 : When $\overline{RBI}$, A, B, C, D are low, all the segment outputs are set high and $\overline{BI}/\overline{RBO}$ is set low
4 : When $\overline{LT}$ is low, all the segment outputs are low
5 : X : Irrelevant

DEFINITION OF SEGMENTS



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character	0	1	2	3	4	5	6	7	8	9	c	ɔ	u	⊆	t	

ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output current	Output high ($\overline{a}$∼$\overline{f}$)	15	V
P_d	Power dissipation		500	mW
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_O	Output break down voltage	Outputs $\overline{a}$∼$\overline{g}$			15	V
I_{OL}	Low-level state output current	Outputs $\overline{a}$∼$\overline{g}$			20	mA
F_O	Fan out	Outputs $\overline{BI}/\overline{RBO}$			5	—

ELECTRICAL CHARACTERISTICS (T_a = −20∼+70℃, unless otherwise noted)

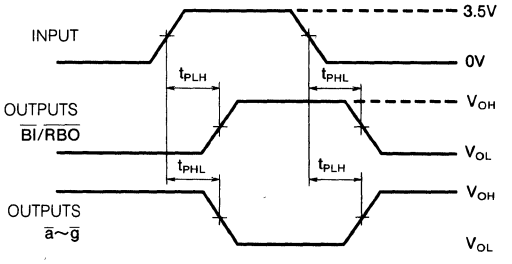
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage (except $\overline{BI}/\overline{RBO}$)	V_{CC} = 4.75V, I_{IC} = −12mA				−1.5	V
V_{OH}	High-level output voltage ($\overline{BI}/\overline{RBO}$)	V_{CC} = 4.75V, I_{OH} = −200μA		2.4	3.7		V
I_{OH}	High-level output current ($\overline{a}$∼$\overline{g}$)	V_{CC} = 5.25V, V_{IH} = 2V, V_{IL} = 0.8V V_{OH} = 15V				250	μA
V_{OL}	Low-level output voltage ($\overline{a}$∼$\overline{g}$)	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V I_{OL} = 20mA			0.27	0.4	V
V_{OL}	Low-level output voltage ($\overline{BI}/\overline{RBO}$)	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V I_{OL} = 8mA			0.3	0.4	V
I_{IH}	High-level input current (except $\overline{BI}/\overline{RBO}$)	V_{CC} = 5.25V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IL}	Low-level input current (except $\overline{BI}/\overline{RBO}$)	V_{CC} = 5.25V, V_I = 0.4V				−1.6	mA
I_{IL}	Low-level input current ($\overline{BI}/\overline{RBO}$)	V_{CC} = 5.25V, V_I = 0.4V				−4.2	mA
I_{OS}	Output short-circuit current ($\overline{BI}/\overline{RBO}$)	V_{CC} = 5.25V, V_O = 0V				−4	mA
I_{CC}	Supply current	V_{CC} = 5.25V			53	90	mA

* : A typical value at T_a = 25℃

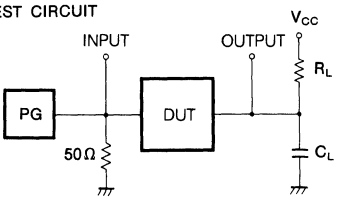
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Output low-to-high, high-to-low propagation time,	C_L = 15pF, R_L = 280Ω			100	ns
t_{PHL}	from input A, $\overline{RBI}$ to outputs $\overline{a}$ thru $\overline{g}$	(Note 6)			100	ns

TIMING DIAGRAM (Reference level = 1.5V)



Note 6 : TEST CIRCUIT



1. The pulse generator (PG) has the following characteristics · t_r ≦ 10ns, t_f ≦ 10ns, PRR = 1MHz, t_{PW} = 500ns, V_P = 3.5V_{P-P}, Z_O = 50Ω.
2. C_L includes probe and jig capacitance.

M54410P

KEY CONTROLLER FOR TAPE DECK

DESCRIPTION

The 54410P is a TTL integrated circuit semiconductor used for controlling the function keys on tape decks.

FEATURES

- Non-locking function keys can be used
- No need to prevent bounce
- Built-in pull-up resistors for input pins
- STOP mode set when power is switched on
- Wired-AND connection and transistor drive possible for output

APPLICATION

Tape decks, cassette recorders and VTRs

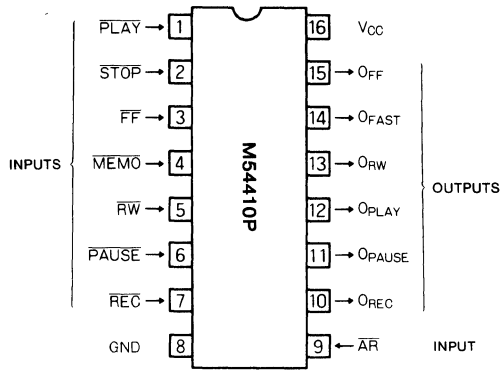
FUNCTION

The 54410P is configured so that the set and reset pins of the five R-S flip-flops serve as the input pins, and the desired tape mode is controlled by setting these input pins momentarily to low. Non-locking function keys can be used and there is no need to prevent bounce.

The input pins contain pull-up resistors to achieve a high noise margin even under open conditions.

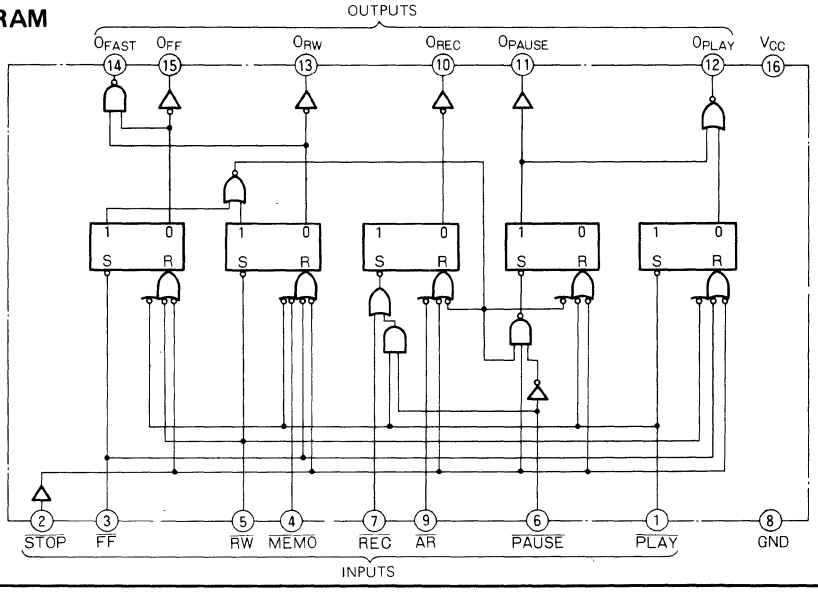
The outputs have a resistive load, and both wired-AND connection and transistor drive are possible. When the power is switched on, the automatic reset function is energized and the mode is set to STOP.

PIN CONFIGURATION (TOP VIEW)



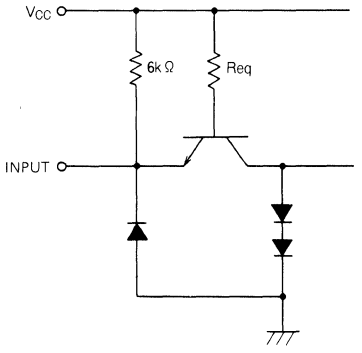
Outline 16P4

BLOCK DIAGRAM

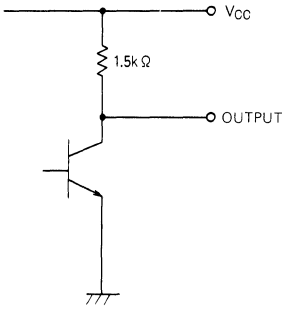


INPUT/OUTPUT EQUIVALENT CIRCUITS

(1) Input equivalent circuit



(2) Output equivalent circuit



Input pin	Req
$\overline{STOP}$, $\overline{MEMO}$, $\overline{REC}$, $\overline{AR}$	8kΩ
$\overline{PAUSE}$	4kΩ
$\overline{FF}$, $\overline{RW}$	2.7kΩ
$\overline{PLAY}$	1.6kΩ

PIN NAMES AND FUNCTIONS

Pin name		Function
Function input pin	$\overline{STOP}$	Stop command input pin
	$\overline{FF}$	FF (Fast forward) command input pin
	$\overline{RW}$	RW (Rewind) command input pin
	$\overline{REC}$	REC (Record) command input pin, effective only when it is set to low together with PLAY
	$\overline{PAUSE}$	Pause command input pin
	$\overline{PLAY}$	Play start command input pin, when set to low together with $\overline{REC}$, recording starts
Control input pin	$\overline{MEMO}$	Memory input pin
	$\overline{AR}$	Recording prevention input pin
Output pin	O_{FAST}	Output pin that goes high in the FF or RW mode
	O_{FF}	Output pin that goes high in the FF mode
	O_{RW}	Output pin that goes high in the RW mode
	O_{REC}	Output pin that goes high in the REC/PLAY ore REC/PAUSE mode
	O_{PAUSE}	Output pin that goes high in the PAUSE mode
	O_{PLAY}	Output pin that goes high in the PLAY mode

OPERATIONS WITH EACH INPUT

Input signal	O_{FAST}	O_{FF}	O_{RW}	O_{REC}	O_{PAUSE}	O_{PLAY}	Output mode
$\overline{STOP}$	L	L	L	L	L	L	STOP mode
$\overline{FF}$	H	H	L	L	L	L	FF mode
$\overline{RW}$	H	L	H	L	L	L	RW mode
$\overline{PLAY}$	L	L	L	L	L	H	PLAY mode
$\overline{PAUSE}$	L	L	L	L	H	L	PAUSE mode
$\overline{REC}/\overline{PLAY}$	L	L	L	H	L	H	REC/PLAY mode
$\overline{REC}/\overline{PAUSE}$	L	L	L	H	H	L	REC/PAUSE mode

Note 1. Input signal operates at the ⌐↓¬ fall.

2. The output maintains the output state until the next input signal arrives
3. $\overline{REC}/\overline{PLAY}$ indicates that $\overline{REC}$ and $\overline{PLAY}$ are simultaneously set to low.
4. $\overline{REC}/\overline{PAUSE}$ indicates that $\overline{REC}$ and $\overline{PAUSE}$ are simultaneously set to low.
5. $\overline{MEMO}$ and $\overline{AR}$ are control input pins, and when $\overline{MEMO}$ is low, the O_{RW} output is not set to high
   Should the $\overline{MEMO}$ = be low when the O_{RW} output is high, the O_{RW} output is set to low.
   When $\overline{AR}$ is low, the O_{REC} output is not set to high.
   Should the $\overline{AR}$ be low when the O_{REC} output is high, the O_{REC} output is set to low.

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OPERATIONS FROM OUTPOUT MODES

Present output mode	$\overline{STOP}$	$\overline{FF}$	$\overline{RW}$	$\overline{PLAY}$	$\overline{PAUSE}$	$\overline{REC}/\overline{PLAY}$	$\overline{REC}/\overline{PAUSE}$	$\overline{MEMO}$	$\overline{AR}$
STOP mode		FF mode	RW mode	PLAY mode	PAUSE mode	REC/PLAY mode	REC/PAUSE mode	STOP mode	STOP mode
FF mode	STOP mode		RW mode	PLAY mode	FF mode	REC/PLAY mode	FF mode	FF mode	FF mode
RW mode	STOP mode	FF mode		PLAY mode	RW mode	REC/PLAY mode	RW mode	STOP mode	RW mode
PLAY mode	STOP mode	FF mode	RW mode		PAUSE mode	REC/PLAY mode	REC/PAUSE mode	PLAY mode	PLAY mode
PAUSE mode	STOP mode	FF mode	RW mode	PLAY mode		REC/PLAY mode	REC/PAUSE mode	PAUSE mode	PAUSE mode
REC/PLAY mode	STOP mode	FF mode	RW mode	REC/PLAY mode	REC/PAUSE mode		REC/PAUSE mode	REC/PLAY mode	PLAY mode
REC/PAUSE mode	STOP mode	FF mode	RW mode	REC/PLAY mode	REC/PAUSE mode	REC/PLAY mode		REC/PAUSE mode	PAUSE mode

When an input signal enters in the present output mode, the output mode given in the above table is established.

: This indicates that the output mode does not change.

INPUT MULTIPLE PUSH OPERATIONS

A input signal	B input signal	Output mode
$\overline{STOP}$	$\overline{FF}$, $\overline{RW}$, $\overline{REC}$, $\overline{PAUSE}$, $\overline{PLAY}$	STOP mode
$\overline{FF}$	$\overline{RW}$	STOP mode
	$\overline{REC}$, $\overline{PAUSE}$	FF mode
	$\overline{PLAY}$	STOP mode
$\overline{RW}$	$\overline{REC}$, $\overline{PAUSE}$	RW mode
	$\overline{PLAY}$	STOP mode

A input signal	B input signal	Output mode
$\overline{REC}$	$\overline{PAUSE}$	REC/PAUSE mode
	$\overline{PLAY}$	REC/PLAY mode
	$\overline{PAUSE}$ と $\overline{PLAY}$	REC/PAUSE mode
$\overline{PAUSE}$	$\overline{PLAY}$	PAUSE mode

The output modes in the above table are established with multiple input signals A and B. When the multiple push input signal operation has been released, the input signal released last is made effective and the corresponding output mode is established.

(This does not apply to the REC/PAUSE and REC/PLAY modes.)

OUTPUT MODE WITH POWER SWITCH-ON

When the power is switched on, all the outputs are set to low and the STOP mode is established.

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Inptu voltage		V_{CC}	V
V_O	Output voltage	When output is "high"	V_{CC}	V
P_d	Power dissipation		500	mW
T_{opr}	Operating temperature		−20 ~ +75	℃
T_{stg}	Storage temperature		−55 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

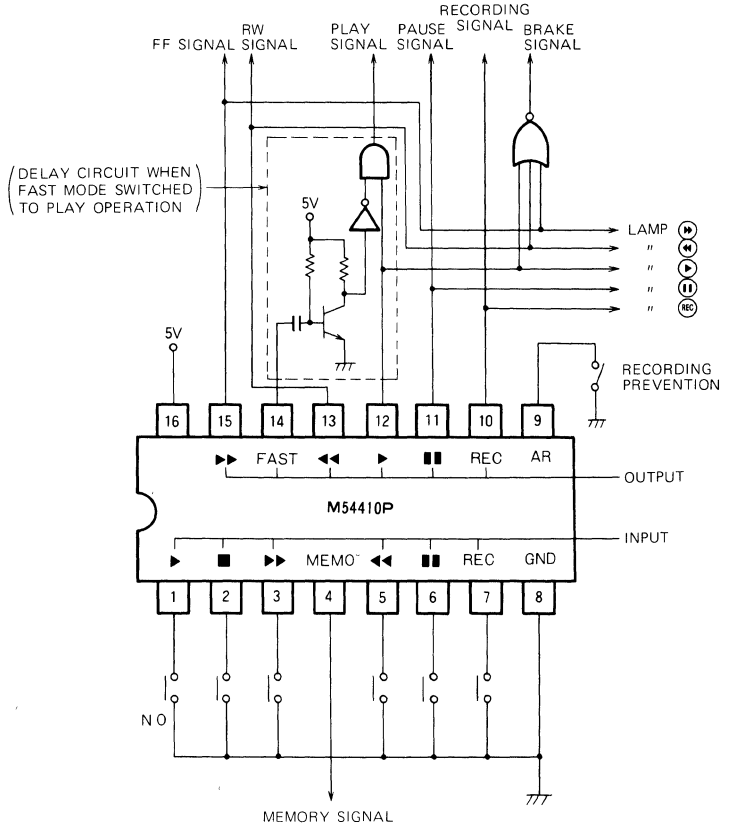
Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{OL}	Low-level output current	V_{CC} = 5V ±10%			10	mA
		V_{CC} = 5V ±20%			7.6	
I_{OH}	High-level output current	V_{CC} = 5V ±10%			−1.6	mA
		V_{CC} = 5V ±20%			−1.4	

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75℃$, unless othersie noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level inptu voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.5V$, $I_{IC}=-12mA$		−1.0	−1.5	V
$V_{I(open)}$	Input open voltage		$V_{CC}=4.5V$, $I_I=0mA$	3.2			V
V_{OH}	High-level output voltage		$V_{CC}=4.5V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-0.4mA$	2.9	4.3		V
V_{OL}	Low-level output voltage		$V_{CC}=4.5V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OL}=10mA$		0.25	0.4	V
I_{IL}	Low-level input current	$\overline{STOP}$, $\overline{MEMO}$, $\overline{REC}$, $\overline{AR}$ input pins	$V_{CC}=5.5V$, $V_I=0V$		−1.4	−2.3	mA
		$\overline{PAUSE}$ input pin			−1.9	−3.3	
		$\overline{FF}$, $\overline{RW}$ input pins			−2.4	−4.2	
		$\overline{PLAY}$ input pin			−3.5	−6.0	
I_{OX}	High-level output current		$V_{CC}=4.5V$, $V_O=0.9V$	−1.6	−2.6		mA
I_{CC}	Circuit current		$V_{CC}=5.5V$		54	90	mA

* : Typical values are at $T_a=25℃$

APPLICATION EXAMPLE



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M54418P

TAPE SELECTOR

DESCRIPTION

The M54418P is a semiconductor integrated circuit consisting of an automatic tape selector capable of switching a recording equalizer and a bias voltage control.

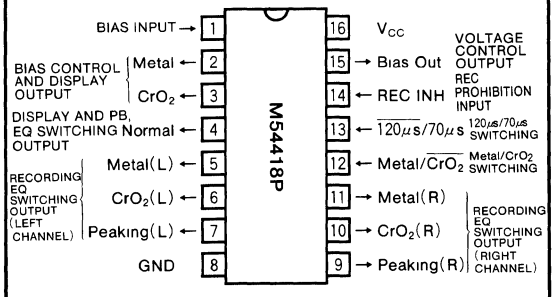
FEATURES

- Recording EQ switch output pin can withstand 3 V positive or negative voltages.
- Output voltage can be set freely to any value from 4 to 18V by adjusting the ratio of externally connected resistors.
- Built-in output current to mute output
- REC INH input available to mute output

APPLICATION

Tape decks, radio cassette recorders, and other audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

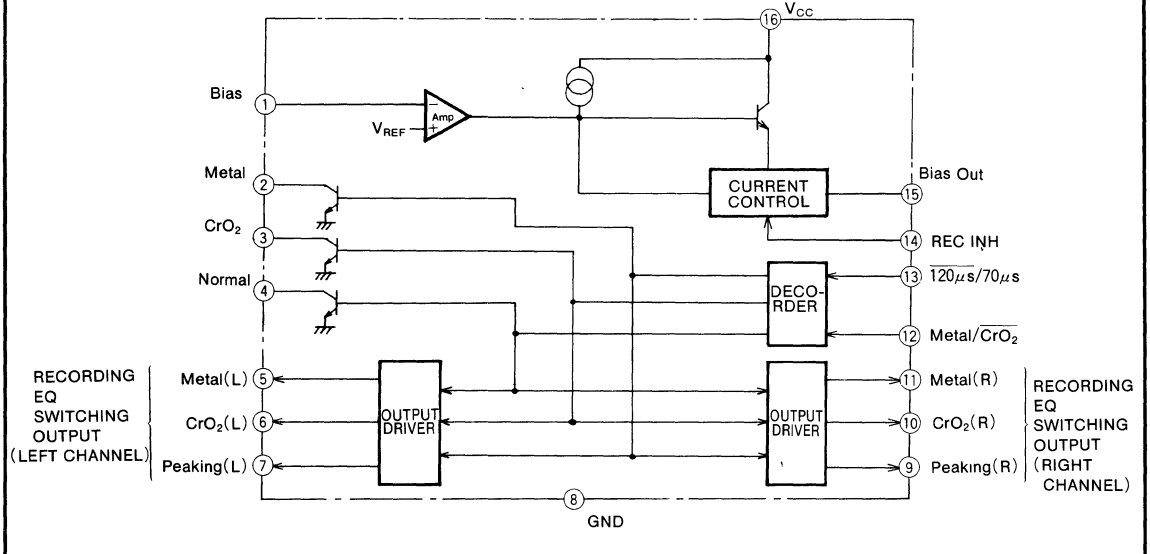
FUNCTION

The M54418P is a semiconductor integrated circuit consisting of an automatic tape selector. It is capable of switching Metal/CrO_2/Normal recording equalization and the OSC bias control voltage based on switches activated by cutouts on the back edge of the cassette shell.

The emitter of the recording EQ switching output transistor is connected to output pin and the collector to GND. As the device operates as a reverse bias transistor, the recording EQ switching pin withstands voltages up to 3 V (low saturation resistance R_S=10Ω max at I_C= 3 mA).

The OSC bias control voltage is supplied by an external power transistor connected at the BIAS OUT pin. The output voltage can be set to any value from 4 to 18V by adjusting the ratio of externally connected resistors. The current control circuit is built-in to meet the safety standards of tape decks. The REC INH pin enables the output to be muted. (V_{OUT} is turned off when REC INH is set high).

BLOCK DIAGRAM



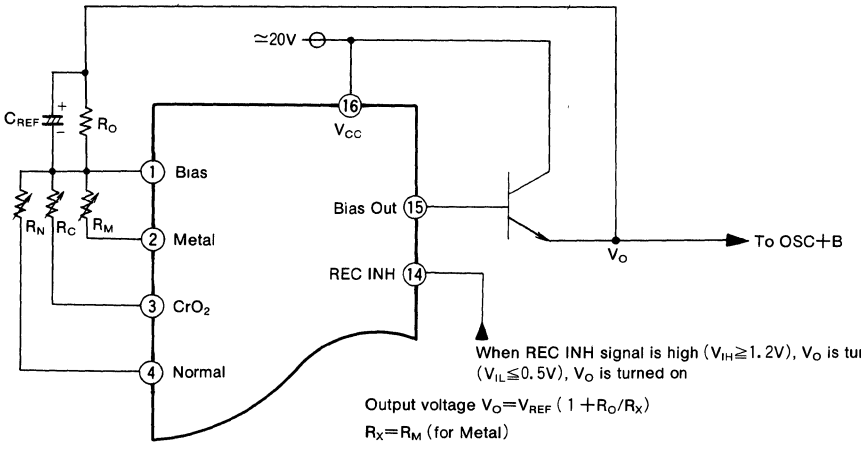
OPERATIONAL DESCRIPTION

Truth Table

Inputs		Outputs									
		Bias switching and display			Recording EQ switching (L)			Recording EQ switching (R)			Corresponding tape
$\overline{120\mu S}/70\mu S$	Metal/$\overline{CrO_2}$	Metal	CrO_2	Normal	Metal(L)	CrO_2(L)	Peaking(L)	Peaking(R)	CrO_2(R)	Metal(R)	
pin 13	pin 12	pin 2	pin 3	pin 4	pin 5	pin 6	pin 7	pin 9	pin 10	pin 11	
H	H	L	H	H	L	H	H	H	H	L	Metal
H	L	H	L	H	H	L	L	L	L	H	CrO_2
L	X	H	H	L	H	H	L	L	H	H	Normal

X : "H" or "L" のいずれかです。

Setting of OSC+B voltage



When REC INH signal is high ($V_{IH} \geqq 1.2V$), V_O is turned off and when it is low ($V_{IL} \leqq 0.5V$), V_O is turned on

Output voltage $V_O = V_{REF}(1 + R_O/R_X)$

$R_X = R_M$ (for Metal)

$= R_C$ (for CrO_2)

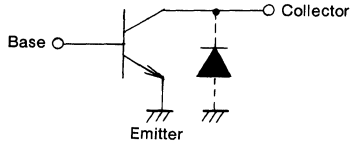
$= R_N$ (for Normal)

$V_{REF} \fallingdotseq 1.5V$

Note 1 . C_{REF} is a capacitor for time constant adjutment at the rising edge of output voltage.

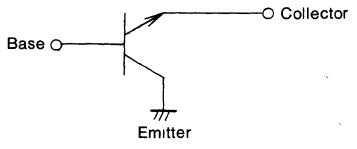
Remark : NPN transistor in semiconductor integrated circuit

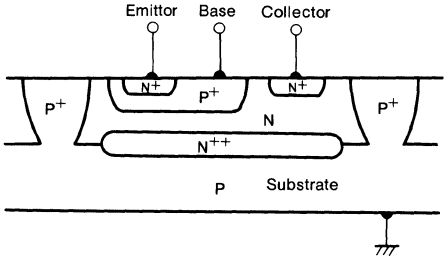
Forward NPN transistor



No negative voltage can be applied to the collector due to the parasitic diode between the substrate and the collector.

Reverse NPN transistor





Negative voltage can be applied to the emitter by leaving the base open and turning the transistor off because no parasitic diode exists.

ABSOLUTE MAXIMUM RATINGS (T_a=−10～+70℃, unless otherwise noted)

Symbol	Parameter	Conditions		Ratings	Unit
V_{CC}	Supply voltage			−0.5～+25	V
V_I	Input applied voltage	120μS/70μS, Metal/CrO_2		−0.5～+25	V
		Bias, REC INH		−0.5～+5	
V_O	Output applied voltage	Recording EQ switching output (output off)		−3～+3	V
		Metal, CrO_2, Normal (output off)		−0.5～+25	
		Bias Out	(output on)	−0.5～V_{CC}	
			(output off)	−0.5～+3	
Topr	Operating temperature			−10～+70	℃
Tstg	Storage temperature			−40～+125	℃
P_d	Power dissipation			0～800	mW
I_O	Output current	Recording EQ switching output (output on)		−5～+5	mA
		Metal, CrO_2, Normal (output on)		0～10	

RECOMMENDED OPERATING CONDITIONS (T_a=−10～+70℃)

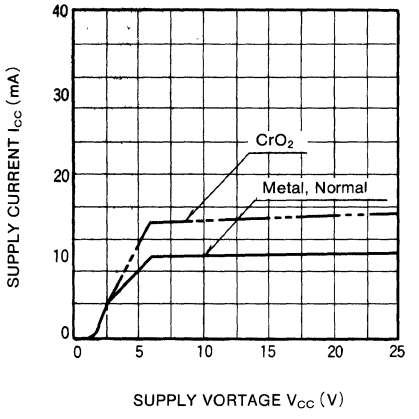
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		8	20	23	V
V_O	Output applied voltage	Metal, CrO_2, Normal (output off)			23	V
		Recording EQ output (output off)			±2.5	
I_{OL}	Low-level output current	Metal, CrO_2, Normal (output on)			5	mA
		Recording EQ on (output on)			±3	
I_O	Output load current	V_{CC}=20V, V_{OUT}=4～18V			−1	mA
R	Externally connected resistor for voltage setting	R_O, R_X	1		20	kΩ

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

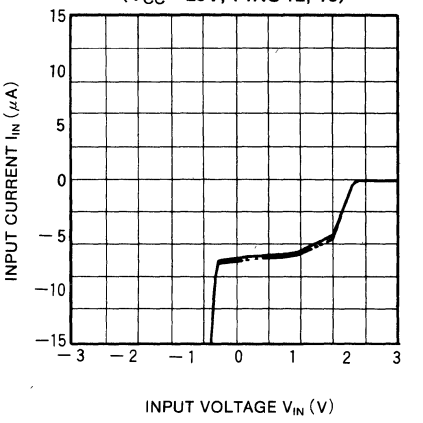
Symbol	Parameter	Test pin	Test coditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	Pins 12, 13	V_{CC}=8～23V	3		23	V
		Pin 14		1.2		4	
V_{IL}	Low-level input voltage	Pins 12, 13	V_{CC}=8～23V	0		0.8	V
		Pin 14		0		0.5	
I_{IH}	High-level input current	Pins 12, 13	V_{CC}=V_{IH}=23V			30	μA
I_{IL}	Low-level input current		V_{CC}=23V, V_{IL}=0V			−100	
I_{IN}	Input current	Pin 14	V_{CC}=23V, V_{IN}=1V			0.5	mA
V_{OL}	Low-level output voltage	Pins 2, 3, 4	V_{CC}=8V, I_{OL}=5mA			100	mV
		Pins 5 through 7, Pins 9 through 11	V_{CC}=8V, I_{OL}=±3mA			±30	
I_{OIK}	High-level output leak current	Pins 2, 3, 4	V_{CC}=23V, V_{OH}=23V			30	μA
		Pins 5 through 7, Pins 9 through 11	V_{CC}=23V, V_C=±3V			±10	
B_{OUT}	Control output voltage	Pin 15	V_{CC}=20V, I_O=−1mA	4		18	V
TC_{VO}	Output voltage temperature coefficient	Pin 15	V_{CC}=20V, V_O=4～18V, T_a=0～50℃		0.02		%/℃
V_{REF}	Reference voltage			1.35	1.5	1.65	V
I_{CC}	Supply current	All outputs open	V_{CC}=23V		15	30	mA
I_{Bias}	Bias input current	Pin 1	V_{CC}=23V, V_{IH}=V_{REF}			10	μA
I_S	Output short circuit current	Pin 15	V_{CC}=23V, V_O=0V		−1.5	−3	mA

TYPICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

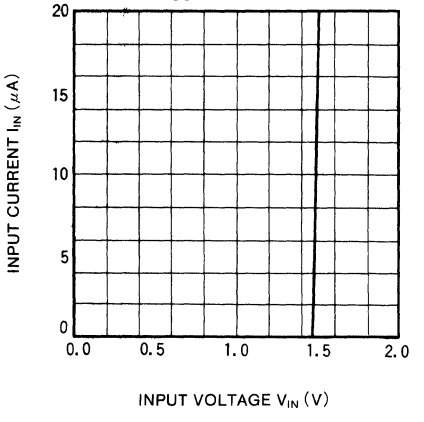
SUPPLY VOLTAGE VS SUPPLY CURRENT



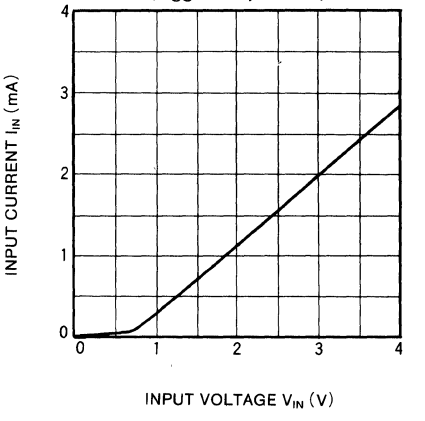
INPUT VOLTAGE VS INPUT CURRENT
(V_{CC}=23V, PINS 12, 13)



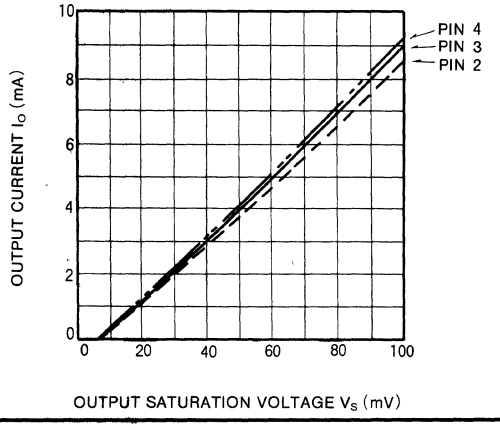
INPUT VOLTAGE VS INPUT CURRENT
(V_{CC}=23V, PIN 1)



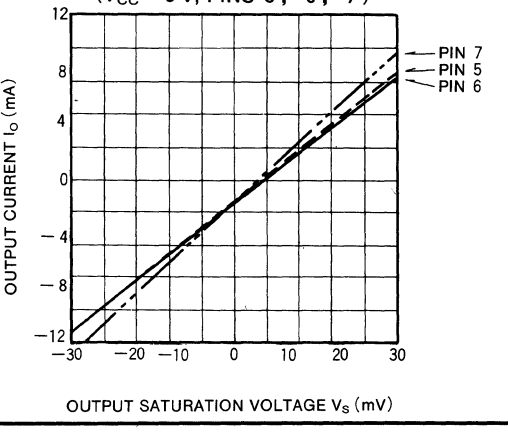
INPUT VOLTAGE VS INPUT CURRENT
(V_{CC}=23V, PIN 14)



OUTPUT SATURATION VOLTAGE
(V_{CC}= 8 V, PINS 2, 3, 4)

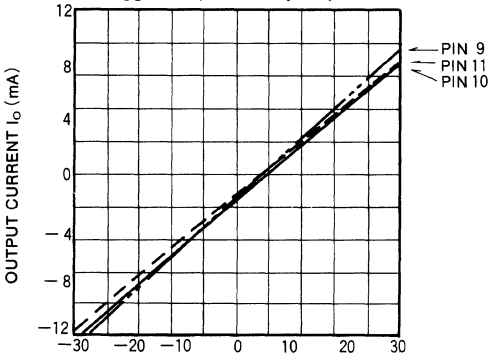


OUTPUT SATURATION VOLTAGE (+, −)
(V_{CC}= 8 V, PINS 5, 6, 7)

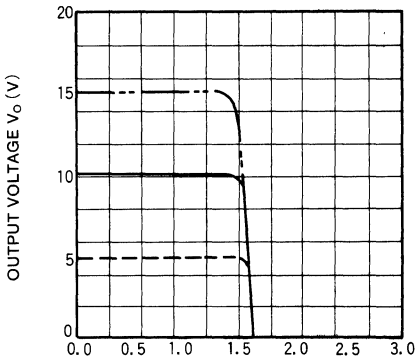


OUTPUT SATURATION VOLTAGE (+, −)

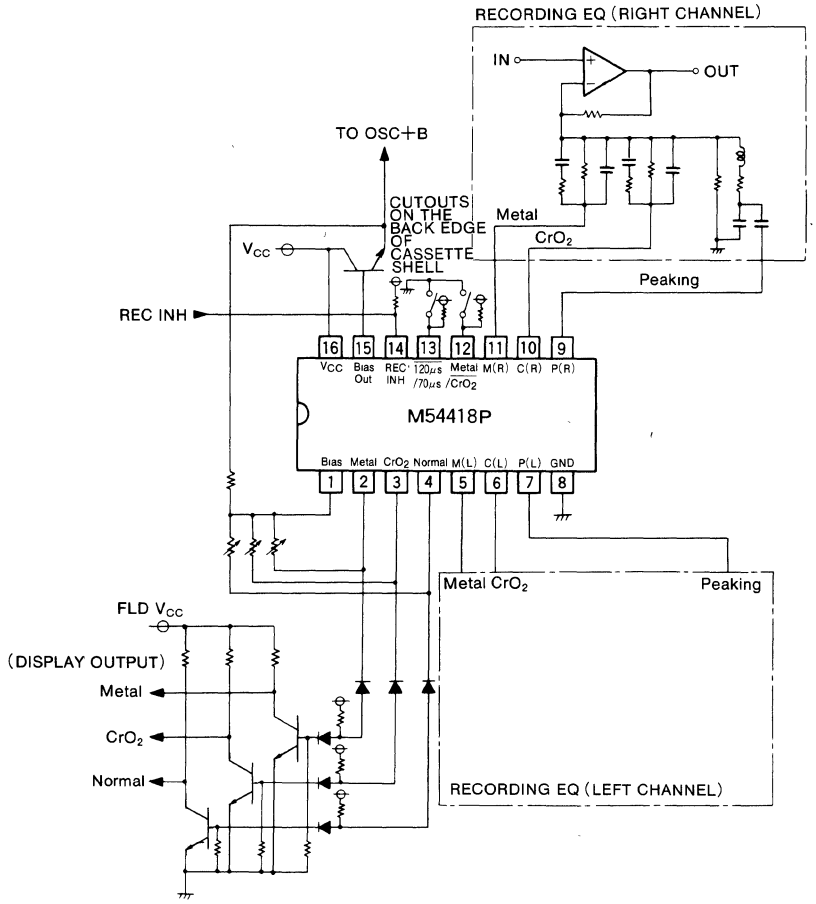
(V_{CC} = 8 V, PINS 9, 10, 11)



LOAD CHARACTERISTICS (PIN 16)



APPLICATION EXAMPLE



M54455L

1/4, 1/8, 1/40 HIGH SPEED DIVIDER

DESCRIPTION

The M54455L is a semiconductor integrated circuit consisting of a 1/4, 1/8, 1/40 high speed frequency divider with an ECL circuit configuration.

FEATURES

- High-speed operation (f_{max} = 130 MHz)
- Operation at low input amplitude (400mV_{P-P} minimum input amplitude)
- TTL level output

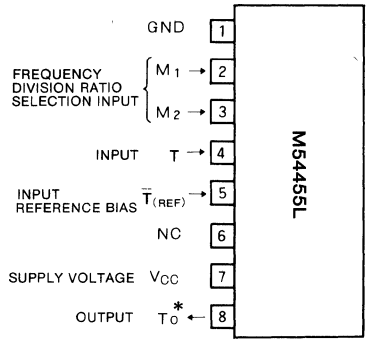
APPLICATION

FM radio prescalers; digital equipment for consumer and industrial applications.

FUNCTION

This divider is based on an ECL circuit configuration. If a frequency up to a maximum of 150MHz is applied to the input (T_1) pin, a 1/4-divided output can be obtained when the frequency division ratio selection input (M_1 and M_2) pins are both low. When pins M_1 and M_2 are at high and low a 1/8-divided output is obtained and both pins are high, a 1/40-divided output is obtained. The output (T_0) conforms to the TTL level open collector format. The table right side gives the relationship between the input conditions and the freqency division ratio.

PIN CONFIGURATION (TOP VIEW)



* : Open collector output
NC : No connection

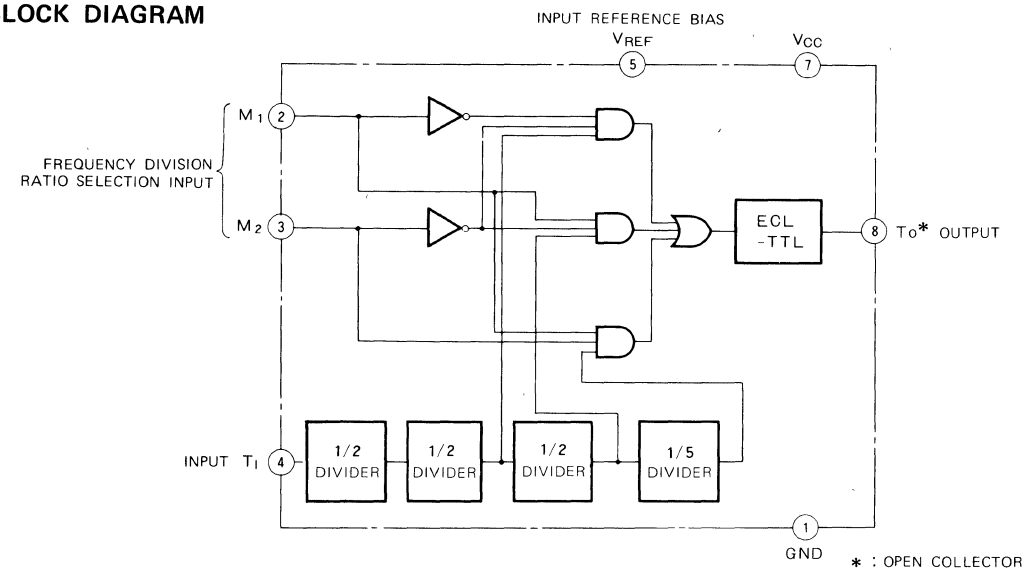
Outline 8P5

FREQUENCY DIVISION RATIO SELECTION INPUTS (M_1, M_2) AND FREQUENCY DIVISION RATIOS

M_1	L	H	H
M_2	L	L	H
Frequency divition ratio	1/4	1/8	1/40

Note Do not use the devider with M_1 low and M_2 high

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		2.5	V
V_{IM}	Input voltage (M input)		V_{CC}	V
V_O	Output applied voltage		5.5	V
Pd	Power dissipation	T_a=25℃	1.33	W
Topr	Operating temperature		−10∼+75	℃
Tstg	Storge temperature		−55∼+125	℃

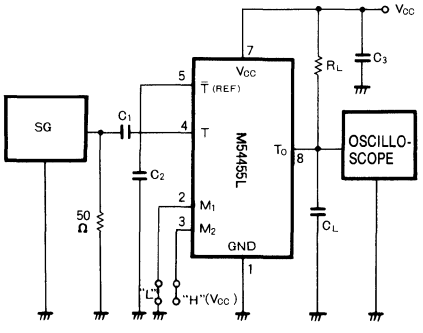
RECOMMENDED OPERATING CONDITIONS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
f_{IN}	Input frequency		30		130	MHz
V_{IN}	Input amplitead	V_{CC}=5V, f_{IN}=30∼130MHz	400		800	mV_{P-P}
$V_{IH(M)}$	High-level M input voltage		2.5		V_{CC}	V
$V_{IL(M)}$	Low-level M input voltage		0		0.4	V

ELECTRICAL CHARACTERISTICS (T_a=−10∼+75℃, unless otherwise noted)

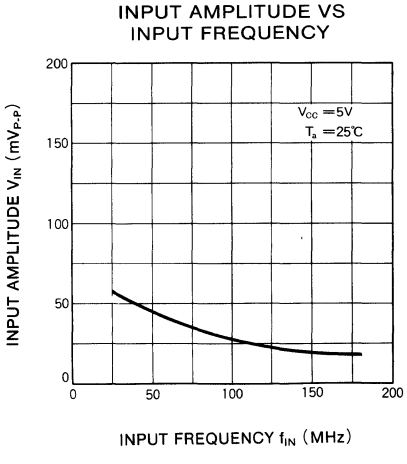
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5V			13	mA
V_{IN}	Prescaler operating input	V_{CC}=5V, f_{IN}=30∼130MHz, T_a=25℃			400	mV_{P-P}
$I_{IH(M)}$	High-level M input current	V_{CC}=5V, V_{OH}=2.5V		0		μA
$I_{IL(M)}$	Low-level M input current	V_{CC}=5V, V_{OL}=0.4V		30		μA
$I_{O(leak)}$	Output leak current	V_{CC}=5V, V_O=5.5V			100	μA
V_{OL}	Low-level output voltage	V_{CC}=5V, I_{OL}=5mA			0.5	V

fmax TEST CIRCUIT



C_1≃1000pF, C_2≃1000pF, C_L≃5pF, R_L=3∼5kΩ, C_3≃0.1μF

TYPICAL CHARACTERISTICS



M54459L

1/20, 1/100 HIGH SPEED DIVIDER

DESCRIPTION

The M54459L is a semiconductor integrated circuit consisting of a built-in 1/20 and 1/100 high speed frequency divider featuring an ECL circuit configuration.

FEATURES

- High-speed operation (f_{max} = 130MHz)
- Operation at low input amplitudes (180mV_{P-P} minimum input amplitude)
- TTL level output

APPLICATION

FM radio prescalers, digital equipment for consumer and industrial applications.

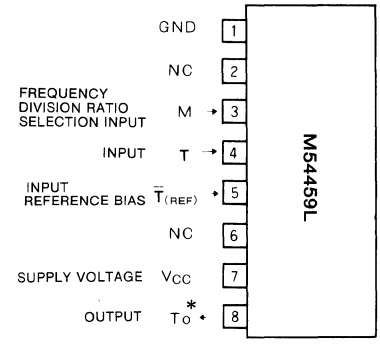
FUNCTION

This divider is based on an ECL circuit configuration. When a frequency up to a maximum of 130MHz is applied to the T_1 input pin, a 1/20-divided output is produced when the division ratio selection input pin (M) is low-level or a 1/100-divided output is produced when the division ratio selection input pin (M) is high-level. The output (T_0) is available in the TTL level open collector format.

Frequency division ratio selection input (M) and ratios

M	Low	High
Division ratio	1/20	1/100

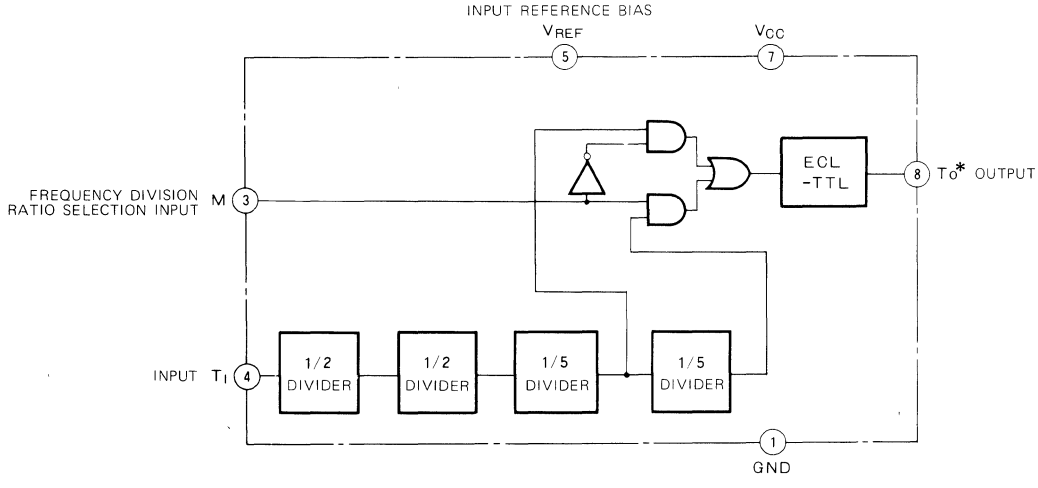
PIN CONFIGURATION (TOP VIEW)



* : Open connector output
NC : No connection

Outline 8P5

BLOCK DIAGRAM



* : OPEN COLLECTOR OUTPUT

MITSUBISHI ELECTRIC

M54459L

1/20, 1/100 HIGH SPEED DIVIDER

ABSOLUTE MAXIMUM RATINGS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		2.5	V
V_O	Output applied voltage		5.5	V
P_d	Power dissipation	T_a=25℃	1.33	W
Topr	Operating temperature		−10∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

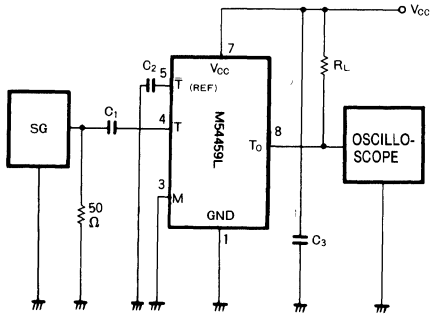
RECOMMENDED OPERATING CONDITIONS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
f_{IN}	Input frequency		30		130	MHz
V_{IN}	Input amplitude	V_{CC}=5V, f_{IN}=30∼130MHz	200		800	mV_{P-P}
$V_{IH(M)}$	High-level M input voltage		2.6		V_{CC}	V
$V_{IL(M)}$	Low-level M input voltage		0		0.4	V

ELECTRICAL CHARACTERISTICS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5V		6.5	10	mA
V_{IN}	Prescaler operating input	V_{CC}=5V, f_{IN}=30∼130MHz, T_a=25℃			180	mV_{P-P}
$I_{IH(M)}$	High-level M input current	V_{CC}=5V, $V_{IH(M)}$=2.6V		2		μA
$I_{IL(M)}$	Low-level M input current	V_{CC}=5V, $V_{IL(M)}$=0.4V		0.1		μA
$I_{O(leak)}$	Output leak current	V_{CC}=5V, V_O=5.5V			100	μA
V_{OL}	Low-level output voltage	V_{CC}=5V, I_{OL}=5mA			0.5	V

fmax TEST CIRCUIT

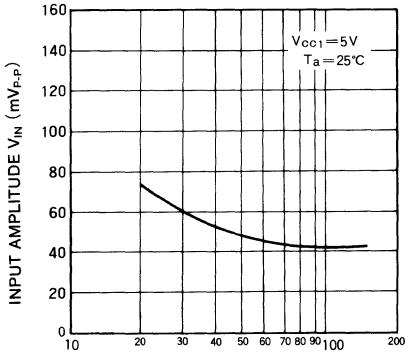


C_1≃1000pF, C_2≃1000pF, C_3≧10000pF, R_L≃5kΩ

Notes : The adove figure shows the configuration with 1/20 frequency division.
Connect the frequency division ratio selection input (M) to the supply voltage V_{CC} pin for 1/100 frequency division.

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54460L

1/10, 1/100 HIGH SPEED DIVIDER

DESCRIPTION

The M54460 is a semiconductor integrated circuit consisting of a built-in 1/10 and 1/100 high speed frequency divider featuring an ECL circuit configuration.

FEATURES

- High-speed operation (f_{max} = 130MHz)
- Operation at low input amplitudes (200mV_{P-P} minimum input amplitude)
- Open collector type of output

APPLICATION

FM radio prescalers

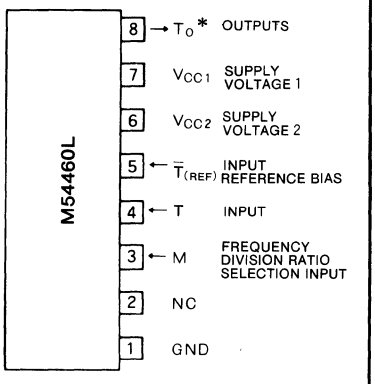
Digital equipment for consumer and industrial applications.

FUNCTION

This driver is based on an ECL circuit configuration. When a frequency up to a maximum of 130MHz is applied to the T input pin, a 1/10-dvded output is produced when the division ratio selection input pin (M) is low-level or a 1/100-divided output is produced when the division ratio selection input pin (M) is high-level. The output (T_0) is an open collector output.

When you use the V_{CC1} (7pin), the V_{CC2} (6pin) must be opened. And you use the V_{CC2} (6pin), the V_{CC1} (7pin) must be opened.

PIN CONFIGURATION (TOP VIEW)

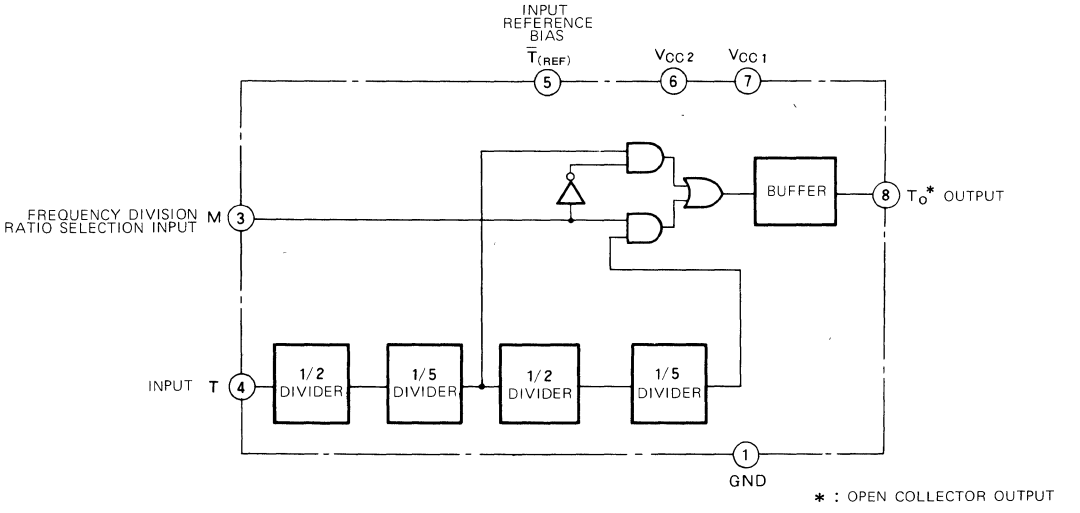


* : Open connector output

NC : No connection

Outline 8P5

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage 1		5	V
V_{CC2}	Supply voltage 2		7	V
V_I	Input voltage		2.5	V
V_O	Output applied voltage		5.5	V
Pd	Power dissipation	T_a=75℃	650	mW
Topr	Operating temperature		−10∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

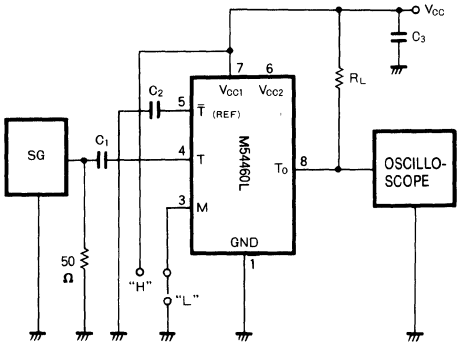
RECOMMENDED OPERATING CONDITIONS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC1}	Supply voltage 1		2.7	3	3.3	V
V_{CC2}	Supply voltage 2		4.5	5	5.5	V
f_{IN}	Input frequency		30		130	MHz
V_{IN}	Input amplitude	V_{CC1}=3V, f_{IN}=30∼130MHz	200		800	mV_{P-P}
$V_{IH(M)}$	High-level M input voltage	V_{CC1}=3V, V_{CC2} : Open	2.6		3	V
		V_{CC1} : Open, V_{CC2}=5V				
$V_{IL(M)}$	Low-level M input voltage				0.4	V

ELECTRICAL CHARACTERISTICS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC1}	Supply current 1	V_{CC1}=3V		6	9	mA
I_{CC2}	Supply current 2	V_{CC2}=5V		8		mA
V_{IN}	Input frequency	V_{CC1}=3V, f_{in}=30∼130MHZ, T_a=25℃			150	mV_{P-P}
$I_{IH(M)}$	High-level M input current	V_{CC}=3V, $V_{IH(M)}$=2.6V		2		μA
$I_{IL(M)}$	Low-level M input current	V_{CC}=3V, $V_{IL(M)}$=0.4V		0.1		μA
$I_{O(leak)}$	Output leak current	V_{CC}=3V, V_O=5.5V			100	μA
V_{OL}	Low-level output voltage	V_{CC}=3V, I_{OL}=5mA			0.5	V

fmax TEST CIRCUIT

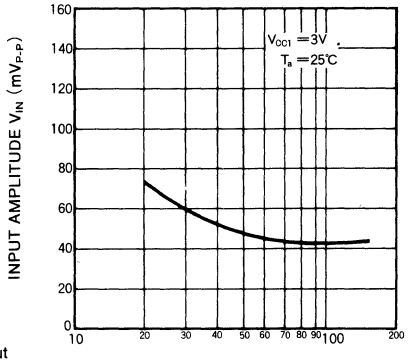


$C_1 \simeq 1000pF$, $C_2 \simeq 1000pF$, $C_3 \simeq 0.1\mu F$, R_L=3∼5KΩ,

Notes : The "H" level of the frequency divider ratio change input M should be 2.6V (min) and 3V (max) when V_{CC1} is used as the power supply, M input can be connocted directly to V_{CC1}
When V_{CC2} is used, "H" level should be see to with in the rarge of values given above

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54466L

1/10,1/11 HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54466L is a semiconductor integrated circuit consisting of a 1/10, 1/11 divider using emitter-coupled logic.

FEATURES

- High-speed operation (f_{max}=300MHz)
- ECL level output
- Synthesized operation up to 300MHz when used in conjunction with PLL ICs such as the M54929P·

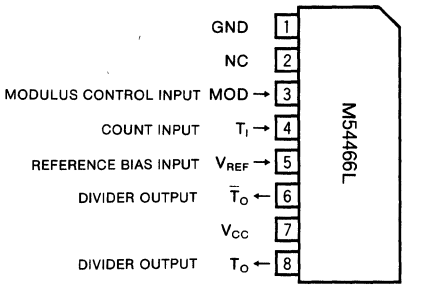
APPLICATION

Amateur radio and other communication equipment

FUNCTIONAL DESCRIPTION

The M54466L consists of a divider using emitter-coupled logic. When a frequency up to 300MHz maximum is applied to input T_I, 1/10 division is obtained. When modulus input changes from low to high, one pulse of input pulse T_I is skipped and 1/11 division is obtained.
The outputs T_O, $\overline{T}_O$ are ECL level.

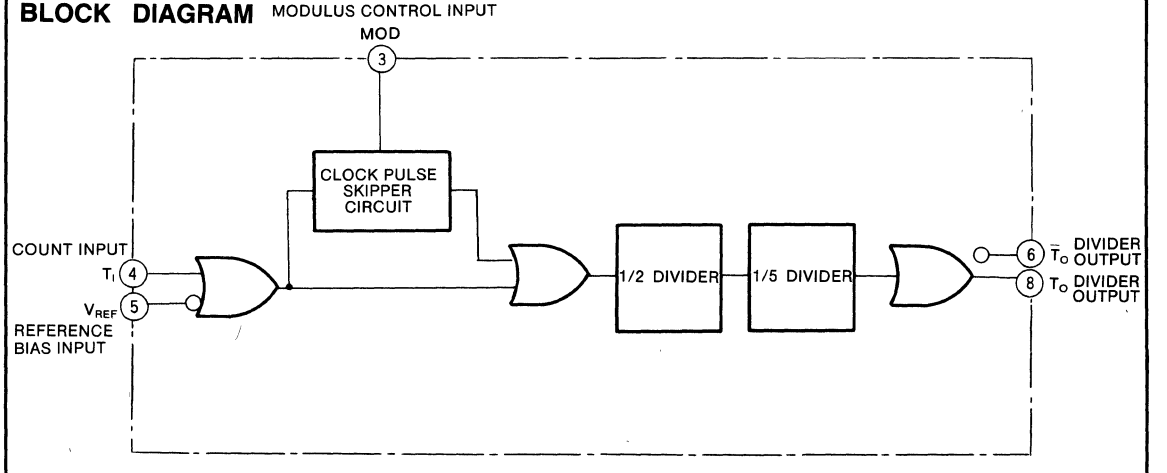
PIN CONFIGURATION (TOP VIEW)



Outline 8P5

NC : No connection

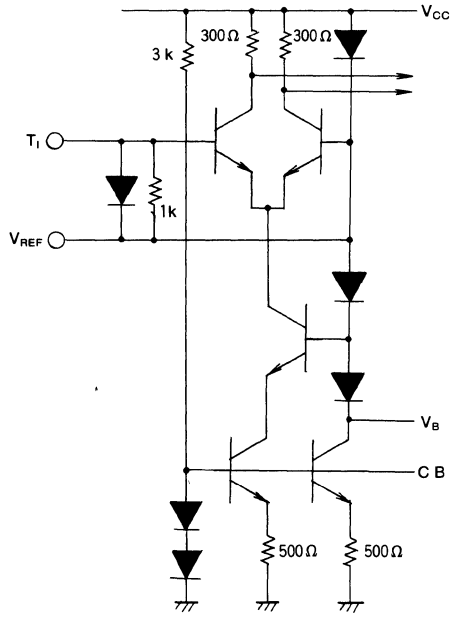
BLOCK DIAGRAM



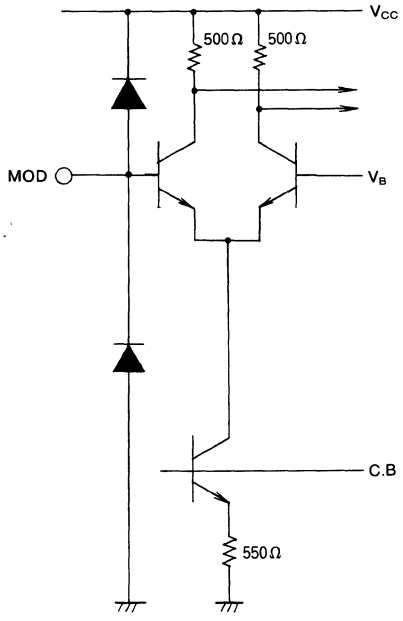
MITSUBISHI ELECTRIC

I/O CIRCUIT DIAGRAM

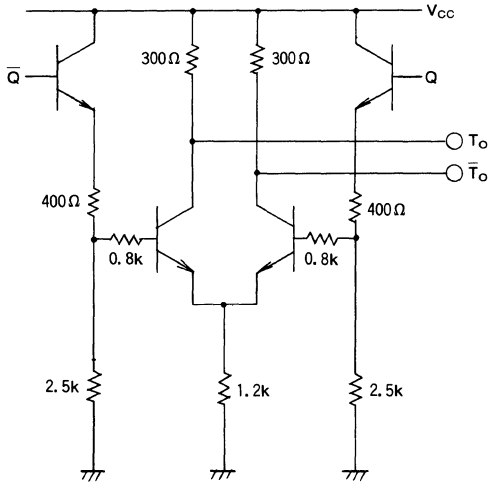
1 T_I, V_{REF} INPUTS



2 MOD INPUT



3 T_O, $\overline{T}_O$ OUTPUT



Note 1. Typical values are at V_{CC}= 5 V, T_a=25℃

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit
			Min	Max	
V_{CC}	Supply voltage		−0.5	6.0	V
V_I	Input voltage		−0.5	V_{CC}	V
V_O	Output voltage		−0.5	V_{CC}	V
P_d	Power dissipation	T_a =75℃		350	mW
Topr	Operating temperature		−20	+75	℃
Tstg	Storage temperature range		−40	+125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=4.5∼5.5V, T_a=−20∼+75℃, unless otherwise noted)

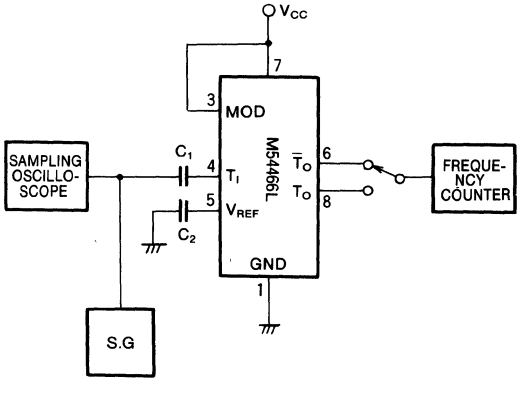
Symbol	Parameter	Conditions	Limits			Unit	Remark
			Min	Typ	Max		
V_{CC}	Supply voltage		4.5	5.0	5.5	V	
F_{IN}	Input frequency		30		300	MHz	Sine wave
V_{IN}	Input amplitude	F_{IN} =30∼300MHz	400		800	mV_{P-P}	
V_{IHMOD}	MOD high-level input voltage	V_{CC} = 5 V, T_a =25℃	2.7			V	
V_{ILMOD}	MOD low-level input voltage	V_{CC} = 5 V, T_a =25℃			2.3	V	
F_{INMOD}	MOD input frequency				30	MHz	

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

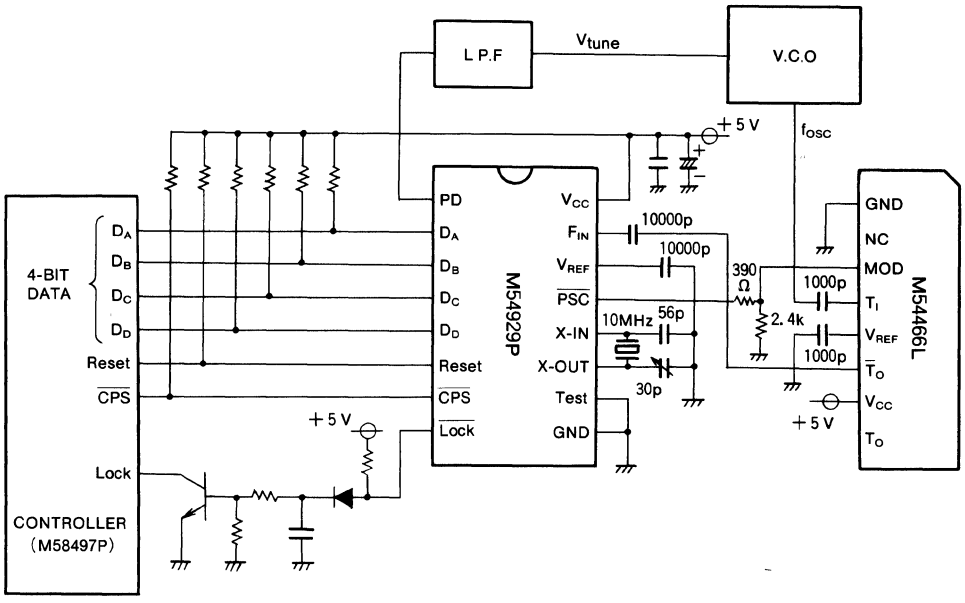
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
I_{IHMOD}	MOD high-level input current	Pin 3	V_{CC} = 5 V V_{IHMOD} =2.7V			30	μA
I_{ILMOD}	MOD low-level input current	Pin 3	V_{CC} = 5 V V_{ILMOD} =2.3V	−20			μA
I_{CC}	Supply current	Pin 7	V_{CC} =5.5V T_a =−20∼+75℃		30	45	mA
V_O	Output amplitude	Pins 6, 8	V_{CC} =4.5∼5.5V F_{IN} =300MHz	300			mV_{P-P}

Typical values are at V_{CC} = 5 V, T_a =25℃.

fmax TEST CIRCUIT

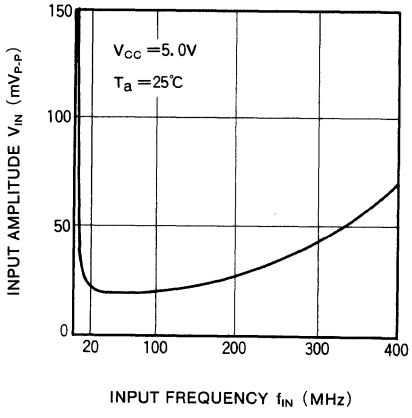


APPLICATION EXAMPLE



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54468AL

1/256 HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54468AL is a semiconductor integrated circuit consisting of an high-speed 1/256 divider using emitter-coupled logic.

FEATURES

- High-speed operation (f_{max}=1.1GHz)
- Operates at low input amplitude (150mVP—P min)
- ECL level output

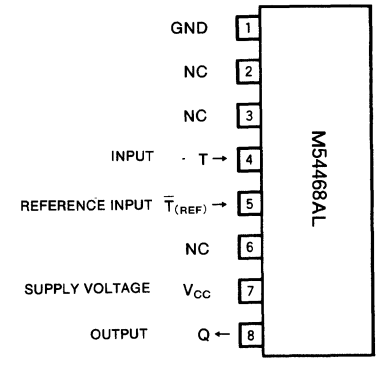
APPLICATION

Prescalers for PLL synthesized TV tuners, and general use in industrial and consumer digital equipment.

FUNCTION

The M54468AL consists of a divider using emitter-coupled logic. When a frequency from 80 through 1,100MHz is applied to the input pin T, the 1/256 divided frequency is obtained.
The output Q is ECL level.

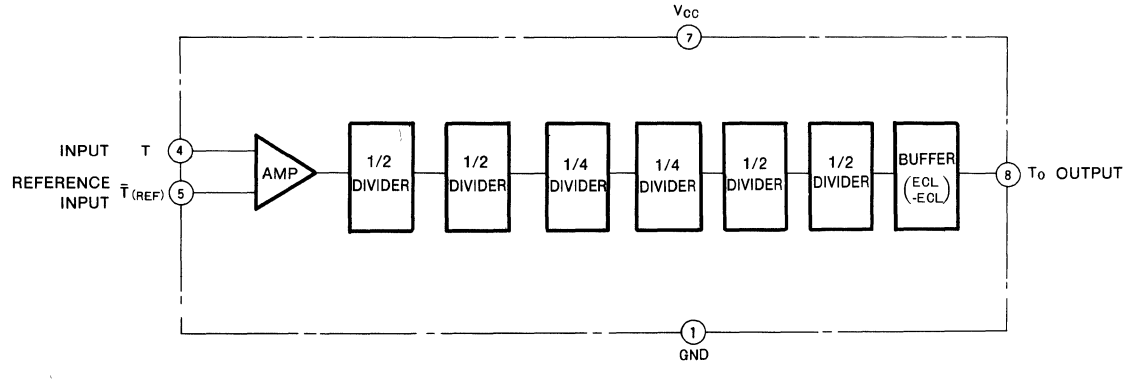
PIN CONFIGURATION (TOP VIEW)



Outline 8P5

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M54468AL

1/256 HIGH SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		V_{CC}	V
Pd	Power dissipation	T_a=25℃	1.33	W
Topr	Operating temperature		−10∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

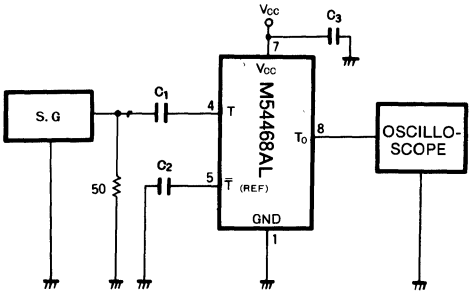
RECOMMENDED OPERATING CONDITIONS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
f_{IN}	Input frequency		80		1100	MHz
V_{IN}	Input amplitude	V_{CC}=5V, f_{IN}=80∼1100MHz, T_a=25℃	150		1000	mV_{P-P}

ELECTRICAL CHARACTERISTICS (T_a=−10∼+75℃, unless otherwise noted)

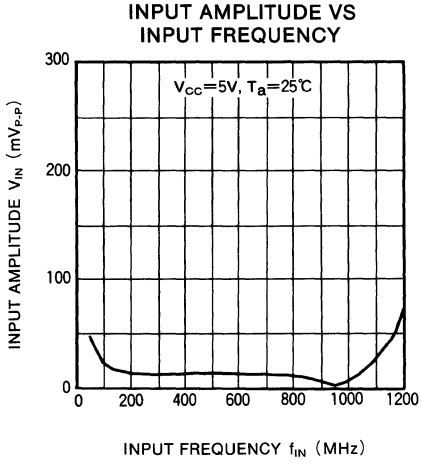
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5V	40	47	60	mA
V_{IN}	Input amplitude	V_{CC}=5V, T_a=25℃ f_{IN}=80MHz∼1100MHz			150	mV_{P-P}
V_O	Output amplitude	V_{CC}=5V	0.6			V_{P-P}

fmax TEST CIRCUIT



C_1=C_2≃1000pF, C_3≃0.1μF
Resistance : Ω

TYPICAL CHARACTERISTICS



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

M54471P/L

1/64 HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54471P/L is a semiconductor integrated circuit consisting of an high-speed 1/64 divider using emitter-coupled logic.

FEATURES

- High-speed operation (f_{max}=1.25GHz)
- ECL level output

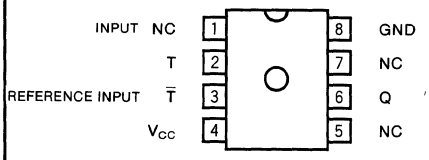
APPLICATION

Prescalers for PLL synthesized TV tuners, and for general use in industrial and consumer digital equipment.

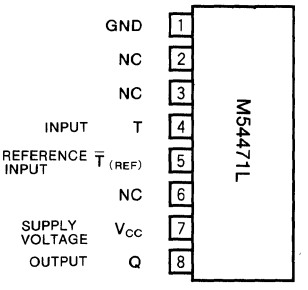
FUNCTION

The M54471P/L consists of a divider using emitter-coupled logic. When a frequency from 80 through 1,250MHz is applied to input pin T, the 1/64 divided frequency is obtained. The output Q is ECL level.

PIN CONFIGURATION (TOP VIEW)



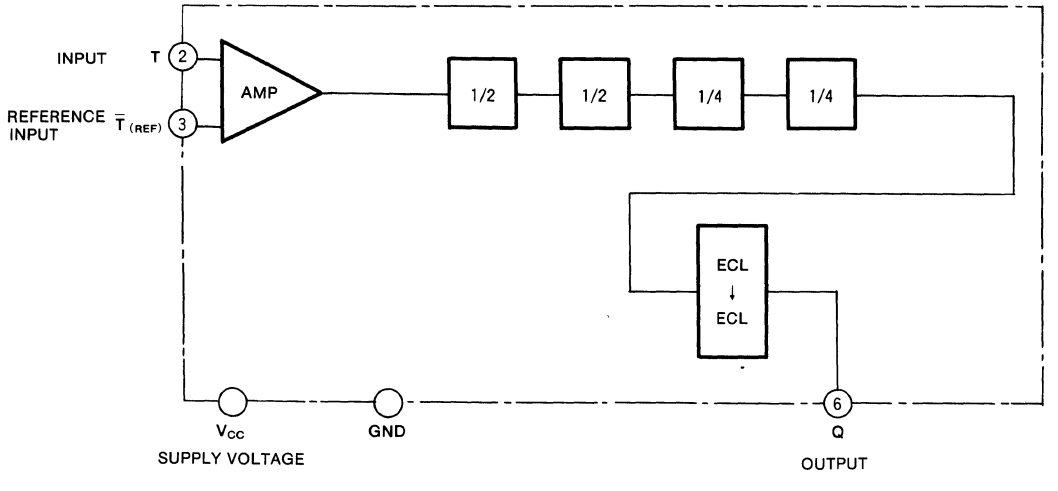
Outline 8P4



Outline 8P5

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/64 HIGH SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼6.5	V
V_I	Input voltage	T, $T_{(REF)}$ inputs	0∼2.5	V
P_d	Power dissipation	T_a=25℃	1.18	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

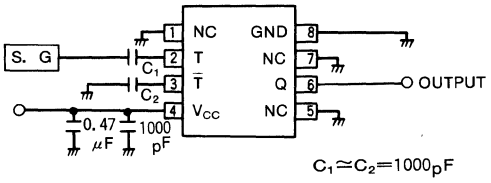
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	Input amplitude	f=80∼1250MHz	−4		4	dBm

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5.5V	30	40	60	mA
V_{IN1}	Input sensitivity 1	f_{IN}=80MHz∼1100MHz	−16		4	dBm
V_{IN2}	Input sensitivity 2	f_{IN}=1100MHz∼1250MHz	−4		4	dBm
V_O	Output amplitude	V_{CC}=4.5V, f_{IN}=1250MHz	0.8	1.3		V_{P-P}

Typical values are at V_{CC}=5.0V, T_a=25℃.

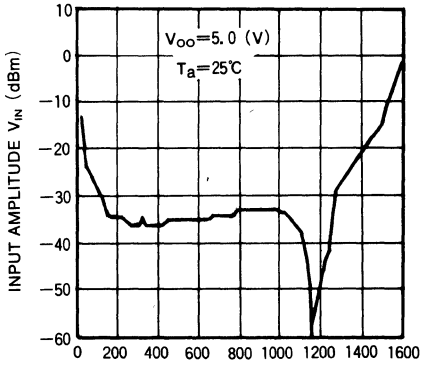
TYPICAL CHARACTERISTICS



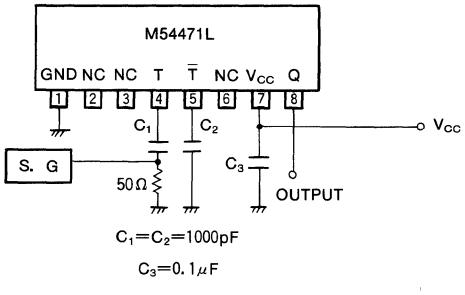
$C_1 \simeq C_2$=1000pF

Note 1 ＊Normally the NC pins must be grounded
2 The probe capacitance and resistance to set the output must have the characteristics of $C_{IN} \leq$ 10pF, $R_{IN} \geq$ 1 MΩ

TYPICAL CHARACTERISTICS
INPUT AMPLITUDE VS INPUT FREQUENCY



TEST CIRCUIT



C_1=C_2=1000pF
C_3=0.1μF

M54472L

1/64 HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54472L is a semiconductor integrated circuit consisting of an high-speed 1/64 divider using emitter-coupled logic.

FEATURES

- High-speed operation (f_{max}=1.1GHz)
- Operates at low input amplitude (150mV_{P-P} min)
- ECL level output

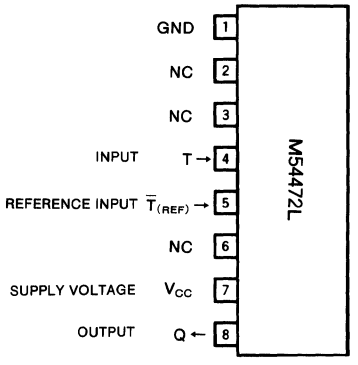
APPLICATION

Prescalers for PLL synthesized TV tuners, and general use in industrial and consumer digital equipment.

FUNCTION

The M54472L consists of a divider using emitter-coupled logic. When a frequency from 80 through 1,100MHz is applied to the input pin T, the 1/64 divided frequency is obtained.
The output Q is ECL level.

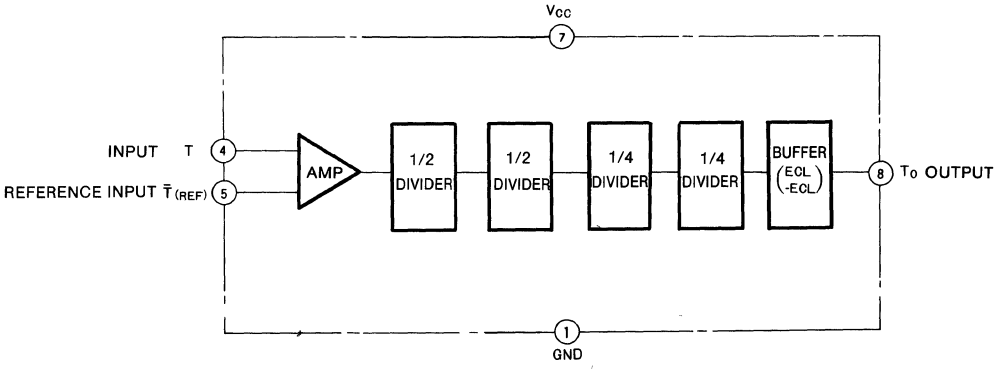
PIN CONFIGURATION (TOP VIEW)



Outline 8P5

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/64 HIGH SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage			V
V_I	Input voltage		V_{CC}	V
P_d	Power dissipation	T_a=25℃	1.33	W
Topr	Operating temperature		−10∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

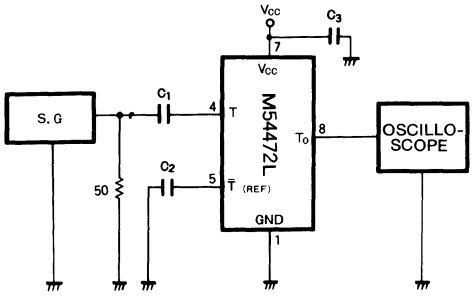
RECOMMENDED OPERATING CONDITIONS (T_a=−10∼+75℃)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
f_{IN}	Input frequency		80		1100	MHz
V_{IN}	Input amplitude	V_{CC}=5V, f_{IN}=80∼1100MHz, T_a=25℃	150		1000	mV_{P-P}

ELECTRICAL CHARACTERISTICS (T_a=−10∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5V	40	47	60	mA
V_{IN}	Input amplitude	V_{CC}=5V, T_a=25℃ f_{IN}=80MHz∼1100MHz			150	mV_{P-P}
V_O	Output amplitude	V_{CC}=5V	0.6			V_{P-P}

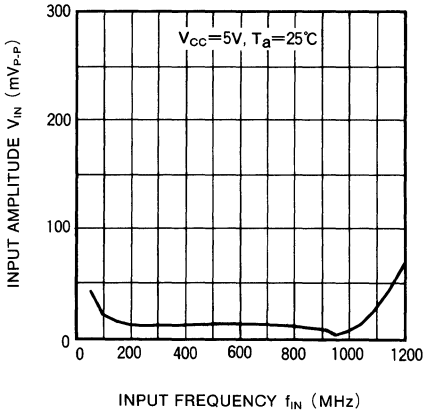
fmax TEST CIRCUIT



C_1=C_2≃1000pF, C_3≃0.1μF
Resistance : Ω

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54473P/L

1/256 HIGH SPEED DIVIDER WITH TTL OUTPUT

DESCRIPTION

The M54473P/L is a semiconductor integrated circuit consisting of an high-speed 1/256 divider using emitter-coupled logic.

FEATURES

- High-speed operation (f_{max}=1.25GHz)
- TTL level output

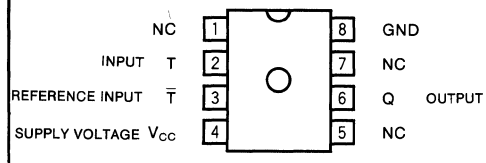
APPLICATION

Prescalers for PLL synthesized TV tuners, and general use in industrial and consumer digital equipment.

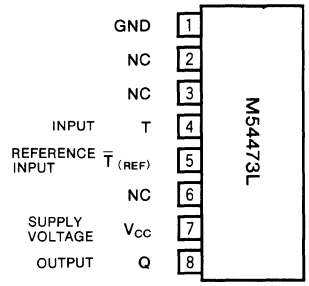
FUNCTION

The M54473P/L consists of a divider using emitter-coupled logic (ECL). When a frequency from 80 through 1,250MHz is applied to the input pin T, the 1/256 divided frequency is obtained.
The output Q is ECL level.

PIN CONFIGURATION (TOP VIEW)



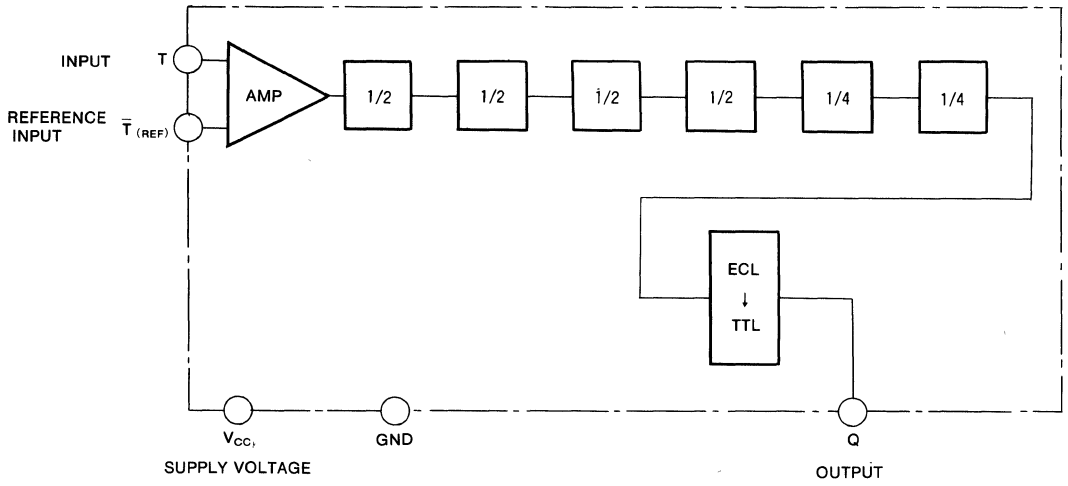
Outline 8P4



Outline 8P5

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/256 HIGH SPEED DIVIDER WITH TTL OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
V_I	Input voltage	T, $\overline{T}$ (REF)	0∼V_{CC}	V
P_d	Power dissipation	T_a=25℃	1.18	W
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS

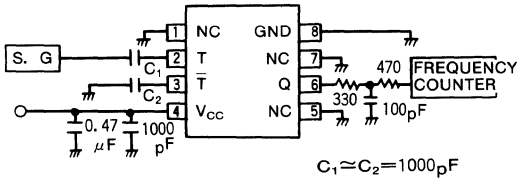
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	Input amplitude	f=80∼1250MHz	−4		4	dBm
I_{OL}	Low-level output current		0	1	2	mA

ELECTRICAL CHARACTERISTICS (V_{CC}=5±10%, T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5.5V	30	40	60	mA
V_{IN1}	Input sensitivity 1	f_{IN}=80∼1100MHz	−16		4	dBm
V_{IN2}	Input sensitivity 2	f_{IN}=1100∼1250MHz	−4		4	dBm
V_O	Output amplitude	V_{CC}=5.0V, test circuit below	1.35			V_{PP}

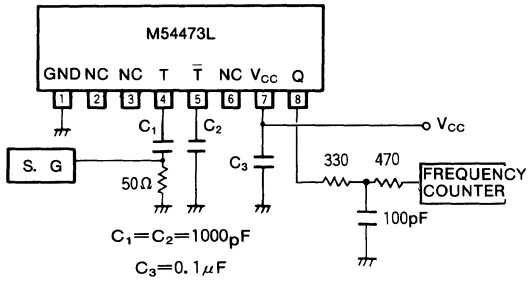
Typical values are at V_{CC}=5.0V, T_a=25℃

TYPICAL CHARACTERISTICS



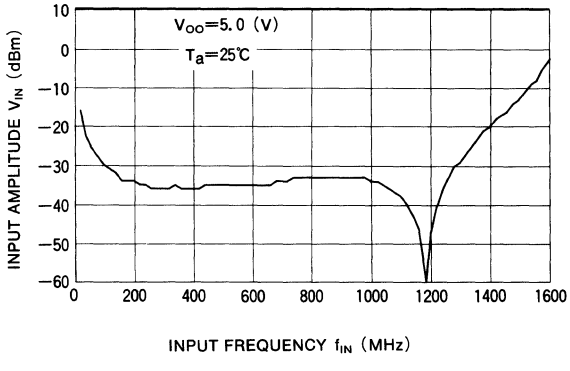
Note 1 ＊Normally NC pins should be grounded
2 The probe capacitance and resistance for output measurement must have the characteristics of C_{IN} <10pF, R_{IN} > 1 MΩ

TEST CIRCUIT



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54475P

1/64,1/65,1/128,1/129 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54475P is a semiconductor integrated circuit consisting of an extremely high-speed 1/64, 1/65, 1/128, 1/129 2-modulus divider using emitter-coupled logic (ECL).

FEATURES

- Extremely high-speed operation (f_{max}=1.0GHz)
- Low power dissipation current (40mA at V_{CC}=5V)
- ECL level output

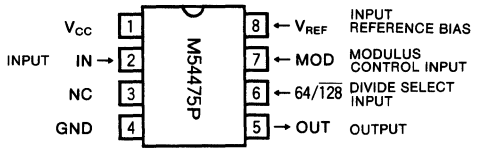
APPLICATION

Prescalers for PLL synthesizers in mobile radio telephones, transceivers, and MCA equipment.

FUNCTION

The M54475P consists of a divider using emitter-coupled logic (ECL). A frequency up to 1.0GHz can be applied to the input pin IN. When divider select input (64/$\overline{128}$) and the modulus control input MOD are high, 1/64 division is provided at the output ; when MOD is low, 1/65 division is provided. When the divider select input (64/$\overline{128}$) is low, and MOD is high, 1/128 division is provided ; when MOD is low, 1/129 division is provided.

PIN CONFIGURATION (TOP VIEW)



Outline 8P4

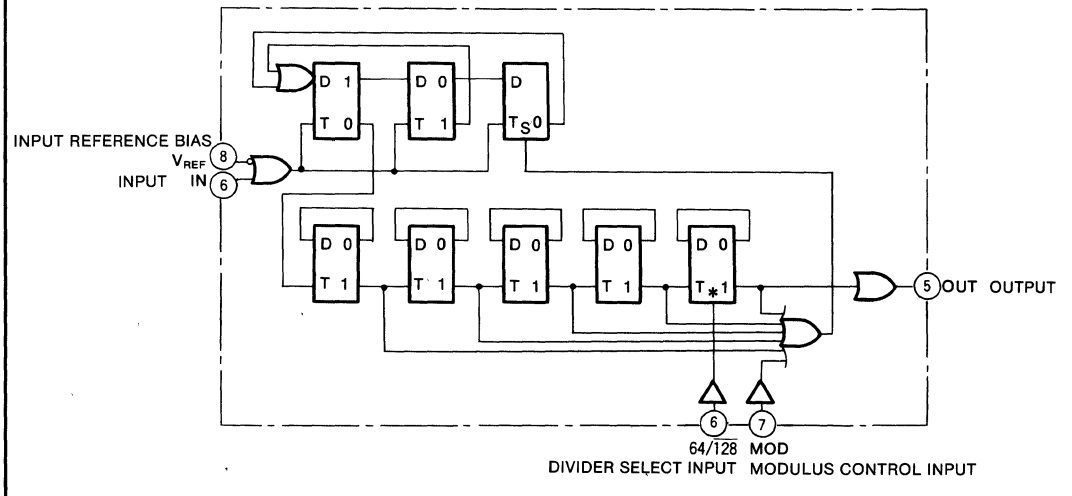
NC : No connection

TRUTH TABLE

64/$\overline{128}$	MOD	DIVIDER SELECT
H	H	1/64
H	L	1/65
L	H	1/128
L	L	1/129

Note 1. 64/$\overline{128}$ inputs
High-level: V_{CC}
Low-level : Open
MOD inputs
High-level: 2.0V~V_{CC}
Low-level : 0~0.8V

BLOCK DIAGRAM



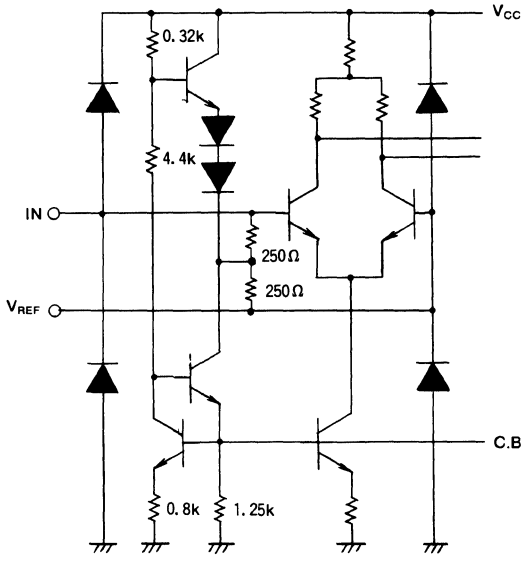
* : When this is high, the clock input signal is output without being divided

MITSUBISHI ELECTRIC

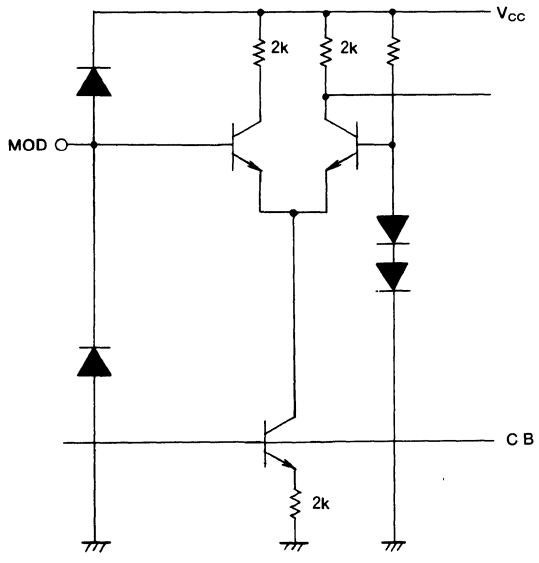
1/64,1/65,1/128,1/129 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

I/O CIRCUIT DIAGRAM

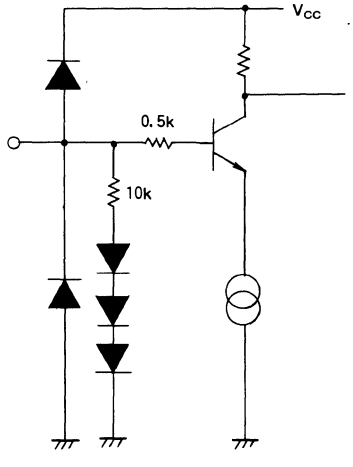
1 IN V_{REF} INPUT



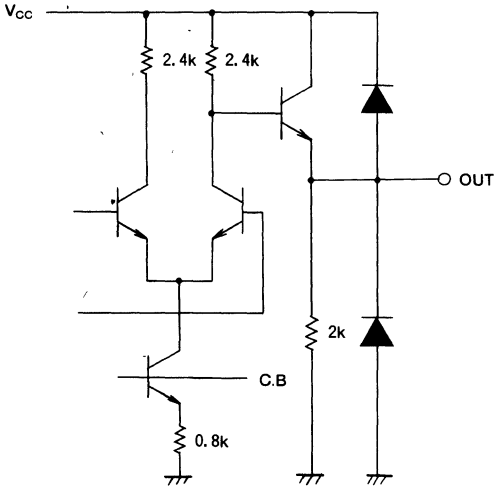
2 MOD INPUT



3 64/$\overline{128}$ INPUT



4 OUTPUT



Note 2. Typical values are at V_{CC}=5V, T_a=25℃.

1/64,1/65,1/128,1/129 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit	Remark
			Min	Max		
V_{CC}	Supply voltage		−0.5	7.0	V	
V_I	Input voltage		−0.5	V_{CC}	V	
I_O	Output current			−10	mA	
Pd	Power dissipation	T_a=75℃		400	mW	Power dissipation of package
Topr	Operating temperature		−20	+75	℃	
Tstg	Storage temperature		−55	+125	℃	

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.5∼5.5V, T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	Remark
			Min	Typ	Max		
V_{CC}	Supply voltage		4.5	5	5.5	V	
F_{IN}	Input frequency	V_{IN} =400mV_{P-P}	100		1000	MHz	Sine wave
V_{IN}	Input amplitude		0.4		1.2	V_{P-P}	
I_O	Output current				−5	mA	
C_L	Output load capacitance				15	pF	

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

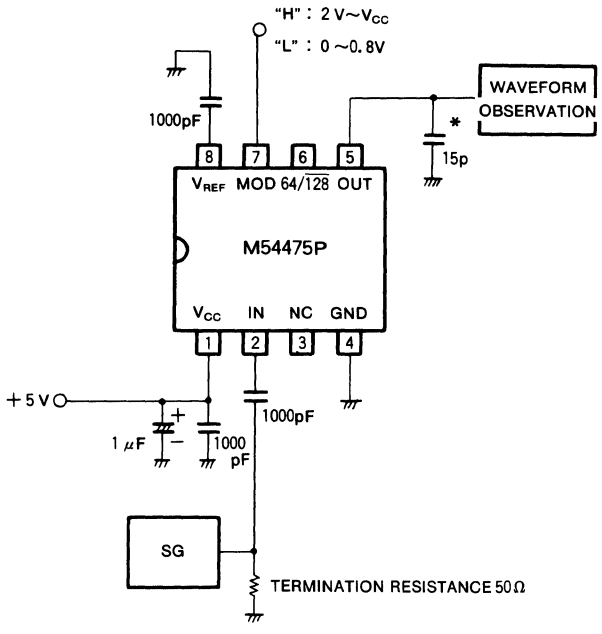
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	MOD 7	V_{CC} =4.5∼5.5V	2		V_{CC}	V
V_{IL}	Low-level input voltage	MOD 7	V_{CC} =4.5∼5.5V	0		0.8	V
I_{IH}	High-level input current	MOD 7	V_{CC} = V_{IN} =5.5V			30	μA
I_{IL}	Low-level input current	MOD 7	V_{CC} =5.5V, V_{IN} = 0V	−20			μA
V_O	Output amplitude	OUT 5	V_{CC} =4.5∼5.5V	0.9	1.2		V
I_{CC}	Supply current		V_{CC} =5.5V		40	60	mA

AC CHARACTERISTICS (V_{CC} = 5V, T_a =25℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IN}	Input sensitivity	IN 2	F_{IN} =100∼1000MHz	0.4		1.2	V_{P-P}
t_S	Set up time	MOD 7	F_{IN} =1000MHz			20	ns

1/64,1/65,1/128,1/129 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

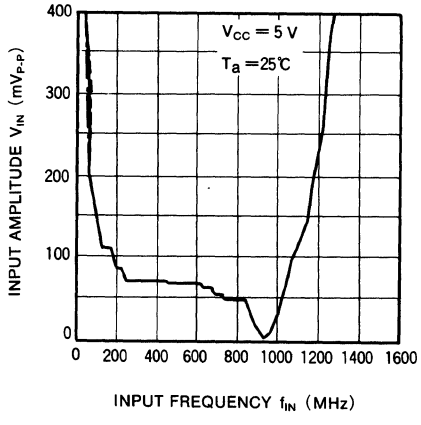
TEST CIRCUIT



* The capacitance includes the probe input capacitance.

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54477P/L

1/128, 1/136 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54477P/L is a semiconductor integrated circuit consisting of a 1/128, 1/136 2-modulus divider using emitter-coupled logic (ECL).

FEATURES

- High-speed operation (f_{max}=1.0GHz)
- Operates at low input amplitudes (−20dBm min)
- ECL level output

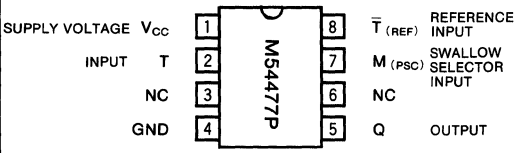
APPLICATION

Prescalers for PLL synthesized TV tuners, and general use in consumer and industrial digital equipment.

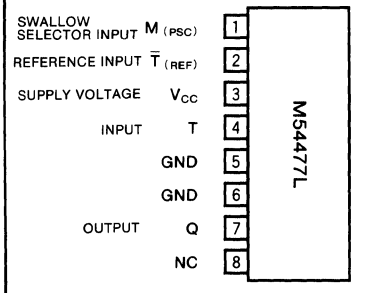
FUNCTION

The M54477P/L, 1/128 or 1/136 prescaler, consists of high speed frequency divider with using an ECL circuit configuration. When the clocks are applied the pulse swallow control input terminal M, the dividing ratio is 1/136, and when M is stable ("H" or "L"), it is 1/128. It operates in the frequency range 80MHz~1000MHz.
The output is ECL level (1.30V_{P-P} typ).

PIN CONFIGURATION (TOP VIEW)



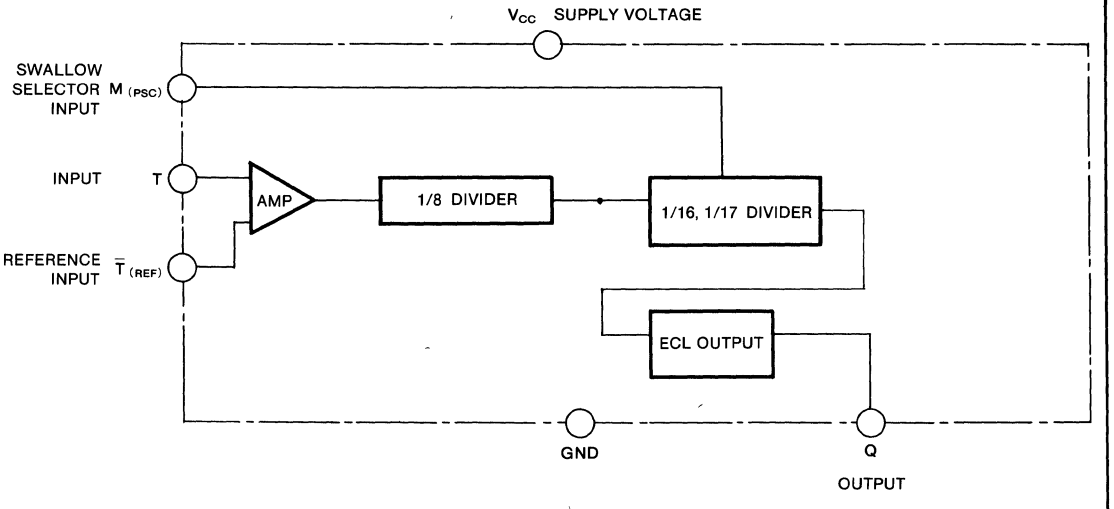
Outline 8P4



Outline 8P5

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/128, 1/136 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
V_I	Input voltage	T, $\overline{T}$ (REF)	0∼V_{CC}	V
Pd	Power dissipation	T_a=25℃	1.15	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

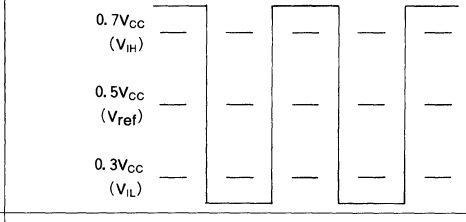
Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	Input amplitude	f_{IN}=80∼1000MHz	−20		4	dBm

ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}	Supply current		V_{CC}=5.5V, T_a=25℃		33	50	mA
V_{IN}	Input sensitivity		f_{IN}=80∼1000MHz	−20		4	dBm
V_O	Output amplitude		f_{IN}=80∼1000MHz, V_{CC}=4.5V	0.9	1.3	1.7	V_{P-P}
V_{IH}	When the dividing ratio is 1/136	High-level input voltage	M terminal ＊Note	0.7V_{CC}			V
V_{IL}		Low-level input voltage	M terminal ＊Note			0.3V_{CC}	V
I_{IH}		High-level input current	M terminal ＊Note V_{CC}=5.0V, V_{IH}=3.5V			50	μA
I_{IL}		High-level input current	M terminal ＊Note V_{CC}=5.0V, V_{IL}=1.5V			−150	μA

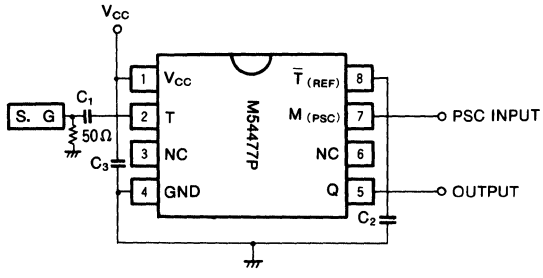
The typical values are at V_{CC}=5.0V, T_a=25℃.

＊Note : Input conditions of pulse swallow control input terminal M

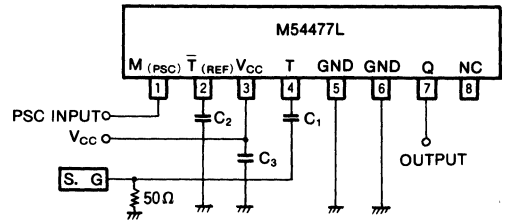
Dividing ratio	Input conditions	Description
1/136		When the clocks are applied to M terminal as shown in the left figure, the dividing ratio changes from 1/128 to 1/136
1/128	V_{IL}=0V, V_{IH}=VCC or V_{IH}=OPEN	M terminal is stable at GND or V_{CC}, or opened

1/128, 1/136 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

TEST CIRCUIT



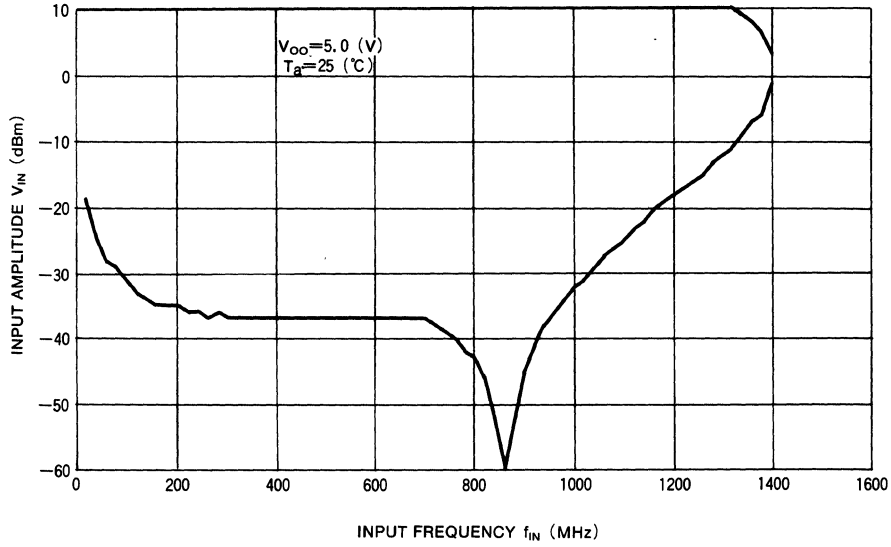
$C_1 \simeq C_2 \simeq 1000_{pF}$, $C_3 \simeq 0.1\mu F$



$C_1 \simeq C_2 \simeq 1000_{pF}$, $C_3 \simeq 0.1\mu F$

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54477AP

1/128,1/136 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54477AP is a semiconductor integrated circuit consisting of a 1/128, 1/136 2-modulus divider using emitter-coupled logic.

FEATURES

- High-speed operation (f_{max}=1.0GHz)
- Operates at low input amplitude (−20dBm min)
- ECL level output

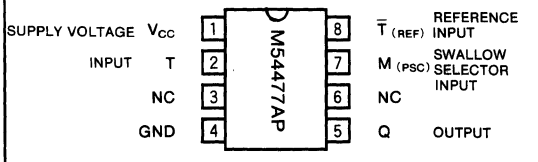
APPLICATION

Prescalers for PLL synthesized TV tuners, and for general use in consumer and industrial digital equipment.

FUNCTION

The M54477AP, 1/128 or 1/136 prescaler, consists of high speed frequency divider with using an ECL circuit configration. When the clocks are applied the pulse swallow control input terminal M, the diving ratio is 1/136, and when M is stable ("H" or "L"), it is 1/128. It operates in the frequency range 80MHz~1000MHz.
The output is ECL level (1.30V_{PP}).

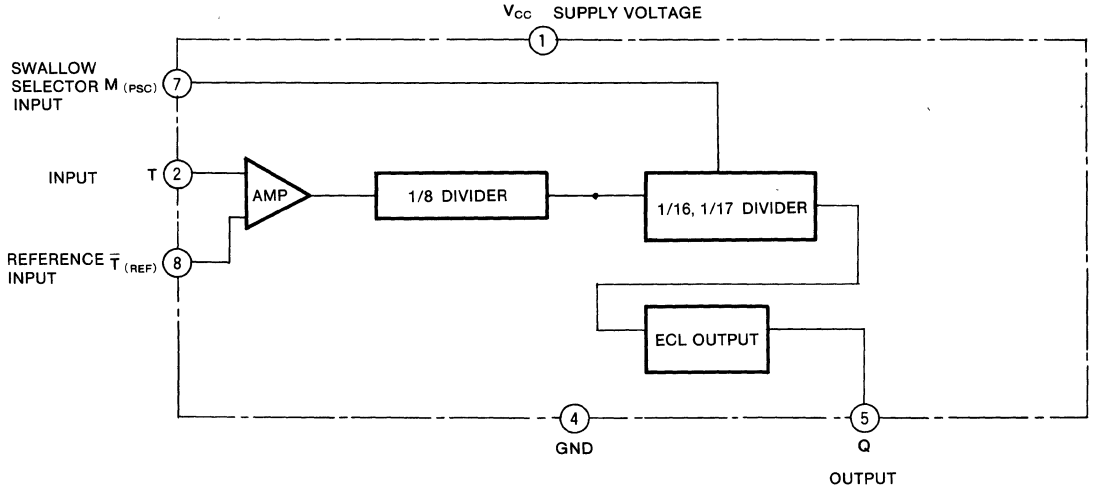
PIN CONFIGURATION (TOP VIEW)



Outline 8P4

NC : No connection

BLOCK DIAGRAM



1/128,1/136 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
V_I	Input voltage	T, $\overline{T}$ (REF) input	0∼V_{CC}	V
Pd	Power dissipation	T_a=25℃	1.15	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

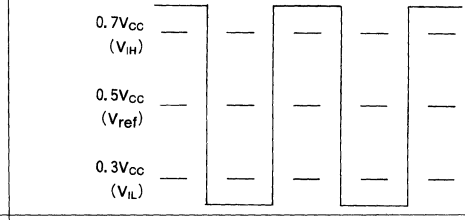
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	Input amplitude	f_{IN}=80∼1000MHz	−20		4	dBm

ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC}	Supply current		V_{CC}=5.5V, T_a=25℃		33	50	mA
V_{IN}	Input sensitivity		f_{IN}=80∼1000MHz	−20		4	dBm
V_O	Output amplitude		f_{IN}=80∼1000MHz, V_{CC}=4.5V	0.9	1.3	1.7	V_{P-P}
V_{IH}	When the dividing ratio is 1/136	High-level input voltage	M terminal ＊Note	0.7V_{CC}			V
V_{IL}		Low-level input voltage	M terminal ＊Note			0.3V_{CC}	V
I_{IH}		High-level input current	M terminal ＊Note V_{CC}=5.0V, V_{IH}=3.5V			50	μA
I_{IL}		High-level input current	M terminal ＊Note V_{CC}=5.0V, V_{IL}=1.5V			−150	μA

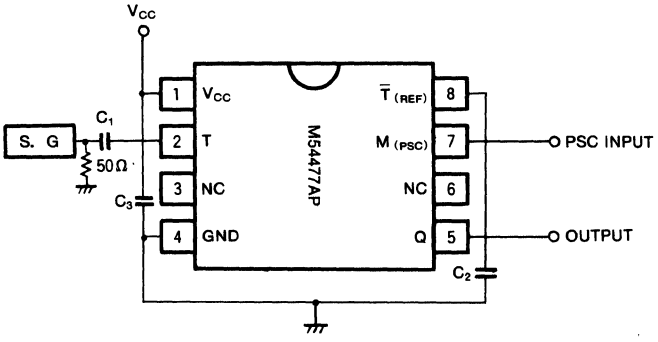
The typical values are at V_{CC}=5.0V, T_a=25℃.

＊Note : Input conditions of pulse swallow control input terminal M

Divider select	Input conditions	Description
1/136		When the clocks are applied to M terminal as shown in the left figure, the dividing ratio changes from 1/128 to 1/136
1/128	V_{IL}=0V, V_{IH}=VCC or V_{IH}=OPEN	M terminal is stable at GND, or V_{CC}, or opened.

1/128,1/136 2-MODULUS HIGH SPEED DIVIDER WITH ECL OUTPUT

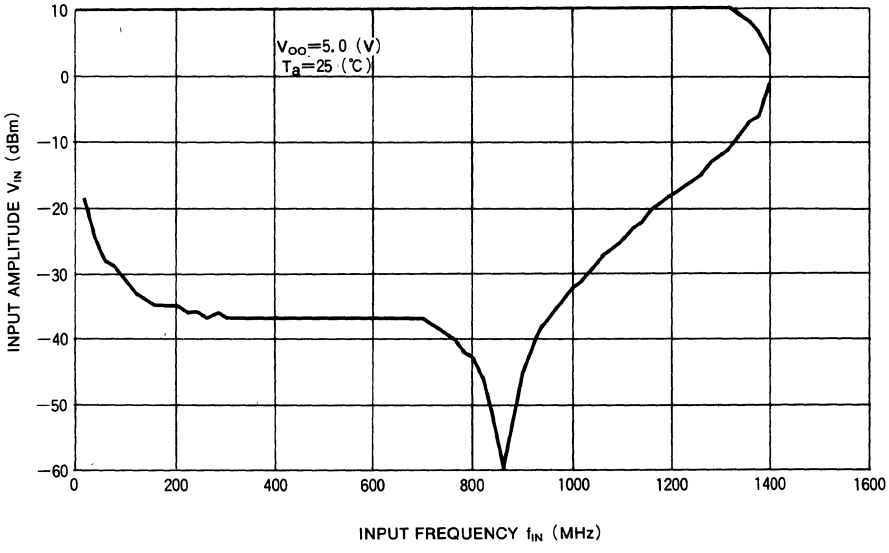
TEST CIRCUIT



$C_1 \simeq C_2 \simeq 1000_{p}F$, $C_3 \simeq 0.1\mu F$

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54478P

1/256 HIGH SPEED DIVIDER WITH ECL OUTPUT

DESCRIPTION

The M54478P is a semiconductor integrated circuit consisting of an high-speed 1/256 divider using emitter-coupled logic.

FEATURES

- High-speed operation (f_{max}=1.0GHz)
- Operates at low input amplitude (−20dBm min)
- ECL level output
- Low power dissipation (I_{CC} 30mA typ)

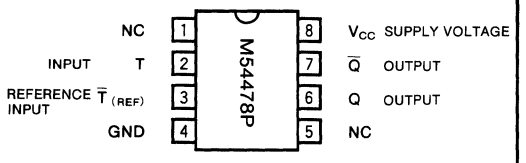
APPLICATION

Prescalers for PLL synthesized TV tuners, and general use in industrial and consumer digital equipment

FUNCTIONAL DESCRIPTION

The M54478P consists of a divider using emitter-coupled logic (ECL). When a frequency from 80 through 1,000MHz is applied to the input pin T, the 1/256 divided frequency is obtained.
The outputs Q, $\overline{Q}$ are ECL level.

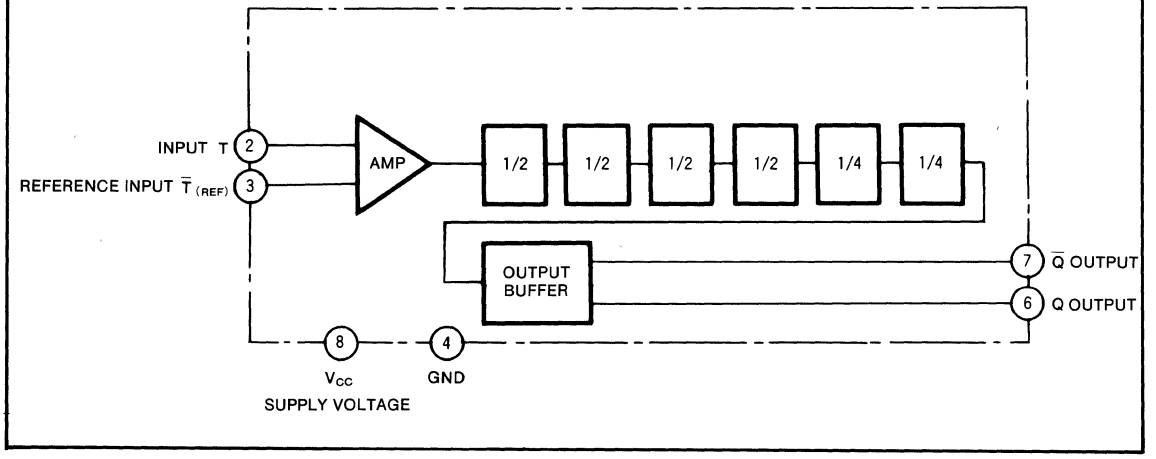
PIN CONFIGURATION (TOP VIEW)



Outline 8P4

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/256 HIGH SPEED DIVIDER WITH ECL OUTPUT

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7.0	V
V_i	Input voltage	T, $\overline{T}_{(REF)}$ Input	0∼V_{CC}	V
P_d	Power dissipation	T_a=25℃	400	mW
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃)

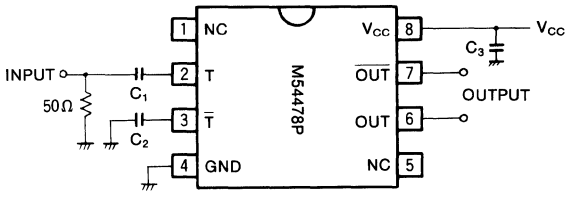
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	Input amplitude	f_{IN}=80∼1000MHz	−20		4	dBm

ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5.5V		30	42	mA
V_{IN}	Input sensitivity	f=80∼1000MHz	−20		4	dBm
V_O	Output amplitude	V_{CC}=4.5V	0.7	1.2	1.5	V_{P-P}
V_{OH}	High-level output level	V_{CC}=5.0V		4.3		V
V_{OL}	Low-level output level	V_{CC}=5.0V		3.1		V

Typical values are at V_{CC}=5.0V, T_a=25℃.

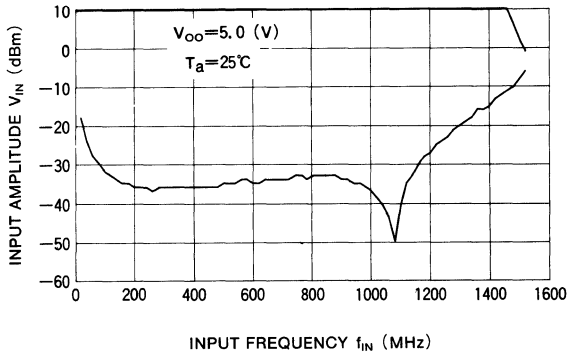
TEST CIRCUIT



C_1=C_2=1000pF C_3=0.1μF

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54479P

1/64 HIGH SPEED DIVIDER

DESCRIPTION

The M54479P is a semiconductor integrated circuit consisting of an extremely high-speed 1/64 divider using emitter-coupled logic.

FEATURES

- Extremely high-speed operation (f_{max}=1.9GHz)
- Low power dissipation current (I_{CC}=35mA)
- 10-pin mini-flat package

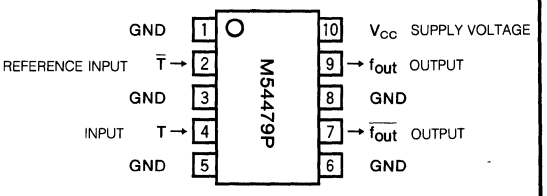
APPLICATION

TV and CATV tuners

FUNCTION

The M54479P consists of an extremely high-speed divider using emitter-coupled logic for applications in TV and CATV equipment. The maximum speed of the divider is 1.9GHz, and division ratio is fixed to 1/64. The output is emitter-coupled logic (ECL) level.

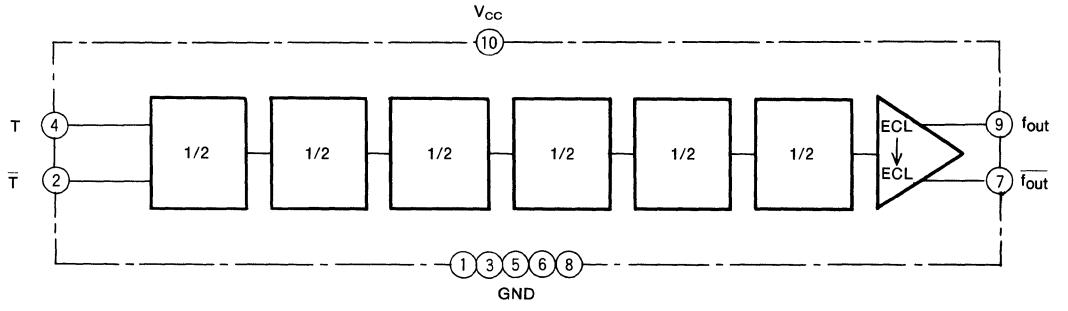
PIN CONFIGURATION (TOP VIEW)



Outline 10P2-C

NC : No connection

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Symbol	Pin name	Functional description	Pin number
V_{CC}	Supply voltage	Supply voltage pin 5.0±0.5V is applied	10
GND	GND	Connect to 0V.	1, 3, 5, 6, 8
T	Prescaler input	Prescaler input pin	4
$\overline{T}$	Reference input	Connect a capacitance of 1000pF between the wire and GND line.	2
f_{out}	Division output	Division output is ECL level	9
$f_{\overline{out}}$	Inverted division output	Inverted division output	7

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+65℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
VI	Input voltage	T, $\overline{T}$	6.5	V
P_d	Power dissipation		300	mW
Topr	Operating temperature		−20∼65	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+65℃, unless otherwise noted)

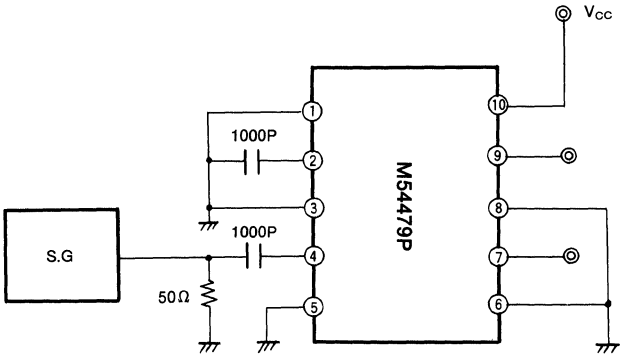
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
fopr	Operating frequency	f_{IN} input	0.7		1.9	GHz

ELECTRICAL CHARACTERISTICS (T_a=−20∼65℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5.5V		35	50	mA
V_O	Output amplitude	V_{CC}=4.5V, f_{IN}=1.0GHz T_a=25℃	350		700	mV_{P-P}
V_{IN}	Input sensitivity	f_{IN}=0.7∼1.9GHz	−8		+3	dBm*

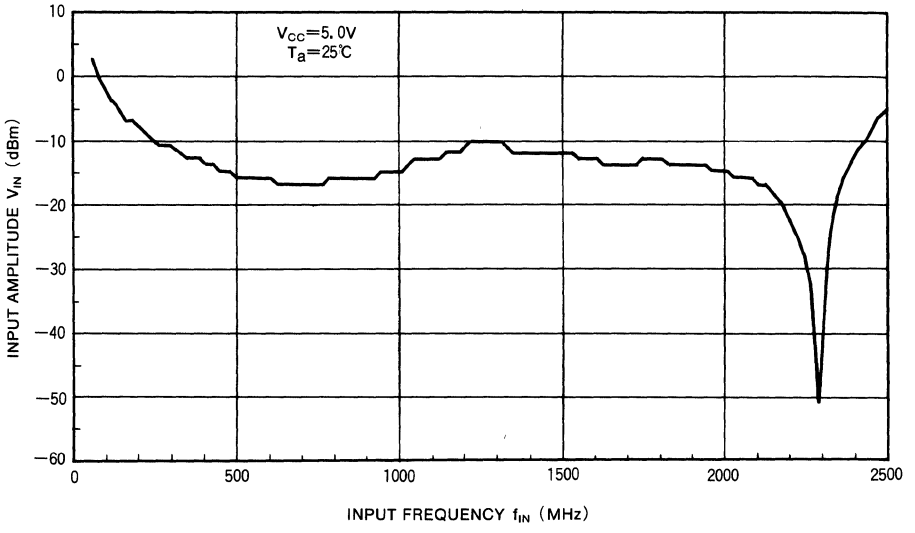
* : dBm (50Ω)
Typical values are at V_{CC}=5.0V, T=25℃.

TEST CIRCUIT



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54480P

RGB DECODER

DESCRIPTION

The M54480P is a semiconductor integrated circuit consisting of an ECL-gate RGB decoder capable of 8 -, 16-, and 64-color display.

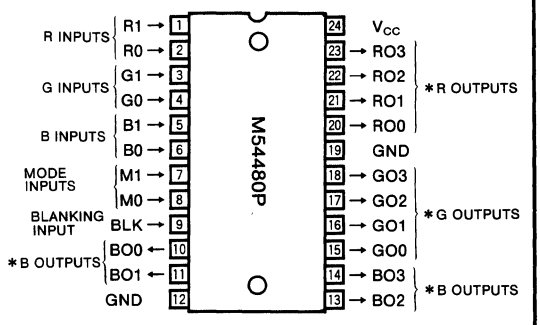
FEATURES

- Three color display modes (8 , 16 and 64 colors)
- Pixel rate over 30MHz is suitable for high-resolution display applications.
- Output skew : less than 5 ns
- Built-in blanking function
- Output drive current>30mA

APPLICATION

Color displays and monitors for use with personal computers

PIN CONFIGURATION (TOP VIEW)



Outline 24P4

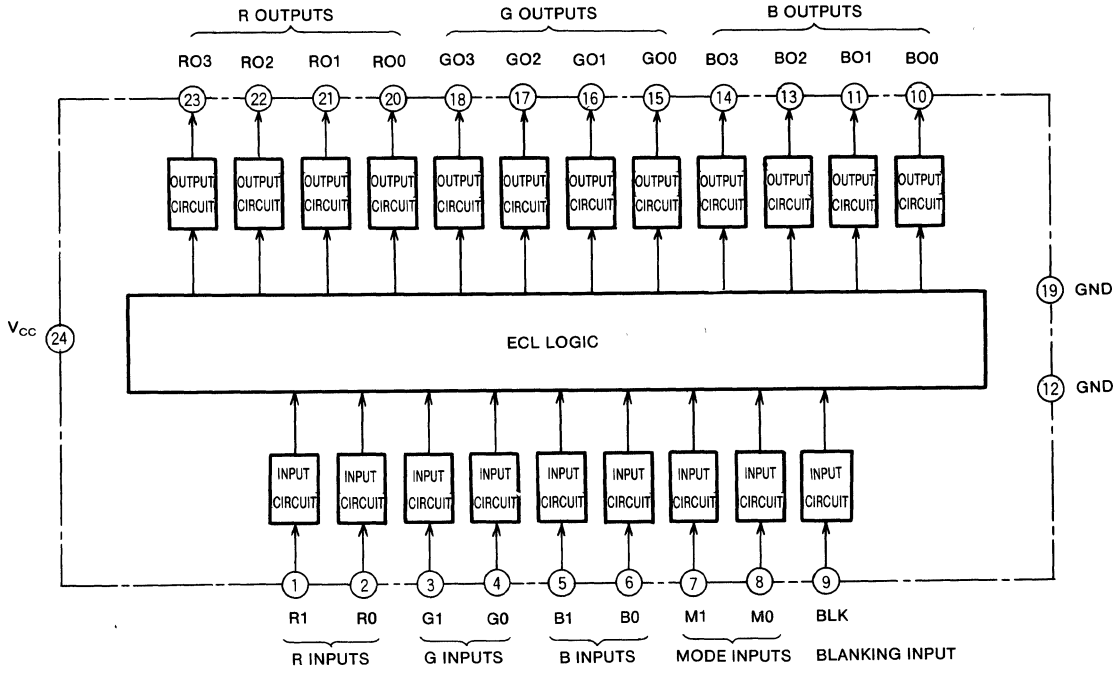
* : Open collector

FUNCTION

THe M54480P is an RGB decoder for personal computer displays with three 8 -, 16- and 64-color modes. Setting M 1 high and M 0 low selects the 8 -color mode; setting M 1 and M 0 both low selects the 16-color mode; setting M 1 and M 0 both high or M 1 low and M 0 high selects the 64-color mode.

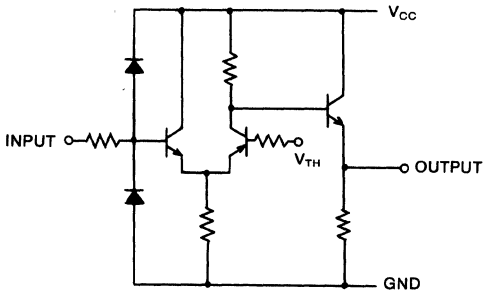
Blanking is enable by setting blanking pin BLK low. The maximum pixel rate is 30MHz. The outputs are open-collectors.

BLOCK DIAGRAM

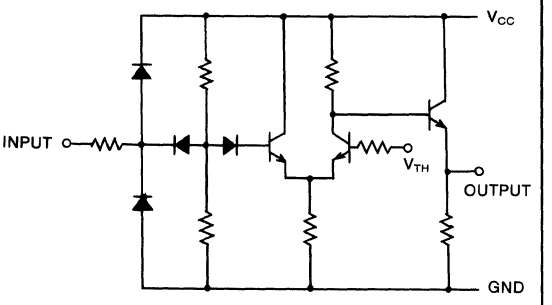


I/O CIRCUIT DIAGRAM

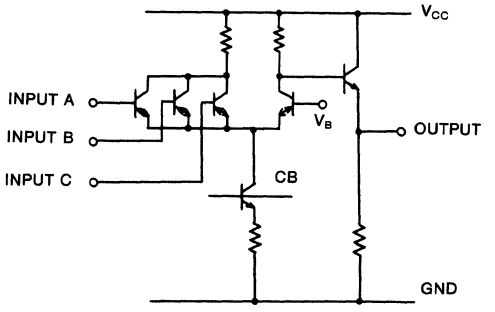
1 Input Circuit (R, G, B Inputs)



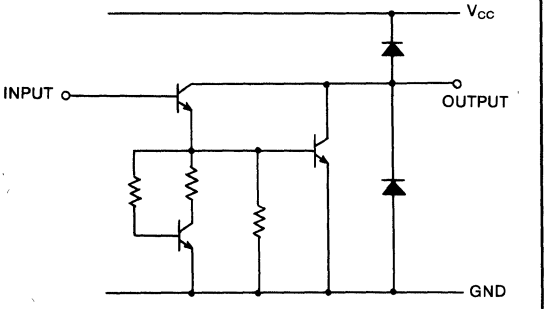
2 Input Circuit (M 1, M 0, BLK Inputs)



3 Internal Circuit

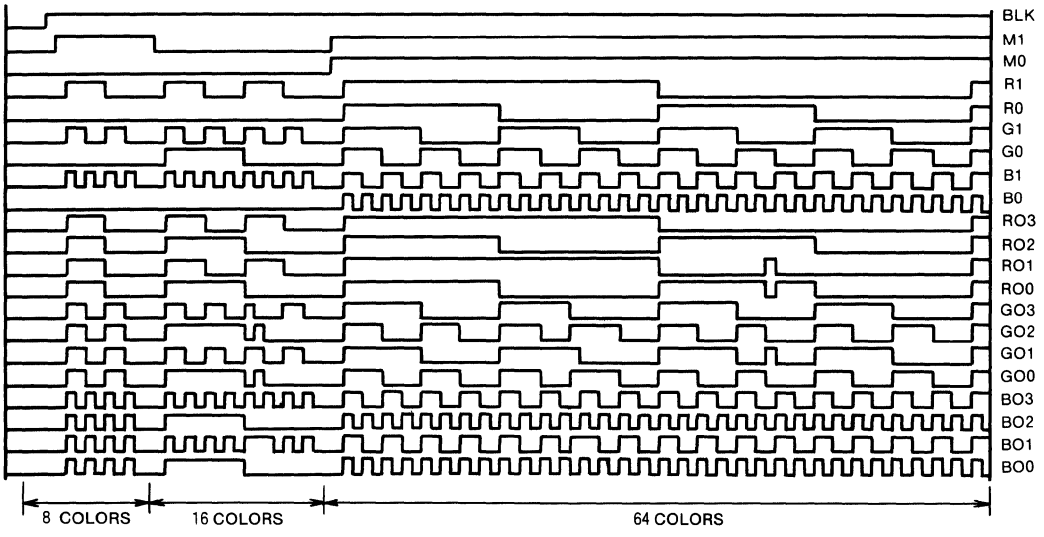


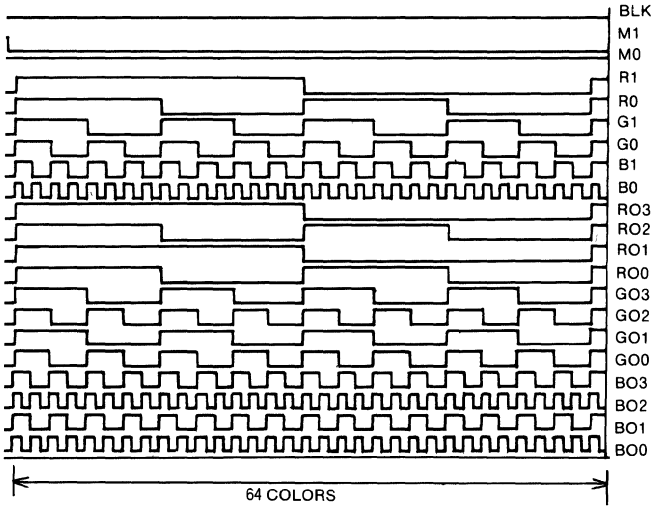
4 Output Circuit (R, G, B Outputs)



MITSUBISHI ELECTRIC

OPERATING TIMING CHART





ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+65℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
V_I	Input voltage		6.5	V
V_O	Output voltage	$V_O \leqq V_{CC}$	6.5	V
P_d	Power dissipation	V_{CC}=6.5V, T_a=25℃	1.3	W
Topr	Operating temperature		−20∼+65	℃
Tstg	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+65℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
I_{OL}	Low-level output current		0		30	mA
P. R	Pixel Rate		0		30	MHz

ELECTRICAL CHARACTERISTICS (T_a=−20∼+65℃, unless otherwise noted)

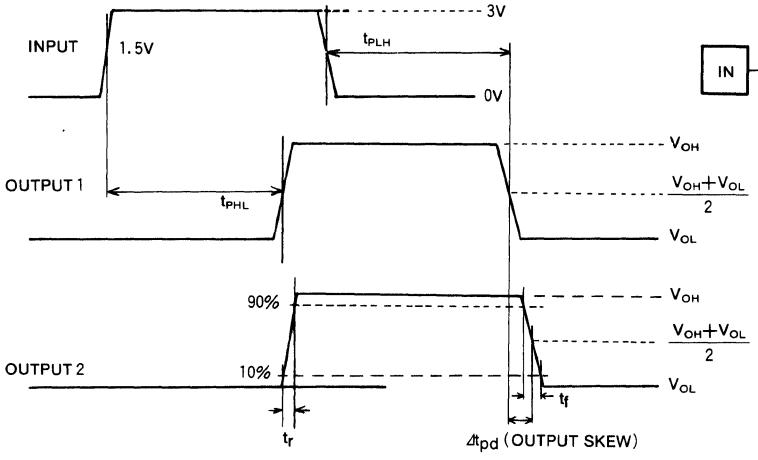
Symbol	Parameter	Test pin	Test Conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	1∼6		2.0		V_{CC}+0.3	V
		7∼9		2.5			
V_{IL}	Low-level input voltage	1∼6				0.7	V
		7∼9				0.7	
I_{IH}	High-level input current	1∼6	V_{CC}=5.25V, V_{IH}=2.0V			+30	μA
		7∼9	V_{CC}=5.25V, V_{IH}=2.0V	−20		+20	
I_{IL}	Low-level input current	1∼6	V_{CC}=5.25V, V_{IH}=0.7V	−20		+20	μA
		7∼9	V_{CC}=5.25V, V_{IH}=0.7V	−300	−200		
V_{OL}	Low-level output voltage	10, 11 13∼18 20∼23	V_{CC}=5.25V, I_{OL}=30mA		0.4	0.6	V
I_{OLK}	Output leakage current	10, 11 13∼18 20∼23	V_{CC}=5.25V, V_O=5.25V			25	μA
I_{CCL}	Low-level supply current	24	V_{CC}=5.25V, all outputs ON		145	180	mA
I_{CCH}	High-level supply current	24	V_{CC}=5.25V, all outputs OFF		116	150	mA

Typical values are at V_{CC}=5.0V, T_a=25℃.

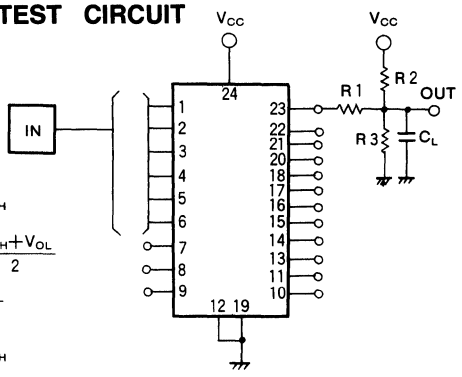
SWITCHING CHARACTERISTICS (V_{CC}=5.0V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to high-level output propagation time	10, 11 13∼18 20∼23	C_L=10.8pF R_1=220Ω R_2=75Ω R_3=680Ω	20	38	50	ns
t_{PHL}	High-to low-level output propagation time	10, 11 13∼18 20∼23		20	38	50	ns
O. S	OUTPUT SKEW	10, 11 13∼18 20∼23				5	ns
P. R	Pixel Rate	10, 11 13∼18 20∼23		30			MHz
t_r	Rise time	10, 11 13∼18 20∼23				10	ns
t_f	Fall time	10, 11 13∼18 20∼23				10	ns

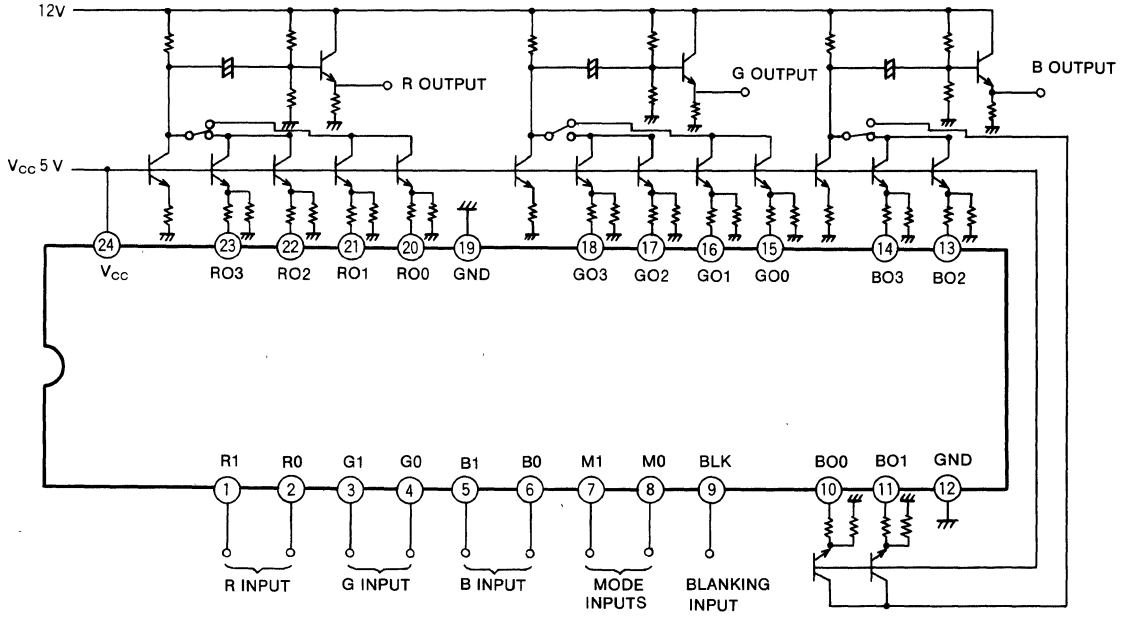
TIMING CHART



TEST CIRCUIT



APPLICATION EXAMPLE



M54502P

DUAL AND GATE WITH DRIVE TRANSISTOR

DESCRIPTION

The M54502P is a semiconductor integrated circuit containing two TTL AND gates and two high current, high breakdown voltage transistors.

FEATURES

- High driving current ($I_{O(max)}$=600mA)
- High breakdown voltage output ($V_{O(max)}$=30V)
- AND gate and transistor are separated.
- Strobe input provided

APPLICATION

General purpose, for use in industrial and consumer digital equipment. Suitable for driving magnetic relays and lamps.

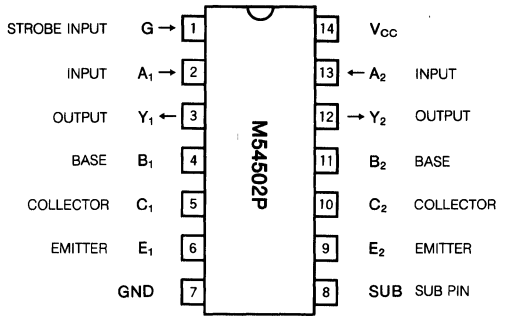
FUNCTION

The M54502P consists of two driver circuits, each having a two input AND gate and a high current, high breakdown voltage transistor. The AND gates and transistors are independent of each other and therefore possible to use as individual circuits. If AND gate output Y is externally connected to base B of the transistor, the unit can be used to drive a magnetic relay or lamp directly. Besides this, the unit can be used as a translater either from TTL to MOS, or from MOS to TTL. With all these features an extremely wide range of usage is ensured.
The AND gate can be directly connected to either TTL or DTL.

FUNCTION TABLE 〈AND Gate〉

A	G	Y
H	H	H
H	L	L
L	H	L
L	L	L

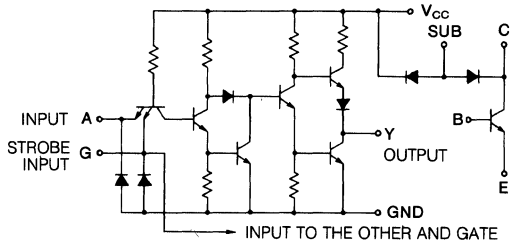
PIN CONFIGURATION (TOP VIEW)



ALWAYS ENSURE THAT SUB PIN IS CONNECTED TO THE LOWEST VOLTAGE POINT (EQUAL TO OR LOWER THAN GND)

Outline 14P4

CIRCUIT SCHEMATIC (EACH DRIVER)



ABSOLUTE MAXIMUM RATINGS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage (output state High) (Note 1)		V_{CC}	V
V_O	Output voltage (output state High) (Note 2)		30	V
I_O	Output current (output state Low) (Note 2)		600	mA
V_{VS}	V_{CC} to substrate voltage		70	V
V_{CS}	Collector to substrate voltage		70	V
V_{CBO}	Collector to base voltage		70	V
V_{CER}	Collector to emitter voltage (R_{BE} = 500Ω)		65	V
V_{EBO}	Emitter to base voltage		5	V
I_C	Collector current		600	mA
P_d	Power dissipation	T_a = 25℃	1.19	W
T_{opr}	Operating temperature		0~75	℃
Tstg	Storage temperature		−65~+150	℃

Note 1 : When gate only is in use.
2 : When gate output is connected to the base of an output transistor.

RECOMMENDED OPERATING CONDITIONS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{CEO}	Collector to emitter voltage			24	V
I_C	Collector current			300	mA

ELECTRICAL CHARACTERISTICS (T_a = 0~75℃, unless otherwise noted)

⟨TTL Gate⟩

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V, V_I = 2V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 0.8V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (A)	V_{CC} = 5.5V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IH}	High-level input current (G)	V_{CC} = 5.5V	V_I = 2.4V			80	μA
			V_I = 4.5V			120	
I_{IL}	Low-level input current (A)	V_{CC} = 5.5V, V_I = 0.4V				−1.6	mA
I_{IL}	Low-level input current (G)	V_{CC} = 5.5V, V_I = 0.4V				−3.2	mA
I_{OS}	Output short-circuit current	V_{CC} = 5.5V, V_O = 4.5V		−18		−55	mA
I_{CCH}	High-level supply current	V_{CC} = 5.5V, V_I = 4.5V				11	mA
I_{CCL}	Low-level supply current	V_{CC} = 5.5V, V_I = 0V				20	mA

⟨Characteristics when TTL Gate and output transistor are connected⟩

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = 4.5V, V_I = 0.8V, V_O = 30V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 2V, I_{OL} = 100mA			0.4	V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 2V, I_{OL} = 300mA			0.7	V
I_{CCL}	Low-level supply current	V_{CC} = 5.5V, V_I = 5V			95	mA

⟨Output transistor⟩

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{(BR)CBO}$	Collector to base breakdown voltage	I_C = 100μA, I_E = 0mA	70			V
$V_{(BR)CER}$	Collector to emitter breakdown voltage	I_C = 100μA, R_{BE} = 500Ω	65			V
$V_{(BR)EBO}$	Emitter to base breakdown voltage	I_E = 100μA, I_C = 0mA	5			V
h_{FE}	Direct current amplification factor (Note 3)	V_{CE} = 3V, I_C = 100mA, T_a = 25℃	25			—
		V_{CE} = 3V, I_C = 300mA, T_a = 25℃	30			
		V_{CE} = 3V, I_C = 100mA, T_a = 0℃	20			
		V_{CE} = 3V, I_C = 300mA, T_a = 0℃	25			
V_{BE}	Base to emitter voltage	I_B = 10mA, I_C = 100mA			1	V
		I_B = 30mA, I_C = 300mA			1.2	
$V_{CE(sat)}$	Collector to emitter saturation voltage	I_B = 10mA, I_C = 100mA			0.4	V
		I_B = 30mA, I_C = 300mA			0.7	

Note 3 : Measurement should be done in a short time.

PRECAUTIONS FOR USE (WHEN TTL GATE AND OUTPUT TRANSISTOR ARE CONNECTED)

The permissible amount of collector current of the output transistor I_O varies according to the conditions. Calculate it as follows, using Fig. 1 "Heat Dissipation Rate Characteristics", Fig. 2 "Pulse Power Chart", and the following formula.

$$P_d = \frac{V_{CC}}{M+N}(M \cdot I_{CCL} + N \cdot I_{CCH}) + M \cdot I_O \cdot V_{OL} \cdots\cdots(1)$$

Where P_d : Power dissipation
I_{CCL} : Supply current when all outputs of output transistors are "Low".
I_{CCH} : Supply current when all outputs of output transistors are "High".
V_{OL} : Output voltage when output is "Low".
M : The number of output transistors whose state is "Low".
N : The number of output transistors whose state is "High".
M+N : The total number of gates included in one package.

When trying to determine permissible amount of constant current, first, read the largest permissible power dissipation P_d for the given operating free-air ambient temperature range from Fig. 1. Then calculate I_O by substituting into Formula (1) the maximum values of I_{CCL}, I_{CCH} and V_{CC} as well as values M and N.

When calculating pulse current I_O, use Fig. 2. First, determine maximum permissible power dissipation P_d from the duty cycle and pulse width, then calculate using Formula (1). In this case, be careful that I_O does not exceed the absolute maximum rating.

TYPICAL CHARACTERISTICS

Fig.1 "HEAT DISSIPATION RATE CHARACTERISTICS"

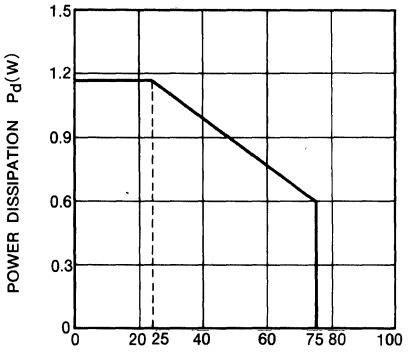
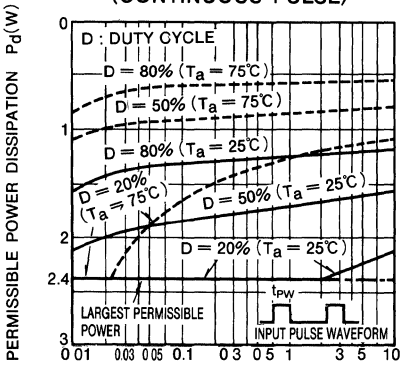


Fig.2 PULSE POWER CHART (CONTINUOUS PULSE)



MITSUBISHI ELECTRIC

SAFE RANGE OF OPERATION FOR THE OUTPUT TRANSISTOR (WHEN USED INDEPENDENTLY OF TTL GATE)

Both Fig. 3 and Fig. 4 show the safe operating ranges of output transistors when they are separate from and independent of the gates. Fig. 4 gives characteristics when t_{PW} = 20ms. When used for values other than 20ms determine the safe operating range using the method given below.

Calculate P_C using Formula (2). (P_C being the total of collector dissipation of all "ON" transistors)

$$P_C = P_d - \frac{V_{CC}}{M+N}(M \cdot I_{CCL} + N \cdot I_{CCH}) \cdots\cdots(2)$$

Where P_d : Permissible power dissipation read from Fig. 1 and Fig. 2.

I_{CCL} : Supply current when gate output state is "Low".

I_{CCH} : Supply current when gate output state is "High".

(NOTE: The values of I_{CCL} and I_{CCH} will vary somewhat depending on the load connected to gate outputs.)

After using Formula (2) to calculate P_C, enter it into the following Formula (3) to find the safe operating range.

$$P_C = V_{CE} \cdot I_C \cdots\cdots(3)$$

However, the absolute maximum rating of $V_{CE} \leqq 30V$ and $I_C \leqq 600mA$ must be observed.

Note that Figs 3 and 4 express power dissipation per package. Therefore, one transistor may consume all the power indicated in Fig. 3 and Fig. 4 if the other transistor and the gates are not used.

Fig.3 SAFE OPERATING RANGE OF OUTPUT TRANSISTOR (ONE SHOT PULSE)

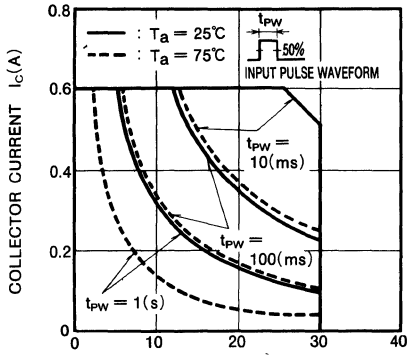
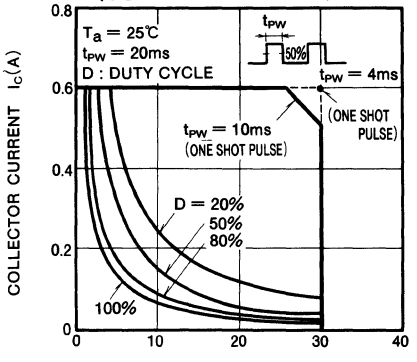


Fig.4 SAFE OPERATING RANGE OF OUTPUT TRANSISTOR (CONTINUOUS PULSE)



M54503P

QUADRUPLE CURRENT DRIVER

DESCRIPTION

The M54503P is a semiconductor integrated circuit containing four TTL NAND drivers with high current, high voltage outputs.

FEATURES

- High driving current ($I_{C(max)}$=200mA)
- High breakdown voltage output ($V_{O(max)}$=30V)
- Having 4 integrated circuits, it has an excellent space factor.

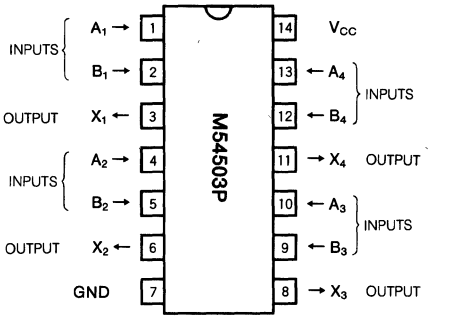
APPLICATION

General purpose, for use in industrial and consumer digital equipment. Suitable for driving magnetic relays and lamps.

FUNCTION

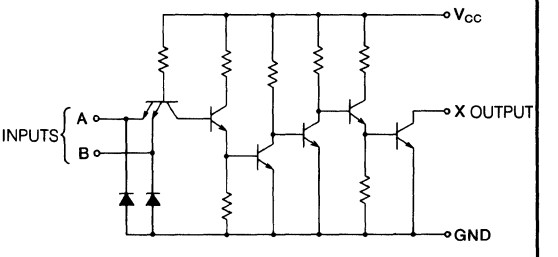
An integrated circuit consisting of 4 TTL driver NAND gate circuits. Having high current, high breakdown voltage output transistors, it can drive magnetic relays and lamps directly. Inputs can be directly connected to TTL or DTL.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH DRIVER)



FUNCTION TABLE

A	B	X
H	H	L
H	L	H
L	H	H
L	L	H

ABSOLUTE MAXIMUM RATINGS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage (output state High)		30	V
I_O	Output current (output state Low)		200	mA
P_d	Power dissipation	T_a = 25℃	1.19	W
Topr	Operating temperature		0~75	℃
Tstg	Storage temperature		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_O	Output voltage (output state High)			24	V
I_O	Output current (output state Low)			100	mA

ELECTRICAL CHARACTERISTICS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current	V_{CC} = 4.5V, V_I = 0.8, V_O = 30V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 2V, I_{OL} = 100mA				0.7	V
I_{IH}	High-level input current	V_{CC} = 5.5V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IL}	Low-level input current	V_{CC} = 5.5V, V_I = 0.4V				−1.6	mA
I_{CCH}	High-level supply current	V_{CC} = 5.5V, V_I = 0V				50	mA
I_{CCL}	Low-level supply current	V_{CC} = 5.5V, V_I = 5V				120	mA

PRECAUTIONS FOR USE

The permissible amount of output current I_O (1 unit) varies according to the conditions. Calculate it as follows, using Fig. 1 "Heat Dissipation Rate Characteristics", Fig. 2 "Pulse Power Chart", and the following formula.

$$P_d = \frac{V_{CC}}{M+N}(M \cdot I_{CCL} + N \cdot I_{CCH}) + M \cdot I_O \cdot V_{OL} \cdots\cdots(1)$$

Where P_d : Power dissipation

I_{CCL} :Supply current when all outputs are "Low".

I_{CCH} :Supply current when all outputs are "High".

V_{OL} : Output voltage when the output "Low".

M : The number of gates whose outputs are "Low".

N : The number of gates whose outputs are "High".

M+N : The total number of gates included in one package.

When trying to determine permissible amount of constant current, first, read the largest permissible power consumption P_d for the given operating free-air ambient temperature range from Fig.1. Then calculate I_O by substituting into Formula (1) the maximum values of I_{CCL}, I_{CCH} and V_{CC} as well as values M and N.

Use Fig.2 to calculate pulse current I_O. First, determine maximum permissible power dissipation P_d from duty cycle and pulse width, then calculate using Formula (1). Be careful that I_O does not exceed absolute maximum rating.

TYPICAL CHARACTERISTICS

Fig.1 HEAT DISSIPATION RATE CHARACTERISTICS

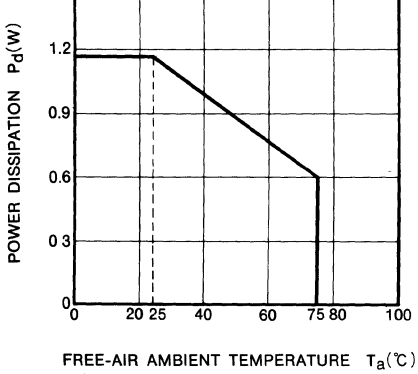
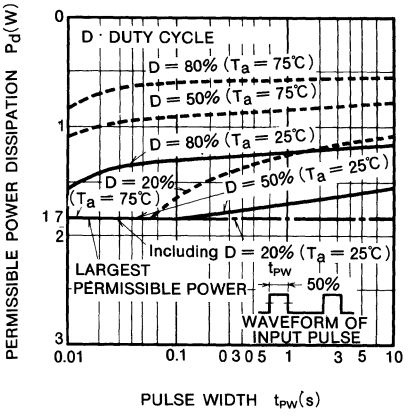


Fig.2 PULSE POWER CHART (CONTINUOUS PULSE)



M54504P

DUAL NAND GATE WITH DRIVE TRANSISTOR

DESCRIPTION

The M54504P is a semiconductor integrated circuit containing two TTL NAND gates and two high current, high breakdown voltage transistors.

FEATURES

- High driving current ($I_{O(max)}$=600mA)
- High breakdown voltage output ($V_{O(max)}$=30V)
- NAND gate and transistor are separated.
- Strobe input provided

APPLICATION

General purpose, for use in industrial and consumer digital equipment. For driving magnetic relays and lamps.

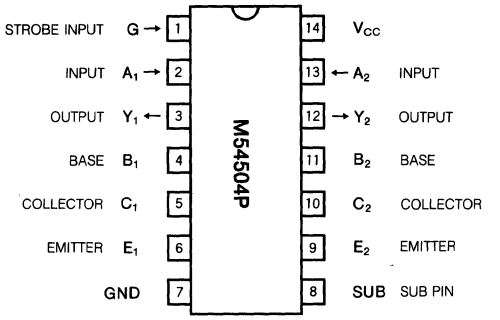
FUNCTION

The M54504P consists of two driver circuits, each having a two input NAND gate and a high current, high breakdown voltage transistor. The NAND gates and transistors are independent of each other and therefore possible to use as individual circuits. If NAND gate output Y is externally connected to base B of the transistor, the unit can be used to drive a magnetic relay or lamp directly. Besides this, the unit can be used as a translater either from TTL to MOS, or from MOS to TTL. With all these features an extremely wide range of usage is ensured.
The NAND gate can be directly connected to either TTL or DTL.

FUNCTION TABLE 〈NAND Gate〉

A	G	Y
H	H	L
H	L	H
L	H	H
L	L	H

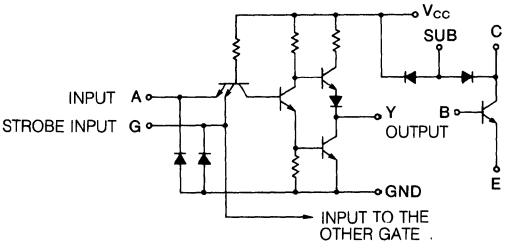
PIN CONFIGURATION (TOP VIEW)



ALWAYS ENSURE THAT SUB PIN IS CONNECTED TO THE LOWEST VOLTAGE POINT (EQUAL TO OR LOWER THAN GND)

Outline 14P4

CIRCUIT SCHEMATIC (EACH DRIVER)



ABSOLUTE MAXIMUM RATINGS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage (output state High) (Note 1)		V_{CC}	V
V_O	Output voltage (output state High) (Note 2)		30	V
I_O	Output current (output state Low) (Note 2)		600	mA
V_{VS}	V_{CC} to substrate voltage		70	V
V_{CS}	Collector to substrate voltage		70	V
V_{CBO}	Collector to base voltage		70	V
V_{CER}	Collector to emitter voltage (R_{BE} = 500Ω)		65	V
V_{EBO}	Emitter to base voltage		5	V
I_C	Collector current		600	mA
P_d	Power dissipation	T_a = 25℃	1.19	W
T_{opr}	Operating temperature		0~75	℃
Tstg	Storage temperature		−65~+150	℃

Note 1 : When gate only is in use.
2 : When gate output is connected to the base of an output transistor

RECOMMENDED OPERATING CONDITIONS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
F_O	Fan out			10	—
V_{CEO}	Collector to emitter voltage			24	V
I_C	Collector current			300	mA

ELECTRICAL CHARACTERISTICS (T_a = 0~75℃, unless otherwise noted)

⟨TTL Gate⟩

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V, V_I = 0.8V, I_{OH} = −400 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 2V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (A)	V_{CC} = 5.5V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IH}	High-level input current (G)	V_{CC} = 5.5V	V_I = 2.4V			80	μA
			V_I = 4.5V			120	
I_{IL}	Low-level input current (A)	V_{CC} = 5.5V, V_I = 0.4V				−1.6	mA
I_{IL}	Low-level input current (G)	V_{CC} = 5.5V, V_I = 0.4V				−3.2	mA
I_{OS}	Output short circuit current	V_{CC} = 5.5V, V_I = 0V		−18		−55	mA
I_{CCH}	High-level supply current	V_{CC} = 5.5V, V_I = 0V				4	mA
I_{CCL}	Low-level supply current	V_{CC} = 5.5V, V_I = 4.5V				11	mA

⟨Characteristics when TTL Gate and output transistor are connected⟩

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = 4.5V, V_I = 2V, V_O = 30V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 0.8V, I_{OL} = 100mA			0.4	V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V, V_I = 0.8V, I_{OL} = 300mA			0.7	V
I_{CCL}	Low-level supply current	V_{CC} = 5.5V, V_I = 0V			95	mA

⟨Output transistor⟩

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{(BR)CBO}$	Collector to base breakdown voltage	I_C = 100μA, I_E = 0mA	70			V
$V_{(BR)CER}$	Collector to emitter breakdown voltage	I_C = 100μA, R_{BE} = 500Ω	65			V
$V_{(BR)EBO}$	Emitter to base breakdown voltage	I_E = 100μA, I_C = 0mA	5			V
h_{FE}	Direct current amplification factor (Note 3)	V_{CE} = 3V, I_C = 100mA, T_a = 25℃	25			—
		V_{CE} = 3V, I_C = 300mA, T_a = 25℃	30			
		V_{CE} = 3V, I_C = 100mA, T_a = 0℃	20			
		V_{CE} = 3V, I_C = 300mA, T_a = 0℃	25			
V_{BE}	Base to emitter voltage	I_B = 10mA, I_C = 100mA			1	V
		I_B = 30mA, I_C = 300mA			1.2	
$V_{CE(sat)}$	Collector to emitter saturation voltage	I_B = 10mA, I_C = 100mA			0.4	V
		I_B = 30mA, I_C = 300mA			0.7	

Note 3 : Measurement should be done in a short time

PRECAUTIONS FOR USE (WHEN TTL GATE AND OUTPUT TRANSISTOR ARE CONNECTED)

The permissible amount of collector current of the output transistor I_O varies according to the conditions. Calculate it as follows, using Fig. 1 "Heat Dissipation Rate Characteristics", Fig. 2 "Pulse Power Chart", and the following formula.

$$P_d = \frac{V_{CC}}{M+N}(M \cdot I_{CCL} + N \cdot I_{CCH}) + M \cdot I_O \cdot V_{OL} \cdots\cdots(1)$$

Where P_d : Power dissipation

I_{CCL} : Supply current when all outputs of output transistors are "Low".

I_{CCH} : Supply current when all outputs of output transistors are "High".

V_{OL} : Output voltage when output is "Low".

M : The number of output transistors whose state is "Low".

N : The number of output transistors whose state is "High".

M+N : The total number of gates included in one package.

When trying to determine permissible amount of constant current, first, read the largest permissible power dissipation P_d for the given operating free-air ambient temperature range from Fig. 1. Then calculate I_O by substituting into Formula (1) the maximum values of I_{CCL}, I_{CCH} and V_{CC} as well as values M and N.

When calculating pulse current I_O, use Fig. 2. First, determine maximum permissible power dissipation P_d from the duty cycle and pulse width, then calculate using Formula (1). Be careful that I_O does not exceed the absolute maximum rating.

TYPICAL CHARACTERISTICS

Fig.1 "HEAT DISSIPATION RATE CHARACTERISTICS"

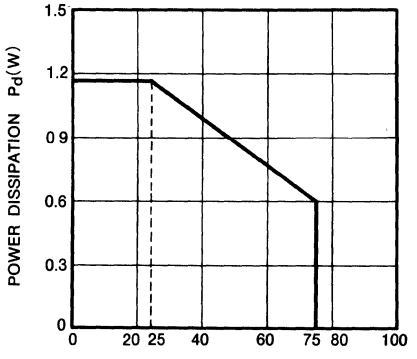
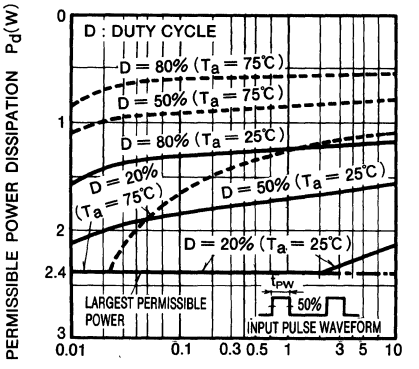


Fig.2 PULSE POWER CHART (CONTINUOUS PULSE)



MITSUBISHI ELECTRIC

SAFE RANGE OF OPERATION FOR THE OUTPUT TRANSISTOR (WHEN USED INDEPENDENTLY OF TTL GATE)

Both Fig. 3 and Fig. 4 show the safe operating ranges of output transistors when they are separate from and independent of the gates. Fig. 4 gives characteristics when t_{PW} = 20ms. When used for values other than 20ms determine the safe operating range using the method given below.

Calculate P_C using Formula (2). (P_C being the total of collector dissipation of all "ON" transistors)

$$P_C = P_d - \frac{V_{CC}}{M+N}(M \cdot I_{CCL} + N \cdot I_{CCH}) \cdots\cdots(2)$$

Where

P_d : Permissible power dissipation read from Fig. 1 or Fig. 2.

I_{CCL} : Supply current when gate output state is "Low".

I_{CCH} : Supply current when gate output state is "High".

(NOTE: The values of I_{CCL} and I_{CCH} will vary somewhat depending on the load connected to gate outputs.)

After using Formula (2) to calculate P_C, enter it into the following Formula (3) to find the safe operating range.

$$P_C = V_{CE} \cdot I_C \cdots\cdots(3)$$

However, the absolute maximum rating of $V_{CE} \leqq 30V$ and $I_C \leqq 600mA$ must be observed.

Note that Figs 3 and 4 express power consumption per package. Therefore, one transistor may consume all the power indicated in Fig. 3 and Fig. 4 if the other transistor and the gates are not used.

Fig.3 SAFE OPERATING RANGE OF OUTPUT TRANSISTOR (ONE SHOT PULSE)

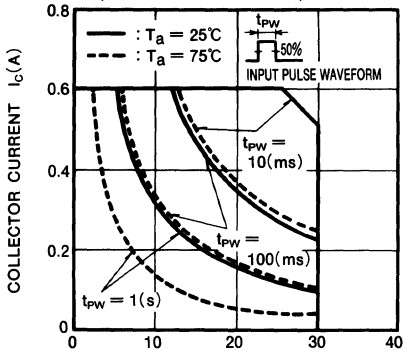
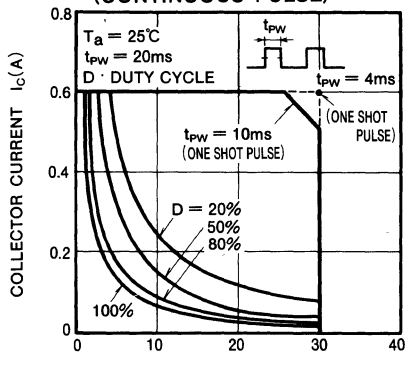


Fig.4 SAFE OPERATING RANGE OF OUTPUT TRANSISTOR (CONTINUOUS PULSE)



M54512L

4-UNIT 50mA TRANSISTOR ARRAY

DESCRIPTION

The M54512L, 4-channel sink driver, consists of four NPN transistors, and designed for use in medium-current switching applications.

FEATURES

- Output sustaining voltage to 20V
- 50mA output sink current capability
- Wide operating temperature range (T_a = −20∼+75℃)

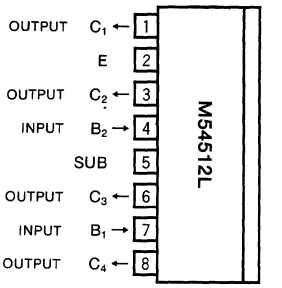
APPLICATION

LED or incandescent display driver

FUNCTION

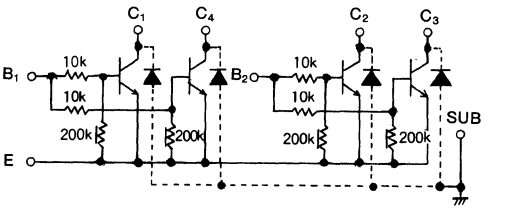
The M54512L is comprised of four NPN transistors with a 10kΩ series input resistor, connected to form dual 2-parallel output drivers. All emitters of transistors are connected together to pin 2. The substrate is connected to pin 5 and pin 5 must be tied to the most negative point in the external circuit. The drivers are capable of sinking 50mA and will withstand 20V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 8P5

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+20	V
V_{EBO}	Emitter-base sustaining voltage		4	V
I_C	Collector current	Transistor ON	50	mA
V_I	Input voltage		20	V
P_d	Power dissipation	T_a =75℃	500	mW
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_C	Output voltage		0		18	V
I_C	Collector current per channel		0		20	mA
V_{IH}	"H" Input voltage	I_C =30mA	11		18	V
V_{IL}	"L" Input voltage		0		0.2	V

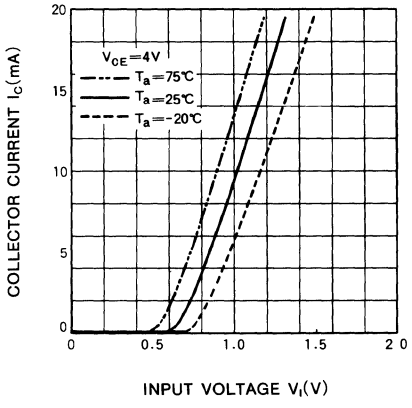
ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE} =20V				20	μA
$V_{CE(sat)}$	Output saturation voltage	I_B = 2 mA	I_C =10mA		0.02	0.1	V
			I_C =20mA		0.04	0.2	
BV_{EBO}	Emitter-base sustaining voltage	I_{EBO} =150 μA		4			V
V_I	Input voltage	I_B = 2 mA		4	11	18	V
h_{FE}	DC forward current gain	V_{CE} = 6 V, I_C =20mA, T_a=25℃		60	150		—

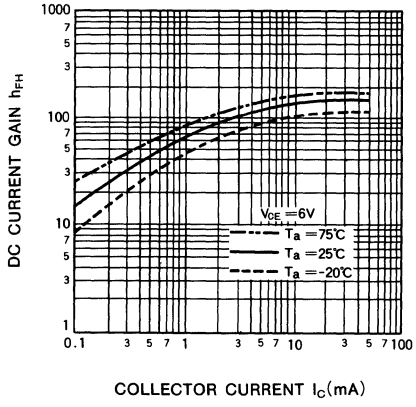
* : Typical values are at T_a = 25℃

TYPICAL CHARACTERISTICS

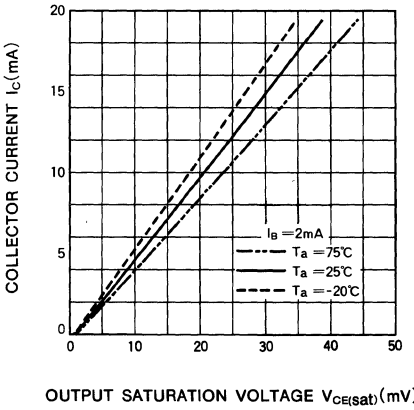
OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



OUTPUT CHARACTERISTICS



M54513P

8-UNIT 50mA TRANSISTOR ARRAY

DESCRIPTION

The M54513P, 8-channel sink drivers, consists of 8 NPN transistors with 2 kΩ series input resistors.

FEATURES

- High output sustaining voltage of 40V
- 50mA output sink current capability
- Wide operating temperature range (T_a = −20∼+75℃)

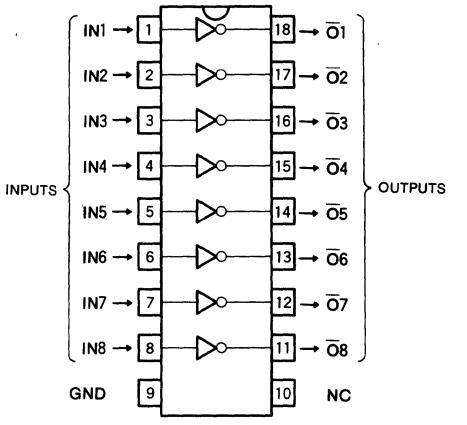
APPLICATION

LED or incandescent display digit driver

FUNCTION

The M54513P is comprised of eight NPN drivers. Each input has a voltage divider by 2kΩ and 13.6kΩ resistors. All emitters and the substrate are connected together to pin 9. The open collector outputs are capable of sinking 50mA and will withstand 40V in the OFF state.

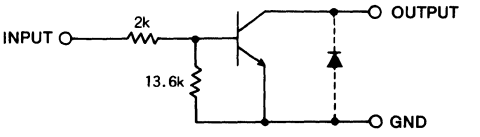
PIN CONFIGURATION (TOP VIEW)



Outline 18P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used. Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+40	V
I_C	Collector current	Transistor ON	50	mA
V_I	Input voltage		10	V
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		40	V
I_C	Collector current per channel		0		20	mA
V_{IH}	"H" Input voltage	I_C = 20 mA	2		8	V
V_{IL}	"L" Input voltage		0		0.2	V

MITSUBISHI ELECTRIC

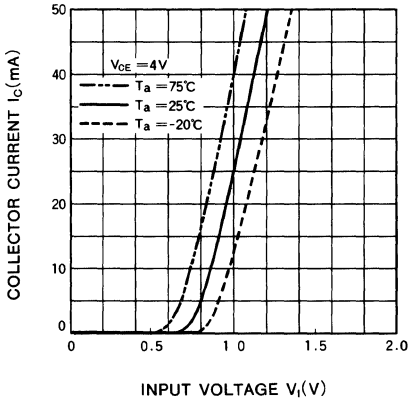
ELECTRICAL CHARACTERISTICS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE} =40V			50	μA
$V_{CE(sat)}$	Output saturation voltage	V_I =2V, I_C =12mA		30	100	mV
		V_I=2.5V, I_C =30mA		70	170	
I_I	Input current	V_I=2.5V		0.85	1.7	mA
h_{FE}	DC forward current gain	V_{CE} = 4 V, I_C =30mA, T_a =25℃	80	200		—

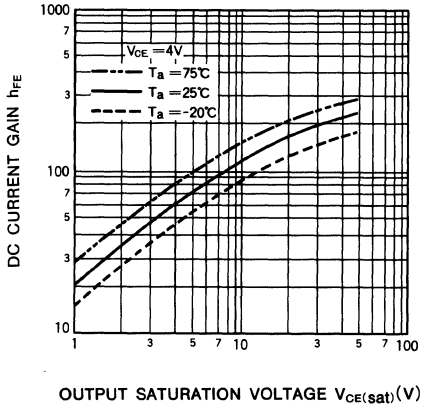
* : A typical value at T_a=25℃.

TYPICAL CHARACTERISTICS

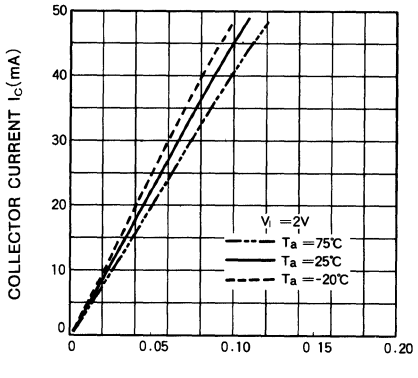
OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



OUTPUT CHARACTERISTICS



M54514AP

7-UNIT 50mA TRANSISTOR ARRAY

DESCRIPTION

The M54514AP, 7-channel sink drivers, consists of 7 NPN transistors with 2.8kΩ series input resistors.

FEATURES

- Output breakdown voltage to 20V
- 50mA output sink current capability
- Low output saturation voltage
- Wide operating temperature range (T_a =−20∼+75℃)

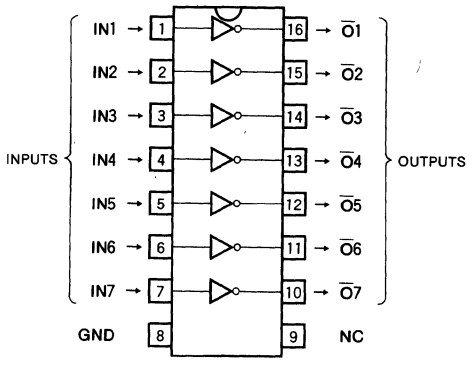
APPLICATION

LED or incandescent display digit driver

FUNCTION

The M54514AP is comprised of seven NPN drivers. Each input has a voltage divider by 2.8kΩ and 10kΩ resistors. All emitters and the substrate are connected together to pin 8. The open collector outputs are capable of sinking 50mA and will withstand 20V in the OFF state.

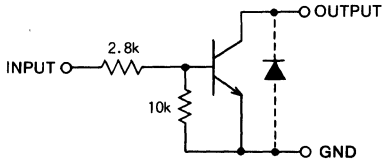
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a =−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+20	V
I_C	Collector current	Transistor ON	50	mA
V_I	Input voltage		10	V
P_d	Power dissipation	T_a=25℃	1.47	W
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a =−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		20	V
I_C	Collector current per channel		0		20	mA
V_{IH}	"H" Input voltage	I_C=50mA	2.4		8	V
V_{IL}	"L" Input voltage		0		0.2	V

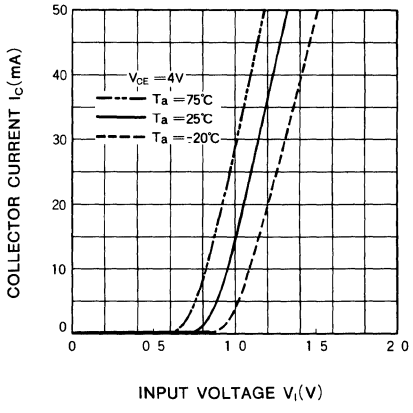
ELECTRICAL CHARACTERISTICS (T_a = −20～+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=20V				20	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=2.4V	I_C=20mA		0.04	0.17	V
			I_C=40mA		0.08	0.23	
I_I	Input current	V_I=2.4V			0.7	1.1	mA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=40mA, T_a=25℃		80	200		—

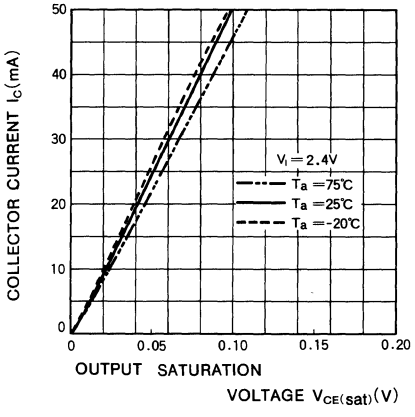
* : A typical value at T_a=25℃

TYPICAL CHARACTERISTICS

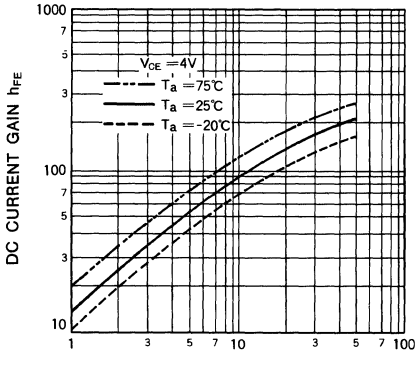
OUTPUT CURRENT CHARACTERISTICS



OUTPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54515P

7-UNIT 16mA TRANSISTOR ARRAY

DESCRIPTION

The M54515P, transistor array, consists of seven NPN transistors and is connected in a common-emitter configuration.

FEATURES

- Output breakdown voltage to 17V
- 16mA output sink current capability
- Wide operating temperature range (T_a = −20∼+75℃)

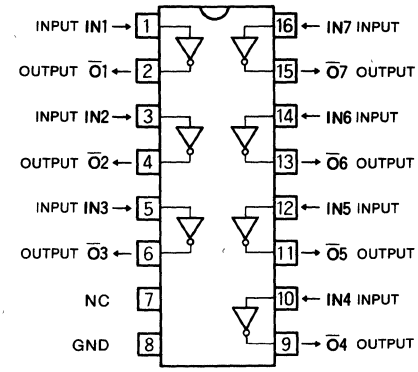
APPLICATION

LED or incandescent display driver

FUNCTION

The M54515P is comprised of seven NPN transistors. All emitters and the substrate are connected together to pin 8. The outputs are capable of sinking 16mA and will withstand 17V in the OFF state.

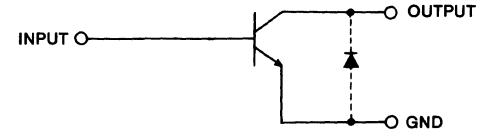
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+17	V
V_I	Input voltage		1.2	V
I_C	Collector current	Transistor ON	16	mA
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_O	Output voltage	0		17	V
I_C	Collector current per channel	0		16	mA

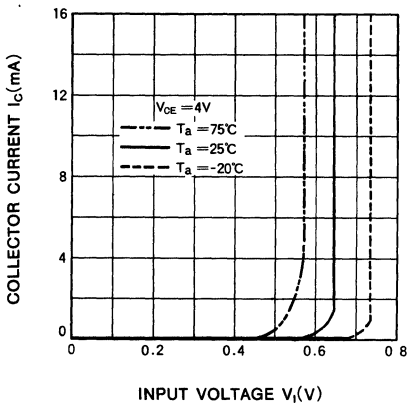
ELECTRICAL CHARACTERISTICS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{OH}=100μA	17			V
$V_{CE(sat)}$	Output saturation voltage	I_{OL}=16mA, I_B=0.5mA		0.14	0.5	V
$V_{BE(sat)}$	Base-emitter saturation voltage	I_{OL}=16mA, I_B=0.5mA		0.64	1.2	V
h_{FE}	DC forward current gain	V_{CE}=5V, I_C=16mA, T_a=25℃	32	50		—
$I_{O(leak)}$	Output leakage current	V_O=17V, V_I=0.2V			700	μA

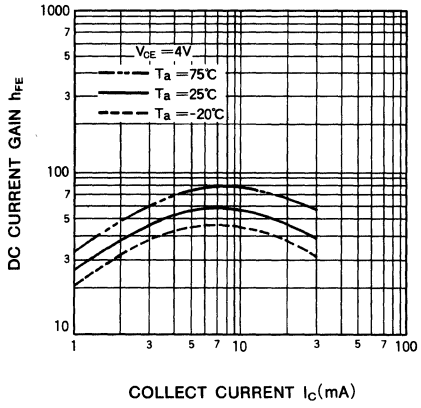
* A typical value at T_a = 25℃.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54516P

5-UNIT 500mA DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54516P, 5-channel sink driver, consists of 10 NPN transistors connected to form five high current gain driver pairs.

FEATURES

- Output sustaining voltage to 25 V
- High output sink current to 500mA
- PMOS Compatible input
- Wide operating temperature range (Ta = −20∼+75℃)

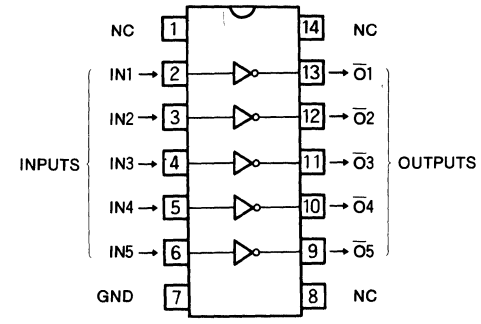
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics.

FUNCTION

The M54516P is comprised of five NPN darlington driver pairs with 20kΩ series input resistors. All emitter and the substrate are connected together to pin 7. The output are capable of sinking 500mA and will withstand 25V in the OFF state.

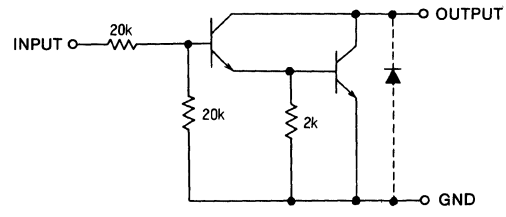
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+25	V
I_C	Collector current per channel	Transistor ON	500	mA
V_I	Input voltage		25	V
P_d	Power dissipation	Ta=25℃	1.47	W
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

5-UNIT 500mA DARLINGTON TRANSISTOR ARRAY

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		25	V
I_C	Collector current per channel	Percent duty cycle less than 10%	0		400	mA
		Percent duty cycle less than 55%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	8		20	V
		I_C=200mA	5		20	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.5	V

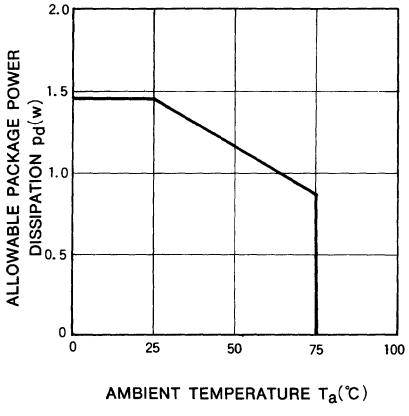
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	25			V
$V_{CE(sat)}$	Output saturation voltage	V_I=8V, I_C=400mA		1.15	2.2	V
		V_I=5V, I_C=200mA		0.95	1.4	
I_I	Input current	V_I=17V	0.3	0.8	1.8	mA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=400mA, T_a=25℃	1000	4000		—

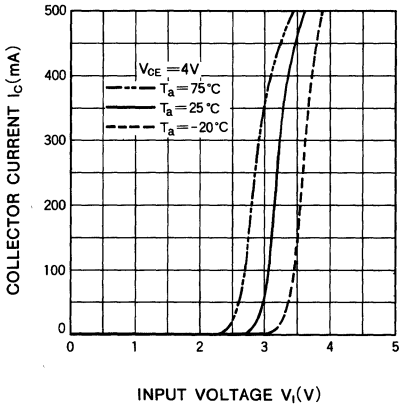
* : A typical value at T_a=25℃.

TYPICAL CHARACTERISTICS

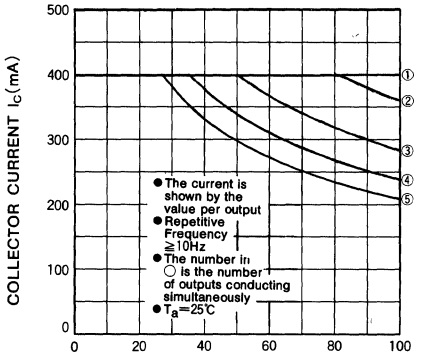
ALLOWABLE AVERAGE POWER DISSIPATION



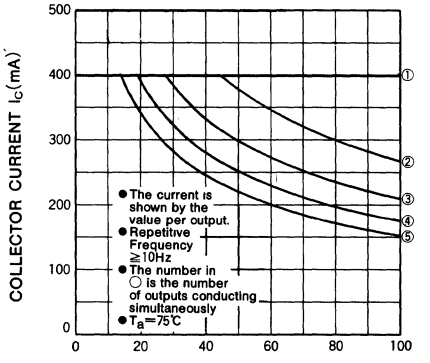
OUTPUT CURRENT CHARACTERISTICS



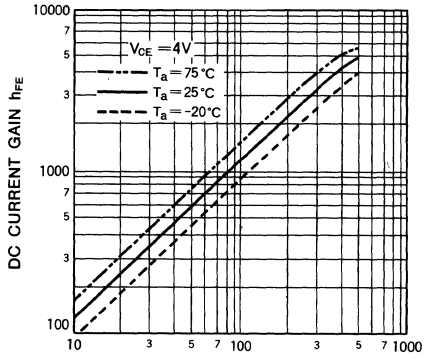
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54517P

7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54517P, 7-channel sink driver, consists of 14 NPN transistors connected to form seven high current gain driver pairs.

FEATURES

- Output sustaining voltage to 25V
- High output sink current to 400mA
- PMOS Compatible input
- Wide operating temperature range (T_a = −20~+75℃)

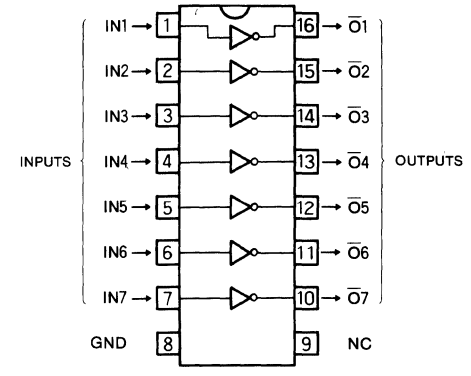
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

The M54517P is comprised of seven NPN darlington driver pairs with 20kΩ series input resistors. All emitters and the substrate are connected to pin 8. The output are capable of sinking 400mA and will withstand 25V in the OFF state.

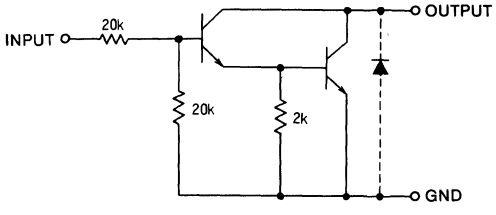
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5~+25	V
I_C	Collector current per channel	Transistor ON	400	mA
V_I	Input voltage		25	V
P_d	Power dissipation	T_a=25℃	1.47	W
T_{opr}	Operating temperature		−20~+75	℃
T_{stg}	Storage temperature		−55~+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		25	V
I_C	Collector current per channel	Percent duty cycle less than 8%	0		400	mA
		Percent duty cycle less than 40%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	8		20	V
		I_C=100mA	5		20	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.5	V

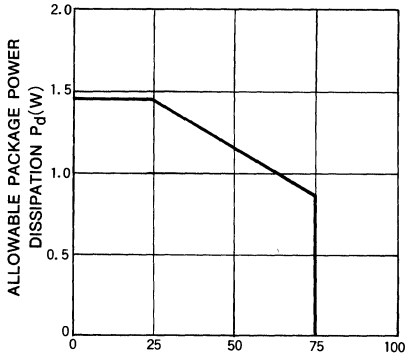
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	25			V
$V_{CE(sat)}$	Output saturation voltage	V_i=8V, I_C=400mA		1.15	2.2	V
		V_i=5V, I_C=200mA		0.95	1.4	
I_I	Input current	V_i=17V	0.3	0.8	1.8	mA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=400mA, T_a=25℃	1000	4500		—

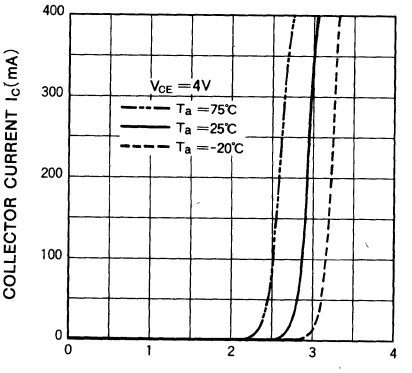
* : A typical value at T_a=25℃.

TYPICAL CHARACTERISTICS

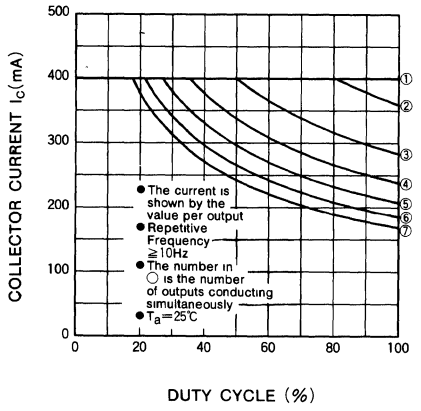
ALLOWABLE AVERAGE POWER DISSIPATION



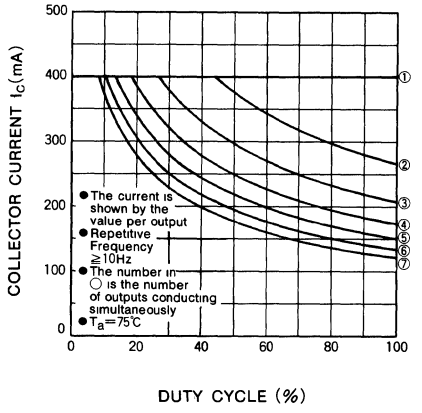
OUTPUT CURRENT CHARACTERISTICS



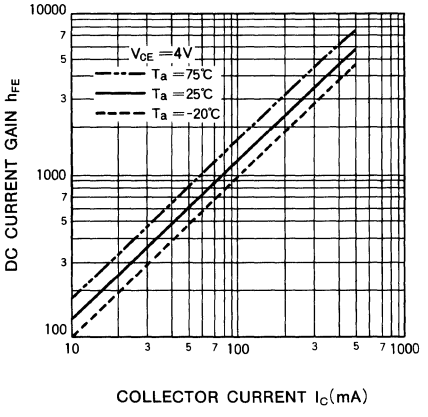
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



M54519P

7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54519P, 7-channel sink driver, consists of 14 NPN transistors connected to form seven high current gain driver pairs.

FEATURES

- High output sustaining voltage to 40V
- High output sink current to 400mA
- PMOS Compatible input
- Wide operating temperature range (T_a=−20∼+75℃)

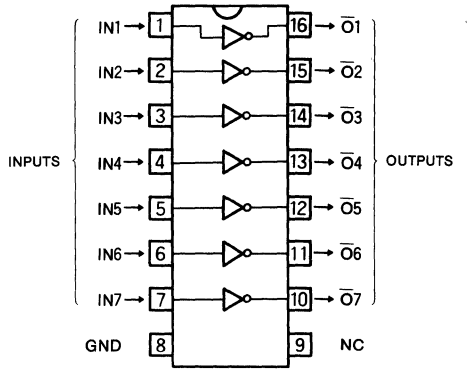
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

The M54519P is comprised of seven NPN darlington driver pairs with 20kΩ series input resistors.
All emitters and the substrate are connected together to pin 8. The output are capable of sinking 400mA and will withstand 40V in the OFF state.

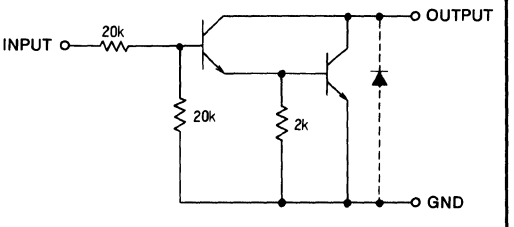
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+40	V
I_C	Collector current per channel	Transistor ON	400	mA
V_I	Input voltage		−0.5∼+40	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter *		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		40	V
I_C	Collector current per channel	Percent duty cycle less than 8%	0		400	mA
		Percent duty cycle less than 30%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	8		30	V
		I_C=100mA	5		30	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.5	V

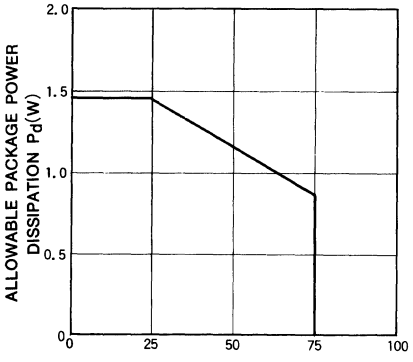
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	40			V
$V_{CE(sat)}$	Output saturation voltage	V_I=8V, I_C=400mA		1.2	2.4	V
		V_I=5V, I_C=200mA		0.9	1.6	
I_I	Input current	V_I=17V	0.3	0.8	1.8	mA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=400mA, T_a=25℃	1000	6000		—

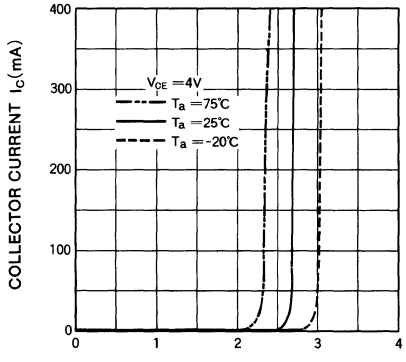
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

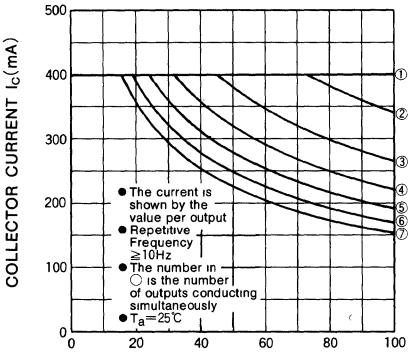
ALLOWABLE AVERAGE POWER DISSIPATION



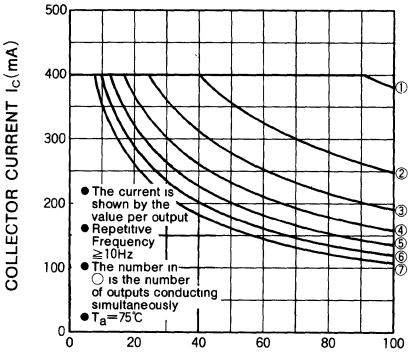
OUTPUT CURRENT CHARACTERISTICS



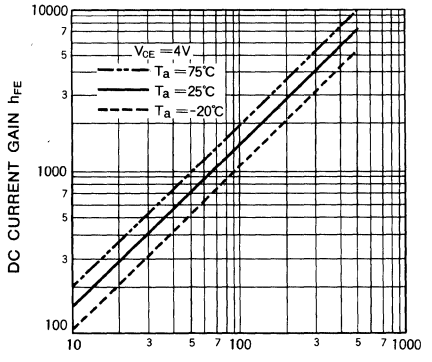
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54521P

5-UNIT 500mA DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54521P, 5-channel sink driver, consists of 10 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output sustaining voltage to 30V
- High output sink current to 500mA
- Wide operating temperature range (Ta = −20～+75℃)

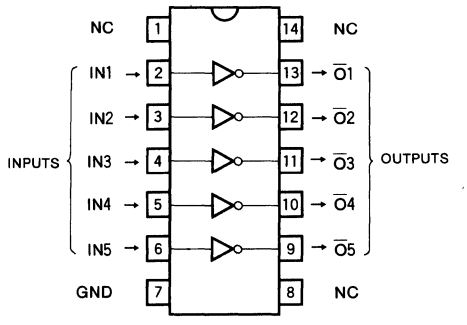
APPLICATION

Relay and printer drivers, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

The M54521P is comprised of five NPN darlington driver pairs. All emitters and the substrate are connected together to pin 7 . The output are capable of sinking 500mA and will withstand 30V in the OFF state.

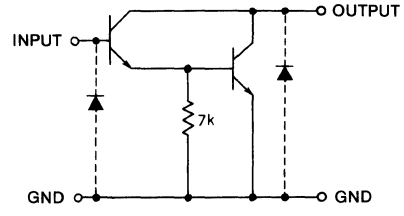
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (Ta=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5～+30	V
I_C	Collector current per channel	Transistor ON	500	mA
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		30	V
I_C	Collector current per channel	Percent duty cycle less than 10%	0		400	mA
		Percent duty cycle less than 55%	0		200	
I_{IH}	"H" Input current	I_C=200mA	1		5	mA
		I_C=400mA	2		5	
I_{IL}	"L" Input current			0	10	μA

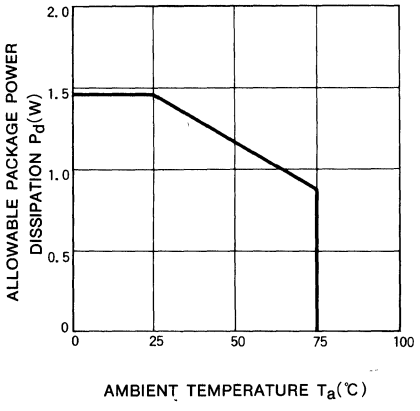
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	30			V
$V_{CE(sat)}$	Output saturation voltage	V_I=2mA, I_C=400mA		1.0	2.4	V
		V_I=1mA, I_C=200mA		0.8	1.6	
V_I	Input voltage	I_I=1mA	0.6	1.35	1.7	V

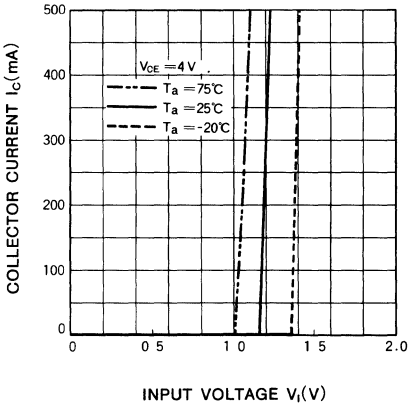
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

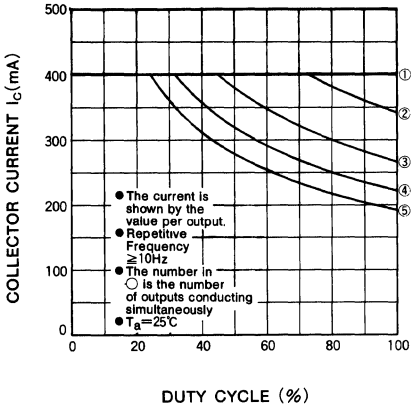


OUTPUT CURRENT CHARACTERISTICS

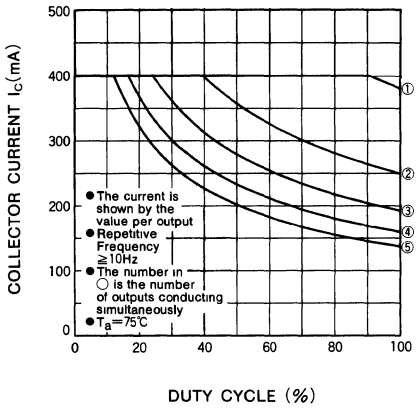


MITSUBISHI ELECTRIC

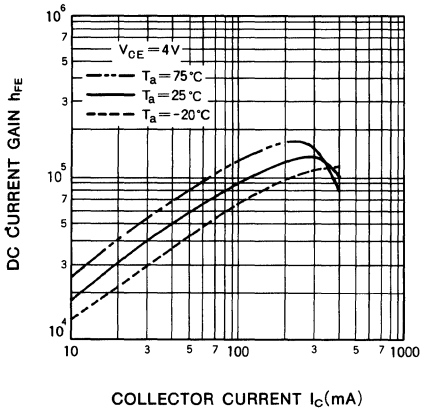
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



M54522P

8-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54522P, 8-channel sink driver, consists of 16 NPN transistors connected to form eight high current gain driver pairs.

FEATURES

- High output sustaining voltage to 40V
- High output sink current to 400mA
- Integral diodes for transient suppression
- PMOS Compatible input
- Wide operating temperature range (T_a = −20∼+75℃)

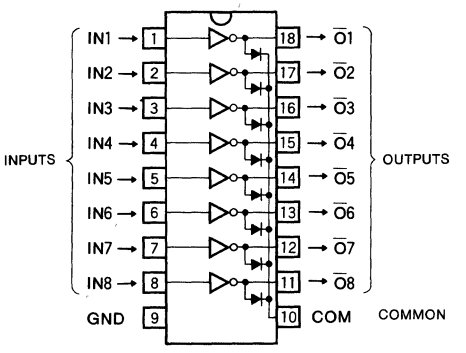
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing between MOS/BIPOLAR logics and high power loads

FUNCTION

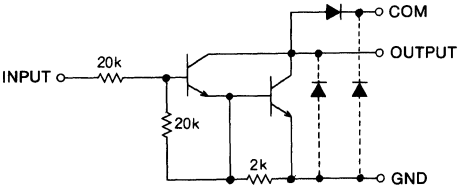
The M54522P is comprised of eight NPN darlington driver pairs with 20kΩ series input resistors. Each output has an integral diode for inductive load transient suppression. The cathodes of the diodes are connected together to pin 10. All emitters and the substrate are connected to pin 9 . The output are capable of sinking 400mA and will withstand 40V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+40	V
I_C	Collector current per channel	Transistor ON	400	mA
V_I	Input voltage		−0.5∼+40	V
I_F	Clamp diode forward current		400	mA
V_R	Clamp diode reverse voltage		−0.5∼+40	V
Pd	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

8-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		40	V
I_C	Collector current per channel	Percent duty cycle less than 7%	0		400	mA
		Percent duty cycle less than 30%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	8		30	V
		I_C=200mA	4		30	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.5	V

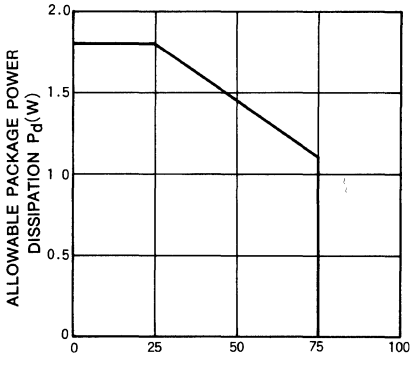
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	40			V
$V_{CE(sat)}$	Output saturation voltage	V_I=8V, I_C=400mA		1.15	2.4	V
		V_I=4V, I_C=200mA		0.94	1.6	
I_I	Input current	V_I=17V	0.3	0.9	1.8	mA
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
V_R	Clamp diode reverse voltage	I_R=100μA	40			V
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=300mA, T_a=25℃	1000	8000		—

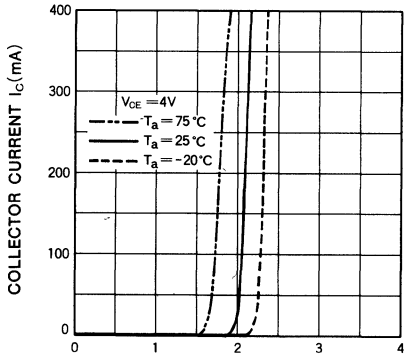
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

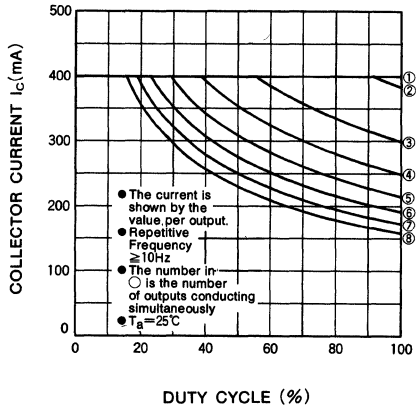


OUTPUT CURRENT CHARACTERISTICS

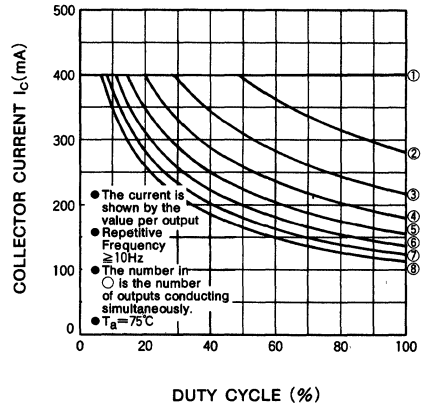


8-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

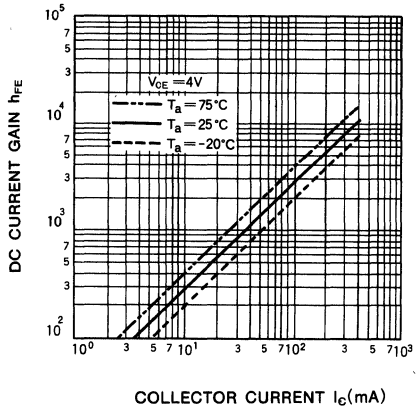
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54523P

7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54523P, 7-channel sink driver, consists of 14 NPN transistors connected to form seven high current gain driver pairs.

FEATURES

- High output sustaining voltage to 50V
- High output sink current to 500mA
- Integral diodes for transient suppression
- PMOS Compatible input
- Wide operating temperature range (T_a = −20～+75℃)

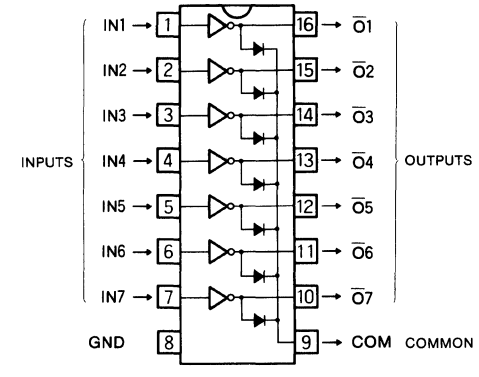
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics.

FUNCTION

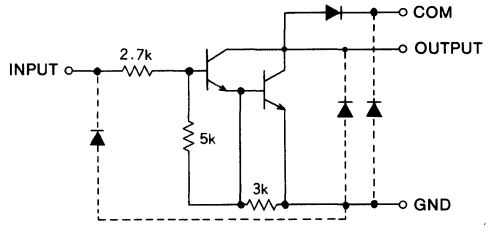
The M54523P is comprised of seven NPN darlington driver pairs with 2.7kΩ series input resistors. Between pin 9 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 8. The outputs are capable of sinking 500mA and will withstand 50V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5～+50	V
I_C	Collector current per channel	Transistor ON	500	mA
V_I	Input voltage		−0.5～+30	V
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		−0.5～+50	V
Pd	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		50	V
I_C	Collector current per channel	Percent duty cycle less than 8%	0		400	mA
		Percent duty cycle less than 30%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	3.85		25	V
		I_C=100mA	3.4		25	
V_{IL}	"L" Input voltage		0		0.6	V

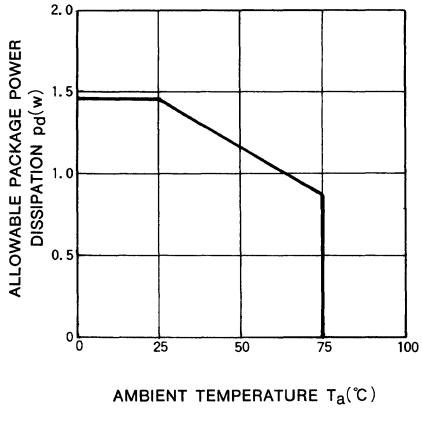
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=50V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=3.85V, I_C=400mA		1.3	2.4	V
		V_I=3.85V, I_C=200mA		0.95	1.6	
I_I	Input current	V_I=3.85V		0.95	1.8	mA
		V_I=25V		9	18	
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
I_R	Clamp diode leakage voltage	V_R=50V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=350mA, T_a=25℃	1000	2500		—

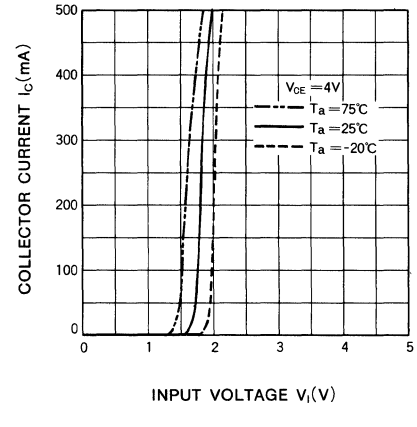
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

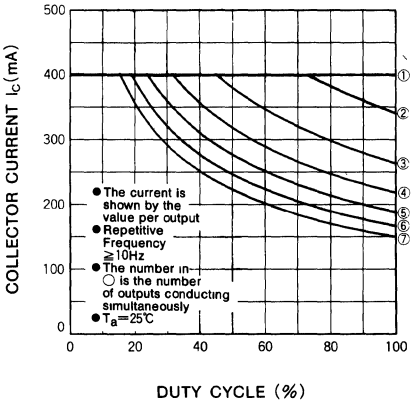


OUTPUT CURRENT CHARACTERISTICS

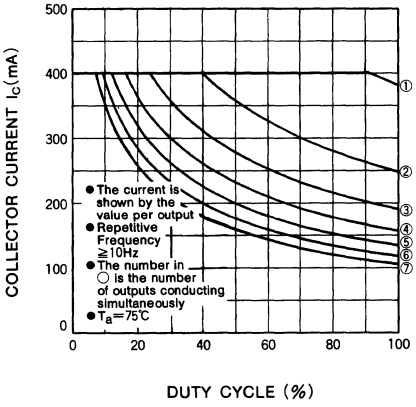


7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

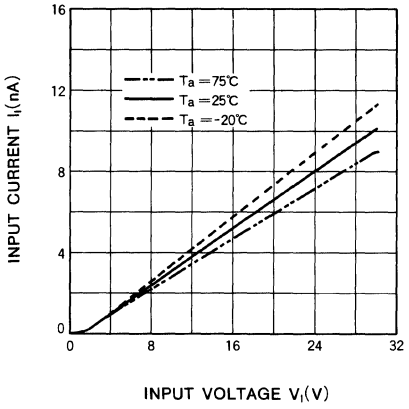
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



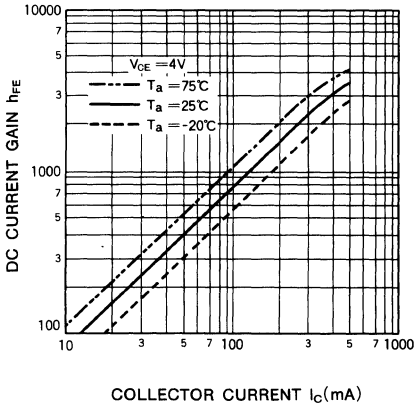
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54524P

7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54524P, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 50V
- High output sink current to 500mA
- Integral diodes for transient suppression
- Wide operating temperature range (T_a = −20~+75℃)

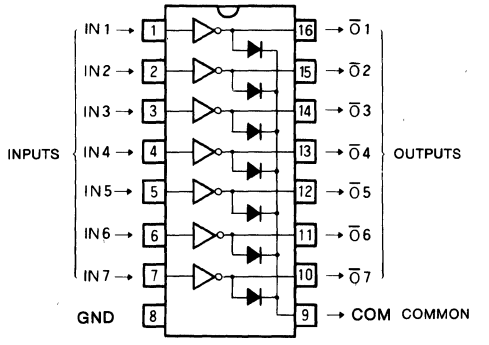
APPLICATION

Relay and printer drivers, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

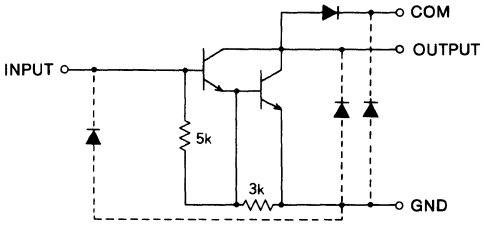
The M54524P is comprised of seven NPN darlington driver pairs. Between pin 9 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 8. The outputs are capable of sinking 500mA and will withstand 50V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5~+50	V
I_C	Collector current per channel	Transistor ON	500	mA
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		−0.5~+50	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20~+75	℃
Tstg	Storage temperature		−55~+125	℃

MITSUBISHI ELECTRIC

7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		50	V
I_C	Collector current per channel	Percent duty cycle less than 8%	0		400	mA
		Percent duty cycle less than 30%	0		200	
I_{IH}	"H" Input current	I_C=400mA	1		20	mA
I_{IL}	"L" Input current		0		20	μA

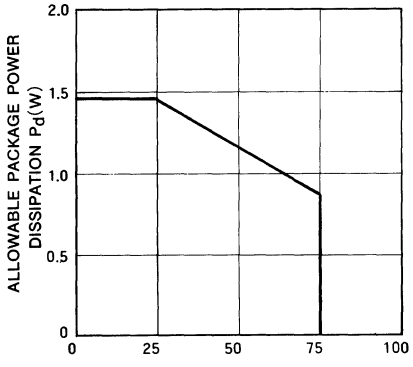
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=50V			100	μA
$V_{CE(sat)}$	Output saturation voltage	I_I=1mA, I_C=400mA		1.3	2.4	V
		I_I=1mA, I_C=200mA		0.95	1.6	
V_I	Input voltage	I_I=1mA		1.35	1.7	V
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
I_R	Clamp diode leakage current	V_R=50V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=350mA, T_a=25℃	1000	2500		—

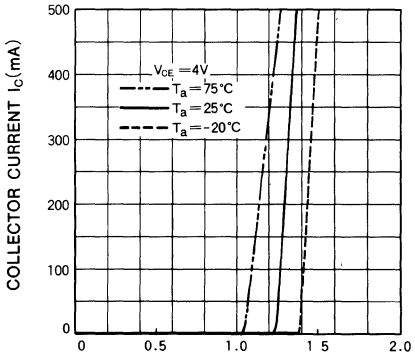
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

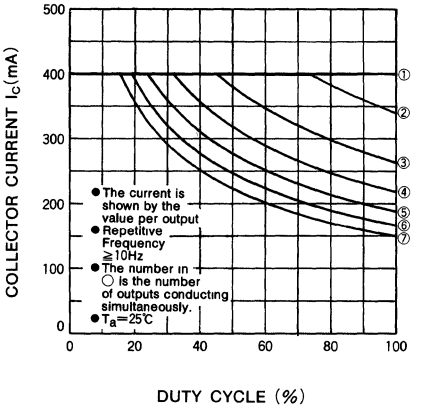


OUTPUT CURRENT CHARACTERISTICS

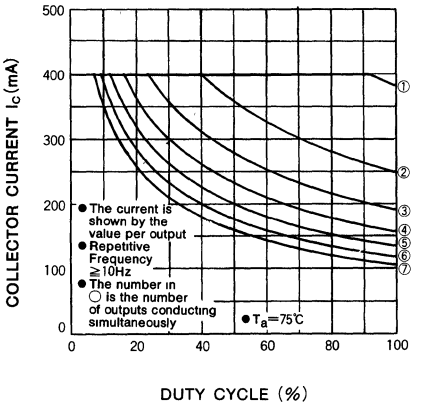


7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

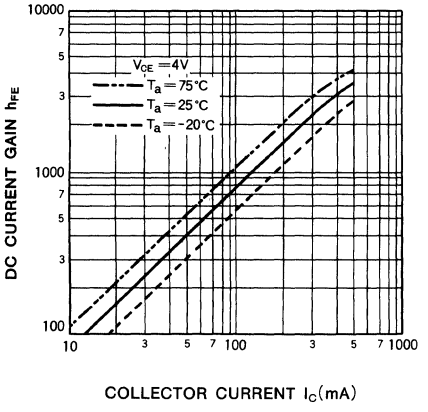
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54525P

7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54525P, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 50V
- High output sink current to 500mA
- Integral diodes for transient suppression
- 24V PMOS compatible input
- Wide operating temperature range (T_a = −20∼+75℃)

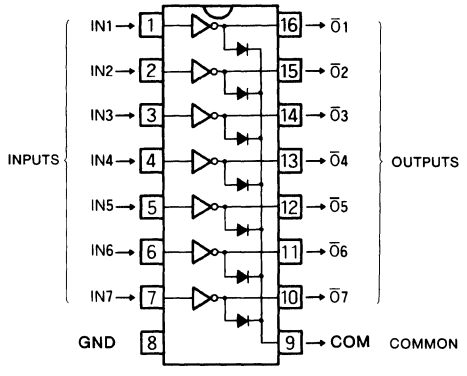
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

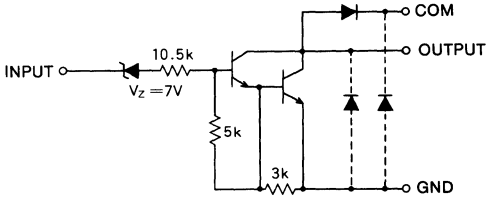
The M54525P is comprised of seven NPN darlington driver pairs. Each input has a Zener diode and 10.5kΩ resistor in series to limit the input current. Between pin 9 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 8 . The outputs are capable of sinking 500mA and will withstand 50V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+50	V
I_C	Collector current per channel	Transistor ON	500	mA
V_I	Input voltage		−0.5∼+30	V
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		−0.5∼+50	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		50	V
I_C	Collector current per channel	Percent duty cycle less than 8%	0		400	mA
		Percent duty cycle less than 30%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	17		25	V
V_{IL}	"L" Input voltage		0		6	V

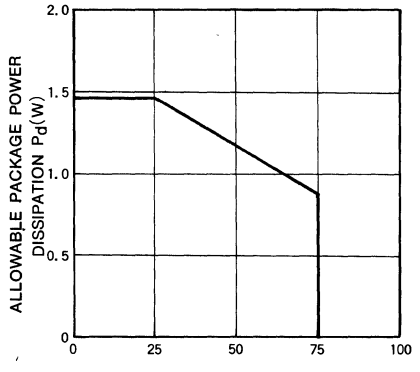
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Input leakage current	V_{CE}=50V	I_I=0mA			100	μA
			V_I=6V			500	
$V_{CE(sat)}$	Output saturation voltage	V_I=17V, I_C=400mA			1.3	2.4	V
		V_I=17V, I_C=200mA			0.95	1.6	
I_I	Input current	V_I=17V			0.85	1.8	mA
		V_I=25V			1.6	3.2	
V_F	Clamp diode forward voltage	I_F=400mA			1.5	2.4	V
I_R	Clamp diode leakage current	V_R=50V				100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=350mA, T_a=25℃		1000	2500		—

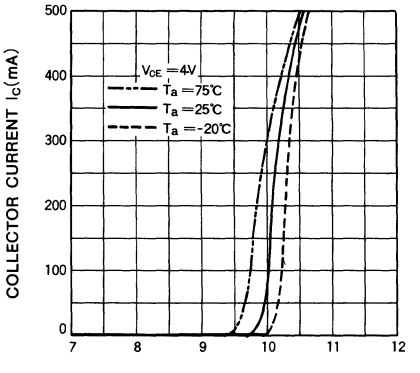
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

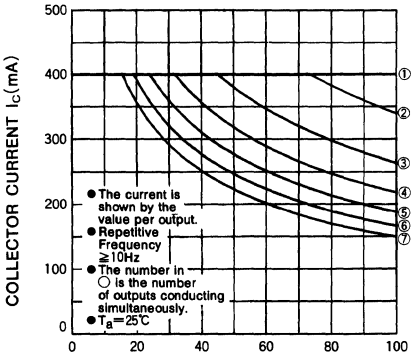


OUTPUT CURRENT CHARACTERISTICS

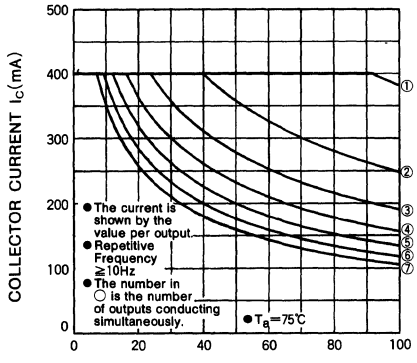


7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

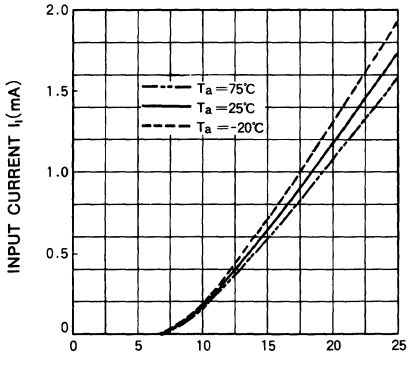
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



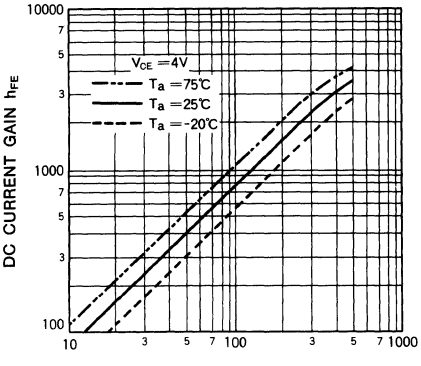
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54526P

7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54526P, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 50V
- High output sink current to 500mA
- Integral diodes for transient suppression
- PMOS compatible input
- Wide operating temperature range (T_a = −20∼+75℃)

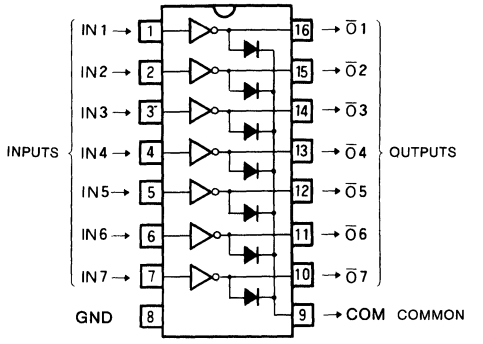
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

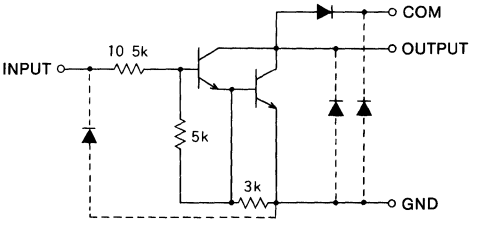
The M54526P is comprised of seven darlington driver pairs with 10.5kΩ series input resistors. Between pin 9 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 8 . The outputs are capable of sinking 500mA and will withstand 50V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be vsed

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+50	V
I_C	Collector current per channel	Transistor ON	500	mA
V_I	Input voltage		−0.5∼+30	V
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		−0.5∼+50	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		50	V
I_C	Collector current per channel	Percent duty cycle less than 8%	0		400	mA
		Percent duty cycle less than 30%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	8	10	25	V
V_{IL}	"L" Input voltage		0		0.5	V

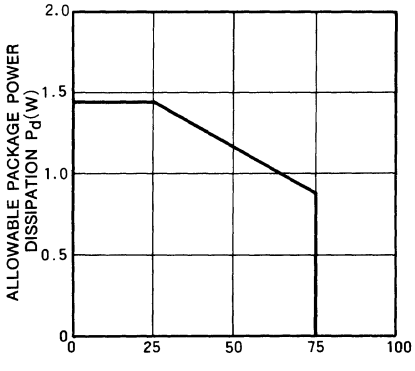
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=50V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=8V, I_C=400mA		1.3	2.4	V
		V_I=8V, I_C=200mA		0.95	1.6	
I_I	Input current	V_I=10V		0.9	1.5	mA
		V_I=25V		2.8	4.1	
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
I_R	Clamp diode leakage current	V_R=50V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=350mA, T_a=25℃	1000	2500		—

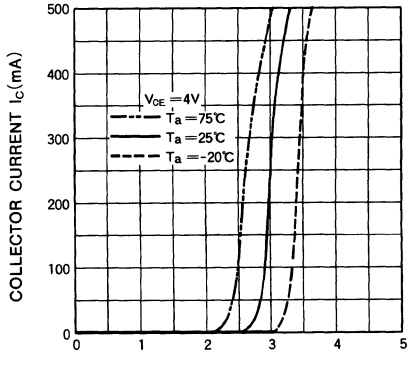
* : Typical values are at T_a = 25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

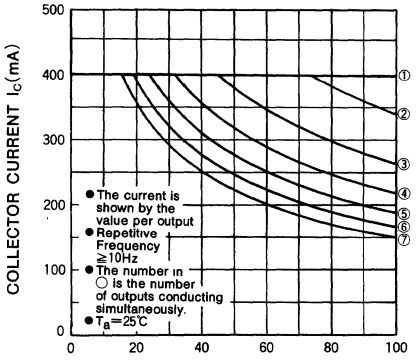


OUTPUT CURRENT CHARACTERISTICS

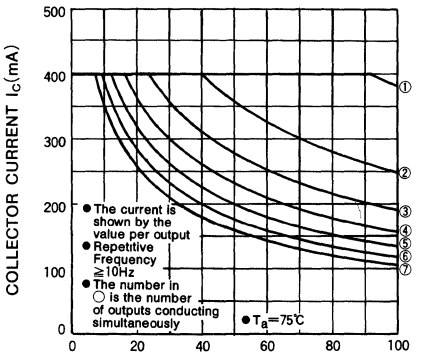


7-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

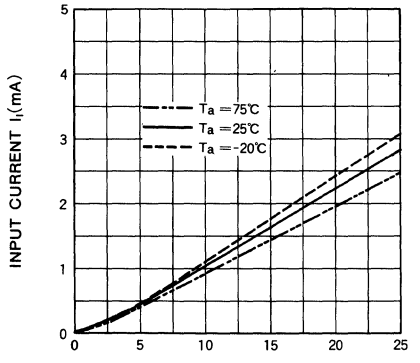
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



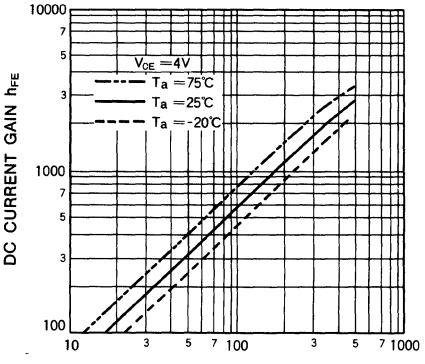
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54527P

6-UNIT 150mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54527P, 6-channel sink driver, consists of 12 NPN transistors connected to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 40V
- Output sink current to 150mA
- PMOS compatible input
- Integral diode for transient suppression
- Wide input voltage range from −40V to +40V
- Wide operating temperature range (T_a = −20~+75℃)

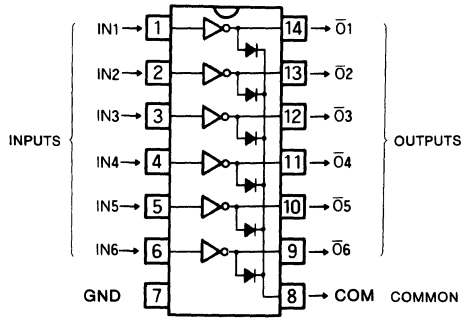
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

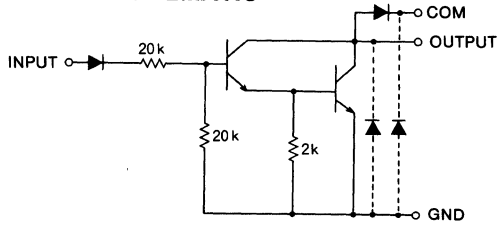
The M54527P is comprised of six darlington driver pairs. Each input has a diode and 20kΩ resistor in series to allow a negative voltage input. Between pin 8 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 7 . The outputs are capable of sinking 150mA and will withstand 40V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be vsed.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5~+40	V
I_C	Collector current per channel	Transistor ON	150	mA
V_I	Input voltage		−40~+40	V
$I_{F(D)}$	Clamp diode forward current		150	mA
$V_{R(D)}$	Clamp diode reverse voltage		−0.5~+40	V
Pd	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20~+75	℃
Tstg	Storage temperature		−55~+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		40	V
I_C	Collector current per channel	Percent duty cycle less than 50%	0		150	mA
V_{IH}	"H" Input voltage	I_C=150mA	7		35	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		1	V

6-UNIT 150mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

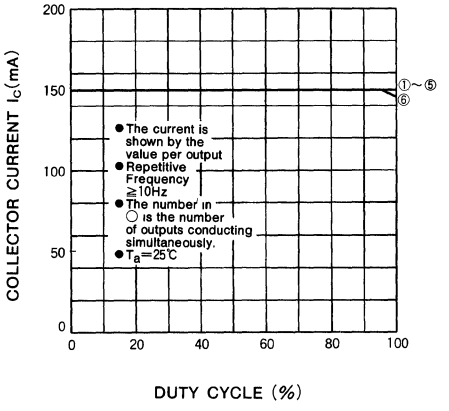
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	40			V
$V_{CE(sat)}$	Output saturation voltage	V_I=7V, I_C=150mA		1.4	1.7	V
		V_I=7V, I_C=100mA		1.2	1.4	
I_I	Input current	V_I=18V		0.9	1.8	mA
		V_I=35V		1.9	5	
I_R	Input leakage current	V_I=−35V			−20	μA
$V_{F(D)}$	Clamp diode forward voltage	$I_{F(D)}$=150mA		1.15	1.6	V
$I_{R(D)}$	Clamp diode leakage current	$V_{R(D)}$=40V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=150mA, T_a=25℃	800	2500		—

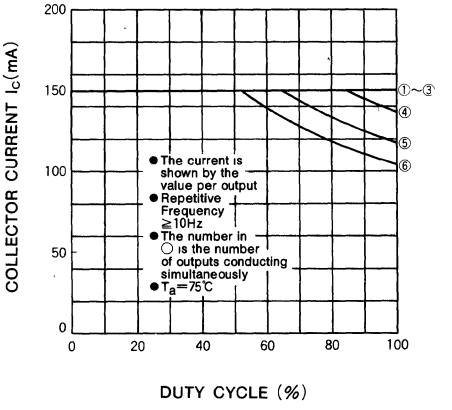
* : Typical values are at T_a = 25℃.

TYPICAL CHARACTERISTICS

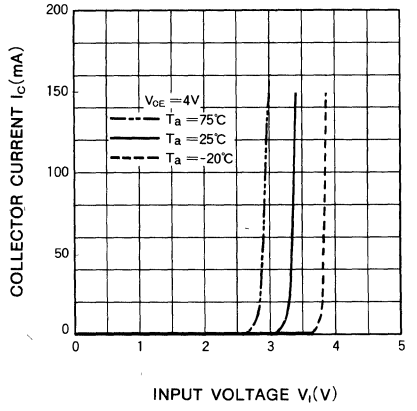
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



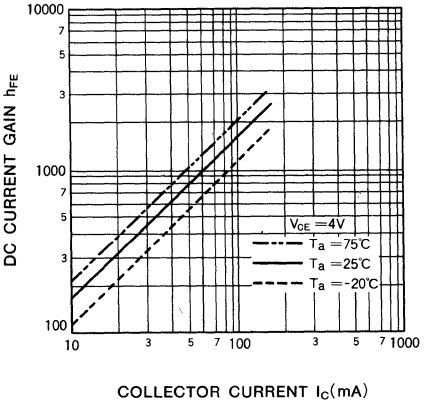
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



MITSUBISHI ELECTRIC

M54528P

7-UNIT 150mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54528P, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 40V
- Output sink current to 150mA
- Efficient I/O pin layout
- PMOS compatible input
- Integral diodes for transient suppression
- Wide input voltage range from −40V to +40V
- Wide operating temperature range (T_a = −20~+75℃)

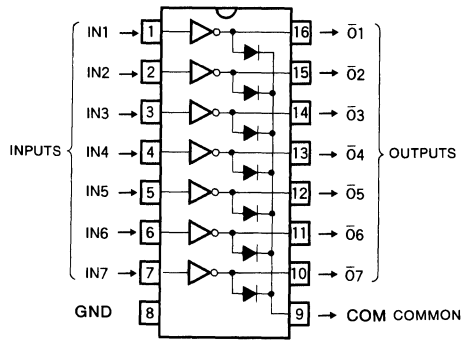
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

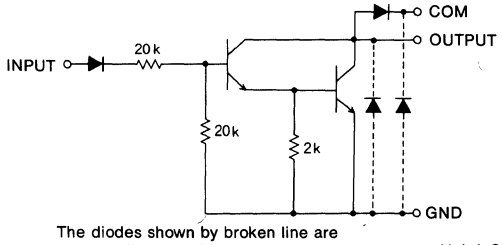
The M54528P is comprised of seven darlington driver pairs. Each input has a diode and 20kΩ resistor in series to allow a negative voltage input. Between pin 9 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 8 . The outputs are capable of sinking 150mA and will withstand 40V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be vsed.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5~+40	V
I_C	Collector current per channel	Transistor ON	150	mA
V_I	Input voltage		−40~+40	V
I_F	Clamp diode forward current		150	mA
V_R	Clamp diode reverse voltage		−0.5~+40	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20~+75	℃
Tstg	Storage temperature		−55~+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		40	V
I_C	Collector current per channel	Percent duty cycle less than 40%	0		150	mA
V_{IH}	"H" Input voltage	I_C=150mA	7		35	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		1	V

7-UNIT 150mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

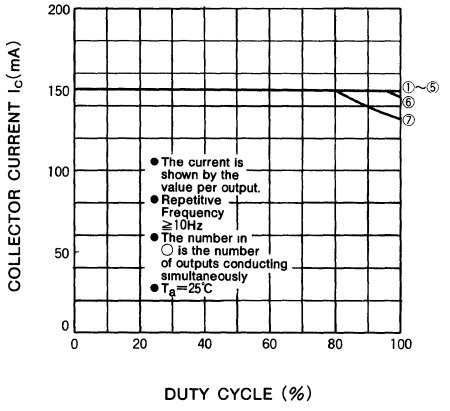
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	40			V
$V_{CE(sat)}$	Output saturation voltage	V_I=7V, I_C=150mA		1.4	1.7	V
		V_I=7V, I_C=100mA		1.2	1.4	
I_I	Input current	V_I=18V		0.9	1.8	mA
		V_I=35V		1.9	5	
I_R	Input leakage current	V_I=−35V			−20	μA
$V_{F(D)}$	Clamp diode forward voltage	$I_{F(D)}$=150mA		1.15	1.6	V
$I_{R(D)}$	Clamp diode leakage current	$V_{R(D)}$=40V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=150mA, T_a=25℃	800	2500		—

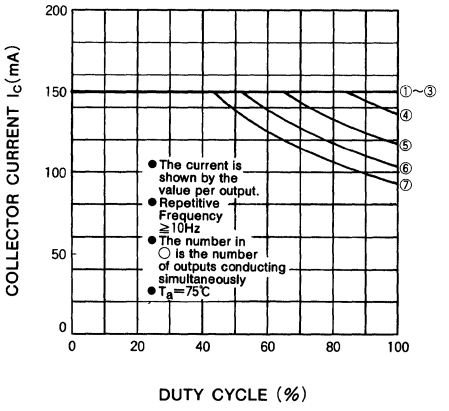
* : Typical values are at T_a = 25℃.

TYPICAL CHARACTERISTICS

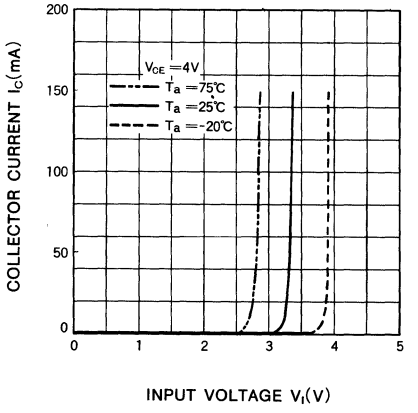
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



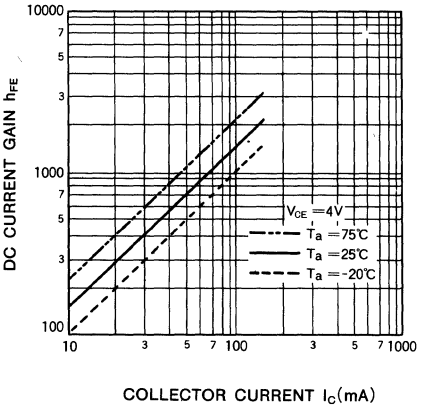
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



MITSUBISHI ELECTRIC

M54529P

5-UNIT 320mA TRANSISTOR ARRAY WITH STROBE

DESCRIPTION

The M54529P, 5-channel sink driver, consists of 10 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output sustaining voltage to 20V
- High output sink current to 320mA
- PMOS Compatible input with strobe control
- Wide operating temperature range (T_a=−20∼+75℃)

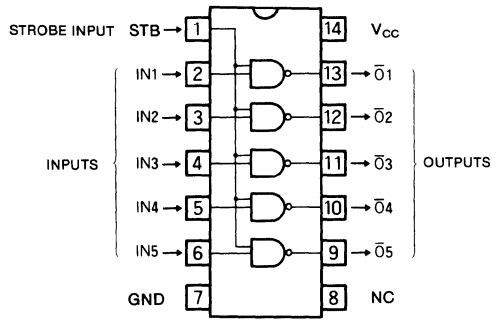
APPLICATION

Relay and printer driver, LED and incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

The M54529P uses a predriver stage. Each input has a diode and 20kΩ resistor in series to have a wide input voltage range from −25V to +20V. All input can be controlled simultaneously by a strobe input at pin 1 . The power supply of the predrivers is connected to pin 14. All emitters and the substrate are connected together to pin 7 . The outputs are capable of sinking 320mA and will withstand 20V in the OFF state.

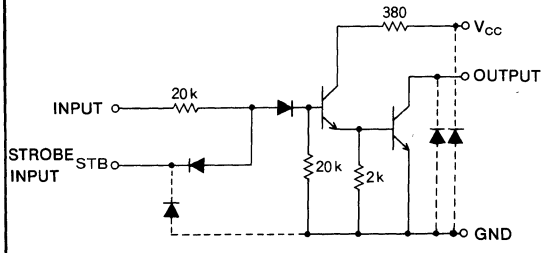
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be vsed

Unit : Ω

FUNCTIONAL TABLE

IN	STB	OUT
L	L	H
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+20	V
I_C	Collector current per channel	Transistor ON	320	mA
V_I	Input voltage		−25∼+20	V
$V_{I(STB)}$	Strobe input voltage		−0.5∼+20	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3		8	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	Percent duty cycle less than 33%, V_{CC}=6.5V	0		300	mA
		Percent duty cycle less than 80%, V_{CC}=6.5V	0		150	
V_{IH}	"H" Input voltage	I_C=300mA	7		15	V
		I_C=150mA	6		15	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		1	V
$V_{IH(STB)}$	"H" Input voltage (strobe input)		2.4		15	V
$V_{IL(STB)}$	"L" Input voltage (strobe input)		0		0.2	V

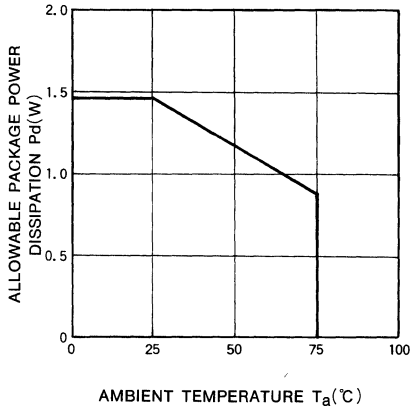
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	V_{CC}=8V, V_I=7V, $V_{I(STB)}$=0.2V I_{CEO}=100μA		20			V
$V_{CE(sat)}$	Output saturation voltage	V_I=7V	V_{CC}=6.5V, I_C=250mA		0.5	0.85	V
		$V_{I(STB)}$=2.4V	V_{CC}=3V, I_C=120mA		0.3	0.5	
I_I	Input current	V_{CC}=8V, V_I=18V, $V_{I(STB)}$=2.4V			0.9	1.8	mA
I_R	Input leakage current	V_{CC}=8V, V_I=−25V			0	−20	μA
$I_{I(STB)}$	Strobe input current	V_{CC}=8V, V_I=7V all input $V_{I(STB)}$=0.2V			−4		mA
$I_{R(STB)}$	Strobe input leakage current	V_{CC}=8V, V_I=0V, $V_{I(STB)}$=20V			0	10	μA
I_{CC}	Supply current	V_{CC}=8V, V_I=7V all input $V_{I(STB)}$=2.4V			95	170	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=6.5V, I_C=300mA, T_a=25℃ $V_{IH(STB)}$=2.4V		1000	3000		—

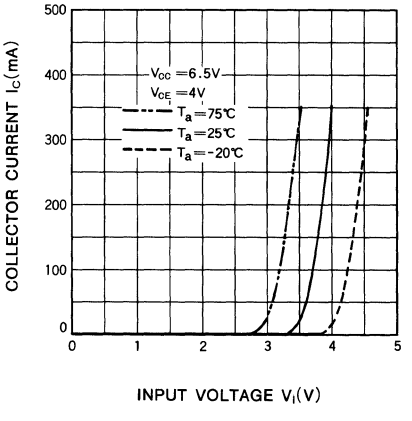
* : Typical values are at T_a = 25℃.

TYPICAL CHARACTERISTICS

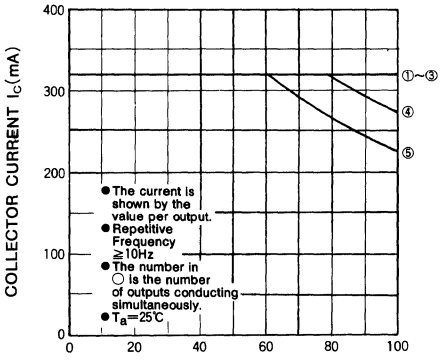
ALLOWABLE AVERAGE POWER DISSIPATION



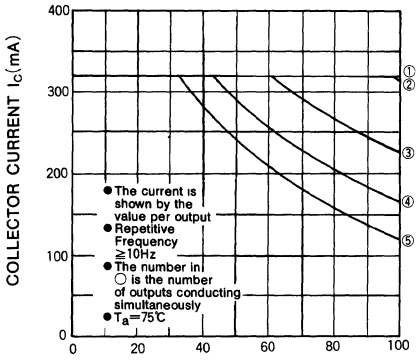
OUTPUT CURRENT CHARACTERISTICS



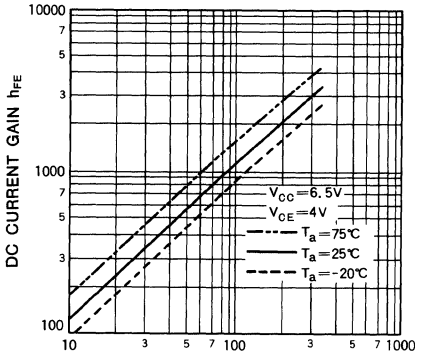
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54529AP

5-UNIT 320mA TRANSISTOR ARRAY WITH STROBE

DESCRIPTION

The M54529AP, 5-channel sink driver, consists of 10 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output sustaining voltage to 20V
- High output sink current to 320mA
- CMOS compatible input with strobe control
- Wide operating temperature range (T_a = −20∼+75℃)

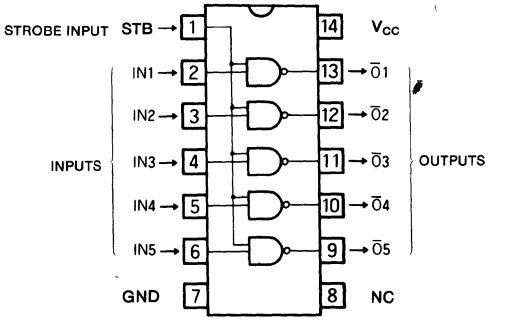
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

The M54529AP uses a predriver stage. Each input has a diode and 30kΩ resistor in series to have a wide input voltage range from −25V to +20V. All input can be controlled simultaneously by a strobe input at pin 1. The power supply of the predrivers is connected to pin 14. All emitters and the substrate are connected together to pin 7 . The outputs are capable of sinking 320mA and will withstand 20V in the OFF state.

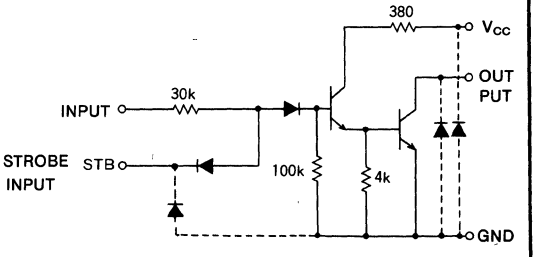
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be vsed.

Unit : Ω

FUNCTIONAL TABLE

IN	STB	OUT
L	L	H
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+20	V
I_C	Collector current per channel	Transistor ON	320	mA
V_I	Input voltage		−20∼+20	V
$V_{I(STB)}$	Strobe input voltage		−0.5∼+20	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

MITSUBISHI ELECTRIC

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3	5	8	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	Percent duty cycle less than 33%, V_{CC}=6.5V	0		300	mA
		Percent duty cycle less than 80%, V_{CC}=6.5V	0		150	
V_{IH}	"H" Input voltage	I_C=150mA	3.5		15	V
		I_C=300mA	5		15	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		1	V
$V_{IH(STB)}$	"H" Input voltage (strobe input)		2.4		15	V
$V_{IL(STB)}$	"L" Input voltage (strobe input)		0		0.2	V

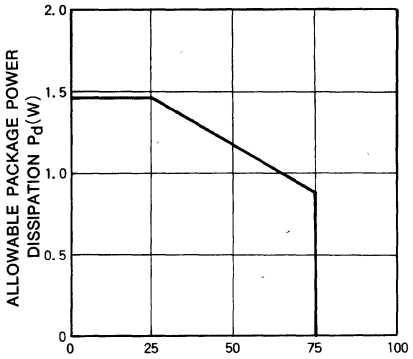
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	V_{CC}=8V, V_I=8V, $V_{I(STB)}$=0.2V, I_{CEO}=100μA		20			V
$V_{CE(sat)}$	Output saturation voltage	$V_{I(STB)}$=2.4V	V_{CC}=6.5V, V_I=5V, I_C=250mA		0.35	0.85	V
			V_{CC}=3V, V_I=3.5V, I_C=150mA		0.2	0.6	
I_I	Input current	V_{CC}=5V, V_I=3.5V, $V_{I(STB)}$=2.4V			20	120	μA
I_R	Input leakage current	V_{CC}=8V, V_I=−20V				−20	μA
$I_{I(STB)}$	Strobe input current	V_{CC}=5V, V_I=5V all input, $V_{I(STB)}$=0.2V			−0.8	−1.5	mA
$I_{R(STB)}$	Strobe input leakage current	V_{CC}=8V, V_I=0V, $V_{I(STB)}$=20V				10	μA
I_{CC}	Supply current	V_{CC}=8V, V_I=5V all input, $V_{I(STB)}$=2.4V			95	170	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=6.5V, I_C=300mA, T_a=25℃, $V_{IH(STB)}$=2.4V		1000	18000		—

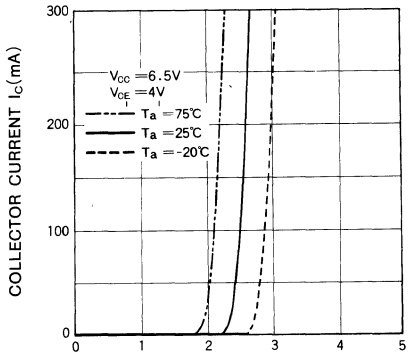
* : Typical values are at T_a = 25℃

TYPICAL CHARACTERISTICS

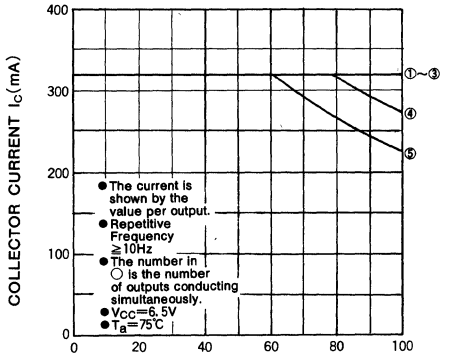
ALLOWABLE AVERAGE POWER DISSIPATION



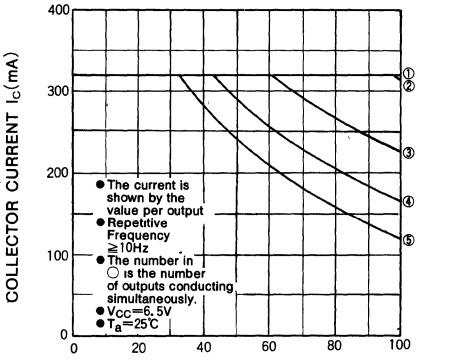
OUTPUT CURRENT CHARACTERISTICS



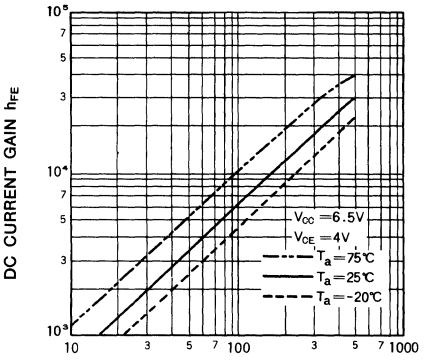
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54530P

7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54530P, 7-channel sink driver, consists of 14 NPN transistors connected to form seven high current gain driver pairs.

FEATURES

- High output sustaining voltage to 40V
- High output sink current to 400mA
- Integral diodes for transient suppression
- PMOS compatible input
- Wide operating temperature range (T_a = −20∼+75℃)

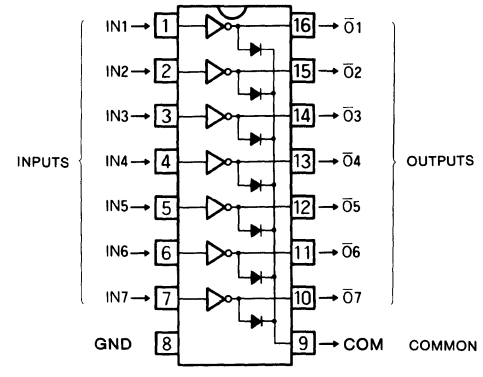
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

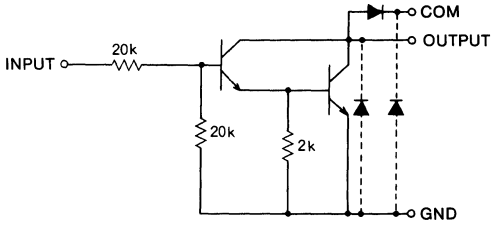
The M54530P is comprised of seven NPN darlington driver pairs with 20kΩ series input resistors. Between pin 9 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 8 . The outputs are capable of sinking 400mA and will withstand 40V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be vsed.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+40	V
I_C	Collector current per channel	Transistor ON	400	mA
V_I	Input voltage		−0.5∼+40	V
I_F	Clamp diode forward current		400	mA
V_R	Clamp diode reverse voltage		−0.5∼+40	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		40	V
I_C	Collector current per channel	Percent duty cycle less than 8%	0		400	mA
		Percent duty cycle less than 30%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	8		35	V
		I_C=200mA	5		35	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.5	V

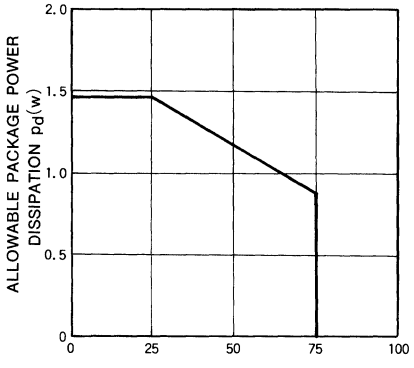
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CER}=100μA	40			V
$V_{CE(sat)}$	Output saturation voltage	V_I=8V, I_C=400mA		1.3	2.4	V
		V_I=5V, I_C=200mA		1	1.6	
I_I	Input current	V_I=17V		0.85	1.8	mA
		V_I=35V		2.0	3.8	
V_F	Clamp diode forward voltage	$I_{F(D)}$=400mA		1.5	2.4	V
V_R	Clamp diode reverse voltage	$V_{R(D)}$=100μA	40			V
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=300mA, T_a=25℃	1000	3500		—

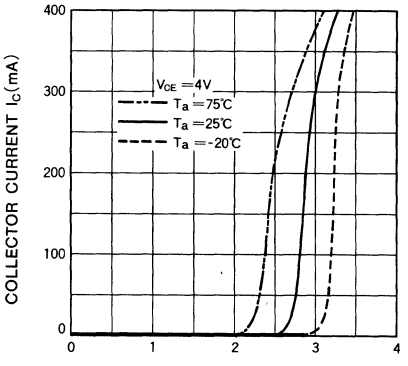
* : Typical values are at T_a = 25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

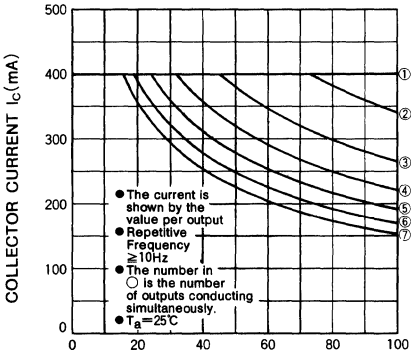


OUTPUT CURRENT CHARACTERISTICS

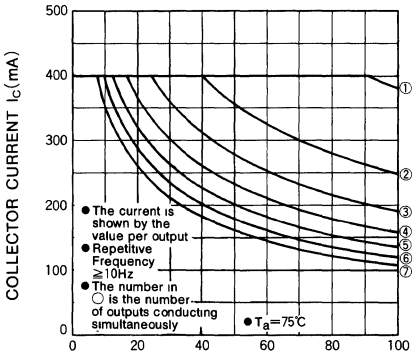


7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

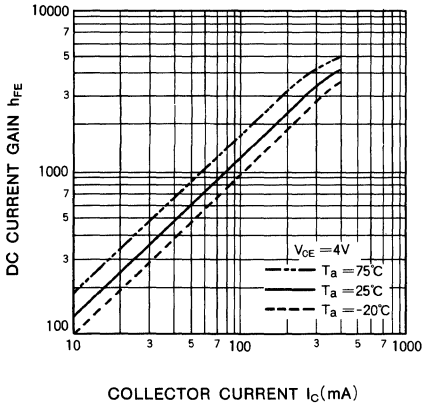
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



M54531P

7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54531P, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 40V
- High output sink current to 400mA
- Integral diodes for transient suppression
- PMOS compatible input
- Wide input voltage range from −40V to +40V
- Wide operating temperature range (T_a = −20～+75℃)

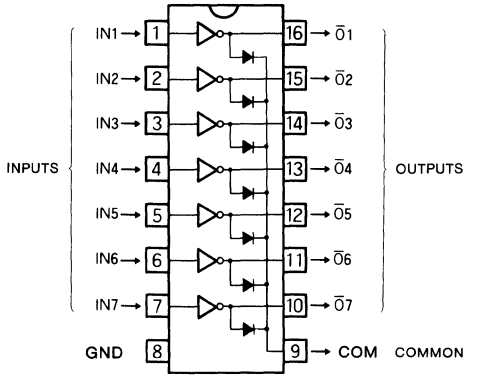
APPLICATION

Relay and printer driver, LED and incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

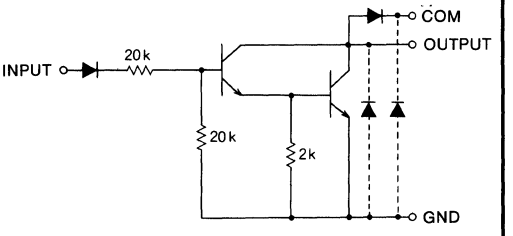
The M54531P is comprised of seven NPN darlington driver pairs. Each input has a diode and 20kΩ resistor in series to allow a negative voltage input. Between pin 9 and each out, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 8 . The outputs are capable of sinking 400mA and will withstand 40V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5～+40	V
I_C	Collector current per channel	Transistor ON	400	mA
V_I	Input voltage		−40～+40	V
$I_{F(D)}$	Clamp diode forward current		400	mA
$V_{R(D)}$	Clamp diode reverse voltage		40	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		40	V
I_C	Collector current per channel	Percent duty cycle less than 8%	0		400	mA
		Percent duty cycle less than 30%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	9		35	V
		I_C=200mA	6		35	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		1	V

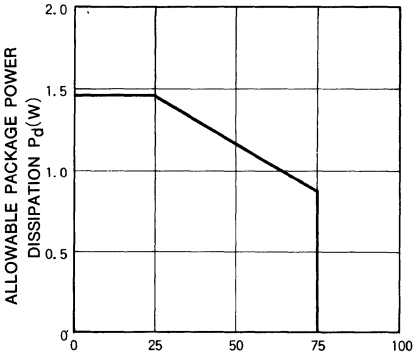
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	40			V
$V_{CE(sat)}$	Output saturation voltage	V_i=9V, I_C=400mA		1.3	2.4	V
		V_i=6V, I_C=200mA		1	1.6	
I_I	Input current	V_i=18V		0.85	1.8	mA
		V_i=35V		2.0	3.8	
I_R	Input leakage current	V_i=−35V			−20	μA
$V_{F(D)}$	Clamp diode forward voltage	$I_{F(D)}$=400mA		1.5	2.4	V
$V_{R(D)}$	Clamp diode reverse voltage	$I_{R(D)}$=100μA	40			V
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=300mA, T_a=25℃	1000	3500		—

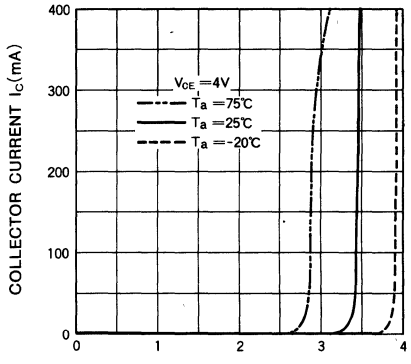
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

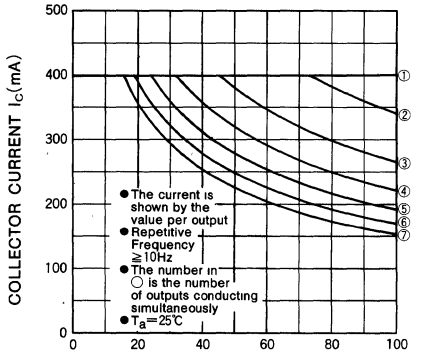


OUTPUT CURRENT CHARACTERISTICS



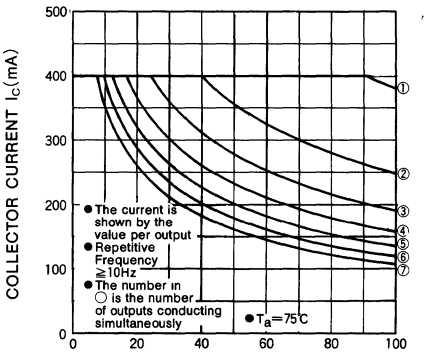
7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



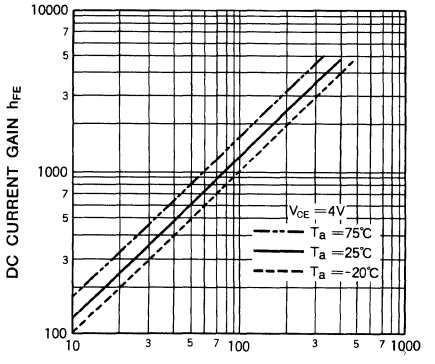
DUTY CYCLE (%)

ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DUTY CYCLE (%)

DC CURRENT GAIN CHARACTERISTICS



COLLECTOR CURRENT I_C(mA)

M54532P

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54532P, 4-channel sink driver, consists of 8 NPN transistors connected to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 50V
- High output sink current to 1.5A
- Integral diodes for transient suppression
- Wide operating temperature range (T_a = −20∼+75℃)

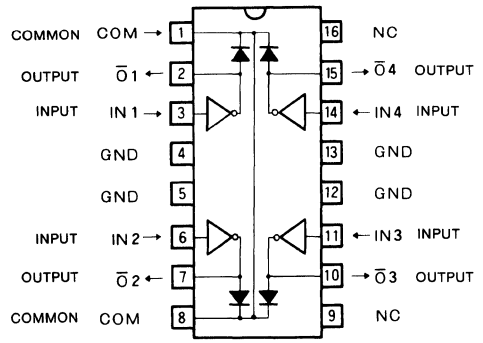
APPLICATION

Relay and printer driver, Display driver

FUNCTION

The M54532P is comprised of eight NPN darlington driver pairs with 340Ω series input resistors. Each output has a diode for inductive load transient suppression and the cathodes of the diodes are connected to pin 8 . The outputs are capable of sinking 1.5A and will withstand 50V in the OFF state.

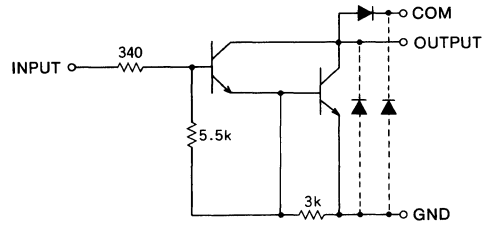
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+50	V
I_C	Collector current per channel	Transistor ON	1.5	A
V_I	Input voltage		−0.5∼+10	V
$I_{F(D)}$	Clamp diode forward current	Pulse width ≦ 10ms, Percent duty cycle ≦ 5%	1.5	A
		Pulse width ≦ 100ms, Percent duty cycle ≦ 5%	1.25	
$V_{R(D)}$	Clamp diode reverse voltage		−0.5∼+50	V
P_d	Power dissipation	T_a=25℃	1.92	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		50	V
I_C	Collector current per channel	Percent duty cycle less than 4%	0		1.25	A
		Percent duty cycle less than 18%	0		700	mA
V_{IH}	"H" Input voltage	I_C=1.25A	3		6	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.4	V

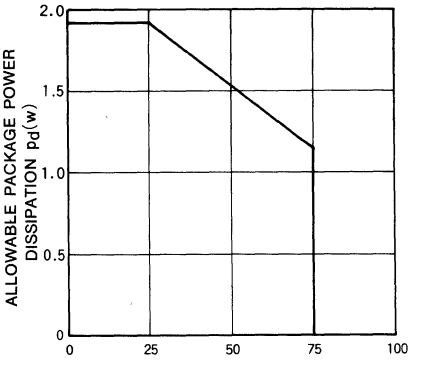
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA		50			V
$V_{CE(sat)}$	Output saturation voltage	I_I=2mA	I_C=1.25A		1.3	2.2	V
			I_C=700mA		1.1	1.7	
I_I	Input current	V_I=3V			5	8.5	mA
V_F	Clamp diode forward voltage	I_F=1.25A			1.6	2.3	V
V_R	Clamp diode reverse voltage	I_R=100μA		50			V
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=1A, T_a=25℃		800	7000		—

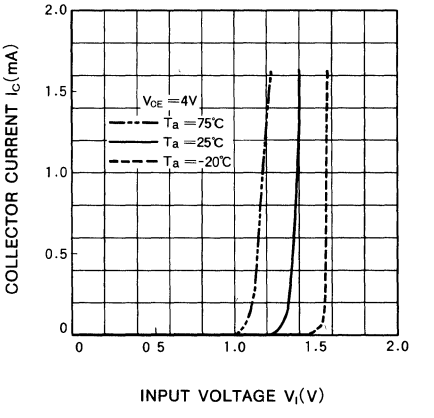
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



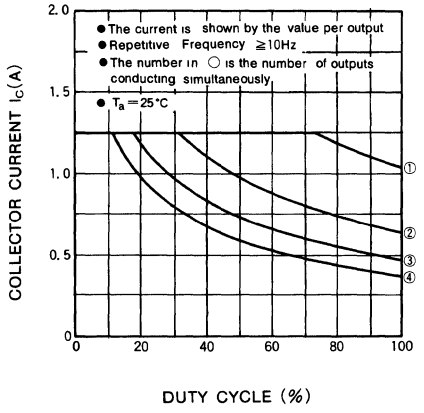
OUTPUT CURRENT CHARACTERISTICS



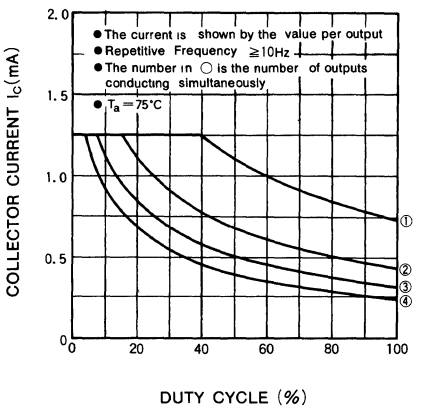
MITSUBISHI ELECTRIC

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

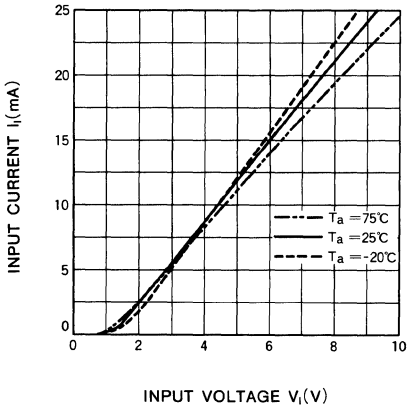
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



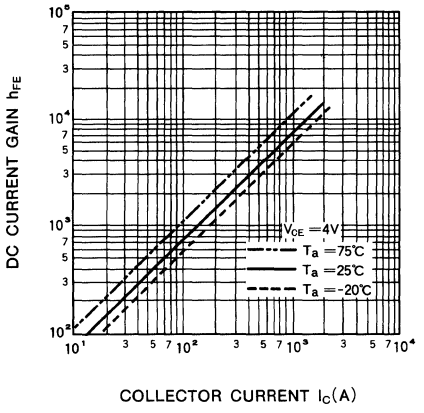
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54533P

6-UNIT 320mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

DESCRIPTION

The M54533P, 6-channel sink driver, consists of 12 NPN transistors to form high current gain driver pairs.

FEATURES

- Output breakdown voltage to 20V
- High output sink current to 320mA
- Integral diode for transient suppression
- Strobe control input
- Wide input voltage range from −25V to +20V
- Wide operating temperature range (T_a = −20～+75℃)

APPLICATION

Relay and printer driver, LED or incandescent display digit driver

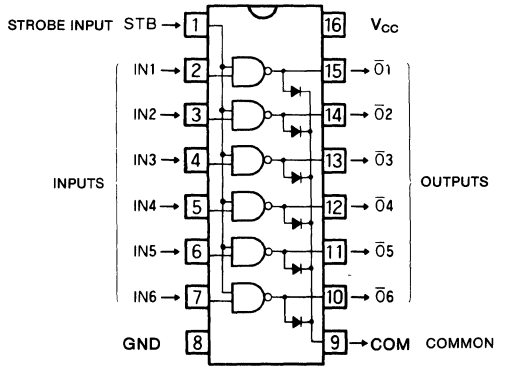
FUNCTION

The M54533P uses a predriver stage. Each input has a diode and 20kΩ resistor in series to allow a negative voltage input. All input can be controlled simultaneously by a strobe input at pin 1 .

The power supply of the predrivers is connected to pin 16. All emitters and the substrate are connected together to pin 8 . Each output has an integral diode for inductive load transient suppression and the cathodes of the diodes are connected to pin 9 .

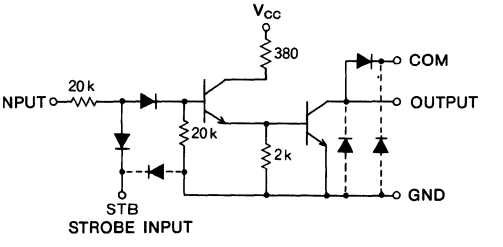
The outputs are capable of sinking 320mA and will withstand 20V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

FUNCTIONAL TABLE

IN	STB	OUT
L	L	H
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a=−25～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5～+20	V
I_C	Collector current	Transistor ON	350	mA
V_I	Input voltage		10	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

6-UNIT 320mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3		8	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	Percent duty cycle less than 25%, V_{CC}=6.5V	0		300	mA
		Percent duty cycle less than 65%, V_{CC}=6.5V	0		150	
V_{IH}	"H" Input voltage	I_C=300mA	7		18	V
		I_C=150mA	5		18	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		1	V
$V_{IH(STB)}$	"H" Input voltage (strobe input)		2.4		18	V
$V_{IL(STB)}$	"L" Input voltage (strobe input)		0		0.2	V

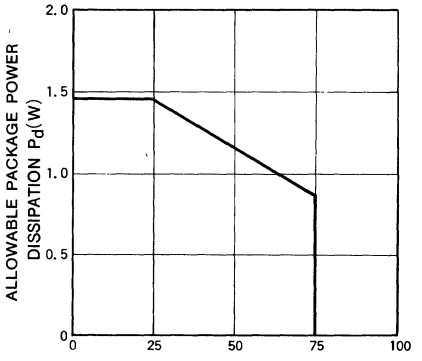
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	V_{CC}=8V, V_I=18V, $V_{I(STB)}$=0.2V, I_{CEO}=100μA		20			V
$V_{CE(sat)}$	Output saturation voltage	V_I=7V	V_{CC}=6.5V, I_C=250mA		0.5	0.85	V
		$V_{I(STB)}$=2.4V	V_{CC}=3V, I_C=120mA		0.3	0.5	
I_I	Input current	V_{CC}=8V, V_I=18V, $V_{I(STB)}$=2.4V			0.8	1.8	mA
I_R	Input leakage current	V_{CC}=8V, V_I=−25V				−20	μA
$I_{I(STB)}$	Strobe input current	V_{CC}=8V, V_I=18V (all input), $V_{I(STB)}$=0.2V			−4	−10	mA
$I_{R(STB)}$	Strobe input leakage current	V_{CC}=8V, V_I=0V, $V_{I(STB)}$=20V				20	μA
$V_{F(D)}$	Clamp diode forward voltage	$I_{F(D)}$=320mA			1.4	2.4	V
$V_{R(D)}$	Clamp diode reverse voltage	$I_{R(D)}$=100μA		20	40		V
I_{CC}	Supply current	V_{CC}=8V, V_I=7V (all input), $V_{I(STB)}$=2.4V			120	200	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=6.5V, I_C=300mA, T_a=25℃, $V_{I(STB)}$=2.4V		1000	3000		—

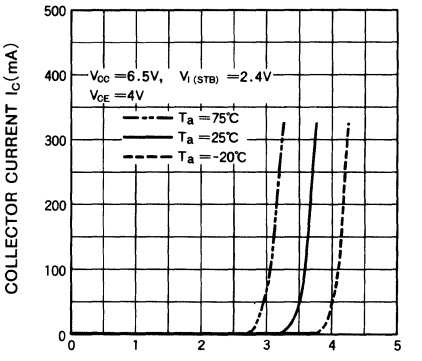
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

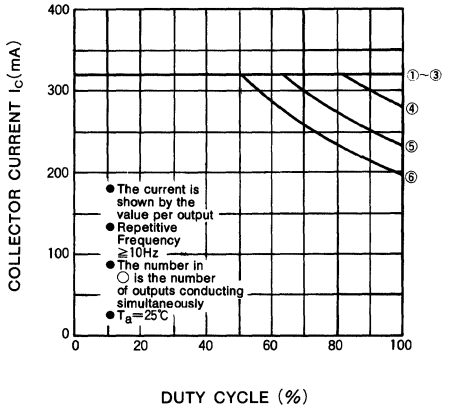
ALLOWABLE AVERAGE POWER DISSIPATION



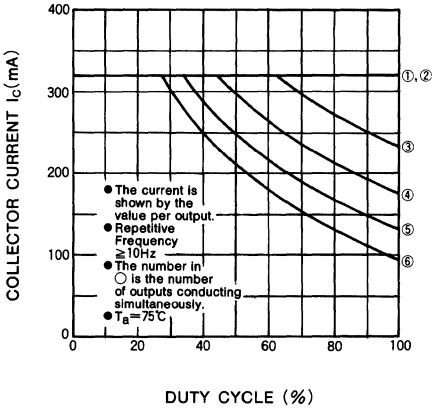
OUTPUT CURRENT CHARACTERISTICS



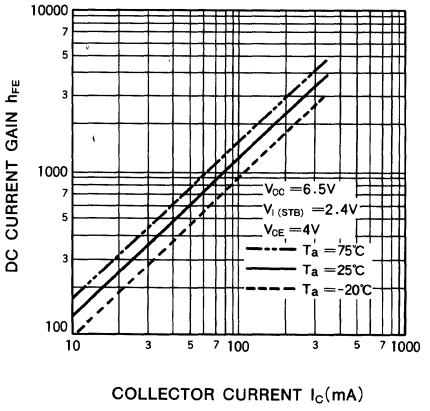
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54534P

6-UNIT 320mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

DESCRIPTION

The M54534P, 6-channel sink driver, consists of 12 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output breakdown voltage to 20V
- High output sink current to 320mA
- Integral diodes for transient suppression
- Strobe control input
- Wide input voltage range from −25V to +20V
- Wide operating temperature range (T_a = −20～+75℃)

APPLICATION

Relay and printer driver, LED or incandescent display digit driver

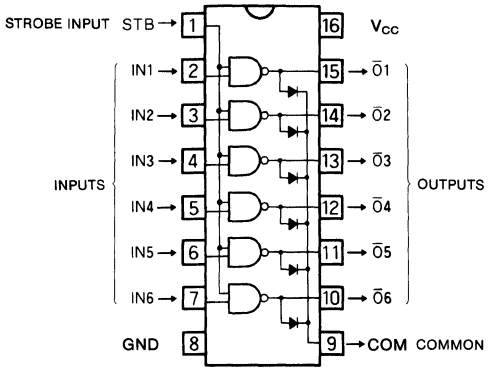
FUNCTION

The M54534P uses a predriver stage. Each input has a diode and 1.6kΩ resistor in series to allow a negative voltage input. All input can be controlled simultaneously by a strobe input at pin 1 .

The power supply of the predrivers is connected to pin 16. Each output has an integral diode for inductive load transient suppression and the cathodes of the diodes are connected to pin 9 . All emitters and the substrate are connected together to pin 8 .

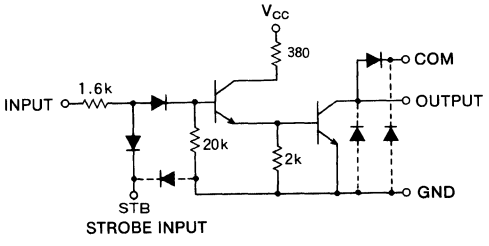
The outputs are capable of sinking 320mA and will withstand 20V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used Unit : Ω

FUNCTIONAL TABLE

IN	STB	OUT
L	L	H
H	L	H
L	H	H
H	H	L

ABSOLUTE MAXIMUM RATINGS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5～+20	V
I_C	Collector current per channel	Transistor ON	320	mA
V_I	Input voltage		−25～+20	V
$V_{I(STB)}$	Strobe input voltage		−0.5～+20	V
$V_{R(D)}$	Clamp diode reverse voltage		20	V
$I_{F(D)}$	Clamp diode forward current		320	mA
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

M54534P

6-UNIT 320mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3		8	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	Percent duty cycle less than 25%, V_{CC}=6.5V	0		300	mA
		Percent duty cycle less than 65%, V_{CC}=6.5V	0		150	
V_{IH}	"H" Input voltage	I_C=300mA	3.2		18	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.7	V
$V_{IH(STB)}$	"H" Input voltage (strobe input)		2.4		18	V
$V_{IL(STB)}$	"L" Input voltage (strobe input)		0		0.2	V

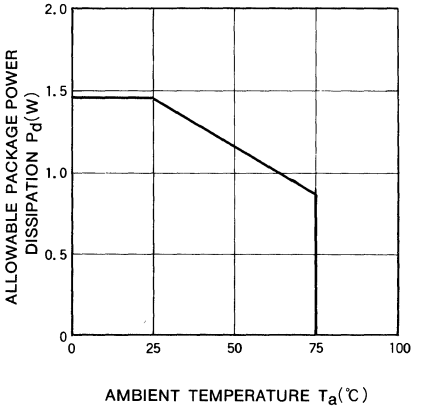
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	V_{CC}=8V, V_I=3.2V, $V_{I(STB)}$=0.2V, I_{CEO}=100μA		20			V
$V_{CE(sat)}$	Output saturation voltage	V_I=3V, $V_{I(STB)}$=2.4V	V_{CC}=6.5V, I_C=250mA		0.5	0.85	V
			V_{CC}=3V, I_C=120mA		0.3	0.5	
I_I	Input current	V_{CC}=8V, V_I=3.2V, $V_{I(STB)}$=2.4V			0.5	1.4	mA
I_R	Input leakage current	V_{CC}=8V, V_I=−25V				−20	μA
$I_{I(STB)}$	Strobe input current	V_{CC}=8V, V_I=3.2V (all input), $V_{I(STB)}$=0.2V			−7.9		mA
$I_{R(STB)}$	Strobe input leakage current	V_{CC}=8V, V_I=0V, $V_{I(STB)}$=20V				20	μA
$V_{F(D)}$	Clamp diode forward voltage	$I_{F(D)}$=320mA			1.4	2.4	V
$V_{R(D)}$	Clamp diode reverse voltage	$I_{R(D)}$=100μA		20	40		V
I_{CC}	Supply current	V_{CC}=8V, V_I=3.2V (all input), $V_{I(STB)}$=2.4V			120	200	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=6.5V, I_C=300mA, T_a=25℃, $V_{I(STB)}$=2.4V		1000	3000		—

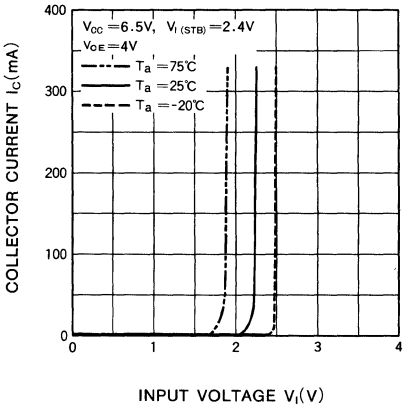
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



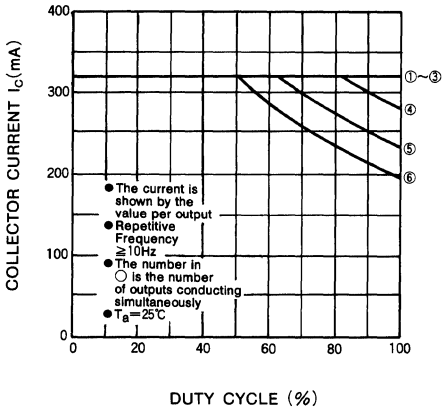
OUTPUT CURRENT CHARACTERISTICS



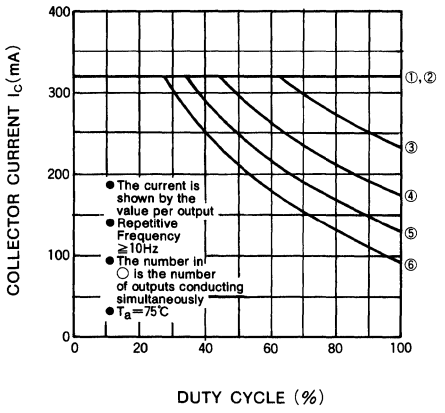
MITSUBISHI ELECTRIC

6-UNIT 320mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

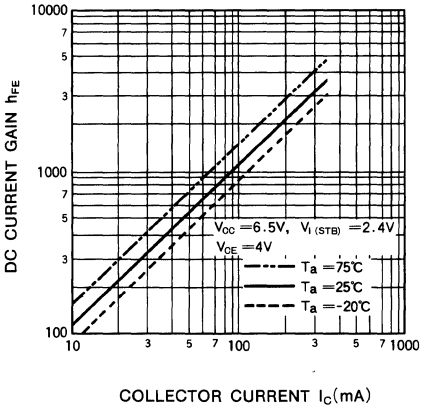
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54535P

7-UNIT 150mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

DESCRIPTION

The M54535P, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output sink current to 150mA
- Strobe input control
- PMOS Compatible input
- Wide operating temperature range (T_a = −20∼+75℃)

APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

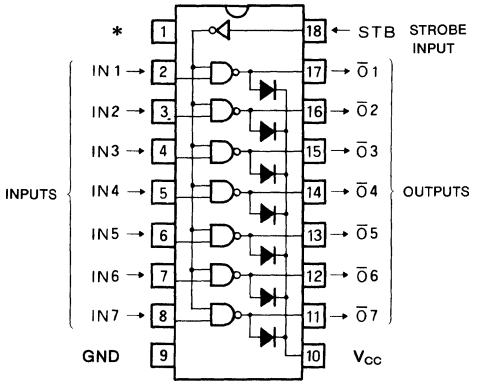
FUNCTION

The M54535P uses a predriver stage. Each input has a diode and 20kΩ resistor in series to allow a negative voltage input. All inputs can be controlled simultaneously by a strobe input at pin 18. Each output has an integral diode for inductive load transient suppression.

The cathodes of the diodes and the power supply of the predrivers are connected to pin 10. All emitters and the substrate are connected together to pin 9 .

The outputs are capable of sinking 150mA and will withstand 10V in the OFF state.

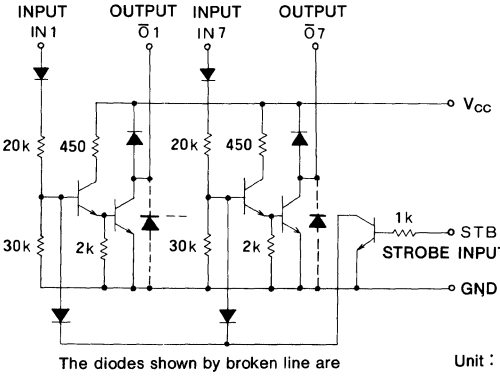
PIN CONFIGURATION (TOP VIEW)



Outline 18P4

* : Open

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

FUNCTIONAL TABLE

IN	STB	OUT
L	L	H
H	L	L
L	H	H
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		10	V
V_O	Output voltage	Transistor OFF	−0.5∼V_{CC}	V
I_C	Collector current	Transistor ON	150	mA
V_I	Input voltage		−25∼+20	V
$V_{I(STB)}$	Strobe input voltage		20	V
$V_{R(D)}$	Clamp diode reverse voltage		10	V
$I_{F(D)}$	Clamp diode forward current		150	mA
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

7-UNIT 150mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3		8	V
V_O	Output voltage	V_{CC}=10V	0		10	V
I_C	Collector current per channel	Percent duty cycle less than 65%	0		150	mA
V_{IH}	"H" Input voltage	I_C=100mA	7		18	V
V_{IL}	"L" Input voltage		0		0.8	V
$V_{IH(STB)}$	"H" Input voltage (strobe input)	V_I=12V	1.3		6	V
		V_I=20V	2.4		6	
$V_{IL(STB)}$	"L" Input voltage (strobe input)		0		0.2	V

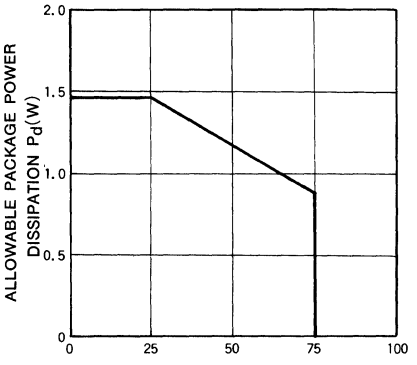
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{CE(sat)}$	Output saturation voltage	$V_{I(STB)}$=0.2V, V_{CC}=6V, I_I=300μA, I_C=100mA			0.1	0.3	V
		V_I=7V, $V_{I(STB)}$=0.2V	V_{CC}=3V, I_C=100mA		0.1	0.3	
			V_{CC}=8V, I_C=150mA		0.16	0.5	
$I_{O(leak)}$	Output leak current	V_{CC}=8V, V_I=0.8V, V_O=8V, $V_{I(STB)}$=0.2V				50	μA
I_I	Input current	V_{CC}=8V, V_I=12V, $V_{I(STB)}$=0.2V			0.5	1	mA
I_R	Input leakage current	V_{CC}=8V, V_I=−25V				−20	μA
$I_{I(STB)}$	Strobe input current	V_I=12V, $V_{I(STB)}$=2.4V			0.6	3	mA
$V_{F(D)}$	Clamp diode forward voltage	$I_{F(D)}$=150mA			1.1	2.1	V
$V_{R(D)}$	Clamp diode reverse voltage	$I_{R(D)}$=100μA		10			V
I_{CC}	Supply current	V_{CC}=8V, V_I=12V all input, $V_{I(STB)}$=0.2V			120	200	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=6V, I_C=150mA, T_a=25℃		700	2500		—

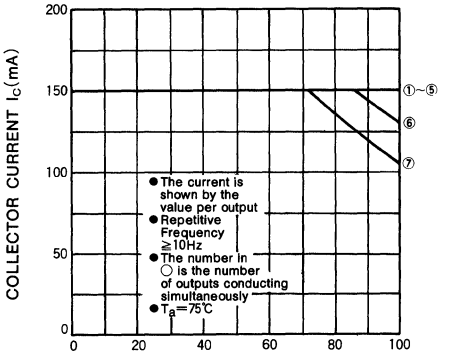
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

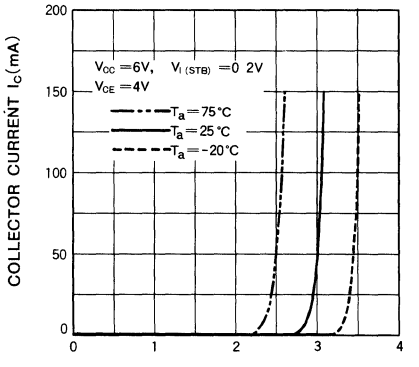
ALLOWABLE AVERAGE POWER DISSIPATION



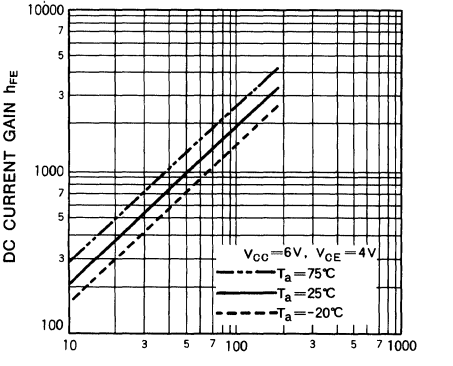
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54536P

7-UNIT 150mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

DESCRIPTION

The M54536P, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output sink current to 150mA
- Strobe input control
- TTL Compatible input
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

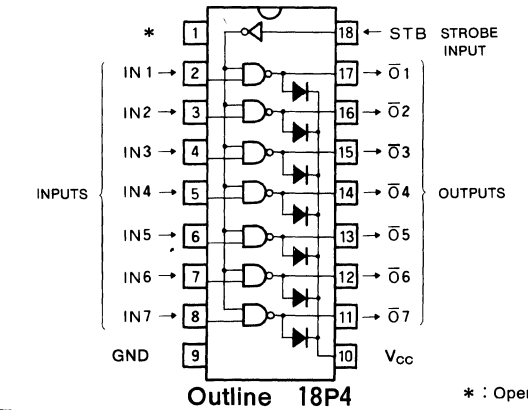
FUNCTION

The M54536P uses a predriver stage. Each input has a diode and 20kΩ resistor in series to allow a negative voltage input. All inputs can be controlled simultaneously by a strobe input at pin 18. Each output has an integral diode for inductive load transient suppression.

The cathodes of the diodes and the power supply of the predrivers are connected to pin 10. All emitters and the substrate are connected together to pin 9.

The outputs are capable of sinking 150mA and will withstand 10V in the OFF state.

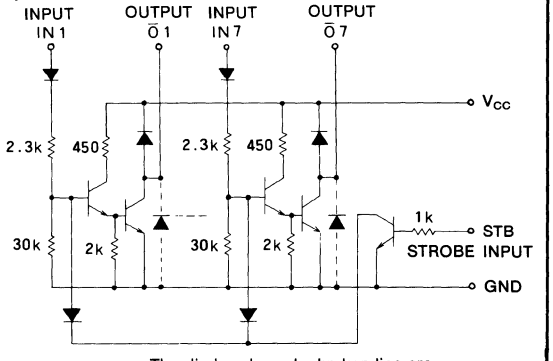
PIN CONFIGURATION (TOP VIEW)



Outline 18P4

* : Open

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

FUNCTION TABLE

IN	STB	OUT
L	L	H
H	L	L
L	H	H
H	H	H

ABSOLUTE MAXIMUM RATINGS (T_a=−25∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		10	V
V_O	Output voltage	Transistor OFF	−0.5∼V_{CC}	V
I_C	Collector current	Transistor ON	150	mA
V_I	Input voltage		−25∼+10	V
$V_{I(STB)}$	Strobe input voltage		20	V
$V_{R(D)}$	Clamp diode reverse voltage		10	V
$I_{F(D)}$	Clamp diode forward current		150	mA
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

7-UNIT 150mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−25∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3		8	V
V_O	Output voltage	V_{CC}=10V	0		10	V
I_C	Collector current per channel	Percent duty cycle less than 65%	0		150	mA
V_{IH}	"H" Input voltage	I_C=100mA	3.2		6	V
V_{IL}	"L" Input voltage		0		0.8	V
$V_{IH(STB)}$	"H" Input voltage (strobe input)	V_I=3.5V	1.3		6	V
		V_I=10V	2.4		6	
$V_{IL(STB)}$	"L" Input voltage (strobe input)		0		0.2	V

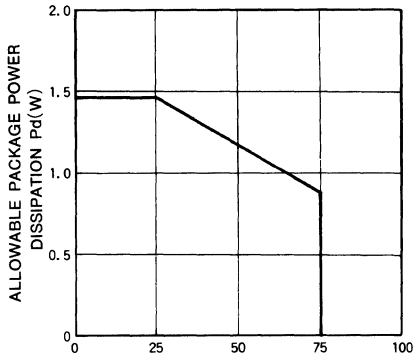
ELECTRICAL CHARACTERISTICS (T_a=−25∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{CE(sat)}$	Output saturation voltage	$V_{I(STB)}$=0.2V, V_{CC}=6V, I_I=300μA, I_C=100mA			0.1	0.3	V
		V_I=3.2V, $V_{I(STB)}$=0.2V	V_{CC}=3V, I_C=100mA		0.1	0.3	
			V_{CC}=8V, I_C=150mA		0.16	0.5	
$I_{O(leak)}$	Output leak current	V_{CC}=8V, V_I=0.8V, V_O=8V, $V_{I(STB)}$=0.2V				50	μA
I_I	Input current	V_{CC}=8V, V_I=3.5V, $V_{I(STB)}$=0.2V			0.6	1.2	mA
I_R	Input leakage current	V_{CC}=8V, V_I=−25V				−20	μA
$I_{I(STB)}$	Strobe input current	V_I=3.5V, $V_{I(STB)}$=2.4V			0.9	3	mA
$V_{F(D)}$	Clamp diode forward voltage	$I_{F(D)}$=150mA			1.1	2.1	V
$V_{R(D)}$	Clamp diode reverse voltage	$I_{R(D)}$=100μA		10			V
I_{CC}	Supply current	V_{CC}=8V, V_I=3.5V (all input), $V_{I(STB)}$=0.2V			120	200	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=6V, I_C=150mA, T_a=25℃		700	3000		—

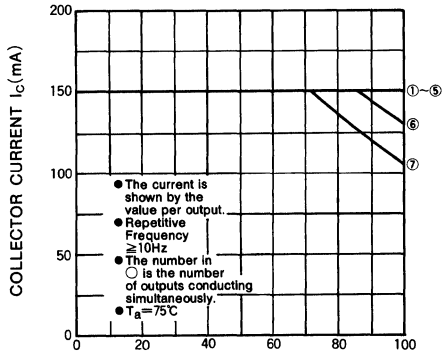
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

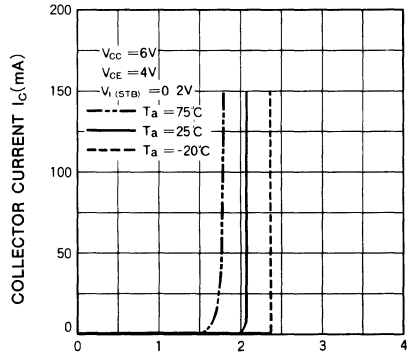
ALLOWABLE AVERAGE POWER DISSIPATION



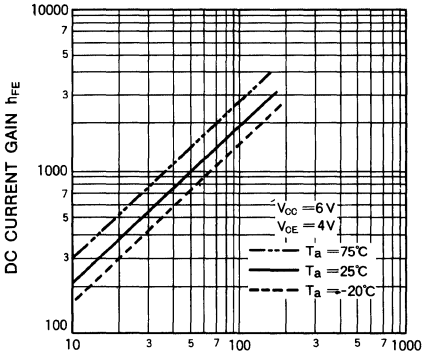
ALLOWABLE COLLECT CURRENT AS A FUNCTION OF DUTY CYCLE



OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54537P

7-UNIT 350mA TRANSISTOR ARRAY

DESCRIPTION

The M54537P, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output breakdown voltage to 20V
- High output sink current to 250mA
- PMOS Compatible input
- Low output saturation voltage
- Wide operating temperature range (T_a = −20∼+75℃)

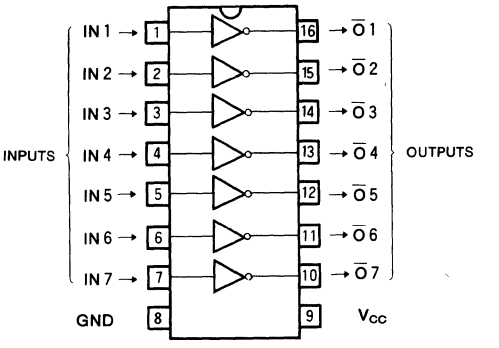
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

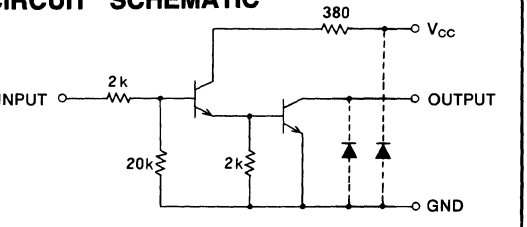
The M54537P uses a predriver stage with 2kΩ series input resistor. The power supply of the predrivers is connected to pin 9 . All emitters and the substrate are connected together to pin 8 . The outputs are capable of sinking 250mA and will withstand 20V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−25∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+20	V
I_C	Collector current	Transistor ON	350	mA
V_I	Input voltage		10	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−25∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3		8	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	V_{CC}=6.5V Percent duty cycle less than 40%	0		250	mA
		V_{CC}=6.5V Percent duty cycle less than 65%	0		150	
V_{IH}	"H" Input voltage	I_C=250mA	3		6	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.3	V

MITSUBISHI ELECTRIC

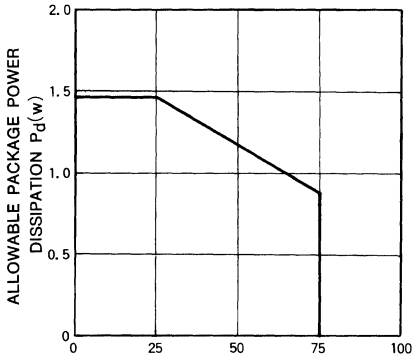
ELECTRICAL CHARACTERISTICS (T_a=−25～+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	V_{CC}=8V, I_{CEO}=100μA		20			V
$V_{CE(sat)}$	Output saturation voltage	V_I=3V	V_{CC}=6.5V, I_C=250mA		0.28	0.5	V
			V_{CC}=3V, I_C=150mA		0.17	0.35	
I_I	Input current	V_{CC}=8V, V_I=3.2V			0.7	1.5	mA
		V_{CC}=8V, V_I=10V			3.8	7.3	
I_{CC}	Supply current	V_{CC}=8V, V_I=3.2V			130	190	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=6.5V, I_C=250mA, T_a=25℃		1000	7000		—

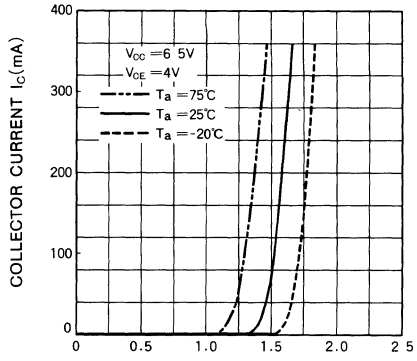
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

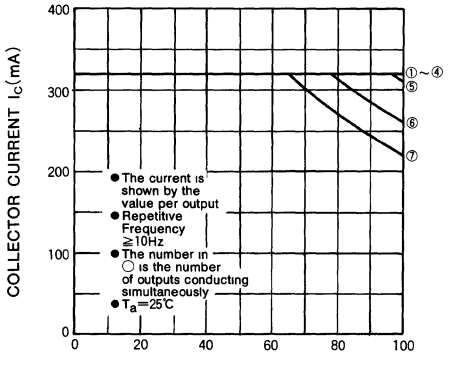
ALLOWABLE AVERAGE POWER DISSIPATION



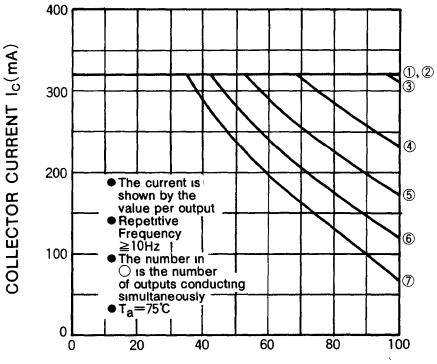
OUTPUT CURRENT CHARACTERISTICS



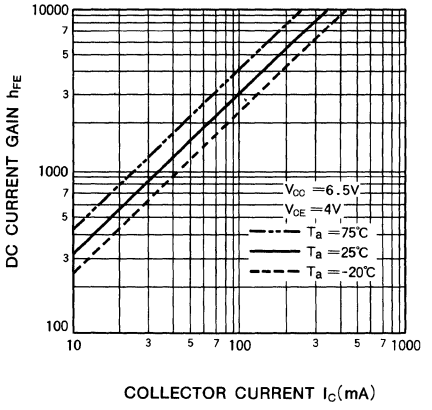
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



MITSUBISHI ELECTRIC

M54538P

7-UNIT 350mA TRANSISTOR ARRAY AND MOTOR DRIVER

DESCRIPTION

The M54538P, 7-channel sink driver and a motor driver, is designed for use in a thermal printer.

FEATURES

- Output breakdown voltage to 20V
- High output sink current to 350mA
- Wide operating temperature range (T_a = −20∼+75℃)

APPLICATION

Thermal printer driver, LED or incandescent display driver, Interfacing for standard MOS/BIPOLAR logic

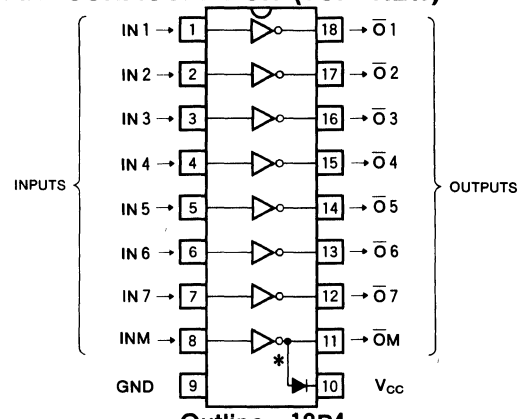
FUNCTION

The M54538P is designed for use in a thermal printer, consisting 7-channel thermal head driver and a D-C or stepper motor driver.

The output of the motor driver has a diode for inductive load transient suppression.

The outputs of the sink drivers are capaple of sinking 350mA and will withstand 20V in the OFF state.

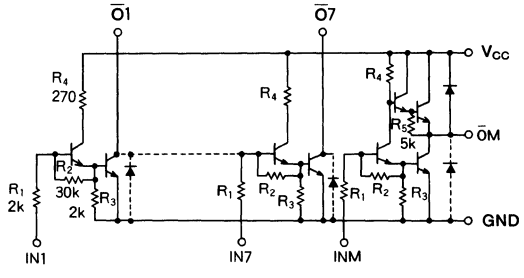
PIN CONFIGURATION (TOP VIEW)



Outline 18P4

* : MOTOR DRIVER

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions		Ratings	Unit
V_{CC}	Supply voltage			10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	Ō1 to Ō7 Outputs	−0.5∼+20	V
			ŌM Output	−0.5∼V_{CC}	
I_C	Collector current	Transistor ON		350	mA
V_I	Input voltage			10	V
I_F	Clamp diode forward current	Pulse width≦35ms, Percent duty cycle≦5%		700	mA
				350	
P_d	Power dissipation	T_a=25℃		1.47	W
Topr	Operating temperature			−20∼+75	℃
Tstg	Storage temperature			−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3		6	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	Percent duty cycle less than 30%, V_{CC}=6V	0		250	mA
		Percent duty cycle less than 35%, V_{CC}=6V	0		170	
V_{IH}	"H" Input voltage	I_C=250mA	3.2		6	V
		I_C=150mA	2.4		6	
V_{IL}	"L" Input voltage		0		0.3	V

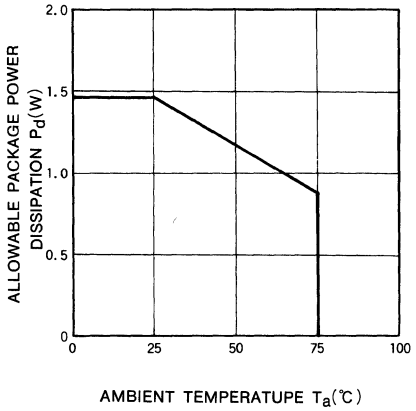
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O\ (leak)}$	Input leakage current	V_{CC}=6V, V_I=0.4V, V_{CE}=20V			50	μA
$V_{CE\ (sat)}$	Output saturation voltage	V_{CC}=3.5V, V_I=3V, I_C=250mA		0.23	0.6	V
		V_{CC}=3V, V_I=2.4V, I_C=150mA		0.14	0.4	
$V_{OH\ (M)}$	"H" Output voltage (motor driver)	V_{CC}=6V, $I_{OH\ (M)}$=−250mA	2.4			V
I_I	Input current	V_{CC}=6V, V_I=3.2V		0.8	1.5	mA
		V_{CC}=6V, V_I=10V		4.6	7.3	
$V_{F\ (M)}$	Clamp diode forward voltage	$I_{F\ (M)}$=350mA		1.6	3	V
I_{CC}	Supply current	V_{CC}=6V, V_I=3.2V (all input)			235	mA
h_{FE}	DC forward current gain	V_{CC}=5V, V_{CE}=4V, I_C=250mA, T_a=25℃	1000	6000		—

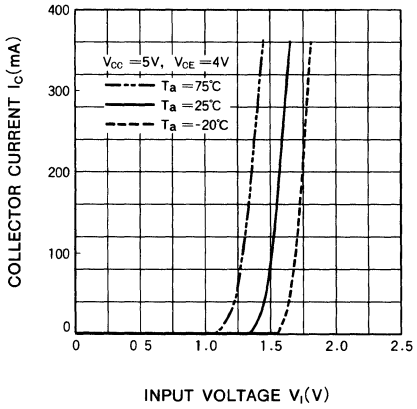
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

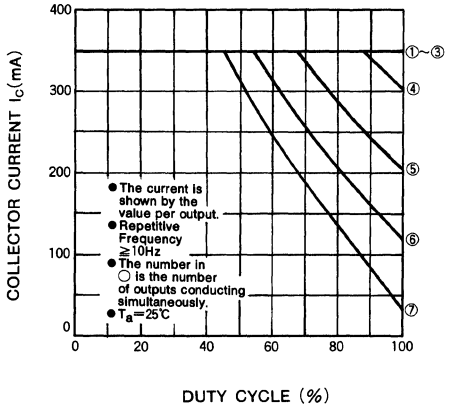
ALLOWABLE AVERAGE POWER DISSIPATION



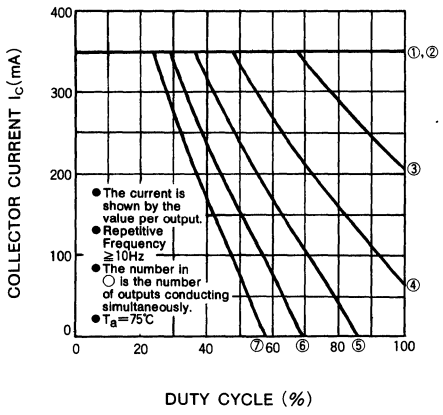
OUTPUT CURRENT CHARACTERISTICS



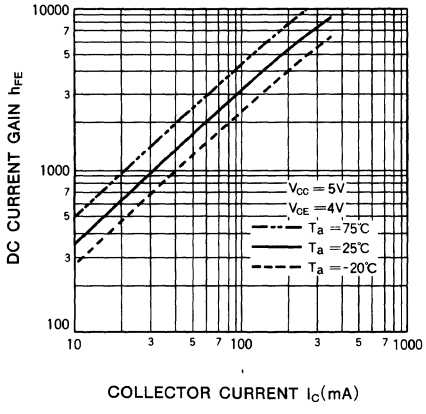
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



M54539P

6-UNIT 700mA TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54539P, 6-channel sink driver, consists of 12 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output breakdown voltage to 20V
- High output sink current to 700mA
- Integral diodes for transient suppression
- Wide operating temperature range (T_a=−20∼+75℃)

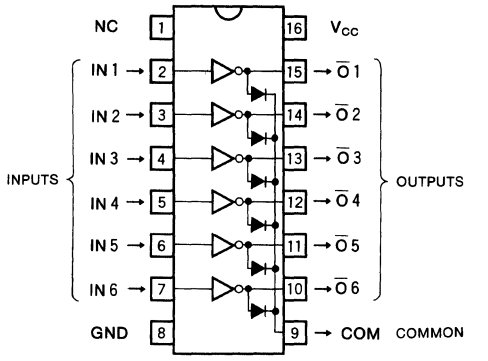
APPLICATION

Relay and solenoid driver, LED or incandescent display driver, Thermal head driver

FUNCTION

The M54539P uses a predriver stage with 2kΩ series input resistor. The power supply of the predrivers is connected to pin 16. Each output has an integral diode for inductive load transient suppression and the cathodes of the diodes are connected to pin 9 . All emitters and the substrate are connected together to pin 8 . The outputs are capable of sinking 700mA and will withstand 20V in the OFF state.

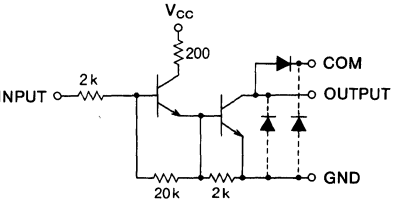
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+20	V
I_C	Collector current	Transistor ON	700	mA
V_I	Input voltage		10	V
V_R	Clamp diode reverse voltage		20	V
I_F	Clamp diode forward current	Pulse width≦35ms, Percent duty cycle≦5%	700	mA
			350	
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3	5	7	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	The three outputs conducting simultaneously Percent duty cycle less than 20%	0		700	mA
		The three outputs conducting simultaneously Percent duty cycle less than 90%	0		200	
V_{IH}	"H" Input voltage	I_C=450mA	3		6	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.3	V

MITSUBISHI ELECTRIC

6-UNIT 700mA TRANSISTOR ARRAY WITH CLAMP DIODE

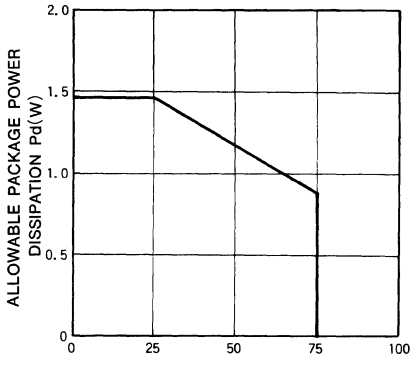
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	V_{CC}=7V, I_{CEO}=100μA		20			V
$V_{CE(sat)}$	Output saturation voltage	V_{CC}=5V	I_C=450mA		0.46	0.8	V
		V_I=3V	I_C=200mA		0.2	0.45	
I_I	Input current	V_{CC}=7V, V_I=3.2V			0.75	1.4	mA
V_R	Clamp diode reverse voltage	I_R=100μA		20			V
V_F	Clamp diode forward voltage	I_F=350mA			1.5	2.7	V
I_{CC}	Supply current	V_{CC}=7V, V_I=3.2V (all input)			190	300	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=6V, I_C=300mA, T_a=25℃		3000	8000		—

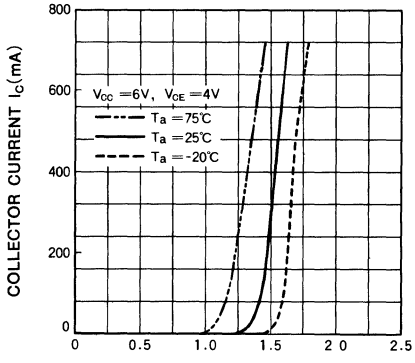
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

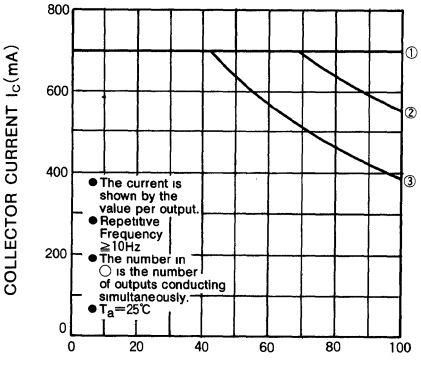
ALLOWABLE AVERAGE POWER DISSIPATION



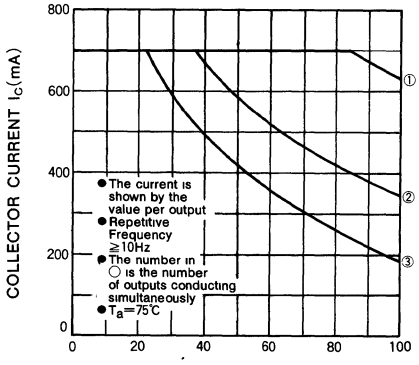
OUTPUT CURRENT CHARACTERISTICS



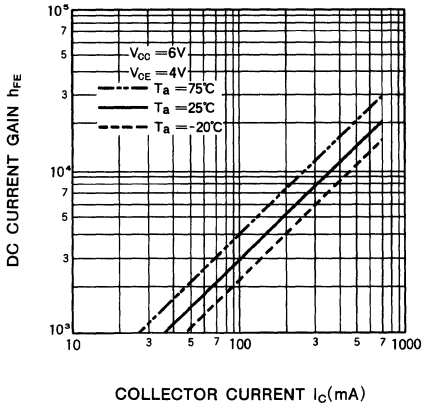
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



M54542L

BI-DIRECTIONAL MOTOR DRIVER

DESCRIPTION

The M54542L, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for D-C motor control.

FEATURES

- 9-pin single inline package with heat shink
- Integral diodes for transient suppression
- 1.2A output current
- PMOS compatible input

APPLICATION

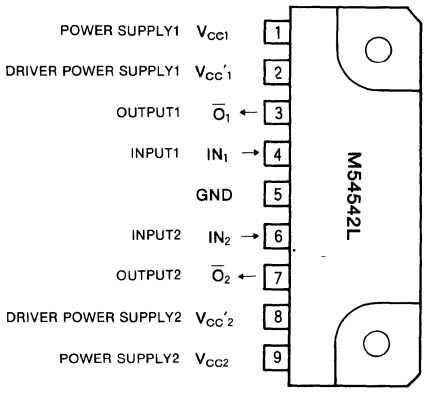
Audio, video cassette recorders, Floppy disk driver

FUNCTION

The M54542L, full bridge motor driver, has the logic circuitry and darlington-pair power drivers for bidirectional control of D-C motors operating at currents up to 1.2A.

The power supplies for the logic circuitry and the drivers are separated so that the applied voltage to the motor can be controlled by the V_{CC}' of the driver power supply voltage.

PIN CONFIGURATION (TOP VIEW)

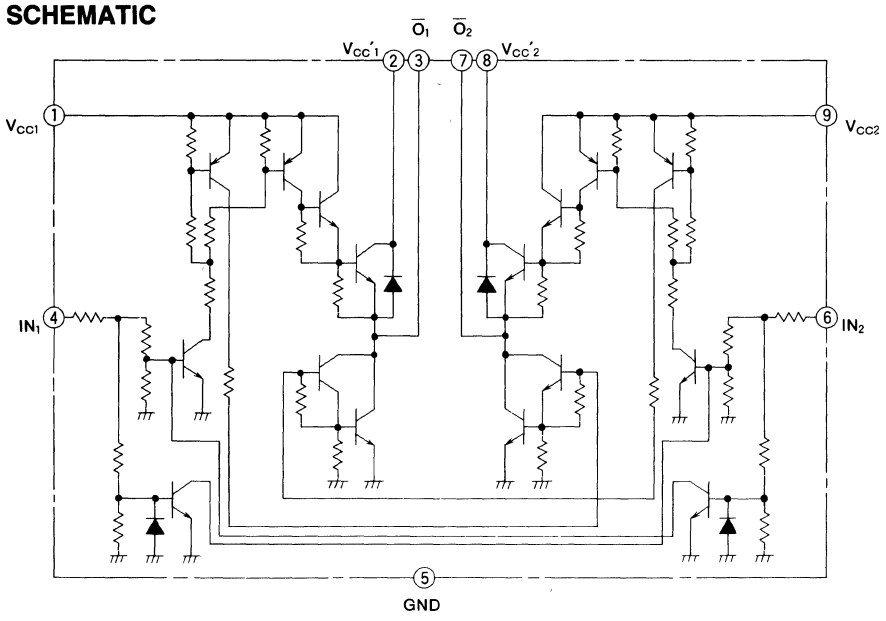


Outline 9P9

LOGIC TRUTH TABLE

INPUT		OUTPUT		NOTE
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	"OFF" state	"OFF" state	Open
H	L	H	L	Ω
L	H	L	H	Ω
H	H	"OFF" state	"OFF" state	Open

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+16	V
V_{CC}'	Driver voltage		−0.5～V_{CC}	V
V_I	Input voltage		−0.5～V_{CC}	V
V_O	Output voltage		−0.5～V_{CC}+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms Repetitive cycle 0.2Hz max	±1200	mA
I_O	Continuous output current		±330	mA
Pd	Power dissipation	T_a=60℃	1000	mW
Topr	Operating temperature		−10～+60	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		6	14	15	V
I_O	Continuous output current				±300	mA
V_{IH}	"H" Input voltage		3	5	V_{CC}	V
V_{IL}	"L" Input voltage			0	0.4	V
T_{OFF}	Input switching interval	It is prohibited to switch the inputs at the same time.	10	300		ms

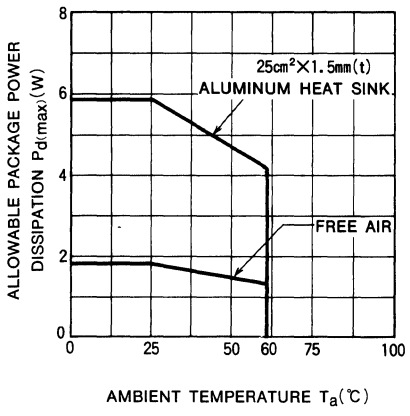
ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=V_{CC}'=20V V_{I1}=V_{I2}=3V	V_O=20V			100	μA
			V_O=0V			−100	
V_{OH}	"H" Output saturation voltage	V_{CC}=V_{CC}'=12V I_{OH}=−300mA	V_{I1}=3V, V_{I2}=0V	9.7	10.2		V
			V_{I1}=0V, V_{I2}=3V				
V_{OL}	"L" Output saturation voltage	V_{CC}=V_{CC}'=12V I_{OL}=300mA	V_{I1}=3V, V_{I2}=0V		0.9	1.4	V
			V_{I1}=0V, V_{I2}=3V				
I_{IH}	"H" Input current	V_{CC}=V_{CC}'=12V	V_{I1}=3V			500	μA
			V_{I2}=3V				
I_{CC}	Supply current	V_{CC}=V_{CC}'=16V	V_{I1}=3V, V_{I2}=0V		7	10	mA
			V_{I1}=0V, V_{I2}=3V				
			V_{I1}=0V, V_{I2}=0V		0		
			V_{I1}=3V, V_{I2}=3V				

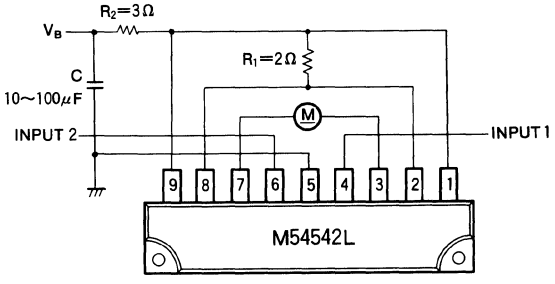
* : A typical value at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



APPLICATION EXAMPLE



Note

1. It is prohibited to switch the both inputs simultaneously. The inputs should be driven separately to avoid high crossover current.
2. The pins 1 , 9 and 2 , 8 are separated and shall be connected externally.

M54543L

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

DESCRIPTION

The M54543L, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for D-C motor control.

FEATURES

- Wide operating voltage range (V_{CC} = 4 ~ 16V)
- TTL, PMOS and CMOS compatible input
- Low output saturation voltage
- Integral diodes for transient suppression
- 1.2A output current
- Braking mode input

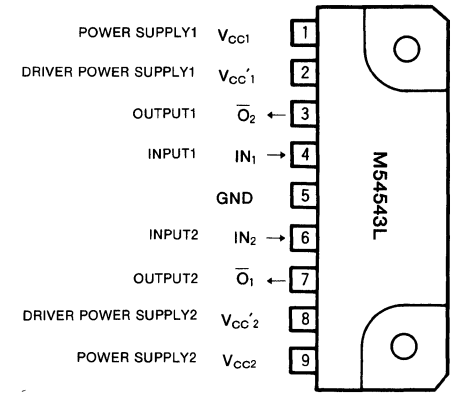
APPLICATION

Audio, video cassette recorder

FUNCTION

The M54543L, full bridge motor driver, has the logic circuitry and non-darlington power drivers for bidirectional control of D-C motors operating at currents up to 1.2A. A braking mode by switching the both inputs high may make easier to control the motor. The both of the separated power supplies for the logic circuitry and the drivers are usable for motor speed control.

PIN CONFIGURATION (TOP VIEW)

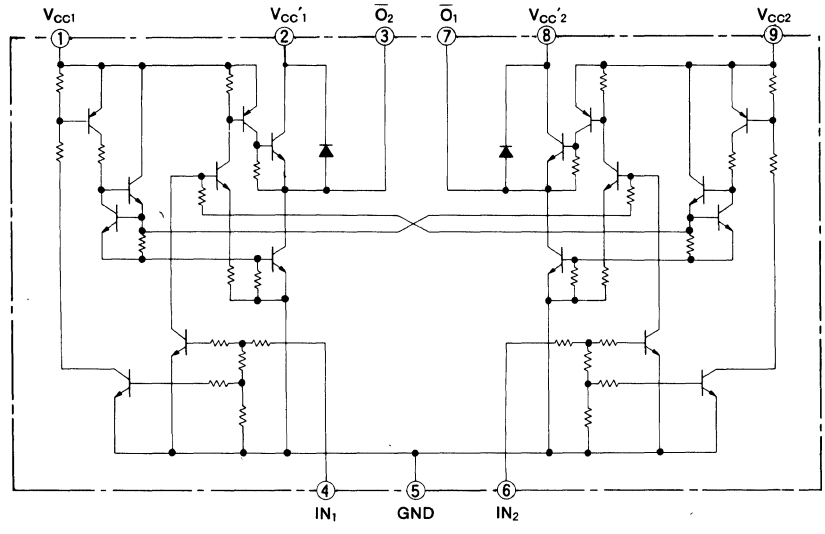


Outline 9P9

LOGIC TRUTH TABLE

INPUT		OUTPUT		NOTE
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	"OFF" state	"OFF" state	Open
H	L	H	L	↻
L	H	L	H	↺
H	H	L	L	Braking

CIRCUIT SCHEMATIC



MITSUBISHI ELECTRIC

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(1)}$	Supply voltage (1)		−0.5～+16	V
$V_{CC(2)}$	Supply voltage (2)	With an external heat sink (3000mm²X1.5mm)	−0.5～+20	V
V_{CC}'	Driver supply voltage		−0.5～+16	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～V_{CC}'+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms. Repetitive cycle 0.2Hz max	±1.2	A
$I_{O(1)}$	Continuous output current (1)		±330	mA
$I_{O(2)}$	Continuous output current (2)	With an external heat sink (3000mm²X1.5mm)	±600	mA
P_d	Power dissipation	T_a=75℃	1.15	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

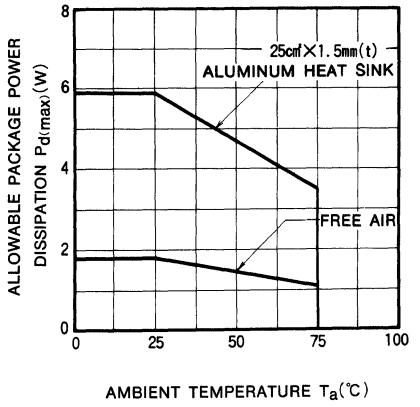
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	15	V
I_O	Continuous output current				±300	mA
V_{IH}	"H" Input voltage		2		V_{CC}	V
V_{IL}	"L" Input voltage		0		0.4	V
t_B	Motor braking interval		10	100		ms

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=V_{CC}'=20V, V_{I1}=V_{I2}=0V	V_O=20V				100	μA
			V_O=0V				−100	
$V_{OH(1)}$	"H" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OH(1)}$=−300mA	10.8			V
				$I_{OH(1)}$=−500mA	10.7			
$V_{OH(2)}$	"H" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OH(2)}$=−300mA	10.8			V
				$I_{OH(2)}$=−500mA	10.7			
$V_{OL(1)}$	"L" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OL(1)}$=300mA			0.5	V
				$I_{OL(1)}$=500mA			0.65	
			V_{I1}=V_{I2}=2V				0.65	
$V_{OL(2)}$	"L" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OL(2)}$=300mA			0.5	V
				$I_{OL(2)}$=500mA			0.65	
			V_{I1}=V_{I2}=2V				0.65	
$I_{IH(1)}$	"H" Input current (1)	V_{CC}=V_{CC}'=12V, V_{I1}=2V, V_{I2}=0V			70		200	μA
$I_{IH(2)}$	"H" Input current (2)	V_{CC}=V_{CC}'=12V, V_{I1}=0V, V_{I2}=2V			70		200	μA
I_{CC}	Supply current	V_{CC}=V_{CC}'=16V	V_{I1}=2V, V_{I2}=0V				40	mA
			V_{I1}=0V, V_{I2}=2V					
			V_{I1}=V_{I2}=2V				60	
			V_{I1}=V_{I2}=0V			0		

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



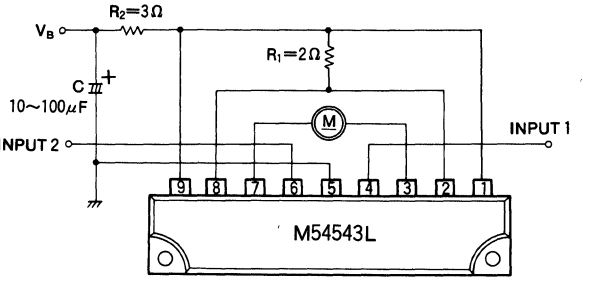
Note

When the V_{CC}' is lower than the V_{CC}, the current will flow from the V_{CC} to the V_{CC}' and may drive the motor.

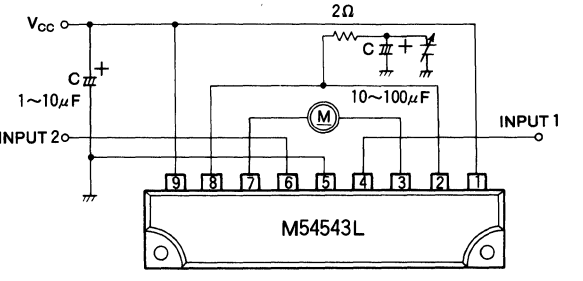
The M54544L may be recommended to have the wider control voltage range of the V_{CC}'.

APPLICATION EXAMPLES

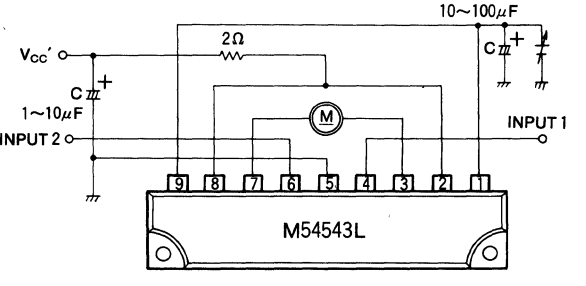
1) Motor speed control by V_{CC} and V_{CC}'



2) Motor speed control by the V_{CC}'



3) Motor speed control by the V_{CC}



M54543AL

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

DESCRIPTION

The M54543AL, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for D-C motor control.

FEATURES

- Wide operating voltage range (V_{CC} = 4 ~16V)
- TTL, PMOS and CMOS compatible input
- Low output saturation voltage
- Integral diodes for transient suppression
- 1.5A output current
- Braking mode input
- Internal thermal shutdown protection

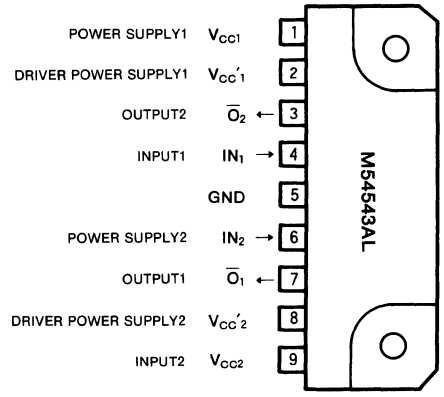
APPLICATION

Audio, video cassette recorder

FUNCTION

The M54543AL, full bridge motor driver, has the logic circuitry and quasi-darlington power drivers for bidirectional control of D-C motors operating at currents up to 1.5A. A braking mode by switching the both inputs high may make easier to control the motor. The both of the separated power supplies for the logic circuitry and the drivers are usable for motor speed control.

PIN CONFIGURATION (TOP VIEW)

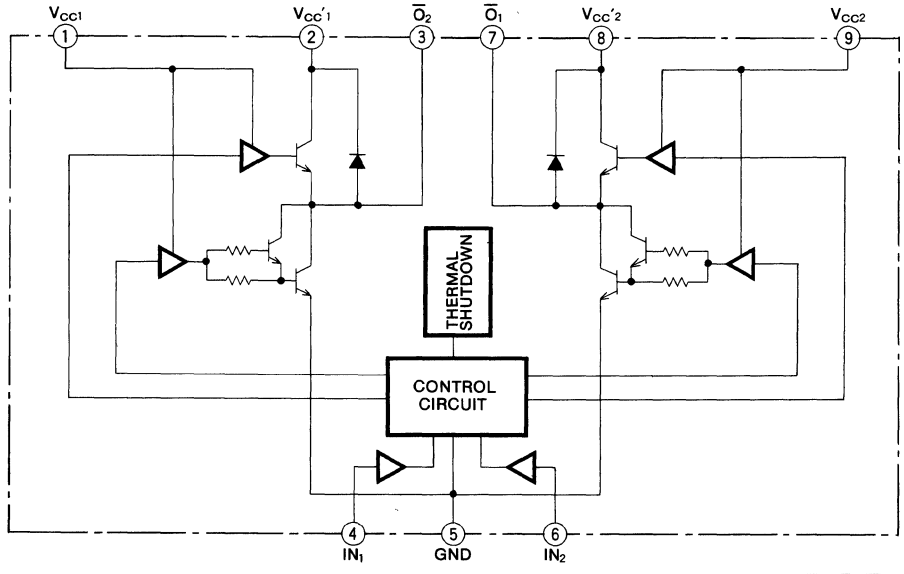


Outline 9P9

LOGIC TRUTH TABLE

INPUT		OUTPUT		NOTE
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	"OFF" state	"OFF" state	Open
H	L	H	L	↻
L	H	L	H	↺
H	H	L	L	Braking

BLOCK DIAGRAM



M54543AL

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(1)}$	Supply voltage (1)		−0.5～+16	V
$V_{CC(2)}$	Supply voltage (2)	With an external heat sink (3000mm²×1.5mm)	−0.5～+20	V
V_{CC}'	Driver supply voltage		−0.5～+16	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～V_{CC}'+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms Repetitive cycle 0.2Hz max	±1.5	A
$I_{O(1)}$	Continuous output current (1)		±330	mA
$I_{O(2)}$	Continuous output current (2)	With an external heat sink (3000mm²×1.5mm)	±600	mA
P_d	Power dissipation	T_a=75℃	1.15	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	15	V
I_O	Continuous output current				±300	mA
V_{IH}	"H" Input voltage		2		V_{CC}	V
V_{IL}	"L" Input voltage		0		0.4	V
t_B	Motor braking interval		10	100		ms
$T_{j(shut)}$	Thermal shutdown temperature	Junction temperature, V_{CC}≧7V		150		℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

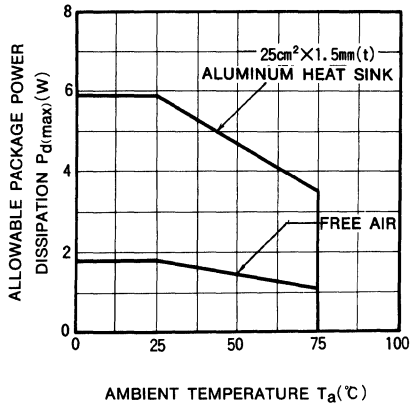
Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=V_{CC}'=20V, V_{I1}=V_{I2}=0V	V_O=20V				100	μA
			V_O=0V				−100	
$V_{OH(1)}$	"H" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OH(1)}$=−200mA	10.8			V
				$I_{OH(1)}$=−500mA	10.7			
$V_{OH(2)}$	"H" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OH(2)}$=−200mA	10.8			V
				$I_{OH(2)}$=−500mA	10.7			
$V_{OL(1)}$	"L" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OL(1)}$=200mA			0.5	V
				$I_{OL(1)}$=500mA			1.35	
			V_{I1}=V_{I2}=2V				1.35	
$V_{OL(2)}$	"L" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OL(2)}$=200mA			0.5	V
				$I_{OL(2)}$=500mA			1.35	
			V_{I1}=V_{I2}=2V				1.35	
$I_{IH(1)}$	"H" Input current (1)	V_{CC}=V_{CC}'=12V, V_{I1}=2V, V_{I2}=0V			50		120	μA
$I_{IH(2)}$	"H" Input current (2)	V_{CC}=V_{CC}'=12V, V_{I1}=0V, V_{I2}=2V			50		120	μA
I_{CC}	Supply current	V_{CC}=V_{CC}'=16V	V_{I1}=2V, V_{I2}=0V				20	mA
			V_{I1}=0V, V_{I2}=2V					
			V_{I1}=V_{I2}=2V				20	
			V_{I1}=V_{I2}=0V				4	

M54543AL

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



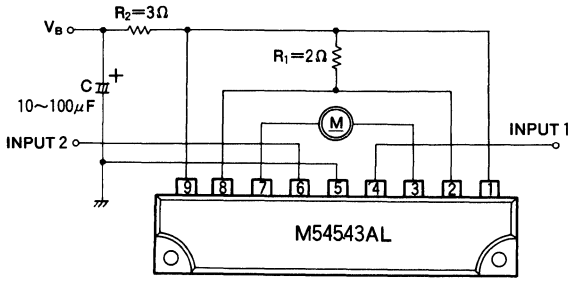
Note

When the V_{CC}' is lower than the V_{CC}, the current will flow from the V_{CC} to the V_{CC}' and may drive the motor.

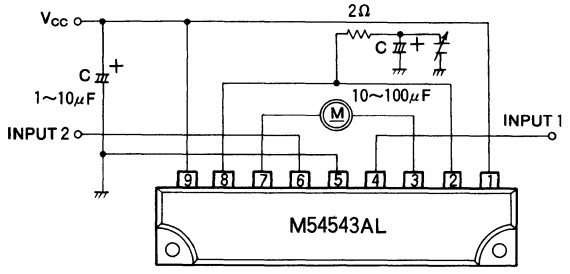
The M54544AL may be recommended to have the wider control voltage range of the V_{CC}'.

APPLICATION EXAMPLES

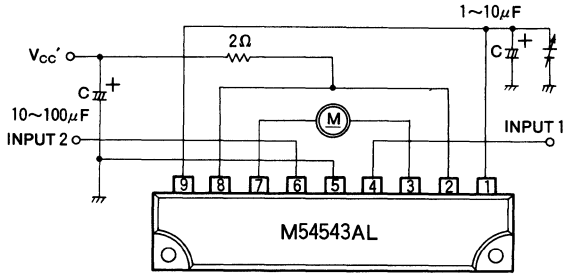
1) Motor speed control by V_{CC} and V_{CC}'



2) Motor speed control by the V_{CC}'



3) Motor speed control by the V_{CC}



M54544L

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

DESCRIPTION

The M54544L, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for D-C motor control.

FEATURES

- Wide operating voltage range (V_{CC}= 4 ~16V)
- TTL, PMOS and CMOS compatible input
- Low output saturation voltage
- Integral diodes for transient suppression
- 1.2A output current
- Braking mode input

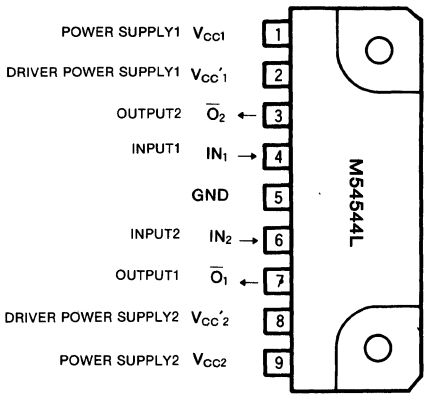
APPLICATION

Audio, video cassette recorders

FUNCTION

The M54544L, full bridge motor driver, has the logic circuitry and non-darlington power drivers for bidirectional control of D-C motors operating at currents up to 1.2A. A braking mode by switching the both inputs high may make easier to control the motor. The both of the separated power supplies for the logic circuitry and the drivers are usable for motor speed control. The power supply for the predriver is connected with the driver power supply to have a wider control range of motor supply voltage.

PIN CONFIGURATION (TOP VIEW)

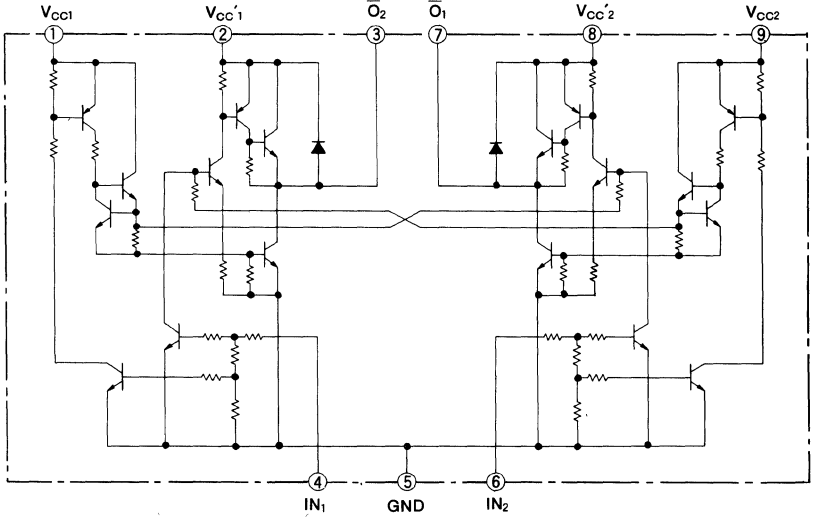


Outline 9P9

LOGIC TRUTH TABLE

Input		Output		Note
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	"OFF" state	"OFF" state	Open
H	L	H	L	↻
L	H	L	H	↺
H	H	L	L	Braking

CIRCUIT SCHEMATIC



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(1)}$	Supply voltage (1)		−0.5～+16	V
$V_{CC(2)}$	Supply voltage (2)	With an external heat sink (3000mm²×1.5mm)	−0.5～+20	V
V_{CC}'	Driver supply voltage		−0.5～+16	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～V_{CC}'+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms. Repetitive cycle 0.2Hz max	±1.2	A
$I_{O(1)}$	Continuous output current (1)		±330	mA
$I_{O(2)}$	Continuous output current (2)	With an external heat sink (3000mm²×1.5mm)	±600	mA
Pd	Power Dissipation	T_a=75℃	1.15	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

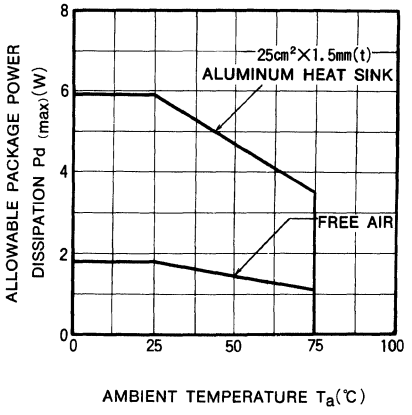
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	15	V
I_O	Continuous output current				±300	mA
V_{IH}	"H" Input voltage		2		V_{CC}	V
V_{IL}	"L" Input voltage		0		0.4	V
t_B	Motor braking interval		10	100		ms

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=V_{CC}'=20V, V_{I1}=V_{I2}=0V		V_O=20V			100	μA
				V_O=0V			−100	
$V_{OH(1)}$	"H" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OH(1)}$=−300mA	10.8			V
				$I_{OH(1)}$=−500mA	10.7			
$V_{OH(2)}$	"H" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I2}=2V	$I_{OH(2)}$=−300mA	10.8			V
				$I_{OH(2)}$=−500mA	10.7			
$V_{OL(1)}$	"L" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OL(1)}$=300mA			0.5	V
				$I_{OL(1)}$=500mA			0.65	
			V_{I1}=V_{I2}=2V				0.65	
$V_{OL(2)}$	"L" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OL(2)}$=300mA			0.5	V
				$I_{OL(2)}$=500mA			0.65	
			V_{I1}=V_{I2}=2V				0.65	
$I_{IH(1)}$	"H" Input current (1)	V_{CC}=V_{CC}'=12V, V_{I1}=2V, V_{I2}=0V			70		200	μA
$I_{IH(2)}$	"H" Input current (2)	V_{CC}=V_{CC}'=12V, V_{I1}=0V, V_{I2}=2V			70		200	μA
I_{CC}	Supply current	V_{CC}=V_{CC}'=16V		V_{I1}=2V, V_{I2}=0V			30	mA
				V_{I1}=0V, V_{I2}=2V				
				V_{I1}=V_{I2}=2V			60	
				V_{I1}=V_{I2}=0V		0		

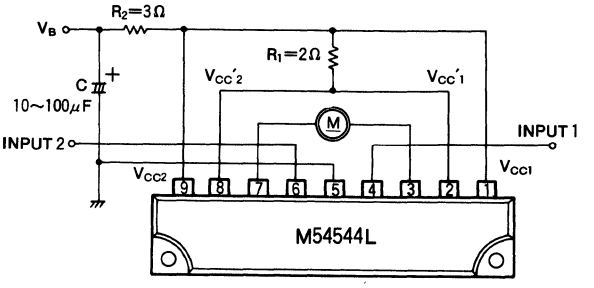
TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

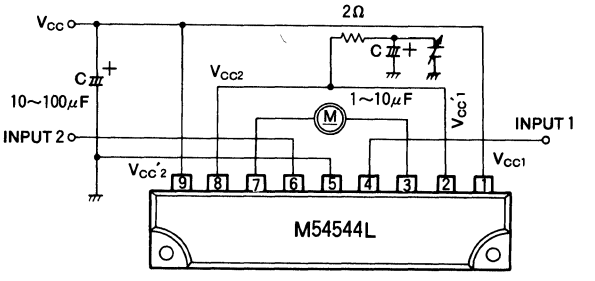


APPLICATION EXAMPLES

1) Motor speed control by V_{CC} and V_{CC}'



2) Motor speed control by the V_{CC}'



M54544AL

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

DESCRIPTION

The M54544AL, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for D-C motor control.

FEATURES

- Wide operating voltage range (V_{CC}= 4 ~16V)
- TTL, PMOS and CMOS compatible input
- Low output saturation voltage
- Integral diodes for transient suppression
- 1.5A output current
- Braking mode input
- Internal thermal shutdown protection

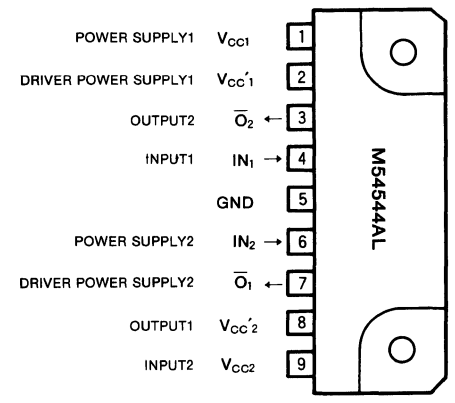
APPLICATION

Audio, video cassette recorders

FUNCTION

The M54544AL, full bridge motor driver, has the logic circuitry and quasi-darlington power drivers for bidirectional control of D-C motors operating at currents up to 1.5A. A braking mode by switching the both inputs high may make easier to control the motor. The both of the separated power supplies for the logic circuitry and the drivers are usable for motor speed control. The power supply for the predriver is connected with the driver power supply to have a wider control range of motor supply voltage.

PIN CONFIGURATION (TOP VIEW)

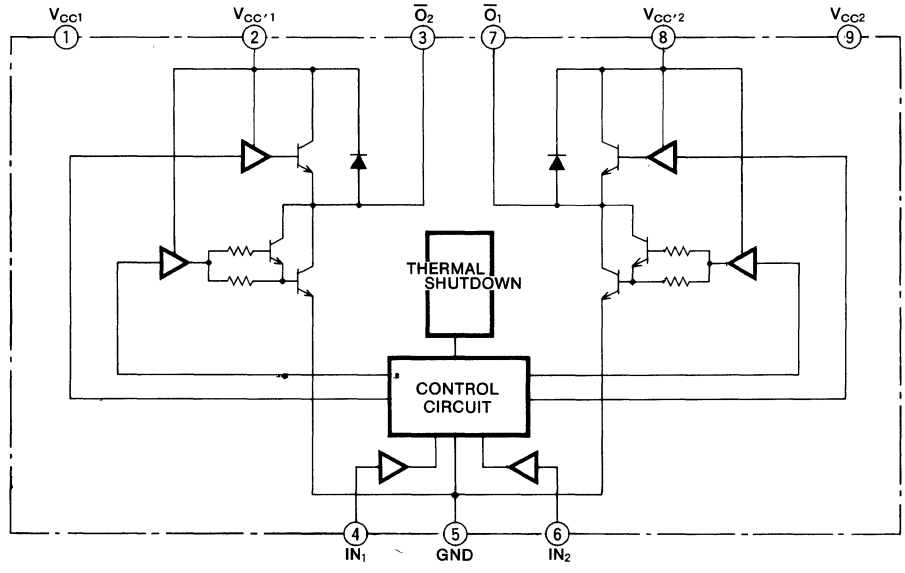


Outline 9P9

LOGIC TRUTH TABLE

Input		Output		Note
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	"OFF" state	"OFF" state	Open
H	L	H	L	↻
L	H	L	H	↺
H	H	L	L	Braking

BLOCK DIAGRAM



M54544AL

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(1)}$	Supply voltage (1)		−0.5～+16	V
$V_{CC(2)}$	Supply voltage (2)	With an external heat sink (3000mm²×1.5mm)	−0.5～+20	V
V_{CC}'	Driver supply voltage		−0.5～+16	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～V_{CC}'+2.5	V
$I_{O(max)}$	Peak output current	Repetitive cycle 0.2Hz max	±1.5	A
$I_{O(1)}$	Continuous output current (1)		±330	mA
$I_{O(2)}$	Continuous output current (2)	With an external heat sink (3000mm²×1.5mm)	±600	mA
Pd	Power Dissipation	T_a=75℃	1.15	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	15	V
I_O	Continuous output current				±300	mA
V_{IH}	"H" Input voltage		2		V_{CC}	V
V_{IL}	"L" Input voltage		0		0.4	V
t_B	Motor braking interval		10	100		ms
$T_{j(shut)}$	Thermal shutdown temperature	junction temperature, V_{CC}≦7V		150		℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

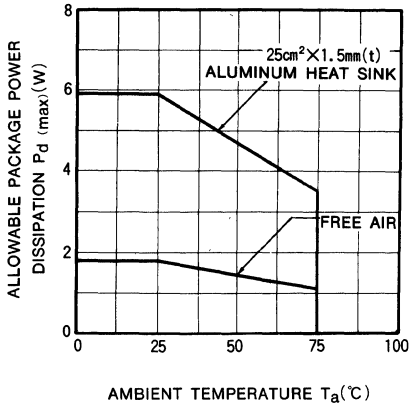
Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=V_{CC}'=20V, V_{I1}=V_{I2}=0V	V_O=20V				100	μA
			V_O=0V				−100	
$V_{OH(1)}$	"H" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OH(1)}$=−200mA	10.8			V
				$I_{OH(1)}$=−500mA	10.7			
$V_{OH(2)}$	"H" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OH(2)}$=−200mA	10.8			V
				$I_{OH(2)}$=−500mA	10.7			
$V_{OL(1)}$	"L" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OL(1)}$=200mA			0.5	V
				$I_{OL(1)}$=500mA			1.35	
			V_{I1}=V_{I2}=2V				1.35	
$V_{OL(2)}$	"L" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OL(2)}$=200mA			0.5	V
				$I_{OL(2)}$=500mA			1.35	
			V_{I1}=V_{I2}=2V				1.35	
$I_{IH(1)}$	"H" Input current (1)	V_{CC}=V_{CC}'=12V, V_{I1}=2V, V_{I2}=0V			50		120	μA
$I_{IH(2)}$	"H" Input current (2)	V_{CC}=V_{CC}'=12V, V_{I1}=0V, V_{I2}=2V			50		120	μA
I_{CC}	Supply current	V_{CC}=V_{CC}'=16V	V_{I1}=2V, V_{I2}=0V				15	mA
			V_{I1}=0V, V_{I2}=2V					
			V_{I1}=V_{I2}=2V				20	
			V_{I1}=V_{I2}=0V				4	

M54544AL

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

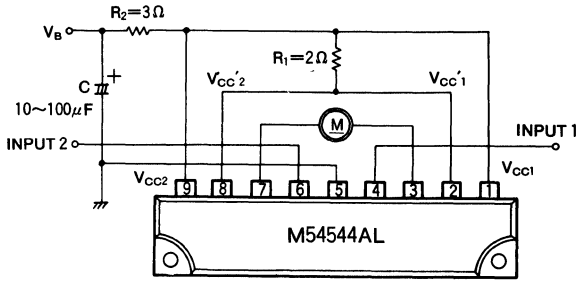
TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

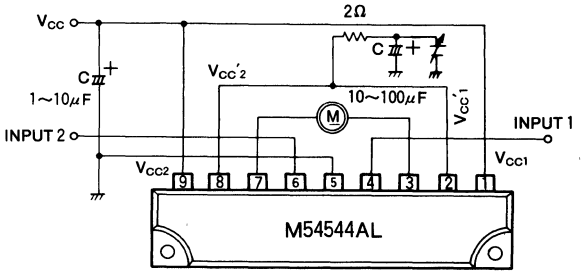


APPLICATION EXAMPLES

1) Motor speed control by V_{CC} and V_{CC}'



2) Motor speed control by the V_{CC}'



M54545L

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

DESCRIPTION

The M54545L, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for D-C motor control.

FEATURES

- Wide operating voltage range (V_{CC} = 3 ~ 16V)
- Low output saturation voltage
- Integral diodes for transient suppression
- 1.2A output current
- Braking mode input
- Low standby current

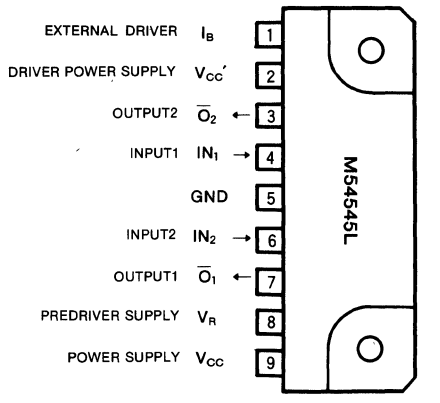
APPLICATION

Audio, video cassette recorder

FUNCTION

The M54545L, full bridge motor driver, has the logic circuitry and the quasi-darlington power driver for bidirectional control of D-C motors operating at currents up to 1.2A. A braking mode by switching the both inputs high may make easier to control the motor. The power supplies for the logic circuitry, the predrivers and the power drivers are separated so that the application circuit with the M54545L can be easily optimized for lower power consumption.

PIN CONFIGURATION (TOP VIEW)

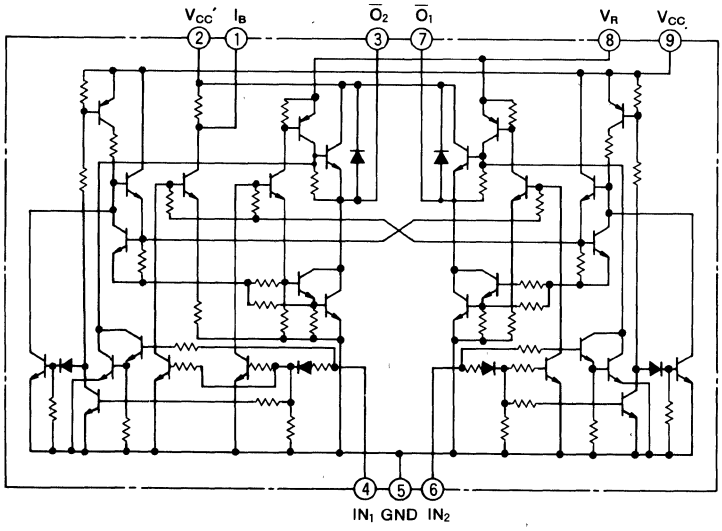


Outline 9P9

LOGIC TRUTH TABLE

Input		Output			Note
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	I_B	
L	L	"OFF" state	"OFF" state	H	Off
H	L	H	L	H	○
L	H	L	H	L	○
H	H	L	L	H	Braking

CIRCUIT SCHEMATIC



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+16	V
V_R	Predriver supply voltage		−0.5～+16	V
V_{CC}'	Driver supply voltage		−0.5～+16	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～V_{CC}'+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms V_{CC}≧5V : Repetitive cycle 0.2Hz max	±1.2	A
I_O	Continuous output current		±330	mA
Pd	Power dissipation	T_a=75℃	1.15	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

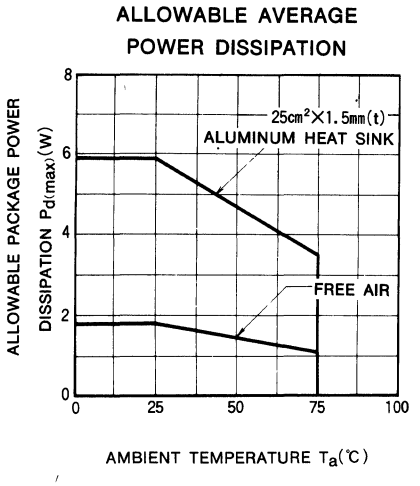
RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3	12	15	V
I_O	Continuous output current				±200	mA
V_{IH}	"H" Input voltage		3		V_{CC}	V
V_{IL}	"L" Input voltage		0		0.4	V
t_B	Motor braking interval		10	100		ms

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

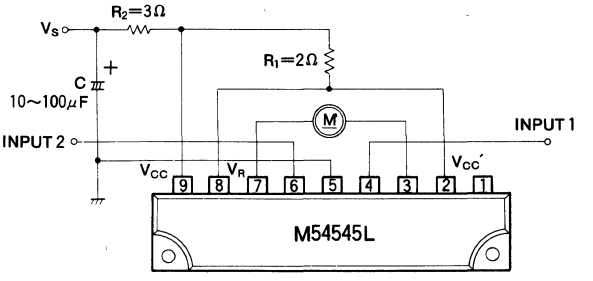
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=V_R=V_{CC}'=16V	V_O=16V			100	μA
		V_{I1}=V_{I2}=0V	V_O=0V			−100	
$V_{OH(1)}$	"H" Output saturation voltage (1)	V_{CC}=V_R=V_{CC}'=12V	V_{I1}=3V, V_{I2}=0V	10.8			V
$V_{OH(2)}$	"H" Output saturation voltage (2)	I_{OH}=−200mA	V_{I1}=0V, V_{I2}=3V	10.8			V
$V_{OL(1)}$	"L" Output saturation voltage (1)	V_{CC}=V_R=V_{CC}'=12V	V_{I1}=0V, V_{I2}=3V			0.4	V
		$I_{OL(1)}$=200mA	V_{I1}=3V, V_{I2}=3V				
$V_{OL(2)}$	"L" Output saturation voltage (2)	V_{CC}=V_R=V_{CC}'=12V	V_{I1}=3V, V_{I2}=0V			0.4	V
		$I_{OL(2)}$=200mA	V_{I1}=3V, V_{I2}=3V				
$I_{IH(1)}$	"H" Input current (1)	V_{CC}=V_R=V_{CC}'=12V	V_{I1}=3V, V_{I2}=0V			700	μA
$I_{IH(2)}$	"H" Input current (2)	V_{CC}=V_R=V_{CC}'=12V	V_{I1}=0V, V_{I2}=3V			700	μA
I_{CC}	Supply current	V_{CC}=V_R=V_{CC}'=12V	V_{I1}=0V, V_{I2}=0V			5	mA
			V_{I1}=3V, V_{I2}=0V			10	
			V_{I1}=0V, V_{I2}=3V				
I_B	I_B Output current	V_{CC}=V_R=V_{CC}'=12V, V_{IB}=12V, V_{I1}=0V, V_{I2}=3V		1.0		15.0	mA

TYPICAL CHARACTERISTICS

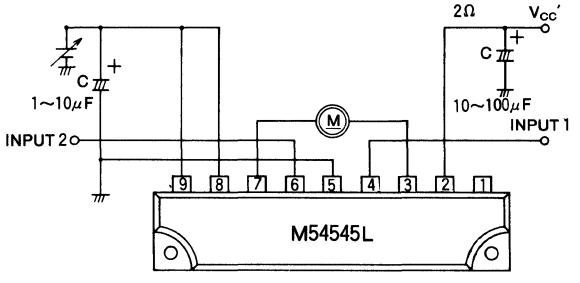


APPLICATION EXAMPLES

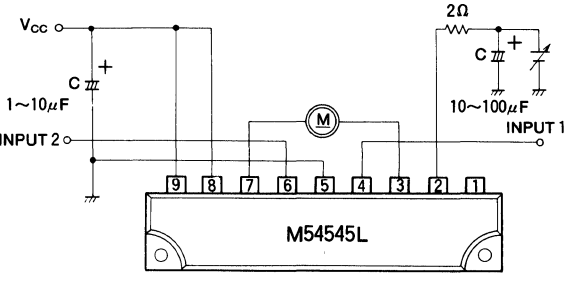
1) Motor speed control by V_{CC} and V_{CC}'



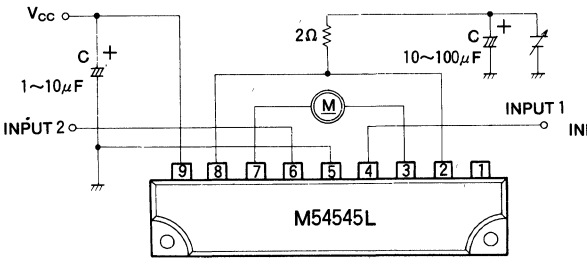
2) Motor speed control by the V_R and V_{CC}



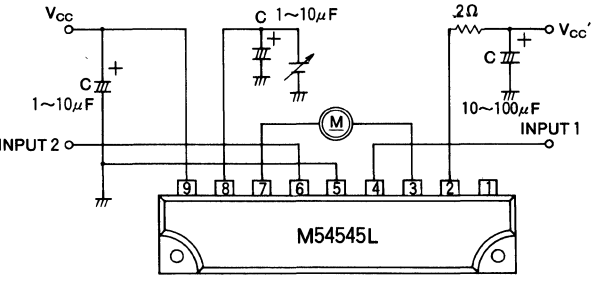
3) Motor speed control by the V_{CC}'



4) Motor speed control by the V_R and V_{CC}'



5) Motor speed control by the V_R



M54546L

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

DESCRIPTION

The M54546L, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for D-C motor control.

FEATURES

- Wide operating voltage range (V_{CC}= 4 ~16V)
- TTL, PMOS and CMOS compatible input
- Low output saturation voltage
- Integral diodes for transient suppression
- Small single inline package
- Braking mode input

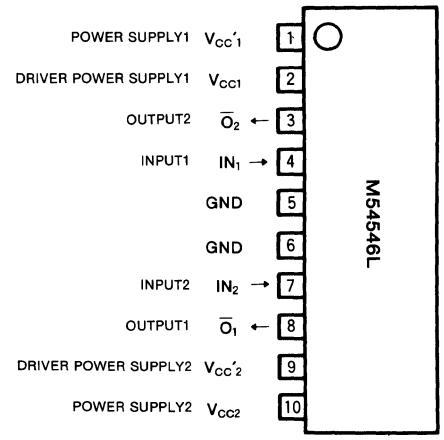
APPLICATION

Audio, video cassette recorder

FUNCTION

The M54546L, full bridge motor driver, has the logic circuitry and non-darlington power drivers for bidirectional control of D-C motors operating at currents up to 700mA. A braking mode by switching the both inputs high may make easier to control the motor. The both of the separated power supplies for the logic circuitry and the drivers are usable for motor speed control. The power supply of the predriver is connected with the driver power supply to have a wider control range of motor supply voltage.

PIN CONFIGURATION (TOP VIEW)

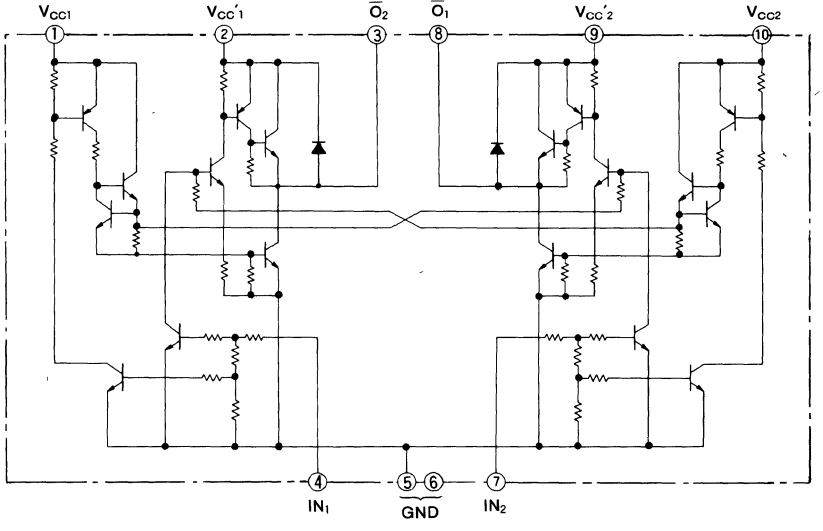


Outline 10P5

LOGIC TRUTH TABLE

INPUT		OUTPUT		NOTE
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	"OFF" state	"OFF" state	Open
H	L	H	L	○
L	H	L	H	○
H	H	L	L	Braking

CIRCUIT SCHEMATIC



BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+16	V
V_{CC}'	Driver supply voltage		−0.5～+16	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～V_{CC}'+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms: Repetitive cycle 0.2Hz max	±700	mA
I_O	Continuous output current		±150	mA
P_d	Power dissipation	T_a=75℃	600	mW
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

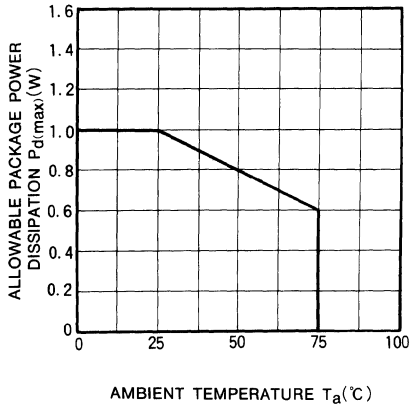
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	15	V
I_O	Continuous output current				±100	mA
V_{IH}	"H" Input voltage		2		V_{CC}	V
V_{IL}	"L" Input voltage		0		0.4	V
t_B	Motor braking interval		10	100		ms

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=V_{CC}'=20V, V_{I1}=V_{I2}=2V	V_O=20V				100	μA
			V_O=0V				−100	
$V_{OH(1)}$	"H" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OH(1)}$=−50mA	11.0			V
				$I_{OH(1)}$=−100mA	10.9			
$V_{OH(2)}$	"H" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OH(2)}$=−50mA	11.0			V
				$I_{OH(2)}$=−100mA	10.9			
$V_{OL(1)}$	"L" Output saturation voltage (1)	V_{CC}=V_{CC}'=12V	V_{I1}=0V, V_{I2}=2V	$I_{OL(1)}$=50mA			0.3	V
				$I_{OL(1)}$=100mA			0.35	
			V_{I1}=V_{I2}=2V				0.35	
$V_{OL(2)}$	"L" Output saturation voltage (2)	V_{CC}=V_{CC}'=12V	V_{I1}=2V, V_{I2}=0V	$I_{OL(2)}$=50mA			0.3	V
				$I_{OL(2)}$=100mA			0.35	
			V_{I1}=V_{I2}=2V				0.35	
$I_{IH(1)}$	"H" Input current (1)	V_{CC}=V_{CC}'=12V, V_{I1}=2V, V_{I2}=0V			70		200	μA
$I_{IH(2)}$	"H" Input current (2)	V_{CC}=V_{CC}'=12V, V_{I1}=0V, V_{I2}=2V			70		200	μA
I_{CC}	Supply current	V_{CC}=V_{CC}'=16V	V_{I1}=2V, V_{I2}=0V				30	mA
			V_{I1}=0V, V_{I2}=2V					
			V_{I1}=V_{I2}=2V				60	
			V_{I1}=V_{I2}=0V			0		

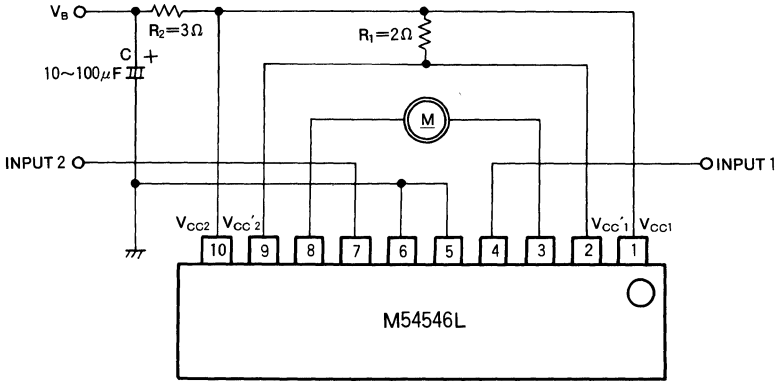
TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

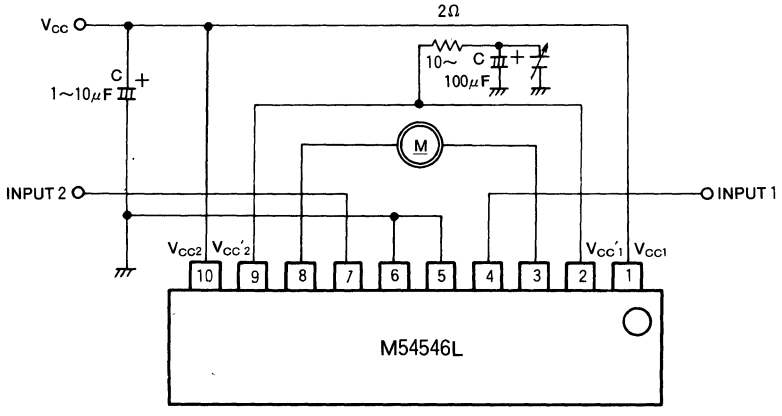


APPLICATION EXAMPLES

1) Motor speed control by V_{CC} and V_{CC}'



2) Motor speed control by the V_{CC}'



M54547P

BI-DIRECTIONAL MOTOR DRIVER WITH OP AMP AND TRANSISTOR ARRAY

DESCRIPTION

The M54547P, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver and dual general purpose NPN darlington pairs.

FEATURES

- 600mA output current
- Braking mode input
- Integral operational amplifier at direction control input
- Output transient suppression

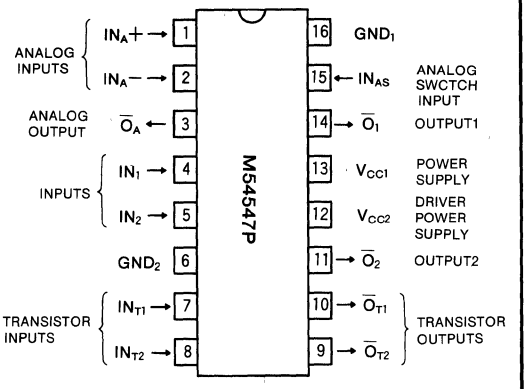
APPLICATION

Audio, video cassette recorder

FUNCTION

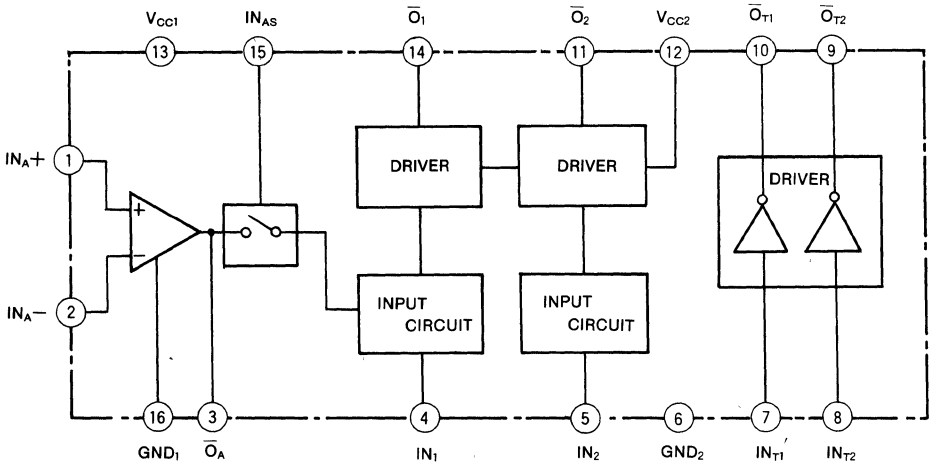
The M54547P, full bridge motor driver, has the logic circuitry and darlington power drivers for bidirectional control of D-C motors operating at currents up to 600mA. The operational amplifier is connected to the direction control input through an analog switch controlled by pin 15 input. By switching the IN_{AS} input high and the IN_1 input low, the output of the amplifier appears at the output $\overline{O}_1$ so that the voltage across the bridge output is altered linearly by the amplifier input. The internal NPN darlington pairs are capable of sinking 300mA and will withstand 20V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

BI-DIRECTIONAL MOTOR DRIVER WITH OP AMP AND TRANSISTOR ARRAY

LOGIC TRUTH TABLE

Input			Output		Note
IN_{AS}	IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	L	H	H	Braking
L	L	H	H	L	↻
L	H	L	L	H	↻
L	H	H	L	L	Braking
H	L	L	A*	H	Analog ↻
H	L	H	A*	L	Analog ↻
H	H	L	L	H	↻
H	H	H	L	L	Braking

A* : The output voltage is controlled by the amplifier output.

ABSOLUTE MAXIMUM RATINGS (T_a=25℃,unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage		−0.5～+16	V
V_{CC2}	Driver supply voltage		−0.5～+16	V
V_I,V_{IAS}	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～V_{CC2}+2.5V	V
I_{OP}	Peak output current	t_{op}=10ms : Repetitive cycle 0.2Hz max	±600	mA
I_O	Continuous output current		±150	mA
V_{CEO}	Collector-emitter applied voltage(transistor array)		20	V
I_C	Collector current(transistor array)		300	mA
V_I	Input voltage(Transistor array)		10	V
P_d	Power dissipation	T_a=25℃	1.47	W
		T_a=60℃	1.06	
Topr	Operating temperature		−10～+60	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC1}	Supply voltage		4	12	15	V
I_O	Continuous output current				±100	mA
V_{IH}	Input voltage(motor driver)		3		V_{CC}	V
V_{IL}	(IN_1, IN_2, IN_{AS})		0		0.6	V
t_B	Motor braking interval		10	100		ms
V_{IH}	Transistor array input voltage		4		10	V
V_{IL}	(IN_{T1}, IN_{T2})		0		0.6	V

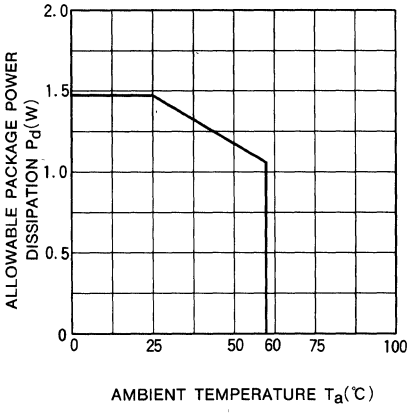
BI-DIRECTIONAL MOTOR DRIVER WITH OP AMP AND TRANSISTOR ARRAY

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

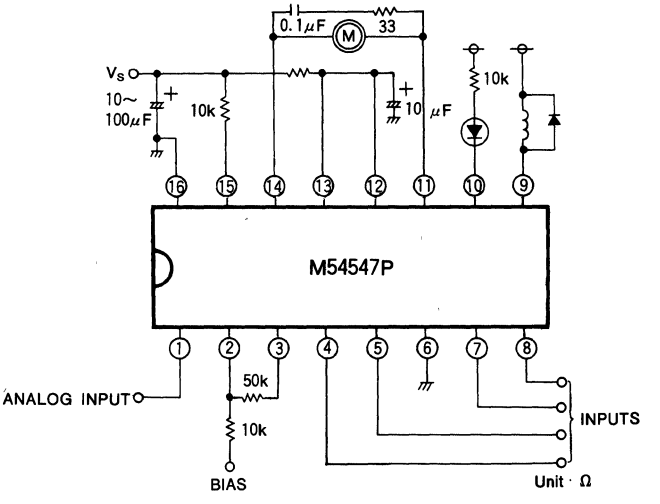
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$I_{O(leak)}$	Output leakage current($\overline{O_1}$, $\overline{O_2}$)	$V_{CC1}=V_{CC2}=16V$	$V_O=0V$			±100	μA
		$V_{IN1}=V_{IN2}=V_{IAS}=0V$	$V_O=16V$				
V_{OH}	"H"Output saturation voltage($\overline{O_1}$, $\overline{O_2}$)	$V_{CC1}=V_{CC2}=12V$	$V_{IN1}=0V$, $V_{IN2}=3V$	10.3			V
		$I_O=-150mA$	$V_{IN1}=3V$, $V_{IN2}=0V$				
V_{OL}	"L"Output saturation voltage($\overline{O_1}$, $\overline{O_2}$)	$V_{CC1}=V_{CC2}=12V$	$V_{IN1}=0V$, $V_{IN2}=3V$			1.2	V
		$I_O=150mA$	$V_{IN1}=3V$, $V_{IN2}=0V$				
I_I	Input current(IN_1, IN_2, IN_{AS})	$V_{CC1}=12V$, $V_I=3V$				0.3	mA
$I_{O(leak)}$	Output leakage current($\overline{O_{T1}}$, $\overline{O_{T2}}$)	$V_O=30V$, $V_I=0.6V$				100	μA
V_{OC}	"L"Output saturation voltage	$V_I=4V$	$I_C=100mA$			1.3	V
			$I_C=200mA$			1.5	
I_I	Input current	$V_I=4V$				0.8	mA
A_O	OP Amp open-loop-gain			40			dB
I_{CC1}	Supply current	$V_{CC1}=12V$, $V_{IN1}=V_{IN2}=V_{IAS}=3V$				6	mA

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M54548L

BI-DIRECTIONAL MOTOR DRIVER WITH MOTOR SPEED CONTROL

DESCRIPTION

The M54548L, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for use in a D-C motor control circuit. The internal operational amplifier is capable for controlling the voltage across the bridge outputs.

FEATURES

- Wide operating voltage range
- NMOS and CMOS compatible input
- 1.2A output current
- Integral operational amplifier for output source voltage
- Intergral diodes for transient suppression
- Braking mode input

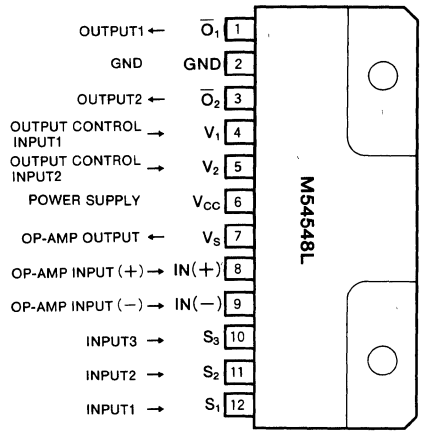
APPLICATION

Audio, video cassette recorder

FUNCTION

The M54548L, full bridge motor driver, has the logic circuitry and the quasi-darlington power driver for bidirectional control of D-C motors operating at current up to 1.2A. The inputs, S_1, S_2 and S_3, are capable to control the bridge output polarity and also to select the supply voltage of the predriver from the voltages drived by V_1, V_2 or the output of the operational amplifier.

PIN CONFIGURATION (TOP VIEW)

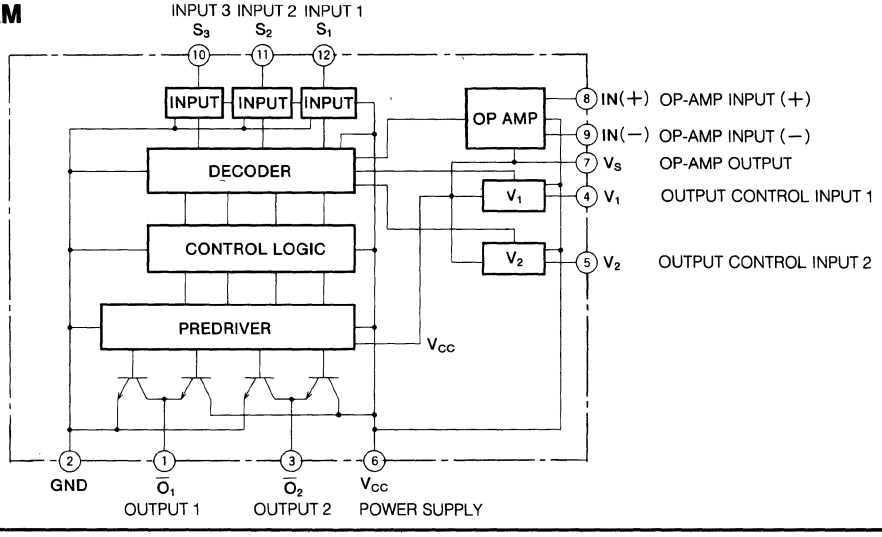


Outline 12P9

LOGIC TRUTH TABLE

Input			Output		Driver power supply	Note
S_1	S_2	S_3	$\overline{O}_1$	$\overline{O}_2$		
L	L	L	"OFF" state	"OFF" state	—	STOP
L	L	H	H	L	OP AMP OUTPUT	PLAY(+)
L	H	L	L	H	OP AMP OUTPUT	PLAY(−)
L	H	H	H	L	V_2	FF(2)
H	L	L	L	H	V_2	REW(2)
H	L	H	H	L	V_1	FF(1)
H	H	L	L	H	V_1	REW(1)
H	H	H	L	L	V_S	BRAKING

BLOCK DIAGRAM



BI-DIRECTIONAL MOTOR DRIVER MITH MOTOR SPEED CONTROL

ABSOLUTE MAXIMUM RATINGS (T_a =25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With an external heat sink (3000mm²X1.5mm^t)	−0.5～+18	V
V_I	Input voltage	4 Pin, 5 Pin	−0.5～+14or V_{CC}	V
			−0.5～V_{CC}	
V_O	Output voltage		−0.5～V_{CC}+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms; Repetitive cycle 0.2Hz max	±1.2	A
$I_{O(1)}$	Continuous output current (1)		±300	mA
$I_{O(2)}$	Continuous output current (2)	With an external heat sink (3000mm²X1.5mm^t)	±600	mA
P_d	Power dissipation	T_a =75℃	1.6	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

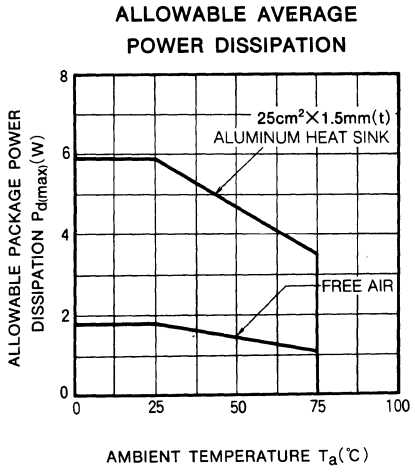
RECOMMENDED OPERATING CONDITIONS (T_a =25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	16	V
I_O	Continuous output current				±200	mA
V_{IH}	"H" Input voltage		3			V
V_{IL}	"L" Input voltage				1	V
t_S	Motor braking interval		10	100		ms

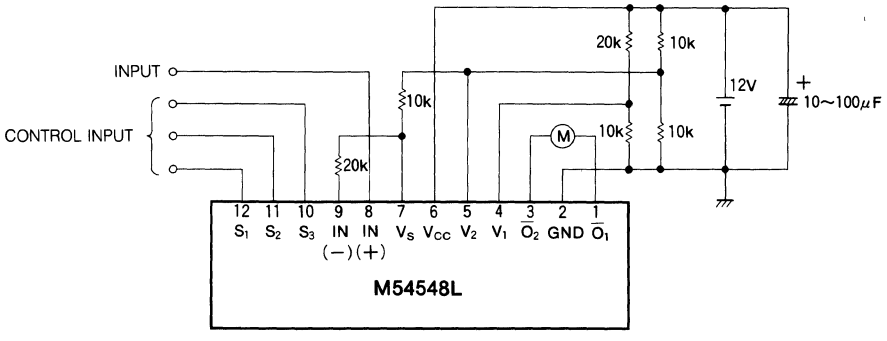
ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{S1}=0V, V_{S2}=0V, V_{S3}=0V		V_O=0V, V_{CC}=V_S=20V			−100	μA
				V_O=14V, V_{CC}=V_S=14V			+100	
$V_{OH(1)}$	"H" Output saturation voltage (1)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S2}=0V, V_{S3}=3V	I_{OH}=−200mA	13			V
				I_{OH}=−500mA	12.8			
$V_{OH(2)}$	"H" Output saturation voltage (2)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S3}=0V, V_{S2}=3V	I_{OH}=−200mA	13			V
				I_{OH}=−500mA	12.8			
$V_{OL(1)}$	"L" Output saturation voltage (1)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S3}=0V, V_{S2}=3V	I_{OL}=200mA			0.5	V
				I_{OL}=500mA			1.4	
$V_{OL(2)}$	"L" Output saturation voltage (2)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S2}=0V, V_{S3}=3V	I_{OL}=200mA			0.5	V
				I_{OL}=500mA			1.4	
I_{IH}	"H" Input current	V_{CC}=16V, V_{IS}=3V (S_1, S_2, S_3)					10	μA
I_{IL}	"L" Input current	V_{CC}=16V, V_{IS}=0V (S_1, S_2, S_3)					−20	μA
I_{CC}	Supply current	V_{CC}=16V, V_{S1}=V_{S2}=V_{S3}=3V					30	mA
A	Op amp open-loop-gain				50			dB

TYPICAL CHARACTERISTICS



APPLICATION EXAMPLE



Unit Ω

M54548AL

BI-DIRECTIONAL MOTOR DRIVER WITH MOTOR SPEED CONTROL

DESCRIPTION

The M54548AL, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for use in a D-C motor control circuit. The internal operational amplifier is capable for controlling the voltage across the bridge outputs.

FEATURES

- Wide operating voltage range
- NMOS and CMOS compatible input
- 1.2A output current
- Integral operational amplifier for output source voltage
- Intergral diodes for transient suppression
- Braking mode input
- 12pin shrink single inline package with heat shink

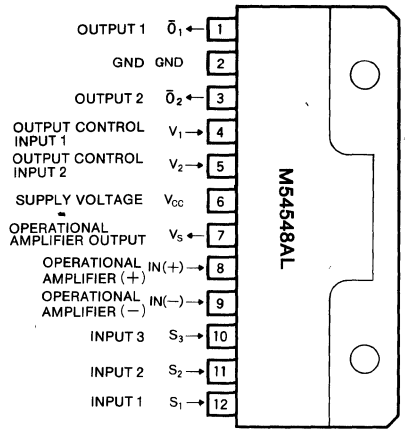
APPLICATION

Audio, video cassette recorder

FUNCTION

The M54548AL, full bridge motor driver, has the logic circuitry and the quasi-darlington power driver for bidirectional control of D-C motors operating at current up to 1.2A. The inputs, S_1, S_2 and S_3, are capable to control the bridge output polarity and also to select the supply voltage of the predriver from the voltages drived by V_1, V_2 or the output of the operational amplifier.

PIN CONFIGURATION (TOP VIEW)

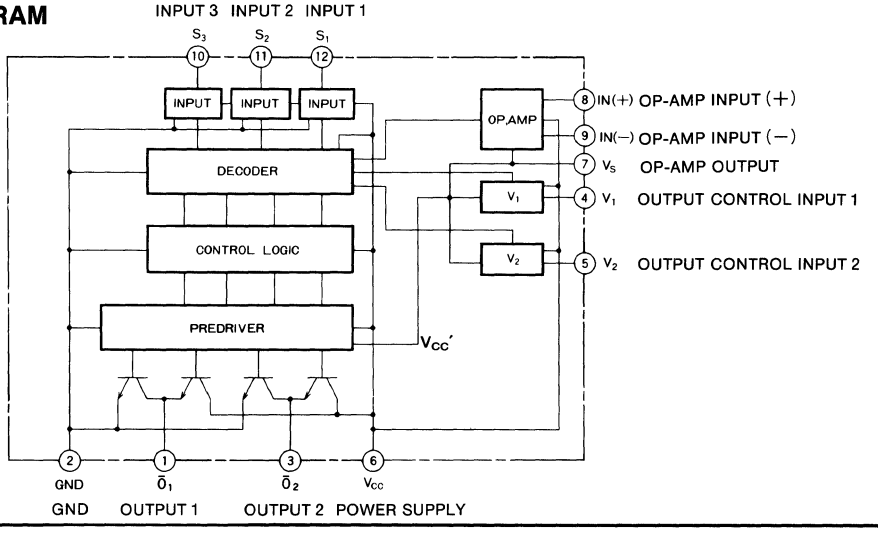


Outline 12P9B

LOGIC TRUTH TABLE

Inputs			Output		Driver power supply	Note
S_1	S_2	S_3	$\bar{O}_1$	$\bar{O}_2$	(V_{CC}')	
L	L	L	"OFF" state	"OFF" state	—	STOP
L	L	H	H	L	OP-AMP OUTPUT	PLAY(+)
L	H	L	L	H	OP-AMP OUTPUT	PLAY(−)
L	H	H	H	L	V_2	FF(2)
H	L	L	L	H	V_2	REW(2)
H	L	H	H	L	V_1	FF(1)
H	H	L	L	H	V_1	REW(1)
H	H	H	L	L	V_S	BRAKING

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

BI-DIRECTIONAL MOTOR DRIVER WITH MOTOR SPEED CONTROL

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With external heat sink (3000mm²×1.5mm^t)	−0.5～+18	V
V_I	Input voltage	4Pin, 5Pin	−0.5～+14 or V_{CC}	V
		Other input pins	−0.5～V_{CC}	
V_O	Output voltage		−0.5～ V_{CC} +2.5	V
$I_{O(max)}$	Allowable motor charge current	t_{op} = 10ms; Repetitive cycle 0.2 Hz max	±1.2	A
$I_{O(1)}$	Continuous output current (1)		±300	mA
$I_{O(2)}$	Continuous output current (2)	With an external heat sink (3000mm²×1.5mm^t)	±600	mA
P_d	Power dissipation	T_a =75℃	1.1	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−25℃, unless otherwise noted)

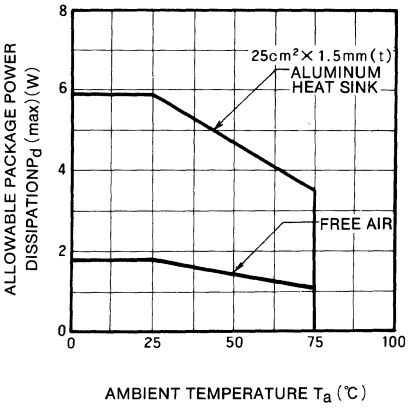
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	16	V
I_O	Output current				±200	mA
V_{IH}	High-level input voltage		3			V
V_{IL}	Low-level input voltage				1	V
t_B	Motor braking interval		10	100		ms

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

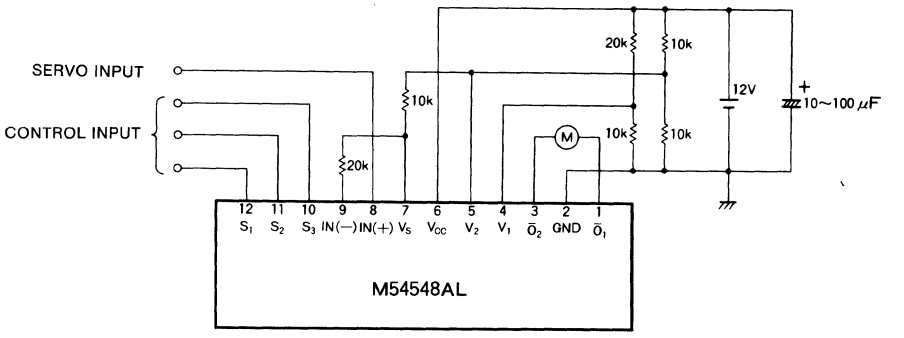
Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{S1}=0V, V_{S2}=0V, V_{S3}=0V		V_O=0V, V_{CC}=V_S=20V			−100	μA
				V_O=14V, V_{CC}=V_S=14V			+100	
$V_{OH(1)}$	High-level output saturation voltage (1)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S2}=0V, V_{S3}=3V	I_{OH}=−200mA	13			V
				I_{OH}=−500mA	12.8			
$V_{OH(2)}$	High-level output saturation voltage (2)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S3}=0V, V_{S2}=3V	I_{OH}=−200mA	13			V
				I_{OH}=−500mA	12.8			
$V_{OL(1)}$	Low-level output saturation voltage (1)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S3}=0V, V_{S2}=3V	I_{OL}=200mA			0.5	V
				I_{OL}=500mA			1.4	
$V_{OL(2)}$	Low-level output saturation voltage (2)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S2}=0V, V_{S3}=3V	I_{OL}=200mA			0.5	V
				I_{OL}=500mA			1.4	
I_{IH}	High-level input current	V_{CC}=16V, V_{IS}=3V (S_1, S_2, S_3)					10	μA
I_{IL}	Low-level input current	V_{CC}=16V, V_{IS}=0V (S_1, S_2, S_3)					−20	μA
I_{CC}	Supply current	V_{CC}=16V, V_{S1}=V_{S2}=V_{S3}=3V					30	mA
A	Op-amp open loop gain				50			dB

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



APPLICATION EXAMPLE



Unit : Ω

M54549L

DUAL BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

DESCRIPTION

The M54549L, BI-DIRECTIONAL MOTOR DRIVER, consists of the two full bridge power designed for use in are two D-C motors control circuit.

FEATURES

- Two separated full bridge driver (only one circuit can be switched by the Se input)
- Wide operating voltage range (V_{CC}=4~16V)
- TTL, PMOS, CMOS outputs, capable of direct drive
- Low output saturation voltage
- Built-in clamp diode
- Large output drive current ($I_{O(max)}$=±2A)
- Braking mode input
- Internal thermal shutdown protection

APPLICATION

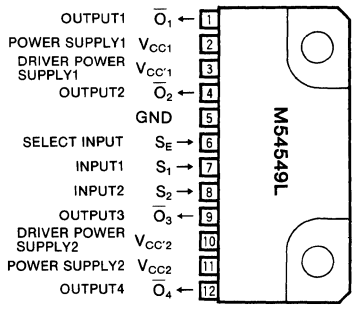
Audio tape-deck player, radio/cassette player, VTR, Home-use equipment

FUNCTION

The M54549L, two-full bridge motor driver, has the logic circuitry and the quasi-darlington power driver for bi-directional control of two D-C motors operating at current up to 2.0A.

The input S_E selects one of the bridges and S_1, S_2 determine the output polarity.

PIN CONFIGURATION (TOP VIEW)

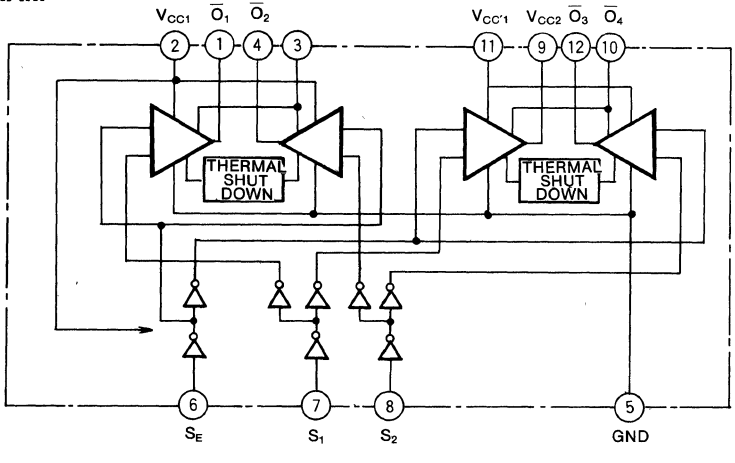


Outline 12P9

LOGIC TRUTH TABLE

Input			Output				Note	
S_E	S_1	S_2	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	Output $\overline{O}_1$, $\overline{O}_2$	Output $\overline{O}_3$, $\overline{O}_4$
0	0	0	OFF	OFF	OFF	OFF	OPen	Open
0	1	0	1	0	OFF	OFF	↺	Open
0	0	1	0	1	OFF	OFF	↺	Open
0	1	1	0	0	OFF	OFF	Braking	Open
1	0	0	OFF	OFF	OFF	OFF	Open	Open
1	1	0	OFF	OFF	1	0	Open	↺
1	0	1	OFF	OFF	0	1	Open	↺
1	1	1	OFF	OFF	0	0	Open	Braking

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(1)}$	Supply voltage (1)		−0.5～+18	V
$V_{CC(2)}$	Supply voltage (2)	With an external sink (3000mm²×1.5mm)	−0.5～+18	V
$V_{CC'}$	Driver supply voltage		−0.5～+18	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−2～$V_{CC'}$+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms, retitive cycle 0.2Hz max	±2.0	A
$I_{O(1)}$	Continuous output current (1)		±330	mA
$I_{O(2)}$	Continuous output current (2)	With an external sink (3000mm²×1.5mm)	±600	mA
P_d	Power dissipation	T_a=75℃	1.6	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

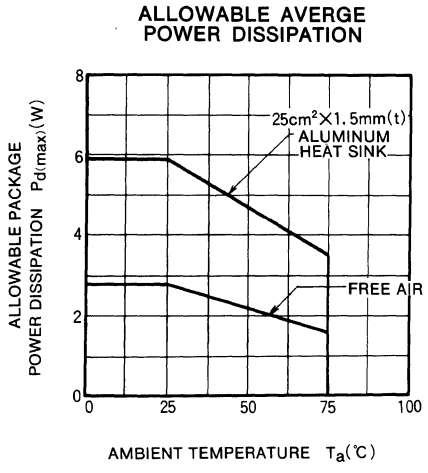
RECOMMNDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	16	V
I_O	Output current				±300	mA
V_{IH}	High-level Input voltage	Input S_1, S_2, S_E	2		V_{CC}	V
V_{IL}	Low-level Input voltage	Input S_1, S_2, S_E	0		0.4	V
t_S	Motor braking interval		10	100		ms
$t_{j(shut)}$	Thermal shut down temperature	V_{CC}≧7V		150		℃

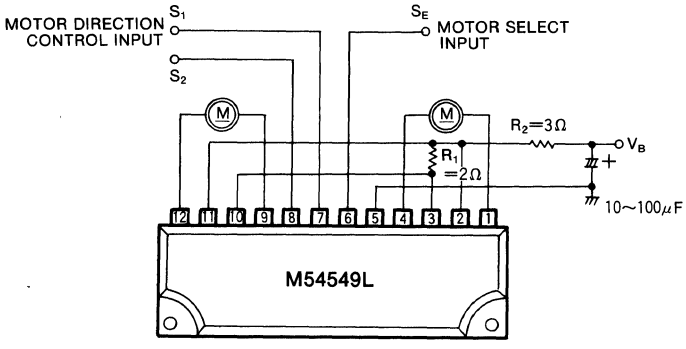
ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$I_{O(leak)}$	Output leakage	V_{CC}=$V_{CC'}$=18V, V_{S1}=V_{S2}=0V, V_{SE}=0V or 2V	V_O=18V			100	μA
			V_O=0V			−100	
V_{OH}	High-level output voltage	V_{CC}=$V_{CC'}$=12V	$I_{OH(1)}$=−200mA	10.8			V
			$I_{OH(1)}$=−500mA	10.7			
V_{OL}	Low-level output voltage	V_{CC}=$V_{CC'}$=12V	I_{OL}=200mA			0.5	V
			$I_{OL(1)}$=500mA			1.35	
I_{IH}	High-level input current	V_{CC}=$V_{CC'}$=12V, V_I=2V		50		120	μA
I_{CC}	Supply current	V_{CC}=V_{CC}=$V_{CC'}$=12V	V_{SE}=0V, V_{S1}=V_{S2}=0V			10	mA
			V_{SE}=0V, V_{S1}=V_{S2}=0V				
			V_{SE}=0V, V_{S1}=0V, V_{S2}=2V			20	

TYPICAL CHARACTERTICS



APPLICATION EXAMPLE



M54549AL

DUAL BI-DIRECTIONAL MOTER DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

DESCRIPTION

The M54549AL, BI-DIRECTIONAL MOTOR DRIVER, consists of the two full bridge power designed for use in are two D-C motors control circuit.

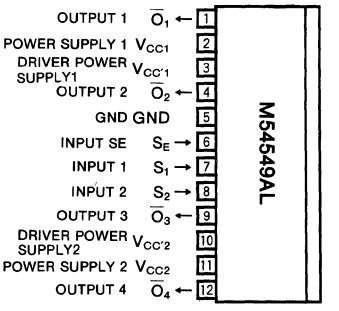
FEATURES

- Two separated full-bridge drivers (only one circuit can be switched by the Se input)
- Wide operating voltage range (V_{CC}=4~16V)
- TTL, PMOS, CMOS outputs, capable of direct drive
- Low output saturation voltage
- Built-in clamp diode
- Large drive current ($I_{O(max)}$=±1.2A)
- Braking mode input
- Internal thermal shutdown protection

APPLICATION

Audio tape-deck player, radio cassette player, VTR, Home-use equipment

PIN CONFIGURATION (TOP VIEW)



Outline 12P5

FUNCTION

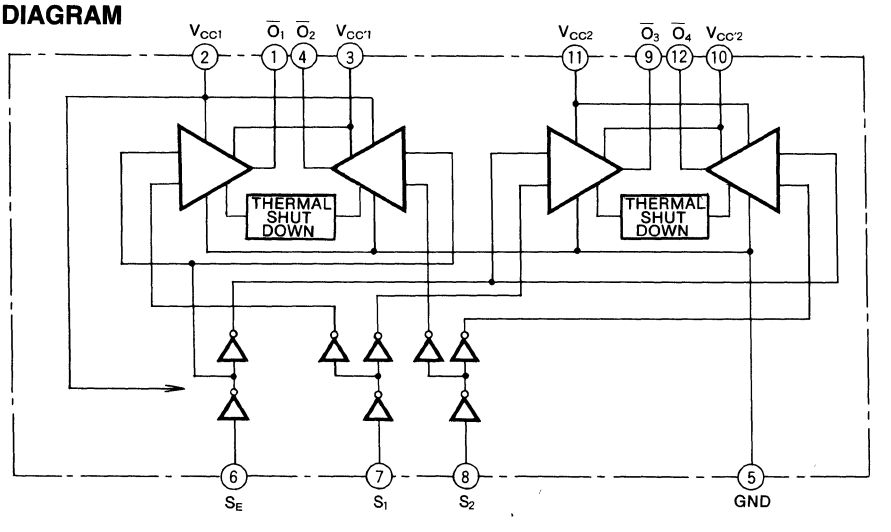
The M54549AL, two-full bridge motor driver, has the logic circuitry and the quasi-darlington power driver for bi-directional control of two D-C motors operating at current up to 1.2A.

The input S_E selects one of the bridges and S_1, S_2 determine the output polarity.

LOGIC TRUTH TABLE

Input			Output				Note	
S_E	S_1	S_2	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	Output $\overline{O}_1$, $\overline{O}_2$	Output $\overline{O}_3$, $\overline{O}_4$
0	0	0	OFF	OFF	OFF	OFF	OPen	Open
0	1	0	1	0	OFF	OFF	↻	Open
0	0	1	0	1	OFF	OFF	↻	Open
0	1	1	0	0	OFF	OFF	Braking	Open
1	0	0	OFF	OFF	OFF	OFF	Open	Open
1	1	0	OFF	OFF	1	0	Open	↻
1	0	1	OFF	OFF	0	1	Open	↻
1	1	1	OFF	OFF	0	0	Open	Braking

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M54549AL

DUAL BI-DIRECTIONAL MOTER DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+18	V
$V_{CC'}$	Driver supply voltage		−0.5～+18	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−2～$V_{CC'}$+2.5	V
$I_{O(max)}$	Peak output current	t_{op}=10ms, retitive cycle 0.2Hz max	±1.2	A
$I_{O(1)}$	Continuous output current (1)		±330	mA
Pd	Power dissipation	T_a=75℃	830	mW
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMNDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

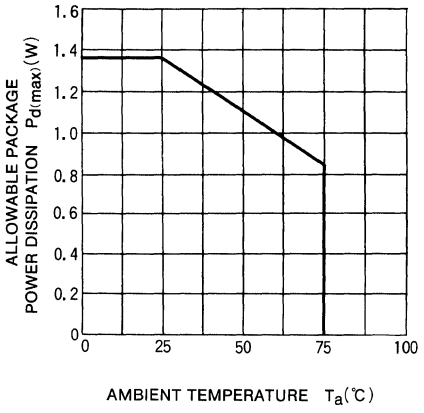
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	16	V
I_O	Output current				±300	mA
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.4	V
t_B	Motor braking interval		100			ms
$t_{j(shut)}$	Thermal shutdown temperature			150		℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

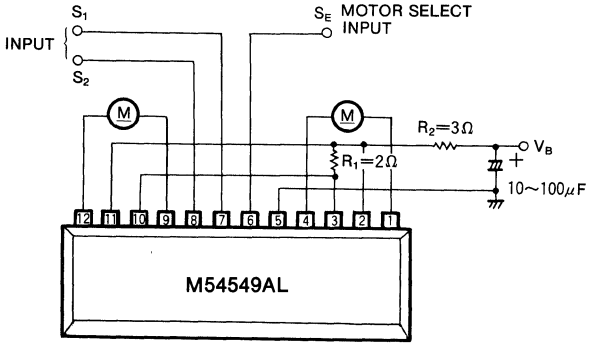
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=$V_{CC'}$=18V	V_O=18V			100	μA
		V_{S1}=V_{S2}=0.4V, V_{SE}=0.4V or 2V	V_O=0V			−100	
V_{OH}	High-level output saturation voltage	V_{CC}=$V_{CC'}$=12V	$I_{OH(1)}$=−200mA	10.8			V
			$I_{OH(1)}$=−500mA	10.7			
V_{OL}	Low-level output saturation voltage	V_{CC}=$V_{CC'}$=12V	I_{OL}=200mA			0.5	V
			$I_{OL(1)}$=500mA			1.35	
I_{IH}	High-level input current	V_{CC}=$V_{CC'}$=12V, V_I=2V		50		120	μA
I_{CC1}	Supply current (1)	V_{CC}=$V_{CC'}$=12V	V_{SEO}=V_{S1}=V_{S2}=0.4V			10	mA
			V_{SE}=V_{S1}=0.4V, V_{S2}=2V			20	
I_{CC2}	Supply current (2)	V_{CC}=$V_{CC'}$=12V	V_{SE}=2V, V_{S1}=V_{S2}=0.4V			10	mA
			V_{SE}=V_{S1}=2V, V_{S2}=2V			20	

TYPICAL CHARACTERTICS

ALLOWABLE AVERGE
POWER DISSIPATION



APPLICATION EXAMPLE



M54560P

7-UNIT 150mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54560P, 7-channel source driver, consists of 7 PNP and 7 NPN transistors, connected to form high current gain driver with PNP action.

FEATURES

- High output sustaining voltage to 40V
- Output source current to 150mA
- Integral diode for transient suppression
- Active "L" input
- Wide operating temperature range (T_a =−20∼+75℃)

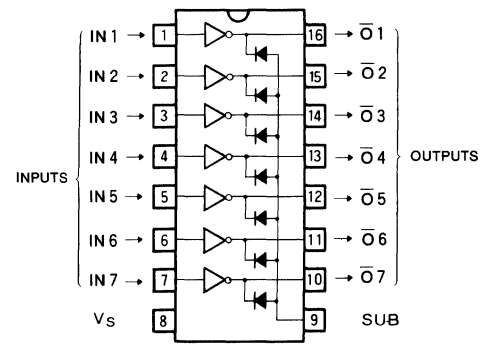
APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

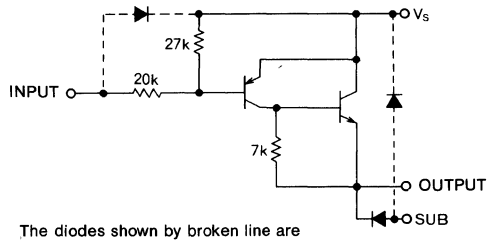
The M54560P is comprised of seven PNP-NPN darlington source driver pairs with 20kΩ series input resistors. Each output has an integral diode for inductive load transient suppression. The anodes of the diodes and the substrate connected together to pin 9 . The outputs are capable of driving 150mA and are rated for operation with output voltages of up to 40V. The output is turned ON by switching the input low.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Output is in "L"	−0.5∼+40	V
V_S	Supply voltage		40	V
V_I	Input voltage		0∼+40	V
I_O	Output current	Per channel current at "H"output	−150	mA
I_F	Clamp diode forward current		−150	mA
V_R	Clamp diode reverse voltage		40	V
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54560P

7-UNIT 150mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		40	V
I_O	Output current per channel	Percent duty cycle less than 90%	0		−100	mA
		Percent duty cycle less than 100%	0		−50	
V_{IH}	High-level Input voltage		V_S−0.2		V_S+0.3	V
V_{IL}	Low-level Input voltage	I_O=−100mA	0		V_S−5	V
		I_O=−50mA	0		V_S−3.5	

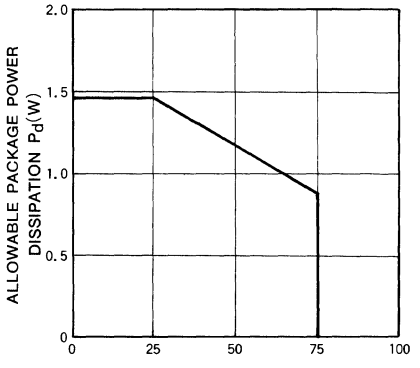
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{S(leak)}$	Supply leakage current	V_S=40V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=V_S−5V, I_O=−100mA		0.82	1.5	V
		V_I=V_S−3.5V, I_O=−50mA		0.75	1.2	
I_I	Input voltage	V_I=V_S−8.5V		−380	−670	μA
V_F	Clamp diode forward voltage	I_F=−100mA		−1.1	−2.4	V
V_R	Clamp diode reverse voltage	I_R=100μA	40			V
h_{FE}	DC forward current gain	V_S−V_O=4V, I_O=−100mA, T_a=25℃	500	2800		—

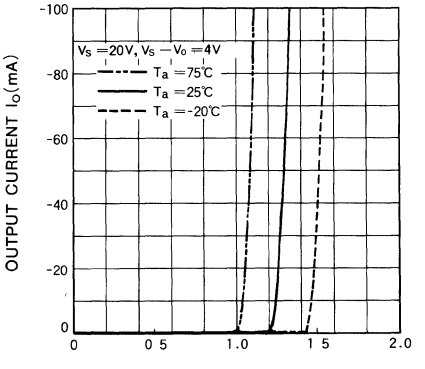
* : A typical value at T_a=25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



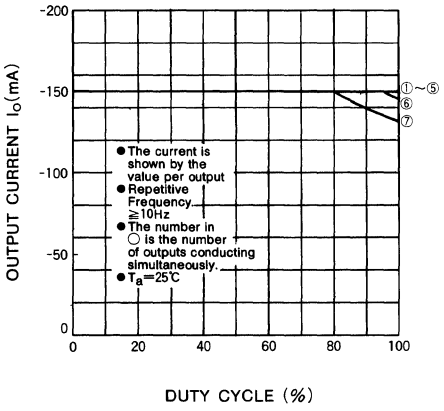
OUTPUT CURRENT CHARACTERISTICS



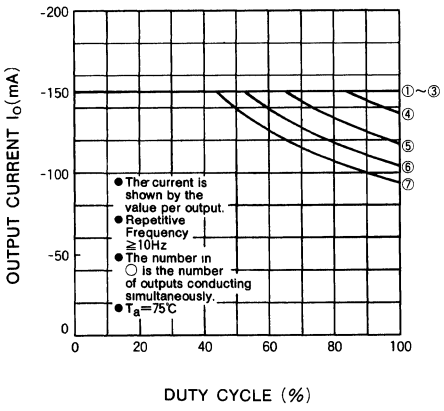
MITSUBISHI ELECTRIC

7-UNIT 150mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

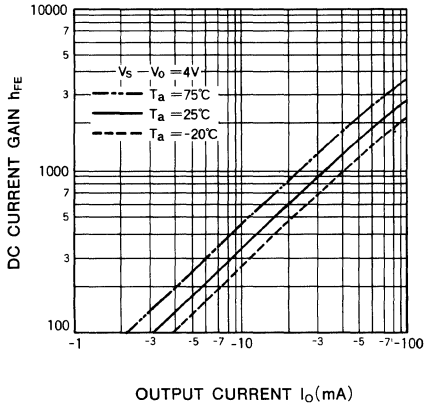
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54561P

7-UNIT 300mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54561P, 7-channel source driver, consists of 7 PNP and 14 NPN transistors connected to form high current gain driver with PNP action.

FEATURES

- High output sustaining voltage to 40V
- High output source current to 300mA
- Integral diode for transient suppression
- Active "L" input
- Wide operating temperature range (T_a =−20∼+75℃)

APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Active "L" input, Interfacing for standard MOS/BIPOLAR logics

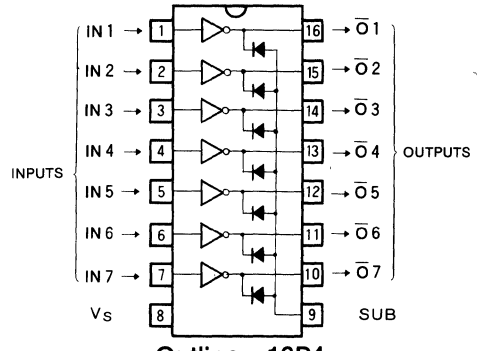
FUNCTION

The M54561P functions like a PNP transistor and the compound PNP/NPN/NPN output provides high current gain. Each output has an integral diode for inductive load transient suppression and the anodes of the diodes and the substrate are connected together to pin 9 .

The output are capable of driving 300mA and are rated for operation with output voltage up to 40V.

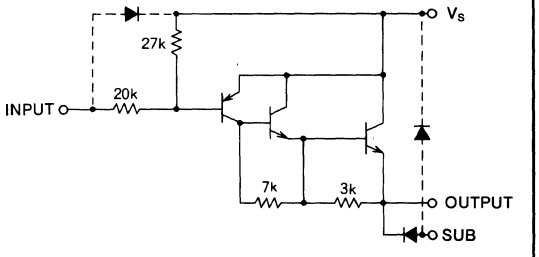
The output is turned ON by switching the input low.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Output is in "L"	−0.5∼+40	V
V_S	Supply voltage		40	V
V_I	Input voltage		0∼+40	V
I_O	Output current	Per channel current at "H"output	−300	mA
I_F	Clamp diode forward current		−300	mA
V_R	Clamp diode reverse voltage		40	V
P_d	Power dissipation	T_a =25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

MITSUBISHI ELECTRIC

M54561P

7-UNIT 300mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		40	V
I_O	Output current per channel	Percent duty cycle less than 15%	0		−250	mA
		Percent duty cycle less than 50%	0		−100	
V_{IH}	High-level Input voltage		V_S−0.2		V_S+0.3	V
V_{IL}	Low-level Input voltage	I_O=−250mA	0		V_S−3	V

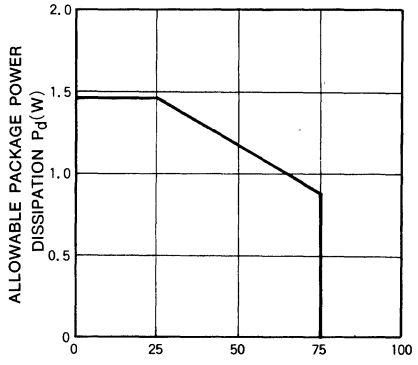
ELECTRICAL CHARACTERISTICS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{S(leak)}$	Supply leakage current	V_S=40V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=V_S−3V, I_O=−250mA		1.6	2.3	V
		V_I=V_S−3V, I_O=−100mA		1.45	2.0	
I_I	Input current	V_I=V_S−3.5V		−150	−250	μA
V_F	Clamp diode forward voltage	I_F=−300mA		−1.6	−2.4	V
V_R	Clamp diode reverse voltage	I_R=100μA	40			V
h_{FE}	DC forward current gain	V_S−V_O=4V, I_O=−300mA, T_a=25℃	1000	8000		—

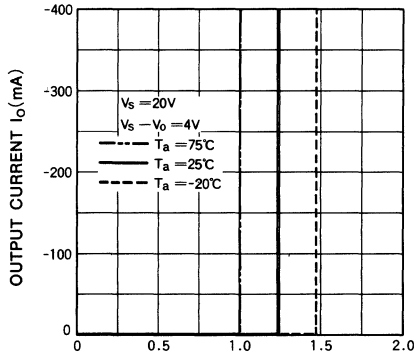
* : A typical value at T_a=25℃.

TYPICAL CHARACTERISTICS

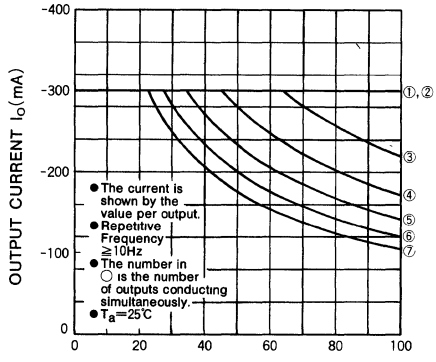
ALLOWABLE AVERAGE POWER DISSIPATION



OUTPUT CURRENT CHARACTERISTICS

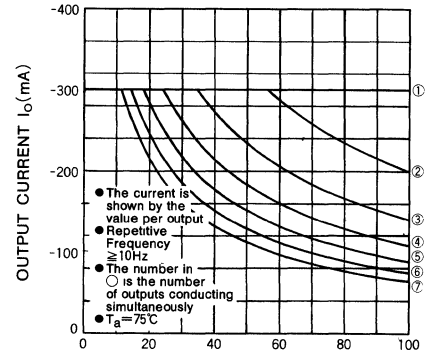


ALLOWABLE OUTPUT CURRENT AS A FUNCTIONAL OF DUTY CYCLE



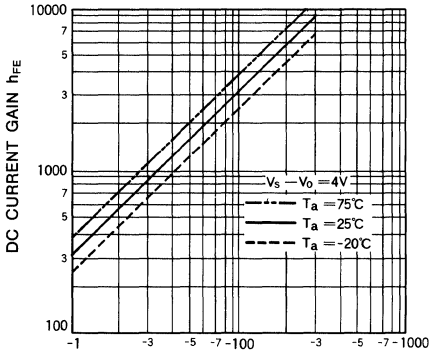
DUTY CYCLE (%)

ALLOWABLE OUTPUT CURRENT AS A FUNCTIONAL OF DUTY CYCLE



DUTY CYCLE (%)

DC CURRENT GAIN CHARACTERISTICS



OUTPUT CURRENT I_O(mA)

M54562P

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54562P, 8-channel source driver, is designed for use with MOS logic systems.

FEATURES

- High output sustaining voltage to 50V
- High output source current to 500mA
- Integral diode for transient suppression
- CMOS compatible input
- Wide operating temperature range (T_a = −20∼+75℃)

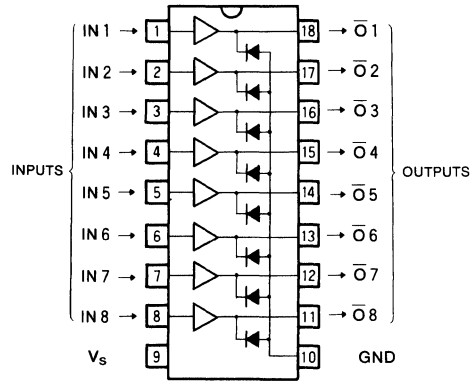
APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

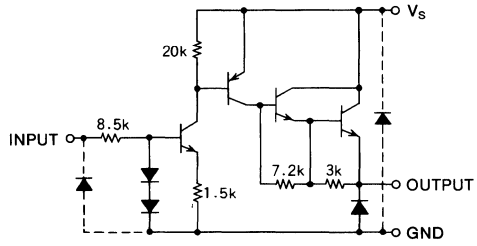
The driver of the M54562P is comprised of a NPN invertor and compound PNP/NPN/NPN output source driver, and the output is turned ON by an active high input level. Each output has an integral diode for inductive load transient suppression. The outputs are capable of driving 500mA and are rated for operation with output voltage up to 50V.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Output is in "L"	−0.5∼+50	V
V_S	Supply voltage		50	V
V_I	Input voltage		0∼+30	V
I_O	Output current	Per channel current at "H" output	−500	mA
I_F	Clamp diode forward current		−500	mA
V_R	Clamp diode reverse voltage		50	V
Pd	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54562P

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a = −20~+75℃, unless otherwise noted)

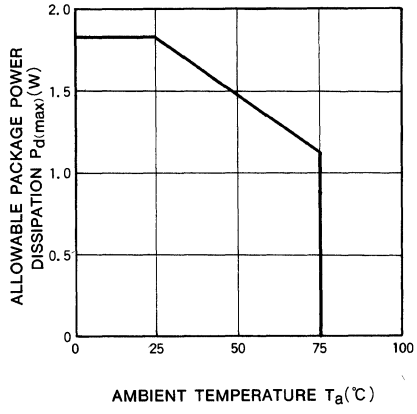
Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		50	V
I_O	Output current per channel	Percent duty cycle less than 8%	0		−350	mA
		Percent duty cycle less than 55%	0		−100	
V_{IH}	High-level Input voltage	I_O=−350mA	2.4	5	30	V
V_{IL}	Low-level Input voltage		0		0.2	V

ELECTRICAL CHARACTERISTICS (T_a = −20~+75℃, unless otherwise noted)

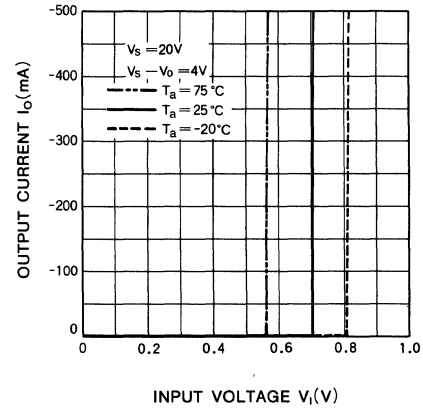
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_S (leak)	Supply leak current	V_S=50V, V_I=0.2V			100	μA
V_{CE} (sat)	Output saturation voltage	V_S=10V, V_I=2.4V, I_O=−350mA		1.6	2.4	V
		V_S=10V, V_I=2.4V, I_O=−100mA		1.45	2.0	
I_I	Input current	V_I=5V		0.48	0.75	mA
		V_I=25V		2.8	4.7	
I_S	Supply current	V_S=50V, V_I=5V		5.6	15	mA
V_F	Clamp diode forward voltage	I_F=−350mA		−1.2	−2.4	V
V_R	Clamp diode reverse voltage	I_R=100μA	50			V

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

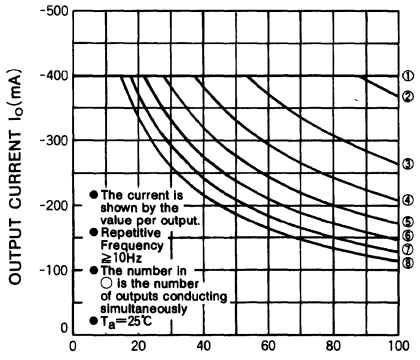


OUTPUT CURRENT CHARACTERISTICS

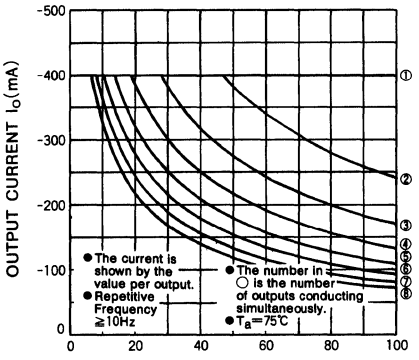


MITSUBISHI ELECTRIC

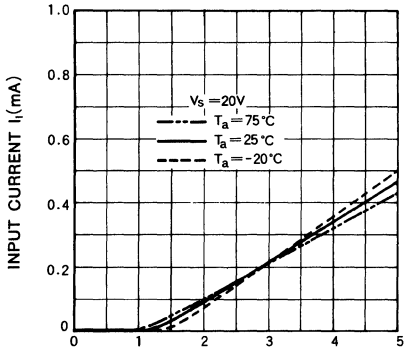
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



M54563P

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54563P, 8-channel source driver, is designed for use with + 6 to +16V MOS logic systems.

FEATURES

- High output sustaining voltage to 50V
- High output source current to 500mA
- Integral diode for transient suppression
- Wide operating temperature range (T_a=−20∼+75℃)

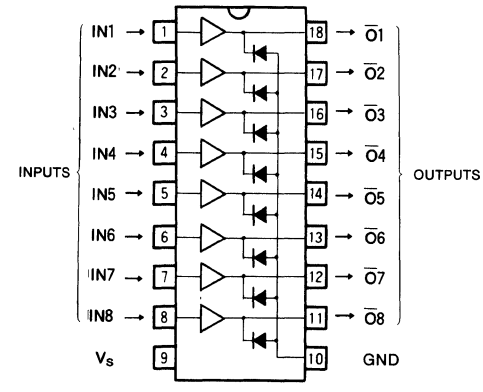
APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

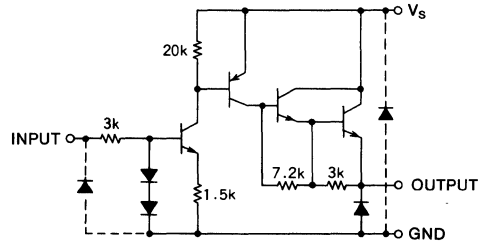
The driver of the M54563P is comprised of a NPN invertor and compound PNP/NPN/NPN output source driver and the output is turned ON by an active high input level. Each output has an integral diode for inductive load transient suppression. The outputs are capable of driving 500mA and are rated for operating with output voltage up to 50V.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+50	V
V_S	Supply voltage		50	V
V_I	Input voltage		0∼+10	V
I_O	Output current	Transistor OFF	−500	mA
I_F	Clamp diode forward current		−500	mA
V_R	Clamp diode reverse voltage		50	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54563P

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		50	V
I_O	Output current per channel	Percent duty cycle less than 8%	0		−350	mA
		Percent duty cycle less than 60%	0		−100	
V_{IH}	High-level Input voltage	I_O=−350mA	2.4		25	V
V_{IL}	Low-level Input voltage		0		0.2	V

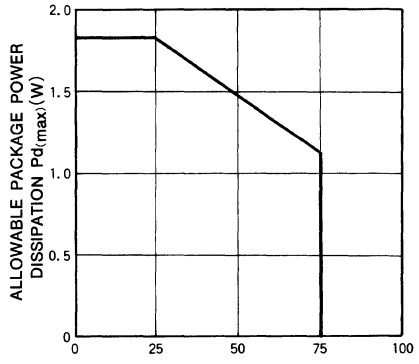
ELECTRICAL CHARACTERISTICS (T_a = −20~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{S(leak)}$	Supply leak current	V_S=50V, V_I=0.2V				100	μA
$V_{CE(sat)}$	Output saturation voltage	V_S=10V	I_O=−350mA		1.6	2.4	V
		V_I=4V	I_O=−100mA		1.45	2	
I_I	Input current	V_I=3V			0.6	2	mA
		V_I=10V			2.9	5	
I_S	Supply current	V_S=50V, V_I=3V			5.6	15	mA
V_F	Clamp diode forward voltage	I_F=−350mA			−1.2	−2.4	V
V_R	Clamp diode forward voltage	I_R=100μA		50			V

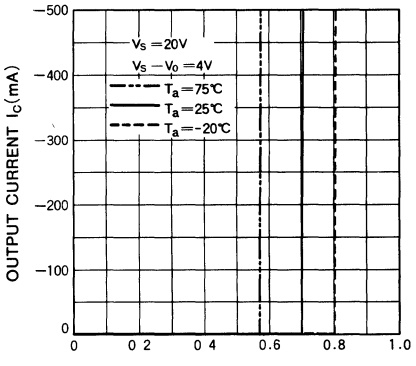
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

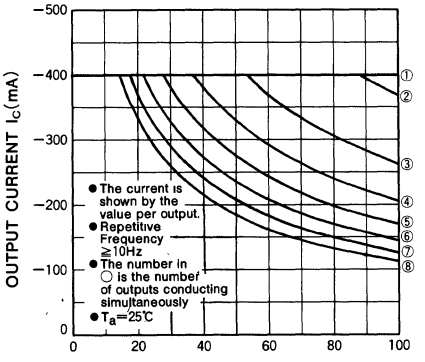
ALLOWABLE AVERAGE POWER DISSIPATION



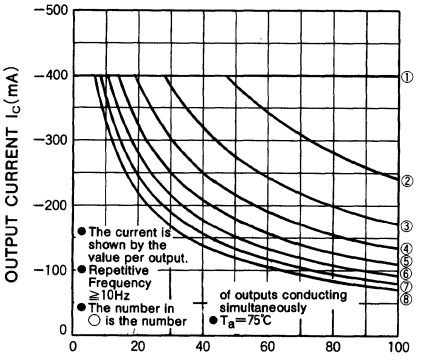
OUTPUT CURRENT CHARACTERISTICS



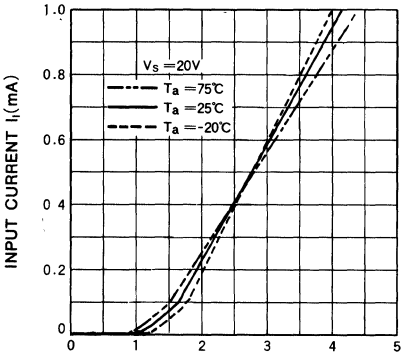
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



M54564P

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54564P, 8-channel source driver, is designed for interfacing between low power digital logic and a fluorescent display.

FEATURES

- High output sustaining voltage to 50V
- High output source current to 500mA
- CMOS, TTL Compatible input
- Internal pull-down resistors
- Wide operating temperature range (T_a = −20∼+75℃)

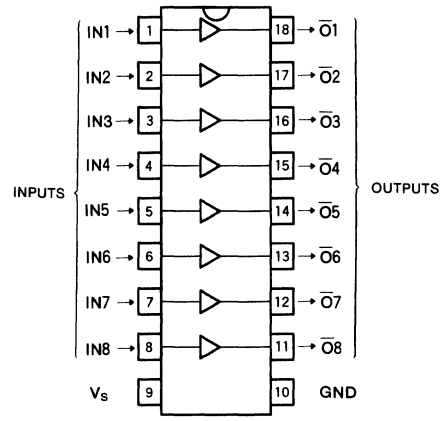
APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

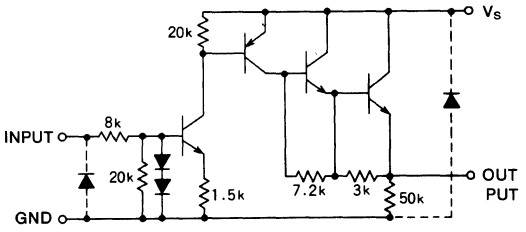
The driver of the M54564P is comprised of a NPN invertor and compound PNP/NPN/NPN output source driver and the output is turned ON by an active high input level. Each output has 50kΩ pull-down resistor suitable for driving fluorescent displays. The outputs are capable of driving 500mA and are rated for operation with output voltage up to 50V.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage		−0.5∼+50	V
V_S	Supply voltage		50	V
V_I	Input voltage		0∼+30	V
I_O	Output current		−500	mA
P_d	Power dissipation	T_a=25℃	1.79	W
T_{opr}	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

RECOMMENDED OPERATIONAL CONDITIONS (T_a = −20～+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		50	V
I_O	Output current per channel	Percent duty cycle less than 8%	0		−350	mA
		Percent duty cycle less than 55%	0		−100	
V_{IH}	High-level Input voltage	I_O=−350mA	2.4		25	V
V_{IL}	Low-level Input voltage		0		0.2	V

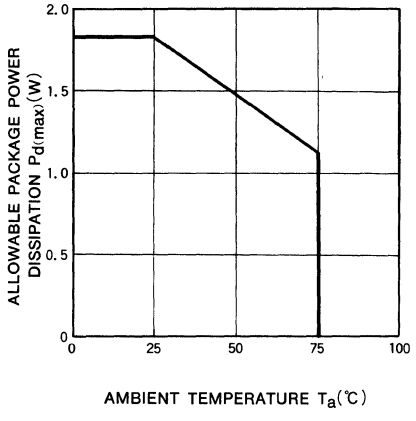
ELECTRICAL CHARACTERISTICS (T_a = −20～+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{S(leak)}$	Supply leak current	V_S=50V, V_I=0.2V				100	μA
$V_{CE(sat)}$	Output saturation voltage	V_S=10V	I_O=−350mA		1.6	2.4	V
		V_I=4V	I_O=−100mA		1.45	2	
I_I	Input current	V_I=4V			0.4	0.7	mA
		V_I=25V			2.9	4.7	
I_S	Supply current	V_S=50V, V_I=4V			5.6	6.5	mA

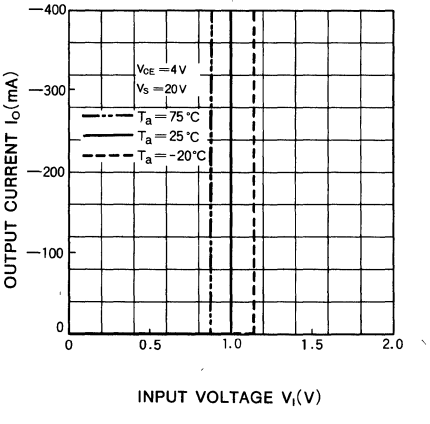
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

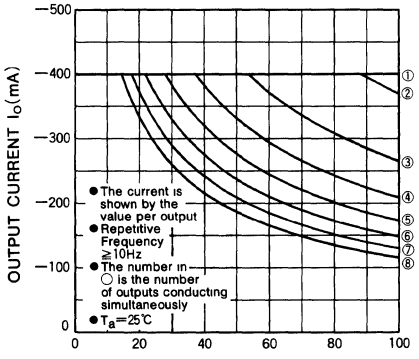


OUTPUT CURRENT CHARACTERISTICS

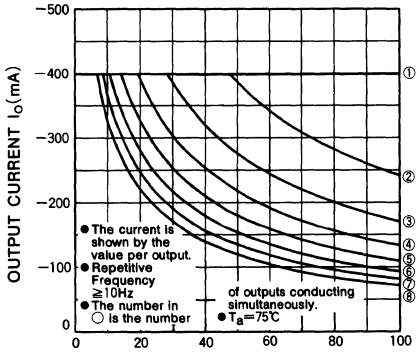


MITSUBISHI ELECTRIC

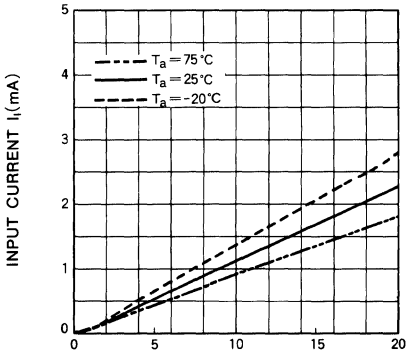
ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



M54565P

8-UNIT 50mA TRANSISTOR ARRAY ("L" ACTIVE INPUT)

DESCRIPTION

The M54565P, 8-channel sink driver, consists of 7 PNP and 7 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output breakdown voltage to 20V
- Output sink current to 50mA
- Wide operating temperature range (T_a = −20~+75℃)
- Low-level Active Input

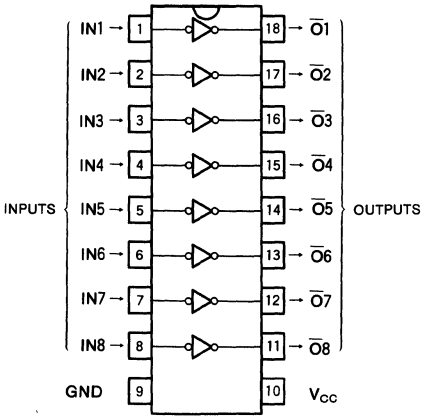
APPLICATION

LED or incandescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

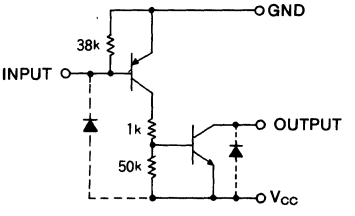
The M54565P is comprised of eight PNP-NPN non darlington sink drivers. It functions from 2 V of supply voltage and features low output saturation voltage. The output is turned ON by switching the input low.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5~+20	V
I_C	Collector current	Transistor ON	50	mA
V_I	Input voltage		0~V_{CC}	V
T_{opr}	Operating temperature		−20~+75	℃
T_{stg}	Storage temperature		−55~+125	℃

8-UNIT 50mA TRANSISTOR ARRAY ("L" ACTIVE INPUT)

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_O	Output voltage		0		20	V
I_C	Collector current		0		20	mA
I_{IH}	"H" Input current		−8		8	μA
I_{IL}	"L" Input current	I_O=40mA	−200		−5000	μA

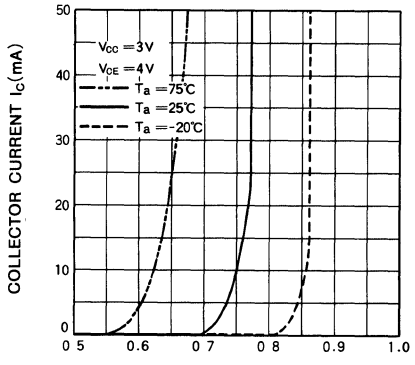
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CC} =6V, V_O =20V				50	μA
$V_{CE(sat)}$	Output saturation voltage	V_{CC} = 3 V, I_I =−200μA	I_C =20mA		0.03	0.17	V
			I_C =40mA		0.05	0.23	
V_I	Input voltage	V_{CC} = 2 V, I_I =−200μA		1	1.25		V
I_{CC}	Supply current	V_{CC}= 3 V, I_I =−200μA			2.3	4	mA
h_{FE}	DC forward current gain	V_{CE} =4V, V_{CC} =3V, I_C =40mA, T_a =25℃		800	2500		—

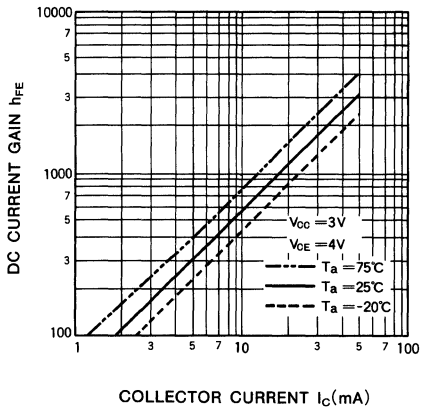
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54566P

7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY ("L" ACTIVE INPUT)

DESCRIPTION

The M54566P, 7-channel sink driver, consists of 7 PNP and 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 50V
- High output sink current to 400mA
- Low-level Active input
- Wide operating temperature range (T_a = −20∼+75℃)

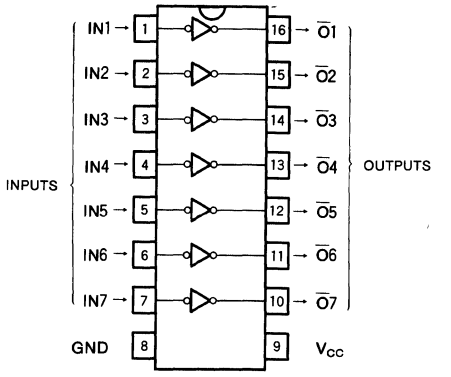
APPLICATION

Relay and printer driver Interfacing between standard MOS/BIPOLAR logics

FUNCTION

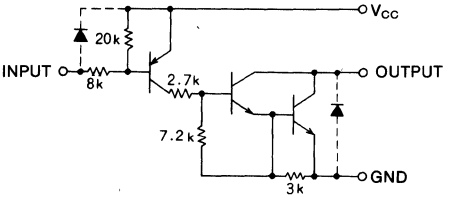
The M54566P is comprised of seven PNP invertors with 8 kΩ series input resistors and NPN darlington sink drivers. The output is turned ON by switching the input low. The outputs are capable of sinking 400mA and will withstand 50V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+50	V
V_I	Input voltage		0∼V_{CC}	V
I_C	Collector current	Transistor ON	400	mA
P_d	Power dissipation	T_a =25℃	1.47	W
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

M54566P

7-UNIT 400mA DARLINGTON TRANSISTOR ARRAY ("L" ACTIVE INPUT)

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	8	V
I_C	Collector current per channel	Percent duty cycle less than 10%	0		350	mA
		Percent duty cycle less than 30%	0		200	
V_{IH}	"H" Input voltage	$I_{O(leak)}$=50μA	V_{CC}−0.2		V_{CC}	V
V_{IL}	"L" Input voltage	I_C=350mA	0		V_{CC}−3	V

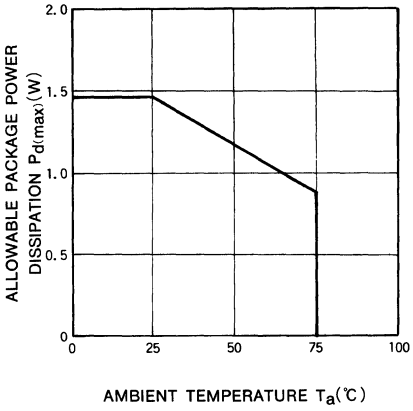
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100 μA		50			V
$V_{CE(sat)}$	Output saturation voltage	V_I = V_{CC} −3V	I_C =350 mA		1.1	2.2	V
			I_C =200 mA		0.9	1.6	
I_I	Input current	V_I = V_{CC} −3.5 V			−0.38	−0.58	mA
I_{CC}	Supply current	V_{CC} =5 V, V_I = V_{CC} −3.5 V			1.4	3	mA
h_{FE}	DC forward current gain	V_{CE} =4 V, V_{CC} =5 V, I_C =350 mA, T_a =25℃		2000	10000		—

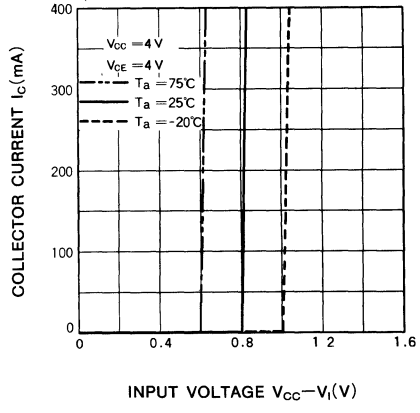
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

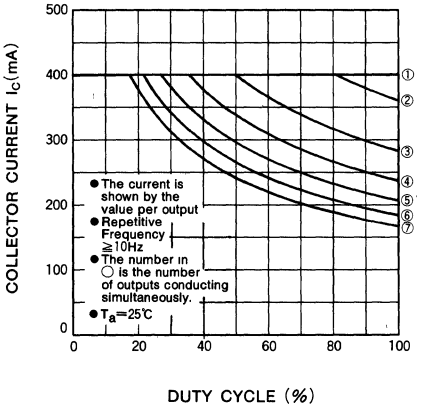
ALLOWABLE AVERAGE POWER DISSIPATION



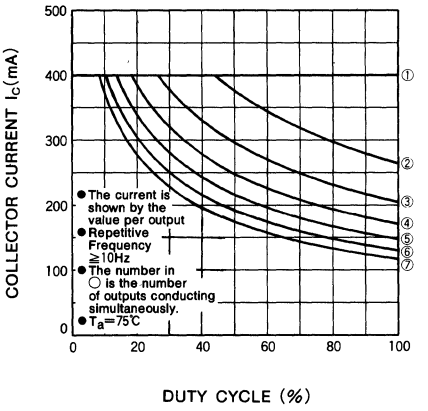
OUTPUT CURRENT CHARACTERISTICS



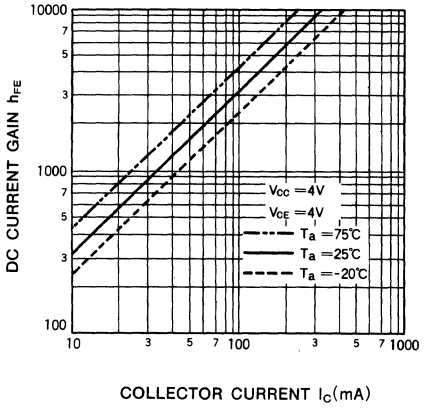
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



M54567P

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54567P, 4-channel sink driver, consists of 4 PNP and 8 NPN transistors to form high current gain driver pairs.

FEATURES

- High output sustaining voltage to 50V
- High output current to 1.5A
- Integral diodes for transient suppression
- NMOS Compatible input
- Wide operating temperature range (T_a = −20∼+75℃)

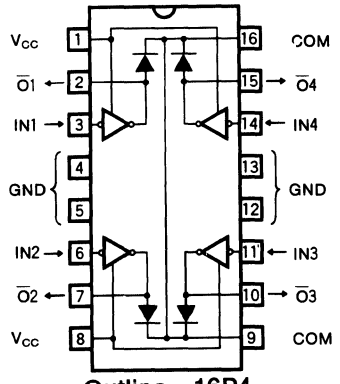
APPLICATION

Relay and printer driver, LED or incandescent display digit driver

FUNCTION

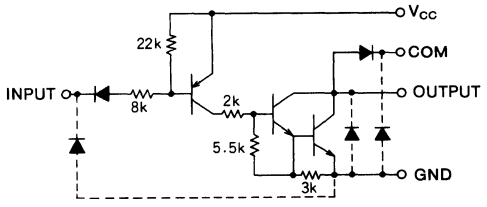
The M54567P is comprised of four PNP invertors with 8kΩ series input resistors and NPN darlington sink drivers. Each output has an integral diode for inductive load transient suppression and the anodes of the diode connected to pins 9 and 16. The outputs are capable of sinking 1.5A and will withstand 50V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+50	V
V_I	Input voltage		30	V
I_C	Collector current	Transistor ON	1.5	A
V_R	Clamp diode reverse voltage		50	V
I_F	Clamp diode foward current	Pulse width≦10ms, Repetitive cycle≦10Hz	1.5	A
			1	
P_d	Power dissipation	T_a =25℃	1.92	W
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
V_O	Output voltage		0		40	V
I_C	Collector current per channel	All units ON Percent duty cycle≦4%	0		1.25	A
		All units ON Percent duty cycle≦18%	0		0.7	
V_{IH}	High-level Input voltage	$I_{O(leak)}$=50μA	V_{CC}−0.5		V_{CC}	V
V_{IL}	Low-level Input voltage	I_C=1.25A	0		V_{CC}−3.5	V

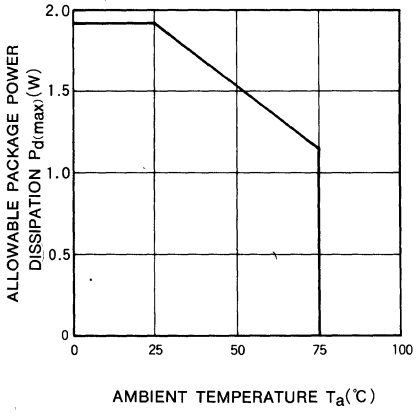
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA		50			V
I_{CC}	Supply current	V_{CC}=6V, V_I=0.5V			3.0	4.5	mA
$V_{CE(sat)}$	Output saturation voltage	V_{CC}=4V, V_I=0.5V	I_C=1.25A		1.6	2.2	V
			I_C=0.7A		1.1	1.7	
I_I	Input current	V_I=V_{CC}−3.5V			−0.3	−0.6	mA
		V_I=V_{CC}−6V			−0.58	−0.95	
V_R	Clamp diode reverse voltage	I_R=100μA		50			V
V_F	Clamp diode forward voltage	I_F=1.25A			1.6	2.3	V
h_{FE}	DC forward current gain	V_{CC}=4V, V_{CE}=4V, I_C=1A, T_a=25℃		4000	30000		—

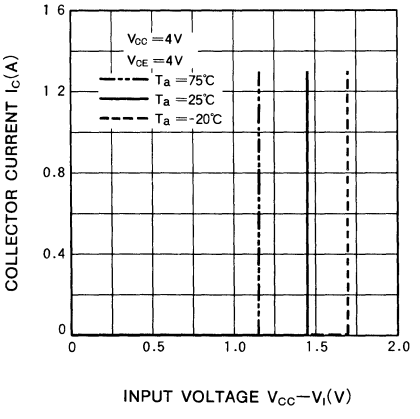
* : Typical valuse are at T_a=25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



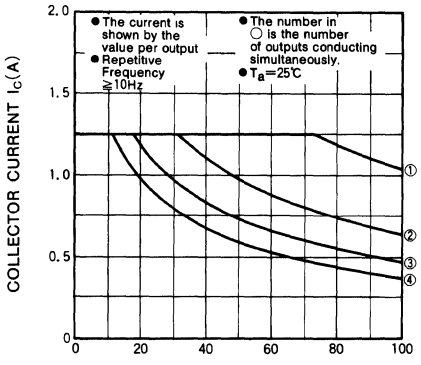
OUTPUT CURRENT CHARACTERISTICS



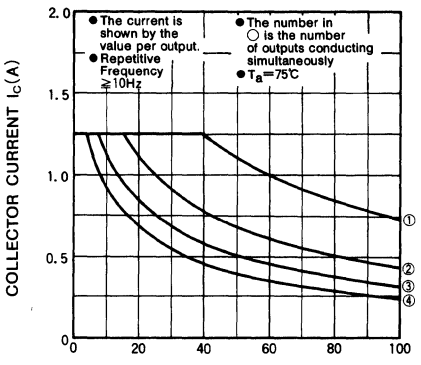
MITSUBISHI ELECTRIC

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

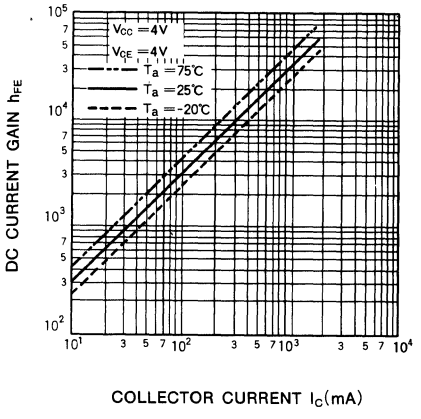
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



M54568L

4-UNIT 30mA PNP TRANSISTOR ARRAY

DESCRIPTION

The M54568L, general purpose transistor array, consists of 4 PNP transistors connected in a commom-emitter configuration.

FEATURES

- 20V breakdown
- 30mA output source current capability
- Wide operating temperature range (T_a=−20∼+75℃)

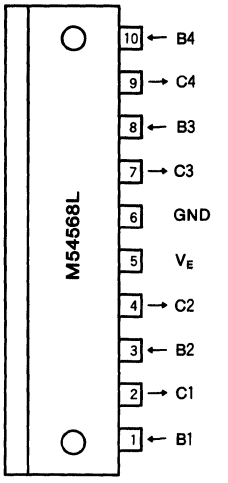
APPLICATION

LED or incandescent display driver

FUNCTION

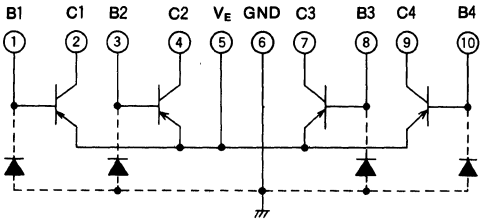
The M54568L is comprised of 4 PNP transistors. ALL emitters are connected to pin 5 . Each transistor is capable of switching 30mA and will withstand 20V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 10P5

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CBO}	Collector-base sustaining voltage	Base voltage : 0V	−40	V
V_{EBO}	Emitter-base sustaining voltage	Base voltage : 0V	−40	V
V_{CEO}	Collector-emitter sustaining voltage	Emitter voltage : 0V	−20	V
I_C	Collector current per transistor		−30	mA
I_B	Base current per transistor		−20	mA
P_d	Power dissipation	T_a =25℃	1000	mW
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
I_C	Collector current	I_B=−3mA	0		−20	mA
I_B	Base current		0		−10	mA
V_E	Emitter current		−0.3		20	V
V_B	Base voltage		−0.3		V_E	V

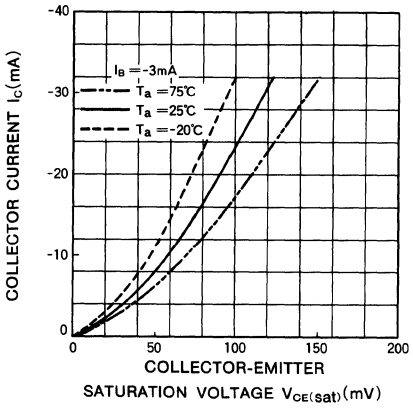
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CBO}$	Collector-emitter sustaining voltage	I_C =−10μA, V_B =0 V, V_E : OPEN		−40			V
$V_{(BR)EBO}$	Emitter-base sustaining voltage	I_E =−10μA, V_B =0 V, V_C : OPEN		−40			V
$V_{(BR)CEO}$	Collector-emitter sustaining voltage	I_C =−100μA, V_E =0 V, V_B : OPEN		−20			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C =−20 mA, I_B =−3 mA, V_E =5 V			−0.09	−0.3	V
		I_C =−2 mA, I_B =−0.2 mA, V_E =5 V			−0.02	−0.28	
h_{FE}	DC forward current gain	V_{CE} =−4 V, T_a =25℃	I_C =−2 mA	20	80		—
			I_C =−20 mA	15	60		

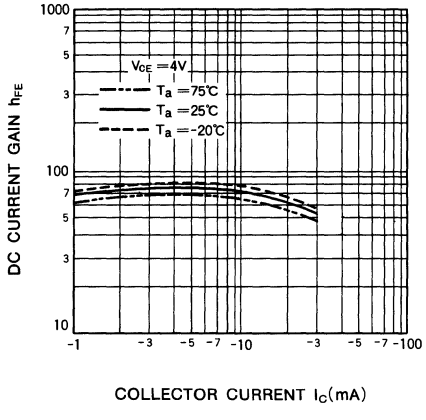
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

OUTPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54569P

8-UNIT 30mA PNP TRANSISTOR ARRAY

DESCRIPTION

The M54569P, general purpose transistor array, consists of 8 PNP transistors connected in a common-emitter configuration.

FEATURES

- 20V breakdown
- 30mA output source current capability
- Wide operating temperature range (T_a = −20∼+75℃)

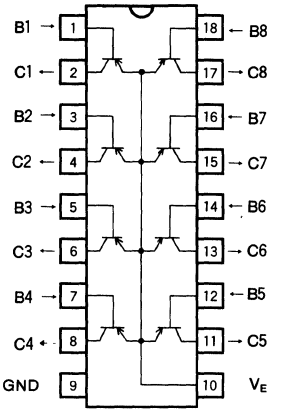
APPLICATION

LED or incandescent display driver

FUNCTION

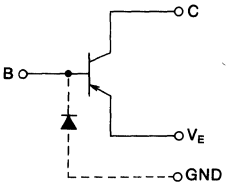
The M54569P is comprised of 8 PNP transistors. All emitters are connected to pin 10. Each transistor is capable of switching 30mA and will withstand 20V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CBO}	Collector-base sustaining voltage	Base voltage 0V	−40	V
V_{EBO}	Emitter-base sustaining voltage	Base voltage 0V	−40	V
V_{CEO}	Collector-emitter sustaining voltage	Emitter voltage 0V	−20	V
I_C	Collector current per transistor		−30	mA
I_B	Base current per transistor		−20	mA
P_d	Power dissipation	T_a=25℃	1.47	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

8-UNIT 30mA PNP TRANSISTOR ARRAY

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
I_C	Collector current	I_B=−3mA	0		−20	mA
I_B	Base current		0		−10	mA
V_E	Emitter voltage		−0.3		20	V
V_B	Base voltage		−0.3		V_E	V

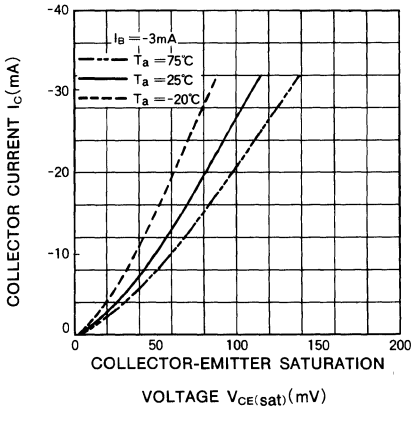
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)\ CBO}$	Collector-emitter sustaining voltage	I_C=−10μA, V_B=0V V_E : OPEN		−40			V
$V_{(BR)EBO}$	Emitter-base sustaining voltage	I_E=−10μA, V_B=0V V_C : OPEN		−40			V
$V_{(BR)\ CEO}$	Collector-emitter sustaining voltage	I_C=−100μA, V_E=0V V_B : OPEN		−20			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C=−20mA I_B=−3mA, V_E=5V			−0.09	−0.3	V
		I_C=−2mA I_B=−0.2mA, V_E=5V			−0.02	−0.28	
h_{FE}	DC forward current gain	V_{CE}=−4V T_a=25℃	I_C=−2mA	20	100		—
			I_C=−20mA	15	70		

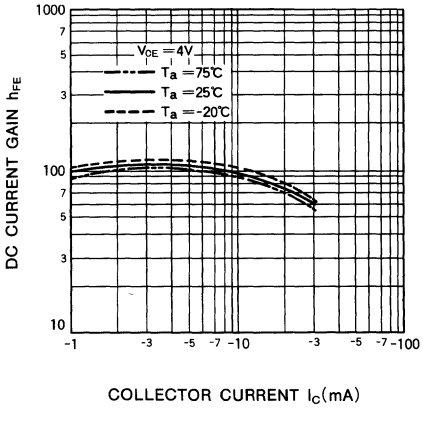
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

OUTPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54570L

TUNER BAND DECODER/DRIVER

DESCRIPTION

The M54570L is a semiconductor integrated circuit capable of switching four bands in TV and VTR tuners.

FEATURES

- Low output saturation voltage ($V_{CE(sat)} \leqq 0.5V$ at $I_O = -35mA$).
- High output sustaining voltage ($BV_{CEO} \geqq 26V$)
- Four-bands switching

APPLICATION

Switching bands in TV and VTR tuners

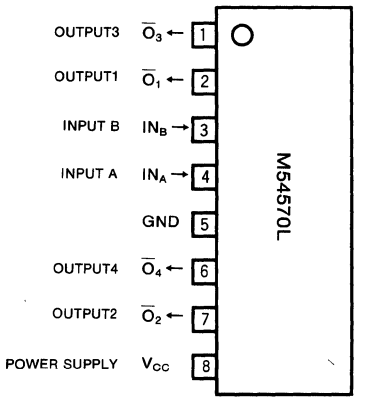
FUNCTION

The M54570L is an IC suitable for four-band switching in TV and VTR tuners. Since the output drives the power supply of each tuner band, a low saturation voltage (V_{CC}-V_O) becomes necessary. This need is satisfied through a first stage configured of PNP transistors.

The input, being three-valued logic input, can be switched into 6 output modes as shown in the truth table.

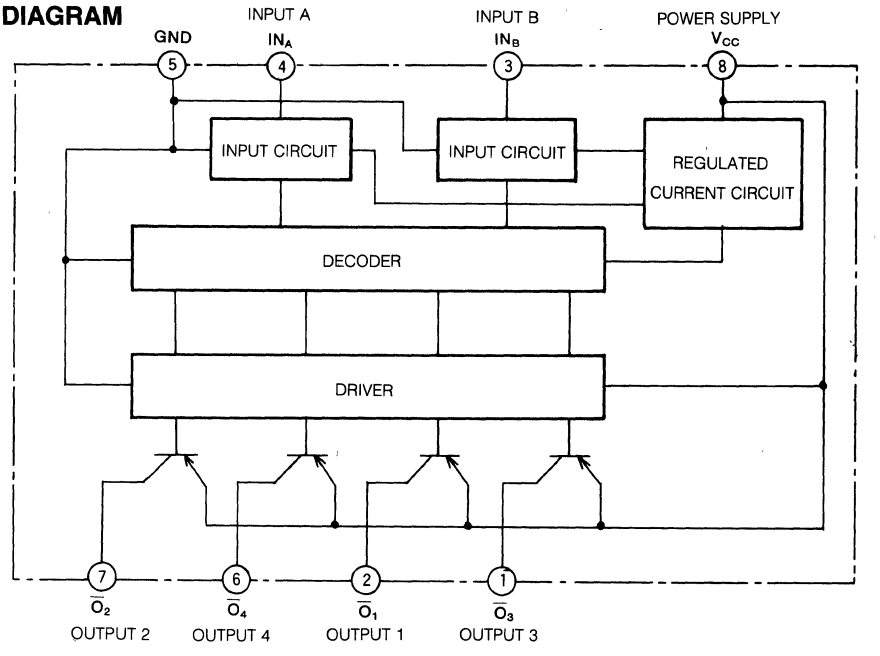
The selection mode can be altered by making a wired OR connection on the outputs when used as a three-band device.

PIN CONFIGURATIONS (TOP VIEW)



Outline 8P5

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

TRUTH TABLE

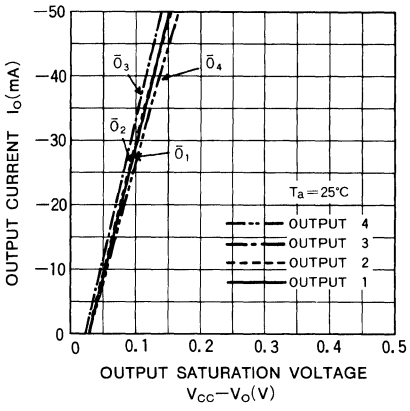
Input		Output			
IN_A	IN_B	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$
0	0	1	1	0	1
0	1	0	0	1	0
1	0	1	1	0	0
1	1	1	0	0	0
1 *	1 *	1	0	0	1
1 *	0	1	1	0	0

Input "0" = 0.4V (max.)
"1" = 4V (min.), 6V (max.)
"1 *" = 10V (min.), V_{CC} (max.)

Output "0" = output transistor off-state
"1" = output transistor on-state

TYPICAL CHARACTERISTICS

SOURCE OUTPUT SATURATION CHARACTERISTICS



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		15	V
V_{CEO}	Output sustaining voltage		−0.5～+26	V
V_I	Input voltage		15	V
I_O	Output current		−40	mA
Topr	Operating temperature		−10～+60	°C
Tstg	Storage temperature		−55～+125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 25°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CEO}	Output sustaining voltage		0		24	V
I_O	Output current	Outputs 1 and 3	0	−35	−40	mA
		Outputs 2 and 4	0	−20	−25	
V_{IH}	High-level input voltage		4		6	V
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}*	High-level* input voltage		10		V_{CC}	V

ELECTRICAL CHARACTERISTICS (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CC}=12V, V_O=−12V, output opened				−100	μA
V_{OH}	High-level output voltage	V_{CC}=12V	I_O=−20mA	11.7	11.9		V
			I_O=−35mA (output 1, 3)	11.5	11.9		
I_{IH}	High-level input current	V_{CC}=12V, V_I=4V				10	μA
I_{IH}*$_A$	High-level* input current (input A)	V_{CC}=12V, V_I*=10V			0.63	1.3	mA
I_{IH}*$_B$	High-level* input current (input B)	V_{CC}=12V, V_I*=10V				20	μA
I_{IL}	Low-level input current	V_{CC}=12V, V_I=0.4V				−100	μA
I_{CC}	Supply current	V_{CC}=13V, V_{IA}=0V, V_{IB}=4V, output opened			17	28	mA

* : A typical value at T_a=25°C.

M54571P

6-UNIT 350mA TRANSISTOR ARRAY AND MOTOR DRIVER

DESCRIPTION

The M54571P, 6-channel sink driver and voltage regulator, is designed for use with a small printer.

FEATURES

- High output sustaining voltage to 40V
- High output sink current to 350mA
- Voltage regulator with a control circuit
- Wide operating temperature range (T_a=−20∼+75℃)

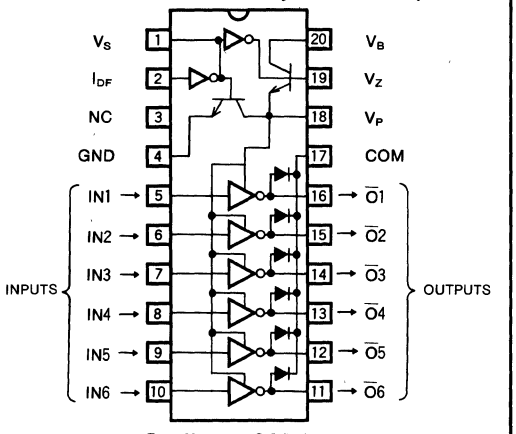
APPLICATION

Small calculator printer driver

FUNCTION

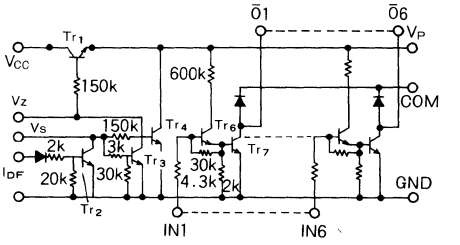
The M54571P is designed for driving a small serial printer made by CITIZEN and EPSON, and consists of 6 relay drivers and 1.2A motor driver. Each driver has 4.3kΩ series input resistor and output transient suppression diode. The driver outputs are capable of sinking 350mA and will withstand 43V in the OFF state. The output of the motor driver at pin 18 can drive 1.2A.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4 NC : NO CONNECTION

CIRCUIT SCHEMATIC



Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		40	V
V_{CEO}	Output sustaining voltage		−0.5∼+40	V
I_{C1}	Collector current	T_{r1}	100	mA
I_{C2}		T_{r2}	100	mA
I_{C3}		T_{r3}	100	mA
I_{C4}		T_{r4} Spike current 2A max Pulse width≦5 ms, Duty cycle≦5 %	1200	mA
I_{C7}		T_{r7} (Per channel)	350	mA
V_I	Input voltage	IN1∼IN6	40	V
$V_{I(IDF)}$			40	V
$V_{R(IDF)}$	Input reverse voltage		−45	V
$V_{R(D)}$	Clamp diode reverse voltage		40	V
$I_{F(D)}$	Clamp diode forward current		350	mA
Pd	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

MITSUBISHI ELECTRIC

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		8		40	V
V_P	Supply voltage		4		18	V
V_S	Reference voltage			10		V
I_C	Collector current	$\bar{O}1$∼$\bar{O}6$	0		250	mA
		$\bar{O}1$∼$\bar{O}6$	0		100	
$V_{I(IDF)}$	Input voltage				−35	V
			9		17	
V_I		IN1∼IN6	9		17	V
V_O	Output voltage	$\bar{O}1$∼$\bar{O}6$	0		40	V

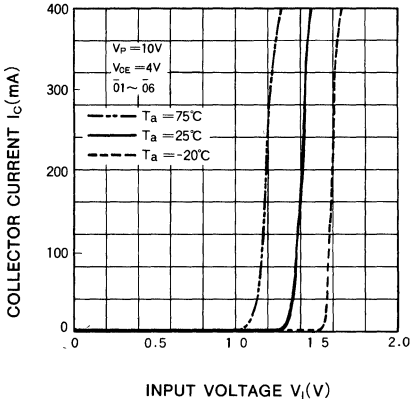
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
$V_{BR(CEO)}$	Output sustaining voltage		I_{CEO}=100μA, V_P=5V, ($\bar{O}1$∼$\bar{O}7$)	40			V
$V_{CE(sat)}$	Collector emitter saturation voltage	01 ∼ 07	V_P=6.5V, V_I=3V, I_C=250mA			0.8	V
			V_P=3V, V_I=2.4V, I_C=120mA			0.5	
		T_{r1}	I_B=1mA, I_C=10mA, V_P=0V			0.5	
		T_{r2}	$V_{I(IDF)}$=10V, I_{VS}=100mA			0.5	
		T_{r3}	$V_{I(Vs)}$=3V, I_{VZ}=30mA, $V_{I(IDF)}$=0V			0.4	
		T_{r4}	I_{VS}=50mA, I_{VP}=0.3V, $V_{I(IDF)}$=0V			0.45	
			I_{VS}=80mA, I_{VP}=1A, $V_{I(IDF)}$=0V			1.2	
I_I	Input current		V_P=6V, V_I=10V, (IN1∼IN6)			3.5	mA
$I_{I(IDF)}$			$V_{I(IDF)}$=10V			6.5	mA
$I_{I(Vs)}$			$V_{I(Vs)}$=3V, $V_{I(IDF)}$=0V			26	mA
$I_{R(IDF)}$	Input leakage current		$V_{R(IDF)}$=−35V			−20	μA
$V_{F(D)}$	Clamp diode forward voltage		$I_{F(D)}$=250mA			2.4	V
I_{VP}	Supply current		V_P=17V, V_I=10V (all input)			240	mA
			V_P=5V, V_I=10V (all input)			60	
h_{FE} 1	DC forward current gain	T_{r4}	I_C=50mA, V_{CE}=4V, T_a=25℃	100			—
h_{FE} 2	DC forward current gain	T_{r4}	I_C=1A, V_{CE}=4V, T_a=25℃	80			—
h_{FE} 3	DC forward current gain	$\bar{O}1$∼$\bar{O}7$	V_P=6.5V, I_C=350mA, V_{CE}=4V, T_a=25℃	1000			—

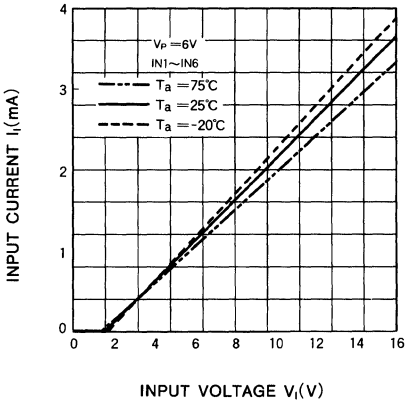
* : A typical value at T_a=25℃.

TYPICAL CHARACTERISTICS

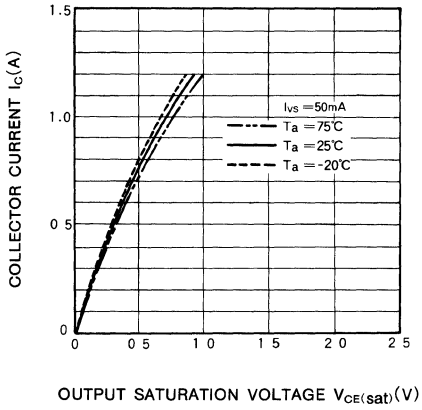
OUTPUT CURRENT CHARACTERISTICS



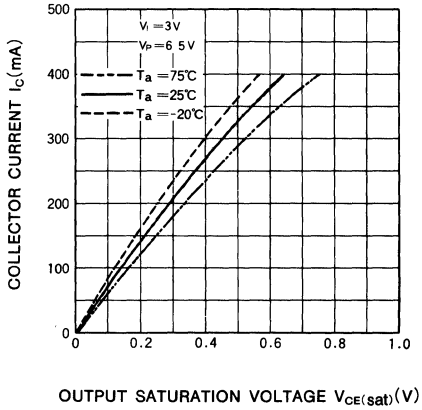
INPUT CHARACTERISTICS



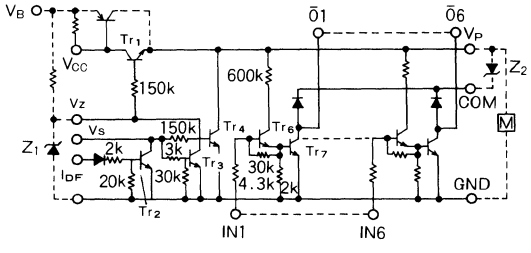
MOTOR DRIVER OUTPUT SATURATION CHARACTERISTICS



MAGNET RELAY DRIVER OUTPUT SATURATION CHARACTERISTICS



TYPICAL APPLICATION



NOTE

	V_B	V_{Z1}	Z_2	Magnet Relay Drive Current
EPSON Printer	15~40V	18V	—	90mA
CITIZEN Printer	3 ~ 9 V	6 V	connect between the V_P and the COM	250mA

M54572L

TUNER BAND DECODER/DRIVER

DESCRIPTION

The M54572L is a semiconductor integrated circuit capable of switching four bands in TV and VTR tuners.

FEATURES

- Low output saturation voltage ($V_{CE(sat)} \leqq 0.5V$ at $I_O = -30mA$).
- High output sustaining voltage ($BV_{CEO} \geqq 28V$)
- Four-bands switching

APPLICATION

Switching bands in TV and VTR tuners

FUNCTION

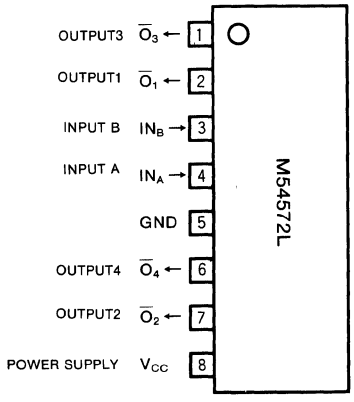
The M54572L is an IC suitable for four-band switching in TV and VTR tuners. Since the output (outputs 1~3) drives the power supply of each tuner band, a low saturation voltage ($V_{CC} - V_O$) becomes necessary. This need is satisfied through a first stage configured of PNP transistors.

Output 4 can be used for changing modes with the same power supply as the NPN transistor has an open collector output.

The input mode can be switched between four modes as shown in the truth table.

The selection mode can be altered by making a wired OR connection to outputs 1 ~ 3 when used as a three-band device.

PIN CONFIGURATIONS (TOP VIEW)



Outline 8P5

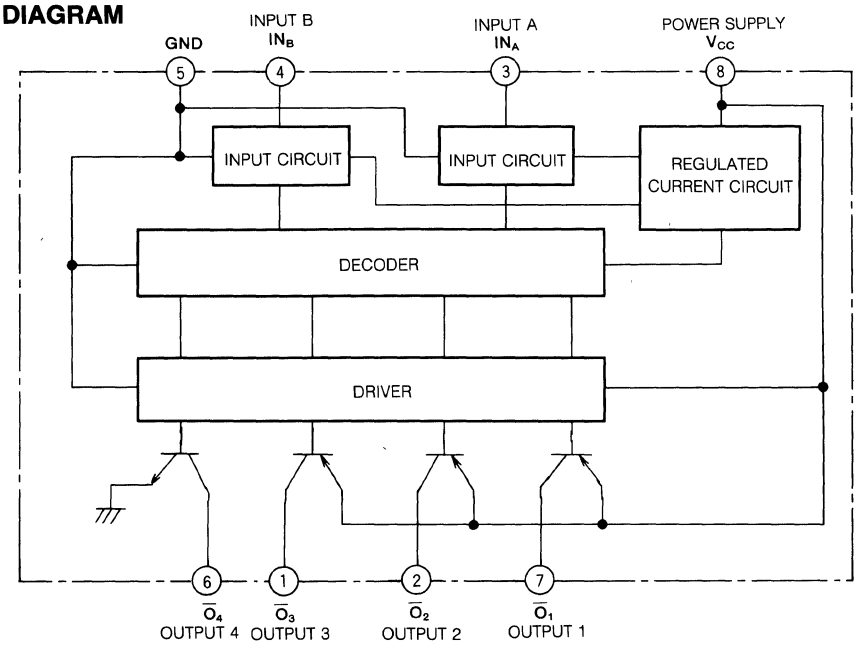
TRUTH TABLE

Input		Output			
IN_A	IN_B	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$	$\overline{O_4}$
0	0	1	Z	Z	Z
0	1	Z	Z	1	Z
1	0	Z	1	Z	Z
1	1	Z	Z	1	0

Input "0" = 1V (max.)
"1" = 3V (min.)

Output "0" = current sink
"1" = current source
"Z" = high impedance

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		18	V
V_{CEO}	Output sustaining voltage		−0.5～+28	V
V_I	Input voltage		18	V
I_{SO}	Output source current	$\overline{O1}$～$\overline{O3}$	−40	mA
I_{SI}	Output sink current	$\overline{O4}$	40	mA
Topr	Operating temperature		−10～+60	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 25℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		12		15	V
V_{CEO}	Output sustaining voltage		0		25	V
I_{SO}	Output source current	$\overline{O1}$～$\overline{O3}$	0		−30	mA
I_{SI}	Output sink current	$\overline{O4}$	0		30	mA
V_{IH}	High-level input voltage		3		V_{CC}	V
V_{IL}	Low-level input voltage		0		1	V

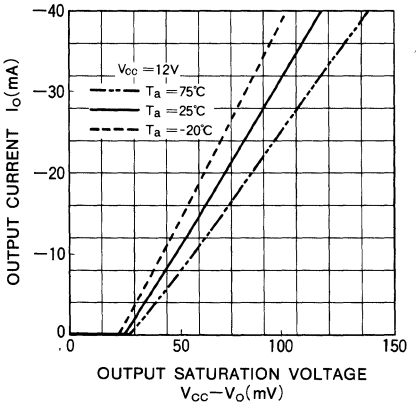
ELECTRICAL CHARACTERISTICS (T_a = 25℃, V_{CC} = 12V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{SO(leak)}$	Source output leakage current	V_{SO}=−12V			−100	μA
$I_{SI(leak)}$	Sink output leakage current	V_{SI}=25V			100	μA
V_{SOH}	Source output High-level voltage	I_{SO}=−30mA	11.5	11.8		V
V_{SIL}	Sink output Low-level voltage	I_{SI}=30mA		0.2	0.5	V
I_{IH}	High-level input current	V_I=3V			10	μA
I_{IL}	Low-level input current	V_I=1V			−100	μA
I_{CC}	Supply current	V_{CC}=13V, V_{IA}=3V, V_{IB}=0V, output opened			28	mA

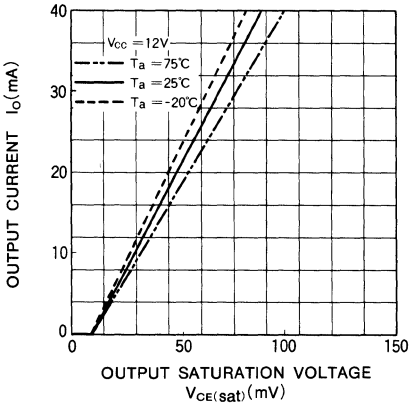
* : A typical value at T_a=25℃.

TYPICAL CHARACTERISTICS

SOURCE OUTPUT SATURATION CHARACTERISTICS



SINK OUTPUT SATURATION CHARACTERISTICS



M54573L

TUNER BAND DECODER/DRIVER

DESCRIPTION

The M54573L is a semiconductor integrated circuit capable of switching three bands in TV and VTR tuners.

FEATURES

- Low output saturation voltage ($V_{CE(sat)} \leqq 0.5V$ at $I_O = -30mA$).
- High output sustaining voltage ($BV_{CEO} \geqq 28V$)

APPLICATION

Switching bands in TV and VTR tuners

FUNCTION

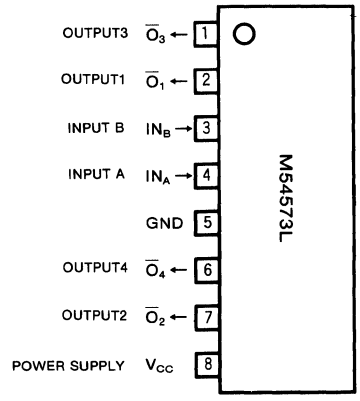
The M54573L is an IC suitable for three-band switching in TV and VTR tuners. Since the output (outputs 1~3) drives the power supply of each tuner band, a low saturation voltage ($V_{CC} - V_O$) becomes necessary. This need is satisfied through a first stage configured of PNP transistors.

Output 4 can be used for changing modes with the same power supply as the NPN transistor has an open collector output.

The input mode can be switched between three modes as shown in the truth table. The "o", "1" mode and the "1", "1" mode are the same modes.

The selection mode can be altered by making an OR connection on outputs 1~3.

PIN CONFIGURATIONS (TOP VIEW)



Outline 8P5

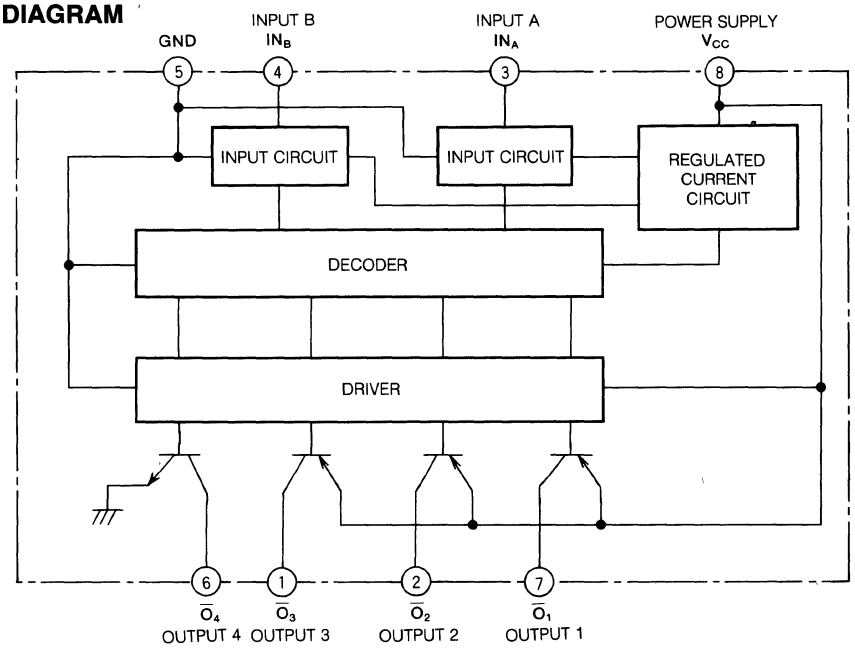
TRUTH TABLE

Input		Output			
IN_A	IN_B	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$
0	0	1	Z	Z	0
0	1	Z	Z	1	0
1	0	Z	1	Z	Z
1	1	Z	Z	1	0

Input "0" = 1V (max.)
"1" = 3V (min.)

Output "0" = current sink
"1" = current source
"Z" = high impedance

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		18	V
V_{CEO}	Output sustaining voltage		−0.5～+28	V
V_I	Input voltage		18	V
I_{SO}	Output source current	$\overline{O1}$～$\overline{O3}$	−40	mA
I_{SI}	Output sink current	$\overline{O4}$	40	mA
Topr	Operating temperature		−10～+60	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 25℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		12		15	V
V_{CEO}	Output sustaining voltage		0		25	V
I_{SO}	Output source current	$\overline{O1}$～$\overline{O3}$	0		−30	mA
I_{SI}	Output sink current	$\overline{O4}$	0		30	mA
V_{IH}	High-level input voltage		3		V_{CC}	V
V_{IL}	Low-level input voltage		0		1	V

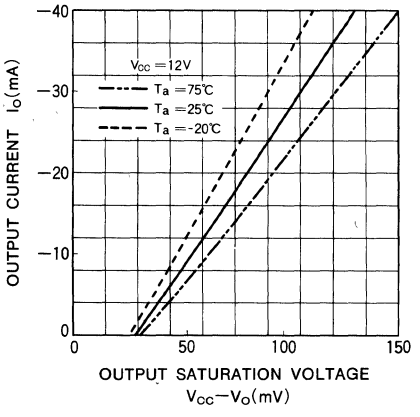
ELECTRICAL CHARACTERISTICS (T_a = 25℃, V_{CC} = 12V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{SO(leak)}$	Source output leakage current	V_{SO}=−12V			−100	μA
$I_{SI(leak)}$	Sink output leakage current	V_{SI}=25V			100	μA
V_{SOH}	Source output High-level voltage	I_{SO}=−30mA	11.5	11.8		V
V_{SIL}	Sink output Low-level voltage	I_{SI}=30mA		0.2	0.5	V
I_{IH}	High-level input current	V_I=3V			10	μA
I_{IL}	Low-level input current	V_I=1V			−100	μA
I_{CC}	Supply current	V_{CC}=13V, V_{IA}=3V, V_{IB}=0V, output opened			28	mA

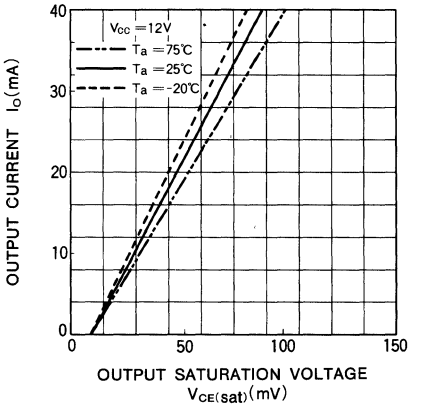
* : A typical value at T_a=25℃

TYPICAL CHARACTERISTICS

SOURCE OUTPUT SATURATION CHARACTERISTICS



SINK OUTPUT SATURATION CHARACTERISTICS



MITSUBISHI ELECTRIC

M54574P

4-UNIT 700mA TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54574P is a semiconductor integrated circuit, consisting of four transistor circuits. Each circuit employs PNP and NPN transistors in a high-gain driver configuration.

FEATURES

- High withstand voltage ($BV_{CEO} \geqq 40V$)
- Large drive current (Ic (max) =700mA)
- Built-in clamp diode
- Can be driven by the output of NMOS ICs
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATIONS

Drivers for relays and small printers; digit drivers for LED displays and other display devices; power amplifiers

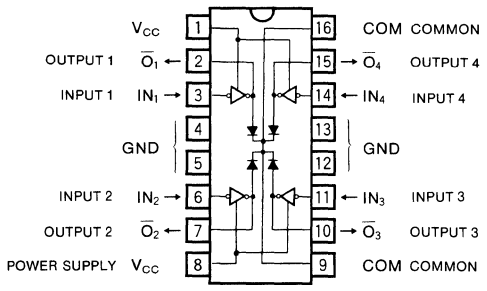
FUNCTION

Each of the four circuits consists of a PNP transistor connected to the input through a 10k_Ω resistor and two NPN transistors at the output.

A clamp diode is connected between the output and COM pins as a spike-killer.

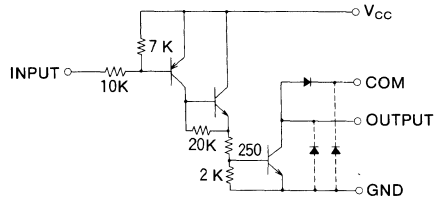
The maximum collector current is 700mA and the maximum collector-to-emitter voltage is 40V. The device operates on a low-level input.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



Resistance unit : Ω

Note 1. COM, V_{CC}, GND pins are shared by all circuits

2. The diodes shown by broken lines are parasitic and must not be used

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5+10	V
V_{CEO}	Collector—to—emitter voltage		−0.5∼+40	V
V_I	Input voltage		0∼V_{CC}	V
I_C	Collector current		700	mA
V_R	Clamp diode reverse voltage		40	V
P_d	Power dissipation	T_a=25℃	1.92	W
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
I_C	Collecter current (per circuit, all circuits conducting simultaneously)	V_{CC}=6V, V_{IN}=1.4V Duty cycle less than 50%			400	mA
V_{IH}	High-level input voltage	I_C=50μA, V_{CC}=5V	V_{CC}−0.7		V_{CC}	V
V_{IL}	Low-level input voltage	I_C=400mA, V_{CC}=5V	0		V_{CC}−3.6	V

4-UNIT 700mA TRANSISTOR ARRAY WITH CLAMP DIODE

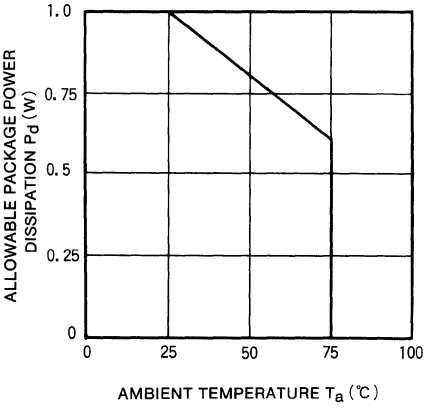
ELECTRICAL CHARACTERISTICS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ*	Max	
$V_{BR(CEO)}$	Collector—to—emitter breakdown voltage	I_{CEO}=100μA, V_{CC}=5V, V_{IN}=4.3V	40			V
$V_{CE(sat)}$	Collector—to—emitter saturation voltage	I_C=400mA, V_{CC}=5V, V_{IN}=1.4V			0.5	V
I_{CC}	Supply current	All circuits conducting simultaneously			150	mA
V_{IN}	Input current	V_{IN}=V_{CC}−3.6V, V_{CC}=5V	−170	−290	−500	μA
V_F	Clamp diode forward current	I_F=700mA		1.5	2.4	V
I_R	Clamp diode reverse current	V_F=40V			100	μA
h_{FE}	DC current amplification	V_{CE}=4V, I_C=400mA, V_{CC}=10V T_a=25℃	1000	2500		—

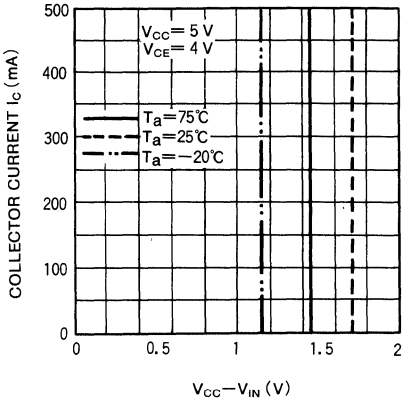
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERRISTICS

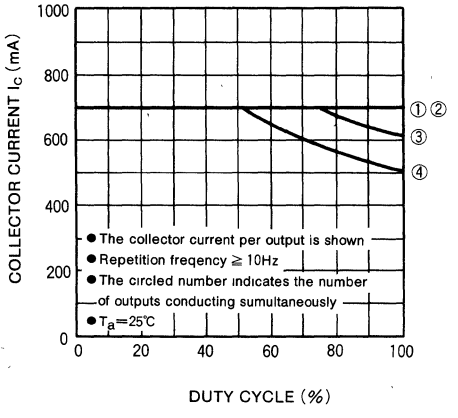
ALLOWABLE AVERAGE POWER DISSIPATION



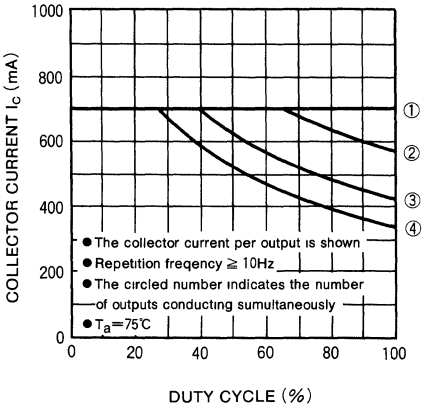
OUTPUT CURRENT CHARACTERISTICS



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



M54575P

8-UNIT 150mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

DESCRIPTION

The M54575P is a semiconductor integrated circuit, consisting of eight sink drivers. Each employs PNP and NPN transistors to form a high-current gain driver.

FEATURES

- Medium withstand voltage ($BV_{CEO} \geqq 25V$)
- Large drive current (Ic (max) =150mA)
- Built-in clamp diode
- Can be driven by the output of NMOS ICs
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATIONS

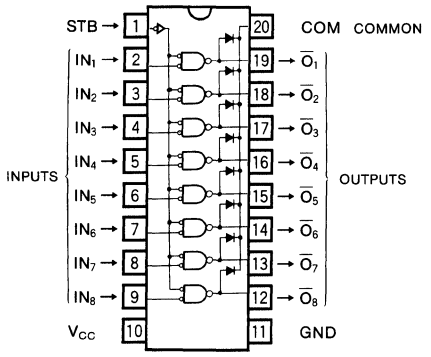
Drivers for relays and small printers; digit drivers for LED displays and other display devices.

FUNCTION

Each of the eight circuits consists of a PNP transistor connected to the input through a 4.8k_Ω resistor, an NPN output transistor, and another pair of transistors at the strobe input. A clamp diode is provided as a spike killer. The emitter of the output transistor is connected to GND (pin 11), the strobe input to pin 1, the clamp diode to COM (pin 20) and V_{CC} to pin 10.

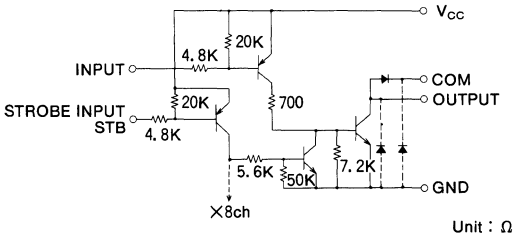
The maximum collector current is 150mA and the maximum collector-to-emitter voltage is 25V. The input voltage range is O to 10V.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

CIRCUIT SCHEMATIC



Unit : Ω

Note 1. COM, STB, V_{CC} and GND pins are shared by all circuits

2. The diodes shown by broken lines are parasitic and must not be used

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+10	V
V_{CEO}	Collector—to—emitter voltage		25	V
V_I	Input voltage		0∼V_{CC}	V
I_C	Collector current		150	mA
V_R	Clamp diode reverse voltage		25	V
P_d	Power dissipation	T_a=25℃	580	mV
T_{opr}	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		1.2	3	6	V
I_C	Collecter current (per channel current)	V_{CC}=3V Percent duty cycle less than 80%	0		100	mA
V_{IH}	High-level input current		V_{CC}−0.4		V_{CC}	V
V_{IL}	Low-level input current		0		V_{CC}−1.2	V

8-UNIT 150mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

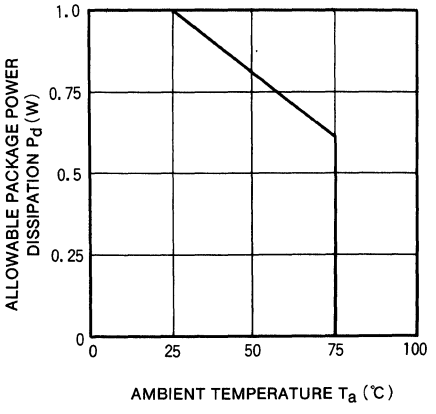
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ*	Max	
$V_{BR(CEO)}$	Collector—to—emitter breakdown voltage	I_{CEO}=100μA, V_{CC}=10V V_{IN}=V_{STB}=9.6V		25			V
$V_{CE(sat)}$	Collector—to—emitter saturation voltage	I_C=100mA, V_{CC}=3V V_{IN}=1V, V_{STB}=2.6V			0.2	0.5	V
I_{CC}	Supply current	Output per channel I_C=0mA V_{STB}=V_{CC}	V_{CC}=6V V_{IN}=1V		7.6	17.0	mA
			V_{CC}=3V V_{IN}=1V		3.3	7.0	
V_{IL}	Low-level input voltage	V_{CC}=3V, V_{IL}=1V, I_C=0mA		−100	−270	−500	μA
		V_{CC}=6V, V_{IL}=0V, I_C=0mA			−1.1	−2.0	mA
V_F	Clamp diode forward current	I_F=150mA			1.5	2.4	V
I_R	Clamp diode reverse current	V_R=25V				100	μA
h_{FE}	DC current amplification	V_{CE}=4V, I_C=100mA, V_{CC}=10V T_a=25℃, V_{STB}=V_{CC}		1000	2500		—

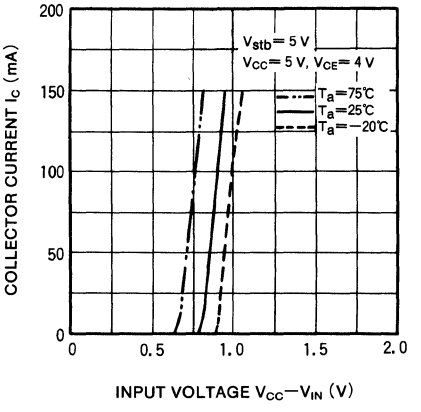
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

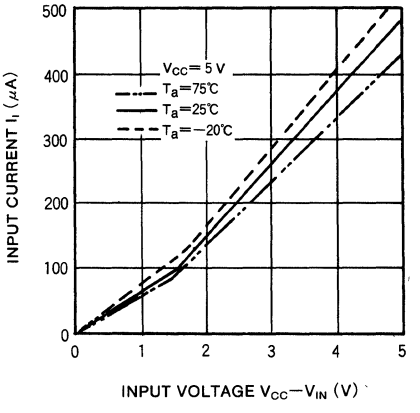
ALLOWABLE AVERAGE POWOR DISSIPATION



OUTPUT CURRENT CHARACTERISTICS



INPUT CHARACTERISTICS



M54576P, FP

7-UNIT 30mA TRANSISTOR ARRAY ("L" ACTIVE INPUT)

DESCRIPTION

The M54576P, FP, 7-channel sink driver, consists of 28 NPN transistors connected to form high current gain driver pairs.

FEATURES

- 30V output breakdown
- 30mA output sink current capability
- CMOS compatible input
- Low output saturation voltage
- Wide operating temperature range (T_a = −20∼+75℃)

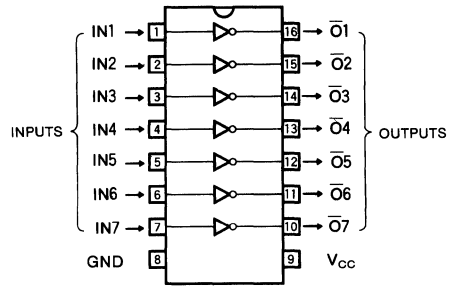
APPLICATION

LED or incandescent display digit driver

FUNCTION

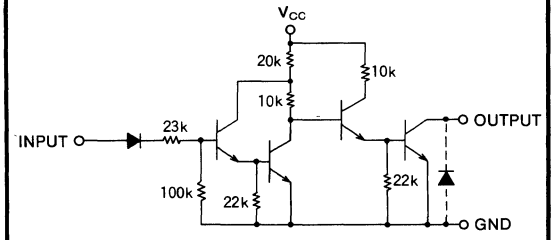
The M54576P, FP is comprised of seven NPN invertors with diodes and 23k Ω resistors in series to the input and non darlington NPN sink drivers. The output is turned ON by switching the input low. The outputs are capable of sinking 30mA and will withstand 30V in the OFF state. The M54576FP features a small flat mold package.

PIN CONFIGURATION (TOP VIEW)



Outline 16P2 (M54576FP)
Outline 16P4 (M54576P)

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+13	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+30	V
I_C	Collector current	Transistor ON	30	mA
V_I	Input voltage		−20∼+13	V
P_d	Power dissipation	T_a=25℃	1.47/0.56	W
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	13	V
I_C	Collector current per channel		0	10	20	mA
V_{IH}	"H" Input voltage		3		V_{CC}	V
V_{IL}	"L" Input voltage	I_C=20mA	0		1	V

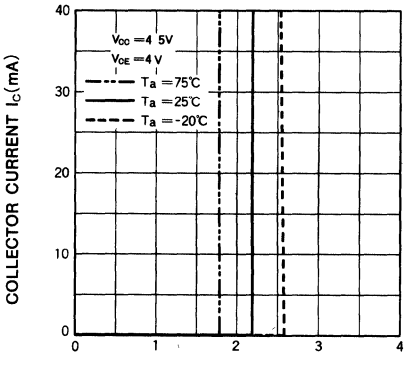
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=30V, V_I=3V, V_{CC}=6V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_{CC}=4.5V, V_I=1V, I_C=10mA		0.02	0.25	V
		V_{CC}=6V, V_I=1V, I_C=20mA		0.04	0.35	
I_I	Input current	V_{CC}=4.5V, V_I=3V	30	60	90	μA
I_{CC}	Supply current	V_{CC}=4.5V, V_I=1V			6.3	mA
		V_{CC}=13V, V_I=1V			18	
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=4.5V, I_C=20mA, T_a=25℃	500	1200		—

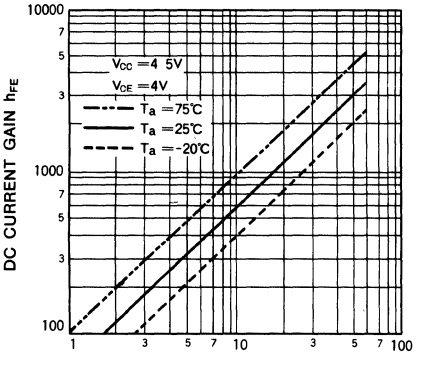
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



MITSUBISHI ELECTRIC

M54577P,FP

7-UNIT 30mA TRANSISTOR ARRAY

DESCRIPTION

The M54577P, FP, 7-channel sink driver, consists of 14 NPN transistors connected to form high current gain driver pairs.

FEATURES

- Output breakdown voltage to 30V
- Output sink current to 30mA
- PMOS, CMOS Compatible input
- Low output saturation voltage
- Wide operating temperature range (T_a = −20∼+75℃)

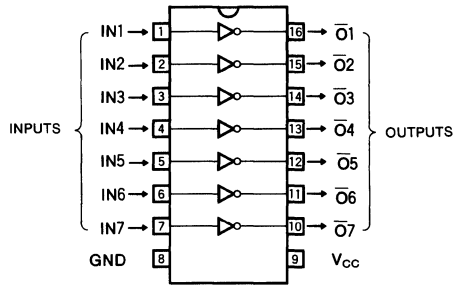
APPLICATION

LED or incandescent display digit driver

FUNCTION

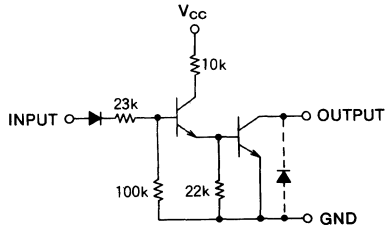
The M54577P, FP uses a predriver stage with a diode and 23kΩ resistor in series to the input. The power supply of the predrivers is connected to pin 9 . The outputs are capable of sinking 30mA and will withstand 30V in the OFF state. The M54577FP features a small flat mold package.

PIN CONFIGURATION (TOP VIEW)



Outline 16P2 (M54577FP)
Outline 16P4 (M54577P)

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+13	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+30	V
I_C	Collector current	Transistor ON	30	mA
V_I	Input voltage		−20∼+13	V
T_{opr}	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	13	V
I_C	Collector current per channel		0	10	20	mA
V_{IH}	"H" Input voltage	I_C=20mA	3		V_{CC}	V
V_{IL}	"L" Input voltage		0		1	V

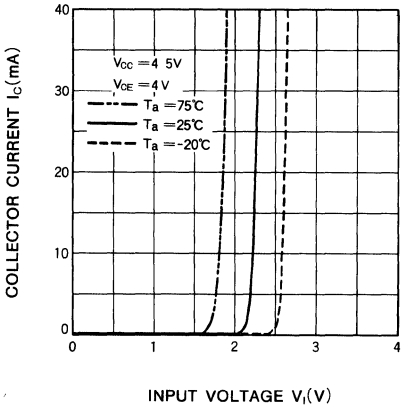
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leak current	V_{CE}=30 V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_{CC}=4.5 V, V_I=3 V, I_C=10 mA			0.25	V
		V_{CC}=6 V, V_I=3 V, I_C=20 mA			0.35	
I_I	Input current	V_{CC}=4.5 V, V_I=3 V	30		90	μA
I_{CC}	Supply current per channel (an only output conducting)	V_{CC}=4.5 V, V_I=3 V		0.4	0.9	mA
		V_{CC}=13 V, V_I=3 V		1.3	2.3	
h_{FE}	DC forward current gain	V_{CE}=4 V, V_{CC}=4.5 V, I_C=20 mA, T_a=25℃	500	1200		—

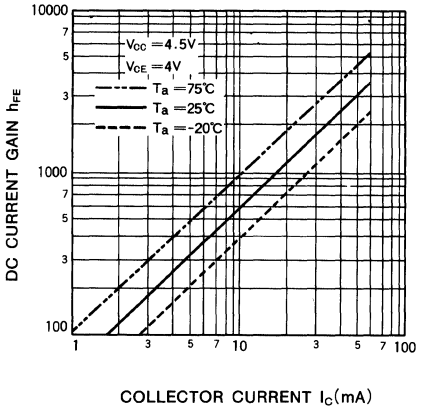
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



MITSUBISHI ELECTRIC

M54578P

6-UNIT 700mA TRANSISTOR ARRAY WITH CLAMP DIODE AND STROBE

DESCRIPTION

The M54578P, 6-channel sink driver, consists of 12 NPN transistors connected to form high current gain driver pairs.

FEATURES

- 20V breakdown
- High output sink current to 700mA
- PMOS Compatible
- Wide operating temperature range (T_a = −20～+75℃)

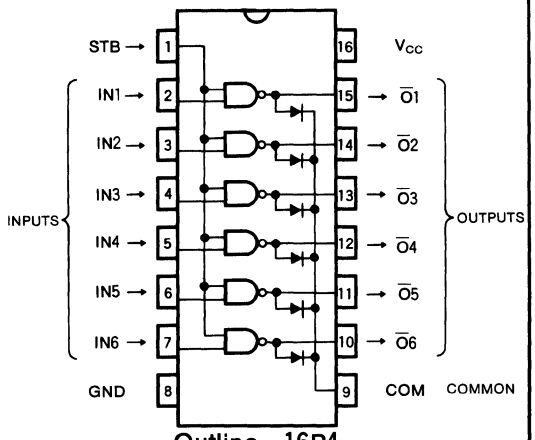
APPLICATION

Relay and printer driver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

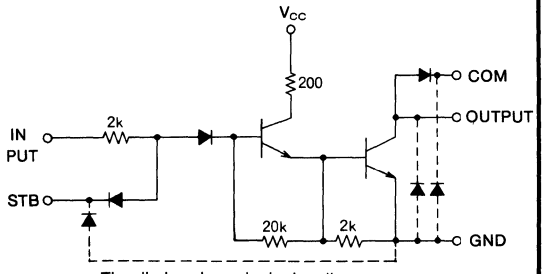
The M54578P uses a predriver stage. Each input has a diode and 2 kΩ resistor in series to allow a negative voltage input. All input can be controlled simultaneously by a strobe input at pin 1 . The power supply of the predrivers is connected to pin 16. Each output has an integral diode for inductive load transient suppression and the cathodes of the diodes are connected to pin 9 . All emitters and the substrate are connected together to pin 8 . The outputs are capable of sinking 700mA and will withstand 20V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5～+20	V
I_C	Collector current	Transistor ON	700	mA
V_I	Input voltage		−25～+20	V
$V_{I(STB)}$	Strobo input voltage		−0.5～+20	V
$V_{R(D)}$	Clamp diode reverse voltage		20	V
$I_{F(D)}$	Clamp diode forward current	Pulse width≦35ms, Duty cycle≦5%	700	mA
			350	
P_d	Power dissipation	T_a=25℃	1.47	W
T_{opr}	Operating temperature		−20～+75	℃
T_{stg}	Storage temperature		−55～+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3	5	8	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	The three outputs conducting simultaneously Percent duty cycle less than 20%	0		700	mA
		The three outputs conducting simultaneously Percent duty cycle less than 90%	0		200	
$V_{IH(STB)}$	"H" Input voltage (strobe input)		2.4		V_{CC}	V
$V_{IL(STB)}$	"L" Input voltage (strobe input)		0		0.2	V
V_{IH}	"H" Input voltage	I_C=450mA, V_{CC}=5V	3.5		V_{CC}	V
		I_C=700mA, V_{CC}=6V	5		V_{CC}	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.8	V

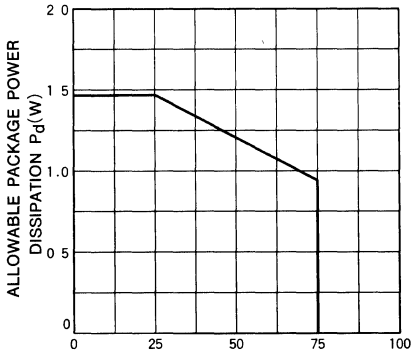
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	V_{CC}=7V, $V_{I(STB)}$=0.4V, V_I=3.5V, I_{CEO}=100μA		20			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC}=5V, V_I=3.5V	I_C=450mA		0.5	0.8	V
			I_C=200mA		0.23	0.45	
I_I	Input current	V_{CC}=7V, V_I=3.5V, $V_{I(STB)}$=2.4V			0.6	1.4	mA
I_R	Input leakage current	V_{CC}=7V, V_R=−25V				−20	μA
$I_{I(STB)}$	Strobe input current	V_{CC}=7V, $V_{I(STB)}$=0.4V, V_I=3.5V (all input)			−7.2	−10.7	mA
$I_{R(STB)}$	Strobe input leakage current	V_{CC}=7V, V_I=0V, $V_{I(STB)}$=20V				20	μA
$V_{F(D)}$	Clamp diode forward current	$I_{F(D)}$=600mA			1.6	5	V
$V_{R(D)}$	Clamp diode reverse voltage	$I_{R(D)}$=100μA		20			V
I_{CC}	Supply current	V_{CC}=8V, $V_{I(STB)}$=2.4V, V_I=3.5V (all input)			220	320	mA
h_{FE}	DC forward current gain	V_{CC}=5V, V_{CE}=4V, I_C=450mA, T_a=25℃		2000	10000		—

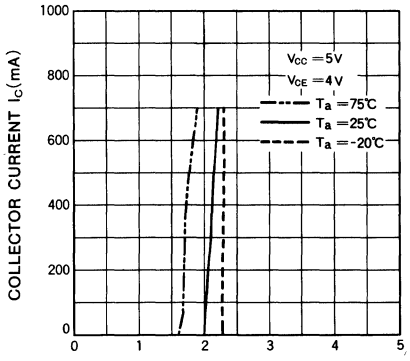
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

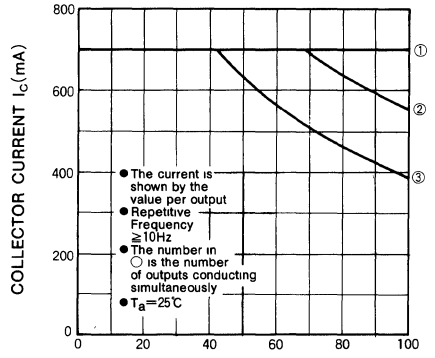
ALLOWABLE AVERAGE POWER DISSIPATION



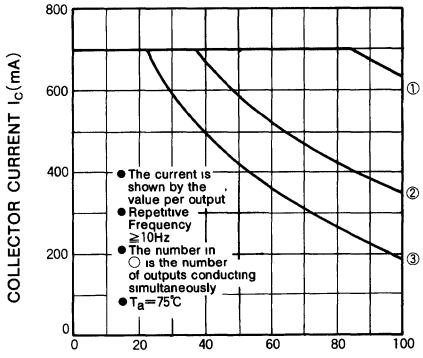
OUTPUT CURRENT CHARACTERISTICS



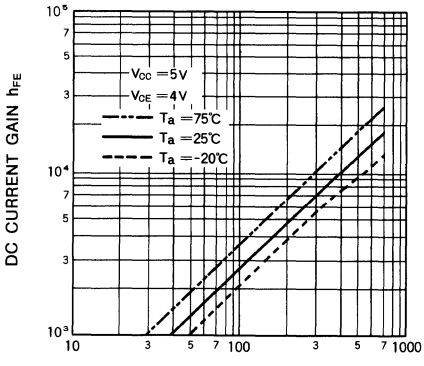
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54580P

7-UNIT 150mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54580P, 7-channel source driver, consists of 7 PNP and 7 NPN transistors connected to form high current gain driver with PNP action.

FEATURES

- High output sustaining voltage to 50V
- High output source current to 150mA
- Wide operating temperature range (T_a = −20∼+75℃)

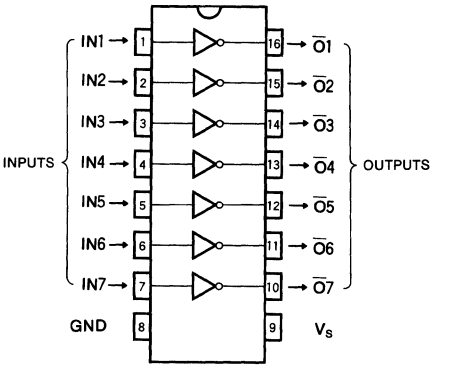
APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

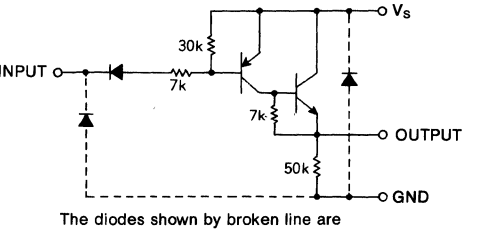
The M54580P is comprised of seven PNP-NPN darlington source driver pairs with a diode and 7 kΩ resistor in series to the input. The output is turned ON by switching the input low. Each output has 50kΩ pull-down resistor suitable for driving fluorescent displays. The outputs are capable of driving 100mA and are rated for operation with output voltage up to 50V.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_S	Supply voltage		−0.5∼+50	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+50	V
V_I	Input voltage		0∼V_S	V
I_O	Output current per channel	Transistor OFF	−150	mA
P_d	Power dissipation	T_a =25℃	1.47	W
T_{opr}	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

7-UNIT 150mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		4		50	V
I_O	Output current per channel	All outputs conducting simultaneously Percent duty cycle less than 85%	0		−100	mA
		All outputs conducting simultaneously Percent duty cycle less than 100%	0		−50	
V_{IH}	"H" Input voltage	$I_{O(leak)}$=50μA	V_S−0.4		V_S	V
V_{IL}	"L" Input voltage	I_O =−100mA	0		V_S−3.2	V

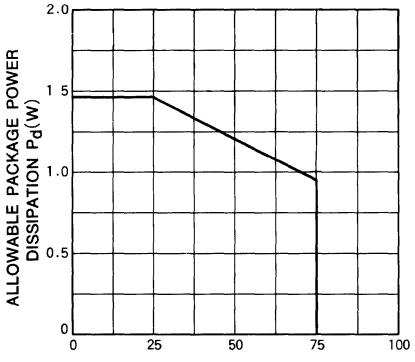
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO} = 100μA		50			V
$V_{CE(sat)}$	Output saturation voltage	$V_I = V_S$−3.2V	I_O =−100mA		0.9	1.5	V
			I_O =−50mA		0.8	1.2	
I_I	Input current	$V_I = V_S$−3.5V			−0.3	−0.6	mA
		$V_I = V_S$−6V			−0.65	−0.95	
I_R	Input leakage current	V_I =40V				100	μA
h_{FE}	DC forward current gain	V_{CE} =4V, V_S =10V, I_C =−100mA, T_a=25°C		800	3000		—

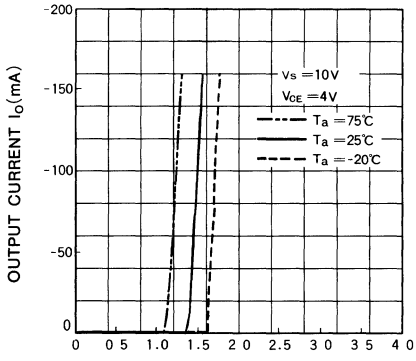
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

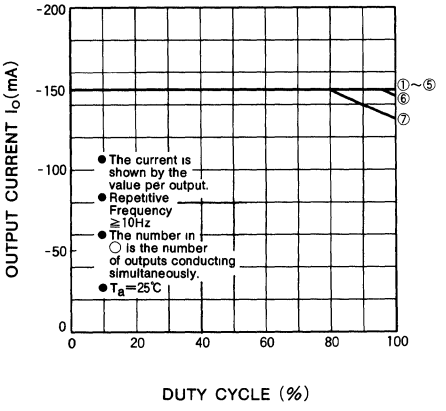


OUTPUT CURRENT CHARACTERISTICS

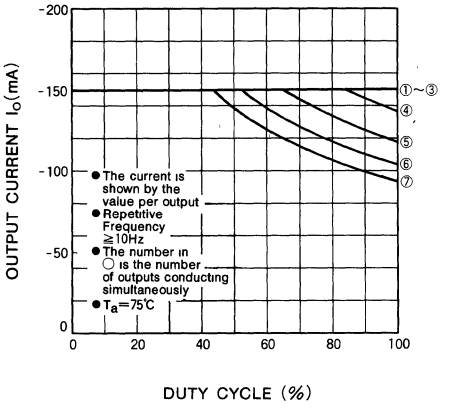


7-UNIT 150mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

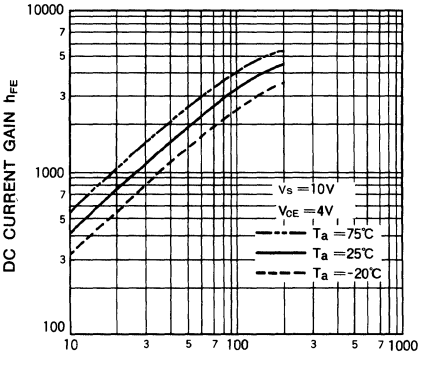
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54581P

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54581P, 8-channel source driver, consists of 8 NPN and 8 PNP source type darlington transistors connected to form high current gain driver.

FEATURES

- High output sustaining voltage to 50V (BV_{CEO}>50V)
- High output source current to 500mA ($I_{O(max)}$=−500mA)
- "L" active input level
- Internal input diode
- Integral clamp diode for transient suppression
- Wide operating temperature range (T_a=−20−+75℃)

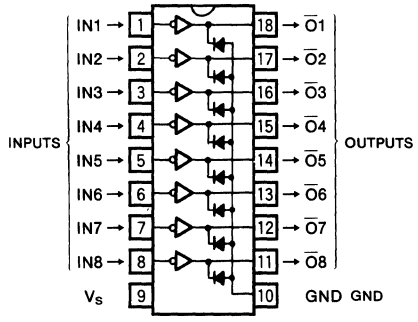
APPLICATION

Relay and printer driver, LED or incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics and interfacing for relay, solenoid or small printer

FUNCTION

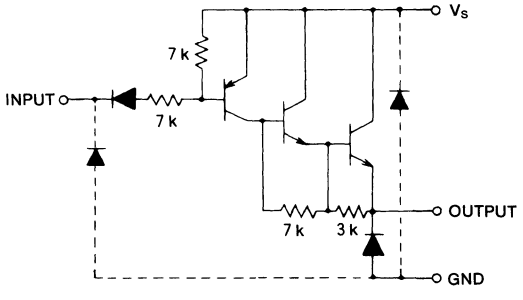
The M54581P is composed of 8 PNP and 8 NPN source type darlington transistors. A diode and a resistor of 7kΩ is connected between the input pin and the base of PNP transistor. The emitter and the collector of NPN transistor are connected to V_S (pin 9), and the output NPN transistors are in darlington configuration. An integral clamp diode is inserted between each output and GND, and V_S (pin 9) and GND (pin 10) are common to the 8 circuits.
The outputs are capable of driving 500mA and are rated for operation with output voltage up to 50V.
The device is activated with "L" level input.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC (EACH CIRCUIT)



V_S and GND are common to the 8 circuits

The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Output is in "L"	−0.5~+50	V
V_S	Supply voltage		−0.5~+50	V
V_I	Input voltage		0~V_S−30	V
I_O	Output current	Per channel current at "H" output	−500	mA
I_F	Clamp diode forward current	Per channel current	−500	mA
V_R	Clamp diode reverse voltage		−0.5~+50	V
Pd	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20~+75	℃
Tstg	Storage temperature		−55~+125	℃

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		50	V
I_O	Output current per channel	Percent duty cycle less than 8%	0		−350	mA
		Percent duty cycle less than 55%	0		−100	
V_{IH}	"H" Input voltage	$I_{O(leak)}$=−50μA	V_S−0.7		V_S	V
V_{IL}	"L" Input voltage	I_O=−350mA	0		V_S−3.6	V

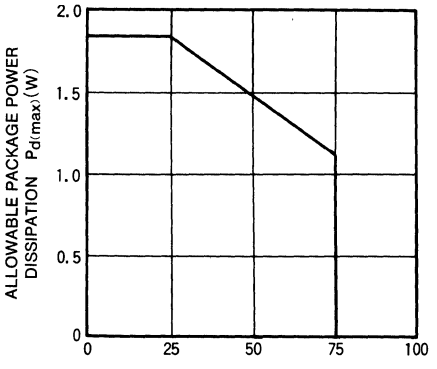
ELECTRICAL CHARACTERISTICS (T_a=−20+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
I_{CEO}	Output leakage current	V_{CEO}=50V			−100	μA
$V_{CE(sat)}$	Output saturation voltage	V_i=V_S−3.2V, I_O=−100mA		1.6	2.0	V
		V_i=V_S−3.6V, I_O=−350mA		1.8	2.4	
I_I	Input current	V_i=V_S−3.6V		−320	−600	μA
		V_i=V_S−15V			−3.2	mA
V_R	Clamp diode reverse voltage	I_R=100μA	50			V
V_F	Clamp diode forward voltage	I_F=−350mA			−2.4	V

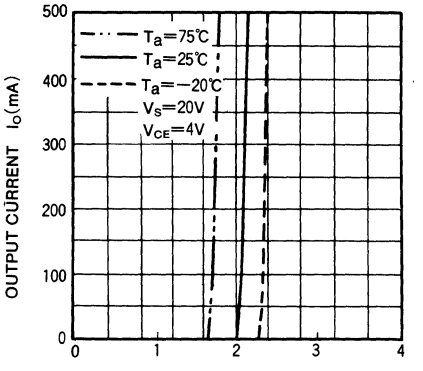
* : A Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

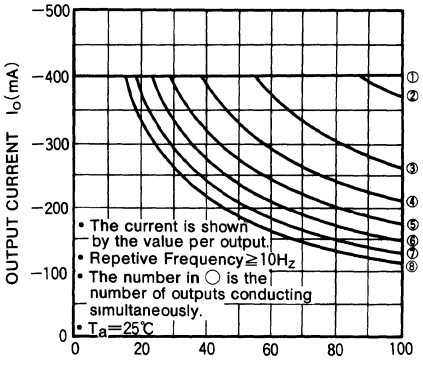


OUTPUT CURRENT CHARACTERISTICS

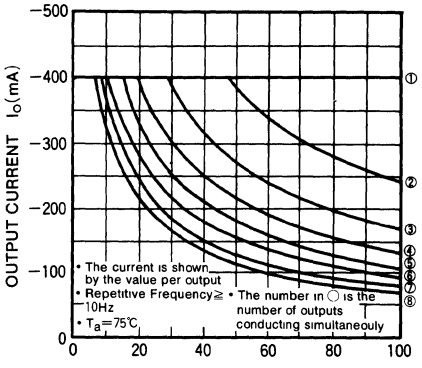


MITSUBISHI ELECTRIC

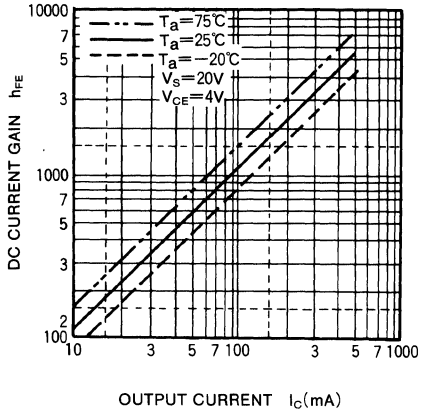
ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



CURRENT GAIN VS
OUTPUT CURRENT



M54583P

8-UNIT 400mA DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54583P, 8-channel source driver, is composed of 16 NPN and PNP current sink darlington transistors which form high current gain driver pairs at low input current.

FEATURES

- High output sustaining voltage to 50V
- High output source current to 400mA
- "L" active level input
- Internal input diodes
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

Interfacing for microcomputer and high voltage and high current driver system, Interfacing for standard MOS/BIPOLAR logics, Relay

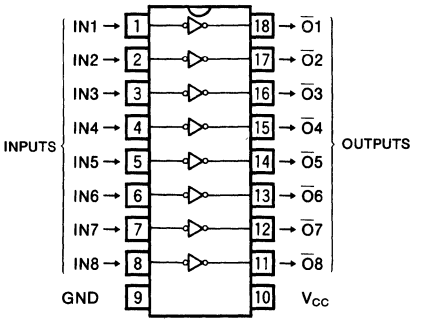
FUNCTION

The driver of the M54583P is composed of an input circuit of the M54523P with additional PNP transistors and "L" active input. A resistor of 7kΩ is connected between the input and the base of PNP transistors. The input diode is intended to prevent the flow of current from the input to the V_{CC}. Without this diode, the current flows from "H" input to the V_{CC} and the "L" input circuit is activated, in such a case where one of the inputs of the 8 circuits is "H" and the others are "L" to save power consumption. The diode is inserted to prevent such misoperation.

The outputs are capable of driving 400mA and are rated for operation with output voltage up to 50V.

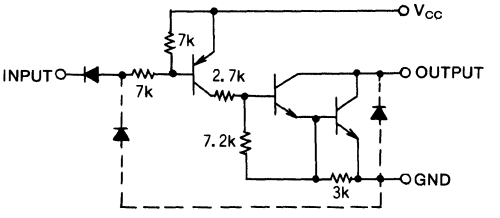
This device is most suitable for a driver using NMOS IC output, especially for the driver of current sink.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC (EACH CIRCUIT)



V_{CC} and GND are common to the 8 pairs.
The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+10	V
V_{CEO}	Ounput sustaining voltage	Transistor OFF	−0.5∼+50	V
V_I	Input voltage		−0.5∼V_{CC}	V
I_C	Collector current per channel	Transistor ON	400	mA
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

MITSUBISHI ELECTRIC

8-UNIT 400mA DARLINGTON TRANSISTOR ARRAY

RECOMMENDED OPERATING CONDITONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	8	V
I_C	Collector current per channel	Percent duty cycle less than 10%, V_{CC}=5V	0		350	mA
		Percent duty cycle less than 34%, V_{CC}=5V	0		200	
V_{IH}	"H" Input voltage	$I_{O(leak)}$≦50μA	V_{CC}−0.7		V_{CC}	V
V_{IL}	"L" Input voltage	I_C≦350mA	0		V_{CC}−3.6	V

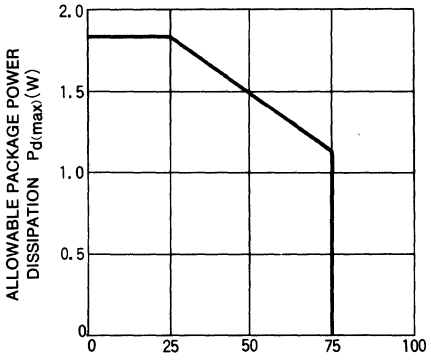
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CEO}=50V				100	μA
$V_{CE(sat)}$	Output saturation voltage	V_i=V_{CC}−3.6V	I_C=350mA		1.1	2.2	V
			I_C=200mA		0.98	1.6	
I_I	Input current	V_i=V_{CC}−3.6V			−320	−600	μA
I_{CC}	Supply current (an only input)	V_{CC}=5V, V_i=V_{CC}−3.6V				3	mA
h_{FE}	DC forward current gain	V_{CE}=4V, V_{CC}=5V, I_C=350mA, T_a=25℃		2000			—

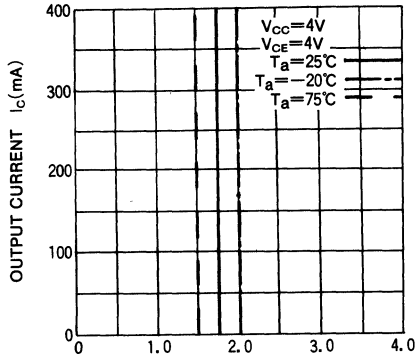
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

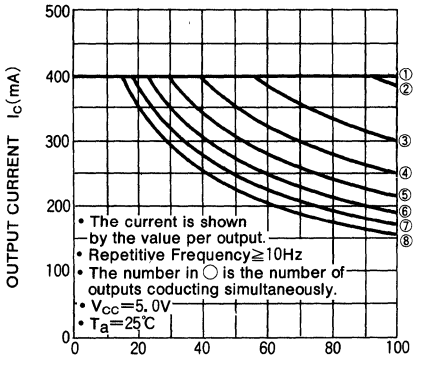
ALLOWABLE AVERAGE POWER DISSIPATION



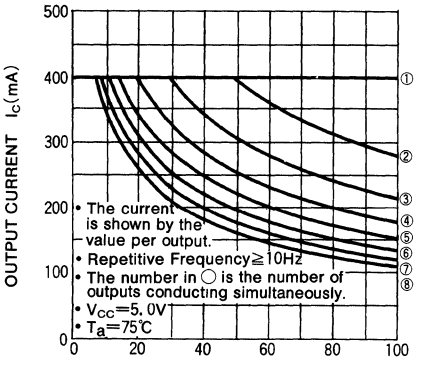
OUTPUT CURRENT CHARACTERISTICS



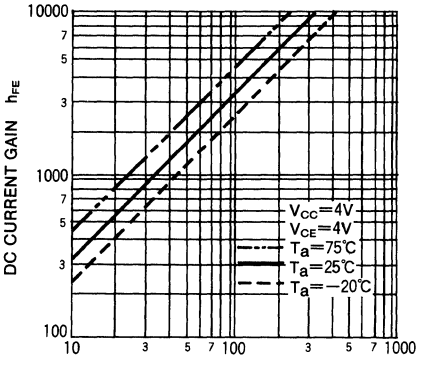
ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



M54584P

8-UNIT 350mA TRANSISTOR ARRAY

DESCRIPTION

The M54584P, 8-channel sink driver, consists of 16 NPN transistors connected to form high current gain driver pairs with low input current.

FEATURES

- High output sustaining voltage to 20V
- High output sink current to 350mA
- PMOS IC output for drive
- Low output saturation voltage
  ($V_{CE(sat)}$=0.5V at I_C=250mA)
- Wide operating temperature range (T_a=−20∼+75℃)

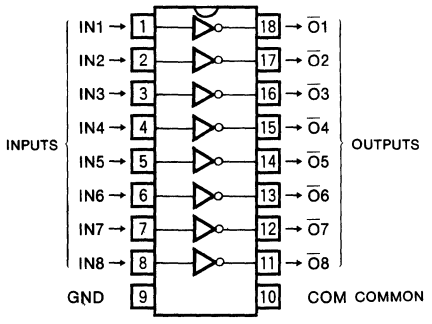
APPLICATION

Relay and thermal printer dot driver, LED or incandescent display digit driver, Interface for MOS-bipolar logic ICs

FUNCTION

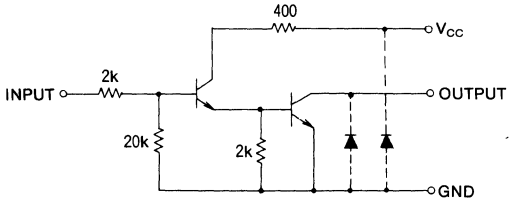
The M54584P is composed of eight NPN transistors with the emitters of output transistors connected to GND pin (pin 9). The collectors of NPN predriver transistors are connected to the V_{CC} (pin 10) via a resistor of 400Ω. The outputs are capable of sinking 350mA and will withstand 20V between collector and emitter.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC (EACH CIRCUIT)



V_{CC} and GND are all common to 8 circuits.
The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+20	V
I_C	Collector current per channel	Transistor ON	350	mA
V_I	Input voltage		−0.5∼+10	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tsqg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		3	5	8	V
V_O	Output voltage		0		20	V
I_C	Collector current per channel	Percent duty cycle less than 45%, V_{CC}=6.5V			250	mA
		Percent duty cycle less than 70%, V_{CC}=6.5V			150	
V_{IH}	"H" Input voltage	I_C≧250mA	3		V_{CC}	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$≧50μA	0		0.4	V

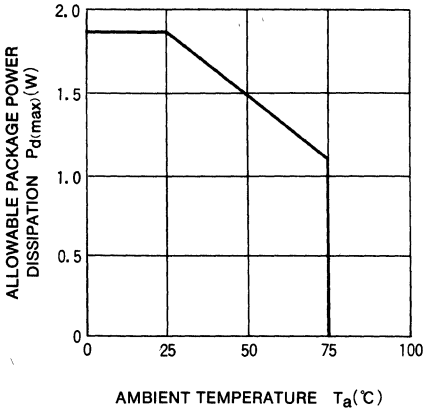
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage voltage	V_{CC}=8V, V_{CE}=20V			100	μA
$V_{CE(sat)}$	Output saturawion voltage	V_{CC}=6.5V, V_I=3V, I_C=250mA		0.3	0.5	V
		V_{CC}=3V, V_I=3V, I_C=150mA		0.17	0.35	
I_I	Input current	V_{CC}=8V, V_I=3V		0.7	1.5	mA
		V_{CC}=8V, V_I=10V		4.3	7.3	
I_{CC}	Supplv current (all output ON)	V_{CC}=8V, V_I=3V			220	mA
h_{FE}	DC forward current transter ratio	V_{CC}=6.5V, V_{CE}=4V, I_C=250mA, T_a=25℃	1000	7000		—

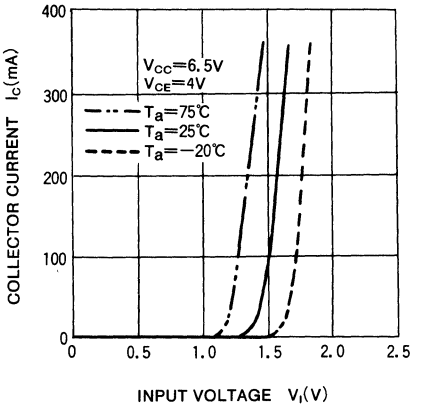
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

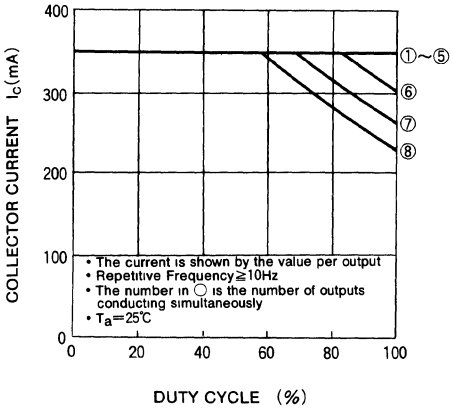


OUTPUT CURRENT CHARACTERISTICS

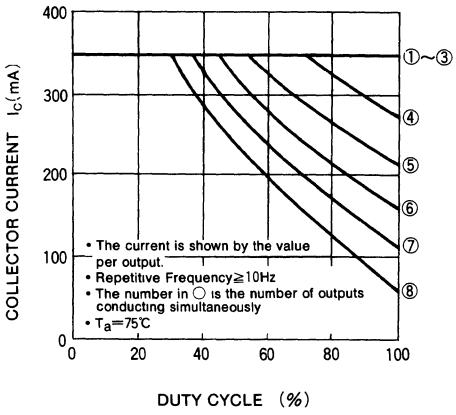


MITSUBISHI ELECTRIC

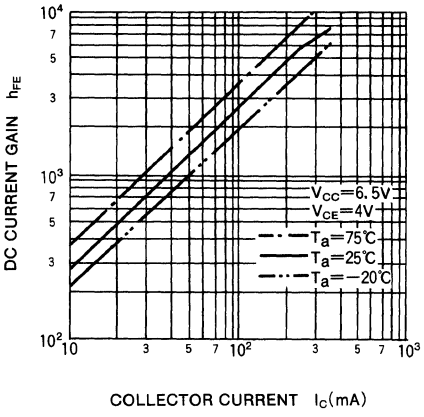
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



CURRENT GAIN CHARACTERISTICS



M54585P

8-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54585P, 8-channel sink driver, consists of 16 NPN darlington transistors with internal clamp diodes connected to form high current gain driver pairs with low input current.

FEATURES

- High output sustaining voltage to 50V
- High output sink current to 500mA
- Built-in clamp diode
- TTL, PMOS IC output for drive
- Wide operating temperature range (T_a=−20∼+75℃)

APPLICATION

Relay and small printer driver, LED or incandescent display digit driver, Output for microcomputer and interface with high voltage system

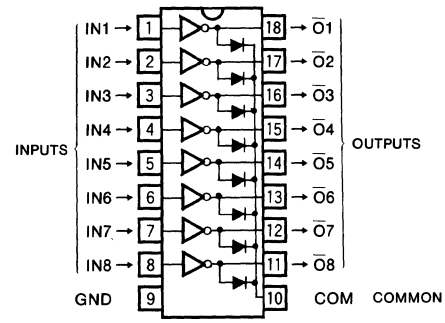
FUNCTION

The M54585P is composed of eight NPN darlington transistor pairs. A resistor of 2.7kΩ is connected between the base of input transistor and the input pin.

A clamp diode for inductive load transient suppression is connected for the output pin (collector) and COM pin (pin 10). All emitters of the output transistors are connected to GND (pin 9).

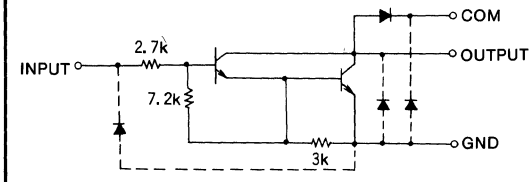
The outputs are capable of sinking 500mA and will withstand 40V between collector and emitter.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC (EACH CIRCUIT)



COM and GND are all common to 8 circuits.
The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20+75℃, unless otherwise noted)

Symbol	Parameteter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+50	V
I_C	Collector current per channel	Transistor ON	500	mA
V_I	Input voltage		−0.5∼+30	V
I_F	Clamp diode forward voltage		500	mA
V_R	Clamp diode reverse current		−0.5∼+50	V
P	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

8-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		50	V
I_I	Collector current per channel	Percent duty cycle less than 6%	0		400	mA
		Percent duty cycle less than 34%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	3.85		30	V
		I_C=200mA	3.4		30	
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.6	V

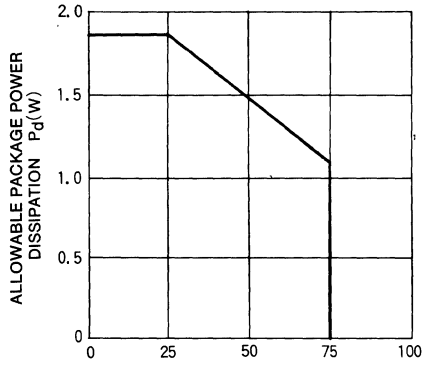
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otterwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=50V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=3.85V, I_C=400mA		1.3	2.4	V
		V_I=3.85V, I_C=200mA		1.0	1.6	
I_I	Input current	V_I=3.85V		0.95	1.8	mA
		V_I=25V		11	18	
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
I_R	Clamp diode reverse voltage	V_R=50V			100	μA
h_{FE}	DC forward current transter ratio	V_{CC}=4V, I_C=350mA, T_a=25℃	1000	2500		—

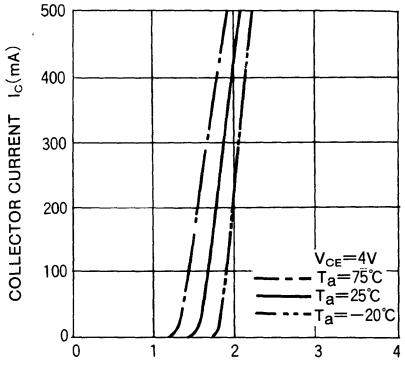
* : Typical values are at T_a=25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

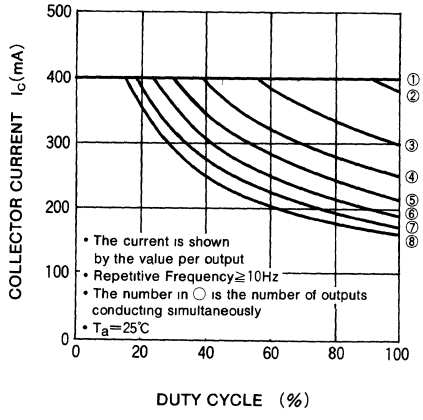


OUTPUT CURRENT CHARACTERISTICS

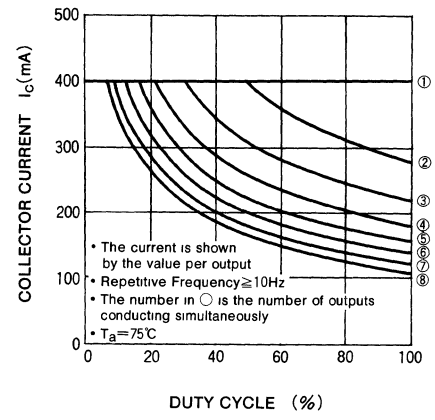


8-UNIT 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

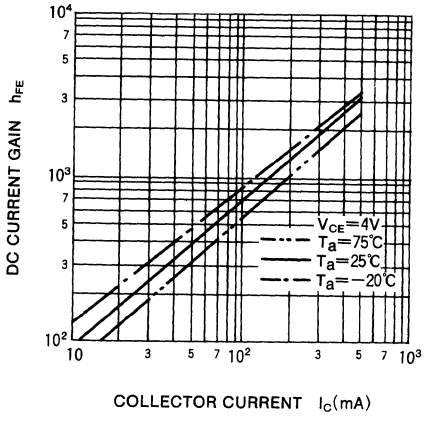
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



CURRENT GAIN CHARACTERISTICS



M54586P

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The 54586P, 8-channel source driver, consists of 8 NPN and 8 PNP source type darlington transistors connected to form high current gain driver.

FEATURES

- High output sustaining voltage to 50V
- High output source current to 500mA
- "L" active input level
- Internal input diode
- Wide operating temperature range (T_a=−20∼+75℃)

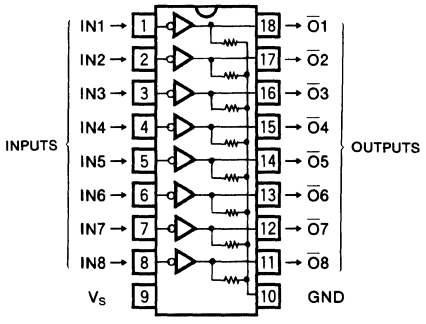
APPLICATION

Relay and printer driver, LED or incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics and interfacing for relay, solenoid or small printer

FUNCTION

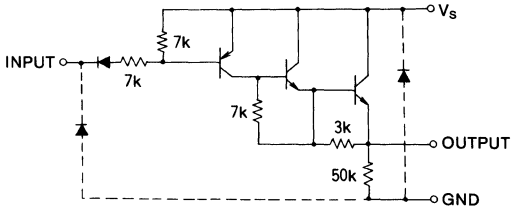
The M54586P is composed of 8 PNP and 8 NPN source type darlington transistors. A diode and a resistor of 7kΩ is connected between the input pin and the base of PNP transistors. The emitter of the transistor and the collector of NPN transistor are connected to V_S (pin 9), and a resistor of 50kΩ is connected between each output pin and GND pin (pin 10).
The outputs are capable of driving 500mA and are rated for operation with ortput voltage up to 50V.
The device is activated with "L" level input.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC (EACH CIRCUIT)



V_S and GND are common to the 8 circuits.
The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_S	Supply voltage		−0.5∼+50	V
V_{CEO}	Output sustaining voltage	Output is in "L"	−0.5∼+50	V
V_I	Input voltage		−0.5∼+V_S	V
I_O	Output current	Per channel current at "H" output	−500	mA
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		4		50	V
I_O	Output current per channel when 8 outputs are conducting simultaneously.	Percent duty cycle less than 8%	0		−350	mA
		Percent duty cycle less than 60%	0		−100	
V_{IH}	"H" Input voltage	$I_{O(leak)}$≧50μA	V_S−0.7		V_S	V
V_{IL}	"L" Input voltage	I_O≧−350mA	0		V_S−3.6	V

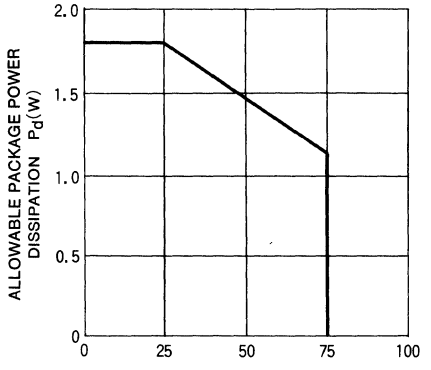
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise notted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage voltage	V_{CEO}=50V			−100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=V_S−3.2V, I_O=−100mA		1.6	2.0	V
		V_I=V_S−3.6V, I_O=−350mA		1.8	2.4	
I_I	Input current	V_I=V_S−3.6V		−320	−600	μA
		V_I=V_S−15V		−1.6	−3.2	mA
h_{FE}	Collector-emitter saturation voltage	V_{CE}=4V, V_S=20V, I_O=−350mA, T_a=25℃	800	3500		—

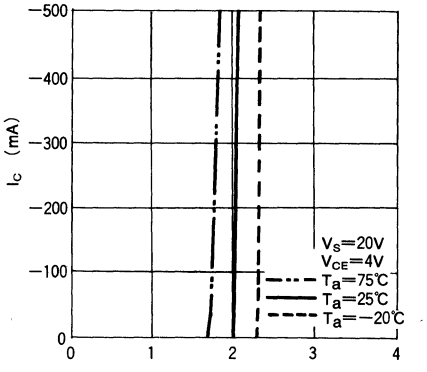
* : Typical values are at T_a=25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



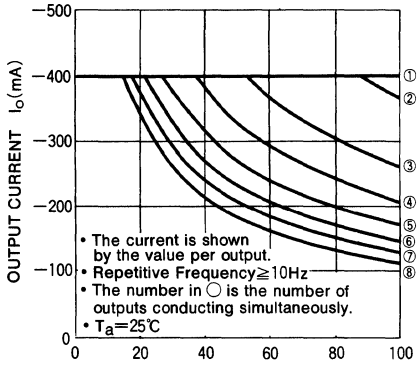
OUTPUT CURRENT CHARACTERISTICS



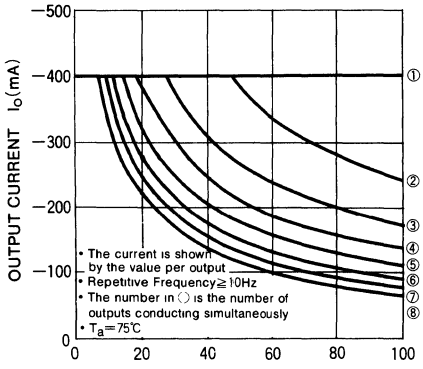
MITSUBISHI ELECTRIC

8-UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

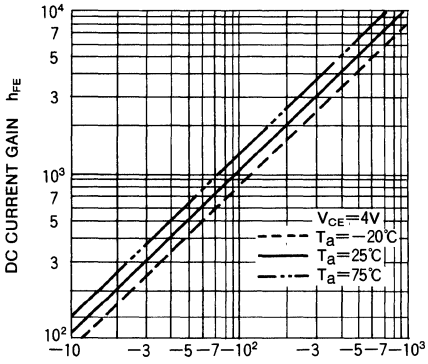
ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



CURRENT GAIN VS
OUTPUT CURRENT



M54590P

8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54590P, 8-channel sink driver, consists of 16 NPN transitors connected to from eight high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output sink current to 500mA
- Integral diodes for transient suppression
- PMOS Compatible input
- Wide operating temperature range (T_a=−20∼+75℃)

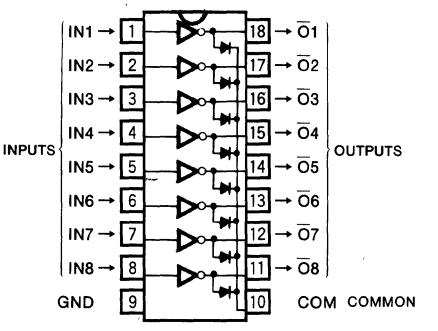
APPLICATION

Relay and printer diver, LED or incandescent display digit driver, Interfacing for standard MOS/BIPOLAR logics.

FUNCTION

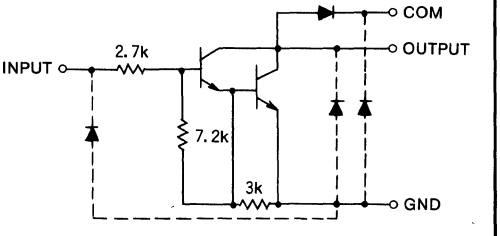
The M54590P is comprised of eight NPN darlington driver pairs with 2.7kΩ series input resistors. Between pin 10 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 9. The outputs are capable of sinking 500mA and will withstand 80V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+80	V
I_C	Collector current	Transistor ON	500	mA
V_I	Input voltage		−0.5∼+30	V
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54590P

8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		80	V
I_C	Collector current per channel	All units ON Percent duty cycle≦6%	0		400	mA
		All units ON Percent duty cycle≦ 34%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	3.85		25	V
		I_C=100mA	3.4		25	
V_{IL}	"L" Input voltage		0		0.6	V

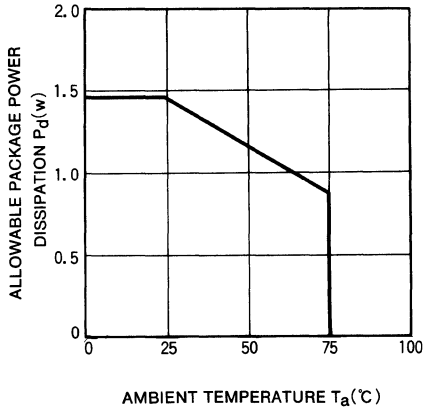
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=80V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=3.85V, I_C=400mA		1.3	2.4	V
		V_I=3.85V, I_C=200mA			1.6	
I_I	Input current	V_I=3.85V		0.95	1.8	mA
		V_I=25V		9	18	
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
I_R	Clamp diode leakage current	V_R=80V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=350mA, T_a=25℃	1000			—

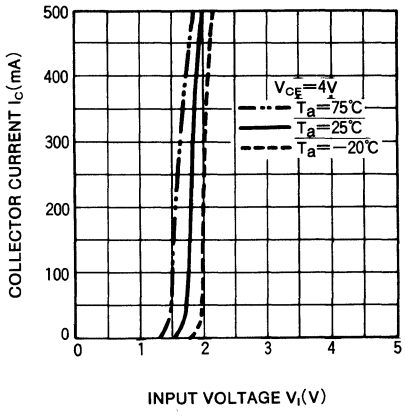
* : A typical value at T_a = 25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

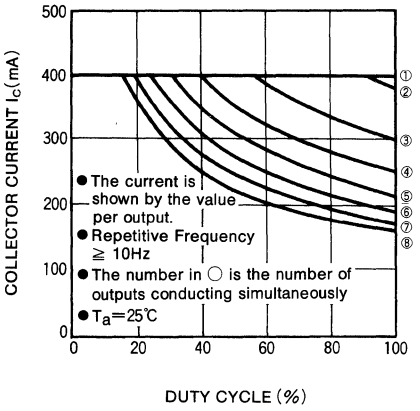


OUTPUT CURRENT CHARACTERISTICS

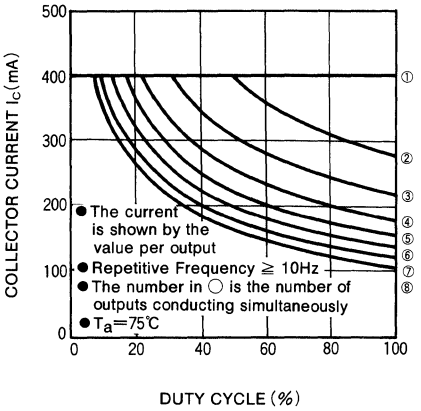


8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

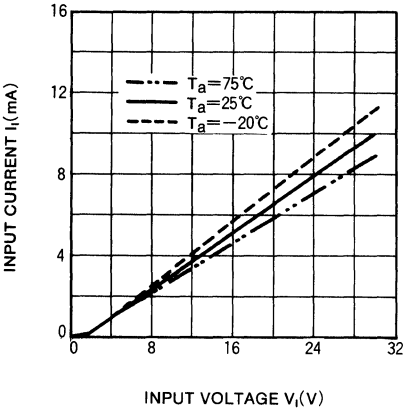
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



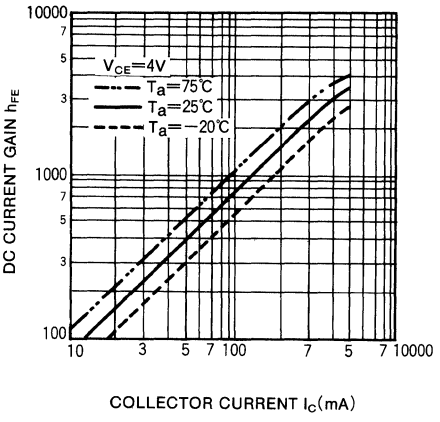
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



MITSUBISHI ELECTRIC

M54591P

8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPION

The M54591P, 8-channel sink driver, consists of 16 NPN transistors connected to from eight high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output sink current to 500mA
- Integral diodes for transient suppression
- Wide operating temperature range (T_a=−20∼+75℃)

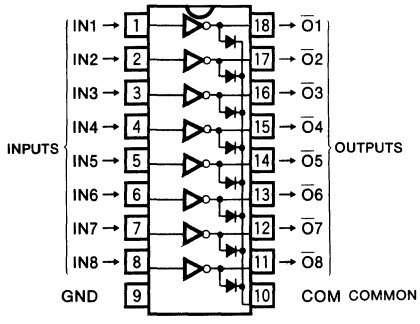
APPLICATION

Relay and printer driver, LED or incandescent display digit driver.

FUNCTION

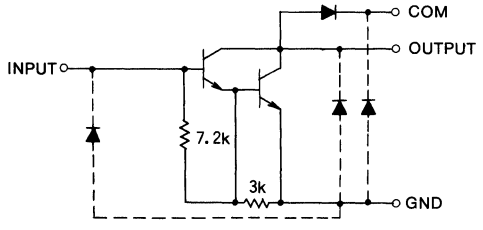
The M54591P is comprised of eight NPN darlington driver pairs. Between pin 10 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 9. The outputs are capable of sinking 500mA and will withstand 80V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+80	V
I_C	Collector current	Transistor ON	500	mA
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54591P

8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		80	V
I_C	Collector current per channel	All units ON Percent duty cycle≦6%	0		400	mA
		All units ON Percent duty cycle≦34%	0		200	
I_{IH}	"H" Input current	I_C=400mA	1		20	mA
I_{IL}	"L" Input current		0		20	μA

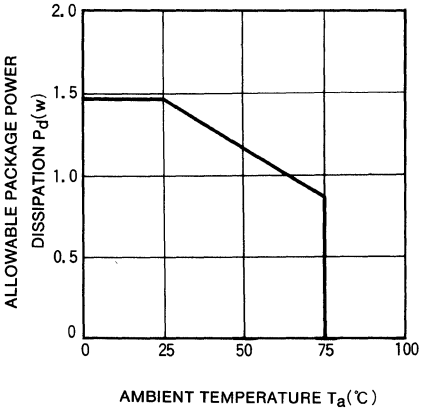
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=80V			100	μA
$V_{CE(sat)}$	Output saturation voltage	I_I=1mA, I_C=400mA		1.3	2.4	V
		I_I=1mA, I_C=200mA			1.6	
V_I	Input voltage	I_I=1mA		1.35	1.7	V
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
I_R	Clamp diode leakage current	V_R=80V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=350mA, T_a=25℃	1000			—

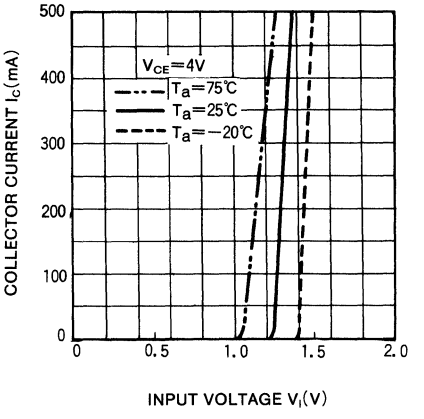
* : A typical value at T_a = 25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

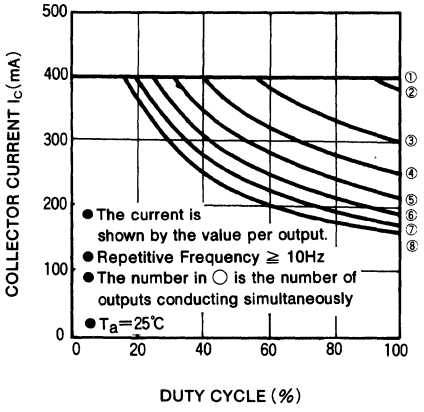


OUTPUT CURRENT CHARACTERISTICS

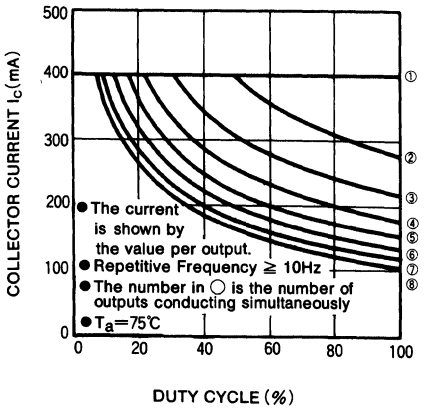


MITSUBISHI ELECTRIC

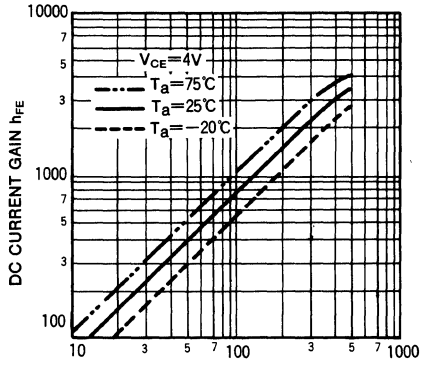
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



M54592P

8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54592P, 8-channel sink driver, consists of 16 NPN transistors connected to from eight high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output sink current to 500mA
- Integral diodes for transient suppression
- 24V PMOS compatible input
- Wide operating temperature range (T_a=−20∼+75℃)

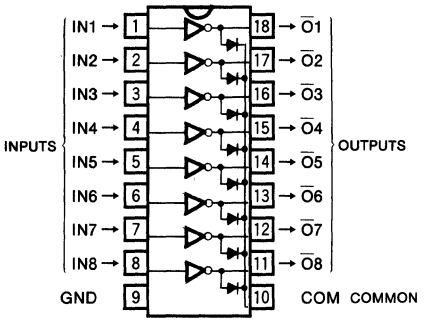
APPLICATION

Relay and printer diver, LED or incandescent display digit driver.

FUNCTION

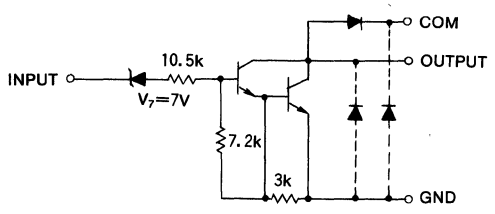
The M54592P is comprised of eight NPN darlington diver pairs. Each input has a Zener diode and 10.5kΩ resistor in series to limit the input current. Between pin 10 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 9. The outputs are capable of sinking 500mA and will withstand 80V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+80	V
I_C	Collector current	Transistor ON	500	mA
V_I	Input voltage		−0.5∼+30	V
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54592P

8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		80	V
I_C	Collector current per channel	All units ON Percent duty cycle≦6%	0		400	mA
		All units ON Percent duty cycle≦34%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	17		30	V
V_{IL}	"L" Input voltage		0		6	V

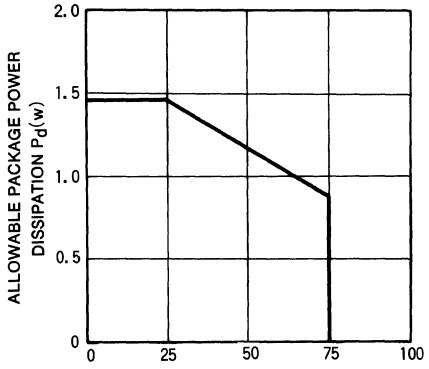
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=80V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=17V, I_C=400mA		1.3	2.4	V
		V_I=17V, I_C=200mA			1.6	
I_I	Input current	V_I=17V		0.85	1.8	mA
		V_I=25V		1.6	3.2	
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
I_R	Clamp diode leakage current	V_R=80V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=350mA, T_a=25℃	1000			—

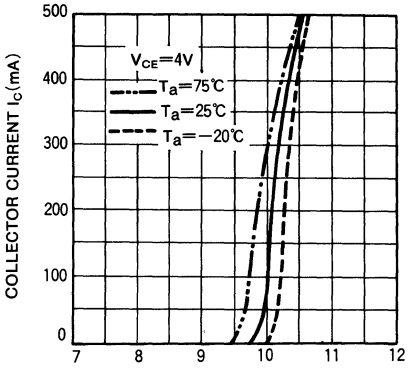
* : A typical value at T_a = 25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

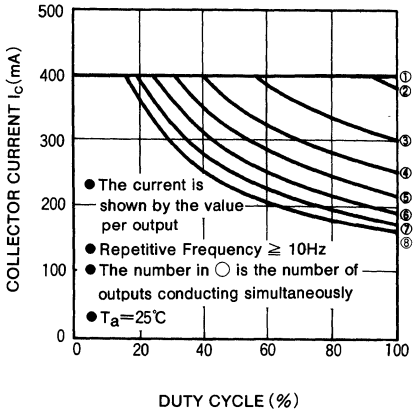


OUTPUT CURRENT CHARACTERISTICS

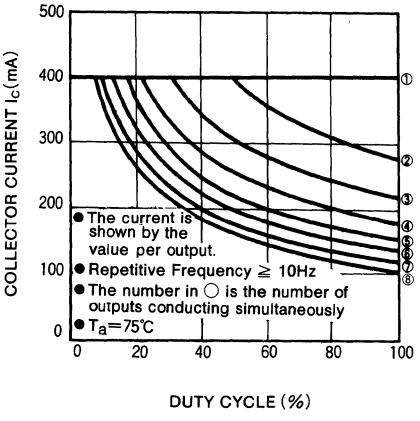


8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

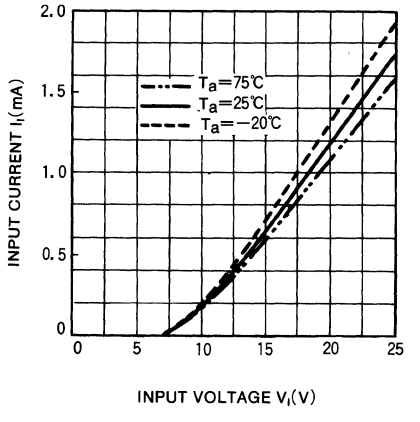
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



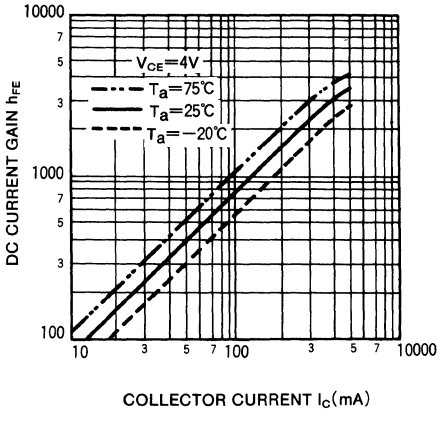
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



MITSUBISHI ELECTRIC

M54593P

8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54593P, 8-channel sink driver, consists of 16 NPN transistors connected to from eight high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output sink current to 500mA
- Integral diodes for transient suppression
- PMOS compatible input
- Wide operating temperature rage (T_a=−20∼+75℃)

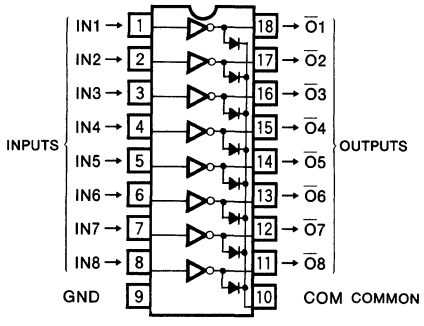
APPLICATION

Relay and printer driver, LED or incandescent display digit driver.

FUNCTION

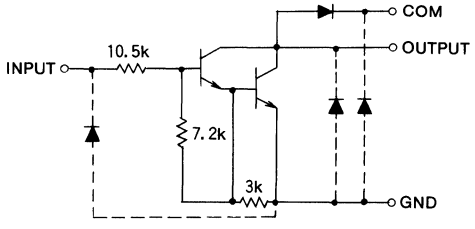
The M54593P is comprised of eight darlington diver pairs with 10.5k Ω series input resistors. Between pin 10 and each output, there are integral diodes for inductive load transient suppression. All emitters and the substrate are connected together to pin 9. The outputs are capable of sinking 500mA and will withstand 80V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+80	V
I_C	Collector current	Transistor ON	500	mA
V_I	Input voltage		−0.5∼+30	V
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54593P

8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		80	V
I_C	Collector current per channel	All units ON Percent duty cycle≦6%	0		400	mA
		All units ON Percent duty cycle≦34%	0		200	
V_{IH}	"H" Input voltage	I_C=400mA	8	10	25	V
V_{IL}	"L" Input voltage		0		0.5	V

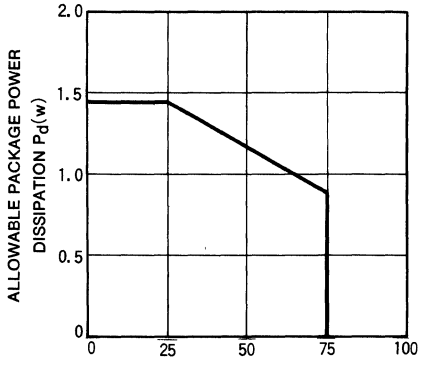
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	V_{CE}=80V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_I=8V, I_C=400mA		1.3	2.4	V
		V_I=8V, I_C=200mA			1.6	
I_I	Input current	V_I=10V		0.9	1.5	mA
		V_I=25V			4.1	
V_F	Clamp diode forward voltage	I_F=400mA		1.5	2.4	V
I_R	Clamp diode leakage current	V_R=80V			100	μA
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=350mA, T_a=25℃	1000			—

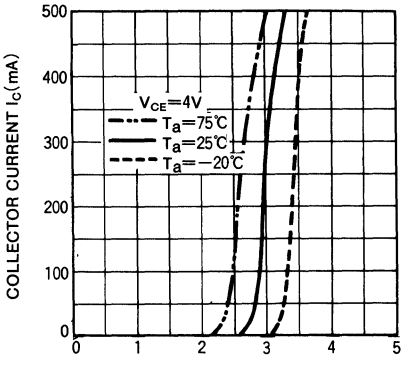
* : A typical value at T_a = 25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

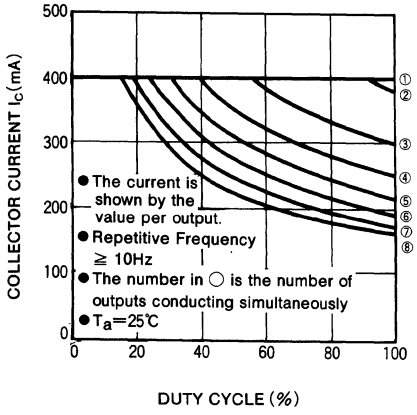


OUTPUT CURRENT CHARACTERISTICS

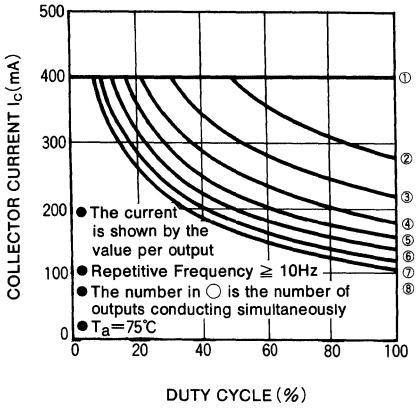


8-UNIT HIGH VOLTAGE 500mA DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

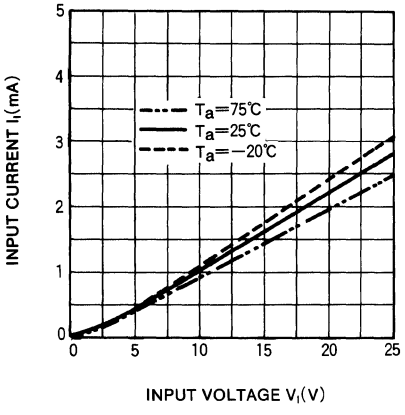
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



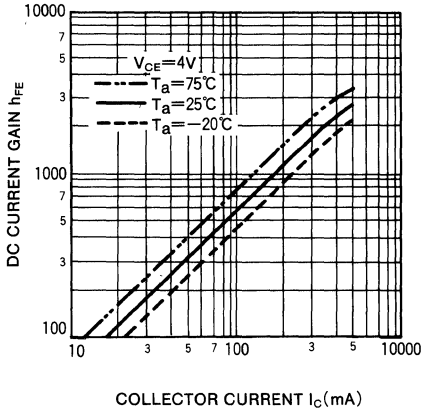
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54594P

4-UNIT HIGH VOLTAGE 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54594P 4-channel sink diver, consists of 8 NPN transistors connected to from four high current gain diver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output sink current to 1.5A
- Integral diodes for transient suppression
- Wide operating temperature range (T_a=−20～+75℃)

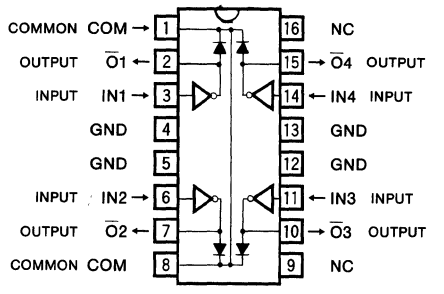
APPLICATION

Relay and printer driver, Display driver

FUNCTION

The M54594P is comprised of four NPN darlington driver pairs with 350 Ω series input resistors. Each output has a diode for inductive load transient suppression and the cathodes of the diodes are connected to pin 8 and 1. The outputs are capable of sinking 1.5A and will withstand 80V in the OFF state.

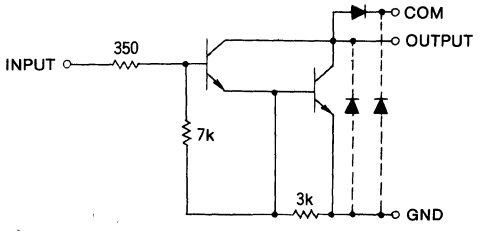
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5～+80	V
I_C	Collector current	Transistor ON	1.5	A
V_I	Input voltage		−0.5～+10	V
$I_{F(D)}$	Clamp diode forward current	Pulse width≦10ms, Percent duty cycle≦5%	1.5	A
		Pulse width≦100ms, Percent duty cycle≦5%	1.25	
$V_{R(D)}$	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.92	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

M54594P

4-UNIT HIGH VOLTAGE 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		80	V
I_C	Collector current per channel	All units ON Percent duty cycle≦4%	0		1.25	A
		All units ON Percent duty cycle≦18%	0		700	mA
V_{IH}	"H" Input voltage	I_C=1.25A	3		10	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.4	V

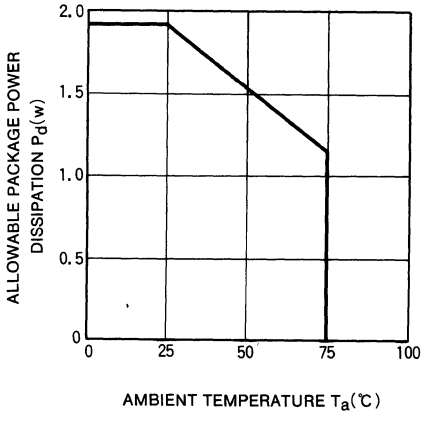
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA		80			V
$V_{CE(sat)}$	Output saturation voltage	I_I=2mA	I_C=1.25A			2.2	V
			I_C=700mA			1.7	
I_I	Input current	V_I=3V			5	8.5	mA
V_F	Clamp diode forward voltage	I_F=1.25A				2.3	V
V_R	Clamp diode reverse voltage	I_R=100μA		80			V
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=1A, T_a=25℃		1000			—

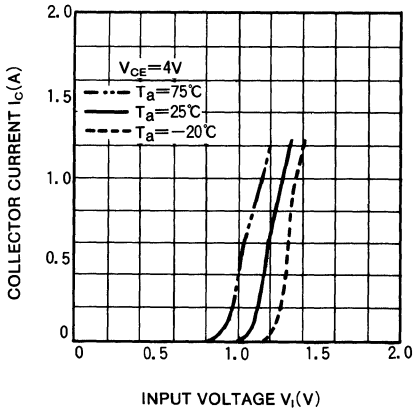
* : A typical value is at T_a = 25℃

TYPICAL CHARACTERISTICS

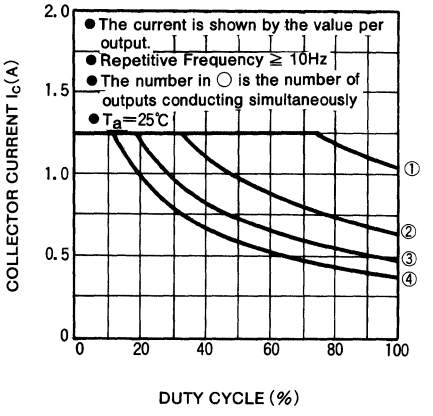
ALLOWABLE AVERAGE POWER DISSIPATION



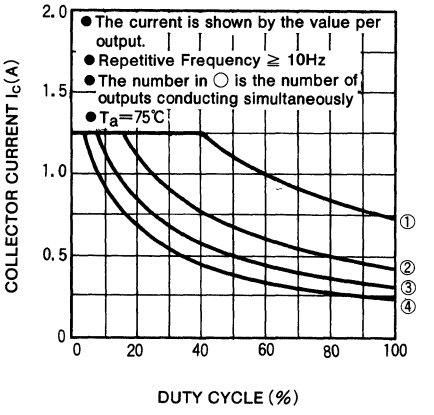
OUTPUT CURRENT CHARACTERISTICS



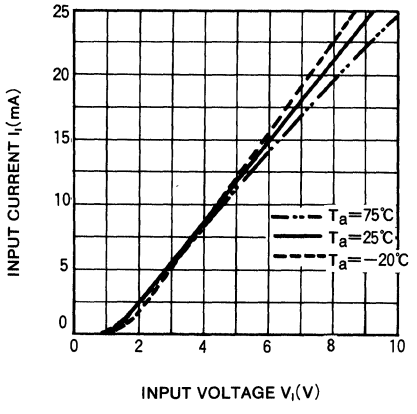
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



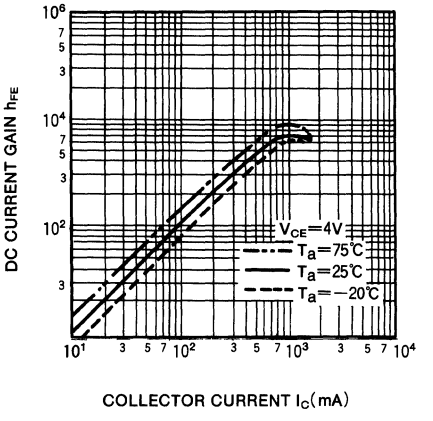
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN
CHARACTERISTICS



M54595P

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54595P, 4-channel sink driver, consists of 8 NPN transistors connected to from four high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80v
- High output sink current to 1.5A
- Integral diodes for transient suppression
- Wide operating temperature range (T_a=−20∼+75℃)

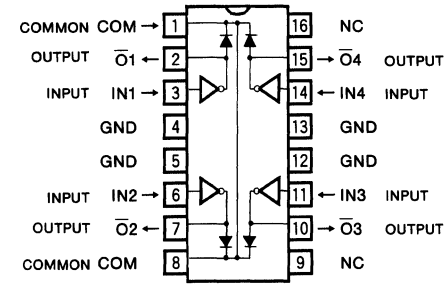
APPLICATION

Relay and printer driver, Display driver

FUNCTION

The M54595P is comprised of four NPN darlington driver pairs with 3kΩ series input resistors. Each output has a diode for inductive load transient suppression and the cathodes of the diodes are connected to pin 8 and 1. The outputs are capable of sinking 1.5A and will withstand 80V in the OFF state.

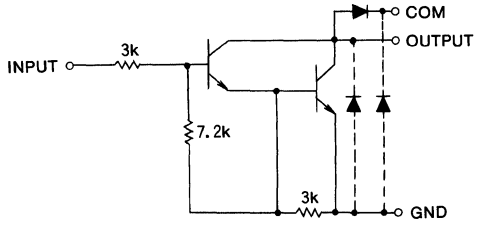
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+80	V
I_C	Collector current	Transistor ON	1.5	A
V_I	Input voltage		−0.5∼+30	V
I_F	Clamp diode forward current	Pulse width≦10ms, Percent duty cycle≦5%	1.5	A
		Pulse width≦100ms, Percent duty cycle≦5%	1.25	
V_R	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.92	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage		0		80	V
I_C	Collector current per channel	All units ON Percent duty cycle≦4%	0		1.25	A
		All units ON Percent duty cycle≦18%	0		700	mA
V_{IH}	"H" Input voltage	I_C=1.25A	8		10	V
V_{IL}	"L" Input voltage	$I_{O(leak)}$=50μA	0		0.4	V

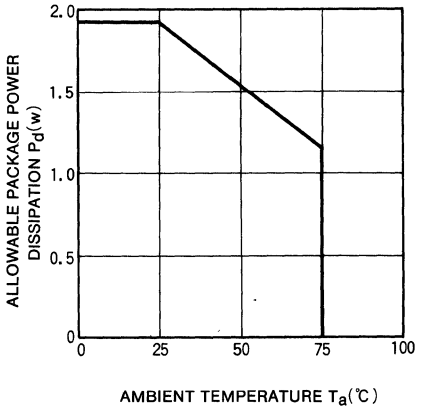
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA		80			V
$V_{CE(sat)}$	Output saturation voltage	I_I=2mA	I_C=1.25A			2.2	V
			I_C=700mA			1.7	
I_I	Input current	V_I=10V			4	8	mA
V_F	Clamp diode forward voltage	I_F=1.25A				2.3	V
V_R	Clamp diode reverse voltage	I_R=100μA		80			V
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=1A, T_a=25℃		800			—

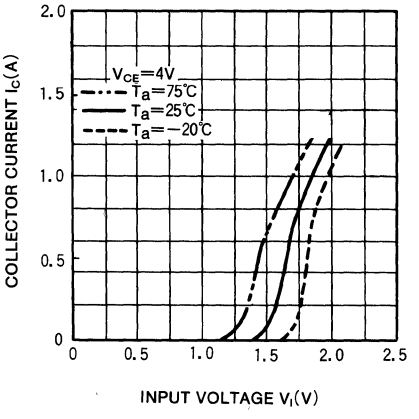
* : A typical value is at T_a = 25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



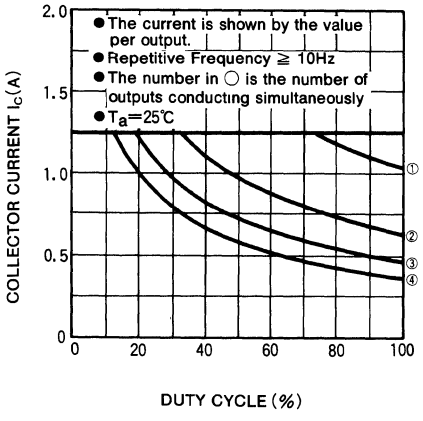
OUTPUT CURRENT CHARACTERISTICS



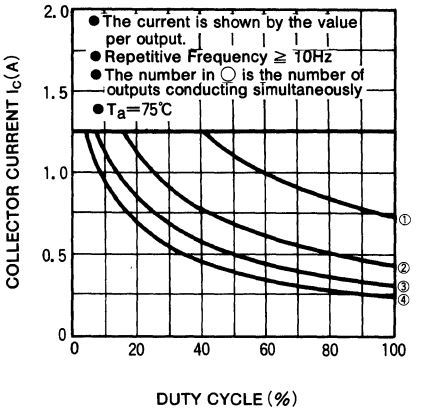
MITSUBISHI ELECTRIC

4-UNIT 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

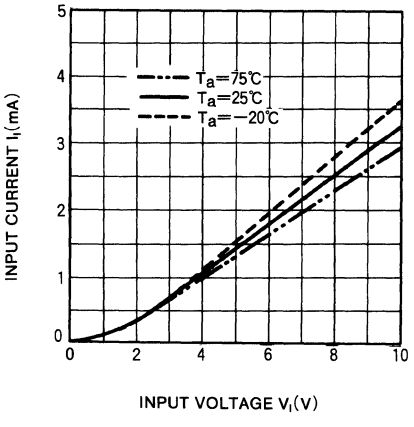
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



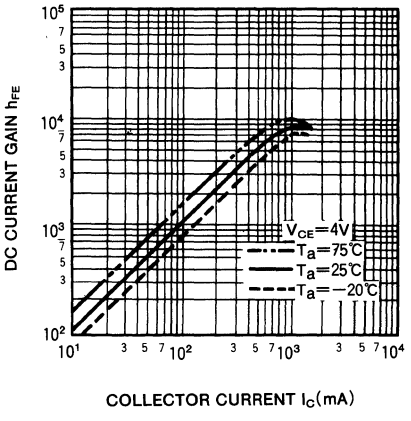
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



DC CURRENT GAIN CHARACTERISTICS



M54596P

4-UNIT HIGH VOLTAGE 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54596P, 4-channel sink driver, consists of 4 PNP and 8 NPN transistors to from four high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output current to 1.5A
- Integral diodes for transient suppression
- NMOS Compatible input
- Wide operating temperature range (T_a=−20∼+75℃)

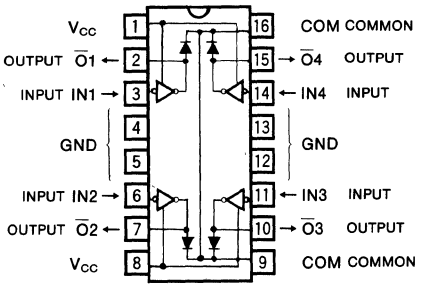
APPLICATION

Relay and printer driver, LED or incandescent display digit driver

FUNCTION

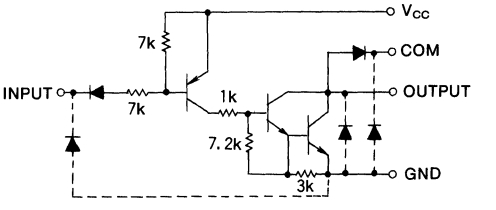
The M54596P is comprised of four PNP invertors with 7kΩ series input resistors and four NPN darlington sink drivers. Each output has an integral diode for inductive load transient suppression and the anodes of the diode connected to pins 9 and 16. The outputs are capable of sinking 1.5A and will withstand 80V in the OFF state.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+80	V
V_I	Input voltage		−0.5∼+30	V
I_C	Collector current	Transistor ON	1.5	A
V_R	Clamp diode reverse voltage		80	V
I_F	Clamp diode forward current	Pulse width≦10ms, Percent duty cycle≦5%	1.5	A
		Pulse width≦100ms, Percent duty cycle≦5%	1.25	
P_d	Power dissipation	T_a=25℃	1.92	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

MITSUBISHI ELECTRIC

M54596P

4-UNIT HIGH VOLTAGE 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
V_O	Output voltage		0		80	V
I_C	Collector current per channel	All units ON Percent duty cycle ≦ 4%	0		1.25	A
		All units ON Percent duty cycle ≦ 18%	0		0.7	
V_{IH}	"H" Input voltage	$I_{O(leak)}$=50μA	V_{CC}−0.5		V_{CC}	V
V_{IL}	"L" Input voltage	I_C=1.25A	0		V_{CC}−3.5	V

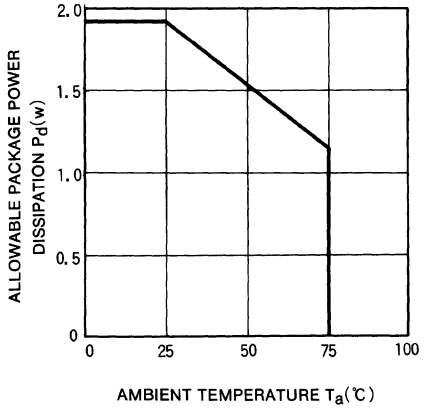
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
I_{CC}	Supply current	V_{CC}=6V, V_I=0.5V (per channel)			4.6	7.5	mA
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA		80			V
$V_{CE(sat)}$	Output saturation voltage	V_{CC}=4V	I_C=1.25A			2.2	V
		V_I=0.5V	I_C=0.7A			1.7	
I_I	Input current	V_I=V_{CC}−3.5V				−0.6	mA
		V_I=V_{CC}−6V				−0.95	
V_R	Clamp diode reverse voltage	I_R=100μA		80			V
V_F	Clamp diode forward voltage	I_F=1.25A				2.3	V
h_{FE}	DC forward current gain	V_{CC}=4V, V_{CE}=4V, I_C=1A, T_a=25℃		4000			—

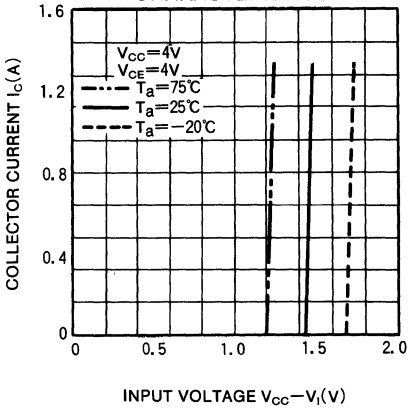
* : A typical value is at T_a = 25℃.

TYPICAL CHARACTERISTICS

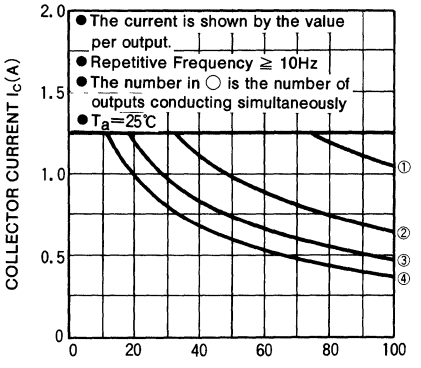
ALLOWABLE AVERAGE POWER DISSIPATION



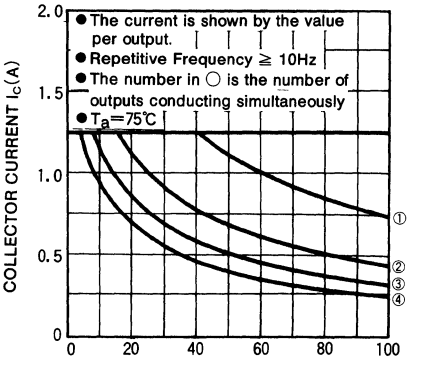
OUTPUT CURRENT CHARACTERISTICS



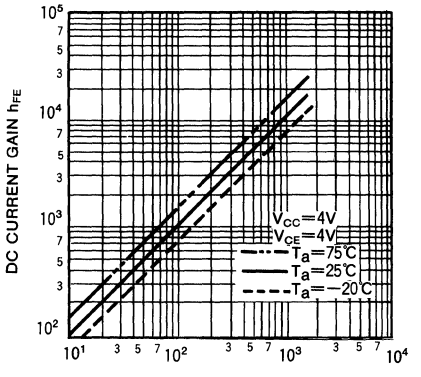
ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN
CHARACTERISTICS



MITSUBISHI ELECTRIC

M54597P

8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54597P, 8-channel source driver, consists of 8 PNP and 24 NPN transistors connected to from eight high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output source current to 500mA
- Integral diode for transient suppression
- PMOS Compatible input
- Wide operating temperature range (T_a=−20∼+75℃)

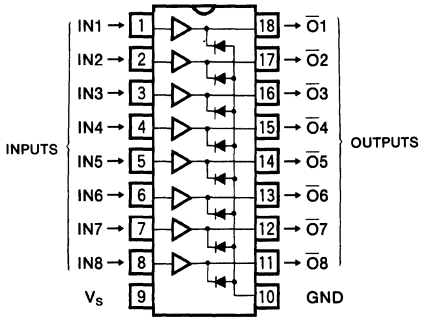
APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

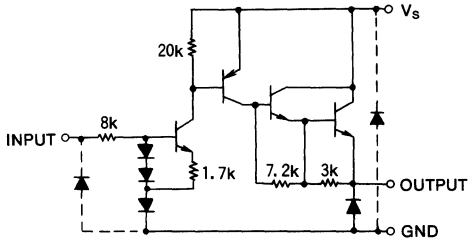
The driver of the M54597P is comprised of a NPN invertor and compound PNP/NPN/NPN output source driver, and the output is turned ON by an active high input level. Each output has an integral diode for inductive load transient suppression. The outputs are capable of driving 500mA and are rated for operation with output voltage up to 80V.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	+80	V
V_S	Supply voltage		−0.5∼+80	V
V_I	Input voltage		−0.5∼+30	V
I_O	Output current	Per channel current at "H" output	−500	mA
I_F	Clamp diode forward current		500	mA
V_R	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54597P

8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		80	V
I_O	Output current per channel	All units ON Percent duty cycle≦8%	0		−350	mA
		All units ON Percent duty cycle≦55%	0		−100	
V_{IH}	"H" Input voltage	I_O=−350mA	2.4	5	10	V
V_{IL}	"L" Input voltage		0		0.2	V

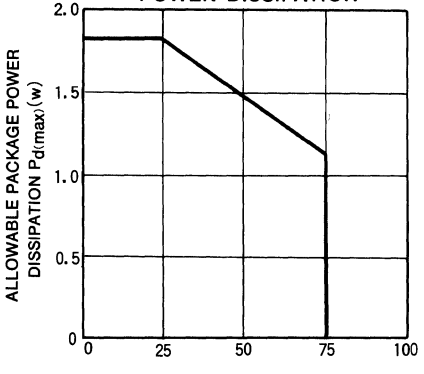
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{S(leak)}$	Supply leakage current	V_S=80V, V_I=0.2V, V_O=0V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_S=10V, V_I=2.4V, I_O=−350mA			2.4	V
		V_S=10V, V_I=2.4V, I_O=−100mA			2	
I_I	Input current	V_I=5V			0.75	mA
		V_I=25V			4.7	
I_S	Supply current	V_S=80V, V_I=5V			15	mA
V_F	Clamp diode forward voltage	I_F=−350mA			−2.4	V
V_R	Clamp diode reverse voltage	I_R=100μA	80			V

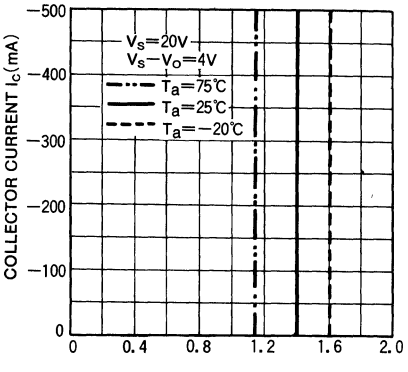
* : A typical value at T_a = 25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



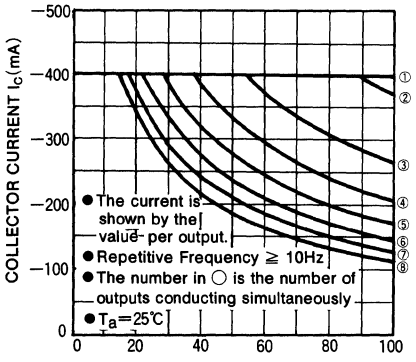
OUTPUT CURRENT CHARACTERISTICS



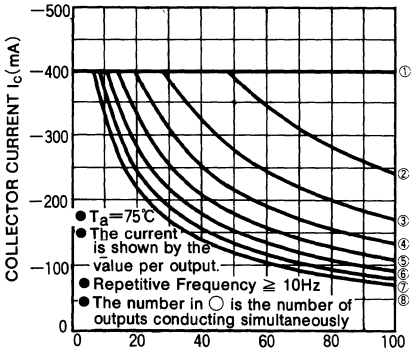
MITSUBISHI ELECTRIC

8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

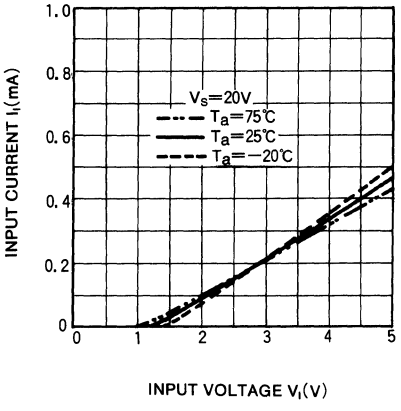
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



M54598P

8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54598P, 8-channel source driver, consists of 8 PNP and 24 NPN transistors connected to from eight high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output source current to 500mA
- Integral diode for transient suppression
- Wide operating temperature range (T_a=−20∼+75℃)

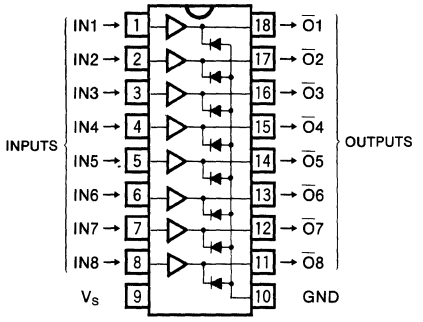
APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

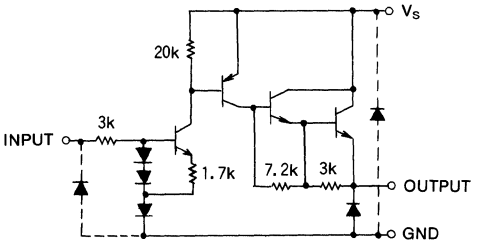
The driver of the M54598P is comprised of a NPN invertor and compound PNP/NPN/NPN output source driver and the output is turned ON by an active high input level. Each output has an integral diode for inductive load transient suppression. The outputs are capable of driving 500mA and are rated for operating with output voltage up to 80V.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used.

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	+80	V
V_S	Supply voltage		−0.5∼+80	V
V_I	Input voltage		−0.5∼+10	V
I_O	Output current	Per channel current at "H" output	−500	mA
I_F	Clamp diode forward current		−500	mA
V_R	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		80	V
I_O	Output current per channel	All units ON Percent duty cycle≦8%	0		−350	mA
		All units ON Percent duty cycle≦55%	0		−100	
V_{IH}	"H" Input voltage	I_O=−350mA	2.4		10	V
V_{IL}	"L" Input voltage		0		0.2	V

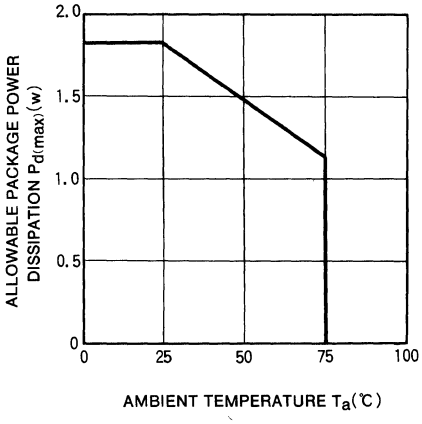
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$I_{S(leak)}$	Supply leak current	V_S=80V, V_I=0.2V, V_O=0V			100	μA
$V_{CE(sat)}$	Output saturation voltage	V_S=10V, V_I=2.4V, I_O=−350mA			2.4	V
		V_S=10V, V_I=2.4V, I_O=−100mA			2	
I_I	Input current	V_I=3V		0.6	1	mA
		V_I=10V		3.2	5	
I_S	Supply current	V_S=80V, V_I=3V			15	mA
V_F	Clamp diode forward voltage	I_F=−350mA			−2.4	V
V_R	Clamp diode reverse voltage	I_R=100μA	80			V

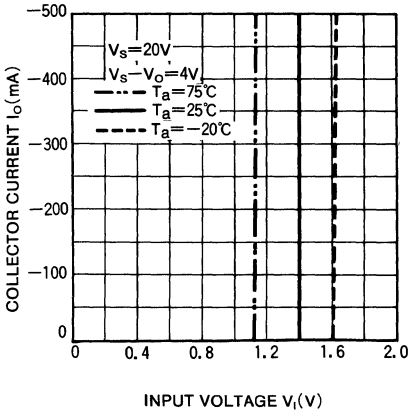
* : A typical value at T_a = 25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

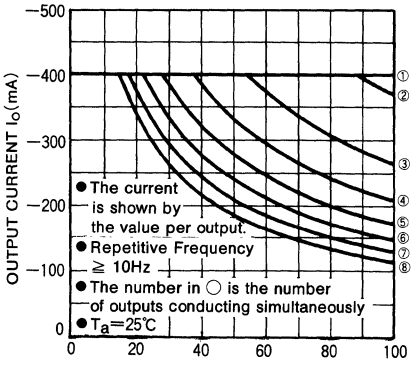


OUTPUT CURRENT CHARACTERISTICS

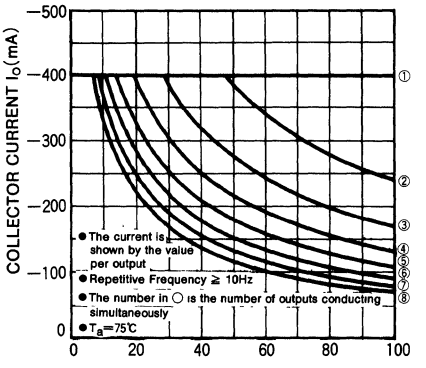


8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

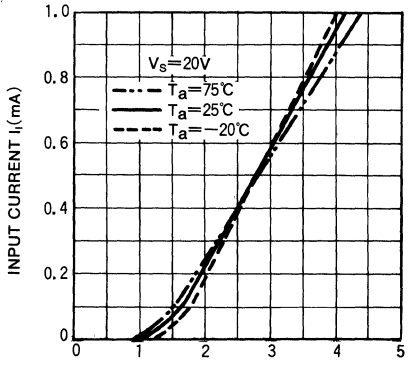
ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE



INPUT CHARACTERISTICS



M54600P

DUAL PERIPHERAL POSITIVE AND DRIVER

DESCRIPTION

M54600P is a semiconductor integrated circuit containing 2 circuits with TTL constructed logical NAND gates and high current, high breakdown voltage NPN transistors.

FEATURES

- NAND gates and NPN transistors are independent of each other.
- High current (I_C = 300mA), high breakdown voltage (BV_{CER}=30V) NPN transistors
- High speed switching (t_{pd}=20ns)
- SUB pin provision
- Strobe input provision

APPLICATION

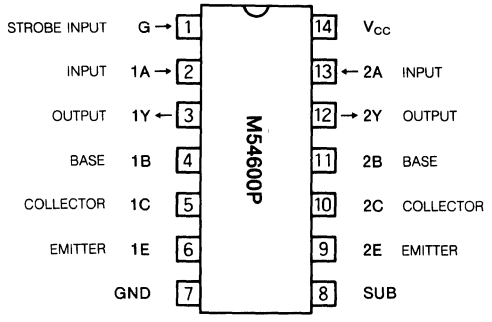
General purpose, for use in industrial and consumer digital equipment.

FUNCTION

This is a high speed driver containing two 2-input NAND gates with two NPN transistors (I_C = 300mA, BV_{CER} = 30V, $R_{BE} \leqq 500\Omega$).

A wide range of application is insured as NAND gate outputs and NPN transistor bases can be either connected or used as independent circuits. SUB pin must always be at the most negative device voltage for proper operation, whether it is GND line or the IC itself.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTION TABLE

Gate only

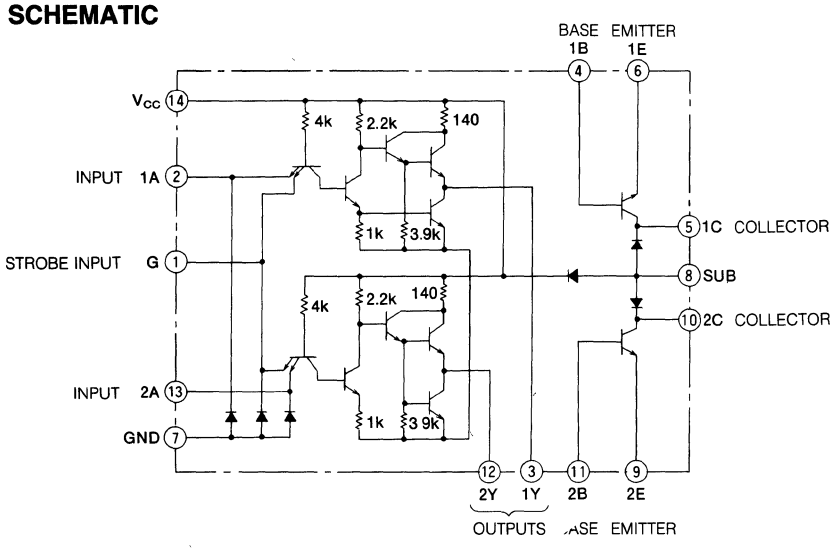
A	G	Y
L	L	H
L	H	H
H	L	H
H	H	L

Gate and transistor

A	G	C
L	L	L
L	H	L
H	L	L
H	H	H

When gate output Y and transistor base B, and when each emitter E and GND are connected directly and collector C is the output.

CIRCUIT SCHEMATIC



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = 0~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_{IE}	Interemitter voltage		5.5	V
V_{CCS}	V_{CC} to substrate voltage		35	V
V_{CS}	Collector to substrate voltage		35	V
V_{CB}	Collector base voltage		35	V
V_{CE}	Collector emitter voltage	The base-emitter resistance(R_{BE}) is $R_{BE} \leqq 500\Omega$	30	V
V_{EB}	Emitter base voltage		5	V
I_C (Note 1)	Collector current		300	mA
P_d	Power dissipation	$T_a \leqq 25$℃	800	mW
Topr	Operating temperature		0~75	℃
Tstg	Storage temperature		−65~+150	℃

Note 1 : Both halves of these dual circuits may conduct rated current simultaneously; but only if used within heat dissipation rating.

RECOMMENDED OPERATING CONDITIONS (T_a = 0~+75℃, unless otherwise noted)

TTL Gate

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
F_O	Fan out			10	—

Gate and transistor combined

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage	High-level state			24	V
I_{OL}	Low-level output current	V_{OL} = 0.4V			100	mA
		V_{OL} = 0.7V			300	

ELECTRICAL CHARACTERISTICS (T_a = 0~+75℃, unless otherwise noted)

TTL Gate

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −12mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OH} = −400μA		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V, V_{IH} = 2V, I_{OL} = 16mA			0.22	0.4	V
$I_{IH(A)}$	High-level input current	Input A	V_{CC} = 5.25V	V_I = 2.4V			40	μA
				V_I = 4.5V			60	
$I_{IH(G)}$		Input G	V_{CC} = 5.25V	V_I = 2.4V			80	μA
				V_I = 4.5V			120	
$I_{IL(A)}$	Low-level input current	Input A	V_{CC} = 5.25V, V_I = 0.4V				−1.6	mA
$I_{IL(G)}$		Input G	V_{CC} = 5.25V, V_I = 0.4V				−3.2	mA
I_{OS}	Short circuit output current (Note 2)		V_{CC} = 5.25V		−18		−55	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V, V_I = 0V			4.5	8	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = 5.25V, V_I = 5V			6	11	mA

* A Typical value at T_a = 25℃

Transistor

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
BV_{CBO}	Collector base breakdown voltage	$I_C = 100\mu A$, $I_E = 0$		35			V
BV_{CER}	Collector emitter breakdown voltage	$I_C = 100\mu A$, $R_{BE} = 500\Omega$		30			V
BV_{EBO}	Emitter base breakdown voltage	$I_E = 100\mu A$, $I_C = 0$		5			V
h_{FE}	Static forward current transfer ratio (Note 3)	$V_{CE} = 3V$	$I_C = 100mA$	25			—
		$T_a = 25℃$	$I_C = 300mA$	30			
		$V_{CE} = 3V$	$I_C = 100mA$	20			
		$T_a = 0℃$	$I_C = 300mA$	25			
V_{BE}	Base emitter voltage (Note 3)	$I_B = 10mA$, $I_C = 100mA$			0.85	1	V
		$I_B = 30mA$, $I_C = 300mA$			1.05	1.2	
$V_{CE(sat)}$	Collector emitter saturation voltage (Note 3)	$I_B = 10mA$, $I_C = 100mA$			0.25	0.4	V
		$I_B = 30mA$, $I_C = 300mA$			0.5	0.7	

With TTL Gate output connected to transistor base 'B', and each emitter 'E', and GND connected

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_O = 30V$				100	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 100mA$		0.25	0.4	V
		$V_{IL} = 0.8V$	$I_{OL} = 300mA$		0.5	0.7	
I_{CCL}	Low-level supply current	$V_{CC} = 5.25V$, $V_I = 0V$				65	mA

* : All typical values are $V_{CC} = 5V$, $T_a = 25℃$

Note 2 : Not more than one output should be shorted at a time

3 : Test with pulse width of $300\mu s$, and duty cycle of $\leqq 2\%$ pulse

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25℃$, unless otherwise noted)

TTL Gate

Symbol (Note 4)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(A-Y)}$	Low-to-high-level output, high-to-low-level output propagation time, from input A, G to output Y	$C_L = 15pF$, $R_L = 400\Omega$ (Note 5)		12	22	ns
$t_{PHL(A-Y)}$				8	15	ns

Output transistor

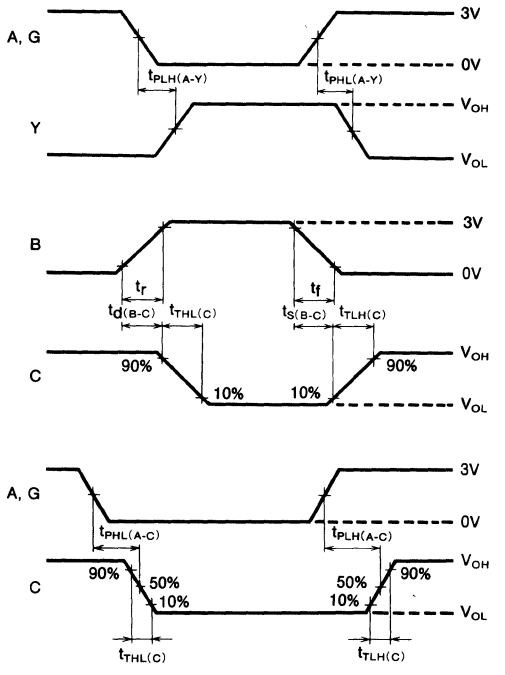
Symbol (Note 4)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(B-C)}$	Delay time	$I_C \approx 200mA$, $I_{B(1)} = 20mA$		8	15	ns
$t_{THL(C)}$	Rise time	$I_{B(2)} = -40mA$, $V_{BE(off)} = -1V$		12	20	ns
$t_{S(B-C)}$	Stotage time	$C_L = 15pF$, $R_L = 50\Omega$		7	15	ns
$t_{TLH(C)}$	Fall time	(Notes 6, 7)		6	15	ns

TTL Gate and output transistor combined

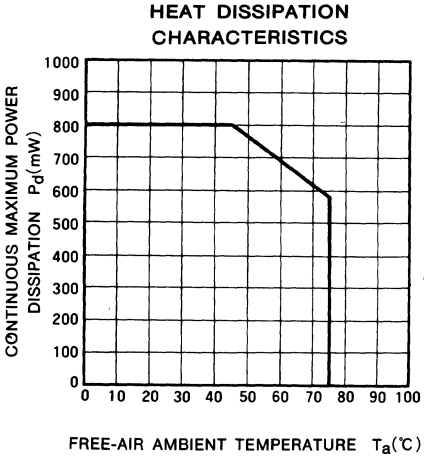
Symbol (Note 4)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(A-C)}$	Low-to-high-level output, high-to-low-level output	$I_C \approx 200mA$		20	30	ns
$t_{PHL(A-C)}$	propagation time; from input A, G to output C	$C_L = 15pF$, $R_L = 50\Omega$		20	30	ns
$t_{TLH(C)}$	Low-to-high-level output, high-to-low-level output	(Notes 7, 8)		7	12	ns
$t_{THL(C)}$	transition time; output C			9	15	ns

Note 4 : Symbols indicate representative examples

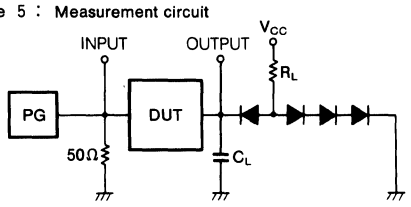
TIMING DIAGRAM (Reference level = 1.5V)



TYPICAL CHARACTERISTICS

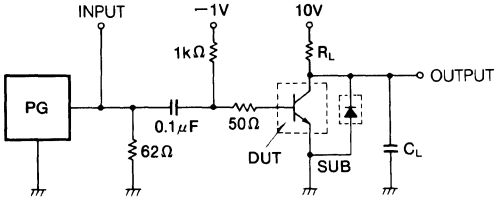


Note 5 : Measurement circuit



1. The pulse generator (PG) has the following characteristics: $t_r \leqq 10ns$, $t_f \leqq 5ns$, PRR = 1MHz, $t_{PW} = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
2. All diodes are high speed switching diodes ($t_{rr} \leqq 4ns$)
3. C_L includes probe and jig capacitance.

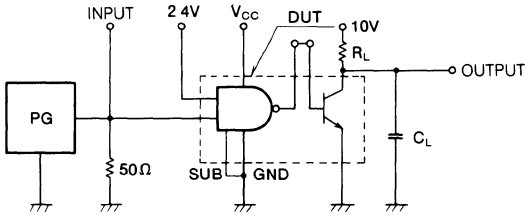
Note 6 : Test circuit



1. The pulse generator (PG) has the following characteristics. $t_r \leqq 5ns$, $t_f \leqq 5ns$, DUTY CYCLE ≦ 1%, $t_{PW} = 300ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

Note 7 : Output breakdown voltage drops upon switching.
Examples: $I_{OL} \cong 300mA$ @ $V_O \cong 15V$ and $I_{OL} \cong 100mA$ @ $V_O \cong 20V$. In case of inductive load use, lower drive supply voltage.
When driving a relay be sure to use a diode in the relay coil to protect against the IC being damaged by relay coil generated counter-electromotive force or when relay coil voltage drops below 12V.

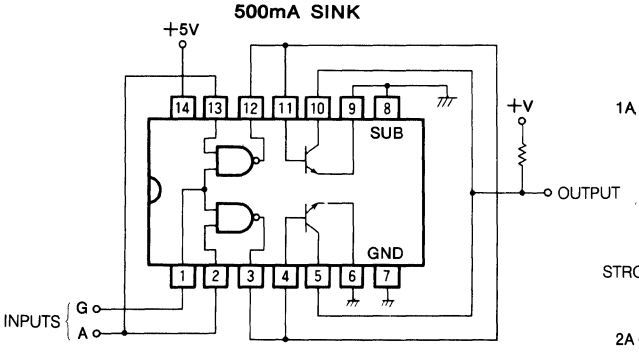
Note 8 : Measurement circuit



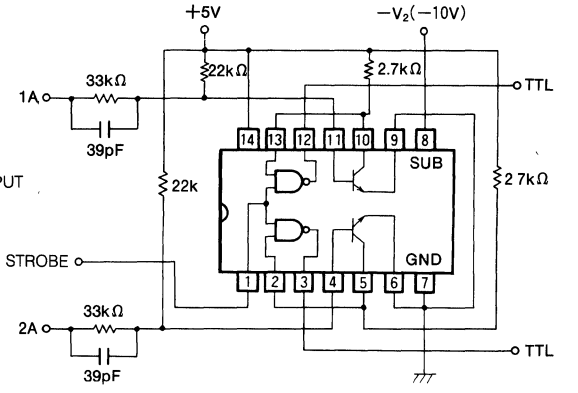
1. The pulse generator (PG) has the following characteristics: $t_r \leqq 10ns$, $t_f \leqq 5ns$, PRR = 1MHz, $T_{PW} = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
2. C_L includes probe and jig capacitance.

APPLICATION EXAMPLES

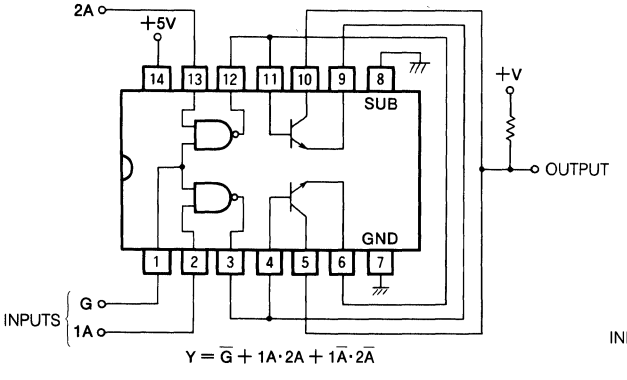
500mA SINK



DUAL MOS TO TTL CONVERTER

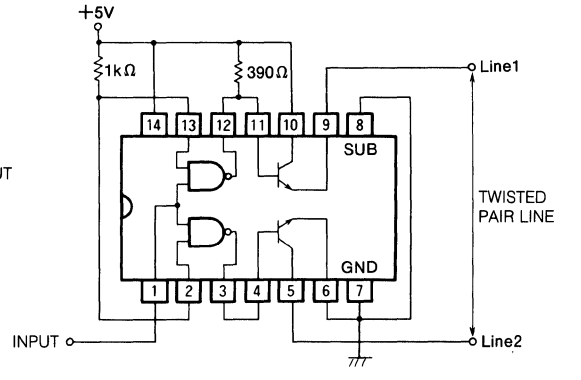


GATED COMPARATOR

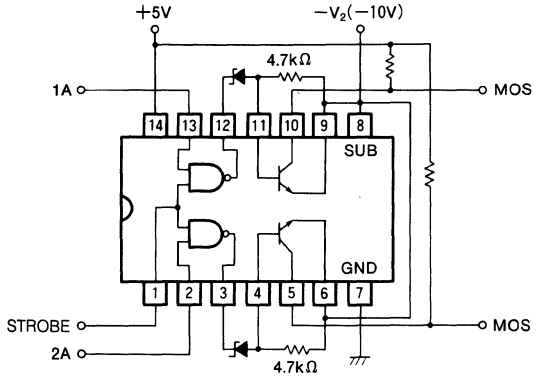


$Y = \overline{G} + 1A \cdot 2A + 1\overline{A} \cdot 2\overline{A}$

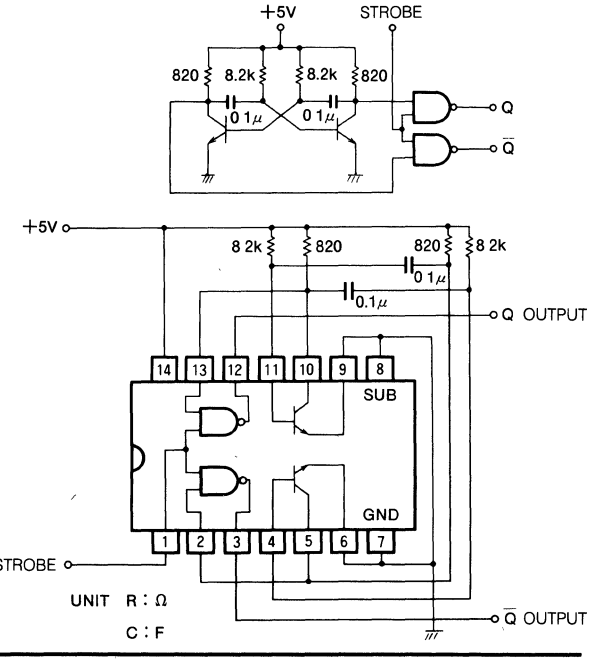
BALANCED LINE DRIVER



DUAL TTL TO MOS CONVERTER



SQUARE-WAVE GENERATOR



MITSUBISHI ELECTRIC

M54601P

DUAL PERIPHERAL POSITIVE AND DRIVER

DESCRIPTION

M54601P is a semiconductor integrated circuit containing 2 circuits with TTL constructed logical AND drivers, each having high output current and high breakdown output voltage characteristics.

FEATURES

- High output current (I_O=300mA)
- High breakdown output voltage (V_O=30V)
- High speed switching (t_{pd}=18ns)
- A small 8 pin DIL package

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

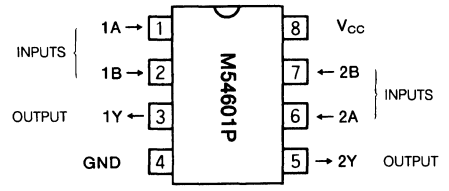
FUNCTION

The output being an open collector, each circuit is capable of handling a maximum output current of 300mA when in low-level state and, when in high-level state, a maximum voltage of 30V can be applied. As mean propagation delay time is 18ns, high speed switching is possible. Supply voltage being 5V ± 5% and input being TTL, this IC can be connected directly to TTL. This IC has a broad range of application as a relay and lamp driver as well as a MOS MEMORY driver.

FUNCTION TABLE

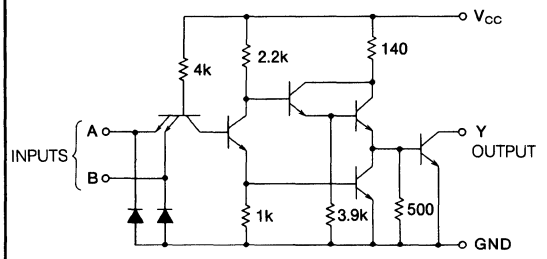
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

PIN CONFIGURATION (TOP VIEW)



Outline 8P4

CIRCUIT SCHEMATIC (EACH DRIVER)



Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = 0~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_{IE}	Interemitter voltage		5.5	V
V_O	Output voltage	High-level state	30	V
I_O	Output current	Low-level state	300	mA
P_d	Power dissipation	$T_a \leq 25$℃	800	mW
T_{opr}	Operating temperature		0~75	℃
Tstg	Storage temperature		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_O	Output voltage	High-level state			24	V
I_{OL}	Low-level output current	V_{OL} = 0.4V			100	mA
		V_{OL} = 0.7V			300	

ELECTRICAL CHARACTERISTICS (T_a = 0~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −12mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75V, V_{IH} = 2V, V_{OH} = 30V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 100mA		0.25	0.4	V
		V_{IL} = 0.8V	I_{OL} = 300mA		0.5	0.7	
I_{IH}	High-level input current	V_{CC} = 5.25V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V			−1	−1.6	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5.25V, V_I = 5V			7	11	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = 5.25V, V_I = 0V			52	65	mA

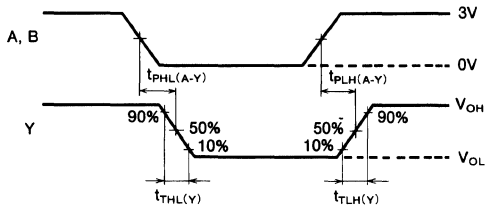
* : A typical value at T_a = 25℃.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃, unless otherwise noted)

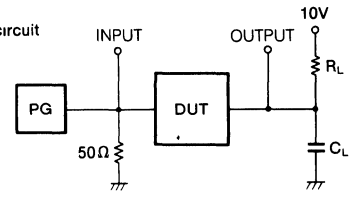
Symbol (Note 1)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(A-Y)}$	Low-to-high-level output, high-to-low-level output propagation time; from input A, B, to output Y	$I_O \approx$ 200mA, C_L = 15pF, R_L = 50Ω (Notes 2, 3)		18	25	ns
$t_{PHL(A-Y)}$				18	25	
$t_{TLH(Y)}$	Low-to-high-level output, high-to-low-level output transition time; output Y			6	10	ns
$t_{THL(Y)}$				9	15	

Note 1 : Symbols indicate representative examples

TIMING DIAGRAM (Reference level = 1.5V)



Note 2 : Test circuit

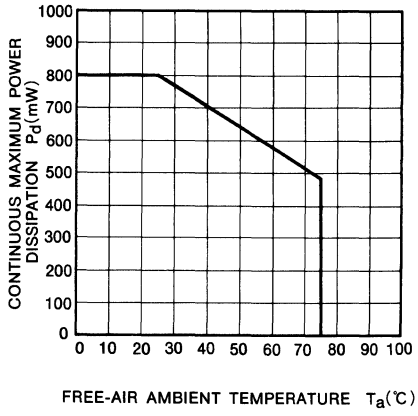


1) The pulse generator (PG) has the following characteristics
$t_r \leqq 10ns$, $t_f \leqq 5ns$, PRR = 1MHz,
$t_{PW} = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$
2) C_L includes probe and jig capacitance

Note 3 : Output breakdown voltage drops upon switching.
Example $I_{OL} \cong 300mA$ @ $V_O \cong 15V$ and $I_{OL} \cong 100mA$ @ $V_O \cong 20V$ In case of inductive load use, lower supply voltage When driving a relay be sure to use a diode in the relay coil to protect against the IC being damaged by relay coil generated counter-electromotive force or when relay coil voltage drops below 12V

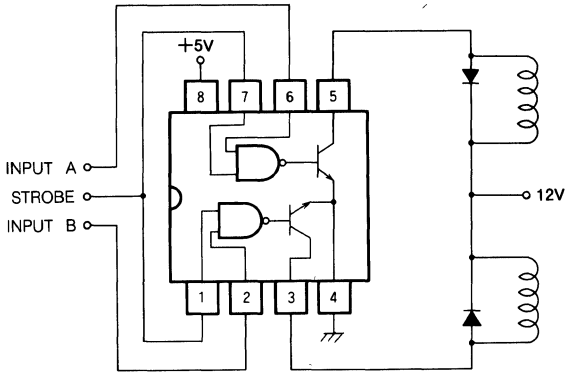
TYPICAL CHARACTERISTICS

HEAT DISSIPATION CHARACTERISTICS



APPLICATION EXAMPLE

RELAY DRIVER



M54602P

DUAL PERIPHERAL POSITIVE NAND DRIVER

DESCRIPTION

M54602P is a semiconductor integrated circuit containing 2 circuits with TTL constructed logical NAND drivers, each having high output current and high breakdown output voltage characteristics.

FEATURES

- High output current (I_O=300mA)
- High breakdown output voltage (V_O=30V)
- High speed switching (t_{pd}=25ns)
- A small 8 pin DIL package

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

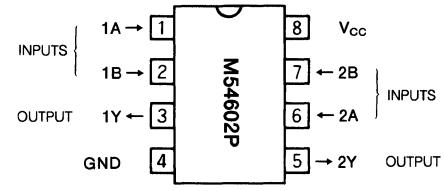
FUNCTION

The output being an open collector, each circuit is capable of handling a maximum output current of 300mA when in low-level output and, when in high-level output, a maximum voltage of 30V can be applied. As mean propagation delay time is 25ns, high speed switching is possible. Supply voltage being 5V±5% and input being TTL, this IC can be connected directly to TTL. This IC has a broad range of application as a relay and lamp driver as well as a MOS MEMORY driver.

FUNCTION TABLE

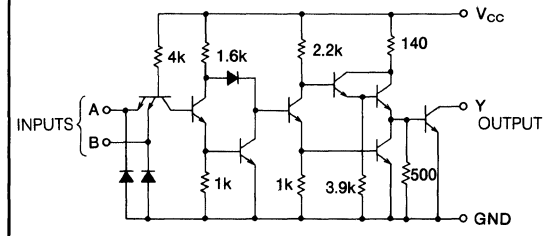
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 8P4

CIRCUIT SCHEMATIC (EACH DRIVER)



Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = 0~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_{IE}	Interemitter voltage		5.5	V
V_O	Output voltage	High-level state	30	V
I_O	Output current	Low-level state	300	mA
P_d	Power dissipation	$T_a \leq 25$℃	800	mW
T_{opr}	Operating temperature		0~75	℃
T_{stg}	Storage temperature		−65~+150	℃

MITSUBISHI ELECTRIC

RECOMMENDED OPERATING CONDITIONS (T_a = 0~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_O	Output voltage	High-level state			24	V
I_{OL}	Low-level output current	V_{OL} = 0.4V			100	mA
		V_{OL} = 0.7V			300	

ELECTRICAL CHARACTERISTICS (T_a = 0~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −12mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75V, V_{IL} = 0.8V, V_{OH} = 30V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_{IH} = 2V	I_{OL} = 100mA		0.25	0.4	V
			I_{OL} = 300mA		0.5	0.7	
I_{IH}	High-level input current	V_{CC} = 5.25V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V			−1	−1.6	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5.25V, V_I = 0V			11	14	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = 5.25V, V_I = 5V			56	71	mA

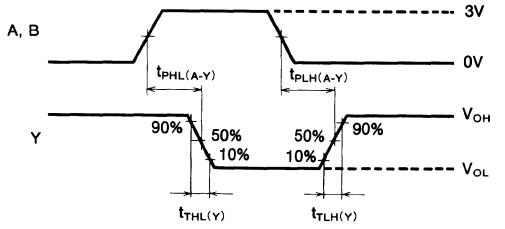
* : A typical value at T_a = 25℃

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃, unless otherwise noted)

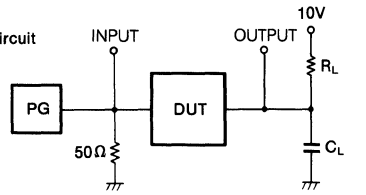
Symbol (Note 1)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(A-Y)}$	Low-to-high-level output, high-to-low-level output propagation time, from input A, B, to output Y	I_O≈200mA, C_L = 15pF, R_L = 50Ω (Notes 2, 3)		26	35	ns
$t_{PHL(A-Y)}$				24	35	ns
$t_{TLH(Y)}$	Low-to-high-level output, high-to-low-level output transition time, output Y			6	10	ns
$t_{THL(Y)}$				9	15	ns

Note 1 : Symbols are representative examples

TIMING DIAGRAM (Reference level = 1.5V)



Note 2 : Test circuit



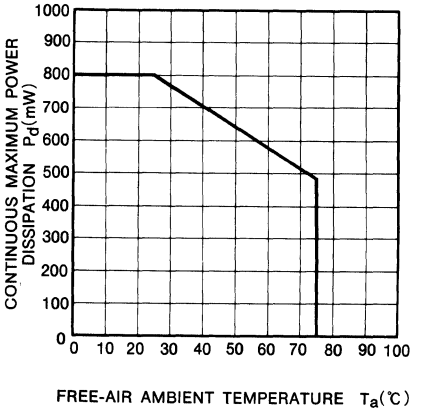
1) The pulse generator (PG) has the following characteristics
$t_r \leqq 5ns$, $t_f \leqq 10ns$, PRR = 1MHz,
$t_{PW} = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

2) C_L includes probe and jig capacitance

Note 3 : Output breakdown voltage drops upon switching
Example· $I_{OL} \cong 300mA$ @ $V_O \cong 15V$ and $I_{OL} \cong 100mA$ @ $V_O \cong 20V$ In case of inductive load use, lower supply voltage. When driving a relay be sure to use a diode in the relay coil to protect against the IC being damaged by relay coil generated counter-electromotive force or when relay coil voltage drops below 12V.

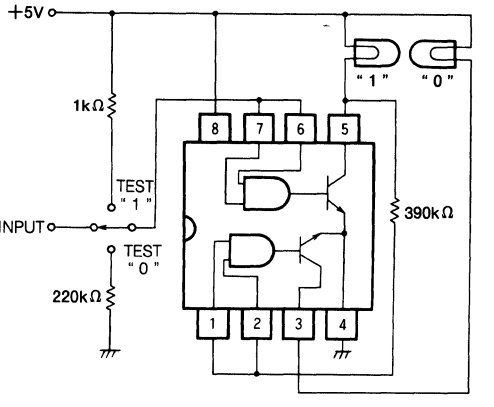
TYPICAL CHARACTERISTICS

HEAT DISSIPATION CHARACTERISTICS



APPLICATION EXAMPLE

TTL or DTL POSITIVE LOGIC LEVEL DETECTOR



MITSUBISHI ELECTRIC

M54603P

DUAL PERIPHERAL POSITIVE OR DRIVER

DESCRIPTION

M54603P is a semiconductor integrated circuit containing 2 circuits with TTL constructed logical OR drivers, each having high output current and high breakdown output voltage characteristics.

FEATURES

- High output current (I_O=300mA)
- High breakdown output voltage (V_O=30V)
- High speed switching (t_{pd}=17ns)
- A small 8 pin DIL package

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

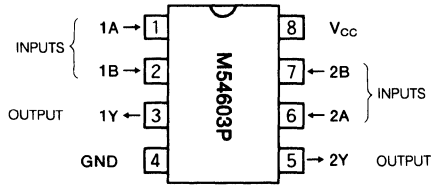
FUNCTION

The output being an open collector, each circuit is capable of handling a maximum output current of 300mA when in low-level output and, when in high-level output, a maximum voltage of 30V can be applied. As mean propagation delay time is 17ns, high speed switching is possible. Supply voltage being 5V ± 5% and input being TTL, this IC can be connected directly to TTL. This IC has a broad range of application as a relay and lamp driver as well as a MOS MEMORY driver.

FUNCTION TABLE

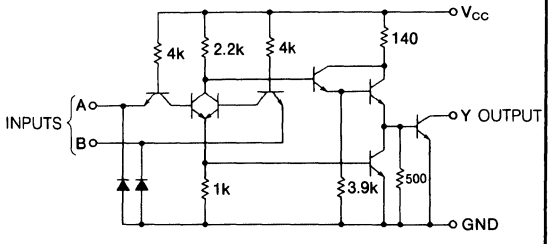
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

PIN CONFIGURATION (TOP VIEW)



Outline 8P4

CIRCUIT SCHEMATIC (EACH DRIVER)



Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = 0~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_{IE}	Interemitter voltage		5.5	V
V_O	Output voltage	High-level state	30	V
I_O	Output current	Low-level state	300	mA
P_d	Power dissipation	$T_a \leq 25$℃	800	mW
T_{opr}	Operating temperature		0~75	℃
Tstg	Storage temperature		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_O	Output voltage	High-level state			24	V
I_{OL}	Low-level output current	V_{OL} = 0.4V			100	mA
		V_{OL} = 0.7V			300	

ELECTRICAL CHARACTERISTICS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −12mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75V, V_{IH} = 2V, V_{OH} = 30V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 100mA		0.25	0.4	V
		V_{IL} = 0.8V	I_{OL} = 300mA		0.5	0.7	
I_{IH}	High-level input current	V_{CC} = 5.25V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V			−1	−1.6	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5.25V, V_I = 5V			8	11	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = 5.25V, V_I = 0V			54	68	mA

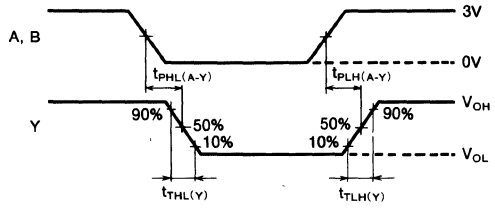
* : A typical value at T_a = 25℃.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃, unless otherwise noted)

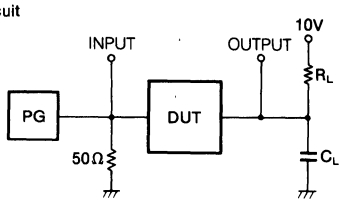
Symbol (Note 1)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(A-Y)}$	Low-to-high-level output, high-to-low-level output propagation time; from input A, B to output Y	I_O≈200mA, C_L = 15pF, R_L = 50Ω (Notes 2, 3)		18	25	ns
$t_{PHL(A-Y)}$				16	25	ns
$t_{TLH(Y)}$	Low-to-high-level output, high-to-low-level output transition time; output Y			6	10	ns
$t_{THL(Y)}$				9	15	ns

Note 1 : Symbols are representative examples

TIMING DIAGRAM (Reference level = 1.5V)



Note 2 : Test circuit

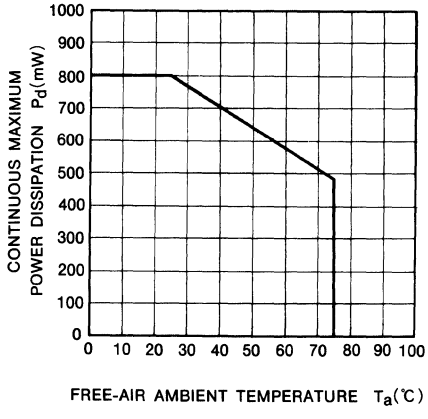


1. The pulse generator (PG) has the following characteristics: $t_r \leqq 10ns$, $t_f \leqq 5ns$, PRR = 1MHz, $t_{PW} = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
2. C_L includes probe and jig capacitance.

Note 3 : Output breakdown voltage drops upon switching. Examples: $I_{OL} \cong 300mA$ @ $V_O \cong 15V$ and $I_{OL} \cong 100mA$ @ $V_O \cong 20V$. In case of inductive load use, lower supply voltage. When driving a relay be sure to use a diode in the relay coil to protect against the IC being damaged by relay coil generated counter-electromotive force or when relay coil voltage drops below 12V.

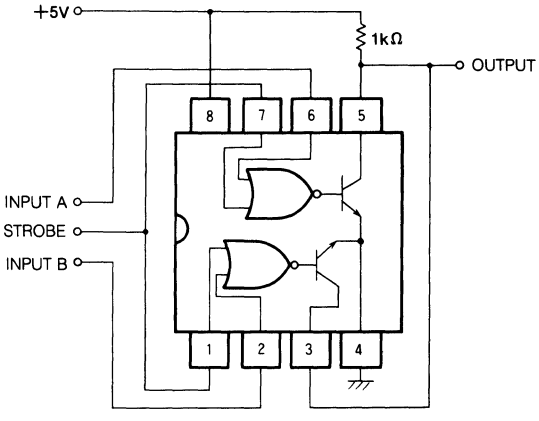
TYPICAL CHARACTERISTICS

HEAT DISSIPATION CHARACTERISTICS



APPLICATION EXAMPLE

LOGIC SIGNAL COMPARATOR



M54604P

DUAL PERIPHERAL POSITIVE NOR DRIVER

DESCRIPTION

M54604P is a semiconductor integrated circuit containing 2 circuits with TTL constructed logical NOR drivers, each having high output current and high breakdown output voltage characteristics.

FEATURES

- High output current (I_O=300mA)
- High breakdown output voltage (V_O=30V)
- High speed switching (t_{pd}=25ns)
- A small 8 pin DIL package

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

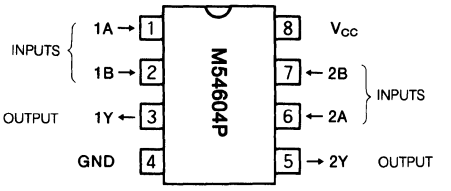
FUNCTION

The output being an open collector, each circuit is capable of handling a maximum output current of 300mA when in low-level output and, when in high-level output, a maximum voltage of 30V can be applied. As mean propagation delay time is 25ns, high speed switching is possible. Supply voltage being 5V ± 5% and input being TTL, this IC can be connected directly to TTL. This IC has a broad range of application as a relay and lamp driver as well as a MOS MEMORY driver.

FUNCTION TABLE

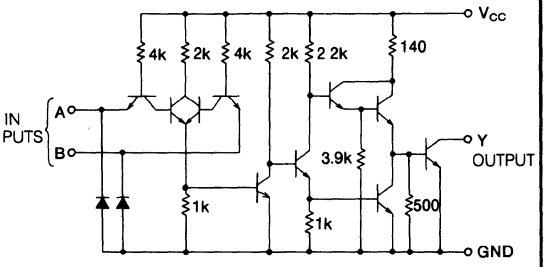
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 8P4

CIRCUIT SCHEMATIC (EACH DRIVER)



Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_{IE}	Interemitter voltage		5.5	V
V_O	Output voltage	High-level state	30	V
I_O	Output current	Low-level state	300	mA
P_d	Power dissipation	$T_a \leq 25$℃	800	mW
T_{opr}	Operating temperature		0~75	℃
Tstg	Storage temperature		−65~+150	℃

MITSUBISHI ELECTRIC

RECOMMENDED OPERATING CONDITIONS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_O	Output voltage	High-level state			24	V
I_{OL}	Low-level output current	V_{OL} = 0.4V			100	mA
		V_{OL} = 0.7V			300	

ELECTRICAL CHARACTERISTICS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −12mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75V, V_{IH} = 0.8V, V_{OH} = 30V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_{IH} = 2V	I_{OL} = 100mA		0.25	0.4	V
			I_{OL} = 300mA		0.5	0.7	
I_{IH}	High-level input current	V_{CC} = 5.25V	V_I = 2.4V			40	μA
			V_I = 4.5V			60	
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V			−1	−1.6	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5.25V, V_I = 0V			13	17	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = 5.25V, V_I = 5V			61	79	mA

* : A typical value at T_a = 25℃.

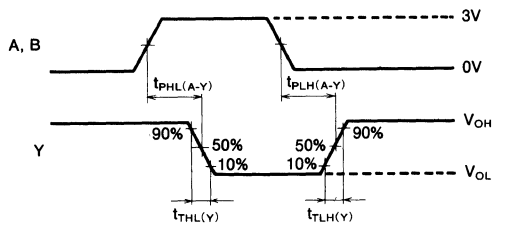
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃, unless otherwise noted)

Symbol (Note 1)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(A-Y)}$	Low-to-high-level output, high-to-low-level output propagation time, from input A, B to output Y	$I_O \approx 200$mA, C_L = 15pF, R_L = 50Ω (Notes 2, 3)		27	35	ns
$t_{PHL(A-Y)}$				24	35	ns
$t_{TLH(Y)}$	Low-to-high-level output, high-to-low-level output transition time; output Y			6	10	ns
$t_{THL(Y)}$				9	15	ns

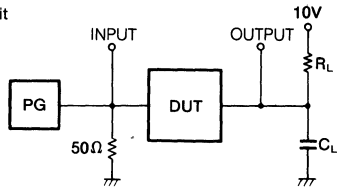
Note 1 : Symbols are representative examples

DUAL PERIPHERAL POSITIVE NOR DRIVER

TIMING DIAGRAM (Reference level = 1.5V)



Note 2 : Test circuit

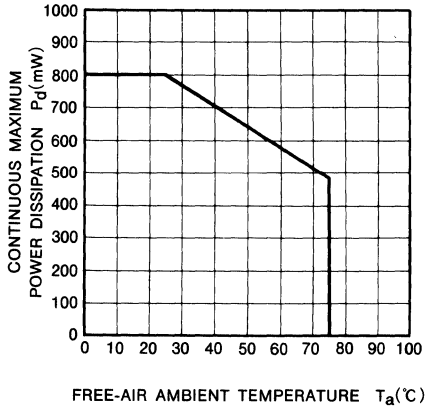


1. The pulse generator (PG) has the following characteristics: $t_r \leqq 10ns$, $t_f \leqq 5ns$, PRR = 1MHz, $t_{PW} = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$
2. C_L includes probe and jig capacitance.

Note 3 : Output breakdown voltage drops upon switching Examples: $I_{OL} \cong 300mA$ @ $V_O \cong 15V$ and $I_{OL} \cong 100mA$ @ $V_O \cong 20V$. In case of inductive load use, lower supply voltage. When driving a relay be sure to use a diode in the relay coil to protect against the IC being damaged by relay coil generated counter-electromotive force or when relay coil voltage drops below 12V.

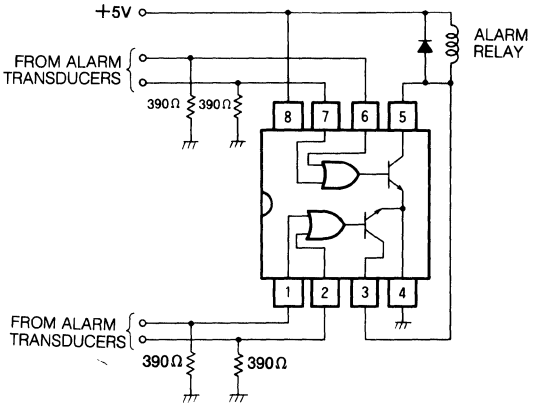
TYPICAL CHARACTERISTICS

HEAT DISSIPATION CHARACTERISTICS



APPLICATION EXAMPLE

ALARM DETECTOR



MITSUBISHI ELECTRIC

M54605P

DUAL PERIPHERAL POSITIVE NAND DRIVER

DESCRIPTION

M54605P is a semiconductor integrated circuit containing 2 circuits with TTL constructed logical AND gates and high current, high breakdown voltage NPN transistors.

FEATURES

- AND gates and NPN transistors are independent of each other.
- High current (I_C = 300mA), high breakdown voltage (BV_{CER}=30V) NPN transistors
- High speed switching (t_{pd}=28ns)
- SUB pin provided
- Strobe input provided

APPLICATION

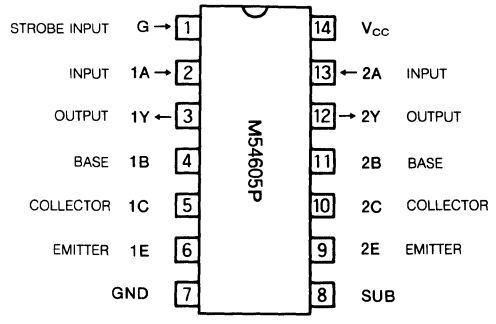
General purpose, for use in industrial and consumer digital equipment.

FUNCTION

This is a high speed driver containing two 2-input AND gates with two NPN transistors (I_C = 300mA, BV_{CER} = 30V, $R_{BE} \leqq 500\Omega$).

A wide range of application is insured as AND gate outputs and NPN transistor bases can be either connected or used as independent circuits. SUB pin must always be at the most negative device voltage for proper operation, whether it is GND line or the IC itself.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTION TABLE

Gate only

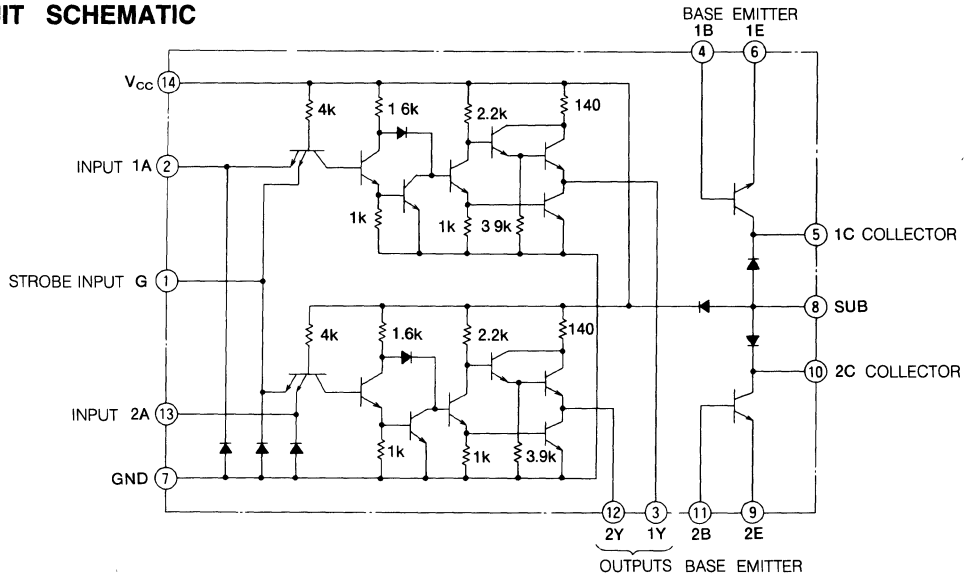
A	G	Y
L	L	L
L	H	L
H	L	L
H	H	H

Gate and transistor

A	G	C
L	L	H
L	H	H
H	L	H
H	H	L

When gate output Y and transistor base B, and when each emitter E and GND are connected directly and collector C is the output

CIRCUIT SCHEMATIC



Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = 0~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_{IE}	Interemitter voltage		5.5	V
V_{CCS}	V_{CC} to substrate voltage		35	V
V_{CS}	Collector to substrate voltage		35	V
V_{CB}	Collector base voltage		35	V
V_{CE}	Collector emitter voltage	The base-emitter resistance (R_{BE}) is $R_{BE} \leqq 500\Omega$.	30	V
V_{EB}	Emitter base voltage		5	V
I_C (Note 1)	Collector current		300	mA
P_d	Power dissipation	$T_a \leqq 25$℃	800	mW
T_{opr}	Operating temperature		0~75	℃
T_{stg}	Storage temperature		−65~+150	℃

Note 1 : Both halves of these dual circuits may conduct rated current simultaneously; but only if used within heat dissipation rating.

RECOMMENDED OPERATING CONDITIONS (T_a = 0~75℃, unless otherwise noted)

TTL Gate

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
F_O	Fan out			10	—

Gate and transistor combined

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_O	Output voltage	High-level state			24	V
I_{OL}	Low-level output current	V_{OL} = 0.4V			100	mA
		V_{OL} = 0.7V			300	

ELECTRICAL CHARACTERISTICS (T_a = 0~75℃, unless otherwise noted)

TTL Gate

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −12mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_{IH} = 2V, I_{OH} = −400μA		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OL} = 16mA			0.22	0.4	V
$I_{IH(A)}$	High-level input current	Input A	V_{CC} = 5.25V	V_I = 2.4V			40	μA
				V_I = 4.5V			60	
$I_{IH(G)}$		Input G	V_{CC} = 5.25V	V_I = 2.4V			80	μA
				V_I = 4.5V			120	
$I_{IL(A)}$	Low-level input current	Input A	V_{CC} = 5.25V, V_I = 0.4V				−1.6	mA
$I_{IL(G)}$		Input G	V_{CC} = 5.25V, V_I = 0.4V				−3.2	mA
I_{OS}	Short circuit output current (Note 2)		V_{CC} = 5.25V		−18		−55	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V, V_I = 5V			10	14	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = 5.25V, V_I = 0V			15	20	mA

* : A typical value at T_a = 25℃.

Transistor

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
BV_{CBO}	Collector base breakdown voltage	$I_C = 100\mu A$, $I_E = 0$		35			V
BV_{CER}	Collector emitter breakdown voltage	$I_C = 100\mu A$, $R_{BE} = 500\Omega$		30			V
BV_{EBO}	Emitter base breakdown voltage	$I_E = 100\mu A$, $I_C = 0$		5			V
h_{FE}	Static forward current transfer ratio (Note 3)	$V_{CE} = 3V$, $T_a = 25℃$	$I_C = 100mA$	25			—
			$I_C = 300mA$	30			
		$V_{CE} = 3V$, $T_a = 0℃$	$I_C = 100mA$	20			
			$I_C = 300mA$	25			
V_{BE}	Base emitter voltage (Note 3)	$I_B = 10mA$, $I_C = 100mA$			0.85	1	V
		$I_B = 30mA$, $I_C = 300mA$			1.05	1.2	
$V_{CE(sat)}$	Collector emitter saturation voltage (Note 3)	$I_B = 10mA$, $I_C = 100mA$			0.25	0.4	V
		$I_B = 30mA$, $I_C = 300mA$			0.5	0.7	

* : A typical value at T_a=25℃.

With TTL Gate output connected to transistor base 'B', and each emitter 'E' and GND connected

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_O = 30V$				100	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 100mA$		0.25	0.4	V
		$V_I = 2V$	$I_{OL} = 300mA$		0.5	0.7	
I_{CCL}	Supply current, all outputs low	$V_{CC} = 5.25V$, $V_I = 5V$				71	mA

* : A typical value at $T_a = 25℃$.
Note 2 : Not more than one output should be shorted at a time.
3 : Test with pulse width of 300μs, and duty cycle of ≦2% pulse.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25℃$, unless otherwise noted)

TTL Gate

Symbol (Note 4)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(A-Y)}$	Low-to-high-level output, high-to-low-level output propagation time; from input A, G to output Y	$C_L = 15pF$, $R_L = 400\Omega$ (Note 5)		20	32	ns
$t_{PHL(A-Y)}$				16	25	ns

Output transistor

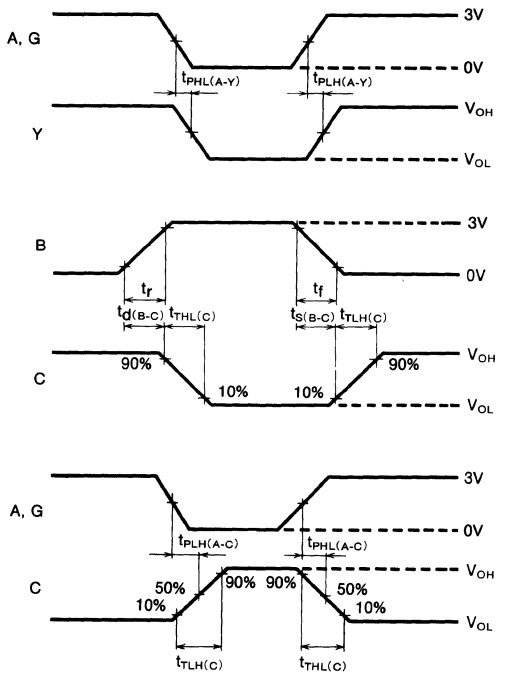
Symbol (Note 4)	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(B-C)}$	Delay time	$I_C \approx 200mA$, $I_{B(1)} = 20mA$		8	15	ns
$t_{THL(C)}$	Rise time	$I_{B(2)} = -40mA$, $V_{BE(off)} = -1V$		12	20	ns
$t_{S(B-C)}$	Stotage time	$C_L = 15pF$, $R_L = 50\Omega$		7	15	ns
$t_{TLH(C)}$	Fall time	(Notes 6, 7)		6	15	ns

TTL Gate and output transistor combined

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(A-C)}$	Low-to-high-level output, high-to-low-level output propagation time; from input A, G to output C	$I_C \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$ (Notes 7, 8)		28	40	ns
$t_{PHL(A-C)}$				28	40	ns
$t_{TLH(C)}$	Low-to-high-level output, high-to-low-level output transition time; output C			7	12	ns
$t_{THL(C)}$				9	15	ns

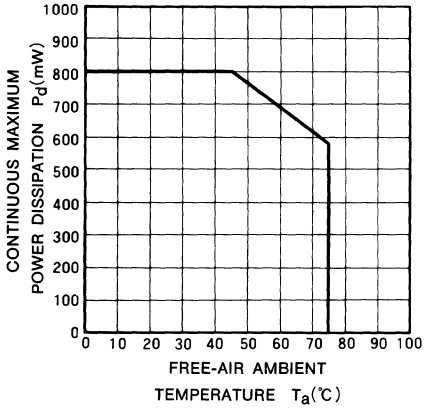
Note 4 : Symbols indicate representative examples.

TIMING DIAGRAM (Reference level = 1.5V)

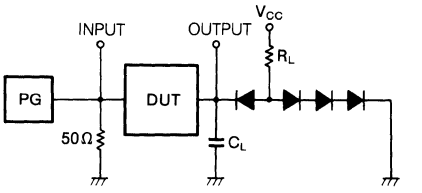


TYPICAL CHARACTERISTICS

HEAT DISSIPATION CHARACTERISTICS

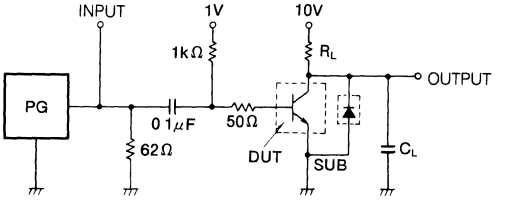


Note 5 : Measurement circuit



1. The pulse generator (PG) has the following characteristics: $t_r \leqq 5ns$, $t_f \leqq 10ns$, PRR = 1MHz, $t_{PW} = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$
2. All diodes are high speed switching diodes ($t_{rr} \leqq 4ns$).
3. C_L includes probe and jig capacitance.

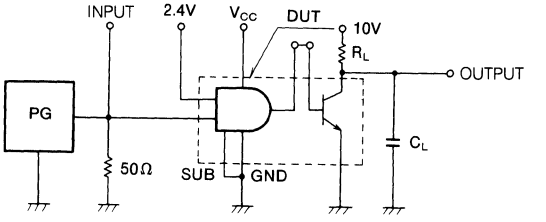
Note 6 : Test circuit



1. The pulse generator (PG) has the following characteristics: $t_r \leqq 5ns$, $t_f \leqq 5ns$, DUTY CYCLE ≦ 1%, $t_{PW} = 300ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

Note 7 : Output breakdown voltage drops upon switching
Examples: $I_{OL} \cong 300mA$ @ $V_O \cong 15V$ and $I_{OL} \cong 100mA$ @ $V_O \cong 20V$ In case of inductive load use, lower drive supply voltage.
When driving a relay be sure to use a diode in the relay coil to protect against the IC being damaged by relay coil generated counter-electromotive force or when relay coil voltage drops below 12V.

Note 8 : Measurement circuit

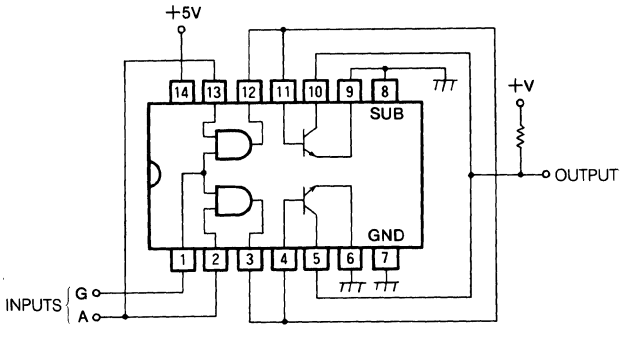


1. The pulse generator (PG) has the following characteristics $t_r \leqq 5ns$, $t_f \leqq 10ns$, PRR = 1MHz, $T_{PW} = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

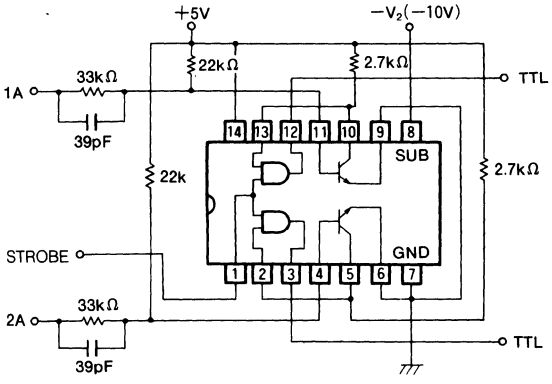
MITSUBISHI ELECTRIC

APPLICATION EXAMPLES

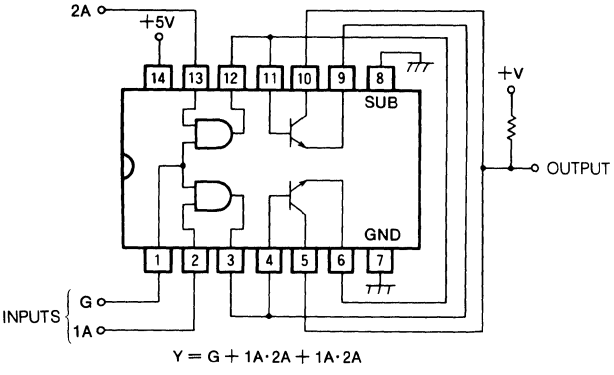
500mA SINK



DUAL MOS TO TTL CONVERTER

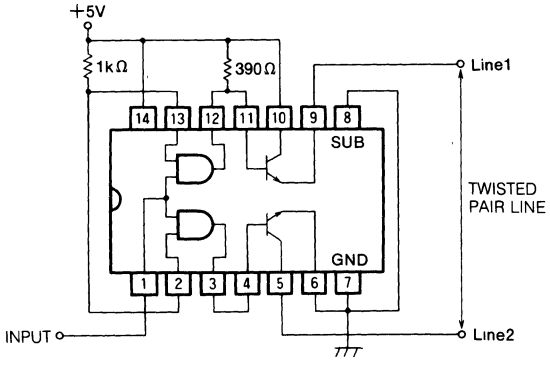


GATED COMPARATOR

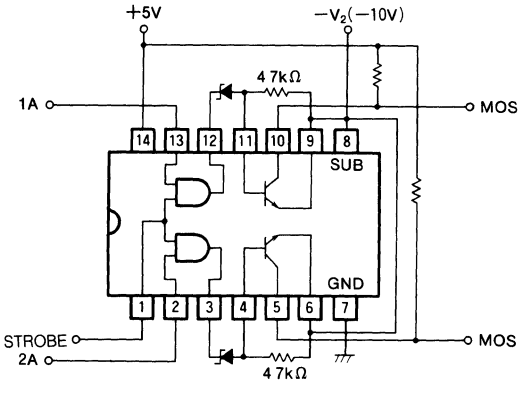


$Y = G + 1A \cdot 2A + 1A \cdot 2A$

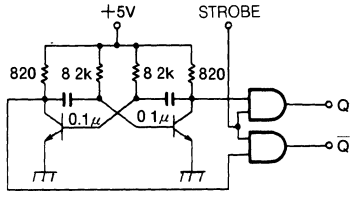
BALANCED LINE DRIVER

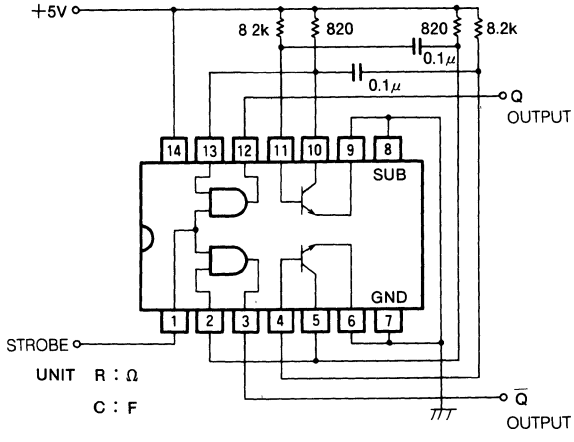


DUAL TTL TO MOS CONVERTER



SQUARE-WAVE GENERATOR





M54610P

8-BIT PARALLEL DATA INTERFACE FOR PRINTER

DESCRIPTION

The M54610P is a semiconductor integrated circuit consisting of an 8-bit parallel data interface.

FEATURES

- I/O electrical characteristics equivalent to LSTTL
- 3-state 8-bit data output
- Strobe signal with polarity switching input
- Wide operating temperature range T_a=−20∼+75℃

APPLICATION

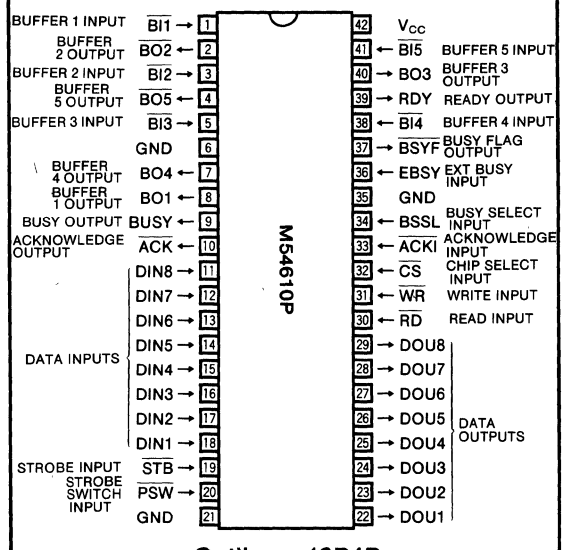
Printer

FUNCTION

The M54610P, when used in a printer, is capable of implementing a standard 8-bit parallel data interface. As shown in the timing diagram, printing data DIN 1 through 8 and strobe pulses $\overline{STB}$ are input from a host computer. Data are exchanged by outputing the BUSY and $\overline{ACK}$ (ACKNOWLEDGE) signals to the host computer.

Control signals EBSY, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$ and $\overline{ACKI}$ are input from a printer controller, and this IC outputs DOU 1 through 8, and $\overline{BSYF}$.

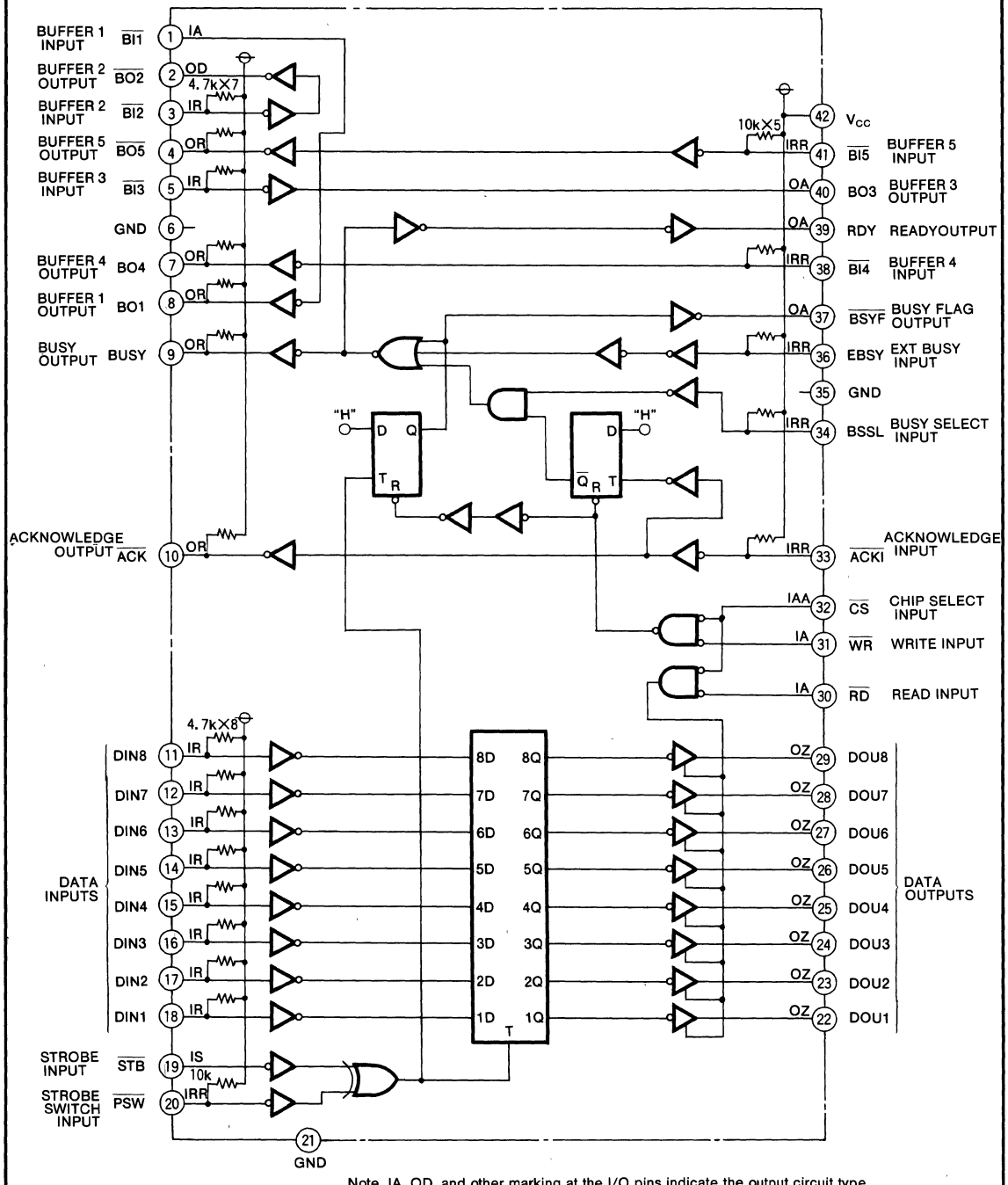
PIN CONFIGURATION (TOP VIEW)



Outline 42P4B

8-BIT PARALLEL DATA INTERFACE FOR PRINTER

BLOCK DIAGRAM

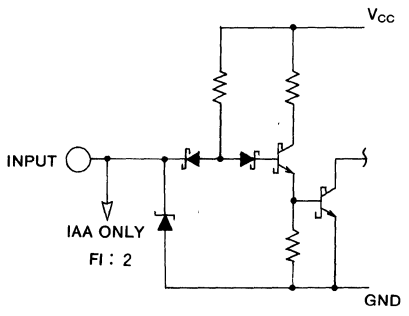


Note. IA, OD, and other marking at the I/O pins indicate the output circuit type

I/O CIRCUIT

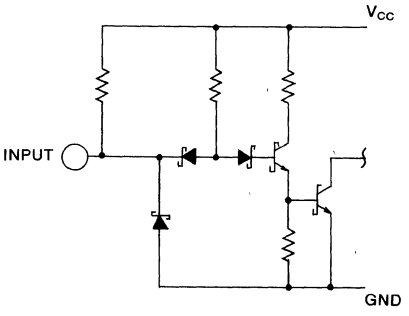
1

INPUT CIRCUIT TYPE : IA, IAA



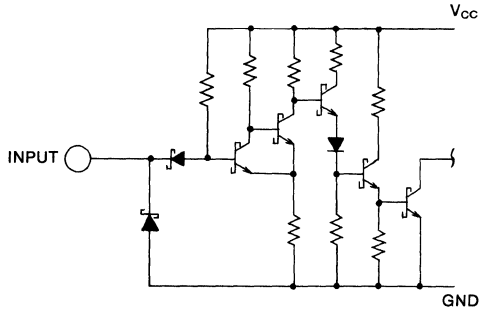
2

INPUT CIRCUIT TYPE : IR, IRR



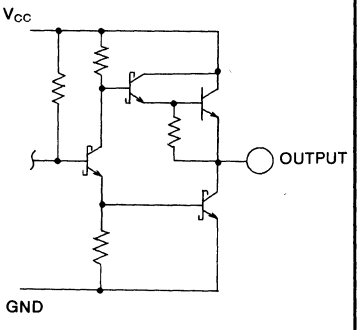
3

INPUT CIRCUIT TYPE : IS



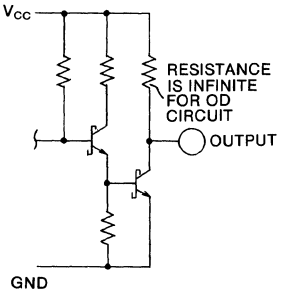
4

OUTPUT CIRCUIT TYPE : OA



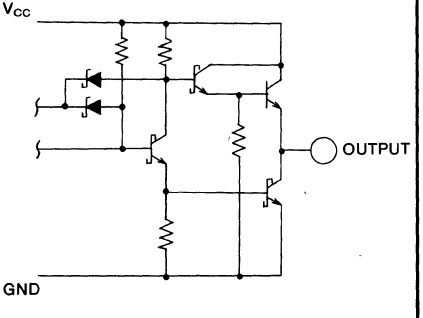
5

OUTPUT CIRCUIT TYPE : OR, OD



6

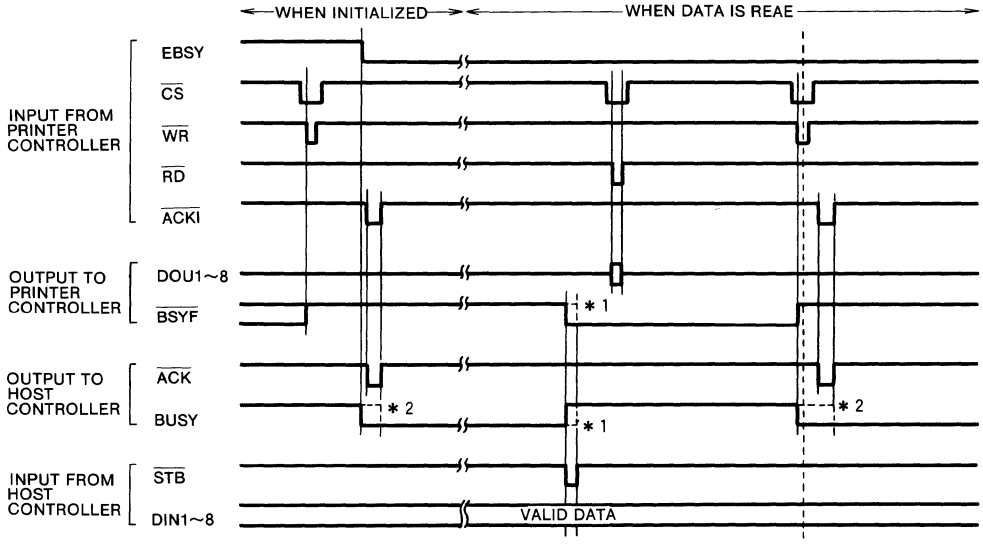
OUTPUT CIRCUIT TYPE : OZ



PIN DESCRIPTION

Pin number	Symbol	Description
9	BUSY	BUSY output to host
10	$\overline{ACK}$	ACKNOWLEDGE output to host
11 ⟆ 18	DIN8 ⟆ DIN1	8-bit parallel data input from host
19	$\overline{STB}$	Data strobe pulse input from host
20	$\overline{PSW}$	Polarity switching input for $\overline{STB}$
6, 21, 35	GND	GND
22 ⟆ 29	DOU1 ⟆ DOU8	8-bit parallel data output to printer controller (3-state)
30	$\overline{RD}$	Read input from printer controller
31	$\overline{WR}$	Write input from printer controller
32	$\overline{CS}$	Chip select input from printer controller
33	$\overline{ACKI}$	ACKNOWLEDGE input from printer controller
34	BSSL	BUSY select input. Switches busy timing
36	EBSY	External BUSY input from printer controller
37	BSYF	BUSY flag output to printer controller
39	RDY	Inverted BUSY output to printer controller
42	V_{CC}	Power supply

OPERATIONAL TIMING DIAGRAM



* 1 : The broken lines of $\overline{BSYF}$ and BUSY show the timing when $\overline{PSW}$ is low

* 2 : The broken lines of BUSY signal show the timing when BSSL is low

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+7	V
V_I	Input voltage	IR, IS		−0.5∼+15	V
		IA, IAA, IRR		−0.5∼V_{CC}	
V_O	Output voltage	OR	When output is high	−0.5∼+15	V
		OA, OD	When output is high	−0.5∼V_{CC}	
		OZ	When output is high	−0.5∼+5.5	
Topr	Operating temperature			−20∼+75	℃
Tstg	Storage temperature			−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	OR, OA	0		−400	μA
		OZ	0		−2.6	mA
		OD V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	OR, OA	0		8	mA
		OZ	0		8	
		OD	0		100	

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage	IA, IAA, IRR, IR			2			V
V_{IL}	Low-level input voltage	IA, IAA, IRR, IR					0.8	V
V_{T+}	Positive threshold voltage	IS	V_{CC}=5V		1.4	1.6	1.9	V
V_{T-}	Negative threshold voltage	IS	V_{CC}=5V		0.5	0.8	1.0	V
$V_{T+}-V_{T-}$	Hysteresis width	IS	V_{CC}=5V		0.4	0.8		V
V_{IC}	Input clamp voltage	All inputs	V_{CC}=4.75V, I_I=−1mA				−1.5	V
V_{OH}	High-level output voltage	OA	V_{CC}=4.75V	I_{OH}=−400μA	2.7	3.1		V
		OZ		I_{OH}=−2.6mA	2.4	2.9		
		OR		I_{OH}=−400μA	2.4	3.1		
I_{OH}	High-level output current	OD	V_{CC}=4.75V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage	OD	V_{CC}=4.75V	I_{OL}=24mA		0.3	0.4	V
		OA, OZ		I_{OL}=8mA		0.3	0.4	
		OR		I_{OL}=8mA		0.3	0.4	
I_{OZH}	Off-state high-level output current	OZ	V_{CC}=5.25V				20	μA
I_{OZL}	Off-state low-level output current	OZ	V_{CC}=5.25V				−20	μA
I_{IH}	High-level input current	IA, IS	V_{CC}=5.25V, V_I=2.7V				20	μA
		IAA					40	
I_{IH}	High-level input current	IRR	V_{CC}=5.25V, V_I=2.7V		−0.2		−0.4	mA
		IR			−0.4		−0.8	
I_{IL}	Low-level input current	IA, IS	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		IAA					−0.8	
I_{IL}	High-level input current	IRR	V_{CC}=5.25V, V_I=0.4V				−1.1	mA
		IR					−1.8	
I_{OS}	Output short-circuit current	OA	(Note 1)		−20		−100	mA
		OZ	V_{CC}=5.25V, V_O=0V		−30		−130	
		OR			−0.8		−1.5	
I_{CC}	Supply current		V_{CC}=5.25V Point A in the operational timing diagram. When 4.5V : $\overline{BI1}$ Open : $\overline{BI2}$, BSSL, $\overline{BI5}$ 0V : $\overline{BI3}$, DIN1 through 8, EBSY, $\overline{BI4}$			35	45	mA

* : Typical values are at V_{CC}=5V, T_a=25℃.
Note 1. Measurements are conducted in the shortest possible time, and no two outputs are shorted simultaneously.

SWITCHING CHARACTERISTICS (V_{CC}=5V T_a=25℃, unless otherwise noted)

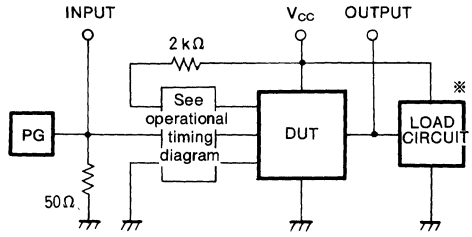
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low to high-level and high to low-level propagation time,				200	ns
t_{PHL}	1 buffer				200	ns
t_{PLH}	Low to high-level and high to low-level propagation time,				300	ns
t_{PHL}	2 buffer				300	ns
t_{PLH}	Low to high-level and high to low-level output propagation time,				500	ns
t_{PHL}	from EBSY to BUSY				500	ns
t_{PLH}	Low to high-level and high to low-level output propagation time,				500	ns
t_{PHL}	from $\overline{STB}$ to DOU1 through 8				500	ns
t_{PLH}	Low to high-level output propagation time, from $\overline{STB}$ to BUSY				500	ns
t_{PHL}	High to low-level output propagation time, from $\overline{ACKI}$ to BUSY				500	ns
t_{PHL}	High to low-level output propagation time, from $\overline{WR}$ to BUSY				500	ns
t_{PLH}	Low to high-level output propagation time, from $\overline{WR}$ to $\overline{BSYF}$				500	ns
t_{PHL}	High to low-level output propagation time, from $\overline{STB}$ to $\overline{BSYF}$				500	ns
t_{PZH}	High-level output enable time	R_L= 1 kΩ, C_L=30pF			80	ns
t_{PZL}	Low-level output enable time	R_L= 1 kΩ, C_L=30pF			80	ns
t_{PHZ}	High-level output disable time	R_L= 1 kΩ, C_L= 5 pF			100	ns
t_{PLZ}	High-level output disable time	R_L= 1 kΩ, C_L= 5 pF			100	ns

Note 2. Refer to switching test circuits for measurement conditions.

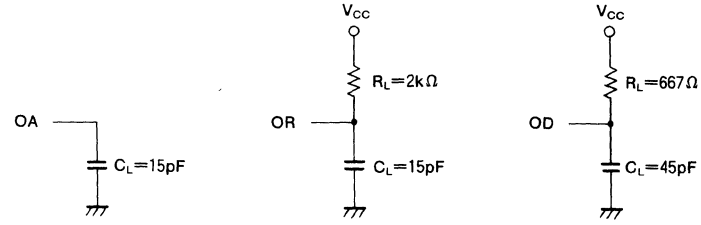
TIMING REQUIREMENTS (V_{CC}=5V T_a=25℃, unless otherwise noted)

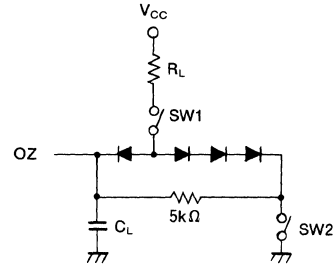
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(STB)}$	$\overline{STB}$ low-level, high-level pulse width		500			ns
$t_{W(ACK)}$	$\overline{ACKI}$ pulse width		500			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		200			ns
$t_{SU(DIN)}$	DIN1 through DIN8 setup time with respect to $\overline{STB}$		500			ns
$t_{h(DIN)}$	DIN1 through DIN8 hold time with respect to $\overline{STB}$		500			ns
$t_{rec(WR)}$	$\overline{WR}$ recovery time with respect to $\overline{ACKI}$		500			ns

SWITCHING TEST CIRCUIT



※The load circuit has the following characteristics depending on the output circuits





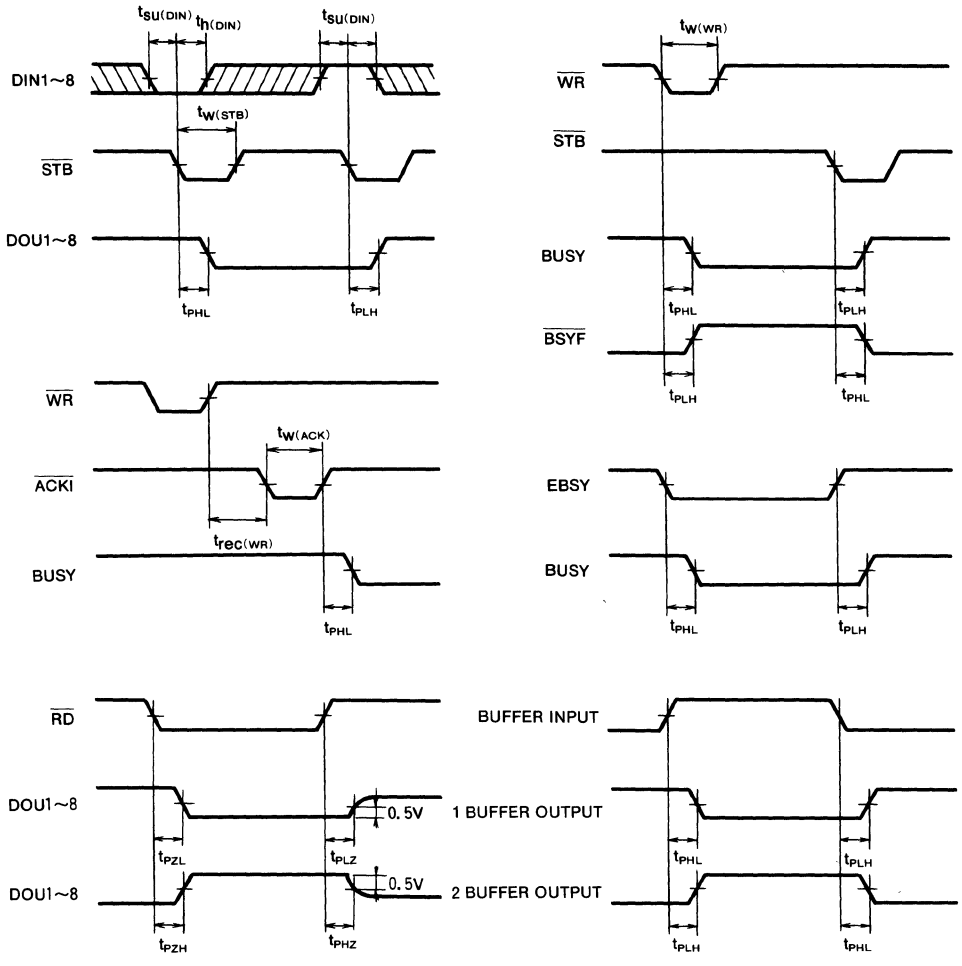
Parameter	SW 1	SW 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics : PRR=100kHz, t_r=6ns, t_W=5μs, V_P=3V_{P-P}, Z_O=50Ω

(2) The diodes used are all high-speed switching diodes (t_{rr}≦4ns).

(3) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM (Reference voltage=1.3V)



The shaded area indicated the period when switching is possible.

M54640P

STEPPER MOTOR DRIVER

DESCRIPTION

The M54640P is bipolar monolithic integrated circuit intended to control and drive the current in one winding of a bipolar stepper motor.

FEATURES

- Wide operating voltage range
- Half-step and full-step mode
- Bipolar drive of stepper motor for maximum motor performance
- Bullt-in protection diodes
- Wide range of current control
- Designed for unstabilized motor supply voltage
- Current levels can be selected in steps or varied continuously

APPLICATION

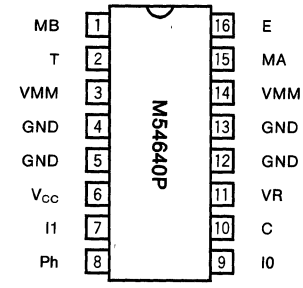
Printer, FDD, HDD

FUNCTION

The M54640P is monolithic IC which cotrols and drives one phase of a bipolar stepper motor with chopper control of the phase current. Current levels may be selected in three by means of two logic inputs which select one of three current comparatortors.

When both of these inputs are high the device is disabled. A separate logic input controls the direction of current flow . A monostable, programmed by an external RC network, sets the curret decay time.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

The power section is a full H-bridge driver with four internal clamp diodes for current reciculation.

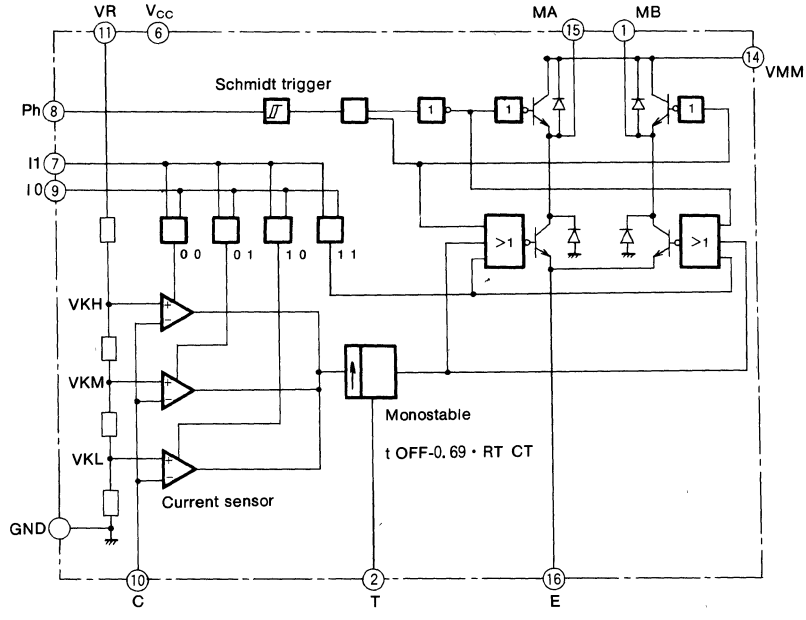
An external connection to the lower cmitters is available for the insertion of a sensing resing resistor.

INPUT LOGIC

If any of the logic inputs is left open the circuit will threat it as a high level input.

I_0	I_1	Current level
H	H	No Current
L	H	Low Current
H	L	Medium Current
L	L	Maximum Current

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=20℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
V_{MM}	Output voltage		−0.3∼45	V
V_L	Logic input Voltage		−0.3∼6	V
V_C	Comparator input Voltage		−0.3∼V_{CC}	V
V_R	Reference input Voltage		−0.3∼15	V
I_L	Logic input Current		−10	mA
I_C	Analog input Current		−10	mA
I_{MM}	Output Current		±1000	mA
P_d	Power Dissipation		1.92	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATIONAL CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{MM}	Driver voltage	10		40	V
I_O	Peak output Current	20		800	mA
t_{PLH}	Rise time logic input			2	μs
t_{PHL}	Fall time logic input			2	μs
T_{ON}	Thernal shutdown temperature		150		℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	Input Voltage	"H"	V_{CC}=5V	2.0		V_{CC}	V
V_{IL}		"L"		0		0.8	
VCH	Comparator threshold Voltage		V_R=5V, I_0=I_1=0	400	430	450	mV
VCM			V_R=5V, I_0=1, I_1=0	240	260	280	
VCL			V_R=5V, I_0=I_1=1	75	90	100	
I_{CO}	Comparator input Current			−20		20	μA
I_{OFF}	Output leakage Current		I_0=I_1=1 (T_a=25℃)			100	μA
V_{sat}	Total suluration Voltage		I_O=500mA			4.0	V
t_{OFF}	Cut off time		V_{MM}=10V, t_{ON} ≧ 5 μs	25	30	35	μs
t_d	Turn off delay		T_a=25℃, dvk/dt ≧ 50mV/μs		1.6	2.0	μs
I_{CC}	Supply Current		V_{CC}=5V			25	mA
P_{tot}	Total power dissipation		Im=500mA, fs=30kHz		1.8	2.3	W
I_{IH}	Input Current	"H"	V_I=2.4V			20	μA
I_{IL}		"L"	V_I=0.4V	0.4			mA

* : Typical values are at T_a=25℃.

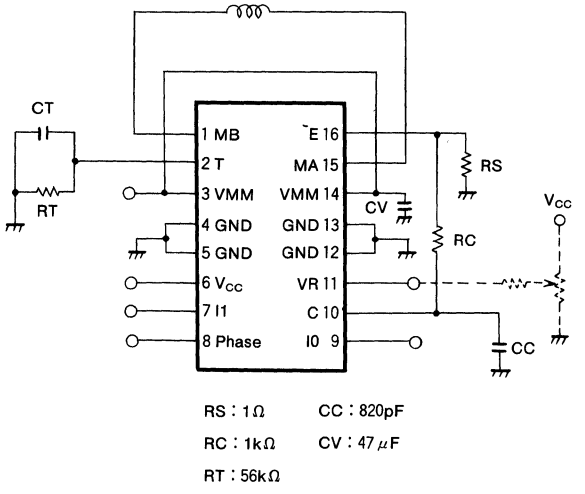


FIGURE 1.

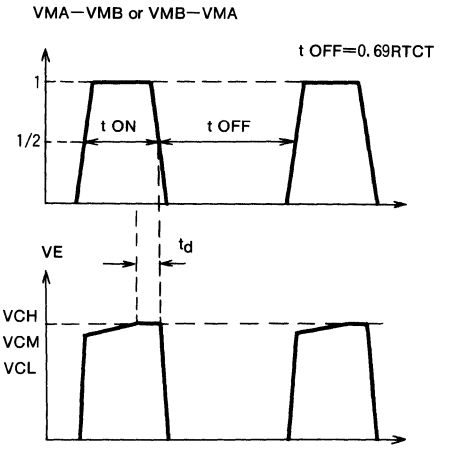


FIGURE 2.

APPLICATION INFORMATION

PHASE

This input determines the direction of current flow in the winding, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to quarantee that no short circuit occurs in the output stage during phase—shift. High level on PHASE-input causes the motor current flow from MA through the winding to MB.

I_0 and I_1

The current level in the motor winding is selected with these input. The values of the different current levels are determined by the reference voltage V_R together with the value of the sensing resistor Rs.

CURRENT SENSOR

This part contains sensing resistor (RS), a low pass filter (Rc , Cc) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_0 and I_1. The motor current flows through the sensing resistor Rs. When the current has increased so that the voltage accross Rs becomes higher than the reference voltage on the other comparator input, the comparator' output goes higt,which triggers the pulse generator and it's output goes high during a fixed pulse time(toff), thus switching off the power feed to the motor winding, and causing the motor current to derease during toff.

SINGLE-PULSE GENETATOR

The pulse generator is monostable triggered on the positive going edge of the comparator output. The monostaBle output is high during the pulse time, toff. Which is determined by the timing components R_T and C_T

$$toff = 0.69 \cdot R_T \cdot C_T$$

The single pulse swtches off the power feed to the motor winding, causing the winding current to decrease during toff.

If a new trigger signal should occur during toff, it is ignored.

ANALOG CONTOROL

The current levels can be varied continuously if V_R is varied as e.g. in Figure 1.

FUNCTIONAL BLOCKS

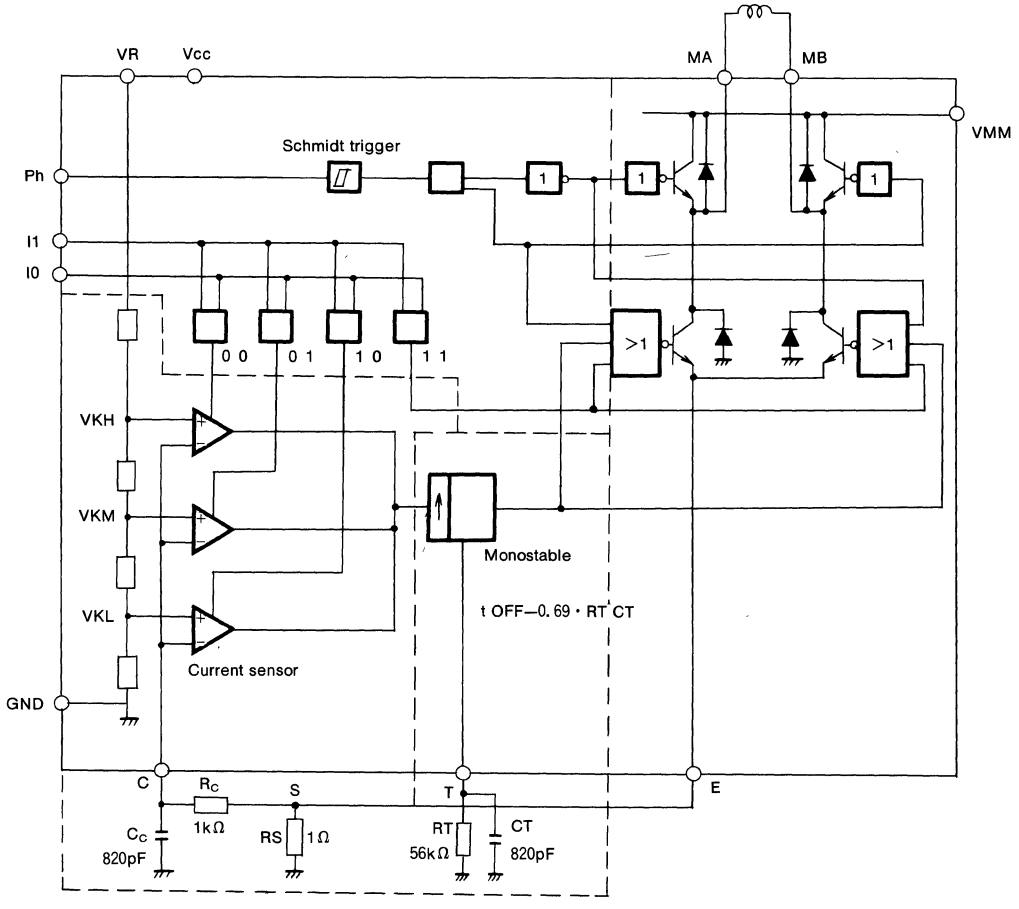


FIGURE 3.

TYPICAL APPLICATION

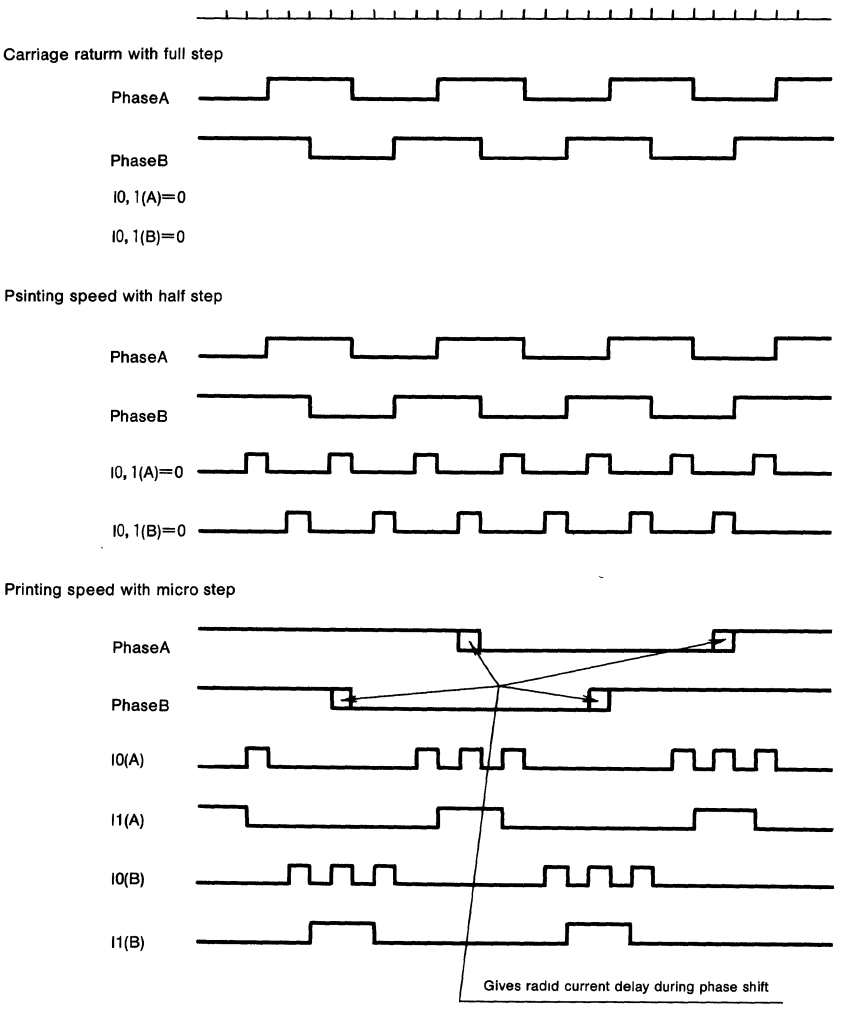


FIGURE 4. SERIAL PRINTER CARRIAGE DRIVE

APPLICATION EXAMPLE

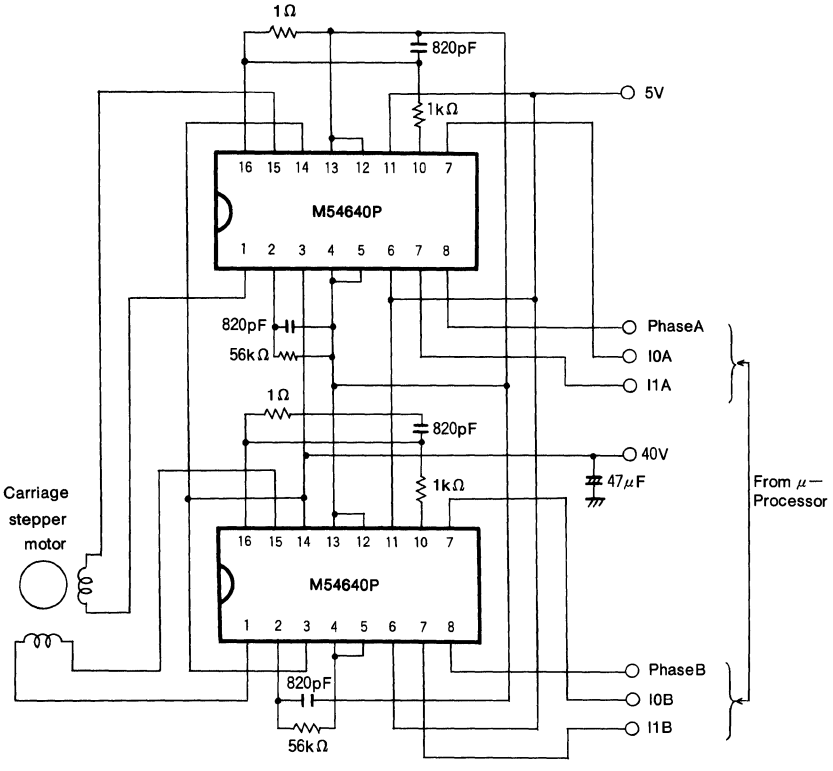


FIGURE 5. PRINCIRAL OPERATING SEQUENCE

M54641L

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

DESCRIPTION

The M54641L, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power driver designed for D-C motor control.

FEATURES

- Wide operating voltage range (V_{CC}=4~10V, $V_{CC'}$(max) =20V)
- Low output saturation voltage in continuos output motor circuit (High voltage between motors)
- Built-in clamp diode
- Output voltage control pin (V_Z)
- Internal thermal shutdown protector ($T_{j(shut)}$=120℃$_{TYP}$)

APPLICATION

Audio tape deck, radio cassette player, VTR

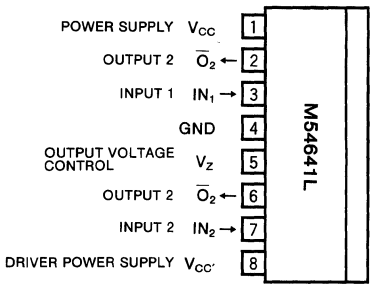
FUNCTION

The M54641L, full bridge motor driver, has the logic circuitry and darlington-per power drivers for bidirectional control of D-C motors operating at currents up to 800mA.

The power supplies for the logic circuitry and the drivers are separated so that the applied voltage to the motor can be controlled by the V_Z or $V_{CC'}$ of the driver power supply voltage.

The internal thermal shut down protector destruction due to blocking of motor, etc.

PIN CONFIGURATION (TOP VIEW)



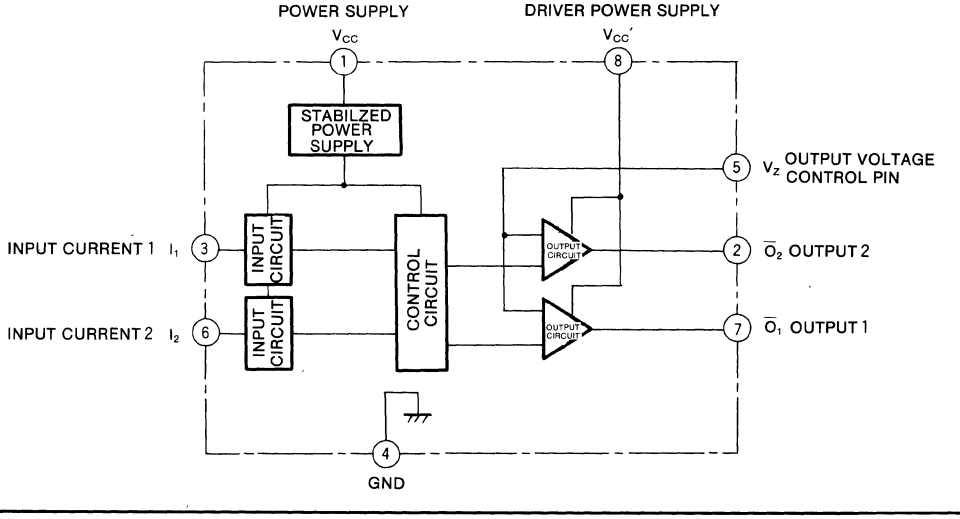
Outline 8P5

LOGIC TRUTH TABLE

Input		Output		Note
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	"OFF" state	"OFF" state	Open
H	L	H	L	↻
L	H	L	H	↺
H	H	L	L	Braking

Protects the IC from thermal

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+12	V
$V_{CC'}$	Driver power supply		−0.5～+20	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～$V_{CC'}$+2.5	V
$I_{O(max)}$	Peak output current	top=10ms top=10ms : repetitive cycle 0.2Hz max	±800	mA
I_O	Continuous output current		±150	mA
P_d	Power dissipation	T_a=60℃	570	mW
Tj	Junction temperature		100	℃
Topr	Operating temperature		−10～+60	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

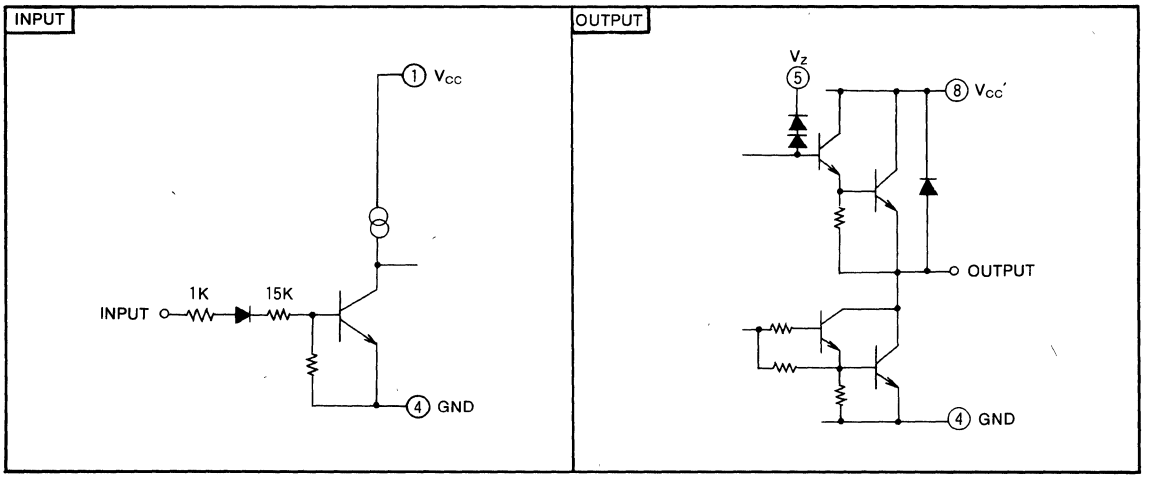
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	10	V
I_O	Output current				±100	mA
V_{IN}	High-level input voltage		3.0		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.6	V
t_S	Motor braking interval		10	100		ms
T_S	Thermal shutdown protector operating temperature (Junction temperature)		100	120		℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ*	Max	
$I_{O(leak)}$	Output lekage current	V_{CC}=20V Vz . open		V_O=20V			100	μA
				V_O=0V			−100	
V_{OH}	High-level output voltage	V_{CC}=12V Vz · open		I_{OH}=−50mA	10.2	10.5		V
				I_{OH}=−100mA	10.0	10.4		
V_{OL}	Low-level output voltage	$V_{CC'}$=12V Vz · open		I_{OH}=50mA		0.1	0.3	V
				I_{OH}=100mA		0.2	0.4	
V_{O1-O2}	Voltage between output(1) and output(2) (voltage between motors)	$V_{CC'}$=12V Vz=7V		I_O=±100mA	6.3	7.0	7.7	V
I_I	Input current	$V_{CC'}$=12V	V_I=3V	Output open		100	180	μA
			V_I=5V			240	380	
I_{CC}	Supply current	V_{CC}=10V $V_{CC'}$=12V		"OFF" state		1.2	3.0	mA
				Clockwise or anti-clockwise		4.5	8.0	
				Braking		7.5	12.0	

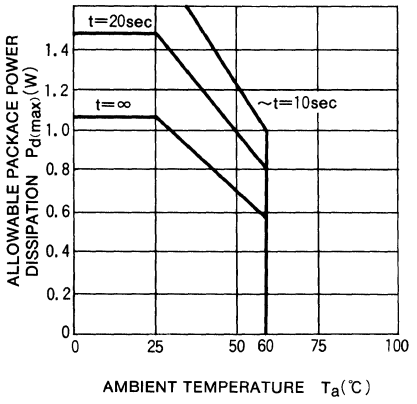
* : Typical values are at T_a=25℃

INPUT/OUTPUT CIRCUIT



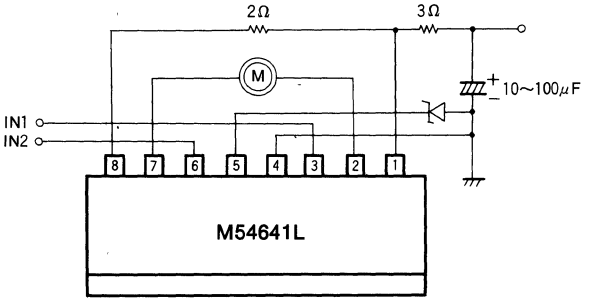
TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



Note 1 : Mounted on an epoxy PC board with Cu cover on one side (5cm×5cm×0.8mmt)
2 : t : time for power application

APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M54642L

BI-DIRECTIONAL MOTOR DRIVER WITH BRAKE FUNCTION

DESCRIPTION

The M54642L is a semiconductor integrated circuit, capable of directly driving bi-directional micro motor.

FEATURES

- Wide operating voltage range (V_{CC}=4~10V, $V_{CC'(max)}$ =20V)
- Low output saturation voltage in continuous output motor circuit (High voltage between motors)
- Built-in clamp diode
- Output voltage control pin (V_Z)
- Internal thermal shutdown protector ($T_{j(shut)}$=120℃$_{TYP}$)
- Additional interrupt input I_1', I_2'

APPLICATION

Audio tape deck, radio cassette player, VTR

FUNCTION

The M54642L is a driver for bi-directional micro motor. The input pin has inputs I_1 and I_2 which are identical to those inputs of the M54641L and interrupt inputs of I_1' and I_2'. The I_1 functions to the I_1' and the I_2, to the I_2'. The I_1' and the I_2', if they are "H", operate just like the I_1 and the I_2 input signals in the M54641L. If the "H" signal is input to the input pin I_1, and the "L" signal is input t_0, the input pin I_2, output $\overline{O}_1$ is "H" and output $\overline{O}_2$ is "L". If a motor is connected between the output pins of $\overline{O}_1$ and $\overline{O}_2$, the output power supply is current source and the $\overline{O}_2$ is current sink and the motor is driven. If the reverse signals are input to the I_1, I_2, the $\overline{O}_1$ becomes "L" and the $\overline{O}_2$ becomes "H", then the motor is driven backward. But, if the I_1 and the I_2 are both "H", and the $\overline{O}_1$ and the $\overline{O}_2$ are "L", then the motor is quickly halted. (Braking mode input)

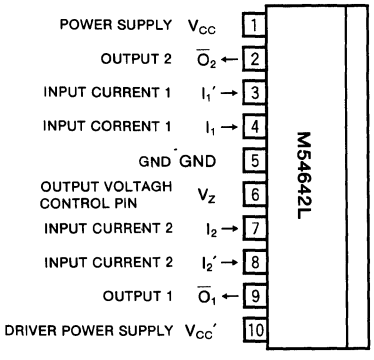
The interrupt input I_1' and I_2' are "L" active inputs and, when the I_1 is "H" and I_2 is "L", the motor is driven, but, if the I_2' is "L", then the outputs $\overline{O}_1$ and the $\overline{O}_2$ are both "L" and becomes brake mode.

The speed of motor becomes constant if a zener diode of a certain voltage is added to the Vz pin, because the output "H" voltage never exceeds this zener voltage. If the Vz pin is connected to the driver power supply V_{CC}', the speed of motor can be changed by changing the V_{CC}'.

The peak output current is $I_{OP(max)}$ = 800mA, and continuous output current is $I_{O(max)}$=150mA.

Threshold temperature of the internal thermal shutdown protector is min 100℃, and the drive current must be set so that the thermal shutdown protector will not operate.

PIN CONFIGURATION (TOP VIEW)



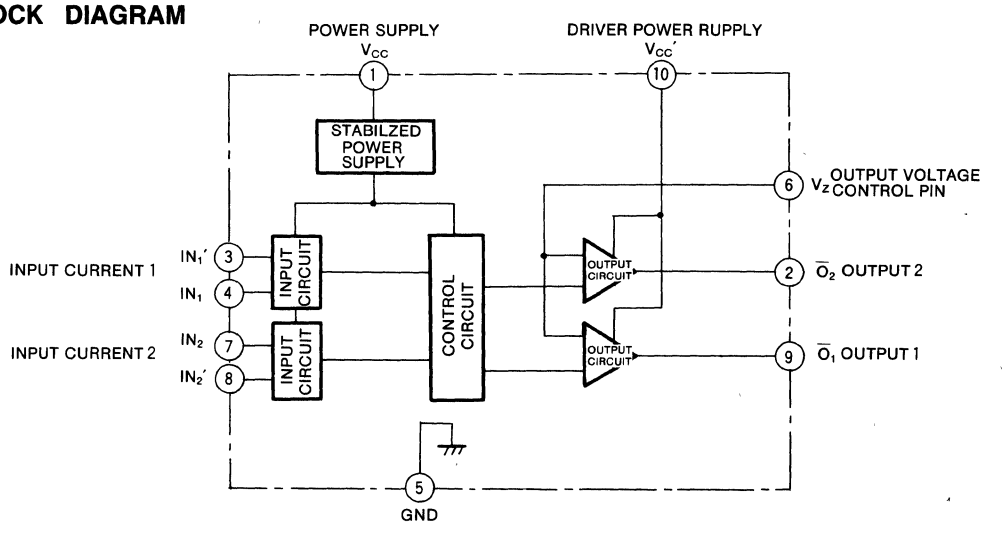
Outline 10P5

LOGIC TRUTH TABLE

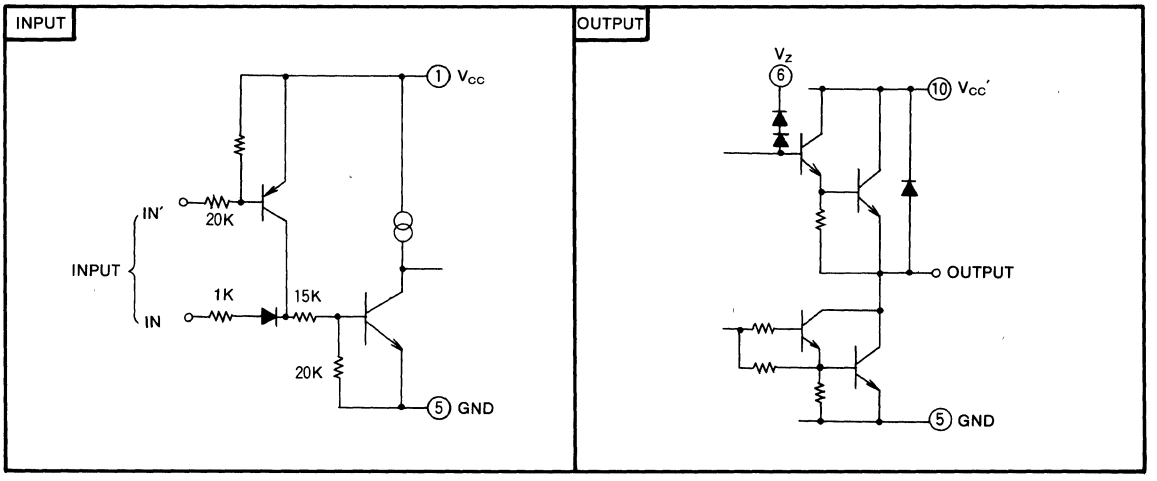
Input				Output		Note
I_1	I_1'	I_2	I_2'	O_1	O_2	
L	H	L	H	"OFF" state	"OFF" state	Open
L	L	L	H	H	L	Clockwise
L	H	L	L	L	H	Anti-clockwise
L	L	L	L	L	L	Braking
H	H	L	H	H	L	Clockwise
H	L	L	H	H	L	Clockwise
H	H	L	L	L	L	Braking
L	H	H	H	L	H	Ahti-clockwise
L	H	H	L	L	H	Anti-clockwise
L	L	H	H	L	L	Braking
H	*	H	*	L	L	Braking

* : Irrelevant

BLOCK DIAGRAM



INPUT/OUTPUT CIRCUIT



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RAINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+12	V
$V_{CC'}$	Driver power supply		−0.5～+20	V
V_I	Input voltage		0～V_{CC}	V
V_O	Output voltage		−0.5～$V_{CC'}$+2.5	V
$I_{O(max)}$	Peak output current	top=10ms top=10ms : repetitive cycle 0.2Hz max	±800	mA
I_O	Continuous output current		±150	mA
Pd	Power dissipation	T_a=60℃	570	mW
Tj	Junction temperature		100	℃
Topr	Operating temperature		−10～+60	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	10	V
I_O	Output current				±100	mA
V_{IH}	High-level input voltage	I_1, I_2 input pins	3.0		V_{CC}	V
$V_{I'H}$	High-level input voltage	I_1, I_2 input pins	V_{CC}−0.5		$V_{CC'}$	V
V_{IL}	Low-level input voltage	I_1, I_2 input pins	0		0.6	V
$V_{I'L}$	Low-level input voltage	I_1, I_2 input pins	0		V_{CC}−3.6	V
t_S	Motor braking interval		10	100		ms
T_S	Thermal shutdown protector operating temperature (Junction temperature)		100	120		℃

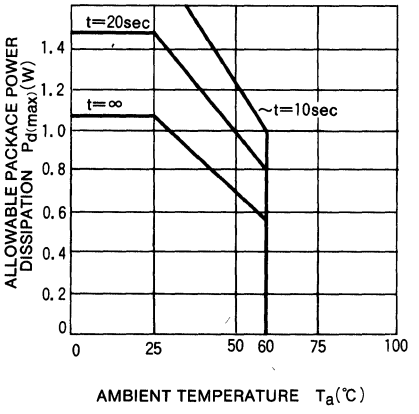
ELECTRICAL CHARACTERISTICS (T_a=25℃, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Output lekage current	$V_{CC'}$=20V, Vz open	V_O=20V			100	μA
			V_O=0V			−100	
V_{OH}	High-level output voltage	V_{CC}=12V, Vz · open	I_{OH}=−50mA	10.2	10.5		V
			I_{OH}=−100mA	10.0	10.4		
V_{OL}	Low-level output voltage	$V_{CC'}$=12V, Vz . open	I_{OL}=50mA		0.1	0.3	V
			I_{OL}=100mA		0.2	0.4	
V_{O1-O2}	Voltage between output(1) and output(2) (voltage between motors)	$V_{CC'}$=12V, Vz=7V	I_O=±100mA	6.3	7.0	7.7	V
I_I	Input current	$V_{CC'}$=12V, V_1=3V, V_1'=4.5V	Output open		100	180	μA
		$V_{CC'}$=12V, V_1=5V, V_1'=4.5V			240	380	
I_I'	Input current	$V_{CC'}$=12V, V_1=0.4V, V_1'=4.5V	Output open		−200	−250	μA
		$V_{CC'}$=12V, V_1'=1.4V, V_1=0.6V			−145	−190	
I_{CC}	Supply current	V_{CC}=10V	"OFF" state		1.2	3.0	mA
		$V_{CC'}$=12V	Clockwise or anti-clockwise		4.5	8.0	
			Braking		7.5	12.0	

* : Typical values are at T_a=25℃

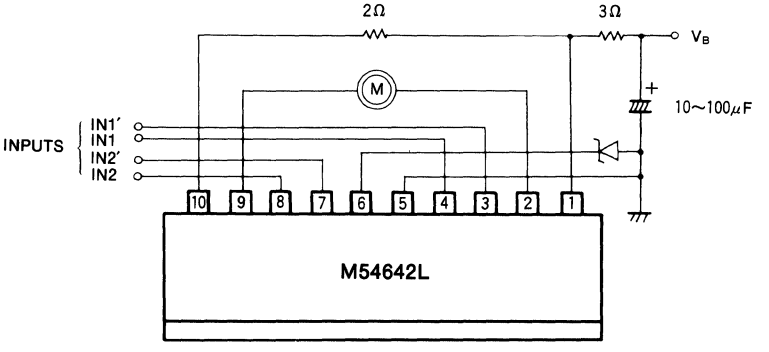
TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



Note 1 : Mounted on an epoxy PC board with Cu cover on one side (5cm×5cm×0.8mmt)
2 : t : time for power application

APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M54643L

BI-DIRECTIONAL MOTER DRIVER

DESCRIPTION

The M54643L is a semiconductor integrated circuit capable of directly driving small bidirectional motors.

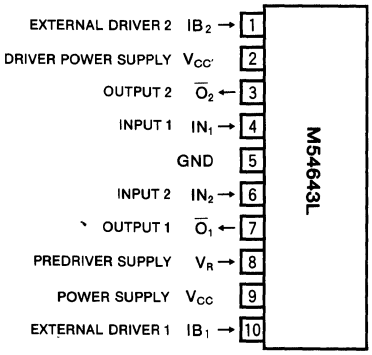
FEATURES

- Wide operating voltage range (V_{CC}= 4 ~16V)
- Low output saturation voltage (high voltage across motors)
- Built-in clamp diode
- Large drive current ($I_{O(max)}$=±1.2A)
- Brake function provided
- Internal thermal shutdown circuit

APPLICATION

Audio equipment such as tape decks and radio cassette recorders; VCRs and other consumer products.

PIN CONFIGURATION (TOP VIEW)



Outline 10P5

FUNCTION

The M54643L can directly drive small bidirectional motors. When inputs 1 and 2 are both low, outputs 1 and 2 are both OFF. When input 1 is high and input 2 is low, output 1 is high and output 2 is low (forward). When input 1 is low and input 2 is high, output 1 is low and output 2 is high (reverse). When inputs 1 and 2 are both high, outputs 1 and 2 are both low (braking).

Separate power supplies for the logic (V_{CC}), predriver (Vr) and output (V_{CC}') provide greater freedom of equipment design. When Vr is connected to V_{CC} or to V_{CC}', the device operates identically as the M54545L.

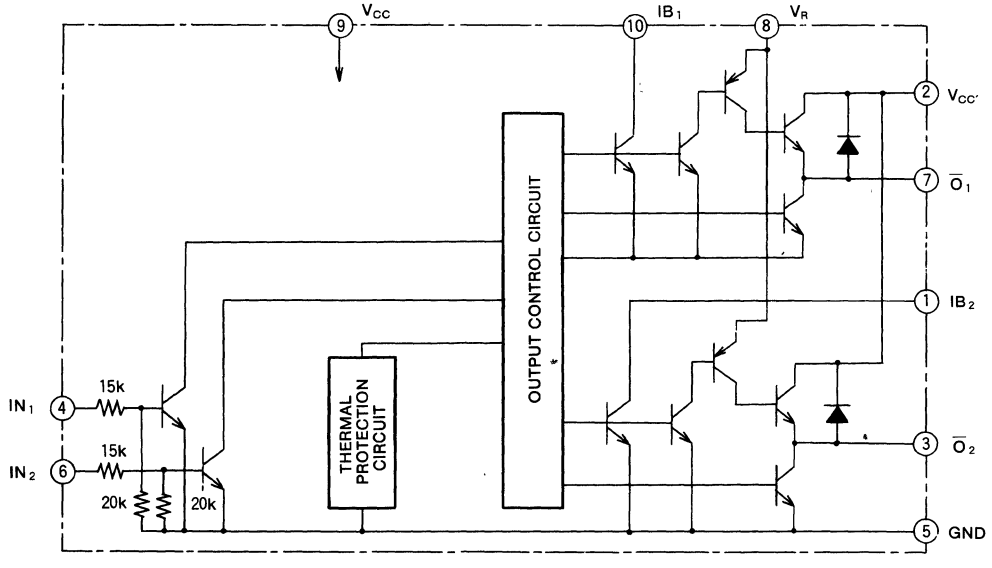
An internal thermal shutdown circuit protects the IC from thermal destruction in the event of motor blockage or other abnormalities.

Pins IB_1 and IB_2 are connected to the base of external PNP transistors to lower the power consumption.

TRUTH TABLE

Inputs		Outputs				Motor state
IN_1	IN_2	O_1	O_2	IB_1	IB_2	
L	L	OFF	OFF	OFF	OFF	Open
H	L	H	L	L	H	Forward
L	H	L	H	H	L	Reverse
H	H	L	L	OFF	OFF	Brake

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RAINGS (T_a=25℃, unless otherwised noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+16	V
$V_{CC'}$	Driver supply voltage		−0.5～+24	V
V_R	Predriver supply voltage		−0.5～+24	V
V_I	Input voltage	$V_I \leqq V_{CC}$	0～7	V
V_O	Output voltage		−0.5～$V_{CC'}$+2.5	V
$I_{O(max2)}$	Peak output current	top≦100ms Repetitive cycle 0.2Hz max	±800	mA
$I_{O(max)}$	Peak output current (single pulse)	top≦100ms	±1.20	A
I_O	Continuous output current		±250	mA
P_d	Power dissipation	T_a=75℃	700	mW
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～+75℃, unless otherwise noted)

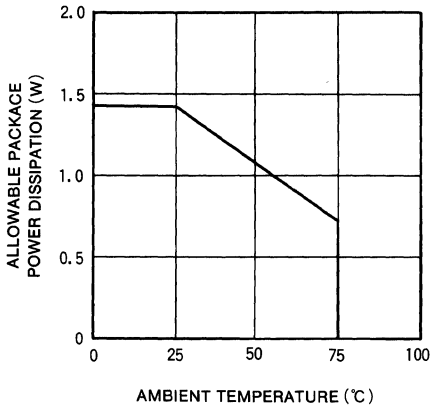
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4	5	16	V
I_O	Output current			±200	mA
V_{IH}	High-level input voltage	2.0		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.4	V
t_B	Motor braking interval	10	100		ms
t_{shut}	Thermal shutdown temperature (chip temperature)	125	150		℃
T_C	Simultaneous switching input inhibit time (forward↔reverse)	10			μs

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃ unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$I_{O(leak)}$	Output lekage current	V_{CC}=16V, $V_{CC'}$=V_R=24V V_{I1}=V_{I2}=0.4V V_O= 0 V or 24V				±100	μA
V_{OH}	High-level output voltage	V_{CC}= 5 V, $V_{CC'}$=V_R=16V, I_O=−200mA (V_{I1}=0.4V, V_{I2}=2.0V) or (V_{I1}=2.0V, V_{I2}=0.4V)		14.5	15.2		V
V_{OL}	Low-level output voltage	V_{CC}=5V, $V_{CC'}$=V_R=16V (V_{I1}=0.4V, V_{I2}=2.0V or	I_O=100mA		0.1	0.35	V
		(V_{I1}=2.0V, V_{I2}=0.4V	I_O=200mA		0.18	0.4	
I_I	Input current	V_{CC}=5V, $V_{CC'}$=V_R=16V, V_I=2.0V		50	90	120	μA
I_{CC}	Supply current	V_{CC}=16V, $V_{CC'}$=V_R=16V V_I=V_{I2}=0.4V			2.6	5	mA
		V_{CC}=16V, $V_{CC'}$=V_R=16V (V_{I1}=0.4V, V_{I2}=2.0V) or (V_{I1}=2.0V, V_{I2}=0.4V)			8	15	
		V_{CC}=16V, V_{I1}=V_{I2}=2.0V $V_{CC'}$=V_R=16V			14	25	
I_B	I_B output current	V_{CC}= 5 V, $V_{CC'}$=V_R=V_{IB}=16V (V_{I1}=0.4V, V_{I2}=2.0V) or (V_{I1}=2.0V, V_{I2}=0.4V)		1.0	5.0	15.0	mA

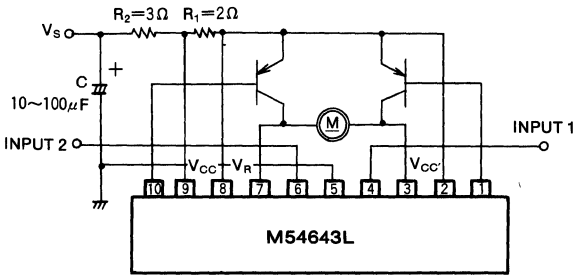
TYPICAL CHARACTERISTICS

THERMAL DERATING CHARACTERISTICS

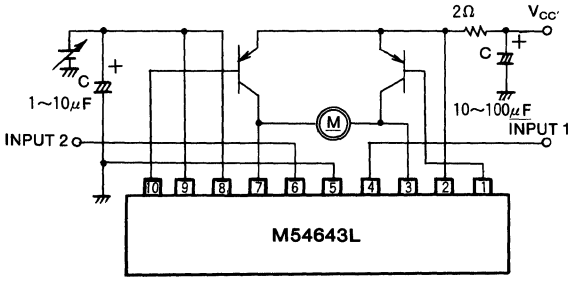


TYPICAL APPLICATION

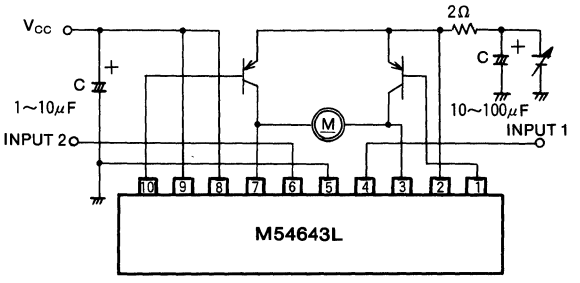
1)



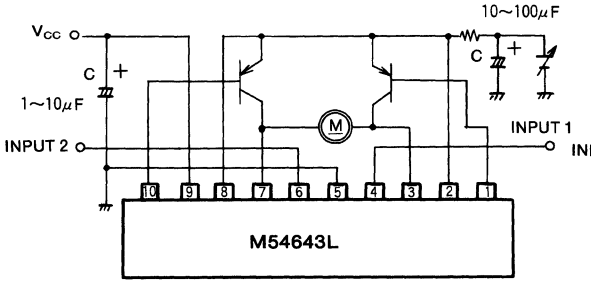
2) Motor speed control by the V_R and V_{CC}



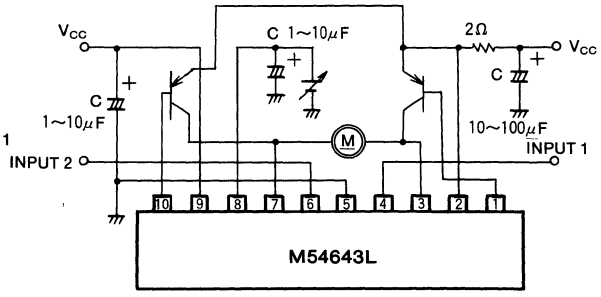
3) Motor speed control by the V_{CC}'



4) Motor speed control by the V_R and V_{CC}'



5) Motor speed control by the V_R



M54644BL

BI-DIRECTIONAL MOTOR DRIVER

DESCRIPTION

The M54644L/AL is a semiconductor integrated circuit capable of directly driving small bidirectional motors.

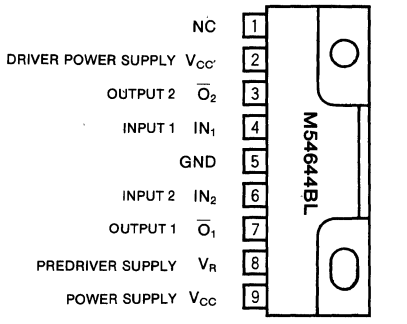
FEATURES

- Wide operating voltage range (V_{CC}= 4 ~16V)
- Low output saturation voltage (high voltage across motors)
- Built-in clamp diode
- Large drive current ($I_{O(max)}$=±2A)
- Brake function provided
- Internal thermal shutdown circuit
- Internal overcurrent protection circuit

APPLICATION

Audio equipment such as tape decks and radio cassette recorders; VCRs and other consumer products.

PIN CONFIGURATION (TOP VIEW)



Outline 9P9

NC : No connection

FUNCTION

The M54644L/AL can directly drive small bidirectional motors. When inputs 1 and 2 are both low, outputs 1 and 2 are both OFF. When input 1 is high and input 2 is low, output 1 is high and output 2 is low (forward). When input 1 is low and input 2 is high, output 1 is low and output 2 is high (reverse). When inputs 1 and 2 are both low (braking).

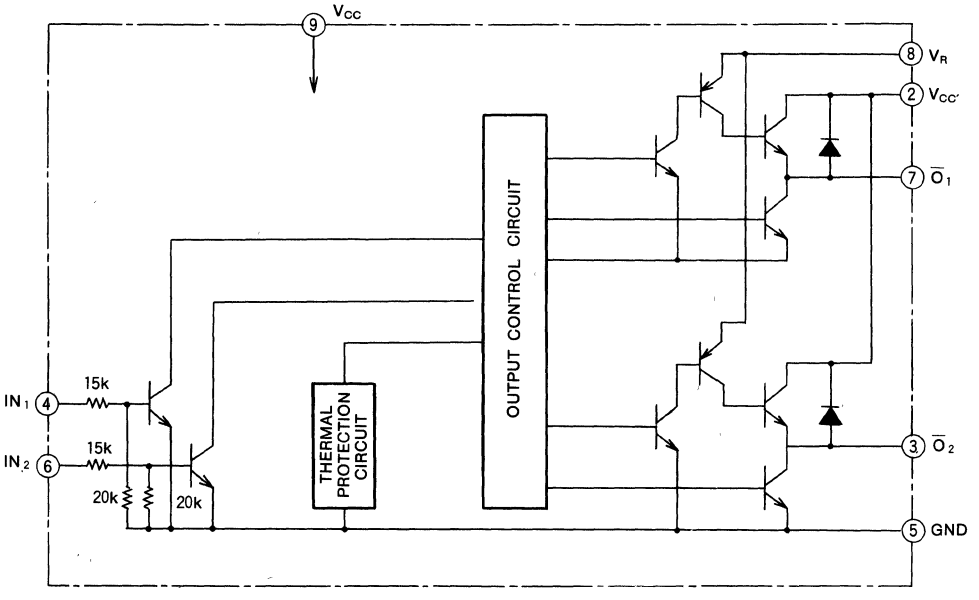
Separate power supplies for the logic (V_{CC}), predriver (Vr) and output ($V_{CC'}$) provide greater freedom of equipment design. When Vr is connected to V_{CC} or to $V_{CC'}$, the device operates identically as the M54545L.

An internal thermal shutdown circuit protects the IC from thermal destruction in the event of motor blockage or other abnormalities.

TRUTH TABLE

Inputs		Outputs		Motor state
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	OFF	OFF	Open
H	L	H	L	Forward
L	H	L	H	Reverse
H	H	L	L	Brake

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RAINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5～+16	V
$V_{CC'}$	Output supply voltage	Heat sink (30cm²×1.5mm)	−0.5～+24	V
V_R	Control voltage		−0.5～+24	V
V_I	Input voltage	$V_I \leqq V_{CC}$	0～7	V
V_O	Output voltage		−0.5～$V_{CC'}$+2.5	V
$I_{O(max)}$	Peak output current	top≦100ms Repetitive cycle 5 sec max	±2	A
I_O	Continuous output current	Heat sink (30cm²×1.5mm)	±600	mA
Pd	Power dissipation		154	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−20～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～+75℃, unless otherwise noted)

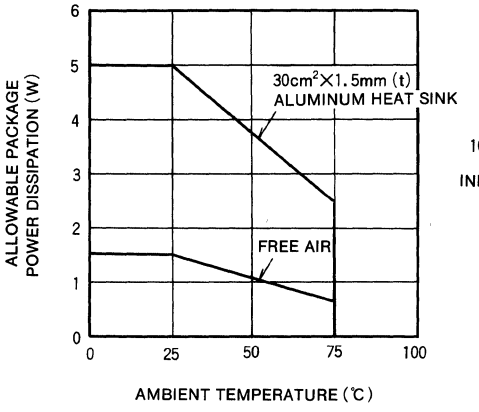
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4	5	16	V
I_O	Output current heat sink (30cm²×1.5mm)			±500	mA
V_{IH}	High-level input voltage	2.0		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.4	V
t_B	Motor braking interval	10	100		ms
t_{shut}	Thermal shutdown temperature	125	150		℃

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃ unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$I_{O(leak)}$	Output lekage current	V_{CC}=16V, $V_{CC'}$=V_R=24V V_{I1}=V_{I2}=0.4V V_O=0V or 24V				±100	μA
V_{OH}	High-level output voltage	V_{CC}=$V_{CC'}$=V_R=16V, I_O=−500mA (V_{I1}=0.4V, V_{I2}=2.0V) or (V_{I1}=2.0V, V_{I2}=0.4V)		14.5	15.2		V
V_{OL}	Low-level output voltage	V_{CC}=$V_{CC'}$=V_R=16V (V_{I1}=0.4V, V_{I2}=2.0V) or	I_O=200mA		0.1	0.4	V
		(V_{I1}=2.0V, V_{I2}=0.4V)	I_O=500mA		0.18	1.4	
I_I	Input current	V_{CC}=$V_{CC'}$=V_R=16V, V_I=2.0V		50	90	120	μA
I_{CC}	Supply current	V_{CC}=16V, $V_{CC'}$=V_R=16V V_I=V_{I2}=0V			2.6	5	mA
		V_{CC}=16V, $V_{CC'}$=V_R=16V (V_{I1}=0.4V, V_{I2}=2.0V) or (V_{I1}=2.0V, V_{I2}=0.4V)			8	15	
		V_{CC}=16V, V_{I1}=V_{I2}=2.0V $V_{CC'}$=V_R=16V			14	25	
I_R	Control pin input current	V_{CC}=16V, $V_{CC'}$=V_R=16V (V_{I1}=0.4V, V_{I2}=2.0V)			0.1	1.0	mA

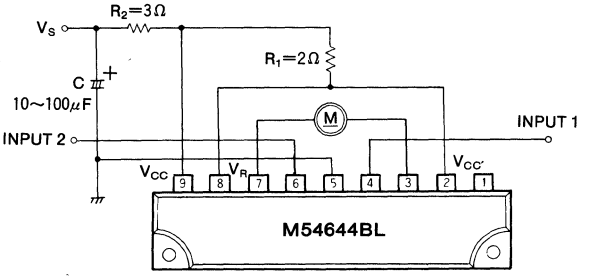
TYPICAL CHARACTERISTICS

THERMAL DERATING CHARACTERISTICS

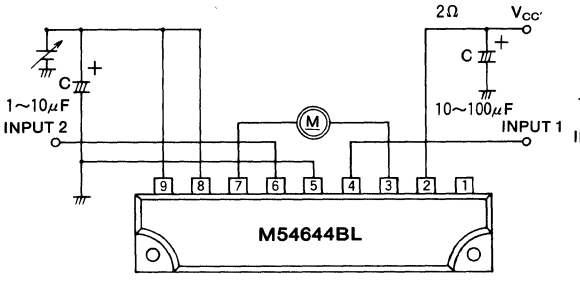


TYPICAL APPLICATION

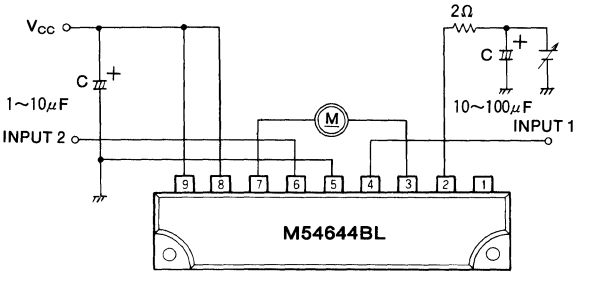
1)



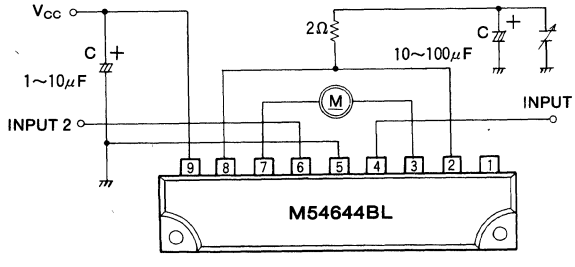
2) Motor speed control by the V_R and V_{CC}



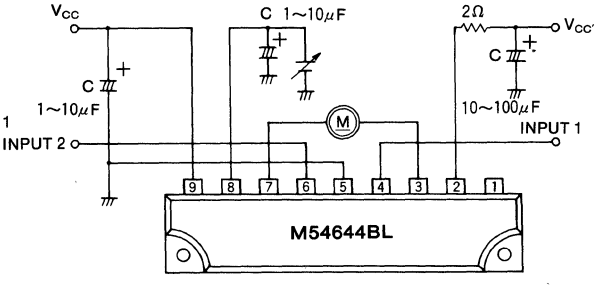
3) Motor speed control by the V_{CC}'



4) Motor speed control by the V_R and V_{CC}'



5) Motor speed control by the V_R



MITSUBISHI ELECTRIC

M54645AL

BI-DIRECTIONAL MOTOR DRIVER

DESCRIPTION

The M54645AL is a semiconductor integrated circuit, capable of directly driving small bidirectional motors.

FEATURES

- Wide operating voltage range (V_{CC}= 4 ~18V)
- Can be driven by the outputs of NMOS and CMOS ICs
- Large drive current ($Io_{(max)}$=±3.0A)
- Internal switching regulator
- Built-in clamp diode
- Brake function provided
- Internal thermal shutdown circuit

APPLICATION

Audio equipment such as tape decks and radio cassette recorders; VCRs and other consumer products.

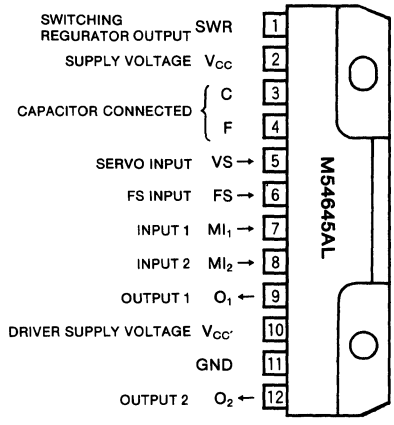
FUNCTION

The M54645AL can directly drive small bidirectional motors. Forward, backward, braking and OFF states are selected by two inputs. The output voltage (either Vs and FS) is selected by the FS input.

The output circuit consists of NPN Darlington transistors for both current source and sink, and can supply output currents of ± 3 A max.

An internal thermal shutdown circuit protects the IC from thermal destruction in the event of motor blockage or other abnormalities by setting both outputs in the open (off) mode.

PIN CONFIGURATION (TOP VIEW)



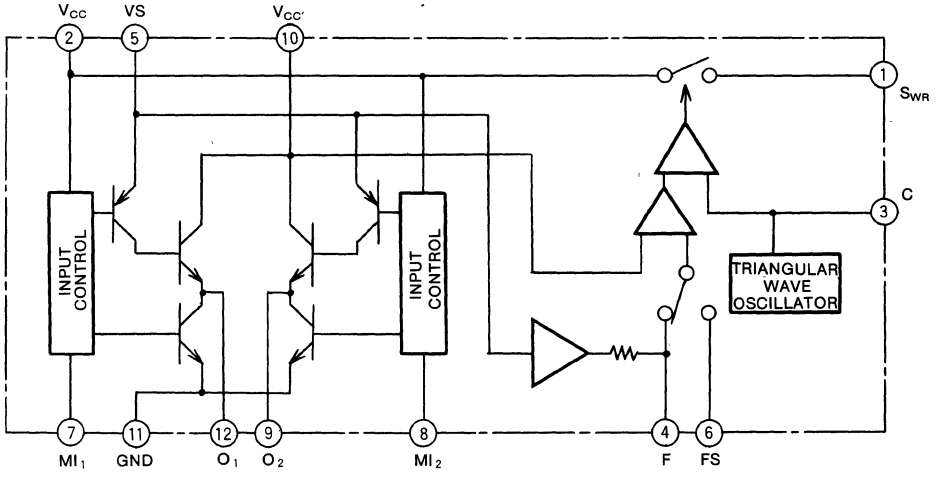
Outline 12P9B

TRUTH TABLE

Inputs		Outputs		Motor state
IN_1	IN_2	$\overline{O}_1$	$\overline{O}_2$	
L	L	OFF	OFF	Open
H	L	H	L	Forward
L	H	L	H	Reverse
H	H	L	L	Brake

FS input	$V_{CC'}$ voltage
L	VS
H	FS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

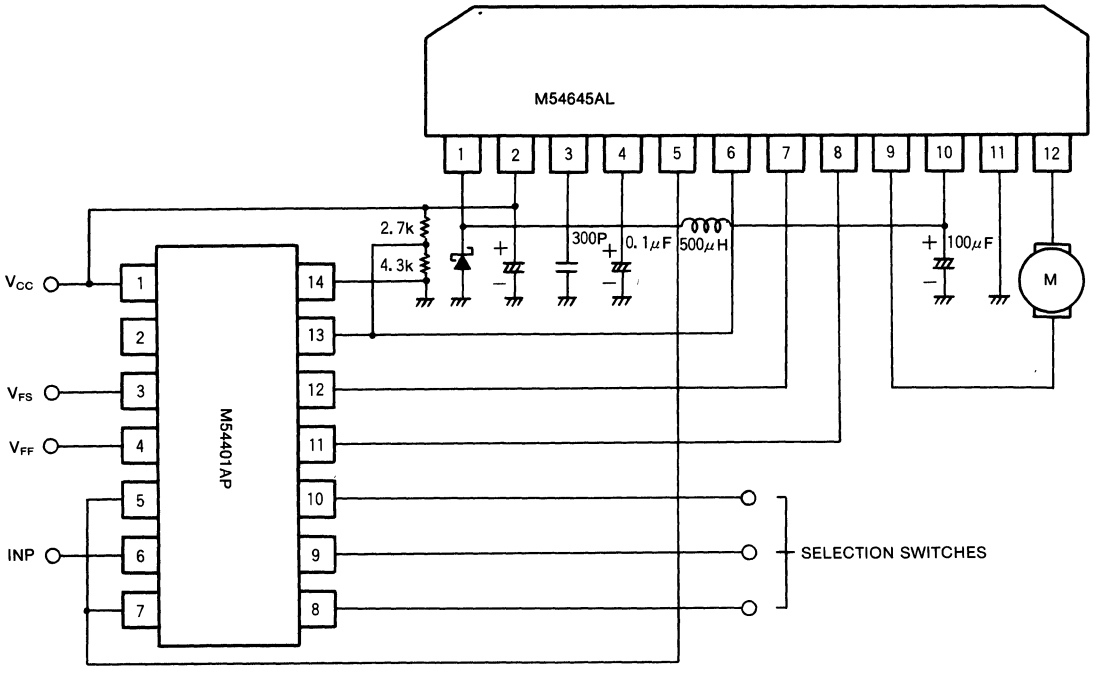
Symbol	Parameter	Note	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+28	V
V_I	Input voltage	$V_I \leqq V_{CC}$	−0.5～+28	V
I_{OP}	Peak output current	$t_{OP} \leqq$ 30msec, repetitive cycle time $\geqq$ 6.0Hz	±3.0	A
I_O	Continuous output current		±600	mA
I_{OSWR}	Switching regulator output current	$t_{OP} \leqq$ 30msec, repetitive cycle time $\geqq$ 6.0Hz	0～3.0	A
P_d	Power dissipation	T_a=75℃	1.2	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, V_{CC}=18V, unless otherwise noted)

Symbol	Parameter	Test conditions	Test pin	Limits			Unit
				Min	Typ	Max	
I_{CC}	Supply current	Output OFF mode	2	3.5	5.5	9.0	mA
$I_{SWR(leak)}$	Switching regulator output leakage current	V_I=0V, output OFF mode V_{CC}=22V	1		0	−100	μA
$V_{SWR(sat)}$	Switching regulator output saturation voltage	I_{SWR}=−0.1A	1		1.4	2.0	V
		I_{SWR}=−1.0A	1		1.9	2.8	V
		I_{SWR}=−2.5A (Note 1)	1		2.5	3.7	V
V_{TR} H	Triangular wave threshold voltage	Pin C : 300pF	3	4.3	5.1	5.3	V
V_{TR} L	Triangular wave threshold voltage	Pin C : 300pF	3	1.5	1.8	2.1	V
f_{TR}	Triangular wave oscillation frequency	Pin C : 300pF	3	31	52	75	kHz
V_{4LIM}	Pin 4 limit	V_5=0V V_6=0V	4	1.1	1.6	2.1	V
V_4	Pin 4 voltage	30kΩ between pin 4 and GND V_5=V_6=0V	4	0.6	1.1	1.3	V
ΔV_{5-4}	Offset voltage between pins 4 and 5	V_5=10V V_6=0V	4,5	−0.15	−0.04	+0.15	V
ΔV_{6-4}	Offset voltage between pins 4 and 6	V_6=8V	4,6	−0.2	0.05	+0.2	V
V_{TH6}	FS input threshold	V_5=3V Voltage when V4 change	6	0.7	1.3	1.8	V
V_{TH7}	MI1 threshold voltage		7	0.6	1.2	1.8	V
V_{TH8}	MI2 threshold voltage		8	0.6	1.2	1.8	V
I_{oleak}	Output leakage current		9,12		0	±100	μA
$V_{OH(sat)}$	High-level output saturation voltage	I_{OH}=−0.1A	9,12		1.4	2.0	V
		I_{OH}=−1.0A	9,12		1.9	2.8	V
		I_{OH}=−2.5A (Note 1)	9,12		2.5	3.7	V
$V_{OL(sat)}$	Low-level output saturation voltage	I_{OL}=0.1A	9,12		0.78	1.05	V
		I_{OL}=1.0A	9,12		1.1	1.7	V
		I_{OL}=2.5A (Note 1)	9,12		1.4	1.9	V
BV_{CER}	Output transistor withstand voltage	I_O=20mA	9,12	28	45		V
ΔV_{4-10}	Offset voltage between pins 4 and 10		10	0	0.1	0.2	V
ΔV_{6-10}	Offset voltage between pins 6 and 10		10	0	0.1	0.2	V
V_{10} ON	Activating voltage at pin 10	V_5=V_6=0V Voltage when V1 changes	10	0.50	0.78	1.10	V
V_{10} OFF	Shutdown voltage at pin 10	V_5=V_6=0V Voltage when V1 changes	10	0.50	0.78	1.10	V
T_S	Thermal shutdown temperature	Temperature at the center of the heat sink		140	165	190	℃

Note 1 : The measurement must be conducted within 30msec.

APPLICATION EXAMPLE



Note. • A fast-recovery or Schottky diode must be used in the filter circuit
• The lead lengths of the capacitor between the M54645AL V_{CC} pin and GND must be as short as possible.
• GND line must be as thick as possible

PRECAUTIONS FOR USE

1. Allowable power dissipation

The allowable power dissipation of the IC (P_d) is calculated by the following formula.

$P_d \fallingdotseq V_{CC} \times I_{CC} + I_O (V_{CC} - V_{OH}) + V_{OL} + V_{SWR(sat)}$

This value must not exceed the maximum allowable power dissipation shown in the thermal derating characteristics.

Please note that if repetive peak currents are applied, the allowable power dissipation is less.

2. Thermal shutdown

A thermal shutdown circuit is built in to protect the device against thermal destruction when excessive currents are applied. This function shuts down the output stage of the switching regulator when the temperature at the back of the IC reaches 165℃ (140℃ min).

3. Triangular wave oscillator

The relationship between the externally connected capacitance C and the frequency is given by the following formula.

$$1/f \fallingdotseq \frac{3.2 \times C}{100 \times 10^{-6}} \times 2 \text{ (Hz)}$$

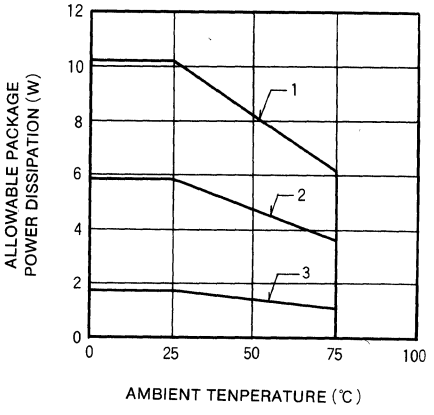
Capacitor should be located close to the IC with lead lengths as short as possible, as it can be easily affected by the switching regulator.

4. Switching regulator

A fast-recovery or Schottky diode should be used in the filter circuit of the switching regulator. If a conventional diode is used, excessively large switching currents may flow.

TYPICAL CHARACTERISTICS

THERMAL DERATING
CHARACTERISTICS



1) INFINITE HEAT SINK
2) 25cm^2×1.5mm (t) ALUMINUM HEAT SINK
3) FREE AIR

M54646P

STEPPER MOTOR DRIVER

DESCRIPTION

The M54646P is a semiconductor integrated circuit capable of controlling and driving the winding current of bipolar stepper motors, and controlling the winding current.

FEATURES

- Wide operating voltage range
- Extremely wide current control range
- Designed to compensate for the effects of unstable motor supply voltages
- Internal diodes protect the motor driver transistors in the output stage

APPLICATION

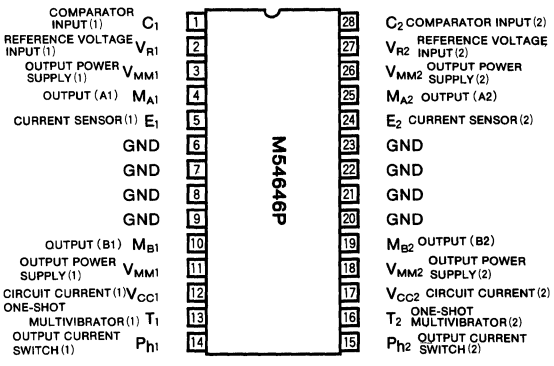
Stepper motor drivers

FUNCTION

The M54646P can drive bipolar stepper motors and control the winding current. By controlling the reference voltage (V_R), it is also possible to vary the output current continuously. PHASE INPUT controls the direction of output current flow.

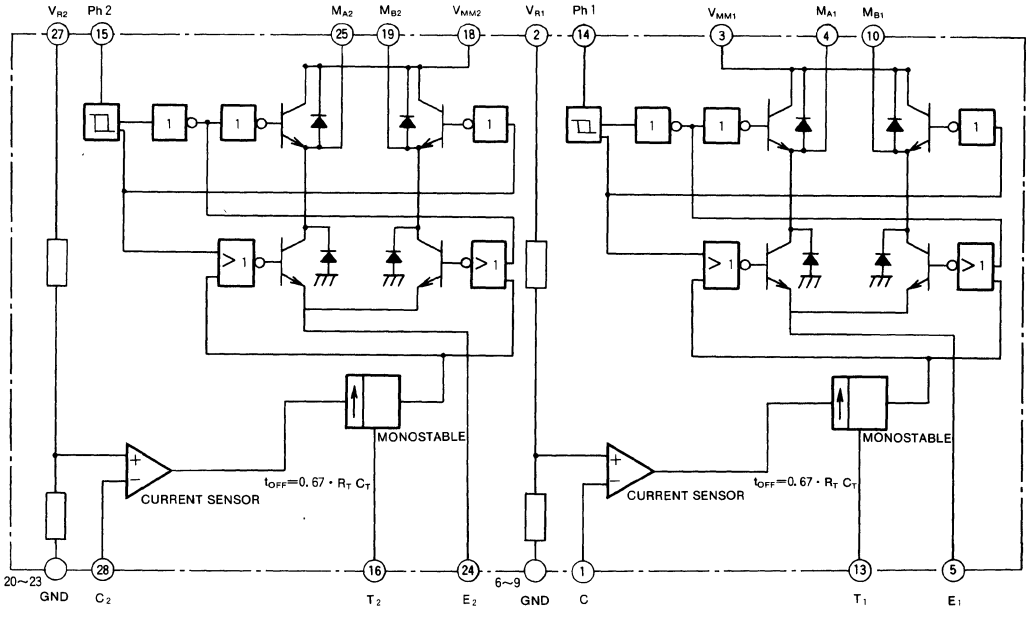
This IC contains two circuits enabling control of a four-phase stepper motor by a single chip instead of the two devices previously required.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4B

BLOCK DIAGRAM



PIN DESCRIPTION

Pin number	Symbol	Description
1	C_1	Comparator input (1)
2	V_{R1}	Reference voltage input (1)
3	V_{MM1}	Output power supply (1)
4	M_{A1}	Output pin (1)
5	E_1	Current sensor (1)
6	GND	GND
7	GND	GND
8	GND	GND
9	GND	GND
10	M_{B1}	Output pin (1)
11	V_{MM1}	Output power supply (1)
12	V_{CC1}	Circuit current (1)
13	T_1	Time constant of one-shot multivibrator
14	P_{h1}	Output current direction switching
15	P_{h2}	Output current direction switching
16	T_2	Time constant of one-shot multivibrator
17	V_{CC2}	Circuit current (2)
18	V_{MM2}	Output power supply (2)
19	M_{B2}	Output pin (2)
20	GND	GND
21	GND	GND
22	GND	GND
23	GND	GND
24	E_2	Current sensor (2)
25	M_{A2}	Output pin (2)
26	V_{MM2}	Output power supply (2)
27	V_{R2}	Reference voltage input (2)
28	C_2	Comparator input (2)

DESCRIPTION OF OPERATION

PHASE INPUT

The phase input determines the output mode as shown.

PHASE	M_A	M_B
H	H	L
L	L	H

V_R (reference voltage)

The current level can be changed continuously by varying the voltage V_R

Current sensor

The voltage drop across the current detector resistance is compared with selected current level, and when they match, the comparator triggers a monostable pulse. The output stage is cut off for an interval t_{OFF}. During this time, the output current drops to below the comparator level. After t_{OFF} elapses, the output stage turns on again, and this process repeats.

Single pulse generator

A monostable pulse is triggered by the rising edge of the comparator output. The pulse width is determined by external timing constants R_t and C_t.

$t_{OFF}=0.69 \times R_t C_t$

Trigger pulses applied during t_{OFF} are ignored.

Analog control

The output current level can be changed continuously by varying V_R or the feedback voltage applied to the comparator.

ABSOLUTE MAXIMUM RAINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3~7	V
V_{MM}	Output supply voltage		−0.3~45	V
V_L	Logic input voltage		−0.3~6	V
V_C	Analog input voltage		−0.3~V_{CC}	V
V_R	Reference voltage		−0.3~15	V
I_L	Logic input current		−10	mA
I_C	Analog input current		−10	mA
I_{MM}	Output supply current		±600	mA
P_d	Power dissipation		1.92	W
Topr	Operating temperature		−20~+75	℃
Tstg	Storage temperature		−55~+125	℃

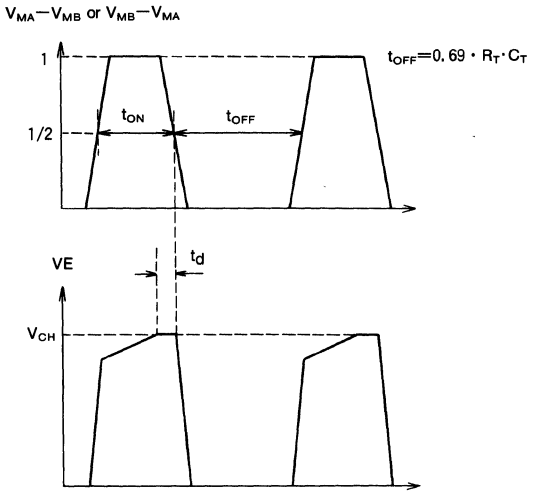
RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{MM}	Output supply voltage		10		40	V
I_O	Output current		20		500	mA
tPLH	Logic input rise time				2	μs
tPHL	Logic input fall time				2	μs
T_{ON}	Thermal shutdown temperature			150		℃
V_{IH}	Logic input voltage	"H"	2.0		V_{CC}	V
V_{IL}		"L"	0		0.8	V

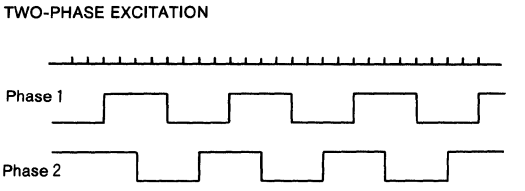
ELECTRICAL CHARACTERISTICS (T_a=25℃ unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{CH}	Comparator threshold voltage		V_R=5V	400	430	450	mV
I_{CO}	Comparator input current			−20		20	μA
I_{OFF}	Output cutoff current					100	μA
Vsat	Saturation voltage		Sensing resistance is not included. I_O=500mA			3.5	V
tOFF	Cutoff time		V_{MM}=10V, t_{ON}≧5μs	25	30	35	μs
t_d	Turn-off delay		dVK/dt≧50mV/μs		1.6	2.0	μs
I_{CC}	Supply current		V_{CC}=5V, one phase			25	mA
P_{top}	Power dissipation		Im=500mA t_s=30kHz		1.8	2.3	W
I_{IH}	Logic input current	"H"	V_i=2.4V			20	μA
I_{IL}		"L"	V_i=0.4V	−0.4			mA

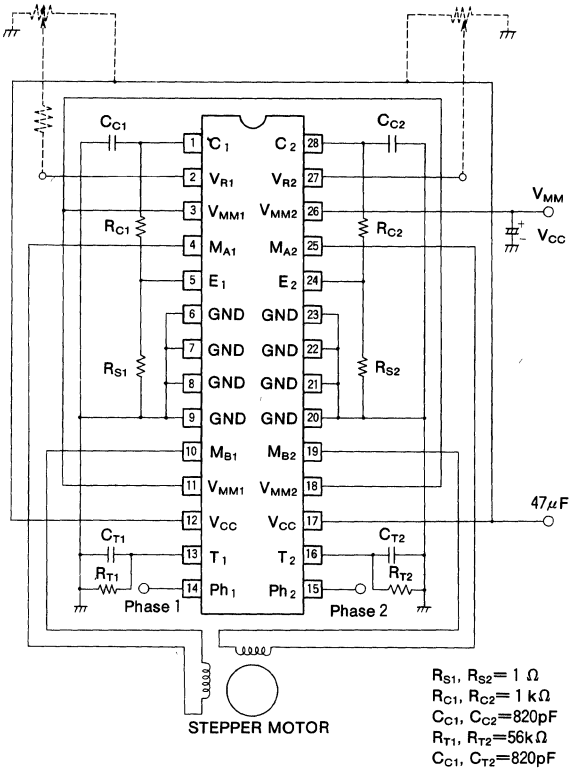
SWITCHING CHARACTERISTICS



TIMING CHART



APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M54648AL

BI-DIRECTIONAL MOTOR DRIVER WITH MOTOR SPEED CONTROL

DESCRIPTION

The M54648AL is a semiconductor integrated circuit, capable of directly driving bi-directional micro motor, with a built in speed control circuit.

FEATURES

- Wide operating voltage range (V_{CC}=4~18V)
- N MOS, C MOS IC output for direct drive
- Large output sink current ($I_{O(max)}$=±3.0A)
- Built-in operational amplifier for "H" output voltage control
- Built-in clamp diode
- Braking mode input
- Compact power package requiring small space

APPLICATION

Audio tape deck player, radio cassette player, VTR, Home-use equipment

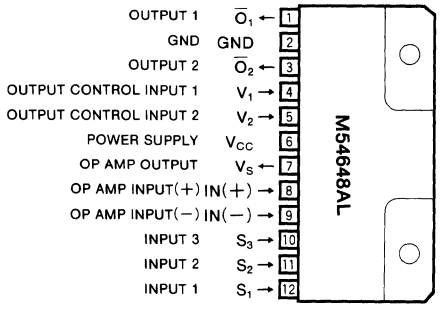
FUNCTION

The M54648AL, full bridge motor driver, has the logic circuitry and the quasi-darlington power driver for driver for bidirectional control of D-C motors operating at current up to 3.0A.

The inputs, S_1, S_2 and S_3, are capable to control the bridge output polarity and also to select the supply Voltage of the predriver from the voltages drived by V_1, V_2 or the output of the operatinal amplifier.

The internal thermal shutdown protector protects the IC from thermal destruction due to blocking of motor, etc.

PIN CONFIGURATION (TOP VIEW)

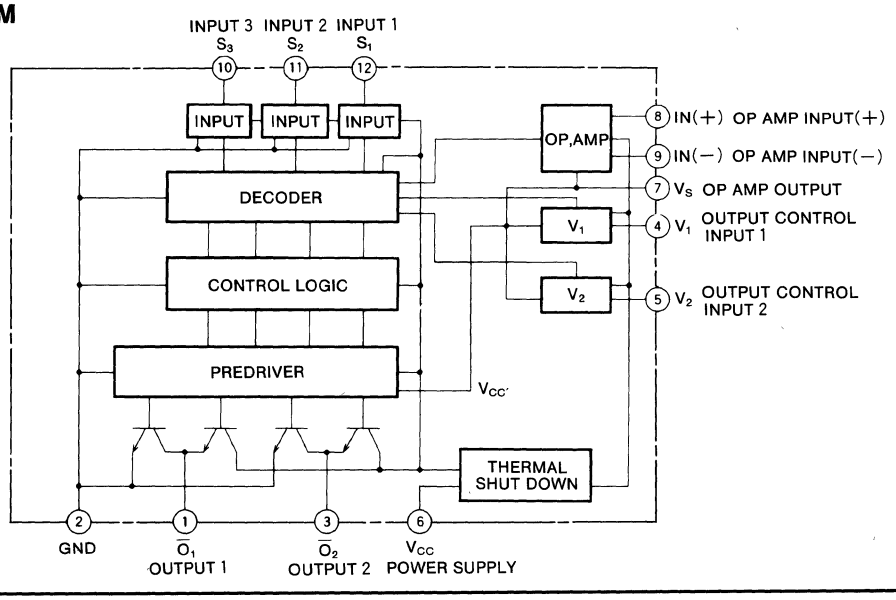


Outline 12P9B

LOGIC TRUTH TABLE

Input			Output		Driver power supply (V_{CC})	Note
S_1	S_2	S_3	$\overline{O}_1$	$\overline{O}_2$		
L	L	L	"OFF" state	"OFF" state	—	STOP
L	L	H	H	L	OP AMP OUTPUT	PLAY(+)
L	H	L	L	H	OP AMP OUTPUT	PLAY(−)
L	H	H	H	L	V_2	FF(2)
H	L	L	L	H	V_2	REW(2)
H	L	H	H	L	V_1	FF(1)
H	H	L	L	H	V_1	REW(1)
H	H	H	L	L	V_S	BRAKE

BLOCK DIAGRAM



BI-DIRECTIONAL MOTOR DRIVER WITH MOTOR SPEED CONTROL

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With an external heat sink (3000mm²×1.5mmt)	−0.5～+20	V
V_I	Input voltage	4Pin, 5Pin	−0.5～+14 or V_{CC}	V
		Inputs pin other than the above	−0.5～V_{CC}	
V_O	Output voltage		−2.0～V_{CC}+2.5	V
$I_{O(max)}$	Peak output current	top=10ms ; repetive cycle 0.2Hz max	±3.0	A
$I_{O(1)}$	Continuous output current (1)		±300	mA
$I_{O(2)}$	Continuous output current (2)	With an external hbat sink (3000mm²×1.5mmt)	±800	mA
P_d	Power dissipation	T_a=75℃	0.8	W
Topr	Operating temperature		−10～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

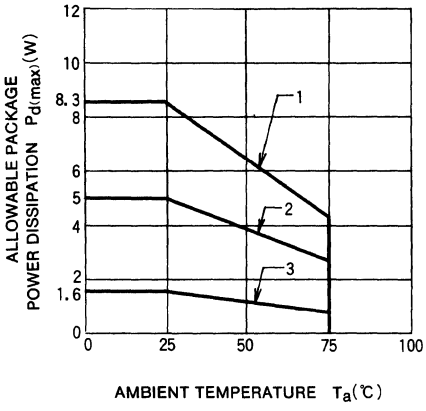
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	12	18	V
I_O	Output current				±300	mA
V_{IH}	High-level input voltage		3		V_{CC}	V
V_{IL}	Low-level input voltage		0		1	V
t_B	Moter braking interval		100			ms
$t_{j(shut)}$	Thermal shutdown temperature		125	150		℃

ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
$I_{O(leak)}$	Output leakage current	V_{S1}=0V, S_{S2}=0V, V_{S3}=0V		V_O=0V, V_{CC}=V_S=20V			−100	μA
				V_O=14V, V_{CC}=V_S=14V			+100	
$V_{OH(1)}$	High-level output voltage (1)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S2}=0V, V_{S3}=3V	I_{OH}=−200mA	13			V
				I_{OH}=−500mA	12.8			
$V_{OH(2)}$	High-level output voltage (2)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S3}=0V, V_{S2}=3V	I_{OH}=−200mA	13			V
				I_{OH}=−500mA	12.8			
$V_{OL(1)}$	Low-level output voltage (1)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S3}=0V, V_{S2}=3V	I_{OL}=200mA			1.1	V
				I_{OL}=500mA			1.2	
$V_{OL(2)}$	Low-level output voltage (2)	V_{CC}=16V, $V_{IN(-)}$=0V, $V_{IN(+)}$=3V	V_{S1}=V_{S2}=0V, V_{S3}=3V	I_{OL}=200mA			1.1	V
				I_{OL}=500mA			1.2	
I_{IH}	High-level input current	V_{CC}=16V, V_{IS}=3V(S_1, S_2, S_3)					10	μA
I_{IL}	Low-level input current	V_{CC}=16V, V_{IS}=0V(S_1, S_2, S_3)					−20	μA
I_{CC}	Supply current	V_{CC}=16V, V_{S1}=V_{S2}=V_{S3}=3V					30	mA
A	Op amp open-loop-gain				50			dB

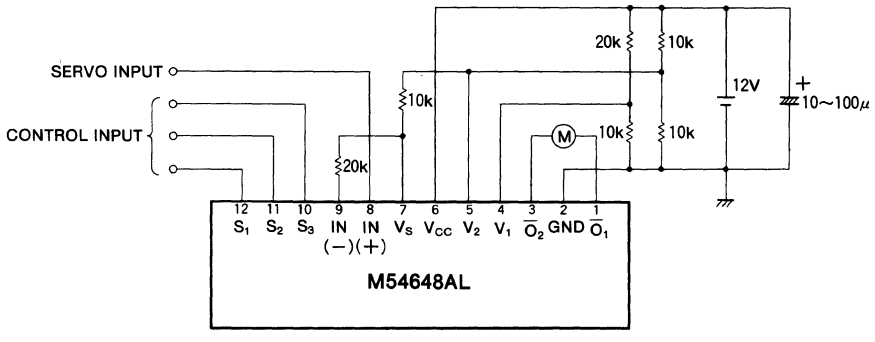
TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



1) WITH HEAT SINK OF INFINITE SIZE
2) 25cm²×1.5mmt ALUMINUM HEAT SINK
3) FREE AIR

APPLICATION EXAMPLE



Unit : Ω

M54649L

DUAL BI-DIRECTIONAL MOTER DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

DESCRIPTION

The M54649L, BI-DIRECTIONAL MOTOR DRIVER, consists of a full bridge power designed for use in are two DC-motor control circuit. The internal operational amplifier is capable for controlling the voltage across the bridge outputs.

FEATURES

- Capable of driving two bi-directional motors
- High-level Output voltage control pin
- Internal thermal shutdown protector
- Large output sink current ($I_{O(max)}$=1.6A)
- Wide operating supply voltage (V_{CC}=4~18V)
- CMOS IC output for direct drive

APPLICATION

Audio tape deck, radio cassette player, VTR, Home-use equipment

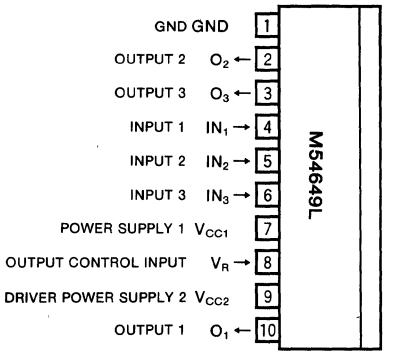
FUNCTION

The M54649L, full bridge motor driver, has the logic circuitry and the darlington power driver for bi-directional control of two DC motors operating at current up to 1.6A.

The input IN1, IN2 and IN3 are capable to control the bridge output polarity.

The internal thermal shutdown protector protects the IC from thermal destruction due to blocking of motor, etc.

PIN CONFIGURATION (TOP VIEW)

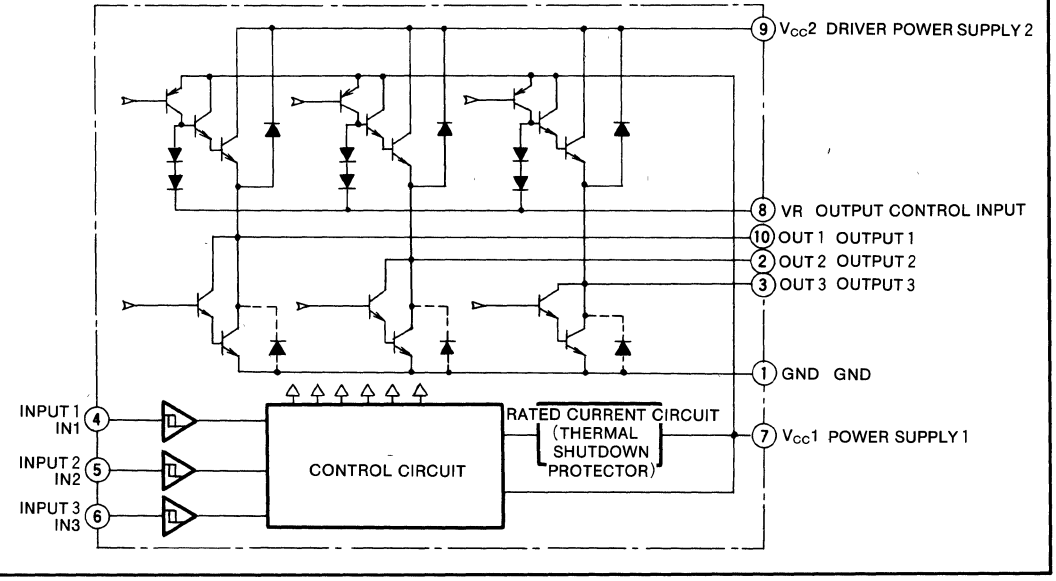


Outline 10P5

LOGIC TRUTH TABLE

Input			Output			Note
4 PIN (IN 1)	5 PIN (IN 2)	6 PIN (IN 3)	10 PIN (OUT 1)	2 PIN (OUT 2)	3 PIN (OUT 3)	
L	L	L / H	L	L	L	Braking
H	L	L	H	L	OPEN	↻
H	L	H	L	H	OPEN	↻
L	H	L	H	OPEN	L	↻
L	H	H	L	OPEN	H	↻
H	H	L / H	L	L	L	Braking

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M54649L

DUAL BI-DIRECTIONAL MOTER DRIVER WITH BRAKE FUNCTION AND THERMAL SHUT DOWN FUNCTION

ABSOLUTE MAXIMUM RATING (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(1)}$	Supply voltage (1)		−0.5～+20.0	V
$V_{CC(2)}$	Supply voltage (2)		−0.5～+22.0	V
V_I	Input voltage		−0.5～+7.0	V
V_O	Output voltage		−2.0～V_{CC}+2.5	V
I_{OP}	Peak output current	top≧50ms; duty cycle 1/50	±1.60	A
I_O	Continuous output current	Note 1	±600	mA
Pd	Power dissipation	Time of power applicatton 10s or less	2.78	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(1)}$	Supply voltage (1)		4.0	12.0	18.0	V
$V_{CC(2)}$	Supply voltage (2)		0.0		22.0	V
I_O	Output current				±600	mA
V_{IH}	High-level input voltage		3.5		V_{CC}	V
V_{IL}	Low-level input voltage		0.0		1.0	V
V_R	Control voltage		0.0		18.0	V
T_{ON}	Thermal shutdown temperature		125	150		℃
$\triangle T_{ON}$-OFF	Hysteresis temperature width			50		℃

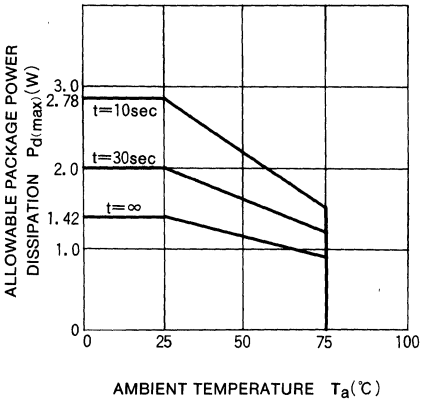
ELECTRICAL CHARACTERISTICS (T_a=25℃, unless oterwise noted)

Simbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$I_{O(leak)}$	Output leakage current	Output open V_O=0 or 20V	$V_{CC1, 2}$=20V			±100	μA
V_{OL}	Low-level output saturation voltage	I_{OL}=500mA	$V_{CC1, 2}$=12V			1.5	V
V_{OH}	High-level output saturation voltage	I_{OH}=−500mA	$V_{CC1, 2}$=12V	10.0			V
$\triangle V_O$	High-level input current	I_O=±500mA V_R=6.0V	$V_{CC1, 2}$=12V	−0.5		0.5	V
I_R	Low-level input current	I_O±500mA V_R=6.0V	$V_{CC1, 2}$=12V	0.2		1.5	mA
I_{CC1}	Supply current	$V_{IN1, 2, 3}$=1.0V I_O=0mA	$V_{CC1, 2}$=12V		8.0	24.0	mA

* : A typical value is at T_a=25℃.

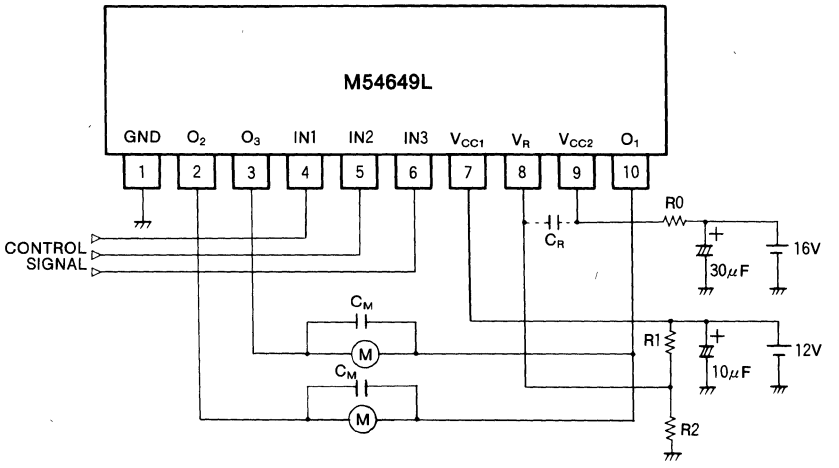
TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION



- Minimum heat protection at 125℃
- Mounted on an epoxy PC board with Cu cover on one side (50×50×0.8mm)
- t : time for power application at single pulse duration

APPLICATION EXAMPLE



CM : Noise absorbing capacitor when the motor is driven should be less than 0.1μF.

RO ($\frac{R_1}{R_2}$) : The "H" output voltage $V_{O(H)}$ is given in,

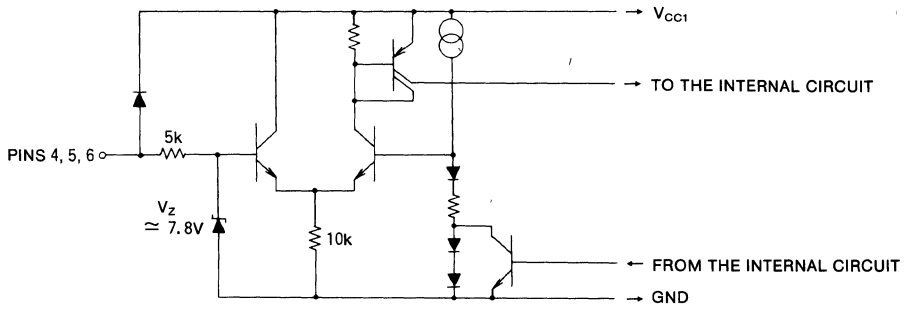
$$V_{O(H)} \fallingdotseq V_{CC1} \times \frac{R_2}{R_1+R_2}$$

If the resistance of the R_1 and R_2, the output current $V_{O(H)}$ is higher than the V_R (pin 8).

CR : If separate power supply is used for the V_R (pin 8), the output may oscillate. In this case, a capacitor C_R (0.01μF) must be connected between the V_R (pin 8) and $V_{CC}2$ (pin 9).

PRECAUTIONS FOR USE

1. Input circuit schematic diagram



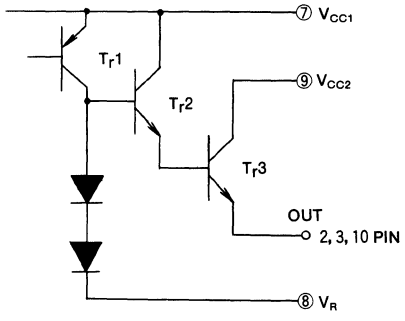
Apply 3.5V−V_{CC} to the ON voltage (V_{IH}) and 0−1V to the OFF voltage (V_{IL}) of the input.
If the input voltage reaches approximately 7.8V or above, the impedance changes to approximately 5kΩ and, therefore the voltage should be kept below 7V.

2. Output voltage control method

The output cotrol circuit using the pin 8 is described on the right, and the voltage which is almost equal to the 8 pin voltage is output from the circuit. ("H" side)
If pin 8 is open, the maximum output voltage is available when $V_{CC2} > V_{CC1}$ and the voltage is given in,

$$V_O = V_{CC1} - V_{sat}(Tr1) - V_{BE}(Tr2) - V_{BE}(Tr3)$$

The output voltage can be controlled by varying the V_{CC1} in this condition.



3. Precaution for braking

Care must be taken to braking mode input because the motor may affect other motors at the moment when it is switched from driving condition to braking condition.

4. Allowable power dissapation

The allowable power dissipation of the IC (P_d), when $V_{CC2} > V_{CC1}$, is given by.

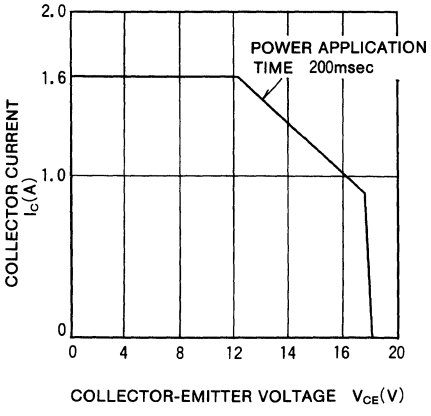
$$P_d = V_{CC1} \times I_{CC1} + I_O \{V_{CC2} - V_{OH} + V_{OL}\}$$

The equipment must be so designed as not exceed this limit.

5. Thermal shutdown

The internal thermal shutdown circuit is provided to protect the IC from overheating when excessive power is applied.
The protection circuit functions when the temperature of the IC reaches 150℃ (Min. 125℃), and all outputs are in the OPEN mode, and is canceled when the temperature is decreased to 100℃ (Max. 125℃).

6. Aso Characteristics



7. Others

Capacitors which are connected between power supply and GND should be placed as close to the IC as possible. Care should be taken as the capacitors may cause oscillation otherwise.

M54660P

8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

DESCRIPTION

The M54660P, 8-channel source driver, consists of 8 PNP and 16 NPN transistors connected to from eight high current gain driver with PNP action.

FEATURES

- High output sustaining voltage to 80V
- High output source current to 500mA
- Wide operating temperature range (T_a=−20∼+75℃)

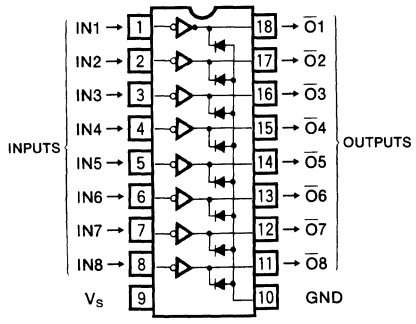
APPLICATION

Relay and printer driver, LED, incandescent or fluorescent display driver, Interfacing for standard MOS/BIPOLAR logics

FUNCTION

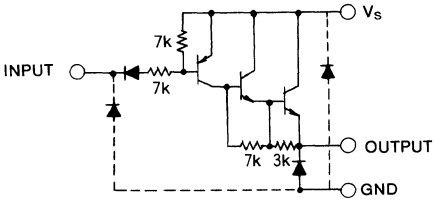
The M54660P is comprised of eight PNP-NPN darlington source driver pairs with a diode and 7kΩ resistor in series to the input. The output is turned ON by switching the input low. Each output has an integral diode for inductive load transient suppression. The outputs are capable of driving 500mA and are rated for operation with output voltage up to 80V.

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+80	V
V_S	Supply voltage	Transistor ON	−0.5∼+80	V
V_I	Input voltage		0∼V_S−30	V
I_O	Output current	Per channel current at "H" output	−500	mA
I_F	Clamp diode forward current		−500	mA
V_R	Clamp diode reverse voltage		80	V
P_d	Power dissipation	T_a=25℃	1.79	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_S	Supply voltage		0		80	V
I_O	Output current per channel	All units ON Percent duty cycle≦8%	0		−350	mA
		All units ON Percent duty cycle≦55%	0		−100	
V_{IH}	"H" Input voltage	$I_{O(leak)}$=−50μA	V_S−0.7		V_S	V
V_{IL}	"L" Input voltage	I_C=−350mA	0		V_S−3.6	V

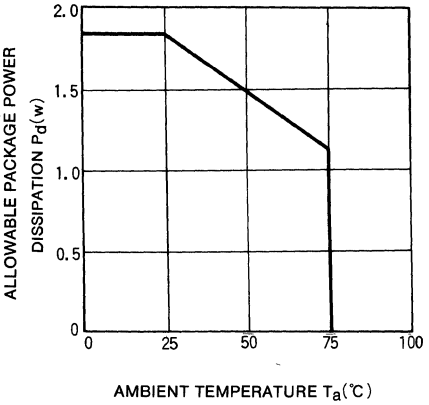
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA	80			V
$V_{CE(sat)}$	Output saturation voltage	V_I=V_S−3.2V, I_O=−100mA			2.0	V
		V_I=V_S−3.6V, I_O=−350mA			2.4	
I_I	Input current	V_I=V_S−3.6V			−0.6	mA
		V_I=V_S−15V			−3.2	
I_R	Input leakage current	V_I=40V			100	μA
V_R	Clamp diode reverse voltage	I_R=100μA	80			V
h_{FE}	DC forward current gain	V_{CE}=4V, I_C=−350mA T_a=25℃	1000			—

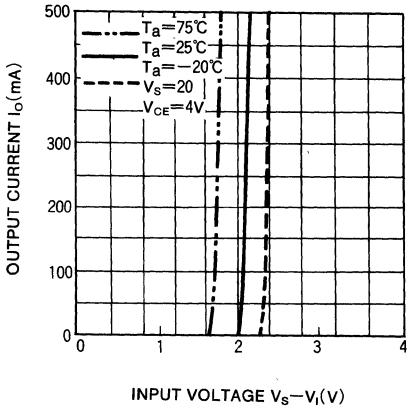
* : A typical value at T_a = 25℃.

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

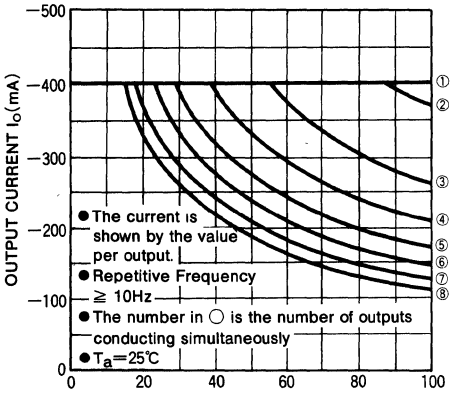


OUTPUT CURRENT CHARACTERISTICS



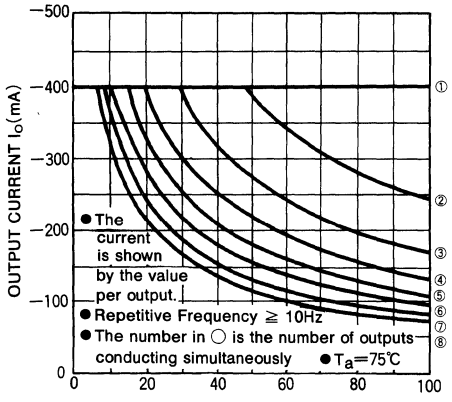
8-UNIT HIGH VOLTAGE 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



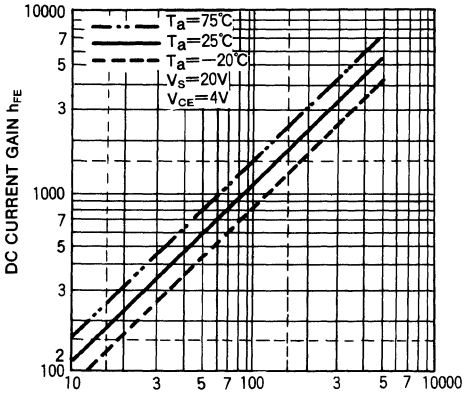
DUTY CYCLE (%)

ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



DUTY CYCLE (%)

DC CURRENT GAIN CHARACTERISTICS



COLLECTOR CURRENT I_C(mA)

M54661P

4-UNIT HIGH VOLTAGE 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

DESCRIPTION

The M54661P, 4-channel sink driver, consists of 4 PNP and 8 NPN transistors to from four high current gain driver pairs.

FEATURES

- High output sustaining voltage to 80V
- High output current to 1.5A
- Integral diodes for transient suppression
- NMOS Compatible input
- Wide operating temperature range (T_a=−20∼+75℃)

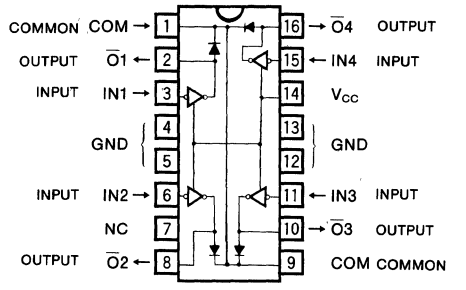
APPLICATION

Relay and printer driver, LED or incandescent display digit driver

FUNCTION

The M54661P is comprised of four PNP invertors with 7kΩ series input resistors and NPN darlington sink drivers. Each output has an integral diode for inductive load transient suppression and the anodes of the diode connected to pins 1 and 9. The outputs are capable of sinking 1.5A and will withstand 80V in the OFF state.

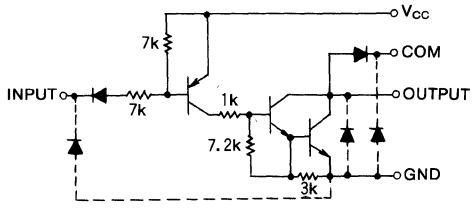
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

CIRCUIT SCHEMATIC



The diodes shown by broken line are parasite diodes and must not be used

Unit : Ω

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+10	V
V_{CEO}	Output sustaining voltage	Transistor OFF	−0.5∼+80	V
V_I	Input voltage		−0.5∼30	V
I_C	Collector current	Transistor ON	1.5	A
V_R	Clamp diode reverse voltage		80	V
I_F	Clamp diode forward current	Pulse width≦10ms, Percent duty cycle≦5%	1.5	A
		Pulse width≦100ms, Percent duty cycle≦5%	1.25	
P_d	Power dissipation	T_a=25℃	1.92	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

M54661P

4-UNIT HIGH VOLTAGE 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

RECOMMENDED OPERATIONAL CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
V_O	Output voltage		0		80	V
I_C	Collector current per channel	All units ON Percent duty cycle≦4%	0		1.25	A
		All units ON Percent duty cycle≦18%	0		0.7	
V_{IH}	"H" Input voltage	$I_{O(leak)}$=50μA	V_{CC}−0.5		V_{CC}	V
V_{IL}	"L" Input voltage	I_C=1.25A	0		V_{CC}−3.5	V

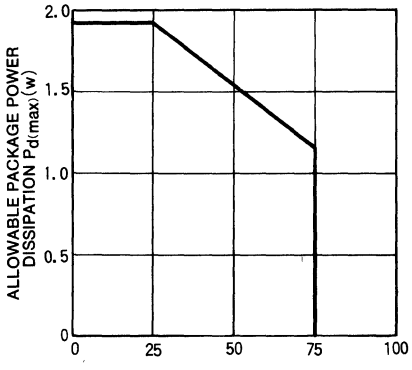
ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
$V_{(BR)CEO}$	Output sustaining voltage	I_{CEO}=100μA		80			V
I_{CC}	Supply current	V_{CC}=6V, V_I=0.5V (per channel)			4.6	7.5	mA
$V_{CE(sat)}$	Output saturation voltage	V_{CC}=4V	I_C=1.25A			2.2	V
		V_I=0.5V	I_C=0.7A			1.7	
I_I	Input current	V_I=V_{CC}−3.5V				−0.6	mA
		V_I=V_{CC}−6V				−0.95	
V_R	Clamp diode reverse voltage	I_R=100μV		80			V
V_F	Clamp diode forward voltage	I_F=1.25A				2.3	V
h_{FE}	DC forward current gain	V_{CC}=4V, V_{CE}=4V, I_C=1A, T_a=25℃		4000			—

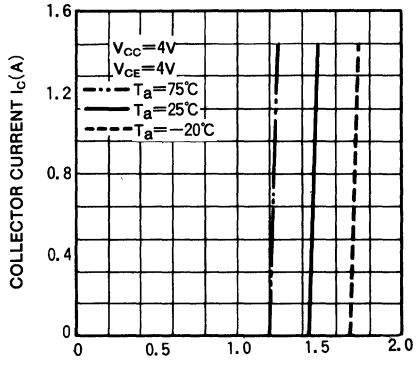
* : A typical value is at T_a = 25℃

TYPICAL CHARACTERISTICS

ALLOWABLE AVERAGE POWER DISSIPATION

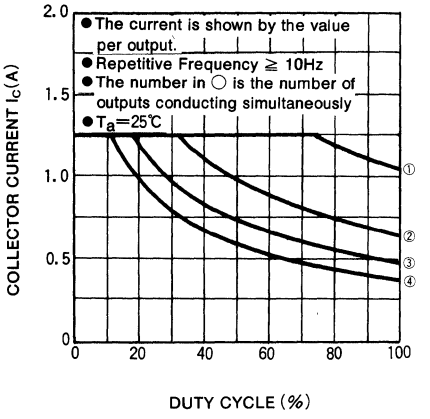


OUTPUT CURRENT CHARACTERISTICS

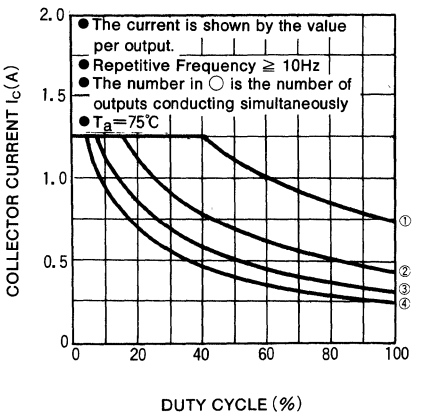


4-UNIT HIGH VOLTAGE 1.5A DARLINGTON TRANSISTOR ARRAY WITH CLAMP DIODE

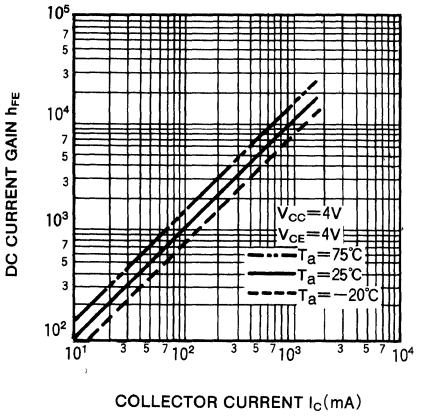
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



DC CURRENT GAIN CHARACTERISTICS



MITSUBISHI ELECTRIC

M54700AP, S/P, S-1/P, S-2
M54701AP, S/P, S-1/P, S-2

1024-BIT (256-WORD BY 4-BIT) FIELD PROGRAMMABLE READ ONLY MEMORY

The electrical characteristics and programming conditions of the M54700P,S were changed to make the M54700AP,S

DESCRIPTION

The M54700AP,S (open collector output) as well as the M54701AP,S (three state output) are field programmable ROM's with fuse links type 1024-bit (256 words × 4-bit) memories.

FEATURES

- Access time
  - M54700AP,S-1/M54701AP,S-1 ..... 30ns (Max)
  - M54700AP,S-2/M54701AP,S-2 ..... 35ns (Max)
  - M54700AP,S/M54701AP,S ..... 50ns (Max)
- Unique built-in test guarantee circuits a high programming yield as well as various performance characteristics after programming.
- Fuse technology is used.
- Memory capacity: 1024 bits (256 words × 4 bits)
- Output type M54700AP,S (open collector output)
  M54701AP,S (three state output)
- Output level before programming is high.
- Chip enable pin $\overline{E_1}$, $\overline{E_2}$ provided for easy expansion of memory capacity.
- Input and output are TTL compatible.
- Package is 16-pin DIL ceramic or plastic.

APPLICATION

General purpose, for use in industrial and consumer equipment

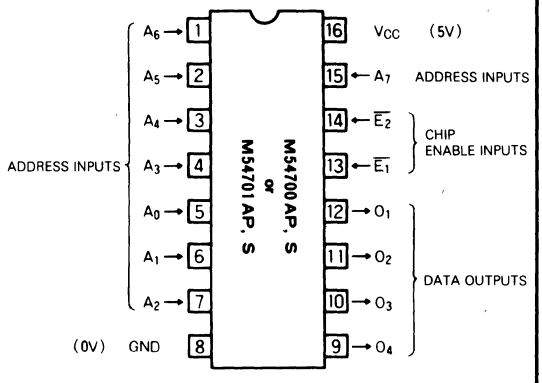
SUMMARY OF OPERATION

The unit consists of an address circuit, decoder circuit, memory circuit, output circuit, and a chip enable circuit. The memory cells are structured from fuses and diodes. Data can be programmed into the PROM by the user using a writer by cutting the fuses of the memory cells. Before programming, the output level is high. After programming, the output level becomes low.

The 1024 bit memory is made up of 256 words with 4 bits associated with each word. Through the address inputs (A_0-A_7) one word out of the 256 is chosen and a 4-bit parallel output (O_1-O_4) is obtained.

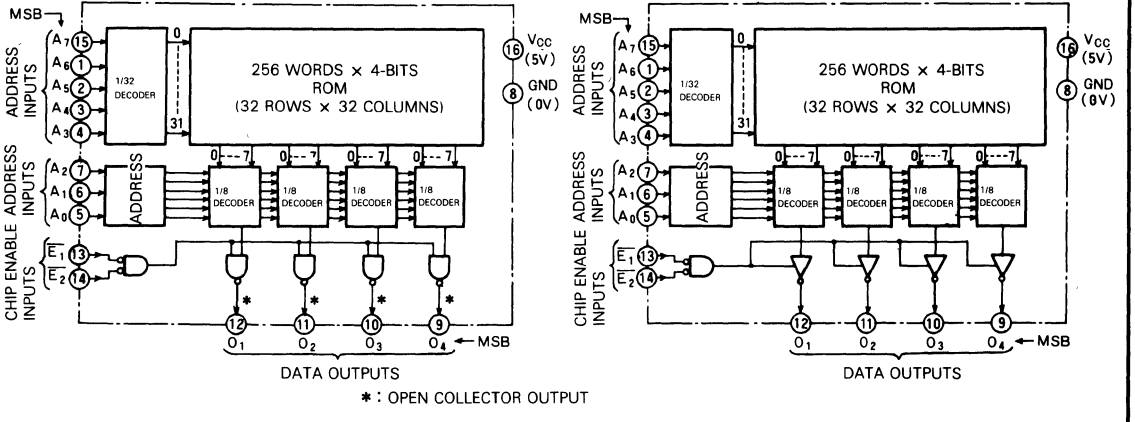
Input and output threshold voltages are the same as that for a TTL system and thus direct coupling can be made with TTL logic. Output is open collector (M54700AP,S) or three-state (M54701AP,S) so AND ties are possible.

PIN CONFIGURATION (TOP VIEW)



Outline 16 S1 (M54700AS, M54701AS)
16 P4 (M54700AP, M54701AP)

BLOCK DIAGRAM



M54700AP, S/P, S-1/P, S-2/M54701AP, S/P, S-1/P, S-2

1024-BIT (256-WORD BY 4-BIT) FIELD PROGRAMMABLE READ ONLY MEMORY

When both of the chip enable inputs, $\overline{E_1}$ and $\overline{E_2}$ are at low level, the otuput is enabled and the content of the memory selected by the address input appears as output. If either $\overline{E_1}$ or $\overline{E_2}$ is at high level, the output is disabled and regardless of the address input, the output is "H" (open collector output) or high impedance (three-state output).

READ-OUT FUNCTION TABLE (Note 1)

M54700AP,S Read-Out Function Table

$\overline{E_1}$	$\overline{E_2}$	$O_1 \sim O_4$
L	L	Wn
H	L	H
L	H	H
H	H	H

M54701AP,S Read-Out Function Table

$\overline{E_1}$	$\overline{E_2}$	$O_1 \sim O_4$
L	L	Wn
H	L	Z
L	H	Z
H	H	Z

Note 1 Wn The memory content programmed in Wn word appears as output
Z High impedance state

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C, unlees otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	When output is high level	−0.5 ~ +5.5	V
V_{OP}	Applied output voltage	During programming	21	V
$t_{W(P)}/t_{C(P)}$	Duty cycle	During programming	25	%
Topr	Operating temperature		−20 ~ +75	°C
Tstg	Storage temperature		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High level output current (M54701AP/S) $V_{OH} \geqq 2.4V$	0		−2	mA
I_{OH}	High level output current (M54700AP/S) V_O=5V	0		50	μA
I_{OL}	Low level output current $V_{OL} \leqq 0.45V$	0		16	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

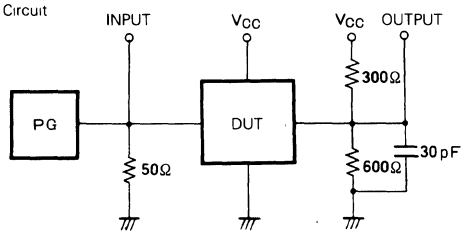
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA			−1.2	V
V_{OH}	High level output voltage (M54701AP, S)	V_{CC}=4.75V, V_I=2V, V_I=0.8V I_{OH}=−2mA	2.4	3.1		V
I_{OH}	High level output current (M54700AP, S)	V_{CC}=5.25V, V_I=2V, V_I=0.8V V_O=5V			50	μA
V_{OL}	Low level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OL}=16mA		0.3	0.45	V
I_{OZH}	Off-state High level output current (M54701AP, S)	V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=2.4V			50	μA
I_{OZL}	Off-state Low level output current (M54701AP, S)	V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=0.4V			−50	μA
I_{IH}	High level input current	V_{CC}=5.25V, V_I=2.4V			40	μA
I_{IL}	Low level input current	V_{CC}=5.25V, V_I=0.4V		−100	−250	μA
I_{OS}	Output short-circuit current (M54701AP, S) (Note 2)	V_{CC}=5.25V, V_O=0V	−15		−100	mA
I_{CC}	Supply current (Note 3)	V_{CC}=5.25V, V_I=0V		80	120	mA
C_{IN}	Input capacitance	V_{CC}=5V, V_I=2V, f=1MHz		4		pF
C_{OUT}	Output capacitance	V_{CC}=5V, V_O=2V, f=1MHz		7		pF

* : A typical value at T_a=25°C
Note 2 All measurements should be done quickly and not more than one output should be shorted at a time
3 I_{CC} is measured with all inputs at GND

SWITCHING CHARACTERISTICS (V_{CC} = 5V ± 5%, T_a = 0 ~ 75°C, unless otherwise noted) (Note 4)

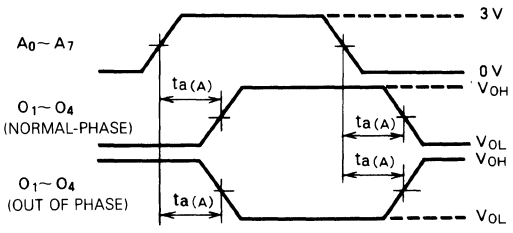
Symbol	Parameter	Limits									Unit
		M54700AP, S-1 M54701AP, S-1			M54700AP, S-2 M54701AP, S-2			M54700AP, S M54701AP, S			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{a(A)}$	Address access time		20	30		20	35		20	50	ns
$t_{a(\overline{E})}$	Chip enable access time		20	30		20	30		20	30	ns
$t_{CD(\overline{E})}$	Chip disable time		20	30		20	30		20	30	ns

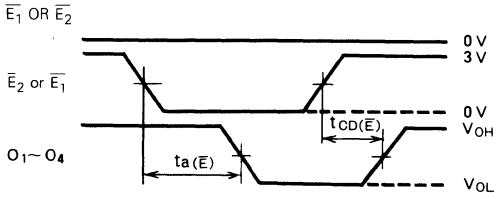
Note 4 Test Circuit



1 PG characteristics t_r = 6ns, t_f = 6ns, PRR = 1MHz, t_{PW} = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
2 The electrostatic capacitance of the load includes probe and jig capacitance

TIMING DIAGRAMS (Reference voltage = 1.5V)

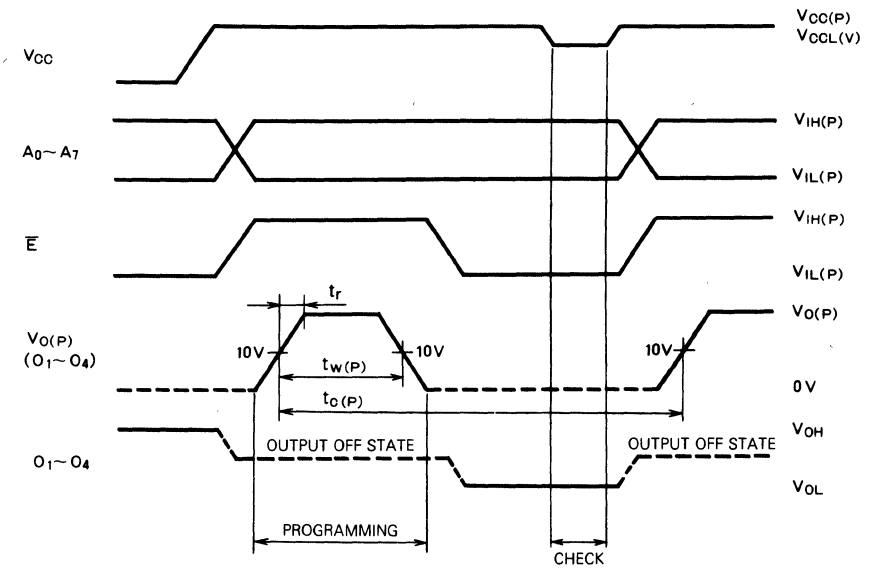




RECOMMENDED OPERATING CONDITIONS FOR PROGRAMMING (Unless otherwise noted, T_a = 25°C)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{IH(P)}$	High level input voltage	2.4	5	5	V
$V_{IL(P)}$	Low level input voltage	0	0	0.4	V
$V_{O(P)}$	Applied output voltage	20	21	21	V
$t_{W(P)}$	Applied pulse width	0.05	0.18	50	ms
$t_{W(P)}/t_{C(P)}$	Duty cycle		20	25	%
t_r	Pulse rise time	5	10	30	μs
$N_{(P)}$	Number of pulse applied	1	4	4	—
$V_{CC(P)}$	Supply voltage during programming	4.9	5	5.1	V
I_{OP}	Applied output current			100	mA
$V_{CCL(V)}$	Low level supply voltage for check after programming	4.4	4.4	4.5	V

PROGRAMMING TIMING DIAGRAM



Note 5 $V_{O(P)}$ is the wave form applied to the output during programming $O_1 \sim O_4$ are the waveforms showing the output of the element itself
6 $\overline{E}$ is the waveform for either $\overline{E}_1$ or $\overline{E}_2$, the other being taken as $V_{IL(P)}$

PROGRAMMING METHOD

The elements actually programmed are the fuses making up the 1,024 memory cells. When the memory cell is not programmed, the output is logic high level (fuse closed). To put these at logic low level (fuse open), the following steps are taken.

(1) Apply $V_{CC(P)}$ supply voltage (5V Typ).
(2) Select the word to be programmed by using the address inputs A_0 - A_7 (Input voltage: $V_{IH(P)}$ 5V Typ, $V_{IL(P)}$ 0V Typ).
(3) Put at least one of the chip enable inputs $\overline{E}_1$, $\overline{E}_2$, at high level ($V_{IH(P)}$ 5V Typ) and put the output in the OFF state.
(4) An output pulse $V_{O(P)}$ (21V Typ) is applied to the output corresponding to the bit to be programmed. $V_{O(P)}$ must be applied to each individual output; do not apply it to two or more outputs at the same time.
(5) Put both $\overline{E}_1$ and $\overline{E}_2$ at low level ($V_{IL(P)}$ 0V Typ).
(6) Put the supply voltage at $V_{CCL(V)}$ (4.4V Typ) and check whether programming was completed or not.
(7) If the test in step (6) is passed, repeat steps (1) through (6) for the next bit or word to be programmed. If the test in step (6) is not passed, repeat steps (1) through (6). If these steps are repeated four times and test results are not positive, the IC can be considered defective.

For timing, refer to the programming timing diagrams.

M54730AP, S/P, S-1/P, S-2
M54731AP, S/P, S-1/P, S-2

256-BIT (32-WORD BY 8-BIT) FIELD PROGRAMMABLE READ ONLY MEMORY

The electrical characteristics and programming conditions of the M54730P,S were changed to make the M54730AP,S

DESCRIPTION

The M54730AP, S (open collector output) as well as the M54730AP,S (three state output) are field programmable ROM's with fuse links type 256 bit (32 word × 8 bit) memories.

FEATURES

- Access time:
  M54730AP, S-1/M54731AP, S-1 ..... 30ns (Max)
  M54730AP, S-2/M54731AP, S-2 ..... 35ns (Max)
  M54730AP, S/M54731AP, S ..... 50ns (Max)
- Unique built-in test circuits guarantee high programming yield as well as various performance characteristics after programming
- Fuse technology is used
- Memory capacity: 256 bits (32 words × 8 bits)
- Output type: M54730AP,S (open collector output)
  M54731AP,S (three state output)
- Output level befor programming is high
- Chip enable pin $\overline{E}$ provided for easy expansion of memory capacity
- Input and output are TTL compatible
- Package is 16-pin DIL ceramic or plastic

APPLICATION

General purpose, for use in industrial and consumer equipment

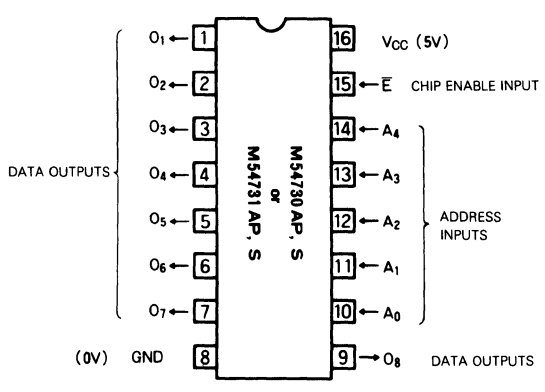
SUMMARY OF OPERATION

The unit consists of an address circuit, decoder circuit, memory circuit, output circuit, and a chip enable circuit. The memory cells are structured from fuses and diodes. Data can be programmed into the PROM by the user using a writer by cutting the fuses of the memory cells. Before programming, the output level is high. After programming, the output level becomes low.

The 256 bit memory is made up of 32 words with 8 bits associated with each word. Through the address inputs $A_0 \sim A_4$, one word out of the 32 is chosen and an 8-bit parallel output, $O_1 \sim O_8$, is obtained.

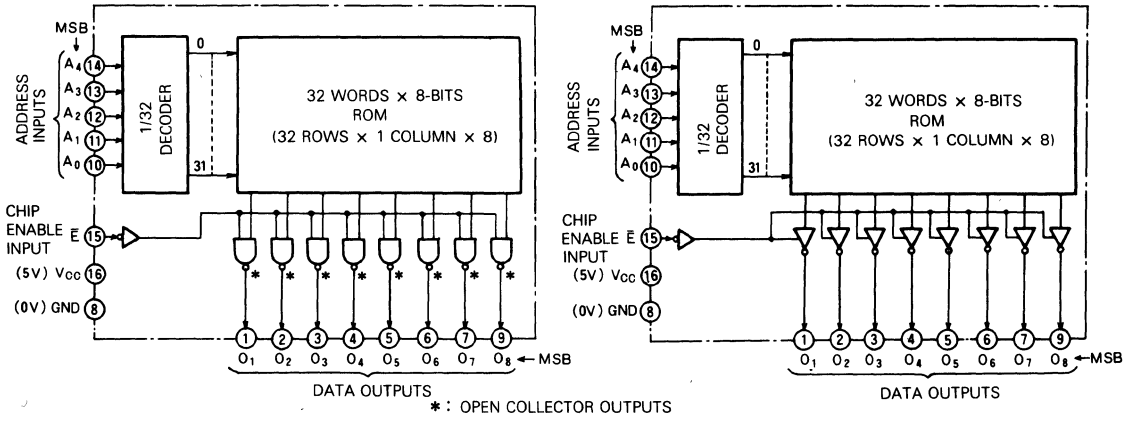
Input and output voltages threshold are the same as that for a TTL system and thus direct coupling can be made with TTL logic. Output is open collector (M54730AP,S) or 3-state (M54731AP,S) so AND ties are possible.

PIN CONFIGURATION (TOP VIEW)



Outline 16 S1 (M54730AS, M54731AS)
16 P4 (M54730AP, M54731AP)

BLOCK DIAGRAM



M54730AP, S/P, S-1/P, S-2/M54731AP, S/P, S-1/P, S-2

256-BIT (32-WORD BY 8-BIT) FIELD PROGRAMMABLE READ ONLY MEMORY

When the chip enable input $\overline{E}$ is at low level, the output is enabled and the content of the memory selected by the address input appears as output. When $\overline{E}$ is at high level, the output is disabled and regardless of the address input the output is high level (open collector output) or high impedance (3-state output).

READ-OUT FUNCTION TABLE (Note 1)

M54730AP,S Read-out function Table

$\overline{E}$	$O_1 \sim O_4$
L	Wn
H	H

M54731AP,S Read-out funciton Table

$\overline{E}$	$O_1 \sim O_4$
L	Wn
H	Z

Note 1 Wn. The memory content programmed in Wn word appears as output
Z High impendance state

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	When output is high level	−0.5 ~ +5.5	V
V_{OP}	Applied output voltage	During programming	21	V
$t_{W(P)}/t_{C(P)}$	Duty cycle	During programming	25	%
Topr	Operating temperature		−20 ~ + 75	°C
Tstg	Storage temperature		−65 ~ + 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High level output current (M54731AP/S) $V_{OH} \geqq 2.4V$	0		−2	mA
I_{OH}	High level output current (M54730AP/S) V_O=5V	0		50	μA
I_{OL}	Low level output current $V_{OL} \leqq 0.45V$	0		16	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA			−1.2	V
V_{OH}	High level output voltage (M54731AP, S)	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OH}=−2mA	2.4	3.1		V
I_{OH}	High level output current (M54730AP, S)	V_{CC}=5.25V, V_I=2V, V_I=0.8V, V_O=5V			50	μA
V_{OL}	Low level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OL}=16mA		0.3	0.45	V
I_{OZH}	Off-state High level output current (M54731AP, S)	V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=2.4V			50	μA
I_{OZL}	Off-state Low level output current (M54731AP, S)	V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=0.4V			−50	μA
I_{IH}	High level input current	V_{CC}=5.25V, V_I=2.4V			40	μA
I_{IL}	Low level input current	V_{CC}=5.25V, V_I=0.4V		−100	−250	μA
I_{OS}	Output short-circuit current (M54731AP, S)(Note 2)	V_{CC}=5.25V, V_O=0V	−15		−100	mA
I_{CC}	Supply current (Note 3)	V_{CC}=5.25V, V_I=0V		70	100	mA
C_{IN}	Input capacitance	V_{CC}=5V, V_I=2V, f=1MHz		4		pF
C_{OUT}	Output capacitance	V_{CC}=5V, V_O=2V, f=1MHz		7		pF

* : A typical value at T_a=25°C

Note 2 All measurements should be done quickly and not more than one output should be shorted at a time
3 I_{CC} is measured with all inputs at GND

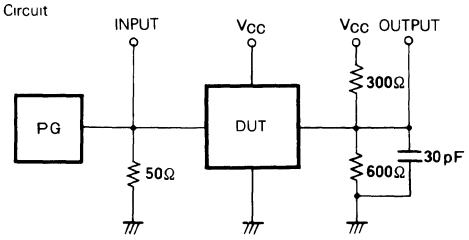
M54730AP, S/P, S-1/P, S-2/M54731AP, S/P, S-1/P, S-2

256-BIT (32-WORD BY 8-BIT) FIELD PROGRAMMABLE READ ONLY MEMORY

SWITCHING CHARACTERISTICS (V_{CC} = 5V ± 5%, T_a = 0 ~ 75°C, unless otherwise noted) (Note 4)

Symbol	Parameter	Limits									Unit
		M54730AP, S-1 M54731AP, S-1			M54730AP, S-2 M54731AP, S-2			M54730AP, S M54731AP, S			
		Min	Type	Max	Min	Typ	Max	Min	Typ	Max	
$t_{a(A)}$	Address access time		20	30		20	35		20	50	ns
$t_{a(\overline{E})}$	Chip enable access time		15	25		15	25		15	25	ns
$t_{CD(\overline{E})}$	Chip disable time		15	25		15	25		15	25	ns

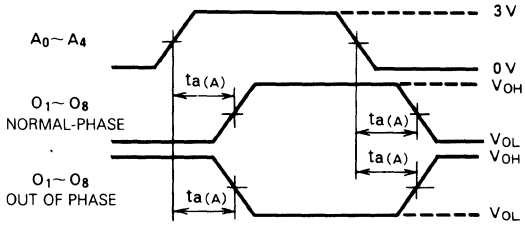
Note 4 Test Circuit

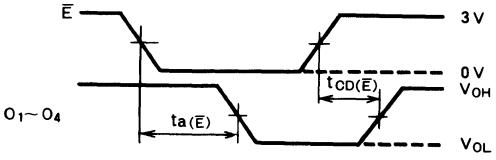


1 PG characteristics t_r = 6ns, t_f = 6ns, PRR = 1MHz, t_{PW} = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω

2 The electrostatic capacitance of the load includes probe and jig capacitance

TIMING DIAGRAM (Reference Voltage = 1.5V)

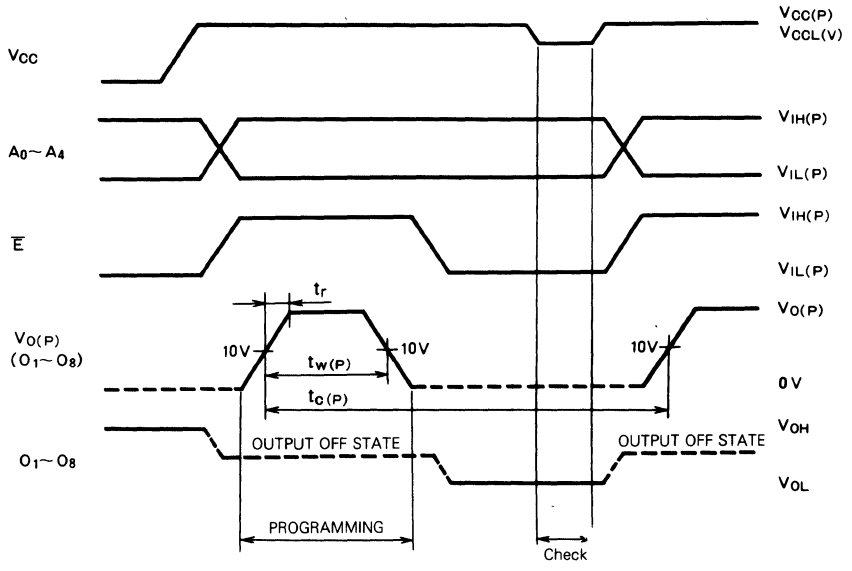




RECOMMENDED OPERATING CONDITIONS FOR PROGRAMMING (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{IH(P)}$	High level input voltage	2.4	5	5	V
$V_{IL(P)}$	Low level input voltage	0	0	0.4	V
$V_{O(P)}$	Applied output voltage	20	21	21	V
$t_{W(P)}$	Applied pulse width	0.05	0.18	50	ms
$t_{W(P)}/t_{C(P)}$	Duty cycle		20	25	%
t_r	Pulse rise time	5	10	30	μs
$N_{(P)}$	Number of pulse applied	1	4	4	—
$V_{CC(P)}$	Supply voltage during programming	4.9	5	5.1	V
I_{OP}	Output applied current			100	mA
$V_{CCL(V)}$	Low level supply voltage for check after programming	4.4	4.4	4.5	V

PROGRAMMING TIMING DIAGRAM



Note 5 $V_{O(P)}$ is the wave form applied to the output during programming O_1-O_8 are the waveforms showing the output of the element itself

PROGRAMMING METHOD

The elements actually programmed are the fuses making up the 256 memory cells. When the memory cell is not programmed, the output is logic high level (fuse closed). To put these at logic low level, the following steps are taken.

(1) Apply $V_{CC(P)}$ supply voltage (5V Typ)
(2) Select the word to be programmed by using the address inputs $A_0 \sim A_4$ (Input voltage: $V_{IH(P)}$ 5V Typ, $V_{IL(P)}$ 0V Typ)
(3) Put the chip enable input, $\overline{E}$, at high level ($V_{IH(P)}$ 5V Typ) and put the output in the OFF state.
(4) An output pulse $V_{O(P)}$ (21V Typ) is applied to the output corresponding to the bit to be programmed. $V_{O(P)}$ must be applied to each individual output; do not apply it to two or more outputs at the same time.
(5) Put $\overline{E}$ at low level ($V_{IL(P)}$ 0V Typ)
(6) Put the supply voltage at $V_{CCL(V)}$ (4.4V Typ) and check whether programming was completed or not.
(7) If the test in step (6) is passed, repeat steps (1) through (6) for the next bit or word to be programmed. If the test in step (6) is not passed, repeat steps (1) through (6). If these steps are repeated four times and test results are not positive, the IC can be considered defective.

For timing, refer to the programming timing diagrams.

M54740AP, S/P, S-1/P, S-2
M54741AP, S/P, S-1/P, S-2

4096-BIT(1024-WORD BY 4-BIT)FIELD PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The M54740AP,S (open collector output) and the M54741AP,S (three-state output) are field programmable ROM's with fuse links type 4096 bit (1,024 words x 4 bits) memories.

FEATURES

- Access time
  M54740AP, S-1/M54741AP, S-1 ..... 30ns (Max)
  M54740AP, S-2/M54741AP, S-2 ..... 35ns (Max)
  M54740AP, S/M54741AP, S ..... 50ns (Max)
- Unique built-in test circuits guarrantee high programming yield as well as various performance characteristics after programming
- Fuse technology is used
- Memory capacity: 4,096 bits (1,024 words × 4 bits)
- Output type: M54740AP,S (open collector output)
  M54741AP,S (three state output)
- Output level before programming is high
- Chip enable pin $\overline{E}_1$, $\overline{E}_2$ provided for easy expansion of memory capacity
- Input and output are TTL compatible
- Package is 18-pin DIL ceramic or plastic

APPLICATION

General purpose, for use in industrial and consumer equipment

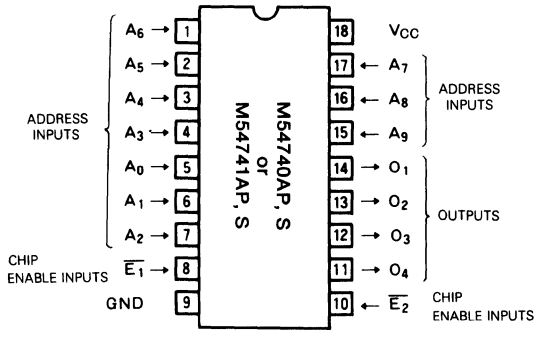
SUMMARY OF OPERATION

The unit consists of an address circuit, decoder circuit, memory circuit, output circuit, and a chip enable circuit. The memory cells are structured from fuses and diodes. Data can be programmed into the PROM by the user using a writer by cutting the fuses of the memory cells. Before programming the output level is high. After programming, the output level becomes low.

The 4,096 bit memory is made up of 1,024 words with 4 bits associated with each word. Through the address inputs ($A_0 \sim A_9$) one word out of the 1,024 is chosen and a 4-bit parallel output, $O_1 \sim O_4$, is obtained.

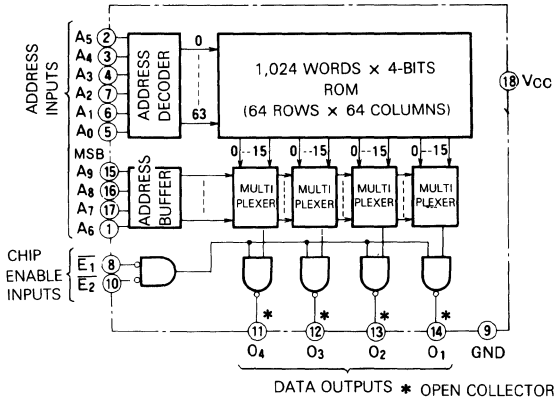
Input and output threshold voltages are the same as that for a TTL system and thus direct coupling can be made with TTL logic (M54740AP,S) or 3-state (M54741AP, S) so AND ties are possible.

PIN CONFIGURATION (TOP VIEW)

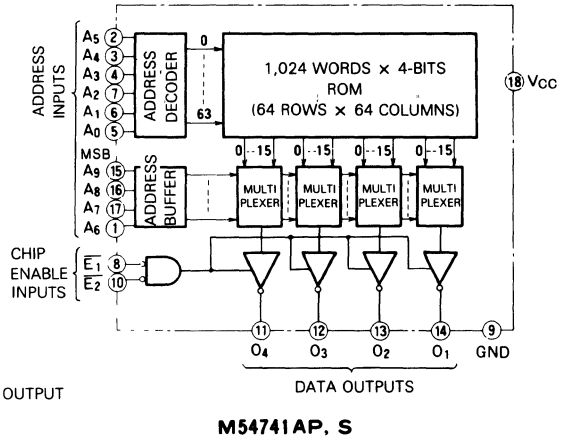


Outline 18S1 (M54740AS, M54741AS)
18P4 (M54740AP, M54741AP)

BLOCK DIAGRAM



M54740AP, S



M54741AP, S

M54740AP, S/P, S-1/P, S-2/M54741AP, S/P, S-1/P, S-2

4096-BIT(1024-WORD BY 4-BIT)FIELD PROGRAMMABLE READ ONLY MEMORY

When both of the chip enable inputs $\overline{E}_1$ and $\overline{E}_2$ are at low level the output is enabled and the content of the memory selected by the address input appears as output. If either $\overline{E}_1$ or $\overline{E}_2$ is at high level, the output is disabled and regardless of the address input, the output is "H" (open collector output) or high impedance (three-state output).

READ-OUT FUNCTION TABLE (Note 1)

M54740AP,S Read-Out Funciton Table

$\overline{E_1}$	$\overline{E_2}$	$O_1 \sim O_4$
L	L	Wn
H	L	H
L	H	H
H	H	H

M54740AP,S Read-Out Function Table

$\overline{E_1}$	$\overline{E_2}$	$O_1 \sim O_4$
L	L	Wn
H	L	Z
L	H	Z
H	H	Z

Note 1 Wn The memory content programmed in Wn word appears as output
Z High impedance state

ABSOLUTE MAXIMUM RATINGS (T_a=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	When output is high level	−0.5 ~ +5.5	V
V_{OP}	Applied output voltage	During programming	21	V
$t_{W(P)}/t_{C(P)}$	Duty cycle	During programming	25	%
Topr	Operating temperature		0 ~ +75	°C
Tstg	Storage temperature		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High level output current (M54741AP/S) $V_{OH} \geq 2.4V$	0		−2	mA
I_{OH}	High level output current (M54740AP/S) V_O=5V	0		50	μA
I_{OL}	Low level output current $V_{OL} \leq 0.45V$	0		16	mA

ELECTRICAL CHARACTERISTICS (T_a=−20 ~ +75°C, unless otherwise noted)

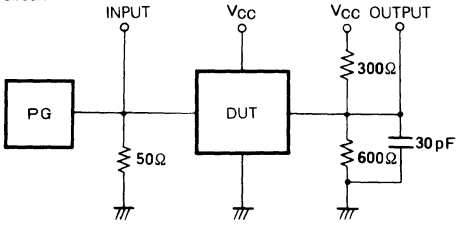
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA			−1.2	V
V_{OH}	High level output voltage (M54741AP, S)	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OH}=−2mA	2.4	3.1		V
I_{OH}	High level output current (M54740AP, S)	V_{CC}=5.25V, V_I=2V, V_I=0.8V, V_O=5V			50	μA
V_{OL}	Low level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OL}=16mA		0.3	0.45	V
I_{OZH}	Off-state high level output current (M54741AP, S)	V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=2.4V			50	μA
I_{OZL}	Off-state low level output current (M54741AP, S)	V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=0.4V			−50	μA
I_{IH}	High level input current	V_{CC}=5.25V, V_I=2.4V			40	μA
I_{IL}	Low level input current	V_{CC}=5.25V, V_I=0.4V		−160	−250	μA
I_{OS}	Output short-circuit current (M54741AP, S)(Note 2)	V_{CC}=5.25V, V_O=0V	−15		−100	mA
I_{CC}	Supply current (Note 3)	V_{CC}=5.25V, V_I=0V		120	170	mA
C_{IN}	Input capacitance	V_{CC}=5V, V_I=2V, f=1MHz		4		pF
C_{OUT}	Output capacitance	V_{CC}=5V, V_O=2V, f=1MHz		7		pF

* : A typical value at T_a=25°C
Note 2 All measurements should be done quickly and not more than one output should be shorted at a time
3 Icc is measured with all inputs at GND

SWITCHING CHARACTERISTICS (V_{CC} = 5V ± 5%, T_a = 0 ~ 75°C, unless otherwise noted) (Note 4)

Symbol	Parameter	Limits									Unit
		M54740AP, S-1 M54741AP, S-1			M54740AP, S-2 M54741AP, S-2			M54740AP, S M54741AP, S			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{a(A)}$	Address access time		25	30		25	35		25	50	ns
$t_{a(\overline{E})}$	Chip enable access time		15	25		15	25		15	25	ns
$t_{CD(\overline{E})}$	Chip disable time		15	25		15	25		15	25	ns

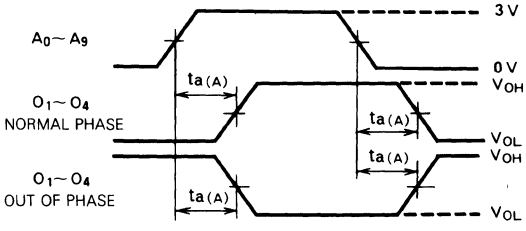
Note 4 Test Circuit

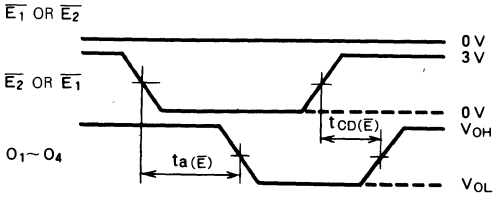


1 PG characteristics t_r = 6ns, t_f = 6ns, PRR = 1MHz, t_{PW} = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω

2 The electrostatic capacitance of the load includes probe and jig capacitance

TIMING DIAGRAMS (Reference voltage = 1 5V)

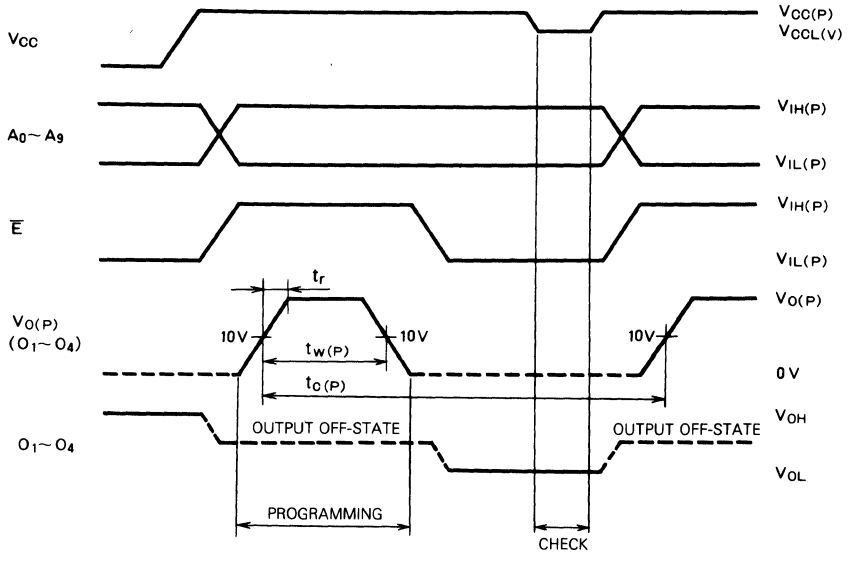




RECOMMENDED OPERATING CONDITIONS FOR PROGRAMMING (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{IH(P)}$	High level input voltage	2 4	5	5	V
$V_{IL(P)}$	Low level input voltage	0	0	0.4	V
$V_{O(P)}$	Applied output voltage	20	21	21	V
$t_{W(P)}$	Applied pulse width	0.05	0 18	50	ms
$t_{W(P)}/t_{C(P)}$	Duty Cycle		20	25	%
tr	Pulse rise time	5	10	30	μs
$N_{(P)}$	Number of pulse applied	1	4	4	—
$V_{CC(P)}$	Supply voltage during programming	4.9	5	5.1	V
I_{OP}	Applied output current			100	mA
$V_{CCL(V)}$	Low level supply voltage for check after programming	4.4	4.4	4.5	V

PROGRAMMING TIMING DIAGRAM



Note 5 $V_{O(P)}$ is the waveform applied to the output during programming
$O_1 \sim O_4$ are the waveforms showing the output of the element itself

6 $\overline{E}$ is the waveform for either $\overline{E}_1$ or $\overline{E}_2$, the other being taken as $V_{IL(P)}$

PROGRAMMING METHOD

The elements actually programmed are the fuses making up the 4,096 memory cells. When the memory cell is not programmed, the output is logic high level (fuse closed). To put these at logic low level (fuse open), the following steps are taken.

(1) Apply $V_{CC(P)}$ supply voltage (5V Typ)
(2) Select the word to be programmed by using the address inputs $A_0 \sim A_9$ (Input voltage: $V_{IH(P)}$ 5V Typ, $V_{IL(P)}$ 5V Typ).
(3) Put at least one of the enable inputs $\overline{E_1}$, $\overline{E_2}$ at "H" ($V_{IH(P)}$ 0V Typ) and put the output in the OFF state.
(4) An output pulse $V_{O(P)}$ (21V Typ) is applied to the output corresponding to the bit to be programmed. $V_{O(P)}$ must be applied to each individual output, do not apply it to two or more outputs at same time.
(5) Put both E_1 and E_2 to "L" ($V_{IL(P)}$ 0V Typ).
(6) Put the supply voltage at $V_{CCL(P)}$ (4.4V Typ) and check whether programming was completed or not.
(7) If the test in step (6) is passed, repeat steps (1) through (6) for the next bit or word to be programmed. If the test in step (6) is not passed, repeat steps (1) through (6). If these steps are repeated four times and test results are not positive, the IC can be considered defective. For timing, refer to the programming timing diagrams.

M54801P

FM DIVERSITY RECEIVER CONTROLLER

DESCRIPTION

The M54801P is an I^2L semiconductor integrated circuit consisting of an FM diversity receiver controller developed especially for car radios.

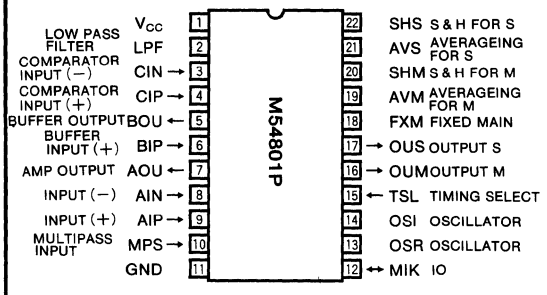
FEATURES

- Compares the reception of two antennas and selects the better one
- Employs the tuner S meter signal voltage as the input
- Wide supply voltage range (4.5~8.5V)
- Low operating supply current range (I_{CC}=10mA, V_{CC}= 7.5V)

APPLICATION

Car radios

PIN CONFIGURATION (TOP VIEW)



Outline 22P4

FUNCTION

The M54801P provides the following functions.

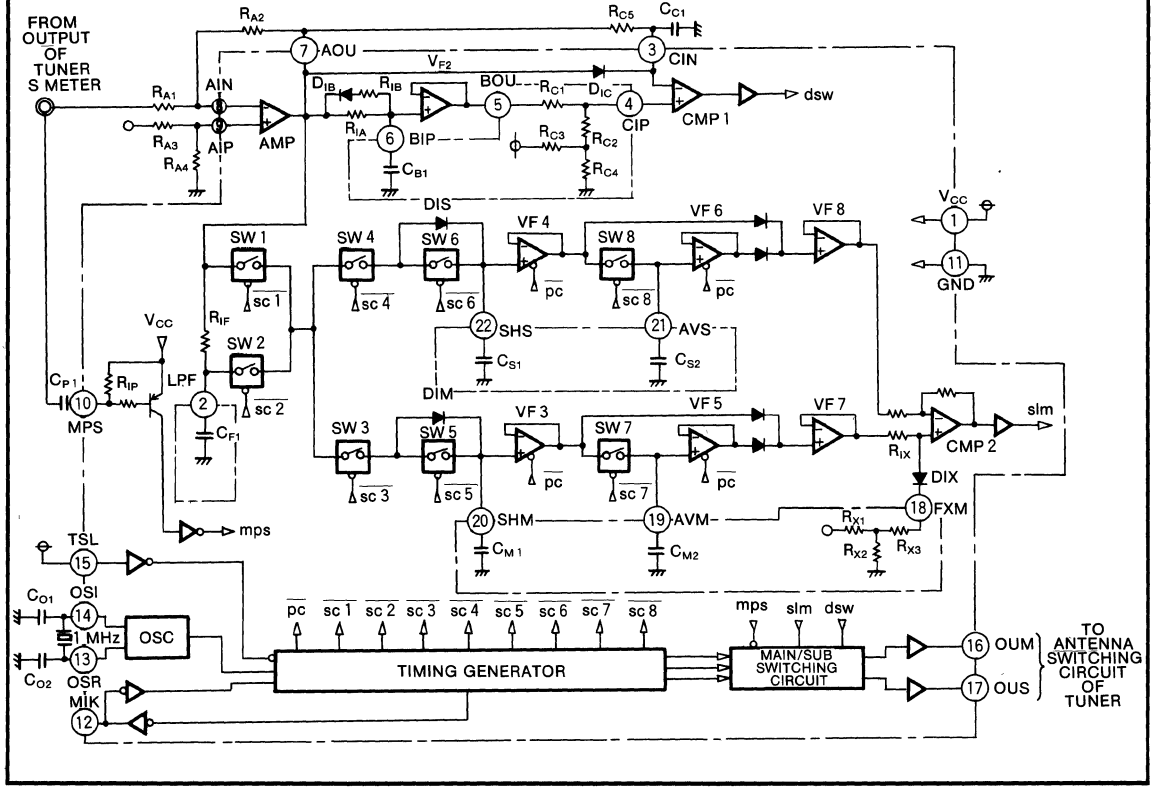
(1) Compares the reception of two antennas (main and sub antennas) at 7 ms intervals and selects the better of the two.

(2) Uses only the main antenna when the signal level at both antennas is weak.

(3) Uses the current antenna as long as the received signal is strong.

(4) Uses the S meter signal voltage of the tuner as the input signal, and outputs two antenna switching signals.

BLOCK DIAGRAM



OPERATION (See block diagram)

(1) Op-amp (AMP)
Amplifies the S meter signal voltage. Amplifier output voltage V_{AOU} increases when the received signal is weak and decreases when the received signal is strong.
(2) Main antenna sample-and-hold circuit (SW 3 →VF 7)
Holds the received signal of main antenna in analog voltage by a capacitor. Sample is held at every 7 ms, and the previous received signal which was sampled 7 ms before is also held in a separate capacitor, and whichever higher voltage is output as the received signal of the main antenna.
(3) Subantenna sample-and-hold circuit (SW 4 →VF 4)
Same as (2) except that the subantenna is monitored.
(4) Level comparator (CMP 2)
Compares the outputs of the sample-and-hold circuits for the main and subantennas, and outputs the result to the MAIN/SUB switching circuit. If the received signals from both antennas are weak, the main antenna is used.
(5) Strong signal hold circuit (VF 2 →CMP 1)
When the received signal is comparatively strong, no antenna switching takes place and the current antenna is used. If excessive multipath reception is detected, however, switching can take place.
(6) Timing generator
All timing signals are generated by this circuit using 1 MHz reference clock.
(7) OSC
Oscillator circuit for a 1 MHz ceramic resonator.

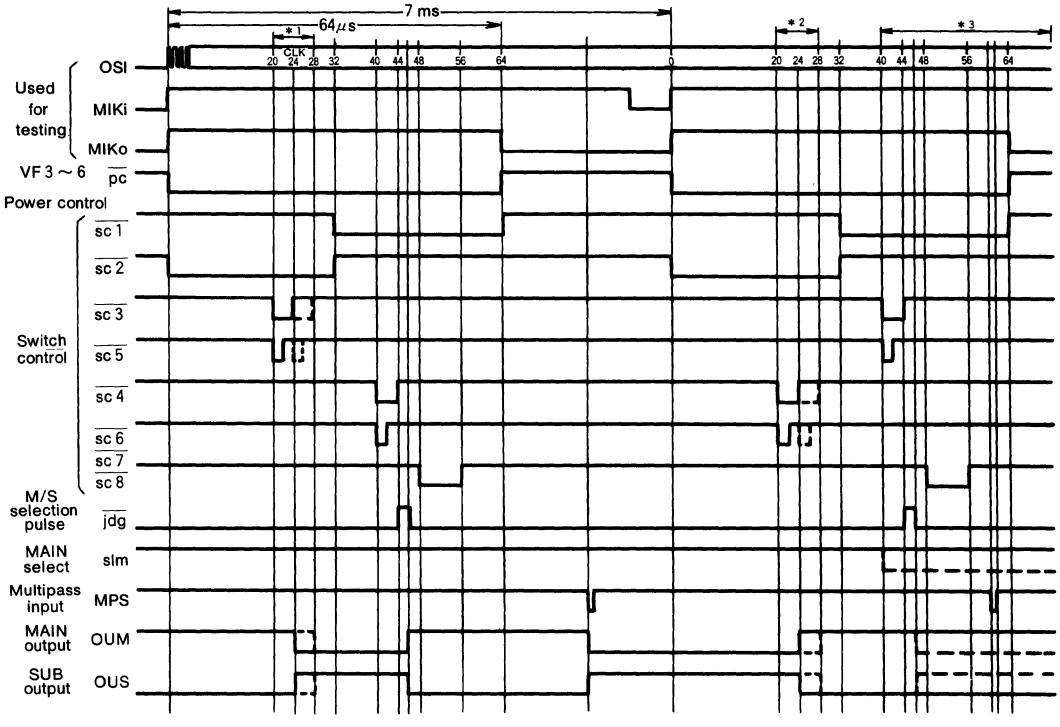
PIN DESCRIPTION

Pin number	Symbol	Description
1	V_{CC}	Supply voltage
2	LPF	Low pass filter capacitor pin
3	CIN	Inverted input of comparator CMP 1
4	CIP	Noninverted input of comparator CMP 1
5	BOU	Output of voltage follower VF 1
6	BIP	Input of voltage follower VF 1
7	AOU	Output of op-amp AMP
8	AIN	Inverted input of op-amp AMP
9	AIP	Noninverted input of op-amp AMP
10	MPS	Multipass direct input
11	GND	GND
12	MIK	I/O pin for testing Leave open This pin is not normally used
13	OSR	Ceramic resonator for oscillator OSC pin
14	OSI	Ceramic resonator for oscillator OSC pin
15	TSL	Timing selector input
16	OUM	MAIN antenna selector output
17	OUS	SUB antenna selector output. Inverted OUM signal
18	FXM	MAIN selector level setting pin
19	AVM	MAIN averaging capacitor pin
20	SHM	MAIN sample-and-hold capacitor pin
21	AVS	SUB averaging capacitor pin
22	SHS	SUB sample-and-hold capacitor pin

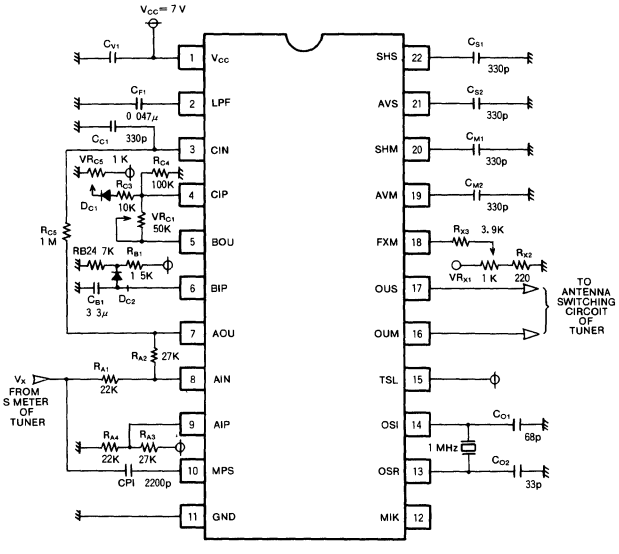
TIMING DIAGRAM

* 1 , * 2 : The timing during this period is shown in broken lines when TSL is high.

* 3 : The timing during this period is shown in broken lines when sim is low.



APPLICATION EXAMPLE



ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+80℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5∼+8.5	V
V_{IN}	Input voltage	Except MPS		−0.5∼V_{CC}+0.5	V
I_{IN}	Input current			−5∼+5	mA
V_{OUT}	Output voltage			−0.5∼V_{CC}+0.5	V
I_{OUT}	Output current			−15∼+15	mA
Topr	Operating temperature			−20∼+80	℃
Tstg	Storage temperature			−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+80℃, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			4.5	7.0	7.5	V
V_I	Input voltage	AIP, AIN		0		V_{CC}−2.0	V
I_I	Input current	MPS		−0.5		1	mA
V_{IH}	High-level input voltage	TSL		2.0		V_{CC}	V
V_{IL}	Low-level input voltage	TSL		0		0.4	V
V_O	Output voltage	AOU		0.4		V_{CC}−1.4	V
I_{OH}	High-level output current	OUS, OUM		−10		0	mA
I_{OL}	Low-level output current	OUS, OUM		0		10	mA
f_{OS}	Oscillation frequency	OSI, OSR		0.9	1.0	1.1	MHz
	Ceramic resonator	OSI, OSR	Typ name is CSB100K		1		MHz
C_{O1}	External capacitor	OSI		61	68	75	pF
C_{O2}	External capacitor	OSR		29	33	37	pF
C_{S1}, C_{M1}	External capacitor	SHS, SHM		290	330	370	pF
C_{S1}, C_{M1}	External capacitor	AVS, AVM		290	330	370	pF

ELECTRICAL CHARACTERISTICS (V_{CC}=7.0V, T_a=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min	Typ*	Max	
I_{CC}	Supply current		V_X=3.0V, I_{CC} : Average current flowing at V_{CC} pin	1		30	40	mA
R_{IP}	Input resistance	MPS	V_{F10}=6.7V, R_{IP}=0.3V/ | I_{M10} |	2	15	20	25	kΩ
V_{TMP}	Threshold voltage	MPS	TIM : D, OUT : −, CLK : 4, V_{S21}=V_{22}=0.4V, V_{S19}=V_{20}=3.0V, V_{TMP} : V_{SMO} when V_{M12}=5V	2	6.2		6.7	V
I_{IA}	Input current	AIN	V_{S9}=3.0V, V_{F8}=0.4V, I_{IA}=I_{M8}	2	−0.8		−0.1	μA
V_{OFA}	I/O offset voltage	AMP	V_{S9}=3.0V, I_{F7A}=1.5mA, AMP : V_{F1}, I_{F7B}=−0.5mA, V_{OFA}=V_{M7}−V_{S9}	2	−10		10	mV
G_{VA}	Voltage gain	AMP	S2 : ON, S_3 : OFF, V_{S8A}=2,990V, V_{S8B}=3.010V, I_{F7}=0mA, G_{VA}=(V_{M7A}−V_{M7B})/0.02V	2	95	100	105	V/V
R_{IA}	Forward resistance	BIP	V_{S9}=3.0V, V_{F6}=0.4V, AMP : V_{F1}, R_{IA}=2.6V/ | I_{M6} |	2	76	100	124	kΩ
R_{IB}	Reverse resistance	BIP	V_{S9}=3.0V, V_{F6}=5.6V, AMP : V_{F1}, R_{IB}=2.0V/($I_{M=6}-\frac{2.6V}{R_{IA}}$)	2	76	100	124	kΩ
I_{IB}	Input current	BIP	V_{S9}=0.4V, AMP : V_{F1}, I_{IB}=(V_{M6}−V_{M7})/R_{IA}	2	−0.15			μA
V_{OFB}	I/O offset voltage	VF 2	V_{S6}=3.0V, I_{F52A}=0.5mA, I_{F5B}=−0.5mA, V_{OFB}=V_{M5}−V_{S6}	2	−80		80	mV
V_{DIC}	Diode forward voltage	DIC	V_{S9}=3.0V, V_{S4}=0.4V, I_{F3}=−10μA, V_{DIC}=V_{S9}−V_{M3}	2	0.4		0.6	V
I_{IC}	Input current	CIN	V_{S9}=0.4V, V_{F3}=0.4V, Short between P3 and P4 (S4 is ON), I_{IC}=I_{M3}	2	−0.3			μA
V_{OFC}	Input offset voltage	CMP 1	TIM : D, OUT : S, CLK : 24, V_{S3}=3.00V, I_{F17}=0μA, When V_{S4A}=2.99V, V_{M17}<3V and when V_{S4B}=3.01V, V_{M17}>3V	2	−10		10	mV
R_{IF}	Parallel resistance	LPF	V_{S9}=3.0V, V_{F2}=0.4V, R_{IF}=2.6V/ | I_{M2} |	2	9	12	15	kΩ
I_{LS}	Leakage current	SHS, AVS, SHM, AVM	TIM : A, n=22, 21, 20, 19, V_{Fn}=3.0V, I_{LS}=I_{Mn}	2	−0.1		0.1	μA
I_{IV}	Input current	SHS, AVS, SHM, AVM	TIM : D, n=22, 21, 20, 19, V_{Fn}=0.4V, I_{IV}=I_{Mn}	2	−0.15			μA
V_{DIS}	Diode forward voltage	DIS	TIM : D, OUT : S, CLK : 22, V_{S2}=3V, I_{F22}=−10μA, V_{DIS}=V_{S2}−V_{M22}	2	0.4		0.6	V
V_{DIM}	Diode forward voltage	DIM	TIM : D, OUT : M, CLK : 22, V_{S2}=3V, I_{F20}=−10μA, V_{DIM}=V_{S2}−V_{M20}	2	0.4		0.6	V
V_{SWE}	Switch on voltage	SW 2, 4, 6	TIM : D, OUT : S, CLK : 20, V_{S9}=3V, V_{S2}=3V, I_{F22A}=0.5mA, I_{F22B}=−0.5mA, V_{SWE}=V_{M22}−V_{S2}	2	0.1		0.1	V
V_{SWO}	Switch on voltage	SW 1, 3, 5	TIM : D, OUT : S, CLK : 40, V_{S9}=3V, V_{S2}=3V, I_{F20A}=0.5mA, I_{F20B}=−0.5mA, V_{SWO}=V_{M20}−V_{S9}	2	−0.1		0.1	V
V_{ONS}	Switch on voltage	SW 7, SW 8	TIM : D, OUT : −, CLK : 48, n=21, 19, V_{S22}=V_{S20}=3.0V, I_{FnA}=0.5mA, I_{FnB}=−0.5mA, V_{ONS}=V_{Mn}−V_{S22}	2	−0.15		0.15	V

Continue to next page

ELECTRICAL CHARACTERISTICS (V_{CC}=7.0V, T_a=25℃, unless otherwise noted)

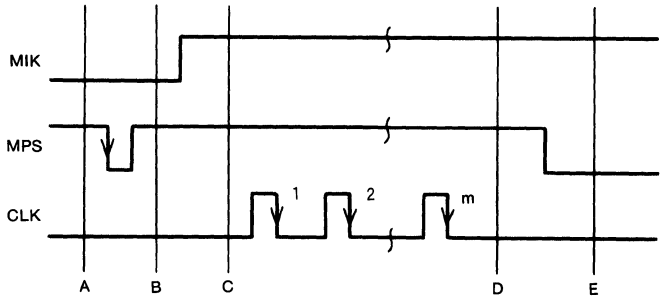
Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min	Typ*	Max	
R_{IX}	Output resistance	FXM	TIM : D, OUT : S, CLK : 4 $V_{S22}=V_{S21}=V_{S20}$=0.4V, V_{S19}=3V $I_{F18A}=-100\mu A$, $I_{F18B}=-200\mu A$ $R_{IX}=(V_{18A}-V_{M18B})/100\mu A$	2	1.1	1.5	1.9	kΩ
V_{OFX}	Output voltage	FXM	TIM : D, OUT : S, CLK : 4 $V_{S22}=V_{21}=V_{S20}$=0.4V, V_{S19}=3V $I_{F18}=-10\mu A$, $V_{OFX}=V_{M18}$	2	2.2		2.6	V
V_{TP}	Positive threshold voltage	CM 2	TIM : D, OUT : S, CLK : 4 $V_{S22}=V_{S20}$=0.4V, V_{S21}=3.00V V_{S10}=5V V_{TP} : V_{TP} is the value of V_{S19} when V_{S19} is gradually increased until $V_{M12}<5V$	2	3.05		3.20	V
V_{TN}	Negative threshold voltage	CM 2	Same as the test conditions for V_{TP}. V_{TN} : V_{TN} is the value of V_{S19} when V_{S19} is gradually decreased until $V_{M12}>5V$	2	2.85		3.00	V
V_{TW}	Hysteresis width	CM 2	$V_{TW}=V_{TP}-V_{TN}$	2	0.12	0.18	0.24	V
V_{OH}	High-level output voltage	OUS, OUM	TIM : A,17, 16 Measured when each output is high. $I_{Fn}=-10mA$, $V_{OL}=V_{Mn}$	2	5.8	6.1		V
V_{OL}	Low-level output voltage	OUS, OUM	TIM : A,n=17, 16 Measured when each output is low. I_{Fn}=10mA, $V_{OL}=V_{Mn}$	2		0.2	0.3	V
I_{ITS}	High-level input current	TSL	TIM : A V_{F15}=7V, $I_{ITS}=I_{M15}$	2	0.48	0.62	0.84	mA
V_{SOI}	High-level input current	OSI	Ceramic resonator : 1 MHz C_{O1}=68pF, C_{O2}=33pF Test probe : 10MΩ, 12pF	1	0.3	0.4	0.6	V_{PP}
V_{OSR}	Oscillation voltage	OSR	Same as test conditions for V_{OSI}	1	0.7	1.1	1.5	V_{PP}
f_{OSC}	Oscillation frequency	OSC	Ceramic resonator : 1 MHz C_{O1}=68pF, C_{O2}=33pF Insert a resistor of 10kΩ between MIK and V_{CC} and measure the output frequency f_{MIK} of MIK. $f_{OSC}=700f_{MIK}$	1	0.98	1	1.02	MHz

* : Typical values are at T_a=25℃

Testing Notes

Note 1 : V_{Sn} : Applied voltage at pin n
V_{Fn} : Applied voltage for current measurement at pin n
I_{Fn} : Applied voltage for voltage measurement at pin n
V_{Mn} : Measured voltage at pin n
I_{Mn} : Measured current at pin n
V_{F1} : Switch S1 is turned on and AMP is operated as a voltage follower.

Note 2 : Testing of some items requires that the internal IC logic be set in specific state. In this case, the state of timing TIM, output OUT and clock CLK signals must be specified.

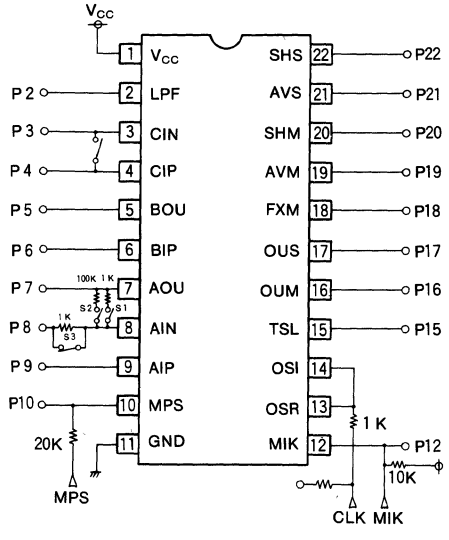


→ When MIK is low, output states of OUS and OUM are inverted by a negative pulse at MPS.

● For each signal, V_{IH}=open, V_{IL}=OV

- TIM : A~E
- OUT : S (Output OUS is set high)
  M (Output OUM is set high)
- CLK : m

TEST CIRCUIT (Test circuit 1 is shown as an application example.)



M54811P

PRESETTABLE TIMER/COUNTER WITH SEVEN SEGMENT LED DRIVER

DESCRIPTION

The M54811P is an I^2L semiconductor integrated circuit consisting of a two-digit decimal counter.

FEATURES

- Two-digit decimal counter
- Seven-segment LED display of count data
- Count start/stop control
- Digit expansion capability
- TTL compatible I/O

APPLICATION

Digital timer and general use in digital equipment.

FUNCTION

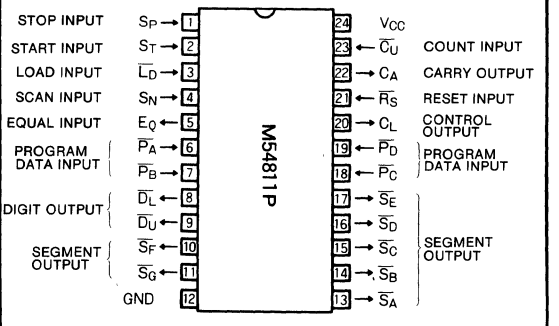
The M54811P consits of an internal-control flip flop, two-digit decimal counter, a seven-segment decoder, a driver, a latch, and a comparator, and is intended for digital timer applications.

The control flip flop is used to control the count ; the count is enabled when the flip flop is set by input S_T, and disabled when the flip flop is reset by input S_P. The "1" output state of this flip flop is indicated by the high C_L output.

While the count is enabled, the count is advanced by input C_U. Output C_A is a carry signal used to expand the number of counter digits. If is connected to the input C_U of the next stage counter.

The comparator compares the count (the contents of counter) against the program data loaded into the latch. If they match, the output E_Q changes to high.

PIN CONFIGURATION (TOP VIEW)



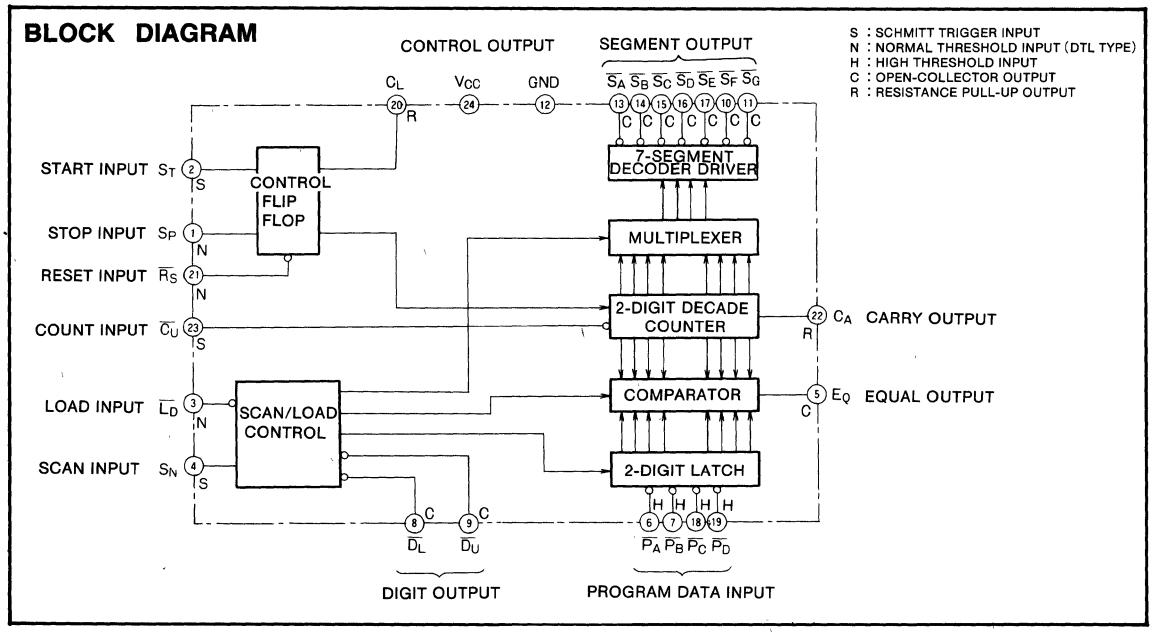
Outline 24P4

The program data applied at $\overline{P_A}-\overline{P_D}$ is loaded into the latch when L_D is set low. The state of S_N determines which digit is set.

Each digit of the count is output at $\overline{S_A}-\overline{S_G}$ allowing dynamic display on seven-segment LEDs by the multiplexer and segment decoder driver.

The scan/load controller loads the program data $\overline{P_A}-\overline{P_D}$ to the latch and switches digits of multiplexer. It has outputs $\overline{D_L}$ and $\overline{D_U}$ to switch the digits of program and count data.

BLOCK DIAGRAM



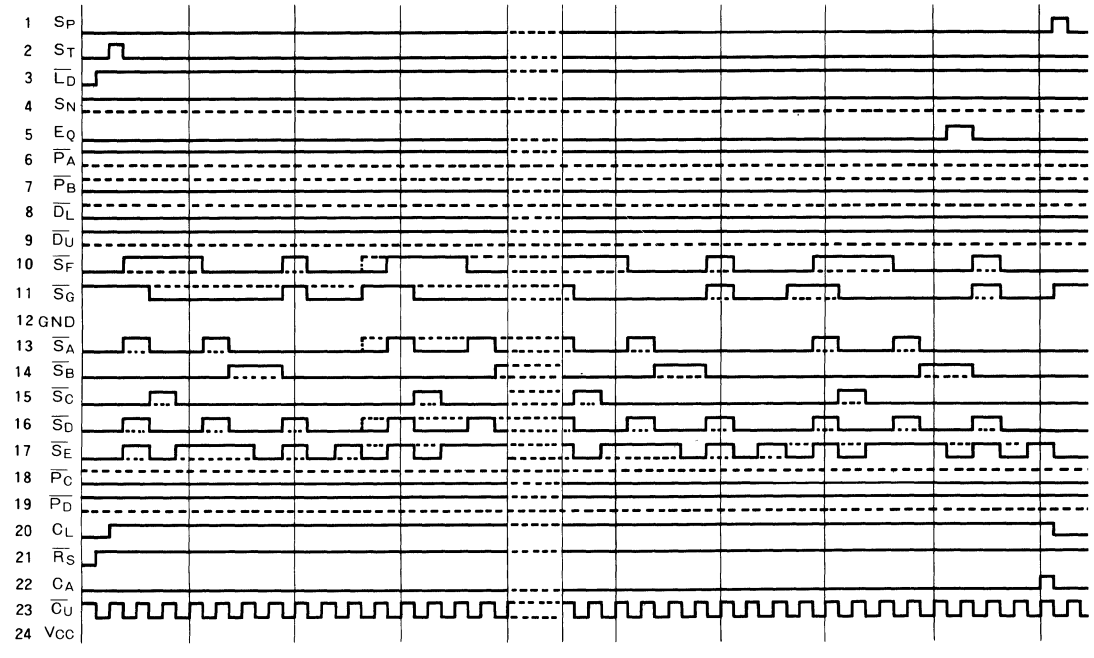
MITSUBISHI ELECTRIC

PRESETTABLE TIMER/COUNTER WITH SEVEN SEGMENT LED DRIVER

PIN NUMBER/FUNCTION

Symbol	Name	I/O	Function
S_T	Start	Input	The control flip flop is set and count enable when S_T is set high.
S_P	Stop	Input	The control flip flop is reset and count disable when S_P is set high This signal overrides S_T.
$\overline{R_S}$	Reset	Input	The control flip flop and counter are reset when $\overline{R_S}$ is set low. But this does not affect the latch contents.
C_L	Control	Output	This control output from external circuits corresponds to the "1" output of the control flip flop The count is enable while this output is high
$\overline{C_U}$	Count	Input	The count advances when the input changes from high to low with the count enabled
$\overline{S_A}$~$\overline{S_G}$	Segment	Output	The seven-segment drive output to display the counter contents When the ones-digit is selected by input S_N, the ones-digit drive signal is output , when the tens-digit is selected, the tens-digit drive signal is output. Low active output
C_A	Carry	Output	Carry output. When the number of digits is expanded, this output is connected to the input $\overline{C_U}$ ofthe next stage counter.
$\overline{P_A}$~$\overline{P_D}$	Program data	Input	Data input for comparing with the counter contents. When the ones-digit is selected by the input S_N, the ones-digit latch-data is input ; when the tens-digit is selected, the tens-digit latch-data is input. Low active BCD input.
$\overline{L_D}$	Load	Input	Program data $\overline{P_A}$—$\overline{P_D}$ are loaded to the ones or tens digit in accordance with the state of the S_N input when $\overline{L_D}$ is set low.
E_Q	Equal	Output	The comparator compares the counter contents to the data loaded into the latch If they match, E_Q becomes high. The comparator does not function while data is loaded
S_N	Scan	Input	Digit selection signal The ones-digit is selected when S_N is high, the tens-digit is selected when S_N is low. To set both digits, S_N should be set both high and low at least once while L_D is low.
$\overline{D_L}$, $\overline{D_U}$	Digit	Output	Output $\overline{D_L}$ becomes low when the ones-digit is selected by SN ; output $\overline{D_U}$ becomes low when the tens-digit is selected These signals are used for dynamic seven-segment display of the counter contents, and for digit synchronization switching when the program data is loaded.

OPERATING TIMING DIAGRAM



Remark : In this case, the preset value is 69

Note : The signal state is shown by solid lines when S_N is high, and by broken lines when S_N is low Signals (or time intervals) unrelated to the state of S_N are shown by solid lines only abbreviated sections are shown by broken lines.

PRESETTABLE TIMER/COUNTER WITH SEVEN SEGMENT LED DRIVER

ABSOLUTE MAXIMUM RATINGS (T_a=0～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
V_I	Input voltage		6	V
V_O	Output voltage	Output high	V_{CC}	V
Pd	Power dissipation		600	mW
Topr	Operating temperature		0～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0～+70℃, unless otherwise noted)

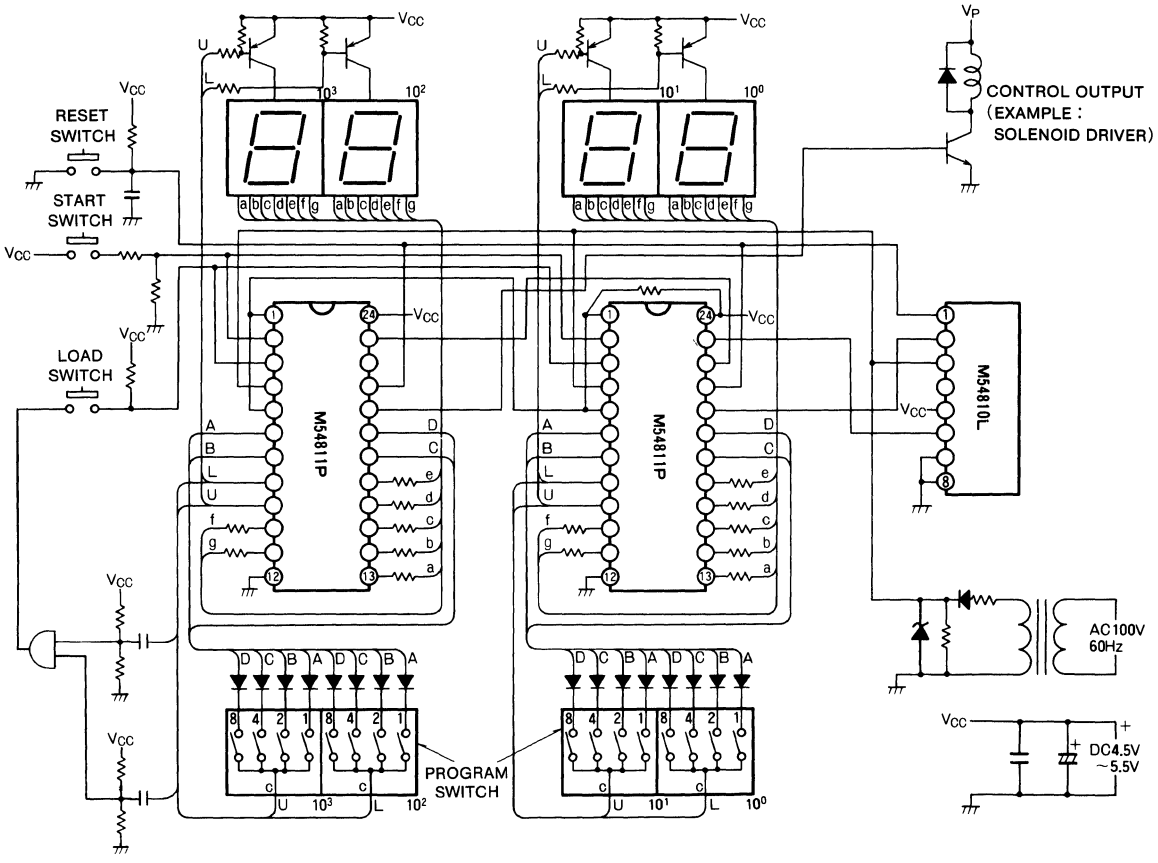
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage (except inputs $\overline{P_A}$–$\overline{P_D}$)	2.2			V
V_{IH}	High-level input voltage (inputs $\overline{P_A}$–$\overline{P_D}$)	2.8			V
V_{IL}	Low-level input voltage (except inputs $\overline{P_A}$–$\overline{P_D}$)			0.6	V
V_{IL}	Low-level input voltage (inputs $\overline{P_A}$–$\overline{P_D}$)			1.4	V
I_{OL}	Low-level output current (outputs C_L, C_A)			16	mA
I_{OL}	Low-level output current (except outputs C_L, C_A)			20	mA
f_C	Count frequency (input $\overline{C_U}$)			1	MHz
f_S	Scan frequency (input SN)			1	kHz
topr	Operating pulse width (inputs S_T, S_P, $\overline{L_D}$, $\overline{R_S}$)	500			ns

ELECTRICAL CHARACTERISTICS (T_a=0～+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5.5V			91	mA
I_{IL}	Low-level input current	V_{CC}=5.5V			−1.6	mA
I_{IH}	High-level input current (except inputs $\overline{P_A}$–$\overline{P_D}$)	V_{CC}=5.5V, V_I=2.4V			80	μA
I_{IH}	High-level input current (inputs $\overline{P_A}$–$\overline{P_D}$)	V_{CC}=5.5V, V_I=3V			80	μA
I_{IH}	High-level input current (except inputs $\overline{P_A}$–$\overline{P_D}$)	V_{CC}=5.5V, V_I=4.5V			120	μA
V_{T+}	Positive threshold voltage (inputs S_T, S_N, $\overline{C_U}$)	V_{CC}=5V	1.4		2.2	V
V_{T-}	Negative threshold voltage (inputs S_T, S_N, $\overline{C_U}$)	V_{CC}=5V	0.6		1.2	V
V_{OH}	High-level output voltage (outputs C_L, C_A)	V_{CC}=4.5V, I_{OH}=−400μA	3			V
I_{OH}	High-level output current (except outputs C_L, C_A)	V_{CC}=4.5V, V_O=6.5V			250	μA
V_{OL}	Low-level output voltage (outputs C_L, C_A)	V_{CC}=4.5V, I_{OL}=16mA			0.5	V
V_{OL}	Low-level output voltage (except C_L, C_A)	V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_{OS}	Output short circuit current (outputs C_L, C_A)	V_{CC}=5.5V, V_O=0V	−2.1		−3.7	mA

APPLICATION EXAMPLE

4-DIGIT DIGITAL TIMER (0-9999 MINUTES)



M54812L

1/4, 1/8, 1/32 DIVIDER/OSCILLATOR

DESCRIPTION

The M54812L is an I^2L semiconductor integrated circuit consisting of a quartz oscillator circuit and 1/32 divider circuit.

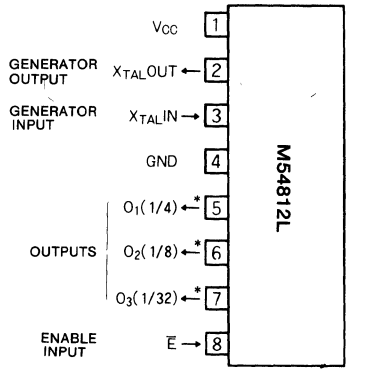
FEATURES

- Built-in quartz oscillator circuit
- Maximum operating frequency (f_{max}) = 4MHz
- Open collector TTL outputs
- Three divider outputs (1/4, 1/8, 1/32)
- Low operating voltage (V_{CC} = 2.3 ~ 5.5V)
- Lower power consumption (V_{CC} = 5.5V, I_{CC} = 6mA)

APPLICATION

General commercial equipment, for generating reference frequencies and for synchronization and frequency dividing.

PIN CONFIGURATION (TOP VIEW)



* : Open collector output

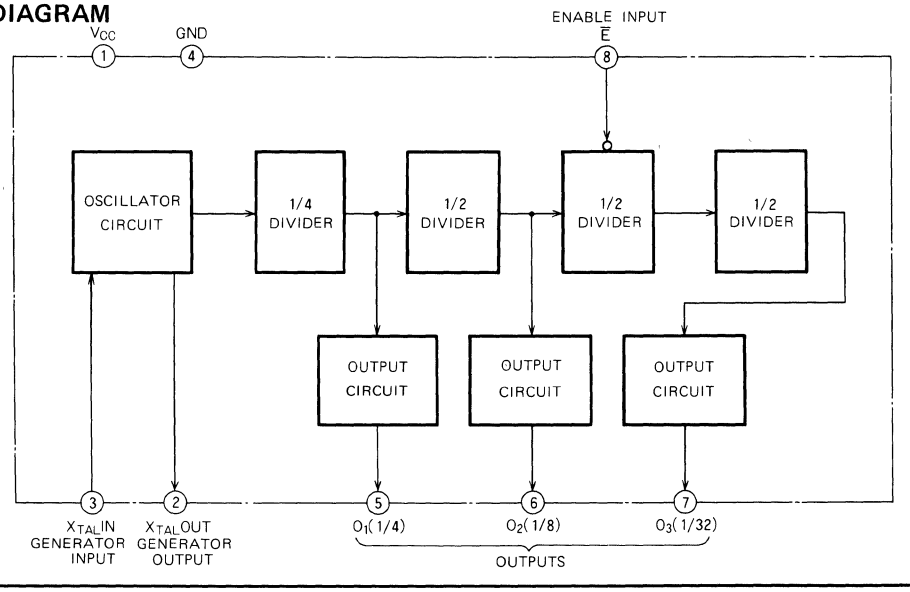
Outline 8P5

FUNCTION

The M54812L is designed as a reference frequency generator, and the oscillator circuit uses a quartz element that can be used at frequencies up to 4MHz, and there is a built-in frequency divider.

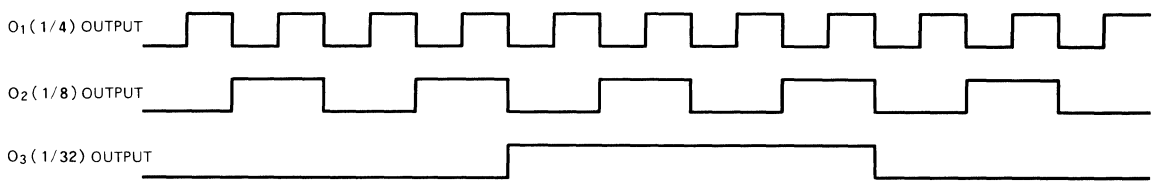
Three outputs are provided; 1/4, 1/8 and 1/32 of the oscillator frequency and the open-collector configuration ensures sink current of 1.6mA. The enable input ($\overline{E}$) is provided specifically for radio reception applications as a crystal frequency-marker generator using the 1/8 output, so that the 1/32 output can be disabled. If the $\overline{E}$ input is open, the 1/32 output is held at either low- or high-level. If the 1/32 output is to be used, then the $\overline{E}$ input must be low.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5 ~ +6.5	V
V_I	Input current	Pin 8	−0.5 ~ +6.5	V
V_O	Output voltage	Pins 5, 6, 7 (with high-level output)	6.5	V
T_{opr}	Operating temperature		−10 ~ +60	℃
T_{stg}	Storage temperature		−55 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2.3	3.5	5.5	V
I_{OL}	Low-level output current			1.6	mA

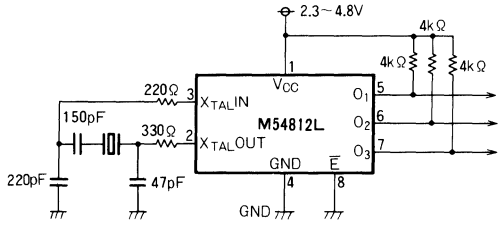
ELECTRICAL CHARACTERISTICS (T_a = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ*	Max	
I_{IL}	Low-level input current ($\overline{E}$ input)	V_{CC} = 5.5V, V_{IL} = 0.2V			−0.3	mA
V_{OL}	Low-level output voltage (O_1 ~ O_3 outputs)	V_{CC} = 2.3V, I_{OL} = 1.6mA			0.4	V
I_{OH}	High-level output current (O_1 ~ O_3 outputs)	V_{CC} = 2.3V, V_{OH} = 5.5V			100	μA
I_{CC}	Circuit current	V_{CC} = 5.5V, $X_{TAL}OUT$ = 0V		6	10	mA
f_{max}	Maximum operating frequency		4			MHz

* : A typical value is at T_a = 25℃

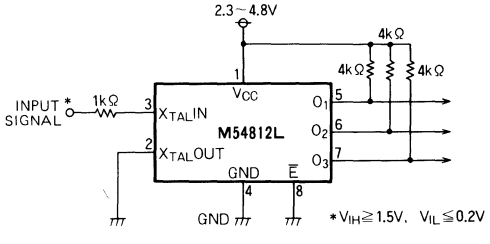
APPLICATION EXAMPLES

1. Quartz-crystal oscillator circuit



Quartz-crystal oscillator specifications, Effective resistance below 100Ω max
Load capacitance 32pF

2. Divider circuit



M54813L

1/4, 1/16, 1/32 DIVIDER/OSCILLATOR

DESCRIPTION

The M54813L is a semiconductor integrated circuit using I^2L technology, consisting of a quartz oscillator circuit and 1/32 divider circuit.

FEATURES

- Built-in quartz oscillator
- Maximum operating frequency, (f_{max}) = 4MHz
- Open collector TTL outputs
- Three divided outputs (1/4, 1/16, 1/32)
- Low supply voltage (V_{cc} = 2.3 ~ 5.5V)
- Low power consumption (V_{cc} = 5.5V, I_{cc} = 6mA)

APPLICATION

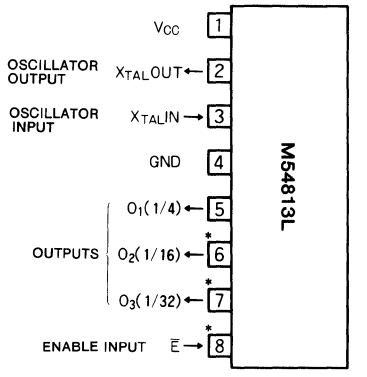
General consumer electronics, reference frequency generators, dividers.

FUNCTION

The M54813L is designed for use as a reference frequency generator, operating up to a frequency of 4MHz and incorporating a 1/32 divider circuit.

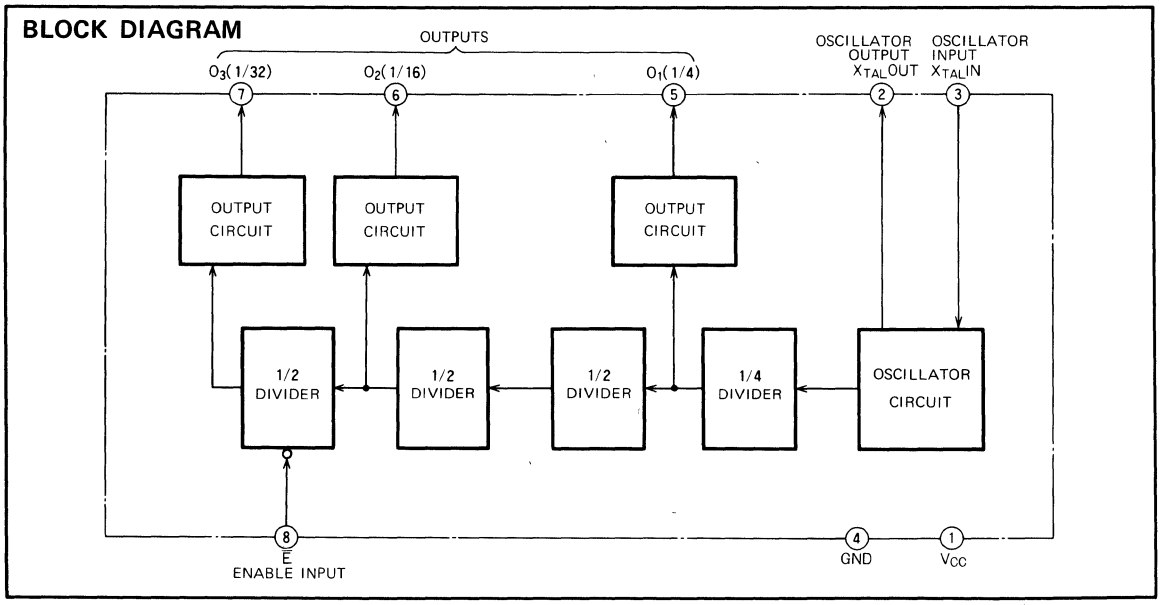
Three outputs are available, 1/4, 1/16, and 1/32 of the oscillator frequency. The outputs are open collector type capable of sinking 1.6mA each. For use of the 1/16 output in radio crystal marker generators, an enable input, $\overline{E}$, used to disable the 1/32 output is provided. When the $\overline{E}$ input is left open, the 1/32 output is fixed at either high- or low-level. To use the 1/32 output, the $\overline{E}$ input is grounded.

PIN CONFIGURATION (TOP VIEW)



Outline 8P5

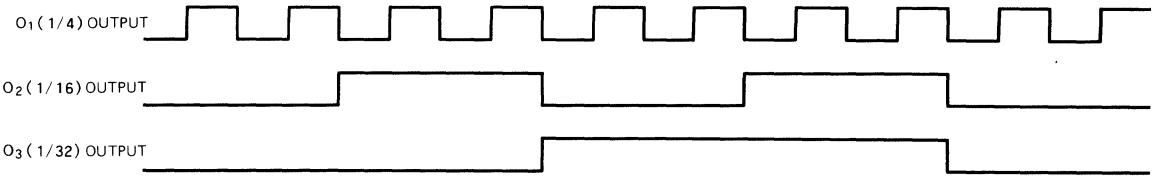
BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1/4, 1/16, 1/32 DIVIDER/OSCILLATOR

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5 ~ +6.5	V
V_I	Input voltage	Pin 8	−0.5 ~ +6.5	V
V_O	Output voltage	Pins 5, 6, 7 (with output high)	6.5	V
T_{opr}	Operating temperature		−10 ~ +60	℃
T_{stg}	Storage temperature		−55 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2.3	3.5	5.5	V
I_{OL}	Low-level output current			16	mA

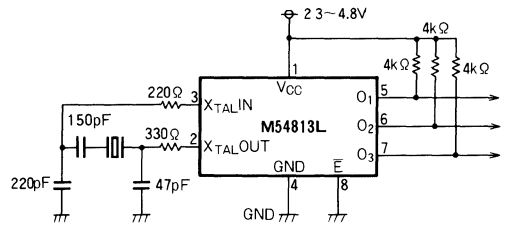
ELECTRICAL CHARACTERISTICS (Ta = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
I_{IL}	Low-level input current ($\overline{E}$ input)	V_{CC} = 5.5V, V_{IL} = 0.2V			−0.3	mA
V_{OL}	Low-level output voltage (O_1 ~ O_3 output)	V_{CC} = 2.3V, I_{OL} = 1.6mA			0.4	V
I_{OH}	High-level output current (O_1 ~ O_3 output)	V_{CC} = 2.3V, V_{OH} = 5.5V			100	μA
I_{CC}	Circuit current	V_{CC} = 5.5V, $X_{TAL}OUT$ = 0V		6	10	mA
f_{max}	Maximum operating frequency		4			MHz

* : A typical value is at T_a=25℃

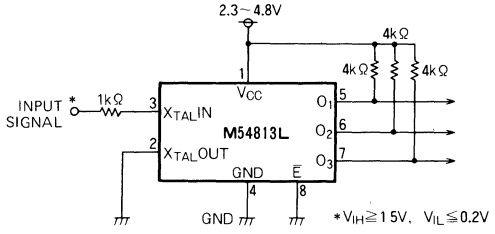
APPLICATION EXAMPLES

1. Quartz oscillator circuit



Crystal specifications effective resistance 100Ω, max.
load capacitance 32pF

2. Divider circuit



M54816P

14-STAGE DIVIDER/OSCILLATOR

DESCRIPTION

The M54816P is an I^2L semiconductor integrated circuit consisting of a 14-stages divider/oscillator designed for use as a general purpose divider circuit. It includes a quartz oscillator circuit and 14-stages of 1/2 divider circuits.

FEATURES

- Built-in quartz oscillator
- Maximum operating frequency f_{max} = 4.2MHz
- Open collector TTL outputs
- Eight divided outputs of frequency $1/2^N$ (N = 2, 8, 9, 10, 11, 12, 13, 14)
  In addition, the divided outputs of frequency $1/2^N$ can be chosen with any N values in the range 2 to 22.
- Reset function allows resetting of the N = 3 through 14 dividers (12 stages)
- Low power consumption (I_{CC} = 11mA for V_{CC} = 5.5V)

APPLICATION

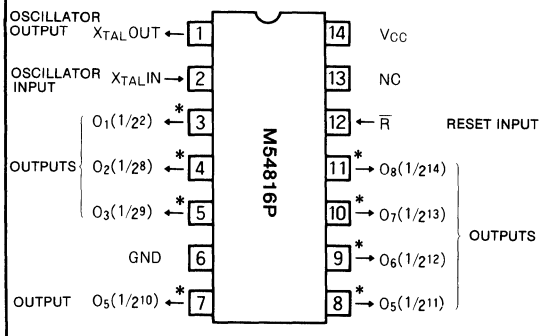
General consumer equipment (reference frequency generators, dividers)

FUNCTION

The M54816P is designed for use as a reference frequency oscillator. It operates at frequencies up to 4.2MHz using a crystal oscillator and consists of the oscillator circuit and 14 stages of divider circuits.

An internal regulated power supply provides good frequency stability with respect to power supply variations.

PIN CONFIGURATION (TOP VIEW)



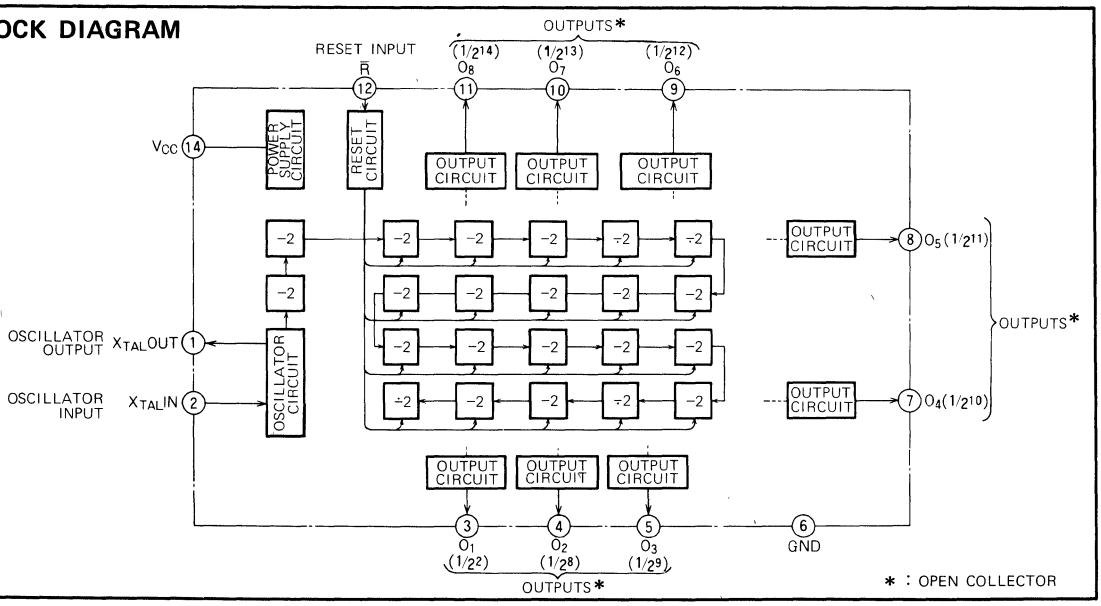
NC : No connection
* : Open collector

Outline 14P4

Eight divided outputs are available for frequencies $1/2^N$ (N = 2, 8, 9, 10, 11, 12, 13, and 14). The outputs are open collector and can sink up to 5mA each.

A reset function is provided so that when reset input R is set to low-level, all outputs except the $1/2^2$ output are reset to high output level. Setting the reset R high, cancels the reset function.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

14-STAGE DIVIDER/OSCILLATOR

ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +60℃, unlews otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.3 ~ +6.5	V
V_I	Input voltage	$\overline{R}$ reset input		−0.3 ~ +6.5	V
		$X_{TAL}IN$ oscillator input		−0.3 ~ +1	
V_O	Output voltage	$X_{TAL}OUT$ oscillator output		−0.3 ~ +1	V
		$O_1 \sim O_8$ outputs		−0.3 ~ +6.5	
T_{opr}	Operating temperature			−10 ~ +60	℃
T_{stg}	Storage temperature			−55 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
I_{OL}	Low-level output current			5	mA

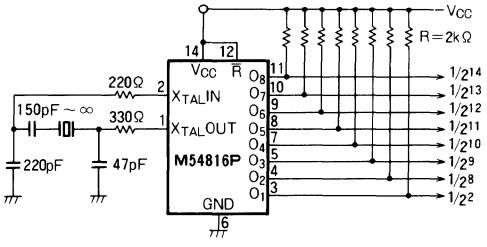
ELECTRICAL CHARACTERISTICS (Ta = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
I_{IH}	High-level input current ($\overline{R}$ input)	V_{CC}=5.5V, V_{IH}=5.5V			40	μA
I_{IL}	Low-level input current ($\overline{R}$ input)	V_{CC}=5.5V, V_{IL}=0.2V		−15	−100	μA
V_{OL}	Low-level output voltage ($O_1 \sim O_8$ outputs)	V_{CC}=4.5V, I_{OL}=5mA			0.4	V
I_{OH}	High-level output current ($O_1 \sim O_8$ outputs)	V_{CC}=4.5V, V_{OH}=6.5V			−100	μA
I_{CC}	Circuit current	V_{CC}=5.5V,	5	11	20	mA
f_{max}	Maximum operating frequency		4.2			MHz

* : Typical values are at T_a=25℃

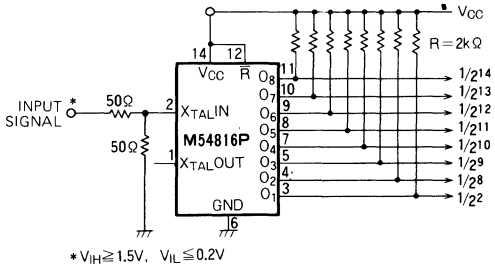
APPLICATION EXAMPLES

1. Quartz oscillator circuit



Crystal specifications
Reference frequency 4.2MHz
Effective resistance 100Ω, max
Load capacitance 32pF

2. Divider circuit



*$V_{IH} \geqq 1.5V$, $V_{IL} \leqq 0.2V$

M54819L

PRESETTABLE DIVIDER

DESCRIPTION

The M54819L is an I^2L semiconductor integrated circuit consisting of a divider circuit which provides seven types of frequency divide ratios.

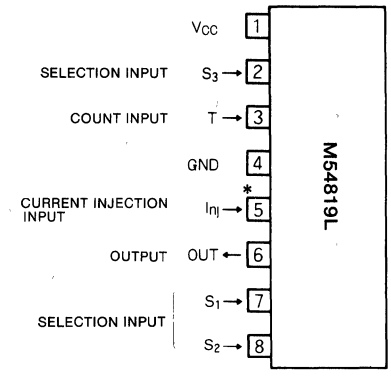
FEATURES

- Built-in regulated power supply
- Maximum operating frequency f_{max} = 3.0MHz
- Reset function
- Selectable divide ratio
  1/2, 1/4, 1/6, 1/8, 1/10, 1/12, or 1/16
- Wide supply voltage range (V_{CC} = 4.0 ~ 14.5V)
- Low power consumption (I_{CC} = 3mA for V_{CC} = 14.5V)

APPLICATION

General consumer equipment, frequency dividers

PIN CONFIGURATION (TOP VIEW)



* : Normally open

Outline 8P5

FUNCTION

The M54819L is designed for use as a general purpose frequency divider and consists of a regulated power supply, and dividers with divide ratios of 1/3, 1/5, and 1/16.

The output frequency division ratio is selectable and determined by a 3-input binary coded division ratio input. This allows the selection of one out of seven division ratios (1/2, 1/4, 1/6, 1/8, 1/10, 1/12, or 1/16). The output is a current source/sink type output capable of sourcing 100μA and sinking 1.6mA.

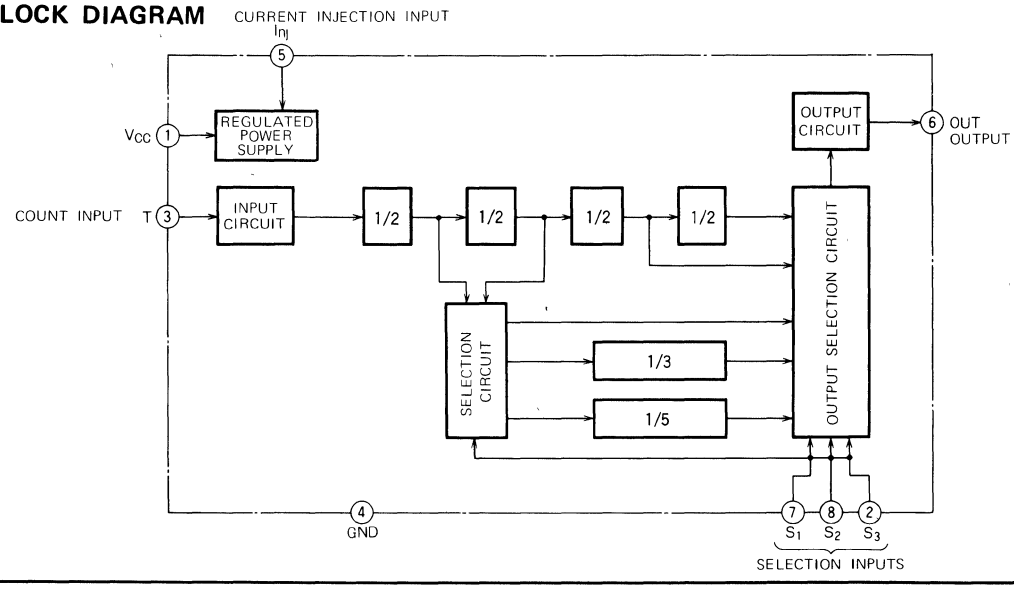
The built-in regulated power supply operates over a wide voltage range from 4.0 to 14.5V. A current injection input is provided to increase operating speed. By supplying this pin with current, the input count frequency can be raised to a maximum of 2MHz.

Resetting is accomplished by setting all the division ratio inputs to high-level, whereupon the internal divider circuits are cleared, the output going to low-level.

PRESETTABLE FUNCTION TABLE

Selection inputs	S_1	H	H	H	L	L	L	H	L
	S_2	H	L	H	H	H	L	L	L
	S_3	H	H	L	H	L	H	L	L
Output divide ratio		Reset	1/2	1/4	1/6	1/8	1/10	1/12	1/16

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			15	V
V_I	Input voltage	Count input T		4	V
		Selection inputs S_1, S_2, S_3		15	
V_O	Output voltage			6	V
T_{opr}	Operating temperature			−20 ~ +75	℃
T_{stg}	Storage temperature			−55 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4		14.5	V
I_{OL}	Low-level output current			1.6	mA

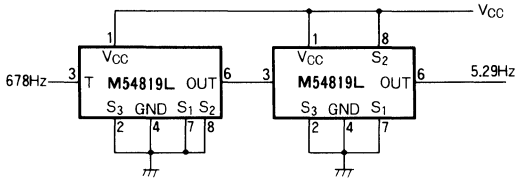
ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage	Count input T		0.9			V
		Selection inputs S_1, S_2, S_3		2			
V_{IL}	Low-level input voltage	Count input T				0.3	V
		Selection inputs S_1, S_2, S_3				0.6	
V_{OH}	High-level output voltage		V_{CC}=7V, I_{OH}=−0.1mA	2.4			V
			V_{CC}=4V, I_{OH}=−0.1mA	0.8			
V_{OL}	Low-level output voltage		V_{CC}=7V, I_{OL}=1.6mA			0.4	V
I_{IH}	High-level input current	Count input T	V_{CC}=14.5V, V_I=1V			1.5	mA
		Selection inputs S_1, S_2, S_3	V_{CC}=14.5V, V_I=14.5V			100	μA
I_{IL}	Low-level input current	Count input T	V_{CC}=14.5V, V_I=0.2V			−10	μA
		Selection inputs S_1, S_2, S_3	V_{CC}=14.5V, V_I=0V			−100	
I_{OS}	Output short-circuit current		V_{CC}=14.5V, V_O=0V	−0.1		−1	mA
I_{CC}	Circuit current		V_{CC}=14.5V, V_I=V_{CC} (pins 2, 7, 8)		3	5	mA

* : A typical value is at T_a=25℃.

APPLICATION EXAMPLE

Capstan motor control application (1/128 divider)



M54820P

FREQUENCY COUNTER WITH 5-DIGIT LED DRIVER

DESCRIPTION

The M54280P is an I^2L semiconductor integrated circuit consisting of a frequency counter and a 5-digit LED driver, for use in driving 7-segment LED display elements.

FEATURES

- Direct drive of a 5-digit common-anode type 7-segment LED display
- Presetting of the first IF frequency of a double superheterodyne receiver
- Built-in zero suppression
- Low power dissipation (I_{CC} = 38mA for V_{CC} = 5V)

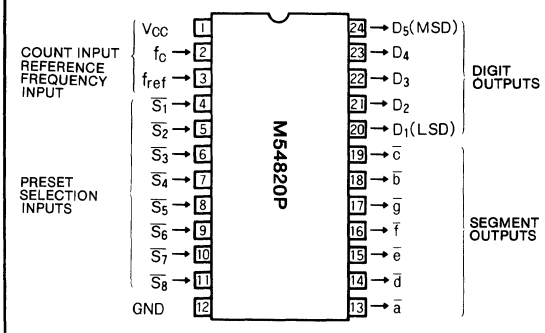
APPLICATION

Received frequency display for shortwave receivers, instrumentation frequency counters.

FUNCTION

The M54820P is a frequency counter capable of displaying the received frequency for a shortwave broadcast in units of 1kHz. The receiver first IF frequency can be preset, allowing direct reading of the received frequency in five digits by counting the local oscillator frequency. The circuit is designed to drive a 5-digit 7-segment commonanode LED display. The M54820P can be used as a conventional frequency counter as well.

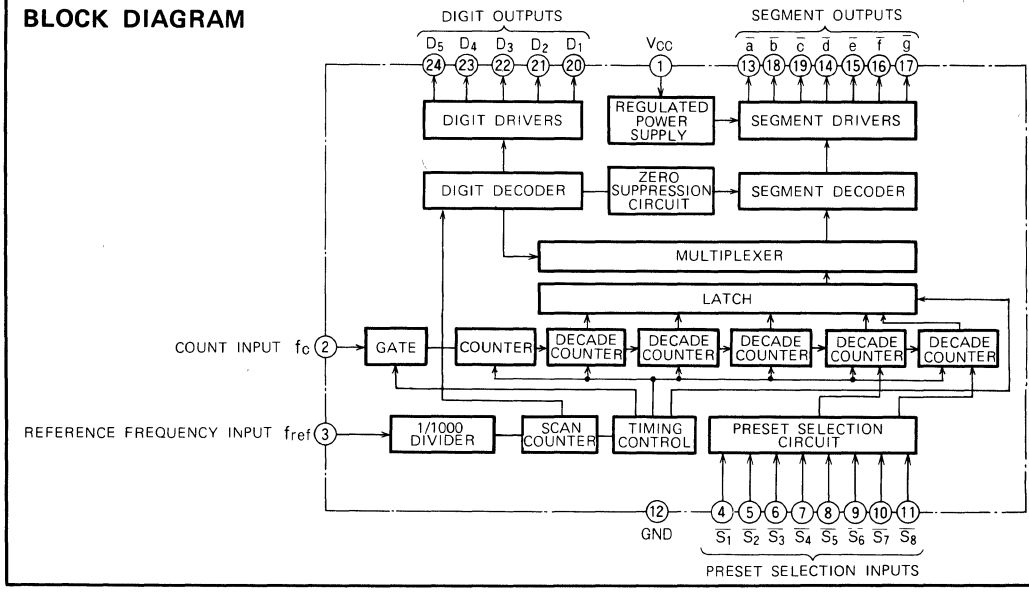
PIN CONFIGURATION (TOP VIEW)



Outline 24P4

For use as a frequency counter, the external circuit required consists of a reference generator IC (M54812L), a prescaler circuit (M53290P), and five 2SC1210 digit-drive transistors. This circuit, in combination with a 5-digit, 7-segment common anode LED display, completes the frequency counter.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FREQUENCY COUNTER WITH 5-DIGIT LED DRIVER

DESCRIPTION OF OPERATION

The following is an operational description of the M54820P frequency counter.

- **Maximum operating frequency**

  The count input (f_c) can accept a measurement frequency of up to 2.5MHz.

  The input signal however, is a TTL level rectangular wave, the duty cycle of which must be approximately 50% when approaching this maximum operating frequency.

- **Reference frequency (f_{ref}) and prescaler.**

  The reference frequency is a TTL level rectangular signal of 1MHz. To extend the frequency counting range of the circuit a prescaler can be used in which case the reference frequency can be made 1.25MHz or 0.625MHz depending upon the prescaler division ratio. The reference frequency is divided and provides the necessary control signals for the entire circuit.

  The counting accuracy is determined by the accuracy of the reference frequency. Therefore, a highly stable source such as a quartz oscillator must be used. For example, when the input frequency f_c is 2.5 MHz, 40ppm deviation of reference frequency will cause an error of ±1 count in the least significant digit (1ppm = 10^{-6}).

- **Preset Values**

  As shown in table 2, nine types of preset values can be selected from. In addition, by presetting the value of zero, the M54820P can be used as a conventional frequency counter.

- **Gate Time**

  The count input signal is counted only while the gate is opened. After counting, the counted value is latched, and the value held until the next count is finished. The time required for the gate time and counting operation for various reference frequencies is shown in table 3.

Table 1 Relationship of reference frequency and prescaler

Reference frequency (f_{ref})	Prescaler	Frequency measurement range (note 1)
1MHz	No	0.1kHz~2.5MHz
	1/10	1kHz~ 25MHz
	1/100	10kHz~250MHz
1.25MHz	1/8	1kHz~ 20MHz
	1/80	10kHz~200MHz
0.625MHz	1/16	1kHz~ 40MHz
	1/160	10kHz~400MHz

Note 1 The measured frequency indicates the prescaler input frequency
The frequency lower limit indicates that frequency at which borrow occurs for the last digit of the five digit display

- **LED Drive Method**

  Dynamic LED drive is provided with a repetition rate of 200Hz.

Table 2 Preset values

Preset selection inputs (note 2)								Preset values (note 3)
$\overline{S_1}$	$\overline{S_2}$	$\overline{S_3}$	$\overline{S_4}$	$\overline{S_5}$	$\overline{S_6}$	$\overline{S_7}$	$\overline{S_8}$	
H	H	H	H	H	H	H	H	0
H	H	H	H	H	H	H	L	−2MHz
H	H	H	H	H	H	L	H	2MHz
H	H	H	H	H	L	H	H	6MHz
H	H	H	H	L	H	H	H	10MHz
H	H	H	L	H	H	H	H	14MHz
H	H	L	H	H	H	H	H	18MHz
H	L	H	H	H	H	H	H	22MHz
L	H	H	H	H	H	H	H	45MHz

Note 2 H Open
L GND
3 Corresponds to a display least significant digit of 1kHz

Table 3 Gate time and count operation repetition frequency

Reference frequency (f_{ref})	Gate time	Count operation repetition frequency
0.625MHz	160ms	3.125Hz
1MHz	100ms	5Hz
1.25MHz	80ms	6.25Hz

Fig.1 Display element configuration

Unnecessary zeroes in the upper digits are suppressed by an internal zero suppression circuit. In addition, rounding is used to insure that the last digit does not vary wildly.

The M54820P is intended to drive a common-anode type LED display as shown in Fig. 1.

The segment and digit outputs do not require current limiting resistors.

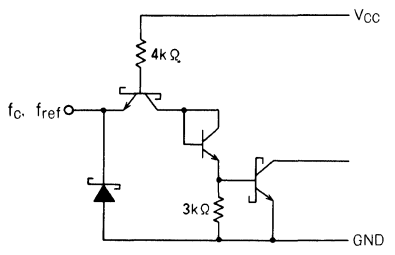
PRECAUTIONS FOR USE

1. The dynamic display system may generate noise so care should be taken in this regard.
2. To set the high-level condition for preset selection inputs S_1 through S_8, these inputs can be left open. Direct application of exaessive voltage to the IC can cause damage.

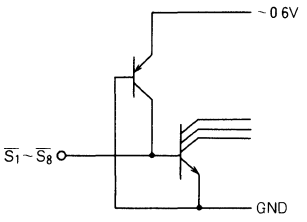
FREQUENCY COUNTER WITH 5-DIGIT LED DRIVER

INPUT/OUTPUT CIRCUITS

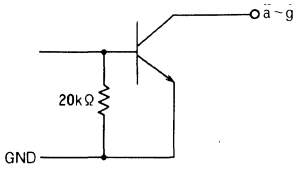
f_C, f_{ref} inputs



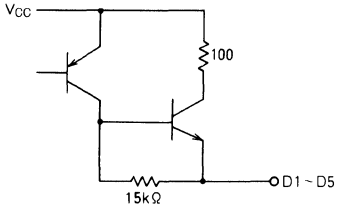
Preset selection inputs



Segment outputs



Digit outputs



ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5 ~ +6.5	V
V_I	Input voltage	Pins 2 and 3		−1.2 ~ +5.5	V
		Pins 4 through 11		−0.5 ~ +1	
V_O	Output voltage			V_{CC}	V
Pd	Power dissipation			600	mW
Topr	Operating temperature			−10 ~ +60	℃
Tstg	Storage temperature			−55 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
f_C	Count frequency	0		2.5	MHz
f_{ref}	Reference frequency	0.5	1.0	1.5	MHz
Duty	Input duty cycle (Pins 2 and 3, f = f(max))	45	50	55	%

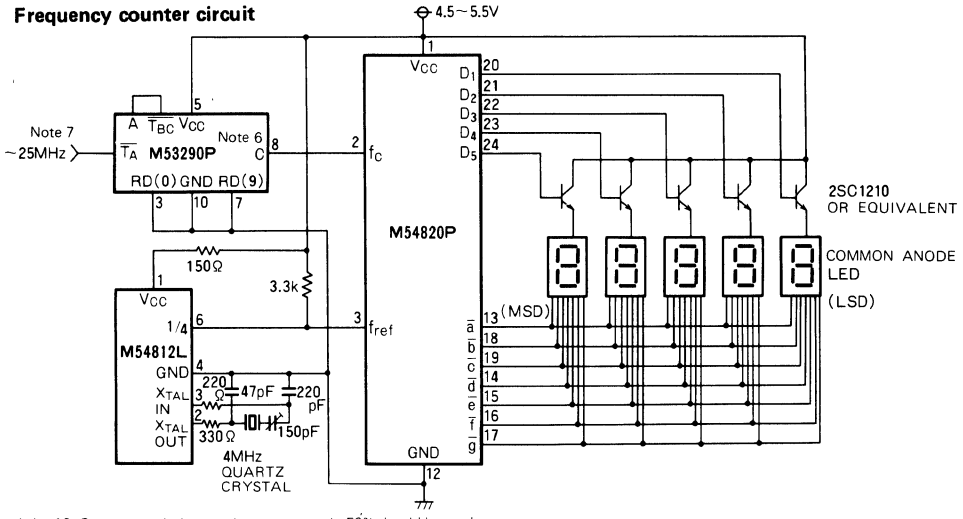
ELECTRICAL CHARACTERISTICS (T_a = −10 ~ +60℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit	Test circuit
V_{IH}	High-level input voltage			2			V	2 · 3
		(Note 4)		0.9		1		4 ~ 11
V_{IL}	Low-level input voltage					0.7	V	2 · 3
				0		0.2		4 ~ 11
I_{IH1}	High-level input current	V_{CC} = 5.5V	V_I = 2.4V			50	μA	2 · 3
I_{IH2}			V_I = 4.5V			80	μA	
I_{IL}	Low-level input current	V_{CC} = 5.5V	V_I = 0.4V			−2	mA	2 · 3
			V_I = 0.1V			−0.1		4 ~ 11
Iseg	Segment current	V_{CC} = 4.5 ~ 5.5V, V_O = 1 ~ 3V		12	20	30	mA	13 ~ 19
Idig	Digit current	V_{CC} = 4.5V, V_O = 3V		−3			mA	20 ~ 24
I_{CC}	Circuit current	V_{CC} = 5.5V (Note 5)			38	60	mA	1

Note 4 : Pins 4 through 11 may be left open for high-level conditions
5 : Apply 1 V to pins 13 through 19
6 : Typical values are at T_a=25℃

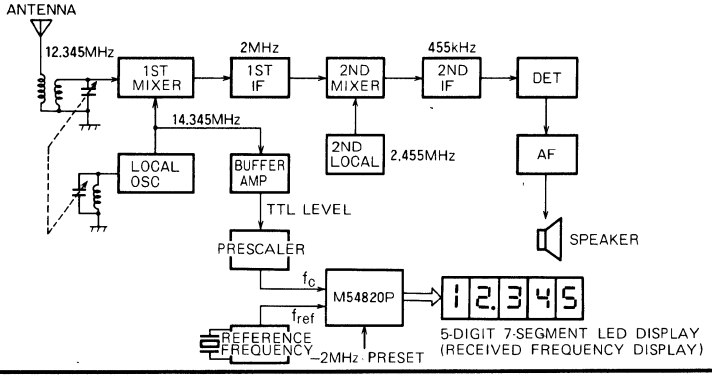
APPLICAITON EXAMPLES

(1) Frequency counter circuit



Note 6: Divide by 10 C output with duty cycle approximately 50% should be used
7: Reference frequency (f_{ref}) = 0.625MHz, using a 74LS93 (1/16 divider) up to 40MHz may be input with a reference frequency (f_{ref}) = 1.25MHz and a M54451P (1/8, 1/80 divider) as a prescaler, the range from 20MHz to 135MHz can be covered

(2) Radio receiver



M54832P

8-CHANNEL SELECTOR

DESCRIPTION

The M54832P channel selector is an I^2L integrated circuit capable of directly selection 8 channels and of continuous selection in both the up and down directions.

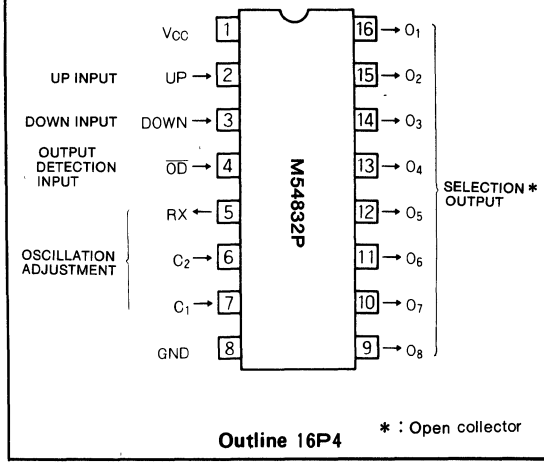
FEATURES

- Channel selection with soft fingertip touch switches
- Direct selection possible
- Continuous selection in up and down directions
- Preset selection possible
- Selection display with direct LED drive
- Wide operating voltage range (V_{CC} = 3.5~6V)
- Low current operation (I_{CC} = 4mA, V_{CC} = 6V)
- Built-in RC oscillator

APPLICATION

Radio and TV selection units; tape recorders, electric fans, microwave ovens and other multiple input units; general consumer equipment and appliances.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

* : Open collector

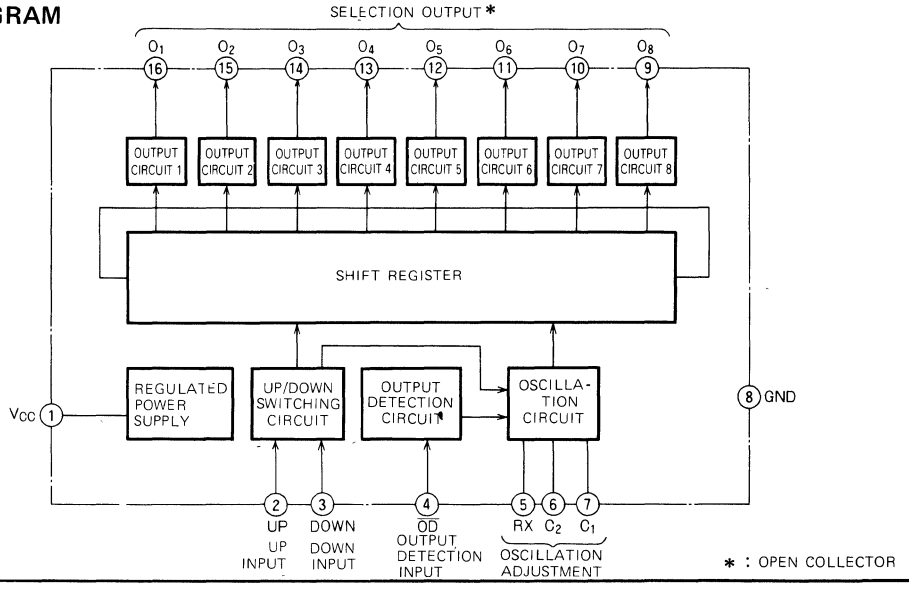
FUNCTION

The M54832P is a channel selector IC with a built-in RC oscillator circuit, serving for 8-channel direct selection and up/down selection.

When the fixed channel (O_1 output) is selected when the power has been switched on and when the up or down switch has been set to on, the on state of one output only among the outputs for the 8 channels can be moved continuously in the up or down direction in accordance to the switch which is on. When both the up and down switches are set to on, there is no channel shift and no up/down select operation. The speed of the up/down select operation can be set by the values of externally mounted RC oscillation circuit resistor (R_X) and capacitors (C_1 + C_2). This speed is 1/64th of the RC oscillation circuit's period.

Channels can be selected directly in an instant by setting the switch connected to the output detection circuit and output pin for the channel which is about to be selected in to on. For this case the select speed is set by the values of the oscillation circuit resistor (R_X) and capacitor (C_1).

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		8	V
V_I	Input voltage		6	V
V_O	Output voltage		12	V
T_{opr}	Operating temperature		−10 ~ +75	℃
T_{stg}	Storage temperature		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	3.5	4.5	6	V
V_{OH}	High-level output voltage			12	V
I_{OL}	Low-level output current			20	mA

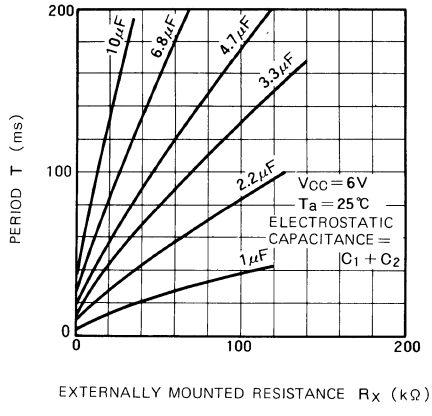
ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	Up, Down input		3		6	V
		$\overline{OD}$ input		3		12	
I_{OH}	High-level output current		V_{CC}=3.5V, V_O=12V			25	μA
V_{OL}	Low-level output voltage		V_{CC}=3.5V, I_{OL}=20mA			0.5	V
V_{IL}	Low-level input voltage	$\overline{OD}$ input	V_{CC}=6V,	0		0.5	V
I_{IH}	High-level input current	Up, Down	V_{CC}=6V, V_I=3V			400	μA
		$\overline{OD}$ input	V_{CC}=6V, V_I=3V			2	mA
I_{CC}	Circuit current		Excluding output current, V_{CC}=6V, input OFF	2	4	6	mA
f_{osc}	Oscillation frequency		V_{CC}=6V (Note 1)	−	60	+	Hz
f_{osc}	Oscillation frequency		(Note 1)	−	100	+	kHz

Note 1 Typical values are with R_X = 51kΩ, C_2 = 0.7μF, C_1 = 330pF

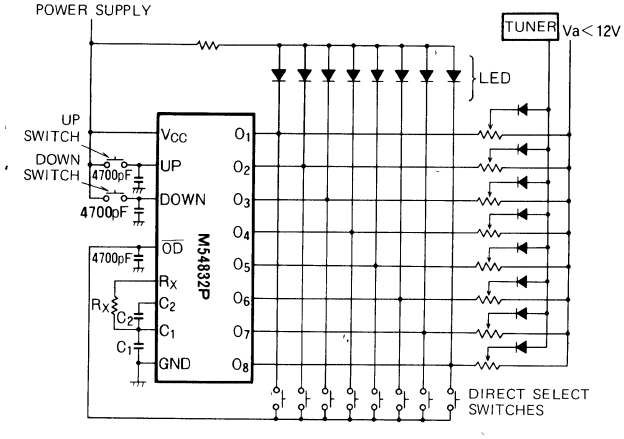
TYPICAL CHARACTERSITICS

OSCILLATION CHARACTERISTICS



APPLICATION EXAMPLE

8-channel selector



M54833P

8-CHANNEL SELECTOR WITH CLOCK OUT

DESCRIPTION

The M54833P is a semiconductor integrated circuit consisting of an I^2L channel selector capable of direct or up/down selection of 8 channels.

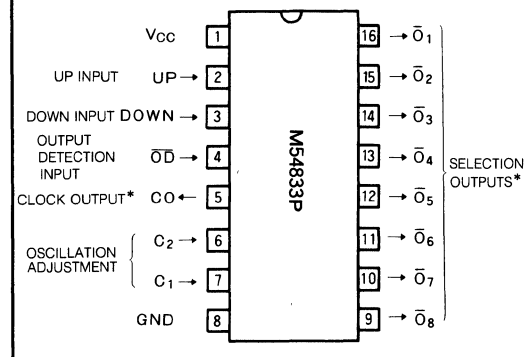
FEATURES

- Channel selection by soft-touch switches
- Direct selection capability
- Sequential up/down selection
- Presettable
- Selection display with direct LED driver
- Wide operating voltage range (V_{CC}=3.5–6V)
- Low current operation (I_{CC}=4mA, V_{CC}=6V)
- Built-in RC oscillator

APPLICATION

Radio and TV channel selectors, tape recorders, electric fans, microwave ovens and other multiple input equipment; general consumer equipment and appliances

PIN CONFIGURATION (TOP VIEW)



* : Open collector output

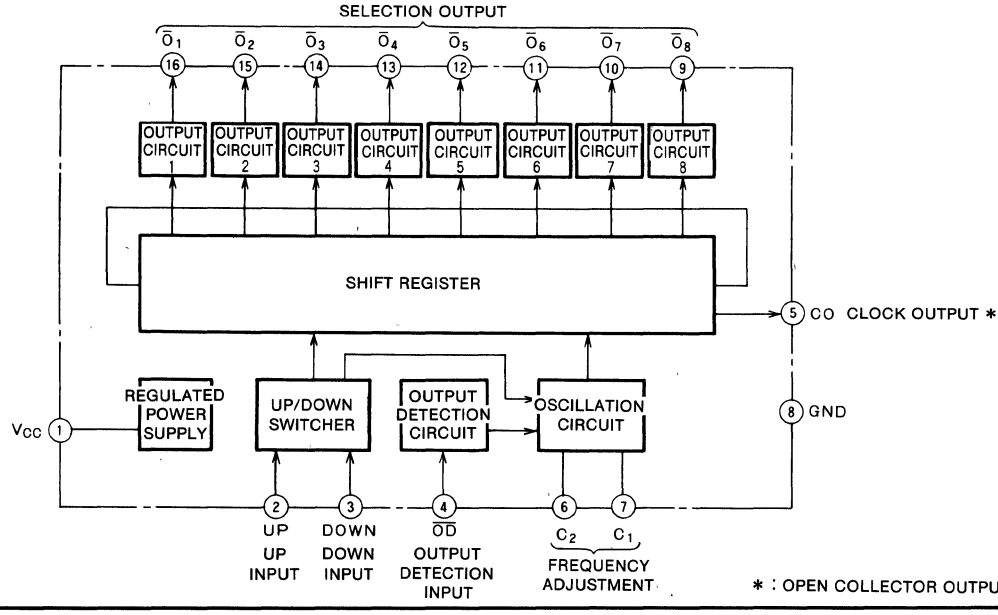
Outline 16P4

FUNCTION

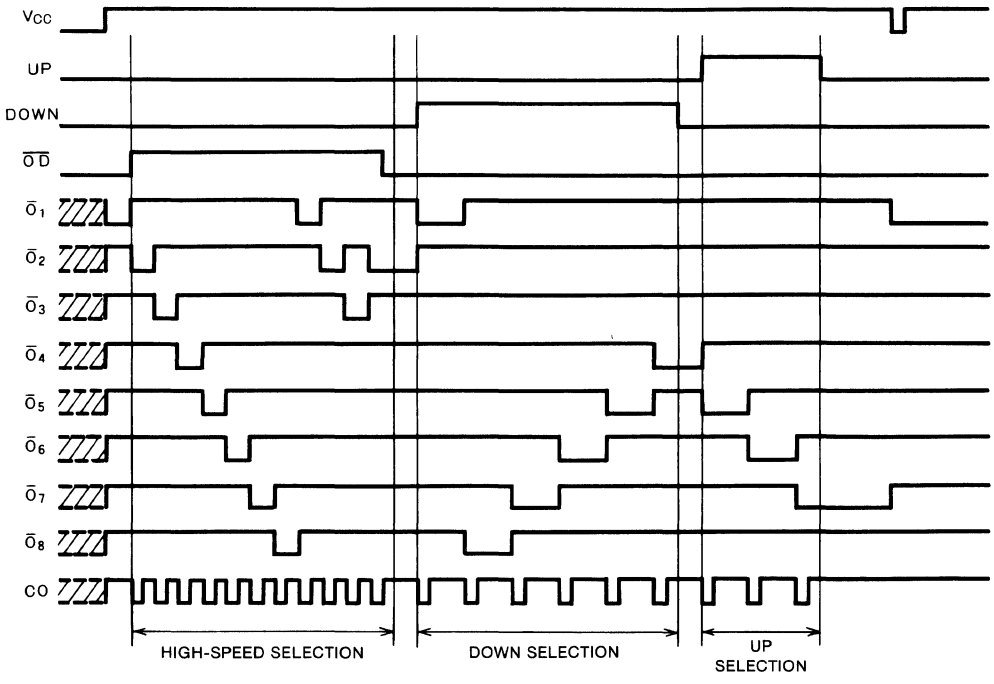
The M54833P is a channel selector IC with a built-in RC oscillator. It is capable of 8 channel direct and up/down selection.

When the power is turned on, output $\overline{O_1}$ is selected. When the up or down switch is closed, the on state output is sequentially transferred either up or down. When both up and down switches are closed, no channel transfer occurs. The speed of the up/down transfer is determined by the externally connected capacitance (C_1+C_2) in the RC oscillator. The transfer speed is 1/64 the period of the RC oscillator. Channels can be directly selected by closing a switch between the the desired output pin and the output detector input. The selection speed is determind by capacitance (C_1) in the oscillator circuit. The pulses at the clock output (CO) are in sync with the movement of output selection.

BLOCK DIAGRAM



OPERATIONAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=40~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		8	V
V_I	Input voltage		6	V
V_O	Output voltage		12	V
Topr	Operating temperature		10~+75	℃
Tstg	Storage temperature		−55~+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=10~+75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	3.5	4.5	6	V
V_{OH}	High-level output voltage			12	V
I_{OL}	Low-level output current			20	mA

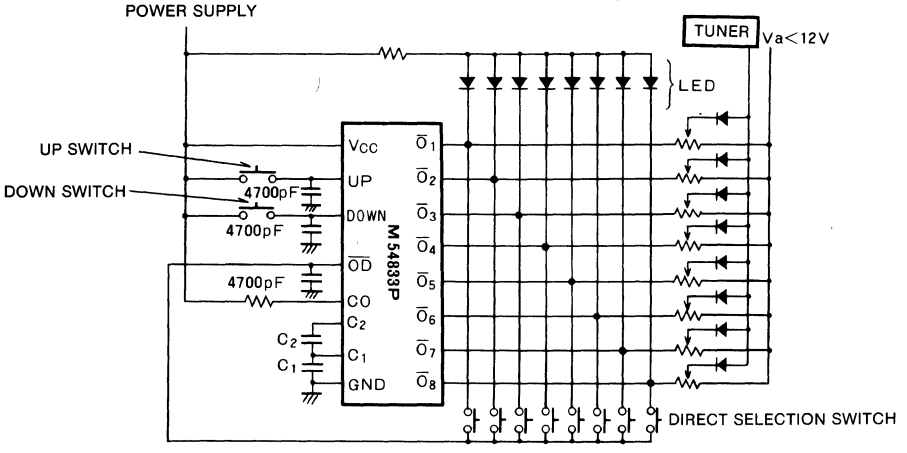
ELECTRICAL CHARACTERISTICS (T_a=−25℃, unless otherwise noted)

Symbol	Parameter		Test condition	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	Up, down inputs		3		6	V
		$\overline{OD}$ input		3		12	
I_{OH}	High-level output current		V_{CC}=3.5V, V_O=12V			25	μA
V_{OL}	Low-level output voltage		V_{CC}=3.5V, I_{OL}=20mA			0.5	V
V_{IL}	Low-level input voltage	$\overline{OD}$ input	V_{CC}=6V	0		0.5	V
I_{IH}	High-level input current	Up, down input	V_{CC}=6V, V_I=3V			400	μA
		$\overline{OD}$ input	V_{CC}=6V, V_I=3V			2	mA
I_{CC}	Supply current		Excluding output current, V_{CC}=6V, input off	2	4	6	mA
f_{OSC}	Oscillation frequency		V_{CC}=6V (Note 1)	—	60	+	Hz
f_{OSC}	Oscillation frequency		(Note 1)	—	100	+	kHz

Note 1. Typical values are with R_X=51kΩ, C_2=0.7μF, C_1=330pF.

APPLICATION EXAMPLE

8-channel selector



M54834P

14-CHANNEL SELECTOR

DESCRIPTION

The M54834P is an I^2L semiconductor integrated circuit consisting of a 14-channels selector capable of directly tuning 14-channels and of continuous tuning in both the up and down directions.

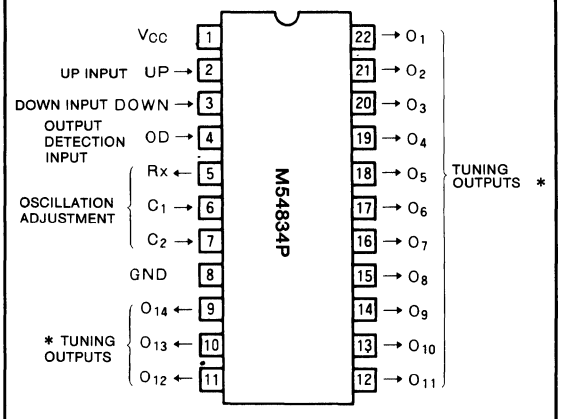
FEATURES

- Channel tuning with soft fingertip touch switches
- Direct tuning possible
- Continuous tuning in up and down directions
- Preset tuning possible
- Tuning display with direct LED drive
- Wide operating voltage range (V_{CC} = 4.0 ~ 6.0V)
- Low current operation (I_{CC} = 8mA, for V_{CC} = 6V)
- Built-in RC oscillator

APPLICATION

Radio and TV tuning units; tape recorders, electric fans, microwave ovens and other multiple input units; general consumer equipment and appliances.

PIN CONFIGURATION (TOP VIEW)



* : Open collector output

Outline 22P4

FUNCTION

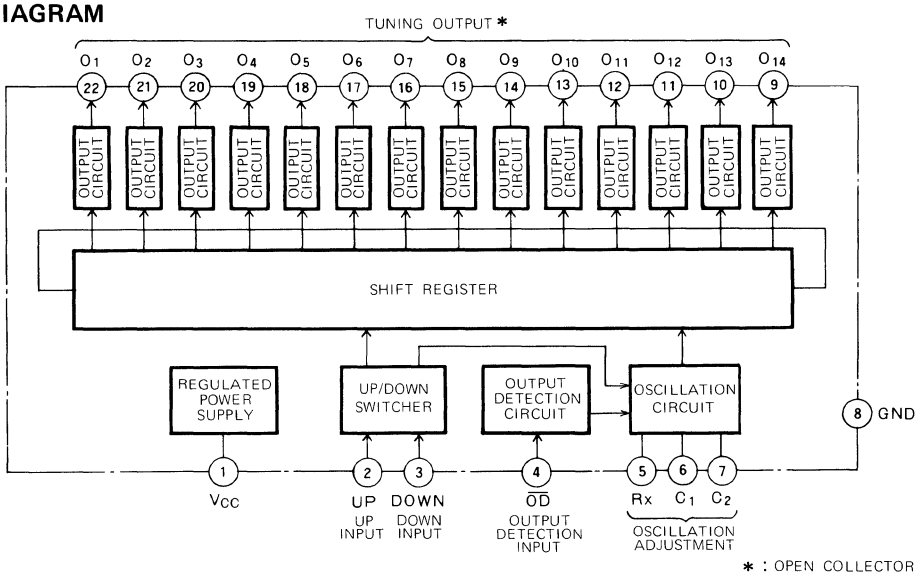
The M54834P is a channel selector IC with a built-in RC oscillator circuit, serving for 14-channels direct tuning and up/down tuning.

When the fixed channel (O_1 output) is tuned in when the power has been switched on and when the up or down switch has been set to on, the on-state of one output only among the outputs for the 14-channels can be moved continuously in the up or down direction in accordance with the switch which is on. When both the up and down switches are set to on, there is no channel shift and no up/down tuning operation.

The speed of the up/down tuning operation can be set by the values of externally mounted RC oscillation circuit resistor (R_X) and capacitors (C_1 + C_2). This speed is 1/64th of the RC oscillation circuit's period.

Channels can be tuned in directly in an instant by setting the switch connected to the output detection circuit and output pin for the channel which is about to be tuned in to on. For this operation, the tuning speed is set by the values of the oscillation circuit resistor (R_X) and capacitor (C_1).

BLOCK DIAGRAM



* : OPEN COLLECTOR OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = −10~+60°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage (UP, DOWN input pins)		6	V
V_O	Output voltage		12	V
Topr	Operating temperature		−10~+60	°C
Tstg	Storage temperature		−55~+125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −10~+60°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4	5	6	V
V_O	Output voltage (when power transistor is OFF)			12	V
I_{OL}	Low-level output voltage			25	mA

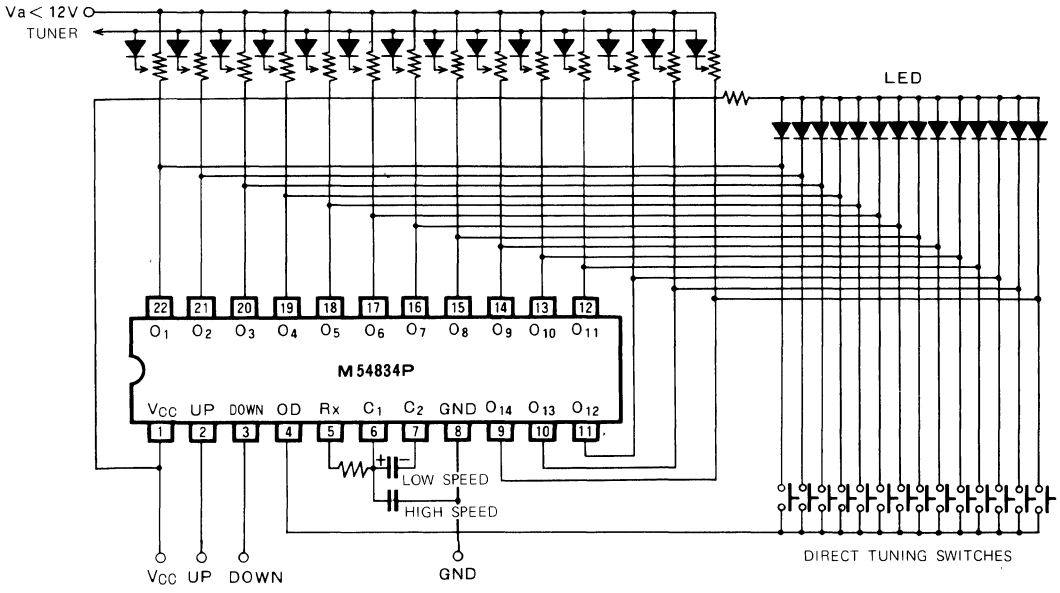
ELECTRICAL CHARACTERISTICS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage	UP, DOWN inputs		3		6	V
		$\overline{OD}$ input		3		12	
I_{OH}	High-level output current		V_{CC}=3V, V_C=12V			25	μA
V_{OL}	Low-level output voltage		V_{CC}=3V, I_{OL}=25mA			0.45	V
V_{IL}	Low-level input voltage	$\overline{OD}$ input	V_{CC}=6V,	0		0.5	V
I_{IH}	High-level input current	UP, DOWN inputs	V_{CC}=6V, V_I=3V			400	μA
		$\overline{OD}$ input	V_{CC}=6V, V_I=3V			2	mA
I_{CC}	Circuit current		Not including output current V_{CC}=6V, input OFF	3	8	15	mA
f_{OSC}	Oscillation frequency		V_{CC}=6V (Note 1)	−	60	+	Hz
f_{OSC}	Oscillation frequency		V_{CC}=6V (Note 1)	−	100	+	kHz

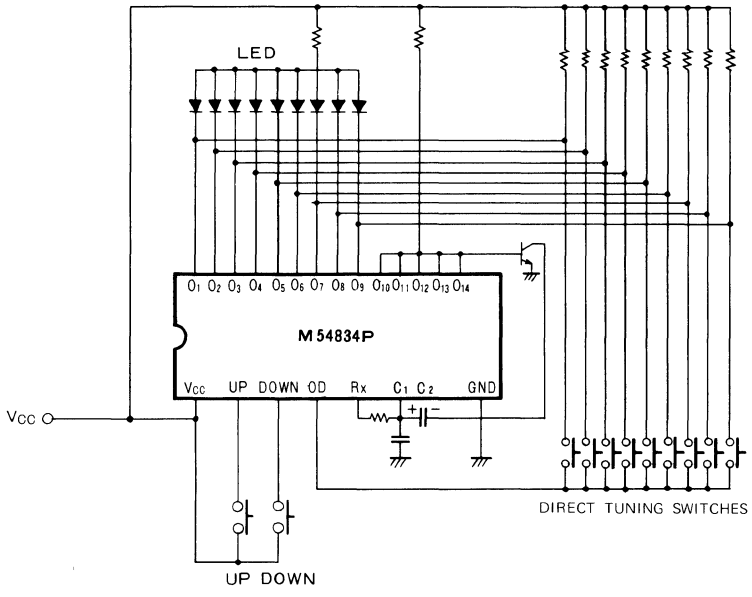
* : Typical values are at T_a=25°C

APPLICATION EXAMPLES

(1) Electronic tuner circuit



(2) Σ_1 Channel skip circuit



M54844P

8-DIGIT FLUORESCENT DISPLAY DRIVER FOR MICROCOMPUTOR

DESCRIPTION

The M54844P, a semiconductor integrated circuit fabricated with using IIL technology, is designed for driving an 8-digit, 8-segment fluorescent display.

FEATURES

- Can be used in either an 8-digit or 7-digit plus a decimal point.
- 4-bit data input
- Mode-input controllable display mode
- Internal clock generator
- Wide operating voltage (V_{CC}=5~12V)

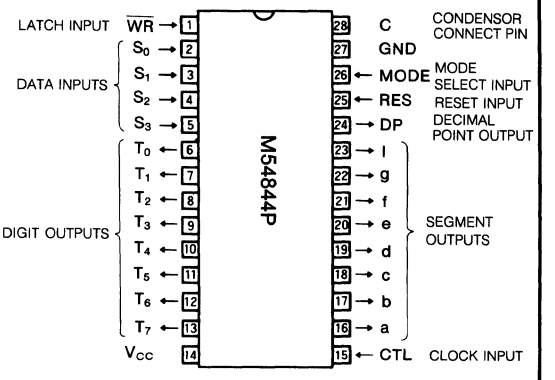
APPLICATION

Micro computer display
Digital equipment for industrial and consumer use

FUNCTION

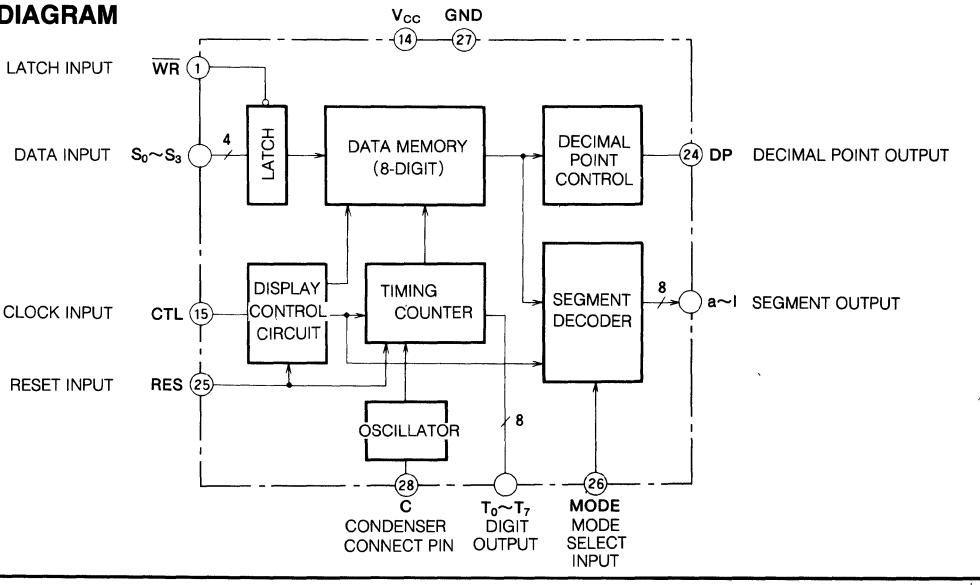
The M54844p, a decoder/driver for fluorescent displays, has a 4-bit X 8-digit memory. Employing the dynamic lighting method, it can light an 8-segment, 8-digit device. Two indication modes can be selected, by the setting of the MODE input.

PIN CONFIGURATIONS (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

DESCRIPTION OF OPERATION

1. Output after reset and during reset.
Outputs during reset (RES=high-state) is shown in the following chart.

Output pin		Output level
Digit output	T_0	H
	T_1~T_7	L
Segment output	a~I	L
	DP	L

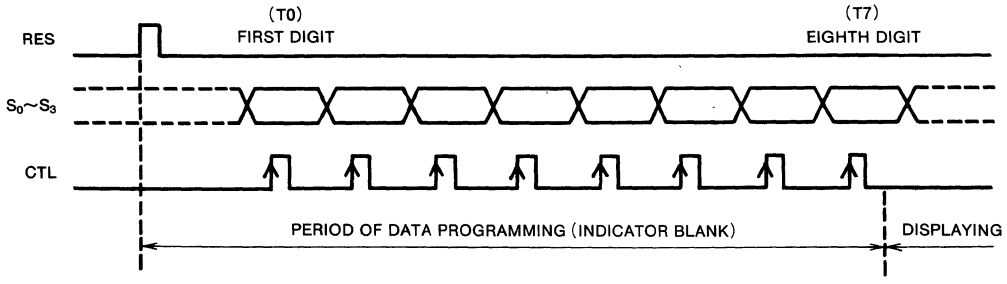
After reset, the outputs T_0~T_7 are scanned beginning with T_0. Outputs S_a~S_I and DP remain in low-state until CTL has been input for 8 cycles.

2. Decimal point setting
The location of the decimal point depends on the contents of the data memory corresponding to T_0. When the decimal point is to be displayed, digit T_0 cannot be used.
The display position of the decimal point is as follows.

Content of digit T_0	Display position of decimal point
0 or 8	T_1
1 or 9	T_2
2 or A	T_3
3 or B	T_4
4 or C	T_5
5 or D	T_6
6 or E	T_7
7 or F	T_0

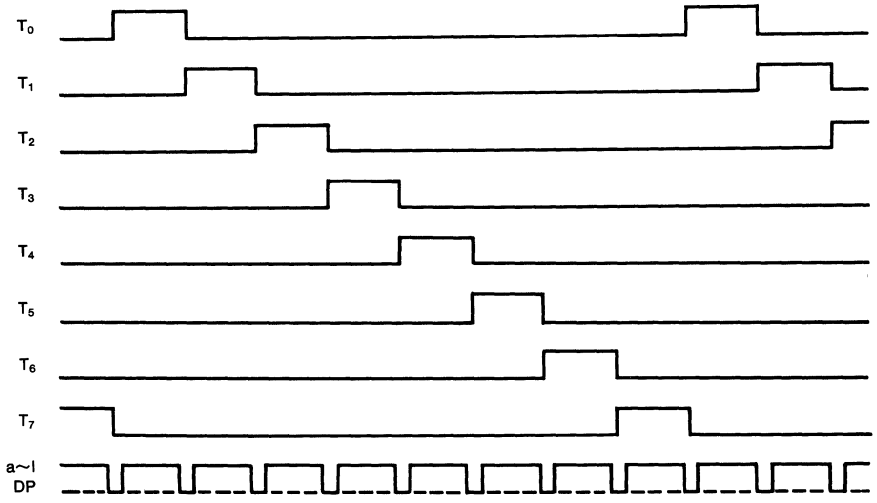
3. Operation timing

(1) Data programming



- Reset input is necessary before data programming input.
- S_0~S_3 data is read at the leading edge of the CTL.

(2) Output timing

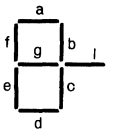


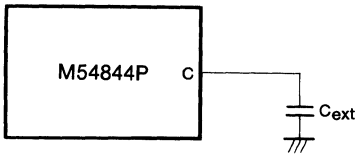
8-DIGIT FLUORESCENT DISPLAY DRIVER FOR MICROCOMPUTOR

DISPLAY CHARACTERS

Mode \ Hexadecimal code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
I	0	1	2	3	4	5	6	7	8	9	-	E	C	-	o	
II	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	+

Mode I is displayed when MODE input is low-state.
Mode II is displayed when MODE input is high-state.





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼+15	V
V_I	Input voltage		−0.3∼V_{CC}	V
V_{CC}-V_O	Voltage between the power supply and output pin	Output off-state	−0.3∼+35	V
Topr	Operating temperature		−30∼+85	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −30∼+85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	10	12	V
V_{CC}-V_O	Voltage between the power supply and output pin			33	V

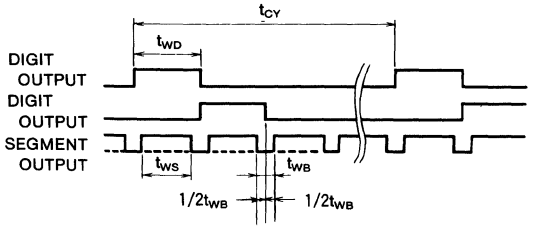
ELECTRICAL CHARACTERISTICS (T_a = −30∼+85℃, V_{CC} = 10V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.7	V
I_{IH}	High-level input current	V_{IH}=10V			20	μA
I_{IL}	Low-level input current	V_{IL}=0.5V			−200	μA
V_{OH}	High-level output voltage	I_{OH}=−10mA	8			V
I_{OLK}	Output leak current	V_O=−20V			−30	μA
I_{CC}	Supply current	Display off-state		12	18	mA
t_{WS}	Segment output width	C_{ext}=1000pF	130	260	520	μs
t_{WB}	Segment blank width	C_{ext}=1000pF	20	40	80	μs
t_{WD}	Digit output width	C_{ext}=1000pF	150	300	600	μs
t_{CY}	Digit period	C_{ext}=1000pF	1.2	2.4	4.8	ms

TIMING REQUIREMENTS (T_a = −30~+85℃, V_{CC} = 4.5~12V, unless otherwise noted)

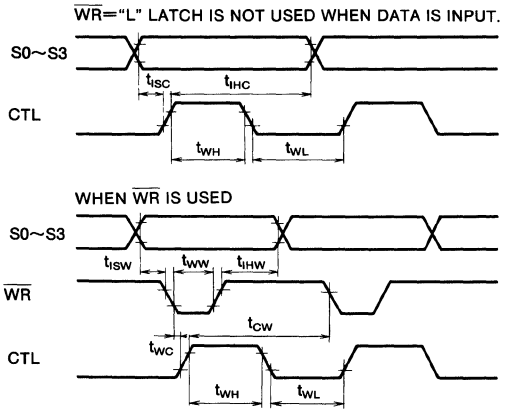
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{ISC}	Input setup time in relation to CLK		5			μs
t_{IHC}	Input hold time in relation to CLK		10			μs
t_{WH}	High-level CTL width		5			μs
t_{WL}	Low-level CTL width		10			μs
t_{ISW}	Input setup time in relation to WR		0			μs
t_{IHW}	Input hold time in relation to WR		5			μs
t_{WW}	WR width		5			μs
t_{WC}	WR→CTL		5			μs
t_{CW}	CTL→WR		15			μs

OUTPUT TIMING DIAGRAM



DIGIT OUTPUT WIDTH $t_{WD}=15t_{OSC}$
SEGMENT OUTPUT WIDTH $t_{WS}=13t_{OSC}$
SEGMENT BLANK WIDTH $t_{WB}=2t_{OSC}$
(t_{OSC} is oscillation period of the oscillator circuit.)

INPUT TIMING DIAGRAM



M54847AP

2-DIGIT BCD-7-SEGMENT DECODER/DRIVER

DESCRIPTION

The M54847AP is a semiconductor integrated circuit consisting of an IIL 2 digit BCD-7 segment decoder/driver.

FEATURES

- Direct drive of LEDs (common cathode type. No need for current limiting resistors, segment current: 10mA max.)
- Direct drive of fluorescent character displays (Segment withstand output is −25V max at V_{CC}=5V.)
- Data input in both serial and parallel formats
- Brightness control input enables continuous LED brightness adjustment.

APPLICATION

TV channel display

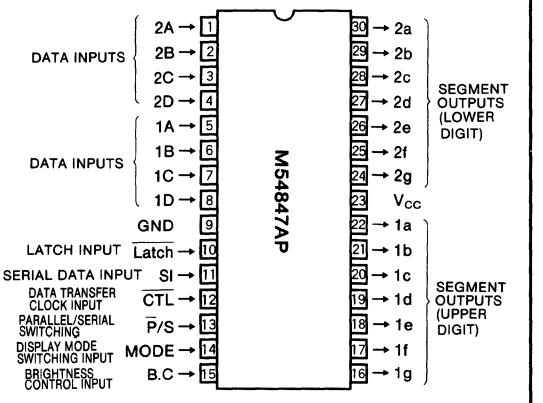
FUNCTIONAL DESCRIPTION

The M54847AP is a 2 digit BCD-7 segment decoder/driver for static drive of LED and fluorescent character displays. The following display modes are possible.

MODE I Numerical display of 00 ~ 99

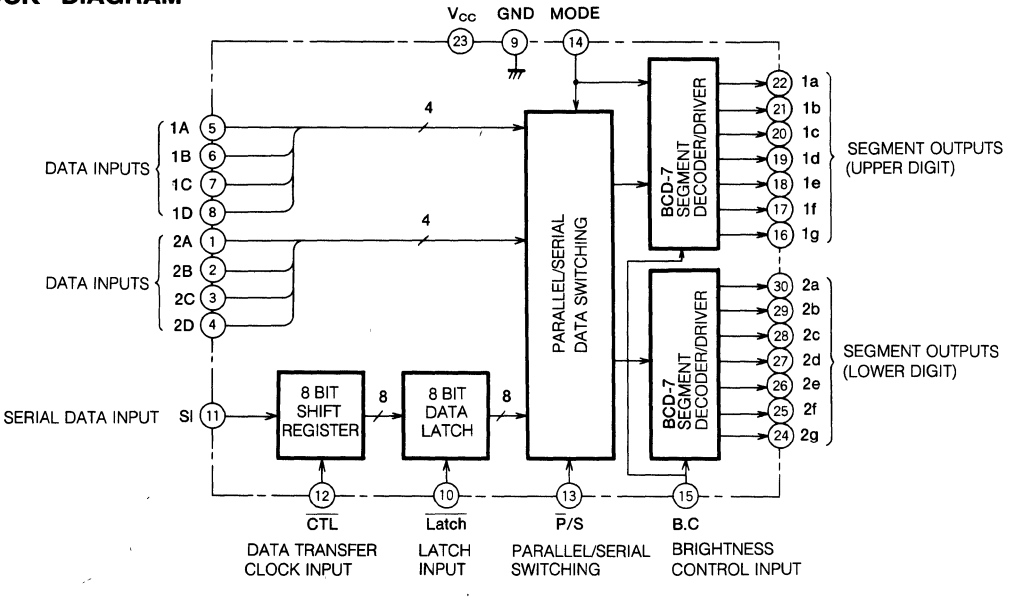
MODE II Numerical display of 0 ~ 39, and AU, CA, −−

PIN CONFIGURATION (TOP VIEW)



Outline 30P4B

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

OPERATING DESCRIPTION

- Display mode

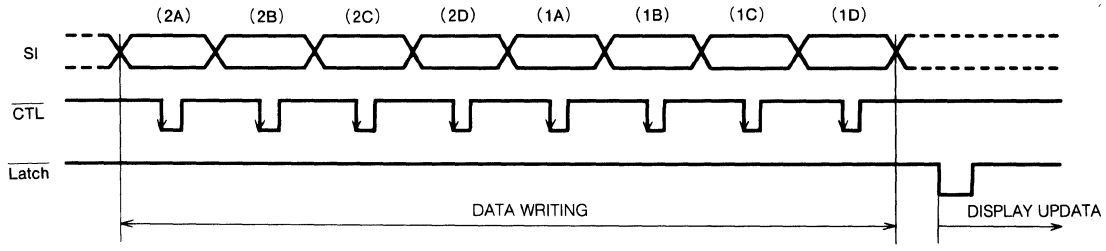
(1) When the mode switching input is high, both digits are driven in accordance with Function Table Ⅰ.

(2) When the mode switching input is low, input 1C and 1D become the character data inputs, driving the display in accordance with Function Table Ⅱ.

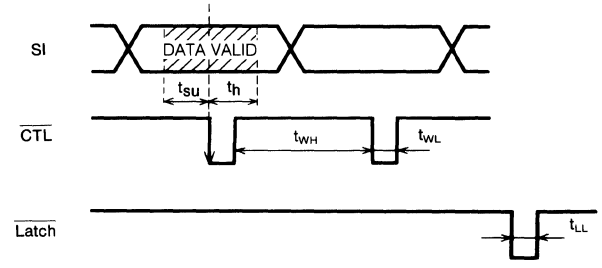
- Serial input data writing

Data 2A→2D and 1A→1D is read sequentially by the low edge of $\overline{CTL}$. After all 8 bits are loaded in the shift register, the display is updated by switching $\overline{Latch}$ input to low.

SERIAL DATA WRITING



INPUT TIMING DIAGRAM



MINIMUM VALUES
$t_{su} = 20\mu s$
$t_h = 20\mu s$
$t_{WH} = 30\mu s$
$t_{WL} = 10\mu s$
$t_{LL} = 10\mu s$

FUNCTION TABLE Ⅰ

Data input				Segment output							Display
A	B	C	D	a	b	c	d	e	f	g	
L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	H	H	L	L	L	L	1
L	H	L	L	H	H	L	H	H	L	H	2
H	H	L	L	H	H	H	H	L	L	H	3
L	L	H	L	L	H	H	L	L	H	H	4
H	L	H	L	H	L	H	H	L	H	H	5
L	H	H	L	H	L	H	H	H	H	H	6
H	H	H	L	H	H	H	L	L	L	L	7
L	L	L	H	H	H	H	H	H	H	H	8
H	L	L	H	H	H	H	H	L	H	H	9
L	H	L	H	L	L	L	L	L	L	H	-
H	H	L	H	H	L	L	H	H	H	H	E
L	L	H	H	H	L	L	H	H	H	L	C
H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	L	L	L	H	H	H	L	o
H	H	H	H	L	L	L	L	L	L	L	Blank

FUNCTION TABLE Ⅱ

Data input		Other data 1A, 1B 2A~2D	Display	
1C	1D		First digit	Second digit
L	L	X	−(Note 1)	−(Note 1)
H	L	X	C	A
L	H	X	A	U
H	H	—	(Note 2)	(Note 3)

Note 1 : Only segment g lights.

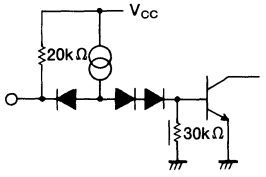
2 : When both 1C and 1D inputs are high, first digit display blanking or numerical display of 1, 2 or 3 is determined by 1A, 1B input state.

Data input				Segment output							Display
1A	1B	1C	1D	1a	1b	1c	1d	1e	1f	1g	
L	L	H	H	L	L	L	L	L	L	L	Blank
H	L	H	H	L	H	H	L	L	L	L	1
L	H	H	H	H	H	L	H	H	L	H	2
H	H	H	H	H	H	H	H	L	L	H	3

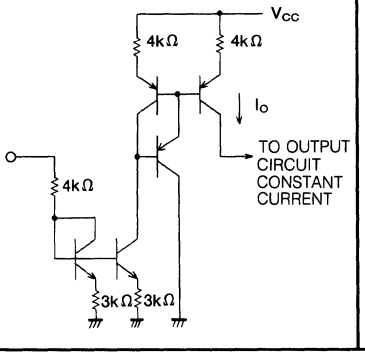
Note 3 : Other digit codes are identical to those in function table Ⅰ

I/O CIRCUIT DIAGRAM

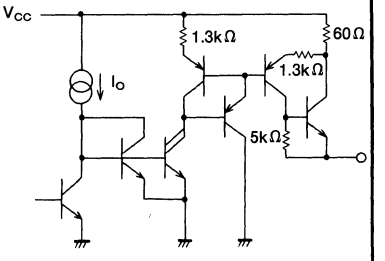
INPUT OTHER THAN B.C
(1A~1D, 2A~2D, Latch, SI, $\overline{CTL}$, $\overline{P/S}$, MODE)



B.C INPUT



SEGMENT OUTPUT (1a~1g, 2a~2g)



ABSOLUTE MAXIMUM RATINGS (T_a = −10~+60℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+V_{CC}	V
$V_{CC}-V_O$	Voltage between supply and output		−0.5~+35	V
Topr	Operating temperature		−10~+60	℃
Tstg	Storage temperature		−40~+125	℃
P_d	Power dissipation	T_a = 60℃	800	mW

RECOMMENDED OPERATING CONDITIONS (T_a = −10~+60℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	6	V
Iseg	Segment current				−10	mA
V_O	Output withstand voltage when output is off				−25	V

ELECTRICAL CHARACTERISTICS (T_a = −10~+60℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High input voltage	V_{CC} = 4.5~6V		2		V_{CC}	V
V_{IL}	Low input voltage	V_{CC} = 4.5~6V		0		0.6	V
I_{IH}	High input current	V_{CC} = 6V	B.C input	0.5	0.75	1.2	mA
		V_{IH} = 6V	Inputs other than B.C			50	μA
I_{IL}	Low input current	V_{CC} = 6V	B.C input			50	μA
		V_{IL} = 0V	Inputs other than B.C	−280	−400	−650	
Iseg	Segment output current	V_{CC} = 5V, V_O = 2V, B.C pin is connected to V_{CC}		−10			mA
Islk	Segment leak current	V_{CC} = 5V, V_O = −25V				−50	μA
I_{CC1}	Supply voltage	V_{CC} = 6V, All inputs and outputs are open			4	8	mA

* : Typical values are at T_a = 25℃.

M54886P

SYSTEM CONTROLLER FOR TAPE DECK

DESCRIPTION

The M54886P is an I^2L semiconductor integrated circuit consisting of a tape deck controller designed to control tape deck mechanisms and amplifier systems.

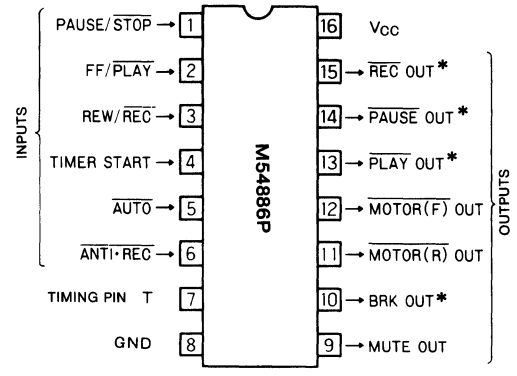
FEATURES

- Non-locking function keys can be used
- Built-in timing circuit
- Simultaneous depressing of a multiple number of input keys, depressing the keys too quickly and other incorrect operations are dealt with
- Easy configuration for timer operations for unattended recording, etc.
- Easy configuration for PLAY -> REW, REW -> PLAY and other auto repeat operations
- Direct drive possible for LEDs that indicate operational modes
- Stop function in about 1.6s when power is switched on

APPLICATION

Tape decks and cassette recorders

PIN CONFIGURATION (TOP VIEW)



* : Open collector output

Outline 16P4

FUNCTION

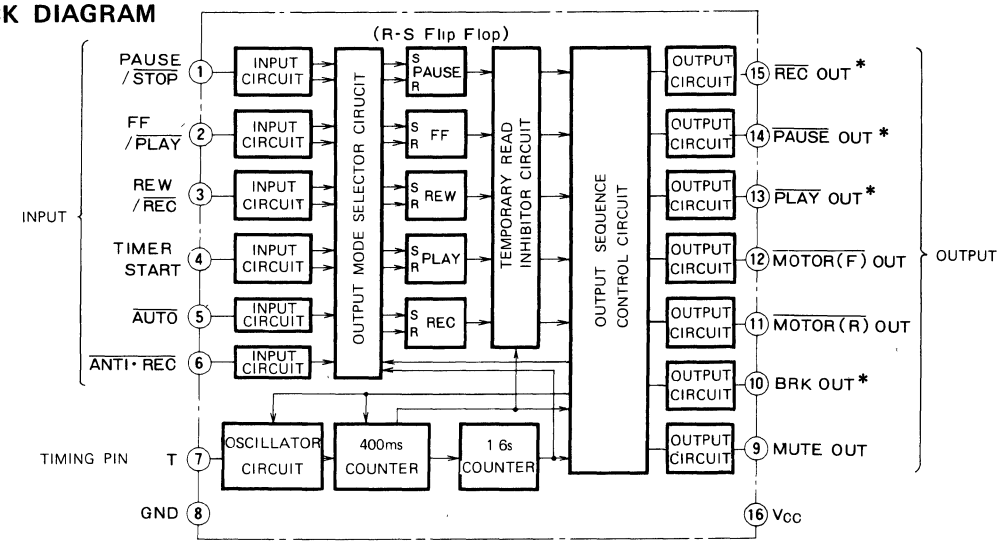
The M54886P is designed to control the operational sequence of a tape deck. The timing of the operations is controlled by the time which is determined by the RC elements making up the oscillator circuit.

The output sequence is designed to correspond with the operational sequence of the mechanism, and since the timing is provided for the rec/pb switching signal and the muting signals as well as other amplifier control signals, the external circuitry can be simplified.

Non-locking keys can be used for the function input keys and the desired operational mode is established simply when one of the keys is depressed. A change can be made from one mode to another directly, and with a mode change from FF·REW ⟷ PLAY (REC) or vide versa, operation goes through the STOP mode for 0.4s (Note 1) automatically. Sufficient provision is made to deal with incorrect operation such as when a multiple number of input keys are depressed simultaneously or when the keys are depressed too quickly.

Operation goes through the STOP mode for 1.6s. (Note 1) when the power is switched on, and it is possible to use the MUTE output as the muting signal when the power is switched on. Unattended recording, wake-up playback and other timer operations can be easily configured using the TIMER START pin.

BLOCK DIAGRAM



* : OPEN COLLECTOR OUTPUT

(Note 1: The time can be changed with the time constants of the RC elements. This is the same for the times which are mentioned below.)

Table 1. Description of pins

Pin no	Name	Function	
1	PAUSE/$\overline{\text{STOP}}$	Function input	Input pin that selects the PAUSE mode at high and STOP mode at low, open when no input
2	FF/$\overline{\text{PLAY}}$		Input pin that selects the FF mode at high and PLAY mode at low
3	REW/$\overline{\text{REC}}$		Input pin that selects the REW mode at high and $\overline{\text{REC}}$ mode at low, the REC input is effective only when fed in together with the PAUSE or $\overline{\text{PLAY}}$ input
4	TIMER START		Input pin that selects the operational mode when the power is switched on The PLAY mode is selected when kept high, the REC mode is selected when kept at low When left open, the STOP mode is selected
5	$\overline{\text{AUTO}}$	Control input	Input pin that commands the PLAY → REW, REW → PLAY, FF → STOP mode changes by feeding in low-level pulses (⌐⌐)
6	$\overline{\text{ANTI}}$ • $\overline{\text{REC}}$		Input pin for inhibiting recordings, when kept at low, the recording input is inhibited
7	T		Externally mounted resistor/capacitor connecting pin for oscillator circuit
8	GND		Ground
9	MUTE OUT	Output	Muting signal output, muting is effective at the high-level
10	BRK OUT		Reel disc brake signal output, brake is released at high
11	$\overline{\text{MOTOR(R)}}$ OUT		Reel motor reverse rotation signal output
12	$\overline{\text{MOTOR(F)}}$ OUT		Reel motor forward rotation signal output
13	$\overline{\text{PLAY}}$ OUT		PLAY signal output, play solenoid drive signal
14	$\overline{\text{PAUSE}}$ OUT		Recording signal output, signal that selects the amplifier's recording and playback
15	$\overline{\text{REC}}$ OUT		PAUSE signal output, pause solenoid drive signal
16	V_{CC}		Supply voltage

Table 2. Output states in each mode

Mode \ Output	$\overline{\text{PAUSE}}$	MUTE*	$\overline{\text{REC}}$	$\overline{\text{PLAY}}$	BRK*	$\overline{\text{MOTOR(F)}}$	$\overline{\text{MOTOR(R)}}$	Notes
STOP mode	H	H	H	H	L	H	H	Stop
FF mode	H	H	H	H	H	L	H	Fast forward
REW mode	H	H	H	H	H	H	L	Rewind
PLAY mode	H	L	H	L	H	L	H	Playback
REC mode	H	L	L	L	H	L	H	Recording
REC/PAUSE mode	L	L	L	H	L	H	H	Recording pause
PAUSE mode	L	H	H	H	L	H	H	Pause

Note: * indicates high-level active output, others outputs are low-level active

DESCRIPTION OF OPERATION

1. Operation timing

In Fig. 1 the timing from the STOP to PLAY mode is taken as an example.

About 50ms after the PLAY key is depressed, the play solenoid is attracted and 50ms later the reel motor starts to rotate and the brake is released simultaneously. Muting ceases to be effective 450ms after the operation and the sound is fed out from the amplifier.

Even with other mode changes, the output timing is aligned with the mechanism timing.

The output modes changes as shown in Table 3 when an input is applied. Timings during the changes are given in the timing chart.

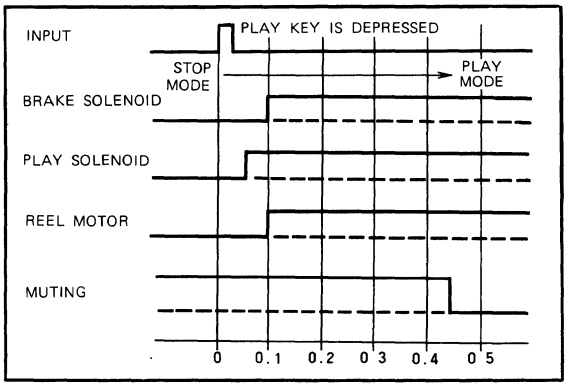


Fig.1 The timing from the STOP to PLAY mode

Table 3. Operations from output modes

Key input / Present mode	STOP	PLAY	REC+PLAY	FF	REW	PAUSE	REC PAUSE	AUTO
STOP mode		PLAY mode	REC mode	FF mode	REW mode	PAUSE mode	REC/PAUSE mode	
PLAY mode	STOP mode		REC mode	FF mode	REW mode	PAUSE mode	REC/PAUSE mode	REW mode
REC mode	STOP mode			FF mode	REW mode	REC/PAUSE mode	REC/PAUSE mode	REW mode
FF mode	STOP mode	PLAY mode	REC mode		REW mode			STOP mode
REW mode	STOP mode	PLAY mode	REC mode	FF mode				PLAY mode
PAUSE mode	STOP mode	PLAY mode	REC mode	FF mode	REW mode		REC/PAUSE mode	
REC/PAUSE mode	STOP mode	REC mode	REC mode	FF mode	REW mode			

Note 1 ⊘ indicates that the output mode does not change
2 REC+PLAY and REC+PAUSE indicates that the two keys are depressed simultaneously

2. Operation with multiple key depressing simultaneously and over fast depressing of keys

Table 4 shows what happens when two input keys are depressed simultaneously. When the keys are released after having been depressed together, the mode designated by the key that was last released is established. Fig. 2 shows an example where the FF and REW input keys are depressed simultaneously.

When the input keys have been depressed too quickly, a change is made to the mode based on the key that was depressed second after the mode has changed based on the key that was depressed first.

The STOP mode is maintained for 0.4s when operation goes through this mode when the keys are depressed too quickly or two keys are depressed simultaneously.

Table 4. Operation when two keys are pressed simultaneously

Input / Input	STOP	FF	REW	PLAY	REC	PAUSE
STOP		STOP mode	STOP mode	STOP mode	mode	
FF			STOP mode		mode	FF mode
REW				STOP mode		REW mode
PLAY					mode	mode
REC						REC/PAUSE mode
PAUSE						

Note ⊘ indicates that no signal can be entered because of the configuration of the input circuits

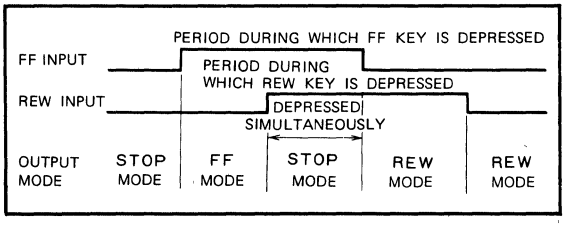


Fig. 2 FF and REW input keys depressed together

3. Operation when power is switched on

When the power is switched on, the STOP mode is established for about 1.6s and all inputs during this period are ignored. Subsequently, when the TIMER START input pin is open, the STOP mode is retained but when the pin has been to the high level, the PLAY mode is established automatically. When the pin has been set to the low, the REC mode is established automatically. The input signal cannot enter from the TIMER START input pin after that period.

4. Operation based on $\overline{\text{AUTO}}$ input

The $\overline{\text{AUTO}}$ input is normally open or high level is kept applied. When the tape-end or other signal is shaped into a pulse below 400ms and applied to the $\overline{\text{AUTO}}$ input, it is possible to order a change from the PLAY or REC mode to the REW mode, REW mode to PLAY mode and FF mode to STOP mode.

5. Determining the RC time constants of oscillator circuit

The operational timing inside the IC is determined by the clock pulses created by the oscillator circuit.

Fig. 3 shows the external connections of the oscillator circuit while Fig. 4 shows the oscillation waveform.

Oscillation is started by the input when the mode changes and after the operation it stops.

The oscillation period is approximately defined by the following relationship:

$$t_{osc} = 0.7\ C_{ext} \times (R_{ext} + 5)\ \text{(ms)}$$

(μF used for C_{ext} units, kΩ for R_{ext} units)

Delay times T_1 and T_2 (see timing chart) for the output with respect to the input keys and stopping time T_3 when the power is switched on are set as follows:

$$T_1 = 2 \times t_{osc}$$
$$T_2 = 16 \times t_{osc}$$
$$T_3 = 68 \times t_{osc}$$

If T_1 is set to 50ms, T_2 to 400ms and T_3 to 1.6s typically, then t_{osc} becomes 25ms which means that the RC constants are 0.33μF for C_{ext} and 100kΩ for R_{ext}. Fig. 6 shows the relationship between C_{ext}/R_{ext} and t_{osc}.

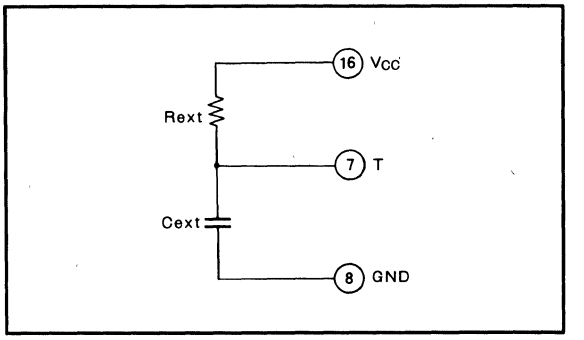


Fig. 3 Oscillator circuit external connection diagram

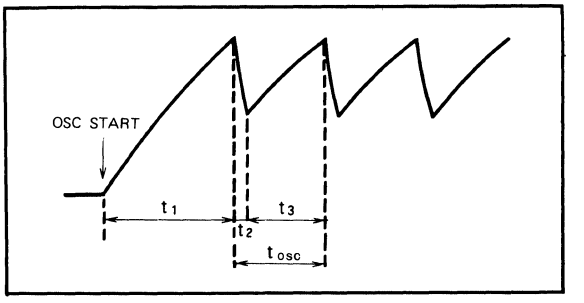
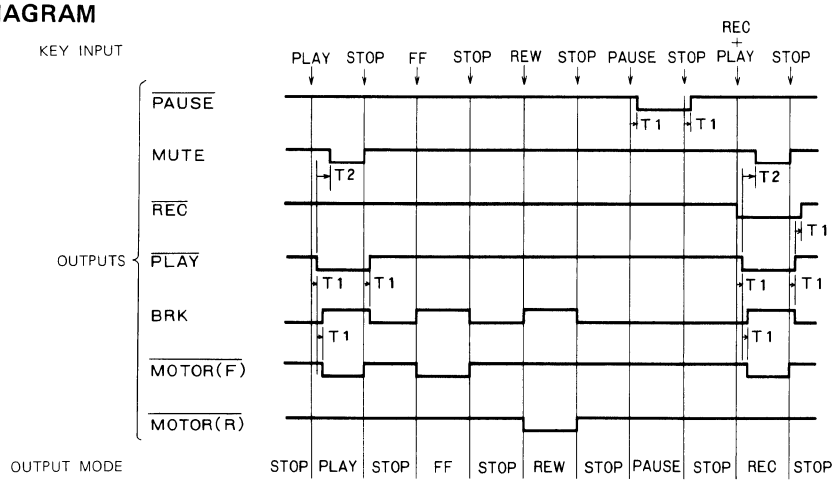
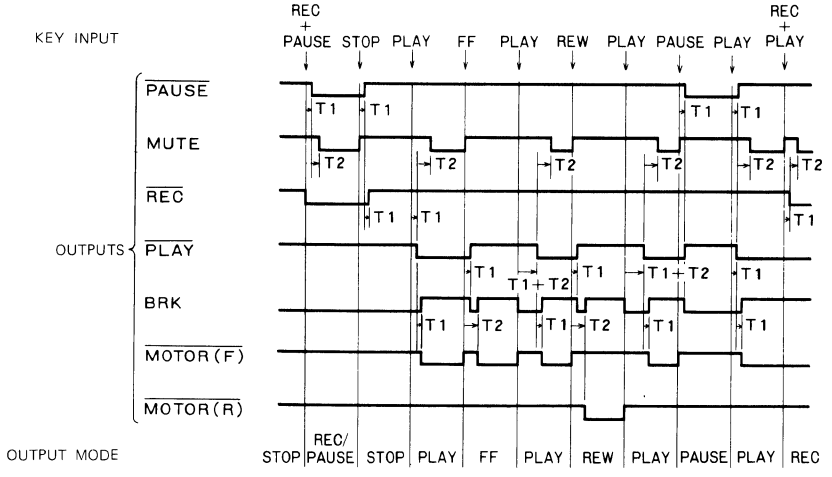


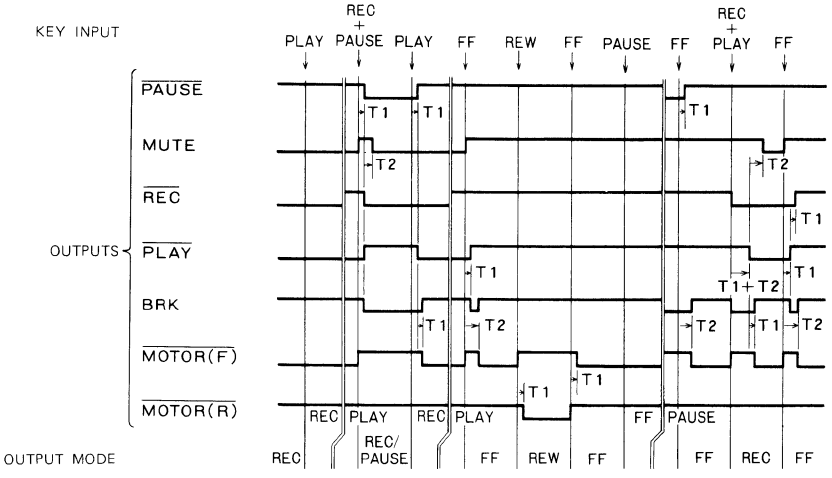
Fig. 4 Oscillation waveform

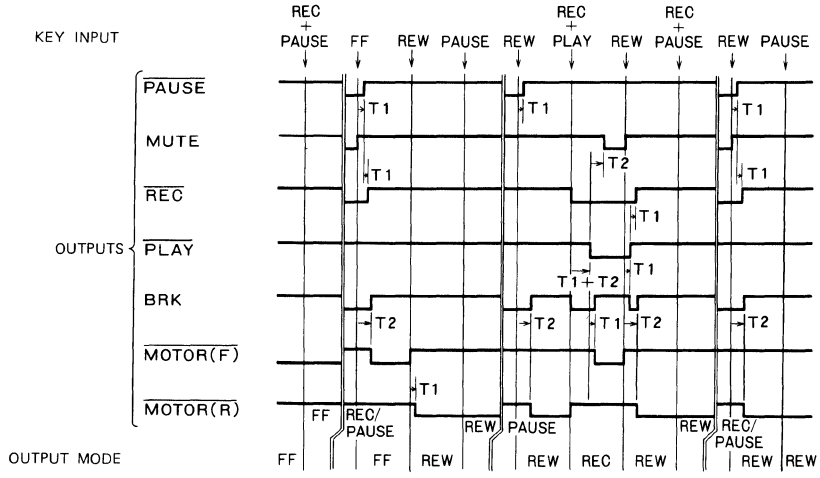
MITSUBISHI ELECTRIC

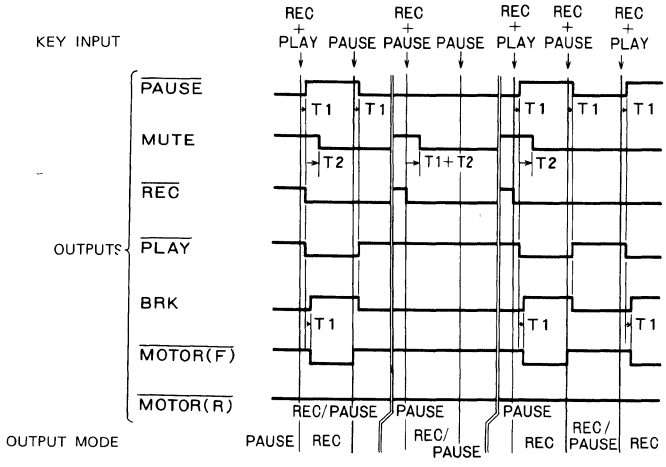
TIMING DIAGRAM





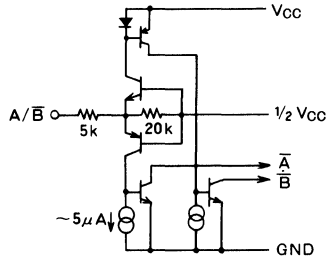



KEY INPUT
REC + PAUSE
FF
REW
PAUSE
REW
REC + PLAY
REW
REC + PAUSE
REW
PAUSE
OUTPUTS
PAUSE
MUTE
REC
PLAY
BRK
MOTOR(F)
MOTOR(R)
T1
T2
T1+T2
OUTPUT MODE
FF
REC/ PAUSE
FF
REW
REW
PAUSE
REW
REC
REW
REC/ PAUSE
REW
REW

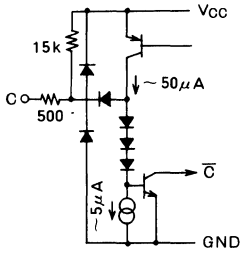

KEY INPUT
REC + PLAY
PAUSE
REC + PAUSE
PAUSE
REC + PLAY
REC + PAUSE
REC + PLAY
OUTPUTS
PAUSE
MUTE
REC
PLAY
BRK
MOTOR(F)
MOTOR(R)
T1
T2
T1+T2
OUTPUT MODE
REC/PAUSE
PAUSE
PAUSE
PAUSE
REC
REC/ PAUSE
REC
REC/ PAUSE
REC

INPUT/OUTPUT CIRCUITS

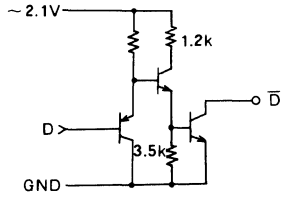
Input 2 circuit (pin 1~4)



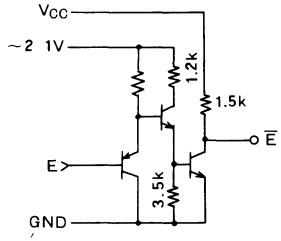
Input 1 circuit (pins 5, 6)



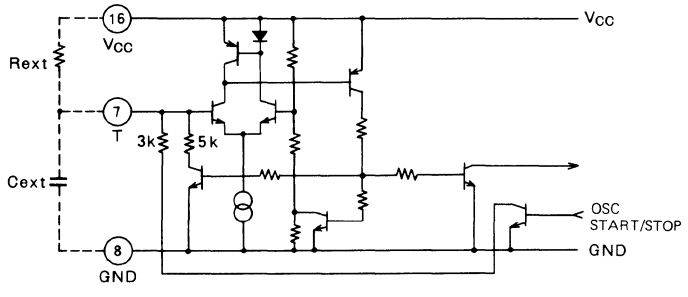
Open collector outputs (pins 10, 13~15)



Output with pull-up resistor (pins 9, 11, 12)



Oscillator circuit



ABSOLUTE MAXIMUM RATINGS (Ta = −10 ~ +60°C, unless otherwise noted)

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage		−0.5 ~ +7.5	V
V_I	Input voltage		−0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage	When output is high	V_{CC}	V
Pd	Power dissipation		500	mW
Topr	Operating temperature		−10 ~ +60	°C
Tstg	Storage temperature		−55 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ +60°C, unless otherwise noted)

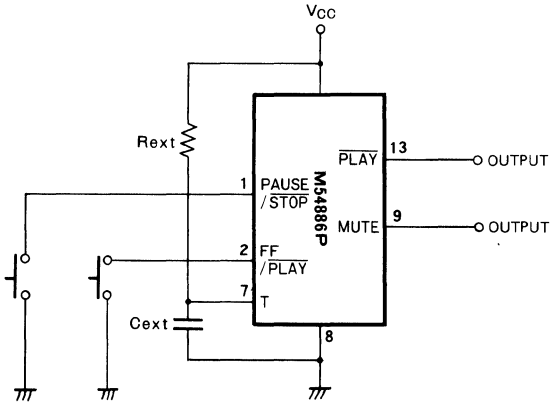
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4	5	6	V
Rext	External timing resistor for oscillator circuit	20	100	200	kΩ

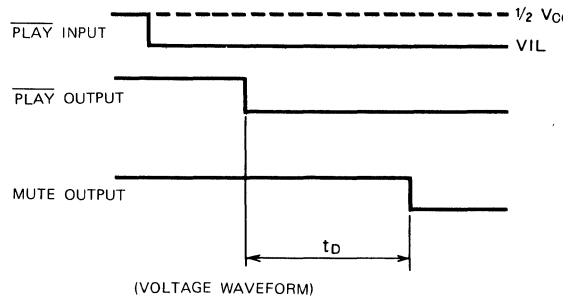
ELECTRICAL CHARACTERISTICS (T_a = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage (pins 5, 6)			2.4			V
V_{IL}	Low input voltage (pins 5, 6)					1.5	V
V_{TH}	High-level threshold voltage (pins 1, 2, 3, 4)				$\frac{V_{CC}}{2}+0.9$		V
V_{TL}	Low-level threshold voltage (pins 1, 2, 3, 4)				$\frac{V_{CC}}{2}-0.9$		V
V_{IOP1}	Input open voltage	Pins 5, 6	V_{CC}=5V	4.7			V
V_{IOP2}		Pins 1, 2, 3, 4	V_{CC}=5V	2.25	2.5	2.75	V
I_{IH2}	High-level input current (pins 1, 2, 3, 4)		V_{CC}=6V, V_{IH}=5.8V		0.45	0.7	mA
I_{IL1}	Low-level input current	Pins 5, 6	V_{CC}=6V, V_{IL}=0.2V		−0.4	−0.6	mA
I_{IL2}		Pins 1, 2, 3, 4	V_{CC}=6V, V_{IL}=0.2V		−0.45	−0.7	mA
V_{OL}	Low-level output voltage (pins 9, 10, 11, 12, 13, 14, 15)		V_{CC}=4V, I_{OL}=30mA		0.2	0.4	V
V_{OH}	High-level output voltage (pins 9, 10, 11)		V_{CC}=4V, I_{OH}=−0.4mA	3.1	3.4	3.7	V
I_{CC1}	Circuit current		V_{CC}=6V, STOP Mode		6	15	mA
I_{CC2}			V_{CC}=6V, REC/PAUSE Mode		13	20	mA
t_D	Delay time		V_{CC}=5V, Rext=100kΩ, Cext=0.33μF (See test circuit figure)	280	400	520	ms

* : Typical values are at T_a=25°C.

TEST CIRCUIT

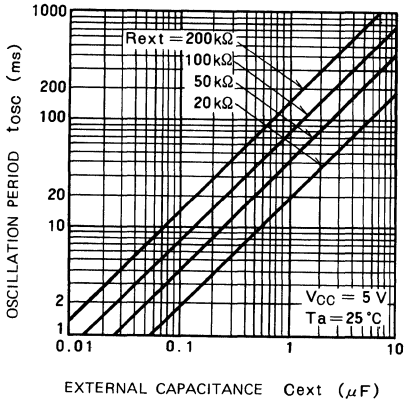




(VOLTAGE WAVEFORM)

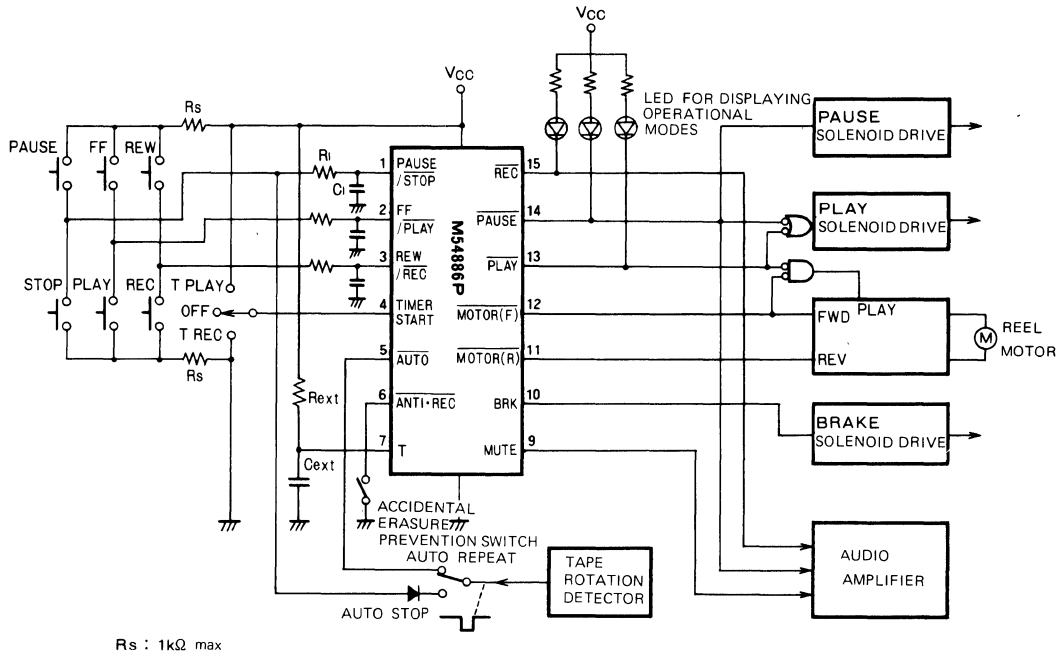
Note The time is measured until the change to the MUTE output from the PLAY output when the mode changes from STOP to PLAY.

OSCILLATION PERIOD OF OSCILLATOR CIRCUIT



MITSUBISHI ELECTRIC

APPLICATION EXAMPLE



Rs : 1kΩ max
Ri : 2kΩ
Ci : 0.01μF

M54910P

F2F MAGNETIC STRIPE ENCORDING CARD READER

DESCRIPTION

The M54910P is an I^2L semiconductor intergrated circuit consisting of an F2F demodulator for magnetic stripe card readers.

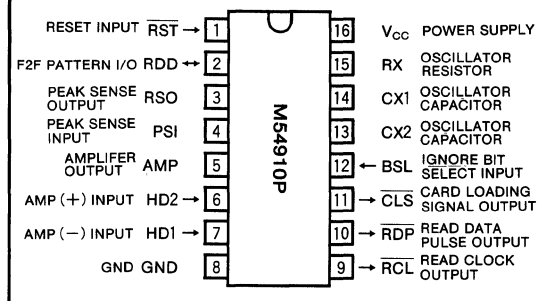
FEATURES

- Low power dissipation (18mA typ)
- Ignore bit select input (bits 2, 8)
- Open collecteor output
- Wide operating temperature range T_a=−20∼+75℃

APPLICATION

Magnetic stripe card readers

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTION

The data signal from a magnetic stripe card is read by a magnetic head and enters the M54910P via inputs HD-1 and HD-2. The signal is analog processed by amplifier OP1, peak detector OP2 and waveform regenerator OP3 to demodulate the F2F pattern signal. The specific bit numbers set by input BSL are ignored, and the data is digitally processed to output card loading signal $\overline{CLS}$, demodulated clock signal $\overline{RCL}$, and demodulated data signal $\overline{RDP}$.

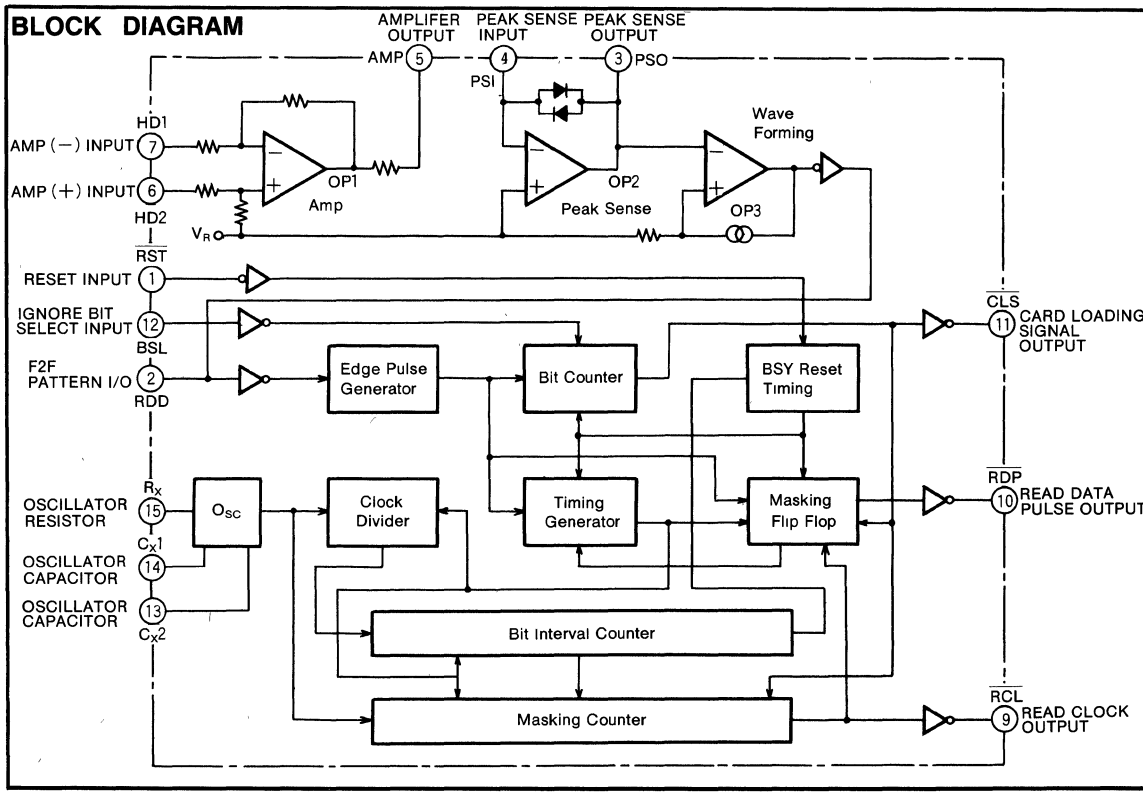
$\overline{CLS}$ becomes low when two rising and falling edges of the F2F pattern signal RDD are counted (eight if BSL is high). If no input data is detected for a specified period, $\overline{CLS}$ returns to high. $\overline{RCL}$ is a clock signal whose period corresponds to T_B, the duration of one data bit when the card speed is constant.

If T_{Bn} is the duration of a particular bit, $\overline{RCL}$ will be high for a period of 2/3 T_{Bn}-1. When the bit value is 1, $\overline{RDP}$ is set low by the timing of RDD. In other words, while $\overline{RCL}$ is high, it can respond to a change of state in RDD. This means that even if the card speed changes, (typically 10∼150cm/s) where T_{Bn} satisfies the following formula.

$2/3\ T_{Bn}-1 < T_{Bn} < 4/3 T_{Bn}$

The T_B is counted by the oscillator period T_{OSC}.

BLOCK DIAGRAM



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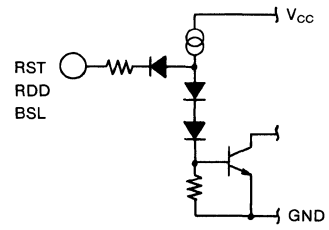
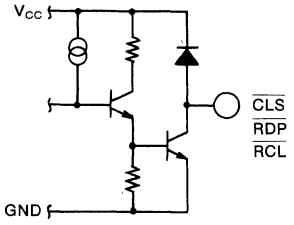
I/O CIRCUIT CHART

INPUT CIRCUIT



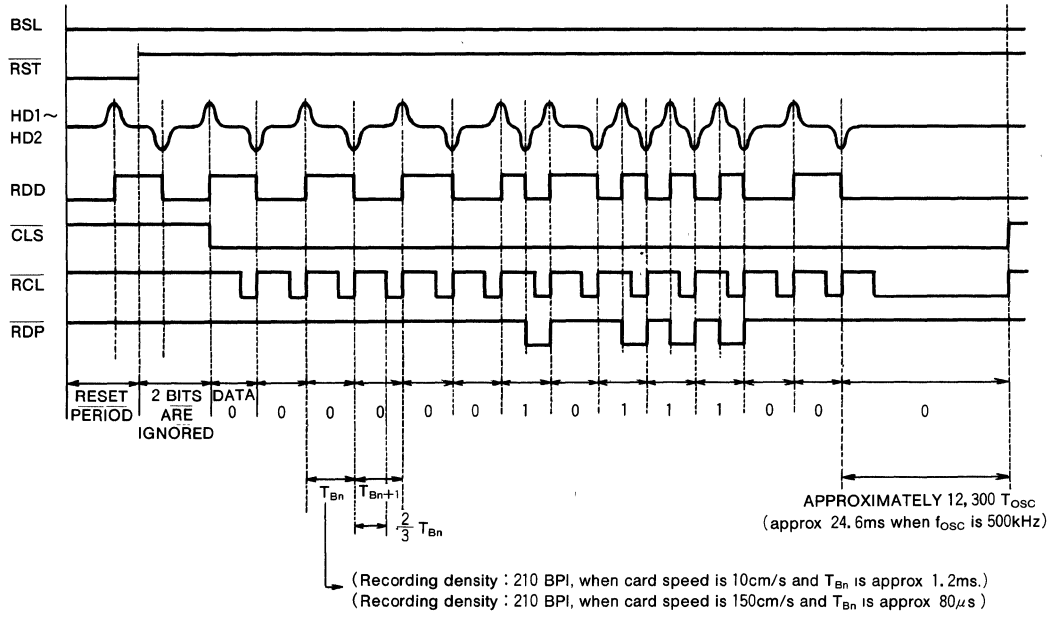
OUTPUT CIRCUIT



PIN DESCRIPTION

pin number	Symbol	Name	Description
1	$\overline{RST}$	Reset input	Resets when low When not used, reset is performed as required by internal logic
2	RDD	F2F pattern I/O	Monitor input/output of F2F pattern reformed magnetic head signal.
3	PSO	Peak sense output	A resistor and capacitor are connected in parallel between PSI and PSO to set the negative feedback impedance of the peak sense circuit.
4	PSI	Peak sense input	Refer to PSO and AMP
5	AMP	Amp output	A resistor and capacitor are connected between PSI and AMP to set the peak sense circuit
6	HD2	Amp (+) input	The magnetic head is connected between HD1 and HD2
7	HD1	Amp (−) input	Same as above
8	GND	GND	
9	$\overline{RCL}$	Read clock output	Clock output after F2F demodulation
10	$\overline{RDP}$	Read data pulse output	Data output after F2F demodulation
11	$\overline{CLS}$	Card loading signal output	Becomes low while a card is running
12	BSL	Ignore bit select input	2 bit are ignored when low, 8 bits when high
13	CX2	Oscillator capacitance	A capacitor is connected between CX1 and CX2 to set the oscillator freqency
14	CX1	Oscillator capacitance	Same as above
15	RX	Oscillator resistance	A resistor is connected between V_{CC} and RX to set the oscillator current
16	V_{CC}	Power supply	

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0. 5∼+6	V
V_I	Input voltage	$\overline{RST}$, PDD, BSL	−0. 5∼V_{CC}	V
V_O	Output voltage	When $\overline{CLS}$, $\overline{RDP}$ and $\overline{RCL}$ are high	−0. 5∼V_{CC}	V
P_d	Power dissipation		150	mW
T_{opr}	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

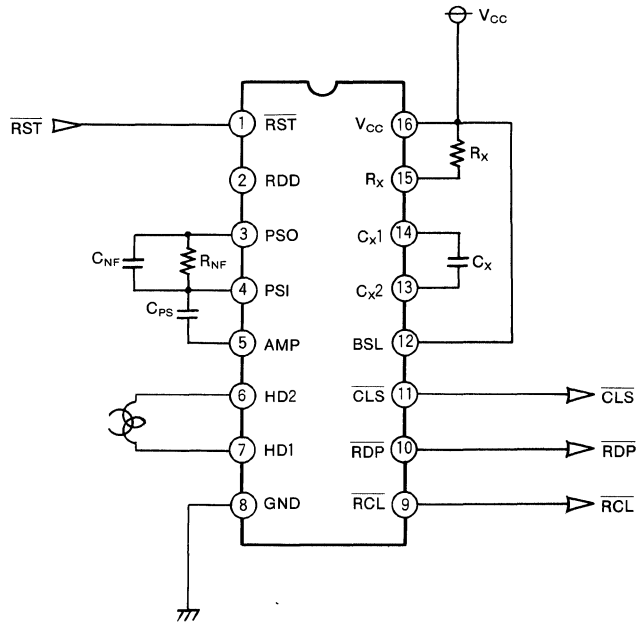
RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{RST}$, RDD, BSL	2		V_{CC}	V
V_{IL}	Low-level input voltage	$\overline{RST}$, RDD, BSL	0		0.8	V
I_{OL}	Low-level output current	$\overline{CLS}$, $\overline{RDP}$, $\overline{RCL}$			16	mA
V_{OH}	High-level output voltage	When $\overline{CLS}$, $\overline{RDP}$ and $\overline{RCL}$ are high.			V_{CC}	V
V_{ID}	Differential input voltage	HD1, HD2	2.5		80	mV_{PP}
f_{IN}	Input frequency	HD1, HD2	0.4		20	kHz
f_{OSC}	Oscillator frequency	$f_{OSC}=\frac{1}{T_{OSC}}\fallingdotseq\frac{1}{2R_XC_X}$				kHz
R_X				15		kΩ
C_X		When recording density is 210 BPI		68		pF
C_{PS}		When recording density is 210 BPI		0.022		μF
C_{NF}		When recording density is 210 BPI		1000		pF
R_{NF}		When recording density is 210 BPI		680		kΩ

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min	Typ	Max	
I_{CC}	Circuit current	V_{CC}	V_{CC}=5.5V, V_{IN}=80mV_{PP}, f_{IN}=20kHz	1			25	mA
I_{IL}	Low-level input current	RST, RDD, BSL	V_{CC}=5.5V, V_{IL}=0.4V	5	−50		−200	μA
I_{IH}	High-level input current	RST, RDD, BSL	V_{CC}=5.5V, V_{IN}=5.5V	5			40	μA
V_{OL}	Low-level output voltage	$\overline{CLS}$, $\overline{RDP}$, $\overline{RCL}$	V_{CC}=4.5, I_{OL}=16mA	6			0.4	V
I_{OL}	High-level output current	$\overline{CLS}$, $\overline{RDP}$, $\overline{RCL}$	V_{CC}=5.5V, V_{OH}=5.5V	6			200	μA
R_{IN}	Input resistance	HD1, HD2	V_{CC}=5V, ΔV_{IN}=40mV	3	1.7		4.2	kΩ
V_R	Reference voltage	AMP	V_{CC}=5V	4	2.25		2.75	V
G_{V1}	Voltage gain 1	Amplifier curcuit	V_{CC}=5V, V_{IN}=80mV_{PP}, f_{IN}=1kHz	2	24		30	V/V
G_{V2}	Voltage gain 2	Amplifier circuit	V_{CC}=5V, V_{IN}=80mV_{PP}, f_{IN}=20kHz	2	21		30	V/V
V_{OPP}	Maximum output voltage	Amplifier circuit	V_{CC}=5V, f_{IN}=20kHz	2	2.6			V_{PP}
I_{IB}	Input bias current	PSI	V_{CC}=5V	3			−0.2	μA
V_{CL}	Clamp voltage	Peak sense circuit	V_{CC}=5V, V_{IN}=80mV_{PP}, f_{IN}=1mkHz	1	0.8		2.4	V_{PP}
V_{TH}	Threshold voltage	Waveform regenerator circuit	V_{CC}=5V	4	±0.15		±0.26	V
DF	Duty factor	Peak sense circuit	V_{CC}=5V, V_{IN}=2.5mV_{PP}, f_{IN}=1kHz	1	40		60	%
f_{OSC}	Oscillator frequency	Oscillator circuit	V_{CC}=5V, R_X=15kΩ, C_X=68pF	4	380		600	kHz
T_{d1}	Delay time 1		V_{CC}=5V	7			T_{OSC}+2	μs
T_{d2}	Delay time 2		V_{CC}=5V	7			$3T_{OSC}$+2	μs
T_{d3}	Delay time 3		V_{CC}=5V	7			$3T_{OSC}$+4	μs
T_{d4}	Delay time 4		V_{CC}=5V	7			$12294T_{OSC}$ +0.5	μs

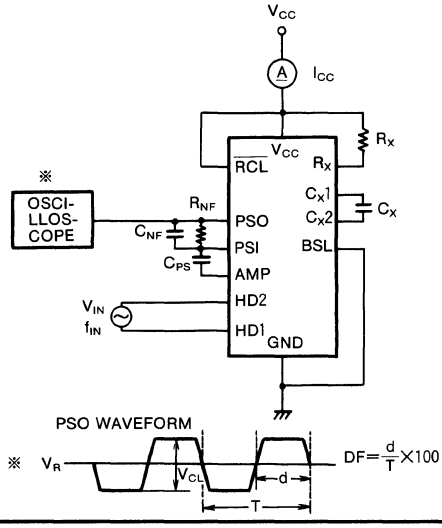
APPLICATION EXAMPLE



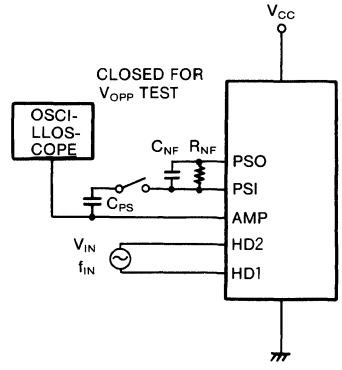
Note : The following procedure allows RDD to be used as an input
1) Shout circuit HD1 and HD2.
2) Leave AMP and PSO open
3) Connect resistor R_{PS} (5kΩ to 50kΩ) between PSI and GND.

TEST CIRCUIT (R_X=15kΩ, C_X=68pF, C_{PS}=0.022μF, C_{NF}=1000pF, RNF=680kΩ, unless otherwise noted)

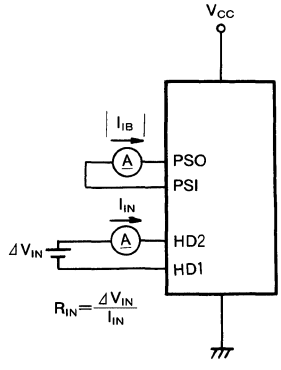
1 • I_{CC}, V_{CL}, DF TEST



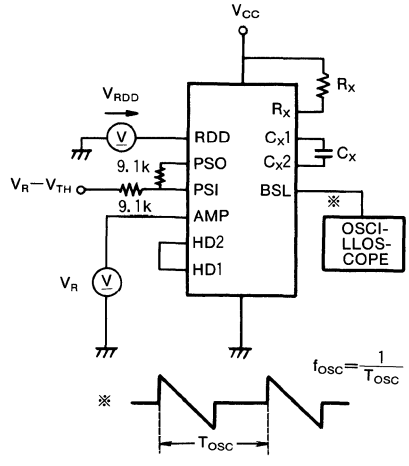
2 • G_{V1}, G_{V2}, V_{OPP} TEST



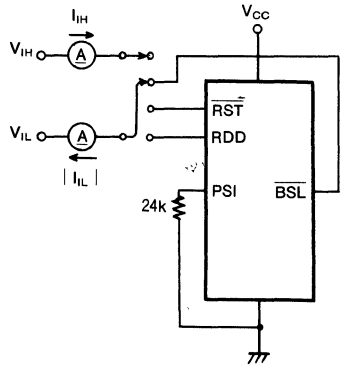
3 • R_{IN}, I_{IB} TEST



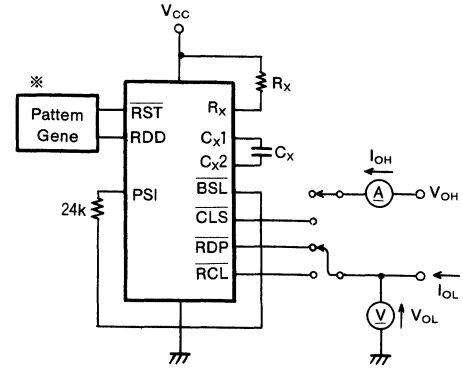
4 • V_R, V_{TH}, f_{OSC} TEST



5 • I_{IL}, I_{IH} TEST

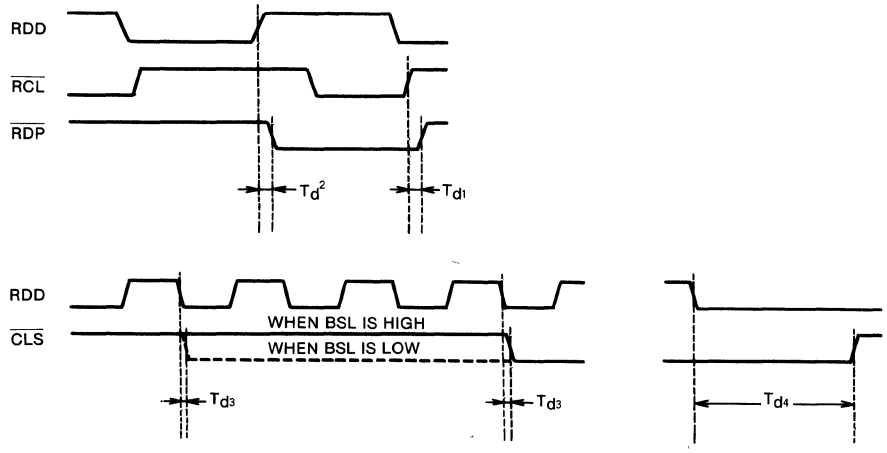


6 • V_{OL}, I_{OH} TEST



※ Apply the appropriate pattern to set the test pin either high or low.

7 • T_{d1}, T_{d2}, T_{d3}, T_{d4} TEST



MITSUBISHI ELECTRIC

M54914FP

F2F MAGNETIC STRIPE ENCORDING CARD READER

DESCRIPTION

The M54914FP is a Bi-CMOS semiconductor integrated circuit consisting of an F2F demodulator for magnetic stripe card readers.

FEATURES

- Low power dissipation (standby current 1mA typ)
- Ignore bit selector input (bits 4, 8, 16)
- Output polarity (low-active, high-active) selector input
- Compact mini-molded pacage
- Wide operating temperature range T_a=−20∼+75℃

APPLICATION

Magnetic stripe card reader

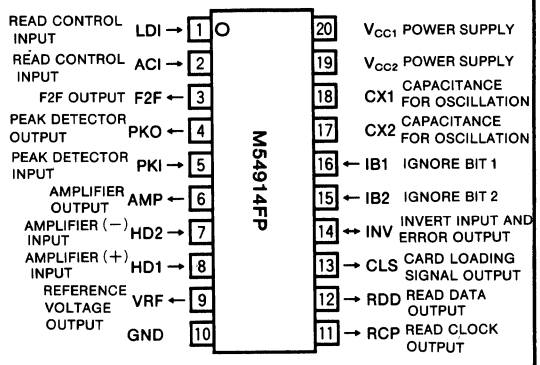
FUNCTION

The data signal read from a magnetic stripe card by a magnetic head is applied to HD-1 and HD-2. It is converted to an F2F pattern signal by analog processing in an amplifier OP1, peak detector OP2, and waveform regulator OP3. The bit numbers set by inputs IB1 and IB2 are ignored and the data receives digital processing to generate the card lording signal CLS, read clock signal RCP, read data signal RDD and error signal ERR (shared by INV pin). Outputs CLS, RCP and RDD are changed from low-active to high-active when INV is set low.

● Reference bit

N is the number of bits ignored by inputs IB1 and IB2.

PIN CONFIGURATION (TOP VIEW)



Outline 20P2

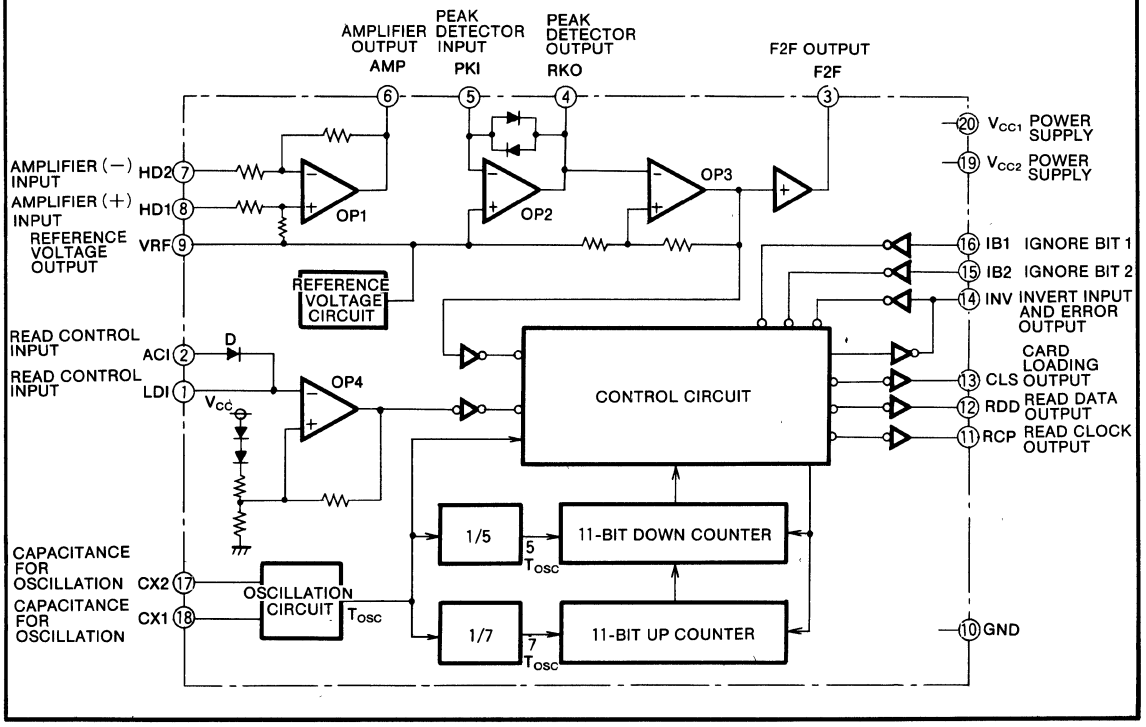
The reference bit is the bit from the Nth flux change to the Nth +1 flux change when input LDI changes from low to high and time width T_{BO} is bit 0. The bits following this reference bit are treated as data bits.

When an error signal ERR is output, that bit becomes the reference bit.

● Logic determination

T_{BN} is the time width of a data bit. If a "1" flux change is found between the flux change at the end of one bit (the beginning of the next bit) and 5/7 T_{BN}, the next bit (B_{n+1})

BLOCK DIAGRAM



is determined to be 1 ; if no flux change is found, the bit is determined to be 0. If two flux changes are found, error signal ERR is output.

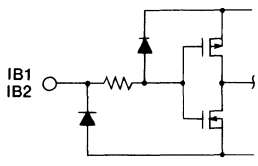
● Time width of the output signal

When the oscillation period of the oscillator is T_{OSC}, the output signals have the following widths ;

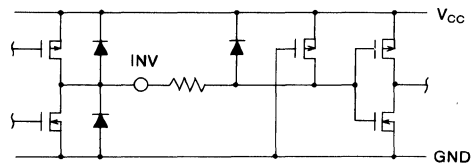
- Output pulse width of RCP, ERR ····· approx. $16T_{OSC}$
- RCP delay time width respect to RDD ··· approx. $8T_{OSC}$

I/O CIRCUIT

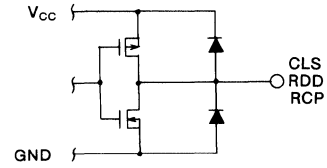
IB 1, IB 2 INPUT CIRCUIT



INV I/O CIRCUIT



CLS, RDD, RCP OUTPUT CIRCUIT



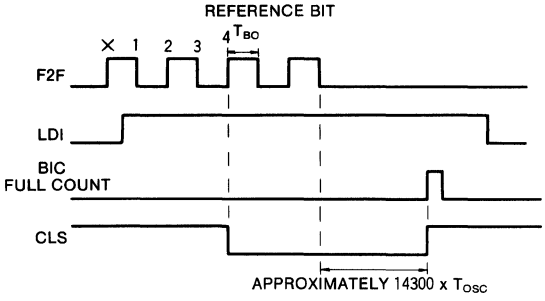
PIN DESCRIPTION

Pinnumber	Symbol	Name	Description
1	LDI	Read control input	Comparator input with hysteresis. When low, it resets the internal digital circuit. When high, F2F demodulation is possible.
2	ACI	Read cotrol input	Read control input connected to LDI using a diode.
3	F2F	F2F output	F2F signal output magnetic head signal after amplification, peak detection and waveform regulation.
4	PKO	Peak detector output	Noise filter C_{NF} is connected between PKI and PKO.
5	PKI	Peak detector input	Refer to PKI, PKO and F2F.
6	AMP	Amplifier output	Resistance RPK and capacitance CPK are connected between AMP and PKI.
7	HD2	Amplifier (−) input	The magnetic head is connected between HD1 and HD2.
8	HD1	Amplifier (+) input	The magnetic head is connected between HD1 and HD2.
9	VRF	Reference voltage output	1/2 V_{CC} reference voltage output
10	GND	GND	
11	RCP	Read clock output	Clock pulse output after F2F demodulation
12	RDD	Read data output	Data output after F2F demodulation
13	CLS	Card loading signal output	signal output to indicate a running card
14	INV	Invert input and error	When high or open, CLS, RDD and RCP outputs become low-active , when low, CLS, RDD and RCD become high-active Shared with error output pin ERR
15	IB2	Ignore bit 2	Pin to set ignore bits
16	IB1	Ignore bit 1	Pin to set ignore bits
17	CX2	Capacitance for oscillation	Capacitance C_{OSC} is connected between CX1 and CX2 to set the oscillation frequency
18	CX1	Capacitance for oscillation	Capacitance C_{OSC} is connected between CX1 and CX2 to set the oscillation frequency.
19	V_{CC2}	Power supply	Power supply pin for digital circuit. Supply voltage is V_{CC}
20	V_{CC1}	Power supply	Power supply pin for analog circuit Supply voltage is V_{CC} (same as V_{CC} 2).

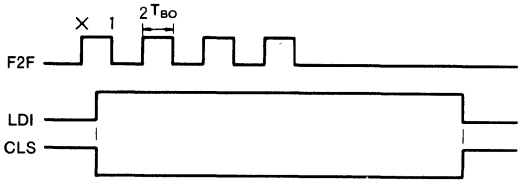
SETTING AND TIMING OF IGNORE BITS USING IB1 AND IB2

IB2 input	IB1 input	Ignore bit number	Description
L	L	4	• When LDI input is, low, the internal digital circuit is reset • LDI input can always be high • With the low-active setting, output CLS becomes low after flux changes (state changes of F2F) corresponding to the number of ignored bits have been counted , CLS becomes high when the BIC (bit interval count) is fully counted.
L	H	8	
H	L	16	
H	H	2	• When input LDI is low, the internal digital circuit is reset. • Output CLS is determined by the timing of input LDI.

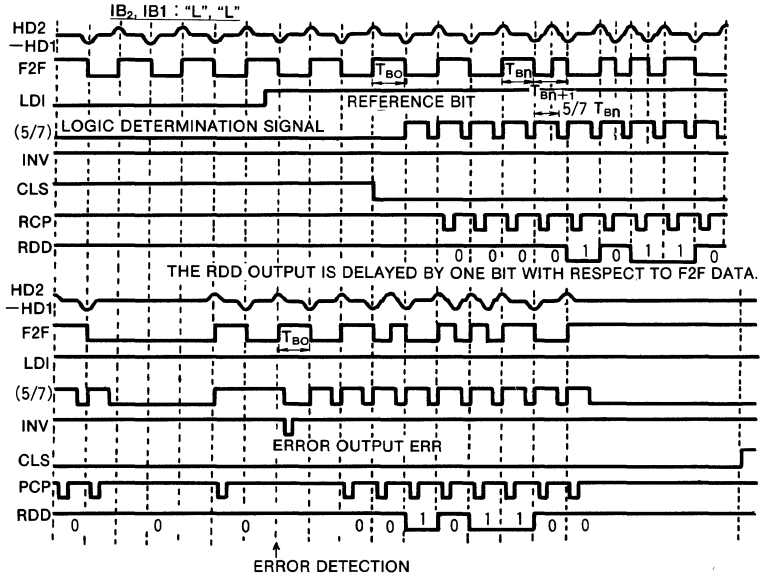
○IB2, IB1 : "L", "L"



○IB2, IB1 : "H", "H"



OPERATIONAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼+7.0	V
V_I	Input voltage	LDI, IB1, IB2	−0.3∼V_{CC}+0.3	V
V_O	Output voltage	INV, CLS, RDD, RCP	−0.3∼V_{CC}+0.3	V
I_I	Input current	ACI, LDI, IB1, IB2	−10∼+10	mA
I_O	Output current	INV, CLS, RDD, RCP	−10∼+10	mA
V_{ID}	Differential input voltage	Between HD1 and HD2	−0.6∼+0.6	V
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC} (Note 1)	Supply voltage	V_{CC1}, V_{CC2}	4.0	5	6.0	V
V_I	Input voltage	LDI	0		V_{CC}	V
V_{IH} (Note 2)	High-level input voltage	IB1, IB2	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	IB1, IB2, INV	0		0.3V_{CC}	V
V_{OH}	High-level output voltage	INV, CLS, RDD, RCP			V_{CC}	V
I_{OL}	Low-level output current	INV, CLS, RDD, RCP			5	mA
V_{IN}	Differential input voltage	HD2−HD1	3		80	mV_{PP}
f_{IN}	Input frequency	HD2−HD1	0.3		15	kHz
f_{OSC}	Oscillation frequency		0.2		2	MHz
C_{OSC} (Note 3)				33		pF
R_{PK} (Note 3)				470		Ω
C_{PK} (Note 3)				0.033		μF
C_{NF} (Note 3)				470		pF
R_{PF} (Note 3)				4.7		MΩ
C_{VC} (Note 4)				0.1		μF
C_{VR} (Note 4)				1		μF

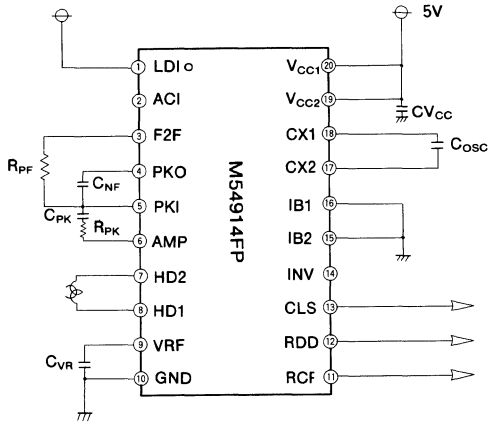
Note 1. V_{CC1} and V_{CC2} are equal.
2. A high input voltage cannot be applied externally as the INV pin is used for both input and output.
3. Reference value at 210BPI
4. Reference value
5. Typical values are at T_a = 25℃.

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test coditions		Test circuit	Limits			Unit
						Min	Typ	Max	
V_{TH}	Threshold voltage	IB1, IB2, INV	V_{CC}=5V		—	0.3V_{CC}		0.7V_{CC}	V
V_{OL}	Low-level output voltage	INV, CLS, RDD	V_{CC}=4V	I_{OL}=10μA	2			0.2	V
		RCP		I_{OL}=5mA	2			0.4	V
V_{OH}	High-level output voltage	INV, CLS, RDD	V_{CC}=4V	I_{OH}=−10μA	2	3.5			V
		RCP		I_{OH}=−100μA	2	2.8			V
I_{IL}	Low-level input current	IB1, IB2	V_{CC}=6V, V_I=1.8V		2	−10		+10	μA
I_{IL}	Low-level input current	INV	V_{CC}=6V, V_I=1.8V		2	−40			mA
I_{IH}	High-level input current	IB1, IB2	V_{CC}=6V, V_I=4.2V		2	−10		+10	μA
V_{REF}	Reference voltage	VRF	V_{CC}=5V, V_{IN}=0mV_{PP}		1	2.3	2.5	2.7	V
G_{V11}	Voltage gain 1	OP1	V_{CC}=5V, f_{IN}=1kHz, V_{IN}=80mV_{PP}		3	18	20	24	V/V
G_{V21}	Voltage gain 2	OP1	V_{CC}=5V, f_{IN}=15kHz, V_{IN}=80mV_{PP}		3	18	20	24	V/V
R_{IN1}	Input resistance	OP1	V_{CC}=5V, f_{IN}=1kHz, V_{IN}=80mV_{PP}		3	6	10	15	kΩ
V_{OPP1}	Maximum output voltage	OP1	V_{CC}=5V, f_{IN}=1kHz, THD_{AMP}=5%		3	2			V_{PP}
I_{IB2}	Input bias current	OP2	V_{CC}=5V		4			0.1	μA
V_{CL+2}	Positive clamp current	OP2	V_{CC}=5V, I_{PKI}=0.5mA		4	0.5		0.9	V
V_{CL-2}	Negative clamp current	OP2	V_{CC}=5V, I_{PKI}=0.5mA		4	−0.9		−0.5	V
V_{TH+3}	Positive threshold voltage	OP3	V_{CC}=5V		5	80		150	mV
V_{TH-3}	Negative threshold voltage	OP3	V_{CC}=5V		5	−150		−80	mV
V_{TH3}	Threshold difference voltage	OP3	$V_{TH3}=V_{TH+3}-\lvert V_{TH-3}\rvert$		5	−30		+30	mV
V_{OL3}	Low-level output voltage	F2F	V_{CC}=5V, V_{PKI}=2V, I_{F2F}=0.5mA		5			0.5	V
V_{OH3}	High-level output voltage	F2F	V_{CC}=5V, V_{PKI}=3V, I_{F2F}=−0.5mA		5	4.5			V
V_{F4}	Diode forward voltage	OP4	V_{CC}=5V, V_{LDI}=0V, I_{ACI}=0.5mA		6	0.55		1.1	V
I_{R4}	Diode reverse current	OP4	V_{CC}=5V, V_{LDI}=5V, V_{ACI}=0V		6	−0.5			μA
I_{IN4}	Input current	OP4	V_{CC}=5V, V_{ACI}=0V, V_{LDI}=0V		6	−0.5			μA
V_{TH+4}	Positive threshold voltage	OP4	V_{CC}=5V, V_{ACI}=0V		6	1.6	1.85	2.1	V
V_{TH-4}	Negative threshold voltage	OP4	V_{CC}=5V, V_{ACI}=0V		6	1.2	1.5	1.7	V
V_{TH4}	Threshold difference voltage	OP4	V_{CC}=5V, V_{ACI}=0V		6	0.25	0.35	0.5	V
I_{CCW}	Standby circuit current		V_{CC}=5V, V_{IN}=0mV_{PP}		1		1.0	1.4	mA
I_{CCR}	Operating circuit current		V_{CC}=5V, V_{IN}=80mV_{PP}, f_{IN}=5kHz f_{OSC}=1MHz		1		2.0	3.0	mA
f_{OSC}	Oscillation frequency		V_{CC}=5V, C_{OSC}=33pF		1	0.6		1.5	MHz
T_{OW}	Output pulse width	INV, RCP	V_{CC}=5V, f_{OSC}=1MHz		7	15	16	17	μs
T_{OD}	Delay time between outputs	RDD, RCP	V_{CC}=5V, f_{OSC}=1MHz		7	7	8	9	μs
T_{NW}	Input noise width	INV	V_{CC}=5V		7	2			μs

APPLICATION EXAMPLE

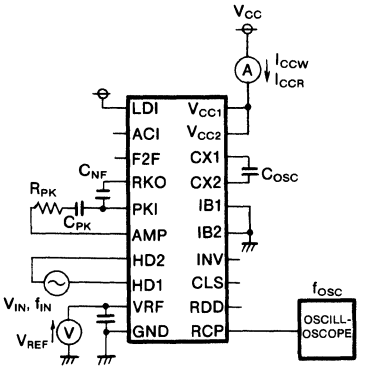
When the 4th bit is ignored and the output is low-active

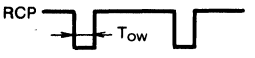


TEST CIRCUIT

In the following figs., C_{OSC}=33pF, R_{PK}=470Ω, C_{PK}=0.033μF, C_{NF}=470pF, C_{VR}=1μF

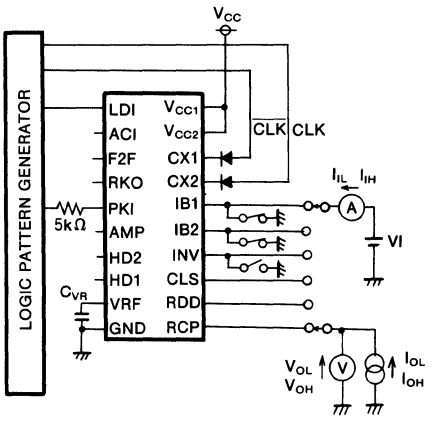
1 • V_{REF}, I_{CCW}, I_{CCR}, f_{OSC} test





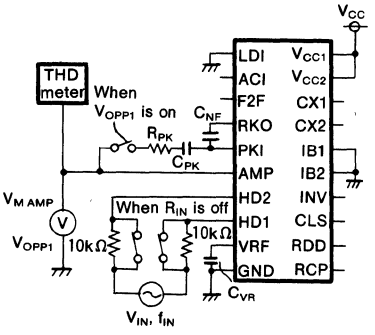
$$f_{OSC}=\frac{16}{T_{OW}}$$

2 • V_{OL}, V_{OH}, I_{IL}, I_{IH} test



Note : IB1 and IB2 must be connected to GND when these pins are not used for testing

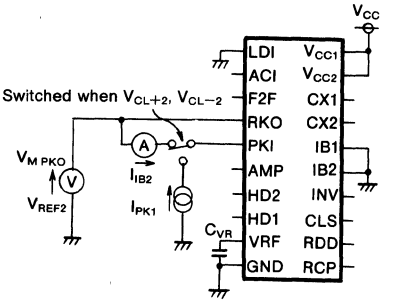
3 • G_{V11}, G_{V21}, R_{IN1}, V_{OPP1} test



$$G_{V11}=\frac{V_{M\,AMP}}{V_{IN}}$$

$$R_{IN1}=\frac{2\,V_{M\,AMP}}{G_{V11}\cdot V_{IN}-V_{M\,AMP}}\times 10\ (k\Omega)$$

4 • I_{IB2}, V_{CL+2}, V_{CL-2} test



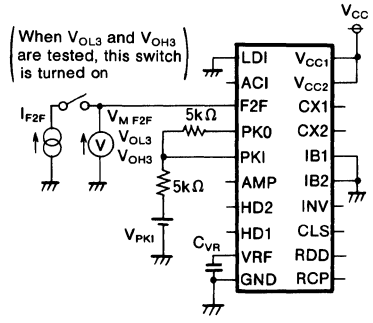
$$V_{CL+2},\ V_{CL-2}=V_{M\,PKO}-V_{REF2}$$

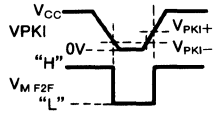
Note : V_{REF2} is $V_{M\,PKO}$ when V_{CC}=5V

MITSUBISHI ELECTRIC

F2F MAGNETIC STRIPE ENCORDING CARD READER

5 • V_{TH+3}, V_{TH-3}, V_{TH3}, V_{OL3}, V_{OH} test





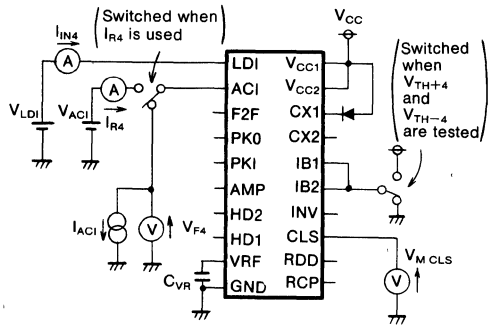
$V_{TH+3}=V_{REF2}-V_{PKI-}$

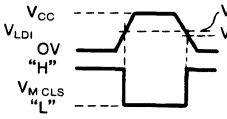
$V_{TH-3}=V_{REF2}-V_{PKI+}$

$V_{TH}=V_{TH+3}-|V_{TH-3}|$

Note : V_{REF2} is measured in test circuit 4

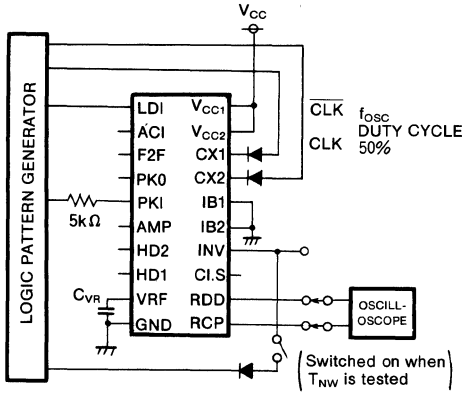
6 • V_{F4}, I_{R4}, I_{IN4}, V_{TH+4}, V_{TH-4}, V_{TH14} test

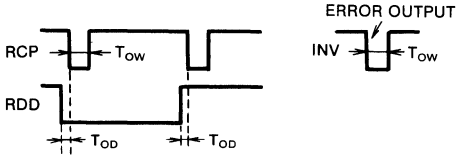


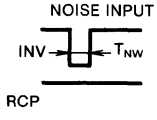


$V_{TH4}=V_{TH+4}-V_{TH-4}$

7 • T_{OW}, T_{OD}, T_{NW} test







T_{NW} is the maximum time width of negative noise entering the INV input which is not considered to be an INV input

M54927P

PLL FREQUENCY SYNTHESIZER FOR DIGITAL TUNING SYSTEMS

DESCRIPTION

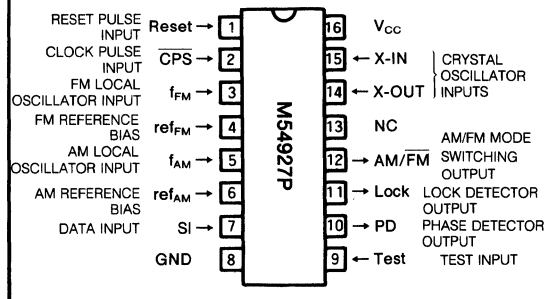
The M54927P is a semiconductor integrated circuit consisting of a PLL frequency synthesizer for use in AM/FM electronically tuned radio receivers. It makes use of ECL-IIL process to enable high density and low power consumption. It contains an FM Prescaler allowing the direct input of the local oscillator frequency signal.

The base frequency is provided by a 4.5MHz crystal oscillator.

FEATURES

- Built-in FM high-speed prescaler (f_{max}=130MHz)
- Low power consumption (I_{CC} = 20mA, typical at V_{CC} = 5V)
- Reference frequency selectable from eight values (100K, 50K, 25K, 12.5K, 10K, 9K, 5K, 1K)
- Modulo-2 swallow counter in FM mode (prescaler ratio 1/32, 1/33)
- Wide range of division ratios (FM=1024~65535, AM= 32~2047, binary coded)
- Built-in 4.5MHz crystal oscillator (only two external components required)
- PLL lock/unlock status output
- AM/FM mode control output
- High sensitivity AM/FM local oscillator frequency input with built-in amplifier (FM: 160mV$_{P-P}$ at 130MHz, AM: 100mV$_{P-P}$ at 4MHz)
- Serial data input

PIN CONFIGURATION (TOP VIEW)



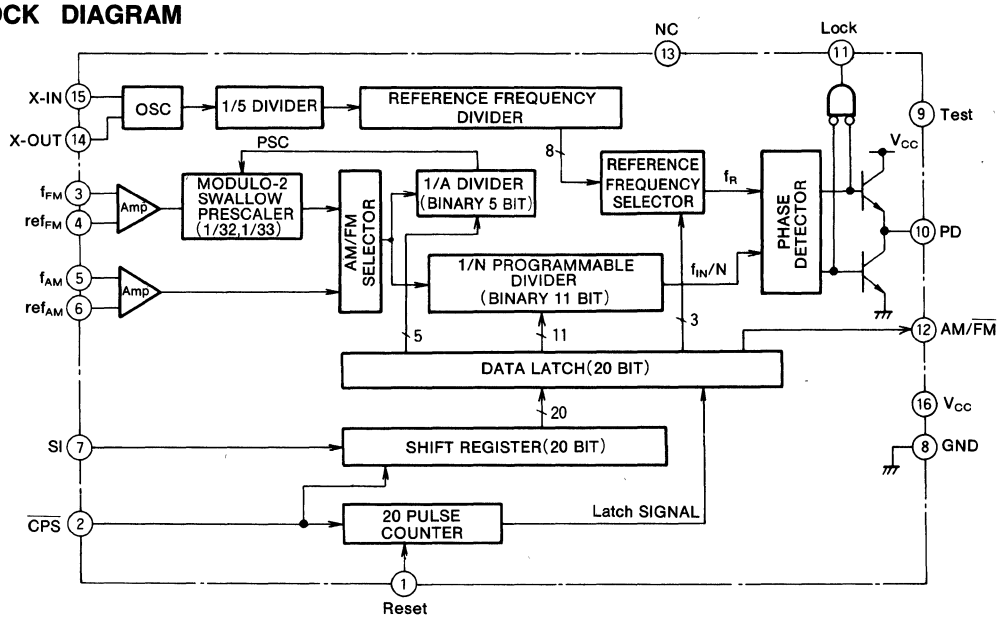
Outline 16P4

NC : No connection

APPLICATION

AM/FM Radios

BLOCK DIAGRAM



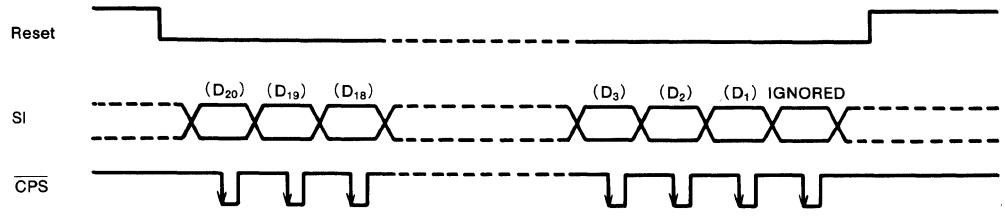
MITSUBISHI ELECTRIC

PIN DESCRIPTION

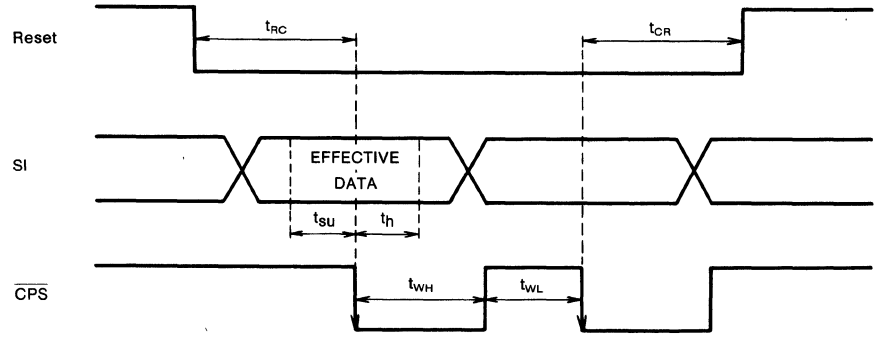
No.	Symbol	Name	Description
1	Reset	Reset pulse input	20 pulse counter reset pulse input
2	$\overline{CPS}$	Clock pulse input	Shift register clock pulse input
3	f_{FM}	FM local oscillator input	Direct input enable (f_{max}=130MHz) Built-in amplifier (input sensitivity 160mV_{P-P})
4	ref_{FM}	FM reference bias	Grounded through 1000pF capacitor
5	f_{AM}	AM local oscillator input	Built-in amplifier (input sensitivity 100mV_{P-P})
6	ref_{AM}	AM reference bias	Grounded through 10000pF capacitor
7	SI	Data input	Serial data input
8	GND	Ground	0V
9	Test	Test input	Normally, set to the low-state. When it is in the high-state, pin 10 (PD) becomes the reference frequency output and pin 11 (Lock) is the programmable divider output.
10	PD	Phase detector output	Tri-state output. High-state for phase lead, low state for phase lag and phase coincidence for high-Z
11	Lock	Lock detector output	High-state when PD is high-Z. Low-state when PD is high or low state. Open collector output
12	AM/$\overline{FM}$	AM/FM mode switching output	Low for FM and High for AM Open collector output
13	NC		No connection
14	X-OUT	Crystal oscillator inputs	4.5MHz Crystal
15	X-IN		
16	V_{CC}	Power supply	4.5~5.5V

DESCRIPTION OF OPERATION

1. Data Input

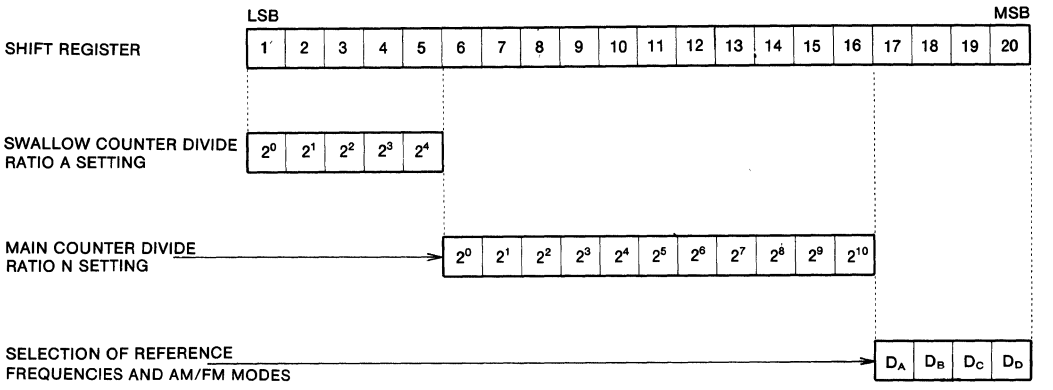


Note 1 : After the reset input goes low, 20 bits of data are read by means of 20 $\overline{CPS}$ input pulses (negative edge triggered).
2 : When the reset input is high, $\overline{CPS}$ input pulses and SI input data are ignored
3 : After the twentieth $\overline{CPS}$ input pulse goes low, all date(Divide ratio, Mode and Reference frequency)are simultaneously set. Date for the 21 and following $\overline{CPS}$ input pulses are ignored.



$t_{su}=t_h=t_{WH}=t_{WL}=10\mu$Smin.
$t_{RC}=t_{CR}=20\mu$Smin.

2. Data Coding



Note 4 : For FM mode, the programmable divider acts as a Modulo-2 swallow counter. The divide ratio is determined by the main counter divide ratio N (binary 11 bit) and the swallow counter divide ratio A (binary 5 bit). Overall divide ratio M is determined by M=A+32N.

5 : For AM mode, the programmable divider acts as a normal presettable counter. The divide ratio is given by N (binary 11 bit). For this mode, the swallow counter divide ratio A is ignored.

6 : The selection of reference frequencies and AM/FM modes is as described in Table 1.

Table 1. Reference frequency and AM/FM mode selection

Data				Mode	Reference frequency	Test="H" (Note 7)	
D_A	D_B	D_C	D_D			PD	Lock
L	L	L	L	FM	100k	100k	f_{FM}/M
H	L	L	L	FM	50k	50k	f_{FM}/M
L	H	L	L	FM	25k	25k	f_{FM}/M
H	H	L	L	FM	12.5k	12.5k	f_{FM}/M
L	L	H	L	FM	10k	10k	f_{FM}/M
H	L	H	L	FM	9k	9k	f_{FM}/M
L	H	H	L	FM	5k	5k	f_{FM}/M
H	H	H	L	FM	1k	1k	f_{FM}/M
L	L	L	H	AM	100k	100k	f_{AM}/N
H	L	L	H	AM	50k	50k	f_{AM}/N
L	H	L	H	AM	25k	25k	f_{AM}/N
H	H	L	H	AM	12.5k	12.5k	f_{AM}/N
L	L	H	H	AM	10k	High	f_{AM}/N
H	L	H	H	AM	9k	Low	f_{AM}/N
L	H	H	H	AM	5k	High-Z	f_{AM}/N
H	H	H	H	AM	1k	High-Z	900kHz/N

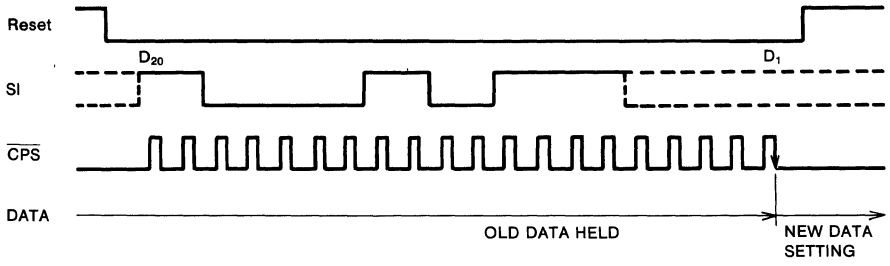
Note 7 : When pin 9 (Test) is set to high-state, pin 10 (PD) is the reference frequency output and pin 11 (Lock) is the programmable divider output

3. Data Coding Example

(1) AM mode, Reference frequency 10KHz, N=207

SHIFT REGISTER DATA

	LSB																		MSB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	X	X	X	X	X	H	H	H	H	L	L	H	H	L	L	L	L	L	H	H
	SWALLOW COUNTER DIVIDE RATIO A IGNORED X : "H" or "L"					MAIN COUNTER DIVIDE RATIO N SETTING $N=2^0+2^1+2^2+2^3+2^6+2^7=207$											AM MODE REFERENCE FREQUENCY 10KHz IS SELECTED			

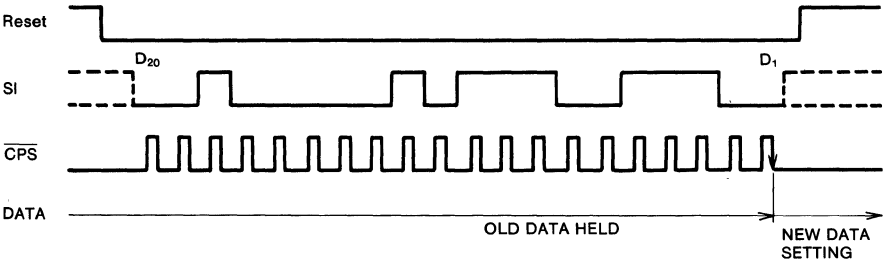


Note 8 : If the PLL goes into lock, $f_{AM}=10\times207=2070KHz$

(2) FM Mode, Reference frequency 25KHz, N=2972

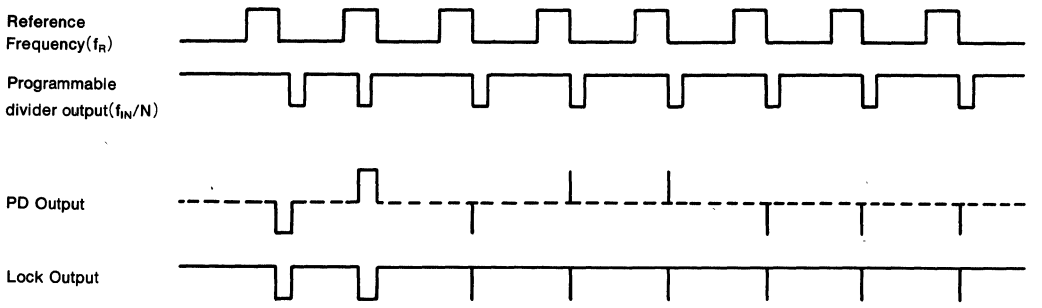
SHIFT REGISTER DATA

	LSB																		MSB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	L	L	H	H	H	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L
	SWALLOW COUNTER DIVIDE RATIO A SETTING $A=2^2+2^3+2^4=28$					MAIN COUNTER DIVIDE RATIO N SETTING $N=2^2+2^3+2^4+2^6=92$											FM MODE REFERENCE FREQUENCY 25KHz IS SELECTED.			



Note 9 : Overall divide ratio M is given by $M=A+32N=28+32\times92=2972$.
10 : If the PLL goes into lock, $f_{FM}=25\times2972=74300MHz$
$=74.3MHz$.

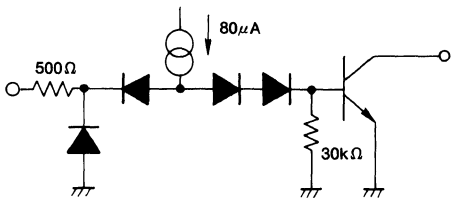
4. PD and Lock signal Output



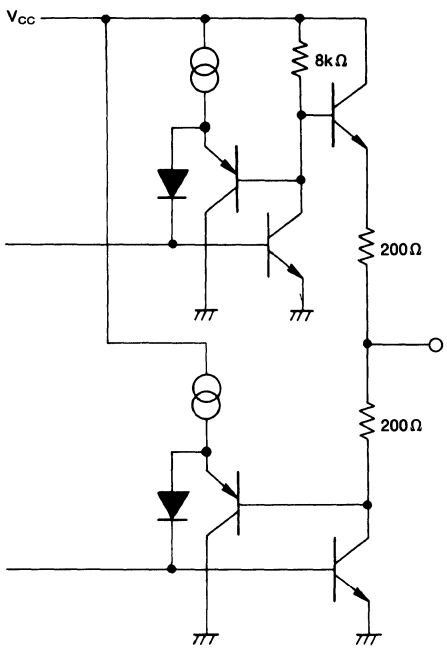
Note 11 : When the programmable divider output($f_{IN} \div N$)lags the reference frequency(f_R), the PD output is low. When it leads, the PD output becomes high
12 : The broken line indicates the high impedance state.
13 : When PD is high or low state, Lock output becomes low.

INPUT/OUTPUT CIRCUITS

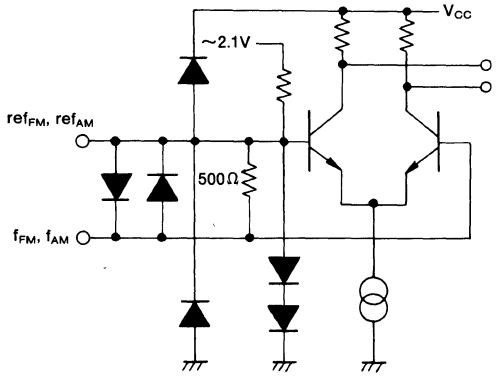
1 Reset, $\overline{CPS}$, SI, Test Inputs



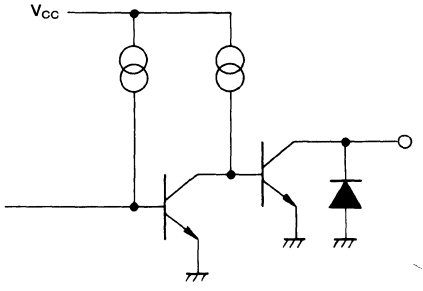
2 PO Output



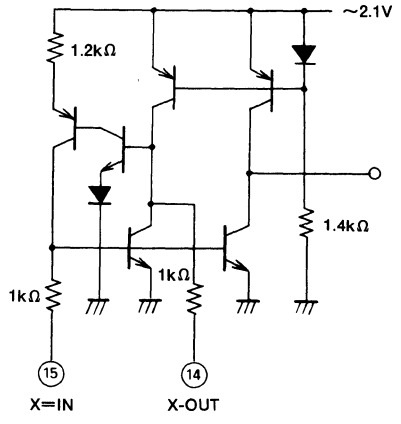
3 f_{FM}, f_{AM} Inputs



4 AM/$\overline{FM}$, Lock, 500Hz Outputs



5 OSC Circuit



Note 14 : Resistance and current values are typical values for Ta=25℃.

PLL FREQUENCY SYNTHESIZER FOR DIGITAL TUNING SYSTEMS

ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

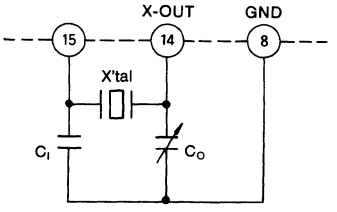
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+6	V
V_I	Input voltage		−0.5∼+6	V
V_O	Output voltage		−0.5∼+6	V
Pd	Power dissipation	T_a=75℃	300	mW
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.5∼5.5V, T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			4.5 (3)*	5	5.5	V
f_{Local}	Input frequency	f_{AM} sinewave		0.5	—	4	MHz
		f_{FM} sinewave		8	—	130	
V_{Local}	Input amplitude	f_{AM}	0.5∼2MHz	200		800	mV_{P-P}
			2∼4MHz	100		800	
		f_{FM}	8∼60MHz	400		800	
			60∼130MHz	160		800	
I_{OL}	Low-level output current	Pin 12, 13 outputs			1	5	mA
f_{OSC}	Reference oscillator frequency				4.5		MHz

* : 3V, T_a=25℃

CRYSTAL ELEMENT CONNECTION CIRCUIT



Note 15 : Crystal specifications

Resonant frequency	4.5MHz±30ppm
Load capacitance	20pF
Effective resistance	100Ω max.

16 : Capacitance values
C_I=56pF
C_O=30pF(trimmer)

ELECTRICAL CHARACTERISTICS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage	1, 2, 7, 9	V_{CC}=5.5V	2			V
V_{IL}	Low-level input voltage	1, 2, 7, 9	V_{CC}=5.5V			0.6	V
I_{IH}	High-level input current	1, 2, 7, 9	V_{CC}=5.5V, V_{IH}=5.5V			30	μA
I_{IL}	Low-level input current	1, 2, 7, 9	V_{CC}=4.5V, V_{IL}=0V		−80	−160	μA
V_{OL}	Low-level output voltage	11, 12	V_{CC}=4.5V, I_{OL}=5mA			0.5	V
V_{OHP1}	PD high-level output voltage	10	V_{CC}=4.5V, I_{OH}=−1mA	3			V
V_{OHP2}	PD high-level output voltage	10	V_{CC}=5V, I_{OH}=−0.1mA	4			V
V_{OLP1}	PD low-level output voltage	10	V_{CC}=4.5V, I_{OL}=1mA			1.5	V
V_{OLP2}	PD low-level output voltage	10	V_{CC}=5V, I_{OL}=0.1mA			1	V
I_{PD1}	PD leakage current	10	V_{CC}=5.5V, V_O=0.8∼4.7V			±1	μA
I_{PD2}	PD leakage current	10	V_{CC}=5V, V_O=2.5V			±100	nA
I_{CC}	Circuit current		V_{CC}=5.5V		20	35	mA
I_{OIK}	Output leakage current	11, 12	V_{CC}=5.5V, V_{OH}=5.5V			30	μA

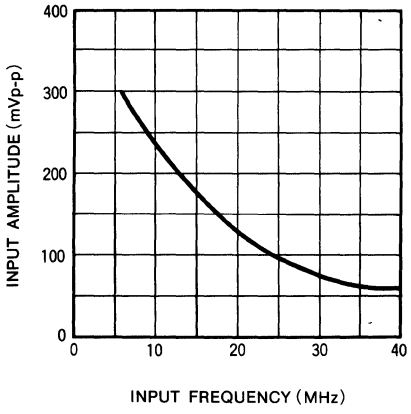
Note 17 : All voltages are measured with respect to circuit ground (pin 8) at 0V
18 : Currents are taken to be positive when flowing into the circuit and negative when flowing out of the circuit, the minimum and maximum values taken to be absolute values.
* : A Typical value at T_a=25℃

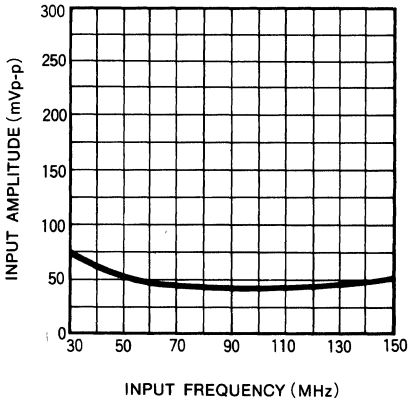
AC CHARACTERISTICS (T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{FM1}	FM input sensitivity	3	$V_{CC1}=V_{CC2}=4.5V$ $f_{FM}=60\sim130MHz$			160	mV_{P-P}
V_{FM2}	FM input sensitivity	3	$V_{CC1}=V_{CC2}=4.5V$ $f_{FM}=8\sim60MHz$			400	mV_{P-P}
V_{AM1}	AM input sensitivity	5	$V_{CC1}=V_{CC2}=4.5V$ $f_{AM}=2\sim4MHz$			100	mV_{P-P}
V_{AM2}	AM input sensitivity	5	$V_{CC1}=V_{CC2}=4.5V$ $f_{AM}=0.5\sim2MHz$			200	mV_{P-P}

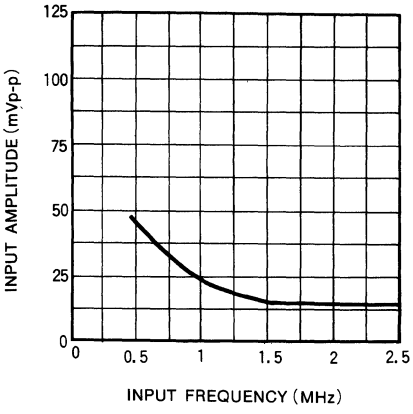
TYPICAL INPUT SENSITIVITY CHARACTERISTICS ($V_{CC1}=V_{CC2}=5V$, Ta=25℃)

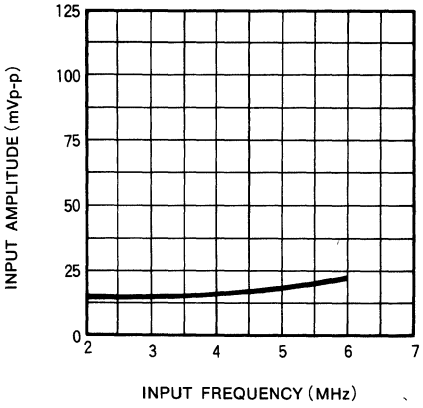
(1) MINIMUM FM INPUT AMPLITUDE VS INPUT FREQUENCY



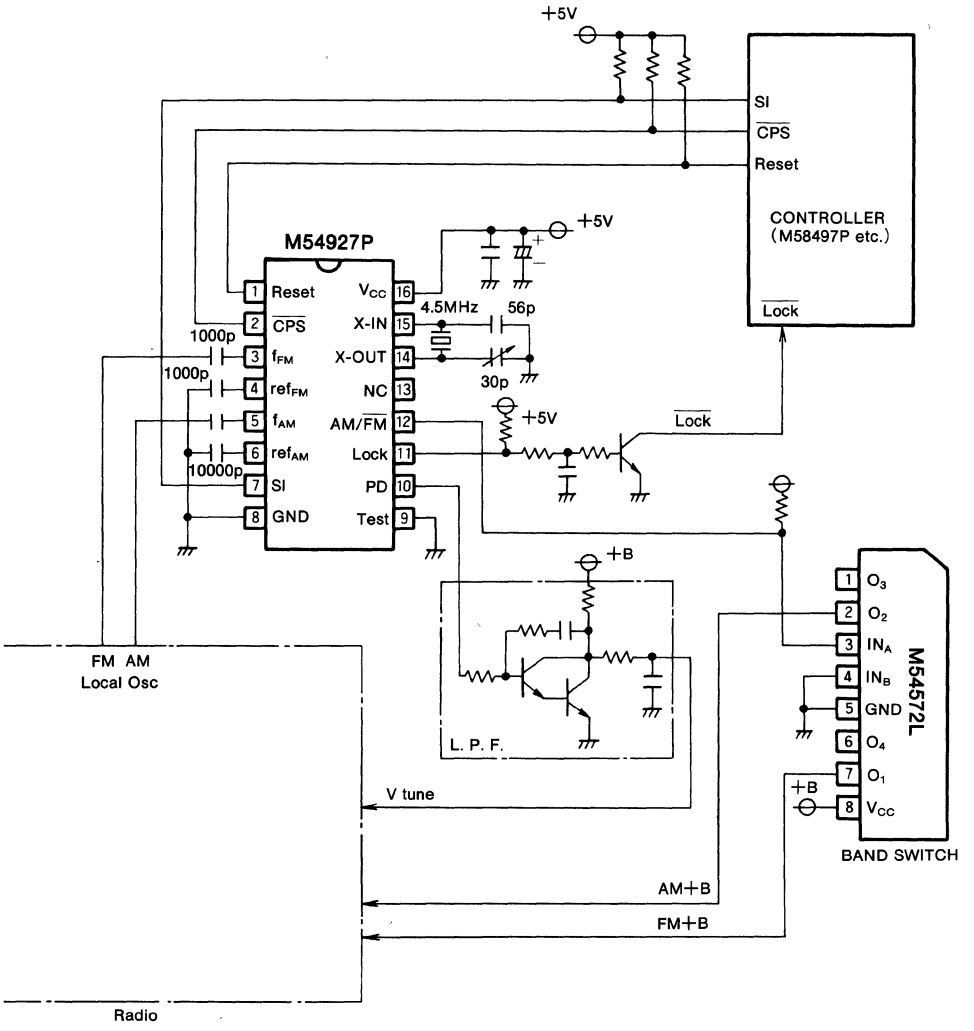


(2) MINIMUM AM INPUT AMPLITUDE VS INPUT FREQUENCY





APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M54928P

PLL FREQUENCY SYNTHESIZER FOR DIGITAL TUNING SYSTEMS

DESCRIPTION

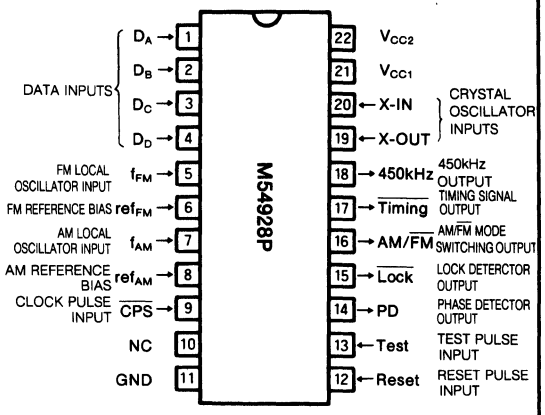
The M54928P is a semiconductor integrated circuit consisting of a PLL frequency synthesizer for use in AM/FM electronically tuned radio receivers. It makes use of ECL-IIL process to enable high density and low power consumption. It contains an FM Prescaler allowing the direct input of the local oscillator frequency signal.

The base frequency is provided by a 4.5MHz crystal oscillator.

FEATURES

- Built-in FM high-speed prescaler (f_{max}=130MHz)
- Low power consumption (I_{CC} = 20mA, typical at V_{CC} = 5V)
- Reference frequency selectable from eight values (50k, 25k, 12.5k, 10k, 9k, 5k, 4.5k, 1k)
- Modulo-2 swallow counter in FM mode (prescaler ratio 1/32, 1/33)
- Wide range of division ratios (FM: 1024~65535, AM: 64 ~65535, binary coded)
- Clock pulse outputs at 450kHz and 500Hz
- Built-in 4.5MHz crystal oscillator (only two external components required)
- PLL rock/unlock status ouptut
- AM/FM mode control output
- High sensitivity AM/FM local oscillator frequency input with buiit-in amplifier (FM: 160mV$_{P-P}$ at 130MHz, AM: 100mV$_{P-P}$ at 4MHz)

PIN CONFIGURATION (TOP VIEW)



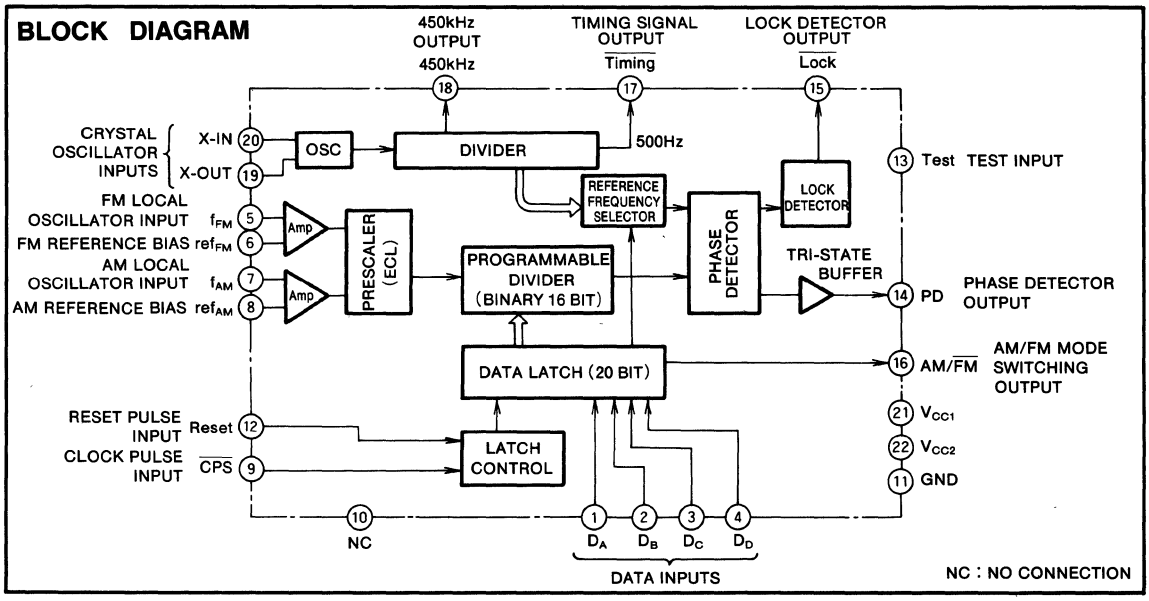
Outline 22P4

NC : No connection

APPLICATION

AM/FM Radios

BLOCK DIAGRAM



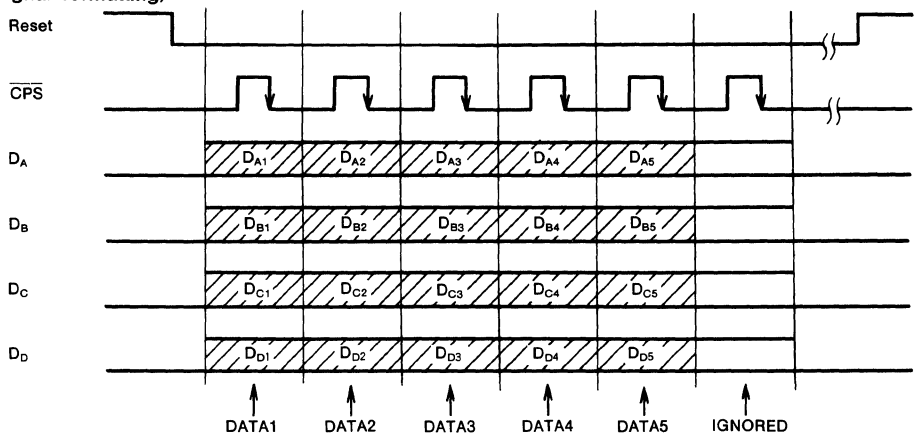
PIN DESCRIPTION

No.	Symbol	Name	Description
1	D_A	Data inputs	Divide ratio input for programmable divider.
2	D_B		
3	D_C		
4	D_D		
5	f_{FM}	FM local oscillator input	Direct input enable (f_{max} = 130MHz) Built-in amplifier (input sensitivity 160mV_{P-P})
6	ref_{FM}	FM reference bias	Grounded through 1000pF capacitor
7	f_{AM}	AM local oscillator input	Built-in amplifier (input sensitivity 100mV_{P-P})
8	ref_{AM}	AM reference bias	Grounded through 10000pF capacitor
9	$\overline{CPS}$	Clock pulse input	Data reading clock input
10	NC	No connection	
11	GND	Ground	0V
12	Reset	Reset pulse input	Data latch reset input
13	Test	Test input	Normally set to low-state. When set to high-state, pin 16 is the programmable divider output and pin 15 is the reference frequency output.
14	PD	Phase detector output	Tri-state output. Phase lead for high-state, phase lag for low-state and high-Z for phase coincidence.
15	$\overline{Lock}$	Lock detector output	Low for PLL lock and high for PLL unlock. Open collector output.
16	AM/$\overline{FM}$	AM/FM mode switching	AM/FM mode switching output. Low for FM and high for AM. Open collector output.
17	$\overline{Timing}$	Timing signal output	500Hz clock pulse output Open collector
18	450kHz	450kHz output	450kHz clock pulse output. Open collector
19	X-IN	Crystal oscillator inputs	4 5MHz crystal input
20	X-OUT		
21	V_{CC1}	Power supply 1	5V±0 5V
22	V_{CC2}	Power supply 2	5V±0 5V

DESCRIPTION OF OPERATION

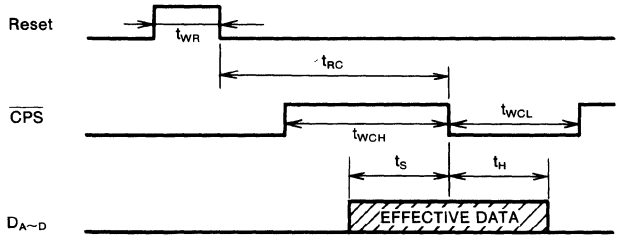
1. Data Input

(Input signal formatting)



Note 1 : After the reset input goes low, 4×5 bits of data are read by means of 5CPS input pulses (negative edge triggered).
2 : Data for the sixth and following CPS input pulses are ignored.
3 : When the Reset input is high, CPS input pulses and D_A~D_D input data are ignored.
4 : After the fifth CPS input pulse goes low, all data (Divide ratio, Mode and Reference frequency) are simultaneously set.

(Input signal timing)



MINIMUM VALUES
t_{WR}=10μs
t_{WCH}=t_{WCL}=10μs
t_{RC}=20μs
t_S=40μs
t_H=40μs

2. AM/FM Mode Setting and Reference Frequency Selection

AM/FM mode selection and reference frequency selection is performed by means of the data 5 (D_{A5}, D_{B5}, D_{C5}, D_{D5}).

When D_{A5} is read as a high level, the AM mode is selected, enabling the f_{AM} input as well (maximum input frequency 4MHz). For this mode the f_{FM} input is disabled.

When D_{A5} is read as a low level, the FM mode is selected, enabling the f_{FM} input as well (maximum input frequency 130MHz). For this condition the f_{AM} input is disabled.

The selection of reference frequencies is as described in table 1.

Table 1. Reference frequency selection

Data 5				Mode	Reference frequency	AM/$\overline{FM}$ output
D_{A5}	D_{B5}	D_{C5}	D_{D5}			
L	L	L	L	FM	50k	L
H	L	L	L	AM	50k	H
L	H	L	L	FM	25k	L
H	H	L	L	AM	25k	H
L	L	H	L	FM	12.5k	L
H	L	H	L	AM	12.5k	H
L	H	H	L	FM	5k	L
H	H	H	L	AM	5k	H
L	L	L	H	FM	4.5k	L
H	L	L	H	AM	4.5k	H
L	H	L	H	FM	9k	L
H	H	L	H	AM	9k	H
L	L	H	H	FM	1k	L
H	L	H	H	AM	1k	H
L	H	H	H	FM	10k	L
H	H	H	H	AM	10k	H

3. Divide Ratio Selection

The divide ratio of the programmable divider is set by means of data 1 through data 4. Binary data coding is used. The coding differs for AM and FM modes.

(1) AM mode

The programmable divider acts as a normal presettable counter. The divide ratio is set in a binary 16-bit coded format.

DIVIDE RATIO SETTING (BINARY 16-BIT)

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}
D_{A1}	D_{B1}	D_{C1}	D_{D1}	D_{A2}	D_{B2}	D_{C2}	D_{D2}	D_{A3}	D_{B3}	D_{C3}	D_{D3}	D_{A4}	D_{B4}	D_{C4}	D_{D4}

(2) FM mode

The programmable divider acts as a Modulo-2 swallow counter. The divide ratio is determined by the main counter divide ratio B (binary 12-bit) and the swallow counter divide ratio A (binary 4-bit).

MAIN COUNTER DIVIDE RATIO B SETTING (BINARY 12-BIT) — SWALLOW COUNTER DIVIDE RATIO A SETTING

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^0	2^1	2^2	2^3
D_{A1}	D_{B1}	D_{C1}	D_{D1}	D_{A2}	D_{B2}	D_{C2}	D_{D2}	D_{A3}	D_{B3}	D_{C3}	D_{D3}	D_{A4}	D_{B4}	D_{C4}	D_{D4}

Note 5 : Overall divide ration N is determined by N=A+16B

4. Data Coding Example

(1) AM mode, Reference frequency 10kHz, N=207

D_{A1}	D_{B1}	D_{C1}	D_{D1}	D_{A2}	D_{B2}	D_{C2}	D_{D2}	D_{A3}	D_{B3}	D_{C3}	D_{D3}	D_{A4}	D_{B4}	D_{C4}	D_{D4}	D_{A5}	D_{B5}	D_{C5}	D_{D5}
H	H	H	H	L	L	H	H	L	L	L	L	L	L	L	L	H	H	H	H
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}				

$N=2^0+2^1+2^2+2^3+2^6+2^7=1+2+4+8+64+128=207$

Note 6 : If the PLL goes into lock, $f_{AM}=10\times207=2070$kHz.

AM MODE SELECTION

REFERENCE FREQUENCY 10kHz IS SELECTED.

MITSUBISHI ELECTRIC

(2) FM mode, Reference frequency 25kHz, N=2972

D_{A1}	D_{B1}	D_{C1}	D_{D1}	D_{A2}	D_{B2}	D_{C2}	D_{D2}	D_{A3}	D_{B3}	D_{C3}	D_{D3}	D_{A4}	D_{B4}	D_{C4}	D_{D4}	D_{A5}	D_{B5}	D_{C5}	D_{D5}
H	L	L	H	H	H	L	H	L	L	L	L	L	L	H	H	L	H	L	L
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^0	2^1	2^2	2^3				

$B=2^0+2^3+2^4+2^5+2^7=1+8+16+32+118=185$

$A=12$

Note 7 : Overall divide ratio N is given by $N=A+16B$.
$=12+16+185$.
$=2972$.

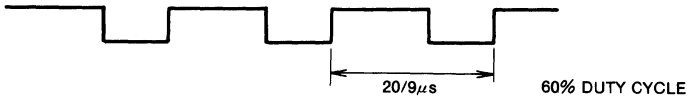
8 : If the PLL goes into lock $f_{FM}=25\times2972=74300$kHz.
$=74.3$MHz.

FM MODE SELECTION

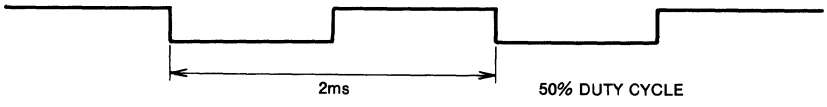
REFERENCE FREQUENCY 25kHz IS SELECTED.

5. Clock Signal Output Waveform

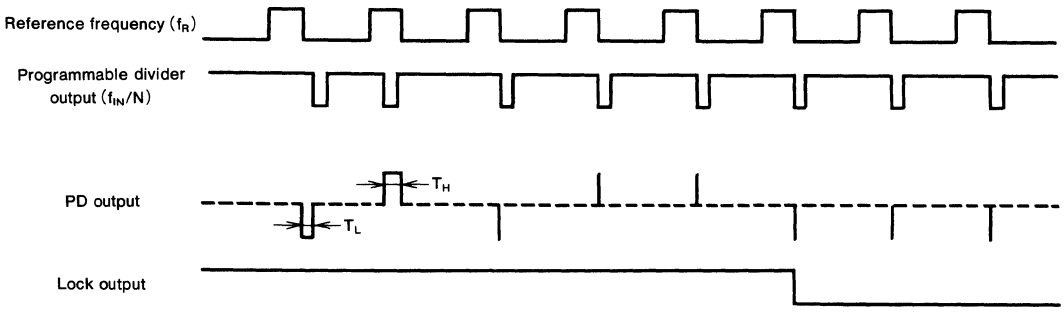
(1) 450kHz output (pin 18)



(2) Timing output (pin 17)



6. PD and Lock Signal Output



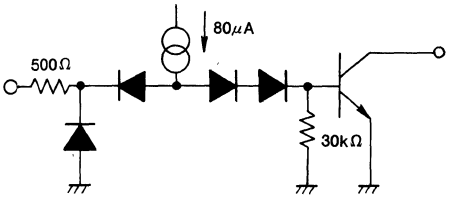
Note 9 : When the programmable divider output ($f_{IN}\div N$) lags the reference frequency (f_R), the PD output is low. When it leads, the PD output becomes high.

10 : If the phase difference T_L or T_H remains below 2.2μs for over three periods of the reference frequency, the lock output goes low indicating the lock condition

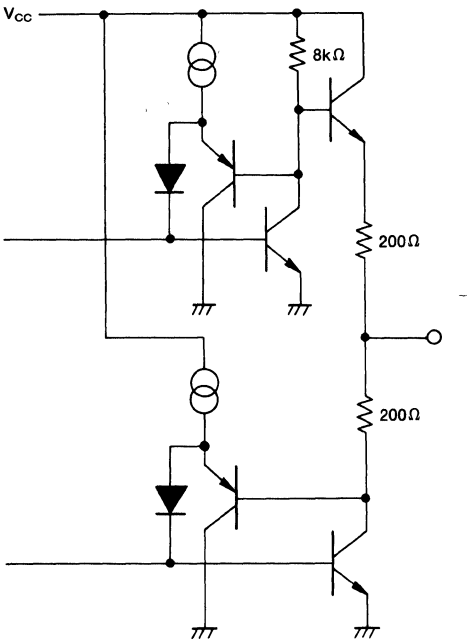
11 : The broken line indicates the high impedance state.

INPUT/OUTPUT CIRCUITS

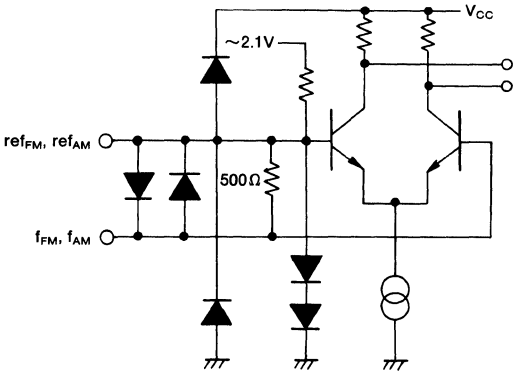
1 D_A, D_B, D_C, D_D, Test, $\overline{CPS}$, Reset Inputs



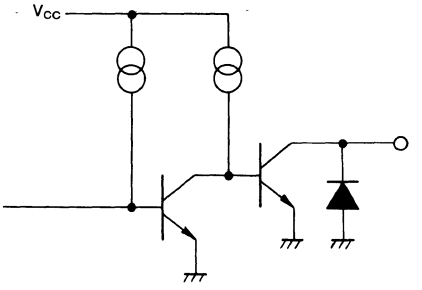
2 PD output



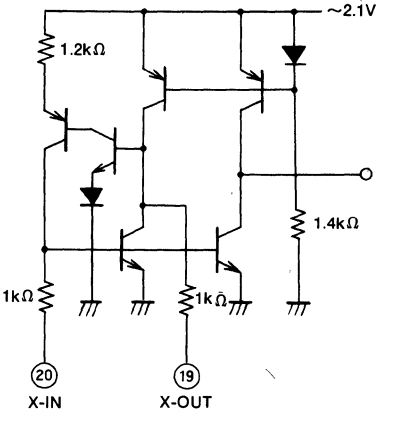
3 f_{FM}, f_{AM} Inputs



4 AM/$\overline{FM}$, $\overline{Lock}$, $\overline{Timing}$, 450kHz outputs



5 OSC circuit



Note 12 : Resistance and current values are typical values for T_a=25℃.

PLL FREQUENCY SYNTHESIZER FOR DIGITAL TUNING SYSTEMS

ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

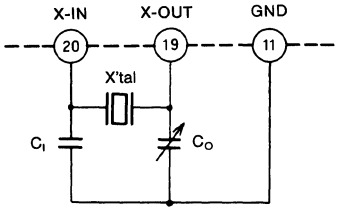
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	V_{CC1}, V_{CC2}	−0.5∼+6	V
V_I	Input voltage		−0.5∼+6	V
V_O	Output voltage		−0.5∼+6	V
P_d	Power dissipation	T_a=75℃	300	mW
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.5∼5.5V, T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage	V_{CC1}, V_{CC2}		4.5 (3)*	5	5.5	V
f_{Local}	Input frequency	f_{AM}		0.5	—	4	MHz
		f_{FM}		8	—	130	
V_{Local}	Input amplitude	f_{AM}	0.5∼2MHz	200		800	mV_{P-P}
			2∼4MHz	100		800	
		f_{FM}	8∼60MHz	400		800	
			60∼130MHz	160		800	
I_{OL}	Low-level output current	Pin 15, 16, 17, 18 outputs			1	5	mA
f_{OSC}	Reference oscillator frequency			—	4.5	—	MHz

* : 3V, T_a=25℃

CRYSTAL ELEMENT CONNECTION CIRCUIT



Note 13 : Crystal specifications
Resonant frequency 4.5MHz±30ppm
Load capacitance 20pF
Effective resistance 100Ω max
14 : Capacitance values
C_I=56pF
C_O=30pF (trimmer)

ELECTRICAL CHARACTERISTICS (T_a = −20∼+75℃, unless otherwise noted)

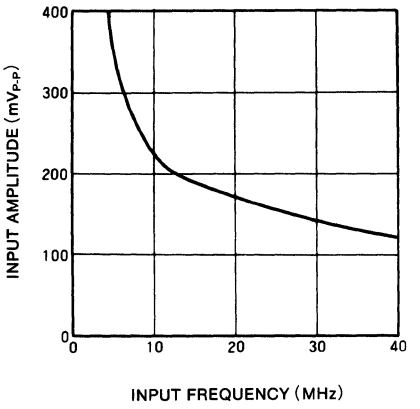
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage	1, 2, 3, 4, 9, 12, 13	V_{CC1}=V_{CC2}=5.5V	2			V
V_{IL}	Low-level input voltage	1, 2, 3, 4, 9, 12, 13	V_{CC1}=V_{CC2}=5.5V			0.6	V
I_{IH}	High-level input current	1, 2, 3, 4, 9, 12, 13	V_{CC1}=V_{CC2}=5.5V, V_{IH}=5.5V			30	μA
I_{IL}	Low-level input current	1, 2, 3, 4, 9, 12, 13	V_{CC1}=V_{CC2}=4.5V, V_{IL}=0V		−80	−160	μA
V_{OL}	Low-level output voltage	15, 16, 17, 18	V_{CC1}=V_{CC2}=4.5V, I_{OL}=5mA			0.5	V
V_{OHP1}	PD high-level output voltage	14	V_{CC1}=V_{CC2}=4.5V, I_{OH}=−1mA	3			V
V_{OHP2}	PD high-level output voltage	14	V_{CC1}=V_{CC2}=5V, I_{OH}=−0.1mA	4			V
V_{OLP1}	PD low-level output voltage	14	V_{CC1}=V_{CC2}=4.5V, I_{OL}=1mA			1.5	V
V_{OLP2}	PD low-level output voltage	14	V_{CC1}=V_{CC2}=5V, I_{OL}=0.1mA			1	V
I_{PD1}	PD leakage current	14	V_{CC1}=V_{CC2}=5.5V, V_O=0.8∼4.7V			±1	μA
I_{PD2}	PD leakage current	14	V_{CC1}=V_{CC2}=5V, V_O=2.5V			±100	nA
I_{CC}	Circuit current		V_{CC1}=V_{CC2}=5.5V		20	35	mA
I_{OIK}	Output leakage current	15, 16, 17, 18	V_{CC1}=V_{CC2}=5.5V, V_{OH}=5.5V			30	μA

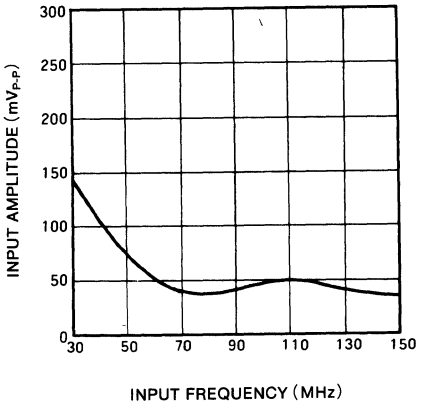
Note 15 : All voltages are measured with respect to circuit ground (pin 11) at 0V
16 : Currents are taken to be positive when flowing into the circuit and negative when flowing out of the circuit, the minimum and maximum values taken to be absolute values.
* : A Typical value at T_a=25℃

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{FM1}	FM input sensitivity	5	$V_{CC1}=V_{CC2}=4.5V$, $f_{FM}=60\sim130MHz$			160	mV_{P-P}
V_{FM2}	FM input sensitivity	5	$V_{CC1}=V_{CC2}=4.5V$, $f_{FM}=8\sim60MHz$			400	mV_{P-P}
V_{AM1}	AM input sensitivity	7	$V_{CC1}=V_{CC2}=4.5V$, $f_{AM}=2\sim4MHz$			100	mV_{P-P}
V_{AM2}	AM input sensitivity	7	$V_{CC1}=V_{CC2}=4.5V$, $f_{AM}=0.5\sim2MHz$			200	mV_{P-P}

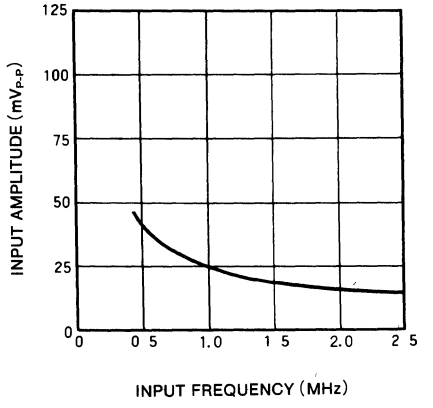
TYPICAL INPUT SENSITIVITY CHARACTERISTICS ($V_{CC1}=V_{CC2}=5V$, $T_a=25℃$)

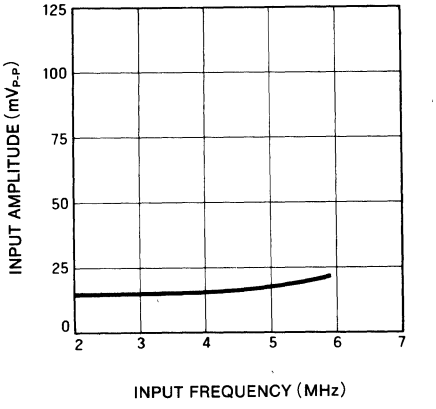
(1) MINIMUM FM INPUT AMPLITUDE VS INPUT FREQUENCY



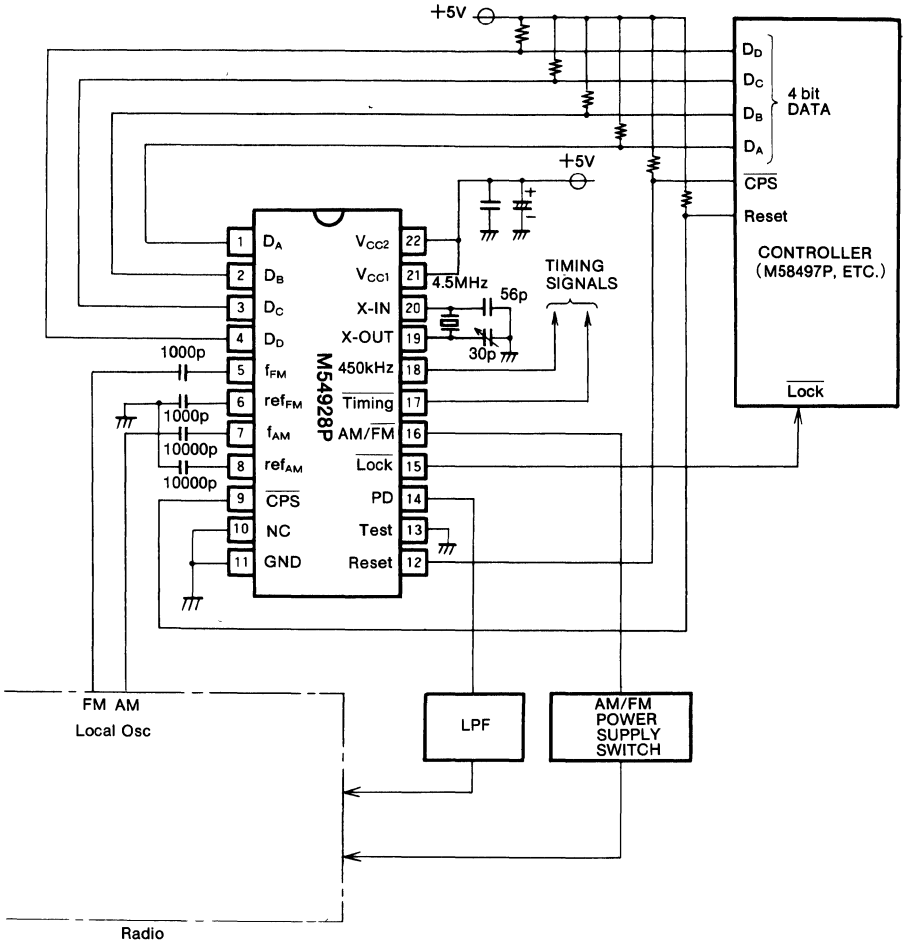


(2) MINIMUM AM INPUT AMPLITUDE VS INPUT FREQUENCY





APPLICATION EXAMPLE



M54929P

PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

DESCRIPTION

The M54929P is an IIL semiconductor integrated circuit consisting of a PLL frequency synthesizer, suitable for use in a amateur radio equipment.

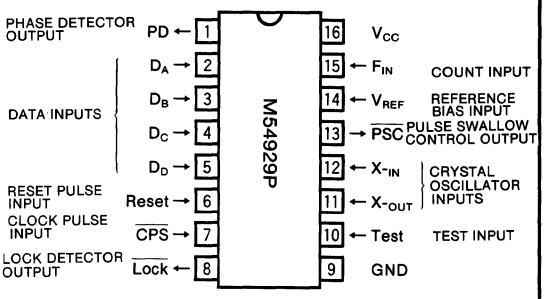
FEATURES

- Capable of synthesizing frequencies up to 300MHz when used with the M54466L 1/10, 1/11 2 -modulus prescaler
- Programmable divider can operate at frequencies up to 30MHz
- Division ratios from 200 to 3999 can be set using a swallow counter (set from 0 ~ 9 by 4 bits of BCD code) and program divider (set from 20 ~ 3999 by 14 bits of BCD code).
- Four reference frequency division ratios (1/20, 1/100, 1/1000, and 1/1024)
- PLL lock/unlock status display outputs
- Two-stage data latch

APPLICATION

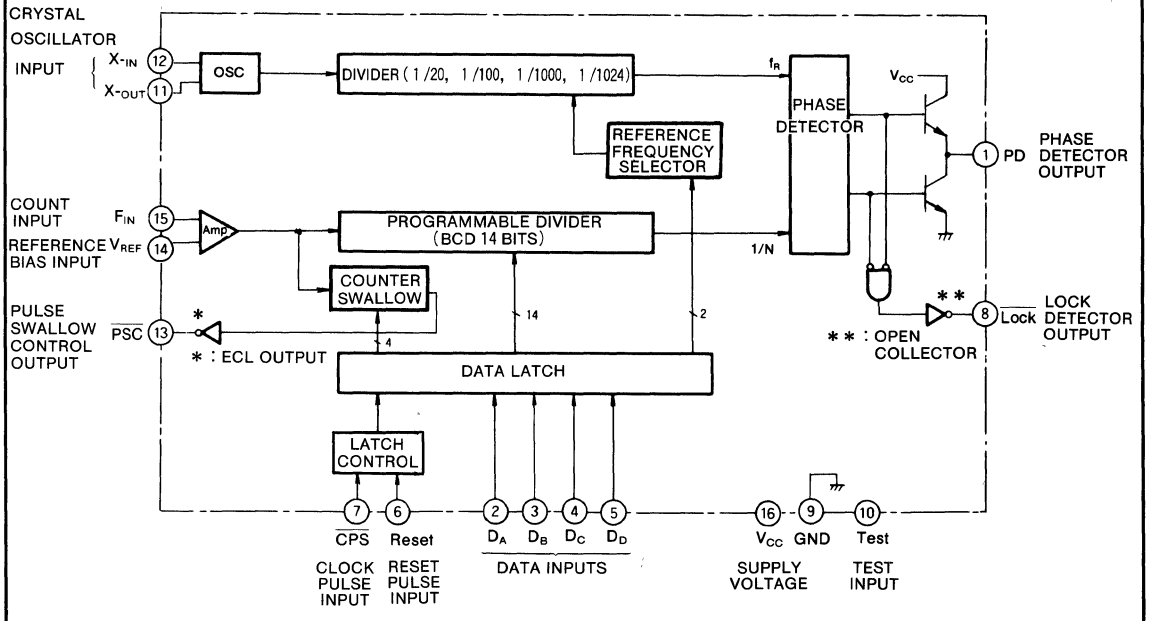
Amateur radio equipment

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

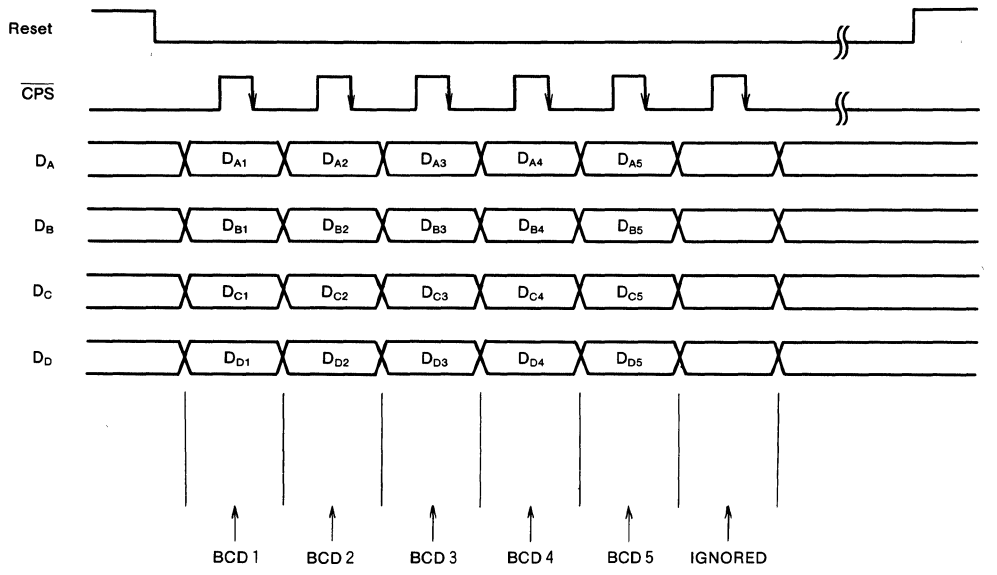
PIN DESCRIPTION

No.	Symbol	Pin name	Description
1	PD	Phase detector output	Three-state High=phase advance, low=phase delay, high impedance=sync
2	D_A	Data input	Input pin to set division ratio of programmable divider Data is set with BCD code
3	D_B		
4	D_C		
5	D_D		
6	Reset	Reset pulse input	Data latch reset input
7	$\overline{CPS}$	Clock pulse input	Data read clock input
8	$\overline{Lock}$	Lock detector output	Low when PD is high-impedance, high when PD is low or high Open collector.
9	GND	GND	0 V
10	Test	Test input	Normally set low When set high, program divider output F_{IN}/N is output at pin 1 (PD), and reference frequency f_R is output at pin 8 ($\overline{Lock}$).
11	$X\text{-}_{OUT}$	Crystal oscilltor input	A 10MHz crystal oscillator is used.
12	$X\text{-}_{IN}$		
13	$\overline{PSC}$	Pulse swallow control output	Controls division ratio of 1/10, 1/11 2-modulus prescaler (M54466L) ECL level output
14	V_{REF}	Reference bias	Grounded through a 10000pF capacitor
15	F_{IN}	Count input	Count frequency input pin. f_{max}=30MHz
16	V_{CC}	Power supply	5 V±0.25V

FUNCTION

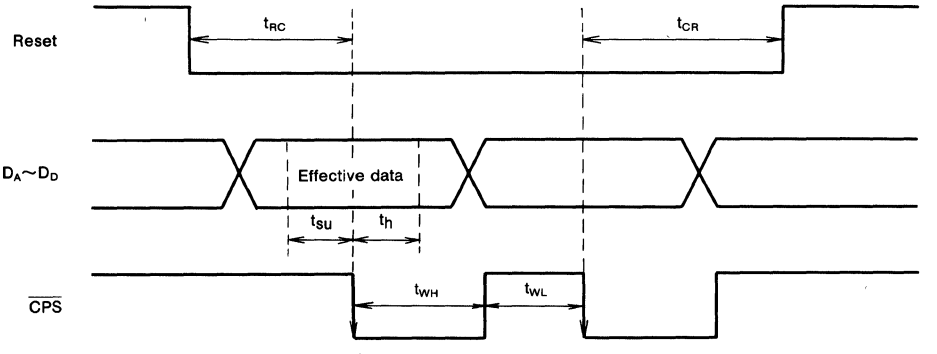
1. DATA INPUT

Configuration of input signals



Note 1 : After the Reset input is set low, five pulses applied at $\overline{CPS}$ (negative-edge trigger) read five sets of 4 -bit BCD data.
2 : General parameters (N value, reference frequency) are set at the falling edge of the 5 th $\overline{CPS}$ pulse. Successive data inputs at $\overline{CPS}$ are ignored.
3 : When the reset input is high, signals applied at $\overline{CPS}$, D_A and D_D have no effect

Timing of input signals

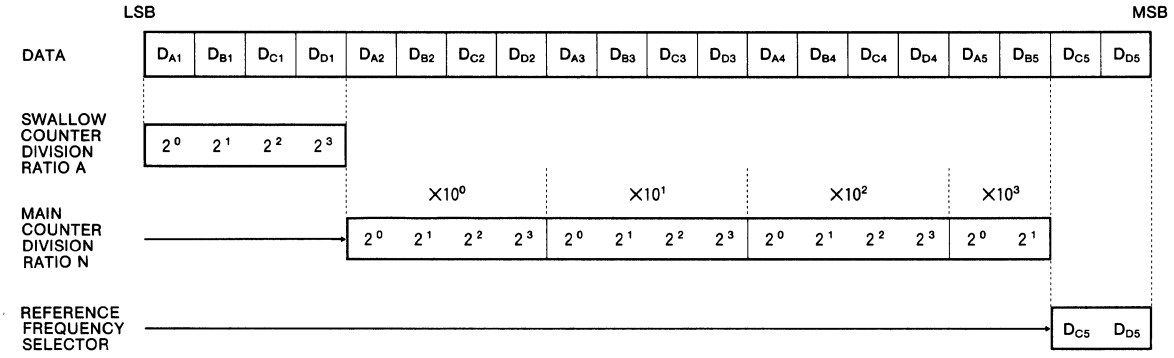


Minimum value $t_{su}=t_h=t_{WH}=t_{WL}=10\mu S$

$t_{RC}=t_{CR}=20\mu S$

MITSUBISHI ELECTRIC

2. CONFIGURATION OF DATA BITS



Note 4 : When 1/10, 1/11 2-modulus prescaler (M54466L) is connected, the overall division ratio M is given by M=A+10N
5 : When a prescaler is not used, the division ratio is determined by N and the data in the swallow counter is not used.
6 : The reference frequency is selected using the values in the table below.

Reference frequencies

BCD 5		Division ratio	Reference frequency	Crystal type
D_{C5}	D_{D5}			
L	L	1024	10kHz	10.24MHz
H	L	1000	10kHz	10MHz
L	H	100	100kHz	10MHz
H	H	20	500kHz	10MHz

3. Example of data coding

(1) The following BCD codes set a reference frequency of 10kHz and a division ratio of 26789 when used with a 1/10, 1/11 2-modulus prescaler

D_{A1}	D_{B1}	D_{C1}	D_{D1}	D_{A2}	D_{B2}	D_{C2}	D_{D2}	D_{A3}	D_{B3}	D_{C3}	D_{D3}	D_{A4}	D_{B4}	D_{C4}	D_{D4}	D_{A5}	D_{B5}	D_{C5}	D_{D5}
H	L	L	H	L	L	L	H	H	H	H	L	L	H	H	L	L	H	H	L
9				8				7				6				2		10kHz reference frequency	

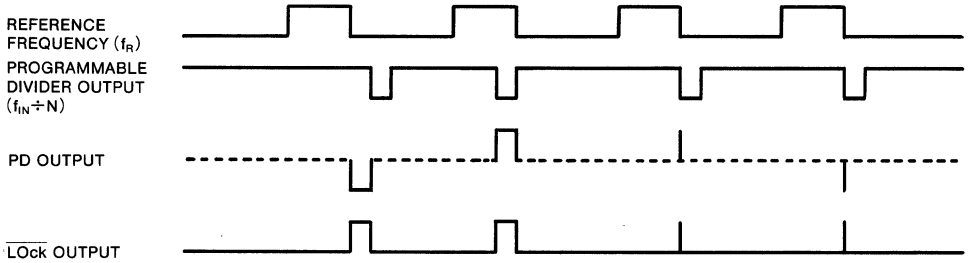
Note 7 : The PLL locks, when $f_{IN}=26789\times 10kHz=267.89MHz$

(2) To set a reference frequency of 100kHz and a division ratio of 254, when a prescaler is not used

D_{A1}	D_{B1}	D_{C1}	D_{D1}	D_{A2}	D_{B2}	D_{C2}	D_{D2}	D_{A3}	D_{B3}	D_{C3}	D_{D3}	D_{A4}	D_{B4}	D_{C4}	D_{D4}	D_{A5}	D_{B5}	D_{C5}	D_{D5}
X	X	X	X	L	L	H	L	H	L	H	L	L	H	L	L	L	L	L	H
X=irrelevant (either high or low)				4				5				2				0		100kHz reference frequency	

Note 8 : The PLL locks, when $f_{IN}=254\times 100kHz=25.4MHz$.

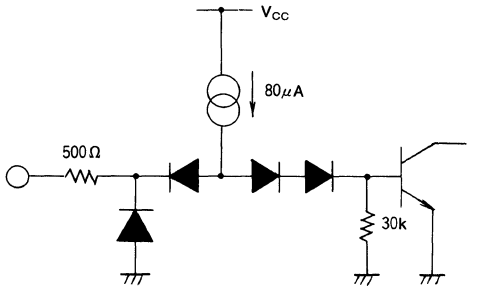
4. PD, $\overline{Lock}$



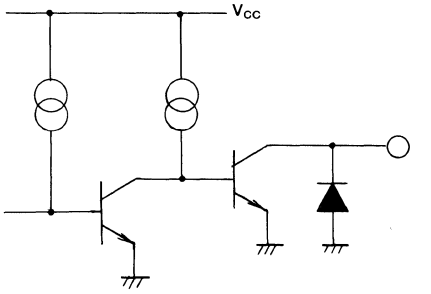
Note 9 : When the phase of program divider output ($f_{IN}\div N$) is delayed with respect to the reference frequency (f_R), PD goes low ; when the phase of $f_{IN}\div N$ is advanced, PD goes high.
10 : Broken lines indicate the high-impedance state

I/O CIRCUIT DIAGRAM

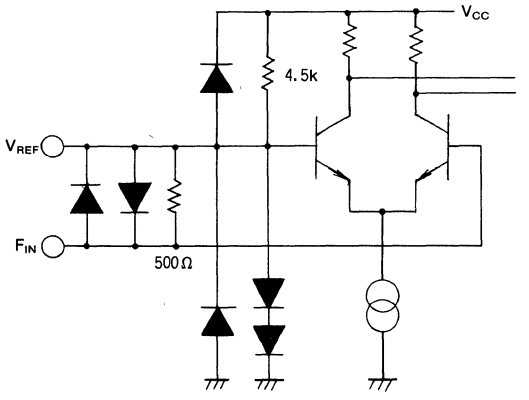
1 D_A through D_D, Reset, $\overline{CPS}$, Test inputs



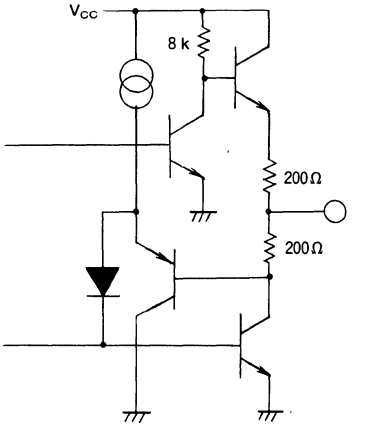
2 $\overline{Lock}$ output



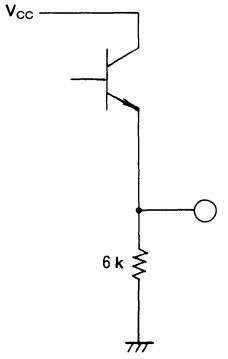
3 F_{IN}, V_{REF} inputs



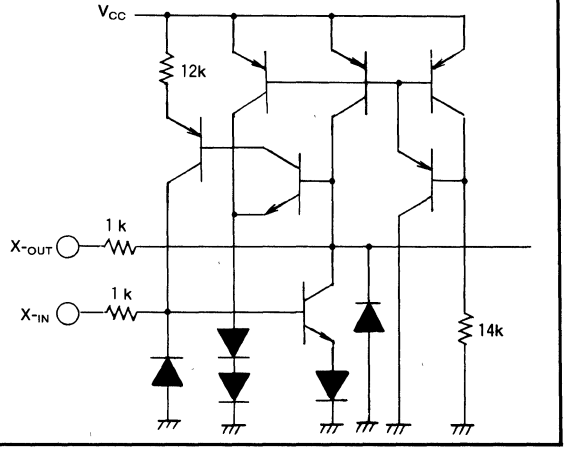
4 PD output



5 PSC output



6 OSC circuit



Note 11 : Resistance and current values shown are typical at T_a=25℃.

PLL FREQUENCY SYNTHESIZER FOR AMATEUR RADIOS

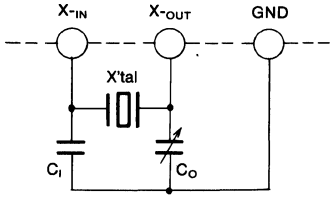
ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits		Unit
			Min	Max	
V_{CC}	Supply voltage		−0.5	6.0	V
V_I	Input voltage	F_{IN}, V_{REF}, $X\text{-}_{IN}$, $X\text{-}_{OUT}$ Input	−0.5	2.0	V
		D_A∼D_D, Reset, $\overline{CPS}$, Test inputs		6.0	
V_O	Output voltage	All outputs		V_{CC}	V
P_d	Power dissipation	T_a=75℃		600	mW
Topr	Operating temperature		−20	+75	℃
Tstg	Storage temperature		−40	+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	Remark
			Min	Typ	Max		
V_{CC}	Supply voltage		4.75	5.0	5.25	V	
F_{IN}	Input frequency		3		30	MHz	Sine wave input
V_{IN}	Input amplitude	F_{IN} = 3 ∼15MHz	200		800	mV_{P-P}	
		F_{IN} =15∼30MHz	200		800		
I_{OL}	Low-level output current	$\overline{Lock}$ output		1	5	mA	
f_{OSC}	Reference frequency			10		MHz	

CRYSTAL OSCILLATOR CIRCUIT



Note 12 : Specifications of crystal oscillator
Resonant frequency 10MHz±30ppm
Capacitive load 20pF
Effective resistancb<100Ω
13 : Capacitance
C_i=56pF, C_O=30pF (trimmer)

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	Pins 2∼7, 10	V_{CC}=5.5V	2.0			V
V_{IL}	Low-level input voltage	Pins 2∼7, 10	V_{CC}=5.5V			0.6	V
I_{IH}	High-level input current	Pins 2∼7, 10	V_{CC}=5.5V, V_{IH}=5.5V			30	μA
I_{IL}	Low-level input current	Pins 2∼7, 10	V_{CC}=4.5V, V_{IL}= 0V		−80	−160	μA
V_{OL}	Low-level output voltage	Pin 8	V_{CC}=4.5V, I_{OL}= 5mA			0.5	V
V_{OHP1}	PD high-level output voltage	Pin 1	V_{CC}=4.5V, I_{OH}=− 1mA	3.0			V
V_{OHP2}	PD high-level output voltage	Pin 1	V_{CC}= 5V, I_{OH}=−0.1mA	4.0			V
V_{OLP1}	PD low-level output voltage	Pin 1	V_{CC}=4.5V, I_{OL}=1mA			1.5	V
V_{OLP2}	PD low-level output voltage	Pin 1	V_{CC}= 5V, I_{OL}=0.1mA			1.0	V
I_{PD1}	PD leakage current	Pin 1	V_{CC}=5.5V, V_O=0.8∼4.0V			±3.0	μA
I_{PD2}	PD leakage current	Pin 1	V_{CC}= 5V, V_O=2.5V			±1.0	μA
I_{ILK}	$\overline{Lock}$ leakage current	Pin 8	V_{CC}=5.5V, V_O=5.5V			30	μA
I_{CC}	Supply current		V_{CC}=5.5V		60	90	mA
V_{OHPSC}	PSC high-level output voltage	Pin 13	V_{CC}= 5V, R_L= 3kΩ	3.2			V
V_{OLPSC}	PSC low-level output voltage	Pin 13	V_{CC}= 5V, R_L= 3kΩ			2.6	V

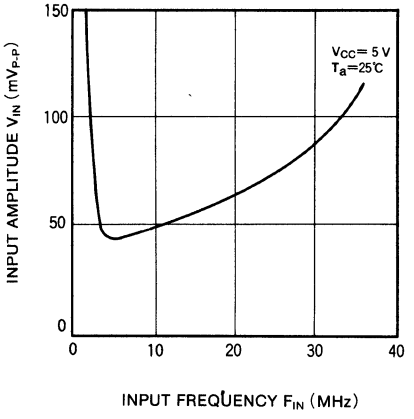
Note 14 : All voltages are measured with respect to circuit ground (pin 9).
15 : Currents are taken to be positive (no sign) when flowing into the circuit and negative when flowing out of the circuit. The minimum and maximum values are taken to be absolute values.

AC CHARACTERISTICS (V_{CC}= 5 V, T_a=25℃, unless otherwise noted)

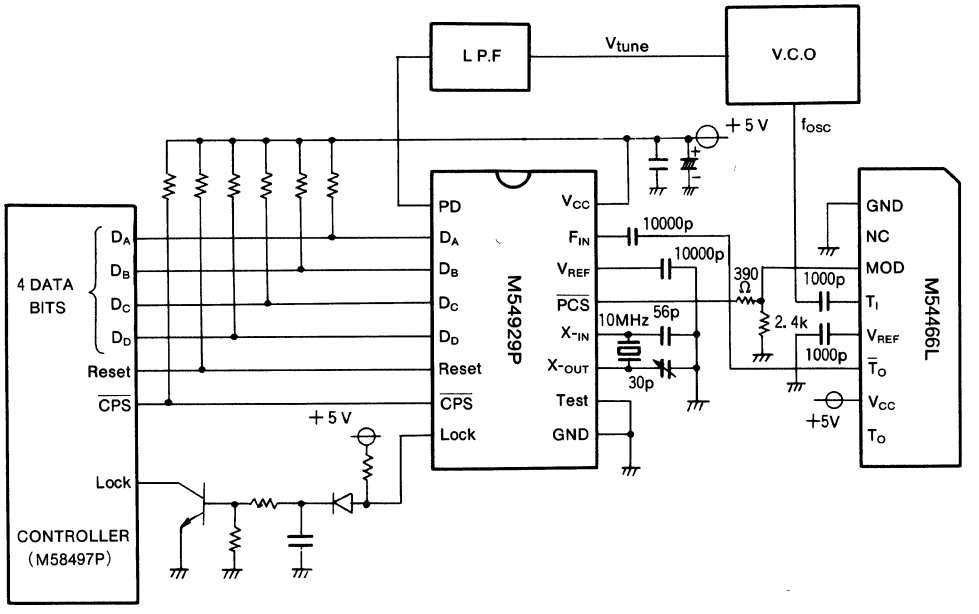
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IN1}	F_{IN} input sensitivity	15	F_{IN} = 3 ~15MHz			200	mV_{P-P}
V_{IN2}	F_{IN} input sensitivity	15	F_{IN} =15~30MHz			200	mV_{P-P}
V_{PSC}	$\overline{PSC}$ output amplitude	13	F_{IN} =30MHz, R_L = 3 kΩ	600			mV_{P-P}

TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



APPLICATION EXAMPLE



M54940P/FP

8-DIGIT FLUORESCENT DISPLAY DRIVER FOR MICROCOMPUTER

DESCRIPTION

The M54940P, a monolithic integrated circuit fabricated with using an IIL technology, is designed for driving an 8-digit, 7-segment fluorescent display.

FEATURES

- Separated power supplies; 5V (Logic circuit), and 35V (Output circuit)
- Integral scanning oscillator circuit for display

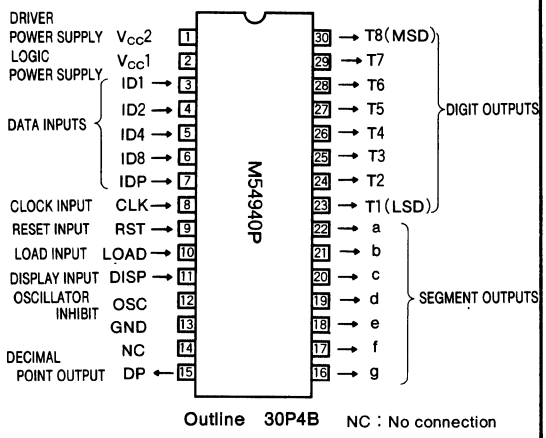
APPLICATION

Micro computer display. Digital equipment for consumer and Industrial use.

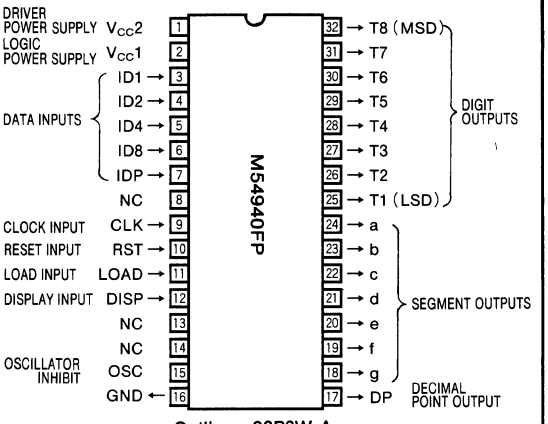
FUNCTION

The M54940P, having a 5-bit×8-digit memory, is a decoder driver for dynamic displaying of a vacuum fluorescent tubes. The data for one digit section is organized into a 4-bit BCD and an 1-bit decimal point. The data memory consists of a shift register and a latch, and is capable of displaying the previous data while the data is being transported.

PIN CONFIGURATION (TOP VIEW)

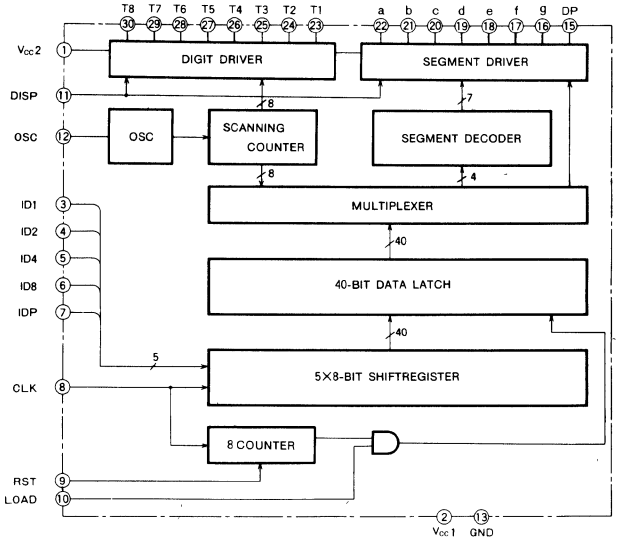


Outline 30P4B NC : No connection



Outline 32P2W-A NC : No connection

BLOCK DIAGRAM



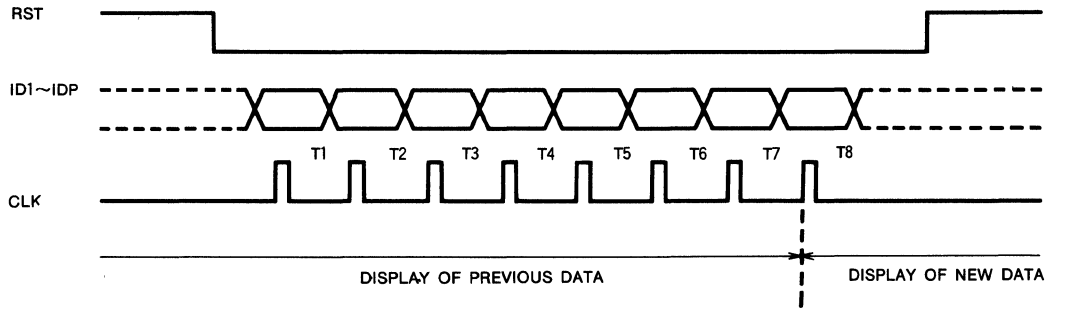
INPUT PIN FUNCTION

1) OSC : External capacitor connecting terminal for the oscillator circuit.
2) ID 1, ID 2, ID 4, ID 8 : BCD Data Input; refer to the numerical Designations-resultant displays for the relation of the input data to the display.
3) IDP : decimal point data Input
4) CLK : Data transport clock Input: the data can be input at a positive-going edge of the CLK
5) RST : Reset Input : the CLK input counter is reset at "H".
6) LOAD : Signal Input to load the data latch with the data of the shift register. The Input LOAD will not be accepted until the 8th CLK Input has been received.
7) DISP : When it is set to "H" it displays. When it is set to "L", the display is inhibitted. During the display inhibition period, both the segment and digit outputs will be at "L".

TIMING CHART

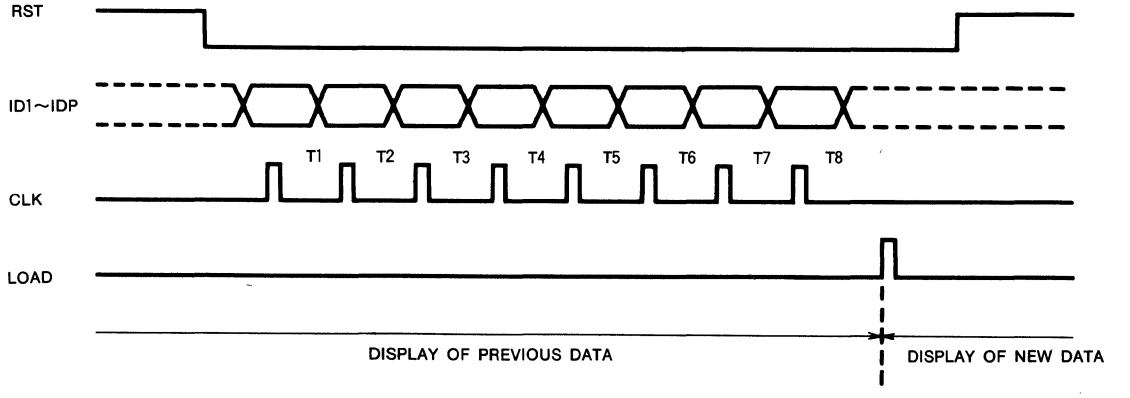
DATA PROGRAMMING

(1) USING CLK AND RST inputs with LOAD=" H ".



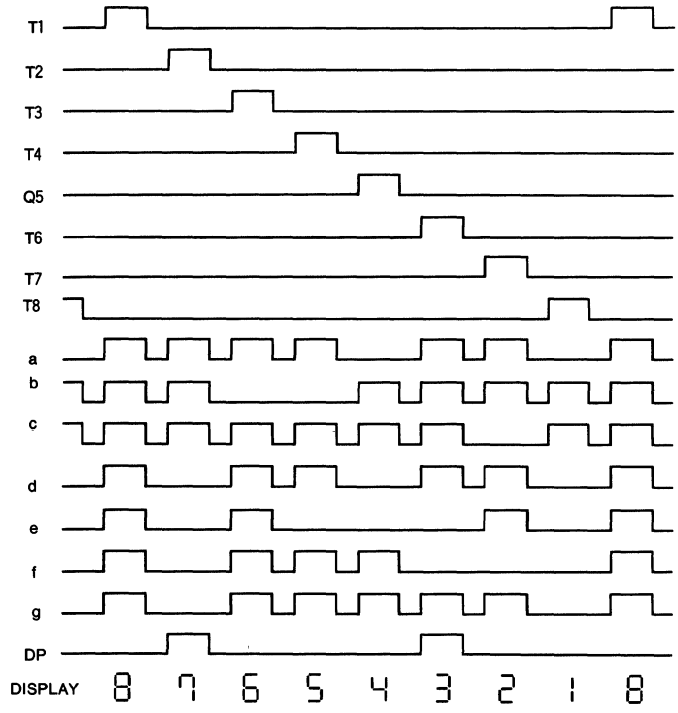
When LOAD is kept at " H ", LOAD is automatically done at the 8th CLK input when RST=" L ".
However, while RST=" L ", if there is a 9th CLK input, the 9th data will be loaded and displayed.

(2) Using CLK, RST and LOAD inputs.



After the 8th clock input, the LOAD is valid only in the period while RST=" L ".
Furthermore, if there is 9th CLK input before the LOAD input, the LOAD input is ignored.

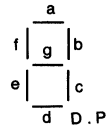
OUTPUT TIMING CHART



NUMERICAL DESIGNATIONS-RESUITANT DISPLAYS

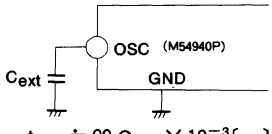
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
BCD DATA	ID1	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	ID2	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	ID4	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	ID8	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
Display		0	1	2	3	4	5	6	7	8	9	-	E	P	L	¬	Blank

*The decimal point, independent of BCD data, is output when the decimal bit of the corresponding digit is at " H ". Furthermore, when the decimal point bit is set at " H " at plural digits, plural decimal points are displayed.



OSCILLATOR CIRCUIT

1) External connection



2) Oscillation period

$t_{osc} \fallingdotseq 20\, C_{ext} \times 10^{-3} [\mu s]$ (Typ.)

(Unit of C_{ext}; [pF])

DISPLAYS IMMEDIATELY "AFTER POWER ON."

The display which appears immediately after "power-on" is indefinable. During the period bofore the regular data is transported the display can be erased if DISP input is set at " L ".

8-DIGIT FLUORESCENT DISPLAY DRIVER FOR MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Logic supply voltage		−0.3∼+9	V
V_{CC2}	Driver supply voltage		−0.3∼+38	V
V_I	Input voltage		−0.3∼V_{CC1}	V
V_O	Output voltage		0∼V_{CC2}	V
T_{stg}	Storage temperature		−55∼+150	℃
T_{opr}	Operating temperature		−20∼+75	℃
P_d	Power dissipation		600	mW

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC1}	Logic supply voltage	4	5	7	V
V_{CC2}	Driver supply voltage	10	30	35	V

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, V_{CC1}=5V, V_{CC2}=35V, unless otherwise noted)

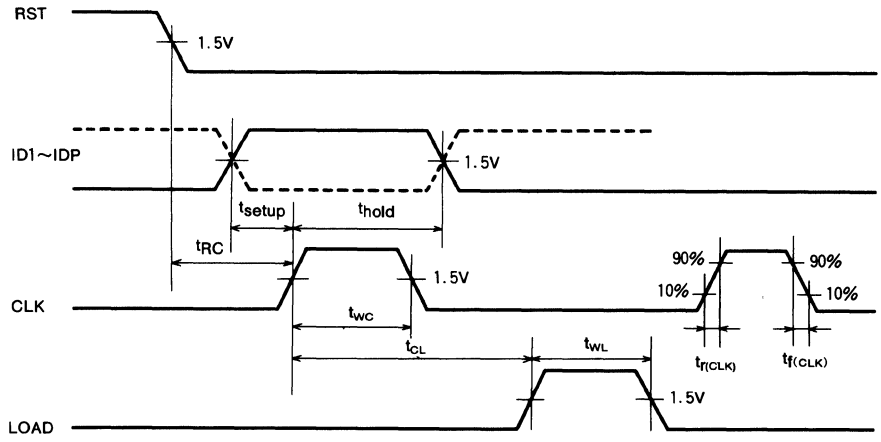
Symbol	Parameter		Test Conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	"H" Input voltage		V_{CC1}=4∼7V	2.7		V_{CC1}	V
V_{IL}	"L" Input voltage		V_{CC1}=4∼7V	0		0.7	V
I_{IH}	"H" Input current		V_{IH}=5V		0	20	μA
I_{IL}	"L" Input current		V_{IL}=0V		−0.25	−0.4	mA
V_{OH}	"H" Output voltage	Digit output	I_{OH}=−10mA	33	33.8		V
		Segment output	I_{OH}=−2mA	33	34		
V_{OL}	"L" Output voltage		I_{OL}=0mA		0	2	V
I_{CC1}	Logic circuit current		Input : open All segment outputs; ON		12	22	mA
I_{CC2}	Driver circuit current		Output : Open All segment outputs : ON		8	14	mA
t_{OSC}	Oscillation Period		C_{ext}=1000pF	10	20	40	μs

*Typical values are measured at 25℃

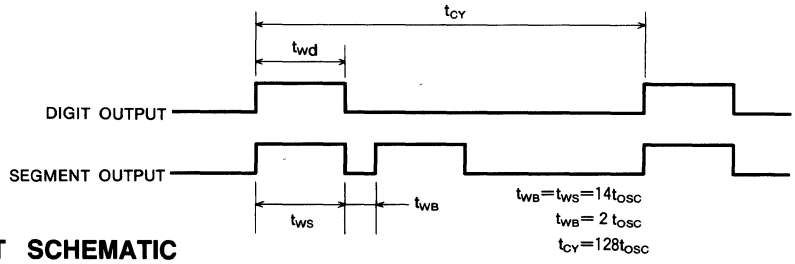
TIMING CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
f_{CLK}	Clock Frequency				100	kHz
f_{OSC}	Oscillation frequency		10		100	kHz
t_{WC}	Clock pulse width		2			μs
t_{WL}	Load Pulse width		2			μs
t_{setup}	Data setup time (DATA→CLK)		4			μs
t_{hold}	Data Hold time(CLK→DATA)		2			μs
t_{RC}	Reset-clock time(RST→CLK)		4			μs
t_{CL}	Clock-load, time(CLK→LOAD)		4			μs
$t_{r(CLK)}$	Clock pulse rise time				10	μs
$t_{f(CLK)}$	Clock pulse fall time				10	μs

INPUT TIMING CHART

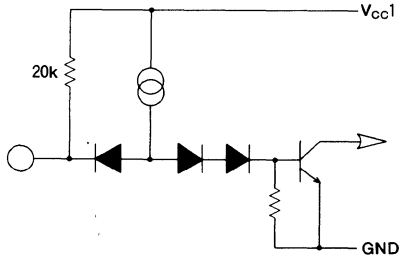


OUTPUT TIMING CHART

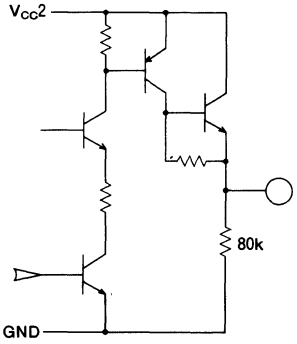


I/O CIRCUIT SCHEMATIC

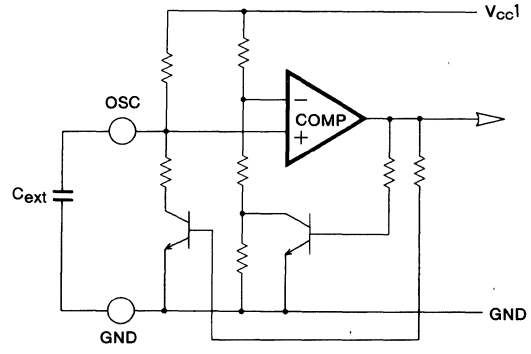
INPUT CIRCUIT



OUTPUT CIRCUIT



OSCILLATOR



M54956P

PLL FREQUENCY SYNTHESIZER FOR PERSONAL RADIOS

DESCRIPTION

The M54956P is a single-chip semiconductor integrated circuit consisting of a PLL frequency synthesizer for personal radio.

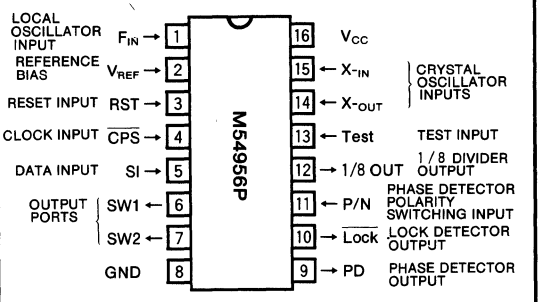
FEATURES

- Built-in 1/256 and 1/258 modulus prescaler (fmax=1.0GHz)
- Low power dissipation (I_{CC}=40mA, at V_{CC}= 5 V)
- Choice of four comparator frequency types (50k, 25k, 12.5k, 6.25k)
- Wide variety of division ratio (32768~262142, binary code)
- 1/8 Clock pulse output for referene oscillator frequency (TTL level)
- Output display for PLL lock/unlock
- Output port status can be set by date transferred from the controller
- Serial data input (three data transfer lines)

APPLICATION

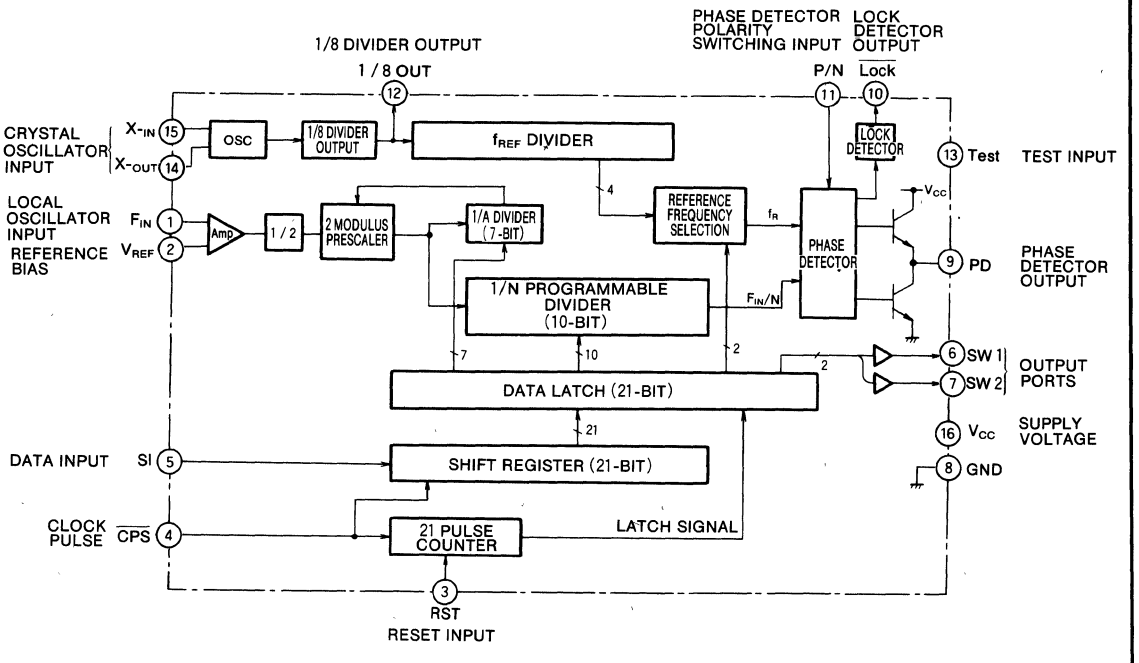
Personal radios, mobile radio telephones, MCA equipment

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



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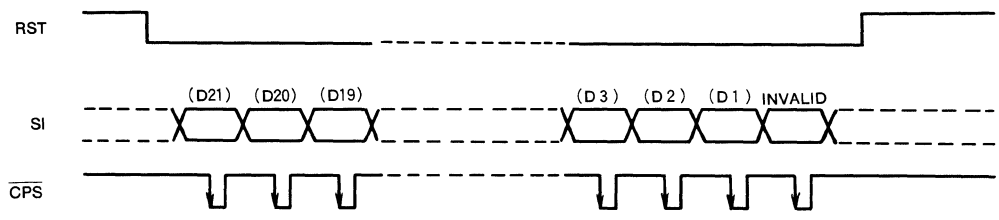
PIN DESCRIPTION

Pin no.	Symbol	Pin name	Description
1	F_{IN}	Local oscillator input	Local oscillator frequency (V C.O) input. f_{max}=1000MHz
2	V_{REF}	Reference bias	Connbct to ground through a 1000pF capacitor
3	RST	Reset input	Reset input of 21-pulse counter
4	$\overline{CPS}$	Clock input	Clock input for shift register
5	SI	Data input	Data input pin for shift register
6	SW1	Output port	Open-collector output port can be set by data tranferred from the controller
7	SW2		
8	GND	Ground	0 V
9	PD	Phase detector output	Three-state
10	$\overline{Lock}$	Lock detector output	Low when the PLL is locked, high when unlocked. Open collector.
11	P/N	Phase detector polarity switching	When P/N is high, the output at PD pin becomes high when the phase is advanced and low when the phase is retarded. When P/N is low, the logic states are inverted.
12	1/8OUT	1/8 divider output	TTL level
13	Test	Test input	Normally set low. When set high, f_R (the comparator frequency) is output at SW1 (pin 6) and the f_{IN}/N (programmable divider) is output at SW2 (pin 7).
14	$X\text{-}_{OUT}$	Crystal oscillator input	The output from 12.8MHz reference oscillator is supplied to $X\text{-}_{IN}$. Oscillation is generated by an externally connected crystal oscillator
15	$X\text{-}_{IN}$		
16	V_{CC}	Supply voltage pin	4.5~5.5V

FUNCTION

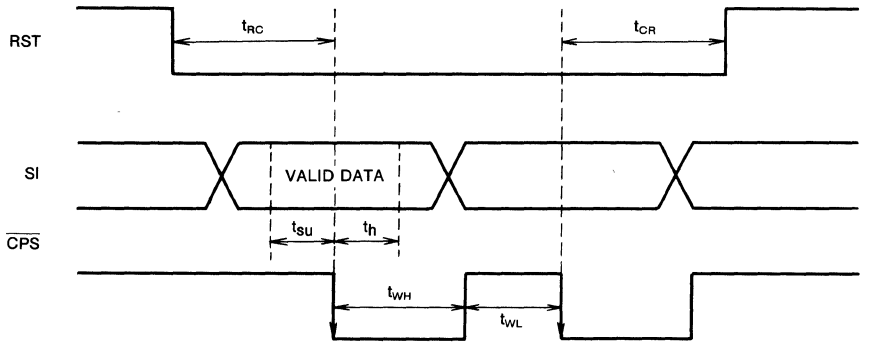
1. DATA INPUT

Configuration of input signal



Note 1 : The status of input SI is read by the shift register at the falling edge of the clock signal at $\overline{CPS}$.
2 : All data (N value, port, comparator frequency) are set at the falling edge of the 21st pulse at $\overline{CPS}$.Subsequent clock pulse at $\overline{CPS}$ are ignored.
3 : Pulses are accepted at neither $\overline{CPS}$ nor SI while RST is high.

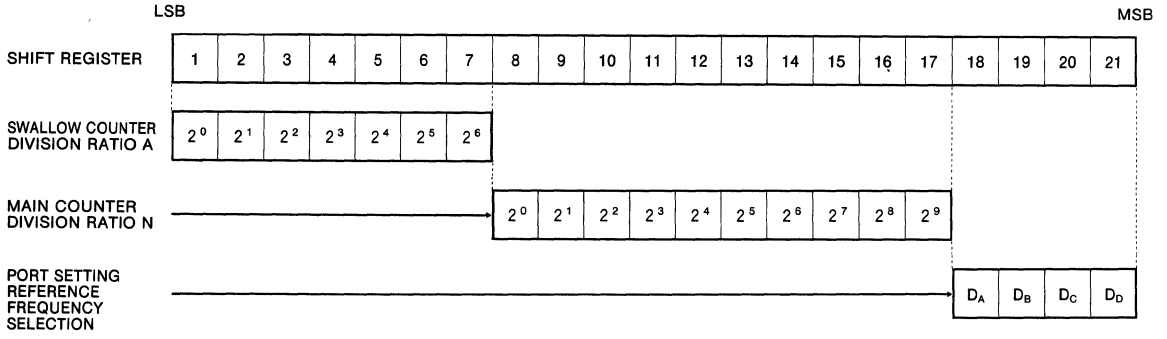
Timing of input signal



$t_{su}=t_h=t_{WH}=t_{WL}=10\mu S$ min.

$t_{RC}=t_{CR}=20\mu S$ min.

2. BIT CONFIGURATION OF SHIFT REGISTER



Note 4 : Total division ratio M is given by $M=2\times(A+128N)$.

5 : Comparator frequency is selected by D_A and D_B.

Data		Reference
D_A	D_B	frequency
L	L	50k
H	L	25k
L	H	12.5k
H	H	6.25k

Note 6 : Output port is set by D_C and D_D.

Data		Output port	
D_C	D_D	SW1	SW2
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

3. DATA CODING EXAMPLE

When reference freqency is 6.25kHz, M is 153784, SW 1 is high and SW 2 is low

LSB

SHIFT REGISTER	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
DATA	L	L	H	H	H	L	H	L	L	L	H	H	L	H	L	L	H	H	H	H	L

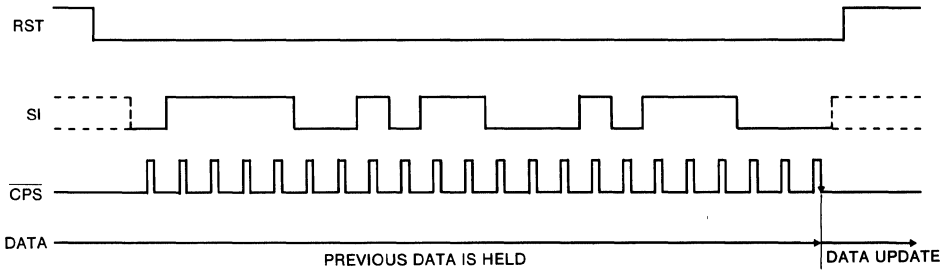
DIVISION RATIO SETTING FOR SWALLOW COUNTER
$A=2^2+2^3+2^4+2^6=92$

DIVISION RATIO SETTING FOR MAIN COUNTER
$N=2^3+2^4+2^6+2^9=600$

REFERENCE FREQUENCY 6.25kHz is selected

SW1 IS SET HIGH

SW2 IS SET LOW

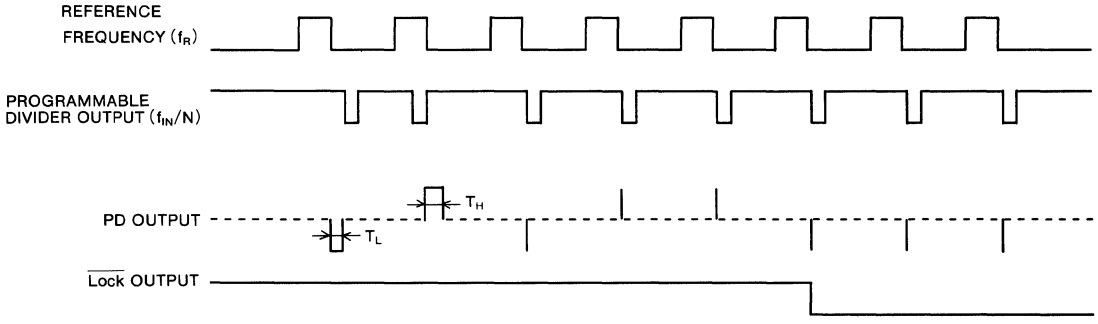


Note 7 : Total division ratio is set by M= 2 ×M(A+128N)= 2 ×(92+128×600)=153784
8 : When PLL is locked, f_{VCO}=6.25×153784=961150kHz
=961.15MHz

4. 1/8 OUTPUT SIGNAL WAVEFORM

※Duty cycle is 50%.

5. PD, $\overline{\text{Lock}}$ SIGNAL OUTPUT WAVEFORM

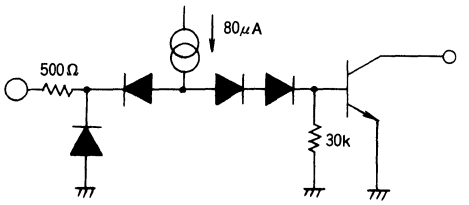


Note 9 : The PD output is low when the phase of the programmable divider output (f_{IN}/N) follows the phase of reference frequency (f_R) and is high when the phase f_{IN}/N leads that of f_R.
10 : Broken lines indicate the high-impedance state.
11 : When phase variance T_L and T_H are less than 625ns for a period of rerence frequency (f_R), the lock output becomes low.

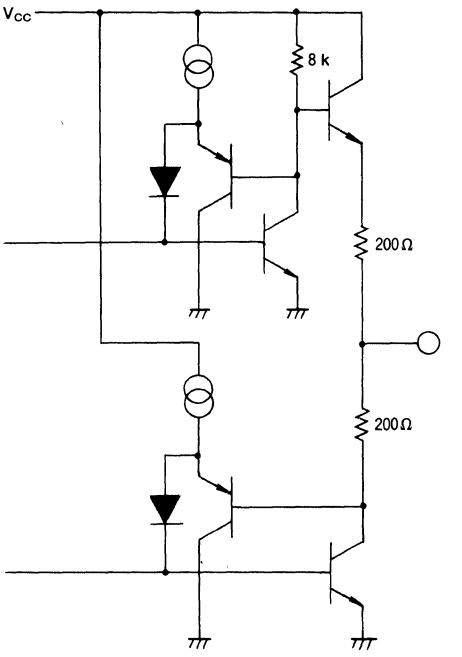
※The above description applies while P/N (pin 11) is high
While P/N input is low, the logic state of the PD output is inverted.

I/O CIRCUIT DIAGRAM

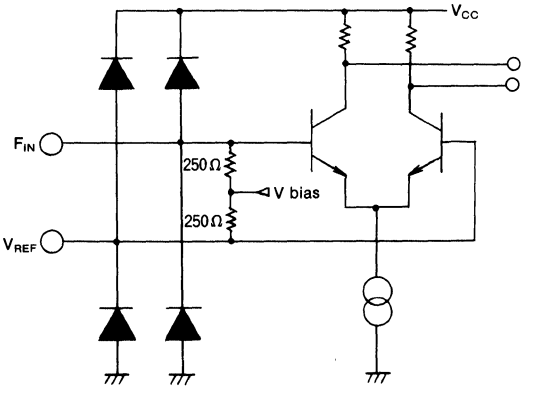
1 RST, $\overline{CPS}$, SI, P/N, Test Inputs



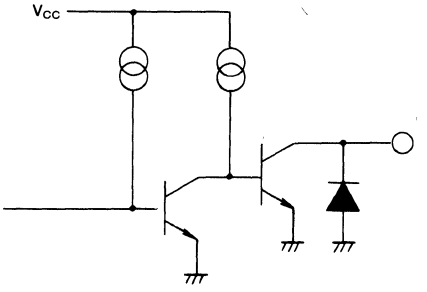
2 PD Output



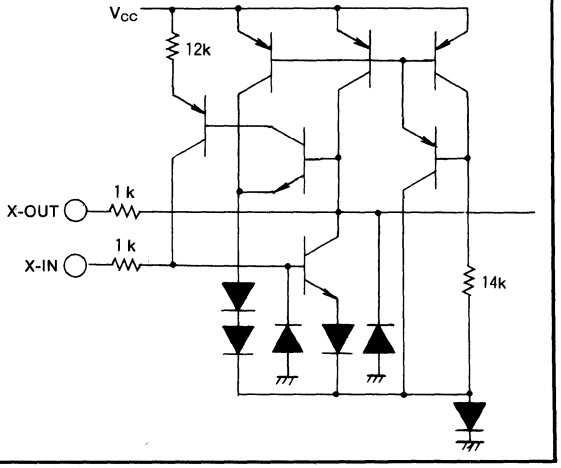
3 F_{IN}, V_{REF} Inputs



4 SW1, SW2, Lock Outputs



5 OSC Circuit



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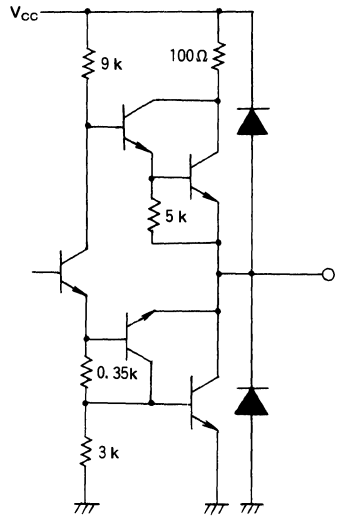
6

1 / 8 OUT Output



Note 12 : Resistance and current are typical values when V_{CC}= 5 V and T_a=−20∼+75℃

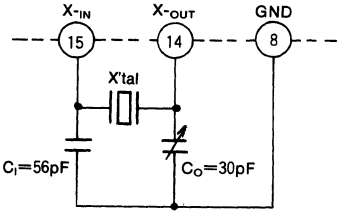
ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit
			Min	Max	
V_{CC}	Supply voltage		−0. 5	6. 0	V
V_I	Input voltage	Each input	−0. 5	6. 0	V
V_O	Output voltage	Each input	−0. 5	6. 0	V
Pd	Power dissipation	T_a =75℃		500	mW
Topr	Operating temperature		−20	+75	℃
Tstg	Storage temperature		−40	+125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4. 5∼5. 5V, T_a = −20∼+75℃ unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	Remark
			Min	Typ	Max		
V_{CC}	Supply voltage		4. 5	5	5. 5	V	
V_{IN}	Input amplitude	F_{IN} =100∼1000MHz	400		1200	mV_{P-P}	
F_{IN1}	Input frequency	V_{IN} =400mV_{P-P}	100		1000	MHz	
I_{OL}	Low-level output current	SW1, SW2, Lock output			5	mA	
V_{X-IN}	X-IN input amplitude	Note 14	1		2	V_{P-P}	Sine wave
f_{OSC}	Reference oscillation frequency	Note 13, Note 14		12. 8		MHz	

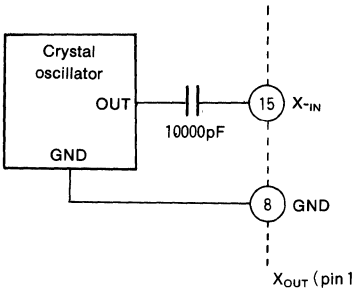
Note 13 : Connection of crystal vibrator



Load capacitance of crystal oscillator

Valid resistance 100Ω or less

Note 14 : Connection of crystal oscillator



X_{OUT} (pin 14) should be left open.

ELECTRICAL CHARACTERISTICS (T_a = −20~+75℃, unless otherwise noted)

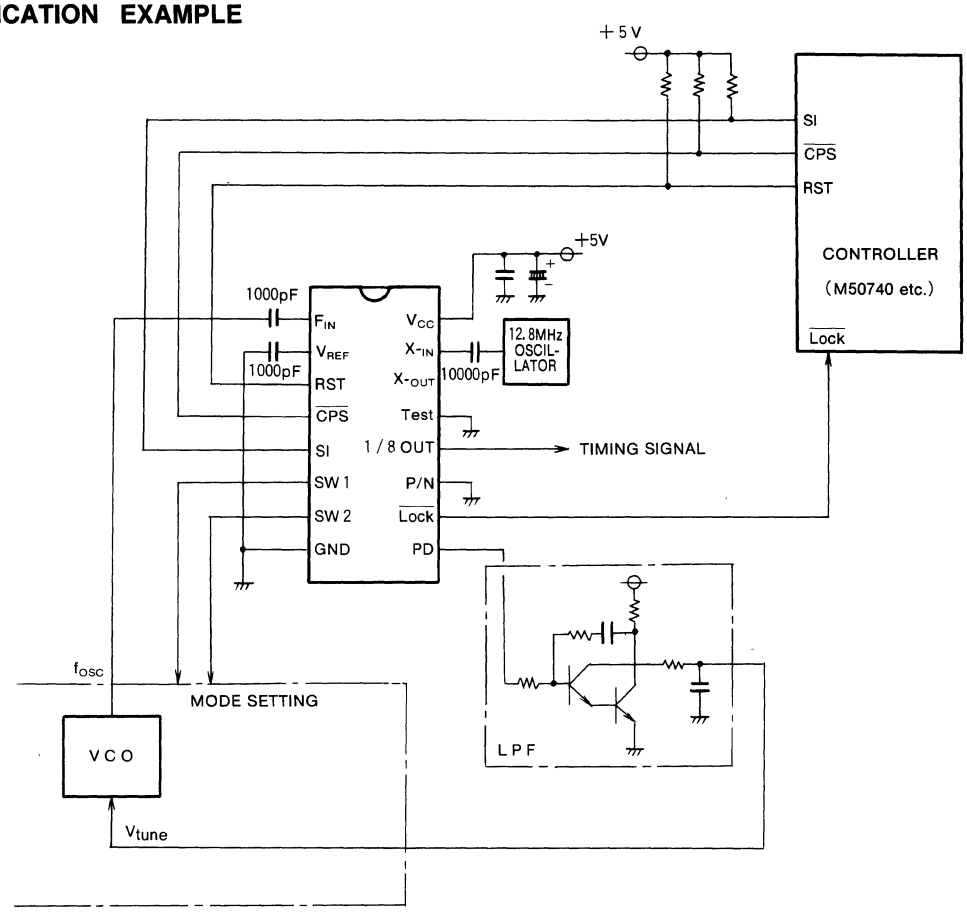
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	3, 4, 5, 11, 13	V_{CC}=5.5V	2.0			V
V_{IL}	Low-level input voltage	3, 4, 5, 11, 13	V_{CC}=5.5V			0.6	V
I_{IH}	High-level input current	3, 4, 5, 11, 13	V_{CC}=5.5V, V_{IH}=5.5V			30	μA
I_{IL}	Low-level input current	3, 4, 5, 11, 13	V_{CC}=4.5V, V_{IL}= 0 V		−80	−160	μA
V_{OL}	Low-level output current	6, 7, 10, 12	V_{CC}=4.5V, I_{OL}= 5 mA			0.5	V
V_{OHP1}	PD high-level output voltage	9	V_{CC}=4.5V, I_{OH}=− 1 mA	3.0			V
V_{OHP2}	PD low-level output voltage	9	V_{CC}= 5 V, I_{OH}=−0.1mA	4.0			V
V_{OLP1}	PD low-level output current	9	V_{CC}=4.5V, I_{OL}= 1 mA			1.5	V
V_{OLP2}	PD low-level output current	9	V_{CC}= 5 V, I_{OL}=0.1mA			1.0	V
I_{PD1}	PD leak current	9	V_{CC}=5.5V, V_O=0.8~4.7V			±1.0	μA
I_{PD2}	PD leak current	9	V_{CC}= 5 V, V_O=2.5V			±100	μA
I_{CC}	Supply voltage	16	V_{CC}=5.5V		40	60	mA
I_{OLK}	Output leak current	6, 7, 10	V_{CC}=5.5V, V_{OH}=5.5V			30	μA
V_{OH}	High-level output voltage	12	V_{CC}=4.5V, I_{OH}=− 1 V	2.0			V

Note 15 : The GND pin (pin 8) for voltages in this circuit is based on the reference voltage (0)

16 : Whn the currents flowing into the circuit are positive (no sings) and the currents flowing out from the circuit are negative (negative sign) and the minimum and maximum are shown in absolute values.

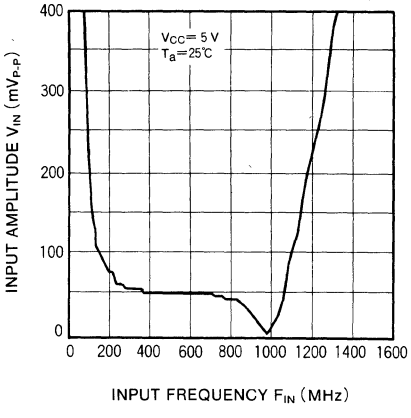
17 : Typical values are at V_{CC}= 5 V, and T_a=25℃

APPLICATION EXAMPLE



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



M54959P

PLL FREQUENCY SYNTHESIZER FOR PERSONAL RADIOS

DESCRIPTION

The M54959P is a semiconductor integrated circuit consisting of a PLL frequency synthesizer for use in personal radio equipment. It contains an 1/128 and 1/129 2-modulus prescaler allowing the direct synthesis of local oscillator frequency up to 500MHz.
The reference frequency is provided by a 12.8MHz crystal oscillator.

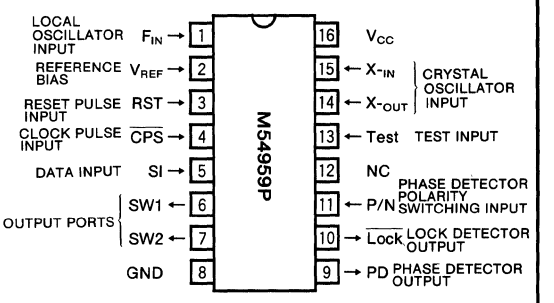
FEATURES

- Built-in 1/128 and 1/129 2-modulus prescaler (fmax=500MHz)
- Low power consumption (I_{CC}=20mA, at V_{CC}= 5 V)
- Reference frequency selectable from four values (25k, 12.5k, 6.25k, 5 k)
- Wide range of division ratio (16384~131071, binary coded)
- Serial data input (3 data-transfer lines)
- PLL Lock/unlock status display output
- Output-ports state can be set by date from a controller

APPLICATION

Personal radio

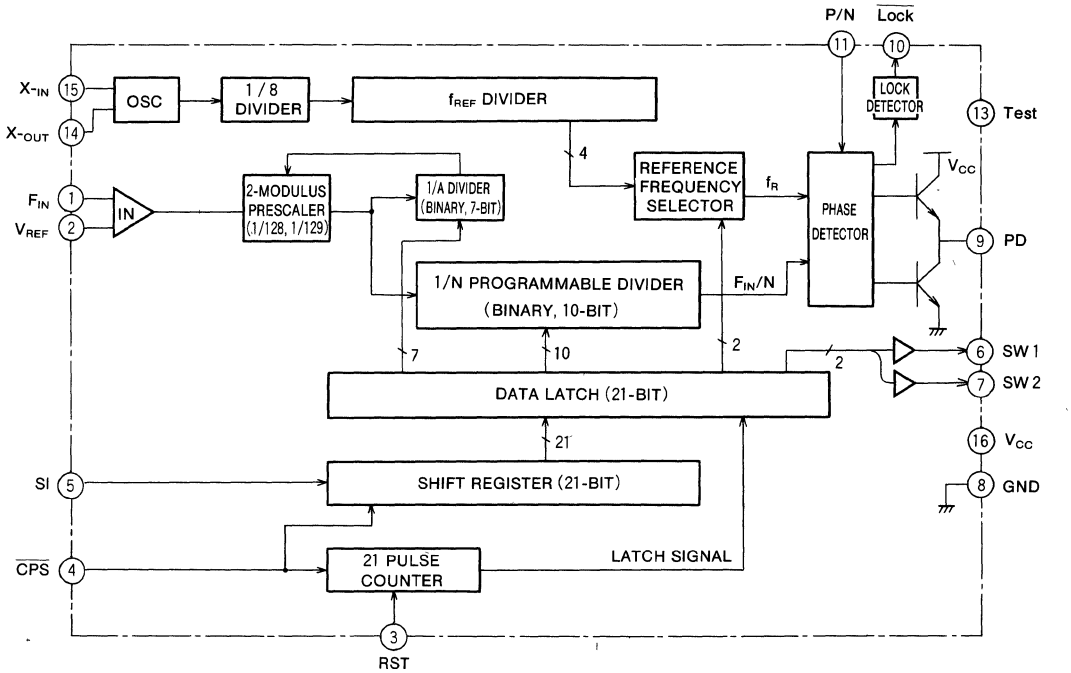
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

NC : No connection

BLOCK DIAGRAM



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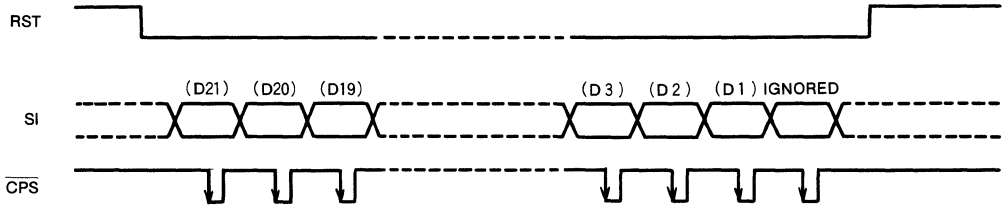
PIN DESCRIPTION

No.	Symbol	Pin name	Description
1	F_{IN}	Local oscillator input	Local oscillator frequency (V C.O) input f_{max}=500MHz
2	V_{REF}	Reference bias	Ground through a 1000pF capacitor
3	RST	Reset pulse input	Reset pulse input for 21-pulse couhter
4	$\overline{CPS}$	Clock pulse input	Clock pulse input for shift register
5	SI	Data input	Data input for shift register
6	SW1	Output port	Open collector output port. State can be set by data from a controller
7	SW2		
8	GND	GND	0 V
9	PD	Phase detector output	Three-state
10	$\overline{Lock}$	Lock detector output	Low when PLL locked, and high when unlocked. Open collector
11	P/N	Phase detector polarity switching	When high, PD goes high as the phase advances and low as the phase delays When low, PD goes low as the phase advances, and high as the phase delays.
12	NC	No connection	Open or GND
13	Test	Test input	Normally set low. When set high, f_R (reference frequency) is output from SW1 (pin 6), and f_{IN}/N (programmable divider output) is output from SW2 (pin 7).
14	$X\text{-}_{OUT}$	Crystal oscillator input	Apply the output from the 12.8MHz reference oscillator to $X\text{-}_{IN}$. A crystal resonator can also be connected.
15	$X\text{-}_{IN}$		
16	V_{CC}	Power supply pin	4.5~5.5V

FUNCTION

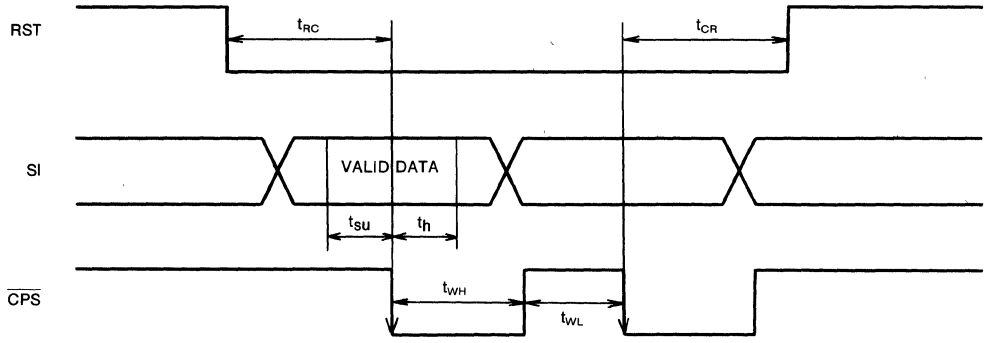
1. DATA INPUT

Configuration of input signal



Note 1 : Data at input SI is read into shift register sequentially by the falling edge of the clock signal at input $\overline{CPS}$.
2 : All data (N value, port, reference frequency) are set by the falling edge of the 21st clock pulse at $\overline{CPS}$.
Additional pulses at CPS are ignored.
3 : When RST is high, inputs are accepted at neither $\overline{CPS}$ nor SI

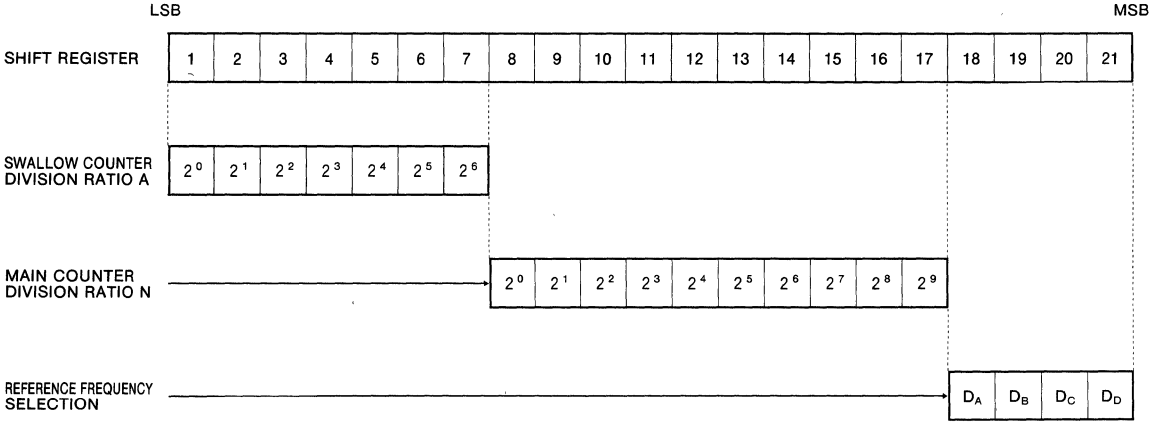
Timing of input signal



$t_{su}=t_h=t_{WH}=t_{WL}=10\mu S$ min

$t_{RC}=t_{CR}=20\mu S$ min

2. BIT CONFIGURATION OF SHIFT REGISTER



Note 4 : Total division ratio M is given by M=A+128N.

Note 5 : The reference frequency is selected by D_A and D_B

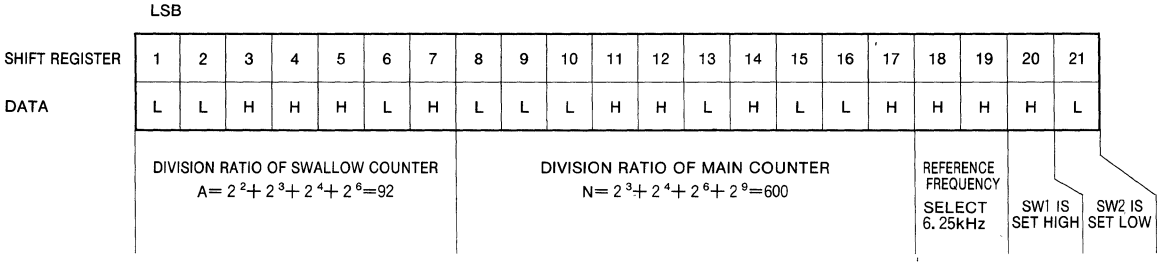
Data		Reference
D_A	D_B	frequency
L	L	50k
H	L	25k
L	H	12.5k
H	H	6.25k

Note 6 : The output port is selected by DC and DD

Data		Output port	
D_C	D_D	SW1	SW2
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

3. DATA CODING EXAMPLE

Reference freqency 6.25kHz, M=76892, SW 1 ="H", SW 2 ="L"



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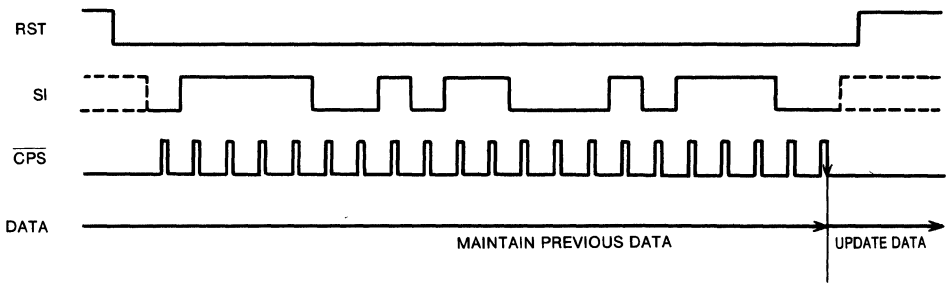
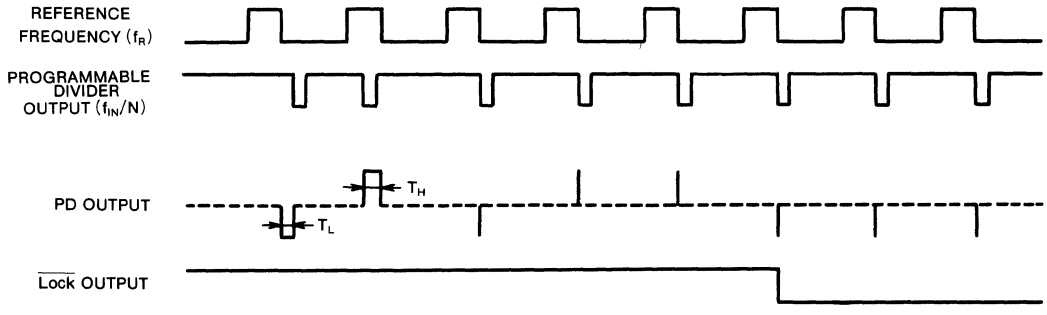


Note 7 : Total division ratio is set by M=A+128N=92+128×600=76892.
8 : When PLL is locked, f_{VCO}=6.25×76892=480575kHz
=480.575MHz

4. PD AND $\overline{Lock}$ WAVEFORMS

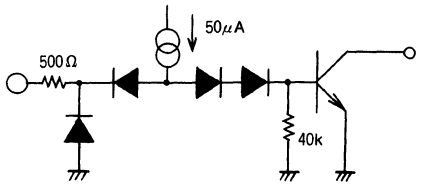


Note 9 : When the phase of programmable divider output f_{IN}/N is behind the phase of reference freqency f_R, PD is low; when $f_{IN/N}$ is ahead of f_R, PD is high.
10 : Broken lines indicate the high impedance state.
11 : If phase differnces T_L and T_H continue at less than 625ns for more than three cycles of reference frequency f_R, $\overline{LOCK}$ becomes low.

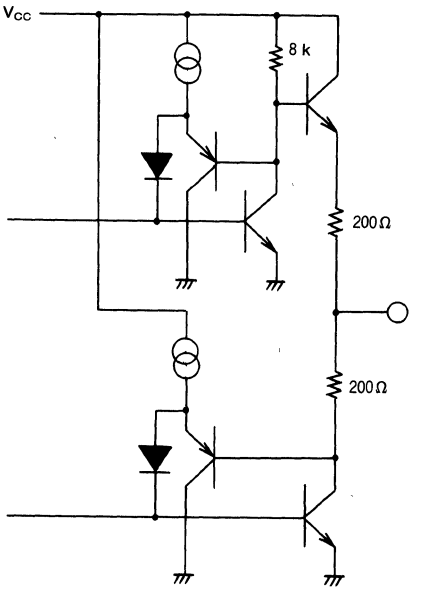
※The above description applies when input P/N (pin 11) is high.
When P/N is low, the output at PD is inverted.

I/O CIRCUITS

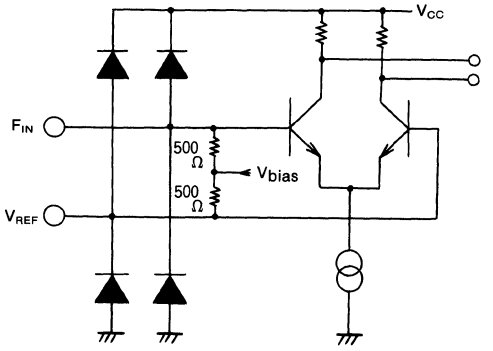
1 RST, $\overline{CPS}$, SI, P/N, and Test Inputs



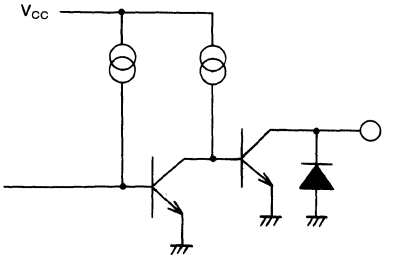
2 PD Output



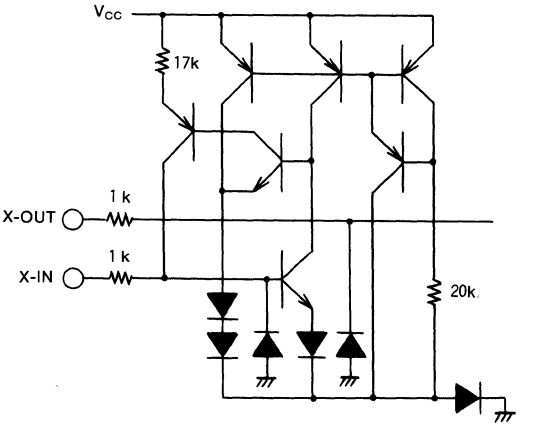
3 F_{IN}, and V_{REF} Inputs



4 SW1, SW2, and $\overline{Lock}$ Outputs



5 OSC Circuit



Note 12 : Resistance and current values are typical at V_{CC}= 5 V, T_a=25℃

MITSUBISHI ELECTRIC

PLL FREQUENCY SYNTHESIZER FOR PERSONAL RADIOS

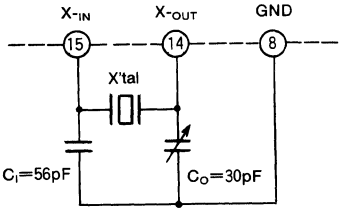
ABSOLUTE MAXIMUM RATINGS (T_a = −20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit	Remarks
			Min	Max		
V_{CC}	Supply voltage		−0.5	6.0	V	
V_I	Input voltage	All inputs	−0.5	6.0	V	
V_O	Output voltage	All outputs	−0.5	6.0	V	
Pd	Power dissipation	T_a =75℃		500	mW	Package permissible power dissipation
Topr	Operating temperature		−20	+75	℃	
Tstg	Storage temperature		−40	+125	℃	

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.5∼5.5V, T_a = −20∼+75℃ unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	Remarks
			Min	Typ	Max		
V_{CC}	Supply voltage		4.5	5	5.5	V	
V_{IN}	Input amplitude	F_{IN} =100∼1000MHz	200		800	mV_{P-P}	
F_{IN1}	Input frequency	V_{IN} =200∼800mV_{P-P}	100		500	MHz	
I_{OL}	Low-level output current	SW1, SW2, and $\overline{Lock}$ ontputs			5	mA	
V_{X-IN}	X_{-IN} input amplitude	Note 14	1		2	V_{P-P}	Sine wave
f_{OSC}	Reference oscillator frequency			12.8		MHz	

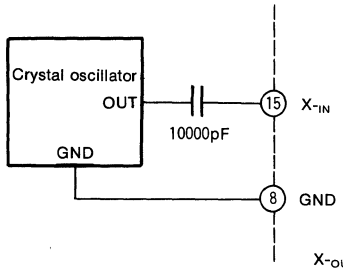
Note 13 : Cristal oscillator circuit



Lpad capacitance of crystal 20pF

Effective resistance less than 100Ω

Note 14 : Cristal oscillator circuit



X_{-OUT} (pin 14) is left open

ELECTRICAL CHARACTERISTICS (T_a = −20∼+75℃, unless otherwise noted)

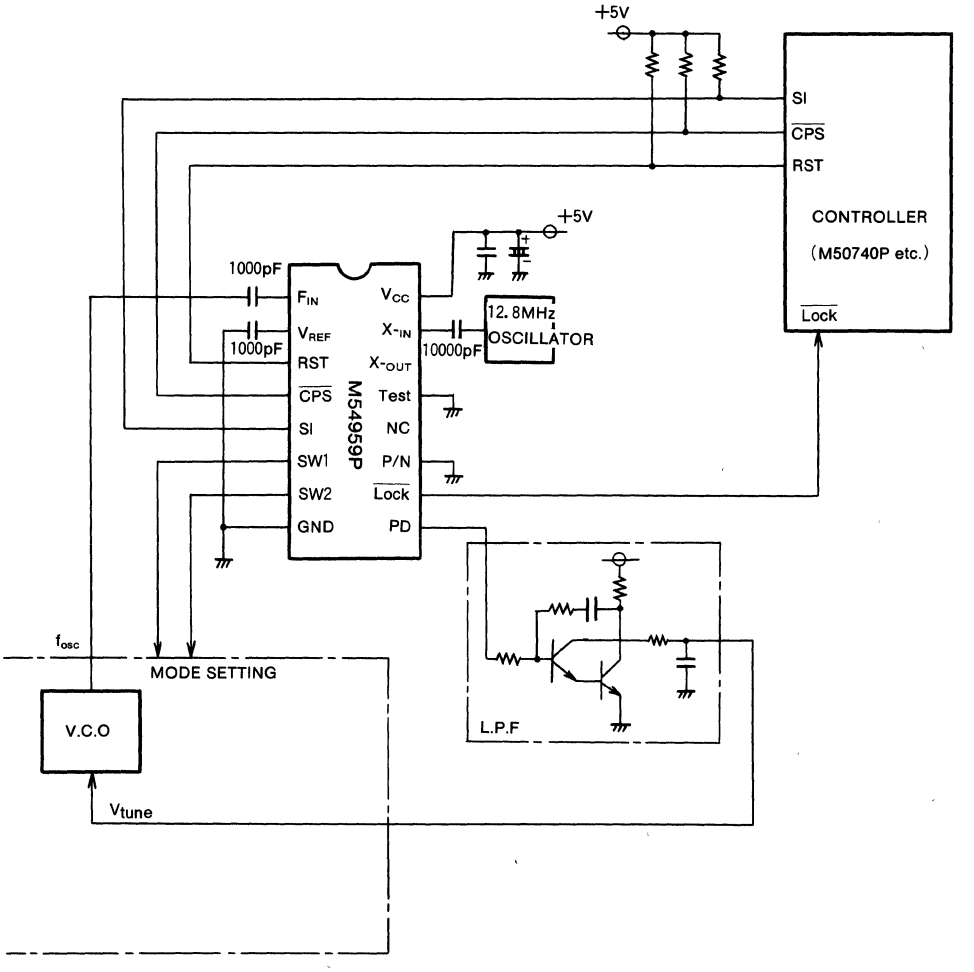
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	3, 4, 5, 11, 13	V_{CC}=5.5V	2.0			V
V_{IL}	Low-level input voltage	3, 4, 5, 11, 13	V_{CC}=5.5V			0.6	V
I_{IH}	High-level input current	3, 4, 5, 11, 13	V_{CC}=5.5V, V_{IH}=5.5V			30	μA
I_{IL}	Low-level input current	3, 4, 5, 11, 13	V_{CC}=4.5V, V_{IL}= 0V		−50	−100	μA
V_{OL}	Low-level output voltage	6, 7, 10, 12	V_{CC}=4.5V, I_{OL}= 5mA			0.5	V
V_{OHP1}	PD high-level output voltage	9	V_{CC}=4.5V, I_{OH}=−1mA	3.0			V
V_{OHP2}	PD high-level output voltage	9	V_{CC}= 5V, I_{OH}=−0.1mA	4.0			V
V_{OLP1}	PD low-level output voltage	9	V_{CC}=4.5V, I_{OL}= 1mA			1.5	V
V_{OLP2}	PD low-level output voltage	9	V_{CC}= 5V, I_{OL}=0.1mA			1.0	V
I_{PD1}	PD leakage current	9	V_{CC}=5.5V, V_O=0.8∼4.7V			±1.0	μA
I_{PD2}	PD leakage current	9	V_{CC}= 5V, V_O=2.5V			±100	μA
I_{CC}	Supply current		V_{CC}=5.5V		20	30	mA
I_{OLK}	Output leakage current	6, 7, 10	V_{CC}=5.5V, V_{OH}=5.5V			30	μA

Note 15 : All voltages are measured with respect to circuit ground (pin 8)

16 : Currents are taken to be positive (negative sign) when flowing out of the circuit.
The minimum and maximum values are taken to be absolute values

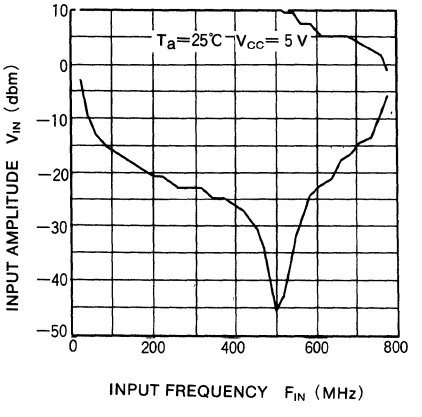
17 : Typical values are at V_{CC}= 5V, T_a=25℃

APPLICATION EXAMPLE



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY



MITSUBISHI ELECTRIC

M54965ASP

PRELIMINARY
Notice This is not a final specification. Some parametric limits are Subject to change.

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

DESCRIPTION

The M54965ASP is a semiconductor integrated circuit consisting of an oxide-film separated ECL/I^2L PLL frequency synthesizer. A prescaler and PLL capable of withstanding operating at a maximum frequency of 1.0GHz are housed in a single chip.

FEATURES

- Built-in prescaler with input amplifier f_{max}=1.0GHz
- Serial data input
- Fine tuning capability (31.25KHz/step)
- Built-in band output
- 5V single power supply

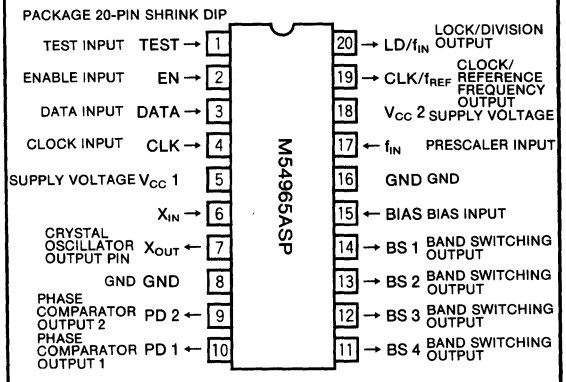
APPLICATION

TV and VTR tuners

FUNCTION

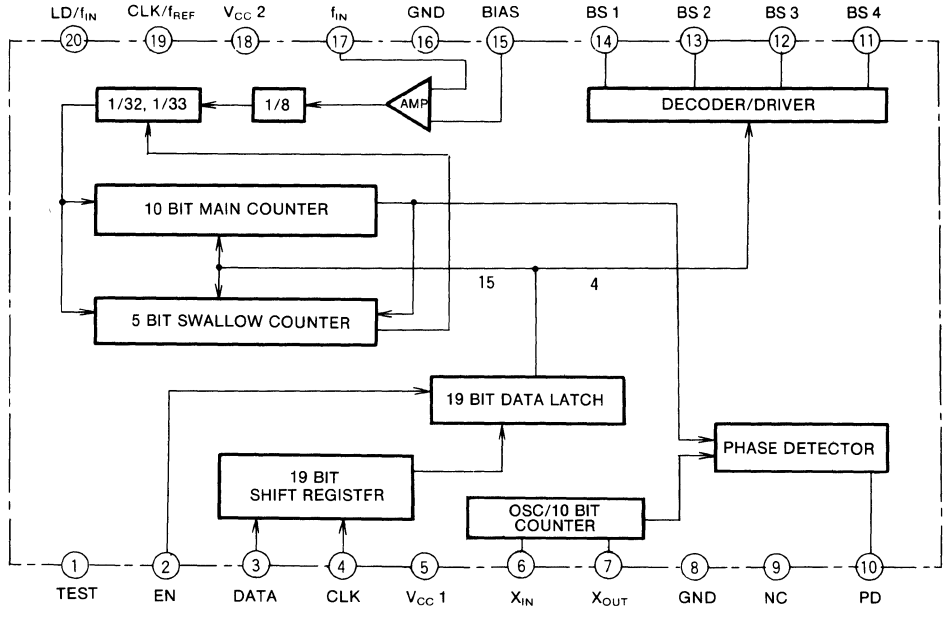
The M54965ASP is a PLL frequency synthesizer IC for TV applications. The prescaler employs emitter-coupled logic, and the PLL, I^2L. The maximum operating frequency of the prescaler is 1.0GHz. The first stage is a fixed 1/8 2-modulus prescaler and the second stage is a 1/32, 1/33 2-modulus prescaler. The PLL consists of a 4MHz crystal oscillator, a 10-bit reference frequency divider, a programmable divider (a 10-bit M counter and a 5-bit S counter), a phase comparator, and a lock detector. Four band switching circuits are also provided.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

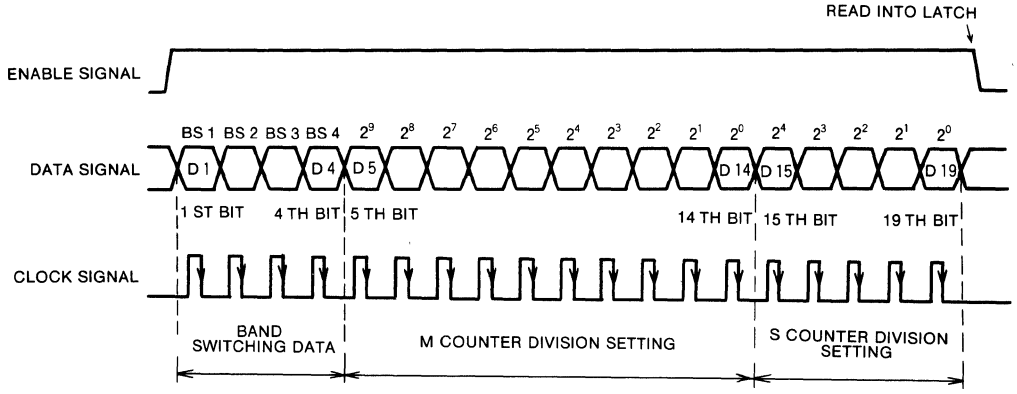
BLOCK DIAGRAM



PIN DESCRIPTION

Pin number	Symbol	Pin name	Functional description
5 18	$V_{CC}1$ (IIL) $V_{CC}2$ (ECL)	Supply voltage 1 (I^2L) Supply voltage 2 (ECL)	Prescaler supply voltage pin 5.0+0.5V is applied I_2L supply voltage pin 5.0+0.5V is applied
8 16	GND 1 (IIL) GND2(ECL)	GND 1 (I^2L) GND 2 (ECL)	Connect to 0V Connect to 0V
6 7	X_{IN} X_{OUT}	Crystal oscillator output pin	4.0MHz crystal oscillator is connected.
17 15	f_{IN} BIAS	Prescaler input pin Bias pin	Prescaler input pin, V, C, O frequency is applied Prescaler bias pin, capacitance of 1000pF is inserted between GND and this pin.
2	ENABLE	Enable input	Normally set low. When high, 19-bit data is read into the shift register. When it drops from high to low, the contents of the shift registers are read into the latch.
4	CLOCK	Clock input	Data is read into shift register at the falling edge of the clock signal.
3	DATA	Data input	Programmable divider division setting input
19	CLK/f_{REF}	Clock/reference frequency output	When the TEST input is low, the 500kHz clock frequency (CLK) is output. When TEST is high, the reference frequency output f_{REF} is output. The reference frequency is 3.90625kHz. (Open-collector output)
20	LD/f_{IN}	Lock detector/division output	When the TEST input is low, the lock detector output (LD) is selected; when TEST is high, the programmable divider output (f 1/N) is selected. The lock detector output is normally high and becomes low for a period corresponding to the phase difference between f_{REF} and f 1/N. (Open collector output)
1	TEST	TEST input	This pin is used for testing and is normally set low. When set high, f_{REF} and f 1/N outputs are selected for CLK/f_{REF} and LD/f 1/N, and the phase comparator output enters the high-impedance state.
10 9	PD 1 PD 2	Phase comparator output 1 Phase comparator output 2	When the phase programmable divider output (f 1/N) is advanced with respect to the reference frequency (f_{REF}), this output becomes high, and when the programmable divider output is delayed, it becomes low. When the two are in sync, this output enters the high-impedance state.
14 13 12 11	BS 1 BS 2 BS 3 BS 4	Band switching output pin	Open-collector outputs are used at all four band switching output pins. When the band switching data is high, the output is ON, and when low, the output is OFF.

How to set the dividing ratio of programmable divider and select the band switching output
The output is read into the latch at the falling edge of enable signal, as shown below.



Total divisor N is given by the following formulas in addition to the prescaler used in the previous stage

$N = 8(32M+S)$

M : 10-bit main counter division
S : 5-bit swallow counter division

The M and S counters are binary and the possible ranges of division are as follows.

$32 \leqq M \leqq 1023$

$0 \leqq S \leqq 31$

The range of divisors N is 8, 136 and 192~262.
The tuning frequency f_{VCO} is given in the following equations.

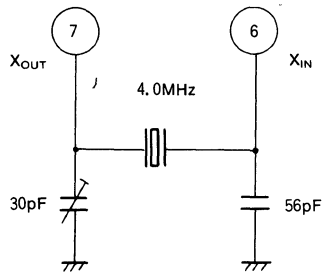
$f_{VCO} = f_{REF} \times N$

$= 3.90625 \times 8(32M+S)$

$= 31.25(32M+S)$(kHz)

Therefore, the range of tuning frequencies is 32MHz — 1000MHz.

CRYSTAL OSCILLATOR CONNECTION DIAGRAM



CRYSTAL OSCILLATOR CHARACTERISTICS

Actual resistance : less than 50Ω
Load capacitance : 20pF

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

ABSOLUTE MAXIMUM RATINGS (T_a=−25∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
VI	Input voltage	Do not exceed supply voltage (V_{CC})	6.5	V
V_O 1	Output voltage (1)	Do not exceed PD output supply voltage	5.5	V
V_O 2	Output voltage (2)	Do not exceed output supply voltage (V_{CC}) other than mentioned above	6.5	V
VBD	Output withstanding voltage	Band switching switch	13.5	V
Pd	Power dissipation		650	mW
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Conditions	Limits	Unit
V_{CC}	Supply voltage			4.5∼5.5	V
fopr 1	Operating frequency (1)		Crystal oscillator	4.0	MHz
fopr 2	Operating frequency (2)		f_{IN} input	80∼1000	MHz
I_{OL}	Low-level output current	19 20		0∼5	mA
IBDL	Low-level band output current	11 12 13 14		0∼1	mA

ELECTRICAL CHARACTERISTICS (T_a=−20∼75℃, unless otherwise noted)

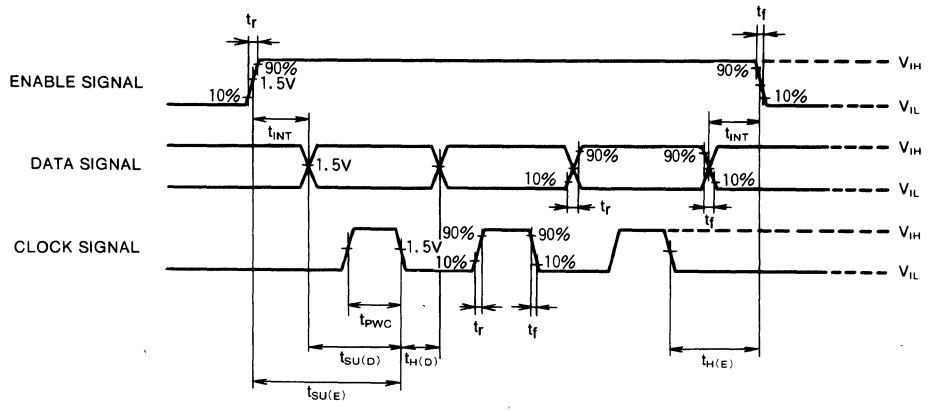
Symbol	Parameter		Test pin	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage		1, 2, 3, 4		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		1, 2, 3, 4				0.7	V
I_{IH}	High-level input current 1		1, 2, 3, 4	V_{CC}=5.5V, V_I=2.7V			50	μA
I_{IL} 1	Low-level input current 1		1, 2, 3, 4	V_{CC}=5.5V, V_I=0.4V		−100	−200	μA
I_{IL} 2	Low-level input current 2		2	V_{CC}=5.5V, V_I=0.4V		−550	−900	μA
I_{IC}	Input clamp voltage		1, 2, 3, 4	V_{CC}=4.5V, V_{IC}=1.0mA		−1.3	−1.8	V
V_{OH}	High-level output voltage	PD output	10	V_{CC}=4.5V, I_{OH}=−1.0mA	2.5	3.0		V
V_{OL} 1	Low-level output voltage	PD output	10	V_{CC}=4.5V, I_{OL}=−1.0mA		0.2	0.4	V
V_{OL} 2		Other than above	19, 20	V_{CC}=4.5V, I_{OL}=5mA		0.3	0.5	V
I_{OLK} 1	Output leakage current	PD output	10	V_{CC}=5.5V, V_O=0.5∼4.8V	−1.0		+1.0	μA
I_{OLK} 2		Other than above	19, 20	V_{CC}=5.5V, V_O=5.5V	−10		+10	μA
I_{CC}	Supply current		5, 18	V_{CC}=5.5V		70	100	mA

Typical values are at V_{CC}=5.0V, T_a=25℃

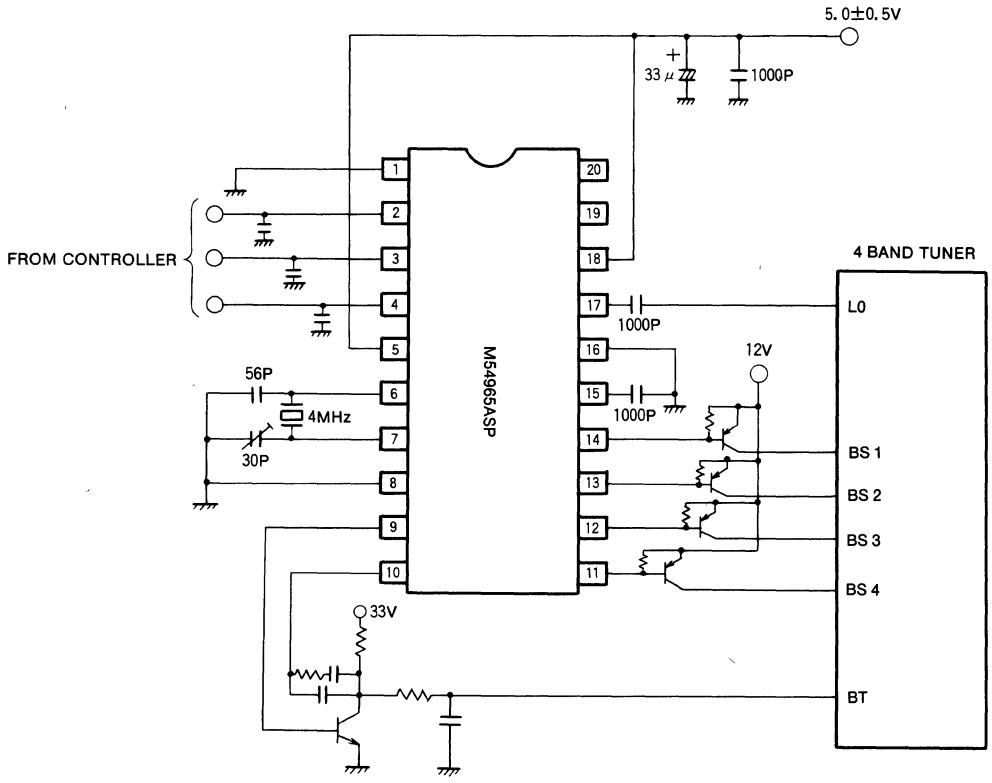
SWITCHING CHARACTERISTICS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
f_{opr}	Prescaler operating frequency	17	V_{CC}=4.5∼5.5V V_{IN}=V_{INmin}∼V_{INmax}		80		1000	V
V_{IN}	Operating input voltage	17	80∼150MHz 150∼1000MHz	V_{CC}=4.5∼5.5V	−20 −27		4 4	dBm
t_{PWC}	Clock pulse width	4	V_{CC}=4.5∼5.5V		10			μA
$t_{SU(D)}$	Data setup time	3			10			μA
$t_{H(D)}$	Data hold time	3			10			μA
$t_{SU(E)}$	Enable setup time	2			20			μA
$t_{H(E)}$	Enable hold time	2			20			μA
t_{INT}	Enable data interval time	2, 3			10			μA
t_r	Rising time	2, 3, 4					1	μA
t_f	Falling time	2, 3, 4					1	μA

TIMING DIAGRAM



APPLICATION EXAMPLE



M54967ASP

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

DESCRIPTION

The M54967ASP is a semiconductor integrated circuit consisting of an oxide-film separated ECL/I^2L PLL frequency synthesizer. A prescaler and PLL capable of operating at a maximum frequency of 1.0GHz are housed in a single chip.

FEATURES

- Built-in prescaler with input amplifier f_{max}=1.0GHz
- Serial data input
- Fine tuning capability (62.5kHz/step)
- Built-in band output
- 5V single power supply

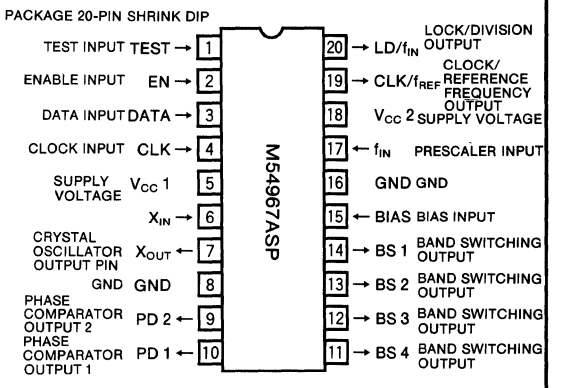
APPLICATION

TV and VTR tuners

FUNCTION

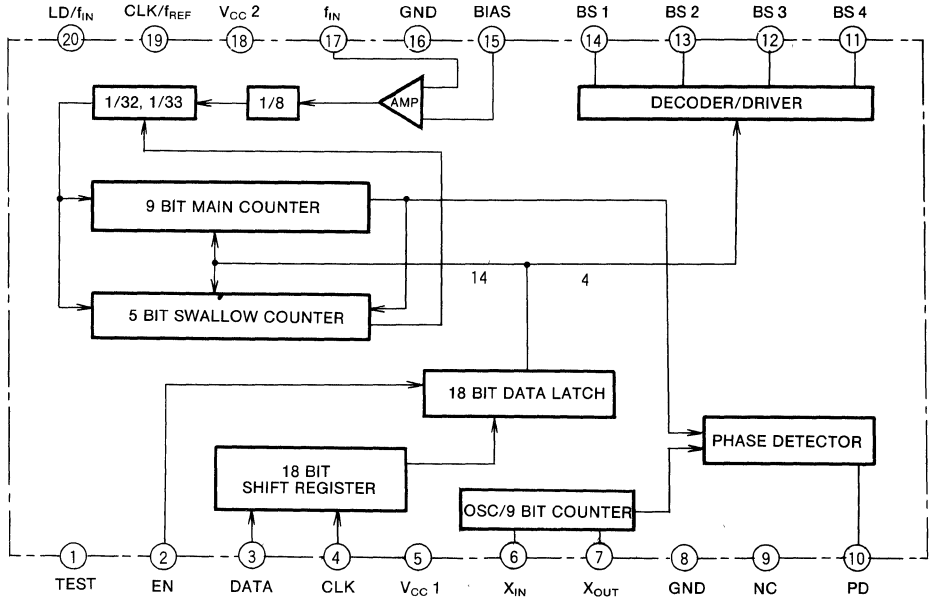
The M54967ASP is a PLL frequency synthesizer IC for TV applications. The prescaler employs emitter-coupled logic, and the PLL, I^2L. The maximum operating frequency of the prescaler is 1.0GHz. The first stage is a fixed 1/8 2-modulus prescaler and the second stage is a 1/32, 1/33 2-modulus prescaler. The PLL consists of a 4MHz crystal oscillator, a 9-bit reference frequency divider, a programmable divider (a 9-bit M counter and a 5-bit S counter), a phase comparator, and a lock detector. Four band switching circuits are also provided.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

BLOCK DIAGRAM

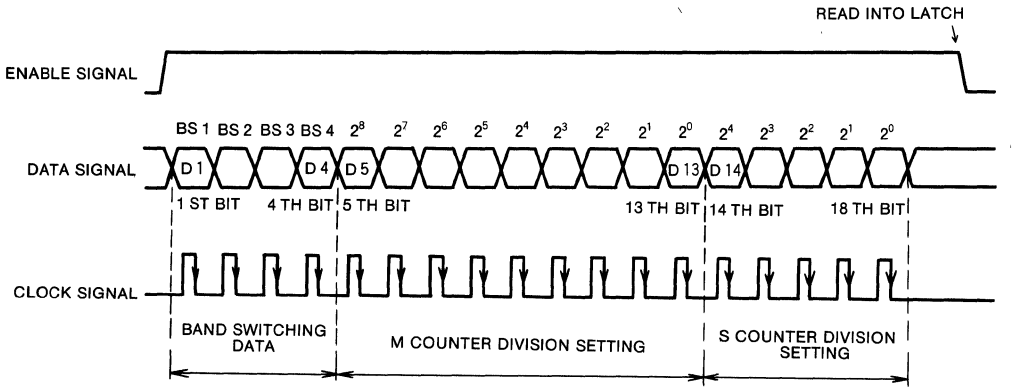


MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin number	Symbol	Pin name	Functional description
5 18	$V_{CC}1$ (IIL) $V_{CC}2$ (ECL)	Supply voltage 1 (I2L) Supply voltage 2 (ECL)	Prescaler supply voltage pin 5.0+0.5V is applied I_2L supply voltage pin 5.0+0.5V is applied
8 16	GND 1 (IIL) GND2(ECL)	GND 1 (I2L) GND 2 (ECL)	Connect to 0V Connect to 0V
6 7	X_{IN} X_{OUT}	Crystal oscillator output pin	4.0MHz crystal oscillator is connected
17 15	f_{IN} BIAS	Prescaler input pin Bias pin	Prescaler input pin, V. C. O frequency is applied. Prescaler bias pin, capacitance of 1000pF is inserted between GND and this pin
2	ENABLE	Enable input	Normally set low When high, 15-bit data is read into the shift register When it drops from high to low, contents of the shift register are read into the latch
4	CLOCK	Clock input	Data is read into the shift register at the falling edge of clock signal
3	DATA	Data input	Programmable divider division setting input
19	CLK/f_{REF}	Clock/reference frequency output	When the TEST input is low, the 400kHz clock frequency (CLK) is output When TEST is high, the reference frequency output f_{REF} is output The reference frequency is 7.8125kHz (Open-collector output)
20	LD/f_{IN}	Lock detector/division output	When the TEST input is low, the lock detector output (LD) is selected, when TEST is high, the programmable divider output (f 1/N) is selected The lock detector output is normally high and becomes low for a period corresponding to the phase difference between f_{REF} and f 1/N (Open collector output)
1	TEST	TEST input	This pin is used for testing and is normally set low When set high, f_{REF} and f 1/N outputs are selected for CLK/f_{REF} and LD/f 1/N, and the phase comparator output enters the high-impedance state.
10 9	PD 1 PD 2	Phase comparator output 1 Phase comparator output 2	When the phase programmable divider output (f 1/N) is advanced with respect to the reference frequency (f_{REF}), this output becomes high, and when the programmable divider output is delayed, it becomes low When the two are in sync, this output enters the high-impedance state
14 13 12 11	BS 1 BS 2 BS 3 BS 4	Band switching output pin	Open-collector outputs are used at all four band switching output pins When the band switching data is high, the output is ON, and when low, the output is OFF

How to set the dividing ratio of programmable divider and band switching output
The output is read into the latch at the falling edge of enable signal, as shown below.



Total division N is given by the following formulas in addition to the prescaler used in the previous stage

$N = 8(32M+S)$

M : 9-bit main counter division
S : 5-bit swallow counter division

The M and S counters are binary and the possible ranges of division are as follows.

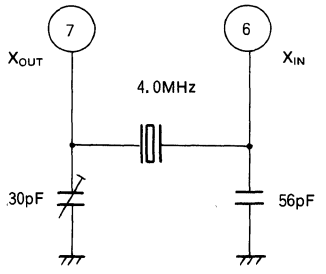
$32 \leqq M \leqq 511$
$0 \leqq S \leqq 31$

Therefore, the range of divisors N is 8, 64, and 131~192.
The tuning frequency f_{VCO} is given in the following equations.

$f_{VCO} = f_{REF} \times N$
$= 7.8125 \times 8 (32M+S)$
$= 62.5 (32M+S)$ (kHz)

Therefore, the range of tuning frequency is 64MHz — 1000MHz.

CRYSTAL OSCILLATOR CONNECTION DIAGRAM



CRYSTAL OSCILLATOR CHARACTERISTICS

Actual resistance : less than 50Ω
Load capacitance : 20pF

MITSUBISHI ELECTRIC

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

ABSOLUTE MAXIMUM RATINGS (T_a=−25～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
VI	Input voltage	Do not exceed supply voltage (V_{CC})	6.5	V
V_O 1	Output voltage (1)	Do not exceed PD output supply voltage	5.5	V
V_O 2	Output voltage (2)	Do not exceed output supply voltage (V_{CC}) other than mentioned above	6.5	V
VBD	Output withstanding voltage	Band switching switch	13.5	V
P_d	Power dissipation		650	mW
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−40～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Conditions	Limits	Unit
V_{CC}	Supply voltage			4.5～5.5	V
fopr 1	Operating frequency (1)		Crystal oscillator	4.0	MHz
fopr 2	Operating frequency (2)		f_{IN}	80～1000	MHz
I_{OL}	Low-level output current	19 20		0～5	mA
IBDL	Low-level band output current	11 12 13 14		0～1	mA

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, unless otherwise noted)

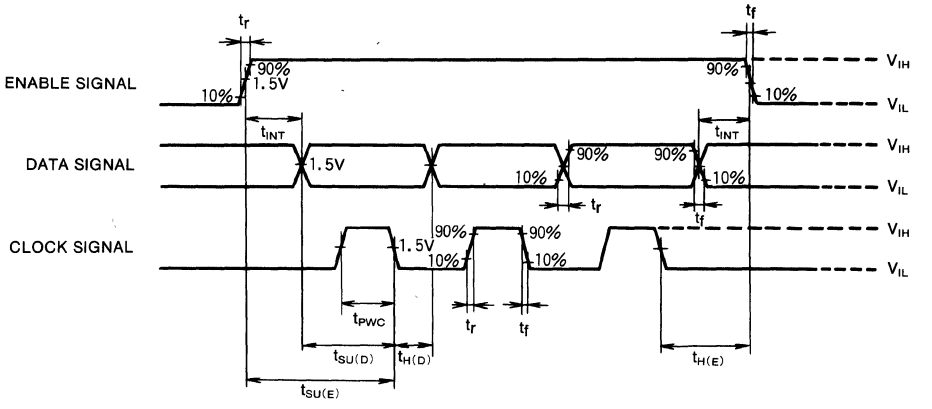
Symbol	Parameter		Test pin	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage		1, 2, 3, 4		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		1, 2, 3, 4				0.7	V
I_{IH}	High-level input current 1		1, 2, 3, 4	V_{CC}=5.5V, V_I=2.7V			50	μA
I_{IL} 1	Low-level input current 1		1, 2, 3, 4	V_{CC}=5.5V, V_I=0.4V		−100	−200	μA
I_{IL} 2	Low-level input current 2		2	V_{CC}=5.5V, V_I=0.4V		−550	−900	μA
I_{IC}	Input clamp voltage		1, 2, 3, 4	V_{CC}=4.5V, V_{IC}=1.0mA		−1.3	−1.8	V
V_{OH}	High-level output voltage	PD output	10	V_{CC}=4.5V, I_{OH}=−1.0mA	2.5	3.0		V
V_{OL} 1	Low-level output voltage	PD output	10	V_{CC}=4.5V, I_{OL}=−1.0mA		0.2	0.4	V
V_{OL} 2		Other than above	19, 20	V_{CC}=4.5V, I_{OL}=5mA		0.3	0.5	V
I_{OLK} 1	Output leakage current	PD output	10	V_{CC}=5.5V, V_O=0.5～4.8V	−1.0		+1.0	μA
I_{OLK} 2		Other than above	19, 20	V_{CC}=5.5V, V_O=5.5V	−10		+10	μA
I_{CC}	Supply current		5, 18	V_{CC}=5.5V		70	100	mA

Typical values are at V_{CC}=5.0V, T_a=25℃.

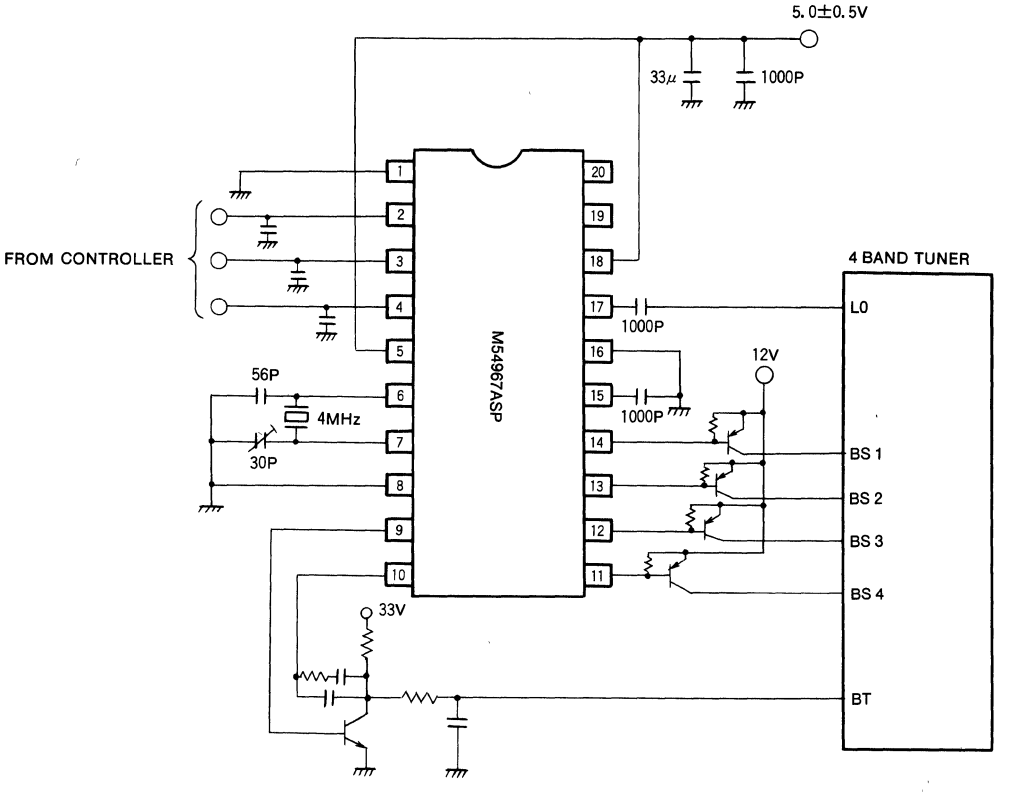
SWITCHING CHARACTERISTICS (T_a=−20～75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
f_{opr}	Prescaler operating frequency	17	V_{CC}=4.5～5.5V V_{IN}=V_{INmin}～V_{INmax}		80		1000	V
V_{IN}	Operating input voltage	17	80～150MHz 150～1000MHz	V_{CC}=4.5～5.5V	−20 −27		4 4	dBm
t_{PWC}	Clock pulse width	4	V_{CC}=4.5～5.5V		10			μA
$t_{SU(D)}$	Data setup time	3			10			μA
$t_{H(D)}$	Data hold time	3			10			μA
$t_{SU(E)}$	Enable setup time	2			20			μA
$t_{H(E)}$	Enable hold time	2			20			μA
t_{INT}	Enable data interval time	2, 3			10			μA
t_r	Rising time	2, 3, 4					1	μA
t_f	Falling time	2, 3, 4					1	μA

TIMING DIAGRAM



APPLICATION EXAMPLE



MITSUBISHI ELECTRIC

M54968ASP

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR VTR

DESCRIPTION

The M54968ASP is a semiconductor integrated circuit consisting of an oxide-film separated ECL/I^2L PLL frequency synthesizer. A prescaler and PLL capable of operating at a maximum frequency at 1.0GHz are housed in a single chip.

FEATURES

- Built-in prescaler with input amplifier f_{max}=1.0GHz
- Serial data input
- Fine tuning capability (50KHz/step)
- Built-in band output
- 5V single power supply

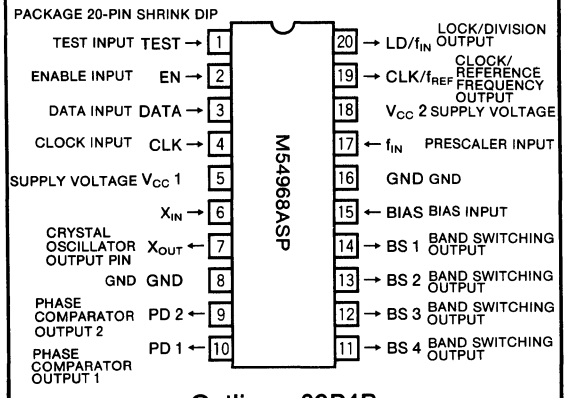
APPLICATION

TV and VTR tuners

FUNCTION

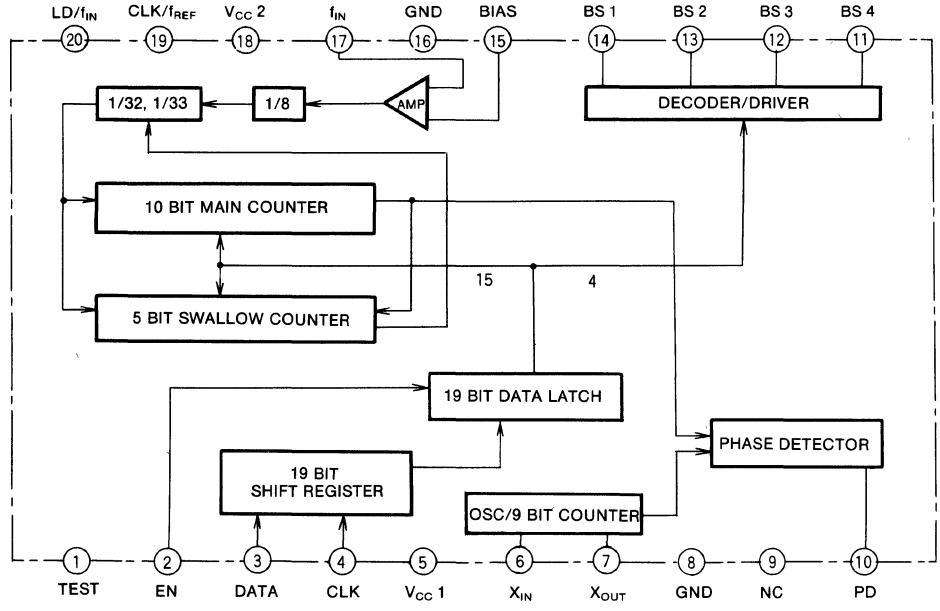
The M54968ASP is a PLL frequency synthesizer IC for TV applications. The prescaler employs emitter-coupled logic and the PLL, I^2L. The maximum operating frequency of the prescaler is 1.0GHz. The first stage is a fixed 1/8 2-modulus prescaler and the second stage is a 1/32, 1/33 2-modulus prescaler. The PLL consists of a 4MHz crystal oscillator, a 9-bit reference frequency divider, a programmable divider (a 10-bit M counter and a 5-bit S counter), a phase comparator, and a lock detector. Four band switching circuits are also provided.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

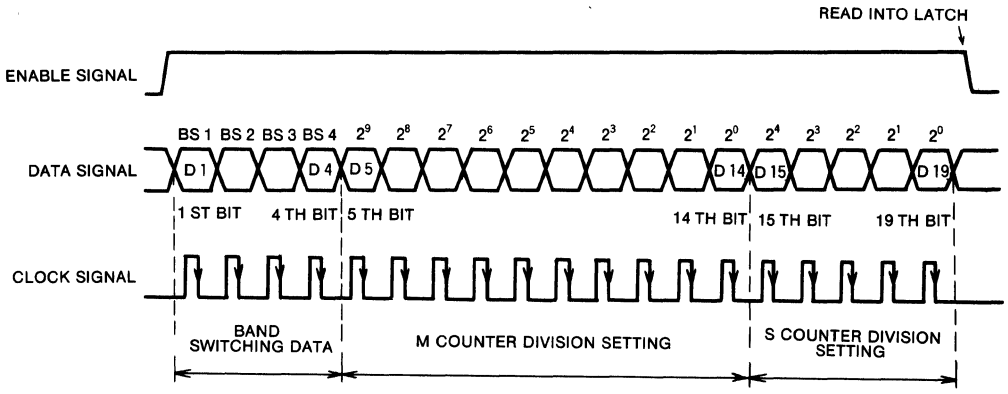
BLOCK DIAGRAM



PIN DESCRIPTION

Pin number	Symbol	Pin name	Functional description
5 18	$V_{CC}1$ (IIL) $V_{CC}2$ (ECL)	Supply voltage 1 (I^2L) Supply voltage 2 (ECL)	Prescaler supply voltage pin 5.0+0.5V is applied I2L supply voltage pin 5.0+0.5V is applied
8 16	GND 1 (IIL) GND2(ECL)	GND 1 (I^2L) GND 2 (ECL)	Connect to 0V Connect to 0V
6 8	X_{IN} X_{OUT}	Crystal oscillator output pin	4.0MHz crystal oscillator is connected.
17 15	f_{IN} BIAS	Prescaler input pin Bias pin	Prescaler input pin, V, C, O frequency is applied Prescaler bias pin, capacitance of 1000pF is inserted between GND and this pin
2	ENABLE	Enable input	Normally set low. When high, 15-bit data is read into the shift register When it drops from high to low, the contents of the shift registers are read into the latch
4	CLOCK	Clock input	Data is read into the shift register at the falling edge of the clock signal
3	DATA	Data input	Programmable divider division setting input
19	CLK/f_{REF}	Clock/reference frequency output	When the TEST input is low, the 400kHz clock frequency (CLK) is output. When TEST is high, the reference frequency output f_{REF} is output. The reference frequency is 6.25kHz. (Open-collector output)
20	LD/f_{IN}	Lock detector/division output	When the TEST input is low, the lock detector output (LD) is selected, when TEST is high, the programmable divider output (f 1/N) is selected The lock detector output is normally high and becomes low for a period corresponding to the phase different between f_{REF} and f 1/N (Open collector output)
1	TEST	TEST input	This pin is used for testing and is normally set low. When set high, f_{REF} and f 1/N outputs are selected for CLK/f_{REF} and LD/f 1/N, and the phase comparator output enters the high-impedance state
10 9	PD 1 PD 2	Phase comparator output 1 Phase comparator output 2	When the phase programmable divider output (f 1/N) is advanced with respect to the reference frequency (f_{REF}), this output becomes high, it becomes low. When the two are in sync, this output enters the high-impedance state.
14 13 12 11	BS 1 BS 2 BS 3 BS 4	Band switching output pin	Open-collector output are used at all four band switching output pin When the band switching data is high, the output is ON, and when low, the output is OFF.

How to set the division of programmable divider and select the band switching output
The output is read into the latch at the falling edge of enable signal, as shown below.



Total divisor N is given by the following formulas in addition to the prescaler used in the previous stage.

$N = 8(32M+S)$

M : 10-bit main counter division
S : 5-bit swallow counter division

The M and S counters are binary and the possible ranges of division are as follows.

$32 \leqq M \leqq 1023$

$0 \leqq S \leqq 31$

The range of diviors N is 8, 136 and 192~262.
The tuning frequency f_{VCO} is given in the following equations.

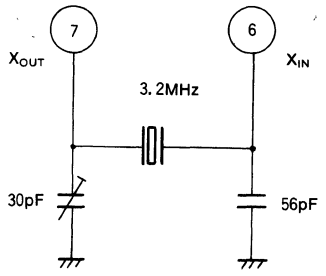
$f_{VCO} = f_{REF} \times N$

$= 6.25 \times 8 (32M+S)$

$= 50 (32M+S)$ (kHz)

Therefore, the range of tuning frequencies is 51.2MHz — 1000MHz.

CRYSTAL OSCILLATOR CONNECTION DIAGRAM



CRYSTAL OSCILLATOR CHARACTERISTICS

Actual resistance : less than 50Ω
Load capacitance : 20pF

ABSOLUTE MAXIMUM RATINGS (T_a=−25∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		6.5	V
VI	Input voltage	Do not exceed supply voltage (V_{CC})	6.5	V
V_O 1	Output voltage (1)	Do not exceed PD output supply voltage	5.5	V
V_O 2	Output voltage (2)	Do not exceed output supply voltage (V_{CC}) other than mentioned above	6.5	V
VBD	Output withstanding voltage	Band switching switch	13.5	V
P_d	Power dissipation		650	mW
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Conditions	Limits	Unit
V_{CC}	Supply voltage			4.5∼5.5	V
fopr 1	Operating frequency (1)		Crystal oscillator	4.0	MHz
fopr 2	Operating frequency (2)		f_{IN}	80∼1000	MHz
I_{OL}	Low-level output current	19 20		0∼5	mA
IBDL	Low-level band output current	11 12 13 14		0∼2	mA

ELECTRICAL CHARACTERISTICS (T_a=−20∼75℃, unless otherwise noted)

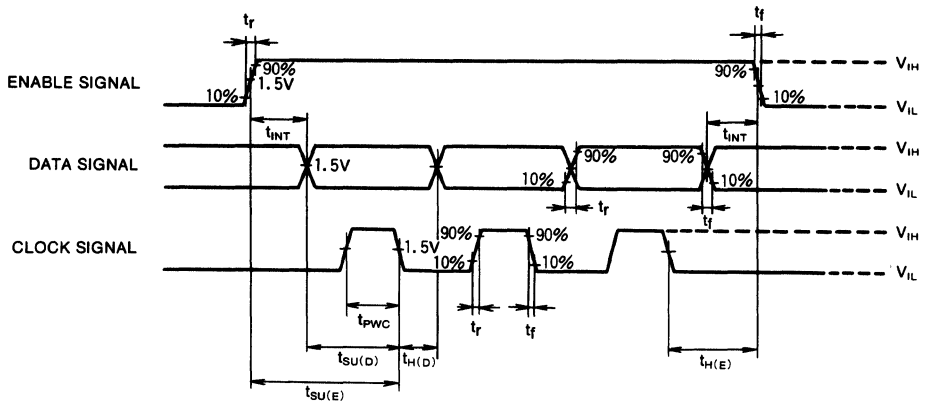
Symbol	Parameter		Test pin	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage		1, 2, 3, 4		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		1, 2, 3, 4				0.7	V
I_{IH}	High-level input current 1		1, 2, 3, 4	V_{CC}=5.5V, V_I=2.7V			50	μA
I_{IL} 1	Low-level input current 1		1, 2, 3, 4	V_{CC}=5.5V, V_I=0.4V		−100	−200	μA
I_{IL} 2	Low-level input current 2		2	V_{CC}=5.5V, V_I=0.4V		−550	−900	μA
I_{IC}	Input clamp voltage		1, 2, 3, 4	V_{CC}=4.5V, V_{IC}=1.0mA		−1.3	−1.8	V
V_{OH}	High-level output voltage	PD output	10	V_{CC}=4.5V, I_{OH}=−1.0mA	2.5	3.0		V
V_{OL} 1	Low-level output voltage	PD output	10	V_{CC}=4.5V, I_{OL}=−1.0mA		0.2	0.4	V
V_{OL} 2		Other than above	19, 20	V_{CC}=4.5V, I_{OL}=5mA		0.3	0.5	V
I_{OLK} 1	Output leakage current	PD output	10	V_{CC}=5.5V, V_O=0.5∼4.8V	−1.0		+1.0	μA
I_{OLK} 2		Other than above	19, 20	V_{CC}=5.5V, V_O=5.5V	−10		+10	μA
I_{CC}	Supply current		5, 18	V_{CC}=5.5V		70	100	mA

Typical values are at V_{CC}=5.0V, T_a=25℃.

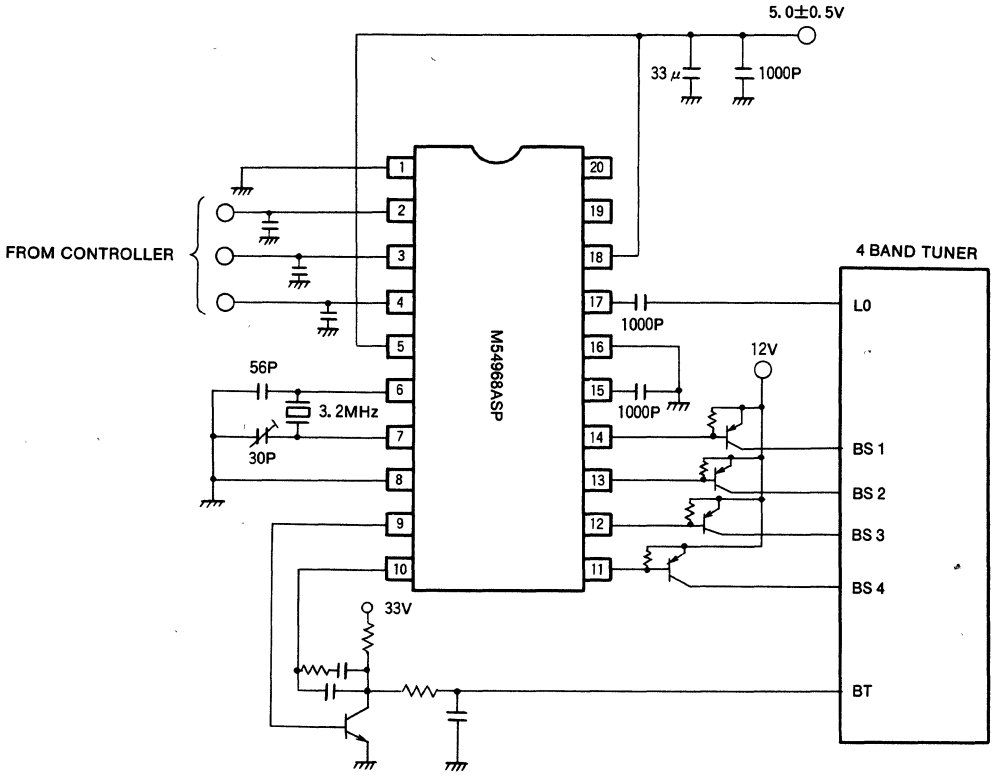
SWITCHING CHARACTERISTICS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
f_{opr}	Prescaler operating frequency	17	V_{CC}=4.5∼5.5V V_{IN}=V_{INmin}∼V_{INmax}		80		1000	V
V_{IN}	Operating input voltage	17	80∼150MHz 150∼1000MHz	V_{CC}=4.5∼5.5V	−20 −27		4 4	dBm
t_{PWC}	Clock pulse width	4	V_{CC}=4.5∼5.5V		10			μA
$t_{SU(D)}$	Data setup time	3			10			μA
$t_{H(D)}$	Data hold time	3			10			μA
$t_{SU(E)}$	Enable setup time	2			20			μA
$t_{H(E)}$	Enable hold time	2			20			μA
t_{INT}	Enable data interval time	2, 3			10			μA
t_r	Rising time	2, 3, 4					1	μA
t_f	Falling time	2, 3, 4					1	μA

TIMING DIAGRAM



APPLICATION EXAMPLE



M54970P

9-BIT SERIAL-INPUT,LATCHED DRIVER

DESCRIPTION

The M54970P is a semiconductor integrated circuit of I^2L structure containing a serial input to serial/parallel output 9-bit shift register and latch as well as a bipolar 9-bit parallel-output driver.

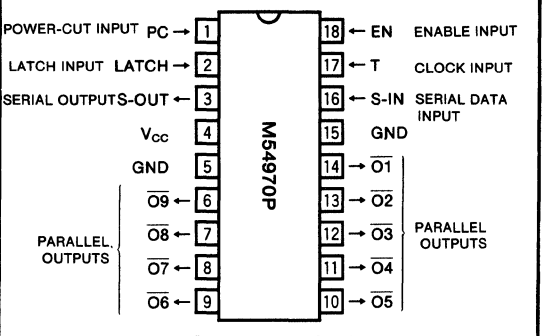
FEATURES

- Serial input to serial/parallel output
- Cascade connections possible through serial output
- Enable input for output control
- Power-cut input
- Driver : Withstand voltage ····· $BV_{CEO} \geqq 20V$
  Large drive current ····· $(I_{O(max)}=300mA)$
- Wide operating temperature range···· $T_a=-20\sim+75℃$

APPLICATION

Thermal printer head dot driver, Serial-to-parallel conversion, Relay and Solenoid driver

PIN CONFIGURATION (TOP VIEW)



Outline 18P4

FUNCTION

The M54970P consists of a 9bit D-type flip-flop, the output of which is connected to 9 latches.

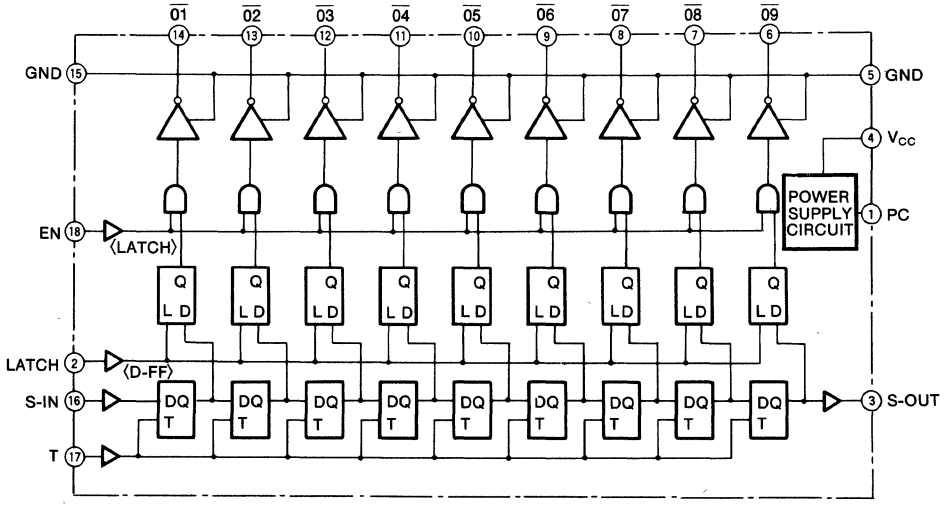
When data is applied to the serial data input (S-IN) and a clock pulse is applied to clock input (T), an "L" to "H" change of the clock will cause the data input signals to enter the internal shift registers and the data in the shift registers will be shifted in order.

Using a number of M54970P units for bit expansion in series will entail connecting serial output (S-OUT) to S-IN of the next-stage M54970P.

In parallel output, when the power-cut input and latch input are set to "H" and the output-control input (enable input EN) is "H", a clock pulse changing from "L" to "H" will cause the serial data input signal to appear at output $\overline{01}$, and the data will be shifted in order at outputs $\overline{02}\sim\overline{09}$.

The parallel output will yield a signal that is inverted with respect to the serial data input.

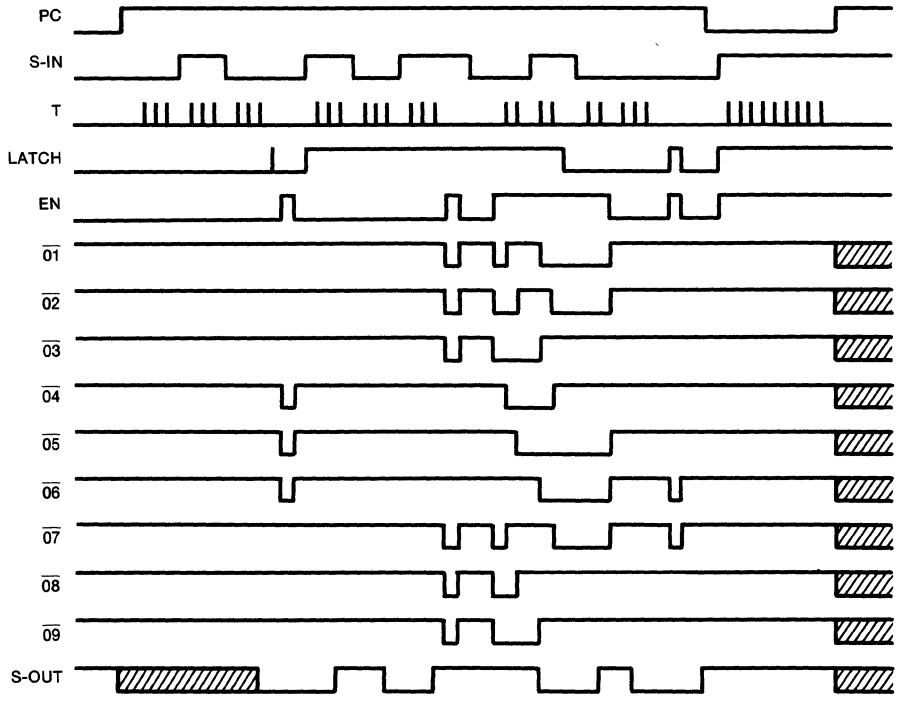
BLOCK DIAGRAM



MITSUBISHI ELECTRIC

Setting the LATCH input to "L" will prevent data from entering the latch.
When the EN input is set to "L", all outputs ($\overline{01}$~$\overline{09}$) will be set to OFF. Since the internal logic state of the IC is uncertain at power-on time, set the EN input to "L" (and outputs $\overline{01}$~$\overline{09}$ will be set to OFF) until the input data is set and the internal logic state has been detrmined.
The power will be cut when the power-cut input is set to "L", and since the data of the shift registers and latches are not maintained in this state, it will be necessary to input data again in order to set the output following a change of PC input from "L" to "H".

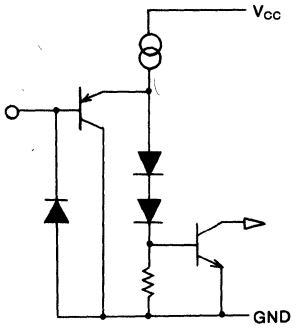
TIMING CHART



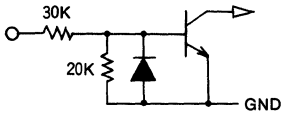
*The state of the shaded areas is uncertain.

INPUT/OUTPUT EQUIVALENT CIRCUIT SCHEMATICS

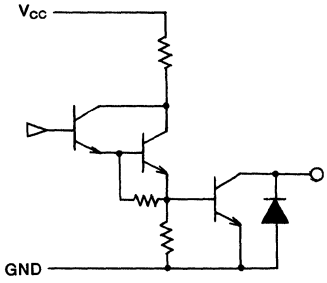
1 T, S-IN, LATCH INPUTS



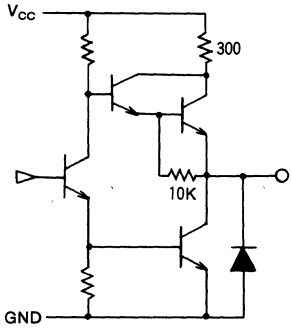
2 PC, EN INPUTS



3 $\overline{O1}$~$\overline{O9}$ OUTPUTS



4 S-OUT OUTPUT



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=−20℃～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+8	V
V_I	Input voltage		−0.5～+10	V
V_O	Output voltage	Output is OFF	−0.5～+20	V
I_O	Output current		350	mA
Pd	Power dissipation	T_a=25℃	1.25	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_O	Applied output voltage	When output is OFF			20	V
I_O	Output current (per circuit)	All outputs ON simultaneously Duty cycle less than 30%			300	mA

ELECTRICAL CHARACTERISTICS (T_a=+25℃, unless otherwise noted)

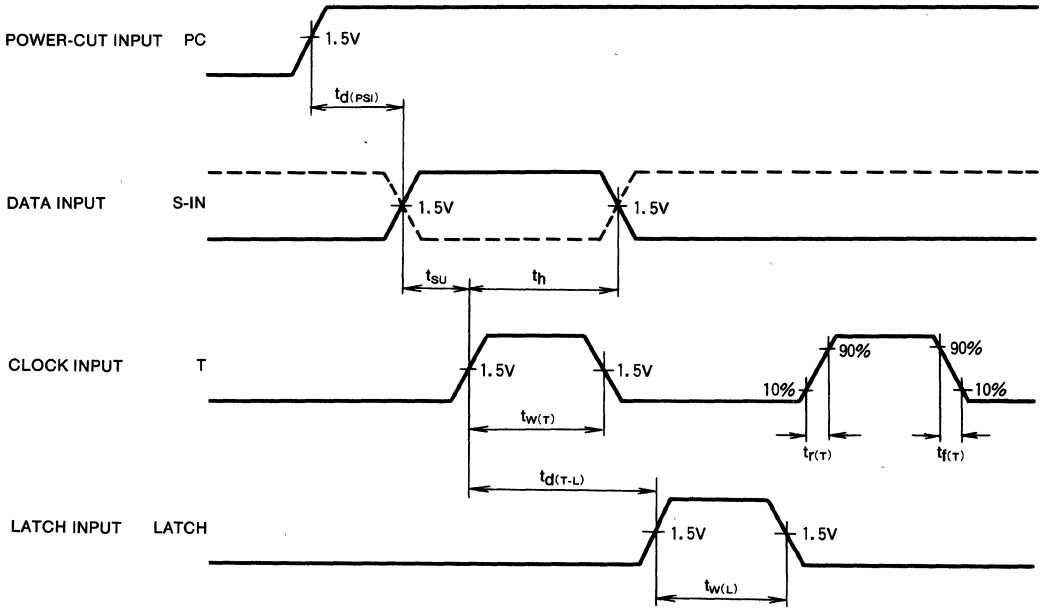
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage	2, 16, 17	T_a=−20～+75℃	2.2		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
V_{IH}	High-level input voltage	1, 18	T_a=−20～+75℃	2.2		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
I_{IH}	High-level input current	2, 16, 17	V_{CC}=5.5V, V_{IH}=2.4V			10	μA
I_{IL}	Low-level input current		V_{CC}=5.5V, V_{IL}=0.4V			−50	μA
I_{IH}	High-level input current	1, 18	V_{CC}=5.5V, V_{IH}=5.5V			250	μA
			V_{CC}=5.5V, V_{IH}=2.4V			100	
I_{IL}	Low-level input current		V_{CC}=5.5V, V_{IL}=0V			−10	μA
V_{OH}	High-level output voltage	3	V_{CC}=4.5V, I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=8mA			0.4	V
V_{OL}	Low-level output voltage	6～14	V_{CC}=4.5V, I_{OL}=300mA			0.6	V
I_{CC1}	Supply current	4	V_{CC}=5.5V, power-cut is ON			10	μA
I_{CC2}			V_{CC}=5.5V, EN is "L"		10	15	mA
I_{CC3}			V_{CC}=5.5V, all outputs are ON		90	130	mA
$I_{O(leak)}$	Output leakage current	6～14	V_{CC}=5.5V, V_{OH}=20V			100	μA

* : Typical values are at T_a = 25℃.

REQUIRED TIMING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$f_{(T)}$	Clock frequency	Input duty cycle 40~60%			1	MHz
$t_{W(T)}$	Clock pulse width		0.4			μS
$t_{W(L)}$	Latch pulse width		0.4			μS
t_{SU}	Data setup time		0.2			μS
t_h	Data hold time		0.3			μS
$t_{d(T-L)}$	Clock-latch time		1			μS
$t_{r(T)}$	Clock pulse rise time				0.5	μS
$t_{f(T)}$	Clock pulse fall time				0.5	μS
$t_{d(P-SI)}$	Power-cut input → data input setting tiwe	Hold EN input at "L" when PC input is changed from "L" to "H"	2			μS

TIMING DIAGRAM

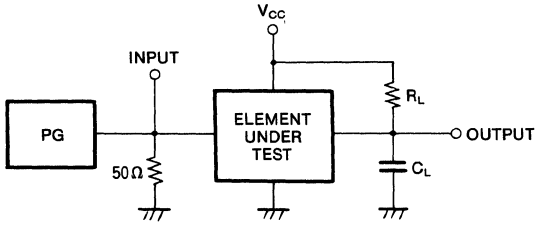


MITSUBISHI ELECTRIC

SWITCHING CHARACTERISTICS (T_a=25℃, V_{CC}=5V)

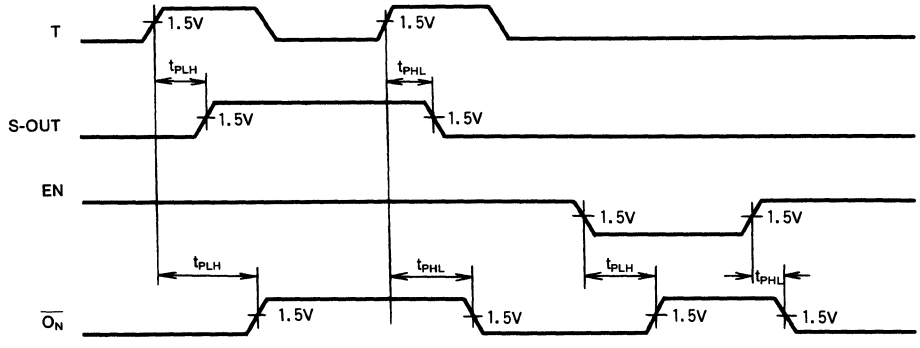
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low to high-level output propagation time (Input T to output S-OUT)	V_{IH}=3V V_{IL}=0V R_L : S_{-OUT}=2KΩ R_L : $\overline{O_N}$=100Ω (N=1~9) C_L=15pF (Note 1)			0.7	μS
t_{PHL}	High to low-level output propagation time (Input T to output S-OUT)				0.8	μS
t_{PLH}	Low to high-level output propagation time (Input T to output $\overline{O_N}$)				5	μS
t_{PHL}	High to low-level output propagation time (Input T to output $\overline{O_N}$)				1	μS
t_{PLH}	Low to high-level output propagation time (Input EN to output $\overline{O_N}$)				10	μS
t_{PHL}	High to low-level output propagation time (Input EN to output $\overline{O_N}$)				1	μS

(Note 1) TEST CIRCUIT



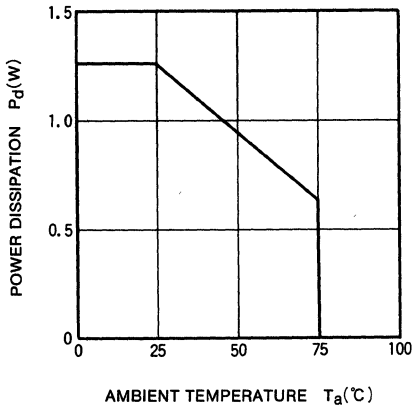
Input waveform is taken as t_r≦50ns and t_f≦50ns

TIMING DIAGRAM

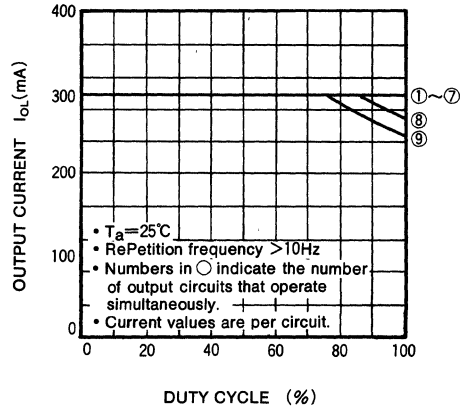


TYPICAL CHARACTERISTICS

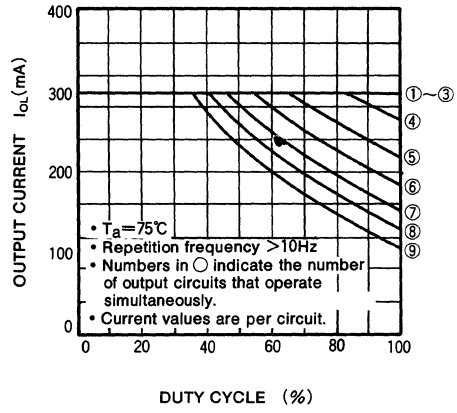
THERMAL DERATING



DUTY CYCLE VS PERMISSIBIE OUTPUT CURRENT



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT



M54972P

BI-CMOS 8-BIT SERIAL-INPUT,LATCHED DRIVER

DESCRIPTION

The M54972P is a semiconductor integrated circuit consisting of eight stages of CMOS shift registers and latches with serial inputs and serial or parallel outputs. It is based on Bi-CMOS process technology, and has eight bipolar drivers at the parallel outputs.

FEATURES

- Serial input and serial or parallel output
- Serial output enables cascade connection
- Built-in latch for each stage
- Enable input provides output control
- Low supply current (standby current $I_{CC} \leqq 10\mu A$)
- Serial I/O level is compatible with typical CMOS drvices
- Driver features : High withstand voltage ($BV_{CEO} \geqq 30V$)
  Capable of large drive currents ($I_{O\,(max)} = 300mA$)
  Low output saturation voltage $V_{OL} < 0.6V$ at $I_O = 300mA$
- Wide operating temperrature range $T_a = -20 \sim +75°C$

APPLICATION

Dot drivers for thermal print heads. Serial/parallel conversion. Drivers for relays and solenoids.

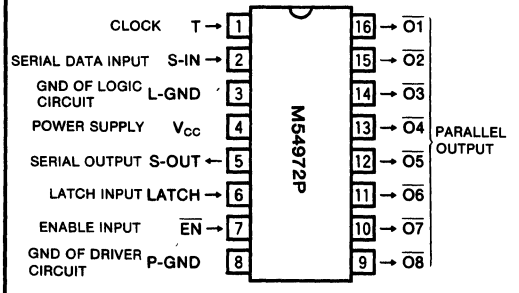
FUNCTION

The M54972P consists of eight stages of D-type flip flops connected to eight latches.

Data is input to serial input S-IN, and clock pulses are input to clock input T. When the clock changes from low to high, the input data enters the first shift register and data already in the shift registers is shifted sequentially.

The serial output S-OUT is used to connect multiple M54972Ps to expand the number of parallel outputs. S-OUT is connected to S-IN of the next stage.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

For parallel output. When the clock pulse changes from low to high, latch input (LATCH) is high and output enable input ($\overline{EN}$) is low the serial input data at S-IN appears at output $\overline{O1}$ and the other data already present is shifted sequentially to outputs $\overline{O2}$ through $\overline{O8}$.

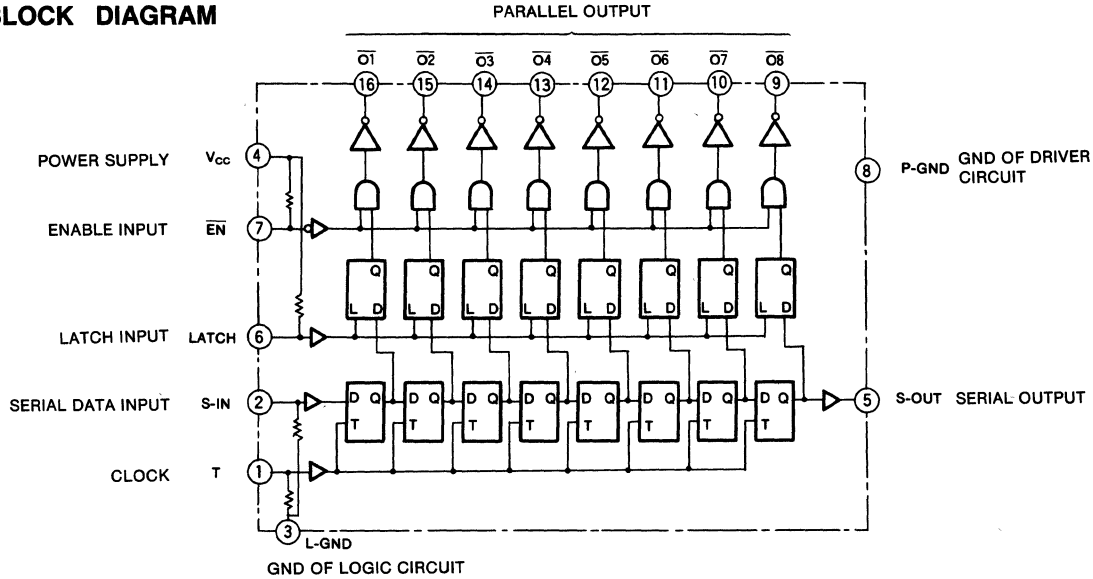
The parallel outputs are inverted.

When the latch input is held low, the latch retains the stored data.

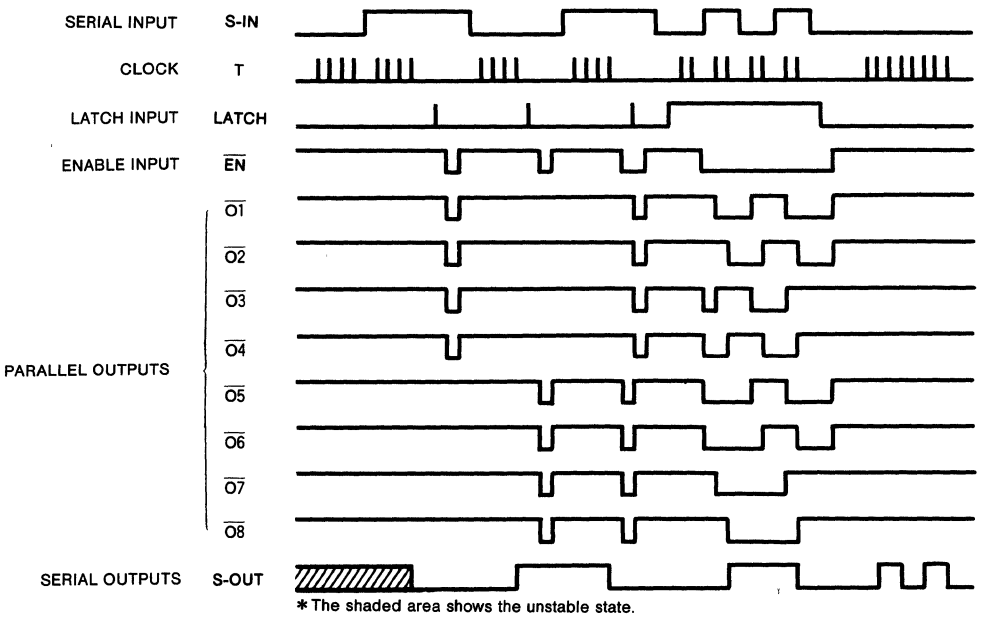
When the EN input is high, outputs $\overline{O1}$ through $\overline{O8}$ all turn off. As the internal logic is unstable when the power is turned on, the $\overline{EN}$ input should be kept high (setting outputs $\overline{O1}$ through $\overline{O8}$ off) until input data is set and the internal logic is initialized.

L-GND is the GND of CMOS logic circuit and P-GND is the GND of output driver circuits $\overline{O1}$ through $\overline{O8}$ which employ bipolar transistors capable of large drive currents.

BLOCK DIAGRAM

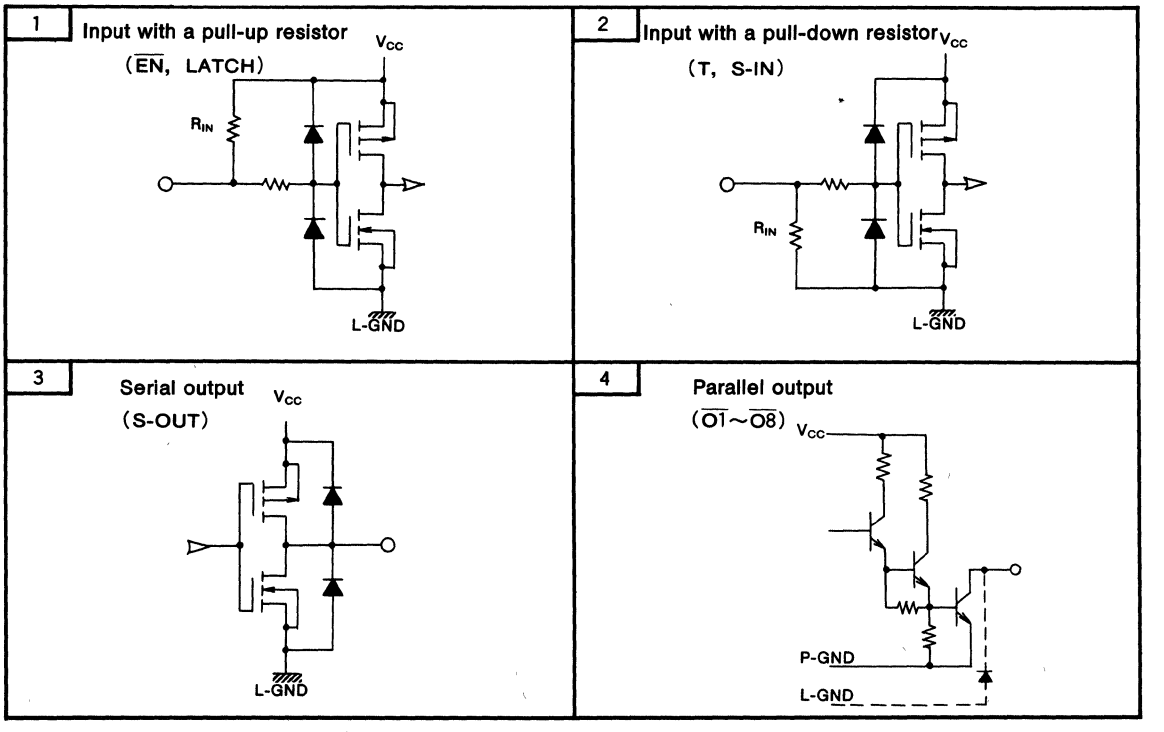


TIMING CHART



* The shaded area shows the unstable state.

I/O CIRCUIT



MITSUBISHI ELECTRIC

M54972P

BI-CMOS 8-BIT SERIAL-INPUT,LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+8	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage	S-OUT	−0.5∼V_{CC}+0.5	V
		$\overline{O1}$∼$\overline{O8}$ Transistor off	−0.5∼+30	
I_O	Output current	$\overline{O1}$∼$\overline{O8}$ Transistor on	300	mA
P_d	Power dissipation	T_a=25℃	1.25	W
Topr	Operating temperrature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
V_O	Applied output voltage	$\overline{O1}$∼$\overline{O8}$ Transistor off			30	V
I_O	Output current per circuit	$\overline{O1}$∼$\overline{O8}$ All outputs on Duty cycle 70% max			200	mA
		$\overline{O1}$∼$\overline{O8}$ All outputs on Duty cycle 35% max			300	mA

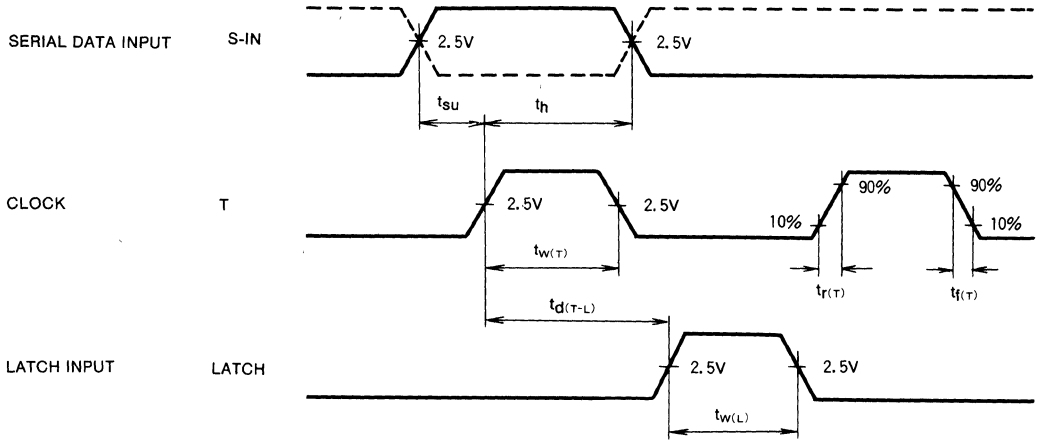
ELECTRICAL CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage		T_a=−20∼+75℃	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
I_{IH}	High-level input current		V_{IH}=5V			100	μA
I_{IL}	Low-level input current		V_{IL}=0V			−100	μA
R_{IN}	Input resistance			50			kΩ
V_{OH}	High-level output voltage	S-OUT output	| I_O | ≦ 1 μA	4.9			V
V_{OL}	Low-level output voltage	S-OUT output				0.1	V
I_{OH}	High-level output current	S-OUT output	V_{OH}=4.5V	−100			μA
I_{OL}	Low-level output current	S-OUT output	V_{OL}=0.4V	400			μA
V_{OL1}	Low-level output voltage	Parallel output	I_{OL}=100mA			0.4	V
V_{OL2}			I_{OL}=200mA			0.5	V
V_{OL3}			I_{OL}=300mA			0.6	V
I_{OLK}	Output leakage current	Parallel output	V_O=30V			50	μA
I_{CC1}	Supply current		Input release all driver output off			10	μA
I_{CC2}			One driver output circuit on			7.5	mA

TIMING REQUIREMENTS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$f_{(T)}$	Clock frequency	Input duty cycle 40∼60%			2	MHz
$t_{W(T)}$	Clock pulse width		200			ns
$t_{W(L)}$	Latch pulse width		200			ns
t_{su}	Data setup tune		100			ns
t_h	Data hold time		100			ns
$t_{d(T-L)}$	Clock-latch time		400			ns
$t_{r(T)}$	Rising edge of clock pulse				500	ns
$t_{f(T)}$	Falling edge of clock pulse				500	ns

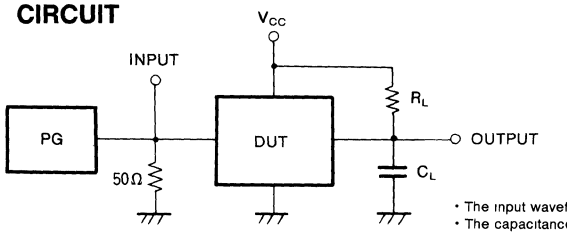
TIMING DIAGRAM



SWITCHING CHARACTERISTICS (T_a=25℃, V_{CC}=5V, unless otherwise noted)

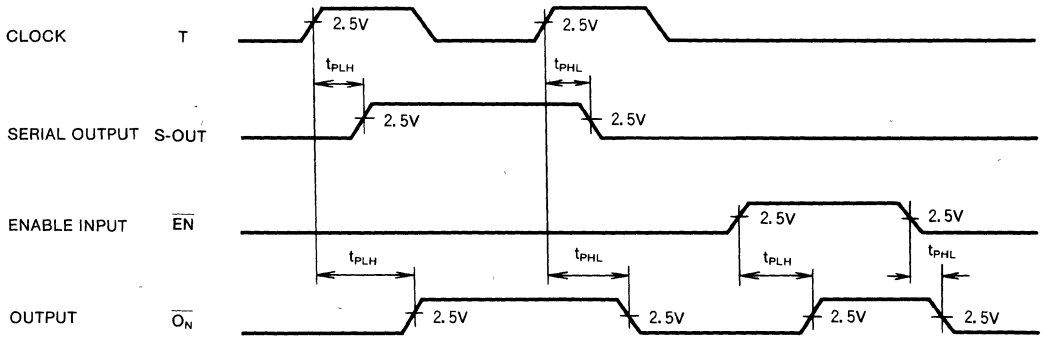
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time From input T to output S-OUT	V_{IH} = 5 V V_{IL} = 0 V $R_{L(S\text{-}OUT)}$ = ∞ $R_L(\overline{O_N})$ = 100Ω (N = 1 ~ 8) C_L = 15pF			0.3	μs
t_{PHL}	High-to-low-level output propagation time From input T to output S-OUT				0.3	μs
t_{PLH}	Low-to-high-level output propagation time From input T to output $\overline{O_N}$				10	μs
t_{PHL}	High-to-low-level output propagation time From input T to output $\overline{O_N}$				5	μs
t_{PLH}	Low-to-high-level output propagation time From input $\overline{EN}$ to output $\overline{O_N}$				10	μs
t_{PHL}	High-to-low-level output propagation time From input $\overline{EN}$ to output $\overline{O_N}$				5	μs

TEST CIRCUIT



- The input waveform has the characteristics of $t_r \leqq 20ns$ $t_f \leqq 20ns$
- The capacitance C_L includes stray wiring capacitance and probe input capacitance

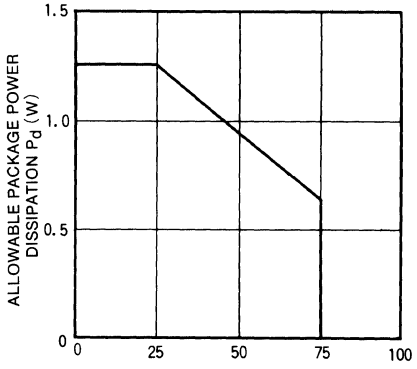
TIMING DIAGRAM



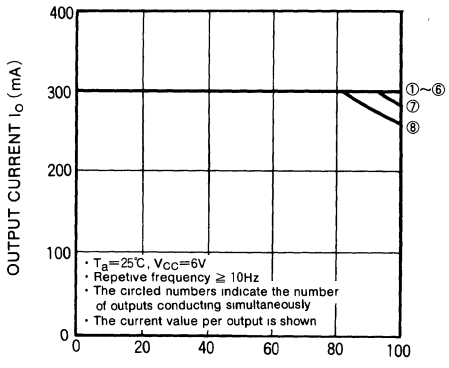
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS

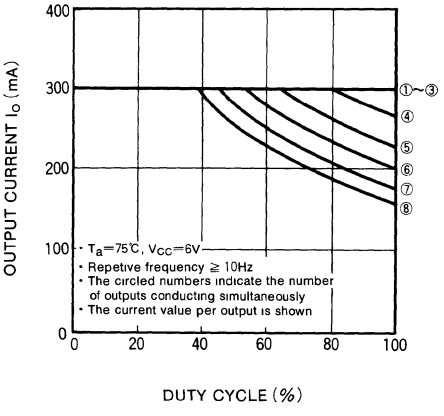
ALLOWABLE AVERAGE POWER DISSIPATION



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



M54973P

BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

DESCRIPTION

The M54973P is a semiconductor integrated circuit consisting of eight CMOS latches and bipolar output drivers product by a Bi-CMOS process.

FEATURES

- Enable input provides output control
- Low supply current (standby current $I_{CC} \leqq 10\mu A$)
- Input level is compatible with typical CMOS
- Driver features : High withstand voltage ($BV_{CEO} \geqq 30V$)
  Capable of large drive currents ($I_{O(max)} = 300mA$)
- Wide operating temperrature range $T_a = -20 \sim +75℃$

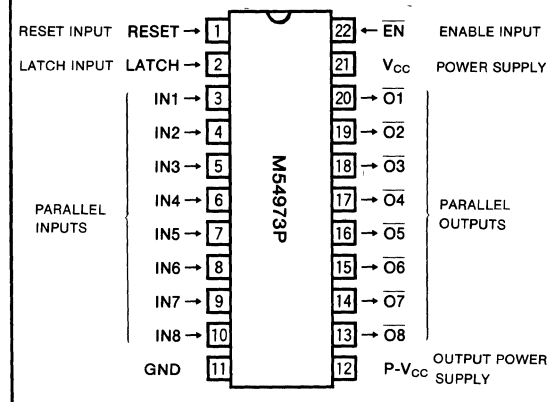
APPLICATION

Dot driver for thermal print heads. Drivers for relays, and solenoids.

FUNCTION

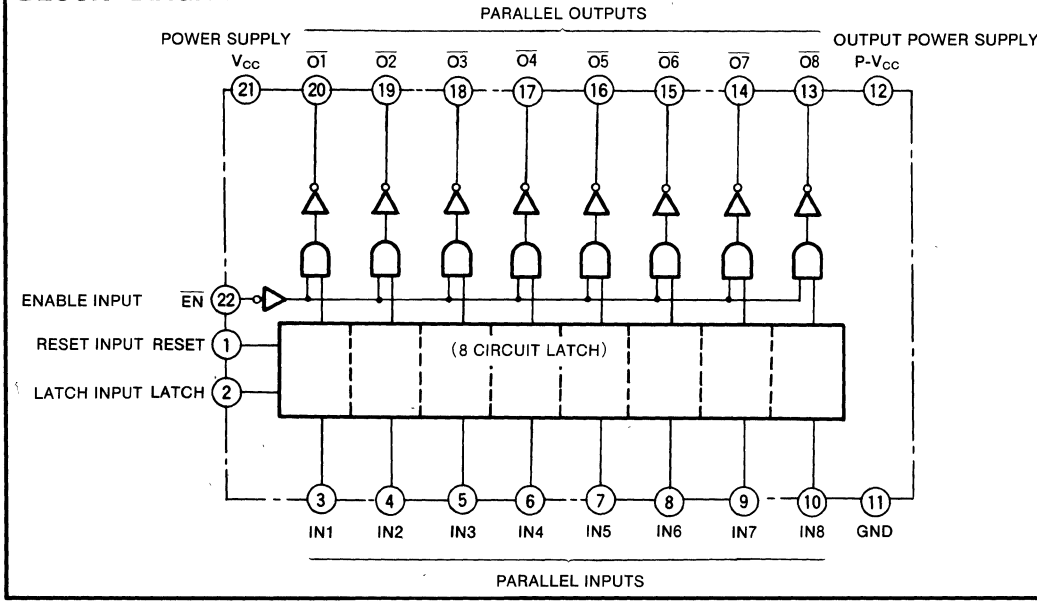
Data are applied to inputs IN1 through IN8. When the LATCH input is set high, the data is latched as shown in the truth table. A high-level signal applied to the RESET input causes the latches to remain open (reset). When the EN input is set low, high data stored in the latches turn on the corresponding outputs and set them low.
When the LATCH and RESET inputs are both low, the latch retains the stored data, irrespective of inputs IN1 through IN8.

PIN CONFIGURATION (TOP VIEW)



Outline 22P4

BLOCK DIAGRAM



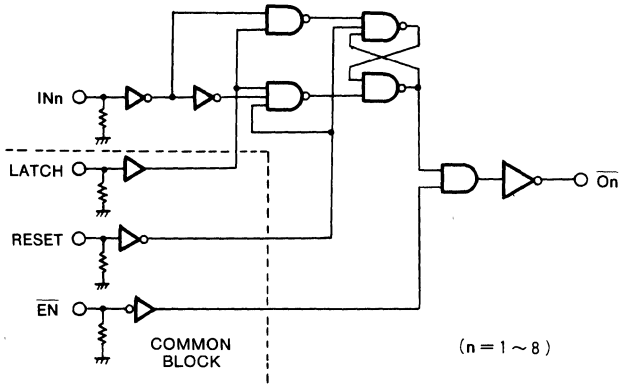
BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

TRUTH TABLE

Inputs				Outputs $\overline{On}$	
INn	LATCH	RESET	$\overline{EN}$	t-1	t
L	H	L	L	X	H
H	H	L	L	X	L
X	X	H	X	X	H
X	X	X	H	X	H
X	L	L	L	L	L
X	L	L	L	H	H

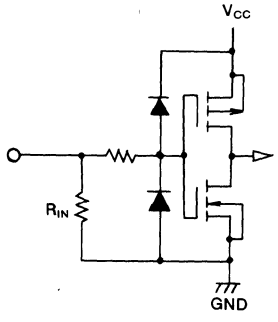
L = low level
H = high level
X = Irrelevant
t-1 = previous state
t = current state
Off state when output is high
On state when output is low

LOGIC DIAGRAM (ONE CIRCUIT)

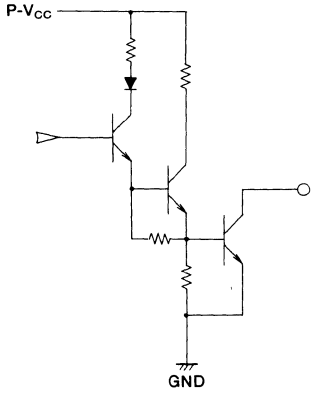


I/O EQUIVALENT CIRCUIT

1 Input circuit (INn, LATCH, RESET, $\overline{EN}$)



2 Output circuit (parallel output On)



BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS (T_a=20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+8	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage	Transistor off	−0.5～+30	V
I_O	Output current	Transistor on	200	mA
P_d	Power dissipation	T_a=25℃	1.42	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
P-V_{CC}	Output spply voltage		4.5	5	7	V
V_O	Applied output voltage	Transistor off			30	V
I_O	Output current per circuit	All outputs on simultaneously Duty cycle 80% max			120	mA

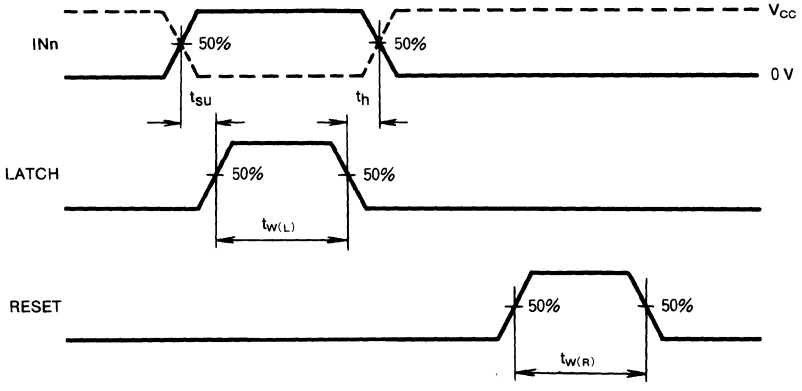
ELECTRICAL CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, P-V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage	T_a=−20～+75℃	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.3V_{CC}	V
R_{IN}	Input resistance		50			kΩ
V_{OL1}	Low-level output voltage	I_{OL}=120mA			0.4	V
V_{OL2}		I_{OL}=200mA			0.5	V
I_{OLK}	Output leakage current	V_O=30V			50	μA
I_{CC1}	Supply current	All inputs=0V, all outputs off			10	μA
I_{CC2}		One output circuit on			0.2	mA
I_{CC3}	Output supply current	All inputs open, all outputs off			10	μA
I_{CC4}		One output circuit on			14	mA

TIMING REQUIREMENTS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(L)}$	Latch pulse width		0.1			μs
$t_{w(R)}$	Reset pulse width		0.1			μs
t_{su}	Data setup time		0			μs
t_h	Data hold time		0.1			μs

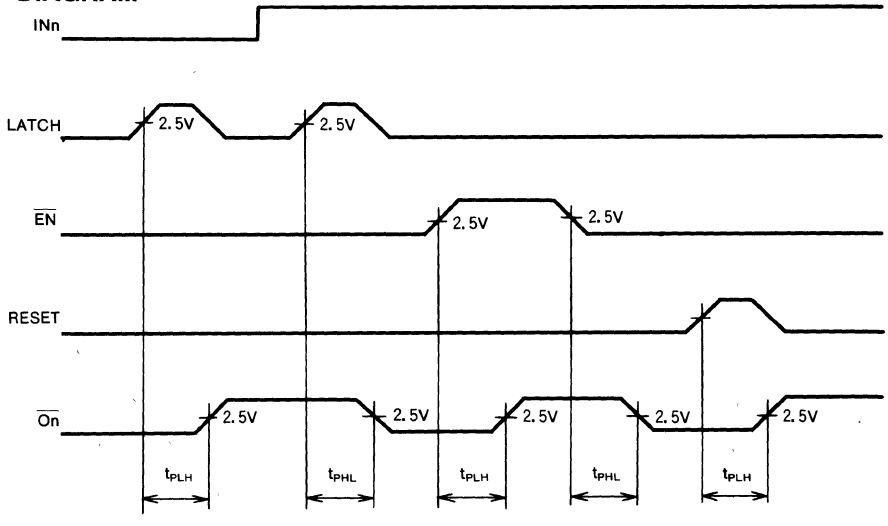
TIMING DIAGRAM



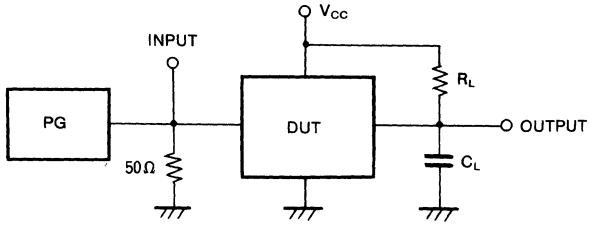
SWITCHING CHARACTERISTICS (T_a=+25℃, V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to high-level output propagation time (Input LATCH to output $\overline{On}$)	V_{IH} = 5 V, V_{IL} = 0 V, R_L = 100Ω, C_L = 15pF (Note 1)		(0.6)	2	μs
t_{PHL}	High-to low-level output propagation time (Input LATCH to output $\overline{On}$)			(0.1)	0.5	μs
t_{PLH}	Low-to high-level output propagation time (Input $\overline{EN}$ to output $\overline{On}$)			(0.6)	2	μs
t_{PHL}	High-to low-level output propagation time (Input $\overline{EN}$ to output $\overline{On}$)			(0.1)	0.5	μs
t_{PLH}	Low-to high-level output propagation time (Input RESET to output $\overline{On}$)			(0.6)	2	μs

TIMING DIAGRAM



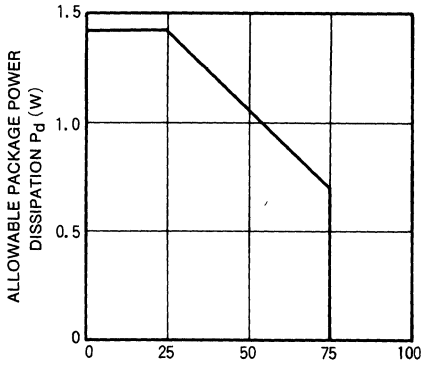
TEST CIRCUIT



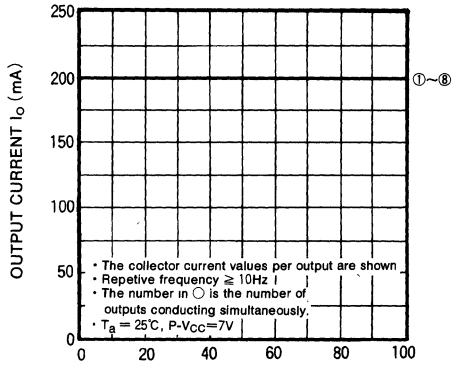
- The input waveform has the characteristics of $t_r \leqq 20ns$ and $t_f \leqq 20ns$
- The capacitance C_L includes stray wiring capacitance and probe input capacitance.

TYPICAL CHARACTERISTICS

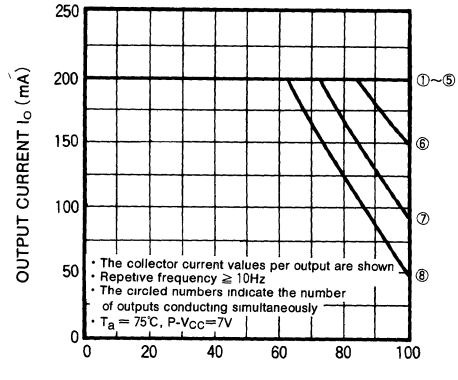
ALLOWABLE AVERAGE POWER DISSIPATION



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



M54974P

BI-CMOS 12-BIT SERIAL-INPUT,LATCHED DRIVER

DESCRIPTION

The M54974P is a semiconductor integrated circuit consisting of twelve stages of CMOS shift registers and latches with serial inputs and serial or parallel outputs. It is based on Bi-CMOS process technology, and has twelve bipolar drivers at the parallel outputs.

FEATURES

- Serial input and serial or parallel output
- Serial output enables cascade connection
- Built-in latch for each stage
- Enable input provides output control
- Low supply current (standby current $I_{CC} \leqq 10\mu A$)
- Serial I/O level is compatible with typical CMOS devices
- Driver features : High withstand voltage ($BV_{CEO} \geqq 30V$)
  Capable of large drive currents ($I_{O\,(max)} = 300mA$)
- Wide operating temperrature range $T_a = -20 \sim +75℃$

APPLICATION

Dot drivers for thermal print heads. Serial/parallel conversion. Drivers for relay and solenoids.

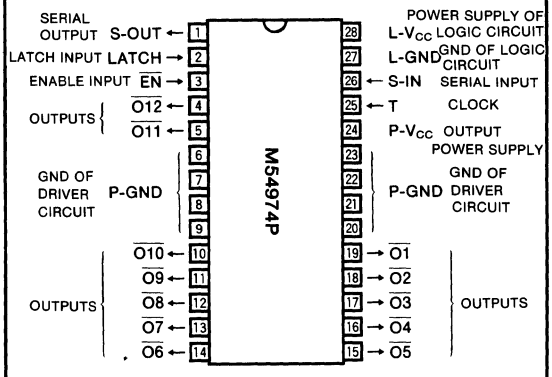
FUNCTION

The M54974P consists of twelve stages of D-type flip flops connected to twelve latches.

Data is input to serial input S-IN, and clock pulses are applied to clock input T. When the clock changes from low to high, the input data enters the first shift register and data already in the shift registers is shifted sequentially.

The serial output S-OUT is used to connect multiple M54974Ps to expand the number of parallel outputs. S-OUT is connected to S-IN of the next stage.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4B-A

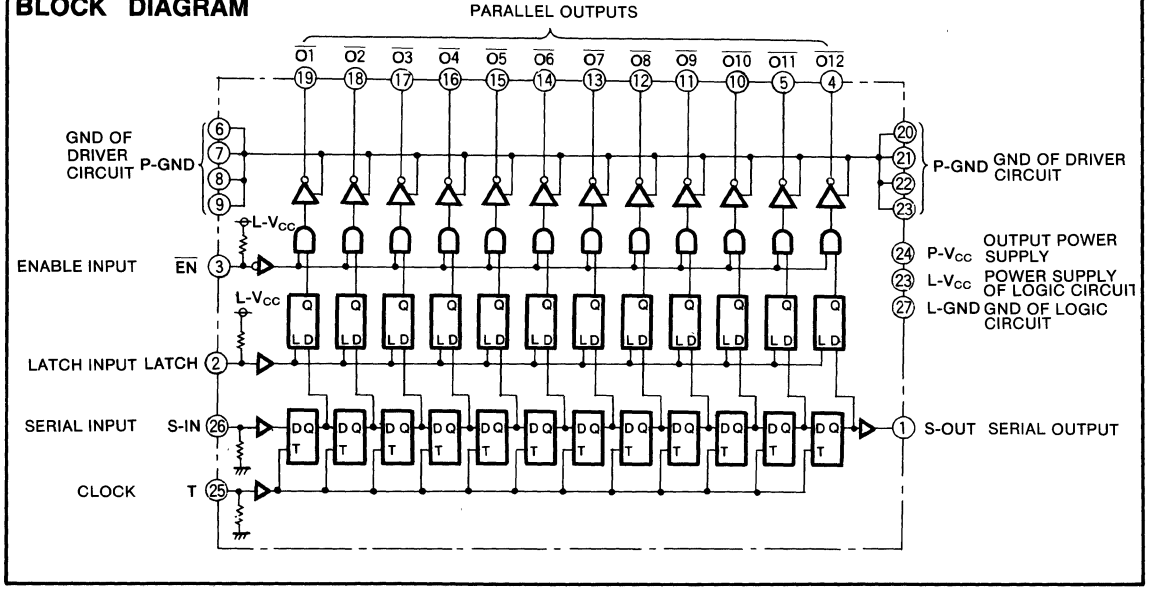
When the clock pulse changes from low to high, latch input (LATCH) is high and output enable input ($\overline{EN}$) is low the serial input data at S-IN appears at output $\overline{O1}$ and the other data already present is shifted sequentially to outputs $\overline{O2}$ through $\overline{O12}$.

The parallel outputs are inverted.

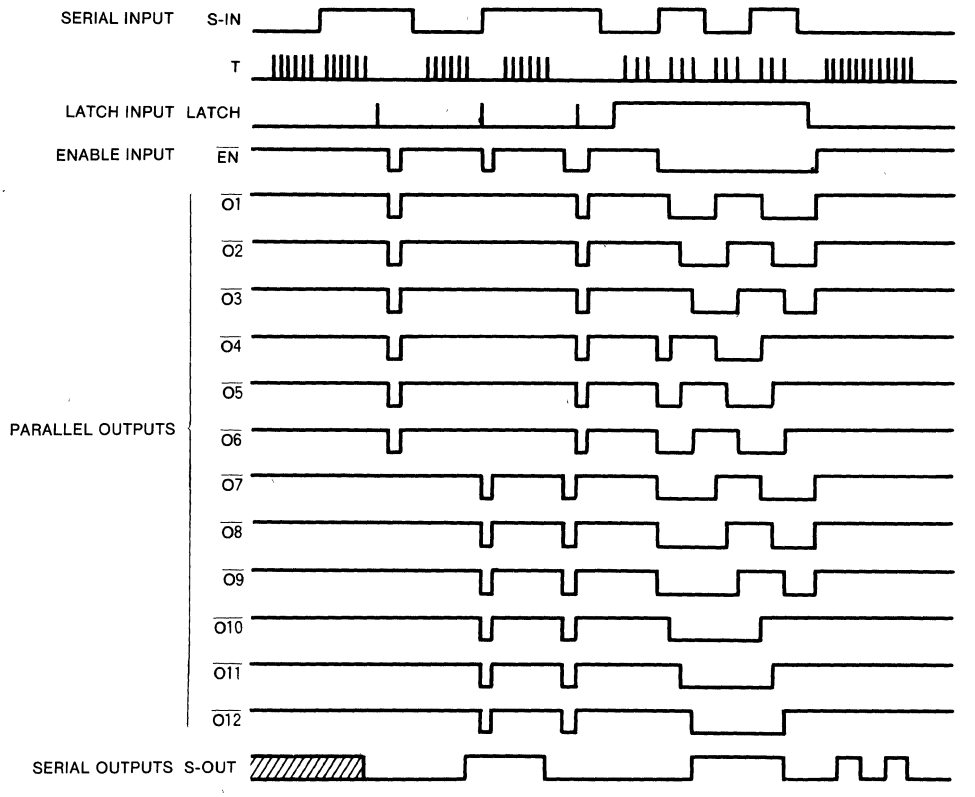
When the latch input is held low, the latch retains the stored data. When the $\overline{EN}$ input is high, outputs $\overline{O1}$ through $\overline{O12}$ all turn off. As the internal logic is unstable when the power is turned on, the $\overline{EN}$ input should be kept high (setting the outputs $\overline{O1}$ through $\overline{O12}$ off) until input data is set and the internal logic is initialized.

L-GND is the GND of CMOS logic circuit and P-GND is the GND of output driver circuits $\overline{O1}$ through $\overline{O12}$ which employ bipolar transistors capable of large drive currents.

BLOCK DIAGRAM



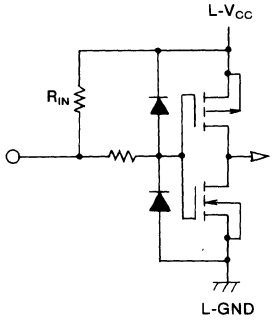
TIMING CHART



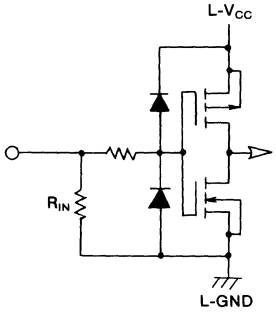
* The shaded area shows the unstable state

I/O CIRCUIT

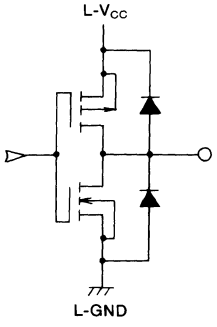
1 Input with a pull-up resistor
($\overline{EN}$, LATCH)



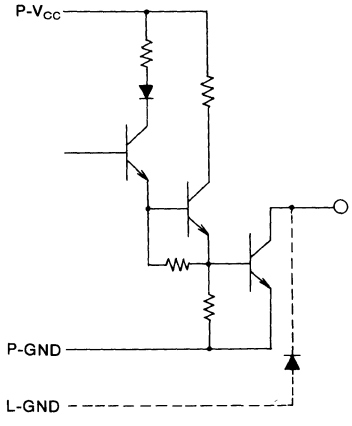
2 Input with a pull-down resistor
(T, S-IN)



3 Serial output
(S-OUT)



4 Parallel output
($\overline{O1}$~$\overline{O12}$)



BI-CMOS 12-BIT SERIAL-INPUT,LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS (T_a=20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～8	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage	S-OUT	−0.5～V_{CC}+0.5	V
		$\overline{O1}$～$\overline{O12}$ Transistor off	−0.5～30	V
I_O	Output current		400	mA
P_d	Power dissipation	T_a =25℃	2.5	W
Topr	Operating temperature		−20～+75	℃
Tstg	Storage temperature		−55～+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
P-V_{CC}	Output supply voltage		4.5	5	6	V
V_O	Applied output voltage	$\overline{O1}$～$\overline{O12}$ Transistor off			30	V
I_O	Output current per circuit	All outputs on Duty cycle 50% max			300	mA

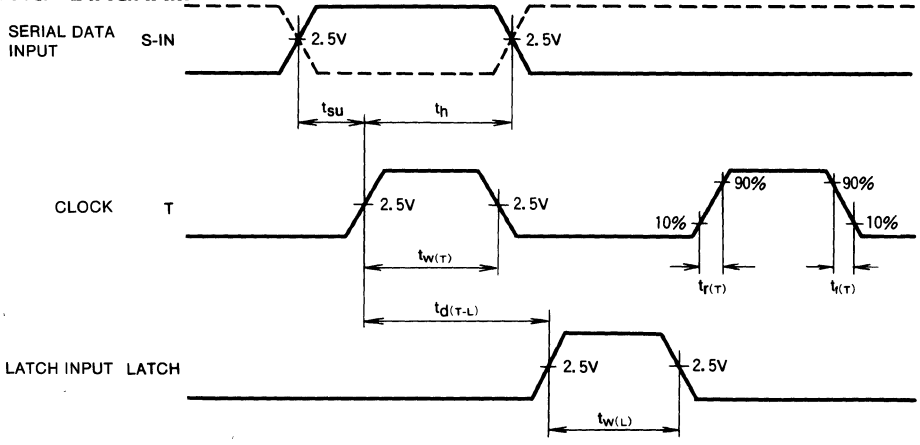
ELECTRICAL CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, P-V_{CC}=5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage		T_a =−20～+75℃	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
R_{IN}	Input resistance			50			kΩ
V_{OH}	High-level output voltage	S-OUT output	$\lvert I_O \rvert \leq 1\ \mu A$	4.9			V
V_{OL}	Low-level output voltage	S-OUT output				0.1	V
I_{OH}	High-level output current	S-OUT output	V_{OH} =4.5V	−100			μA
I_{OL}	Low-level output current	S-OUT output	V_{OL} =0.4V	400			μA
V_{OL1}	Low-level output voltage	Parallel output	I_{OL} =120mA			0.4	V
V_{OL2}			I_{OL} =300mA			0.5	V
V_{OL3}			I_{OL} =400mA			0.7	V
I_{OLK}	Output leakage current	Parallel output	V_O =30V			50	μA
I_{CC1}	Supply current (L-V_{CC})		Input release all driver output off			10	μA
I_{CC2}			One driver output circuit on			0.2	mA
I_{CC3}	Output supply current (P-V_{CC})		One driver output circuit on			14	mA

TIMING REQUIREMENTS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$f_{(T)}$	Clock frequency	Input duty cycle 40~60%			2	MHz
$t_{w(T)}$	Clock pulse width		200			ns
$t_{w(L)}$	Latch pulse width		200			ns
t_{su}	Data setup time		100			ns
t_h	Data hold time		100			ns
$t_{d(T-L)}$	Clock-latch time		400			ns
$t_{r(T)}$	Rising edge of clock pulse				500	ns
$t_{f(T)}$	Falling edge of clock pulse				500	ns

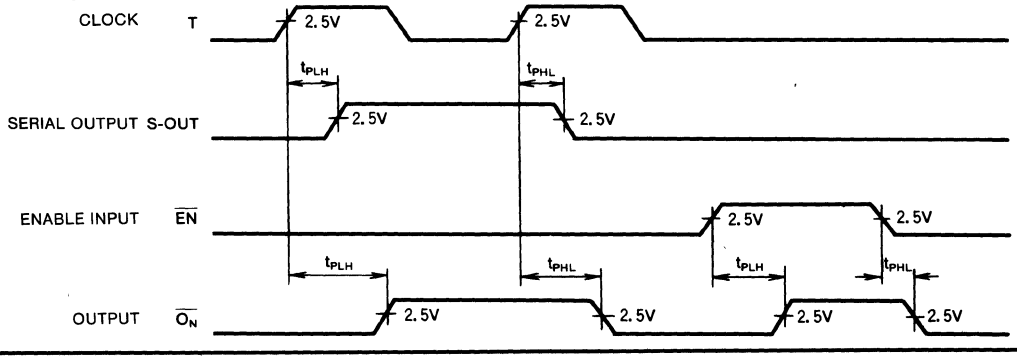
TIMING DIAGRAM



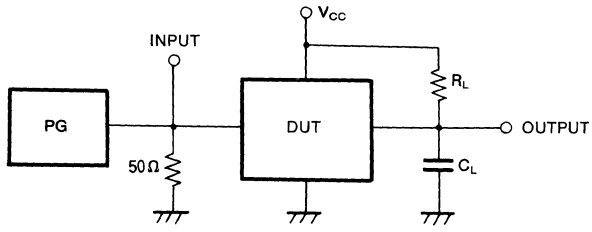
SWITCHING CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time From input T to output S-OUT	V_{IH}=5 V V_{IL}=0 V R_L(S-OUT)=∞ R_L($\overline{O_N}$)=100Ω (N=1~12) C_L=15pF		(0.15)	0.3	μs
t_{PHL}	High-to-low-level output propagation time From input T to output S-OUT			(0.15)	0.3	μs
t_{PLH}	Low-to-high-level output propagation time From input T to output $\overline{O_N}$			(2)	10	μs
t_{PHL}	High-to-low-level output propagation time From input T to output $\overline{O_N}$			(1)	5	μs
t_{PLH}	Low-to-high-level output propagation time From input $\overline{EN}$ to output $\overline{O_N}$			(2)	10	μs
t_{PHL}	High-to-low-level output propagation time From input $\overline{EN}$ to output $\overline{O_N}$			(1)	5	μs

TIMING DIAGRAM



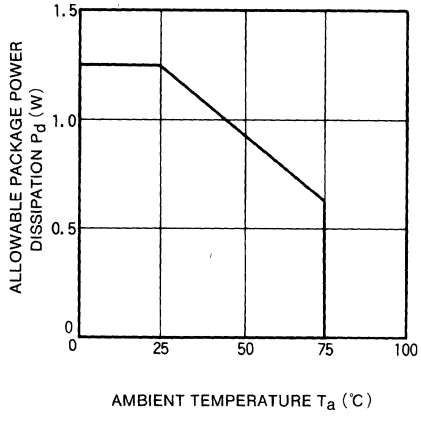
TEST CIRCUIT



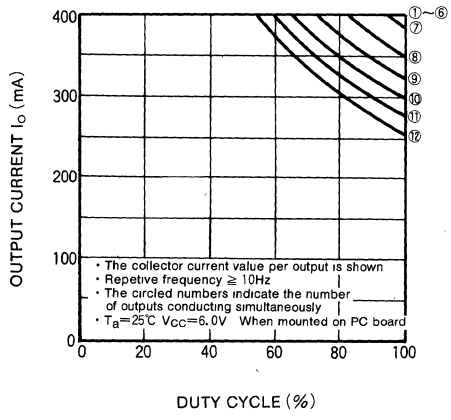
- The input waveform has the characteristics of $t_r \leqq 20ns$ $t_f \leqq 20ns$
- The capacitance C_L includes stray wiring capacitance and probe input capacitance

TYPICAL CHARACTERISTICS

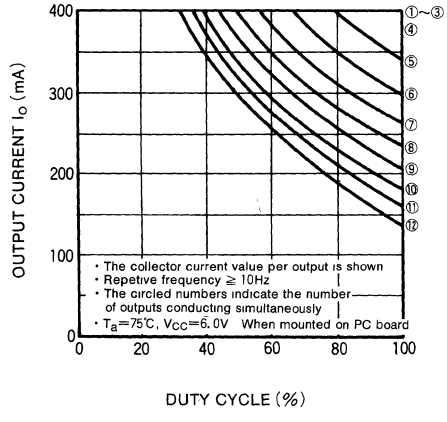
ALLOWABLE AVERAGE POWER DISSIPATION



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



MITSUBISHI ELECTRIC

M54975P

BI-CMOS 8-BIT SERIAL-INPUT,LATCHED DRIVER

DESCRIPTION

The M54975P is a semiconductor integrated circuit fabricated using Bi-CMOS technology. It contains a serial input to serial/parallel output 8-bit CMOS shift register and CMOS latch as well as bipolar 8-bit parallel-output driver.

FEATURES

- Serial input to serial/parallel output
- Cascade connections possible through serial output
- Latch circuit included for each stage
- Enable input for output control
- Low supply current ····· $I_{CC} \geqq 10\mu A$ at standby
- Serial input/output level is compatible with standard CMOS
- Driver : Withstand voltage ····· $BV_{CEO} \geqq 30$
  Large drive current ····· ($I_{O(max)}$=300mA)
- Wide operating temperature range···· T_a=−20∼+75℃

APPLICATION

Thermal printer head dot driver, Serial-to parallel conversion, Relay and Solenoid driver

FUNCTION

The M54975P consists of an 8-bit D-type flip-flop, the output of which is connected to 8 latches.

When data is applied to the serial data input (S-IN) and a clock pulse is applied to clock input (T), an "L" to "H" change of the clock will cause the data input signals to enter the internal shift registers and the data in the shift registers will be shifted in order.

Using a number of M54975P units for bit expansion in series will entail connecting serial output (S-OUT) to S-IN of the next-stage M54975P.

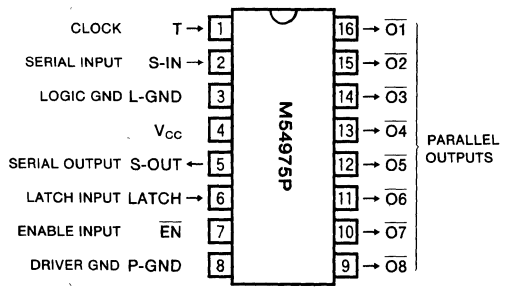
In parallel output, when the latch input is set to "H" and the output-control input (enable input $\overline{EN}$) is "L", a clock pulse changing from "L" to "H" will cause the serial data input signal to appear at output $\overline{O1}$, and the data will be shifted in order at outputs $\overline{O2}$∼$\overline{O8}$.

The parallel output will yield a signal that is inverted with respect to the serial data input.

Setting the LATCH input to "L" will prevent data from entering the latch.

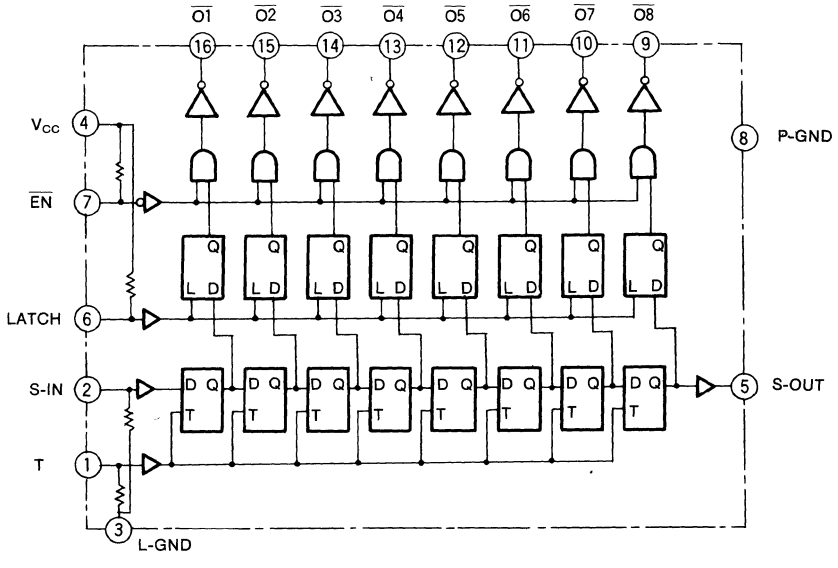
When the $\overline{EN}$ input is set to "H", all outputs ($\overline{O1}$∼$\overline{O8}$) will be set to OFF. Since the internal logic state of the IC is uncertain at power-on time, set the $\overline{EN}$ input to "H" (and outputs $\overline{O1}$∼$\overline{O8}$ will set to OFF) until the input data is set and

PIN CONFIGURATION (TOP VIEW)



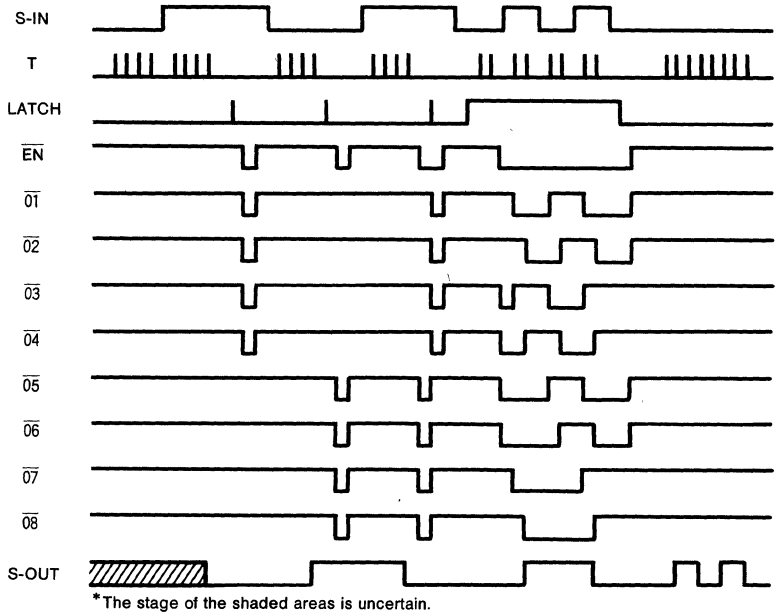
Outline 16P4

BLOCK DIAGRAM



the internal logic state has been determined.
L-GND is the ground of the CMOS logic circuit section and P-GND is the ground for the output driver section ($\overline{O1}$ ~ $\overline{O8}$), which is made up of bipolar transistors that are capable of driving large currents.

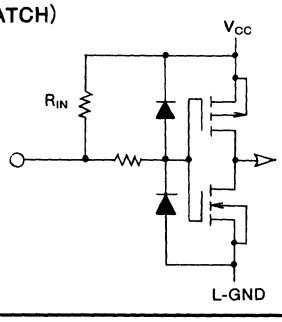
TIMING CHART



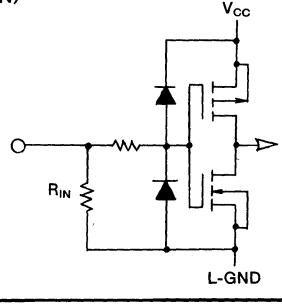
*The stage of the shaded areas is uncertain.

INPUT/OUTPUT CIRCUIT SCHEMATICS

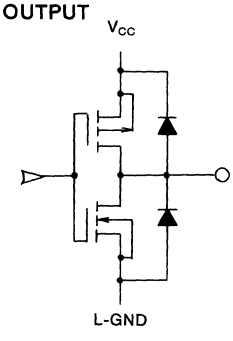
1 INPUT WITH PULL-UP RESISTOR ($\overline{EN}$, LATCH)



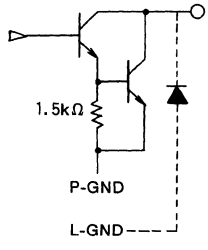
2 INPUT WITH PULL-DOWN RESISTOR (T, S-IN)



3 SERIAL OUTPUT (S-OUT)



4 PARALLEL OUTPUT ($\overline{O1}$~$\overline{O8}$)



MITSUBISHI ELECTRIC

BI-CMOS 8-BIT SERIAL-INPUT,LATCHED DRIVER

ABSOLUTE MAXIMUM RATING (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+8	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage	S-OUT	−0.5∼V_{CC}+0.5	V
		$\overline{O1}$∼$\overline{O8}$: Output is OFF	−0.5∼+30	
I_O	Output Current	$\overline{O1}$∼$\overline{O8}$: Output is ON	350	mA
P_d	Power dissipation	T_a=25℃	1.25	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃ unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
V_O	Applied output voltage	$\overline{O1}$∼$\overline{O8}$: When output is OFF			30	V
I_O	Output current (per circuit)	$\overline{O1}$∼$\overline{O8}$: All outputs ON simultaneously Duty cycle less than 15%			300	mA

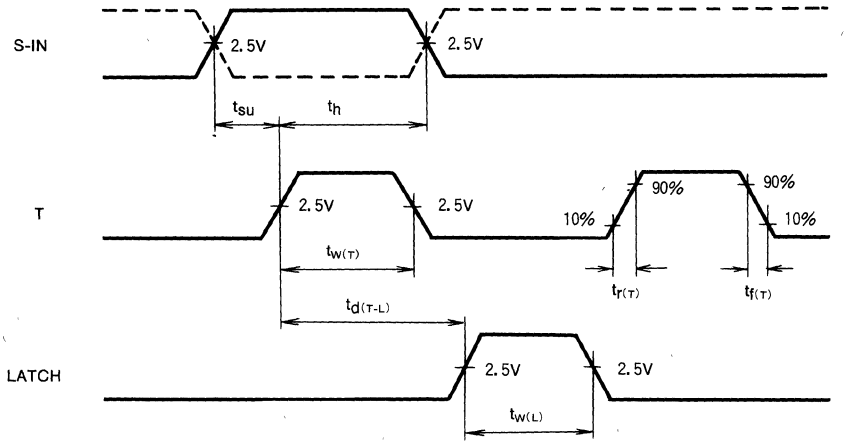
ELECTRICAL CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	1, 2 6, 7	T_a=−20∼+75℃	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
R_{IN}	input resistance			50		—	kΩ
V_{OH}	High-level output voltage	5	| I_O | ≦1μA	4.9		—	V
V_{OL}	Low-level output voltage			—		0.1	V
I_{OH}	High-level output current		V_{OH}=4.5V	−100		—	μA
I_{OL}	Low-level output current		V_{OL}=0.4V	400		—	μA
V_{OL1}	Low-level output voltage	9∼16	I_{OL}=100mA	—		1.2	V
V_{OL2}			I_{OL}=200mA	—		1.4	V
V_{OL3}			I_{OL}=300mA	—		1.6	V
I_{OLK}	Output leakage current		V_O=30V	—		50	μA
I_{CC1}	Supply current	4	Inputs free, all driver outputs OFF	—		10	μA
I_{CC2}			Driver output : 1 circuit ON	—		1.7	mA

REQUIRED TIMING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$f_{(T)}$	Clock frequency	Input duty cycle 40∼60%			2	MHz
$t_{W(T)}$	Clock pulse width		200			nS
$t_{W(L)}$	Latch pulse width		200			nS
t_{su}	Data setup time		100			nS
t_h	Data hola time		100			nS
$t_{d(T-L)}$	Clock-latch time		400			nS
$t_{r(T)}$	Clock pulse rise time				500	nS
$t_{f(T)}$	Clock pulse fall time				500	nS

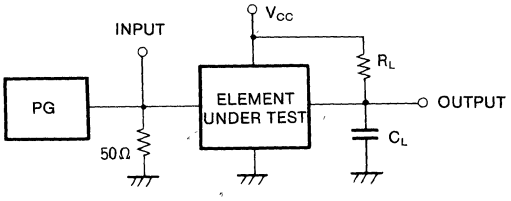
TIMING DIAGRAM



SWITCHING CHARACTERISTICS (T_a=+25℃, V_{CC}=5V)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low to high-level output propagation time (Input T to output S-OUT)	V_{IH}=5V V_{IL}=0V R_L : S-OUT=∞ R_L : $\overline{O_N}$=100Ω (N=1~8) C_L=15pF (Note 1)			0.3	μS
t_{PHL}	High to low-level output propagation time (Input T to output S-OUT)				0.3	μS
t_{PLH}	Low to high-level output propagation time (Input T to output $\overline{O_N}$)				10	μS
t_{PHL}	High to low-level output propagation time (Input T to output $\overline{O_N}$)				2	μS
t_{PLH}	Low to high-level output propagation time (Input EN to output $\overline{O_N}$)				10	μS
t_{PHL}	High to low-level output propagation time (Input EN to output $\overline{O_N}$)				2	μS

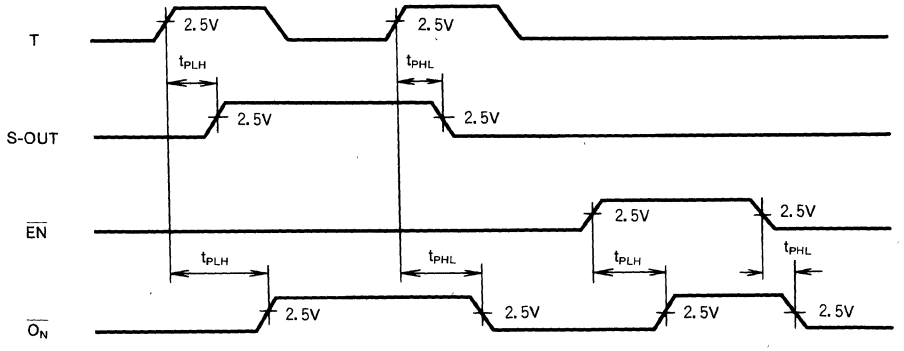
(Note 1) TEST CIRCUIT



Input waveform is taken as $t_r \leqq 20ns$ and $t_f \leqq 20ns$

C_L includes wiring stray capacitance and probe input capacitance.

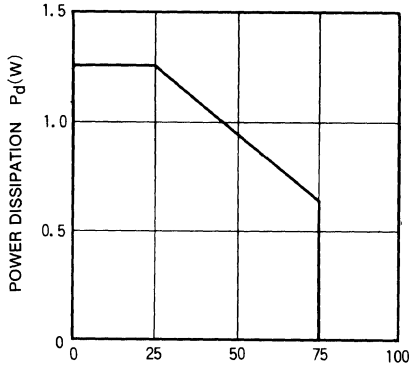
TIMING DIAGRAM



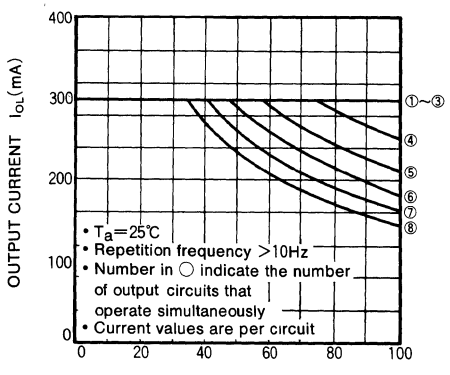
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS

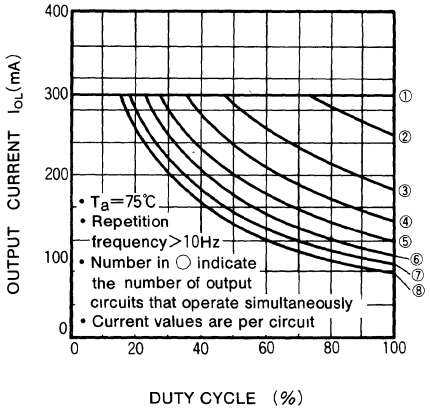
THERAL DREATING



DUTY CYCLE VS
PERMISSIBLE OUTPUT CURRENT



DUTY CYCLE VS
PERMISSIBLE OUTPUT CURRENT



M54976P

BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

DESCRIPTON

The M54976P is a semiconducnductor integrated circuit fabricated using Bi-CMOS technology. It contains bipolar 8 output drivers of CMOS latch.

FEATURES

- Enable input for output control
- Low supply current ····· $I_{CC} \leqq 10\mu A$ at standby
- Input level is compatible with standard CMOS
- Driver : Withstand voltage ····· $BV_{CEO} \geqq 30$
  Large drive current ····· ($I_{O(max)}$=300mA)
- Wide operating temperature range···· T_a=−20∼+75℃

APPLICATION

Thermal printer head dot driver, Relay driver, Solenoid driver

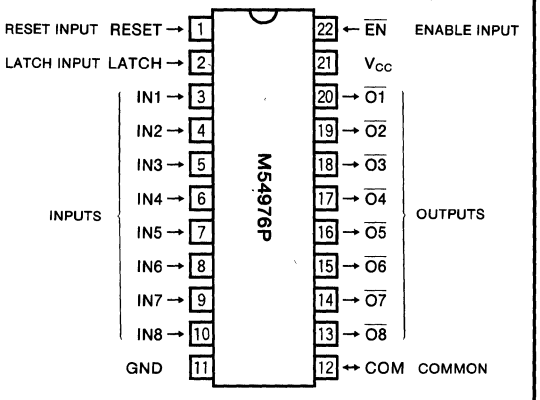
FUNCTION

When data is applied to inputs IN1-IN8 and LATCH input is set to "H", the data will be latchedance with the truth table. Note that when an "H" signal is applied to the RESET input, the latch will maintain the reset state.

When the $\overline{EN}$ input is set to "L" and the data maintained in the latch are "H", the corresponding output will be ON and become "L".

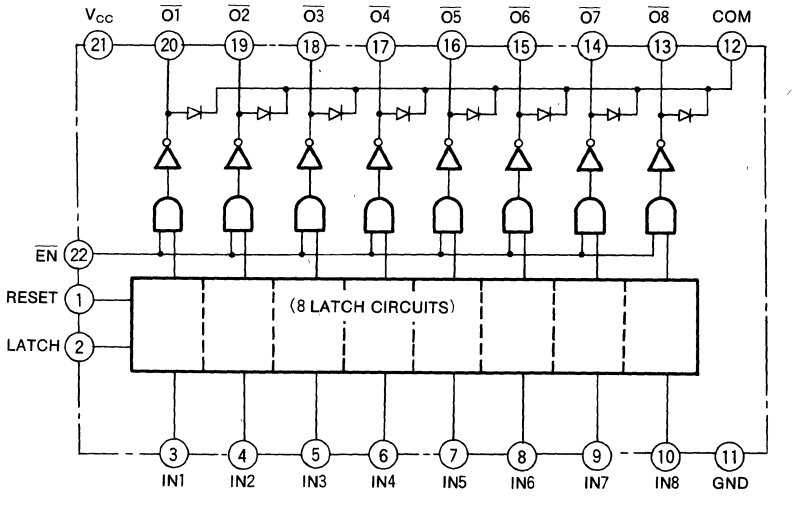
When both the LATCH and RESET inputs are "L", the latch will maintain the prior state irrespective of input signals IN1-IN8.

PIN CONFIGURATION (TOP VIEW)



Outline 22P4

BLOCK DIAGRAM



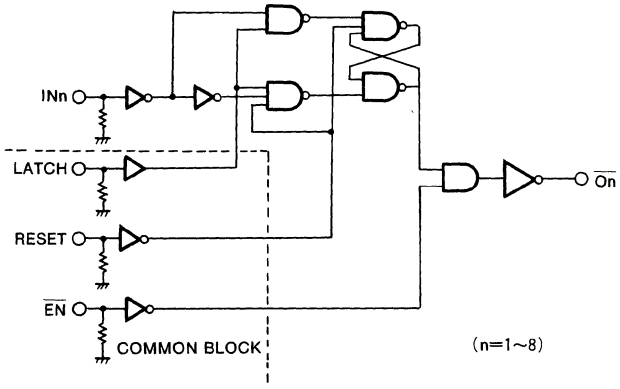
MITSUBISHI ELECTRIC

TRUTH TABLE

INPUTS				OUTPUT $\overline{On}$	
INn	LATCH	RESET	$\overline{EN}$	t-1	t
L	H	L	L	X	H
H	H	L	L	X	L
X	X	H	X	X	H
X	X	X	H	X	H
X	L	L	L	L	L
X	L	L	L	H	H

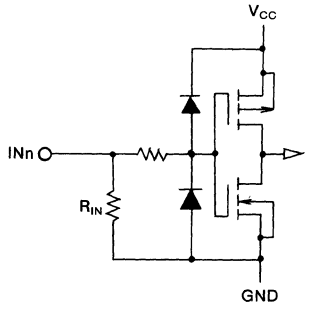
L : "L" level
H : "H" level
X : Irrelevant
t-1 : Previous state
t : Present state
Output H is in the OFF state
Output L is in the ON state

LOGIC DIAGRAM (1 CIRCUIT)

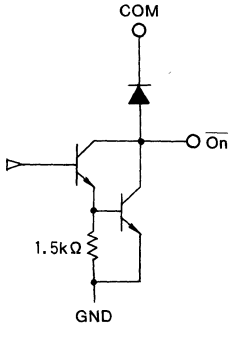


INPUT/OUTPUT EQUIVALENT CIRCUIT SCHEMATICS

1 INPUT CIRCUIT



2 OUTPUT CIRCUIT



BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS (T_a=−20℃∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+8	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage	Output is OFF	−0.5∼+30	V
I_O	Output current	Output is on	350	mA
Pd	Power dissipation	T_a=25℃	1.42	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
V_O	Applied output voltage	When output is OFF			30	V
I_O	Output current (per circuit)	All outputs ON simultaneously Duty cycle less than 25%			300	mA

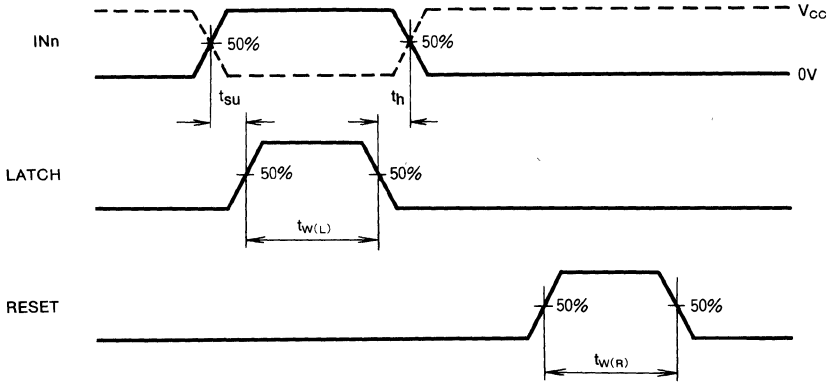
ELECTRICAL CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	1∼10 22	T_a=−20∼+75℃	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
R_{IN}	Input resistance			50			kΩ
V_{OL1}	Low-level output voltage	13∼20	I_{OL}=100mA			1.2	V
V_{OL2}			I_{OL}=200mA			1.4	V
V_{OL3}			I_{OL}=300mA			1.6	V
I_{OLK}	Output leakage current	13∼20	V_O=30V			50	μA
V_F	Clamp diode forward current	13∼20	I_F=300mA			2	V
I_R	Clamp diode reverse current		V_R=30V			50	μA
I_{CC1}	Supply current	21	All inputs are 0V, all outputs OFF			10	μA
I_{CC2}			Output : 1 circuit ON			1.4	mA

REQUIRED TIMING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(L)}$	Latch pulse width		0.1			μS
$t_{W(R)}$	Reset pulse width		0.1			μS
t_{su}	Data setup time		0			μS
t_h	Data hold time		0.1			μS

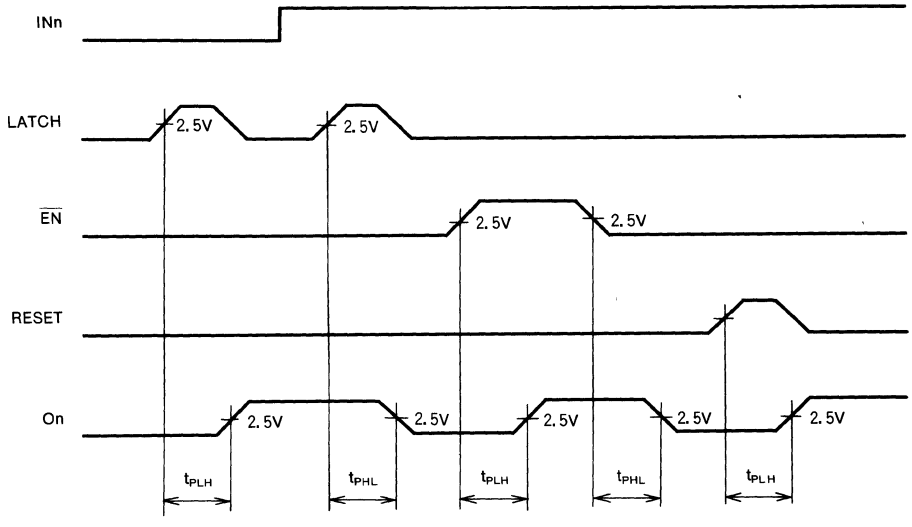
TIMING DIAGRAM



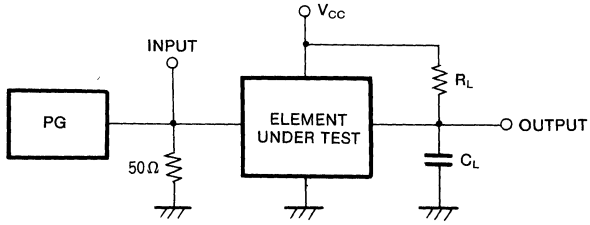
SWITCHING CHARACTERISTICS (T_a=+25℃, V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low to high-level output propagation time (Input LATCH to output $\overline{On}$)	V_{IH}=5V, V_{IL}=0V, R_L=100Ω, C_L=15pF (Note 1)		(0.6)	2	μS
t_{PHL}	High to low-level output propagation time (Input LATCH to output $\overline{On}$)			(0.1)	0.5	μS
t_{PLH}	Low to high-level output propagation time (Input $\overline{EN}$ to output $\overline{On}$)			(0.6)	2	μS
t_{PHL}	High to low-level output propagation time (Input $\overline{EN}$ to output $\overline{On}$)			(0.1)	0.5	μS
t_{PLH}	Low to high-level output propagation time (Input RESET to output $\overline{On}$)			(0.6)	2	μS

TIMING DIAGRAM

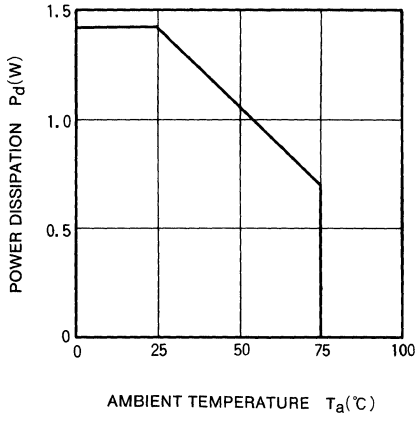


(Note 1) TEST CIRCUIT

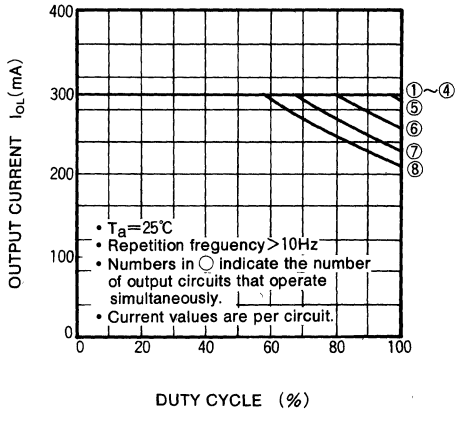


- Input waveform is taken as $t_r \leqq 20ns$ and $t_f \leqq 20ns$
- C_L includes wiring stray capacitance and probe input capacitance

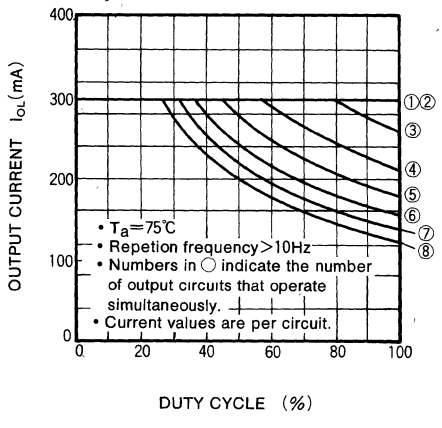
THERMAL DERATING



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT



M54977P

BI-CMOS 12-BIT SERIAL-INPUT,LATCHED DRIVER

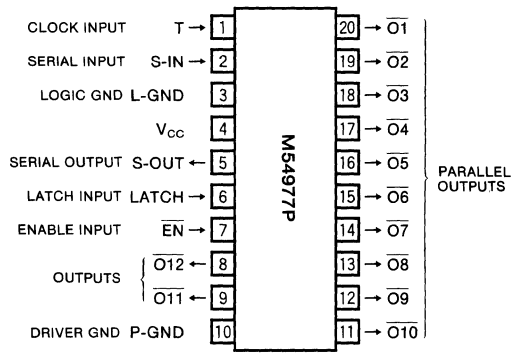
DESCRIPTION

The M54977P is a semiconductor integrated circuit fabricated using Bi-CMOS technology. It contains a serial input to serial/parallel output 12-bit CMOS shift register and CMOS latch as well as bipolar 12-bit parallel-output driver.

FEATURES

- Serial input to serial/parallel output
- Cascade connections possible through serial output
- Latch circuit included for each stage
- Enable input for output control
- Low supply current····· $I_{CC} \geqq 10\mu A$ at standby
- Serial input/output level is compatible with standard CMOS
- Driver : Withstand voltage····· $BV_{CEO} \geqq 30$
  Large drive current·····($I_{O(max)}$=200mA)
- Wide operating temperature range···· T_a=−20~+75℃

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

APPLICATION

Thermal printer head dot driver, Serial-to parallel conversion, Relay, solenoid driver

FUNCTION

The M54977P consists of an 12-bit D-type flip-flop, the output of which is connected to 12 latches.

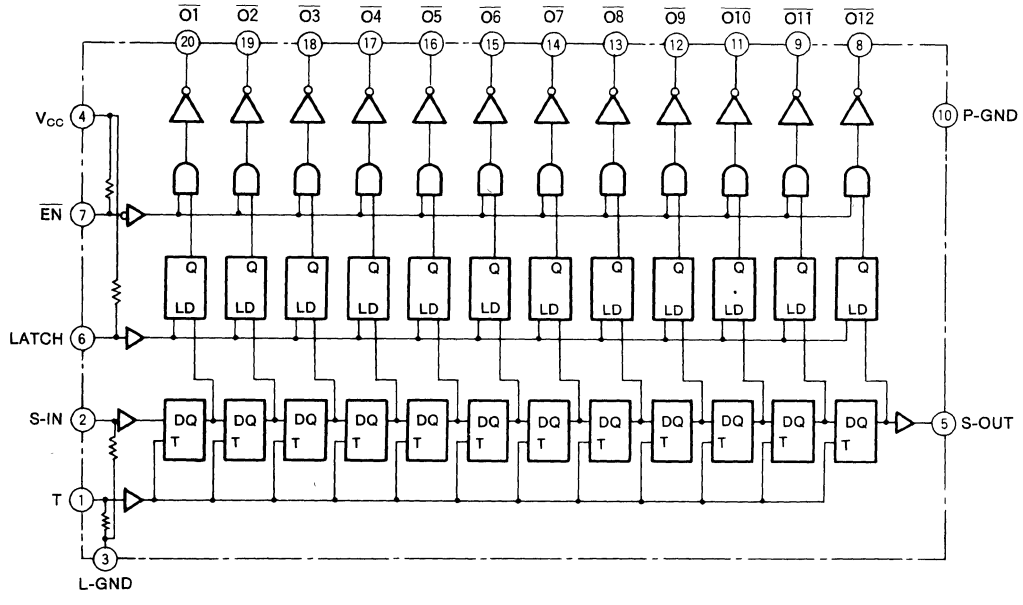
When data is applied to the serial data input (S-IN) and a clock pulse is applied to clock input (T), an "L" to "H" change of the clock will cause the data input signals to enter the internal shift registers and the data in the shift registers will be shifted in order.

Using a number of M54977P units for bit expansion in series will entail connecting serial output (S-OUT) to S-IN of the next-stage M54977P.

In parallel output, when the latch input is set to "H" and the output-control input (enable input $\overline{EN}$) is "L", a clock pulse changing from "L" to "H" will cause the serial data input signal to appear at output $\overline{O1}$, and the data will be shifted in order at outputs $\overline{O2}$~$\overline{O12}$.

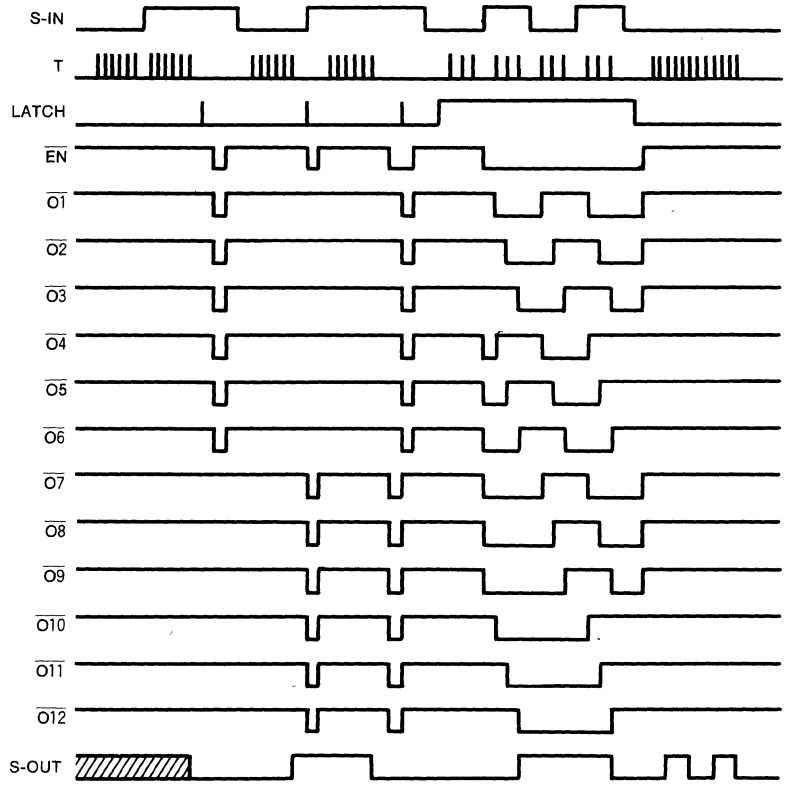
The parallel output will yield a signal that is inverted with

BLOCK DIAGRAM



respect to the serial data input.
Setting the LATCH input to "L" will prevent data from entering the latch.
When the $\overline{EN}$ input is set to "H", all outputs ($\overline{O1}$~$\overline{O12}$) will be set to OFF. Since the internal logic state of the IC is uncertain at power-on time, set the $\overline{EN}$ input to "H" (and outputs $\overline{O1}$~$\overline{O12}$ will set to OFF) until the input data is set and the internal logic state has been determined.
L-GND is the ground of the CMOS logic circuit section and P-GND is the ground for the output driver section ($\overline{O1}$~$\overline{O12}$), which is made up of bipolar transistors that are capable of driving large currents.

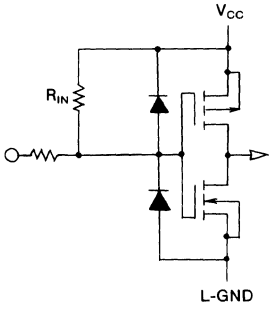
TIMING CHART



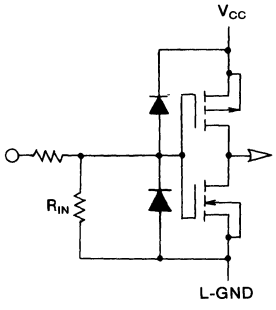
*The stage of the shaded areas is uncertain

INPUT/OUTPUT CIRCUIT SCHEMATICS

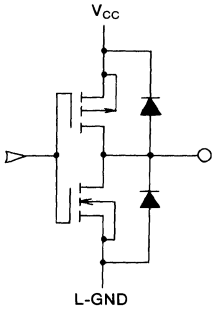
1 INPUT WITH PULL-UP RESISTOR
($\overline{EN}$, LATCH)



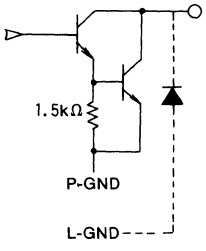
2 INPUT WITH PULL-DOWN RESISTOR
(T, S-IN)



3 SERIAL OUTPUT
(S-OUT)



4 PARALLEL OUTPUT
($\overline{O1}$~$\overline{O12}$)



BI-CMOS 12-BIT SERIAL-INPUT,LATCHED DRIVER

ABSOLUTE MAXIMUM RATING (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+8	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage	S-OUT	−0.5∼V_{CC}+0.5	V
		$\overline{O1}$∼$\overline{O12}$: Output is OFF	−0.5∼+30	
I_O	Output Current	$\overline{O1}$∼$\overline{O8}$: Output is ON	250	mA
P_d	Power dissipation	T_a=25℃	1.25	W
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃ unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
V_O	Applied output voltage	$\overline{O1}$∼$\overline{O12}$: When output is OFF			30	V
I_O	Output current (per circuit)	All outputs ON simultaneously Duty cycle less than 20%			200	mA

ELECTRICAL CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, unless otherwise noted)

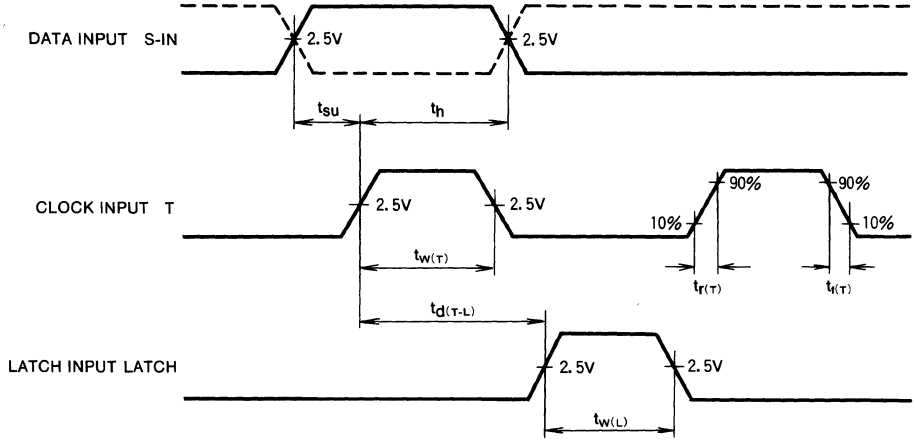
Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	1, 2 6, 7	T_a=−20∼+75℃	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
R_{IN}	input resistance			50		—	kΩ
V_{OH}	High-level output voltage	5	| I_O | ≦1μA	4.9		—	V
V_{OL}	Low-level output voltage			—		0.1	V
I_{OH}	High-level output current	5	V_{OH}=4.5V	−100		—	μA
I_{OL}	Low-level output current		V_{OL}=0.4V	400		—	μA
V_{OL1}	Low-level output voltage	8, 9 11∼20	I_{OL}=100mA	—		1.2	V
V_{OL2}			I_{OL}=200mA	—		1.4	V
I_{OLK}	Output leakage current		V_O=30V	—		50	μA
I_{CC1}	Supply current	4	Inputs free, all driver outputs OFF	—		10	μA
I_{CC2}			Driver output : 1 circuit ON	—		1.25	mA

BI-CMOS 12-BIT SERIAL-INPUT,LATCHED DRIVER

REQUIRED TIMING CONDITIONS (T_a=−20～+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$f_{(T)}$	Clock frequency	Input duty cycle 40～60%			2	MHz
$t_{W(T)}$	Clock pulse width		200			nS
$t_{W(L)}$	Latch pulse width		200			nS
t_{su}	Data setup time		100			nS
t_h	Data hola time		100			nS
$t_{d(T-L)}$	Clock-latch time		400			nS
$t_{r(T)}$	Clock pulse rise time				500	nS
$t_{f(T)}$	Clock pulse fall time				500	nS

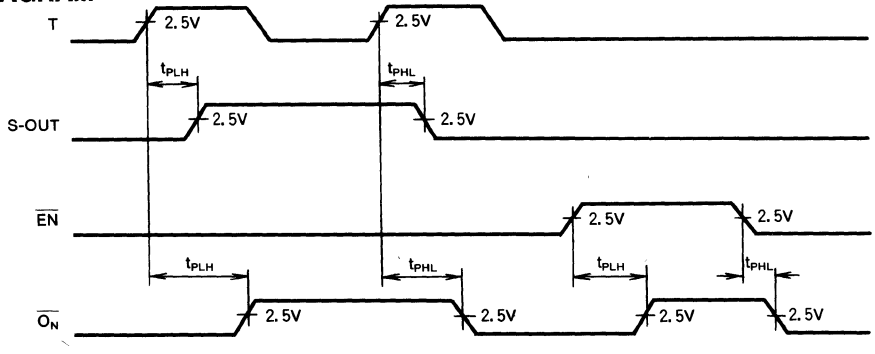
TIMING DIAGRAM



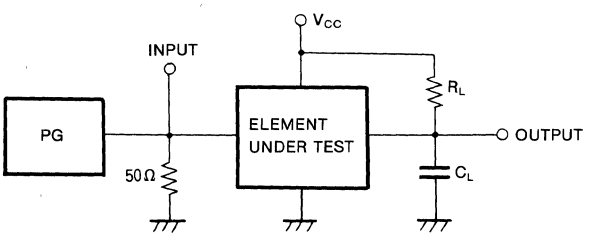
SWITCHING CHARACTERISTICS (T_a=+25℃, V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low to high-level output propagation time (Input T to output S-OUT)	V_{IH}=5V V_{IL}=0V R_L : S_{-OUT}=∞ R_L : $\overline{O_N}$=100Ω (N=1～8) C_L=15pF (Note 1)		(0.15)	0.3	μS
t_{PHL}	High to low-level output propagation time (Input T to output S-OUT)			(0.15)	0.3	μS
t_{PLH}	Low to high-level output propagation time (Input T to output $\overline{O_N}$)			(2)	10	μS
t_{PHL}	High to low-level output propagation time (Input T to output $\overline{O_N}$)			(0.5)	2	μS
t_{PLH}	Low to high-level output propagation time (Input EN to output $\overline{O_N}$)			(2)	10	μS
t_{PHL}	High to low-level output propagation time (Input EN to output $\overline{O_N}$)			(0.5)	2	μS

TIMING DIAGRAM



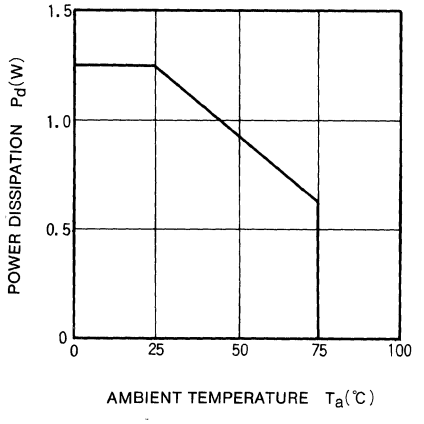
(Note 1) TEST CIRCUIT



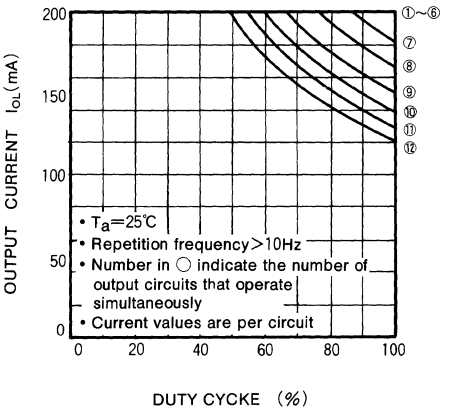
• Input waveform is taken as $t_r \leqq 20ns$ and $t_f \leqq 20ns$
C_L includes wiring stray capacitance and probe input capacitance.

TYPICAL CHARACTERISTICS

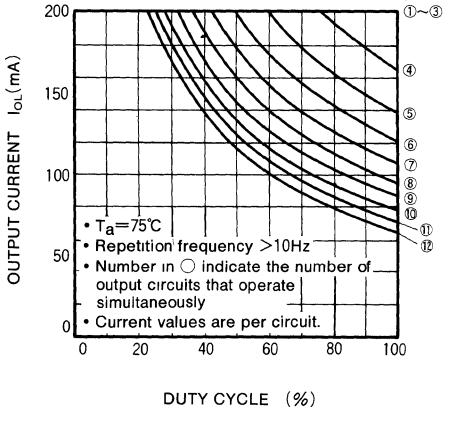
THERAL DREATING



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT



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