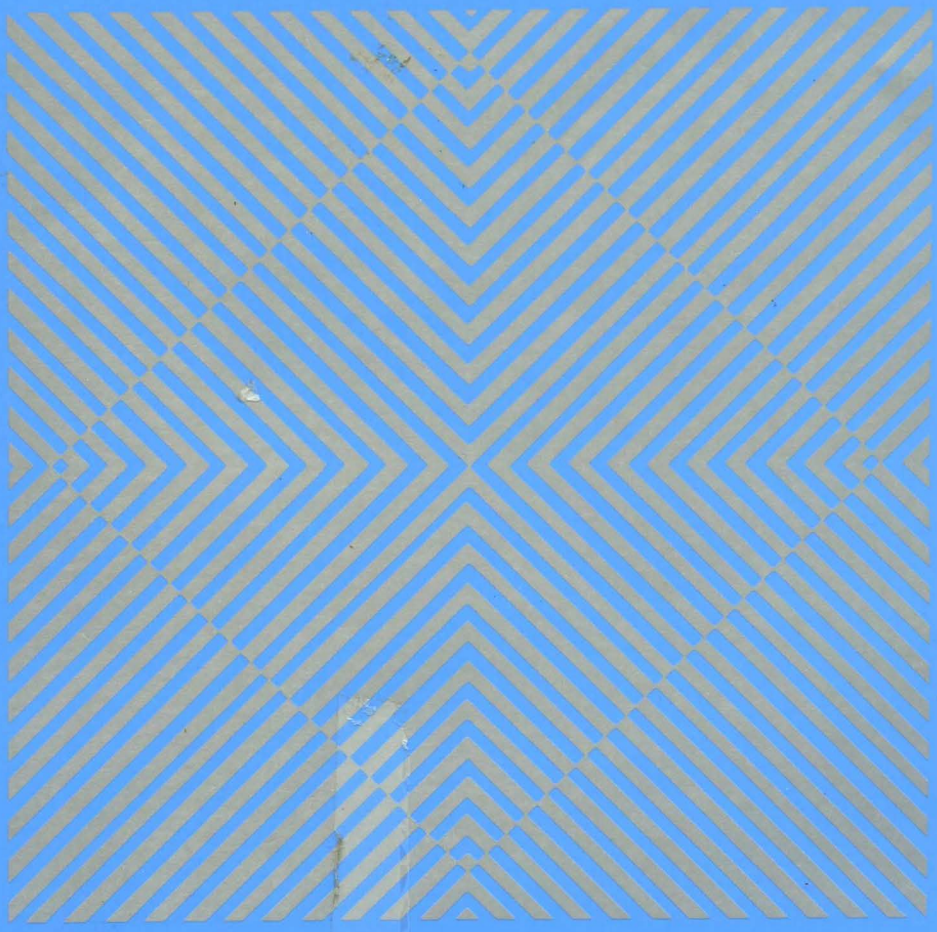
MITSUBISHI SEMICONDUCTORS

M38063M6-XXXFP/GP

USER'S MANUAL



MITSUBISHI ELECTRIC

USER'S MANUAL

M38063M6-XXXFP/GP

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FOREWORD

This user's manual describes the hardware of Mitsubishi's M38063M6-XXXFP/GP CMOS 8-bit microcomputer.
After reading this manual, the user should have a through knowledge of the functions and features of the M38063M6-XXXFP/GP, and should be able to fully utilize the product. The manual starts with specifications and ends with application examples.
For software details, refer to the "MELPS 740 Programming Manual".

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CHAPTER 1

DESCRIPTION

DESCRIPTION

The M38063M6-XXXFP/GP is an 8-bit single-chip microcomputer created in a silicon gate CMOS process.

Built into this single-chip microcomputer are:

- Serial I/O1 function (either clock synchronous or UART method selectable in software)
- Serial I/O2 function (clock synchronous method only)
- Eight-bit timers
- A-D converter (successive approximation comparison method)
- D-A converter (R-2R network method)

The M38063M6-XXXFP/GP is designed as a dedicated microcomputer for household appliances, office automation (OA) equipment, and audiovisual equipment. The reduced power dissipation of the CMOS process also makes this microcomputer extremely useful for applications utilizing battery power.

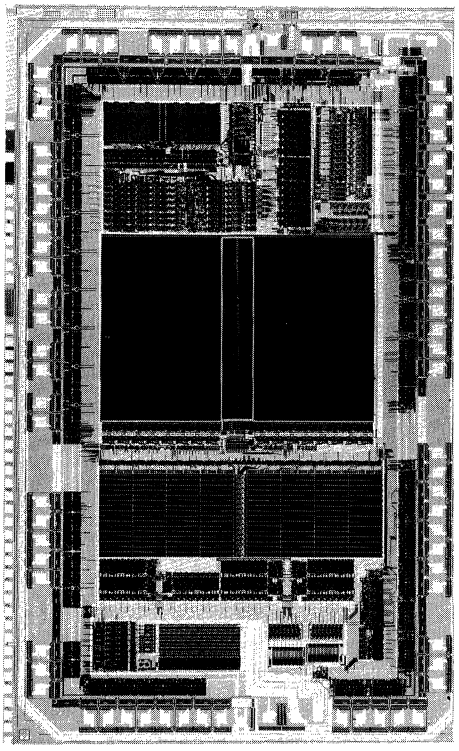


Photo of M38063M6-XXXFP/GP Chip

1.1 Function Description

The functions of the M38063M6-XXXFP/GP are outlined in Table1.1.1. These two types (M38063M6-XXXFP and M38063M6-XXXGP) differ only in the package. In this manual, the two types are distinguished only where there is a functional difference between them. The suffix FP indicates a 0.8mm-lead pitch package and GP indicates a 0.65mm-lead pitch package.

Table 1.1.1 Functions of M38063M6-XXXFP/GP

Parameter		Function
Basic instructions		71
Instruction execution time		0.8μs (shortest instruction, at 5MHz oscillation frequency)
Oscillation frequency		5MHz (max.)
Memory size	ROM	24,316 bytes of user area
	RAM	512 bytes
Input/output ports	P0~P6,P8	8-bit X 8 (CMOS output)
	P7	8-bit X 1 (N-channel open drain output)
Serial I/O1		Clock synchronous or asynchronous
Serial I/O2		Clock synchronous
Timers		8-bit prescaler X 3 and 8-bit timer X 4
A-D converter		8-bit resolution X 8 channels
D-A converter		8-bit resolution X 2 channels
Interrupts		7 external, 8 internal, 1 software
Clock generation circuit		Built-in (connect to external ceramic resonator or quartz crystal oscillator)
Supply voltage		4.0 to 5.5V
Power dissipation		20mW (at 5MHz oscillation frequency, typ.)
Input/output characteristics	Input/output break -down voltage	5V
	Output current	10mA
External memory expansion		Possible
Operating temperature range		–20 to 85°C
Device structure		CMOS silicon gate
Package	M38063M6-XXXFP	80-pin plastic molded QFP (0.8mm-lead pitch)
	M38063M6-XXXGP	80-pin plastic molded QFP (0.65mm-lead pitch)

1.2 M3806x Expansion

Mitsubishi plans to expand the M3806x group by producing a wide range of variations. The concept behind this expansion is to support:

(1) Products with the same functions but different memory capacities
(2) Mask ROM, one-time programmable ROM, and EPROM versions
(3) A variety of packages

Products with ROM capacities ranging from 12K bytes to 32K bytes and RAM capacities ranging from 384 bytes to 1024 bytes are under development, as shown in Figure 1.2.1. ROM capacity is plotted along the vertical axis and RAM capacity is plotted along the horizontal axis.

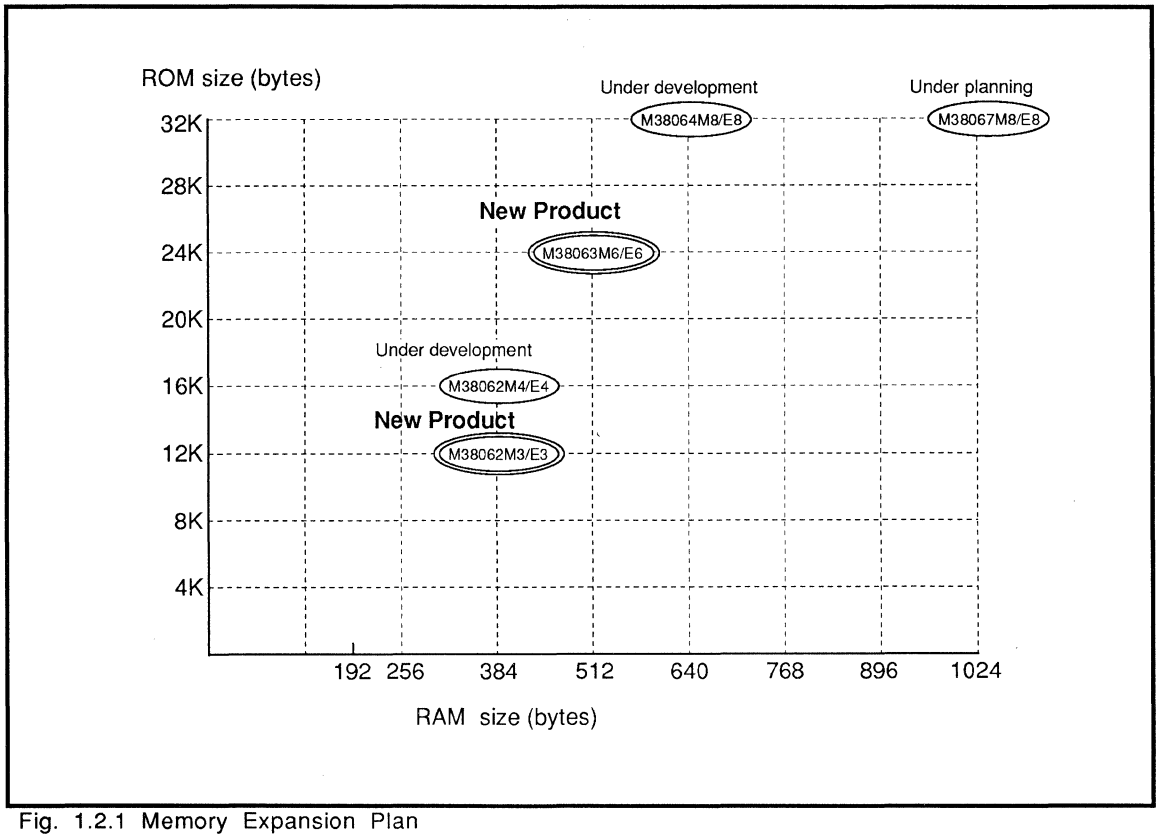


Fig. 1.2.1 Memory Expansion Plan

The one-time programmable version of the M38062M3-XXXFP is the M38062E3-XXXFP. The one-time programmable version of the M38062M3-XXXGP is the M38062E3-XXXGP. The EPROM version, which can be erased by ultra-violet light, is the M38062E3FS.
The one-time programmable version of the M38063M6-XXXFP is the M38063E6-XXXFP. The one-time programmable version of the M38063M6-XXXGP is the M38063E6-XXXGP. The EPROM version, which can be erased by ultra-violet light, is the M38063E6FS.
Mitsubishi intends to support mask ROM, one-time programmable ROM, and EPROM versions of all the products with the ROM and RAM capacities that are currently under development as shown in Figure 1.2.1.

(1) One-time programmable version
Non-erasable programs can be written into the internal PROM of this one-time programmable microcomputer. For details of the functions of this version, see Chapter 3, "INTERNAL PROM VERSION".
(2) EPROM version
Erasable programs can be written into the internal EPROM of this EPROM microcomputer. For details of the functions of this version, see Chapter 3, "INTERNAL PROM VERSION".

Table 1.2.1 Products Supported as of September 1990

Type name	ROM	RAM	Package	Remarks
M38062M3-XXXFP	12K bytes	384 bytes	0.8mm-pitch QFP	
M38062M3-XXXGP	12K bytes	384 bytes	0.65mm-pitch QFP	
M38062E3-XXXFP	12K bytes	384 bytes	0.8mm-pitch QFP	One-time programmable version
M38062E3-XXXGP	12K bytes	384 bytes	0.65mm-pitch QFP	One-time programmable version
M38062E3FP	12K bytes	384 bytes	0.8mm-pitch QFP	One-time programmable version*
M38062E3GP	12K bytes	384 bytes	0.65mm-pitch QFP	One-time programmable version*
M38062E3FS	12K bytes	384 bytes	0.8mm-pitch LCC	EPROM version
M38063M6-XXXFP	24K bytes	512 bytes	0.8mm-pitch QFP	
M38063M6-XXXGP	24K bytes	512 bytes	0.65mm-pitch QFP	
M38063E6-XXXFP	24K bytes	512 bytes	0.8mm-pitch QFP	One-time programmable version
M38063E6-XXXGP	24K bytes	512 bytes	0.65mm-pitch QFP	One-time programmable version
M38063E6FP	24K bytes	512 bytes	0.8mm-pitch QFP	One-time programmable version*
M38063E6GP	24K bytes	512 bytes	0.65mm-pitch QFP	One-time programmable version*
M38063E6FS	24K bytes	512 bytes	0.8mm-pitch LCC	EPROM version

* : Shipped blank.

The names of all Mitsubishi's single-chip microcomputers reflect differences in ROM capacity, RAM capacity, memory type, and package. The names of types in the M3806x group are as shown in Figure 1.2.2.

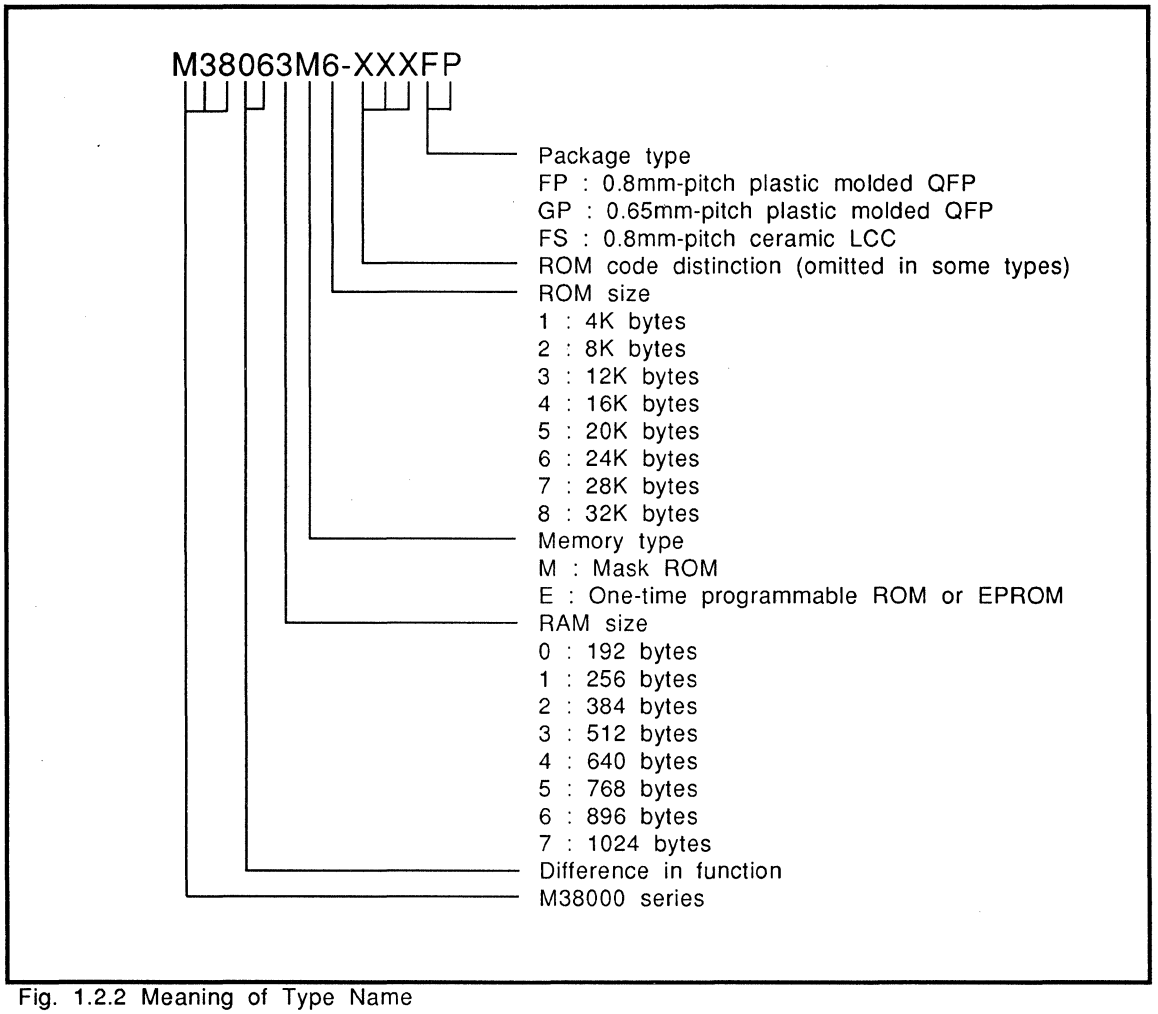
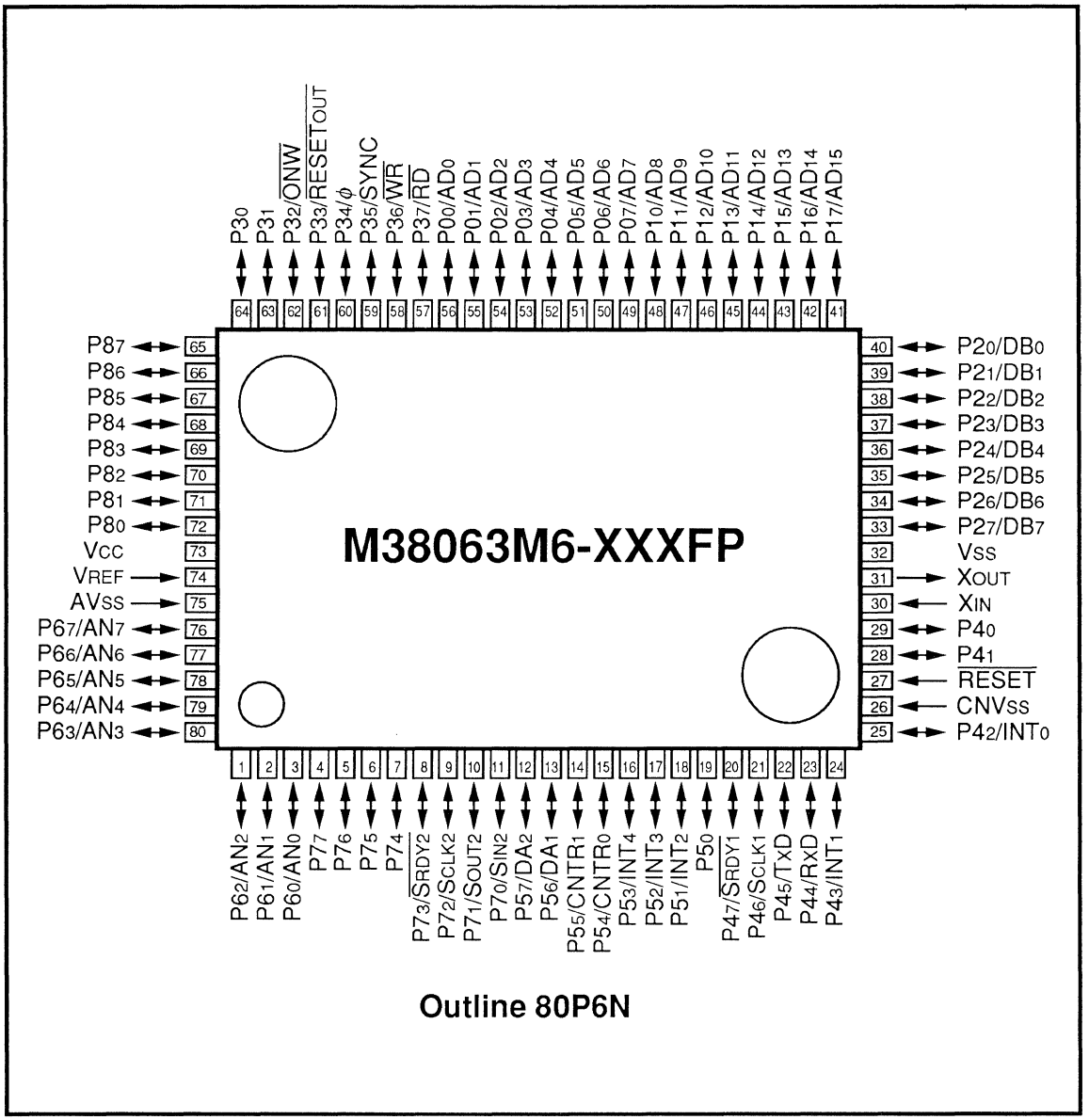


Fig. 1.2.2 Meaning of Type Name

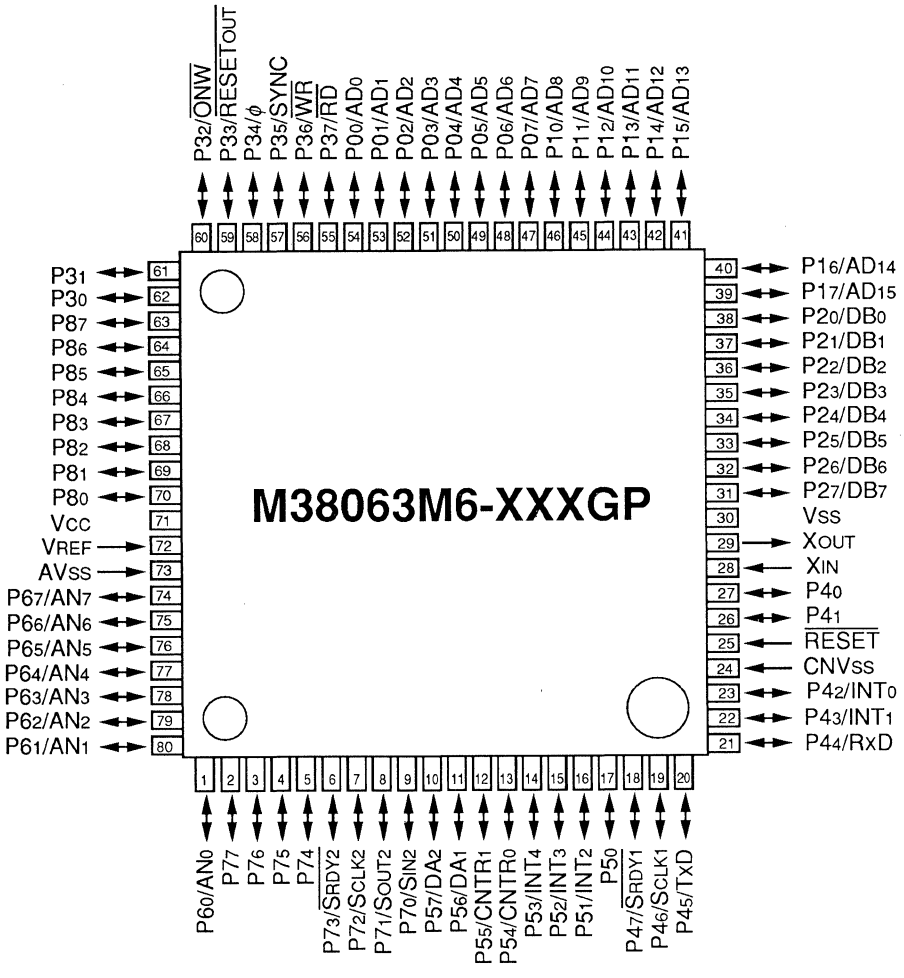
1.3 Pin Configuration

The pin configuration of the M38063M6-XXXFP is shown in Figure 1.3.1 and the pin configuration of the M38063M6-XXXGP is shown in Figure 1.3.2.



Outline 80P6N

Fig. 1.3.1 M38063M6-XXXFP Pin Configuration (Top View)



Outline 80P6S

Fig. 1.3.2 M38063M6-XXXGP Pin Configuration (Top View)

1.4 Pin Description

The pin functions are listed in Table 1.4.1.

Table 1.4.1 Pin Description

Pin	Name	Function
V_{CC}, V_{SS}	Power supply	Power supply inputs 4.0 to 5.5V to V_{CC}, and 0V to V_{SS}.
AV_{SS}	Analog power supply	The GND input pin for the A-D converter and the D-A converter. Keep at the same potential as V_{SS}.
V_{REF}	A-D/D-A reference voltage input	The reference voltage input pin for the A-D converter and the D-A converter.
CNV_{SS}	CNV_{SS}	Controls the operating mode of the chip. Normally connected to V_{SS} or V_{CC}.
$\overline{RESET}$	Reset input	To enter the reset state, this pin must be kept "L" for more than 2μs (under normal V_{CC} conditions). If the crystal or ceramic resonator requires more time to stabilize, extend this "L" level time as appropriate.
X_{IN}	Clock input	Input and output signals to and from the internal clock generation circuit. Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency. If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.
X_{OUT}	Clock output	
$P0_0$~$P0_7$	I/O port P0	An 8-bit CMOS I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. In modes other than single-chip, P0 is used to output the low-order bits of the address bus.
$P1_0$~$P1_7$	I/O port P1	An 8-bit CMOS I/O port with the same function as port P0. In modes other than single-chip, P1 is used to output the high-order bits of the address bus.
$P2_0$~$P2_7$	I/O port P2	An 8-bit CMOS I/O port with the same function as port P0. In modes other than single-chip, P2 is used as data bus I/O.
$P3_0$~$P3_7$	I/O port P3	An 8-bit CMOS I/O port with the same functions as port P0. In modes other than single-chip, P3 is used as a control bus.
$P4_0$~$P4_7$	I/O port P4	An 8-bit CMOS I/O port with the same functions as port P0. Can also be programmed to be serial I/O1 function pins.
$P5_0$~$P5_7$	I/O port P5	An 8-bit CMOS I/O port with the same functions as port P0. Can also be programmed to be I/O pins for timer X and timer Y, or output pins for the D-A converter.
$P6_0$~$P6_7$	I/O port P6	An 8-bit CMOS I/O port with the same functions as port P0. Can also be used as input pins for the A-D converter.
$P7_0$~$P7_7$	I/O port P7	An 8-bit I/O port with the same functions as port P0, except that the output structure is N-channel open drain. Can also be programmed to be serial I/O2 function pins.
$P8_0$~$P8_7$	I/O port P8	An 8-bit CMOS I/O port with the same functions as port P0.

1.5 Functional Block Diagram

A block diagram of the M38063M6-XXXFP is shown in Figure 1.5.1.

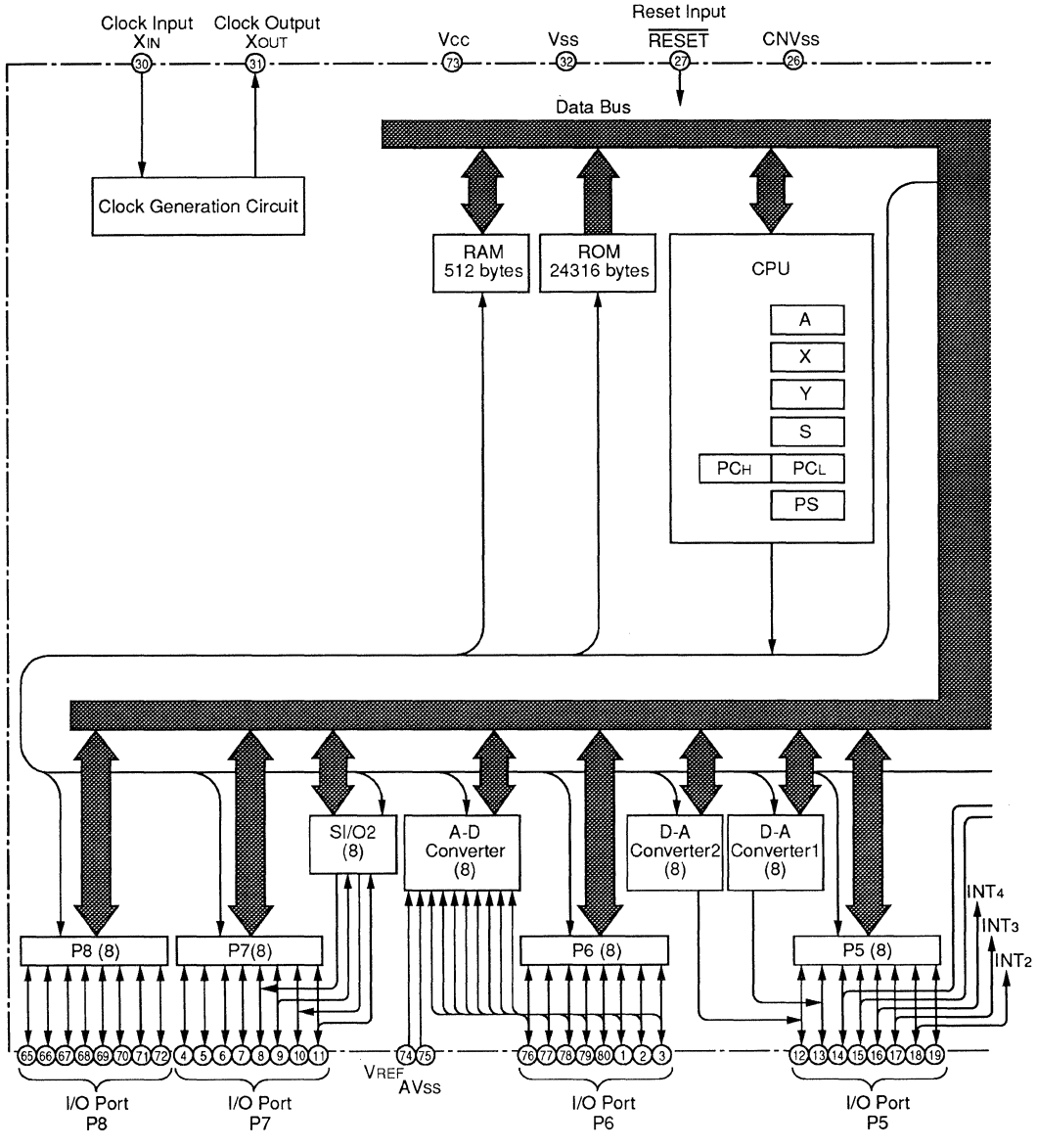
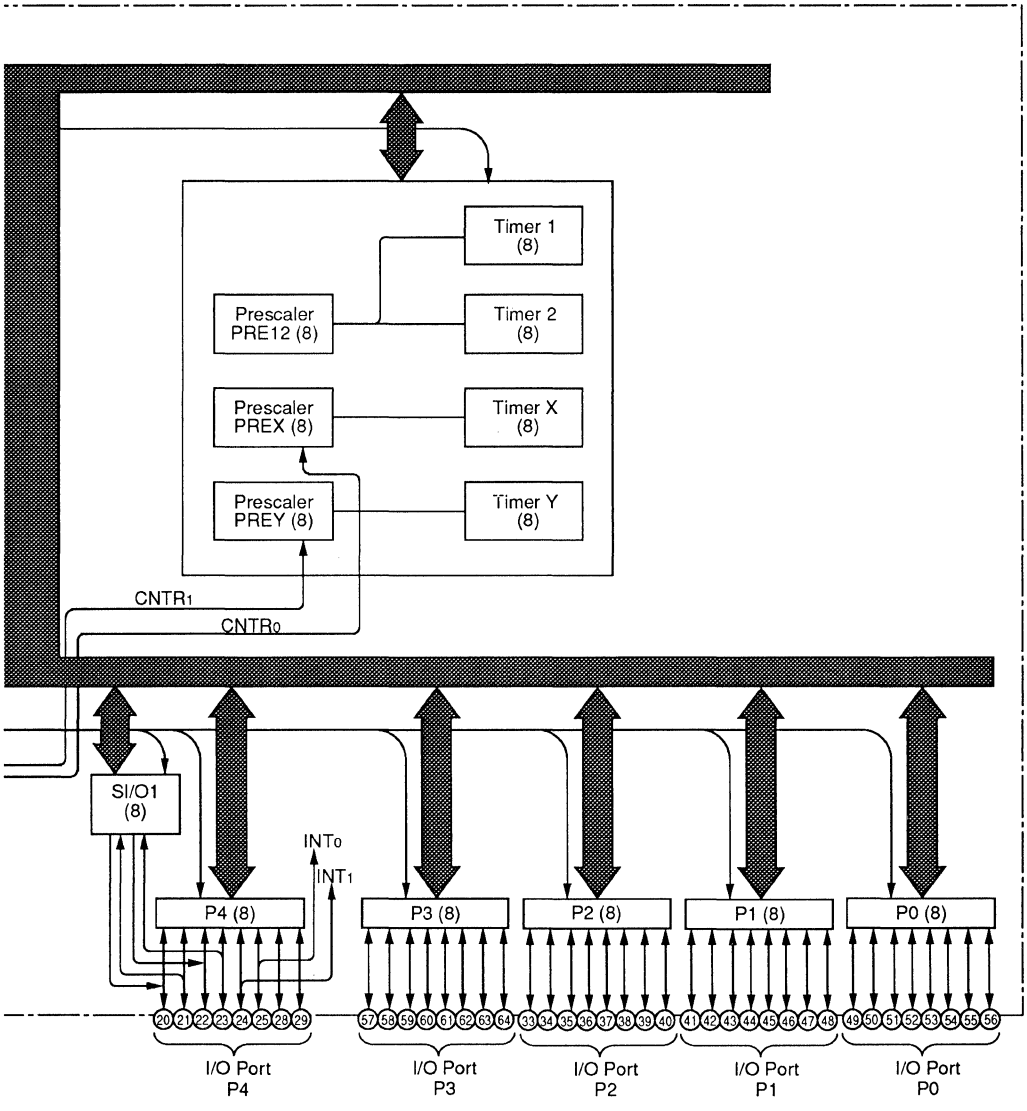


Fig. 1.5.1 Functional Block Diagram of M38063M6-XXXFP


Timer 1
(8)
Prescaler
PRE12 (8)
Timer 2
(8)
Prescaler
PREX (8)
Timer X
(8)
Prescaler
PREY (8)
Timer Y
(8)
CNTR1
CNTR0
SI/O1
(8)
INT0
INT1
P4 (8)
P3 (8)
P2 (8)
P1 (8)
P0 (8)
20 21 22 23 24 25 28 29
57 58 59 60 61 62 63 64
33 34 35 36 37 38 39 40
41 42 43 44 45 46 47 48
49 50 51 52 53 54 55 56
I/O Port
P4
I/O Port
P3
I/O Port
P2
I/O Port
P1
I/O Port
P0

1.6 Comparison with the 740 Series

The main differences between the M38000 series (M38063M6-XXXFP/GP) and the 740 series (M50747-XXXSP/FP) are listed in Table 1.6.1.

Table 1.6.1 Main Differences between the M38000 Series and the 740 Series

Parameter	M38063M6-XXXFP/GP	M50747-XXXSP/FP
Minimum instruction execution time	0.8μs (at 5MHz)	1.0μs (at 8MHz)
Reset vector address	$FFFD_{16}$, $FFFC_{16}$	$FFFF_{16}$, $FFFE_{16}$
SFR area	0000_{16} to $003F_{16}$	$00E0_{16}$ to $00FF_{16}$
ROM area reserved for device testing	130 bytes (Note 1)	None
Readout of port direction registers	Disabled (Note 2)	Enabled
Supply voltage	4.0 to 5.5V	4.5 to 5.5V
Operating temperature range	−20 to 85°C	−10 to 70°C
Feedback resistor for clock generation circuit	Built in	None
$\overline{ONW}$ function (for memory expansion)	Built in	None
$\overline{RD}/\overline{WR}$ separation signal generation function (for memory expansion)	Built in	None
External memory area (for memory expansion)	0000_{16} to 0007_{16}, and 0440_{16} up	$00C0_{16}$ to $00E7_{16}$, and 0140_{16} up

Note 1: Addresses $A000_{16}$ to $A07F_{16}$, $FFFE_{16}$, and $FFFF_{16}$

Note 2: The direction registers should not be read. Instructions that read the direction registers before writing, e.g. the read modify write instructions such as the SEB, CLB, and BBC instructions, should not be used.

Note 3: For details of the reset vector addresses, the SFR area, and the ROM area reserved for device testing, see "2.3 Memory Allocation".

Note 4: For details of port direction register readout, the $\overline{ONW}$ function, the $\overline{RD}/\overline{WR}$ separation signal generation function, and the external memory area, see "2.4 Processor Mode and Input/ Output Pins".

The M38000 series uses the same machine language instructions as the 740 series. For software details, refer to the "MELPS 740 Programming Manual".

CHAPTER 2

FUNCTIONAL DESCRIPTION

2.1 Central Processing Unit (CPU)

The central processing unit (CPU) of the M38063M6-XXXFP/GP has the following six registers:

- Accumulator (A)
- Index register X (X)
- Index register Y (Y)
- Stack pointer (S)
- Processor status register (PS)
- Program counter (PC)

These registers are described below.

2.1.1 Register structure

Five of these registers (the accumulator (A), index register X (X), index register Y (Y), stack pointer (S), and processor status register (PS)) are 8-bit registers, but the program counter (PC) is a 16-bit register consisting of two 8-bit registers (PC_H and PC_L).

After a hardware reset, bit 2 (the I flag) of the PS is set to "1" and the values of addresses $FFFC_{16}$ and $FFFD_{16}$ are stored in the PC, but the values of the rest of the PS and the other registers are undefined. Initialization of undefined registers may be necessary for some programs.

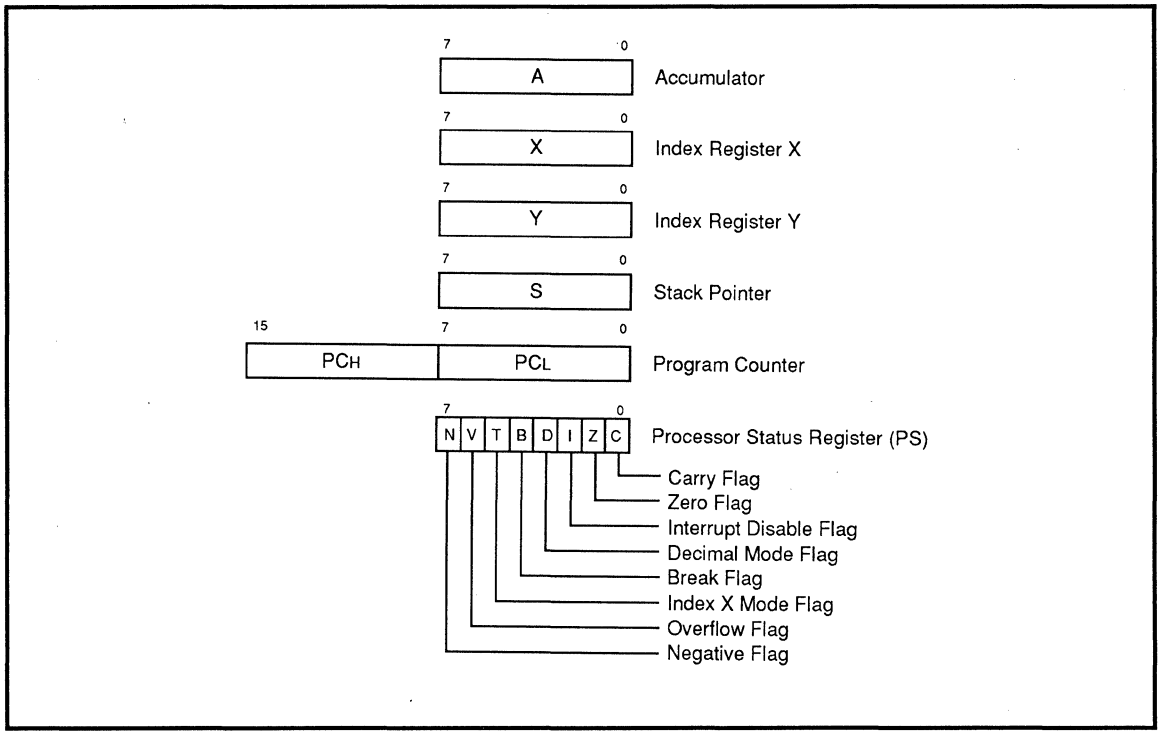


Fig. 2.1.1 Register Structure

2.1.2 Accumulator (A)

The accumulator is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., are executed mainly through the accumulator.

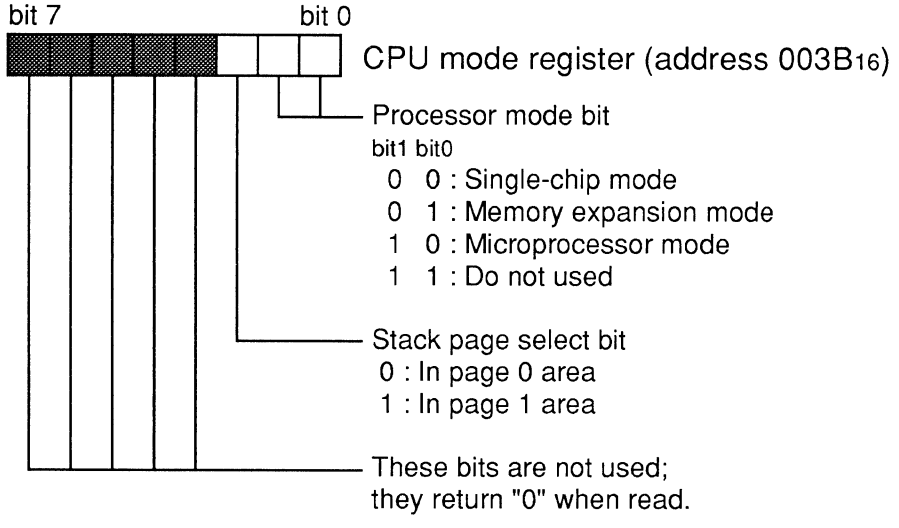
2.1.3 Index register X (X), index register Y (Y)

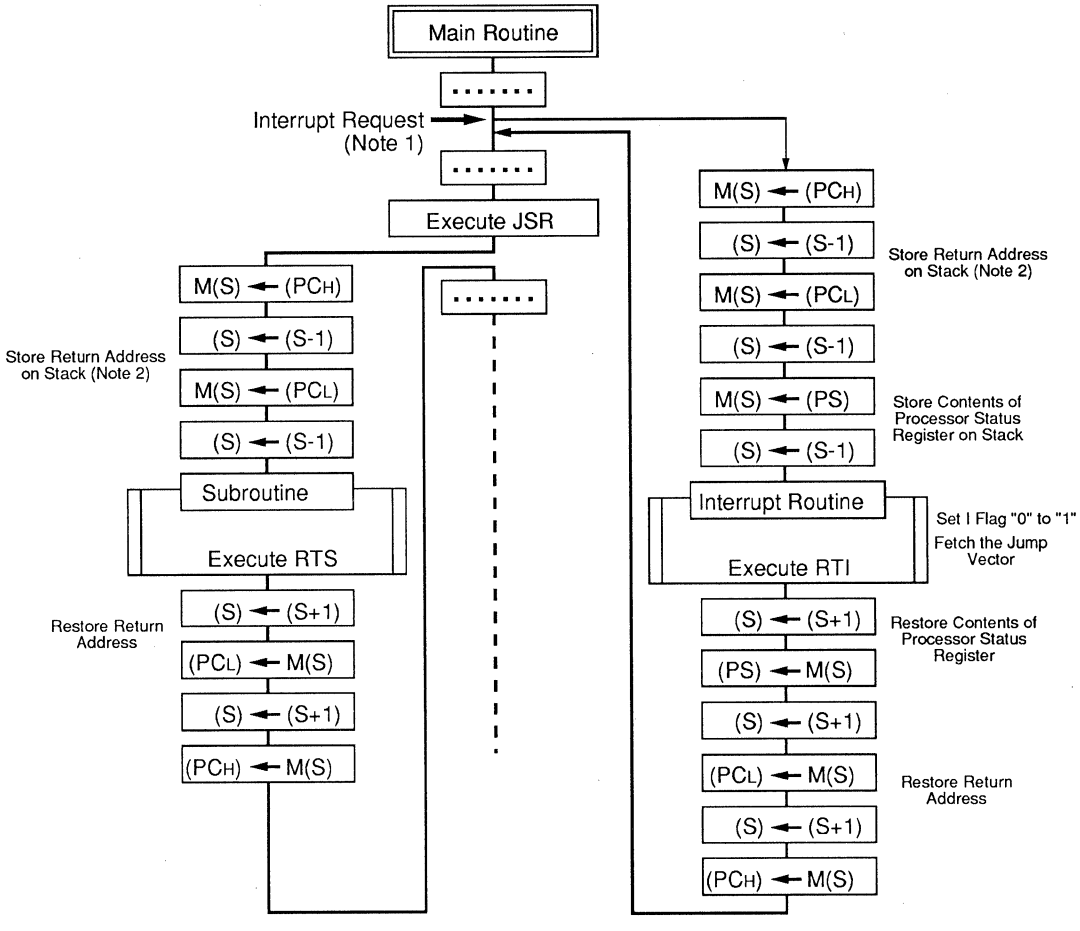
Both index register X and index register Y are 8-bit registers. In the index addressing modes, the contents of these registers are added to the value of the OPERAND to specify the real address. These addressing modes are useful for referencing subroutine tables and memory tables.
These index registers also have increment, decrement, comparison, and data transfer functions to allow these registers to have some of the functions of the accumulator.
In indirect addressing mode, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address. When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

2.1.4 Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines. The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Select Bit, bit 2 of the CPU Mode Register (address $003B_{16}$). If the Stack Page Select Bit is "0" (the default value), then the RAM in the zero page (addresses 0040_{16} to $00FF_{16}$) is used as the stack area. If the Stack Page Select Bit is "1", then RAM in page 1 (addresses 0100_{16} to $01FF_{16}$) is used as the stack area. The base of the stack must be set in software, and the stack grows towards lower addresses from that point.
The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 2.1.2.

Table 2.1.1 Structure of CPU Mode Register





Note 1 : The condition to enable an interrupt → Interrupt enable bit is "1"
Interrupt disable flag is "0"

Note 2 : When an interrupt occurs, the address of the next instruction to be executed is stored in the stack area. When a subroutine is called, the address of the instruction the next instruction to be executed minus one is stored in the stack area.

Fig. 2.1.2 Register Push and Pop when servicing interrupts and calling subroutines

2.1.5 Program counter (PC)

The program counter is a 16-bit register consisting of two 8-bit sub-registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

2.1.6 Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag.

After reset, the I flag is set to "1", but all other flags are undefined. Since the T and D flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

Each bit of the processor status register are explained below.

(1) Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It is also changed by shift or rotate instructions. The C flag can be set directly by the set carry (SEC) instruction and cleared by the clear carry (CLC) instruction.

(2) Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0". In decimal mode, the Z flag is invalid.

(3) Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1". When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The I flag can be set by the set interrupt disable (SEI) instruction and cleared by the clear interrupt disable (CLI) instruction.

(4) Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic. The D flag can be set by the set decimal mode (SED) instruction and cleared by the clear decimal mode (CLD) instruction.

Since the D flag directly affects calculations, it should always be initialized after a reset.

(5) Break flag (B)

The B flag is used to indicate whether the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes. The T flag can be set by the set T flag (SET) instruction and cleared by the clear T flag (CLT) instruction.

Since the T flag directly affects calculations, it should always be initialized after a reset.

(7) Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds the range from + 127 to −128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag. The V flag can be cleared by the CLV instruction, but there is no set instruction. In decimal mode, the V flag is invalid.

(8) Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative (bit 7 is "1"). When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag. These are no instructions for directly setting or clearing the N flag. In decimal mode, the N flag is invalid.

2.2 Access Area

The program counter of the M38063M6-XXXFP/GP is 16-bits wide and can access 64K bytes of memory area (from address 0000_{16} to $FFFF_{16}$). Of this 64K-byte memory area, the first 256 bytes are the zero page area and the last 256 bytes are the special page area. These areas can be accessed by two byte commands by using special addressing modes.

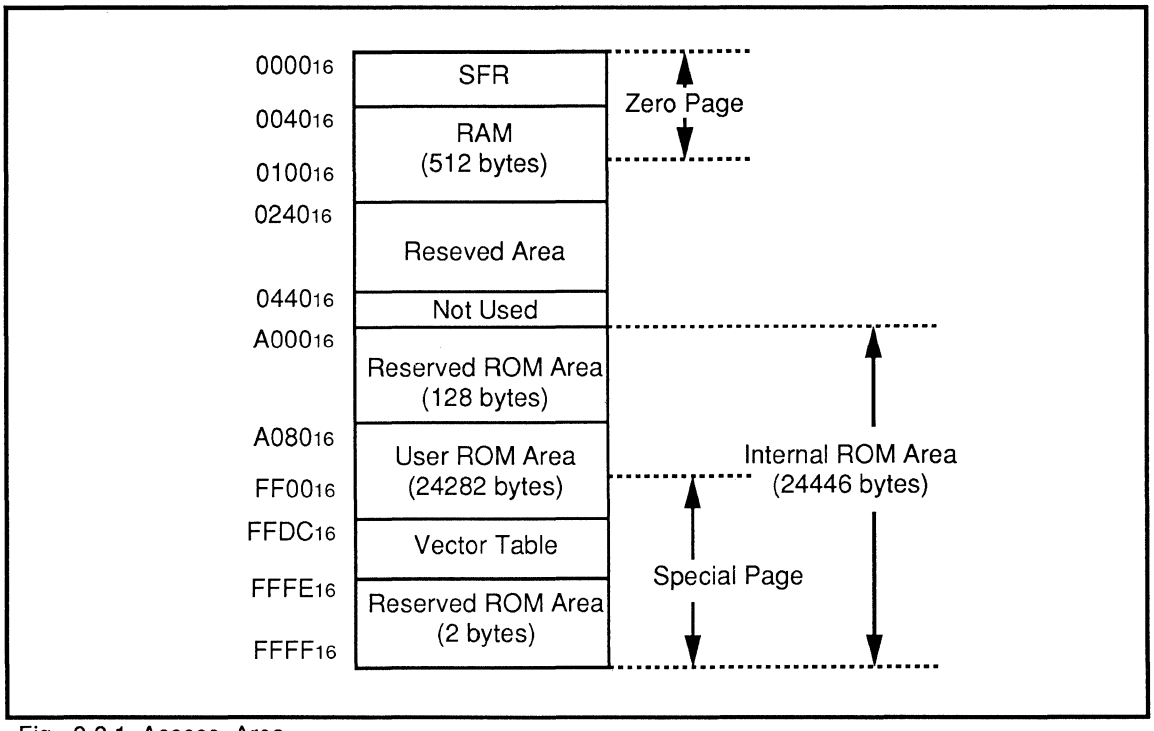


Fig. 2.2.1 Access Area

In the M38063M6-XXXFP/GP, all the ROM, RAM, I/O functions, and control registers are located in the same memory map. This means that there is no need for programs to distinguish between memory and I/O operations; the same instructions can both transfer data and operate on data.

2.2.1 Zero page (addresses 0000_{16} to $00FF_{16}$)

The 256 bytes from address 0000_{16} to address $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode shown in Figure 2.2.2 can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with fewer instruction cycles.

2.2.2 Special page (addresses $FF00_{16}$ to $FFFF_{16}$)

The 256 bytes from address $FF00_{16}$ to address $FFFF_{16}$ are called the special page area.
The special page addressing mode shown in Figure 2.2.2 can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with fewer instruction cycles.
Frequently used subroutines are normally stored in this area.

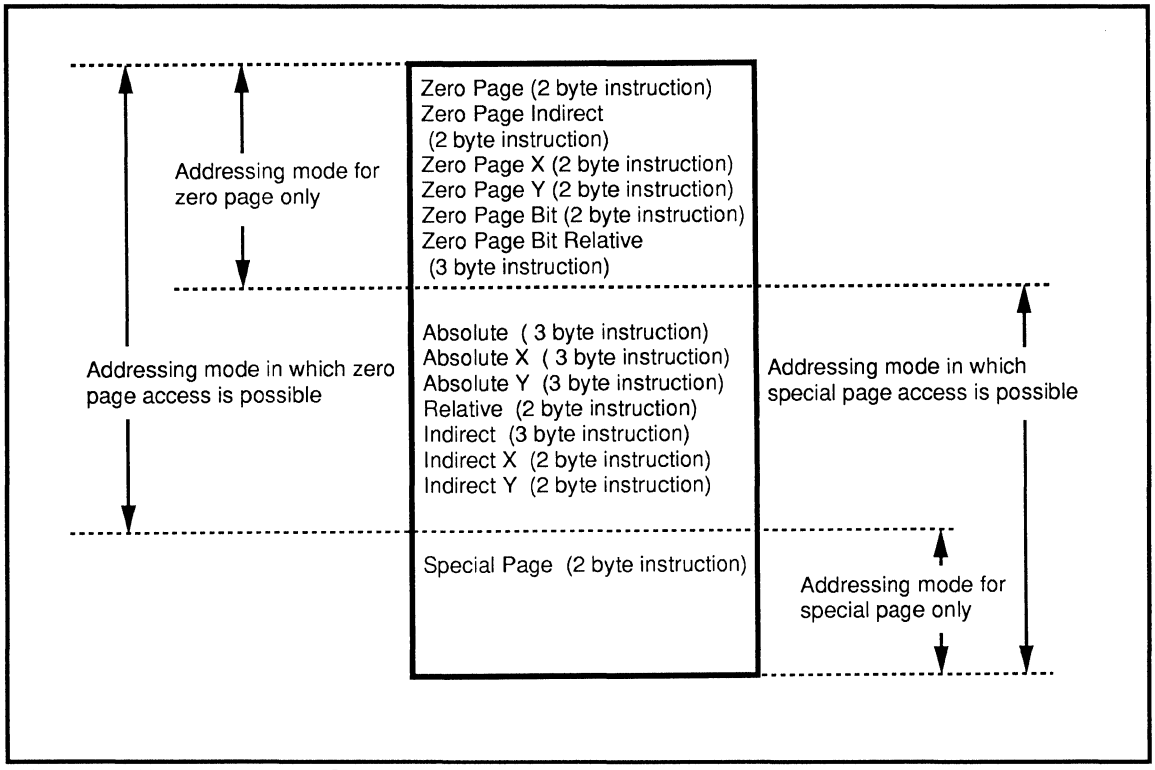


Fig. 2.2.2 Zero Page and Special Page Addressing Modes

2.3 Memory Allocation

The memory allocation of the M38063M6-XXXFP/GP in single-chip mode is shown in Figure 2.3.1.

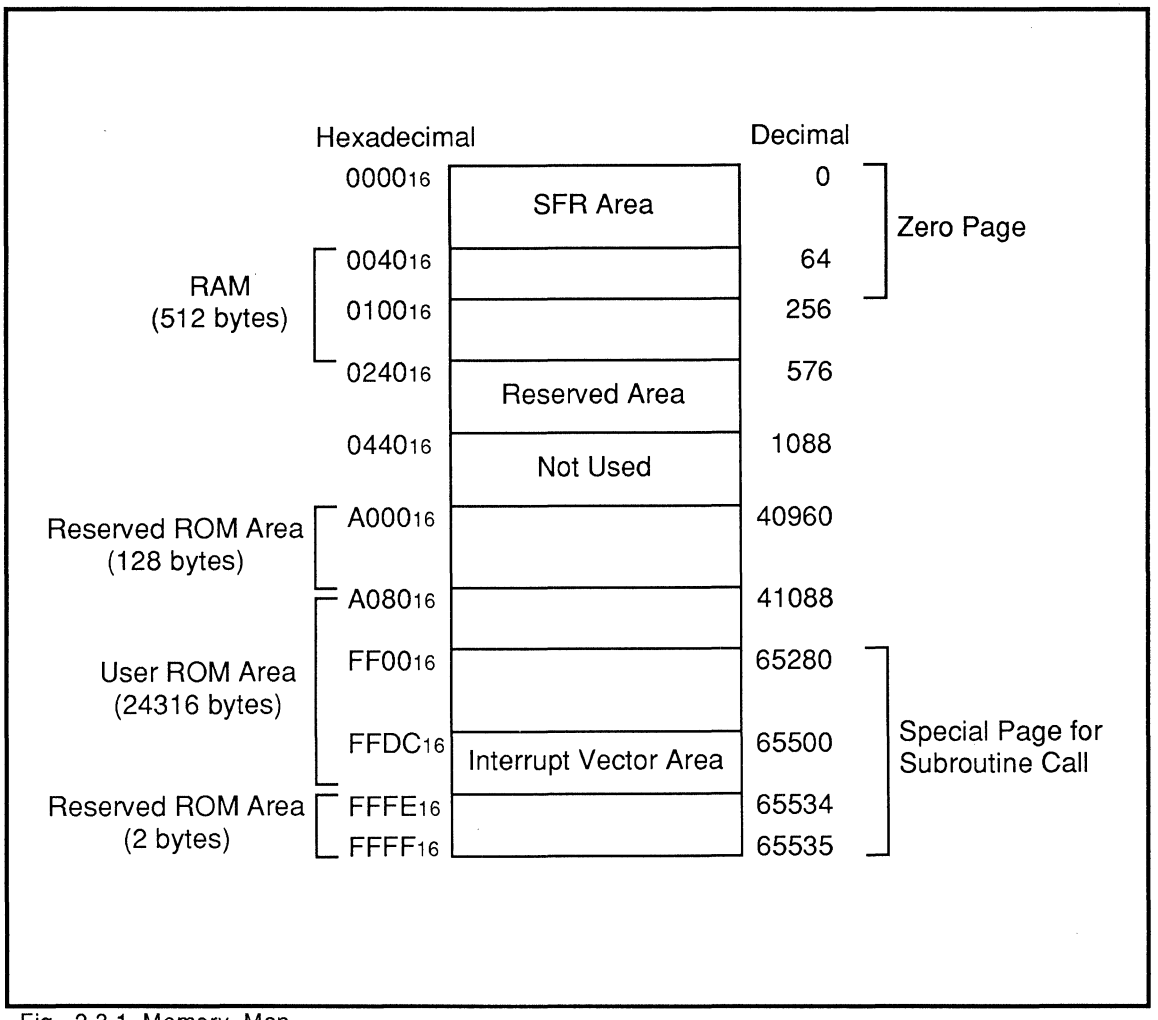


Fig. 2.3.1 Memory Map

2.3.1 Special function register (SFR)

The Special function register (SFR) area contains the registers relating to functions such as I/O ports, timers, serial I/O, and interrupts. The SFR area is allocated to addresses 0000_{16} to $003F_{16}$, as shown in Figure 2.3.2.

0000_{16}	Port P0	0020_{16}	Prescaler 12
0001_{16}	Port P0 Direction Register	0021_{16}	Timer 1
0002_{16}	Port P1	0022_{16}	Timer 2
0003_{16}	Port P1 Direction Register	0023_{16}	Timer XY Mode Register
0004_{16}	Port P2	0024_{16}	Prescaler X
0005_{16}	Port P2 Direction Register	0025_{16}	Timer X
0006_{16}	Port P3	0026_{16}	Prescaler Y
0007_{16}	Port P3 Direction Register	0027_{16}	Timer Y
0008_{16}	Port P4	0028_{16}	
0009_{16}	Port P4 Direction Register	0029_{16}	
$000A_{16}$	Port P5	$002A_{16}$	
$000B_{16}$	Port P5 Direction Register	$002B_{16}$	
$000C_{16}$	Port P6	$002C_{16}$	
$000D_{16}$	Port P6 Direction Register	$002D_{16}$	
$000E_{16}$	Port P7	$002E_{16}$	
$000F_{16}$	Port P7 Direction Register	$002F_{16}$	
0010_{16}	Port P8	0030_{16}	
0011_{16}	Port P8 Direction Register	0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	AD/DA Control Register
0015_{16}		0035_{16}	A-D Conversion Register
0016_{16}		0036_{16}	D-A1 Conversion Register
0017_{16}		0037_{16}	D-A2 Conversion Register
0018_{16}	Transmit/Receive Buffer	0038_{16}	
0019_{16}	Serial I/O1 Status Register	0039_{16}	
$001A_{16}$	Serial I/O1 Control Register	$003A_{16}$	Interrupt Edge Selection Register
$001B_{16}$	UART Control Register	$003B_{16}$	CPU Mode Register
$001C_{16}$	Baud Rate Generator	$003C_{16}$	Interrupt Request Register 1
$001D_{16}$	Serial I/O2 Control Register	$003D_{16}$	Interrupt Request Register 2
$001E_{16}$		$003E_{16}$	Interrupt Control Register 1
$001F_{16}$	Serial I/O2 Register	$003F_{16}$	Interrupt Control Register 2

Fig. 2.3.2 Memory Map of Special Function Register (SFR)

2.3.2 RAM

The M38063M6-XXXFP/GP has a 512 X 8-bit static RAM from address 0040_{16} to $023F_{16}$. This internal RAM is used for data storage as well as stack area. When the RAM is used as stack area, the depth of subroutine nesting and the interrupt levels should be kept in mind in order to avoid overwriting the RAM contents.

2.3.3 ROM

The M38063M6-XXXFP/GP has a 24,446 X 8-bit mask programmable ROM from address $A000_{16}$ to $FFFF_{16}$. The 128 bytes from address $A000_{16}$ to address $A07F_{16}$ and addresses $FFFE_{16}$ and $FFFF_{16}$ are reserved for device testing, leaving 24,316 bytes of user ROM area.
Addresses $FFDC_{16}$ and $FFFD_{16}$ are allocated as a vector table for storing jump destination addresses used at reset or when an interrupt is generated. A memory map of the vector table is shown in Figure 2.3.3.

$FFDC_{16}$ $FFDD_{16}$	BRK Instruction Interrupt
$FFDE_{16}$ $FFDF_{16}$	A-D Conversion Interrupt
$FFE0_{16}$ $FFE1_{16}$	INT_4 Interrupt
$FFE2_{16}$ $FFE3_{16}$	INT_3 Interrupt
$FFE4_{16}$ $FFE5_{16}$	INT_2 Interrupt
$FFE6_{16}$ $FFE7_{16}$	Serial I/O2 Interrupt
$FFE8_{16}$ $FFE9_{16}$	$CNTR_1$ Interrupt
$FFEA_{16}$ $FFEB_{16}$	$CNTR_0$ Interrupt
$FFEC_{16}$ $FFED_{16}$	Timer 2 Interrupt

$FFEE_{16}$ $FFEF_{16}$	Timer 1 Interrupt
$FFF0_{16}$ $FFF1_{16}$	Timer X Interrupt
$FFF2_{16}$ $FFF3_{16}$	Timer Y Interrupt
$FFF4_{16}$ $FFF5_{16}$	Serial I/O1 Transmit Interrupt
$FFF6_{16}$ $FFF7_{16}$	Serial I/O1 Receive Interrupt
$FFF8_{16}$ $FFF9_{16}$	INT_1 Interrupt
$FFFA_{16}$ $FFFB_{16}$	INT_0 Interrupt
$FFFC_{16}$ $FFFD_{16}$	Reset

Fig. 2.3.3 Memory Map of Vector Area

2.4 Processor Mode and Input/Output Pins

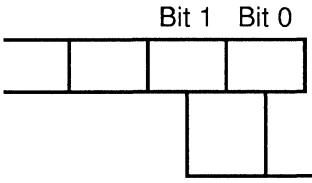
The level of the signal input to the CNVss pin of the M38063M6-XXXFP/GP can be used to control the chip's processor mode.

Three modes can be selected by changing the values of the processor mode bits (bits 0 and 1 of address $003B_{16}$) when the CNVss pin is connected to Vss.

The microcomputer will automatically be in single-chip mode when reset if the CNVss pin is connected to Vss. With the CNVss pin connected to Vss and the chip in single chip mode, memory expansion mode can be accessed by setting the processor mode bits to (0, 1) and microprocessor mode can be accessed by setting the processor mode bits to (1, 0).

The relationships between the values of the processor mode bits and the selected processor modes are shown in Table 2.4.1.

Table 2.4.1 Relationships between Processor Mode Bits and Processor Modes



CPU Mode Register (address $003B_{16}$)

Bit 1	Bit 0	Processor Mode Bit
0	0	Single-Chip Mode
0	1	Memory Expansion Mode
1	0	Microprocessor Mode
1	1	Do Not Use

If the system is reset with the CNVss pin connected to Vcc, the processor mode bits are automatically set to (1, 0), and the system will operate only in microprocessor mode.

2.4.1 Input/Output pins

(1) I/O ports

The M38063M6-XXXFP/GP has 72 programmable input/output pins arranged as ports P0 to P8. Of these ports, the functions of ports P0 to P3 depend on the processor mode, and ports P4 to P7 are double-function ports with program-selectable functions.

The circuits relating to these ports are shown in Figure 2.4.1, and the functions of these ports are listed in Table 2.4.2.

(2) Vss and Vcc pins

The Vss and Vcc pins supply power to the chip.

(3) CNVss pin

The level of signal input to the CNVss pin at reset start enables control of the chip's processor mode.

(4) XIN and XOUT pins

The XIN and XOUT pins are clock input and output pins. The M38063M6-XXXFP/GP has a built-in clock generation circuit whose oscillation frequency is set by a ceramic resonator or quartz crystal. However, an external clock can also be used by connecting the XIN pin to a clock generator and leaving the XOUT pin open.

(5) ϕ pin (also functions as $P3_4$ pin)

In memory expansion mode and microprocessor mode, the ϕ pin outputs the internal system clock (half the oscillation frequency of the resonator crystal connected between XIN and XOUT). When the STP or WIT instruction is executed, the output of the ϕ pin stops at a "H" level.

Table 2.4.2 Port Functions

Port P0	8-bit programmable I/O port Input/output format : CMOS	In modes other than single-chip, outputs the low-order address byte.
Port P1	8-bit programmable I/O port Input/output format : CMOS	In modes other than single-chip, outputs the high-order address byte.
Port P2	8-bit programmable I/O port Input/output format : CMOS	In modes other than single-chip, functions as the data bus.
Port P3	8-bit programmable I/O port Input/output format : CMOS	In modes other than single-chip, functions as the control bus.
Port P4	8-bit programmable I/O port Input/output format : CMOS	Not affected by processor mode. $P4_2$ to $P4_7$ are double-function pins with program-selectable functions.
Port P5	8-bit programmable I/O port Input/output format : CMOS	Not affected by processor mode. $P5_1$ to $P5_7$ are double-function pins with program-selectable functions.
Port P6	8-bit programmable I/O port Input/output format : CMOS	Not affected by processor mode. All pins are double-function pins with program-selectable functions.
Port P7	8-bit programmable I/O port Input format : CMOS Output format : N-channel open drain	Not affected by processor mode. $P7_0$ to $P7_3$ are double-function pins with program-selectable functions.
Port P8	8-bit programmable I/O port Input/output format : CMOS	Not affected by processor mode.

(6) SYNC pin (also functions as $P3_5$ pin)
In memory expansion mode and microprocessor mode, the SYNC pin outputs a signal that is "H" for one cycle of ϕ every time an opcode is fetched.

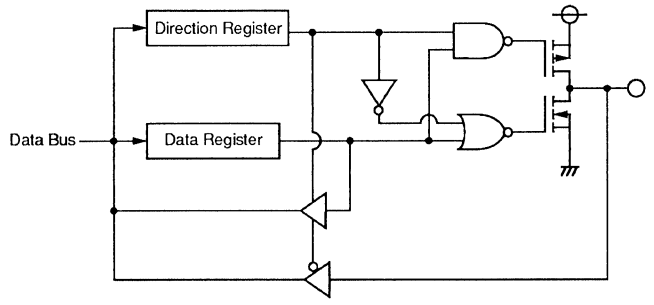
(7) $\overline{\text{RESET}}$ pin
The system is reset if the $\overline{\text{RESET}}$ pin is held "L" for at least 2μs before returning to "H".

(8) $\overline{\text{RESET}}_{\text{OUT}}$ pin (also functions as $P3_3$ pin)
When the M38063M6-XXXFP/GP is reset with the CNV_{SS} pin connected to V_{CC}, a "L" level signal is output from the $\overline{\text{RESET}}_{\text{OUT}}$ pin.

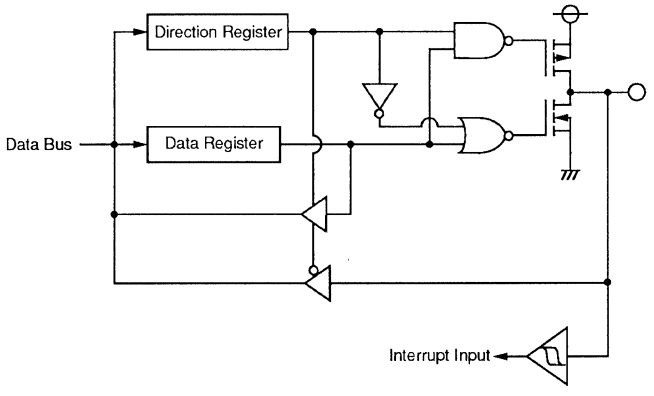
(9) $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins (also function as $P3_7$ and $P3_6$ pins)
A read control signal is output from the $\overline{\text{RD}}$ pin and a write control signal is output from the $\overline{\text{WR}}$ pin. A "L" from the $\overline{\text{RD}}$ pin indicates that the CPU is reading and a "L" from the $\overline{\text{WR}}$ pin indicates that the CPU is writing.
The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are output only in memory expansion mode and microprocessor mode.

(10) $\overline{\text{ONW}}$ pin (also functions as $P3_2$ pin)
When the CPU is either reading or writing, an "L" level input to this pin extends the corresponding read or write cycle by one cycle of ϕ. During this extended period, the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal remains "L".

Ports P0,P1,P2,P3,P4$_0$,P4$_1$,P5$_0$,P8



Ports P4$_2$,P4$_3$,P5$_1$,P5$_2$,P5$_3$



Port P4$_4$

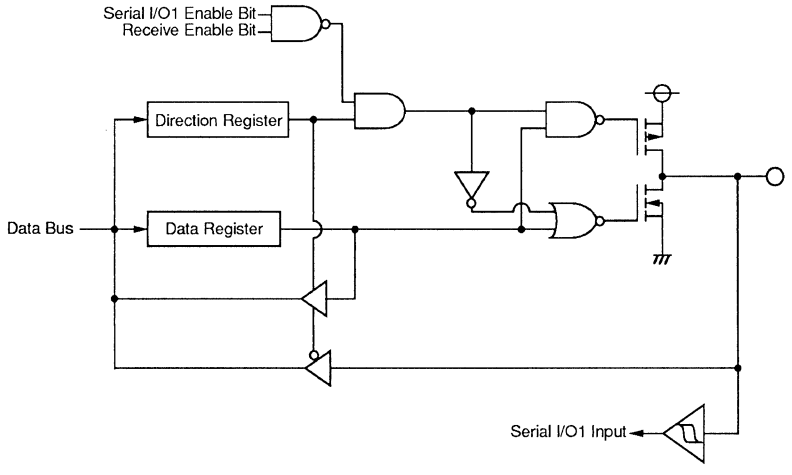


Fig. 2.4.1 Port Circuits (1)

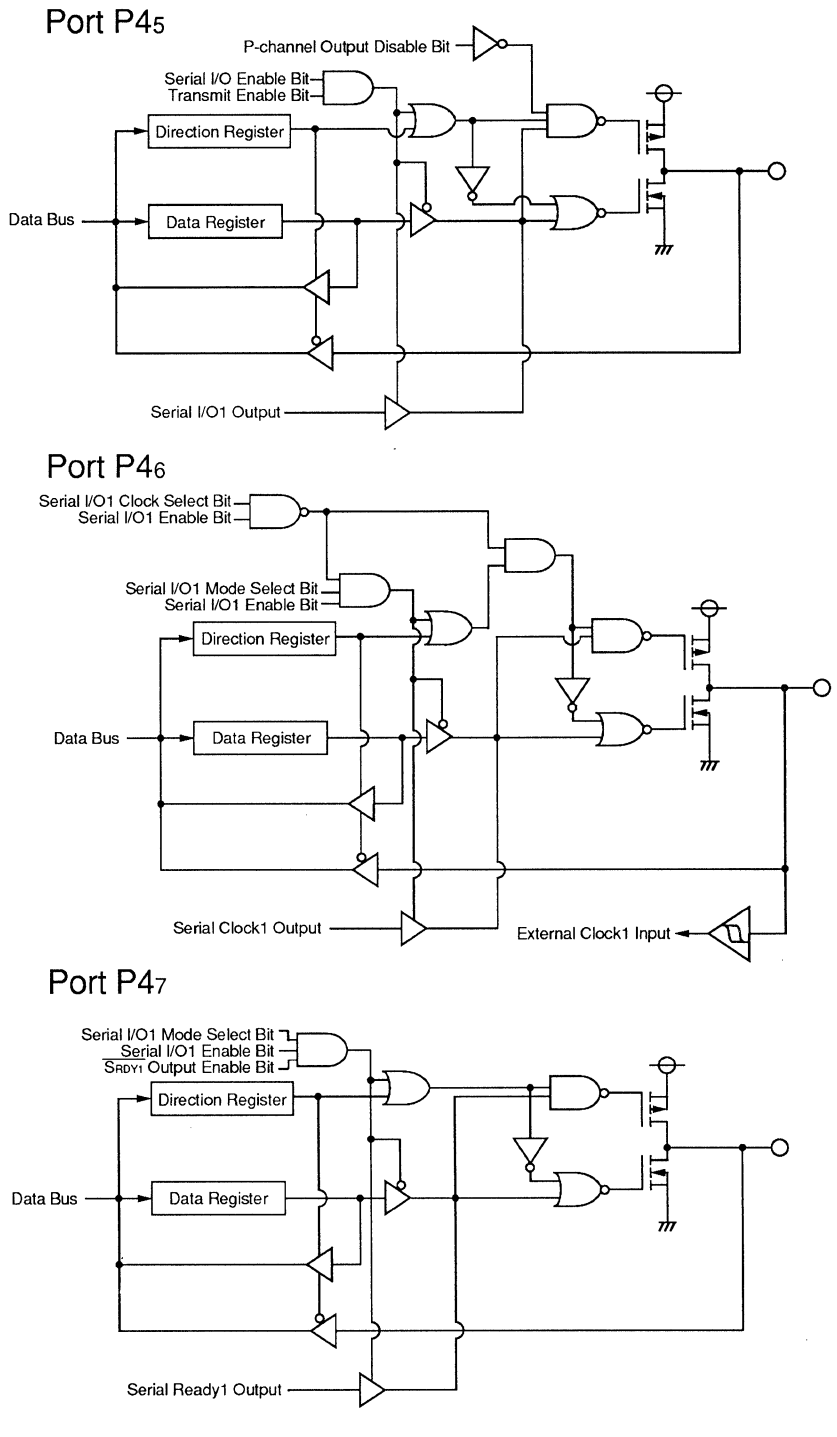
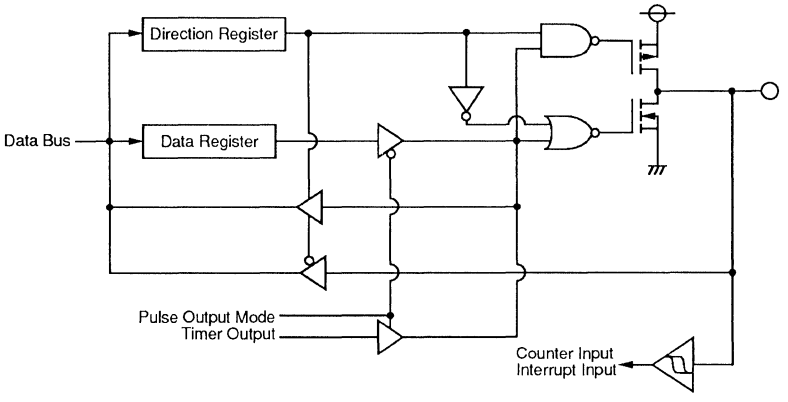
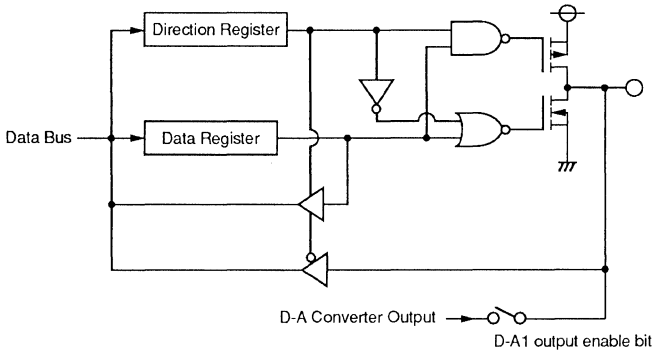


Fig. 2.4.1 Port Circuits (2)

Ports $P5_4$,$P5_5$



Port $P5_6$



Port $P5_7$

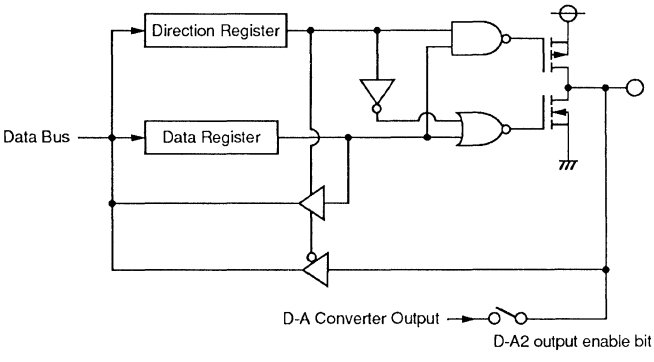
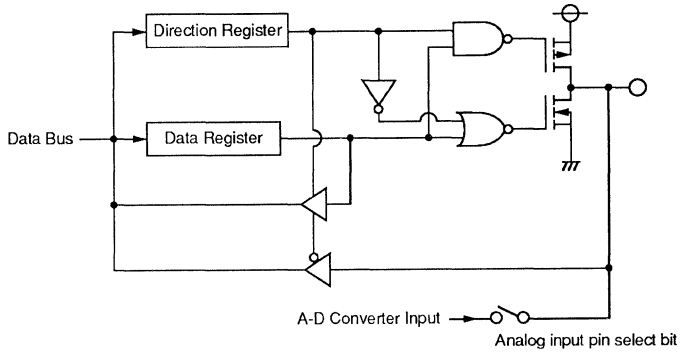
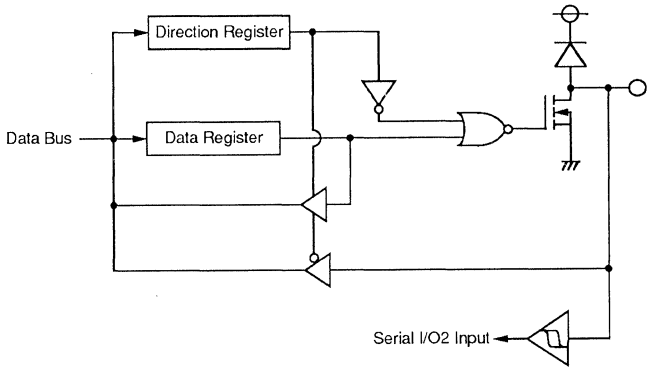


Fig. 2.4.1 Port Circuits (3)

Port P6



Port $P7_0$



Port $P7_1$

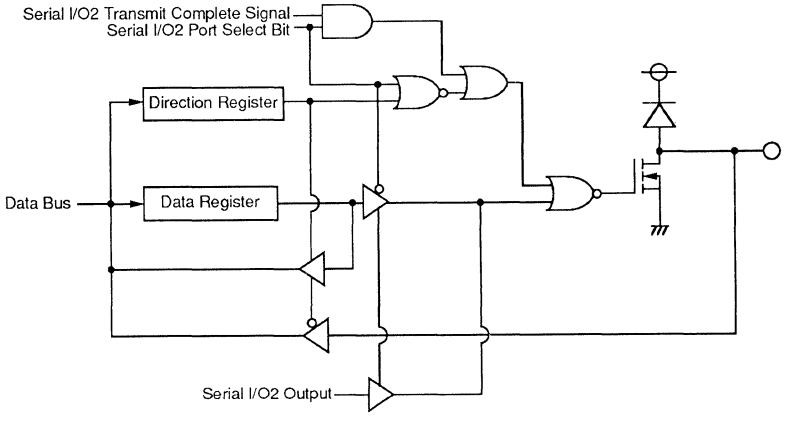
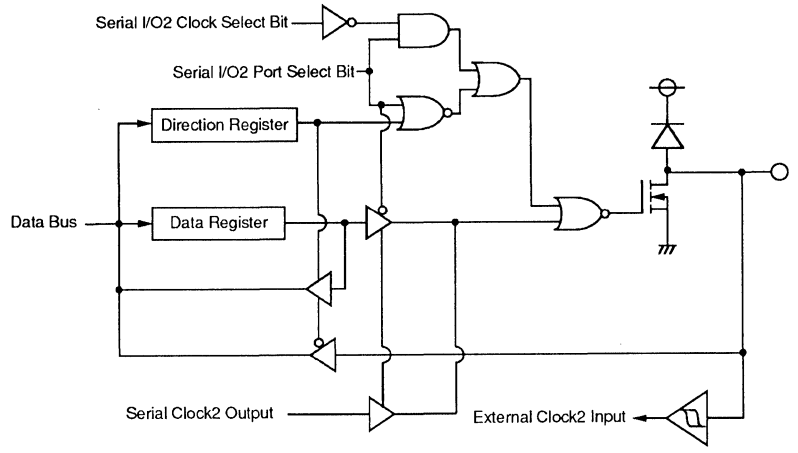
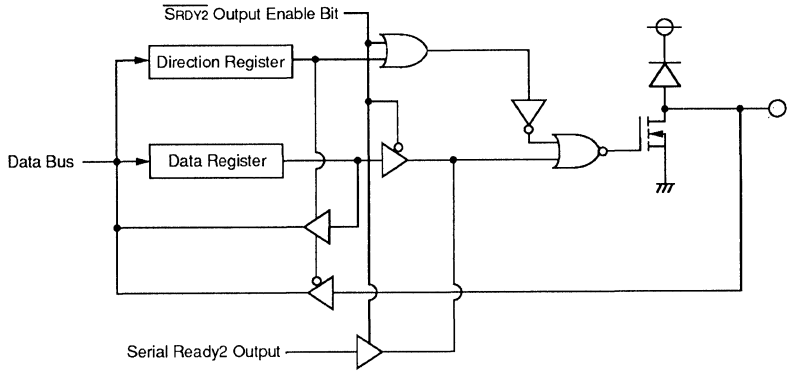


Fig. 2.4.1 Port Circuits (4)

Port $P7_2$



Port $P7_3$



Port $P7_4$~$P7_7$

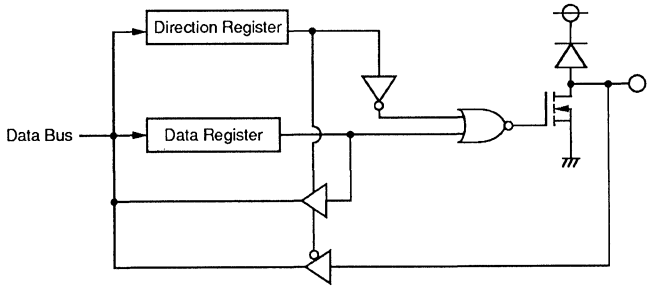
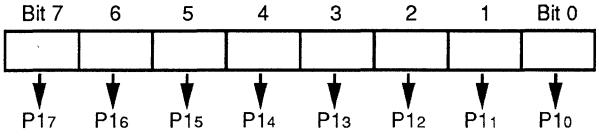


Fig. 2.4.1 Port Circuits (5)

2.4.2 Single-chip mode

The M38063M6-XXXFP/GP has 72 input/output pins. Of these pins, the 32 pins of ports P0 to P3 are affected by the processor mode.
In single-chip mode, all the ports function as input/output ports. Switch these ports between input and output as shown below.

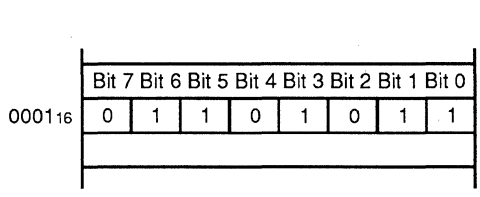
The registers that determine the input/output direction of the each ports are allocated to the SFR area (addresses 0000_{16} to $003F_{16}$) in the zero page. Therefore, the fastest way to write to these registers is to use the zero page addressing mode.
Each bit of a direction register corresponds to one pin, as shown below, and values can be written to each individual bit to switch the corresponding pin to either input or output.

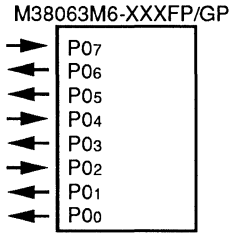


Port P1 direction register (address 0003_{16})

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin; when "1" is written to that bit, that pin becomes an output pin.
At reset, all the direction registers are initialized to "00_{16}", setting all of the input/output ports to input.

Example : If "$6B_{16}$" is written to the P0 direction register (address 0001_{16}):





Note that the direction registers should not be read. Do not use the set bit or clear bit commands on the direction registers, and do not try to use the direction registers for logical operations, arithmetic operations, condition judgements, or address calculations.

If data is read from a pin which is set for output, the value of the port latch is read, not the level of the pin itself. Even if an external load pulls down the voltage of an output from "H", or drives it up from "L", the output latch data is still read correctly.
Pins set to input are floating. If a pin which is set to input is written to, only the port latch is written to, and the pin itself remains floating.

2.4.3 Memory expansion mode

Use memory expansion mode if the internal memory, I/O, or related functions are found to be insufficient.

In this mode, use of the register area relating to ports P0 to P3 is disabled, but all of the other memory and related functions can be used.

Once memory expansion mode has been selected, the functions of ports P0 to P3 change as shown in Table 2.4.3.

Table 2.4.3 Port Functions in Memory Expansion Mode

Port name	Function
Port P0	Outputs low-order 8 bits of address
Port P1	Outputs high-order 8 bits of address
Port P2	Acts as input/output pins for data D_7 ~ D_0 (including instruction codes)
Port P3	$P3_0$ and $P3_1$ function as output pins (note that the port latch cannot be read) $P3_2$ is the $\overline{ONW}$ input pin $P3_3$ outputs "H" $P3_4$ outputs ϕ $P3_5$ outputs the $\overline{SYNC}$ signal $P3_6$ outputs the $\overline{WR}$ signal $P3_7$ outputs the $\overline{RD}$ signal

External memory can add addresses 0000_{16} to 0007_{16} and 0440_{16} to $9FFF_{16}$. If an address within the area 0008_{16} to $043F_{16}$ or $A000_{16}$ to $FFFF_{16}$ is read, the internal area is read. If an address within the area 0008_{16} to $043F_{16}$ or $A000_{16}$ to $FFFF_{16}$ is written to, the data is written to both internal and external areas.

2.4.4 Microprocessor mode

Microprocessor mode is basically the same as memory expansion mode, except that access to the internal ROM area is disabled and the $P3_3$ pin acts as the $\overline{RESET_{OUT}}$ output pin. Since external ROM can be freely added in this mode, it is useful for small production lots and for testing prototypes before mass production begins.

Memory allocations of modes other than single-chip mode are shown in Figure 2.4.2, and the functions of ports P0 ~ P3 in the different processor modes are shown in Figure 2.4.3.

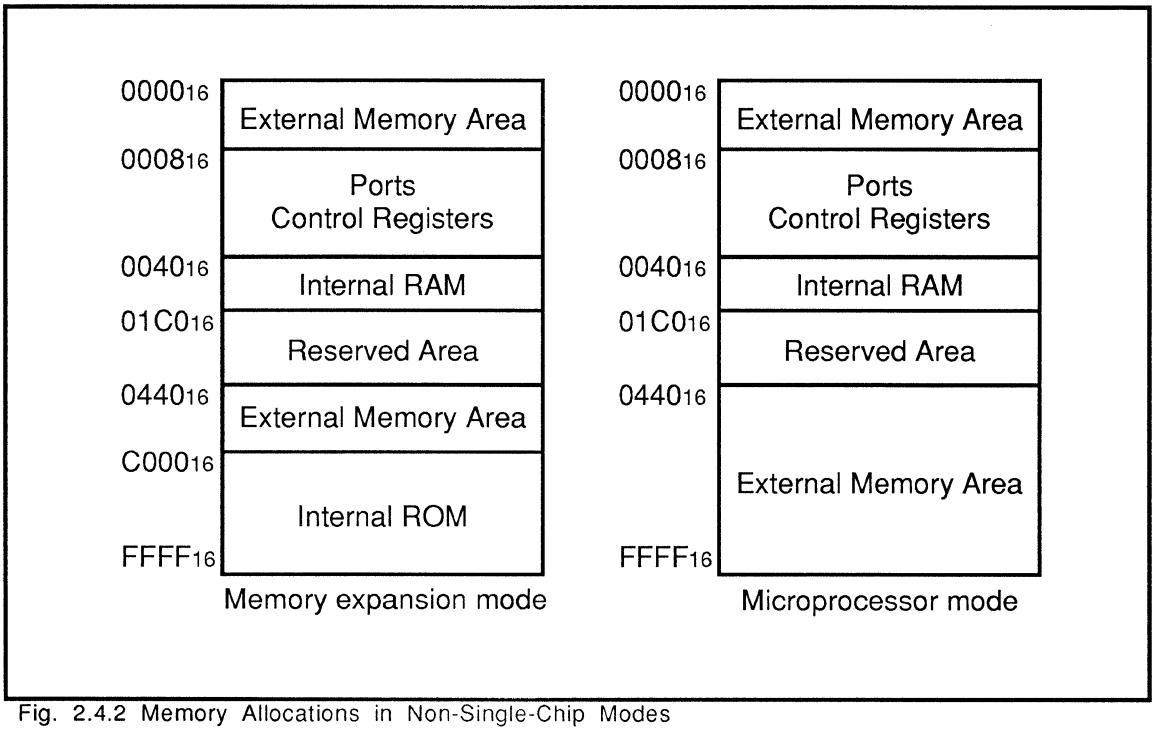


Fig. 2.4.2 Memory Allocations in Non-Single-Chip Modes

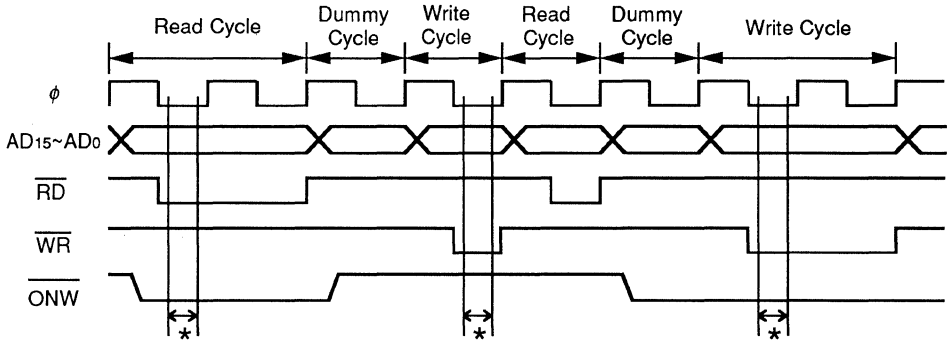
CM_1	0	1	0
CM_0	0	0	1
Mode / Port	Single-chip Mode	Microprocessor Mode	Memory Expansion Mode
Port P0	Internal φ Port $P0_7$~$P0_0$ I/O Port	Internal φ Port $P0_7$~$P0_0$ Address Output AD_7~AD_0	Same as left
Port P1	Internal φ Port $P1_7$~$P1_0$ I/O Port	Internal φ Port $P1_7$~$P1_0$ Address Output AD_{15}~AD_8	Same as left
Port P2	Internal φ Port $P2_7$~$P2_0$ I/O Port	Internal φ Port $P2_7$~$P2_0$ Data I/O DB_7~DB_0	Same as left
Port P3	Internal φ Port $P3_7$~$P3_0$ I/O Port	Internal φ Port $P3_4$ Port $P3_7$ $\overline{RD}$ Output Port $P3_6$ $\overline{WR}$ Output Port $P3_5$ SYNC Output Port $P3_2$ $\overline{ONW}$ Input Port $P3_3$ $\overline{RESET_{OUT}}$ Output Port $P3_1$,$P3_0$ Output Port (in case set for output)	Same as left except that $P3_3$ outputs "H"

Fig. 2.4.3 The Function of Ports P0~P3 in Each Processor Mode

2.4.5 Bus control with memory expansion

The M38063M6-XXXFP/GP has a built-in $\overline{ONW}$ function to ease access to the extra memory and I/O functions that are expanded in memory expansion mode or microprocessor mode.

If a "L" level signal is input to the $\overline{ONW}$ pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of ϕ. During this extended period, the $\overline{RD}$ or $\overline{WR}$ signal remains "L". This extension period is valid only when writing to and reading from addresses 0000_{16} to 0007_{16} and 0440_{16} to $FFFF_{16}$. Only read and write cycles are extended.

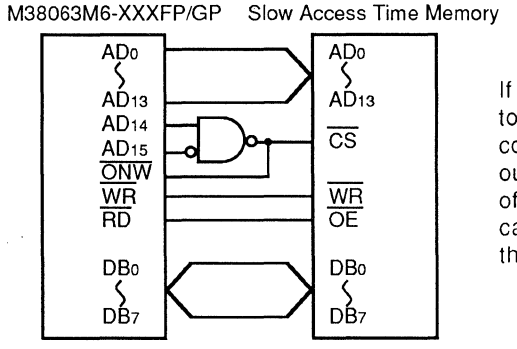


* : $\overline{ONW}$ Input Signal Acceptable Period

The ONW signal must be stably "H" or "L" during this period. In other periods, it does not matter whether the $\overline{ONW}$ signal input level is high or not.

Also note that when the address is at 0008_{16}~$043F_{16}$, the $\overline{ONW}$ signal is not accepted, and the bus cycle is not extended.

Fig. 2.4.4 $\overline{ONW}$ Function Timing



If a peripheral device with a slower access time is to be connected to the M38063M6-XXXFP/GP, connect the $\overline{ONW}$ pin to the address decoder output (active "L") of the device as a simple means of extending the bus cycle by one cycle. In this case, do not input the ϕ, $\overline{RD}$, and $\overline{WR}$ signals to the address decoder.

Fig. 2.4.5 Example of Circuit Using the $\overline{ONW}$ Function

2.5 Interrupts

Interrupts are used in the following cases:

- When a process which is more important than the currently executing process routine is requested.
- When a process must be executed at a specific time.

The M38063M6-XXXFP/GP can be interrupted by 16 sources. These interrupts are vectored interrupts with a fixed priority sequence. If two or more interrupts are requested in the same sampling period, the interrupt with the higher priority is accepted. The priority sequence is determined in hardware, but interrupts can be processed in a different order by using the interrupt request bits and interrupt disable flag.
Interrupt sources, interrupt vector addresses, and interrupt priorities are listed in Table 2.5.1.

Table 2.5.1 Interrupt Vector Addresses and Priorities

Priority	Interrupt source	Interrupt vector address		Remarks
		High-order byte	Low-order byte	
1	Reset (Note)	$FFFD_{16}$	$FFFC_{16}$	Non-maskable
2	INT_0 interrupt	$FFFB_{16}$	$FFFA_{16}$	External event interrupts (active edge selectable)
3	INT_1 interrupt	$FFF9_{16}$	$FFF8_{16}$	
4	Serial I/O1 receive interrupt	$FFF7_{16}$	$FFF6_{16}$	Valid only when serial I/O1 function is selected
5	Serial I/O1 transmit interrupt	$FFF5_{16}$	$FFF4_{16}$	
6	Timer X interrupt	$FFF3_{16}$	$FFF2_{16}$	
7	Timer Y interrupt	$FFF1_{16}$	$FFF0_{16}$	
8	Timer 1 interrupt	$FFEF_{16}$	$FFEE_{16}$	
9	Timer 2 interrupt	$FFED_{16}$	$FFEC_{16}$	
10	$CNTR_0$ interrupt	$FFEB_{16}$	$FFEA_{16}$	External event interrupts (active edge selectable)
11	$CNTR_1$ interrupt	$FFE9_{16}$	$FFE8_{16}$	
12	Serial I/O2 interrupt	$FFE7_{16}$	$FFE6_{16}$	
13	INT_2 interrupt	$FFE5_{16}$	$FFE4_{16}$	External event interrupts (active edge selectable)
14	INT_3 interrupt	$FFE3_{16}$	$FFE2_{16}$	
15	INT_4 interrupt	$FFE1_{16}$	$FFE0_{16}$	
16	A-D conversion interrupt	$FFDF_{16}$	$FFDE_{16}$	
17	BRK instruction interrupt	$FFDD_{16}$	$FFDC_{16}$	Non-maskable software interrupt

Note : Reset is included in this table because it functions in the same way as an interrupt.

2.5.1 Interrupt sources

The various interrupt sources are described below.

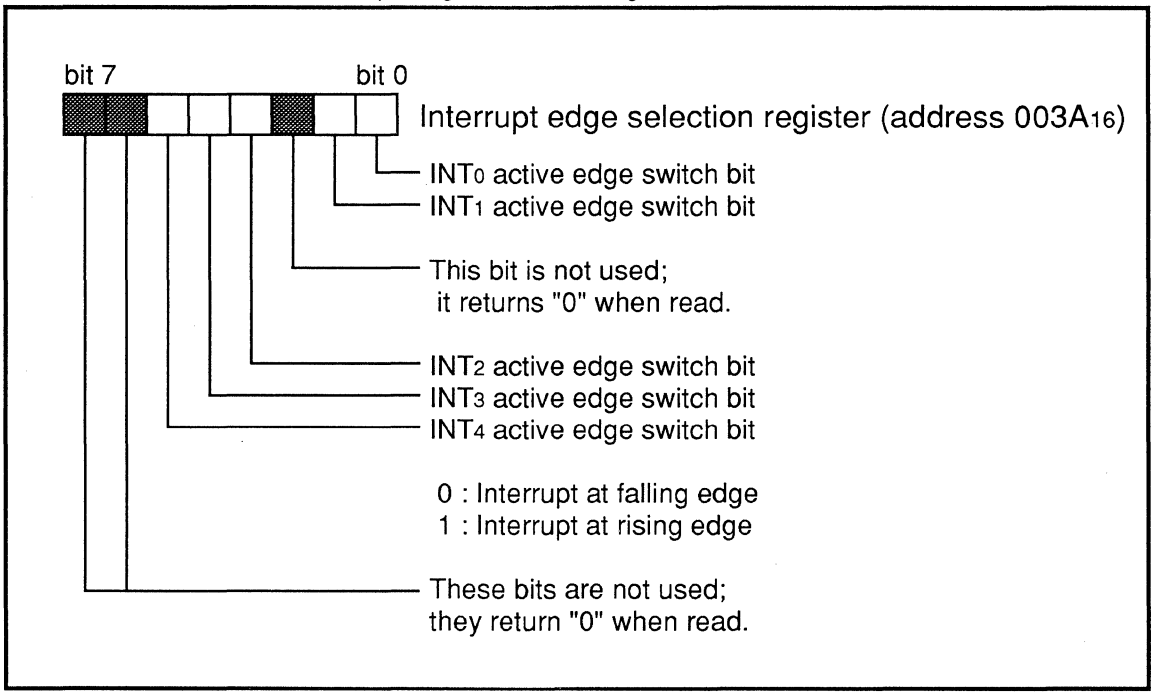
(1) INT_0, INT_1, INT_2, INT_3, and INT_4 interrupts

An interrupt request is generated when a level-transition from either "H" to "L" or from "L" to "H" is detected at the INT_0, INT_1, INT_2, INT_3, or INT_4 pin. The active edge can be selected by the corresponding bit (0, 1, 3, 4, and 5) of the interrupt edge selection register (address $003A_{16}$).

The interrupt edge selection register is cleared to "00_{16}" by a reset, so requests for INT_0, INT_1, INT_2, INT_3, and INT_4 interrupts are generated after a reset when falling edges are detected at the corresponding pins.

The INT_0, INT_1, INT_2, INT_3, and INT_4 pins also function as the $P4_2$, $P4_3$, and $P5_1$ ~ $P5_3$ pins. No special operation is necessary for selecting INT input pins; the edges at the $P4_2$, $P4_3$, and $P5_1$ ~ $P5_3$ pins are always detected.

Table 2.5.2 Structure of Interrupt Edge Selection Register



(2) Timer 1, timer 2, timer X, and timer Y interrupts

If the contents of timer 1, timer 2, timer X, or timer Y become "00_{16}", an interrupt request is generated when the next count pulse is input to that counter.

(3) $CNTR_0$ and $CNTR_1$ interrupts

An interrupt request is generated when a level-change from either "H" to "L" or from "L" to "H" of the $CNTR_0$ or $CNTR_1$ pin is detected. The active edge can be selected by the corresponding bit (2 and 6) of the timer XY mode register (address 0023_{16}).

The timer XY mode register is cleared to "00_{16}" by reset, so requests for $CNTR_0$ and $CNTR_1$ interrupts are generated after a reset when falling edges are detected at the corresponding pins.

The $CNTR_0$ and $CNTR_1$ pins also function as the $P5_4$ and $P5_5$ pins. No special operation is necessary for selecting CNTR input pins; the edges at the $P5_4$ and $P5_5$ pins are always detected.

(4) Serial I/O1 receive interrupt
When data has all arrived in the receive shift register, and the contents of the shift register are transferred to the receive buffer, an interrupt request is generated.
Receive interrupts are valid only when the serial I/O1 function is enabled.

(5) Serial I/O1 transmit interrupt
The timing at which a transmit interrupt request is generated can be selected by the transmit interrupt source select bit (TIC), bit 3 of the serial I/O1 control register (address $001A_{16}$).
Transmit interrupts are valid only when the serial I/O1 function is enabled.
Note that transmit enable status (transmit buffer empty, transmit shift completed) bits are set if the transmit enable bit is set to enable, so an interrupt request is generated without regard to the TIC bit.

Table 2.5.3 Selection of Interrupt Source by TIC

TIC	Interrupt source
"0"	An interrupt request is generated when data written to the transmit buffer is transferred to the transmit shift buffer, and the transmit buffer becomes empty
"1"	An interrupt request is generated when the shift operation of the transmit shift register is completed

(6) Serial I/O2 interrupt
An interrupt request is generated at the same time that the contents of the serial I/O counter 2 reach "0".

(7) A-D conversion interrupt
An interrupt request is generated at the same time that A-D conversion is completed.

(8) BRK instruction interrupt
The BRK interrupt has the lowest priority of software interrupts; it does not have a corresponding interrupt enable bit and the interrupt disable flag has no effect on it (it is non-maskable).

For further details of the various interrupts, see the sections on the corresponding functions.

Table 2.5.4 Structure of Timer XY Mode Register

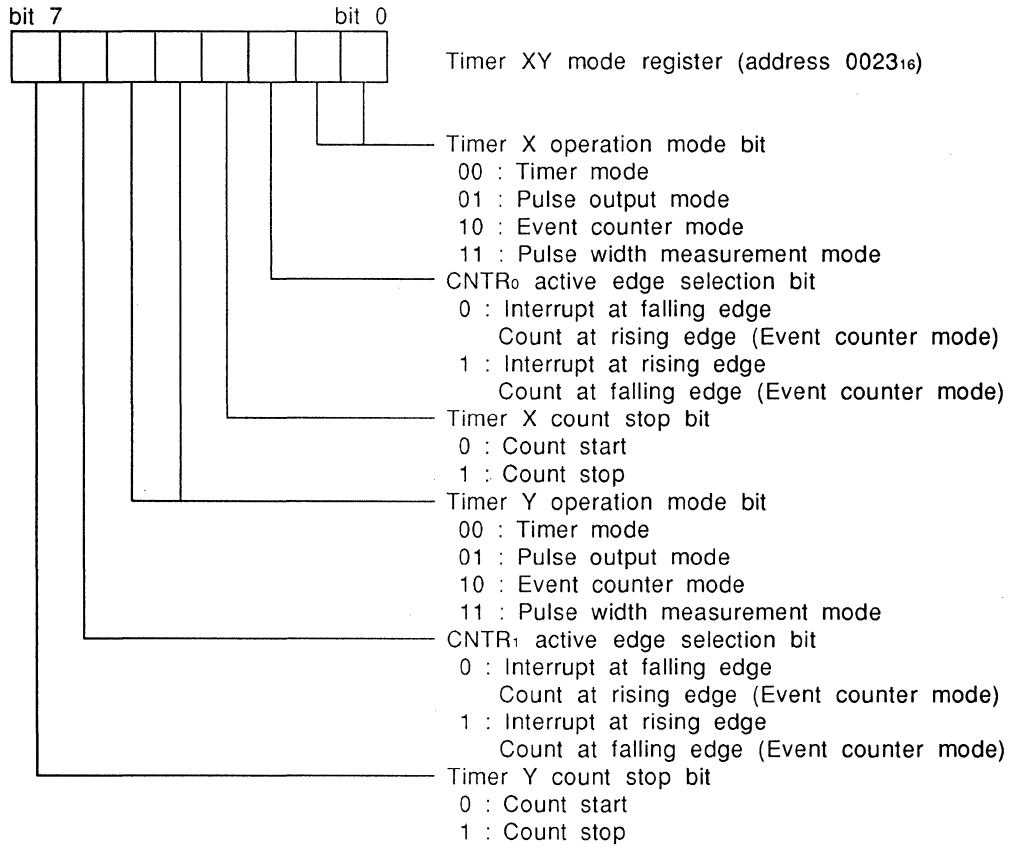
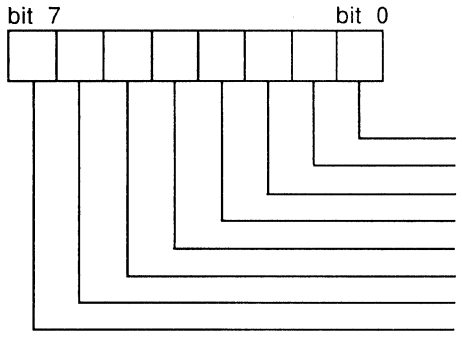
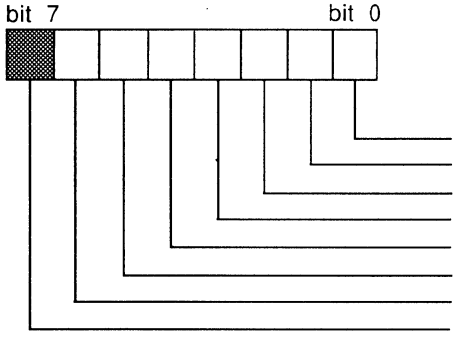


Table 2.5.5 Structure of Interrupt Request Registers



Interrupt request register 1 (address $003C_{16}$)

INT_0 interrupt request bit
INT_1 interrupt request bit
Serial I/O1 receive interrupt request bit
Serial I/O1 transmit interrupt request bit
Timer X interrupt request bit
Timer Y interrupt request bit
Timer 1 interrupt request bit
Timer 2 interrupt request bit

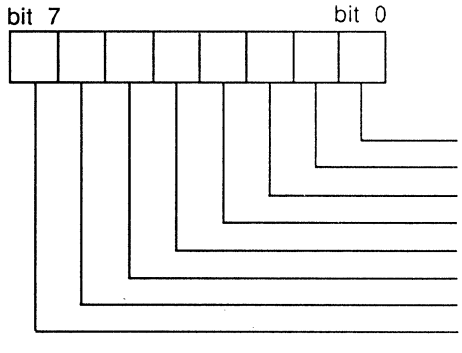


Interrupt request register 2 (address $003D_{16}$)

$CNTR_0$ interrupt request bit
$CNTR_1$ interrupt request bit
Serial I/O2 interrupt request bit
INT_2 interrupt request bit
INT_3 interrupt request bit
INT_4 interrupt request bit
A-D conversion interrupt request bit
This bit is not used; it returns "0" when read.

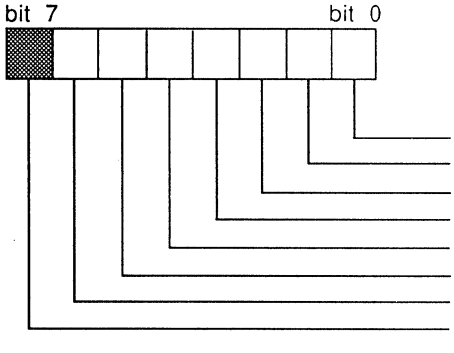
0 : No interrupt request issued
1 : Interrupt request issued

Table 2.5.6 Structure of Interrupt Control Registers



Interrupt control register 1 (address $003E_{16}$)

INT_0 interrupt enable bit
INT_1 interrupt enable bit
Serial I/O1 receive interrupt enable bit
Serial I/O1 transmit interrupt enable bit
Timer X interrupt enable bit
Timer Y interrupt enable bit
Timer 1 interrupt enable bit
Timer 2 interrupt enable bit



Interrupt control register 2 (address $003F_{16}$)

$CNTR_0$ interrupt enable bit
$CNTR_1$ interrupt enable bit
Serial I/O2 interrupt enable bit
INT_2 interrupt enable bit
INT_3 interrupt enable bit
INT_4 interrupt enable bit
A-D conversion interrupt enable bit
This bit is not used; it returns "0" when read. Do not write "1" to this bit.

0 : Interrupt disabled
1 : Interrupt enabled

2.5.2 Interrupt control

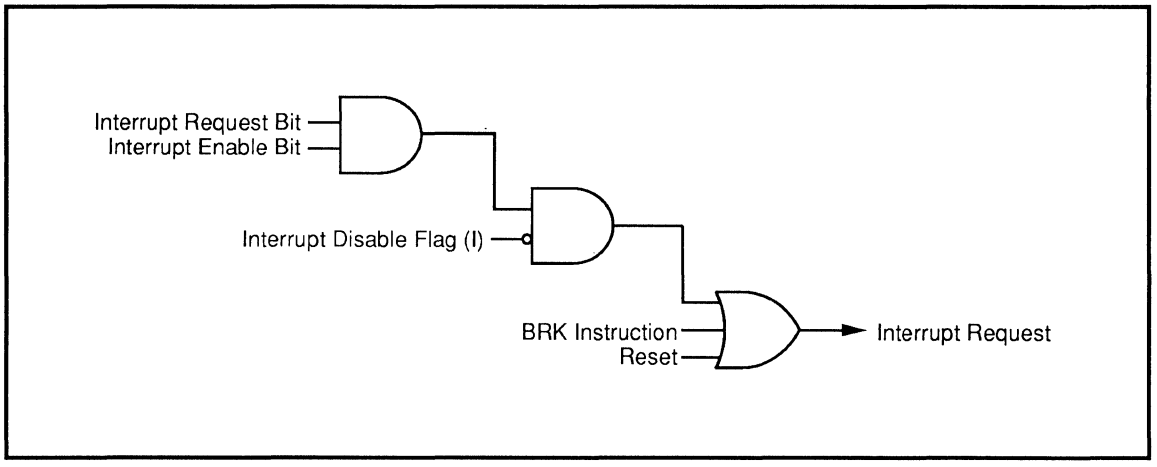


Fig. 2.5.1 Interrupt Control

Each interrupt is controlled by its interrupt request bit, its interrupt enable bit, and the interrupt disable flag, as shown in Figure 2.5.1, except for the software interrupt set by the BRK instruction. The control bits and the control flag are independent. An interrupt is generated when the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

(1) Interrupt request bits
The interrupt request bits are located in interrupt request registers 1 and 2 (addresses $003C_{16}$ and $003D_{16}$).
When an interrupt is generated, the request bit corresponding to that interrupt is set to "1". The interrupt request bit remains set until the time that the interrupt is serviced. They can be cleared in software as well. These bits cannot be set by software.

(2) Interrupt enable bits
The interrupt enable bits are located in interrupt control registers 1 and 2 (addresses $003E_{16}$ and $003F_{16}$).
These bits control the acceptance of interrupts. When the bit corresponding to an interrupt is "0", the acceptance of that interrupt is disabled; when the bit is "1", the corresponding interrupt is enabled.

(3) Interrupt disable flag (I)
The I flag is allocated to bit 2 of the processor status register. This flag disables all interrupts except the BRK instruction interrupt.
When the interrupt disable flag is set to "1", interrupts are disabled; when it is cleared to "0", interrupts are enabled. Use the SEI instruction to set the interrupt disable flag, and the CLI instruction to clear it.
Once the interrupt service routine has started, the I flag is automatically set and concurrent interrupts are disabled. In order to allow multiple interrupts, this flag must be cleared by the CLI instruction within the interrupt service routine.

2.5.3 Interrupt sequence

When an interrupt is received, the currently executing process is temporarily halted and the appropriate interrupt service routine is executed. Before an interrupt service routine can be executed, a jump destination address must be set in the vector table to correspond to the interrupt. After the interrupt service routine ends, the program flow must allow the previous process to continue.

When the M38063M6-XXXFP/GP accepts an interrupt, it automatically pushes the high-order bits of the program counter, the low-order bits of the program counter, and the contents of the processor status register onto the stack. (A push consists of storing data in the stack address and decrementing the stack pointer.) Interrupt inhibit flag I is set and the program counter is set to the address specified in the vector table. The corresponding interrupt request flag is cleared automatically.

Figure 2.5.2 shows the changes in the stack pointer and program counter when an interrupt is serviced.

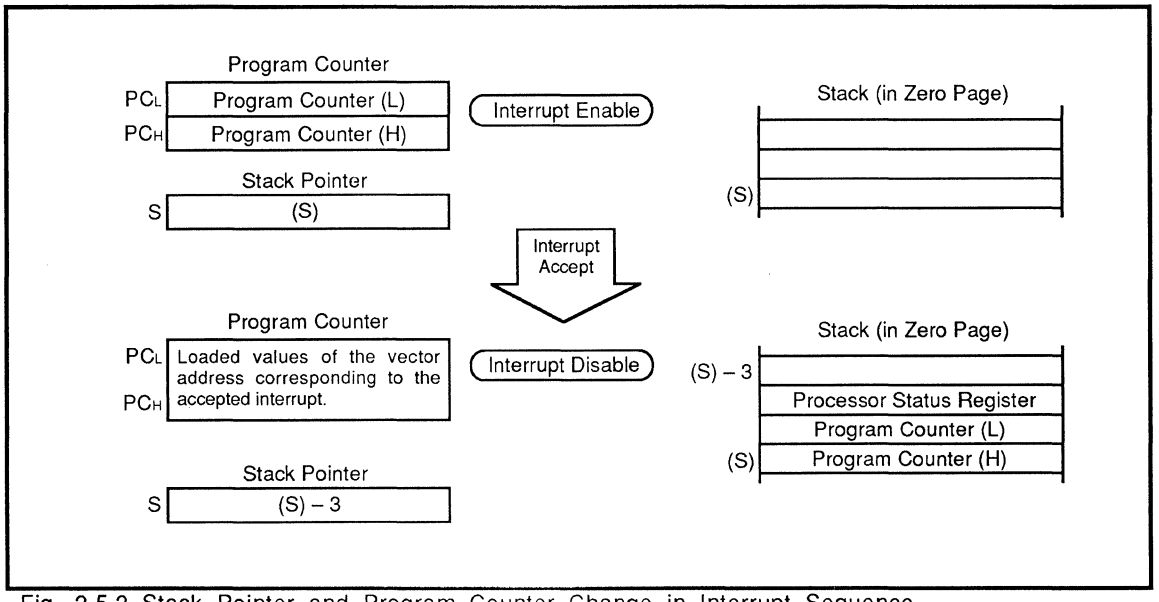
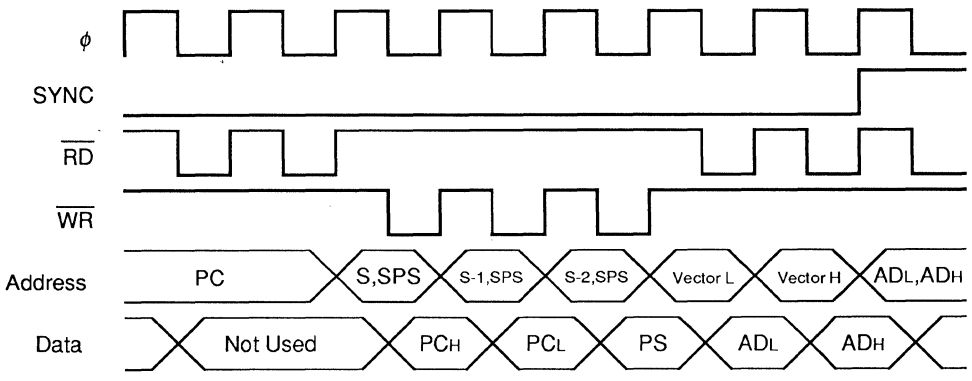


Fig. 2.5.2 Stack Pointer and Program Counter Change in Interrupt Sequence

2.5.4 Timing after interrupt

An interrupt service routine starts at the machine cycle following the end of the currently executing instruction.

The timing after an interrupt is accepted and is serviced is shown in Figure 2.5.3, and the time until the interrupt service routine starts is shown in Figure 2.5.4.



Note: Vector L and vector H are the addresses where the jump destination is stored, and ADL and ADH are the values of those addresses. For details of jump destination addresses, see Table 2.5.1.

Fig. 2.5.3 Timing after Interrupt

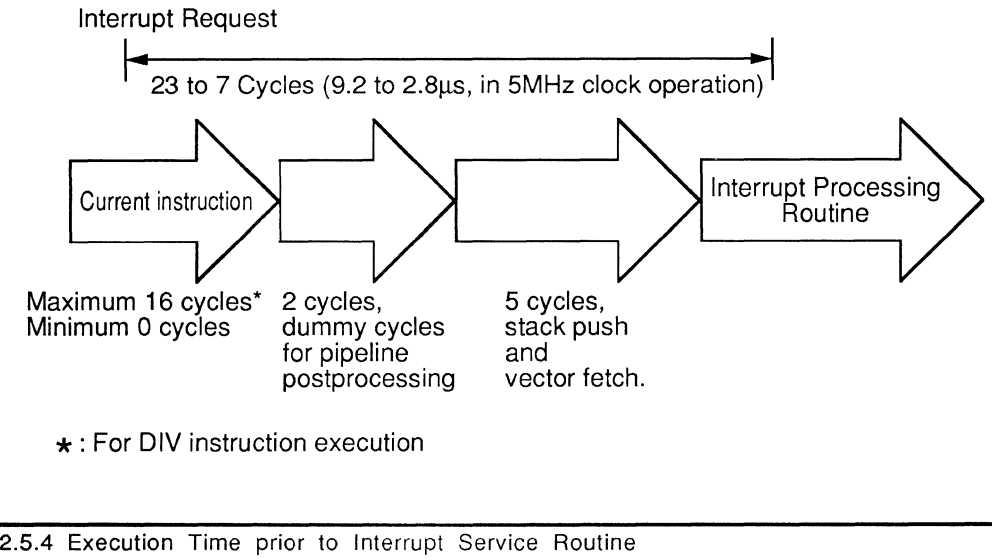


Fig. 2.5.4 Execution Time prior to Interrupt Service Routine

2.6 Timers

The M38063M6-XXXFP/GP has four built-in timers: timer X, timer Y, timer 1, and timer 2. A block diagram of these timers is shown in Figure 2.6.1.

2.6.1 Timer blocks

Each timer has an 8-bit timer latch, and each of the prescalers has an 8-bit prescaler latch. Divide ratios can be determined by the contents of a latch. Timer 1 and timer 2 share a prescaler. The timers and prescalers can be written to and read from at any time.

(1) Timer X

Timer X can be set to any of the four modes listed below by setting the timer X mode bits (bit 0 and bit 1) of the timer XY mode register (address 0023_{16}). If the timer X count stop bit (bit 3) of the timer XY mode register is set to "1", timer X's count stops in all four modes.

- Timer mode
- Pulse output mode
- Event counter mode
- Pulse width measurement mode

(2) Timer Y

Timer Y can be set to any of the four modes listed below by setting the timer Y mode bits (bit 4 and bit 5) of the timer XY mode register. If the timer Y count stop bit (bit 7) of the timer XY mode register is set to "1", timer Y's count stops in all four modes.

- Timer mode
- Pulse output mode
- Event counter mode
- Pulse width measurement mode

(3) Timer 1, timer 2

Timer 1 and timer 2 can only be used in timer mode.

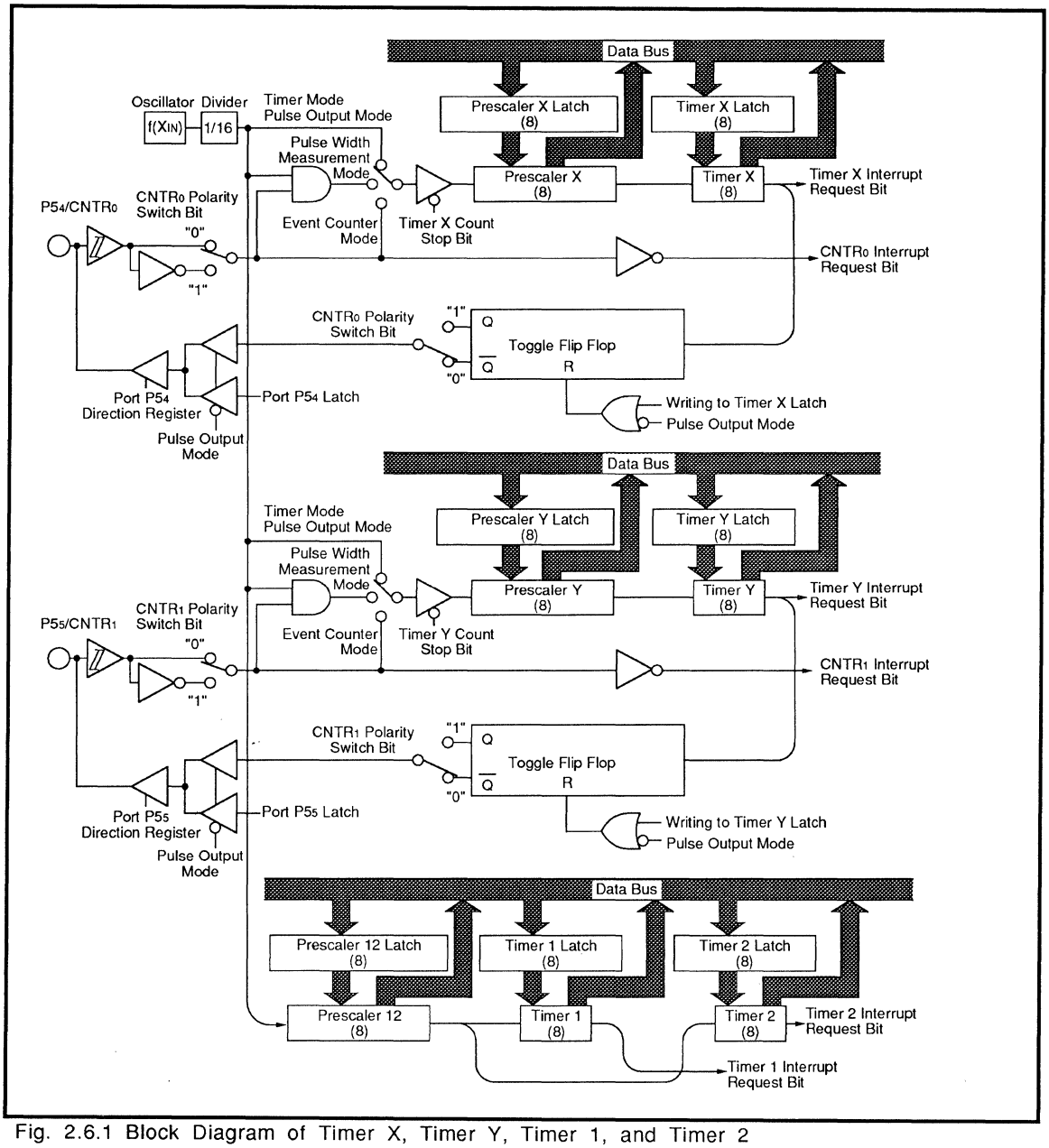
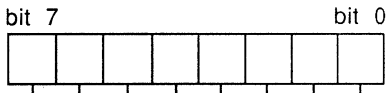


Fig. 2.6.1 Block Diagram of Timer X, Timer Y, Timer 1, and Timer 2

Table 2.6.1 Structure of Timer XY Mode Register



Timer XY mode register (address 0023_{16})

Timer X operation mode bit
00 : Timer mode
01 : Pulse output mode
10 : Event counter mode
11 : Pulse width measurement mode

$CNTR_0$ active edge selection bit
0 : Interrupt at falling edge
Count at rising edge (Event counter mode)
1 : Interrupt at rising edge
Count at falling edge (Event counter mode)

Timer X count stop bit
0 : Count start
1 : Count stop

Timer Y operation mode bit
00 : Timer mode
01 : Pulse output mode
10 : Event counter mode
11 : Pulse width measurement mode

$CNTR_1$ active edge selection bit
0 : Interrupt at falling edge
Count at rising edge (Event counter mode)
1 : Interrupt at rising edge
Count at falling edge (Event counter mode)

Timer Y count stop bit
0 : Count start
1 : Count stop

Note : At reset, the timer XY mode register is cleared to "00_{16}".

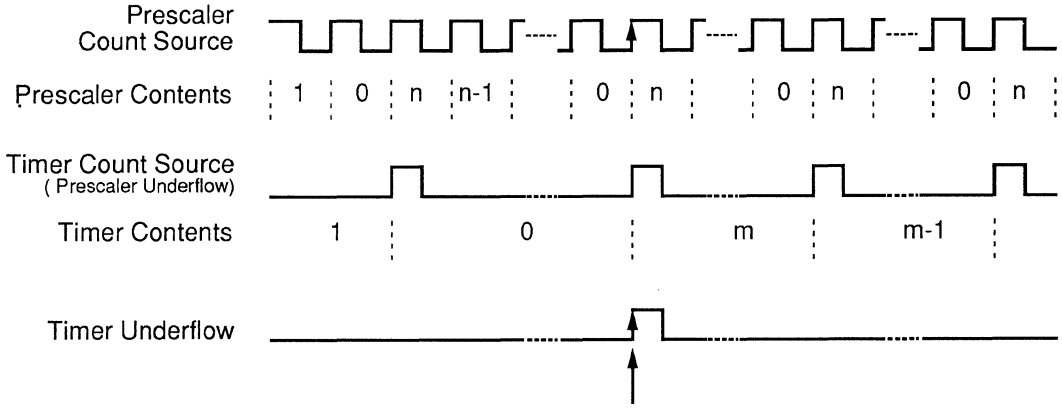
2.6.2 Timer operation

The timers all count down. When a timer underflows (the count pulse after the timer reaches "00_{16}") the contents of the corresponding timer latch are reloaded into the timer and the interrupt request bit is set. Addresses and initial timer and prescaler values after reset is shown in Table 2.6.2. A value written into a timer or prescaler is written simultaneously into both the latch and the counter. When a value is read from a timer or prescaler, the value in the counter at the time of the read is returned. The divide ratio of a timer or prescaler is given by 1/(n+1), where n is the value of the timer or prescaler (n = 0 ~ 255).

When the STP instruction is executed, "01_{16}" is written to timer 1 and the timer 1 latch, and "FF_{16}" is written to prescaler 12 and the prescaler 12 latch.

Table 2.6.2 Timer and Prescaler Memory Map and Initial Values after Reset

Prescaler	Address	Initial value	Timer	Address	Initial value
Prescaler X	0024_{16}	FF_{16}	Timer X	0025_{16}	FF_{16}
Prescaler Y	0026_{16}	FF_{16}	Timer Y	0027_{16}	FF_{16}
Prescaler 12	0020_{16}	FF_{16}	Timer 1	0021_{16}	01_{16}
			Timer 2	0022_{16}	FF_{16}



n : Value set in prescaler and prescaler latch.
m : Value set in timer and timer latch.

Fig. 2.6.2 Prescaler and Timer Count Operations

2.6.3 Timer mode

(1) Count source

The count is based on the oscillation frequency divided by 16.

(2) Operation

Each time a timer underflows, the corresponding timer interrupt request bit is set to "1", the contents of the timer latch are loaded into the timer, and the count continues.

2.6.4 Pulse output mode

(1) Count source

The count is based on the oscillation frequency divided by 16.

(2) Operation

Each time a timer underflows, the output of the $CNTR_0$ (or $CNTR_1$) pin is inverted, the corresponding timer interrupt request bit is set to "1", the contents of the timer latch are loaded into the timer, and the count continues. In this way, a square wave with a 50% duty ratio is output from the $CNTR_0$ (or $CNTR_1$) pin.

(3) Output pins

- Timer X : $CNTR_0$ pin
- Timer Y : $CNTR_1$ pin

(4) Initial values of output

Timer	Selection bit	Initial output value
Timer X	$CNTR_0$ active edge selection bit	0 : Initial value "H"
Timer Y	$CNTR_1$ active edge selection bit	1 : Initial value "L"

(5) Notes on use

1. When using pulse output mode, set the bit corresponding to $P5_4$ ($CNTR_0$) or $P5_5$ ($CNTR_1$) in the port P5 direction register (bit 4 or bit 5 of address $000B_{16}$) to "1" (output status).
2. If the bit corresponding to $P5_4$ ($CNTR_0$) or $P5_5$ ($CNTR_1$) in the port P5 register (bit 4 or bit 5 of address $000A_{16}$) is read while pulse output mode is being used, the current output value is read, not the contents of the data register.

2.6.5 Event counter mode

(1) Count source

- Timer X : Input from $CNTR_0$ pin
- Timer Y : Input from $CNTR_1$ pin

(2) Operation

Each time a timer underflows, the corresponding timer interrupt request bit is set to "1", the contents of the timer latch are loaded into the timer, and the count continues.

Timer	Selection bit	Operation
Timer X	$CNTR_0$ active edge selection bit	0 : Count at rising edge of input from $CNTR_0$ pin
		1 : Count at falling edge of input from $CNTR_0$ pin
Timer Y	$CNTR_1$ active edge selection bit	0 : Count at rising edge of input from $CNTR_1$ pin
		1 : Count at falling edge of input from $CNTR_1$ pin

(3) Note on use

When using event counter mode, set the bit corresponding to $P5_4$ ($CNTR_0$) or $P5_5$ ($CNTR_1$) in the port P5 direction register (bit 4 or bit 5 of address $000B_{16}$) to "0" (input status).

2.6.6 Pulse width measurement mode

(1) Count source

The count is based on the oscillation frequency divided by 16.

(2) Operation

• When the $CNTR_0$ ($CNTR_1$) active edge selection bit is "0":

While the input level of the $CNTR_0$ ($CNTR_1$) pin is "H", the count source is counted. When the input level of the $CNTR_0$ ($CNTR_1$) pin changes from "H" to "L", the timer stops counting and a $CNTR_0$ ($CNTR_1$) interrupt request is generated. When the input level of the $CNTR_0$ ($CNTR_1$) pin returns to "H", the count restarts.

• When the $CNTR_0$ ($CNTR_1$) active edge selection bit is "1":

While the input level of the $CNTR_0$ ($CNTR_1$) pin is "L", the count source is counted. When the input level of the $CNTR_0$ ($CNTR_1$) pin changes from "L" to "H", the timer stops counting and a $CNTR_0$ ($CNTR_1$) interrupt request is generated. When the input level of the $CNTR_0$ ($CNTR_1$) pin returns to "L", the count restarts.

Each time a timer underflows, the corresponding timer interrupt request bit is set to "1", the contents of the timer latch are loaded into the timer, and the count continues.

(3) Measurement pins

• Timer X : $CNTR_0$ pin

• Timer Y : $CNTR_1$ pin

(4) Levels of measurement pins

Timer	Selection bit	Pin level
Timer X	$CNTR_0$ active edge selection bit	0 : "H" level
Timer Y	$CNTR_1$ active edge selection bit	1 : "L" level

(5) Notes on use

1. When using pulse width measurement mode, set the bit corresponding to $P5_4$($CNTR_0$) or $P5_5$ ($CNTR_1$) in the port P5 direction register (bit 4 or bit 5 of address $000B_{16}$) to "0" (input status).
2. If the value of the $P5_4$ or $P5_5$ pin is set as an input pin, it is read normally without regard to the value of the $CNTR_0$ ($CNTR_1$) active edge switch bit.

2.7 Serial I/O1

In the M38063M6-XXXFP/GP, the user can select either clock synchronous or asynchronous (UART) serial I/O for the serial I/O1 function. The two methods are described in sequence below.

2.7.1 Clock synchronous serial I/O1

Select clock synchronous serial I/O mode by setting the serial I/O1 mode select bit of the serial I/O1 control register (bit 6 of address $001A_{16}$) to "1" (see Table 2.7.1). The clock synchronous serial I/O1 function is outlined below.

- Transfer method
  Either half duplex or full duplex data transfer can be selected.
- Synchronization clock
  Either the internal clock or an external clock can be selected by setting the serial I/O1 synchronization clock select bit (bit 1) of the serial I/O1 control register.

Synchronization clock
- Internal clock (when serial I/O1 synchronization clock select bit is "0")
  The clock is the BRG output divided by four.
- External clock (when serial I/O1 synchronization clock select bit is "1")
  An external clock input from the S_{CLK1} pin is selected (max. 1.25MHz).

A block diagram of the clock synchronous serial I/O1 function is shown in Figure 2.7.1, and the individual blocks are described below.

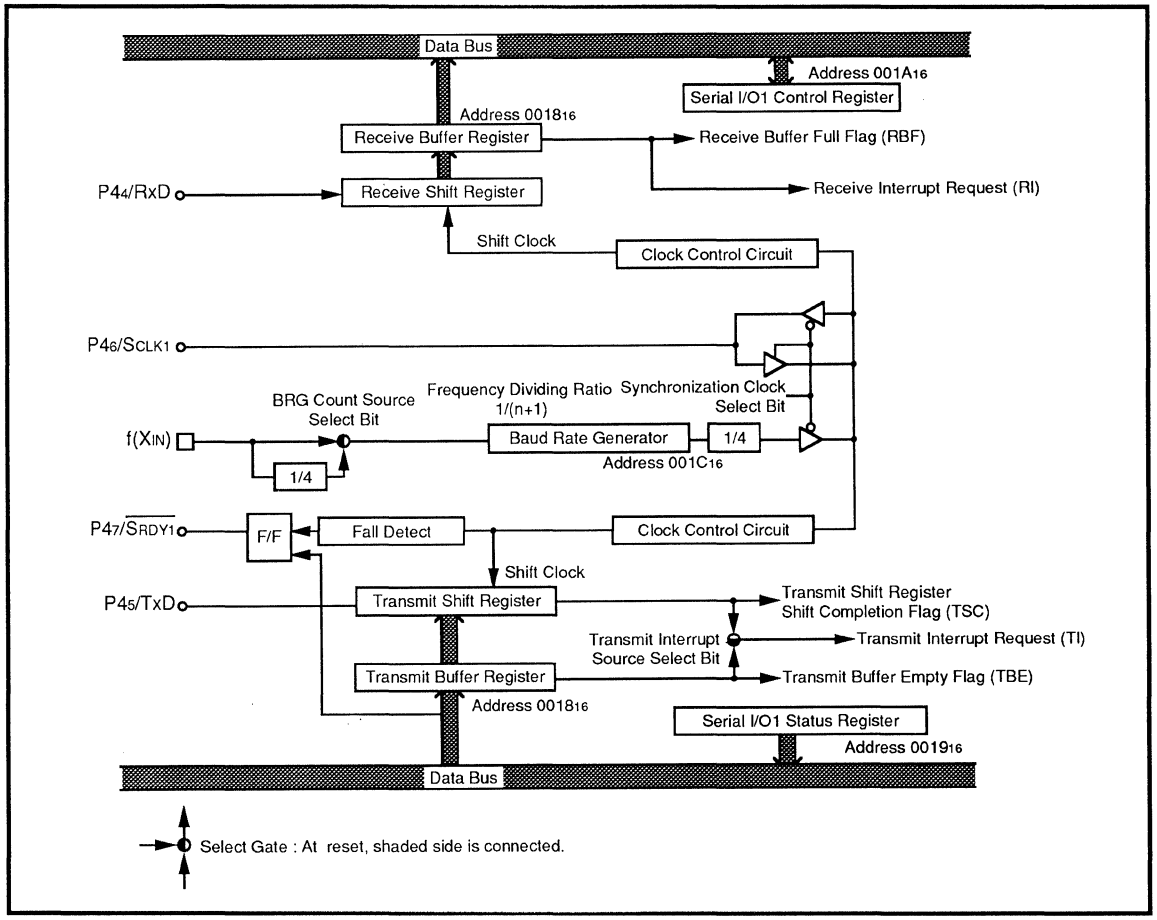


Fig. 2.7.1 Block Diagram of Clock Synchronous Serial I/O1 Function

(1) Baud rate generator (BRG) (address $001C_{16}$)

The BRG is a dedicated 8-bit timer used as a baud rate generator for the serial I/O1 function. When the internal clock is selected as the synchronization clock, the shift clock is the BRG output divided by four. A block diagram of the BRG is shown in Figure 2.7.2.

Note that the clock input to the BRG can be selected by setting the BRG count source select bit of the serial I/O1 control register.

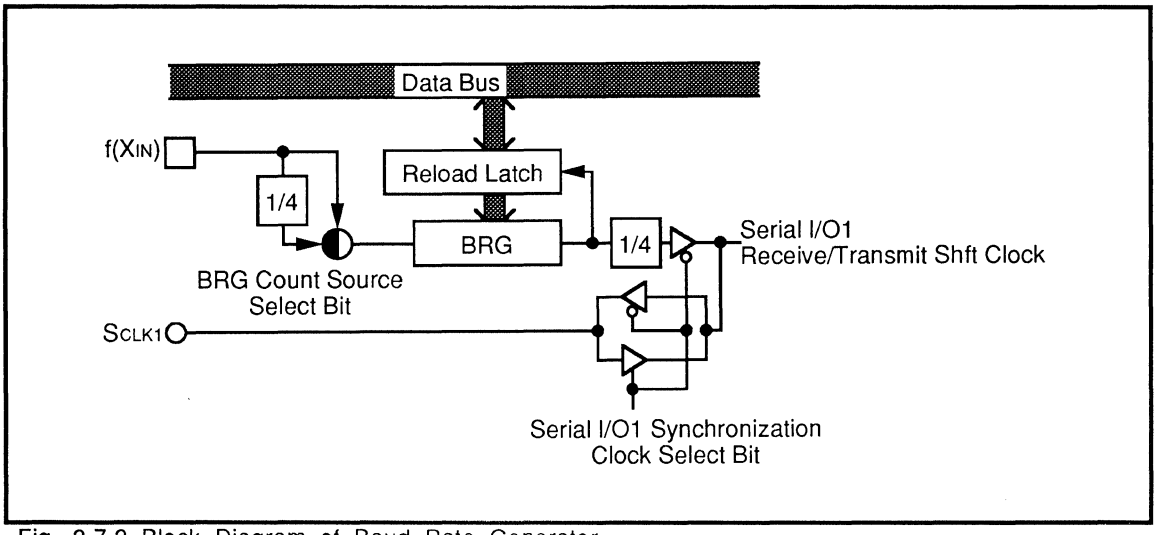


Fig. 2.7.2 Block Diagram of Baud Rate Generator

(2) Serial I/O1 control register (address $001A_{16}$)

The serial I/O1 control register contains bits which control the various serial I/O1 functions. All bits can be read from and written to by software. At reset, this register is cleared to "00_{16}", disabling serial I/O1.

The structure of the serial I/O1 control register is shown in Table 2.7.1.

The serial I/O1 control register determines whether pins $P4_4$ to $P4_7$ are used as ordinary input/output ports or as serial I/O1 function pins. The setting of the serial I/O1 status register also affects these pins.

The control functions specified by the serial I/O1 control register are described in Table 2.7.2.

Table 2.7.1 Structure of Serial I/O1 Control Register

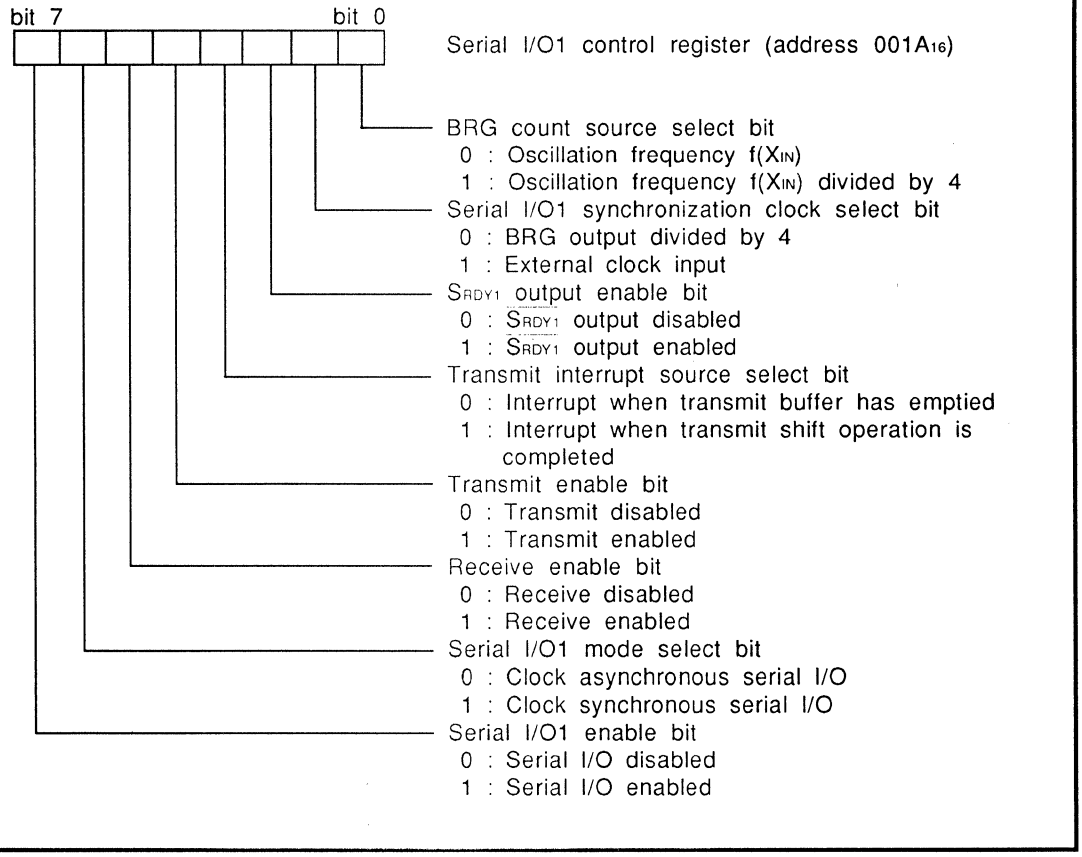


Table 2.7.2 Control Functions of Serial I/O1 Control Register

Bit 1 (serial I/O1 synchronization clock select bit) and Pin $P4_6$*

0	BRG output divided by 4	Pin $P4_6$ can be used as a synchronization clock output pin
1	External clock input	Pin $P4_6$ can be used as an external clock input pin

Bit 2 ($\overline{SRDY1}$ output enable bit) and Pin $P4_7$*

0	$\overline{SRDY1}$ output disabled	Pin $P4_7$ can be used as an ordinary input/output pin
1	$\overline{SRDY1}$ output enabled	Pin $P4_7$ can be used as the $\overline{SRDY1}$ signal output pin

Bit 4 (transmit enable bit) and Pin $P4_5$*

0	Transmit disabled	Pin $P4_5$ can be used as an ordinary input/output pin
1	Transmit enabled	Pin $P4_5$ can be used as the serial data output pin

Bit 4 (transmit enable bit) and the serial I/O1 status register

0	Transmit disabled	Bits 0 and 2 of serial I/O1 status register are cleared
1	Transmit enabled	Bits 0 and 2 of serial I/O1 status register are valid

Bit 5 (receive enable bit) and Pin $P4_4$*

0	Receive disabled	Pin $P4_4$ can be used as an ordinary input/output pin
1	Receive enabled	Pin $P4_4$ can be used as a serial data input pin

Bit 5 (receive enable bit) and the serial I/O1 status register

0	Receive disabled	Bits 1, 3, 4, 5, and 6 of serial I/O1 status register are cleared
1	Receive enabled	Bits 1 and 3 of serial I/O1 status register are valid

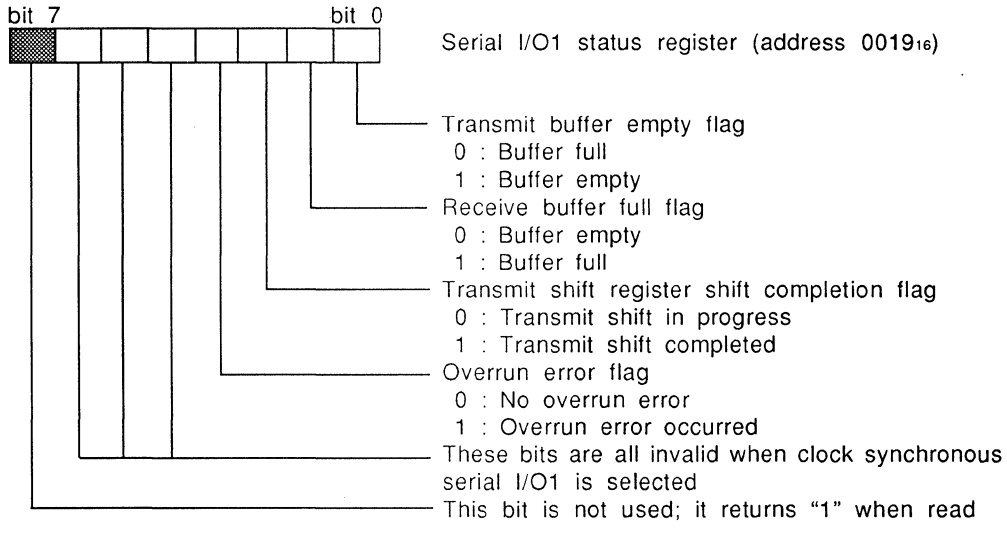
Bit 7 (serial I/O1 enable bit) and the serial I/O1 status register

0	Serial I/O disabled	Bits 1, 3, 4, 5, and 6 of serial I/O1 status register are cleared
1	Serial I/O enabled	Bits 1 and 3 of serial I/O1 status register are valid

*: The function changes for pins $P4_4$ to $P4_7$ are valid only when the serial I/O1 enable bit is "1" (enabled).

(3) Serial I/O1 status register (address 0019_{16})
The serial I/O1 status register consists of seven flags which indicate the transmit/receive status of serial I/O1. It is a read-only register.
At reset, the serial I/O1 status register is set to "80_{16}".

Table 2.7.3 Structure of Serial I/O1 Status Register



- Bit 0 : transmit buffer empty flag (TBE)
  The TBE flag indicates the status of the transmit buffer. It is set to "1" when data written to the transmit buffer is transferred to the transmit shift register, and it is cleared to "0" when data is written into the transmit buffer.
- Bit 1 : receive buffer full flag (RBF)
  The RBF flag indicates the status of the receive buffer. It is set to "1" when data accumulated in the receive shift register is transferred to the receive buffer, and it is cleared to "0" when data is read out of the receive buffer.
- Bit 2 : transmit shift register shift completion flag (TSC)
  The TSC flag indicates the operating status of the transmit shift register. It is cleared to "0" when the transmit shift operation starts, and it is set to "1" as soon as the transmit shift operation is completed.
- Bit 3 : overrun error flag (OE)
  The OE flag is set to "1" if there is still data in the receive buffer when the next character has accumulated in the receive shift register during continuous serial data reception.

(4) Transmit shift register (TSR) and transmit buffer (TB)

The transmit shift register and transmit buffer are 8-bit registers.

Data written to the transmit buffer, is transferred to the transmit shift register and is output from the transmit shift register. During transmission the transmit buffer is empty so the next character to be transmitted can be written into the transmit buffer during this time.

(5) Receive shift register (RSR) and receive buffer (RB)

The receive shift register and receive buffer are each 8-bit registers.

When data has accumulated in the receive shift register, the data is transferred to the receive buffer. The receive buffer can be read normally. When data is transferred to the receive buffer, the receive shift register is empty and it can accept the next character.

Note that in the serial I/O1 function, the receive buffer and the transmit buffer are located at the same address (address 0018_{16}). Reads from that address will read the receiver buffer; writes to that address will write to the transmit buffer.

(6) Reception method

Setting the serial I/O1 control register as shown below will enable the receive status of the M38063M6-XXXFP/GP.

Initialization sequence for serial I/O1 control register

1. Set the serial I/O1 enable bit to enabled ("1").
2. Select either internal or external clock with the synchronization clock select bit.
3. Set the receive enable bit to enabled ("1").

Note that the following settings are also necessary if receive interrupts are to be used:

1. Clear the receive interrupt request bit to "0".
2. After step 1, set the receive interrupt enable bit to "1".

In the serial I/O1 function, the $\overline{SRDY1}$ signal is output when the receive status is enabled. To enable the output of the $\overline{SRDY1}$ signal, the following steps should be added to the initialization of the serial I/O1 control register:

1. Set the $\overline{SRDY1}$ output enable bit to "1".
2. Set the transmit enable bit to "1".

Once the receiver initialization is complete, write to the receive/transmit buffer. (For full duplex data transfer, write transmit data; for half duplex data transfer, write dummy data). As soon as this data is written, the $\overline{SRDY1}$ signal will change from "H" to "L", and will output the receive enabled status.

The $\overline{SRDY1}$ pin returns to a "H" level at the first falling edge of the synchronization clock.

(7) Receiver operation

1. Receive data input through the RxD pin is read into the receive shift register one bit at a time, LSB first, at the rising edge of the shift clock.
2. When a full character has accumulated in the receive shift register, that character is transferred to the receive buffer.
3. The receive buffer full flag and the receive interrupt request bit are set to "1".

The receive buffer full flag is cleared to "0" when data has been read from the receive buffer. The receive interrupt request bit is cleared when the receive interrupt processing sequence starts. Note that the overrun error flag of the serial I/O1 status register will be set to "1" if the receive shift register fills while there is still an unread character in the receive buffer. In this case, the data in the receive shift register is not transferred to the receive buffer, and the character in the receive buffer is held.

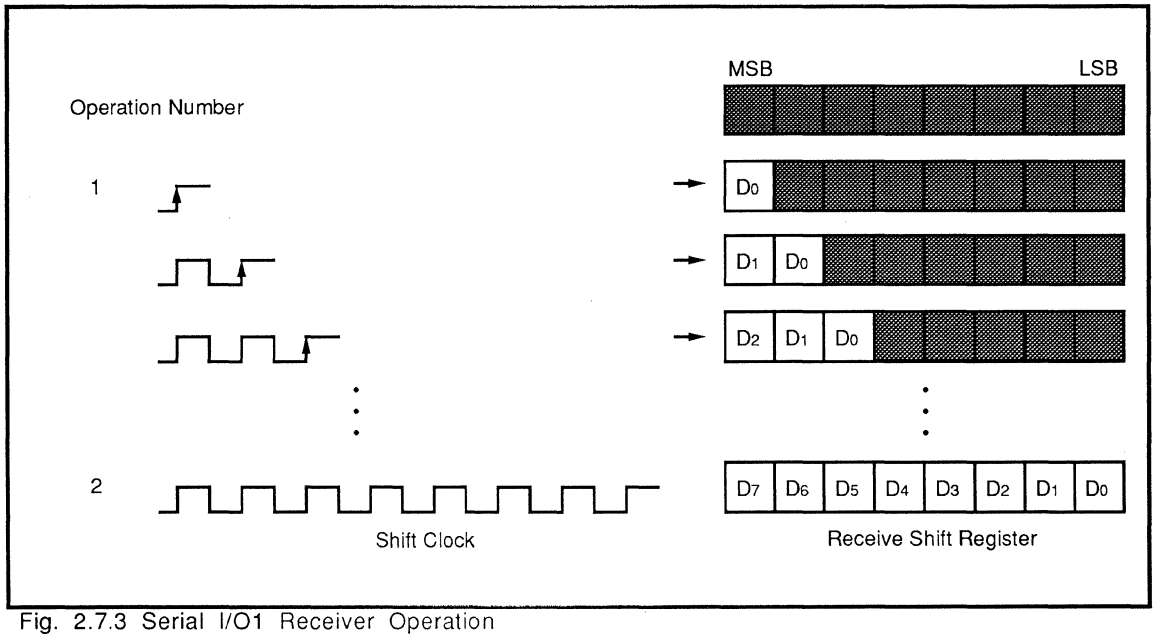


Fig. 2.7.3 Serial I/O1 Receiver Operation

(8) Transmission method

Setting the serial I/O1 control register as shown below puts the M38063M6-XXXFP/GP in transmit enabled status.

Initialization sequence for serial I/O1 control register

1. Set the serial I/O1 enable bit to "1".
2. Select either internal or external clock with the clock select bit.
3. Set the transmit enable bit to "1".

Note that the following settings are also necessary if transmitter interrupts are to be used:

1. Clear the transmit interrupt request bit to "0".
2. Set the transmit interrupt enable bit to "1".

Once the above transmitter initialization is complete, write transmit data to the receive/transmit buffer. If the internal clock is selected, a write generates eight shift clocks.

(9) Transmitter operation

1. If data is written to the transmit buffer, the transmit buffer empty flag is cleared to "0".
2. The data written to the transmit buffer is transferred to the transmit shift register.
3. The data transferred to the transmit shift register is output from the TxD pin one bit at a time, at the falling edges of the shift clock.
4. The data is output from the transmit shift register, starting with the LSB, and is shifted each time one bit is output.
5. Once the transmit shift operation starts, the transmit shift register shift completion flag of the serial I/O1 status register is cleared to "0". If the internal clock is selected and data is written to the transmit buffer at this time, the following data will be output at the shift clock cycle immediately following the end of the current data.
6. The transmit shift register shift completion flag is set to "1" as soon as the transmit operation is completed.

The transmit buffer empty flag is set at step 2, allowing the next character to be written to the transmit buffer while the current data is being sent.

A transmit interrupt request is generated at step 2 if the transmit interrupt source select bit is set to "0", or at step 6 if the bit is set to "1".

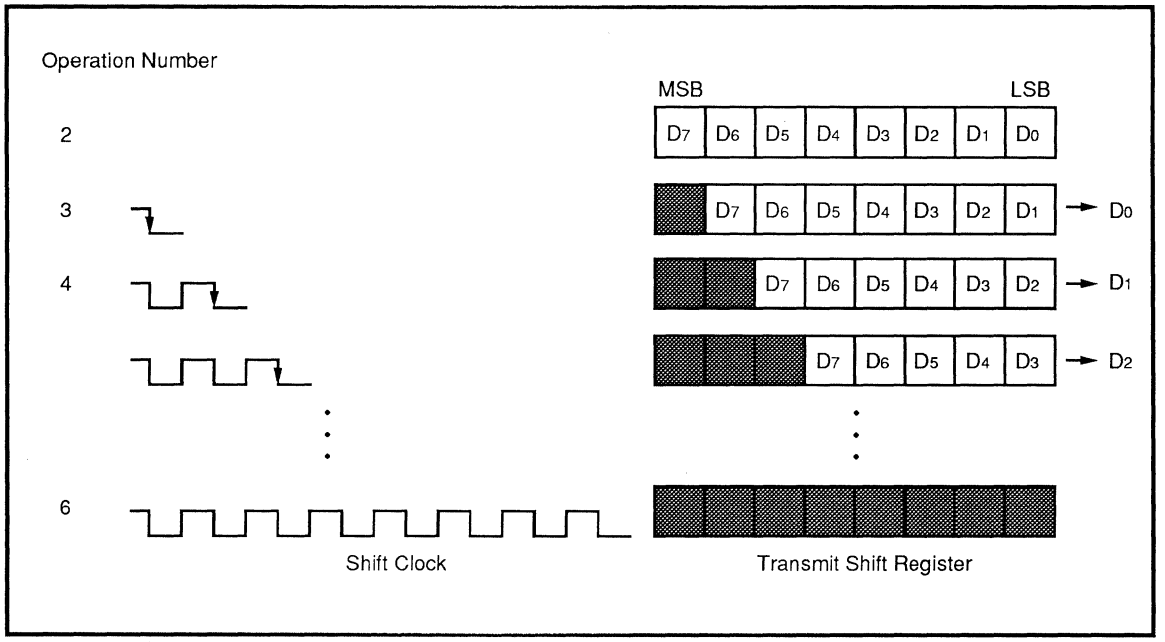


Fig. 2.7.4 Serial I/O1 Transmitter Operation

(10) If an overrun error occurs

An overrun error occurs if a character has accumulated in the receive shift register while there is still data in the receive buffer.

When an overrun error occurs, the data in the receive shift register is not transferred to the receive buffer, and the character in the receive buffer is held. The data in the receive shift register becomes inaccessible, even if the data in the receive buffer is read out.

When an overrun error occurs, the overrun flag of the serial I/O1 status register should be cleared and then the receiver should be initialized.

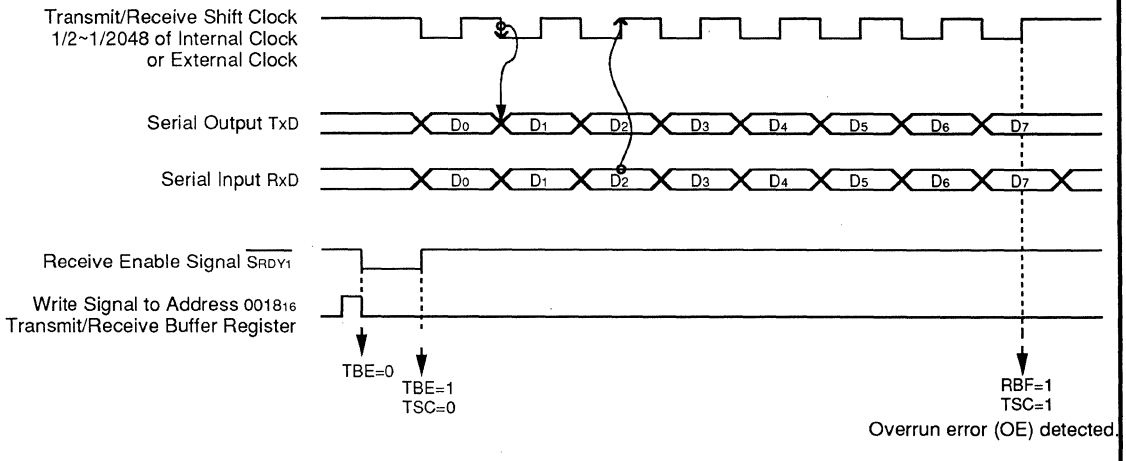
Clear the overrun error flag by any of the following actions:

- Set the serial I/O1 enable bit to "0".
- Set the receive enable bit to "0".
- Write dummy data to the serial I/O1 status register.

(11) Notes on clock selection

Either the internal clock or an external clock can be selected as the synchronization clock of the serial I/O1 function. Note the following points if selecting an external clock when clock synchronization has been selected:

1. If the external clock source has a 50% duty cycle, use a clock of 1.25MHz or less. If the duty cycle is different, make sure that the "H" and "L" widths are at least 400ns for f(X_{IN}) = 5MHz.
2. The shift operation of the transmit or receive shift register will continue as long as the synchronization clock is input to the serial I/O1 circuit, so the synchronization clock should only provide eight pulses per character.
   If the internal clock is selected, the synchronization clock stops automatically when shifting is complete.
3. If an external clock is selected for data transmission, set the transmit enable bit to "1" and write to the transmit buffer with S_{CLK1} held "H".



Note 1: Use the transmit interrupt source select bit (TIC) in the serial I/O1 control register to specify whether to generate a transmit interrupt (TI) when the transmit buffer becomes empty (TBE=1) or when transmit shift operation completes (TSC=1).

Note 2: If data is written in the transmit buffer register when TSC=0, transmit clock is generated continuously and serial data is output continuously from the TxD pin.

Note 3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) is set.

Fig. 2.7.5 Timing of Clock Synchronous Serial I/O1 Function

(12) Clock synchronous serial I/O1 connection examples

Examples of connections for clock synchronous serial I/O1 are shown in Figures 2.7.6, and 2.7.7.

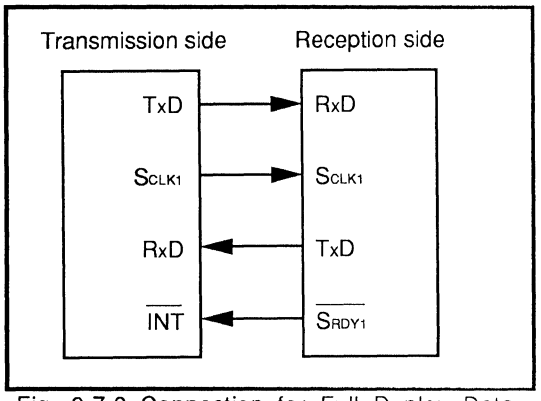


Fig. 2.7.6 Connection for Full Duplex Data Transfer

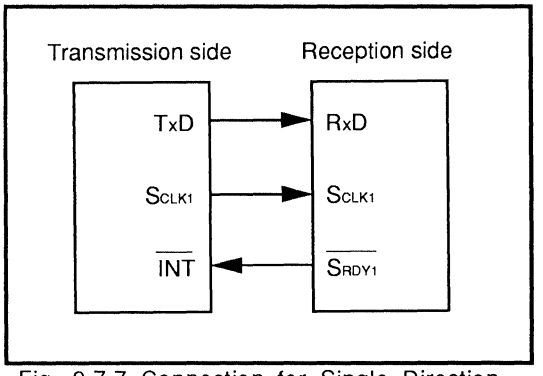


Fig. 2.7.7 Connection for Single Direction Data Transfer

2.7.2 Clock asynchronous serial I/O (UART)

Select clock asynchronous serial I/O mode (UART) by clearing the serial I/O1 mode select bit of the serial I/O1 control register to "0". The clock asynchronous serial I/O function is outlined below.

- Data format

  The following bit configurations can be selected from the UART control register (see Table 2.7.8):

Data format
- Start bit (ST) : 1 bit
- Data bits (DATA) : 7 or 8 bits
- Parity bit (PAR) : None or 1 bit
- Stop bit(s) : 1 bit or 2 bits

- Synchronization clock

  Either the internal clock or an external clock can be selected by setting the serial I/O1 synchronization clock select bit of the serial I/O1 control register.

Synchronization clock
- Internal clock (when serial I/O1 synchronization clock select bit is "0")
  The clock is the BRG output divided by 16.
- External clock (when serial I/O1 synchronization clock select bit is "1")
  An external clock input from the S_{CLK1} pin is selected (max. 5MHz, when $f(X_{IN})$ = 5MHz).

A block diagram of the clock asynchronous serial I/O1 function is shown in Figure 2.7.8.

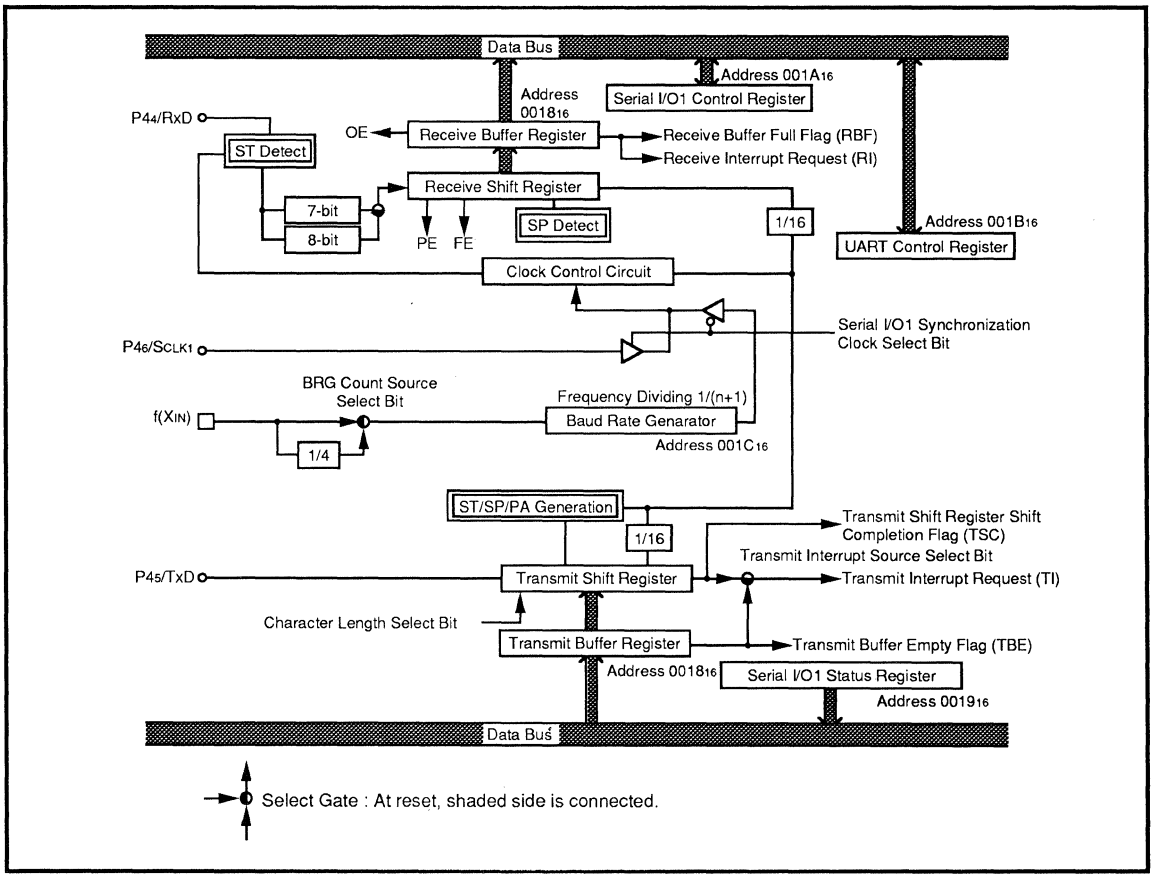


Fig. 2.7.8 Block Diagram of Clock Asynchronous Serial I/O Function

The individual blocks of the clock asynchronous serial I/O function are described below.

(1) Baud rate generator (BRG) (address $001C_{16}$)

The BRG is an 8-bit timer used exclusively for the serial I/O1 function. When the internal clock is selected as the synchronization clock, the shift clock is the BRG output divided by 16. A block diagram of the BRG is shown in Figure 2.7.9.

Up to 312.5kbps can be selected as the baud rate, depending on the value of the BRG count source select bit (bit 0 of the serial I/O1 control register) and the setting of the BRG. The baud rates available when UART is selected are listed in Table 2.7.4.

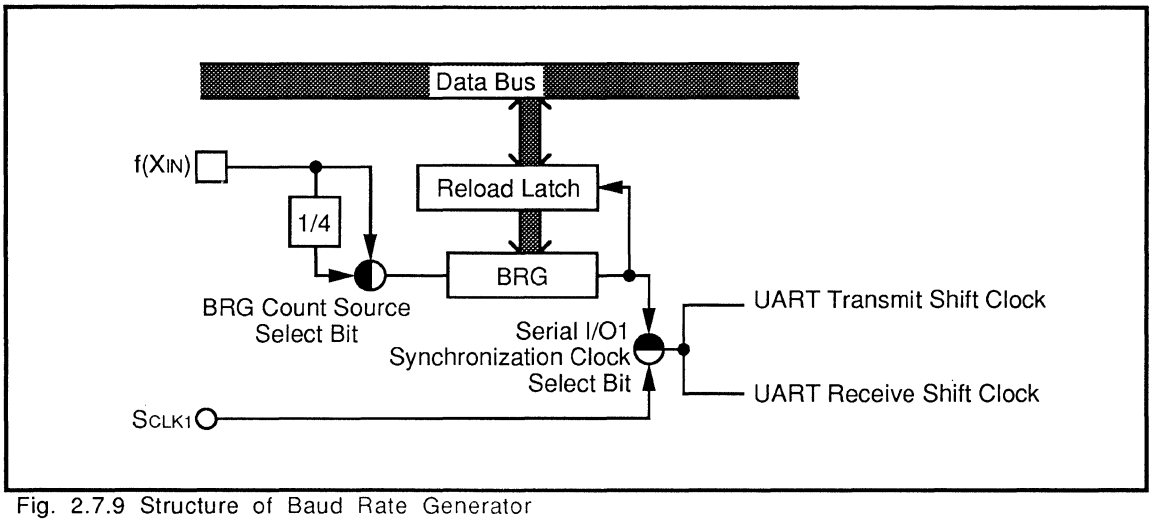


Fig. 2.7.9 Structure of Baud Rate Generator

Table 2.7.4 Baud Rate Settings

BRG count source	Setting of BRG	Baud rate (bps)	
		When f(XIN) = 4.9152MHz	When f(XIN) = 5MHz
f(XIN)/4	255(FF_{16})	300	305.17578
f(XIN)/4	127($7F_{16}$)	600	610.35156
f(XIN)/4	63($3F_{16}$)	1200	1220.7031
f(XIN)/4	31($1F_{16}$)	2400	2441.4063
f(XIN)/4	15($0F_{16}$)	4800	4882.8125
f(XIN)/4	7(07_{16})	9600	9765.625
f(XIN)/4	3(03_{16})	19200	19531.25
f(XIN)/4	1(01_{16})	38400	39062.5
f(XIN)	3(03_{16})	76800	78125
f(XIN)	1(01_{16})	153600	156250
f(XIN)	0(00_{16})	307200	312500

(2) Serial I/O1 control register (address $001A_{16}$)

The serial I/O1 control register contains bits that control the various serial I/O1 functions. All of this register's bits can be read from and written to from software. At reset, this register is cleared to "00_{16}", disabling serial I/O1.

The structure of the serial I/O1 control register is shown in Table 2.7.5.

The serial I/O1 control register determines whether pins $P4_4$ to $P4_7$ are used as ordinary input/output ports or as serial I/O1 function pins. The bits of the serial I/O1 status register also affect these pins.

The control functions specified by the serial I/O1 control register are described in Table 2.7.6.

Table 2.7.5 Structure of Serial I/O1 Control Register

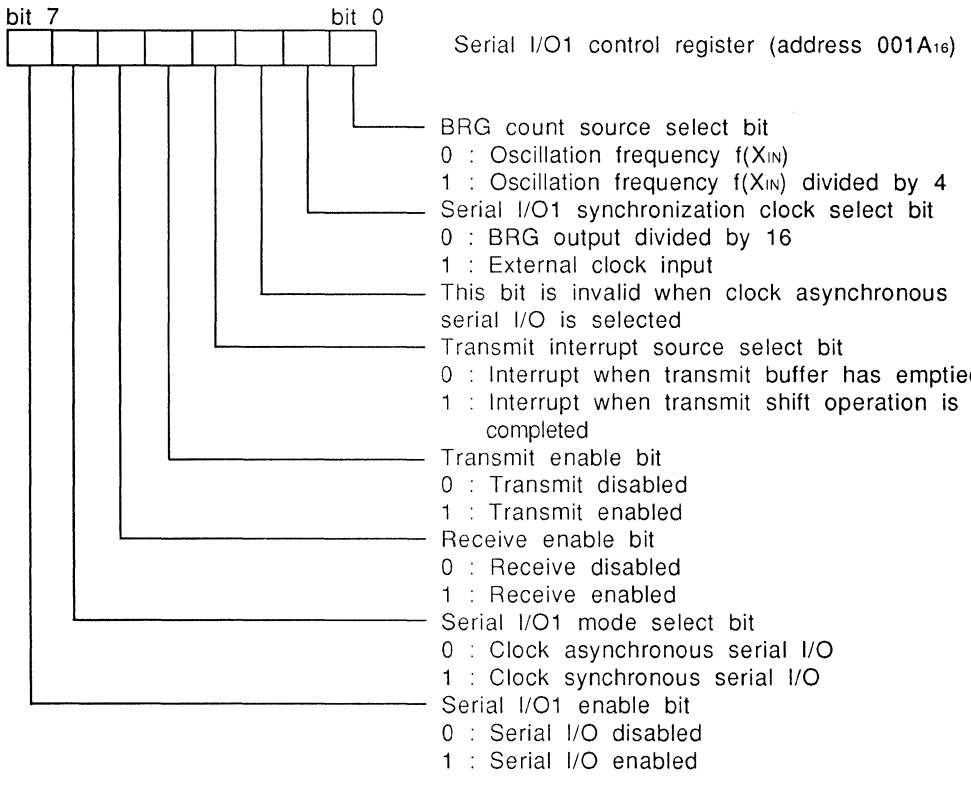


Table 2.7.6 Control Functions of Serial I/O1 Control Register

Bit 1 (serial I/O1 synchronization clock select bit) and Pin $P4_6$*

0	BRG output divided by 16	The $P4_6$ pin is an ordinary input/output pin
1	External clock input	The $P4_6$ pin can be used as external clock input pin

Bit 4 (transmit enable bit) and Pin $P4_5$*

0	Transmit disabled	The $P4_5$ pin is an ordinary input/output pin
1	Transmit enabled	The $P4_5$ pin can be used as a serial data output pin

Bit 4 (transmit enable bit) and serial I/O1 status register

0	Transmit disabled	Bits 0 and 2 of serial I/O1 status register cleared
1	Transmit enabled	Bits 0 and 2 of serial I/O1 status register valid

Bit 5 (receive enable bit) and Pin $P4_4$*

0	Receive disabled	The $P4_4$ pin is an ordinary input/output pin
1	Receive enabled	The $P4_4$ pin can be used as a serial data input pin

Bit 5 (receive enable bit) and serial I/O1 status register

0	Receive disabled	Bits 1, 3, 4, 5, and 6 of serial I/O1 status register cleared
1	Receive enabled	Bits 1, 3, 4, 5, and 6 of serial I/O1 status register valid

Bit 7 (serial I/O1 enable bit) and serial I/O1 status register

0	Serial I/O disabled	Bits 1, 3, 4, 5, and 6 of serial I/O1 status register cleared
1	Serial I/O enabled	Bits 1, 3, 4, 5, and 6 of serial I/O1 status register valid

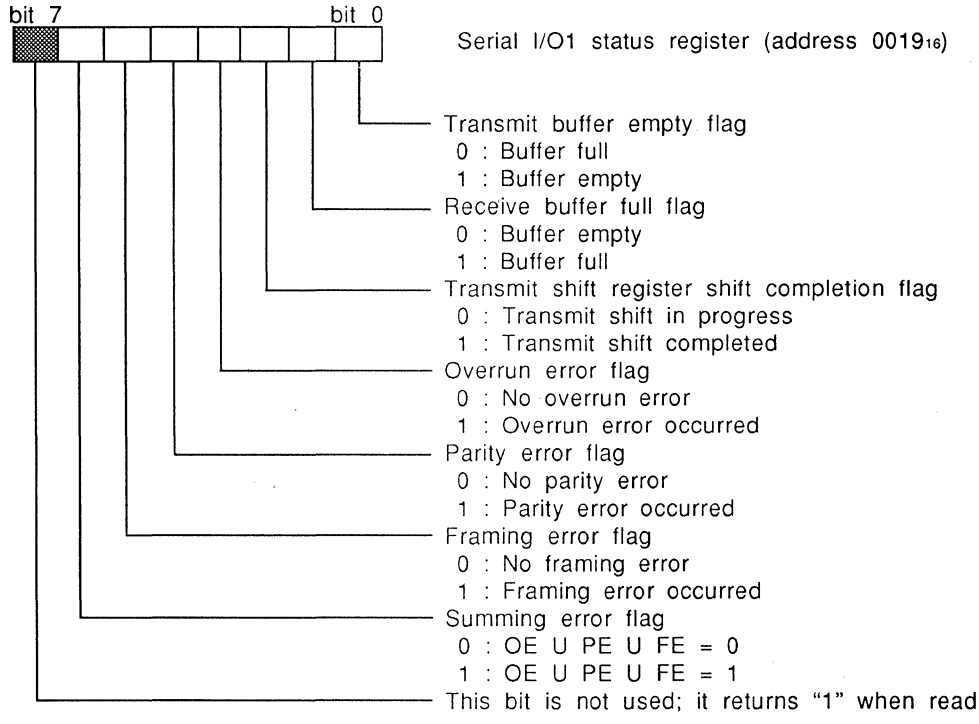
* : The function changes for pins $P4_4$ to $P4_6$ are valid only when the serial I/O1 enable bit is "1" (enabled). The $P4_7$ pin can be used as an ordinary input/output pin.

(3) Serial I/O1 status register (address 0019_{16})

The serial I/O1 status register consists of seven flags which indicate the transmit/receive status of each of the serial I/O functions. It is a read-only register.

At reset, the serial I/O1 status register is set to "80_{16}".

Table 2.7.7 Structure of Serial I/O1 Status Register



- Bit 0 : transmit buffer empty flag (TBE)
  The TBE flag indicates the status of the transmit buffer. It is set to "1" when data written to the transmit buffer is transferred to the transmit shift register, and it is cleared to "0" when data is written into the transmit buffer.
- Bit 1: receive buffer full flag (RBF)
  The RBF flag indicates the status of the receive buffer. It is set to "1" when the character accumulated in the receive shift register is transferred to the receive buffer, and it is cleared to "0" when data is read out of the receive buffer.
- Bit 2: transmit shift register shift completion flag (TSC)
  The TSC flag indicates the operating status of the transmit shift register. It is cleared to "0" when the transmit shift operation starts, and it is set to "1" as soon as the transmit shift operation is completed.
- Bit 3: overrun error flag (OE)
  The OE flag is set to "1" if a character has not been read from the receive buffer when the next character has accumulated in the receive shift register.
- Bit 4: parity error flag (PE)
  The PE flag is set if the parity of receive data differs from the specified parity. The PE flag is valid only when parity checking is enabled.

- Bit 5 : framing error flag (FE)
  The FE flag determines whether the frame synchronization is correct. If the stop bit is not received when it is expected, the FE bit is set to "1".
  Note that only the first stop bit is checked; following stop bits are ignored.
- Bit 6 : summing error flag (SE)
  The SE flag is set if there is an error in one or more of the OE, PE, and FE flags.

(4) UART control register (address $001B_{16}$).
The UART control register consists of five control bits which determine the format of data transmitted and received by the clock asynchronous serial I/O function. These low-order 5 bits of the UART control register can be read and written to by programs. At reset, this register is set to "$E0_{16}$".

Table 2.7.8 Structure of UART Control Register

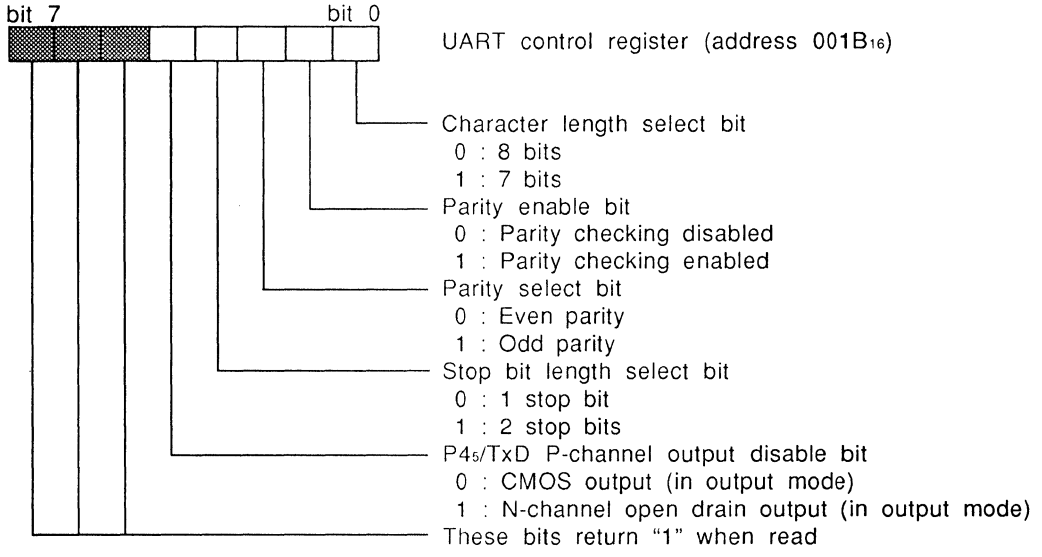


Table 2.7.9 Relationship between Contents of UART Control Register and Data Format

UART control register				Serial data transfer format
bit 3	bit 2	bit 1	bit 0	
0	X	0	0	1ST-8DATA-1SP
0	X	0	1	1ST-7DATA-1SP
0	X	1	0	1ST-8DATA-1PAR-1SP
0	X	1	1	1ST-7DATA-1PAR-1SP
1	X	0	0	1ST-8DATA-2SP
1	X	0	1	1ST-7DATA-2SP
1	X	1	0	1ST-8DATA-1PAR-2SP
1	X	1	1	1ST-7DATA-1PAR-2SP

ST : Start bit
DATA : Data bits
SP : Stop bit(s)
PAR : Parity bit

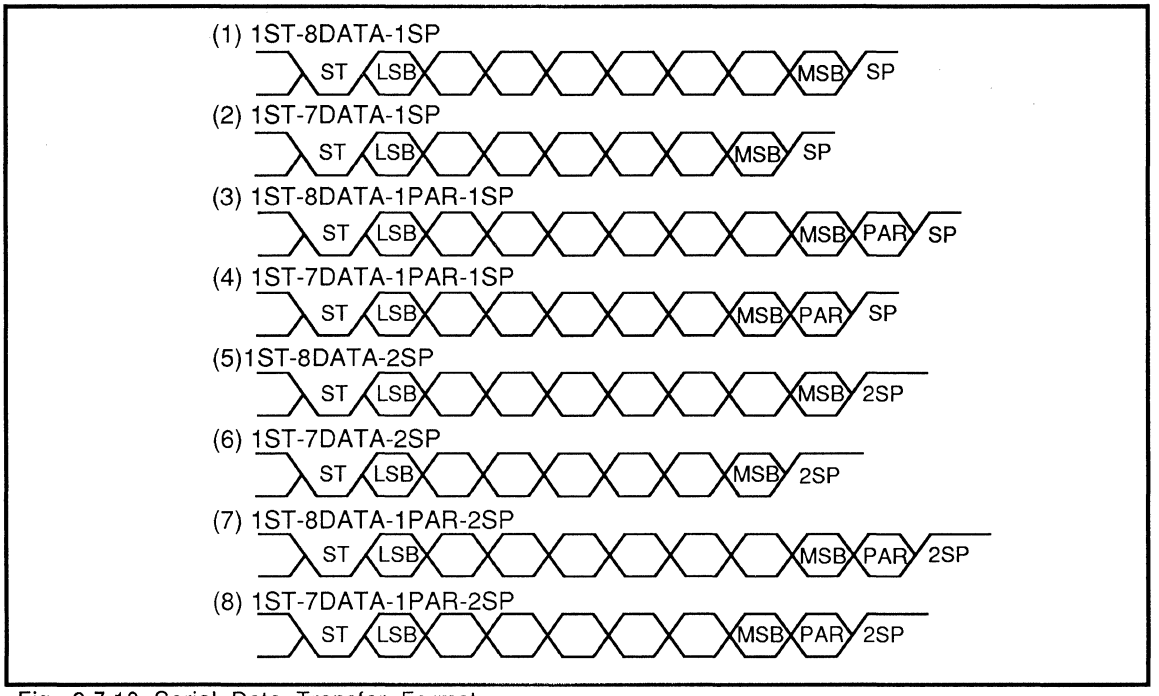


Fig. 2.7.10 Serial Data Transfer Format

(5) Transmit shift register (TSR) and transmit buffer (TB)

The transmit shift register and transmit buffer each are 8-bits.

When data is written to the transmit buffer, that data is transferred to the transmit shift register and it is output by the transmit shift register. During transmission, the next character to be transmitted can be written into the transmit buffer.

(6) Receive shift register (RSR) and receive buffer (RB)

The receive shift register and receive buffer each are 8-bits.

When a character has accumulated in the receive shift register, it is transferred to the receive buffer. At this time, the next character can be received into the receive shift register.

Note: in the serial I/O 1 function, the receive buffer and the transmit buffer are located at the same address (address 0018_{16}). During full duplex data transfer, if that address is read from, receive data is read out; if that address is written to, transmit data is written.

(7) Reception method

Setting the serial I/O1 control register and UART control register as shown below enables the serial I/O1 receiver.

Reception preparation

1. Set the serial I/O1 enable bit to "1".
2. Select either internal or external clock with the synchronization clock select bit.
3. Set the required data format in the UART control register.

Note that the following settings are necessary if receive interrupts are to be used:

1. Clear the receive interrupt request bit to "0".
2. After step 1, set the receive interrupt enable bit to "1".

Once the above reception preparation is complete, set the receive enable bit of the serial I/O1 control register to enabled. This operation enables the detection of a start bit, and serial data reception starts.

(8) Receiver operation

1. Receive data input through the RxD pin is read one bit at a time into the receive shift register.
2. After the start bit is detected at the falling edge at the RxD pin (start bit reception), the bit is checked again at the expected center of the start bit. The start bit is valid if the signal level is "L". If the signal level is "H", the system judges that there is noise on the line and waits for another start bit.
3. When the specified number of bits of the signal have been received and the first stop bit is detected, the contents of the receive shift register are transferred to the receive buffer. If 7-bit character length is selected, the MSB of the receive data stored in the receive buffer is set to "0".
4. At the center of the first stop bit, the receive buffer full flag is set and a receive interrupt request is generated. At the same time, the error status is checked and the error flags are updated.

The receive buffer full flag is cleared to "0" when data is read from the receive buffer. The receive interrupt request bit is cleared when the receive interrupt processing sequence starts.

(9) Transmission method

Setting the serial I/O1 control register and UART control register as shown below enables the serial I/O1 transmitter.

Transmission preparation

1. Set the serial I/O1 enable bit to "1".
2. Select either internal or external clock with the synchronization clock select bit.
3. Set the data format in the UART control register.
4. Set the transmit enable bit to "1".

Note that the following settings are necessary if transmit interrupts are to be used:

1. Clear the transmit interrupt request bit to "0".
2. After step 1, set the transmit interrupt enable bit to "1".

Once the above transmitter preparation is complete, write transmit data to the receive/transmit buffer. If the internal clock is selected as the synchronization clock, this write generates the shift clock.

(10) Transmission operation

1. When data is written to the transmitter buffer, the transmit buffer empty flag is cleared to "0".
2. The data written to the transmit buffer is transferred to the transmit shift register.
3. The data transferred to the transmit shift register is output from the TxD pin one bit at a time, starting with a start bit. The start, parity, and stop bits are generated by the hardware as determined by the UART control register.
4. Once the transfer shift operation starts, the transmit shift register shift completion flag of the serial I/O1 status register is cleared to "0".
5. The transmit shift register shift completion flag of the serial I/O1 status register is set to "1" at the center of the final stop bit.

The transmit buffer empty flag is set at step 2, enabling the writing of the next batch of transmit data to the transmit buffer.

A transmit interrupt request is generated at step 2 if the transmit interrupt source select bit is set to "0", or at step 5 if that bit is set to "1".

(11) Handling if parity, framing, or summing error occurs

If a parity, framing, or summing error occurs, the flag in the serial I/O1 status register corresponding to that error is set. Since these flags are not cleared automatically, they should be cleared by software. Parity, framing, and summing errors can be cleared by clearing the receive enable bit or by writing dummy data to the serial I/O1 status register.

(12) Handling if overrun error occurs

An overrun error occurs if a character is accumulated in the receive shift register while there is still a character in the receive buffer.

When an overrun error occurs, the character in the receive buffer is maintained and the character in the receive shift register becomes inaccessible.

When an overrun error occurs, the overrun flag of the serial I/O status register should be cleared and then the receiver should be re-initialized.

Clear the overrun error flag by performing any of the following actions:

- Set the serial I/O1 enable bit to "0".
- Set the receive enable bit to "0".
- Write dummy data to the serial I/O1 status register.

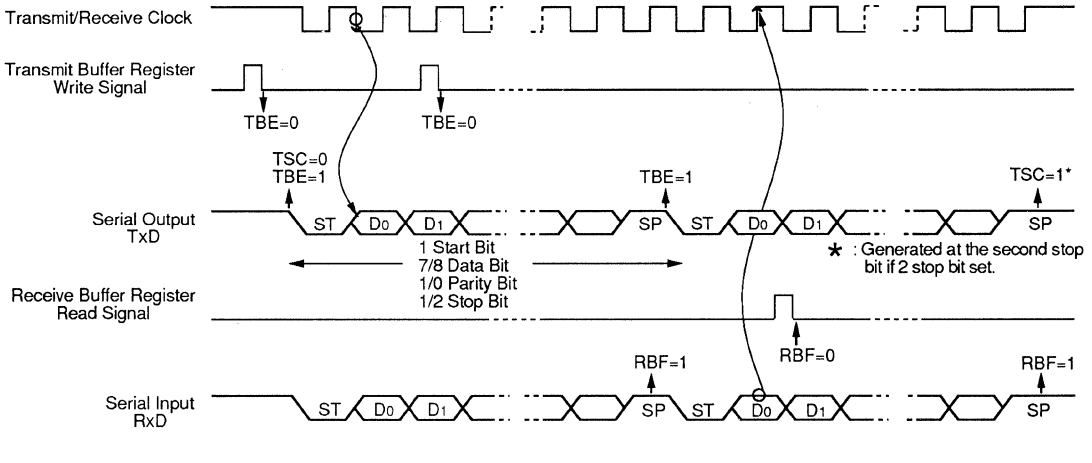
(13) Notes on clock selection

Either the internal clock or an external clock can be selected as the synchronization clock of the serial I/O1 function. If an external clock is selected as the synchronization clock, use a clock of 5MHz or less when the duty cycle is 50%. If the duty cycle is different, make sure that the "H" and "L" widths are at least 100ns.

(14) Notes on using the TxD/P45 pin for N-channel open drain output

Bit 4 of the UART control register (address $00E9_{16}$) is the P-channel transistor output disable bit for the TxD/P45 pin. This bit is valid whenever the TxD/P45 pin is being used as an output pin. When this bit is "0", ordinary CMOS output is selected; when it is "1", N-channel open drain output is selected.

Note that when the TxD/P45 pin is being used for N-channel open drain output, the voltage applied to it must not exceed V_{CC} + 0.3V.



Note 1: Error flag detection is performed as soon as RBF=1 (first received stop bit).
Note 2: Transmit interrupt (TI) is set to either TBE=1 or TSC=1 according to the transmit interrupt source select bit (TIC) in the serial I/O1 control register.
Note 3: Receive interrupt (RI) is set by RBF=1.

Fig. 2.7.11 Timing of Clock Asynchronous Serial I/O Function

2.7.3 Notes on using serial I/O1 function

(1) Resetting the serial I/O1 control register

Before resetting the serial I/O1 control register, set the transmit and receive enable bits to disabled (if they were enabled) and reset the transmit and receive circuits. If the serial I/O1 control register is reset without resetting the circuits in this way, the new setting may not operate correctly.

(2) Transmit interrupt requests when the transmit enable bit is set

If the transmit enable bit is set to "1", the transmit buffer empty flag and the transmit shift register shift completion flag are also set to "1". An interrupt request is generated and the transmit interrupt request bit is set, regardless of the timing selected for the generation of transmit interrupts.

To use transmit interrupts, first set the transmit enable bit, then clear the transmit interrupt request bit and set the transmit interrupt enable bit to enabled.

(3) To disable transmission after one byte of data has been transmitted

The transmit shift register shift completion (TSC) flag is used by the serial I/O1 function to signal the completion of data transmission. The TSC flag is cleared to "0" while data is being transmitted, and it is set to "1" when the data transmission is completed. If transmission is disabled after confirming that the TSC flag has been set, transmission can be forced to end after one byte of data is transmitted.

If the TSC flag is checked immediately after the serial I/O1 function has been enabled, transmission can be disabled before it has begun. Make sure that the TSC flag is referenced after transmission has started.

(4) Using the TxD/$P4_5$ pin for N-channel open drain output

Bit 4 of the UART control register (address $00E9_{16}$) is the P-channel transistor output disable bit for the TxD/$P4_5$ pin. This bit is valid whenever the TxD/$P4_5$ pin is being used as an output pin. When this bit is "0", ordinary CMOS output is selected; when it is "1", N-channel open drain output is selected.

Note that when the TxD/$P4_5$ pin is being used for N-channel open drain output, the voltage applied to it must not exceed V_{CC} + 0.3V.

For details of how to use the serial I/O1 function, see Appendix 3, "Notes on Use".

2.8 Serial I/O2

The serial I/O2 function of the M38063M6-XXXFP/GP uses the clock synchronous method.

- Transfer method
  Half duplex data transfer is available.
- Synchronization clock
  Select either the internal clock or an external clock by setting the synchronization clock select bit of the serial I/O2 control register.

Synchronization clock

- Internal clock (when serial I/O2 synchronization clock select bit is "1")
  f(XIN) divided by 8, 16, 32, 64, 128, or 256 can be selected.
- External clock (when serial I/O2 synchronization clock select bit is "0")
  An external clock input from the SCLK2 pin is selected (max. 1MHz).

A block diagram of the clock synchronous serial I/O2 function is shown in Figure 2.8.1.

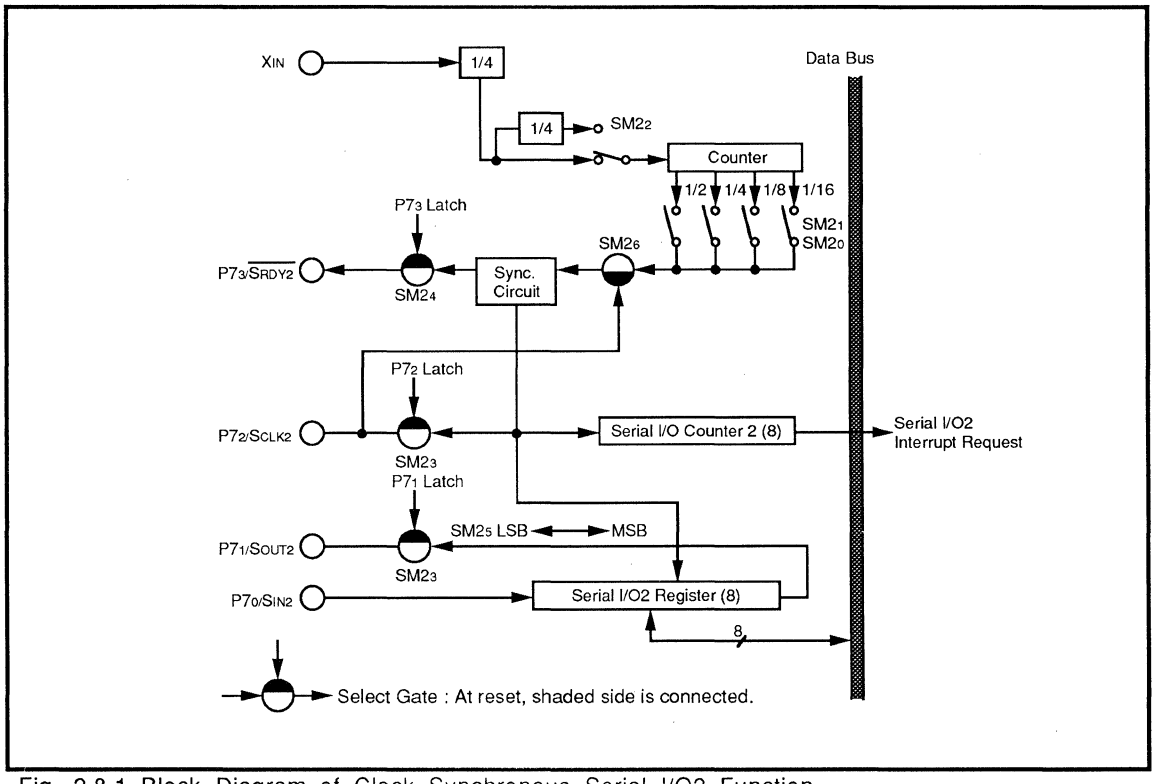
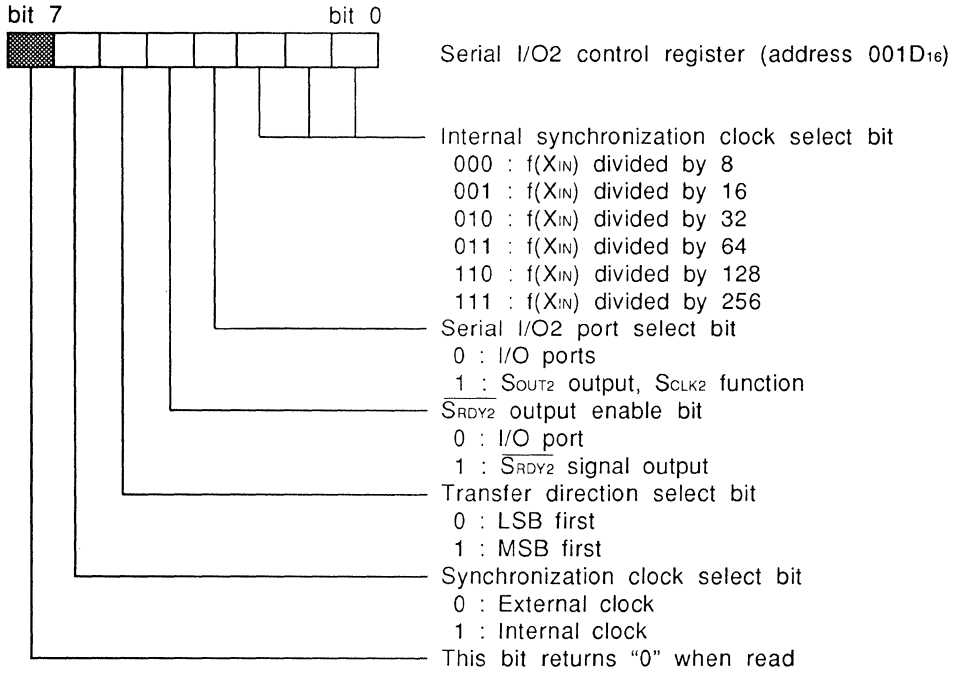


Fig. 2.8.1 Block Diagram of Clock Synchronous Serial I/O2 Function

2.8.1 Serial I/O2 control register (address $001D_{16}$)

The serial I/O2 control register controls the various serial I/O2 functions. All of this register's bits can be read from and written to by software. At reset, this register is cleared to "00_{16}".
The structure of the serial I/O2 control register is shown in Table 2.8.1.
The serial I/O2 control register determines whether pins $P7_1$ to $P7_3$ are used as ordinary input/output ports or as serial I/O2 function pins. This register also determines the transfer direction and transfer clock for serial data.

Table 2.8.1 Structure of Serial I/O2 Control Register



2.8.2 Reception

(1) Reception method

Setting the serial I/O2 control register as shown below enables the M38063M6-XXXFP/GP serial I/O2 receiver.

Initialization sequence for serial I/O2 control register

1. Select either internal or external clock using the synchronization clock select bit.
2. If using the internal clock, select the divide ratio with the internal synchronization clock select bits.
3. Set the serial I/O2 port select bit to "1".
4. Select the transfer direction with the transfer direction select bit.

Note that the following settings are also necessary if serial I/O2 interrupts are to be used:

5. Clear the serial I/O2 interrupt request bit to "0".
6. After step 5, set the serial I/O2 interrupt enable bit to "1".

The $\overline{S_{RDY2}}$ signal outputs the receive enabled status of the serial I/O2 function. To enable the output of the $\overline{S_{RDY2}}$ signal, add the following step after step 3 when initializing the serial I/O2 control register:

- Set the $\overline{S_{RDY2}}$ output enable bit to "1".

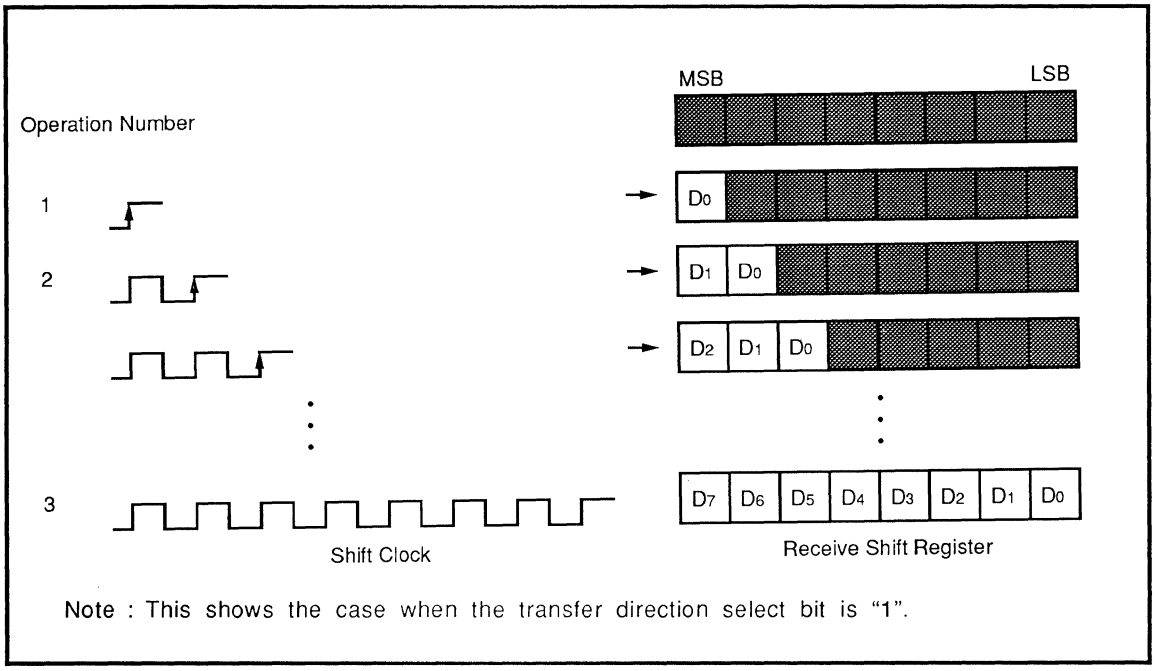
Once the above reception preparation is complete, write dummy data to the serial I/O2 register. During the write cycle, the $\overline{S_{RDY2}}$ pin's level is "H"; when the write cycle ends, the $\overline{S_{RDY2}}$ pin falls to "L", outputing the receive enabled status.

The $\overline{S_{RDY2}}$ pin returns to "H" level at the first falling edge of the synchronization clock.

(2) Reception operation

1. During a write cycle to the serial I/O2 register, the serial I/O counter 2 is set to "7" and the transfer clock goes "H".
2. After the write cycle ends, receive data is input from the S_{IN} pin one bit at a time, at the rising edge of the transfer clock.
3. The input data is read one bit at a time into the serial I/O2 register. Each time new data is read in, the contents of the serial I/O2 register are shifted one bit.
4. An interrupt request is generated after eight counts of the transfer clock. If the internal clock is selected as the transfer clock, the transfer clock stops at "H".

Whether the data is read from the LSB or the MSB (step 3) can be selected by the transfer direction select bit of the serial I/O2 control register.
The interrupt request bit is cleared when the interrupt processing sequence starts.



Note : This shows the case when the transfer direction select bit is "1".

Fig. 2.8.2 Serial I/O2 Reception Operation

2.8.3 Transmission

(1) Transmission method

Setting the serial I/O2 control register as shown below puts the serial I/O2 function in transmit enabled status.

Initialization sequence for serial I/O2 control register

1. Select either internal or external clock with the synchronization clock select bit.
2. If using the internal clock, select the divide ratio with the internal synchronization clock select bits.
3. Set the serial I/O2 port select bit to "1".
4. Select the transfer direction with the transfer direction select bit.

Note that the following settings are also necessary if serial I/O2 interrupts are to be used:

5. Clear the serial I/O2 interrupt request bit to "0".
6. After step 5, set the serial I/O2 interrupt enable bit to "1".

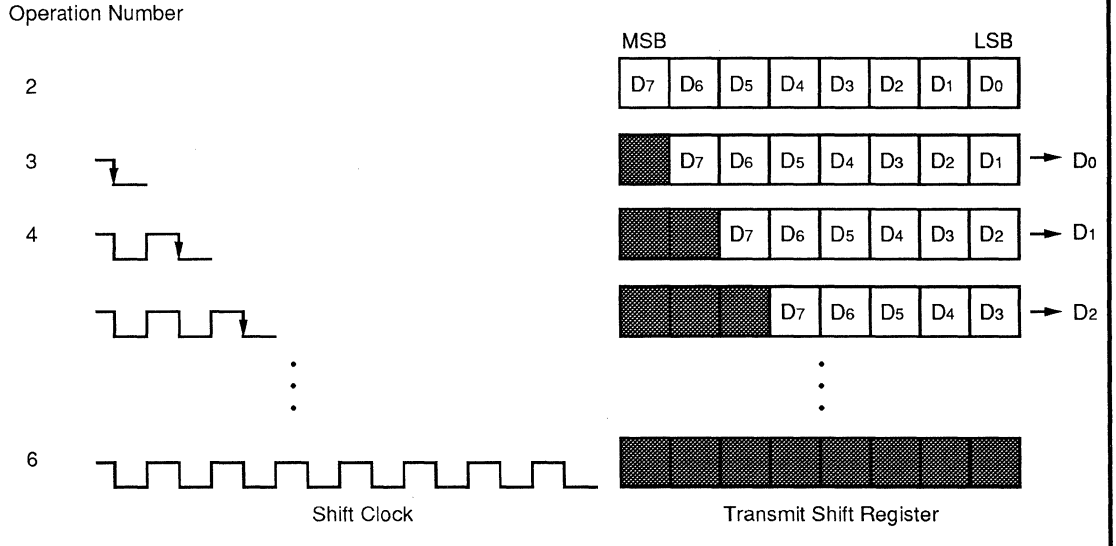
Once the above transmission preparation is complete, write transmit data to the serial I/O2 register. If the internal clock is selected as the synchronization clock, this write generates eight shift clocks.

(2) Transmission operation

1. During a write cycle to the serial I/O2 register, the serial I/O counter 2 is set to "7" and the transfer clock goes "H".
2. After the write cycle ends, transmit data is output from the S_{OUT} pin one bit at a time, at the falling edge of the transfer clock.
3. Data is read one bit at a time from the serial I/O2 register, starting at either the LSB or the MSB. The contents of the serial I/O2 register are shifted each time new data is read out.
4. An interrupt request is generated after eight counts of the transfer clock. If the internal clock is selected as the transfer clock, the transfer clock stops at "H".

Whether the read from the serial I/O2 register in step 3 starts at the LSB or the MSB can be selected by the transfer direction select bit of the serial I/O2 control register.

The interrupt request bit is cleared when the interrupt processing sequence starts.



Note : This shows the case when the transfer direction select bit is "0".

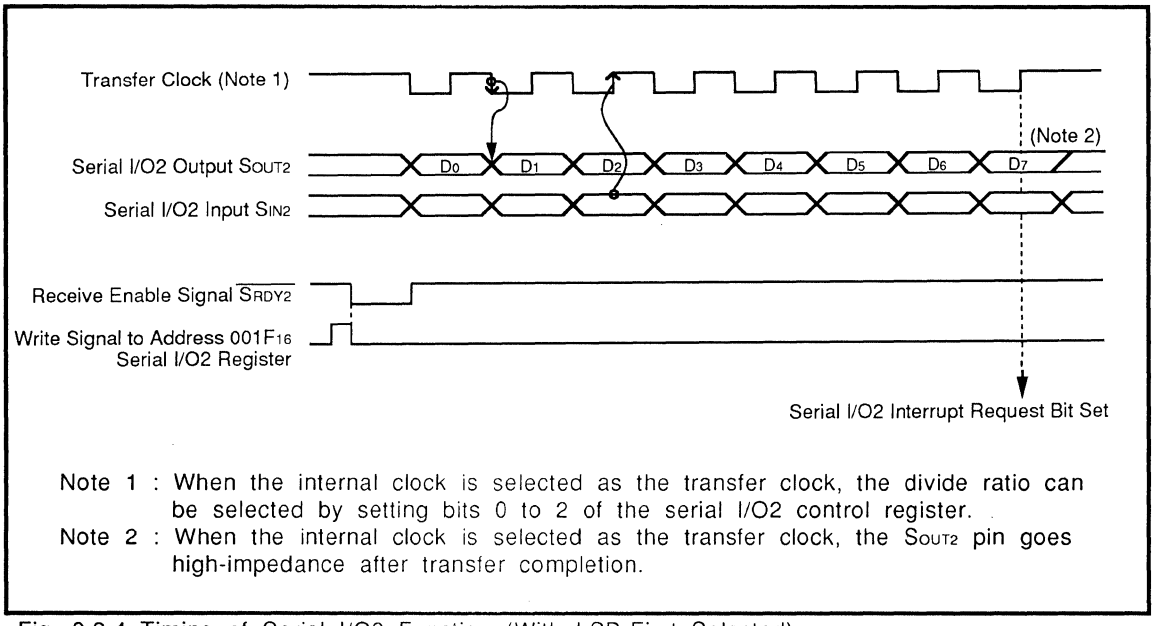
Fig. 2.8.3 Serial I/O2 Transmission Operation

2.8.4 Notes on external clock selection

Either the internal clock or an external clock can be selected as the synchronization clock of the serial I/O2 function. If an external clock is selected, note the following points:

(1) Use a clock of 1.25MHz or less for the clock source, with a 50% duty cycle.
If the duty cycle is different, make sure that the "H" and "L" widths are at least 400ns (for f(X_{IN}) = 5MHz).

(2) The shift operation continues so long as the synchronization clock is input to the serial I/O2 circuit. Only eight pulses should be input for each character.
If the internal clock is selected, the synchronization clock stops automatically.



Note 1 : When the internal clock is selected as the transfer clock, the divide ratio can be selected by setting bits 0 to 2 of the serial I/O2 control register.

Note 2 : When the internal clock is selected as the transfer clock, the S_{OUT2} pin goes high-impedance after transfer completion.

Fig. 2.8.4 Timing of Serial I/O2 Function (With LSB-First Selected)

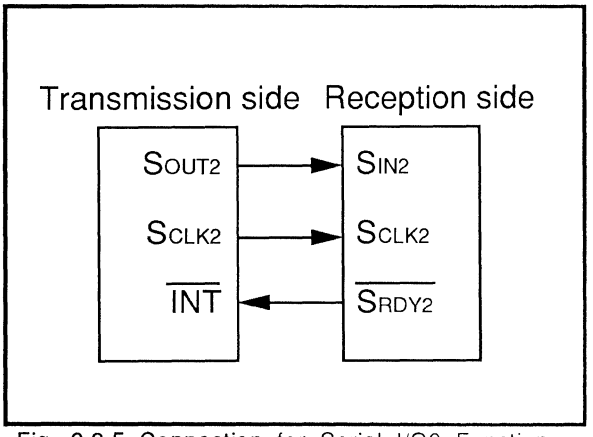


Fig. 2.8.5 Connection for Serial I/O2 Function

2.9 A-D Converter

The A-D converter built into the M38063M6-XXXFP/GP has the following characteristics:

- Analog input pins (also used as port P6) : 8 channels
- Conversion method : Successive comparison approximation
- Resolution : 8 bits
- Absolute accuracy : ± 1 LSB (Typ.)
- Conversion speed : 20μs (at f(XIN) = 5MHz)

A block diagram of the A-D converter is shown in Figure 2.9.1.

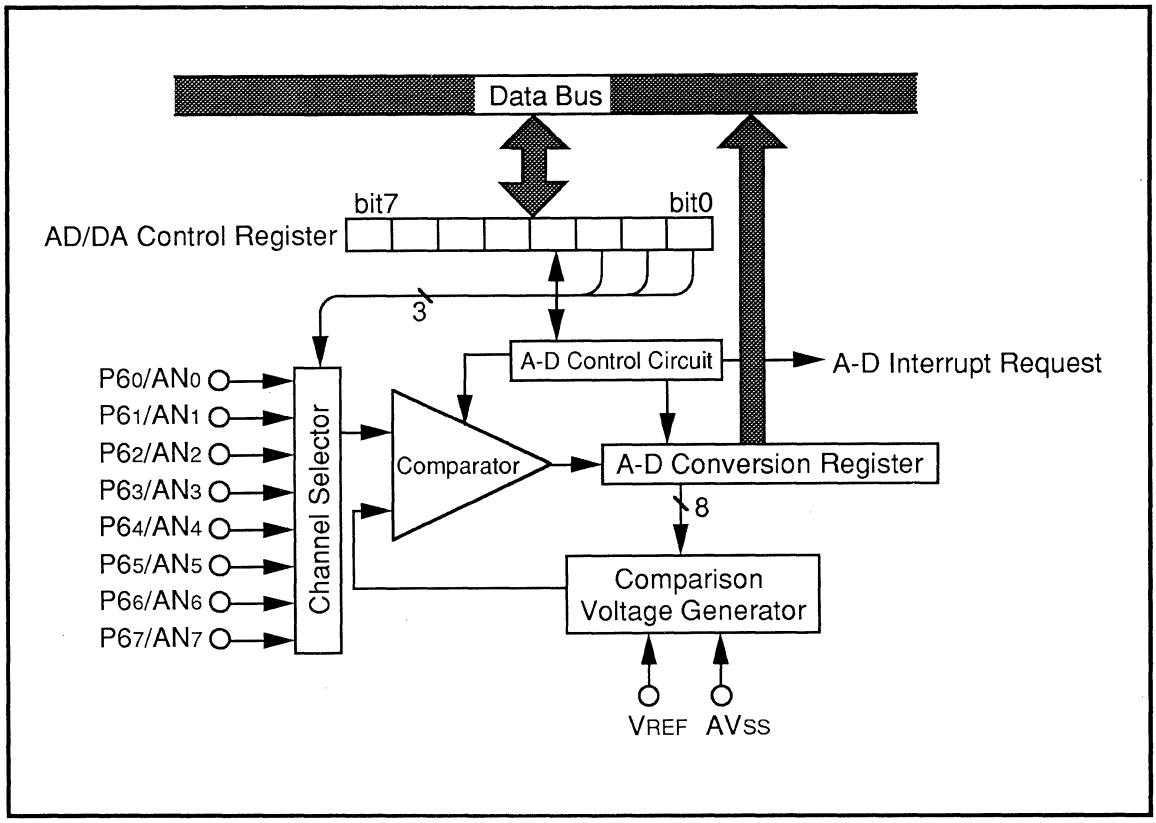


Fig. 2.9.1 Block Diagram of A-D Converter

2.9.1 Block description

The blocks of the A-D converter are described below.

(1) A-D conversion register

The A-D conversion register is a read-only register that contains the result of an A-D conversion. Do not read the contents of this register during A-D conversion.

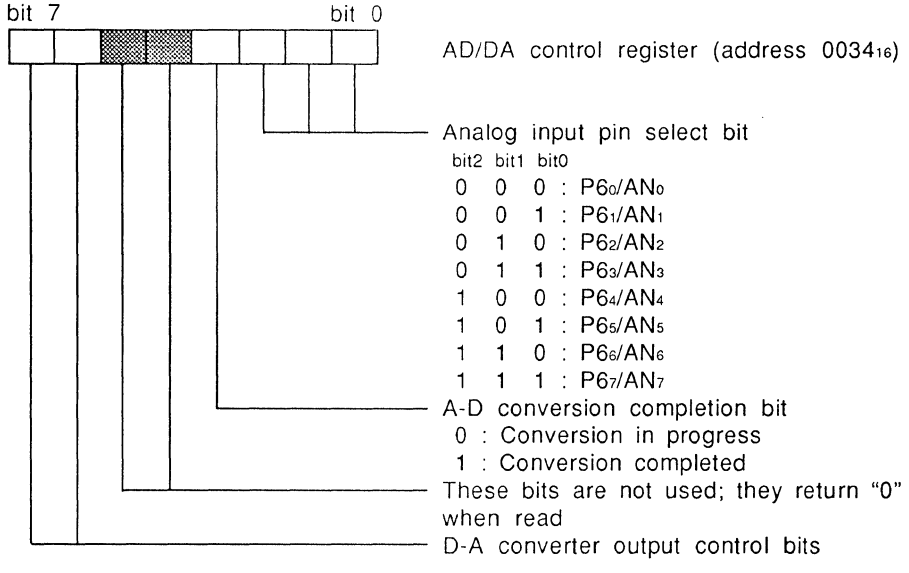
(2) AD/DA control register

Select bits for the analog input pins are allocated to the low-order three bits of the AD/DA control register. In the M38063M6-XXXFP/GP, these analog input select bits can be used to select an analog input pin. Note that the analog input pins also act as port P6, so they can also be used as ordinary input ports.

Bit 3 of the AD/DA control register is the A-D conversion completion bit—A-D conversion starts when "0" is written to this bit.

At reset, all the bits of the AD/DA control register (except bit 3) are cleared to "0". Bit 3 is set to "1".

Table 2.9.1 Structure of AD/DA Control Register



(3) Comparison voltage generator

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} by 256, and outputs the divided voltage.

(4) Channel selector

The channel selector selects one of the ports $P6_0/AN_0$ to $P6_7/AN_7$, and inputs its voltage to the comparator.

(5) Comparator and control circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage then store the result in the A-D conversion register. When A-D conversion is complete, the control circuit sets the A-D conversion completion bit and the A-D conversion interrupt request bit (bit 6 of address $003D_{16}$) to "1".

Note that the comparator is linked to a capacitor, so set $f(X_{IN})$ to at least 500kHz during A-D conversion.

2.9.2 Method of use

The A-D conversion method is described below.

(1) If using A-D interrupts, clear the A-D interrupt request bit (bit 6 of address $003D_{16}$) to "0", then set the A-D interrupt enable bit (bit 6 of address $003F_{16}$) to "1" and clear the interrupt disable flag to "0".
(2) Select an analog input pin by setting the analog input pin select bits of the AD/DA control register.
(3) Clear the A-D conversion completion bit to "0". This write operation starts the A-D conversion. Remember not to read the A-D conversion register during the A-D conversion.
(4) Verify the completion of the conversion from the status of the A-D conversion completion bit—if this bit is "1", conversion is complete.
(5) Read the A-D conversion register to obtain the conversion result.

2.9.3 Operation

A-D conversion starts when "0" is written to the A-D conversion completion bit. Operations within the M38063M6-XXXFP/GP during the A-D conversion are described below.

(1) When A-D conversion starts, the A-D conversion register is cleared to "00_{16}".
(2) Next, the most significant bit of the A-D conversion register is set to "1", and the comparison voltage Vref is input to the comparator. At this point, the analog input voltage V_{IN} is compared with Vref.
(3) If the result of the comparison is Vref < V_{IN}, the most significant bit of the A-D conversion register remains at "1" as set. If Vref > V_{IN}, the most significant bit is cleared to "0".

The A-D converter repeats the above steps down to the least significant bit of the A-D conversion register, to convert the analog value into a digital value. The A-D conversion ends 50 clock cycles (20μs, when f(X_{IN}) = 5MHz) after it starts, and the conversion result is stored in the A-D conversion register. An A-D interrupt request is generated at the same time that the A-D conversion ends, and the A-D interrupt request bit is set to "1".

Relationship between Vref and V_{REF}
When n = 0 : Vref = 0
When n =1 to 255 : Vref = $V_{REF}/256 \times (n - 0.5)$
n : Value in the A-D conversion register (decimal notation)

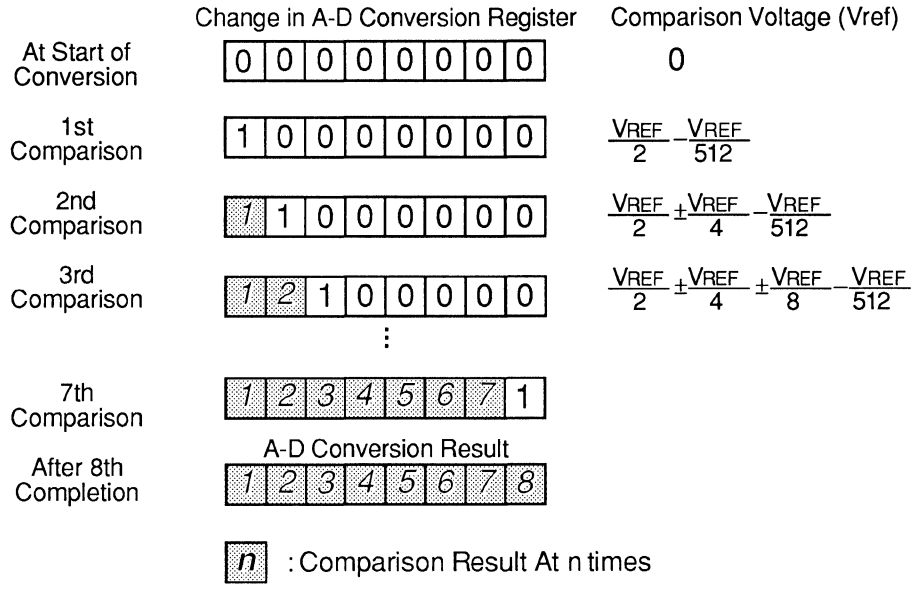


Fig. 2.9.2 Changes in A-D Conversion Register during A-D Conversion

2.9.4 Equivalent circuit

An equivalent connection circuit of the A-D converter is shown in Figure 2.9.3, and a timing chart of A-D conversion is shown in Figure 2.9.4.

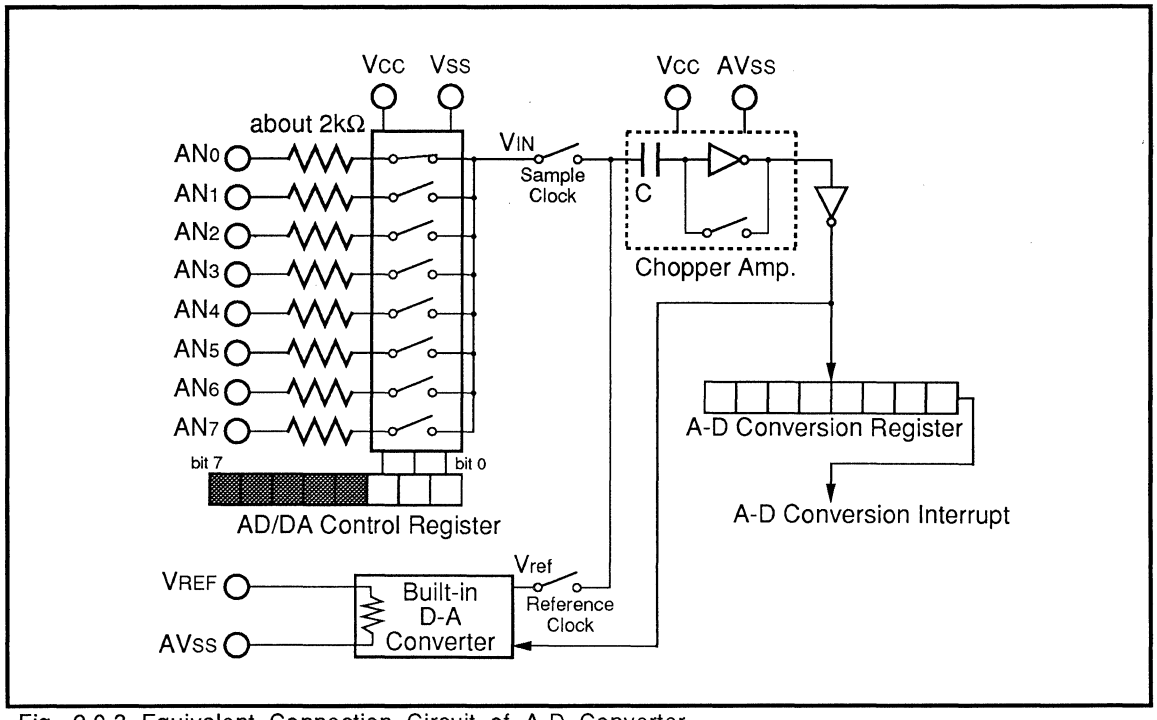


Fig. 2.9.3 Equivalent Connection Circuit of A-D Converter

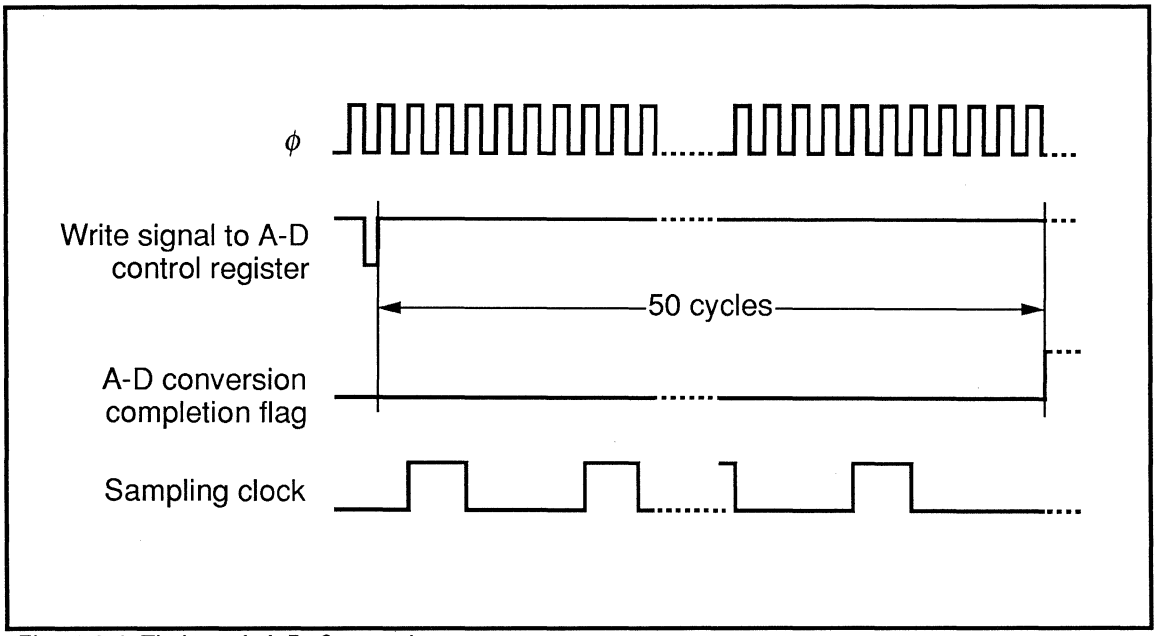


Fig. 2.9.4 Timing of A-D Conversion

2.10 D-A Converter

The D-A converter built into the M38063M6-XXXFP/GP has the following characteristics:

- Analog output pins : 2 channels
- Conversion method : R–2R network
- Resolution : 8 bits

A block diagram of the D-A converter is shown in Figure 2.10.1.

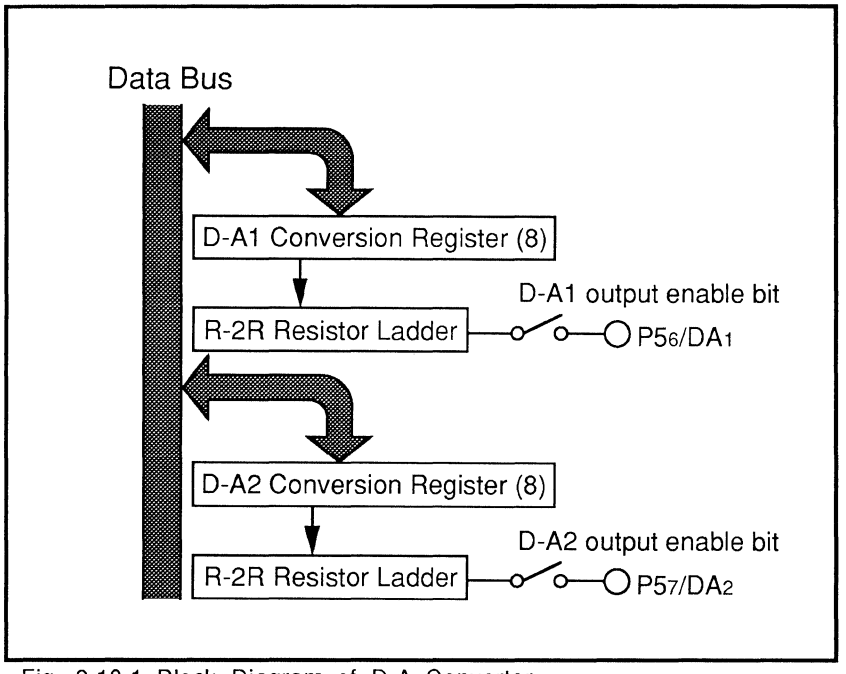


Fig. 2.10.1 Block Diagram of D-A Converter

2.10.1 Block description

The blocks of the D-A converter are described below.

(1) D-A conversion register

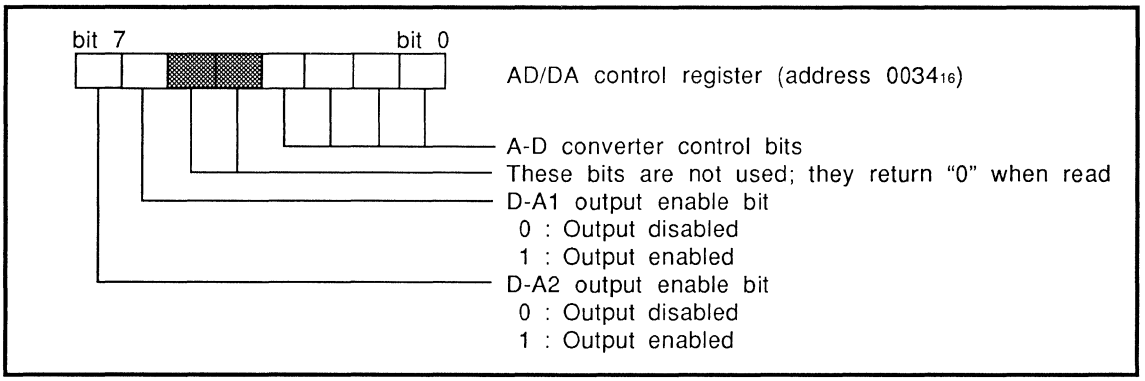
When a digital value is set in this register, the digital value is converted into an analog voltage.

(2) AD/DA control register

D-A output enable bits are allocated to bits 6 and 7 of the AD/DA control register. Set one of these bits to "1" to enable D-A output from the corresponding channel.

At reset, these bits are cleared to "0", disabling D-A output.

Table 2.10.1 Structure of AD/DA Control Register



2.10.2 Method of use

Set the M38063M6-XXXFP/GP as follows when using D-A conversion:

(1) Set the pin to be used for D-A output to input status by setting the direction register of the pin to "0". (The DA_1 and DA_2 pins can also be used as ports $P5_6$ and $P5_7$.)

(2) Set the D-A output enable bit of the AD/DA control register to enabled.

When the above setting is complete, write a value to the D-A conversion register. An analog voltage equivalent to the written value will be output from the DA_1 or DA_2 pin.

2.10.3 Operation

The D-A converter divides the voltage between V_{REF} and AV_{SS}, and outputs an analog voltage equivalent to the digital value written into one of the D-A conversion registers. The conversion result is output from the DA pin whose D-A output enable bit is set to "1" in the AD/DA control register. The D-A1 conversion register corresponds to the DA_1 pin, and the D-A2 conversion register corresponds to the DA_2 pin.

The relationship between analog voltage and digital value is shown below.

Relationship between analog voltage and digital value

$V = V_{REF} \times n/256$ (n = 0 to 255)

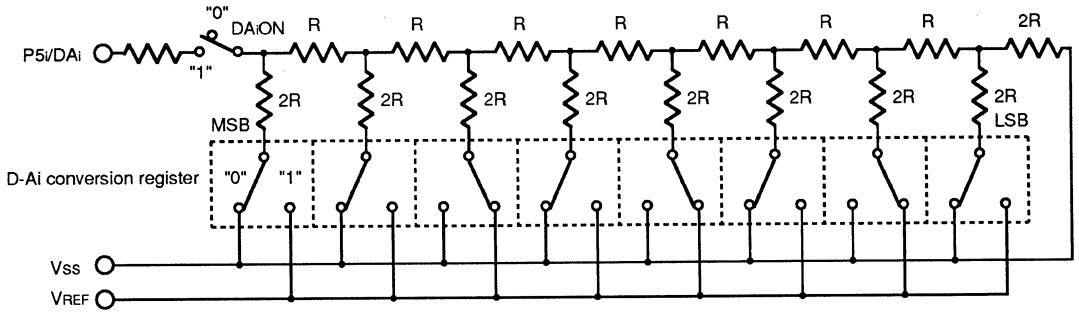
V : Output voltage

V_{REF} : Reference voltage

n : Value in D-A conversion register (decimal notation)

At reset, both of the D-A1 and D-A2 conversion registers are reset to "00_{16}", so the voltages output from the DA_1 and DA_2 pins after a reset are at the same potential as AV_{SS}.

An equivalent connection circuit of the D-A converter is shown in Figure 2.10.2. The D-A1 and D-A2 conversion registers have the same structure. Note that a resistance ladder output is connected directly to each of the DA pins, so an external buffer amplifier must be used.



This figure shows the case in which the value in the D-A1 conversion register is "$2A_{16}$"

Fig. 2.10.2 Equivalent Connection Circuit of D-A Converter

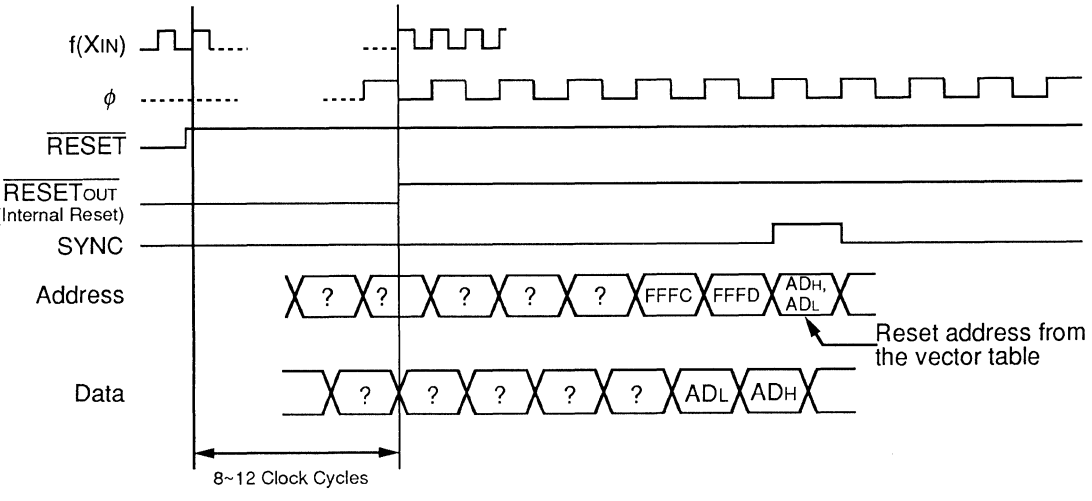
2.11 Reset

2.11.1 Reset description

The M38063M6-XXXFP/GP is reset if the $\overline{\text{RESET}}$ pin is held at a "L" level for 2μs after the oscillator has stabilized, while the supply voltage is 4.0 to 5.5V. When the $\overline{\text{RESET}}$ pin returns to a "H" level, the reset status is released in the sequence shown in Figure 2.11.1.

After the reset is released, the M38063M6-XXXFP/GP starts executing the current program at the address contained in addresses $FFFD_{16}$ and $FFFC_{16}$. The high-order byte of the address is contained in address $FFFD_{16}$ and the low-order byte of the address is contained in address $FFFC_{16}$.

The internal status of the microcomputer after a reset is shown in Figure 2.11.2. The contents of all bits, registers, and RAM not specified in this figure are undefined after a reset, so they must be initialized in software.



Note 1: The frequency relation of f(XIN) and ϕ is f(XIN) = 2 • ϕ .
Note 2: The "?" means that the address is changing depending upon the previous state.

Fig. 2.11.1 Internal Processing Sequence after Reset

	Address	Register contents
Port P0 direction register	0001_{16}	00_{16}
Port P1 direction register	0003_{16}	00_{16}
Port P2 direction register	0005_{16}	00_{16}
Port P3 direction register	0007_{16}	00_{16}
Port P4 direction register	0009_{16}	00_{16}
Port P5 direction register	$000B_{16}$	00_{16}
Port P6 direction register	$000D_{16}$	00_{16}
Port P7 direction register	$000F_{16}$	00_{16}
Port P8 direction register	0011_{16}	00_{16}
Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 0
Serial I/O1 control register	$001A_{16}$	00_{16}
UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
Serial I/O2 control register	$001D_{16}$	0 0 0 0 0 0 0 0
Prescaler 12	0020_{16}	FF_{16}
Timer 1	0021_{16}	01_{16}
Timer 2	0022_{16}	FF_{16}
Timer XY mode register	0023_{16}	00_{16}
Prescaler X	0024_{16}	FF_{16}
Timer X	0025_{16}	FF_{16}
Prescaler Y	0026_{16}	FF_{16}
Timer Y	0027_{16}	FF_{16}
AD/DA control register	0034_{16}	0 0 0 0 1 0 0 0
D-A1 conversion register	0036_{16}	00_{16}
D-A2 conversion register	0037_{16}	00_{16}
Interrupt edge selection register	$003A_{16}$	00_{16}
CPU mode register	$003B_{16}$	0 0 0 0 0 0 * 0
Interrupt control register1	$003E_{16}$	00_{16}
Interrupt control register2	$003F_{16}$	00_{16}
Processor status register	(PS)	1
Program counter	(PC_H)	Contents of address $FFFD_{16}$
	(PC_L)	Contents of address $FFFC_{16}$

* = CM1. The initial value of CM1 depends on the level of the CNVss pin.

Fig. 2.11.2 Internal Status of Microcomputer after Reset Release

2.11.2 Reset circuit

Design the reset circuit in such a way that the reset input voltage falls below 0.8V when the power supply voltage rises above 4.0V, as shown in Figure 2.11.3. Make sure that reset is released after oscillation has time to stabilize.

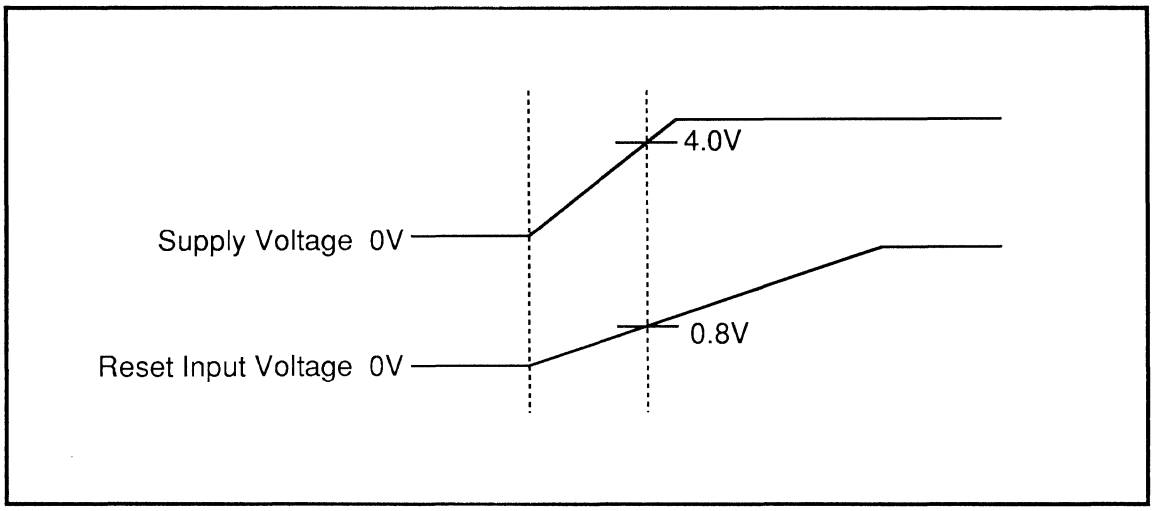


Fig. 2.11.3 Power-on Reset Condition

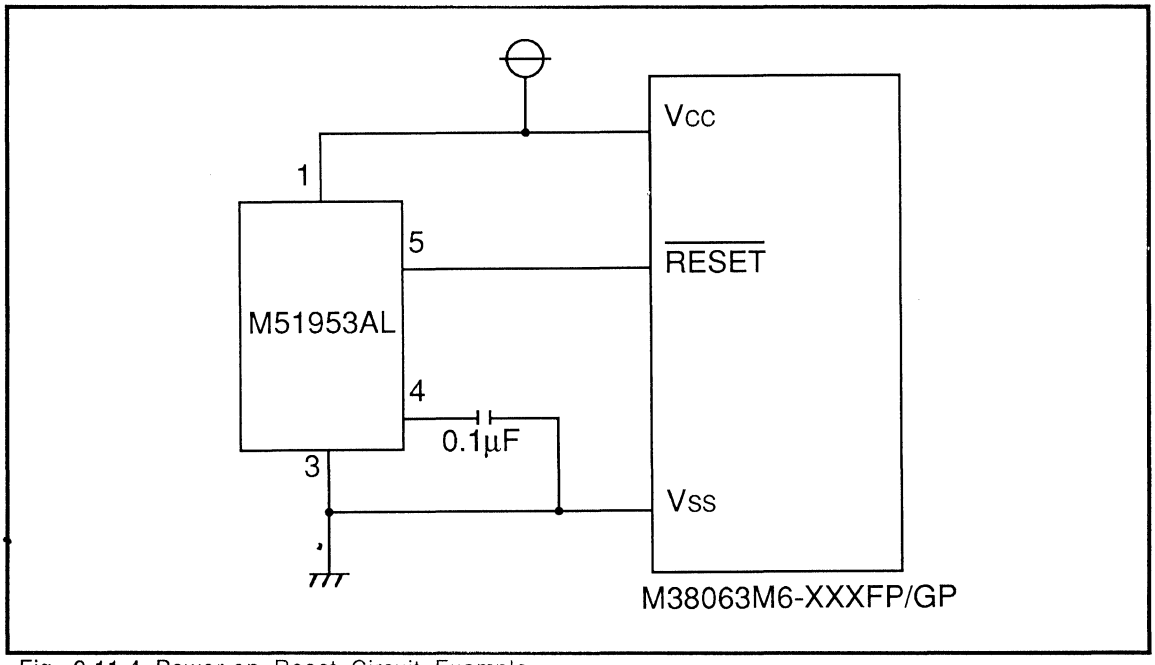


Fig. 2.11.4 Power-on Reset Circuit Example

2.12 Oscillation Circuit

2.12.1 Circuit description

The M38063M6-XXXFP/GP has a built-in oscillation circuit which generates the clock signals. This built-in oscillation circuit consists of an oscillation gate which acts as an amplifier and an oscillation control pre-amplifier block which controls the oscillation.

A block diagram of the M38063M6-XXXFP/GP's oscillation circuit is shown in Figure 2.12.1.

The frequency input to the clock input pin X_{IN} is normally divided by two to give the internal clock ϕ. Connect either a ceramic resonator or a quartz crystal to the outside of this circuit.

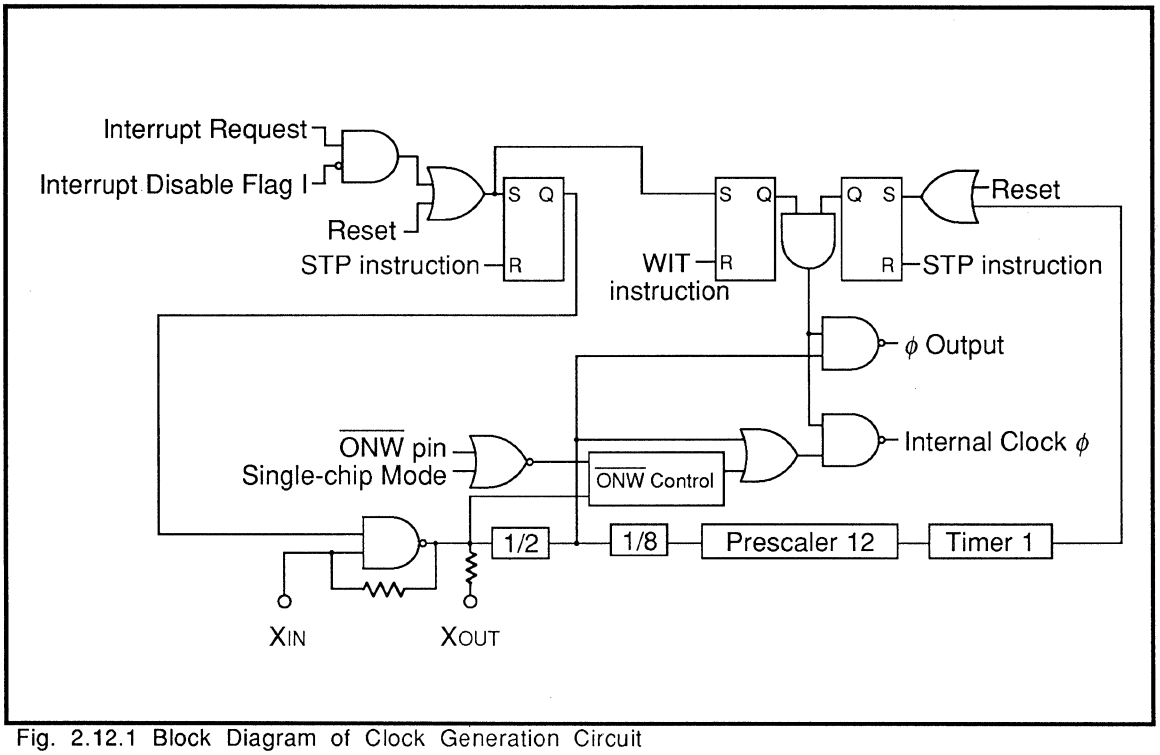


Fig. 2.12.1 Block Diagram of Clock Generation Circuit

(1) Oscillation circuit using ceramic resonator or quartz crystal

Examples of circuits using a ceramic resonator or quartz crystal are shown in Figures 2.12.2, and 2.12.3. As shown in these figures, an oscillation circuit can be formed by connecting a resonator between XIN and XOUT. Set the capacitors (CIN, COUT, etc.) in accordance with the resonator manufacturer's recommended values.

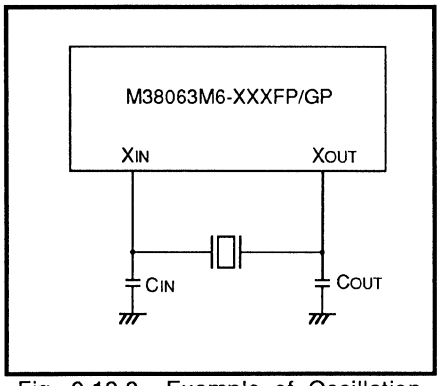


Fig. 2.12.2 Example of Oscillation Circuit

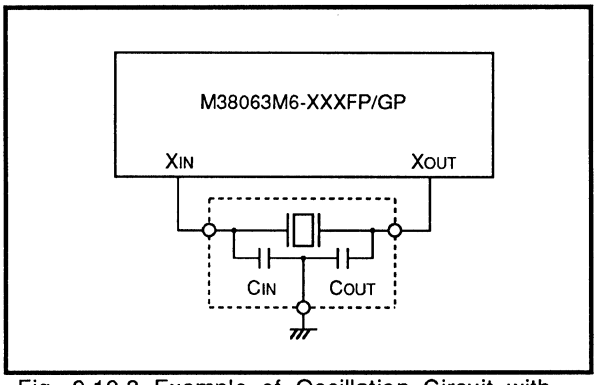


Fig. 2.12.3 Example of Oscillation Circuit with Internal Capacitors

(2) External clock input circuit

An external clock signal can also be applied to the M38063M6-XXXFP/GP. An example of the circuit to be used in this case is shown in Figure 2.12.4. Leave the XOUT pin open.

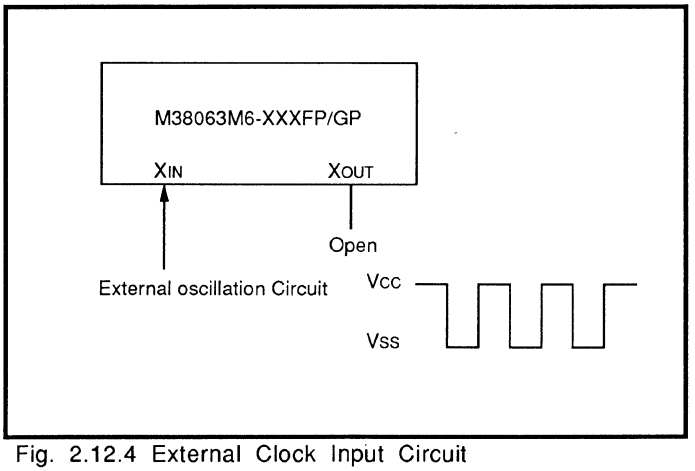


Fig. 2.12.4 External Clock Input Circuit

2.12.2 Oscillation control

In the M38063M6-XXXFP/GP, oscillation can be stopped and restarted as required.

(1) Stop mode

If the STP instruction is executed, oscillation stops with the internal clock ϕ at "H" (stop mode). The functions operating in stop mode are listed in Table 2.12.1.

In stop mode, the contents of all registers except timer 1 and prescaler 12 are held. This function ensures that operations can restart with exactly the same status. Placing the chip in stop mode greatly reduces power dissipation.

The internal operation after the STP instruction is executed is as follows:

1. Oscillation stops with the internal clock ϕ at "H".
2. Timer 1 is set to "01_{16}" and prescaler 12 is set to "FF_{16}".

Table 2.12.1 Functions Operating in Stop Mode

Timers	Timer X and timer Y can be used, but only in event counter mode (timer X and timer Y interrupts can be used)
Serial I/O	The BRG is stopped, but the serial I/O functions can operate in external clock mode (transmit and receive interrupts can be used)
A-D converter	Stopped (A-D conversion interrupts cannot be used)
D-A converter	Analog output voltage is held
External pin interrupts	Enabled

To restart oscillation (recover from stop mode), either cause a reset or an interrupt. If an interrupt is used for restart, prescaler 12 and timer 1 start operating. After timer 1 overflows, the internal clock ϕ starts. This provides the time necessary for oscillation to stabilize, if a ceramic resonator or quartz crystal is used.

Make the following preparation immediately before executing the STP instruction:

1. Disable the timer 1 interrupt. (Set the timer 1 interrupt enable bit to "0").
2. Enable the interrupt to be used for wake-up (set the corresponding interrupt enable bit to "1" and the interrupt disable flag to "0").

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at "H", but the oscillator itself does not stop (wait mode). The functions operating in wait mode are listed in Table 2.12.2.

Recovery from wait mode is done in the same way as recovery after the STP instruction. However, since there is no need to provide time to enable the oscillation to stabilize, operation can start immediately.

Table 2.12.2 Functions Operating in Wait Mode

Timers	Operating (timer 1, timer 2, timer X, and timer Y interrupts can be used)
Serial I/O	Operating (transmit and receive interrupts can be used)
A-D converter	Stopped (A-D conversion interrupts cannot be used)
D-A converter	Analog output voltage is held
External pin interrupts	Enabled

CHAPTER 3

INTERNAL PROM VERSION

3.1 Function Description

In addition to the mask ROM versions of the M38063M6-XXXFP/GP, there are internal programmable ROM versions which are microcomputers with built-in programmable ROM. The EPROM version has an internal EPROM that can be written to and can also be erased. The one-time programmable microcomputer contains an internal PROM which can be written to but can not be erased. The functions of the internal EPROM and one-time programmable versions are exactly the same, apart from the erasability of the ROM. Both are referred to as internal PROM versions in this manual. The internal PROM versions have functions similar to those of the mask ROM versions, but they also have a PROM mode that enables writing to internal PROM.
The various types of internal PROM versions are listed in Table 3.1.1, and their functions are listed in Table 3.1.2.

Table 3.1.1 Internal PROM Version Types

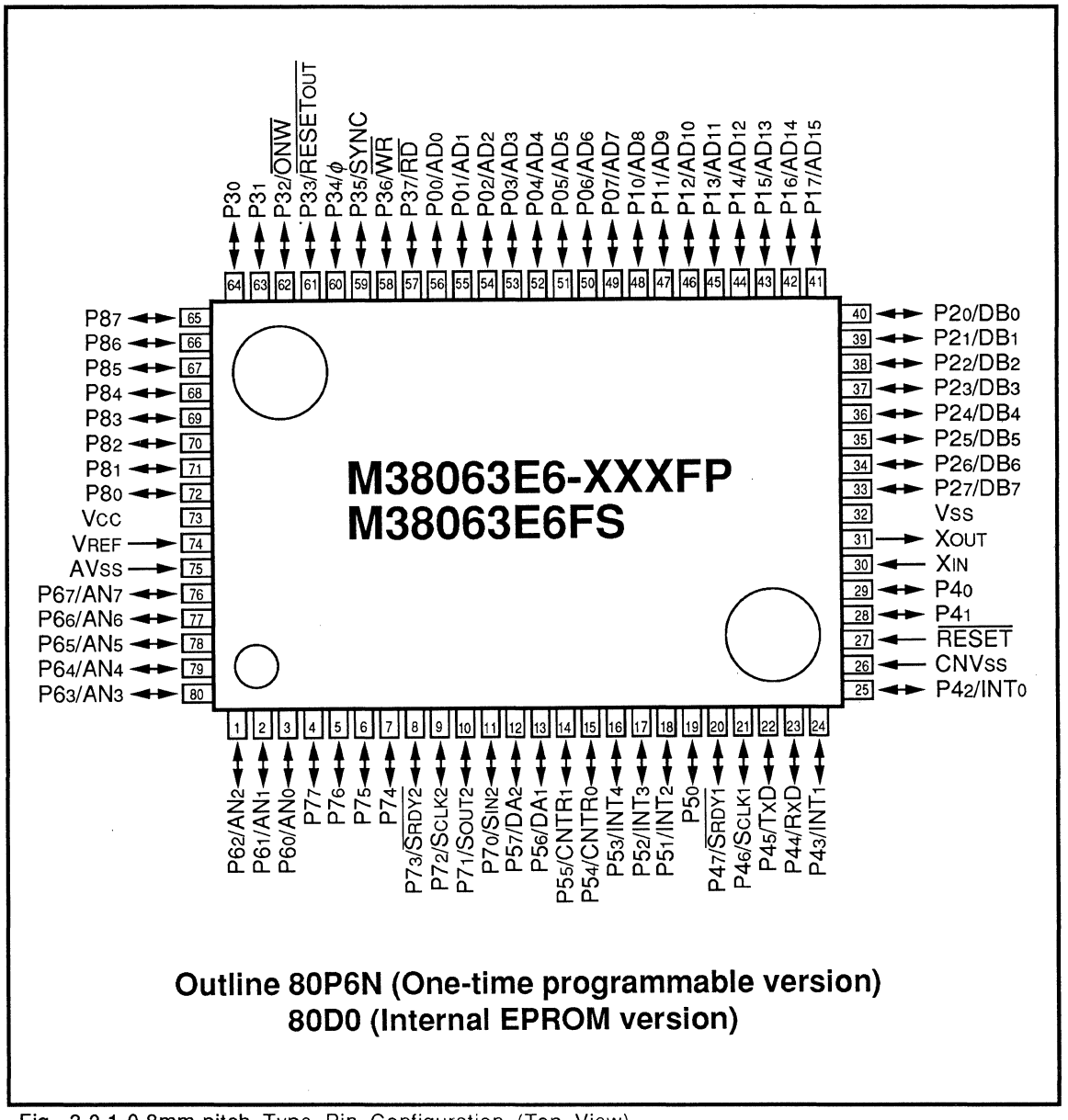
Type name	PROM	RAM	Package	Remarks
M38063E6-XXXFP	24K bytes	512 bytes	0.8mm-pitch QFP	
M38063E6-XXXGP	24K bytes	512 bytes	0.65mm-pitch QFP	
M38063E6FP	24K bytes	512 bytes	0.8mm-pitch QFP	shipped blank
M38063E6GP	24K bytes	512 bytes	0.65mm-pitch QFP	shipped blank
M38063E6FS	24K bytes	512 bytes	0.8mm-pitch LCC	EPROM version

Table 3.1.2 Functions of Internal PROM Version

Parameter		Function
Basic instructions		71
Instruction execution time		0.8μs (shortest instruction, at 5HMz oscillation frequency)
Oscillation frequency		5MHz (max.)
Memory size	PROM	24,316 bytes of user area
	RAM	512 bytes
Input/output ports	P0~P6,P8	8-bit × 8 (CMOS output)
	P7	8-bit × 1 (N-channel open drain output)
Serial I/O1		Clock synchronous or asynchronous
Serial I/O2		Clock synchronous
Timers		8-bit prescaler × 3 and 8-bit timer × 4
A-D converter		8-bit resolution × 8 channels
D-A converter		8-bit resolution × 2 channels
Interrupts		7 external, 8 internal, 1 software
Clock generation circuit		Built-in (connect to external ceramic resonator or quartz crystal oscillator)
Supply voltage		4.0 to 5.5V
Power dissipation		20mW (at 5MHz oscillation frequency, typ.)
Input/output characteristics	Input/output breakdown voltage	5V
	Output current	10mA
External memory expansion		Possible
Operating temperature range		−20 to 85°C
Device structure		CMOS silicon gate

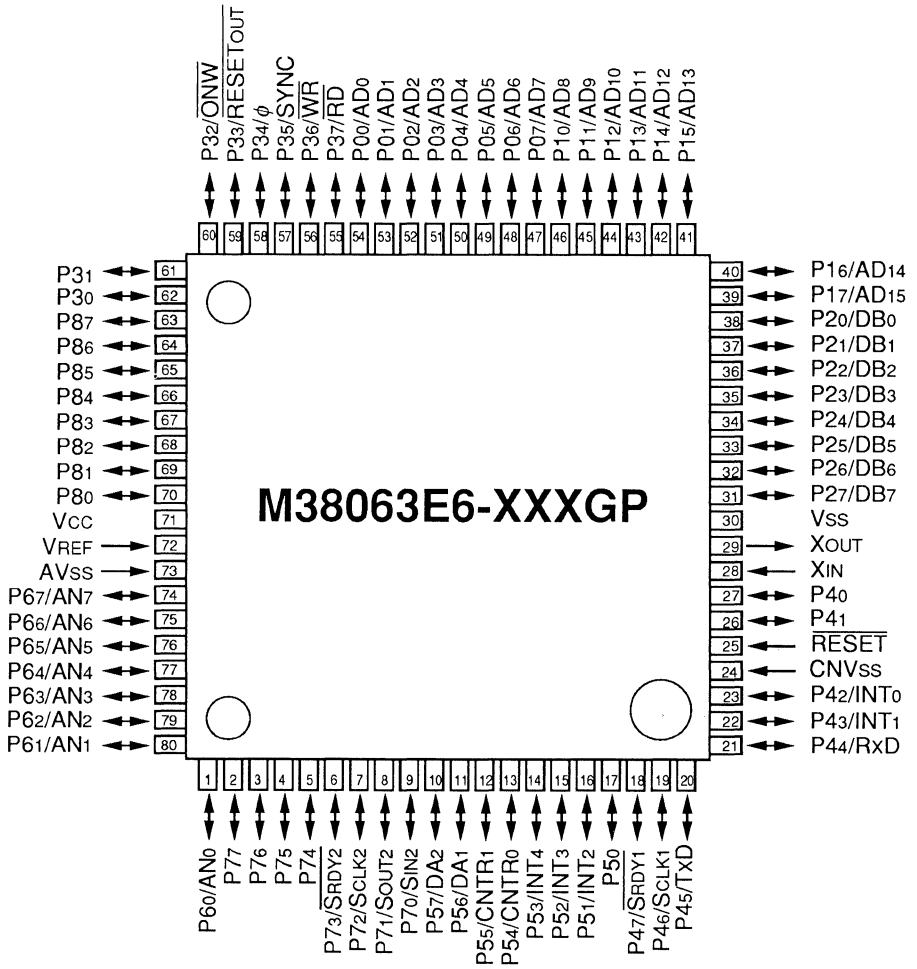
3.2 Pin Configuration

The pin configuration of the 0.8mm-pitch type is shown in Figure 3.2.1 and that of the 0.65mm-pitch type is shown in Figure 3.2.2.
Internal PROM version is pin compatible with mask ROM version.



Outline 80P6N (One-time programmable version)
80D0 (Internal EPROM version)

Fig. 3.2.1 0.8mm-pitch Type Pin Configuration (Top View)



Outline 80P6S (One-time programmable version)

Fig. 3.2.2 0.65mm-pitch Type Pin Configuration (Top View)

3.3 Functional Block Diagram

A block diagram of M38063E6-XXXFP is shown in Figure 3.3.1.

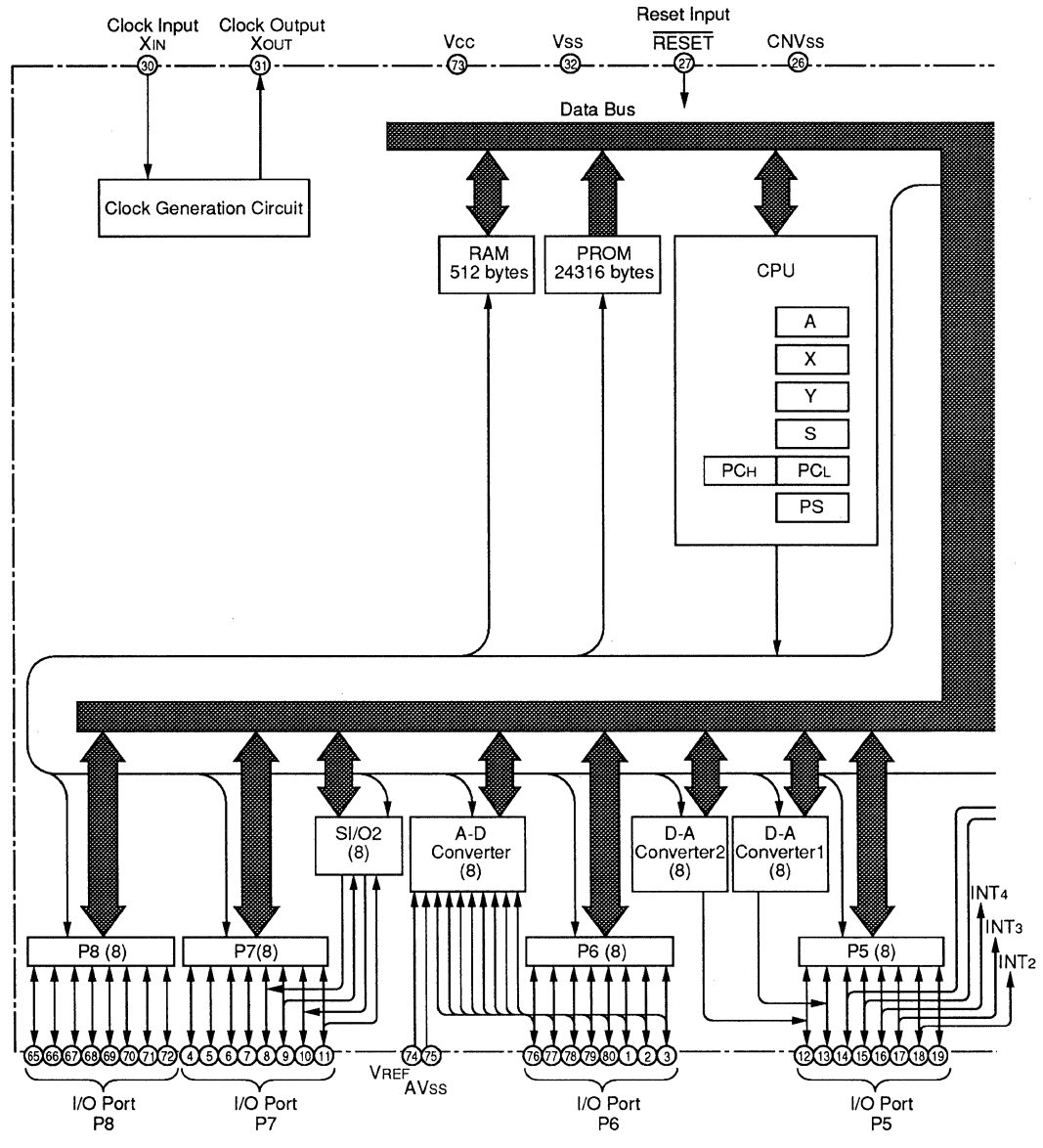
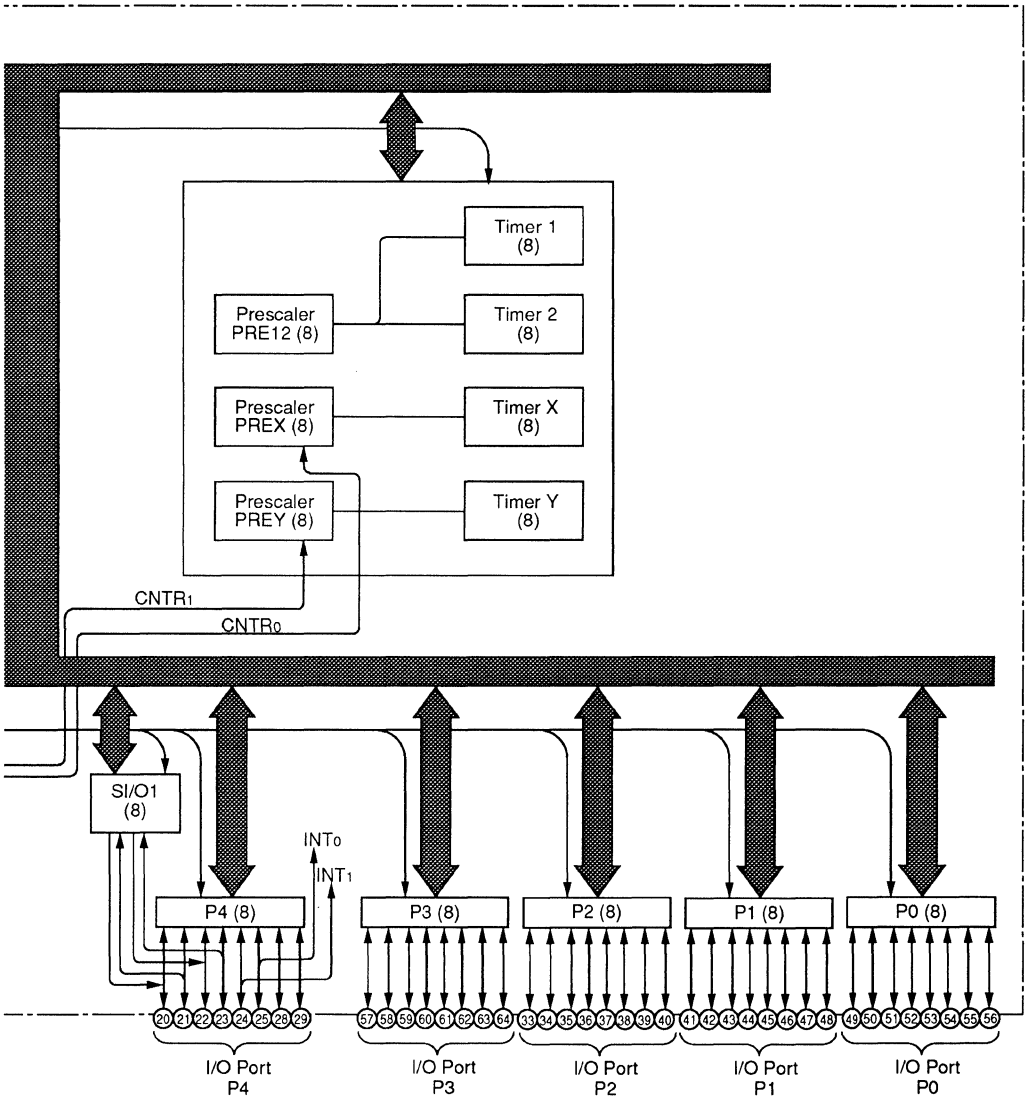


Fig. 3.3.1 Functional Block Diagram of Internal PROM Version


Timer 1
(8)
Prescaler
PRE12 (8)
Timer 2
(8)
Prescaler
PREX (8)
Timer X
(8)
Prescaler
PREY (8)
Timer Y
(8)
CNTR1
CNTR0
SI/O1
(8)
INT0
INT1
P4 (8)
P3 (8)
P2 (8)
P1 (8)
P0 (8)
20 21 22 23 24 25 28 29
57 58 59 60 61 62 63 64
33 34 35 36 37 38 39 40
41 42 43 44 45 46 47 48
49 50 51 52 53 54 55 56
I/O Port
P4
I/O Port
P3
I/O Port
P2
I/O Port
P1
I/O Port
P0

3.4 PROM Mode

3.4.1 PROM mode

The internal PROM versions of the M38063M6-XXXFP/GP have a PROM mode in addition to the ordinary operating mode.

The PROM mode is used to write to and read from internal PROM. In PROM mode, a write adapter can be used with a general-purpose PROM writer to write to or read from the internal PROM as if it were a M5M27C256K. Write adapters are listed in Table 3.4.1.

Table 3.4.1 Write Adapters

Microcomputer type name	Name of write adapter
M38063E6FP	PCA4738F-80
M38063E6GP	PCA4738G-80
M38063E6FS	PCA4738L-80

3.4.2 Notes on writing and reading

(1) Use a programming voltage of 12.5V.

(2) During writing and reading with write adapter PCA4738F-80, PCA4738G-80, or PCA4738L-80, set switches SW1, SW2, and SW3 to "off".

(3) Addresses $A080_{16}$ to $FFFD_{16}$ of internal PROM correspond to addresses 2080_{16} to $7FFD_{16}$ on a PROM writer. Addresses 0000_{16} to $207F_{16}$, $7FFE_{16}$, and $7FFF_{16}$ on a PROM writer cannot be written to or read from correctly, so limit the PROM writer area to the range from 2080_{16} to $7FFD_{16}$.

Note that addresses $A000_{16}$ to $FFFF_{16}$ (addresses 2000_{16} to $7FFF_{16}$ on a PROM writer) can be written to and read from correctly, except in the internal EPROM versions.

3.4.3 Erasure

Only the internal EPROM version has an erasure window on the top surface of the package. To erase the EPROM, shine an ultraviolet light source of wavelength 2537Å onto the window for a minimum dose of 15W·s/cm².

3.4.4 Notes on handling

(1) Sunlight and fluorescent light include wavelengths which will erase an EPROM. Unless the internal EPROM version is being erased, cover the transparent glass window with a light-proof seal.

(2) Mitsubishi provides light-proof seals designed to cover the transparent glass window of the internal EPROM version. Make sure that the seal does not touch the pins of the microcomputer.

(3) Before erasing the EPROM version, clean the transparent glass window. Oil from fingers and glue may hinder the transmission of ultraviolet light and adversely affect erasure.

(4) Insure that excessive voltages are not used when writing.
Pay particular attention when turning on the power source.

(5) Mitsubishi does not test or screen any writing to PROM in the M38063E6-XXXFP/GP after it has left the factory. To improve reliability after writing, we recommend that the M38063E6-XXXFP/GP is written to and tested in the sequence shown in Figure 3.4.1.

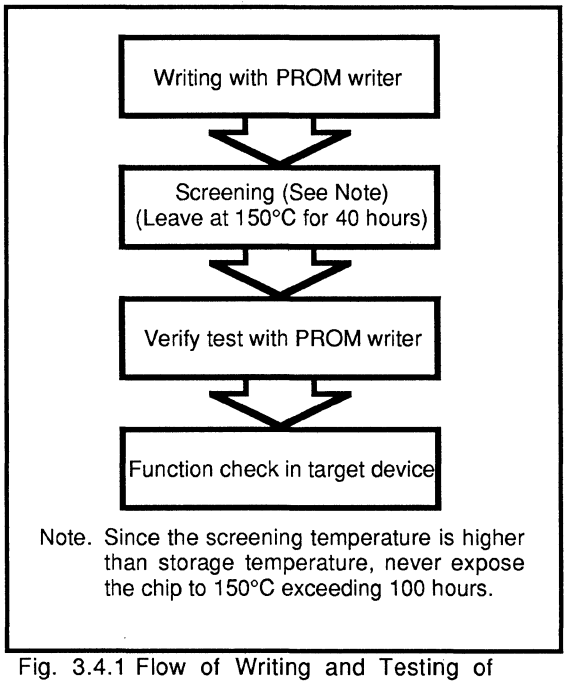


Fig. 3.4.1 Flow of Writing and Testing of One-Time Programmable Versions

CHAPTER 4

APPLICATIONS

4.1 Application Circuit Examples

Since the M38063M6-XXXFP/GP has 72 I/O ports, it can be used alone to construct a system that would conventionally need two microcomputers. Its two built-in serial I/O functions enable its use as master microcomputer in a system which makes use of a number of microcomputers, and its large memory capacity (24K bytes of ROM and 512 bytes of RAM) enables its use in a wide range of applications. Some of these applications are described below.

4.1.1 CD player system

An example of a CD player system which uses the M38063M6-XXXFP is shown in Figure 4.1.1. This system also uses a CD LSI kit produced by Mitsubishi, with the M38063M6-XXXFP controlling the CD LSIs and the display functions. Display is on a 7×5 dot, 16-digit dot matrix fluorescent panel (FLD), using the M66004SP/FP as a driver. The M38063M6-XXXFP is used in memory expansion mode, connected to 256K bits of SRAM which store disk information and programs. The built-in A-D converter of the M38063M6-XXXFP is used to provide level search for disk playback—the results of A-D conversion determine the recording (playback) level. An electronic voltage controlled amplifier is controlled by the D-A converter. By storing Table-of-Contents data in the internal RAM, a wide variety of functions such as high-speed access and disk editing can be implemented.

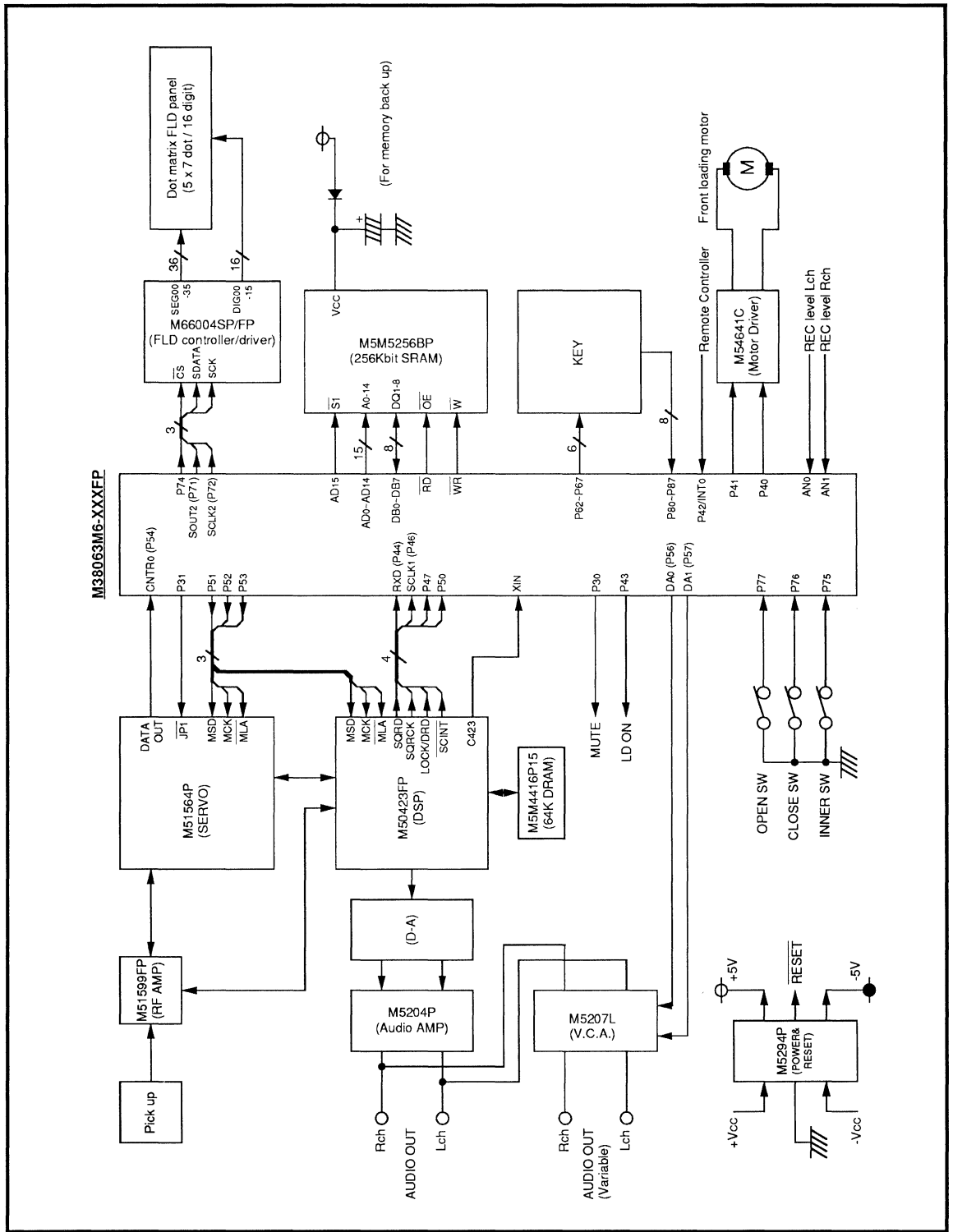


Fig. 4.1.1 Example of CD Player System

4.1.2 VCR system controller

An example of a VCR system controller which uses the M38063M6-XXXFP is shown in Figure 4.1.2. The M38063M6-XXXFP has two built-in serial I/O channels—in this system, one channel is used for serial communications with a timer microcontroller and the other is used for serial communications with a servo IC.

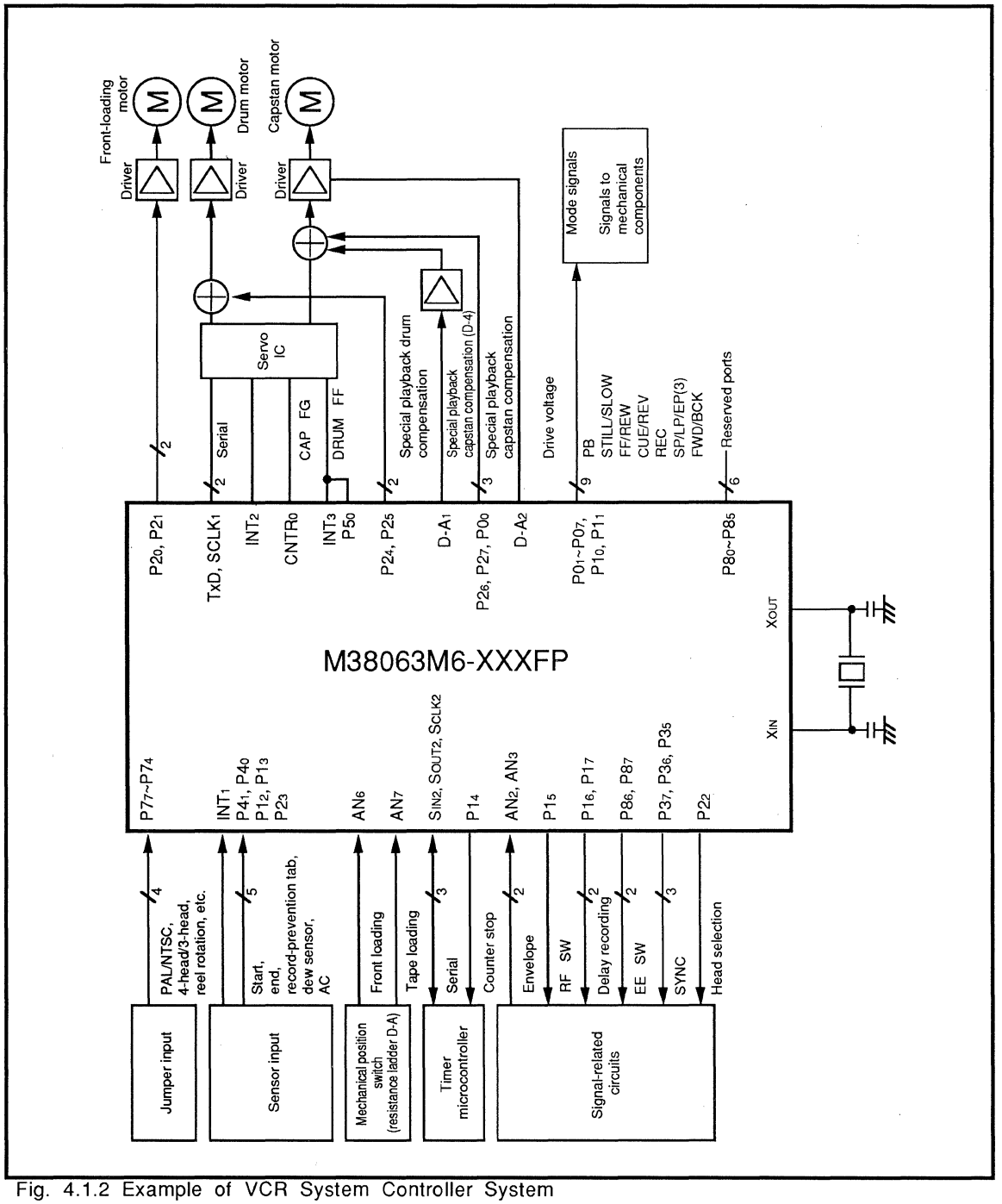


Fig. 4.1.2 Example of VCR System Controller System

CHAPTER 5

ELECTRICAL CHARACTERISTICS

5.1 Electrical Characteristics

5.1.1 Absolute maximum ratings

Absolute Maximum Ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage		All voltages measured with reference to the V_{SS} pin, output transistors isolated.	-0.3~7.0	V
V_I	Input voltage	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, V_{REF}		-0.3~V_{CC}+0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		-0.3~V_{CC}+0.3	V
V_I	Input voltage	CNV_{SS}		-0.3~13	V
V_O	Output voltage	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, X_{OUT}		-0.3~V_{CC}+0.3	V
Pd	Power dissipation		Ta=25°C	500	mW
Topr	Operating temperature			-20~85	°C
Tstg	Storage temperature			-40~125	°C

5.1.2 Recommended operating conditions

Recommended Operating Conditions (V_{CC} = 4.0 to 5.5V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power supply voltage		4.0	5.0	5.5	V
V_{SS}	Power supply voltage			0		V
V_{REF}	Analog reference voltage (when A-D converter is used)		2.0		V_{CC}	V
	Analog reference voltage (when D-A converter is used)		4.0		V_{CC}	V
AV_{SS}	Analog power supply voltage			0		V
V_{IA}	Analog input voltage	AN_0~AN_7	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$,X_{IN},CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage	CNV_{SS}	0		0.2V_{CC}	V
ΣI_{OH1}(peak)	"H" peak output total current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P8_0$~$P8_7$			-80	mA
ΣI_{OH2}(peak)	"H" peak output total current	$P4_0$~$P4_7$,$P5_0$~$P5_7$,$P6_0$~$P6_7$			-80	mA
ΣI_{OL1}(peak)	"L" peak output total current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P8_0$~$P8_7$			80	mA
ΣI_{OL2}(peak)	"L" peak output total current	$P4_0$~$P4_7$,$P5_0$~$P5_7$,$P6_0$~$P6_7$, $P7_0$~$P7_7$			80	mA
ΣI_{OH1}(avg)	"H" average output total current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P8_0$~$P8_7$ (Note 1)			-40	mA
ΣI_{OH2}(avg)	"H" average output total current	$P4_0$~$P4_7$,$P5_0$~$P5_7$,$P6_0$~$P6_7$ (Note 1)			-40	mA
ΣI_{OL1}(avg)	"L" average output total current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P8_0$~$P8_7$ (Note 1)			40	mA
ΣI_{OL2}(avg)	"L" average output total current	$P4_0$~$P4_7$,$P5_0$~$P5_7$,$P6_0$~$P6_7$, $P7_0$~$P7_7$ (Note 1)			40	mA
I_{OH}(peak)	"H" peak output current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$			-10	mA
I_{OL}(peak)	"L" peak output current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$			10	mA
I_{OH}(avg)	"H" average output current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ (Note 1)			-5	mA
I_{OL}(avg)	"L" average output current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ (Note 1)			5	mA
f(X_{IN})	Internal clock oscillation frequency				5	MHz

Note 1 : The average output currents are average values measured over 100ms.

5.1.3 Electrical characteristics

Electrical Characteristics (V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P8_0$~$P8_7$ (Note 2)	I_{OH}=-10mA	Vcc-2.0			V
V_{OL}	"L" output voltage	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$	I_{OL}=10mA			2.0	V
V_{T+}-V_{T-}	Hysteresis	$CNTR_0$,$CNTR_1$,INT_0~INT_4			0.4		V
V_{T+}-V_{T-}	Hysteresis	RxD,SCLK			0.5		V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	"H" input current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$	V_I=Vcc			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$,CNV_{SS}	V_I=Vcc			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I=Vcc		4		µA
I_{IL}	"L" input current	$P0_0$~$P0_7$,$P1_0$~$P1_7$,$P2_0$~$P2_7$, $P3_0$~$P3_7$,$P4_0$~$P4_7$,$P5_0$~$P5_7$, $P6_0$~$P6_7$,$P7_0$~$P7_7$,$P8_0$~$P8_7$ $\overline{RESET}$,CNV_{SS}	V_I=Vss			-5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I=Vss		-4		µA
V_{RAM}	RAM retention voltage		Clock is stopped	2.0		5.5	V
I_{CC}	Power supply current (Note 3)	f(X_{IN})=5MHz			4	8	mA
		f(X_{IN})=5MHz (wait mode)			1		mA
		With all oscillation stopped (stop mode)	Ta=25°C		0.1	1	µA
			Ta=85°C			10	

Note 2 : $P4_5$ is measured when the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".

Note 3 : Not including the current flowing through the V_{REF} pin. The A-D converter has completed conversion. Output transistors isolated.

5.1.4 A-D converter characteristics

A-D Converter Characteristics (V_{CC} = 4.0 to 5.5V, V_{SS} = AV_{SS} = 0V, V_{REF} = 2.0V to V_{CC}, Ta= −20 to 85°C, $f(X_{IN})$ = 5MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limit			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (disregarding quantization error)			±1	±2.5	LSB
t_{CONV}	Conversion time				50	$tc(\phi)$
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power supply input current	(Note 4)	50	150	200	µA
$I_{I(AD)}$	A-D port input current			0.5		µA

Note 4 : When D-A conversion registers (addresses 0036_{16} and 0037_{16}) are at "00_{16}".

5.1.5 D-A converter characteristics

D-A Converter Characteristics (V_{CC} = 4.0 to 5.5V, V_{SS} = AV_{SS} = 0V, V_{REF} = 4.0V to V_{CC}, Ta= −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
tsu	Setting time				3	µs
R_O	Output resistor		1	2.5	4	kΩ
I_{VREF}	Reference power supply input current	(Note 5)			3.2	mA

Note 5 : Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00_{16}", and not including the ladder resistor of A-D converter.

5.1.6 Timing requirements and switching characteristics

Timing Requirements

(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input "L" pulse width	2			μs
$t_{c(X_{IN})}$	External clock input cycle time	200			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width	50			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width	50			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0 to INT_4 input "H" pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0 to INT_4 input "L" pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial clock input 1 cycle time	800			ns
$t_{c(S_{CLK2})}$	Serial clock input 2 cycle time	1000			ns
$t_{WH(S_{CLK1})}$	Serial clock input 1 "H" pulse width (Note 6)	370			ns
$t_{WH(S_{CLK2})}$	Serial clock input 2 "H" pulse width	400			ns
$t_{WL(S_{CLK1})}$	Serial clock input 1 "L" pulse width (Note 6)	370			ns
$t_{WL(S_{CLK2})}$	Serial clock input 2 "L" pulse width	400			ns
$t_{su(R_xD\text{-}S_{CLK1})}$	Serial input 1 setup time	220			ns
$t_{su(S_{IN2}\text{-}S_{CLK2})}$	Serial input 2 setup time	200			ns
$t_{h(S_{CLK1}\text{-}R_xD)}$	Serial input 1 hold time	100			ns
$t_{h(S_{CLK2}\text{-}S_{IN2})}$	Serial input 2 hold time	200			ns

Note 6 : When $f(X_{IN})$ = 5MHz and bit 6 of address $001A_{16}$ is "1". The minimum time is quarter of the value when $f(X_{IN})$ = 5MHz and bit 6 of address $001A_{16}$ is "0".

Switching Characteristics

(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(S_{CLK1})}$	Serial clock output 1 "H" pulse width	$t_{c(S_{CLK1})}$/2-30			ns
$t_{WL(S_{CLK1})}$	Serial clock output 1 "L" pulse width	$t_{c(S_{CLK1})}$/2-30			ns
$t_{WH(S_{CLK2})}$	Serial clock output 2 "H" pulse width	$t_{c(S_{CLK2})}$/2-160			ns
$t_{WL(S_{CLK2})}$	Serial clock output 2 "L" pulse width	$t_{c(S_{CLK2})}$/2-160			ns
$t_{d(S_{CLK1}\text{-}T_xD)}$	Serial output delay time (Note 7)			140	ns
$t_{d(S_{CLK2}\text{-}S_{OUT2})}$	Serial output delay time			0.2t_c	
$t_{v(S_{CLK1}\text{-}T_xD)}$	Serial output hold time (Note 7)	-30			ns
$t_{v(S_{CLK2}\text{-}S_{OUT2})}$	Serial output hold time	0			
tr	Total CMOS pin rise time (Note 8)		10	30	ns
tf	Total CMOS pin fall time (Note 8)		10	30	ns

Note 7 : When the $P4_5/T_xD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is at "0".

Note 8 : X_{OUT} pin excluded.

Memory Expansion Mode and Microprocessor Mode Timing Requirements
(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tsu($\overline{ONW}$- ϕ)	$\overline{ONW}$ input setup time	-20			ns
th(ϕ -$\overline{ONW}$)	$\overline{ONW}$ input hold time	-20			ns
tsu(DB- ϕ)	Data bus setup time	60			ns
th(ϕ -DB)	Data bus hold time	0			ns

Memory Expansion Mode and Microprocessor mode Switching Characteristics
(V_{CC} = 4.0 to 5.5V, V_{SS} = 0V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tc(ϕ)	ϕ clock cycle time		2×tc(X_{IN})		ns
t_{WH}(ϕ)	ϕ clock "H" pulse width	tc(X_{IN})-10			ns
t_{WL}(ϕ)	ϕ clock "L" pulse width	tc(X_{IN})-10			ns
td(ϕ -AH)	AD_{15} to AD_8 delay time		20	40	ns
tv(ϕ -AH)	AD_{15} to AD_8 valid time	6	10		ns
td(ϕ -AL)	AD_7 to AD_0 delay time		25	45	ns
tv(ϕ -AL)	AD_7 to AD_0 valid time	6	10		ns
td(ϕ -SYNC)	SYNC delay time		20		ns
tv(ϕ -SYNC)	SYNC valid time		10		ns
td(ϕ -$\overline{WR}$)	$\overline{RD}$ and $\overline{WR}$ delay time		10	20	ns
tv(ϕ -$\overline{WR}$)	$\overline{RD}$ and $\overline{WR}$ valid time	3	5	10	ns
td(ϕ -DB)	Data bus delay time		20	70	ns
tv(ϕ -DB)	Data bus valid time	15			ns
td($\overline{RESET}$-$\overline{RESET_{OUT}}$)	$\overline{RESET_{OUT}}$ output delay time (Note 9)			200	ns
tv(ϕ -$\overline{RESET}$)	$\overline{RESET_{OUT}}$ output valid time (Note 9,10)	0		200	ns

Note 9 : This is valid only in microprocessor mode.
Note 10 : The $\overline{RESET_{OUT}}$ output goes "H" with the rise of the ϕ clock, between 1 cycle and 19 cycles after the $\overline{RESET}$ input goes "H".

5.1.7 Test conditions

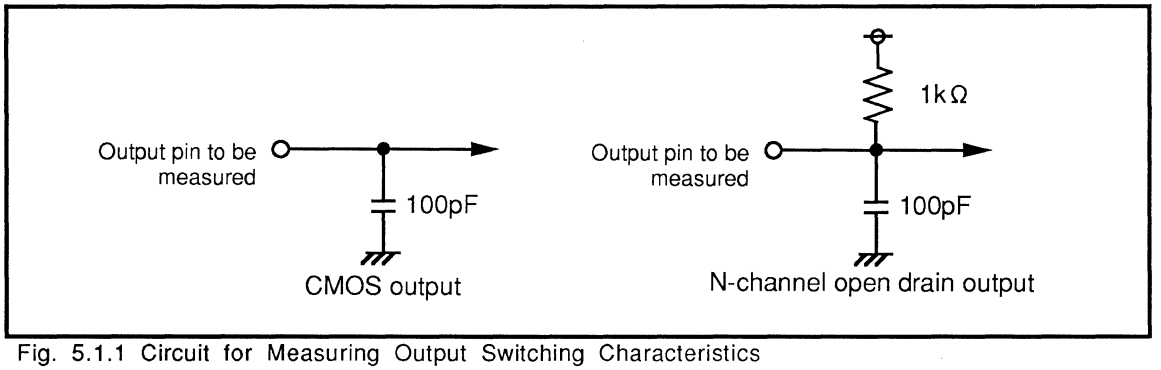
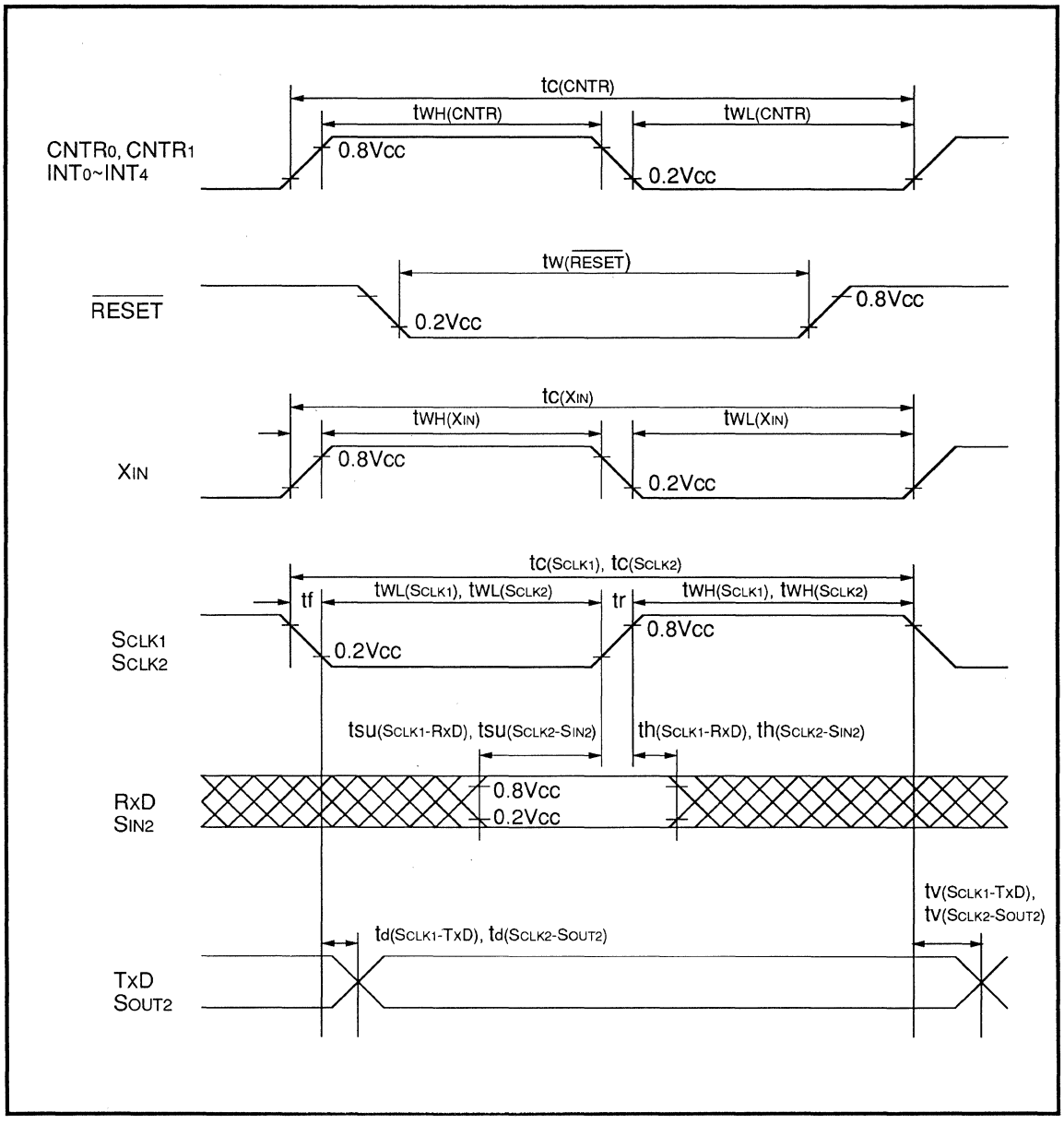


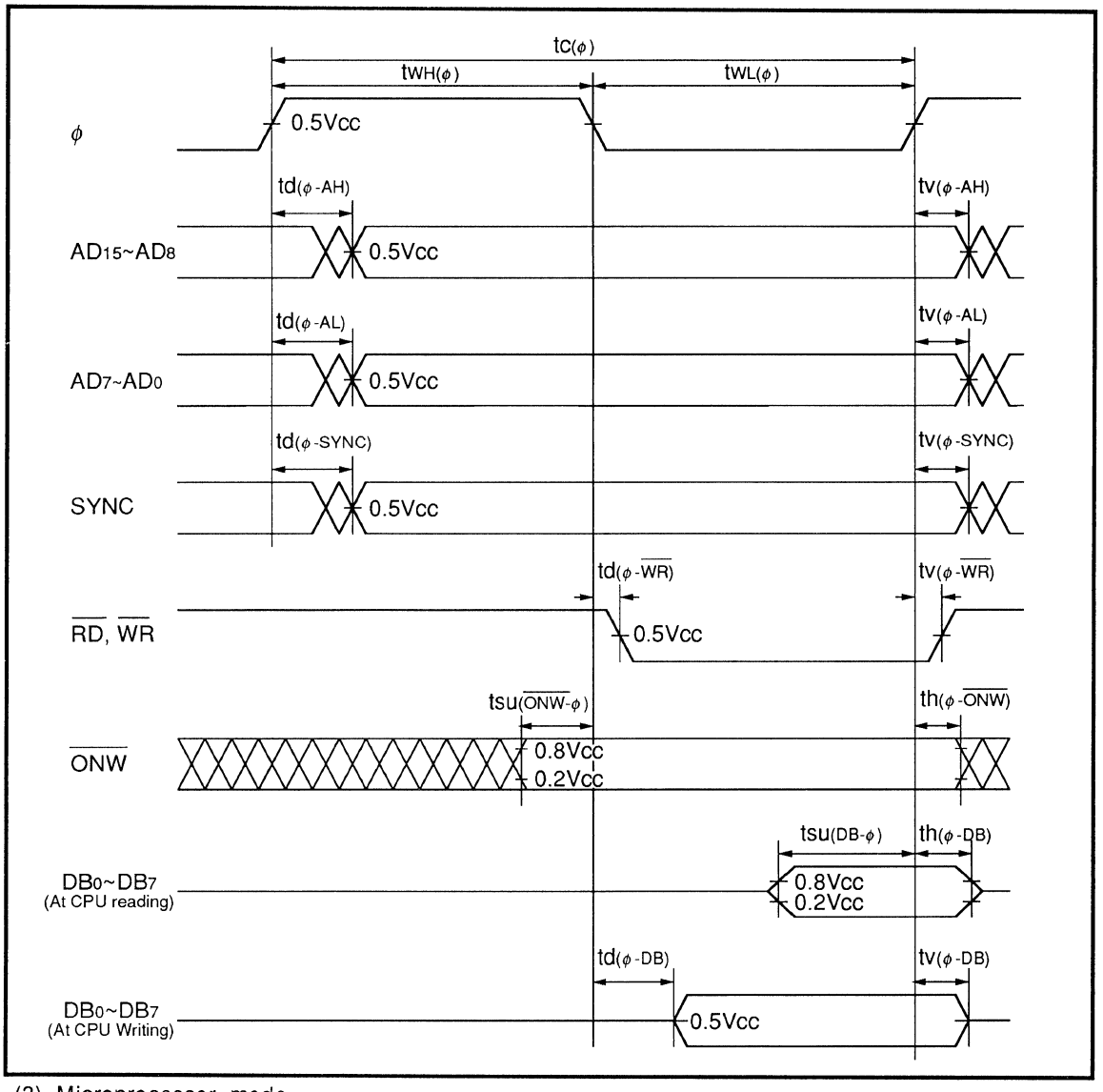
Fig. 5.1.1 Circuit for Measuring Output Switching Characteristics

5.1.8 Timing diagram

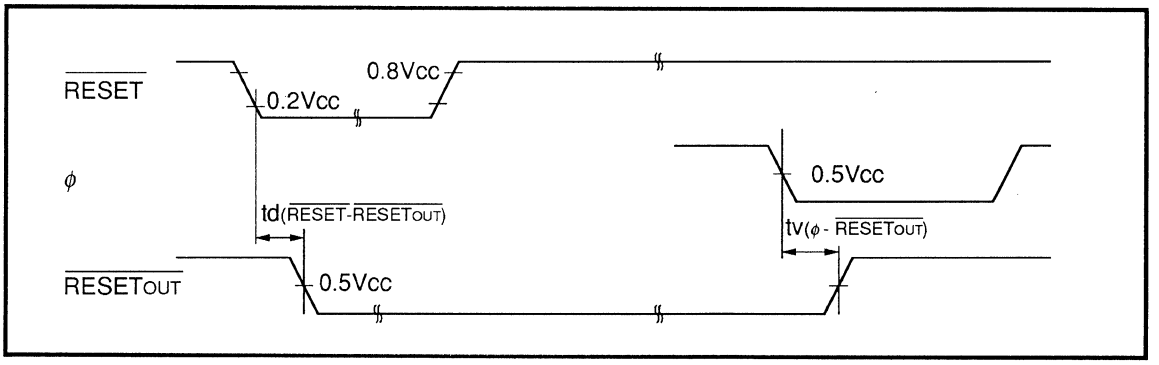
(1) Timing diagram



(2) Memory expansion mode, microprocessor mode



(3) Microprocessor mode



5.2 Typical Characteristics

5.2.1 Typical current consumption

The typical current consumption of the M38063M6-XXXFP/GP is as shown in Figure 5.2.1.

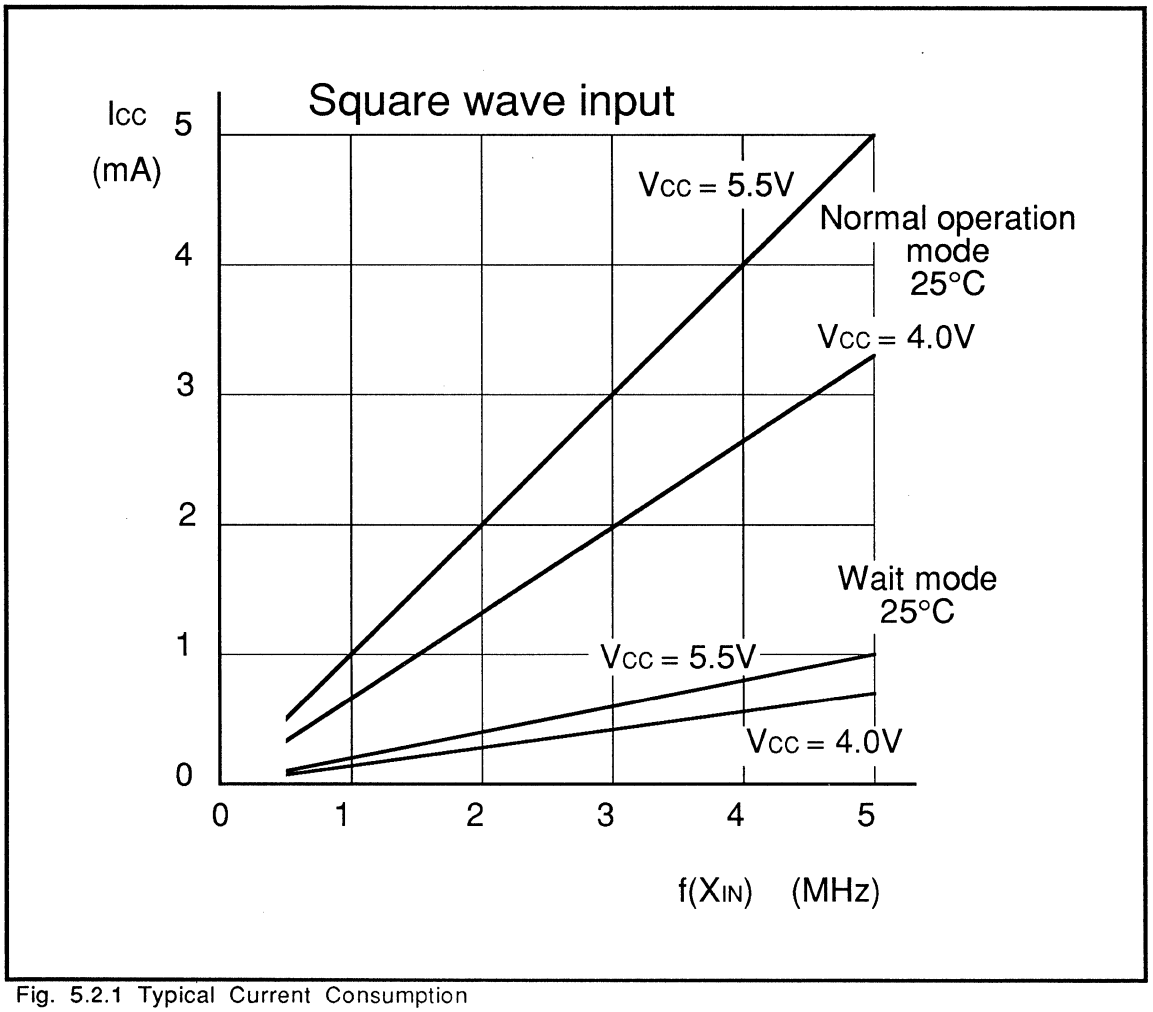


Fig. 5.2.1 Typical Current Consumption

5.2.2 Typical port characteristics

Typical port characteristics of the M38063M6-XXXFP/GP are shown in Figures 5.2.2 and 5.2.3

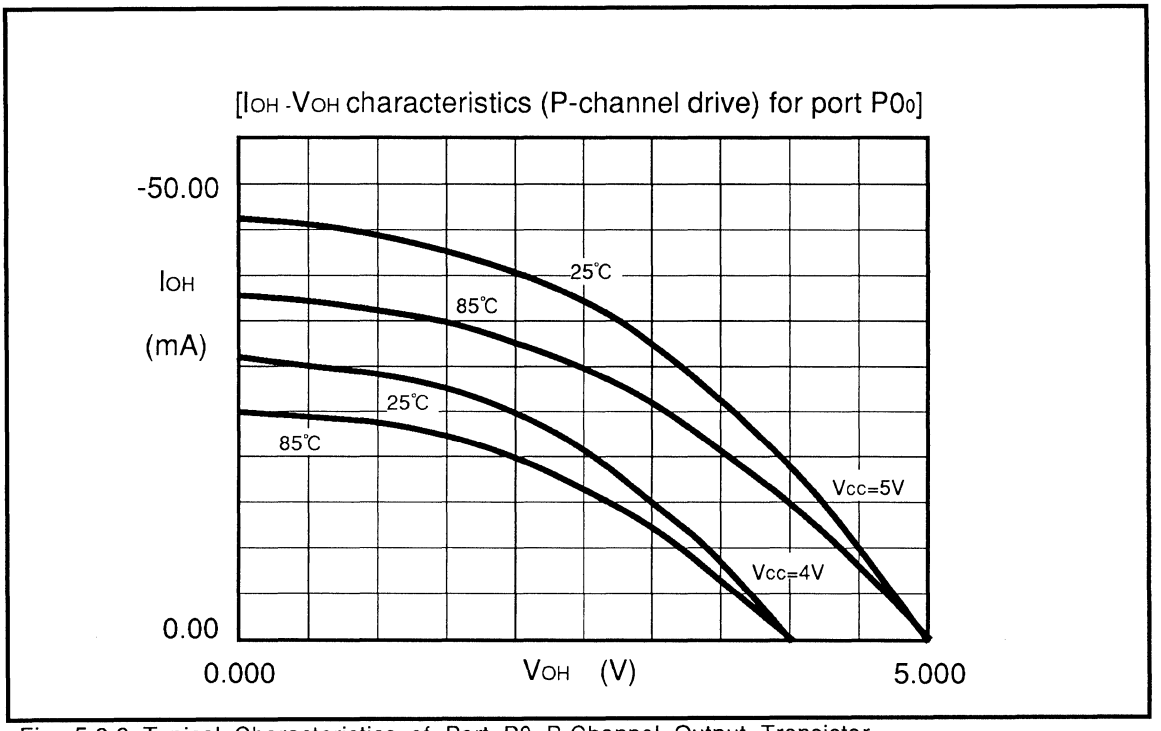


Fig. 5.2.2 Typical Characteristics of Port P0 P-Channel Output Transistor

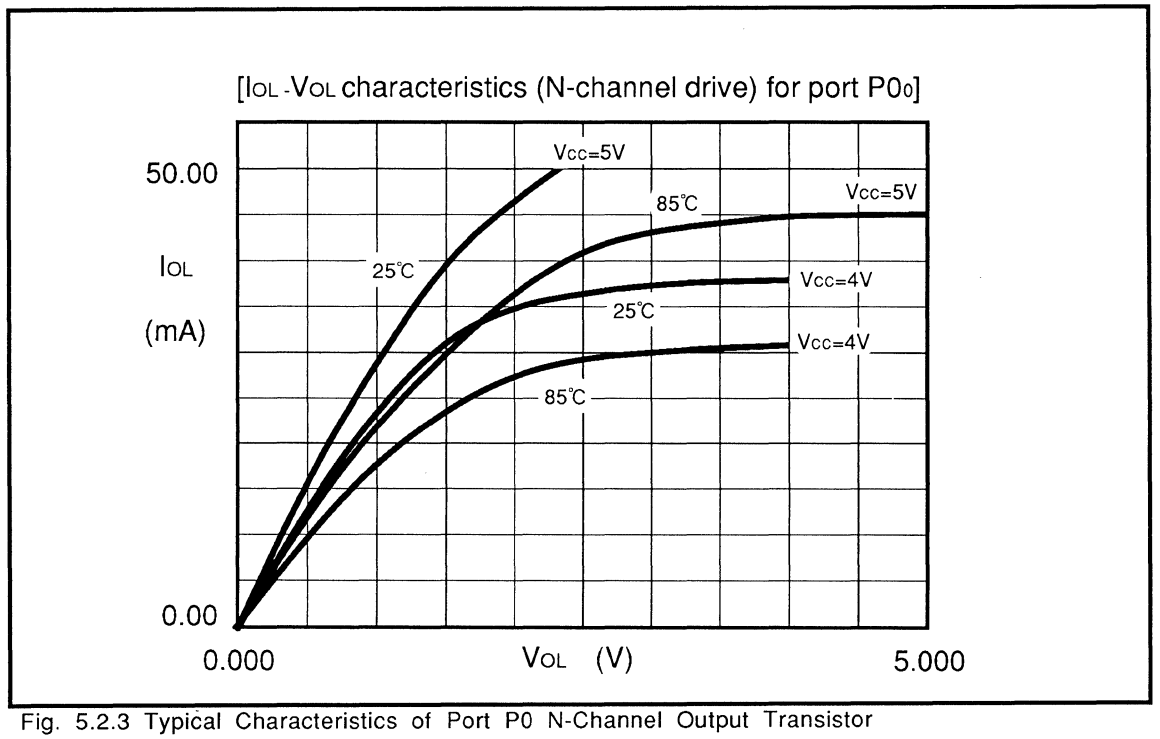
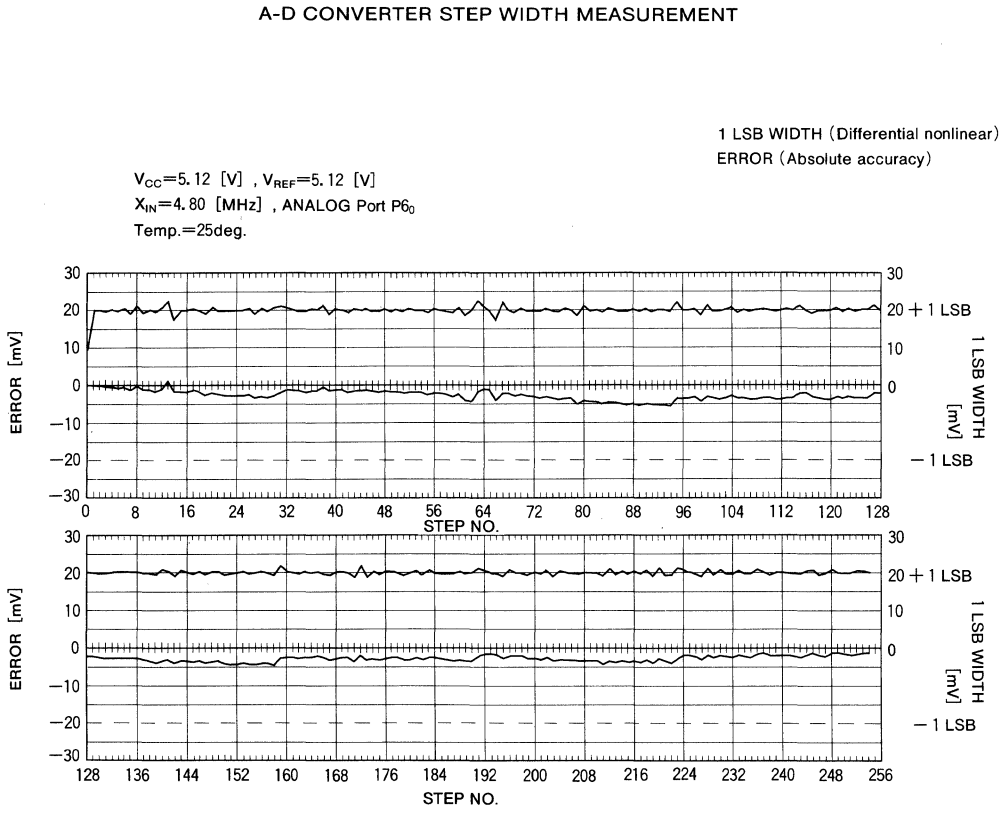


Fig. 5.2.3 Typical Characteristics of Port P0 N-Channel Output Transistor

5.2.3 Typical A-D conversion characteristics

Typical A-D conversion characteristics of the M38063M6-XXXFP/GP are shown in Figure 5.2.4. The line in the lower part of the graph shows the absolute accuracy error. This indicates the deviation from the ideal value at the point that the A-D output changes. For example, the change in the A-D output from 00_{16} to 01_{16} should ideally occur at the point that AN_1 = 10mV, but since it changes at 0mV, the error is: 10 − 0 = 10mV.

The line in the upper part of the graph shows the step width of the input voltage at any given A-D output value. For example, the measured step width of the input voltage is 22mV when the A-D code is $0D_{16}$, and the non-linearity error is 22 − 20 = 2mV (0.3 LSB).

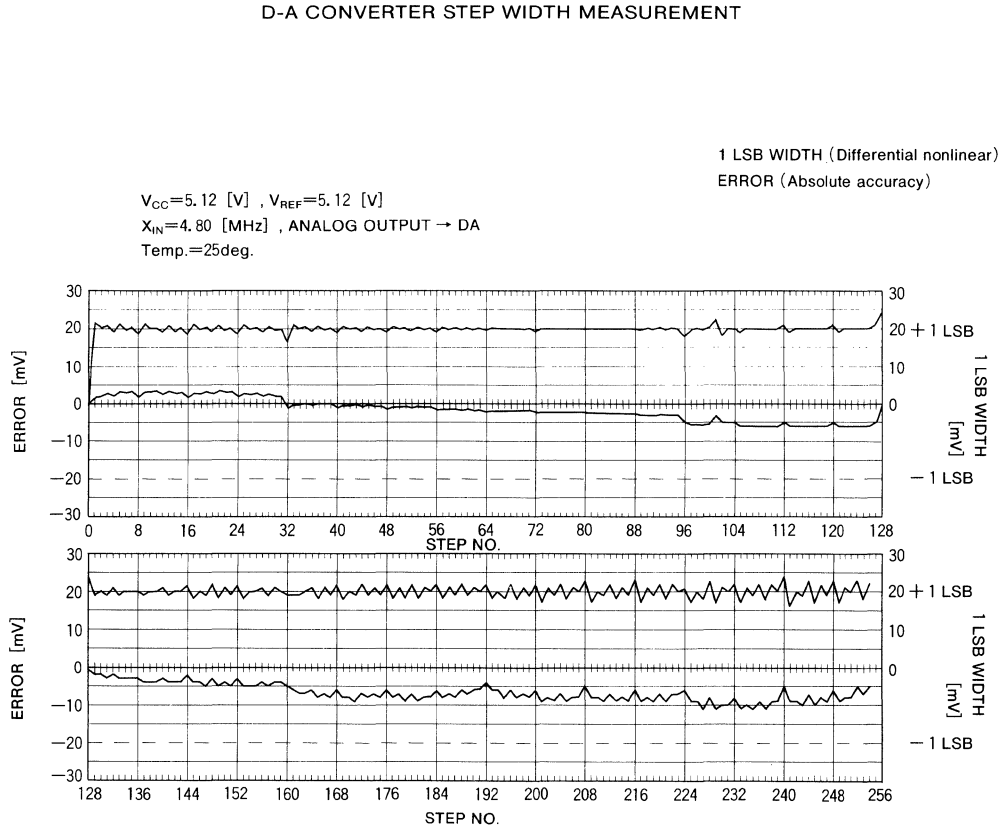


Measured after the power source has stabilized during operation in single-chip mode

Fig. 5.2.4 Typical A-D Conversion Characteristics

5.2.4 Typical D-A conversion characteristics

Typical D-A conversion characteristics of the M38063M6-XXXFP/GP are shown in Figure 5.2.5.
The line in the lower part of the graph shows absolute accuracy error. This indicates the difference between the ideal analog output and the measured output value.
The line in the upper part of the graph shows the step width of the output analog value for a one-bit change in the value input to the D-A converter.



Measured after the power source has stabilized during operation in single-chip mode

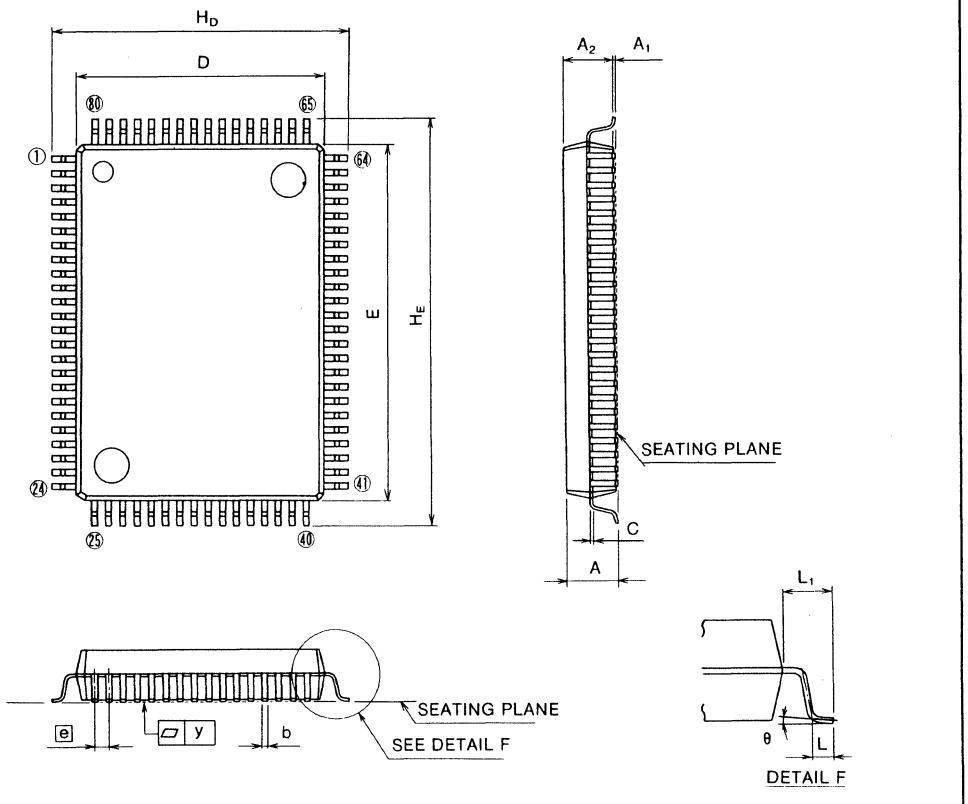
Fig. 5.2.5 Typical D-A Conversion Characteristics

APPENDIX

Appendix 1 Package Outlines

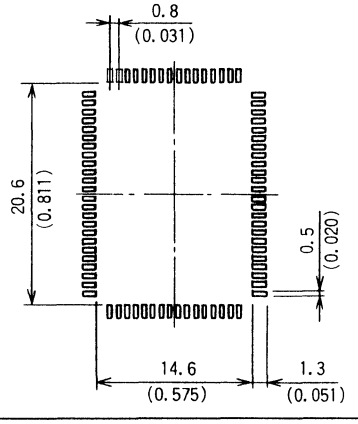
Package Name	Surface Treatment	Weight(g)	EIAJ Code No.	JEDEC Code No.
80P6N	Solder plating		SC-564-A or equivalent	—

Scale : 2.5/1



Unit : mm(inch)
Scale : 1.5/1

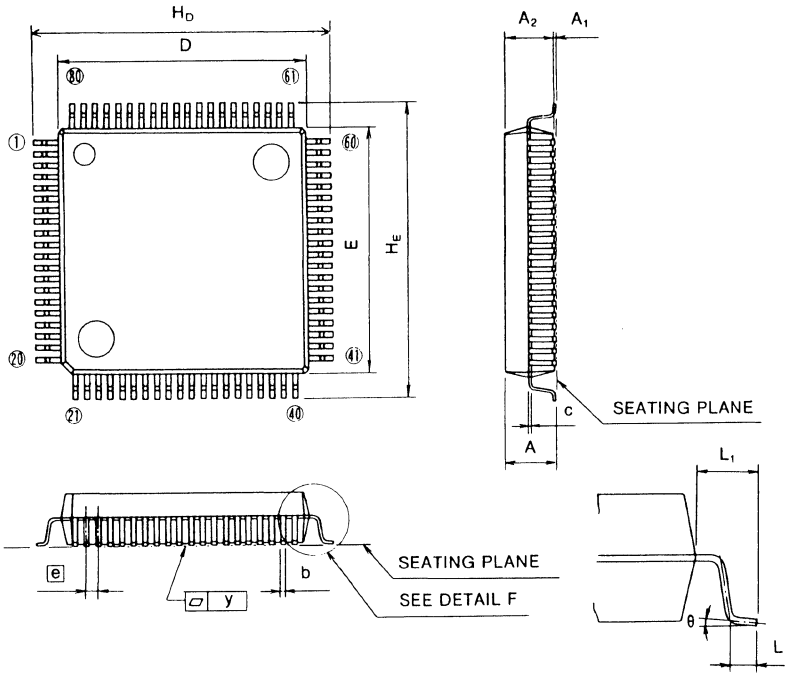
Symbol	Dimension in Millimeters			Dimension in Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.05	—	—	0.120
A_1	0	—	—	0	—	—
A_2	—	2.8	—	—	0.110	—
b	0.25	0.35	0.45	0.012	0.014	0.018
c	0.13	0.15	0.2	0.005	0.006	0.008
D	13.8	14.0	14.2	0.543	0.551	0.559
E	19.8	20.0	20.2	0.740	0.787	0.795
e	—	0.8	—	—	0.031	—
H_D	16.5	16.8	17.1	0.650	0.661	0.673
H_E	22.5	22.8	23.1	0.886	0.898	0.909
L_1	—	1.4	—	—	0.055	—
L	0.4	0.6	0.8	0.016	0.024	0.031
y	—	—	0.1	—	—	0.004
θ	0°	—	10°	0°	—	10°



Appendix 1 Package Outlines

Package Name	Lead Treatment	Weight(g)	EIAJ Code No.	JEDEC Code No.
80P6S	Solder plating		SC-563-A or equivalent	—

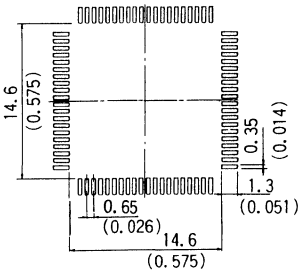
Scale : 2.5/1



Unit : mm(inch)

Scale : 1.5/1

Symbol	Dimension in Millimeters			Dimension in Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.05	—	—	0.120
A_1	0	—	—	0	—	—
A_2	—	2.8	—	—	0.110	—
b	0.2	0.3	0.4	0.008	0.012	0.016
c	0.13	0.15	0.2	0.005	0.006	0.008
D	13.8	14.0	14.2	0.543	0.551	0.559
E	13.8	14.0	14.2	0.543	0.551	0.559
e	—	0.65	—	—	0.026	—
H_D	16.5	16.8	17.1	0.650	0.661	0.673
H_E	16.5	16.8	17.1	0.650	0.661	0.673
L_1	—	1.4	—	—	0.055	—
L	0.4	0.6	0.8	0.016	0.024	0.031
y	—	—	0.15	—	—	0.006
θ	0°	—	10°	0°	—	10°



Recommended Mount Pad

Appendix 2 Handling of Unused Pins

Table 1 Example of Handling of Unused Pins (in single-chip mode)

Pin or port	Handling
Ports P0 to P8	Set to input mode, and use a pull-down resistor
V_{REF}	Use a pull-down resistor
X_{OUT} pin	Leave open

Table 2 Example of Handling of Unused Pins (in memory expansion or microprocessor mode)

Pin or port	Handling
Port $P3_0$, $P3_1$, P4 to P8	Set to input mode, and use a pull-down resistor
V_{REF}	Use a pull-down resistor
X_{OUT} pin	Leave open
$\overline{ONW}$ pin	Use a pull-up resistor
$\overline{RESET_{OUT}}$ pin	Leave open
SYNC pin	Leave open
ϕ pin	Leave open
$\overline{RD}$ and $\overline{WR}$ pins	Leave open
AD_0 to AD_{15} pins	Leave open

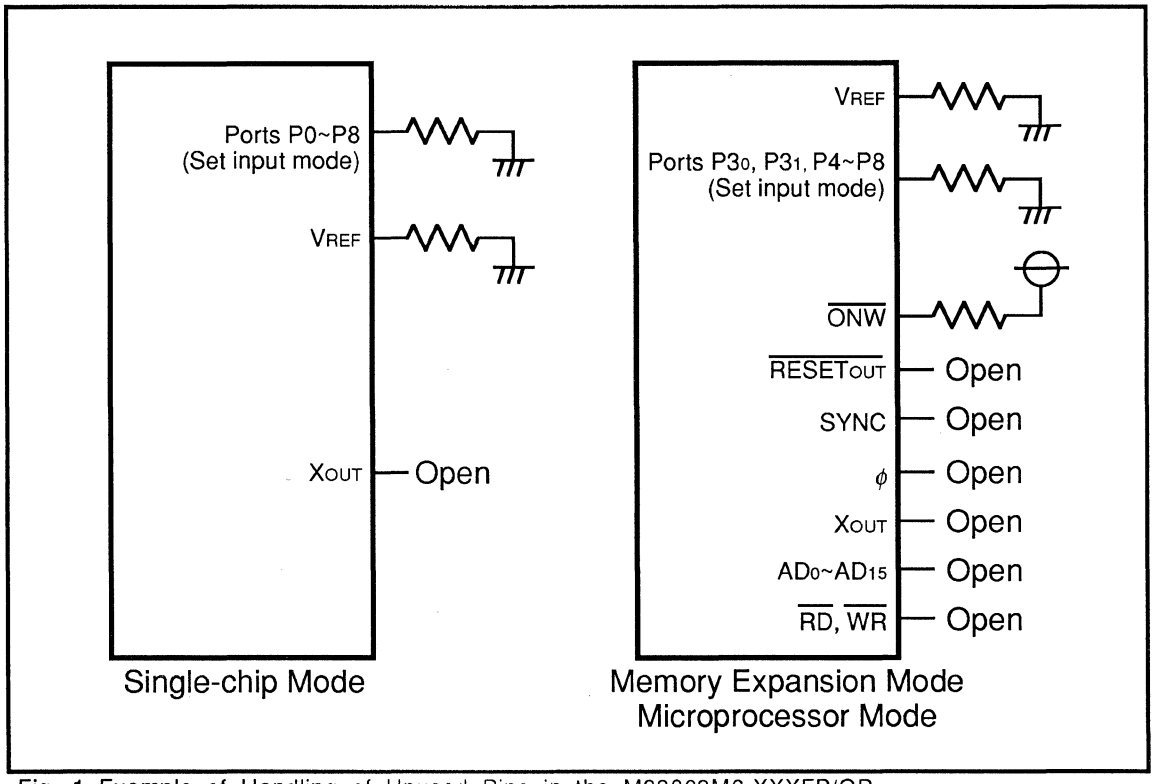


Fig. 1 Example of Handling of Unused Pins in the M38063M6-XXXFP/GP

Appendix 3 Notes on Use

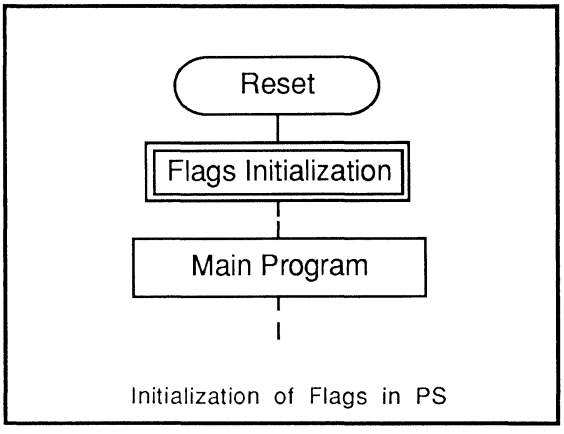
Keep the following points in mind during programming:

1. Processor status register

(1) Initialization of processor status register

The contents of the processor status register (PS) after a reset are undefined, except for the I flag which is "1". Therefore, flags which affect program execution must be initialized after a reset.

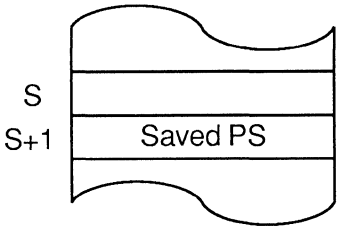
In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.



Initialization of Flags in PS

(2) How to reference the processor status register

To reference the contents of the processor status register (PS), execute the PHP instruction once then read out the contents of (S + 1). If necessary, execute the PLP instruction as well to return the PS to its original, saved status.



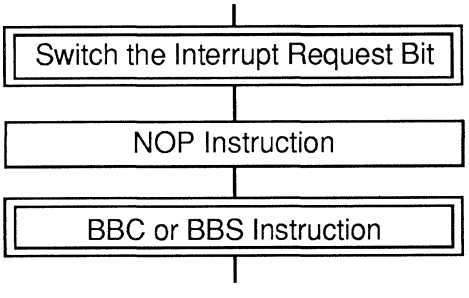
Stack Memory Contents after PHP Instruction Execution

2. Interrupts

The contents of the interrupt request bits can be changed by software, but the values will not change immediately after the overwriting instruction is executed. Therefore, note the following point:

(1) To execute a BBC or BBS instruction

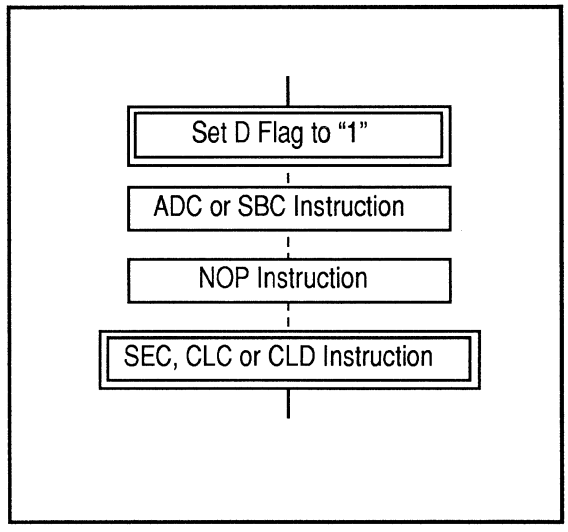
After changing the value of the interrupt request bits, execute at least one instruction before executing a BBC or BBS instruction.



3. Decimal calculations

(1) Execution of decimal calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1" with the SED instruction, then execute the ADC or SBC instruction. After executing the ADC or SBC instruction, execute another instruction before executing a SEC, CLC, or CLD instruction.



(2) Note on flags in decimal mode

When decimal mode is selected (D flag = 1), the values of three of the flags in the status register (the N, V, and Z flags) are invalid after the ADC or SBC instruction is executed. The carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or it is cleared to "0" if a borrow is generated. It can be used as a flag to determine whether the calculation has generated a carry or a borrow, but the C flag must be initialized before the calculation.

4. Timers

(1) Timer division

If a value N (between 0 and 255) is written to a timer latch, a division ratio of 1/(N + 1) is obtained.

5. Clock synchronous serial I/O1

(1) $\overline{S_{RDY1}}$ output

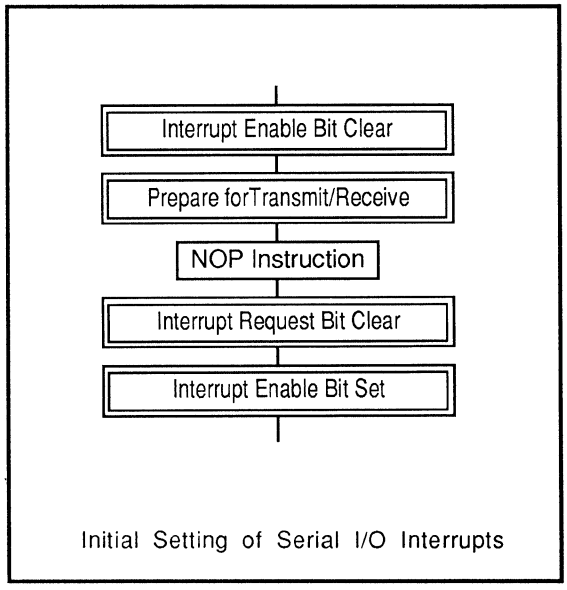
In clock synchronous serial I/O1 mode, if the receiver is using an external clock and it is to output the $\overline{S_{RDY1}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY1}}$ output enable bit to "1".

If the receiver is not to output the $\overline{S_{RDY1}}$ signal, or if it is using the internal clock, there is no need to set the transmit enable bit.

(2) Initial setting of serial I/O1 interrupts

To enable serial I/O1 interrupts, set the system in the following sequence:

1. Use the CLB instruction to clear the interrupt enable bits to "0" (disabled).
2. Prepare for serial I/O1 transfer.
3. After at least one instruction, use the CLB instruction to clear the interrupt request bits to "0".
4. Set the interrupt enable bits to "1" (enabled).



Initial Setting of Serial I/O Interrupts

6. A-D conversion
The comparator has capacitors in its construction, and charge will be lost if the clock frequency is too low. Therefore, make sure that f(X_{IN}) is at least 500kHz when using A-D conversion. (If the $\overline{ONW}$ pin is to "L", the A-D conversion will take twice as long to match the bus cycle. In this case f(X_{IN}) must be at least 1MHz.)
Do not execute the STP or WIT instruction during A-D conversion.

7. Multiplication and division instructions
The MUL and DIV instructions do not affect the T and D flags.

8. JMP instruction
When using the JMP instruction (in indirect addressing mode), do not specify the last address on a page as an indirect address.

9. Ports
(1) Note on using the $P4_5$ pin for N-channel open drain output
The output format of the $P4_5$ pin can be selected by the P-channel output disable bit of the UART control register. When this bit is "0", ordinary CMOS output is selected; when it is "1", N-channel open drain output is selected.
Note that the voltage applied to this pin must not exceed V_{CC} + 0.3V, even if N-channel open drain output is selected.

(2) Port direction registers
The contents of the port direction registers should not be read. Do not use the following instructions to determine the contents of these registers:
- A memory operation instruction (e.g., LDA) when the T flag is "1".
- An addressing mode that treats the value of a port direction register as a modified value.
- A bit test instruction (e.g., BBC or BBS).
- A bit manipulation instruction (e.g., CLB or SEB).
- An instruction that performs a read-modify-write on a port direction register (e.g., ROR).

Use instructions such as the LDM and STA instructions to set the port direction registers.

10. Read-only and write-only registers
Read-only and write-only registers are listed in Table 3.

Table 3 Read-Only and Write-Only Registers

Read/write	Register name
Read-only register	Serial I/O1 status register, Serial I/O1 Receive Buffer, Interrupt request register 1, interrupt request register 2 (Note 1)
Write-only register	Port direction registers (Note 2)

Note 1 : The bits of the interrupt request registers can only be cleared (1 to 0).
Note 2 : For further details, see the previous section, 9. "Ports".

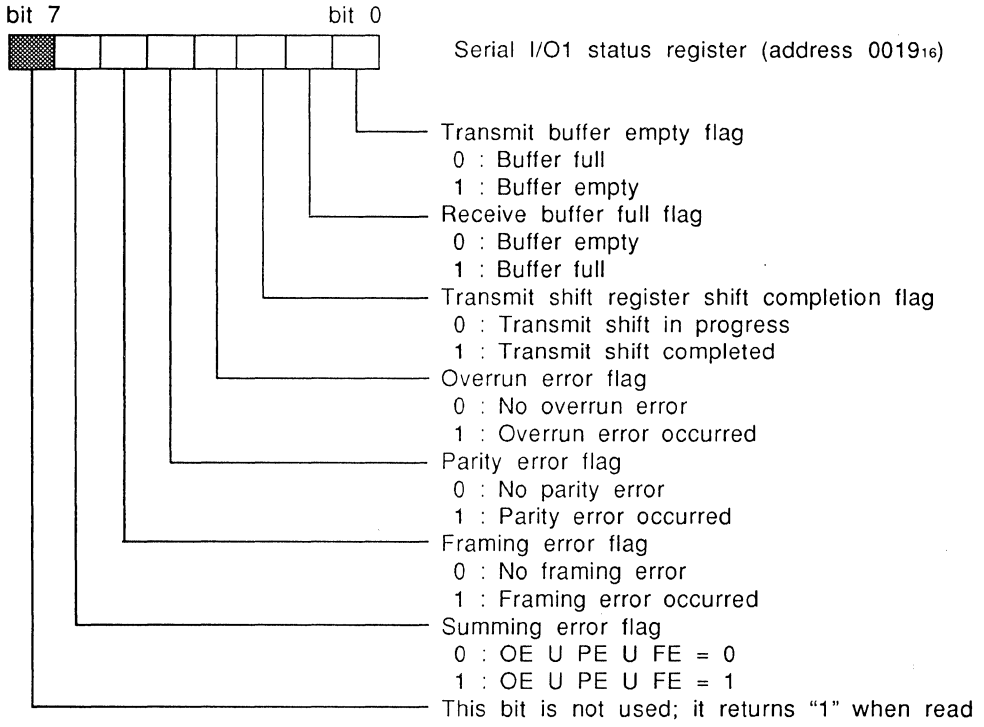
Appendix 4 SFR Memory Map

0000_{16}	Port P0	0020_{16}	Prescaler 12
0001_{16}	Port P0 Direction Register	0021_{16}	Timer 1
0002_{16}	Port P1	0022_{16}	Timer 2
0003_{16}	Port P1 Direction Register	0023_{16}	Timer XY Mode Register
0004_{16}	Port P2	0024_{16}	Prescaler X
0005_{16}	Port P2 Direction Register	0025_{16}	Timer X
0006_{16}	Port P3	0026_{16}	Prescaler Y
0007_{16}	Port P3 Direction Register	0027_{16}	Timer Y
0008_{16}	Port P4	0028_{16}	
0009_{16}	Port P4 Direction Register	0029_{16}	
$000A_{16}$	Port P5	$002A_{16}$	
$000B_{16}$	Port P5 Direction Register	$002B_{16}$	
$000C_{16}$	Port P6	$002C_{16}$	
$000D_{16}$	Port P6 Direction Register	$002D_{16}$	
$000E_{16}$	Port P7	$002E_{16}$	
$000F_{16}$	Port P7 Direction Register	$002F_{16}$	
0010_{16}	Port P8	0030_{16}	
0011_{16}	Port P8 Direction Register	0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	AD/DA Control Register
0015_{16}		0035_{16}	A-D Conversion Register
0016_{16}		0036_{16}	D-A1 Conversion Register
0017_{16}		0037_{16}	D-A2 Conversion Register
0018_{16}	Transmit/Receive Buffer	0038_{16}	
0019_{16}	Serial I/O1 Status Register	0039_{16}	
$001A_{16}$	Serial I/O1 Control Register	$003A_{16}$	Interrupt Edge Selection Register
$001B_{16}$	UART Control Register	$003B_{16}$	CPU Mode Register
$001C_{16}$	Baud Rate Generator	$003C_{16}$	Interrupt Request Register 1
$001D_{16}$	Serial I/O2 Control Register	$003D_{16}$	Interrupt Request Register 2
$001E_{16}$		$003E_{16}$	Interrupt Control Register 1
$001F_{16}$	Serial I/O2 Register	$003F_{16}$	Interrupt Control Register 2

Fig. 2 SFR Memory Map

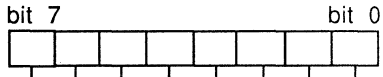
Appendix 5 Control Registers

Table 4 Serial I/O1 Status Register



This register is read only.

Table 5 Serial I/O1 Control Register



Serial I/O1 control register (address $001A_{16}$)

BRG count source select bit
0 : Oscillation frequency f(X_{IN})
1 : Oscillation frequency f(X_{IN}) divided by 4

Serial I/O1 synchronization clock select bit
(1) When clock synchronous serial I/O1 is selected
0 : BRG output divided by 4
1 : External clock input
(2) When clock asynchronous serial I/O is selected
0 : BRG output divided by 16
1 : External clock input

$\overline{S_{RDY1}}$ output enable bit
(1) When clock synchronous serial I/O1 is selected
0 : $\overline{S_{RDY1}}$ output disabled
1 : $\overline{S_{RDY1}}$ output enabled
(2) When clock asynchronous serial I/O is selected, this bit is invalid.

Transmit interrupt source select bit
0 : Interrupt when transmit buffer has emptied
1 : Interrupt when transmit shift operation is completed

Transmit enable bit
0 : Transmit disabled
1 : Transmit enabled

Receive enable bit
0 : Receive disabled
1 : Receive enabled

Serial I/O1 mode select bit
0 : Clock asynchronous serial I/O
1 : Clock synchronous serial I/O

Serial I/O1 enable bit
0 : Serial I/O disabled
1 : Serial I/O enabled

Table 6 UART Control Register

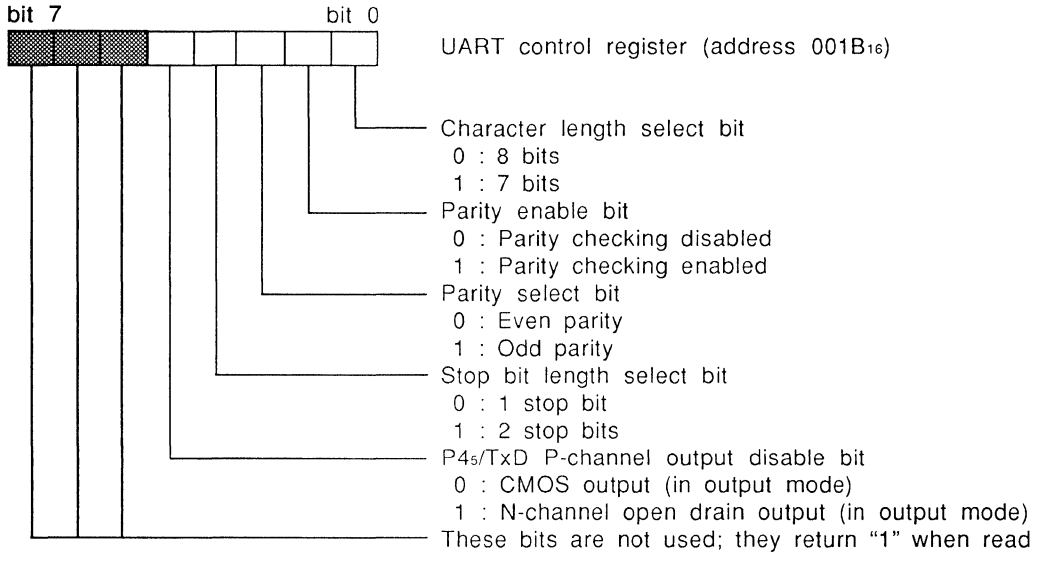


Table 7 Serial I/O2 Control Register

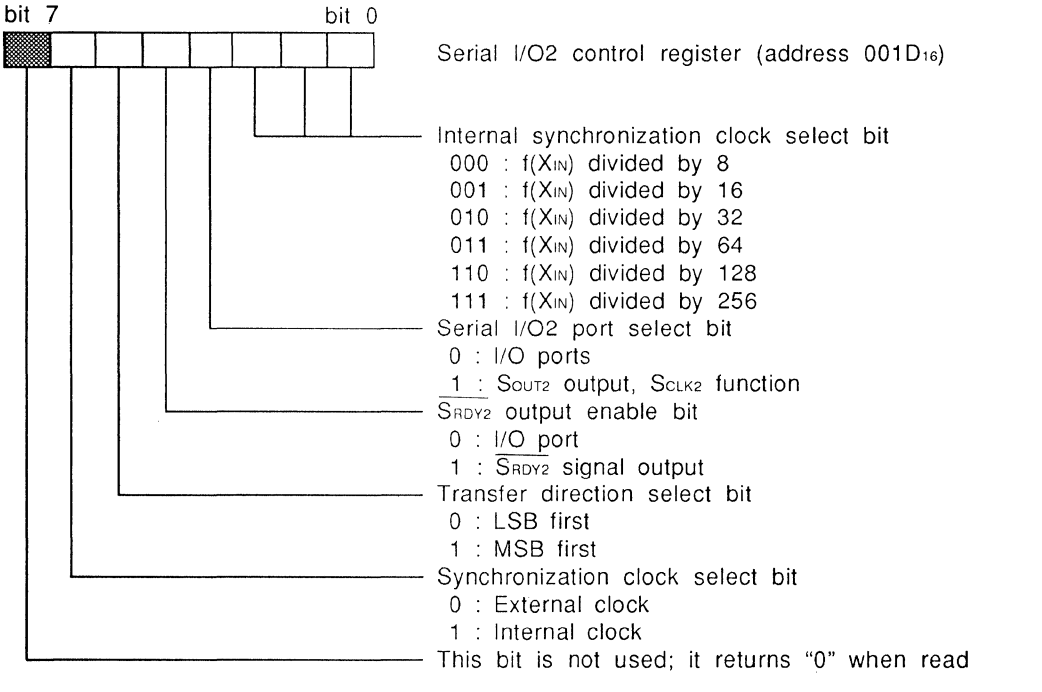
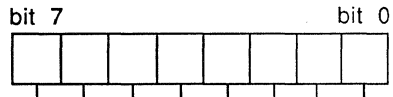


Table 8 Timer XY Mode Register



Timer XY mode register (address 0023_{16})

Timer X operation mode bit
- 00 : Timer mode
- 01 : Pulse output mode
- 10 : Event counter mode
- 11 : Pulse width measurement mode

$CNTR_0$ active edge selection bit
- 0 : Interrupt at falling edge
  Count at rising edge (Event counter mode)
- 1 : Interrupt at rising edge
  Count at falling edge (Event counter mode)

Timer X count stop bit
- 0 : Count start
- 1 : Count stop

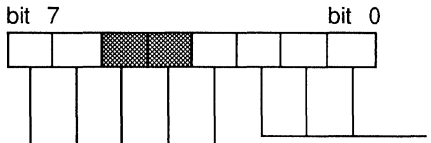
Timer Y operation mode bit
- 00 : Timer mode
- 01 : Pulse output mode
- 10 : Event counter mode
- 11 : Pulse width measurement mode

$CNTR_1$ active edge selection bit
- 0 : Interrupt at falling edge
  Count at rising edge (Event counter mode)
- 1 : Interrupt at rising edge
  Count at falling edge (Event counter mode)

Timer Y count stop bit
- 0 : Count start
- 1 : Count stop

Note : At reset, the timer XY mode register is cleared to "00_{16}".

Table 9 AD/DA Control Register



AD/DA control register (address 0034_{16})

Analog input pin select bit

bit2	bit1	bit0	
0	0	0	: $P6_0/AN_0$
0	0	1	: $P6_1/AN_1$
0	1	0	: $P6_2/AN_2$
0	1	1	: $P6_3/AN_3$
1	0	0	: $P6_4/AN_4$
1	0	1	: $P6_5/AN_5$
1	1	0	: $P6_6/AN_6$
1	1	1	: $P6_7/AN_7$

A-D conversion completion bit
0 : Conversion in progress
1 : Conversion completed

These bits are not used; they return "0" when read

D-A1 output enable bit
0 : Output disabled
1 : Output enabled

D-A2 output enable bit
0 : Output disabled
1 : Output enabled

Table 10 Interrupt Edge Selection Register

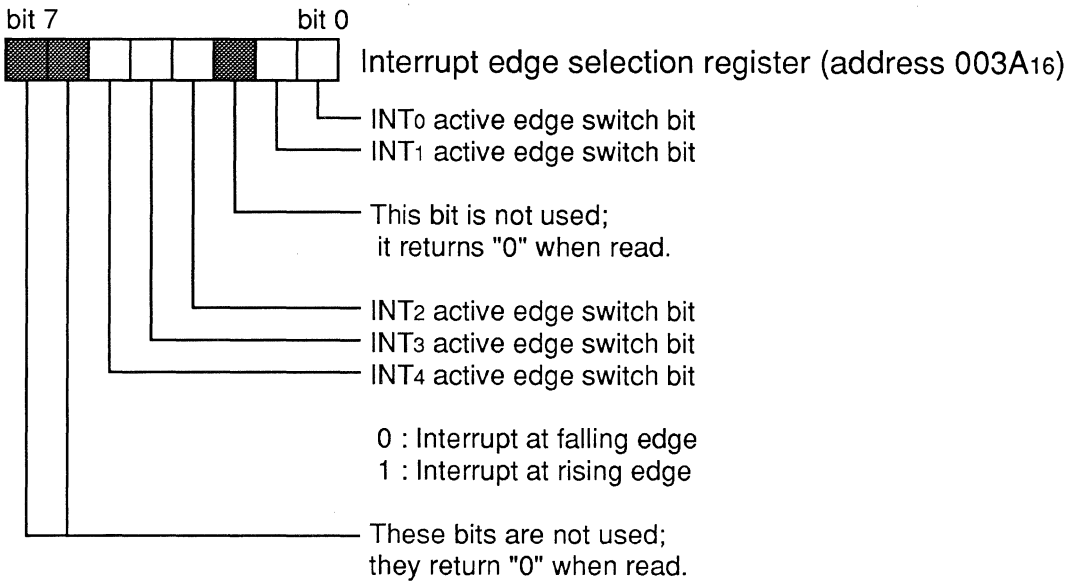


Table 11 CPU Mode Register

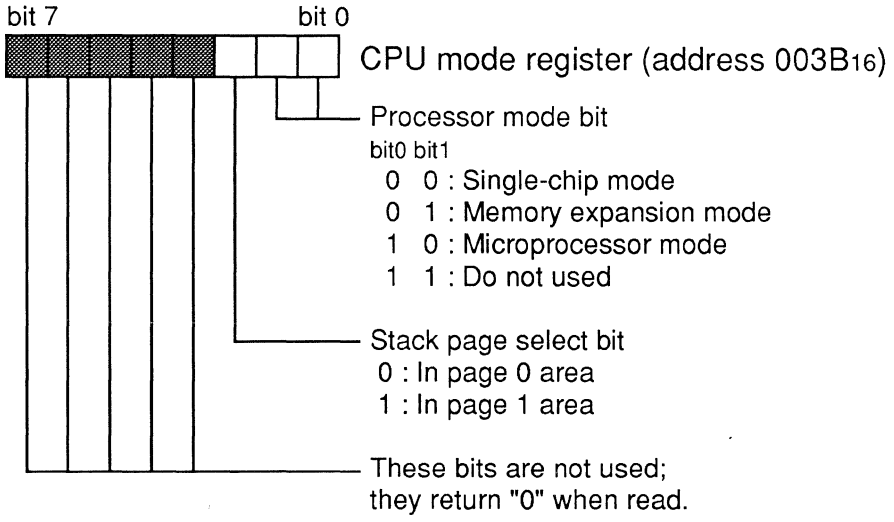
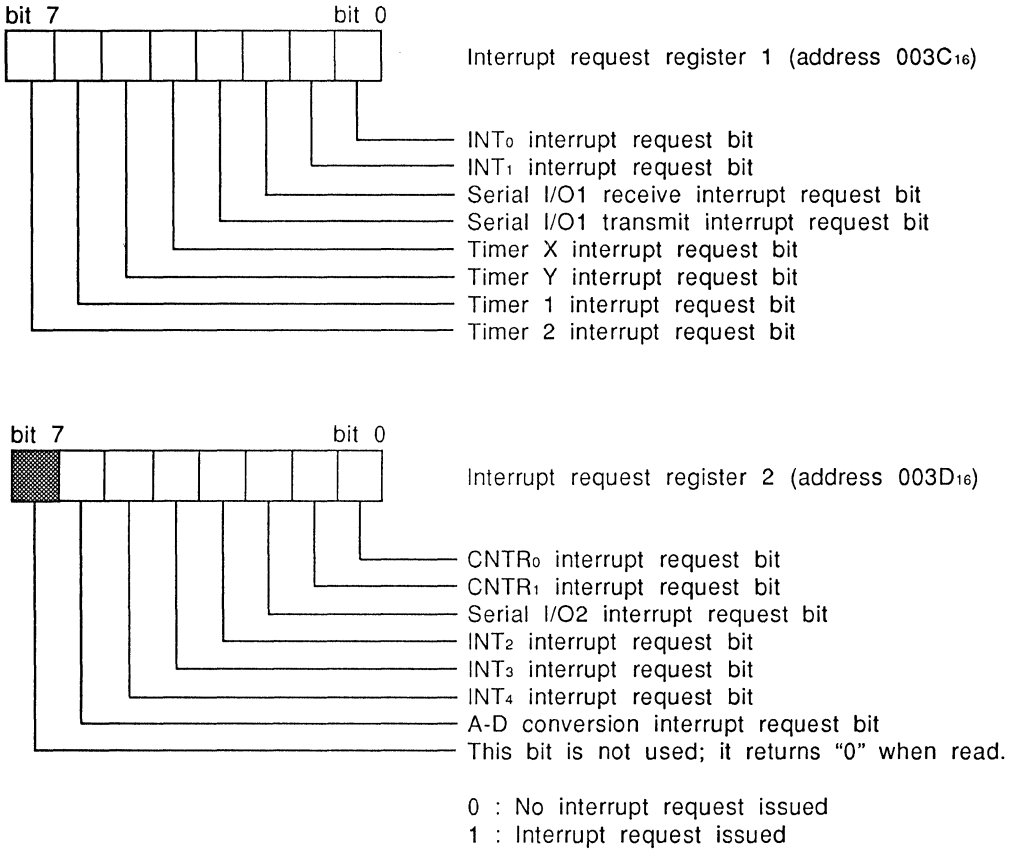
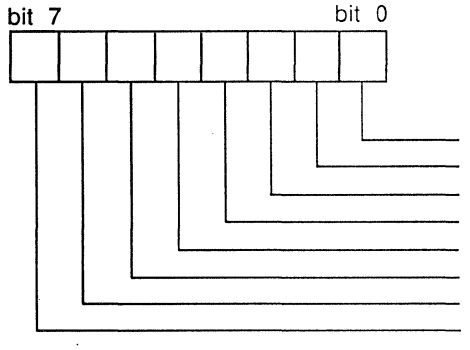


Table 12 Interrupt Request Registers



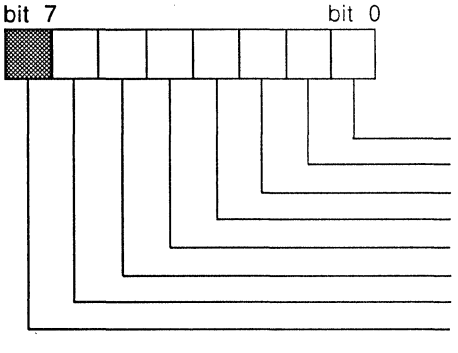
The bits of these registers can only be cleared (1 to 0).

Table 13 Interrupt Control Registers



Interrupt control register 1 (address $003E_{16}$)

- INT_0 interrupt enable bit
- INT_1 interrupt enable bit
- Serial I/O1 receive interrupt enable bit
- Serial I/O1 transmit interrupt enable bit
- Timer X interrupt enable bit
- Timer Y interrupt enable bit
- Timer 1 interrupt enable bit
- Timer 2 interrupt enable bit



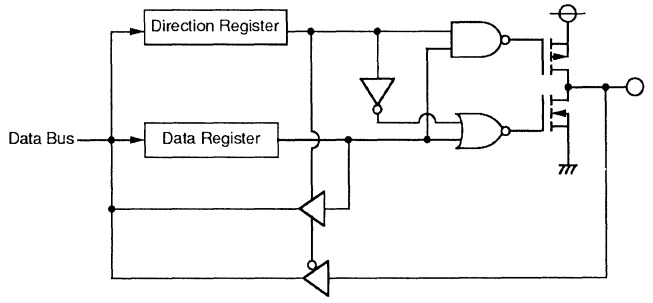
Interrupt control register 2 (address $003F_{16}$)

- $CNTR_0$ interrupt enable bit
- $CNTR_1$ interrupt enable bit
- Serial I/O2 interrupt enable bit
- INT_2 interrupt enable bit
- INT_3 interrupt enable bit
- INT_4 interrupt enable bit
- A-D conversion interrupt enable bit
- This bit is not used; it returns "0" when read. Do not write "1" to this bit.

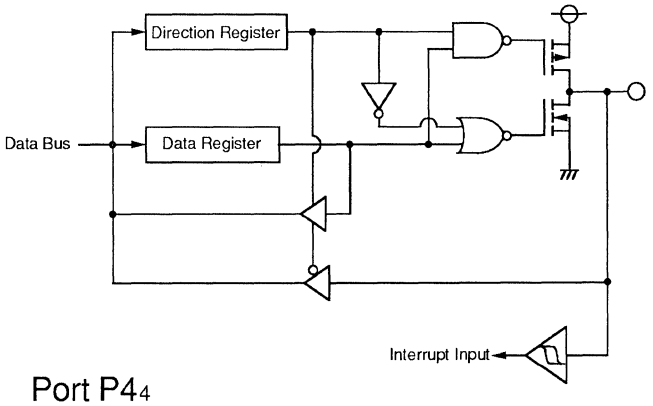
0 : Interrupt disabled
1 : Interrupt enabled

Appendix 6 Ports

Ports P0,P1,P2,P3,P4$_0$,P4$_1$,P5$_0$,P8



Ports P4$_2$,P4$_3$,P5$_1$,P5$_2$,P5$_3$



Port P4$_4$

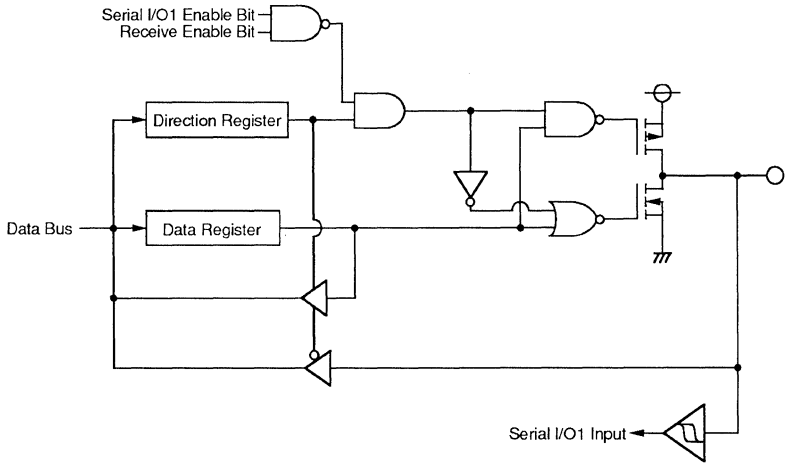


Fig. 3 Port Circuits (1)

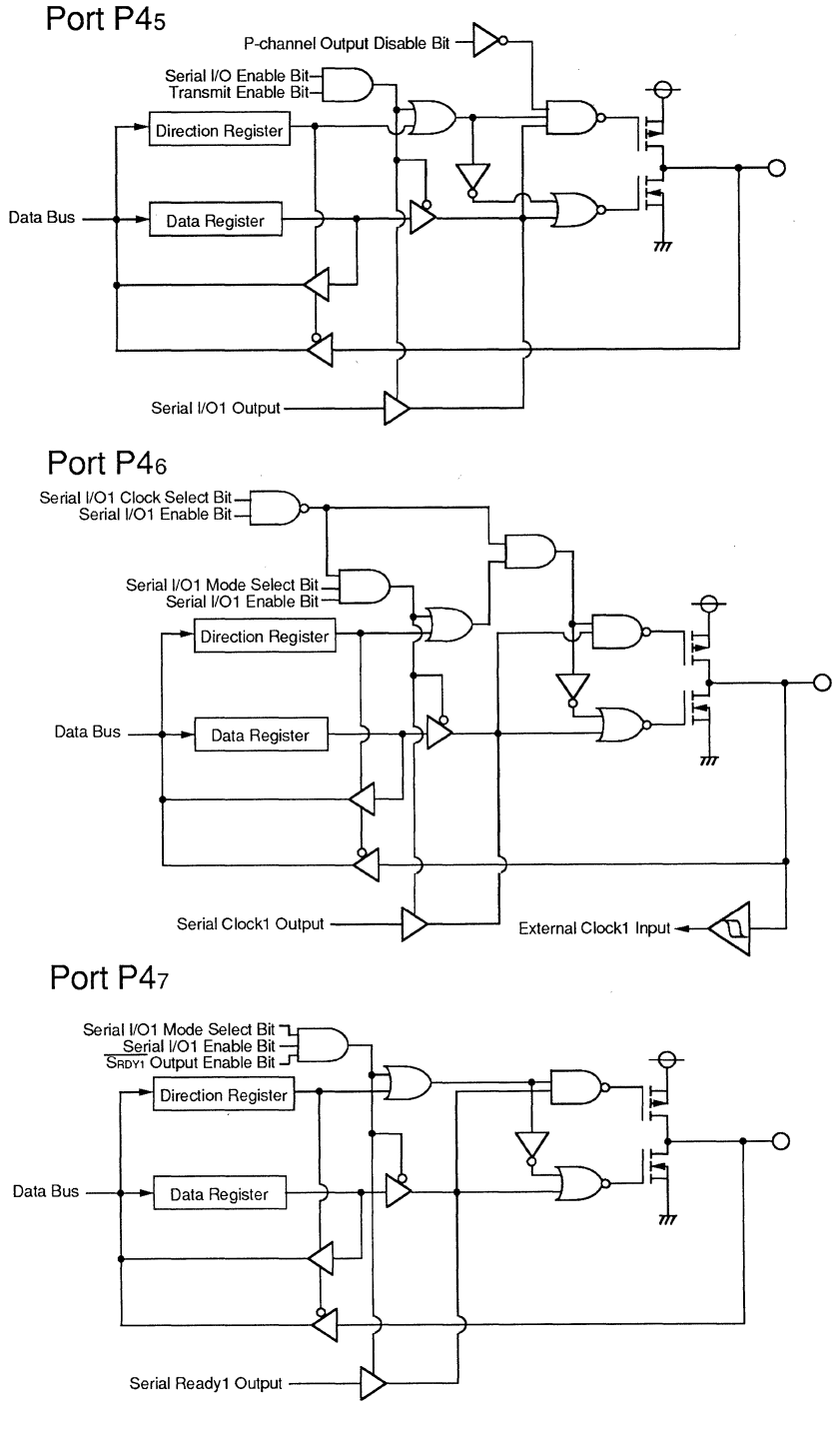
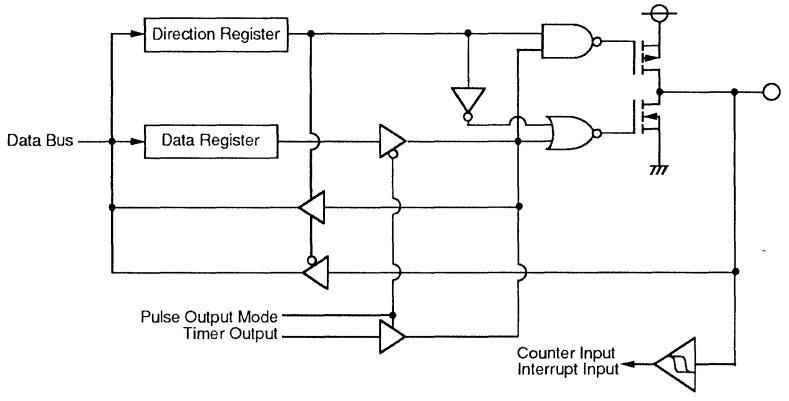
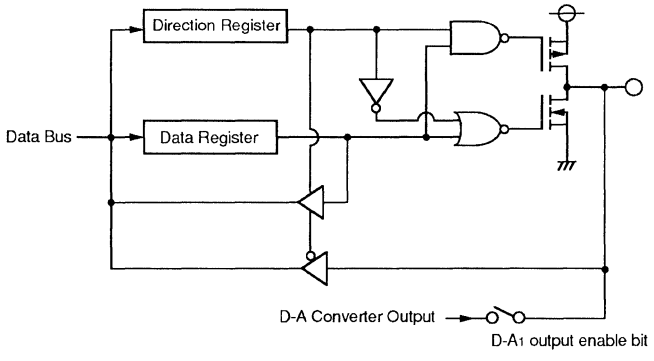


Fig. 4 Port Circuits (2)

Ports $P5_4$,$P5_5$



Port $P5_6$



Port $P5_7$

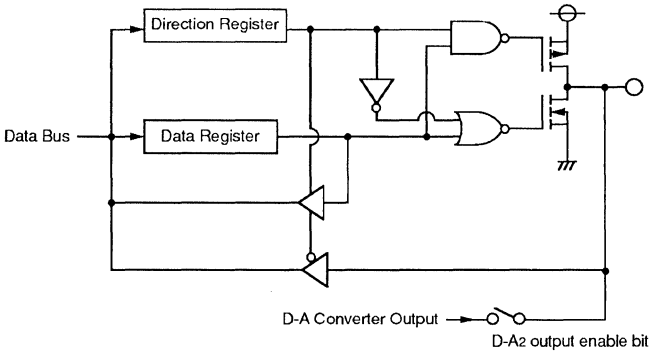
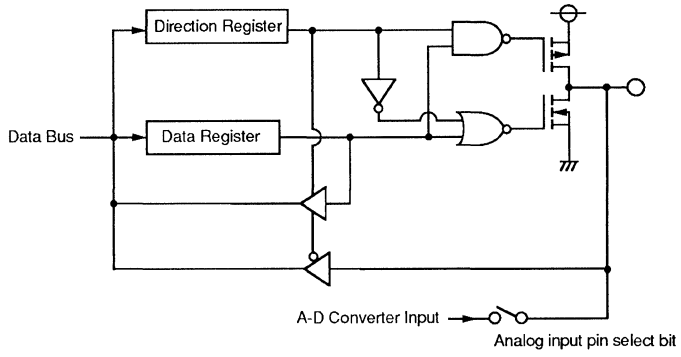
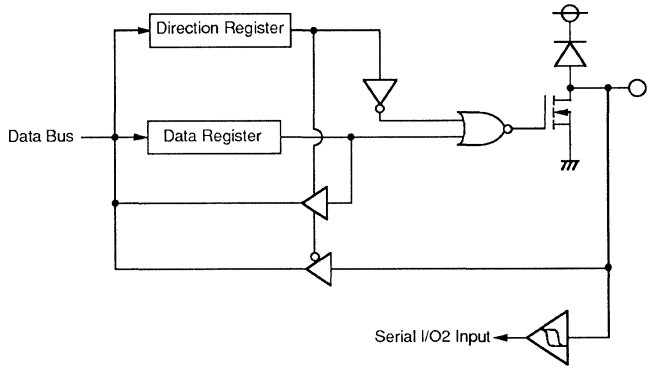


Fig. 5 Port Circuits (3)

Port P6



Port $P7_0$



Port $P7_1$

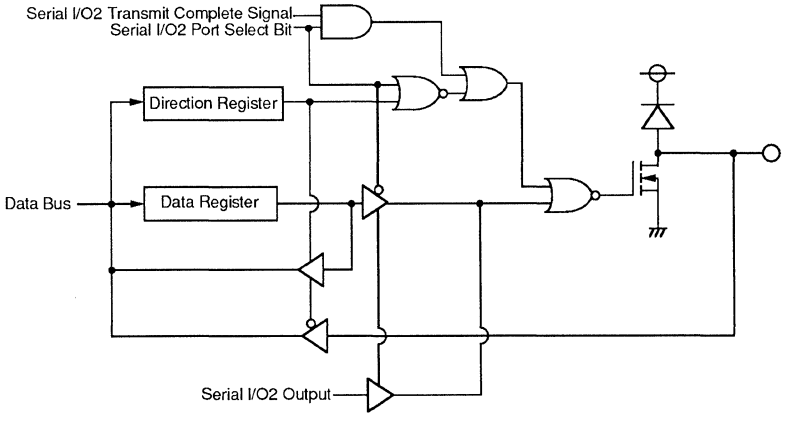
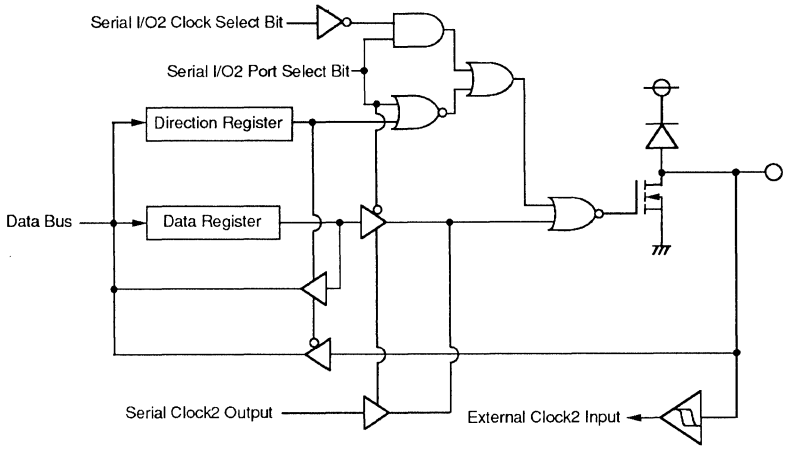
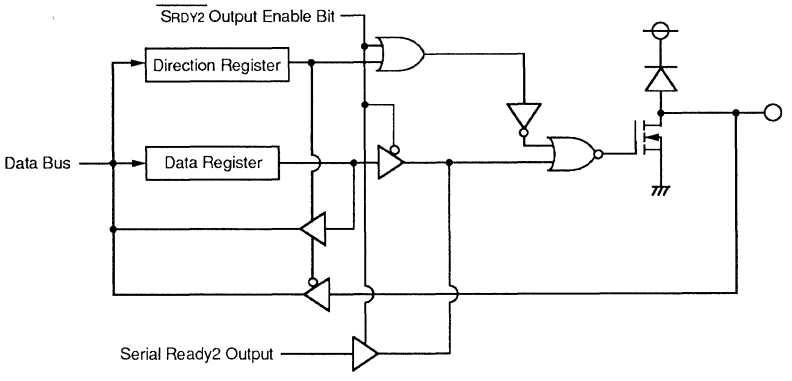


Fig. 6 Port Circuits (4)

Port $P7_2$



Port $P7_3$



Port $P7_4$~$P7_7$

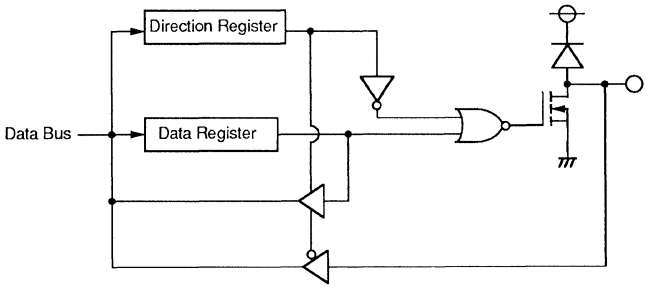


Fig. 7 Port Circuits (5)

Appendix 7 Machine Instruction

MACHINE INSTRUCTIONS

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC (Note 1) (Note 5)	When T=0 A←A+M+C When T=1 M(X)←M(X)+M+C	Adds the carry, accumulator and memory contents. The results are entered into the accumulator. Adds the contents of the memory in the address indicated by index register X, the contents of the memory specified by the addressing mode and the carry. The results are entered into the memory at the address indicated by index register X.				69	2	2							65	3	2			
AND (Note 1)	When T=0 A←A∧M When T=1 M(X)←M(X)∧M	"AND's" the accumulator and memory contents. The results are entered into the accumulator. "AND's" the contents of the memory of the address indicated by index register X and the contents of the memory specified by the addressing mode. The results are entered into the memory at the address indicated by index register X.				29	2	2							25	3	2			
ASL	7 0 C ← □ ←0	Shifts the contents of accumulator or contents of memory one bit to the left. The low order bit of the accumulator or memory is cleared and the high order bit is shifted into the carry flag.							0A	2	1				06	5	2			
BBC (Note 4)	A_b or M_b=0?	Branches when the contents of the bit specified in the accumulator or memory is "0".										13+2i	4	2				17+2i	5	3
BBS (Note 4)	A_b or M_b=1?	Branches when the contents of the bit specified in the accumulator or memory is "1".										03+2i	4	2				07+2i	5	3
BCC (Note 4)	C=0?	Branches when the contents of carry flag is "0".																		
BCS (Note 4)	C=1?	Branches when the contents of carry flag is "1".																		
BEQ (Note 4)	Z=1?	Branches when the contents of zero flag is "1".																		
BIT	A∧M	"AND's" the contents of accumulator and memory. The results are not entered anywhere.													24	3	2			
BMI (Note 4)	N=1?	Branches when the contents of negative flag is "1".																		
BNE (Note 4)	Z=0?	Branches when the contents of zero flag is "0".																		
BPL (Note 4)	N=0?	Branches when the contents of negative flag is "0".																		
BRA	PC←PC±offset	Jumps to address specified by adding offset to the program counter.																		
BRK	B←1 $M(S)←PC_H$ S←S−1 $M(S)←PC_L$ S←S−1 M(S)←PS S←S−1 $PC_L←AD_L$ $PC_H←AD_H$	Executes a software interrupt.	00	7	1															

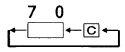
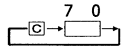
Addressing mode																												Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
75	4	2				6D	4	3	7D	5	3	79	5	3							61	6	2	71	6	2							N	V	•	•	•	•	Z	C
35	4	2				2D	4	3	3D	5	3	39	5	3							21	6	2	31	6	2							N	•	•	•	•	•	Z	•
16	6	2				0E	6	3	1E	7	3																						N	•	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																											90	2	2				•	•	•	•	•	•	•	•
																											B0	2	2				•	•	•	•	•	•	•	•
																											F0	2	2				•	•	•	•	•	•	•	•
						2C	4	3																										M_7	M_6	•	•	•	•	Z	•
																											30	2	2				•	•	•	•	•	•	•	•
																											D0	2	2				•	•	•	•	•	•	•	•
																											10	2	2				•	•	•	•	•	•	•	•
																											80	4	2				•	•	•	•	•	•	•	•
																																	•	•	•	1	•	1	•	•

Symbol	Function	Details	Addressing mode																
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
BVC (Note 4)	V=0?	Branches when the contents of overflow flag is "0."																		
BVS (Note 4)	V=1?	Branches when the contents of overflow flag is "1."																		
CLB	A_b or M_b←0	Clears the contents of the bit specified in the accumulator or memory to "0."										1B+2i	2	1				1F+2i	5	2
CLC	C←0	Clears the contents of the carry flag to "0."	18	2	1															
CLD	D←0	Clears the contents of decimal mode flag to "0."	D8	2	1															
CLI	I←0	Clears the contents of interrupt disable flag to "0."	58	2	1															
CLT	T←0	Clears the contents of index X mode flag to "0."	12	2	1															
CLV	V←0	Clears the contents overflow flag to "0."	B8	2	1															
CMP (Note 3)	When T=0 A−M When T=1 M(X)−M	Compares the contents of accumulator and memory. Compares the contents of the memory specified by the addressing mode with the contents of the address indicated by index register X.				C9	2	2							C5	3	2			
COM	M←$\overline{M}$	Forms a one's complement of the contents of memory, and stores it into memory.													44	5	2			
CPX	X−M	Compares the contents of index register X and memory.				E0	2	2							E4	3	2			
CPY	Y−M	Compares the contents of index register Y and memory.				C0	2	2							C4	3	2			
DEC	A←A−1 or M←M−1	Decrements the contents of the accumulator or memory by 1.							1A	2	1				C6	5	2			
DEX	X←X−1	Decrements the contents of index register X by 1.	CA	2	1															
DEY	Y←Y−1	Decrements the contents of index register Y by 1.	88	2	1															
DIV	A←(M(zz+X+1), M(zz+X))/A M(S) ← 1's complement of Remainder S←S−1	Divides the 16-bit data that is the contents of M(zz+x+1) for high byte and the contents of M(zz+x) for low byte by the accumulator. Stores the quotient in the accumulator and the 1's complement of the remainder on the stack.																		
EOR (Note 1)	When T=0 A←A¥M When T=1 M(X)←M(X)¥M	"Exclusive-ORs" the contents of accumulator and memory. The results are stored in the accumulator. "Exclusive-ORs" the contents of the memory specified by the addressing mode and the contents of the memory at the address indicated by index register X. The results are stored into the memory at the address indicated by index register X.				49	2	2							45	3	2			
INC	A←A+1 or M←M+1	Increments the contents of accumulator or memory by 1.							3A	2	1				E6	5	2			
INX	X←X+1	Increments the contents of index register X by 1.	E8	2	1															
INY	Y←Y+1	Increments the contents of index register Y by 1.	C8	2	1															

Addressing mode																														Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
																											50	2	2				•	•	•	•	•	•	•	•
																											70	2	2				•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	0
																																	•	•	•	•	0	•	•	•
																																	•	•	•	•	•	0	•	•
																																	•	•	0	•	•	•	•	•
																																	•	0	•	•	•	•	•	•
D5	4	2				CD	4	3	DD	5	3	D9	5	3							C1	6	2	D1	6	2							N	•	•	•	•	•	Z	C
																																	N	•	•	•	•	•	Z	•
						EC	4	3																									N	•	•	•	•	•	Z	C
						CC	4	3																									N	•	•	•	•	•	Z	C
D6	6	2				CE	6	3	DE	7	3																						N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
E2	16	2																															•	•	•	•	•	•	•	•
55	4	2				4D	4	3	5D	5	3	59	5	3							41	6	2	51	6	2							N	•	•	•	•	•	Z	•
F6	6	2				EE	6	3	FE	7	3																						N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
JMP	If addressing mode is ABS $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$ If addressing mode is IND $PC_L \leftarrow M(AD_H, AD_L)$ $PC_H \leftarrow M(AD_H, AD_L+1)$ If addressing mode is ZP, IND $PC_L \leftarrow M(00, AD_L)$ $PC_H \leftarrow M(00, AD_L+1)$	Jumps to the specified address.																		
JSR	$M(S) \leftarrow PC_H$ $S \leftarrow S-1$ $M(S) \leftarrow PC_L$ $S \leftarrow S-1$ After executing the above, if addressing mode is ABS, $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$ If addressing mode is SP, $PC_L \leftarrow AD_L$ $PC_H \leftarrow FF$ If addressing mode is ZP, IND, $PC_L \leftarrow M(00, AD_L)$ $PC_H \leftarrow M(00, AD_L+1)$	After storing contents of program counter in stack, and jumps to the specified address.																		
LDA (Note 2)	When T=0 A←M When T=1 M(X)←M	Load accumulator with contents of memory. Load memory indicated by index register X with contents of memory specified by the addressing mode.				A9	2	2							A5	3	2			
LDM	M←nn	Load memory with immediate value.													3C	4	3			
LDX	X←M	Load index register X with contents of memory.				A2	2	2							A6	3	2			
LDY	Y←M	Load index register Y with contents of memory.				A0	2	2							A4	3	2			
LSR	7 0 0 → □ → C	Shift the contents of accumulator or memory to the right by one bit. The low order bit of accumulator or memory is stored in carry, 7th bit is cleared.							4A	2	1				46	5	2			
MUL	M(S)·A←A×M(zz+X) S←S− 1	Multiplies the accumulator with the contents of memory specified by the zero page X addressing mode and stores the high byte of the result on the stack and the low byte in the accumulator.																		
NOP	PC←PC+1	No operation.	EA	2	1															
ORA (Note 1)	When T=0 A←AVM When T=1 M(X)←M(X)VM	"Logical OR's" the contents of memory and accumulator. The result is stored in the accumulator. "Logical OR's" the contents of memory indicated by index register X and contents of memory specified by the addressing mode. The result is stored in the memory specified by index register X.				09	2	2							05	3	2			

Addressing mode																													Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
						4C	3	3							6C	5	3	B2	4	2												•	•	•	•	•	•	•	•
						20	6	3										02	7	2										22	5	2	•	•	•	•	•	•	•	•
B5	4	2				AD	4	3	BD	5	3	B9	5	3							A1	6	2	B1	6	2							N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
			B6	4	2	AE	4	3				BE	5	3																			N	•	•	•	•	•	Z	•
B4	4	2				AC	4	3	BC	5	3																						N	•	•	•	•	•	Z	•
56	6	2				4E	6	3	5E	7	3																						0	•	•	•	•	•	Z	C
62	15	2																															•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
15	4	2				0D	4	3	1D	5	3	19	5	3							01	6	2	11	6	2							N	•	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#
PHA	M(S)←A S←S−1	Saves the contents of the accumulator in memory at the address indicated by the stack pointer and decrements the contents of stack pointer by 1.	48	3	1															
PHP	M(S)←PS S←S−1	Saves the contents of the processor status register in memory at the address indicated by the stack pointer and decrements the contents of the stack pointer by 1.	08	3	1															
PLA	S←S+1 A←M(S)	Increments the contents of the stack pointer by 1 and restores the accumulator from the memory at the address indicated by the stack pointer.	68	4	1															
PLP	S←S+1 PS←M(S)	Increments the contents of stack pointer by 1 and restores the processor status register from the memory at the address indicated by the stack pointer.	28	4	1															
ROL		Shifts the contents of the memory or accumulator to the left by one bit. The high order bit is shifted into the carry flag and the carry flag is shifted into the low order bit.							2A	2	1				26	5	2			
ROR		Shifts the contents of the memory or accumulator to the right by one bit. The low order bit is shifted into the carry flag and the carry flag is shifted into the high order bit.							6A	2	1				66	5	2			
RRF		Rotates the contents of memory to the right by 4 bits.													82	8	2			
RTI	S←S+1 PS←M(S) S←S+1 PC_L←M(S) S←S+1 PC_H←M(S)	Returns from an interrupt routine to the main routine.	40	6	1															
RTS	S←S+1 PC_L←M(S) S←S+1 PC_H←M(S)	Returns from a subroutine to the main routine.	60	6	1															
SBC (Note 1) (Note 5)	When T=0 A←A−M−$\overline{C}$ When T=1 M(X)←M(X)−M−$\overline{C}$	Subtracts the contents of memory and complement of carry flag from the contents of accumulator. The results are stored into the accumulator. Subtracts contents of complement of carry flag and contents of the memory indicated by the addressing mode from the memory at the address indicated by index register X. The results are stored into the memory of the address indicated by index register X.				E9	2	2							E5	3	2			
SEB	A_b or M_b←1	Sets the specified bit in the accumulator or memory to "1."										0B+2i	2	1				0F+2i	5	2
SEC	C←1	Sets the contents of the carry flag to "1."	38	2	1															
SED	D←1	Sets the contents of the decimal mode flag to "1."	F8	2	1															
SEI	I←1	Sets the contents of the interrupt disable flag to "1."	78	2	1															
SET	T←1	Sets the contents of the index X mode flag to "1."	32	2	1															

Addressing mode																														Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
36	6	2				2E	6	3	3E	7	3																						N	•	•	•	•	•	Z	C
76	6	2				6E	6	3	7E	7	3																						N	•	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	(Value saved in stack)							
																																	•	•	•	•	•	•	•	•
F5	4	2				ED	4	3	FD	5	3	F9	5	3							E1	6	2	F1	6	2							N	V	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	1
																																	•	•	•	•	1	•	•	•
																																	•	•	•	•	•	1	•	•
																																	•	•	1	•	•	•	•	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#
STA	M←A	Stores the contents of accumulator in memory.													85	4	2			
STP		Stops the oscillator.	42	2	1															
STX	M←X	Stores the contents of index register X in memory.													86	4	2			
STY	M←Y	Stores the contents of index register Y in memory.													84	4	2			
TAX	X←A	Transfers the contents of the accumulator to index register X.	AA	2	1															
TAY	Y←A	Transfers the contents of the accumulator to index register Y.	A8	2	1															
TST	M=0?	Tests whether the contents of memory are "0" or not.													64	3	2			
TSX	X←S	Transfers the contents of the stack pointer to index register X.	BA	2	1															
TXA	A←X	Transfers the contents of index register X to the accumulator.	8A	2	1															
TXS	S←X	Transfers the contents of index register X to the stack pointer.	9A	2	1															
TYA	A←Y	Transfers the contents of index register Y to the accumulator.	98	2	1															
WIT		Stops the internal clock.	C2	2	1															

Note 1 : The number of cycles "n" is increased by 3 when T is 1.
2 : The number of cycles "n" is increased by 2 when T is 1.
3 : The number of cycles "n" is increased by 1 when T is 1.
4 : The number of cycles "n" is increased by 2 when branching has occurred.
5 : N, V, and Z flags are invalid in decimal operation mode.

APPENDIX

Appendix 7 Machine Instruction

Addressing mode																												Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	N	V	T	B	D	I	Z	C
95	5	2				8D	5	3	9D	6	3	99	6	3							81	7	2	91	7	2							•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
			96	5	2	8E	5	3																									•	•	•	•	•	•	•	•
94	5	2				8C	5	3																									•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•

Symbol	Contents
IMP	Implied addressing mode
IMM	Immediate addressing mode
A	Accumulator or Accumulator addressing mode
BIT, A	Accumulator bit relative addressing mode
ZP	Zero page addressing mode
BIT, ZP	Zero page bit relative addressing mode
ZP, X	Zero page X addressing mode
ZP, Y	Zero page Y addressing mode
ABS	Absolute addressing mode
ABS, X	Absolute X addressing mode
ABS, Y	Absolute Y addressing mode
IND	Indirect absolute addressing mode
ZP, IND	Zero page indirect absolute addressing mode
IND, X	Indirect X addressing mode
IND, Y	Indirect Y addressing mode
REL	Relative addressing mode
SP	Special page addressing mode
C	Carry flag
Z	Zero flag
I	Interrupt disable flag
D	Decimal mode flag
B	Break flag
T	X-modified arithmetic mode flag
V	Overflow flag
N	Negative flag

Symbol	Contents
+	Addition
−	Subtraction
∧	Logical OR
∨	Logical AND
∀	Logical exclusive OR
—	Negation
←	Shows direction of data flow
X	Index register X
Y	Index register Y
S	Stack pointer
PC	Program counter
PS	Processor status register
PC_H	8 high-order bits of program counter
PC_L	8 low-order bits of program counter
AD_H	8 high-order bits of address
AD_L	8 low-order bits of address
FF	FF in Hexadecimal notation
nn	Immediate value
M	Memory specified by address designation of any addressing mode
M (X)	Memory of address indicated by contents of index register X
M (S)	Memory of address indicated by contents of stack pointer
M(AD_H, AD_L)	Contents of memory at address indicated by AD_H and AD_L, in AD_H is 8 high-order bits and AD_L is 8 low-order bits.
M(00, AD_L)	Contents of address indicated by zero page AD_L
A_b	1 bit of accumulator
M_b	1 bit of memory
OP	Opcode
n	Number of cycles
#	Number of bytes

Appendix 8 List of Instruction Code

D4~D7 \ D3~D0	Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	BRK	ORA IND,X	JSR ZP,IND	BBS 0,A	—	ORA ZP	ASL ZP	BBS 0,ZP	PHP	ORA IMM	ASL A	SEB 0,A	—	ORA ABS	ASL ABS	SEB 0,ZP
0001	1	BPL	ORA IND,Y	CLT	BBC 0,A	—	ORA ZP,X	ASL ZP,X	BBC 0,ZP	CLC	ORA ABS,Y	DEC A	CLB 0,A	—	ORA ABS,X	ASL ABS,X	CLB 0,ZP
0010	2	JSR ABS	AND IND,X	JSR SP	BBS 1,A	BIT ZP	AND ZP	ROL ZP	BBS 1,ZP	PLP	AND IMM	ROL A	SEB 1,A	BIT ABS	AND ABS	ROL ABS	SEB 1,ZP
0011	3	BMI	AND IND,Y	SET	BBC 1,A	—	AND ZP,X	ROL ZP,X	BBC 1,ZP	SEC	AND ABS,Y	INC A	CLB 1,A	LDM ZP	AND ABS,X	ROL ABS,X	CLB 1,ZP
0100	4	RTI	EOR IND,X	STP	BBS 2,A	COM ZP	EOR ZP	LSR ZP	BBS 2,ZP	PHA	EOR IMM	LSR A	SEB 2,A	JMP ABS	EOR ABS	LSR ABS	SEB 2,ZP
0101	5	BVC	EOR IND,Y	—	BBC 2,A	—	EOR ZP,X	LSR ZP,X	BBC 2,ZP	CLI	EOR ABS,Y	—	CLB 2,A	—	EOR ABS,X	LSR ABS,X	CLB 2,ZP
0110	6	RTS	ADC IND,X	MUL ZP,X	BBS 3,A	TST ZP	ADC ZP	ROR ZP	BBS 3,ZP	PLA	ADC IMM	ROR A	SEB 3,A	JMP IND	ADC ABS	ROR ABS	SEB 3,ZP
0111	7	BVS	ADC IND,Y	—	BBC 3,A	—	ADC ZP,X	ROR ZP,X	BBC 3,ZP	SEI	ADC ABS,Y	—	CLB 3,A	—	ADC ABS,X	ROR ABS,X	CLB 3,ZP
1000	8	BRA	STA IND,X	RRF ZP	BBS 4,A	STY ZP	STA ZP	STX ZP	BBS 4,ZP	DEY	—	TXA	SEB 4,A	STY ABS	STA ABS	STX ABS	SEB 4,ZP
1001	9	BCC	STA IND,Y	—	BBC 4,A	STY ZP,X	STA ZP,X	STX ZP,X	BBC 4,ZP	TYA	STA ABS,Y	TXS	CLB 4,A	—	STA ABS,X	—	CLB 4,ZP
1010	A	LDY IMM	LDA IND,X	LDX IMM	BBS 5,A	LDY ZP	LDA ZP	LDX ZP	BBS 5,ZP	TAY	LDA IMM	TAX	SEB 5,A	LDY ABS	LDA ABS	LDX ABS	SEB 5,ZP
1011	B	BCS	LDA IND,Y	JMP ZP,IND	BBC 5,A	LDY ZP,X	LDA ZP,X	LDX ZP,Y	BBC 5,ZP	CLV	LDA ABS,Y	TSX	CLB 5,A	LDY ABS,X	LDA ABS,X	LDX ABS,Y	CLB 5,ZP
1100	C	CPY IMM	CMP IND,X	WIT	BBS 6,A	CPY ZP	CMP ZP	DEC ZP	BBS 6,ZP	INY	CMP IMM	DEX	SEB 6,A	CPY ABS	CMP ABS	DEC ABS	SEB 6,ZP
1101	D	BNE	CMP IND,Y	—	BBC 6,A	—	CMP ZP,X	DEC ZP,X	BBC 6,ZP	CLD	CMP ABS,Y	—	CLB 6,A	—	CMP ABS,X	DEC ABS,X	CLB 6,ZP
1110	E	CPX IMM	SBC IND,X	DIV ZP,X	BBS 7,A	CPX ZP	SBC ZP	INC ZP	BBS 7,ZP	INX	SBC IMM	NOP	SEB 7,A	CPX ABS	SBC ABS	INC ABS	SEB 7,ZP
1111	F	BEQ	SBC IND,Y	—	BBC 7,A	—	SBC ZP,X	INC ZP,X	BBC 7,ZP	SED	SBC ABS,Y	—	CLB 7,A	—	SBC ABS,X	INC ABS,X	CLB 7,ZP

Appendix 9 Mask ROM Ordering Method

Please send the following data for a mask order.
(1) Mask ROM order confirmation form
(2) Mark specification form
(3) Three copies of the ROM data.....three EPROMs

GZZ—SH03—26A〈9YA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38063M6-XXXFP/GP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

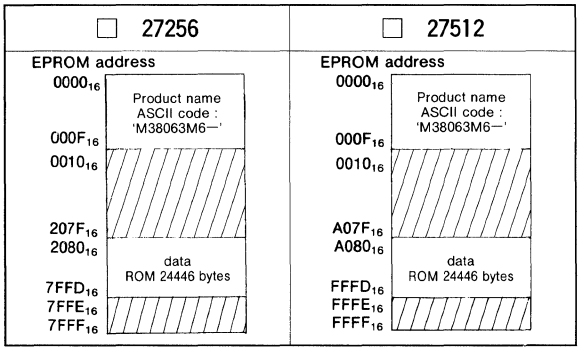
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name ☐ M38063M6-XXXFP ☐ M38063M6-XXXGP

Checksum code for entire EPROM ☐☐☐☐ (hexadecimal notation)

EPROM type (indicate the type used)



In the address space of the microcomputer, the internal ROM area is from address $A080_{16}$ to $FFFD_{16}$. The reset vector is stored in addresses $FFFC_{16}$ and $FFFD_{16}$.

(1) Set the data in the unused area (the shaded area of the diagram) to "FF_{16}".
(2) The ASCII codes of the product name 'M38063M6-' must be entered in addresses 0000_{16} to 0008_{16}. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address		Address	
0000_{16}	'M' = $4D_{16}$	0008_{16}	'—' = $2D_{16}$
0001_{16}	'3' = 33_{16}	0009_{16}	FF_{16}
0002_{16}	'8' = 38_{16}	$000A_{16}$	FF_{16}
0003_{16}	'0' = 30_{16}	$000B_{16}$	FF_{16}
0004_{16}	'6' = 36_{16}	$000C_{16}$	FF_{16}
0005_{16}	'3' = 33_{16}	$000D_{16}$	FF_{16}
0006_{16}	'M' = $4D_{16}$	$000E_{16}$	FF_{16}
0007_{16}	'6' = 36_{16}	$000F_{16}$	FF_{16}

GZZ—SH03—26A〈9YA0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38063M6-XXXFP/GP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program.

EPROM type	27256	27512
The pseudo-command	*=△$8000 .BYTE△ 'M38063M6—'	*=△$0000 .BYTE△ 'M38063M6—'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N for M38063M6-XXXFP, 80P6S for M38063M6-XXXGP) and attach it to the mask ROM confirmation form.

※ 3. Delivery standard

Choose the format of the specifications for the product to be delivered.

(1) Specifications for each ROM

☐ ROM code list unnecessary (standard).

☐ ROM code list necessary.

Note that each format has the same scope of guarantee. Therefore, the standard format is recommended.

※ 4. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator ?

☐ Ceramic resonator ☐ Quartz crystal

☐ External clock input ☐ Other ( )

At what frequency ? $f(X_{IN})$= ☐ MHz

(2) In which operation mode will you use your microcomputer ?

☐ Single-chip mode ☐ Memory expansion mode

☐ Microprocessor mode

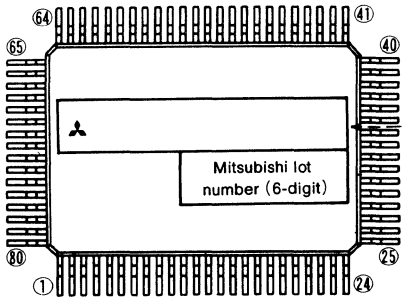
※ 5. Comments

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

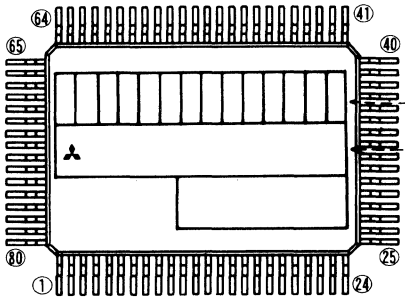
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi Catalog Name



Note : The fonts and size of characters are standard Mitsubishi type.

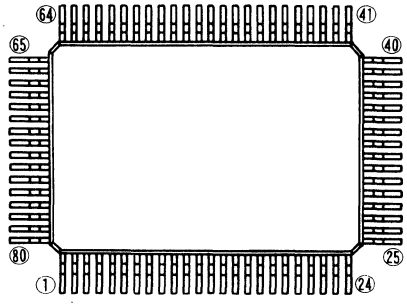
Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.

Note3 : Customer's parts number can be up to 14 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, · (period), and, (commas) are usable.

4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

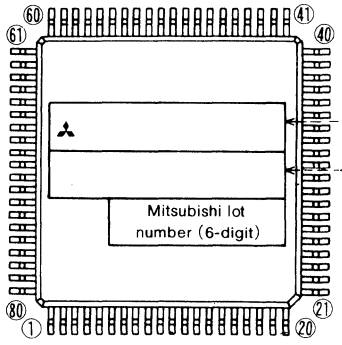
The standard Mitsubishi font is used for all characters except for a logo.

80P6S (80-PIN QFP) MARK SPECIFICATION FORM

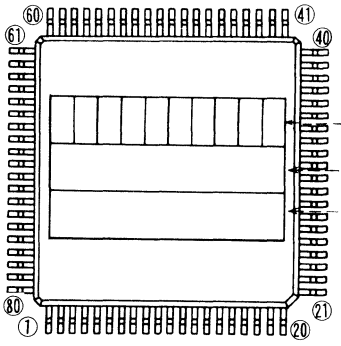
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

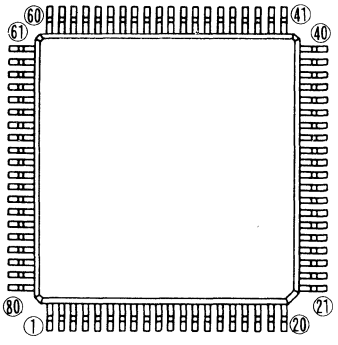


B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type. (The character size become smaller than A (standard Mitsubishi mark) type)

C. Special Mark Required



Note3 : Customer's parts number can be up to 10 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, · (period), and, (commas) are usable.

4 : If the Mitsubishi logo ⅄ is not required, check the box below.

⅄ Mitsubishi logo is not required ☐

5 : Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo ⅄ is required or not.

Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

The standard Mitsubishi font is used for all characters except for a logo.

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