Advance Information

MC68(7)05R/U
SERIES

8-BIT
MICROCOMPUTERS

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SECTION 1
INTRODUCTION

The M6805 Family of low-cost single-chip microcomputers was designed for the user who needs an economical microcomputer with the proven capabilities of the M6800-based instruction set. This rapidly expanding family includes a number of memory and package sizes with various I/O functions in both HMOS and CMOS.

This document describes the eight 8-bit high-density N-channel silicon-gate microcomputers which comprise the MC68(7)05R/U series. These devices are listed below:

MC6805R2	MC6805R3	MC68705R3	MC68705R5
MC6805U2	MC6805U3	MC68705U3	MC68705U5

These eight devices are 8-bit high-density N-channel silicon-gate microcomputers. They are available in 40-pin dual-in-line packages.

1.1 DEVICE FEATURES

The following tables summarize the hardware and software features of each device. Differences between the devices will be highlighted throughout this document when applicable.

HARDWARE FEATURES

	MC6805R2	MC6805R3	MC6805U2	MC6805U3	MC68705R3	MC68705U3	MC68705R5	MC68705U5
24 Bidirectional I/O Lines	X	X	X	X	X	X	X	X
Eight Input-Only Lines	X	X	X	X	X	X	X	X
A/D Converter	X	X	—	—	X	—	X	—
User ROM (Bytes)	2048	3776	2048	3776	—	—	—	—
User EPROM (Bytes)	—	—	—	—	3776	3776	3776	3776
RAM (Bytes)	64	112	64	112	112	112	112	112
Self-Check Mode	X	X	X	X	—	—	—	—
Zero/Crossing Detect/Interrupt	X	X	X	X	X	X	X	X
Timer with 7-Bit Prescaler	X	X	X	X	X	X	X	X
Programmable Prescaler	—	—	X	X	X	X	X	X
5-Volt Single Supply	X	X	X	X	X	X	X	X
Memory Mapped I/O	X	X	X	X	X	X	X	X
On-Chip EPROM Programmer	—	—	—	—	X	X	X	X
EPROM Security Feature	—	—	—	—	—	—	X	X

SOFTWARE FEATURES

	MC6805R2	MC6805R3	MC6805U2	MC6805U3	MC68705R3	MC68705U3	MC68705R5	MC68705U5
Addressing Modes	10	10	10	10	10	10	10	10
Byte Efficient Instruction Set	X	X	X	X	X	X	X	X
True Bit Manipulation	X	X	X	X	X	X	X	X
Bit Test and Branch Instructions	X	X	X	X	X	X	X	X
Versatile Interrupt Handling	X	X	X	X	X	X	X	X
Versatile Index Register	X	X	X	X	X	X	X	X
Powerful Indexed Addressing for Tables	X	X	X	X	X	X	X	X
Full Set of Conditional Branches	X	X	X	X	X	X	X	X
Memory Usable as Registers/Flags	X	X	X	X	X	X	X	X
Single Instruction Memory Examine/Change	X	X	X	X	X	X	X	X
User Callable Self-Check Subroutines	X	X	X	X	−	−	−	−
Complete Development System Support on EXORciser	X	X	X	X	X	X	X	X
Supported by EPROM Version	X	X	X	X	−	−	−	−

1.2 HARDWARE

Every M6805 Family microcomputer contains hardware common to all versions, plus a combination of options unique to a particular version. Figures 1-1 through 1-6 illustrate the unique options available on the eight versions described in this document.

EXORciser is a registered trademark of Motorola Inc.
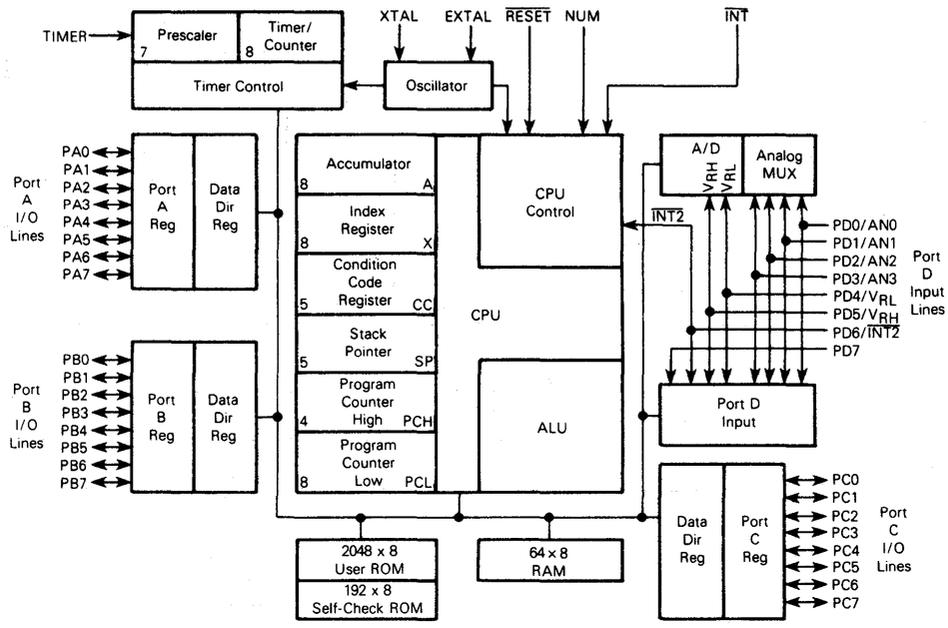
Figure 1-1. MC6805R2 Block Diagram
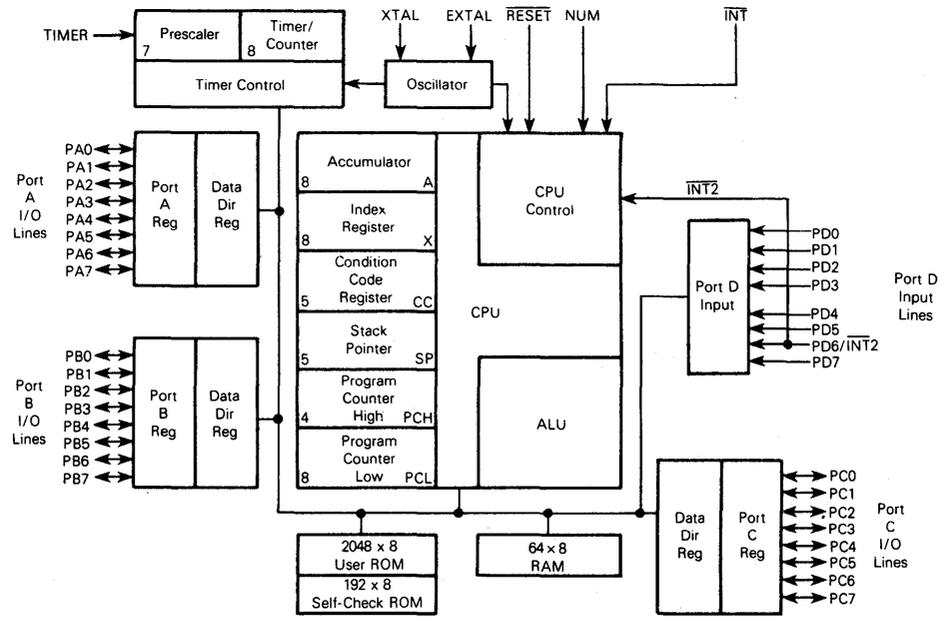
Figure 1-2. MC6805U2 Block Diagram
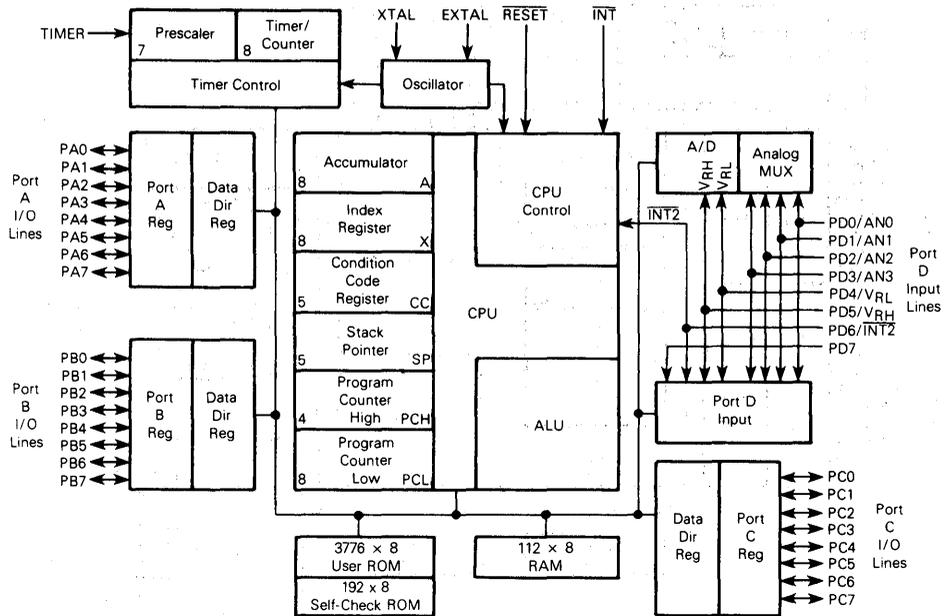
Figure 1-3. MC6805R3 Block Diagram
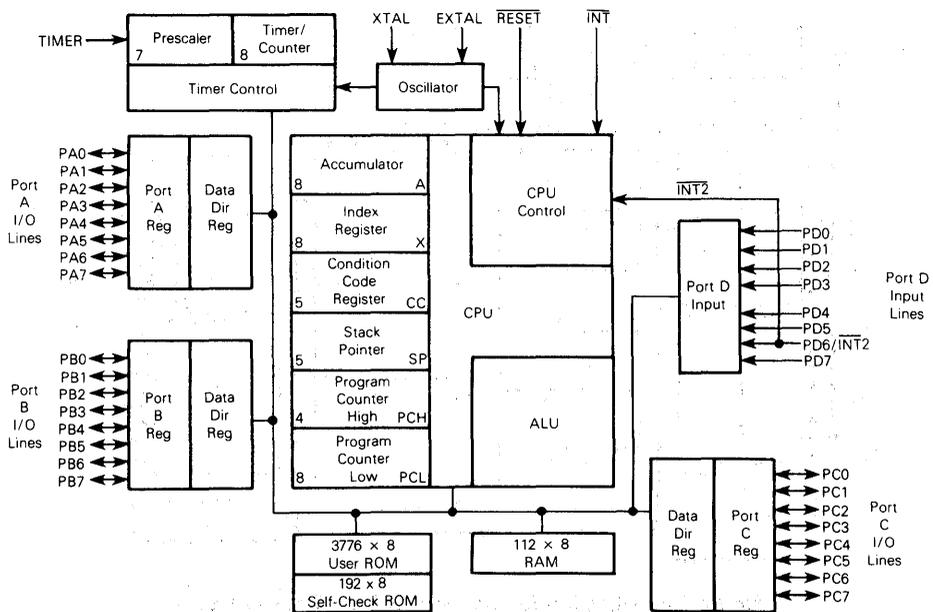
Figure 1-4. MC6805U3 Block Diagram
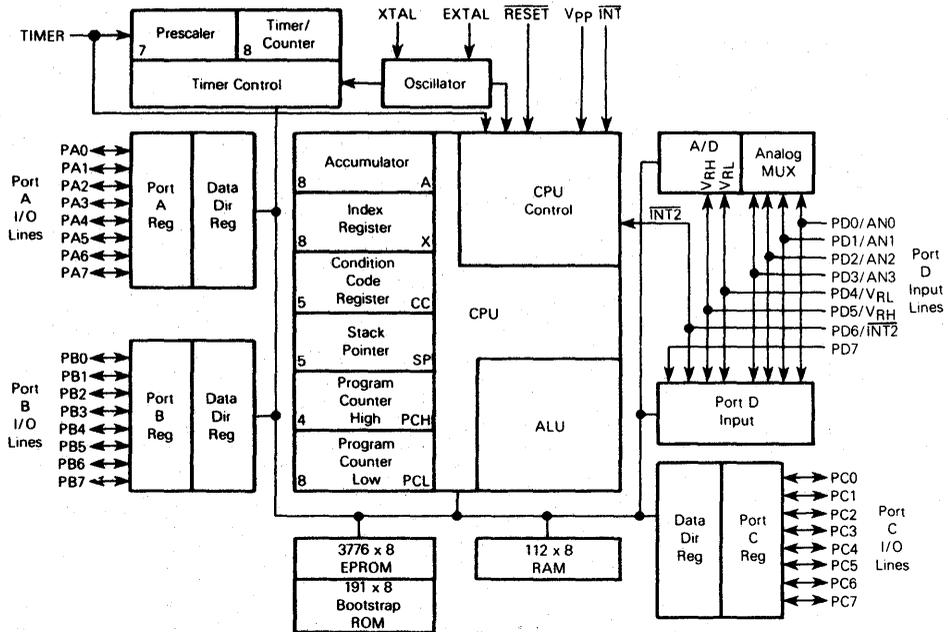
Figure 1-5. MC68705R3 and MC68705R5 Block Diagram
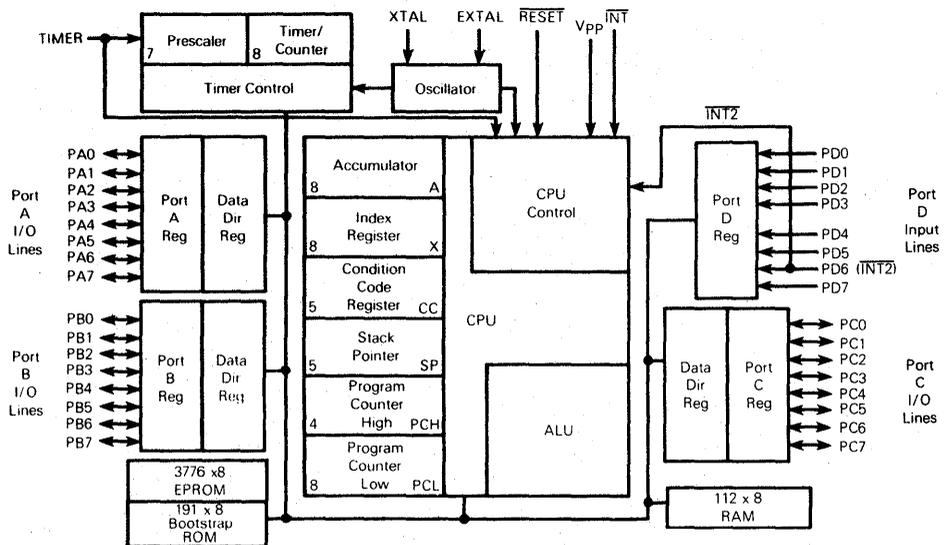
Figure 1-6. MC68705U3 and MC68705U5 Block Diagram

SECTION 2
SIGNAL DESCRIPTION

The following paragraphs contain brief descriptions of the input and output signals. Where applicable reference has been made to other sections that contain more detail about the function being performed.

2.1 V_{CC} AND V_{SS}

Power is supplied to the microcomputers using these two pins. V_{CC} is power and V_{SS} is the ground connection.

2.2 $\overline{INT}$

This pin provides the capability for asynchronously applying an external interrupt to the microcomputer. Refer to **SECTION 7 RESET, CLOCK, AND INTERRUPT STRUCTURE** for additional information regarding the interrupt operation.

2.3 EXTAL AND XTAL

These pins provide control input for the on-chip clock oscillator circuit. A crystal, a resistor, or an external signal, depending on user selectable manufacturing mask option, can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized. Refer to **SECTION 7 RESET, CLOCK, AND INTERRUPT STRUCTURE** for recommendations about these inputs.

2.4 TIMER

This pin is used as an external input to control the internal timer/counter circuitry. On the MC68705R3, MC68705U3, MC68705R5, and MC68705U5 versions, this pin also detects a higher voltage level used to initiate the bootstrap program for loading the internal EPROM (see **SECTION 10 SOFTWARE**). On the MC6805R2, MC6805U2, MC6805R3, and MC6805U3 this pin also detects a higher voltage level used to initiate the self-test program (see **SECTION 6 SELF CHECK**).

Refer to **SECTION 5 TIMER** for more detailed information about the timer circuitry.

2.5 $\overline{RESET}$

This pin has a Schmitt trigger input and an on-chip pullup. The microcomputer can be reset by pulling $\overline{RESET}$ low. Refer to **SECTION 7 RESET, CLOCK, AND INTERRUPT STRUCTURE** for additional information.

2.6 NUM (NON-USER MODE)

Pin 7 of the MC6805R2 and MC6805U2 is identified as NUM (non-user mode). This pin is not for user application and must be connected to V_{SS}.

2.7 V_{PP}

This pin is used when programming the EPROM versions (MC68705R3, MC68705U3, MC68705R5, and MC68705U5). By applying the programming voltage to this pin, one of the requirements is met for programming the EPROMs. In normal operation, this pin is connected to V_{CC}. Refer to **SECTION 9 MASK OPTIONS AND PROGRAMMING** for more detailed information.

2.8 INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7)

These 32 lines are arranged into four 8-bit ports (A, B, C, and D). Ports A, B, and C are programming as either inputs or outputs under software control of the data direction registers.

For the MC6805U2, MC6805U3, MC68705U3, and MC68705U5 port D is for digital input only and bit 6 may be used for a second interrupt ($\overline{INT2}$). Refer to **SECTION 7 RESET, CLOCK, AND INTERRUPT STRUCTURE** and **SECTION 8 INPUT/OUTPUT CIRCUITRY AND ANALOG-TO-DIGITAL CONVERTER** for additional information.

For the MC6805R2, MC6805R3, MC68705R3, and MC68705R5 port D has up to four analog inputs, plus two voltage reference inputs when the analog-to-digital converter is used (PD5/V_{RH}, PD4/V_{RL}) and an $\overline{INT2}$ input. All port D lines can be read directly and used as binary inputs. If any analog input is used, then the voltage reference pins (PD5/V_{RH}, PD4/V_{RL}) must be used in the analog mode. Refer to **SECTION 7 RESET, CLOCK, AND INTERRUPT STRUCTURE** and **SECTION 8 INPUT/OUTPUT CIRCUITRY AND ANALOG-TO-DIGITAL CONVERTER** for additional information.

SECTION 3
MEMORY CONFIGURATIONS

Each member of the MC68(7)05R/U series of microcomputers is capable of addressing 4096 bytes of memory and I/O registers. The memory maps for the eight versions of the M6805 Family described in this document are shown in Figures 3-1 through 3-6. The amount of ROM, EPROM, and RAM for each device is detailed in 1.1 DEVICE FEATURES.

3.1 MC6805U2 MEMORY MAP

The memory map for the MC6805U2 is shown in Figure 3-1. From $FF8 to $FFF are the interrupt and RESET vectors. A self-check ROM occupies 192 bytes from $F38 to $FF7. The user ROM is
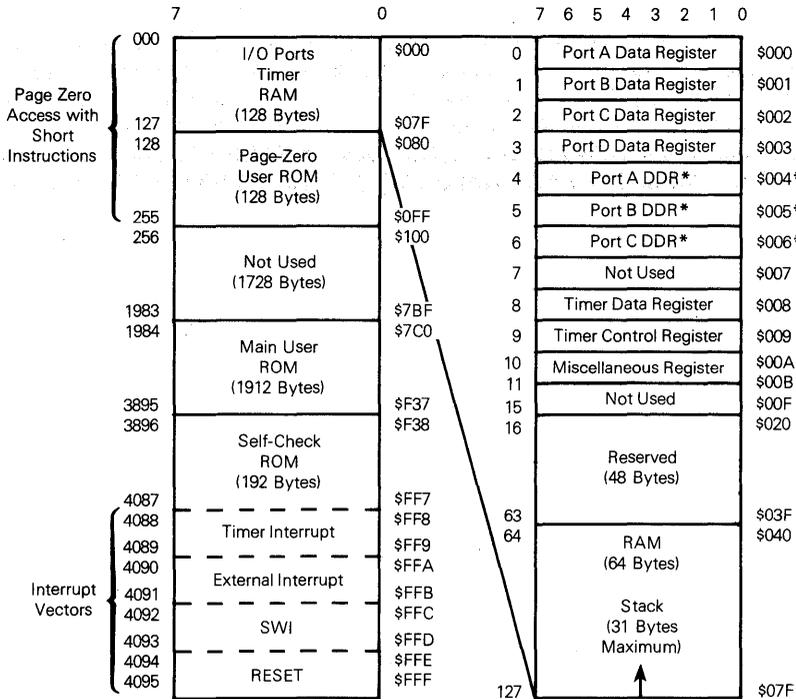
* Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 3-1. MC6805U2 Memory Map

divided into two portions located from $080 to $0FF and $7C0 to $F37. The portioning allows 128 bytes of ROM to be addressed with direct instructions. A RAM area of 64 bytes occupies $040 to $07F. Only the 31 bytes from $061 to $07F can be used for the stack RAM due to the limitation imposed by the 5-bit stack pointer. The data direction, peripheral data, timer, and miscellaneous registers are located from $000 to $00F.

3.2 MC6805R2 MEMORY MAP

The memory map for the MC6805R2 is shown in Figure 3-2 and is identical to the MC6805U2 except that two additional registers, the analog-to-digital control register and the analog-to-digital result register, have been added at locations $00E and $00F, respectively.
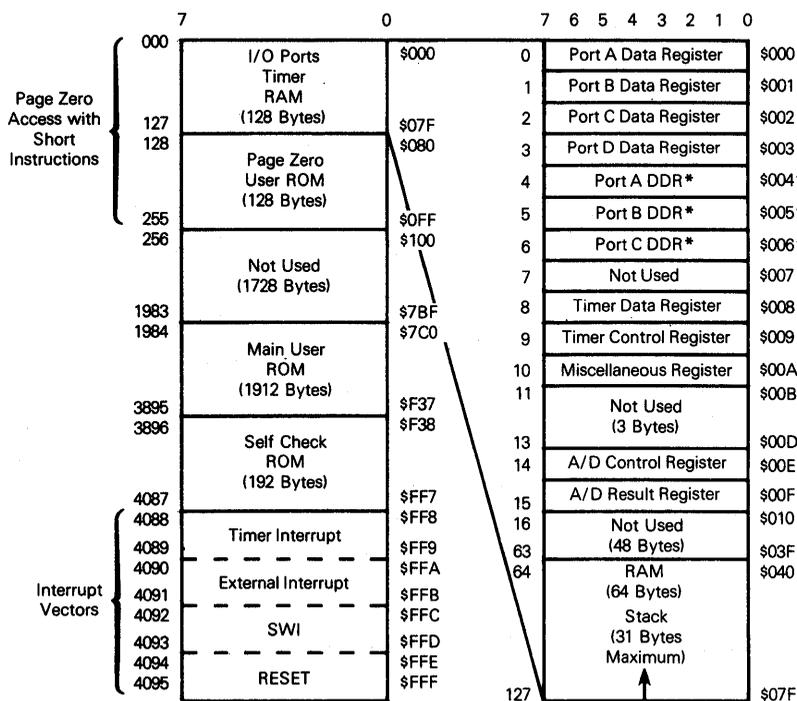
*Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 3-2. MC6805R2 Memory Map

3.3 MC6805U3 MEMORY MAP

The memory map for the MC6805U3 is shown in Figure 3-3. The MC6805U3 has an expanded ROM and RAM area over the MC6805U2. The user ROM in the MC6805U3 consists of 3768 bytes from $080 to $F37. The RAM is expanded to 112 bytes from $010 to $07F. All other registers remain identical to the MC6805U2. The 5-bit stack pointer still allows only 31 bytes of RAM to be used as stack area.

* Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 3-3. MC6805U3 Memory Map

3.4 MC6805R3 MEMORY MAP

The memory map for the MC6805R3 is shown in Figure 3-4 and is identical to the MC6805U3 except that two additional registers, the analog-to-digital control register and the analog-to-digital result register, have been added at locations $00E and $00F, respectively.
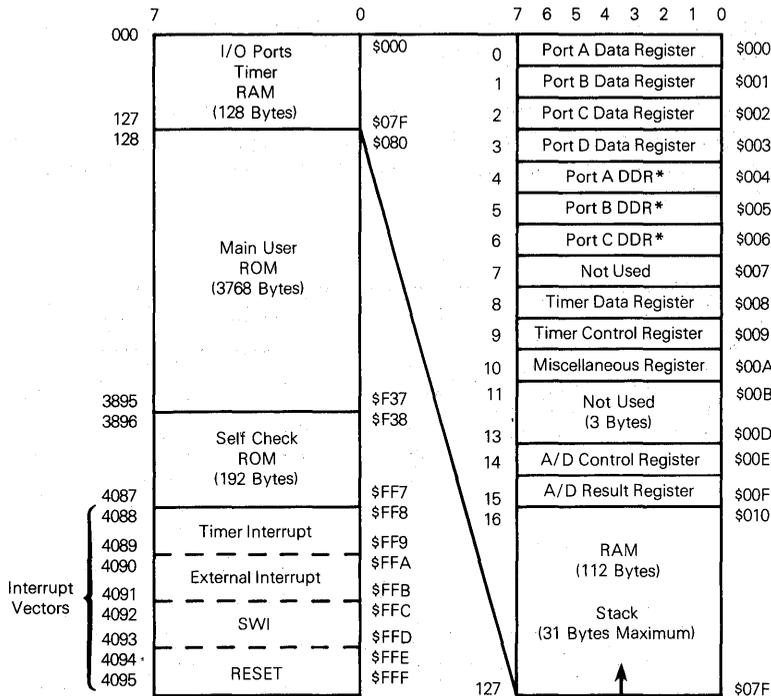
* Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 3-4. MC6805R3 Memory Map

3.5 MC68705U3 and MC68705U5 MEMORY MAP

The memory maps for the MC68705U3 and MC68705U5 are shown in Figure 3-5 and are identical to the masked programmed equivalent, the MC6805U3, with respect to RAM, ROM, I/O, special purpose registers, and interrupt and RESET vectors. The ROM area ($080 to $F37) of the MC68705U3 and MC68705U5 is an ultraviolet erasable EPROM.

A bootstrap ROM is located between $F39 and $FF7 which allows the MC68705U3 and MC68705U5 to program their own EPROMs. The bootstrap is a mask programmed ROM.

At location $F38 is the mask option register (MOR) which is an EPROM byte. It allows the user to set up the MC68705U3 and the MC68705U5 for a crystal or RC oscillator, set the timer prescaler, the clock source, etc. In addition, the mask option register allows the user to select the secure mode offered by the MC68705U5.
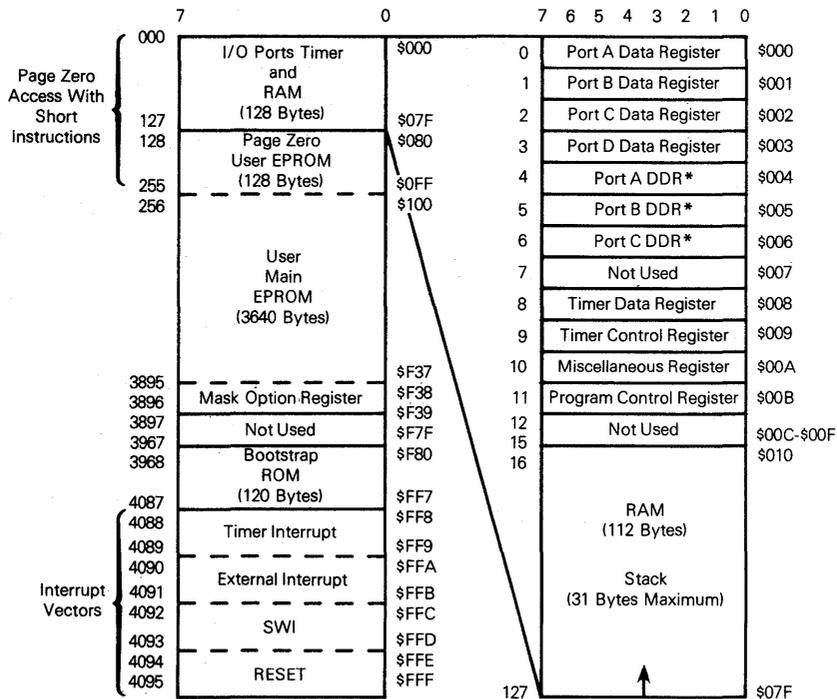
* Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 3-5. MC68705U3 and MC68705U5 Memory Map

3.6 MC68705R3 and MC68705R5 MEMORY MAP

The memory maps for the MC68705R3 and MC68705R5 are shown in Figure 3-6 and are identical to the MC68705U3 and MC68705U5 except that two additional registers, the analog-to-digital control register and the analog-to-digital result register have been added at locations $00E and $00F, respectively.

The MC68705U3/MC68705U5 and MC68705R3/MC68705R5 are intended to exactly emulate the MC6805U3 and MC6805R3 respectively.

7	0	7 6 5 4 3 2 1 0	
Page Zero Access With Short Instructions 000	I/O Ports Timer RAM (128 Bytes) $000	0 Port A Data Register	$000
127	$07F	1 Port B Data Register	$001
128	Page Zero User EPROM (128 Bytes) $080	2 Port C Data Register	$002
255	$0FF	3 Port D Data Register	$003
256	$100	4 Port A DDR*	$004*
	User Main EPROM (3640 Bytes)	5 Port B DDR*	$005*
		6 Port C DDR*	$006*
		7 Not Used	$007
		8 Timer Data Register	$008
		9 Timer Control Register	$009
3895	$F37	10 Miscellaneous Register	$00A
3896	Mask Option Register $F38	11 Program Control Register	$00B
3897	$F39	12 Not Used	$00C
3967	Not Used $F7F	13 Not Used	$00D
3968	Bootstrap ROM (120 Bytes) $F80	14 A/D Control Register	$00E
4087	$FF7	15 A/D Register	$00F
4088	$FF8	16	$010
4089	Timer Interrupt $FF9	RAM (112 Bytes)	
4090	$FFA		
Interrupt Vectors 4091	External Interrupt $FFB		
4092	$FFC	Stack (31 Bytes Maximum)	
4093	SWI $FFD		
4094	$FFE		
4095	Reset $FFF	127	$07F

*Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 3-6. MC68705R3 and MC68705R5 Memory Map

3.7 SHARED STACK AREA

The shared stack area (RAM locations $061-$07F) is used during the processing of an interrupt or subroutine call to save the contents of the central processing unit state. The register contents are pushed onto the stack in the order shown in Figure 3-7. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program counter is stacked first, then the high order four bits (PCH) are stacked. This ensures that the program counter is loaded correctly during pulls from the stack since the stack pointer increments when it pulls data from the stack. A subroutine call results in only the program counter (PCL, PCH) contents being pushed onto the stack; the remaining CPU registers are not pushed. The shared stack area must be used with care when it is used for data storage or temporary work locations to protect it from being overwritten due to stacking from an interrupt or subroutine call.
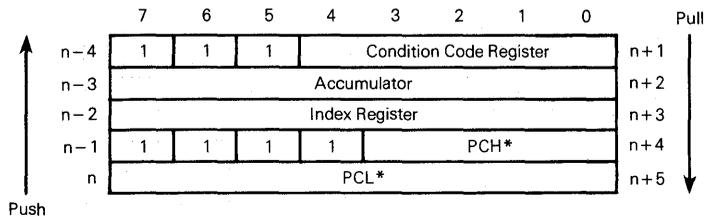
*For subroutine calls, only PCH and PCL are stacked.

Figure 3-7. Interrupt Stacking Order

3.8 CENTRAL PROCESSING UNIT

The central processing unit for the M6805 Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal address, data, and control buses.

SECTION 4
PROGRAMMABLE REGISTERS

The M6805 Family CPU has five registers available to the programmer. They are shown in Figure 4-1 and are explained in the following paragraphs.
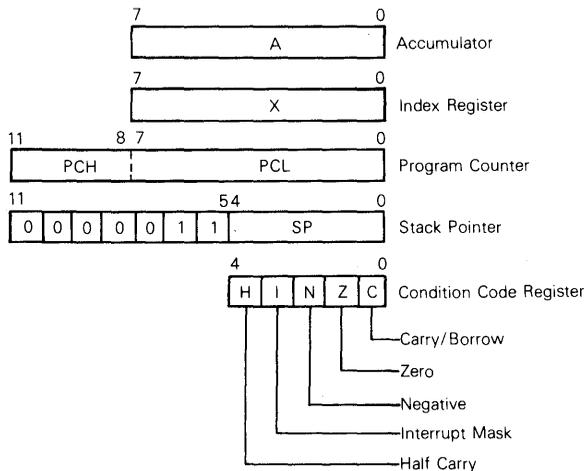
Figure 4-1. Programming Model

4.1 ACCUMULATOR (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

4.2 INDEX REGISTER (X)

The index register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit value that may be added to an 8- or 16-bit immediate value to create an effective address. The index register may also be used as a temporary storage area.

4.3 PROGRAM COUNTER (PC)

The program counter is a 12-bit register that contains the address of the next bye to be fetched.

4.4 STACK POINTER (SP)

The stack pointer is a 12-bit register that contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $07F. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack. The seven most significant bits of the stack pointer are permanently set to 0000011. Subroutines and interrupts may be nested down to location $061 (31 bytes maximum) which allows the programmer to use up to 15 levels of subroutine calls (less if interrupts are allowed).

4.5 CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each bit is explained in the following paragraphs.

4.5.1 Half Carry (H)

Set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

4.5.2 Interrupt (I)

When this bit is set, the timer and external interrupts ($\overline{INT}$ and $\overline{INT2}$) are masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and is processed as soon as the interrupt bit is cleared.

4.5.3 Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logic one).

4.5.4 Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

4.5.5 Carry/Borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions plus shifts and rotates.

SECTION 5
TIMER

The following paragraphs describe the timer circuitry for the eight versions of the M6805 Family found in this document. Note that while each timer consists of an 8-bit software programmable counter driven by a 7-bit prescaler there are three distinctly different configurations (Figures 5-1, 5-2, and 5-3).

5.1 MC6805R2/MC6805U2 TIMER CIRCUITRY

The timer circuitry for the MC6805R2 and MC6805U2 microcomputers is shown in Figure 5-1. The 8-bit counter may be loaded under program control and is decremented toward zero by the clock input (or prescaler output). When the timer reaches zero, the timer interrupt request bit (bit 7) in the timer control register (TCR) is set. The timer interrupt can be masked (disabled) by setting the timer interrupt mask bit (bit 6) in the TCR. The interrupt bit (I bit) in the condition code register also prevents a timer interrupt from being processed. The MCU responds to this interrupt by saving the present CPU state on the stack, fetching the timer interrupt vector from locations $FF8 and $FF9 and executing the interrupt routine (see **SECTION 7 RESET, CLOCK, AND INTERRUPT STRUC-TURE**). *The timer interrupt request bit must be cleared by software.* The TIMER and $\overline{INT2}$ share the same interrupt vector. *The interrupt routine must check the request bits to determine the source of the interrupt.*

The clock input to the timer can be from an external source (decrementing of timer counter occurs on a positive transition of the external source) applied to the TIMER input pin, or it can be the internal phase two signal. Three machine cycles are required for a change in state of the TIMER pin to
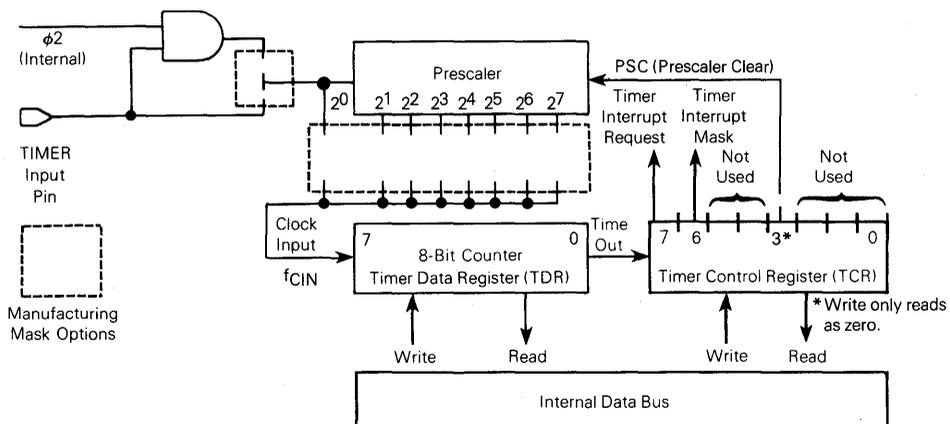
Figure 5-1. MC6805R2/MC6805U2 Timer Block Diagram

decrement the timer prescaler. The maximum frequency of a signal that can be recognized by the TIMER pin logic is dependent on the parameter labeled t_{WL}, t_{WH}. The pin logic that recognizes the high state on the pin must also recognize the low state on the pin in order to "re-arm" the internal logic. Therefore, the period can be calculated as follows (assumes 50/50 duty cycle for a given period):

$$t_{cyc} \times 2 + 250 \text{ ns} = \text{period} = \frac{1}{\text{freq}}$$

The period is not simply $t_{WL} + t_{WH}$. This computation is allowable, but it does reduce the maximum allowable frequency by defining an unnecessarily longer period (250 nanoseconds times two).

When the phase two signal is used as the source, it can be gated by an input applied to the TIMER input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one of the mask options that is specified before manufacture of the MCU.

NOTE

For ungated phase two clock input to the timer prescaler, the TIMER pin should be tied to V_{CC}.

A prescaler option, divide by 2^n, can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before decrementing the counter. This prescaling mask option is also specified before manufacture. To avoid truncation errors, the prescaler is cleared when bit 3 of the timer control register is written to a logic one (this bit always reads a logic zero).

The timer continues to count past zero, falling through to $FF from $00 and then continuing the countdown. Thus, the counter can be read at any time by reading the timer data register (TDR). This allows a program to determine the length of time since a timer interrupt has occurred, and not disturb the counting process.

At power up or reset, the prescaler and counter are initialized with all logic ones; the timer interrupt request bit (bit 7) is cleared and the timer interrupt mask bit (bit 6) is set.

5.2 MC6805R3/MC6805U3 TIMER CIRCUITRY

The timer circuitry for the MC6805R3/MC6805U3 microcomputers is shown in Figure 5-2. The timer contains a single 8-bit software programmable counter with 7-bit software selectable prescaler. The counter may be preset under program control and decrements toward zero. When the counter decrements to zero, the timer interrupt request bit, i.e., bit 7 of the timer control register (TCR), is set. Then if the timer interrupt is not masked, i.e., bit 6 of the TCR and the I bit in the condition code register are both cleared, the processor receives an interrupt. After completion of the current instruction, the processor proceeds to store the appropriate registers on the stack, and then fetches the timer interrupt vector from locations $FF8 and $FF9 in order to begin servicing the interrupt.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter become stable prior to the read portion of a cycle and do not change during the read. The timer interrupt request bit remains set until cleared by the software. If a write occurs before the timer interrupt is serviced, the interrupt is lost. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR = 1).
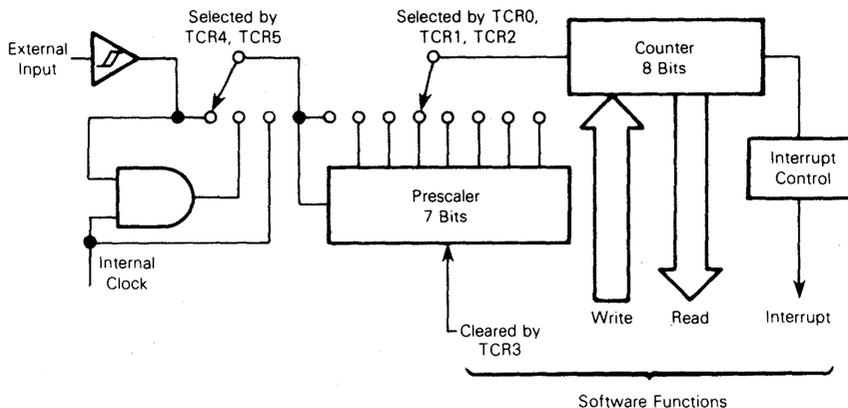
NOTES:
1. The prescaler and 8-bit counter are clocked on the rising edge of the internal clock (phase two) or external input.
2. The counter is written to during data strobe (DS) and counts down continuously.

Figure 5-2. MC6805R3/MC6805U3 Timer Block Diagram

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output which is used as the counter input. The processor cannot write into or read from the prescaler; however, its contents are cleared to all zeros by the write operation into TCR when bit 3 of the written data equals one, which allows for truncation-free counting.

The timer input can be configured for three different operating modes, plus a disable mode, depending on the value written to the TCR4 and TCR5 control bits. Refer to **5.2.5 Timer Control Register (TCR)** for further information.

5.2.1 Timer Input Mode 1

If TCR5 and TCR4 are both programmed to a zero, the input to the timer is from an internal clock and the external TIMER input is disabled. The internal clock mode can be used for periodic interrupt generation, as well as a reference in frequency and event measurement. The internal clock is the instruction cycle clock.

5.2.2 Timer Input Mode 2

With TCR5 = 0 and TCR4 = 1, the internal clock and the TIMER input pin are ANDed to form the timer input signal. This mode can be used to measure external pulse widths. The external timer input pulse simply turns on the internal clock for the duration of the pulse widths.

5.2.3 Timer Input Mode 3

If TCR5 = 1 and TCR4 = 0, then all inputs to the timer are disabled.

5.2.4 Timer Input Mode 4

If TCR5 = 1 and TCR4 = 1, the internal clock input to the timer is disabled and the TIMER input pin

5-3

becomes the input to the timer. The external TIMER pin can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts.

5.2.5 Timer Control Register (TCR)

TCR7	TCR6	TCR5	TCR4	TCR3*	TCR2	TCR1	TCR0	$009

*Write only (read as zero)

TCR7 — Timer interrupt request bit: indicates the timer interrupt when it is a logic one.
    1 — Set whenever the counter decrements to zero, or under program control.
    0 — Cleared on external reset, power-on reset, or program control (write).

TCR6 — Timer interrupt mask bit: inhibits the timer interrupt to the processor, when this bit is a logic one.
    1 — Set on external reset, power-on reset, or program control.
    0 — Cleared under program control.

TCR5 — External or internal bit: selects the input clock source to be either the external TIMER pin or the internal clock (unaffected by $\overline{RESET}$).
    1 — Select external clock source. Set to a logic one on external reset, power-on reset, or program control.
    0 — Select internal clock source (phase two). Cleared under program control.

TCR4 — External enable bit: control bit used to enable the external TIMER pin (unaffected by $\overline{RESET}$).
    1 — Enable external TIMER pin. Set on external reset, power-on reset, or program control.
    0 — Disable external TIMER pin. Cleared under program control.

TCR5	TCR4	
0	0	Internal clock to timer
1	1	AND of internal clock and TIMER pin to timer
1	0	Input to timer disabled
1	1	TIMER pin to timer

TCR3 — Timer prescaler reset bit: writing a one to this bit resets the prescaler to zero. A read of this location always indicates a zero (unaffected by $\overline{RESET}$).

TCR2, TCR1, and TCR0 — Prescaler address bits: decoded to select one of eight outputs of the prescaler (set to all ones by $\overline{RESET}$).

PRESCALER

TCR2	TCR1	TCR0	Result	TCR2	TCR1	TCR0	Result
0	0	0	÷ 1	1	0	0	÷ 16
0	0	1	÷ 2	1	0	1	÷ 32
0	1	0	÷ 4	1	1	0	÷ 64
0	1	1	÷ 8	1	1	1	÷ 128

5.3 MC68705R3/MC68705U3 AND MC68705R5/MC68705U5 TIMER CIRCUITRY

The timer for the MC68705R3 and MC68705U3 microcomputers is shown in Figure 5-3 and the timer for the MC68705R5 and MC68705U5 microcomputers is shown in Figure 5-4. The timer for all four devices contains an 8-bit software programmable counter which is driven by a 7-bit prescaler with one-of-eight selectable outputs. Various timer clock sources may be selected ahead of the prescaler and counter. The timer selections are made via the timer control register (TCR) and/or the mask option register (MOR). The TCR also contains the interrupt control bits. Note that the MC68705R5 and MC68705U5 offer a secure/non-secure mode option which is implemented through bit 3 of the mask option register (refer to **SECTION 9 MASK OPTIONS AND PROGRAMMING** for further information regarding the secure/non-secure mode option).

The 8-bit counter may be loaded under program control and is decremented toward zero by the counter input frequency (f_{CIN}) input (output of the prescaler selector). Once the 8-bit counter has decremented to zero, it sets the TIR (timer interrupt request) bit 7 (b7 of TCR). The TIM (timer interrupt mask) bit (b6) can be software set to inhibit the interrupt request, or software cleared to pass the interrupt request to the processor. When the I bit in the condition code register is cleared, the processor receives the timer interrupt. The MCU responds to this interrupt by saving the present CPU state on the stack, fetching the timer interrupt vector from locations $FF8 and $FF9, and executing the interrupt routine. The processor is sensitive to the level of the timer interrupt request line; therefore if the interrupt is masked, the TIR bit may be cleared by software (e.g., BCLR) without generating an interrupt. The TIR bit *must* be cleared by the timer interrupt service routine to clear the timer interrupt request.

The timer interrupt and $\overline{INT2}$ share the same interrupt vector. The interrupt routine thus must check the two request bits to determine the source of the interrupt.

The counter continues to count (decrement) by falling through to $FF from zero. Thus, the counter can be read at any time by the processor without disturbing the count. This allows a program to determine the length of time since the occurrence of a timer interrupt and does not disturb the counting process.

The clock input to the timer can be from an external source (decrementing the counter occurs on a positive transition of the external source) applied to the TIMER input pin, or it can be the internal phase two signal. The maximum frequency of a signal that can be recognized by the TIMER or $\overline{INT}$ pin logic is dependent on the parameter labeled t_{WL}, t_{WH}. The pin logic that recognizes the low (or high) state on the pin in order to "re-arm" the internal logic. Therefore, the period can be calculated as follows (assumes 50/50 duty cycle for a given period):

$$t_{cyc} \times 2 + 250 \text{ ns} = \text{period} = \frac{1}{\text{freq}}$$

The period is not simply $t_{WL} + t_{WH}$. This computation is allowable, but it does reduce the maximum allowable frequency by defining an unnecessarily longer period (250 nanoseconds twice).

When the phase two signal is used as the source, it can be gated by an input applied to the TIMER pin allowing the user to easily perform pulse width measurements. The source of the clock input is selected via the TCR or the MOR as described later.
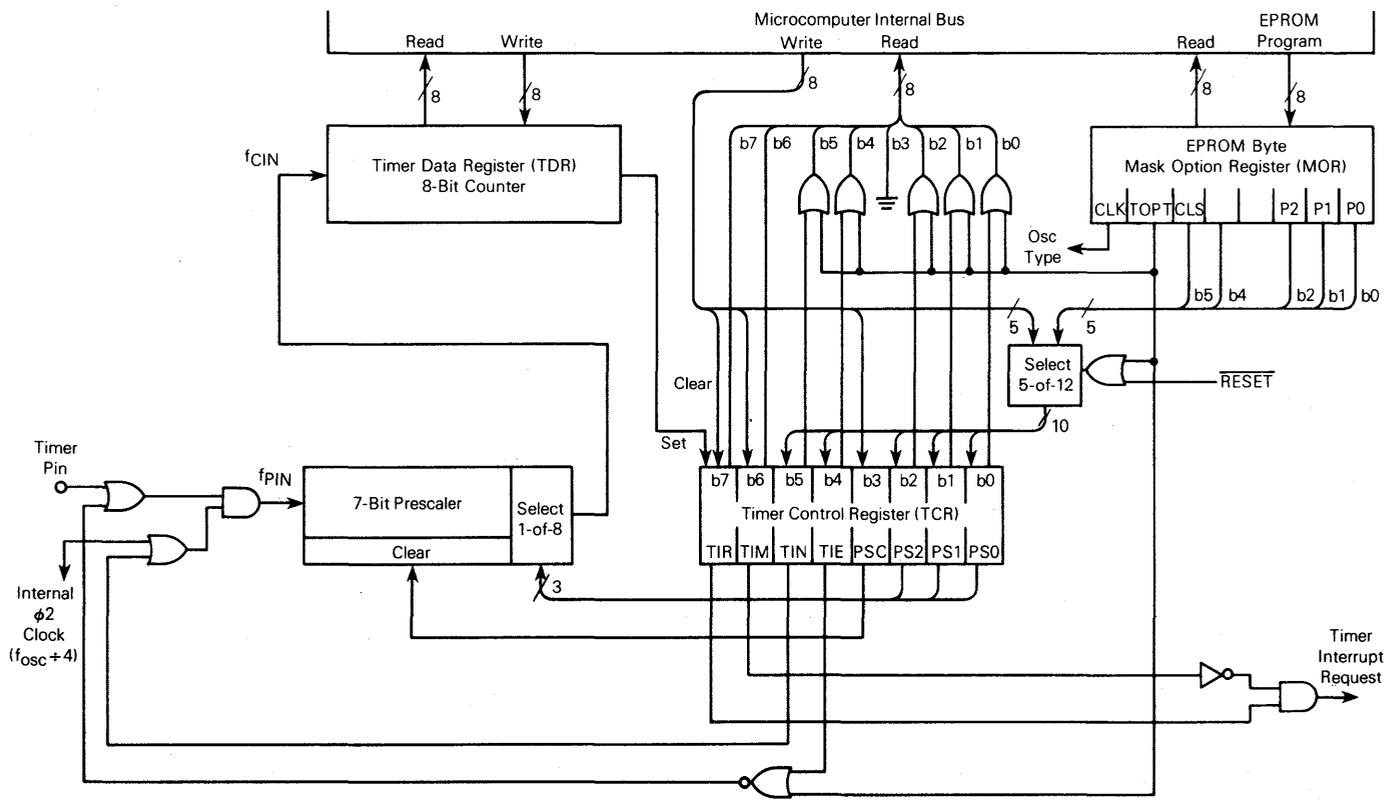
Figure 5-3. MC68705R3/MC68705U3 Timer Block Diagram

f_{PIN} — Prescaler Input Frequency
f_{CIN} — Counter Input Frequency

Timer Control Register Bits:
TIR — Timer Interrupt Request Status
TIM — Timer Interrupt Mask
TIN — Timer Input Select
TIE — Timer External Input Enable
PSC — Prescaler Clear
PS2, PS1, PS0 — Prescaler Select

Mask Option Register Bits:
CLK — Clock Oscillator Type
TOPT — Timer Mask/Programmable Option
CLS — Timer Clock Source
P2, P1, P0 — Prescaler Option

NOTE: The TOPT bit in the mask option register selects whether the timer is software programmable via the timer control register or emulates the mask programmable parts via the MOR EPROM byte.

Microcomputer Internal Bus

EPROM Program

Read Write   Write Read   Read

f_{CIN}

Timer Data Register (TDR) 8-Bit Counter

b7 b6 b5 b4 b3 b2 b1 b0

EPROM Byte Mask Option Register (MOR)

CLK TOPT CLS (TIE) SNM P2 P1 P0

Osc Type

b5 b4 b3 b2 b1 b0

Clear

Select 5-of-12

RESET

Set

10

Timer Pin

f_{PIN}

7-Bit Prescaler

Select 1-of-8

Clear

b7 b6 b5 b4 b3 b2 b1 b0

Timer Control Register (TCR)

TIR TIM TIN TIE PSC PS2 PS1 PS0

Internal $\phi 2$ Clock $(f_{OSC} \div 4)$

3

Timer Interrupt Request

f_{PIN} — Prescaler Input Frequency
f_{CIN} — Counter Input Frequency

Timer Control Register Bits:
  TIR — Timer Interrupt Request Status
  TIM — Timer Interrupt Mask
  TIN — Timer Input Select
  TIE — Timer External Input Enable
  PSC — Prescaler Clear
  PS2, PS1, PS0 — Prescaler Select

Mask Option Register Bits:
  CLK — Clock Oscillator Type
  TOPT — Timer Mask/Programmable Option
  CLS — Timer Clock Source
  (TIE) — (Timer External Input Enable)
  SNM — Secure/Non-Secure Mode Option
  P2, P1, P0 — Prescaler Option

NOTES: The TOPT bit in the mask option register selects whether the timer is software programmable via the timer control register or emulates the mask programmable parts via the MOR PROM byte.

The TIE bit in the mask option register is not used if MOR TOPT = 1 (MC6805P2 emulation). It sets the intial value of TCR TIE if MOR TOPT = 0.

Figure 5-4. MC68705R5/MC68705U5 Timer Block Diagram

A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before decrementing the counter. This prescaling TCR or MOR option selects one of eight outputs on the 7-bit binary divider; one output bypasses prescaling. To avoid truncation errors, the prescaler is cleared when bit 3 (b3) of the TCR is written to a logic one; however, TCR bit 3 always reads as a logic zero to ensure proper operation with read-modify-write instructions (bit set and clear for example).

At reset, the prescaler and counter are initialized to an all ones condition; the timer interupt request bit (TCR, b7) is cleared and the timer interrupt request mask (TCR, b6) is set. TCR bits b0, b1, b2, b4, and b5 are initialized by the corresponding mask option register (MOR) bits at reset. They are then software selectable after reset (if the TOPT bit (b6) in the MORE is equal to zero).

Note that the timer block diagrams in Figures 5-3 and 5-4 reflect two separate timer control configurations: a) software controlled mode via the timer control register (TCR), and b) MOR controlled mode to emulate a mask ROM version with the mask option register. In the software controlled mode, all TCR bits are read/write, except bit b3 which is write-only (always reads as a logic zero). In the MOR controlled mode, for all four devices, TCR bit b7 and b6 are read/write and bits b5, b4, b2, b1, and b0 have no effect on a write (always read as logic ones). For the MC68705R3/MC68705U3, bit b3 is write-only (reads as logic zero), and for the MC68705R5/MC68705U5, bit b3 has no effect on a write (reads as a logic one).

5.3.1 Software Controlled Mode

The TOPT (timer option) bit (b6) in the mask option register is EPROM programmed to a logic zero to select the software controlled mode, which is described first. TCR bits b5, b4, b3, b2, b1, and b0 give the program direct control of the prescaler and input select options.

The timer prescaler input frequency (f_{PIN}) can be configured for three different operating modes plus a disable mode, depending upon the value written to TCR control bits b4 and b5 (TIE and TIN).

When the TIE and TIN bits are programmed to zero the timer input is from the internal clock (phase two) and TIMER input pin is disabled. The internal clock mode can be used for periodic interrupt generation as well as a reference for frequency and event measurement.

When TIE = 1 and TIN = 0, the internal clock and the TIMER input pin signals are ANDed to form the timer input. This mode can be used to measure external pulse widths. The external pulse simply gates in the internal clock for the duration of the pulse. The accuracy of the count in this mode is plus or minus one count.

When TIE = 0 and TIN = 1, no prescaler input frequency is applied to the prescaler and the timer is disabled.

When TIE and TIN are both programmed to a one, the timer is from the external clock. The external clock can be used to count external events as well as provide an external frequency for generating periodic interrupts.

Bits b0, b1, and b2 in the TCR are program controlled to choose the appropriate prescaler output. The prescaling divides the prescaler input frequency by 1, 2, 4, etc. in binary multiplex to 128 producing counter input frequency to the counter. The processor cannot write into or read from the

prescaler; however, the prescaler is set to all ones by a write operation to TCR, b3 (when bit 3 of the written data equals one), which allows for truncation-free counting.

5.3.2 MOR Controlled Mode

The MOR controlled mode of the timer is selected when the TOPT (timer option) bit (b6) in the MOR is programmed to a logic one to emulate the MC6805R2 mask-programmable prescaler and timer clock source. The timer circuits are the same as described above, however, the timer control register (TCR) is configured differently, as discussed below.

The logic level for the functions of bits b0, b1, b2, and b5 in the TCR are all determined at the time of EPROM programming. They are controlled by corresponding bits within the mask option register (MOR, $F38). The value programmed into MOR bits b0, b1, b2, and b5 controls the prescaler division and the timer clock selection. Bit b4 (TIE) is set to a logic one in the MOR controlled mode (when read by software, these five TCR bits always read as logic ones). As in the software programmable configuration, the TIM (b6) and TIR (b7) bits of the TCR are controlled by the counter and software as described above. Bit b3 of the TCR (in the MOR controlled mode) for the MC68705R3/MC68705U3 always reads as a logic zero and can be written to a logic one to clear the prescaler; however, for the MC68705R5/MC68705U5 bit b3 is set to a logic one and when read by software always reads as a logic one. The MOR controlled mode is designed to exactly emulate the MC6805R2 which has only TIM, TIR, and PSC in the TCR and has the prescaler options defined as manufacturing mask options.

5.3.3 Timer Control Register (TCR)

The configuration of the TCR is determined by the logic level of bit 6 (timer option, TOPT) in the mask option register (MOR). Two configurations of the TCR are shown below, one for TOPT = 1 and the other for TOPT = 0. TOPT = 1 configures the TCR to emulate the MC6805R2. When TOPT = 0, it provides software control of the TCR. When TOPT = 1, the prescaler "mask" options are user programmable via the MOR. A description of each TCR bit is provided below (also see Figures 5-3 and 5-4).

<div align="center">TCR with MOR TOPT = 1 (MC6805R2 Emulation)</div>

b7	b6	b5	b4	b3	b2	b1	b0	Timer Control
TIR	TIM	1	1	PSC*	1	1	1	Register $009

*For the MC68705R3/MC68705U3 write only, reads as a zero—for the MC68705R5/MC68705U5 reads as a one and has no effect on the prescaler.

<div align="center">TCR with MOR TOPT = 0 (Software Programmable Timer)</div>

b7	b6	b5	b4	b3	b2	b1	b0	Timer Control
TIR	TIM	TIN	TIE	PSC*	PS2	PS1	PS0	Register $009

*Write only, reads as a zero.

b7, TIR   Timer Interrupt Request — Used to initiate the timer interrupt or signal a timer data register underflow when it is a logic one.
        1 = Set when the timer data register changes to all zeros.
        0 = Cleared by external reset or under program control

b6, TIM Timer Interrupt Mask — Used to inhibit the timer interrupt to the processor when it is a logic one.
1 = Set by an external reset or under program control.
0 = Cleared under program control.

b5, TIN External or Internal — Selects the input clock source to be either the external TIMER (pin 8) or the internal phase two.
1 = Selects the external clock source.
0 = Selects the internal phase two ($f_{OSC} \div 4$) clock source.

b4, TIE External Enable — Used to enable the external TIMER (pin 8) or to enable the internal clock (if TIN = 0) regardless of the external TIMER pin state (disables gated clock feature). When TOPT = 1, TIE is always a logic one.
1 = Enables external TIMER pin.
0 = Disables external TIMER pin.

TIN-TIE MODES

TIN	TIE	CLOCK
0	0	Internal Clock (phase two)
0	1	Gated (AND) of External and Internal Clocks
1	0	No Clock
1	1	External Clock

b3, PSC Prescaler Clear — When TOPT = 0, this is a write-only bit. It reads as a logic zero so the BSET and BCLR on the TCR function correctly. Writing a one into PSC generates a pulse which clears the prescaler. When TOPT = 1, operation remains the same for the MC68705R3/MC68705U3; however, for the MC68705R5/MC68705U5 this bit is always read as a logic one and has no effect on the prescaler.

b2, PS2 Prescaler Select — These bits are decoded to select one of eight outputs on the timer pre-
b1, PS1 scaler division resulting from decoding these bits.
b0, PS0

PS2	PS1	PS0	Prescaler Division
0	0	0	1 (Bypass Prescaler)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

NOTE

When changing the PS2-PS0 bits in software, the PSC bit should be written to a one in the same write cycle to clear the prescaler. Changing the PS bits without clearing the prescaler may cause an extraneous toggle of the timer data register.

SECTION 6
SELF-CHECK

The self-check capability of the MC6805R2, MC6805U2, MC6805R3, and MC6805U3 microcomputers provides an internal check to determine if the part is functional. Connect the MCU as shown in Figure 6-1 and monitor the output of port C bit 3 for an oscillation of approximately 7 hertz. A 10-volt level (through a 10k resistor) on the timer input, pin 8, and pressing then releasing the RESET button, energizes the ROM-based self-check feature. The self-check program exercises the RAM, ROM, TIMER, interrupts, and I/O ports, as well as the A/D for the MC6805R2 and MC6805R3.

Several of the self-check subroutines can be called by a user program with a JSR or BSR instruction. They are the RAM, ROM, and four-channel A/D tests. The timer routine may also be called if the timer input is the internal phase two clock.

6.1 RAM SELF-CHECK SUBROUTINE

The RAM self-check is called at location $F6F for the MC6805R2/MC6805U2 and at location $F84 for the MC6805R3/MC6805U3. If any error is detected, it returns with the Z bit cleared; otherwise the Z bit is set. The walking diagnostic pattern method is used on the MC6805R2/U2. The MC6805R3/U3 test causes each byte to count from 0 up to 0 again with a check after each count.

The RAM test must be called with the stack pointer at $07F. When run, the test checks every RAM cell except for $07F and $07E which are assumed to contain the return address.

The A and X registers and all RAM locations except $07F and $07E are modified.

6.2 ROM CHECKSUM SUBROUTINE

The ROM self-check is called at location $F8A for the MC6805R2/MC6805U2 and at location $F95 for the MC6805R3/MC6805U3.

The A register should be cleared before calling the routine in the MC6805R3/MC6805U3. If any error is detected, it returns with the Z bit cleared; otherwise Z = 1, X = 0 on return, and A is zero if the test passes. RAM location $040 is overwritten.

6.3 ANALOG-TO-DIGITAL CONVERTER SELF-CHECK

The analog-to-digital self-check for the MC6805R2 is called at location $FA4 and for the MC6805R3 at $FAE. For both devices, it returns with the Z bit cleared if any error was found; otherwise the Z bit is set.
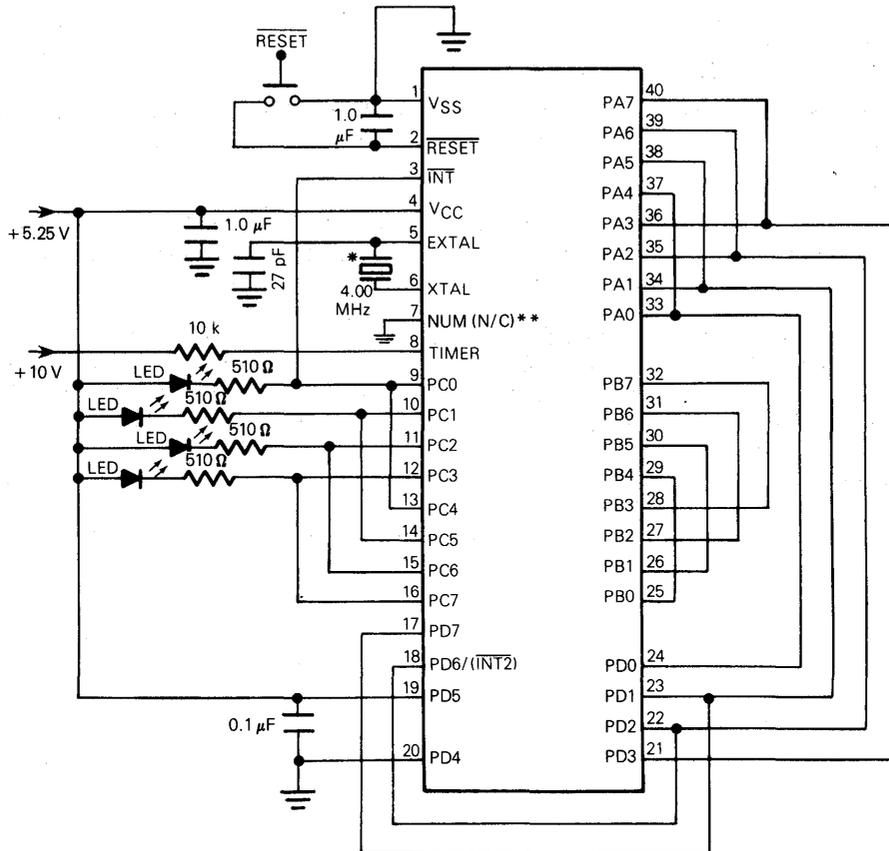
* This connection depends on clock oscillator user selectable mask option. Use jumper if the RC mask option is selected.

** For the MC6805R2/MC6805U2 pin 7 is not for user application and must be connected to V_{SS}. For the MC6805R3/MC6805U3 pin 7 is not connected.

LED Meanings

PC0	PC1	PC2	PC3	Remarks [1:LED ON; 0:LED OFF]
1	0	1	0	Bad I/O
0	0	1	0	Bad Timer
1	1	0	0	Bad RAM
0	1	0	0	Bad ROM
1	0	0	0	Bad A/D
0	0	0	0	Bad Interrupts or Request Flag
All Flashing				Good Device

Anything else bad Part, Bad Port C, etc.

Figure 6-1. Self-Check Connections

The A and X register contents are lost. The X register must be set to four before the call. On return, X = 8 and A/D channel 7 is selected. The A/D test uses the internal voltage references and confirms port connections.

6.4 TIMER SELF-CHECK SUBROUTINE

The timer self-check is called at location $FCF for the MC6805R2/MC6805U2 and at location $F6D for the MC6805R3/MC6805U3. If any error was found, it returns with the Z bit cleared; otherwise the Z bit is set.

In order to work correctly as a user subroutine, the internal phase two clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock is running and the interrupt mask is not set so the caller must protect from interrupts if necessary.

The A and X register contents are lost. The timer self-check routine in the MC6805R2/U2 counts how many times the clock counts in 128 cycles. The number of counts should be a power of two since the prescaler is a power of two. If not, the timer probably is not counting correctly. The routine also detects a timer which is not running. In the MC6805R3/U3, this routine sets the prescaler for divide-by-128 and the timer data register is cleared. The X register is configured to count down the same as the timer data register. The two registers are then compared every 128 cycles until they both count down to zero. Any mismatch during the count down is considered an error. In the MC6805R3/U3, the A and X registers are cleared on exit from the routine.

SECTION 7
RESET, CLOCK, AND INTERRUPT STRUCTURE

7.1 RESET

The MCU can be reset three ways: by initial powerup, by the external reset input ($\overline{\text{RESET}}$) and by an optional internal low-voltage detect circuit (not available on the MC68705U3 or MC68705R3 EPROM versions). The $\overline{\text{RESET}}$ input consists mainly of a Schmitt trigger which senses the $\overline{\text{RESET}}$ line logic level. A typical reset Schmitt trigger hysteresis curve is shown in Figure 7-1. The Schmitt trigger provides an internal reset voltage if it senses a logical zero on the $\overline{\text{RESET}}$ pin.
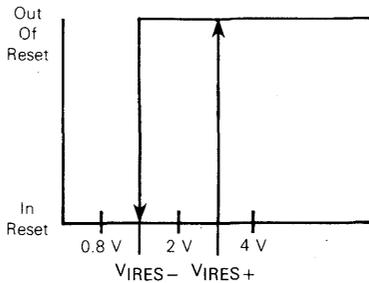
Figure 7-1. Typical Reset Schmitt Trigger Hysteresis

7.1.1 Power-On Reset (POR)

An internal reset is generated upon powerup that allows the internal clock generator to stabilize. A delay of t_{RHL} milliseconds is required before allowing the $\overline{\text{RESET}}$ input to go high. Refer to the power and reset timing diagram of Figure 7-2. Connecting a capacitor to the $\overline{\text{RESET}}$ input (as illustrated in Figure 7-3) typically provides sufficient delay. During powerup, the Schmitt trigger switches on (removes reset) when $\overline{\text{RESET}}$ rises to V_{IRES+}.
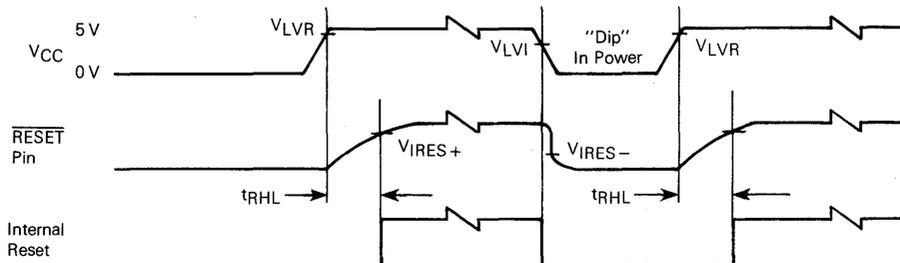
Figure 7-2. Power and Reset Timing
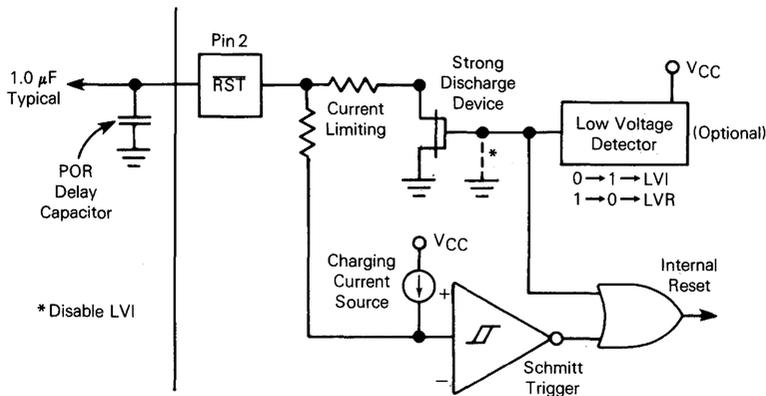
Figure 7-3. RESET Configuration

7.1.2 External Reset Input

The MCU will be reset if a logical zero is applied to the RESET input for a period longer than one machine cycle (t_{cyc}). Under this type of reset, the Schmitt trigger switches off at $V_{IRES} -$ to provide an internal reset voltage.

7.1.3 Low-Voltage Inhibit (LVI)

The optional low-voltage detection circuit (not available on the MC68705R3, MC68705R5, MC68705U3, and MC68705U5) causes a reset of the MCU if the power supply voltage falls below a certain level (V_{LVI}). The only requirement is that V_{CC} remains at or below the V_{LVI} threshold for one t_{cyc} minimum. In typical applications, the V_{CC} bus filter capacitor will eliminate negative-going voltage glitches of less than one t_{cyc}. The output from the low-voltage detector is connected directly to the internal reset circuitry. It also forces the RESET pin low via a strong discharge device through a resistor. The internal reset will be removed once the power supply voltage rises above a recovery level (V_{LVR}), at which time a normal power-on-reset occurs.

7.2 INTERNAL CLOCK GENERATOR OPTIONS

The internal clock generator circuit is designed to require a minimum of external components. A crystal, a resistor, a jumper wire, or an external signal may be used to generate a system clock with various stability/cost tradeoffs. The mask option register (EPROM) is programmed to select crystal or resistor operation. The oscillator frequency is internally divided by four to produce the internal system clocks. For MC6805R2, MC6805U2, MC6805R3, and MC6805U3 a manufacturing mask option is used to select crystal or resistor operation.

The different connection methods are shown in Figure 7-4. Crystal specifications and suggested PC board layouts are given in Figure 7-5. A resistor selection graph is given in Figure 7-6.

The crystal oscillator start-up time is a function of many variables: crystal parameters (especially R_S), oscillator load capacitances, IC parameters, ambient temperature, and supply voltage. To ensure rapid oscillator start up, neither the crystal characteristics nor the load capacitances should exceed recommendations.

XTAL 6

EXTAL 5
(See Note 2)

C_L

MCU
(Crystal Option,
See Note 1)

Crystal

XTAL 6

EXTAL 5

MCU
(RC Option,
See Note 1)

Approximately 25% to 50% Accuracy
Typical $t_{cyc} = 1.25\ \mu s$
External Jumper

XTAL 6

External
Clock
Input

EXTAL 5

MCU
(Crystal Option,
See Note 1)

External Clock

V_{CC}

R
(See Figure 7-5)

No
Connection

XTAL 6

EXTAL 5

MCU
(RC Option,
See Note 1)

Approximately 10% to 25% Accuracy
(Excludes Resistor Tolerance)
External Resistor

NOTES:
1. For the MC68705R3, MC68705U3, MC68705R5, and MC68705U5 MOR b7 = 0 for the crystal option and MOR b7 = 1 for the RC option. When the TIMER input pin is in the V_{IHTP} range (in the bootstrap EPROM programming mode), the crystal option is forced. When the TIMER input is at or below V_{CC}, the clock generator option is determined by bit 7 of the Mask Option Register (CLK).
2. The recommended C_L value with a 4.0 MHz crystal is 27 pF maximum, including system distributed capacitance. There is an internal capacitance of approximately 25 pF on the XTAL pin. For crystal frequencies other than 4 MHz, the total capacitance on each pin should be scaled as the inverse of the frequency ratio. For example, with a 2 MHz crystal, use approximately 50 pF on EXTAL and approximately 25 pF on XTAL. The exact value depends on the Motional-Arm parameters of the crystal used.

Figure 7-4. Clock Generator Options

When utilizing the on-board oscillator, the MCU should remain in a reset condition (reset pin voltage below V_{IRES+}) until the oscillator has stabilized at its operating frequency. Several factors are involved in calculating the external reset capacitor required to satisfy this condition: the oscillator start-up voltage, the oscillator stabilization time, the minimum V_{IRES+}, and the reset charging current specification.

Once V_{CC} minimum is reached, the external $\overline{RESET}$ capacitor will begin to charge at a rate dependent on the capacitor value. The charging current is supplied from V_{CC} through a large resistor, so it appears almost like a constant current source until the reset voltage rises above V_{IRES+}. Therefore, the $\overline{RESET}$ pin will charge at approximately:

$$(V_{IRES+}) \bullet C_{ext} = I_{RES} \bullet t_{RHL}$$

Assuming the external capacitor is initially discharged.

(a)
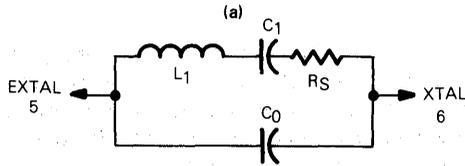
AT — Cut Parallel Resonance Crystal
$C_O = 7$ pF Max
Freq. = 4.0 MHz @ $C_L = 24$ pF
$R_S = 50$ ohms Max.

Piezoelectric ceramic resonators which
have the equivalent specifications may be
used instead of crystal oscillators. Follow
ceramic resonator manufacturer's sug-
gestions for C_0, C_1, and R_S values.

(b)

(c)
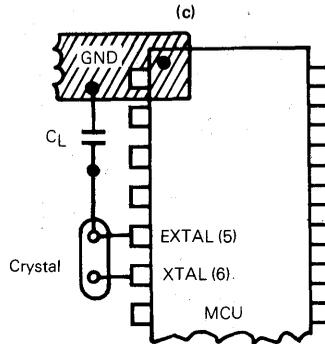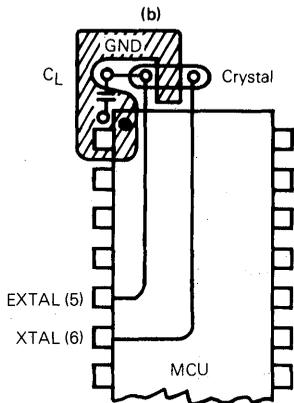
NOTE: Keep crystal leads and circuit connections as short as possible.

**Figure 7-5. Crystal Motional-Arm Parameters
and Suggested PC Board Layout**

$V_{CC} = 5.25$ V
$T_A = 25°C$
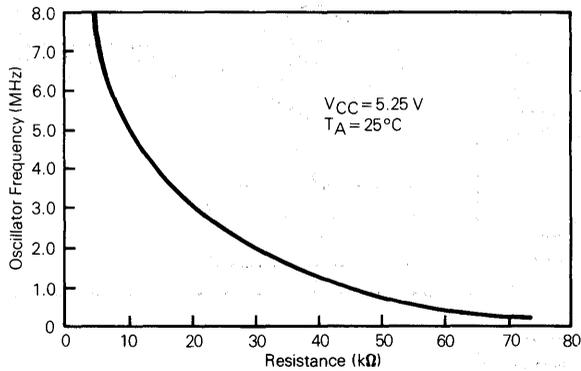
**Figure 7-6. Typical Frequency Selection for
Resistor (RC Oscillator Option)**

7.3 INTERRUPTS

The microcomputers can be interrupted four different ways: through the external interrupt ($\overline{\text{INT}}$) input pin, the internal timer interrupt request, the external port D bit 6 ($\overline{\text{INT2}}$) input pin, or the software interrupt instruction (SWI). When any interrupt occurs: the current instruction (including SWI) is completed, processing is suspended, the present CPU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. Stacking the CPU register, setting the I bit, and vector fetching require a total of 11 t_{cyc} periods for completion. A flowchart of the interrupt sequence is shown in Figure 7-7. The interrupt service routine must end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the
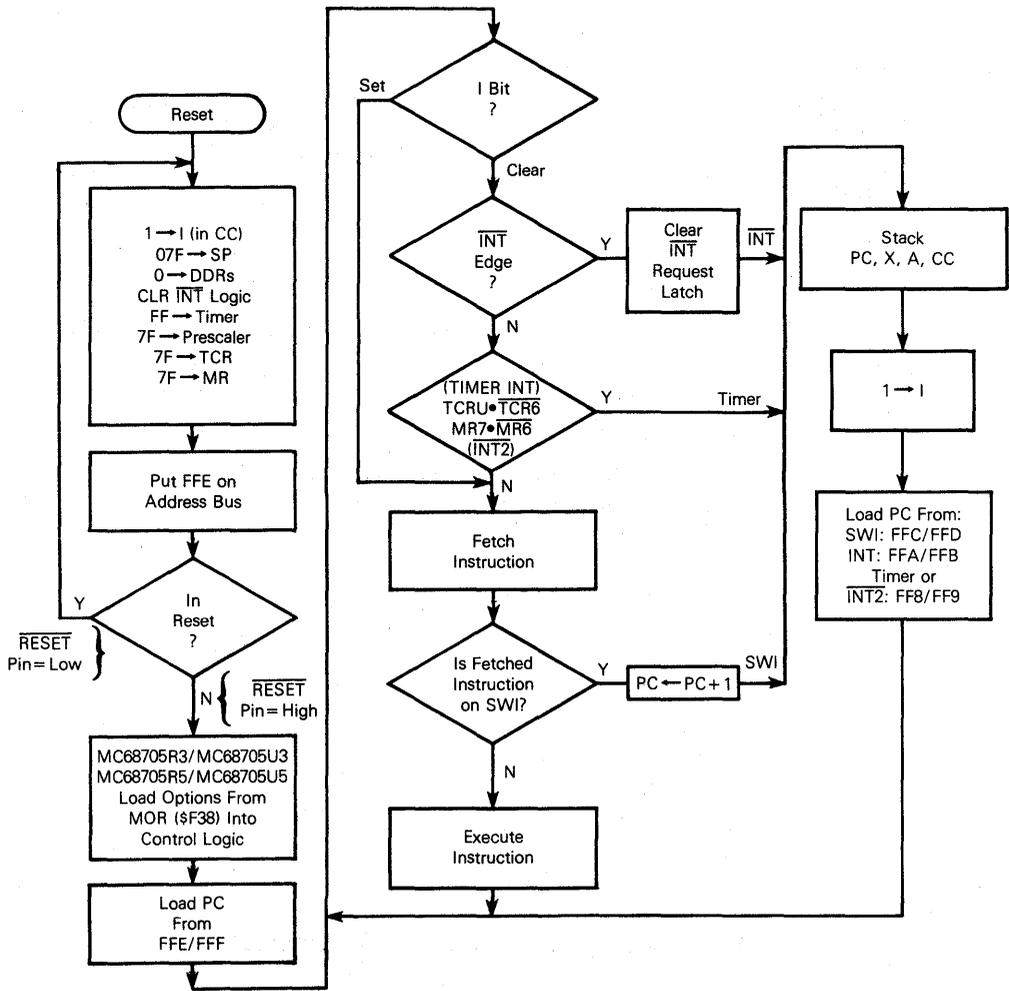
Figure 7-7. Reset and Interrupt Processing Flowchart

program prior to the interrupt (by unstacking the previous CPU state). Unlike $\overline{RESET}$, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction execution is complete.

When the current instruction is complete, the processor checks all pending hardware interrupts and if unmasked, proceeds with interrupt processing; otherwise the next instruction is fetched and executed. Note that masked interrupts are latched for later interrupt service.

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed as any other instruction.

NOTE

The timer and $\overline{INT2}$ interrupts share the same vector address. The interrupt routine must determine the source by examining the interrupt request bits (TCR b7 and MR b7). Both TCR b7 and MR b7 can only be written to zero by software.

The external interrupt, $\overline{INT}$ and $\overline{INT2}$, are synchronized and then latched on the falling edge of the input signal. The $\overline{INT2}$ interrupt has an interrupt request bit (bit 7) and a mask bit (bit 6) located in the miscellaneous register (MR). The $\overline{INT2}$ interrupt is inhibited when the mask bit is set. The $\overline{INT2}$ is always read as a digital input on port D. The $\overline{INT2}$ and timer interrupt request bits, if set, cause the MCU to process an interrupt when the condition code I bit is clear.

A sinusoidal input signal (f_{INT} maximum) can be used to generate an external interrupt for use as a zero-crossing detector. This allows applications such as servicing time-of-day routines and engaging/disengaging ac power control devices. Off-chip full wave rectification provides an interrupt at every zero crossing of the ac signal and thereby provides a 2f clock. See Figure 7-8.

A software interrupt (SWI) is an executable instruction which is executed regardless of the state of the I bit in the condition code register. SWIs are usually used as breakpoints for debugging or as system calls.

(a) Zero-Crossing Interrupt

(b) Digital-Signal Interrupt
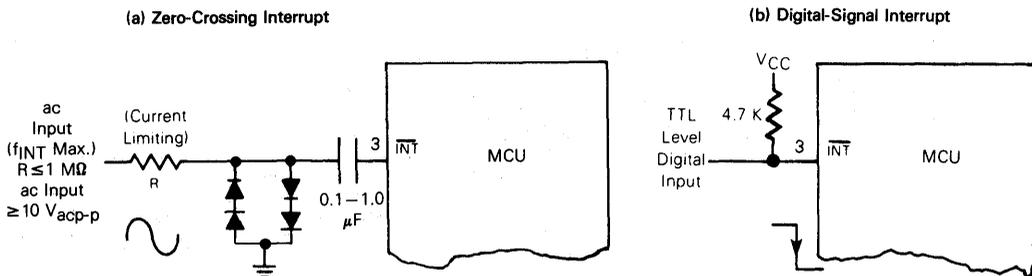
Figure 7-8. Typical Interrupt Circuits

SECTION 8
INPUT/OUTPUT CIRCUITRY AND
ANALOG-TO-DIGITAL CONVERTER

8.1 INPUT/OUTPUT CIRCUITRY

There are 32 input/output pins. The $\overline{INT}$ pin may be polled with branch instructions to provide an additional input pin. All pins on ports A, B, and C are programmable as either inputs or outputs under software control of the corresponding data direction register (DDR). The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic one for output or a logic zero for input. On reset all the DDRs are initialized to a logic zero state, placing the ports in the input mode. The port output registers are not initialized on reset and should be initialized by software before changing the DDRs from input to output. A read operation on a port programmed as an output will read the contents of the output latch regardless of the logic levels at the output pin, due to output loading. Refer to Figure 8-1.

Data Direction Register Bit	Latched Output Data Bit	Output State	Input To MCU
1	0	0	0
1	1	1	1
0	X	Hi-Z**	Pin
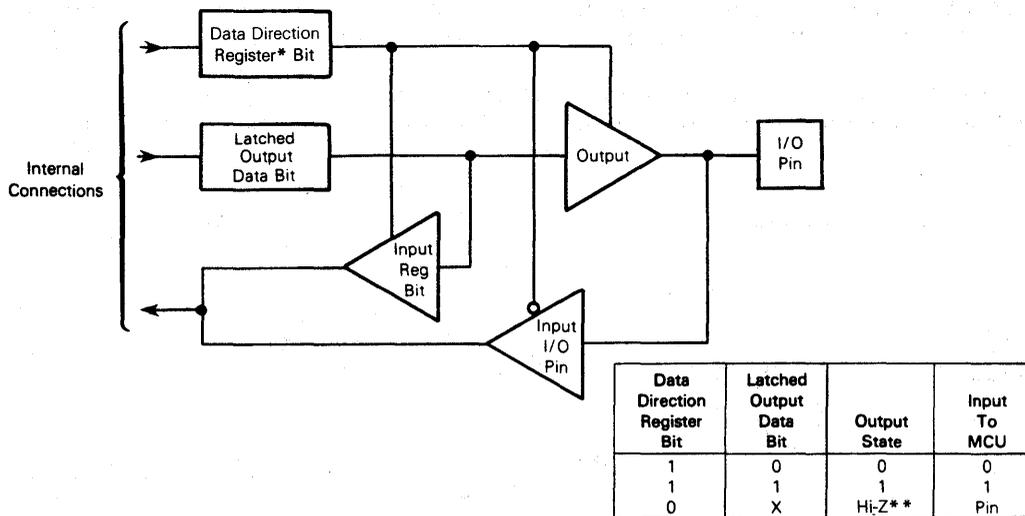
*DDR is a write-only register and reads as all ones.
**Port B and C are three-state ports. Port A has optional internal pullup devices to provide CMOS data drive capability.
See **SECTION 11 ELECTRICAL CHARACTERISTICS.**

Figure 8-1. Typical Port I/O Circuitry

All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs (mask option on the MC6805R2, MC6805U2, MC6805R3, and MC6805U3) while port B, C, and D lines are CMOS compatible as inputs. Port D lines are input only; thus, there is no corresponding DDR. When programmed as outputs, port b is capable of sinking 10 milliamperes and sourcing 1 milliampere on each pin.

Port D provides the reference voltage, $\overline{INT2}$, and multiplexed analog inputs for the MC6805R2, MC6805R3, MC68705R3, and MC68705R5. All of these lines are shared with the port D digital inputs. Port D may always be used as digital inputs and may also be used as analog inputs providing V_{RH} and V_{RL} are connected to the appropriate reference voltages. The V_{RL} and V_{RH} lines (PD4 and PD5) are internally connected to the A/D resistor. Analog inputs may be prescaled to attain the V_{RL} and V_{RH} recommended input voltage range.

The address maps in Section 3 give the addresses of data registers and data direction registers. The register configuration is provided in Figure 7-6. Figure 8-2 provides some examples of port connections.

CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at $004, $005, and $006). A read operation on these registers is undefined. Since BSET and BCLR are read-modfiy-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port be written using a single-store instruction.
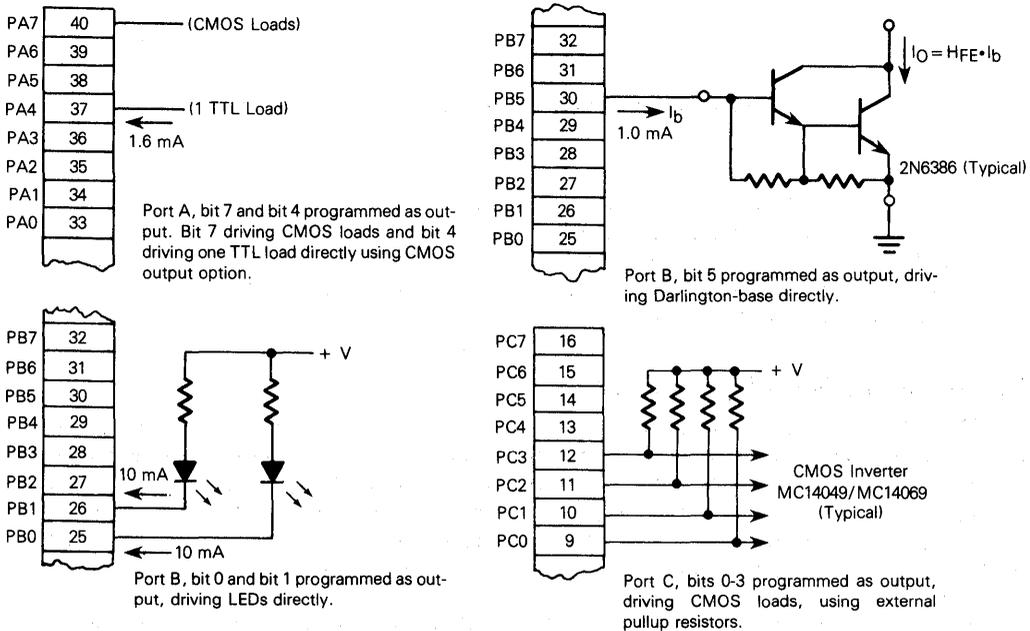
Figure 8-2a. Typical Port Connections—Output Modes

SN74LS04 (Typical)

40	PA7
39	PA6
38	PA5
37	PA4
36	PA3
35	PA2
34	PA1
33	PA0

TTL driving port A directly.

SN74LS04 or MC14069 (Typical)

32	PB7
31	PB6
30	PB5
29	PB4
28	PB3
27	PB2
26	PB1
25	PB0

CMOS or TTL driving port B directly.

MC14069 (Typical)

16	PC7
15	PC6
14	PC5
13	PC4
12	PC3
11	PC2
10	PC1
9	PC0

SN74LS04 (Typical)

CMOS and TTL driving port C directly.

AN0→	24	PD0/AN0
AN1→	23	PD1/AN1
AN2→	22	PD2/AN2
AN3→	21	PD3/AN3
0 V—	20	V_{RL}
+5 V—	19	V_{RH}
	18	PD6/$\overline{INT2}$
	17	PD7

MC14069

Port D used as 4-channel A/D input with bit 7 used as CMOS digital input. MC6805R2, MC6805R3, MC6805R3, and MC68705R5 only.

Figure 8-2b. Typical Port Connections—Input Modes

The latched output data bit (see Figure 8-1) must always be written. Therefore, any write to a port writes all of its data bits even though the port DDR is set to input. This may be used to initialize the data register and avoid undefined outputs; however, care must be exercised when using read-modify-write instructions, since the data read corresponds to the pin level if the DDR is an input (zero) and corresponds to the latched output data when the DDR is an output (one).

8.2 ANALOG-TO-DIGITAL CONVERTER

The MC6805R2, MC6805R3, MC68705R3 and MC68705R5 microcomputers have an 8-bit analog-to-digital (A/D) converter implemented on the chip using a successive approximation technique, as shown in Figure 8-3. Up to four external analog inputs, via port D, are connected to the A/D through a multiplexer. Four internal analog channels may be selected for calibration purposes (V_{RH}-V_{RL}, V_{RH}-V_{RL}/2, V_{RH}-V_{RL}/4, and V_{RL}). The accuracy of these internal channels will not necessarily meet the accuracy specifications of the external channels.

The multiplexer selection is controlled by the A/D control register (ACR) bits 0, 1, and 2; see Table 8-1. This register is cleared during any reset condition. Refer to Figure 7-6 for the register configuration.
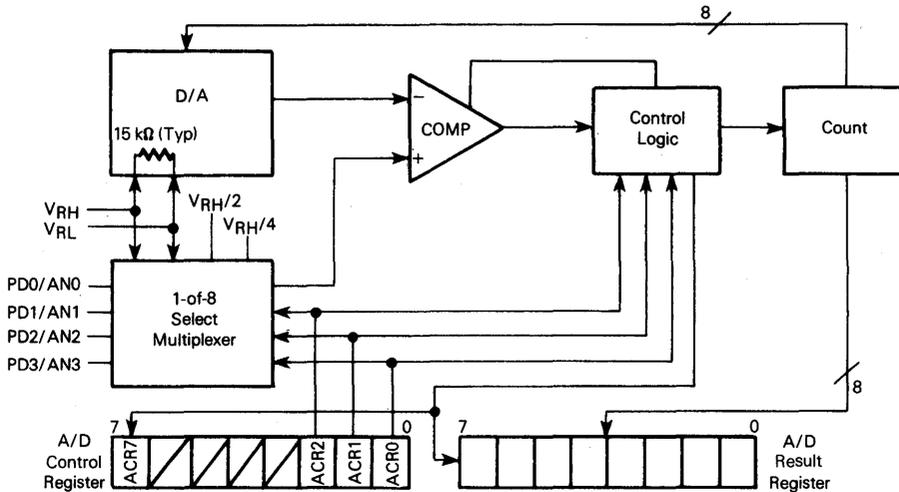
Figure 8-3. A/D Block Diagram

Table 8-1. A/D Input MUX Selection

A/D Control Register			Input Selected	A/D Output (Hex)		
ACR2	ACR1	ACR0		Min	Typ	Max
0	0	0	AN0			
0	0	1	AN1			
0	1	0	AN2			
0	1	1	AN3			
1	0	0	V_{RH}*	FE	FF	FF
1	0	1	V_{RL}*	00	00	01
1	1	0	$V_{RH}/4$*	3F	40	41
1	1	1	$V_{RH}/2$*	7F	80	81

*Internal (Calibration) Levels

Whenever the ACR is written, the conversion in progress is aborted, the conversion complete flag (ACR bit 7) is cleared, and the selected input is sampled for five machine cycles and held internally. During these five cycles, the analog input will appear approximately like a 25 picofarad (maximum) capacitor (plus approximately 10 pF for packaging) charging through a 2.6 kilohm resistor (typical). Refer to Figure 8-4.

The converter operates continuously using 30 machine cycles to complete a conversion of the sampled analog input. When the conversion is complete, the digitized sample of digital value is placed in the A/D result register (ARR), the conversion complete flag is set, the selected input is sampled again, and a new conversion is started.

The A/D is ratiometric. Two reference voltages (V_{RH} and V_{RL}) are supplied to the converter via port D pins. An input voltage equal to V_{RH} converts to $FF (full scale) and an input voltage equal to V_{RL} converts to $00. An input voltage greater than V_{RH} converts to $FF and no overflow indication is provided. Similarly, an input voltage less than V_{RL}, but greater than V_{SS} converts to $00. Maximum and minimum ratings must not be exceeded. For ratiometric conversion, the source of each analog input should use V_{RH} as the supply voltage and be referenced to V_{RL}. To maintain the full
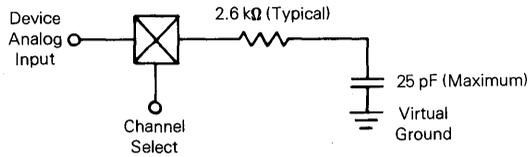
Figure 8-4. Effective Analog Input Inpedance (During Sampling Only)

accuracy on the A/D, V_{RH} should be equal to or less than V_{DD}, V_{RL} should be equal to or greater than V_{SS} but less than the maximum specification and (V_{RH}-V_{RL}) should be equal to or greater than 4 volts.

The A/D has a built-in ½ LSB offset intended to reduce the magnitude of the quantizing error to ± ½ LSB, rather than +0, −1 LSB with no offset. This implies that, ignoring errors, the transition point from $00 to $01 occurs at ½ LSB above V_{RL}. Similarly, the transition from $FE to $FF occurs 1½ LSB below V_{RH}, ideally. Refer to Figures 8-5 and 8-6.

On release of reset, the A/D control register (ACR) is cleared therefore after reset, channel zero will be selected and the conversion complete flag will be clear.
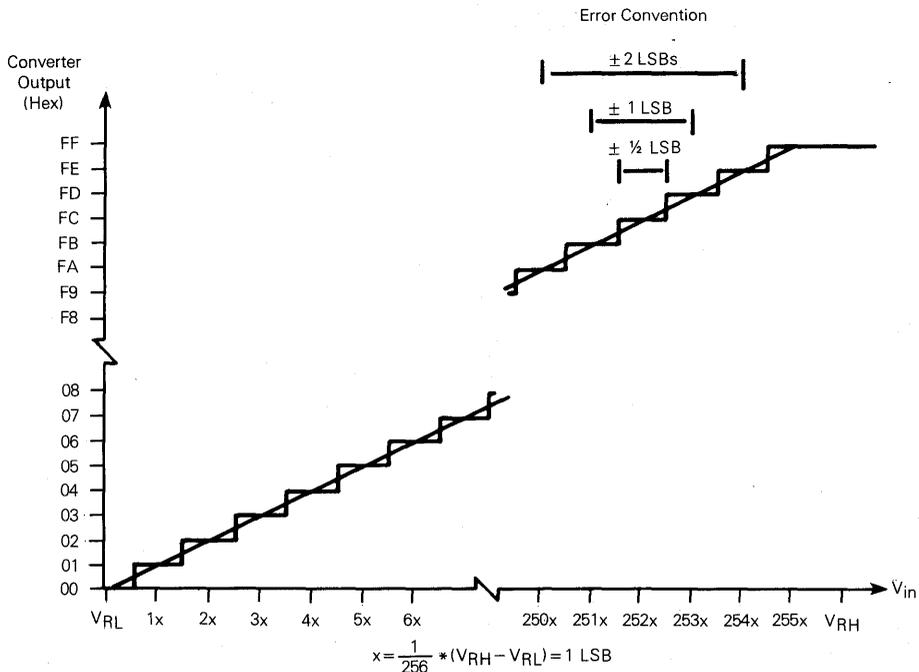
Figure 8-5. Ideal Converter Transfer Characteristic

(a) Offset Error

(b) Full Scale Error

(c) Non-Linearity
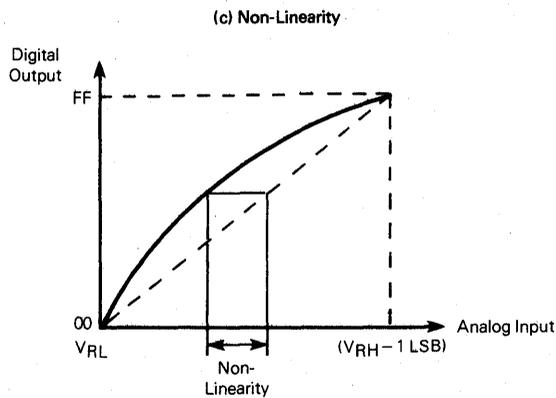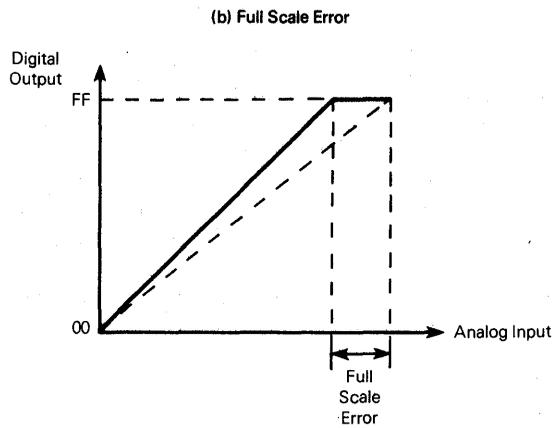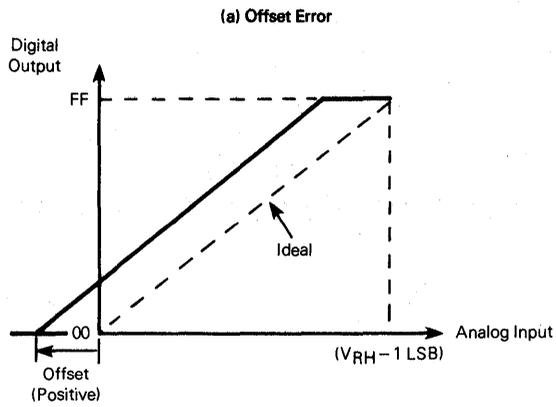
Figure 8-6. Types of Conversion Errors

SECTION 9
MASK OPTIONS AND PROGRAMMING

The information in this section pertains only to the MC68705R3, MC68705U3, MC68705R5, and MC68705U5 EPROM versions of the M6805 Family.

9.1 MASK OPTIONS

The MC68705R3, MC68705U3, MC68705R5, and MC68705U5 mask option registers are implemented in EPROM. Like all other EPROM bytes, the MOR contains all zeros prior to programming (if erased).

When used to emulate the MC6805R2 and MC6805U2, five of the eight MOR bits are used in conjunction with the prescaler. Of the remaining, the b7 bit is used to select the type of clock oscillator, b3 is the secure/non-secure mode option for the MC68705R5/MC68705U5 only (b3 is not used by the MC68705R3/MC68705U3), and b4 is not used. Bits b0, b1, and b2 determine the division of the timer prescaler. Bit b6 determines the timer option selection. The value of the TOPT bit (b6) is programmed to configure the TCR (a logic one for MC6805R2/MC6805U2 emulation).

If the MOR timer option (TOPT) bit is a zero, the MC6805R3 and MC6805U3 are emulated. Here, bits b5, b4, b2, b1, and b0 set the initial value of their respective TCR bits during reset. After initialization the TCR is software controllable.

A description of the MOR bits is as follows:

b7	b6	b5	b4	b3	b2	b1	b0	Mask Option
CLK	TOPT	CLS		SNM*	P2	P1	P0	Register $F38

*MC68705R5 and MC68705U5 only.

b7, CLK   Clock Oscillator Type
            1 = RC
            0 = Crystal

NOTE

V_{IHTP} on the TIMER (pin 8) forces the crystal mode.

b6, TOPT   Timer Option
            1 = MC6805R2/MC6805U2 type timer/prescaler. All bits, except b6 and b7, of the timer control register (TCR) are invisible to the user. Bits b5, b2, b1, and b0 of the mask option register determine the equivalent MC6805R2/MC6805U2 mask options.
            0 = MC6805R3/MC6805U3 type timer/prescaler. All TCR bits are implemented as a software programmable timer. The state of bits b5, b4, b2, b1, and b0 set the initial values of their respective TCR bits (TCR is then software controlled after initialization).

b5, CLS　Timer/Prescaler Clock Source
1 = External TIMER pin.
0 = Intenal phase two.

b4　　　　Not used if MOR TOPT = 1 (MC6805R2/MC6805U2 emulation). Sets initial value of TCR TIE if MOR TOPT = 0 (MC6805R3/MC6805U3 emulation).

b3, SNM*　When this bit is set, i.e., programmed to a one, it is not possible to access the EPROM contents of the MC68705R5 and MC68705U5 externally. For more information refer to **9.4 PROGRAMMING FIRMWARE.**

Note, For MC68705R3 and MC68705U3 operation, b3 is not used.

b2, P2　Prescaler Option — the logic levels of these bits, when decoded, select one of eight out-
b1, P1　puts on the timer prescaler. The table below shows the division resulting from decoding
b0, P0　combinations of these three bits.

P2	P1	P0	Prescaler Division
0	0	0	1 (Bypass Prescaler)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Two examples for programming the mask option register are discussed below.

Example 1
　　To emulate an MC6805R2/MC6805U2 to verify your program with an RC oscillator and an event count input for the timer with no prescaling, the mask option register would be set to 11110000. To write the mask option register, it is simply programmed as any other EPROM byte.

Example 2
　　Suppose you wish to use programmable prescaler functions (MC6805R3/MC6805U3 emula-tion), and you wish the initial condition of the prescaler to be divided by 64, with the input dis-abled and an internal clock source. If the clock oscillator was to be in the crystal mode, the mask option register would be set to 00000110.

9.2 ON-CHIP PROGRAMMING HARDWARE

The programming control register (PCR) at location $00B is an 8-bit register which utilizes the three least significant bits (the five most significant bits are set to logic ones). This register provides the

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*MC68705R5 and MC68705U5 only.

necessary control bits to allow programming the EPROM. The bootstrap program manipulates the PCR when programming so that users need not be concerned with the PCR in most applications. A description of each bit follows.

b7	b6	b5	b4	b3	b2	b1	b0	Programming
1	1	1	1	1	$\overline{VPON}$	$\overline{PGE}$	$\overline{PLE}$	Control

Register $00B

b0, $\overline{PLE}$ Programming Latch Enable — When cleared, this bit allows the address and data to be latched into the EPROM. When this bit is set, data can be read from the EPROM.
  1 = (set) read EPROM
  0 = (clear) latch address and data into EPROM (read disable)
  PLE is set during a reset, but may be cleared any time. However, its effect on the EPROM is inhibited if $\overline{VPON}$ is a logic one.

b1, $\overline{PGE}$ Program Enable — When cleared, $\overline{PGE}$ enables programming of the EPROM. $\overline{PGE}$ can only be cleared if $\overline{PLE}$ is cleared. $\overline{PGE}$ must be set when changing the address and data; i.e., setting up the byte to be programmed.
  1 = (set) inhibit EPROM programming
  0 = (clear) enable EPROM programming (if $\overline{PLE}$ is low)
  $\overline{PGE}$ is set during a reset; however, it has no effect on EPROM circuits if $\overline{VPON}$ is a logic one.

b2, $\overline{VPON}$ (VPP ON) — $\overline{VPON}$ is a read-only bit and when at a logic zero it indicates that a "high voltage" is present at the VPP pin.
  1 = no "high voltage" on VPP pin
  0 = "high voltage" on VPP pin
  $\overline{VPON}$ being one "disconnects" $\overline{PGE}$ and $\overline{PLE}$ from the rest of the chip, preventing accidental clearing of these bits from affecting the normal operating mode.

NOTE
$\overline{VPON}$ being zero does not indicate that the VPP level is correct for programming. It is used as a safety interlock for the user in the normal operating mode.

The programming control register functions are shown below.

$\overline{VPON}$	$\overline{PGE}$	$\overline{PLE}$	Programming Conditions
0	0	0	Programming mode (program EPROM byte)
1	0	0	$\overline{PGE}$ and $\overline{PLE}$ disabled from system
0	1	0	Programming disabled (latch address and data in EPROM)
1	1	0	$\overline{PGE}$ and $\overline{PLE}$ disabled from system
0	0	1	Invalid state; $\overline{PGE}$ = 0 iff $\overline{PLE}$ = 0
1	0	1	Invalid state; $\overline{PGE}$ = 0 iff $\overline{PLE}$ = 0
0	1	1	"High voltage" on VPP
1	1	1	$\overline{PGE}$ and $\overline{PLE}$ disabled from system (operating mode)

9.3 ERASING THE EPROM

The EPROM can be erased by exposure to high-intensity ultraviolet (UV) light with a wavelength of 2537 angstroms. The recommended integrated dose (UV intensity × exposure time) is 25 Ws/cm^2. The lamps should be used without shortwave filters and the EPROM should be positioned about one inch from the UV tubes. Ultraviolet erasure clears all bits of the EPROM to the zero state. Data is the entered by programming ones into the desired bit locations.

CAUTION

Be sure that the EPROM window is shielded from light except when erasing. This protects both the EPROM and light-sensitive nodes.

9.4 PROGRAMMING FIRMWARE

The MC68705R3, MC68705U3, MC68705R5, and MC68705U5 have 120 bytes of mask ROM containing a bootstrap program which can be used to program the EPROM. The vector at addresses $FF6 and $FF7 is used to start executing the program. This vector is fetched when V_{IHTP} is applied to pin 8 (TIMER pin) and the $\overline{RESET}$ pin is allowed to rise above V_{IRES+}. Figure 9-1 provides a schematic diagram of a circuit and a summary of programming steps which can be used to program the EPROM. It is possible to program the EPROM via the bootstrap software and validate its contents in the secure mode. The only way to go from the secure mode to the non-secure mode is by erasing the entire EPROM.

9.5 PROGRAMMING STEPS

The MCM2532 UV EPROM must first be programmed with an exact duplicate of the information that is to be transferred to the MC68705R3, MC68705U3, MC68705R5, or MC68705U5. Non-EPROM addresses are ignored by the bootstrap. Since the MC68705R3, MC68705U3, MC68705R5, or MC68705U5 and the MCM2532 are to be inserted and removed from the circuit, they should be mounted in sockets. In addition, the precaution below must be observed (refer to Figure 9-1).

CAUTION

Be sure S1 and S2 are closed and V_{CC} and +26 V are not applied when inserting the MC68705R3, MC68705U3, MC68705R5, or MC68705U5 and MCM2532 into their respective sockets. This ensures that $\overline{RESET}$ is held low while inserting the devices.

When ready to program the MC68705R3, MC68705U3, MC68705R5, or MC68705U5 it is only necessary to provide V_{CC} and +26 volts, open switch S2 (to apply V_{PP} and V_{IHTP}), and then open S1 (to remove reset). Once the voltages are applied and both S2 and S1 are open, the CLEAR output control line (PB4) goes high and then low, then the 12-bit counter (MC14040B) is clocked by the PB3 output (COUNT). The counter selects the MCM2532 EPROM byte which is to load the equivalent EPROM byte selected by the bootstrap program. Once the EPROM location is loaded, COUNT clocks the counter to the next EPROM location. This continues until the EPROM is completely programmed at which time the programmed indicator LED is lit. The counter is cleared and the loop is repeated to verify the programmed data. The verified indicator LED lights if the programming is correct.

Figure 9-1. Programming Connections Schematic Diagram

$V_{CC} = +5.0 \text{ V (typical)}$
$V_{SS} = 0.0 \text{ V}$
$V_{PP} = 21.0 \text{ V} \pm 1.0 \text{ V (Programming Mode)}$
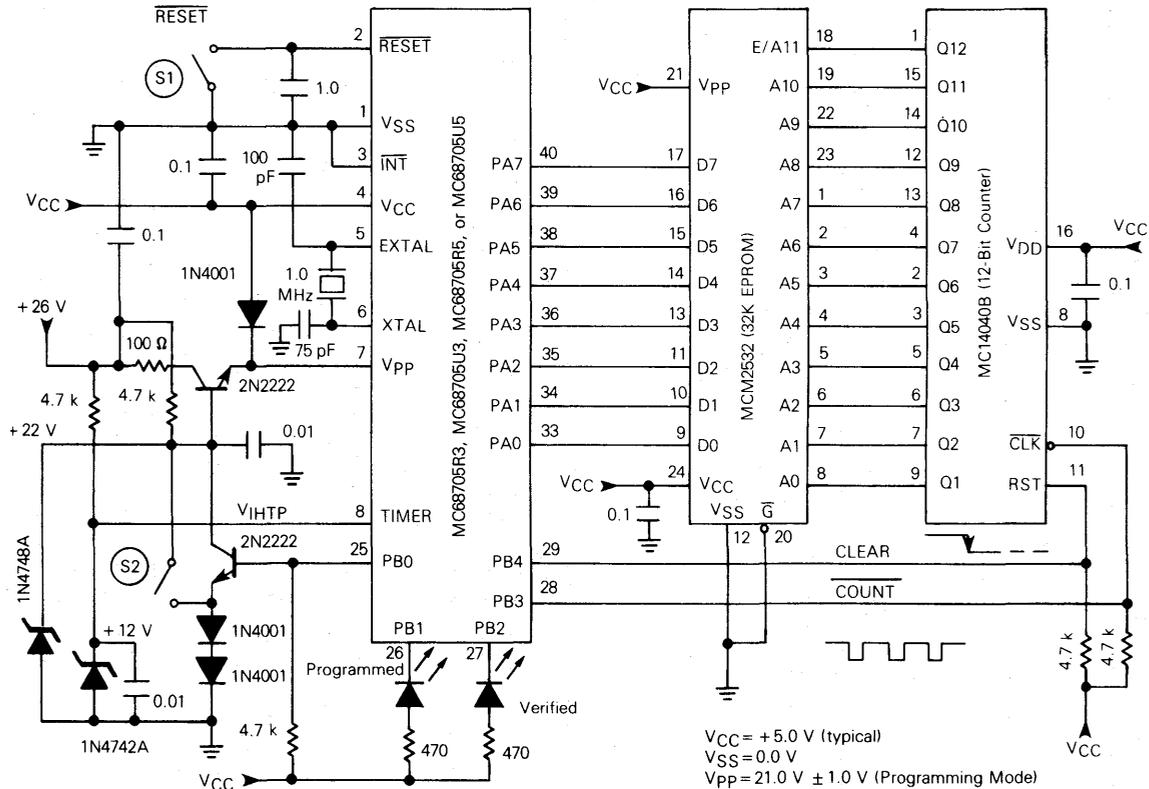
Summary of Programming Steps:
1. When plugging in the MC68705R3, MC68705U3, MC68705R5, or MC68705U5 or the MCM2532 be sure that S1 and S2 are closed and that V_{CC} and +26 V are not applied.
2. To initiate programming, be sure S1 is closed, S2 is closed and V_{CC} and +25 V are applied. Then open S2, followed by S1.
3. Before removing the MC68705R3, MC68705U3, MC68705R5, or MC68705U5, first close S2 and then close S1. Disconnect V_{CC} and +26 V then remove the MC68705R3, MC68705U3, MC68705R5, or MC68705U5.

Once the EPROM has been programmed and verified, close switch S2 (to remove V_{PP} and V_{IHTP}) and close switch S1 (to reset). Disconnect + 26 volts and V_{CC}, then remove the EPROM from its socket.

9.6 EMULATION

The MC68705R3 and MC68705R5 emulate the MC6805R2 and MC6805R3 while the MC68705U3 and MC68705U5 emulate the MC685U2 and MC6805U3 "exactly." MC6805R2, MC6805U2, MC6805R3, and MC6805U3 mask features are implemented in the mask option register (MOR) EPROM byte. There are a few minor exceptions to the exactness of emulation which are listed below.

1. The MC6805R2/MC6805U2 and MC6805R3/MC6805U3 "future ROM" areas are implemented in the MC68705R3/MC68705U3 and MC68705R5/MC68705U5 and these 1728 bytes must be left unprogrammed to accurately simulate the MC6805R2/MC6805U2 and MC6805R3/MC6805U3. (The MC6805R2/MC6805U2 and MC6805R3/MC6805U3 read all zeros from this area.)

2. The reserved ROM areas have different data stored in them and this data is subject to change without notice. The MC6805R2, MC6805U2, MC6805R3, and MC6805U3 use the reserved ROM for the self-check feature while the MC68705R3, MC68705U3, MC68705R5, and MC68705U5 use this area for the bootstrap program.

3. The MC6805R2/MC6805U2 and MC6805R3/MC6805U3 read all ones in their 48 byte "future RAM" area. This RAM is not implemented in the MC6805R2/MC6805U2 and MC6805R3/MC6805U3 mask ROM version, but is implemented in the EPROM version (MC68705R3/MC68705U3 and MC68705R5/MC68705U5).

4. The V_{PP} line (pin 7) in the MC68705R3/MC68705U3 and MC68705R5/MC68705U5 EPROM versions is tied to V_{CC} for normal operation. In the MC6805R2/MC6805U2 and MC6805R3/MC6805U3 mask ROM versions, pin 7 is grounded in normal operation.

5. The LVI feature is not available in the EPROM version.

6. The MC68705R3/MC68705U3 and MC68705R5/MC68705U5 EPROM versions do not function in the MEX6805 Support System. In normal operation, all pin functions are the same as on the MC6805R2/MC6805U2 and MC6805R3/MC6805U3 mask ROM versions, except for pin 7 as previously noted.

The operation of all other circuitry has been exactly duplicated or designed to function exactly the same way in all devices including interrupts, timer, data ports, and data direction registers (DDRs).

SECTION 10
SOFTWARE

10.1 BIT MANIPULATION

The microcomputers have the ability to set or clear any single RAM or I/O bit (except the data direction registers) with a single instruction (BSET, BCLR) (see Caution below). Any bit in page zero can be tested using the BRSET and BRCLR instructions and the program branches as a result of its state. The carry bit equals the value of the bit references by BRSET or BRCLR. The capability of working with any bit in RAM, ROM, or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines.

CAUTION

The corresponding data direction registers for ports A, B, and C are write-only registers (locations $004, $005, and $006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write functions, they cannot be used to set a data direction regiser bit (all "unaffected" bits would be set). It is recommended that all data direction register bits in a port be written using a single-store instruction.

The coding examples shown in Figure 10-1 illustrate the usefulness of the bit manipulation and test instruction. Assume that the microcomputer is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line to clock data one bit at a time, least significant bit first out of the device. The microcomputer waits until the data is ready, clocks the external device, picks up the data in the carry flag, clears the clock line, and finally accumulates the data bit in a random-access memory location.

```
                                                         •
                                                         •
                                                         •
              READY                   SELF   BRSET   2,PORTA,SELF
                     2 P                                 •
   Serial     Clock    O    MCU                          •
   Device            1  R                                •
                       T                     BSET    1,PORTA
              Data   0 A                      BRCLR   0,PORTA,CONT
                                      CONT   BCLR    1,PORTA
                                             ROR     RAMLOC
                                                         •
                                                         •
                                                         •
```
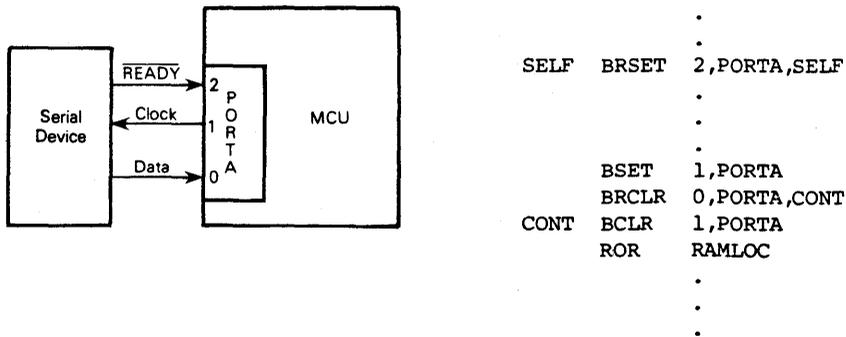
Figure 10-1. Bit Manipulation Examples

10.2 ADDRESSING MODES

The microcomputers have ten addressing modes available for use by the programmer. They are explained briefly in the following paragraphs. For additional details and illustrations, refer to the *M6805 HMOS/M146805 CMOS Family Microcomputer/Microprocessor User's Manual.*

The term "effective address" (EA) is used in describing the addressing modes. EA is defined as the address from which the argument for an instruction is fetched or stored.

10.2.1 Immediate

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

10.2.2 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction. This address area includes all on-chip RAM and I/O registers and 128 bytes of ROM. Direct addressing is an effective use of both memory and time.

10.2.3 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing modes are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the shortest form of the instruction.

10.2.4 Relative

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode is added to the PC if, and only if, the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from -126 to $+129$ from the opcode address. The programmer need not worry about calculating the correct offset if he uses the Motorola assembler, since it calculates the proper offset and checks to see if it is within the span of the branch.

10.2.5 Indexed, No Offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only on byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

10.2.6 Indexed, 8-Bit Offset

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. This addressing mode is

useful in selecting the kth element in an n element table. With this two-byte instruction, k would typically be in X with the address of the beginning of the table in the instruction. As such, tables may begin anywhere within the first 256 addressable locations and could extend as far as location 510 ($1FE is the last location at which the instruction may begin).

10.2.7 Index, 16-Bit Offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended, the Motorola determines the shortest form of indexed addressing.

10.2.8 Bit Set/Clear

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct addressing of the byte in which the specified bit is to be set or cleared. Thus, any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two-byte instruction.

<div align="center">CAUTION</div>

The corresponding DDRs for ports A, B, and C are write-only registers (registers at $004, $005, and $006). A read operation on these registers is undefined since BSET and BCLR are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port must be written using a single-store instruction.

10.2.9 Bit Test and Branch

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit which is to be tested and condition (set or clear) is included in the opcode, and the address of the byte to be tested is in the single byte immediately following the opcode byte. The signed relative 8-bit offset in the third byte is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branching is from -125 to $+130$ from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code registers. See Caution under paragraph 10.2.8.

10.2.10 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as control instruction with no other agruments, are included in this mode. These instructions are one byte long.

10.3 INSTRUCTION SET

The MCU has a set of 59 basic instructions, which when combined with the 10 addressing modes produce 207 usable opcodes. They can be divided into five types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

10.3.1 Register/Memory Instructions

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from meory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 10-1.

10.3.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register (see Caution under paragraph 10.2.8). The test for negative or zero (TST) instructions is included in the read-modify-write instructions, though it does not perform the write. Refer to Table 10-2.

10.3.3 Branch Instructions

The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 10-3.

10.3.4 Bit Manipulation Instructions

These instructions are used on any bit in the first 256 bytes of memory; see Caution under paragraph 10.2.8. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 10-4.

10.3.5 Control Instructions

The control instructions control the MCU operations during program execution. Refer to Table 10-5.

10.3.6 Alphabetical Listing

The complete instruction set is given in alphabetical order in Table 10-6.

10.3.7 Opcode Map Summary

Table 10-7 is an opcode made for the instructions used on the MCU.

Table 10-1. Register Memory Instructions

		Addressing Modes																
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
Load X from Memory	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
Store A in Memory	STA	—	—	—	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
Store X in Memory	STX	—	—	—	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
Add Memory to A	ADD	AB	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
Add Memory and Carry to A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
Subtract Memory	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND Memory to A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR Memory with A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
Jump Unconditional	JMP	—	—	—	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
Jump to Subroutine	JSR	—	—	—	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

Table 10-2. Read-Modify-Write Instructions

Function	Mnemonic	Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
Decrement	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
Clear	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
Complement	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
Negate (2's Complement)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
Rotate Left Thru Carry	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
Rotate Right Thru Carry	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
Logical Shift Left	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
Logical Shift Right	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
Arithmetic Shift Right	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
Test for Negative or Zero	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

Table 10-3. Branch Instructions

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	4
Branch Never	BRN	21	2	4
Branch IFF Higher	BHI	22	2	4
Branch IFF Lower or Same	BLS	23	2	4
Branch IFF Carry Clear	BCC	24	2	4
(Branch IFF Higher or Same)	(BHS)	24	2	4
Branch IFF Carry Set	BCS	25	2	4
(Branch IFF Lower)	(BLO)	25	2	4
Branch IFF Not Equal	BNE	26	2	4
Branch IFF Equal	BEQ	27	2	4
Branch IFF Half Carry Clear	BHCC	28	2	4
Branch IFF Half Carry Set	BHCS	29	2	4
Branch IFF Plus	BPL	2A	2	4
Branch IFF Minus	BMI	2B	2	4
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	4
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	4
Branch IFF Interrupt Line is Low	BIL	2E	2	4
Branch IFF Interrupt Line is High	BIH	2F	2	4
Branch to Subroutine	BSR	AD	2	8

Table 10-4. Bit Manipulation Instructions

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n(n=0. . .7)	—	—	—	$2 \cdot n$	3	10
Branch IFF Bit n is Clear	BRCLR n(n=0. . .7)	—	—	—	$01 + 2 \cdot n$	3	10
Set Bit n	BSET n(n=0. . .7)	$10 + 2 \cdot n$	2	7	—	—	—
Clear Bit n	BCLR n(n=0. . .7)	$11 + 2 \cdot n$	2	7	—	—	—

Table 10-5. Control Instructions

Function	Mnemonic	Inherent Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	11
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2

Table 10-6. Instruction Set (Sheet 1 of 2)

Mnem	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			∧	●	∧	∧	∧
ADD		X	X	X		X	X	X			∧	●	∧	∧	∧
AND		X	X	X		X	X	X			●	●	∧	∧	●
ASL	X		X			X	X				●	●	∧	∧	∧
ASR	X		X			X	X				●	●	∧	∧	∧
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	∧	∧	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●

Condition Code Symbols:
- H   Half Carry (From Bit 3)
- I   Interrupt Mask
- N   Negative (Sign Bit)
- Z   Zero
- C   Carry/Borrow
- ∧   Test and Set if True, Cleared Otherwise
- ●   Not Affected

Table 10-6. Instruction Set (Sheet 2 of 2)

	Addressing Modes										Condition Code				
Mnem	**Inherent**	**Immediate**	**Direct**	**Extended**	**Relative**	**Indexed (No Offset)**	**Indexed (8 Bits)**	**Indexed (16 Bits)**	**Bit Set/Clear**	**Bit Test & Branch**	**H**	**I**	**N**	**Z**	**C**
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	∧
BRSET										X	●	●	●	●	∧
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLL	X										●	●	●	●	O
CLI	X										●	O	●	●	●
CLR	X		X			X	X				●	●	O	1	●
CMP		X	X	X		X	X	X			●	●	∧	∧	∧
COM	X		X			X	X				●	●	∧	∧	1
CPX		X	X	X		X	X	X			●	●	∧	∧	∧
DEC	X		X			X	X				●	●	∧	∧	●
EOR		X	X	X		X	X	X			●	●	∧	∧	●
INC	X		X			X	X				●	●	∧	∧	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	∧	∧	●
LDX		X	X	X		X	X	X			●	●	∧	∧	●
LSL	X		X			X	X				●	●	∧	∧	∧
LSR	X		X			X	X				●	●	O	∧	∧
NEQ			X			X	X				●	●	∧	∧	∧
NOP	X										●	●	●	●	●
ORA	X	X	X	X		x	X	X			●	●	∧	∧	●
ROL	X		X			X	X				●	●	∧	∧	∧
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	∧	∧	∧
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	∧	∧	●
STX			X	X		X	X	X			●	●	∧	∧	●
SUB		X	X	X		X	X	X			●	●	∧	∧	∧
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	∧	∧	●
TXA	X										●	●	●	●	●

Condition Code Symbols:

H	Half Carry (From Bit 3)	C	Carry/Borrow
I	Interrupt Mask	∧	Test and Set if True, Cleared Otherwise
N	Negative (Sign Bit)	●	Not Affected
Z	Zero	?	Load CC Register From Stack

Table 10-7. M6805 HMOS Family Instruction Set Opcode Map

	Bit Manipulation		Branch	Read/Modify/Write				
	BTB	BSC	REL	DIR	A	X	IX1	IX
Hi →	0	1	2	3	4	5	6	7
Low ↓	0000	0001	0010	0011	0100	0101	0110	0111
0 0000	10⌐5 BRSET0 3 BTB	7⌐5 BSET0 2 BSC	4⌐3 BRA 2 REL	6⌐5 NEG 2 DIR	4⌐3 NEG 1 A	4⌐3 NEG 1 X	7⌐6 NEG 2 IX1	6⌐5 NEG 1 IX
1 0001	10⌐5 BRCLR0 3 BTB	7⌐5 BCLR0 2 BSC	4⌐3 BRN 2 REL					
2 0010	10⌐5 BRSET1 3 BTB	7⌐5 BSET1 2 BSC	4⌐3 BHI 2 REL					
3 0011	10⌐5 BRCLR1 3 BTB	7⌐5 BCLR1 2 BSC	4⌐3 BLS 2 REL	6⌐5 COM 2 DIR	4⌐3 COM 1 A	4⌐3 COM 1 X	7⌐6 COM 2 IX1	6⌐5 COM 1 IX
4 0100	10⌐5 BRSET2 3 BTB	7⌐5 BSET2 2 BSC	4⌐3 BCC 2 REL	6⌐5 LSR 2 DIR	4⌐3 LSR 1 A	4⌐3 LSR 1 X	7⌐6 LSR 2 IX1	6⌐5 LSR 1 IX
5 0101	10⌐5 BRCLR2 3 BTB	7⌐5 BCLR2 2 BSC	4⌐3 BCS 2 REL					
6 0110	10⌐5 BRSET3 3 BTB	7⌐5 BSET3 2 BSC	4⌐3 BNE 2 REL	6⌐5 ROR 2 DIR	4⌐3 ROR 1 A	4⌐3 ROR 1 X	7⌐6 ROR 2 IX1	6⌐5 ROR 1 IX
7 0111	10⌐5 BRCLR3 3 BTB	7⌐5 BCLR3 2 BSC	4⌐3 BEQ 2 REL	6⌐5 ASR 2 DIR	4⌐3 ASR 1 A	4⌐3 ASR 1 X	7⌐6 ASR 2 IX1	6⌐5 ASR 1 IX
8 1000	10⌐5 BRSET4 3 BTB	7⌐5 BSET4 2 BSC	4⌐3 BHCC 2 REL	6⌐5 LSL 2 DIR	4⌐3 LSL 1 A	4⌐3 LSL 1 X	7⌐6 LSL 2 IX1	6⌐5 LSL 1 IX
9 1001	10⌐5 BRCLR4 3 BTB	7⌐5 BCLR4 2 BSC	4⌐3 BHCS 2 REL	6⌐5 ROL 2 DIR	4⌐3 ROL 1 A	4⌐3 ROL 1 X	7⌐6 ROL 2 IX1	6⌐5 ROL 1 IX
A 1010	10⌐5 BRSET5 3 BTB	7⌐5 BSET5 2 BSC	4⌐3 BPL 2 REL	6⌐5 DEC 2 DIR	4⌐3 DEC 1 A	4⌐3 DEC 1 X	7⌐6 DEC 2 IX1	6⌐5 DEC 1 IX
B 1011	10⌐5 BRCLR5 3 BTB	7⌐5 BCLR5 2 BSC	4⌐3 BMI 2 REL					
C 1100	10⌐5 BRSET6 3 BTB	7⌐5 BSET6 2 BSC	4⌐3 BMC 2 REL	6⌐5 INC 2 DIR	4⌐3 INC 1 A	4⌐3 INC 1 X	7⌐6 INC 2 IX1	6⌐5 INC 1 IX
D 1101	10⌐5 BRCLR6 3 BTB	7⌐5 BCLR6 2 BSC	4⌐3 BMS 2 REL	6⌐4 TST 2 DIR	4⌐3 TST 1 A	4⌐3 TST 1 X	7⌐5 TST 2 IX1	6⌐4 TST 1 IX
E 1110	10⌐7 BRSET7 3 BTB	7⌐5 BSET7 2 BSC	4⌐3 BIL 2 REL					
F 1111	10⌐7 BRCLR7 3 BTB	7⌐5 BCLR7 2 BSC	4⌐3 BIH 2 REL	6⌐5 CLR 2 DIR	4⌐3 CLR 1 A	4⌐3 CLR 1 X	7⌐6 CLR 2 IX1	6⌐5 CLR 1 IX

Abbreviations for Address Modes

INH	Inherent	EXT	Extended	IX	Indexed (No Offset)
A	Accumulator	REL	Relative	IX1	Indexed, 1 Byte (8-Bit) Offset
X	Index Register	BSC	Bit Set/Clear	IX2	Indexed, 2 Byte (16-Bit) Offset
IMM	Immediate	BTB	Bit Test and Branch	*	M146805 CMOS Family Only
DIR	Direct				

	Control		Register/Memory						
	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	Hi
	8	9	A	B	C	D	E	F	Low
	1000	1001	1010	1011	1100	1101	1110	1111	
0 / 0000	RTI (9/9, 1, INH)		SUB (2/2, 2, IMM)	SUB (4/3, 2, DIR)	SUB (5/4, 3, EXT)	SUB (6/5, 3, IX2)	SUB (5/4, 2, IX1)	SUB (4/3, 1, IX)	
1 / 0001	RTS (6/6, 1, INH)		CMP (2/2, 2, IMM)	CMP (4/3, 2, DIR)	CMP (5/4, 3, EXT)	CMP (6/5, 3, IX2)	CMP (5/4, 2, IX1)	CMP (4/3, 1, IX)	
2 / 0010			SBC (2/2, 2, IMM)	SBC (4/3, 2, DIR)	SBC (5/4, 3, EXT)	SBC (6/5, 3, IX2)	SBC (5/4, 2, IX1)	SBC (4/3, 1, IX)	
3 / 0011	SWI (11/10, 1, INH)		CPX (2/2, 2, IMM)	CPX (4/3, 2, DIR)	CPX (5/4, 3, EXT)	CPX (6/5, 3, IX2)	CPX (5/4, 2, IX1)	CPX (4/3, 1, IX)	
4 / 0100			AND (2/2, 2, IMM)	AND (4/3, 2, DIR)	AND (5/4, 3, EXT)	AND (6/5, 3, IX2)	AND (5/4, 2, IX1)	AND (4/3, 1, IX)	
5 / 0101			BIT (2/2, 2, IMM)	BIT (4/3, 2, DIR)	BIT (5/4, 3, EXT)	BIT (6/5, 3, IX2)	BIT (5/4, 2, IX1)	BIT (4/3, 1, IX)	
6 / 0110			LDA (2/2, 2, IMM)	LDA (4/3, 2, Dir)	LDA (5/4, 3, EXT)	LDA (6/5, 3, IX2)	LDA (5/4, 2, IX1)	LDA (4/3, 1, IX)	
7 / 0111		TAX (2/2, 1, INH)		STA (5/4, 2, DIR)	STA (6/5, 3, EXT)	STA (7/6, 3, IX2)	STA (6/5, 2, IX1)	STA (5/4, 1, IX)	
8 / 1000		CLC (2/2, 1, INH)	EOR (2/2, 2, IMM)	EOR (4/3, 2, DIR)	EOR (5/4, 3, EXT)	EOR (6/5, 3, IX2)	EOR (5/4, 2, IX1)	EOR (4/3, 1, IX)	
9 / 1001		SEC (2/2, 1, INH)	ADC (2/2, 2, IMM)	ADC (4/3, 2, DIR)	ADC (5/4, 3, EXT)	ADC (6/5, 3, IX2)	ADC (5/4, 2, IX1)	ADC (4/3, 1, IX)	
A / 1010		CLI (2/2, 1, INH)	ORA (2/2, 2, IMM)	ORA (4/3, 2, DIR)	ORA (5/4, 3, EXT)	ORA (6/5, 3, IX2)	ORA (5/4, 2, IX1)	ORA (4/3, 1, IX)	
B / 1011		SEI (2/2, 1, INH)	ADD (2/2, 2, IMM)	ADD (4/3, 2, DIR)	ADD (5/4, 3, EXT)	ADD (6/5, 3, IX2)	ADD (5/4, 2, IX1)	ADD (4/3, 1, IX)	
C / 1100		RSP (2/2, 1, INH)		JMP (3/2, 2, DIR)	JMP (4/3, 3, EXT)	JMP (5/4, 3, IX2)	JMP (4/3, 2, IX1)	JMP (3/2, 1, IX)	
D / 1101		NOP (2/2, 1, INH)	BSR (8/6, 2, REL)	JSR (7/5, 2, DIR)	JSR (8/6, 3, EXT)	JSR (9/7, 3, IX2)	JSR (8/6, 2, IX1)	JSR (7/5, 1, IX)	
E / 1110	STOP (*/2, 1, INH)		LDX (2/2, 2, IMM)	LDX (4/3, 2, DIR)	LDX (5/4, 3, EXT)	LDX (6/5, 3, IX2)	LDX (5/4, 2, IX1)	LDX (4/3, 1, IX)	
F / 1111	WAIT (*/2, 1, INH)	TXA (2/2, 1, INH)		STX (5/4, 2, DIR)	STX (6/5, 3, EXT)	STX (7/6, 3, IX2)	STX (6/5, 2, IX1)	STX (5/4, 1, IX)	

LEGEND

Cell format:

F		Opcode in Hexadecimal
1111		
4 (Cycles, M6805 HMOS)	3 (Cycles, M146805 CMOS)	
SUB (Mnemonic)	0 / 0000 (Opcode in Binary)	
1 (Bytes)	IX (Address Mode)	

SECTION 11
ELECTRICAL CHARACTERISTICS

11.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	− 0.3 to + 7.0	V

Input Voltage
  MC6805R2, MC6805R3, MC6805U2,
  and MC6805U3 (Except
  TIMER in Self-Check Mode
  and Open-Drain Inputs)
  Self-Check Mode (TIMER Pin Only)
	
	V_{in}
	V_{in}
		
		− 0.3 to + 7.0
		− 0.3 to + 15.0
			
			V
			V

MC68705R3/MC68705U3
  EPROM Programming Voltage
  (V_{PP} Pin)
  TIMER Pin — Normal Mode
  TIMER Pin — Bootstrap
  Programming Mode
  All Others
	
	V_{PP}
	V_{in}
	
	V_{in}
	V_{in}
		
		− 0.3 to + 22.0
		− 0.3 to + 7.0
		
		− 0.3 to + 15.0
		− 0.3 to + 7.0
			
			V
			V
			
			V
			V

Operating Temperature Range
  MC6805R2, MC6805U2, MC6805R3,
  MC6805U3, MC68705R3,
  MC68705U3, MC68705R5,
  MC68705U5
  MC6805R2C, MC6805U2C,
  MC6805R3C, MC6805U3C,
  MC68705R3C, MC68705U3C,
  MC68705R5C, MC68705U5C
  MC6805R2V, MC6805U2V,
  MC6805R3V, MC6805U3V
	
	T_A
		T_L to T_H
		
		0 to + 70
		
		− 40 to 85
		
		− 40 to 105
			
			°C

Storage Temperature Range	T_{stg}	− 55 to + 150	°C

Junction Temperature
  Plastic
  Ceramic
  Cerdip
	
	T_J
		
		150
		175
		175
			
			°C/W

These devices contain circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ and $V_{out}) \leq V_{CC}$. Reliabiity of operation is enhanced if unused inputs except EXTAL are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

11.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit

Thermal Resistance
  Plastic (P Suffix) — MC6805R2, MC6805U2,
  MC6805R3, MC6805U3
 	
  Ceramic — MC6805R2, MC6805U2, MC6805R3,
  MC6805U3, MC68705R3, MC68705U3,
  MC68705R5, MC68705U5
 	
  Cerdip — MC6805R2, MC6805U2, MC6805R3
  MC6805U3, MC68705R5, MC68705U5
	
	θ_{JA}
		
		60
		
		50
		
		60
			
			°C/W

11.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad\quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \blacktriangleleft P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An appropriate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°) \quad\quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D{}^2 \quad\quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.
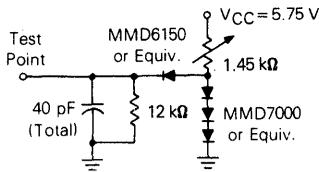
Figure 11-1. TTL Equivalent Test Load
(Port B)
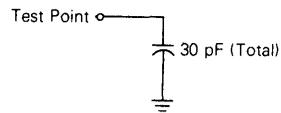
Figure 11-2. CMOS Equivalent Test Load
(Port A)
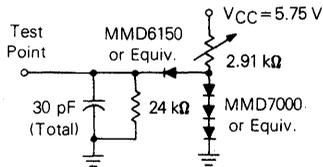
Figure 11-3. TTL Equivalent Test Load
(Ports A and C)
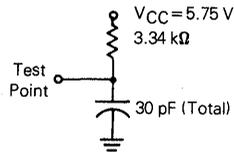
Figure 11-4. Open-Drain Equivalent Test Load
(Port C)

11.4 MC6805R2 AND MC6805R3

11.4.1 Electrical Characteristics ($V_{CC} = +5.25$ Vdc ± 0.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage $\overline{RESET}$ $(4.75 \leq V_{CC} \leq 5.75)$ $(V_{CC} < 4.75)$ $\overline{INT}$ $(4.75 \leq V_{CC} \leq 5.75)$ $(V_{CC} < 4.75)$ All Other	V_{IH}	4.0 $V_{CC} - 0.5$ 4.0 $V_{CC} - 0.5$ 2.0	— — * * —	V_{CC} V_{CC} V_{CC} V_{CC} V_{CC}	V
Input High Voltage Timer Timer Mode Self-Check Mode	V_{IH}	2.0 9.0	— 10.0	$V_{CC} + 1.0$ 15.0	V
Input Low Voltage $\overline{RESET}$ $\overline{INT}$ All Other (Except A/D Inputs)	V_{IL}	V_{SS} V_{SS} V_{SS}	— * —	0.8 1.5 0.8	V
$\overline{RESET}$ Hysteresis Voltages (See Figures 7-1, 7-2, and 7-3) "Out of Reset" "Into Reset"	V_{IRES+} V_{IRES-}	2.1 0.8	— —	4.0 2.0	V
$\overline{INT}$ Zero Crossing Input Voltage, Through a Capacitor	V_{INT}	2	—	4	$V_{ac\,p-p}$
Power Dissipation — (No Port Loading, $V_{CC} = 5.75$ V $\quad T_A = 0°C$ for Steady-State Operation) $\quad T_A = -40°C$	P_D	— —	520 580	740 800	mW
Input Capacitance XTAL All Other Except Analog Inputs (See Note)	C_{in}	— —	25 10	— —	pF
Low Voltage Recover	V_{LVR}	—	—	4.75	V
Low Voltage Inhibit	V_{LVI}	2.75	3.75	4.70	V
Input Current TIMER $(V_{in} = 0.4)$ $\overline{INT}$ $(V_{in} = 2.4$ V to $V_{CC})$ EXTAL $(V_{in} = 2.4$ V to V_{CC} Crystal Option) $(V_{in} = 0.4$ V Crystal Option) $\overline{RESET}$ $(V_{in} = 0.8$ V) (External Capacitor Charging Current)	I_{in} I_{RES}	— — — — -4.0	— 20 — — —	20 50 10 -1600 -40	μA

NOTE: Port D Analog Inputs, when selected, $C_{in} = 25$ pF for the first 5 out of 30 cycles.
* Due to internal biasing this input (when unused) floats to approximately 2.0 V.

11.4.2 Switching Characteristics (V_{CC} = +5.25 Vdc ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}	0.4	—	4.2	MHz
Cycle Time (4/f_{osc})	t_{cyc}	0.95	—	10	μs
$\overline{INT}$, $\overline{INT2}$, and TIMER Pulse Width	t_{WL}, t_{WH}	t_{cyc} + 250	—	—	ns
$\overline{RESET}$ Pulse Width	t_{RWL}	t_{cyc} + 250	—	—	ns
$\overline{INT}$ Zero-Crossing Detection Input Frequency	f_{INT}	0.03	—	1	kHz
External Clock Input Duty Cycle (EXTAL)	—	40	50	60	%
Crystal Oscillator Start-Up Time*	—	—	—	100	ms

*See Figure 7-5 for typical crystal parameters.

11.4.3 A/D Converter Characteristics (V_{CC} = +5.25 Vdc ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H
unless otherwise noted)

	Min	Typ	Max	Unit	Comments
Resolution	8	8	8	Bits	
Non-Linearity	—	—	±1/2	LSB	For V_{RH} = 4.0 to 5.0 V and V_{RL} = 0 V
Quantizing Error	—	—	±1/2	LSB	
Conversion Range	V_{RL}	—	V_{RH}	V	
V_{RH}	—	—	V_{CC}	V	A/D accuracy may decrease proportionately as
V_{RL}	V_{SS}	—	0.2	V	V_{RH} is reduced below 4.0 V. The sum of V_{RH} and
					V_{RL} must not exceed V_{CC}.
Conversion Time	30	30	30	t_{cyc}	Includes sampling time
Monotonicity	Inherent (within total error)				
Zero Input Reading	00	00	01	hexadecimal	V_{in} = 0
Ratiometric Reading	FE	FF	FF	hexadecimal	V_{in} = V_{RH}
Sample Time	5	5	5	t_{cyc}	
Sample/Hold Capacitance, Input	—	—	25	pF	
Analog Input Voltage	V_{RL}	—	V_{RH}	V	Negative transients on any analog lines (Pins 19-24) are not allowed at any time during conversion

11.4.4 Port Electrical Characteristics (V_{CC} = +5.25 Vdc ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Low Voltage I_{Load} = 1.6 mA	V_{OL}	—	—	0.4	V
Output High Voltage I_{Load} = −100 μA	V_{OH}	2.4	—	—	V
Output High Voltage I_{Load} = −10 μA	V_{OH}	V_{CC}−1	—	—	V
Input High Voltage I_{Load} = −300 μA (max)	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage I_{Load} = −500 μA (max)	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current (V_{in} = 2.0 V to V_{CC})	I_{IH}	—	—	−300	μA
Hi-Z State Input Current (V_{in} = 0.4 V)	I_{IL}	—	—	−500	μA
Port B					
Output Low Voltage I_{Load} = 3.2 mA	V_{OL}	—	—	0.4	V
Output Low Voltage I_{Load} = 10 mA (sink)	V_{OL}	—	—	1.0	V
Output High Voltage I_{Load} = −200 μA	V_{OH}	2.4	—	—	V
Darlington Current Drive (Source) V_O = 1.5 V	I_{OH}	−1.0	—	−10	mA
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	μA
Port C and Port A with CMOS Device Disabled					
Ouput Low Voltage I_{Load} = 1.6 mA	V_{OL}	—	—	0.4	V
Output High Voltage I_{Load} = −100 μA	V_{OH}	2.4	—	—	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	μA
Port C (Open-Drain Option)					
Input High Voltage	V_{IH}	2.0	—	13.0	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input Leakage Current (V_{in} = 13.0 V)	I_{LOD}	—	<3	15	μA
Output Low Voltage I_{Load} = 1.6 mA	V_{OL}	—	—	0.4	V
Port D (Digital Inputs Only)					
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input Current *	I_{in}	—	<1	5	μA

*PD4/V_{RL}−PD5/V_{RH}: The A/D conversion resistor (15 kΩ typical) is connected internally between these two lines, impacting their use as digital inputs in some applications.

11.5 MC6805U2 AND MC6805U3

11.5.1 Electrical Characteristics ($V_{CC} = +5.25$ Vdc ± 0.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage RESET ($4.75 \leq V_{CC} \leq 5.75$) ($V_{CC} < 4.75$) INT ($4.75 \leq V_{CC} \leq 5.75$) ($V_{CC} < 4.75$) All Other (Except Timer)	V_{IH}	4.0 $V_{CC} - 0.5$ 4.0 $V_{CC} - 0.5$ 2.0	— — * * —	V_{CC} V_{CC} V_{CC} V_{CC} V_{CC}	V
Input High Voltage Timer Timer Mode Self-Check Mode	V_{IH}	2.0 9.0	— 10.0	$V_{CC} + 1.0$ 15.0	V
Input Low Voltage RESET INT All Other	V_{IL}	V_{SS} V_{SS} V_{SS}	— * —	0.8 1.5 0.8	V
RESET Hysteresis Voltages (See Figures 7-1, 7-2, and 7-3) "Out of Reset" "Into Reset"	V_{IRES+} V_{IRES-}	2.1 0.8	— —	4.0 2.0	V
INT Zero Crossing Voltage, Through a Capacitor	V_{INT}	2	—	4	$V_{ac\ p-p}$
Internal Power Dissipation (No Port Loading, $V_{CC} = 5.75$ V $T_A = 0°C$ for Steady-State Operation) $T_A = -40°C$	P_{INT}	— —	520 580	740 800	mW
Input Capacitance XTAL All Other	C_{in}	— —	25 10	— —	pF
Low Voltage Recover	V_{LVR}	—	—	4.75	V
Low Voltage Inhibit	V_{LVI}	2.75	3.75	4.70	V
Input Current TIMER ($V_{in} = 0.4$ V) INT ($V_{in} = 2.4$ V to V_{CC}) EXTAL ($V_{in} = 2.4$ V to V_{CC} Crystal Option) ($V_{in} = 0.4$ V Crystal Option) RESET ($V_{in} = 0.8$ V) (External Capacitor Charging Current)	I_{in} I_{RES}	— — — — −4.0	— 20 — — —	20 50 10 −1600 −40	μA

*Due to internal biasing, this input (when unused) floats to approximately 2.0 V.

11.5.2 Switching Characteristics ($V_{CC} = +5.25$ Vdc ± 0.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}	0.4	—	4.2	MHz
Cycle Time ($4/f_{osc}$)	t_{cyc}	0.95	—	10	μs
INT, INT2, and TIMER Pulse Width	t_{WL}, t_{WH}	$t_{cyc} + 250$	—	—	ns
RESET Pulse Width	t_{RWL}	$t_{cyc} + 250$	—	—	ns
RESET Delay Time (External Cap = 1 μF)	t_{RHL}	—	100	—	ms
INT Zero Crossing Detection Input Frequency	f_{INT}	0.03	—	1.0	kHz
External Clock Input Duty Cycle (EXTAL)	—	40	50	60	%
Crystal Oscillator Start-Up Time*	—	—	—	100	ms

*See Figure 7-5 for typical crystal parameters.

11.5.3 Port Electrical Characteristics (V_{CC} = +5.25 Vdc ± 0.5 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A with CMOS drive enabled					
Output Low Voltage I_{Load} = 1.6 mA	V_{OL}	—	—	0.4	V
Output High Voltage I_{Load} = −100 μA	V_{OH}	2.4	—	—	V
Output High Voltage I_{Load} = −10 μA	V_{OH}	V_{CC} − 1.0	—	—	V
Input High Voltage I_{Load} = −300 μA (max)	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage I_{Load} = −500 μA (max)	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current (V_{in} = 2.0 V to V_{CC})	I_{IH}	—	—	−300	μA
Hi-Z State Input Current (V_{in} = 0.4 V)	I_{IL}	—	—	−500	μA
Port B					
Output Low Voltage I_{Load} = 3.2 mA	V_{OL}	—	—	0.4	V
Output Low Voltage I_{Load} = 10 mA (sink)	V_{OL}	—	—	1.0	V
Output High Voltage I_{Load} = −200 μA	V_{OH}	2.4	—	—	V
Darlington Current Drive (Source) V_O = 1.5 V	I_{OH}	−1.0	—	−10	mA
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	μA
Port C and Port A with CMOS drive disabled					
Output Low Voltage I_{Load} = 1.6 mA	V_{OL}	—	—	0.4	V
Output High Voltage I_{Load} = −100 μA	V_{OH}	2.4	—	—	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	μA
Port C (Open-Drain Option)					
Input High Voltage	V_{IH}	2.0	—	13.0	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input Leakage Current (V_{in} = 13.0 V)	I_{LOD}	—	<3	15	μA
Output Low Voltage I_{Load} = 1.6 mA	V_{OL}	—	—	0.4	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input Current	I_{in}	—	<1	5	μA

11.6 MC68705R3 AND MC68705R5

11.6.1 Programming Operation Electrical Characteristics ($V_{CC} = 5.25$ Vdc ± 0.5, $V_{SS} = 0$, $T_A = 20°$ to $30°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage	V_{PP}	20.0	21.0	22.0	V
V_{PP} Supply Current $V_{PP} = 5.25$ V $V_{PP} = 21.0$ V	I_{PP}	— —	— —	8 30	mA
Oscillator Frequency	$f_{osc(p)}$	0.9	1.0	1.1	MHz
Bootstrap Programming Mode Voltage (TIMER Pin) @ $I_{IHTP} = 100 \mu A$ Max	V_{IHTP}	9.0	12.0	15.0	V

11.6.2 Electrical Characteristics ($V_{CC} = +5.25$ Vdc ± 0.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = 0°$ to $70°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage $\overline{RESET}$ ($4.75 \leq V_{CC} \leq 5.75$) ($V_{CC} < 4.75$) $\overline{INT}$ ($4.75 \leq V_{CC} \leq 5.75$) ($V_{CC} < 4.75$) All Other	V_{IH}	4.0 $V_{CC} - 0.5$ 4.0 $V_{CC} - 0.5$ 2.0	— — ** ** —	V_{CC} V_{CC} V_{CC} V_{CC} V_{CC}	V V V
Input High Voltage (TIMER Pin) Timer Mode Bootstrap Programming Mode	V_{IH}	2.0 9.0	— 12.0	$V_{CC} + 1.0$ 15.0	V V
Input Low Voltage $\overline{RESET}$ $\overline{INT}$ All Other	V_{IL}	V_{SS} V_{SS} V_{SS}	— ** —	0.8 1.5 0.8	V V V
$\overline{INT}$ Zero-Crossing Input Voltage — Through a Capacitor	V_{INT}	2.0	—	4.0	$V_{ac\ p-p}$
Internal Power Dissipation (No Port Loading, $V_{CC} = 5.25$ V $T_A = 0°C$ for Steady-State Operation) $T_A = -40°C$	P_{INT}	— —	520 580	740 800	mW
Input Capacitance EXTAL All Other (See Note)	C_{in}	— —	25 10	— —	pF pF
$\overline{RESET}$ Hysteresis Voltage (See Figure 7-1) Out of Reset Voltage Into Reset Voltage	V_{IRES+} V_{IRES-}	2.1 0.8	— —	4.0 2.0	V V
Programming Voltage (V_{PP} Pin) Programming EPROM Operating Mode	$V_{PP}*$	20.0 4.75	21.0 V_{CC}	22.0 5.75	V V
Input Current TIMER ($V_{in} = 0.4$ V) $\overline{INT}$ ($V_{in} = 0.4$ V) EXTAL ($V_{in} = 2.4$ V to V_{CC}) ($V_{in} = 0.4$ V) $\overline{RESET}$ ($V_{in} = 0.8$ V) (External Capacitor Changing Current)	I_{in} I_{RES}	— — — — -4.0	— 20 — — —	20 50 10 -1600 -40	μA

*V_{PP} is pin 7 on the MC68705R3 and MC68705R5 and is connected to V_{CC} in the normal operating mode. In the MC6805R2, pin 7 is connected to V_{SS} in the normal operating mode. The user must allow for this difference when emulating the MC6805R2 ROM-based MCU.

**Due to internal biasing, this input (when not used) floats to approximately 2.0 V.

NOTE: Port D analog inputs, when selected, $C_{in} = 25$ pF for the first 5 out of 30 cycles.

MC68705R3 AND MC68705R5

11.6.3 Switching Characteristics ($V_{CC} = +5.25$ Vdc ± 0.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = 0°$ to $70°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency Normal	f_{osc}	0.4	–	4.2	MHz
Instruction Cycle Time ($4/f_{osc}$)	t_{cyc}	0.950	–	10	μs
$\overline{INT}$, $\overline{INT2}$, or Timer Pulse Width	t_{WL}, t_{WH}	$t_{cyc} + 250$	–	–	ns
$\overline{RESET}$ Pulse Width	t_{RWL}	$t_{cyc} + 250$	–	–	ns
$\overline{RESET}$ Delay Time (External Cap = 1.0 μF)	t_{RHL}	–	100	–	ms
$\overline{INT}$ Zero Crossing Detection Input Frequency	f_{INT}	0.03	–	1.0	kHz
External Clock Duty Cycle (EXTAL)	–	40	50	60	%
Crystal Oscillator Start-Up Time*	–	–	–	100	ms

*See Figure 7-5 for typical crystal parameters.

11.6.4 A/D Converter Characteristics ($V_{CC} = +5.25$ V ± 0.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = 0°$ to $70°C$ unless otherwise noted)

Characteristic	Min	Typ	Max	Unit	Comments
Resolution	8	8	8	Bits	
Non-Linearity	–	–	$\pm 1/2$	LSB	For $V_{RH} = 4.0$ to 5.0 V and $V_{RL} = 0$ V.
Quantitizing Error	–	–	$\pm 1/2$	LSB	
Conversion Range	V_{RL}	–	V_{RH}	V	
V_{RH}	–	–	V_{CC}	V	A/D accuracy may decrease proportionately as
V_{RL}	V_{SS}	–	0.2	V	V_{RH} is reduced below 4.0 V. The sum of V_{RH} and
Conversion Time	30	30	30	t_{cyc}	V_{RL} must not exceed V_{CC}. Includes sampling time
Monotonicity	Inherent (within total error)				
Zero Input Reading	00	00	01	hexadecimal	$V_{in} = 0$
Ratiometric Reading	FE	FF	FF	hexadecimal	$V_{in} = V_{RH}$
Sample Time	5	5	5	t_{cyc}	
Sample/Hold Capacitance, Input	–	–	25	pF	
Analog Input Voltage	V_{RL}	–	V_{RH}	V	Negative transients on any analog lines (pins 19-24) are not allowed at any time during conversion.

11.6.5 Port Electrical Characteristics ($V_{CC} = +5.25$ Vdc ± 0.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = 0°$ to $70°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A					
Output Low Voltage, $I_{Load} = 1.6$ mA	V_{OL}	—	—	0.4	V
Output High Voltage, $I_{Load} = -100\ \mu A$	V_{OH}	2.4	—	—	V
Output High Voltage, $I_{Load} = -10\ \mu A$	V_{OH}	$V_{CC} - 1.0$	—	—	V
Input High Voltage, $I_{Load} = -300\ \mu A$ (Max)	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage, $I_{Load} = -500\ \mu A$ (Max)	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current ($V_{in} = 2.0$ V to V_{CC})	I_{IH}	—	—	−300	μA
Hi-Z State Input Current ($V_{in} = 0.4$ V)	I_{IL}	—	—	−500	μA
Port B					
Output Low Voltage, $I_{Load} = 3.2$ mA	V_{OL}	—	—	0.4	V
Output Low Voltage, $I_{Load} = 10$ mA (Sink)	V_{OL}	—	—	1.0	V
Output High Voltage, $I_{Load} = -200\ \mu A$	V_{OH}	2.4	—	—	V
Darlington Current Drive (Source), $V_O = 1.5$ V	I_{OH}	−1.0	—	−10	mA
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	μA
Port C					
Output Low Voltage, $I_{Load} = 1.6$ mA	V_{OL}	—	—	0.4	V
Output High Voltage, $I_{Load} = -100\ \mu A$	V_{OH}	2.4	—	—	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	μA
Port D (Input Only)					
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input Current	I_{in}	—	<1	5	μA

11.7 MC68705U3 AND MC68705U5

11.7.1 Programming Operation Electrical Characteristics ($V_{CC} = 5.25$ Vdc ± 0.5, $V_{SS} = 0$ Vdc, $T_A = 20°$ to $30°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage	V_{PP}	20.0	21.0	22.0	V
V_{PP} Supply Current $V_{PP} = 5.25$ V $V_{PP} = 21.0$ V	I_{PP}	— —	— —	8 30	mA
Programming Oscillator Frequency	f_{oscp}	0.9	1.0	1.1	MHz
Bootstrap Programming Mode Voltage (TIMER Pin)(@ $I_{IHTP} = 100\ \mu A$ Max)	V_{IHTP}	9.0	12.0	15.0	V

11.7.2 Electrical Characteristics (V_{CC} = + 5.25 Vdc ± 0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage					
$\overline{RESET}$ (4.99 ≤ V_{CC} ≤ 5.51)		4.0	–	V_{CC}	
(V_{CC} < 4.75)		V_{CC} – 0.5	–	V_{CC}	
$\overline{INT}$ (4.99 ≤ V_{CC} ≤ 5.51)	V_{IH}	4.0	**	V_{CC}	V
(V_{CC} < 4.75)		V_{CC} – 0.5	**	V_{CC}	
All Other		2.0	–	V_{CC}	
Input High Voltage (TIMER Pin)					
Timer Mode	V_{IH}	2.0	–	V_{CC} + 1.0	V
Bootstrap Programming Mode		9.0	12.0	15.0	
Input Low Voltage					
$\overline{RESET}$		V_{SS}	–	0.8	
$\overline{INT}$	V_{IL}	V_{SS}	**	1.5	V
All Other		V_{SS}	–	0.8	
Internal Power Dissipation (No Port Loading, V_{CC} = 5.25 V T_A = 0°C	P_{INT}	–	520	740	mW
for Steady-State Operation) T_A = – 40°C		–	580	800	
Input Capacitance					
XTAL	C_{in}	–	25	–	pF
All Other		–	10	–	
$\overline{INT}$ Zero-Crossing Voltage, through a Capacitor	V_{INT}	2.0	–	4.0	$V_{ac\ p-p}$
$\overline{RESET}$ Hysteresis Voltage (See Figure 7-1)					
Out of Reset Voltage	V_{IRES+}	2.1	–	4.0	V
Into Reset Voltage	V_{IRES-}	0.8	–	2.0	
Programming Voltage (Vpp Pin)					
Programming EPROM	V_{PP}*	20.0	21.0	22.0	V
Operating Mode		4.75	V_{CC}	5.75	
Input Current					
TIMER (V_{in} = 0.4 V)		–	–	20	
$\overline{INT}$ (V_{in} = 0.4 V)		–	20	50	
EXTAL (V_{in} = 2.4 V to V_{CC} Crystal Option)	I_{in}	–	–	10	μA
(V_{in} = 0.4 V Crystal Option)		–	–	– 1600	
$\overline{RESET}$ (V_{in} = 0.8 V)	I_{RES}	– 4.0	–	– 40	
(External Capacitor Changing Current)					

*Vpp is Pin 7 on the MC68705U3 and MC68705U5 and is connected to V_{CC} in the Normal Operating Mode. In the MC6805U2, Pin 7 is NUM and is connected to V_{SS} in the Normal Operating Mode. The user must allow for this difference when emulating the MC6805U2 ROM-based MCU.

**Due to internal biasing, this input (when not used) floats to approximately 2.0 V.

11.7.3 Switching Characteristics (V_{CC} = + 5.25 Vdc, ± 0.5 V, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency					
Normal	f_{osc}	0.4	–	4.2	MHz
Instruction Cycle Time (4/f_{osc})	t_{cyc}	0.950	–	10	μs
$\overline{INT}$, $\overline{INT2}$, or Timer Pulse Width	t_{WL}, t_{WH}	t_{cyc} + 250	–	–	ns
$\overline{RESET}$ Pulse Width	t_{RWL}	t_{cyc} + 250	–	–	ns
$\overline{RESET}$ Delay Time (External Cap = 1.0 μF)	t_{RHL}	100	–	–	ms
$\overline{INT}$ Zero Crossing Detection Input Frequency	f_{INT}	0.03	–	1.0	kHz
External Clock Duty Cycle (EXTAL)	–	40	50	60	%
Crystal Oscillator Start-Up Time*	–	–	–	100	ms

* See Figure 7-5 for typical crystal parameters.

11.7.4 Port Electrical Characteristics ($V_{CC} = +5.25$ Vdc ± 0.5 Vdc, $V_{SS} = 0$ Vdc, $T_A = 0°$ to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A					
Output Low Voltage, $I_{Load} = 1.6$ mA	V_{OL}	—	—	0.4	V
Output High Voltage, $I_{Load} = -100\ \mu A$	V_{OH}	2.4	—	—	V
Output High Voltage, $I_{Load} = -10\ \mu A$	V_{OH}	$V_{CC} - 1.0$	—	—	V
Input High Voltage, $I_{Load} = -300\ \mu A$ (Max)	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage, $I_{Load} = -500\ \mu A$ (Max)	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current ($V_{in} = 2.0$ V to V_{CC})	I_{IH}	—	—	-300	μA
Hi-Z State Input Current ($V_{in} = 0.4$ V)	I_{IL}	—	—	-500	μA
Port B					
Output Low Voltage, $I_{Load} = 3.2$ mA	V_{OL}	—	—	0.4	V
Output Low Voltage, $I_{Load} = 10$ mA (Sink)	V_{OL}	—	—	1.0	V
Output High Voltage, $I_{Load} = -200\ \mu A$	V_{OH}	2.4	—	—	V
Darlington Current Drive (Source), $V_O = 1.5$ V	I_{OH}	-1.0	—	-10	mA
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	μA
Port C					
Output Low Voltage, $I_{Load} = 1.6$ mA	V_{OL}	—	—	0.4	V
Output High Voltage, $I_{Load} = -100\ \mu A$	V_{OH}	2.4	—	—	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	μA
Port D (Input Only)					
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input Current	I_{in}	—	<1	5	μA

11.8 I/O CHARACTERISTICS

Figures 11-5 through 11-15 illustrate I/O characteristic data for HMOS M6805 Family devices. Simplified port logic diagrams are shown in Figures 11-16 and 11-17, typical input protection in Figure 11-18, and an I/O characteristic measurement circuit in Figure 11-19. The I/O characteristic curves and logic diagrams are intended to allow the system designer to interface the M6805 in a variety of applications where non-TTL loading conditions exist.

A minimum specification curve (included with V_{OH} vs I_{OH} charts only) is provided as a guaranteed limit of performance under the conditions shown. The expected minimum and maximum curves in each figure represent the anticipated performance window under normal manufacturing and operating conditions. A typical curve also is illustrated indicating performance under nominal conditions.

Figure 11-15 represents the variation of I_{DD} with temperature and V_{DD} for a typical M6805 Family device. As shown, I_{DD} varies directly with V_{DD} and inversely with temperature.
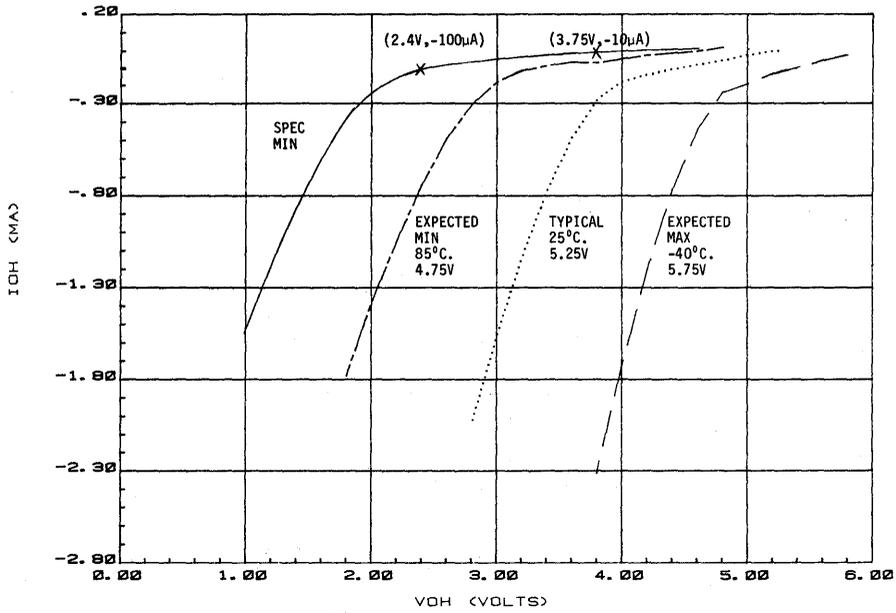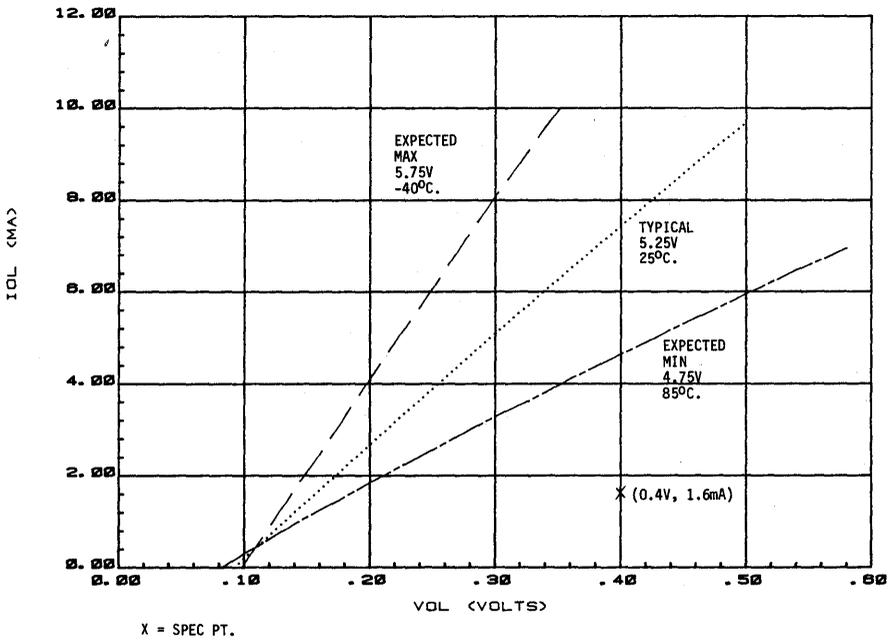
Figure 11-5. Port A V_{OH} vs I_{OH}
(with CMOS Pull-ups)

X = SPEC PT.

Figure 11-6. Port A V_{OL} vs I_{OL}
(with CMOS Pull-ups)
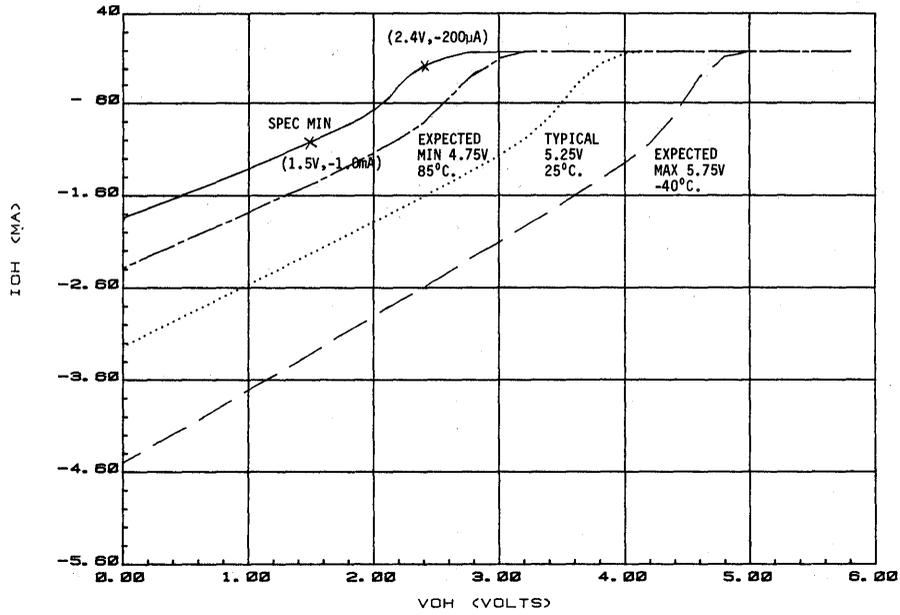
Figure 11-7. Port B V_{OH} vs I_{OH}

X = SPEC PT.
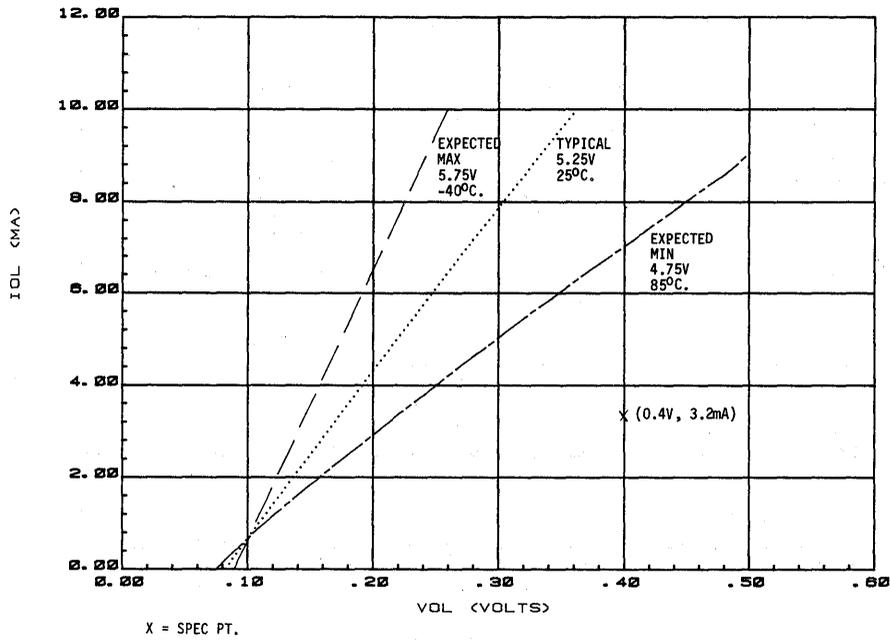
Figure 11-8. Port B V_{OL} vs I_{OL}
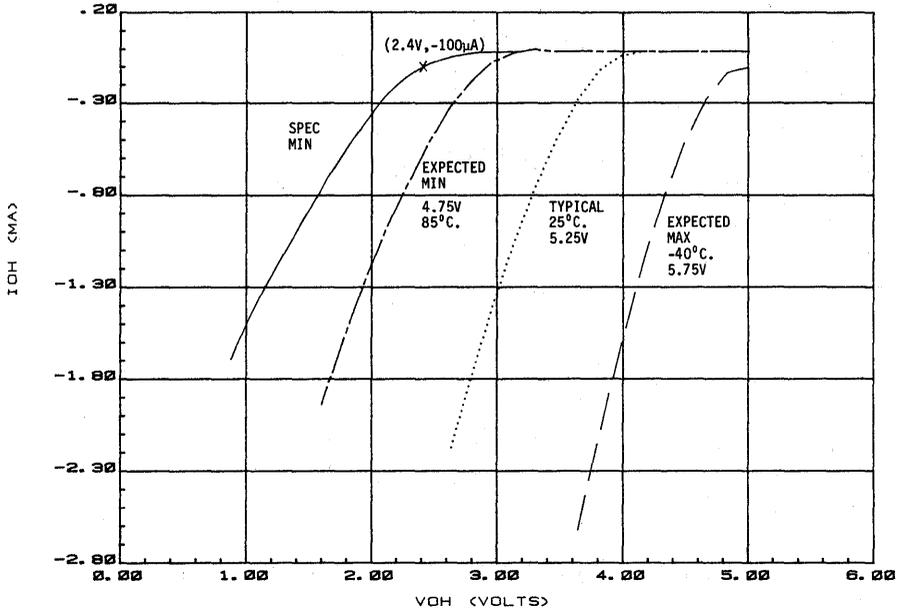
Figure 11-9. Port C V_{OH} vs I_{OH}
(Port A Without CMOS Pull-ups)

X = SPEC PT.
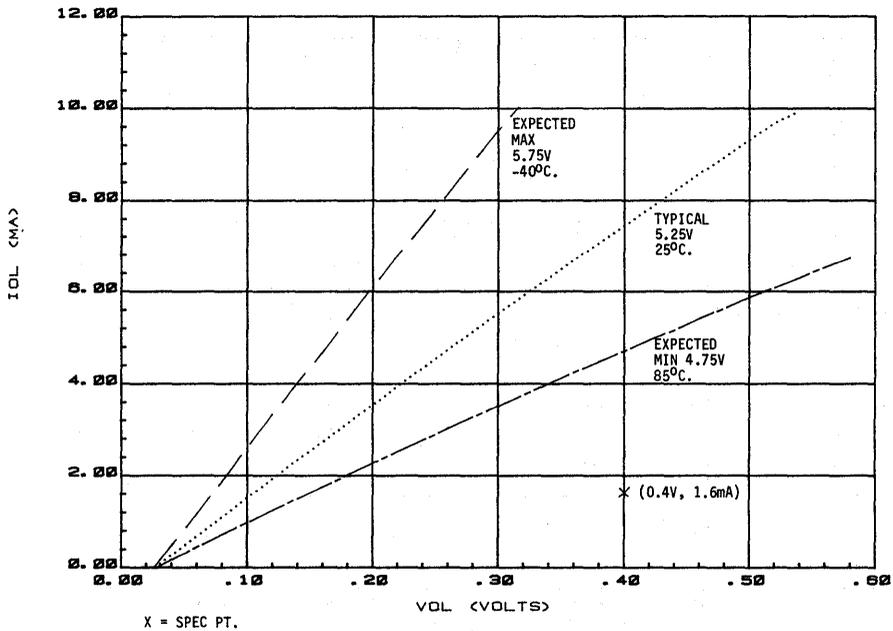
Figure 11-10. Port C V_{OL} vs I_{OL}
(Port A Without CMOS Pull-ups)
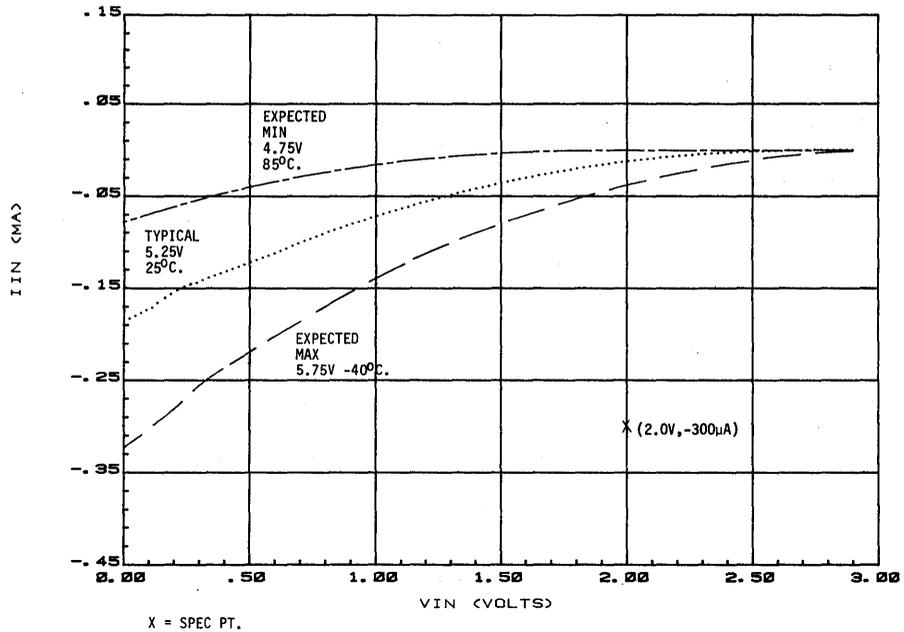
Figure 11-11. Port A V_{in} vs I_{in}
(with CMOS Pull-ups)

Figure 11-12. EXTAL V_{in} vs I_{in}
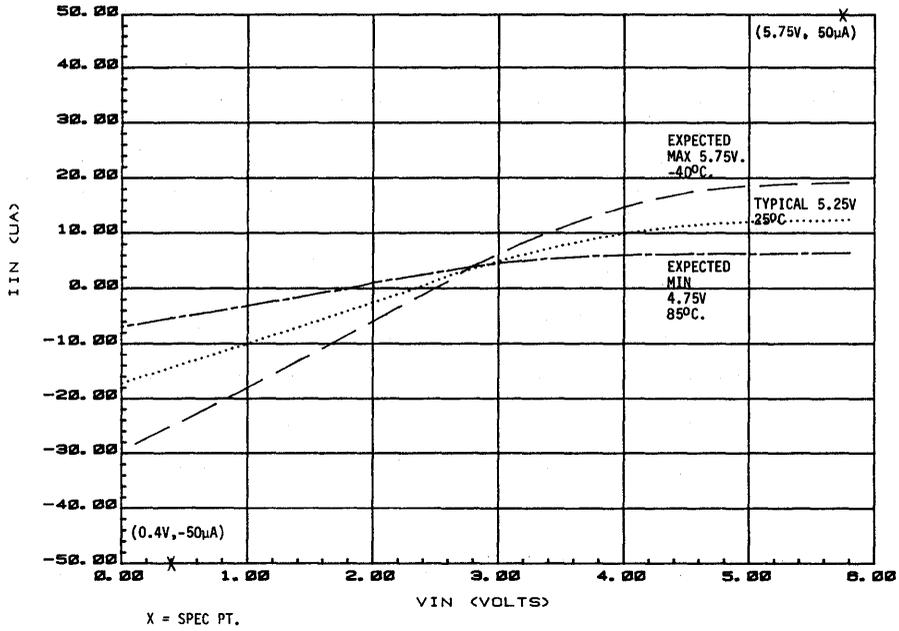
Figure 11-13. Interrupt V_{in} vs I_{in}
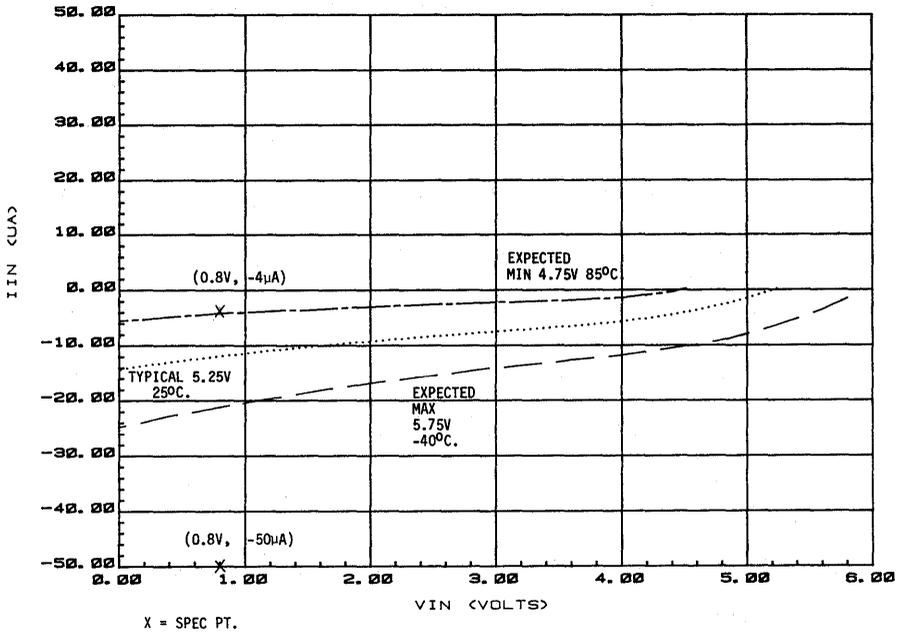
Figure 11-14. $\overline{RESET}$ V_{in} vs I_{in}
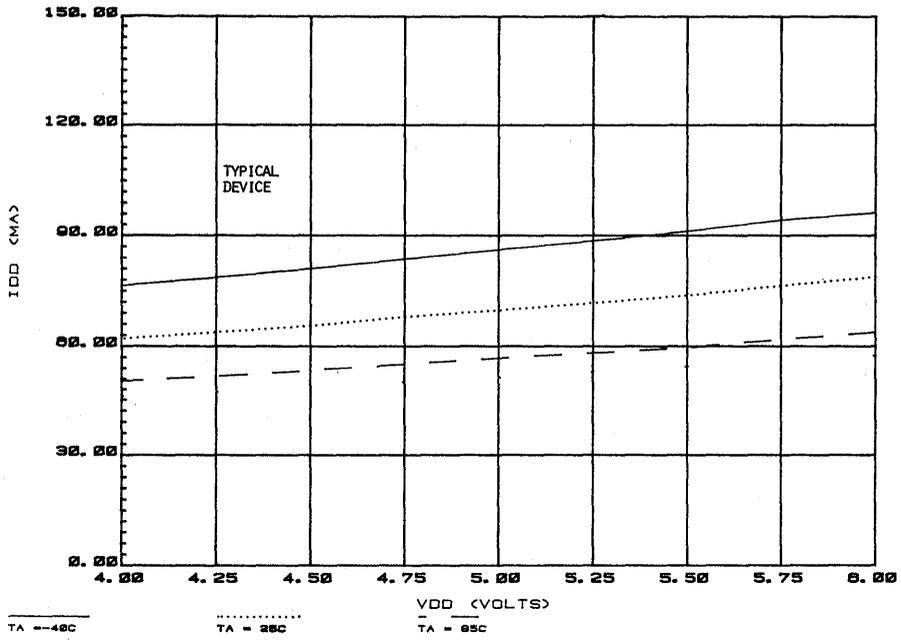
Figure 11-15. V_{DD} vs I_{DD}
(Variation with Temperature)
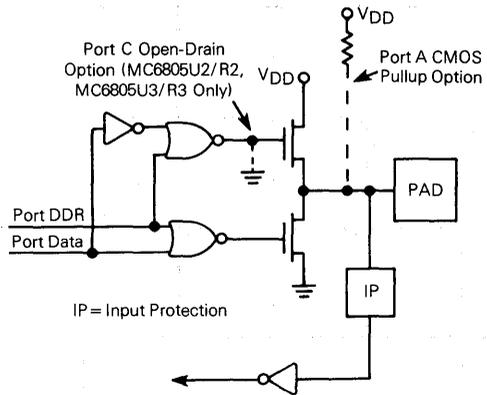
Figure 11-16. Ports A and C Logic Diagram
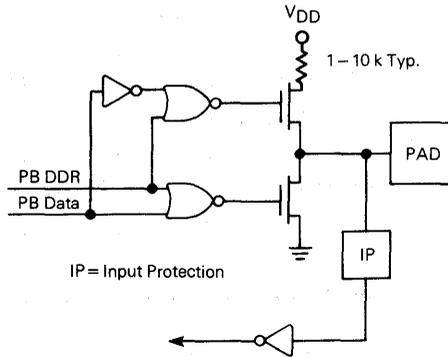
Figure 11-17. Port B Logic Diagram
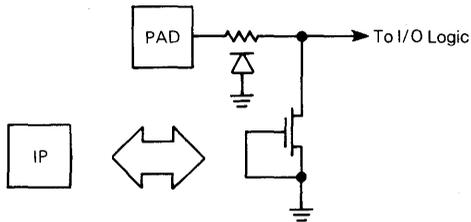
Figure 11-18. Typical Input Protection
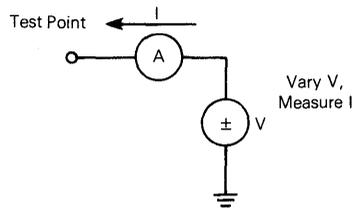
Figure 11-19. I/O Characteristic
Measurement Circuit

SECTION 12
ORDERING INFORMATION

This section contains detailed information to be used as a guide when ordering an MC68(7)05 series device.

12.1 MC6805R2

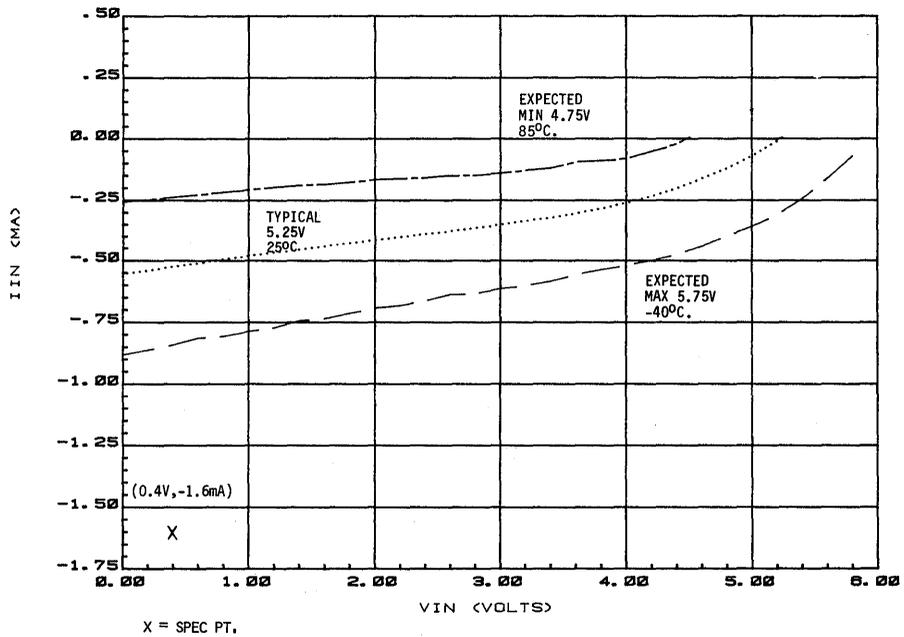| Package Type	Temperature	Generic Number
Ceramic	0°C to 70°C	MC6805R2L
L Suffix	−40°C to 85°C	MC6805R2CL
Plastic	0°C to 70°C	MC6805R2P
P Suffix	−40°C to 85°C	MC6805R2CP
Cerdip	0°C to 70°C	MC6805R2S
S Suffix	−40°C to 85°C	MC6805R2CS

12.2 MC6805R3

Package Type	Temperature	Generic Number
Ceramic	0°C to 70°C	MC6805R3L
L Suffix	−40°C to 85°C	MC6805R3CL
Plastic	0°C to 70°C	MC6805R3P
P Suffix	−40°C to 85°C	MC6805R3CP
Cerdip	0°C to 70°C	MC6805R3S
S Suffix	−40°C to 85°C	MC6805R3CS

12.3 MC6805U2

Package Type	Temperature	Generic Number
Ceramic	0°C to 70°C	MC6805U2L
L Suffix	−40°C to 85°C	MC6805U2CL
Plastic	0°C to 70°C	MC6805U2P
P Suffix	−40°C to 85°C	MC6805U2CP
Cerdip	0°C to 70°C	MC6805U2S
S Suffix	−40°C to 85°C	MC6805U2CS

12.4 MC6805U3

Package Type	Temperature	Generic Number
Ceramic	0°C to 70°C	MC6805U3L
L Suffix	−40°C to 85°C	MC6805U3CL
Plastic	0°C to 70°C	MC6805U3P
P Suffix	−40°C to 85°C	MC6805U3CP
Cerdip	0°C to 70°C	MC6805U3S
S Suffix	−40°C to 85°C	MC6805U3CS

12.5 MC68705R3

Package Type	Temperature	Generic Number
Ceramic	0°C to 70°C	MC68705R3L
L Suffix	−40°C to 85°C	MC68705R3CL

12.6 MC68705R5

Package Type	Temperature	Generic Number
Ceramic	0°C to 70°C	MC68705R5L
L Suffix	−40°C to 85°C	MC68705R5CL
Cerdip	0°C to 70°C	MC68705R5S
S Suffix	−40°C to 85°C	MC68705R5CS

12.7 MC68705U3

Package Type	Temperature	Generic Number
Ceramic	0°C to 70°C	MC68705U3L
L Suffix	−40°C to 85°C	MC68705U3CL

12.8 MC68705U5

Package Type	Temperature	Generic Number
Ceramic	0°C to 70°C	MC68705U5L
L Suffix	−40°C to 85°C	MC68705U5CL
Cerdip	0°C to 70°C	MC68705U5S
S Suffix	−40°C to 85°C	MC68705U5CS

12.9 CUSTOM MCUs

The information required when ordering a custom MCU is listed below. The ROM program may be transmitted to Motorola on EPROM(s) or an MDOS disk file.

To initiate a ROM pattern for the MCU it is necessary to first contact your local Motorola representative or Motorola distributor.

12.9.1 EPROMs

The MCM2716 or MCM2532 type EPROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The EPROM must be clearly marked to indicate which EPROM corresponds to which address space. The recommended marking procedure for two MCM2716 EPROMs is shown in Figure 12-1.
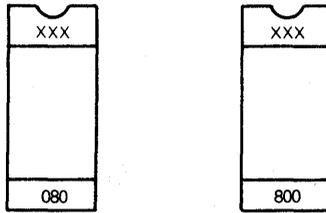
XXX = Customer ID

Figure 12-1. Recommended Marking Procedure

After the EPROM(s) are marked, they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.

12.9.2 Verfication Media

All original pattern media (EPROMs or floppy disk) are filed for contractural purposes and are not returned. A computer listing of the ROM code will be generated and returned along with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed, and returned to Motorola. The signed verification form constitutes the contractual agreement for creation of the customer mask. If desired, Motorola will program one blank EPROM from the data file used to create the custom mask to aid in the verification process.

12.9.3 ROM Verification Units (RVUs)

Ten MCUs containing the customer's ROM pattern will be sent for program verification. These units will have been made using the custom mask but are for the purpose of ROM verification only. For expediency they are usually unmarked, packaged in ceramic, and tested only at room temperature and 5 volts. These RVUs are included in the mask charge and are not production parts. Therefore, the RVUs are not guaranteed by Motorola Quality Assurance, and should be discarded after verification is completed.

12.9.4 Flexible Disk

The disk media submitted must be single-sided, single-density, 8-inch MDOS compatible floppies. The customer must write the binary file name and company name on the disk with a felt-tip pen. The minimum MDOS system files as well as the absolute binary object file (filename .LO type of file) from the M6805 cross assembler must be on the disk. An object file made from a memory dump using the ROLLOUT command is also acceptable. Consider submitting a source listing as well as the following files: filename .LX (EXORciser loadable format) and filename .SA (ASCII source code). These files will of course be kept confidential and are used 1) to speed up the process in-house if any problems arise, and 2) to speed up the user-to-factory interface if the user finds any software errors and needs assistance quickly from Motorola factory representatives.

MDOS is Motorola's Disk Operating System available on development systems such as EXORcisers, EXORsets, etc.

EXORset and MDOS are trademarks of Motorola Inc.

Date _____ Customer PO Number _____

Customer Company _____ Motorola Part Number
                                                MC _____
Address _____ SC _____

City _____ State _____ Zip _____

Country _____

Phone _____ Extension _____

Customer Contact Person _____

Customer Part Number _____

MC6805R2/U2/R3/U3 OPTION LIST

Select the options for your MCU from the following list. A manufacturing mask will be generated from this information.

Internal Oscillator Input
☐ Crystal
☐ Resistor

Low Voltage Inhibit
☐ Disable
☐ Enable

Timer Clock Source
MC6805R2/U2 Only
☐ Internal $\phi2$ clock
☐ TIMER input pin

Timer Prescaler
MC6805R2/U2 Only
☐ 2^0 (divide by 1)
☐ 2^1 (divide by 2)
☐ 2^2 (divide by 4)
☐ 2^3 (divide by 8)
☐ 2^4 (divide by 16)
☐ 2^5 (divide by 32)
☐ 2^6 (divide by 64)
☐ 2^7 (divide by 128)

Port A Output Drive
☐ CMOS and TTL
☐ TTL Only

Port C Output Drive
☐ TTL
☐ Open-Drain

Pattern Media (All other media requires prior factory approval)
☐ EPROMs (MCM2716 or MCM2532)
☐ Floppy Disk
☐ Other* _____

Clock Frequency _____

Temperature Range _____ 0°C to +70°C (Standard)
                                                              −40°C to +85°C
                                                              −40°C to +105°C

Marking Information (12 Characters Maximum)

Title _____

Signature _____

Figure 12-2. Sample Custom MCU Order Form

SECTION 13
MECHANICAL DATA

This section contains the pin assignments and package dimensions for the MC68(7)05 series devices.

13.1 PIN ASSIGNMENT

MC6805R2

Left	Pin		Pin	Right
V_{SS}	1 ●		40	PA7
$\overline{RESET}$	2		39	PA6
$\overline{INT}$	3		38	PA5
V_{CC}	4		37	PA4
EXTAL	5		36	PA3
XTAL	6		35	PA2
(V_{SS}) NUM	7		34	PA1
TIMER	8		33	PA0
PC0	9		32	PB7
PC1	10		31	PB6
PC2	11		30	PB5
PC3	12		29	PB4
PC4	13		28	PB3
PC5	14		27	PB2
PC6	15		26	PB1
PC7	16		25	PB0
PD7	17		24	PD0/AN0
PD6/$\overline{INT2}$	18		23	PD1/AN1
PD5/V_{RH}	19		22	PD2/AN2
PD4/V_{RL}	20		21	PD3/AN3

MC6805R3

Left	Pin		Pin	Right
V_{SS}	1 ●		40	PA7
$\overline{RESET}$	2		39	PA6
$\overline{INT}$	3		38	PA5
V_{CC}	4		37	PA4
EXTAL	5		36	PA3
XTAL	6		35	PA2
NC	7		34	PA1
TIMER	8		33	PA0
PC0	9		32	PB7
PC1	10		31	PB6
PC2	11		30	PB5
PC3	12		29	PB4
PC4	13		28	PB3
PC5	14		27	PB2
PC6	15		26	PB1
PC7	16		25	PB0
PD7	17		24	PD0/AN0
PD6/$\overline{INT2}$	18		23	PD1/AN1
PD5/V_{RH}	19		22	PD2/AN2
PD4/V_{RL}	20		21	PD3/AN3

MC6805U2

V$_{SS}$	1 ●	40	PA7
$\overline{RESET}$	2	39	PA6
$\overline{INT}$	3	38	PA5
V$_{CC}$	4	37	PA4
EXTAL	5	36	PA3
XTAL	6	35	PA2
(V$_{SS}$) NUM	7	34	PA1
TIMER	8	33	PA0
PC0	9	32	PB7
PC1	10	31	PB6
PC2	11	30	PB5
PC3	12	29	PB4
PC4	13	28	PB3
PC5	14	27	PB2
PC6	15	26	PB1
PC7	16	25	PB0
PD7	17	24	PD0
PD6/$\overline{INT2}$	18	23	PD1
PD5	19	22	PD2
PD4	20	21	PD3

MC6805U3

V$_{SS}$	1 ●	40	PA7
$\overline{RESET}$	2	39	PA6
$\overline{INT}$	3	38	PA5
V$_{CC}$	4	37	PA4
EXTAL	5	36	PA3
XTAL	6	35	PA2
NC	7	34	PA1
TIMER	8	33	PA0
PC0	9	32	PB7
PC1	10	31	PB6
PC2	11	30	PB5
PC3	12	29	PB4
PC4	13	28	PB3
PC5	14	27	PB2
PC6	15	26	PB1
PC7	16	25	PB0
PD7	17	24	PD0
PD6/$\overline{INT2}$	18	23	PD1
PD5	19	22	PD2
PD4	20	21	PD3

MC68705R3/MC68705R5

```
        VSS   1  ●        40   PA7
      RESET   2            39   PA6
        INT   3            38   PA5
        VCC   4            37   PA4
      EXTAL   5            36   PA3
       XTAL   6            35   PA2
        VPP   7            34   PA1
      TIMER   8            33   PA0
        PC0   9            32   PB7
        PC1  10            31   PB6
        PC2  11            30   PB5
        PC3  12            29   PB4
        PC4  13            28   PB3
        PC5  14            27   PB2
        PC6  15            26   PB1
        PC7  16            25   PB0
        PD7  17            24   PD0/AN0
   PD6/INT2  18            23   PD1/AN1
   PD5/VRH   19            22   PD2/AN2
   PD4/VRL   20            21   PD3/AN3
```

MC68705U3/MC68705U5

```
        VSS   1  ●        40   PA7
      RESET   2            39   PA6
        INT   3            38   PA5
        VCC   4            37   PA4
      EXTAL   5            36   PA3
       XTAL   6            35   PA2
        VPP   7            34   PA1
      TIMER   8            33   PA0
        PC0   9            32   PB7
        PC1  10            31   PB6
        PC2  11            30   PB5
        PC3  12            29   PB4
        PC4  13            28   PB3
        PC5  14            27   PB2
        PC6  15            26   PB1
        PC7  16            25   PB0
        PD7  17            24   PD0
   PD6/INT2  18            23   PD1
        PD5  19            22   PD2
        PD4  20            21   PD3
```

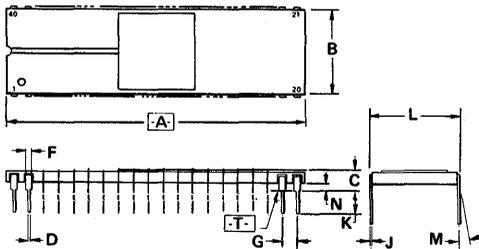## 13.2 PACKAGE DIMENSIONS

13.2.1 Ceramic — MC6805R2, MC6805R3, MC6805U2, MC6805U3

L SUFFIX
CERAMIC PACKAGE
CASE 715-05

NOTES:
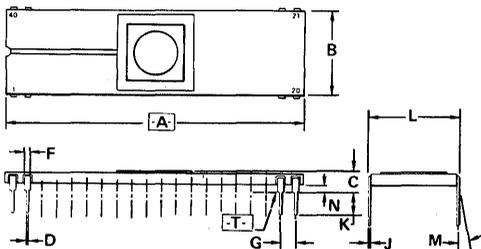1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

| ⊕ | 0.25 (0.010) Ⓜ | T | A Ⓜ |

3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

13.2.2 Ceramic — MC68705R3, MC68705R5, MC68705U3, MC68705U5

L SUFFIX
CERAMIC PACKAGE
CASE 715-06

NOTES:
1. DIMENSION -A- IS DATUM.
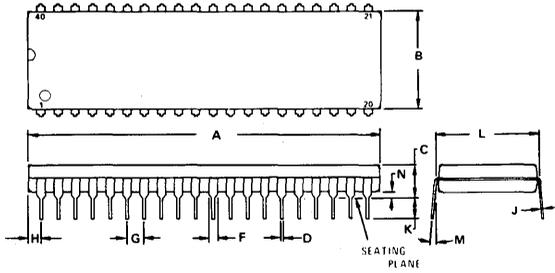2. POSITIONAL TOLERANCE FOR LEADS:

| ⊕ | 0.25 (0.010) Ⓜ | T | A Ⓜ |

3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	3.18	5.08	0.125	0.200
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

13.2.3 Plastic — MC6805R2, MC6805R3, MC6805U2, MC6805U3

P SUFFIX
PLASTIC PACKAGE
CASE 711-01

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

13.2.4 Cerdip — MC6805R2, MC6805R3, MC6805U2, MC6805U3

S SUFFIX
CERDIP PACKAGE
CASE 734-03
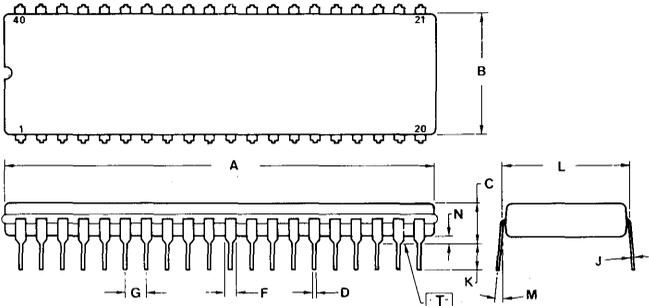
NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

⊕ | ∅ 0.25(0.010) Ⓜ | T | A Ⓜ |

3. -T- IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050