MOS DESIGN COURSE

March 1

Monday	Introduction to MOS Business	Robert Handy
	The MOS Transistor	Bill Richardson
	MOS Processing	Jim Rutledge
	Logic Circuit Families	Bruce Fette
	Shift Register Circuit Familes	Geoff Batchelder
Tuesday	RAM Circuit Families	Charles Hoffman
	ROM Circuit Families	John Buchanan
	MOS Device Parameters	Ed Armstrong
	MOS Device Model	Bill Lattin
	DC Circuit Design	Bruce Fette
Wednesday	AC Circuit Design	Tom Gunter
	Systems Design	Tom Bennett
	Custom - Design Interface	Gene Schriber
	C-MOS Design	Bernie Schmidt
	Bipolar Interface	John Buchanan
Thursday	Computer Aids - Design Software	Bruce Fette
	Computer Aids - Layout Software	Warren Crews
	Computer Aids - Layout Hardware	Warren Crews
	Computer Aids - Cell Library	Bert Cutler
Friday	Design Economics	Robert Handy
	Packaging - Assembly	Steve Fryncko
	Circuit Evaluation	Terry Holdt
	Circuit Testing	Hal Hall
	Customer Support	Gene Puckett

CHAPTER I

INTRODUCTION TO THE MOS BUSINESS

The MOS Market

The recorded history of the MOS industry was started in 1967 by EIA. The numbers obtained from the MOS manufacturers concerned only the total product shipped and did not breakout the functions or types of circuits that were involved until 1969. The chart in Figure 1.1 shows the reported growth through 1975. The total MOS business includes a large amount of custom development and production work which is not included in the normal EIA reporting system. Examples of this are internal consumption and suppliers who are not participating in the EIA program. This makes the total MOS market somewhat larger than that being reported by EIA. It is this figure that we use to compare to the total IC industry.

The Market in 1969

Figure 1.2 summarizes the EIA reported 1969 MOS IC market from a product point of view. Note the four largest entries excluding subtotals. These are:

Dynamic Shift Registers over 100 bits	$ 3,556,200
Static Shift Registers, 4-50 bits	2,041,707
Dynamic Shift Registers, 4-100 bits	1,536,059
Static Shift Registers, 51-100 bits	852,846
TOTAL	$ 7,986,812

This means that shift register sales comprised the majority of the reported MOS IC business for 1969. Following is a breakout of market percentages by product category:

Shift Registers	59.5%
Complex Logic Functions	13.6%
Memories	12.1%
Simple Logic Functions	9.8%
LSI excluding Shift Registers	5.0%
TOTAL EIA REPORTED MOS IC	100.0%

The 25 million dollars of MOS IC business indicated for 1969 includes the 13.5 million reported to the EIA. The remaining 11.5 million of unreported business is estimated to be almost entirely custom with the exception of internal consumption. Percentage distributions by product category for this business is estimated to be approximately the same as indicated in the EIA percentage breakout. Custom business for 1969 was estimated at $18 million, and standard product business was $7 million.

MARKET TRENDS

Product Trends

Although uniform reporting media has been in effect for only one year, it is possible to detact trends in certain product areas:

(a) Memories are increasing their share of the MOS IC market. Rate of increase is indeterminate at present.

(b) Shift registers are slowly decreasing their share of the market. However, the losses in market share of dynamic shift registers may be offset by gains in static shift registers as their volume increases. Static shift registers show surprising customer interest, and dollar volume for static shift registers will surpass dollar volume for dynamic shift registers in 1970.

(c) Simple logic functions are increasing their share of the market, but this is probably due to the increasing popularity of complementary MOS IC and MOS interface elements.

Price Trends

The ASP will continue to decline for all categories. EIA reported ASP's by product category for 1969 are shown in Figure 1.2. The downward trend is shown in Figure 1.3. The EIA reported ASP for 1970 will be less than $6.00. However, the ASP's for unreported sales, which are principally custom programs, will raise the overall ASP to approximately $6.50 for 1970. The overall ASP for 1971 will be approximately in the $4.50 to $5.00 range.

General Trends

The lower ASP's are expanding the MOS IC market into areas where semiconductor logic was heretofore unfeasible due to price, power, or packaging density. These areas already include memories, low cost desk calculators, and delay lines. Other potential markets are electronic clocks and timers, electronic fuel systems and anti-skid systems on automobiles, continuous room status monitoring for hotels and motels, and electronic wrist watches. Other markets not yet know will undoubtedly become viable as the ASP's of MOS IC's drop.

Figure 1.4 compares projected MOS IC growth with TTL growth and total IC growth. This Figure substantiates, on the basis of past history, the validity of the high growth rate projected for the MOS IC market. Figure 1.5 graphically compares the growth rates for MOS IC versus total IC. Estimated end-use applications for MOS IC product in 1970 are shown in Figure 1.6.

The International Market

The usage of MOS integrated circuits in Europe is characterized by a wide variety of applications as they are in the United

States. The growth of the European market is treading along a similar pattern to the U.S. and is lagging by approximately two years. A projection recently made by Telefunken is:

European MOS Market

1969	1970	1971	1972	1973	1974
$5M	10M	20M	40M	60M	100M

The primary competition is found in the efforts of General Instruments and National Semiconductor. These manufacturers have had MOS facilities in the common market for approximately 2 years. Activity is being stepped up by several other companies such as Fairchild, Phillips, Seimens, Plessey, Ferranti, Telefunken, Sescosem, and SGS.

In the Far East the MOS usage has been concentrated in the desk top calculator and organ industry and is now finding its way into small computers and computer terminals. Much of the volume has been imported from the United States but the Japanese are rapidly gearing up their own source of supply. A projection of the MOS market has been made by Motorola Sales in Japan, starting at $20M in 1969 and growing at $20M/per year. Because of equipment slippage and lack of product from suppliers this estimate has been adjusted to:

Japanese MOS Market

1969	1970	1971	1972	1973	1974
$12M	25M	40M	60M	80M	110M

Summary

Approximately $45 million worth of MOS IC's will be sold in 1970. EAI will report about $29 million of this. Over two-thirds of the business will be custom. Half the business will be in shift registers. The ASP (EIA reported) will be less than $6.00. The market will continue to double for several years. By 1974, more than 30 percent of the total integrated circuit market will be MOS, and the ASP will be in the $2.00 to $2.50 range. The broadening customer base will continue to enhance custom MOS IC business, and make a custom capability worthwhile.

EIA REPORTED

U.S. FACTORY SALE OF MOS INTEGRATED CIRCUITS

GRAND TOTAL 1969

Line	Major Function	Units (#)	Dollars ($)	Percent of Dollars	ASP
1	Logic Gates	153,880	699,584	5.17	4.55
2	Logic Input Expanders	10,207	24,685	0.18	2.42
3	Drivers, Buffers & Expanders	28,471	159,596	1.18	5.61
4	Multivibrators Monostable	2,160	4,588	0.03	2.11
5	Single & Dual Flip-Flops	43,117	379,441	2.80	8.80
6	Other	26,631	56,265	0.42	2.11
7	SUB-TOTAL - Class I	264,466	1,324,129	9.78	5.01
8	Adders & Subtractors	11,438	99,394	0.73	8.69
9	Encoders, Decoders & Translators	21,333	240,862	1.78	11.29
10	Counters & Timers 4-50 bits	115,581	497,351	3.67	4.30
11	Counters & Timers 51-100 bits	2,352	18,108	0.13	7.70
12	Latches	8,557	148,533	1.10	17.36
13	Static Shift Registers 4-50 bits	299,603	2,041,707	15.08	6.81
14	Static Shift Registers 51-100 bits	61,644	852,486	6.30	13.83
15	Dynamic Shift Registers 4-100 bits	307,954	1,536,059	11.35	4.99
16	MUX Switches & Commutators	34,387	557,345	4.12	16.21
17	A-D/D-A Converters	5,472	148,264	1.10	27.10
18	Other	8,456	133,771	0.99	15.82
19	SUB-TOTAL - Class II	876,777	6,273,880	46.34	7.16
20	ROM 4-256 bits	4,832	92,994	0.69	19.25
21	ROM 256-1024 bits	16,890	591,608	4.37	35.03
22	ROM 1025 & over bits	15,906	549,519	4.06	34.55
23	RAM 4-32 bits	6,817	72,123	0.53	10.58
24	RAM 33-256 bits	12,065	329,334	2.43	27.30
25	RAM 257 & over bits	0	0	----	---
26	SUB-TOTAL - Class III	56,510	1,635,578	12.08	28.94
27	Static Shift Registers over 100 bits	4,957	69,906	0.52	14.10
28	Dynamic Shift Registers over 100 bits	302,890	3,556,200	26.27	11.74
29	Other Arrays over 100 gates	29,404	679,102	5.02	23.10
30	SUB-TOTAL - Class IV	337,251	4,305,208	31.08	12.77
31	GRAND TOTAL - All Classes	1,535,004	13,538,795	100.00	8.82
32	Total Static Shift Registers	366,204	2,964,099	21.89	8.09
33	Total Dynamic Shift Registers	610,844	4,092,259	37.61	8.34
34	Total Shift Registers	977,048	8,056,308	59.51	8.25

Figure 1.2

FIGURE 1.3

MOS INTEGRATED CIRCUITS
EIA REPORTED ASP BY QUARTER

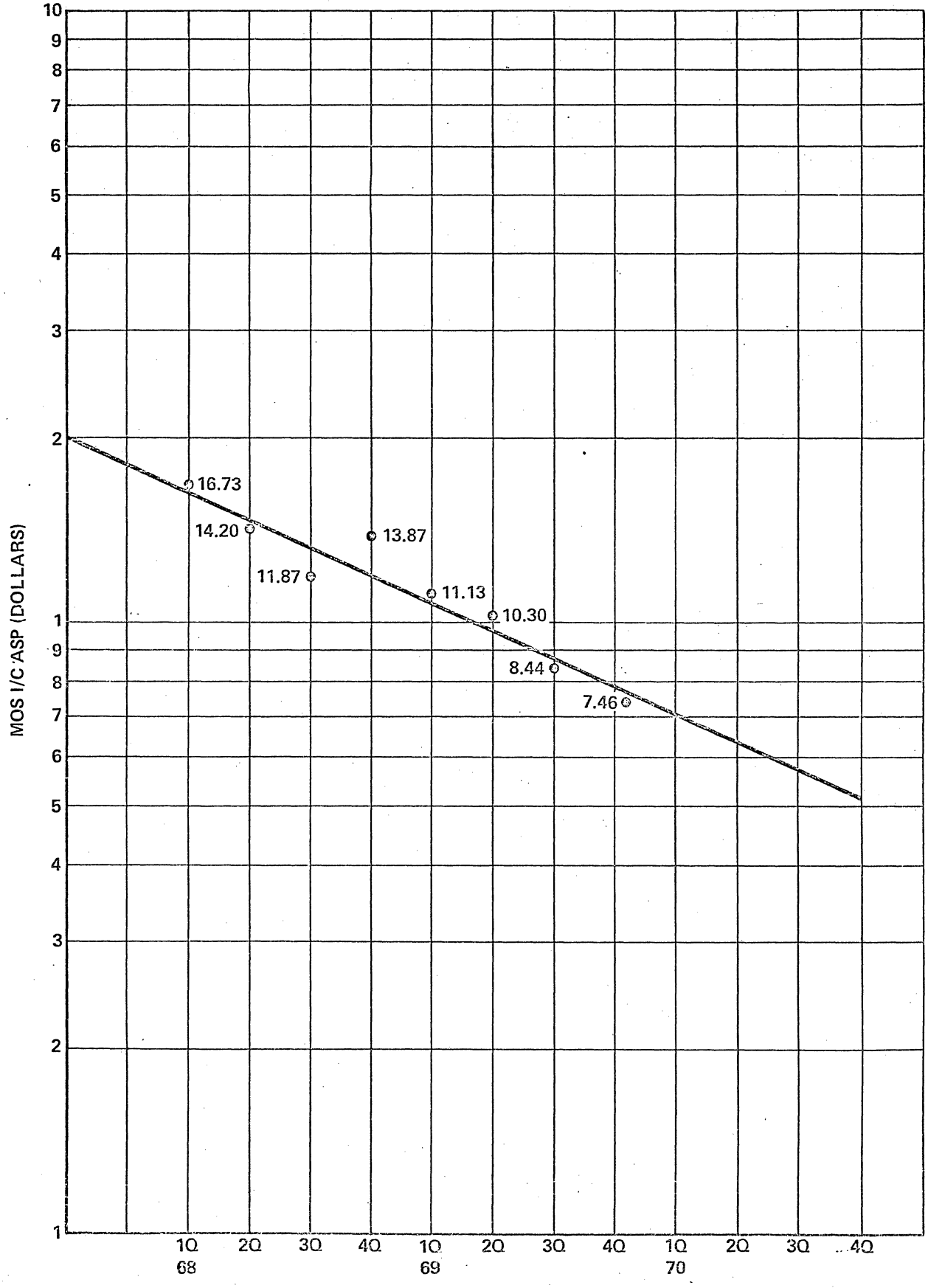


FIGURE 1.4

COMPARISON OF TTL vs MOS GROWTH

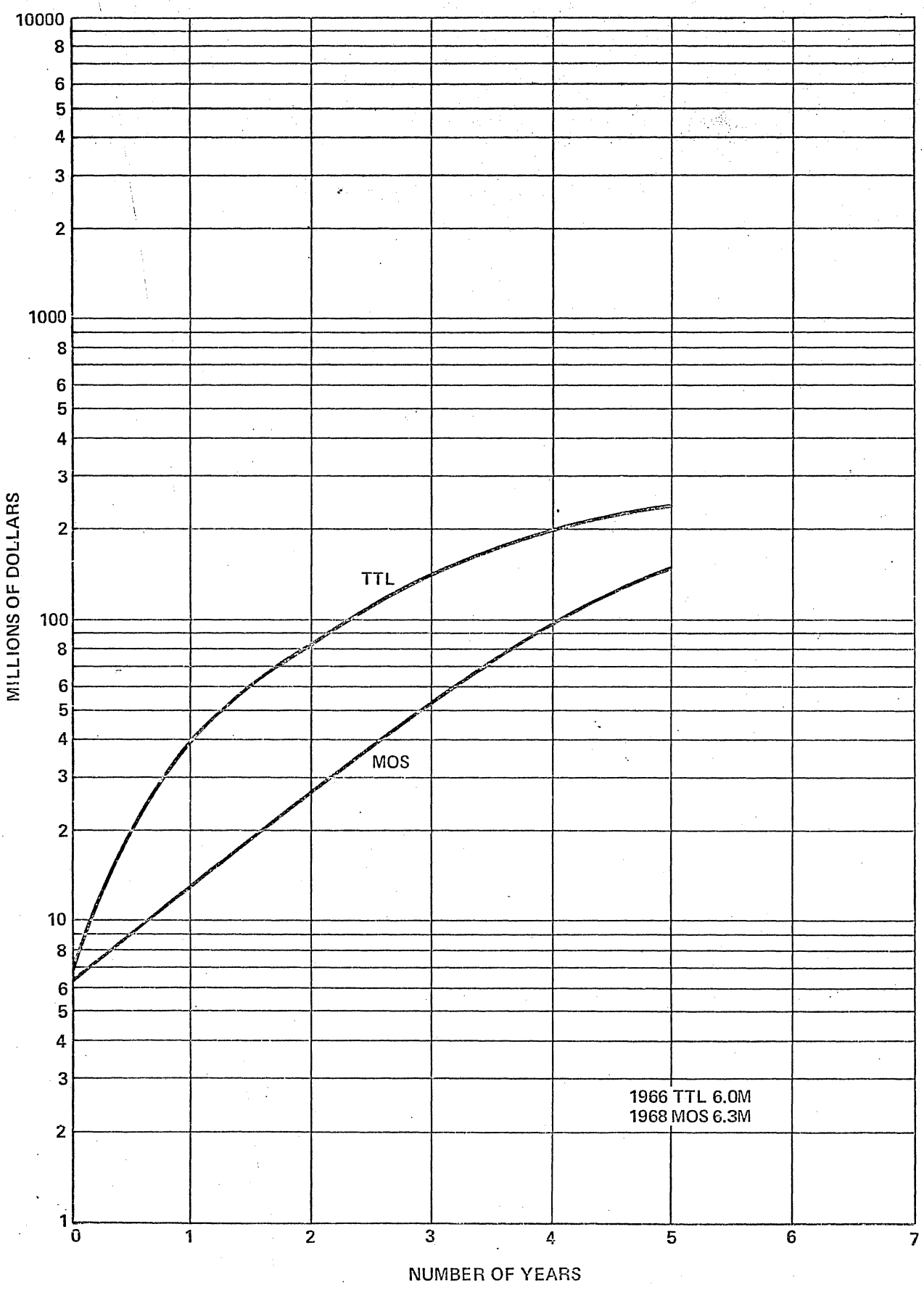
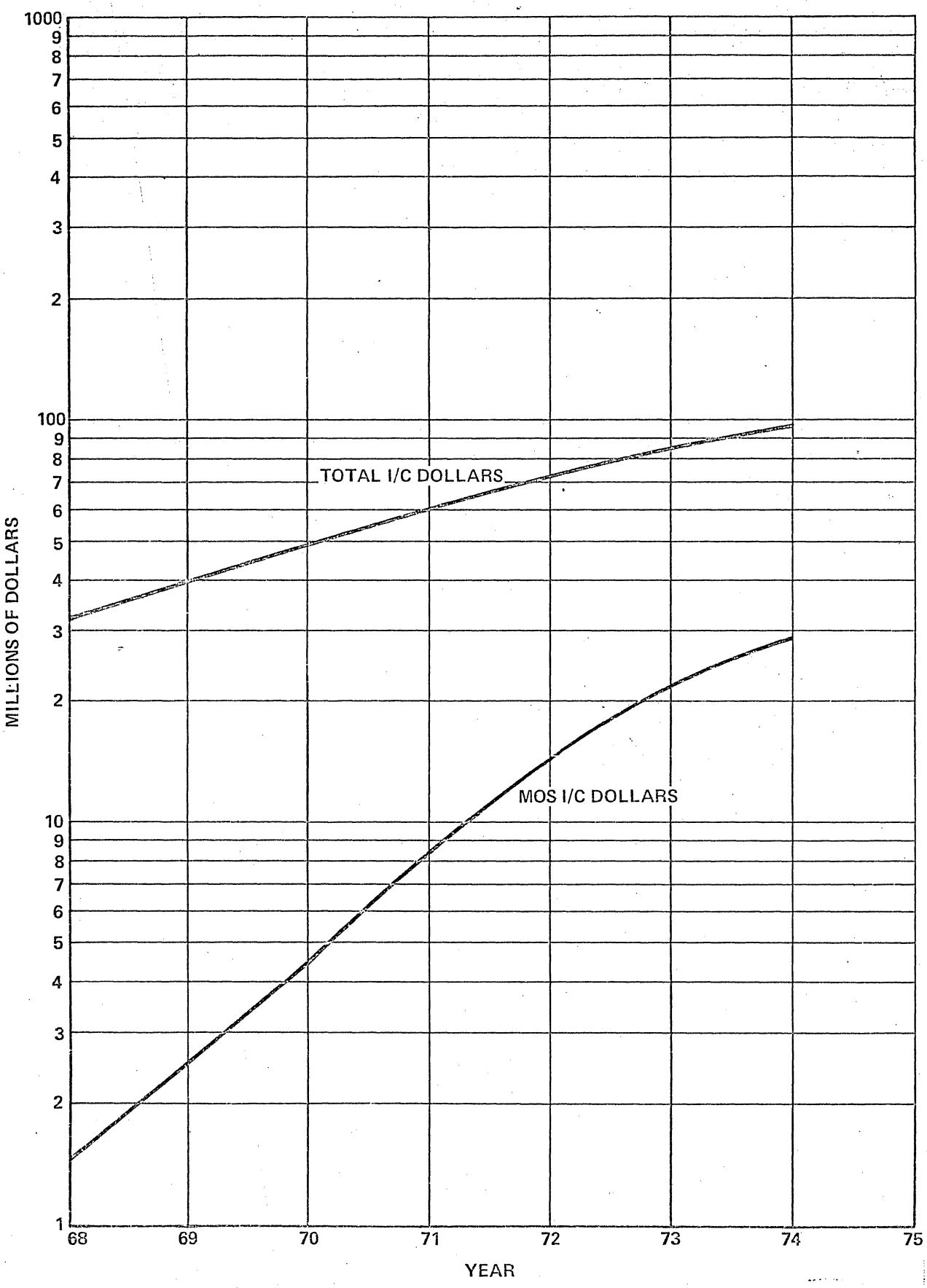


FIGURE 1.5

MOS I/C vs TOTAL I/C DOLLARS



ESTIMATED 1970 MOS INTEGRATED CIRCUITS

END USE APPLICATIONS

EIA REPORTED	
Consumer	71,000
Industrial	12,907,000
Government	3,945,000
Distributor	7,350,000
Export	4,727,000
TOTAL EIA REPORTED	29,000,000
NON EIA REPORTED	
Internal	1,600,000
Industrial	5,979,000
Military	4,392,000
Export	4,029,000
TOTAL NON EIA REPORTED	16,000,000
GRAND TOTAL MOS 1970	45,000,000

Figure 1.6

MOS Applications

The high density, low cost and low power dissipation of MOS makes it an ideal candidate for digital applications where its lower speed is acceptable. In the area of standard products, MOS is well suited for shift registers in the DC to 5Mc speed range. MOS shift registers find wide applications in the areas of serial memories in CRT display systems, disk and drum replacements, and in desk calculators. MOS Random Access Memories (RAM) will replace cores in main-frame memory applications where access times of greater than 150 ns are acceptable and volatility can be tolerated. Read-Only Memories (ROM) find wide application as character generators, and they replace random logic in many applications, such as desk calculators and mini-computers.

Another application where MOS performs well is as coder and decoder in digital multiplex (MUK) systems and also in multichannel audio MUX systems.

The low costal MOS logic will open up new markets in areas such as traffic control systems, digital clocks, automatic meter-reading systems, security systems and many more.

The rapidly-growing CAD capability in the areas of logic simulation and automatic artwork generation will also greatly reduce design costs and open up markets for lower volume custom MOS.

CHAPTER II

THE MOS TRANSISTOR

Structure of the MOS Device

There are two types of MOS transistors: p-channel and n-channel. Figure 3.1 shows cross sectional views of both types, and also shows the circuit symbol for both types. The acronym MOS is an abbreviation for Metal-Oxide Semiconductor. As can be seen in Figure 3.1, the gate metal, the thin oxide under the gate metal and the semiconductor substrate form a metal-oxide-semiconductor sandwich, hence the acronym MOS.

The source and drain are formed by making diffusions into the substrate. The thin oxide under the gate metal is formed by processes described in the following chapter. Metal contacts can be used to contact the source and drain diffusions. When the proper voltage is put on the gate electrode the region under the thin oxide inverts, that is, the field across the gate oxide causes the substrate material close to the oxide-silicon interface to change type, so that majority carriers can flow between the source and the drain terminals. The region under the oxide of a device which in on is called the Channel.

It should be noticed that the MOS transistor is self-isolating. That means that many transistors can be built on a single substrate with no isolation diffusions, which are required for bipolar integrated circuits.

Qualitative Description of MOS Transistor Operation

The source is roughly analogous to the emitter of a bipolar transistor or the cathode of a vacuum tube, the gate is analogous to the base or grid, and the drain is somewhat analogous to the collector or plate.

Most of the MOS integrated circuits made by the industry so far are p-channel because they have been more easily manufactured. In the future n-channel MOS circuits will become important also. However, in this chapter the operation of the MOS transistor will be explained for the p-channel device. The operation of the n-channel device is entirely analogous.

Figure 3.2 shows the drain characteristics of a typical p-channel enhancement mode MOS transistor. (Enhancement mode means that when $V_{GS} = 0$, the device is off and $I_{DS} = 0$.) It is helpful to keep the general appearance of the curves in Figure 3.2 in mind as the operation of the MOSFET is discussed. The drain family shows that the MOSFET is turned on harder as the gate is made more negative with respect to the source. It also shows that as the drain voltage gets larger in magnitude, the drain characteristic curves tend to flatten out. (The value of gate to source voltage V_{GS} at which conduction begins is designated V_{TO}, the threshold voltage. The subscript letter "0" indicates that the source and substrate are the same potential.)

The region where the curves tend to flatten out is called the current saturation region. The region for smaller values of V_{DS}, where a given curve has increasing slope is called the triode region.

As indicated in Figure 3.2, there are two "on" regions of operation for a MOSFET: the ohmic region, and the current saturation region. It may be helpful to remember that in the ohmic region, the MOS transistor can be considered to be a voltage controlled resistance, while in the current saturation region it can be considered a voltage controlled current limiter. This is apparent from Figure 3.3 by noticing that in the ohmic region the slope changes with V_{GS}, while in the current saturation region the current is fairly constant for a given value of V_{GS}.

When the device is off, the p-type source, the n-type substrate and the p-type drain form back-to-back diodes, and only the diode reverse leakage current can flow from source to drain.

The input resistance of the MOS transistor is very high (about 10^{12} ohms) because of course no DC current can flow into the gate terminal.

It should be observed that the device is symetrical; that is, either p-type diffusion could be the source and either could be the drain. Thus the device is a bilateral switch.

When a p-channel is formed by the presence of a sufficiently negative gate-to-source voltage, it should be noticed that holes, which are majority carriers, flow from source to drain. (For an n-channel device, electrons are the majority carriers.)

Regions Under the Gate Oxide

Figure 3.3 shows the regions near the gate oxide-silicon interface for several conditions of gate bias. The charges involved in each of the cases are identified and explained. The charges used in this explanation are defined below:

Q_G - Charge on the gate

Q_{SS} - Surface-state charge. Q_{SS} is the lumped effect of silicon surface states, oxide traps, interface energy states, and ionic centers within the oxide.

Q_D - Charge in the depletion region (defined in Figure 3.3b) are all at zero potential. Under these conditions the region under the gate oxide is called the accumulation region. The gate metal-oxide-silicon n-type substrate configuration can be considered to form a parallel plate capacitor. There is no charge on the gate metal ($Q_G = 0$) in this case. However, Q_{SS} is a distribution of positive charge assumed to be located very close to the oxide-silicon interface, and attracts an equal amount of negative charge in the form of mobile electrons which migrate from the bulk of the n-type substrate. These accumulate to form a conducting layer at the silicon side of the oxide-silicon interface. In the accumulation region, the gate capacitance per unit area is essentially the same as that of a parallel plate capacitor with oxide dielectric of thickness t_{ox}.

Figure 3.3b illustrates the region under the gate oxide for the case when a small negative voltage of magnitude E (less than the threshold voltage V_{TO}) is put on the gate. The region is then called the depletion region, because the negative charge on the gate creates a field in the region under the gate which sweeps the mobile electrons away and depletes the region of mobile carriers. The semiconductor material within the depletion region acts essentially as an insulator due to the absence of mobile charge carriers. The gate capacitance is approximately that of a parallel plate capacitor of thickness equal to the sum of oxide thickness and the distance that the depletion region extends into the substrate.

Figure 3.3c illustrates the case when a negative voltage larger in magnitude than the threshold voltage is put on the gate. The threshold voltage is the voltage at which inversion of the silicon at the silicon-oxide interface begins to occur, forming a p-type channel. As the gate voltage becomes still more negative, the amount of inversion increases, the number of mobile holes forming the channel increases, and the conductivity of the channel increases. As can be inferred from Figure 3.3c, the gate capacitance is again approximately that of a parallel plate capacitor with plates separated by the thickness of the gate oxide.

Figure 3.3d shows how the gate capacitance varies as a function of gate voltage.

Figure 3.4 shows the band diagrams and corresponding charge distributions for the accumulation, depletion and inversion regions.

Turn-On Voltage or Threshold Voltage

Strictly speaking the surface becomes inverted when the minority carrier concentration at the surface equals the majority carrier at the surface, i.e., $N_S = P_S = N_I$. However, this is not a useful measure of inversion because the corresponding charge of minority carriers is very small and the current is immeasurably small.

Strong inversion is defined to be the point at which N_S (the minority carrier concentration of holes near the surface) equals N_A, the impurity concentration of the substrate. Under these conditions, the total band-bending at the onset of strong inversion will be $\phi_s(inv) = 2\phi_F$.

Once an inversion layer is formed, the width of the surface depletion region reaches a maximum because once the bands are bent up far enough for strong inversion, even a very small increase in band bending, corresponding to a very small decrease in depletion region width will result in a very large increase in the change in the inversion layer.

Capacitance-Voltage Characteristics of the MOS Structure

Assume that a negative voltage is applied to the gate of an MOS device. This applied voltage will appear partly across the oxide

and partly across the silicon, i.e.

$$(a)\quad V_G = V_O + \phi_S$$

where

V_O is the portion across the oxide and ϕ_S is the potential variation across the depletion region of the semiconductor substrate. The electric field in the oxide is

$$(b)\quad \mathcal{E}_O = \frac{V_O}{X_O}$$

The electric field at the silicon surface is

$$(c)\quad \mathcal{E}_S = \frac{Q_S}{K_S}$$

where

Q_S is the charge induced at the surface (Gauss' Law).

Gauss' Law requires that the electric displacement be continuous at the oxide silicon interface, so that

$$(d)\quad K_O \mathcal{E}_O = K_S \mathcal{E}_S$$

at the interface.

Combining equations (b), (c), and (d) yields

$$(e)\quad V_O = \frac{X_O}{K_O \epsilon_O} Q_S = \frac{-Q_S}{C_O}$$

for the voltage drop across the oxide, where $C_O = \frac{K_S \epsilon_O}{X_O}$.

Then $(f)\quad V_G = \frac{-Q_S}{C_O} + \phi_S$ is obtained by substituting (e) in (a).

The simplest measurable electrical characteristic of an MOS structure is the small-signal capacitance, which is

$$(g)\quad C = \frac{dQ_G}{dV_G} = \frac{-dQ_S}{dV_G} = \frac{-dQ_S}{\frac{-dQ_S}{C_O} + dQ_S} = \frac{1}{\frac{1}{C_O} + \frac{1}{C_S}}$$

where

$$C_S = \frac{-dQ_S}{dQ_S} = \frac{K_S \epsilon_O}{X_d}$$

X_d is the width of the depletion layer in the silicon, and is given by

$$(h)\quad X_d = \sqrt{\frac{2K_S \epsilon_0 \phi_S}{qN_A}}$$

By substituting (h) in (g) we get the following formula for the capacitance of an MOS device in the depletion region.

$$(i)\quad C = \frac{C_O}{\sqrt{\frac{1 + 2K_O{}^2 \epsilon_0}{qN_A K_S X_O{}^2}}} \qquad V_G \text{ (depletion region)}$$

It must be emphasized that this formula only holds while the surface is being depleted.

When the device is in the accumulation region the capacitance is C_O. When it is in the depletion region it is given by (i). When strong inversion sets in,

$$V_G = \frac{-Q_B}{C_O} + \phi_S \text{ (inv)} = V_{TO}.$$

In the inversion region the value of C levels off to the value obtained when $V_G = V_{TO}$ is substituted into (i).

Figure 3.5 shows the C-V plot for the MOS structure at high frequencies. At low frequencies, the recombination-generation rates can keep up with the small signal variation, causing the incremental charge change to appear at the interface rather than at the edge of the depletion region. See Grove's "Physics and Technology of Semiconductor Devices" page 274 for an explanation of this. Figure 3.6 shows the C-V plot of the MOS structure for various frequencies.

The Physical Constants and Parameters in the MOS Current-Voltage Equation

A chapter comparing several MOS device models is presented later in this manual. The following list of equations presents one of these models for the purpose of explaining the effect of the various quantities that affect the current-voltage relationship for a p-channel MOS transistor.

1) Channel current in ohmic or linear region

$$I_D = \left(\frac{Z}{L}\right)\mu_p C_O \left\{V_{GS} - V_T - V_{DS}\right\} V_{DS}$$

$$-\frac{2}{3}\frac{2K_S \epsilon_O q N_D}{C_O}\left\{\left|V_{DS} + V_{SB} + 2\phi_F\right|^{\frac{3}{2}} - \left|V_{SB} + 2\phi_F\right|^{\frac{3}{2}}\right\}$$

2) Threshold Voltage

$$V_T = V_{TO} \sqrt{\frac{2K_S \epsilon_O q N_D + \left|2\phi_F + V_{SB}\right|}{C_O}} + \sqrt{\frac{2K_S \epsilon_O q N_D - \left|2\phi_F\right|}{C_O}}$$

3) Zero Bias Threshold Voltage

$$V_{TO} = V_{FB} + \phi_S - \sqrt{\frac{2K_S \epsilon_O q N_D - \left|\phi_S\right|}{C_O}}$$

4) Gate Capacitance

$$C_O = \frac{K_O \epsilon_O}{t_o}$$

5) Surface Mobility

$$\mu_p = K\mu_{bulk}$$

6) $\mu_p C_O = \beta$

Each of the quantities in equation (1), beginning on the left will be described, some of them with reference to equations (2), (3), (4), and (5).

a) Z = effective channel width. $Z = Z_{drawn}$ -2 (overetch). (Perpendicular to direction of flow of I_{DS}.)

b) L = channel length. $L = L_{drawn}$ -2 (out-diffusion). (In the same direction as I_{DS}.)

c) μp = surface hole mobility. $\mu p = K \mu bulk$, where K is a factor that relates bulk mobility and is a function of the applied voltage across the oxide. In other words, surface mobility is degraded by applied gate voltage. Mobility decreases as N_D increases, and is higher for ⟨111⟩ material than for ⟨100⟩ material.

d) C_O = Gate capacitance = $\frac{K_O \epsilon_O}{t_o}$. Gate capacitance is directly proportional to dielectric constant of the insulator, and inversely proportional to its thickness.

e) $\beta = \mu p C_O$ = gain parameter.

f) V_{GS} = gate to source voltage

g) V_T = threshold voltage, the point at which strong inversion occurs. The threshold voltage increases as the source-to-bulk voltage V_{SB} increases. This phenomenon is called Body Effect. Also, V_T increases as oxide thickness decreases. ϕ_F is the Fermi potential given by

$$\phi_F = \frac{kT}{q} \ln \frac{N_D}{n_i}$$

h) V_{DS} = source-to-drain applied voltage

i) K_S = dielectric constant of silicon; K_O = dielectric constant of the insulator.

j) N_D = impurity concentration of the substrate.

The following table shows how increasing various processing parameters affect device characteristics.

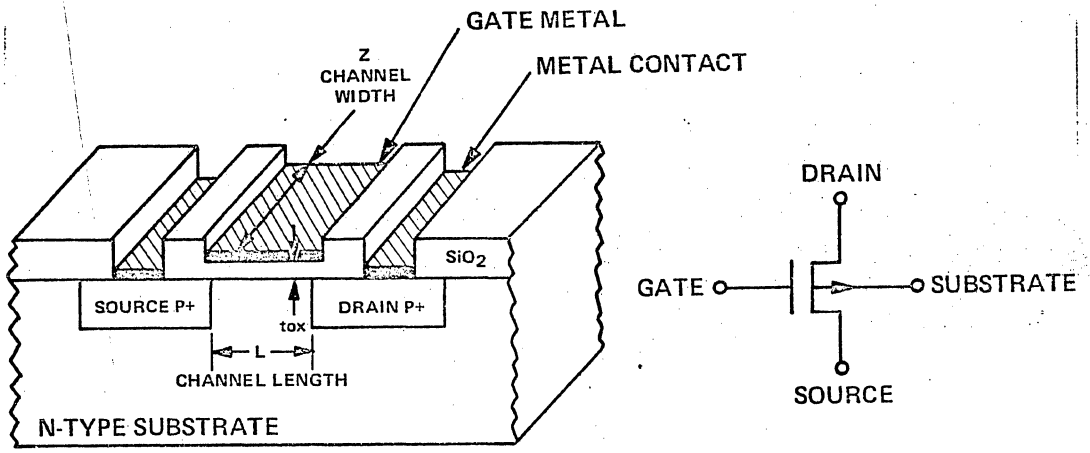
1) N_D (substrate impurity concentration)
   a) decreases channel length modulation, or increases punch-through voltage
   b) increases V_{TO}
   c) increases body effect
   d) decreases mobility μp, and therefore decreases β
2) t_o (oxide or insulator thickness)
   a) decreases C_O, and therefore decreases β

3) K_0 (insulator dielectric constant)

a) increases C_0, and therefore increases β

FIGURE 3.1

CROSS SECTIONAL VIEWS OF P—CHANNEL AND N—CHANNEL MOSFETS AND CIRCUIT SYMBOLS



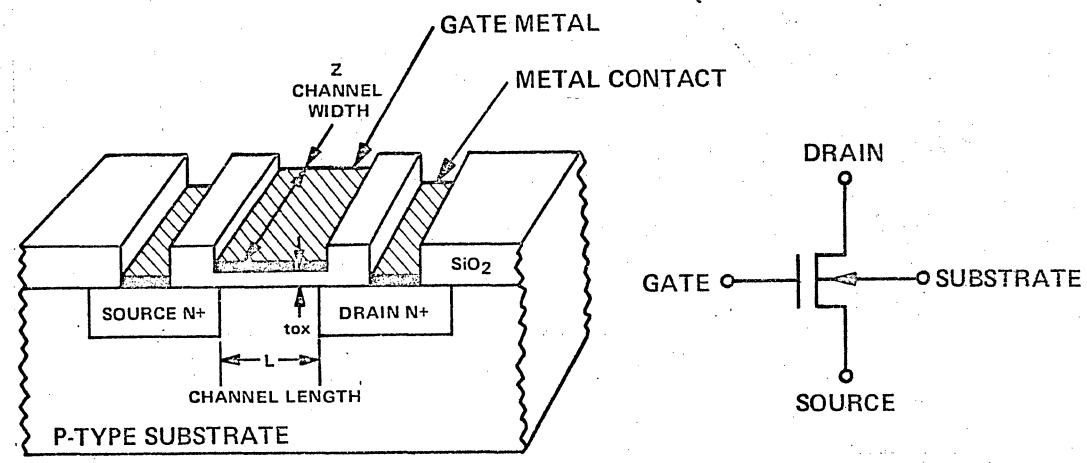


FIGURE 3.2

FOR MOS P—CHANNEL
DRAIN CURRENT CURVES

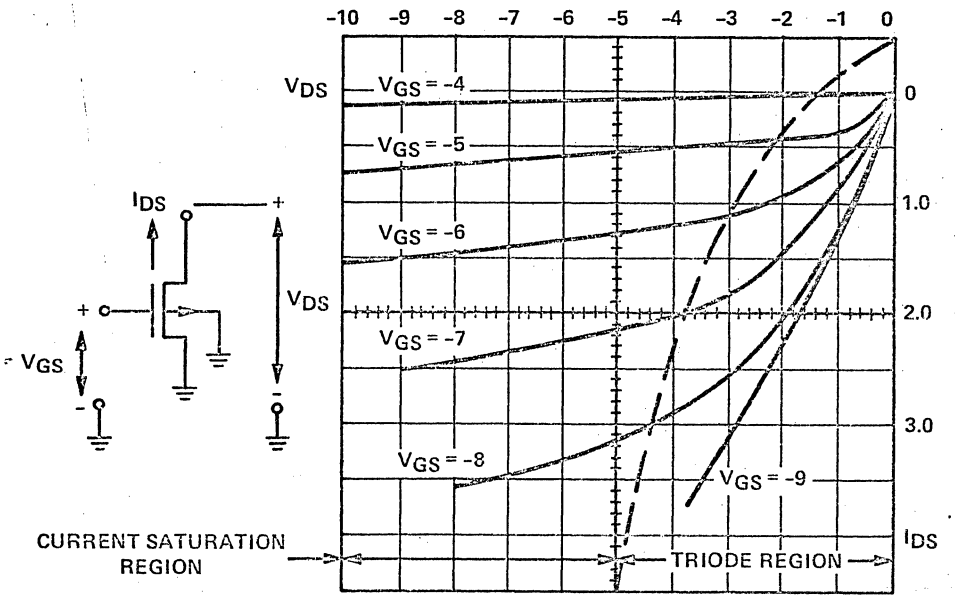


FIGURE 3.3

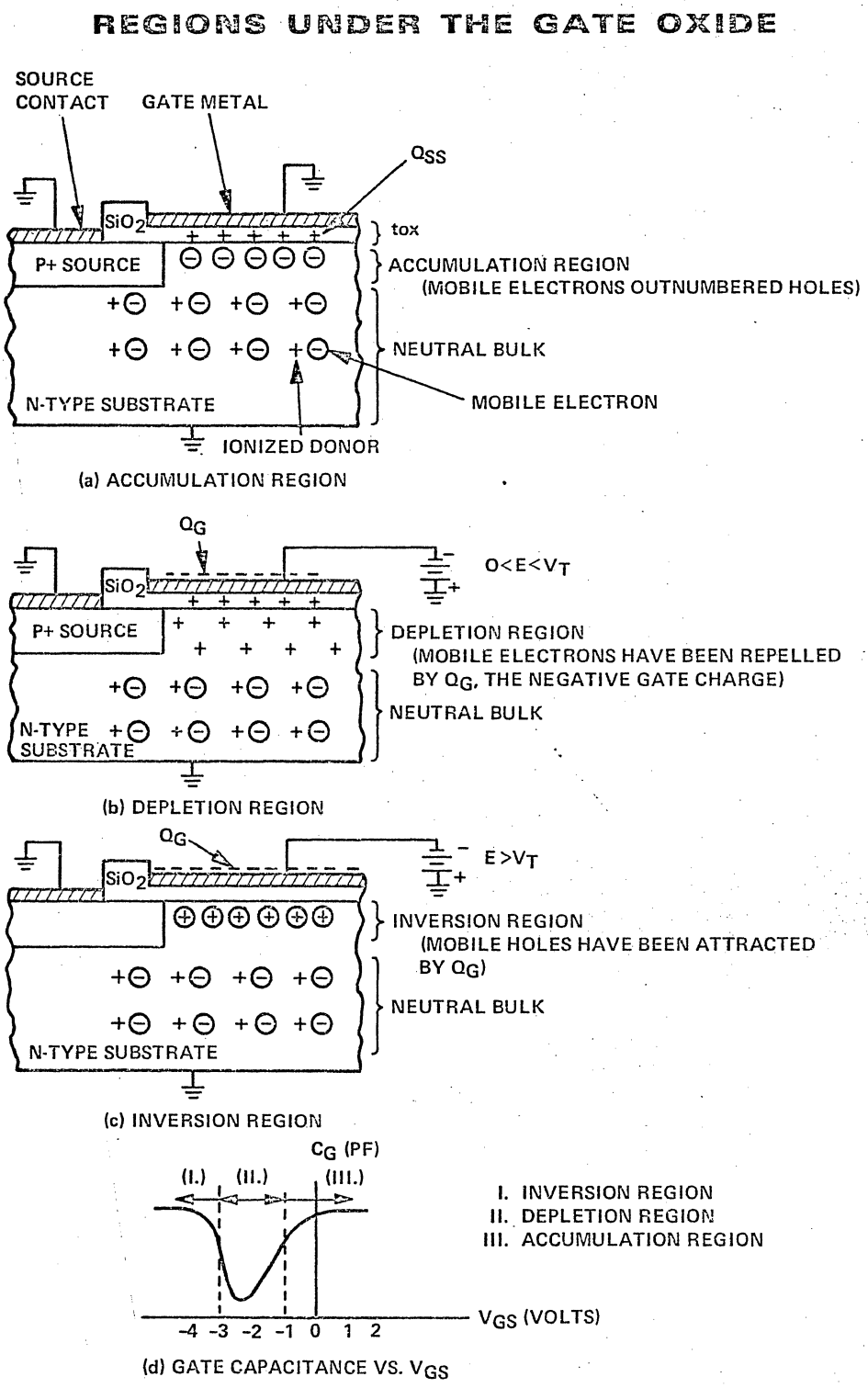
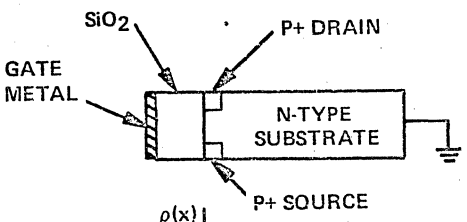

REGIONS UNDER THE GATE OXIDE
SOURCE CONTACT
GATE METAL
Q_{SS}
SiO_2
tox
P+ SOURCE
ACCUMULATION REGION
(MOBILE ELECTRONS OUTNUMBERED HOLES)
NEUTRAL BULK
N-TYPE SUBSTRATE
MOBILE ELECTRON
IONIZED DONOR
(a) ACCUMULATION REGION
Q_G
$O<E<V_T$
DEPLETION REGION
(MOBILE ELECTRONS HAVE BEEN REPELLED BY Q_G, THE NEGATIVE GATE CHARGE)
N-TYPE SUBSTRATE
(b) DEPLETION REGION
$E>V_T$
INVERSION REGION
(MOBILE HOLES HAVE BEEN ATTRACTED BY Q_G)
(c) INVERSION REGION
C_G (PF)
(I.) (II.) (III.)
I. INVERSION REGION
II. DEPLETION REGION
III. ACCUMULATION REGION
V_{GS} (VOLTS)
-4 -3 -2 -1 0 1 2
(d) GATE CAPACITANCE VS. V_{GS}

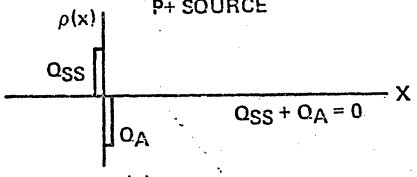
FIGURE 3.4-a

CHARGE DENSITY DISTRIBUTIONS FOR REGIONS UNDER THE GATE OXIDE

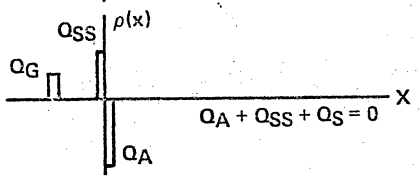
DEFINITIONS OF CHARGES

Q_G – CHARGE ON THE GATE.
Q_{SS} – SURFACE-STATE CHARGE.
(THE EFFECTS OF SILICON SURFACE STATES, OXIDE TRAPS, INTERFACE ENERGY STATES, AND IONIC CENTERS WITHIN THE OXIDE ARE ALL LUMPED TOGETHER TO FORM Q_{SS})
Q_D – CHARGE IN THE DEPLETION REGION.
Q_A – CHARGE IN THE ACCUMULATION REGION.
Q_I – CHARGE IN THE INVERSION REGION.

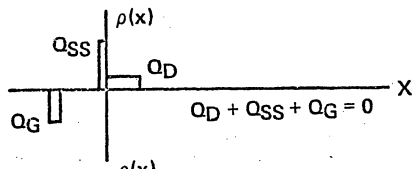




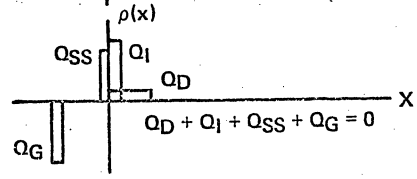
DUE TO SURFACE STATES



DUE TO SURFACE STATES IN ADDITION TO POSITIVE APPLIED GATE VOLTAGE



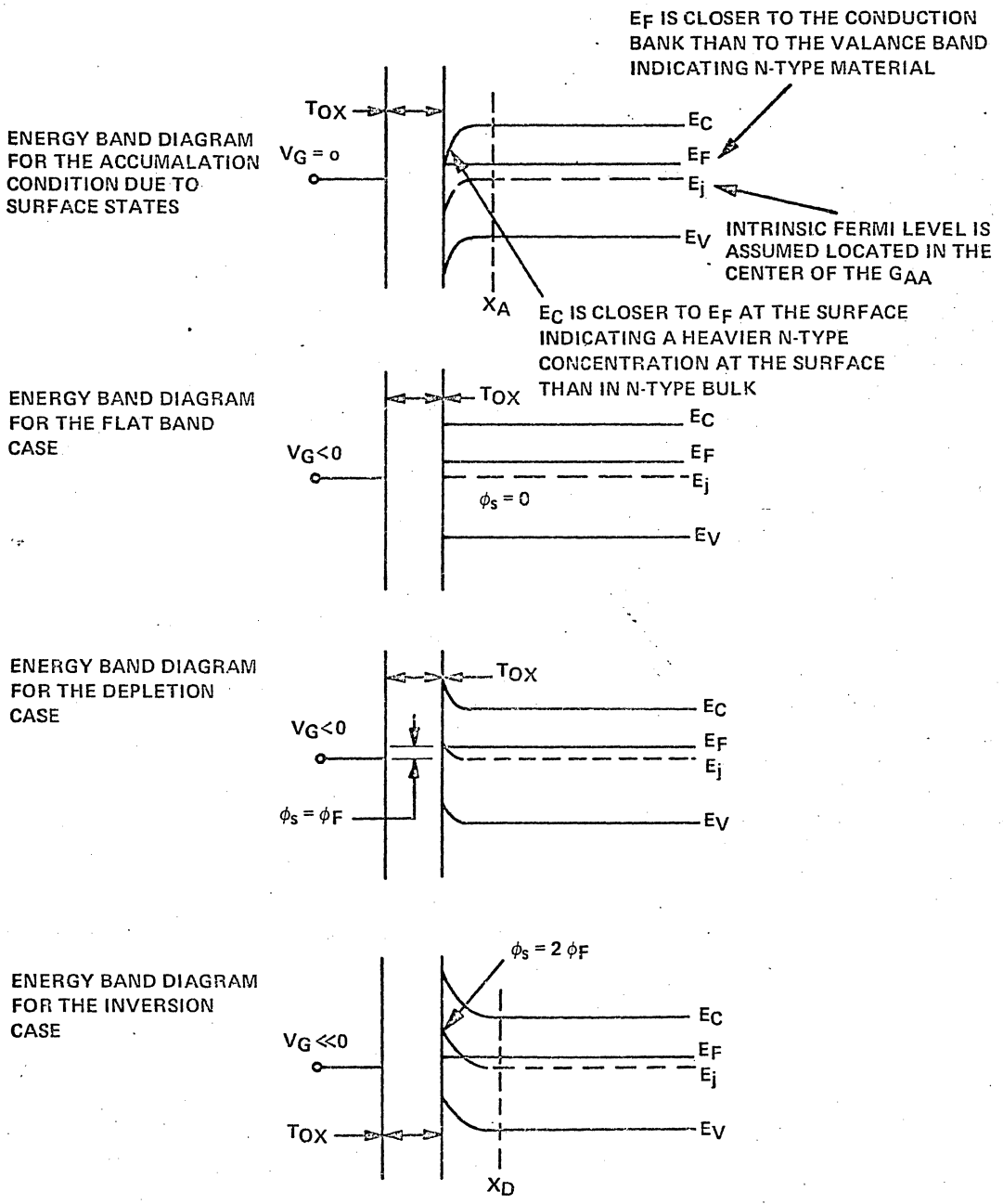
FOR THE DEPLETION REGION



FOR THE INVERSION REGION

FIGURE 3.4-6

BAND DIAGRAMS FOR P—CHANNEL MOS DEVICE



CHAPTER III

General Introduction to Processing

Due to many possible variations in processing technique a brief reminder of a standard PMOS thick field oxide process is presented. The starting material is normally phosphorus doped <111> orientation single crystal silicon whose resistivity lies in the range of 1 to 20 Ω-cm. For a cross-sectional reference consult Figure I "MOSIC Process 'B'" while proceeding through the following steps.

1. Oxidation: A passivating layer of silicon dioxide is grown on the surface of a polished and clean silicon substrate in a high temperature oxygen ambient. This oxide layer protects the silicon surface from unwanted impurities and renders the surface electrically less active to undesirable surface conduction.
2. Photo-masking: Source, Drain, and "Crossunder" Pattern Delineation: Through a series of photo-masking operations, discrete patterned regions are defined in which oxide is removed and the underlying silicon is exposed. Some exposed areas of silicon will ultimately be the diffused source and drain elements of the MOS-FET. Other diffused regions will be used as interconnection tunnels crossing under other metal interconnections.
3. Dopant Impurity Deposition: The silicon substrates are introduced into an atmosphere of some impurity dopant at an elevated temperature. The impurity atoms diffuse in the silicon in the discrete patterned regions where oxide has been removed. The remaining oxide acts as a barrier to prevent shorts between the discrete devices.

4. Drive-in and Oxidation: The high temperature furnace operation causes the prior diffused dopant impurities to penetrate the silicon even deeper. During this operation, the source and drain regions are diffused toward one another laterally, to a specified separation. This separation is critical as related to the electrical characteristics of the device. During this operation, an oxide layer is also grown over the diffused regions to passivate and protect the surface. An alternative method is to remove all the oxide used for diffusion masking and to deposit a thick uniform layer.

5. Photo-masking: Gate Delination: Photo-masking techniques are again used to remove or decrease the oxide thickness in the gate region. The oxide that remains can be used for the final gate oxide thickness or additional oxide can be grown. In either case, the oxide thickness is critical since this thickness is inversely a measure of the voltage required to cause electrical conduction from source to drain.

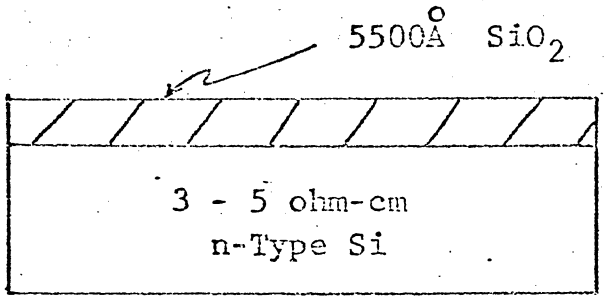
6. Gate Oxide Regrowth: If additional oxide is required in the gate channel region, the silicon substrates are again introduced into a high temperature oxidizing (oxygen) atmosphere.

7. Photo-masking; Diffused Region Contact "Windows": As a result of this photo-masking operation, oxide is removed in small areas over the diffused regions (source, drain, crossunders) to allow mechanical and electrical contact to these regions.

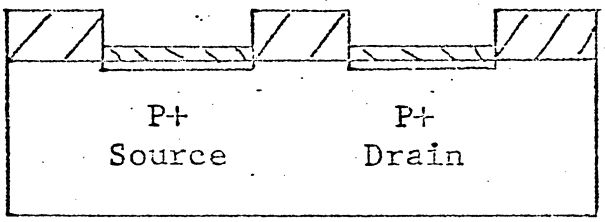
MOSIC Process "B"

I. Starting Material

3 - 5 ohm-cm
n-Type C_Z Si



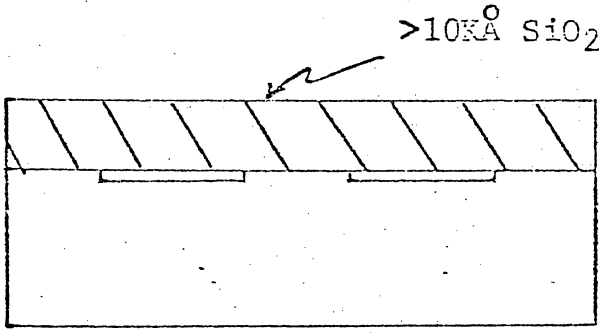
II. Source-Drain Deposition
& Re-oxidation



III. Thick Oxide Deposition

(Initial oxide stripped and regrown or thinned to ~ 2000Å)

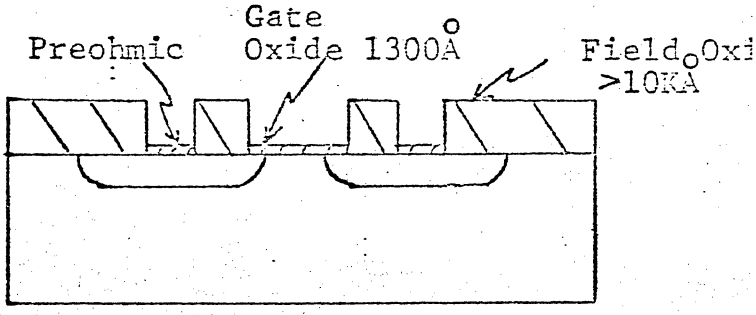
>10KÅ oxide deposited



IV. Gate & Contact Definition and Oxidation.

ρ_s (Boron) = 75 ± 25 ohms/sq

X_j (Boron) = 3.1μ



V. Metallization & Lead Pattern Definition

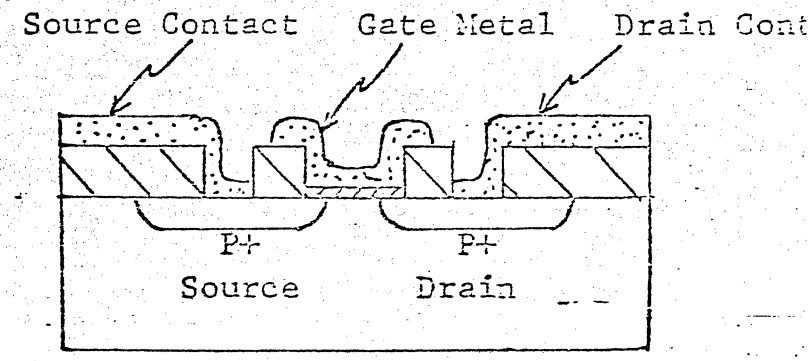


FIGURE I

5-26-69

8. Metal Deposition: A thin film of metal, commonly aluminum, is deposited over the entire patterned surface of the silicon substrate.

9. Photo-masking; Metal Interconnect Delineation: A pattern is now defined in the metal, to interconnect all discrete MOS-FET's and crossunders, thereby forming a specified circuit. All other metal is removed.

10. Alloy: This is a low temperature furnace operation which bonds the aluminum to the silicon in the diffused regions. This is performed to assure a low resistance electrical contact between the aluminum and the silicon.

Silicon gate PMOS processing technique is now coming into importance. It features the advantages of a lower threshold voltage ($\sim$2 volts on $\langle 111 \rangle$) and a self alignment which reduces stray gate capacitances. The starting material is similar to that of regular PMOS. Figure 2 gives a cross-section of this process.

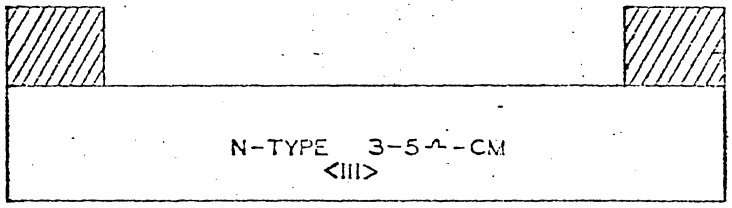
1) Oxidation: Passivation layer of SiO_2 is either thermally grown or deposited on a clean polished silicon surface. This layer serves as an insulating medium in the finished structure as well as a diffusion mark during processing.

2) Source-Drain Cut: Photolithographic techniques are used to remove all oxide from the surface over source, drain and gate areas as well as regions where a diffused cross-under is desired.

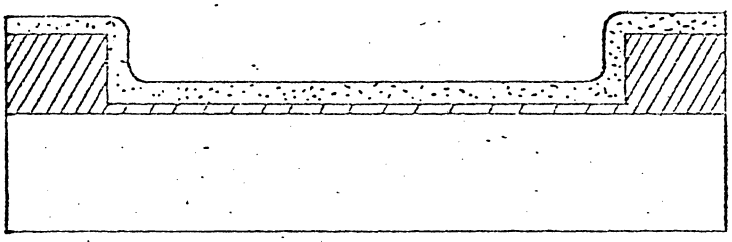
3) Gate growth and poly deposition: The gate insulator is thermally grown in bare regions and a layer of poly crystalline silicon is deposited over the entire wafer.

MOS/IC SILICON GATE PROCESS

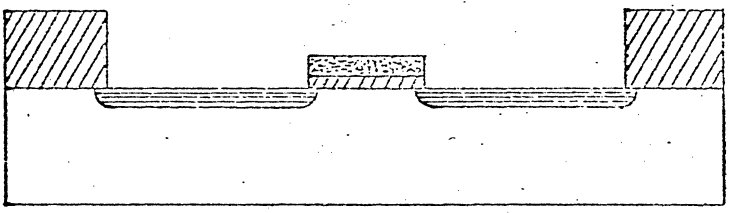
1. INITIAL OXIDATION AND SOURCE-DRAIN PHOTORIST



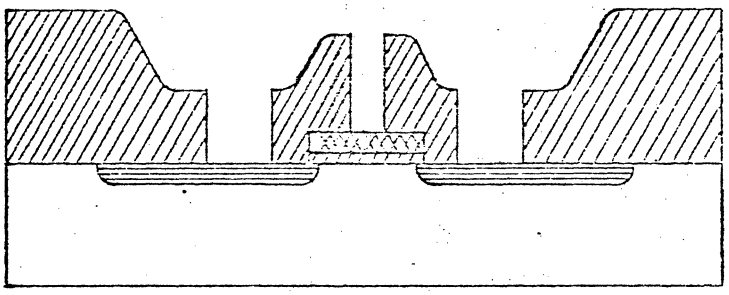
2. GATE OXIDATION AND POLYCRYSTALLINE SILICON DEPOSITION



3. POLY DEFINITION AND P+ DIFFUSION



4. OXIDE DEPOSITION AND CONTACT PHOTORESIST



5. METAL DEPOSITION AND DEFINITION

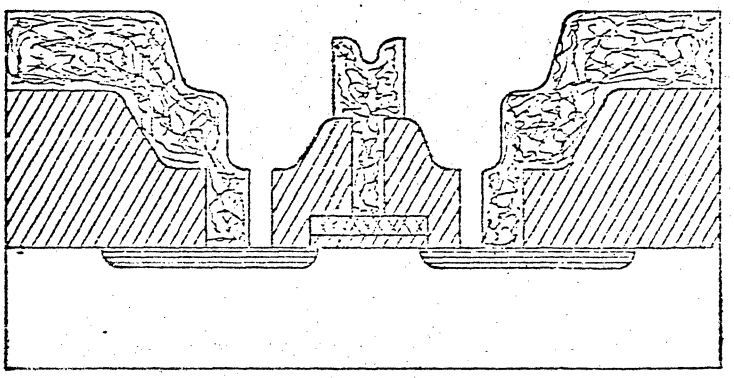


FIGURE II

4) Gate Cut: The poly silicon is removed from the surface in all areas except the gate areas and poly silicon cross unders. Following this step the surface is etched to remove oxide in regions cleaned in step two but not covered by poly silicon.

5) Source Drain Diffusion: The wafer is introduced into a non-oxidizing diffusion ambient and p regions are formed in the exposed poly silicon and single crystal areas. Following the diffusion an additional passivation layer of SiO_2 is deposited on the wafer.

6) Preohmic Cut: Small contact areas to Source, drain, diffused cross unders, poly silicon cross unders, etc. are formed by removing oxide using standard photolithographic techniques.

7) Metallization, passivation etc, formed as in standard process.

Though not currently available a complementary silicon gate fabrication is possible. One such processing scheme is presented in Table I and a cross-section of the finished part is given in Figure 3.

It should be readily apparent by now that many processing schemes are possible, each with a particular advantage. The following are some comments as to the properties of various modifications:

1) Alternate Insulator Structure: Both Al_2O_3 and Si_3N_4 have been used in gate insulators to increase gain as their dielectric constant is higher than that of oxide. Both can reduce thresholds as the effective thickness of the

insulator is reduced. The interface to bulk silicon of either insulator is of rather poor quality so a thin oxide layer is used between the silicon and Al_2O_3 or Si_3N_4. This technique can lead to an instability mechanism known as interfacial polarization. Al_2O_3 has an added property in that its interface with SiO_2 can be negatively charged thus affecting the threshold voltage.

2) Insulating Substrate: Single crystal silicon can be grown either on sapphire or spinel substrates. By using a thin layer of silicon ($\sim 2\mu$) and diffusing the drain regions completely through it, the drain substrate capacitance can be greatly reduced, thus increasing the frequency response. At present the mobility is lower than that of currently available bulk silicon.

3) Ion Implantation: Ion implantations can be used after metallization to dope regions of the substrate of either type. Thus a method of self alignment is possible to orient the drain junctions edge with the edge of the gate. This approach greatly reduces the gate drain capacitance (similar to that of silicon gate) and reduces the Miller effect. In addition very light-shallow doped regions are possible so that threshold voltages can be adjusted (eg. fabrication of a p depletion load device).

4) N channel devices: Higher gain can be achieved with n channel devices due to higher mobilities. This requires greater care than p-channel in processing cleanliness due to the ease of inverting the field.

5) Complementary MOS (CMOS): Fabrication of both n channel and p channel devices on the same chip gives some speed advantage and a tremendous power advantage over standard PMOS products. CMOS fabrication is roughly three times as complicated so yield is reduced and wafer cost is increased.

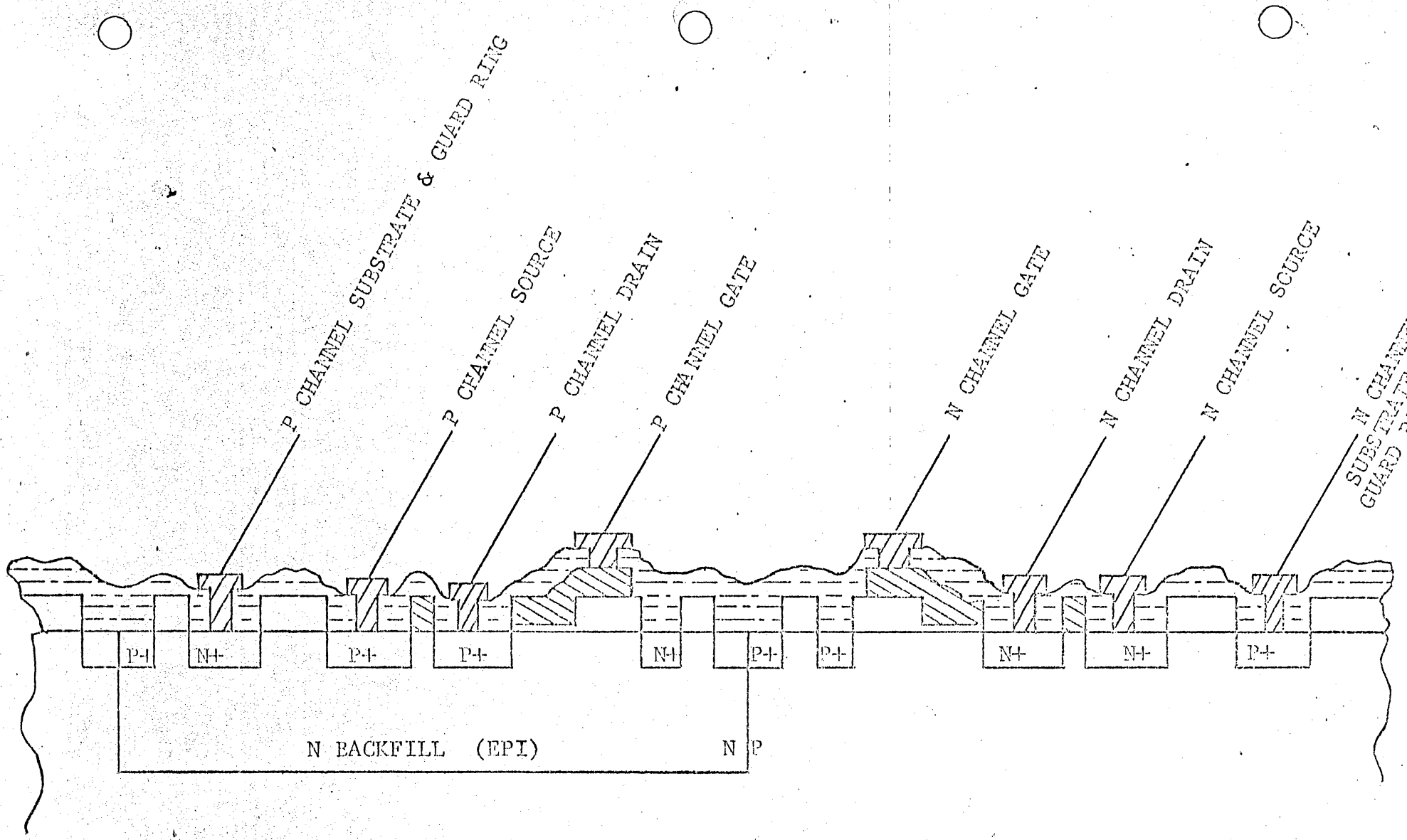
6) Bilpolar - MOS: Bipolar parts with their associated low input impedance and large current capability have many attractive features. Fabrication of both types of parts requires at least two diffusions and a greater degree of diffusion control than currently needed on MOS circuits.

7) Thin Film: MOSFETS can be fabricated on poly crystalline or amprphous thin films of semiconductor material deposited or insulating substrates. Advantages to this scheme include reduced substrate capacitances and complete high voltage isolation. Currently the quality of such devices is poor.

8) Field Inversion Control: It should be readily apparent that the region between active elements fulfills the requirements of an MOS device under metal interconnects. Two alternatives are available to prevent this parasitic behavior, either diffusing the substrate to a high level by area channel stopper diffusion or by increasing the oxide thickness in the field inversion voltage above that of any potential applied to the chip.

As indicated earlier wafer fabrication requires many independent operations and each step must be within limits if the finished devices or circuits are to function properly. During photoresist operations and others frequent checks are made to insure quality. Table III is a partial listing of checks made to insure that nothing has gone out of specification in wafer processing.

This introduction to wafer processing has admittedly been very brief. The outlines of various processes should give a qualitative outline of the major techniques currently in use as well as identify some of the properties of technologies which may become more important in the future.



Final Structure of Silicon Gate Complementary MOS Devices

METAL

POLY SILICON

OXIDE

Current PMOS Processes

Flow Sheet	Material	S-D Diffusion	N+ Diffusion	Field Oxide	Field Inversion	Bipolar Compatible	Threshold & Gain	Comments
AP01D	<100>	15 ± 5 Ω/□ 3.5μ	Yes	>10,000Å	>20 Volts		1.5-2.5V 2.5-4μA/V²	
AP02D	<100>	15 ± 5 Ω/□ 3.5μ	Yes	5,500Å	5-10 Volts		1.5-2.5V 2.5-4μA/V²	No Gold Backing
AP03D	<100>	15 ± 5 Ω/□ 3.5μ	Yes	5,500Å	5-10 Volts		1.5-2.5V 2.5-4μA/V²	
AP04D	<111>	75 ± 25 Ω/□ 2.5μ	Yes	>10,000Å	>30 Volts	Yes	3.5-4.5V 3-6μA/V²	
AP05D	<111>	75 ± 25 Ω/□ 2.5μ		>10,000Å	>30 Volts		3.5-4.5V 3-6μA/V²	
AP06D	<100>	15 ± 5 Ω/□ 4μ	Yes	5,500Å	5-10 Volts		1.5-2.5V 2.5-4μA/V²	
AP07D	<100>	75 ± 25 Ω/□ 2.5μ	Yes	>10,000Å	>20 Volts	Yes	1.5-2.5V 2.5-4μA/V²	
AP08D	<100>	75 ± 25 Ω/□ 2.5μ		>10,000Å	>20 Volts		1.5-2.5V 2.5-4μA/V²	

TABLE II

LOW THRESHOLD CMOS PROCESSING

1. P wafer with oxide.
2. Cut SiO_2 for n pots.
3. Etch and regrow n epi.
4. Polish back.
5. Clean and grow about 5K oxide.
6. Thick oxide cut--active device area, guard area, scribe grid.
7. Apply gate insulator and poly Si gates.
8. Pattern gates.
9. Deposit oxide.
10. Cut P washout--P channel S-D, grid, n channel guards and substrates.
11. P^+ diffusion.
12. Deposit oxide.
13. Cut N washout--N channel S-D, P channel guards and substrates.

13a. N+ diffusion.

14. Deposit thick oxide.
15. Cut pre-ohmic and scribe grid.
16. Metal.
17. Ohmic.
18. Deposit passivation SiO_2.
19. Cut P and apertures and grid.
20. Prepare back of wafer.

TABLE I

MOSIC PROCESS CONTROL OUTLINE

Control Point	Measurement	Frenquency
1. Incoming Material	(a)Resistivity (b)Orientation	(a)Rely on Materials QC (b)Each lot
2. Initial Oxidation	Thickness	Each lot by color
3. N^+ Deposition	Sheet resistance	Control wafer from each lot
4. P^+ Deposition	Sheet resistance	Control wafer from each lot
5. Oxide Deposition	Thickness	Control wafer from each lot
6. Gate Oxidation	(a)Thickness(color) (b)Contamination(CV plot)	(a)Control wafer from each lot (b)Sample test pattern on wafers from each lot
7. Source Drain Diffusion	(a)Sheet resistance (b)Junction depth	(a)Control wafer each lot (b)Occasional spot check
8. Metallization	(a)Thickness (b)Contamination(CV plot)	(a)&(b)Control wafer each lot
9. Test Probe	(a)V_T(1μamp) (b)Contamination(CV plot) (c)BVDSS(10μamp) (d)Field Inversion	All on each wafer except (b). (b)On two wafers from each lot.
10. Stress packaged (TO5) discrete devices	Same as 9 except for (b) and stress at 175°C, 16 hr ± 30V on gates	Spot check on in-process control
11. Packaged Circuits	Operating life	Periodic check by product engineers

TABLE III

JA

MOS LOGIC FAMILIES

The designer of an MOS system has at his disposal various methods in which to implement his logic equations. Depending upon performance and price specifications, he may choose from static logic, 2Ø logic, 4Ø logic, complimentary logic or a combination of the above.

Let us consider the basic logic elements used in MOS designs. The symbols, with their corresponding circuit diagram are negative logic since this is generally used in MOS. Figure 1 is the representation of an inverter. This device performs the complement of the input. That is, assuming a logic "0" input, the output is a logic "1". It's associated truth table is shown in Figure 2. Secondly, we have the NAND gate and it's associated circuitry in Figure 3. If a logic "1" is on both A and B, the output is a logic "0". For any other input, the output is a logic "1". This circuit is not often used with more than 3 inputs because of the cumulative series resistance of the switch devices. That is, assuming a device is a resistor, a 3 input NAND would require switch devices 3 times as large as an inverter switch. To eliminate this problem, MOS circuits are usually implemented using NOR logic where possible. A NOR gate is shown in Figure 4. This circuit, since all switch devices are parallel, has switch devices that are the same size as the inverter. For a NOR gate, if all inputs are a 0, the output is a 1. If any input is a one, the output is a zero. The devices can be stacked in parallel until the leakage current lowers the output voltage of the "1" level.

Another aspect of MOS is use of the functional gate. This reduces the number of load devices, thus reducing power, chip area, & improving speed. For example, suppose we wanted to implement the Boolean Function $F=\overline{AB+CD}$. The most straight-forward method is shown in Figure 5.

A	F
0	1
1	0

1 = 12V

0 = -1V

Figure 2

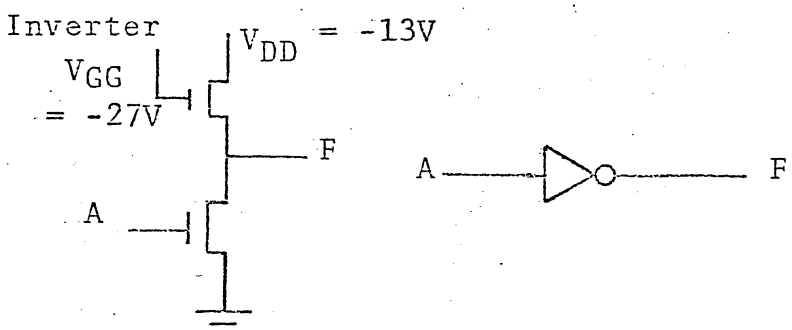
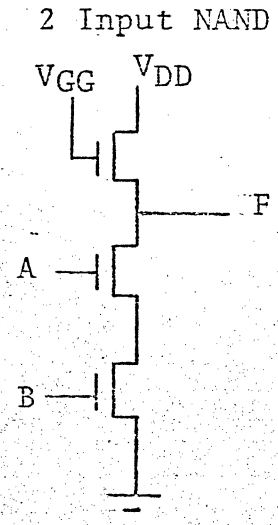


Figure 1

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



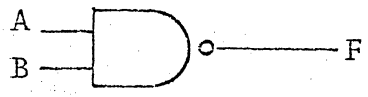
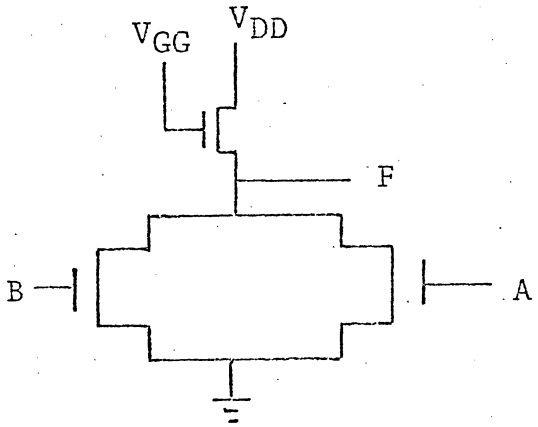


Figure 3

2 Input NOR

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0



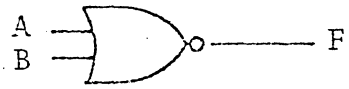


Figure 4

$F = \overline{AB + CD}$

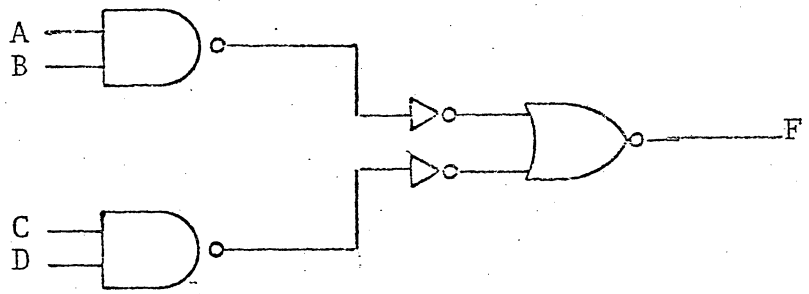
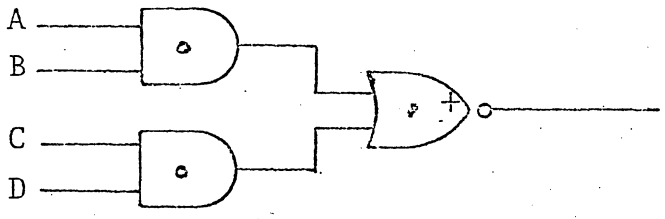


Figure 5

This circuit requires 13 devices, 5 of which are load resistors. In functional representation, the equation can be represented as shown in Figure 6.



$F = \overline{AB + CD}$

The Circuit is

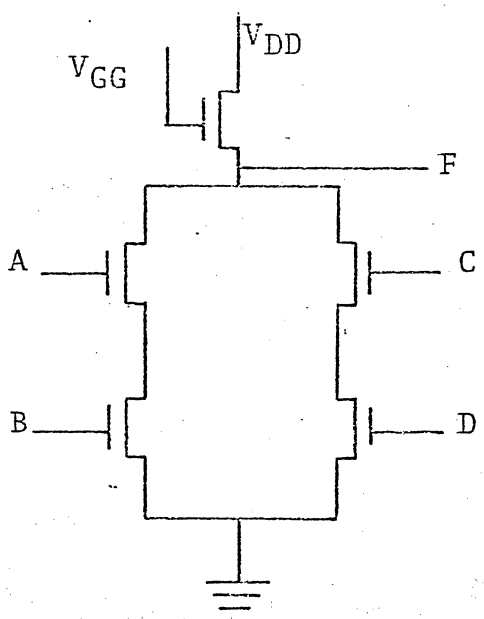


Figure 6

The use of the functional gate is limited only by the ingenuity of the designer.

Now that the basic logic blocks have been defined, consider the options available as far as implementation of MOS circuitry. First, is static or DC logic.

Static logic is the easiest of the options to implement. From Table 1, advantages and disadvantages of static logic are shown.

Advantages	Disadvantages
Easiest to Implement	High power consumption
Requries at most 1 clock	Large area required
Operates at DC	Potential Race problems difficult to eliminate

Characteristics

DC - 2 MHz

Requires 2 supplies

Table 1

From the circuit shown in Figure 7 it can be seen that when a switch device is 'ON', there is a current path to ground, through the load device. In addition, the voltage stored on the gate cap of the next device must be discharged through the switch device. This necessitates the use of a larger switch to accommodate the additional current.

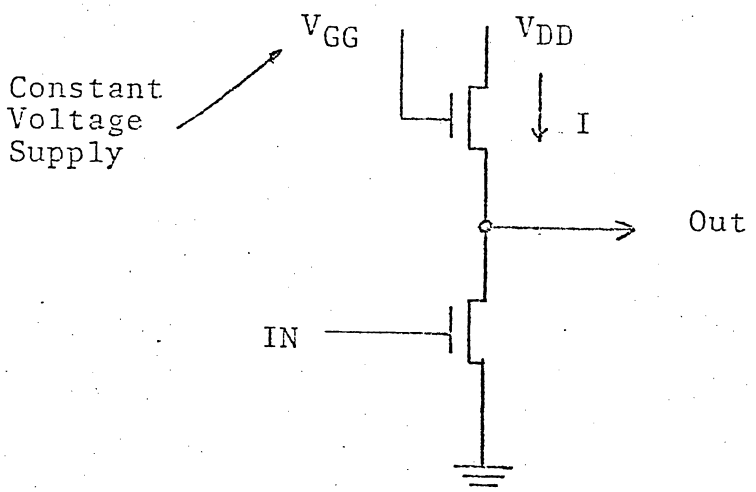
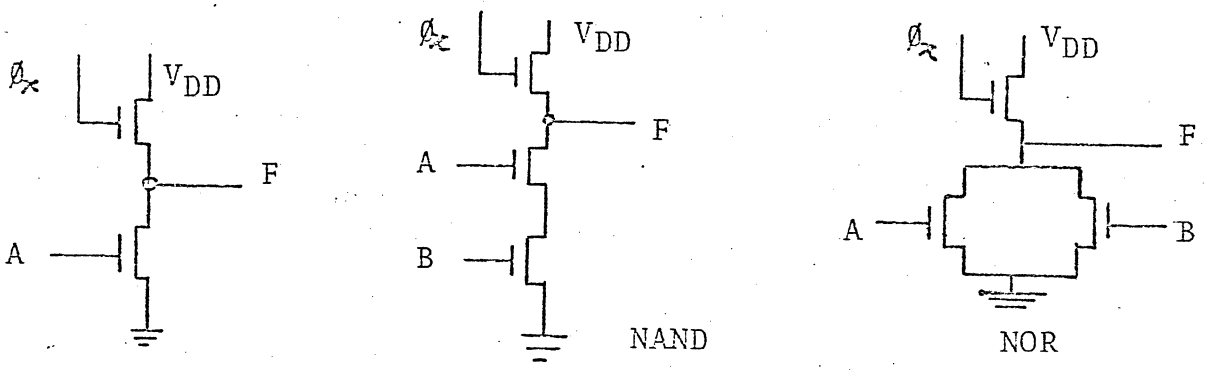
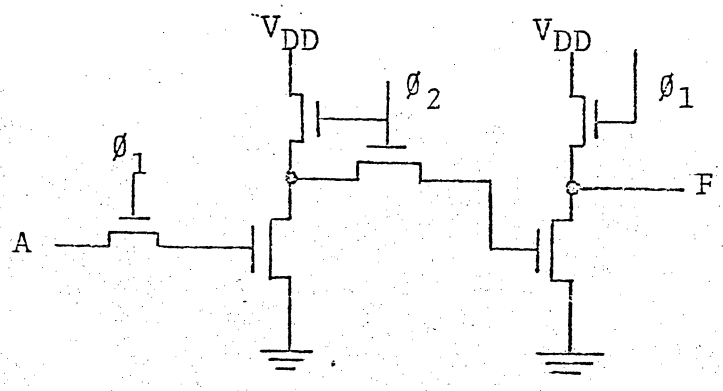


Figure 7: Characteristic Static Circuit

The second cell type utilizes the ability of an MOS device to store charge on a capacitor. The logic gates are shown in Figure 8.





1 Bit of Delay

Figure 8

The circuit configurations are like those for static cells except the gate of the load device is clocked rather than fixed at a supply voltage This reduces the power consumption considerably. Power now is calculated as:

$$P_T = CV^2 F (a + b) + (VI) T$$

where
- a = Duty cycle of Clock 1
- b = Duty cycle of Clock 2
- F = Clock Frequency
- V = Voltage Transition
- C = Capacitive Load

In addition, the devices can be made smaller since the switch device need only discharge the charged capacitance and not sink current from the load.

Two phase logic has the advantage of being able to eliminate race conditions by clocking.

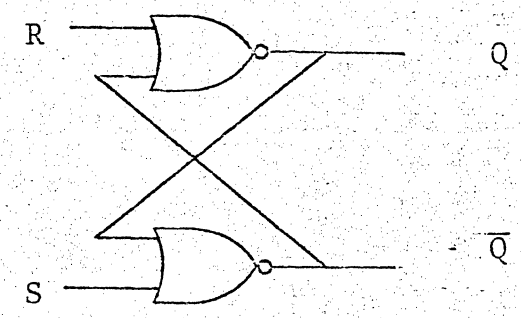
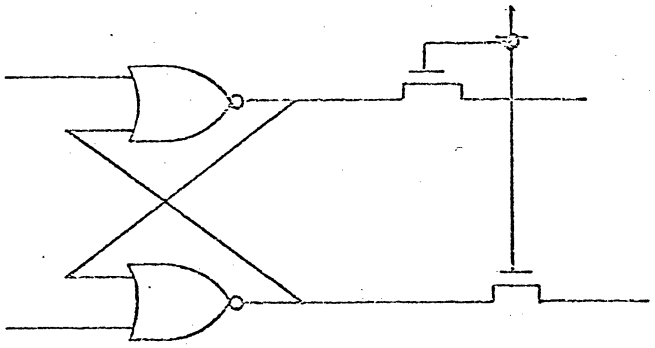


Figure 9

If the initial conditions are as such:

$$R = 0 \qquad S = 0 \qquad Q = 0 \qquad \overline{Q} = 1$$

If S is changed to a 1, $\overline{Q}$ goes to a 0 and Q will change to a 1 after the propagation delay. This obviously presents a problem since for about 200ns both Q and $\overline{Q}$ are 0. To eliminate this condition, a series coupling device can be placed in the outputs to allow the outputs to appear at the proper levels at the same time.



Additions of these gates eliminates the transitory state of 0, 0.

Another example is the shift register. As shown in Figure 10, the Dynamic Shift Register utilizes stored capacitance and delay elements to provide delays. A timing diagram of the shift register is shown in Figure 11.

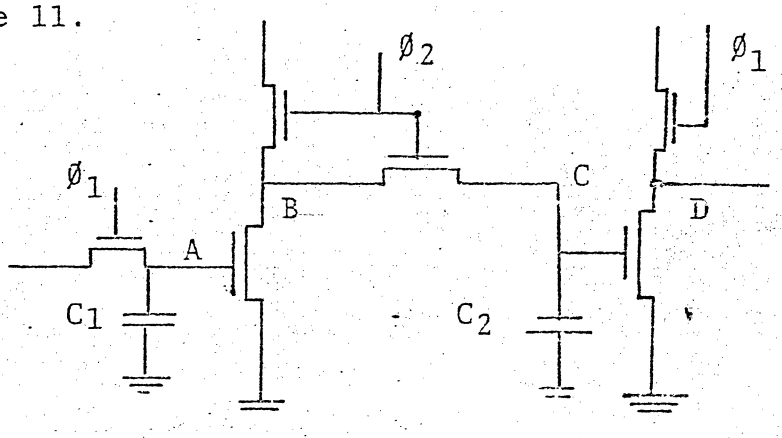


Figure 10

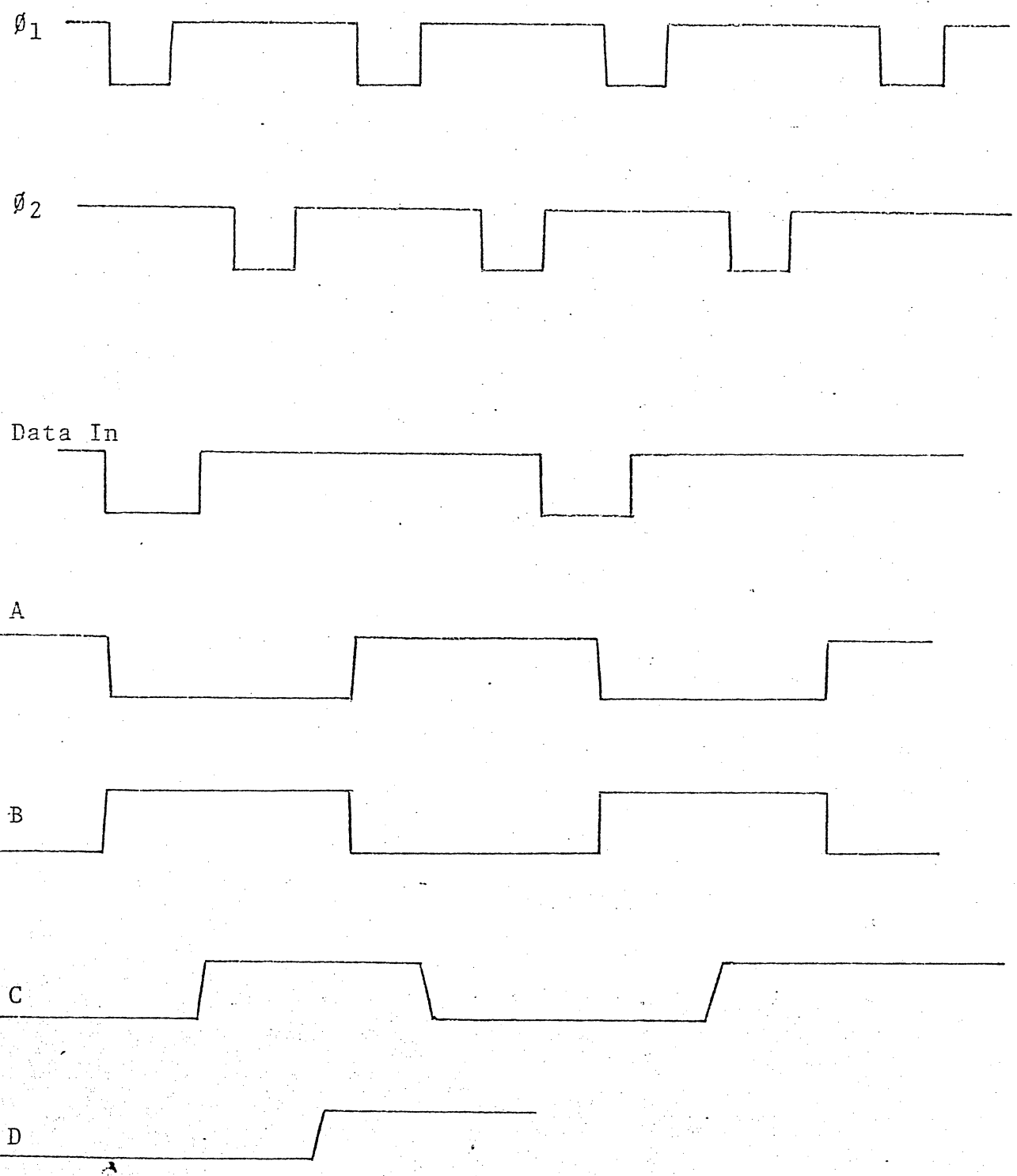
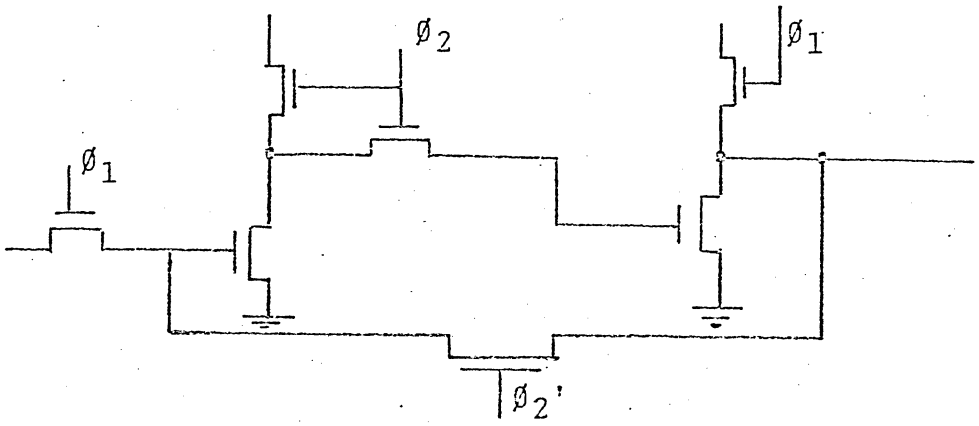


Figure 11

This shift register is limited to about 5 KHz min. frequency due to leakage of stored charge.

Now to demonstrate use of delay elements, let's examine a 2Ø S/R known as a Quasi-Static Register. This cell allows one to utilize delays in static systems where 2 clocks are available.



Ø2' is a slower clock to avoid a race conditions when output is 0 and next bit is a 1.

In summary, 2Ø cells give:

Advantages

Smaller Area

Faster Operation

Completely Synchronous Systems

Eliminate Race Conditions

Disadvantages

Have a minimum operating frequency

Have a DC component of power when clocks are on

For even lower power dissipation, the theory of capacitive charge storage was extended to a 4Ø system. Here, 4 clocks are used instead of two. This type of circuit has all the advantages of a 2Ø circuit plus it uses smaller area because the devices do not have to be ratioed. 4Ø circuitry is shown in Figure 12.

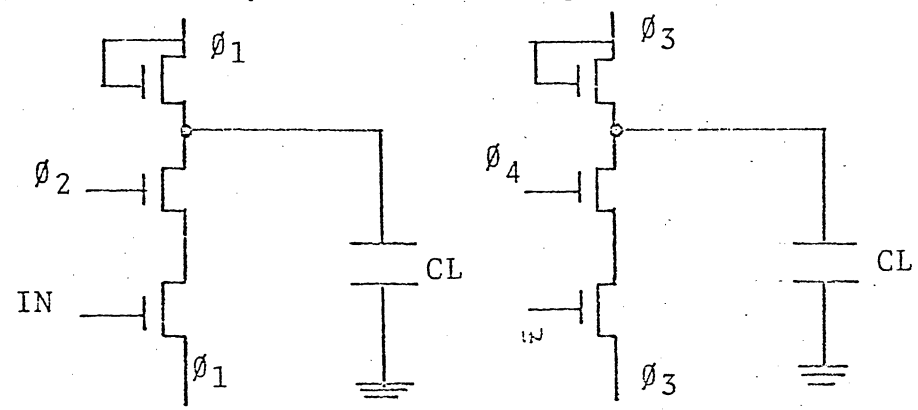


Figure 12

Timing diagrams for a 4Ø circuit are shown in Figure 13.

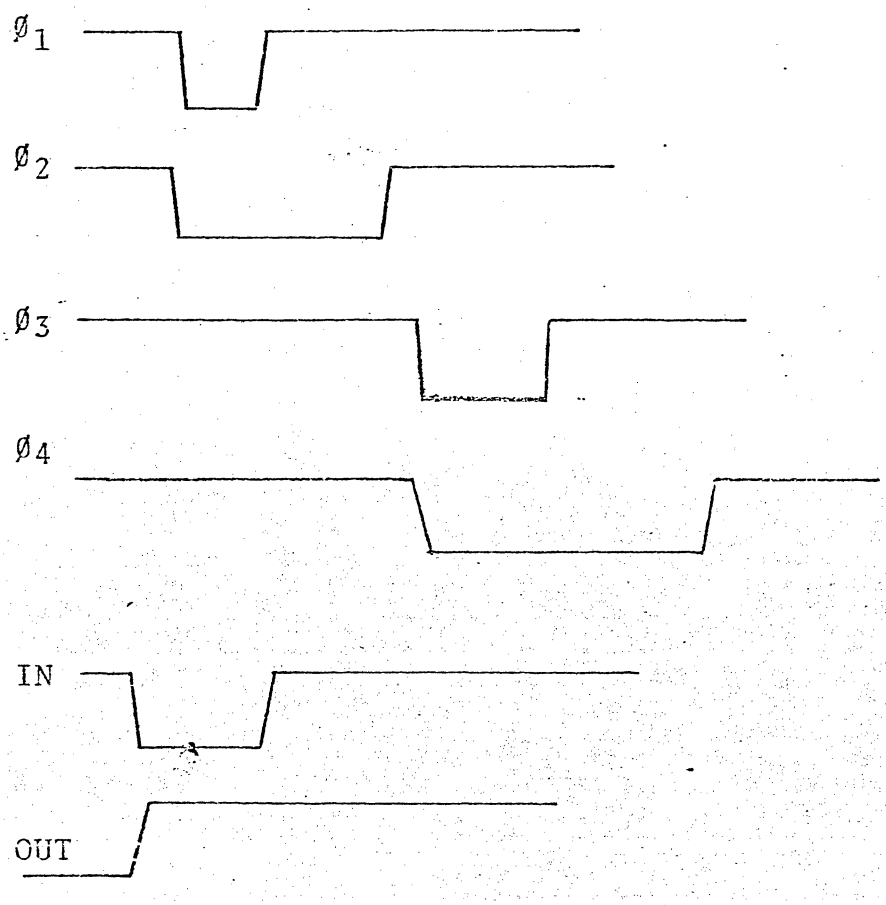


Figure 13

In summary, let's compare the various approaches as to usage.

Static	2Ø	4Ø
DC - 2 MHz	5 KHz - 2 MHz	10 KHz - 10 MHz
Hi Power	Moderate Power	Low Power
Large Area	Smaller Area	Smallest Area
Asynchronous	Requires 2 clocks	Requires 4 clocks
Potential Race Problems	Synchronous	Synchronous

In conclusion, it can be seen that the choices available to a circuit designer are numerous, and a little consideration to the approach taken in design can result in an optimally designed circuit.

CHAPTER V

MOS SHIFT REGISTERS

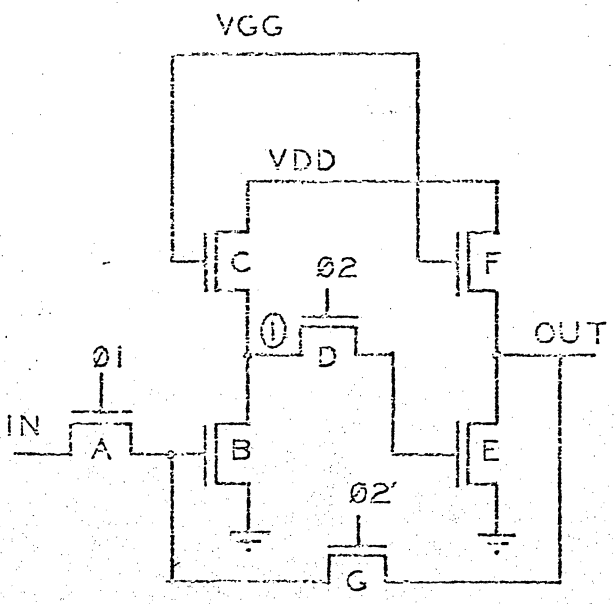
A shift register holds N bits of data that are entered, stored and sampled on command. The data at the input appears at the output after N clock pulses.

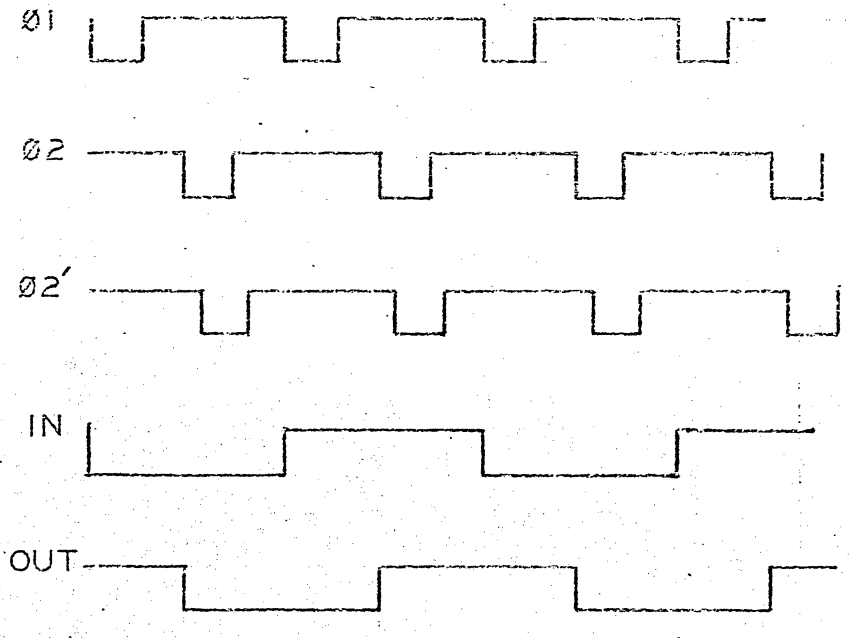
There are two main types of MOS shift registers. One is static and the other dynamic. Static registers are the easiest to understand and design. They are able to store data indefinitely without recirculating. However, they consume more power, are physically larger in their layout, and are slower than dynamic shift registers.

This discussion will cover P channel enhancement mode MOS registers. Logic levels will be assumed to be negative logic, the most negative voltage being a logical one and the most positive being a logical zero. Ø1 time is defined as that time when Ø1 is at a logical one and likewise for Ø2.

STATIC SHIFT REGISTERS

A static shift register bit is made up of 2 ratioed inverters and 3 coupling devices.





At Ø1, time data is coupled from the input of the bit, through A to the gate of B. This sets the state of node 1 to the complement of the input data bit. Note that the second inverter is isolated from the first inverter until Ø2 time when data on node 1 is passed to the gate of E. This causes the output node to assume the same state that was present on the input node during the previous Ø1 time. This level remains throughout the second Ø1 time resulting in one bit of delay.

In order for data to be held indefinitely, device G is added from the output to the input of the bit. This forms a cross coupled flip flop which stores data when Ø2 and Ø2' are logical one and Ø1 is logical 0. Ø2' is a delayed Ø2 to prevent data from racing from the output to input before the output reaches its final state.

The static shift register requires 6 supply lines, Ø1, Ø2, Ø2', VGG, VDD, and ground. The inverters must be ratioed to give good 0 levels. For these reasons the bits tend to be big, 35-50 mil^2. This results in large chip areas. A clock driver for Ø2' is also required which further adds to the chip area.

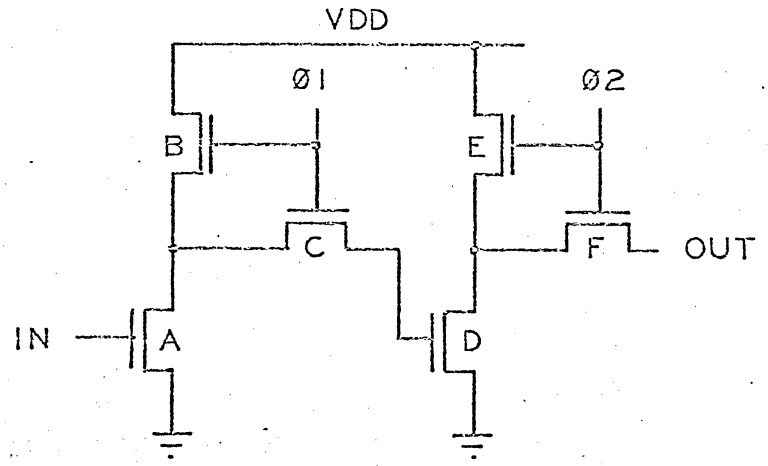
Speed is slower with static shift registers because the load device has a relatively high impedance and cannot charge the output capacitance very fast.

DYNAMIC SHIFT REGISTERS

MOS dynamic shift registers take advantage of several unique MOS characteristics. These are:

1. MOS load devices may be switched on and off.
2. Charge can be stored temporarily on the gates of MOS devices.
3. MOS devices are bilateral, ie they can transfer charge in both directions.

2Ø DYNAMIC RATIOED



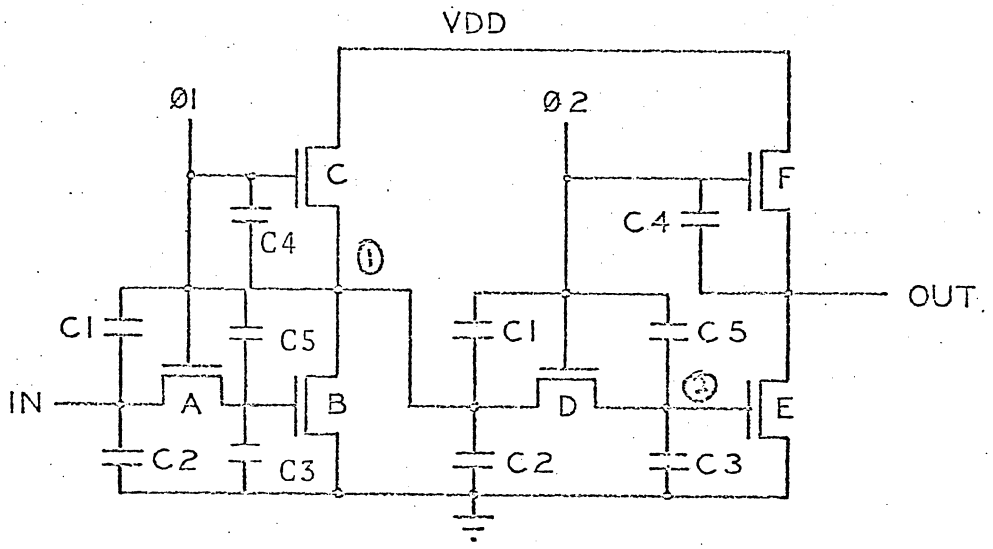
The 2Ø dynamic raticed cell is made up of two ratioed inverters and two coupling devices. The operation of this cell is similar to that of the static cell. However, the load devices are clocked resulting in a significant reduction in power dissipation per bit. Ø1 and Ø2 clock timing is the same as that for the static cell.

This circuit has a lower frequency limit that is determined by the magnitude of the surface leakage on the gate nodes of devices A and D. If a zero is placed on the input during Ø1 time,

then the gate node of D will be charged to a 1. When Ø1 goes off, this node will store that 1 level giving a good 0 level on the output of the bit during Ø2 time. However, if the clock frequency is low enough, charge on the gate node of D may leak off the P diffusion of device C to the N substrate. This will cause bad data to appear at the output during Ø2 time. This lower frequency limit usually occurs from 100 to 500 cycles.

This cell is large because of the ratioed inverters required. However, it is relatively easy to design because the cell does not depend on capacitance ratios for proper operation. Four supply lines are required. An average bit size is about 40 mil^2.

2Ø DYNAMIC RATIOLESS



The 2Ø dynamic ratioless bit is made up of six ratioless devices. For correct operation of this bit the following capacitance ratios must be maintained:

1. $\frac{C_1}{C_2 + C_3} > 1$, C_1 is enhanced MOS overlap capacitance.

   C_2 and C_3 are PN capacitances to the grounded substrate.

2. $\frac{C_2 + C_1}{C4} > 1$, C_1 is MOS overlap capacitance.

3. $\frac{C_3}{C_5} > 1$, C_5 is MOS overlap capacitance of device D.

4. $\frac{C_1}{C_3} > 1$

Assume first a logical 1 is present on the input. During $Ø_1$ time, this 1 is clocked through A to the gate of B. At the same time node 1 will assume some voltage between VDD and ground. When Ø1 goes off, node 1 will be discharged to ground through A leaving a logical 0 on node 1. During Ø2 time, any voltage on node 2 will be discharged to ground through D and A leaving a 0. This allows the output node to be charged to VDD through F. However, as Ø2 goes off (goes positive towards ground), the output node will be deteriorated due to the voltage divider action of C2 + C1 and C4. If C2 and C1 are much larger than C4 then the output node remains close to VDD. This logical 1 remains on the output during the second Ø1 resulting in one bit of delay.

Now, if a zero is on the input during Ø1 time it will be passed to the gate of B allowing node 1 to be charged to VDD. The charge

2Ø DYNAMIC RATIOLESS

The 2Ø dynamic ratioless bit is made up of six ratioless devices. For correct operation of this bit the following capacitance ratios must be maintained:

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2. $\frac{C_2 + C_1}{C_4} > 1$, C_1 is MOS overlap capacitance.

3. $\frac{C_3}{C_5} > 1$, C_5 is MOS overlap capacitance of device D.

& $\frac{C_1}{C_3} > 1$

Assume first a logical 1 is present on the input. During Ø1 time, this 1 is clocked through A to the gate of B. At the same time node 1 will assume some voltage between VDD and ground. When Ø1 goes off, node 1 will be discharged to ground through A leaving a logical 0 on node 1. During Ø2 time, any voltage on node 2 will be discharged to ground through D and A leaving a 0. This allows the output node to be charged to VDD through F. However, as Ø2 goes off (goes positive towards ground), the output node will be deteriorated due to the voltage divider action of C2+C1 and C4. If C2 and C1 are much larger than C4 then the output node remains close to VDD. This logical 1 remains on the output during the second Ø1 resulting in one bit of delay.

Now, if a zero is on the input during Ø1 time it will be passed to the gate of B allowing node 1 to be charged to VDD. The charge

on this node is now equal to (VDD) (C1+C2). During Ø2 time this charge will be divided between C2 and C3. The voltage on node 2 will then be $\frac{VDD\ (C1+C2)}{C2+C3}$. If C1 > C3 then the voltage on node 2 will be reasonably close to VDD. Also, because C_1 is larger than C2+C3, the magnitude of the voltage on node 1 when Ø1 goes will be increased because of the capacitive feed through of Ø2 through C1. This increase is approximately $\frac{C1}{C1+C2+C3}$ VØ, where VØ is the voltage of Ø2 when Ø2 comes on. Node 2 now goes more negative until device D turns off. The voltage on node 2 will be approximately

$\frac{VDD\ (C1+C2)}{(C2+C3)} + \frac{C1}{C1+C2+C3}$ VØ or (VØ-VTH-VBE), whichever is

smaller. Usually this is (VØ-VTH-VBE). Now as Ø2 goes off this voltage on node 2 is deteriorated by the feedthrough of Ø2 through C5. This decreases the magnitude of voltage on node 2 by VØ $\frac{C5}{C5+C3}$

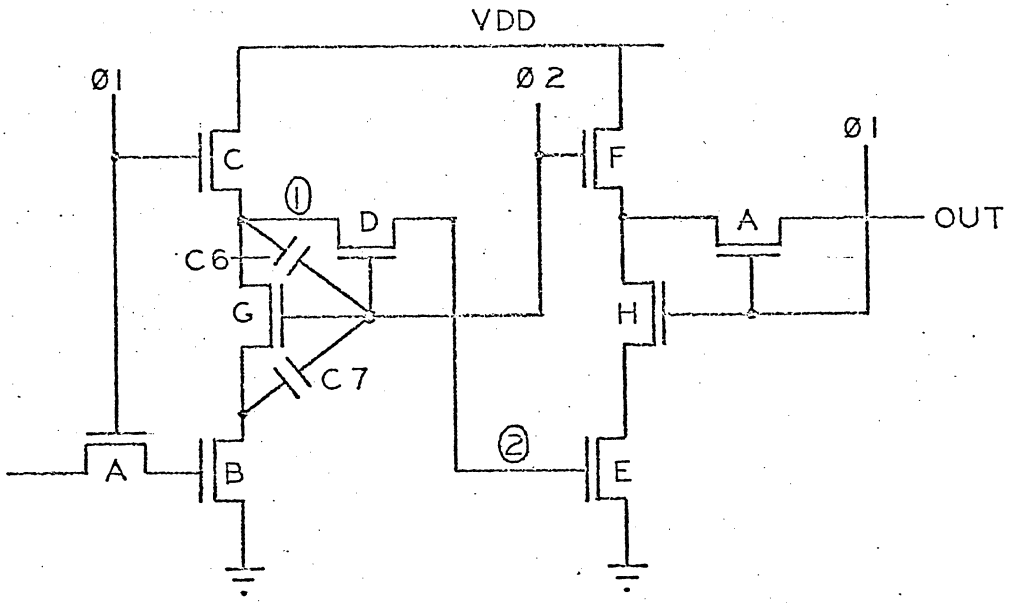
leaving 1. $\frac{VDD(C1+C2)}{(C2+C3)} + \frac{C1}{C1+C2+C3}$ VØ $-$ VØ $\frac{C5}{C5+C3}$

or 2. (VØ-VTH-VBE) - VØ $\frac{C5}{C5+C3}$ whichever is smaller.

For maximum voltage transfers C3 > C5. The output node is then discharged to ground through E and remains at logical 0 throughout the second Ø1 resulting in one bit of delay.

This cell has four supply lines. All devices can be minimum size, significantly reducing bit area. Devices B and E have impedances nearly an order of magnitude smaller than the load devices in ratioed shift register cells resulting in much faster switching times and hence a higher frequency of operation. The lower frequency limit is determined by the same PN junction leakage as discussed in the previous section on 2Ø dynamic ratioed shift registers. An average bit size is 25-30 mil^2.

2Ø DYNAMIC RATIOLESS POWERLESS



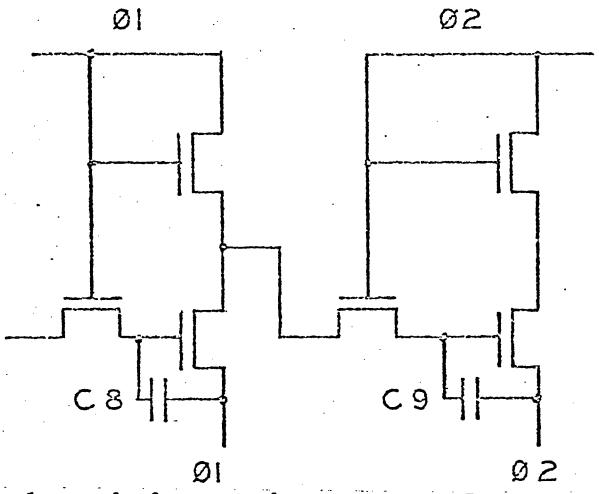
This cell is made up of eight ratioless devices. It is similar to the 2Ø Dynamic ratioless cell except that devices G and H have been added. This circuit consumes no DC power. Note that VDD has two branches to ground. One branch is made up of C,G, and B; the other of F,H, and E. Each branch has a device clocked by Ø1 and a device clocked by Ø2. Since Ø1, and Ø2 are non-overlapping there is never a DC current path between VDD and ground.

The same capacitance ratios as in the ratioless cell must be maintained. Devices G and H add additional capacitances that must be considered. C6 will be enhanced with C1. C7 should be made as small as possible.

All devices in this cell can be made minimum size. The two additional devices per bit make it somewhat larger than the 2Ø dynamic ratioless bit. Four supply lines are required. This bit is one of the hardest to design because of all the capacitance ratios that must be considered.

2Ø W/Ø GROUND, VDD DYNAMIC RATIOLESS, POWERLESS

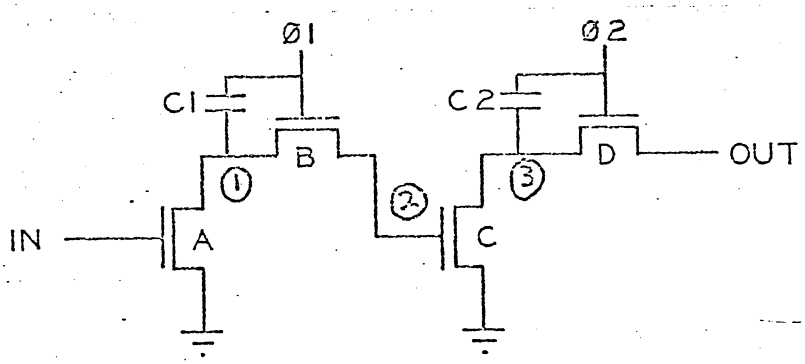
This bit is similar to the 2Ø dynamic ratioless except that VDD and ground have been replaced with clocks.



All devices can be minimum size. No DC power is drawn in this circuit. The capacitance ratios will be the same as the 2Ø dynamic ratioless with the addition of C8 and C9. These capacitances should be as small as possible to prevent clock feedthrough.

This bit is the smallest of any discussed so far because only two supply lines are required, Ø1 and Ø2. Average bit sizes are 15 to 20 mil^2. The clock capacitance is higher in this circuit because there is a PN capacitance that must be driven in addition to the two MOS gate capacitances.

2Ø DYNAMIC CAPACITIVE LOADS W/GROUND

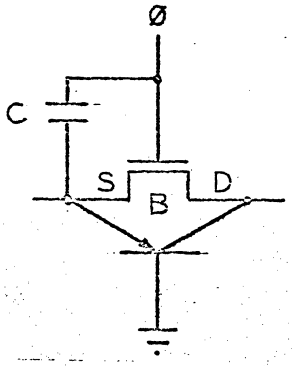


Only four devices are required in this bit making it one of the smallest shift register bits. The normal MOS load devices have been replaced by capacitors C1 and C2. These are enhanced overlap capacitances. Again, the capacitance ratios that must be maintained are similar to those of the 2Ø dynamic ratioless shift register bit.

If a logical 1 is present on the gate of A then node 1 will be discharged to a zero. During Ø1 any voltage on node 2 is discharged through B and A leaving a 0 on node 2. Prior to Ø2 time node 3 is undefined. As Ø2 turns on, the voltage on node 3 is increased by almost the magnitude of Ø2 if C2 is large enough. This logical 1 is then coupled to the output of the bit during Ø2 and remains on the output node during the second Ø1 resulting in one bit of delay.

A logical 0 on the input leaves the state of node 1 undefined until Ø1 time when most of the clock voltage is fed through to node 1 and transfered through B to node 2. This causes node 3 to be discharged to ground. At Ø2 time any voltage on the output node is then discharged to ground through D and C.

The operation of this circuit is greatly influenced by a parasitic PNP bipolar transistor across coupling devices B and D.



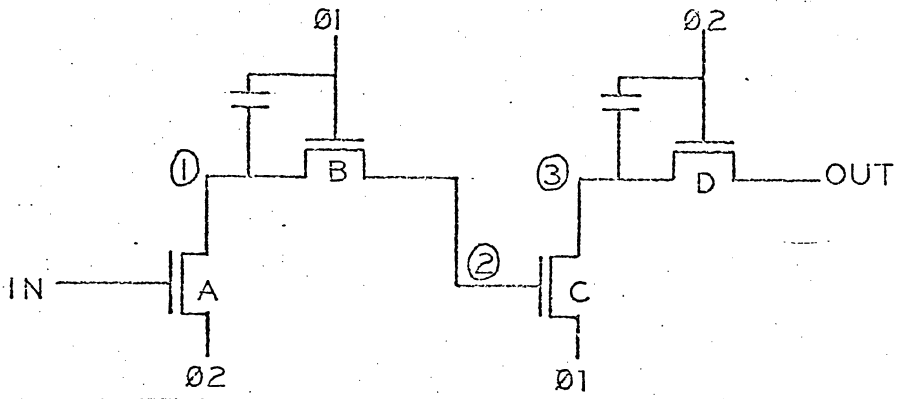
The emitter of the parasitic device is the P diffusion of the coupling device, the collector is the drain, and the base is the N

substrate. Because of the enhanced MOS overlap capacitance C, it is possible for the source of the coupling device to go positive with respect to the substrate. This will occur as Ø returns to ground. The parasitic transistor is then placed in its active region and positive current flows from source to drain of the coupling device. This current will deteriorate a 1 level on on the gate of the next switch device. This effect can greatly increase the lower frequency limit of this bit.

To correct this situation the channel length of the coupling devices must be made as large as possible. This decreases C_{ϕ} by making the base width of the parasitic device wider. However, if it is too long the high frequency performance will deteriorate because charge will not be transferred fast enough through the high impedance of the coupling device. A compromise must be achieved.

This circuit has three supply lines and occupies an area of 10 - 15 mil^2. Because the parasitic transistor effects are fairly unpredictable this bit has not found wide acceptance among MOS designers.

2Ø DYNAMIC CAPACITIVE LOAD W/O/ GROUND



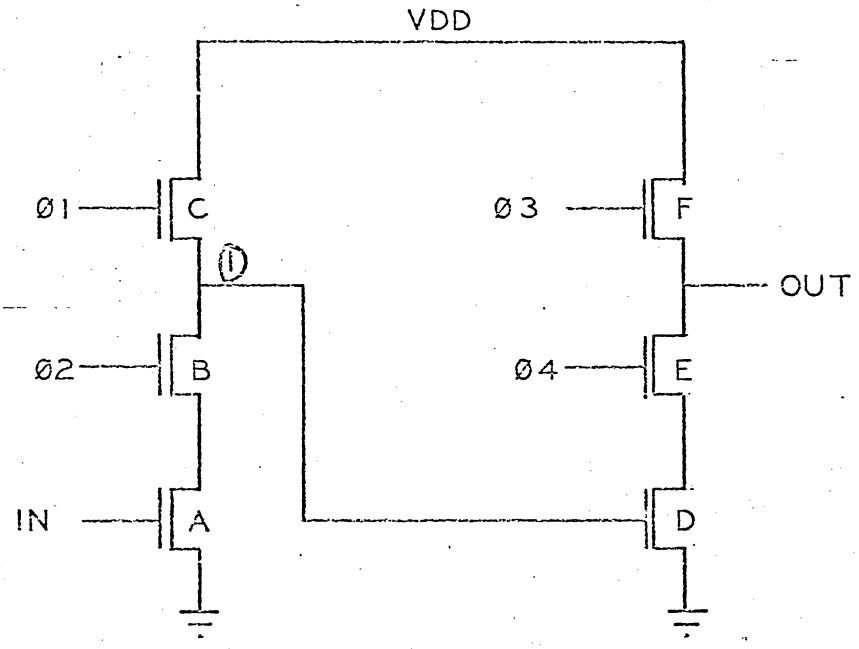
The layout and operation of this bit is practically the same as the previous shift register except that ground has been removed and replaced with the clocks.

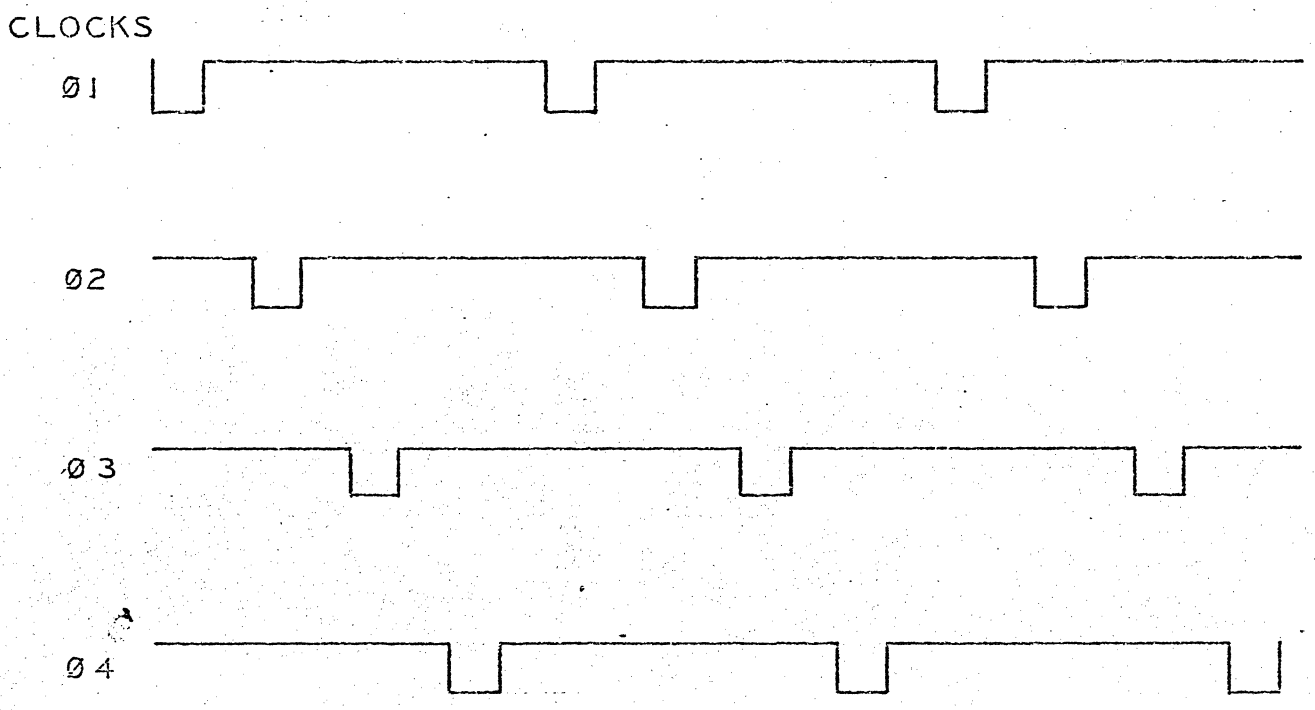
Assuming Ø2 is at ground, a logical 1 at the input discharges node 1 to ground. At Ø1 time node 2 is discharged through B and A. This leaves node 3 undefined until Ø2 time when a 1 is fed through capacitor C from the clock. During Ø2 time this logical one appears on the output of the bit.

A zero on the input causes node 1 to be charged to a 1 during Ø1 time pulling node 3 to ground when Ø1 goes off and appearing on the output during Ø2.

This bit suffers from the same parasitic effect as discussed previously.

4Ø DYNAMIC RATIOLESS W/NON-OVERLAPPING CLOCKS





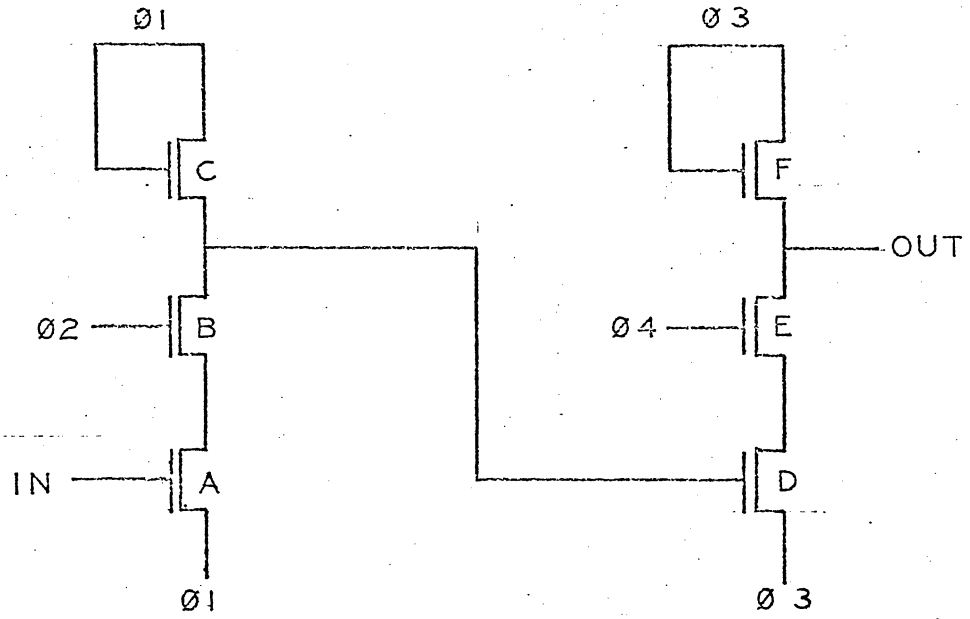
This bit is used in 4Ø systems. All devices are minimum size. No DC power is dissipated because no DC current path exists between VDD and ground.

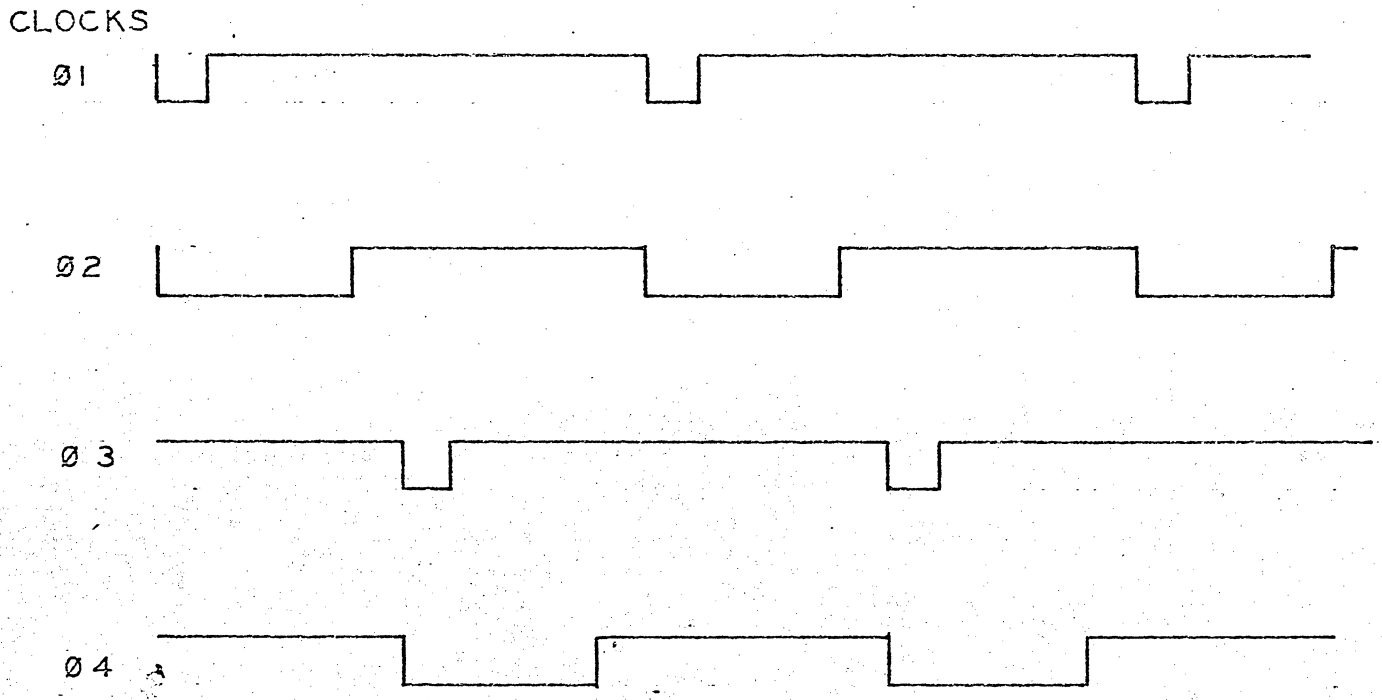
During each Ø1 time, node 1 is charged to a 1. If a 1 exists on the input during Ø2 time then node 1 will be discharged through B and A to a 0. Ø3 charges the output node to a 1. Since D is turned off, the output node will not be discharged during Ø4 time resulting in one bit of delay.

A zero on the input leaves node 1 at a 1 during Ø2 time. Ø3 charges the output node to a 1. When Ø4 comes on this 1 is discharged through E and D leaving a 0 on the output.

Six supply lines are required. A typical cell size is about 20 mil^2. Since C and F are minimum size with relatively low impedances this cell is one of the fastest shift register bits.

4Ø Dynamic ratioless with overlapping clocks





This cell is similar to the previous cell except that V_{DD} and ground have been replaced with clocks. Only four supply lines are required.

Overlap capacitances should be minimum to prevent clock feedthroughs.

CHAPTER VI

M E M O R I E S

I. READ/WRITE MEMORIES

Types of Storage

In the design of a computer system, the systems designer has traditionally employed a "hierarchy" of types of information storage. A list of the levels in this hierarchy is given below, with the fastest (and also the most expensive) types being listed first. The amount of each type of storage employed in a computer system typically increases as we go down this list.

1. Discrete bit storage. The usual implementation of this type of storage is a bipolar integrated circuit flip-flop, which may have quite a few inputs, such as an AND type clocked JK flip-flop. The usual function of discrete bit storage is as indicators, storage or generation of control and timing signals, stages in counters, etc. Usually a small number of these circuits on a chip are possible because of their high power consumption and large number of leads. Their speed is usually equal to several gate delays.
2. Registers and Buffers. Registers are usually implemented using integrated circuit flip-flops, and are used for temporary storage of intermediate results and also for implementation of logical operations, such as in arithmetic units.
3. Scratch Pad Memories. These are used for temporary storage of intermediate results which will be used in the next operation, and for storage of frequently used data, for short iterative subroutines, and for other similar applications where information needs to be

accessed or processed in a time less than the cycle time of the main memory and are implemented using bipolar arrays. Thin-film memories and plated wire memories have sometimes also been used.

4. Main memories. The main program, the software used by the system, and the data used by and generated by the program being run is stored in the main memory. Magnetic cores have dominated this area in the past, but MOS random access memories are challenging.
5. On-line Auxiliary Storage. This type of storage is for large data files and programs that may be recalled by the computer, but where speed is less important than capacity, and low cost is necessary. Disks and drums are often used to implement this type of storage; however MOS shift registers are being used as disk replacements in applications which require faster access times. The speed of on-line auxiliary storage is usually several orders of magnitude slower than that of the main memory.

Off-Line Auxiliary Storage. This type is used for storing large data files and program libraries, etc., which are used infrequently enough to permit a manual operation to load the stored information into the main memory of the computer. Magnetic and paper tape and punched cards are the major modes of this type of storage.

Definitions of Memory Terms

Sequential Memory.

Information is serially written into or read out of the memory one bit at a time. Thus the access time for the memory is equal to the number of bits multiplied by the

time required to perform a read or write operation on one bit.

Random Access Memory (RAM)

This is a type of memory in which any location can be accessed without regard to any other location. The access time is the same for any location in the memory; all that must be provided is the address of that location (as well as various commands and timing signals). RAM's are used primarily as scratch pad memories, buffer memories, and main memories.

Content-Addressable Memory (CAM)

Also called associative memory. A CAM has read/write capability, just as a RAM. However, data is not stored in a specific location or address in the memory. Some portion of a word is specified as Search Criteria and the rest is masked. Then, in one operation all words in the memory are compared with the search criteria, and a word which matches is accessed. Memory allocation in time-shared computers, sorting, merging, and pattern recognition are applications where CAM's are used.

Access Time

This is the time required to address a location of a memory and obtain useful information. There is no single sacred definition of access time applicable to all memories; the individual situation must be all memories; the individual situation must be analyzed to determine the most meaningful or convenient definition of access time.

Cycle Time

This is the time required to perform a complete read or write operation at any address of the memory. It will usually include the time necessary for address inputs to stabilize, the time to access the memory or to write into it, the time required to transfer the obtained information where it is needed, and also the time for the memory to recover from the read or write operation. There is no universal way to measure or specify cycle time; each case must be examined individually.

Read Recovery Time

The time that must be allowed for the memory to recover after location has been accessed before another read or write cycle can be initiated.

Write Recovery Time

The time that must be allowed after a write operation before a new read or write operation can be initiated.

Non-Destructive Read-Out (NDRO)

This means that the information at a location is not destroyed if that location is accessed. Then no rewrite operation is necessary. In general, semiconductor memories are NDRO, while core memories have destructive read-out.

Memory Organization

Number of words by number of bits.

Volatility

A memory is said to be volatile if the incormation is lost when the power fails. Semiconductor memories are always volatile unless there is a power back-up system. Some types of magnetic memories are non-volatile

Linear Select Memory (2D)

A cell of a memory array can be selected by one line to the cell. Figure 5.C.1 shows an example of a linear select MOS storage cell.

X-Y Select Memory (3D)

Decoding occurs at the cell; ie, an X and a Y line going to the cell must have a "1" level before the cell is selected. Figure 5.C.2 shows an X-Y MOS cell.

The main memory, or main-frame memory, is the primary operational storage block of a computer. Although this area is dominated by cores in today's computers, the next generation of computers is expected to use semiconductor main-frame memories, and MOS dynamic memories are a leading candidate to fill this role. The fastest core memories operate with about 400ns cycle time. Semiconductor memories in the 100-500 ns region can be economically made. There are many requirements for buffer memories in computer peripheral equipment, where slower data rates permit the use of slower memory cycle times. Static MOS memory is already a finding application in this area.

The DC MOS Memory Cell

The typical DC MOS storage cell is a simple, effective, and low-cost design. The cell consists of six p-channel, enhancement mode devices and is shown in Figure 5.C.3. Two of these (R_1 and R_2 in Figure 1) act as resistors and are biased on by the V_{GG}

supply. The two cross-coupled transistors Q_1 and Q_2, act as a storage element, and Q_3 and Q_4 are switches that selectively connect or isolate the individual storage cell from the sense-digit lines. Two sense-digit lines are used, providing signal and complement drive to the cell. The word-select line drives the gates of Q_3 and Q_4.

With the p-channel devices used, the V_{SS} power supply is the most positive voltage and V_{DD} is negative by 10 V or more. Depending on the particular processing technology used in the construction of the cell and the cell operating constraints, V_{GG} is equal to, or more negative than, V_{DD}. Since p-channel enhancement mode devices are turned on when the gate is sufficiently negative (relative to the substrate), the substrate is connected to the most positive system voltage, i.e., V_{SS}.

In the storage mode, the cell maintains one of its two stable states. The word select line is in the high logic state (close to V_{SS}) so that transistors Q_3 and Q_4 are off. As a result, the storage cell is isolated from the sense-digit line. One of the possible stable states exists when the gate of Q_2 is low. This means that Q_2 is conducting so that its drain (node B) is at a high potential (close to V_{SS}). The difference in potential between V_{DD} and the drain of Q_2 is dissipated across resistor R2. The high potential on node B is coupled to the gate of Q_1. With this high potential on the gate, Q_1 is turned off. As a result, node A is at approximately V_{DD} since there is essientially no current flow through R_1. The drain of Q_1 (node A), which is connected to the gate of Q2, provides the low or V_{DD} potential that we defined as being stable state 1.

To change the information stored in the basic cell, the sense-digit lines are appropriately biased and the word-selection line placed in the active or low state. Sense-digit line A is a high potential. The complementary signal is present on sense-digit line B which is connected to a low potential. When the word select line goes to a low potential, transistors Q_3 and Q_4 turn on, connecting the sense-digit lines to the cross-coupled transistors Q_1 and Q_2. In the example shown in Figure 2, Q_3 connects node A to the high level on sense-digit line A. This high potential is coupled to the gate of Q_2 and tends to turn Q_2 off. At the same time, because Q_4 is conducting, node B is coupled to the low supply. This low voltage is applied to the gate of Q_1 and tends to turn Q_1 on. This provides an additional path from V_{SS} to node A, further increasing the potential on the gate Q_2. Therefore, the indicated sense-digit line potentials result in transistor Q_1 turning on and transistor Q_2 turning off. This is the alternate stable-state of the storage element. Completing the write operation, raising the word-select line potential, turns off Q_3 and Q_4 and isolates the storage cell from the sense-digit lines.

Connecting sense-digit line B to V_{SS}, sense-digit line A to V_{DD}, and activating the word-select line will reverse the state of the flip-flop, turning Q_2 and Q_1 off.

For reading, the word-select line is again activated. If the sense-digit lines are terminated by high-resistance MOS resistors, so that both are at a negative voltage prior to activating the word-select line, then if Q_2 is on, the adjacent sense-digit line B will be pulled to ground when Q_3 and Q_4 are turned on. Then the state of sense-digit line B can be detected by a simple MOS inverter or gate.

Figure 5.C.4 shows a partial circuit schematic of the MC1170, which is a static 64 bit fully decoded RAM using the above storage cell. This memory has a cycle time of less than 800 ns.

The Dynamic MOS Memory Cell

The dynamic memory cell is shown in Figure 5.C.5. Its operation is as follows: Initially, when the Row Select Line is at 0 Volts, the Data Bus and the Read Bus are pre-charged to a negative voltage. When the Row Select Line voltage goes to the intermediate voltage -IV, the Read Bus is conditionally discharged to ground through Q_B and Q_C, or remains at the precharged voltage, depending on whether a "1" or a "0" is stored on the capacitance of the storage node. When the Row Select voltage goes to -V volts, the complement of the stored information, which is now on the Read Bus, is inverted by the column amplifier. Thus the information on the storage node re-appears on the Data Bus and the storage node is refreshed through Q_A.

Operation of the Dynamic Memory

Figure 5.C.6 shows timing diagrams for Read/Refresh and Write cycles. Prior to the beginning of each cycle, PRECH is at -20V, which causes the Data Bus and the Read Bus and also certain nodes to be pre-charged to the proper voltages.

The decoding section selects the row and column specified by the address inputs.

The XENBL input goes to -20V after the X address inputs are stable. The intermediate voltage then appears on the row select line determined by the X address inputs. During

the time that the intermediate voltage is present, the Read Bus is conditionally discharged to ground through Q_C and Q_B if a "1" is stored on the storage node; the value of the intermediate voltage is designed so that Q_C remains off. The intermediate voltage must remain on the Row Select Line long enough to permit discharging the Read Bus voltage to a value lower than the threshold of the column amplifier.

When the conditional discharge of the Read Bus is complete, the YENBL input is set to -20V. This enables the dynamic Y decode gates so that the addressed column is selected. The information on the Read Bus of each column is gated into the respective column amplifiers, is inverted, and appears on the respective Data Bus, in the case of a Read/Refresh cycle. The Row Select Line of the addressed row goes from the intermediate voltage to a more negative -V volts, and transfers the information on each Data Bus to the respective storage node through Q_C of each respective cell. Thus the original information on each storage node of the selected row is refreshed. The column select line of the addressed column gates the information on the Data Bus of the selected column to the I/O circuit; a stored "0" results in an output current in the Data Out Line.

For the case of a write cycle, the information on the Data In line is gated to the Data Bus of the selected column and is transferred through Q_C of the selected cell to its storage node. The remaining cells of the selected row are refreshed.

Figure 5.C. shows a block diagram of a 1024 bit chip using dynamic storage.

On the other hand a dynamic ROM will normally use AND decoding because it can be reduced in size and validated by the clocks. These of course are not hard and fast rules. The design may need special configurations to fit its specific needs. As for the memory matrix itself, it's designed to be of an optimum nature and as small as possible. Present day techniques for programming are one of two types; they are metal and gate. Gate programming is predominent over metal because it requires less area to do. When the gate technique is used the mask for this process is programmed by eliminating gates. The disadvantage of this technique is that it is in the early process steps and turn around time is relatively long. Where as with metal program a metal link connects all gates to the drive line and this line is etched out after all the basic process steps are complete. Because the area required to do this is so large, the advantages of a post process step is overweighted (in my opinion) by the monsterous chip size.

Buffers are designed to make the necessary signal amplifications for external use and their design is usually at the discretion of the engineer. The actual output stage is usually open end or of the push pull type and prior driven stages have to be compatible with the type of output stage and functional requirements.

As for the future of ROM's it is obvious that they are here to stay but the manner in which they will be designed and processed is best left to the crystal ball gayer. It is safe to say that the companies that have the ability to product and are leaders in process techniques and development will get the majority of the business.

Figure 5.C.1 Linear Select MOS Storage Cell

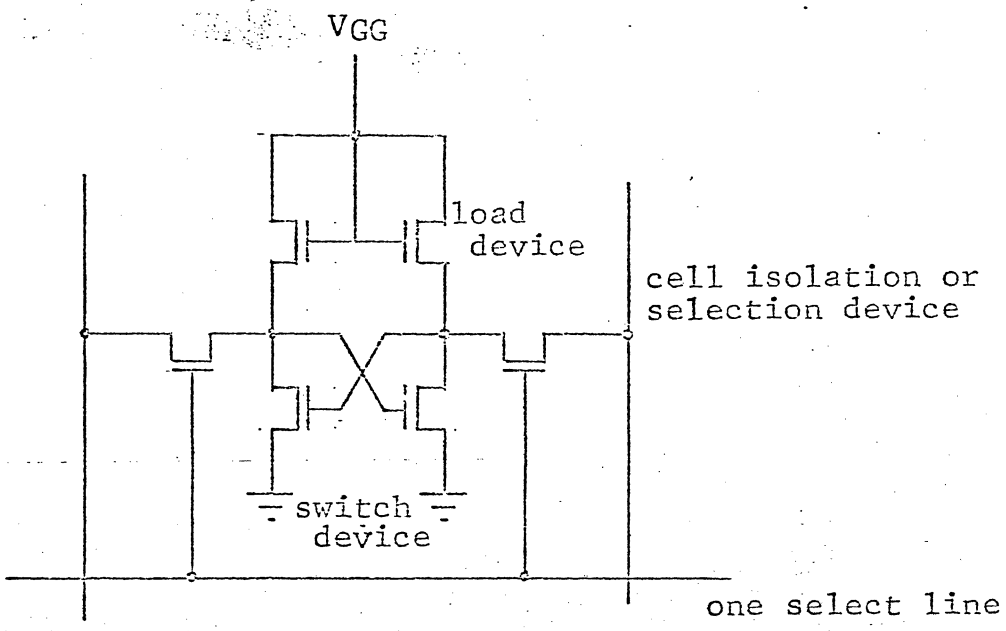
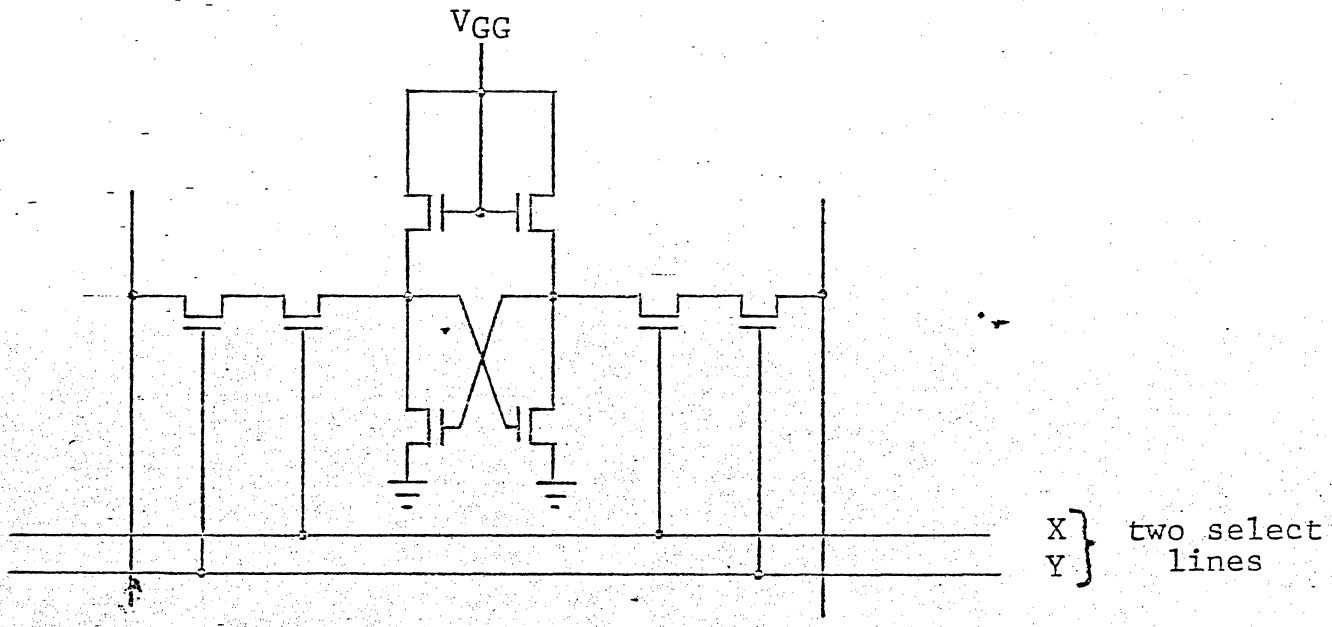


Figure 5.C.2 X-Y Select MOS Storage Cell



The Basic MOS Storage Cell

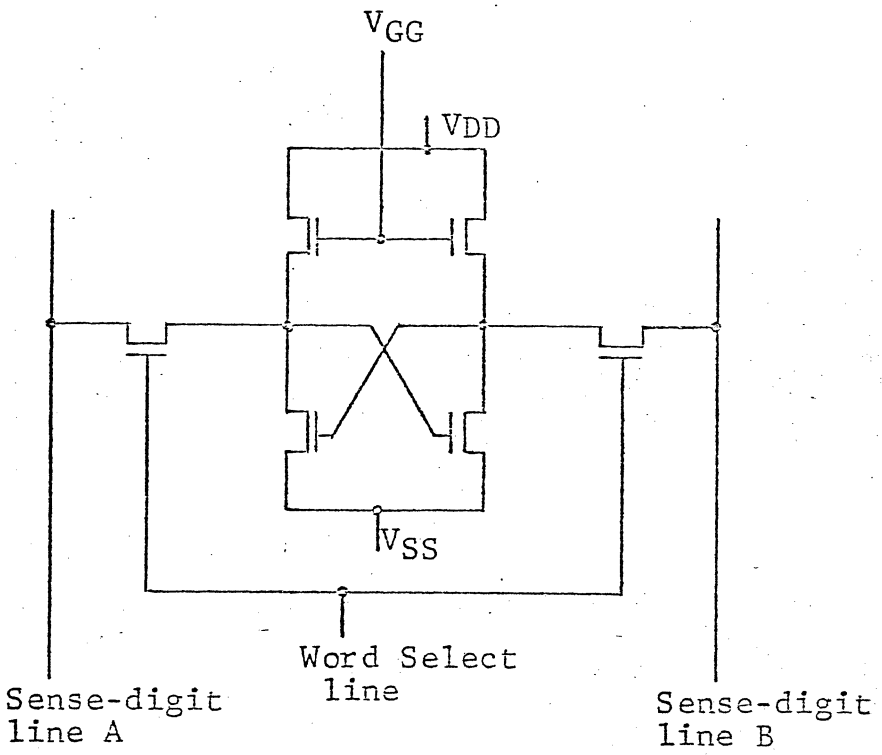


FIGURE 3.C.3

FIGURE 5.C.5

DYNAMIC STORAGE CELL

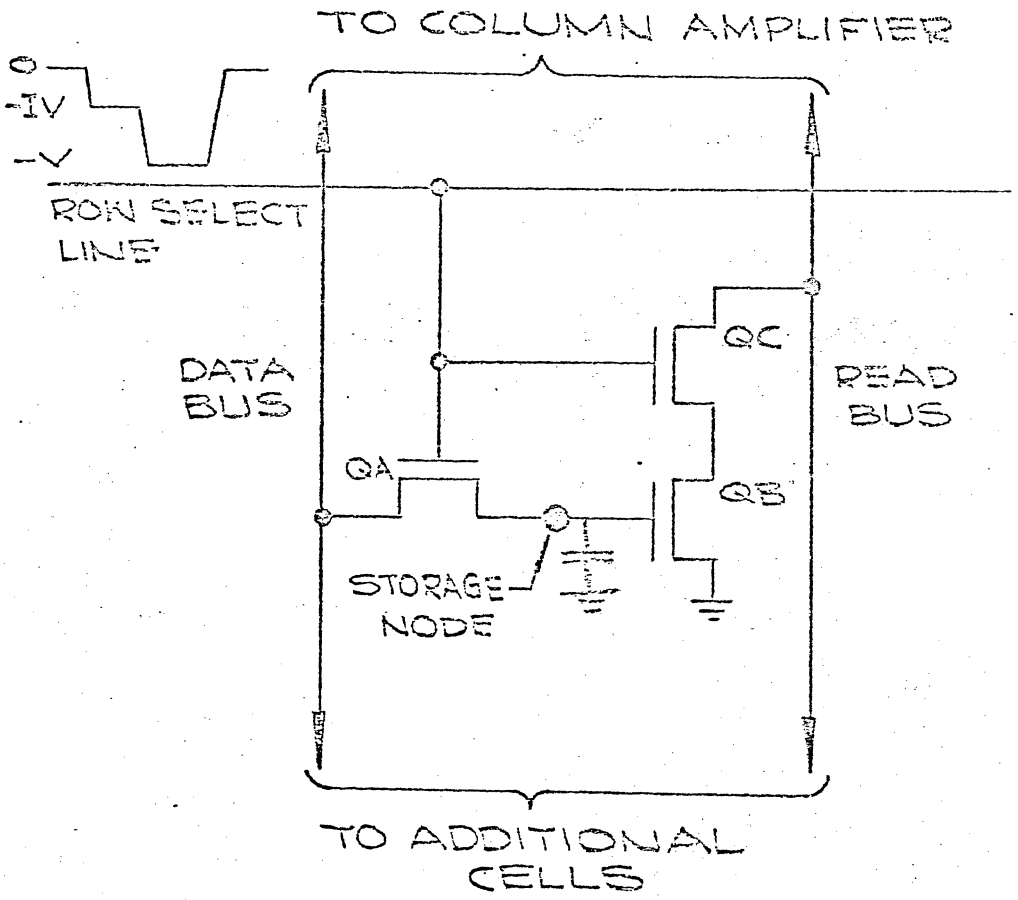
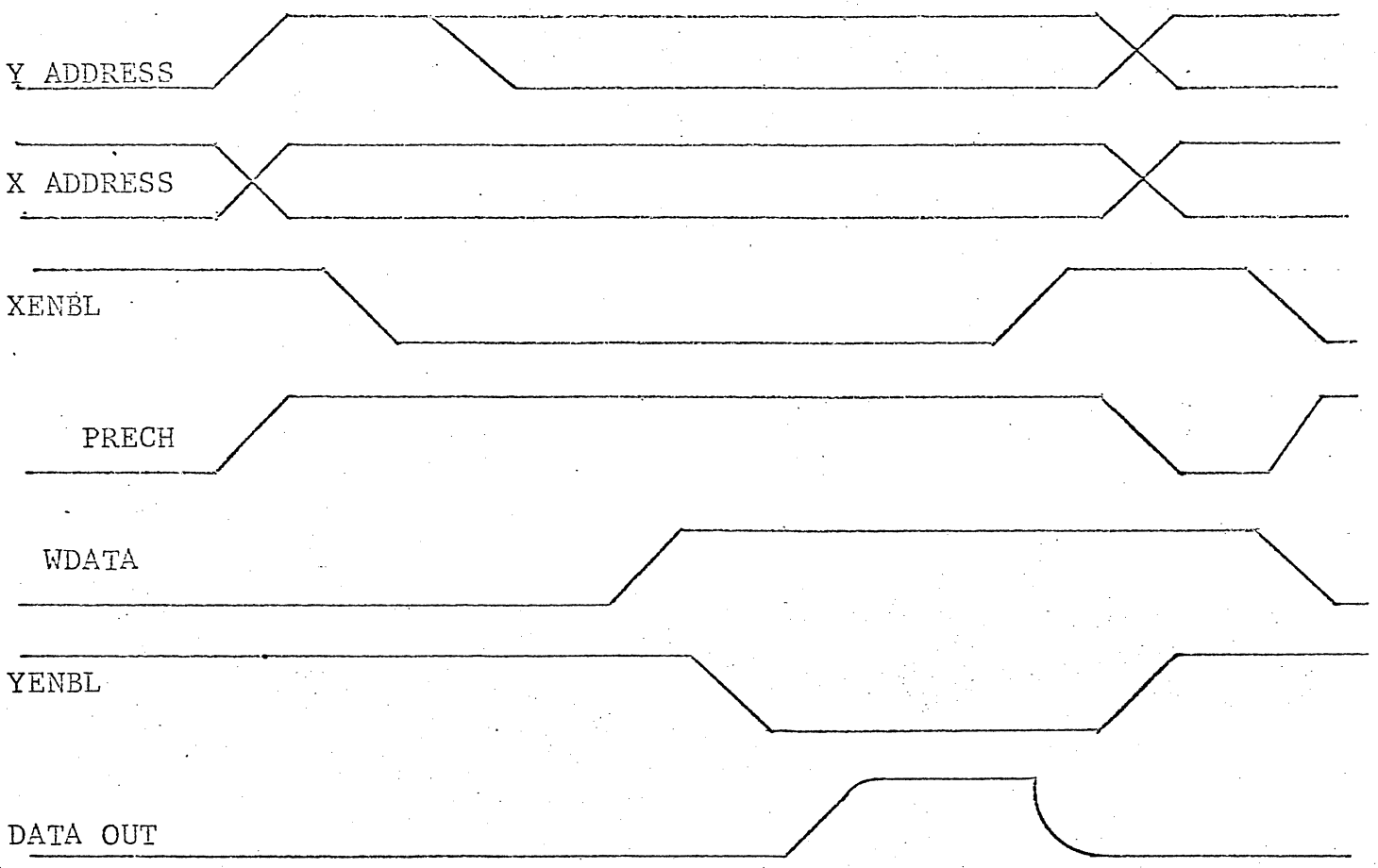


FIG. 5.C.6

TIMING DIAGRAM FOR DYNAMIC MEMORY.

TIMING : READ, REFRESH



TIMING : WRITE

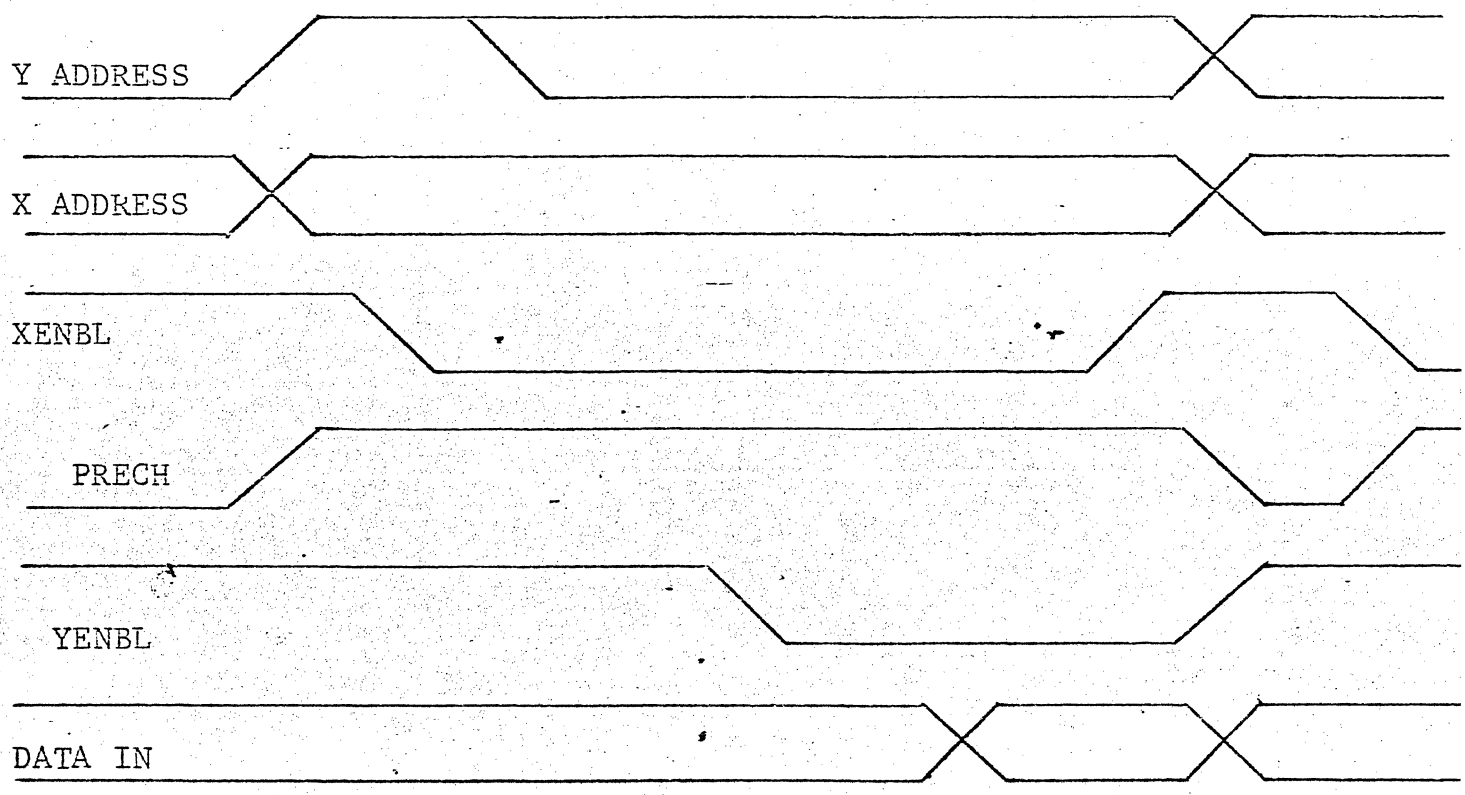
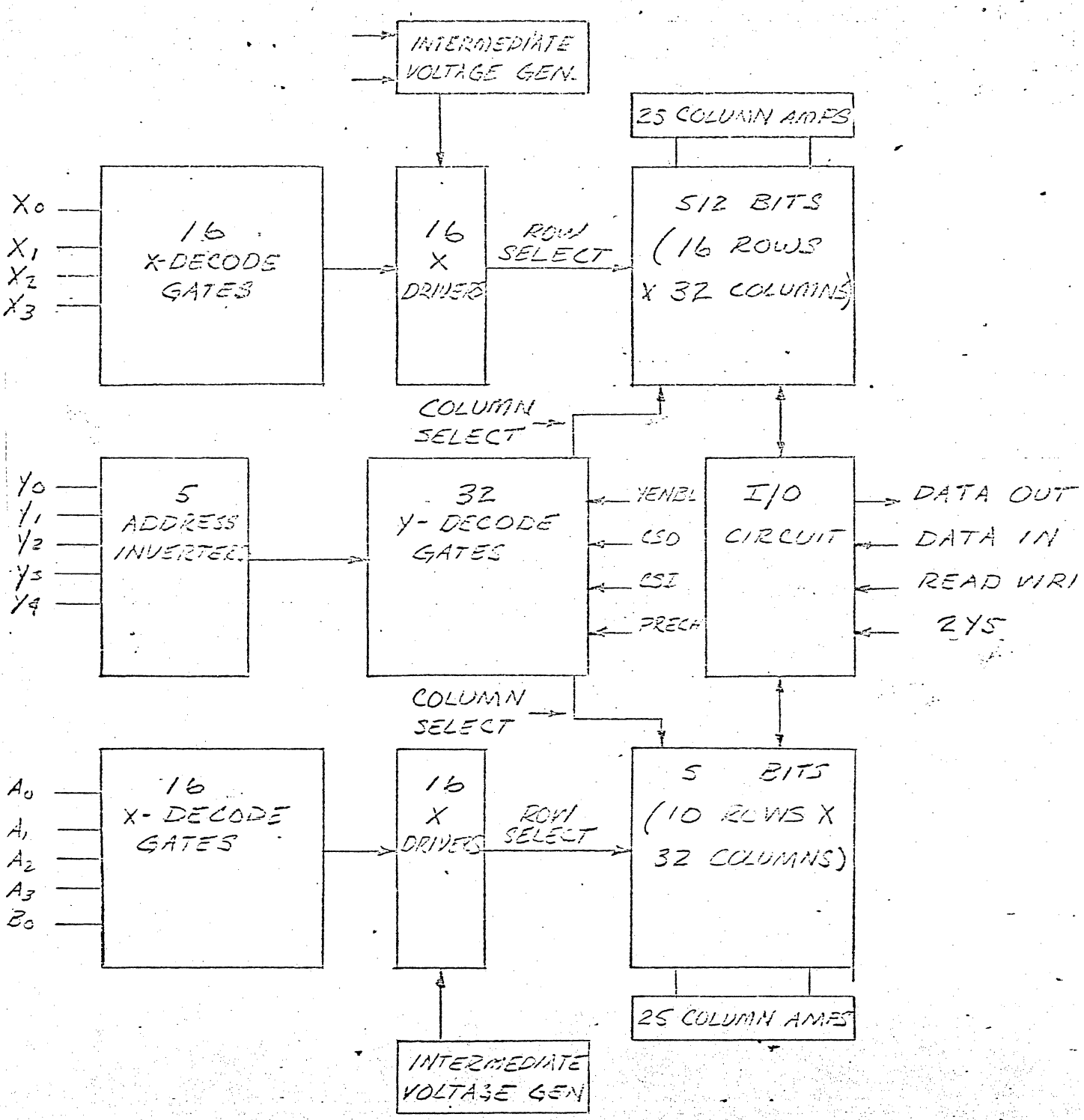


FIG. 5.C.1

BLOCK DIAGRAM



PIN COUNT

ADDRESS	10
CLOCK	3
POWER	3
DATA IN	1
DATA OUT	1
	18

Comparison of Mainframe Memory Characteristics

Table I presents a comparison of typical characteristics that can be expected from mainframe memories implemented with cores, bipolar, and MOS technologies. The access times for dynamic MOS memories can be expected to decrease to less than 200 ns within a year.

TABLE I

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COMPARISON OF MAINFRAME CHARACTERISTICS

	FERRITE CORES	BIPOLAR	DYNAMIC MOS	STATIC MOS
Cycle Time	600 ns	150 ns	700 ns	300 ns
Access Time	320 ns	50-100 ns	600 ns	200 ns
Total Power Dissipation	300W	200W	50W	100W
Word Drive Current	400 mA	5-10 mA	100 mA (charging)	100 mA (charging)
Word Drive Voltage	25V	2V	5-20V	5-20V
Sense Voltage	20-50 mV (pulse)	1-5V	5-20V	5-20V
Cell Spacing	25 × 25 mils	8 × 8 mils	2 × 4 mils	6 × 6 mils

II. READ ONLY MEMORIES

In general all memories serve the same purpose regardless of the type or category. That is they are a warehouse for storing information for use at a later time. As the name read only implies this type of memory stores permanent unalterable information, where as the read-write type allows the user to change the stored information at his discretion. The usefullness of read only memories (ROM's) have found their way into many situations such as micro programs, look up table, character generators, patch panel controls, logic simulation, etc. The limit for their utilization is controlled entirely by the design engineers ingenuity. The metal oxide semiconductor (MOS) memory has taken on a large portion of the market place because it offers three basic and distinct advantages.

1. Cost per bit is very economical and is expected to get even better.
2. Compactness combined with the ability to have a chip decode logic.
3. Ease with which the stored information can be altered, such as a single process step and even this is expected to be improved to a post process electrical programming.

It can be said that the prime purpose of ROM's are those situations where there is a need to store information that has to be repeated with random use in a particular system.

The types of ROM's that are prevalent today are a function of the type of operation and the expected end use. Operation types fall into three categories:

1. Dynamic; either 2Ø or 4Ø operation and must be continually clocked and the inputs and outputs must be synchronized to the appropriate clock times.
2. Static; this type is capable of indefinite DC operation on both inputs and outputs.
3. Latching; this is somewhat of a hybrid of the above two, that is the input is strobed in and the outputs remain static until a new address is received.

The above mentioned operational types are normally the designers choice but even they are dictates to a degree by what the end use is to be. The type of ROM such as arrangement and capacity is always determined by its expected end use in a system. The present market place is being supplied by ROM's that fall into three categories such as:

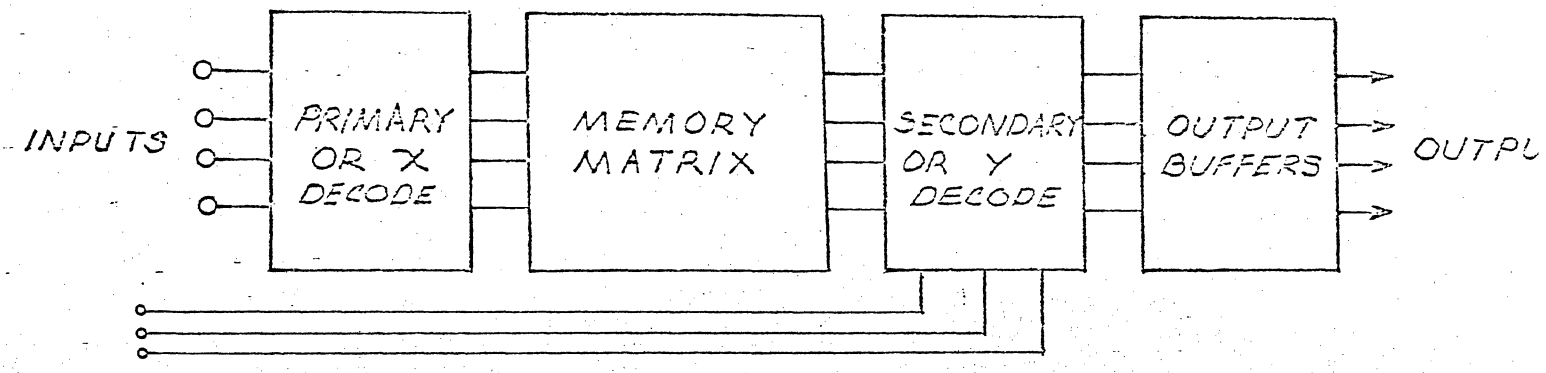
1. Conventional: These are memories that have a capacity that is a 2^{nth} factor and fully decoded for 2^n words with an appropriate bit length. For instance:

Capacity	Word-Bit Options
1024	1024x1
	512x2
	256x4
	128x8
2048	2048x1
	1024x2
	512x4
	256x8
4096	4096x1
	2048x2
	1024x4

2. Specialized: These are memories that are designed for special jobs such as character generators and code converters. They may or maynot have capacities that are a 2^{nth} factor. For instance character generators are 2240 bits and 2560 bit capacities with word lengths of 5,7,8, and 10 bits. Whereas a Hollerith to ASCII converter would have 1024 bit capacity and a 12 bit input and 8 bit output, and would require a programmable decode section.

3. Custom: ROM's of this type are specifically designed to meet the peculiar requirements of a given customer.

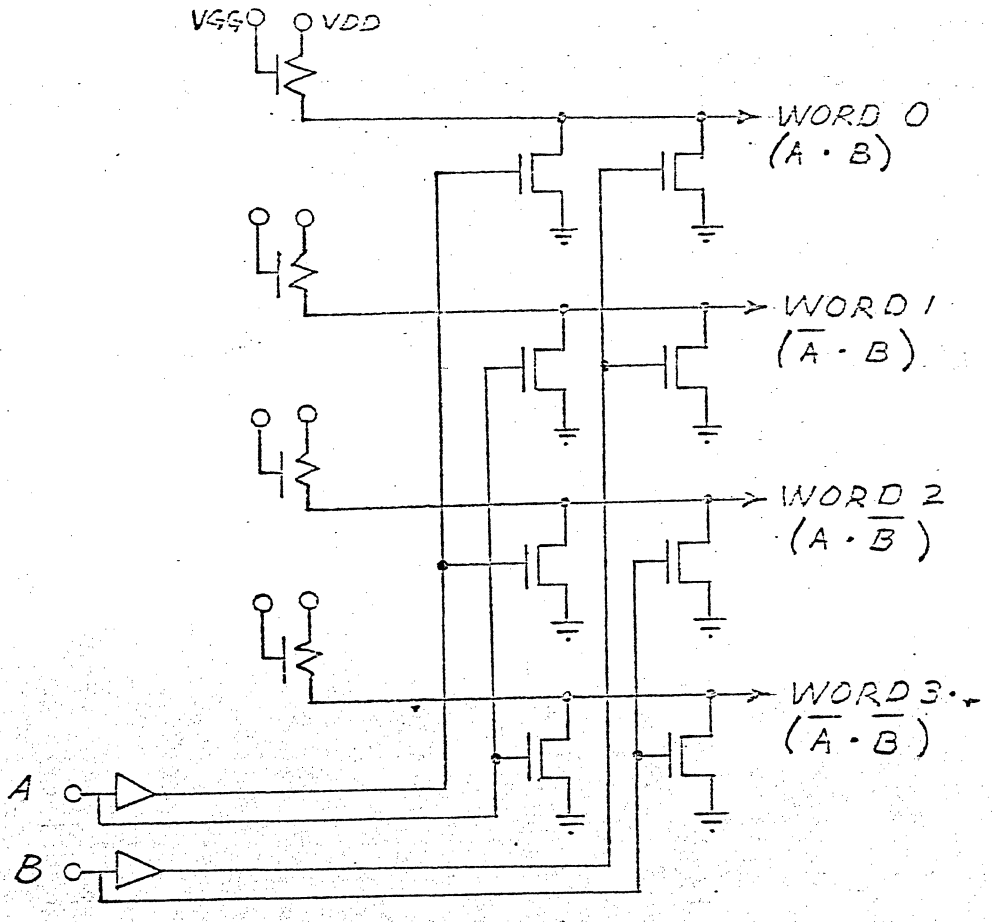
All ROM's regardless of the type or category they fall in can normally be broken in four basic sections as shown in the block diagram below.



The X decode is composed of a network of multiple gates that when given a specific binary input they supply a signal to the gates of one line in the X direction of matrix. This inturn then causes information to come out of all the Y terminals of the matrix in accordance with how the matrix has been programmed. This information is then further decoded to pass only the appro-

priate information to the buffer section that amplifies the signal to a useable level for the outside world.

The manner in which each section is designed is for the most part controlled by functional requirments and chip size. If the ROM is to be static the decode sections will be multiple input NOR gates. Each input is connected to the appropriate true or false side of an input line in a direct binary word fashion. This is illustrated in the four word decoder schematic below:



CHAPTER VII

PROCESS PARAMETER VARIATIONS

The inputs to the MOS device model are listed below:

To = Oxide thickness
ND = Substrate doping
Vto = Extrapolated threshold voltage
Z = Device length
yo = P^+ -P^+ spacing (device width)
X_j = junction depth
AF = Low field mobility reduction factor

The probability distributions of these parameters is very important in worst-case analysis because of the strong dependence of cell size upon worst-case limits. For this reason, data is presently being gathered on these distributions. Samples are shown on the graphs which follow.

An example of their use is shown below for 3-5Ω-cm, ⟨111⟩, 1200Å gate oxide process:

Suppose a logic cell would be twice as large for a two volt variation in Vt as it would for a one volt variation.

A. From table I, what would be the % loss if a one volt interval were used?

ANS: The one volt interval (Vt @ 1 0Ma) -3.2 to -4.2 volts indicates that 97.71% of the wafers would be in the interval. Thus only 2.29% of the wafers would fail because of Vt variation.

B. What would be the % loss if there was a uniform shift in the Vt distribution of -.3 volts?

ANS: If the cell were designed to operate between -3.2 and -4.2 volts, table II shows that after a -.3 volt shift, the percentages related to the relevant intervals would be:

3.1 - 3.2	16.70%
3.2 - 3.3	16.40%
3.3 - 3.4	11.40%
3.4 - 3.5	8.03%
3.5 - 3.6	5.40%
3.6 - 3.7	3.21%
3.7 - 3.8	1.35%
3.8 - 3.9	1.05%
3.9 - 4.0	3.21%
4.0 - 4.1	0.33%
4.1 - 4.2	0.33%
	64.20%

Thus 35.8% of the wafers would now fail.

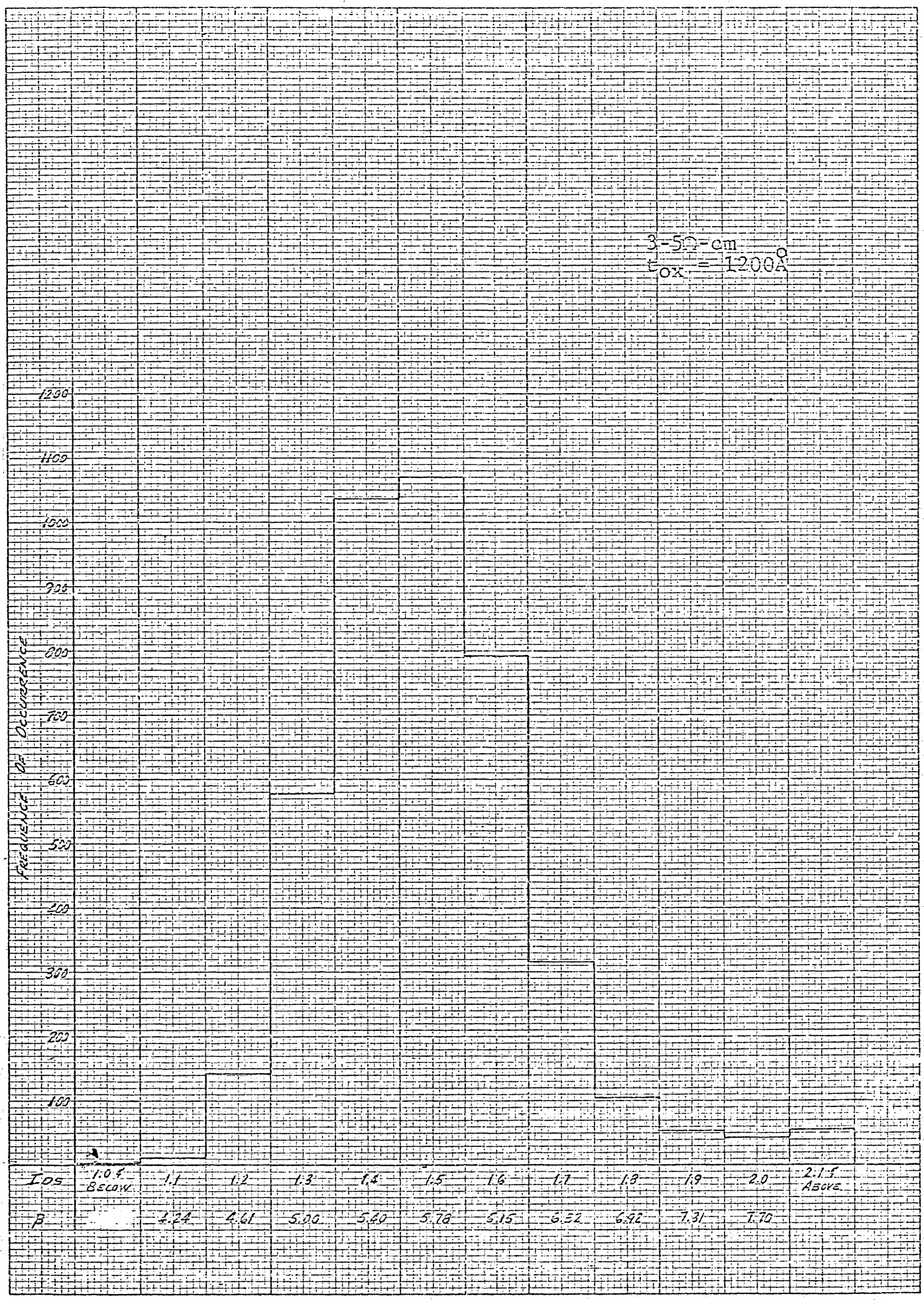
TABLE I

V_T INTERVAL	% Wafers IN INTERVAL	INTERVAL
0.0	16.70	3.5 - 3.5
0.1	33.35	3.4 - 3.5
0.2	49.75	3.4 - 3.6
0.3	61.15	3.4 - 3.7
0.4	72.27	3.3 - 3.7
0.5	80.30	3.3 - 3.8
0.6	86.70	3.2 - 3.8
0.7	92.10	3.2 - 3.9
0.8	95.31	3.2 - 4.0
0.9	96.66	3.2 - 4.1
1.0	97.71	3.2 - 4.2
1.1	98.50	3.1 - 4.2
1.2	98.83	3.1 - 4.3
1.3	99.16	3.1 - 4.4
1.4	99.40	3.0 - 4.4
1.5	99.58	3.0 - 4.5
1.6	99.76	3.0 - 4.6
1.7	99.85	3.0 - 4.7
1.8	99.94	3.0 - 4.8
1.9	99.97	3.0 - 4.9
2.0	100.00	3.0 - 5.0

TABLE II

Vt INTERVAL	% IN INTERVAL
3.0 - 3.1	0.24
3.1 - 3.2	0.79
3.2 - 3.3	6.40
3.3 - 3.4	11.12
3.4 - 3.5	16.70
3.5 - 3.6	16.40
3.6 - 3.7	11.40
3.7 - 3.8	8.03
3.8 - 3.9	5.40
3.9 - 4.0	3.21
4.0 - 4.1	1.35
4.1 - 4.2	1.05
4.2 - 4.3	0.33
4.3 - 4.4	0.33
4.4 - 4.5	0.18
4.5 - 4.6	0.18
4.6 - 4.7	0.09
4.7 - 4.8	0.09
4.8 - 4.9	0.03
4.9 - 5.0	0.03

P FREQUENCY DISTRIBUTION FOR <111> NONE – EPI



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CHAPTER VIII

MOS DEVICE MODELS

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MOS Equations

In Grove's derivation[1] of the current-voltage relationship for n-channel MOS devices, all potentials are referenced to the bulk. The equation for the voltage drop across an elemental section of the channel is given by:

$$dV = \frac{-I_D dy}{Z\mu_n Q_n(y)} \qquad 1\text{-}1$$

The drain current can be solved for by integrating $I_D dy$ from Y=0 to Y=L:

$$\int_0^L I_D d_y = Z\mu_n \int_{V(0)}^{V(L)} \left[-Q_n(y)\right] dy \qquad 1\text{-}2$$

therefore,

$$I_D = \mu_n \frac{Z}{L} \int_{V(0)}^{V(L)} \left[-Q_n(y)\right] dV \qquad 1\text{-}3$$

From Grove's derivation, $-Q_n(y)$ can be written as follows:

$$-Q_n(y) = C_O \left[V_{GB}-V_{FB}-2\phi_{fp}-V(y)\right] - \sqrt{2K_S\epsilon_o qN_A \left[V(y)+2\phi_{fp}\right]} \qquad 1\text{-}4$$

where all potentials are referenced to the bulk. Then different from Grove's approach, one can solve the integral for I_D assuming there is a source to bulk voltage. Substituting in the equation for $-Q_n(y)$, the equation for I_D becomes:

$$I_D = \mu_n \frac{Z}{L} \int_{V_{SB}}^{V_{DB}} \left\{ \left[V_{GB}-V_{FB}-2\phi_{fp}-V(y) \right] C_O - \sqrt{2K_S\epsilon_o qN_A \left[V(y)+2\phi_{fp}\right]} \right\} dV \qquad 1\text{-}5$$

Wang[2] has integrated the above equation and his results are:

$$I_D = \mu_n \frac{Z}{L} C_O \left\{ \left[V_{GS}-V_{FB}-2\phi_{fp} \right] V_{DS} - \frac{V_{DS}^2}{2} - \frac{2}{3C_O} \sqrt{2K_S\epsilon_o qN_A} \left[(V_{DS}+V_{SB}+2\phi_{fp})^{3/2} - (V_{SB}+2\phi_{fp})^{3/2} \right] \right\} \qquad 1\text{-}6$$

The drain conductance is defined as:

$$G_{DS} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=\text{constant}} \qquad 1\text{-}7$$

Differentiating the equation for I_D with respect to V_{DS} results in the following equation:

$$G_{DS} = \mu_n \frac{Z}{L} C_O \left\{ \left[V_{GS} - V_{FB} - 2\phi_{fp} \right] - V_{DS} - \frac{2}{3 C_O} \sqrt{2K_S \epsilon_o q N_A} \left[\frac{3}{2} (V_{DS} + V_{SB} + 2\phi_{fp})^{1/2} \right] \right\} \qquad 1\text{-}8$$

Threshold voltage is defined as the gate voltage when the drain conductance is zero and the drain to source voltage is zero. Wang's result is:

$$V_T = V_{GS} \Big|_{\substack{G_{DS}=0 \\ V_{DS}=0}} = V_{FB} + 2\phi_{fp} + \frac{\sqrt{2K_S \epsilon_o q N_A}}{C_O} (V_{SB} + 2\phi_{fp})^{1/2} \qquad 1\text{-}9$$

V_{TO} is defined as the threshold voltage for zero source to bulk voltage:

$$V_{TO} = V_{FB} + 2\phi_{fp} + \frac{\sqrt{2K_S \epsilon_o q N_A}}{C_O} (2\phi_{fp})^{1/2} \qquad 1\text{-}10$$

By subtracting equation (1-10) from equation (1-9), V_T can be written in terms of V_{TO}:

$$V_T = V_{TO} + \frac{\sqrt{2K_S \epsilon_o q N_A}}{C_O} \left[(V_{SB} + 2\phi_{fp})^{1/2} - (2\phi_{fp})^{1/2} \right] \qquad 1\text{-}11$$

Equation (1-11) is the same equation used by Crawford.

To simplify the current equation, the last term on the right side of equation (1-6) can be expanded:

$$f(V_{DS}) = \frac{2}{3C_O}\sqrt{2K_S\epsilon_o qN_A}\left[(V_{DS}+V_{SB}+2\phi_{fp})^{3/2} - (V_{SB}+2\phi_{fp})^{3/2}\right] \qquad 1\text{-}12$$

$$f(V_{DS}) = \frac{2}{3C_O}\sqrt{2K_S\epsilon_o qN_A}\left[\frac{3}{2}\left(1+\frac{V_{SB}}{2\phi_{fp}}\right)^{1/2}\left(\frac{V_{DS}}{2\phi_{fp}}\right) + \frac{3}{2}\cdot\frac{1}{2}\left(1+\frac{V_{SB}}{2\phi_{fp}}\right)^{-1/2}\left(\frac{V_{DS}}{2\phi_{fp}}\right)^2 + \ldots\right](2\phi_{fp})^{3/2}$$

Since the linear region implies $V_{DS} < 2\phi_{fp}$ [ref.2] the higher order terms of $(V_{DS}/2\phi_{fp})$ are neglected:

$$f(V_{DS}) = \frac{\sqrt{2K_S\epsilon_o qN_A}}{C_O}(2\phi_{fp}+V_{SB})^{1/2}V_{DS} \qquad 1\text{-}13$$

Then the drain current equation can be written as:

$$I_D=\mu_n\frac{Z}{L}C_O\left\{\left[V_{GS}-V_T\right]V_{DS}-\frac{V_{DS}^2}{2}\right\} \qquad 1\text{-}14$$

Where $V_T=V_{FB}+2\phi_{fp}+\frac{\sqrt{2K_S\epsilon_o qN_A}}{C_O}(V_{SB}+2\phi_{fp})^{1/2}$

This equation is the same as the equation used by Crawford.[3]

The saturation voltage can be solved for as done by Wang and his result is:

$$V_{Dsat}=V_{GS}-2\phi_{fp}-V_{FB}+\frac{\epsilon_o K_S qN_A}{C_O^2}\left[1-\sqrt{1+\frac{2C_O^2}{K_S\epsilon_o qN_A}(V_{GS}-V_{FB}+V_{SB})}\right]$$

This completes the list of equations which will be discussed in the computer simulation section of this report.

The equations have been derived for n-channel devices. The equations are more easily handled for n-channel devices because the mathematician does not need to worry about raising negative quantities to fractional powers. The equations for n-channel devices can be changed to p-channel

equations by using absolute values of the negative potentials which are raised to fractional powers. This will require throwing in a few sign changes external to the absolute value quantities to assure the equation is altered in the proper direction, negative or positive. A list of the p-channel equations will follow:

$$I_D=\mu_{PL}\frac{Z}{L}C_O\left\{\left[V_{GS}-V_{FB}-2\phi_{fn}\right]V_{DS}-\frac{V_{DS}^2}{2}-\frac{2}{3C_O}\sqrt{2K_S\epsilon_o qN_D}\left[\left|V_{DS}+V_{SB}+2\phi_{fn}\right|^{3/2}-\left|V_{SB}+2\phi_{fn}\right|^{3/2}\right]\right\} \quad 1\text{-}6a$$

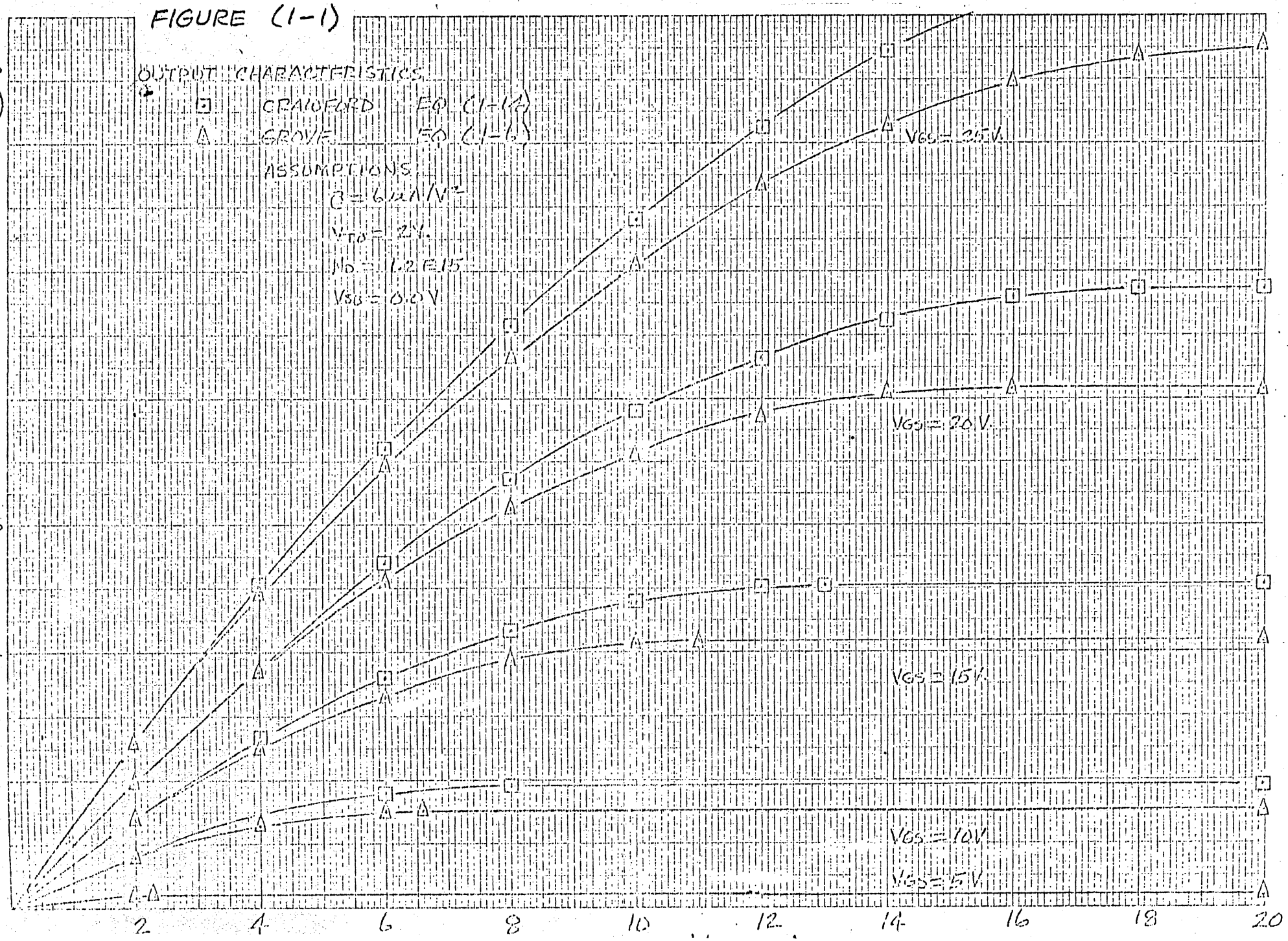
$$V_T=V_{FB}+2\phi_{fn}-\frac{\sqrt{2K_S\epsilon_o qN_D}}{C_O}\left|V_{SB}+2\phi_{fn}\right|^{1/2} \quad 1\text{-}9a$$

$$V_T=V_{TO}-\frac{\sqrt{2K_S\epsilon_o qN_D}}{C_O}\left[\left|V_{SB}+2\phi_{fn}\right|^{1/2}-\left|2\phi_{fn}\right|^{1/2}\right] \quad 1\text{-}11a$$

$$V_{Dsat}=V_{GS}-2\phi_{fn}-V_{FB}-\frac{\epsilon_o K_S qN_D}{C_O^2}\left[1-\sqrt{1-\frac{2C_O^2}{K_S\epsilon_o qN_D}(V_{GS}-V_{FB}+V_{SB})}\right] \quad 1\text{-}15a$$

Equation 1-14 is a simplified form of equation 1-6. Equation 1-14 is Crawford's equation describing the drain current in the triode region. The drain characteristic curves are plotted in figure 1-1 for equation 1-14 and equation 1-6. The curves were calculated assuming the equations were valid up to the saturation voltage and constant for higher voltages. Crawford assumes saturation begins at the point when $V_{DS}=(V_{GS}-V_T)$. Equation 1-6 was plotted assuming equation 1-15 described the saturation voltage. The comparison of the output characteristics show a 14% difference at higher drain voltages.

FIGURE (1-1)



Crawford's equation does not include the doping concentration N_D for $V_{SB}=0$. If there is a source to bulk voltage, N_D is included in ΔV_{TH} and therefore is involved in the drain current equation. Grove's equation involves N_D more directly. For the $V_{SB}=0$ case, current decreases 10% for a 150% increase in N_D.

Chapter 2

MOBILITY DEGRADATION

An essential part of the MOS device model is the gain parameter or forward-transfer-conductance ratio. The transconductance is defined as the ratio of a small change in drain current to a small change in gate voltage with the drain voltage constant.

$$gm = \left.\frac{\partial I_D}{\partial V_G}\right| \quad V_D = \text{constant} \qquad 2\text{-}1$$

Differentiating (Eq1-14) with respect to V_G yields the following equation for transconductance in the triode region:

$$gm = \beta \frac{W}{L} V_{DS} \qquad \text{[Triode Region]} \qquad 2\text{-}2$$

A similar expression can be written for the saturation region from equation (1-16):

$$gm = \beta \frac{W}{L} (V_G - V_{TO}) \qquad \text{[Saturation Region]} \qquad 2\text{-}3$$

The β parameter is obviously an important part of the gain parameter. It is the variation of this parameter with operating conditions that is the focus of this chapter.

The gain of an MOS device is directly proportional to β, which is dependent on mobility, oxide thickness and the oxide dielectric constant:

$$\beta = \mu C_O = \frac{\mu \varepsilon_{ox}}{t_{ox}} \qquad 2\text{-}4$$

The oxide thickness is a well controlled process parameter, which means the variation in β with operating conditions is a direct function of mobility variation.

Mobility of carriers in MOS devices has been under investigation for a number of years. There are a number of effects taking place at semiconductor surfaces that are not well understood. To help understand how each effect reduces mobility, the effects are considered independently. The first is the reduction of bulk mobility to surface mobility. Leistiko, Grove and Sah[4] reported extensive measurements of electron and hole mobilities in inversion layers on thermally oxidized silicon surfaces. They concluded that surface mobility is approximately equal to one half the bulk mobility and a constant value up to surface fields of 1.5×10^5 volts/cm. It is therefore reasonable to calculate bulk mobility as a function of impurity concentration and then reduce bulk mobility by a constant to get surface mobility.

$$\mu_{surface} = \mu_{bulk} \cdot K \qquad 2\text{-}5$$

This reduction of bulk mobility to surface mobility has been attributed to the additional scattering mechanisms associated with the presence of the surface and to excess charge being immobilized in surface states. For normal electric fields in excess of 1.5×10^5 volts/cm, the reduction of bulk mobility to surface mobility is no longer constant. This, therefore, suggests the following model:

$$\text{when } E_x = \frac{V_G - V_{TO}}{t_{ox}} \geq 1.5 \times 10^5 \text{ volts/cm} \qquad 2\text{-}6$$

$$\mu_{surface} = \mu_{bulk} \cdot K \cdot y$$

γ is the normal field reduction factor.

There are a number of methods of deriving γ (the normal field mobility reduction factor). The methods of Crawford, Wang and Bentchkowsky will be presented in sufficient detail to ascertain the strengths and weakness of each method.

Crawford[3] has developed an empirical relation expressing mobility as a function of applied gate voltage by adjusting the measured values of incremental drain resistance (triode region) to the theoretical values of incremental drain resistance. The incremental drain resistance in the triode region, r_{dt}, is defined as the ratio of a small change in drain voltage to a small change in drain current:

$$r_{dt} = \frac{\partial V_D}{\partial I_D} \qquad 2\text{-}7$$

The expression for drain current in the triode region is given by equation (1-14):

$$I_D = -\beta\left[(V_G - V_T)\, V_D - 1/2\, V_D^2\right] \qquad 2\text{-}8$$

The drain conductance in the triode region can be calculated by differentiating the equation for drain current with respect to drain voltage:

$$\frac{\partial I_D}{\partial V_D} = -\beta\left[(V_G - V_T) - V_D\right] \qquad 2\text{-}9$$

If the drain voltage is near the origin, the drain conductance becomes:

$$\frac{\partial I_D}{\partial V_D} = -\beta\,(V_G - V_T) \qquad 2\text{-}10$$

Then the incremental drain resistance can be written as:

$$r_{dt} = \frac{1}{-\beta\,(V_G - V_T)} \qquad \text{(theoretical)} \qquad 2\text{-}11$$

Assuming β to be a constant, low field value, Crawford found the measured values of incremental drain resistance were greater than the theoretical values of incremental drain resistance by a constant resistance R. This can be written in equation form as:

$$r_{dt(\text{measured})} = r_{dt}\left|\begin{matrix}\text{theorectical}\\ \text{constant } \beta\end{matrix}\right| + R = \frac{1}{-\beta_0(V_G - V_T)} + R \qquad 2\text{-}12$$

where β_o is a constant, low field value

The β in the theoretical equation for incremental drain resistance is not constant but is a function of gate voltage. If the equations for theoretical and measured incremental drain resistance are set equal to each other, a normalized value for β can be obtained:

$$\frac{1}{-\beta\,(V_G - V_T)} = \frac{1}{-\beta_o(V_G - V_T)} + R \qquad 2\text{-}13$$

rearranging yield:

$$\frac{\beta}{\beta_o} = \frac{\mu}{\mu_o} = \frac{1}{1 - \beta_o R(V_G - V_T)} \qquad 2\text{-}14$$

	⟨100⟩ material	⟨111⟩ material
$\mu_o (cm^2/V\text{-}sec)$	180-200	240-250
$\beta_o R\ (\frac{1}{V})$	0.034	0.028

Table (2-1) μ_o and $\beta_o R$ for 1 to 10Ω-cm material

Crawford's mobility reduction equation has normalized mobility versus (V_G-V_T). The normal field can be written as:

$$E_x = \frac{V_G-V_T}{t_o} \quad \text{where to is oxide thickness} \qquad 2\text{-}15$$

Crawford's equation can not be written as a function of field unless the oxide thickness of his test devices is known. Since the normal field varies with oxide thickness, Crawford's equation for mobility reduction is good for devices where the oxide thickness is the same as his test devices.

Wang[2] has used the DC channel conductance technique to obtain an equation for mobility versus normal field. The equation for drain current for the triode region can be written as:

$$I_{DS} = \overline{\mu_p} \frac{Z}{L} C_O \left[(V_{GS}-V_{TO})\, V_{DS}-1/2V_{DS}^2\right] \qquad 2\text{-}16$$

and solving for $\overline{\mu_p}$, the average mobility, the equation is:

$$\overline{\mu_p} = \frac{I_{DS}}{\frac{Z}{L} C_O \left[(V_{GS}-V_{TO})\, V_{DS}-1/2V_{DS}^2\right]} \qquad 2\text{-}17$$

The DC channel conductance technique solves for $\overline{\mu_p}$ by setting V_{DS} at a small known voltage. For V_{DS}=0.1V, $\overline{\mu_p}$ can be written as:

$$\overline{\mu_p} = \frac{10\ I_{DS}}{\frac{Z}{L} C_O (V_{GS}-V_{TO})} = \frac{10\ I_{DS}}{\frac{Z}{L} \frac{ko\epsilon o}{to} (V_{GS}-V_{TO})} \qquad 2\text{-}18$$

Wang calculated the average mobility using the equation above and measuring I_{DS} and $(V_{GS}-V_{TO})$. The results when normalized compared well with Crawford's results. Wang's

equation can be written to show the mobility reduction as a function of field:

$$\bar{\mu}_P = \frac{10 I_{DS}}{\frac{ZC}{L}(V_{GS}-V_{TO})} = \frac{10 I_{DS}}{\frac{Z}{L}(k_o \epsilon_o)\left[\frac{(V_{GS}-V_{TO})}{t_o}\right]} \qquad 2\text{-}19$$

$$\text{where } \frac{V_{GS}-V_{TO}}{t_o} = E_X \text{ (normal field)}$$

The mobility was found to be constant up to a field of 10^5V/cm. This agrees with Grove and Leistiko's results. At fields greater than the critical field Ec, a curve fit was made for the mobility versus normal field. This result is used in FCP.

Bentchkowsky[5] has derived an empirical equation to predict the mobility reduction as a function MOS device characteristics. Bentchkowsky's experimental data indicated the mobility was constant up to a field of $E=6\times10^4$ and beyond this field could be approximated by:

$$\mu_{eff} = \mu_{eff}(E_{SO})\left[\frac{E_{SO}}{E_S}\right]^{C_1} \qquad 2\text{-}20$$

where $E_{SO}=6\times10^4$V/cm and $C_1=0.15$ for P channel devices. E_S is the surface field and can be expressed as a function of the total charge per unit surface area induced in the semiconductor:

$$E_{S(Y)} = \frac{Q_{S(Y)}}{K_S \epsilon_0} = -\frac{\left[V_G - V_{FB} - V_{(Y)} - 2\phi_F\right] C_O}{K_S \epsilon_0} \qquad 2\text{-}21$$

Bentchkowsky approximated $Q_S(Y)$ by finding the average value along the channel. The boundary conditions are:

Y=0 V(Y)=0

Y=L V(Y)=V_D

The average value of $Q_{S(Y)}$ can be calculated as:

$$\overline{Q_S} = \frac{\int_o^{V_D} Q_S(V)\, dV}{V_D}$$

$$\overline{Q_S} = \frac{\int_o^{V_D} -\left[V_G - V_{FB} - 2\phi_F - V\right] C_O\, dV}{V_D} \qquad 2\text{-}22$$

$$\overline{Q_S} = -\left[VG - V_{FB} - 2\phi_F - 0.5V_D\right] C_O$$

The Bentchkowsky's equation for mobility can be written as:

$$\mu eff = \mu eff\,(E_{SO}) \left[\frac{E_{SO}}{E_S}\right] C_1$$

where $\overline{E_S} = \frac{\overline{Q_S}}{K_S \epsilon_O}$

$$\mu eff = \mu eff\,(E_{SO}) = \left(\frac{E_{SO}}{-\left[V_G - V_{FB} - 2\phi_F - 0.5V_D\right]} \frac{C_O}{k_s \epsilon_o}\right)^{C_1} \qquad 2\text{-}23$$

The matching constants C_1 is an empirical fit.

Bentchkowsky's results show a higher effective mobility for a given field. The derivation does not specify if the material is <100> or <111> .

When using mobility reduction equations, there are three things which should receive special attention to avoid misuse of the equation. The first consideration should be field dependence. Bentchkowsky's and Wang's equations are in a form which allows mobility to be a function of normal field, $Ex=(V_{GS}-V_T)/t_o$. Mobility should be considered as being field dependent. Crawford's equation is written as a function of $(V_{GS}-V_T)$. The oxide thickness in Crawford's equation is included in the $\beta_o R$ factor which multiplies $(V_{GS}-V_T)$. One can alter the $\beta_o R$ factor to obtain a field dependent equation if the oxide thickness of the test devices is known. The second consideration should be material. Crawford changes the value of the $\beta_o R$ factor to account for <100> material and <111> material. Wang has two equations: One equation for <100> and one equation for <111> . Bentchkowsky's equation does not

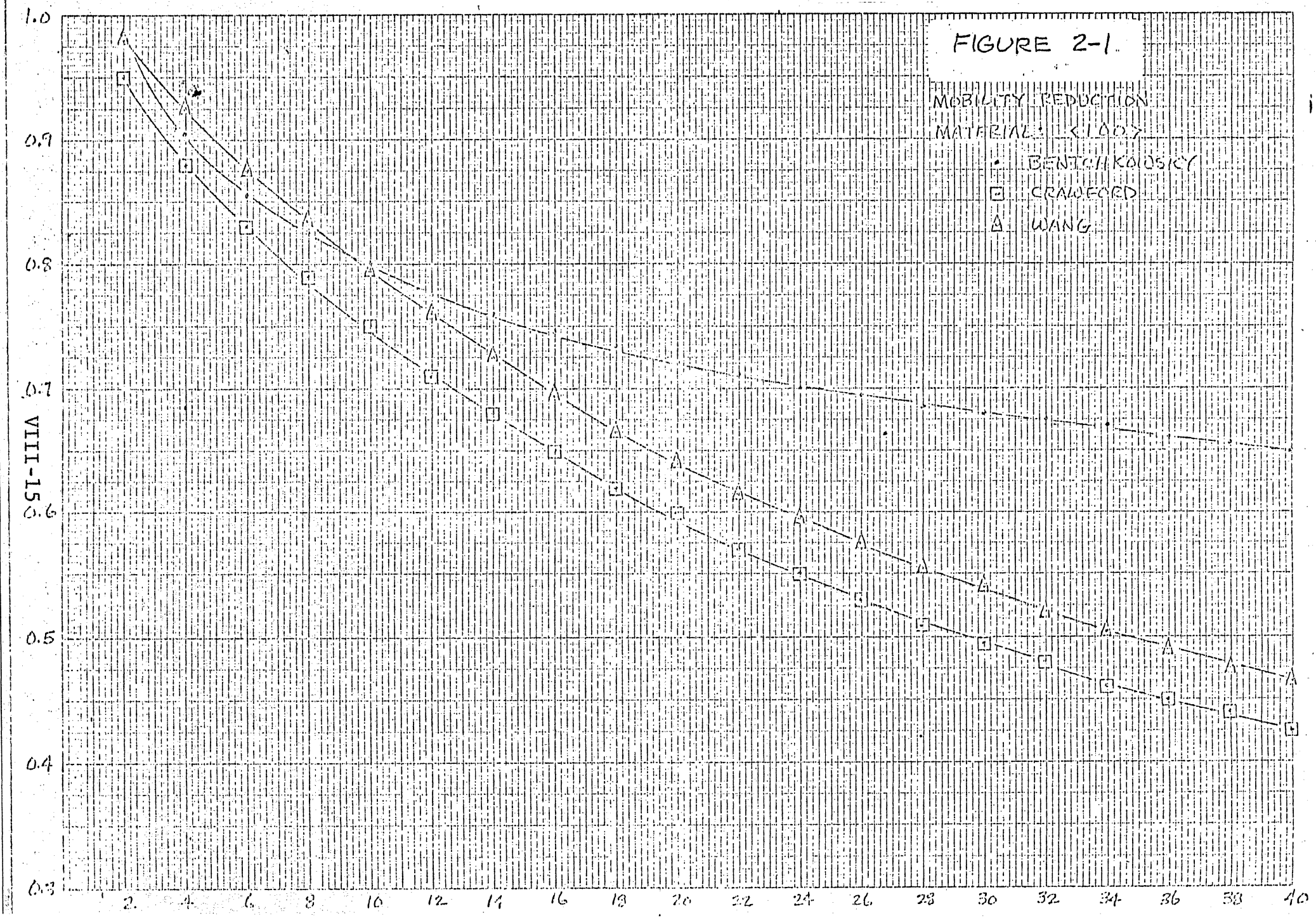
account for <100> and <111> material. The third thing which one should consider is source to bulk voltage. The source to bulk voltage can be accounted for in the (V_G-V_T) term. V_G is referenced to ground and V_T is increased by ΔV_T by the source to bulk voltage.

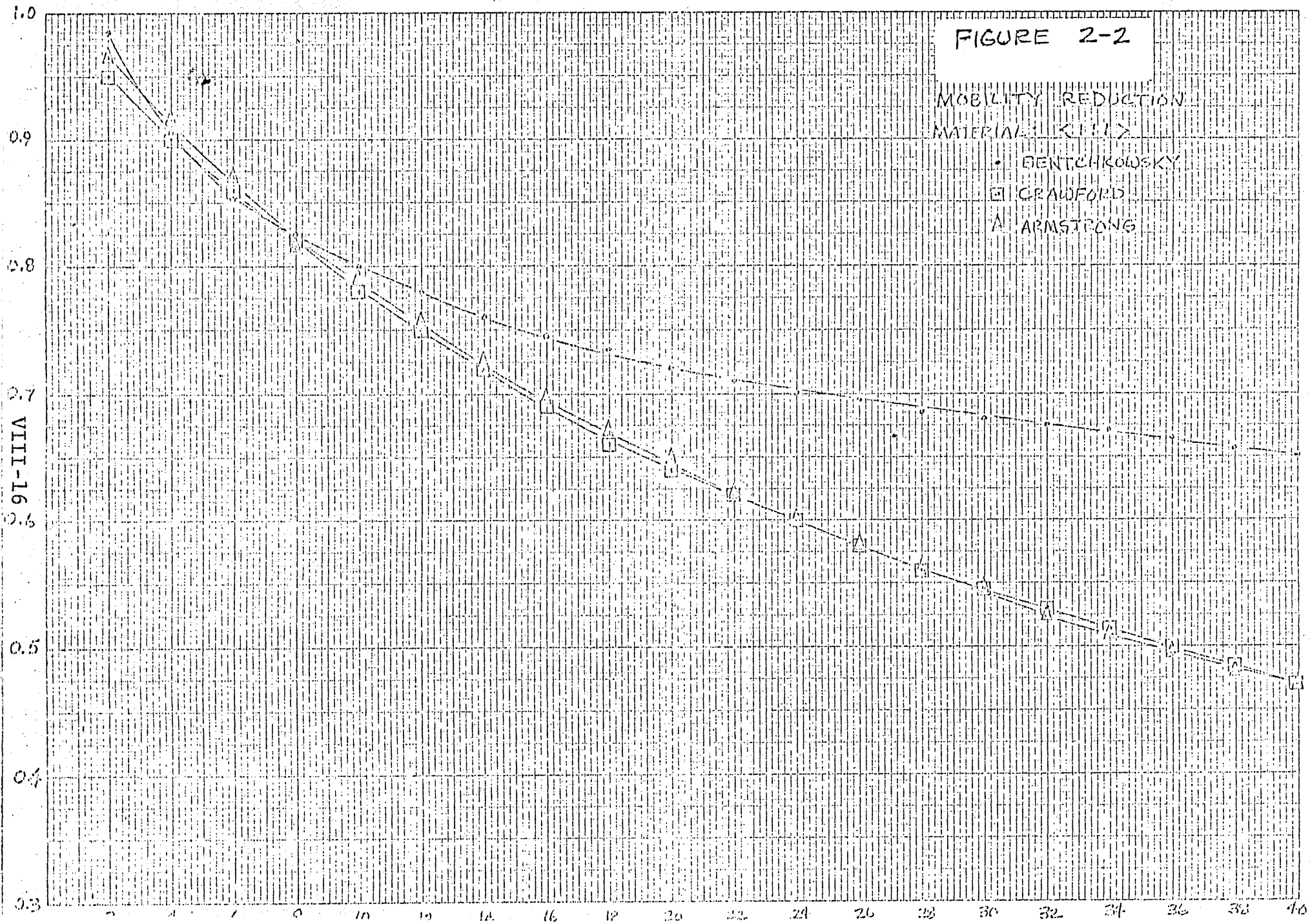
The mobility reduction equations are plotted in figure (2-1) and (2-2) for <100> and <111> material respectively. The equations are plotted versus (V_G-V_T). If the oxide thickness is known, the normal field can be calculated for a given (V_G-V_T).

The final component of surface mobility reduction is that due to the transverse field. It is well known that the carrier drift velocity will increase with increasing electric field. Shockley described the drift velocity versus electric field as three distinct regions. In figure 2-4 these three regions are identified. From data presented by Norris and Gibbons[7] a bulk mobility versus transverse electric field curve was constructed by Wang. This curve is for holes in the bulk (see Fig.2-5). In an effort to achieve a model which would account for transverse field reduction, Wang proposed the following:

$$\mu surface = \mu bulk \cdot K \cdot \gamma \cdot \delta \qquad 2\text{-}24$$

Recall that k is a constant which transforms bulk mobility to surface mobility and γ is the normal field reduction factor. δ is the transverse field reduction





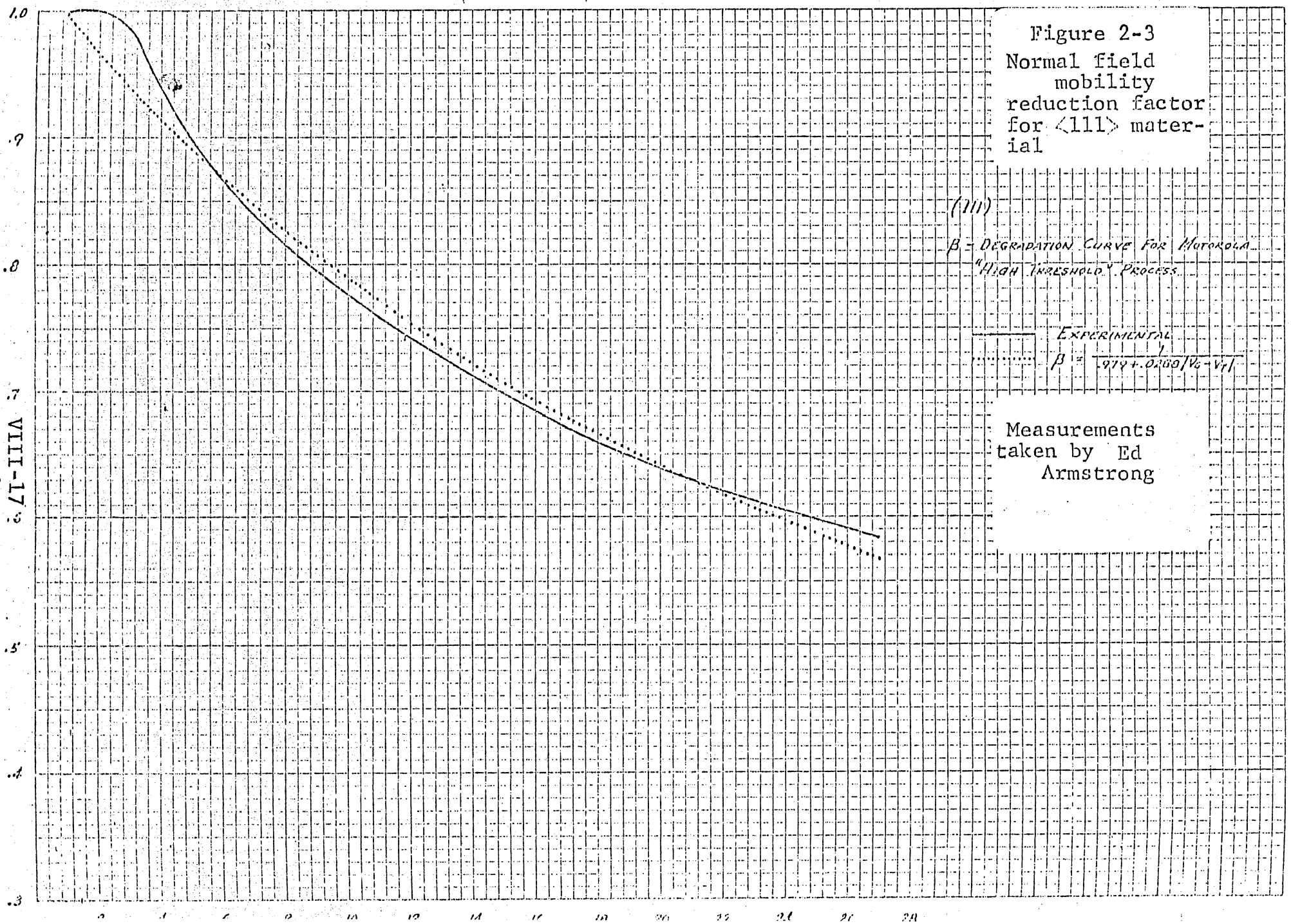


Figure 2-3
Normal field mobility reduction factor for <111> material

(111)

β = Degradation Curve for Motorola "High Threshold" Process

——— Experimental

..... $\beta = \frac{1}{.979 + .020|V_G - V_T|}$

Measurements taken by Ed Armstrong

factor. As one can see from Fig.2-5, a line equal to low field surface mobility is drawn on the bulk mobility versus field graph. The intersection of this line and the empirical curve representing bulk mobility reduction is taken to be the critical field at which the surface mobility will undergo transverse field reduction. Once this critical field is reached, the assumption is made that surface reduction would be equal to bulk reduction. In this model the field should be calculated using the voltage from drain to source until saturation occurs and V_D saturation thereafter. The distance over which this voltage is distributed is the effective channel length.

$$Ey = \frac{V_{DS}}{L} \quad \text{in the triode region}$$

$$Ey = \frac{V_D}{L_{eff}} \quad \text{saturation in the saturation region} \qquad 2\text{-}25$$

Since bulk mobility in silicon is anisotropic, Wang's tranverse field model is not dependent on crystal orientation. Although the low field mobility is different for different crystal orientations, the critical field at which the tranverse mobility reduction becomes operational will change. If this model is used in cases where the channel length is short and the drain voltage large, a very unusual and unrealistic I_D versus V_D curve results.* The dip in the I_D versus V_D curve points out that surface and bulk mobilities

*See Figure 2-6

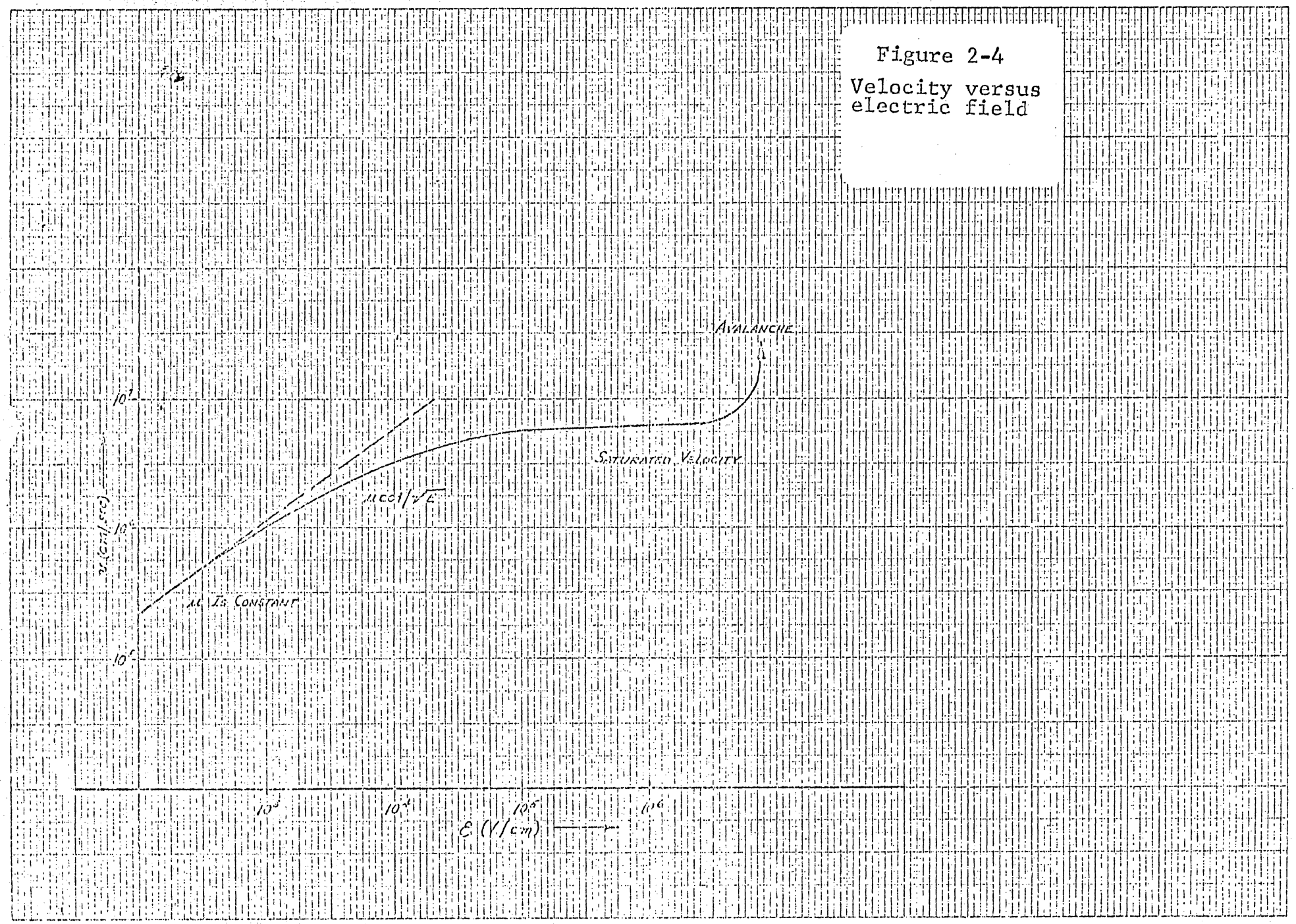


Figure 2-4
Velocity versus electric field

Figure 2-5

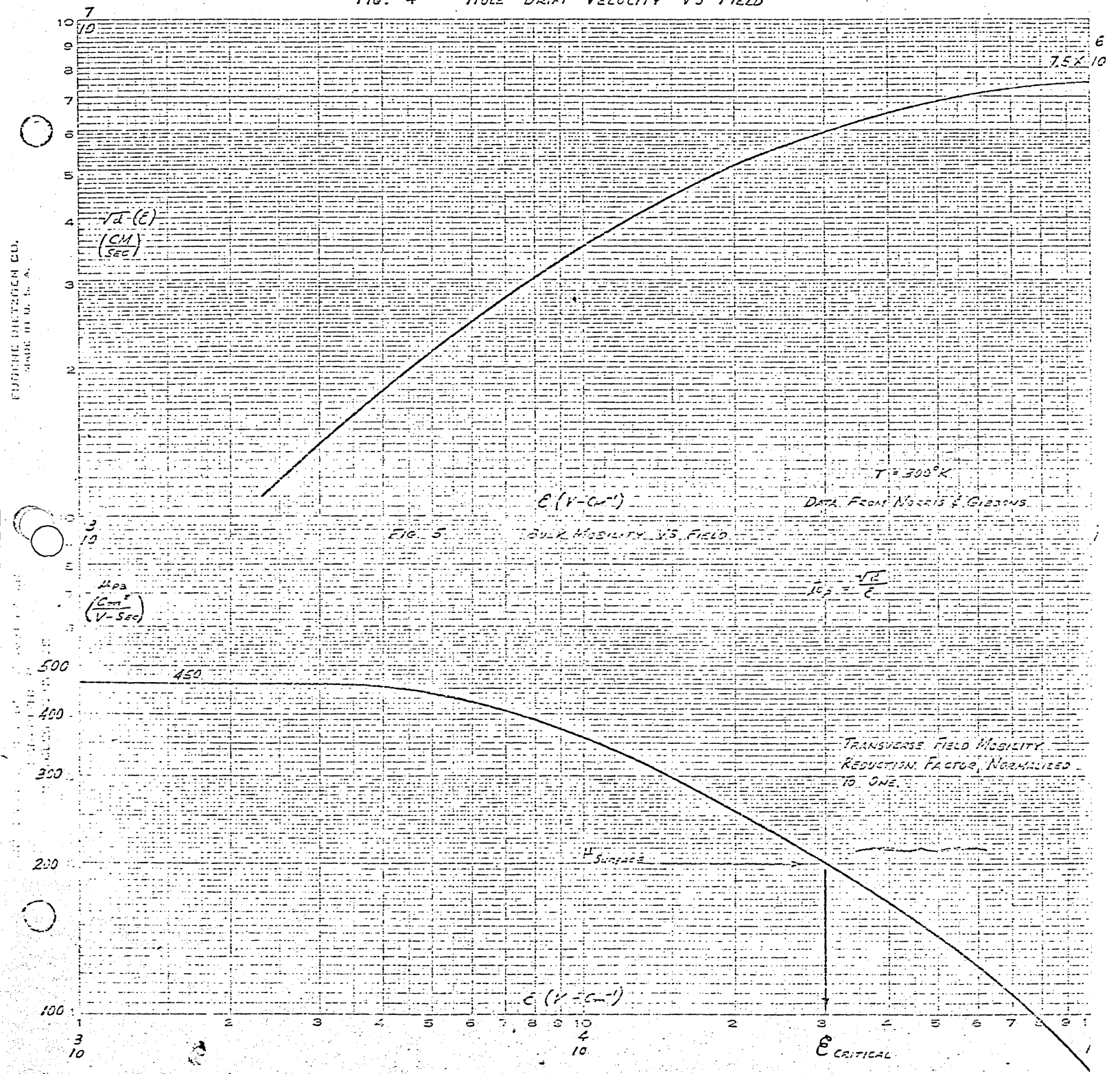


FIG. 4 HOLE DRIFT VELOCITY VS FIELD
$\sqrt{d}$ (E)
(CM/SEC)
7.5 X 10^6
E (V-CM^-1)
T = 300°K
DATA FROM NORRIS & GIBBONS
FIG. 5 BULK MOBILITY VS FIELD
μ_{pa}
$\left(\frac{Cm^2}{V\text{-}Sec}\right)$
$10^2 = \frac{\sqrt{E}}{E}$
500
450
400
300
200
100
TRANSVERSE FIELD MOBILITY REDUCTION FACTOR, NORMALIZED TO ONE.
$\mu_{Surface}$
E (V-Cm^-1)
$\mathcal{E}_{CRITICAL}$

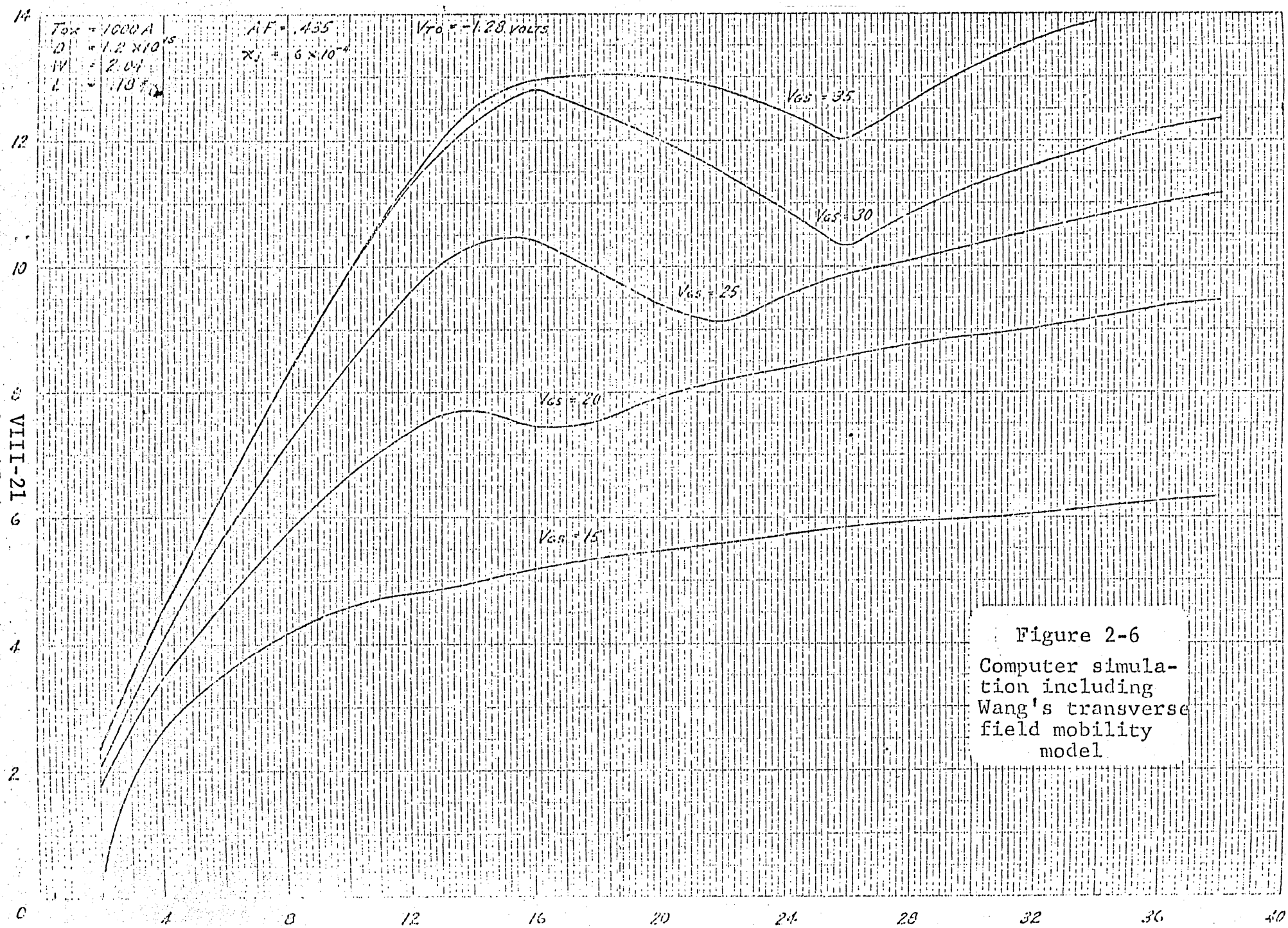


Figure 2-6

Computer simulation including Wang's transverse field mobility model

are not reduced by the same phenomena and Wang's model of transverse field mobility reduction is not useable. The most plausible explanation for the failure of this model is that the low energy scattering mechanisms are more efficient at the surface than those in the bulk and make it possible for a hole to lose the energy it gains from the electric field through collisions with the lattice. This provides that the hole can stay in thermal equilibrium at the surface for higher electric fields than possible in the bulk. The critical electric field at which the transverse field mobility reduction factor would have an effect should therefore be much higher for carriers at the surface than for carriers in the bulk. At the present time there does not seem to be a satisfactory model for transverse field mobility reduction and therefore it is our recommendation that in computer simulation this effect be neglected.

Chapter 3

Channel-Length Modulation

The drain current equation shows the current is indirectly proportional to the channel length. This makes channel-length an important parameter. The designed channel length can vary due to one of several reasons. The designed channel length, L_{DESIGN}, can be increased in length or decreased in length due to photo resist processing variations. L_{DESIGN} can be decreased by the out diffusion of the drain and source diffusions. The above changes in channel length are due to processing. The channel length can also be changed due to bias conditions. If all channel length variations are grouped together and called ΔL_{eff}, the effective channel length can be written as:

$$L_{eff} = L_{DESIGN} - \Delta L_{eff} \qquad 3\text{-}1$$

This would modify the drain current calculated for designed channel length as follows:

$$I_D' = I_D \frac{L_{DESIGN}}{L_{DESIGN}-\Delta L_{eff}} \qquad 3\text{-}2$$

The channel-length variation due to bias has been described by several authors.* Once a MOS device saturates, the voltage from the source to the point of channel pinch-off is (V_G-V_T). The remaining voltage, drain to sources, must be dropped across the depletion region between channel pinch-off and the drain. This voltage is $V_{DS}-(V_G-V_T)$.

*See Ref. 2,3,6

As this voltage increases, the depletion width increases and the channel length decreases. Then as V_{DS} increases channel length decreases and as V_G increases channel length increases.

Crawford used simple p-n junction theory to describe the depletion width versus $\left[V_{DS}-(V_G-V_T)\right]$ relationship. Then the depletion width, L' can be written as:

$$L' = \sqrt{\frac{2\epsilon_S \left[V_{DS}-(V_G-V_T)\right]}{qN}} \qquad 3\text{-}3$$

where N is the substrate doping.

Wang used Lawrence-Warner's curves for an erfc distribution to calculate the change in channel length due to bias conditions. Wang's result is:

$$L' = \sqrt[3]{\frac{2\epsilon_S \left\{V_{DS}-(V_{GS}-V_T)\right\}}{aq}} \qquad 3\text{-}4$$

where $a = \frac{N_D}{0.7x_j} \ln\left(\frac{N_O}{N_D}\right)$

Bentchkowsky and Grove have developed a more complete model describing channel length modulation due to bias conditions. They present a simple physical model which accounts for the modification of the electric field in the drain depletion region near the Si-SiO_2 interface, due to the presence of the gate electrode. They describe the depletion width as:

$$L' = \frac{V_D - V_{Dsat}}{\mathcal{E}_T} \qquad 3\text{-}5$$

where $\mathcal{E}_T$ is the transverse field component near the Si-SiO_2 surface. $\mathcal{E}_T$ is the sum of three components, $\mathcal{E}_1$, $\mathcal{E}_2$, and $\mathcal{E}_3$.

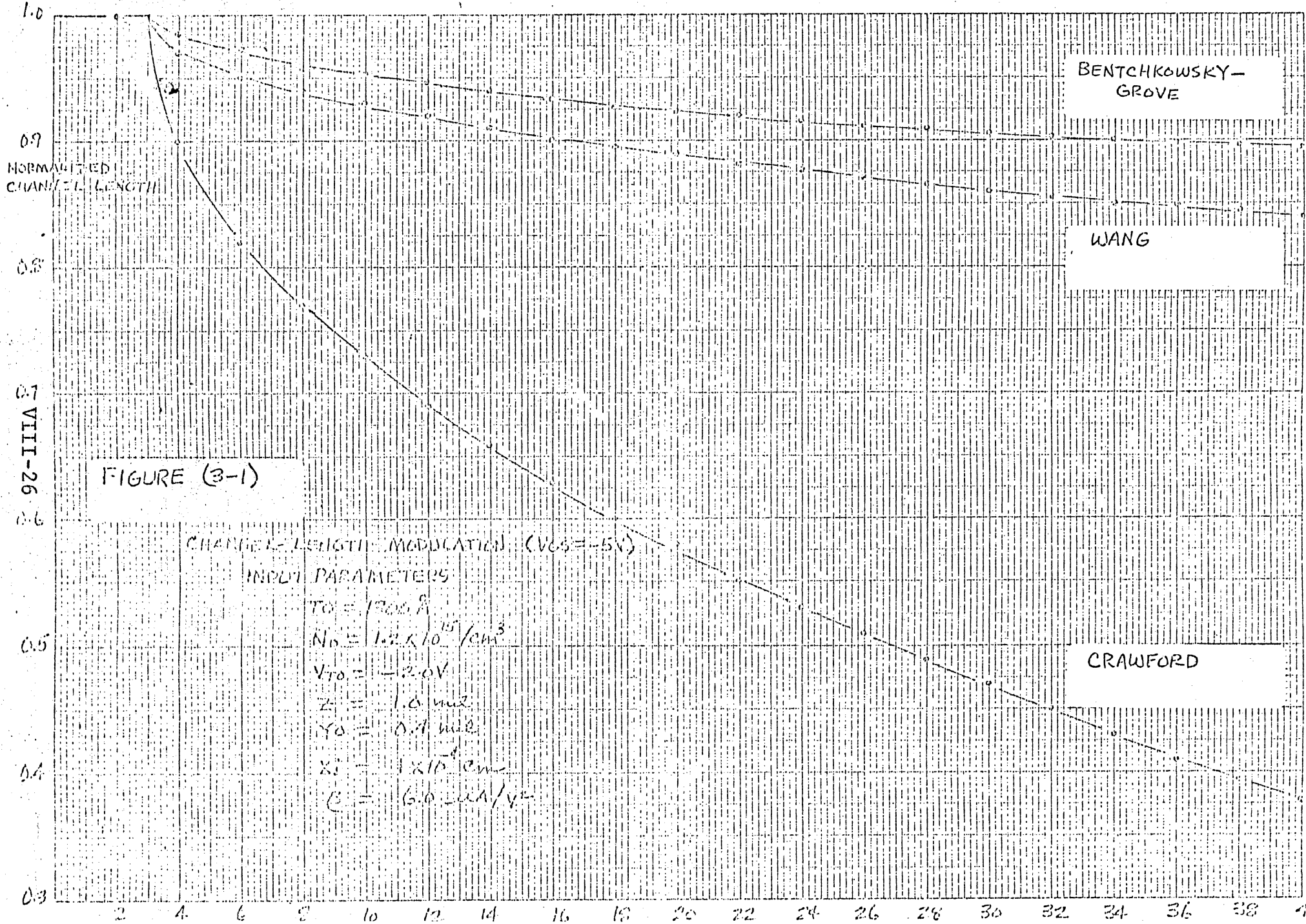


FIGURE (3-1)

Chapter 4

Computer Simulation

The equations programmed into the computer for MOS Device Simulation are as follows: (See Chapter 1)

$$I_{DS}=\frac{W}{L}\,\mu p\, C_O\left\{\left[V_{GS}-V_{FB}-2\phi_F-\frac{V_{DS}}{2}\right]V_{DS}\right. \qquad 4\text{-}1$$

$$\left.-\frac{2}{3}\,\frac{2K_S\,\epsilon_o q N_D}{C_O}\left[\left|V_{DS}+V_{SB}+2\phi_F\right|^{3/2}-\left|V_{SB}+2\phi_F\right|^{3/2}\right]\right\}$$

$$V_{D\,saturation}=V_{GS}-V_{FB}-2\phi_F \qquad 4\text{-}2$$

$$=\frac{K_S\,\epsilon_o q N_D}{C_O^{\,2}}\left[1-\sqrt{1-\frac{2C_O^{\,2}\,(V_{GS}+V_{SB}-V_{FB})}{K_S\,\epsilon_o q N_D}}\right]$$

$$V_{TO}=V_{FB}+2\phi_F-\sqrt{\frac{2K_S\,\epsilon_o q N_D\,\left|2\phi_F\right|}{C_O}} \qquad 4\text{-}3$$

$$V_T=V_{TO}-\sqrt{\frac{2K_S\,\epsilon_o q N_D\,\left|2\phi_F+V_{SB}\right|}{C_O}} \qquad 4\text{-}4$$

$$+\sqrt{\frac{2K_S\,\epsilon_o q N_D\,\left|2\phi_F\right|}{C_O}}$$

When $V_{DS} > V_D$ saturation

V_{DS} is used in the solution of equation 4-1

When $V_{DS} < V_D$ saturation

V_D saturation is used in the solution of equation 4-1

The gain parameter β can be written as follows:

$$\beta = \mu surface\, C_O = \frac{\mu surface\, \epsilon_{oxide}}{t_{oxide}}$$

and if we assume Wang's[2] mobility model, the surface mobility can be expressed as the product of four factors.

$$\mu surface = (K)\ (\mu bulk)\ (\gamma)\ (\delta) \qquad 4\text{-}5$$

K is a constant which transforms μbulk to μsurface. μbulk is the mobility of free holes in bulk silicon. γ is the normal field mobility reduction factor and δ is the transverse mobility reduction factor.

In our opinion the K factor should be maintained as one of the input parameters, even though $\beta(0)$ (low field β) is a more familiar parameter to the circuit designer. In most cases $\beta(0)$ is a measured parameter, but its measurement depends on knowing I_{DS}, V_{GS}, W, and L. The degree of uncertainty in each of the above parameters will then be the degree of uncertainty in $\beta(0)$. Since the physics of the scattering mechanism has been shown not to be a sensitive function of device geometries, bulk doping concentration, oxide thickness, channal lengths, surface charge densities or redistribution of impurities during thermal oxidation, the uncertainties in $\beta(0)$ and μsurface are believed to be due to uncertainties in the structural parameters used in their computation. (Grove, Leistiko and Sah) The following is a suggested method for calculation of K. Measure the voltage at 100μa with the gate shorted to the drain and proceed with the following calculation,

$$100 = \frac{\beta}{2}\frac{W}{L}\ (V_{GS} - V_{TO})^2 \qquad 4\text{-}6$$

$$\beta = 200 \frac{L}{W} \frac{1}{(V_{GS} - V_{TO})^2} \qquad 4\text{-}7$$

Read bulk mobility from figure 4-1.

$$\beta = \frac{\epsilon \mu surface}{t_{ox}} = \frac{\mu a}{v^2} \qquad 4\text{-}8$$

$$\mu surface = \beta\, tox\ (\text{Å})\ .0029 = \beta\, tox\ (\text{Å})\ .0029\ \frac{cm^2}{V\text{-}sec} \qquad 4\text{-}9$$

$$K = \frac{\mu surface}{\mu bulk} \qquad 4\text{-}10$$

Once K has been determined there should be no need to continually change this parameter.

μbulk is a well known quantity for silicon and the following equation is a curve fit of μbulk versus impurity level.

$$\mu bulk_{holes} = \frac{447.3}{1+\left(\frac{ND}{6.3\times10^{16}}\right)^{0.76}} + 47.7 \qquad 4\text{-}11$$

See Figure 4-1

γ is the normal field reduction factor and is crystal orientation dependent. The following are empirical equations which represent <100> and <111> P-channel MOS devices.

<100> From Wang	<111> From Armstrong
$\mathcal{E}_y = \frac{V_{GS}-V_T}{t_{ox}}$	$\mathcal{E}_y = \frac{V_{GS} - V_T}{t_{ox}}$
if $\mathcal{E}_y \geq .001025$ then $\gamma = \frac{1}{.96+39.\mathcal{E}_y}$	if $\mathcal{E}_y \geq .000561$ $\gamma = \frac{1}{.979+37.4\mathcal{E}_y}$

At the present time there is not a complete theoretical model of surface mobility, and therefore the empirical

Hole Bulk Mobility Variation With Doping In Si

Figure 4-1

μ_{MAX} ($Cm^2/V\text{-}Sec$)

500

400

300

200

100

0

$\mu_D = \frac{447.3}{1 + \left(\frac{N_D}{6.3 \times 10^{16}}\right)^{0.76}} + 47.7$

From Wang

10^{14} 10^{15} 10^{16} 10^{17} 10^{18} 10^{19}

equations are the only available descriptions of normal field mobility reduction.

δ is the tranverse field mobility reduction, which according to Wang will yield the following result for <100> material,

$$\mathcal{E}_y = \frac{[V]}{Leff} \qquad \text{where } V=V_{DS} \text{ in the triode region} \qquad 4\text{-}12$$

$V=V_D$ saturation in the saturation region

<100>	<111>
$\mathcal{E}_y \geq 81.5$ V/mil	$\mathcal{E}_y \geq 76.0$ V/mil
$\delta = \frac{10.}{2.88+.0874(\mathcal{E}y)}$	$\delta = \frac{10.}{3.36+.0874(\mathcal{E}y)}$

This model of transverse field reduction is <u>not</u> recommended for computer simulation as stated in Chapter 2.

The threshold voltage is a very important MOS device parameter and is defined as the voltage that will bring about surface inversion. The basic theory of surface inversion is developed from energy band considerations and it can be shown that the following equation has both practical and theoretical significance:

$$V_{TO}=V_{FB} - \frac{\sqrt{2K_S \epsilon_o q N_D \left|\phi_S \text{ inv.}\right|}}{C_O} + \phi_S \text{ (inv.)} \qquad 4\text{-}13$$

where V_{FB} = flatband voltage.

To complete the preceeding equation the surface potential at inversion must be substituted into equation 4-13. This consideration leads to what is known as the onset of "strong inversion".

As a practical matter a surface may be considered inverted when the surface hole concentration is equal to the impurity concentrate in the bulk. This same criterion restated in terms of band theory requires the surface potential to equal two times the energy difference between the intrinsic Fermi level and equilibrium Fermi level,

$$\phi_S = 2\phi_F$$

so threshold voltage becomes

$$V_{TO} = V_{FB} - \frac{\sqrt{2K_S \epsilon_o q N_D \left|2\phi_F\right|}}{C_O} + \left|2\phi_F\right| \qquad 4\text{-}14$$

The preceeding definition of threshold voltage is not completely accurate as there are some free carriers at the surface before $\phi_S = 2\phi_F$. Threshold voltage measurement can be made but some care should be taken to insure that strong inversion has occured.

This is the definition of threshold used in deriving the basic MOS equations. This therefore suggests an easy measurement technique. Let $V_{GS}=V_{DS}$ (to insure application of the saturation equation) and measure the voltage at two different low currents. Knowing two points on the

$$I_{DS}=\frac{\beta}{2}\frac{W}{L}\ (V_{GS}-V_{TO})^2 \qquad 4\text{-}15$$

equation, the extrapolated value at $I_{DS}=0$ is easily obtained.

On the following $\sqrt{I_{DS}}$ versus $(V_{GS}-V_{TO})$ curves one can observe a departure from the straight portion of the curve at small values of $\sqrt{I_{DS}}$. This departure indicates that the

equation

$$I_{DS} = \frac{\beta}{2} \frac{W}{L} (V_{GS} - V_{TO})^2 \qquad 4\text{-}16$$

or $$\sqrt{I_{DS}} = \sqrt{\frac{\beta}{2} \frac{W}{L}} (V_{GS} - V_{TO})$$

is no longer valid. Since the actual MOS device can conduct current before $V_{GS} = V_{TO}$ (ie before the onset of strong inversion), the points used to calculate the extrapolated threshold voltage must both be on the straight line portion of the curve. For a large ratio device there is a very real possibility of making the lowest of the two current measurements before the on set of strong inversion and thereby obtaining a smaller extrapolated threshold voltage. The measurements shown in Fig.4-2 were taken on the same die, and it is reasonable to assume that the physics at the surface are identical. For the three devices shown the extrapolated threshold voltages are approximately the same, but from Figure 4.2, one can see that 10μA a measurement on the large ratio device is almost off the staright line portion of the $\sqrt{I_D}$ versus $(V_{GS} - V_{TO})$ plot. Care should be taken to assure that the threshold voltage which is inputed for computer simulation be as accurate as possible.

The effect of substrate bias on the MOS device characteristic can be calculated by considering the device as a four terminal element. A complete development of the equations which describe the four terminal device model was presented by Cobbold in 1966. It is this model

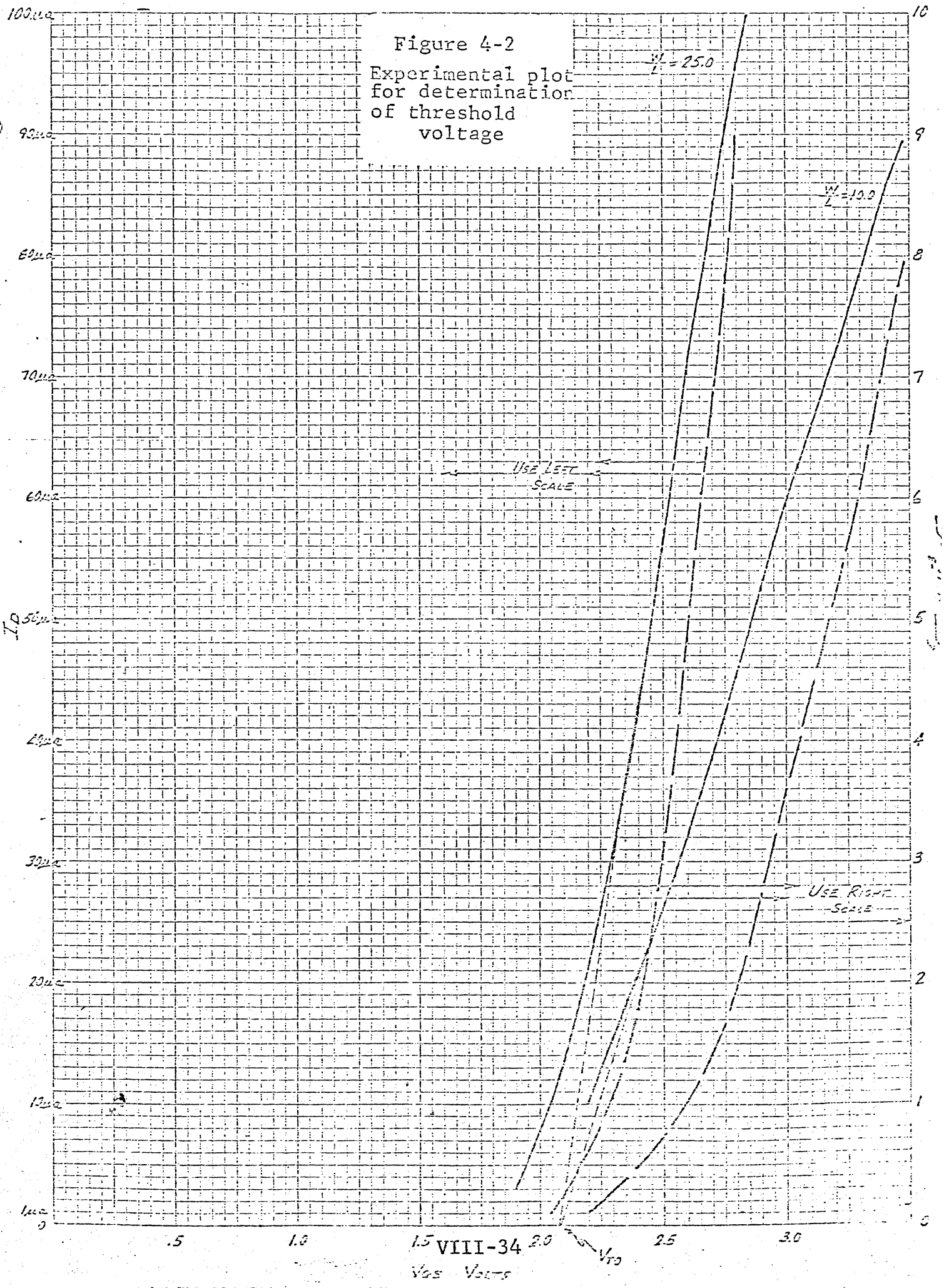


Figure 4-2

Experimental plot for determination of threshold voltage

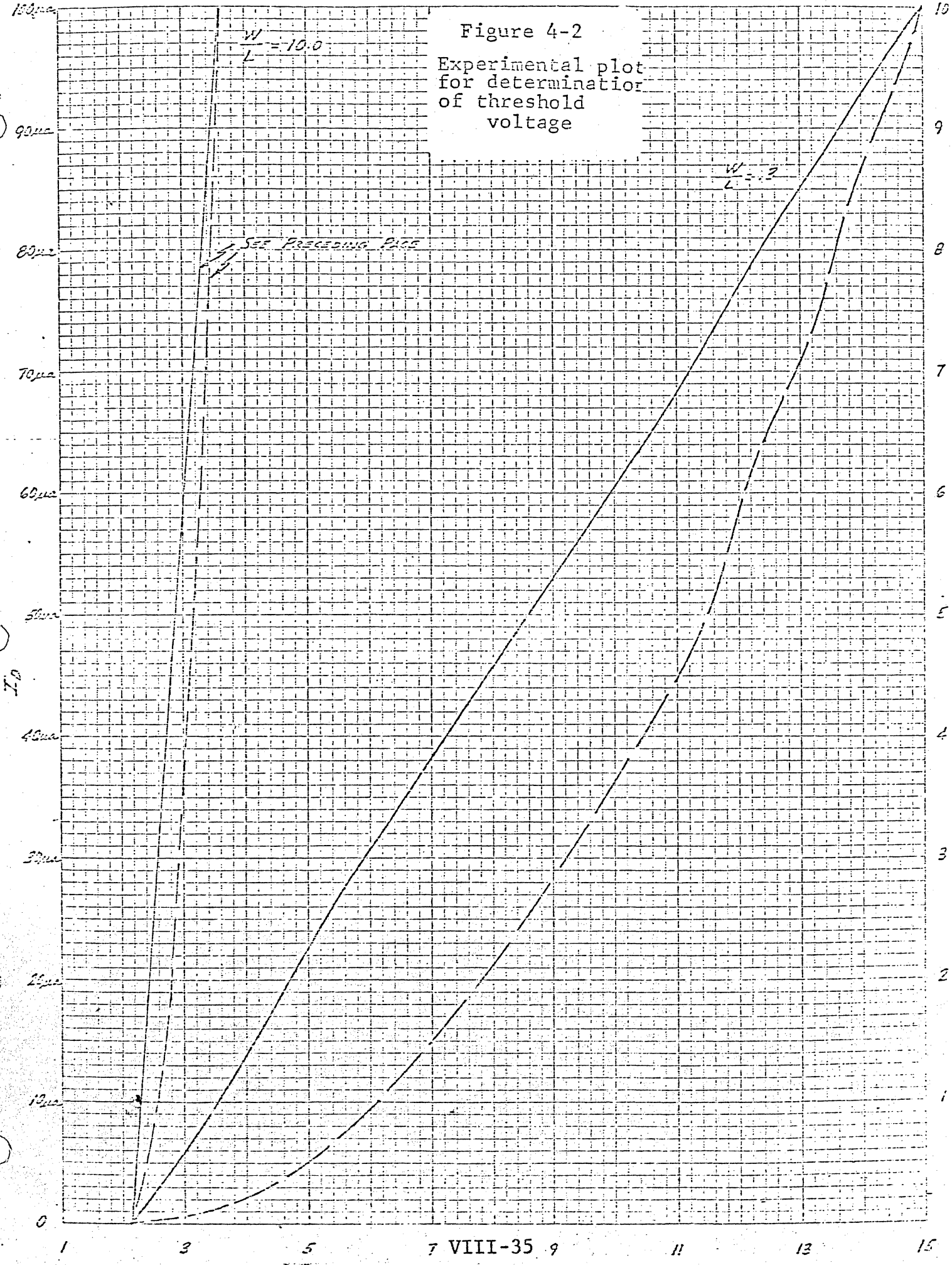
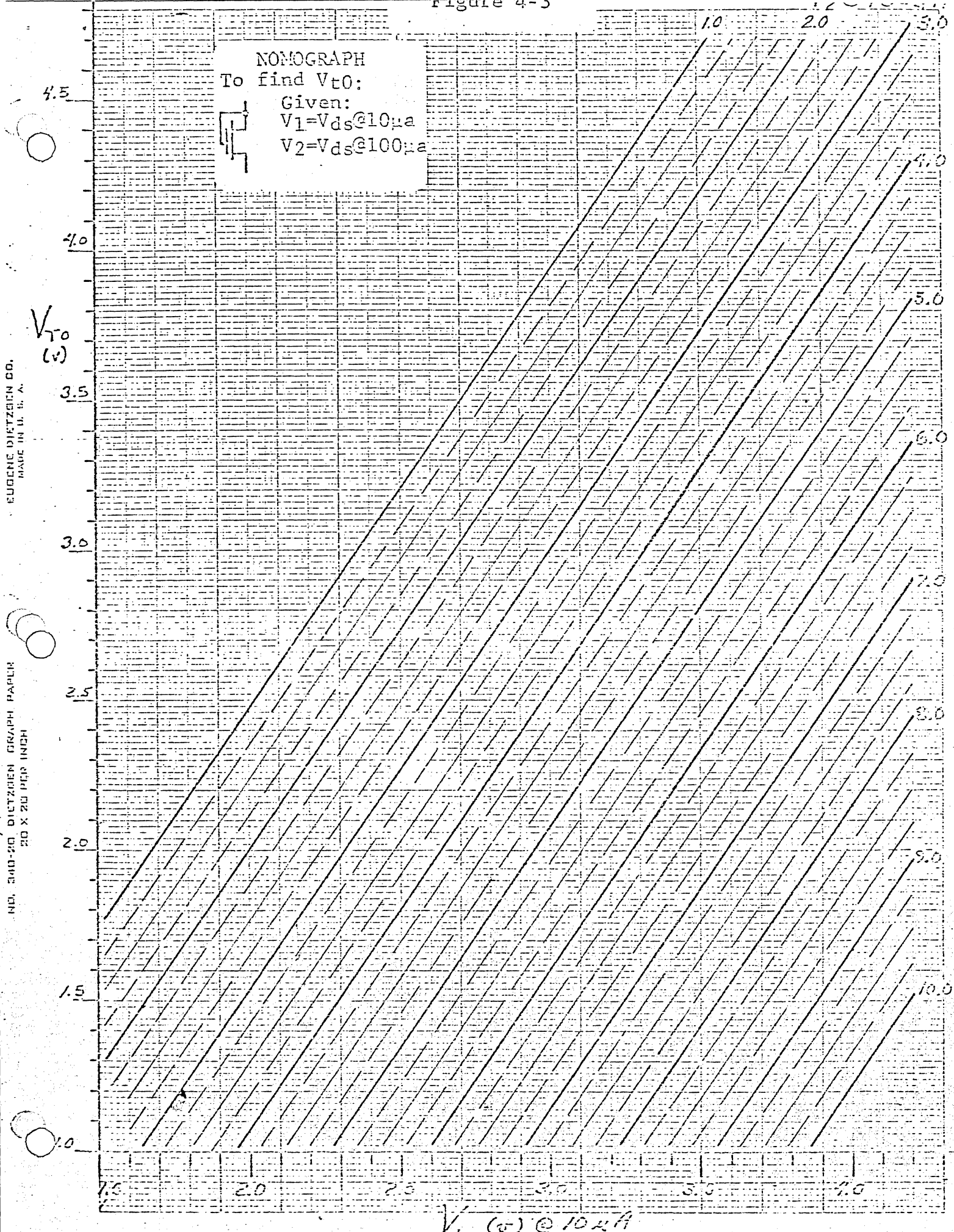


Figure 4-2

Experimental plot for determination of threshold voltage

Figure 4-3



modified by Wang that is used in computer simulation. Another modification that is now included is the effective threshold voltage. Threshold voltage with the source grounded to the substrate is one of the input parameters. An effective threshold is then calculated using the following equation:

$$V_T = V_{TO} - \frac{\sqrt{2K_S \epsilon_o q N_D \left|2\phi_F + V_{SB}\right|}}{C_O} + \frac{\sqrt{2K_S \epsilon_o q N_D \left|2\phi_F\right|}}{C_O} \qquad 4\text{-}17$$

This is the same equation used to calculate V_{BE} in the MOS Design Manual.

Length and width parameters used in the program are actual not drawn size.

The following is a list of the input cards that the design engineers must change under different circumstances.

1 DATA D, VTO, XJ, AF/1.2E15, -2.0, 1E-4, .59/

D = inpurity doping density in Atom/cm^3

V_{TO} = Measure threshold voltage with source and substrate tied together. A minus sign must be included for the P channel model.

XJ = Junction depth in microns.

AF = Surface mobility reduction factor (see page 29)

For <111> material

IF (EI. GT. 0.000561) GOTO 20

20 E = 1.0/(.979+37.4*E1)

For <100> material

```
If  (EI. GT. 0.001025)  GOTO 20
20 E = 1.0/(.96+39.*E1)
```

This is the extent of the card or statement changes needed to go one material or crystal orientation to another. As the final goal of this project is to obtain a model for use with the SCEPTRE computer program, the length, width and oxide thickness parameters are inputs which come from the main program to the function program. The changes listed are those which must be made in the function program.

In computer simulation one must be cognizant that the final vindication of a model is its ability to predict device characteristics. In order to make a comparison between the computer simulation and the actual device characteristics, a silicon gate test chip was chosen for evaluation. The process parameters were as follows:

$N_D = 1.2 \times 10^{15}$ atoms/cm^3

$x_j = .6$ microns

$t_{ox} = 1000$ Å

<111> material

The length and width were obtained very accurately accounting for over etch and side diffusion. Measurements were made to determine V_{TO} and β, (see Fig 4-4){hole mobility.} The size of the device should provide a good test for the model as channel length modulation, normal field mobility

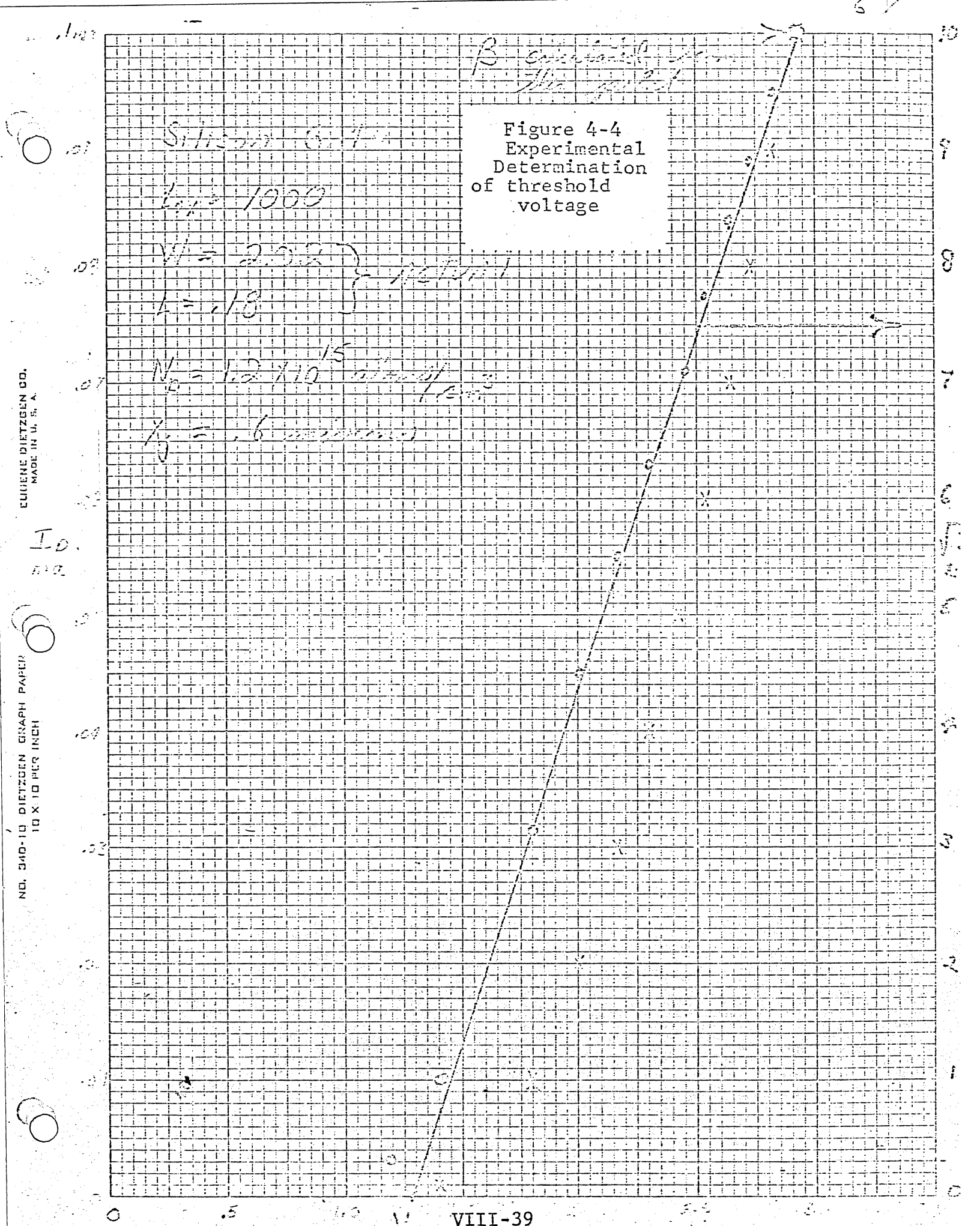


Figure 4-4
Experimental
Determination
of threshold
voltage

reduction and transverse mobility reduction can become operational effects.

Figure 4-5 is a comparison between two programs that model MOS I-V characteristics. TRANS was written by Pat O'Farrell. This program uses Crawford's normal field reduction factor which is a function of voltage not electric field, and Bentchkowsky-Grove channel length modulation. The modified FCP program written by Nygaard-Wang and modified by Lattin-Richardson, uses Wang's empirical normal field mobility reduction factor and Wang's channel length modulation model, but without transverse field mobility reduction factor. In figure 4-6 the same device characteristics are compared with modified FCP which includes Wang's transverse field mobility reduction. Note the dip at large values of V_{DS}. This departure from the actual I-V device characteristics is the result of an improper model. At the present time there is no accepted model for this phenomenon, therefore this effect should not be included in the MOS device model. Figure 4-7 is a comparison of the MOS I-V characteristics and the computer simulation using the Bentchkowsky normal field mobility reduction model. At large values of V_D, mobility is increased rather than decreased, which results in an unrealistic increase in drain current.

Figures 4-8, 4-9, and 4-10 are included to demonstrate the computer model's ability to account for source to substrate bias. The drain current should decrease when

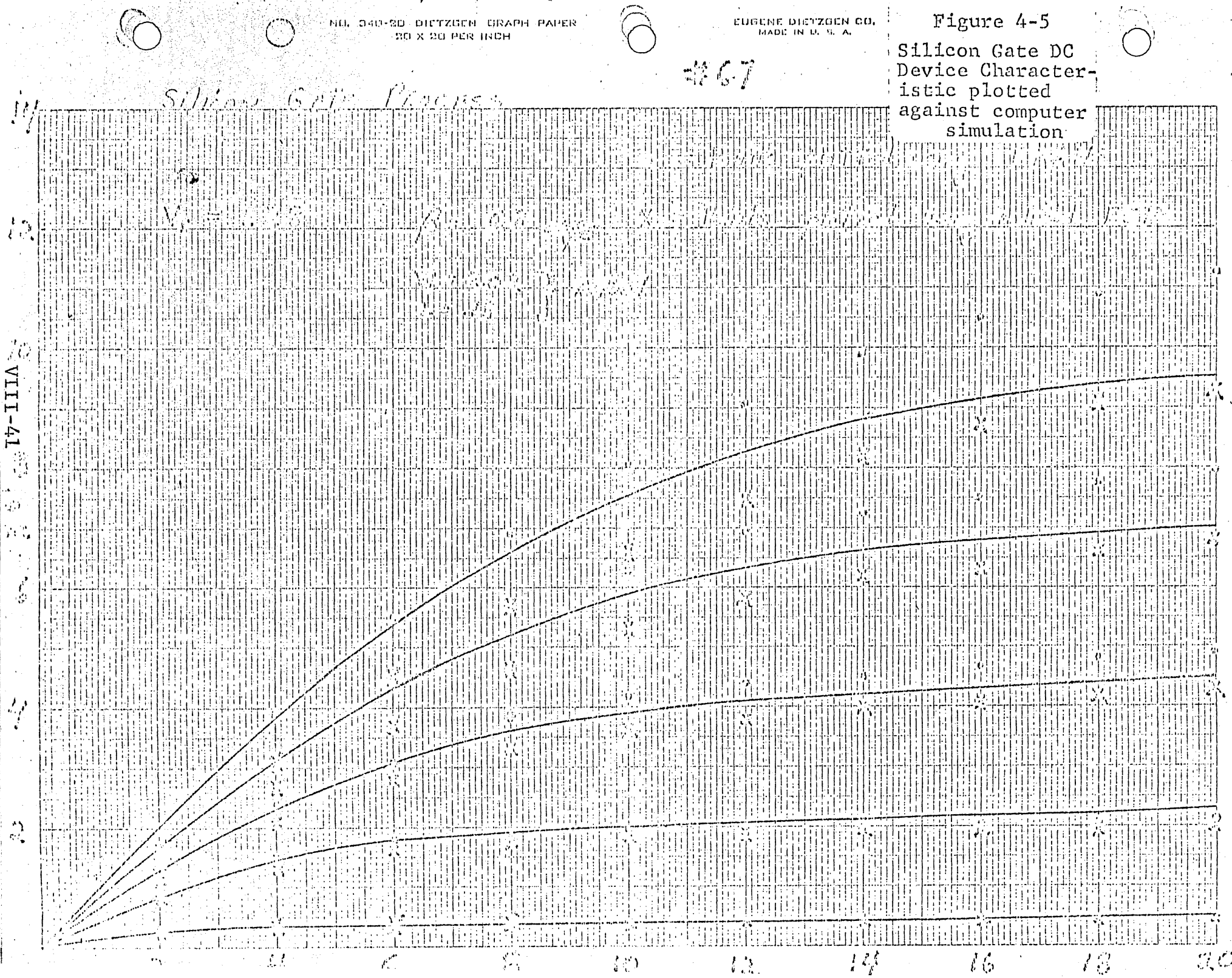


Figure 4-5

Silicon Gate DC Device Characteristic plotted against computer simulation

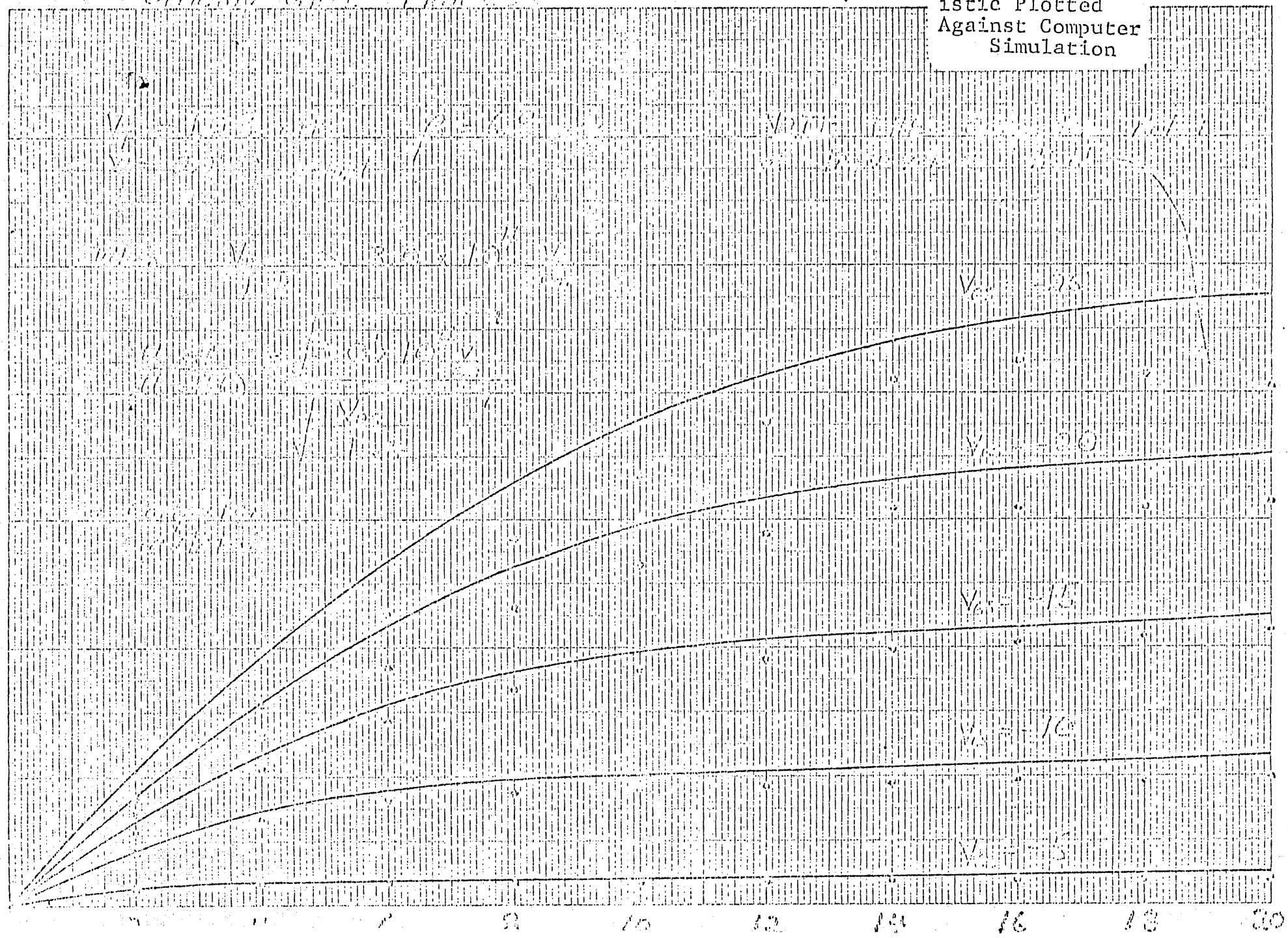


Figure 4-6
Silicon Gate DC Device Characteristic Plotted Against Computer Simulation

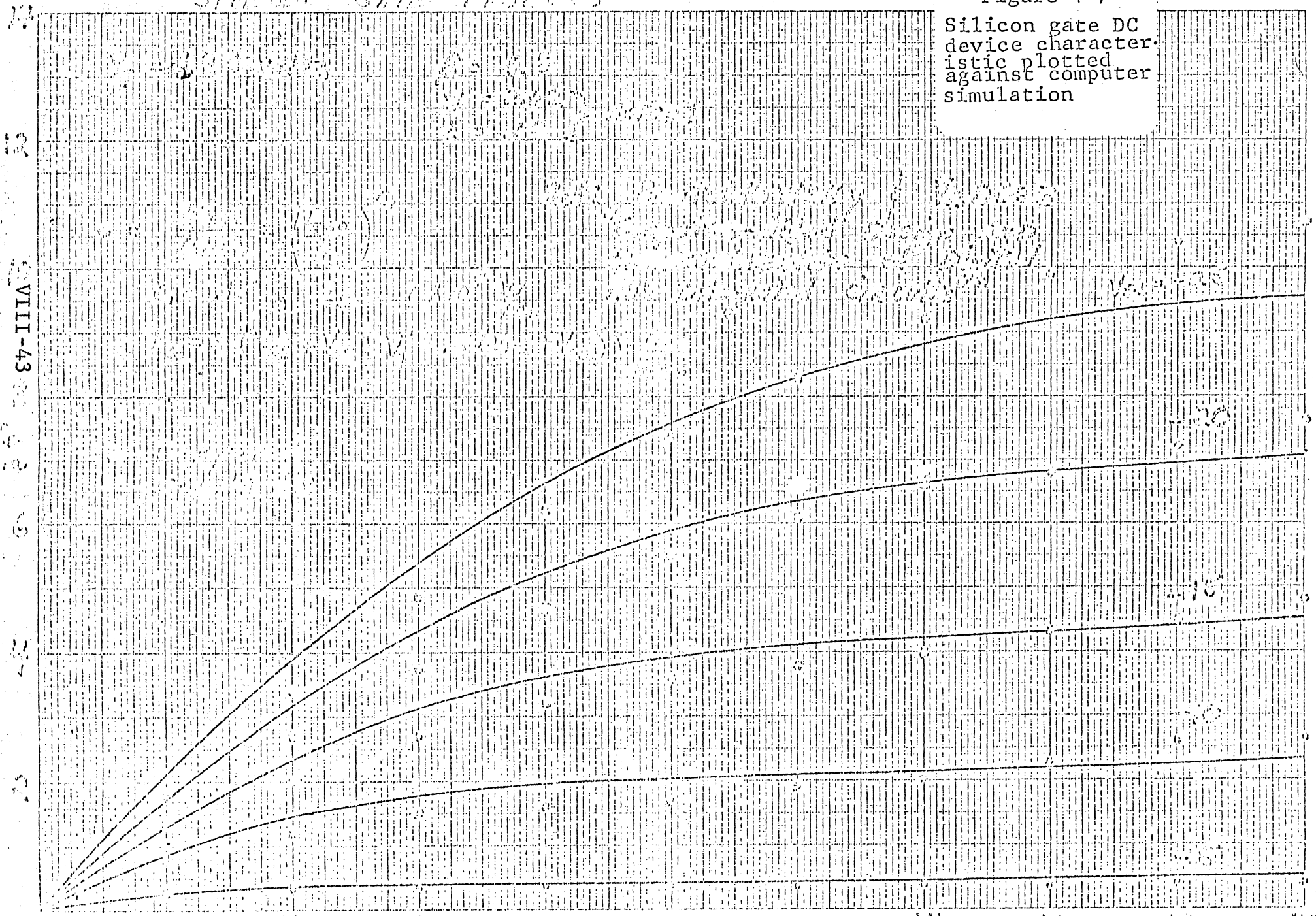


Figure 4-7
Silicon gate DC device characteristic plotted against computer simulation

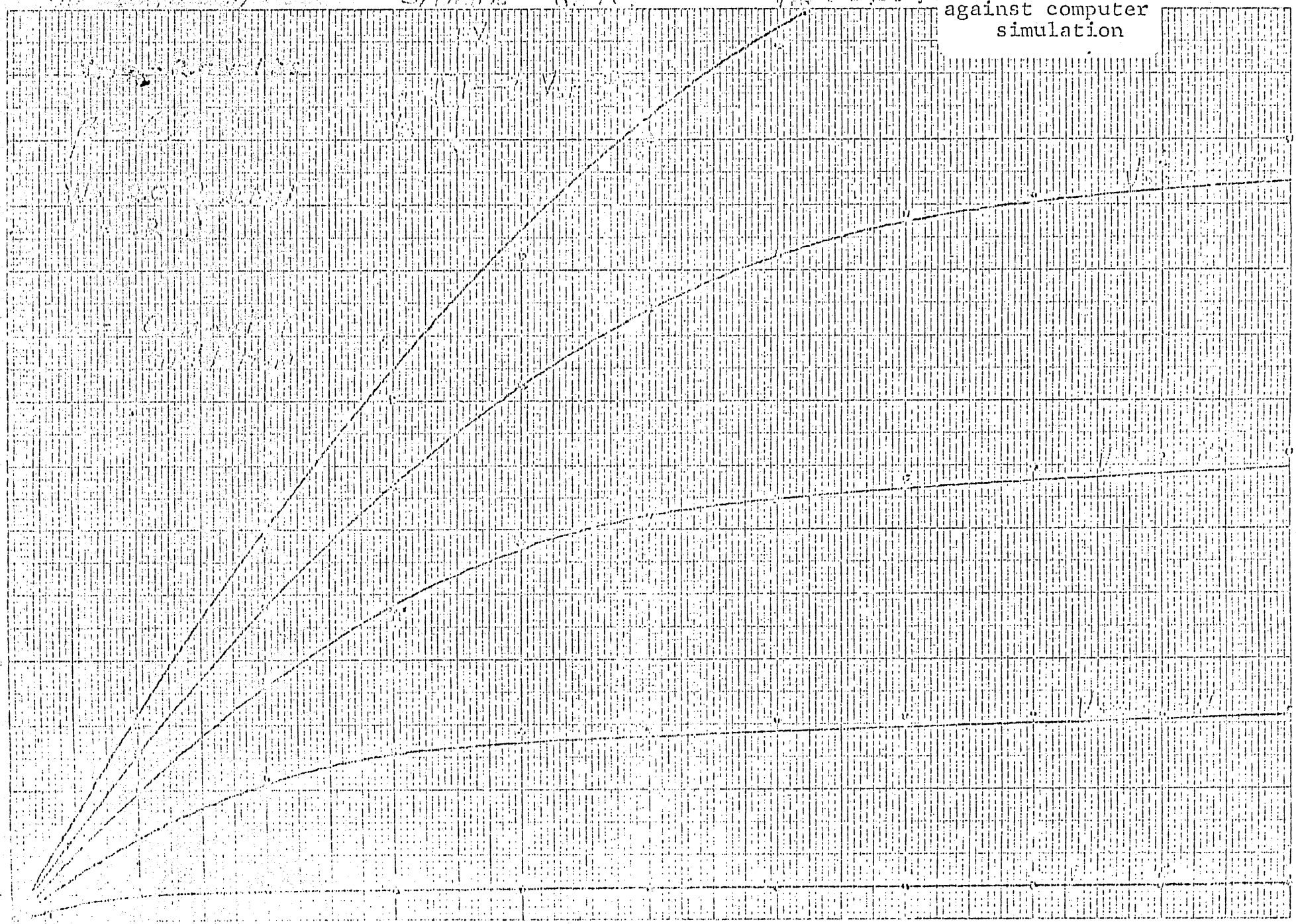


Figure 4-8
Silicon gate DC device characteristic plotted against computer simulation

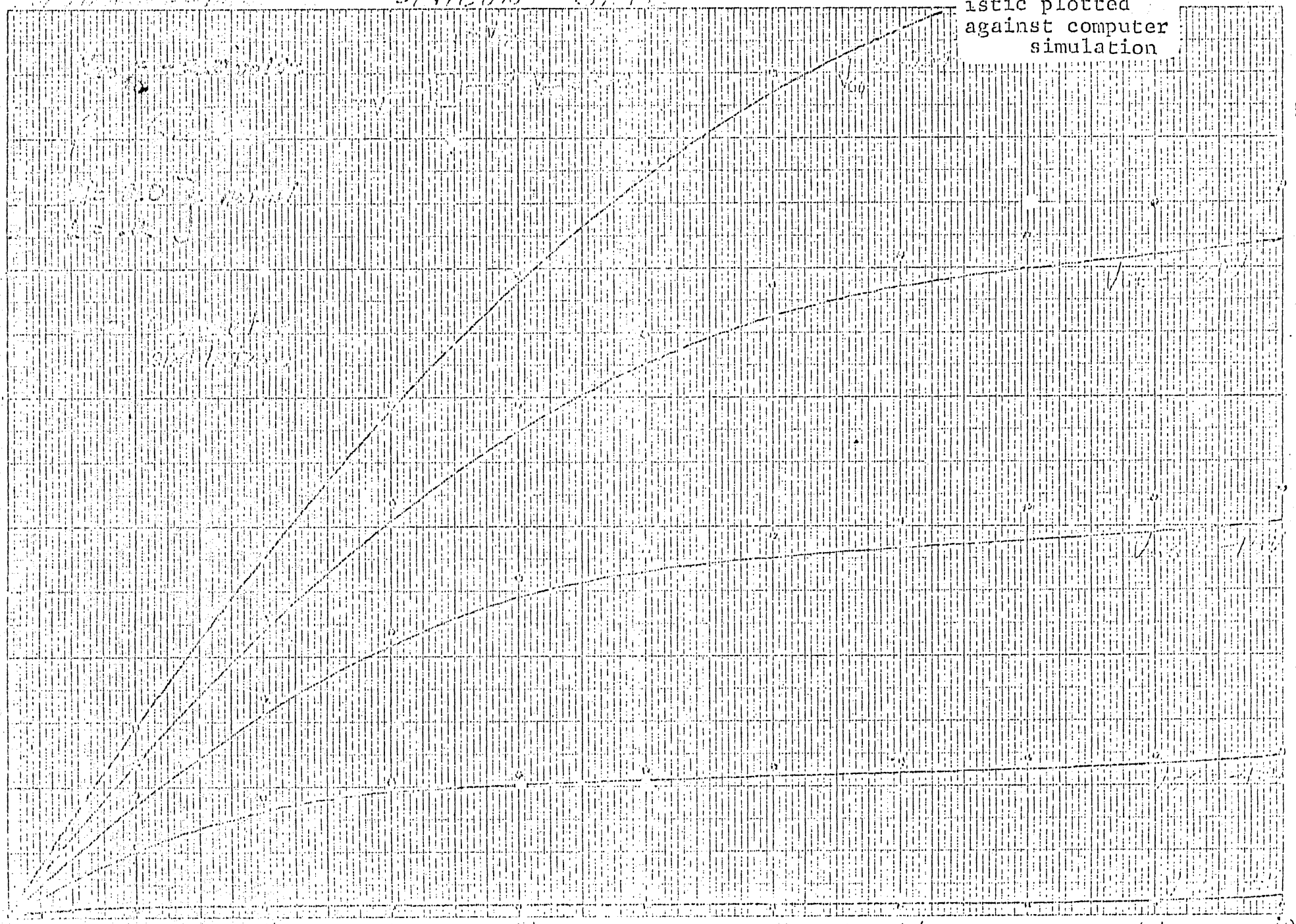


Figure 4-9
Silicon gate DC device characteristic plotted against computer simulation

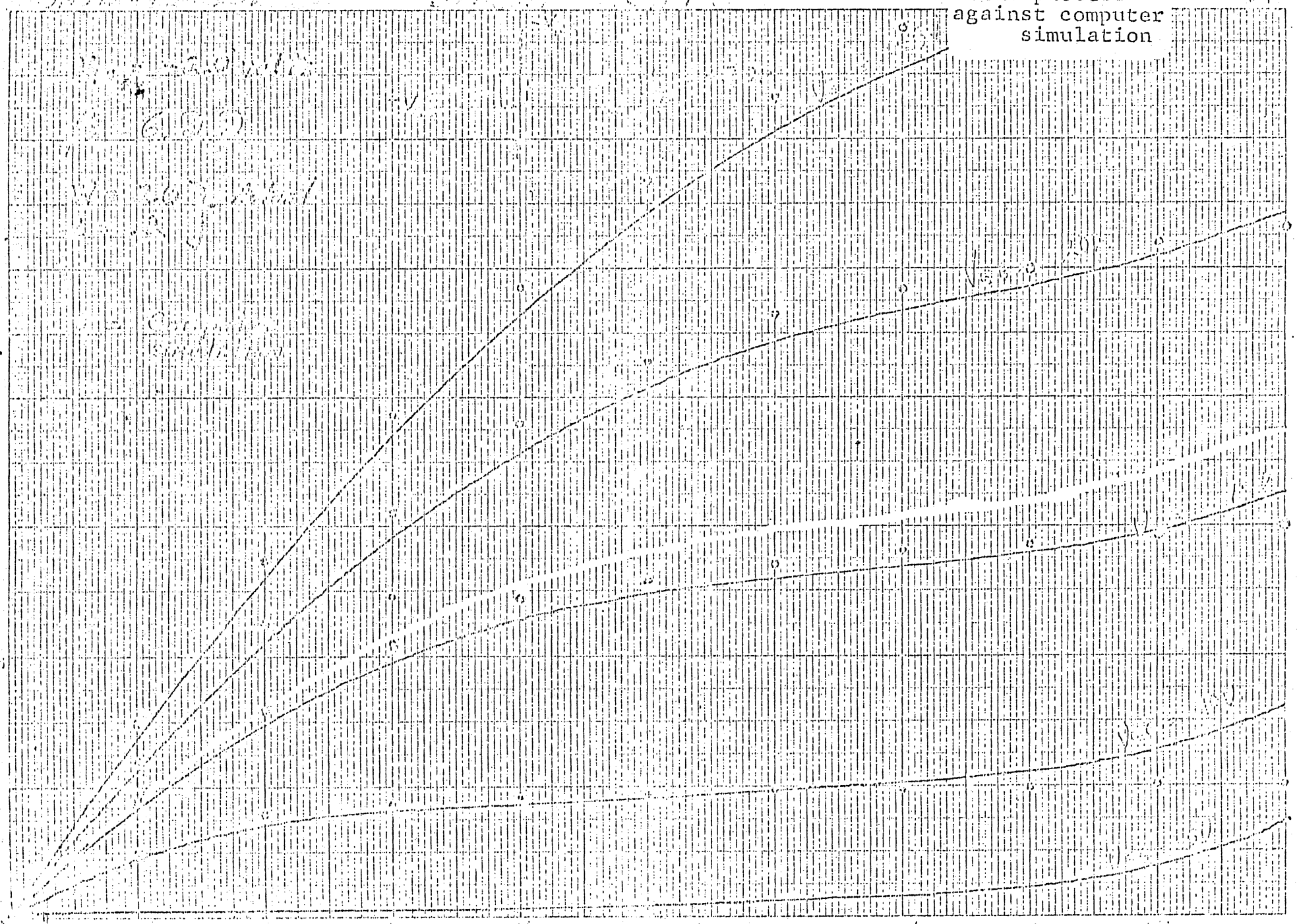


Figure 4-10
Silicon gate DC device characteristic plotted against computer simulation

the drain to substrate junction is reversed biased. The amount of current decrease is directly related to substrate doping and in the example given the doping was about 1.2×10^{15} atoms/cm^3. If the doping were higher the decrease in current would be greater.

Chapter 5

Conclusions

The purpose of this project was to obtain the best MOS model for computer simulation using input parameters familiar to the design engineer. The basic equations are those presented by Grove. These must be modified to accommodate a four terminal description.

Chapter 1 presents the four terminal equations and compares them with the accepted simplified design equations (referred to as Crawford's equations). This should acquaint the circuit designer with possible errors in using these equations.

Mobility and effective channel length, assumed constant in simplified model, are two important device parameters that vary under certain bias conditions. Chapter 2 presents different mathematical models of mobility variation. The empirical model which is a function of electric field seems to be the best model. This model also has the advantage of being easy to change for different crystal orientations. Chapter 3 presents different mathematical models for channel length modulation. The standard p-n junction theory approximation (or Crawford's method) is <u>not</u> acceptable, while the practical difference between the Bentchkowsky-Grove and the Wang model is negligible. As a result of measurements and integration of mathematical models, a computer simulation

program is now available which will give accurate results over a wide operating range. The program does not account for junction breakdown or excessive driving voltages. The program model cannot yield accurate results without proper input parameters, such as L, W, and V_{TO}, therefore the design engineer must be cognizant of these parameters, and their measurement.

An accurate MOS device model for computer simulation should include normal field mobility reduction and channel length modulation. We recommend that the normal field mobility reduction be modeled by the empirical model presented by Wang. Channel length modulation can be modeled by either the Bentchkowsky-Grove or Wang method. Transverse field mobility reduction should not be used as presently modeled.

In Appendix A the two programs available for MOS device simulation are listed.

```
LATTIN

100 VGS=0.;VDS=0.;VSB=0.
110 T0=1000.;D=1.2E15
120 VT0=-1.3
130 Z=2.;Y0=.2
140 XJ=.6E-4;AF=.416
141 ES0=6.9E4
150 C0=3.55E-5/T0
160 P1=1.19E-11*T0*SQRT(D)
170 P2=1.125*P1*P1
180 P4=2./P2
190 P3=(3.33E7*XJ/(D*ALOG(1.E20/D)))**.333/(Y0*2.54E-3)(Junction Grade Constan
195 P5=C0/(3.9*8.87E-14)
200 VFN=-.052*ALOG(D/1.5E10)
210 VMS=-0.026*(ALOG(D/1.4E10)+ALOG(1.E15/1.4E10))
220 VI=VT0+1.5*P1*(ABS(VFN))**.5 <---- Flat Band Voltage
221 VI=VT0-1.5*P1*(ABS(VFN-VSB))**.5+1.5*P1*(ABS(VFN))**.5
230 B=447.3/(1.+(D/6.3E16)**.76)+47.7 <---- Bulk Mobility ASA Function of Doping
240 PRINT,"VT0                VT                VI                VFB"
250 PRINT,VT0,VT,VI,VFN
260 10 VI=VT0+1.5*P1*(ABS(VFN))**.5
270 PRINT,"VBS=",VBS
280 PRINT,"VDS                FCP               BETA              V"
290 VDS=-2.
300 15 CONTINUE
310 V=VBS-VI-P2*(1.-SQRT(ABS(1.+P4*(VGS+VSB+VFN-VI))))
320 EI=ABS(VLS-VI)/T0
330 IF (EI.GT.0.033631) GO TO 20
340 E=1.
350 GO TO 30
360 20 E=1./(.979+37.4*EI)          For <111>
370 30 IF(VDS.LT.V) GO TO 40
380 V=VDS
390 40 IF(V.GT.0.) V=0.
400 Y=Y0+(1.-P5*(ABS(V-VDS+.8))**.333+.025*P3)Effective Channel Length
                                                    (See Chp. 3 )
410 G1=ABS(V)/Y
420 IF(G1.LE.76.0) GO TO 50
430 G=SQRT(76.)/SQRT(G1)
440 GO TO 55
450 50 G=1.
460 60 BETA=AF*B*G*D*Z*C0/Y
470 C1=ABS((VGS-VI)*V-.5*V*V)
480 C2=ABS(P1*((ABS(V+VSB+VFN))**1.5-(ABS(VSB+VFN))**1.5))
490 FCP=BETA*(ABS(C1+C2))*1.E5
500 PRINT,VDS,FCP,BETA,V
510 VDS=VDS-2.
520 IF(VDS.GT.(-22.)) GO TO 15
530 VSB=VSB-5.
540 IF(VSB.GT.(-40.)) GO TO 10
550 STOP
560 END
```

Normal Field Mobility Functio
See Page 38
For <100>

Transverse Field Mobility Reduction
(See Pg. 20)

```
TRANS

100 READ,RSUB,VTH,VGST,VDST,VSB,B
110 READ,VGDEL,VDDEL
120 READ,W,XL
130    PRINT" RSUB   VTH   B     W     L "
140    PRINT 50,RSUB ,VTH,B,W,XL
150    50 FORMAT (5F5.1)
160 E0=8.87E-14
170  L=0
180 N=1
190 K=1
200 QK=11.7
210 Q=1.6E-19
220 COX=3.9
230 C0=(QK*COX*E0)/1.3E-5
240 U0=B/C0
250 QND=1/(2E-16*RSUB)
260 FERMI=-0.026*LOG(QND/1.4E10)
270 VFB=VTH-2*FERMI+(SQRT(2*E0*QK*Q*QND*(2*ABS(FERMI)+VSB)))/C0
280 C1=SQRT((2*QK*E0)/(Q*QND))
290  YSMS=0.05*0.45429*LOG(QND)-1.22
300  QSSC0=YSMS*VFB
310    PRINT"     C0   FERMI   VFB     C1     SMS QSS/C0"
320    PRINT 60,C0,FERMI,VFB,C1,YSMS,QSSC0
330    60 FORMAT (E9.1,2F5.2,E8.1,2F5.2)
340  VG=VGST
350  VD=VDST
360  90 IF(VTH-VG)140,140,100
370 100 VDSAT=VG-VFB-2*FERMI-((QK*E0*Q*QND)/(C0*C0))*(1-SQRT(1-(2*C0
380 + *C0*(VG-VFB))/(QK*E0*Q*QND)))
390  IF (L) 120,115,120
400  115 VD=VDSAT
410  X=0
420  GO TO 255
430 120 VGPR=VG-QSSC0
440  105 IF (VDSAT-VD) 110,110,125
450 110 X=0
460 GO TO 255
470 125 XINV=1/(C1*SQRT(VDSAT-VD))+(QK*COX/(QK*1.3E-5))*(0.2*(VGPR
480 + -VD)+0.6*(VDSAT-VGPR))/(VDSAT-VD)
490 X=1/XINV
500 X=X*(1E3/2.54)
510 QID=QIDSAT*(XL/(XL-X))
520 GO TO 145
530 255 QID=(W/(XL-X))*E0*(1/(1+0.025*(VTH-VG)))
540 + *C0*(((VG-VFB-2*FERMI-(VD/2))*VD-(VG-VFB-2*FERMI-(VSB/2))*VSB)
550 + -(2/(3*C0))*(SQRT(2*QK*E0*Q*QND)
560 + *(((ABS(VD+2*FERMI))**1.5)-((ABS(VSB+2*FERMI))**1.5)))
570  IF (L) 145,135,145
580  135 L=1
590 QIDSAT=QID
```

TRANS CONTINUED

```
600     PRINT" VDSAT  IDSAT"
610   PRINT 260,VDSAT,QIDSAT
620   260 FORMAT(F5.2,F7.2)
630     PRINT"  VG      ID      VD  LDEP"
640   VD=VDST
650  GO TO 105
660  140 QID=0
670   145 PRINT 320,VG,QID,VD,X
680   320 FORMAT(F6.2,F7.2,F6.2,F6.3)
690  N=N+1
700  IF(N-10)150,150,200
710  150 VD=VD+VDDEL
720  GO TO 90
730  200 K=K+1
740  IF(K-10)250,250,300
750  250 VG=VG+VGDEL
760  VD=VDST
770  N=1
780  L=0
790  GO TO 90
800  300 STOP
810  SDATA
820    6,-4.2,-5,-1,0,.4
830    -1,-1
840    2.0,.5
850  END
```

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10. C.T. Sah and H.C. Pao, "The Effects of Fixed Bulk Charge on the Characteristics of Metal-Oxide-Semiconductor Transistors" IEEE Trans. Electron Devices, Vol, ED-13, pp 393-409.

11. R. Wang and P. Nygaard, "MOS Device Modeling" Motorola Inter-office Correspondence, 5/5/69.

12. V. Rodriques, H. Ruegg, and M.A. Nicolet, Measurement of Drift Velocity of holes in Si at High-Field Strengths: IEEE Trans. Electron Devices, Vol, ED-14, pp 44-46, January 1967.

CIRCUIT DESIGN

CHAPTER IX

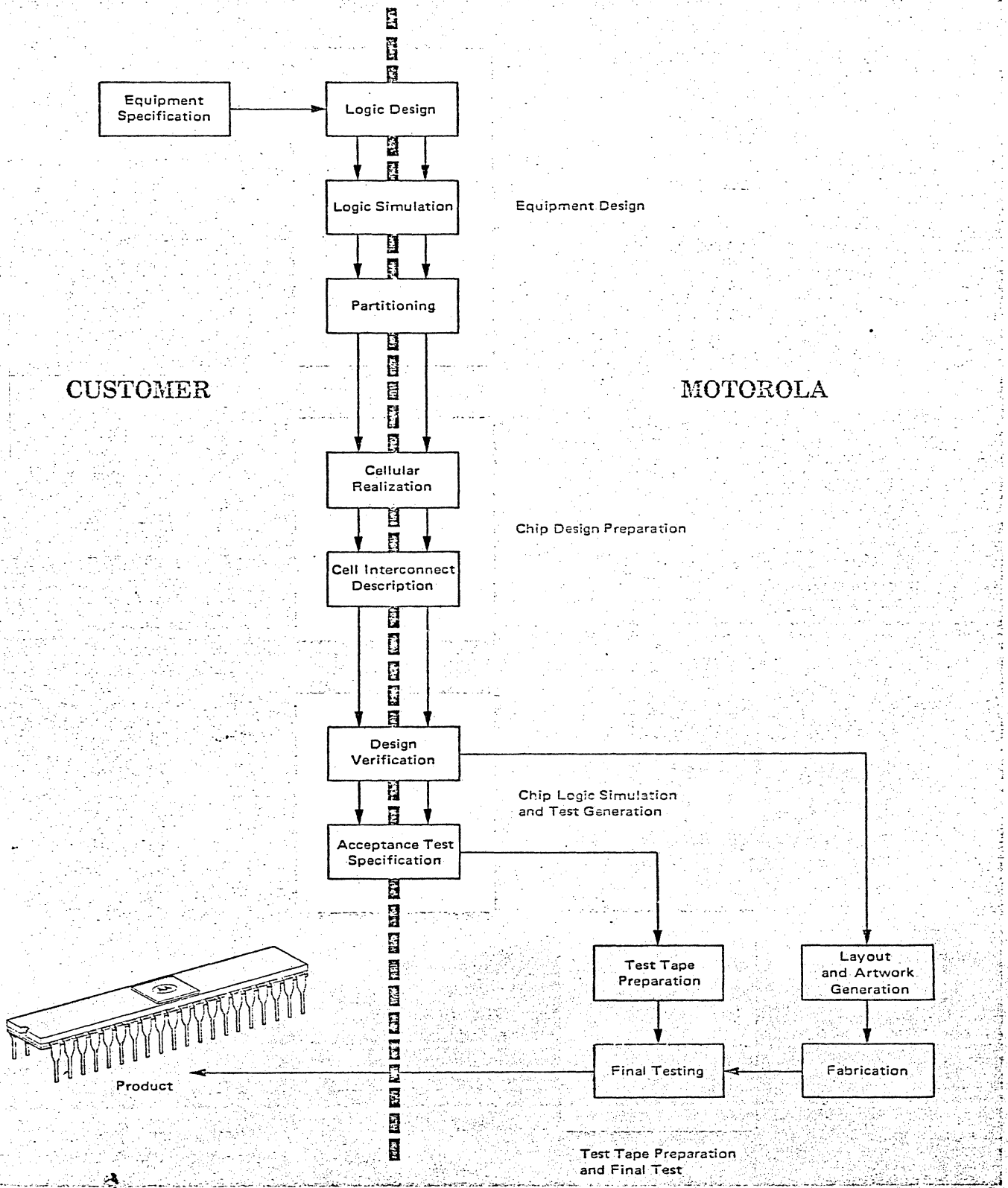
Integrated Circuit Design

The initial step of LSI design is the verification of the customer's logic system. This should eliminate errors in the customer's logic system. This should eliminate errors in the customer's design and prevent misinterpretation of the system by the engineer. When the logic system is verified (see SIMUL 8), the logical functions, are broken into cells, or small electronic circuits. The following section is a detailed description of the design procedure of MOS electronic functions.

Once the cells are designed, the system is again simulated to ensure that it meets the customer's specifications. The electronic design is then converted to graphical structures, and arranged for area optimization on the chip. The graphical structure of the chip is then photo reduced and parts are manufactured. Simultaneously the logical simulation information is used to generate a sequence to test the finished parts. See Figure 9.1.

get the book
book by Crawford on MOS

FIGURE 9.1 – Customer-Motorola Interface



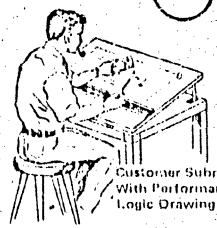
CUSTOMER

MOTOROLA

MOTOROLA

CUSTOMER

1



Customer Submits Information Sheet With Performance Specification and Logic Drawing

Evaluate Motorola's Response – If Acceptable

3

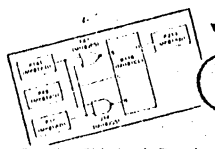
2

Motorola Responds With a Design and Delivery Schedule, Design Cost, and Production Part Cost

4

Negotiate Contract. Customer and Motorola Engineers Review Design Requirements and Schedule

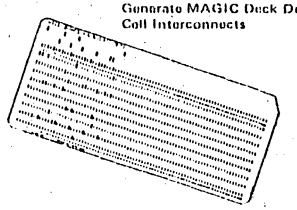
5



Prepare Detailed Chip Logic Drawing Utilizing Cells from Library

6

Generate MAGIC Deck Describing Cell Interconnects



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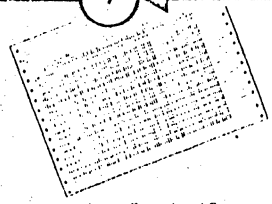
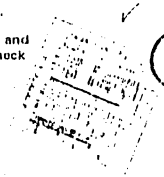


Generate Input Functional Sequence for SIMULB. Verify Design

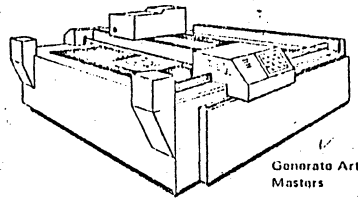
8

(Continued)



Ink Plot and Final Check

10c

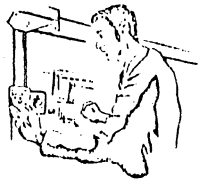


Generate Artwork Masters

10d

10b

Route Interconnections



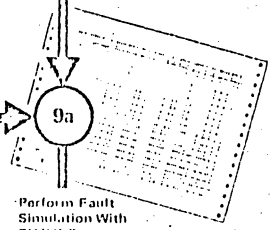
10a

Determine Cell Placements

8

Review Simulation

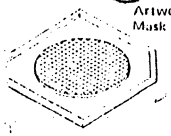
9a



Perform Fault Simulation With SIMULB to Generate Tests

10e

Artwork Reduction and Mask Stepping

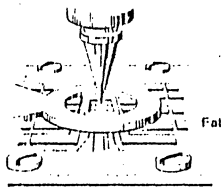


9b

Evaluate Fault Simulation Run

Additional Tests Required

If Acceptable



11

Fabrication

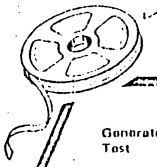
9c

Generate DC Parametric Tests

9d

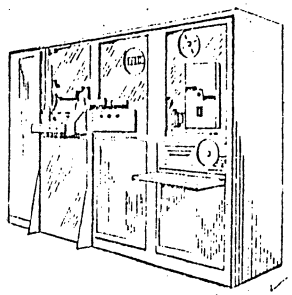
Review Acceptance Specification

Product



9e

Generate Test Tape for Final Test



12

Final Test

13

Customer Part Eval

CHAPTER IX

D-C Circuit Design

DC Design

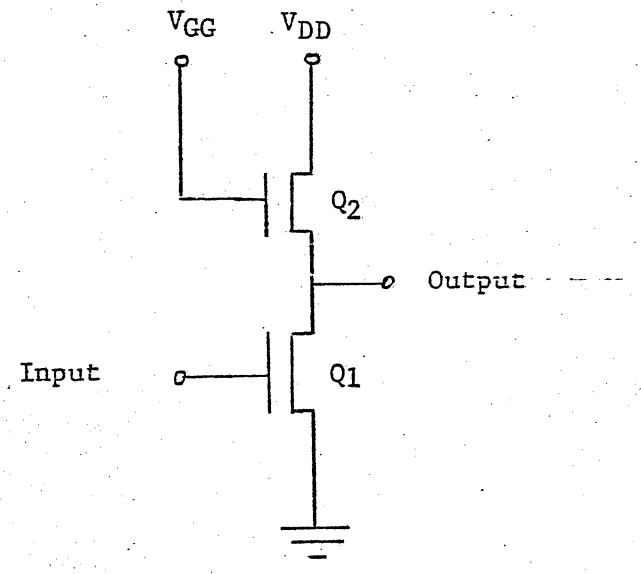
The design engineer begins building an MOS integrated circuit by dividing the chip into circuit functions or cells. He then proceeds to design these cells electrically to fit the requirements specified by the customer, the technology, and/or marketing information.

The DC design of any cell usually reduces to the design of an equivalent set of inverters which fit a group of design criteria.

Design Criteria

The following criteria usually describe the inverter design completely:

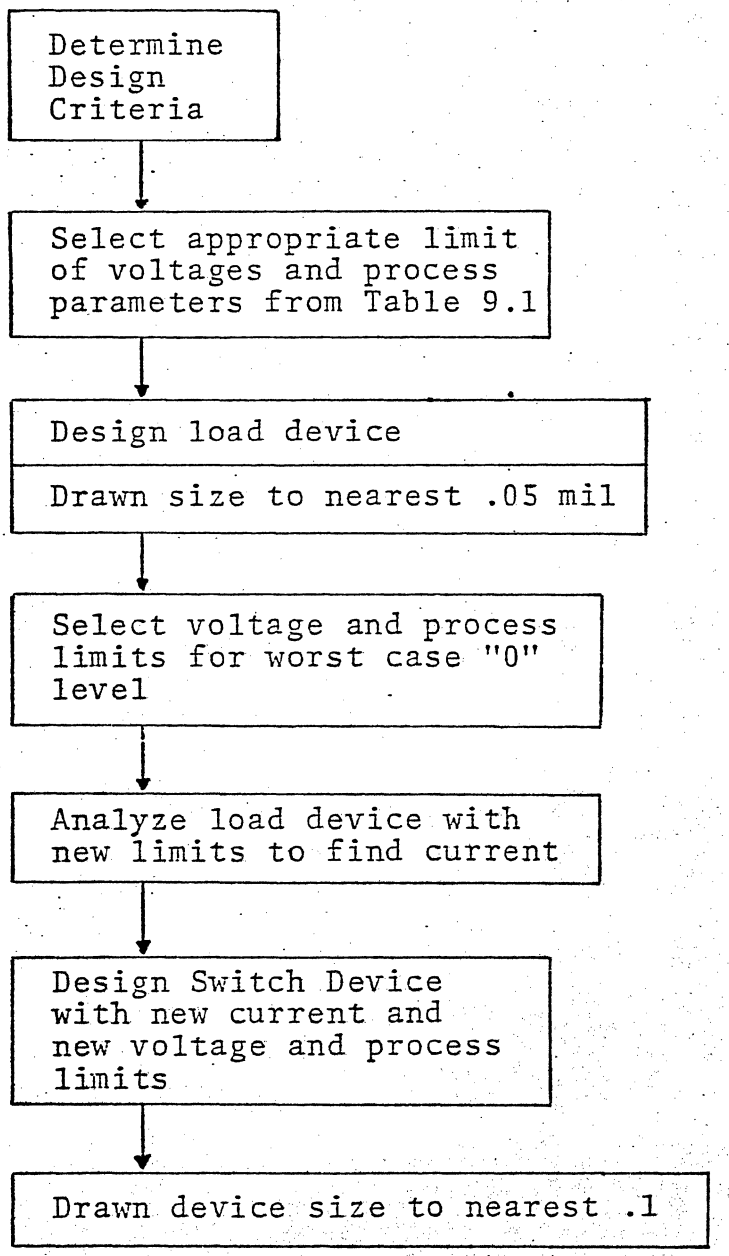
1. Process required to design chip
2. Supply Range:
   V_{DD} max., V_{DD} typ., V_{DD} min.
   V_{GG} max., V_{GG} typ., V_{GG} min.
3. Input Signal Levels
   0 min., 0 max.
   1 min., 1 max.
4. Output Signal Levels
   0 min., 0 max.
   1 min., 1 max.
5. Output Current Loading
   0 Level Current
   1 Level Current
6. Minimum, Typical, Maximum Power Dissipation
7. Minimum, Typical, Maximum, Rise and Fall times or propagation delay.
8. Noise Immunity



With these criterion the engineer can begin designing an inverter.

The inverter is simply a switch transistor Q_1, and a resistance device Q_2. A high resistance MOS device, always biased on, is often used as a resistor because it requires significantly smaller chip area than a diffused resistor.

DC DESIGN OF PMOS INVERTER



The inverter works as follows: The switch device is turned off when the voltage applied between its gate and source is lower than its threshold voltage. The output voltage is then a "1" level or approximately equal to V_{DD}: When the input voltage on the gate of the switch transistor is greater than the threshold voltage the switch device turns on. Q_1 and Q_2 then become a resistive voltage divider. If the resistance of Q_1 is small, the output voltage is near ground. The resistance of Q_2 is non linear, and a better speed power product is realized by connecting the gate to a supply voltage (V_{GG}) greater than the drain supply voltage (V_{DD}).

The appropriate process is chosen from the supply voltage specification, and interface requirements. The low threshold process, used at Motorola requires V_{GG} supplies between -12 and -20, and V_{DD} supplied between -7 and -20. The High Threshold Process requires $-15 \geq V_{GG} \geq -30$ and $-10 \geq V_{DD} \geq -30$. Silicon Gate requires Low Threshold supplies.

The input and output signal levels are determined by the Process, available supplies, and the required noise immunity at the chip terminals or the required noise immunity at connections between cells on the chip.

Cell s which connect to chip terminals are generallly required to source or sink current at a given output voltage as an interface requirement. Next, the customer may specify a minimum speed or may specify a typical or maximum power which reflects a min., typ., or max. cell current.

Now, before designing the transistors let us review the MOS device equations and the effects of Beta degradation, substrate reverse bias, side diffusion, and oxide etching.

An MOS device can be biased for two different regions of operation. These two regions are the saturation and triode or nonsaturation region.

The ideal equations which describe the operation of the MOS device for the two regions and the bias conditions which are necessary are given by

Saturation Region

$$I_{DS} = \frac{\beta W}{2L} \lfloor V_{GS} - V_t$$

where

$$V_{GS} < V_{DS} + V_{T\phi}$$

Triode Region

$$I_{DS} = \frac{\beta W}{2L} \quad 2 (V_{GS} - V_{TO}) V_{DS} - V_{DS}^2$$

where

$$V_{GS} > V_{DS} + V_{T\phi}$$

The above ideal MOS device equations will now be modified to include the effects of beta degradation, body effect, and the effective length and width of an MOS device.

Beta Degradation

For the above equations,

$$\beta = \frac{\epsilon_{ox} \mu p}{t_{ox}}$$

where

ϵ_{ox} = dielectric constant of the gate oxide

tox = thickness of the gate oxide

μp = mobility of holes in the inversion layer

The mobility term μp was assumed to be constant when the equations were derived. For an actual MOS device, as the gate field becomes larger, the carriers in the channel are attracted toward the surface and are subjected to an increased surface scattering effect. This surface scattering effect tends to decrease the effective mobility of the holes and thus cause a reduction in the beta term of the equations.

This effect can be illustrated by a plot of the incremental drain resistance r_{dt} in the triode region. The equation for r_{dt} is given by:

$$r_{dt} = \frac{L}{\beta W} \quad \frac{1}{(V_G - V_{TH})}$$

This plot is shown in figure 3-11, page 64, in Crawford's, MOSFET in Circuit Design.

The curve on page 67 of Crawford will be used to determine the beta degradation (β_{deg}) value to be used for a design.

Body Effect

If the substrate has a reverse bias applied with respect to the source, it can modulate the channel current flow between the source and drain. The substrate bias will decrease the amount of mobile carriers available for conduction and thus the I_{DS} current will also be reduced.

Body effect is given by

$$V_{BE} = -K_1 \left(\quad 2\,_F + V \text{ source} - \quad 2\,_F \right)$$

The body effect values to be used for a design are given in a series of graphs in the design manual under the section called V_{BE}. These graphs are plots of V_{BE} versus the source substrate reverse bias and the substrate resistivity.

Side Diffusion

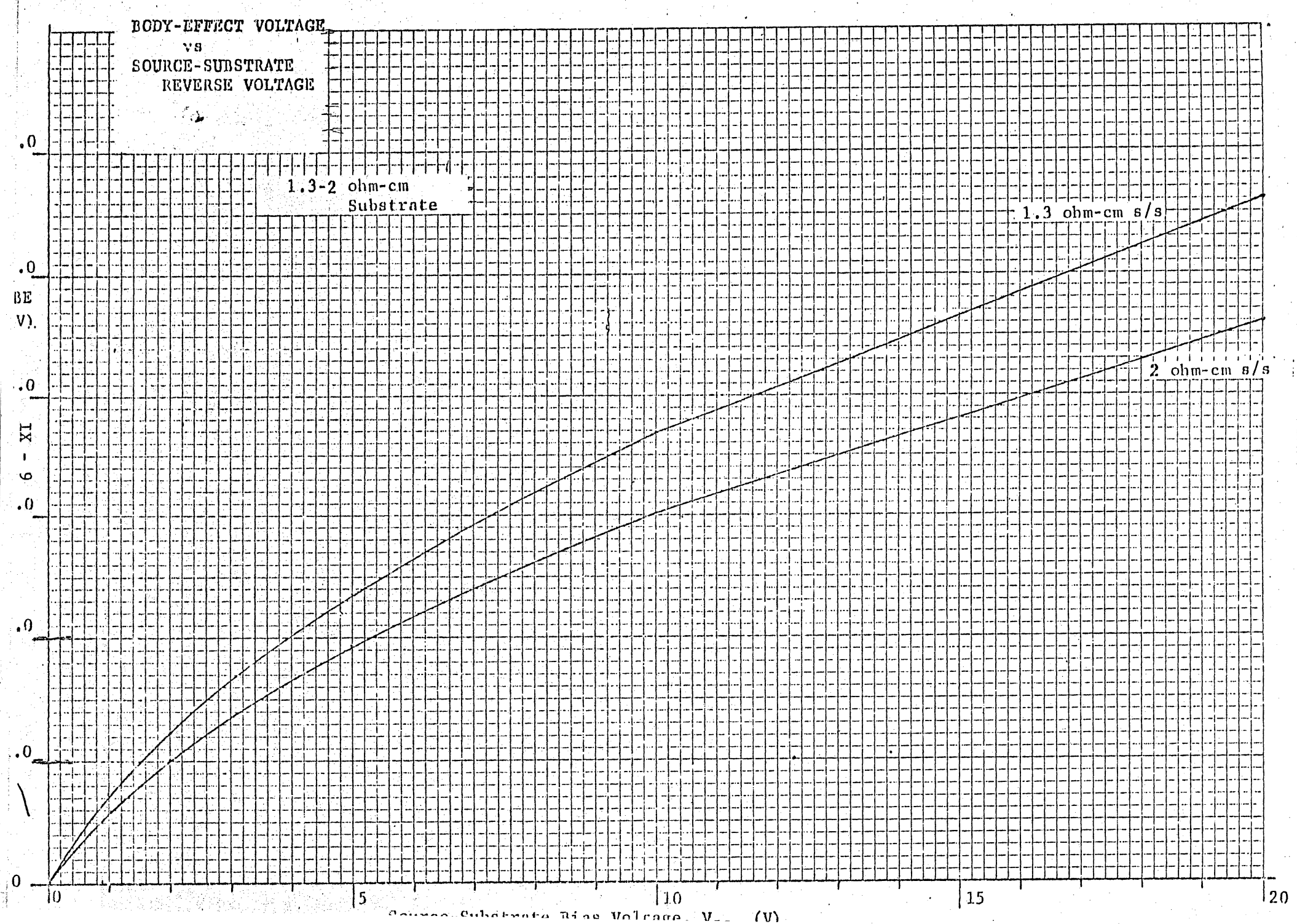
The length to be used in the MOS equations must be modified to include the side or lateral diffusion of the P-regions, photo mask bloating, and photo resist etching. This is illustrated in the following diagram.

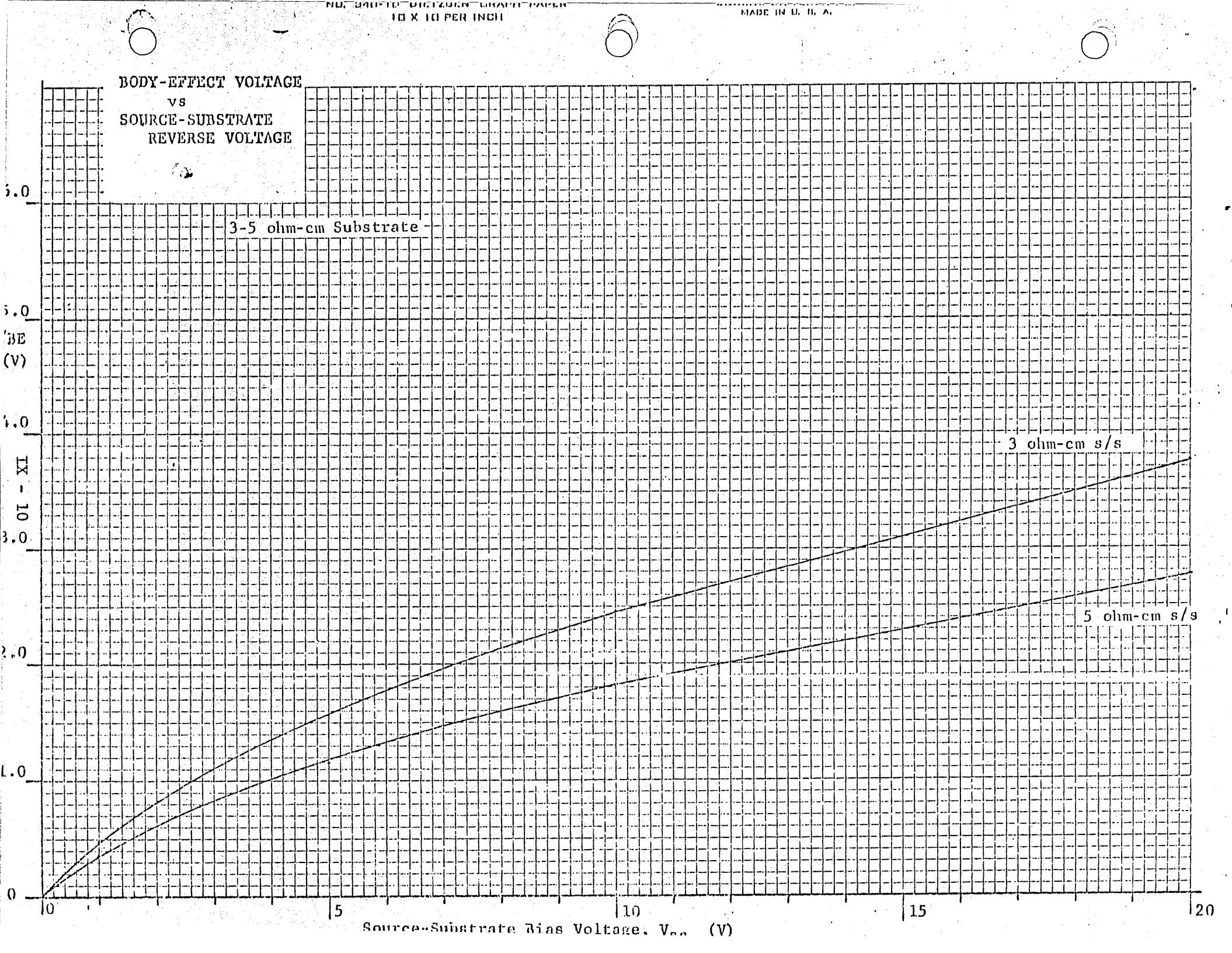
DRAWN ACTUAL

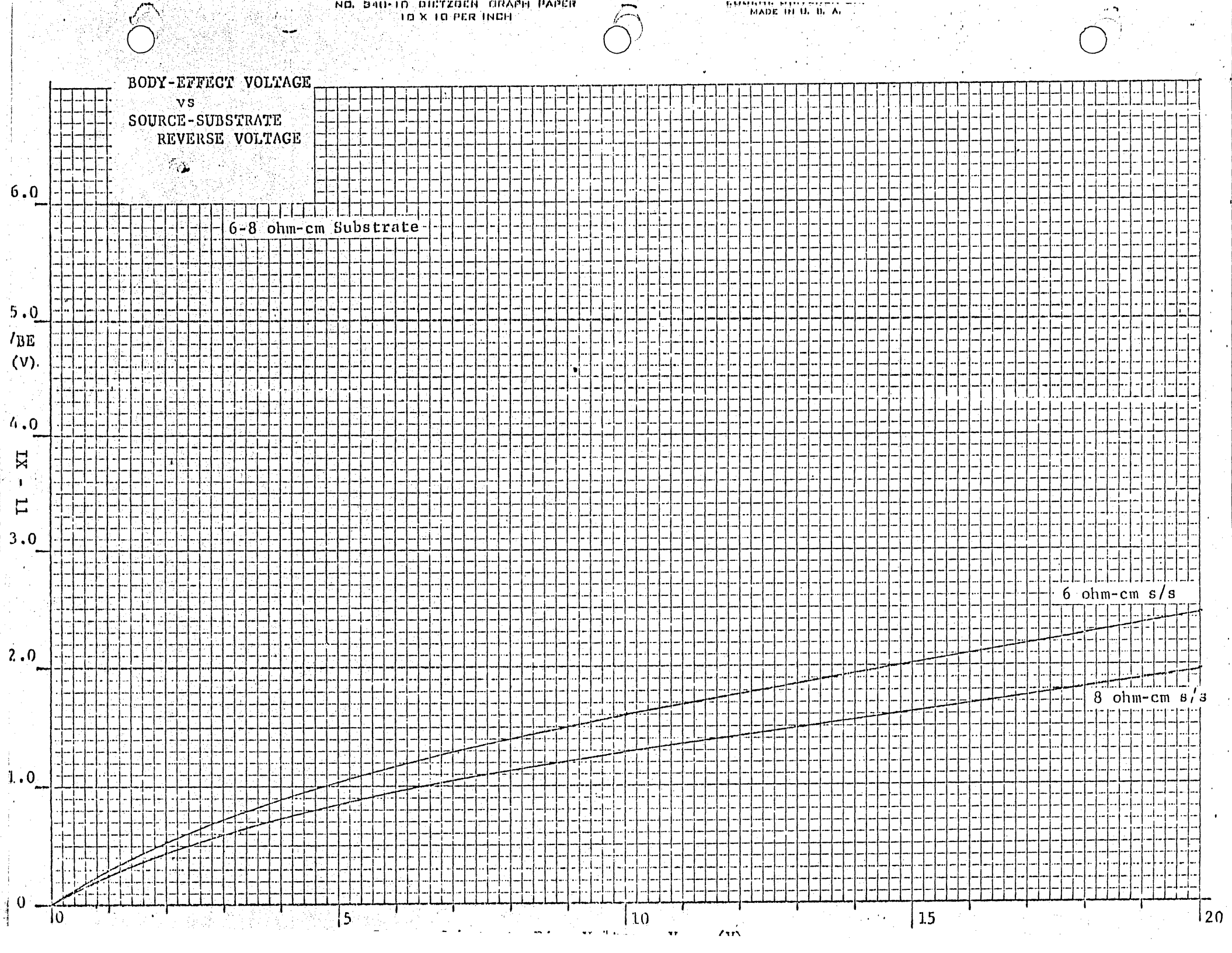
From the figure, the effective length (L) is given by

$$L_{eff} = L_{drawn} - 2\ \Delta L$$

The value to be used for ΔL is given in a table 9.1 in the design manual.







The effective width is given by

$$W_{eff} = W_{drw} + 0.05 \pm 0.05$$

where

W_{drw} = drawn width

W_{eff} = actual design width

The modified equations for the MOS device are now given by

Saturation

$$I_{DS} = \frac{\beta_{eta}\, W_{eff}}{2 l_{eff}} \left[(V_{GS} - V_{TO} - V_{BE})^2 \right] \beta_{deg}$$

for

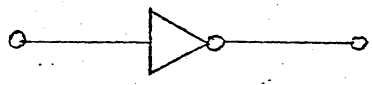
$$\left| V_{GS} \right| < \left| V_{DS} \right| + \left| V_{TH} \right|$$

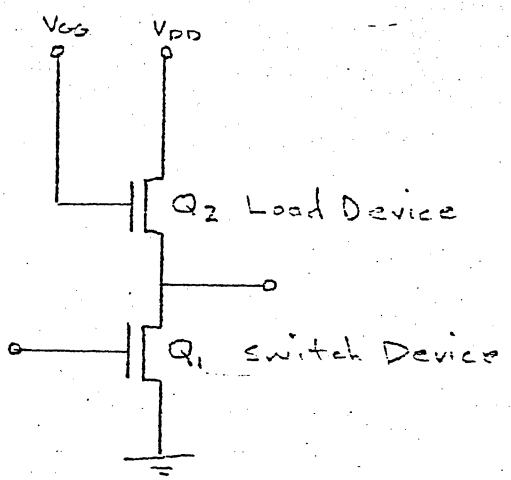
Triode

$$I_{DS} = \frac{\beta_{eta} W}{2l} \left[2 (V_{GS} - V_{TO} - V_{BE})\ V_{DS} - V_{DS}^2 \right] \beta_{deg}$$

for

$$\left| V_{GS} \right| > \left| V_{DS} \right| + \left| V_{TH} \right|$$





DESIGN OF LOAD TRANSISTOR

The engineer now begins the inverter design by designing Q_2 to meet its specifications. When done by hand, the designer will probably chose to use Crawford's equations as a first approximation although greater accuracy may be obtained from Grove's device model as used in the design software.

First the appropriate terminal voltages for the load device are determined by selecting the minimum, typical, or maximum V_{DD}, V_{GG}, and output "0" level. Choose the appropriate limit by whether the design is for minimum, typical, or maximum current. Next determine the appropriate limit of the process parameters from Table 9.1, and the value of those parameters from Table 9.2, 9.3, or 9.4.

Now determine whether the device operates in the triode or saturation region.

$V_{GS} = V_{GG}$ - "0" level

$V_{DS} = V_{DD}$ - "0" level

Triode	Saturation
$V_{DS} < V_{GS} - V_{T\emptyset} + V_{BE}$	$V_{DS} > V_{GS} - V_{TO} + V_{BE}$
$V_{TH} = V_{T\emptyset} + V_{BE}$	

Now solve Crawford's equation for the W/L ratio:

β = Beta x $\beta_{degradation}$

Triode	Saturation
$I_{DS} = \frac{\beta}{2}\frac{W}{L}(2V_{GS} - V_{TH})V_{DS} - V_{DS}^2$	$I_{DS} = \frac{\beta}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$
$\frac{W}{L} = \frac{I_{DS}}{-\frac{\beta}{2}(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2)}$	$\frac{W}{L} = \frac{I_{DS}}{\frac{\beta}{2}(V_{GS} - V_{TH})^2}$

This is the actual width to length ratio. The process parameters Gate Etch and Delta must now be considered to determine the drawn size of the width and length.

$$\frac{W}{L} = \frac{W_{drawn} + \text{Gate etch}}{L_{drawn} - 2\ \text{Delta}}$$

In order to make the transistor as small as possible either the drawn width or drawn length will be chosen to be a minimum size (see layout rules).

For a load device minimum width is usually required, solving:

$$L_{drawn} = \frac{W_{min} + \text{Gate etch}}{\left(\frac{W}{L}\right)} + 2\ \text{Delta}$$

occasionally a minimum length device is required:

$$W_{drawn} = (L_{min} + 2\ \text{Delta})\left(\frac{W}{L}\right) - \text{Gate etch}$$

Check L_{drawn} or W_{drawn} to be sure it is greater than L_{min} or W_{min}. Next these drawn sizes are used to analyze the load device under the conditions which give the highest output "0" level, (see Table 9.1).

Solve for the current:

$$\frac{W}{L} = \frac{W_{drawn} + \text{Gate etch}}{L_{drawn} - 2\ \text{Delta}}$$

$$\beta = \text{Beta} \cdot \beta_{degradation}$$

$$V_{TH} = V_{T\emptyset} + V$$

$$V_{GS} = V_{GG} - \text{"0" level}$$

$$V_{DS} = V_{DD} - \text{"0" level}$$

Triode or Saturation

$$\left|V_{DS}\right| < \left|V_{GS}\right| - \left|V_{TH}\right| \qquad \left|V_{DS}\right| > \left|V_{GS}\right| - \left|V_{TH}\right|$$

solve for the current

$$I_{DS} = \frac{\beta}{2}\frac{W}{L}\left(2\,(V_{GS} - V_{TH})\,V_{DS} - V_{DS}^2\right) \qquad I_{DS} = \frac{\beta}{2}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

Switch Transistor Design

Now design the switch device Q_1 by solving for $\frac{W}{1}$ with the same process parameters. Be sure to consider the voltage drop in the ground bussline, which also causes a small V_{BE} effect.

V_{GS} = Input "1" level - V_{GND}

V_{DS} = Output "0" level - V_{GND}

$V_{TH} = V_{T\emptyset} - V_{BE}$

β = Beta β_{deg}

$$\frac{W}{L} = \frac{I_{DS}}{\frac{B}{2}\left(2(V_{GS} - V_{TH})\ V_{DS} - V_{DS}^2\right)} \qquad \frac{W}{L} = \frac{I_{DS}}{\frac{B}{2}\ (V_{GS} - V_{TH})^2}$$

The switch device isusually drawn minimum length.

$W_{drawn} = (L_{min} - 2 \text{ delta}) \left(\frac{W}{L}\right)$ - Gate etch

Now the size of the switch and load are determined and the circuit is ready for analysis.

The same approach is used to design bootstrap inverters and all transistors in High Threshold, Low Threshold and Silicon Gate. In CMOS minimum size devices are used for internal logic and input output buffers are designed using similar techniques.

TABLE 9.1 - PROCESS LIMITS FOR INVERTER DESIGN

Condition	V_{GG}	V_{DD}	V_{IN} "1"	V_{OUT} "0"	$V_{T\emptyset}$	BETA	Substrate Resistivity	Delta	Gate Etch
Typical: Power Current 0 Level	typ	typ	typ	typ	typ	typ	typ	typ	typ
Maximum Power Current	max	max	max	min	min	max	max	max	max
Minimum Power Current	min	min	min	max	max	min	min	min	min
Maximum Output "0" Level	max	max	min	max	max	typ	max	min	max
Minimum Output "0" Level	min	min	max	min	min	typ	min	max	min

DRAWN SIZE MINIMUMS

Process	L_{min}	W_{min}
PMOS AP05D, AP08D	.4	.25
Silicon Gate AP09D	.3	.2

DESIGN EXAMPLE

We are now ready for a design example

Assume the following parameters are given.

$V_{GG} = -16 \pm 1.5V$

$V_{DD} = -10 \pm 1V$

$V_{IN} = -1.5$ to $-7V$

$V_{OUT} = -1$ to $-8V$

Power (max) = 3mw @ $V_{OUT} = -1V$.

$\rho_S = 3$ to $5\ \Omega$-cm

Low threshold process

From the low threshold voltage section of the design manual, we obtain

$V_{TO} = -2.0 \pm .5V$

$\beta = 2.5$ to $4\ \mu A$

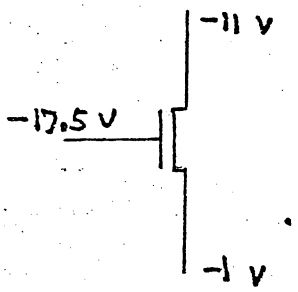
From Table 9.3 we get

$\Delta L = 0.1$

LOAD DEVICE DESIGN

The I_{DS} current for the worse case power situation must now be calculated.

$$I_{DS} = \frac{P}{V_{DD}} = \frac{3\times10^{-3}}{11} = 273\mu A$$



From V_{BE} curve for $P_S = 5\Omega$-cm and $V_{SS} = -1V$, $V_{BE} = 0.35V$

From graph on page 67 of Crawford for $V_{GS}-V_{TH} = (16.5-1.5-.35) = 14.65$ we get $\beta_{deg} = 0.67$

Now check for region of operation.

$$|V_{GS}| \overset{?}{>} |V_{DS}| + |V_{TH}|$$

$$16.5 \overset{?}{>} 10 + 1.85$$

$16.5 > 11.85$ therefore the device is operating in the triode region.

Substituting these parameters into the triode equation and solving for $(\frac{W}{L})_{load}$, we have

$$I_{DS} = \frac{\beta W}{2I}\left[2\,(V_{GS} - V_{TO} - V_{BE})\,V_{DS} - V_{DS}^2\right]\beta_{deg}$$

$$273\times10^{-6} = \left(\frac{4\times10^{-6}}{2}\right)\left(\frac{W}{L}\right) \quad 2(16.5 - 1.5 - 0.35)\ 10-(10)^2 \quad (0.67)$$

$$\left(\frac{W}{L}\right)_{load} = 0.618$$

Use a minimum width of $W_{drawn} = .3$ then $W_{eff} = .4$

then

$$l_{eff} = \frac{0.4}{0.618} = 0.65 \qquad L_{drw} = 0.65 + 2(0.1) = \underline{0.85}$$

Switch Design

The worse case design of the switch is done by examining the I_{DS} equation to determine which parameter will maximize the $(\frac{W}{L})$ switch.

$$I_{DS} = \frac{\beta W}{2L}\left[2\,(V_{GS} - V_{TO})\,V_{DS} - V_{DS}^2\right]\beta_{deg}$$

Note that the body effect, V_{BE}, term is zero since the substrate and source are at the same potential.

The parameters to use are

$$\beta_{min} = 2.5$$

$$V_{TO(max)} = 2.5$$

The current flow in the load device must now be calculated using these parameters.

$$|V_{GS}| > |V_{DS}| + |V_{TH}|$$

$$|16.5| > 10 + 2.85$$

$$16.5 > 13.85$$

load device is still in triode region and

$$I_{DS} = \frac{\beta W}{2L}\left[2\,(V_{GS} - V_{TO} - V_{BE})\,V_{DS} - V_{DS}^2\right]\beta_{deg}$$

For $\rho_S = 5\Omega$-cm, $V_{BE} = 0.35$

For β_{deg} @ $V_{GS} - V_{TH} = 16.5 - 2.5 - 3.5 = 13.75$

$$\beta_{deg} = 0.68$$

$$I_{DS} = \left(\frac{2.5\times10^{-6}}{2}\right)(0.618)\quad 2(16.5-2.5-0.35)\ 10-(10)^2\quad (0.68)$$

$$I_{DS} = 88\mu A$$

This value of current is now used to calculate the $(\frac{W}{L})_{swt.}$ ratio of the switch.

Check for region of operation

$$|V_{GS}| \overset{?}{>} |V_{DS}| + |V_{TH}|$$

$$7 > 1 + 2.5$$

$$7 > 3.5$$

in triode region.

$$I_{DS} = \frac{\beta W}{2l}\left[2(V_{GS} - V_{TO})\ V_{DS} - V_{DS}^{2}\right]\beta_{deg}$$

For $V_G - V_{TH} = 7 - 2.5 = 4.5V$, $\beta_{deg} = 0.85$

$$88\times10^{-6} = 2.5\times10^{-6}\ \left(\frac{W}{L}\right)\left[2(7-2.5)\ 1 - 1\right](0.85)$$

$$\left(\frac{W}{l}\right)_{swt} = 10.3$$

Assume $\underline{l_{eff} = 0.2}$ $\qquad l_{drw} = 0.2 + (2)\ (0.1) = \underline{0.4}$

$W_{eff} = (0.2)\ (10.3) = \underline{2.06}$ $\quad W_{drw} = 2.06 - .1 = \underline{1.96}$

A similar technique can be used for a saturated load device using the proper equations.

DC Analysis

There are three analyses to be done on the inverter, now that it is designed:

1) DC Power
2) DC Noise Immunity
3) Transient Analysis
   a) Rise and Fall time
   b) Propagation delay

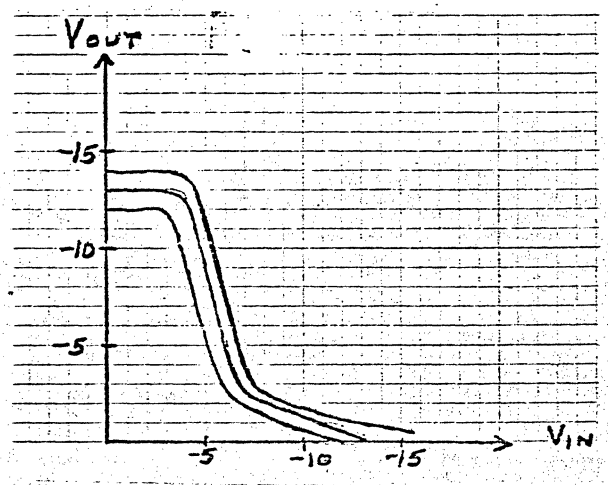
DC Noise Immunity

The noise immunity designed into the inverter is a function of the choice of output zero level, input one level, and the threshold voltage $V_{T\emptyset}$. Measurements often required are Noise Sensitivity, Noise Imminity, and Output Impedance. This information is derived from two curves:

1) Transfer curve.
2) Output loading curves.

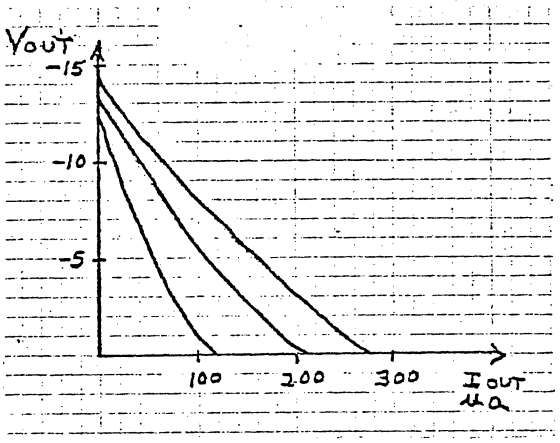
Typical, worst and best case examples are shown:

Transfer-Curve

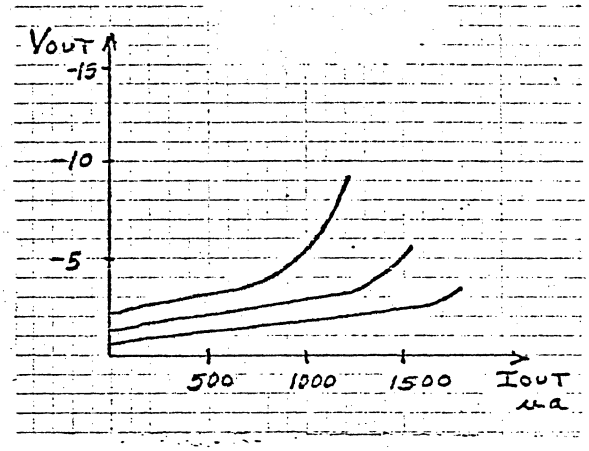


Output Loading

1 Level



0 Level



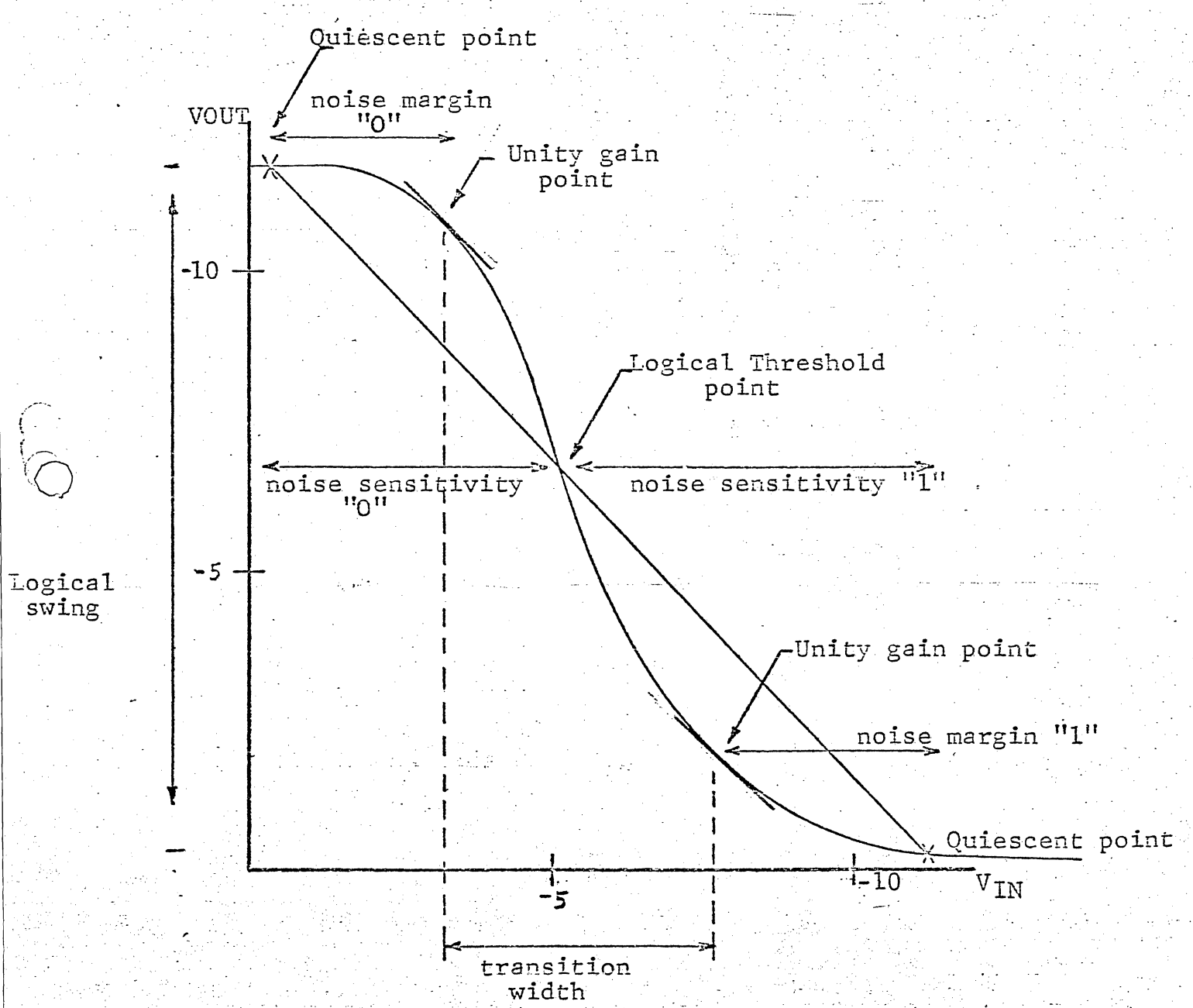
Measurement[1] of noise immunity is shown in graph 9.5. The engineer should be sure that his input-output buffers meet signal level and noise immunity requirements with worst and best case processing. The engineer can compute the noise margin required for cells on the chip by considering the capacitive coupling between signal lines and cell output impedance.

MOS offers higher voltage noise immunity than many logic types to inductively coupled noise since this tends to act as a voltage source. MOS has lower noise immunity than other logic types to capacitively coupled noise since this tends to act as a current source, and MOS impedances are typically very high. The maximum current spike immunity is:

$$I_{spike} = \frac{\text{Noise Margin}}{Z_{out}}$$

[1] See page 154 "Analysis and Design of Integrated Circuits", Lynn, Meyer, and Hamilton

GRAPH 9.5



$$\text{Noise immunity} = \frac{\text{noise sensitivity}}{\text{logical swing}}$$

Power Analysis

The power analysis is important for a knowledge of the package dissipation requirements. The current for each cell is derived by analyzing the load device with Minimum, Typical, and Maximum current, processing parameters. From this, the power dissipation range is calculated for the cell.

After all the cells are designed the dissipation range of the chip can be calculated. For some logical state, the chip dissipates its maximum power. This heat is dissipated to the ambient heat sink through the thermal impedance of the package. However, the package thermal impedance varies significantly with mounting techniques.

Thermal Impedance

The thermal impedance, θ, determines the difference between the chip temperature and ambient temperature by the formula:

$$T_{chip} - T_{sink} = \text{Power} \times \theta$$

Chip temperature should not be above 150°C., when the logic state dissipates maximum power. The thermal impedance of the package varies with mounting techniques, however. For example a 16 pin package in still air has a θ of °C/watt. (See figs.

For a given mounting technique, the ambient sink temperature must be low enough that the chip temperature is not above 150°C:

$$T_{sink}\ ^{\circ}C \leq 150 - \text{Power}_{(max)} \times \theta$$

θ_{jA} is defined as the thermal impedance from junction to ambient.
θ_{jC} is defined as the thermal impedance from junction to case.

Fig 9.6

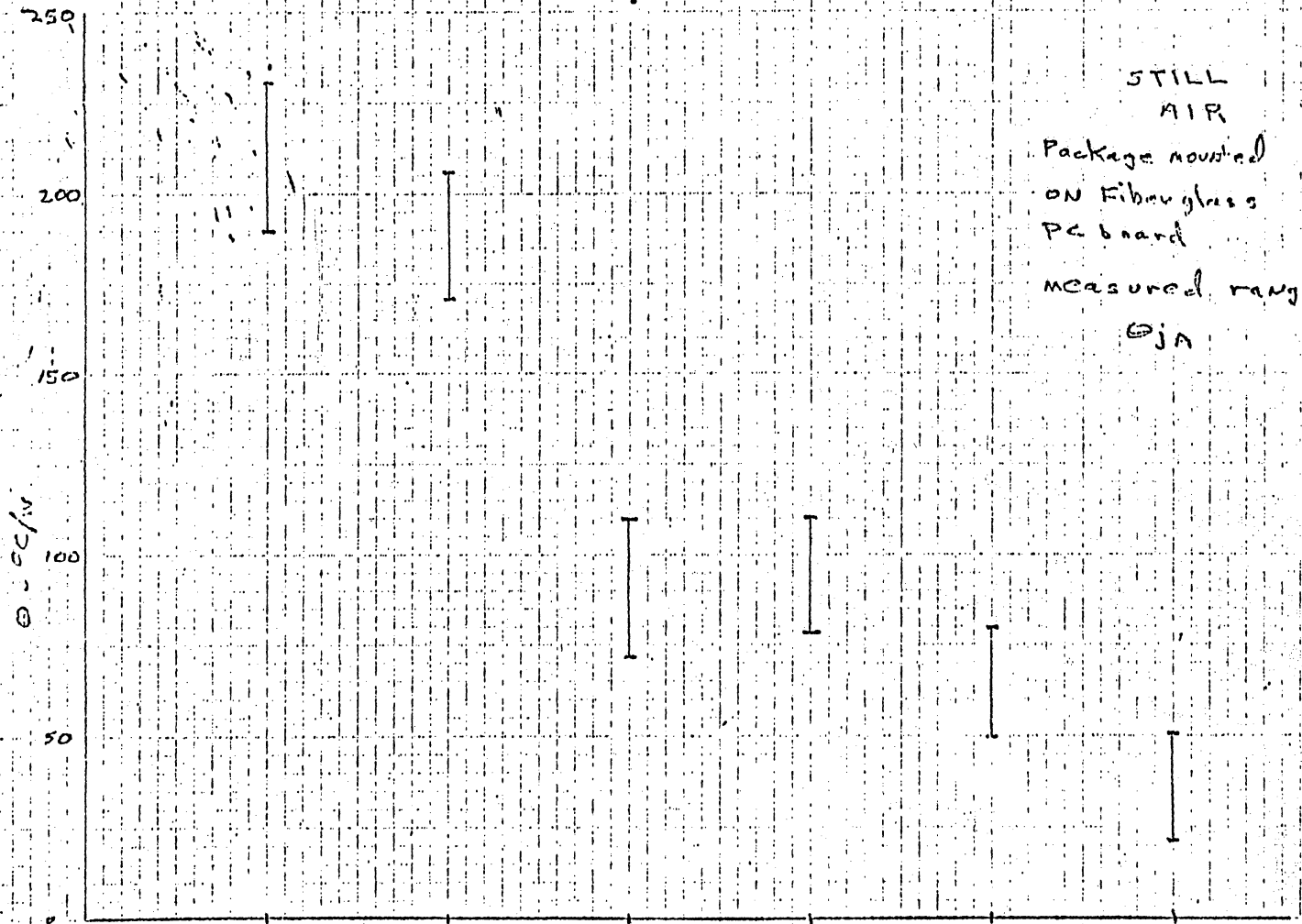

250
200
150
100
50
0
θ - °C/W
STILL AIR
Package mounted on Fiberglass PC board
measured range θJA
TO-5 8 PIN
TO-5 10 PIN
14 PIN WHITE CERAMIC
16 PIN WHITE CERAMIC
24 PIN WHITE CERAMIC
40 PIN WHITE CERAMIC

Fig 9.7

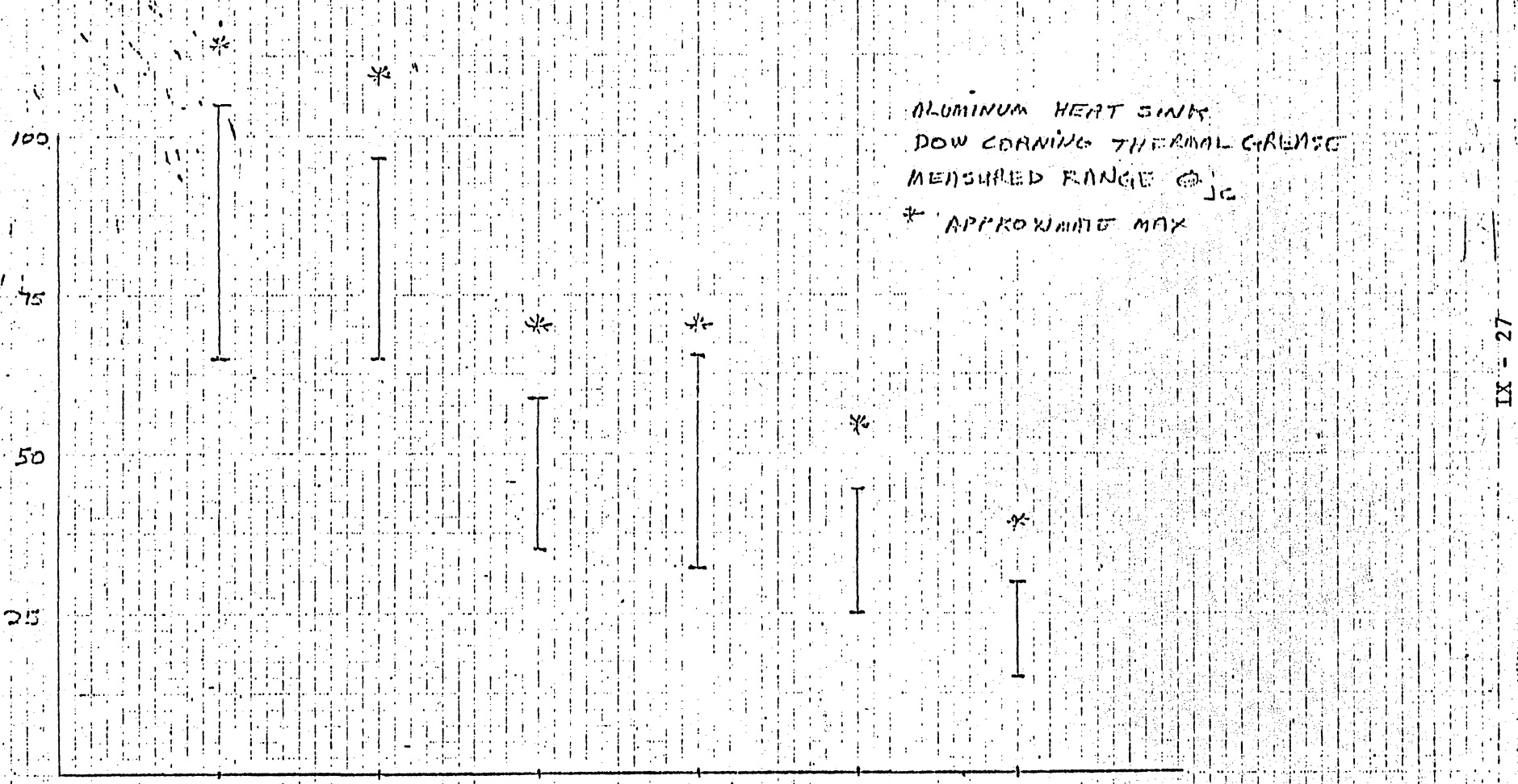
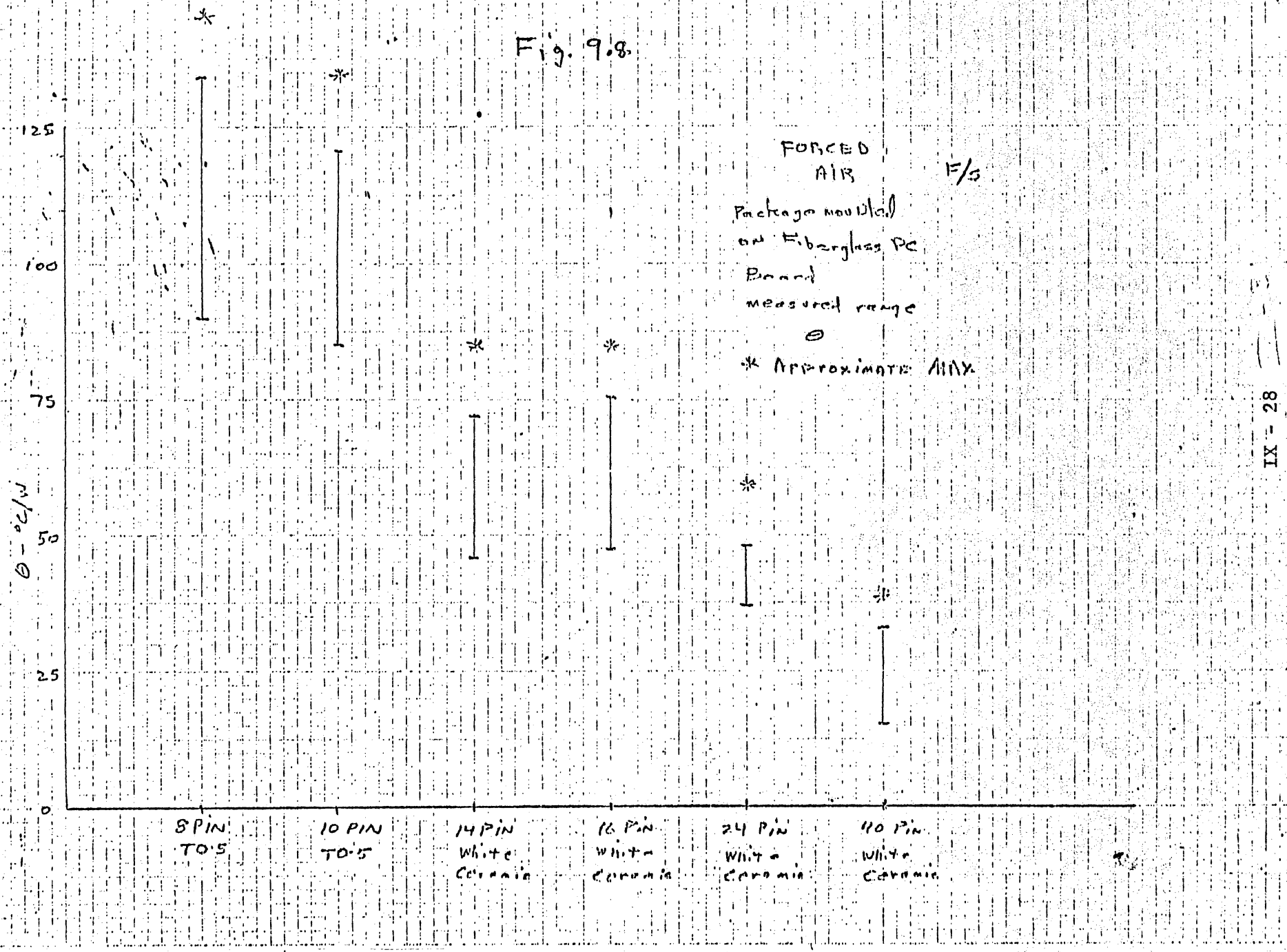

ALUMINUM HEAT SINK
DOW CORNING THERMAL GREASE
MEASURED RANGE @ T_C
* APPROXIMATE MAX
100
75
50
25
8 PIN TO5
10 PIN TO5
14 PIN WHITE CERAMIC
16 PIN WHITE CERAMIC
24 PIN WHITE CERAMIC
40 PIN WHITE CERAMIC

Fig. 9.8.

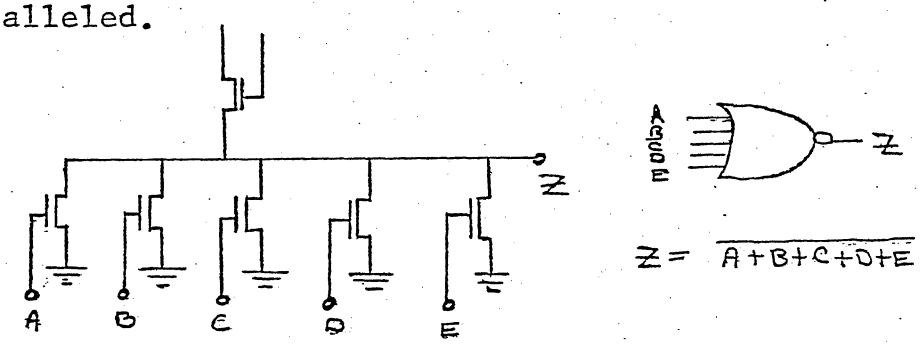

FORCED AIR
Package mounted on Fiberglass PC Board
measured range
* Approximate MAX
θ - °C/W
125
100
75
50
25
0
8 PIN TO-5
10 PIN TO-5
14 PIN White Ceramic
16 PIN White Ceramic
24 PIN White Ceramic
40 PIN White Ceramic

Logical Function Generation

The generation of a simple Boolean function in MOS positive or negative logic is simply a matter of placing devices in series or parallel.

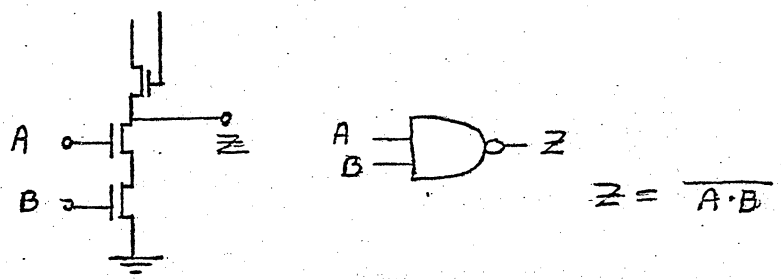
In negative logic the "or" function is done by paralleling, the "and" function by putting elements in series.

For example the 5 input NOR is a modified inverter with the switch device paralleled.



The worst case path to ground is one switch on, the remainder off. Each switch transistor is therefore the same size as in the inverter.

The two input NAND is a modified inverter with the switches in series.

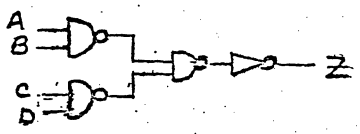


The worst case path to ground is through 2 transistors. To keep the total resistance the same, the resistance of each switch device must be half that of the inverter switch. Therefore, the $\frac{W}{L}$ ratio and therefore W_{drawn} of the switch must be twice that of the inverter switch. It is obvious that NAND structures should be limited since the transistor size multiplies by the number

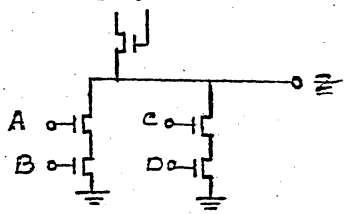
of NAND inputs.

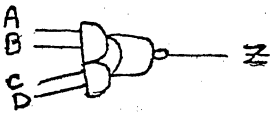
The NOR structure fan-in must also be limited because of the leakage of the MOS device in the off state.

Suppose we need the Boolean function $Z = \overline{(A \cdot B)+(C \cdot D)}$. The simple NAND-NOR logic would be:

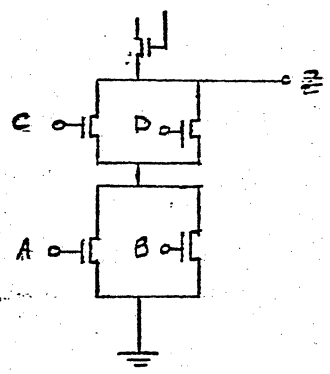


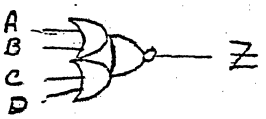
This is done simply in MOS with 1 cell:



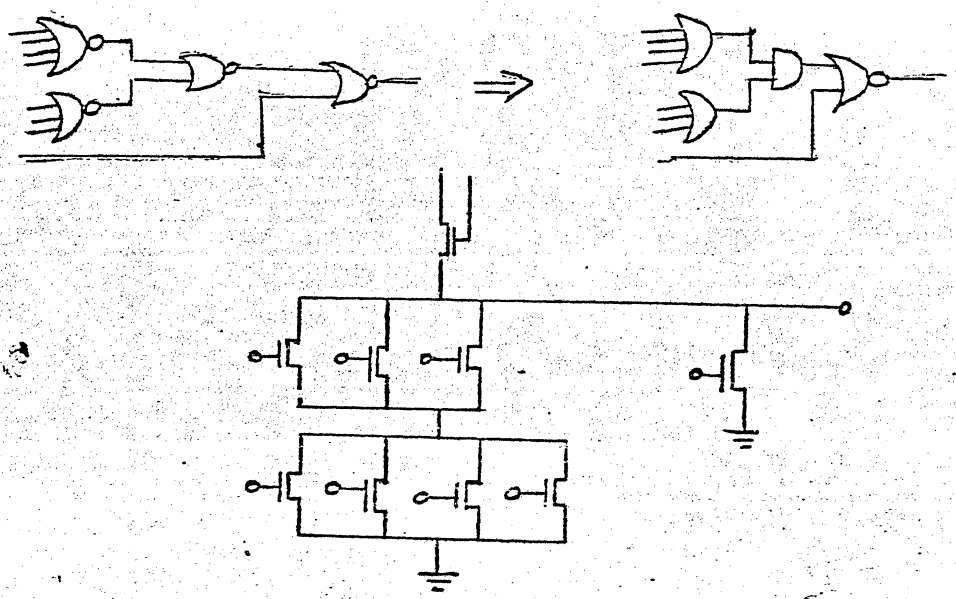


Similarly $Z = \overline{(A+B).(C+D)}$ is done as follows:

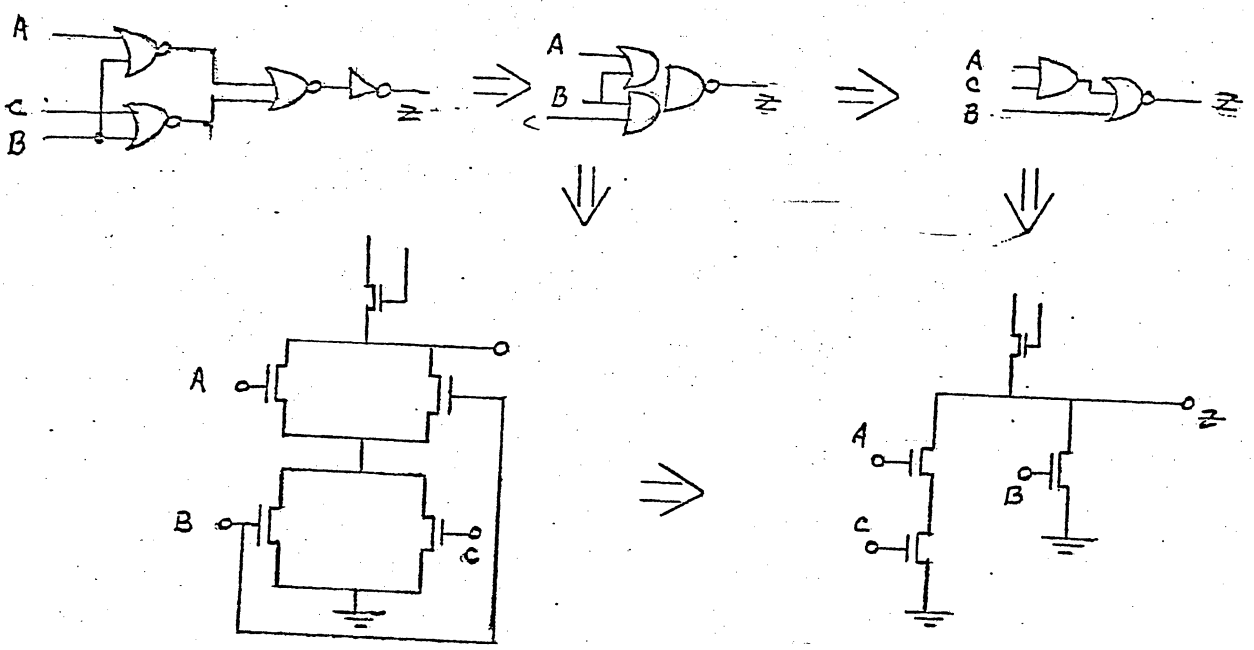




And extremely complex structures can be built reducing the required logic, and chip area.

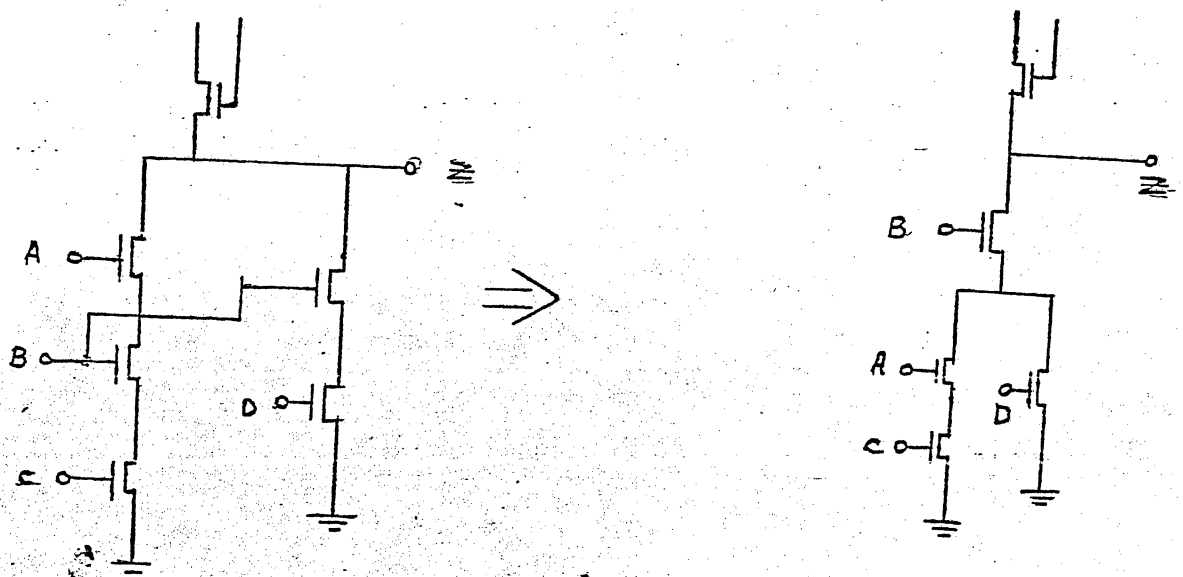


The engineer should be careful to remove superfluous transistors:



Notice the size of B is reduced 1/4.

SIMILARLY



Worst Case, Two Sigma, and Monte Carlo

Worst Case

The previous sections describe worst case design. However, the probability of all parameters being worst case simultaneously is extraordinarily low. Circuits need only be designed for those events in extraordinary applications.

Two Sigma

A somewhat more reasonable design is done by replacing the absolute limits of the parameters with limits which assure a 95% probability of occuring. This is reasonable on the assumption that not all parameters will be near worst case limits simultaneously.

Monte Carlo

A more realistic design results from Monte Carlo statistical techniques. This technique is particularly useful for optimizing a design between opposing design criteria such as high speed and low power.

Monte Carlo Analysis

The Monte Carlo method is a technique for analyzing physical systems using statistical methods. Nominal values of system parameters are replaced by mathematical models in which the parameters are represented by probability distributions. The system is then solved numerous times using a computer. The results of a Monte Carlo Analysis are presented as statistical distribution of physical parameters.

For Integrated Circuit design the Monte Carlo method is useful for predicting the probability distribution of circuit test parameters, voltages, currents, etc. The method is superior to the usual worst case design. Worst case design has several drawbacks:

1) The actual probability of the worst case may be very small. In logic circuits the device sizes may be such

that chip area or processing restrictions make the results impractical.

2) No actual measure of probability is determined. The probability of one set of worst case values to another is not known.

The Monte Carlo method has some disadvantages also:

1) Probability distributions have to be determined for all parameters that vary. This requires a large amount of past history data or perhaps a prohibitive amount of testing.

2) Accurate answers often require a large number of solutions. This makes the design cost very high. A partial solution may be to use the statistical method known as "unbiased estimate" to reduce the required number of solutions.

The probability distributions, used in place of nominal values in the design model, are easily generated for use in a computer program. The only information required is the mean value, standard deviation, and an elementary subroutine. The (fortran) subroutine is as follows:

```
Function Dist. (A, DMN, SIG)
Sum = 0
DO  0, I = 1, N, 1
Sum = SUM + RND (A)
80 Dist = (SUM - 0.5*N) * SIG+DMN
RETURN
END
```

The dummy variables are:

DMN = mean value

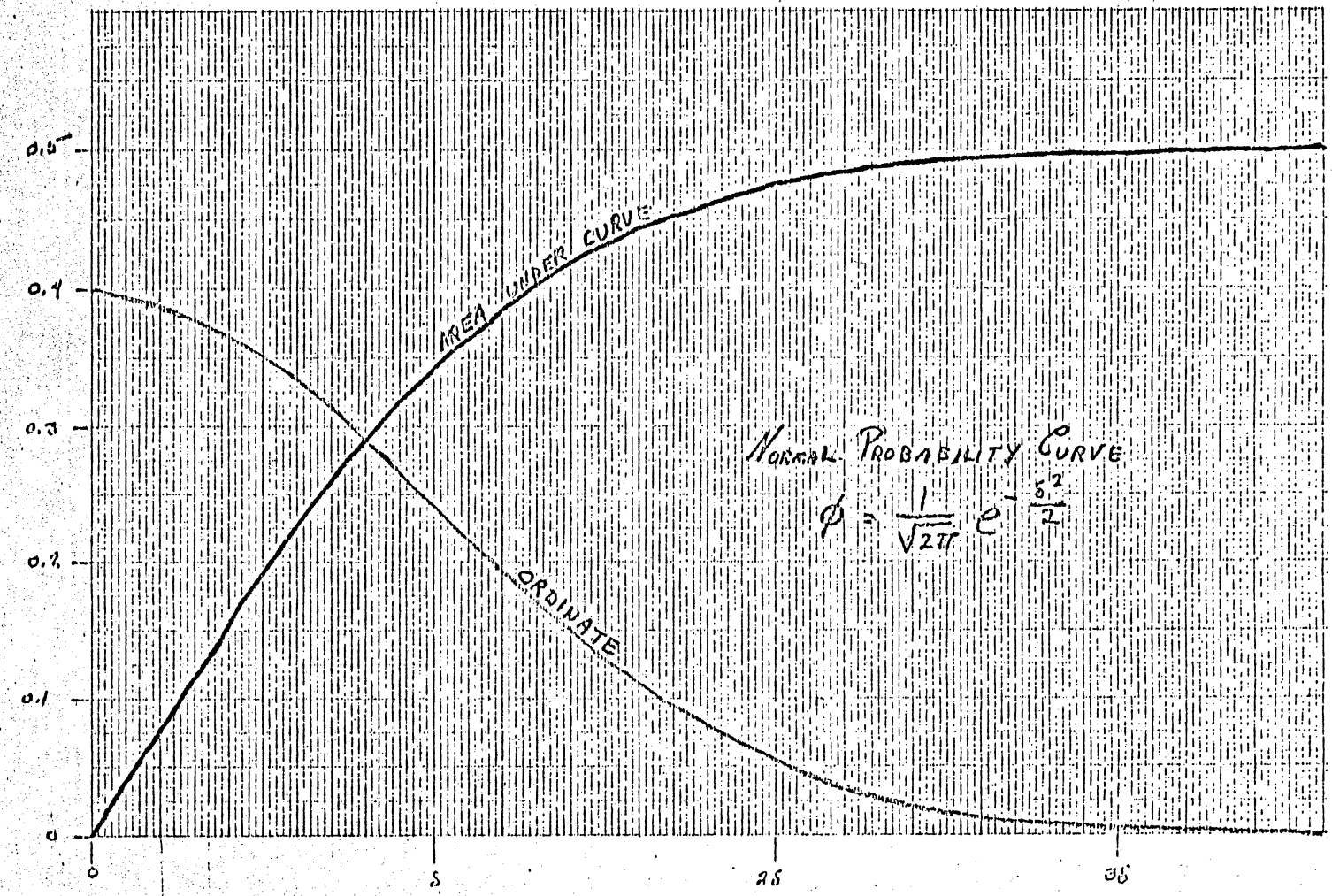
SIG = standard deviation

A = negative number which is required by random number generator to assure independant random number generation.

The results of this subroutine are then transferred to the main program and used as an iterative value. The form the value takes in the main program is:

$$V_{T\phi} = \text{DIST } (-1,4., 0.5)$$

The results of this design technique are generally very useful and correlate with the performance of the actual circuit form.


0.5
0.4
0.3
0.2
0.1
0
0
1
2
3
AREA UNDER CURVE
ORDINATE
NORMAL PROBABILITY CURVE
$\varphi = \frac{1}{\sqrt{2\pi}} e^{-\frac{z^2}{2}}$

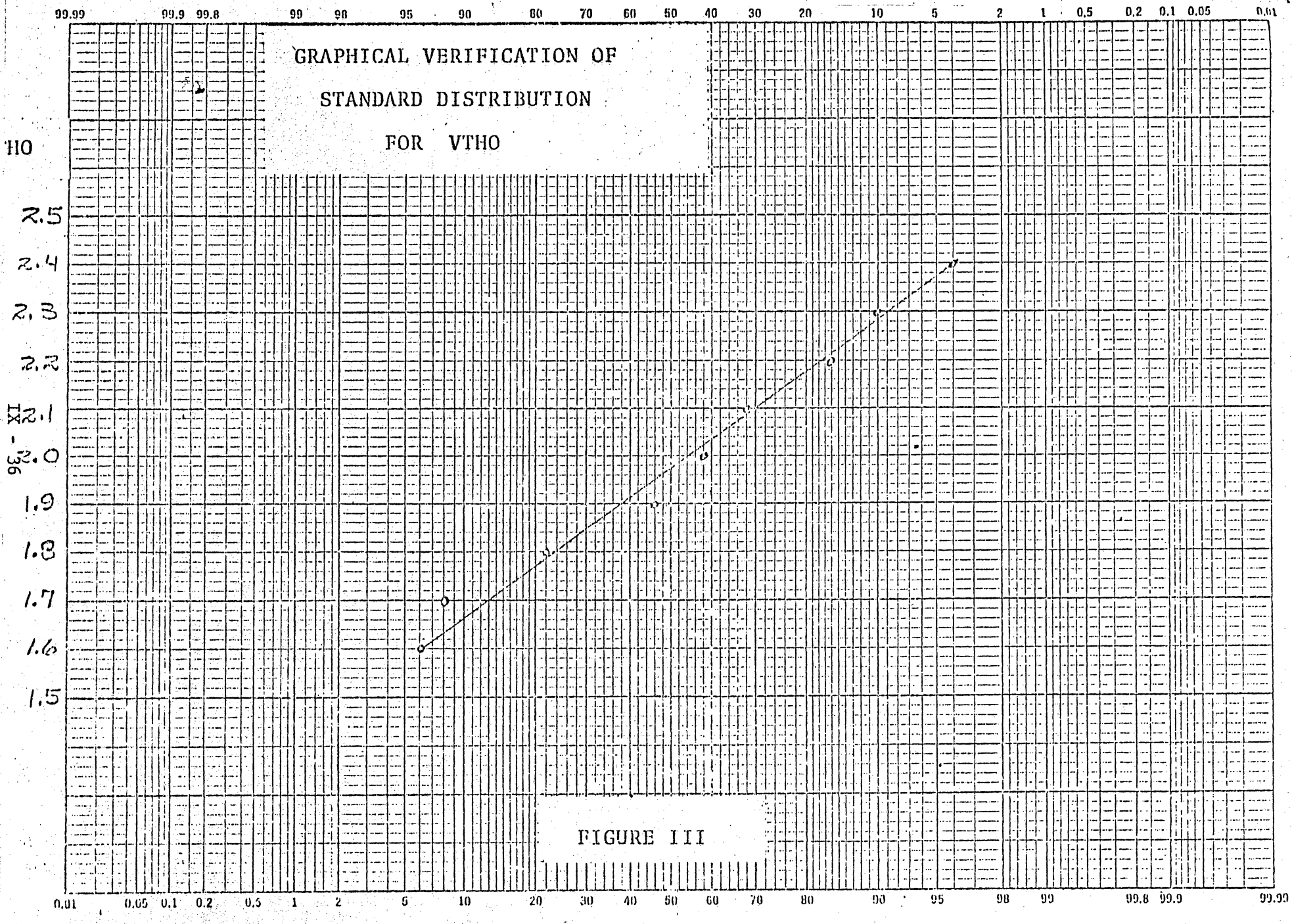


FIGURE III

Resistance

Since the source and drain of the MOS device are diffusions with high resistance, the actual device resistance will be higher than calculated. If the device must conduct considerable current then good metal contacts should parallel the source and drain.

Diffusion resistance is also used in MOS for interconnect, and on input signals to limit the current through the static protection device.

The resistance is calculated as follows:

$$R = \frac{\rho_s L}{W + .6 X_j}$$

R = resistance

ρ_s = sheet resistance $\Omega/\square$

L = length

W = drawn width

Xj= junction depth or side diffusion

For example, design a 10K resistor.

$\rho_s = 60\Omega/\square$ $\quad W_{min} = .3$ $\quad X_j = .1$

$$L = \frac{10^4 \cdot (.369)}{60} = 61.5 \text{ mils long}$$

Channel Breakdown

As in any transistor there is a maximum voltage permissible between the nodes. Approximately 100 volts will rupture the gate oxide. The Drain-Source region begins to breakdown according to the formula:

$$V_{\substack{\text{punch} \\ \text{through}}} = \frac{Q_{ND}}{2K_S\epsilon_0} (L_{eff})^2$$

Q = charge on electron = 1.6×10^{-19}

N_D = doping of substrate

K_S = dielectric constant of silicon = 11.7

ϵ_0 = free space permittivity = $8.87 \cdot 10^{-14}$

Example

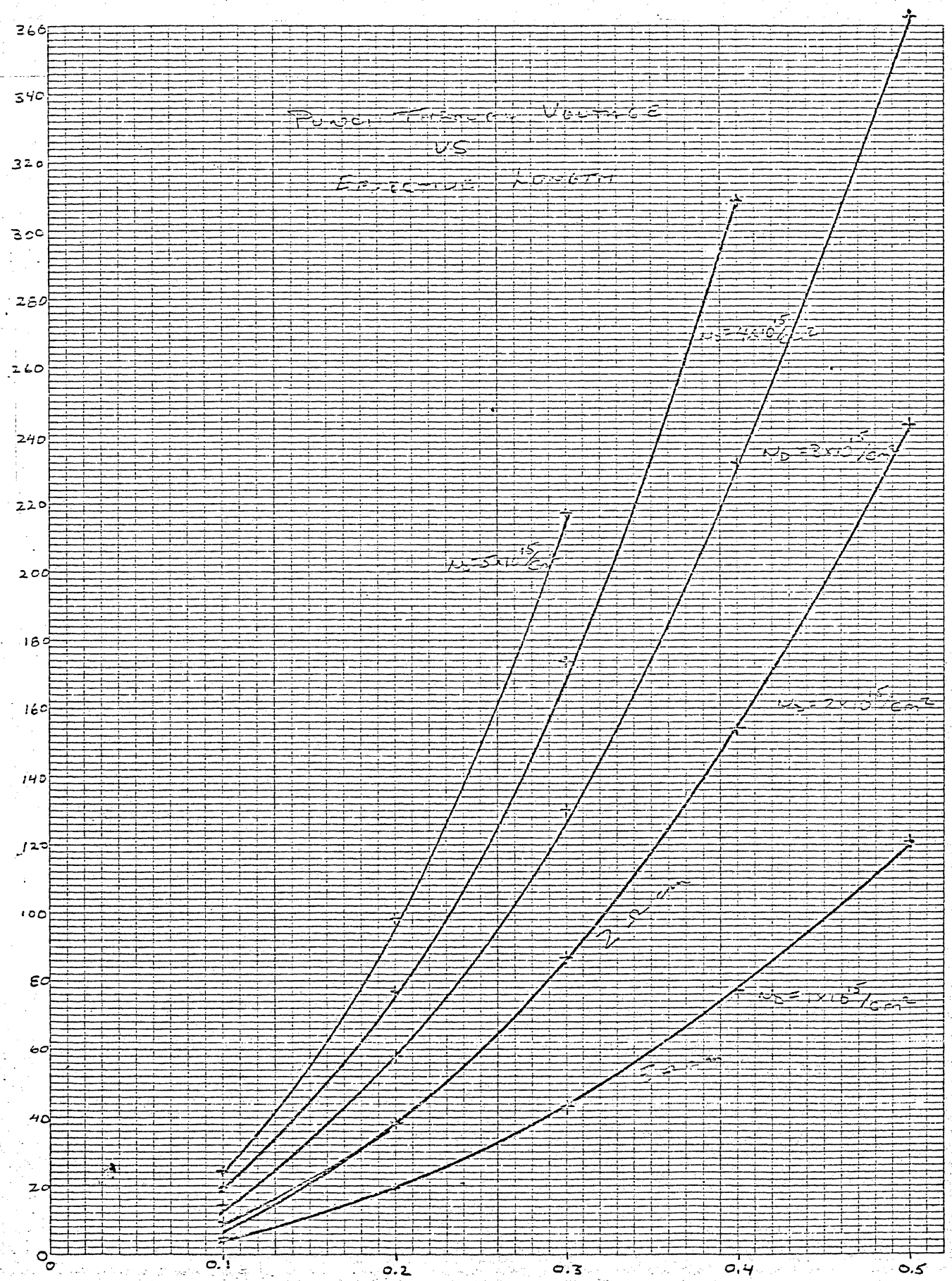
High threshold 4Ω cm substrate, drawn channel = .4 mils

$$V_{pt} = \frac{Q}{2K_S\epsilon_0} \cdot N_D \cdot (L_{eff})^2$$

$$= 4.95 \cdot 10^{-13} \cdot 1.2 \cdot 10\text{-}15$$

$$= 24 \text{ volts}$$

If metal crosses over the two P regions, the breakdown is altered somewhat.



CHAPTER X

AC ANALYSIS

AC Analysis

Logic, Shift Register, or Memory - the part is useless if its output is only steady state. The transient analysis of any function is important, in order to verify that it meets design specifications.

To explain transient analysis, the example analysis of static and two phase inverters is utilized. The AC analysis of any MOS circuit will use similar techniques.

The present approach to time domain analysis is the application of the DC MOS device model, the constant capacitances, and the nonlinear diffusion capacitance models to various time step integrating routines.

First, the diffusion capacitance model is presented, then approximation methods to this capacitance.

Step-by-Step Procedure for Calculating Junction Capacitance

Given: X_j, ρ, ρ_s for the specified process

1. Calculate grade constant for Gaussian diffusion, using the formula

$$a = \text{grade constant} = \frac{2\ N_{BC}}{X_j} \quad \ln\left(\frac{N_o}{N_{BC}}\right)$$

where

N_{BC} = substrate concentration (N-type)

N_o = surface concentration of P-diffusion

a) Find on vertical axis of resistivity vs. impurity of Irvin's curve concentration graph. Read N_{BC} for n-type material on horizontal axis.

b) Calculate effective conductivity $= \rho_s \frac{1}{X_j}$, where

ρ_s is expressed in $\Omega/\square$

X_j is expressed in cm (.1 mil=$2.54 \cdot 10^{-4}$ cm)

c) Determine N_o from the vertical axis of the appropriate sheet of Irvin's curves.

Note: On Irvin's curves, $N_o = C_s$

$N_{BC} = C_B$

d) Calculate a.

2-a) Read Contact potential ϕo from graph of contact potential vs. grade constant.

2-b) Read Equilibrium Capacitance per mil^2 C_o from graph of capacitance vs. grade constant.

3-a) Calculate bottom component of junction area. (length x width)

3-b) Calculate sidewall component of junction area.

sidewall area $\doteq$ (perimeter)$\times(\frac{\pi}{2} X_j)$; perimeter & X_j in mils.

3-c) Add 3-a & 3-b to get total junction area

4) For a given logic swing of ϕ_2-ϕ_1 volts, calculate the average capacitance $\overline{C}$ from the equation

Capacitance Calculation Example

Find capacitance of P-diffusion 61.5 x .3 mils, voltage swing from $\phi_1 = -1$ to $\phi_2 = -11$

$\rho = 4\Omega cm$ (n-type substrate)

$\rho_s = 60\Omega/\square$ (P-diffusion)

$X_j = .1$ mil $= 2.54 \cdot 10^{-4}$ cm (diffusion depth)

From graph $4\Omega cm \Longrightarrow N_{BC} = 1.2 \cdot 10^{15}$

$$= \frac{1}{\rho_s X_j} = \frac{1}{60 \cdot 2.54 \cdot 10^{-4}} = \frac{10^2}{1.52} = \frac{1}{66\Omega cm}$$

$N_D = 2 \cdot 10^{19}$ (Irvin's Curve)

$$a = \frac{2N_{BC}}{X_j} \ln\left(\frac{N_D}{N_{BC}}\right)$$

$$= \frac{2 \cdot 1.2 \cdot 10^{15}}{2.54 \cdot 10^{-4}} \ln\left(\frac{2.10^{19}}{1.2 \cdot 10^{15}}\right)$$

$$= 9.45 \cdot 10^{18} \ln(1.66 \cdot 10^4)$$

$$= 9.2 \cdot 10^{19}$$

$\phi_0 = -.655$

$C_0 = 8.2 \cdot 10^{-2}$

$$A = (61.5) \cdot (.3) + 123\ (\pi/2)(.1)$$

$$= 18.4 + 19.4$$

$$= 37.8$$

$$\overline{C} = \frac{(8.2 \cdot 10^{-2})(37.8)(-.665)}{(-10)(.66)} \left[\frac{11}{(1+.665)}^{2/3} - \frac{1}{(1+.665)}^{2/3}\right]$$

$$= .312 \left[(17.66)^{2/3} - (2.5)^{2/3}\right]$$

$$= .312\ (4.96)$$

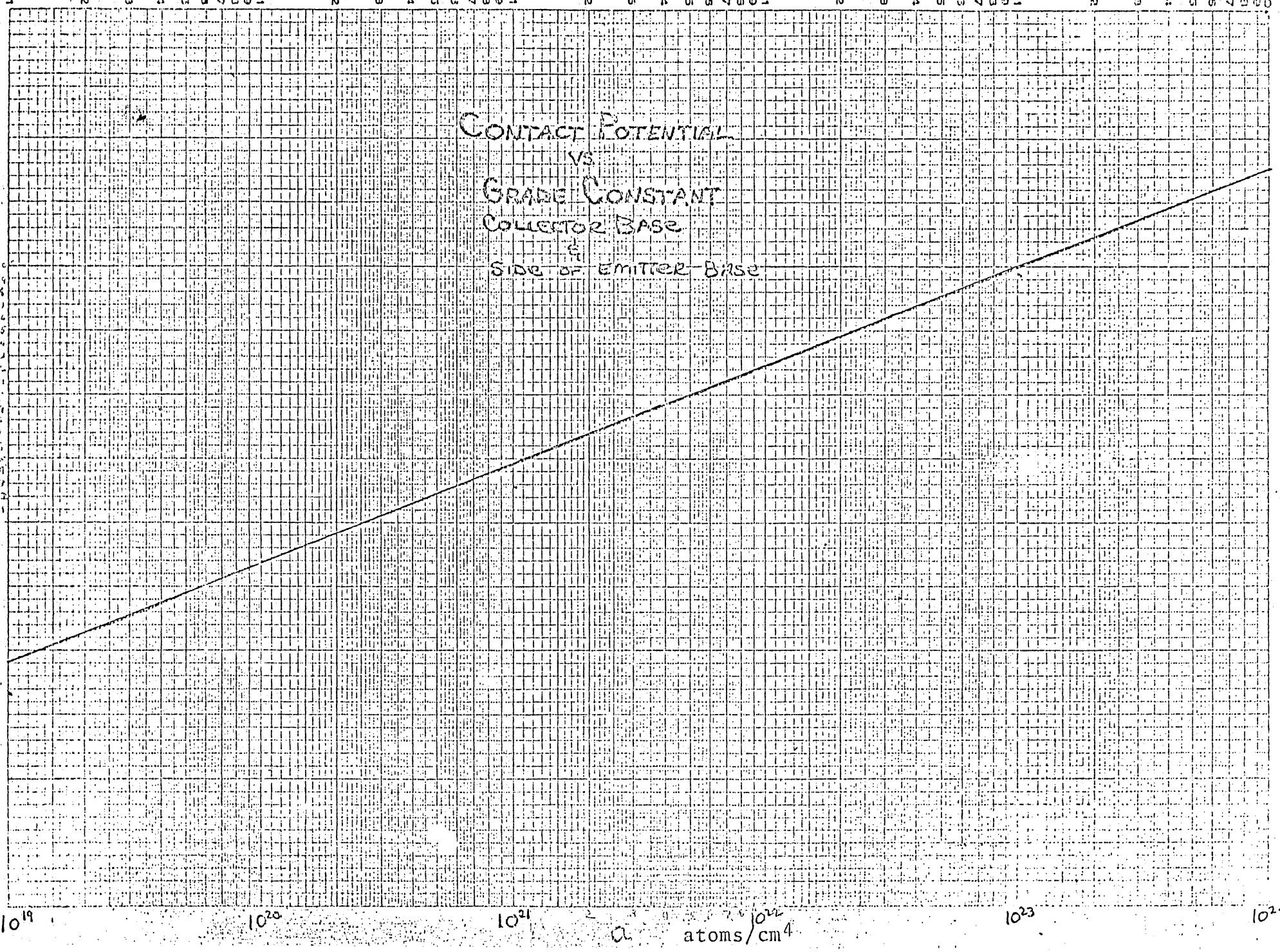
$$= 1.55pf$$

Note that rough approximations for capacitance are:

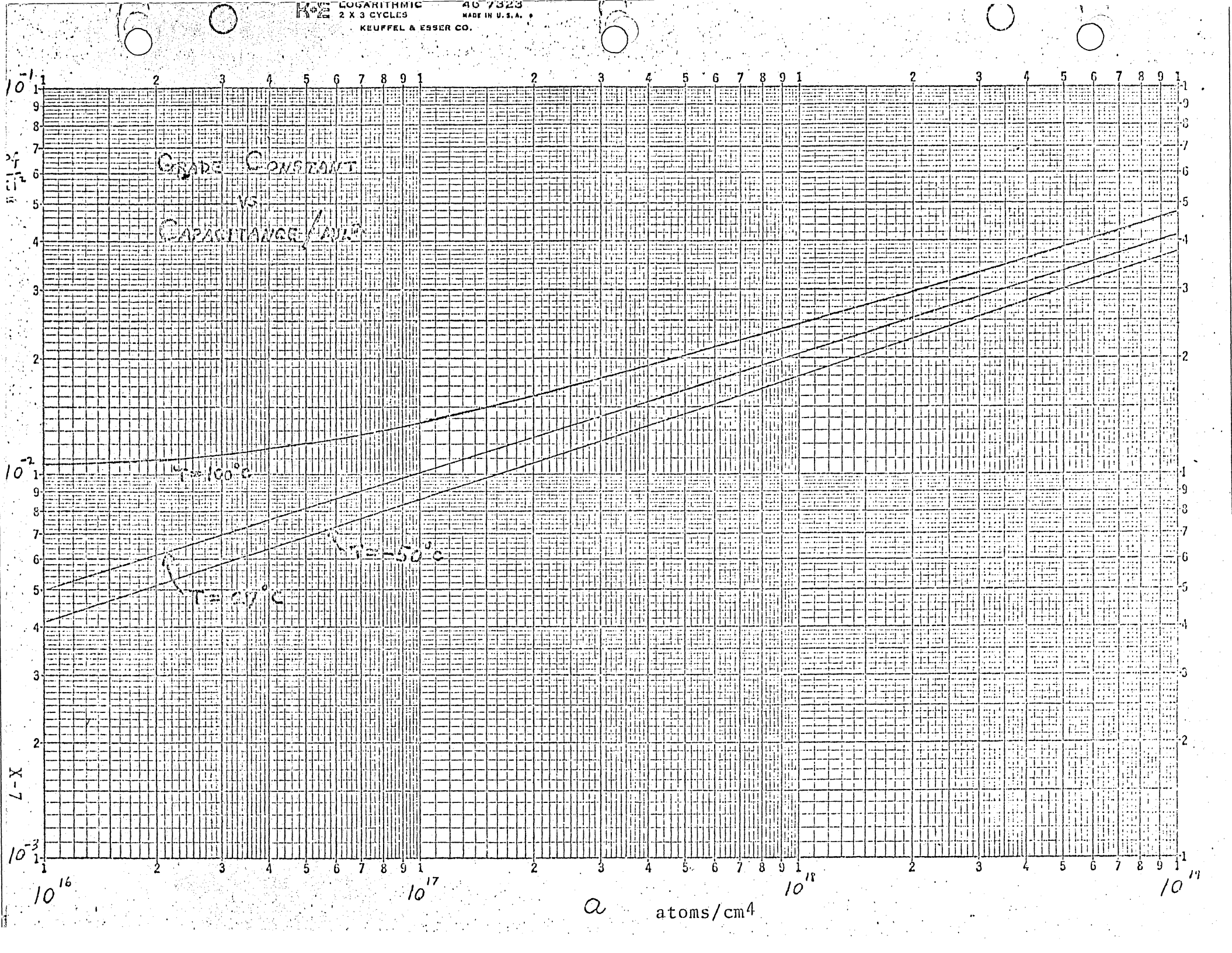
P-diffusion	.03 pf/mil^2 (4Ωcm substrate)
Metal over thick oxide	.023 pf/mil^2
Metal over thin-oxide	.176 pf/mil^2

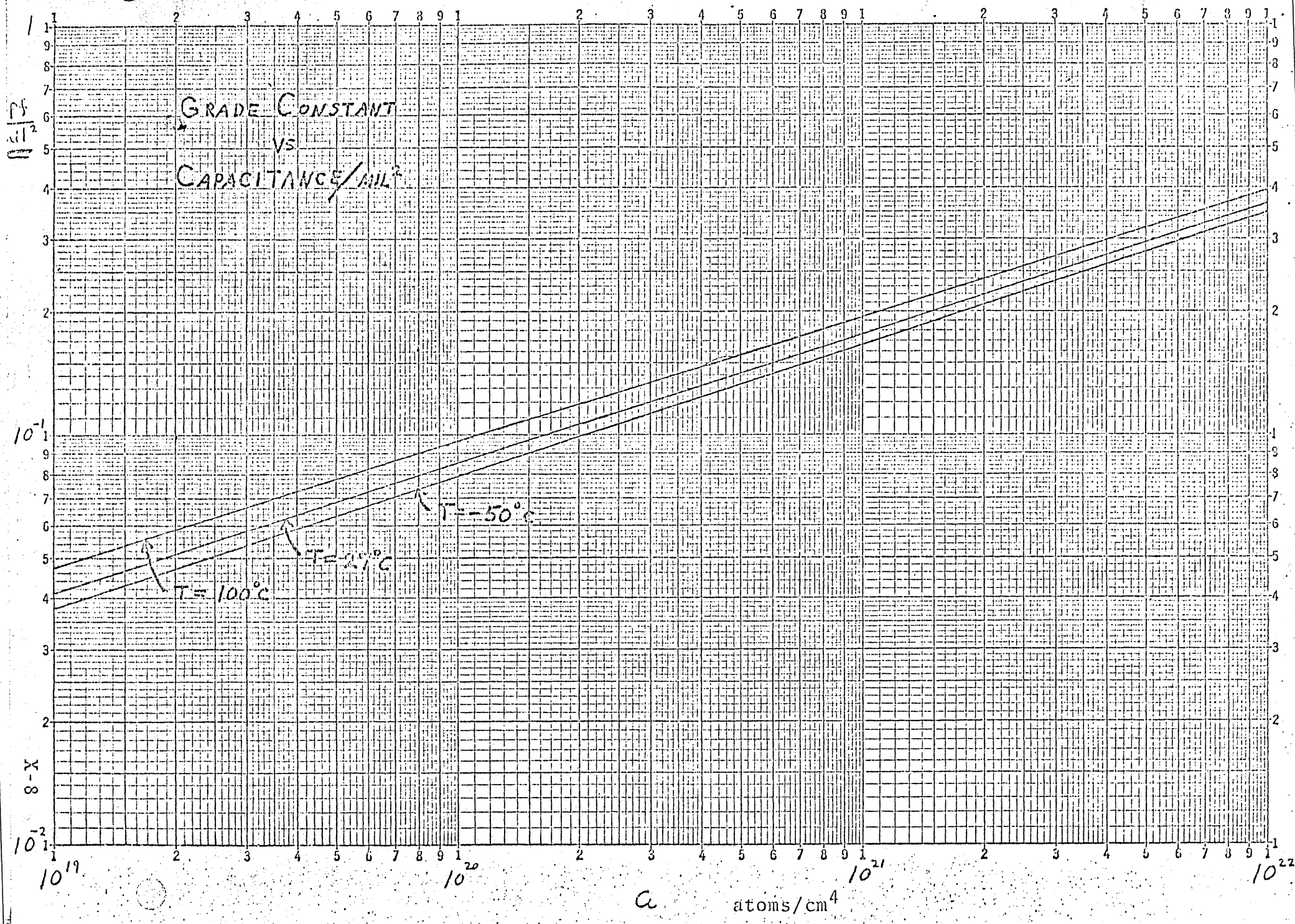
SEMI-LOGARITHMIC
5 CYCLES X 10 DIVISIONS PER INCH

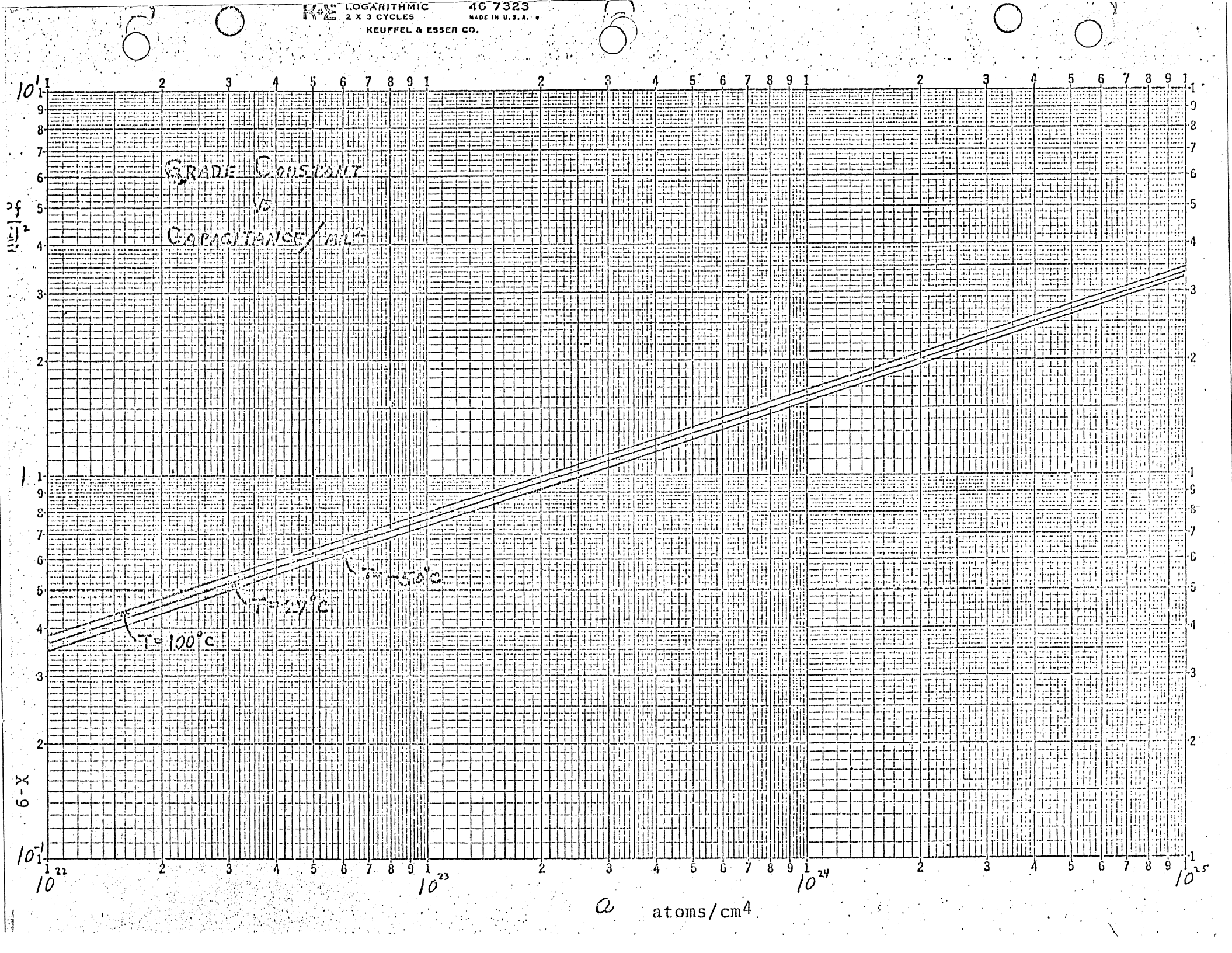
MADE IN U. S. A.



9-X


K&E LOGARITHMIC 46 7323
2 X 3 CYCLES MADE IN U.S.A.
KEUFFEL & ESSER CO.
GRADE CONSTANT
VS
CAPACITANCE (AUC)
T = 100°C
T = 150°C
T = 200°C
X-7
a atoms/cm4




K&E LOGARITHMIC 46 7323
2 X 3 CYCLES MADE IN U.S.A.
KEUFFEL & ESSER CO.
GRADE CONSTANT
VS
CAPACITANCE/AREA
T = 100°C
T = 27°C
T = -55°C
a atoms/cm4

AC Analysis

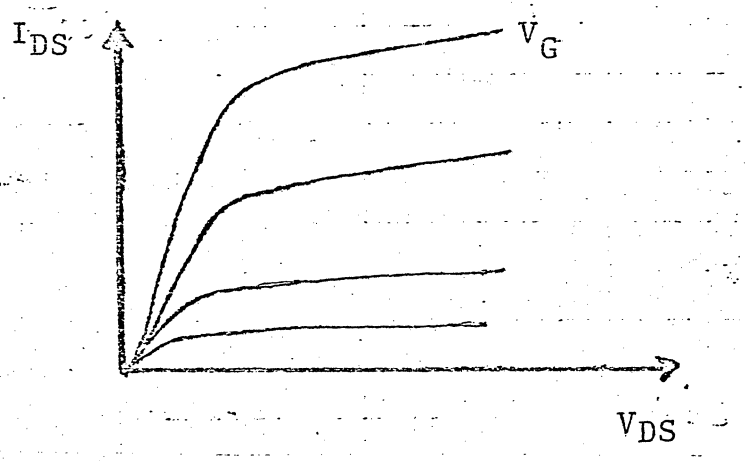
This analysis will only be concerned with the static logic gate AC characteristics.

The unsaturated or triode biased load device will give a faster switching speed (for the same amount of power) than the saturated load device. This is because the unsaturated load remains turned on during the switching transient. (See fig. 1)

The higher the gate voltage becomes, the more linear the load V-I characteristics become and thus the load approaches a constant resistor whose time constant is given by

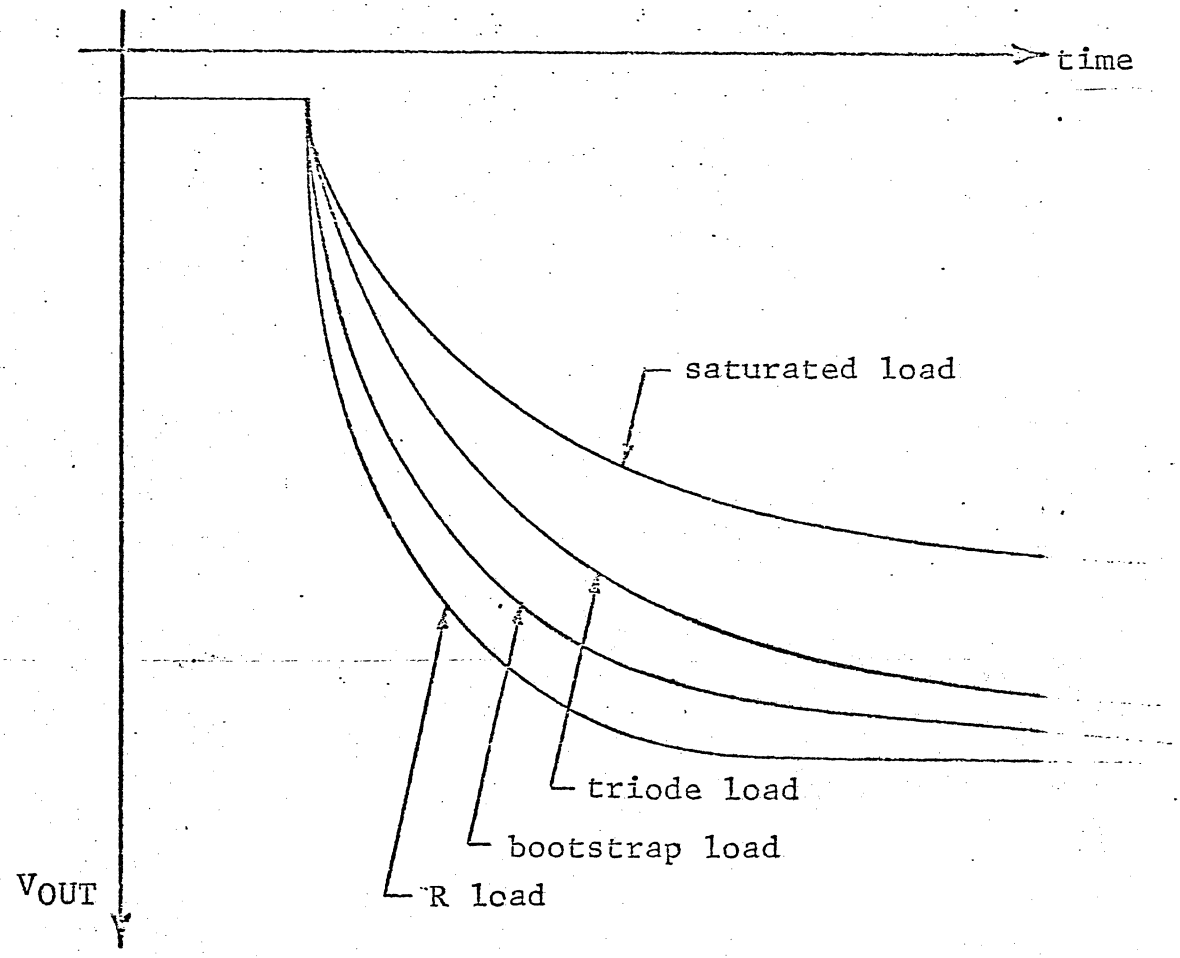
$$T = 2.2R_LC_L \quad (10\% - 90\%)$$

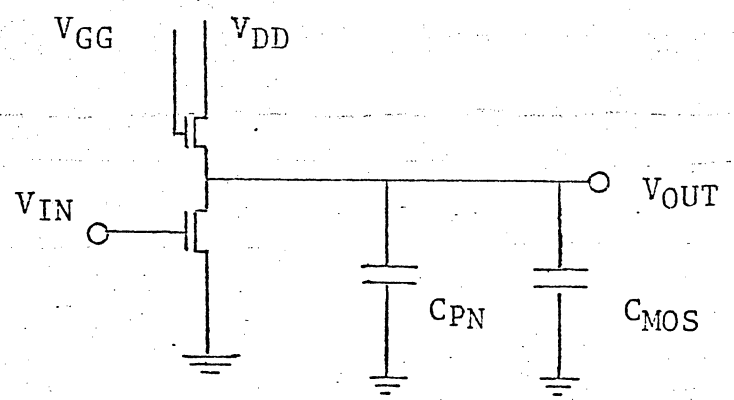
The following V-I characteristic illustrates the effect of V_{GG}.



The following inverter circuit will be used to illustrate two methods of calculating the turn-off time. The two methods are (1) a piecewise linear method and (2) a fast rough ballpark estimate.

Transient Response
of Various Load Device
Configurations





where

C_{MOS} is the capacitance associated with metal over (1) field oxide, (2) gate oxide, (3) P and N diffusion oxide. This capacitance is not a function of voltage.

C_{PN} is the capacitance associated with P-cross unders, device drain and source. It is a function of voltage. Graphs for P-N junction capacitance (pf/mil^2) as a function of voltage are included in the design manual for the various processes.

The inverter is assumed to have been turned on and the output node has been discharged to a V_{OUT} = -1 volt. Assuming an ideal step function input for the switch, V_{IN} is lowered to a logic "0" level and the switch is turned off. We now want to calculate time required for the load device to charge up the output node to a V_0 = -8V level. The following table will be used to record the results.

V_{OUT} (volts)	C_{PN} (pf)	C_{MOS} (pf)	C_T (AVG) (pf)	β deg	V_{BE} (volts)	I_{DS} (μA)	I_{DS} (AVG) (μA)	Δt (ns)
1	0.208	0.4		0.73	0.5	57		
			0.592				48	12.35
2	0.176	0.4		0.74	0.8	39		
			0.560				34.8	16.20
3	0.144	0.4		0.74	1.1	30.6		
			0.532				26.4	20.20
4	0.120	0.4		0.75	1.3	22.2		
			0.516				18.3	28.2
5	0.112	0.4		0.75	1.6	14.4		
			0.508				12.55	40.5
6	0.104	0.4		0.76	1.8	8.7		
			0.500				6.5	77.0
7	0.096	0.4		0.76	2.0	4.28		

Total Time = 194.45 ns

The following parameters will be used to determine the worse case switching time. They are determined by examining the current equation to see which parameters will minimize the current available. The inverter device sizes will be the ones obtained in the DC Analysis section.

$$I_{DS} = \frac{\beta W}{2L}\left[2(V_{GS} - V_{TO} - V_{BE})\,V_{DS} - V_{DS}^2\right]\beta_{deg}$$

$V_{GG} = -14.5V$

$V_{DD} = -9V$

$V_{TO} = -2.5$

$= 2.5\ \mu A/V^2$

$\left(\frac{W}{L}\right)$ load $= 0.618$

V_{BE} will be obtained from the $P_S = 3\ \Omega$-cm graph

β_{deg} will be obtained from the curve on page 67 of Crawford.

Assume that the following parameters were calculated from the circuit layout.

$A_{pn} = 4\ mil^2$ Area of C_{pn}

CMOS = 0.4pf

Step 1: Calculation of C_{pn}

Use the graph of P-N junction capacitance/mil^2 as a function of junction voltage. The curve for $P_s = 3\ \Omega$-cm and low threshold process (<100> material) will be used.

C_{pn} = Area x C_{pn}/mil^2 @ $V_O = 1V$

$C_{pn} = 4 \times .052$

$C_{pn} = 0.208$ pf

C_{pn} @ V_O = 2V is

$C_{pn} = 4 \times .044$

$C_{pn} = 0.176pf$

Step 2: Calculation of C_T (average) for a $\Delta V = 2-1 = 1V$

$$C_{T(AVG)} = \frac{(C_{pn(1V)} + (C_{MOS}) + (C_{pn(2)} + C_{MOS})}{2}$$

$$C_{T(AVG)} = \frac{C_{pn}\ (1V) + C_{pn}(2V)}{2} + C_{MOS}$$

$$= \frac{0.208 + 0.176}{2} + 0.4$$

$C_{T(AVG)} = \underline{0.592pf}$

Step 3: Determine deg and V_{BE}

@V_O = 1 volt $\quad \underline{V_{BE} = 0.5V}$

@$V_{GS} - V_{TO} - V_{BE} = 13.5 - 2.5 - 0.5 = 10.5V$ $\beta_{deg} = 0.73$

@V_O = 2V $\quad \underline{V_{BE} = 0.8V}$

@ $V_{GS} - V_{TO} - V_{BE} = 12.5 - 2.5 - 0.8 = 9.2V$ $\beta_{deg} = 0.74$

Step 4: Calculate I_{DS}

$$I_{DS} = \frac{\beta W}{2L} 2(V_{GS} - V_{TO} - V_{BE}) V_{DS} - V_{DS}^2) \beta_{deg}$$

@V_O = 1V

$$I_{DS} = \frac{(2.5 \times 10^{-6})}{2} (0.618) \quad 2(13.5-2.5-.5)\ 8 - 64 \quad 0.73$$

$I_{DS} = 57\mu A$

@V_O = 2V

$$I_{DS} = \frac{2.5 \times 10^{-6}}{2} (0.618) \quad 2(12.5-2.5-.8)\ 7 - 49 \quad 0.74$$

$I_{DS} = 39\mu A$

Step 5: Calculate I_{DS} (average) for $\Delta V_{cut} = 1V$

$$I_{DS(AVG)} = \frac{I_{DS}\ (1V) + I_{DS}\ (2V)}{2}$$

$$= \frac{57 + 39}{2}$$

$$I_{DS(AVG)} = 48\mu A$$

Step 6: Calculate Δt for a $\Delta V = 1V$

Using the charge density equation,

$$Q = CV = It$$

and solving for t,

$$t = \frac{CV}{I}$$

and

$$\Delta t = \frac{\Delta C \Delta V}{\Delta I}$$

$$\Delta t_1 = \frac{(0.592)(1)}{48} = \underline{12.35ns}$$

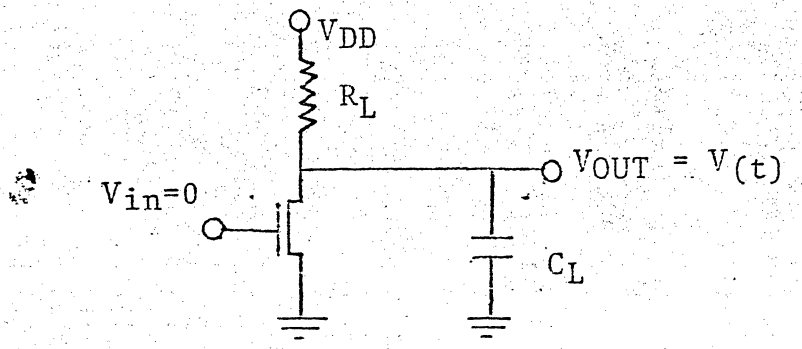
The above six steps are repeated until the table is completely filled in. The total time required for the output swing is the sum of the Δt's.

$$t = \Delta t$$

$$\underline{t = 194.45ns}$$

Rough Ball Park Estimate

If the MOS load device is treated as an average constant resistance over the operating range, we can use the following model for estimating switching speed.



Therefore, we have an exponential equation of the form

$$V(t) = V_{DD}\ (1-e^{-t/\tau}) =$$

$$V_{DD}\ (1 - e^{-t/R_LC_L})$$

If we treat the turn off time as an exponential, we can calculate its approximate value.

Step 1: Determine the average resistance of the load over the operating range.

$$R_L(V_0 = 1V) = \frac{V_{DS}}{I_{DS}} = \frac{8}{57\mu A} = 140K\Omega$$

$$R_L(V_0 = 7V) = \frac{3}{4.28\mu A} = 700K\Omega$$

$$R_L(AVG) = \frac{R_L(V_0 = 1V) + R_L(V_0 = 7V)}{2}$$

$$= \frac{140 + 700}{2}$$

$$R_L(AVG) = \underline{420K\Omega}$$

Step 2: Determine the average capacitance over the operating range.

$$C_{LAVG} = \frac{C_{pn}\ (V_O = 1V) + C_{pn}(V_O = 7V)}{2} + C_{MOS}$$

$$= \frac{0.208 + 0.096}{2} + 0.4$$

$$C_{LAVG} = \underline{0.552pf}$$

Step 3: Calculate the time constant (τ)

$$= R_{L(AVG)}\ C_{L(AVG)}$$

$$= (420x10^3)(0.552x10^{-12})$$

$$= \underline{232\ ns}$$

Step 4: Determine the number of time constants (t/τ) using the graph of ($1-e^{-t/\tau}$) vs t/τ

There is a possible voltage swing at the output of 9 volts. We are interested in only a 6 volt swing.

$$(1-e^{-t/\tau}) = \frac{\Delta V_O}{\Delta V_{DD}}$$

$$= \frac{7-1}{9-0}$$

$$(1-e^{-t/\tau}) = \frac{6}{9} = 0.67$$

and from the graph we obtain $t/\tau = 1.25$

Step 5: Calculate switching time

$$t/\tau = 1.25$$

$$t = 1.25\tau$$

$$t = (1.25)(232)$$

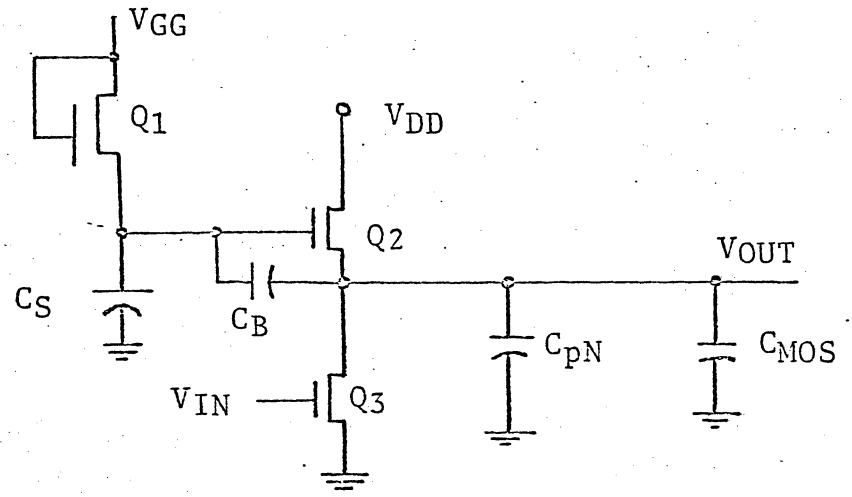
$$t = \underline{290ns}$$

This method gives a value of 290ns compared to the previous value of 194ns.

This rough estimate becomes more accurate as the values

of the load device resistance at the two extremes of the operating range approach equal values.

A bootstrap circuit can be used to improve the switching speed for the same amount of power. The circuit is as follows:



The operation of the bootstrap circuit depends upon the gate-to-source capacitance, C_B. The operation works on the principle that the voltage across a capacitor cannot be changed instantaneously. Therefore a change in the output, V_{OUT}, will be reflected at the gate of Q_2 by an amount given by

$$\Delta V_O \frac{C_B}{C_B + C_S}$$

Therefore, for transistor Q_2

$$V_{GS} = V_{GG} - V_{TH} + V_O \left[\frac{C_B}{C_B+C_S} - 1\right]$$

$$V_{DS} = V_{DD} - V_O$$

For this circuit V_{GS} of Q_2 remains almost constant except for the amount of charge lost to the stray capacitance, C_S.

A design example will now be illustrated.

The same parameters as in the previous AC Analysis and the following assumptions will be used.

Assume:

1) $\beta_{deg} = 0.73$

2) Q_3 is off

3) No more 10% loss to C_{stray} for each $\Delta V_O = 1$ volt.

4) Q_2 is saturated

5) $\Delta C_{T(AVG)}$ is same

Step 1:

To compare the speeds between the bootstrap circuit and the triode inverter, we must have the same power drain. Therefore, we must calculate an effective length for Q_2 to give the same I_{DS} value initially as before.

$$I_{DS} = \frac{W}{2l} (V_{GS} - V_{TO} - V_{BE})^2 \beta_{deg}$$

$$57\mu A = \frac{(2.5\times10^{-6})(0.4)}{2l'} \left[(14.5 - 2.5 - 2.4) - 2.5 - 0.5\right]^2 (0.73)$$

$l' = 0.263$ mil

Step 2:

Calculate I_{DS} current using, the l' calculated in Step 1 and using the 10% loss of gate to source voltage (V_{GS}) where V_{GS} initially is equal to 9.4V.

$$I_{DS1} = \frac{(2.5)(0.4)}{(2)(0.263)} \left[(9.3 - 2.5 - 0.8)^2\right] (0.73)$$

$I_{DS1} = 50\mu A$

$$\Delta t = \frac{C_{T(AVG)}}{I_{DS(AVG)}} = \frac{0.592}{53.5} = \Delta t = \underline{11ns}$$

Similar calculations can be done to generate the following table:

V_{OUT} (volts)	$C_{T(AVG)}$ (pf)	I_{DS} (μA)	$I_{DS(AVG)}$ (μA)	Δt (ns)
1		57		
	0.592		53.5	11.0
2		50		
	0.560		46.7	12.0
3		43.5		
	0.532		41.25	12.9
4		39.0		
	0.516		36.2	14.3
5		33.4		
	0.508		31.4	16.2
6		29.4		
	0.500		27.5	18.2
7		25.7		
			Total time =	84.6 ns

This switching time is considerably lower than the previous circuit's time of 194ns.

The advantages of the bootstrap are

1) faster rise times

2) Improved speed-power product

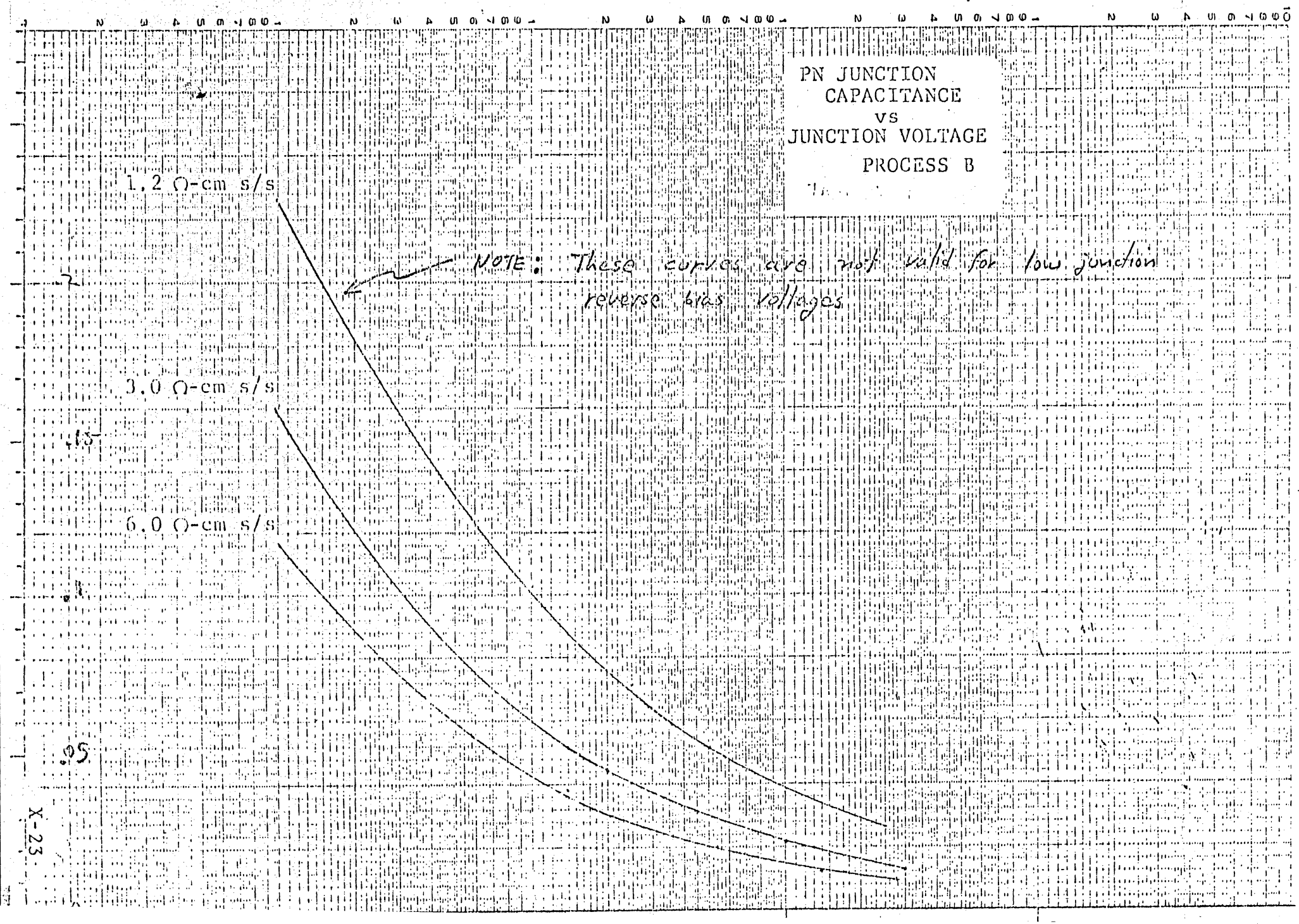
Some of the disadvantages are:

1) Requires an extra MOS device

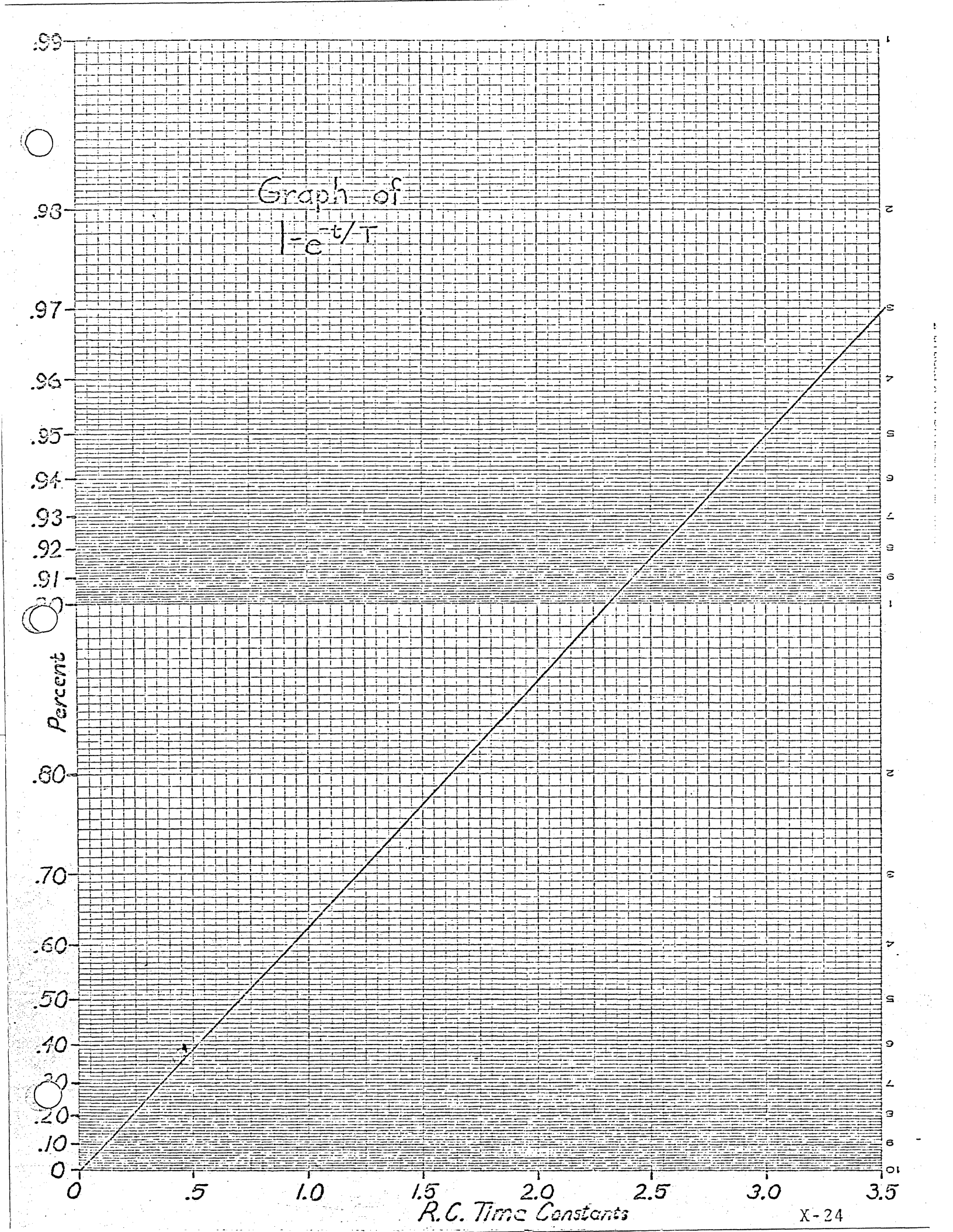
2) The gate-to-source capacitance, C_B, must be built into the circuit which will decrease yield since yield $\propto$ $\frac{1}{\text{gate area}}$

NO. 340-1510 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
5 CYCLES X 10 DIVISIONS PER INCH

EUGENE DIETZGEN CO.
MADE IN U. S. A.



X-23


Graph of
$1-e^{-t/T}$
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.93
.92
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.20
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Percent
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.5
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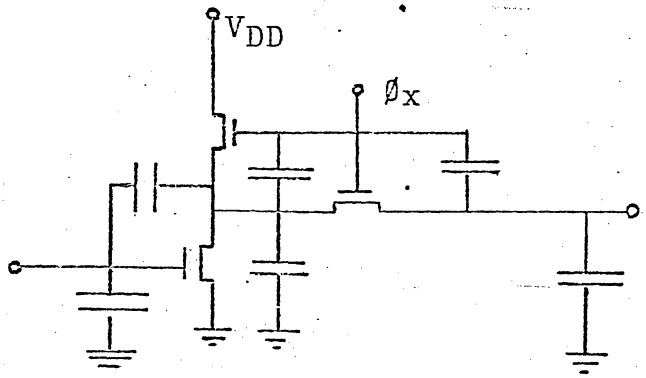
2.0
2.5
3.0
3.5
R.C. Time Constants

Multiple Phase Logic

Two phase logic, four phase logic, and shift registers are much more complex to analyze. For example the simple inverter in two phase logic includes a coupling device which is used to sample and hold logical data on the next gate. This cell has many parasitic capacitances and accurate analysis by hand is virtually impossible. Either approximate methods or computer analysis must be used.



Some effects which are present here but did not exist in the analysis of static logic must be discussed now.

In dynamic logic the signal stored on the output capacitance is sampled by successive stages after the clock has returned to ground. However, the + going edge of the clock can also degrade stored "1" levels through the parasitic capacitances C_1 and C_2.

It is therefore recommended that all dynamic circuitry be analyzed by computer.

Propagation Delay

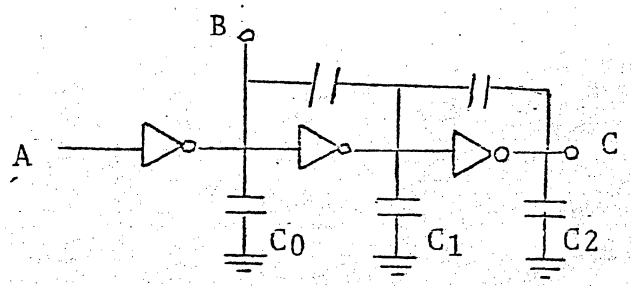
The rise and fall time of a cell output is often a design criterion when the cell provides a chip output. However, internal to the chip, the cell propagation delay is the important speed criterion.

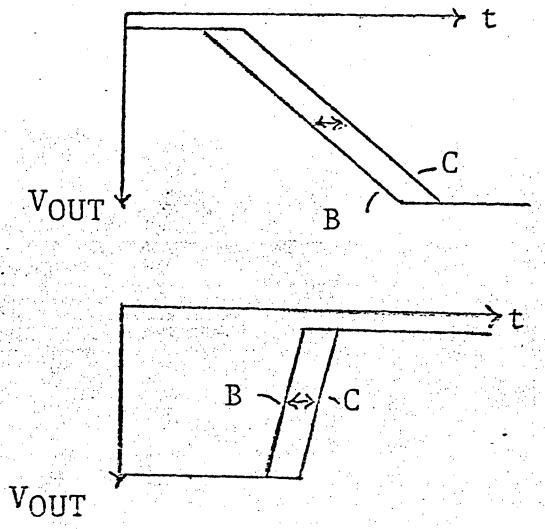
The propagation delay through a cell is different for an output transition from logical 1 to logical 0 than for the other transition.

The best way to model signal propagation is by studying pair delay (delay time between 50% point of waveforms across 2 serial inverters). This time can be computed by hand in an approach quite similar to that used for rise and fall time or modeled by computer with greater accuracy by including Miller feedback capacities. Two approaches are feasible by computer. (1) The entire system can be modeled as designed and the exact propagation delay computed, or (2) each cell can be modeled approximately by the formula:

$$T_{PD+} = t_{d+} + K_1 C_{node}$$

$$T_{PD-} = t_{d-} + K_2 C_{node}$$





The constants for this approximate model are derived in the following way. A chain of three inverters is modeled including Miller capacitances and substrate capacitances (see Sceptre). With a step transition at A the time difference between the 50% points at B and C is recorded for both logical transitions. Now capacitance C_1 is multiplied by 10 and the delay recorded again for both transitions. The equations can now be solved simultaneously for K_1, K_2 and $t_{d+} + t_{d-}$.

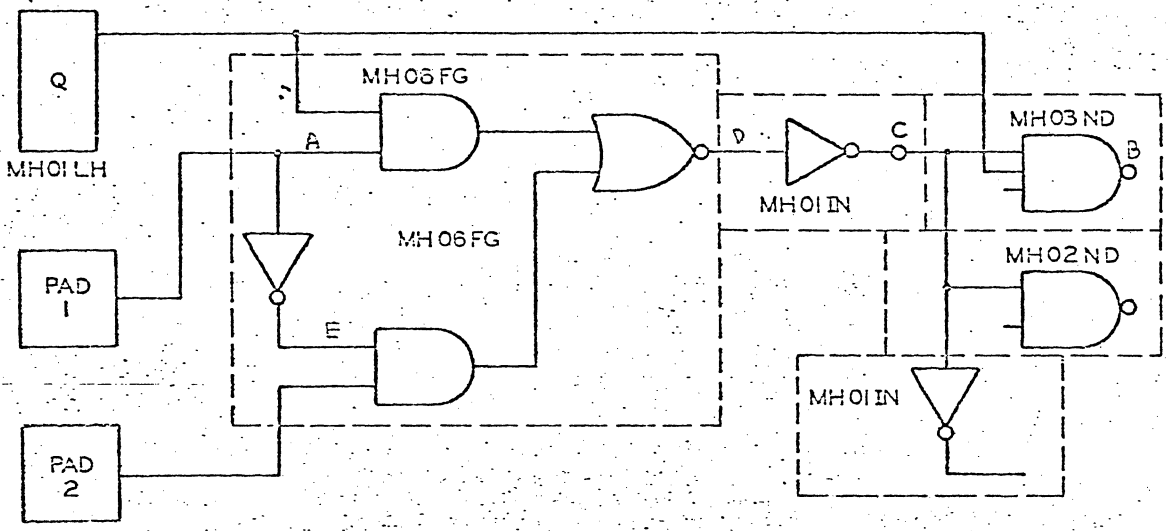
The cell is now modeled accurately enough to predict delay time for any mode of logic signal propagation (see SIMUL8).

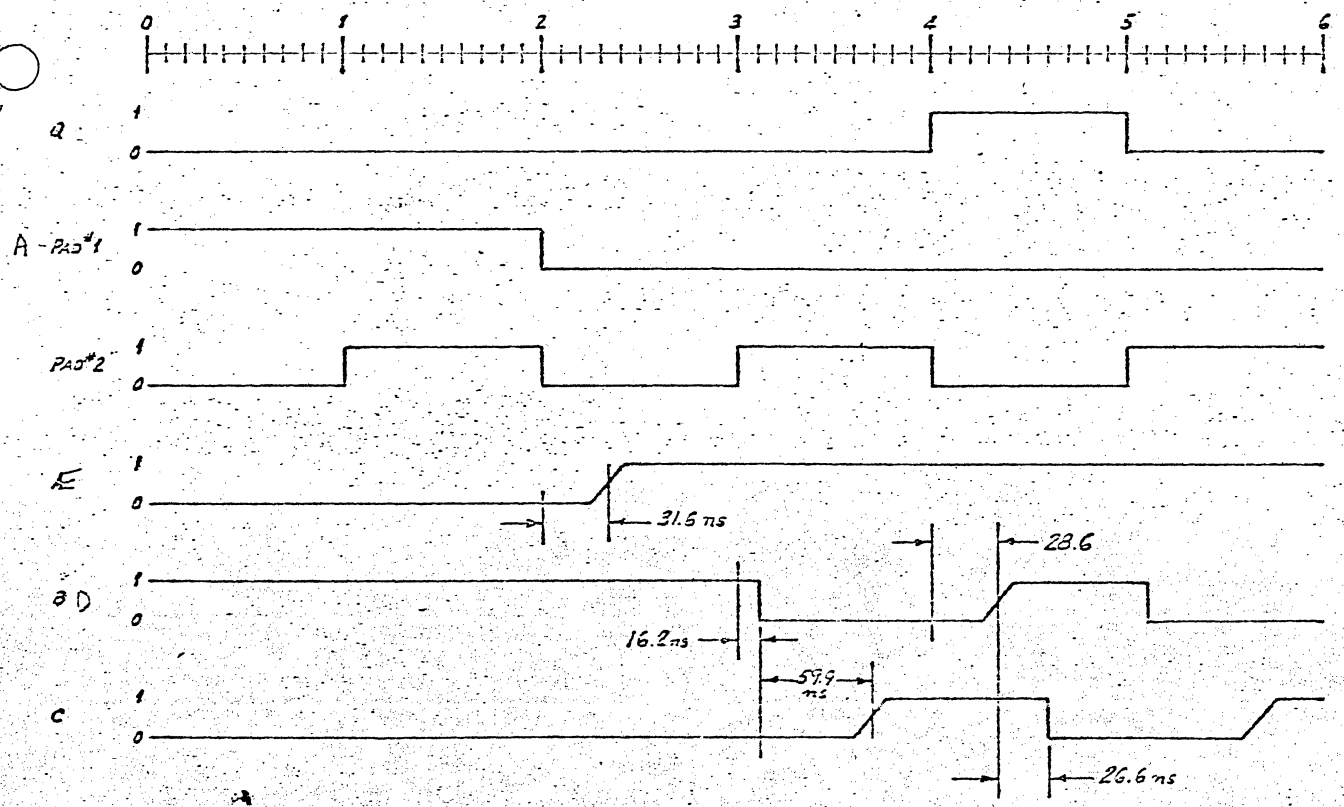
For example, the critical time path through this circuit from A to B is modeled on graph paper by computing the node capacitance at B, C, D, and E and using the derived constants to compute delay through each gate (Node capacitance =

$$\left(C_{\substack{\text{output} \\ \text{cell}}} + C_{\substack{\text{cell} \\ \text{inputs}}} + C_{\substack{\text{metal} \\ \text{interconnect}}} + C_{\substack{\text{P-diffusion} \\ \text{interconnect}}} \right).$$

See Figure 2.

FIG. 2


Q
MH01 LH
MH06FG
A
MH06FG
E
PAD 1
PAD 2
D
C
MH01IN
MH03ND
B
MH02ND
MH01IN


0
1
2
3
4
5
6
Q
A - PAD#1
PAD#2
E
31.6 ns
B D
28.6
16.2ns
59.9 ns
C
26.6 ns

CHAPTER XI

D E S I G N D O C U M E N T A T I O N

Design Documentation

Any design must be well documented to prevent design errors, to speed their correction, and to allow the product engineer to analyze low yielding circuits and to detect and correct the faulty situation.

Most of the following check list will be applicable to each product design notebook (Fig.).

Each project engineer is required to keep a notebook containing this documentation.

1. Customer's electrical specification sheets should include: _____

    1. Supplies-tolerance
    2. Operating temperature range
    3. Input-output signal levels, impedances, rise and fall times, operating frequency, interface circuitry, timing diagrams
    4. Required function description, logic diagram, or schematic.
    5. Competitor spec sheets, if available.

2. Engineer's original chip size, power, cost estimate _____

3. Full logic diagram clearly indicating positive or negative logic. _____

4. Truth table simulation of function. Customer verification of simulation. _____

5. Cellular documentation (computer listings) indicating cell design criteria and verification of criteria (all cases AC and DC analysis) - drawn device sizes. _____

6. Full schematic showing drawn device sizes. _____

7. Current and power consumption range of entire chip. Thermal Impedance evaluation. _____

8. Final chip size (including 1.5 mils for scribe grid each side) X, Y, chip area, thin oxide area. _____

9. Final cost estimate. _____

10. Design review committee comments 1, 2, 3. _____

11. Prototype run #, mapping and results. _____

CHIP SIZE ESTIMATION

SWAG based on DTL equivalent gates implemented PMOS static or 2Ø.

This approach assumes you are given the number of DTL equivalent gates which are on the average 3 input NANDS, and is a rough estimate of chip size (1 JK FF = 4 equivalent gates). Much of this logic will be reduced to functional gates in hand design; somewhat less if CAD implemented.

Good HAND Hew	CAD
1.35 equivalent gate $\Rightarrow$ 1 functional gate	1.25 equivalent gate $\Rightarrow$ 1 functional gate
4 input FG = 54 $mils^2$	4 input FG = 60 $mils^2$
ToxA = 9.9 mil^2	ToxA = 9.9 mil^2
Routing area = cell area $(.5 + .2(FO-1)^2)$	Routing area = cell area $(.5 + .5(FO-1)^2)$

Utilized area = cell area + routing area

Xu = Yu = $\sqrt{\text{utilized area}}$

24 mils must be added to each dimension for bonding pads, and scribe grid. For CAD add 6 mils to X for busslines.

X = Xu + 24	X = Xu + 30
Y = Yu + 24	Y = Yu + 24
Total Area = X • Y	Total Area = X • Y

This approach will yield an estimate within 20%. Notice that for silicon gate, or 4 phase smaller chips may be built.

ACCURATE ESTIMATION APPROACH

The following chip area estimation approach is based on knowledge of the MOS implementation in terms of CAD cells.

First list each cell used for implementation, then the number used for each. Now compute the total cell area. The routing area required is a function of the average fanout and the total number of cell contacts. This can be approximated as a function of fanout and cell area.

$$\text{Route area} \approx \text{Cell Area} * (.5 + .5(FO-1)^2)$$

Add cell area and route area for utility area. Add 24 to the utility Y dimension and 30 to the X utility dimension, to include bonding pads, busslines, and scribe grid.

Example: Fanout = 2.4

Cells Used	Area	No. Required	A
MH01JK	240	3	720
MH01IN	24	10	240
MH01PP	60	6	360
MH02PS	36	5	180
MH03PS	48	4	192
MH02SS	36	3	108
MH01FG	60	2	120
MH02FG	60	3	180
MH10FG	36	4	144
Total Cells		40	
Total Cell Area			2244
Routing Area			3320
			5564

Utility $X_u = Y_u = \sqrt{5564} = 75$

$X = 75 + 30 = 105$ $Y = 75 + 24 = 99$

Chip area = 10,400

This approach will most often lead to an estimate within 10%.

For hand designs the accuracy of the estimate depends of the designers full utilization of functional gates and the draftsman's efficiency of cell layout and wire routing. Cell area can usually be reduced 20% and routing area often 30%. So for the above design

Cell Area = 1800

Route Area = 2330

Utility Area = 4130

$X_u = Y_u$ = 64

$X = 64 + 30 = 94$

$Y = 64 + 24 = 88$

Chip Area = 8,300

Use of silicon gate cells will reduce cell area 20%. Three level routing will reduce route area approximately 30%.

CHAPTER XII

LAYOUT

LAYOUT RULES

for

STANDARD MOS PRODUCTS

Attached are the layout rules and allowable minimum geometries for standard MOS product chips. Any modification of these rules must be discussed and approved by MOS Production Engineering prior to use.

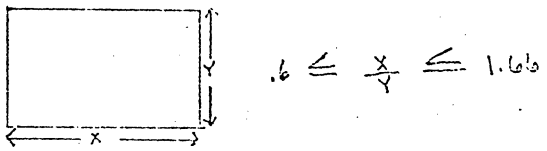
CHIP

LAYOUT RULES

Chip Layout Rules

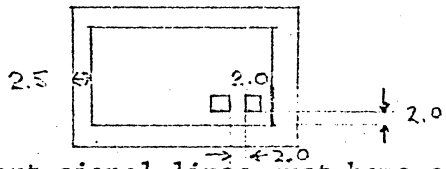
All chips, no matter what technology or cell set is used, must obey the following rules.

1. The chip aspect ratio must not exceed 1.66.

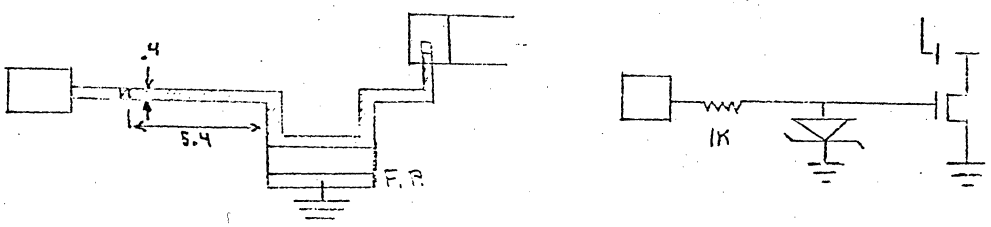


2. The bonding pads must be 2 mils from the scribe grid, 2 mils from other pads, and 2 mils from all P diffusion, or non-common metal lines. No signal lines between the bonding pads and the scribe grid.

3. The scribe grid must be 2.5 mils wide.



4. All input signal lines must have a static protection device. A resistor made of P diffusion .3 x 4.1 or .4 x 5.4 mils connected to a "Field Plate Diode" will be used.



5. The following Peripheral devices must be on each chip:
   1. MS99SW - Switch Test Device
   2. MS99FI - Field Inversion Test Device
   3. MS99LR - Load Resistor Test Device
   4. MS99TP - Optical Test Pattern
   5. MT01P - Alphameric "Top" at top of chip

6. The following Peripheral devices will be of convenience in chip layout:
   1. MS99BP - Bonding Pad
   2. Contacts:

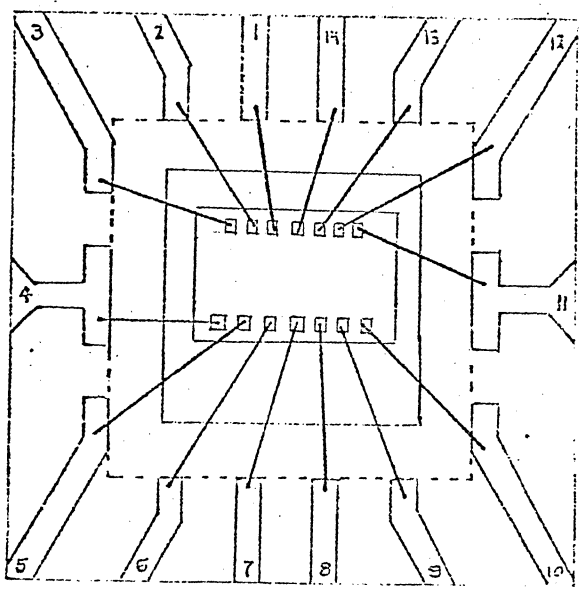
2. Contacts:

Partial coverage	a.	MS01CN	.7 x .9
	b.	MS02CN	.9 x .7
	c.	MS03CN	.8 x .8
Full metal coverage			
	d.	MS04CN	.7 x .9
	e.	MS05CN	.9 x .7
	f.	MS06CN	.8 x .8

3. MS01FP - Field Gate
4. MS06AL - Alignment Key
5. BW01 - Motorola Emblem

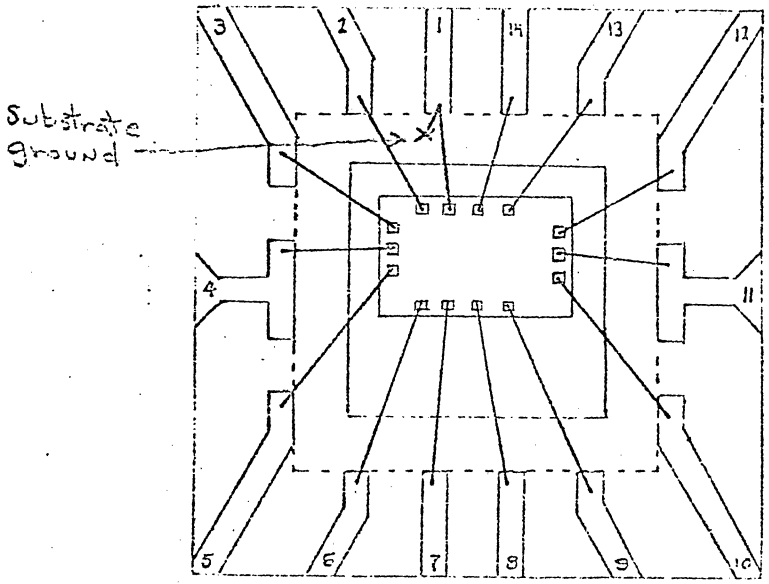
7. Bonding Pads muct be positioned around the chip so that straight line wire bonding to package posts may be used. (Fig. 5,6)
8. Substrate must be grounded by a contact from ground metal to substrate or by bonding.

Figure 5



Bad
Placement

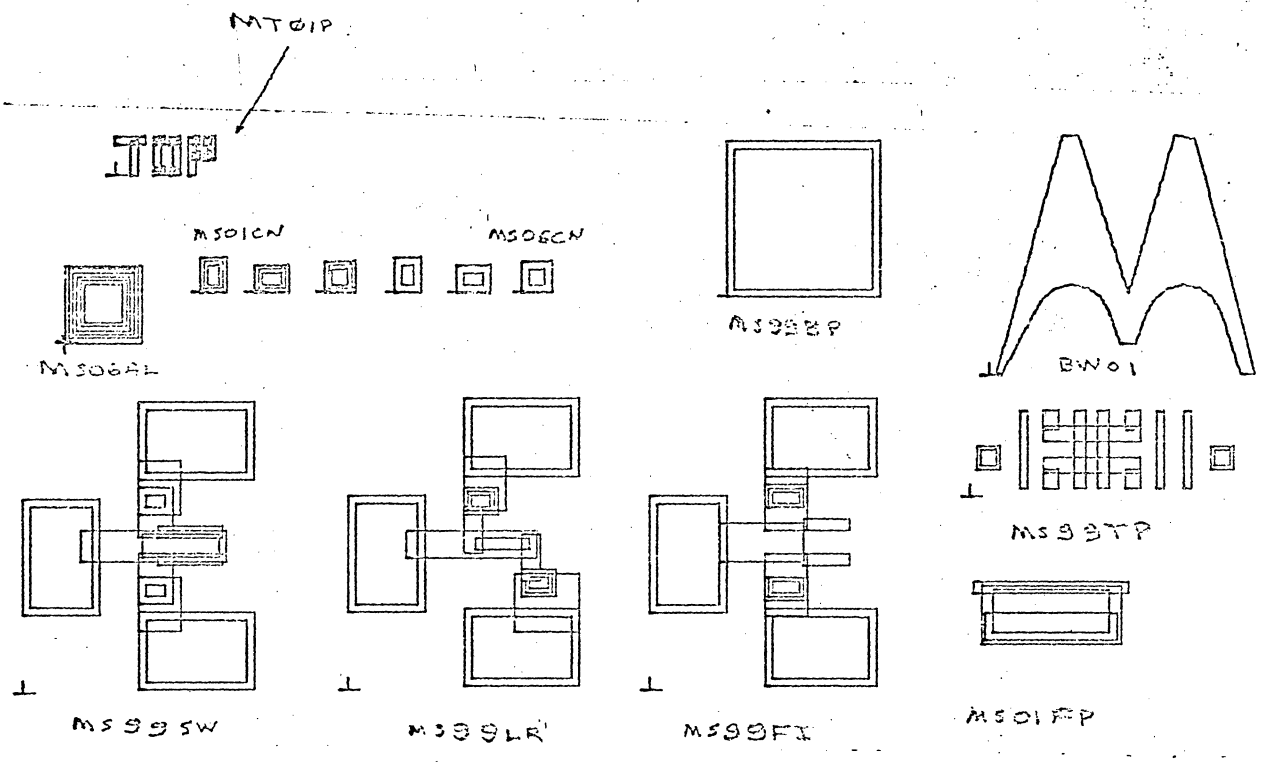
Figure 6



Good
Placement

Peripheral Devices

Function	Name	Size (mils)
Bonding Pad	MS99BP	4x4
Contacts:		
Preohmic Metal Coverage	MS01CN	.7x.9
	MS02CN	.9x.7
	MS03CN	.8x.8
Full Metal Coverage	MS04CN	.7x.9
	MS05CN	.9x.7
	MS06CN	.8x.8
Field Plate	MS01FP	1.5x3.6
	MH01FP	2.4x10
Optical Test Pattern	MS00TP	7x2.5
Alignment Key	MS06AL	2x2
Field Inversion Test Device	MS99FI	6x7.5
Switch Test Device	MS99SW	6x7.5
Load Test Device	MS99LR	6x7.5
Motorola Batwing	BW01	6.5x6.5
"Top"	MT01P	


MT01P
TOP
MS01CN
MS06CN
MS06AL
MS99BP
BW01
MS99SW
MS99LR
MS99FI
MS99TP
MS01FP

MWA53894W

NOTE

If your layout contains CAD cells designed prior to 1-15-71, do not use 0.2 mil dimensions on the gate mask.

The reason for this is that the previous layout rules provided only 0.1 mil metal overlap of the gate cut. In order to insure the metal completely covers the gate cut, we order the gate mask 0.5 mil undersize. If 0.2 mil images are present on the mask, they will be reduced to the point where the image will not satisfactorily print.

Joe Adamic

MOTOROLA Semiconductor Products Inc.

PRODUCTION SPECIFICATIONS DEPARTMENT

PRODUCTION PROCESS SPECIFICATION

PRODUCT GROUP: INTEGRATED CIRCUITS PRODUCT LINE: MOS

TITLE: MOTOROLA MOSIC LAYOUT RULES P-CHANNEL (METAL GATE) PROCESS

NO. MWA53894W

INTRODUCTION

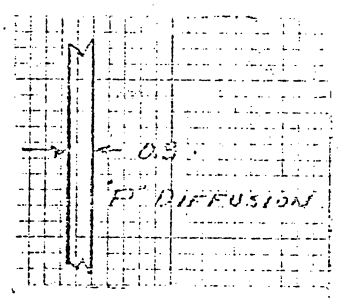
These layout rules represent acceptable artwork dimensions and spacings for the thick oxide p-channel MOSIC process from the standpoint of processability. They attempt to take into account minor errors in mask registration which originate from such sources as artwork generation and mask making. Some allowances have also been made for operator error and process variation during wafer fabrication.

The designer should make additional considerations of such factors as current carrying capacities of lines and contacts, effect of high voltages (such as voltage doubler circuit) and high substrate resistivities on "p" to "p" spacing, and possible field inversion problems when using <100> material or circuit designs which contain elements hypersensitive to leakage currents.

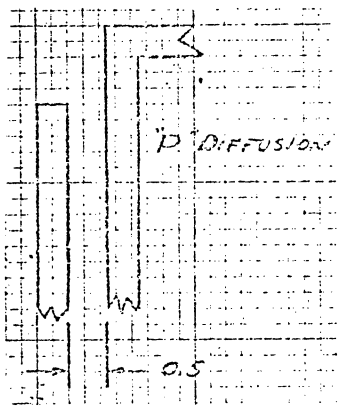
In order that circuits can be processed with a minimum delay upon receipt of masks, scale drawings of all CAD cells and circuits must be approved by process and product engineering before committing the circuits to artwork. At this time possible problem areas and exceptions should be noted.

MINIMUM ARTWORK DIMENSIONS

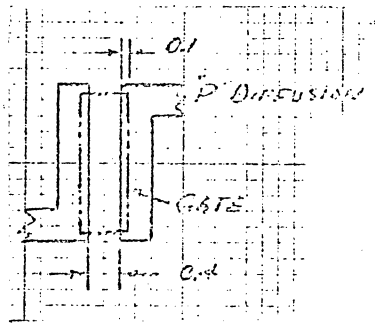
	Dimensions (Mils)		
	Min Drawn	Mask	Etched
1. SOURCE DRAIN MASK (04)			
(a) Line width	0.3		
(b) Unrelated "p" to "p" spacing	0.5		
If line to line voltage >25V	0.6		
(c) Source-drain spacing	0.4	0.39-0.45	0.37-0.4



(a)



(b)



(c)

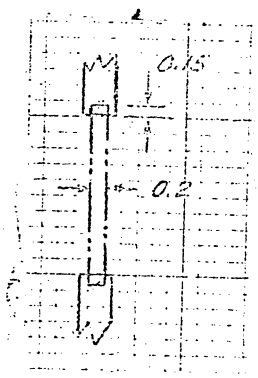
Approvals:
Process Engr. [signature] 1-11-71
Prod. Engr. [signature]
Design Engr. [signature] 1-11-71

SEE REVISION SHEET							SPECIFICATION NO MWA53894W
MEMO	DATE	ISS	MEMO	DATE	ISS	PAGE 1 OF 7 PA	

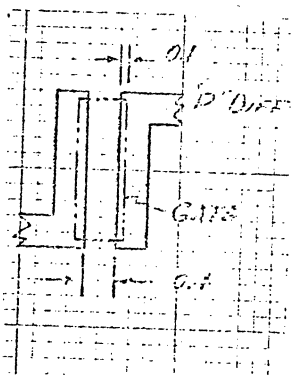
MOTOROLA FORM NO. SPD-3550

2. GATE MASK (06B)

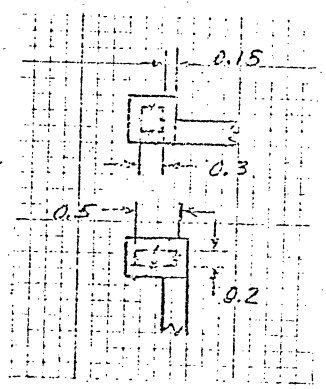
		Dimensions (Mils) Min Drawn	Mask	Etched
(a)	Gate width	0.2	0.18-0.22	0.25-0.30
	NOTE: All gate mask dimensions will etch 0.05 to 0.1 mil wider than drawn. (Drawn dimensions of 0.2 mils do not allow any tolerance for reducing image sizes during mask making or wafer processing.)	0.3 Preferred	0.27-0.33	0.34-0.40
(b)	Gate to p overlap			
	W ≤ 0.3 mil	0.15		
	W > 0.3 mil	0.10		
(c)	Gate to unrelated gate separation	0.6		
(d)	Gate to unrelated "p" separation	0.6		
(e)	Contact size	0.3 x 0.3		
	NOTE: (Drawn dimensions of 0.2 mils do not allow any tolerance for reducing image sizes during mask making or wafer processing.)	0.2 x 0.5		
(f)	Contact to "p" edge	0.15		
	If contact is made to a "p" at substrate potential	0.00		
(g)	Pre-ohmic (oversize contact) to gate spacing	0.20		



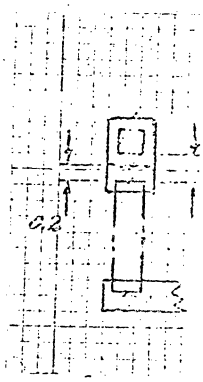
(a) & (b)



(b)

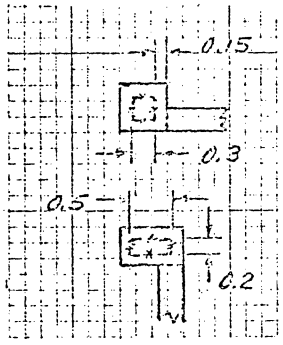


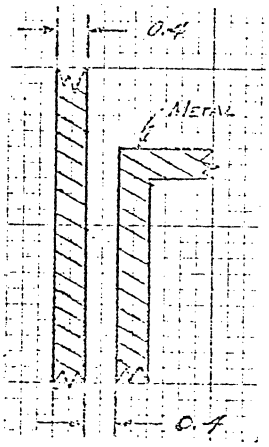
(e) & (f)



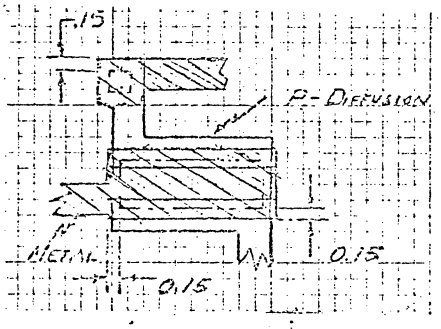
(g)

	Dimensions (Mils)		
	Min Drawn	Mask	Etched
3. PRE-OHMIC MASK (06A) (Oversized Contact)			
(a) Overlap of (06B) contact	0.15		
(b) Overlap of "p"	0.00		
4. METAL MASK (08)			
(a) Line width	0.4	0.38-0.42	0.30-0.35
If < 2 mils long	0.3		
(b) Line spacing	0.4		
(c) Min. overlap of gate mask (all cuts)	0.15		





(a & b)

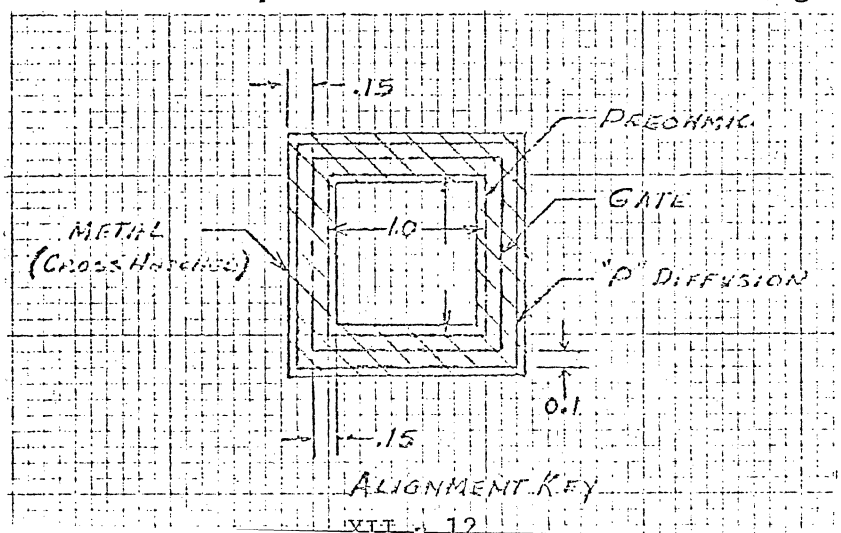


(c)

	Dimensions (Mils) Min Drawn	Mask	Etched
5. PASSIVATION MASK (09)			
(a) Passivation opening to be inside bonding pad by	0.2		
6. BONDING PADS			
(a) Size	5 x 5		
(b) Spacing from pad to pad Preferred	4.0 6.0		
(c) Spacing from pad to non-common diffusion	1.0		
(d) Spacing from pad to non-common metal	2.0		
7. CHIP PERIPHERY			
(a) Scribe Grid Width	3.0		
(b) Distance from oxide to center of scribe grid	1.5		
(c) Additional allowance in scribe grid width for stepping overlap on Gerber artwork	1.0		
(d) Spacing from edge of scribe grid to active circuit areas.	2.0		

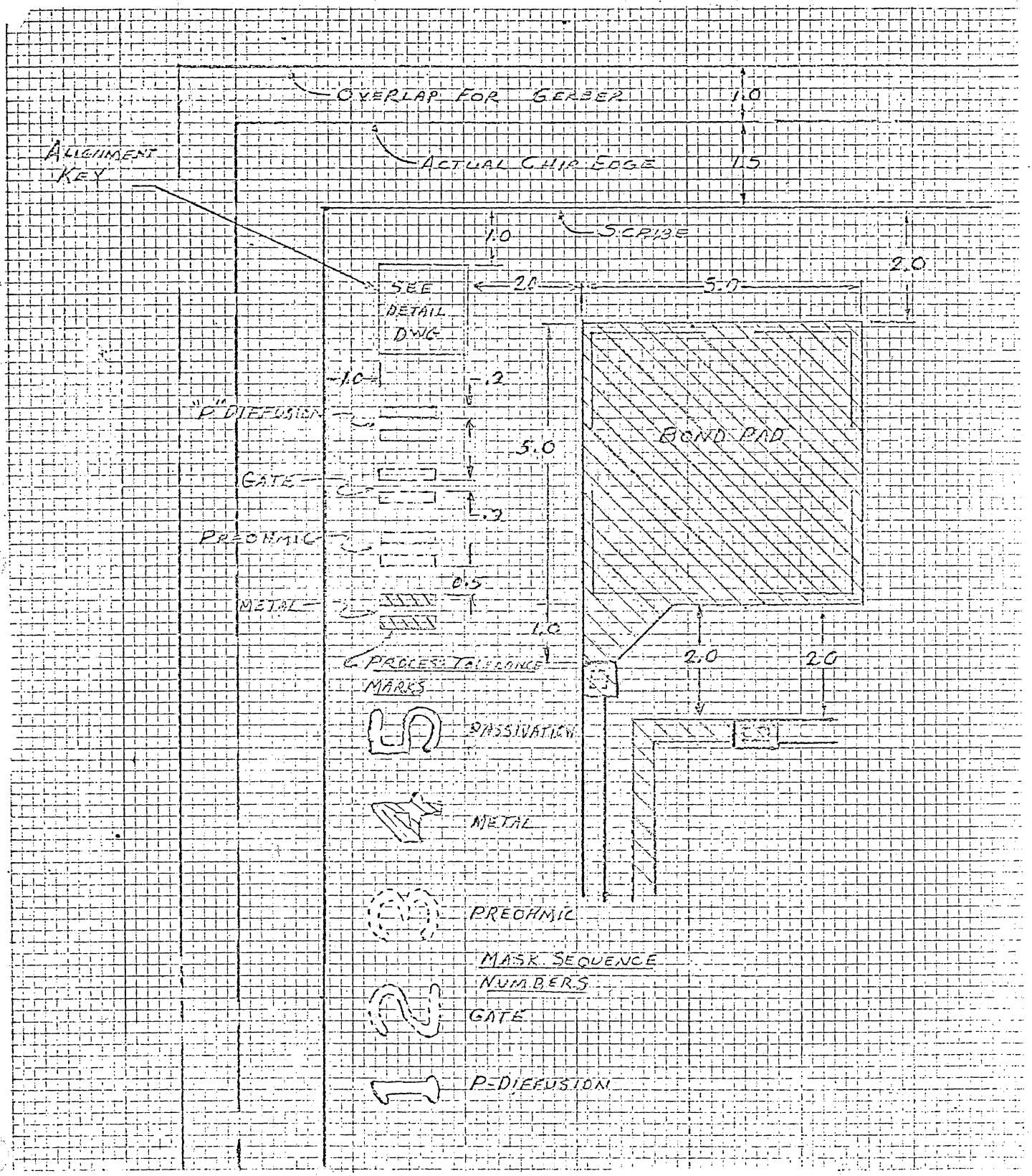
8. ALIGNMENT KEYS

Alignment keys shall be placed in all four corners of the chip. This allows quick assessment of mask alignment accuracy.



MS07AL

CHIP PERIPHERY

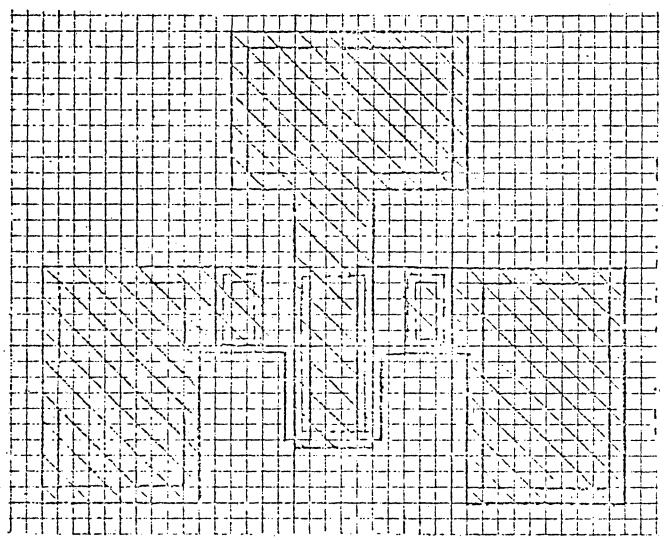


9. PROCESS TOLERANCE MARKS

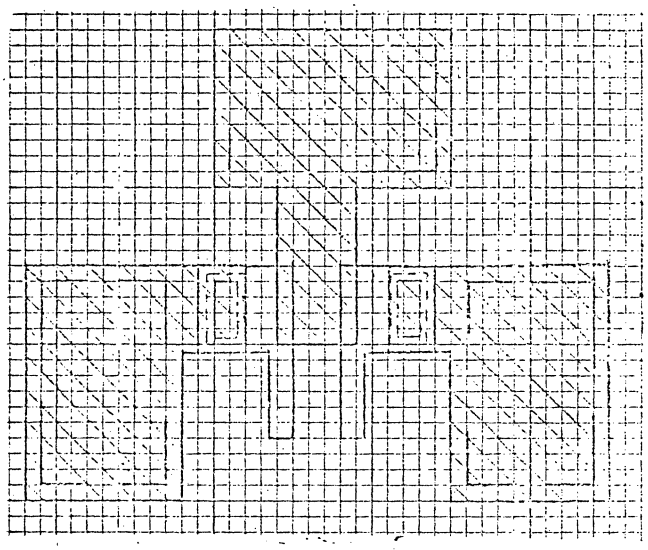
Process tolerance marks are to be placed near one corner of the chip. This is to provide a qualitative check whether design dimensions are being held.

10. TEST DEVICES (If space permits)

Test devices are placed on the periphery of each chip to determine threshold voltage and field inversion. These devices should be as follows:



MS99SW



MS99FI

11. MASK SEQUENCE NUMBER (If space permits)

Each mask layer shall have a number showing the mask sequence in which it should be applied.

Source-Drain	-	1
Gate	-	2
Preohmic	-	3
Metal	-	4
Passivation	-	5

The numbers should be placed next to each other on the periphery of the chip as shown on page 5. The number 1 is cut with the "p" diffusion the 2 with the gate and so on.

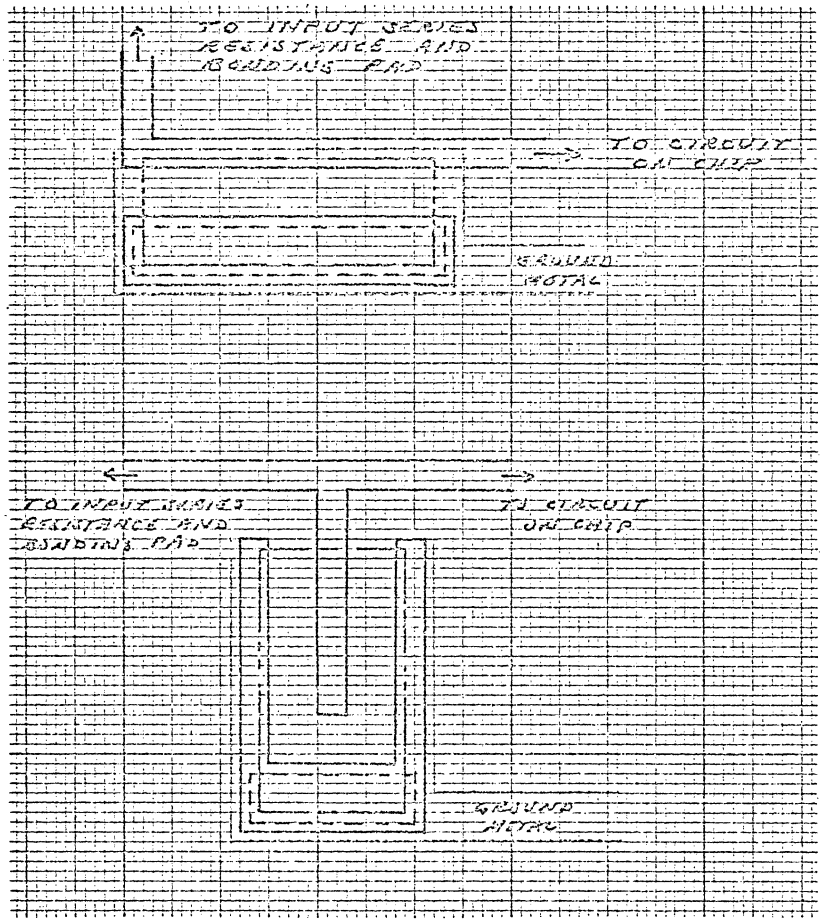
12. CIRCUIT ID NUMBER (If space permits)

Each circuit has a unique Motorola number. This number should be cut into each layer coincident with the previous layer or that layer which is not common to other circuits. (i.e. ROMS have all masks in common except the gate.) If the Motorola number is determined by electrical sorting it should not be cut into each chip since the masking operation does not solely determine the part number.

Field plate diodes. The field plate diode protective device is required on all input which are connected to a device gate. For signal inputs with a short time constant, up to 1000 Ω of resistance should be included to delay transients and allow time for protective breakdown to occur. For clock inputs and supply (V_{GG}) inputs involving long time constants or high current drain, input series resistance should be decreased or eliminated as necessary for specified performance.

The field plate diode is a physical MOS device with its gate and source grounded, and its drain tied to the signal to be protected. The device width should be a minimum of 3.0 mil, and may be interdigitated. For determining input series resistance, nominal value of 75 Ω/sq. for the thick oxide process should be used.

Examples of protective devices are shown below.



Mask Inspections

The chip designer is responsible for a number of mask checks, as follows:

a. A blueprint of each mask must be dimensioned to aid in mask measurements and to ensure that critical dimensions are held. The SPD mask shop prefers to designate additional areas to be measured, and a blueprint will be marked by them for the dimensions they wish specified. For the Mesa mask shop, the designer should designate the images to be measured. Specifically, the 6B (GT) mask should include a minimum width gate, and the 04 (PD) mask should include a minimum P-P wide device spacing dimension. A copy of the dimensioned blueprint must be provided the MOS processing group to aid them in checking the mask dimensions.

b. Working plates must be inspected by the designer for such things as:

(1) correct image (not mirror-image)

(2) test patterns

(3) correct mask numbering

(4) stepped in defects.

The MOS processing group will inspect the masks for defect density and check critical dimensions. The MOS processing group will run a stack set for their files, which will be available to the designer upon request.

A. Mask Numbering System

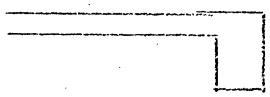
Mask	05	N+ Diffusion (if used)	(DN)
	04	P Diffusion	(PD)
	06B	Gate	(GT)
	06A	Pre-ohmic	(PI)
	08	Metal	(MI)
	09	Passivation	(VI)

Mask options are usually lettered, i.e., two metal mask options would be designated 08A and 08B. Revisions would normally be indicated by a dash number, i.e., 08A-1 is a revised version of metal mask 08A.

B. Identification of patterns on composite drawings.

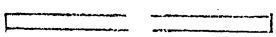
P Diffusion:

Solid Line



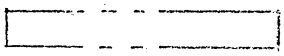
N+ Diffusion:

Broken Line



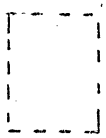
Gates

Broken Line



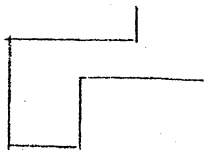
Pre-ohmic

Dashed Line



Metal:

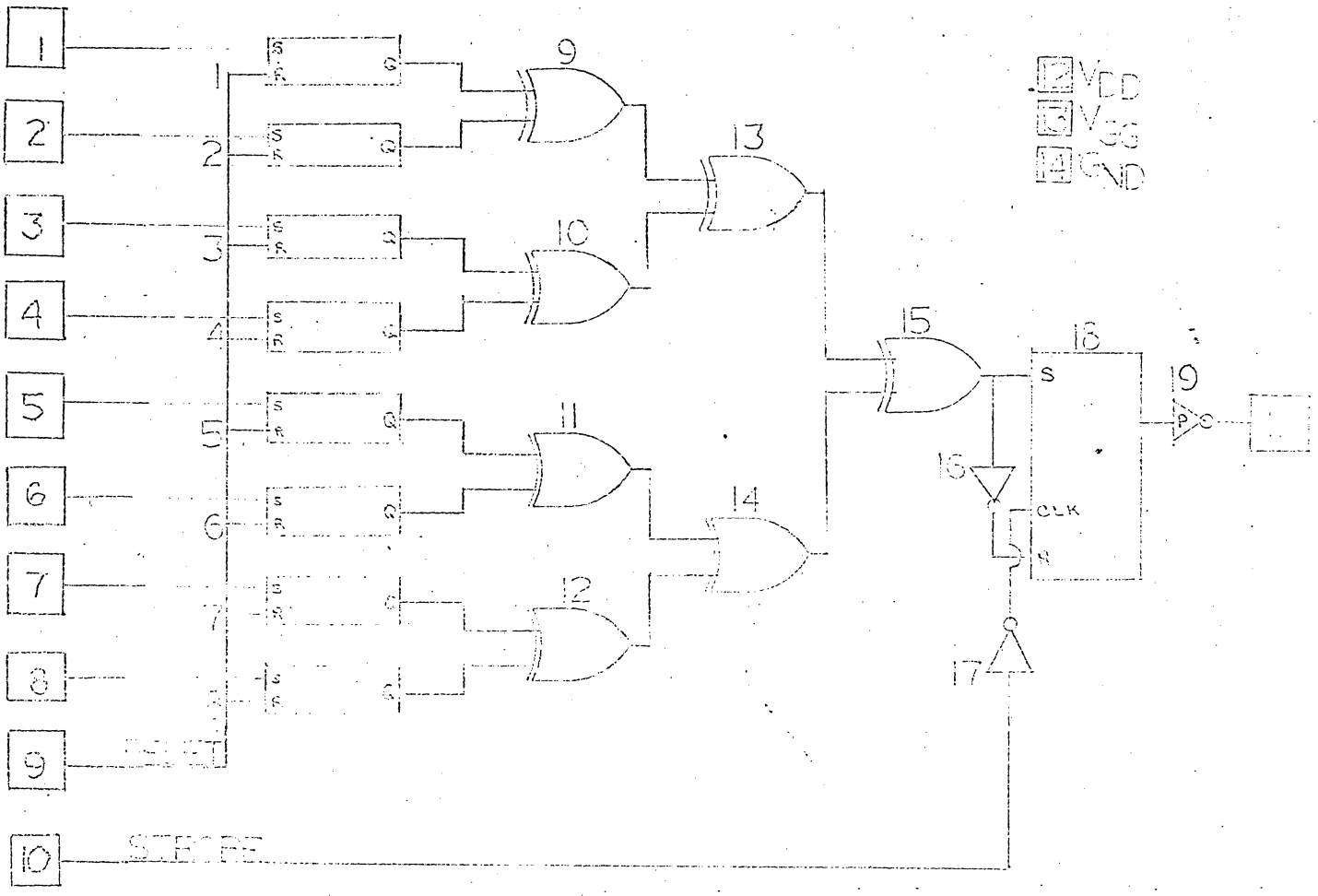
Metal pattern is a solid line on a separate drawing.



TYPICAL DESIGN

Typical Design

This is an example layout of an 8 bit parity checker, implemented with the high threshold DC Logic cell set.



The cells chosen to be implemented as follows:

MH01IH - 1,2,3,4,5,6,7,8

MH01EO - 9,10,11,12,13,14,15

MH01IN - 16,17

MH01CL - 18

MH01PP - 19

MH01FP - 10 required

Computer aided simulation predicts that R information at logic block #18 is valid 240 ns maximum after the last data in. Since strobe appears 1us after valid data there is plenty of time margin.

The computer also predicts a typical power of 80 mw, well under package thermal limitation. 14 terminals allowable die size is 130 x 160 mils.

Now using paper dolls or computer simulation the layout begins.

The pads must be placed as shown in Fig. 2. The length of all cells placed in one row is computed:

8 x 3.6	MH01LH
+10 x 2.4	MH01FP
+7 x 6.0	MH01EO
+2 x 2.4	MH01IN
+1 x 6.0	MH01CL
+1 x 6.0	MH01PP
111.6	

This row would be 111.6 x 10, obviously a poor design. However, we fold the row in half making it approximately 56 x 20. Now use 20 x 56 mils for metal and P diffusion interconnect for a 1.4 aspect ratio.

Next we determine the order of the cells for optimum routing interconnect ability. This can be done with computer aids by on diagonal algorithm, or by eyeball for relatively simple circuits as in Fig. 6.

The on diagonal method is as follows:

The cell numbers of the elements are listed at the top of a matrix representing output node connections. The cell numbers

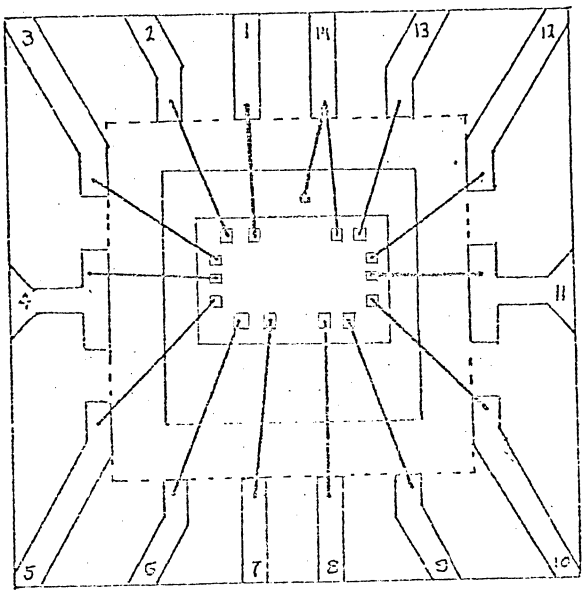


FIG. 2

in the same order along the side of the matrix represent input nodes. Since no cell may connect to itself there are no asterisks on the diagonal. A cell is optimally placed if it connects to its neighbors and therefore the asterisks should be as close as possible to the diagonal. Shifting the placement order will move them closer to or farther from the diagonal. (See Fig. 3&4) Another aid to optimum placement is the number of signal wires passing the input-output terminal of a cell.

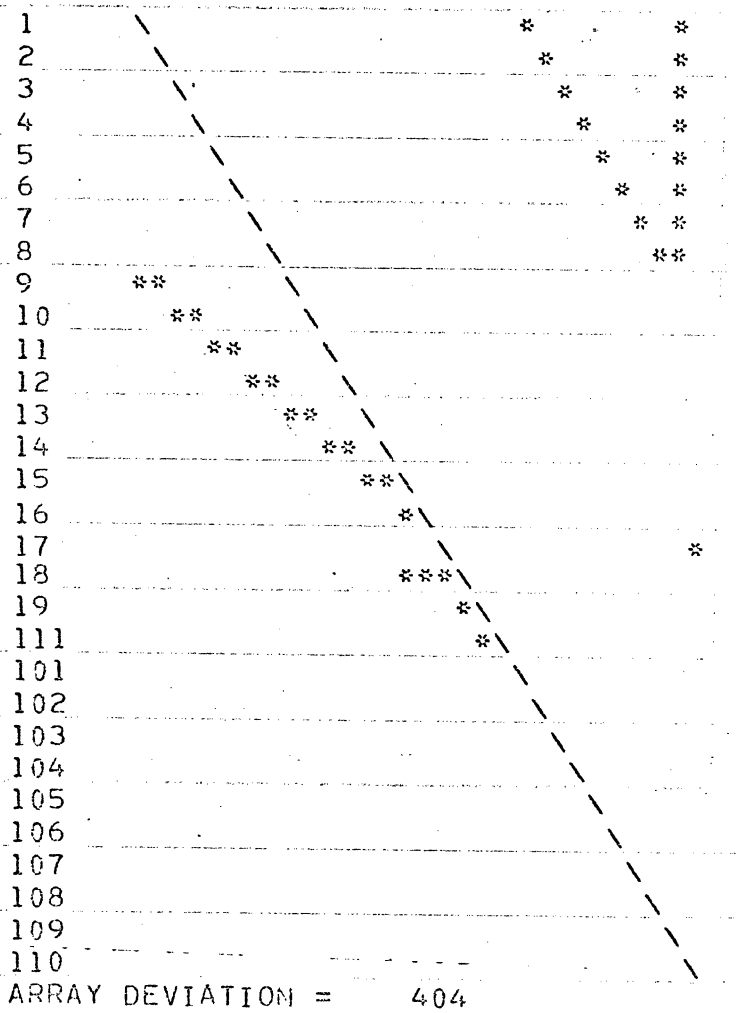
The wire thickness algorithm ignores input-output bonding pads, and considers only the wires from cell to cell. Fig.4 shows the placement forces a maximum of only four wires running parallel, and a minimum of one. The thickness is relatively constant -- another characteristic of good placement.

07/15/70 TITLE FOR BRUCE FETTE

GATE NAME	CELL NAME	PAD NAME	PAD TYPE	LEAD DENSITY
1	MH01LH	S	1	1*
1	MH01LH	R	1	2**
1	MH01LH		2	3***
2	MH01LH	S	1	4****
2	MH01LH	R	1	4****
2	MH01LH		2	5*****
3	MH01LH	S	1	6******
3	MH01LH	R	1	6******
3	MH01LH		2	7*******
4	MH01LH	S	1	8********
4	MH01LH	R	1	8********
4	MH01LH		2	9*********
5	MH01LH	S	1	10**********
5	MH01LH	R	1	10**********
5	MH01LH		2	11***********
6	MH01LH	S	1	12************
6	MH01LH	R	1	12************
6	MH01LH		2	13*************
7	MH01LH	S	1	14**************
7	MH01LH	R	1	14**************
7	MH01LH		2	15***************
8	MH01LH	S	1	16****************
8	MH01LH	R	1	16****************
8	MH01LH		2	17*****************
9	MH01EO		1	17*****************
9	MH01EO		1	16****************
9	MH01EO		3	15***************
9	MH01EO		3	15***************
9	MH01EO		2	16****************
10	MH01EO		1	16****************
10	MH01EO		1	15***************
10	MH01EO		3	14**************
10	MH01EO		3	14**************
10	MH01EO		2	15***************
11	MH01EO		1	15***************
11	MH01EO		1	14**************
11	MH01EO		3	13*************
11	MH01EO		3	13*************
11	MH01EO		2	14**************
12	MH01EO		1	14**************
12	MH01EO		1	13*************
12	MH01EO		3	12************
12	MH01EO		3	12************
12	MH01EO		2	13*************
13	MH01EO		1	13*************
13	MH01EO		1	12************
13	MH01EO		3	11***********
13	MH01EO		3	11***********
13	MH01EO		2	12************
14	MH01EO		1	12************
14	MH01EO		1	11***********
14	MH01EO		3	10**********
14	MH01EO		3	10**********
14	MH01EO		2	11***********
15	MH01EO		1	11***********
15	MH01EO		1	10**********
15	MH01EO		3	9*********
15	MH01EO		3	9*********
15	MH01EO		2	10**********
16	MH01IN		1	10**********
16	MH01IN		2	11***********
17	MH01IN		1	12************
17	MH01IN		2	13*************
18	MH01CL	S	1	13*************
18	MH01CL	CL	1	12************
18	MH01CL	R	1	11***********
18	MH01CL		3	10**********
18	MH01CL		2	11***********
19	MH01PP		1	11***********
19	MH01PP		3	10**********
19	MH01PP		3	10**********
19	MH01PP		2	11***********
19	MH01PP		3	11***********
111	MP01AD		3	11***********
111	MP01AD		3	11***********
111	MP01AD		1	11***********
111	MP01AD		3	10**********
111	MP01AD		3	10**********
101	MP01AD		3	10**********
101	MP01AD		3	10**********
101	MP01AD		2	10**********
101	MP01AD		3	9*********
101	MP01AD		3	9*********
102	MP01AD		3	9*********
102	MP01AD		3	9*********
102	MP01AD		2	9*********
102	MP01AD		3	8********
102	MP01AD		3	8********
103	MP01AD		3	8********
103	MP01AD		3	8********
103	MP01AD		2	8********
103	MP01AD		3	7*******
103	MP01AD		3	7*******
104	MP01AD		3	7*******
104	MP01AD		3	7*******
104	MP01AD		2	7*******
104	MP01AD		3	6******
104	MP01AD		3	6******
105	MP01AD		3	6******
105	MP01AD		3	6******
105	MP01AD		2	6******
105	MP01AD		3	5*****
105	MP01AD		3	5*****
106	MP01AD		3	5*****
106	MP01AD		3	5*****
106	MP01AD		2	5*****
106	MP01AD		3	4****
106	MP01AD		3	4****
107	MP01AD		3	4****
107	MP01AD		3	4****
107	MP01AD		2	4****
107	MP01AD		3	3***
107	MP01AD		3	3***
108	MP01AD		3	3***
108	MP01AD		3	3***
108	MP01AD		2	3***
108	MP01AD		3	2**
108	MP01AD		3	2**
109	MP01AD		3	2**
109	MP01AD		3	2**
109	MP01AD		2	2**
109	MP01AD		3	1*
109	MP01AD		3	1*
110	MP01AD		3	1*

Bad Placement

07/15/70 TITLE FOR BRUCE FETTE

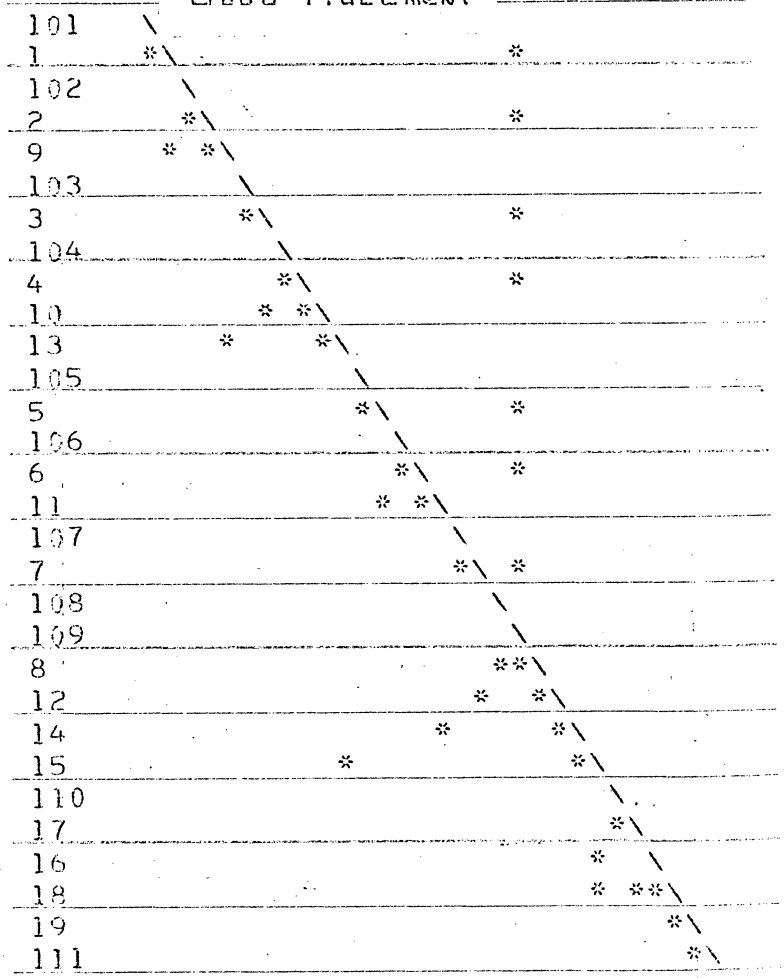


ARRAY DEVIATION = 404

GATE NAME	CELL NAME	PAD NAME	PAD TYPE	LEAD DENSITY
101	MP01AD		3	0
101	MP01AD		3	0
101	MP01AD		2	1*
101	MP01AD		3	1*
101	MP01AD		3	1*
1	MH01LH	S	1	1*
1	MH01LH	R	1	1*
1	MH01LH		2	2**
102	MP01AD		3	2**
102	MP01AD		3	2**
102	MP01AD		2	3***
102	MP01AD		3	3***
102	MP01AD		3	3***
2	MH01LH	S	1	3***
2	MH01LH	R	1	2**
2	MH01LH		2	3***
9	MH01EO		1	3***
9	MH01EO		1	2**
9	MH01EO		3	1*
9	MH01EO		3	1*
9	MH01EO		2	2**
103	MP01AD		3	2**
103	MP01AD		3	2**
103	MP01AD		2	3***
103	MP01AD		3	3***
103	MP01AD		3	3***
3	MH01LH	S	1	3***
3	MH01LH	R	1	2**
3	MH01LH		2	3***
104	MP01AD		3	3***
104	MP01AD		3	3***
104	MP01AD		2	4****
104	MP01AD		3	4****
104	MP01AD		3	4****
4	MH01LH	S	1	4****
4	MH01LH	R	1	3***
4	MH01LH		2	4****
10	MH01EO		1	4****
10	MH01EO		1	3***
10	MH01EO		3	2**
10	MH01EO		3	2**
10	MH01EO		2	3***
13	MH01EO		1	3***
13	MH01EO		1	2**
13	MH01EO		3	1*
13	MH01EO		3	1*
13	MH01EO		2	2**
105	MP01AD		3	2**
105	MP01AD		3	2**
105	MP01AD		2	3***
105	MP01AD		3	3***
105	MP01AD		3	3***
5	MH01LH	S	1	3***
5	MH01LH	R	1	2**
5	MH01LH		2	3***
106	MP01AD		3	3***
106	MP01AD		3	3***
106	MP01AD		2	4****
106	MP01AD		3	4****
106	MP01AD		3	4****
6	MH01LH	S	1	4****
6	MH01LH	R	1	3***
6	MH01LH		2	4****
11	MH01EO		1	4****
11	MH01EO		1	3***
11	MH01EO		3	2**
11	MH01EO		3	2**
11	MH01EO		2	3***
107	MP01AD		3	3***
107	MP01AD		3	3***
107	MP01AD		2	4****
107	MP01AD		3	4****
107	MP01AD		3	4****
7	MH01LH	S	1	4****
7	MH01LH	R	1	3***
7	MH01LH		2	4****
108	MP01AD		3	4****
108	MP01AD		3	4****
108	MP01AD		2	5*****
108	MP01AD		3	5*****
108	MP01AD		3	5*****
109	MP01AD		3	5*****
109	MP01AD		3	5*****
109	MP01AD		2	5*****
109	MP01AD		3	5*****
109	MP01AD		3	5*****
8	MH01LH	S	1	5*****
8	MH01LH	R	1	4****
8	MH01LH		2	4****
12	MH01EO		1	4****
12	MH01EO		1	3***
12	MH01EO		3	2**
12	MH01EO		3	2**
12	MH01EO		2	3***
14	MH01EO		1	3***
14	MH01EO		1	2**
14	MH01EO		3	1*
14	MH01EO		3	1*
14	MH01EO		2	2**
15	MH01EO		1	2**
15	MH01EO		1	1*
15	MH01EO		3	0
15	MH01EO		3	0
15	MH01EO		2	1*
110	MP01AD		3	1*
110	MP01AD		3	1*
110	MP01AD		2	2**
110	MP01AD		3	2**
110	MP01AD		3	2**
17	MH01IN		1	2**
17	MH01IN		2	2**
16	MH01IN		1	2**
16	MH01IN		2	3***
18	MH01CL	S	1	3***
18	MH01CL	CL	1	2**
18	MH01CL	R	1	1*
18	MH01CL		3	0
18	MH01CL		2	1*
19	MH01PP		1	1*
19	MH01PP		3	0
19	MH01PP		3	0
19	MH01PP		2	1*
19	MH01PP		3	1*
111	MP01AD		3	1*
111	MP01AD		3	1*

```
101 (MP01AD).
  1 (MH01LH) = S:101; R: 109.
102 (MP01AD).
  2 (MH01LH) = S:102; R:109.
  9 (MH01EO) = 1,2.
103 (MP01AD).
  3 (MH01LH) = S:103; R:109.
104 (MP01AD).
  4 (MH01LH) = S:104; R:109.
 10 (MH01EO) = 3,4.
 13 (MH01EO) = 9,10.
105 (MP01AD).
  5 (MH01LH) = S:105; R:109.
106 (MP01AD).
  6 (MH01LH) = S:106; R:109.
 11 (MH01EO) = 5,6.
107 (MP01AD).
  7 (MH01LH) = S:107;R:109.
108 (MP01AD).
109 (MP01AD).
  8 (MH01LH) = S:108;R:109.
 12 (MH01EO) = 7,8.
 14 (MH01EO) = 11,12.
 15 (MH01EO) = 13,14.
110 (MP01AD).
 17 (MH01IN) = 110.
 16 (MH01IN) = 15.
 18 (MH01CL) = R:16; CL:17; S:15.
 19 (MH01PP) = 18.
111 (MP01AD) = 19.
END
```

Good Placement



ARRAY DEVIATION = 104

The above placement algorithms are also implemented in Motorola's CAD facility and logic diagram data is entered by "Magic" deck punched cards. This card deck specifies all interconnections and all cells used in a circuit design to all the available CAD software.

A third cell placement algorithm, also implemented in software, places all cells without iteration. The program first sorts all devices into a linear string minimizing horizontal interconnect length. It then folds the string. The rows are then resorted individually to aline interconnecting cells and bonding pads vertically to again minimize line length.

Two methods of row design may be applied to the linear sortment of cells: fold and mix. The fold method overlaps buss lines and forces the routing area to the chip periphery. Connections from Row A to Row B must be around the end. The mix method overlaps the routing areas allowing easier connections between rows and more efficient use of the routing area. However, it is significantly more difficult to analyze the interconnect routing by computer.

Fig.6 and Fig.7 are examples of these chip layout algorithms generated either by computer or by a draftsman using 100x paper replicas of the cell outlines.

Chip design is verified by the chip design check list.

Fig. 6. EXAMPLE OF FOLDED LINEAR STRING

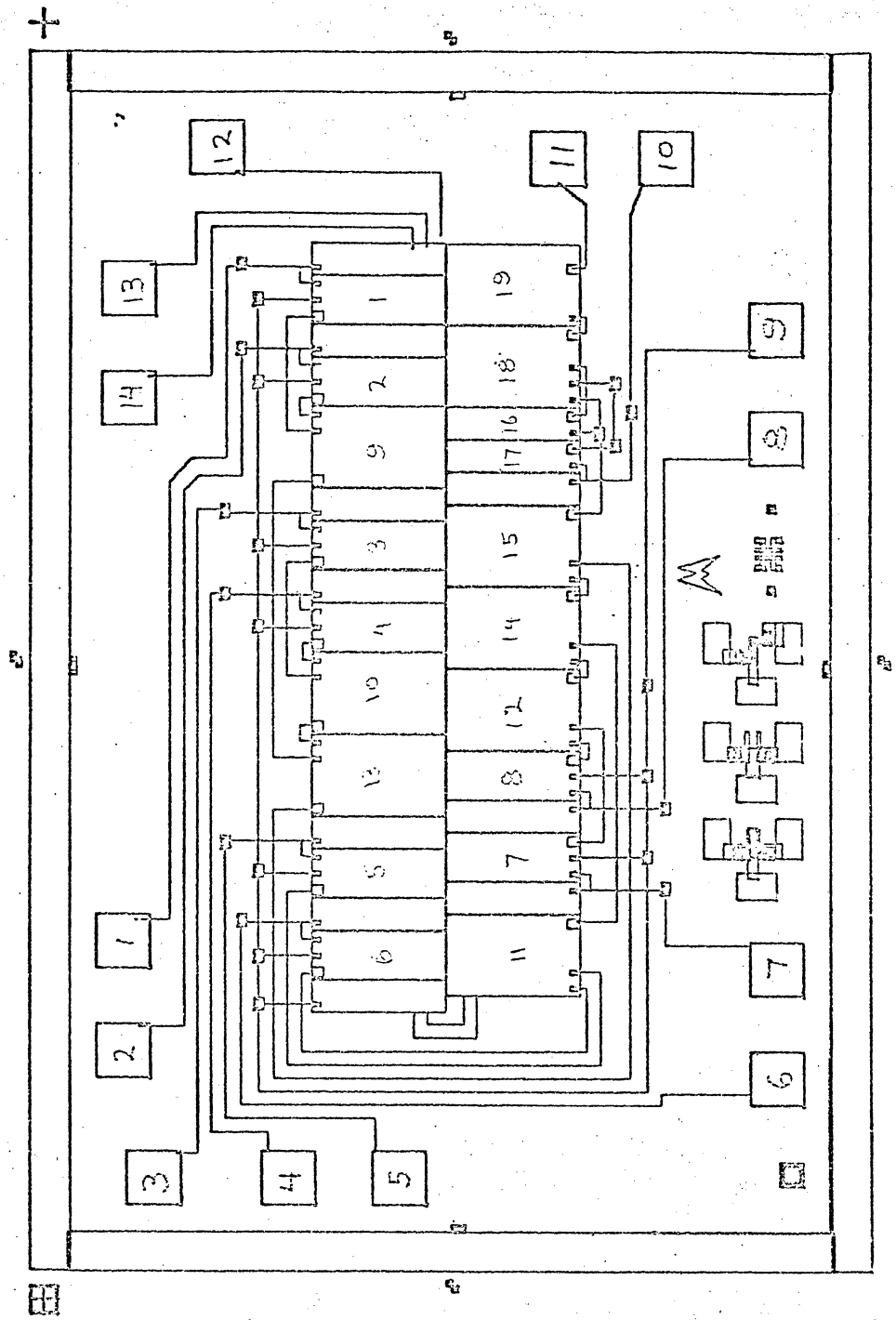
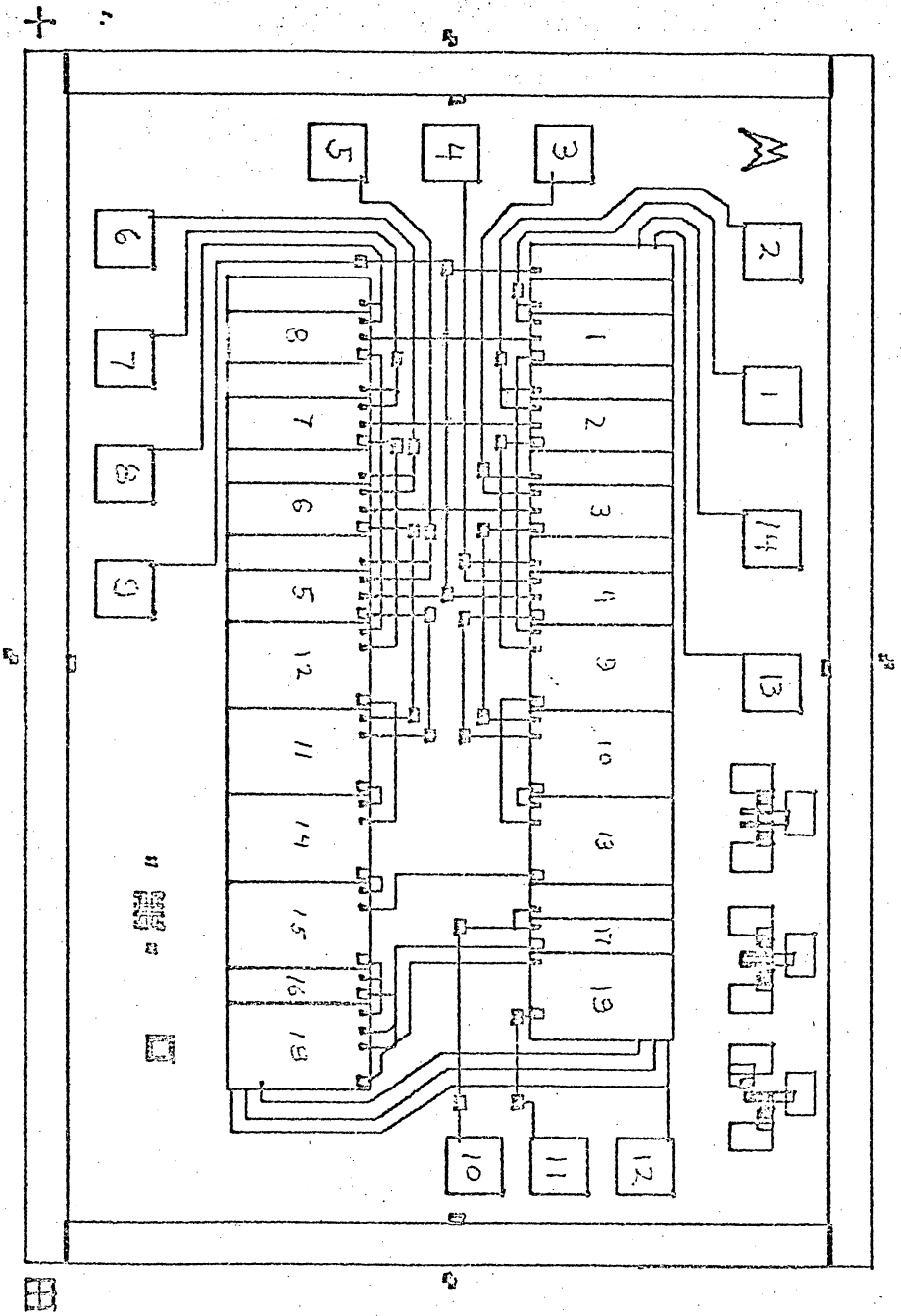


Fig.7 EXAMPLE OF MIXED INTERCONNECT



Chip Design Check List

1. System partitioned into chips _____
2. Cell choice _____
3. Logic reduction _____
4. Magic deck _____
5. Logic simulation, verification _____
6. Cell placement optimization _____
7. Fold or mix cell placement _____
8. Routing optimization _____
9. No violations: Cell layout rules _____
10. No violations: Chip layout rules _____
11. Timing simulation _____
12. Test sequence generation _____
13. 100X master artwork _____
14. Step and reduce artwork _____
15. Prototype parts test _____
16. Rework (if necessary) _____
17. Production! _____

MOS Parasitics

Several Phenomenon frequently occur which result in designs which function improperly. The layout draftsman and engineer should design to avoid these and each should be considered in the design review.

Field Inversion

Field Inversion is the MOS device Phenomenon occuring where it was not intended. It occurs whereever a metal line crosses two P diffusions. Using the MOS device model the same equations apply for $V_{T\phi}$ and BETA,

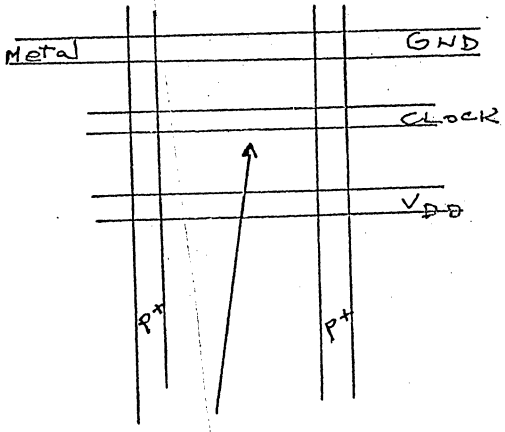
$$V_{T\phi} = V_{fB} + 2\phi_{fp} + \frac{\sqrt{2K_S \epsilon_0 9 N_A \left| 24_{fp} \right|}}{C_0}$$

$$BETA = \frac{\mu \epsilon_{ox}}{t_{ox}}$$

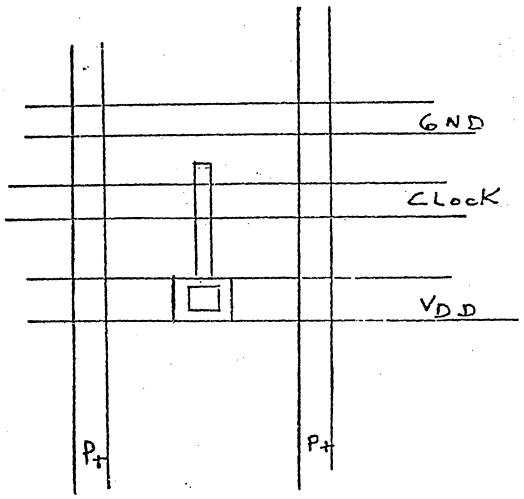
except that $V_{T\phi}$ is much higher and BETA is much lower.

Field Inversion	High Threshold	Low Threshold	Silicon Gate	
BETA				$\mu a/V^2$
$V_{T\phi}$				Volts

There are two methods to avoid problems with field inversion. For High or Low threshold field inversions from signal to signal, or signal to ground can, instead, be returned to V_{DD} by inserting a P diffusion between the two affected P diffusions which returns to V_{DD}.



Probable Field Inversion



Fixed

This works when a field inversion to ground is degrading a high impedance "1" level. The field inversion now enhances the "1" level, but doesn't significantly degrade the low impedance "0" level. This is particularly important in the vicinity of bootstrap circuits.

The second method comes in two forms applicable to the low threshold process. First - N plus channel stoppers significantly increase the field inversion threshold and can be placed between P diffusions under the metal. The second method is a Motorola confidential process in which all thick oxide regions are doped to a higher field inversion by donor deposition.

P to Substrate Leakage

P to substrate leakage causes the time degradation of logical voltages stored on MOS capacitive nodes. This therefore determines the lower frequency limit of dynamic circuits such as the dynamic shift register, and 2 phase logic. The equation for junction leakage is:

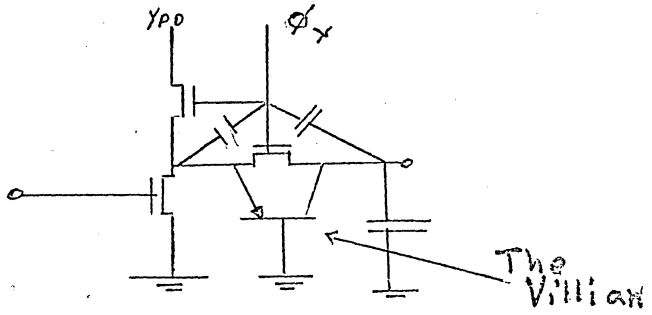
$$I = I_R \left(e^{\frac{qV}{K_T}} - 1\right)$$

However surface leakage is the predominant node for silicon leakage and random surface contamination accounts for a wide range of

capacitance leakage time constants (about 2m sec to 2sec).

Lateral PNP

In dynamic circuitry it is quite common to use a coupling or delay device under a clocked power line to sample and store a logical value on an MOS capacitance. If this is a large negative voltage, and if the capacitive coupling from the clock to P diffusion is large enough the P-N junction (a) can be driven into conduction on the + going edge of the clock, causing lateral PNP transistor action, and significantly degrading the stored "1" level.

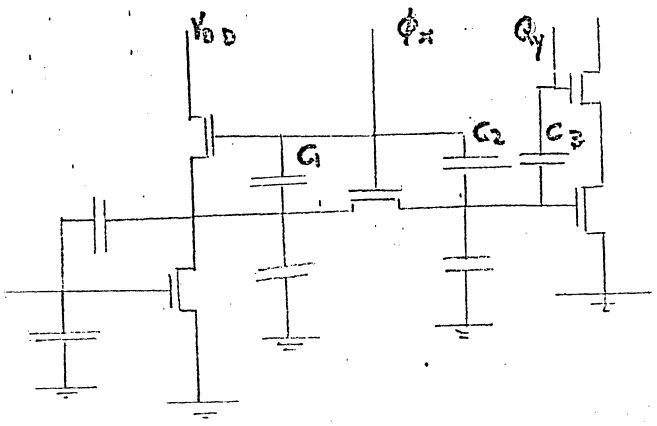


The effects of this parasitic are reduced with careful layout of clock lines and overlap capacitances, and by making the coupling device minimum width, but slightly longer than minimum length.

Capacitance Parasitics

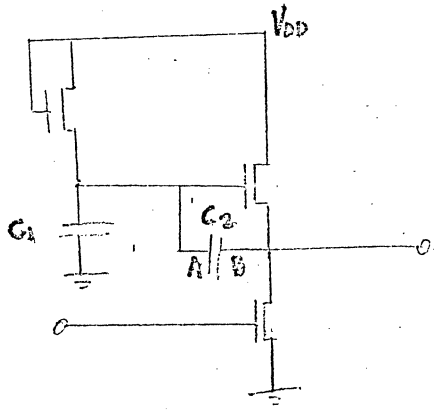
Several capacitances can be avoided with careful layout, which will result in higher component performance. Other capacitances should be considered, which aid performance.

Example 1.



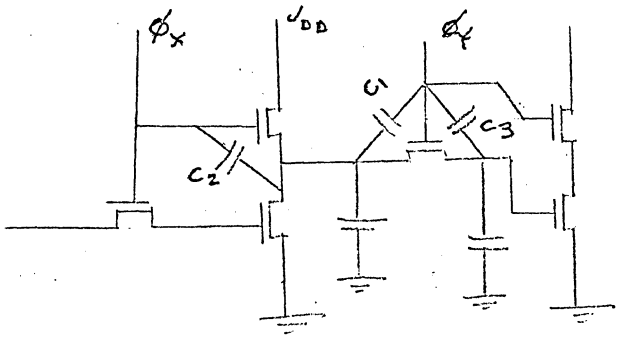
Capacitor C_1 and C_2 will cause significant degradation of a stored "1" level on the gate of Q_1. However, they will enhance the stored "0" level. Note that C_3 can be chosen to balance the degradation caused by C_2.

Example 2.



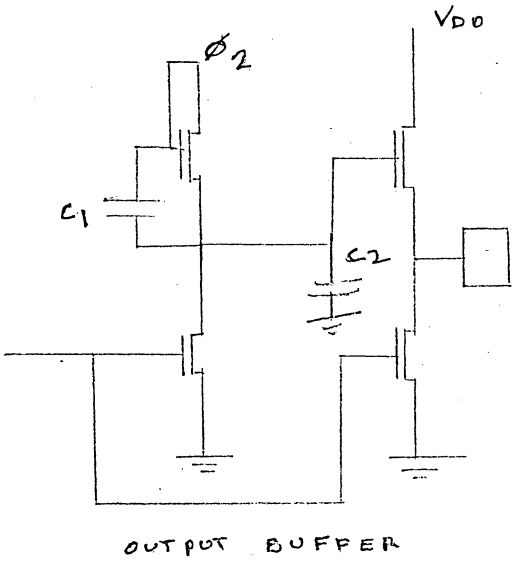
In this example C_2 is designed into the circuit to improve its speed characteristics, and C_1 is parasitic. C_1 is reduced significantly if C_2 is made as a thin oxide capacitor where side B is P diffusion and side A is metal.

Example 3.



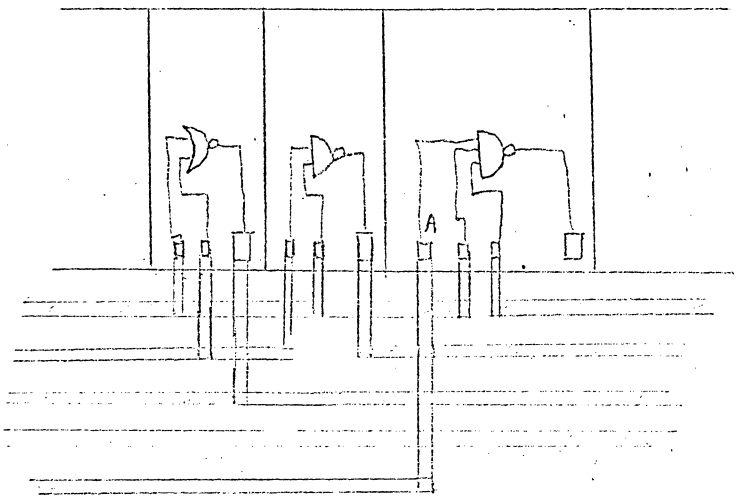
In the ratioless dynamic shift register the capacitor C_1 is designed in to enhance the "1" level while C_2 and C_3 are minimized to prevent "1" level degradation.

Example 4.



In this example the capacitor C_1 degrades the "1" level stored on C_2 when ϕ_2 goes to ground. The "1" level here must be very high in order to achieve a solid "1" level at the output.

Example 5.



In this example the three input NAND has 4 parasitic capacitances coupling noise signal to the input A. It is possible that these signals can be either aiding or opposing. Timing simulation and cell noise immunity allow the engineer to determine if false data will enter at A. The situation can be corrected by adding parasitic capacitance to ground or to an opposing phase signal.

Drain-Source Punch Through

This breakdown phenomenon limits the voltage across a transistor, causing the MOS device to act much like a Zener. Notice then, that the only current limiting is external circuitry.

This phenomenon is observed in circuitry with abnormally large voltage swings, as an output voltage which never reaches its appropriate supply limit.

$$V_{P\dagger} = \frac{Q}{2 K_S \epsilon_0} N_D (1eff)^2$$

This can happen in either switch or 1 ad device if the effective channel length gets too small. Load device breakdown causes excessive supply current and poor "0" levels. For this reason minimum length load devices should be avoided if large signal swings occur.

Parasitic Resistance

The P diffusion and poly silicon layers have a rather high resistance. Care must be used if design requires these layers to conduct large current.

As illustration suppose an output transistor must conduct 2 milliamperes, with V_{DS} = 3 volts. Suppose this transistor must be drawn 20 x .4 mils. If drawn as two parallel P-diffusions (20 x .4) with contacts at one end, then current in the P diffusion debiases the other end, and therefore failing to meet requirements with 25 squares resistance.

Now suppose that the transistor is drawn as an interdigitated device with 2 drain fingers 5 x .3, 3 source fingers 5 x .3. This still has 3.3 squares of resistances.

This device can only be drawn with metal contacts running the full length of the source and the drain thereby cutting parasitic resistance to .1 square.

Similarly this high current transistor cannot be connected to the bonding pad with high resistance poly silicon. It must be connected with metal.

But even metal has resistance and a thousand squares of ground would not be uncommon between the bonding pad and the final cell, causing an increase in ground level, noise on the ground, and V_{BE} effect on the switch device.

Sheet Resistance

Pd	Poly	Metal
$60 \begin{smallmatrix} + 40 \\ - 10 \end{smallmatrix}$ Ω/		

MOTOROLA

inter-office correspondence

From: Don Black
Jim Remedi

Date: February 17, 1971

To: Durrell Hillis

Subject: MOS Array Design and Checkout Procedure

xc Bob Handy
Tom Bennett
All MOS Engineers and
Layout Draftsmen

The following will be the new design and checkout procedure for all new arrays coming from the MOS group.

Attached to the end of the memo are copies of the cell checkout form, array checkout form, and matrix board wiring form.

I. Obtain customers specifications or logic diagrams.

A. Check specs with reliability

II. Design or convert logic into the appropriate Motorola cell set.

A. Partition logic

1. Arrays will have 900 linear mils maximum.

B. Minimize logic

1. Don't convert from positive to negative logic or vice-versa.

C. Think about how you will test the array while it is being designed.

D. All logic drawings should be completely interconnected. No lines left hanging with names.

1. Exceptions V_{DD}, V_{GG}, G_{ND}, and possibly clocks.

E. Cell names beside each and every logical symbol.

F. Current and Power consumption calculations.

III. Logic diagram should be checked by array designer.

III-A. Any new required cells should be designed by CAD people.

A. Check of mylar by two circuit engineers and processing.

1. Device sizes
2. Design rules

B. Digitize cell

C. Check coding and make corrections

D. Check 500X plots (2 different people)

1. Device sizes
2. Design rules

E. Sign off processing

F. Sign off to cell library

A. NO CHANGES IN CELLS IN LIBRARY EXCEPT BY PROJECT LEADER.

IV. Logic diagram simulated

A. Simulate with test pattern OR

B. Simulate with a functional logic checking pattern

1. For random logic control arrays
2. Check critical timing paths

V. Design review of simulated logic diagram and sign off.

A. Check by original designer

B. Project leader

C. Sign off by project leader

1. ALL CHANGES IN LOGIC MUST BE APPROVED BY PROJECT LEADER.

V-A. Customer verify simulation

VI. Draftsman takes signed-off logic diagrams and performs layout of 400X.

A. First makes 100X sketch to obtain rough cell placement.

VI-A. Designer writes test pattern if not already done.

A. Simulate test pattern to make sure it is OK. Then sign off.

1. Keep revision number updated in file for probe and functional test patterns.

B. Write DC test pattern

C. Write preliminary array specifications.

VII. Check of 400X layout

A. Check by layout draftsman

1. Continuity
2. Correct cells are used
3. Design rules in interconnect area
4. I/O locations of cells
5. Continuous metal bus lines with minimum resistance on G_{ND}, VDD, VGG, and clock lines.
6. All output buffers have metal from cell to pad
7. All required alignment marks are in place and test devices in periphery.

B. Check by design engineer and sign off.

1. Continuity
2. Correct cells
3. Good bus structure
4. Critical timing paths
5. Distribution of pads
6. Protection devices on all inputs including V_{GG}, but not VDD and G_{ND}.

C. Check by packaging engineer and sign off.

1. Pad spaced for good assembly
2. Does it fit in required package

D. Check by processing

E. Check by product engineer

F. Check by reliability

VIII. Digitize Array

VIII-A. Have matrix boards and probe card made.

A. Two matrix boards required one for probe and one for final test.

IX. Plot and check stick diagram by original layout draftsman.

A. Things to check

1. Continuity
2. Correct cells used

a. Includes alignment cells and test devices

3. Interconnect gets into cell in right location

X. Plot and check of full composite and separate layers of interconnect area by design engineer.

A. Things to check

1. Alignment of cell I/O's and interconnect
2. Design rules in interconnect area
3. Power bus metal continuity and low resistance
4. All alignment marks present and test devices
5. Protection devices on all inputs including V_{GG}, but not V_{DD} and G_{ND}.

XI. Release to artwork generation by project leader

A. ANY CHANGES IN LAYOUT MUST BE SIGNED BY PROJECT LEADER.

XI-A. Obtain 200X plots on Cal-Comp of separate layers.

XII. Check of artwork copies, black and white both + and - copies, against pen plots by original layout draftsman. Do this on light table.

XIII. Check of artwork copies against pen plots by design engineer.

A. Opaque all pinholes in Gerber artwork.

B. Provide blue line copies of artwork copies showing typical spacing, minimum spacing, and die size on each layer to mask shop.

XIV. Release to mask shop.

XV. Insure that masks are not mirror imaged.

XVI. Provide processing with blue line copies of artwork copies showing typical spacing, minimum spacing, and die size in each layer.

XVII. Provide processing and product engineering with 40X colored overlays. (Available in mask shop.)

Don Black
Don Black

Jim Remedi
Jim Remedi

DB/JR/1a

NEW MOS CELL CHECKLIST

	Signature	Date
Mylar:		
1. Compatible with cell library		
2. Continuity (project leader)		
3. Device Sizes a. cell designer b. circuit engineer c. project leader d. processing		
4. Separate layer-line widths and spacing a. cell designer b. circuit engineer c. processing		
5. Overlapping layers a. cell designer b. circuit engineer c. processing		
6. Sign-off to digitizing (cell designer)		
Check Plots:		
1. Continuity (project leader)		
2. Device sizes a. cell designer b. circuit engineer c. project leader d. processing		
3. Separate layers-line widths and spacings a. cell designer b. circuit engineer c. processing		
4. Overlapping layers a. cell designer b. circuit engineer c. processing		
5. Sign-off to cell library a. cell designer b. processing c. project leader		

MOS ARRAY CHECKLIST

	Signature	Date
Designs:		
1. Reliability OK specifications		
2. Simulation of logic (designer)		
3. Sign-off of logic diagram a. designer b. project leader		
Layout:		
Mylar:		
1. Checks by layout draftsman a. continuity b. correct cells used c. I/O location of cells d. Design rules in interconnect area. e. Continuous metal bus lines with minimum resistance on G_{ND} and clocks lines f. All output buffers have metal from cell to pad. g. All required alignment marks in place, and test devices.		
2. Check by design engineer a. continuity b. correct cells c. good bus structure d. critical timing paths e. distribution of pad f. protective devices on all inputs and V_{GG} but not G_{ND} and V_{DD}.		
3. Sign-off by packaging engineer a. pad distribution b. fit in required package		
4. Sign-off by processing		
5. Sign-off to digitizing (project leader)		

MOS ARRAY CHECKLIST cont'd

	Signature	Date
Plots:		
1. Check by layout draftsman of stick plot a. continuity b. correct cells used c. interconnection into cells		
2. Check by design engineer of full composite a. alignment of cell I/O's and interconnect b. line widths and spacings of interconnect area c. Overlap of layers in interconnect area d. low resistance and continuity of busses e. all alignment marks present f. protective devices on all inputs including VGG but not GND and VDD g. Test devices present		
3. Sign-off to artwork generation (project leader)		
Artwork copies:		
1. Check by layout draftsman a. all layers checked by overlaying on light table of artwork copies and Cal-Comp plots of separate layers.		
2. Check by design engineer a. all layers checked again on light table b. opaque all pinholes in Gerber artwork		
3. Release to mask shop (project leader)		
Masks:		
1. Design engineer check masks for absence of mirror image.		

MOS ARRAY CHECKLIST cont'd

	Signature	Date
Testing:		
1. Simulate functional test pattern.		
2. Probe cards		
3. Matrix boards both probe and final test (product engineer)		

ARRAY NAME _____

PACKAGE

TESTER CHANNEL		MATRIX BOARD NUMBER	ARRAY PIN NUMBER	ARRAY PIN NAME
REC	1	2		
	2	4		
	3	6		
	4	8		
	5	26		
	6	28		
	7	30		
	8	32		
	9	50		
	10	52		
	11	54		
	12	56		
	13	61		
	14	62		
	15	63		
	16	64		
DRIVER	1	9		
	2	49		
	3	11		
	4	16		
	5	17		
	6	18		
	7	23		
	8	24		
	9	25		
	10	33		

ENGINEER APPROVED	NAME	DATE

SHEET 10

ARRAY NAME _____

TESTER CHANNEL	MATRIX BOARD NUMBER	ARRAY PIN NUMBER	ARRAY PIN NAME
DRIVER 11	55		
12	57		
13	53		
14	51		
15	46		
16	31		
17	35		
18	45		
19	37		
20	41		
21	39		
22	44		
$\phi 1$	34		
$\phi 2$	36		
$\phi 3$	38		
$\phi 4$	40		
V_{SS}	10		
V_{GG}	14		
V_{DD}	12		

SPECIAL INSTRUCTIONS

ENGINEER APPROVED	NAME

SHEET 20

AN-539
Application Note

INTERFACING WITH MOS I/C's

Prepared by
Tom Reynolds
Applications Engineering

This application note discusses the problem of interfacing MOS integrated circuits with the logic levels of MECL, MDTL, MTTL, and MRTL. The emphasis is placed primarily on the use of other integrated circuits to achieve this interfacing.

MOTOROLA *Semiconductor Products Inc.*

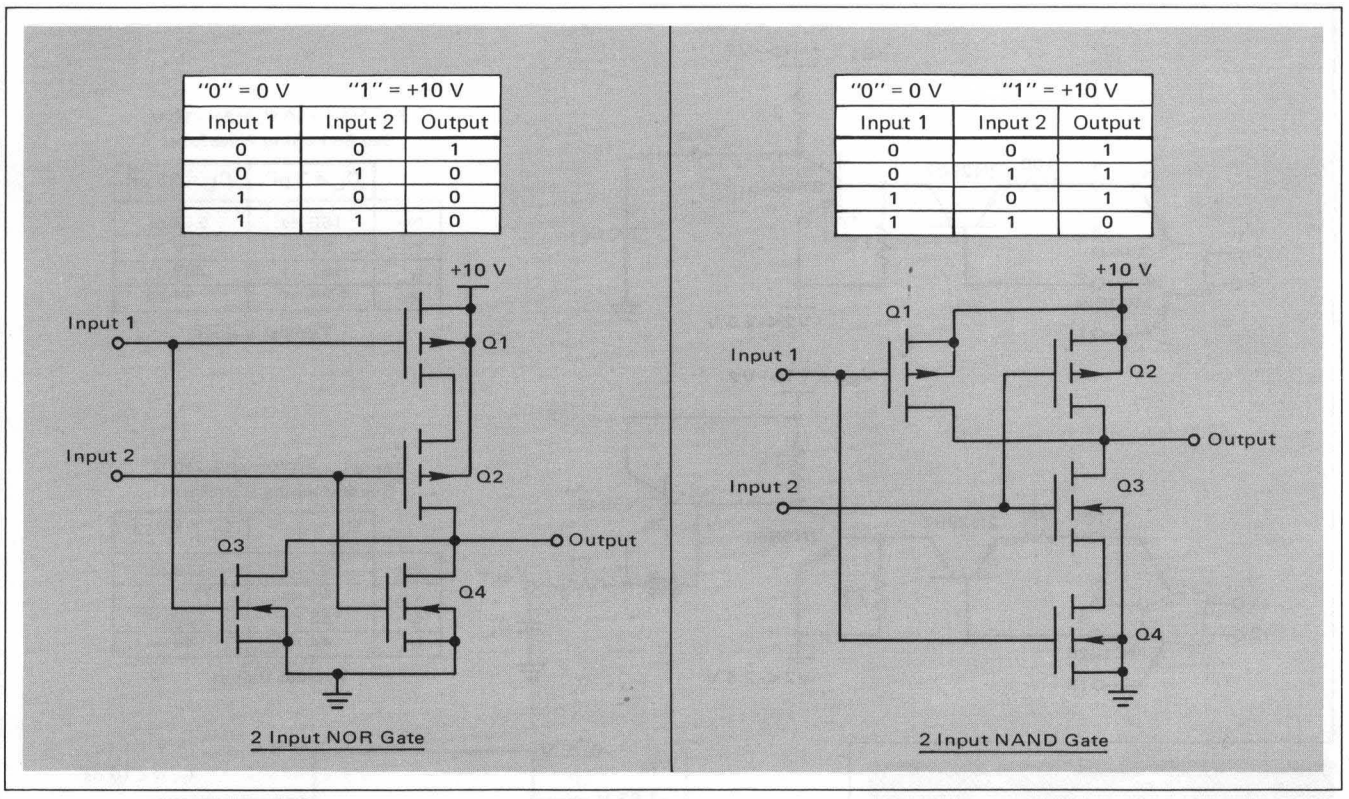


FIGURE 2 – Circuit Configuration for CMOS Gates

Thus, Q1 and Q3 function as one inverter circuit and Q2 and Q4 function as another. When input 1 is at +10 V, Q1 is OFF and Q3 is ON. When input 1 is at 0 V, Q1 is ON and Q3 is OFF. A similar statement can be made about Q4 and Q2. Since Q1 and Q2 are connected in series and Q3 and Q4 are in parallel, the output is at +10 V only when both inputs are at 0 V. This configuration yields the truth table of a NOR gate. The NAND gate consists of two P-channel devices in parallel and two N-channel devices in series. Its operation is similar to the NOR gate. The MCMOS gate gives low output impedances (about 1 kΩ) in either logic state. It can also operate over a power supply range of +4.5 V to +20 V, although its speed increases as the supply voltage increases. With a +5 V power supply the MCMOS gate inputs are directly TTL compatible with the addition of a resistor from the output of the TTL gate to V_{CC}; however, the output drive capability is not sufficient to drive the input of a high power TTL gate.

THE MECL – MOS INTERFACE

The typical voltage swing at the output of a MECL NOR gate is about 0.80 V; however the minimum specified voltage swing is only 0.70 V. In general, the NOR gate output is not sufficient to drive a silicon bipolar transistor in most switching applications. The MC1024 (see Figure 3) dual

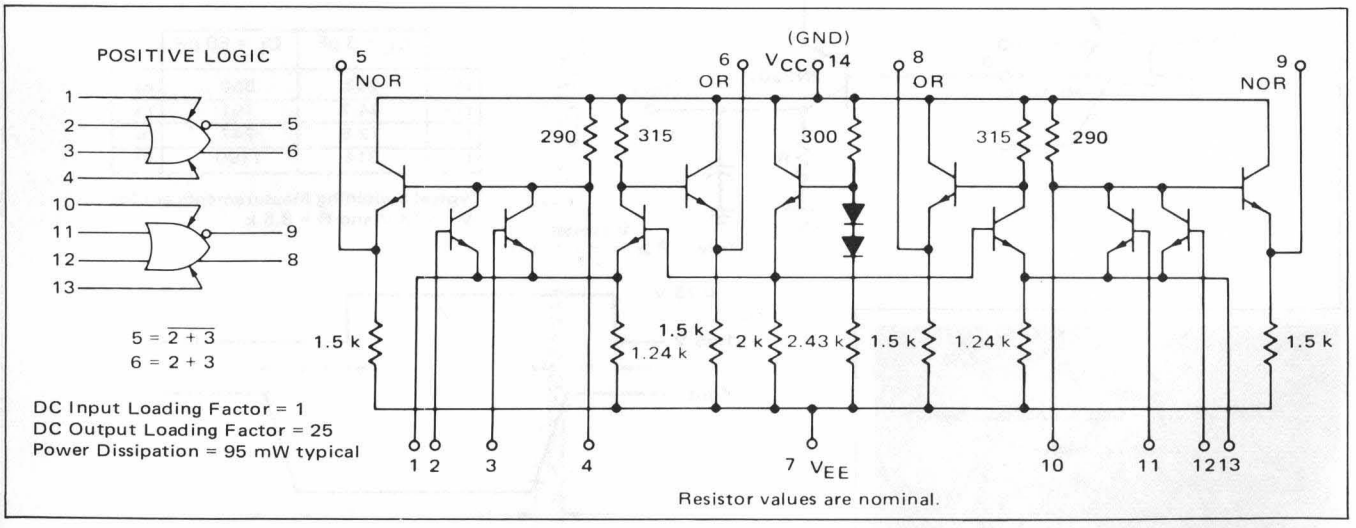


FIGURE 3 – MECL II - MC1024 Dual 2-Input Expandable Gate

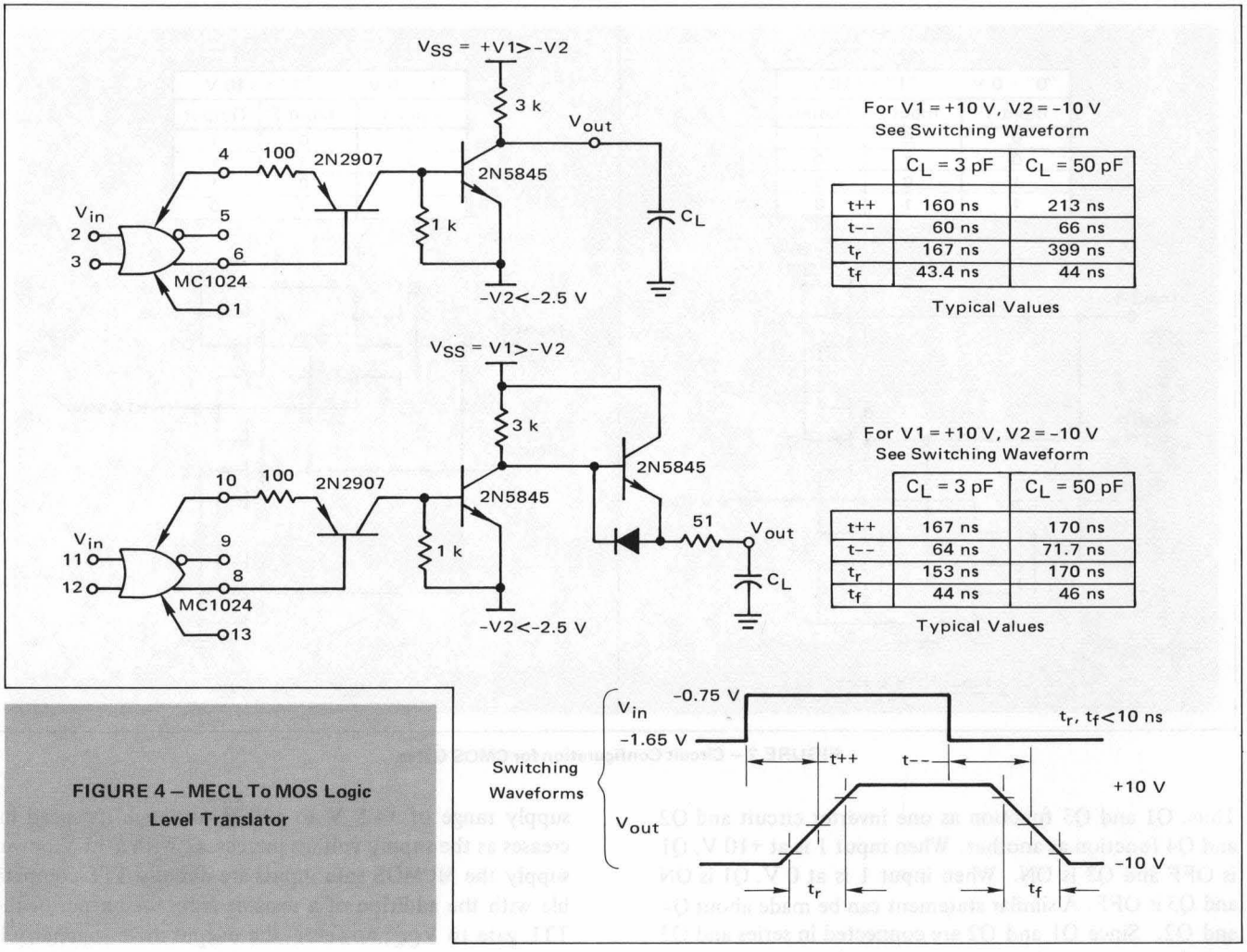


FIGURE 4 – MECL To MOS Logic Level Translator

2-input expandable gate does provide a differential output voltage swing which is sufficient to drive a silicon bipolar transistor. Assume pin 7 is at V_{EE} = -5.2 V and let V_{CC} = 0 V. When pin 3 is -0.8 V, pin 6 is about -0.8 V as well as pin 4. When pin 3 is -1.5 V, pin 6 is about -1.60 V and pin 4 is 0 V. These output signals make possible the use of the discrete interface circuits shown in Figure 4. The differential voltage, which appears between pins 4 and 6

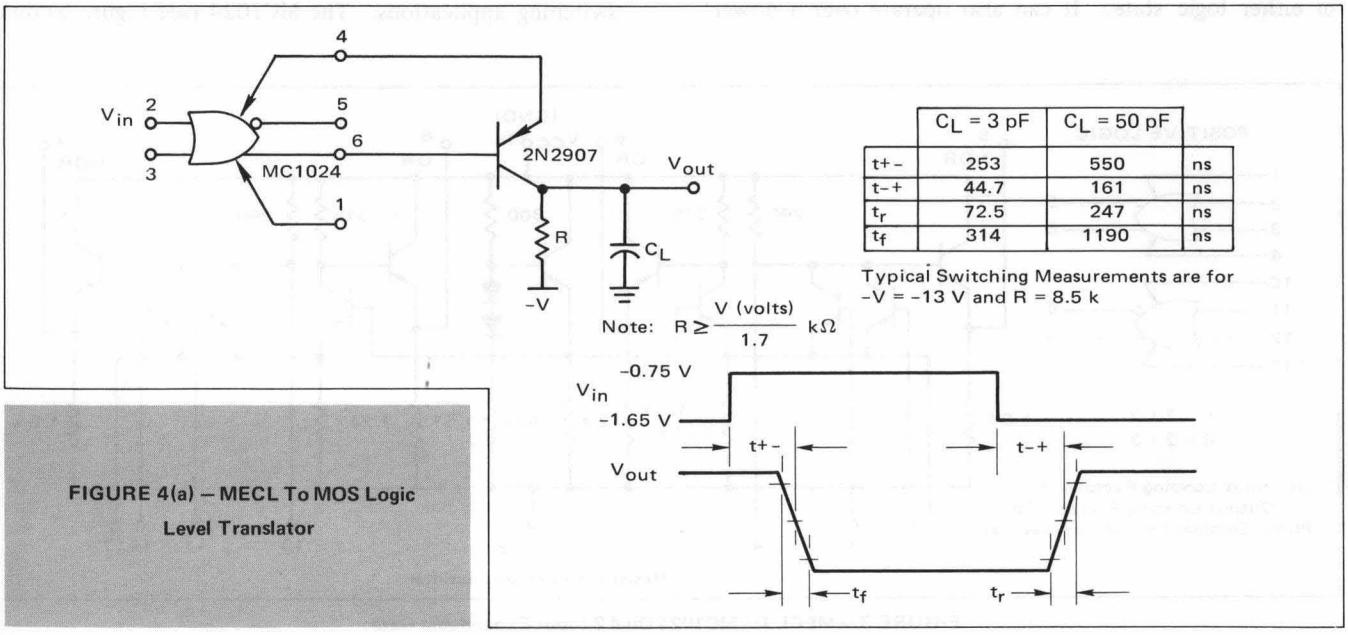


FIGURE 4(a) – MECL To MOS Logic Level Translator

or pins 10 and 8 of the MC1024, is used to bias the base emitter junction of a PNP transistor. The PNP transistor provides voltage level shifting as well as base drive to the NPN transistor. The voltage -V2 at the emitter of the NPN transistor can be anything less than -2.5 V and within the collector-emitter breakdown of the PNP transistor. V1 can be anything greater than -V2 and within the breakdown of the NPN transistor. The typical switching waveforms and times for various capacitive loads are given in Figure 4. Also included in Figure 4 is an interface circuit which has an active pull-up. Switching times for this MECL to MOS converter are given.

Another useful and simple MECL to MOS interface circuit is shown in Figure 4a. This circuit can be used to interface with MOS when the substrate is at ground (0 V). The value of R must satisfy the inequality $R \geq [V(volts)/1.7]$ kΩ since the collector of the PNP is effectively a current source. Switching times for several load capacitances are included in the figure.

Driving MECL gates with MOS circuitry is less expensive than driving MOS with MECL. Figure 5 shows a MCMOS NOR gate driving a MECL NOR gate. In one case the MCMOS NOR gate is operating between +5.2 V and -5.2 V. At this point a clamp diode to V_{BB} is required to prevent the MCMOS gate from pulling the MECL gate input above -0.6 V. In the other case the MCMOS gate is operating between 0 V and -10 V. Here a clamp diode is required to the -5.2 V supply to prevent the voltage on the MECL gate from falling more than a diode drop below -5.2 V. If the supply voltages for the MCMOS gate were 0 V and -5.2 V, the MCMOS gate could directly drive the MECL gate; however the MCMOS speed is considerably reduced at the 5 V potential difference. Driving the MECL gate with a P-channel push-pull buffer is similar to driving with a MCMOS gate. If an open drain output buffer is being used, an external pull-down resistor is required. The basic requirement on the MECL gate input is to maintain its voltage potential between 0 V and -5.2 V.

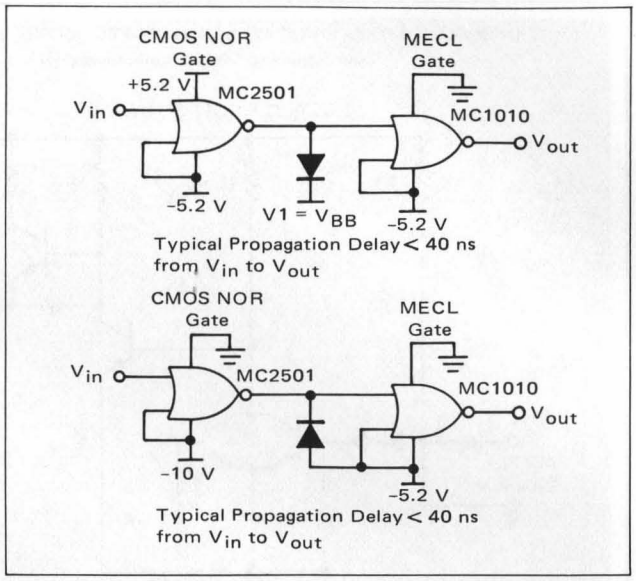


FIGURE 5 – CMOS To MECL Translation

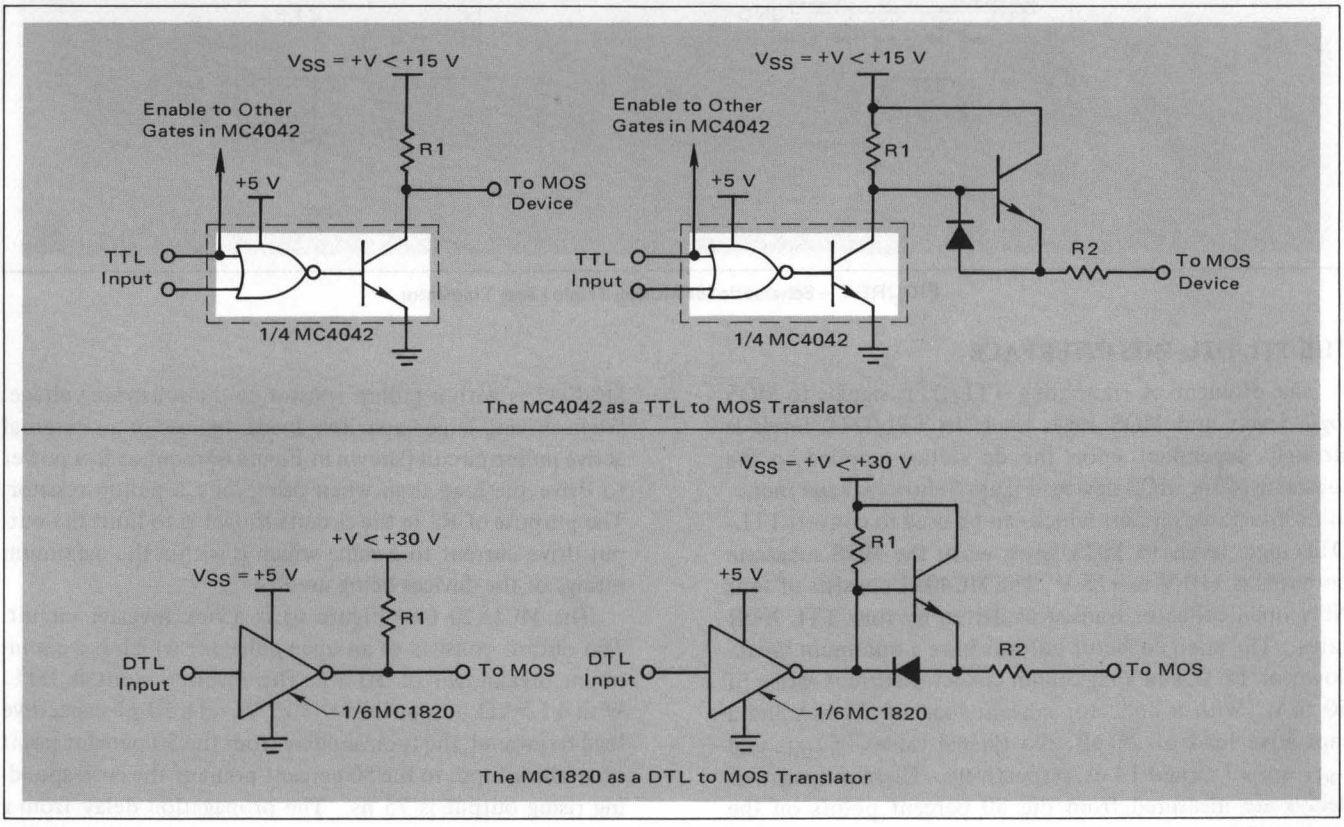


FIGURE 6 – Translators for Positive Substrate Voltage

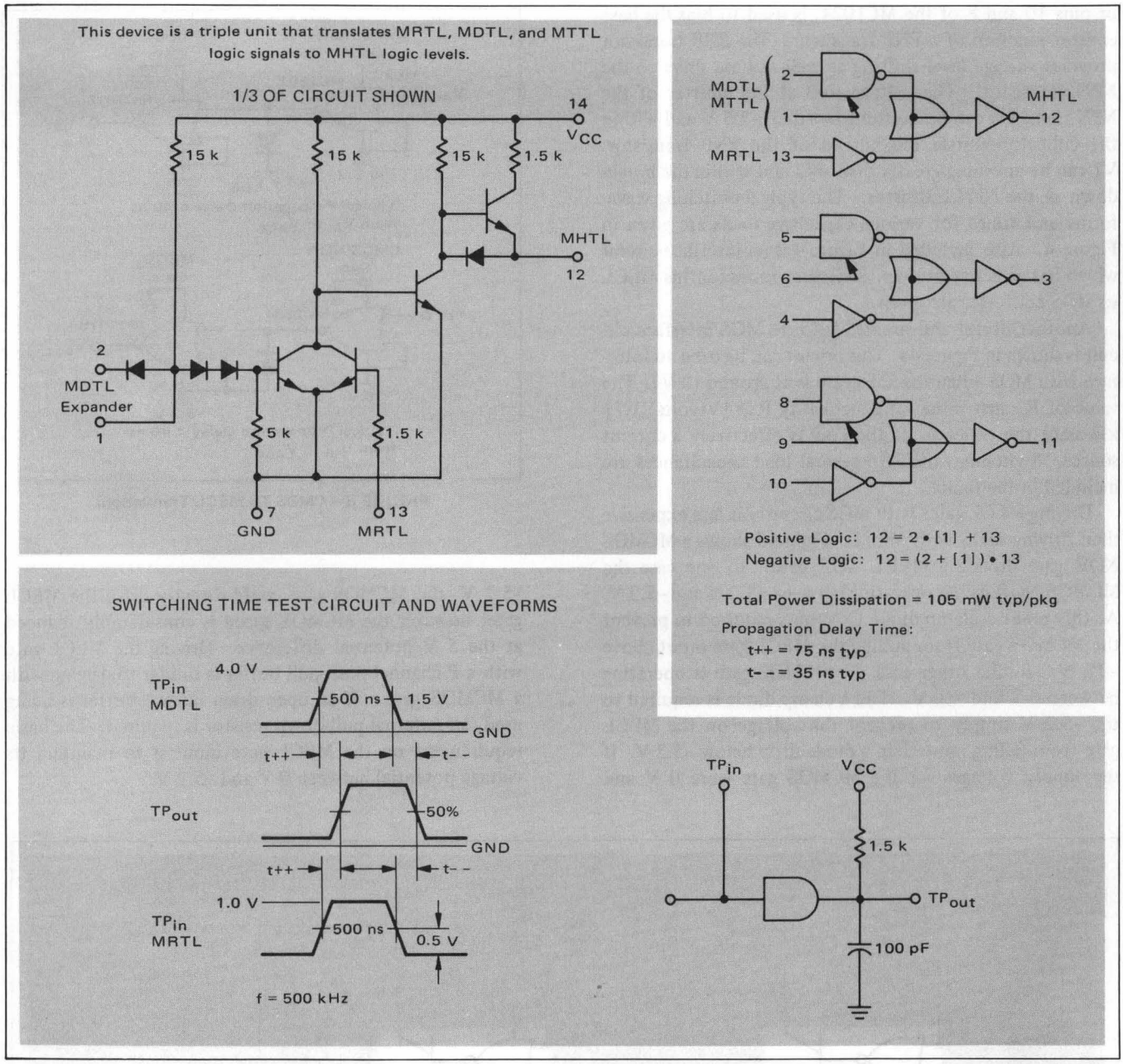


FIGURE 7 – Schematic for MC666 Triple Level Translator

THE TTL/DTL–MOS INTERFACE

The problem of translating TTL/DTL signals to MOS logic levels and MOS logic levels to TTL/DTL levels is strongly dependent upon the dc voltage applied to the substrate of the MOS device. Figure 6 shows several monolithic integrated circuits which can be used to convert TTL/DTL logic levels to MOS levels when the MOS substrate potential is +10 V to +15 V. The MC4042 consists of four NPN open collector transistors driven by four TTL NOR gates. The open collector outputs have a minimum breakdown of 15 V, and a maximum collector current rating of 50 mA. With a collector current load of 30 mA and a capacitive load of 25 pF, the typical values of t_{pd-} and t_{pd+} are 13 ns and 14 ns, respectively. These propagation delays are measured from the 50 percent points on the input and output waveforms. The simplest way to use the MC4042 is with a pullup resistor to the substrate voltage. When driving large capacitive loads, the use of an external active pullup circuit (shown in Figure 6) requires less power to drive the load than when using only a pullup resistor. The purpose of R2 in the circuits shown is to limit the output drive current to a value which is within the maximum ratings of the devices being used.

The MC1820 (see Figure 6) is a hex inverter circuit. The output consists of an open collector which has a minimum breakdown of 30 V. The inverter input is DTL. With a 1.5 kΩ output load to +15 V and a 50 pF capacitive load to ground, the typical delay from the 50 percent point of a falling input to the 50 percent point of the corresponding rising output is 75 ns. The propagation delay from a rising input signal to a falling output signal is typically

28 ns. The use of the MC1820 as a translator is similar to the use of the MC4042. A circuit showing the use of the MC1820 with an external active pullup is also given in Figure 6.

The MC666 is an HTL device which is useful in converting DTL, TTL, or RTL to MOS levels when the MOS substrate is at a voltage in the neighborhood of +15 V. The device has three level translators, as shown in Figure 7. A translator output will pull a MOS capacitive load to one diode drop below the V_{CC} power supply and within 1.5 V of ground. The specified operating voltage for the MC666 is +15 V ± 1 V; however, the device will operate down to +12 V with a reduced output drive capability.

The MC1489 Quad Line Receiver is useful in converting MOS logic levels to TTL/DTL logic levels. Each of the four line receivers has a response control input which allows one to vary the input switching threshold over a wide range as shown by the graph in Figure 8. The MC1489 is particularly useful in converting MOS output levels to TTL/DTL levels when the MOS substrate is at ground. In this

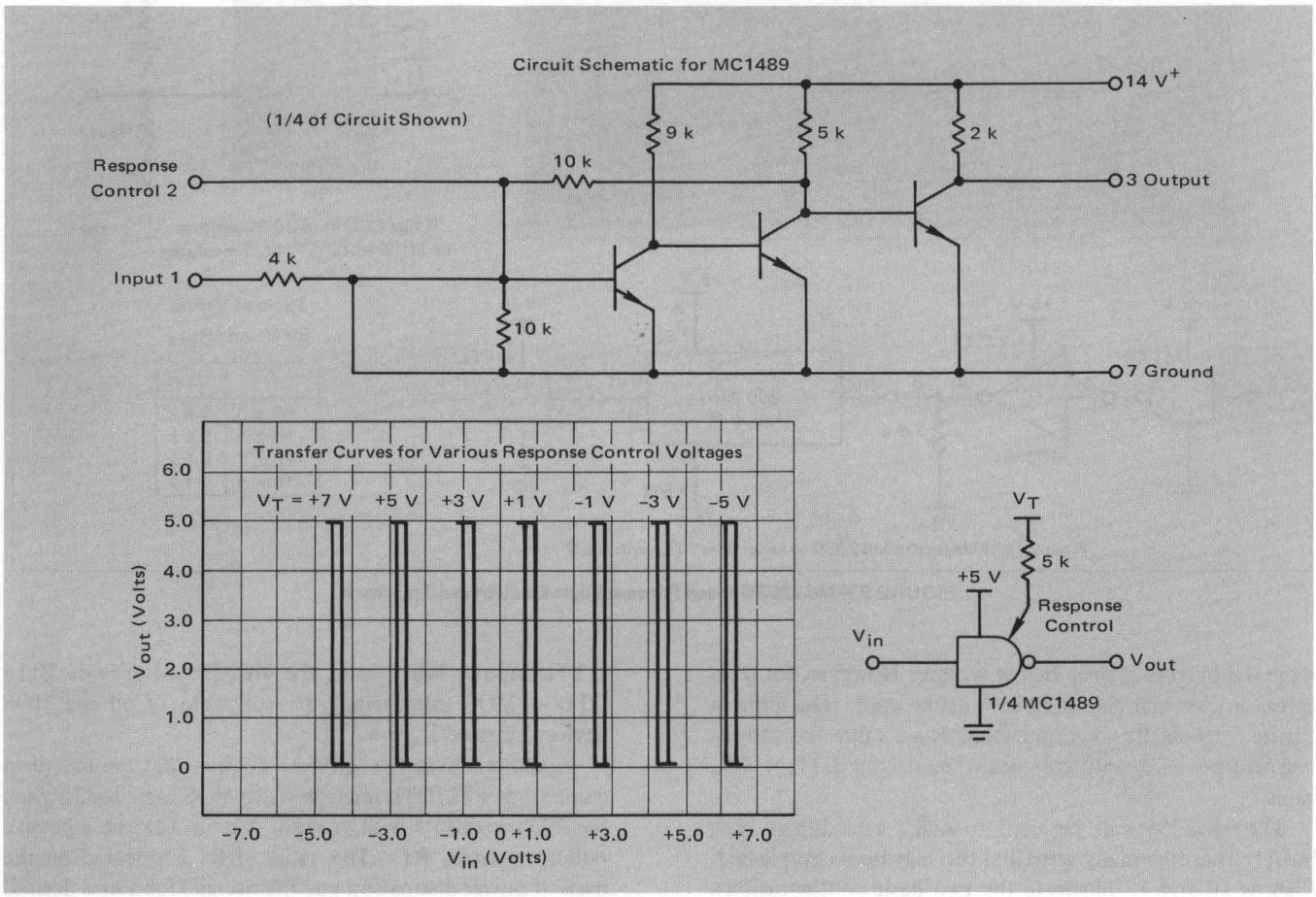
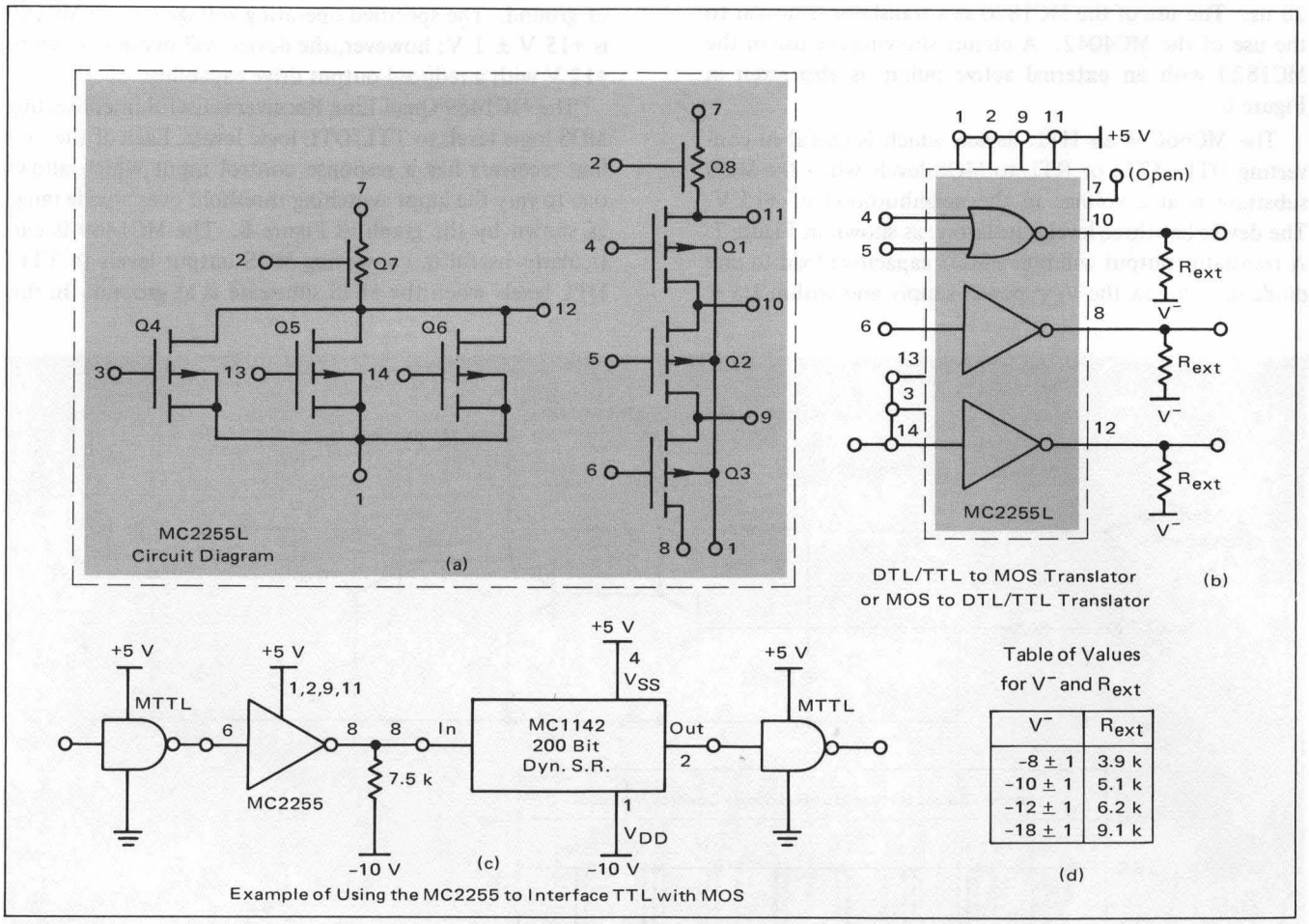


FIGURE 8 – MC1489 Line Receiver

case the current injected into the line receiver response control is set such that the switching threshold is about -3 V or -4 V. The typical propagation delay through a receiver is t_{pd-} = 25 ns and t_{pd+} = 25 ns. The typical power dissipation is 100 mW per package.

The MC2255 General Purpose Logic Element is a PMOS integrated circuit that is useful for interfacing MOS to TTL or DTL. The circuit schematic for the device is given in Figure 9a. The gain of devices Q1, Q2, and Q3 is three times that of Q4, Q5, and Q6; whereas the gain of Q4, Q5, and Q6 is 30 times that of Q7 and Q8. Figure 9b gives the external connections required to create three logic translators. These translators are capable of receiving a DTL or TTL signal and driving a MOS input. In this application the substrates of all the MOS devices must be at +5 Vdc, the TTL/DTL power supply voltage. The value of R_{ext} is selected to produce the desired fall time on the capacitive input of the MOS device. Figure 9c gives a typical application of this type. The MC1142 200-bit dynamic shift register has an output buffer with sufficient drive capability to interface with a TTL gate; however, the input requires at least a 10 V logic swing. One of the translators in the MC2255, along with a 7.5 kΩ external resistor, provides the TTL to MOS logic level translation.

The translators of Figure 9b can also be used to drive TTL or DTL with a MOS input. When using these translators to drive TTL or DTL, the value of R_{ext} is selected to guarantee that the TTL/DTL gate input will be pulled to ground. For Motorola's TTL gates an internal clamp diode on the input prevents R_{ext} from pulling the gate input



V^-	R_{ext}
-8 ± 1	3.9 k
-10 ± 1	5.1 k
-12 ± 1	6.2 k
-18 ± 1	9.1 k

FIGURE 9 – MC2255 General Purpose Logic Element as a Translator

more the one diode drop below ground. However, for DTL gates, an external clamp diode must be used. The table in Figure 9d lists the recommended R_{ext} value for various negative power supply voltages when driving DTL or TTL gates.

The MC2255 can be used to make a push-pull type buffer. There are many ways that this may be accomplished. Figures 10 and 13 illustrate the two basic configurations. Circuit (a) of Figure 10 requires the utilization of all the devices in the MC2255 and provides the fastest switching speeds. Circuit (b) of Figure 13 does not require the use of the three parallel devices which constitute a NOR gate. The two buffers of Figures 10 and 13 require a +5 V and a -10 V power supply. Figures 11 and 12 give the V_{out} versus I_{out} characteristics for the buffer of Figure 10, and Figures 14 and 15 give the same information for the buffer of Figure 13. The basic circuit configurations in Figures 10 and 13 can also be used with different voltage levels to give increased drive capability. Figures 16 and 19 show the buffers with +5 V on the substrate, -7 V on the pull-down resistors, and -15 V on the gates of the pulldown resistor. The V_{out} versus I_{out} characteristics of these two circuits are given in Figures 17, 18, 20, and 21. All of these output buffers have the capability of driving TTL/DTL logic levels when the input is presented with a MOS signal. The buffers in Figures 10 and 13 can also drive MOS with a TTL input. When using the MC2255 to provide TTL/DTL – MOS interfacing, the substrate of all the MOS devices must be at +5 V.

Figure 22 gives two discrete circuits that are useful in converting TTL/DTL logic levels to MOS logic levels when the MOS substrate is at ground. Circuit (a) uses a passive pull-up resistor, R1. The value of R1 is selected on the basis of power dissipation and the rise and fall times desired on the MOS capacitive load. Q1 acts as a level shifter and provides drive to Q2. If $-V2 < -1$ volt, Q1 is never in saturation and therefore has little effect on the speed of the circuit. The circuit speed is dependent primarily on Q2. The operation of the circuit in Figure 22b is essentially the same as in Figure 22(a) except for the active pull-up configuration consisting of Q3, CR1, and R2. Circuit (b) is useful when driving large capacitive loads.

MOS-RTL INTERFACE

There are few integrated circuits which can be used to solve the MOS-RTL interface problem. The application of the MC666 MHTL device shown in Figure 7 was discussed in the section on interfacing with TTL and DTL. The MC1489 line receiver can be used to convert from MOS to RTL when the MOS substrate is at a positive voltage. The line receiver is particularly useful when the MOS substrate is at ground. In this case the threshold at the

line receiver input is set to about -4 V. The line receiver output has DTL logic levels which can be used to directly drive an RTL gate input.

Figure 23 gives three discrete circuits that can be used in converting RTL signals to MOS logic levels. The circuits in (a) and (b) are the most versatile, and their operation has been discussed in the section on TTL-MOS interfacing. These two circuits are particularly useful when the MOS substrate is at the RTL power supply voltage or ground. Circuit (b) has an active pull-up and should be used when driving large capacitive loads. Resistor R1 should be selected on the basis of power dissipation and the desired rise and fall time at the output. If the MOS substrate is at a voltage in the range of +10 V to +15 V, Circuit (c) provides an efficient interface. Again the value of R1 is selected on the basis of available bade drive from the RTL gate,

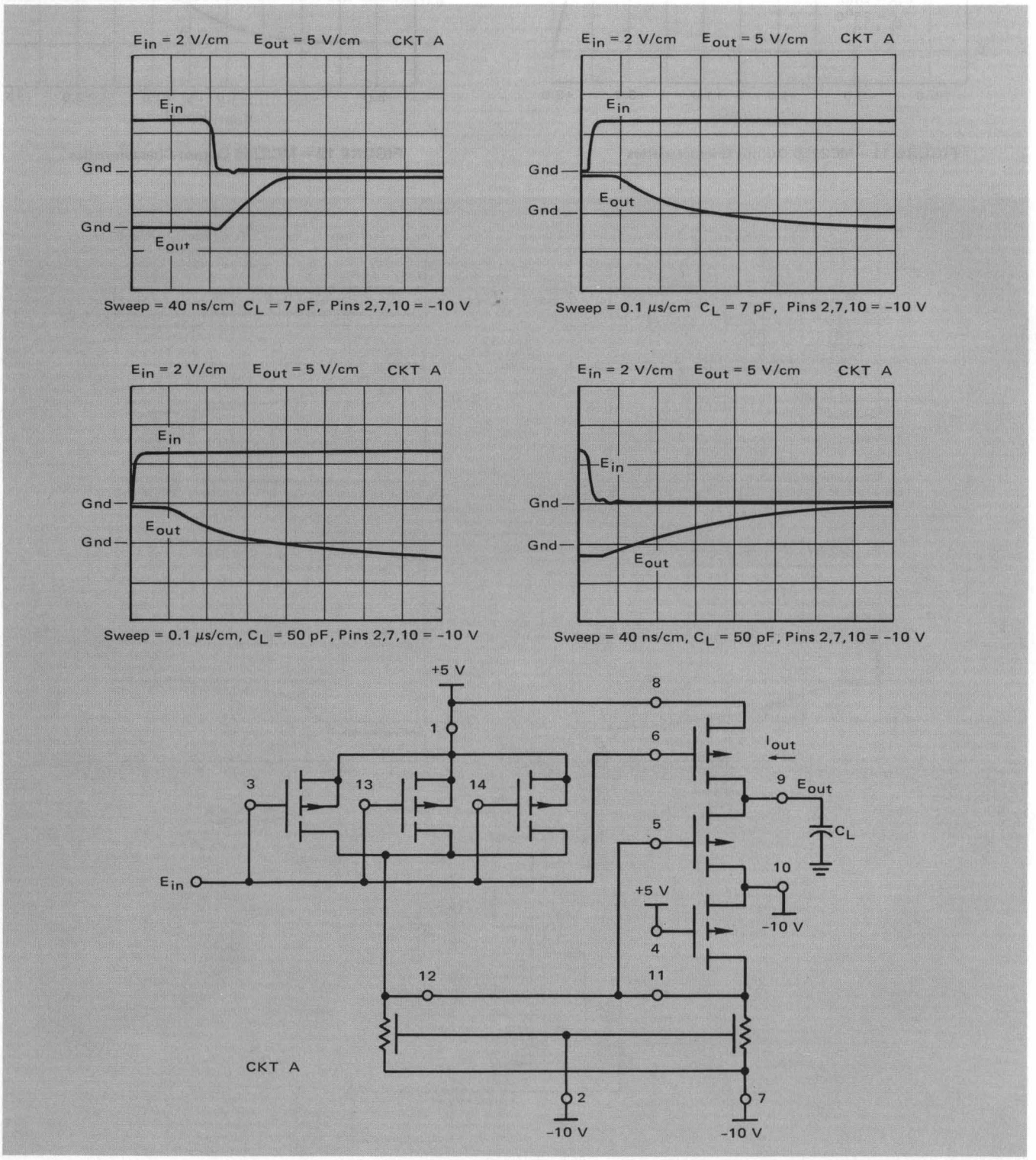


FIGURE 10 – The MC2255 as a Push-Pull Buffer

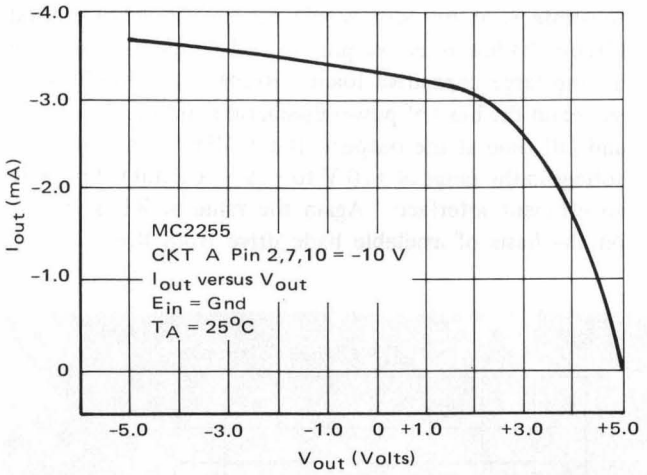


FIGURE 11 – MC2255 Output Characteristics

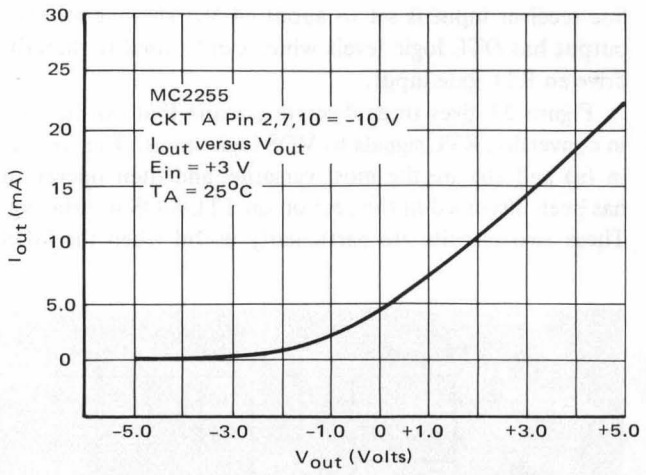


FIGURE 12 – MC2255 Output Characteristics

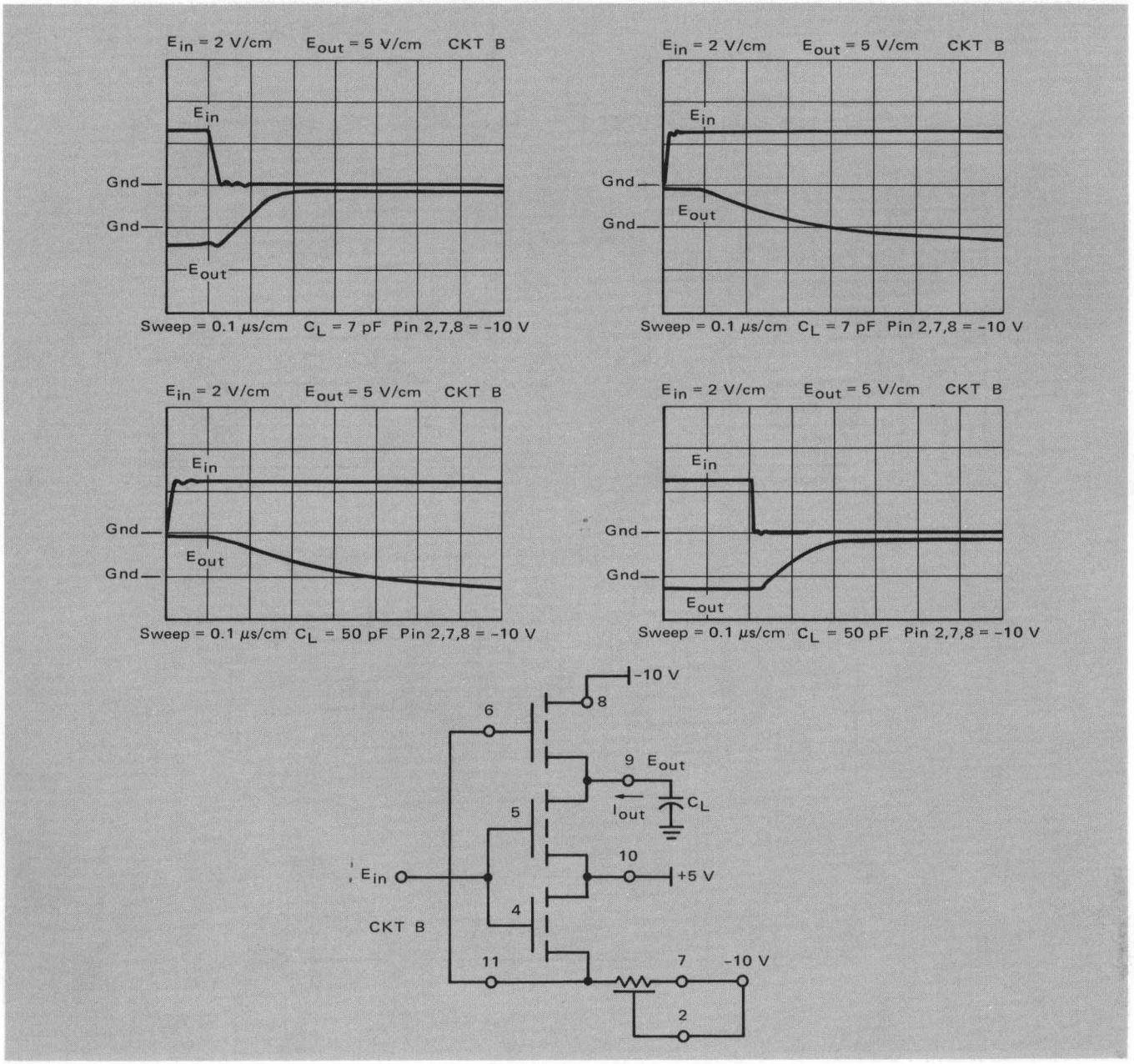


FIGURE 13 – MC2255 as a Push-Pull Buffer

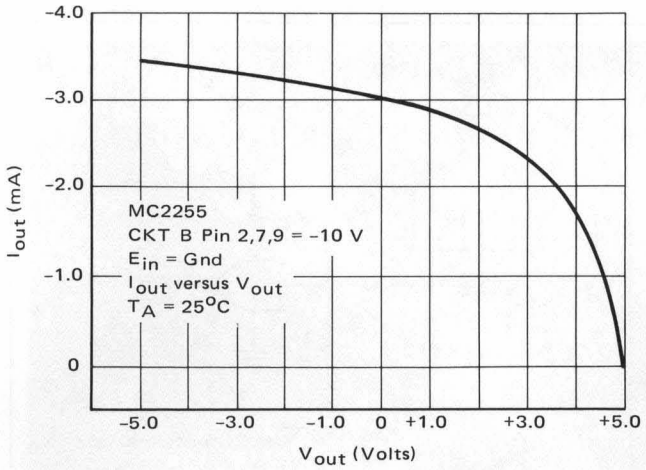


FIGURE 14 – MC2255 Output Characteristics

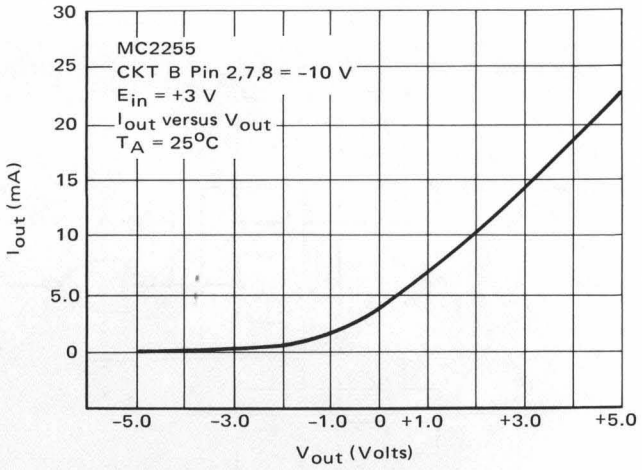


FIGURE 15 – MC2255 Output Characteristics

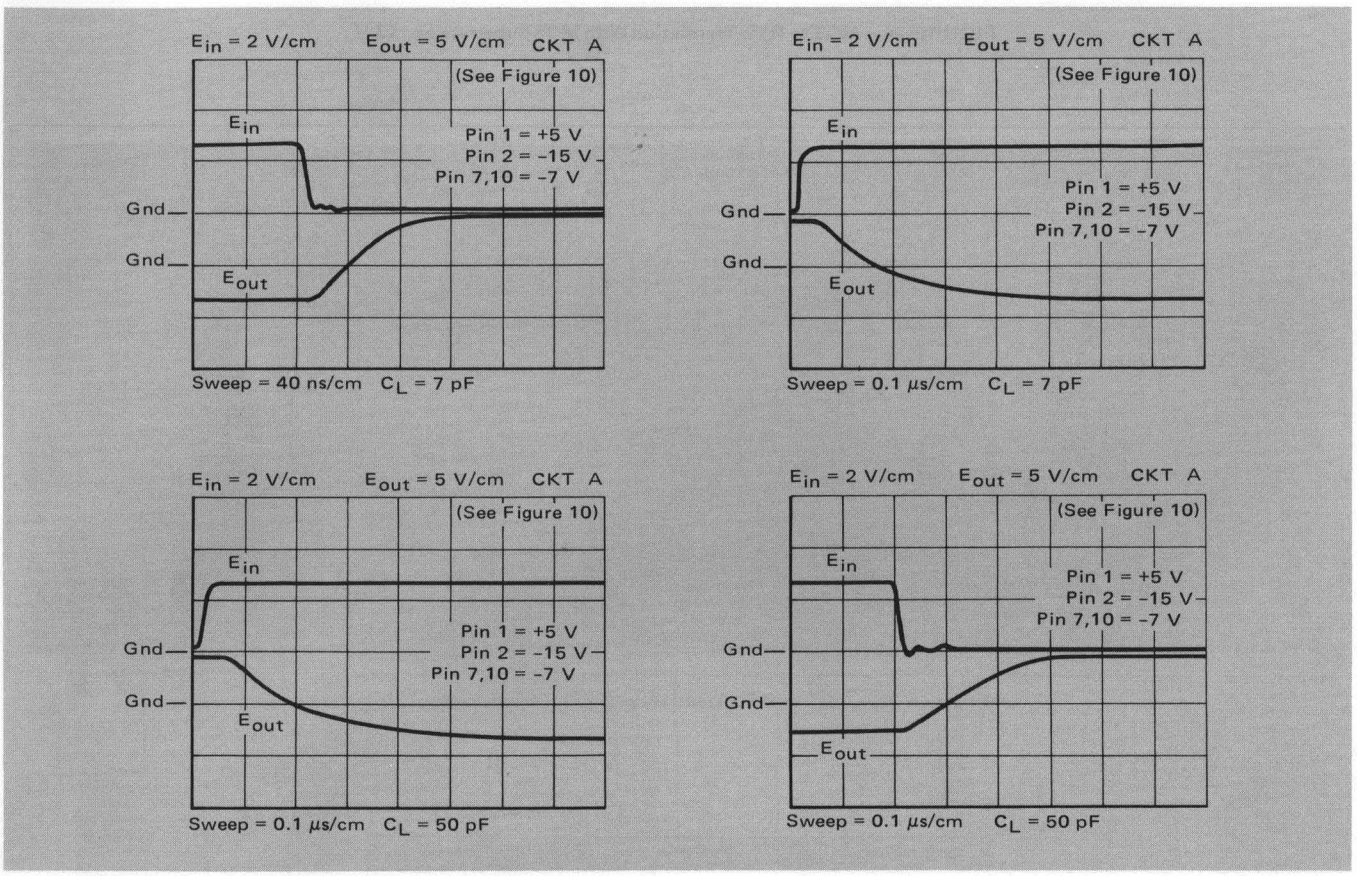


FIGURE 16 – The MC2255 as a Push-Pull Buffer

desired rise and fall times, and power dissipation.

Figure 24 illustrates the conversion from MOS to RTL when the MOS substrate voltage is at +13 V. The diode clamps the gate input to the RTL power supply voltage which prevents the MOS output driver from pulling the gate input above the maximum specified rating at +4.0 V. When V_{CC} = +3.6 V, the clamp diode should be germanium. In Figure 25, the MOS substrate is at the RTL power supply voltage. In this mode of operation, the clamp diode is used to prevent the voltage on the RTL gate input from falling below the -4 V rating.

CONCLUSION

There are a number of integrated circuits which can be used to interface the various logic families with MOS integrated circuits. The applicability of these circuits as translators is dependent primarily upon the MOS substrate potential. In general, it is best to place the substrate at a potential equal to the most positive voltage applied to the logic family with which one is interfacing. A summary of the topics covered in this application note along with their related figures is given in Figure 26.

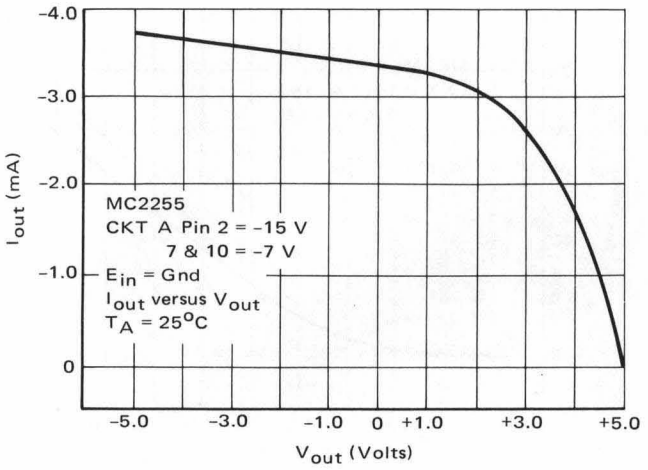


FIGURE 17 — MC2255 Output Characteristics

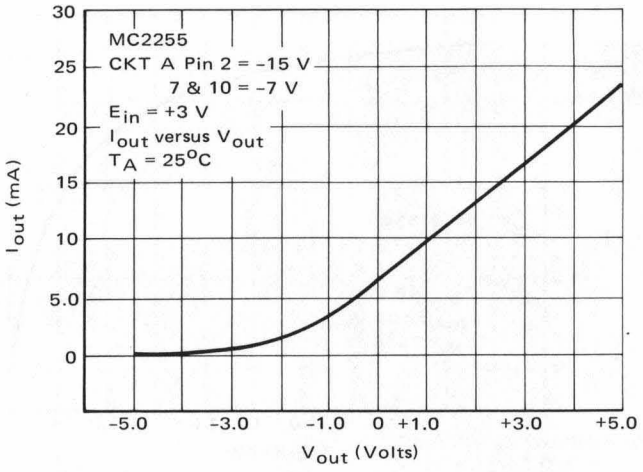


FIGURE 18 — MC2255 Output Characteristics

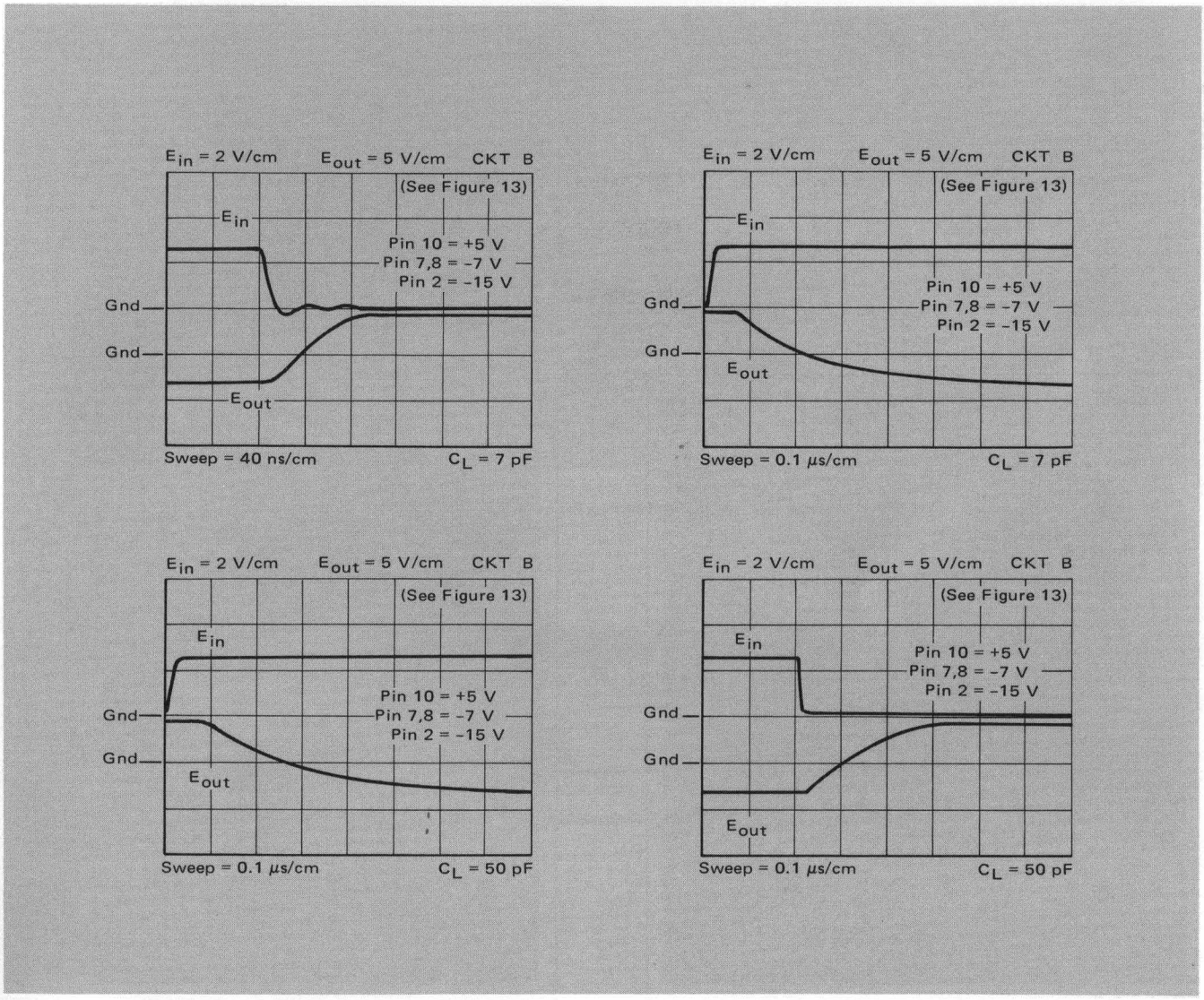


FIGURE 19 — The MC2255 as a Push-Pull Buffer

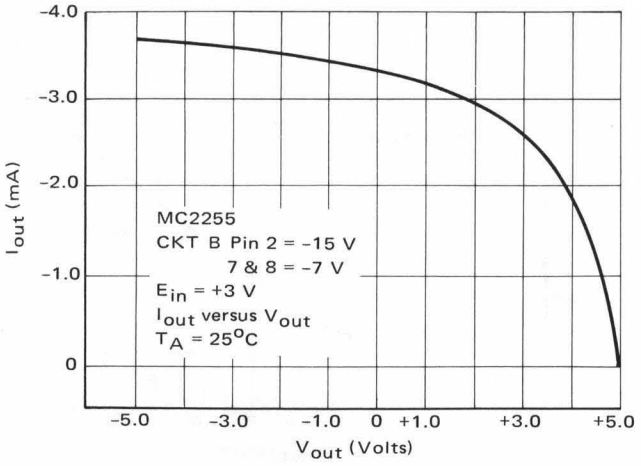


FIGURE 20 – MC2255 Output Characteristics

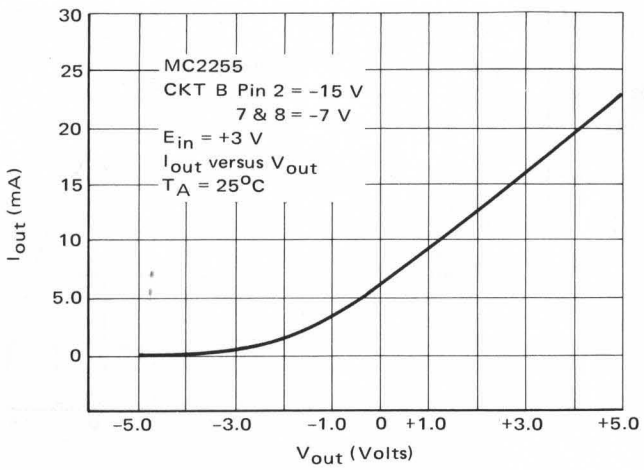


FIGURE 21 – MC2255 Output Characteristics

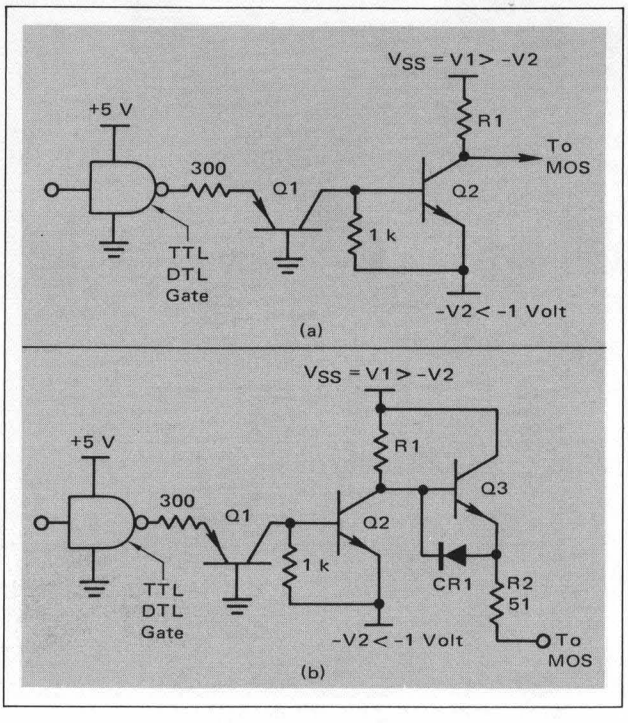


FIGURE 22 – Discrete Buffers for TTL/DTL to MOS Conversion

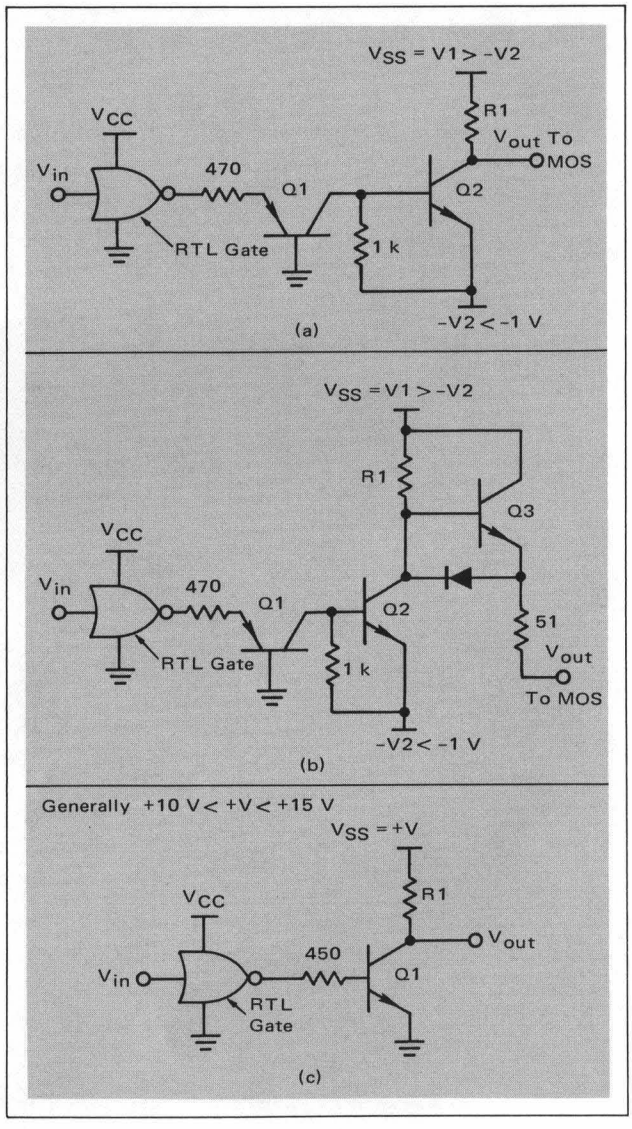


FIGURE 23 – RTL to MOS Translation

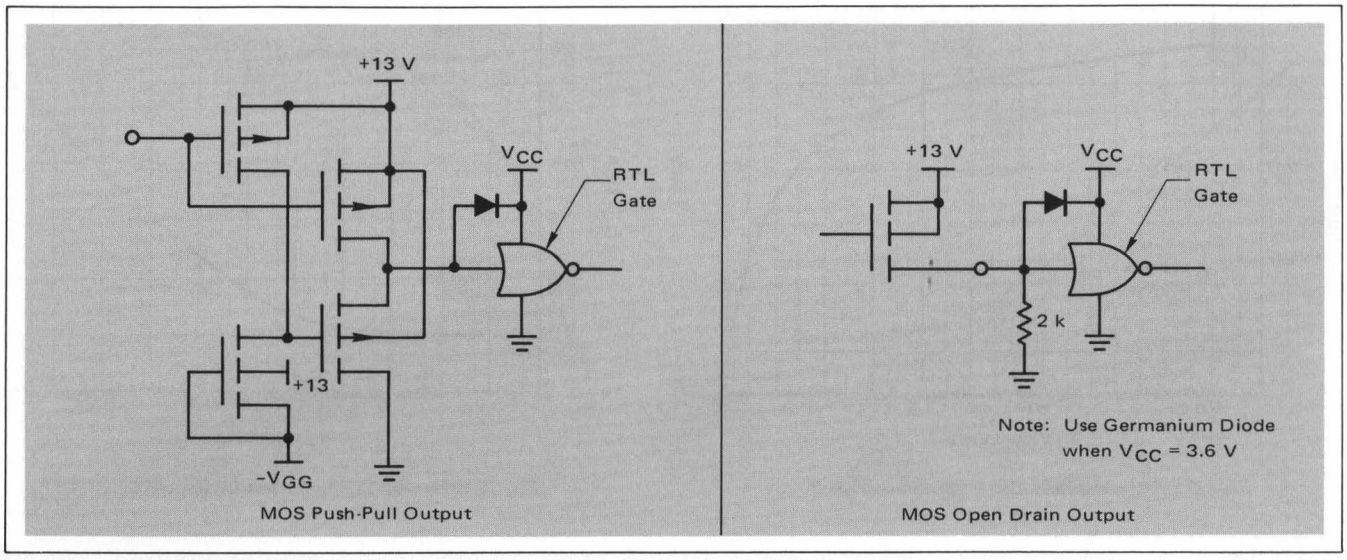


FIGURE 24 – MOS to RTL Translation With MOS Substrate at +13 V

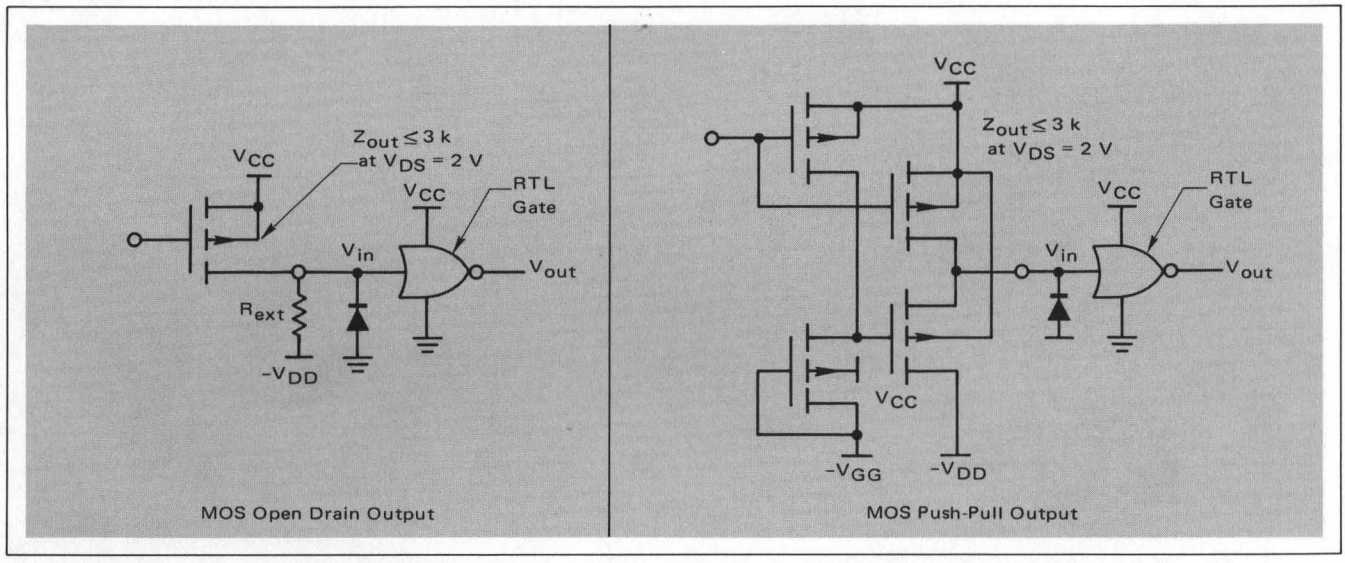


FIGURE 25 – MOS to RTL Translation With MOS Substrate at V_{CC}

Logic Levels To Be Interfaced	Applicable Figures
TTL or DTL to MOS	6,7,9,10,13,16,19,22
MOS to TTL or DTL	9,10,13,16,19
ECL to MOS	4,4(a)
MOS to ECL	5
RTL to MOS	7,23
MOS to RTL	24,25

FIGURE 26 – Summary of Topics and Related Figures

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6202 PRINTED IN USA 1-71 IMPERIAL LITHO 820505 14M

CHAPTER XIV

COMPUTER AIDS - DESIGN SOFTWARE

X. Computer Aids

A. Design Software

1. MOS Device Models in Fortran
2. Timesharing Software
   a. Automatic Cell Design
   b. Transient Analysis-CNET
   c. Chip area estimates
   d. Economic analysis
3. Sceptre
4. Non-Linear D/C Analysis
5. Simul 8

B. Layout Software

1. BLIST
2. PARRAY
3. MARS
4. PDIGT
5. CAMP
6. ATPL
7. ASRD
8. ACD
9. A ROMD

C. Layout Hardware

1. CRT
2. Digitizer
3. Plotter
4. Gerber

D. MOS Cell Library

1. Static High Power HIVTH
2. Static Low Power HIVTH
3. Static High Power LOVTH
4. Static Low Power LOVTH
5. Two Phase
6. Four Phase
7. Shift Registers
8. Peripherals
9. CAD Design Example

Design Software

It is the intent of the MOS Computer Aids Group to provide the MOS design engineer with design approaches which relieve the engineer of design drudgery, thus allowing him more time for creativity.

This section of the MOS Design Manual will contain descriptions of current software of major use in electronic circuit design.

MOS Device Models (FORTRAN)

For SCEPTRE

For NLDCA

For Timesharing

TIMESHARING SOFTWARE

Q Chip

Q Chip is a chip size estimation program. The program reads the CAD cells required to build a chip, and the average fanout, and computes chip size, and associated data. The input data is in data file "DATCHP" in the following format:

```
100 CHIP NAME
110 AVERAGE FANOUT ,NUMBER PADS
120 CELL NAME
130 NUMBER USED
140 CELL NAME
150 NUMBER
 .
 .
200 END
```

```
PROBLEM NAME:  DATCHP

READY
100 TYPICAL DESIGN
110 1.2,17
120 MH01IN
130 3
140 MH02PS
150 4
160 MH01EO
170 1
180 MH01JK
190 3
200 END
SAVE

READY
```

The program is then run as follows:

```
PROBLEM NAME:  QCHIP

READY
RUN

 TYPICAL DESIG

TOTAL CELLS                          11
CELL AREA                  9.960000000E+02
NO OF CELL ROWS                       2
ROUTING AREA               5.428800000E+02
ACTIVE AREA                1.854000000E+02
CHIP SIZE          81                 51
EQUIVALENT GATES                      31
TRANSISTORS                          127
TYPICAL POWER              9.130000000E+01
```

LIBINF - Library Information this program requests option T, or option I.

T = table and prints the current list of available CAD logic cells.

I - information and then asks for a specific cell. It then reaches the library for that cell and prints out all relative information.

SCEPTRE

SCEPTRE is a unified system of digital computer programs by which the electrical engineer can communicate with the computer to determine the initial conditions and transient response of electronic circuits. SCEPTRE has a number of features which make it easy to use. The following is a list of some of the main features in SCEPTRE:

1. Stored Models - Any active element or interconnected group of elements that can be described as a combination of sources, passive elements and mutual inductance may be stored on tape by the user and called into use at any point in a network.

2. Automatic Initial Conditions - The user has the option of using a special portion of the program to determine the initial conditions of a network. He may then either use the transient section in the same run or just accept the output of the initial condition section for inspection. Any run may use the initial condition mode only, the transient mode only, or may automatically combine the two modes.

3. Rerun - Multiple case rerun based on a single master run may be carried out automatically. The user supplies only the changes that apply from the master run for each repeated run.

4. Defined Parameters - A special section has been created to enable the user to define quantities that may be output other than sources or passive currents and voltages. The user may enter systems of first-order differential equations that may or may not have anything to do with a particular electrical network.

5. Output - In addition to the conventional output format, which allows all sources and passive currents and voltages at each solution increment, the user may request as output any defined parameter from item 4. He may also select any element value, step size, and pass count. Time is not the only independent variable for these outputs; the user may select others from a fairly large list.

6. Linearly Dependent Sources - Voltage and current sources that are linearly dependent on resistor voltages and currents respectively, can be accommodated without computational delay. This feature permits the extensive use of the family of small signal transistor equivalent circuits.

7. Subprogram Capability - The user who is familiar with computer programming may write FORTRAN subroutines and insert them in otherwise conventional SCEPTRE runs. This feature permits the extensive use of the family of small signal transistor equivalent circuits.

8. Program Language - The program has been written entirely in FORTRAN IV to facilitate the task of adapting it to digital computers other than the IBM 7090 or 7094.

9. Economical Operation - A new solution approach has been employed to insure rapid solution, and therefore, a comparatively small amount of computer time for most problems.

10. Automatic Termination - Runs may be automatically terminated contingent on the behavior of specified network quantities.

11. Flexibility - Non-conventional source dependencies and network topologies can be accommodated.

12. Save and Continue Capability - Runs may be terminated and then subsequently continued after examination.

13. Input Convenience - Provision has been made for a free-form format for input data.

SCEPTRE can be used to evaluate MOS circuits with reasonable accuracy and with a nominal amount of computer time. The results from SCEPTRE have been checked against fabricated circuits with very good accuracy.

SCEPTRE is available from:

1.) Motorola, Palo Verde

2.) University Computing Corporation

3.) LSS

Figure 3 shows a circuit diagram prepared in the recommended manner.

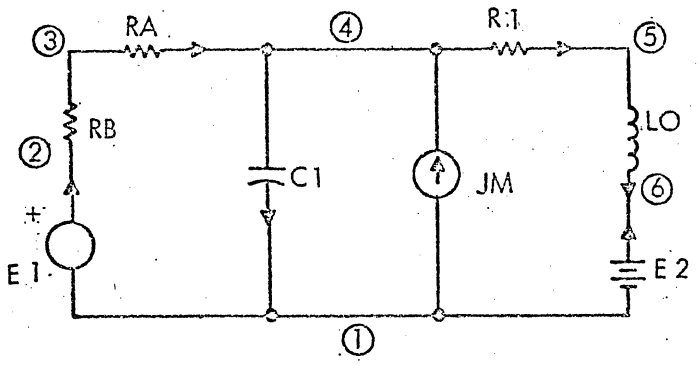


Figure 3. Circuit in SCEPTRE Form

2.2 PREPARING THE SCEPTRE INPUT DATA

The SCEPTRE circuit description language is a structured free-format language, the syntax of which is easy to learn and remember. The language consists of descriptive statements constructed syntactically from user-derived component names, parameter names, node names, and value specifications. These are delimited by special characters such as comma, dash, parenthesis, and equal sign; thereby, allowing the program to interpret the statements properly. Thus, the statements themselves can be punched anywhere on the input data card (columns 1-72) with any desired spacing. In general, several complete statements can be punched on a card separated only by a comma. The rules for continuing a statement from one card to another generally require that the discontinuation be made immediately after delimiters, with the delimiter appearing as the last non-blank character on the card.

2.2.1 HEADINGS AND SUBHEADINGS

Networks are described in SCEPTRE language under the following major headings and subheadings regardless of which mode of analysis is desired.

A. MODEL DESCRIPTION (INITIAL, PRINT)
MODEL NAME (PERM or TEMP) (NODE-NODE-....NODE)
(Comment or message cards, if any, up to 11 allowed)

1. ELEMENTS
2. DEFINED PARAMETERS
3. OUTPUTS
4. FUNCTIONS

B. CIRCUIT DESCRIPTION
(Comment or message cards, if any, up to 11 allowed)

1. ELEMENTS
2. DEFINED PARAMETERS
3. OUTPUTS
4. INITIAL CONDITIONS
5. FUNCTIONS
6. RUN CONTROLS

C. RERUN DESCRIPTION (N)
(Comment or message cards, if any, up to 11 allowed)

1. ELEMENTS
2. DEFINED PARAMETERS
3. INITIAL CONDITIONS
4. FUNCTIONS
5. RUN CONTROLS

D. CONTINUE

1. RUN CONTROLS

E. RE-OUTPUT

F. END

The MODEL DESCRIPTION heading is used when it is desired to store one or more models. The MODEL NAME card, comment cards (optional), and any or all of the four subheadings listed can be used for each model for either permanent or temporary storage under the MODEL DESCRIPTION heading. One or more models may be entered under one MODEL DESCRIPTION heading.

The CIRCUIT DESCRIPTION heading is always used when any network is presented for analysis. Any or all of the six subheadings listed under the heading may be used.

The RERUN DESCRIPTION heading is used whenever the rerun feature is exercised. All changes to the master network must appear under this card. Any or all of the five subheadings listed under this heading may be used.

The CONTINUE heading is intended for use only when continued computation is desired after a problem has been originally run. The only subheading permitted under this heading is RUN CONTROLS. The only other heading that may appear together with CONTINUE in a run is END.

The RE-OUTPUT heading is used whenever the user desires output from a previously completed run without repeating that run. No subheadings are permitted under this heading. The only other heading that may appear with RE-OUTPUT is END.

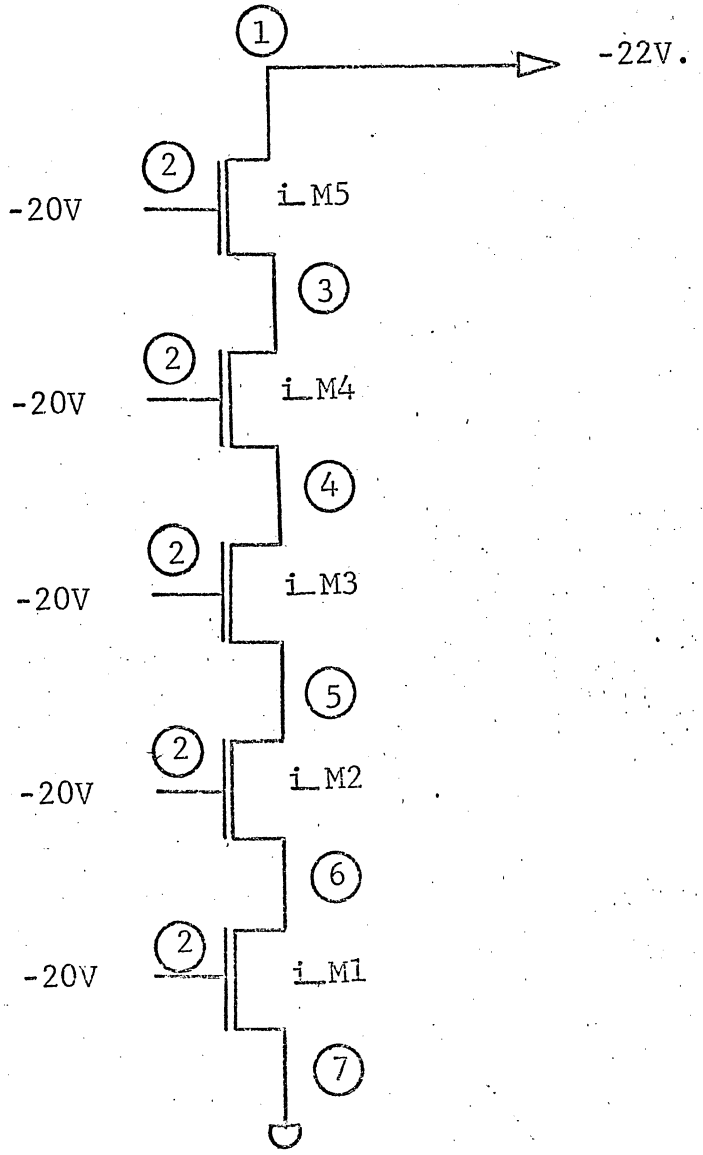
NLDCA is a non-linear dc analysis program. The program is valuable for solving transfer curves and equilibrium conditions of MOS circuits.

The first example shown was run on CSS computer timesharing system. The NLDCA program on CSS requires a simple input of the circuit topology. For MOS the input is simple as illustrated in Example I. The input to the computer and the corresponding output from the computer is listed for the circuit shown in Example I.

The second example shown was run on GE MARK II timesharing system. This version of the NLDCA program is very unsophisticated. The circuit being analyzed has to be described to the NLDCA program by means of a SUBROUTINE FUNCT (N). This subroutine includes process parameters, device ratios and circuit topology. The circuit is described by defining the voltage arrangement of the circuit (ie VGSPI = E2 - V(1)) and by summing the currents (ie x(1), x(2), ...) at each of the N nodes. F(N) is the sum of the currents at node N. In the circuit description, EPS is the maximum convergence error allowed before NLDCA assumes the solution is correct. DELTA is the increment which the node voltages are stepped in making an iteration. N is the number of nodes. V(N) is the voltage at node N.

After a program similiar to LEVEL is written, the written program is merged with NLDCA and ROFCP. ROFCP is a MOS model based on Grove's equation using Wang's four-terminal analysis. The program will solve the circuit described if less than 50 iterations are necessary.

EXAMPLE 1:



7 , 7 , 0 ,

Elements Nodes Model Desc.

C I R C U I T D E S C R I P T I O N

V S 1 , 0 , 2 , (VARIABLE SOURCE)

Initial Node Final Node

V C 1 , 0 , 1 , - 2 2 ,

Initial Node Final Node Value

I M 1 , 7 , 6 , 2 , 0 , P , .4 , .2 ,

S D G B P Channel Z L

```
      END

15.30.05 log *
36.793 CPU SECS, 921 DISK ACCESSES, 0 UNIT RECD OPNS SINCE LOGIN AT 14.56.09
LOGGED OFF AT 15.30.27 ON 06/10/70
#
CSS Online     XRR Qsyosu




1 motcad
PASSWORD:
********
A/C INFO:
vhw
READY AT 15.31.24 ON 06/10/70
CSS.190 04/13/70
TABS?
n

15.31.30 c bill
NONSTANDARD FILETYPE
NEW FILE.
INPUT:
7,7,
vs1,0,2,
vc1,0,1,-22.
im1,7,6,2,0,p,.4,.2
im2,6,5,2,0,p,.4,.2
im3,5,4,2,0,p,.4,.2
im4,4,3,2,0,p,.3@4,.2
im5,3,1,2,0,p,.4,.2

EDIT:
t
p 20
7,7,
VS1,0,2,
VC1,0,1,-22.
IM1,7,6,2,0,P,.4,.2
IM2,6,5,2,0,P,.4,.2
IM3,5,4,2,0,P,.4,.2
IM4,4,3,2,0,P,.4,.2
IM5,3,1,2,0,P,.4,.2
EOF:
file

15.34.14
```

ELEMENTS, NODES, MODELS

```
          nldca bill
EXECUTION:

                    NONLINEAR DC ANALYSIS

DO YOU WISH TO SKIP BRANCH AND NODE PRINT OUT?

MODEL NO.    0   0   0   0   0   0   0
ELEM. TYPE  VS  VC  IM  IM  IM  IM  IM
ELEM. NO.    1   1   1   2   3   4   5
BRANCH NO.   1   2   3   4   5   6   7

MODEL NO.    0   0   0   0   0   0   0
MODEL NODE   1   2   3   4   5   6   7
CKT. NODE    1   2   3   4   5   6   7

PROGRAM CONTROL CHANGES?

ENTER NODE VOLTAGES TO BE PRINTED (UP TO 8)
3,4,5,6,7,
ENTER BRANCH VOLTAGES TO BE PRINTED (UP TO 9)

ENTER BRANCH CURRENTS TO BE PRINTED (UP TO 9)
3,4,5,6,7,

ENTER VOLTAGES TO BE PLOTTED (UP TO 3)


ENTER VOLTAGES TO BE PLOTTED LATER (UP TO 10)


ENTER INPUT0,DELIN,NP,SOLVBACK
-20,0,1,
IT      INPUT VS      V3            V4            V5            V6            V7
          IM1           IM2           IM3           IM4           IM5

IT=  25
```

```
IT=  50
ANY MORE ITERATIONS?
50,

IT= 100
ANY MORE ITERATIONS?

IF YOU WISH TO RETURN TO THE LAST POINT WITH A NEW DVIN:

ENTER DELIN,NP,SOLVBACK

NEW ANALYSIS WITH NEW PARAMETER VALUES?
IF SO,ENTER BRANCH NO.AND NEW PARAMETER VALUE,
ONE SET AT A TIME
?

IIHC0021 STOP      0

15.41.11 c bill
NONSTANDARD FILETYPE
EDIT:
p
7,7,
o 8
8,7,
b
IM5,3,1,2,0,P,.4,.2
i rr1,7,0,10000.
file

15.42.51 nldca bill
EXECUTION:

                    NONLINEAR DC ANALYSIS

DO YOU WISH TO SKIP BRANCH AND NODE PRINT OUT?

MODEL NO.    0  0  0  0  0  0  0  0
ELEM. TYPE VS VC RR IM IM IM IM IM
ELEM. NO.    1  1  1  1  2  3  4  5
BRANCH NO.   1  2  3  4  5  6  7  8

MODEL NO.    0  0  0  0  0  0  0
MODEL NODE   1  2  3  4  5  6  7
CKT. NODE    1  2  3  4  5  6  7

PROGRAM CONTROL CHANGES?

ENTER NODE VOLTAGES TO BE PRINTED (UP TO 8)
3,4,5,6,7,
ENTER BRANCH VOLTAGES TO BE PRINTED (UP TO 9)
ENTER BRANCH CURRENTS TO BE PRINTED (UP TO 9)
4,5,6,7,8,

ENTER VOLTAGES TO BE PLOTTED (UP TO 3)

ENTER VOLTAGES TO BE PLOTTED
```

```
 ENTER INPUTO,DELIN,NP,SOLVBACK
 -20,0,1,
 IT      INPUT VS        V3              V4              V5              V6              V7
           IM1             IM2             IM3             IM4             IM5
   8  -2.0000D 01  -1.3509D 01  -1.3238D 01  -1.2961D 01  -1.2727D 01  -1.2520D 01
       1.2520D-03   1.2520D-03   1.2520D-03   1.2520D-03   1.2520D-03

 ENTER DELIN,NP,SOLVBACK

 NEW ANALYSIS WITH NEW PARAMETER VALUES?
 IF SO,ENTER BRANCH NO.AND NEW PARAMETER VALUE,
 ONE SET AT A TIME
 ?
 3,1e5,
 ?

 PROGRAM CONTROL CHANGES?

 ENTER NODE VOLTAGES TO BE PRINTED (UP TO 8)
 3,4,5,6,7,
 ENTER BRANCH VOLTAGES TO BE PRINTED (UP TO 9)

 ENTER BRANCH CURRENTS TO BE PRINTED (UP TO 9)
 1,4,5,6,7,8,

 ENTER VOLTAGES TO BE PLOTTED (UP TO 3)

 ENTER VOLTAGES TO BE PLOTTED LATER (UP TO 10)

 ENTER INPUTO,DELIN,NP,SOLVBACK
 -20,0,1,
 IT      INPUT VS        V3              V4              V5              V6              V7
           IVS1            IM1             IM2             IM3             IM4             IM5
   6  -2.0000D 01  -1.4151D 01  -1.4032D 01  -1.3941D 01  -1.3865D 01  -1.3797D 01
       4.2487D-13   1.3797D-04   1.3797D-04   1.3797D-04   1.3797D-04   1.3797D-04

 ENTER DELIN,NP,SOLVBACK

 NEW ANALYSIS WITH NEW PARAMETER VALUES?
 IF SO,ENTER BRANCH NO.AND NEW PARAMETER VALUE,
 ONE SET AT A TIME
 ?
 3,1e7,
 ?

 PROGRAM CONTROL CHANGES?

 ENTER NODE VOLTAGES TO BE PRINTED (UP TO 8)
 3,4,5,6,7,
 ENTER BRANCH VOLTAGES TO BE PRINTED (UP TO 9)

 ENTER BRANCH CURRENTS TO BE PRINTED (UP TO 9)
```

```
 ENTER VOLTAGES TO BE PLOTTED (UP TO 3)

 ENTER VOLTAGES TO BE PLOTTED LATER (UP TO 10)


 ENTER INPUT0,DELIN,NP,SOLVBACK
 -20,0,1,
 IT      INPUT VS      V3            V4            V5            V6            V7
           IM1           IM2           IM3           IM4           IM5
   9  -2.0000D 01  -1.4398D 01  -1.4386D 01  -1.4377D 01  -1.4369D 01  -1.4362D 01
        1.4362D-06    1.4362D-06    1.4362D-06    1.4362D-06    1.4362D-06

 ENTER DELIN,NP,SOLVBACK

 NEW ANALYSIS WITH NEW PARAMETER VALUES?
 IF SO,ENTER BRANCH NO.AND NEW PARAMETER VALUE,
 ONE SET AT A TIME
 ?
 3,1e10,
 ?

 PROGRAM CONTROL CHANGES?

 ENTER NODE VOLTAGES TO BE PRINTED (UP TO 8)
 3,4,5,6,7,
 ENTER BRANCH VOLTAGES TO BE PRINTED (UP TO 9)

 ENTER BRANCH CURRENTS TO BE PRINTED (UP TO 9)
 4,5,6,7,8,

 ENTER VOLTAGES TO BE PLOTTED (UP TO 3)

 ENTER VOLTAGES TO BE PLOTTED LATER (UP TO 10)


 ENTER INPUT0,DELIN,NP,SOLVBACK
 -20,0,1,
 IT      INPUT VS      V3            V4            V5            V6            V7
           IM1           IM2           IM3           IM4           IM5

 IT=  25
 ANY MORE ITERATIONS?
 50,
  34  -2.0000D 01  -1.4425D 01  -1.4425D 01  -1.4424D 01  -1.4424D 01  -1.4424D 01
        1.4427D-09    1.4427D-09    1.4427D-09    1.4427D-09    1.4427D-09


 ENTER DELIN,NP,SOLVBACK

 NEW ANALYSIS WITH NEW PARAMETER VALUES?
 IF SO,ENTER BRANCH NO.AND NEW PARAMETER VALUE,
 ONE SET AT A TIME
 ?
```

Simul 8

Simulation of logical systems to verify the customer's logic design is a very important engineering requirement. It is also important for the design engineer to provide reasonable logical testing sequences.

Simul8 reads a system description in terms of polycell interconnect, (MAGIC DECK) and converts the system structure and timing information to Simpf format for logical simulation or for test generation and test grading.

The timing diagram simulation is then presented to the customer as verification of functional logic.

The testing sequence is graded to determine if all possible faults are detected.

Sumul8 is available at Motorola Mesa.

LOGIC SIMULATION PROGRAM (PARALLEL FAULTS) "SIMPF"

I. INTRODUCTION

The program SIMPF is set up for the CDC 1700 computer and written to simulate logical networds (combinational or sequential) with or without some fault conditions. It is a flexible program in the sense that it is open for a quite general use. For example, it may be used to simulate a particular circuit where the external inputs (externals) are changed as a function of time, and where any number of gate outputs (and externals) may be monitored to observe circuit performance. The program may also be employed to find out how many of the specified faults are detected at the circuit outputs within a certain amount of time during which the external inputs may change their state several times, according to the user's specification. The way the program will be used, as well as the circuit and fault information, is given on data cards; there are no special instructions necessary for the computer operator.

CHAPTER XV

Computer Aids — Layout Software

Several programs have been written to assist in the graphical design of MOS Integrated Circuits leading to the final goal of artwork from which the circuits will be made.

CAMP

Computer Aided Mask Preparation

This program is the heart of photo artwork production. It has the capability to convert graphical information from cards, magnetic tape, or CRT design into ink plots for error checking or high accuracy Gerber film for the photo reduction process.

The first step is the graphical description of the cell structures. Once stored, a cell structure can be repeatedly positioned wherever the structure is required. Finally the interconnect wiring is described. The entire graphical structure is then converted to Gerber machine language, from which high resolution films are produced.

For further description see the LSI software manual.

MARS

Motorola Automatic Routing System has two functions. (1) It generates a linear string placement of MOS cells automatically by a wire routing algorithm. (2) It automatically interconnects MOS cells placed in rows. These automatic design capabilities take considerable drudgery out of the initial graphical structure of complex integrated circuits.

The initial results of the linear string placement algorithm are then studied, the string is folded, and then each row placement is studied for optimization of wire routing.

When final row placements are determined MAES will automatically interconnect the cells. This initial routing is then studied and optimized resulting in the final chip.

For further description see the LSI software manual.

BLIST

This is a wire routing analysis program. The input to this program is the "Magic" deck describing cell interconnect, and the order of cells in each row.

The program produces a routing analysis indicating the required number of horizontal and verticle routing channels required between each row and at the end of each row. The program also produces a wire routing matrix. This matrix is a visual indicator of which direction a cell must be moved to reduce the length of wire routing.

The engineer uses this program in an iterative approach to optimize cell placement and thereby minimize chip area required for routing.

For further description see the LSI software manual.

PARRAY

This program generates CAMP placement information for Poly cell LSI designs. The input to this program is the "Magic" deck describing the order of cells in each row. The program looks up the semigraphical description of each cell, and places them in rows or columns adjusted to mate buss lines and so that cell input output contacts will be on routing grids.

For further description see the LSI software manual.

P DIGIT, PEDIT

Cell coding, cell placement, and wire routing can all be done on the digitizer, saving timeand reducing errors. The P DIGIT program converts digitizer information into CAMP information. The PEDIT program makes modification of digitized information easy. It also is used to compare the "Magic" deck with digitizer routing information in order to detect errors.

For further description see the LSI software manual.

ATPL System

The Automatic Two Phase Logic system is a complete design software package for design, simulation, and graphical artwork production of medium scale 2 phase logic PMOS systems.

The system has a set of predesigned 2 phase logic and shift register cells. Systems implemented with this logic can then be simulated by Logblosim - the Logical Block Simulator of the ATPL System. System design and implementation is thusly verified.

Signal Trace is the portion of the ATPL system which verifies that no timing errors will occur, by checking that no signal can propagate through more than four cells during one clock phase.

PRF or Place Route Fold is a completely automatic approach to placing cells in a linear string by a wire routing algorithm. The cellular interconnect is then computed. Finally, the linear string is broken at appropriate places, and folded to snake the cell rows back and forth horizontally across the chip.

The plot routing takes graphical information from PRF and generates Geeber language magnetic tape.

The system, however, has a few major weaknesses. (1) It is presently incapable of simulating systems built with other cells. (2) It is incapable of timing analysis at system clock frequencies other than 660 Kc.

(3) PRF can only handle approximately 200 cells including bonding pads.

(4) The plot routine does not allow ink plots previous to Gerber.

This last fault has been circumvented by a link between

PRF and Motorola CAMP.

For further information call Murray Goldman.

ASRD

The Automatic Shift Register Designer automatically generates CAMP placement and routing information for any N x M static, Ratio Dynamic, or Ratioless Dynamic 2 phase shift register ($N \leq 8$).

The cells used for this program are predesigned and stored, and are highly optimized to conserve chip area.

The program generates graphical structures as efficiently as is consistant with automation.

CHAPTER XVI

LAYOUT HARDWARE

Design turn-around time can be significantly reduced by effectively utilizing the layout hardware. The digitizer, the CRT, the plotter and the Gerber each significantly reduce turn-around time in preparing photo-artwork from the circuit design.

DIGITIZER

The digitizer is a large drafting board with a movable crosshair. The machine records the X, Y coordinates and the status of several sense switches on IBM punch cards when the operator pushes the "RECORD" button.

All shapes, can be coded into cells, cells into polycells, and polycells can be placed and routed by recording the appropriate coordinates onto punched cards. The P digit and P edit programs will convert the digitizer card deck to a camp deck ready for input to camp.

CRT

The Control Data 274 is a Cathode Ray tube with a 1744 controller interface to a computer. In conjunction with the "ONLINE" program it is a powerful interactive tool for cell design, cell checkout and chip design. Its chief advantage is the instant visual feedback of correct or incorrect design. Furthermore it directly interfaces with Camp which allows instant visual checking of a chip layout, correction, then return to Camp for plots.

PLOTTER

A plotter is an instrument which reads magnetic tape and records graphical information in multicolor ink.

This plot is used to check any portion of the chip design and to provide a permanent record verifying the design.

GERBER

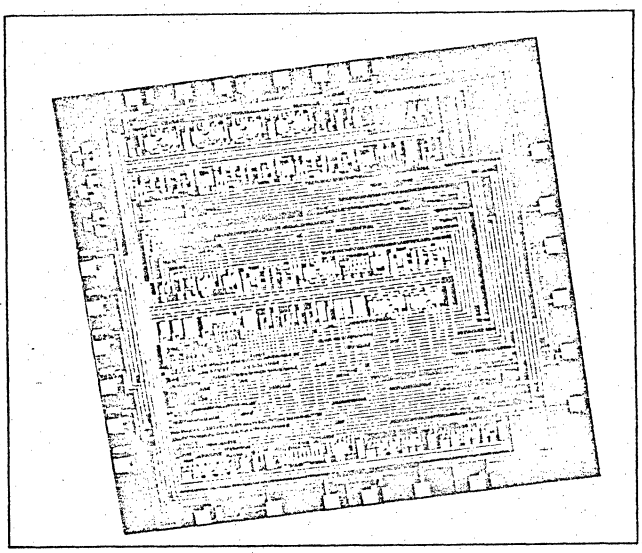
The Gerber machine is a high accuracy photo-graphic artwork generator. It eliminates the need for cutting, peeling and reducing ruby lithiographs. The same card deck which produces the final ink plot is then used to generate a magnetic tape. This tape is read by the Gerber machine which then drives a light with a high accuracy X, Y index on a large table. The lamp exposes high contrast film. The final product is a 100X film which is then used for photo reduction.

CHAPTER XVII

COMPUTER AIDS - CELL LIBRARY

The development of a large area, high density MOS chip fabrication technology makes LSI possible today. The Motorola Polycell LSI System provides the design capability that makes LSI practical as well.

The ability to quickly and economically reduce custom circuit requirements to working chips is the key to LSI. This is the role of the Polycell LSI System. Starting with equipment design specifications, the Motorola Polycell LSI System is used to produce the photomask artwork for circuit fabrication and to control the final testing of the finished chips.



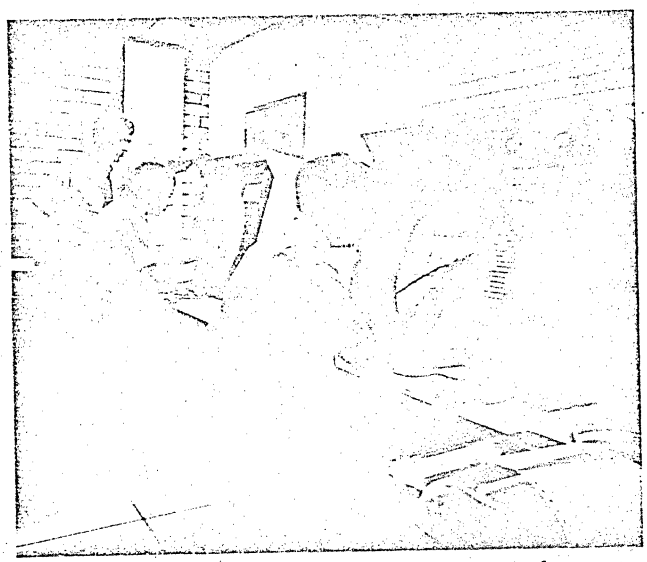
Photomicrograph of an MOS array designed with the Polycell LSI System and fabricated on a high-volume Motorola production line.

The Polycell LSI System is the result of Motorola's application of advanced Computer-Aided Design (CAD) techniques to integrated circuit design, fabrication, and testing. Design Automation programs and man-machine interaction are combined in this system to provide maximum flexibility, speed and economy.

The heart of this system is a library of MOS P-channel logic cells, self-contained units for performing logic functions. The electrical performance of each cell, consisting of a number of interconnected

components, has been characterized. The fact that these cells are handled as units greatly expedites the entire design procedure.

The Polycell LSI System is part of a total capability that has been integrated with an advanced and carefully controlled manufacturing operation. Backed by years of accumulated experience in the manufacture of reliable, complex integrated circuits, this total capability provides for the complete and efficient development of prototypes and the manufacture of production quantity custom MOS-LSI circuits.



The Polycell LSI System employs an imposing array of computer equipment such as these interactive CRT terminals.

Discussed within this manual are the following topics: Operation of the Polycell LSI System, the Design Interface between Customer and Motorola, MOS Technology, Manufacturing, Logic Symbology and Packaging. The final section contains a customer information sheet that is the first step toward utilizing Motorola's Polycell LSI System for your applications.

The MOS Polycell is a logical function, designed to be placed side by side in rows, and interconnected to reduce total design time.

The MH series of cells are High Threshold, high power, static logic cells. They are generally 10 mils or 12 mils high and a multiple of 1.2 mils wide. Input-output contacts are at the bottom on both P diffusion and metal, and power lines at the top: V_{DD}, V_{GG}, Ground.

The ML series of cells are High Threshold Low power static logic cells. They are generally 8 mils high and a multiple of 1.2 mils wide. They are fully compatible with the MH series.

The MS series is a set of string two phase shift registers. Their busslines are not compatible with other cells, however, the cells do fit the same routing grid, and guarantee compatible logic levels.

MH01FP	FIELD PLATE DIODE	2.4	10.0
MH01IN	INVERTER	2.4	10.0
MH02PS	TWO INPUT NOR	3.6	10.0
MH03PS	THREE INPUT NOR	4.8	10.0
MH04PS	FOUR INPUT NOR	6.0	10.0
MH05PS	FIVE INPUT NOR	7.2	10.0
MH06PS	SIX INPUT NOR	8.4	10.0
MH07PS	SEVEN INPUT NOR	9.6	10.0
MH08PS	EIGHT INPUT NOR	10.8	10.0
MH02SS	TWO INPUT NAND	3.6	10.0
MH03SS	THREE INPUT NAND	4.8	10.0
MH01FG	Z=/(A1.A2+B1.B2)	6.0	10.0
MH02FG	Z=/((B1+B2).(A1+A2))	6.0	10.0
MH03FG	Z=/(A1.A2+B)	4.8	10.0
MH04FG	Z=/(A1.A2+B1+B2)	6.0	10.0
MH05FG	Z=/(A1+A2+A3)(B1+B2+B3	8.4	10.0
MH06FG	MULTIPLEX SWITCH	6.0	10.0
MH07FG	Z=/((A1+A2).A3)	4.8	10.0
MH08FG	Z=/((A1.A2.A3)+(B1.B2.	8.4	10.0
MH09FG	Z=/((A1+A2+A3).A4)	6.0	10.0
MH10FG	Z=/((A1+A2+A3+A4).A5)	7.2	10.0
MH010S	800 NS ONE SHOT	8.4	10.0
MH12FG	Z=/((A1+A2+A3+A4+A5+A6	9.6	10.0
MH13FG	Z=/((A1+A2).(A3+A4+A5)	7.2	10.0
MH14FG	Z=/((A1+A2).(A3+A4+A5+	8.4	10.0
MH15FG	Z=/((A1+A2+A3).(A4+A5+	9.6	10.0
MH01EO	EXCLUSIVE OR	6.0	10.0
MH01EN	EXCLUSIVE NOR	7.2	10.0
MH01FA	FULL ADDER	15.6	10.0
MH010S	500 NS ONE SHOT	10.8	10.0
MH01ID	INVERTER BUFFER	2.4	10.0
MH01CD	CLOCK DRIVER	2.4	10.0
MH02CD	BOOTSTRAP CLOCK DRIVER	3.6	10.0
MH01PP	PUSH PULL BUFFER	6.0	10.0
MH02PP	PUSH PULL BUFFER	7.2	10.0

'H01LH	R S LATCH	3.6	10.0
'H02LH	R S LATCH	4.8	10.0
'H01CL	CLOCKED RS LATCH	6.0	10.0
'H02CL	CLOCKED RS LATCH	7.2	10.0
'H01JK	MASTER SLAVE JK FF	24.0	10.0
'H02JK	LOW POWER JK	9.6	10.0
'H01RS	RS MASTER SLAVE FF	24.0	10.0
'H01WR	1 INPUT NOR EXPANDER	2.4	10.0
'H02WR	2 INPUT NOR EXPANDER	3.6	10.0
'H02WD	2 INPUT NAND EXPANDER	3.6	10.0
'H01SP	WURLITZER SPECIAL	14.4	8.0
'H02SP	WURLITZER SPECIAL	8.4	8.0
'H03SP	WURLITZER SPECIAL	16.8	8.0
'H04SP	WURLITZER SPECIAL	16.8	8.0
'H05SP	WURLITZER SPECIAL	18.0	8.0
'H06SP	WURLITZER SPECIAL	8.4	8.0
'H01WB	VIATRON CARRY FF	12.0	18.0
'H02WB	VIATRON CARRY FF	12.0	15.6

NAME	DESCRIPTION	SIZE	
LL03PS	LOW POWER 3 NOR	8.4	10.0
LL01IN	LOW POWER INVERTER	2.4	8.0
LL02PS	LOW POWER NOR	3.6	8.0
LL04SS	LOW POWER 4 NAND	6.0	8.0
LL03XS	LOW POWER NOR	4.8	8.0
LL04PS	LOW POWER NOR	6.0	8.0
LL05PS	LOW POWER NOR	7.2	8.0
LL06PS	LOW POWER NOR	8.4	8.0
LL07PS	LOW POWER NOR	9.6	8.0
LL08PS	LOW POWER NOR	10.8	8.0
LL02SS	LOW POWER NAND	3.6	8.0
LL03SS	LOW POWER NAND	4.8	8.0
LL01FG	Z=/(A1.A2.+B1.B2)	6.0	8.0
LL02FG	Z=/((B1+B2).(A1+A2))	6.0	8.0
LL03FG	Z=/(A1.A2+B)	4.8	8.0
LL04FG	Z=/(A1.A2+B1+B2)	6.0	8.0
LL05FG	Z=/((A1+A2+A3).(B1+B2+	8.4	8.0
LL07FG	Z=/((A1+A2).A3)	4.8	8.0
LL08FG	Z=/((A1.A2.A3)+(B1.B2.	8.4	8.0
LL09FG	Z=/((A1+A2+A3).A4)	6.0	8.0
LL10FG	Z=/((A1+A2+A3+A4).A5)	7.2	8.0
LL11FG	Z=/((A1+A2+A3+A4+A5).A	8.4	8.0
LL12FG	Z=/((A1+A2+A3+A4+A5+A6	9.6	8.0
LL13FG	Z=/((A1+A2).(A3+A4+A5)	7.2	8.0
LL14FG	Z=/((A1+A2).(A3+A4+A5+	8.4	8.0
LL15FG	Z=/((A1+A2+A3).(A4+A5+	9.6	8.0
LL01EO	LOW POWER EXCL. OR	6.0	8.0
LL01EN	LOW POWER EXCL. NOR	6.0	8.0

NAME	DESCRIPTION	SIZE	
MS01SR	PHI PRIME GEN	4.8	9.0
MS02SR	INPUT BIT STATIC SR	6.0	9.0
MS03SR	STND BIT STATIC SR	4.8	9.0
MS04SR	ON CHIP BUF STATIC SR	4.8	9.0
MS05SR	OFF CHIP BUF STATIC SR	20.4	9.0
MS01RD	INPUT BIT RATIO DYNAMI	4.8	8.0
MS02RD	STND BIT RD SR	4.8	8.0
MS03RD	OUTPUT BUF RD SR	12.0	8.0
MS01RL	INPUT BIT RATIOLESS DY	7.2	5.0
MS02RL	STND BIT RATIOLESS SR	6.0	5.0
MS03RL	ON CHIP BUF RATIOLESS	6.0	8.0
MS04RL	OFF CHIP BUF RATIOLESS	16.8	8.0

CHAPTER XVIII

PACKAGES

XI. Packages

A. Package Catalog

B. Bonding Diagrams

C. Assembly Sheets

Package Limitations

There are three basic packaging limitations:

1. Number of pins
2. Maximum chip size
3. Thermal Impedance

The number of pins on a given package is an immediate limitation to the number of signals and power leads which can be brought in and out of a chip. An example chip might require 6 output leads, 10 input leads, and 3 power leads, or 19 pins. However a simple coding and decoding scheme can reduce the 10 input leads to 7, and then be decoded on the chip. This would allow use of a 16 pin package. Circuits with pin requirements other than those in the standard package table are available on request.

The maximum chip size which can be placed in a given package is a limitation on the complexity of the logic. For example the 16 pin white ceramic package can handle a 130 x 160 mil chip. A typical chip this size might have 140 logic cells, depending on the area required to interconnect the cells. A more complex logic function will require a larger chip and more pins, and therefore a larger package.

Thermal impedance is another limitation. Chip temperature should never be above 150°C. For some logical state, the chip dissipates its maximum power. This heat is dissipated to the ambient heat sink through the thermal impedance

of the package. However, the package thermal impedance varies significantly with mounting techniques. (See Thermal Impedance)

Package costs alone often exceed more than half the total cost of producing finished MOS Integrated Circuits.

Higher finished-device yields can be obtained by designing circuits to conform, where possible, to standard packages having known characteristics.

The seven packages listed will meet a variety of packaging requirements. For some applications, however, packages with a greater number of pins are required. In addition, some equipment manufacturers prefer packages other than the standard types listed. Motorola is prepared to employ other package types as required. However, special package requirements should be discussed in the initial stages of negotiation.

This approach will not only provide time to obtain the quantities of standard packages required, but will also permit new and different packages to be developed where needed.

Basic Assembly Operations

Although the package used may vary from circuit to circuit the basic operations necessary to assemble an I/C are:

a. Wafer probe

b. Scribe and break the wafer

c. Hi-Power inspection of die

d. Die bond and inspection

e. Wire bond and inspection

f. Seal and inspection

(The mechanical, environmental, and final test specifications normally vary greatly from device to device.)

All Motorola MOS devices currently made employ as "standard operations" gold-silicon eutectic die-bonding, aluminum ultrasonic wire bonding, and gold-tin solder sealing. (Solder-glass packages and plastic packages are available but not recommended for Motorola MOS circuits as they are processed at this time.) (The thermal characteristics discussed in the next section were based on devices assembled utilizing the "standard operations" previously mentioned.)

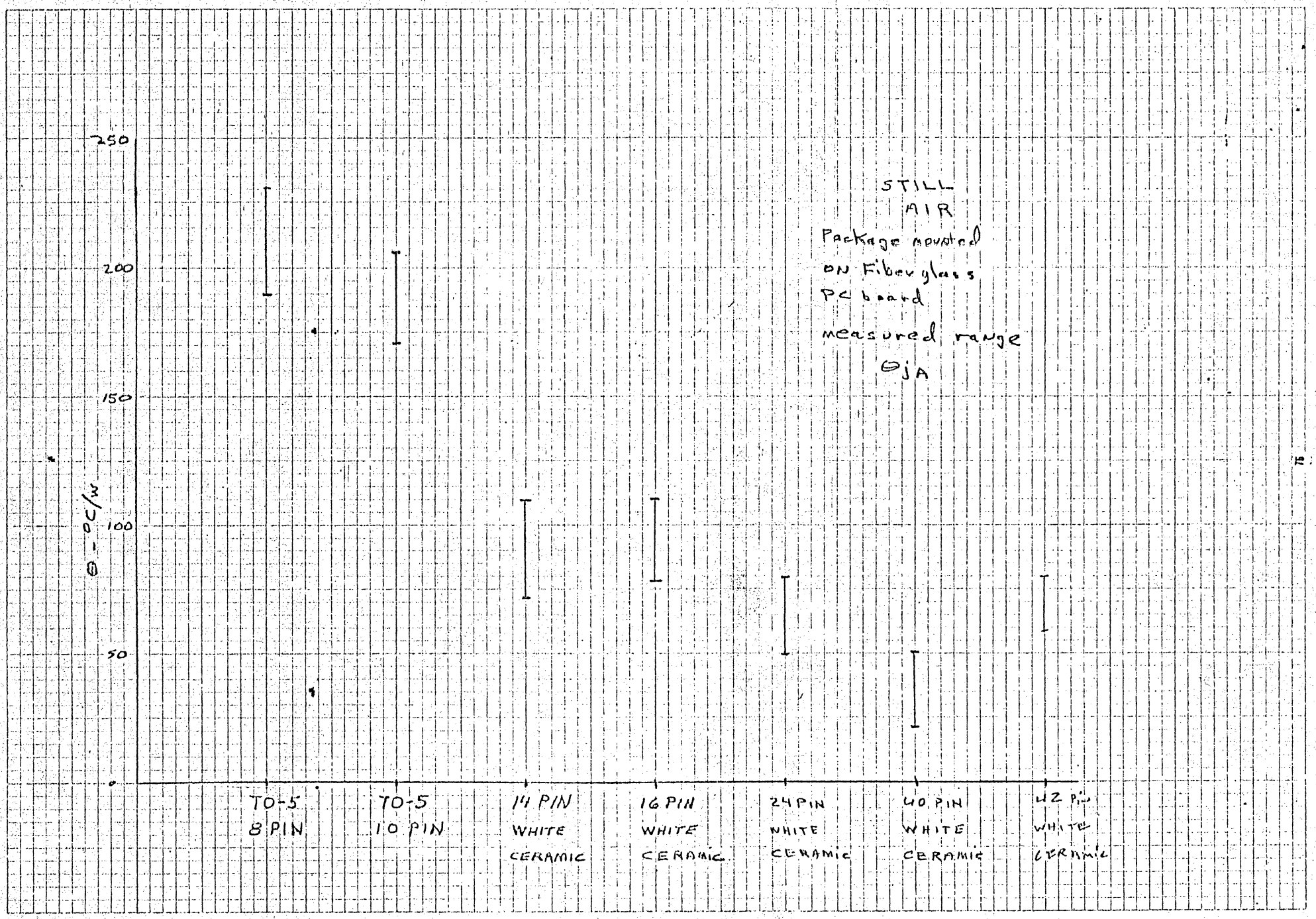
Thermal Impedance

The thermal impedance, θ, determines the difference between the chip temperature and ambient temperature by the formula:

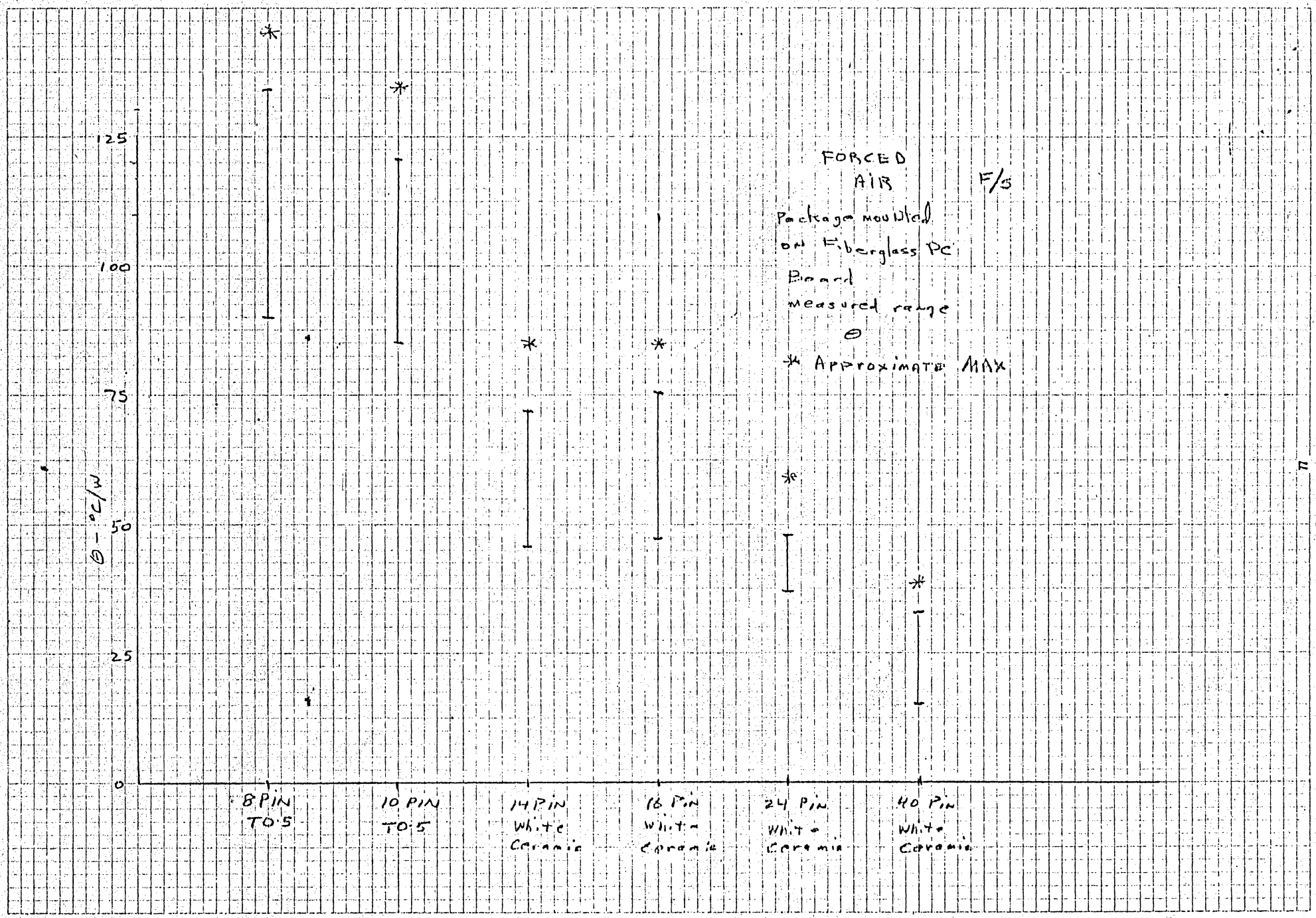
$$T_{chip} - T_{sink} = Power \cdot \theta$$

Chip temperature should not be above 150°C., when the logic state dissipates maximum power. The thermal impedance of the package varies with mounting techniques, however. For example a 16 pin package in still air has a θ of °C/watt. (See figs.1,2,3) For a given mounting technique, the ambient sink temperature must be low enough that the chip temperature is not above 150°C:

$$T_{sink}\ ^{\circ}C \leq 150 - Power_{(max)} \cdot \theta$$

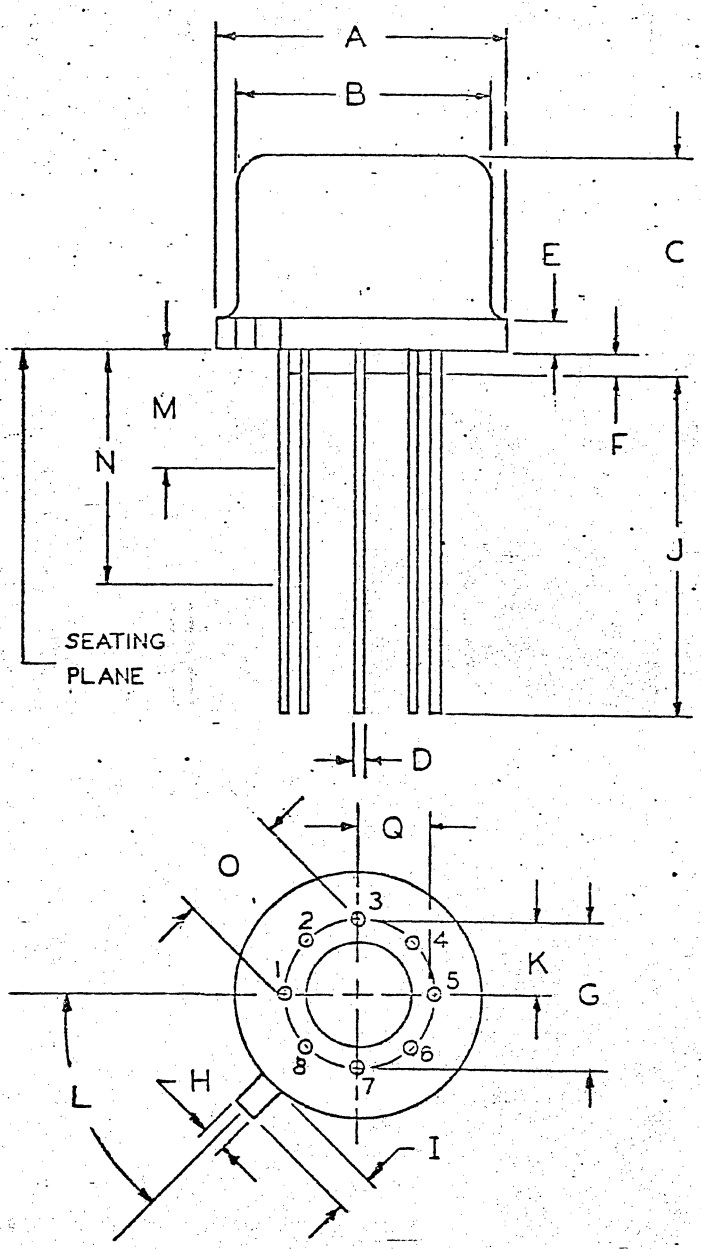

STILL
AIR
Package mounted
on Fiberglass
PC board
measured range
θJA
250
200
150
100
50
0
θ - °C/W
TO-5
8 PIN
TO-5
10 PIN
14 PIN
WHITE
CERAMIC
16 PIN
WHITE
CERAMIC
24 PIN
WHITE
CERAMIC
40 PIN
WHITE
CERAMIC
42 PIN
WHITE
CERAMIC

ALUMINUM HEAT SINK
DOW CORNING THERMAL GREASE
MEASURED RANGE @ 1C
* APPROXIMATE MAX
100
75
50
25
8 PIN TO5
10 PIN TO5
14 PIN WHITE CERAMIC
16 PIN WHITE CERAMIC
24 PIN WHITE CERAMIC
40 PIN WHITE CERAMIC



8 PIN T.O.5	MECHANICAL OUTLINES DICTIONARY
DO NOT SCALE	DATE

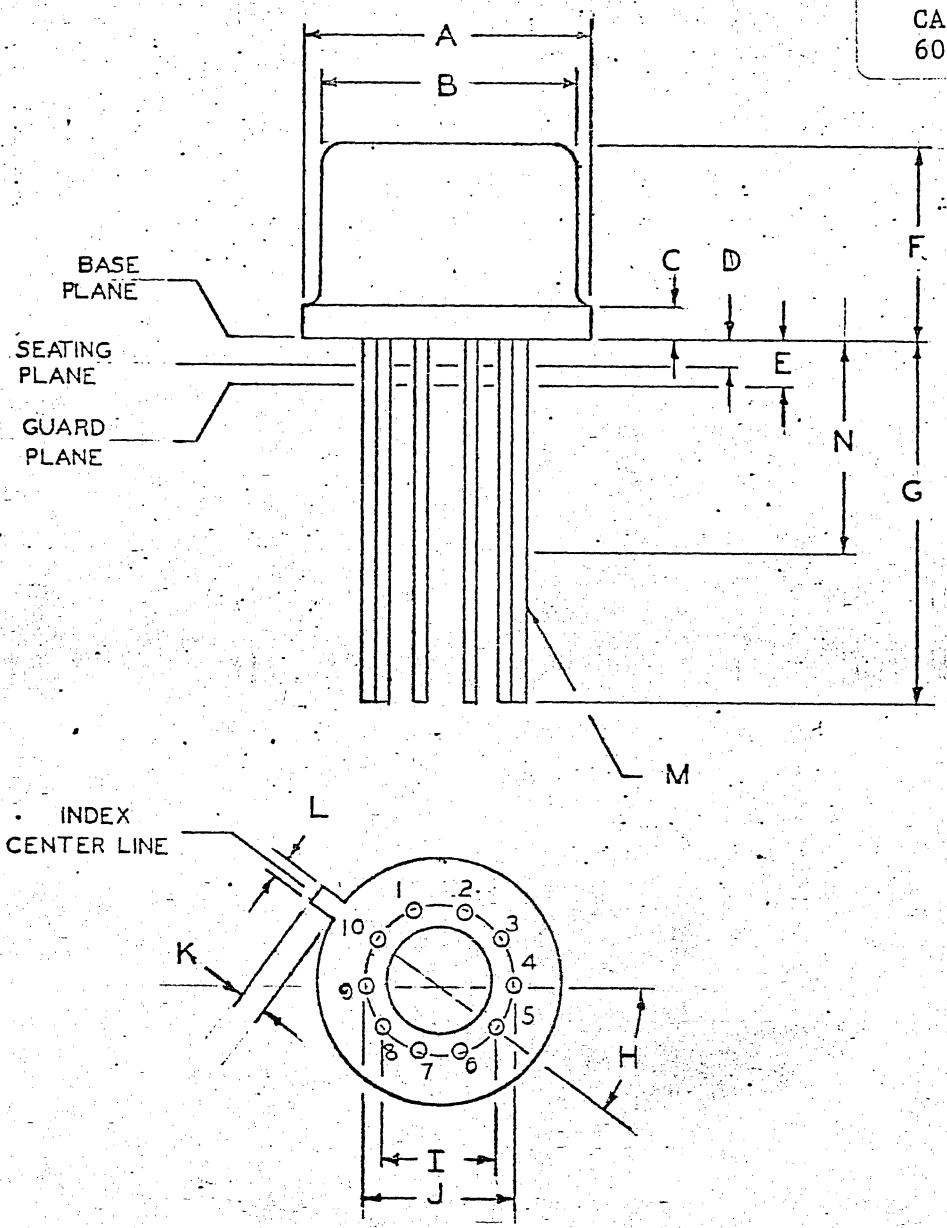
CASE 619-02
601 (TO-99)



DIM	INCHES	NOMINAL	DIM	INCHES	NOMINAL
A	0.350		J	0.500	MIN.
B	0.320		K	0.100	T.P.
C	0.250		L	45°	T.P.
D	0.018		M	0.050	MAX.
E	0.040	MAX.	N	0.250	MIN.
F	0.025	NO standoff preferred	O	0.150	— —
G	0.200	T.P.	P		
H	0.031		Q		
I	0.037		R		XVIII-9

10 PIN T.O. 5	MECHANICAL OUTLINES DICTIONARY
DO NOT SCALE	DATE

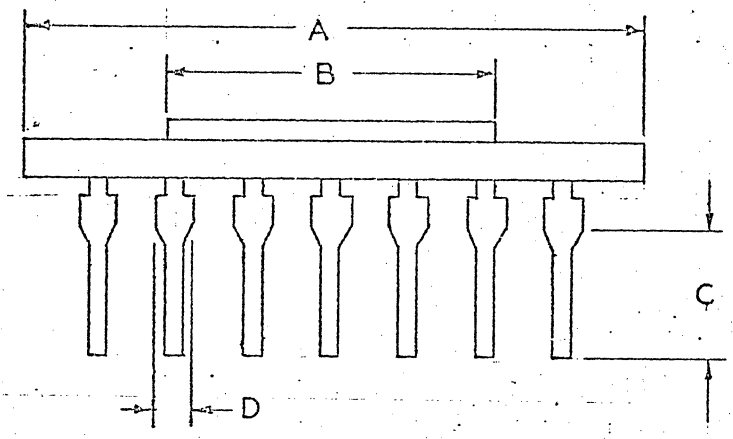
CASE 602-A
603 (T0100)

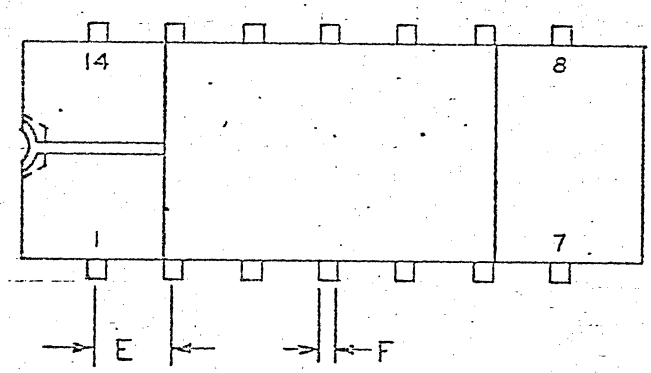


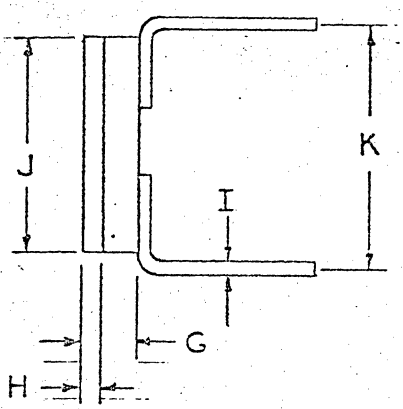
DIM	INCHES	NOMINAL	DIM	INCHES	NOMINAL
A	0.350		J	0.230	T.P.
B	0.320		K	0.037	
C	0.040	MAX.	L	0.030	
D	0.030	prefer no standoff	M	0.019	
E	0.050	MAX.	N	0.375	
F	0.170		O		
G	0.500	MIN.	P		
H	36°	T.P.	Q		
I	0.150		R		

14 PIN WHITE CERAMIC	MECHANICAL OUTLINES DICTIONARY
DO NOT SCALE	DATE

CASE 637





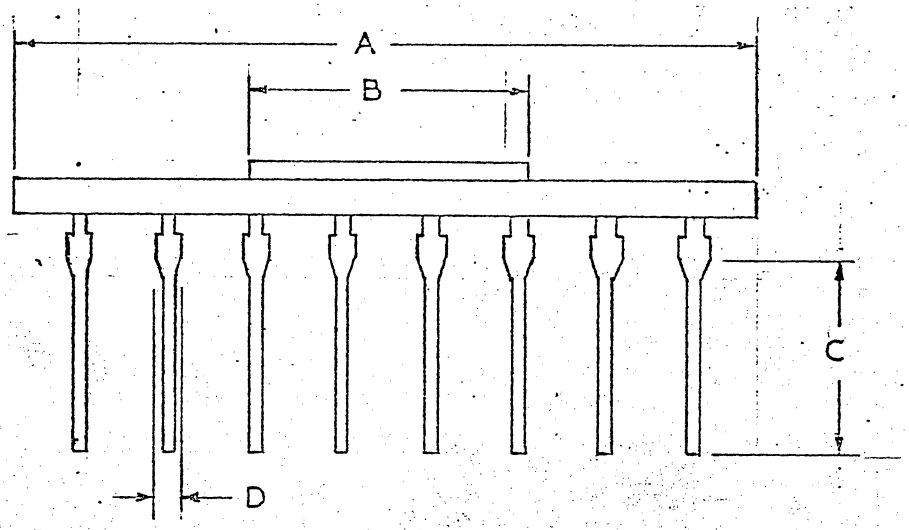


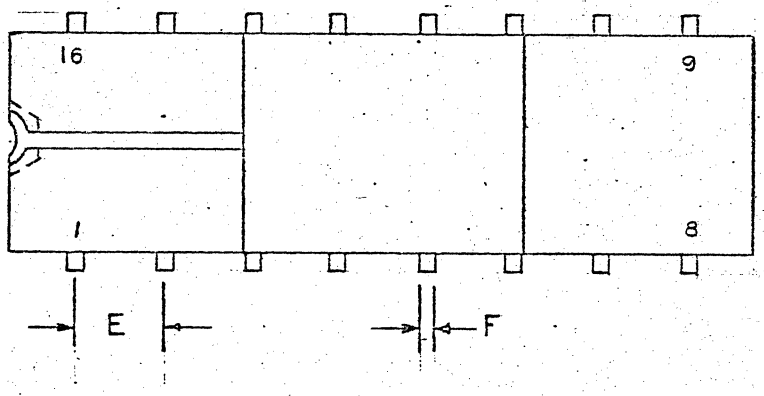
DIM	INCHES	NOMINAL
A	0.740	
B	0.400	
C	0.160	TYP.
D	0.048	
E	0.100	
F	0.017	
G	0.060	
H	0.015	
I	0.010	

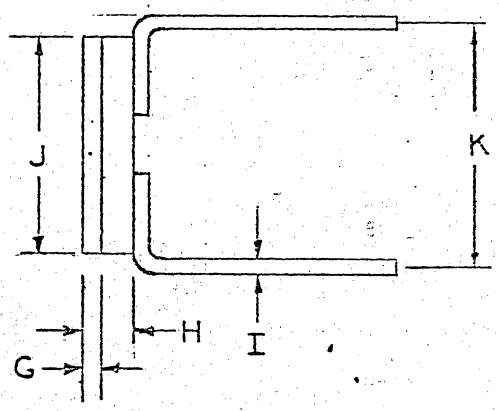
DIM	INCHES	NOMINAL
J	0.275	
K	0.300	REF.
L		
M		
N		
O		
P		
Q		
R		

16 PIN WHITE CERAMIC	MECHANICAL OUTLINES DICTIONARY
DO NOT SCALE	DATE

CASE 638



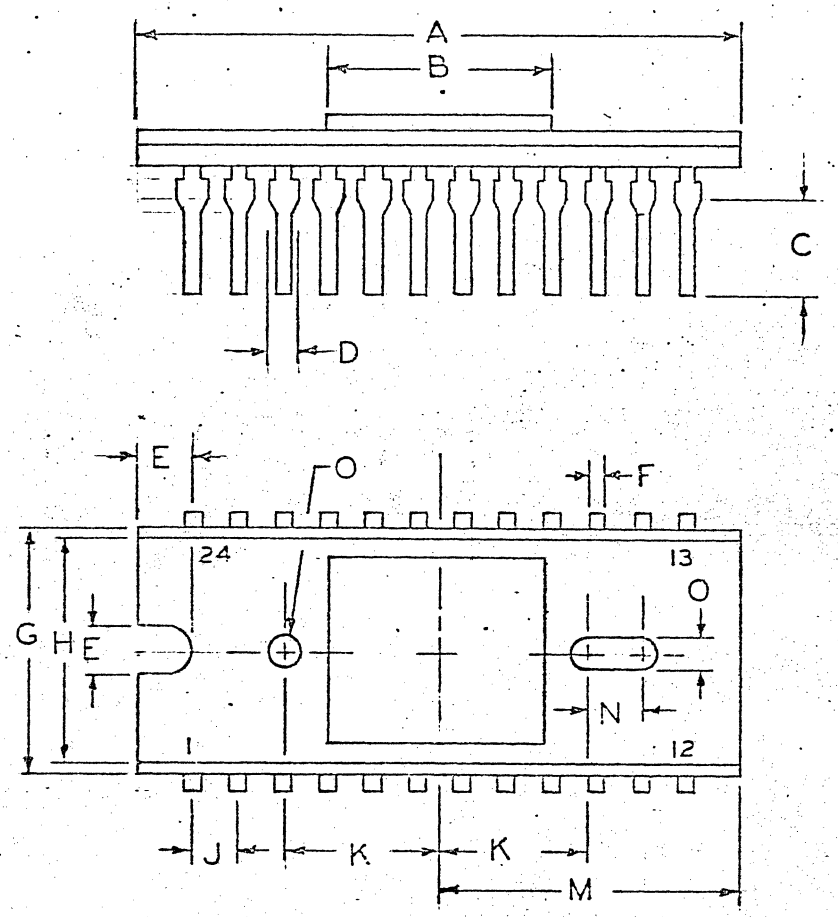




DIM	INCHES	NOMINAL	DIM	INCHES	NOMINAL
A	0.820		J	0.275	
B	0.400		K	0.300	
C	0.160	TYP.	L		
D	0.047		M		
E	0.100		N		
F	0.017		O		
G	0.015		P		
H	0.060		Q		
I	0.010		R		

24 PIN WHITE CERAMIC	MECHANICAL OUTLINES DICTIONARY
DO NOT SCALE	DATE

CASE 635

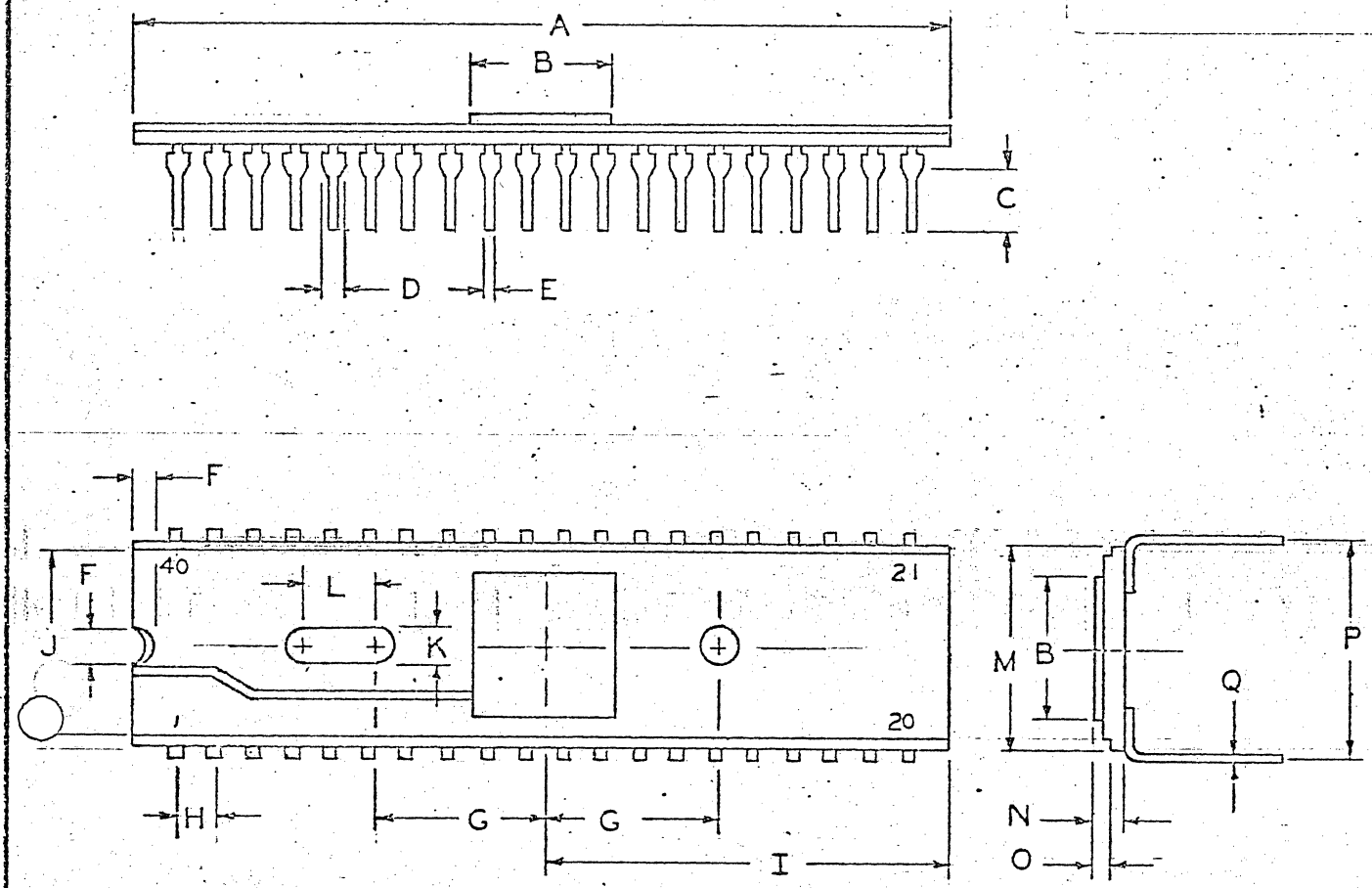


DIM	INCHES	NOMINAL
A	1.170	
B	0.400	
C	0.160	
D	0.030	
E	0.095	
F	0.017	
G	0.500	
H	0.460	
I	0.030	

DIM	INCHES	NOMINAL
J	0.100	TYP.
K	0.300	
L	0.050	
M	0.585	
N	0.125	
O	0.065	---
P	0.010	
Q		
R	0.600	REF. XVIII-92

40 PIN WHITE CERAMIC	MECHANICAL OUTLINES DICTIONARY
DO NOT SCALE	DATE

CASE 639

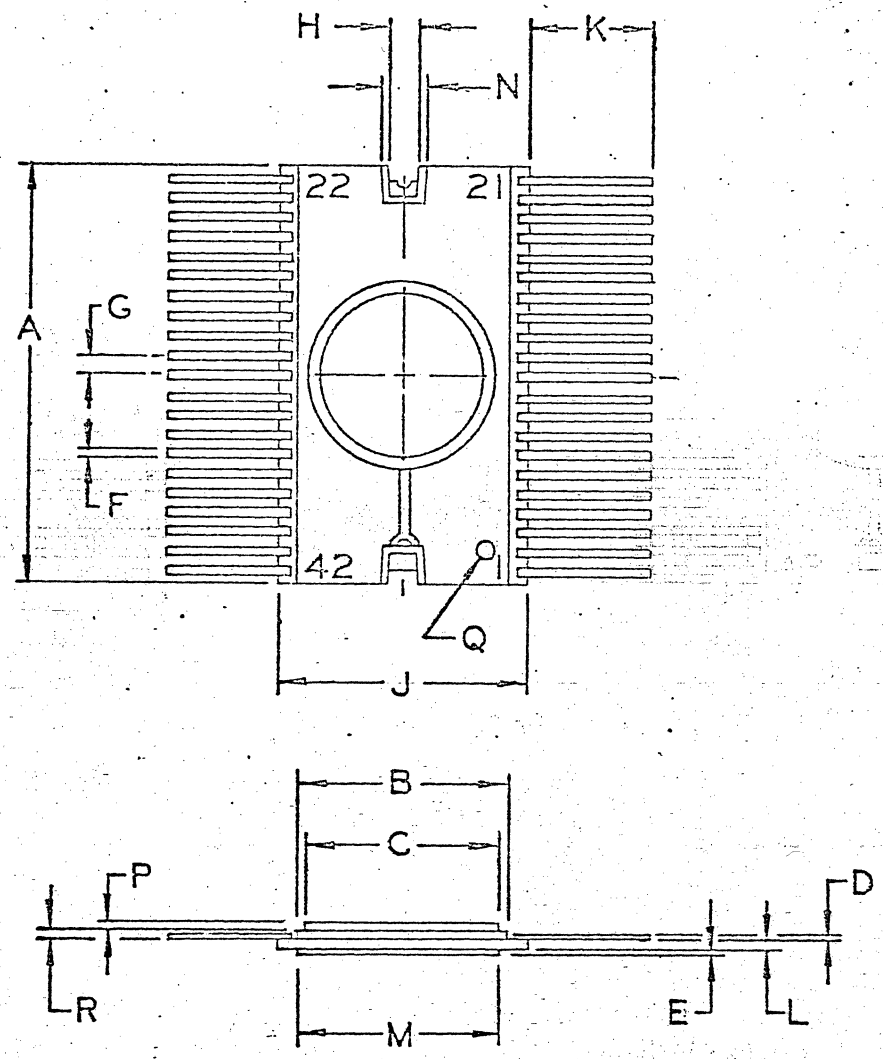


DIM	INCHES	NOMINAL
A	1.970	
B	0.400	
C	0.160	TYP.
D	0.047	
E	0.017	
F	0.097	
G	0.650	
H	0.100	
I	0.985	

DIM	INCHES	NOMINAL
J	0.460	
K	0.065	
L	0.125	
M	0.500	
N	0.060	
O	0.015	
P	0.600	REF.
Q		
R		XVIII-14

42 PIN WHITE CERAMIC	MECHANICAL OUTLINES DICTIONARY
DO NOT SCALE	DATE

CASE 645

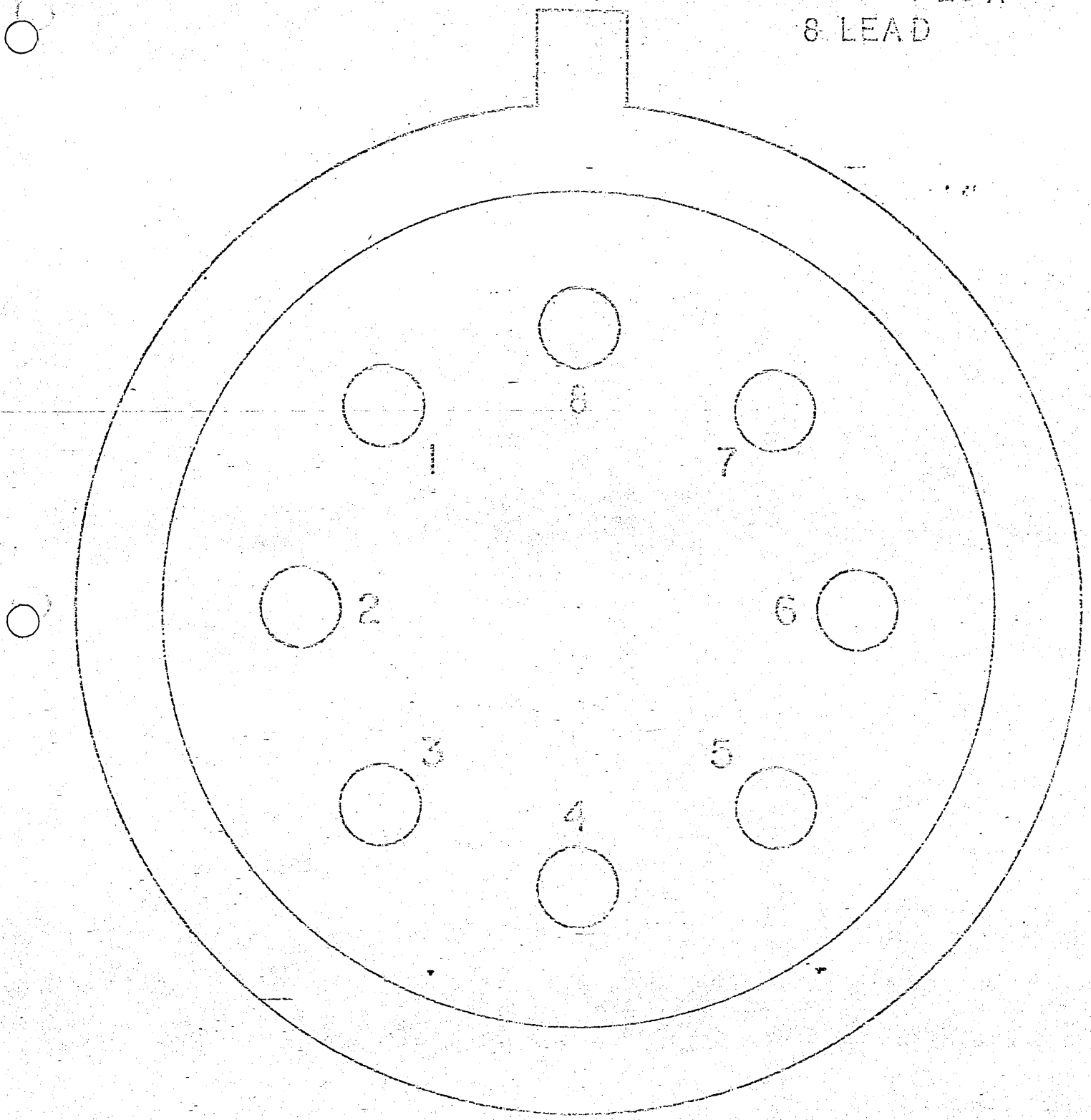


DIM	INCHES	NOMINAL
A	1.060	
B	0.550	
C	0.500	
D	0.010	
E	0.012	
F	0.020	
G	0.050	REF
H	0.080	
I		

DIM	INCHES	NOMINAL
J	0.640	
K	0.290	MIN
L	0.022	
M	0.500	
N	0.010	TYP
O		
P	0.020	
Q	0.050	
R	0.022	XVIII-15

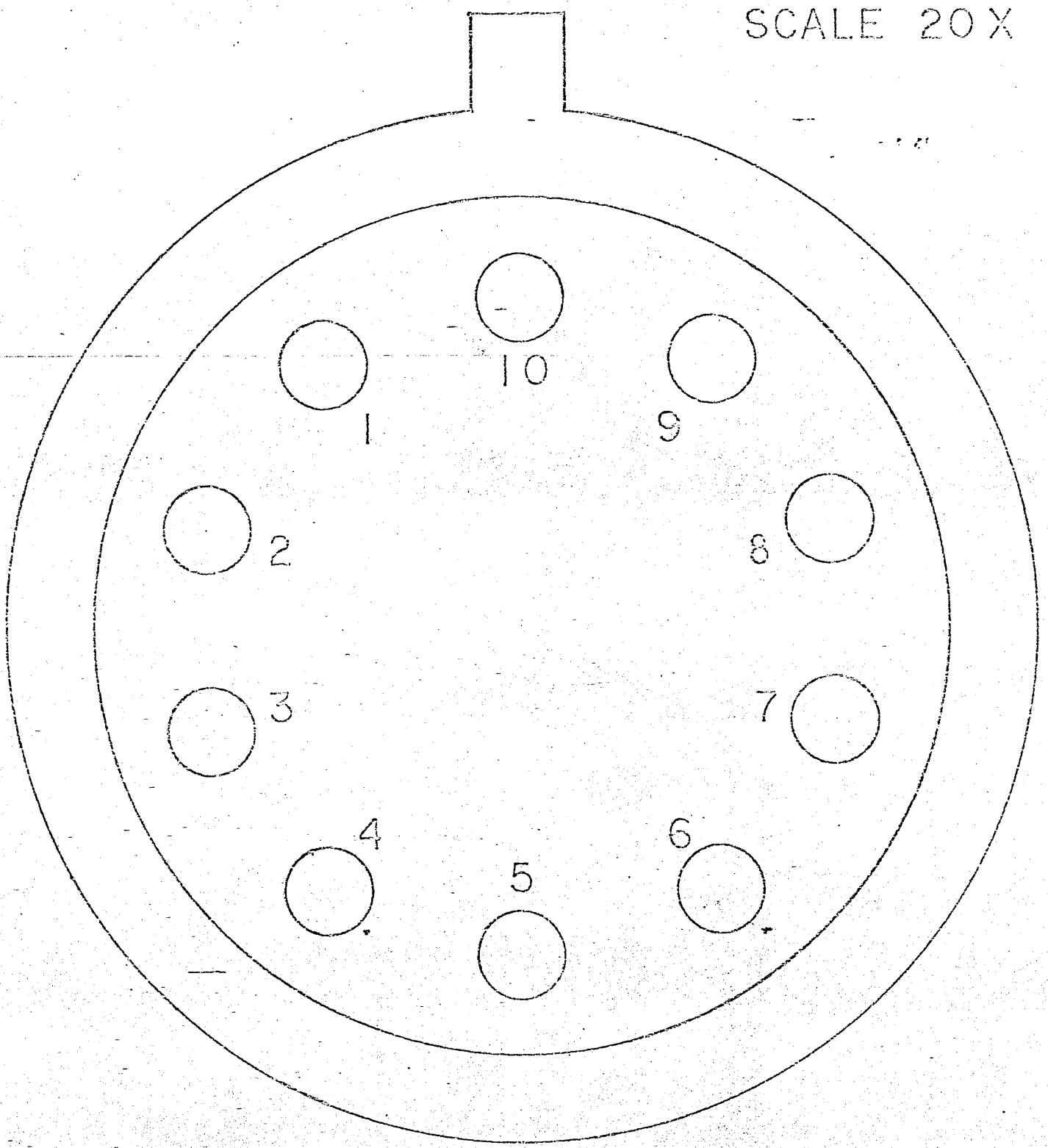
BONDING DIAGRAM

TO-5
SCALE: 20X
8 LEAD

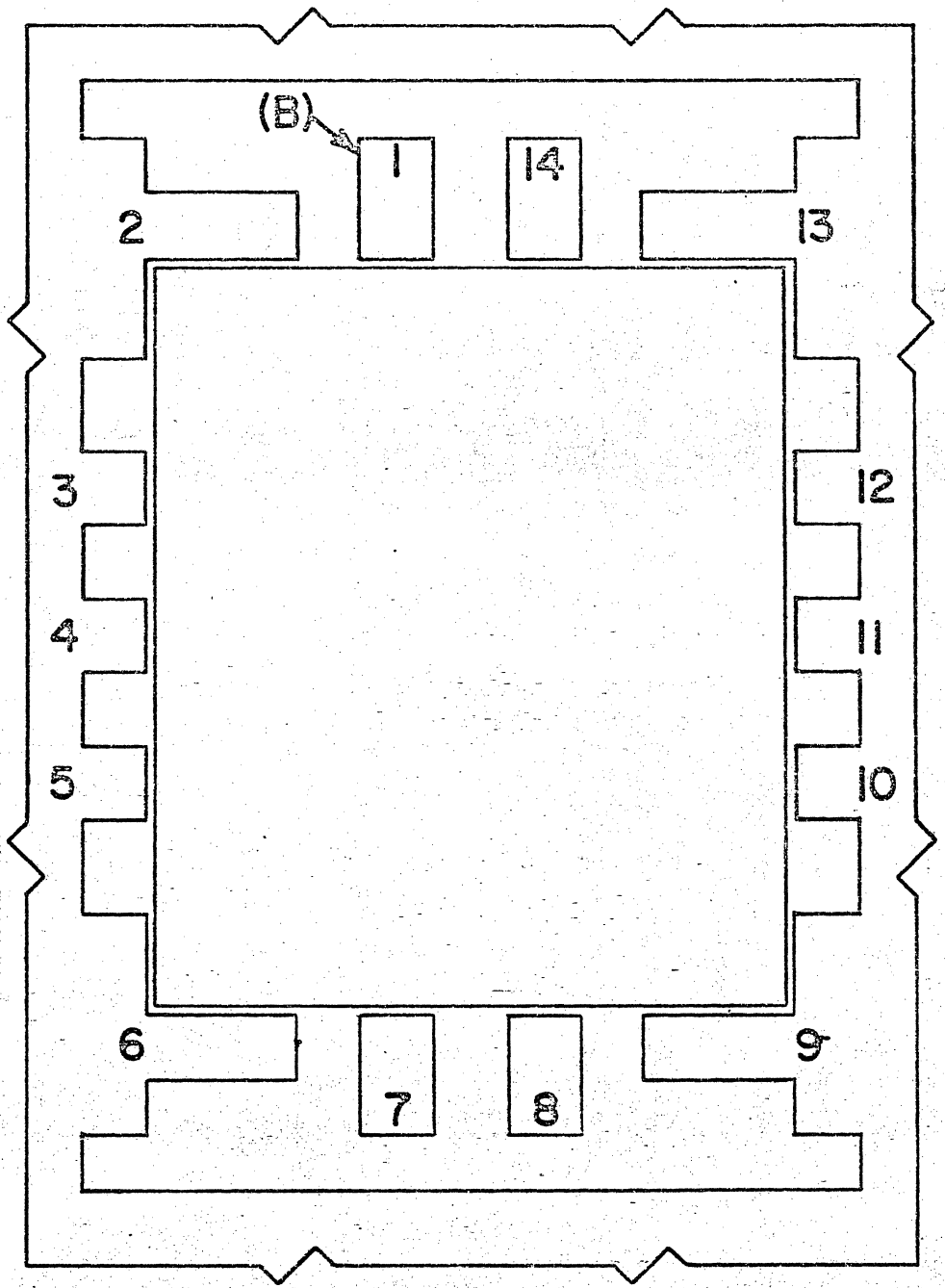


BONDING DIAGRAM

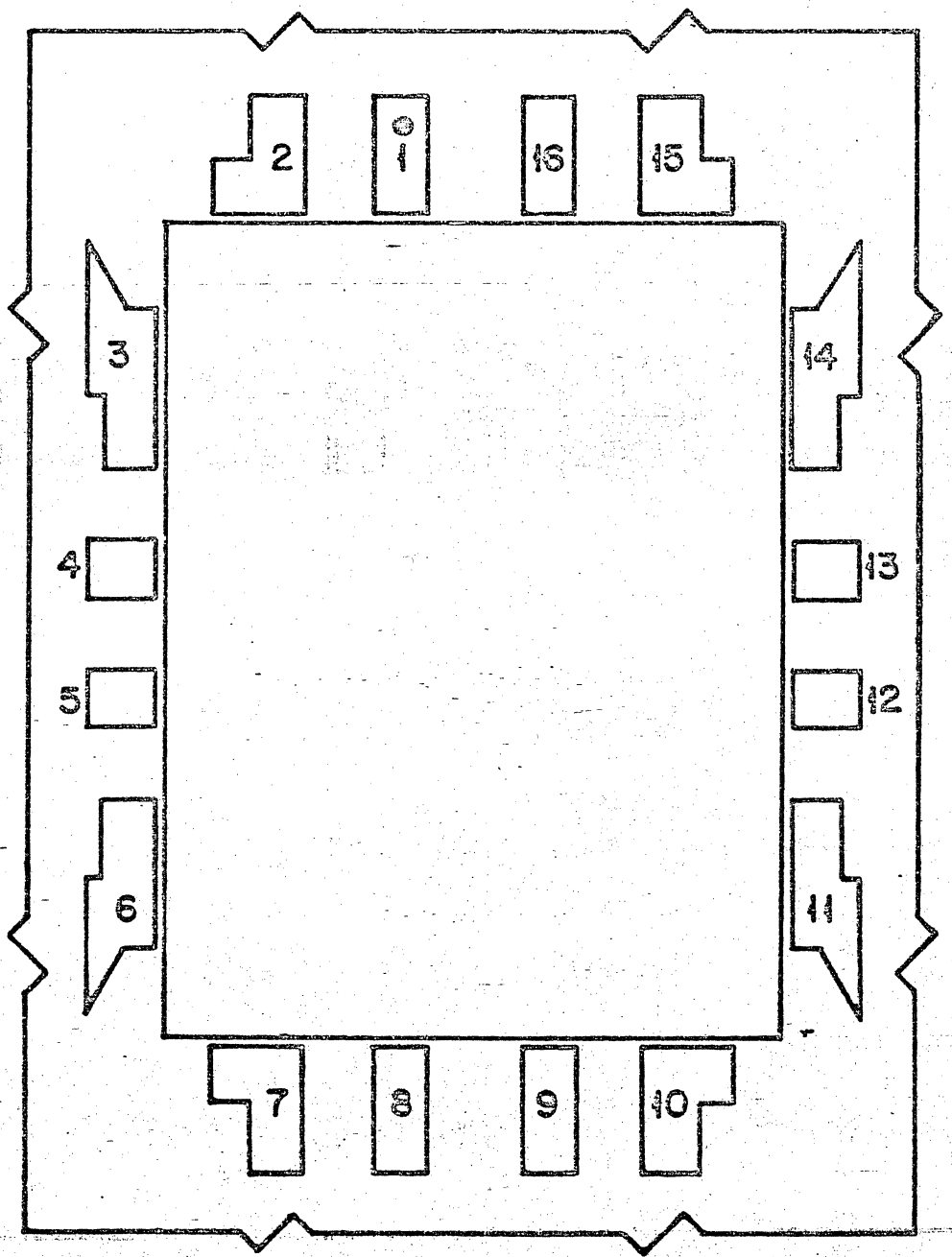
10 LEAD
TO-5
SCALE 20X



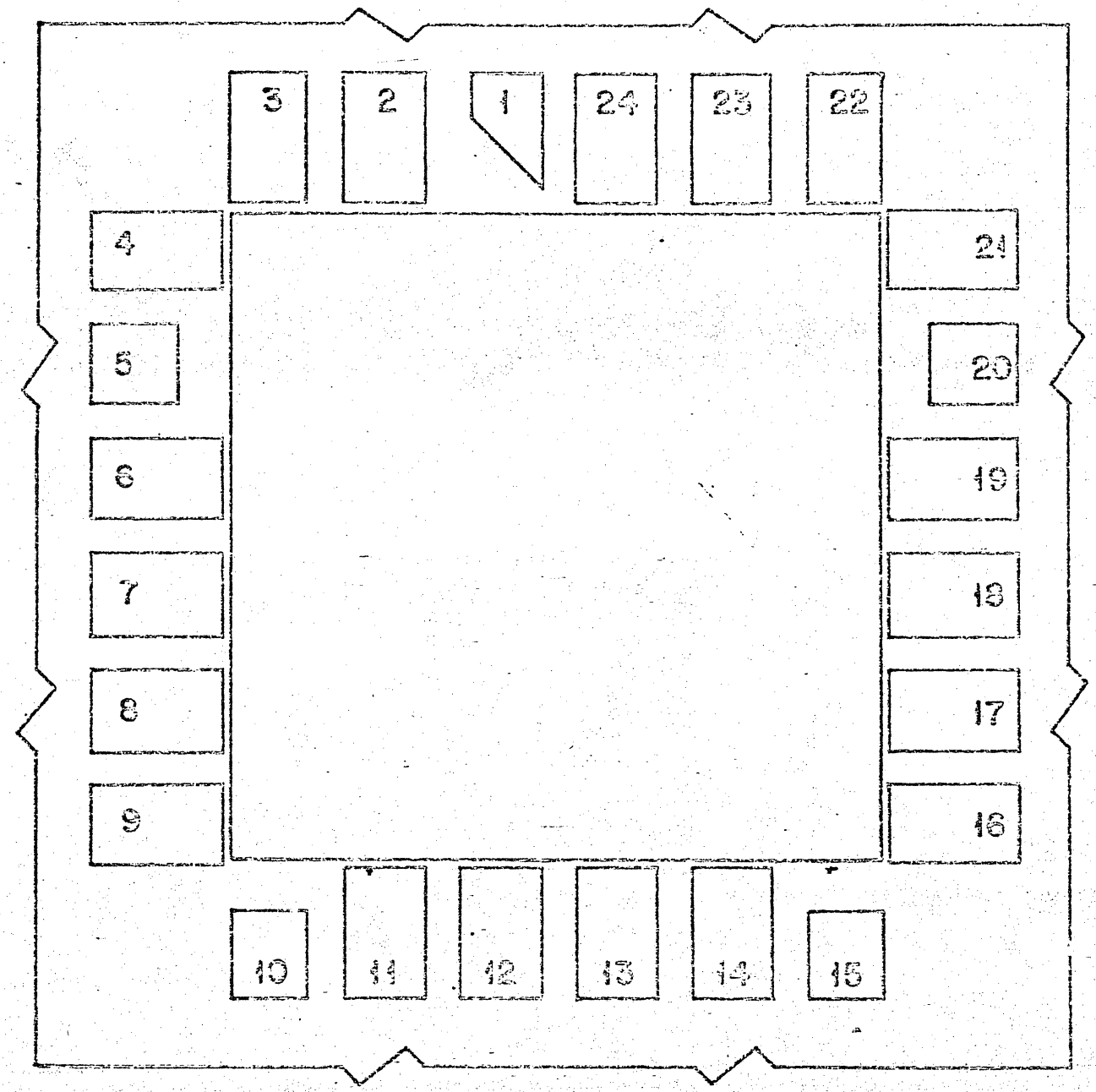
14 LEAD WHITE CERAMIC 20X



16 LEAD WHITE CERAMIC 20X

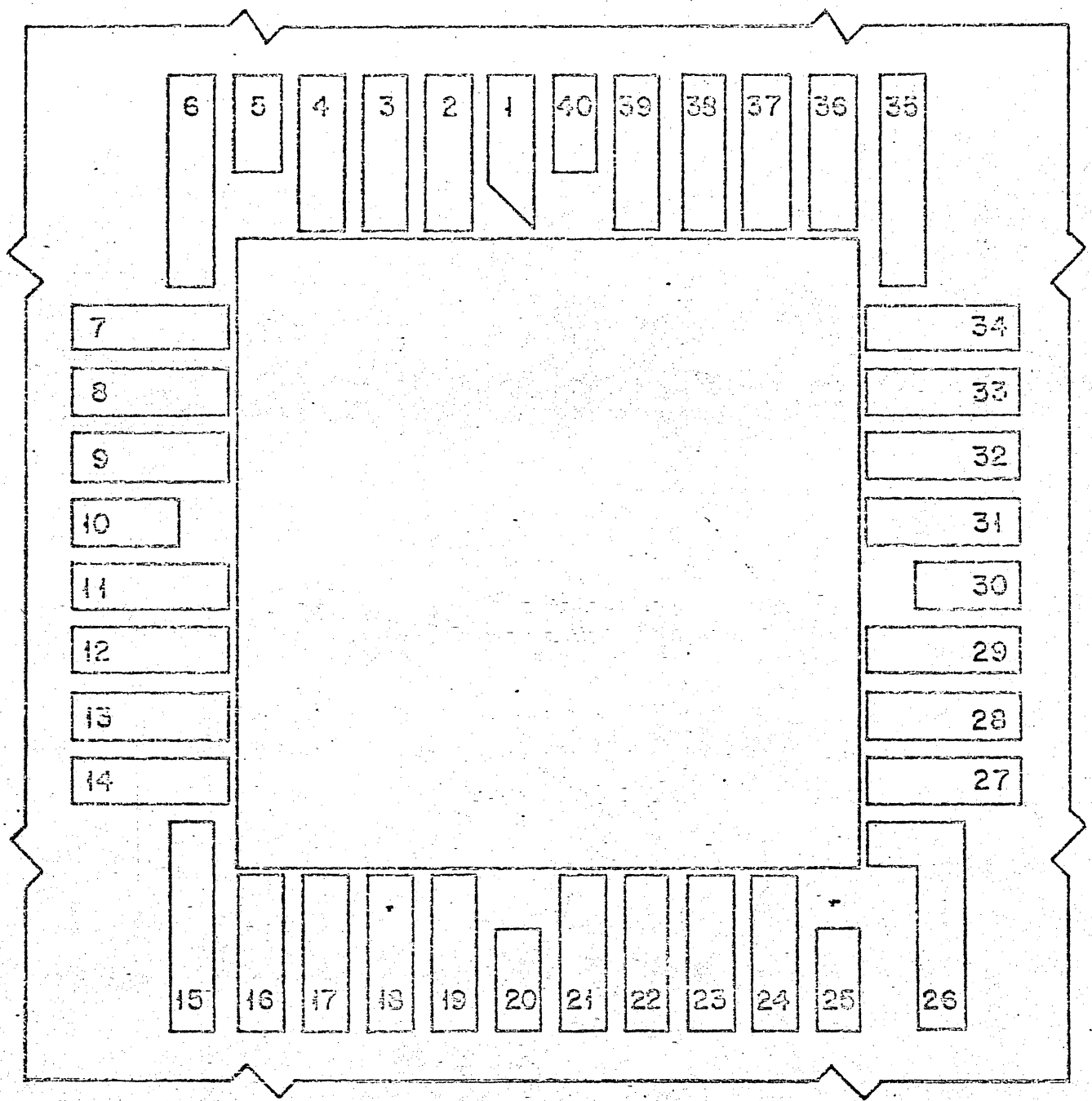


24 LEAD WHITE CERAMIC 20X



Note that pin 1 is connected to substrate unless otherwise requested.

40 LEAD WHITE CERAMIC 20X



Note that pin 1 is connected to substrate unless otherwise requested.

MOTOROLA INC.
Semiconductor
Products Division

INTEGRATED CIRCUITS
BONDING DIAGRAM

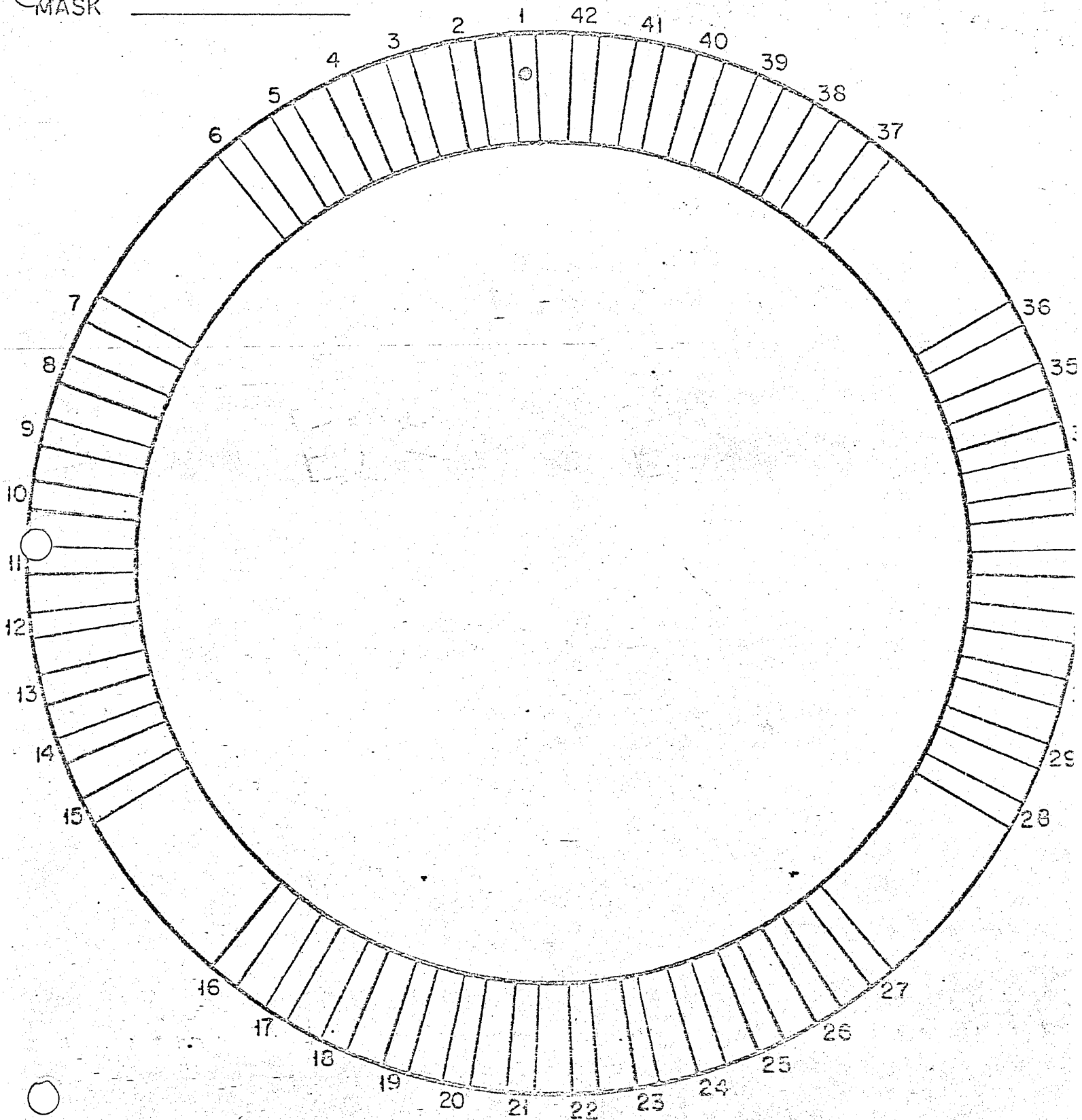
TITLE _____

DEVICE _____

IC- _____

MASK _____

42 LEAD WHITE CERAMIC 20X

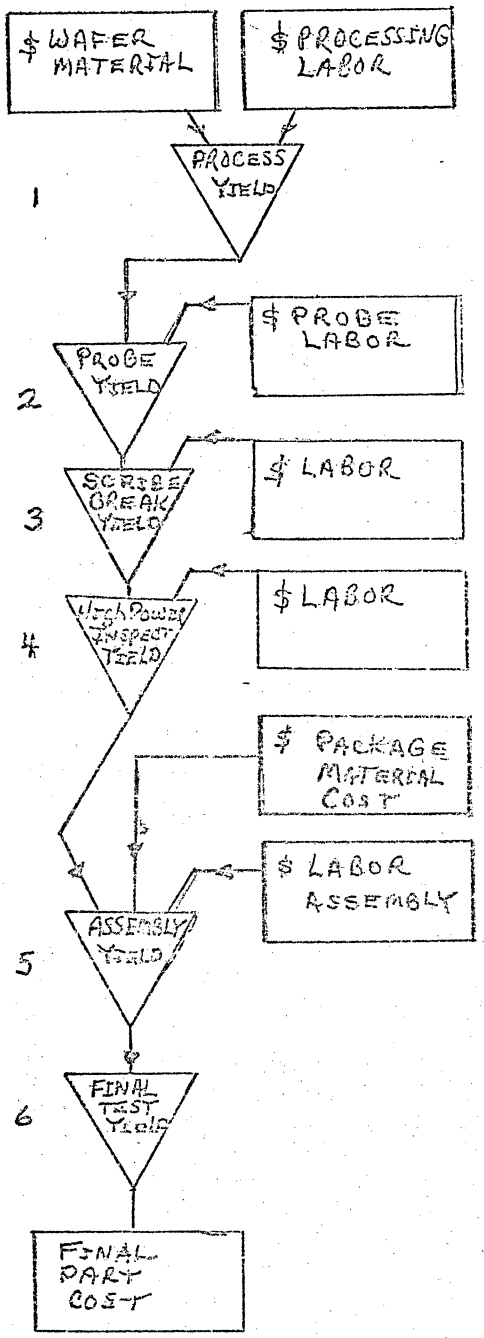


WAFER NUMBERS	DIE SIZE			PIECE PART NUMBER	MASK
					MIC-
	APPROVAL			532136	

Design Economics

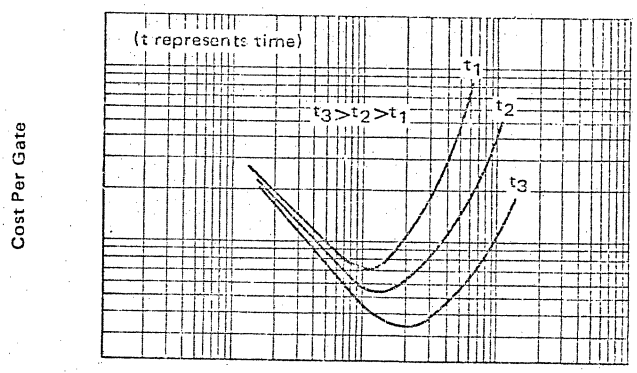
There is one more design specification: cost. All of the previous design sections are guidelines for optimizing part yield, because optimizing yield usually raises profit. However this is not always the case.

From the accompanying diagram we can approximate the cost of the part as it is built at six major cost positions or cost blocks. At each block the cost is increased by Labor, Material, or Yield. Through block 2 the cost is cost/wafer. At block 3 it is converted to cost/dice and is the only place where the price drops (appears to drop).

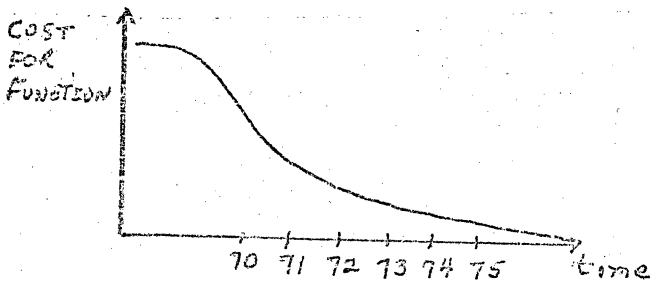


$$\text{Cost}_{OUT} = \frac{\text{Cost}_{IN} + \$\text{LABOR} + \$\text{MATERIAL}}{\text{YIELD}}$$

Cost Per Gate versus Chip Complexity



Complexity — Gates Per Chip



Now let us see the consequences of this cost function. If the processed wafer were free. the part would still cost more than the cost of the package. As the cost of the dice goes up, (by putting more logic functions on it) the cost continues to rise but the cost/function falls. This continues until the circuit is so complex that the probe yield falls. Then the cost/function begins to rise. However, as processing and assembly improve their techniques the point of minimum cost/function grows larger.

The engineer will economically optimize his design if he can estimate the estimate the effect of design decisions on yield and die size. There are two good examples:

1. Layout rules. If the engineer chooses to use loose layout rules to improve his yield, he will also increase die size. If he uses tight layout rules to get more die/wafer he will decrease his yield.
2. Bond Pads. Larger bonding pads give higher probe yield and higher final test yield, yet make the chips larger - resulting in fewer chips/wafer.

Profit is optimized by designing slightly beyond the current minimum. Thus at the time the part is in production it will be at minimum cost. Similarly if a package pin number choice can be made, both approaches should be analysed and the maximum profit approach chosen.

Soft ware is available to assist in economic optimization.

CIRCUIT EVALUATION AND TESTING

CHAPTER XX

Designer Responsibility

It is the designer's responsibility to see that useful, profitable, quality components will be the result of his design effort.

Design requirements come to the MOS Design Department from Marketing, from customers, and from management. The designer must first determine product feasibility and verify the product's usefulness or marketable applications. This is necessary to guarantee that the design cost is recoverable.

The designer next must analyze the design so that he can guarantee quality parts within the given environment and process distribution. His documentation will reflect this.

Finally the design engineer does the ground work in optimizing the profitability of a part. He does this by optimizing the circuit design, redesigning the internal structure where this will improve performance and reduce cost, suggesting system modifications where applicable, and insuring a reasonable yield. The guide lines for minimizing chip size, and optimizing performance and yield are the design rules and layout rules.

Finally the design engineer initiates the interface between design and production with the documentation of his design. The final proof is the engineering run of prototype parts. The engineer provides the initial test methods, and tests his prototypes proving that they meet all specifications, and documenting the range of process parameters in the prototype circuits.

Transfer to Production

Transferral of products from design engineering to production entails the transfer of pertanent information about the newly designed product to the appointed product engineer. This information includes logic diagrams, schematics, suggested test methods, customer or internal electrical and mechanical specifications, all characterization data that had been accumulated, and any special facts, such as critical dimensions or difficult electrical performance. This product transfer from design engineering to product responsibility is most efficiently accomplished by having a final design review and product transfer meeting where all related people are in attendance.

Product Engineer's Responsibility

Product engineers are responsible for individual products that have been released for production. Product engineers act like customer representatives within our factory. They assure that the products are manufactured on schedule, meet all specifications, and meet or better the cost objectives. Product engineers accomplish their goals by monitoring masks, quality process and production methods, performing yield improvements, specifying test procedures and methods, and maintaining good communication with the customer, and also reviewing customer specifications and preparing data sheet outlines.

TESTING OF MOS LSI CIRCUITS

Testing of MOS LSI circuits during and after manufacturing includes both electrical and mechanical tests which determine that the finished product is of the highest quality and meets all imposed specifications.

Near the completion of processing wafers, developmental and manufacturing lots are checked for threshold voltage, transistor gain, junction breakdown voltage and field-oxide inversion voltage. All wafers must pass within narrow, closely specified limits for these parameters. Wafer lots are then subjected to severe bias-temperature stress testing during manufacture and immediately prior to functional probe testing to insure that the process is yielding a stable, high quality, drift free product. These stress tests are performed at a temperature of 250°C and substantially exceed the severity of conditions faced by the circuits during normal operation.

When the wafer has completed the processing sequence and passed all process control inspections to determine that process requirements have been met, it is sent to a computer-controlled probe station. Utilizing the test control tape generated during the design phase, complete parametric and functional tests of the individual circuits on the wafer are performed. Functional tests exercise the circuits to demonstrate that they, in fact, perform the logical function specified by the designer. At the same time, a series of parametric measurements is performed to check the input and output terminals, the clock lines (if present on the circuit), and the power supply buses for excessive leakage current and low breakdown voltage. When design permits, power consumption is

measured to determine that it is within the design rating. Die that do not meet design requirements are automatically inked to mark them for discard during assembly operations.

Parametric measurement at wafer probe is a unique feature of the Motorola Production System. Special computer-controlled wafer probe test equipment has been designed and constructed by Motorola expressly for testing custom MOS LSI circuits. As far as can be determined, this equipment exceeds the capability of any commercially available equipment in terms of data rates, length of non-repetitive test patterns, parametric measurement ranges, and overall speed and capacity. Fault categorization, data logging, and interactive operating modes through a CRT interface are provided for ease of evaluating circuit performance over a wide variety of engineering conditions.

Following wafer sort, the electrical good die are subjected to stringent visual inspection under high-power magnification. Fully tested and inspected dice are then bonded and sealed in packages. The sealed packages are subjected to normal forms of mechanical tests such as centrifuge, temperature cycling, and gross and helium-fine leak tests in order to insure that the assembly operations have been properly carried out. The exact testing plan followed, ranging from limited lot sample to 100% testing, depends on customer requirements.

Completed devices are final tested using the high-speed computer-controlled tester. The test tape developed during the design phase is used to determine conformance to both functional and parametric specifications for the unit.

The customer may request any combination of electrical and mechanical test of the finished units. These final test require-

ments may range from commercial practice through high-reliability, military-type programs, and may involve such operations as high- and low-temperature functional testing, and burn-in. Generally, the more stringent the testing conditions scheduled, the higher the cost. Unless specified by the customer, it will be assumed that standard commercial practice is desired.

All tests are normally done by production personnel under the direction of product engineers, who write and review all test specifications and procedures.

Quality assurance is provided by quality conformance inspections and tests done on a lot sample bases by personnel of the quality assurance department.

Reliability assurance is demonstrated by exhaustive and extensive testing to verify that the design, manufacture, inspection, and testing are adequate to assure the reliability of the products.

MOS/LSI Tester

This advanced tester consists of test electronics controlled by a PDP-8/L computer and multiplex unit that allows testing capabilities at four remote stations. Peripheral equipment includes a 64-k disk and two magnetic tape units for storing existing tests and data logging.

For dc parametric testing, the tester is capable of handling up to 64-pin through the use of 64 completely independent voltage or current generators. Voltages over the range of +40V-40V can be forced or measured with an accuracy of ±20 mV. Currents can be forced or measured with an accuracy of ±1% over a range of 5 nA to 20 mA. Typical test rates of 50 kHz can be realized at each test station.

In the functional test mode, input driver channels and output receiver channels are hard-wired to the socket of the unit under

test. This technique does not require a relay matrix to route test signals to and from the chip. In addition, unity gain buffers are mounted within 2 inches of the output pins under test which present an equivalent test load of 10 pF and 10 MΩ. As a result, a test rate as high as 4 MHz is attainable.

Each input driver channel (60 total) can buffer up to 1000 bits of data before reloading from the disk. Functional input levels from the drivers are programmable from 0 V to -35 V range with an accuracy of ±50 mV. Since the tester output is programmable relative to data input within ±20 ns, one has the capability of measuring output transition times of the unit under test.

CHAPTER XXI

I N T E R F A C E S

PHOTOLAB ORDER FORM

DATE 6 JAN 70

CUSTOMER W. BRIDWELL

NO. ASSIGNED THIS NO. ASSIGNED BY MASK SHOP

EXTENSION 273 6041

TARGET SET NO. PC 26 (MESA) IC 41(6

DEVICE DESCRIPTION DUAL 50 BIT STATIC SHIFT REG

TARGET DIE SIZE LEAVE BLANK

PATTERN DIE SIZE (ADD 3" MILLS" TO H & W OF L.O. FOR SCRIBE

DEPARTMENT NO. BB 587

PATTERN ARRAY SIZE 2" X 2"

PROJECT NO. 3580

PLATE SIZE 2½ X 2½

NO. OF MASTERS 5 (6 IF DN)

APPROVAL Your Signature

LEAVE THIS AREA BLANK

DATE RECEIVED

ARTWORK SCALE

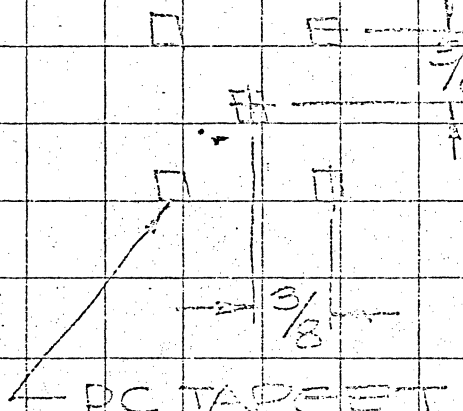
DATE REQUIRED

TARGET SCALE

DATE COMPLETED

TARGET Q.C.

MASK LISTING	DESCRIPTION	DENSITY	NO. OF COPIES	TARGET NO.	ARTWORK CUT	ART. CHECKED	LANSTON POS.	LANSTON NEG.	MANN 1ST. RED.	CONTACTS	CONT. MOUNTED	STEP SHEET	BOXES LABELED	MASTER STEPPED	PROD. MASTER	COPIES
04	"P" DIFF	P	10	04												
06A	PRE-OHMIC	P	10	06A												
06B	GATE	P	10	06B												
08	METAL	N	10	08												
09	PASSIVAT.	P	10	09												
05	DN+	P	10	NO TARGET												



MOTOROLA FORM NO. SPD-3383

VVT 1

SPECIAL RUN TICKET

This sheet will accompany all engineering lots through probe.

Date: _____ Device Type: _____

Lot Identification: _____

Lot History: _____

Probe Instructions: _____

_____

_____

Probe Operation	Quantity In	Quantity Out	Operator Initial	Date
1. Set Up To Attached Diagram				
2. Load Attached Program				
3. Probe & Ink				
4. Data Log				
5. Dice Size				

SPECIAL INSTRUCTIONS: _____

_____

_____

_____

_____

_____

MOS INFORMATION SHEET

Project No. _____ Mask Set No. _____

I. Circuit No. & Type: _____ Date: _____

II. Starting Material:

1. W25A00 - 1 1/2:
   W25A00 - 2"
   Epi 12-16μ ⟨100⟩
   Res. 1.3-2.0Ω-cm
   1400Å Deposited Oxide

2. W26A00 - 2"
   Non-Epi ⟨111⟩
   Res. 3-5Ω-cm

3. W27A00 - 2"
   Non-Epi ⟨100⟩
   Res. 3-5Ω-cm

4. W28A00
   Non-Epi ⟨111⟩
   Res. 1-3Ω-cm

5. W29A00
   Non-Epi
   ⟨100⟩ 1-3Ω-cm

6. L15B00
   Non-Epi ⟨111⟩
   Res. 6-7Ω-cm

7. L15C00
   Non-Epi ⟨100⟩
   Res. 7-8Ω-cm

III. Flow Sheet:

1. AP01D a. Source/drain 15±5Ω/sq
   b. N+ Diffusion
   c. Field Oxide 10K Å

2. AP02D a. Source/drain 15±5Ω/sq
   b. N+ Diffusion
   c. Field Oxide 5.5K Å
   d. No gold backing

3. AP03D a. Source/drain 15±5Ω/sq
   b. N+ Diffusion
   c. Field Oxide 5.5K Å

4. AP04D a. Source/drain 75±25Ω/sq
   b. With N+ Diffusion
   c. Field Oxide 10K Å
   d. ⟨111⟩ Material

5. AP05D a. Source/drain 75±25Ω/sq
   b. Without N+ Diffusion
   c. Field Oxide 10K Å
   d. ⟨111⟩ Material

6. AP06D a. Source/drain 75±25Ω/sq
   b. N+ Diffusion
   c. Field Oxide 5.5K Å
   d. S&D Redistribution(±j4.0μ

7. AP07D a. Source/drain 75±25Ω/sq
   b. With N+ Diffusion
   c. Field Oxide 10K Å
   d. ⟨100⟩ Material

8. AP08D a. Source/drain 75±25Ω/sq
   b. Without N+ Diffusion
   c. Field Oxide 10K Å
   d. ⟨100⟩ Material

IV. Die Size: _____

V. Mask Sequence: _____

VI. No. of Wafers Required: _____

Cycle Time Needed: _____

VII. Requester's Name: _____

VIII. Comments: _____

RB 587
.8666

CER DIP
SPECIAL RUN TICKET

This sheet should accompany the lot through production and be delivered to Final Test with the lot.

Date: 3/13/70 Device Type: F-2

Lot Identification: TR #387 #2

Lot History:

Special Assembly Instructions: Package Pictured Die, ~~25~~ from each wafer. Return unused die.

Assembly Operation	Quantity In	Quantity Out	Operator Initial	Date
1. ~~Scribe~~				
2. ~~Break~~				
3. Hi Power Insp		30-30	DL	3-16-70
4. Load		30	[illegible]	3-16-70
5. Die Bond		30	[illegible]	3-16-70
6. Die Bond Insp.	27	25	SKS	3-17-70
7. Wire Bond		25	RSH	3-17-70
8. Wire Bond Insp.		24	EEG	3-17-70
9. Wash	22	22	LC	3-19-70
10. Preseal Insp.	22	22	CS	3-19-70
11. Furnace Seal	22	22	LC	3-24-70
12. Final Seal Insp.				
13. ~~Bake 24 hrs. 175°~~				
14. ~~Temp. Cycle 5 cycles -65° +175°~~				
15. Centrifuge 20,000G's				
16. ~~Plating~~				
17. ~~Gross Leak Test FL-30~~				
18. ~~Helium Leak Test 1 x 10-8cc/sec.~~				
19. Lead Clip		22	DL	3-25-70

Please Expedite
Thanks

Return to Processing

MOTOROLA INC.
Semiconductor
Products Division

INTEGRATED CIRCUITS BONDING DIAGRAM

TITLE _____

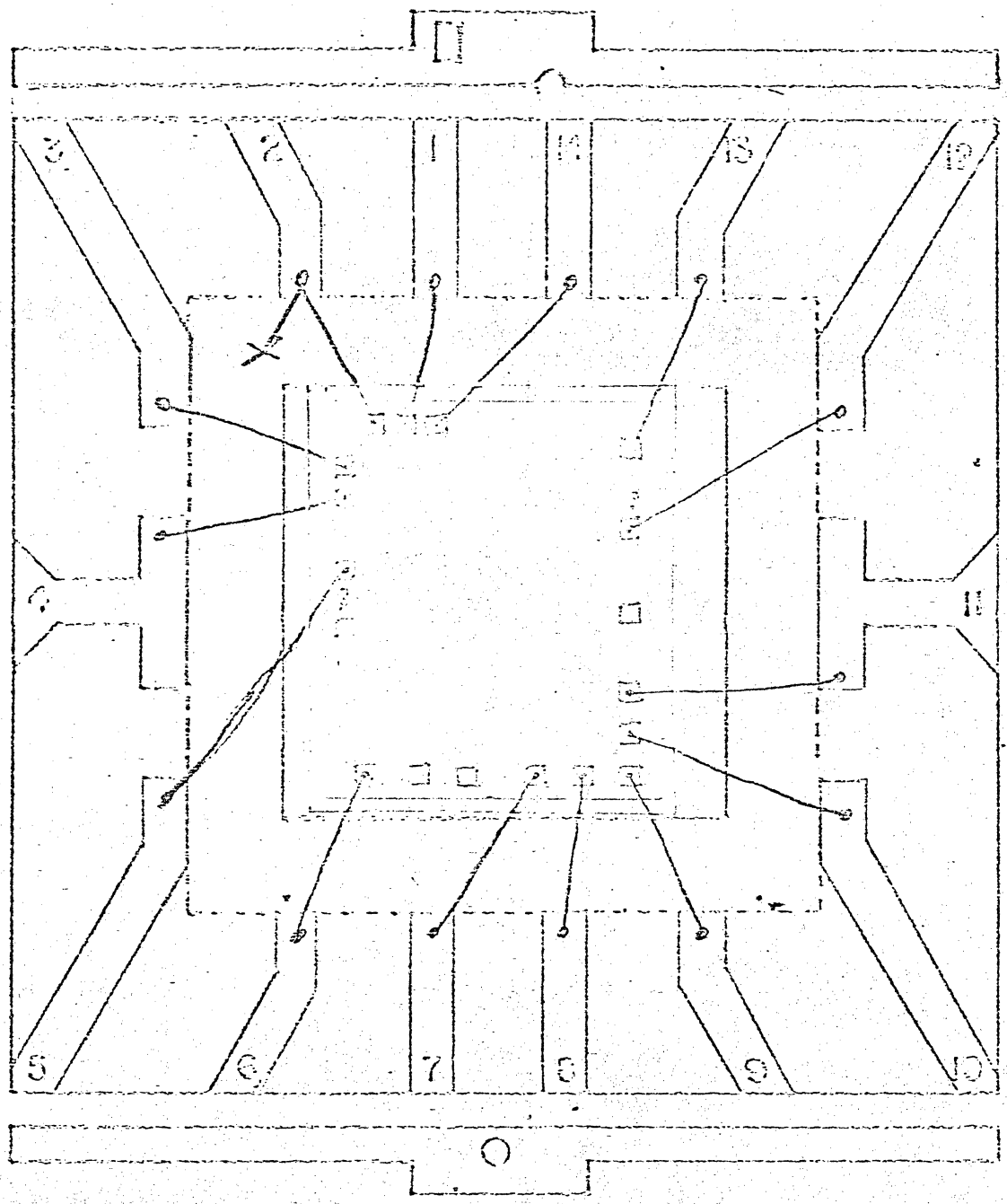
DEVICE _____

MASK _____

14-lead Dual-In-Line Package

Cavity size: 112 x 146 mils

SOLDER GLASS DIP



SECTION

DIE SIZE

SPECIFICATION

CHAPTER XXII

GLOSSARY

AF	Reduction of carrier mobility at surface due to random surface scattering.
Beta	Gain term in equation for MOS device current in $\mu a/volt^2$ $\beta = \frac{A_f \cdot \mu_p \epsilon_o K_{si}}{t_{ox}} Q_2$
Beta Degradation	Decrease in gain due to reduction of mobility in high fields.
Body Effect	Increase in effective threshold voltage due to bias voltage on source.
Cam	Content addressable memory
Channel	Region of MOS device between source and drain through which current flows.
Channel Length Modulation	Apparent decrease in channel length of MOS transistor biased in saturation, decreases channel length with increased drain-source voltage.
CMOS	Complementary MOS - Both N channel and P channel MOS devices on same chip
Cost Block	Point at which yield loss, labor, or material increase part cost
C_{PN}	Capacitance of a PN junction
Depletion	Device which allows drain current when $V_{GS} = 0$
Drain	MOS device terminal which receives carriers from channel

Enhancement	Device which requires gate bias before conduction
ϵ_o	Permittivity of free space = $8.87 \cdot 10^{-14}$
FET	Field Effect Transistor - Voltage controlled current source transistor.
Field Inversion	Unwanted MOS action between diffusions covered with thick oxide
Field Plate	Device used to protect gate from over voltage rupture
Gate	Voltage actuated control terminal of transistor; or logical function
I_{DS}	Current flowing from source to drain
IGFET	Insulated Gate Field Effect -any FET device where gate is electrically insulated
Inversion	Voltage point at which carriers form in channel
JFET	Junction Field Effect Transistor - gate is not insulated and can draw current when forward biased
K_s	Dielectric constant of silicon - 11.7
K_{siO_2}	Dielectric constant of silicon dioxide - 3.9
L	Channel length - physical distance between source and drain parallel to current

MIS	Metal insulator semiconductor
MNOS	Metal Nitride Oxide Semiconductor - a nitride is used in device to reduce pinholes and increase device gain
MOS	Metal Oxide Semiconductor - particular structure of field effect transistor
N_D	Doping level in N type semiconductor
NDRO	Non-destructive readout memory
NMOS	N channel MOS - The MOS transistor is fabricated with N doped diffusions into a P-type silicon substrate
ϕ_F	Fermi function - the amount the fermi level is displaced from the intrinic level (units in volts)
θ_j	Thermal impedance from the junction
PMOS	P channel MOS - the MOS transistors fabricated with P doped diffusion into a N-type silicon substrate
Q_{ss}	Surface state charge
RAM	Random Access Memory - memory
ROM	Read Only Memory
SAG, SAGMOS	Self aligning gate MOS - either silicon gate or ion implanted structure

Saturation	The point of operation when drain current tends to be a constant value independent of drain voltage
SIG, Silicon Gate	A type of MOS fabrication in which doped polysilicon replaces the metal gate used in conventional MOS
Source	Power terminal of MOS transistor which sources carriers
Substrate	The material on which the MOS circuit is fabricated. For P-channel MOS the substrate is normally N-type silicon
Threshold	The voltage applied to gate terminal just at the point of conduction
V_{DD}	Drain supply voltage
V_{DS}	Drain to source voltage
V_{FB}	Flat band voltage
V_{GG}	Gate supply voltage
V_{GS}	Gate to source voltage
V_{SB} , V_S	The voltage applied between source and substrate
V_{SS}	The voltage applied to the substrate of a device
V_{to}	The gate to source voltage at which "current from source to drain begins to flow". This value is obtained by extrapolating from higher current levels to the zero current intercept.

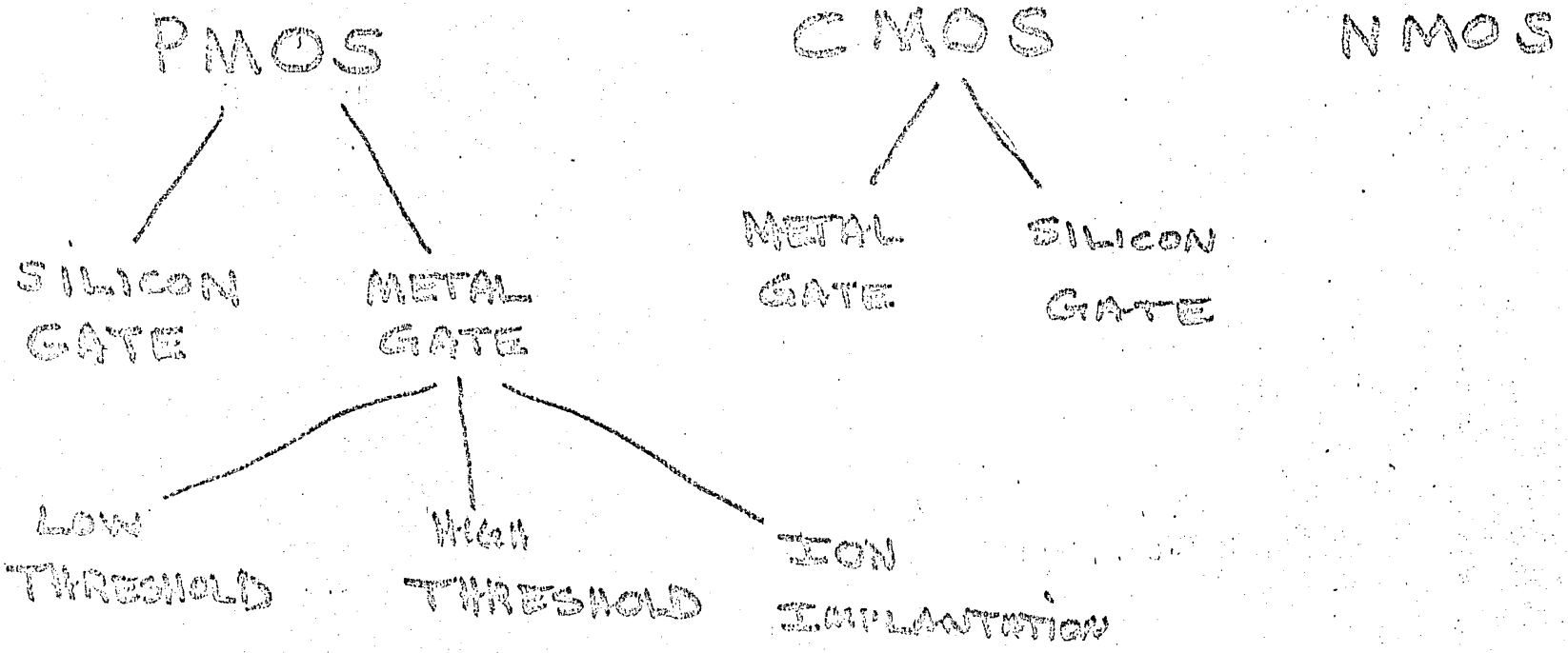
W	See Z
X_j	Depth of the source-drain (or other) diffusion
Z	Also called W - The width of the channel perpendicular to the direction of current flow
⟨111⟩	The crystal oreintation which gives higher threshold voltages
⟨100⟩	The crystal orientation which gives smaller threshold voltages

MOS

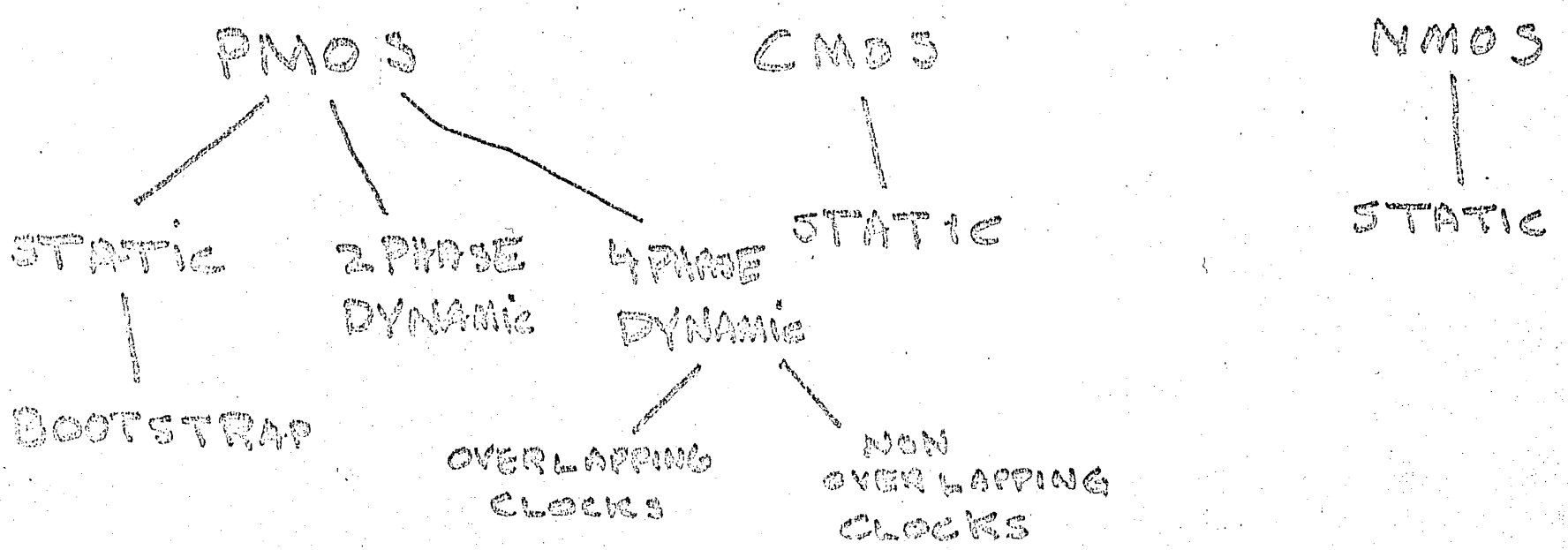
LOGIC

CIRCUITS

PROCESS LOGIC FAMILY TREE



LOGIC FAMILY TREE

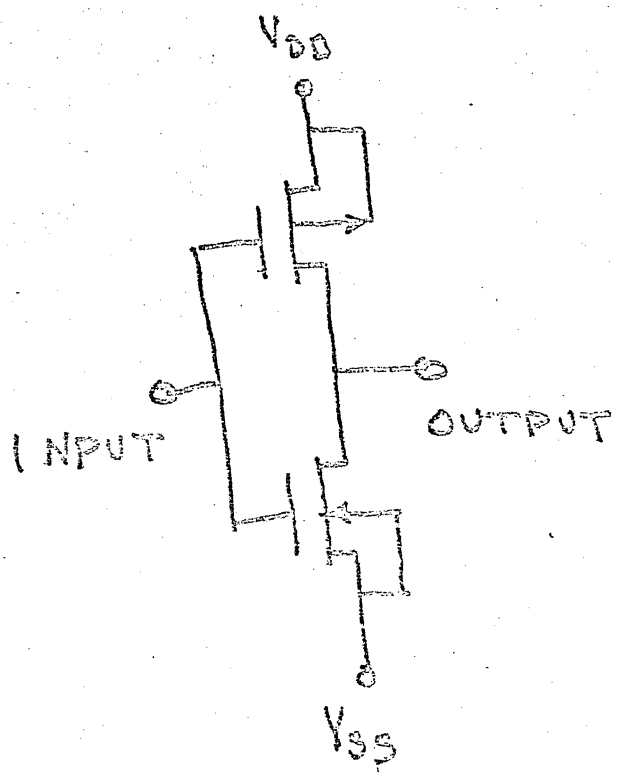


STATIC

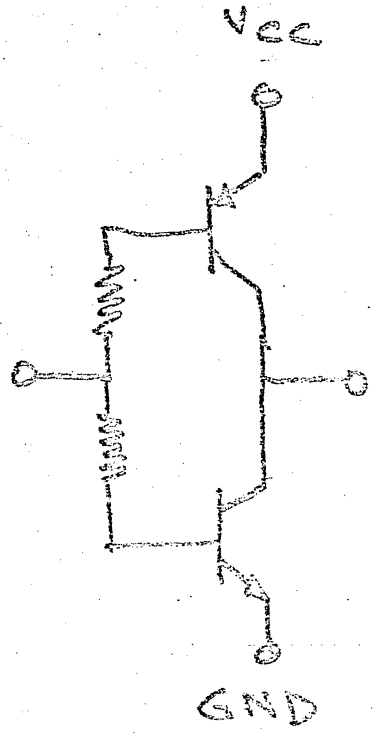
LOGIC

CMOS INVERTER

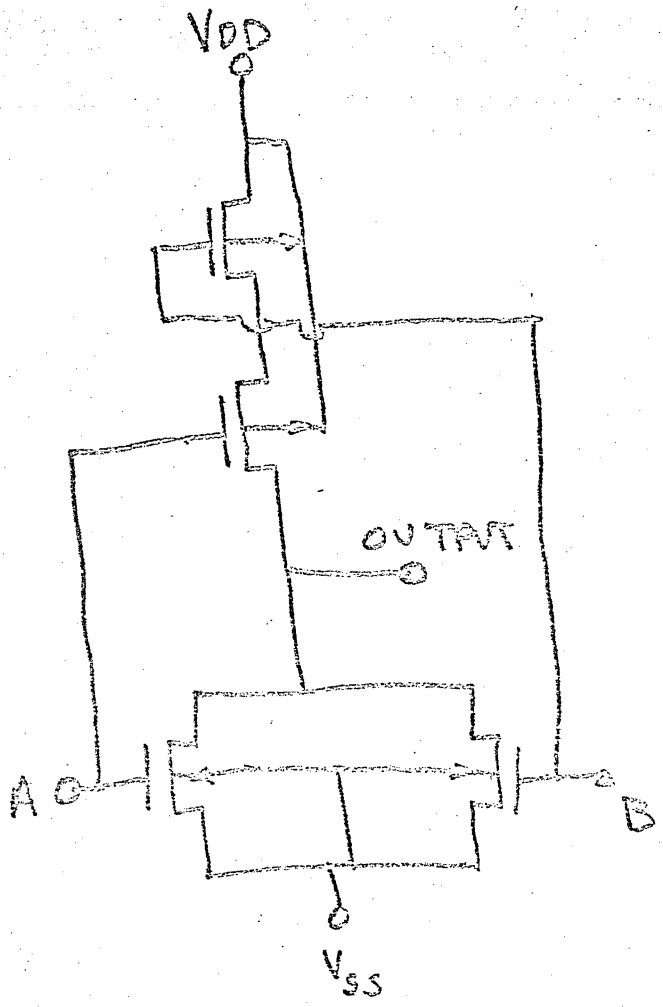
CMOS

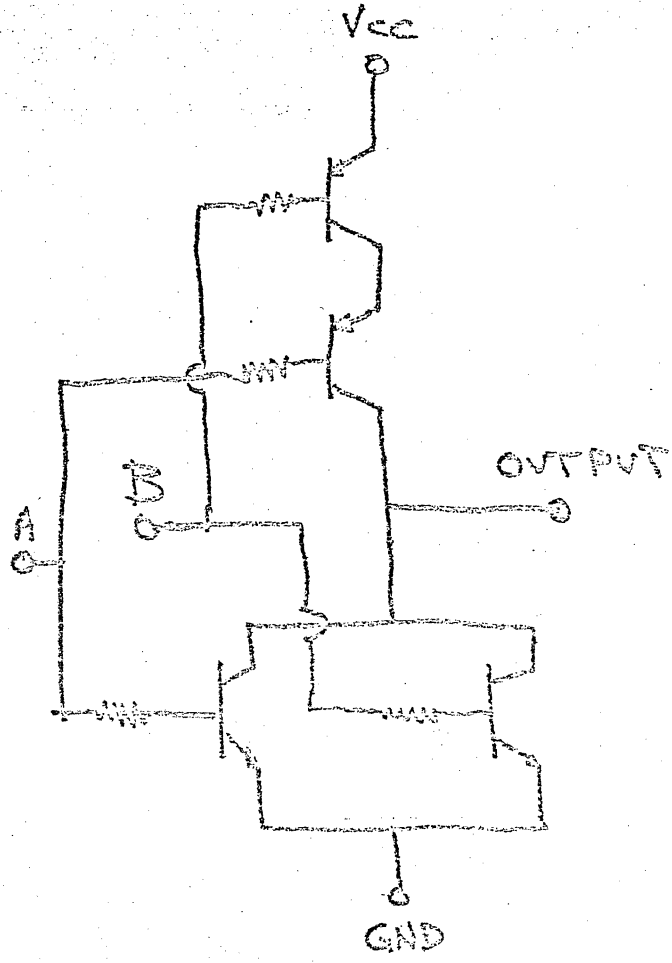


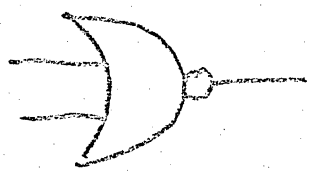
BIPOLAR EQUIVALENT



CMOS
Two Input NOR

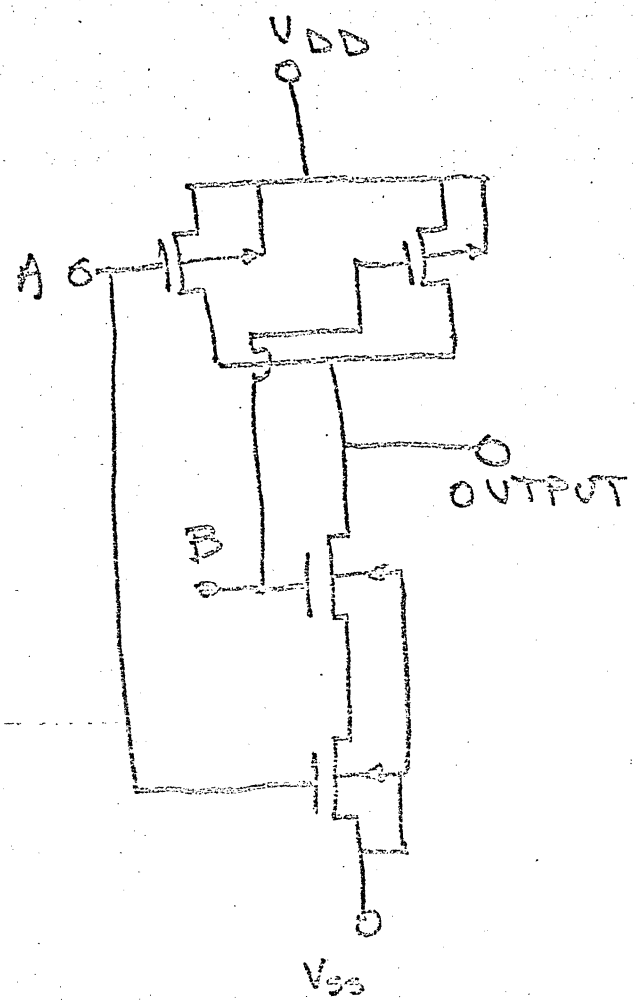


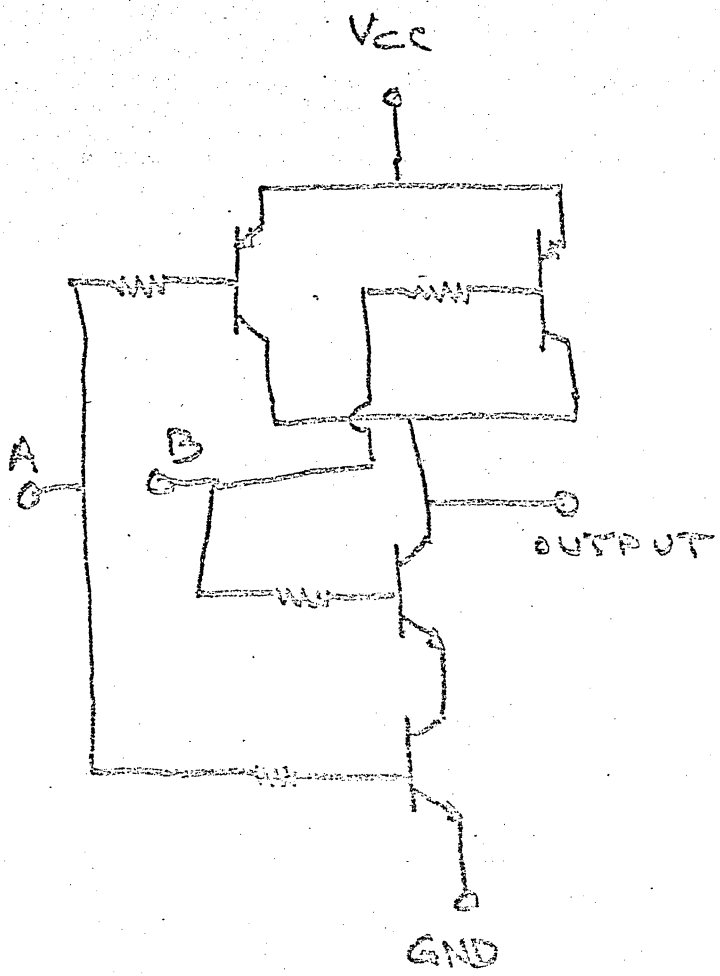


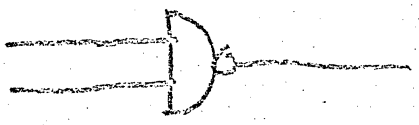


CMOS

Two Input Nand

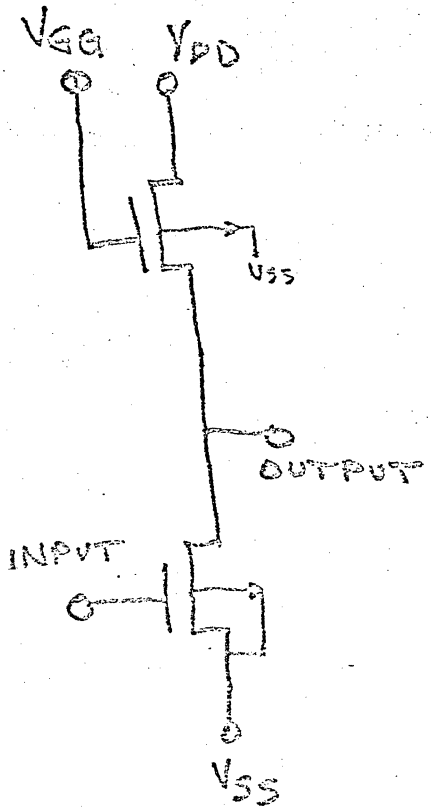




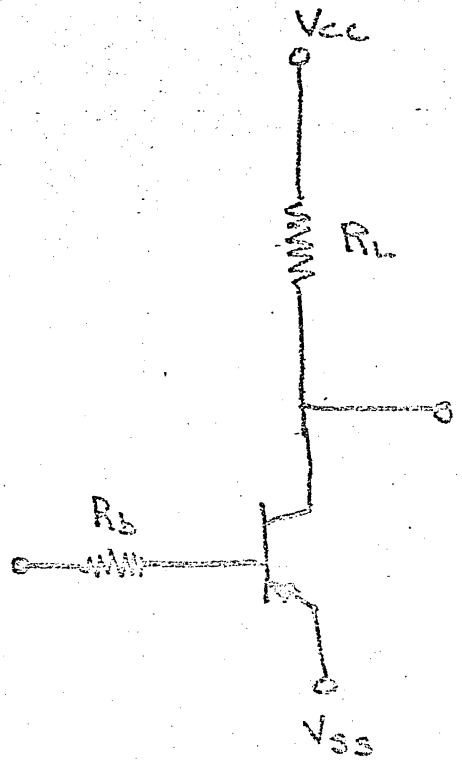


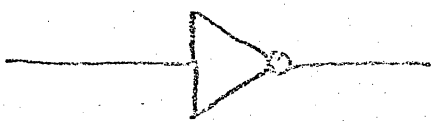
PMOS INVERTER

PMOS

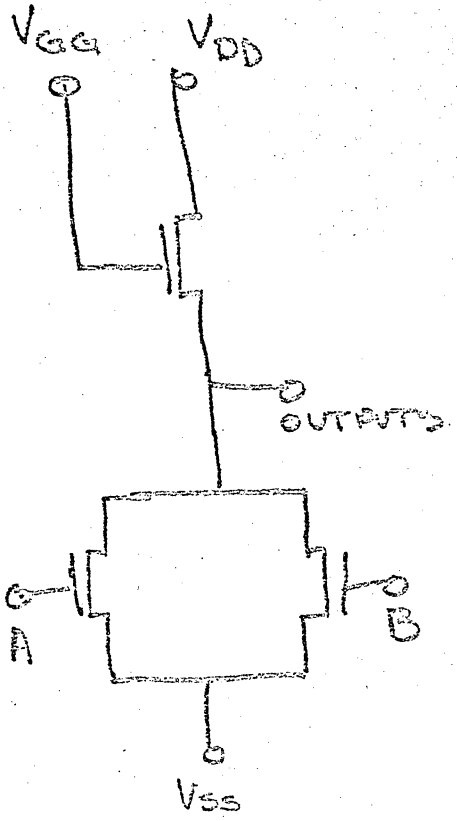


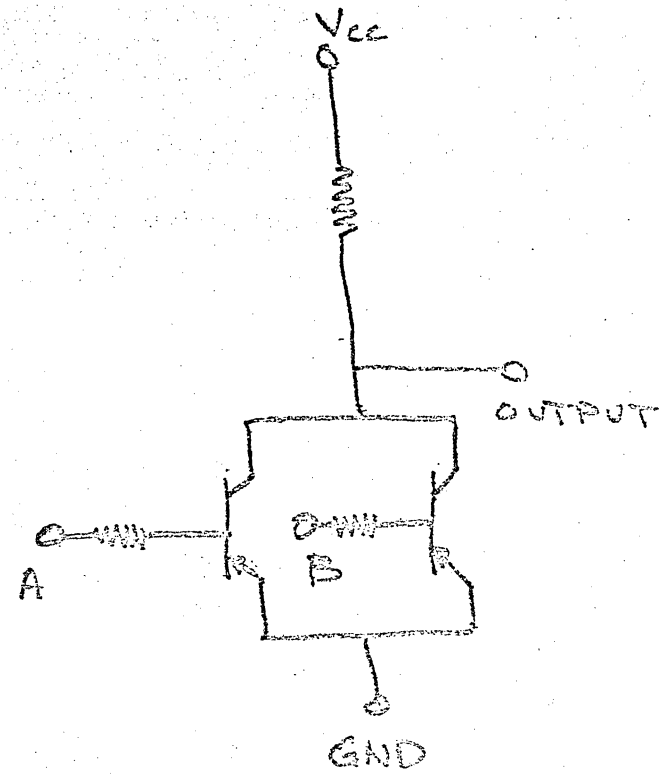
Bipolar Equivalent

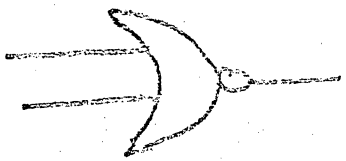




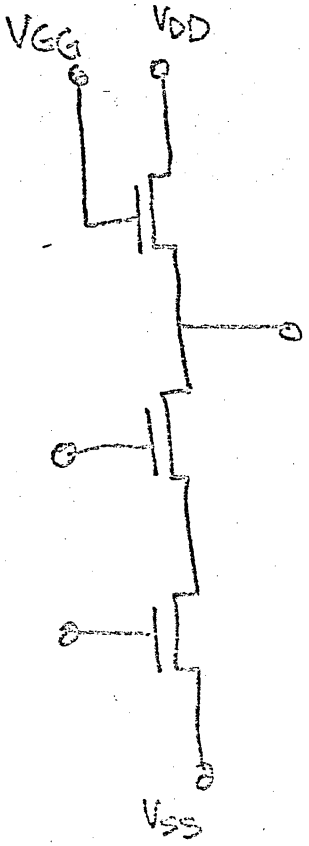
PMOS
Two Input NOR

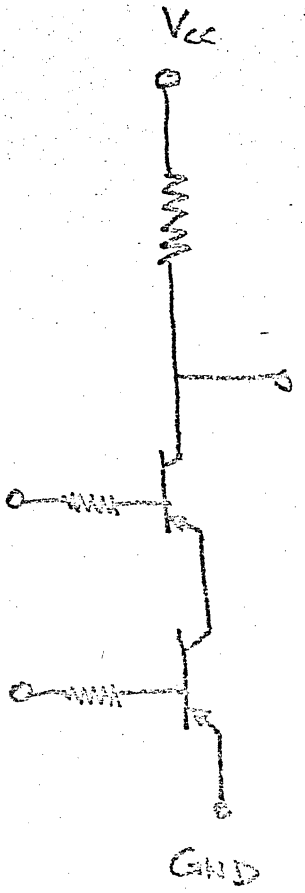


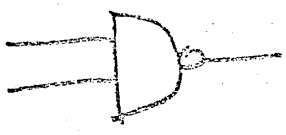




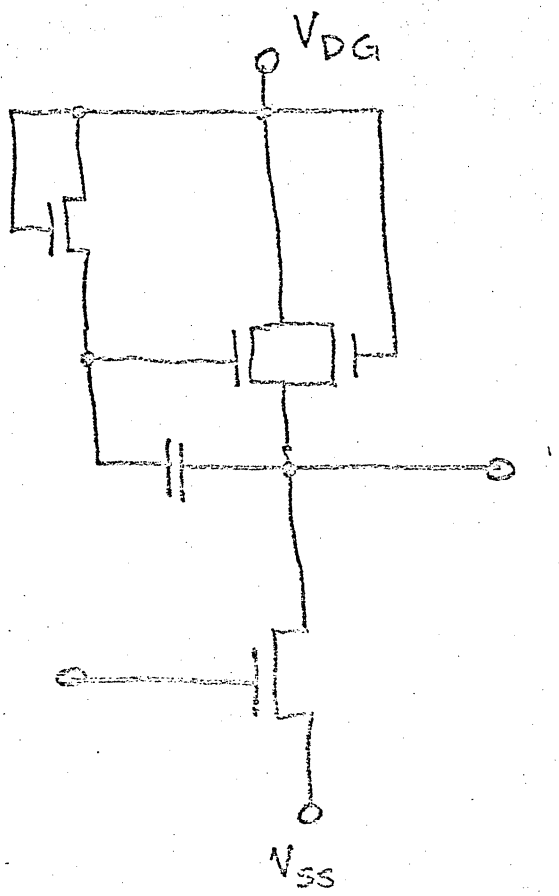
PMOS
Two Input Nand



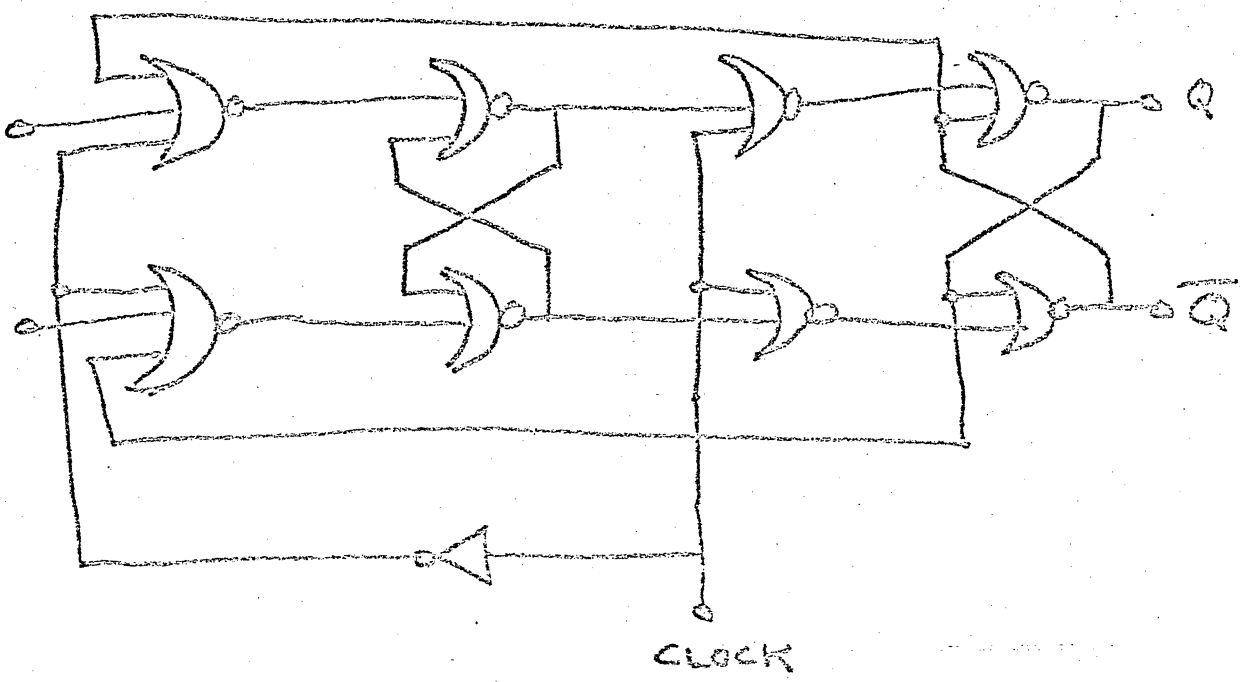


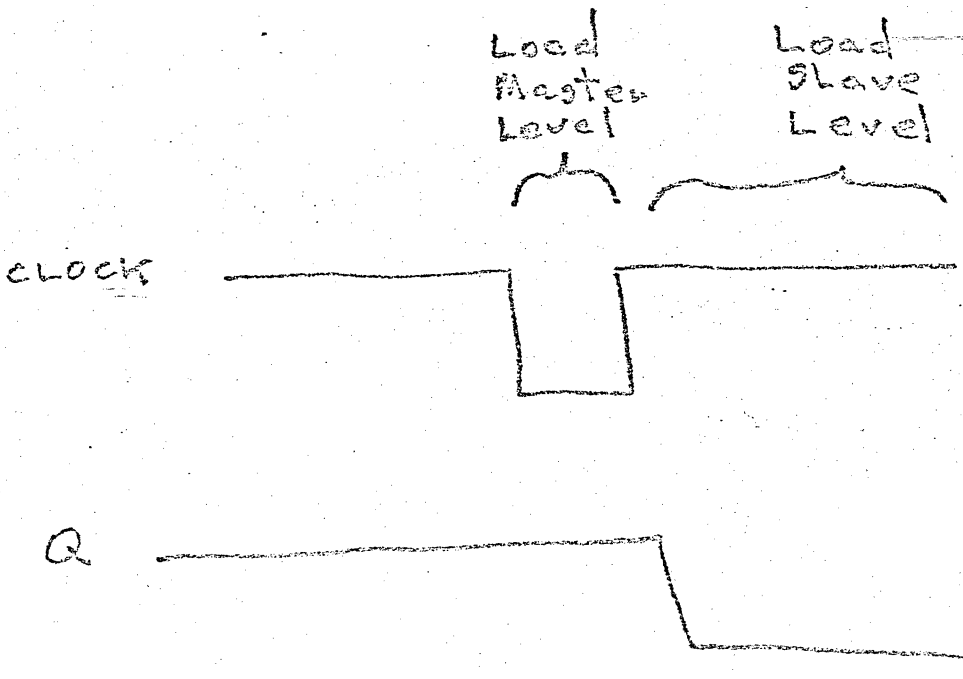


PMOS Bootstrap Load Device



MASTER SLAVE JK FLIP FLOP

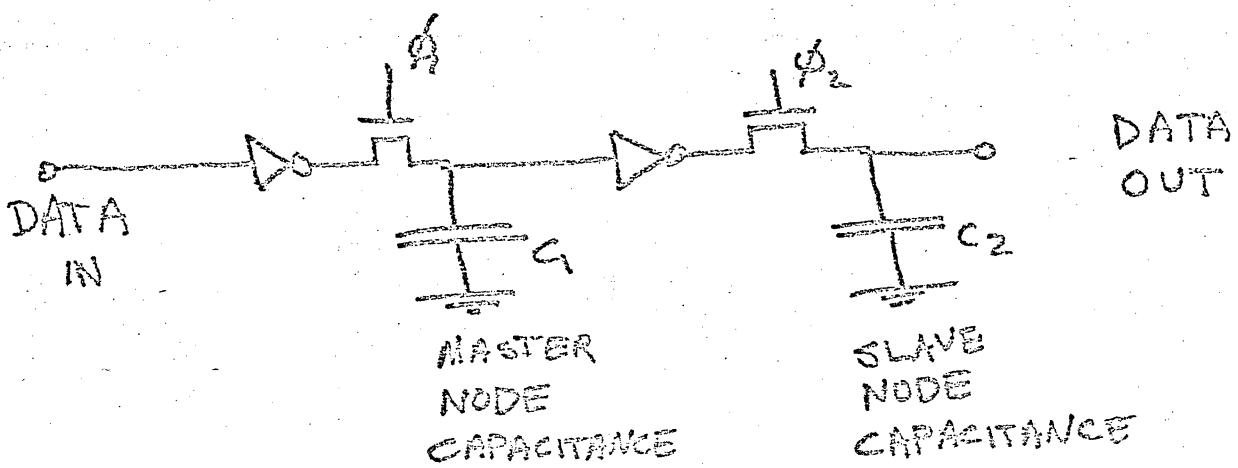


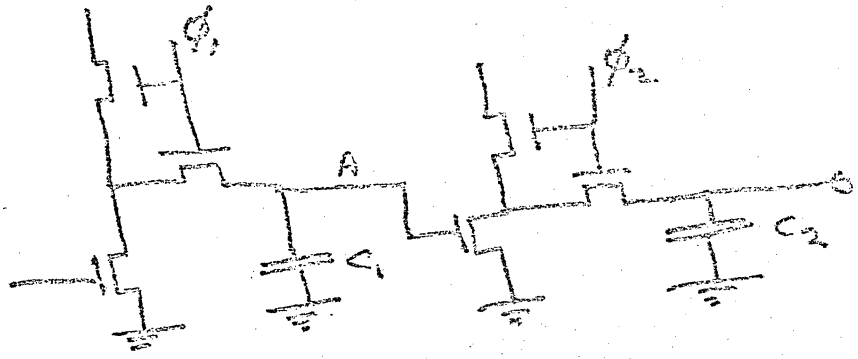


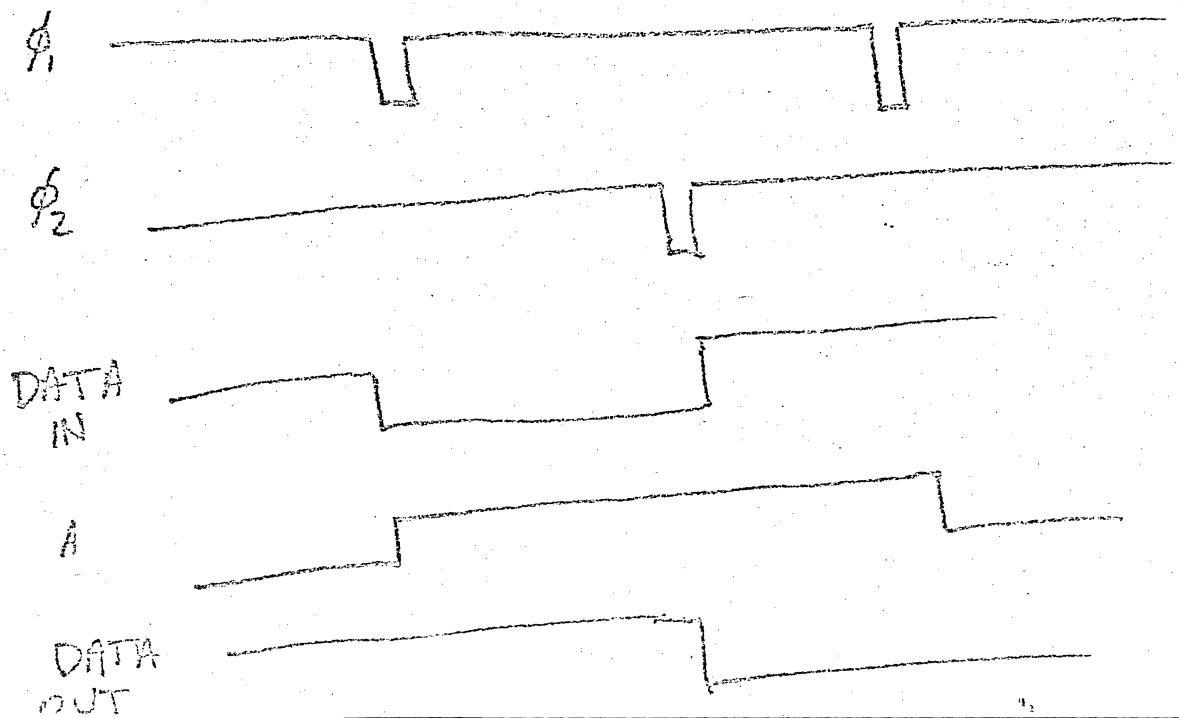
TWO PHASE DYNAMIC LOGIC

Two Phase Operation

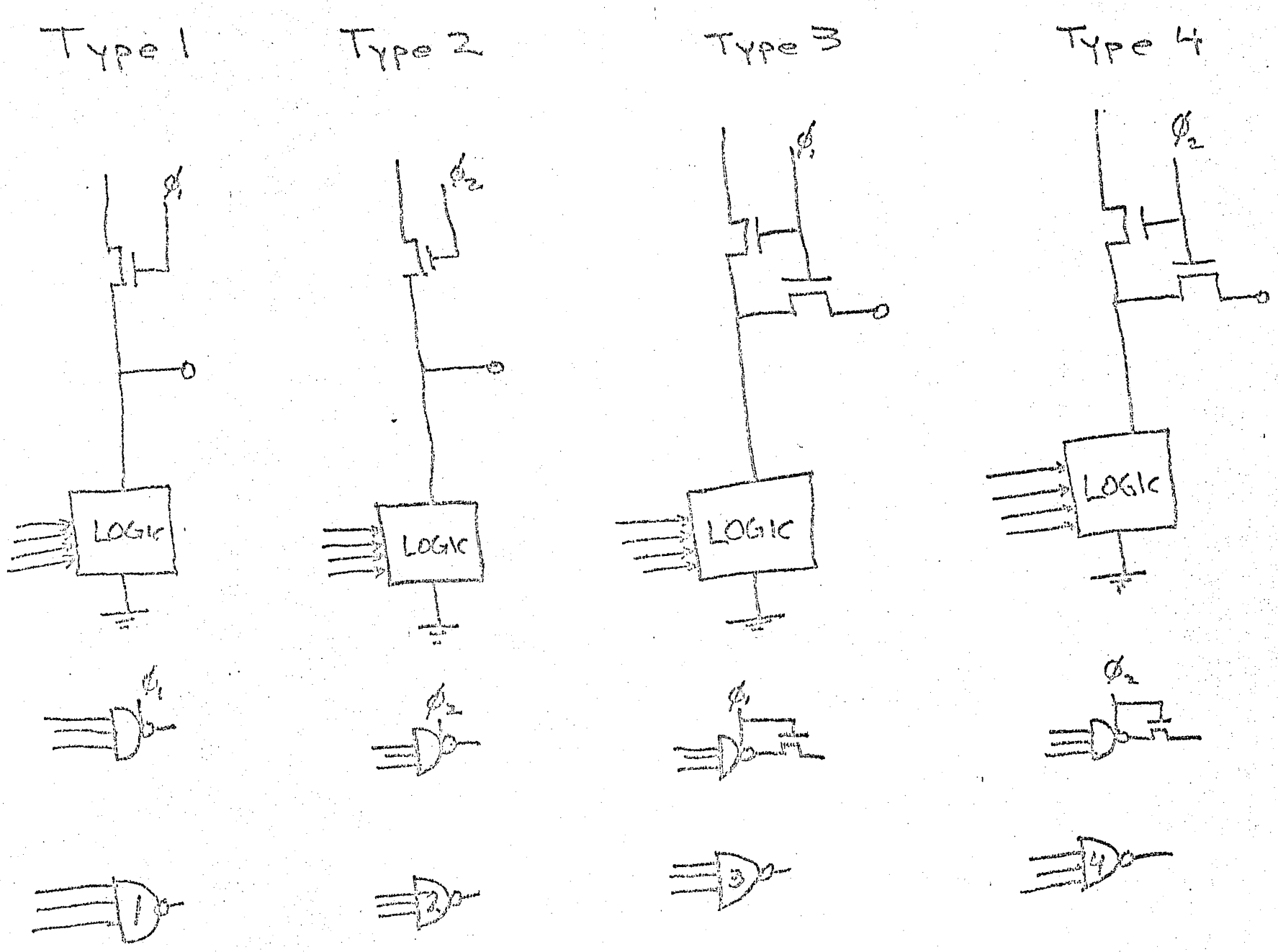
Shift Register Bit



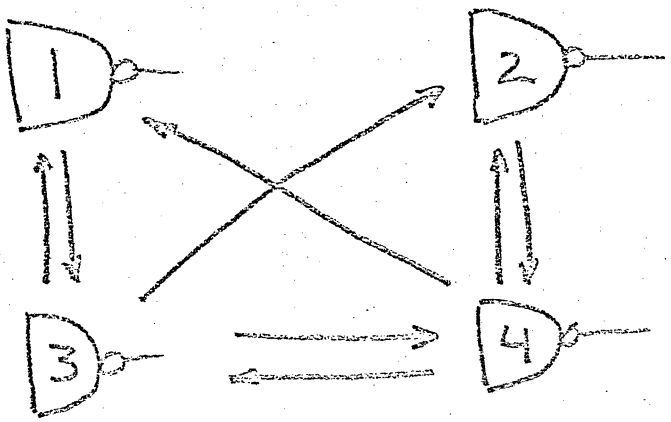


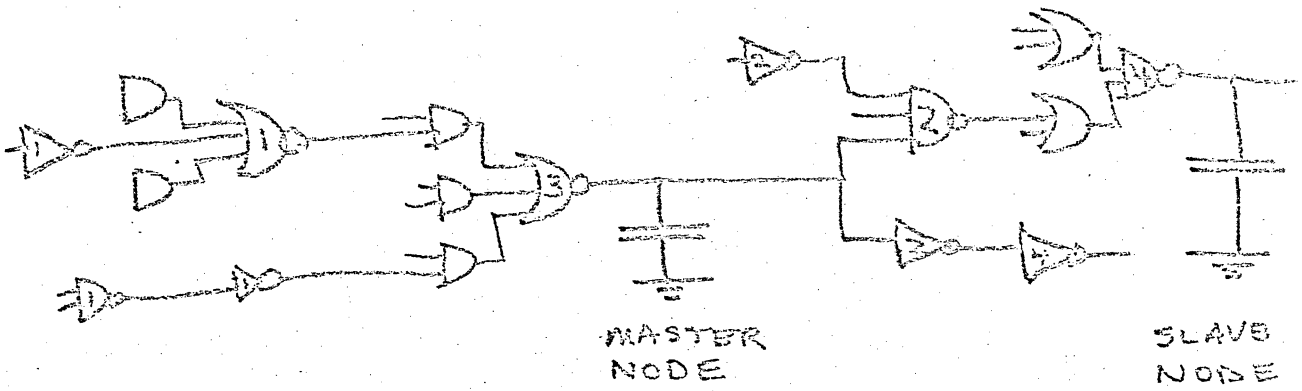


Two Phase Gate Structures



Two Phase Logic Flow Diagram

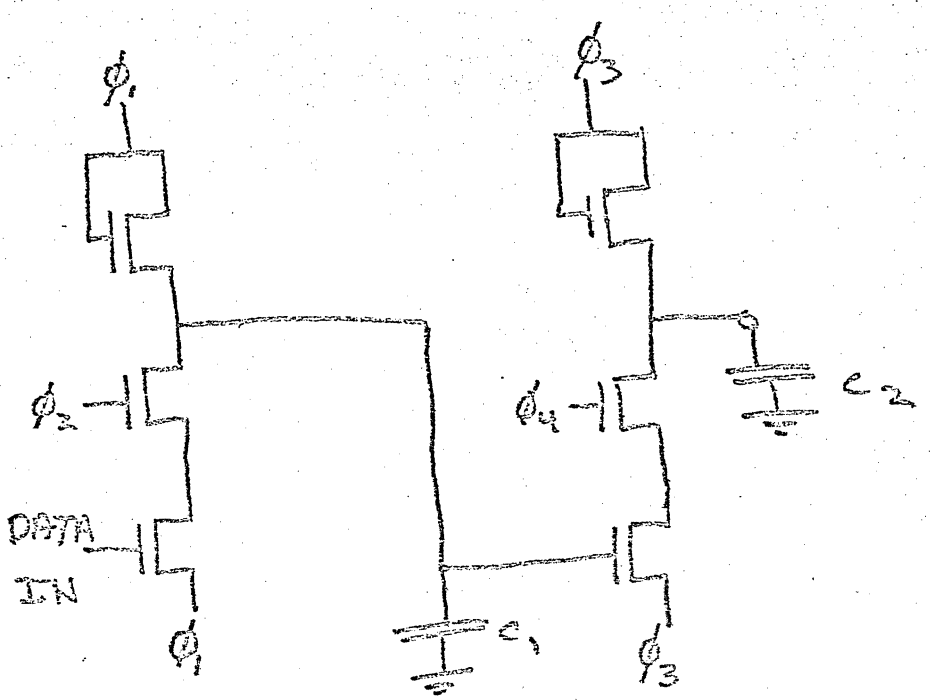


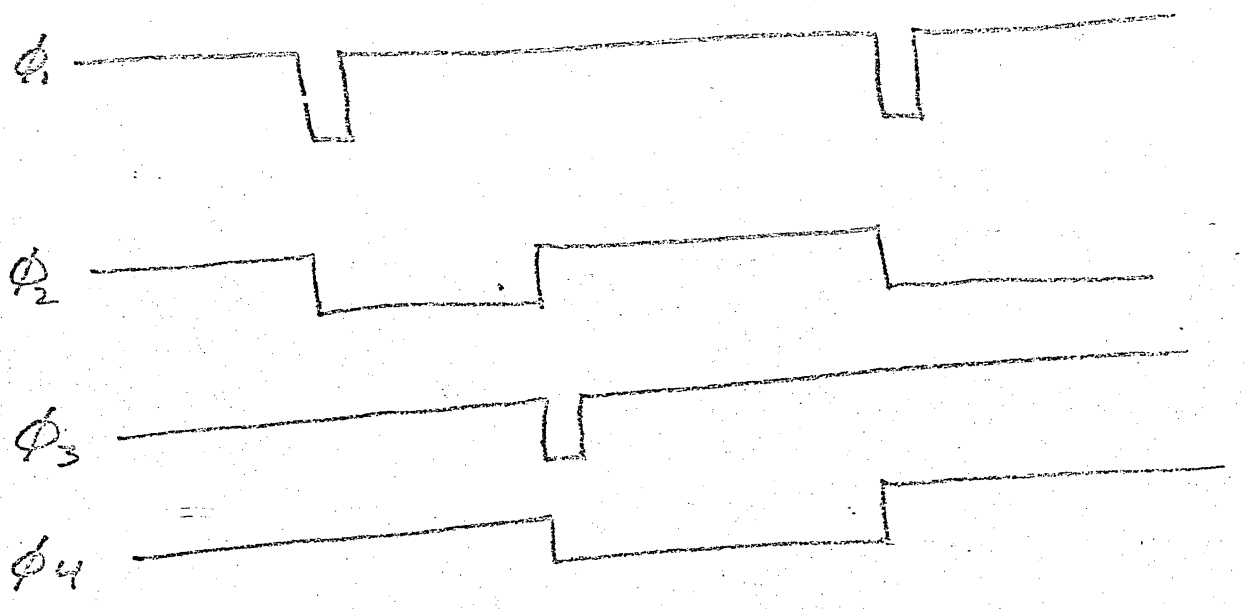


FOUR PHASE DYNAMIC LOGIC

Four Phase Operation

Shift Register Bit





FOUR PHASE GATES

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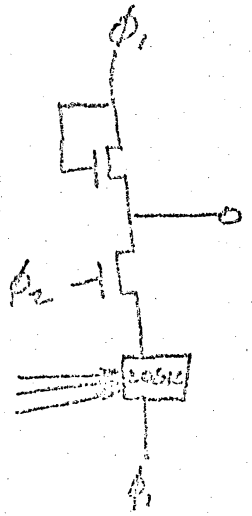

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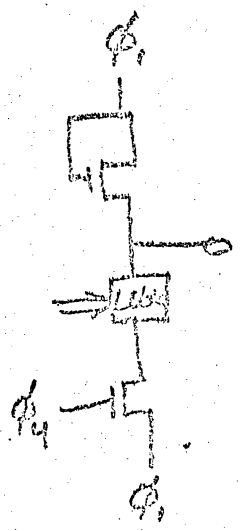

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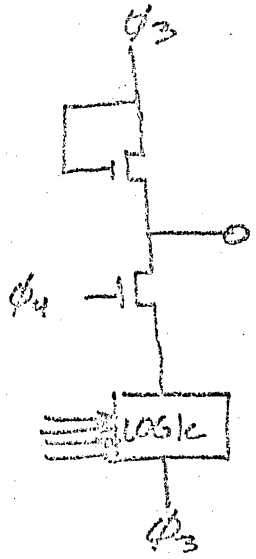

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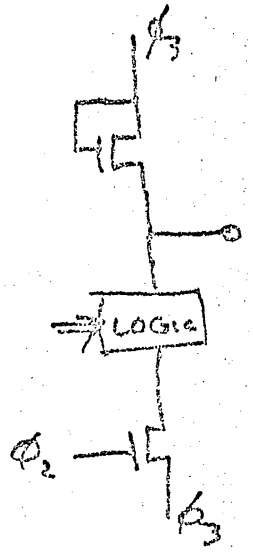
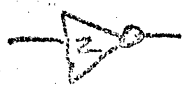
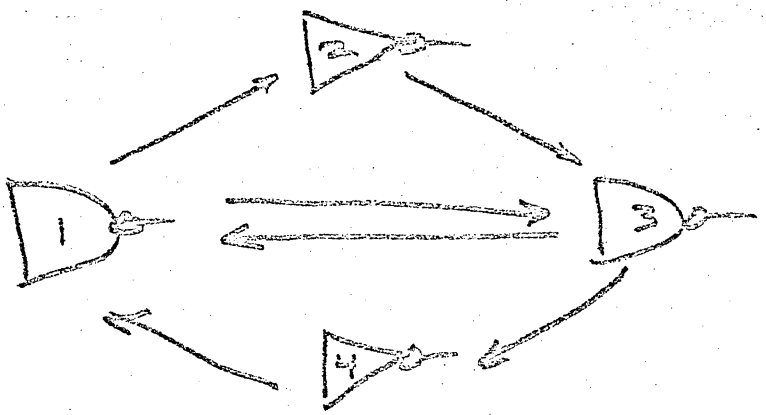
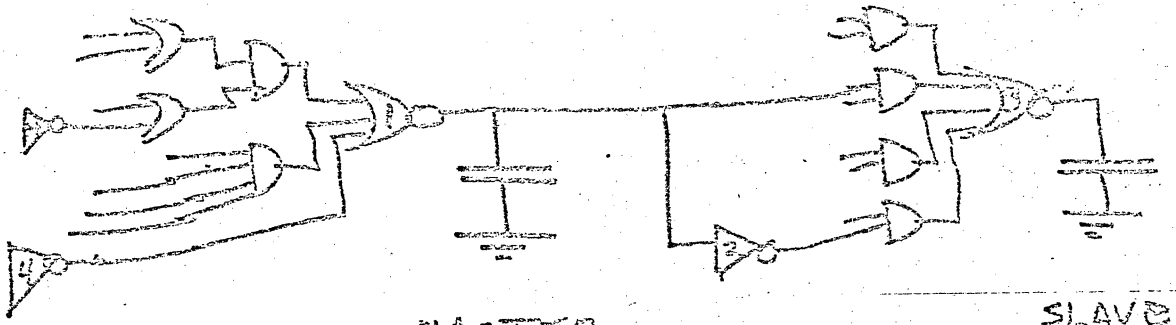




Four Phase Logic Flow Diagrams





MASTER NODE

SLAVE NODE

Static	2 Phase	4 Phase
DC – 3 MHz	5Kc – 2 MHz	10Kc – 10 Mc
Hi Power	Medium Power	Low Power
Large Area	Smaller Area	Smallest Area
Requires 1 clock	Requires 2 clocks	Requires 2 clocks
Requires 2 supplies	Requires 1 supply	Requires 1 supply
Asynchronous	Synchronous	Synchronous
Potential Race	No Race	No Race
Easy design	more difficult design	Very difficult design.