MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

Order this document
as AN449/D

AN449

An MC68340 to M88000 MBUS Bus Translator

By Dave McCartney
Highend Applications Group
Motorola Ltd, East Kilbride

INTRODUCTION

In a high performance processor system built around the M88000 family it makes sense to off-load many of the common I/O tasks to a dedicated I/O processor. This I/O processor is likely to be from a different family and therefore will use a different bus structure from that of the main processor system. Therefore some form of interface is required between the main processor bus system and the bus system of the I/O processor. This application note describes a circuit that can act as an interface between an M88000 type MBUS and the bus system of an I/O processor system based on the MC68340 which has an M68000 type asynchronous bus.

FUNCTIONAL DESCRIPTION

The function of this interface circuit is to translate all of the signal lines from the I/O processor to the type of signals required for an M88000 MBUS structure. The application is constructed from several PALs and standard TTL packages. The main section consists of a state machine built from a registered PAL. This is used to control the operation of the translator and allows for differing processor speeds and memory architectures. A block diagram of the full translator is shown in Figure 1. External connections via two 96 way DIN connectors are shown in Figure 1a. The translator consists of four main functional blocks as follows:

1. **ARBITER** — This block monitors the I/O processor's bus cycles until it detects a valid bus cycle from the I/O processor which indicates an access to memory on the MBUS. It then implements the standard MBUS bus arbitration protocol to gain control of the MBUS and signals the controller block once bus tenure has been obtained.

2. **CONTROLLER**—This block generates the seven bits of control information required by MBUS along with the parity bit for these control signals. In addition this block also generates the handshake signals to the I/O processor to terminate its bus cycles. It also generates some internal control signals for other parts of the bus translator.

3. **MUX** — This takes as input the 32-bit address bus and 16-bit data bus of the I/O processor and multiplexes them on to the 32-bit multiplexed address and data lines of the 88000 MBUS. The 16-bit data bus from the I/O processor is duplicated to produce a 32-bit data bus for the MBUS system.

4. **PARITY CHECKER** — This block generates the four parity bits during the address phase of all MBUS cycles and during the data phase of MBUS write cycles. In addition, this block checks for any parity errors during the data phase of all MBUS read cycles.

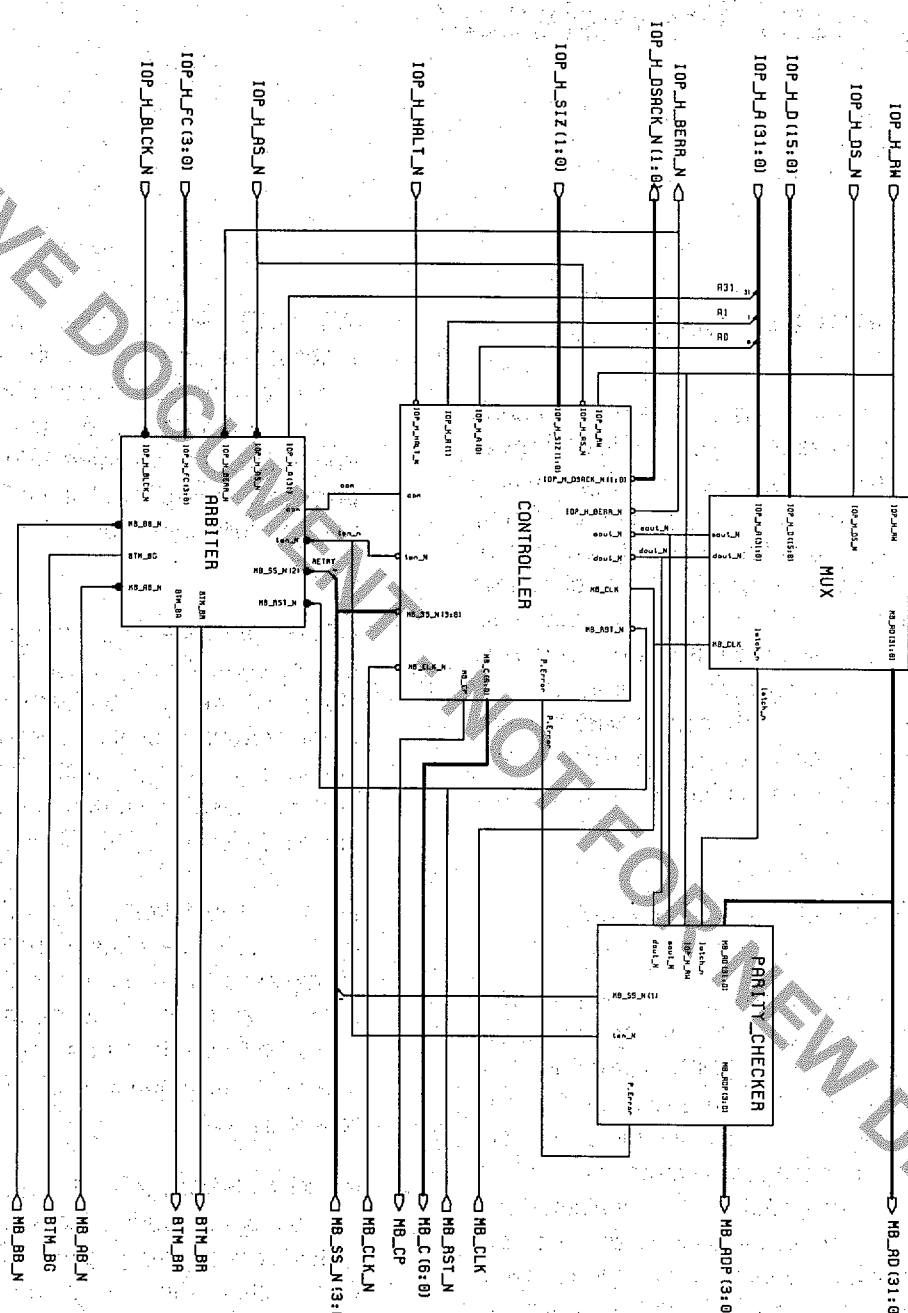

Figure 1. Top-level block diagram

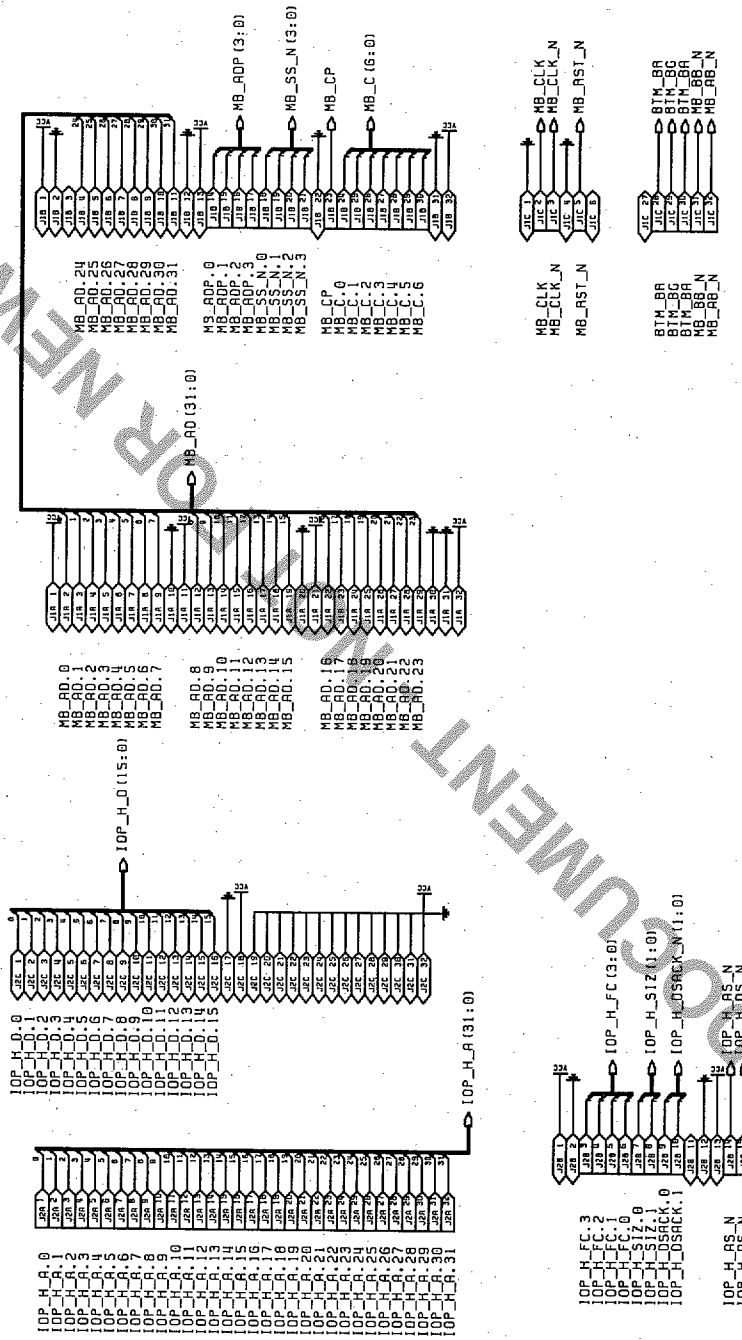

Figure 1a. External connections via two 96 way DIN connectors

CIRCUIT DESCRIPTION

ARBITER — This is implemented in a 18P8 PAL (U1) as shown in Figure 2. The PAL equations are given in the appendix (see BTM_ARBITER) and describe in detail the operation of this block.

CONTROLLER — This is implemented using two PALs (U2) and (U3) as shown in Figure 3. The 16R6 PAL implements a simple state machine to generate two control signals, AOUT and DOUT, plus the handshake signals to the I/O processor. The state diagram is shown in Figure 4. The 16L8 PAL generates the seven MBUS control signals and the parity bit for these signals. It uses the AOUT and DOUT control signals to signify which phase is currently being run on the MBUS. The PAL equations are given in the appendix (see BTM_CONTROLLER and BTM_HANDSHAKE) and describe the detailed operation.

MUX — This block contains buffers and latches on the address and data buses of the I/O processor which allow them to be multiplexed onto one 32-bit bus on the MBUS, as shown in Figure 5. The buffers U5, U6, U7 and U21 are used to buffer the I/O processor's 32-bit address bus to the MBUS address and data lines. The output enable of these buffers is controlled by the AOUT control signal produced by the Controller block. The latched buffers U8, U9, U10 and U11 are used to buffer the 16-bit data bus from the I/O processor and multiplex it onto the MBUS address and data lines. Since the I/O processor's data bus is only 16 bits wide it is duplicated to produce a 32-bit bus on the MBUS side of the translator. During I/O processor read cycles the data on the MBUS side is valid only during rising MBUS clock edges. The latching capabilities of the 74FCT652 devices are used to sample the data on the clock edge and supply the appropriate 16 bits to the I/O processor. The PAL (U4) takes as input the internal DOUT signal produced by the Controller sub-block and uses this with the I/O processor's read/write signal to derive control signals for the latches and output enables for the data buffers. The PAL equations are given in the appendix (see MUX_CONTROLLER). This PAL also produces a latch enable signal which is fed to the Parity Checker sub-block.

PARITY CHECKER — This optional sub-block performs the function of generating the four MBUS parity bits during all address phases and during data phases of MBUS write cycles. These parity bits are then driven out on the parity lines defined by MBUS. During the data phase of an MBUS read transaction this block samples the parity bits from the MBUS slave and again generates parity based on the data from the slave. It then compares the generated parity with the sampled values from the slave and signals any error to the Controller sub-block. The circuit diagram of this block is shown in Figure 6. To minimise the number of parity generator devices used in the design all the parity generation is done only on the multiplexed MBUS address and data lines. U12, U13, U14 and U15 are transparent latches which are used to sample the data during MBUS read cycle data phases. The outputs of these latches are fed into U16, U17, U18 and U19 parity generator devices to produce the four parity bits. These bits are then buffered through one half of U21 to the MBUS parity lines. The PAL (U20) generates the output enable signal for the U21 buffer to turn it on only during address phases and the data phases of MBUS write cycles. The latch (U22) is used to sample the four parity bits during an MBUS read and then feed these to the PAL. The comparison between the generated parity and the sampled parity is performed in the PAL and an error signal called P.Error is generated for any comparison that fails. This is used in the Controller sub-block to force an early termination of the bus transaction. The PAL equations for U20 are given in the appendix (see PARITY_CHECKER). In any systems where parity is not considered to be an important feature this Parity Checker sub-block can be omitted from the design and the P.Error input to the Controller sub-block would then be pulled high (to its negated state).

COMPONENTS LIST

U1	PAL18P8	U12	74F373
U2	PAL16L8	U13	74F373
U3	PAL16R6	U14	74F373
U4	PAL16L8	U15	74F373
U5	74F827	U16	74F280
U6	74F827	U17	74F280
U7	74F827	U18	74F280
U8	74FCT652	U19	74F280
U9	74FCT652	U20	PAL16L8
U10	74FCT652	U21	74F244
U11	74FCT652	U22	74F373

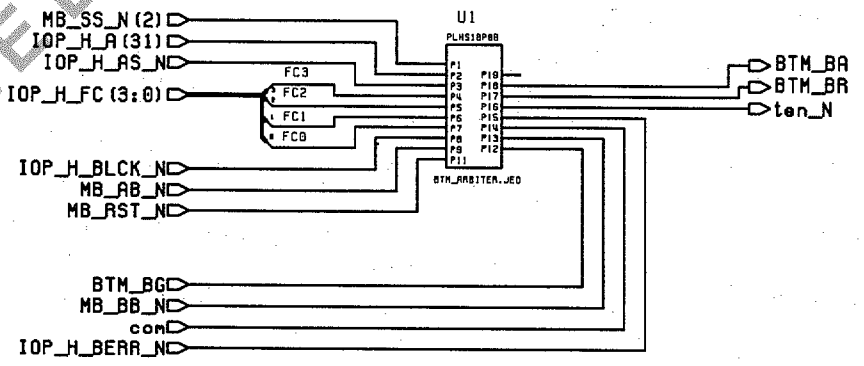

Figure 2. Schematic of ARBITER block

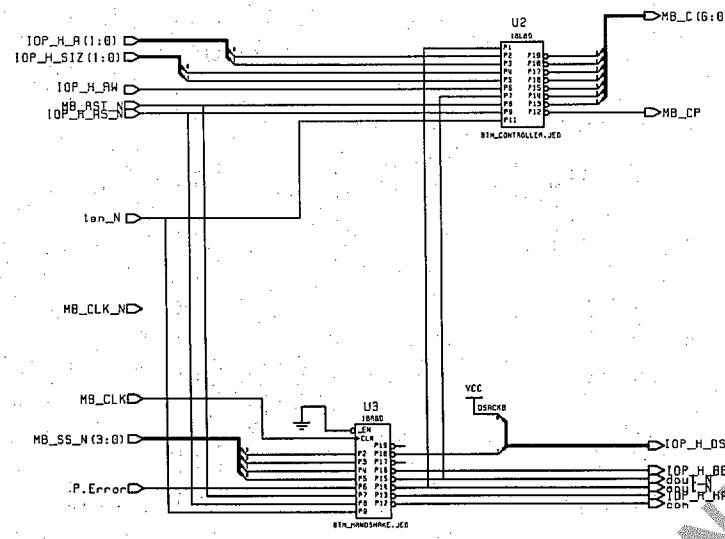

Figure 3. Schematic of CONTROLLER block

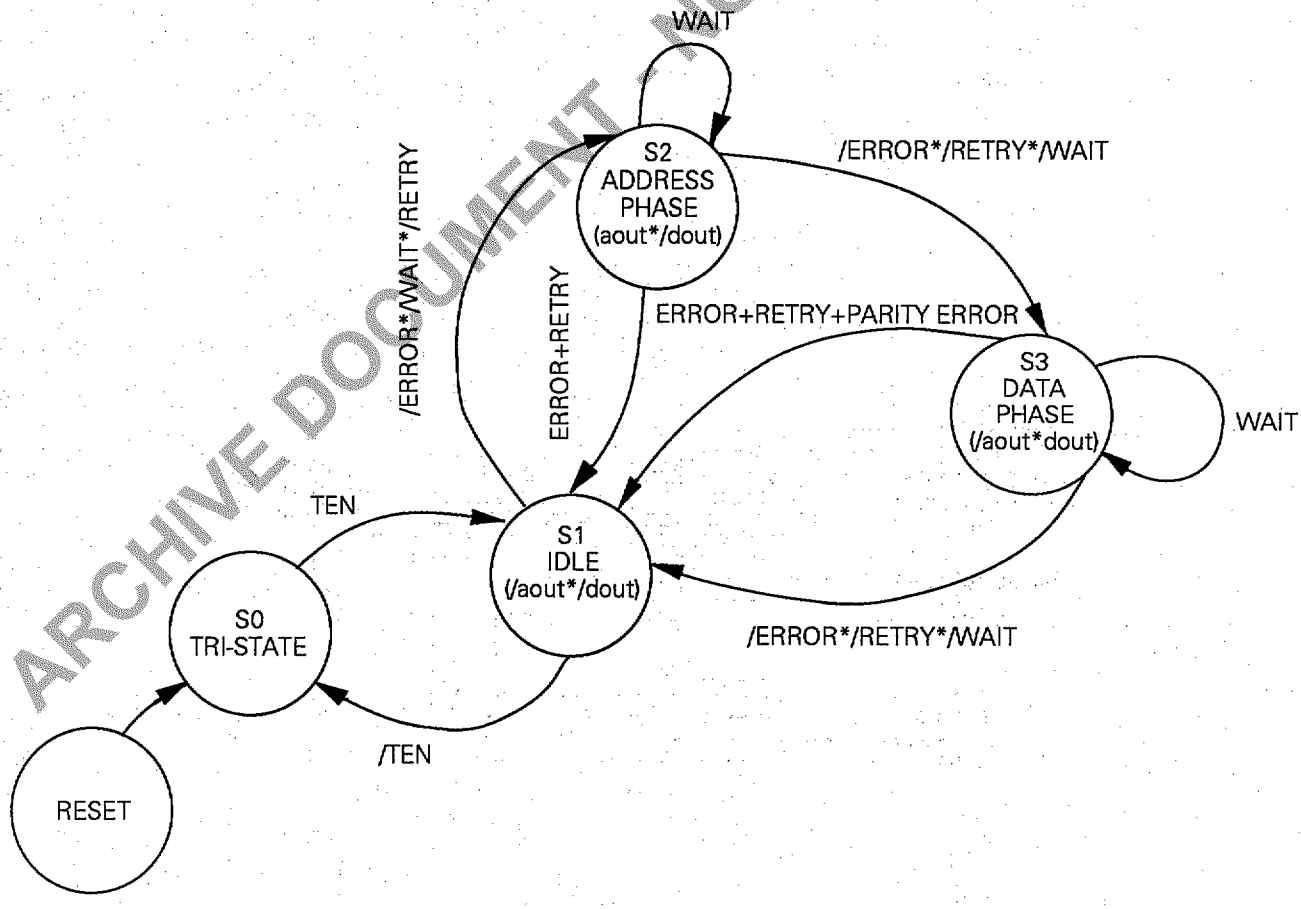

Figure 4. State diagram of CONTROLLER block

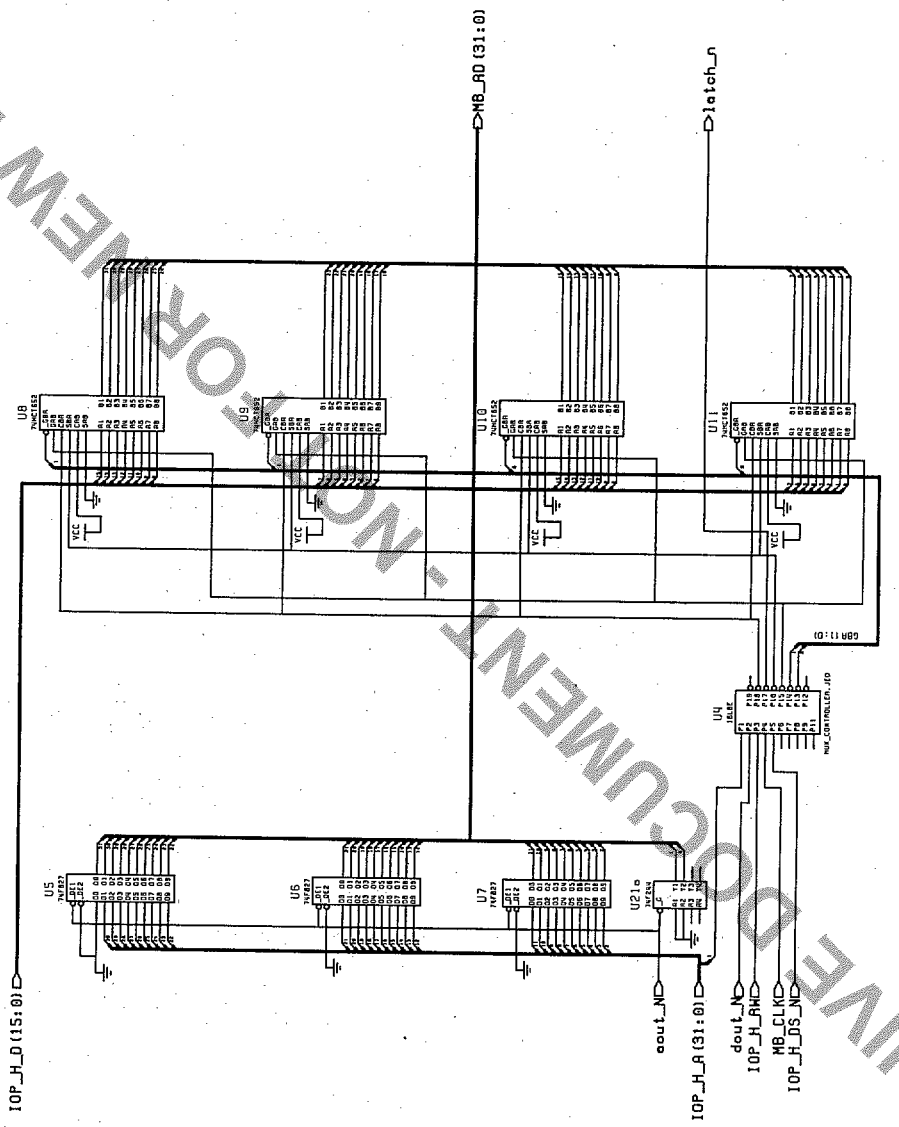

Figure 5. Schematic of MUX block

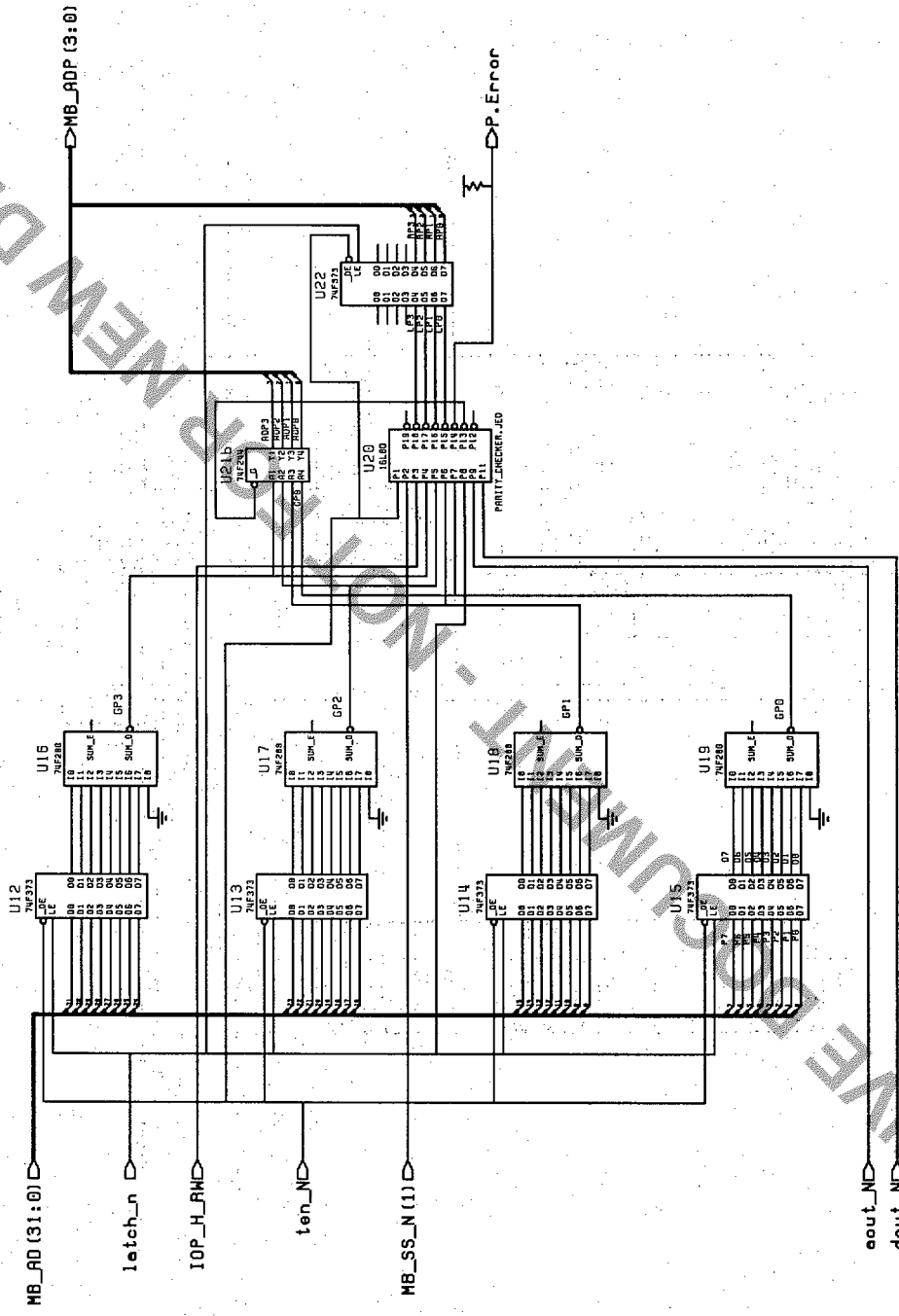

Figure 6. Schematic of PARITY CHECKER block

APPENDIX

This appendix contains the full source listings of the PAL equations used in this design. These source listings are shown in PALASM syntax as defined by AMD.

U1 - 18P8B - BTM_ARBITER

```
TITLE       BTM_ARBITER
PATTERN     BTM_A001
REVISION    1.0
AUTHOR      Dave McCartney
COMPANY     MOTOROLA EKB
DATE        14th December 1989

CHIP        BTM_ARBITER         PAL18P8

;This PAL implements the ARBITER sub-block of the MBIOPBTM module. It monitors the IOP bus until
;it detects a Data address space bus cycle with A31= 1. The PAL then monitors the MBUS
;arbitration signals and generates a Bus Request to the MBUS Arbiter. On receipt of a Bus Grant
;it asserts the BA signal which is reflected in the MBUS BB signal. It then negates
;the Bus Request. The internal Bus Tenure signal TEN is generated for the controller sub-block
;and then the PAL waits for the internal Transaction Complete signal COM.
;This terminates the bus tenure and negates the BA signal for this module.

;                        PIN DEFINITIONS
;PINS   1      2    3     4     5     6     7     8      9     10
       /RETRY  A31  /AS   FC3   FC2   FC1   FC0  /BLCK  /AB    GND

;PINS  11     12   13    14    15    16    17    18     19     20
       /RST   BG  /BB   COM  /BERR /TEN   BR    BA     NC     VCC

;PIN 1 = /RETRY = MBUS System Status Line 2          MB_SS_N(2)
;PIN 2 = A31 = Address line A31 from the IOP         IOP_H_A(31)
;PIN 3 = /AS = Address strobe from the IOP           IOP_H_AS_N
;PIN 4 = FC3 = Function code 3 from the IOP          IOP_H_FC(3)
;PIN 5 = FC2 = Function code 2 from the IOP          IOP_H_FC(2)
;PIN 6 = FC1 = Function code 1 from the IOP          IOP_H_FC(1)
;PIN 7 = FC0 = Function code 0 from the IOP          IOP_H_FC(0)
;PIN 8 = /BLCK = Bus lock signal from the IOP        IOP_H_BLCK_N
;PIN 9 = /AB = MBUS Arbitration Busy Signal          MB_AB_N
;PIN 11 = /RST = MBUS Reset Signal                   MB_RST_N
;PIN 12 = BG = Bus Grant Signal from MBUS Arbiter    BTM_BG
;PIN 13 = /BB = MBUS Bus Busy Signal                 MB_BB_N
;PIN 14 = COM = Transaction Complete Internal Signal
;PIN 15 = /BERR = Bus Error Signal from the IOP      IOP_H_BERR_N
;PIN 16 = /TEN = Bus Tenure Internal Signal
;PIN 17 = BR = Bus Request Signal to MBUS Arbiter   BTM_BR
;PIN 18 = BA = Bus Acknowledge to MBUS Arbiter      BTM_BA

;Internal Bus Tenure signal /TEN is used to enable main controller sub-block when the MBIOPBTM has
;gained control of the MBUS. Internal Transaction Complete signal /COM is generated by the
;controller sub-block to terminate a bus tenure.

;           Boolean Equations

EQUATIONS

BR.TRST = VCC
BR=A31*/FC1*FC0*AS*/RETRY*/TEN*/COM*/BA*/BERR*/RST          ; Generate Bus Request

BA.TRST = VCC
BA=BG*/BB*/RST+BA*/COM*/RETRY*/RST+BA*BLCK*/RETRY*/RST      ; Generate Bus Acknowledge

TEN.TRST = VCC
TEN=BA*/COM*/RETRY*/RST                                     ; Generate bus tenure once bus is obtained

SIMULATION
```

U2 - 16L8B - BTM_CONTROLLER

```
TITLE       BTM_CONTROLLER
PATTERN     BTM_C001
REVISION    1.0
AUTHOR      Dave McCartney
COMPANY     MOTOROLA EKB
DATE        28th November 1989

CHIP         BTM_CONTROLLER          PAL16L8

;This PAL generates the 7-bit MBUS Control bus and the Parity bit for
;this control bus. It generates the control bus signals for three
;distinct phases, namely IDLE, ADDRESS and DATA. The tristate control
;for all the PAL outputs is connected to the internal Bus Tenure signal
;TEN generated by the Arbiter sub-block. The PAL output phase is
;determined by the state of two internal signals AOUT and DOUT which
;are generated by the BTM Handshake PAL.

;           PIN DEFINITIONS
;PINS   1      2     3     4      5      6      7       8      9      10
     /AOUT    A0    A1    SIZ0   SIZ1   R_W   /DOUT   /RESET   /AS    GND

;PINS  11     12    13    14     15     16     17      18     19     20
     /TEN     CP    C6    C5     C4     C3     C2      C1     C0     VCC

;PIN 1 = /AOUT = Internal signal indicating Address Phase
;PIN 2 = A0 = Address line A0 from the IOP IOP_H_A(0)
;PIN 3 = A1 = Address line A1 from the IOP IOP_H_A(1)
;PIN 4 = SIZ0 = Size 0 line from the IOP IOP_H_SIZ(0)
;PIN 5 = SIZ1 = Size 1 line from the IOP IOP_H_SIZ(1)
;PIN 6 = R_W = Read/write line from the IOP IOP_H_RW
;PIN 7 = /DOUT = Internal signal showing Data Phase
;PIN 8 = /RESET = MBUS Reset Signal MB_RST_N
;PIN 9 = /AS = Address Strobe from the IOP IOP_H_AS_N
;PIN 11 = /TEN = Bus Tenure Internal Signal
;PIN 12 = CP = Parity bit for MBUS Control Signals MB_CP
;PIN 13 = C6 = MBUS Control Signal 6 MB_C(6)
;PIN 14 = C5 = MBUS Control Signal 5 MB_C(5)
;PIN 15 = C4 = MBUS Control Signal 4 MB_C(4)
;PIN 16 = C3 = MBUS Control Signal 3 MB_C(3)
;PIN 17 = C2 = MBUS Control Signal 2 MB_C(2)
;PIN 18 = C1 = MBUS Control Signal 1 MB_C(1)
;PIN 19 = C0 = MBUS Control Signal 0 MB_C(0)

;The internal signals AOUT and DOUT are generated by the BTM_Handshake
;PAL and the internal TEN signal comes from the BTM_Arbiter PAL


;           Boolean Equations

EQUATIONS

C0.TRST = TEN                       ;Enable output during MBUS Tenure
C0 = AOUT*/DOUT*/RESET              ;Only assert during Address Phase

C1.TRST = TEN                       ;Enable output during MBUS Tenure
C1 = /AOUT*DOUT*/RESET              ;Shows LDT during Data Phase

C2.TRST = TEN                       ;Enable output during MBUS Tenure
C2 = /AOUT*/DOUT*/RESET             ;Assert as Read during Idle Phase
    +AOUT*/DOUT*R_W*/RESET          ;Assert during Address Phase for Reads
    +/AOUT*DOUT*R_W*/RESET          ;Assert during Data Phase for Reads

C3.TRST = TEN                                   ;Enable output during MBUS Tenure
C3 = /AOUT*DOUT*AS*/RESET*/A0*/A1*SIZ0*/SIZ1    ;Byte transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A0*/A1*/SIZ0*SIZ1    ;Word transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A0*/A1*SIZ0*SIZ1     ;3 Byte transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A0*/A1*/SIZ0*/SIZ1   ;Long Word transfer Data Phase
```

```
C4.TRST = TEN                                   ;Enable output during MBUS Tenure
C4 = /AOUT*DOUT*AS*/RESET*A0*/A1*SIZ0*/SIZ1     ;Byte transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A1*/SIZ0*SIZ1        ;Word transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A1*SIZ0*SIZ1         ;3 Byte transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A1*/SIZ0*/SIZ1       ;Long Word transfer Data Phase

C5.TRST = TEN                                   ;Enable output during MBUS Tenure
C5 = AOUT*/DOUT*AS*/RESET                       ;Global flag Address Phase
    +/AOUT*DOUT*AS*/RESET*/A0*A1*SIZ0*/SIZ1     ;Byte transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A0*A1*/SIZ0*SIZ1     ;Word transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A0*A1*SIZ0*SIZ1      ;3 Byte transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*/A0*A1*/SIZ0*/SIZ1    ;Long Word transfer Data Phase

C6.TRST = TEN                                   ;Enable output during MBUS Tenure
C6 = /AOUT*DOUT*AS*/RESET*A0*A1*SIZ0*/SIZ1      ;Byte transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*A1*/SIZ0*SIZ1         ;Word transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*A1*SIZ0*SIZ1          ;3 Byte transfer Data Phase
    +/AOUT*DOUT*AS*/RESET*A1*/SIZ0*/SIZ1        ;Long Word transfer Data Phase

CP.TRST = TEN                                   ;Enable output during MBUS Tenure
/CP = AOUT*/DOUT*/R_W                           ;address Phase Write
     +/AOUT*DOUT*/R_W*SIZ0*/SIZ1                ;data Phase Write Byte
     +/AOUT*DOUT*R_W*/SIZ0*SIZ1                 ;data Phase Read Word
     +/AOUT*DOUT*R_W*SIZ0*SIZ1                  ;data Phase Read 3 Byte
     +/AOUT*DOUT*R_W*/SIZ0*/SIZ1                ;data Phase Read Long Word

SIMULATION
```

U3 - 16R6D - BTM_HANDSHAKE

```
TITLE       BTM_HANDSHAKE
PATTERN     BTM_H001
REVISION    1.0
AUTHOR      Dave McCartney
COMPANY     MOTOROLA EKB
DATE        12th December 1989

CHIP        BTM_HANDSHAKE              PAL16R6

;This PAL generates the handshake signals to the IOP to terminate the
;IOP bus cycles. These include DSACK1 (16-bit port size),BERR and HALT.
;It also generates the AOUT and DOUT signals to signify what state the
;MBUS is in and it generates a transaction complete COM signal which
;is used by the Arbiter to terminate bus tenure. The PAL operates as
;a state machine which is clocked by the main MBUS system clock and
;implements 3 distinct phases for MBUS :-
;
;           IDLE PHASE              AOUT negated and DOUT negated
;           ADDRESS PHASE           AOUT asserted and DOUT negated
;           DATA PHASE              AOUT negated and DOUT asserted
;
;On gaining MBUS tenure the state machine shows an idle phase until the
;first rising clock edge when it moves into address phase. It will stay
;in this phase until an O.K. status is seen on the MBUS system status lines.
;The machine then moves into Data phase and again waits for an O.K. before
;returning to Idle phase where it waits until MBUS tenure is relinquished.

;           PIN DEFINITIONS

;PINS   1      2      3      4      5      6       7       8       9     10
     CLOCK   /SS3   /SS2   /SS1  /SS0   /PE   /RESET  /AS   /TEN   GND

;PINS  11     12     13     14     15      16   17    18         19     20
      /OE    COM   /HALT  /AOUT  /DOUT  /BERR  NC  /DSACK1C  /DSACK1  VCC

;PIN 1 = CLOCK = MBUS system clock                          MB_CLK
;PIN 2 = /SS3 = MBUS System Status line 3 (Error)           MB_SS_N(3)
;PIN 3 = /SS2 = MBUS System Status line 2 (Retry)           MB_SS_N(2)
;PIN 4 = /SS1 = MBUS System Status line 1 (Wait)            MB_SS_N(1)
;PIN 5 = /SS0 = MBUS System Status line 0 (EOD)             MB_SS_N(0)
;PIN 6 = /PE = Internal Parity Error Signal
;PIN 7 = /RESET = MBUS Reset Signal                         MB_RST_N
;PIN 8 = /DS = Address Strobe from the IOP                  IOP_H_AS_N
;PIN 9 = /TEN = Bus Tenure Internal Signal
;PIN 11 = /OE = Active low output enable control
;PIN 12 = COM = Internal Transaction Complete Signal
;PIN 13 = /HALT = HALT handshake to the IOP                 IOP_H_HALT_N
;PIN 14 = /AOUT = Internal Signal showing Address phase
;PIN 15 = /DOUT = Internal Signal showing Data phase
;PIN 16 = /BERR = BERR handshake to the IOP                 IOP_H_BERR_N
;PIN 18 = /DSACK1C = clocked version of DSACK1 to IOP       (Not Connected)
;PIN 19 = /DSACK1 = DSACK1 handshake to IOP (uses pin 18)   IOP_H_DSACK_N(1)

;The internal PE signal is generated by the parity checker block and the
;internal bus tenure signal TEN is generated by the Arbiter block. The
;transaction complete signal COM is an output which is used by the Arbiter
;to terminate the MBUS tenure. The AOUT and DOUT signals are used to
;produce to MBUS control signals C(6:0) and are used by the multiplexer
;block to control the information placed on the MBUS AD(31:0) lines.
;
;For a normal bus cycle this PAL will generate a normal DSACK handshake
;to the IOP. A cycle which results in an error on the MBUS system status
;lines gives a BERR handshake to the IOP. A retry cycle forces a retry
;handshake by the assertion of HALT and BERR to the IOP, and MBUS tenure
;is terminated early. A detected Parity error during the data phase of
;an MBUS read cycle results in a Late Bus Error Handshake to the IOP
;following the normal DSACK termination.
```

```
;           Boolean Equations

EQUATIONS

HALT:= SS2*AS*/RESET                ;Assert if RETRY is valid
       +HALT*AS*/RESET              ;HOLD till AS negates

DOUT:= AOUT*/DOUT*AS*/RESET*TEN     ;Change to Data Phase if
       */SS1*/SS2*/SS3*/PE          ;no error detected
       +DOUT*AS*SS1*/RESET*TEN      ;Hold if WAIT detected

AOUT:= /AOUT*/DOUT*AS*/RESET*TEN*/DSACK1      ;Enter Address Phase
       */SS1*/SS2*/SS3*/PE                    ;if no error detected
       +AOUT*AS*SS1*/RESET*TEN                ;Hold if WAIT detected

COM = /AS*/RESET*TEN                ;Assert when IOP AS negates to terminate tenure
     +SS3*/RESET*TEN                ;Assert if ERROR asserted to terminate tenure
     +SS2*/RESET*TEN                ;Assert if RETRY asserted to terminate tenure

BERR := SS3*AS*/RESET*TEN           ;Assert if ERROR detected
       +SS2*AS*/RESET               ;Assert if RETRY detected
       +PE*AS*DSACK1*/RESET*TEN     ;Assert if Parity Error detected
       +BERR*AS*/RESET              ;Hold till AS negates

DSACK1 = DSACK1C*AS*/BERR           ;Assert DSACK after clock edge
                                    ;Negate when AS negates
                                    ;or BERR asserts

DSACK1C :=/AOUT*DOUT*AS*/RESET*TEN  ;Assert at end of Data Phase
         */SS3*/SS2*/SS1            ;if no errors or wait asserted
         +DSACK1*AS*/RESET*TEN      ;Hold till AS negates

SIMULATION
```

U4 - 16L8E - MUX_CONTROLLER

```
TITLE       MUX_CONTROLLER
PATTERN     MUX_C001
REVISION    1.0
AUTHOR      Dave McCartney
COMPANY     MOTOROLA EKB
DATE        18th December 1989

CHIP        MUX_CONTROLLER          PAL16L8

;This PAL generates the control signals required to operate 74FCT652
;bus transceivers during the data phase of every MBUS cycle when the
;module has been granted MBUS tenure. These control signals consist
;of output enables for data flow in either direction, a signal which
;selects either real time or stored data and a signal which controls
;the data latches inside the 75FCT652 devices. In addition a second
;latch control signal is generated which is used by the Parity Checker
;block to hold data coming from an MBUS slave.

;           PIN DEFINITIONS

;PINS  1     2     3     4     5     6     7     8     9     10
      A1   /DOUT  R_W   CLK   /DS    NC    NC    NC    NC    GND

;PINS 11    12    13    14    15    16    17    18    19    20
      NC    NC  /GBA0  /GBA1  GAB   SBA  /LATCH  CBA   NC    VCC

;PIN 1 = A1 = Address line A1 from the IOP IOP_H_A(1)
;PIN 2 = /DOUT = Internal Signal Showing Data phase
;PIN 3 = R_W = Read/Write line from the IOP IOP_H_RW
;PIN 4 = CLK = MBUS System Clock MB_CLK
;PIN 5 = /DS = Data Strobe from the IOP IOP_H_DS_N
;PIN 13 = /GBA0 = Transceiver Enable B to A direction
;PIN 14 = /GBA1 = Transceiver Enable B to A direction
;PIN 15 = GAB = Transceiver Enable A to B direction
;PIN 16 = SBA = Real time or Stored data Select for B to A
;PIN 17 = /LATCH = Latch signal used by Parity Checker
;PIN 18 = CBA = Use to latch data into internal latches

;All of the above internal signals generated by the PAL are fed
;directly to the appropriate control inputs on the 74FCT652 devices.


;           Boolean Equations

EQUATIONS

GBA0.TRST = VCC                     ;Output always enabled
GBA0 = DOUT*R_W*A1*/GBA1*/GAB       ;Assert for A1=1 for a read
      +GBA0*DS                      ;Hold till DS negates

GBA1.TRST = VCC                     ;Output always enabled
GBA1 = DOUT*R_W*/A1*/GBA0*/GAB      ;Assert for A1=0 for a read
      +GBA1*DS                      ;Hold till DS negates

GAB.TRST = VCC                      ;Output always enabled
GAB = DOUT*/R_W*/GBA0*/GBA1         ;Assert for writes

CBA.TRST = VCC                      ;Output always enabled
/CBA = DOUT*R_W*/CLK                ;Negate during read and low clock

SBA.TRST = VCC                      ;Output always enabled
/SBA = DOUT*R_W*/CLK                ;Real time during read and low clock

LATCH.TRST = VCC                    ;Output always enabled
LATCH = DOUT*R_W*CLK                ;Asserted at end of data phase
       +LATCH*CBA*DS                ;Hold till DS negates

SIMULATION
```

U20 - 16L8D - PARITY_CHECKER

```
TITLE       PARITY_CHECKER
PATTERN     PARITY_P001
REVISION    1.0
AUTHOR      Dave McCartney
COMPANY     MOTOROLA EKB
DATE        16th January 1990

CHIP        PARITY_CONTRL          PAL16L8

;This PAL is used to compare the four parity bits from the parity
;generators with the four bits read from an MBUS slave and generates
;a parity error if they do not agree. This check is only done on
;the data phase of read cycles.

;           PIN DEFINITION
;PINS  1     2      3      4     5     6      7      8       9      10
     /TEN  /WAIT   R_W    GP3   GP2   GP1    GP0   LATCH   /AOUT   GND

;PINS 11     12     13     14     15    16    17     18       19     20
    /DOUT    NC    /OC    /PE    LP0   LP1   LP2    LP3       NC    VCC

;PIN 1 = /TEN = Bus Tenure Internal Signal
;PIN 2 = /WAIT = MBUS System Status line 1 MB_SS_N(1)
;PIN 3 = R_W = Read/Write line from the IOP IOP_H_RW
;PIN 4 = GP3 = Generated parity bit 3
;PIN 5 = GP2 = Generated parity bit 2
;PIN 6 = GP1 = Generated parity bit 1
;PIN 7 = GP0 = Generated parity bit 0
;PIN 8 = LATCH = Internal latch control signal
;PIN 9 = /AOUT = Internal signal showing address phase
;PIN 11 = /DOUT = Internal signal showing data phase
;PIN 13 = /OC = Output Control Signal for parity bits
;PIN 14 = /PE = Internal Parity Error Signal
;PIN 15 = LP0 = Latched read parity bit 0
;PIN 16 = LP1 = Latched read parity bit 1
;PIN 17 = LP2 = Latched read parity bit 2
;PIN 18 = LP3 = Latched read parity bit 3

;The internal output control signal OC is used to control a four-bit
;tri-state buffer which allows the generated parity bits to be driven
;out on the ADP bus during the data phase of write cycles. The internal
;LATCH control signal is the signal used to latch the data and parity bits
;during read cycles and is used by the PAL to enable the parity checking.
;For a fault during parity checking the PAL generates the active low
;Parity Error signal (/PE) which is detected by the controller block and
;a bus error is returned to the IOP.


;           Boolean Equations

EQUATIONS

OC.TRST = VCC                          ;Output always enabled
OC = TEN*/R_W                          ;Valid for all write cycles
   +TEN*R_W*AOUT*/DOUT                 ;or address phase of reads

PE.TRST = VCC                          ;Output always enabled
PE = GP0*/LP0*R_W*/WAIT*/OC*/LATCH     ;Is GP0=LP0 during read
     +GP1*/LP1*R_W*/WAIT*/OC*/LATCH    ;or GP1=LP1
     +GP2*/LP2*R_W*/WAIT*/OC*/LATCH    ;or GP2=LP2
     +GP3*/LP3*R_W*/WAIT*/OC*/LATCH    ;or GP3=LP3

SIMULATION
```

Literature Distribution Centres:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
ASIA PACIFIC: Motorola Semiconductors (H.K.) Ltd.; Silicon Harbour Center, No. 2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

MOTOROLA

Printed in Great Britain by Tavistock Press (Bedford) Ltd. 4500 9/91 PO.2097