DL413/D
REV 1

Radio, RF and Video Applications

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Radio, RF and Video Applications

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Preface

This compilation of Application Notes, Engineering Bulletins, Design Concepts, etc. was originally published by the European Literature Centre of Motorola Ltd. in Milton Keynes, England, and has subsequently gained worldwide acceptance.

Because of the worldwide popularity of the Application Manuals Series it is important for the reader to take note of the following:

The various Application Notes, Engineering Bulletins, Design Concepts, etc. which are included were developed at Design Centres strategically located throughout the global community and many were originally written to support a local need. Whilst the basic concepts of each of the publications included may have broad global applicability, specific Motorola semiconductor parts may be referred to that are currently available for limited distribution in a specific region and may only be supported by the country of origin of the document in which it is referenced.

Also included in the series for completeness and historical significance are documents that may no longer be available individually because obsolete devices are referenced or perhaps, simply, the original document is out of print. Such items are marked in the Table of Contents, Cross Reference, Abstracts and on the first page of the document with the letters '**HI**' to indicate that these documents are included for Historical Information only.

All the Application Notes, Engineering Bulletins, Design Concepts, etc. are included to enhance the user's knowledge and understanding of Motorola's products. However, before attempting to design-in a device referenced in this Series, the user should contact the local Motorola supplier or sales office to confirm product availability and if application support is available.

Thank you.

Other books in this series include:

DL408/D Rev. 1	*8-bit MCU Applications Manual*
DL409/D Rev. 1	*16/32-bit Applications Manual*
DL410/D Rev. 1	*Power Applications Manual*
DL411/D Rev. 1	*Communications Applications*
DL412/D Rev. 1	*Industrial Control Applications*
DL414/D	*FET Applications Manual*

Contents

Contents (continued)

Device Cross Reference

Device Cross Reference

This quick-reference list indicates where specific components are featured in applications documents reproduced in this Manual.

Abstracts of Applications Documents

Abstracts

AN438 300W, 88–108MHz Amplifier Using the TP1940 MOSFETs Push-Pull Transistor

Provides the design of an efficient 300W amplifier with high power gain, compact physical layout and operation on a 50V power supply. It uses the TP1940, a high power, high gain, broadband push-pull Power MOSFET with low Reverse Transfer Capacitance. Includes circuit, parts list, PCB artwork and component layout.

AN448 "FLOF" Teletext using M6805 Microcontrollers

The "-T" members of Motorola's M68HC05 MCU family provide a cost-effective method of adding On Screen Display (OSD) to TVs and VCRs. This note describes an example of Full Level One Feature (FLOF) Teletext control software written for the MC68HC05T7 to control type 5243 Teletext chips. Around 3K bytes of ROM are used, allowing the code to fit with tuning, OSD and stereo functions into the 7.9K bytes of the MC68HC05T7. The example software includes the Spanish implementation of Packet 26; Packet 26 allows for the substitution of specific characters for a particular country.

AN460 An RDS Decoder Using the MC68HC05E0

The Radio Data System (RDS) adds digital data capability to VHF FM transmissions on band II (87.5 to 108MHz). The system is in use in the UK and in several other European countries, and it is intended that it will be adopted eventually by most of Western Europe; it is defined by EBU Technical Document 3244. Information is transmitted in groups of four 26-bit blocks on a supressed 57kHz sub-carrier. This note describes an MC68HC05E0-based clock/radio application; it includes a complete software listing.

AN463 68HC05K0 Infra-Red Remote Control

In addition to the same CPU and registers as other members of the M68HC05 family the MC68HC05K0 has a 15-stage multi-function timer and 10 bidirectional I/O lines. A mask option is available for software programmable pull-downs on all the I/0 pins; 4 of the pins are capable of generating interrupts. It is ideally suited for remote-control keyboard applications because the pull-downs and the interrupt drivers on the port pins allow keyboards to be built without any external components except the keys themselves. This application makes use of many of the on-chip features to control a TV infra-red remote control.

AN479 Universal Input Voltage Range Power Supply for High Resolution Monitors with Multi-Sync Capability

This note describes an easy-to-build, high performance, low cost 100W flyback power supply, able to work on any mains supply from 85Vac to 265Vac, and from 40Hz to 100Hz. It is automatically synchronised to the horizontal scanning frequency for minimum screen interference on a multi-sync colour monitor. It uses a low cost MC44602P2 current mode controller – designed specifically for driving high voltage bipolar transistors – with an MJH18010 switchmode power transistor.

AN749 Broadband Transformers and Broadband Combining Techniques for RF

This application note provides a number of practical examples of broadband transformers for RF applications. It includes detailed design formulae and performance data, and discusses power combining techniques that are useful in designing high power RF amplifiers.

AN756 Crystal Switching Methods for MC12060/ MC12061 Oscillators

This report discusses methods of using diodes to select series resonant crystals electronically. Circuit designs suitable for use with crystal frequencies from 100kHz to 20MHz are developed, with emphasis on minimizing frequency pulling. Although developed for use with the MC12060 and MC12061 integrated circuit crystal oscillators, the techniques will generally be useful in any application where it is necessary to select electronically one of a group of crystals with minimum disturbance to the series resonant frequency of the selected crystal.

AN790 Thermal Rating of RF Power Transistors

Reliability is of primary concern to most transistor users. The degree of reliability achieved in practice is controlled by the device user because he determines environmental conditions and the stress levels applied. Knowledge of the basic physical properties of the materials, and the methods used to calculate thermal resistance, will assist the user in transistor selection and equipment design. This note clarifies and corrects some long-standing industry-wide assumptions about thermal resistance and high temperature derating.

AN879 Monomax: Application of the MC13001 Monochrome Television Integrated Circuit

This application note presents a complete 12" black and white line-operated television receiver including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome and the significance of component selections and locations are discussed.

AN925 UHF Preamplifier Centers on Budget Dual-Gate GaAs FET

The signal-to-noise ratio of a communications system can be improved by increasing the power of the transmitter, increasing the gain of the antenna, or improving the sensitivity of the receiver. A low-noise preamplifier is an economical solution for receiver enhancement and this note describes the design, construction and performance of a 400-512MHz preamplifier using Motorola's dual-gate GaAs FET.

Abstracts (continued)

AN932 Application of the MC1377 Colour Encoder

The MC1377 is and economical, high quality, RGB encoder for NTSC or PAL applications. It accepts RGB and composite sync inputs, and delivers a 1V p–p composite NTSC or PAL video output into a 75Ω load. It can provide its own colour oscillator and burst gating, or it can easily be driven from external sources. Performance virtually equal to high-cost studio equipment is possible with common colour receiver components.

AN1019 Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Operation

The TDA3330 is a Composite Video to RGB Colour Decoder originally intended for PAL and NTSC colour TV receivers and monitors – so its data sheet concentrates on picture tube drive. This practical application note supplements the data sheet by providing circuits for video cable drive as used in video processing, frame store and other specialized applications, and expands on TDA3330 functional details. Includes PCB artwork and layout of an evaluation board.

AN1020 A High-Performance Video Amplifier for High Resolution CRT Applications

This note describes a state-of-the-art video amplifier making use of the superior performance characteristics of Motorola CRT driver transistors. In particular, it shows the high speed obtainable with low DC power consumption. The circuit is insensitive to load variations and interconnect methods.

AN1021 A Hybrid Video Amplifier for High Resolution CRT Applications

Many of the 1024 x 1024 and 1280 x 1024 pixel, 64kHz horizontal sweep rate CRTs used in CAD/CAM and high resolution graphics applications have not realized their potential performance because of the speed of their video amplifiers. The CR2424 and CR2425 video amplifiers are hybrid circuits designed for high resolution CRT applications. They feature less than 2.9ns rise and fall time for a 40V output swing, and provide a low power dissipation solution to the problem.

AN1022 Mechanical and Thermal Considerations in Using RF Linear Hybrid Amplifiers

Motorola's thin film hybrid amplifiers are medium power (0.2W to 2.0W power output) broadband devices (1 to 1000MHz) that are biased in a class A mode for linear operation. To ensure a proper electrical and mechanical interface with adequate RF and thermal characteristics, certain guidelines are presented here so that the design engineer can obtain maximum electrical performance and the longest operating life.

AN1025 Reliability Considerations in Design and Use of RF Integrated Circuits

RF integrated circuits – located at strategic points in a CATV system – feature prominently in the overall reliability assessment. Low noise and distortion require state-of-the-art transistor structures. Gold metallization, thermal equilibrium and automated process control have resulted in transistor lifetimes of over 100 years. An overview of the physics of construction involved with the die and interconnects is discussed, together with a definition of major reliability terms and an introduction to hardware and software microcircuit reliability tools.

AN1027 Reliability/Performance Aspects of CATV Amplifier Design

Discusses the reliability advantages offered by the RF hybrid amplifier used in CATV applications. The active part of the hybrid is the transistor – metallization, ballasting and ruggedness are reliability-related factors that must be considered by the device engineer when designing a high performance CATV transistor. Vertical and horizontal geometry and device distortion are performance-related factors that must also be taken into account. The relationship between these factors is examined, and life test data is presented to illustrate the advantages gained by careful device design.

AN1028 35/50 Watt Broadband (160-240MHz) Push-Pull TV Amplifier Band III

The main design aim for this broadband ultra-linear push-pull amplifier was to keep the design as simple as possible, in order to obtain the best performance from the two TPV375 transistors and to minimise the cost. A further target was to obtain the maximum gain by reducing input matching circuit losses. Includes circuit, background description, Smith charts and PCB layout.

AN1029 TV Transposers Band IV and V Po = 0.5W/1.0W

Describes the performance of a 470-860MHz broadband ultra linear amplifier designed for use in band IV and V TV transposers. The design is based on the TPV596, and is intended to be as inexpensive and straightforward as possible: the load line is defined to provide the correct match for peak power; VSWR at the collector is less than 2:1; input matching is designed to provide flat gain with decreasing frequency; and the design is optimized with a CAD program.

AN1030 1W/2W Broadband TV Amplifier Band IV and V

Describes the design and performance of a 470-860MHz broadband linear amplifier for use in band IV and V TV transposers, based on a TPV597 transistor. The design uses a reflection technique to achieve an insertion loss of 6dB per octave with 0dB for the highest frequency. Two amplifiers are connected together with

3dB quadrature hybrids to create a balanced amplifier avoiding the inconvenience of needing a good match of reflected power.

AN1032 How Load VSWR Affects Non-Linear Circuits

If your amplifiers pass lab tests but fail QC testing, the testing environment – not the product – is most likely at fault! Often the culprit is correlation of test systems – RF Correlation occurs only when target error limits are adhered to on a continuous basis among two or more testing stations. Such correlation is essential for non-linear RF and microwave power amplifiers, whose circuits are extremely sensitive to the impedance of their loads. It is easy to compensate for the insertion loss errors in an attenuator, but much more difficult to compensate for load VSWR.

AN1033 Match Impedances in Microwave Amplifiers

The key to successful solid-state microwave power-amplifier design is impedance matching. In any high-frequency power-amplifier design, improper impedance matching will degrade stability and reduce circuit efficiency. At microwave frequencies, this consideration is even more critical, since the transistor's bond-wire inductance and base-to-collector capacitance become significant elements in input/output impedance network design. Includes table of characteristic impedance and velocity factor for various width/height ratios and various materials.

AN1034 Three Balun Designs for Push-Pull Amplifiers

Single RF power transistors seldom satisfy today's design criteria; several devices must be coupled to obtain the required amplifier output power. The push-pull technique is often chosen because it allows input and output impedances to be connected in series for RF operation. Balun-transformers provide the key to push-pull design. This note develops three balun-transformers, culminating with a microstrip version. None of the baluns was tuned nor were the parasitic elements compensated. In this way, their deviation from their theoretical performance could be evaluated more easily.

AN1037 Solid State Power Amplifier, 300W FM, 88-108MHz

A solid state power amplifier in a high efficiency FM transmitter can be made by operating a number of building block amplifiers in parallel. This note describes such a building block amplifier with high output power, high gain, good collector efficiency and broadband (88-108 MHz) frequency response. The design is simple, reproducible and reliable, and is suitable for several architectures. The amplifier has been developed using a pair of TP9383 transistors in push-pull configuration; TP9383 is a double-diffused silicon epitaxial transistor using gold metallization and diffused ballast resistors for long operating life and ruggedness.

AN1039 470-860 MHz Broadband Amplifier 5W

This note describes an ultra linear broadband (470-860MHz) amplifier developed for TV transposer applications. The amplifier incorporates two TPV593 transistors. Each transistor is used to build a separate broadband amplifier which are combined with 3dB hybrids. Includes circuit, parts list and PCB layout.

AN1040 Mounting Considerations for Power Semiconductors

The operating environment is a vital factor in setting current and power ratings of a semiconductor device. Reliability is increased considerably for relatively small reductions in junction temperature. Faulty mounting not only increases the thermal gradient between the device and its heat sink, but can also cause mechanical damage. This comprehensive note shows correct and incorrect methods of mounting all types of discrete packages, and discusses methods of thermal system evaluation.

AN1041 Mounting Procedures for Very High Power RF Transistors

High power (200-600W) RF semiconductors such as the MRF153... and MRF141G... series dissipate an abnormally large amount of heat within a small physical area. Heat sink material, surface finish, mounting screws, washers and screw torque are extremely important factors in ensuring reliability. This note explains why.

AN1044 The MC1378 — A Monolithic Composite Video Synchronizer

The MC1378 provides an interface between a remote composite colour video source and local RGB. On-chip circuitry can lock a local computer to the remote source, switching between local and remote signals to generate composite video overlays. This detailed note describes local and remote operation, picture-in-picture applications and the design of test fixtures to help system development. Printed circuit artwork for an evaluation board is provided. The NTSC/PAL colour encoder is similar to the MC1377, discussed in detail in AN932.

AN1047 Electrical Characteristics of the CR2424 and CR2425 CRT Driver Hybrid Amplifiers

Describes the circuit and thermal characteristics of the CR2424 and CR2425 CRT driver hybrid amplifiers, and discusses three different methods of protecting against damage by a tube arc. Provides details of bandwidth and rise and fall times.

Abstracts (continued)

AN1061 Reflecting on Transmission Line Effects

In recent years, microprocessors and digital logic have seen substantial increases in line drive capability. The fast rise and fall times of modern devices make an understanding of transmission lines and their effects on system reliability a necessity. Includes a procedure for assessing possible transmission line problems in practical designs.

AN1080 External-Sync Power Supply with Universal Input Voltage Range for Monitors

As the resolution of colour monitors increases, the performance and features of their power supplies becomes more critical. EMI/RFI generated by switching power supplies can adversely affect resolution if switching frequency is not synchronised to horizontal scanning frequency. This 90W flyback switching supply demonstrates the use of new high-performance devices in a low-cost design, and includes a new universal input voltage adapter.

AN1092 Driving High Capacitance DRAMs in an ECL System

In systems where speed and efficiency are of utmost importance, designers often mix technologies to achieve the right combination of speed, power, cost and processing capability. Motorola's Emitter Coupled Logic (ECL) makes it possible to operate up to 1GHz clock rates. However, ECL speeds are not necessary in memory that is not accessed every clock cycle – a large CMOS DRAM is cheaper and uses less power and board space than ECL memory. The MC10H/100H660 4-bit ECL-TTL Load Reducing DRAM Driver was designed as a translator for such applications.

AN1106 Considerations in Using the MHW801 and MHW851 Series RF Power Modules

The MHW801 and MHW851 series of power modules are designed for use in cellular portable radios. A considerable amount of applications information is included in the data sheet; this note provides additional information concerning general electrical considerations, noise characteristics, gain control, circuit considerations and mounting.

AN1107 Understanding RF Data Sheet Parameters

The data sheet is often the only source of information about the characteristics and capability of a product. This is especially true of RF devices, which have many unique specifications. It is therefore important that the manufacturer and designer speak a common language. This paper reviews the significance of the quoted values and highlights critical characteristics. Descriptions cover the procedures used to obtain impedance and thermal data, the importance of test circuits, low noise considerations and linearity requirements.

AN1122 Running the MC44802A PLL Circuit

The MC44802A provides the Phase Locked Loop (PLL) portion of a tuning circuit intended for TV, FM radio and set-top converter applications up to 1.3GHz; a complete tuning circuit is formed by adding a Voltage Controlled Oscillator (VCO) and mixer. The data sheet recommends use of an MCU for sending the control bytes that set the tuning frequency. This note describes a serial (IIC) interface with an MC68HC11E9 in a tuner design – the information is sufficiently general to allow almost any MCU to be used. Includes M68HC11 program listing.

AN1207 The MC145170 in Basic HF and VHF Oscillators

Frequency synthesisers such as the MC145170 use digital dividers which are typically under MCU control. Tuning in less than a millisecond can be achieved, and the device can generate many frequencies from a single reference source; the overall frequency capability ranges from a few Hertz to 160MHz. Typical applications include the carrier oscillator in transmitters, local oscillator in receivers, cellular phones, and multiple synchronised clocks in computers and other systems.

AN1306 Thermal Distortion in Video Amplifiers

Thermal distortion is a problem in many high resolution video amplifiers. It occurs when there are instantaneous power changes in the transistor stages, and if the problem remains uncompensated it leads to the visual effect known as smearing. This note discusses what smearing is, what causes thermal distortion, how to measure it, and how to compensate for it.

AN1401 Using SPICE to Analyze the Effects of Board Layout on System Skew when Designing with the MC10/100H640 Family of Clock Drivers

Illustrates the complex influences of board layout on the total skew of a system when designing with the MC10H/100H64x family of clock drivers. Discusses transmission line theory and the various termination techniques, and presents guidelines to assist designers in analyzing board layouts and loading schemes using SPICE simulations to predict and minimise the total skew of a system.

AN1402 MC10/100H00 Translator Family I/O SPICE Modelling Kit

The difficulties of designing high-speed, controlled-impedance PC boards – and the expense of reworking them – makes it essential for designers to model circuit performance prior to committing to a layout. This note provides sufficient information for basic SPICE analysis on the interconnect traces driving or being driven by the 'H600, 'H601, 'H602, 'H603, 'H604, 'H605, 'H606 and 'H607 translator chips. It includes schematics of the input, output and ESD structures, and package

models which may affect the waveforms. A SPICE parameter set for the referenced devices is provided.

AN1404 ECLinPS Circuit Performance at Non-Standard VIH Levels

When ECLinPS devices are interfaced to other technologies there may be times when the input voltages do not meet the specification detailed in the ECLinPS data book. This application note discusses the consequences of driving ECLinPS devices with an Input Voltage HIGH level which is outside the specification.

AN1405 ECL Clock Distribution Techniques

Clock skew – the time difference between supposedly simultaneous clock transitions within a system – is one of the main factors limiting system performance at high frequencies. If clock skew can be reduced, designers can increase performance without using faster logic or more complex and more expensive architectures. Emitter Coupled Logic (ECL) technologies offer a number of advantages over the CMOS and TTL alternatives; this note describes the advantages, the three skew problem areas, and methods of clock distribution to minimise skew.

EB27A Get 300 Watts PEP Linear Across 2 to 30MHz from this Push-Pull Amplifier

Includes circuit, PCB artwork and layout for a 300W push-pull linear amplifier based on two MRF422s, designed to operate over the 2 to 30MHz band. An MC1723 voltage regulator is used as a bias supply.

EB29 The Common Emitter TO-39 and its Advantages

The Common Emitter TO-39 package differs from conventional TO-39s or TO-5s in that the emitter – not the collector – is connected to the metal case. With NPN transistors this configuration allows direct connection of the can to RF and negative DC ground in many class B and C circuits. There are two important advantages: by connecting the case to RF ground, emitter inductance is reduced and gain increased by 3 to 5 dB over that of comparable, conventionally wired transistors. And the case may be directly pressed, clipped, or soldered to the heat sink with no effect on RF performance.

EB59 Predict Frequency Accuracy for MC12060 and MC12061 Crystal Oscillator Circuits

Crystal oscillators are used to generate a precise and highly stable signal. Such circuits typically provide this signal at a frequency close to the resonant frequency of their crystal. However, circuit components and other factors external to the crystal influence its natural resonance to some degree, an effect often referred to as "pulling" or "warping". This bulletin discusses the variation in crystal frequency as a function of different ICs, temperature and DC supply voltage to help the designer to predict the amount of frequency pull in a particular design.

EB77 A 60 Watt 225-400MHz Amplifier – 2N6439

This bulletin describes a 60 watt, 28 volt broadband amplifier covering the 225-400 MHz military communications band. The amplifier may be used singly as a 60 watt output stage in a 225-400 MHz transmitter; by using two of these amplifiers combined with quadrature couplers a 100 watt output amplifier stage may be constructed. The circuit is designed to be driven from a 50 ohm source and work into a nominal 50 ohm load.

EB89 A 1 Watt, 2.3GHz Amplifier

This S-band amplifier features simplicity and repeatability, delivering 8dB minimum gain at 1 watt output on a 24V supply. It uses an MRF2001 transistor in a common base, class C configuration, and is tunable from 2.25 to 2.35GHz. Applications include micowave communications and other systems requiring medium power, narrow band amplification. The Bulletin stresses the importance of physical construction as well as electrical design.

EB90 Low-Cost VHF Amplifier Has Broadband Performance

This bulletin presents two VHF amplifier designs intended for FM or CW service in the 136-174 MHz band. Both feature the Motorola MRF260 and MRF262 plastic encased VHF transistors which are rated at 5.0 W and 15 W power output respectively. The devices are packaged in a standard T0-220 silicone epoxy case with the emitter wired to the metal tab and centre lead of the device. This common emitter configuration results in good RF performance, improved thermal conductivity, and ease of mounting in an RF amplifier by connecting the transistor mounting flange to RF and DC ground.

EB93 60 Watt VHF Amplifier Uses Splitting/Combining Techniques

Proven combining techniques can be used to obtain higher output power and added reliability at VHF. Simple matching networks and power transistors with moderate gain can produce performance comparable to that of a single-stage amplifier with a larger, more expensive device. Though not the ultimate answer, the splitter/combiner method has distinct advantages over designs that force transistors into a parallel configuration. This 60 W amplifier operates from 150 to 175 MHz and features two low-cost MRF264 transistors. The design uses a modified Wilkinson combiner technique to produce 60W output with a drive level of 15W.

EB107 Mounting Considerations for Motorola RF Power Modules

The packaging used for Motorola RF Power Modules consists of a copper flange on which the ceramic substrates are soldered, and a non-conductive cover which is either a snap-on design or attached by epoxy. The substrates are either 96% Alumina, 95.5% Alumina, or 99% Beryllium Oxide, and are attached to the copper flange using lead-tin or indium based soft solders. This bulletin discusses the mechanical factors that should be considered when mounting these modules in equipment.

EB411 A Digital Video Prototyping System

This bulletin describes a Digital Video Prototyping System (DVPS) developed using Motorola's latest multimedia devices, together with a PC-based Field Programmable Gate Array (FPGA) development system. It is designed to provide a fast and effective means of prototyping and demonstrating digital video processing functions. A Reference Section lists datasheets and user manuals containing detailed descriptions and information on the devices. The DVPS has been successfully used to implement two TV sub-systems, namely a Picture-In-Picture Processor and a 4:3 to 16:9 Picture Processor, which are also described.

Applications Documents

300W, 88–108MHz Amplifier using the TP1940 MOSFETs Push-pull Transistor

By Georges Chambaudu
Motorola Semiconducteurs Bordeaux SA

INTRODUCTION

The TP1940 is a high power, high gain and broadband device with low Reverse Transfer Capacitance, C_{rss}. It makes possible fully solid-state transmitters of above 5 kW for FM broadcasts.

Like all MOS devices, it is susceptible to damage from electrostatic discharge. Observe reasonable precautions in handling and packaging it.

The 300 W amplifier described in this Application Note has these features:

- Operates from a 50 V supply
- High power gain
- Compact physical layout
- High efficiency

Typical data for the circuit in Figure 2 are given below.

FUNCTIONAL TESTS (V_{DD} = 50 V, P_{out} = 300 W, I_{dq} = 2 x 200 mA)

	Option 1 (with C9p and without C9s)		Option 2 (with C9s and without C9p)	
f (MHz)	G_A (dB)	η (%)	G_A (dB)	η (%)
108	19.2	62	18.3	65.4
98	19.7	62.6	19.1	68
88	19.4	64	19.6	66.6

Note:

1. Bias increases counter-clockwise with R4.
2. Bias shown is set for 200 mA at 50 V.
3. A copper heat spreader must be mounted on, or laid on top of, a heat sink with thermal grease interface.
4. Drain efficiency can be increased by:
   a. Lowering Drain Idle current (power gain will be reduced by 1–2 dB).
   b. Increasing the value of feedback resistors R8 and R9. This will change the Gain–Frequency slope and Input VSWR. The value of C1 must be raised.
5. In addition to the normal cooling of the units, some air flow is recommended over the top side of the amplifier boards.

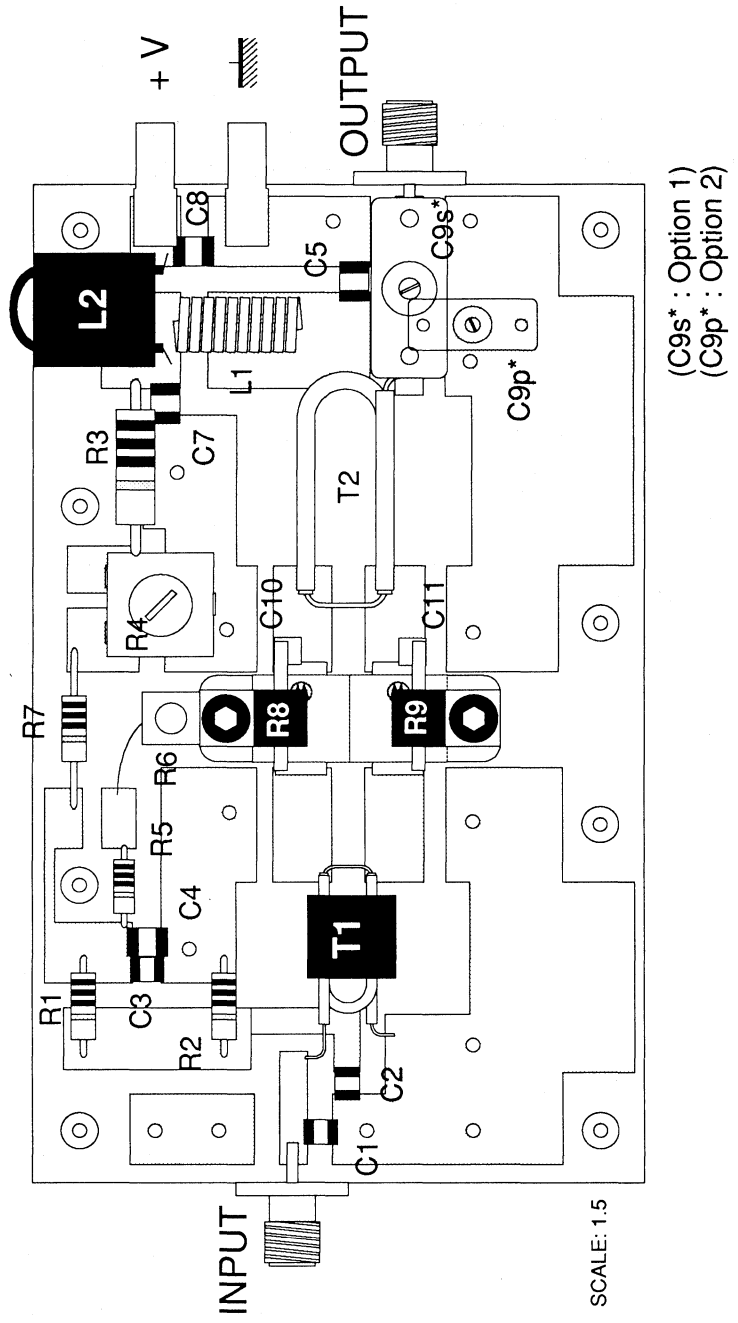
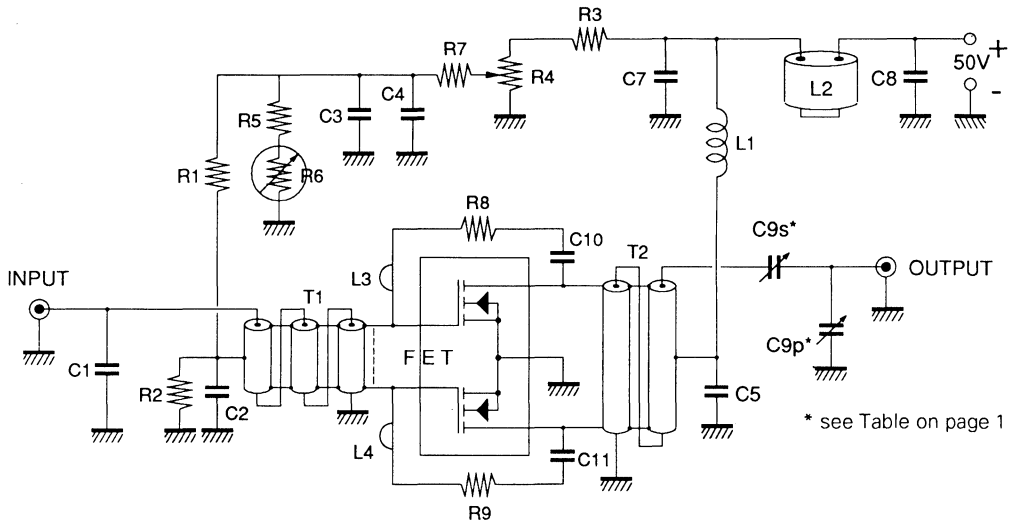


Figure 1. Component layout of 300 W amplifier



C1	24pF Ceramic Chip
C2	1000pF Ceramic Chip
C3, C10, C11	0.1µF Ceramic Chip
C4, C5	1000pF Ceramic Chip
C7	5000pF Ceramic Chip
C8	0.47µF Ceramic Chip or lower values in parallel to reach the value indicated.
C9p	ARCO 404, 8-60pF or equivalent
C9s	ARCO 425, 40-200pF or equivalent
Note 1:	*All ceramic capacitors of 5000pF or less in value are ATC type 100 or equivalent.*
Note 2:	*The Table on Page 1 shows the effect of operating with C9p only or C9s only.*
R1	1KΩ 1/2W
R2	1.5KΩ 1/2W
R3	1.5KΩ 2W
R4	1KΩ Trimmer Potentiometer
R5	6.8 - 8.2 KΩ 1/4W (depending on FET g_{fs})
R6	Thermistor, 10KΩ at 25°C/2.5KΩ at 75°C
R7	2KΩ 1/2W
R8, R9	KDI Pyrofilm PPR515-20-3 or EMC Technologie model 5310 or equivalent 100Ω
L1	10 turns AWG #16 enamelled Wire, 0.2" I.D.
L2	Ferrite beads, 1.5 µH Total
L3, L4	Lead lengths of R8 and R9, 0.6" total.
FET	TP1940
T1	9:1 impedance ratio (input transformer) 25Ω, 0.062" O.D. semi rigid co-ax., with L = 28 mm, l = 11 mm (see Figure 3)
T2	4:1 impedance ratio (output transformer) 25Ω, 0.090" O.D. semi rigid co-ax., with L = 19 mm, l = 9 mm (see Figure 3)
	(T1 transformer must be loaded with ferrite toroids of suitable dimensions and µi of 35-40, or other type ferrite cores, such as Fair-Rite Products Corporation E and I types 9467012002 and 9367021002 respectively.)

Figure 2. 300 W, 88–108 MHz amplifier schematic and parts list

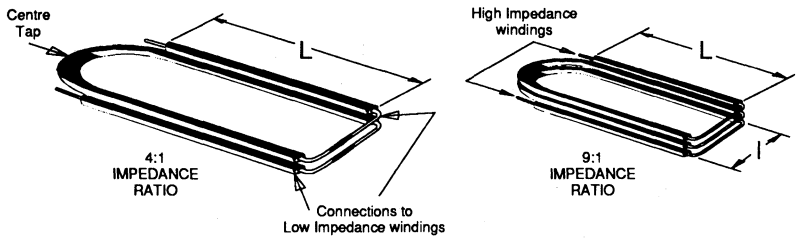
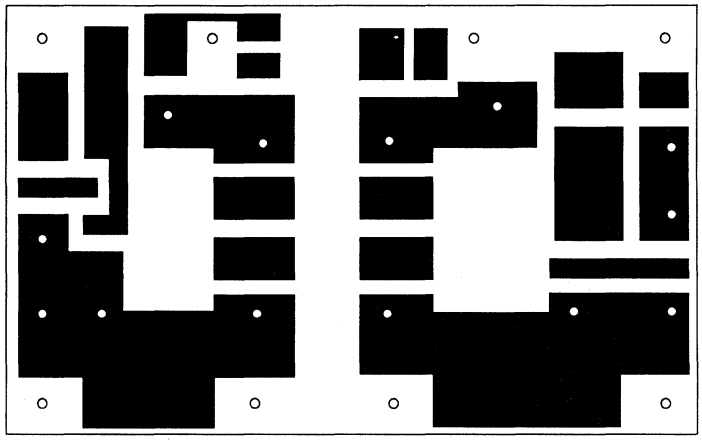


Figure 3. Constructional details of transformers



Epoxy glass 1/16"

Figure 4. Printed Circuit Board (not full size)

"FLOF" Teletext using M6805 Microcontrollers

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1. INTRODUCTION

The "T" members of the MC68HC05 family of MCUs provide a convenient and cost effective method of adding on-screen-display (OSD) to TVs and VCRs. As well as the 64-character OSD capability, they include 8 Kbytes of ROM (adequate for Teletext, frequency-synthesis, stereo and OSD), 320 bytes of RAM, a 16-bit timer and 8 pulse-width-modulated D/A converters. The MC68HC05T7 also includes IIC hardware and, by using a 56-pin package, 4 ports of I/O independent of the OSD, serial and D/A outputs. It is thus suitable for large full-feature chassis. The MC68HC05T1 is in the middle of the price/performance range and includes most of the features of the MC68HC05T7 but in a 40-pin package. This is achieved by sharing I/O with the other pin functions (SPI, OSD, D/A). Even if all these features are used, there is sufficient I/O for most applications.

The MC68HC05T2 is a 16K upgrade of the MC68HC05T1 and the MC68HC05T3 a 24K version with increased RAM (512 bytes) and enhanced OSD (112 characters and 2 rows of OSD buffer). The low cost MC68HC05T4 has 5 Kbytes of ROM and 96 bytes of RAM making it suitable in simpler (eg mono, non-Teletext) applications. The T4 and T7 also include a 14-bit D/A converter to facilitate voltage synthesis tuning. There are EPROM (and OTP) versions of the T3 (including T1 and T2 emulation), T4 and T7.

This application note describes an example of Teletext control software written for the MC68HC05T7 which directly controls Teletext chips of the type 5243. Spanish FLOF Teletext (level 1.5) is handled using packet X/26. If no CCT teletext chip is present on the IIC bus (as indicated by the lack of an acknowledge), all Teletext functions are disabled in software. About 3Kbytes of ROM are used allowing the code to fit into the 7.9K bytes available in an MC68HC05T7 along with tuning, OSD and stereo functions.

The software in the included listing has been written for the MC68HC05T7 but could, with a little modification, be implemented on other M6805 microcontrollers. A microcontroller without IIC hardware can be used as long as additional software is included to facilitate the IIC bus using I/O pins. An example of IIC master I/O driven software can be found in application note AN446.

2. "FLOF" TELETEXT FEATURES

Full Level One Feature (FLOF) Teletext utilises "ghost" packets to provide features in addition to those available with the original CCT Teletext. The primary enhancement is the provision of a menu with a choice of four linked pages selectable by the user with a single press of one of four coloured buttons on the remote control. The menu itself is sent in the ghost page using packet 24 while the linked page numbers are contained in packet 27. In addition to linked pages, packets 26 and 30 are used. Packet 26 allows for the substitution of selected characters in the display by special characters specific to a particular country. This example application includes the Spanish implementation of packet 26. The broadcast service data packet (8/30) is used to get the initial (index) page for each channel and to display station identification information.

"Ghost" packets handled

X/24 :

The FLOF menu information contained in this page extension packet is transferred by the microcomputer to row 24 of the display chapter. When links are disabled because there is no packet 27 (destination code 0) or when bit 4 of byte 43 is 0, row 24 is blank.

X/26 :

Optional handling of modes 1xxxx, 01111 and 00010 in accordance with the Spanish Teletext specification. All the additional characters which are available in the 5243 CCT chip are handled. The feature can be disabled with a hardware link on an I/O pin (see figure 1) so that the software can be used at level 1.0 in non-Spanish countries also using packet 26.

X/27 :

This packet contains the linked page numbers for the red, green yellow, blue and index (black) keys. Bit 4 on the link control byte (byte 43) is used to determine if these links are enabled (1) or disabled (0). When enabled, the Spanish specification requires that bits 1, 2 and 3 be used to enable the green, yellow and blue links respectively. This use of these bits is not defined in the World Teletext Specification. For this reason their use is selectable by a hardware link (see figure 1). If these bits are not used, all links (if enabled by bit 4) will be taken from packet 27 but will be automatically disabled if the broadcast links are default (FF3F7F) or invalid.

8/30 :

The broadcast service packet is used to supply the index page number on exit from standby and (if teletext is not stopped) after a channel change. Bytes 10-30 of this packet are displayed for 5 seconds on exit from standby and (if teletext is not stopped) after a channel change.

3. IMPLEMENTATION

The software listing is in two parts. The first part contains the "idle" loop and IIC routines from the main TV control part of the MC68HC05T7 application. The idle loop controls the timing of everything performed by the microprocessor, scans the local keyboard, checks whether or not an IR command has been received, etc. It also monitors the relevant flags in the Teletext chip and performs the tasks (eg fetching linked pages) which have to be performed independently of requests for the user.

The second and main listing is the Teletext module itself. It contains all the subroutines required to carry out automatic and user requested Teletext activity. Both modules use the same RAM allocation file (RAMT8.S05) which is included in the listing of the Teletext module. This listing also includes a symbol cross-reference table.

Figure 1 shows a simplified circuit diagram of the application. Most of the MC68HC05T7's I/O is used for purposes other that Teletext and is not shown in detail. Communication with the 5243 Teletext chip is via an IIC bus in which the T7 is always the master. The function of the three I/O pins used for Teletext is described under "Ghost packets handled" and "Inputs and Outputs".

A version of this Teletext software has been implemented on an MC68HC05C4 for use in a TV where the other control functions were handled by a separate microcontroller. The signal from the IR pre-amp was fed into the C4 which used Teletext commands to control a 5243 via a software IIC bus. Non-Teletext commands were re-generated by the C4 and sent to the other microcontroller. This arrangement allows Teletext to be added to a chassis which was originally designed without considering Teletext.

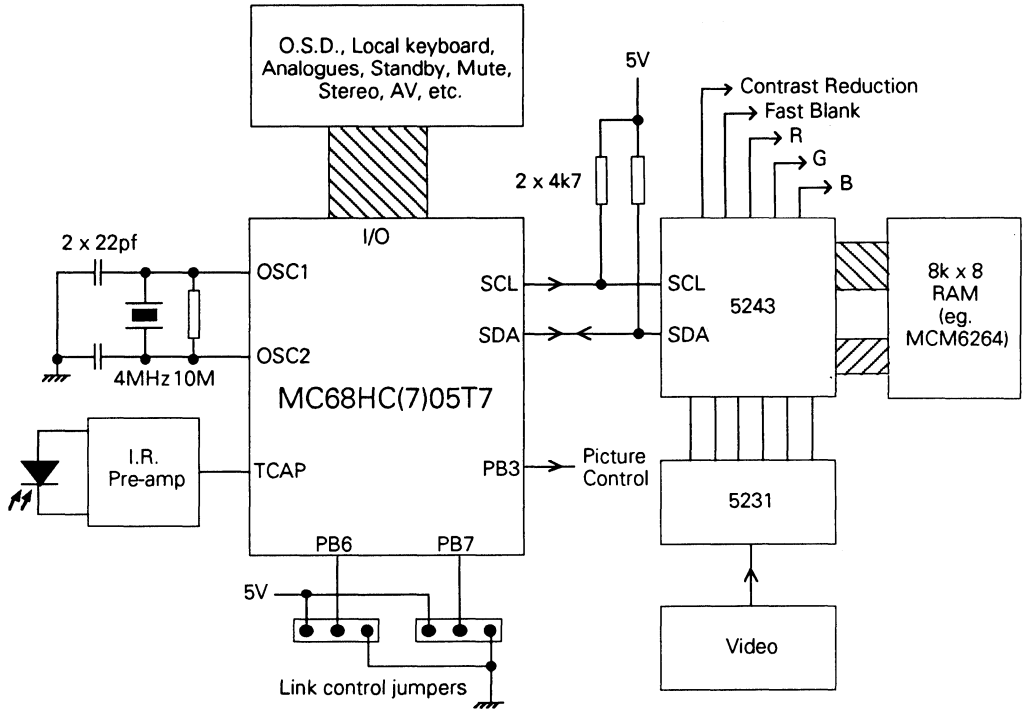

Figure 1. MC68HC(7)05T7 – Teletext application circuit

4. IDLE LOOP

In the example application the idle loop code is in the main TV control software module rather than in the teletext module. Listing 1 shows the relevant parts of this module. The loop time is 12.8mS and it is at this rate that the timing counters used by Teletext (CNT1 and CNT4) are incremented. The standby condition is checked first; if the TV set is in standby then there is no IIC activity and hence no reading from, or writing to, the 5243. If the TV has just exited from standby, as indicated by the flag 3,STAT2, then Teletext is initialised using the sub-routine RESTRT. This sub-routine writes to the 5243's control and mode registers (R5, R6 and R7) and checks that the IIC acknowledge is present. If there was no acknowledge, as indicated by flag 6,STAT7, then no further Teletext activity is attempted.

If an acknowledge is present, Teletext polling goes ahead, although it is suspended if there is a mute or time display. A mute indicates that the channel has just been changed, or no channel is tuned. During time display, all other Teletext activity is suspended. Re-initialisation using sub-routine START2 is performed if flag 7,STAT5 is set by a change of the tuned frequency.

Counter CNT4 is used to delay the transfer of packets 24 (page extension – FLOF menu), 27 (links), 26 (enhanced display characters) and the control bits from row 25 (display page) after the initial arrival of a page. When row 24 is read the 5243 FOUND flag is set to indicate that the arrival has been acted upon. If UPDATE is on then an update indicator appears if the update control bit (C9) is set or if the sub-page has changed or if it is the first arrival of the page. The update display is performed by the sub-routine ARRVD which clears the transient flags and enables the required display, i.e. page no. in normal mode and the whole of row 0 in sub-page mode. Any boxed information (eg sub-titles or newsflash) in the current page is also displayed. The last Teletext function performed by the idle loop is the checking of the FOUND flag in the 5243. This is accessed via the IIC bus; it is on the last (not displayed) row of the display page along with the current page and sup-page numbers and the control bits.

If there is a current Teletext transient (time, row 0 box or packet 8/30), the transient control branch from the idle loop is executed. This routine checks to see if it is time to end the transient. If it is, the subroutine OSDLE is executed. It resets transients for both the OSD generated by the MC68HC05T7 and Teletext. The sub-routine RSTMD2 performs this function for Teletext. It is called from within the sub-routine OSDLE (not listed).

5. REMOTE CONTROL FUNCTIONS

TV/TXT

Toggle between TV & Teletext mode.

0-9

Number keys for entry of page and sub-page numbers

Red, Green, Yellow, Blue

Linked page access keys. The decoder stores four pages of text. These are the display page and the three pages corresponding to the red, green and yellow links. The blue linked page is not acquired in advance. In the absence of FLOF data or if the links are disabled by the control bit in packet 27, the red key is page+1 and the green key page-1. Under these circumstances the requested page and the next three pages are acquired.

PC+/-

These keys always select page+1/page-1 regardless of the availability of FLOF information. As with the red, green and yellow keys, the page is displayed immediately if it is already in RAM.

INDEX

This key operates as an additional link with the difference that if the link is invalid the initial page from packet 8/30 is selected.

SUB-PAGE/TIME

Text mode: Enter sub-page mode, (max. 3979). TV mode: Display time in top-right-hand corner for 5 seconds. Pressing this key during a station identification display (packet 8/30 bytes 10-30) can be used to extend this display beyond the five seconds it appears for, after a channel change.

STOP

Halt acquisition, "STOP" is displayed instead of page number. Press again to restart. If acquisition has been stopped by partially entering a new page number then this key can be used to return to the original page.

MIX/NO-MIX

Toggle between Teletext and mixed display. Use of this key causes the display of the top status row for 5 seconds if it is not being displayed because the current page is a newsflash or a sub-title. 5243 contrast reduction is enabled in mixed mode.

FULL/TOP/BOT

Selects one of the three display formats, normal, top half enlarged, bottom half enlarged.

REVEAL

Reveal hidden text, toggle action.

UPDATE

Return to picture until a new version of the requested page arrives. When it arrives, its page no. is displayed in the top-right-hand corner, the key operates in both TV and Teletext mode, set is put into TV mode. Any boxed information (alarm clock, newsflash or sub-title) will be displayed. In sub-page mode the complete header is displayed so that both page & sub-page numbers can be seen. Cancel update by entering Teletext mode and then going back to TV mode by pressing the TV/Text key twice.

6. TELETEXT SUBROUTINES

6a. Subroutines: TVTX, UPDATE, DIGIT0 and GETIT

The Teletext module (listing 2) comprises various sub-routines which are used both by the idle loop and to perform any Teletext actions initiated by commands from the IR remote control. They are described in the order in which they appear in the listing.

TVTX is executed when the TV/TEXT button is pressed. Its function is to toggle between TV mode and Teletext mode. The flag 0,STAT indicates the current mode. This flag routes the microprocessor to execute either TXTOFF or TXTON according to the current mode. TXTON checks that Teletext hardware is present and does nothing if there has been no IIC acknowledge. If, however, a 5243 is present in the TV, it clears all transients (OSDLE) and sets up the Teletext mode. It initialises the control registers (R5 and R6) to display text and background both in and out of boxes. For newsflashes the set-up is text and background within boxes and picture outside. TXTOFF also resets transients but forces TV mode and sync. Polling and updating continue as a background activity.

When the UPDATE key is pressed the update flag 4,STAT2 is set and TXTOFF executed so the TV is forced to TV mode. If there is a current transient hold (eg time), the hold is cleared before TXTOFF is executed.

The number entry sub-routine DIGIT0 branches to DIGITS in sub-page mode but otherwise accepts any number key as a page number input. Three digits are required, the pointer PDP holding the current position (0, 1 or 2 for hundreds, tens or units). During entry the flag 2,STAT is set to stop Teletext activity. The numbers have to be written to the top-left-hand corner of the display page as well as saved in RAM. Once all three digits have been entered the page is requested and page acquisition restarted.

The code at label GETIT makes this request after first checking whether or not the selected page has already been requested (it could be the current display page or an already requested linked page). If it has, then a switch is made to the chapter associated with the appropriate acquisition circuit and no new request is generated. If not, the new request is made and the FOUND flag set.

6b. Subroutines: Colours, INDEX, NPAGE and PPAGE

The four colour keys (Red, Green, Yellow and Blue) are primarily intended for selecting Teletext linked pages. When pressed the chapter which corresponds to the appropriate acquisition circuit is selected for display. If links are disabled (by the link control bit or because there is no packet 27), then the RED and GREEN keys select current page +1 and -1 respectively. This choice is taken according to the state of flag 3, STAT3 which reflects the condition of the link control bit in packet 27. The code executed by RED, if links are not in use, is the same as that executed by the "+" function (NPAGE) which always selects the next page. Similarly the alternative GREEN function (PPAGE) is the same as for the "-" key. The YELLOW and BLUE keys do nothing under these circumstances. In Spanish Teletext the GREEN, YELLOW and BLUE links can be individually inhibited, but the RED link is only inhibited if all links are off.

The chapter associated with the selected page is displayed immediately if it has already been requested. This will normally be the case if a linked page (red, green or yellow) has been selected. The code at label LPT is executed if the page has already been requested. If not, a jump to CLRPD is performed. CLRPD is a label within DIGIT0; the code at CLRPD requests a new page just as if the page number had been entered manually. If the required acquisition circuit is the one already current, then the "unstop" code is executed. This causes the green page-being-looked-for header to roll as though the page number had just been entered. This means that something can be seen to happen in the case where the linked page differs only from the current page in its sub-page number. Linked sub-pages are not fully supported in this implementation as they are rarely used by broadcasters and would significantly increase the size of the software. When the chapter is changed the Teletext PBLF (page being looked for) flag is checked. If it is low the FOUND flag is cleared. This forces the fetching of the links associated with the new display page. If the page is not already in, this will automatically happen when it arrives so the FOUND flag does not need to be cleared.

The BLUE (or cyan) key is different in that its page will not normally be immediately available (the four pages: display, red, green and yellow occupy the four acquisition circuits and RAM chapters).

The INDEX (or black link) function is similar to BLUE except that if its link is not valid it defaults to the initial (index) page number supplied by packet 8/30 (see sub-routine GIP).

6c. Subroutines: LINK, GLP1, GLP2, SRCH, CHCK1 and NOTOKx

The sub-routine LINK allocates the three linked pages (RED, YELLOW and GREEN) to the three free acquisition circuits (not in use by the display page). To do this it checks the page numbers in turn to see if they have already been requested. If so they are left in their current acquisition circuit. If they have not already been requested the page number is put into a LIFO. Only 0-9 are regarded as acceptable digits for page numbers; this is consistent with the Spanish specification although the additional HEX numbers (A-F) may be used experimentally or by Teletext page generators. Within this first loop the sub-routine GLP1 is used to get the linked page numbers from packet 27, perform a decode of the Hamming encoded data and calculate the new magazine number (page hundreds) if different from that of the display page. GLP1 uses sub-routine SRCH to check if the page has already been requested. If there are no links, or if links are disabled, then displayed page +1, +2 and +3 are requested.

The second loop in LINK allocates new page numbers to the remaining unused acquisition circuits. It uses GLP2 to clear the relevant chapters in the Teletext memory and make the new requests. Subroutine CHCK1 is used to check whether or not an acquisition circuit is in use before it is loaded with a new page number from the LIFO.

This method of organising new page requests prevents unnecessary requests being made for pages already requested. This is particularly important when links are disabled and pages are being requested using the "+" or "-" functions. Under these circumstances when the page number is incremented (or decremented) only one new page has to be requested (new display page+3), while page, page+1 and page+2 do not need to change and can be left in their current acquisition circuits.

NOTOK3 and NOTOK2 handle the RED and GREEN functions when links are disabled. They are disabled if the link control bit (packet 27 bit 3, byte 43) is zero or if there is no packet 27. These subroutines respectively increment and decrement the current page number (units and tens). The current magazine number (page hundreds) is not affected.

6d. Subroutines: ROW24, W2B, R2B, GCYI, CLINK and DECODE

ROW24 is used to transfer ghost row 20 (packet 24) into the display chapter. This has to be done via the IIC bus. The loop reads two bytes via the IIC (sub-routine R2B) bus from the ghost page and writes it to the display page (sub-routine W2B). The FOUND flag is then set to indicate that the arrival of the page has been recognised and acted upon. This sub-routine is only called by the idle loop and is used along with the other sub-routines which get information from the ghost page (CLINK, LINK and GET25).

R2B and W2B use IIC routines READ and SEND which are outwith the Teletext module. These subroutines will differ according to the microprocessor in use. An MC68HC05C8 implementation would need to use I/O lines (see reference for suitable software) while the MC68HC05T7 can use its IIC hardware. The routines used in this example are included in the listing extract from the TV control software module (listing 1).

The sub-routine GCYI is used by LINK to store the data associated with the BLUE an INDEX links. As explained above, these pages will not be acquired in advance, the page number only being sent to an acquisition circuit if requested by an IR command.

CLINK fetches the link control byte from packet 27 if the destination code is OK and, after decoding the Hamming encoded data, transfers the bits to STAT3.

The Hamming decode sub-routine DECODE corrects for single bit errors. This is done with in-line code using the table HAM (at the end of listing 2) as this uses less ROM than an algorithmic method.

6e. Subroutines: MIX, TRANx, TXTx, HOLD, and NOHOLD

The mixed display capability of the Teletext chip (5243) is toggled using an IR key which calls the sub-routine MIX. When mixed mode is entered, interlaced broadcast sync. (312/313) is selected because the non-interlaced sync. used for teletext is not suitable if a TV picture is present on the screen. This is set up via the 5243 mode register R1. The control registers R5 and R6 are updated to provide the mixed display.

When returning to a non-mixed display, the code at NOMIX is used to re-configure the control registers and to set up a Teletext only 312/312 non-interlaced sync. This sync. reduces adjacent line flicker in a pure Teletext display.

The subroutine TRAN2 sets up a transient which retains a black background on the top row so that the page number, time etc. can be seen clearly. This type of transient is also started if the page number or sub-page number is being entered in mixed mode. Sub-routines TRAN1, TRAN2 and TRAN3 are used to initialise the various transient displays. These displays are cancelled as discussed above by actions taken within the idle loop controlled by the free-running timer within the MC68HC05T7.

The TXTx sub-routines are used in conjunction with the IIC SEND routine to write to various sub-sets of the registers within the 5243.

If the Teletext STOP function is requested by an IR command the routine HOLD is executed. This is a toggled function when requested in this way. HOLD displays the word "STOP" in place of the page number and stops the display acquisition circuit by clearing the 5243 HOLD flag accessed via its page request register R3.

NOHOLD is executed to restart the display acquisition circuit. It returns the page number to the top-left-hand corner. If a new page number has been partially entered, a press of STOP (executing an UNHOLD) will allow a return to the most recent page request. This takes only a single press as the start of the entry of a new page number cause a HOLD. The completion of a page number entry (3 digits) causes a NOHOLD.

6f. Subroutines: REVEAL, EXPTB and TIME

The REVEAL function causes any hidden display information to appear. It is controlled by a bit in the display mode register (R7). The software example leaves any revealed information permanently displayed. If, however, it is required that such information disappear when the page is updated (this may be better for a quiz page), then the two commented out lines (80 and 81) in the idle loop should be enabled.

The display expand facility is controlled by another two bits in R7. The EXPTB sub-routine cycles through normal, top-half double height and bottom-half double height.

The example application uses a single IR key (subroutine TIME) for both the display of the Teletext clock and the entry into sub-page mode. IF the set is in TV mode then the time is displayed for 5 seconds. If the TV is in Text mode then sub-page mode is selected. Sub-page number entry is described in the following section. When the Teletext clock is requested it appears (boxed) at the top-right-hand corner. It is removed by the idle loop 5 seconds after the last press of the time button. When the time is being displayed all other Teletext activity is stopped using UCHOLD.

6g. Subroutines: DIGITS, SUBPG, GET25 and GET26

DIGITS is the sub-page version of DIGIT0 and uses similar code. More checks on the input data are required as the four digits of the sub-page number have different maximum values. These maximums are 3 for thousands, 7 for the tens and 9 for the hundreds and units. These values reflect the sub-page number's original use as a time (24hr format). For tens and thousands a keyed 8 becomes a 0 and a 9 becomes a 1; for thousands only 4, 5, 6 and 7 become 0, 1, 2 and 3 respectively.

The code at the label SETIT is the sub-page equivalent of GETIT, described above. It requests the new sub-page and sets the FOUND flag.

The sub-routine SUBPG is called when the TIME (or clock) key is pressed (TV in Teletext mode). It toggles between normal mode and sub-page mode. When sub-page mode is entered the page number display (P—) is replaced with **** to indicate the mode change and to prompt for the entry of a sub-page number. Once all four digits have been entered the new sub-page is requested by SETIT. The code at the label RSTR is used to exit from this mode back to the normal (page number) mode, restoring the page number display to the top-left-hand corner.

GET25 is used by the idle loop to get the information stored in row 25 of the display chapter. This row is not displayed but contains various information used by the control microprocessor. The current page number, magazine number, sub-page number, Teletext control bits and the FOUND and PBLF flags are available. GET25 gets the required information and stores it in the RAM of the MC68HC05T7.

At the end of this sub-routine the I/O line 7,portB is checked. If it is low, packet 26 is handled. If it is high, this packet is disabled. This would be required if this application were to be used in a country other than Spain which used packet 26. It would require to be switched off as the enhanced display feature uses different characters depending on the country. In countries which do not use packet 26 (eg the UK) it does not matter whether or not packet 26 is enabled.

If packet 26 is enabled, GET26 processes all packet 26 data present in the ghost page. The tables G2TAB, G3TAB and CTAB contain the characters used to replace the character at the display location defined by each packet.

6h. Subroutines: GIP, R24T and SR24T

The sub-routine GIP gets the initial (index) page from packet 8/30. It will be doing this as the set is brought out of standby or just after a channel change. It may thus initially get a poor signal (or there may be no Teletext) so it tries repeatedly until it finds a valid packet 8/30 format 1. If this is not found after 96 tries it gives up and sets the flag 6,STAT2 to indicate that there is no packet 8/30 (or no Teletext). In this circumstance it defaults to an index page number of 100.

R24T transfers bytes 10-30 of the broadcasting service data packet (8/30) into the display chapter. It is called once a second for five seconds after power-on or a channel change. The data is transferred to row 0 of the display page which can be displayed either at the bottom or, as in this example, the top of the screen. This transient display is setup using the sub-routine SR24T if Teletext is present. If the flag 6,STAT2 has been set by GIP as described above then SR24T does nothing. The transient display is terminated by code executed at the appropriate time from within the idle loop.

7. INPUT AND OUTPUTS

Apart from the IIC bus, only three pins on the controlling microprocessor are relevant to Teletext. Two inputs select the usage of packets 26 and 27 and one output can be used to control any hardware which requires to be changed according to whether or not there is a TV picture currently being displayed. In many applications some or all of these functions will not be required and could be eliminated from the software thus freeing up the pins for other uses.

PB3)

This pin is active (high) during a pure (no-mixed, no-boxed) teletext display, otherwise it is low.

PB6)

When this pin is low, Spanish use of link control bits 1, 2 and 3 is enabled. When it is high, these bits are ignored.

PB7)

Packet 26 control. When low, packet 26 is enabled and handles all the Spanish alternate characters which are available in the 5243. When PB7 is high, packet 26 is ignored.

8. REFERENCES

Application note AN446, MCM2814 Gang-programmer using an MC68HC05B6.

LISTING 1

```
                                ****************************************************
                                *                                                  *
                                *       Idle loop.                                 *
                                *                                                  *
                                ****************************************************

00000000  0d13fd        ILP     BRCLR   6,TSR,*         OUTPUT COMPARE FLAG
00000003 >3c00                  INC     CNT1            TELETEXT TRANSIENT
00000005 >3c00                  INC     CNT4            ROW 24 DELAY
00000007 >3c00                  INC     CNT5            MUTE TRANSIENT
00000009 >cd0000                JSR     KBD             KEYBOARD & TIMERS
0000000c  030104                BRCLR   1,PORTB,FON     STANDBY ?
0000000f >1600                  BSET    3,STAT2         MAKE SURE FLAG AGREES
00000011  205f                  BRA     F1              AND IDLE WITH NO IIC ACTIVITY
00000013 >070009        FON     BRCLR   3,STAT2,ALRON   NO, JUST ON ?
00000016 >1700                  BCLR    3,STAT2         YES, RESTART
00000018 >1500                  BCLR    2,STAT2         CLEAR THIS FLAG ALSO ?
0000001a >1f00                  BCLR    7,STAT5         RE-INITIALISATION NOT NECESSARY
0000001c >cd0000                JSR     RESTRT
0000001f >cd0000        ALRON   JSR     VCRPOLL         POLL SCART LINES
00000022 >02004d                BRSET   1,STAT2,F1       REMOTE REPEATING ?
00000025 >02004a                BRSET   1,STAT4,F1       LOCAL REPEATING ?
00000028 >0c0047                BRSET   6,STAT7,F1       TELETEXT CHIP ON BUS ?
0000002b >040044                BRSET   2,STAT2,F1       SEARCH/STANDBY ?
0000002e >0a0041                BRSET   5,STAT,F1        TIME DISPLAY HOLD
00000031 >06003e                BRSET   3,STAT4,F1       TRANSIENT MUTE ?
00000034 >0c003b                BRSET   6,STAT4,F1       COINCIDENCE MUTE ?
00000037 >0f0005                BRCLR   7,STAT5,DNTRS    TO BE RE-ITIALISED ?
0000003a >1f00                  BCLR    7,STAT5         YES, CLEAR FLAG &
0000003c >cd0000                JSR     START2          RE-INITIALISE TELETEXT
0000003f >01001c        DNTRS   BRCLR   0,STAT2,NO24
00000042 >b600                  LDA     CNT4            PAUSE WHILE PACKET 24
00000044  a130                  CMP     #48             (PAGE EXT.) ARRIVES
00000046  252a                  BLO     F1
00000048 >cd0000                JSR     CLINK           CHECK LINK CONTROL BYTE
0000004b >cd0000                JSR     LINK            FETCH LINKS
0000004e >cd0000                JSR     ROW24           FETCH ROW 24 AND SET FOUNDB
00000051 >cd0000                JSR     GET25           GET ROW 25 & PACKET 26
00000054 >090005                BRCLR   4,STAT2,NOUP    UPDATE ENABLED ?
00000057 >0b0002                BRCLR   5,STAT2,NOUP    DIFFERENCES ?
0000005a  ad6e                  BSR     ARRVD
0000005c >1100          NOUP    BCLR    0,STAT2
0000005e >b600          NO24    LDA     ACC
00000060 >b700                  STA     R8
00000062  a608                  LDA     #8              COLUMN 8 (FOUNDB & PBLF)
00000064 >b700                  STA     R10
00000066  a619                  LDA     #25             ROW
00000068 >cd0000                JSR     R2B
0000006b >080104                BRSET   4,IOBUF+1,F1    FOUNDB FLAG SET ?
0000006e >1000                  BSET    0,STAT2         NO, SO FETCH GHOST ROWS
                        *       BCLR    5,R7            KILL REVEAL
                        *       JSR     TXT2
00000070 >3f00                  CLR     CNT4
00000072 >04008b        F1      BRSET   2,STAT2,ILP     SEARCHING ?
00000075 >060088                BRSET   3,STAT2,ILP     STANDBY ?
00000078 >090085                BRCLR   4,STAT,ILP      TRANSIENT ?

                                ****************************************************
                                *                                                  *
                                *       Transient control.                         *
                                *                                                  *
                                ****************************************************

0000007b >b600                  LDA     CNT1            YES
0000007d  a150                  CMP     #80
0000007f  2403                  BHS     NILP
00000081 >cc0000                JMP     ILP             1S TIMER
00000084 >b600          NILP    LDA     R4
00000086  a104                  CMP     #4
00000088  2603                  BNE     NOTE            IF PAGE 4 THEN IT'S
0000008a >cd0000                JSR     R24T            THE 8/30 TRANSIENT
0000008d >3f00          NOTE    CLR     CNT1            CLEAR 1S TIMER
0000008f >3a00                  DEC     TMR             DECREMENT SECONDS COUNTER
00000091  2703                  BEQ     DNILP           TRANSIENT FINISHED ?
00000093 >cc0000                JMP     ILP             NO

00000096 >cd0000        DNILP   JSR     OSDLE           OSD TIMEOUT (INC RSTMD)
00000099 >cc0000                JMP     ILP

                                ****************************************************
                                *                                                  *
                                *       End Teletext transients.                   *
                                *                                                  *
                                *       Clear mode bits (channel mode, 2-digit     *
                                *       prog. no. entry etc.)                      *
                                *                                                  *
                                ****************************************************

0000009c >010003        RSTMD   BRCLR   0,STAT5,SOS2    2-DIGIT Pr. No. ENTRY ?
0000009f >cd0000                JSR     RES             YES, RESTORE DISP
000000a2 >1500          SOS2    BCLR    2,STAT4         MAKE SURE ITS PROGRAM MODE

000000a4 >1900          RSTMD2  BCLR    4,STAT4         RESET OSD TRANSIENT FLAG
000000a6 >1900          RSTMD3  BCLR    4,STAT          RESET MAIN TRANSIENT FLAG
000000a8 >0b0011                BRCLR   5,STAT,TXTR1    TIME HOLD ?
000000ab >1b00                  BCLR    5,STAT          YES, CLEAR IT
000000ad  a603                  LDA     #$03
000000af >b700                  STA     R5
000000b1 >b700                  STA     R6
000000b3 >cd0000                JSR     TXT2            STOP TIME EXIT FLASH
000000b6 >040003                BRSET   2,STAT,TXTR1    OTHER HOLD ?
000000b9 >cd0000                JSR     NOTTH           NO, SO CLEAR HOLD
000000bc >1100          TXTR1   BCLR    0,R7            BOX OFF ROW 0
000000be >000006                BRSET   0,STAT,TXTR2    TELETEXT ?
000000c1 >b600                  LDA     ACC
000000c3 >b700                  STA     R4
000000c5 >3f00                  CLR     R7              NO, ALL BOXES OFF
000000c7 >cc0000        TXTR2   JMP     TXT2            YES
```

```
                                ********************************************************
                                *                                                      *
                                *       Updated page has arrived.                      *
                                *                                                      *
                                ********************************************************

000000ca >b600          ARRVD   LDA     ACC
000000cc >b700                  STA     R4
000000ce >1900                  BCLR    4,STAT          KILL TRANSIENTS
000000d0 >1b00                  BCLR    5,STAT
000000d2  4f                    CLRA
000000d3 >cd0000                JSR     BOX0ON
000000d6 >0c0005                BRSET   6,STAT,SPMD     SUB-PAGE MODE ?
000000d9  a606                  LDA     #6              NO, SMALL BOX
000000db >cd0000                JSR     BOX0OF
000000de  a646          SPMD    LDA     #$46
000000e0 >b700                  STA     R5
000000e2 >b700                  STA     R6
000000e4  a603                  LDA     #$03
000000e6 >050002                BRCLR   2,C3,NNF        NEWSFLASH ?
000000e9  a602                  LDA     #$02            YES, NO ROW 0
000000eb >b700          NNF     STA     R7
000000ed >cc0000                JMP     TXT2


000000f0  a610          RESTRT  LDA     #$10            BROADCAST SYNC.
000000f2 >b700                  STA     R1
000000f4  a606                  LDA     #6
000000f6 >b700                  STA     R5
000000f8 >b700                  STA     R6
000000fa >3f00                  CLR     R7
000000fc >cd0000                JSR     TXT2            SWITCH PICTURE ON

000000ff  013c03                BRCLR   0,MSR,ACKOK     ACKNOWLEDGE ?
00000102 >1c00                  BSET    6,STAT7         NO, SET FLAG
00000104  81                    RTS

00000105 >cc0000        ACKOK   JMP     INITXT


00000108 >b600          RES     LDA     PROG            YES, RESTORE PROG. NO.
0000010a >b700                  STA     DISP
0000010c >1100                  BCLR    0,STAT5
0000010e  81            ABS     RTS

                                ********************************************************
                                *                                                      *
                                *       IIC write.                                     *
                                *                                                      *
                                ********************************************************


0000010f  ad23          SEND    BSR     IICSU

00000111 >bf00                  STX     DPNT            SAVE X
00000113 >1100                  BCLR    0,ADDR          SET-UP TO WRITE
00000115 >b600                  LDA     ADDR
00000117  ad25                  BSR     SHIFT           SEND CHIP ADDRESS

00000119 >b600          WRBU    LDA     ADDR
0000011b  a180                  CMP     #$80            STEREOTONE ?
0000011d  2606                  BNE     WRB
0000011f >b600                  LDA     SUBADR          YES, SO ENABLE AUTO
00000121  ad1b                  BSR     SHIFT           SUB-ADDRESS INCREMENTING
00000123 >3c00                  INC     SUBADR

00000125 >be00          WRB     LDX     DPNT            DATA BUFFER POINTER
00000127  f6                    LDA     0,X
00000128  ad14                  BSR     SHIFT           SEND DATA
0000012a >3c00                  INC     DPNT
0000012c >3a00                  DEC     W1
0000012e  26e9                  BNE     WRBU            DONE ?

00000130  1b3b                  BCLR    5,MCR           STOP
00000132  9a                    CLI
00000133  81                    RTS

00000134  9b            IICSU   SEI
00000135  3f3c                  CLR     MSR             IIC SET-UP
00000137  3f3a                  CLR     FDR             90 KHz
00000139  a6b0                  LDA     #$B0            ENABLE IIC AS MASTER
0000013b  b73b                  STA     MCR             TRANSMITTER & START
0000013d  81                    RTS

0000013e  b73d          SHIFT   STA     MDR
00000140  0f3cfd                BRCLR   7,MSR,*
00000143  81                    RTS

00000144  adc9          WRITE   BSR     SEND
00000146  a602                  LDA     #2
00000148 >cd0000                JSR     TPAU            WAIT 10mS (EEPROM WRITE)
```

```
230                                 ********************************************************
231                                 *                                                      *
232                                 *       IIC read.                                      *
233                                 *                                                      *
234                                 ********************************************************
235
236 0000014b  ad0c                READ    BSR     READ1           GET FIRST BYTE
237 0000014d >b600                        LDA     IOBUF
238 0000014f >b701                        STA     IOBUF+1         MOVE IT UP
239 00000151 >b600                        LDA     ADDR
240 00000153  a1a1                        CMP     #$A1            NVM ?
241 00000155  2602                        BNE     READ1
242 00000157 >3c00                        INC     SUBADR          YES, NEXT SUB-ADDRESS
243
244 00000159  add9                READ1   BSR     IICSU
245 0000015b >1100                        BCLR    0,ADDR          RW = 0 ALWAYS WRITE (SUB-ADDRESS)
246 0000015d >b600                        LDA     ADDR
247 0000015f  add4                        BSR     SHIFT           SEND CHIP-ADDRESS
248 00000161 >b600                        LDA     SUBADR
249 00000163  add9                        BSR     SHIFT           SEND SUB-ADDRESS
250 00000165  1b3b                        BCLR    5,MCR           NO STOP BUT
251
252 00000167  1a3b                        BSET    5,MCR           A RESTART
253 00000169 >1000                        BSET    0,ADDR          SET BIT 0 FOR READ
254 0000016b >b600                        LDA     ADDR
255 0000016d  adcf                        BSR     SHIFT           RE-SEND CHIP ADDRESS
256 0000016f  193b                        BCLR    4,MCR           CHANGE TO RECEIVER
257 00000171  163b                        BSET    3,MCR           SWITCH OFF ACK.
258 00000173  b63d                        LDA     MDR             INITIATE RECEPTION
259
260                                 *       BRCLR   7,MSR,*         WAIT FOR IT
261                                 *       BSET    3,MCR           SECOND LAST SO SWITCH OFF ACK.
262                                 *       LDA     MDR             GET FIRST BYTE
263                                 *       STA     IOBUF+1         AND SAVE IT
264
265 00000175  0f3cfd                       BRCLR   7,MSR,*         WAIT FOR IT
266 00000178  1b3b                        BCLR    5,MCR           LAST BYTE SO STOP
267 0000017a  b63d                        LDA     MDR             GET BYTE
268 0000017c >b700                        STA     IOBUF           AND SAVE IT
269 0000017e  9a                          CLI
270 0000017f  81                          RTS
271
272                                 ********************************************************
273                                 *                                                      *
274                                 *       IIC interrupt.                                 *
275                                 *                                                      *
276                                 ********************************************************
277
278 00000180  3f3c                MBINT   CLR     MSR
279 00000182  80                  RETURN  RTI
```

LISTING 2

```
                        ********************************************************************************
                        *                                                                              *
                        *              TV/Teletext/OSD/Stereo program (MC68HC05T7).                    *
                        *                                                                              *
                        *                  CCT Teletext control module (Spain).                        *
                        *                                                                              *
                        *                Used with RAMT8.S05, OST.S05 & TMT7.S05                       *
                        *                                                                              *
                        * This software was developed by Motorola Ltd. for demonstration purposes.     *
                        *  No liability can be accepted for its use in any specific application.       *
                        *       Original software copyright Motorola - all rights reserved.            *
                        *                                                                              *
                        *                P. Topping                19th October '90                    *
                        *                                                                              *
                        ********************************************************************************


                                EXPORT  DIGIT0,RED,GREEN,YELLOW,CYAN
                                EXPORT  NPAGE,PPAGE,REVEAL,EXPTB,UPDATE,TVTX,GIP
                                EXPORT  TIME,MIX,INDEX,HOLD,SR24T,START2,INITXT

                                EXPORT  CLINK,LINK,ROW24,GET25,R2B,TXT2
                                EXPORT  R24T,NOTTH,BOX0ON,BOX0OF

                                IMPORT  SEND,READ,OSDLE,TPAU2


                                LIB     RAMT8.S05

                        ************************************************************
                        *                                                          *
                        *       RAM allocation for OST.S05, TMT7.S05 & TXT7.S05.   *
                        *                                                          *
                        ************************************************************

                                SECTION.S .RAM,COMM

                        ******************************************************
                        *                                                    *
                        *       Equates.                                     *
                        *                                                    *
                        ******************************************************

00000000                PORTA   EQU     $00             Port A address
00000001                PORTB   EQU     $01             Port B    "
00000002                PORTC   EQU     $02             Port C    "
00000003                PORTD   EQU     $03             Port D    "
00000004                DDRA    EQU     $04             Port A data direction reg.
00000005                DDRB    EQU     $05             Port B    "       "       "
00000006                DDRC    EQU     $06             Port C    "       "       "
00000007                DDRD    EQU     $07             Port D    "       "       "

00000008                LED1    EQU     $08             D/A 0  STEREO LED
00000009                LED2    EQU     $09             D/A 1  BILINGUAL LED
0000000a                LED3    EQU     $0A             D/A 2  FM -/- NICAM LED

                        *VOLU   EQU     $0A             D/A 2        JP08 IN T1 EVB
0000000b                CONT    EQU     $0B             D/A 3        JP09 IN T1 EVB
0000000c                BRILL   EQU     $0C             D/A 4        JP10 IN T1 EVB
0000000d                SATU    EQU     $0D             D/A 5        JP11 IN T1 EVB
0000000e                VOLU    EQU     $0E             D/A 6

00000012                TCR     EQU     $12             Timer control register.
00000013                TSR     EQU     $13             Timer status register.
00000014                ICRH    EQU     $14             Input capture register, high.
00000015                ICRL    EQU     $15             Input capture register, low.
00000016                OCRH    EQU     $16             Output compare register, high.
00000017                OCRL    EQU     $17             Output compare register, low.
00000018                TDRH    EQU     $18             Timer data register, high.
00000019                TDRL    EQU     $19             Timer data register, low.
0000001c                MISC    EQU     $1C             Misc. register

00000020                OSD     EQU     $20             18 OSD data registers
00000032                CAS     EQU     $32             Color & status register
00000033                C34     EQU     $33             Color 3/4 register
00000034                RAD     EQU     $34             Row address & character size
00000035                WCR     EQU     $35             Window/Column register
00000036                CCR     EQU     $36             Column/color register
00000037                HPD     EQU     $37             Horizontal position delay

00000039                MADR    EQU     $39
0000003a                FDR     EQU     $3A
0000003b                MCR     EQU     $3B
0000003c                MSR     EQU     $3C
0000003d                MDR     EQU     $3D

0000003e                TR1     EQU     $3E             Test 1, OSD/Timer/PLM
0000003f                TR2     EQU     $3F             Test 2, EPROM
```

```
27                              ********************************************************
27                              *                                                      *
27                              *       Teletext RAM allocation.                       *
27                              *                                                      *
27                              ********************************************************
27
27 00000000                     SUB1    RMB     1
27 00000001                     R1      RMB     1               mode register
27 00000002                     R2      RMB     1               page request address register
27 00000003                     R3      RMB     1               page req. data reg. col. 0 : mag.
27 00000004                     C1      RMB     1               "     "    "    "    "   1 : pgt.
27 00000005                     C2      RMB     1               "     "    "    "    "   2 : pgu.
27 00000006                     C3      RMB     1               "     "    "    "    "   3 : ht.
27 00000007                     C4      RMB     1               "     "    "    "    "   4 : hu.
27 00000008                     C5      RMB     1               "     "    "    "    "   5 : mt.
27 00000009                     C6      RMB     1               "     "    "    "    "   6 : mu.
27 0000000a                     SUB2    RMB     1
27 0000000b                     R4      RMB     1               display chapter register
27 0000000c                     R5      RMB     1               display control register (normal)
27 0000000d                     R6      RMB     1               display control register (news/sub)
27 0000000e                     R7      RMB     1               display mode register
27 0000000f                     SUB3    RMB     1
27 00000010                     R8      RMB     1               active chapter register
27 00000011                     R9      RMB     1               active row register
27 00000012                     R10     RMB     1               active column register
27 00000013                     R11     RMB     1               active data register
27 00000014                     PH      RMB     1               2nd     "       "
27 00000015                     PT      RMB     1               3rd     "       "
27 00000016                     PU      RMB     1               4th     "       "
27 00000017                     LIFO    RMB     9               LINKED PAGE No. LIFO BUFFER
27 00000020                     PAGE    RMB     7               PAGE No. INPUT BUFFER
27 00000027                     PAG0    RMB     3               AC0 PAGE No.
27 0000002a                     PAG1    RMB     3               AC1 PAGE No.
27 0000002d                     PAG2    RMB     3               AC2 PAGE No.
27 00000030                     PAG3    RMB     3               AC3 PAGE No.
27 00000033                     PAGC    RMB     3               CYAN PAGE No.
27 00000036                     PAGI    RMB     3               INDEX PAGE No.
27 00000039                     PDP     RMB     1               PAGE DIGIT POINTER
27 0000003a                     ACC     RMB     4               DISP, RED, GREEN, YELLOW AC. CIR.
27 0000003e                     WACC    RMB     1               WORKING ACC No.
27 0000003f                     ADDR    RMB     1               IIC ADDRESS
27 00000040                     DPNT    RMB     1               IIC DATA POINTER FOR WRITE
27 00000041                     SUBADR  RMB     1               IIC SUB-ADDRESS
27 00000042                     IOBUF   RMB     4               IIC BUFFER, +2 & +3 RSRVD FOR PLL
27 00000046                     STAT2   RMB     1               0: ROW24 FETCH FLAG
27                              *                               1: REMOTE REPEATING
27                              *                               2: SEARCH/STANDBY IIC LOCK
27                              *                               3: STANDBY STATUS
27                              *                               4: UPDATE PENDING
27                              *                               5: DIFFERENCE FOUND
27                              *                               6: NO TELETEXT TRANSMISSION
27                              *                               7: MIXED
27
27 00000047                     STAT3   RMB     1               0: CYAN   LINK ON
27                              *                               1: YELLOW LINK ON
27                              *                               2: GREEN  LINK ON
27                              *                               3: LINKS/ROW24  ON
27
27
27                              ********************************************************
27                              *                                                      *
27                              *       General RAM allocation.                        *
27                              *                                                      *
27                              ********************************************************
27
27 00000048                     PLLHI   RMB     1               PLL DIVIDE RATIO MSB
27 00000049                     PLLOW   RMB     1               PLL DIVIDE RATIO LSB
27 0000004a                     W1      RMB     1               WORKING
27 0000004b                     W2      RMB     1               "
27 0000004c                     W3      RMB     1               "
27 0000004d                     COUNT   RMB     1               LOOP COUNTER
27 0000004e                     KOUNT   RMB     1               LOCAL KEYBOARD COUNTER
27 0000004f                     CNT     RMB     1               12.8mS (inc, free running)
27 00000050                     CNT1    RMB     1               12.8mS (inc, reset every 1s during transient)
27 00000051                     CNT3    RMB     1               3.25 S (dec, automatic standby timeout)
27 00000052                     CNT4    RMB     1               12.8mS (cleared for row24 delay when page arrives)
27 00000053                     CNT5    RMB     1               12.8mS (inc, transient mute)
27 00000054                     TMR     RMB     1               TRANSIENT DISPLAY SECONDS COUNTER
27 00000055                     STAT    RMB     1               0: TV/TELETEXT
27                              *                               1: IIC R/W
27                              *                               2: HOLD
27                              *                               3: IR REPEAT INHIBIT
27                              *                               4: TRANSIENT DISPLAY ON
27                              *                               5: TIME HOLD
27                              *                               6: SUB-PAGE MODE
27                              *                               7: IR TASK PENDING
27 00000056                     STAT4   RMB     1               0: KEY FUNCTION PERFORMED
27                              *                               1: LOCAL REPEATING
27                              *                               2: P/C PROG : 0, CHAN : 1
27                              *                               3: MUTE (TRANSIENT)
27                              *                               4: OSD STATUS TRANSIENT
27                              *                               5: MUTE (BUTTON)
27                              *                               6: COINCIDENCE MUTE
27                              *                               7: SEARCH
27 00000057                     PWR     RMB     1               $55 AT RESET, $AA NORMALLY
27 00000058                     PROG    RMB     1               CURRENT PROGRAM NUMBER
27 00000059                     CHAN    RMB     1               CURRENT CHANNEL NUMBER
27 0000005a                     DISP    RMB     1               CURRENT DISPLAY NUMBER (PROGRAM)
27 0000005b                     DISC    RMB     1               CURRENT DISPLAY NUMBER (CHANNEL)
27 0000005c                     FTUNE   RMB     1               FINE TUNING REGISTER
27 0000005d                     AVOL    RMB     1               VOLUME LEVEL
27 0000005e                     BRIL    RMB     1               BRILLIANCE LEVEL
27 0000005f                     KEY     RMB     1               CODE OF PRESSED KEY (LOCAL)
27                              *NUM0   RMB     4               LED DISPLAY RAM
27 00000060                     IRRA1   RMB     1               IR INTERRUPT TEMP.
27 00000061                     IRRA2   RMB     1               "       "       "
27 00000062                     IRRA3   RMB     1               "       "       "
27 00000063                     IRRA4   RMB     1               "       "       "
27 00000064                     DIFFH   RMB     1               IR TIME DIFFERENCE
27 00000065                     DIFFL   RMB     1               "    "      "
27 00000066                     IRH     RMB     1               IR CODE BIT
27 00000067                     IRL     RMB     1               COLLECTION
27 00000068                     IRCODE  RMB     1
27 00000069                     IRCNT   RMB     1
27 0000006a                     IRCMCT  RMB     1
27 0000006b                     OLDIR   RMB     1
```

```
27                              ****************************************************
27                              *                                                  *
27                              *       RAM allocation for Stereoton.              *
27                              *                                                  *
27                              ****************************************************
27
27 0000006c                     SHADMAT RMB     1               TEMPORARY MATRIX
27 0000006d                     LBAL    RMB     1               Loudspeaker balance variable
27 0000006e                     SNDMD   RMB     1               SOUND MODE 0:ST, 1:DA, 2:DB, 3:W, 4:M, 5:FM
27 0000006f                     ABAV    RMB     1               SCART SOUND MODE 0:STEREO, 1:DUAL A, 2:DUAL B
27
27 00000070                     K1      RMB     1               K1 level                                (reg 0)
27 00000071                     LVL     RMB     1               Loudspeaker left volume                 (reg 1)
27 00000072                     LVR     RMB     1               Loudspeaker right volume                (reg 2)
27 00000073                     HVL     RMB     1               Headphone volume left                   (reg 3)
27 00000074                     HVR     RMB     1               Headphone volume right                  (reg 4)
27 00000075                     TONE    RMB     1               Tone variable (Bass/Treble)             (reg 5)
27 00000076                     MATRIX  RMB     1               Current matrix                          (reg 6)
27 00000077                     K2      RMB     1               K2 level                                (reg 7)
27
27
27 00000078                     STAT5   RMB     1               0: 2-DIGIT PROGRAM ENTRY
27                                                              1: ANY MUTE REQUIRED ?
27                                                              2: OSD NAME TABLE
27                                                              3: OSD DEFAULT P/C NUMBER
27                                                              4: ANALOGUE OSD ON
27                                                              5: NAME-TABLE STANDARD
27                                                              6: STANDARD CHANGED
27                                                              7: RE-INITIALISE TELETEXT
27
27 00000079                     STAT6   RMB     1               0: AV MODE BIT 0 (0:TV, 1:S-VHS)
27                                                              1: AV MODE BIT 1 (2:SCRT1, 3:SCADT2)
27                                                              2:
27                                                              3:
27                                                              4:
27                                                              5:
27                                                              6: SCART INPUT #1
27                                                              7: SCART INPUT #2
27
27 0000007a                     STAT7   RMB     1               0: AV MODE CHANGE
27                                                              1: FORCE FM SOUND
27                                                              2: CS : TELETEXT NEWSFLASH
27                                                              3: C6 : TELETEXT SUBTITLES
27                                                              4: LANGUAGE A/B (TV)
27                                                              5: WIDE-PSEUDO
27                                                              6: NO TELETEXT ACKNOWLEDGE
27                                                              7: POWER UP IN STANDBY
27
27                              ****************************************************
27                              *                                                  *
27                              *       OSD RAM allocation.                        *
27                              *                                                  *
27                              ****************************************************
27
27 0000007b                     CAS1    RMB     1               ROW 1, colour 1/2 & outline enable
27 0000007c                     RAD1    RMB     1               Row address & character size
27 0000007d                     CCR1    RMB     1               Window colour & end column
27 0000007e                     CAS2    RMB     1               ROW 2, colour 1/2 & outline enable
27 0000007f                     RAD2    RMB     1               Row address & character size
27 00000080                     CCR2    RMB     1               Window colour & end column
27 00000081                     CAS3    RMB     1               ROW 3, colour 1/2 & outline enable
27 00000082                     RAD3    RMB     1               Row address & character size
27 00000083                     CCR3    RMB     1               Window colour & end column
27 00000084                     CAS4    RMB     1               ROW 4, colour 1/2 & outline enable
27 00000085                     RAD4    RMB     1               Row address & character size
27 00000086                     CCR4    RMB     1               Window colour & end column
27 00000087                     CAS5    RMB     1               ROW 5, colour 1/2 & outline enable
27 00000088                     RAD5    RMB     1               Row address & character size
27 00000089                     CCR5    RMB     1               Window colour & end column
27 0000008a                     CAS6    RMB     1               ROW 6, colour 1/2 & outline enable
27 0000008b                     RAD6    RMB     1               Row address & character size
27 0000008c                     CCR6    RMB     1               Window colour & end column
27 0000008d                     CAS7    RMB     1               ROW 7, colour 1/2 & outline enable
27 0000008e                     RAD7    RMB     1               Row address & character size
27 0000008f                     CCR7    RMB     1               Window colour & end column
27 00000090                     CAS8    RMB     1               ROW 8, colour 1/2 & outline enable
27 00000091                     RAD8    RMB     1               Row address & character size
27 00000092                     CCR8    RMB     1               Window colour & end column
27
27 00000093                     OSDL    RMB     1               CURRENT OSD ROW POINTER
27 00000094                     LIND    RMB     1               ROW TABLE INDEX
27 00000095                     BROW    RMB     1               CHARACTER FLASH ROW
27 00000096                     BCOL    RMB     1               CHATACTER FLASH COLUMNS
27 00000097                     WROW    RMB     1               WINDOW FLASH ROW
27 00000098                     ROW1    RMB     1               FIRST ROW No. (NAME TABLE)
27
27 00000099                     ANAL    RMB     1
27 0000009a                     ANAF    RMB     1
27
27 0000009b                     TMP1    RMB     1
27 0000009c                     TMP2    RMB     1
27
27 0000009d                             RMB     12              UNUSED
27
27 000000a9                     STACK   RMB     22              23 BYTES USED FOR STACK
27 000000bf                     SP      RMB     1               (1 INTERRUPT AND 9 NESTED SUBS)
27
27                                      SECTION .RAM2,COMM
27 00000000                     DRAM    RMB     128
28
29                                      SECTION .ROM2
```

```
                                ********************************************************
                                *                                                      *
                                *       Teletext/TV switching.                         *
                                *                                                      *
                                ********************************************************

00000000 >000037        TVTX    BRSET   0,STAT,TXTOFF
00000003 >0c0074        TXTON   BRSET   6,STAT7,PANIC   TELETEXT CHIP ON BUS ?
00000006 >1000                  BSET    0,STAT          TELETEXT MODE
00000008 >cd0000                JSR     OSDLE
0000000b  a616                  LDA     #$16            CCT, 312/312 SYNC
0000000d >b700                  STA     R1              ENABLING GHOST ROWS
0000000f >1900                  BCLR    4,STAT          ABORT TRANSIENTS
00000011 >1900                  BCLR    4,STAT2         KILL UPDATES
00000013 >1f00                  BCLR    7,STAT2         NOT MIXED
00000015 >0b0008                BRCLR   5,STAT,NOTT
00000018 >1b00                  BCLR    5,STAT
0000001a >040003                BRSET   2,STAT,NOTT
0000001d >cd0000                JSR     NOTTH
00000020  a6cc          NOTT    LDA     #$CC
00000022 >b700                  STA     R5
00000024  a646                  LDA     #$46
00000026 >b700                  STA     R6
00000028 >b600                  LDA     ACC
0000002a >b700                  STA     R4
0000002c >cc0000                JMP     TRAN2

0000002f >0c0048        UPDATE  BRSET   6,STAT7,PANIC   TELETEXT CHIP ?
00000032 >1800                  BSET    4,STAT2         UPDATE ON
00000034 >090003                BRCLR   4,STAT,TXTOFF   TRANSIENT HOLD ?
00000037 >cd0000                JSR     NOTTH           YES, RESTART
0000003a >1100          TXTOFF  BCLR    0,STAT          TV MODE
0000003c >cd0000                JSR     OSDLE
0000003f >1100          TXTOF   BCLR    0,STAT          TV MODE
00000041  a610                  LDA     #$10            BROADCAST, 312/313 SYNC
00000043 >b700                  STA     R1              ENABLING GHOST ROWS
00000045 >1900                  BCLR    4,STAT          ABORT TRANSIENTS
00000047 >1b00                  BCLR    5,STAT          ABORT TIME TIMEOUT
00000049  a603          RST     LDA     #$03            $06 FOR TRANSIENTS
0000004b >b700                  STA     R5
0000004d >b700                  STA     R6
0000004f >3f00                  CLR     R7
00000051 >cd0000                JSR     TXT2
00000054  a602                  LDA     #2
00000056 >cc0000                JMP     SPM

00000059 >e602          TEST    LDA     PAG0+2,X
0000005b  a139                  CMP     #$39
0000005d  221b                  BHI     PANIC
0000005f  a130                  CMP     #$30
00000061  2517                  BLO     PANIC
00000063 >e601                  LDA     PAG0+1,X
00000065  a139                  CMP     #$39
00000067  2211                  BHI     PANIC
00000069  a130                  CMP     #$30
0000006b  250d                  BLO     PANIC
0000006d >e600                  LDA     PAG0,X
0000006f  a137                  CMP     #$37
00000071  2207                  BHI     PANIC
00000073  a130                  CMP     #$30
00000075  2503                  BLO     PANIC
00000077 >b700                  STA     PAGE
00000079  81            ABO     RTS                     OK, CARRY CLEAR
0000007a  99            PANIC   SEC                     NOT OK, CARRY SET
0000007b  81                    RTS
```

```
 97                                  ****************************************************
 98                                  *                                                  *
 99                                  *       Number entry routines.                     *
100                                  *                                                  *
101                                  ****************************************************
102
103 0000007c >0d0003          DIGIT0  BRCLR   6,STAT,DIGIT
104 0000007f >cc0000                  JMP     DIGITS
105 00000082 >1700           DIGIT   BCLR    3,R3            HOLD DURING
106 00000084 >b600                    LDA     ACC             ENTRY
107 00000086 >cd0000                  JSR     UP
108 00000089  a604                    LDA     #4
109 0000008b >cd0000                  JSR     SPM
110 0000008e >1400                    BSET    2,STAT          SET HOLD FLAG
111 00000090 >b600                    LDA     W2
112 00000092  a010                    SUB     #16
113 00000094 >be00           LD0      LDX     PDP
114 00000096  2606                    BNE     NOCH            NOT HUNDREDS SO DON'T CHANGE
115 00000098  a107                    CMP     #7              YES, MORE THAN 7 ?
116 0000009a  2302                    BLS     NOCH            NO, SO DON'T CHANGE
117 0000009c  a008                    SUB     #8              YES, 8->0 & 9->1
118 0000009e  ab30           NOCH     ADD     #$30            CONVERT TO ASCII
119 000000a0 >e700                    STA     PAGE,X
120 000000a2  a302                    CPX     #2              UNITS ?
121 000000a4  270e                    BEQ     CLRPD           YES, SO CLEAR PDP
122 000000a6  a62d                    LDA     #$2D            DASH
123 000000a8  a301                    CPX     #1              TENS ?
124 000000aa  2702                    BEQ     TEN             YES, SO LEAVE TENS
125 000000ac >b701                    STA     PAGE+1          CLEAR TENS
126 000000ae >b702           TEN      STA     PAGE+2          CLEAR UNITS
127 000000b0 >3c00                    INC     PDP
128 000000b2  2002                    BRA     DPGN
129 000000b4 >3f00           CLRPD    CLR     PDP
130 000000b6 >b600           DPGN     LDA     R4
131 000000b8 >b700                    STA     R8
132 000000ba >3f00                    CLR     R9              ROW 0
133 000000bc  a602                    LDA     #2
134 000000be >b700                    STA     R10             COLUMN 2
135 000000c0  a650                    LDA     #$50            P
136 000000c2 >b700                    STA     R11
137 000000c4 >b600                    LDA     PAGE
138 000000c6 >b700                    STA     PH
139 000000c8 >b601                    LDA     PAGE+1
140 000000ca >b700                    STA     PT
141 000000cc >b602                    LDA     PAGE+2
142 000000ce >b700                    STA     PU
143 000000d0 >cd0000                  JSR     TXT38
144 000000d3 >cd0000                  JSR     TRAN1
145 000000d6 >b600                    LDA     PDP
146 000000d8  269f                    BNE     ABO
147 000000da  a606                    LDA     #6
148 000000dc >cd0000                  JSR     NOBX
149 000000df >b600                    LDA     PAGE
150 000000e1 >b700                    STA     PH
151
152                                  ****************************************************
153                                  *                                                  *
154                                  *       Get requested page.                        *
155                                  *                                                  *
156                                  ****************************************************
157
158 000000e3 >cd0000          GETIT   JSR     SRCH            IS PAGE ALREADY IN ?
159 000000e6  2545                    BLO     LPT2            YES
160 000000e8  ad23                    BSR     INDX            DISPLAY CHAPTER
161 000000ea >b600                    LDA     PAGE            PAGE HUNDREDS
162 000000ec >e700                    STA     PAG0,X          SAVE IN RAM
163 000000ee >b601                    LDA     PAGE+1          PAGE TENS
164 000000f0 >e701                    STA     PAG0+1,X        SAVE IN RAM
165 000000f2 >b700                    STA     C1              PAGE REQUEST TENS
166 000000f4 >b602                    LDA     PAGE+2          PAGE UNITS
167 000000f6 >e702                    STA     PAG0+2,X        SAVE IN RAM
168 000000f8 >b700                    STA     C2              PAGE REQUEST UNITS
169 000000fa >b600                    LDA     PAGE            PAGE HUNDREDS
170 000000fc  a018                    SUB     #$18
171 000000fe >b700                    STA     R3              PAGE REQUEST HUNDREDS
172 00000100 >b600                    LDA     R4
173 00000102 >cd0000                  JSR     UP
174 00000105 >cd0000                  JSR     TXT1            REQUEST IT
175 00000108 >1500                    BCLR    2,STAT          RESET HOLD FLAG
176 0000010a >cc0000                  JMP     SEND            WRITE ONE TO FOUND
177
178
179 0000010d >b600           INDX     LDA     ACC
180 0000010f  48                      LSLA                    x2
181 00000110 >bb00                    ADD     ACC             x3
182 00000112  97                      TAX
183 00000113  81             YIP      RTS
184
185 00000114  48             UP       LSLA
186 00000115  48                      LSLA
187 00000116  48                      LSLA
188 00000117  48                      LSLA
189 00000118 >b700                    STA     R2
190 0000011a  81                      RTS
```

```
                                ******************************************************
                                *                                                    *
                                *       Red, Green & Yellow keys.                    *
                                *                                                    *
                                ******************************************************

0000011b >3f00          RED     CLR     PDP
0000011d >06000b                BRSET   3,STAT3,RED2     LINKS ON ?

00000120 >cd0000        NPAGE   JSR     INDXP
00000123 >cd0000                JSR     NOTOK3          NO, SO FORCE AN INCREMENT
00000126  252c                  BLO     LPT             ALREADY REQUESTED ?
00000128 >cc0000                JMP     CLRPD           NO, GETIT
0000012b >b601          RED2    LDA     ACC+1
0000012d  2025          LPT2    BRA     LPT

0000012f >3f00          GREEN   CLR     PDP
00000131 >06000b                BRSET   3,STAT3,GLOK    LINKS ON ?

00000134 >cd0000        PPAGE   JSR     INDXP
00000137 >cd0000                JSR     NOTOK2          NO, SO FORCE A DECREMENT
0000013a  2518                  BLO     LPT             ALREADY REQUESTED ?
0000013c >cc0000                JMP     CLRPD           NO, GETIT
0000013f  0c0103        GLOK    BRSET   6,PORTB,IG0     GYC BITS ENABLED ?
00000142 >010061                BRCLR   0,STAT3,ABC     GREEN LINK ON ?
00000145 >b602          IG0     LDA     ACC+2
00000147  200b                  BRA     LPT

00000149 >07005a        YELLOW  BRCLR   3,STAT3,ABC     LINKS ON ?
0000014c  0c0103                BRSET   6,PORTB,IG1     GYC BITS ENABLED ?
0000014f >030054                BRCLR   1,STAT3,ABC     YELLOW LINKS ON ?
00000152 >b603          IG1     LDA     ACC+3
00000154 >b700          LPT     STA     W3
00000156  48                    LSLA                    X2
00000157 >bb00                  ADD     W3              X3 FOR PAGE POINTER
00000159  97                    TAX
0000015a >cd0000                JSR     TEST            IS PAGE No. OK ?
0000015d  2547                  BCS     ABC             IF NOT ABORT
0000015f >b600                  LDA     W3              ACC No
00000161 >b100                  CMP     ACC             IF SAME ACC CCT
00000163  2604                  BNE     NTSAC           THEN FORCE UNSTOP
00000165 >1400                  BSET    2,STAT
00000167  2009                  BRA     CARO
00000169 >0d0003        NTSAC   BRCLR   6,STAT,SKOSP    SUB-PAGE MODE ?
0000016c >cd0000                JSR     OUTSP           YES, ABANDON IT
0000016f >cd0000        SKOSP   JSR     RSTR            PUT PAGE No. BACK
00000172 >3f00          CARO    CLR     PDP
00000174 >050003        COK     BRCLR   2,STAT,NOTHLD   IF OLD PAGE ON HOLD
00000177 >cd0000                JSR     NOHOLD          CANCEL HOLD
0000017a  a60f          NOTHLD  LDA     #$0F            CORRUPT C6 FOR UPDATE
0000017c >b700                  STA     C6
0000017e >b600                  LDA     W3
00000180 >b700                  STA     R4
00000182 >b700                  STA     ACC
00000184 >cd0000                JSR     CFND            CHECK PBLF, IF HIGH DO NOTHING
00000187 >1500                  BCLR    2,STAT          IF LOW (PAGE FOUND) CLEAR FOUNDB
00000189 >cc0000                JMP     TXT2            TO FORCE FETCHING OF LINKS.

                                ******************************************************
                                *                                                    *
                                *       Index & Cyan keys.                           *
                                *                                                    *
                                ******************************************************

0000018c  ae0f          INDEX   LDX     #15
0000018e >cd0000                JSR     TEST
00000191  2414                  BCC     IAC
00000193 >cc0000                JMP     GIP

00000196 >07000d        CYAN    BRCLR   3,STAT3,ABC     LINKS ON ?
00000199  0c0103                BRSET   6,PORTB,IG2     GYC BITS ENABLED ?
0000019c >050007                BRCLR   2,STAT3,ABC     CYAN LINK ON ?
0000019f  ae0c          IG2     LDX     #12
000001a1 >cd0000                JSR     TEST
000001a4  2401                  BCC     IAC
000001a6  81            ABC     RTS

000001a7 >1d00          IAC     BCLR    6,STAT          RESET PAGE MODE
000001a9 >3f00                  CLR     PDP
000001ab >e602                  LDA     PAG0+2,X
000001ad >b700                  STA     PU
000001af >b700                  STA     C2
000001b1 >e601                  LDA     PAG0+1,X
000001b3 >b700                  STA     PT
000001b5 >b700                  STA     C1
000001b7 >e600                  LDA     PAG0,X
000001b9 >b700                  STA     PH
000001bb  a018                  SUB     #$18
000001bd >b700                  STA     R3
000001bf >cd0000                JSR     INDX
000001c2 >b600                  LDA     PH
000001c4 >e700                  STA     PAG0,X
000001c6 >b600                  LDA     PT
000001c8 >e701                  STA     PAG0+1,X
000001ca >b600                  LDA     PU
000001cc >e702                  STA     PAG0+2,X
000001ce >b600                  LDA     ACC
000001d0 >b700                  STA     R8
000001d2 >cd0000                JSR     UP
000001d5  a650                  LDA     #$50
000001d7 >b700                  STA     R11
000001d9 >3f00                  CLR     R9
000001db  a602                  LDA     #2
000001dd >b700                  STA     R10

000001df >1500          CYOK    BCLR    2,STAT          RESET HOLD FLAG
000001e1 >cd0000                JSR     TXT38
000001e4 >cd0000                JSR     TRAN1           DISPLAY TOP ROW
000001e7 >cd0000                JSR     SFND            SET FOUNDB
000001ea >cc0000                JMP     TXT1
```

```
303                                     ******************************************************
304                                     *                                                    *
305                                     *       Get linked page nos & allocate to ACCs.      *
306                                     *                                                    *
307                                     ******************************************************
308
309 000001ed >b600                     LINK    LDA     ACC             CHAPTER
310 000001ef  ab04                             ADD     #4              ADD 4 FOR GHOST ROWS
311 000001f1 >b700                             STA     R8
312 000001f3 >3f00                             CLR     COUNT
313 000001f5  a601                             LDA     #1
314 000001f7 >b700                             STA     W3
315 000001f9  a6ff                             LDA     #$FF
316 000001fb >b701                             STA     ACC+1
317 000001fd >b702                             STA     ACC+2
318 000001ff >b703                             STA     ACC+3
319 00000201 >cd0000                           JSR     INDXP
320 00000204 >3c00                     LLOP    INC     COUNT           LOOP ROUND RED, GREEN & YELLOW
321 00000206 >b600                             LDA     W3
322 00000208 >b700                             STA     R10
323 0000020a  ad43                             BSR     GLP1            GET LINKED PAGE No.
324 0000020c  2406                             BHS     NOTFND          ALREADY IN RAM ?
325 0000020e >be00                             LDX     COUNT           YES, SAVE ACC No.
326 00000210 >e700                             STA     ACC,X           AGAINST COLOUR
327 00000212  2003                             BRA     NEXTC
328 00000214 >cd0000                   NOTFND  JSR     PUSH            NOT IN RAM, SO SAVE
329 00000217 >b600                     NEXTC   LDA     W3              PAGE NUMBER IN LIFO
330 00000219  ab06                             ADD     #6
331 0000021b >b700                             STA     W3              NEXT LINK
332 0000021d >b600                             LDA     COUNT
333 0000021f  a103                             CMP     #3              ALL DONE ?
334 00000221  25e1                             BLO     LLOP
335
336 00000223 >cd0000                           JSR     GCYI            GET CYAN AND INDEX LINKS
337 00000226 >3f00                             CLR     WACC
338 00000228  a604                             LDA     #4
339 0000022a >b700                             STA     COUNT
340
341 0000022c >3a00                     LLOOP   DEC     COUNT
342 0000022e >be00                             LDX     COUNT
343 00000230 >e600                             LDA     ACC,X
344 00000232  a1ff                             CMP     #$FF            IF STILL AN ACC AT $FF THEN
345 00000234  2612                             BNE     ALOC            RECOVER PAGE No. FROM LIFO
346 00000236 >cd0000                           JSR     PULL
347 00000239 >b600                             LDA     WACC
348 0000023b >cd0000                           JSR     CHCK1           ALREADY USED ? IF SO INCREMENT
349 0000023e >be00                             LDX     COUNT
350 00000240 >e700                             STA     ACC,X
351 00000242 >cd0000                           JSR     UP
352 00000245 >cd0000                           JSR     GLP2
353 00000248 >b600                     ALOC    LDA     COUNT
354 0000024a  a101                             CMP     #$01
355 0000024c  22de                             BHI     LLOOP
356
357 0000024e  81                               RTS
358
359                                     ******************************************************
360                                     *                                                    *
361                                     *       Fetch linked page & magazine numbers.        *
362                                     *                                                    *
363                                     ******************************************************
364
365 0000024f >b600                     GLP1    LDA     R10
366 00000251  a113                             CMP     #19             IF INDEX IGNORE LINK CONTROL
367 00000253  2203                             BHI     COR
368 00000255 >07006c                           BRCLR   3,STAT3,NOTOK   LINKS OK ?
369 00000258  a610                     COR     LDA     #16             YES, ROW 16 FOR LINKED PAGES
370 0000025a >cd0000                           JSR     R2B             FETCH 2 LINK BYTES
371 0000025d >b601                             LDA     IOBUF+1
372 0000025f >cd0000                           JSR     DECODE          DECODE UNITS
373 00000262 >b700                             STA     W2
374 00000264 >b600                             LDA     IOBUF
375 00000266 >cd0000                           JSR     DECODE          DECODE TENS
376 00000269 >b700                             STA     PT
377 0000026b >b600                             LDA     W2
378 0000026d >b700                             STA     PU
379 0000026f >cd0000                           JSR     INDX            CHECK FOR ZERO ?
380 00000272 >e600                             LDA     PAG0,X          FETCH CURRENT MAG. NO.
381 00000274 >b700                             STA     PH              PAGE HUNDREDS
382
383 00000276 >cd0000                   R2BJ1   JSR     RADIO
384 00000279 >070009                           BRCLR   3,IOBUF,OK0     MAG BIT ZERO OK ?
385 0000027c >000004                           BRSET   0,PH,H1         NO, SO TOGGLE
386 0000027f >1000                             BSET    0,PH
387 00000281  2002                             BRA     OK0
388 00000283 >1100                     H1      BCLR    0,PH
389 00000285 >cd0000                   OK0     JSR     RADIO
390 00000288 >050009                           BRCLR   2,IOBUF,OK1     MAG BIT ONE OK ?
391 0000028b >020004                           BRSET   1,PH,PT1        NO, SO TOGGLE
392 0000028e >1200                             BSET    1,PH
393 00000290  2002                             BRA     OK1
394 00000292 >1300                     PT1     BCLR    1,PH
395 00000294 >070009                   OK1     BRCLR   3,IOBUF,OK2     MAG BIT TWO OK ?
396 00000297 >040004                           BRSET   2,PH,PU1        NO, SO TOGGLE
397 0000029a >1400                             BSET    2,PH
398 0000029c  2002                             BRA     OK2
399 0000029e >1500                     PU1     BCLR    2,PH
400 000002a0 >cc0000                   OK2     JMP     SRCH
401
402 000002a3 >cd0000                   R2BJ2   JSR     R2B             FETCH 2 LINK BYTES
403 000002a6 >b601                             LDA     IOBUF+1
404 000002a8 >cd0000                           JSR     DECODE          DECODE UNITS
405 000002ab >b700                             STA     PU
406 000002ad >b600                             LDA     IOBUF
407 000002af >cd0000                           JSR     DECODE          DECODE TENS
408 000002b2 >b700                             STA     PT
409 000002b4  20c0                             BRA     R2BJ1
410
411 000002b6 >cd0000                   NOTTH   JSR     REL1
412 000002b9  a018                             SUB     #$18
413 000002bb >b700                             STA     R3
414 000002bd  a604                             LDA     #4
415 000002bf >cc0000                           JMP     SPM
```

```
                                ****************************************************
                                *                                                  *
                                *       New bits for default (+1 & -1) links.      *
                                *                                                  *
                                ****************************************************

000002c2 >1d00          NOTOK3  BCLR    6,STAT          CANCELL SUB-PAGE
000002c4 >cd0000        NOTOK   JSR     INDX
000002c7 >e600                  LDA     PAG0,X
000002c9 >b700                  STA     PH
000002cb >b602                  LDA     PAGE+2
000002cd  4c                    INCA
000002ce >b700                  STA     PU
000002d0 >b702                  STA     PAGE+2
000002d2  a139                  CMP     #$39
000002d4  2312                  BLS     NOV9
000002d6  a630                  LDA     #$30
000002d8 >b700                  STA     PU
000002da >b702                  STA     PAGE+2
000002dc >3c01                  INC     PAGE+1
000002de >b601                  LDA     PAGE+1
000002e0  a139                  CMP     #$39
000002e2  2304                  BLS     NOV9
000002e4  a630                  LDA     #$30
000002e6 >b701          NOV9A   STA     PAGE+1
000002e8 >b601          NOV9    LDA     PAGE+1
000002ea >b700                  STA     PT
000002ec  20b2                  BRA     OK2

000002ee >1d00          NOTOK2  BCLR    6,STAT          CANCEL SUB-PAGE
000002f0 >e600                  LDA     PAG0,X
000002f2 >b700                  STA     PH
000002f4 >b602                  LDA     PAGE+2
000002f6  4a                    DECA
000002f7 >b700                  STA     PU
000002f9 >b702                  STA     PAGE+2
000002fb  a130                  CMP     #$30
000002fd  24e9                  BHS     NOV9
000002ff  a639                  LDA     #$39
00000301 >b700                  STA     PU
00000303 >b702                  STA     PAGE+2
00000305 >3a01                  DEC     PAGE+1
00000307 >b601                  LDA     PAGE+1
00000309  a130                  CMP     #$30
0000030b  24db                  BHS     NOV9
0000030d  a639                  LDA     #$39
0000030f  20d5                  BRA     NOV9A

                                ****************************************************
                                *                                                  *
                                *       Request new linked page.                   *
                                *                                                  *
                                ****************************************************

00000311 >b700          GLP2    STA     R2
00000313  44                    LSRA
00000314  44                    LSRA
00000315  44                    LSRA
00000316 >b700                  STA     C2              x2
00000318  44                    LSRA
00000319 >bb00                  ADD     C2              x3
0000031b  97                    TAX                     X <- 3 x ACC No.
0000031c >b600                  LDA     PU
0000031e >b700                  STA     C2
00000320 >e702                  STA     PAG0+2,X
00000322 >b600                  LDA     PT
00000324 >b700                  STA     C1
00000326 >e701                  STA     PAG0+1,X
00000328 >b600                  LDA     PH
0000032a >e700                  STA     PAG0,X
0000032c  a018                  SUB     #$18
0000032e >b700                  STA     R3

00000330  a309                  CPX     #9
00000332  221c                  BHI     ABORT
00000334  a650                  LDA     #$50
00000336 >b700                  STA     R11
00000338 >b600                  LDA     WACC            ACC
0000033a  ab08                  ADD     #$08            CLEAR CHAPTER
0000033c >b700                  STA     R8              INTO IIC
0000033e >3f00                  CLR     R9              ROW 0
00000340  a602                  LDA     #2              COLUMN 2
00000342 >b700                  STA     R10
00000344 >b600                  LDA     C2
00000346  a139                  CMP     #$39
00000348  2206                  BHI     ABORT
0000034a >b600                  LDA     C1
0000034c  a139                  CMP     #$39
0000034e  2301                  BLS     LOK
00000350  81            ABORT   RTS

00000351 >cd0000        LOK     JSR     TXT3            CLEAR CHAPTER
00000354  a606                  LDA     #6              WAIT
00000356 >cd0000                JSR     TPAU2           FOR IT
00000359 >1700                  BCLR    3,R8            DON'T CLEAR THIS TIME
0000035b >cd0000                JSR     TXT38           PUT PAGE NUMBER IN CHAPTER
0000035e >cd0000                JSR     SFND            SET FOUND FLAG
00000361 >cc0000                JMP     TXT1L           AND REQUEST IT

00000364  ae08          PUSH    LDX     #8
00000366 >e600          PSHL    LDA     PH,X
00000368 >e700                  STA     LIFO,X
0000036a  5a                    DECX
0000036b  2af9                  BPL     PSHL
0000036d  81                    RTS
```

```
523                                 ********************************************************
524                                 *                                                      *
525                                 *       Is page already in RAM ?                       *
526                                 *                                                      *
527                                 ********************************************************
528
529 0000036e >3f00                  SRCH    CLR     WACC
530 00000370 >b600                  LOOPS   LDA     WACC
531 00000372  48                            LSLA
532 00000373 >bb00                          ADD     WACC
533 00000375  97                            TAX
534 00000376 >e600                          LDA     PAG0,X
535 00000378 >b100                          CMP     PH
536 0000037a  260c                          BNE     FINI
537 0000037c >e601                          LDA     PAG0+1,X
538 0000037e >b100                          CMP     PT
539 00000380  2606                          BNE     FINI
540 00000382 >e602                          LDA     PAG0+2,X
541 00000384 >b100                          CMP     PU
542 00000386  2708                          BEQ     FND2
543 00000388 >3c00                  FINI    INC     WACC
544 0000038a >b600                          LDA     WACC
545 0000038c  a104                          CMP     #4
546 0000038e  25e0                          BLO     LOOPS
547
548 00000390 >b600                  FND2    LDA     WACC            IF MATCH THEN CHECK FOR
549 00000392  a104                          CMP     #4              SUB-PAGE MATCH (SHOULD
550 00000394  81                            RTS                     DISPLAY PAGE BE DIFFERENT)
551
552                                 ********************************************************
553                                 *                                                      *
554                                 *       Is Accquisition circuit in use ?               *
555                                 *                                                      *
556                                 ********************************************************
557
558 00000395 >3c00                  SAM     INC     WACC
559 00000397  5f                    CHCK1   CLRX
560 00000398 >b600                  CHCK2   LDA     WACC
561 0000039a >e100                          CMP     ACC,X
562 0000039c  27f7                          BEQ     SAM
563 0000039e  5c                            INCX
564 0000039f  a304                          CPX     #4
565 000003a1  25f5                          BLO     CHCK2
566 000003a3  81                            RTS
567
568 000003a4 >3c00                  RADIO   INC     R10
569 000003a6 >3c00                          INC     R10
570 000003a8 >cd0000                        JSR     R2BN9
571 000003ab >b600                          LDA     IOBUF
572 000003ad >cd0000                        JSR     DECODE
573 000003b0 >bf00                          STX     IOBUF
574 000003b2  81                    DDI     RTS
575
576                                 ********************************************************
577                                 *                                                      *
578                                 *       Transfer ghost row 20 to display row 24.       *
579                                 *       & set found flag.                              *
580                                 *                                                      *
581                                 ********************************************************
582
583 000003b3 >3f00                  ROW24   CLR     R10
584 000003b5 >b600                  MRE     LDA     ACC             CHAPTER
585 000003b7  ab04                          ADD     #4              ADD 4 FOR GHOST ROWS
586 000003b9 >b700                          STA     R8
587 000003bb  a614                          LDA     #20             ROW 20
588 000003bd  ad5a                          BSR     R2B
589
590 000003bf  a620                          LDA     #$20            SPACE
591 000003c1 >b700                          STA     R11
592 000003c3 >b700                          STA     PH
593 000003c5 >070008                        BRCLR   3,STAT3,BLANK   ROW24 ENABLED ?
594
595 000003c8 >b601                          LDA     IOBUF+1         YES, SO USE DATA
596 000003ca >b700                          STA     R11
597 000003cc >b600                          LDA     IOBUF
598 000003ce >b700                          STA     PH
599 000003d0 >b600                  BLANK   LDA     ACC             BACK TO
600 000003d2 >b700                          STA     R8              DISPLAY CHAPTER
601 000003d4  a618                          LDA     #24
602 000003d6  ad31                          BSR     W2B
603 000003d8  23db                          BLS     MRE
604
605 000003da >1800                  SFND    BSET    4,R11           SET FOUND FLAG
606 000003dc  a619                  SFND2   LDA     #25             WRITE IT
607 000003de >b700                          STA     R9              ROW
608 000003e0  a608                          LDA     #8
609 000003e2 >b700                          STA     R10             COLUMN
610 000003e4  a605                          LDA     #5
611 000003e6 >cc0000                        JMP     TXT32
612
613 000003e9 >cd0000                CFND    JSR     CPBLF
614 000003ec  250f                          BCS     ABCF
615 000003ee >1900                          BCLR    4,R11           CLEAR FOUND FLAG
616 000003f0  20ea                          BRA     SFND2
617
618 000003f2 >cd0000                INDXP   JSR     INDX
619 000003f5 >e601                          LDA     PAG0+1,X
620 000003f7 >b701                          STA     PAGE+1
621 000003f9 >e602                          LDA     PAG0+2,X
622 000003fb >b702                          STA     PAGE+2
623 000003fd  81                    ABCF    RTS
624
625 000003fe  5f                    PULL    CLRX
626 000003ff >e600                  PLLL    LDA     LIFO,X
627 00000401 >e700                          STA     PH,X
628 00000403  5c                            INCX
629 00000404  a309                          CPX     #9
630 00000406  25f7                          BLO     PLLL
631 00000408  81                            RTS
```

```
                                ****************************************************
                                *                                                  *
                                *       Read and write subroutines.                *
                                *                                                  *
                                *       Cyan & Index links & link control byte.    *
                                *                                                  *
                                ****************************************************

00000409 >b700                  W2B     STA     R9              ROW 24
0000040b  a606                          LDA     #6
0000040d >cd0000                        JSR     TXT32
00000410 >3c00                          INC     R10
00000412 >3c00                          INC     R10
00000414 >b600                          LDA     R10
00000416  a126                          CMP     #38
00000418  81                    V5      RTS

00000419 >b700                  R2B     STA     R9              ROW
0000041b  a608                  R2BN9   LDA     #8
0000041d >b700                          STA     SUB3
0000041f  a604                          LDA     #4
00000421 >b700                          STA     W1
00000423 >ae00                          LDX     #SUB3
00000425 >cd0000                        JSR     SEND22
00000428  42                            MUL                     DELAY TO SATISFY
00000429  42                            MUL                     IIC TIMING
0000042a  a60b                          LDA     #11
0000042c >b700                          STA     SUBADR
0000042e  a622                  READ22  LDA     #$22
00000430 >b700                          STA     ADDR
00000432 >cc0000                        JMP     READ

00000435  a613                  GCYI    LDA     #19             CYAN
00000437 >b700                          STA     R10
00000439 >cd0000                        JSR     GLP1
0000043c  a640                          LDA     #$40
0000043e >cd0000                        JSR     GLP2
00000441  a61f                          LDA     #31             INDEX
00000443 >b700                          STA     R10
00000445 >cd0000                        JSR     GLP1
00000448  a650                          LDA     #$50
0000044a >cc0000                        JMP     GLP2

0000044d >b600                  CLINK   LDA     ACC
0000044f  ab04                          ADD     #4
00000451 >b700                          STA     R8
00000453 >3f00                          CLR     STAT3
00000455 >3f00                          CLR     R10
00000457  a610                          LDA     #16
00000459 >cd0000                        JSR     R2B
0000045c >b601                          LDA     IOBUF+1         DESTINATION BYTE
0000045e  260e                          BNE     NPK27           IF NOT ZERO, NO PK27
00000460  a625                          LDA     #37             CHAIN CONTROL BYTE
00000462 >b700                          STA     R10
00000464  a610                          LDA     #16
00000466  adb1                          BSR     R2B
00000468 >b601                          LDA     IOBUF+1
0000046a  ad03                          BSR     DECODE
0000046c >bf00                          STX     STAT3
0000046e  81                    NPK27   RTS

                                ****************************************************
                                *                                                  *
                                *       Hamming decode.                            *
                                *                                                  *
                                ****************************************************

0000046f >b700                  DECODE  STA     W1
00000471  5f                            CLRX
00000472 >d60000                TRA     LDA     HAM,X
00000475 >b100                          CMP     W1
00000477  2732                          BEQ     FNDJ

00000479 >b700                  TRZE    STA     SUB2
0000047b >000004                        BRSET   0,SUB2,ZE1
0000047e >1000                          BSET    0,SUB2
00000480  2002                          BRA     ZE1+2
00000482 >1100                  ZE1     BCLR    0,SUB2
00000484 >cd0000                        JSR     SSUB
00000487  2722                          BEQ     FNDJ

00000489 >d60000                TRON    LDA     HAM,X
0000048c >b700                          STA     SUB2
0000048e >020004                        BRSET   1,SUB2,ON1
00000491 >1200                          BSET    1,SUB2
00000493  2002                          BRA     ON1+2
00000495 >1300                  ON1     BCLR    1,SUB2
00000497  ad7a                          BSR     SSUB
00000499  2774                          BEQ     FND

0000049b >d60000                TRTW    LDA     HAM,X
0000049e >b700                          STA     SUB2
000004a0 >040004                        BRSET   2,SUB2,TW1
000004a3 >1400                          BSET    2,SUB2
000004a5  2002                          BRA     TW1+2
000004a7 >1500                  TW1     BCLR    2,SUB2
000004a9  ad68                          BSR     SSUB
000004ab  2762                  FNDJ    BEQ     FND

000004ad >d60000                TRTH    LDA     HAM,X
000004b0 >b700                          STA     SUB2
000004b2 >060004                        BRSET   3,SUB2,TH1
000004b5 >1600                          BSET    3,SUB2
000004b7  2002                          BRA     TH1+2
000004b9 >1700                  TH1     BCLR    3,SUB2
000004bb  ad56                          BSR     SSUB
000004bd  2750                          BEQ     FND
```

```
                                ********************************************************
                                *                                                      *
                                *       More Hamming decode.                           *
                                *                                                      *
                                ********************************************************

000004bf >d60000        TRFO    LDA     HAM,X
000004c2 >b700                  STA     SUB2
000004c4 >080004                BRSET   4,SUB2,FO1
000004c7 >1800                  BSET    4,SUB2
000004c9  2002                  BRA     FO1+2
000004cb >1900          FO1     BCLR    4,SUB2
000004cd  ad44                  BSR     SSUB
000004cf  273e                  BEQ     FND

000004d1 >d60000        TRFI    LDA     HAM,X
000004d4 >b700                  STA     SUB2
000004d6 >0a0004                BRSET   5,SUB2,FI1
000004d9 >1a00                  BSET    5,SUB2
000004db  2002                  BRA     FI1+2
000004dd >1b00          FI1     BCLR    5,SUB2
000004df  ad32                  BSR     SSUB
000004e1  272c                  BEQ     FND

000004e3 >d60000        TRSI    LDA     HAM,X
000004e6 >b700                  STA     SUB2
000004e8 >0c0004                BRSET   6,SUB2,SI1
000004eb >1c00                  BSET    6,SUB2
000004ed  2002                  BRA     SI1+2
000004ef >1d00          SI1     BCLR    6,SUB2
000004f1  ad20                  BSR     SSUB
000004f3  271a                  BEQ     FND

000004f5 >d60000        TRSE    LDA     HAM,X
000004f8 >b700                  STA     SUB2
000004fa >0e0004                BRSET   7,SUB2,SE1
000004fd >1e00                  BSET    7,SUB2
000004ff  2002                  BRA     SE1+2
00000501 >1f00          SE1     BCLR    7,SUB2
00000503  ad0e                  BSR     SSUB
00000505  2708                  BEQ     FND

00000507  5c                    INCX
00000508  a30f                  CPX     #$0F
0000050a  2203                  BHI     FND
0000050c >cc0000                JMP     TRA
0000050f >d60000        FND     LDA     NUM,X
00000512  81                    RTS

00000513 >b600          SSUB    LDA     SUB2
00000515 >b100                  CMP     W1
00000517  81                    RTS

                                ********************************************************
                                *                                                      *
                                *       Mix/nomix.                                     *
                                *                                                      *
                                ********************************************************

00000518 >0e0015        MIX     BRSET   7,STAT2,NOMIX  ALREADY MIXED ?
0000051b >1e00                  BSET    7,STAT2         NO, SO MIX IT
0000051d  a610                  LDA     #$10            BROADCAST, 312/313 SYNC
0000051f >b700                  STA     R1              ENABLING GHOST ROWS
00000521  a606                  LDA     #$06
00000523 >cd0000                JSR     NOBX
00000526  a66e                  LDA     #$6E
00000528 >b700                  STA     R5
0000052a  a617                  LDA     #$17            $46 FOR NOMIX FLASH/SUBT.
0000052c >b700                  STA     R6
0000052e  2015                  BRA     TRAN2

00000530 >1f00          NOMIX   BCLR    7,STAT2         MIXED, SO NOMIX
00000532  a616                  LDA     #$16            CCT, 312/312 SYNC
00000534 >b700                  STA     R1              ENABLING GHOST ROWS
00000536  a6cc                  LDA     #$CC
00000538 >b700                  STA     R5
0000053a  a646                  LDA     #$46
0000053c >b700                  STA     R6
0000053e  2005                  BRA     TRAN2

00000540  a606          TRAN1   LDA     #6
00000542 >cd0000                JSR     BOX0OF
00000545  a602          TRAN2   LDA     #2
00000547 >cd0000                JSR     SPM             SET-UP SYNC
0000054a  4f                    CLRA
0000054b >cd0000                JSR     BOX0ON
0000054e >1800          TRAN3   BSET    4,STAT
00000550  ad15                  BSR     FR0             FORCE HEADER DISPLAY
00000552  a606                  LDA     #6
00000554 >b700                  STA     TMR             5s TIMER
00000556  a607                  LDA     #$07
00000558 >b700                  STA     R7              ENABLE ALL BOXES

0000055a  a605          TXT2    LDA     #5              DISPLAY CONTROL
0000055c >b700                  STA     W1
0000055e  a604                  LDA     #4
00000560 >b700                  STA     SUB2
00000562 >ae00                  LDX     #SUB2
00000564 >cc0000                JMP     SEND22

00000567  a619          FR0     LDA     #25             FORCE DISPLAY OF HEADER
00000569 >b700                  STA     R9
0000056b  a606                  LDA     #6
0000056d >b700                  STA     R10
0000056f >b600                  LDA     ACC
00000571 >b700                  STA     R8
00000573 >3f00                  CLR     R11
00000575  a605                  LDA     #5
00000577 >cc0000                JMP     TXT32
```

```
852                                 ********************************************************
853                                 *                                                      *
854                                 *       Hold.                                          *
855                                 *                                                      *
856                                 ********************************************************
857
858 0000057a >3f00                HOLD    CLR     PDP
859 0000057c >040062                       BRSET   2,STAT,NOHOLD
860 0000057f >1400                         BSET    2,STAT
861 00000581 >b600                         LDA     ACC
862 00000583 >b700                         STA     R8
863 00000585 >cd0000                       JSR     UP
864 00000588 >3f00                         CLR     R9              ROW 0
865 0000058a >1d00                         BCLR    6,STAT          RESET SUB-PAGE MODE
866 0000058c  5f                           CLRX
867 0000058d  ad2b                         BSR     DISP8
868 0000058f >b600                UCHOLD  LDA     ACC
869 00000591 >b700                         STA     R8              DISPLAY CHAPTER
870 00000593 >cd0000                       JSR     UP
871 00000596 >3f00                         CLR     R9              ROW 0
872 00000598 >1700                         BCLR    3,R3            HOLD
873 0000059a  a604                         LDA     #4
874 0000059c  ad11                         BSR     SPM             WAS TXT1
875 0000059e  20ae                         BRA     TRAN3
876
877 000005a0 >0c000a              TXT1    BRSET   6,STAT,SPM2
878 000005a3 >3f00                TXT1L   CLR     C3
879 000005a5 >3f00                        CLR     C4
880 000005a7 >3f00                        CLR     C5
881 000005a9  a60f                        LDA     #$0F            CORRUPT C6 SO THAT NEXT
882 000005ab >b700                        STA     C6              ARRIVAL IS SEEN BY UPDATE
883 000005ad  a60a                SPM2    LDA     #10
884 000005af >b700                SPM     STA     W1
885 000005b1  a601                        LDA     #1
886 000005b3 >b700                        STA     SUB1
887 000005b5 >ae00                        LDX     #SUB1
888 000005b7 >cc0000                      JMP     SEND22
889
890 000005ba >bf00                DISP8   STX     W3
891 000005bc >3f00                        CLR     R9
892 000005be  4f                          CLRA
893 000005bf  ad07                        BSR     DISP4
894 000005c1 >b600                        LDA     W3
895 000005c3  ab04                        ADD     #4
896 000005c5  97                          TAX
897 000005c6  a604                        LDA     #4
898 000005c8 >b700                DISP4   STA     R10
899 000005ca >d60000                      LDA     LHOLD,X
900 000005cd >b700                        STA     R11
901 000005cf >d60001                      LDA     LHOLD+1,X
902 000005d2 >b700                        STA     PH
903 000005d4 >d60002                      LDA     LHOLD+2,X
904 000005d7 >b700                        STA     PT
905 000005d9 >d60003                      LDA     LHOLD+3,X
906 000005dc >b700                        STA     PU
907 000005de >cc0000                      JMP     TXT3
908
909                                 ********************************************************
910                                 *                                                      *
911                                 *       Nohold.                                        *
912                                 *                                                      *
913                                 ********************************************************
914
915 000005e1 >1500                NOHOLD  BCLR    2,STAT
916 000005e3 >b600                        LDA     ACC
917 000005e5 >b700                        STA     R8
918 000005e7 >3f00                        CLR     R9              ROW 0
919 000005e9  a602                        LDA     #2
920 000005eb >b700                        STA     R10             COLUMN 2
921 000005ed  a650                        LDA     #$50
922 000005ef >b700                        STA     R11             P
923 000005f1  ad0b                        BSR     REL1
924 000005f3  ad14                        BSR     REL2
925 000005f5 >cd0000                      JSR     TXT38
926 000005f8 >cd0000                      JSR     SFND
927 000005fb >cc0000                      JMP     TRAN2
928
929 000005fe >b600                REL1    LDA     ACC
930 00000600 >cd0000                      JSR     UP
931 00000603 >cd0000                      JSR     INDX
932 00000606 >e600                        LDA     PAG0,X
933 00000608  81                          RTS
934 00000609 >b700                REL2    STA     PH
935 0000060b  a018                        SUB     #$18
936 0000060d >b700                        STA     R3
937 0000060f >e601                        LDA     PAG0+1,X
938 00000611 >b700                        STA     PT
939 00000613 >b700                        STA     C1
940 00000615 >e602                        LDA     PAG0+2,X
941 00000617 >b700                        STA     PU
942 00000619 >b700                        STA     C2
943 0000061b >cc0000                      JMP     TXT1
944
945 0000061e >b600                CPBLF   LDA     ACC
946 00000620 >b700                        STA     R8
947 00000622  a609                        LDA     #9
948 00000624 >b700                        STA     R10
949 00000626  a619                        LDA     #25
950 00000628 >cd0000                      JSR     R2B
951 0000062b  99                          SEC
952 0000062c >0a0101                      BRSET   5,IOBUF+1,HIGH
953 0000062f  98                          CLC
954 00000630  81                HIGH    RTS
```

```
                                ****************************************************
                                *                                                  *
                                *       Reveal,top/bottom & clock.                 *
                                *                                                  *
                                ****************************************************

00000631 >0a0004        REVEAL  BRSET   5,R7,REV
00000634 >1a00                  BSET    5,R7
00000636  2016                  BRA     OUT
00000638 >1b00          REV     BCLR    5,R7
0000063a  2012                  BRA     OUT
0000063c >07000b        EXPTB   BRCLR   3,R7,EXP
0000063f >090004                BRCLR   4,R7,BOT
00000642 >1700                  BCLR    3,R7            SINGLE HEIGHT
00000644  2008                  BRA     OUT
00000646 >1800          BOT     BSET    4,R7            BOTTOM
00000648  2004                  BRA     OUT
0000064a >1600          EXP     BSET    3,R7
0000064c >1900                  BCLR    4,R7            TOP
0000064e >cc0000        OUT     JMP     TXT2

00000651 >0c00dc        TIME    BRSET   6,STAT7,HIGH    TELETEXT CHIP ?
00000654 >010003                BRCLR   0,STAT,CLOCK    TELETEXT MODE ?
00000657 >cc0000                JMP     SUBPG           YES
0000065a >0a0025        CLOCK   BRSET   5,STAT,TAO      NO, TIME ALREADY ON ?
0000065d >b600                  LDA     ACC
0000065f >b700                  STA     R4
00000661 >cd0000                JSR     UCHOLD
00000664 >1800                  BSET    4,STAT
00000666 >1a00                  BSET    5,STAT
00000668  4f                    CLRA
00000669  ad1c                  BSR     NOBX
0000066b  a61e                  LDA     #30
0000066d  ad1e                  BSR     BOX0ON
0000066f >cd0000                JSR     FR0
00000672  a609                  LDA     #$09
00000674 >b700                  STA     R7
00000676 >cd0000                JSR     TXT2            STOP FLASHES ON FIRST PRESS
00000679  a646                  LDA     #$46
0000067b >b700                  STA     R5
0000067d >b700                  STA     R6
0000067f >cd0000                JSR     TXT2
00000682  a606          TAO     LDA     #6
00000684 >b700                  STA     TMR
00000686  81                    RTS
00000687 >b700          NOBX    STA     R10
00000689  a620                  LDA     #$20
0000068b  200a                  BRA     BOX
0000068d >b700          BOX0ON  STA     R10
0000068f  a60b                  LDA     #$0B
00000691  2004                  BRA     BOX
00000693 >b700          BOX0OF  STA     R10
00000695  a60a                  LDA     #$0A
00000697 >b700          BOX     STA     R11
00000699 >b700                  STA     PH
0000069b >b600                  LDA     R4
0000069d >b700                  STA     R8
0000069f >3f00                  CLR     R9
000006a1  a606                  LDA     #6
000006a3 >cc0000                JMP     TXT32
```

```
1017                            ********************************************************
1018                            *                                                      *
1019                            *       Sub-page number entry routine.                 *
1020                            *                                                      *
1021                            ********************************************************
1022
1023 000006a6 >cd0000  DIGITS  JSR     TPSTP
1024 000006a9 >b600            LDA     W2
1025 000006ab  a010            SUB     #16
1026 000006ad >be00    SD0     LDX     PDP
1027 000006af  2704            BEQ     THOU
1028 000006b1  a302            CPX     #2
1029 000006b3  260f            BNE     SORTD
1030 000006b5  a107    THOU    CMP     #7              THOUSANDS OR TENS
1031 000006b7  2302            BLS     SOCH            NO, SO DON'T CHANGE
1032 000006b9  a008            SUB     #8              YES, 8->0 & 9->1
1033 000006bb  5d      SOCH    TSTX                    WAS  CPX  #0
1034 000006bc  2606            BNE     SORTD
1035 000006be  a103            CMP     #3              MORE THAN 3 ?
1036 000006c0  2302            BLS     SORTD           NO
1037 000006c2  a004            SUB     #4              YES, 4->0 THRU 7->3
1038 000006c4  ab30    SORTD   ADD     #$30            CONVERT TO ASCII
1039 000006c6 >e703            STA     PAGE+3,X
1040 000006c8  a303            CPX     #3              UNITS ?
1041 000006ca  2714            BEQ     SLRPD           YES, SO CLEAR PDP
1042 000006cc  a62a            LDA     #$2A            ASTERISK
1043 000006ce  a301            CPX     #1              HUNDREDS ?
1044 000006d0  2706            BEQ     HUN             YES, SO LEAVE HUNDREDS
1045 000006d2  a302            CPX     #2              TENS ?
1046 000006d4  2704            BEQ     SEN             YES, SO LEAVE TENS & HUNDREDS ?
1047 000006d6 >b704            STA     PAGE+4          CLEAR HUNDREDS
1048 000006d8 >b705    HUN     STA     PAGE+5          CLEAR TENS
1049 000006da >b706    SEN     STA     PAGE+6          CLEAR UNITS
1050 000006dc >3c00            INC     PDP
1051 000006de  2002            BRA     SPGN
1052 000006e0 >3f00    SLRPD   CLR     PDP
1053 000006e2 >b600    SPGN    LDA     ACC
1054 000006e4 >b700            STA     R8
1055 000006e6  4f              CLRA
1056 000006e7 >b700            STA     R9              ROW 0
1057 000006e9 >cd0000          JSR     BOX0ON          COLUMN 0
1058 000006ec  a602            LDA     #2
1059 000006ee >b700            STA     R10             COLUMN 2
1060 000006f0 >b603            LDA     PAGE+3
1061 000006f2 >b700            STA     R11
1062 000006f4 >b604            LDA     PAGE+4
1063 000006f6 >b700            STA     PH
1064 000006f8 >b605            LDA     PAGE+5
1065 000006fa >b700            STA     PT
1066 000006fc >b606            LDA     PAGE+6
1067 000006fe >b700            STA     PU
1068 00000700 >cd0000          JSR     TXT3
1069 00000703 >cd0000          JSR     TRAN1
1070 00000706 >b600            LDA     PDP
1071 00000708  2661            BNE     SBO
1072 0000070a  a606            LDA     #6
1073 0000070c >cd0000          JSR     NOBX
1074 0000070f >b603            LDA     PAGE+3
1075 00000711 >b700            STA     R11
1076 00000713 >b604            LDA     PAGE+4
1077 00000715 >b700            STA     PH
1078
1079                            ********************************************************
1080                            *                                                      *
1081                            *       Get requested sub-page.                        *
1082                            *                                                      *
1083                            ********************************************************
1084
1085 00000717 >b601    SETIT   LDA     PAGE+1
1086 00000719 >b700            STA     C1
1087 0000071b >b602            LDA     PAGE+2
1088 0000071d >b700            STA     C2
1089 0000071f >b603            LDA     PAGE+3
1090 00000721 >b700            STA     C3
1091 00000723 >b604            LDA     PAGE+4
1092 00000725 >b700            STA     C4
1093 00000727 >b605            LDA     PAGE+5
1094 00000729 >b700            STA     C5
1095 0000072b >b606            LDA     PAGE+6
1096 0000072d >b700            STA     C6
1097
1098 0000072f >b600            LDA     PAGE            PAGE HUNDREDS
1099 00000731  a018            SUB     #$18
1100 00000733 >b700            STA     R3              PAGE REQUEST HUNDREDS
1101 00000735 >b600            LDA     ACC
1102 00000737 >cd0000          JSR     UP
1103 0000073a >cd0000          JSR     TXT1            REQUEST IT
1104 0000073d >1500            BCLR    2,STAT          NOHOLD
1105 0000073f >cc0000          JMP     SFND            WRITE ONE TO FOUND
1106
1107 00000742 >b600    TXT38   LDA     PH
1108 00000744  a130            CMP     #$30
1109 00000746  2604            BNE     TXT3
1110 00000748  a638            LDA     #$38
1111 0000074a >b700            STA     PH
1112
1113 0000074c  a608    TXT3    LDA     #8
1114 0000074e >b700    TXT32   STA     W1
1115 00000750  a608            LDA     #8              WRITE CCT RAM VIA IIC
1116 00000752 >b700            STA     SUB3
1117 00000754 >ae00            LDX     #SUB3
1118
1119 00000756  a622    SEND22  LDA     #$22
1120 00000758 >b700            STA     ADDR
1121 0000075a >cc0000          JMP     SEND
1122
1123 0000075d >b600    TPSTP   LDA     PAGE            HOLD DURING
1124 0000075f >b700            STA     R3              SUB-PAGE NUMBER
1125 00000761 >b600            LDA     ACC             ENTRY
1126 00000763 >cd0000          JSR     UP
1127 00000766  a604            LDA     #4
1128 00000768 >cc0000          JMP     SPM
1129 0000076b  81      SBO     RTS
```

```
1131                                    ********************************************************
1132                                    *                                                      *
1133                                    *       Sub (timed) pages.                             *
1134                                    *                                                      *
1135                                    ********************************************************
1136
1137 0000076c >0c002e                  SUBPG   BRSET   6,STAT,OUTSP
1138 0000076f >1c00                            BSET    6,STAT
1139 00000771  adea                            BSR     TPSTP
1140 00000773 >3f00                            CLR     PDP
1141 00000775 >cd0000                          JSR     INDX
1142 00000778 >e600                            LDA     PAG0,X
1143 0000077a >b700                            STA     PAGE
1144 0000077c >e601                            LDA     PAG0+1,X
1145 0000077e >b701                            STA     PAGE+1
1146 00000780 >e602                            LDA     PAG0+2,X
1147 00000782 >b702                            STA     PAGE+2
1148 00000784  a62a                            LDA     #$2A            *
1149 00000786 >b700                            STA     R11
1150 00000788 >b700                            STA     PH
1151 0000078a >b700                            STA     PT
1152 0000078c >b700                            STA     PU
1153 0000078e >b600                            LDA     ACC
1154 00000790 >b700                            STA     R8
1155 00000792 >3f00                            CLR     R9
1156 00000794  a602                            LDA     #2
1157 00000796 >b700                            STA     R10
1158 00000798  adb2                            BSR     TXT3
1159 0000079a >cc0000                          JMP     TRAN1
1160
1161 0000079d  ad0d                    OUTSP   BSR     RSTR
1162 0000079f >b600                            LDA     ACC
1163 000007a1 >cd0000                          JSR     UP
1164 000007a4 >1500                            BCLR    2,STAT          RESET HOLD FLAG
1165 000007a6 >cd0000                          JSR     TXT1
1166 000007a9 >cc0000                          JMP     TRAN1
1167
1168 000007ac >1d00                    RSTR    BCLR    6,STAT
1169 000007ae >3f00                            CLR     PDP
1170 000007b0  a650                            LDA     #$50            P
1171 000007b2 >b700                            STA     R11
1172 000007b4 >cd0000                          JSR     INDX
1173 000007b7 >e600                            LDA     PAG0,X
1174 000007b9 >b700                            STA     PH
1175 000007bb  a018                            SUB     #$18
1176 000007bd >b700                            STA     R3
1177 000007bf >e601                            LDA     PAG0+1,X
1178 000007c1 >b700                            STA     PT
1179 000007c3 >b700                            STA     C1
1180 000007c5 >e602                            LDA     PAG0+2,X
1181 000007c7 >b700                            STA     PU
1182 000007c9 >b700                            STA     C2
1183 000007cb >3f00                            CLR     R9
1184 000007cd  a602                            LDA     #2
1185 000007cf >b700                            STA     R10
1186 000007d1 >b600                            LDA     ACC
1187 000007d3 >b700                            STA     R8
1188 000007d5 >cc0000                          JMP     TXT38
1189
1190                                    ********************************************************
1191                                    *                                                      *
1192                                    *       Read in Row 25 information.                    *
1193                                    *                                                      *
1194                                    ********************************************************
1195
1196 000007d8 >b600                    GET25   LDA     ACC
1197 000007da >b700                            STA     R8
1198 000007dc >1b00                            BCLR    5,STAT2         CLEAR DIFFERENCE FLAG
1199 000007de  a602                            LDA     #2              COLUMN 2 (MINUTES)
1200 000007e0 >b700                            STA     R10
1201 000007e2  a619                            LDA     #25             ROW
1202 000007e4 >cd0000                          JSR     R2B
1203 000007e7 >b601                            LDA     IOBUF+1
1204 000007e9 >b100                            CMP     C6
1205 000007eb  2704                            BEQ     SM6
1206 000007ed >1a00                            BSET    5,STAT2
1207 000007ef >b700                            STA     C6              MINUTES UNITS
1208 000007f1 >b600                    SM6     LDA     IOBUF
1209 000007f3 >b700                            STA     SUB2            MINUTES TENS & CBIT 4
1210
1211 000007f5  a604                            LDA     #4              COLUMN 4 (HOURS)
1212 000007f7 >b700                            STA     R10
1213 000007f9  a619                            LDA     #25             ROW
1214 000007fb >cd0000                          JSR     R2B
1215 000007fe >b601                            LDA     IOBUF+1
1216 00000800 >b100                            CMP     C4
1217 00000802  2704                            BEQ     SM4
1218 00000804 >1a00                            BSET    5,STAT2
1219 00000806 >b700                            STA     C4              HOURS UNITS
1220 00000808 >b600                    SM4     LDA     IOBUF
1221 0000080a >b100                            CMP     C3
1222 0000080c  2704                            BEQ     SM3
1223 0000080e >1a00                            BSET    5,STAT2
1224 00000810 >b700                            STA     C3              HOURS TENS & CBITS 5 & 6
1225
1226 00000812  a40c                    SM3     AND     #$0C            SAVE CBITS 5 & 6 IN STAT7
1227 00000814 >1500                            BCLR    2,STAT7         CLEAR NEWSFLASH BIT
1228 00000816 >1700                            BCLR    3,STAT7         CLEAR SUBTITLE BIT
1229 00000818 >ba00                            ORA     STAT7
1230 0000081a >b700                            STA     STAT7
1231 0000081c  a606                            LDA     #6              COLUMN 6 (CONTROL BITS)
1232 0000081e >b700                            STA     R10
1233 00000820  a619                            LDA     #25             ROW
1234 00000822 >cd0000                          JSR     R2B
1235 00000825 >1700                            BCLR    3,SUB2          XFER CBIT8 (UPDATE)
1236 00000827 >030102                          BRCLR   1,IOBUF+1,TR5   TO BIT 3 OF MINUTES TENS
1237 0000082a >1600                            BSET    3,SUB2          (REPLACING CBIT4 (ERASE))
1238 0000082c >b600                    TR5     LDA     SUB2
1239 0000082e >b100                            CMP     C5
1240 00000830  2704                            BEQ     CGET26
1241 00000832 >1a00                            BSET    5,STAT2
1242 00000834 >b700                            STA     C5
1243
1244 00000836  0f0101                  CGET26  BRCLR   7,PORTB,GET26   PACKET 26 ENABLED ?
1245 00000839  81                              RTS
```

```
1247                                ********************************************************
1248                                *                                                      *
1249                                *       Process packet 26 info.                        *
1250                                *                                                      *
1251                                ********************************************************
1252
1253 0000083a  a6ff          GET26   LDA     #$FF
1254 0000083c >b700                  STA     LIFO
1255
1256 0000083e >3f01          LOOP26  CLR     LIFO+1          START NEW ROW
1257 00000840 >b600                  LDA     ACC
1258 00000842  ab04                  ADD     #4              GHOST CHAPTER
1259 00000844 >b700                  STA     R8
1260 00000846 >b601                  LDA     LIFO+1
1261 00000848 >b700                  STA     R10
1262 0000084a >3c00                  INC     LIFO
1263 0000084c >b600                  LDA     LIFO
1264 0000084e  a10e                  CMP     #14             STILL PACKET 26 ?
1265 00000850  2303                  BLS     OKROW
1266 00000852 >cc0000                JMP     END26
1267 00000855 >b600          OKROW   LDA     LIFO
1268 00000857 >cd0000                JSR     R2B
1269 0000085a >b601                  LDA     IOBUF+1
1270 0000085c >b100                  CMP     LIFO            IS BYTE ZERO OK ?
1271 0000085e  26de                  BNE     LOOP26          NO, TRY NEXT ROW
1272 00000860 >3a01                  DEC     LIFO+1
1273
1274 00000862 >b600          LOOP62  LDA     ACC
1275 00000864  ab04                  ADD     #4
1276 00000866 >b700                  STA     R8
1277 00000868 >3c01                  INC     LIFO+1
1278 0000086a >3c01                  INC     LIFO+1
1279 0000086c >b601                  LDA     LIFO+1
1280 0000086e >b700                  STA     R10
1281 00000870  a126                  CMP     #38             PAST END OF ROW ?
1282
1283
1284 00000872  230d                  BLS     NXTCH
1285 00000874 >3f00                  CLR     R10             YES, BLOW AWAY ROW
1286 00000876  a6ff                  LDA     #$FF
1287 00000878 >b700                  STA     R11             CORRUPT SEQUENCE No.
1288 0000087a >b600                  LDA     LIFO
1289 0000087c >cd0000                JSR     W2B
1290 0000087f  20bd                  BRA     LOOP26          NEXT ROW
1291
1292 00000881 >b600          NXTCH   LDA     LIFO
1293 00000883 >cd0000                JSR     R2B             GET 2 BYTES
1294 00000886 >b601                  LDA     IOBUF+1
1295 00000888 >b708                  STA     LIFO+8
1296 0000088a >b600                  LDA     IOBUF
1297 0000088c >b707                  STA     LIFO+7
1298 0000088e >3c01                  INC     LIFO+1
1299 00000890 >b601                  LDA     LIFO+1
1300 00000892 >b700                  STA     R10
1301 00000894 >cd0000                JSR     R2BN9           GET THIRD BYTE
1302
1303 00000897 >b600                  LDA     IOBUF
1304 00000899 >b706                  STA     LIFO+6
1305 0000089b >b607                  LDA     LIFO+7
1306 0000089d  a47c                  AND     #$7C
1307 0000089f  44                    LSRA
1308 000008a0  44                    LSRA
1309 000008a1 >b702                  STA     LIFO+2          SAVE MODE
1310 000008a3 >cd0000                JSR     EXAD
1311 000008a6 >b605                  LDA     LIFO+5
1312 000008a8  a128                  CMP     #40             ROW 24 ?
1313 000008aa  2706                  BEQ     RW24
1314 000008ac  250a                  BLO     NOTROW
1315
1316 000008ae  a028                  SUB     #40             SUBTRACT 40 FOR ROW
1317 000008b0  2002                  BRA     SKIP
1318 000008b2  a618          RW24    LDA     #24
1319
1320 000008b4 >b704          SKIP    STA     LIFO+4
1321 000008b6  20aa                  BRA     LOOP62
1322
1323 000008b8 >b604          NOTROW  LDA     LIFO+4
1324 000008ba >b700                  STA     R9
1325 000008bc >b600                  LDA     ACC
1326 000008be >b700                  STA     R8
1327 000008c0 >b605                  LDA     LIFO+5
1328 000008c2 >b700                  STA     R10
1329
1330 000008c4 >090241                BRCLR   4,LIFO+2,NOTD   DIACRITICAL ?
1331 000008c7 >b602                  LDA     LIFO+2
1332 000008c9  a110                  CMP     #$10            NULL ?
1333 000008cb  2775                  BEQ     NULD            YES, JUST SEND IT (BIT7=1)
1334
1335 000008cd  5f                    CLRX
1336 000008ce >1f06                  BCLR    7,LIFO+6
1337 000008d0 >d60000        TRNCH   LDA     CTAB,X
1338 000008d3 >b106                  CMP     LIFO+6
1339 000008d5  270a                  BEQ     CHFND
1340 000008d7  9f                    TXA
1341 000008d8  ab07                  ADD     #7
1342 000008da  97                    TAX
1343 000008db  a15b                  CMP     #91
1344 000008dd  23f1                  BLS     TRNCH
1345 000008df  2063                  BRA     CHNF
1346
1347 000008e1 >b602          CHFND   LDA     LIFO+2
1348 000008e3  a40f                  AND     #$0F
1349 000008e5 >b703                  STA     LIFO+3
1350 000008e7  275b                  BEQ     CHNF            NULL DIA.
1351 000008e9  a104                  CMP     #4
1352 000008eb  2312                  BLS     GTT
1353 000008ed  a108                  CMP     #8
1354 000008ef  2604                  BNE     NOTCF
1355 000008f1  a003                  SUB     #3
1356 000008f3  2008                  BRA     UOC
```

```
000008f5  a10b                NOTCF   CMP     #11
000008f7  2702                        BEQ     CEDI
000008f9  2049                        BRA     CHNF            ILLEGAL MODE
000008fb  a005                CEDI    SUB     #5
000008fd >b703                UOC     STA     LIFO+3
000008ff  9f                  GTT     TXA
00000900 >bb03                        ADD     LIFO+3
00000902  97                          TAX
00000903 >d60000                      LDA     CTAB,X
00000906  203e                        BRA     GOTCH

00000908 >b602                NOTD    LDA     LIFO+2
0000090a  a10f                        CMP     #$0F
0000090c  271c                        BEQ     G2BIT
0000090e  a102                        CMP     #$02
00000910  263e                        BNE     END26

00000912 >1f06                G3BIT   BCLR    7,LIFO+6
00000914  5f                          CLRX
00000915 >d60000              TN32    LDA     G3TAB,X
00000918  2603                        BNE     STRM
0000091a >cc0000                      JMP     LOOP62
0000091d >b106                STRM    CMP     LIFO+6
0000091f  2704                        BEQ     G32F
00000921  5c                          INCX
00000922  5c                          INCX
00000923  20f0                        BRA     TN32
00000925 >d60001              G32F    LDA     G3TAB+1,X
00000928  201c                        BRA     GOTCH

0000092a >1f06                G2BIT   BCLR    7,LIFO+6
0000092c  5f                          CLRX
0000092d >d60000              TN23    LDA     G2TAB,X
00000930  2603                        BNE     STMR
00000932 >cc0000                      JMP     LOOP62
00000935 >b106                STMR    CMP     LIFO+6
00000937  2704                        BEQ     G23F
00000939  5c                          INCX
0000093a  5c                          INCX
0000093b  20f0                        BRA     TN23
0000093d >d60001              G23F    LDA     G2TAB+1,X
00000940  2004                        BRA     GOTCH

00000942 >1e06                NULD    BSET    7,LIFO+6
00000944 >b606                CHNF    LDA     LIFO+6
00000946 >b700                GOTCH   STA     R11

00000948  a605                        LDA     #5
0000094a >cd0000                      JSR     TXT32
0000094d >cc0000                      JMP     LOOP62

00000950  81                  END26   RTS

                              ********************************************************
                              *                                                      *
                              *       Packet 26 character look-up table.             *
                              *                                                      *
                              ********************************************************

00000951  202021e02383        G2TAB   FCB     $20,$20,$21,$E0,$23,$83
00000957  248426932740                FCB     $24,$84,$26,$93,$27,$40
0000095d  289429a72aa2                FCB     $28,$94,$29,$A7,$2A,$A2
00000963  2cbc2d5e2ebe                FCB     $2C,$BC,$2D,$5E,$2E,$BE
00000969  2f7630cb37c7                FCB     $2F,$76,$30,$CB,$37,$C7
0000096f  388a39a73aa2                FCB     $38,$8A,$39,$A7,$3A,$A2
00000975  3c823d8c3e89                FCB     $3C,$82,$3D,$8C,$3E,$89
0000097b  3fe161f963e5                FCB     $3F,$E1,$61,$F9,$63,$E5
00000981  69fd6be66cfe                FCB     $69,$FD,$6B,$E6,$6C,$FE
00000987  71f879fc7cff                FCB     $71,$F8,$79,$FC,$7C,$FF
0000098d  7f7f00                      FCB     $7F,$7F,$00

00000990  51815b8d5c8b        G3TAB   FCB     $51,$81,$5B,$8D,$5C,$8B
00000996  5d8e5f2000                  FCB     $5D,$8E,$5F,$20,$00

0000099b  61eaebd2c59261      CTAB    FCB     $61,$EA,$EB,$D2,$C5,$92,$61       a
000009a2  41f1f041d59b41              FCB     $41,$F1,$F0,$41,$D5,$9B,$41       A
000009a9  65e9ecdc65db65              FCB     $65,$E9,$EC,$DC,$65,$DB,$65       e
000009b0  45f2904545454545            FCB     $45,$F2,$90,$45,$45,$45,$45       E
000009b7  6969edde69d469              FCB     $69,$69,$ED,$DE,$69,$D4,$69       i
000009be  4949f34949f449              FCB     $49,$49,$F3,$49,$49,$F4,$49       I
000009c5  6fc8eed8c6986f              FCB     $6F,$C8,$EE,$D8,$C6,$98,$6F       o
000009cc  4ff6f5d8d69c4f              FCB     $4F,$F6,$F5,$D8,$D6,$9C,$4F       O
000009d3  75c1efd975e275              FCB     $75,$C1,$EF,$D9,$75,$E2,$75       u
000009da  5555f755559e55              FCB     $55,$55,$F7,$55,$55,$9E,$55       U
000009e1  6e6e6e6ee86e6e              FCB     $6E,$6E,$6E,$6E,$E8,$6E,$6E       n
000009e8  4e4e4e4ee74e4e              FCB     $4E,$4E,$4E,$4E,$E7,$4E,$4E       N
000009ef  6363636363e363              FCB     $63,$63,$63,$63,$63,$63,$E3       c
000009f6  434343434343d7              FCB     $43,$43,$43,$43,$43,$43,$D7       C

000009fd >3f05                EXAD    CLR     LIFO+5
000009ff >030702                      BRCLR   1,LIFO+7,NO32
00000a02 >1a05                        BSET    5,LIFO+5
00000a04 >010702              NO32    BRCLR   0,LIFO+7,NO16
00000a07 >1805                        BSET    4,LIFO+5
00000a09 >0d0802              NO16    BRCLR   6,LIFO+8,NO8
00000a0c >1605                        BSET    3,LIFO+5
00000a0e >0b0802              NO8     BRCLR   5,LIFO+8,NO4
00000a11 >1405                        BSET    2,LIFO+5
00000a13 >090802              NO4     BRCLR   4,LIFO+8,NO2
00000a16 >1205                        BSET    1,LIFO+5
00000a18 >050802              NO2     BRCLR   2,LIFO+8,NO1
00000a1b >1005                        BSET    0,LIFO+5
00000a1d  81                  NO1     RTS
```

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1462                                ****************************************************
1463                                *                                                  *
1464                                *       Fetch initial page from 8/30 format 1.     *
1465                                *                                                  *
1466                                ****************************************************
1467
1468 00000a1e >1b00          GIP     BCLR    5,STAT          CLEAR TIME HOLD
1469 00000a20 >1d00                  BCLR    6,STAT          CLEAR SUB-PAGE MODE
1470 00000a22 >1d00                  BCLR    6,STAT2         CLEAR NO TXT FLAG
1471 00000a24 >3f00                  CLR     PDP
1472 00000a26  a602                  LDA     #2
1473 00000a28 >cd0000                JSR     SPM             TXT1 1 BYTE ONLY
1474 00000a2b  a604                  LDA     #4
1475 00000a2d >b700                  STA     R8              CHAPTER 4 (GHOST)
1476 00000a2f  a660                  LDA     #96             96 TRYS
1477 00000a31 >b700                  STA     W3
1478 00000a33 >3a00          TRYAG   DEC     W3
1479 00000a35  2735                  BEQ     IPNF            AGAIN ?
1480 00000a37  a601                  LDA     #1
1481 00000a39 >cd0000                JSR     TPAU2
1482 00000a3c >3f00                  CLR     R10
1483 00000a3e  a617                  LDA     #23
1484 00000a40 >cd0000                JSR     R2B
1485 00000a43 >b601                  LDA     IOBUF+1         8/30 FORMAT 1 FOR INITIAL PAGE
1486 00000a45  26ec                  BNE     TRYAG
1487 00000a47  a601                  LDA     #1              COLUMN 1
1488 00000a49 >b700                  STA     R10
1489 00000a4b  a630                  LDA     #$30            RESET PAGE HUNDREDS
1490 00000a4d >b700                  STA     PH
1491 00000a4f  a617                  LDA     #23             LINE 23 (PACKET 8/30)
1492 00000a51 >cd0000                JSR     R2BJ2
1493 00000a54 >b600          GETIND  LDA     PH              INITIALISE INDEX (BLACK)
1494 00000a56 >b700                  STA     PAGI
1495 00000a58 >b700                  STA     PAGE
1496 00000a5a >b600                  LDA     PT
1497 00000a5c >b701                  STA     PAGI+1
1498 00000a5e >b600                  LDA     PU
1499 00000a60 >b702                  STA     PAGI+2
1500 00000a62 >b600                  LDA     ACC
1501 00000a64 >b700                  STA     WACC
1502 00000a66 >cd0000                JSR     UP
1503 00000a69 >cc0000                JMP     GLP2
1504 00000a6c >b601          IPNF    LDA     IOBUF+1
1505 00000a6e  a110                  CMP     #$10
1506 00000a70  2502                  BLO     P830OK
1507 00000a72 >1c00                  BSET    6,STAT2
1508 00000a74  a631          P830OK  LDA     #$31            REQUEST
1509 00000a76 >b700                  STA     PH              PAGE 100
1510 00000a78  4a                    DECA                    IN CASE
1511 00000a79 >b700                  STA     PT              INITIAL PAGE
1512 00000a7b >b700                  STA     PU              NOT FOUND
1513 00000a7d  20d5                  BRA     GETIND
1514
1515                                ****************************************************
1516                                *                                                  *
1517                                *       Row 24 transient.                          *
1518                                *                                                  *
1519                                ****************************************************
1520
1521 00000a7f  a604          R24T    LDA     #4
1522 00000a81 >b700                  STA     R8              CHAPTER 4
1523 00000a83  48                    LSLA
1524 00000a84 >b700                  STA     R10             BOX ON AT 8 & 9
1525 00000a86  a60b                  LDA     #$0B
1526 00000a88 >b700                  STA     R11
1527 00000a8a >b700                  STA     PH
1528 00000a8c  a618                  LDA     #24             ROW 24
1529 00000a8e >b700                  STA     R9
1530 00000a90  a606                  LDA     #6
1531 00000a92 >cd0000                JSR     TXT32           WRITE BOX ON
1532 00000a95  a61f                  LDA     #31             BOX OFF AT 31 & 32
1533 00000a97 >b700                  STA     R10
1534 00000a99  a60a                  LDA     #$0A
1535 00000a9b >b700                  STA     R11
1536 00000a9d >b700                  STA     PH
1537 00000a9f  a606                  LDA     #6
1538 00000aa1 >cd0000                JSR     TXT32           WRITE BOX OFF
1539 00000aa4  a614                  LDA     #20
1540 00000aa6 >b700                  STA     W3              START READING @ COLUMN 20
1541 00000aa8 >b700          EA      STA     R10
1542 00000aaa  a617                  LDA     #23             ROW 23 - PACKET 8/30
1543 00000aac >cd0000                JSR     R2B
1544 00000aaf >b601                  LDA     IOBUF+1
1545 00000ab1  a47f                  AND     #$7F
1546 00000ab3 >b700                  STA     R11
1547 00000ab5 >b601                  LDA     IOBUF
1548 00000ab7  a47f                  AND     #$7F
1549 00000ab9 >b700                  STA     PH
1550 00000abb >b600                  LDA     W3
1551 00000abd  a00a                  SUB     #10             START WRITING AT COLUMN 10
1552 00000abf >b700                  STA     R10
1553 00000ac1  a618                  LDA     #24             WRITE TO ROW 24
1554 00000ac3 >cd0000                JSR     W2B
1555 00000ac6 >3c00                  INC     W3
1556 00000ac8 >3c00                  INC     W3
1557 00000aca >b600                  LDA     W3
1558 00000acc  a127                  CMP     #39             ALL DONE ?
1559 00000ace  23d8                  BLS     EA
1560 00000ad0  81            NOTR    RTS
1561
1562 00000ad1 >cd0000        START2  JSR     TXTOF
1563 00000ad4  a614                  LDA     #20
1564 00000ad6 >cd0000        SDLY    JSR     TPAU2
1565 00000ad9  a60c          NIICD   LDA     #$0C
1566 00000adb >b700                  STA     R8
1567 00000add >cd0000                JSR     TXT3            CLEAR CHAPTER 4
1568 00000ae0  a606                  LDA     #6
1569 00000ae2 >cd0000                JSR     TPAU2
1570 00000ae5 >cd0000        INITXT  JSR     GIP             GET PAGE No. FROM 8/30
```

```
1572                                    ********************************************************
1573                                    *                                                      *
1574                                    *       Set up Row 24 transient.                       *
1575                                    *                                                      *
1576                                    ********************************************************
1577
1578 00000ae8 >0c0022                  SR24T   BRSET   6,STAT2,NOTXTX
1579 00000aeb >1a00                             BSET    5,STAT          "TIME HOLD"
1580 00000aed  4f                               CLRA                    *
1581 00000aee >cd0000                           JSR     UP              ACC 0
1582 00000af1 >1700                             BCLR    3,R3            STOP IT
1583 00000af3  a604                             LDA     #4              3 BYTES
1584 00000af5 >cd0000                           JSR     SPM
1585 00000af8  a604                             LDA     #4
1586 00000afa >b700                             STA     R4
1587 00000afc  a606                             LDA     #6
1588 00000afe >b700                             STA     R5
1589 00000b00 >b700                             STA     R6
1590 00000b02  a684                             LDA     #$84            PUT 24 AT TOP ($44 FOR CURSOR)
1591 00000b04 >b700                             STA     R7
1592 00000b06 >cd0000                           JSR     TXT2
1593 00000b09  a606                             LDA     #6
1594 00000b0b >b700                             STA     TMR
1595 00000b0d >1800                  NOTXTX     BSET    4,STAT
1596 00000b0f  81                               RTS
1597
1598
1599
1600                                    ********************************************************
1601                                    *                                                      *
1602                                    *       Tables for HEX-ASCII conversion, "STOP"        *
1603                                    *       and Hamming decode.                            *
1604                                    *                                                      *
1605                                    ********************************************************
1606
1607 00000b10  30313233343536373637      NUM     FCC     "0123456789ABCDEF7"
1608 00000b21  0b0b53544f500a0a          LHOLD   FCB     $0B,$0B,$53,$54,$4F,$50,$0A,$0A
1609 00000b29  1502495e64733d2f          HAM     FCB     $15,$02,$49,$5E,$64,$73,$3D,$2F
1610 00000b31  d0c78c9ba1b6fdea          HAM8    FCB     $D0,$C7,$8C,$9B,$A1,$B6,$FD,$EA
1611
1612                                            END
```

Symbol cross-reference

```
.RAM                *27
.RAM2               *27
.ROM2               *29
ABAV                *27
ABC                  216    220    222    229    261    263   *267
ABCF                 614   *623
ABO                 *93    146
ABORT                491    502   *506
ACC                 *27     54    106    179    181    205    217    223    231    245    288    309    316    317    318    326
                     343    350    561    584    599    676    846    861    868    916    929    945    981   1053   1101   1125
                    1153   1162   1186   1196   1257   1274   1325   1500
ADDR                *27    662   1120
ALOC                 345   *353
ANAF                *27
ANAL                *27
AVOL                *27
BCOL                *27
BLANK                593   *599
BOT                  968   *971
BOX                 1003   1006  *1009
BOX0OF                22    822  *1007
BOX0ON                22    826    989  *1004   1057
BRIL                *27
BROW                *27
C1                  *27    165    276    483    503    939   1086   1179
C2                  *27    168    273    475    477    480    500    942   1088   1182
C3                  *27    878   1090   1221   1224
C4                  *27    879   1092   1216   1219
C5                  *27    880   1094   1239   1242
C6                  *27    242    882   1096   1204   1207
CARO                 234   *238
CAS1                *27
CAS2                *27
CAS3                *27
CAS4                *27
CAS5                *27
CAS6                *27
CAS7                *27
CAS8                *27
CCR1                *27
CCR2                *27
CCR3                *27
CCR4                *27
CCR5                *27
CCR6                *27
CCR7                *27
CCR8                *27
CEDI                1359  *1361
CFND                 246   *613
CGET26              1240  *1244
CHAN                *27
CHCK1                348   *559
CHCK2               *560    565
CHFND               1339  *1347
CHNF                1345   1350   1360  *1402
CLINK                21    *676
CLOCK                978   *980
CLRPD                121   *129    204    214
CNT                 *27
```

Symbol cross-reference

```
CNT1            *27
CNT3            *27
CNT4            *27
CNT5            *27
COK             *239
COR              367   *369
COUNT           *27    312   320   325   332   339   341   342   349   353
CPBLF            613   *945
CTAB             1337  1366  *1432
CYAN             17    *261
CYOK            *297
DDI             *574
DECODE           372   375   404   407   572   690   *700
DIFFH           *27
DIFFL           *27
DIGIT            103   *105
DIGIT0           17    *103
DIGITS           104   *1023
DISC            *27
DISP            *27
DISP4            893   *898
DISP8            867   *890
DPGN             128   *130
DPNT            *27
DRAM            *27
EA              *1541  1559
END26            1266  1373  *1409
EXAD             1310  *1447
EXP              967   *973
EXPTB            18    *967
FI1              758   760   *761
FINI             536   539   *543
FND              721   730   739   754   763   772   781   785   *787
FND2             542   *548
FNDJ             704   712   *730
FO1              749   751   *752
FR0              828   *842   990
FTUNE           *27
G23F             1394  *1398
G2BIT            1371  *1388
G2TAB            1390  1398  *1417
G32F             1381  *1385
G3BIT           *1375
G3TAB            1377  1385  *1429
GCYI             336   *665
GET25            21    *1196
GET26            1244  *1253
GETIND          *1493  1513
GETIT           *158
GIP              18    259   *1468  1570
GLOK             209   *215
GLP1             323   *365   667   672
GLP2             352   *471   669   674   1503
GOTCH            1367  1386  1399  *1403
GREEN            17    *208
GTT              1352  *1363
H1               385   *388
HAM              702   714   723   732   747   756   765   774   *1609
HAM8            *1610

HIGH             952   *954   977
HOLD             19    *858
HUN              1044  *1048
HVL             *27
HVR             *27
IAC              258   266   *269
IG0              215   *217
IG1              221   *223
IG2              262   *264
INDEX            19    *256
INDX             160   *179   281   379   424   618   931   1141  1172
INDXP            201   211   319   *618
INITXT           19    *1570
IOBUF           *27    371   374   384   390   395   403   406   571   573   595   597   683   689   952   1203
                 1208  1215  1220  1236  1269  1294  1296  1303  1485  1504  1544  1547
IPNF             1479  *1504
IRCMCT          *27
IRCNT           *27
IRCODE          *27
IRH             *27
IRL             *27
IRRA1           *27
IRRA2           *27
IRRA3           *27
IRRA4           *27
K1              *27
K2              *27
KEY             *27
KOUNT           *27
LBAL            *27
LD0             *113
LHOLD            899   901   903   905   *1608
LIFO            *27    518   626   1254  1256  1260  1262  1263  1267  1270  1272  1277  1278  1279  1288  1292
                 1295  1297  1298  1299  1304  1305  1309  1311  1320  1323  1327  1330  1331  1336  1338  1347
                 1349  1362  1364  1369  1375  1380  1388  1393  1401  1402  1447  1448  1449  1450  1451  1452
                 1453  1454  1455  1456  1457  1458  1459
LIND            *27
LINK             21    *309
LLOOP           *341   355
LLOP            *320   334
LOK              505   *508
LOOP26          *1256  1271  1290
LOOP62          *1274  1321  1379  1392  1407
LOOPS           *530   546
LPT              203   206   213   218   *224
LPT2             159   *206
LVL             *27
LVR             *27
```

Symbol cross-reference

Symbol cross-reference

```
READ                *24     663
READ22              *661
RED                  17    *198
RED2                 199   *205
REL1                 411    923   *929
REL2                 924   *934
REV                  962   *965
REVEAL               18    *962
ROW1                *27
ROW24                21    *583
RST                 *69
RSTR                 237    1161  *1168
RW24                 1313  *1318
SAM                 *558    562
SBO                  1071  *1129
SDO                 *1026
SDLY                *1564
SEI                  776    778   *779
SEN                  1046  *1049
SEND                *24     1121

SEND22               656    839    888   *1119
SETIT               *1085
SFND                 176    300    513   *605    926    1105
SFND2               *606    616
SHADMAT             *27
SII                  767    769   *770
SKIP                 1317  *1320
SKOSP                235   *237
SLRPD                1041  *1052
SM3                  1222  *1226
SM4                  1217  *1220
SM6                  1205  *1208
SNOMD               *27
SOCH                 1031  *1033
SORTD                1029   1034   1036  *1038
SP                  *27
SPGN                 1051  *1053
SPM                  75     109    415    824    874   *884    1128   1473   1584
SPM2                 877   *883
SR24T                19    *1578
SRCH                 158    400   *529
SSUB                 711    720    729    738    753    762    771    780   *790
STACK               *27
START2               19    *1562
STAT                *27     37     39     43     46     47     48     60     62     64     67     68     103    110    175    233
                     235    239    247    269    297    423    446    827    859    860    865    877    915    978    980    984
                     985    1104   1137   1138   1164   1168   1468   1469   1579   1595
STAT2               *27     44     45     59     800    801    812    1198   1206   1218   1223   1241   1470   1507   1578
STAT3               *27     199    209    216    220    222    261    263    368    593    679    691
STAT4               *27
STAT5               *27
STAT6               *27
STAT7               *27     38     58     977    1227   1228   1229   1230
STMR                 1391  *1393
STRM                 1378  *1380
SUB1                *27     886    887
SUB2                *27     706    707    708    710    715    716    717    719    724    725    726    728    733    734    735
                     737    748    749    750    752    757    758    759    761    766    767    768    770    775    776    777
                     779    790    837    838    1209   1235   1237   1238
SUB3                *27     652    655    1116   1117
SUBADR              *27     660
SUBPG                979   *1137
TAC                  980   *998
TEN                  124   *126
TEST                *77     228    257    265
THI                  734    736   *737
THOU                 1027  *1030
TIME                 19    *977
TMP1                *27
TMP2                *27
TMR                 *27     830    999    1594
TN23                *1390   1397
TN32                *1377   1384
TONE                *27
TPAU2               *24     510    1481   1564   1569
TPSTP                1023  *1123   1139
TR5                  1236  *1238
TRA                 *702    786
TRAN1                144    299   *821    1069   1159   1166

TRAN2                56     810    819   *823    927
TRAN3               *827    875
TRFI                *756
TRFO                *747
TRNCH               *1337   1344
TRON                *714
TRSE                *774
TRSI                *765
TRTH                *732
TRTW                *723
TRYAG               *1478   1486
TRZE                *706
TVTX                 18    *37
TW1                  725    727   *728
TXT1                 174    301   *877    943    1103   1165
TXT1L                514   *878
TXT2                 21     73     248   *834    975    993    997    1592
TXT3                 508    907    1068   1109  *1113   1158   1567
TXT32                611    643    850    1015  *1114   1406   1531   1538
TXT38                143    298    512    925   *1107   1188
TXTOF               *64     1562
TXTOFF               37     60    *62
TXTON               *38
UCHOLD              *868    983
UOC                  1356  *1362
UP                   107    173   *185    290    351    863    870    930    1102   1126   1163   1502   1581
UPDATE               18    *58
```

Symbol cross-reference

```
V5          *648
W1          *27    654    700    703    791    835    884    1114
W2          *27    111    373    377    1024
W2B          602   *641   1289   1554
W3          *27    224    226    230    243    314    321    329    331    890    894    1477   1478   1540   1550   1555
             1556  1557
WACC        *27    337    347    494    529    530    532    543    544    548    558    560    1501
WROW        *27
YELLOW       17   *220
YIP         *183
ZE1          707    709   *710
```

AN460

An RDS Decoder using the MC68HC05E0

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INTRODUCTION

The Radio Data System (RDS) adds a digital data capability to the FM VHF transmissions on band II (87.5 to 108 MHz). This capability is in use in the UK and several other European countries, the intention being that most of western Europe will eventually adopt it. The specification is defined in EBU Technical Document 3244 (see reference 1).

To transmit the data, a sub carrier is added at 57 KHz. This sub carrier is amplitude modulated with a shaped bi-phase coded signal. The sub carrier itself is suppressed to avoid data modulated cross-talk in phase-locked loop stereo decoders and to maintain compatibility with the German ARI system which uses the same sub carrier frequency. Information is sent in groups of four 26-bit blocks. Each group of 104 bits is one of several types containing different information. It is up to the broadcaster which features are transmitted. The only constraints are that the specified format must be adhered to and that PI, PTY and TP should always be included. Each group contains a different sub-set of the RDS features; table1 lists all currently defined RDS features.

Table 1. RDS features

Feature	Information
PI	Program identification
PTY	Program type
PS	Program service name
RT	Radiotext
CT	Clock time and date
AF	Alternative frequencies
TA	Traffic announcement
TP	Traffic program
MS	Music/speech switch
DI	Decoder identification
PIN	Programme item number
EON	Enhanced other networks
TDC	Transparent data channel
INH	In-house data

The retrieval of data is carried out by a demodulator circuit which generates clock and data signals that can be used by a microprocessor. Suitable demodulators which can perform this function include SAA7579T, TDA7330, LA2231 and RDS hybrids. The block diagram of a typical application is shown in figure 1. The microprocessor, in this case an MC68HC05E0, decodes the RDS data using the clock and data signals from one of these demodulators and sends selected data to dot-matrix display modules.

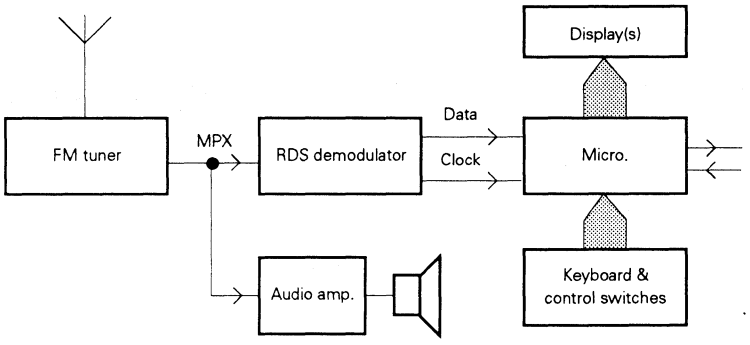

Figure 1. Typical application

This application incorporates an alarm clock which, if permanently powered, can be used to switch on the radio supplying the RDS data, at the required alarm time. There is a second alarm output intended to sound an alarm. This output is cancelled when any key is pressed, leaving the control output active. The control output could be used to switch the power supply of the radio or the audio stage. If an audio mute is used, RDS information can be updated even when the radio is "off". Alternatively the decoder can be used simply to display RDS data with its power being supplied from the radio and manually switched on and off.

RDS FEATURES

This application supports PI, PTY, PS, RT, CT, TP, TA, MS, DI, PIN and EON (see table 1). These features facilitate permanent display of the 8-digit station name (PS) and time (CT) and, on request, can display program type (PTY), radiotext data (RT) and the status of the other RDS features. EON data can be displayed, but the retuning features associated with AF and EON are not supported as there is no capability to control the tuned frequency. In a car radio EON data would be used to switch the radio to a station which is broadcasting local traffic information and AF data to tune the radio to the strongest signal carrying the selected service.

PI is a two byte number which identifies the country, coverage area and service. It can be used by the control microprocessor but is not normally intended for display. A change in PI code causes the initialisation of all RDS data as it indicates that the radio has been retuned. This application also facilitates the display of the current PI code.

PTY is a 5-bit number which indicates the current program type. At present 16 of these types are defined. Examples include "no programme type", "Current affairs" and "Pop music", although the actual syntax which is displayed is determined by the software of the controlling microprocessor. In this example PTY can be displayed on request. Table 2 shows the display used for each PTY code.

PS is the eight character name of the station and is permanently displayed (except in the standby mode).

RT is radiotext and constitutes a string of up to 64 characters which give additional information regarding the service or programme currently being transmitted. In this application, RT is displayed on request on the 16-digit dot-matrix displays using scrolling.

Table 2. PTY Types

PTY	Display
0	No program type
1	News
2	Current affairs
3	Information
4	Sport
5	Education
6	Drama
7	Culture
8	Science
9	Varied
10	Pop music
11	Rock music
12	Easy listening
13	Light classics
14	Serious classics
15	Other music
16-31	No program type

The data often contains extra spaces to centre the text on a 2x32 character display. As this is not suitable for a 16-character scrolling display the software reduces all sequences of two or more spaces to a single space.

CT data is transmitted every minute on the minute and provides a very accurate clock, traceable to national standards. The (Modified Julian) date and local time variation are also transmitted. Time is permanently displayed. In standby mode (see below) the date is displayed instead of the PS name. The MJD number, which is the form in which the date is received, can also be displayed. The microprocessor converts this number into day-of-week, day-of-month, month and year.

AF would be used by a car radio to retune to the strongest signal carrying the selected service. AF data, along with TDC and INH, is not used in this application.

TA and TP are flags. TP is set if the transmitter normally carries traffic information and TA is set if a traffic announcement is in progress. The combination, TA=1 and TP=0, is used to indicate that EON data is being used to supply information on other networks including traffic announcements. The status of these flags can be displayed and the combination, TA=TP=1, is brought out to a pin and can be used to control a LED or external hardware. An example of this could be to demute the radio or switch from cassette when a traffic announcement is taking place.

MS is a single bit indicating either music or speech and is intended to be used to make a tone or volume adjustment to a radio's audio stage. The MS bit is displayed on request.

Decoder information (DI) constitutes four bits indicating the type of transmission (mono, stereo, binaural, etc.). It is not currently in use in the UK but can be displayed as a number between 0 and 15.

Programme item number or PIN is used to identify the programme currently being broadcast. The format is a 2-byte number which includes the scheduled time and date (day-of-month) of the start of the programme. It can be displayed as four hexadecimal digits or fully decoded to day-of-month and time.

EON (Enhanced Other Networks) replaces the older ON format. If type 14 groups are used to provide EON data then type 3 groups (ON) will not be used (table 6 shows the currently defined group types). Type 14A groups are used to send information about other networks. The PS name and principal frequency of up to 11 other networks can be displayed. Type 14B groups are intended to be used to switch to traffic announcements in a radio in which the microprocessor can control the tuned frequency.

DECODING

Each 26-bit block contains 16 bits of data and 10 extra bits which are used for synchronisation and error detection. There are no gaps between blocks or groups, the synchronisation being done by looking for specific checkwords in the incoming data. In order to look for a checkword a stream of 26 consecutive data bits has to be multiplied by the fixed 10x26 matrix shown in figure 2.

The result of this multiplication is a 10-bit word which is compared with allowed values. There are 5 of these 10-bit "syndromes", one for each of the blocks 1, 2 and 4 and two for block 3 (see table 3). The alternative syndrome for block 3 is used in the B version of a group. In this version the PI code is sent in block 3, replacing what would be sent in the A version of the same group type. This is done to increase the frequency of sending the PI code so that it can be acquired more quickly.

```
10 0000 0000  ($02,$00)
01 0000 0000  ($01,$00)
00 1000 0000  ($00,$80)
00 0100 0000  ($00,$40)
00 0010 0000  ($00,$20)
00 0001 0000  ($00,$10)
00 0000 1000  ($00,$08)
00 0000 0100  ($00,$04)
00 0000 0010  ($00,$02)
00 0000 0001  ($00,$01)
10 1101 1100  ($02,$DC)
01 0110 1110  ($01,$6E)
00 1011 0111  ($00,$B7)
10 1000 0111  ($02,$87)
11 1001 1111  ($03,$9F)
11 0001 0011  ($03,$13)
11 0101 0101  ($03,$55)
11 0111 0110  ($03,$76)
01 1011 1011  ($01,$BB)
10 0000 0001  ($02,$01)
11 1101 1100  ($03,$DC)
01 1110 1110  ($01,$EE)
00 1111 0111  ($00,$F7)
10 1010 0111  ($02,$A7)
11 1000 1111  ($03,$8F)
11 0001 1011  ($03,$1B)
```

Figure 2. 10x26 decoding matrix

Table 3. Syndromes

Block	Syndrome	Binary	Hex
1	A	11 1101 1000	$03,$D8
2	B	11 1101 0100	$03,$D4
3	C	10 0101 1100	$02,$5C
	C'	11 1100 1100	$03,$CC
4	D	01 0101 1000	$01,$58

This syndrome test has to take place after each bit is received. The test inspects the last 26 bits received, until a valid syndrome is found. In this application, only syndrome A is accepted during the bit-by-bit syndrome check and the data is used only after four valid syndromes have been acquired. A more complex algorithm could allow all syndromes to be accepted during initial synchronisation and require less than four valid syndromes before the data is used. This can reduce the time taken to acquire the PI code, which is also included in block 3 of type B groups, but increases the likelihood that random data, giving a valid syndrome, will be used in error. The bit rate is 1187.5 Hz so the control microprocessor has a lot to do during this initial synchronisation. Once the first valid syndrome has been found, subsequent syndrome checks need be done only after the next 26 bits have been received, as this is when the next valid syndrome would be expected. If it is not found, then the bit-by-bit synchronisation check is re-started. Once consecutive A, B, C (or C') and D syndromes have been detected, a complete group has been acquired and the data can be used.

Four bits in block 2 determine the group type. Block 2 also contains TP and PTY data. The use of the other bits in blocks 2, 3 and 4 depends upon the group type while block 1 always contains the PI code. Table 7 shows the structures of the group types which are handled in this application.

CIRCUIT

Figure 3 shows the circuit diagram. As different demodulator devices can be used, the circuitry for the demodulator is not shown. The clock from the demodulator interrupts the microprocessor on each positive edge. At this time a data bit is available and is read on bit 2 of port B. Both an LCD and a VFD module are shown but normally only one will be used. If the LCD module is not connected, a pull-down resistor should be connected to bit 7 of port C, as the microprocessor uses this bit to check that the controller in the module is ready to receive a command. If this bit is left open circuit, it may cause the software to hang up. Alternatively the LCD drive software could be removed, allowing the use of port C for other purposes.

With more I/O available, additions to the software would allow access to the other control bits intended for controlling external hardware. These include the MS bit, DI data (4 bits) and PIN (match with current time and date). They could be brought out to port pins in a manner similar to that used for the TA=TP=1 signal. The unused port A and D pins could also be used for this purpose but in this application they were used during debug by the EOBUG monitor (reference 2). The application could make use of the port A and D pins, if debugging was done on a development system which did not have this limitation.

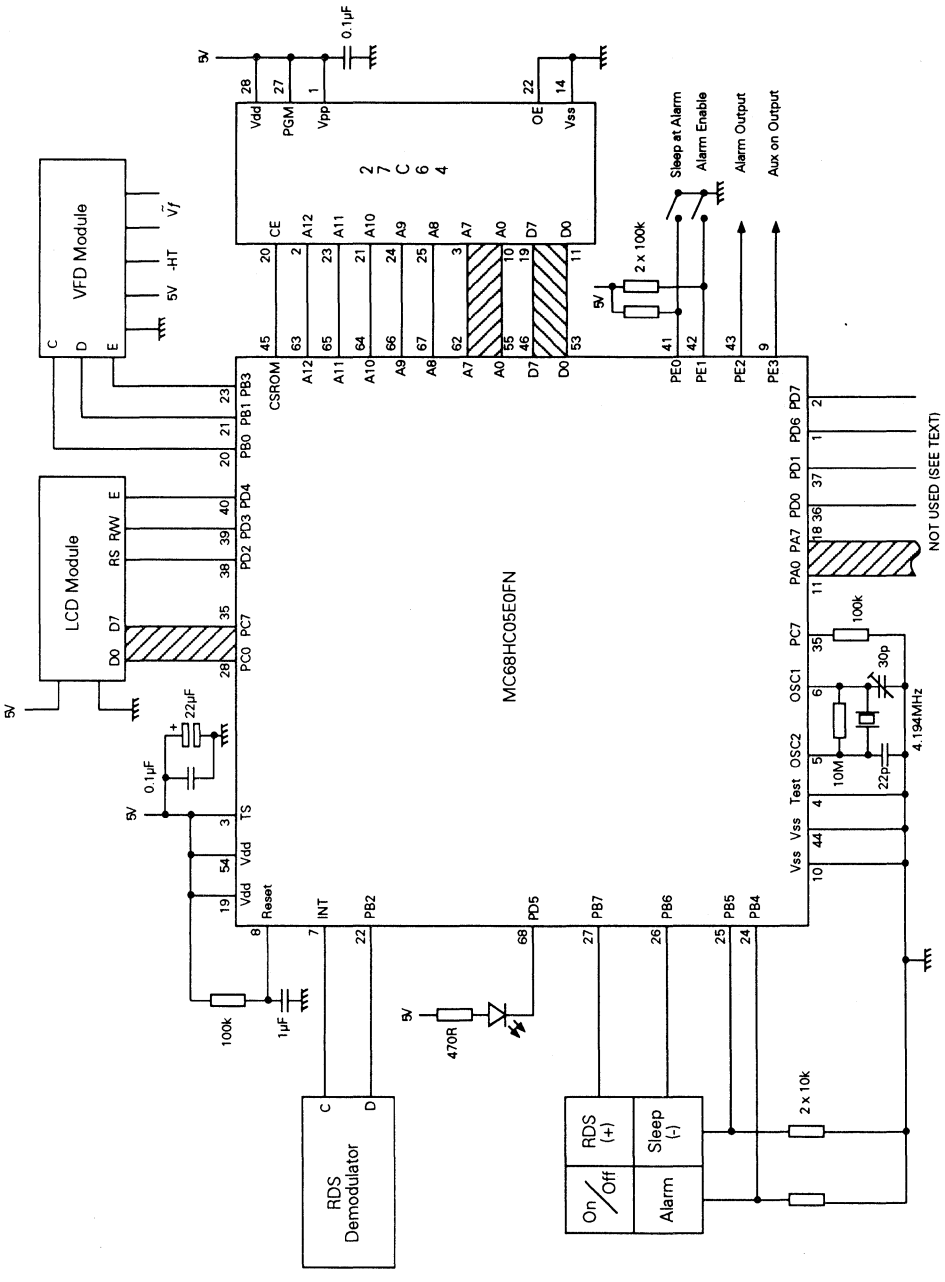

Figure 3. Circuit diagram

SOFTWARE

The complete software is listed. The reset routine (START) sets up the I/O ports including the enabling of some of the special functions available on port D. These signals (A15, A14, R/W and the P02 clock) were used during debug. The pins are not used in the final application. This also applies to all the port A pins which are configured as outputs. External interrupts are enabled on positive edges so that the RDS clock can interrupt the microprocessor when each data bit is available. Timer B runs as a real-time clock with interrupts every 125 ms. Correct operation of this clock in the absence of an RDS signal requires that a 4.194 MHz crystal be used (the trimmer on pin 6 should be adjusted for accurate timekeeping). Timer A's pre-scaler is set up to divide by 64; this causes the idle loop to cycle at 64Hz. The reset routine also initialises the LCD module (the display shows Mon 0 inv 00:00 until a valid group 4A is received), clears the RAM and calls a subroutine (INITD) to initialise the RAM locations used for displaying data.

Lines 114-118 and 193-208 are commented out as they are only relevant when de-bugging using the E0BUG monitor (reference 2).

The idle loop (IDLE) regularly checks the local keyboard for a keypress, compares the current time with the alarm time and performs other time-dependent functions related to the display modules and the sleep timer.

The keyboard software (KBD) scans the 4-key matrix for a keypress every 16ms. If the same key is held pressed for 3 successive scans, it acts on this key function by calling the relevant subroutine (ALARM, ONOFF, SLEEP or RDS). This software also controls the repeat rate of the SLEEP and RDS keys. This rate is set at 6Hz (after an initial 750ms delay) when the keys are used to change the alarm time and 1Hz for their normal function. The other keys do not repeat if held down. Table 4 shows the functions available in each mode.

Table 4. Key functions

<table>
<tr><th rowspan="2">MODE</th><th colspan="4">KEY</th></tr>
<tr><th>On/Off</th><th>Sleep</th><th>Alarm</th><th>RDS</th></tr>
<tr><td>Standby (Off)</td><td>mode normal (On)</td><td rowspan="4">mode sleep (On)</td><td rowspan="2">mode alarm</td><td>—</td></tr>
<tr><td>Normal (On)</td><td rowspan="2">mode stndby (Off)</td><td rowspan="4">RT
PTY
PI
TA/TP
PIN(h)
PIN(d)
MJD
MS/DI
EON 1
:
:
EON 11</td></tr>
<tr><td>Alarm OFF</td><td>mode alarm ON</td></tr>
<tr><td>Alarm ON</td><td>mode alarm set-up</td><td rowspan="2">mode alarm OFF</td></tr>
<tr><td>Alarm SET UP</td><td>toggle hr/min</td><td>dec. hr/min</td><td>inc. hr/min</td></tr>
</table>

The On/Off key uses the subroutine ONOFF to toggle between ON and standby. A port pin (3,PORTE) can be used to control the power to the VHF radio and/or other external hardware. In standby mode, with the alarm disabled, the time and date are displayed. If the alarm is enabled, the alarm time is displayed. In the ON mode the time is displayed along with the current RDS PS-name. Table 5 shows these display formats.

Table 5. Display formats

Display mode		Format
Standby (Off)	Alarm off	Thu 30 Apr 18:05
	Alarm off, no CT	Mon 0 inv 0:00
	Alarm on	0659 ALARM 18:05
Normal (On)	With RDS PS name	BBC R4 18:05
	Without RDS	-------- 18:05
Alarm	Alarm off	Alarm - OFF
	Alarm on	Alarm - 6:59
Sleep		Sleep 60 min.
RDS	RT	BBC Radio 4 ....
	PTY	News
	PI	PI code - C204
	TA & TP	TP - 0 TA - 1
	PIN(hex)	PIN no. - F480
	PIN(decod)	30th at 18:00
	MJD	MJ day - 48742
	MS & DI	M/S M DI 15
	EON 1	BBC R3 92.10
	2	BBC R.Sc 103.60
	3	BBC Nwcl 96.00
	4	BBC Scot 94.30
	5	BBC Mtme 92.50
	6	BBC Twed 93.50
	7	BBC R5 909kHz
	8	BBC Eng. 100.00
	9	BBC R1 99.50
	10	BBC R2 89.90
	11	--------

The Alarm key calls the subroutine ALARM which displays the current alarm status. A second press changes the alarm armed status. When the alarm is armed, the alarm time is displayed. In this mode the On/Off key can be used to select either hours or minutes (indicated by flashing) and the Sleep and RDS keys used to increment and decrement the settings. If the alarm has triggered then the first press of any key cancels it. The alarm display has one of the two alarm formats shown in table 5 according to whether or not the alarm is armed. As all the keys have a special function in the alarm mode the only way to exit this mode is to wait for a timeout. If no keys are pressed for 5 seconds, the mode returns to normal.

The Sleep key controls the sleep timer. If the decoder is in the standby mode the first press of Sleep switches it on and initialises the sleep time to 60 minutes. When the sleep timer is running, this is indicated by a flashing decimal point in the right-most character of the display modules. Subsequent presses of the Sleep key decrement the time remaining by 5 minutes. When the sleep time has elapsed, the decoder returns to standby. In the alarm set-up mode this key decrements the alarm time.

The RDS key uses subroutine RDS to step through the various RDS data which can be displayed. Holding down this key steps through the displays at 1Hz. The displays are RT (scrolling), PTY, PI, TA/TP, PIN (hex), PIN (decoded), MJD, MS/DI and EON (11 networks) as shown in table 5. In the alarm set-up mode this key increments the alarm time.

The timer interrupt routine (TINTB) updates the RT scrolling pointers (DISP1 and DISP2). These pointers are incremented regularly whether or not an RT display is active. In this way, the software can be easily converted to using a 2-line LCD module in which the top line is the normal display of PS-name and time and the lower line a permanent display of scrolling RT. The timer interrupt also decrements the sleep timer and updates the RAM locations used to store hours, minutes, seconds and eighth-seconds. All RDS data (except date and time) is cleared by this routine if no valid RDS data is detected for a period of 10 seconds.

SYNDROME AND CONFIDENCE

Hardware interrupts are vectored to jump to SDATA where serial data is received from the RDS demodulator. The clock edge causes an interrupt and the first instruction reads the data into the carry bit of the condition code register. The bit is shifted into a 4-byte RAM register and the matrix multiplication performed. The state of flag 0,STAT2, determines if the multiplication is to take place after every bit or only after all 26 bits have arrived. The multiplication is performed using two EOR instructions for every bit (two are required as the 10-bit syndrome requires two bytes). As the top of the matrix (see figure 2) is the unity matrix, the first 10 bits are transferred directly into the syndrome RAM locations (SYN). This, the omission of any EOR #$00 instructions, the reordering of the bits and the use of the index register for temporary storage help to reduce the length of inline code in this routine. The routine could be shortened by using a loop but this would incur an unacceptable penalty in execution time. Microprocessors with two accumulators would find this task a lot simpler and quicker but an MC68HC05E0, at half its maximum speed, can easily perform the calculation in the required time.

After the multiplication has been performed the resultant 10-bit number is compared with the allowed syndromes (see table 3). The variable LEV records the current block level. It is initially zero but incremented each time a valid syndrome is found. When it is zero only syndrome A is accepted, if this is found then syndrome B is expected 26 bits later so when LEV is one only syndrome B is accepted. If an invalid syndrome is found LEV is cleared, the syndrome confidence level CONF is decremented and the interrupt ended.

When a valid syndrome is found, CONF in increased by 4 and the 16 data bits saved in the relevant bytes of TMPGRP. If the valid syndrome is type D then a complete group has been received and all 8 bytes are transferred to the 8 RAM locations at GROUP. This double buffer means that the data in GROUP can be used while interrupts are overwriting TMPGRP with new data.

The confidence level CONF is used to decide what should be done if the data becomes unreliable due to a poor RF input to the receiver. When the first valid syndrome is found it is initialised to 42. Subsequent valid syndromes increment it by four and invalid ones decrement it by 1. If CONF falls below 41, then it is assumed that synchronisation has been lost and a bit-by-bit re-synchronisation is carried out. If it falls below 10, the signal is deemed unacceptable and the displays are re-initialised. The confidence level is not incremented by the detection of a valid syndrome if it is higher than 56.

GROUPS HANDLED

If a complete group has been received the data can be processed. The buffering used would allow this to be done outside the interrupt but in this case there is sufficient time to do it within the interrupt. The PI code is checked to see if it has changed. If it has changed the displays are initialised. In an application using the AF capability of RDS, more use would be made of the PI code.

Next PTY and TP are updated and the group type identified. Group types 0A, 0B, 1A, 1B, 2A, 4A, 14A and 15B are handled. Table 6 shows the type of information contained in each group and table 7 shows the detailed structure of the groups actually used.

Table 6. RDS Groups

Group	Features
All	PI, PTY, TP
0	TA, DI, MS, PS, AF
1	PIN
2	RT
3	ON (replaced by EON)
4A	CT
5	TDC
6	INH
14	EON
15B	TA, DI, MS

Group 0 & 15B

As AF data is not handled, there is no difference in the treatment of groups 0A and 0B. PS data is extracted and placed in RAM according to the address bits in block 2 (see table 7). TA, DI and MS data are then read, DI is sent a single bit at a time and uses the same address bits as the PS name to determine which of the four bits is being updated. Groups of type 15B also contains all this switching information. They are used to increase the repetition rate of this data but contain no PS or AF information.

Group 1

Group types 1A and 1B contain the same data except for the repetition of the PI code in type 1B. The PIN data is recovered and saved in RAM. This is intended for future use to control external hardware, for example a tape recorder. This would facilitate the unattended recording of a pre-selected program. At present this application simply allows the display of PIN data both in its raw hexadecimal form and fully decoded to day-of-month and time. Full use of PIN data would require continuously comparing the PIN day-of-month and time with the current day-of-month and time enabling an I/O pin to be switched when there is a match.

Group 2A

RT data from blocks 3 and 4 is written to RAM according to the address included in block 2. There are four address bits and four ASCII encoded bytes giving the possibility of 64 characters. If the Text A/B flag changes state, the RT area in RAM is cleared, indicating that the message has changed. Group 2B is not handled as it is rarely, if ever, used.

Group 4A

Two of the more complex tasks to be performed are required by the CT calculations for group 4A. These are for the local time difference and the conversion of the MJD number into a recognisable date.

The broadcast time is Universal Coordinated Time (UTC), effectively the same as GMT. Time differences from UTC, including summer (daylight saving) time, are sent as an offset of up to +/- 12 hours in half-hour increments.

The software includes 4-function, 9-digit integral BCD arithmetic which is used to decode the date from the MJD number using the formulae:

```
Y'      =  int[(MJD-15078.2)/365.25]
M'      =  int[(MJD-14956.1-int(Y'x365.25))/30.6001]
Day     =  MJD-14956-int(Y'x365.25)-int(M'x30.6001)
If M'=14 or M'=15,
        then K=1;
        else K=0
Year    =  Y'+K
Month   =  M'-1-12K
```

Group 14A

This group contains EON data. A large amount of information can be sent using this group, and it can take up to two minutes for all the data to arrive after the radio has been retuned. This application saves the PI code, PS name and principal frequency of up to 11 networks although more networks, each with many frequencies, and other data (e.g. PTY(ON), PIN(ON), TA(ON) etc.) may be sent. Table 5 shows the format of the EON display. All the information shown is real data from the Black Hill transmitter in central Scotland.

Displays

The software drives both a parallel LCD module (based on an HD44780 driver with or without an HD44100) and a serial VFD module (based on an MSC7128 driver) to give a choice of display types. The displays show the same data (within the limitations of their character ROMs).

The display routine (MOD) is executed in the idle loop if flag 3,STAT2 is set. It is set every 125ms by timer B interrupts. If flag 4,STAT2 is set, the display is initialised, indicating no valid RDS data. The LCD module is then updated with new data. Each time anything is written to the module, the subroutine WAIT is used before the write is executed; this checks that the controller in the module is not busy. This is indicated by a low on bit 7, so bit 7 on port C should have a pull-down resistor to satisfy this condition if an LCD module is not being used.

Table 7.

	Block 1		Block 2		Block 3		Block 4	
Group 0 and 15B	PI code	chck A	bit(s) use 15–12 : group no. 11 : group type 10 : TP flag 9–5 : PTY code 4 : TA flag 3 : M/S bit 2 : DI bit 1–0 : PS/DI address	chck B	AF (PI code in type 0B and 15B)	chck C or C'	PS name (as block 2 for 15B)	chck D
Group 1	PI code	chck A	15–12 : 0001 11 : group type 10 : TP flag 9–5 : PTY code 4–0 : not used	chck B	not used (PI code in type 1B)	chck C or C'	PIN data 15–11 : day-of-month 10–6 : hour 5–0 : minute	chck D
Group 2A	PI code	chck A	15–12 : 0010 11 : 0 10 : TP flag 9–5 : PTY code 4 : text A/B flag 3–0 : text address	chck B	RT 2 ASCII characters	chck C	RT 2 ASCII characters	chck D
Group 4A	PI code	chck A	15–12 : 0100 11 : 0 10 : TP flag 9–5 : PTY code 4–2 : not used 1–0 : MJD (16–15)	chck B	CT 15–1 : MJD (14–0) 0 : hour (4)	chck C	CT 15–12 : hour (3–0) 11–6 : minute (5–0) 5 : offset sense 4–0 : offset (4–0)	chck D
Group 14A	PI code	chck A	15–12 : 1110 11 : 0 10 : TP flag 9–5 : PTY code 4 : TP (On) flag 3–0 : usage code	chck B	EON information code: 0–3 : PS 4 : AF 5–9 : AF (map) 10–11 : not used 12–15 : not imp.	chck C	PI (On)	chck D

The listing is shown for use with a divide by 8 multiplexing LCD module. This module will normally contain an HD44780 and an HD44100.

If a divide by 16 module (HD44780 only) is to be used then line 1294 should be replaced by line 1293 and line 1371 commented out to include the execution of the code on lines 1379 to 1392.

The different display formats are selected by checking the various flags and the relevant routine executed. The normal display permanently shows PS name and time. As the locations in RAM used for hours and minutes contain binary numbers they are converted to BCD before being written to the relevant bytes in DISP. Once all 16 bytes in DISP have been loaded, a loop is used to send the data to the LCD module.

The VFD routine sends the same data as is shown on the LCD module to the serial VFD module. The display driver used has a different character set from the standard ASCII set used by the LCD module. The table VTAB is used to convert ASCII data into the required character in the VFD module. The small table INITF is used to send the required initialisation bytes to the VFD module. This module does not require a busy check but does require a delay between successive bytes. This is satisfied by the wait loop within the serial output loop VFDF.

Alarm functions

The alarm time can be entered as described above. If the alarm is enabled (alarm time displayed on first press of the ALARM key, and permanently displayed in standby mode) then, at the alarm time, the auxiliary control line will go high. This can be used to control external hardware, for example to switch on the VHF radio supplying the RDS data. If the auxiliary line is already high (decoder fully on or on via the sleep timer), then it simply stays high. The operation of the sleep timer is not affected if bit 0 of port E is high. If this I/O line is low at the alarm time, then the sleep timer is activated for an hour. This takes place whether the decoder was previously on, off, or running the sleep timer, and has the effect of switching the auxiliary line low an hour after the alarm time, regardless of its condition prior to the alarm.

At the alarm time the alarm output will also be activated (active low) as long as it is enabled by bit 1 of port E being held low. This is intended to drive an alarm sounder. When this output is active, a press of any key cancels it until the next alarm. This cancellation does not affect the auxiliary output.

REFERENCES

1 EBU Technical Document 3244, Specifications of the Radio Data System RDS for VHF/FM Sound Broadcasting.

2 AN459, A Monitor for the MC68HC05E0.

APPENDIX (listing) follows

```
0001                    ********************************************
0002                    *                                          *
0003                    *              HC05E0 RDS Decoder.         *
0004                    *                                          *
0005                    *    P. Topping          29th February '92 *
0006                    *                                          *
0007                    ********************************************
0008
0009 0000               PORTA   EQU     $00             PORT A ADDRESS
0010 0001               PORTB   EQU     $01               "  B    "
0011 0002               PORTC   EQU     $02               "  C    "
0012 0003               PORTD   EQU     $03               "  D    "
0013 0004               PORTE   EQU     $04               "  E    "
0014 0005               PORTAD  EQU     $05             PORT A DATA DIRECTION REG.
0015 0006               PORTBD  EQU     $06               "  B    "       "       "
0016 0007               PORTCD  EQU     $07               "  C    "       "       "
0017 0008               PORTDD  EQU     $08               "  D    "       "       "
0018 0009               PORTED  EQU     $09               "  E    "       "       "
0019 000a               TAP     EQU     $0A             TIMER A PRE-SCALLER
0020 000b               TBS     EQU     $0B             TIMER B SCALLER
0021 000c               TCR     EQU     $0C             TIMER CONTROL REGISTER
0022 000e               ICR     EQU     $0E             INTERRUPT CONTROL REGISTER
0023 0012               PORTDSF EQU     $12             PORTD SPECIAL FUNCTIONS
0024
0025 0009               ND      EQU     9               No. BCD DIGITS
0026
0027 0030                       ORG     $0030
0028
0029 0030               Q       RMB     9               BCD WORKING NUMBERS
0030 0039               TMQ     RMB     9               SCRATCH
0031 0042               P       RMB     9               WORKING NUMBER 2
0032 004b               TMP     RMB     9               MULT. OVER. OR DIV. REMAINDER
0033 0054               R       RMB     9               WORKING NUMBER 3
0034 005d               MJD     RMB     9               MODIFIED JULIAN DAY NUMBER
0035 0066               YR      RMB     9               YEAR
0036 006f               MNTH    RMB     2               MONTH
0037 0071               DOM     RMB     2               DATE
0038 0073               DOW     RMB     1               DAY OF WEEK
0039 0074               BMJD    RMB     3               BINARY MJD
0040 0077               DIST    RMB     1               DISPLAY TRANSIENT TIMEOUT COUNTER
0041 0078               SLEPT   RMB     1               SLEEP TIMER MINUTES COUNTER
0042 0079               RDSTO   RMB     1               RDS TIMEOUT COUNTER
0043 007a               DAT     RMB     4               SERIAL DATA BUFFER
0044 007e               TMPGRP  RMB     8               TEMPORARY GROUP DATA
0045 0086               GROUP   RMB     8               COMPLETE GROUP DATA
0046 008e               PTY     RMB     1               PROGRAM-TYPE CODE (CURRENT)
0047 008f               PI      RMB     2               PROGRAM IDENTIFICATION CODE
0048 0091               PIN     RMB     2               PROGRAM ITEM NUMBER
0049 0093               LEV     RMB     1               VALID BLOCK LEVEL
0050 0094               BIT     RMB     1               BIT LEVEL
0051 0095               ITMP1   RMB     1               TEMP BYTE FOR USE IN IRQ
0052 0096               SYN     RMB     2               SYNDROME
0053 0098               CONF    RMB     1               SYNDROME CONFIDENCE
0054 0099               TH8     RMB     1               TICS (EIGHTHS OF SECONDS)
0055 009a               SEC     RMB     1               SECONDS
0056 009b               MIN     RMB     1               MINUTES
0057 009c               OUR     RMB     1               HOURS
0058 009d               AMIN    RMB     1               ALARM MINUTES
0059 009e               AOUR    RMB     1               ALARM HOURS
0060 009f               DISP1   RMB     1               RT DISPLAY POINTER #1
0061 00a0               DISP2   RMB     1               RT DISPLAY POINTER #2
0062 00a1               W1      RMB     1               W
0063 00a2               W2      RMB     1               O
0064 00a3               W3      RMB     1               R
0065 00a4               W4      RMB     1               K
0066 00a5               W5      RMB     1               I
0067 00a6               W6      RMB     1               N
0068 00a7               W7      RMB     1               G
0069 00a8               W8      RMB     1
0070 00a9               KEY     RMB     1               CODE OF PRESSED KEY
0071 00aa               KCOUNT  RMB     1               KEYBOARD COUNTER
0072 00ab               CARRY   RMB     1               BCD CARRY
0073 00ac               COUNT   RMB     1               LOOP COUNTER
0074 00ad               NUM1    RMB     1               1ST NO. POINTER (ADD & SUBTRACT)
0075 00ae               NUM2    RMB     1               2ND NO. POINTER (ADD & SUBTRACT)
0076 00af               RTDIS   RMB     1               RDS DISPLAY TYPE
0077 00b0               DI      RMB     1               DECODER IDENTIFICATION
0078 00b1               DISP    RMB     16              LCD MODULE BUFFER
0079 00c1               PSN     RMB     8               PS NAME
0080
0081 00c9               STAT2   RMB     1               0: VALID SYNDROME
0082                    *                               1: VALID GROUP
0083                    *                               2: RT DISPLAY
0084                    *                               3: UPDATE DISPLAY
0085                    *                               4: CLEAR DISPLAY
0086                    *                               5: SPACE FLAG
0087 00ca               STAT3   RMB     1               0: M/S. 0: M. 1: S
0088                    *                               1: TEXTA/TEXTB BIT (RT)
0089                    *                               2: TA FLAG
0090                    *                               3: TP FLAG
0091                    *                               4: KEY REPEATING
0092                    *                               5: KEY FUNCTION PERFORMED
0093                    *                               6: UPDATE DATE
0094 00cb               STAT4   RMB     1               0: DISPLAY TRANSIENT
0095                    *                               1: SLEEP TIMER RUNNING
0096                    *                               2: SLEEP DISPLAY
0097                    *                               3: ALARM DISPLAY
0098                    *                               4: ALARM ARMED
0099                    *                               5: ALARM SET-UP
0100                    *                               6: ALARM HOURS (SET-UP)
0101                    *                               7: RDS DISPLAYS
0102
0103 00cc                       RMB     35              not used
0104 00ed               STACK   RMB     18              19 BYTES USED (1 INTERRUPT
0105 00ff               SP      RMB     1               AND 7 NESTED SUBROUTINES)
0106
0107 0100                       ORG     $0100
0108
0109 0100               RT      RMB     69              RADIOTEXT
0110 0145               EON     RMB     176             EON DATA (MAX: 11 NETWORKS)
```

```
0112 e000                              ORG     $E000
0113
0114                           *STRST   JMP     START           RESET VECTOR                ($0400 DURING DE-BUG)
0115                           *IRQ     JMP     SDATA           IRQ                         ($0403 DURING DE-BUG)
0116                           *TIMERA  JMP     START           TIMER A INTERRUPT (NOT USED, $0406 DURING DE-BUG)
0117                           *TIMERB  JMP     TINTR           TIMER B INTERRUPT           ($0409 DURING DE-BUG)
0118                           *SERINT  JMP     START           SERIAL INTERRUPT  (NOT USED, $040C DURING DE-BUG)
0119
0120                           ************************************************
0121                           *                                              *
0122                           *       Reset routine - setup ports.           *
0123                           *                                              *
0124                           ************************************************
0125
0126 e000 a6 c3                START   LDA     #$C3            ENABLE PORTD SPECIAL FUNCTIONS
0127 e002 b7 12                        STA     PORTDSF         P02, R/W, A14 & A15 (0,1,6,7)
0128 e004 a6 45                        LDA     #$45            ENABLE POSITIVE EDGE/LEVEL
0129 e006 b7 0e                        STA     ICR             INTERRUPTS
0130 e008 a6 01                        LDA     #1              TIMER B SCALER: /2
0131 e00a b7 0b                        STA     TBS             125 mS INTERRUPTS (4.194 MHz XTAL)
0132 e00c a6 3f                        LDA     #63             TIMER A PRE-SCALER: /64
0133 e00e b7 0a                        STA     TAP             64Hz IDLE LOOP
0134
0135 e010 3f 00                        CLR     PORTA
0136 e012 a6 ff                        LDA     #$FF            E0BUG DISPLAY/KEYBOARD I/O
0137 e014 b7 05                        STA     PORTAD          NOT USED IN RDS APPLICATION
0138 e016 3f 01                        CLR     PORTB           0, 1: SERIAL CLOCK AND DATA
0139 e018 a6 cb                        LDA     #$CB            2: RDS DATA IN, 3: VFD SELECT
0140 e01a b7 06                        STA     PORTBD          4, 5: KEYBOARD IN, 6, 7: KEYBOARD OUT
0141 e01c 3f 02                        CLR     PORTC
0142 e01e a6 ff                        LDA     #$FF            ALL OUT, LCD DATA BUS
0143 e020 b7 07                        STA     PORTCD
0144 e022 a6 3c                        LDA     #$3C            BITS 2, 3 & 4 OUT, LCD
0145 e024 3f 03                        CLR     PORTD           2: RS, 3: R/W, 4: CLOCK, 5: LED (TA=TP=1)
0146 e026 b7 08                        STA     PORTDD          0, 1, 6 & 7 USED DURING DE-BUG
0147 e028 a6 0c                        LDA     #$0C            BIT0: INPUT, ENABLE SLEEP TIMER AT ALARM TIME
0148 e02a b7 04                        STA     PORTE           BIT1: INPUT, ENABLE ALARM OUTPUT
0149                           *       LDA     #$00            BIT2: ALARM OUTPUT (ACTIVE LOW)
0150 e02c b7 09                        STA     PORTED          BIT3: RADIO ON OUTPUT (ACTIVE HIGH)
0151
0152                           ************************************************
0153                           *                                              *
0154                           *       Initialise LCD.                        *
0155                           *                                              *
0156                           ************************************************
0157
0158 e02e a6 30                        LDA     #$30
0159 e030 cd eb 65                     JSR     CLOCK           INITIALISE LCD
0160 e033 cd eb e6                     JSR     CLRDIN          CLEAR BUS DATA
0161 e036 cd eb e6                     JSR     CLRDIN
0162 e039 cd eb e6                     JSR     CLRDIN          4 TIMES TO PROVIDE A 1mS DELAY
0163 e03c cd eb e6                     JSR     CLRDIN          FOR LCD MODULE INITIALISATION
0164 e03f a6 30                        LDA     #$30
0165 e041 cd eb 65                     JSR     CLOCK           INITIALISE LCD
0166
0167 e044 ae 30                        LDX     #6              INITIALISE RAM
0168 e046 7f                   CLOOP   CLR     0,X
0169 e047 5c                           INCX                    PROVIDES A 1mS DELAY FOR LCD
0170 e048 a3 ed                        CPX     #STACK
0171 e04a 26 fa                        BNE     CLOOP
0172
0173 e04c a6 30                        LDA     #$30
0174 e04e cd eb 65                     JSR     CLOCK           INITIALISE LCD
0175
0176 e051 cd eb 6c                     JSR     WAIT
0177 e054 a6 30                        LDA     #$30            1-LINE DISPLAY
0178 e056 cd eb 65                     JSR     CLOCK           LATCH IT
0179 e059 cd eb 6c                     JSR     WAIT
0180 e05c a6 08                        LDA     #$08            SWITCH DISPLAY OFF
0181 e05e cd eb 65                     JSR     CLOCK           LATCH IT
0182 e061 cd eb 6c                     JSR     WAIT
0183 e064 a6 01                        LDA     #$01            CLEAR DISPLAY
0184 e066 cd eb 65                     JSR     CLOCK           LATCH IT
0185 e069 cd eb aa                     JSR     INITD
0186
0187                           ************************************************
0188                           *                                              *
0189                           *       Vectors for de-bug using E0BUG monitor.*
0190                           *                                              *
0191                           ************************************************
0192
0193                           *       LDA     #$0C            ENABLE EXTERNAL RAM WRITE
0194                           *       STA     TCR
0195
0196                           *       LDA     #$04            VECTORS FOR E0 MONITOR
0197                           *       STA     $0201
0198                           *       STA     $0204           USING JUMP TABLE AT $0400
0199                           *       STA     $0207
0200                           *       STA     $020A           (LINES 126-130)
0201                           *       LDA     #$03
0202                           *       STA     $0202           IRQ ($0403)
0203                           *       LDA     #$06
0204                           *       STA     $0205           TIMER A ($0406)
0205                           *       LDA     #$09
0206                           *       STA     $0208           TIMER B ($0409)
0207                           *       LDA     #$0C
0208                           *       STA     $020B           SERIAL ($040C)
0209
0210                           ************************************************
0211                           *                                              *
0212                           *       Enable interrupts                      *
0213                           *                                              *
0214                           ************************************************
0215
0216 e06c a6 0b                        LDA     #$0B            EDGE SENSITIVE IRQ, TIMERS A & B ENABLED
0217 e06e b7 0c                        STA     TCR             SUB-SYS CLK = 262144 Hz  (4.194 MHz XTAL)
0218                           *                               DISABLE EXTERNAL RAM WRITE
0219 e070 9a                           CLI
```

```
0221                    ***************************************************
0222                    *                                                 *
0223                    *       Idle loop.                                *
0224                    *                                                 *
0225                    ***************************************************
0226
0227 e071 09 0e fd      IDLE    BRCLR   4,ICR,*        64 Hz
0228 e074 19 0e         BCLR    4,ICR
0229
0230 e076 01 cb 07      NO2D    BRCLR   0,STAT4,NOPS    DISPLAY TRANSIENT ?
0231 e079 b6 77                 LDA     DIST
0232 e07b 26 03                 BNE     NOPS            YES, TIMED OUT ?
0233 e07d cd e8 0a              JSR     CLTR            YES, CLEAR TRANSIENT DISPLAYS
0234
0235 e080 07 c9 05      NOPS    BRCLR   3,STAT2,SCAN    DISPLAY UPDATE REQUIRED ?
0236 e083 cd e6 b6              JSR     MOD             YES, DO IT
0237 e086 17 c9                 BCLR    3,STAT2         AND CLEAR FLAG
0238
0239 e088 09 cb 1d      SCAN    BRCLR   4,STAT4,CHSLP   ALARM ARMED ?
0240 e08b b6 9e                 LDA     AOUR            YES, COMPARE ALARM HOURS
0241 e08d b1 9c                 CMP     OUR             WITH TIME
0242 e08f 26 17                 BNE     CHSLP           SAME ?
0243 e091 b6 9d                 LDA     AMIN            YES, COMPARE ALARM MINUTES
0244 e093 b1 9b                 CMP     MIN             WITH TIME
0245 e095 26 11                 BNE     CHSLP           SAME ?
0246 e097 b6 9a                 LDA     SEC             ONLY ALLOW WAKE-UP IN FIRST SECOND
0247 e099 26 0d                 BNE     CHSLP           TO PREVENT SWITCH-OFF LOCKOUT
0248 e09b 16 04                 BSET    3,PORTE         YES, SWITCH ON
0249
0250 e09d 02 04 02              BRSET   1,PORTE,FULON2  ALARM ENABLED (SWITCH) ?
0251 e0a0 15 04                 BCLR    2,PORTE         YES, SOUND ALARM
0252 e0a2 00 04 03      FULON2  BRSET   0,PORTE,CHSLP   SLEEP TIMER AT ALARM TIME ?
0253 e0a5 cd e2 09              JSR     INSLP           YES, START SLEEP TIMER
0254
0255 e0a8 03 cb 08      CHSLP   BRCLR   1,STAT4,FLN     SLEEP TIMER RUNNING ?
0256 e0ab b6 78                 LDA     SLEPT           YES
0257 e0ad 26 04                 BNE     FLN             TIME TO FINISH ?
0258 e0af 13 cb                 BCLR    1,STAT4         YES, CLEAR FLAG
0259 e0b1 17 04                 BCLR    3,PORTE         AND SWITCH OFF
0260
0261 e0b3 cd e1 11      FLN     JSR     KEY             READ KEYBOARD
0262 e0b6 cd e1 6f              JSR     KEYP            EXECUTE KEY
0263
0264 e0b9 b6 ca                 LDA     STAT3
0265 e0bb a4 0c                 AND     #$0C
0266 e0bd a1 0c                 CMP     #$0C            TA AND TP BOTH HIGH ?
0267 e0bf 27 07                 BEQ     TATP
0268 e0c1 0a 03 09              BRSET   5,PORTD,IOOK    NO, I/O LINE ALREADY HIGH ?
0269 e0c4 1a 03                 BSET    5,PORTD         NO, MAKE IT HIGH
0270 e0c6 20 05                 BRA     IOOK
0271 e0c8 0b 03 02      TATP    BRCLR   5,PORTD,IOOK    TA=TP=1, I/O LINE ALREADY LOW ?
0272 e0cb 1b 03                 BCLR    5,PORTD         NO, MAKE IT LOW
0273
0274 e0cd 0d ca 02      IOOK    BRCLR   6,STAT3,IDLEJ   UPDATE DATE ?
0275 e0d0 ad 02                 BSR     MJDAT           YES, CONVERT FROM MJD
0276 e0d2 20 9d         IDLEJ   BRA     IDLE
0277
0278                    ***************************************************
0279                    *                                                 *
0280                    *       Extract MJD and convert to decimal.       *
0281                    *                                                 *
0282                    ***************************************************
0283
0284 e0d4 b6 76         MJDAT   LDA     BMJD+2
0285 e0d6 b7 68                 STA     YR+2
0286 e0d8 b6 75                 LDA     BMJD+1
0287 e0da b7 67                 STA     YR+1
0288 e0dc b6 74                 LDA     BMJD
0289 e0de b7 66                 STA     YR
0290 e0e0 ae 5d                 LDX     #R              CLEAR
0291 e0e2 bf ad                 STX     NUM1
0292 e0e4 cd ef 86              JSR     CLRAS           R
0293 e0e7 3c 5c                 INC     R+NT+1          R = 1
0294 e0e9 ae 5d                 LDX     #MJD
0295 e0eb cd ef 86              JSR     CLRAS           CLEAR MJD
0296 e0ee a6 11                 LDA     #17             17 BITS TO CONVERT
0297 e0f0 b7 a6                 STA     W6
0298 e0f2 34 66         LOOPJ   LSR     YR              MOVE OUT
0299 e0f4 36 67                 ROR     YR+1
0300 e0f6 36 68                 ROR     YR+2            FIRST (LS) BIT
0301 e0f8 24 07                 BCC     NXTJ            ZERO ?
0302 e0fa ae 5d                 LDX     #MJD            ONE, ADD
0303 e0fc bf ae                 STX     NUM2            CURRENT VALUE
0304 e0fe cd ee 33              JSR     ADD             OF R
0305 e101 ae 54         NXTJ    LDX     #R              ADD R
0306 e103 bf ae                 STX     NUM2            TO
0307 e105 cd ee 33              JSR     ADD             ITSELF
0308 e108 3a a6                 DEC     W6              ALL
0309 e10a 26 e6                 BNE     LOOPJ           DONE ?
0310 e10c 1d ca                 BCLR    6,STAT3         MJD UPDATED
0311 e10e cc ef 95              JMP     MJDC            CONVERT MJD TO DAY, DATE, MONTH & YEAR
```

```
0313                    ************************************************
0314                    *                                              *
0315                    *       Keyboard routine.                      *
0316                    *                                              *
0317                    ************************************************
0318
0319 e111 a6 20         KBD     LDA     #$20
0320 e113 ae 02                 LDX     #2
0321 e115 48            KEY1    LSLA                    SELECT ROW
0322 e116 a4 c0                 AND     #$C0            BITS 6 & 7 ONLY
0323 e118 aa 08                 ORA     #$08            VFD ENABLE HIGH
0324 e11a b7 01                 STA     PORTB
0325 e11c b6 01         ROW     LDA     PORTB           READ KEYBOARD
0326 e11e a5 30                 BIT     #$30            ANY INPUT LINE HIGH ?
0327 e120 26 07                 BNE     L1
0328 e122 5a                    DECX                    NO, TRY NEXT COLUMN
0329 e123 26 f0                 BNE     KEY1            LAST COLUMN ?
0330 e125 3f a9                 CLR     KEY             YES, NO KEY PRESSED
0331 e127 20 0c                 BRA     EXIT
0332
0333 e129 b6 01         L1      LDA     PORTB           READ KEYBOARD
0334 e12b a4 f0                 AND     #$F0
0335 e12d b1 a9                 CMP     KEY             SAME AS LAST TIME ?
0336 e12f 27 04                 BEQ     EXIT
0337 e131 b7 a9                 STA     KEY             NO, SAVE THIS KEY
0338 e133 3f aa                 CLR     KOUNT
0339 e135 3c aa         EXIT    INC     KOUNT           YES, THE SAME
0340 e137 b6 aa                 LDA     KOUNT
0341 e139 09 ca 04              BRCLR   4,STAT3,NRML    REPEATING ?
0342 e13c a1 0a                 CMP     #10             YES, REPEAT AT 6 Hz
0343 e13e 20 08                 BRA     GON2
0344 e140 a1 03         NRML    CMP     #3              NO, 3 THE SAME ?
0345 e142 25 29                 BLO     KCLC            IF NOT DO NOTHING
0346 e144 27 1b                 BEQ     GOON            IF 3 THEN PERFORM KEY FUNCTION
0347 e146 a1 30                 CMP     #48             MORE THAN 3, MORE THAN 48 (750mS) ?
0348 e148 22 06         GON2    BHI     GOON2           TIME TO DO SOMETHING ?
0349 e14a b6 a9                 LDA     KEY             NO
0350 e14c 27 19                 BEQ     RKEY            KEY PRESSED ?
0351 e14e 98                    CLC
0352 e14f 81                    RTS                     YES BUT DO NOTHING
0353
0354 e150 b6 a9         GOON2   LDA     KEY
0355 e152 a1 50                 CMP     #$50            SLEEP (DEC.)
0356 e154 27 04                 BEQ     GOON3
0357 e156 a1 90                 CMP     #$90            RDS (INC.)
0358 e158 26 0f                 BNE     DNT2            IF NOT A REPEAT KEY, DO NOTHING
0359 e15a 0b cb 0c      GOON3   BRCLR   5,STAT4,DNT2    REPEAT KEY, BUT IS MODE ALARM SET-UP ?
0360 e15d 18 ca                 BSET    4,STAT3         YES, SET REPEAT FLAG
0361 e15f 3f aa                 CLR     KOUNT
0362 e161 b6 a9         GOON    LDA     KEY
0363 e163 27 02                 BEQ     RKEY            SOMETHING TO DO ?
0364 e165 99                    SEC                     YES, SET C
0365 e166 81                    RTS
0366 e167 1b ca         RKEY    BCLR    5,STAT3         NO, CLEAR DONE FLAG
0367 e169 19 ca         DNT2    BCLR    4,STAT3         CLEAR REPEAT FLAG
0368 e16b 3f aa                 CLR     KOUNT           CLEAR COUNTER
0369 e16d 98            KCLC    CLC
0370 e16e 81                    RTS
0371
0372                    ************************************************
0373                    *                                              *
0374                    *       Execute key function.                  *
0375                    *                                              *
0376                    ************************************************
0377
0378 e16f 24 26         KEYP    BCC     DNT             ANYTHING TO DO ?
0379 e171 b6 a9         KEYP2   LDA     KEY             YES, GET KEY
0380 e173 a1 50                 CMP     #$50            SLEEP (DEC.)
0381 e175 27 07                 BEQ     RPT
0382 e177 a1 90                 CMP     #$90            RDS (INC.)
0383 e179 27 03                 BEQ     RPT
0384 e17b 0a ca 19              BRSET   5,STAT3,DNT     NOT A REPEAT KEY, DONE FLAG SET ?
0385
0386 e17e 5f            RPT     CLRX
0387 e17f d6 e1 98      RJ      LDA     CTAB,X          FETCH KEYCODE
0388 e182 b1 a9                 CMP     KEY             THIS ONE ?
0389 e184 27 0b                 BEQ     RJ              YES
0390 e186 c1 e1 a4              CMP     LAST            NO, LAST CHANCE ?
0391 e189 27 0c                 BEQ     DNT             YES, ABORT
0392 e18b 5c                    INCX                    NO
0393 e18c 5c                    INCX                    TRY
0394 e18d 5c                    INCX                    THE
0395 e18e 5c                    INCX                    NEXT
0396 e18f 20 ee                 BRA     RJ              KEY
0397 e191 1a ca         RJ      BSET    5,STAT3         KEY FUNCTION DONE
0398 e193 5c                    INCX
0399 e194 dd e1 98              JSR     CTAB,X
0400 e197 81            DNT     RTS
0401
0402                    ************************************************
0403                    *                                              *
0404                    *       Keyboard jump table.                   *
0405                    *                                              *
0406                    ************************************************
0407
0408 e198 60            CTAB    FCB     $60             ALARM
0409 e199 cc e1 a8              JMP     ALARM
0410 e19c a0                    FCB     $A0             ON/OFF
0411 e19d cc e1 c7              JMP     ON/OFF
0412 e1a0 50                    FCB     $50             SLEEP TIMER START
0413 e1a1 cc e1 fa              JMP     SLEEP
0414 e1a4 90            LAST    FCB     $90             RDS DISPLAYS
0415 e1a5 cc e2 26              JMP     RDS
```

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0417                        ********************************************************
0418                        *                                                      *
0419                        *       Alarm key.                                     *
0420                        *                                                      *
0421                        ********************************************************
0422
0423 e1a8 05 04 4c          ALARM   BRCLR   2,PORTE,ALRG     ALARM RINGING ?
0424 e1ab 07 cb 0b                  BRCLR   3,STAT4,ADON    NO, ALARM DISPLAY ON ?
0425 e1ae 09 cb 04                  BRCLR   4,STAT4,ALOF    YES, ALARM ON ?
0426 e1b1 19 cb                     BCLR    4,STAT4         YES, SWITCH OFF
0427 e1b3 20 09                     BRA     UDCNT
0428 e1b5 18 cb             ALOF    BSET    4,STAT4         NO, SWITCH ON
0429 e1b7 20 05                     BRA     UDCNT
0430 e1b9 cd e8 0a          ADON    JSR     CLTR
0431 e1bc 16 cb                     BSET    3,STAT4         ALARM DISPLAY FLAG
0432 e1be 1b cb             UDCNT   BCLR    5,STAT4         CANCEL SET-UP
0433 e1c0 a6 19                     LDA     #25             3 SECOND TIMEOUT
0434 e1c2 b7 77                     STA     DIST
0435 e1c4 10 cb                     BSET    0,STAT4         SET DISPLAY TRANSIENT FLAG
0436 e1c6 81                ABOA    RTS
0437
0438                        ********************************************************
0439                        *                                                      *
0440                        *       On/off key (alarm set-up).                     *
0441                        *                                                      *
0442                        ********************************************************
0443
0444 e1c7 05 04 2d          ONOFF   BRCLR   2,PORTE,ALRG    ALARM RINGING ?
0445 e1ca 07 cb 1c                  BRCLR   3,STAT4,NOTALR  NO, ALARM DISPLAY ?
0446 e1cd 09 cb 19                  BRCLR   4,STAT4,NOTALR  YES, ALARM ARMED ?
0447 e1d0 0a cb 0b                  BRSET   5,STAT4,AISM    YES, ALREADY SET-UP MODE ?
0448 e1d3 1a cb                     BSET    5,STAT4         NO, ENTER SET-UP MODE
0449 e1d5 1c cb                     BSET    6,STAT4         WITH HOURS
0450 e1d7 a6 50             A5SD    LDA     #80
0451 e1d9 b7 77                     STA     DIST
0452 e1db 10 cb                     BSET    0,STAT4         SET DISPLAY TRANSIENT FLAG
0453 e1dd 81                NTB2    RTS
0454
0455 e1de 0c cb 04          AISM    BRSET   6,STAT4,MSM     SET-UP HOURS ?
0456 e1e1 1b cb                     BCLR    5,STAT4         NO, CANCELL SET-UP
0457 e1e3 20 f2                     BRA     A5SD
0458 e1e5 1d cb             MSM     BCLR    6,STAT4         YES, MAKE IT MINUTES
0459 e1e7 20 ee                     BRA     A5SD
0460
0461                        ********************************************************
0462                        *                                                      *
0463                        *       On/off key (normal function).                  *
0464                        *                                                      *
0465                        ********************************************************
0466
0467 e1e9 cd e8 0a          NOTALR  JSR     CLTR            CLEAR DISPLAY TRANSIENTS
0468 e1ec 13 cb                     BCLR    1,STAT4         CANCEL SLEEP TIMER
0469 e1ee 06 04 03                  BRSET   3,PORTE,ALRON   ON ?
0470 e1f1 16 04             SODM    BSET    3,PORTE         NO, SWITCH ON
0471 e1f3 81                        RTS
0472 e1f4 17 04             ALRON   BCLR    3,PORTE         YES, SWITCH OFF
0473 e1f6 81                        RTS
0474 e1f7 14 04             ALRG    BSET    2,PORTE         CANCEL ALARM
0475 e1f9 81                        RTS
0476
0477                        ********************************************************
0478                        *                                                      *
0479                        *       Sleep key.                                     *
0480                        *                                                      *
0481                        ********************************************************
0482
0483 e1fa 05 04 fa          SLEEP   BRCLR   2,PORTE,ALRG    ALARM RINGING ?
0484 e1fd 0b cb 03                  BRCLR   5,STAT4,NOTAL   NO, ALARM SET-UP ?
0485 e200 cc e2 79                  JMP     PDEC            YES
0486 e203 04 cb 10          NOTAL   BRSET   2,STAT4,DECS    NO, ALREADY SLEEP DISPLAY ?
0487 e206 02 cb 06                  BRSET   1,STAT4,STR2    NO, SLEEP TIMER ALREADY RUNNING ?
0488 e209 a6 3c             INSLP   LDA     #60             NO, INITIALISE SLEEP TIMER
0489 e20b b7 78                     STA     SLEPT
0490 e20d 12 cb                     BSET    1,STAT4         START SLEEP TIMER
0491 e20f cd e8 0a          STR2    JSR     CLTR            YES, CLEAR DISPLAY TRANSIENTS
0492 e212 14 cb                     BSET    2,STAT4         SLEEP DISPLAY
0493 e214 20 08                     BRA     SLPTOK          NO DECREMENT IF FIRST TIME
0494 e216 b6 78             DECS    LDA     SLEPT           DECREMENT SLEEP TIMER
0495 e218 a0 05                     SUB     #5
0496 e21a b7 78                     STA     SLEPT
0497 e21c 2b eb                     BMI     INSLP           IF UNDERFLOW WRAP ROUND TO 60
0498 e21e a6 19             SLPTOK  LDA     #25
0499 e220 b7 77                     STA     DIST
0500 e222 10 cb                     BSET    0,STAT4         START DISPLAY TRANSIENT
0501 e224 20 cb                     BRA     SODM
0502
0503                        ********************************************************
0504                        *                                                      *
0505                        *       RDS display key.                               *
0506                        *                                                      *
0507                        ********************************************************
0508
0509 e226 05 04 ce          RDS     BRCLR   2,PORTE,ALRG    ALARM RINGING ?
0510 e229 0a cb 29                  BRSET   5,STAT4,PINC    NO, ALARM SET-UP ?
0511 e22c 07 04 17                  BRCLR   3,PORTE,SRT3    NO, STANDBY ?
0512 e22f 0e cb 03                  BRSET   7,STAT4,NOTRT   ALREADY RDS ?
0513 e232 05 c9 12                  BRCLR   2,STAT2,NORT    ALREADY RT DISPLAY ?
0514 e235 1e cb             NOTRT   BSET    7,STAT4         SET RDS DISPLAY FLAG
0515 e237 b6 af                     LDA     RTDIS           MOVE ON
0516 e239 4c                        INCA
0517 e23a a1 13                     CMP     #19
0518 e23c 27 09                     BEQ     NORT
0519 e23e b7 af                     STA     RTDIS
0520 e240 a6 64                     LDA     #100            12 SECOND TIMEOUT
0521 e242 b7 77                     STA     DIST
0522 e244 10 cb                     BSET    0,STAT4         RE-START TRANSIENT TIMEOUT
0523 e246 81                SRT3    RTS
0524
0525 e247 cd e8 0a          NORT    JSR     CLTR            CLEAR DISPLAY TRANSIENTS
0526 e24a 14 c9                     BSET    2,STAT2         SET RT DISPLAY FLAG
0527 e24c a6 09                     LDA     #9
0528 e24e b7 9f                     STA     DISP1
0529 e250 a6 01                     LDA     #1
0530 e252 b7 a0                     STA     DISP2
0531 e254 81                        RTS
```

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0533                            ***************************************************
0534                            *                                                 *
0535                            *       Increment alarm time.                     *
0536                            *                                                 *
0537                            ***************************************************
0538
0539 e255 0c cb 0e      PINC    BRSET   6,STAT4,IHR     SET-UP HOURS ?
0540 e258 b6 9d                 LDA     AMIN            NO, MINUTES
0541 e25a a1 3b                 CMP     #59
0542 e25c 24 04                 BHS     TCOH
0543 e25e 3c 9d                 INC     AMIN
0544 e260 20 0c                 BRA     T5S
0545 e262 3f 9d         TCOH    CLR     AMIN
0546 e264 20 08                 BRA     T5S
0547 e266 b6 9e         IHR     LDA     AOUR
0548 e268 a1 17                 CMP     #23
0549 e26a 24 09                 BHS     HTOH
0550 e26c 3c 9e                 INC     AOUR
0551 e26e a6 50         T5S     LDA     #80             10 SECOND TIMEOUT
0552 e270 b7 77                 STA     DIST
0553 e272 10 cb                 BSET    0,STAT4         SET DISPLAY TRANSIENT FLAG
0554 e274 81                    RTS
0555 e275 3f 9e         HTOH    CLR     AOUR
0556 e277 20 f5                 BRA     T5S
0557
0558                            ***************************************************
0559                            *                                                 *
0560                            *       Decrement alarm time.                     *
0561                            *                                                 *
0562                            ***************************************************
0563
0564 e279 0c cb 0e      PDEC    BRSET   6,STAT4,IHRD    SET-UP HOURS ?
0565 e27c 3d 9d                 TST     AMIN            NO, MINUTES
0566 e27e 27 04                 BEQ     MZ
0567 e280 3a 9d                 DEC     AMIN
0568 e282 20 0c                 BRA     T5SD
0569 e284 a6 3b         MZ      LDA     #59
0570 e286 b7 9d                 STA     AMIN
0571 e288 20 06                 BRA     T5SD
0572 e28a 3d 9e         IHRD    TST     AOUR
0573 e28c 27 09                 BEQ     HZ
0574 e28e 3a 9e                 DEC     AOUR
0575 e290 a6 50         T5SD    LDA     #80             10 SECOND TIMEOUT
0576 e292 b7 77                 STA     DIST
0577 e294 10 cb                 BSET    0,STAT4         SET DISPLAY TRANSIENT FLAG
0578 e296 81                    RTS
0579 e297 a6 17         HZ      LDA     #23
0580 e299 b7 9e                 STA     AOUR
0581 e29b 20 f3                 BRA     T5SD
0582
0583                            ***************************************************
0584                            *                                                 *
0585                            *       Timer interrupt routine.                  *
0586                            *                                                 *
0587                            ***************************************************
0588
0589 e29d 3c 9f         TINTB   INC     DISP1             DISP1    DISP2    DISPLAY
0590 e29f b6 9f                 LDA     DISP1              0 -  8       0     PTY
0591 e2a1 a1 08                 CMP     #8                 9 -  78   1 - 70   MOVING RT
0592 e2a3 23 06                 BLS     NWR               78 -  88      70   END OF RT
0593 e2a5 a1 4e                 CMP     #78
0594 e2a7 22 02                 BHI     NWR             END OF RADIOTEXT ?
0595 e2a9 3c a0                 INC     DISP2           NO, MOVE RADIOTEXT ONE CHARACTER
0596 e2ab a1 58         NWR     CMP     #88             2 SECONDS AT END OF RADIOTEXT
0597 e2ad 25 02                 BLO     NWR2
0598 e2af 15 c9                 BCLR    2,STAT2         RETURN TO NORMAL DISPLAY
0599 e2b1 1b 0e         NWR2    BCLR    5,ICR           CLEAR TIMER B INTERRUPT FLAG
0600 e2b3 16 c9                 BSET    3,STAT2         UPDATE DISPLAY
0601 e2b5 3c 99         CLCK    INC     TH8             UPDATE EIGHTHS OF SECONDS
0602 e2b7 3a 77                 DEC     DIST            DECREMENT TRANSIENT DISPLAY TIMER
0603 e2b9 3c 79                 INC     RDSTO
0604 e2bb b6 79                 LDA     RDSTO
0605 e2bd a1 50                 CMP     #80             10S WITHOUT A GROUP 0 OR 15 ?
0606 e2bf 25 10                 BLO     RDSOK
0607 e2c1 15 ca                 BCLR    2,STAT3         YES, CLEAR TA FLAG
0608 e2c3 3f 8e         N14B    CLR     PTY             PROGRAM TYPE
0609 e2c5 3f 8f                 CLR     PI              AND
0610 e2c7 3f 90                 CLR     PI+1            PI CODE
0611 e2c9 3f 91                 CLR     PIN             AND
0612 e2cb 3f 92                 CLR     PIN+1           PIN
0613 e2cd 3f b0                 CLR     DI              AND DI
0614 e2cf 11 ca                 BCLR    0,STAT3         AND M/S
0615 e2d1 b6 99         RDSOK   LDA     TH8             EIGHTHS OF SECONDS
0616 e2d3 a1 08                 CMP     #8
0617 e2d5 26 32                 BNE     NOTC            PAST 7 ?
0618 e2d7 3f 99                 CLR     TH8             YES, CLEAR
0619 e2d9 3c 9a                 INC     SEC             UPDATE SECONDS
0620 e2db b6 9a                 LDA     SEC
0621 e2dd a1 38                 CMP     #56
0622 e2df 26 02                 BNE     NOT5
0623 e2e1 3a 78                 DEC     SLEPT           DECREMENT SLEEP TIMER MINUTES
0624 e2e3 a1 3c         NOT5    CMP     #60
0625 e2e5 26 22                 BNE     NOTC            PAST 59 ?
0626 e2e7 3f 9a                 CLR     SEC             YES, CLEAR
0627 e2e9 3c 9b                 INC     MIN             UPDATE MINUTES
0628 e2eb b6 9b                 LDA     MIN
0629 e2ed a1 3c                 CMP     #60
0630 e2ef 26 18                 BNE     NOTC            PAST 59 ?
0631 e2f1 3f 9b                 CLR     MIN             YES, CLEAR
0632 e2f3 3c 9c                 INC     OUR             UPDATE HOURS
0633 e2f5 b6 9c                 LDA     OUR
0634 e2f7 a1 18                 CMP     #24
0635 e2f9 26 0e                 BNE     NOTC            PAST 23 ?
0636 e2fb 3f 9c                 CLR     OUR             YES CLEAR
0637 e2fd 3c 76                 INC     BMJD+2          AND ADD A DAY
0638 e2ff 26 06                 BNE     NOTD
0639 e301 3c 75                 INC     BMJD+1
0640 e303 26 02                 BNE     NOTD            INC BMJD only ever executes once, at midnight
0641 e305 3c 74                 INC     BMJD            on the night of Thu/Fri 22/23 April 2038.
0642 e307 1c ca         NOTD    BSET    6,STAT3         UPDATE DATE
0643 e309 80            NOTC    RTI
```

```
0645                            ************************************************
0646                            *                                              *
0647                            *       RDS clock interrupt (IRQ).             *
0648                            *       Get a bit and calculate syndrome.      *
0649                            *                                              *
0650                            ************************************************
0651
0652 e30a 04 01 00      SDATA   BRSET   2,PORTB,*+3
0653 e30d 39 7d                 ROL     DAT+3
0654 e30f 39 7c                 ROL     DAT+2
0655 e311 39 7b                 ROL     DAT+1
0656 e313 39 7a                 ROL     DAT
0657 e315 01 c9 0b              BRCLR   0,STAT2,TRY2    BIT BY BIT CHECK ?
0658 e318 3a 94                 DEC     BIT             NO, WAIT FOR BIT 26
0659 e31a 27 03                 BEQ     TRY1            THIS TIME ?
0660 e31c 17 0e                 BCLR    3,ICR           CLEAR IRQ INTERRUPT FLAG
0661 e31e 80                    RTI
0662
0663 e31f a6 1a         TRY1    LDA     #26
0664 e321 b7 94                 STA     BIT
0665 e323 b6 7a         TRY2    LDA     DAT             MSB (2 BITS)
0666 e325 a4 03                 AND     #3
0667 e327 97                    TAX
0668 e328 b6 7b                 LDA     DAT+1
0669 e32a b7 97                 STA     SYN+1           LSB
0670 e32c 01 7d 0a      S03     BRCLR   0,DAT+3,S13
0671 e32f b6 97                 LDA     SYN+1
0672 e331 a8 1b                 EOR     #$1B
0673 e333 b7 97                 STA     SYN+1
0674 e335 9f                    TXA
0675 e336 a8 03                 EOR     #$03
0676 e338 97                    TAX
0677 e339 03 7d 0a      S13     BRCLR   1,DAT+3,S23
0678 e33c b6 97                 LDA     SYN+1
0679 e33e a8 8f                 EOR     #$8F
0680 e340 b7 97                 STA     SYN+1
0681 e342 9f                    TXA
0682 e343 a8 03                 EOR     #$03
0683 e345 97                    TAX
0684 e346 05 7d 0a      S23     BRCLR   2,DAT+3,S43
0685 e349 b6 97                 LDA     SYN+1
0686 e34b a8 a7                 EOR     #$A7
0687 e34d b7 97                 STA     SYN+1
0688 e34f 9f                    TXA
0689 e350 a8 02                 EOR     #$02
0690 e352 97                    TAX
0691 e353 09 7d 0a      S43     BRCLR   4,DAT+3,S53
0692 e356 b6 97                 LDA     SYN+1
0693 e358 a8 ee                 EOR     #$EE
0694 e35a b7 97                 STA     SYN+1
0695 e35c 9f                    TXA
0696 e35d a8 01                 EOR     #$01
0697 e35f 97                    TAX
0698 e360 0b 7d 0a      S53     BRCLR   5,DAT+3,S63
0699 e363 b6 97                 LDA     SYN+1
0700 e365 a8 dc                 EOR     #$DC
0701 e367 b7 97                 STA     SYN+1
0702 e369 9f                    TXA
0703 e36a a8 03                 EOR     #$03
0704 e36c 97                    TAX
0705 e36d 0d 7d 0a      S63     BRCLR   6,DAT+3,S73
0706 e370 b6 97                 LDA     SYN+1
0707 e372 a8 01                 EOR     #$01
0708 e374 b7 97                 STA     SYN+1
0709 e376 9f                    TXA
0710 e377 a8 02                 EOR     #$02
0711 e379 97                    TAX
0712 e37a 0f 7d 0a      S73     BRCLR   7,DAT+3,S02
0713 e37d b6 97                 LDA     SYN+1
0714 e37f a8 bb                 EOR     #$BB
0715 e381 b7 97                 STA     SYN+1
0716 e383 9f                    TXA
0717 e384 a8 01                 EOR     #$01
0718 e386 97                    TAX
0719 e387 01 7c 0a      S02     BRCLR   0,DAT+2,S12
0720 e38a b6 97                 LDA     SYN+1
0721 e38c a8 76                 EOR     #$76
0722 e38e b7 97                 STA     SYN+1
0723 e390 9f                    TXA
0724 e391 a8 03                 EOR     #$03
0725 e393 97                    TAX
0726 e394 03 7c 0a      S12     BRCLR   1,DAT+2,S22
0727 e397 b6 97                 LDA     SYN+1
0728 e399 a8 55                 EOR     #$55
0729 e39b b7 97                 STA     SYN+1
0730 e39d 9f                    TXA
0731 e39e a8 03                 EOR     #$03
0732 e3a0 97                    TAX
0733 e3a1 05 7c 0a      S22     BRCLR   2,DAT+2,S32
0734 e3a4 b6 97                 LDA     SYN+1
0735 e3a6 a8 13                 EOR     #$13
0736 e3a8 b7 97                 STA     SYN+1
0737 e3aa 9f                    TXA
0738 e3ab a8 03                 EOR     #$03
0739 e3ad 97                    TAX
0740 e3ae 07 7c 0a      S32     BRCLR   3,DAT+2,S42
0741 e3b1 b6 97                 LDA     SYN+1
0742 e3b3 a8 9f                 EOR     #$9F
0743 e3b5 b7 97                 STA     SYN+1
0744 e3b7 9f                    TXA
0745 e3b8 a8 03                 EOR     #$03
0746 e3ba 97                    TAX
0747 e3bb 09 7c 0a      S42     BRCLR   4,DAT+2,S62
0748 e3be b6 97                 LDA     SYN+1
0749 e3c0 a8 87                 EOR     #$87
0750 e3c2 b7 97                 STA     SYN+1
0751 e3c4 9f                    TXA
0752 e3c5 a8 02                 EOR     #$02
0753 e3c7 97                    TAX
0754 e3c8 0d 7c 0a      S62     BRCLR   6,DAT+2,S72
0755 e3cb b6 97                 LDA     SYN+1
0756 e3cd a8 6e                 EOR     #$6E
0757 e3cf b7 97                 STA     SYN+1
0758 e3d1 9f                    TXA
0759 e3d2 a8 01                 EOR     #$01
0760 e3d4 97                    TAX
0761 e3d5 0f 7c 09      S72     BRCLR   7,DAT+2,S33
0762 e3d8 b6 97                 LDA     SYN+1
0763 e3da a8 dc                 EOR     #$DC
0764 e3dc b7 97                 STA     SYN+1
0765 e3de 9f                    TXA
0766 e3df a8 02                 EOR     #$02
0767 e3e1 b7 96         S33     STA     SYN
0768 e3e3 b6 97                 LDA     SYN+1
0769 e3e5 07 7d 02              BRCLR   3,DAT+3,S52
0770 e3e8 a8 f7                 EOR     #$F7
0771 e3ea 0b 7c 02      S52     BRCLR   5,DAT+2,FIN
0772 e3ed a8 b7                 EOR     #$B7
0773 e3ef b7 97         FIN     STA     SYN+1
```

```
0775                            ***************************************************
0776                            *                                                 *
0777                            *       Check for syndromes A, B, C & C'.         *
0778                            *                                                 *
0779                            ***************************************************
0780
0781 e3f1 17 0e                        BCLR    3,ICR           CLEAR IRQ INTERRUPT FLAG
0782
0783 e3f3 b6 93                        LDA     LEV
0784 e3f5 a1 03                        CMP     #3
0785 e3f7 27 5d                        BEQ     TRYD
0786 e3f9 a1 02                        CMP     #2
0787 e3fb 27 22                        BEQ     TRYC
0788 e3fd a1 01                        CMP     #1
0789 e3ff 27 10                        BEQ     TRYB
0790 e401 3f 93                        CLR     LEV
0791
0792 e403 b6 97                TRYA    LDA     SYN+1           BLOCK 1
0793 e405 a1 d8                        CMP     #$D8
0794 e407 26 31                        BNE     NOTV
0795 e409 b6 96                        LDA     SYN
0796 e40b a1 03                        CMP     #$03
0797 e40d 26 2b                        BNE     NOTV
0798 e40f 20 53                        BRA     VALID
0799
0800 e411 b6 97                TRYB    LDA     SYN+1           BLOCK 2
0801 e413 a1 d4                        CMP     #$D4
0802 e415 26 23                        BNE     NOTV
0803 e417 b6 96                        LDA     SYN
0804 e419 a1 03                        CMP     #$03
0805 e41b 26 1d                        BNE     NOTV
0806 e41d 20 45                        BRA     VALID
0807
0808 e41f 06 80 0c             TRYC    BRSET   3,TMPGRP+2,TRYCD    BLOCK 3 TYPE A
0809 e422 b6 97                        LDA     SYN+1
0810 e424 a1 5c                        CMP     #$5C
0811 e426 26 12                        BNE     NOTV
0812 e428 b6 96                        LDA     SYN
0813 e42a a1 02                        CMP     #$02
0814 e42c 20 0a                        BRA     VC
0815
0816 e42e b6 97                TRYCD   LDA     SYN+1               BLOCK 3 TYPE B
0817 e430 a1 cc                        CMP     #$CC
0818 e432 26 06                        BNE     NOTV
0819 e434 b6 96                        LDA     SYN
0820 e436 a1 03                        CMP     #$03
0821 e438 27 2a                VC      BEQ     VALID
0822
0823                            ***************************************************
0824                            *                                                 *
0825                            *       Invalid syndrome handling, check for      *
0826                            *       block 4 and save group data if valid.     *
0827                            *                                                 *
0828                            ***************************************************
0829
0830 e43a 3f 93                NOTV    CLR     LEV             RESTART AT BLOCK 1
0831 e43c b6 98                        LDA     CONF
0832 e43e a1 29                        CMP     #41             CONFIDENCE 41 OR GREATER ?
0833 e440 24 0e                        BHS     DECC
0834 e442 11 c9                        BCLR    0,STAT2         BIT BY BIT SYNDROME CHECK
0835 e444 a1 0a                        CMP     #10
0836 e446 23 0b                        BLS     SKPDC           CONFIDENCE 10 OR LESS ?
0837 e448 3a 94                        DEC     BIT
0838 e44a 26 06                        BNE     NNOW            USE BIT COUNTER TO SLOW CONFIDENCE
0839 e44c a6 1a                        LDA     #26             DROP DURING BIT BY BIT ATTEMPT TO
0840 e44e b7 94                        STA     BIT             RE-SYNCRONISE
0841 e450 3a 98                DECC    DEC     CONF
0842 e452 80                   NNOW    RTI
0843 e453 18 c9                SKPDC   BSET    4,STAT2         10 OR LESS, INITIALISE DISPLAY
0844 e455 80                   NOT4    RTI
0845
0846 e456 b6 97                TRYD    LDA     SYN+1
0847 e458 a1 58                        CMP     #$58
0848 e45a 26 de                        BNE     NOTV
0849 e45c b6 96                        LDA     SYN
0850 e45e a1 02                        CMP     #$02
0851 e460 26 d8                        BNE     NOTV
0852 e462 12 c9                        BSET    1,STAT2         GROUP COMPLETE
0853
0854 e464 00 c9 06             VALID   BRSET   0,STAT2,VLD     VALID SYNDROME FLAG ALREADY SET ?
0855 e467 a6 26                        LDA     #38             NO,
0856 e469 b7 98                        STA     CONF            INITIALISE CONFIDENCE (38+4=42)
0857 e46b 10 c9                        BSET    0,STAT2         AND SET FLAG
0858 e46d b6 98                VLD     LDA     CONF
0859 e46f a1 38                        CMP     #56
0860 e471 22 04                        BHI     NMR
0861 e473 ab 04                        ADD     #4
0862 e475 b7 98                        STA     CONF
0863 e477 be 93                NMR     LDX     LEV
0864 e479 59                           ROLX
0865 e47a 3c 93                        INC     LEV
0866 e47c a6 1a                        LDA     #26
0867 e47e b7 94                        STA     BIT
0868 e480 36 7a                        ROR     DAT
0869 e482 36 7b                        ROR     DAT+1
0870 e484 36 7c                        ROR     DAT+2
0871 e486 36 7a                        ROR     DAT
0872 e488 36 7b                        ROR     DAT+1
0873 e48a 36 7c                        ROR     DAT+2
0874 e48c b6 7c                        LDA     DAT+2
0875 e48e e7 7f                        STA     TMPGRP+1,X
0876 e490 b6 7b                        LDA     DAT+1
0877 e492 e7 7e                        STA     TMPGRP,X
0878 e494 03 c9 be                     BRCLR   1,STAT2,NOT4    GROUP COMPLETE ?
0879 e497 ae 08                XFER    LDX     #8
0880 e499 e6 7d                TXLP    LDA     TMPGRP-1,X
0881 e49b e7 85                        STA     GROUP-1,X
0882 e49d 5a                           DECX
0883 e49e 26 f9                        BNE     TXLP
```

```
0885                            ************************************************
0886                            *                                              *
0887                            *       Update PI code, initialise if changed. *
0888                            *       All block 1s used, block 3s not used.  *
0889                            *                                              *
0890                            ************************************************
0891
0892 e4a0 b6 86                 PROC    LDA     GROUP           COMPARE PI WITH PREVIOUS
0893 e4a2 b1 8f                         CMP     PI
0894 e4a4 26 06                         BNE     DNDX
0895 e4a6 b6 87                         LDA     GROUP+1
0896 e4a8 b1 90                         CMP     PI+1
0897 e4aa 27 10                         BEQ     PTYL
0898 e4ac b6 86                 DNDX    LDA     GROUP           DIFFERENT, SAVE NEW PI
0899 e4ae b7 8f                         STA     PI
0900 e4b0 b6 87                         LDA     GROUP+1
0901 e4b2 b7 90                         STA     PI+1
0902 e4b4 cd eb e6                      JSR     CLREON          CLEAR EON,
0903 e4b7 cd e8 0a                      JSR     CLTR            TRANSIENTS
0904 e4ba 18 c9                         BSET    4,STAT2         AND INITIALISE DISPLAY DATA
0905
0906                            ************************************************
0907                            *                                              *
0908                            *       Update PTY and TP.                     *
0909                            *       All block 2s used, not block 4 (grp 15B).*
0910                            *                                              *
0911                            ************************************************
0912
0913 e4bc b6 88                 PTYL    LDA     GROUP+2
0914 e4be b7 95                         STA     ITMP1
0915 e4c0 05 95 04                      BRCLR   2,ITMP1,TPL1    TP HIGH ?
0916 e4c3 16 ca                         BSET    3,STAT3         YES, FLAG HIGH
0917 e4c5 20 02                         BRA     TPL
0918 e4c7 17 ca                 TPL1    BCLR    3,STAT3         NO, FLAG LOW
0919 e4c9 b6 89                 TPL     LDA     GROUP+3
0920 e4cb 36 95                         ROR     ITMP1
0921 e4cd 46                            RORA
0922 e4ce 44                            LSRA
0923 e4cf 44                            LSRA
0924 e4d0 44                            LSRA
0925 e4d1 44                            LSRA
0926 e4d2 b7 8e                         STA     PTY
0927
0928                            ************************************************
0929                            *                                              *
0930                            *       Groups handled.                        *
0931                            *                                              *
0932                            *       All         PI, PTY & TP               *
0933                            *       0 A & B     TA, PS, DI & M/S           *
0934                            *       1 A & B     PIN                        *
0935                            *       2 A         RT                         *
0936                            *       4 A         CT                         *
0937                            *      14 A         EON                        *
0938                            *      15 B         TA, DI & M/S               *
0939                            *                                              *
0940                            ************************************************
0941
0942                            ************************************************
0943                            *                                              *
0944                            *       Process groups 0 & 15B (PS & TA).      *
0945                            *                                              *
0946                            ************************************************
0947
0948 e4d4 b6 88                         LDA     GROUP+2
0949 e4d6 a4 f8                         AND     #$F8
0950 e4d8 27 0a                         BEQ     GRP0            GROUP 0A
0951 e4da a1 08                         CMP     #$08            GROUP 0B
0952 e4dc 27 06                         BEQ     GRP0
0953
0954 e4de a1 f8                 TGRP15  CMP     #$F8            GROUP 15B
0955 e4e0 27 10                         BEQ     TACK
0956 e4e2 20 57                         BRA     PROC1
0957
0958 e4e4 b6 89                 GRP0    LDA     GROUP+3         GROUP 0  -  PS & TA
0959 e4e6 a4 03                         AND     #$03
0960 e4e8 48                            LSLA
0961 e4e9 97                            TAX
0962 e4ea b6 8c                         LDA     GROUP+6
0963 e4ec e7 c1                         STA     PSN,X
0964 e4ee b6 8d                         LDA     GROUP+7
0965 e4f0 e7 c2                         STA     PSN+1,X
0966
0967 e4f2 3f 79                 TACK    CLR     RDSTO           RDS OK, RESET TIME-OUT
0968 e4f4 08 89 04                      BRSET   4,GROUP+3,TAH   TA HIGH ?
0969 e4f7 15 ca                         BCLR    2,STAT3         NO, TA FLAG LOW
0970 e4f9 20 02                         BRA     NTD
0971 e4fb 14 ca                 TAH     BSET    2,STAT3         YES, TA FLAG HIGH
```

```
0973                            ************************************************
0974                            *                                              *
0975                            *       Process group 0 & 15B (DI & M/S).      *
0976                            *                                              *
0977                            ************************************************
0978
0979 e4fd b6 89                 NTD     LDA     GROUP+3         DI
0980 e4ff a4 03                         AND     #3
0981 e501 97                            TAX
0982 e502 b6 89                         LDA     GROUP+3
0983 e504 a4 40                         AND     #$40
0984 e506 5d                            TSTX
0985 e507 26 07                         BNE     NOT0
0986 e509 11 b0                         BCLR    0,DI
0987 e50b 4d                            TSTA
0988 e50c 27 02                         BEQ     NOT0
0989 e50e 10 b0                         BSET    0,DI
0990 e510 a3 01                 NOT0    CPX     #1
0991 e512 26 07                         BNE     NOT1
0992 e514 13 b0                         BCLR    1,DI
0993 e516 4d                            TSTA
0994 e517 27 02                         BEQ     NOT1
0995 e519 12 b0                         BSET    1,DI
0996 e51b a3 02                 NOT1    CPX     #2
0997 e51d 26 07                         BNE     NOT2
0998 e51f 15 b0                         BCLR    2,DI
0999 e521 4d                            TSTA
1000 e522 27 02                         BEQ     NOT2
1001 e524 14 b0                         BSET    2,DI
1002 e526 a3 03                 NOT2    CPX     #3
1003 e528 26 07                         BNE     NOT3
1004 e52a 17 b0                         BCLR    3,DI
1005 e52c 4d                            TSTA
1006 e52d 27 02                         BEQ     NOT3
1007 e52f 16 b0                         BSET    3,DI
1008
1009 e531 11 ca                 NOT3    BCLR    0,STAT3         M/S
1010 e533 07 89 02                      BRCLR   3,GROUP+3,MSZ
1011 e536 10 ca                         BSET    0,STAT3
1012 e538 cc e6 18              MSZ     JMP     OUT1
1013
1014                            ************************************************
1015                            *                                              *
1016                            *       Process group 1 (PIN).                 *
1017                            *                                              *
1018                            ************************************************
1019
1020 e53b a1 10                 PROC1   CMP     #$10            GROUP 1A
1021 e53d 27 04                         BEQ     GRP1
1022 e53f a1 18                         CMP     #$18            GROUP 1B
1023 e541 26 0b                         BNE     PROC2
1024
1025 e543 b6 8c                 GRP1    LDA     GROUP+6
1026 e545 b7 91                         STA     PIN
1027 e547 b6 8d                         LDA     GROUP+7
1028 e549 b7 92                         STA     PIN+1
1029
1030 e54b cc e6 18                      JMP     OUT1
1031
1032                            ************************************************
1033                            *                                              *
1034                            *       Process group 2A (RT).                 *
1035                            *       Group 2B not handled.                  *
1036                            *                                              *
1037                            ************************************************
1038
1039 e54e a1 20                 PROC2   CMP     #$20            GROUP 2A
1040 e550 26 30                         BNE     PROC4
1041
1042 e552 08 89 07              GRP2    BRSET   4,GROUP+3,TEXTB
1043 e555 02 ca 0c              TEXTA   BRSET   1,STAT3,NCH
1044 e558 12 ca                         BSET    1,STAT3
1045 e55a 20 05                         BRA     LCDINI
1046 e55c 03 ca 05              TEXTB   BRCLR   1,STAT3,NCH
1047 e55f 13 ca                         BCLR    1,STAT3
1048 e561 cd eb aa              LCDINI  JSR     INITD
1049
1050 e564 b6 89                 NCH     LDA     GROUP+3         GROUP 2A  -  RT
1051 e566 a4 0f                         AND     #$0F
1052 e568 48                            LSLA
1053 e569 48                            LSLA
1054 e56a 97                            TAX
1055 e56b b6 8a                         LDA     GROUP+4
1056 e56d d7 01 05                      STA     RT+5,X
1057 e570 b6 8b                         LDA     GROUP+5
1058 e572 d7 01 06                      STA     RT+6,X
1059 e575 b6 8c                         LDA     GROUP+6
1060 e577 d7 01 07                      STA     RT+7,X
1061 e57a b6 8d                         LDA     GROUP+7
1062 e57c d7 01 08                      STA     RT+8,X
1063 e57f cc e6 18                      JMP     OUT1
```

```
1065                        ************************************************
1066                        *                                              *
1067                        *       Process group 4A (CT).                 *
1068                        *                                              *
1069                        ************************************************
1070
1071 e582 a1 40             PROC4   CMP     #$40            GROUP 4A  -  CT
1072 e584 27 03                     BEQ     GRP4
1073 e586 cc e6 1b                  JMP     PROC14
1074
1075 e589 b6 89             GRP4    LDA     GROUP+3
1076 e58b 46                        RORA
1077 e58c a4 01                     AND     #$01
1078 e58e b7 74                     STA     BMJD            MJD MS BIT
1079 e590 b6 8a                     LDA     GROUP+4
1080 e592 46                        RORA
1081 e593 b7 75                     STA     BMJD+1          MJD MSD
1082
1083 e595 b6 8c                     LDA     GROUP+6         GROUP 4
1084 e597 36 8b                     ROR     GROUP+5         3210xxxx 4
1085 e599 46                        RORA                    43210xxx x
1086 e59a 44                        LSRA                    -43210xx x
1087 e59b 44                        LSRA                    --43210x x
1088 e59c 44                        LSRA                    ---43210 x
1089 e59d b7 9c                     STA     CUR
1090
1091 e59f b6 8b                     LDA     GROUP+5
1092 e5a1 b7 76                     STA     BMJD+2          MJD LSD
1093
1094 e5a3 b6 8c                     LDA     GROUP+6         xxxx5432 x
1095 e5a5 38 8d                     LSL     GROUP+7         xxxx5432 1
1096 e5a7 49                        ROLA                    xxx54321 x
1097 e5a8 38 8d                     LSL     GROUP+7         xxx54321 0
1098 e5aa 49                        ROLA                    xx543210 x
1099 e5ab a4 3f                     AND     #$3F            --543210 x
1100 e5ad b7 9b                     STA     MIN
1101 e5af 3f 9a                     CLR     SEC
1102 e5b1 3f 99                     CLR     TH8
1103 e5b3 1c ca                     BSET    6,STAT3         UPDATE MJD
1104
1105                        ************************************************
1106                        *                                              *
1107                        *       Local time difference adjustment.      *
1108                        *                                              *
1109                        ************************************************
1110
1111 e5b5 b6 8d             LOCAL   LDA     GROUP+7
1112 e5b7 48                        LSLA
1113 e5b8 27 5e                     BEQ     OUT1            ADJUSTMENT ?
1114 e5ba 24 32                     BCC     POS             YES. POSITIVE ?
1115
1116 e5bc 44                NEG     LSRA                    NO. NEGATIVE
1117 e5bd 44                        LSRA
1118 e5be 44                        LSRA
1119 e5bf 44                        LSRA
1120 e5c0 97                        TAX                     HOURS IN X
1121 e5c1 24 0c                     BCC     NOTHN           1/2 HOUR ?
1122 e5c3 b6 9b                     LDA     MIN             YES
1123 e5c5 a0 1e                     SUB     #30             SUBTRACT 30 MINUTES
1124 e5c7 2a 04                     BPL     LT60            UNDERFLOW ?
1125 e5c9 ab 3c                     ADD     #60             YES. ADD 60 MINUTES
1126 e5cb 3a 9c                     DEC     CUR             AND SUBTRACT 1 HOUR
1127 e5cd b7 9b             LT60    STA     MIN
1128
1129 e5cf 9f                NOTHN   TXA                     NEGATIVE HOUR OFFSET
1130 e5d0 b0 9c                     SUB     CUR             MINUS UTC HOURS
1131 e5d2 43                        COMA                    WRONG WAY ROUND SO COMPLEMENT
1132 e5d3 4c                        INCA                    AND INCREMENT
1133 e5d4 2a 14                     BPL     ZOM             UNDERFLOW ?
1134 e5d6 ab 18                     ADD     #24             YES. ADD 24 HOURS
1135 e5d8 b7 9c                     STA     CUR
1136
1137 e5da 3d 76                     TST     BMJD+2          AND SUBTRACT A DAY
1138 e5dc 26 08                     BNE     TT2             LSB WILL UNDERFLOW ?
1139 e5de 3d 75                     TST     BMJD+1          YES
1140 e5e0 26 02                     BNE     TT1             MSB WILL UNDERFLOW ?
1141 e5e2 3a 74                     DEC     BMJD            YES DECREMENT MS BIT
1142 e5e4 3a 75             TT1     DEC     BMJD+1          DECREMENT MSB
1143 e5e6 3a 76             TT2     DEC     BMJD+2          DECREMENT LSB
1144 e5e8 20 2e                     BRA     OUT1
1145
1146 e5ea b7 9c             ZOM     STA     CUR
1147 e5ec 20 2a                     BRA     OUT1
1148
1149 e5ee 44                POS     LSRA                    POSITIVE ADJUSTMENT
1150 e5ef 44                        LSRA
1151 e5f0 44                        LSRA
1152 e5f1 44                        LSRA
1153 e5f2 97                        TAX                     HOURS IN X
1154 e5f3 24 0e                     BCC     NOTHP           HALF HOUR ?
1155 e5f5 a6 1e                     LDA     #30             YES. ADD 30 MINUTES
1156 e5f7 bb 9b                     ADD     MIN
1157 e5f9 a1 3b                     CMP     #59
1158 e5fb 23 04                     BLS     HDON            OVERFLOW ?
1159 e5fd a0 3c                     SUB     #60             YES. SUBTRACT 60 MINUTES
1160 e5ff 3c 9c                     INC     CUR             AND ADD AN HOUR
1161 e601 b7 9b             HDON    STA     MIN
1162
1163 e603 9f                NOTHP   TXA                     HOUR OFFSET
1164 e604 bb 9c                     ADD     CUR             ADD UTC HOURS
1165 e606 a1 17                     CMP     #23
1166 e608 23 0c                     BLS     ADDON           OVERFLOW ?
1167 e60a a0 18                     SUB     #24             YES. SUBTRACT 24 HOURS
1168 e60c 3c 76                     INC     BMJD+2          AND ADD A DAY
1169 e60e 26 06                     BNE     ADDON
1170 e610 3c 75                     INC     BMJD+1
1171 e612 26 02                     BNE     ADDON
1172 e614 3c 74                     INC     BMJD
1173 e616 b7 9c             ADDON   STA     CUR
1174 e618 13 c9             OUT1    BCLR    1,STAT2         GROUP HANDLED. CLEAR FLAG
1175 e61a 80                        RTI
```

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1177                            ************************************************
1178                            *                                              *
1179                            *       Process group 14 (EON).                *
1180                            *                                              *
1181                            ************************************************
1182
1183 e61b a1 e0          PROC14  CMP     #$E0
1184 e61d 27 03                 BEQ     GRP14A
1185 e61f cc e6 b3              JMP     OUT2
1186
1187 e622 3f 95          GRP14A  CLR     ITMP1           LOOK FOR PI CODE IN TABLE
1188 e624 be 95          LPIL    LDX     ITMP1
1189 e626 d6 01 45              LDA     EON,X
1190 e629 b1 8c                 CMP     GROUP+6
1191 e62b 26 69                 BNE     NOTH
1192 e62d d6 01 46              LDA     EON+1,X
1193 e630 b1 8d                 CMP     GROUP+7
1194 e632 26 62                 BNE     NOTH
1195
1196                            *       LDA     GROUP+3         TP (ON), NOT USED
1197                            *       AND     #$10
1198                            *       LDX     ITMP1
1199                            *       STA     EON+11,X
1200
1201 e634 b6 89                         LDA     GROUP+3         PI CODE FOUND
1202 e636 a4 0f                         AND     #$0F
1203 e638 a1 04                         CMP     #4              PS ?
1204 e63a 24 10                         BHS     NPS
1205 e63c 48                            LSLA                    YES
1206 e63d bb 95                         ADD     ITMP1
1207 e63f 97                            TAX
1208 e640 b6 8a                         LDA     GROUP+4
1209 e642 d7 01 47                      STA     EON+2,X         SAVE 2 PS-NAME CHARACTERS
1210 e645 b6 8b                         LDA     GROUP+5
1211 e647 d7 01 48                      STA     EON+3,X
1212 e64a 20 cc                         BRA     OUT1
1213
1214 e64c a1 04          NPS    CMP     #4              AF ?
1215 e64e 26 34                 BNE     TRYPIN
1216
1217 e650 b6 8a                         LDA     GROUP+4         YES, METHOD A
1218
1219 e652 a1 fa                         CMP     #250
1220 e654 26 1a                         BNE     NMLW            MEDIUM OR LONG WAVE ?
1221 e656 d6 01 51                      LDA     EON+12,X        YES
1222 e659 a1 ff                         CMP     #$FF            FIRST 2 BYTES ALREADY IN ?
1223 e65b 27 56                         BEQ     OUT2            IF NOT, DO NOTHING
1224 e65d d6 01 53                      LDA     EON+14,X        YES
1225 e660 a1 ff                         CMP     #$FF            M/L FREQUENCY ALREADY IN ?
1226 e662 26 4f                         BNE     OUT2            IF SO, DO NOTHING
1227 e664 a6 fa                         LDA     #250            NO, STORE FIRST FREQUENCY AFTER
1228 e666 d7 01 53                      STA     EON+14,X        ARRIVAL OF INITIAL BYTES
1229 e669 b6 8b                         LDA     GROUP+5
1230 e66b d7 01 54                      STA     EON+15,X
1231 e66e 20 43                         BRA     OUT2
1232
1233 e670 a1 e0          NMLW   CMP     #224            FM
1234 e672 25 0e                 BLO     TOOLS           LEGAL ? (No. OF FREQUENCIES)
1235 e674 a1 f9                 CMP     #249
1236 e676 22 0a                 BHI     TOOLS
1237 e678 be 95                 LDX     ITMP1
1238 e67a d7 01 51              STA     EON+12,X        YES, SAVE No. OF FREQUENCIES
1239 e67d b6 8b                 LDA     GROUP+5
1240 e67f d7 01 52              STA     EON+13,X        AND FIRST FREQUENCY
1241 e682 20 2f          TOOLS  BRA     OUT2
1242
1243                            *TRYPTY CMP     #$0D
1244                            *       BNE     TRYPIN
1245                            *       LDA     GROUP+4         PTY (EON), NOT USED
1246                            *       LSRA
1247                            *       LSRA
1248                            *       LSRA
1249                            *       LDX     ITMP1
1250                            *       STA     EON+10,X
1251                            *       BRA     OUT2
1252
1253 e684 a1 0e          TRYPIN CMP     #$0E
1254 e686 26 2b                 BNE     OUT2
1255 e688 be 95                 LDX     ITMP1           PIN
1256 e68a b6 8a                 LDA     GROUP+4
1257 e68c d7 01 4f              STA     EON+10,X
1258 e68f b6 8b                 LDA     GROUP+5
1259 e691 d7 01 50              STA     EON+11,X
1260 e694 20 1d                 BRA     OUT2
1261
1262 e696 a1 ff          NOTH   CMP     #$FF            END OF PI LIST ?
1263 e698 26 0c                 BNE     NOTH1
1264 e69a b6 8c                 LDA     GROUP+6         YES, ADD THIS PI CODE
1265 e69c d7 01 45              STA     EON,X
1266 e69f b6 8d                 LDA     GROUP+7         TO EON TABLE
1267 e6a1 d7 01 46              STA     EON+1,X
1268 e6a4 20 0d                 BRA     OUT2
1269
1270 e6a6 b6 95          NOTH1  LDA     ITMP1           NOT END, TRY NEXT ENTRY
1271 e6a8 ab 10                 ADD     #16
1272 e6aa b7 95                 STA     ITMP1
1273 e6ac a1 b0                 CMP     #$B0            END OF TABLE (11 ENTRIES) ?
1274 e6ae 27 03                 BEQ     OUT2
1275 e6b0 cc e6 24              JMP     LPIL
1276
1277 e6b3 13 c9          OUT2   BCLR    1,STAT2         GROUP HANDLED, CLEAR FLAG
1278 e6b5 80                    RTI
```

```
                        ***************************************************
                        *                                                 *
                        *       Display type selection.                   *
                        *                                                 *
                        ***************************************************

e6b6 09 c9 05   MOD     BRCLR   4,STAT2,NOCL    SHOULD DISPALY BE INITIALISED ?
e6b9 cd eb aa           JSR     INITD           YES, DO IT
e6bc 19 c9              BCLR    4,STAT2         AND CLEAR FLAG
e6be cd eb 6c   NOCL    JSR     WAIT
e6c1 a6 0c              LDA     #$0C            SWITCH DISPLAY ON
e6c3 cd eb 65           JSR     CLOCK           LATCH IT
e6c6 cd eb 6c           JSR     WAIT
                *       LDA     #$3R            /16 DISPLAY
e6c9 a6 30              LDA     #$30            /8  DISPLAY
e6cb cd eb 65           JSR     CLOCK           LATCH IT
e6ce cd eb 6c           JSR     WAIT
e6d1 a6 80              LDA     #$80            ADDRESS DISPLAY RAM
e6d3 cd eb 65           JSR     CLOCK           LATCH IT

e6d6 06 04 0b           BRSET   3,PORTE,TRYRT   STANDBY ?
e6d9 04 cb 59           BRSET   2,STAT4,SLPD    YES, SLEEP DISPLAY ?
e6dc 06 cb 66           BRSET   3,STAT4,ALRMJ   NO, ALARM DISPLAY ?
e6df cd e8 69           JSR     STBYD           NO, NORMAL STANDBY DISPLAY
e6e2 20 64              BRA     ROW1

e6e4 0f cb 46   TRYRT   BRCLR   7,STAT4,RTITS   RDS DISPLAYS ? .
e6e7 b6 af              LDA     RTDIS
e6e9 a1 01              CMP     #1
e6eb 26 05              BNE     NPTY
e6ed cd e8 19           JSR     PTYD            PTY
e6f0 20 56              BRA     ROW1

e6f2 a1 02      NPTY    CMP     #2
e6f4 26 05              BNE     NPI
e6f6 cd e8 fa           JSR     DIPI            PI
e6f9 20 4d              BRA     ROW1

e6fb a1 03      NPI     CMP     #3
e6fd 26 05              BNE     NTAP
e6ff cd e9 5a           JSR     DITAP           TA & TP
e702 20 44              BRA     ROW1

e704 a1 04      NTAP    CMP     #4
e706 26 05              BNE     NPIN1
e708 cd e9 72           JSR     DPIN1           PIN - HEX
e70b 20 3b              BRA     ROW1

e70d a1 05      NPIN1   CMP     #5
e70f 26 05              BNE     NPIN2
e711 cd e9 92           JSR     DPIN2           PIN - DAY AND TIME
e714 20 32              BRA     ROW1

e716 a1 06      NPIN2   CMP     #6
e718 26 05              BNE     NMJD
e71a cd e9 f6           JSR     DMJD            MJD
e71d 20 29              BRA     ROW1

e71f a1 07      NMJD    CMP     #7
e721 26 05              BNE     NMSD
e723 cd eb 03           JSR     DMSD            M/S & DI
e726 20 20              BRA     ROW1

e728 cd ea 25   NMSD    JSR     DEON
e72b 20 1b              BRA     ROW1

e72d 05 c9 05   RTITS   BRCLR   2,STAT2,SLPD    RT DISPLAY ?
e730 cd e8 4a           JSR     RTDS
e733 20 13              BRA     ROW1

e735 05 cb 05   SLPD    BRCLR   2,STAT4,NRMD    SLEEP TIMER DISPLAY ?
e738 cd ea ee           JSR     SLEEPD
e73b 20 0b              BRA     ROW1

e73d 06 cb 05   NRMD    BRSET   3,STAT4,ALRMJ   ALARM DISPLAY ?
e740 cd e7 cc           JSR     NORMD
e743 20 03              BRA     ROW1

e745 cd e9 1a   ALRMJ   JSR     ALRMD

e748 5f         ROW1    CLRX
e749 cd eb 6c   LCD     JSR     WAIT
e74c 14 03              BSET    2,PORTD         WRITE DATA
e74e e6 b1              LDA     DISP,X          GET A BYTE
e750 a1 ff              CMP     #$FF
e752 26 02              BNE     COK
e754 a6 2d              LDA     #$2D
e756 cd eb 65   COK     JSR     CLOCK           SEND IT TO MODULE
e759 5c                 INCX
e75a a3 10              CPX     #16             DONE ?
e75c 26 eb              BNE     LCD
e75e 20 1e              BRA     VFD             REMOVE FOR /16 LCDs

                        ***************************************************
                        *                                                 *
                        *       Additional bits for /16 LCD modules.      *
                        *                                                 *
                        ***************************************************

e760 cd eb 6c   LCD401  JSR     WAIT
e763 a6 a8              LDA     #$A8            TO 40
e765 cd eb 65           JSR     CLOCK           SEND IT TO MODULE
e768 5f                 CLRX
e769 cd eb 6c   LCD41   JSR     WAIT
e76c 14 03              BSET    2,PORTD         WRITE DATA
e76e e6 b9              LDA     DISP+8,X        GET A BYTE
e770 a1 ff              CMP     #$FF
e772 26 02              BNE     COK2
e774 a6 2d              LDA     #$2D
e776 cd eb 65   COK2    JSR     CLOCK           SEND IT TO MODULE
e779 5c                 INCX
e77a a3 08              CPX     #8              DONE ?
e77c 26 eb              BNE     LCD41
```

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1394                            ************************************************
1395                            *                                              *
1396                            *       VFD.                                   *
1397                            *                                              *
1398                            ************************************************
1399
1400 e77e 13 01                VFD     BCLR    1,PORTB         DATA LOW ?
1401 e780 10 01                        BSET    0,PORTB         CLOCK HIGH ?
1402 e782 17 01                        BCLR    3,PORTB         ENABLE LOW
1403
1404 e784 5f                           CLRX                    SEND VFD SET-UP BYTES
1405 e785 d6 e7 c5             DIS5    LDA     INITF,X
1406 e788 bf a7                        STX     W7              SAVE INDEX
1407 e78a ad 20                        BSR     VFDL
1408 e78c a3 07                        CPX     #7
1409 e78e 26 f5                        BNE     DIS5            LAST BYTE ?
1410
1411 e790 5f                           CLRX                    SEND 16 CHARACTER BYTES
1412 e791 bf a7                VFD3    STX     W7              SAVE INDEX
1413 e793 e6 b1                        LDA     DISP,X          ASCII
1414 e795 a1 ff                        CMP     #$FF
1415 e797 26 02                        BNE     NOTFF
1416 e799 a6 2d                        LDA     #$2D            REPLACE $FF WITH '-'
1417 e79b a4 7f                NOTFF   AND     #$7F            IGNORE BIT 7
1418 e79d 97                           TAX
1419 e79e d6 ed ae                     LDA     VTAB,X          CONVERT TO VFD CHARACTER SET
1420 e7a1 ad 09                        BSR     VFDL
1421 e7a3 a3 10                        CPX     #16
1422 e7a5 26 ea                        BNE     VFD3            LAST BYTE ?
1423
1424 e7a7 16 01                        BSET    3,PORTB         ENABLE HIGH
1425 e7a9 11 01                        BCLR    0,PORTB         CLOCK LOW ?
1426 e7ab 81                           RTS
1427
1428 e7ac ae 08                VFDL    LDX     #8
1429 e7ae 44                   DIS3    LSRA                    GET A BIT
1430 e7af 24 02                        BCC     DIS4
1431 e7b1 12 01                        BSET    1,PORTB         DATA HIGH
1432 e7b3 11 01                DIS4    BCLR    0,PORTB         CLOCK
1433 e7b5 10 01                        BSET    0,PORTB         IT
1434 e7b7 13 01                        BCLR    1,PORTB         CLEAR DATA
1435 e7b9 5a                           DECX                    COMPLETE ?
1436 e7ba 26 f2                        BNE     DIS3            NO
1437 e7bc ae 40                        LDX     #64
1438 e7be 5a                   DEL     DECX                    WAIT 200uS
1439 e7bf 26 fd                        BNE     DEL
1440 e7c1 be a7                        LDX     W7              RESTORE INDEX
1441 e7c3 5c                           INCX
1442 e7c4 81                           RTS
1443
1444 e7c5 a0 0f b0 00 80 00    INITF   FCB     $A0,$0F,$B0,$00,$80,$00,$90
     90
1445
1446                            ************************************************
1447                            *                                              *
1448                            *       Normal display (PS and time).          *
1449                            *                                              *
1450                            ************************************************
1451
1452 e7cc a6 20                NORMD   LDA     #$20
1453 e7ce b7 b1                        STA     DISP
1454 e7d0 b7 ba                        STA     DISP+9
1455 e7d2 b7 c0                        STA     DISP+15
1456 e7d4 a6 2e                        LDA     #$2E
1457 e7d6 03 cb 05                     BRCLR   1,STAT4,TYP1    DP TO INDICATE SLEEP TIMER RUNNING
1458 e7d9 05 99 02                     BRCLR   2,TH8,TYP1      FLASH IT
1459 e7dc b7 c0                        STA     DISP+15
1460
1461 e7de 5f                   TYP1    CLRX
1462 e7df e6 c1                MPS     LDA     PSN,X           GET PS NAME
1463 e7e1 e7 b2                        STA     DISP+1,X
1464 e7e3 5c                   SCNG    INCX
1465 e7e4 a3 07                        CPX     #7
1466 e7e6 23 f7                        BLS     MPS
1467
1468 e7e8 b6 9c                CJ      LDA     OUR             GET TIME
1469 e7ea cd eb 84                     JSR     CBCD
1470 e7ed a3 30                        CPX     #$30            LEADING ZERO ?
1471 e7ef 26 02                        BNE     TNZ
1472 e7f1 ae 20                        LDX     #$20            YES, MAKE IT A SPACE
1473 e7f3 bf bb                TNZ     STX     DISP+10
1474 e7f5 b7 bc                        STA     DISP+11
1475 e7f7 b6 9b                CMIN    LDA     MIN
1476 e7f9 cd eb 84                     JSR     CBCD
1477 e7fc bf be                        STX     DISP+13
1478 e7fe b7 bf                        STA     DISP+14
1479 e800 a6 20                CSEC    LDA     #$20
1480 e802 05 99 02                     BRCLR   2,TH8,DDC
1481 e805 a6 3a                        LDA     #$3A            0.5 Hz FLASHING COLON
1482 e807 b7 bd                DDC     STA     DISP+12
1483 e809 81                           RTS
1484
1485                            ************************************************
1486                            *                                              *
1487                            *       Clear display transient flags.         *
1488                            *                                              *
1489                            ************************************************
1490
1491 e80a 11 cb                CLTR    BCLR    0,STAT4         CLEAR DISPLAY TRANSIENT FLAG
1492 e80c 15 c9                        BCLR    2,STAT2         NOT RT DISPLAY
1493 e80e 3f af                        CLR     RTDIS           CLEAR RDS DISPLAY INDEX
1494 e810 17 cb                        BCLR    3,STAT4         NOT ALARM DISPLAY
1495 e812 1b cb                        BCLR    5,STAT4         NOT ALARM SET-UP
1496 e814 1f cb                        BCLR    7,STAT4         NOT RDS DISPLAYS
1497 e816 15 cb                        BCLR    2,STAT4         NOT SLEEP TIMER DISPLAY
1498 e818 81                           RTS
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1500                            ********************************************************
1501                            *                                                      *
1502                            *       PTY display.                                   *
1503                            *                                                      *
1504                            ********************************************************
1505
1506 e819 be 8e                PTYD    LDX     PTY             PTY
1507 e81b a3 10                        CPX     #16
1508 e81d 25 01                        BLO     XOK2
1509 e81f 5f                           CLRX
1510 e820 a6 10                XOK2    LDA     #16
1511 e822 42                           MUL
1512 e823 b7 a8                        STA     W8
1513 e825 3f a7                        CLR     W7
1514 e827 be a8                LCD3    LDX     W8
1515 e829 d6 ec ae                     LDA     PTYT.X
1516 e82c be a7                        LDX     W7
1517 e82e e7 b1                        STA     DISP.X          WAS MOD2
1518 e830 3c a8                        INC     W8
1519 e832 3c a7                        INC     W7
1520 e834 b6 a7                        LDA     W7
1521 e836 a1 10                        CMP     #16
1522 e838 25 ed                        BLO     LCD3
1523 e83a 81                           RTS
1524
1525                            ********************************************************
1526                            *                                                      *
1527                            *       RDS display.                                   *
1528                            *                                                      *
1529                            ********************************************************
1530
1531 e83b be a0                NXTC    LDX     DISP2
1532 e83d e6 ff                        LDA     RT-1.X          RT
1533 e83f a1 20                        CMP     #$20
1534 e841 26 13                        BNE     NOTSP           SPACE ?
1535 e843 0b c9 0c                     BRCLR   5,STAT2,FSP     YES. FIRST ONE ?
1536 e846 3c 9f                        INC     DISP1           NO. SKIP THIS ONE
1537 e848 3c a0                        INC     DISP2
1538 e84a b6 a0                RTDS    LDA     DISP2
1539 e84c a1 45                SKP1    CMP     #69
1540 e84e 22 18                        BHI     LCD4            END OF RT BUFFER
1541 e850 20 e9                        BRA     NXTC            NO. GET NEXT CHARACTER
1542
1543 e852 1a c9                FSP     BSET    5,STAT2         FIRST SPACE. SET FLAG
1544 e854 20 02                        BRA     CONT
1545 e856 1b c9                NOTSP   BCLR    5,STAT2         NOT A SPACE. CLEAR FLAG
1546 e858 b7 a8                CONT    STA     W8              SAVE NEW CHARACTER
1547 e85a 5f                           CLRX
1548 e85b e6 b2                ILP1    LDA     DISP+1.X        MOVE
1549 e85d e7 b1                        STA     DISP.X          REST
1550 e85f 5c                           INCX                    LEFT
1551 e860 a3 0f                        CPX     #15             ONE
1552 e862 26 f7                        BNE     ILP1            PLACE
1553 e864 b6 a8                        LDA     W8
1554 e866 b7 c0                        STA     DISP+15         ADD NEW CHAR. (WAS MOD2)
1555 e868 81                   LCD4    RTS
1556
1557
1558                            ********************************************************
1559                            *                                                      *
1560                            *       Standby display.                               *
1561                            *                                                      *
1562                            ********************************************************
1563
1564 e869 08 cb 4f              STBYD   BRSET   4,STAT4,ALRMA   ALARM ARMED ?
1565 e86c b6 73                        LDA     DOW             NO. GET DAY OF WEEK
1566 e86e 48                           LSLA
1567 e86f bb 73                        ADD     DOW
1568 e871 97                           TAX
1569 e872 d6 ec 72                     LDA     DNAME.X
1570 e875 b7 b1                        STA     DISP
1571 e877 d6 ec 73                     LDA     DNAME-1.X
1572 e87a b7 b2                        STA     DISP+1
1573 e87c d6 ec 74                     LDA     DNAME-2.X
1574 e87f b7 b3                        STA     DISP+2
1575 e881 a6 20                        LDA     #$20
1576 e883 b7 b4                        STA     DISP+3
1577 e885 b7 b7                        STA     DISP+6
1578 e887 b7 bb                        STA     DISP+10
1579 e889 b6 72                        LDA     DOM+1           DATE
1580 e88b ab 30                        ADD     #$30
1581 e88d b7 b6                        STA     DISP+5
1582 e88f b6 71                        LDA     DOM
1583 e891 27 02                        BEQ     ADD20           IF ZERO USE A SPACE
1584 e893 ab 10                        ADD     #$10            IF NOT MAKE ASCII
1585 e895 ab 20                ADD20   ADD     #$20
1586 e897 b7 b5                        STA     DISP+4
1587 e899 be 70                        LDX     MNTH+1          MONTH. LSD
1588 e89b b6 6f                        LDA     MNTH            MONTH. MSD
1589 e89d 27 04                        BEQ     MTHZ
1590 e89f 9f                           TXA
1591 e8a0 ab 0a                        ADD     #10
1592 e8a2 97                           TAX
1593 e8a3 bf a8                MTHZ    STX     W8
1594 e8a5 9f                           TXA
1595 e8a6 48                           LSLA
1596 e8a7 bb a8                        ADD     W8
1597 e8a9 97                           TAX
1598 e8aa d6 ec 87                     LDA     MNAME-3.X
1599 e8ad b7 b8                        STA     DISP+7
1600 e8af d6 ec 88                     LDA     MNAME-2.X
1601 e8b2 b7 b9                        STA     DISP+8
1602 e8b4 d6 ec 89                     LDA     MNAME-1.X
1603 e8b7 b7 ba                        STA     DISP+9
1604 e8b9 20 1d                        BRA     STIME
```

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1606                            ***************************************************
1607                            *                                                 *
1608                            *       Standby (alarm armed) display.            *
1609                            *                                                 *
1610                            ***************************************************
1611
1612 e8bb b6 9e          ALRMA   LDA     AOUR            GET ALARM HOURS
1613 e8bd cd eb 84              JSR     CBCD
1614 e8c0 bf b1                 STX     DISP
1615 e8c2 b7 b2                 STA     DISP+1
1616 e8c4 b6 9d                 LDA     AMIN
1617 e8c6 cd eb 84              JSR     CBCD
1618 e8c9 bf b3                 STX     DISP+2
1619 e8cb b7 b4                 STA     DISP+3
1620 e8cd 5f                    CLRX
1621 e8ce d6 eb f3      ALOP2   LDA     ALARMS+1,X
1622 e8d1 e7 b5                 STA     DISP+4,X
1623 e8d3 5c                    INCX
1624 e8d4 a3 06                 CPX     #6
1625 e8d6 23 f6                 BLS     ALOP2
1626 e8d8 b6 9c         STIME   LDA     OUR             GET TIME
1627 e8da cd eb 84              JSR     CBCD
1628 e8dd a3 30                 CPX     #$30            LEADING ZERO ?
1629 e8df 26 02                 BNE     TMZ
1630 e8e1 ae 20                 LDX     #$20            YES, MAKE IT A SPACE
1631 e8e3 bf bc         TMZ     STX     DISP+11
1632 e8e5 b7 bd                 STA     DISP+12
1633 e8e7 b6 9b                 LDA     MIN
1634 e8e9 cd eb 84              JSR     CBCD
1635 e8ec bf bf                 STX     DISP+14
1636 e8ee b7 c0                 STA     DISP+15
1637 e8f0 a6 20                 LDA     #$20
1638 e8f2 05 99 02              BRCLR   2,TH8,DTF       FLASH ?
1639 e8f5 a6 3a                 LDA     #$3A            0.5 Hz FLASHING COLON
1640 e8f7 b7 be         DTF     STA     DISP+13
1641 e8f9 81                    RTS
1642
1643                            ***************************************************
1644                            *                                                 *
1645                            *       PI display.                               *
1646                            *                                                 *
1647                            ***************************************************
1648
1649 e8fa 5f             DIPI   CLRX
1650 e8fb d6 ec 02       DLOP   LDA     PIST,X
1651 e8fe e7 b1                 STA     DISP,X
1652 e900 5c                    INCX
1653 e901 a3 0f                 CPX     #15
1654 e903 23 f6                 BLS     DLOP
1655 e905 b6 8f                 LDA     PI
1656 e907 27 10                 BEQ     PINV
1657 e909 cd eb 48              JSR     SPLIT
1658 e90c bf bc                 STX     DISP+11
1659 e90e b7 bd                 STA     DISP+12
1660 e910 b6 90                 LDA     PI+1
1661 e912 cd eb 48              JSR     SPLIT
1662 e915 bf be                 STX     DISP+13
1663 e917 b7 bf                 STA     DISP+14
1664 e919 81            PINV    RTS
1665
1666                            ***************************************************
1667                            *                                                 *
1668                            *       Alarm display.                            *
1669                            *                                                 *
1670                            ***************************************************
1671
1672 e91a 5f             ALRMD  CLRX                    YES
1673 e91b d6 eb f2       ALOP   LDA     ALARMS,X
1674 e91e e7 b1                 STA     DISP,X
1675 e920 5c                    INCX
1676 e921 a3 0f                 CPX     #15
1677 e923 23 f6                 BLS     ALOP
1678 e925 09 cb 31              BRCLR   4,STAT4,ALOF2   ALARM ARMED ?
1679 e928 a6 3a                 LDA     #$3A            YES
1680 e92a b7 bd                 STA     DISP+12
1681 e92c b6 9e                 LDA     AOUR            GET ALARM HOURS
1682 e92e cd eb 84              JSR     CBCD
1683 e931 a3 30                 CPX     #$30            LEADING ZERO ?
1684 e933 26 02                 BNE     TN3
1685 e935 ae 20                 LDX     #$20            YES, MAKE IT A SPACE
1686 e937 bf bb         TN3     STX     DISP+10
1687 e939 b7 bc                 STA     DISP+11
1688 e93b b6 9d                 LDA     AMIN
1689 e93d cd eb 84              JSR     CBCD
1690 e940 bf be                 STX     DISP+13
1691 e942 b7 bf                 STA     DISP+14
1692 e944 0b cb 12              BRCLR   5,STAT4,ALOF2   SET-UP ?
1693 e947 05 99 0f              BRCLR   2,TH8,ALOF2
1694 e94a a6 20                 LDA     #$20
1695 e94c 0c cb 06              BRSET   6,STAT4,FH      HOURS ?
1696 e94f b7 be                 STA     DISP+13         NO, FLASH MINUTES
1697 e951 b7 bf                 STA     DISP+14
1698 e953 20 04                 BRA     ALOF2
1699 e955 b7 bb         FH      STA     DISP+10         YES, FLASH HOURS
1700 e957 b7 bc                 STA     DISP+11
1701 e959 81            ALOF2   RTS
1702
1703                            ***************************************************
1704                            *                                                 *
1705                            *       TA & TP flags display.                    *
1706                            *                                                 *
1707                            ***************************************************
1708
1709 e95a 5f             DITAP  CLRX
1710 e95b d6 ec 12       BLOP   LDA     TAPST,X
1711 e95e e7 b1                 STA     DISP,X
1712 e960 5c                    INCX
1713 e961 a3 0f                 CPX     #15
1714 e963 23 f6                 BLS     BLOP
1715 e965 a6 31                 LDA     #$31
1716 e967 07 ca 02              BRCLR   3,STAT3,TPLOW   TP FLAG HIGH ?
1717 e96a b7 b7                 STA     DISP+6          YES, DISPLAY A 1
1718 e96c 05 ca 02      TPLOW   BRCLR   2,STAT3,TALOW   TA FLAG HIGH ?
1719 e96f b7 bf                 STA     DISP+14         YES, DISPLAY A 1
1720 e971 81            TALOW   RTS
```

```
                        ********************************************
                        *                                          *
                        *       PIN displays.                      *
                        *                                          *
                        ********************************************

e972 5f         DPIN1   CLRX
e973 d6 ec 22   PLOP    LDA     PINST1,X
e976 e7 b1              STA     DISP,X
e978 5c                 INCX
e979 a1 0f              CPX     #15
e97b 23 f6              BLS     PLOP
e97d b6 91              LDA     PIN
e97f 27 10              BEQ     PINNV
e981 cd eb 48           JSR     SPLIT
e984 bf bc              STX     DISP+11
e986 b7 bd              STA     DISP+12
e988 b6 92              LDA     PIN+1
e98a cd eb 48           JSR     SPLIT
e98d bf be              STX     DISP+13
e98f b7 bf              STA     DISP+14
e991 81         PINNV   RTS

e992 5f         DPIN2   CLRX
e993 d6 ec 32   PLOP2   LDA     PINST2,X
e996 e7 b1              STA     DISP,X
e998 5c                 INCX
e999 a1 0f              CPX     #15
e99b 23 f6              BLS     PLOP2
e99d b6 91              LDA     PIN             DATE
e99f 27 f0              BEQ     PINNV
e9a1 44                 LSRA
e9a2 44                 LSRA
e9a3 44                 LSRA
e9a4 cd eb 84           JSR     CBCD
e9a7 a3 30              CPX     #$30
e9a9 26 02              BNE     DTN0
e9ab ae 20              LDX     #$20
e9ad bf b3      DTN0    STX     DISP+2
e9af b7 b4              STA     DISP+3
e9b1 a3 31              CPX     #$31
e9b3 27 24              BEQ     NOTRD
e9b5 a1 31              CMP     #$31
e9b7 26 08              BNE     NOTST
e9b9 a6 73              LDA     #'s
e9bb b7 b5              STA     DISP+4
e9bd a6 74              LDA     #'t
e9bf b7 b6              STA     DISP+5
e9c1 a1 32      NOTST   CMP     #$32
e9c3 26 08              BNE     NOTNI
e9c5 a6 6e              LDA     #'n
e9c7 b7 b5              STA     DISP+4
e9c9 a6 64              LDA     #'d
e9cb b7 b6              STA     DISP+5
e9cd a1 33      NOTNI   CMP     #$33
e9cf 26 08              BNE     NOTRI
e9d1 a6 72              LDA     #'r
e9d3 b7 b5              STA     DISP+4
e9d5 a6 64              LDA     #'d
e9d7 b7 b6              STA     DISP+5
e9d9 b6 91      NOTRD   LDA     PIN             HOURS
e9db a4 07              AND     #7
e9dd be 92              LDX     PIN+1
e9df 58                 ASLX
e9e0 49                 ROLA
e9e1 58                 ASLX
e9e2 49                 ROLA
e9e3 cd eb 84           JSR     CBCD
e9e6 bf bb              STX     DISP+10
e9e8 b7 bc              STA     DISP+11
e9ea b6 92              LDA     PIN+1           MINUTES
e9ec a4 3f              AND     #$3F
e9ee cd eb 84           JSR     CBCD
e9f1 bf be              STX     DISP+13
e9f3 b7 bf              STA     DISP+14
e9f5 81                 RTS

                        ********************************************
                        *                                          *
                        *       MJD display.                       *
                        *                                          *
                        ********************************************

e9f6 ad 21      DMJD    BSR     SMJD
e9f8 b6 5d              LDA     MJD
e9fa 27 1c              BEQ     MJDNV
e9fc ab 30              ADD     #$30
e9fe b7 bb              STA     DISP+10
ea00 b6 5e              LDA     MJD+1
ea02 ab 30              ADD     #$30
ea04 b7 bc              STA     DISP+11
ea06 b6 5f              LDA     MJD+2
ea08 ab 30              ADD     #$30
ea0a b7 bd              STA     DISP+12
ea0c b6 60              LDA     MJD+3
ea0e ab 30              ADD     #$30
ea10 b7 be              STA     DISP+13
ea12 b6 61              LDA     MJD+4
ea14 ab 30              ADD     #$30
ea16 b7 bf              STA     DISP+14
ea18 81         MJDNV   RTS

ea19 5f         SMJD    CLRX
ea1a d6 ec 42   MLOP    LDA     MJDST,X
ea1d e7 b1              STA     DISP,X
ea1f 5c                 INCX
ea20 a3 0f              CPX     #15
ea22 23 f6              BLS     MLOP
ea24 81                 RTS
```

```
1832                            ************************************************
1833                            *                                              *
1834                            *       EON display.                           *
1835                            *                                              *
1836                            ************************************************
1837
1838 ea25 cd ea 19        DEON    JSR     SMJD            CLEAR FREQUENCY CHARACTERS
1839 ea28 b6 af                   LDA     RTDIS
1840 ea2a a0 08                   SUB     #8
1841 ea2c ae 10                   LDX     #16
1842 ea2e 42                      MUL
1843 ea2f 97                      TAX
1844 ea30 a6 20                   LDA     #$20
1845 ea32 b7 b9                   STA     DISP+8
1846 ea34 b7 ba                   STA     DISP+9
1847 ea36 d6 01 47                LDA     EON+2,X         DISPLAY PS (EON)
1848 ea39 b7 b1                   STA     DISP
1849 ea3b d6 01 48                LDA     EON+3,X
1850 ea3e b7 b2                   STA     DISP+1
1851 ea40 d6 01 49                LDA     EON+4,X
1852 ea43 b7 b3                   STA     DISP+2
1853 ea45 d6 01 4a                LDA     EON+5,X
1854 ea48 b7 b4                   STA     DISP+3
1855 ea4a d6 01 4b                LDA     EON+6,X
1856 ea4d b7 b5                   STA     DISP+4
1857 ea4f d6 01 4c                LDA     EON+7,X
1858 ea52 b7 b6                   STA     DISP+5
1859 ea54 d6 01 4d                LDA     EON+8,X
1860 ea57 b7 b7                   STA     DISP+6
1861 ea59 d6 01 4e                LDA     EON+9,X
1862 ea5c b7 b8                   STA     DISP+7
1863
1864 ea5e d6 01 52                LDA     EON+13,X
1865 ea61 a1 cd                   CMP     #205            FILLER ?
1866 ea63 26 04                   BNE     NFIL
1867 ea65 5c                      INCX
1868 ea66 d6 01 52                LDA     EON+13,X        YES, TRY AGAIN
1869 ea69 a1 fa           NFIL    CMP     #250            MEDIUM/LONG ?
1870 ea6b 27 43                   BEQ     MLWF
1871 ea6d a1 cc                   CMP     #204            NO, FREQUENCY OK ?
1872 ea6f 22 3e                   BHI     FNOK2
1873 ea71 ae 0a           FOK2    LDX     #10             VHF
1874 ea73 42                      MUL
1875 ea74 ab 2e                   ADD     #52E            CALCULATE FREQUENCY (BINARY)
1876 ea76 b7 a1                   STA     W1
1877 ea78 9f                      TXA
1878 ea79 a9 22                   ADC     #$22
1879 ea7b b7 a2                   STA     W2
1880 ea7d cd eb 1f                JSR     DCON2           CONVERT TO DECIMAL
1881
1882 ea80 b6 34           TYPE3   LDA     Q+4             DISPLAY VHF EON FREQUENCY
1883 ea82 26 02                   BNE     NZ1
1884 ea84 a6 f0                   LDA     #$F0
1885 ea86 ab 30           NZ1     ADD     #$30
1886 ea88 b7 bb                   STA     DISP+10
1887 ea8a 97                      TAX
1888 ea8b b6 35                   LDA     Q+5
1889 ea8d 26 06                   BNE     NZ2
1890 ea8f a3 20                   CPX     #$20
1891 ea91 26 02                   BNE     NZ2
1892 ea93 a6 f0                   LDA     #$F0
1893 ea95 ab 30           NZ2     ADD     #$30
1894 ea97 b7 bc                   STA     DISP+11
1895 ea99 b6 36                   LDA     Q+6
1896 ea9b ab 30                   ADD     #$30
1897 ea9d b7 bd                   STA     DISP+12
1898 ea9f a6 2e                   LDA     #$2E
1899 eaa1 b7 be                   STA     DISP+13
1900 eaa3 b6 37                   LDA     Q+7
1901 eaa5 ab 30                   ADD     #$30
1902 eaa7 b7 bf                   STA     DISP+14
1903 eaa9 b6 38                   LDA     Q+8
1904 eaab ab 30                   ADD     #$30
1905 eaad b7 c0                   STA     DISP+15
1906 eaaf 81              FNOK2   RTS
1907
1908 eab0 5c              MLWF    INCX                    DISPLAY M/L EON FREQUENCY
1909 eab1 d6 01 52                LDA     EON+13,X
1910 eab4 a1 0f                   CMP     #15
1911 eab6 23 02                   BLS     LONG
1912 eab8 ab 1b                   ADD     #27             MW OFFSET
1913 eaba ab 10           LONG    ADD     #16             M/L OFFSET
1914 eabc ae 09                   LDX     #9
1915 eabe 42                      MUL
1916 eabf bf a2                   STX     W2
1917 eac1 b7 a1                   STA     W1
1918 eac3 ad 5a                   BSR     DCON2           CONVERT TO BCD IN Q
1919 eac5 b6 35                   LDA     Q+5
1920 eac7 26 02                   BNE     NZ3             IF THOUSANDS OF kHz A ZERO
1921 eac9 a6 f0                   LDA     #$F0            DISPLAY AS A SPACE
1922 eacb ab 30           NZ3     ADD     #$30
1923 eacd b7 ba                   STA     DISP+9
1924 eacf b6 36                   LDA     Q+6
1925 ead1 ab 30                   ADD     #$30
1926 ead3 b7 bb                   STA     DISP+10
1927 ead5 b6 37                   LDA     Q+7
1928 ead7 ab 30                   ADD     #$30
1929 ead9 b7 bc                   STA     DISP+11
1930 eadb b6 38                   LDA     Q+8
1931 eadd ab 30                   ADD     #$30
1932 eadf b7 bd                   STA     DISP+12
1933 eae1 a6 6b                   LDA     #'k'
1934 eae3 b7 be                   STA     DISP+13
1935 eae5 a6 48                   LDA     #'H'
1936 eae7 b7 bf                   STA     DISP+14
1937 eae9 a6 7a                   LDA     #'z'
1938 eaeb b7 c0                   STA     DISP+15
1939 eaed 81                      RTS
```

```
                        ****************************************************
                        *                                                  *
                        *       Sleep display.                             *
                        *                                                  *
                        ****************************************************

eaee 5f                 SLEEPD  CLRX
eaef d6 ec 52           SLOP    LDA     SLPST,X
eaf2 e7 b1                      STA     DISP,X
eaf4 5c                         INCX
eaf5 a3 0f                      CPX     #15
eaf7 23 f6                      BLS     SLOP
eaf9 b6 78                      LDA     SLEPT
eafb cd eb 84                   JSR     CBCD
eafe bf b9                      STX     DISP+8
eb00 b7 ba                      STA     DISP+9
eb02 81                         RTS

                        ****************************************************
                        *                                                  *
                        *       M/S & DI display.                          *
                        *                                                  *
                        ****************************************************

eb03 5f                 DMSD    CLRX
eb04 d6 ec 62           ILOP    LDA     MSDST,X
eb07 e7 b1                      STA     DISP,X
eb09 5c                         INCX
eb0a a3 0f                      CPX     #15
eb0c 23 f6                      BLS     ILOP
eb0e 01 ca 04                   BRCLR   0,STAT3,MSM2    M/S FLAG SET
eb11 a6 4d                      LDA     #'M'            YES, MUSIC
eb13 b7 b7                      STA     DISP+6
eb15 b6 b0              MSM2    LDA     DI
eb17 cd eb 84                   JSR     CBCD
eb1a bf be                      STX     DISP+13
eb1c b7 bf                      STA     DISP+14
eb1e 81                         RTS

                        ****************************************************
                        *                                                  *
                        *       Convert binary to unpacked BCD in Q.       *
                        *                                                  *
                        ****************************************************

eb1f ae 54              DCON2   LDX     #R              CLEAR
eb21 bf ad                      STX     NUM1
eb23 cd ef 86                   JSR     CLRAS           RR
eb26 3c 5c                      INC     R+8             R <- 1
eb28 cd ef 84                   JSR     CLQ             CLEAR RQ
eb2b a6 0e                      LDA     #14             14 BITS TO CONVERT
eb2d b7 a6                      STA     W6
eb2f 34 a2              LOOP2   LSR     W2              MOVE OUT
eb31 36 a1                      ROR     W1              FIRST (LS) BIT
eb33 24 07                      BCC     NXT             ZERO
eb35 ae 30                      LDX     #Q              ONE, ADD
eb37 bf ae                      STX     NUM2            CURRENT VALUE
eb39 cd ee 33                   JSR     ADD             OF R
eb3c ae 54              NXT     LDX     #R              ADD R
eb3e bf ae                      STX     NUM2            TO
eb40 cd ee 33                   JSR     ADD             ITSELF
eb43 3a a6                      DEC     W6              ALL
eb45 26 e8                      BNE     LOOP2           DONE ?
eb47 81                         RTS

                        ****************************************************
                        *                                                  *
                        *       Split A nibbles into A (LS) and X (MS)     *
                        *       and convert to ASCII.                      *
                        *                                                  *
                        ****************************************************

eb48 97                 SPLIT   TAX                     MSD INTO X, LSD INTO A
eb49 99                         SEC
eb4a 56                         RORX
eb4b 99                         SEC
eb4c 56                         RORX
eb4d 54                         LSRX
eb4e 54                         LSRX
eb4f a3 39                      CPX     #$39            $30-$39 <- 0-9
eb51 23 07                      BLS     XOK
eb53 5c                         INCX
eb54 5c                         INCX
eb55 5c                         INCX
eb56 5c                         INCX
eb57 5c                         INCX
eb58 5c                         INCX
eb59 5c                         INCX
eb5a a4 0f              XOK     AND     #$0F            $41-$46 <- A-F
eb5c ab 30                      ADD     #$30
eb5e a1 39                      CMP     #$39
eb60 23 02                      BLS     AOK
eb62 ab 07                      ADD     #7
eb64 81                 AOK     RTS
```

```
2036                            ************************************************
2037                            *                                              *
2038                            *       Send and clock data to LCD module.     *
2039                            *                                              *
2040                            *       Check to see if LCD module is busy     *
2041                            *                                              *
2042                            ************************************************
2043
2044 eb65 b7 02                CLOCK   STA     PORTC
2045 eb67 18 03                        BSET    4,PORTD
2046 eb69 19 03                        BCLR    4,PORTD         CLOCK IT
2047 eb6b 81                           RTS
2048
2049 eb6c 15 03                WAIT    BCLR    2,PORTD
2050 eb6e 16 03                        BSET    3,PORTD         READ LCD MODULE BUSY FLAG
2051 eb70 19 03                        BCLR    4,PORTD
2052 eb72 3f 07                        CLR     PORTCD          INPUT ON PORTC
2053 eb74 18 03                WLOOP   BSET    4,PORTD         CLOCK HIGH
2054 eb76 b6 02                        LDA     PORTC           READ MODULE
2055 eb78 19 03                        BCLR    4,PORTD         CLOCK LOW
2056 eb7a b7 a7                        STA     W7
2057 eb7c 0e a7 f5                     BRSET   7,W7,WLOOP      BUSY ?
2058 eb7f 33 07                        COM     PORTCD          OUTPUT ON PORTC
2059 eb81 17 03                        BCLR    3,PORTD
2060 eb83 81                           RTS
2061
2062                            ************************************************
2063                            *                                              *
2064                            *       Hex->BCD conversion (& decimal adjust).*
2065                            *                                              *
2066                            ************************************************
2067
2068 eb84 ad 1c                CBCD    BSR     UPX
2069 eb86 ad 13                        BSR     ADJI            DECIMAL ADJUST
2070 eb88 b7 a7                BCD     STA     W7              SAVE
2071 eb8a ab 16                        ADD     #$16            ADD $16 (BCD 10)
2072 eb8c ad 08                        BSR     ADJU            ADJUST
2073 eb8e 5a                           DECX
2074 eb8f 2a f7                        BPL     BCD             TOO FAR ?
2075 eb91 b6 a7                        LDA     W7              YES. RESTORE A
2076 eb93 cc eb 48                     JMP     SPLIT
2077
2078 eb96 28 03                ADJU    BHCC    ADJI            OVERFLOW ?
2079 eb98 ab 06                        ADD     #6              YES
2080 eb9a 81                           RTS
2081
2082 eb9b ab 06                ADJI    ADD     #6              NO, BUT IS LS DIGIT
2083 eb9d 29 02                        BHCS    ARTS            BIGGER THAN 9 ?
2084 eb9f a0 06                        SUB     #6              NO. RESTORE
2085 eba1 81                   ARTS    RTS
2086
2087 eba2 97                   UPX     TAX
2088 eba3 54                           LSRX
2089 eba4 54                           LSRX
2090 eba5 54                           LSRX
2091 eba6 54                           LSRX                    MSB IN X
2092 eba7 a4 0f                        AND     #$0F            LSB IN A
2093 eba9 81                           RTS
2094
2095                            ************************************************
2096                            *                                              *
2097                            *       LCD initialisation.                    *
2098                            *                                              *
2099                            ************************************************
2100
2101 ebaa a6 a0                INITD   LDA     #$A0
2102 ebac c7 01 00                     STA     RT              SPACES BETWEEN PTY & RT
2103 ebaf c7 01 01                     STA     RT+1
2104 ebb2 c7 01 03                     STA     RT+3
2105 ebb5 c7 01 04                     STA     RT+4
2106 ebb8 a6 2d                        LDA     #$2D
2107 ebba c7 01 02                     STA     RT+2            DASH BETWEEN EXISTING DISPLAY & RT
2108 ebbd a6 20                        LDA     #$20            INITIALISE RADIOTEXT TO SPACES
2109 ebbf ae 05                        LDX     #5              AFTER CONF LOSS OR TEXT A/B CHANGE
2110 ebc1 d7 01 00             CLOP    STA     RT,X
2111 ebc4 5c                           INCX
2112 ebc5 a3 45                        CPX     #69
2113 ebc7 26 f8                        BNE     CLOP
2114 ebc9 3f 9f                        CLR     DISP1           INITIALISE SCROLLING POINTERS
2115 ebcb 3f a0                        CLR     DISP2
2116 ebcd 3f 8e                        CLR     PTY             CLEAR PTY
2117 ebcf 3f 91                        CLR     PIN             AND
2118 ebd1 3f 92                        CLR     PIN+1           PIN
2119 ebd3 3f b0                        CLR     DI              AND DI
2120 ebd5 11 ca                        BCLR    0,STAT3         AND M/S
2121 ebd7 17 ca                        BCLR    3,STAT3         CLEAR TP FLAG
2122 ebd9 15 c9                        BCLR    2,STAT2         CANCEL RT DISPLAY
2123
2124 ebdb 5f                           CLRX
2125 ebdc a6 2d                        LDA     #$2D
2126 ebde e7 c1                PLOP3   STA     PSN,X           CLEAR PS NAME
2127 ebe0 5c                           INCX
2128 ebe1 a3 08                        CPX     #8
2129 ebe3 26 f9                        BNE     PLOP3
2130 ebe5 81                           RTS
2131
2132 ebe6 5f                   CLRBDN  CLRX
2133 ebe7 a6 ff                        LDA     #$FF
2134 ebe9 d7 01 45             ELOP    STA     BDN,X           BDN RAM CLEAR
2135 ebec 5c                           INCX
2136 ebed a3 b0                        CPX     #176
2137 ebef 26 f8                        BNE     ELOP
2138 ebf1 81                           RTS
```

```
2140                            ;***************************************************
2141                            ;*                                                 *
2142                            ;*      Display strings.                           *
2143                            ;*                                                 *
2144                            ;***************************************************
2145
2146 ebf2 20 20 41 6c 61 72  ALARMS  FCC     ' Alarm - OFF '
     6d 20 2d 20 20 4f
     46 46 20 20
2147 ec02 20 50 49 20 63 6f  PIST   FCC       PI code -
     64 65 20 2d 20 20
     20 20 20 20
2148 ec12 20 54 50 20 2d 20  TAPST  FCC       TP - 0  TA - 0
     30 20 20 54 41 20
     2d 20 30 20
2149 ec22 20 50 49 4e 20 6e  PINST1 FCC       PIN no. -
     6f 2e 20 2d 20 20
     20 20 20 20
2150 ec32 20 20 20 20 20 74  PINST2 FCC          th at --:--
     20 61 74 20 2d 2d
     2e 2d 2d 20
2151 ec42 20 4d 4a 20 64 61  MJDST  FCC     ' MJ day -
     79 20 2d 20 20 20
     20 20 20 20
2152 ec52 20 53 6c 65 65 70  SLPST  FCC     ' Sleep   0 min.
     20 20 20 30 20 6d
     69 6e 2e 20
2153 ec62 20 4d 2f 53 20 20  MSDST  FCC     ' M/S  S   DI  0 '
     53 20 20 20 44 49
     20 20 30 20
2154
2155                            ;***************************************************
2156                            ;*                                                 *
2157                            ;*      MJD day and month strings.                 *
2158                            ;*                                                 *
2159                            ;***************************************************
2160
2161 ec72 4d 6f 6e 54 75 65  DNAME  FCC       MonTueWedThuFriSatSun
     57 65 64 54 68 75
     46 72 69 53 61 74
     53 75 6e
2162
2163 ec87 69 6e 76                  FCC       inv'
2164
2165 ec8a 4a 61 6e 46 65 62  MNAME  FCC       JanFebMarAprMayJunJulAugSepOctNovDec
     4d 61 72 41 70 72
     4d 61 79 4a 75 6e
     4a 75 6c 41 75 67
     53 65 70 4f 63 74
     4e 6f 76 44 65 63
2166
2167
2168                            ;***************************************************
2169                            ;*                                                 *
2170                            ;*      Programme Type (PTY) Codes.                *
2171                            ;*                                                 *
2172                            ;***************************************************
2173
2174 ecae 6e 6f 20 70 72 6f  PTYT   FCC       no program type     0
     67 72 61 6d 20 74
     79 70 65 20
2175 ecbe 20 20 20 20 20 20         FCC            News           1
     4e 65 77 73 20 20
     20 20 20 20
2176 ecce 43 75 72 72 65 6e         FCC       Current affairs     2
     74 20 61 66 66 61
     69 72 73 20
2177 ecde 20 20 49 6e 66 6f         FCC         Information       3
     72 6d 61 74 69 6f
     6e 20 20 20
2178 ecee 20 20 20 20 20 53         FCC           Sport           4
     70 6f 72 74 20 20
     20 20 20 20
2179 ecfe 20 20 20 45 64 75         FCC       Education           5
     63 61 74 69 6f 6e
     20 20 20 20
2180 ed0e 20 20 20 20 20 44         FCC           Drama           6
     72 61 6d 61 20 20
     20 20 20 20
2181 ed1e 20 20 20 20 43 75         FCC         Culture           7
     6c 74 75 72 65 20
     20 20 20 20
2182 ed2e 20 20 20 20 53 63         FCC         Science           8
     69 65 6e 63 65 20
     20 20 20 20
2183 ed3e 20 20 20 20 20 56         FCC          Varied           9
     61 72 69 65 64 20
     20 20 20 20
2184 ed4e 20 20 20 50 6f 70         FCC        Pop music          10
     20 6d 75 73 69 63
     20 20 20 20
2185 ed5e 20 20 20 52 6f 63         FCC       Rock music          11
     6b 20 6d 75 73 69
     63 20 20 20
2186 ed6e 20 45 61 73 79 20         FCC     Easy listening        12
     6c 69 73 74 65 6e
     69 6e 67 20
2187 ed7e 20 4c 69 67 68 74         FCC     Light classics        13
     20 63 6c 61 73 73
     69 63 73 20
2188 ed8e 53 65 72 69 6f 75         FCC    'Serious classics'     14
     73 20 63 6c 61 73
     73 69 63 73
2189 ed9e 20 20 4f 74 68 65         FCC       Other music         15
     72 20 6d 75 73 69
     63 20 20 20
```

```
2191                            ********************************************************
2192                            *                                                      *
2193                            *                  VFD character set.                  *
2194                            *                                                      *
2195                            *       Position in table is ASCII value.              *
2196                            *       Entry is the VFD character used.               *
2197                            *       Last column shows characters replaced          *
2198                            *       by spaces. $00 to $1F are ASCII control        *
2199                            *       characters and shouldn't occur.                *
2200                            *       : has been entered as -                        *
2201                            *       / has been entered as -                        *
2202                            *       ' has been entered as `                        *
2203                            *                                                      *
2204                            ********************************************************
2205
2206 edae 7e 7e 7e 7e          VTAB    FCB     $7E,$7E,$7E,$7E                 all
2207 edb2 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E                 all
2208 edb6 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E                 all
2209 edba 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E                 all
2210
2211 edbe 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E                 all
2212 edc2 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E                 all
2213 edc6 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E                 all
2214 edca 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E                 all
2215
2216 edce 7e 7b 7a 7e                  FCB     $7E,$7B,$7A,$7E       !  "  #
2217 edd2 7e 7e 7e 7a                  FCB     $7E,$7E,$7E,$7A       $  %  &  '        $%&
2218 edd6 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E       (  )  *  +        all
2219 edda 3f 7d 3e 7d                  FCB     $3F,$7D,$3E,$7D       ?  -  >  /
2220
2221 edde 00 01 02 03                  FCB     $00,$01,$02,$03       0  1  2  3
2222 ede2 04 05 06 07                  FCB     $04,$05,$06,$07       4  5  6  7
2223 ede6 08 09 7d 7e                  FCB     $08,$09,$7D,$7E       8  9  :  ;        :
2224 edea 7e 7e 7e 7c                  FCB     $7E,$7E,$7E,$7C       <  =  >  ?        <=>
2225
2226 edee 7e 0a 0b 0c                  FCB     $7E,$0A,$0B,$0C       @  A  B  C        @
2227 edf2 0d 0e 0f 10                  FCB     $0D,$0E,$0F,$10       D  E  F  G
2228 edf6 11 12 13 14                  FCB     $11,$12,$13,$14       H  I  J  K
2229 edfa 15 16 17 18                  FCB     $15,$16,$17,$18       L  M  N  O
2230
2231 edfe 19 1a 1b 1c                  FCB     $19,$1A,$1B,$1C       P  Q  R  S
2232 ee02 1d 1e 1f 20                  FCB     $1D,$1E,$1F,$20       T  U  V  W
2233 ee06 21 22 23 7e                  FCB     $21,$22,$23,$7E       X  Y  Z  [        [
2234 ee0a 7e 7e 7e 7d                  FCB     $7E,$7E,$7E,$7D       \  ]  ^  -        \]^
2235
2236 ee0e 7a 24 25 26                  FCB     $7A,$24,$25,$26          a  b  c
2237 ee12 27 28 29 2a                  FCB     $27,$28,$29,$2A       d  e  f  g
2238 ee16 2b 2c 2d 2e                  FCB     $2B,$2C,$2D,$2E       h  i  j  k
2239 ee1a 2f 30 31 32                  FCB     $2F,$30,$31,$32       l  m  n  o
2240
2241 ee1e 33 34 35 36                  FCB     $33,$34,$35,$36       p  q  r  s
2242 ee22 37 38 39 3a                  FCB     $37,$38,$39,$3A       t  u  v  w
2243 ee26 3b 3c 3d 7e                  FCB     $3B,$3C,$3D,$7E       x  y  z  {        {
2244 ee2a 7e 7e 7e 7e                  FCB     $7E,$7E,$7E,$7E       |  }  ~           all
2245
2246
2247                            ********************************************************
2248                            *                                                      *
2249                            *              MC68HC05E0 functions.                   *
2250                            *                                                      *
2251                            *       Add, Subtract, Multiply, Divide,               *
2252                            *       MJD -> day, date, month and year               *
2253                            *                                                      *
2254                            *       P. Topping              5th December '91       *
2255                            *                                                      *
2256                            *       Transfer of BCD numbers.                       *
2257                            *       (X) <- (NUM1), X preserved                     *
2258                            *                                                      *
2259                            ********************************************************
2260
2261 ee2e bf ae                  TRA     STX     NUM2            CLEAR DESTINATION
2262 ee30 cd ef 86                        JSR     CLRAS           AND ADD IT TO No. AT NUM1
2263
2264                            ********************************************************
2265                            *                                                      *
2266                            *       Addition of BCD numbers.                       *
2267                            *                                                      *
2268                            *       (X) <- (NUM1) + (NUM2), X preserved            *
2269                            *                                                      *
2270                            ********************************************************
2271
2272 ee33 3f ab                  ADD     CLR     CARRY
2273 ee35 bf a7                          STX     W7
2274 ee37 bf a5                  AD      STX     W5              ANSWER POINTER
2275 ee39 a6 09                          LDA     #N1
2276 ee3b b7 ac                          STA     COUNT
2277 ee3d be ad                          LDX     NUM1            1st No. POINTER
2278 ee3f bf a3                          STX     W3
2279 ee41 be ae                          LDX     NUM2            2nd No. POINTER
2280 ee43 bf a4                          STX     W4
2281 ee45 be a3                  LOOP    LDX     W3
2282 ee47 e6 08                          LDA     N1-1,X
2283 ee49 3a a3                          DEC     W3
2284 ee4b be a4                          LDX     W4
2285 ee4d eb 08                          ADD     N1-1,X          ADD
2286 ee4f 3a a4                          DEC     W4
2287 ee51 bb ab                          ADD     CARRY           SET ON ADDITION OVERFLOW
2288 ee53 3f ab                          CLR     CARRY           /A PUS. RESULT SUBTRACTION
2289 ee55 ad 11                          BSR     ADJ             DECIMAL ADJUST
2290 ee57 be a5                          LDX     W5
2291 ee59 e7 08                          STA     N1-1,X          SAVE ANSWER
2292 ee5b 3a a5                          DEC     W5
2293 ee5d 3a ac                          DEC     COUNT
2294 ee5f 26 e4                          BNE     LOOP            DONE ?
2295 ee61 be a7                          LDX     W7
2296 ee63 81                             RTS
2297
2298 ee64 a0 0a                  AJ      SUB     #10             YES, SUTRACT 10
2299 ee66 3c ab                          INC     CARRY           AND RECORD CARRY
2300 ee68 a1 0a                  ADJ     CMP     #10
2301 ee6a 24 f8                          BHS     AJ              10 OR MORE ?
2302 ee6c 81                             RTS                     NO
```

```
2304                    ********************************************************
2305                    *                                                      *
2306                    *       Subtraction, complementing and incre-          *
2307                    *       menting (X=REG-ND) of BCD numbers.             *
2308                    *                                                      *
2309                    *       (X) <- (NUM1) - (NUM2), X preserved.           *
2310                    *       (X and NUM2 should not be equal)               *
2311                    *                                                      *
2312                    ********************************************************
2313
2314 ee6d bf a6        SUB     STX     W6              ANSWER POINTER
2315 ee6f ad 06                BSR     COM2            9S COMP. SECOND NUMBER
2316 ee71 3f ab                CLR     CARRY           SET CARRY TO ONE
2317 ee73 1c ab                INC     CARRY           BEFORE ADDING
2318 ee75 ad c0                BSR     AD              ADD FIRST NUMBER
2319
2320 ee77 be ae        COM2    LDX     NUM2            9S COMPLIMENT
2321 ee79 ad 03                BSR     COMP            SECOND NUMBER
2322 ee7b be a6                LDX     W6              RESTORE ANSWER POINTER
2323 ee7d 81                   RTS
2324
2325 ee7e a6 09        COMP    LDA     #ND             9S COMPLIMENT
2326 ee80 b7 ac                STA     COUNT
2327 ee82 a6 09        LOOP3   LDA     #$09
2328 ee84 e0 08                SUB     ND-1,X
2329 ee86 e7 08                STA     ND-1,X
2330 ee88 5a                   DECX
2331 ee89 3a ac                DEC     COUNT
2332 ee8b 26 f5                BNE     LOOP3
2333 ee8d 81                   RTS
2334
2335 ee8e ad ee        COM10   BSR     COMP            NINES COMPLIMENT THEN
2336 ee90 a6 09        ADD1    LDA     #ND             ADD 1 FOR TENS COMPLIMENT
2337 ee92 b7 ac                STA     COUNT           ENTER WITH X = REG-ND
2338 ee94 6c 11        ADD2    INC     2+ND-1,X
2339 ee96 e6 11                LDA     2+ND-1,X
2340 ee98 a1 0a                CMP     #$0A
2341 ee9a 25 09                BLO     RETURN
2342 ee9c a0 0a                SUB     #10
2343 ee9e e7 11                STA     2+ND-1,X
2344 eea0 5a                   DECX
2345 eea1 3a ac                DEC     COUNT
2346 eea3 26 ef                BNE     ADD2
2347 eea5 81           RETURN  RTS
2348
2349                    ********************************************************
2350                    *                                                      *
2351                    *       Mult:  P <- P x (, overl  in TMP. X = #P.      *
2352                    *                                                      *
2353                    ********************************************************
2354
2355 eea6 ae 54        MULT    LDX     #R
2356 eea8 cd ef 86                JSR     CLRAS
2357 eeab ae 4b                 LDX     #TMP
2358 eead cd ef 86              JSR     CLRAS           CLEAR RESULT
2359 eeb0 ae 12                LDX     #2*ND
2360 eeb2 bf a6                STX     W6              INIT  P POINTER
2361 eeb4 ae 09                LDX     #ND
2362 eeb6 e6 41        STR     LDA     P+1,X
2363 eeb8 bf a1                STX     W1              SAVE P POINTER
2364 eeba b7 ab                STA     CARRY           SAVE P
2365 eebc ae 09                LDX     #ND             INIT  Q POINTER
2366 eebe e6 2f        MTT     LDA     Q-1,X
2367 eec0 b7 a4                STA     W4              SAVE Q
2368 eec2 27 3c                BEQ     TST             IF ZERO: GOTO NEXT Q
2369 eec4 b6 ab                LDA     CARRY           RECALL P
2370 eec6 b7 a3                STA     W3              SAVE P
2371 eec8 4f                   CLRA
2372 eec9 34 ab        PLY     LSR     CARRY           RIGHT SHIFT INTO P
2373 eecb 24 02                BCC     SHF             P = ZERO ?
2374 eecd 1b a4                ACC     W4              YES: A=A+Q
2375 eecf 3d ab        SHF     TST     CARRY           ZERO ?
2376 eed1 27 04                BEQ     C4              YES: FINISHED WITH THIS Q
2377 eed3 38 a4                ASL     W4              NO: LEFT SHIFT Q
2378 eed5 20 f2                BRA     PLY
2379 eed7 5a           C4      DECX                    X = X - 1
2380 eed8 bf a2                STX     W2              SAVE Q POINTER
2381 eeda be a6                LDX     W6              R POINTER
2382 eedc eb 4a                ADD     R+ND-1,X        ADD R TO A
2383 eede cd ee 68              JSR     ADJ             ADJUST
2384 eee1 e7 4a        C2      STA     R+ND-1,X        R = R + A
2385 eee3 b6 ab                LDA     CARRY
2386 eee5 eb 49                ADD     R+ND-2,X        ADD R+(ND+2) TO CARRY
2387 eee7 e7 49                STA     R+ND-2,X        R+(ND+2) = R+(ND+2) + CARRY
2388 eee9 b6 a3                LDA     W3              RECALL P
2389 eeeb b7 ab                STA     CARRY           SAVE IN CARRY
2390 eeed 5a                   DECX
2391 eeee bf a6                STX     W6              SAVE R POINTER
2392 eef0 be a2                LDX     W2              Q POINTER
2393 eef2 20 03                BRA     C3
2394 eef4 3a a6        T20     DEC     W6              DEC  R POINTER
2395 eef6 5a                   DECX                    DEC  Q POINTER
2396 eef7 26 c5        C3      BNE     MTT
2397 eef9 b6 a6                LDA     W6              R POINTER
2398 eefb ab 08                ADD     #ND-1
2399 eefd b7 a6                STA     W6              R = R + ND-1
2400 eeff be a1                LDX     W1
2401 ef01 5a                   DECX                    P = P - 1
2402 ef02 26 b2                BNE     STR             IF NOT ZERO: GOTO NEXT P
2403 ef04 ae 54                LDX     #R
2404 ef06 81                   RTS
```

```
2406                            ************************************************
2407                            *                                              *
2408                            *       Division of BCD numbers.               *
2409                            *                                              *
2410                            *       R <- P / Q, remainder in TMP.          *
2411                            *       on exit X = #R, TMQ used.              *
2412                            *                                              *
2413                            ************************************************
2414
2415 ef07 ae 54                 DIV     LDX     #R              CLEAR
2416 ef09 cd ef 86                      JSR     CLRAS           RESULT
2417 ef0c ae 42                        LDX     #P              TRANSFER
2418 ef0e bf ad                        STX     NUM1            P TO
2419 ef10 ae 4b                        LDX     #TMP            WORKING
2420 ef12 cd ee 2e                     JSR     TRA             P (TMP)
2421 ef15 ae 30                        LDX     #Q              TRANSFER
2422 ef17 bf ad                        STX     NUM1            Q TO
2423 ef19 ae 39                        LDX     #TMQ            WORKING
2424 ef1b cd ee 2e                     JSR     TRA             Q (TMQ)
2425
2426 ef1e a6 09                 POSS    LDA     #ND             NUMBER
2427 ef20 b7 ac                        STA     COUNT           DIGITS
2428 ef22 ae 39                 LOOP6   LDX     #TMQ            FIND LEAST SIGNIFICANT
2429 ef24 f6                           LDA     0,X             NON-ZERO DIGIT
2430 ef25 26 07                        BNE     NOSH            ZERO ?
2431 ef27 cd ef 64                     JSR     SHIFT           YES, SHIFT Q
2432 ef2a 26 f6                        BNE     LOOP6           UP ONE PLACE
2433 ef2c 20 33                 ZQ      BRA     RTRN            Q WAS ZERO
2434 ef2e b6 ac                 NOSH    LDA     COUNT           SAVE
2435 ef30 b7 a1                        STA     W1              No. DIDITS - No. SHIFTS
2436
2437 ef32 ae 4b                 SUBB    LDX     #TMP            SUBTRACT Q
2438 ef34 bf ad                        STX     NUM1            FROM
2439 ef36 cd ee 6d                     JSR     SUB             P
2440 ef39 b6 ab                        LDA     CARRY           TOO FAR ?
2441 ef3b 27 06                        BEQ     NEXTD           IF YES, GO TO NEXT DIGIT
2442 ef3d be a1                        LDX     W1              INCREMENT RELEVANT
2443 ef3f 6c 53                        INC     R-1,X           DIGIT IN RESULT
2444 ef41 20 ef                        BRA     SUBB            ONCE AGAIN
2445 ef43 ae 4b                 NEXTD   LDX     #TMP            TOO FAR, ADD
2446 ef45 cd ee 33                     JSR     ADD             Q BACK ON
2447 ef48 ae 39                 ROR     LDX     #TMQ            SET UP TO
2448 ef4a a6 08                        LDA     #ND-1           SHIFT BACK
2449 ef4c b7 ac                        STA     COUNT           WORKING Q
2450 ef4e e6 07                 RRR     LDA     ND-2,X          MOVE ALL
2451 ef50 e7 08                        STA     ND-1,X          DIGITS
2452 ef52 5a                           DECX                    DOWN
2453 ef53 3a ac                        DEC     COUNT           ONE PLACE
2454 ef55 26 f7                        BNE     RRR             DONE ?
2455 ef57 6f 08                        CLR     ND-1,X          CLEAR MS DIGIT
2456 ef59 3c a1                        INC     W1              INCREMENT POINTER
2457 ef5b b6 a1                        LDA     W1
2458 ef5d a1 0a                        CMP     #ND+1           FINISHED ?
2459 ef5f 26 d1                        BNE     SUBB            NO, NEXT DIGIT
2460 ef61 ae 54                 RTRN    LDX     #R
2461 ef63 81                           RTS
2462
2463                            ************************************************************
2464                            *                                                          *
2465                            *       Shift.                                             *
2466                            *                                                          *
2467                            ************************************************************
2468
2469 ef64 b7 a3                 SHIFT   STA     W3
2470 ef66 cd ef 79                      JSR     DR1             W1: MSD, W2: LSD
2471 ef69 be a1                        LDX     W1
2472 ef6b e6 01                 AGS     LDA     1,X             MOVE ALL DIGITS
2473 ef6d f7                           STA     0,X             UP ONE PLACE
2474 ef6e 5c                           INCX
2475 ef6f b3 a2                        CPX     W2
2476 ef71 26 f8                        BNE     AGS             DONE ?
2477 ef73 b6 a3                        LDA     W3              YES, RECOVER NEW DIGIT
2478 ef75 f7                           STA     0,X             AND PUT IT IN LSD
2479 ef76 3a ac                        DEC     COUNT
2480 ef78 81                           RTS
2481
2482 ef79 bf a1                 DR1     STX     W1              STORE POINTERS
2483 ef7b a6 08                        LDA     #ND-1           (USED IN DIGIT AND DQ)
2484 ef7d 5c                    AXL     INCX
2485 ef7e 4a                           DECA
2486 ef7f 26 fc                        BNE     AXL
2487 ef81 bf a2                        STX     W2
2488 ef83 81                           RTS
2489
2490                            ************************************************
2491                            *                                              *
2492                            *       Clear.                                 *
2493                            *                                              *
2494                            ************************************************
2495
2496 ef84 ae 30                 CLQ     LDX     #Q              CLEAR Q
2497 ef86 bf a5                 CLRAS   STX     W5
2498 ef88 a6 09                        LDA     #ND             CLEAR No. DIGITS
2499 ef8a b7 ac                        STA     COUNT           STARTING AT X
2500 ef8c 7f                    CR      CLR     0,X
2501 ef8d 5c                           INCX
2502 ef8e 3a ac                        DEC     COUNT
2503 ef90 26 fa                        BNE     CR              DONE ?
2504 ef92 be a5                        LDX     W5
2505 ef94 81                           RTS
```

```
2507                            ****************************************************************
2508                            *                                                              *
2509                            *       MJD - day of week and year.                            *
2510                            *                                                              *
2511                            *       DOW = (MJD+2)MOD7 (= WD-1)                  (DOW)      *
2512                            *       Y   = INT((MJD-15078.2)/3652500)             (YR)      *
2513                            *                                                              *
2514                            ****************************************************************
2515
2516 ef95 ae 5d                MJDC    LDX     #MJD
2517 ef97 bf ad                        STX     NUM1
2518 ef99 ae 42                        LDX     #P
2519 ef9b cd ee 2e                     JSR     TRA             P <- MTD
2520 ef9e ae 5d                        LDX     #MJD
2521 efa0 cd f0 83                     JSR     T10K            MJD <- MJD TIMES 10.000
2522
2523 efa3 ae 39                DOFFW   LDX     #P-ND
2524 efa5 cd ee 90                     JSR     ADD1            P <- MJD + 1
2525 efa8 ae 39                        LDX     #P-ND
2526 efaa cd ee 90                     JSR     ADD1            P <- MJD + 2
2527 efad ae 30                        LDX     #Q
2528 efaf cd ef 86                     JSR     CLRAS
2529 efb2 a6 07                        LDA     #7
2530 efb4 b7 38                        STA     Q+ND-1          Q <- 7
2531 efb6 cd ef 07                     JSR     DIV             R <- (MJD+2)/7
2532 efb9 b6 53                        LDA     TMP+ND-1        REMAINDER (WD-1) IN TMP
2533 efbb b7 73                        STA     DOW
2534
2535 efbd ae 5d                YEAR    LDX     #MJD
2536 efbf bf ad                        STX     NUM1
2537 efc1 ae 30                        LDX     #Q
2538 efc3 bf ae                        STX     NUM2
2539 efc5 cd f0 98                     JSR     TRCY            Q <- CY (150782000)
2540 efc8 ae 42                        LDX     #P
2541 efca cd ee 6d                     JSR     SUB             P <- 10K(MJD-15078.2)
2542 efcd cd f0 a3                     JSR     TRDY            Q <- 3652500
2543 efd0 cd ef 07                     JSR     DIV             R <- Y  ((MJD-15078.2)/365.25)
2544 efd3 bf ad                        STX     NUM1
2545 efd5 ae 66                        LDX     #YR
2546 efd7 cd ee 2e                     JSR     TRA             YR <- Y
2547
2548                            ****************************************************************
2549                            *                                                              *
2550                            *       MJD - month and day.                                   *
2551                            *                                                              *
2552                            *       M = INT(MJD-14956.1-INT(Y *365.25))/306001)      (P)   *
2553                            *       D = MJD-14956-INT(Y *365.25)-INT(M *30.6001) /Q(x10K))  *
2554                            *                                                              *
2555                            ****************************************************************
2556
2557 efda cd f0 6b             MONTH   JSR     INT             R <- 10K(INT(Y *365.25))
2558 efdd ae 5d                        LDX     #MJD
2559 efdf bf ad                        STX     NUM1
2560 efe1 ae 42                        LDX     #P
2561 efe3 bf ae                        STX     NUM2
2562 efe5 cd f0 b9                     JSR     TRD01           P <- 149561000
2563 efe8 ae 30                        LDX     #Q
2564 efea cd ee 6d                     JSR     SUB             Q <- 10K(MJD-14956.1)
2565 efed bf ad                        STX     NUM1
2566 efef ae 54                        LDX     #R
2567 eff1 bf ae                        STX     NUM2
2568 eff3 ae 42                        LDX     #P
2569 eff5 cd ee 6d                     JSR     SUB             P <- 10K(MJD-14956.1-INT(Y *365.25))
2570 eff8 cd f0 ae                     JSR     TRDM            Q <- 306001
2571 effb cd ef 07                     JSR     DIV             R <- M      ;  MJD-14956.1-INT(Y *365.25)  ;
2572 effe bf ad                        STX     NUM1                  INT (  ------------------------  )
2573 f000 ae 42                        LDX     #P                    '              306001           '
2574 f002 cd ee 2e                     JSR     TRA             P <- M
2575 f005 b6 49                        LDA     P+ND-2          SAVE M
2576 f007 b7 6f                        STA     MNTH
2577 f009 b6 4a                        LDA     P+ND-1
2578 f00b b7 70                        STA     MNTH+1
2579
2580 f00d cd f0 ae             DAY     JSR     TRDM            Q <- 306001
2581 f010 cd f0 77                     JSR     MULTI           R <- 10K(INT(M *30.6001))
2582 f013 bf ad                        STX     NUM1
2583 f015 ae 39                        LDX     #TMQ
2584 f017 cd ee 2e                     JSR     TRA             TMQ <- 10K(INT(M *30.6001))
2585 f01a cd f0 6b                     JSR     INT             R <- 10K(INT(Y *365.25))
2586 f01d bf ae                        STX     NUM2
2587 f01f ae 39                        LDX     #TMQ
2588 f021 bf ad                        STX     NUM1
2589 f023 cd ee 33                     JSR     ADD             TMQ <- 10K(INT(Y *365.25)+INT(M *30.6001))
2590 f026 bf ad                        STX     NUM1
2591 f028 ae 42                        LDX     #P
2592 f02a bf ae                        STX     NUM2
2593 f02c cd f0 b9                     JSR     TRD01           P <- 149561000
2594 f02f 3f 47                        CLR     P+ND-4          P <- 149560000
2595 f031 ae 54                        LDX     #R
2596 f033 cd ee 33                     JSR     ADD             R <- 10K(14956+INT(Y *365.25)+INT(M *30.6001))
2597 f036 bf ae                        STX     NUM2
2598 f038 ae 5d                        LDX     #MJD
2599 f03a bf ad                        STX     NUM1
2600 f03c ae 30                        LDX     #Q
2601 f03e cd ee 6d                     JSR     SUB             Q <- MJD-R (10K*DAY)
2602 f041 e6 04                        LDA     ND-5,X
2603 f043 b7 72                        STA     DAY+1           MJD-14956-INT(Y *365.25)-INT(M *30.6001)
2604 f045 e6 03                        LDA     ND-6,X
2605 f047 b7 71                        STA     DAY
```

```
                        ************************************************************
                        *                                                          *
                        *       MJD - final correction of year & month and subs.   *
                        *                                                          *
                        *       If M' = 14 or 15, then K = 1, else K = 0           *
                        *       Y = Y' + K                                         *
                        *       M = M' - 1 - K*12                                  *
                        *                                                          *
                        ************************************************************

f049 b6 6f              ADJU2   LDA     MNTH            MONTH, MSD
f04b 27 1b                      BEQ     KE02            0 ?
f04d b6 70                      LDA     MNTH+1          NO, M'= 10 THRU 15
f04f 27 11                      BEQ     KE01            0 ?
f051 a1 04                      CMP     #4              NO, M'= 11 THRU 15
f053 25 13                      BLO     KE02            LESS THAN 14
f055 ae 5d              KE1     LDX     #YR-ND          NO, M'= 14 OR 15, K=1
f057 cd ee 90                   JSR     ADD1            Y <- Y'+1
f05a 3f 6f                      CLR     MNTH            MONTH, MSD (-10)
f05c 3a 70                      DEC     MNTH+1          DEC. MONTH
f05e 3a 70                      DEC     MNTH+1          AND AGAIN (-2)
f060 20 06                      BRA     KE02            -12
f062 a6 0a              KE01    LDA     #10             M'= 10
f064 b7 70                      STA     MNTH+1          PUT 10 IN LSD
f066 3f 6f                      CLR     MNTH            CLEAR MSD
f068 3a 70              KE02    DEC     MNTH+1          9<-10, 1,2<-14,15, 3-8<-4-9, 10-12<-11-13
f06a 81                         RTS

f06b ae 66              INT     LDX     #YR
f06d bf ad                      STX     NUM1
f06f ae 42                      LDX     #P
f071 cd ee 2e                   JSR     TRA             P <- Y'
f074 cd f0 a3                   JSR     TRDY            Q <- 10K*365.25
f077 cd ee a6           MULTI   JSR     MULT            R <- 10K*Y'*365.25
f07a 3f 59                      CLR     R+ND-4
f07c 3f 5a                      CLR     R+ND-3
f07e 3f 5b                      CLR     R+ND-2
f080 3f 5c                      CLR     R+ND-1          R <- 10K(INT(Y'*365.25))
f082 81                         RTS

f083 9f                 T10K    TXA                     TIMES 10.000
f084 ab 05                      ADD     #ND-4
f086 b7 a1                      STA     W1
f088 e6 04              SLP     LDA     4,X
f08a f7                         STA     0,X
f08b 5c                         INCX
f08c b3 a1                      CPX     W1
f08e 26 f8                      BNE     SLP
f090 7f                         CLR     0,X
f091 6f 01                      CLR     1,X
f093 6f 02                      CLR     2,X
f095 6f 03                      CLR     3,X
f097 81                         RTS

                        ************************************************
                        *                                              *
                        *       MJD constants.                         *
                        *                                              *
                        ************************************************

f098 ae 09              TRCY    LDX     #ND
f09a d6 f0 c3           CYL     LDA     CY-1,X
f09d e7 2f                      STA     Q-1,X
f09f 5a                         DECX
f0a0 26 f8                      BNE     CYL
f0a2 81                         RTS

f0a3 ae 09              TRDY    LDX     #ND
f0a5 d6 f0 cc           DYL     LDA     DY-1,X
f0a8 e7 2f                      STA     Q-1,X
f0aa 5a                         DECX
f0ab 26 f8                      BNE     DYL
f0ad 81                         RTS

f0ae ae 09              TRDM    LDX     #ND
f0b0 d6 f0 de           DML     LDA     DM-1,X
f0b3 e7 2f                      STA     Q-1,X
f0b5 5a                         DECX
f0b6 26 f8                      BNE     DML
f0b8 81                         RTS

f0b9 ae 09              TRDO1   LDX     #ND
f0bb d6 f0 d5           DO1L    LDA     DO1-1,X
f0be e7 41                      STA     P-1,X
f0c0 5a                         DECX
f0c1 26 f8                      BNE     DO1L
f0c3 81                         RTS

f0c4 01 05 00 07 08 02  CY      FCB     1,5,0,7,8,2,0,0,0
     00 00 00
f0cd 00 00 03 06 05 02  DY      FCB     0,0,3,6,5,2,5,0,0
     05 00 00
f0d6 01 04 09 05 06 01  DO1     FCB     1,4,9,5,6,1,0,0,0
     00 00 00
f0df 00 00 00 03 00 06  DM      FCB     0,0,0,3,0,6,0,0,1
     00 00 01

                        ************************************************
                        *                                              *
                        *       Vectors.                               *
                        *                                              *
                        ************************************************

fff4                            ORG     $FFF4

fff4 e0 00                      FDB     START           SERIAL
fff6 e2 9d                      FDB     TINTR           TIMER B
fff8 e0 00                      FDB     START           TIMER A
fffa e3 0a                      FDB     SDATA           EXTERNAL INTERRUPT & RTI
fffc e0 00                      FDB     START           SWI
fffe e0 00                      FDB     START           RESET

                                END
```

68HC05K0 Infra-red Remote Control

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The MC68HC05K0 is a low cost, low pin count single chip microcomputer with 504 bytes of user ROM and 32 bytes of RAM. The MC68HC05K0 is a member of the 68HC05K series of devices which are available in 16-pin DIL or SOIC packages. It uses the same CPU as the other devices in the 68HC05 family and has the same instructions and registers. Additionally, the device has a 15-stage multi-function timer and 10 general purpose bi-directional I/0 lines. A mask option is available for software programmable pull-downs on all of the I/O pins and four of the pins are capable of generating interrupts.

The device is ideally suited for remote-control keyboard applications because the pull-downs and the interrupt drivers on the port pins allow keyboards to be built without any external components except the keys themselves. There is no need for external pull-up or pull-down resistors, or diodes for wired-OR interrupts, as these features are already designed into the device.

This application makes use of many of the device features to control an infra-red television remote control. The application could be very easily modified to control any device with a similar transmission protocol. It will run on any of the 'K' devices without modification.

Remote Control Specifications

The basic purpose of a television remote control is to transmit a control instruction to the television. The instruction is generated by a keystroke on the remote control keyboard. The detection and decoding of a key press and the transmission encoding is carried out by the remote control micro controller.

When a key on the remote control keypad is pressed, the micro controller must first determine what key is being pressed and generate an individual code for the key. The key code is then converted to a instruction code that is inserted into the transmission command which, using a defined protocol, is transmitted to the television receiver. The command is continually transmitted as long as the key is being held down.

As the remote control is battery powered it needs to use as little power as possible. This is achieved by entering STOP mode when no keys are being pressed and effectively switches off the device. The micro controller comes out of STOP mode upon receipt of an interrupt request that is generated when a key is pressed.

Remote Control Keyboard

The 68HC05K0 has ten general purpose I/O pins. One of these is used for the transmission signal output leaving nine pins for the keyboard control. Of these, four pins on PortA have internal interrupt request hardware. Using these four pins as inputs allows key presses to be detected without any external interrupt hardware. This leaves the five remaining pins for outputs.

Using the internal pull-down facility and the rising edge interrupt request on the four inputs permits interrupts to be generated. **If the five outputs are set to logic '1', so driving an input from logic '0' to logic '1' when a key is pressed, an interrupt request can be generated.** Using this arrangement a five by four keyboard matrix can be used. An extra four keys can be controlled if the Vdd line is used to drive one row of four keys to logic '1'. Therefore the maximum amount of keys controllable becomes twenty four.

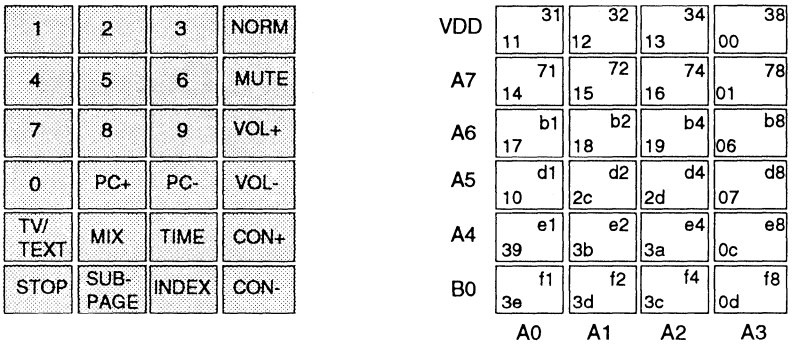


Figure 1 Keyboard layout with associated scanned and transmitted codes

A depressed key will set one of the input columns to logic '1'. By scanning the columns, and setting each row output to logic '0' and then checking if the inputs all become logic '0', the associated row for the key can be determined. If rotating the logic '0' through the five output pins fails to identify a key column, then the key must be connected to the Vdd line. This process gives an individual code for each key which is a combination of the code from the column inputs and the row outputs. This can then be decoded to an instruction that is inserted into the output signal for transmission.

Figure 1 shows the layout of the keyboard on the left and the scanned and transmitted codes on the right. The keyboard layout incorporates the various television controls plus controls for TELETEXT. On the left hand side the codes returned from scanning the keyboard are shown in the upper right-hand corner of each key and the code sent for transmission for that key instruction are shown in the bottom left-hand corner. The I/O pins for each row and column are also shown for each key.

Transmission Protocol

The transmission protocol in this application is that used by the MC144105 IR Remote Control Transmitter. It uses a binary coded 9-bit data word with the LSB being transmitted first. Each bit of the transmitted signal is in the form of a bi-phase pulse code modulated (PCM) signal, whose bit coding is shown in figure 2. For a transmitted '0' there is a 512µs pause followed by a 32kHz pulse train for 512µs. For a transmitted '1' there is 32kHz pulse train followed by a 512µs pause. This gives a bit time of 1024µs for all bits. This is shown as figure 2.

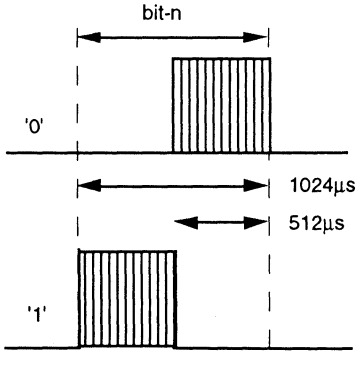


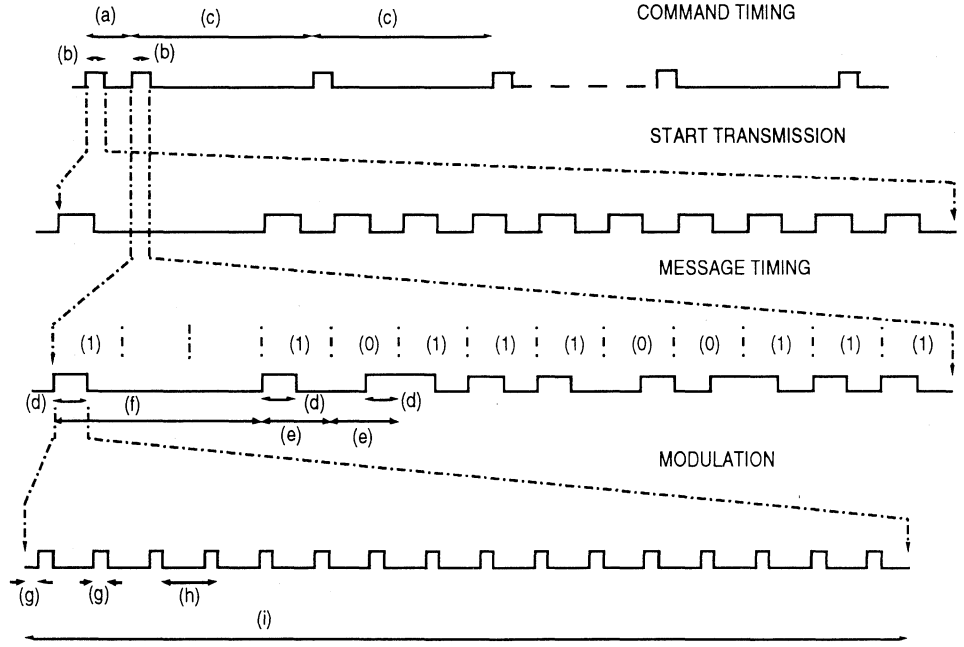
Figure 2 Bit coding of PCM signal

A complete transmission command consists of several messages. Each command begins with a start message of nine 1's followed by the message appropriate to the key pressed. This message is repeatedly transmitted until the key is released. The transmission is terminated after the key is released by a end message of nine 1's.

Every message consists of a pre-bit, a pre-bit pause, a start bit and nine data bits. The pre-bit and the start-bit are always logical '1'. The pre-bit allows for the set up of the automatic gain control in the receiving preamplifier. Figure 3 gives the exact timing relationships for the transmissions.

The command timing in figure 3 shows that after the start transmission the message is continually re-transmitted at intervals of 131ms (approximately 8Hz) until the key is released. This is shown as time (c). The control timing shows the nine bit instruction 111001110 being transmitted starting with the LSB. The pre-bit pause is equal to two bit periods and is followed by a start-bit of logical '1'. The pulse train is continuous during the transition between transmitting a logic '0' and a logic '1'. The modulating pulse train has a frequency of approximately 32kHz with a mark-to-space ratio of one to three.

The signal for transmission is output through one port pin and is used to drive an IR diode amplifier circuit.



Command timing	(a) = 32.8ms (b) = 13.3ms (c) = 131ms	start transmission start command control transmission	13 * bit time
Message timing	(d) = 512µs (e) = 1.024ms (f) = 3.072ms	(half-bit time) (bit time) (pre-pulse time)	$16/f_{carrier}$
Modulation	(g) = 8µs (h) = 32µs (i) = 512µs	$(1/f_{carrier})$ (half-bit time)	$16/f_{carrier}$

Figure 3 Circuit timing

Remote Control Operation

Figure 4 is a flow diagram showing the operation of the remote control on power-up or reset. After the initial set-up of the ports as inputs or outputs the remote control goes into STOP mode. It will remain in STOP mode as long as the device is not reset or a key is not pressed. When a key is pressed an interrupt request is generated. A short time delay makes sure that it is a true key press and not noise and also allows time for any switching effects on the inputs to pass prior to checking the inputs.

The keyboard is then read to find which key has been pressed and the code for the key is decoded into an instruction and transmitted to the television. If the key is held down the instruction is re-transmitted until the key is released. This is useful for the instructions which count through the television channels or adjust the volume, colour or brightness controls.

When the key is released a terminating instruction is sent to the receiver to inform it that the next message received is a separate instruction. This is useful in the case of a one time instruction like sending a channel number. In this example the receiver will tune to a channel only once; to tune to another channel the key must be released and a new instruction sequence received.

After terminating the transmission the ports are reset ready for the next key press and the processor returns to the STOP mode.

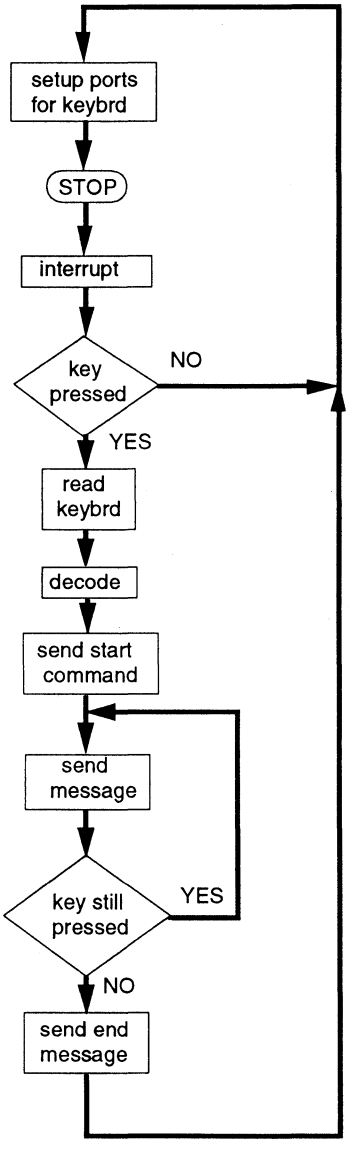


Figure 4 Flow diagram

Hardware

The remote control circuit is shown in figure 5. The hardware consists of the keyboard, the oscillator and the infra-red amplifier. The oscillator can be a crystal or a ceramic resonator with a frequency of 2MHz. The oscillator frequency is important since the transmission timing is based around a 1MHz internal clock frequency.

The infra-red amplifier uses two transistors and two standard diodes to limit the current through the IR diodes to approximately 1A. There is a need for a large capacitor close to the IR diodes because of the high switching current of the circuit.

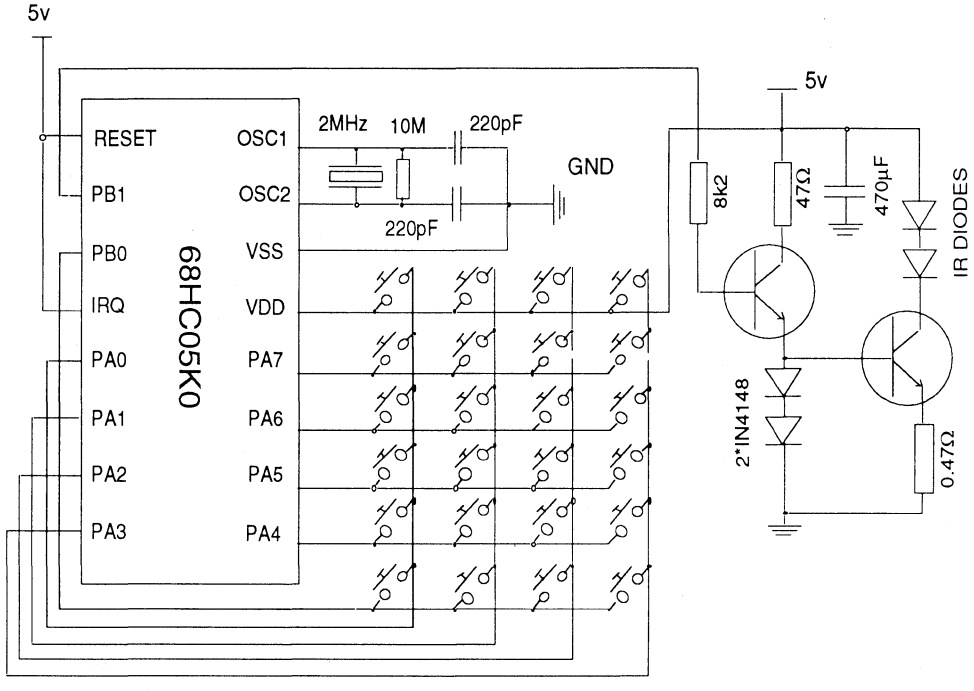


Figure 5 Infra-red remote control

Software

The listing of the remote control assembler code is contained at the end of this application note. The first section of the listing sets up the ports prior to going into STOP mode and waiting for a key to be pressed. PortA bits 0-3 are set up as inputs with the pull-downs enabled. Bits 4-7 are set up as outputs logic '1' as is PortB bit 0. PortB bit 1 is set-up as output logic '0' to switch off the IR amplifier before going into STOP mode.

The next section of code named 'presd' is the routine pointed to by the interrupt vector and is entered when a key is pressed. This routine first calls the keyboard scanning routine to determine which key has been pressed. It then calls the decoding routine to convert the code from the keyboard to a code that will be accepted by the television. The start message is then transmitted and is followed by the instruction message. There is then a check to see if the same key is still being pressed. If it is then the instruction message is re-transmitted until the key is released and the end message is transmitted.

As the transmission protocol requires nine data bits and only one byte instructions are being decoded a flag has to be set for the ninth bit of the transmission routine. For the start and end transmissions this flag is set to 1 to give the nine 1's message. For all instructions the ninth bit is 0 so the flag is cleared.

The decoding routine compares the code from the keyboard scan routine with data array 'keydat'. On a match it takes the corresponding element from the array 'tvdat' as the instruction code for transmission.

The values of the instruction codes shown in the right-hand side of figure 1 are specific for the receiver application. Each receiver using the same communications protocol will receive the same nine bit instruction but what the instruction does is dependent upon the receiver software. In this example the eight bit instruction '14' changes the channel to number four. In another receiver application the receiver may interpret the instruction code '14' as increase volume.

The transmission routine is entered with the instruction for transmission in 'keyst3'. After the pre-bit and the start-bit are transmitted the instruction byte is rotated (LSB first) into the carry flag. A logic '1' is sent for transmission if the flag is set after rotation and a logic '0' is sent for transmission if the flag is cleared. Each bit is transmitted as shown in figure 1. The routines 'send0' and 'send1' send a pause of 512µs followed by a 32kHz pulse train for 512µs and a 32kHz pulse train for 512µs followed by a 512µs pause respectively. In the situation when a '1' follows a '0' then a pulse train of 1024µs is required. To avoid breaks in this pulse train the 'send0' routine checks the next bit to be transmitted to see if a double length pulse train must be transmitted. The 'send1' routine then has to check that a double length pulse train has not been sent in the previous one and a half bit periods before sending a pulse train.

The routine 'burst' produces the 32kHz pulse train for a duration set by a count in the accumulator. As the instruction time for setting the PortB bit 1 pin high or low is five clock cycles then the minimum processor clock period is derived by dividing the minimum output state time, which is 8µs when the output is high, by the minimum number of clock cycles to change this state. This gives an internal clock period of 8µs/5 equalling 1.6µs. Adding a three cycle delay will require an internal clock period of 8µs/8 = 1µs, allowing a 2MHz oscillator to be used.

The code size is approximately 300 bytes, leaving memory space for more features to be added to the controller.

Debug

On applying power to the circuit the RESET vector will initialise the program counter at the beginning of the software. When examining the output at PortB bit 1 with an oscilloscope or logic analyser it should be noted that when trying to capture the signal by pressing a key the first signal out will be the start message of nine 1's. To capture the instruction the key should be held down and as the instruction will be continually re-transmitted then the capture can be initiated at this point.

Listing

```
0026                    ************************************************************
0027                    * INFRA RED REMOTE CONTROL FOR K0,K1                       *
0028                    ************************************************************
0029                    * WRITTEN BY A.BRESLIN    13.1.92                          *
0030                    ************************************************************
0031                    * THIS PROGRAM READS AND ENCODES A KEY FROM A 24 KEY KEYBOARD *
0032                    * TO A FORM OF BIPHASE PULSE CODE MODULATION (PCM) FOR INFRA  *
0033                    * RED TRANSMISSION. IT USES THE TRANSMISSION PROTOCOL OF THE  *
0034                    * MC144105 IR REMOTE CONTROL TRANSMITTER                      *
0035                    ************************************************************
0036
0037
0038 0000               porta   equ     00
0039 0001               portb   equ     01
0040 0004               ddra    equ     04
0041 0005               ddrb    equ     05
0042 0008               tcsr    equ     $08
0043 0010               papd    equ     $10
0044
0045 00e0                       org     $e0
0046
0047 00e0               keyst1  rmb     1               ; initial code from keyboard
0048 00e1               keyst2  rmb     1               ; keycode
0049 00e2               keyst3  rmb     1               ; code transmitted
0050 00e3               dflag   rmb     1               ; flag for last and 9th bits
0051
0052
0053                    ************************************************************
0054                    * THE PORTS ARE SET UP USING PORTA 0-3 AS INPUTS MAKING USE  *
0055                    * OF THE INTERNAL INTERUPT GENERATION ON THESE I/O LINES.    *
0056                    * STOP MODE IS ENTERED UNTIL A KEY IS PRESSED                *
0057                    ************************************************************
0058
0059 0200                       org     $200
0060
0061 0200 9a            start   cli
0062 0201 ad 04         wpres   bsr     setup
0063 0203 9c                    rsp
0064 0204 8e                    stop
0065 0205 20 fa                 bra     wpres
0066
0067 0207 a6 f0         setup   lda     #$f0            ; porta 0-3 inputs
0068 0209 b7 04                 sta     ddra            ; 4-7 as outputs
0069 020b b7 00                 sta     porta           ; set outputs high
0070 020d b7 10                 sta     papd            ; 0-3 pulldown
0071 020f a6 03                 lda     #$03            ; portb 0-1 outputs
0072 0211 b7 05                 sta     ddrb
0073 0213 a6 01                 lda     #$01            ; set portb 0 high
0074 0215 b7 01                 sta     portb
0075 0217 81                    rts
0076
0077
```

```
0078                    ************************************************************
0079                    * THE KEY READ IS DECODED FOR TRANSMISSION.                 *
0080                    * THE TRANSMISSION PROTOCOL REQUIRES A START MESSAGE OF 9   *
0081                    * ONES FOLLOWED BY THE KEYPRESSED CODE. THIS CODE IS       *
0082                    * CONTINUALLY RETRANSMITTED IF THE KEY IS HELD DOWN. AN END *
0083                    * CODE OF 9 ONES TERMINATES THE TRANSMISSION AND THE DEVICE *
0084                    * RETURNS TO STOP MODE.                                    *
0085                    ************************************************************
0086
0087 0218 ad 34        presd   bsr     keyscn          ; get key pressed
0088 021a b6 e1                lda     keyst2          ; save key to check
0089 021c b7 e0                sta     keyst1          ; if key held down
0090 021e ad 67                bsr     decode          ; decode key pressed
0091 0220 12 e3                bset    1,dflag         ; set nineth bit to 1
0092 0222 a6 ff                lda     #$ff            ; send start data
0093 0224 b7 e2                sta     keyst3          ; to transmission routine
0094 0226 ad 71                bsr     trnmit          ; nine one's
0095 0228 b6 e1        sndagn  lda     keyst2          ; send key press message
0096 022a b7 e2                sta     keyst3          ; byte
0097 022c 13 e3                bclr    1,dflag         ; set nineth bit to 0
0098 022e ad 69                bsr     trnmit
0099 0230 b6 00                lda     porta           ; check if key still pressed
0100 0232 a4 0f                and     #$0f            ; end if no key pressed
0101 0234 26 0f                bne     endtrn
0102 0236 ad 16                bsr     keyscn          ; else check if same
0103 0238 b6 e0                lda     keyst1          ; key pressed
0104 023a b1 e1                cmp     keyst2
0105 023c 26 07                bne     endtrn          ; end if not
0106 023e ae c8                ldx     #$c8            ; delay
0107 0240 5a            tloop   decx                    ; before next
0108 0241 26 fd                bne     tloop           ; transmission
0109 0243 20 e3                bra     sndagn
0110 0245 12 e3        endtrn  bset    1,dflag         ; send end message
0111 0247 a6 ff                lda     #$ff            ; of nine ones
0112 0249 b7 e2                sta     keyst3
0113 024b ad 4c                bsr     trnmit
0114 024d 80                   rti                     ; re-enter stop mode
0115
0116                    ************************************************************
0117                    * WHEN A KEY IS PRESSED THE DEVICE COMES OUT OF STOP MODE   *
0118                    * THE KEYBOARD IS SCANNED TO SEE WHICH KEY IS PRESSED       *
0119                    ************************************************************
0120
0121 024e cd 02 fc      keyscn  jsr     datwt           ; wait for debounce
0122 0251 b6 00                lda     porta           ; check if key press
0123 0253 b7 e0                sta     keyst1          ; store inputs
0124 0255 a4 0f                and     #$0f            ; mask outputs
0125 0257 27 a7                beq     start           ; stop if no key pressed
0126 0259 ae ef                ldx     #$ef            ; set one row low
0127 025b 9f            nxtrow  txa                     ; read ouput lines
0128 025c b4 e0                and     keyst1          ; combine with inputs
0129 025e b7 e1                sta     keyst2          ; store key code
0130 0260 bf 00                stx     porta           ; to find row which clears inputs
0131 0262 b6 00                lda     porta           ; check for inputs cleared
0132 0264 a4 0f                and     #$0f            ; mask outputs
0133 0266 27 1c                beq     gotit           ; zero in key-press row clears inputs
0134 0268 58                   lslx                    ; check if last row
0135 0269 5c                   incx                    ; set lsb to 1
0136 026a 24 02                bcc     tryb            ; try portb output if not porta
0137 026c 20 ed                bra     nxtrow          ; try next porta output row
0138
0139 026e b6 e0        tryb    lda     keyst1
0140 0270 b7 e1                sta     keyst2
0141 0272 ae f0                ldx     #$f0
0142 0274 bf 00                stx     porta           ; set all porta outputs high
0143 0276 11 01                bclr    0,portb         ; set portb 0 output low
0144 0278 b6 00                lda     porta           ; check for inputs cleared
0145 027a a4 0f                and     #$0f            ; mask outputs
0146 027c 27 06                beq     gotit           ; zero in key-press row clears inputs
0147 027e b6 e1                lda     keyst2          ;
0148 0280 a4 3f                and     #$3f            ; set individual code since last row
0149 0282 b7 e1                sta     keyst2          ; store code
0150 0284 10 01        gotit   bset    0,portb         ; set portb column high again
0151 0286 81                   rts
0152
```

```
0153                    ************************************************************
0154                    * THE DECODE ROUTINE USES TWO ARRAYS. IT COMPARES THE KEY    *
0155                    * VALUE WITH THE ARRAY KEYDAT AND WHEN A MATCH IS FOUND THE  *
0156                    * CORRESPONDING ELEMENT IN THE ARRAY TVDAT BECOMES THE       *
0157                    * TRANSMITTED CODE.                                          *
0158                    ************************************************************
0159
0160 0287 ae 18         decode  ldx     #$18            ; data array offset to zero
0161 0289 d6 03 02      nxtel   lda     keydat,x        ; look at each element of array
0162 028c b1 e1                 cmp     keyst2          ; compare with key read
0163 028e 27 03                 beq     match           ; decode if match
0164 0290 5a                    decx                    ; else try next element
0165 0291 26 f6                 bne     nxtel           ; norm if no match found
0166 0293 d6 03 1a      match   lda     tvdat,x         ; get key code
0167 0296 b7 e1                 sta     keyst2          ; store code to transmit
0168 0298 81                    rts
0169
0170                    ************************************************************
0171                    * THE TRANSMISSION PROTOCOL REQUIRES A PRE-BIT, A PRE-BIT    *
0172                    * PAUSE, A START BIT AND NINE DATA BITS, WHERE THE PRE-BIT   *
0173                    * AND THE START BIT ARE LOGIC '1'.                           *
0174                    ************************************************************
0175
0176 0299 10 e3         trnmit  bset    0,dflag         ; initialise for first bit
0177 029b ad 32                 bsr     send1           ; send pre-bit
0178 029d cd 02 fc              jsr     datwt           ; pre-bit pause
0179 02a0 cd 02 fc              jsr     datwt           ; equalling four half data periods
0180 02a3 cd 02 fc              jsr     datwt           ;
0181 02a6 cd 02 fc              jsr     datwt           ;
0182 02a9 ad 24                 bsr     send1           ; send start bit
0183 02ab ae 08                 ldx     #$08            ; transmit 8 data bits
0184 02ad 34 e2         nxtbit  lsr     keyst3          ; get next bit
0185 02af 25 04                 bcs     data1           ; send 1 if carry set
0186 02b1 ad 28                 bsr     send0           ; send 0 if carry clear
0187 02b3 20 02                 bra     bitsnt
0188 02b5 ad 18         data1   bsr     send1
0189 02b7 5a            bitsnt  decx                    ; countdown bits sent
0190 02b8 26 f3                 bne     nxtbit          ; send next bit if count not zero
0191 02ba 03 e3 04              brclr   1,dflag,send00  ; if flag set
0192 02bd ad 10                 bsr     send1           ; send 1 as nineth bit
0193 02bf 20 02                 bra     endend          ;
0194 02c1 ad 18         send00  bsr     send0           ; else send 0
0195 02c3 ae 18         endend  ldx     #$18
0196 02c5 ad 35         loopw   bsr     datwt           ; delay between successive
0197 02c7 ad 33                 bsr     datwt           ; transmissions
0198 02c9 ad 31                 bsr     datwt
0199 02cb 5a                    decx
0200 02cc 26 f7                 bne     loopw
0201 02ce 81                    rts
0202
0203
0204                    ************************************************************
0205                    * TO TRANSMIT A LOGIC '1' A 32kHz PULSE TRAIN FOR 512us IS   *
0206                    * FOLLOWED BY A 512us PAUSE.                                 *
0207                    ************************************************************
0208
0209 02cf 01 e3 04      send1   brclr   0,dflag,last0   ; check if last bit was zero
0210 02d2 a6 10                 lda     #$10            ; burst if last bit was 1
0211 02d4 ad 15                 bsr     burst           ; 32kHz pulse for 512us
0212 02d6 ad 24         last0   bsr     datwt           ; wait 512us
0213 02d8 10 e3                 bset    0,dflag         ; set flag as 1 sent
0214 02da 81                    rts
0215
```

```
0216                        ************************************************************
0217                        * TO TRANSMIT A LOGIC '0' A 512us PAUSE IS FOLLOWED BY A     *
0218                        * 32kHz PULSE TRAIN FOR 512us. IF A LOGIC '1' FOLLOWS A '0'  *
0219                        * THE 32kHz IS CONTINUED FOR 1024us TO AVOID A PROCESSING    *
0220                        * DELAY                                                      *
0221                        ************************************************************
0222
0223 02db ad 1f             send0   bsr     datwt           ; wait 512us
0224 02dd 00 e2 04                  brset   0,keyst3,next1  ; check if next bit is 1
0225 02e0 a6 10                     lda     #$10            ; single burst if 1
0226 02e2 20 02                     bra     datset          ; data set
0227 02e4 a6 20             next1   lda     #$20            ; double burst required
0228 02e6 ad 03             datset  bsr     burst           ; 32kHz pulse for 512us
0229 02e8 11 e3                     bclr    0,dflag         ; clear flag as 0 sent
0230 02ea 81                        rts
0231
0232                        ************************************************************
0233                        * THE 32kHz PULSE TRAIN HAS A MARK TO SPACE RATIO OF 1 TO 3  *
0234                        ************************************************************
0235
0236 02eb 13 01             burst   bclr    1,portb         ; portb 1 low
0237 02ed 21 fe                     brn     *
0238 02ef 12 01                     bset    1,portb         ; portb 1 high
0239 02f1 21 fe                     brn     *
0240 02f3 13 01                     bclr    1,portb         ; portb 1 low
0241 02f5 9d                        nop
0242 02f6 4a                        deca                    ; decrement count
0243 02f7 27 02                     beq     endbur          ; end of burst ?
0244 02f9 20 f0                     bra     burst
0245 02fb 81                endbur  rts
0246
0247
0248 02fc a6 52             datwt   lda     #$52            ; count
0249 02fe 4a                loop    deca                    ; to provide 512us delay
0250 02ff 26 fd                     bne     loop            ; after instruction times
0251 0301 81                        rts
0252
0253 0302 31 f1 e1 d1 b1 71 keydat  fcb     $31,$f1,$e1,$d1,$b1,$71
0254 0308 32 f2 e2 d2 b2 72         fcb     $32,$f2,$e2,$d2,$b2,$72
0255 030e 34 f4 e4 d4 b4 74         fcb     $34,$f4,$e4,$d4,$b4,$74
0256 0314 38 f8 e8 d8 b8 78         fcb     $38,$f8,$e8,$d8,$b8,$78
0257
0258 031a 11 3e 39 10 17 14 tvdat   fcb     $11,$3e,$39,$10,$17,$14
0259 0320 12 3d 3b 2c 18 15         fcb     $12,$3d,$3b,$2c,$18,$15
0260 0326 13 3c 3a 2d 19 16         fcb     $13,$3c,$3a,$2d,$19,$16
0261 032c 00 0d 0c 07 06 01         fcb     $00,$0d,$0c,$07,$06,$01
0262
0263
0264 0332 80                softin  rti
0265
0266 03fa                           org     $3fa
0267
0268 03fa 02 18                     fdb     presd           ; scan keybrd on int
0269 03fc 03 32                     fdb     softin          ; software interrupt
0270 03fe 02 00                     fdb     start           ; resett
```

Universal Input Voltage Range Power Supply for High Resolution Monitors with Multi-sync Capability

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ABSTRACT

This Application Note describes an easy to build, high performance, low cost 100W FLYBACK power supply, able to work on any mains supply from 85 Vac to 265 Vac, from 40 Hz to 100 Hz. It is automatically synchronised on the horizontal scanning frequency for minimum screen interference on a multi-sync colour monitor, thanks to the versatile, high performance, low cost current mode controller MC44602P2, associated with the state of the art switchmode power transistor MJH18010.

INTRODUCTION

The MC44602 has been specifically designed to drive high voltage bipolar transistors. Its 1A source and 1.5A sink capability, with all the protection features associated with flyback power supplies, make it ideal for this kind of application.

New multi-sync high resolution colour monitors have horizontal frequencies in the range of 31.5 kHz to 85 kHz. The switchmode power supply associated with these high resolution colour monitors must be synchronized to the horizontal frequency in order to reduce any EMI/RFI effects visible on the screen. An important feature for an off line power supply is that it can be automatically adapted to any mains voltage without any hardware adaptation.

SPECIFICATION

Universal input voltage: 85 Vac to 265 Vac, 40 Hz to 100 Hz

Output voltages:

135V	0.4A
87V	0.2A
25V	0.8A
16V	0.3A
6.3V	0.8A

Output power: 100W

Short circuit protection on all outputs

Overload protection

Minimum efficiency: 80% at full load

Line regulation: $\leq \pm$ 1%

Load regulation: $\leq \pm$ 1%

External synchronisation: from 31.5 kHz to 85 kHz

Low overall cost.

TOPOLOGY AND MODE OF OPERATION CHOICE

For multi output voltages at 100W output power, the best choice is the SINGLE ENDED FLYBACK TOPOLOGY. The best price/performance ratio is offered by a combination of a high performance current mode controller MC44602 and a MJH18010 switching planar power transistor.

Depending on timebase frequency and mains voltage, the power supply works in either a discontinuous or a continuous current mode. Continuous current mode is for low mains voltage, and discontinuous current mode is for high mains voltage and low power. The continuous current mode at low mains voltage lowers the peak current (I Peak) on the transistor and as a consequence lowers the V_{ce} sat, the I_{b1} and the losses. At high mains voltage the discontinuous current mode allows lower switch-on losses and lower stress on the high voltage output diode. When the output diode has to switch current, its losses are higher (Trr).

The losses on the output diode depend on its current during conduction and current during switching. In discontinuous current mode there is no current in the diode at switch on. In continuous current mode there is always current in the diode at switch on and the Trr of the diode (switching losses) depends on this current. To accommodate a wide range of applications, the frequency of operation will be between 31.5 kHz and 85 kHz.

The MC44602 has a separate synchronisation input which resets the oscillator when a 5V positive pulse is applied. Since the oscillator of the MC44602 is working at twice the output frequency, the power supply will be synchronised at half the horizontal scanning frequency resulting in less disturbance on the screen with the synchronisation occurring only every two lines. Another advantage is for the power transistor which results in fewer switching losses, as it works at half the scanning frequency. Switching losses are directly related to the switching frequency, since they are the same for each cycle. The higher the frequency, the greater the losses.

A zener limits the input voltage to 4.7V on the sync. input. (See figure 1.) The synchronisation transformer is a toroidal bifilar core which receives the pulses from the time base of the monitor. The sync. pulse will have 5V amplitude and about 2 µS width. The main noise source is the high di/dt occurring at switch off. The power supply works at half the scanning frequency, so the impact of that disturbance is divided by two.

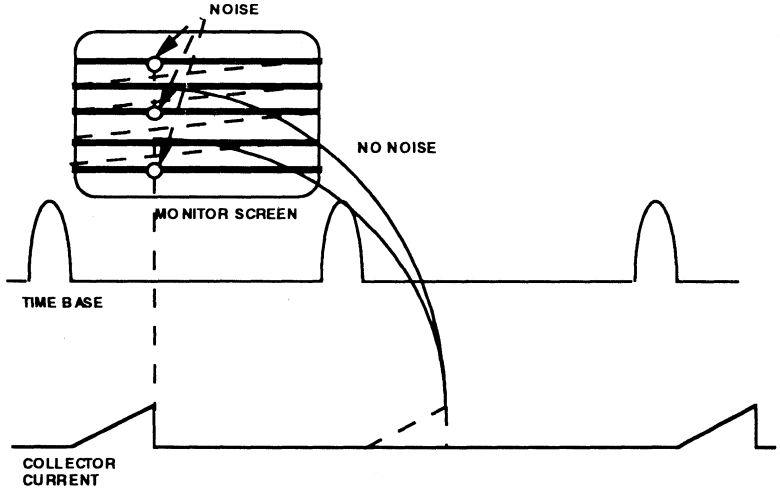


Figure 1 Switch off screen polution

TRANSFORMER DESIGN

Since the transformer plays one of the most important parts in the performance of a flyback power supply, due to coupling and leakage inductance, the transformer was designed around a SMT47 multislots former and a B3 GETV 53.18.18. ferrite core from THOMSON OREGA.

The feedback from the output voltage is magnetically realised by the auxiliary winding which performs good load, line and cross regulation, without the need for an optocoupler.

This auxiliary winding has three main functions (see MC44602 data sheet):

Self supply of the MC44602

Image of output voltage for regulation

Image of output voltage for overload detection.

Since the power supply will work from 85Vac to 265Vac, the minimum rectified voltage U is $85\sqrt{2}=120V$.

To provide a safety margin in worst case conditions (low mains-high power), let us choose a minimum DC voltage U of 90V.

The maximum DC voltage is $265\sqrt{2}=375V$.

Assuming an 80% efficiency with an output power of 100 W, the input power P_{in} is 100/0.8=125W.

The maximum primary current occurs at minimum voltage U and minimum switching frequency Fs which is 31.5 kHz/2 = 15.25 kHz.

The transformer must be calculated for 15 kHz minimum frequency.

Let us choose a maximum duty cycle of D= 0.4 for a minimum mains voltage, a minimum switching frequency and maximum power. Then I_p, the peak current in the transistor, becomes:

$$I_p = 2P_{in}/U*D = 2*125/90*0.4 = 7A$$

$$L_p = 2P_{in}/Ip^2*Fs = 2*125/49*15*10^3 = 340\mu H$$

A ferrite material with AL=460 nH/T can be chosen. The number of primary turns is:

$$Np = \sqrt{L_p/AL} = \sqrt{340*10^{-6}/460*10^{-9}} = 27 \text{ Turns}$$

TRANSFORMER CONSTRUCTION

The technique used is the multi slot developed and widely used by OREGA THOMSON. Figures 2 and 3 depict the way to couple the different windings in order to achieve a high coupling; this ensures an acceptable magnetic feedback signal and a low leakage inductance.

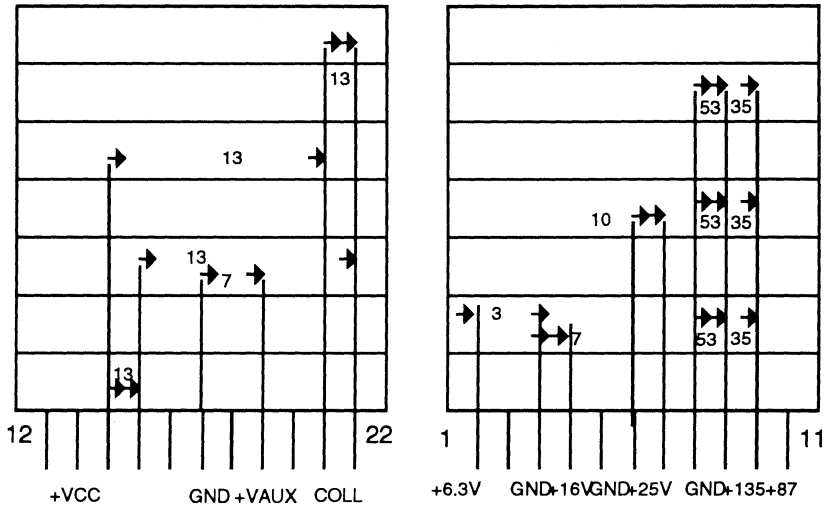


Figure 2 Multi slot winding

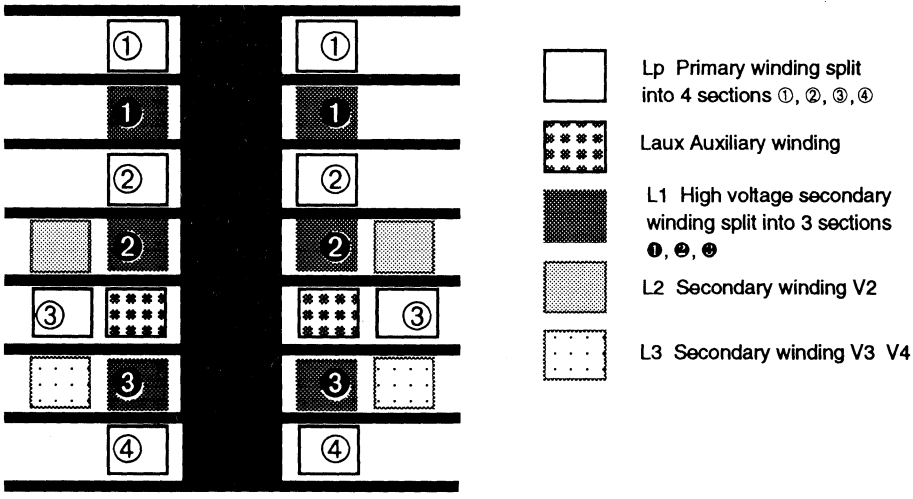


Figure 3 Physical winding position

For multislot construction we chose 2*13 Turns =26 Turns

Ns 135V	=Np*(1-D)*(Vs+Vf)/Vin min *D =26*0.6*136/100*0.4 = 53 turns =2.5V/Turn
Np=26T	0.5mm diameter
Ns 135V=53T	0.315mm diameter
Ns 87V=35T	0.5mm diameter
Ns 25V=10T	0.5mm diameter
Ns 16V= 7T	0.5mm diameter
Ns6.3V= 3T	0.5mm diameter
N V_{aux} =7T	0.5mm diameter

All wires are enamelled grade 2

Leakage inductance < 2%

SEMICONDUCTOR SELECTION

THE CONTROLLER

The MC44602 high performance, fixed frequency, current mode controller is the heart of the flyback power supply.

This circuit, specially designed for off-line and high voltage DC-DC converter applications with bipolar transistors, offers:

- Separate high current source and sink outputs
- Unique overload and short circuit protection
- Thermal protection
- Oscillator with sync input
- Current mode operation to 500 kHz output switching frequency
- Output dead time adjustment
- Automatic feed-forward compensation
- Latching PWM for cycle by cycle current limiting
- Input and reference undervoltage lockouts with hysteresis
- Low start-up and operating current

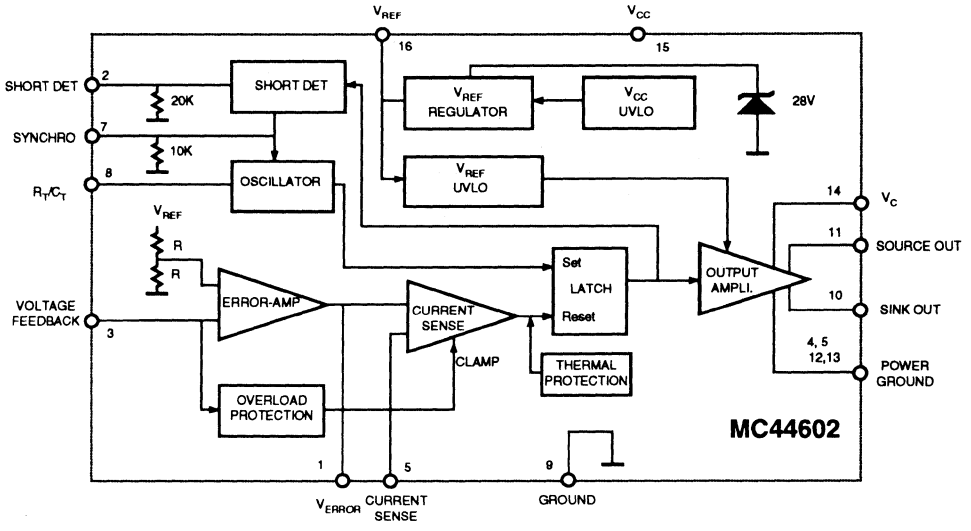


Figure 4 Simplified block diagram

THE SWITCHING TRANSISTOR

With a peak current of 7A, the state-of-the-art planar switchmode bipolar power transistor MJH18010 is a good choice.

On control: its power gain of 10 at 7A needs an I_b current of only 0.7A.

With I_{b1} = 0.7A, the base resistor R6= (V_{aux}-V_{sat} MC44602 -V_Z -$V_{be\ on}$ - V_{pin5})/I_{b1}.

V_{pin5}=R9*$I_{peak\ max}$.

R6 = (16V-2V-4.7V-0.7v-1.5V)/0.7A =10Ω

Off control: for reverse base current I_{b2}, a zener limits the reverse voltage to 4.7V, and the 2.2 µH L2 inductor limits the di/dt of reverse current to avoid I_c current crowding during T_{off}.

A clamping circuit is added on the collector of the power transistor to limit the peak voltage and stress during the RBSOA.

The maximum collector voltage is: V_{coll} = U+(V_{out}/N)

N=Np/Ns =0.5

For V_{out} = 135V, V_{coll}= 375+(135/0.5) = 645V

The snubbing capacitor of 330pF limits the dv/dt of the transistor at switch off; see ANE424 and AN1080.

THE OUTPUT DIODES

Since the power supply can work in continuous current mode, the output diodes need to be ULTRAFAST diodes thanks to their low TRR.

For 135V output, maximum reverse voltage is V_{out} +(max $V_{cc/n}$) n=Ns/Np

135+(375/0.5)=885V + ripple. The diode is a MUR4100E.

For 87V output, maximum reverse voltage is 87+(375/0.75)=587V. The diode is a MUR460.

For 25V out the diode is a MUR420.

For 16V out the diode is a 1N4934.

For 6.3V the diode is a MUR415.

SCHEMATIC DIAGRAM

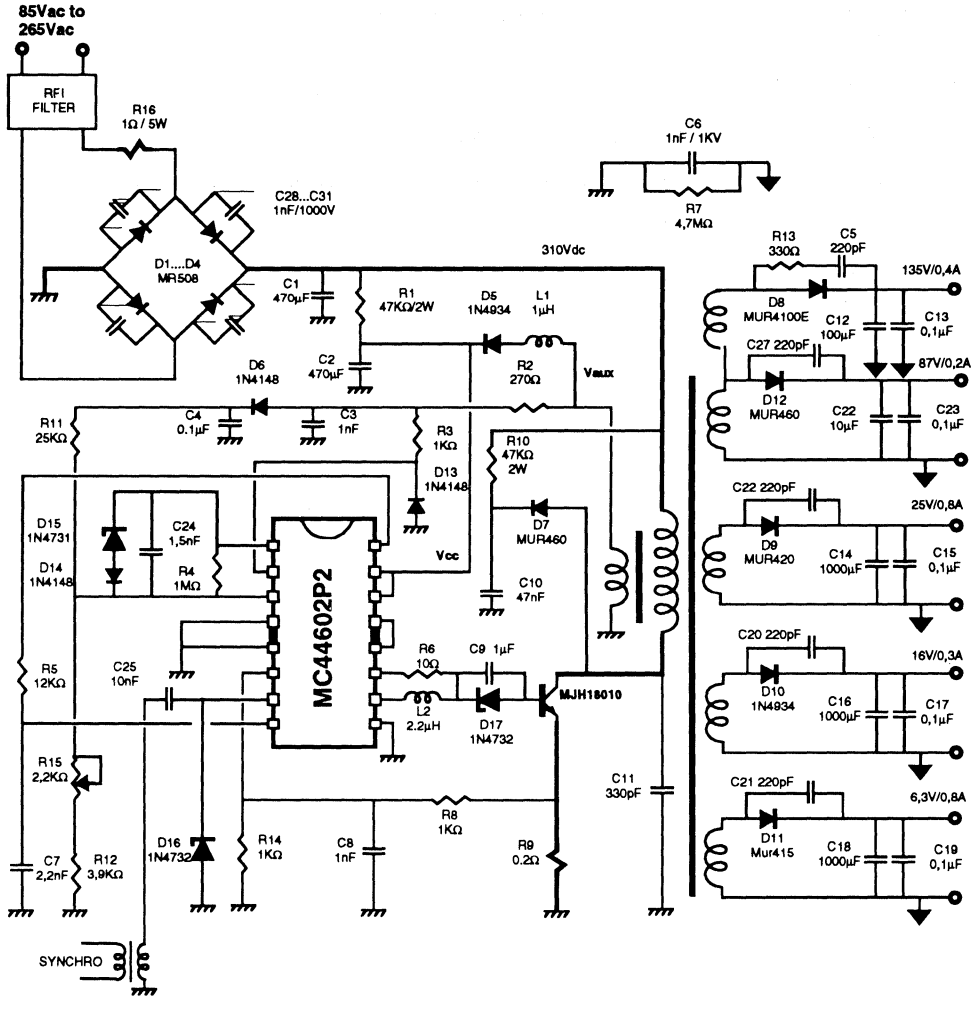


Figure 5 100W power supply schematic

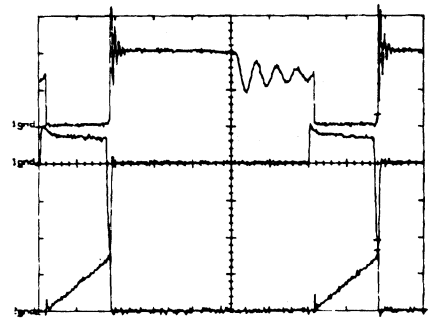
PERFORMANCE

Test	Conditions	Results 31.5 KHz to 85 KHz
Line Reg	V_{in} = 85Vac to 265Vac	
135V	I_{out} = 0.4A	Δ= 0.3V or +/-0.15%
87V	I_{out} = 0.2A	Δ= 0.1V or +/- 0.1%
25V	I_{out} = 0.8A	Δ= 0.15V or +/-0.3%
16V	I_{out} = 0.3A	Δ= 0V
6.3V	I_{out} = 0.8A	Δ = 0V
Load Reg	V_{in} = 110Vac	
	V_{in} = 220Vac	
135V	I_{out} = 0.2A to 0.4A	Δ= 2V or +/- 0.75%
Ripple	I_{out} = 0.4A	
135 V	V_{in} = 85Vac	1V (31 KHz) 0.4V(85 KHz)
	V_{in} = 85Vac	0.3V (50 Hz)
	V_{in} = 265Vac	1V (31 KHz) 0.3V (85 KHz)
	V_{in} = 265Vac	0V (50 Hz)
Efficiency	V_{in} = 110Vac/220Vac P_{out} = 100W	80%
Stand-by Mode		
P input	V_{in} = 90Vac, P_{out} = 0W	2.5 W
P input	V_{in} = 220Vac, P_{out} = 0W	5.5 W
Output short circuit	Safe on all outputs	

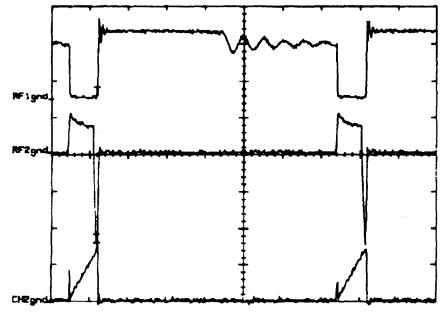
LIST OF SEMICONDUCTORS

Integrated Circuit	MC44602P2	1
Transistor	MJH18010	1
Diodes	MR508	4
	1N4934	2
	1N4732	2
	MUR460	2
	MUR4100E	1
	MUR420	2
	MUR415	1
	1N4148	3
	1N4731	1

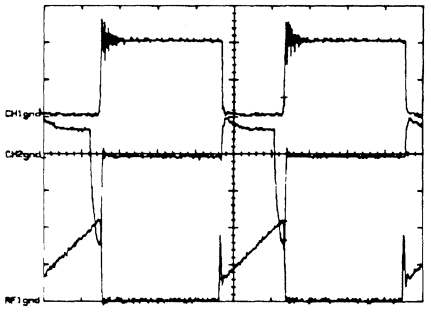
OSCILLOGRAMS



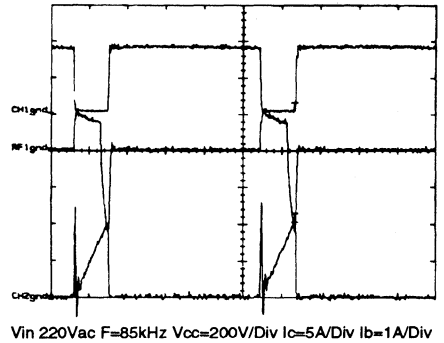
Vin 110Vac F=31.5kHz Vcc=100V/Div Ic=5A/Div Ib=1A/Div



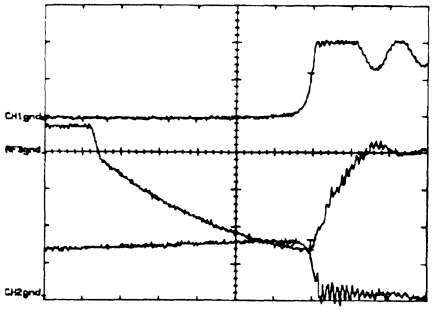
Vin 220Vac F=31.5kHz Vcc=200V/Div Ic=5A/Div Ib=1A/Div



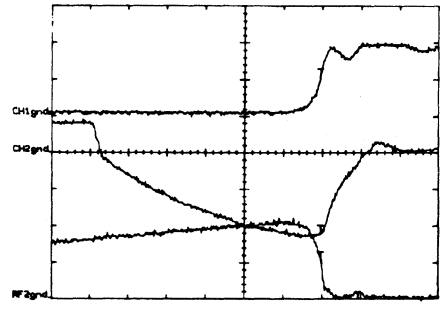
Vin 110V F=85kHz Vcc=100V/Div Ic=5A/Div Ib=1A/Div



Vin 220Vac F=85kHz Vcc=200V/Div Ic=5A/Div Ib=1A/Div



Vin 220Vac F=31.5kHz Vcc=200V/Div Ic=2A/Div Ib=1A/Div



Vin 220Vac F=85kHz Vcc=200V/Div Ic=2A/Div Ib=1A/Div

Figure 6 Typical results obtained

CONCLUSION

This paper demonstrates that the use of the new current mode controller is an easy way to realise a high performance, low cost, universal input, voltage range power supply with multisync capability.

The regulation performance can be improved at extra cost by using an optocoupler and a TL431 voltage reference in the feedback loop.

This power supply can be adapted to other output voltages by changing the transformer.

REFERENCES

AN1080/D Application note

MC44602 Data sheet

MJH18010 Data sheet

ANE424/D Application note

AN749

Broadband Transformers and Power Combining Techniques for RF

Prepared by:
H. Granberg
RF Circuits Engineering

This Application Note discusses broadband transformers for RF power applications. Practical examples are given with performance data and power combining techniques are discussed in detail.

BROADBAND TRANSFORMERS AND POWER COMBINING TECHNIQUES FOR RF

INTRODUCTION

The following discussion focuses on broadband transformers for RF power applications with practical examples of various types given with performance data. Detailed design formula are available in the Reference section. Power combining techniques useful in designing high power amplifiers are discussed in detail.

BROADBAND TRANSFORMERS

The input and output transformers are among the most critical components in the design of a multi-octave amplifier. The total performance of the amplifier (linearity, efficiency, VSWR, gain flatness) will depend on their quality. Transformers with high impedance ratios and for low impedances are more difficult to design in general. In the transmission line transformers very low line impedances are required, which makes them impractical for higher than 16:1 impedance ratios in a 50-Ohm system. Other type transformers require tight coupling coefficients between the primary and secondary, or excessive leakage inductances will reduce the effective bandwidth. Twisted line transformers (Figure 1C, D, F, G) are described in References 1, 2, and 4. Experiments have shown that the dielectric losses in certain types of magnet wire, employed for the twisted lines, can limit the power handling capability of such transformers. This appears as heat generated within the transformer at higher frequencies, although part of this may be caused by the losses in the magnetic core employed to improve the low frequency response. At low frequencies, magnetic coupling between the primary and secondary is predominant. At higher frequencies the leakage inductance increases and the permeability of the magnetic material decreases, limiting the bandwidth unless tight capacitive coupling is provided. In a transmission line transformer this coupling can be clearly defined in the form of a line impedance.

The required minimum inductance on the low impedance side is:

$$L = \frac{4\,R}{2\pi f}$$

where L = Inductance in μH
R = Impedance in Ohms
f = Frequency in MHz

This applies to all transformers described here.

Some transformers, which exhibit good broad band performance and are easy to duplicate are shown in Figure 1.

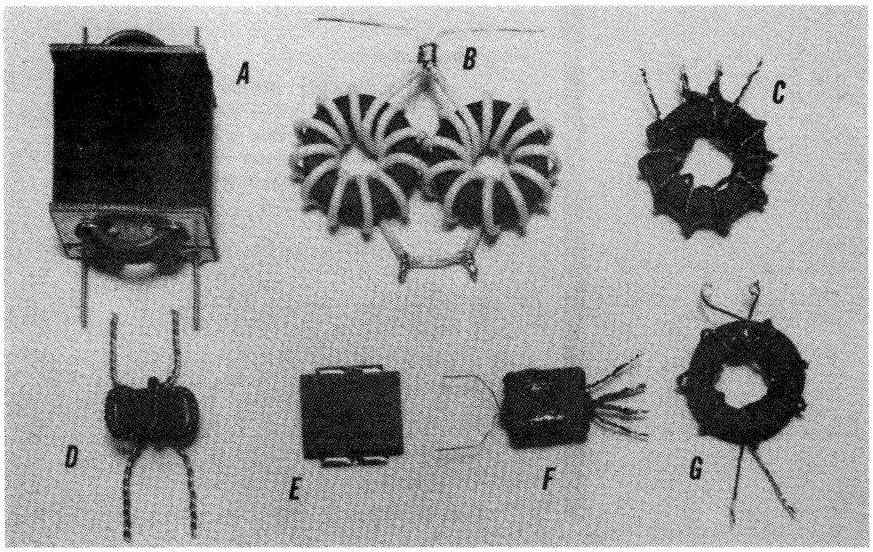


FIGURE 1 – HF Broadband Transformers

Transformers E and F are intended for input applications, although A in a smaller physical form is also suitable. In E, the windings are photo etched on double sided copper-Kapton* (or copper-fiberglass) laminate. The dielectric thickness is 3 mils, and the winding area is 0.25 in^2.

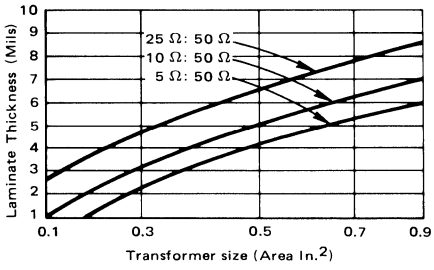


FIGURE 2 – Laminate Thickness versus Winding Area

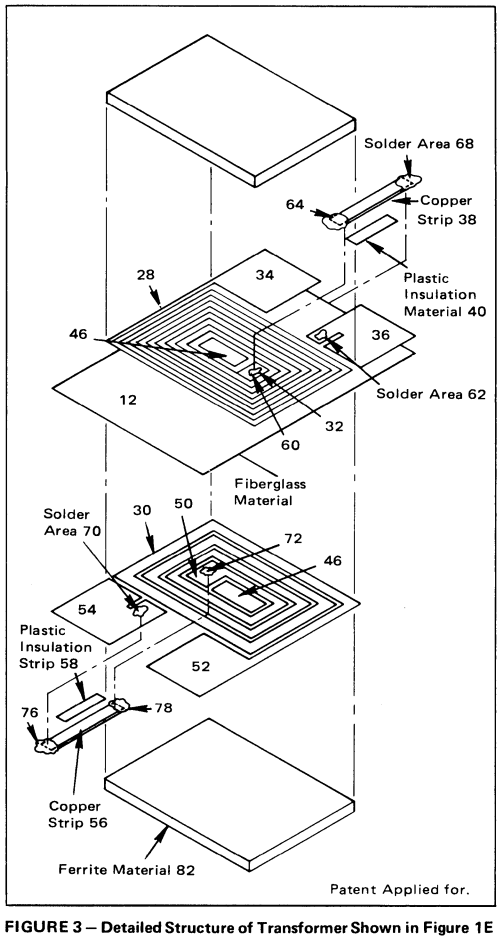


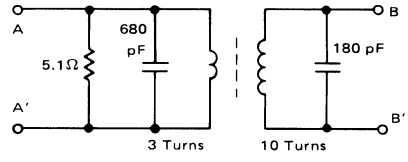
FIGURE 3 – Detailed Structure of Transformer Shown in Figure 1E

*Trademark of E. I. DuPont, De Nemours and Co., Inc.

Ferrite plates (μ_r = 2000 to 3000) are cemented on each side to improve the low frequency response. This type transformer in the size shown, can handle power levels to 10 W. Figure 2 shows curves for laminate thickness versus winding area for various impedance ratios.

Impedance ratios of this transformer are not limited to integers as 1:1, 4:1 — N:L, and the dc isolated primary and secondary have an advantage in certain circuit configurations. This design will find its applications in high volume production or where the small physical size is of main concern. Table 1 shows the winding configuration and measured data of the transformer shown in Figure 3.

TABLE 1 – Impedance at Terminals BB'
Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	50.7	+j 81
2.0	53.0	+j 185
4.0	53.1	+j 1518
8.0	53.5	-j 214
16.0	50.5	-j 79
32.0	52.9	-j 30

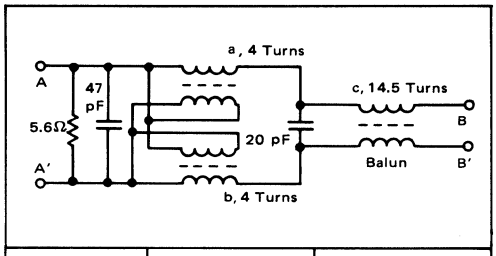
In the transformer shown in Figure 1F and Table 2, a regular antenna balun core is employed (Indiana General F684-1 or equivalent). Lines A and B each consist of two twisted pairs of AWG #30 enameled wire. The line impedances are measured as 32 Ohms, which is sufficiently close to the optimum 25 Ohms calculated for 4:1 impedance ratio. ($Z_O = \sqrt{R_{in} R_L}$).

Windings a and b are wound one on top of the other, around the center section of the balun core. Line c should have an optimum Z_O of 50 Ohms. It consists of one pair of AWG #32 twisted enameled wire with the Z_O measured as 62 Ohms. The balun core has two magnetically isolated toroids on which c is wound, divided equally between each. The inductance of c should approach the combined inductance of Lines a and b (Reference 4, 6).

The reactance in the 50 Ohm port (BB') should measure a minimum of + j 200. To achieve this for a 4:1 transformer, a and b should each have three turns, and for a 9:1 transformer, four turns. When the windings are connected as a 9:1 configuration, the optimum Z_O is 16.6 Ohms, and a larger amount of high frequency compensation will be necessary. Lower impedance lines can be realized with heavier wires or by twisting more than two pairs together. (e.g., four pairs of AWG #36 enameled wire

would result in the Z_O of approximately 18 Ohms.) Detailed information on the manufacture of twisted wire transmission lines can be found in References 2, 4, and 8.

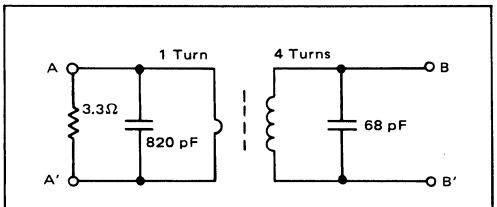
TABLE 2 – Impedance at Terminals BB'
Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	53.0	+j 185
2.0	52.6	+j 330
4.0	52.9	+j 430
8.0	53.1	+j 600
16.0	53.2	+j 750
32.0	53.5	+j 3060

Figure 1A shows one of the most practical designs for higher impedance ratios (16 and up). The low impedance winding always consists of one turn, which limits the available ratios to integers 1, 4, 9 — N. Data taken of this type of a 16:1 transformer is shown in Table 3, while Figure 4 illustrates the physical construction. Two tubes, 1.4" long and 1/4" in diameter – copper or brass – form the primary winding. The tubes are electrically shorted on one end by a piece of copper-clad laminate with holes for the tubes and the tube ends are soldered to the copper foil. The hole spacing should be larger than the outside diameter of the ferrite sleeves.

TABLE 3 – Impedance at Terminals BB'
Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	54.0	+j 1030
2.0	54.0	+j 3090
4.0	54.0	+j 5800
8.0	53.9	-j 300
16.0	53.1	-j 760
32.0	53.2	-j 600

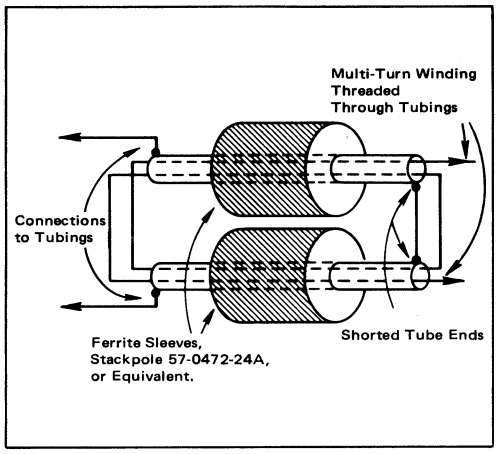


FIGURE 4 – Physical Construction of a 16:1 Transformer
(Actual Number of Turns Not Shown)

A similar piece of laminate is soldered to the opposite ends of the tubes, and the copper foil is divided into two sections, thus isolating the ends where the primary connections are made. The secondary winding is formed by threading wire with good RF insulating properties through the tubes for the required number of turns.

Although the measurements indicate negligible differences in performance for various wire sizes and types (stranded or solid), the largest possible diameter should be chosen for lower resistive losses. The initial permeability of the ferrite sleeves is determined by the minimum inductance required for the lowest frequency of operation according to the previous formula. Typical μ_T's can vary from 800 to 3000 depending upon the cross sectional area and lowest operating frequency. Instead of the ferrite sleeves, a number of toroids which may be more readily available, can be stacked.

The coupling coefficient between the primary and secondary is almost a logarithmic function of the tube diameter and length. This factor becomes more important with very high impedance ratios such as 36:1 and up, where higher coupling coefficients are required. The losses in the ferrite are determined by the frequency, permeability and flux density. The approximate power handling capability can be calculated as in Reference 4 and 6, but the ferrite loss factor should be taken into consideration. The μ_T in all magnetic materials is inversely proportional to the frequency, although very few manufacturers give this data.

Two other variations of this transformer are shown in Figure 5. The smaller version is suitable for input matching, and can handle power levels to 20 W. It employs a stackpole dual balun ferrite core 57-1845-24B. The low impedance winding is made of 1/8" copper braid. The portions of braid going through the ferrite are rounded, and openings are made in the ends with a pointed tool. The high impedance winding is threaded through the rounded portions of the braid, which was uncovered in each end of the ferrite core. (See Figures 4 and 5.)

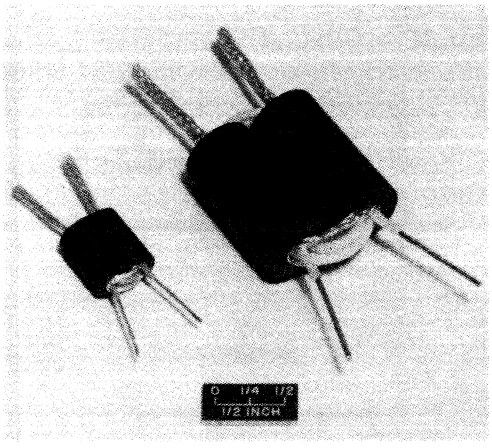


FIGURE 5 – Variations of Transformers in Figure 1A

The construction technique of the larger version transformer is similar, except two separate ferrite sleeves are employed. They can be cemented together for easier handling. This transformer is intended for output applications, with a power handling capability of 200-250 W employing Stackpole 57-0472-27A ferrites. For more detail, see Reference 7.

The transformer shown in Figure 1B is superior in bandwidth and power handling capability. Table 4 shows data taken on a 4:1 transformer of this type. The transmission lines (a and b) are made of 25-Ohm miniature co-axial cable, Microdot 260-4118-000 or equivalent. Two 50 Ohm cables can also be connected in parallel.

The balun, normally required to provide the balanced to unbalanced function is not necessary when the two transmission lines are wound on separate magnetic cores, and the physical length of the lines is sufficient to provide the necessary isolation between AA' and BB'. The minimum line length required at 2.0 MHz employing Indiana General F627-19-Q1 or equivalent ferrite toroids is 4.2 inches, and the maximum permissible length at 30 MHz would be approximately 20 inches, according to formulas 9 and 10 presented in Reference 2. The 4.2 inches would amount to four turns on the toroid, and measures 1.0 μH. This complies with the results obtained with the formula given earlier for minimum inductance calculations.

Increasing the minimum required line length by a factor of 4 will provide the isolation, and the total length is still within the calculated limits. The power loss in this PTFE insulated co-axial cable is 0.03 dB/ft at 30 MHz in contrast to 0.12 dB/ft for a twisted wire line. The total line loss in the transformer will be about 0.1 dB

The number of turns on the toroids has been increased beyond the point where the flux density of the magnetic core is the power limiting factor. The combined line and core losses limit the power handling capability to approximately 300 W, which can be slightly increased by employing lower loss magnetic material.

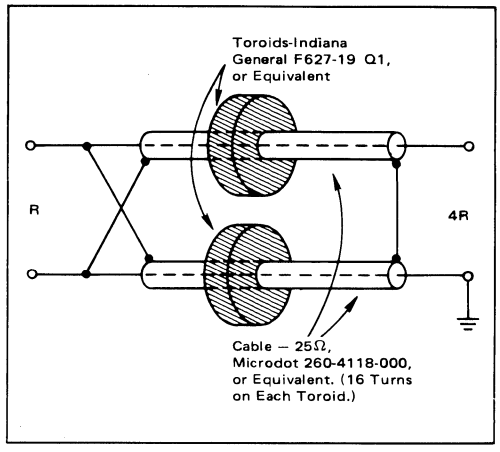
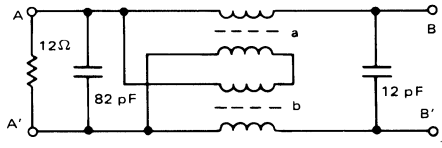


FIGURE 6 – Transformer Construction (Figure 1B)

Note the connection arrangement (Figure 6), where the braid of the cable forms the high current path of the primary.

TABLE 4 – Impedance at Terminals BB'
Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	48.3	+j 460
2.0	48.1	+j 680
4.0	48.0	+j 920
8.0	48.0	+j 1300
16.0	48.1	+j 900
32.0	48.1	+j 690

HIGH-FREQUENCY POWER COMBINING TECHNIQUES EMPLOYING HYBRID COUPLERS

The zero degree hybrids described here are intended for adding the powers of a multiple of solid-state amplifiers, or to combine the outputs of groups of amplifiers, usually referred to as modules. With this technique, powers to the kW level at the high-frequency bands can be realized.

When reversed, the hybrids can be used for splitting signals into two or more equal phase and amplitude ports. In addition, they provide the necessary isolation between the sources. The purpose of the isolation is to keep the system operative, even at a reduced power level during a possible failure in one amplifier or module. The isolation is especially important in output combining of linear

amplifiers, where a constant load impedance must be maintained. Sometimes the inputs can be simply paralleled, and a partial system failure would not have catastrophic effects, but will merely result in increased input VSWR.

For very high frequencies and narrow bandwidths, the hybrid couplers may consist of only lengths of transmission line, such as co-axial cable. The physical lengths of the lines should be negligible compared to the highest operating frequency to minimize the resistive losses, and to avoid possible resonances. To increase the bandwidth and improve the isolation characteristics of the line, it is necessary to increase the impedance for non-transmission line currents (parallel currents) without effecting its physical length. This can be done by loading the line with magnetic material. Ideally, this material should have a linear BH curve, high permeability and low losses over a wide frequency range. For high-frequency applications, some ferrites offer satisfactory characteristics, making bandwidths of four or more octaves possible.

Depending upon the balance and phase differences between the sources, the currents should be mostly cancelled in the balun lines. In a balanced condition, very little power is dissipated in the ferrite cores, and most occurring losses will be resistive. Thus, a straight piece of transmission line loaded with a high permeability ferrite sleeve, will give better results than a multiturn toroid arrangement with its inherent higher distributed winding capacitance.

It is customary to design the individual amplifiers for 50 Ohm input and output impedances for testing purposes and standardization. 50-and 25-Ohm co-axial cable can then be employed for the transmission lines. Twisted wire lines should not be used at power levels higher than 100 Watts average, due to their higher dielectric losses.

Variations of the basic hybrid are shown in Figure 7A and B where both are suitable for power dividing or combining.

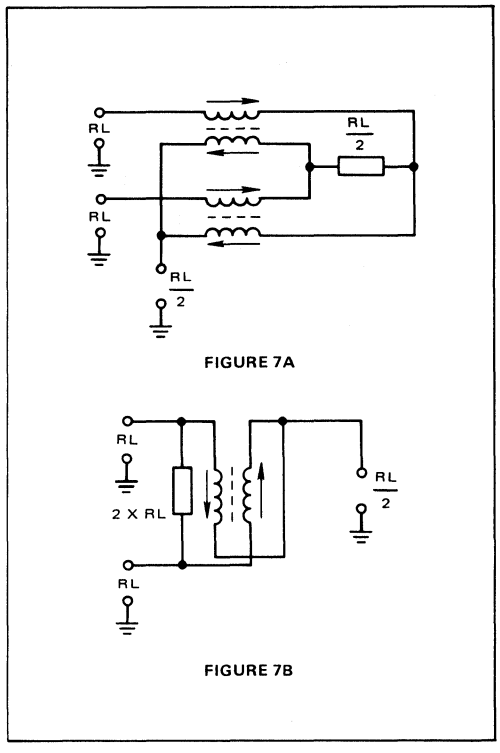


FIGURE 7 – Variations of Basic Hybrid

The balancing resistors are necessary to maintain a low VSWR in case one of the 50-Ohm points reaches a high impedance as a result of a transistor failure. As an input power splitter, neither 50-Ohm port will ever be subjected to a short due to the base compensation networks, should a base-emitter junction short occur. An open junction will result in half of the input power being dissipated by the balancing resistor, the other half still being delivered to the amplifier in operation. The operation is reversed when the hybrid is used as an output combiner. A transistor failure will practically always cause an increase in the amplifier output impedance. Compared to the 50-Ohm load impedance it can be regarded as an open circuit. When only one amplifier is operative, half of its output power will be dissipated by R, the other half being delivered to the load. The remaining active source will still see the correct load impedance, which is a basic requirement in combining linear amplifiers. The resistors (R) should be of noninductive type, and rated for 25% of the total power, unless some type of automatic shutoff system is incorporated. The degree of isolation obtainable depends upon the frequency, and the overall design of the hybrid. Typical figures for 2 to 30 MHz operation are 30-40 dB. Figures 8A and B show 4 port "totem pole" structures derived from Figures 7A and 7B. Both can be used with even number of sources only, e.g. 4, 8, 16, etc. For type 8B, it is more practical to employ toroidal multi-turn lines, rather than the straight line alternatives, discussed earlier. The power output with various numbers of inoperative sources can be calculated as follows, if the phase differences are negligible: (Reference 2)

$$P_{out} = \left(\frac{P}{N}\right) N_1$$

where: P = Total power of operative sources
N = Total number of sources
N_1 = Number of operative sources

Assuming the most common situation where one out of four amplifiers will fail, 75% of the total power of the remaining active sources will be delivered to the load.

Another type of multiport hybrid derived from Figure 7A is shown in Figure 9. It has the advantage of being capable of interfacing with an odd number of sources or loads.

In fact, this hybrid can be designed for any number of ports. The optimum values of the balancing resistors will vary according to this and also with the number of ports assumed to be disabled at one time. Two other power combining arrangements are shown in Figures 10 and 11.

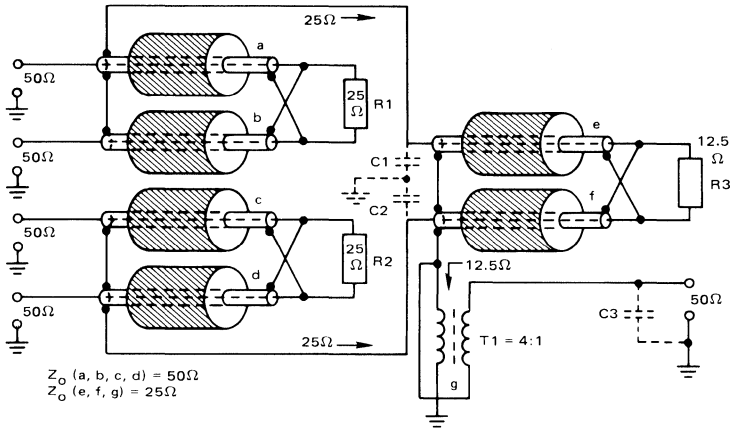


FIGURE 8A

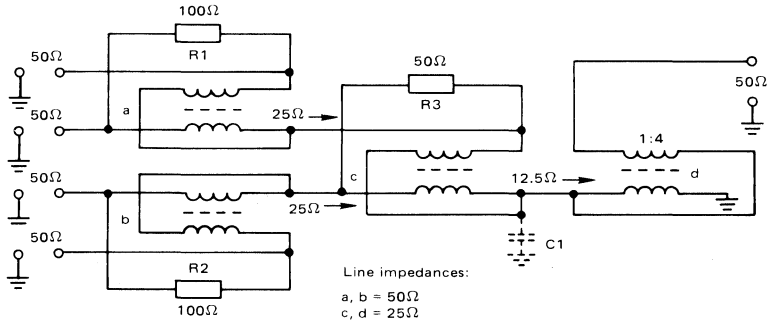


FIGURE 8B

FIGURE 8 – Four Port "Totem Pole" Structure

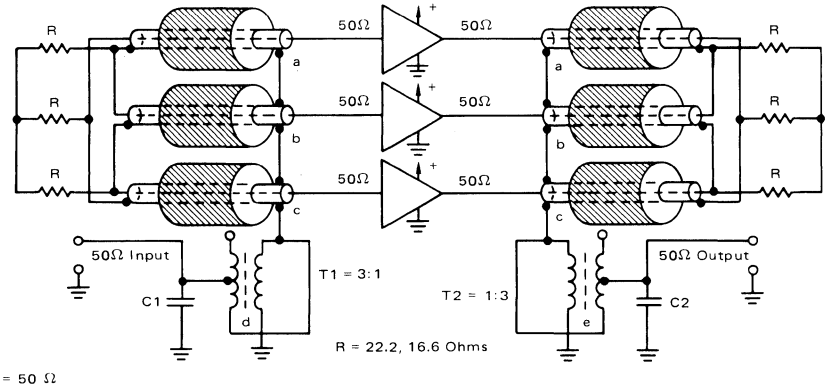
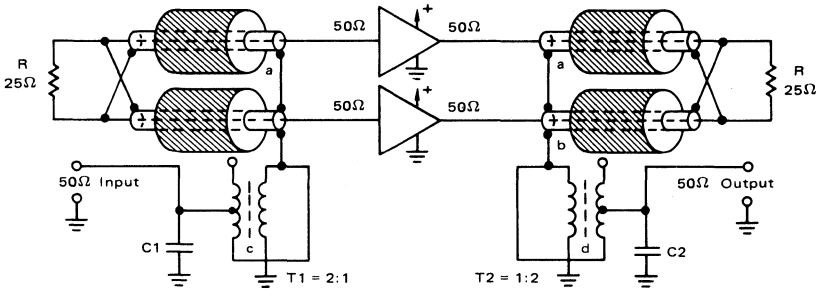
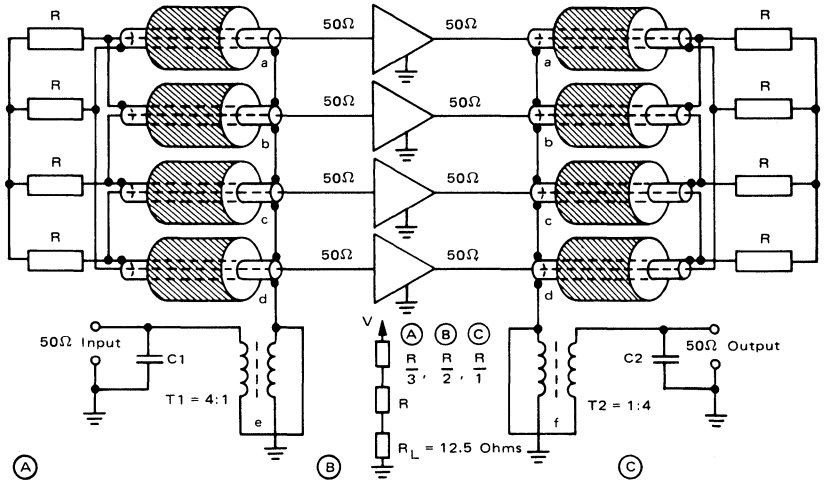


FIGURE 9 – Three-Port Hybrid Arrangement



Z_o (a,b) = 50 Ω
Z_o (c,d) = 25 Ω (optimum 35.4 Ω)

FIGURE 10 — Two-Port Hybrid System



Ⓐ

1 PORT INOPERATIVE.

Optimum R = 28.3 Ohms

$P_{out} = (P1+P2+P3)-(P_R + P\frac{R}{3})$

Ⓑ

2 PORTS INOPERATIVE.

Optimum R = 25 Ohms

$P_{out} = (P1+P2)-(P_R+P\frac{R}{2})$

Ⓒ

3 PORTS INOPERATIVE.

Optimum R = 18.75 Ohms

$P_{out} = P1-(P_R+P\frac{R}{1})$

P1, P2, P3 = Power at any operative port, P_R = Power dissipated in R, excluding R_L.
V = RMS voltage at any 50 Ohm point.
(The phase differences are assumed negligible.)

Z_o (a,b,c,d) = 50 Ω
Z_o (e,f) = 25 Ω (optimum)

FIGURE 11 — Four-Port Hybrid System

The isolation characteristics of the four-port output combiner were measured, the data being shown in Table 5. The ferrite sleeves are Stackpole 57-0572-27A, and the transmission lines are made of RG-142/U co-axial cable. The input power dividers described here, employ Stackpole 57-1511-24B ferrites, and the co-axial cable is Microdot 250-4012-0000.

TABLE 5 – Isolation Characteristics of Four Port Output Combiner

f (MHz)	Isolation, Port-to-Port (dB)
2.0	27.0-29.4
4.0	34.8-38.2
7.5	39.0-41.2
15	32.1-33.5
20	31.2-33.0
30	31.0-33.4

The input and output matching transformers (T1 – T2) will be somewhat difficult to implement for such impedance ratios as 2:1 and 3:1. One solution is a multi-turn toroid wound with co-axial cable, such as Microdot 260-4118-000. A tap can be made to the braid at any point, but since this is 25-Ohm cable, the Z_O is optimum for a 4:1 impedance ratio only. Lower impedance ratios will normally require increased values for the leakage inductance compensation capacitances (C1 – C2). For power levels above 500-600 W, larger diameter co-axial cable is desirable, and it may be necessary to parallel two higher impedance cables. The required cross sectional area of the toroid can be calculated according to the B_{max} formulas presented in References 4 and 6.

The 2 to 30 MHz linear amplifier (shown in Figure 13) consists of two 300 W modules (8). This combined amplifier can deliver 600 W peak envelope power. The CW power output is limited to approximately 400 W by the heatsink and the output transformer design.

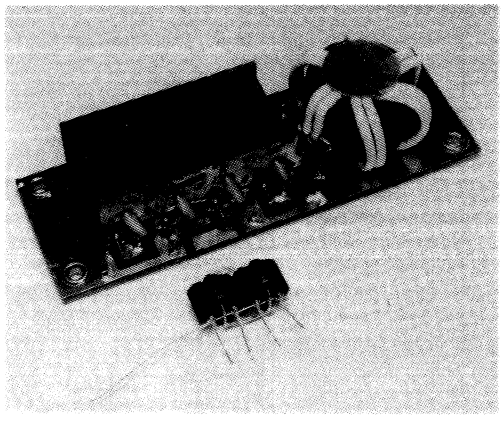


FIGURE 12 – Two-Four Port Hybrids

The one at the lower left is intended for power divider applications with levels to 20 – 30 W. The larger one was designed for amplifier output power combining, and can handle levels to 1 – 1.5 kW. (The balancing resistors are not shown with this unit.)

The power combiner (Figure 13A) and the 2:1 step-up transformer (Figure 13B) can be seen in the upper right corner. The input splitter is located behind the bracket (Figure 13C). The electrical configuration of the hybrids is shown in Figures 7A and 10. Note the loops equalizing the lengths of the co-axial cables in the input and output to assure a minimum phase difference between the two modules.

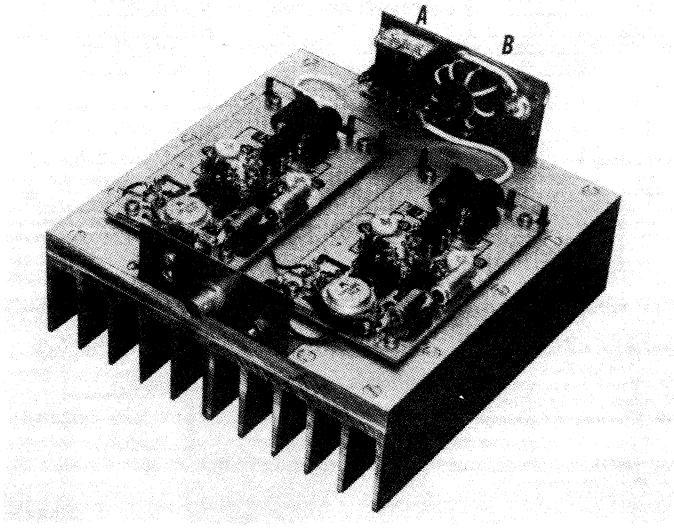


FIGURE 13 – 2 to 30 MHz Linear Amplifier Layout

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1. Ruthroff: Some Broad Band Transformers, *IRE, Volume 47,* August 1957.
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5. *Philips Telecommunication Review, Volume 30, No. 4,* pp. 137-146, November 1972.
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CRYSTAL SWITCHING METHODS FOR MC12060/MC12061 OSCILLATORS

Prepared by:
John Hatchett
Roger Janikowski

This report discusses methods of using diodes to select series resonant crystals electronically. Circuit designs suitable for use with crystal frequencies from 100 kHz to 20 MHz are developed with emphasis being placed on minimizing frequency pulling. Although developed for use with the MC12060 and MC12061 integrated circuit crystal oscillators, the techniques will, in general, be useful in any application where it is desired to electronically select one out of a group of crystals with a minimum of disturbance to the series resonant frequency of the selected crystal.

CRYSTAL SWITCHING METHODS FOR MC12060/MC12061 OSCILLATORS

INTRODUCTION

Crystal switching can be achieved electronically for the MC12060 and MC12061 crystal oscillator integrated circuits by utilizing diodes as RF switches. The switching is controlled by applying a forward bias to the diode associated with the desired crystal and applying a reverse bias to the remaining diodes related to the unselected crystals.

In addition to functioning with the MC12060/MC12061 IC's, the switching circuit designs described here can also be used in other applications where it is desired to electronically switch series-resonant crystals with a minimum of frequency pulling.

Advantages to this switching scheme include the following:

1. Eliminates the need to run high frequency signals through a mechanical switch;
2. Permits switching crystals from a remote position with a minimum of disturbance to the oscillator;
3. Minimizes RF radiation;
4. Adapts easily to electronic scanning methods;
5. Operates from a single polarity, low voltage supply (5.0 volts).

GENERAL

The MC12060 and MC12061 crystal oscillators are specified for operating frequency ranges of 100 kHz to 2.0 MHz, and 2.0 MHz to 20 MHz respectively. Their outputs consist of a single-ended TTL signal, plus complementary sine wave and ECL signals. The sine wave outputs are capable of driving an ac load of 50 ohms at 500 mVp−p (typical) when an external resistor is used to increase the current in the emitter follower output. The ECL and TTL outputs are capable of driving five and ten gate loads respectively.

Series resonant crystals connected between Pins 5 and 6 are required for use with these oscillators. The total effective ac series resistance (crystal series resonance resistance plus any additional resistance contributed by switching components) between these pins must be less than 4 k ohms for the MC12060, and less than 155 ohms for the MC12061.

For additional information on these IC's, see the device data sheet and Engineering Bulletins EB59 and EB60.

Schematic diagrams for the MC12060 and MC12061 crystal switching circuits are given in Figures 1 and 2 respectively. The same basic technique is employed for each IC except that an additional diode-resistor pair (D6, R18 through D10, R22) is incorporated for the MC12060 to offset its greater sensitivity to ac loading.

The MPN3401 PIN diode and the MSD7000 PN junction diode are used to switch the crystals. The MSD7000 was selected for use with the MC12060 oscillator because of its low capacitance (1.5 pF max. for V_R = 0 volts). It is also an economical dual diode in the configuration needed for this circuit.

The MPN3401 is used with the MC12061 circuit because it offers a large off-to-on impedance ratio for low dc bias currents at frequencies within the range of the MC12061.

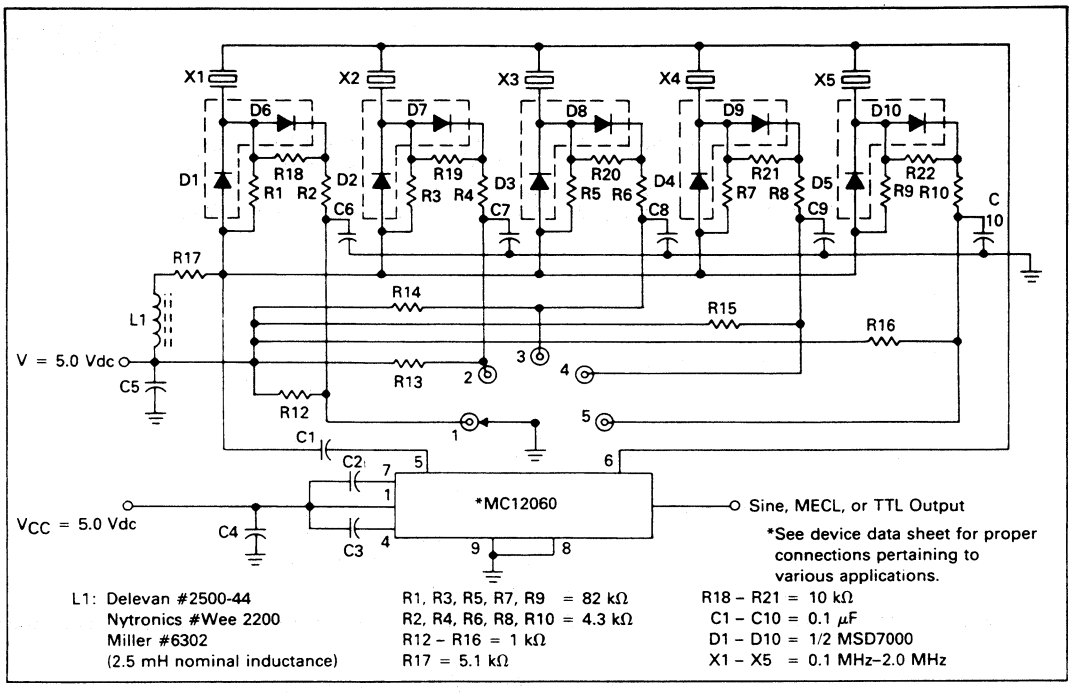

FIGURE 1 — Schematic Diagram of Crystal Switching for the MC12060.

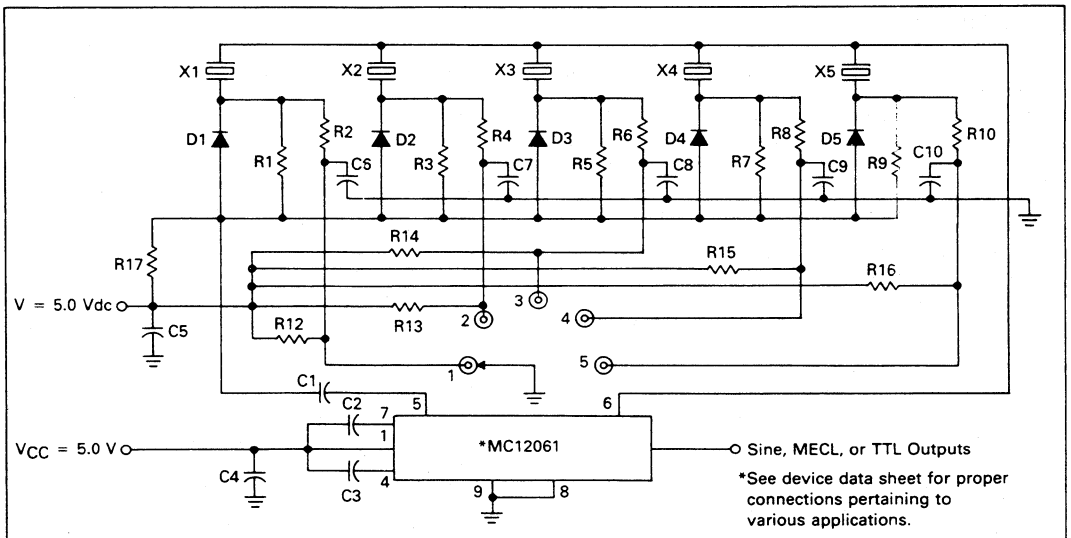

FIGURE 2 — Schematic Diagram of Crystal Switching for the MC12061

DC BIAS REQUIREMENTS

Forward bias for the desired crystal selecting diode (D1, D2, D3, D4, or D5) is applied by setting the five position switch. The bias current is primarily set by R17 and R2 (R4, R6, R8, and R10 have identical functions to R2 when they are switched-in). The four remaining sets of bias resistors, corresponding to the unselected crystals, add a smaller amount of current to the forward-biased diode. The total forward bias current, I_D, can be described by the formulas:

$$I_D = \frac{V - 2V_D}{R2 + \{R17 \parallel \left(\frac{R3 + R4 + R19}{4}\right)\}} - \left(\frac{V_D}{R1}\right) \text{ (For MC12060);}$$

$$I_D = \frac{V - V_D}{R2 + \{R17 \parallel \left(\frac{R3 + R4 + R13}{4}\right)\}} - \left(\frac{V_D}{R1}\right) \text{ (For MC12061).}$$

While one diode (or one diode pair in the case of Figure 1) is always forward biased, the remaining diodes are reverse biased to minimize their capacitance. This is accomplished with a single polarity supply by using pullup resistors (R12, R13, R14, R15, and R16) from the positive potential to each switch terminal. Therefore, the cathodes of the diodes corresponding to the unselected crystals are pulled up to approximately the supply voltage. Since one diode (or diode pair) is always selected, current is flowing through R17 continuously, causing a voltage drop. Therefore, the anodes of the unselected diodes will be negative with respect to their cathodes. When using a 5.0 volt supply, this reverse bias will be 1.6 volts for the MC12060 and 1.2 volts for the MC12061 crystal switching array.

ADDITIONAL CONSIDERATIONS

A sufficient amount of forward current through the diode selecting the desired crystal is required to insure a low value for diode resistance R_D (see Figure 3). This is important for two reasons:

1. To minimize the effects of diode capacity on the crystal's natural series resonant frequency.
2. To minimize the total effective external resistance between Pins 5 and 6 of the integrated circuit.

From Figure 3 it is apparent that as R_D is made smaller, X_S is decreased and C_S is increased. A large value for C_S relative to the crystal's equivalent series capacitance is required to satisfy item 1.

The impedance of the MSD7000 diode with 0.45 mA of bias current has a typical value of 115 $-3°$ = 114.6-j6 ohms at 100 kHz and 115 $-8°$ = 113.8-j16 ohms at 2 MHz; resulting C_S values are respectively 0.265 μF and 0.005 μF. Since typical series resonant crystals in this frequency range exhibit equivalent series capacitance values, C_X, ranging from 0.024 pF to 0.012 pF, item 1 is satisfied. Also, since the equivalent series resistance of the diode is much less than the maximum effective resistance specification (4 k ohms) for the MC12060, item 2 is satisfied.

For the MC12061 circuit, the diode forward bias current is 1.15 mA. This current is sufficient to keep the series impedance of the MPN3401 PIN diode low. At 2 MHz the impedance is nominally 22 $-28°$ = 19.4-j10 ohms and at 20 MHz 3.3 $-37°$ = 2.6-j1.98 ohms. The resulting C_S values in this case are 0.008 μF and 0.004 μF. Typical series resonant crystals in this frequency range exhibit equivalent C_X capacity values of 0.012 pF to 0.003 pF and the maximum series resistance specification for the MC12061 is 155 ohms. Again, the requirements of both items 1 and 2 above are met.

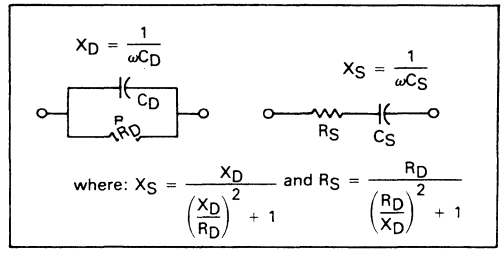

FIGURE 3 — Diode Equivalent Circuits

DECOUPLING UNSELECTED CRYSTALS

Isolating unselected crystals is very important from the standpoint of minimizing frequency pull of the selected crystal, and insuring that the oscillator will lock on a new crystal frequency when switched from a previous one.

The objective for decoupling unselected crystals is to place a high impedance in series with them. The MSD7000 typically has 0.72 pF of shunt capacitance C_D (refer to Figure 3) at V_R = 1.6 volts, and the MPN3401 typically 0.75 pF at 1.2 volts of reverse bias. Since R_D is extremely large for the reverse bias condition, the resulting diode R_S resistance will not be exceptionally large and C_S will approximately equal C_D. This series capacitance is 30 to 300 times greater than typical values of equivalent crystal series resonant capacitance (C_X). Therefore, the total series equivalent capacitance ($CT = \frac{C_S C_X}{C_S + C_X}$) decreases by only 3.2% to 0.33% respectively. This, combined with a low value for R_S, maintains considerable coupling between the unselected crystal (s) and the oscillator. Thus, the oscillator may remain at the previous crystal frequency, or operate at some random frequency.

To reduce this problem, a shunt resistor (R_1, R_3, R_5, R_7, R_9) is added to each switching diode (D_1, D_2, D_3, D_4, D_5) in Figures 1 and 2. This shunt resistor establishes a new and lower value for R_D in Figure 3, which results in a new R_S value — much greater than the maximum allowable effective resistance specification for the MC12060/MC12061.

Worst-case coupling effects occur at 2 MHz for the MC12060 and 20 MHz for the MC12061. Referring to Figure 3: assume C_D is equal to 1 pF; this gives $X_D = \frac{1}{2\pi f C_D}$ = 79.5 k ohms at 2 MHz, and 7.95 k ohms at 20 MHz. To maximize the series equivalent resistor (R_S), the parallel resistor R_D is made equal to the reactance X_D at the highest operating frequency. For the MC12060, the values of $R_D = X_D$ = 79.5 k ohms give $R_S = X_S$ = 39.7 k ohms. Since R_S is now much greater than 4 k ohms, the unselected crystals will be virtually isolated

from the oscillator. This isolation will become greater with a decrease in frequency.

Using the same formulas to determine the required R_D and to calculate R_S and X_S at 20 MHz for the MC12061 results in $R_D = X_D = 7.95$ k ohms, giving a new value of $R_S = X_S = 3.97$ k ohms. This value of R_S is much greater than 155 ohms, the maximum effective resistance specification for the MC12061. Therefore, the oscillator will now have sufficient isolation from the unselected crystals to prevent erratic performance.

The values used for R1, R3, R5, R7 and R9 are 82 k ohms, and 10 k ohms for Figures 1 and 2 respectively.

OSCILLATOR AC LOADING

Oscillator ac loading must be minimized to reduce frequency pulling and sine wave distortion. For the circuits shown in Figures 1 and 2 the ac loading is primarily attributable to the biasing networks for the five diodes (D1–D5). All bias elements contribute to an effective ac load, regardless of which crystal position is selected. This occurs because the RF signal is coupled through the parallel capacitance (C_O) of the unselected crystals.

Due to a greater sensitivity to ac loading of the MC12060, additional elements are used in the switching networks for this device. An RF choke, L1, is incorporated to minimize the loading effects of the common bias resistor, R17. In addition, a modified approach is used to bias diodes D1 through D5. The networks (D6, R18) through (D10, R22) are added to minimize ac loading and, at the same time, supply sufficient forward current with a 5-volt supply. One diode (D1–D5) in the MSD7000 dual diode package is used to switch the crystal and the second diode (D6–D10) is used for reducing ac loading. R18 through R22 are essential to supply a small amount of current for reverse bias of diodes D1–D5 corresponding to the unselected crystals.

Loading and therefore frequency pulling will be greater for higher frequency crystals and will increase as the total number of crystals to be switched is increased. However, by using the switching techniques shown in Figures 1 and 2, any frequency pulling in addition to that for a single crystal connected directly to Pins 5 and 6 (i.e. pulling caused by the ICs alone) is negligible below approximately 1 MHz for the MC12060 and 15 MHz for the MC12061. Measurements of this additional pulling are summarized in Table 1. Typical frequency pulling values attributable to the ICs themselves are given in Table II. In this case the devices are operating with a single crystal connected directly to Pins 5 and 6 with no crystal switching circuits. The Table II values have been taken as a reference in establishing the pulling (noted in Table I) caused by the switching networks. When using the crystal switching circuits, complete pulling from the crystal's series resonant frequency is obtained by algebraically adding the respective values in Tables I and II. For example, absolute crystal pulling for the five crystal switching system when selecting the nominal 1.0 MHz crystal is approximately $-0.0040 + 0.0031 = -0.0009$ percent. Similarly, absolute pulling for the 8.0 MHz crystal becomes $-0.004 + 0.0001 = -0.0039$ percent. Pulling effects of the switching circuits when selecting the 0.2 MHz crystal offset pulling caused by the IC to give approximately zero absolute crystal pull.

When desirable, a trim capacitor can be added in series with the crystals and adjusted to pull the oscillator up in frequency.

Several options are possible to reduce ac loading for both the MC12060 and MC12061 crystal switching circuits. Using a higher voltage supply for the bias networks will allow larger values of bias resistors to be used at the same diode current, resulting in reduced loading. Also, RF decoupling chokes may be added between resistors R2, R4, R6, R8, and R10 and capacitors C6 through C10. Where frequency pulling is not as critical, L1 in Figure 1 may be eliminated. These options are left to the discretion of the user.

TABLE I. Typical Frequency Pull In Percent Attributable to Crystal Switching Networks

Device	MC12060					MC12061			
Nominal crystal frequency (MHz)	0.1	0.2	0.5	1.0	2.0	2.5	8.0	13.4	20.0
One crystal (connected directly to Pins 5 and 6)	Ref.	Ref.	Ref.	Ref.	Ref.	Ref.	Ref.	Ref.	Ref.
Two crystal switching system	*	+0.0005	+0.0006	+0.0035	−0.004	+0.0008	+0.0013	+0.0004	−0.005
Five crystal switching system	*	+0.0005	+0.0006	+0.0031	−0.018	+0.0008	+0.0001	−0.0006	−0.023

*Less than one Hertz pull, measurement limited to resolution of test equipment.

TABLE II. Typical Frequency Pull In Percent for ICs Only

Device	MC12060					MC12061			
Nominal crystal frequency (MHz)	0.1	0.2	0.5	1.0	2.0	2.5	8.0	13.4	20.0
Pull in percent	*	−0.0005	−0.0012	−0.0040	−0.03	−0.0002	−0.004	−0.01	−0.05

*Less than one Hertz pull, measurement limited to resolution of test equipment.

AN-790

THERMAL RATING OF RF POWER TRANSISTORS

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Reliability is of primary concern to many users of transistors. The degree of reliability achieved is controlled by the device user because he determines the stress levels applied by his circuit and environmental conditions. This application note will permit the device user to estimate transistor reliability from the circuit designer's point of view, namely power dissipation and case temperature.

Introduction

The temperature-dependent thermal properties of silicon and beryllium oxide have been measured and documented by many laboratories during the last twenty years. Only in rare cases has this information been disseminated by semiconductor device manufacturers to the users. The purpose of this note is to clarify and correct some long-standing industry-wide assumptions which have been commonly maintained about thermal resistance and high temperature derating.

Most manufacturer's data sheets include a single thermal resistance number ($R_{\theta JC}$) and use this number to calculate a linear derating constant out to some specified maximum junction temperature. The number cited on the data sheet was probably measured in the 25°C to 50°C range, and assumed constant over the whole range of temperatures up to the maximum specified junction temperature. How often have you calculated a junction temperature from a data sheet, as $T_J = T_A + (\theta_{JC})P_D$? Unfortunately, the thermal resistance of silicon increases by 80% from 25°C to 200°C. The thermal resistance of BeO changes by 30%, if the case temperature goes from 25°C to 100°C. Knowledge of the basic physical properties of the materials and the methods used to calculate and measure thermal resistance will assist the device user in transistor selection and equipment design.

NOTE: °K = °C + 273.

Temperature-Dependent Thermal Properties Of Silicon and Beryllia

The temperature-dependent thermal conductivities of silicon and beryllium oxide are seen in Figures 1 through 3 and Table 1. The temperature ranges are somewhat wider than are necessary for typical transistor operation, but are shown to emphasize the wide variation in thermal conductivities. Fulkerson et al[3] tabulate the values for thermal conductivity and resistivity of silicon from 100°K to 1350°K (see Table 1), and they find that the thermal resistivity of silicon as a function of temperature can be estimated by a linear approximation over the temperature range shown.

$$(400 - 660^{\circ}K)$$
$$1/k = -0.1171 + 2.954 \times 10^{-3}\ T\ (^{\circ}K) \quad (1)$$

$$(600 - 1050^{\circ}K)$$
$$1/k = -0.9609 + 4.229 \times 10^{-3}\ T\ (^{\circ}K) \quad (2)$$

A similar least-square fit to Fulkerson's data over the range 200 to 700°K, within 1%, is given by:

$$(200 - 700^{\circ}K)$$
$$1/k = -0.2286 + 3.1683 \times 10^{-3}\ T\ (^{\circ}K) \quad (3)$$

Similarly for beryllia, one can fit the data of Elston et al[2] over the range of 200 to 800°K, with equation (4).

$$(200 - 800^{\circ}K)$$
$$1/k = 1.943 \times 10^{-5}\ T\ (^{\circ}K)^{1.7} \quad (4)$$

where k is the thermal conductivity in units of watts/cm°K.

TABLE 1 – Smoothed Data for Thermal Conductivity and Resistivity of Silicon (Ref. 3)

T (°K)	Smoothed ORNL Values	
	k (W cm^{-1} deg^{-1})	W = 1/k (cm deg W^{-1})
100	7.52	0.133
150	3.88	0.258
200	2.44	0.410
250	1.78	0.563
300	1.40	0.716
350	1.15	0.870
400	0.939	1.065
450	0.825	1.212
500	0.736	1.359
550	0.663	1.508
600	0.604	1.656
650	0.555	1.803
700	0.500	1.999
750	0.452	2.210
800	0.413	2.420
850	0.380	2.634
900	0.351	2.845
950	0.327	3.055
1000	0.306	3.268
1050	0.287	3.479
1100	0.273	3.65
1150	0.261	3.82
1200	0.251	3.97
1250	0.245	4.08
1300	0.241	4.14
1350	0.239	4.18

FIGURE 1 – Temperature Dependent Thermal Conductivity of Silicon (Ref. 1)

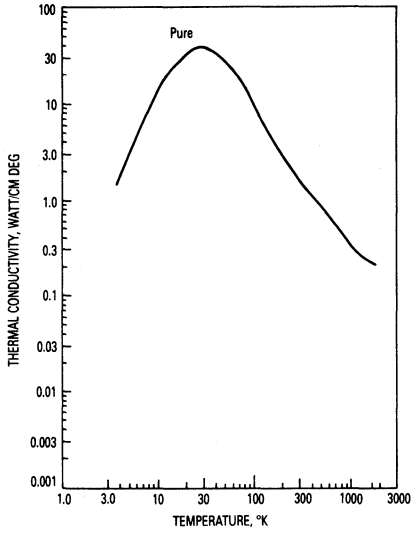


FIGURE 2 – Thermal Conductivity of BeO (Ref. 2)

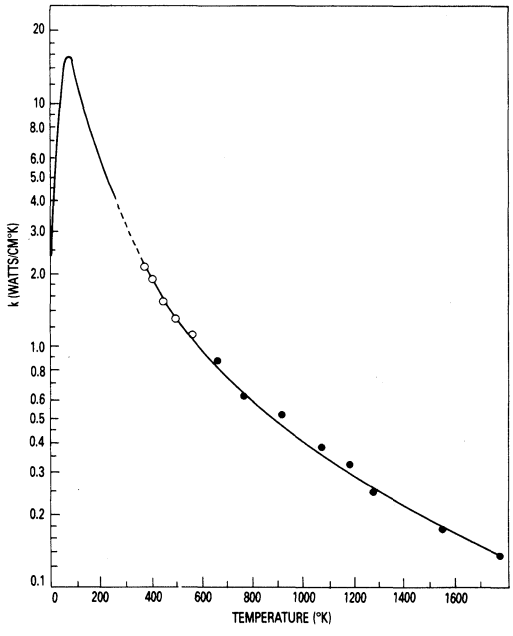
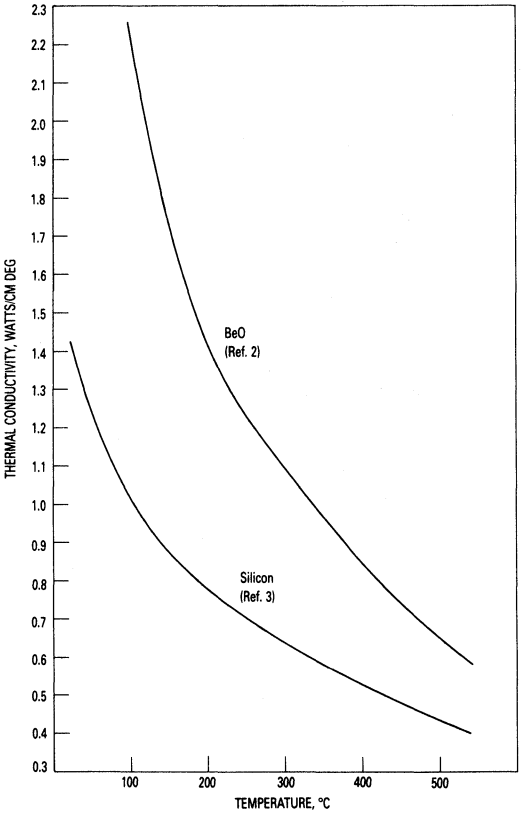


FIGURE 3 – Thermal Conductivity



Geometric Factors and Thermal Resistance Calculation

The thermal resistance of most silicon RF transistors is controlled by the bulk properties of silicon and beryllium oxide, geometry of the heat generating (base) areas, and the temperature of the heat sink (case). The interfaces generally are well behaved and contribute little to the overall total thermal resistance if the device, die and package elements are assembled and handled properly.

Die temperature calculations are performed in two steps. The first uses the method of Linsted and Surtey[4] to calculate the temperature distribution of a die by using a double Fourier series solution to Laplace's equation. Figure 4 shows the device geometry and some of the boundary conditions. Equation (5) will calculate the temperature rise at any (x,y,z) point in the die, where A,B,C,D,F are die and heat-generating area boundaries. Q is the heat input in watts, and k is the thermal conductivity of the material in watts/cm°K (Linsted's equation).

$$
\begin{aligned}
T = &-\frac{Q}{K}\left(\frac{CD}{AB}\right)(z-F) \\
&+\sum_{m=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{2BC}{m^2\pi^2A}\right)e^{m\pi z/B}\left(\frac{1-\exp\left[2m\pi(F-z)/B\right]}{1+\exp\left(2m\pi F/B\right)}\right)\left[\sin\left(\frac{m\pi D}{B}\right)\cos\left(\frac{m\pi y}{B}\right)\right] \\
&+\sum_{n=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{2AD}{n^2\pi^2B}\right)e^{n\pi z/A}\left(\frac{1-\exp\left[2n\pi(F-z)/A\right]}{1+\exp\left(2n\pi F/A\right)}\right)\left[\sin\left(\frac{n\pi C}{A}\right)\cos\left(\frac{n\pi x}{A}\right)\right] \\
&+\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{4}{\pi^2mn\gamma}\right)\left(\frac{1-\exp\left[2\gamma(F-z)\right]}{1+\exp\left(2\gamma F\right)}\right) \\
&\cdot e^{\gamma z}\sin\left(\frac{n\pi C}{A}\right)\sin\left(\frac{m\pi D}{B}\right)\cos\left(\frac{n\pi x}{A}\right)\cos\left(\frac{m\pi y}{B}\right)
\end{aligned}
\tag{5}
$$

where

$$\gamma^2 = \pi^2\left[\left(\frac{n}{A}\right)^2+\left(\frac{m}{B}\right)^2\right].$$

The Fourier series solutions are amenable to computer calculation and converge adequately within ten to twenty terms. Figure 5 shows the treatment of multiple base cell transistors. Lines of symmetry between adjacent base cells are considered to be adiabatic die boundaries as assumed by Lindsted. The power dissipated is assumed to be equally shared among the several base cells. The result of this calculation is the temperature rise of the silicon chip, assuming a constant thermal resistance for bulk silicon. The same model is used to calculate the temperature rise for the beryllia piece, using the silicon die area as the power dissipating area for the beryllia, again assuming the thermal resistance of the beryllia as a constant. The thermal resistances of the silicon die and the beryllia substrate are in series, so adding the above numbers gives a value for the thermal resistance of the device at a particular temperature and a power level low enough to avoid the effects of the temperature variations of the respective thermal resistances.

The second step in the thermal resistance calculation takes into account the temperature-dependent thermal resistivity. The calculated thermal resistance of the beryllia piece (from the previous section) is mathematically divided into fifty layers, each with 1/50 of the total BeO thermal resistance. The first layer at the bottom is assumed to have its temperature at the heat-sink ambient with its thermal resistance value corrected to the proper temperature using the equations for the temperature-dependent resistivity. The power flux through the first layer then leads to its temperature rise, and this new temperature determines the thermal resistivity value for the second layer. Its temperature rise is calculated, and so on, until the result for the top surface of the fiftieth layer gives the temperature rise above the ambient for the beryllia piece.

The same method is used for the silicon die, using the beryllia top surface temperature as the starting point, and correcting the thermal resistance of each of fifty layers based upon the temperature of the layer directly beneath it, until the top surface of the silicon die result gives the calculated die temperature for that particular case of ambient temperature and power dissipation. The results of these calculations indicate that the thermal resistance of a given device is not a constant number, but is a function of the dissipated power and the ambient (case) temperature. Another result is that the junction temperature of a device dissipating power will rise more than 1°C for a 1°C rise in ambient temperature, because of the increase in thermal resistance. Figures 6 through 9 show the calculated thermal resistance and die temperature for several different devices as a function of ambient temperature and power dissipation.

FIGURE 4 – Model for Heat Flow

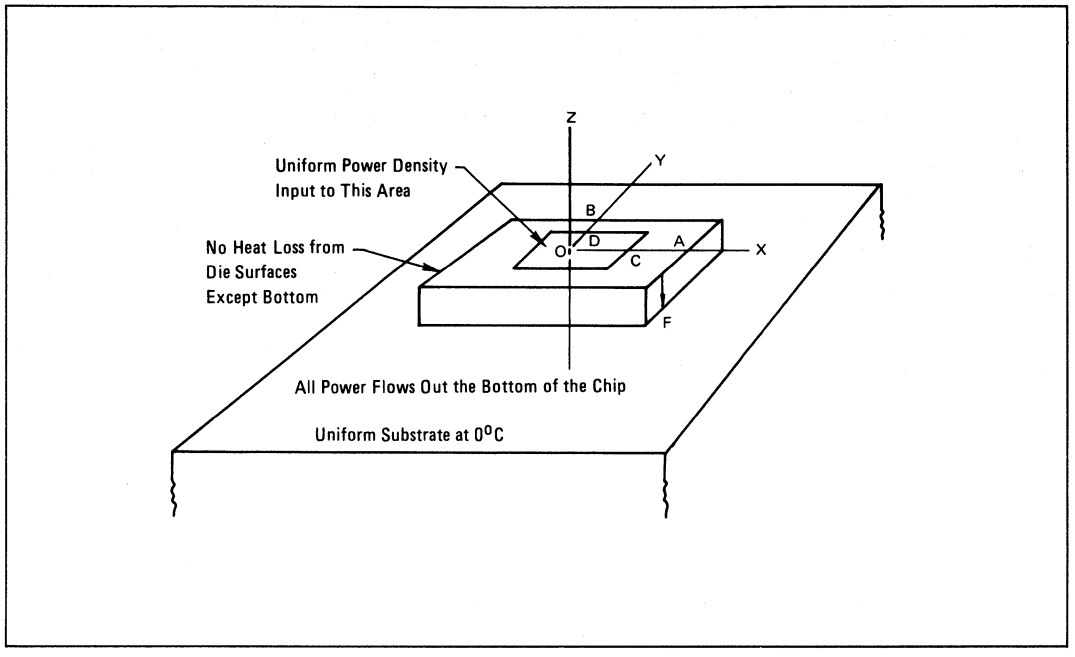


FIGURE 5 – Array of Base Areas in a Silicon Die

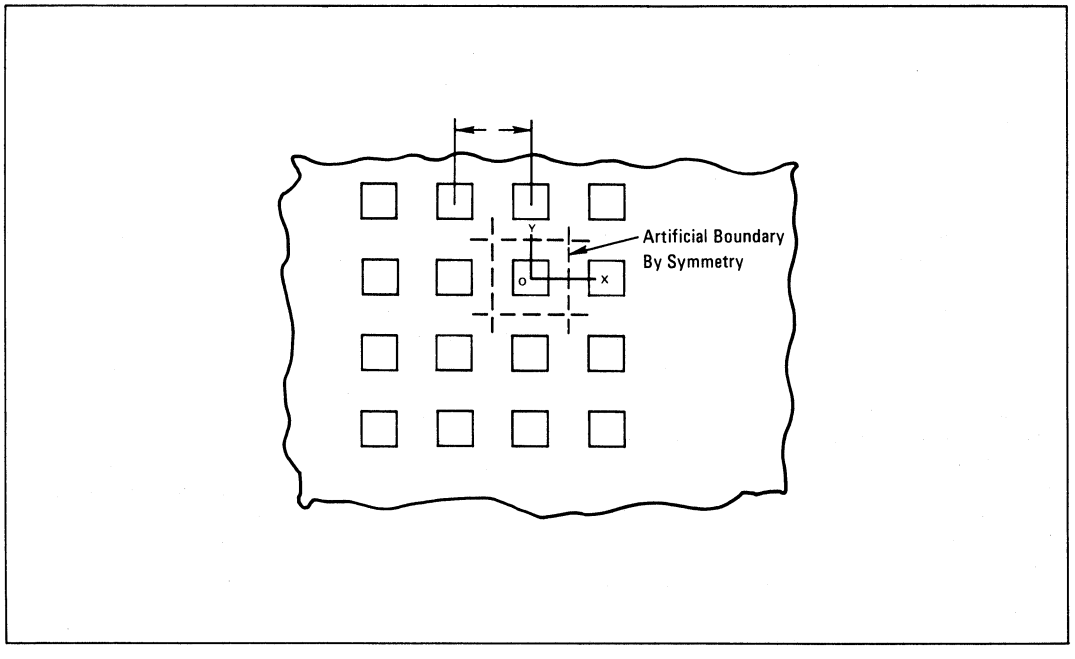


FIGURE 6 – Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

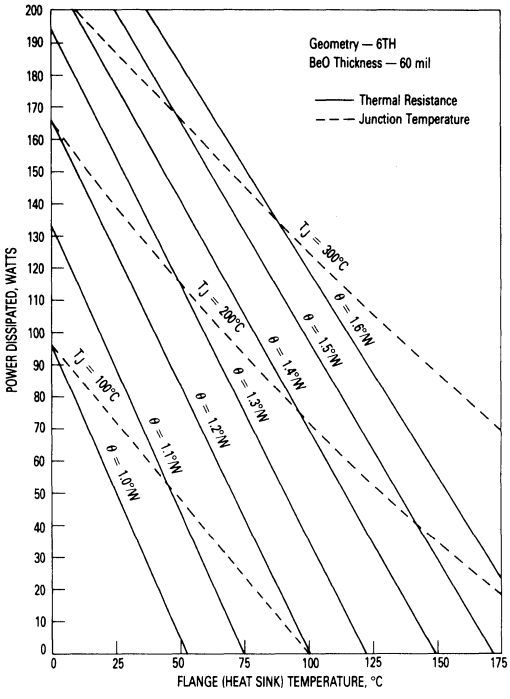


FIGURE 7 – Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

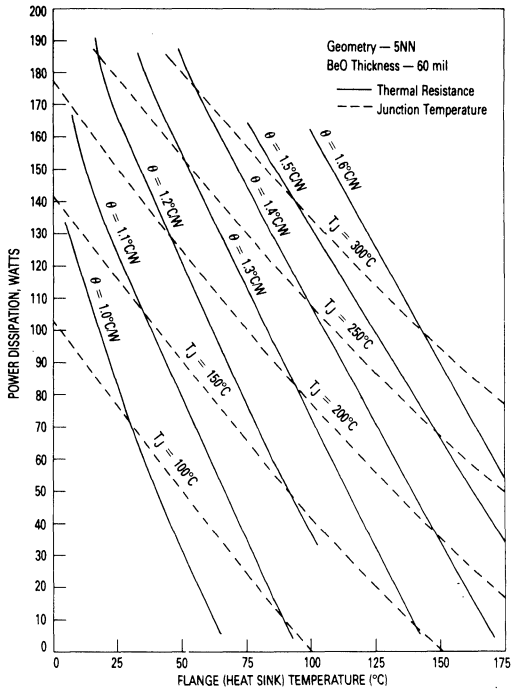


FIGURE 8 – Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

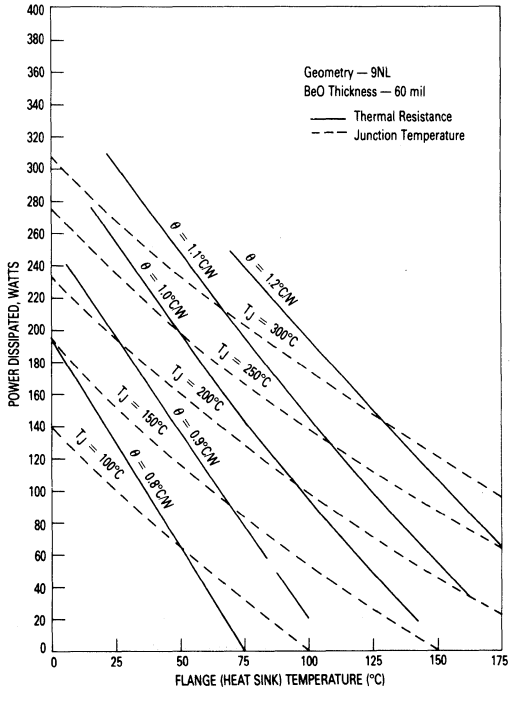
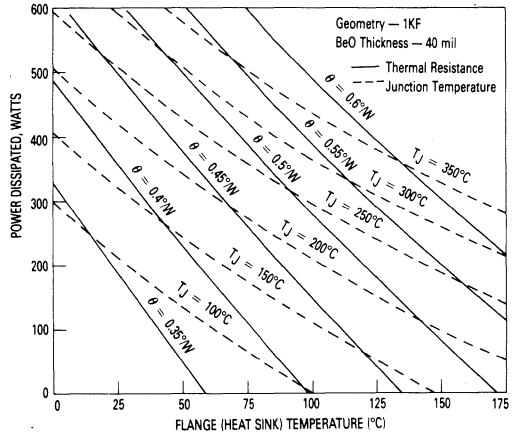


FIGURE 9 – Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature



Experimental Verification Of Calculated Die Temperature

Actual temperature measurements are made with an infrared microscope, Barnes Eng. Co. Model RM2A. This instrument uses an indium antimonide diode photodetector at liquid nitrogen temperatures to measure the infrared radiance emitted from a 1.5 mil spot on the surface being examined. The IR radiance versus temperature curve is calibrated by measuring the radiance at various known temperatures monitored by a calibrated thermocouple while the device is heated by external means. An experimental calibration is necessary because the radiance output of the device at a given temperature is a function of the average emissivity in the area seen by the microscope, and this average emissivity is a function of the geometry and processing history of the device in question. The effective emissivity depends upon the relative amounts of metal and silicon and the infrared transparency of the varying thicknesses of SiO_2 glass in the field of view. The calibration data of radiance versus temperature can be least-squares curve fit to an equation of the form $T = (A)(R)^b$, where A and b are the fitted constants, and R the measured radiance.

The device is then powered up in its circuit, and the radiance data collected point-by-point around the surface of the silicon die. A computer program inputs the array of radiance data, calculates the actual temperature from the calibration equation, and prints a map of the temperature profile, as well as some statistical information about the temperature distribution.

Figures 10 through 12 are plots showing the correlation of measured to calculated temperature for several geometries, under various conditions of flange temperature (30°C to 150°C), supply voltage, drive power, and

FIGURE 11 – Actual vs Calculated Die Temperatures

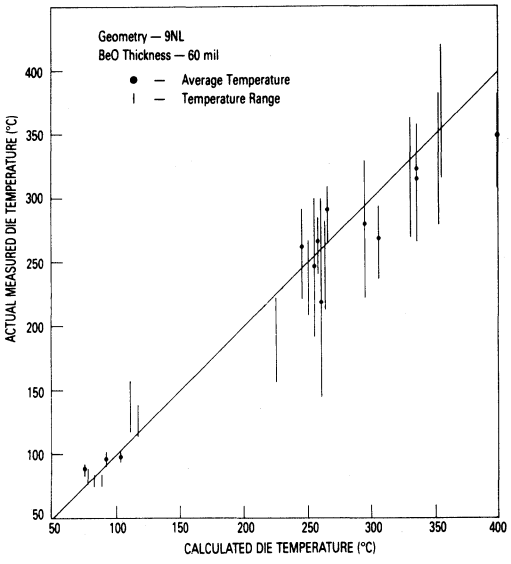


FIGURE 10 – Actual vs Calculated Die Temperatures

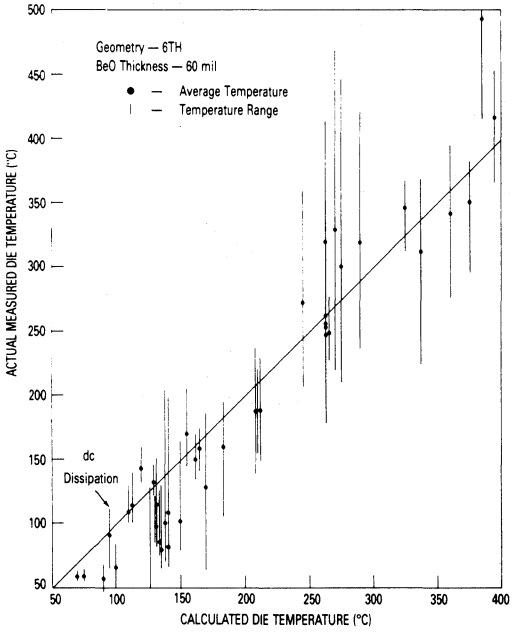
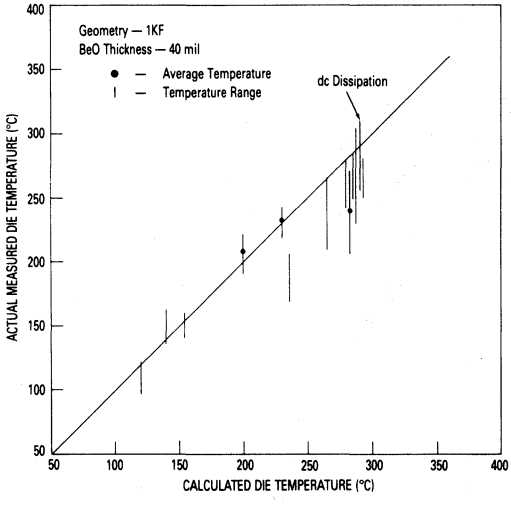


FIGURE 12 – Actual vs Calculated Die Temperatures



output load magnitude and phase angles from 50 Ω to over 30:1 VSWR. The calculated temepratures seem to be somewhat higher than measured at the higher power levels. The calculated temperatures are based on the calculated power dissipation, disregarding RF losses in the actual loads and circuits.

Metal Migration and Mean Time to Failure

The calculated/observed temperature agreements are seen to be close enough so that the calculated temperature can be used as the basis for reliability calculations of Mean Time Before Failure (MTBF) for metal migration based upon Black's[5] work.

$$\text{MTBF} = \frac{(\text{cross section})^3}{I^2 \cdot f(T^O)} \qquad (6)$$

Equation (6) is the equation used for calculating metal migration lifetime, where the cross section refers to the conducting stripe dimensions in cm^2, and I is the current in the stripe in amps. $f(T^O)$ is an Arrhenius function of the stripe material, having the form:

$$f(T^O) = B \exp(-\phi/KT) \qquad (7)$$

The material dependent parameters B and ϕ are shown in Table 2. K is Boltzman's constant, and T is in degrees Kelvin. A series of graphs (Figures 13 through 16) have been constructed, one for each device, that present the results of the calculations of device temperature and MTBF as a function of power and ambient temperature.

The temperature lines are valid for any combination of supply voltage, efficiency and drive power, by reading the power axis as power dissipated. The MTBF lines, because of the current dependence, have been constructed based upon the assumptions of 12.5-volt supply and 50% efficiency, so that the power axis should be interpreted as output power. It is possible to use the MTBF set of lines at other conditions. Enter the graphs by reading the power output parameter as power dissipated, and find the MTBF, then scale the MTBF by the ratio square of the η = 50% current to the actual current.

$$\text{MTBF} = \text{MTBF (from graph)} \times \left(\frac{I\ @\ \eta = 50\%}{I\ \text{actual}}\right)^2 \qquad (8)$$

TABLE 2 – Material Dependent Parameters

Material	B	ϕ
Large Crystal Glassed Al (Ref. 5)	8.5×10^{-10}	1.2
Al–2% Cu Alloy (Ref. 6)	7.9×10^{-17}	0.6

FIGURE 13 – Metal Migration – MTBF

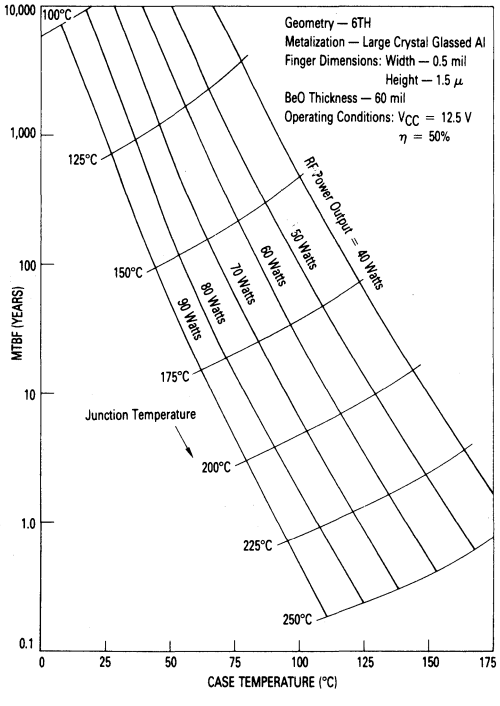


FIGURE 14 – Metal Migration – MTBF

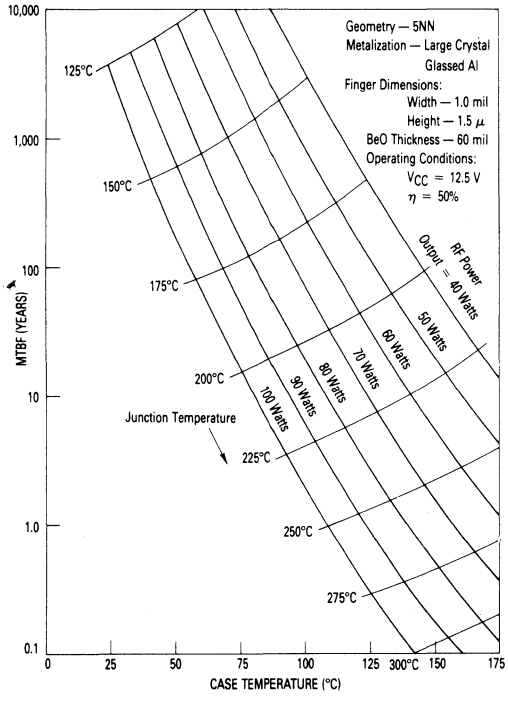


FIGURE 15 – Metal Migration – MTBF

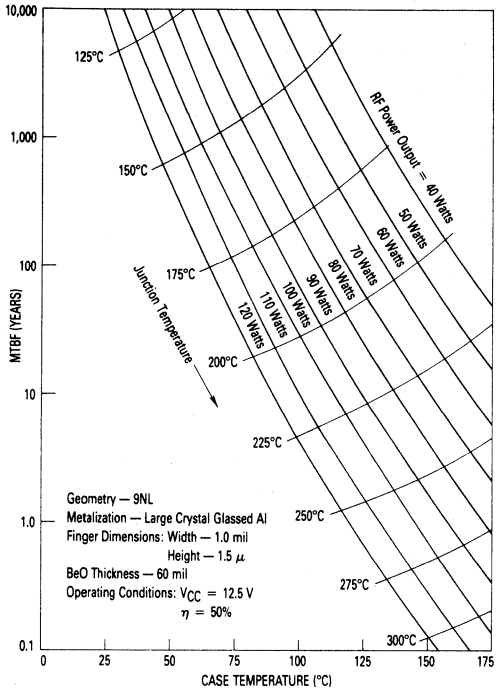


FIGURE 16 – Metal Migration – MTBF

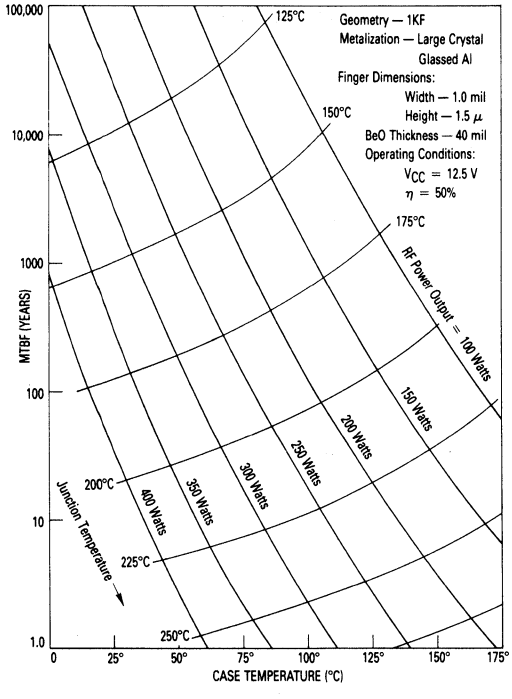


FIGURE 17 – Geometry Code to Standard Part Cross-Reference

Geometry Code	12.5	28		50	V_{CC} (V)
	Al	Al	Au	Al	Metal
1KF	MRF421	MRF422		MRF428A	
5NN	MRF243 MRF453/A MRF455/A MRF460		MRF316		
9NL	MRF245 MRF454/A	MRF463 MRF464/A	MRF317		
6TH	MRF648		MRF327 MRF328		

To Scale Metal Migration MTBF From 12.5 V to Other Operating Voltages

Keeping P_D and η constant, then the current for 28 V operation compared with that for 12.5 V operation is given by:

$$I_{12.5} \times 12.5 = I_{28} \times 28$$

$$\frac{I_{12.5}}{I_{28}} = \frac{28}{12.5}$$

From Black's[5] equation:

$$MTBF \propto \frac{1}{I^2}$$

For like geometries, the ratio of the MTBF at 28 V to the MTBF at 12.5 V is:

$$MTBF_{28} = MTBF_{12.5} \times \left(\frac{28}{12.5}\right)^2$$

$$MTBF_{28} = MTBF_{12.5} \times 5.02$$

Similarly, for 50 V operation:

$$MTBF_{50} = MTBF_{12.5} \times 16.$$

Conclusion

We have discussed the elements of thermal resistance and metal migration lifetime with particular attention paid to their variation with temperature as functions of power dissipation and ambient temperature.

Graphical presentations of the results are included which should be useful to the device user who is interested in better reliability in his application.

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MONOMAX — APPLICATION OF THE MC13001 MONOCHROME TELEVISION INTEGRATED CIRCUIT

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This application note presents a complete 12" black and white line-operated television receiver, including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome, and the significance of component selections and locations are discussed. The design has only 4 factory adjustments: H. Hold, Height, AGC Delay, and V. Linearity, and there are no alignments.

Note that while this discusses MC13001 (525 line, positive tuner AGC) there are also parts for 625 line and negative tuner AGC, in all combinations.

INTRODUCTION

Monomax has been on the market since mid-1981. It was originally developed in a joint effort between Zenith and Motorola for the purpose of creating a high performance B&W receiver. It was intended for all types of monochrome receivers, including the demanding portable and mobile applications, which require immunity to noise, "airplane flutter" and multipath signal conditions. Features suggested by these requirements included: noise filtering and cancelling, dual-loop horizontal PLL, countdown vertical, and a flexible AGC system.

It was also required that the resulting receivers be low in component and manufacturing cost. To meet this objective, effort was made to minimize external components (especially precision components) and adjustments.

Above all, the receiver was to be reliable, so the chip was designed to operate at low voltage and low dissipation. Special attention was given to ESD (electrostatic discharge) immunity on all pins. An extremely stable horizontal oscillator was devised.

Additional features which resulted from this design effort included: a completely integrated IF and detector with no detector tuning or external filtering components, an on-chip dc contrast control which permits remote location of the control without shielded cable, and fully black level clamped video with blanking and beam current limiting. The combination of system functions in the Monomax chip permitted some elegant solutions which would not have been practical or economically feasible in more conventional designs.

It is not the purpose of this AN to describe the overall Monomax chip in any greater detail than is required for understanding receiver design decisions. The reader is urged to obtain a copy of the MC13001 data sheet available from Motorola Literature Distribution or Linear Applications. It contains some of the basic

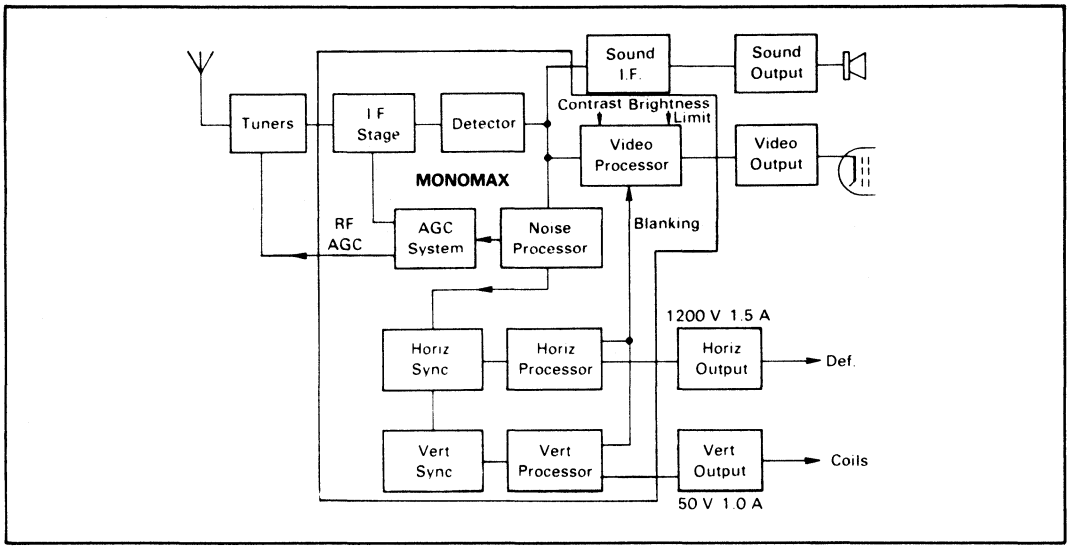


FIGURE 1 — Simplified Block Diagram

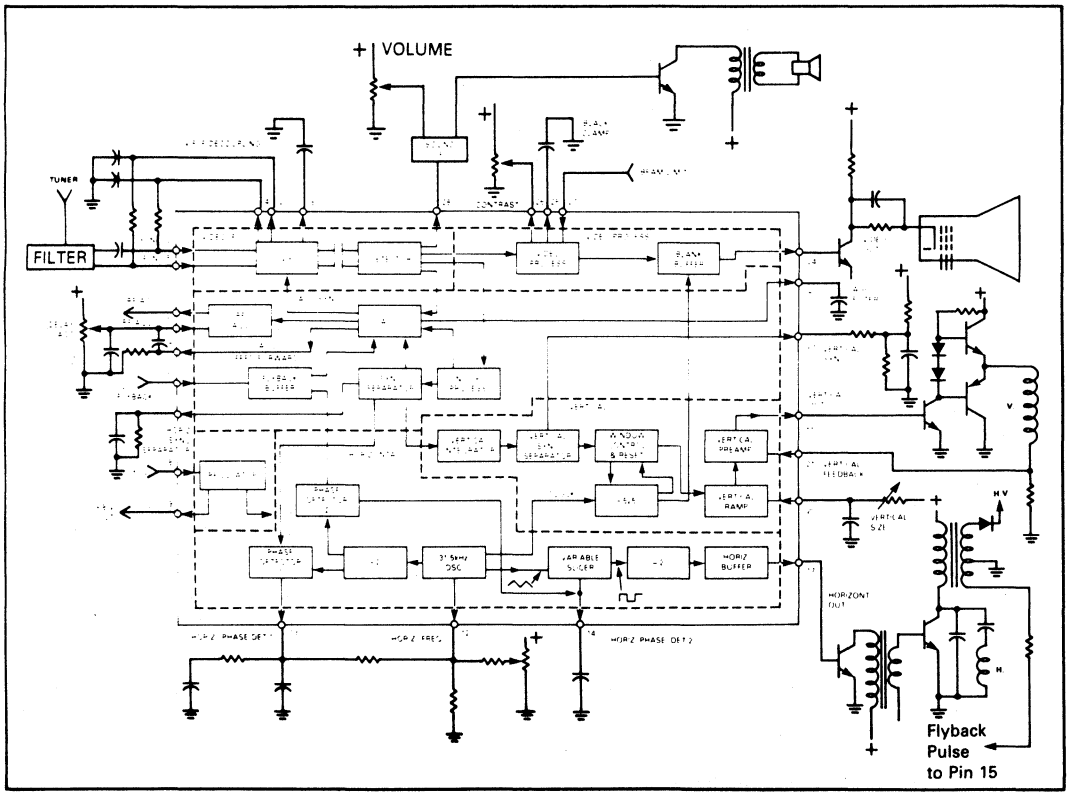


FIGURE 2 — Monomax Functional Block Diagram

application information which will not be repeated in this note. Also recommended is a paper entitled "Monomax — An Approach to the One-Chip TV" by Gerald Lunn and Mike McGinn of Motorola. This can be obtained from the proceedings of the IEEE Chicago Spring Conference on Consumer Electronics, June, 1981, or from Linear Applications, Motorola.

Monomax is not difficult to apply. A functional TV set is virtually assured on the first try. But as anyone closely associated with television design can attest, there are, in every new design, a number of small but objectional problems which stubbornly resist solution. The receiver described here does not represent the "last word", but it is pretty close to production quality, and it includes solutions to some of the most common beginner's problems. In the following text, an attempt will be made to explain component value choices and locations in terms of problems solved or behavior avoided, so that the future experimenter will be alerted.

THE BASIC DECISIONS/POWER SUPPLY

One of the first considerations in a new TV design is whether the set is to be ac/dc (12 Vdc operable) or ac line only. Monomax fits well into either, and has been used in production designs of both types.

Figure 3 shows the architecture of an ac/dc type with all systems operated from 12 Vdc. In this case, the horizontal output stage is of the "boost" type, to minimize horizontal deflection current and make the yoke easier to manufacture. The flyback transformer contains auxiliary windings which provide supply voltages for the video output, picture tube grids, and vertical deflection. Sometimes the boost voltage of 20 to 30 Vdc is used as a power supply for the vertical output. The audio output section is usually a Class B type, operated directly from 12 Vdc. An IC combining the sound IF, detector, and audio output is ideal in this architecture. TDA1190 is an example which fits well with Monomax.

Figure 4 shows the basic power supply structure for the ac line operated type of design. This is the most economical and the most common approach for B&W television in most of the world, and it is the subject of much of this AN. Special thought was given to this type of set in the design of the MC13001 itself. Note that the horizontal oscillator and driver are supplied through high value resistors directly from the rectified power line dc (120 V). Only 4.0 mA are needed into Pin 18 to power the horizontal oscillator system. The balance of the horizontal circuit is also line operated so it is fully operable from the line supply. The horizontal section then produces the 12-14 Vdc for the rest of Monomax (50 mA), and for the tuners, the sound IF, the vertical output, etc., about 150 mA in all. This method avoids the problem of developing 12 Vdc directly from the line; i.e., the waste of power in a linear approach, the extra components for a switch-mode dc-dc converter, or the cost of a line transformer. As in the previous example, the TDA1190 can be used for the entire sound system, but many designers prefer to use a Class A, line operated, discrete output stage, and one of the standard sound IF/detector ICs, such as MC1358, CA3065 or TBA120. This removes the 12 V supply ripple caused by loud low-frequency audio passages, but costs a small audio output transformer. This is the approach presented in the complete receiver in this AN, but it could be easily changed to the single-chip sound system.

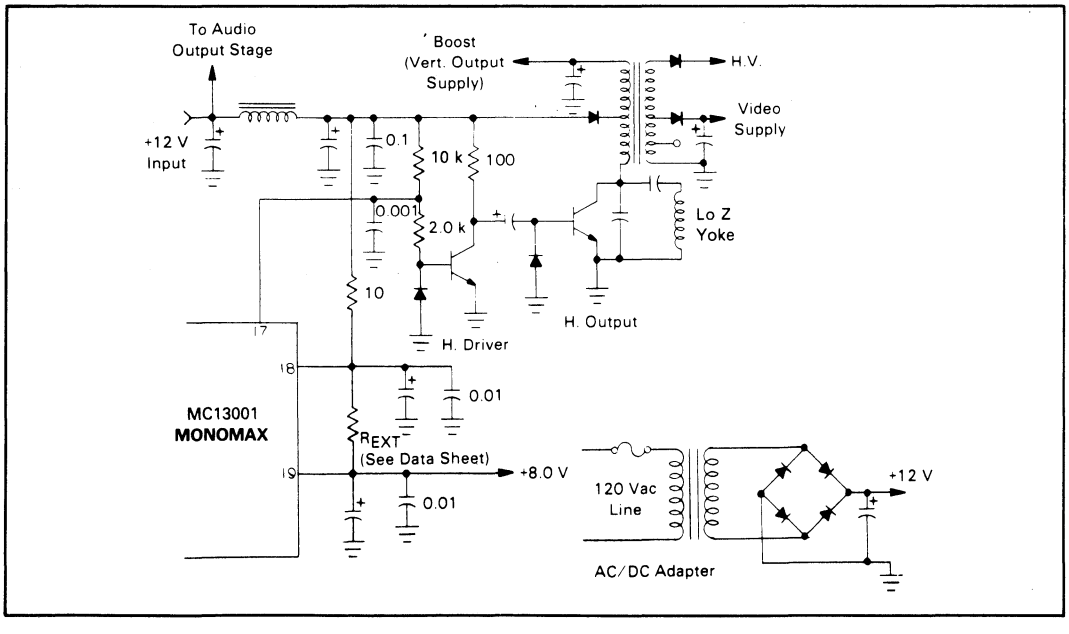


FIGURE 3 — Basic AC/DC Architecture

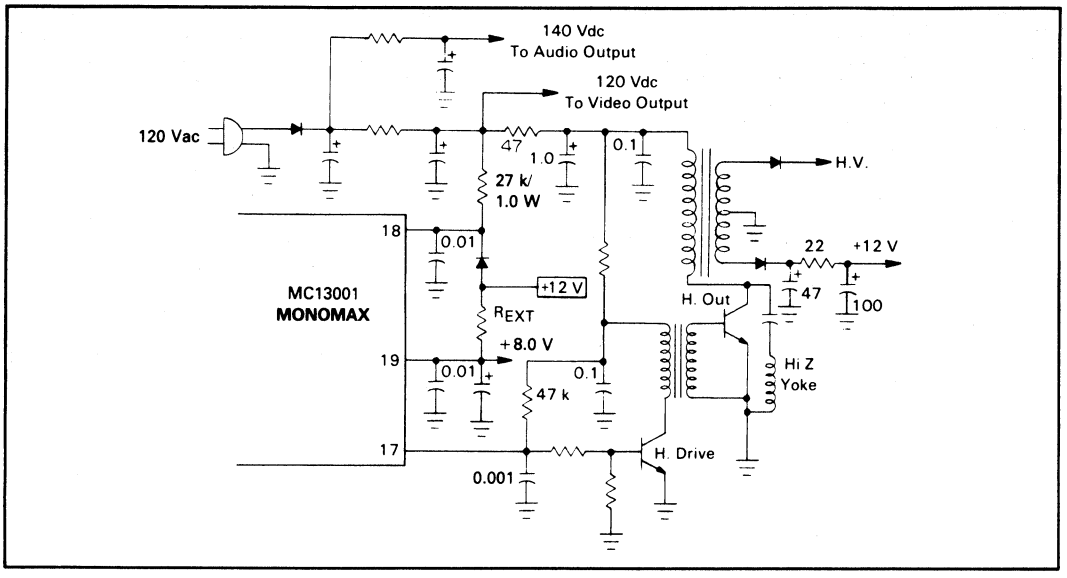


FIGURE 4 — Line Operated Architecture

It is important to use good bypass techniques on all power supplies, not only for low frequencies, but also for RF. It is critical in prevention of faint but objectional vertical lines in the picture, caused by horizontal deflection system waveforms getting into the supplies. Good high-frequency bypasses on Pins 18 and 19, with respect to Pin 16, are essential.

THE IF

The four stage IF in the MC13001 has 80 μV sensitivity, sufficient for excellent overall performance when used with an ordinary tuner and a conventional L/C input bandpass network. It is recommended that the input always be used differentially to reduce the possibility of feedback problems. The differential input capacitance decreases from its normal 5.0 pF, to about 2.0 pF, in the top 10 dB of gain-range of the IF. This can be used to narrow the input L/C filter, at very weak signals, to reduce overall detected noise, and improve picture lock.

If a SAW (surface acoustic wave) filter is used, as in this AN, the above bandpass "walking" technique cannot be used. Furthermore, if a SAW filter is used, an additional fixed gain-preamplifier is needed to overcome the 20 to 25 dB loss thus imposed. Nevertheless, this approach has become increasingly popular with the introduction of low cost SAW filters, because it eliminates a crucial and time consuming production alignment.

There is a steadily increasing supply of SAW filters in the marketplace, so some criteria for choosing the best one for the design are in order. Bear in mind that all of the video selectivity is concentrated in the tuner and the IF input filter in this design. In a B&W receiver, it is important to obtain a good compromise of picture and sound quality with a single selectivity channel. This means keeping color and sound subcarriers low enough to avoid 920 kHz beat generation in the detector, and yet not attenuating the sound so deeply that good sound quieting is irretrievably lost. A well-proven characteristic for achieving this goal is as shown in Figure 5, taken from tuner-mixer input to detector. Of this, some selectivity comes from the mixer-tuned circuits, but most of it is provided by the SAW filter.

Table I shows some available types, data normalized to 0 dB picture carrier. The major difference is the depth of 41.25 MHz. In this regard, the Toshiba F1032U, Kyocera, and the muRata parts are best for B&W design. The mixer-tuned circuits will supply the

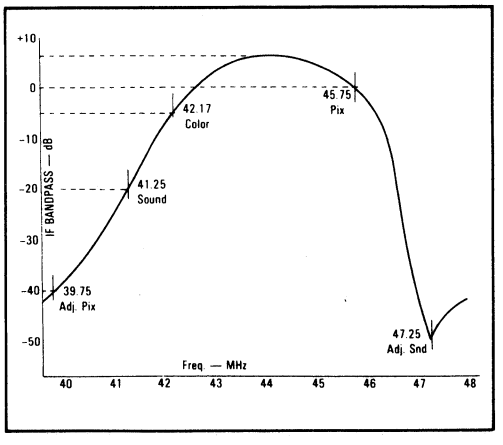


FIGURE 5 — IF Bandpass Characteristic

TABLE 1 — Some Available SAW Filters

Relative Response	Toshiba F1032B	Toshiba F1032U	Toshiba F1032V	Toshiba F1052	Kyocera KAF45MR-MA	muRata SAF45MC 027
39.75 Adjacent Picture	-40	-48	-45	-40	-37	-37
41.25 Sound	-12	-16	-6.5	-25	-18	-19
42.17 Color	+1.0	0	0	0	0	0
Peak	+4.0	+4.0	+4.0	4.0	4.0	4.0
45.75 Picture	0	0	0	0	0	0
47.25 Adjacent Sound	-45	-48	-47	-40	-42	-38
Insertion Loss	-18	-19	-18	-21	-23	-20

additional slight amount of narrowing required. The F1032V part is too wide, and F1052 is too narrow. These are intended for color receiver architectures of different types. The SAW manufacturers loading recommendations should be adhered to closely to prevent ghosts (before and after the picture) caused by capacitive feed-through and/or "triple transit" reflections.

At the input of the MC13001, it is important to use good bypass capacitors on Pins 2, 4 and 6 with respect to Pin 1 of the MC13001. The best value was found to be a straight lead, low-inductance 0.02 μF disc ceramic for reducing the infamous channel 6 beat. Pickup in this area is also a possible source of vertical scan bars in the picture caused by horizontal sweep currents. It is desirable to keep the SAW filter close to Pins 1, 2, 4 and 6. See the PC board layout Figure 14, Also, the IF preamplifier must be kept compact and well grounded to prevent feedback and oscillation with the tuner.

AGC

The AGC system was implemented here essentially as described in the Data Sheet, including the AGC speed-up capacitor between Pins 9 and 10. This keeps the AGC airplane flutter response time fast, even when the signal is strong enough to move the AGC into the tuner control region. The RF AGC delay setting is one of only 4 factory adjustments. Ideally it should be made with a calibrated signal level, but acceptable results can be obtained with a strong off-the-air signal and a switch type attenuator. A discussion of this adjustment is contained in Appendix I.

Remember that AGC loops have a large amount of gain, and **fast** AGC loops, with good airplane flutter performance, are especially vulnerable to deflection currents. Only a few millivolts on the AGC lines from stray fields or ground loops can cause a significant "bar" in the picture. Keep the tuner AGC lead away from yoke leads. The small bypass capacitor on Pin 11 further reduces this problem, and should be placed as close to the MC13001 as possible.

Monomax was designed so that in the strong signal region, "above the delay", the IF gain is held constant while AGC acts upon the RF stage in the tuner. This means that a small amount of IF AGC range may not be accessible in the normal implementation. Optimum setting of the delay pot keeps the RF section at maximum gain for RF signal levels of from <10 μV to 1.0 mV_{rms}, using 40 dB of the IF AGC range. The tuner is not likely to be able to provide more than 40-46 dB of additional AGC, which will accommodate signal levels up to approximately 200 mV_{rms}. This is adequate for the Monopole antenna applications, but certainly doesn't offer a lot to spare. Above this level, the AGC system loses control, the receiver overloads and eventually falls out of sync. One way to improve this, and pick up the remaining 6.0 dB or so of IF AGC capability, is to put a resistor from Pin 11 to Pin 10. The value of the resistor will be about 33 k for delay resistor values shown, but will have to be tailored to the particular tuner used. This can also be accomplished by a resistor from Pin 9 to Pin 10. This, in fact, is the only solution in parts providing negative tuner AGC.

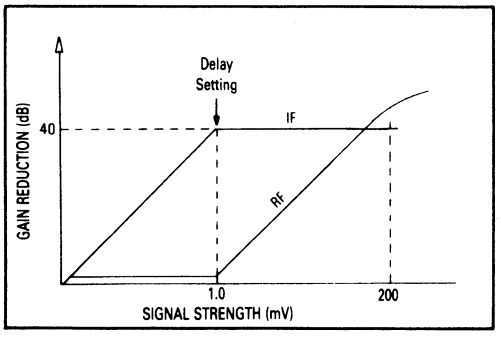


FIGURE 6 — Monomax AGC Behavior

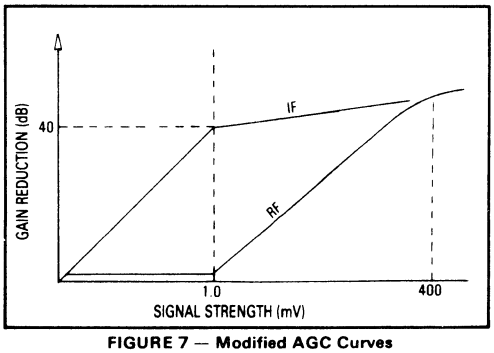


FIGURE 7 — Modified AGC Curves (Resistor from Pin 11 to Pin 10)

THE SYNC SEPARATORS

Composite sync is stripped from noise-cancelled video in a peak detecting sync separator, as shown in Figure 2. The time constants for setting the slice level of the detector are connected at Pin 7. As always, there is the compromise between optimum noise immunity and tilting of the slice level during vertical interval. For best horizontal separation, a short time constant is required. There is also an AGC anti-lockup system which responds to the voltage at Pin 7. It also requires a short time constant. A second, longer time constant can be diode connected to the same pin, to prevent too much charge-up during the vertical interval.

Composite sync is subsequently integrated internally and fed to another amplifier whose emitter is brought out at Pin 23. Satisfactory vertical sync can be obtained (internally) by simply connecting Pin 23 to a divider. Weak signal performance can be improved by using an RC network on Pin 23 to make the separation self compensating, as in the horizontal separator. Also AGC from Pin 9 can be fed to Pin 23 to improve airplane flutter vertical hold.

FLYBACK INPUT

The only flyback pulse input to the MC13001 is at Pin 15. It takes care of keying the AGC, blanking the video output stage, and phase locking the horizontal system. The Pin 15 input is a base-emitter junction, with a reverse polarity diode for protection. The input requirement is for a negative-going pulse of 0.6 mA, but it is best to choose a pulse voltage and series resistor to give about -2.0 mA peak. This will make the effective width be the pulse width near its base.

HORIZONTAL OSCILLATOR/AFC

Monomax contains a really unique group of features in this area: dual-loop; variable-loop-gain (bandwidth) on the first (sync) PLL; externally adjustable phasing in the second PLL; simple flyback pulse input, requiring no ramp generation. These are described in detail in the data sheet, and will not be repeated here.

Shown in Figure 8(a) are the first PLL components as presented in earlier publications, and in 8(b) a new variation which has been implemented in this receiver. This very simple change retains the dual time constant on the phase detector. The improvement is the 13 k/22 k divider which sets a 5.0 V point for the return of the longer time constant filter. Since 5.0 V is the reference level in the oscillator, it is also the operating voltage at Pin 12, and at Pin 13 when in-lock. The benefit, then, is that the 0.47 μF doesn't have to charge up, so there's very little frequency pulling during power-up or power-down. This reduces audible chirps and momentary stresses due to long cycles on the horizontal output device. Also the picture locks-in quickly, which is highly desirable with fast warm-up picture tubes.

Note that the proper setting of the horizontal hold control occurs when no average current flows through the 390 k resistor, either to, or from, the oscillator. A simple alignment procedure is to set the average Pin 12 to Pin 13 voltage to zero by adjusting the hold control, when locked to a standard broadcast signal, using a high impedance voltmeter.

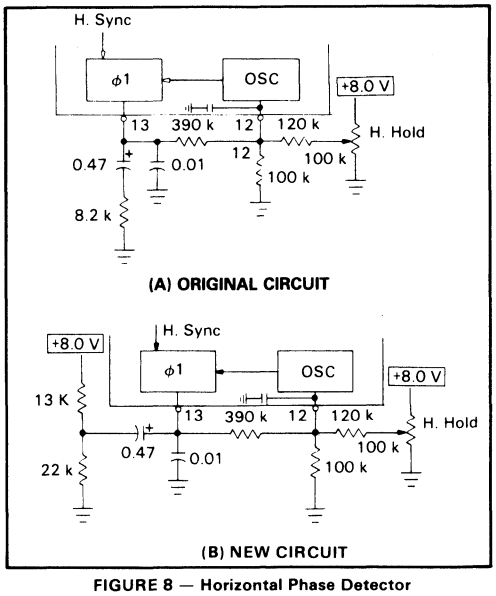


FIGURE 8 — Horizontal Phase Detector

The second horizontal phase detector compares the flyback output phase with that of the oscillator, and develops a proportional dc voltage, which is filtered at Pin 14. This dc voltage then sets the slice level on the oscillator ramp to produce the output timing desired. See Figure 9(a). Picture phasing can be adjusted slightly by a high value resistor on Pin 14 to +8.0 V or ground. A 220 k to +8.0 V will move the picture about 2.0 μs to the left. A 220 k to ground will move it 2.0 μs to the right.

Another application of Pin 14 provides a method of changing the duty cycle of the horizontal output waveform from Pin 17. Normally, the desired waveform would be 50%. This has been assured in the MC13001 by operating the slicer at 31.5 kHz. This permits output phasing correction **without** changing duty cycle, as shown in Figure 9(a). In some receivers, when large amounts of dc power are drawn from the flyback, the "on" time of the horizontal output may have to be more than 50% of the cycle. This can be accommodated by feeding back some driver collector signal to the second phase detector filter, as shown in Figure 10. This imposes alternate slice levels and hence, the desired change of duty cycle. Some tentative values for a set configured like the one in this AN are given in Figure 10. This was not actually used in the final design, because it wasn't needed. It is supplied here as a reference for future designs having more power drain from the horizontal output. Bear in mind that the driver collector voltage would be much lower in the 12 Vdc receiver architecture mentioned earlier, requiring much different values to implement this idea. A practical limit of control by this technique is about a 60/40 duty cycle. The 0.001 capacitors on Pin 17 and the driver base are to "soften" waveform edges, to reduce their radiation into signal circuits.

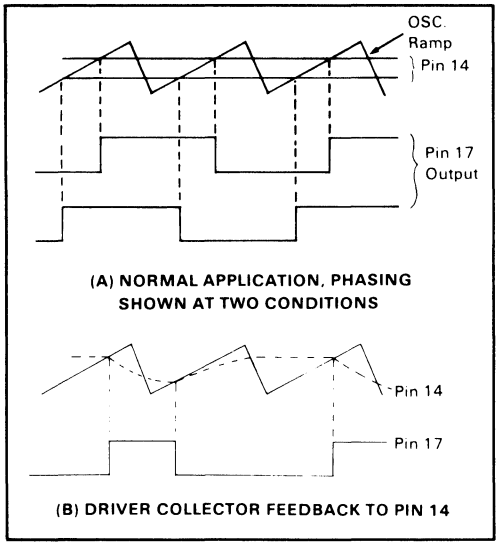


FIGURE 9 — Second Phase Detector Slicer

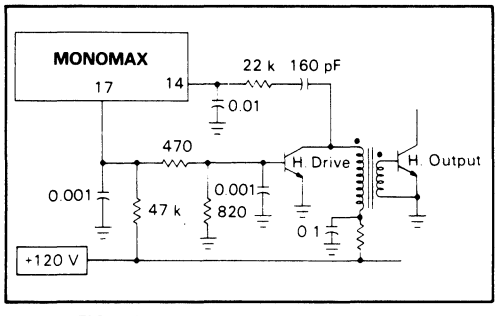


FIGURE 10 — Driver Feedback For Extended Horizontal Output "On" Time

THE VERTICAL SYSTEM

Aside from all of the sophistication of the countdown vertical system within the Monomax chip, what remains to be accomplished outside of the device is fairly conventional. At Pin 20, there is an external capacitor, charged from a high voltage, to produce a good linear ramp. It is discharged within the chip, usually by vertical sync, but sometimes by the countdown circuit when sync is momentarily absent. It is important for the capacitor to be a good stable low ESR type and to be located close to Pin 20 and grounded as closely as possible to Pin 1 to avoid pickup of horizontal sweep which could hurt interlace.

The approximately 1.5 $V_{p\text{-}p}$ waveform on Pin 20 is inverted and buffered to Pin 22 to drive the external output circuit. In the receiver design in this AN, a fairly conventional vertical output stage has been used. An **optional** linearity control has been added, because many customers like to have one, but also because it permits using a smaller coupling capacitor for the yoke. The smaller coupling capacitor saves money and reduces picture bounce, but introduces some curvature which must be compensated. Feedback to Pin 21 provides overall output stage linearization and prevention of deflection current change with temperature. It is also a handy place to feedback a variable parabolic waveshape for linearity control, as shown in Figure 11.

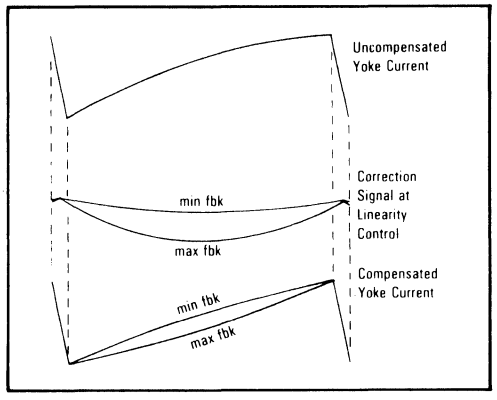


FIGURE 11 — Vertical Linearity Control

THE SOUND SECTION

The buffered video detector output at Pin 28 is a wideband signal used for sound take-off. A ceramic sound take-off filter and detector "tank" were chosen to eliminate alignment steps. The MC1358 is a popular, multi-sourced, FM IF, detector and dc volume control. It can be used with conventional L-C circuits or the ceramic devices shown here. The L-C application costs less in piece parts, but has a higher manufacturing cost in assembly and alignment.

Keep in mind that a limiting IF produces a wide spectrum of 4.5 MHz harmonics. The sound IF grounds should be kept together and returned to Pin 1 by a single path as shown in the copper layout of Figure 14. Also it is a good idea to keep the input of the sound IF IC close to Pin 28 to reduce radiation of video IF harmonics, generated in the video detector, from getting back to the tuner or IF input.

In the receiver described here, an ac volume control has been used. A potentiometer is placed between the MC1358 detector output, Pin 8, and the post amplifier input, Pin 14. The dc volume control, Pin 6, is grounded for maximum volume. If the volume control is to be mounted some distance away, and deflection pickup is likely, then the dc volume control could be the better choice. This can be done by ac coupling Pin 8 to Pin 10, and placing a variable 50 k pot from Pin 6 to ground. The disadvantage is that the control contour is less predictable in the dc control configuration. It is, nonetheless, a production proven method.

THE VIDEO OUTPUT

Pin 24 provides up to 1.4 V, black-to-white video drive, black level clamped, with a widened and amplified blanking pulse added. This is sufficient to drive a single stage common-emitter video output transistor. A dc voltage of 0 to 5.0 V applied to Pin 26, varies the black-to-white amplitude at Pin 24 from 1.4 V to 0.1 V without changing the absolute black level of the output voltage. Beam current limiting can also be used to control maximum brightness. This is accomplished by circuit shown in Figure 12. As beam current increases, the H.V. winding current flowing in the 39 k resistor, pulls the Pin 27 voltage down. When Pin 27 falls below about 1.0 V, the contrast begins to be reduced. This circuit was not used in the complete receiver in this AN, for reasons which will be explained shortly.

The black level clamp capacitor on Pin 25 is usually shown connected to ground. It can also be connected to +8.0 V to cause the screen to be blanked for about 1 second after turn-on. This permits the scan systems to stabilize before the picture becomes visible. Note: If the brightness control design window is set too high, the raster may still be visible during start-up.

There are several approaches to sound trapping in the video output stage: series tuned L-C from the video output base to ground; parallel tuned L-C in the video output emitter; or a ceramic shunt element in the video output base circuit. All of these can be detrimental to picture quality, if not carefully done. The ceramic element is in keeping with the "no alignment" philosophy successfully implemented thus far, so there was a strong motivation to use it. However, shunt loading Pin 24, if too severe, causes considerable distortion of high-frequency detail, due to excessive loading of the video driver. This can be reduced by adding a resistor between Pin 24 and the trap, and by returning the bottom of the trap to the video output stage emitter. The compromise chosen is shown in the full schematic. Again, it is good to keep these parts close to Pin 24 to reduce radiation of video detector products back to the tuner and IF front end.

The video output circuit can take many forms. Monomax was designed to accommodate full dc coupling, as described earlier. However, many TV designers, and users, don't like full dc coupling, because it sometimes seems to go too black, creating the suspicion that some information is hidden. Also, a directly coupled video output to picture tube cathode usually requires a negative voltage for at least one of the grids for proper set-up at high contrast settings. Finally, fully dc coupled designs are harder to protect from power-off flash or spot burn.

For these reasons the receiver described in this AN was a partially dc coupled type. This puts the brightness control in the cathode circuit, removes the need for the brightness limiting configuration, and makes spot/flash prevention easier. (The diode and electrolytic in G1 are for this latter purpose).

In the video output stage emitter, some dc set-up from the +12 V supply has been used to adjust the output dc level, to minimize overall dissipation. Also some additional vertical blanking has been fed through a diode, from the top of the vertical yoke. This blanking will be accomplished in the IC internally in later Monomax devices.

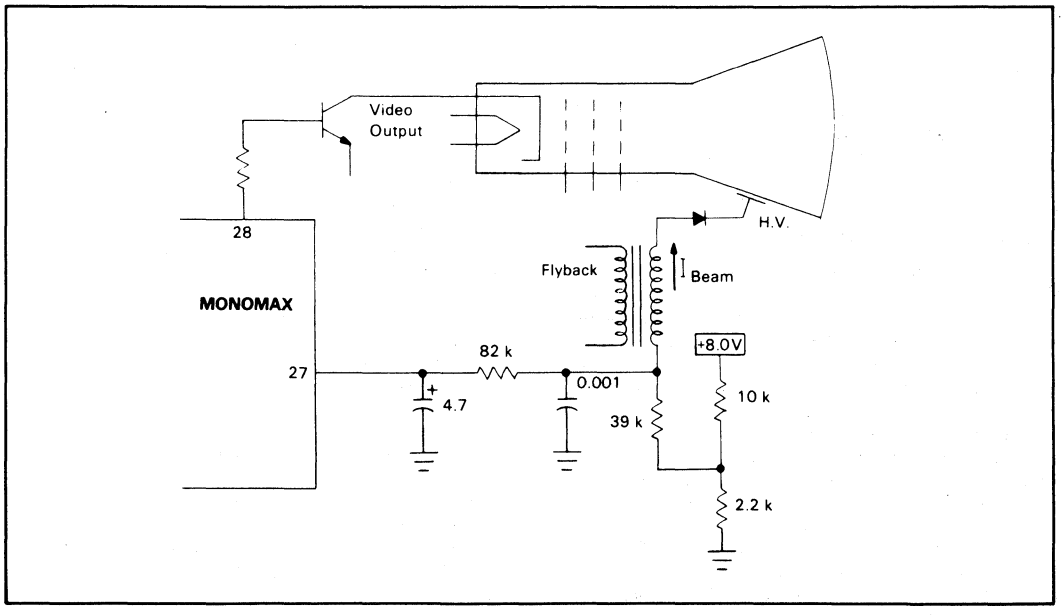


FIGURE 12 — Beam Current Limiting

APPENDIX I — AGC DELAY ADJUSTMENT

Ideally, a known antenna signal level of 1.0 mV (300 Ω balanced) or 500 μV (75 Ω unbalanced) is supplied to the tuner input. This signal level corresponds to the threshold of "snow" in the picture, for most receivers. With this signal level, the AGC delay pot is turned until the RF AGC voltage just begins to rise, and then is backed off slightly. The picture should be snow-free. If the RF AGC is permitted to rise, the picture will start to show some snow, which therefore represents less than optimum overall performance. If the setting is backed-off too much, the delay may be too large and mixer overload may occur at stronger signals.

The correctness of this setting should be checked at weaker and stronger signals. At weaker signals, say 6.0 dB down, it should not be possible to improve the picture noise by resetting the RF Delay. At stronger signal, say 40 dB stronger, there should be neither snow or overload evident in the picture, although the distance between these two conditions, as a function of delay setting, may be very narrow. The AGC system should automatically avoid these troubles. It may be necessary to make a slight compromise to avoid overload, which may produce a slight amount of snow in the 1.0 mV picture.

The above compromises can be achieved successfully without calibrated signals, with just a switchable attenuator and a strong signal. Starting at strong signal, note the available AGC Delay setting range between picture overload and snow. Using the switched attenuator, reduce the signal strength and make sure that neither problem appears. If necessary tweak the Delay, but don't move outside the original range. Eventually the picture will get snowy, but the control will only be able to make it snowier. Setting it to the optimum (just barely) should still be within the noted range.

APPENDIX II — COMPONENT & CONSTRUCTION DETAILS

In order to make the enclosed PC board pattern easy to use, the following components are recommended: Remember that these are pertinent to **this** design architecture and this specific design. Many variations are possible with a little redesign work.

Flyback — Gold Star Type 154-028A with self-contained H.V. rectifier. Certainly, substitution is possible, but very careful attention to pin-outs and taps is required. The primary is, of course, a 120 Vdc type, which corresponds to about 800 $V_{p\text{-}p}$ positive pulse at Pin 2. Pin 3 is a negative going pulse of 35 $V_{p\text{-}p}$ and Pin 7 is a negative-going pulse of about 120 $V_{p\text{-}p}$. The H.V. terminal, which is internal in the above model, would be a positive going pulse of about 12 $kV_{p\text{-}p}$. Very little flexibility can be permitted on these values. Be careful to watch pin-outs and horizontal polarity.

Yoke —Gold Star Type 153-020A for 90° 12" — 20 mm neck picture tube. It requires approximately 1.0 $A_{p\text{-}p}$ in both horizontal and vertical windings to give proper overscan in the 90° tube at 10-11 kV. This means a horizontal (saddle) winding of about 3.4 mH and a vertical (toroid) winding of approximately 3.0 Ω, 10 mH. Numerous substitutions are available, but the above values must be adhered to for this set architecture.

Horizontal Output Transistor — The board was designed for a TO-3 type, such as a BU205, BU204, or MJ12003. A plastic TO-220 type MJE12007 will do the job with some mechanical revision. The important parameters are $V_{(BR)CEX}$ = 1300 V and I_C = 2.0 A. A small amount of heat sinking, such as a U channel with 2 flags of 1 square inch each is recommended. A mica or Thermalloy isolator is suggested to reduce shock hazard to the experimenter. If an ac/dc design is contemplated, as referred to back in Figure 3, a lower voltage, higher current part like BU806 will be required for the horizontal output, along with a different yoke and flyback.

Vertical Output Transistors — It is possible to "get by" with a TO-92 complementary pair, such as MPS6560 and MPS6562, or the new, tall TO-92, MPSW01 and MPSW51. However, the author's opinion is that these operate too hot, with dissipation approaching 1 watt, each, worst case. Recommended alternatives include D40E1 and D41E1 in the TO-202, or TIP29 and TIP30 in TO-220. No heat sink is required. The devices need only $V_{(BR)CEO}$ = 30 V and good h_{FE} at 1.0 A.

Video Output Transistor — For the load value shown in this design, a case 152 uniwatt, such as MPSU10, is best. The 300 V $V_{(BR)CEO}$ is not needed, but the device must be "small geometry"; i.e., high f_T and low C_{cb} to preserve picture resolution. A tall TO-92 or even an MPSA43, TO-92, can be used if the collector load is increased to 6.8 k, but some picture quality will be lost.

Audio Output Section — The transformer should be approximately 30:1 turns ratio, capable of handling 1 watt into 8.0 Ω. The output transistor should be set up at about I_Q = 12-14 mA, and should be capable of 1.5 W continuous dissipation. A TO-220 type MJE2360T, mounted on at least 3 square inches of aluminum is suggested.

H. Driver Stage — In the prototype receiver, the available driver transformer had only about 12:1 turns ratio. This necessitated a large wattage dropping resistor to provide the rather low-voltage, high-current primary waveforms. It would be better to obtain a transformer of 30:1 or so, to permit a more efficient driver stage. The 4.3 k/2.0 W resistor could then be reduced considerably. In either case a TO-92 driver, type MPSA42, is a good choice.

SUMMARY:

Figures 13 and 14 provide the copper pattern for the PC board and the component locations. Note that signal input circuits are compact and grounded near Pin 1. Subsequently these and all other circuits are connected to the central ground at Pin 16, without being interconnected beforehand. The full receiver schematic is given in Figure 15.

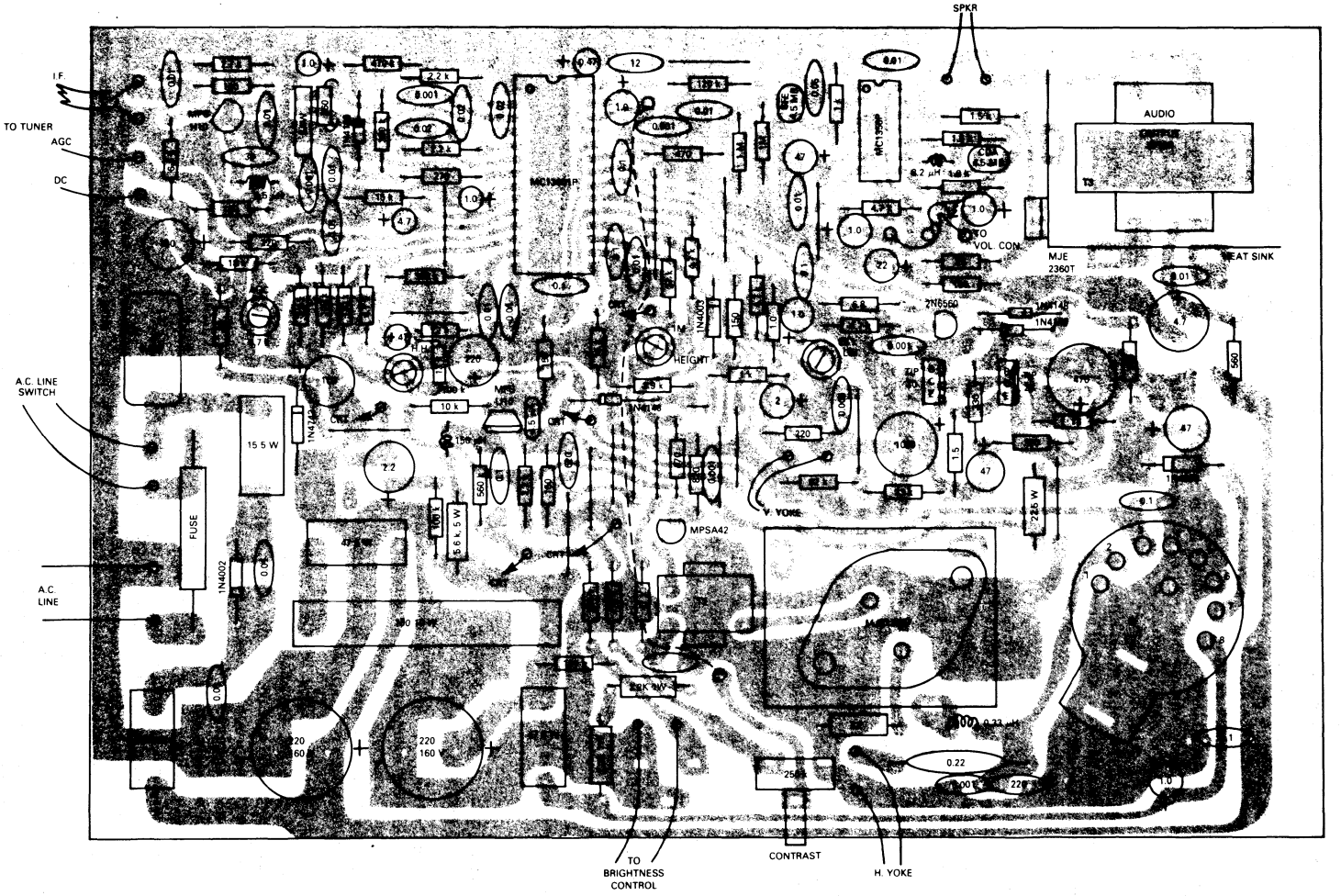


FIGURE 13 – Component Layout (not full size)

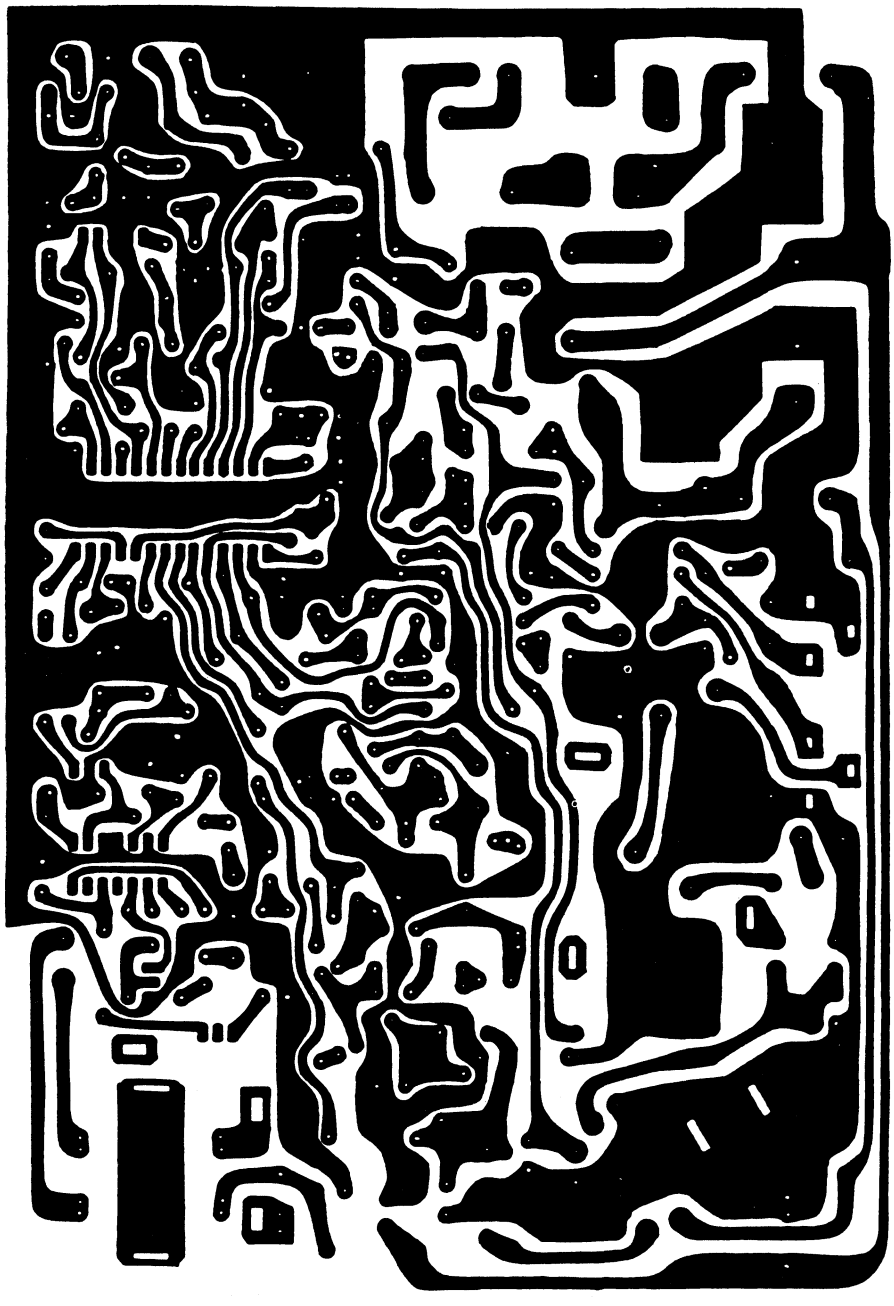


FIGURE 14 – Printed Circuit, Copper Side (not full size)

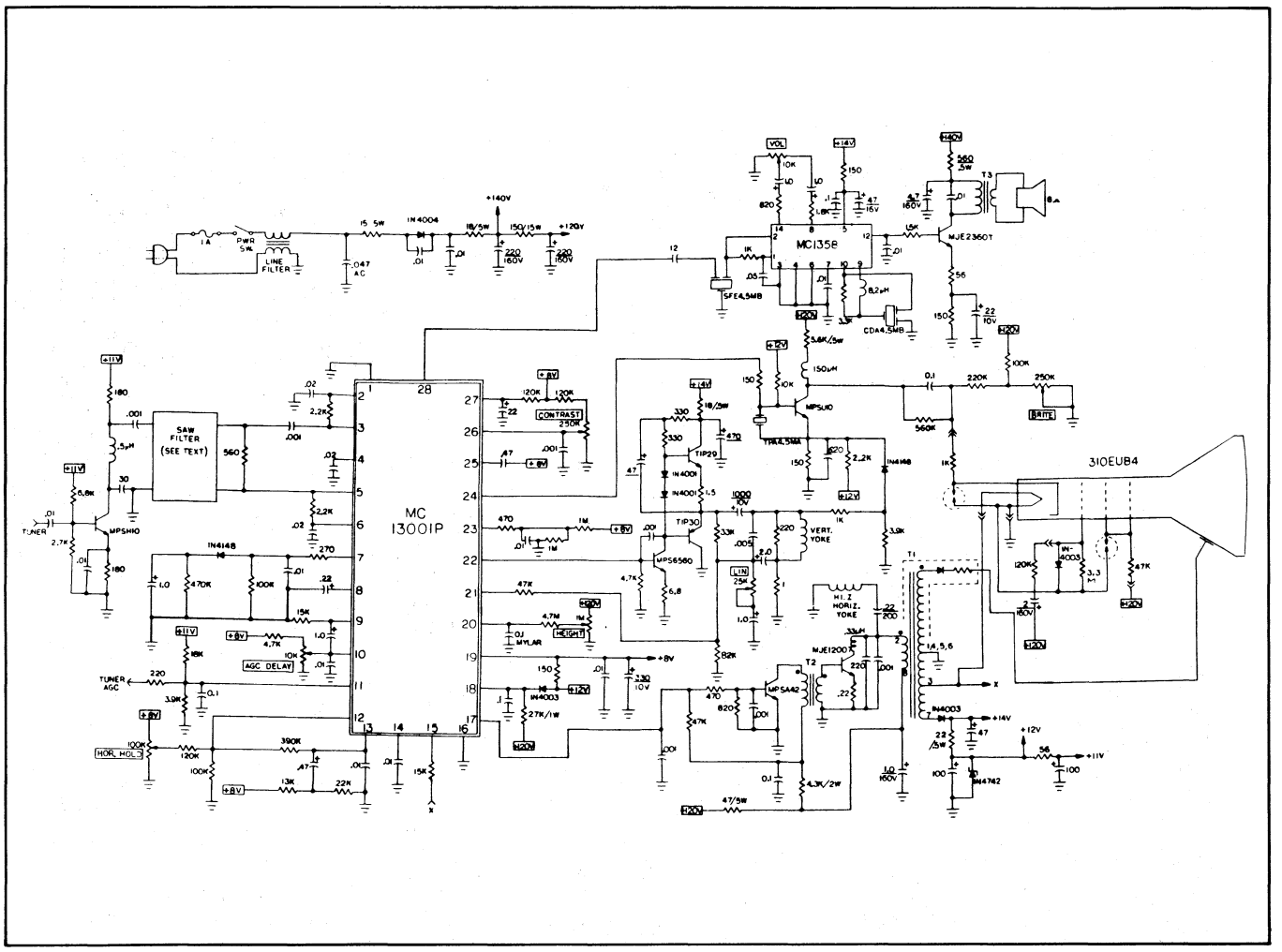


FIGURE 15 — Complete Receiver Schematic

UHF PREAMPLIFIER CENTERS ON BUDGET DUAL-GATE GaAs FET

Prepared by
Gary Barbari, Applications Engineer, RF Products
and
Steve Lazar, Principal Staff Engineer, Advanced RF GaAs Development*

INTRODUCTION

This note describes the design, construction and performance of a 400–512 MHz preamplifier utilizing Motorola's GaAs dual-gate field-effect-transistor.

In two-way communications, the ability to receive a transmitted signal depends on the systems' signal-to-noise ratio (S/N). The S/N can be improved by increasing the output power of the transmitter; by increasing the gain of the antenna; or by improving the sensitivity of the receiver. The first two solutions could be quite expensive. A low noise preamplifier would be an economical solution for improving the receiver system noise figure.

DESIGN

The main criteria in the selection of a transistor for a preamplifier is low noise figure coupled with sufficient gain to minimize the second stage contribution to the system noise figure. The Motorola MRF966 is a GaAs dual-gate field-effect transistor designed for UHF applications.

Designing impedance transformation networks requires S-parameter and noise figure data at the operating frequencies. Table 1 lists the required information for the MRF966.

Parameter	f = 400 MHz	f = 450 MHz	f = 500 MHz
S11	0.99 ∠12°	0.98 ∠14°	0.98 ∠15°
S21	1.60 ∠165°	1.59 ∠163°	1.59 ∠162°
S12	0.004 ∠83°	0.004 ∠84°	0.004 ∠85°
S22	0.97 ∠7°	0.97 ∠8°	0.97 ∠9.4°
Γms	0.87 ∠14°	0.81 ∠20°	0.81 ∠16°
Γml	0.8 ∠9°	0.8 ∠11°	0.76 ∠21°
NF_{min} dB	0.9	0.9	1

TABLE 1
S-Parameter and NF Data @
V_{DS} = 5 V, I_{DS} = 10 mA

The MRF966 was matched by means of slug tuners to obtain the minimum noise figure. The optimum source (Γms) and load (Γml) impedances were then measured on a network analyzer.

The slug-tuned circuit used in this procedure is illustrated in Figure 1.

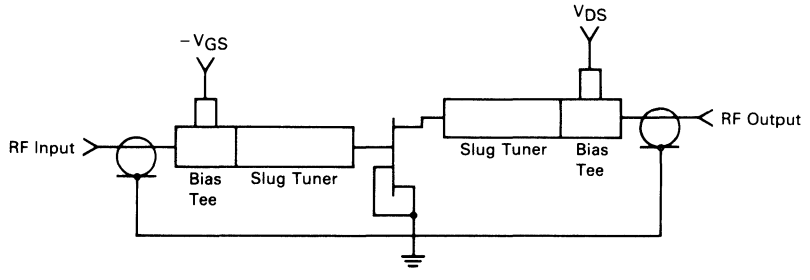


FIGURE 1 — NF Test Circuit

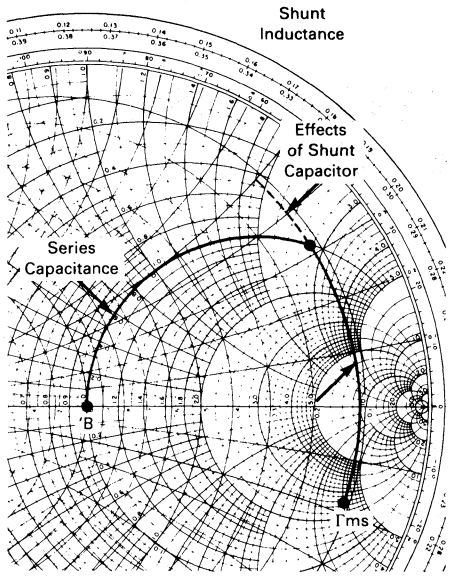


FIGURE 2 — Input Matching Network

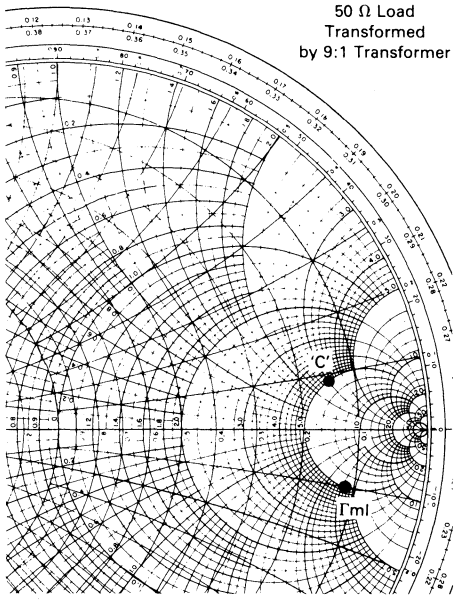


FIGURE 3 — Output Matching Network

The network required to transform the optimum impedances to the required 50-ohm source and load was designed using a Smith Chart. The input matching network is shown in Figure 2. At the input of the preamplifier it is necessary to transform the 50-ohm input impedance to the optimum source reflection coefficient (Γms). Taking the values from Table 1 for 450 MHz an input matching circuit can be designed using a series

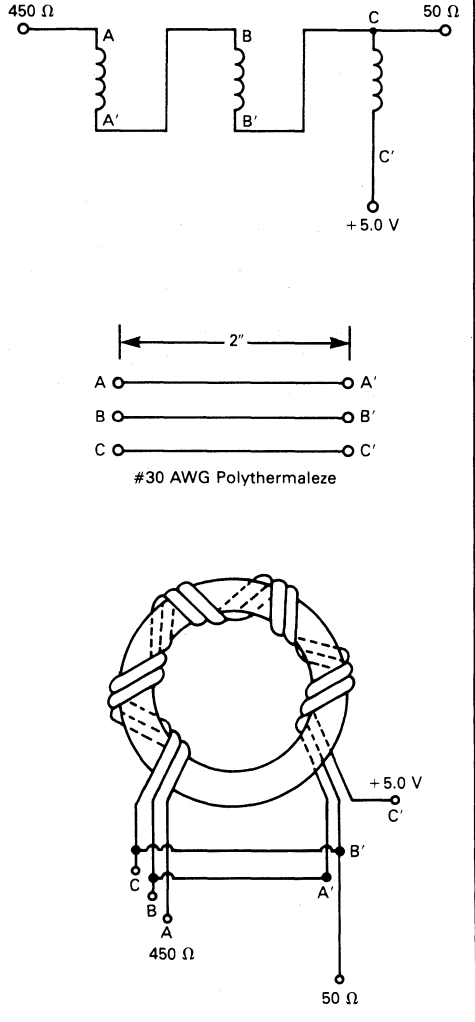
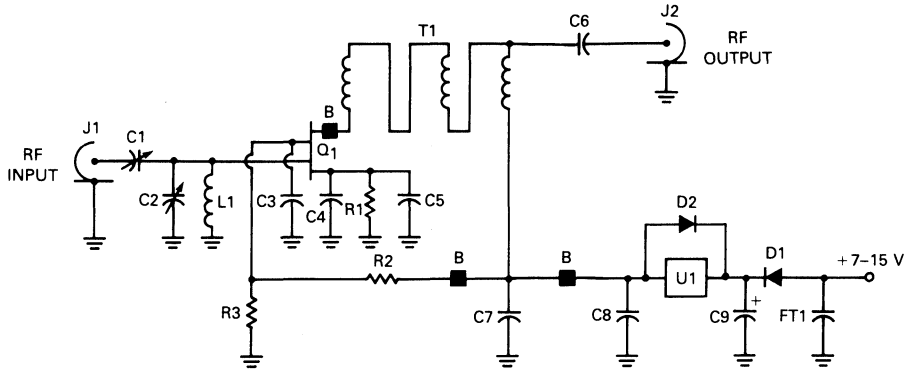


FIGURE 4 — 9:1 Transformer

capacitance, shunt inductance, and shunt capacitance. Starting at the input of the device (Γms), the shunt inductance moves the impedance to the value of 50 + j145 ohms (point A); (the shunt capacitor is used to fine tune the inductor along the constant admittance circle). Finally the series capacitance transforms point A to the desired 50 + jO ohms center (point B). The required reactance value for the three components can be obtained directly from the Smith Chart. From Figure 2 the shunt inductance moves the vector along the path to position A. This move requires an X_L of 104.2 ohms. Therefore the shunt inductor has a value of 37 nH at 450 MHz. The shunt capacitor needs to be variable from 0.8–10 pF to accommodate variations between devices. The series capacitance rotates the input impedance from 50 + j145 ohms to the center of the chart (50 + jO) ohms at point B. Therefore, the required capacitive reactance is j2.9 or j145 ohms which leads to a value of 2.4 pF at 450 MHz. A variable capacitor (0.8–10 pF) will also be used here to fine tune the preamplifier for a specific frequency over the 400–512 MHz band.

The output matching circuit could be designed using a shunt capacitor with a series inductor, but a more convenient matching technique involves a 9:1 transformer. This simple matching technique although not presenting the optimum load reflection coefficient (Γ_L) to the MRF966 provides improved stability at the expense of slight gain reduction. The 50 ohm impedance of the load is transformed to a value of 450 + j150 (point C, Figure 3). The materials needed to construct the transformer are inexpensive and readily available. The lumped element form of the transformer and the winding procedure are shown in Figure 4.

Source self-bias is used utilizing a 100 Ω resistor. The resistor will set the operating current at approximately 20 mA. Decoupling the source and Gate 2 is accomplished using 1000 pF and 56 pF chip caps. Gate 2 is positively biased using a simple voltage divider circuit. A low positive voltage on the gate will lower the noise figure and increase the power gain. The complete preamplifier schematic and the parts list are shown in Figure 5.

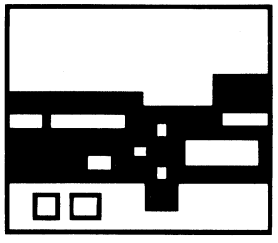


C1, C2 — 0.8–10 pF
C3, C4, C7 — 1000 pF Chip Capacitor
C5 — 56 pF Chip Capacitor
C6 — 470 pF Chip Capacitor
C8 — 0.1 MFD Mylar
C9 — 10 MFD Tantalum
FT1 — 1000 pF Feed Thru
R1 — 150-Ohm 0.125 Watt
R2 — 12-Kilohm 0.125 Watt
R3 — 7.5-Kilohm 0.125 Watt
L1 — 2 Turns No. 16 AWG 0.375" Diameter
T1 — 4 Turns No. 30 AWG, Indiana General Core, F2062-1-Q1
U1 — MC78L05
D1, D2 — 1N4001
Q1 — MRF966
J1, J2 — SMA-Type Female Connectors
B — Ferroxcube Bead 56-590-65

FIGURE 5 — Schematic Diagram

CONSTRUCTION

The preamplifier is assembled on a 43 mm (1.7") x 38 mm (1.5") double-sided circuit board. The board material is 1.5 mm (0.062") Teflon-Fiberglass. A 1:1 photomaster of the top side of the board is shown in Figure 6. The under side of the board is used as a ground plane and the copper foil is not removed. A 0.2" clearance hole, centered between the device mounting tabs, is drilled to allow the MRF966 to fit flush with the pc board. This location is shown on the photomaster. The four sides of the board are wrapped with thin copper foil and then soldered on both sides.

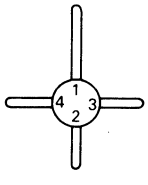


Top of PCB

FIGURE 6 – Photomaster (not full size)

Handling precautions should be taken before mounting the MRF966. A grounding bracelet should be worn at all times when handling the device. A well grounded soldering iron should be used when soldering the FET. Before mounting, cut the gate, drain and source leads in half.

Place the MRF966 (Figure 7) flush with the pc board (with marking face up) and solder the leads to the conductive tabs located on the board. Using tweezers, place the decoupling bypass chip capacitors as close to the device as possible. Installing the bias circuitry is very straightforward. The locations of the components are shown in Figure 8. Construction details of the 9:1 transformer are shown in Figure 4. Solder the Coil (L1) directly onto the Gate 1 lead and ground the other end. The placement of the coil depends upon the size and shape of the variable input capacitor (refer to Figure 8).



1 = Drain
2 = Source
3 = Gate 1
4 = Gate 2

FIGURE 7 — Pin Configuration

Do same for the input shunt capacitor. Solder the 450 Ω wire on the transformer (Wire A in Figure 4) directly to the drain lead. All of the components should be on the board.

The preamplifier was built using "open chassis" construction as shown in Figures 8 and 9 from brass extrusion stock. This technique was chosen to allow visibility of the various components. SMA style connectors were utilized although other types are suitable at this frequency.

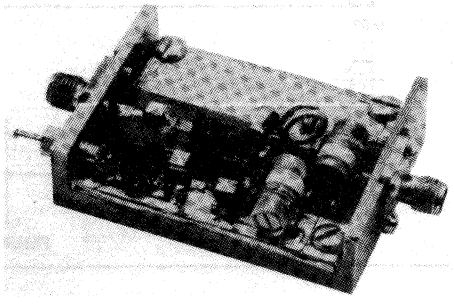


FIGURE 8

TUNE-UP PROCEDURE

Apply a voltage, between 7 and 15 volts, to the dc input and check for 5 volts at the output of the voltage regulator and at the drain lead. Now adjust capacitors C1 and C2 for maximum gain. By using this maximum gain tuning procedure, a gain of about 20 dB with a noise figure of 0.8 dB at 450 MHz is obtained. To obtain a minimum noise figure (measured to be about 0.5 dB with an associated gain of 19 dB at 450 MHz) a commercial noise and gain analyzer is recommended, such as the HP8970A or Eaton 2075 Noise Figure Meters. With the noise analyzer in place, adjust C1 and C2 for best noise figure. The variable capacitors on the input of the preamplifier allow precise tuning at any frequency in the 400–512 MHz band.

PERFORMANCE

The preamplifier was tuned for minimum noise figure at 430 MHz and 480 MHz using the HP8970A noise figure meter. The voltage was set at 12 V and the operating current was found to be approximately 20 mA. The variable capacitors were adjusted to obtain a noise figure of 0.5 dB at 430 MHz and a value of 0.6 dB at 480 MHz. The gain at noise figure and noise figure optimum versus frequency curves are shown in Figures 10 and 11. Figure 12 shows the input and output return loss versus frequency for the preamplifier tuned at 430 MHz, while Figure 13 shows the same parameters at 480 MHz.

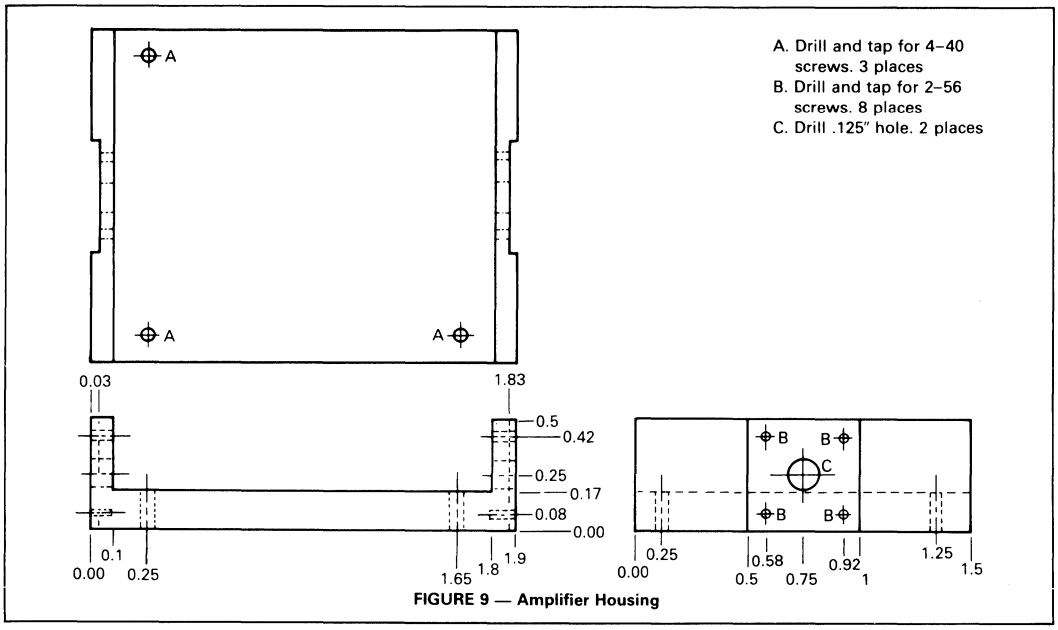


FIGURE 9 — Amplifier Housing

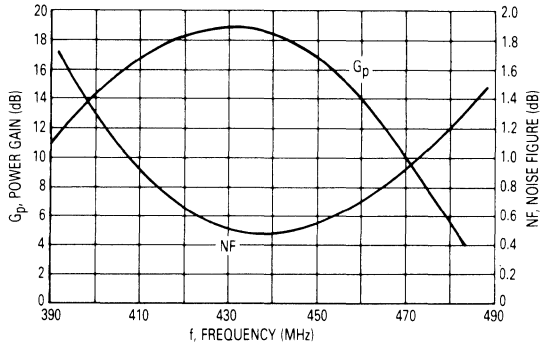


FIGURE 10 — Gain at Noise Figure and Optimum Noise Figure versus Frequency (Tuned @ 430 MHz)

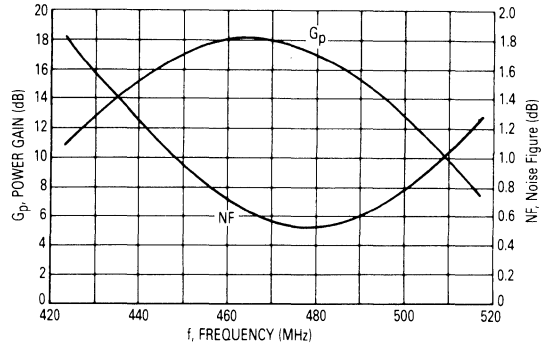


FIGURE 11 — Gain at Noise Figure and Optimum Noise Figure versus Frequency (Tuned @ 480 MHz)

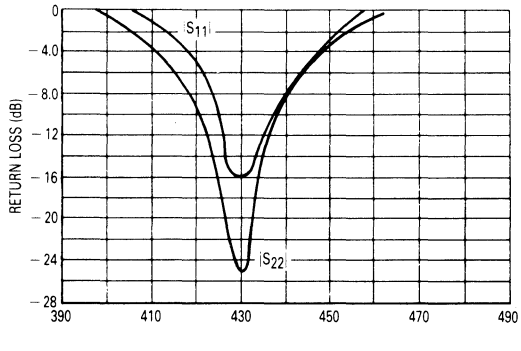


FIGURE 12 — Input and Output Return Loss versus Frequency (Preamp Tuned @ 430 MHz)

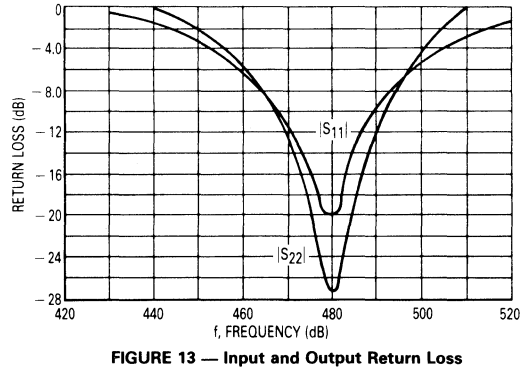


FIGURE 13 — Input and Output Return Loss versus Frequency (Preamp Tuned @ 480 MHz)

APPLICATION OF THE MC1377 COLOR ENCODER

by Ben Scott and Marty Bergan
Linear I.C. Applications, Tempe, AZ

The MC1377 is an economical, high quality, RGB encoder for NTSC or PAL applications. It accepts red, green, blue, and composite sync inputs and delivers IVpp composite NTSC or PAL video output into a 75 ohm load. It can provide its own color oscillator and burst gating, or it can be easily driven from external sources. Performance virtually equal to high cost studio equipment is possible with common color receiver components. The following note is intended to explain the operation of the device and guide the prospective user in selecting the optimum circuit for his needs.

PREFACE

Since this device has applications in color cameras, video games, video text and computer generated graphics, it may attract potential users who are skilled in computer architecture, but not familiar with the encoding of color television. Perhaps they have spent extensive hours viewing graphics on a full R, G, B wideband monitor. This preface is intended to caution that PAL or NTSC encoding, no matter how rigorously executed, will cause some degree of picture degradation. The process of encoding involves some bandwidth reduction, which means loss of high frequency detail, and it creates the possibility of spurious picture patterns, due to coding and decoding system limitations. The original standards were established about 25 years ago and will probably be in use for many years to come. It is not the objective here to detail these standards as many references[1-4] are available. Appendix A shows pictorially why some loss of information and detail is incurred.

The MC1377 is capable of encoding NTSC and PAL to virtually studio standards. It also can be used for very low cost applications where appropriate, with some compromises to picture quality. It can readily drive the 75Ω input of a composite video monitor, or be used to drive a UHF or VHF modulator so that color television receivers can be used.

CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the color encoder. The three color inputs at Pins 3, 4, and 5 are matrixed to produce chrominance envelopes, (R–Y) and (B–Y), and luminance (–Y) by the standard NTSC/PAL formulae:

$$Y = .59G + .30R + .11B$$
$$R\text{–}Y = .70R - .59G - .11B$$
$$B\text{–}Y = .89B - .59G - .30R$$

Texts on the NTSC system will show that studio modulation is done on a different set of orthogonal axes called I and Q. Also they will point out that I is a somewhat wider bandwidth than Q. The MC1377 does not permit the circuit designer this refinement, but it should be noted that very few monitors or receivers contain any circuitry to process the unequal bandwidths. (This is the only compromise of standards in the MC1377 which cannot be circumvented by application means.) Rotation of the coordinate system from I/Q to (R–Y)/(B–Y) does not constitute any further compromise whatsoever, and it makes the encoding formulae for PAL and NTSC the same. It also aligns (B–Y) with the axis of the NTSC color burst, for internal circuit simplicity and system accuracy.

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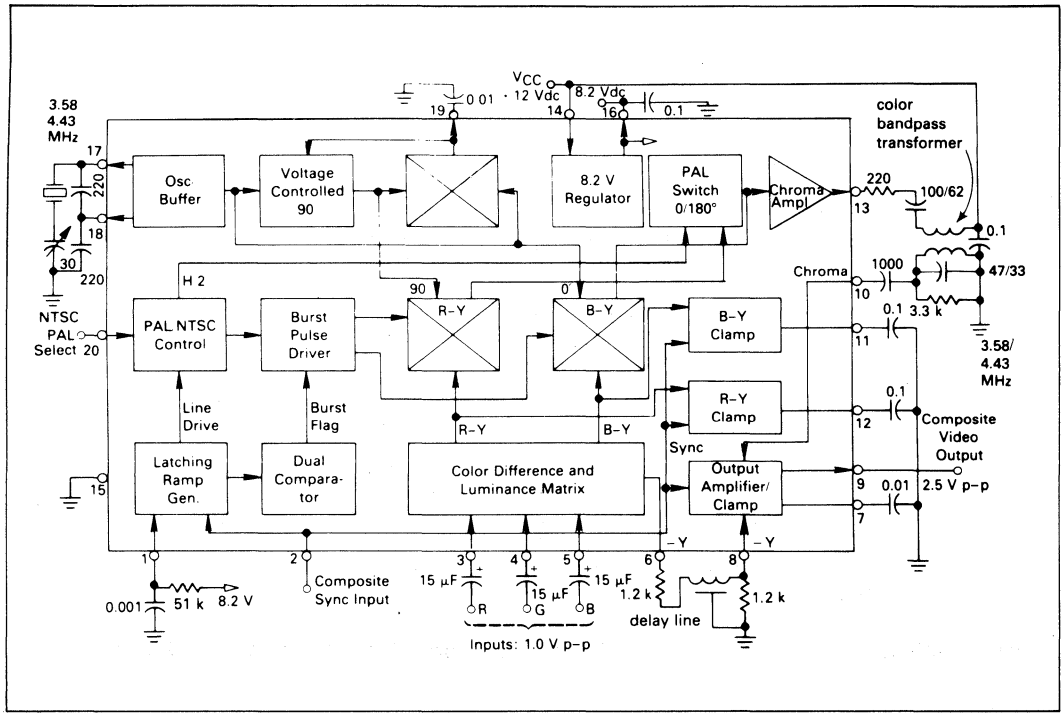


FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT

The (B–Y) and (R–Y) signals drive two double balanced (double sideband suppressed carrier) modulators whose carriers are set at 0° and 90°, respectively. In the NTSC mode, the outputs of these chroma modulators are added to produce composite chroma. Burst envelope or "burst flag" is applied to the (B–Y) modulator in the negative direction to produce a burst pulse at a reference angle of 180°. Composite chroma is amplified and buffered to Pin 13 (to permit external bandwidth control as desired) and is then fed back into the IC at Pin 10 to be combined with the luminance component. The luminance signal is also "looped out" from Pin 6 to Pin 8 to permit insertion of a delay line to match the delay incurred in the chroma channel due to bandwidth reduction. The passive components used in the chroma and luma channels are like those used in the most common implementation of color television receivers.

In PAL mode, burst flag is driven into both modulators equally to produce a 225°/135° burst phase. The output phase, or polarity, of the (R–Y) modulator output is alternately switched from 90° to 270° on successive horizontal lines, before being combined with (B–Y), which remains at 0°. The switching of the modulator polarities for PAL mode is driven by the latching ramp generator through the PAL/NTSC control. This control allows PAL switching when Pin 20 is open, and stops when Pin 20 is grounded. The PAL phase can be detected at Pin 20 and controlled by means of external logic. The PAL phase can be reversed by sensing when Pin 20 is high and Pin 1 is low, and momentarily pulling Pin 20 to ground with an external switch.

The color subcarrier source for the modulators can be implemented by free running the on-chip crystal oscillator, or by external drive into Pin 17, or by a combination of both methods. The common collector Colpitts oscillator is completed by connecting a standard tv receiver color crystal and capacitor divider as shown. The oscillator is followed by a 90° phase shifter to provide the quadrature signal to the (R–Y) modulator. The direct oscillator output is taken as reference 0° and is fed directly to the (B–Y) modulator.

The composite sync input at Pin 2 performs three important functions: it provides the timing (but not the amplitude) for the sync in the final output; it drives the black level clamps in the modulators and output amplifier; and it triggers the ramp generator at Pin 1, which produces burst envelope and PAL switching signal.

The ramp generator at Pin 1 is a simple R – C type in which the pin is held low until the arrival of the leading edge of sync. The rising ramp function passes through two level sensors — the first one starts the burst pulse and the second stops it. Since the "early" part of the exponential function is used, the timing provided is relatively accurate from chip-to-chip and assembly-to-assembly. Fixed components are usually adequate. The ramp continues to rise for more than ½ of the line in-

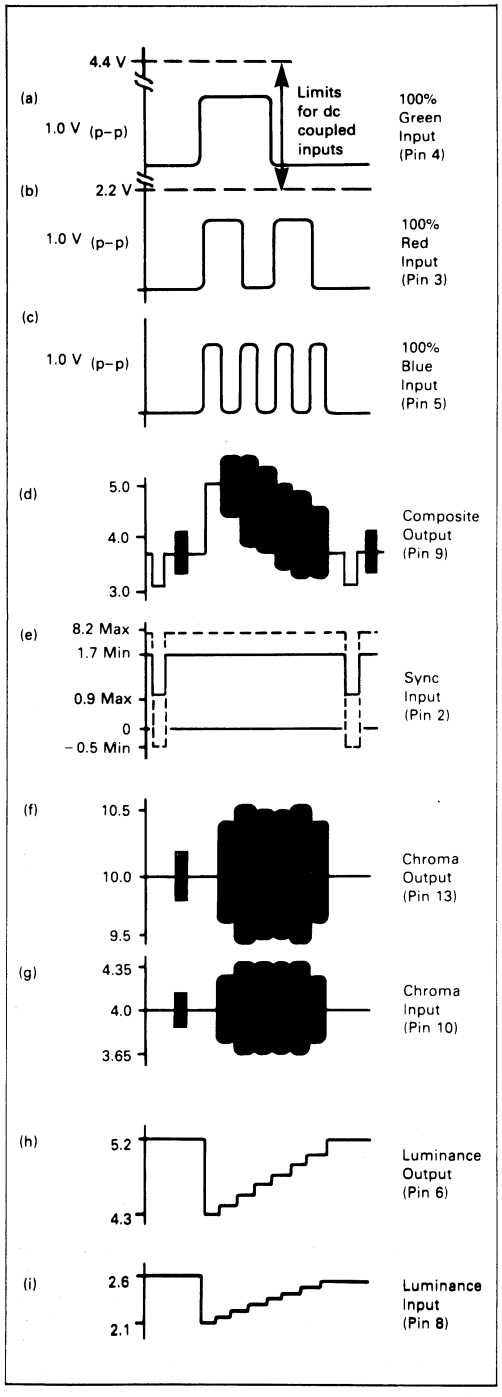


FIGURE 2 — SIGNAL VOLTAGES (Circuit Values of Figure 1)

terval, thereby inhibiting burst generation on "half interval" pulses on vertical front and back porches. Burst is also inhibited if sync is wider than the time required for the ramp to reach the sense levels, as is the case during vertical sync. The ramp method *will* produce burst on the vertical front and back "porches" at full line intervals. In most applications, this discrepancy from standards will not cause any problem. If it is objectionable, and if a proper burst envelope signal is available, then it can be injected into Pin 1 directly. Another method, suitable for either PAL or NTSC, will be described later.

STANDARD INPUT LEVELS

The signals into Pins 3, 4, and 5 should each be 1 V_{pp} for standard, fully saturated, color output levels as shown in Figure 2. The levels are important because the IC will generate a predetermined 0.6 V_{pp} sync and 0.6 V_{pp} burst at the output, and it will need 1.0 V_{pp} input signals to produce the corresponding full luminance and chrominance amplitudes. The inputs are internally biased and present a 10 k input impedance. The 15μF input coupling capacitors are sufficient to prevent tilt during the 50 or 60 Hz vertical period. Input signals can be dc coupled (to save the cost of the capacitors), provided that the signal levels are between 2.2 V and 4.4 V at all times. It is essential that the portion of each input which occurs during the sync interval represent black for that input, because it will be clamped to reference black in the color modulators and the output stage. A refinement such as a difference between black and blanking level must be incorporated in the RGB input signals if required.

THE SYNC INPUT

As shown in Figure 2, the sync input can be varied over a wide latitude, but will require bias pull-up from most sync sources. The important requirements are that during the period *between* sync pulses, the voltage must be above 1.7 V and below the 8.2 V internal regulator. During sync, the voltage (negative going) must extend below +0.9 V and should not exceed −0.5 V (to prevent substrate leakage in the IC). For PAL operation, correctly serrated vertical sync is necessary to properly trigger the PAL divider. In NTSC mode, simplified "block" vertical sync can be used but the loss of proper horizontal timing may cause "top hook" or flag waving in some monitors. An interesting note is that composite video can be used directly as a sync signal, provided that it meets the sync input criteria.

THE LATCHING RAMP (BURST FLAG) GENERATOR

The recommended application is to connect a close tolerance (5%) 0.001 μF capacitor from Pin 1 to ground and a resistor of 51 k or 56 k from Pin 1 to the 8.2 V internally regulated supply (Pin 16). This will produce a burst pulse of 2.5 to 3.5 μs in duration, as shown in Figure 3. As the ramp on Pin 1 rises toward the charging voltage of 8.2 V, it passes first through a burst "start threshold" at 1.0 V, then a "stop threshold" at 1.3 V, and finally a ramp reset threshold at 5.0 V. If the resistor is reduced to 43 k, the ramp will rise more quickly, producing a narrower and earlier burst pulse (starting about

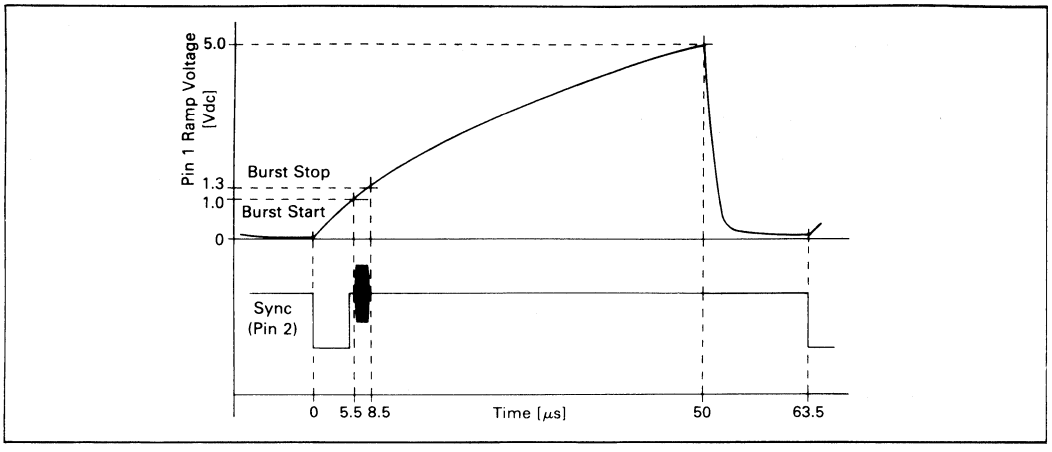


FIGURE 3 — RAMP/BURST GATE GENERATOR

0.4 μs after sync and only about 0.6 μs wide). The burst will be wider and later if the resistor is raised to 62 k, but more importantly, the 5.0 V reset point may not be reached in one full line interval, resulting in loss of alternate burst pulses.

As mentioned earlier, the ramp method does produce burst at full line intervals on the vertical porches. This is not rigorously correct for studio applications. If external burst flag is available, a positive pulse of between 1.0 V and 1.3 V (absolute value) can be applied to Pin 1 in the NTSC mode. This approach must be handled carefully, because a square pulse smaller than 1.0 V will not trigger the burst generator, and a square pulse larger than 1.3 V will shut off the burst generator almost before it starts. This direct injection technique does not provide the ramp to operate the PAL flip-flop. Another method, suitable for either PAL nor NTSC, is shown in Figure 4. It requires a "vertical drive" pulse, starting at the leading edge of vertical blanking and as wide as the interval where burst is *not* wanted (usually 9 line intervals). The extra transistor and diodes in the circuit add an abrupt step at the beginning of each line ramp which *inhibits* burst generation.

THE COLOR REFERENCE OSCILLATOR/BUFFER

As stated earlier in the general description, there is an on-board common collector Colpitts color reference oscillator with the transistor base at Pin 17 and the emitter at Pin 18. When used with a common low-cost tv crystal and capacitive divider, about 0.65 V_{pp} will be developed at Pin 17. The adjustment of oscillator frequency can be done with a series 30 pF trimmer capacitor over a total range of about 1.0 kHz. Oscillator frequency should be adjusted for each unit, keeping in mind that most monitors and receivers can pull in 1200 Hz.

If an external color reference is to be used exclusively, it must be continuous. The components on Pins 17 and 18 can be removed, and the external source capacitively coupled into Pin 17. The amplitude at Pin 17 should be between 0.5 V_{pp} and 1.0 V_{pp}, either sine or square wave.

It is also possible to do both; i.e., let the oscillator "free run" on its own crystal, and also be capable of being overridden from an external source. An extra coupling capacitor of 50 pF from the external source to Pin 17, and a signal of 1.0 V_{pp} was adequate with the limited experimentation attempted.

VOLTAGE CONTROLLED 90°

The oscillator drives the (B–Y) modulator and a voltage controlled phase shifter which produces an oscillator phase of 90° ± 7° at the (R–Y) modulator. If it is necessary to adjust the angle to better accuracy, the circuit shown in Figure 6 can be used.

Pulling Pin 19 up will increase the (R–Y) to (B–Y) angle by about 0.25°/μA. Pulling Pin 19 down reduces the angle by the same sensitivity. The nominal Pin 19 voltage is about 6.3 V, so the 12 V supply is best for good control, even though it is unregulated. In most situations, the result of an error of 7° is very subtle to all but the most expert eye. For effective adjustment, the simplest approach is to apply RGB color bar inputs and use a vectorscope. A simple bar generator giving R, G and B outputs is shown in Appendix D.

RESIDUAL FEEDTHROUGH COMPONENTS

As shown on the MC1377 data sheet (and in Figure 2 (d), the composite output at Pin 9 for fully saturated color bars is about 2.6 V_{pp}, output with full chroma on the largest bars (cyan and red) being 1.7 V_{pp}. The typical device, due to imperfections in gain, matrixing, and modulator balance, will exhibit about 20 mV_{pp} residual color subcarrier in both white and black. Both residuals can be reduced to less than 10 mV_{pp} for the more exacting applications. The black imbalance is primarily in the modulators and can be nulled by sourcing or sinking small currents into clamp Pins 11 and 12 as shown in Figure 7. The nominal voltage on these pins is about 4.0 Vdc, so 8.2 V is capable of supplying a pull up source. (Pulling Pin 11 down is in the 0° direction, up is 180°. Pulling Pin 12 down is in the 90° direction, up is 270°.)

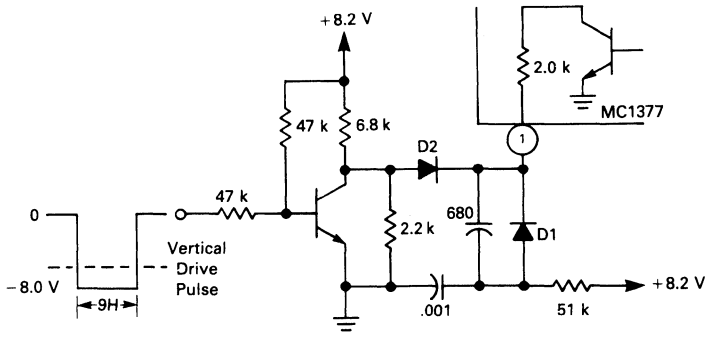


FIGURE 4(a) — VERTICAL PERIOD BURST INHIBITOR

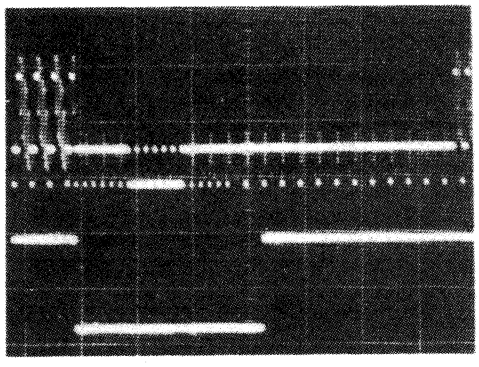


FIGURE 4(b) — VERTICAL INTERVAL WHEN MC1377 STANDARD RAMP CIRCUIT IS USED

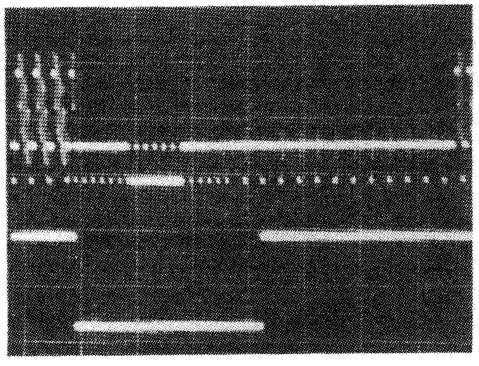


FIGURE 4(d) — VERTICAL INTERVAL WITH BURST INHIBITOR CIRCUIT

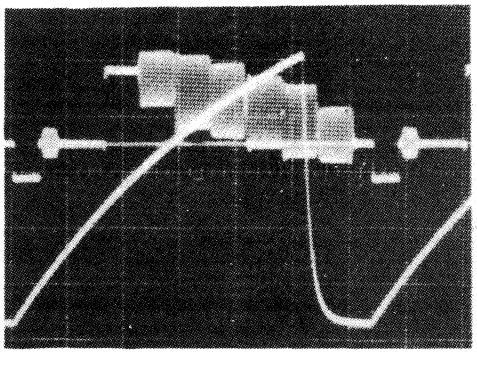


FIGURE 4(c) — STANDARD RAMP CIRCUIT

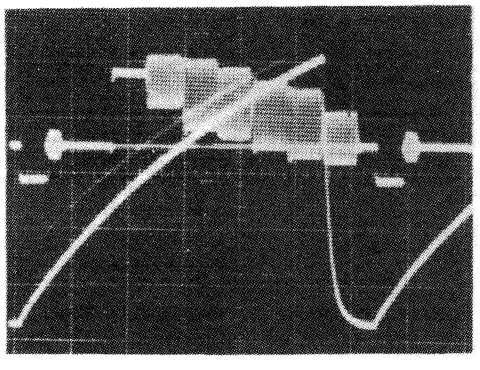


FIGURE 4(e) — BURST INHIBITOR RAMP CIRCUIT
(NOTE FAINT RAMP CAUSED BY VERTICAL DRIVE PULSE)

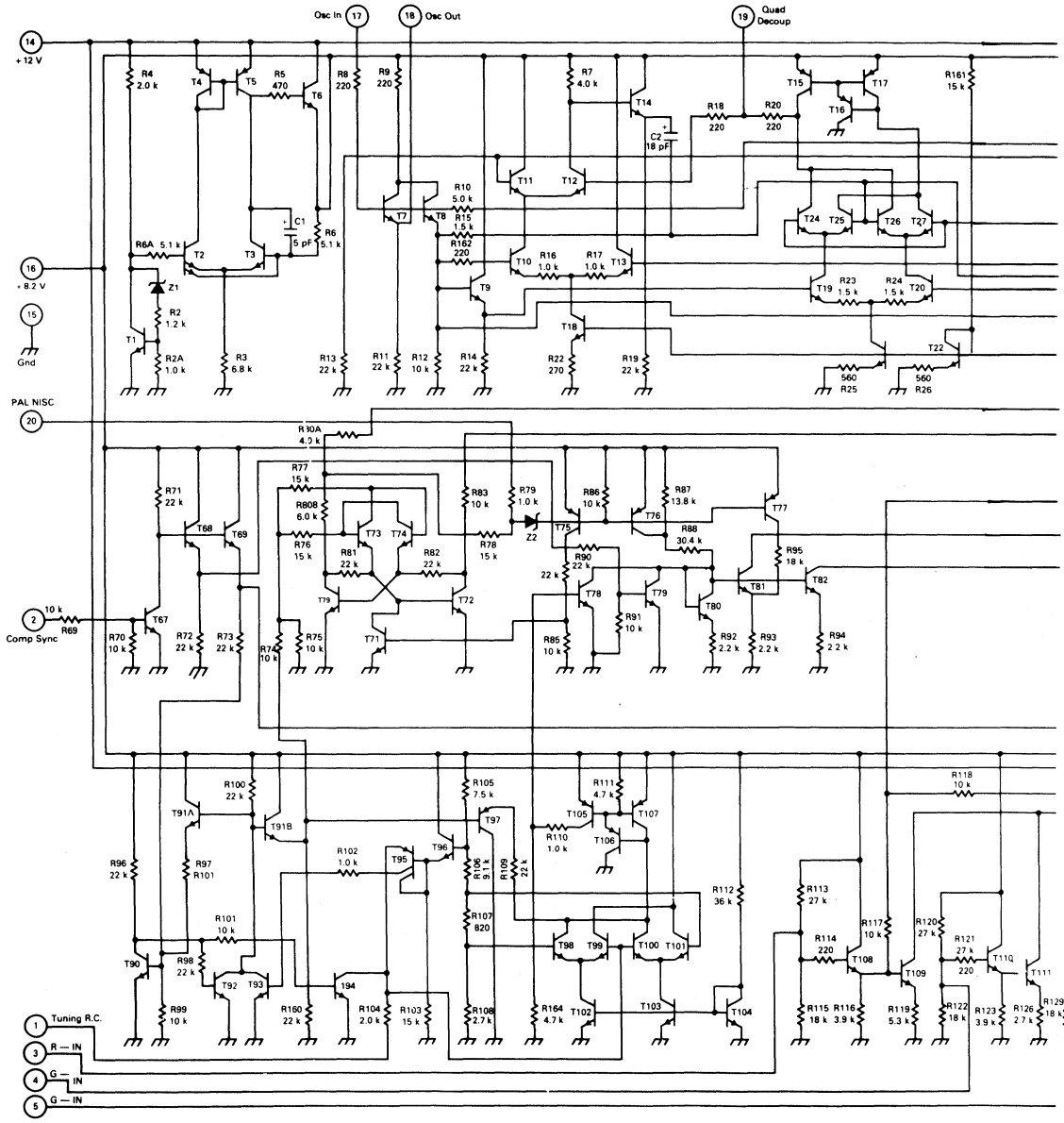
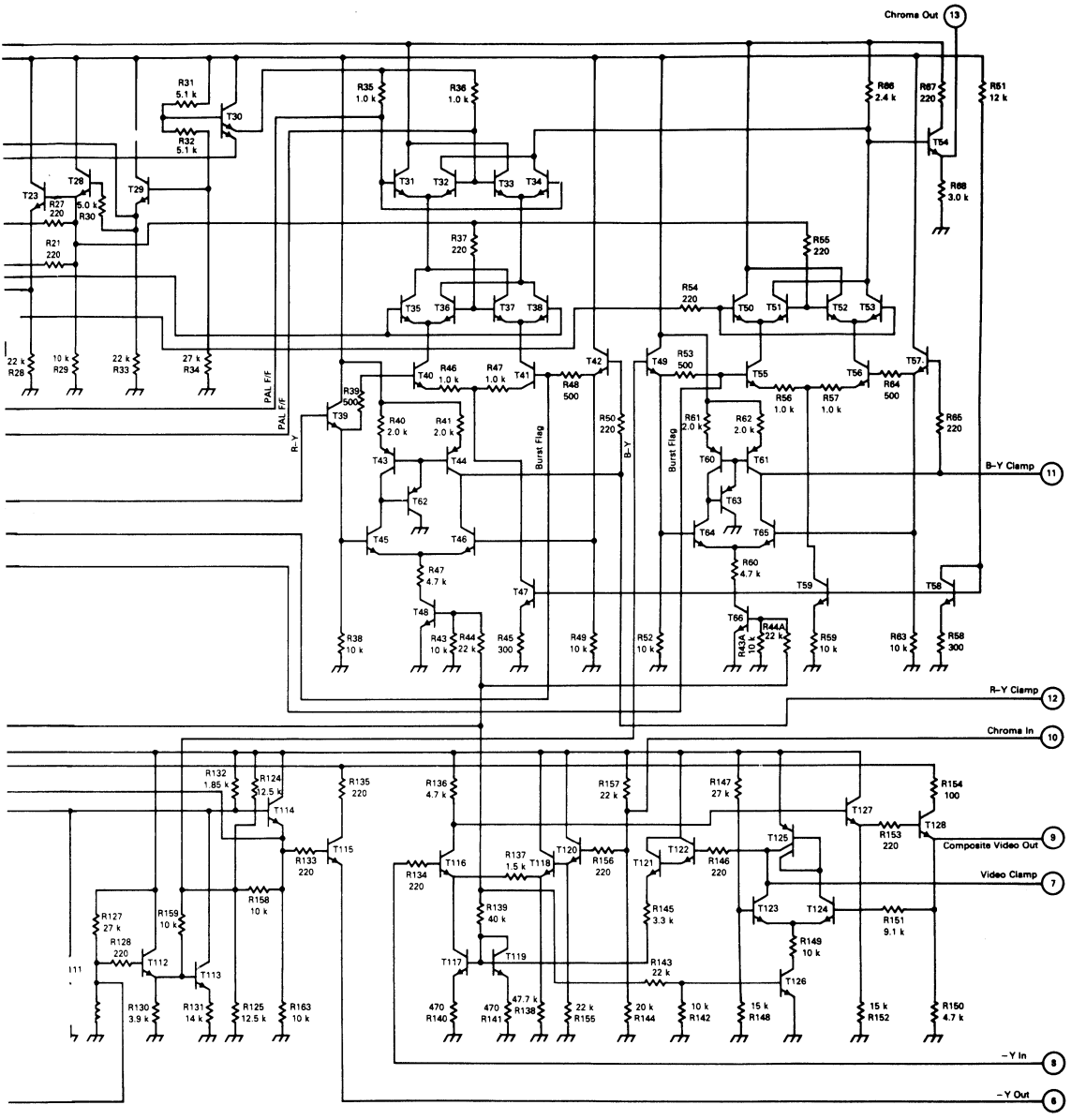

Osc In
Osc Out
Quad Decoup
+12 V
+8.2 V
Gnd
PAL NISC
Comp Sync
Tuning R.C.
R — IN
G — IN
G — IN

FIGURE 5 —



INTERNAL SCHEMATIC

Any direction of correction may be required from part to part. (Note that pulling Pin 11 up can produce a residual carrier on the horizontal back porch which is the same phase as burst, and can result in an almost normal color display even with burst not present.)

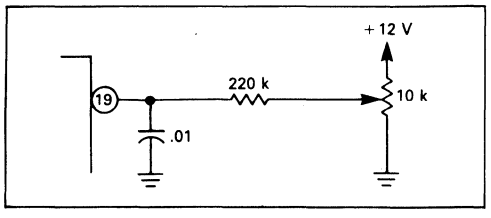


FIGURE 6 — ADJUSTING MODULATOR ANGLE

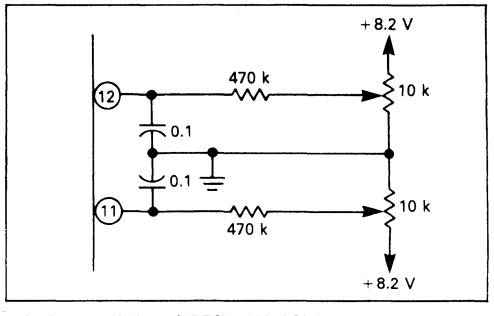


FIGURE 7 — NULLING RESIDUAL COLOR CARRIER IN BLACK

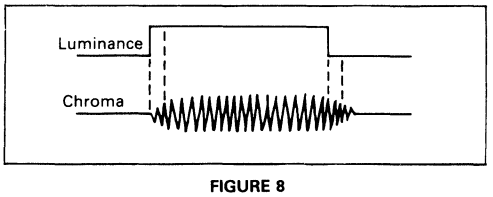


FIGURE 8

White carrier imbalance at the output can only be corrected by juggling the relative levels of R, G and B inputs for perfect balance. Standard devices are tested to be within 5% of balance at full saturation. Black balance should be adjusted first, because it affects all levels of gray scale equally. There is also usually some residual baseband video at the chroma output (Pin 13), which is most easily observed by disabling the color oscillator. Typical devices show 0.4 V_{pp} of residual luminance for saturated color bar inputs. This is not a major problem since Pin 13 is always coupled to Pin 10 through either a bandpass or a high pass filter, but it serves as a warning to pay proper attention to the coupling network.

THE CHROMA COUPLING CIRCUITS

Without going deeply into the subject, it is generally true that monitors and receivers have color IF 6.0 dB bandwidths of ±0.5 MHz. It is therefore recommended that the encoder should also limit the chroma bandwidth to approximately ±0.5 MHz through insertion of a bandpass circuit between Pins 13 and 10. For proper color level in the composite output, a mid-band insertion loss of 3.0 dB is desired. The bandpass circuit shown in Figure 1, using the TOKO fixed tuned transformer (see Appendix B) gives this result. One of many tv color IF bandpass circuits could also be used. When such a bandwidth reduction is inserted, the chroma is delayed by approximately 350 ns (as shown in Figure 8).

This 350 ns delay results in a visible displacement of the color and black and white information on the final display. The solution is to place a delay line in the luminance path from Pins 6 to 8 to realign the two components. Again, a normal tv receiver delay line can be used. These delay lines are usually of 1.0 k to 1.5 k characteristic impedance, and the resistors at Pins 6 and 8 should be selected accordingly. A very compact, lumped constant delay line is available from TDK (see Appendix C for specifications). Some types of delay lines have very low impedances (approximately 100 ohms) and should not be used, due to drive and power dissipation requirements.

In some applications, it may be possible to delete both the bandpass transformer and the delay line. For instance, when the RGB information itself is very low resolution, i.e., very narrow band (less than 1.5 MHz), no cross-talk would be generated in the encoder (see Figure 9). Keep in mind, however, that the standard monitor or receiver will still "see" an incorrect luminance sideband at X′. This points up the value of at least some chroma bandwidth reduction in the encoder. A simpler, lower cost bandpass circuit is shown in Figure 10(a). It provides the proper insertion loss, approximately ±1.0 MHz bandwidth, and about 100 ns delay.

The circuit shown in Figure 10(b) is even less costly, but has about 6.0 dB greater loss, provides very little bandwidth reduction except to remove the baseband feedthrough, and produces essentially no delay.

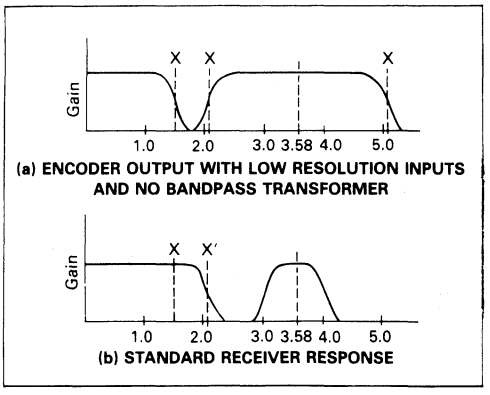


FIGURE 9

It will be left to the designer to decide which, if any, compromises are acceptable. Color bars viewed on a good monitor can be used to judge acceptability of step luminance/chrominance alignment and step edge transients, but signals containing the finest detail to be encountered in the system must also be examined before settling on a compromise.

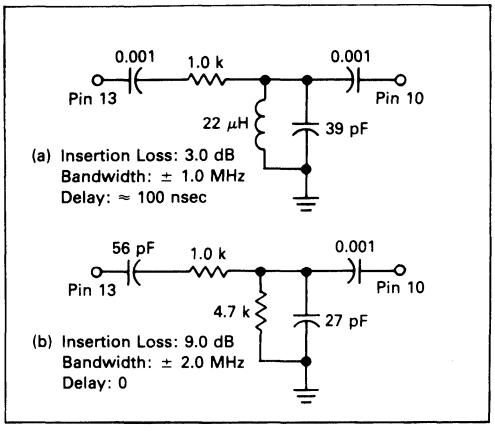


FIGURE 10 — OPTIONAL CHROMA COUPLING CIRCUITS

THE OUTPUT STAGE

The output amplifier normally produces about 2.0 V_{pp} and is intended to be loaded with 150 ohms as shown in Figure 11. This provides about 1.0 V_{pp} into 75 ohms, an industry standard level (RS-343). In some cases the input to the monitor may be through a large coupling capacitor. If so, it is necessary to connect a 150 ohm resistor from Pin 9 to ground to provide a low impedance path to discharge the capacitor. The nominal average voltage at Pin 9 is over 4.0 volts. The 150 ohm dc load causes the current supply to rise another 30 mA (to approximately 60 mA total into Pin 14). Under this (normal) condition the total device dissipation is about 600 mW. The calculated worst case die temperature rise is 60°C, but the typical device in a test socket is only slightly warm to the touch at room temperature. The solid copper 20-Pin lead frame in a printed circuit board will be even more effectively cooled.

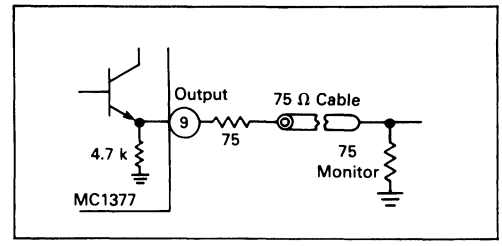


FIGURE 11

The MC1377 is designed to operate from an unregulated 10.8 to 13.2 volt dc power supply. Device current into Pin 14 with open output is typically 30 to 32 mA. To provide a stable reference for the ramp generator and the video output, a high quality 8.2 V internal regulator is provided. The 8.2 V regulator can supply up to 10 mA for external uses, with an effective source impedance of less than 1.0 ohm. This regulator is convenient for a tracking dc reference for dc coupling the output to an RF modulator. Typical turn-on drift for the regulator is approximately +35 mV over 1–2 minutes in otherwise stable ambient conditions.

SUMMARY

The preceding Application Note was intended to detail the application and basis of circuit choices for this versatile tv signal encoder. A complete MC1377 application with the MC1374 VHF modulator is shown in Figure 12. The internal schematic diagram of the MC1377 is provided in Figure 5. If further assistance is needed, contact Motorola Linear and Military IC Division, Applications Engineering.

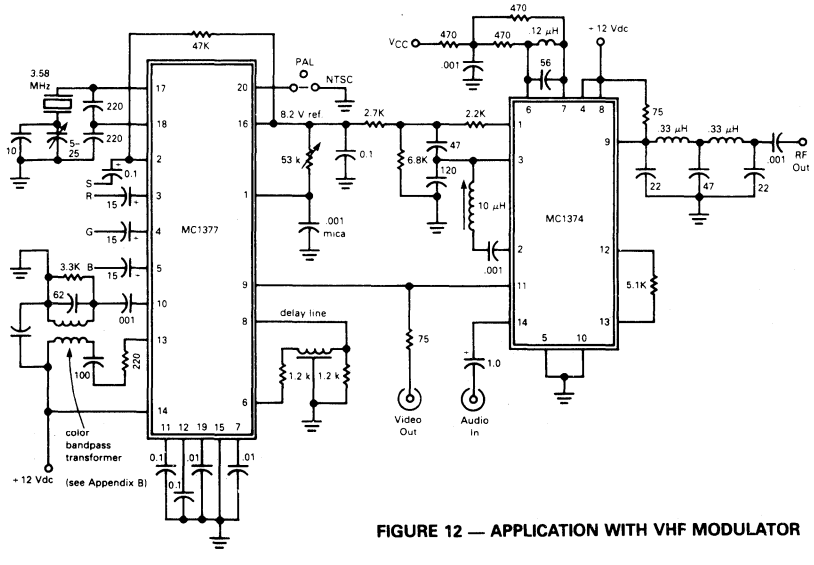


FIGURE 12 — APPLICATION WITH VHF MODULATOR

APPENDIX A

In full RGB systems, three information channels are wired from the signal source to the display to permit unimpaired image resolution. The detail reproduction of the system is limited only by the signal bandwidth and the capability of the color display device. Higher than normal sweep rates may be employed to add more lines within a vertical period. Three separate projection picture tubes can be used to eliminate the "shadow mask" limitations of a conventional color CRT.

Figure (b) below shows the "baseband" components of a studio NTSC signal. As in the previous example, energy is concentrated at multiples of the horizontal sweep frequency. The system is further refined by precisely locating the color subcarrier midway between luminance spectral components. This places all color spectra between luminance spectra and can be accomplished in the MC1377 only if "full interlaced" external color reference and sync are applied. The individual components of luminance and color can then be separated by use of a comb filter in the monitor or receiver. This technique has not been widely used in consumer products, due to cost, but it is rapidly becoming less expensive and more common. The unequal bandwidths of I and Q cannot be implemented with the MC1377, first because I and Q axes are not used, and second, because outputs of the two color modulators are added before any bandwidth reduction is imposed. Most monitors and receivers compromise the "standard" quite a bit, by using responses as shown in Figure (c). Some crosstalk of luminance information into chroma, and vice versa, is always present. The acceptability of the situation is enhanced by the suppression of the color carrier and the generally limited ability of the CRT to display information above 2.5 MHz. If the signal from the MC1377 is to be used primarily to drive conventional non-comb filtered monitors or receivers, it would be best to reduce the bandwidth at the MC1377 to that of Figure (c) to lessen crosstalk.

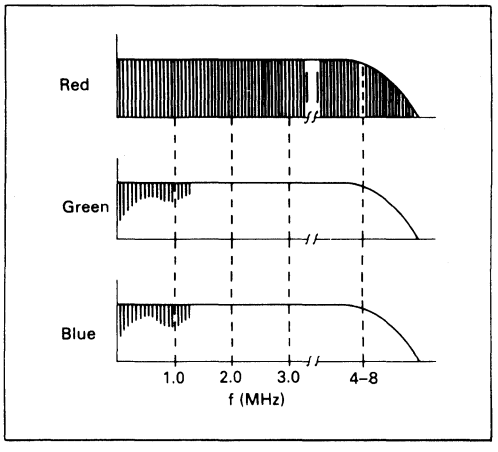


FIGURE 13(a) — SPECTRA OF A FULL RGB SYSTEM

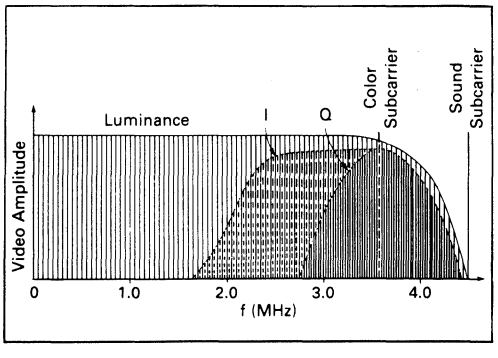


FIGURE 13(b) — NTSC STANDARD SPECTRAL CONTENT

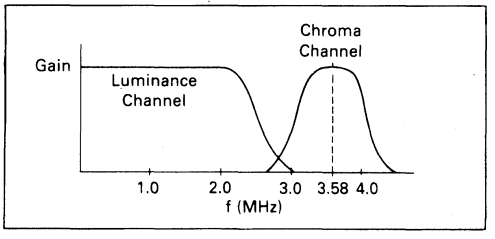


FIGURE FIGURE 13(c) — TYPICAL MONITOR/TV

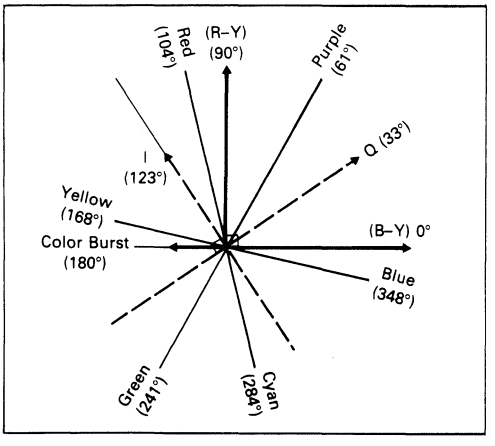
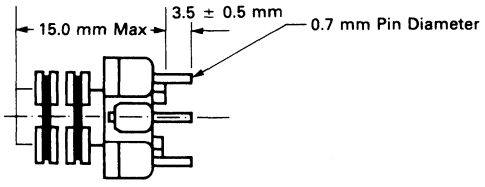
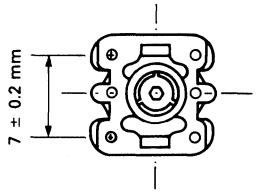


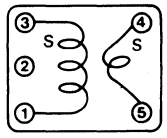
FIGURE 13(d) — COLOR VECTOR RELATIONSHIP, I/Q SYSTEM versus (R–Y)/(B–Y) SYSTEM SHOWING STANDARD COLORS

APPENDIX B

A PROTOTYPE CHROMA BANDPASS TRANSFORMER
TOKO SAMPLE NUMBER 166NNF-10264AG







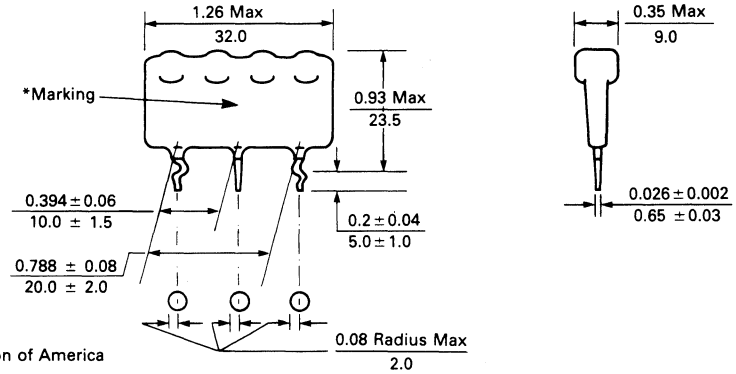
Connection Diagram
Bottom View

Toko America
5552 West Touhy Avenue
Skokie, IL 60077
(312) 677-3640

Unloaded Q (Pin 1–3): 15 @ 2.5 MHz
Inductance: 30 μH ± 10% @ 2.5 MHz
Turns: 60 (each winding)
Wire: #38 AWG (0.1 m/m)

APPENDIX C

A PROTOTYPE DELAY LINE
TDK SAMPLE NUMBER DL122401D-1533



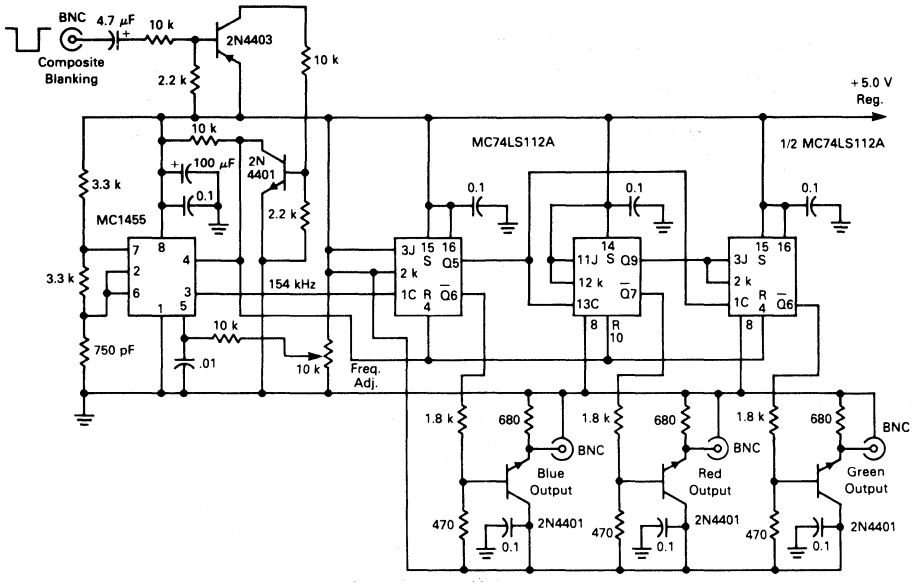
TDK Corporation of America
4711 Golf Road
Skokie, IL 60076
(312) 679-8200

*MARKING: PART NUMBER, MANUFACTURER'S IDENTIFICATION, DATE CODE AND LEAD NUMBER.

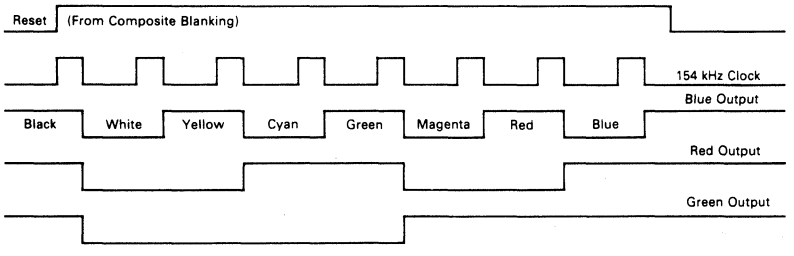
	Item	Specifications
1	Time Delay	400 ns ± 10%
2	Impedance	1200 Ohms ± 10%
3	Resistance	Less Than 15 Ohms
4	Transient Response with 20 ns Rise-Time Input Pulse	Pre-Shoot: 10% Max
		Over-Shoot: 10% Max
		Rise-Time: 120 ns Max
5	Attenuation	3 dB Max at 6.0 MHz

APPENDIX D

AN RGB PULSE GENERATOR



RGB PULSE GENERATOR TIMING DIAGRAM



AN1019

NTSC Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Operation

Prepared by
Ben Scott and Khalid Shah
Bipolar Analog IC Division

PREFACE

The TDA3330 is a composite video to RGB Color Decoder originally intended for PAL and NTSC color TV receivers and monitors. The data sheet is oriented toward picture tube drive, rather than cable level outputs. This application note is intended to supplement the data sheet by providing circuits for video cable drive, such as used in video processing circuits, frame store, and other specialized applications, and to expand upon the functional details of the TDA3330.

CIRCUIT CONSTRUCTION TECHNIQUES

The best solution is a single or double sided PC board, such as shown in Figure 11, with as much ground plane as possible. The oscillator components at Pins 8 and 9 must be close to the pins. A low profile socket is acceptable for prototyping. Wirewrap is definitely not recommended. In most respects the part is not sensitive to layout, except for the oscillator, however, unwanted picture artifacts, beats and noise are much easier to control with a good ground plane layout.

MEASURING THE OSCILLATOR

The oscillator amplitude at Pin 9 should be about 400 mV_{pp}, measured with an ordinary 4.0 pF/10 MΩ scope probe. Keep in mind that the oscillator frequency is 3.58 MHz and is part of a phase-locked loop with only a few hundred Hz pull-in range. The scope probe loading is enough to push the oscillator into or out of lock. It is recommended that Pin 9 be observed initially to ascertain that it is running, and then leave Pins 8 and 9 alone. A procedure for adjustment will be covered later. Of course, an output buffer (emitter follower) can be connected to Pin 9, permanently, and the Pin 9 tuning capacitor reduced accordingly.

THE SANDCASTLE INPUT

"Sandcastle" is a familiar term to European TV engineers. It is basically a 0 V baseline with a 4.0 V blanking pulse and a 10 V burst-gating pulse on top of it, as shown in Figure 1. Sometimes the expression "super sandcastle" is used, which means that composite blanking is present, i.e. vertical and horizontal blanking, in addition to the burst-gating pulse. Sometimes the vertical blanking is 2.5 V and the horizontal is 4.0 V, sometimes both are at 4.0 V. In the TDA3330, the blanking portion is only used to provide a blanking waveform at the blanking output, Pin 11, which is used to supply "extra" blanking in the picture tube driver application. Pin 11 is not used in other applications, so the blanking portions of the "sandcastle" are not required. For the "cable to cable" decoder, all that the TDA3330 really needs at Pin 15 is the burst-gate pulse. Pin 16 should be grounded.

The burst-gate pulse has 3 functions:

1. Gating the color IF gain control (ACC) so that IF gain is adjusted to keep burst amplitude constant;
2. Setting the black level in the R, G, B outputs, and
3. Gating the color phase detector (APC) so that the VCO can be phase-locked to the burst. See the block diagram in Figure 2.

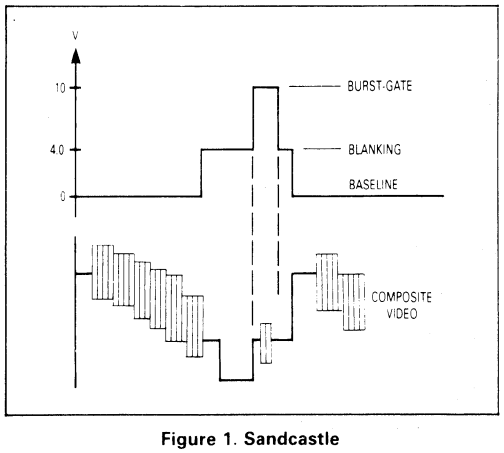


Figure 1. Sandcastle

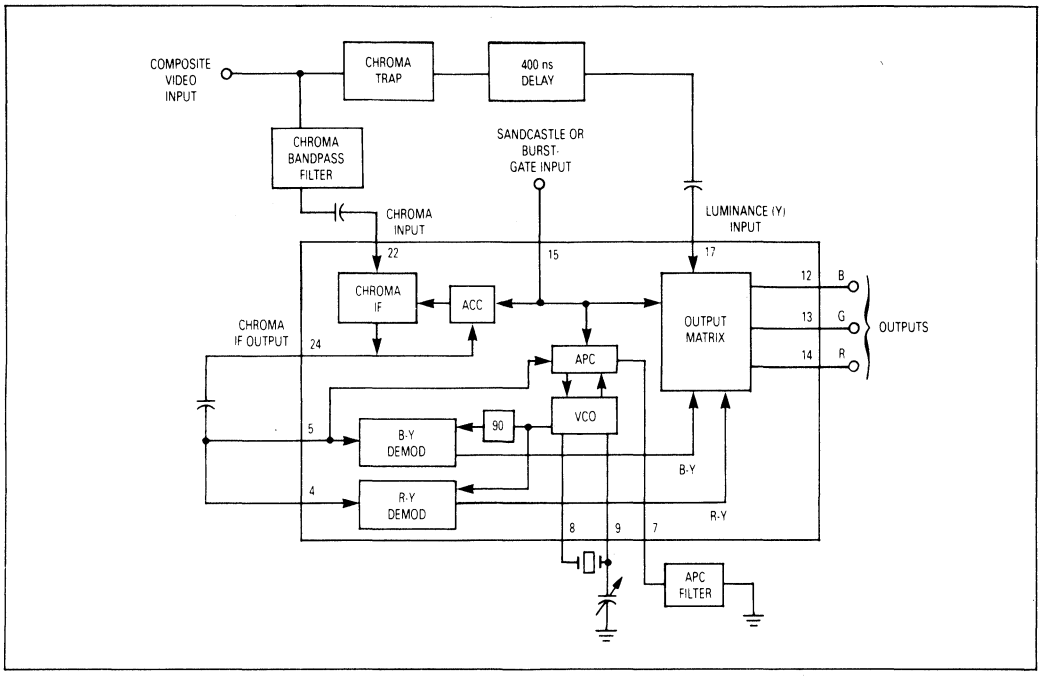


Figure 2. Simplified Block Diagram for NTSC Mode

It is important that the burst-gate pulse into Pin 15 be at least 8.0 V and timed correctly with respect to incoming video, as shown in Figure 3. If the gate pulse is too late or too wide it will still be present after the blanking has ended, leading to serious errors in black level, color level and VCO lock. The burst-gate pulse can sometimes be obtained from the same equipment that supplies the video, or it can be generated by a couple of one-shots and a sync separator; see Figure 4. Another method is to separate sync. Use a one-shot pulse stretcher to make an 8–8.5 μs wide pulse for Pin 15, and then put the separated sync into Pin 16. (Pin 16 could be called the "burst-gate inhibit"). This will prevent the first part of the Pin 15 pulse from gating sync, which would upset the black level clamping function; see Figure 5.

THE LUMINANCE PATH

The outputs at Pins 12, 13 and 14 are positive-going video, with the sync pulse almost completely removed. The black level of the output remains constant as the **contrast, saturation** and **hue** are changed. The **contrast** control changes both luminance and chrominance together, so that, for example, output color bar waveforms maintain the same shape. The DC level of all outputs is moved by the **brightness** control, with no change in the peak to peak signal amplitude. The **brightness** control can change black level from 1.4 V to about 6.7 V as the control voltage on Pin 18 is raised from about 2.0 V to 5.0 Vdc. See Figure 6. The **contrast** control, Pin 19, is at maximum at 5.0 Vdc; the output is reduced 6.0 dB when the control is 3.5 Vdc, and is reduced about 40 dB when the control voltage is 1.0 Vdc.

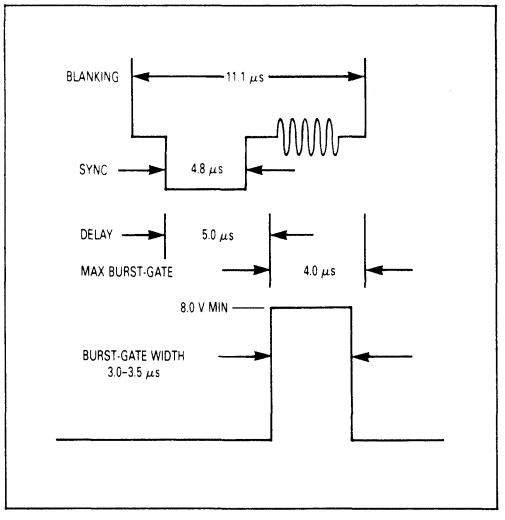


Figure 3. Burst-Gating

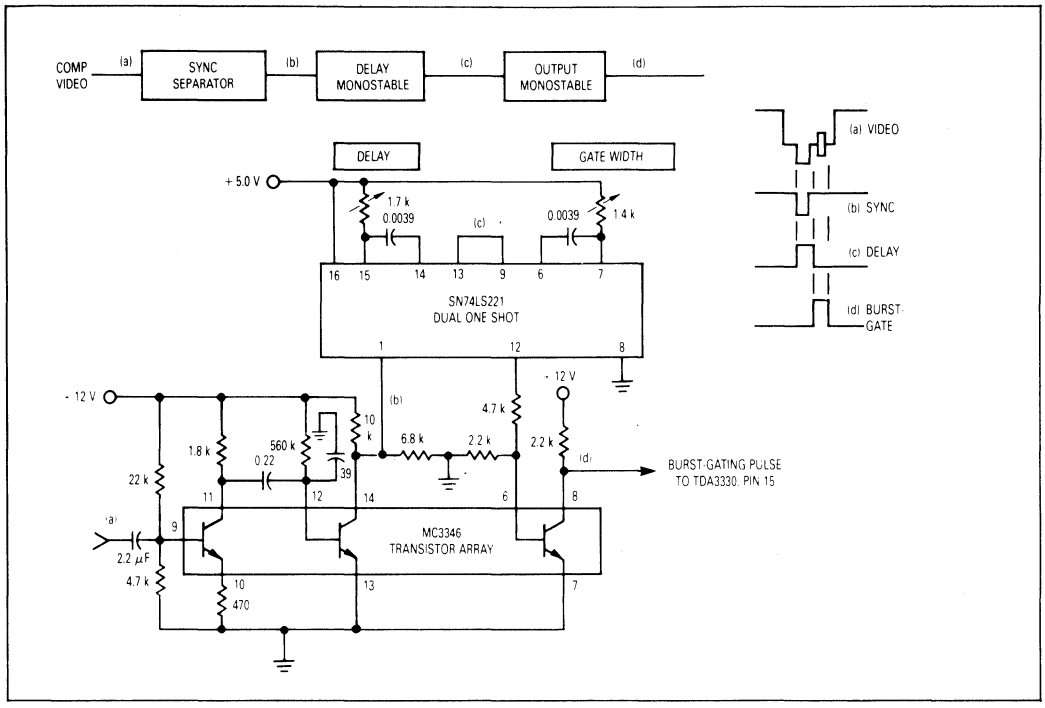


Figure 4. Method of Obtaining Burst-Gate from Composite Video

The maximum output voltage, black to white, is about 7 times greater than the *black* to *white* level at Pin 17. For a composite input signal of 1.0 V_{pp}, there is 0.5 V_{pp} at Pin 17, due to the delay line matching resistors. This is about 0.35 V_{pp} *white to black* and gives about 2.5 V_{pp} max at the outputs. The input to the total circuit can be doubled to 2.0 V_{pp}, which then yields about 5.0 V_{pp} at Pins 12, 13, and 14. However, note that any change in input amplitude requires readjustment of the **saturation** control for correct chroma/luma proportion. This is because the luminance component directly follows the input, while the color component is almost unchanged due to the ACC of the color IF. Therefore, it is important to note that the TDA3330 can be set up to work with different levels of input, but it is not automatically compensated for input changes. Also note that at 5.0 V_{pp} out and max **brightness** (black level out 6.7 V) there will be clipping of the positive peaks. The upper limit for the output is about 10 V.

Troubleshooting note: If a proper (positive) video signal is AC coupled into Pin 17, and a proper burst-gate is applied to Pin 15, there should be video out, regardless of any aspects of the color processing portions of the IC

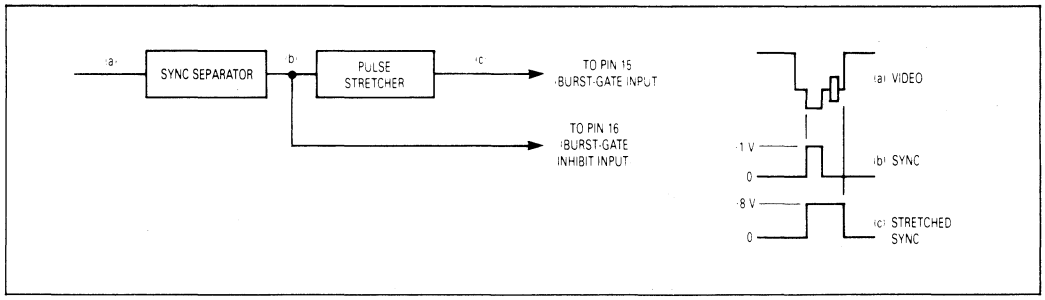


Figure 5. Alternate Method of Gating from Video

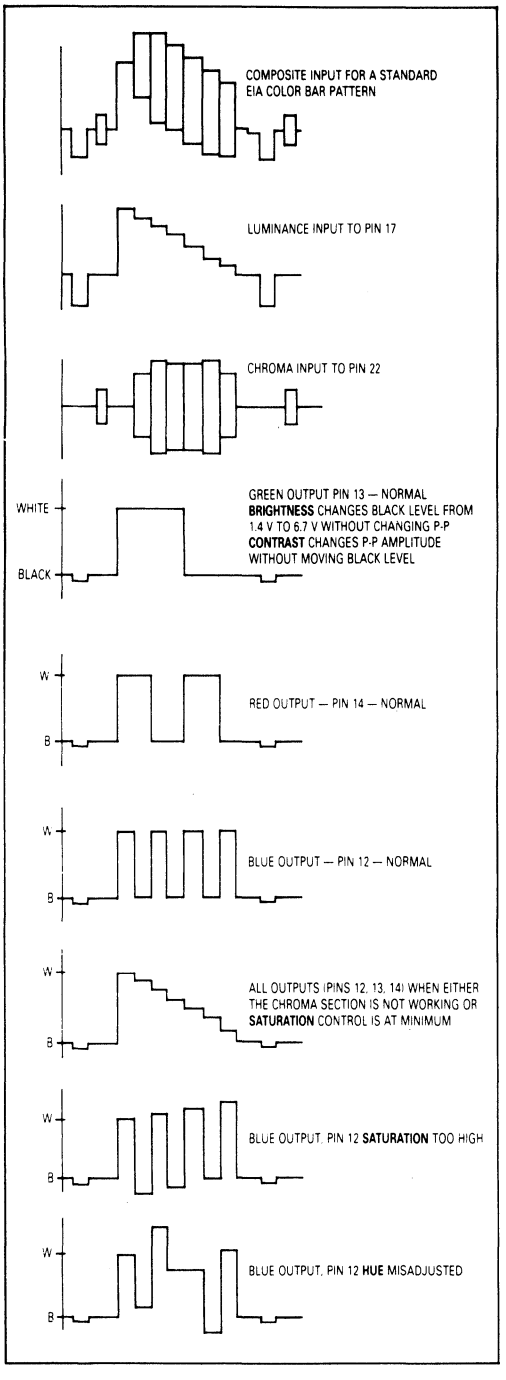


Figure 6. Some Normal and Other Waveforms

THE CHROMA PATH

The chroma input is derived from the composite input by a simple 3.58 MHz single-tuned bandpass circuit with about ±0.5 MHz (6 dB) bandwidth. The chroma portion of a color bar pattern should look like Figure 7. The circuit components recommended in our application circuit should yield about 100 mV_{pp} of burst at Pin 22, but anything from 10–200 mV_{pp} will work. The output of the chroma IF is at Pin 24, where the burst should be about 150 mV_{pp}. There may or may not be chroma present, depending on the **contrast** and **saturation** control settings. (Both controls have exactly the same effect at Pin 24, changing the picture chroma amplitude between the burst pulses.)

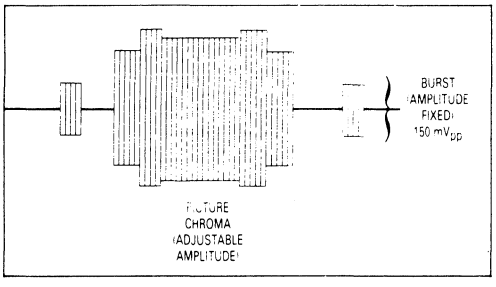


Figure 7. Chroma IF Output, Pin 24

Troubleshooting note: If there is 1.5 V_{pp} of burst at Pin 24, the burst-gating pulse is either too small or incorrectly positioned in time.

The chroma IF output from Pin 24 is coupled to the chroma demodulators, Pins 4 and 5 by a small capacitor. (Note: 100 pF performs better than the 1.0 nF on the data sheet; it reduces luminance component feedthrough.) Tweaking of demodulator balance to reduce residual chroma subcarrier in the outputs can be done at Pins 4 and 5 by the trimmer technique shown in Figure 8. This is a fine tuning which is usually not needed, but is available for the demanding application.

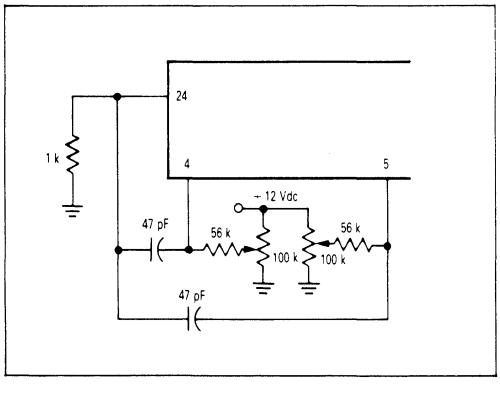


Figure 8. Optional Tweak of Demodulator Balance

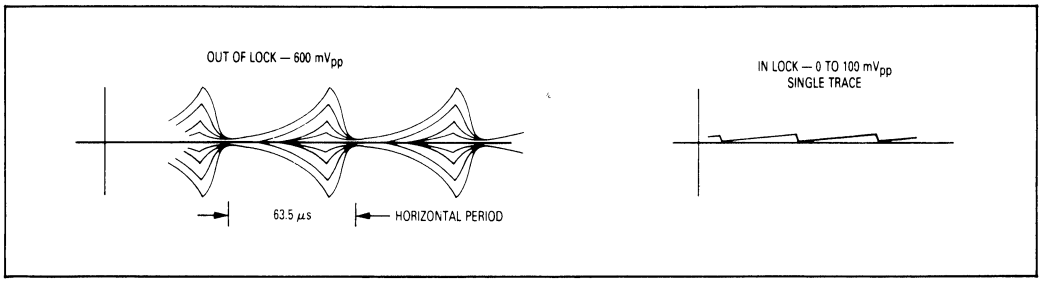


Figure 9. VCO Lock — Voltage at Pin 7

COLOR LOCKUP

If the required chroma is present at Pins 4, 5 (same as Pin 24), and if the oscillator is known to be running, then lockup is just a matter of adjusting the trimmer on Pin 9. As noted earlier, the scope probe cannot be put on the oscillator for this adjustment. Instead, put the scope on the AFC filter, Pin 7. Waveforms as shown in Figure 9 will be observed as the trimmer is adjusted.

Lock-in range is about 18–22 pF with the typical socket and PC board and ordinary (Radio Shack) 3.58 MHz TV crystal.

BUFFERING THE OUTPUTS

In order to be able to drive a cable, it is necessary to provide an output amplifier. The design shown in Figure 10 has two additional benefits:

1. It provides an opportunity to reduce the residual 2nd harmonic of the color subcarrier (7.16 MHz) by means of a trap, and
2. It reduces the DC level another 0.7 Vdc at the emitter of the 2N4401, and an additional 2:1 reduction due to the 75 Ω series R into the 75 Ω cable. Therefore, the black level into the cable can be as low as 0.35 V, for the minimum brightness control setting.

MISCELLANEOUS GREMLINS

It has been reported from the field that the internally supplied NTSC mode switch current (I3 in Figure 12 of the data sheet) is occasionally insufficient. This is characterized by a decoder which intermittently decodes and then "color kills." In the killed mode, Pin 3 is above 1.5 V and Pin 2 is below 0.7 V, which holds the **saturation** control low (off). This can be fixed by putting 22 k from Pin 3 to V_{CC}. This supplies additional current into Pin 3, causing an internal latch to pull Pin 3 low (have faith), and returns Pin 2 to an open state so it can be varied by the **Saturation** control.

SUMMARY

The TDA3330 has a wide range of functional capability with relatively simple application circuitry (once understood). It is hoped that this paper will assist users in becoming familiar and satisfied with it.

APPENDIX

Initial Setup Sequence for TDA3330 Evaluation Board

After connecting a Composite Video Signal In and connecting the Sync, Red, Green and Blue outputs to an appropriate RGB monitor, follow the subsequent steps, in order, to adjust the 11 variable components to optimize performance of the RGB decoder:

1. Look at the signal out of the collector of the 2N4402 transistor. Adjust POT #9 so that the Composite Video Signal at this point is 1.0 V_{pp}.
2. Set POTS #2 and 3 to approximately the middle of their values (i.e., 50 kΩ). This helps in making the subsequent adjustments.
3. POT #7 sets the Burst-Gate Width and POT #8 sets the Burst-Gate Delay relative to the Video Sync Signal. Use a dual input oscilloscope and look at the Video In signal and the Burst-Gate Signal at Pin 15 of the TDA3330. Adjust POT #8 so that the Burst-Gate Signal begins ~250 ns after the Sync Signal ends. Next adjust POT #7 so that the width of the Burst-Gate Signal is 3.5–4 μs. Note: See Figure 3.
4. Put the oscilloscope probe on Pin 7 of the TDA3330. Adjust the Variable Capacitor, connected to Pin 9, until the VCO is In Lock. This will happen when the trace signal drops from ~650 mV_{pp} to less than 100 mV_{pp}. Try to make the signal as small as possible, possibly down to dc. (Make tilt flat) Note: See Figure 9.
5. Put the oscilloscope probe on Pin 17 of the TDA3330. Adjust the 10 μH Variable Inductor to minimize Chroma Signal Feedthrough.
6. In order to fine tune chroma demodulator balance, remove the chroma signal from the Composite Video Signal In (or, alternatively, turn the Saturation POT all the way down). Look at the Red output on the oscilloscope and adjust POT #2 to minimize subcarrier from the V Signal (i.e., R-Y) input. Next look at the Blue signal and adjust POT #3 to minimize subcarrier from the U signal (i.e., B-Y) input.
7. POTS #1, 4, 5 and 6 can next be adjusted to optimize picture color quality. Suggestion for doing this is to set Saturation (POT #1) and Brightness (POT #5) to middle and then adjust Contrast (POT #4 and Hue POT #6) till picture colors are approximately right. Next adjust POT's 1 and 5. Repeat the above sequence until satisfied with color quality of picture.

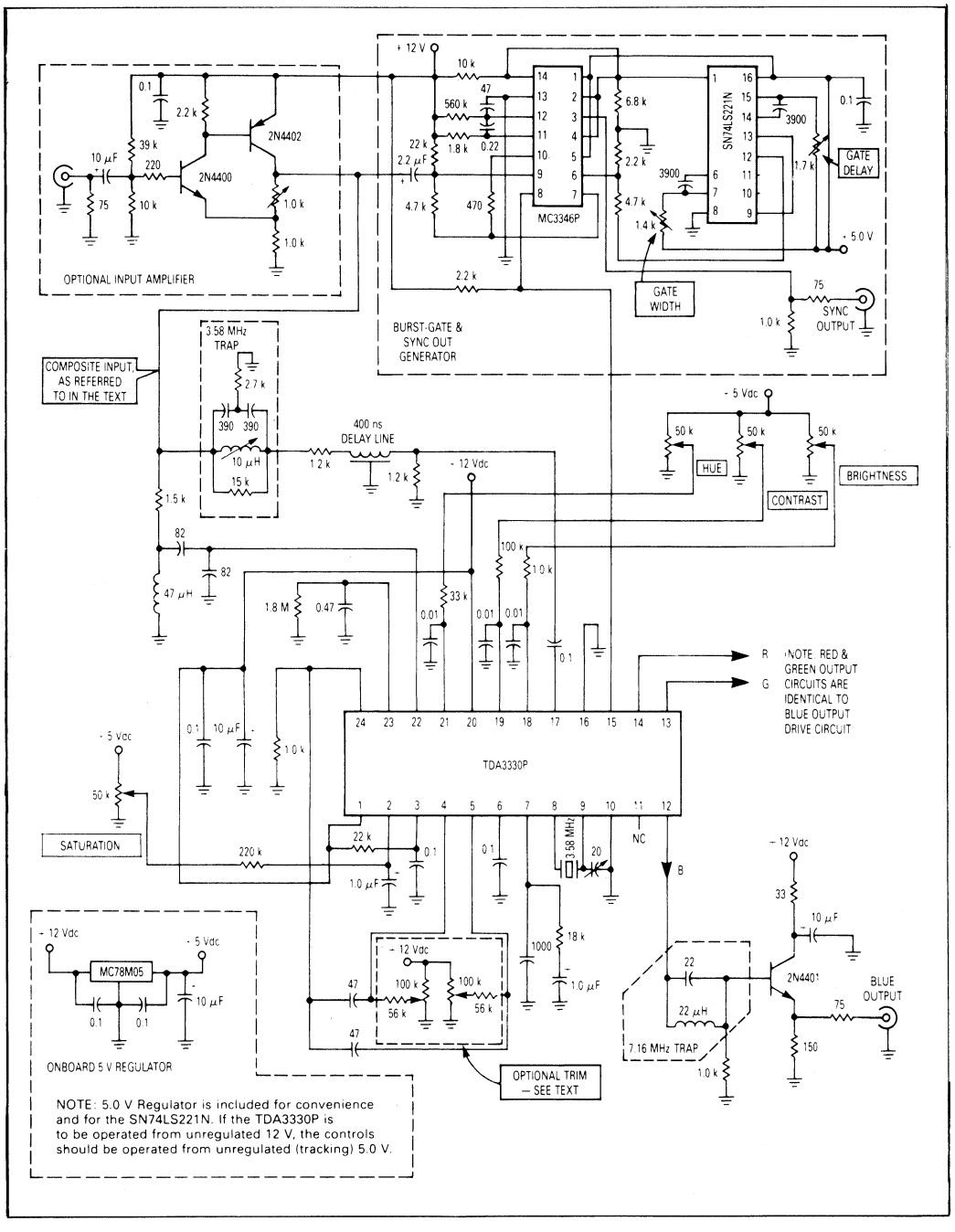
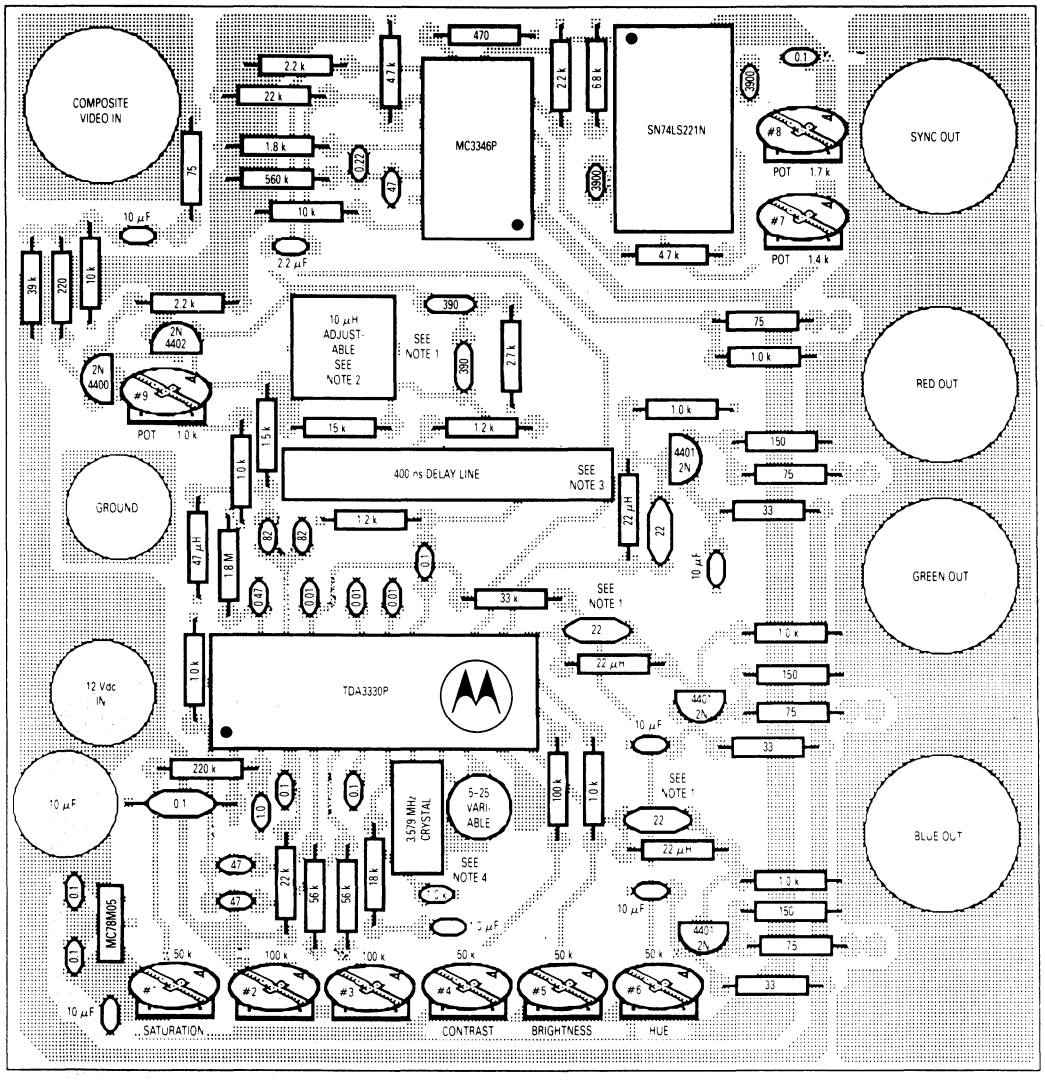


Figure 10. TDA3330 RGB NTSC Decoder Circuit



NOTES: 1. For the 390 pF and the 22 pF capacitors in the 3.58 MHz and in the 7.16 MHz traps, silver mica capacitors should be used for better trap performance.
2. The board layout is for Toko part #BTKANS-9439HM.
3. Board layout will accommodate a Toko or a TDK 400 ns delay line.
4. A 3.58 MHz crystal available through Radio Shack was used.

Figure 11a. TDA3330P RGB NTSC Decoder Evaluation Board, Component Layout

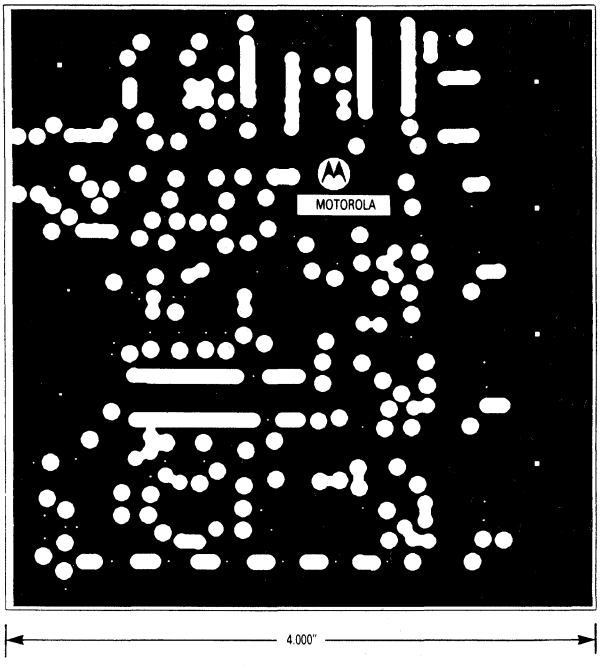


Figure 11b. TDA3330 RGB NTSC Decoder Evaluation Board, Component Side (not full size)

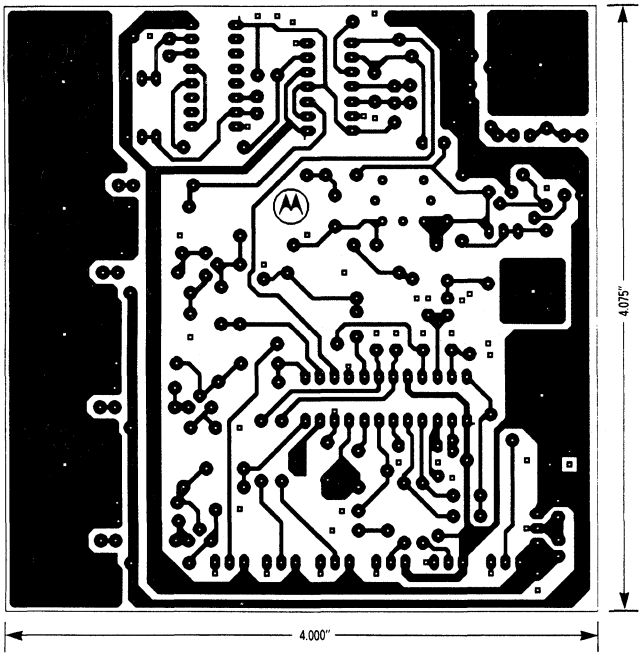


Figure 11c. TDA3330 RGB NTSC Decoder Evaluation Board, Bottomside (not full size)

AN1020

A High-Performance Video Amplifier For High Resolution CRT Applications

I. INTRODUCTION

This application note describes the superior performance characteristics of Motorola CRT driver transistors in a state-of-the-art video amplifier. In particular, the high speed obtainable with low DC power consumption is shown. A circuit which is insensitive to load variations and interconnect methods is given.

II. APPROACH

The performance requirements for the amplifier are these:

Voltage Gain	20
Rise and fall times	3 nS
Output	40 V p-p min.
Overshoot	5% max.
Load capacitance	8 pF min.
Power supplies	60 V, 5 V, −5 V

The voltage gain is obtained in a transconductance amplifier in the form of a common-emitter, common-base cascode circuit. In this circuit the load capacitance is isolated from the cascode by a set of complementary emitter-followers. Thus, the capacitive loading on the cascode is low, which allows operation at a moderate dissipation level.

The emitter followers are biased at a Class "B" operating point. They conduct only during voltage transitions, while charging or discharging the CRT capacitance. This operation is similar to the way highly efficient C-MOS logic ICs function.

The emitter followers provide a combined output signal from a low impedance, or "stiff" source. This stiff source makes the entire circuit insensitive to load variations and to different methods of connecting the video amplifier to the CRT.

III. THE CIRCUIT

A. The Input Circuit

Refer to the circuit diagram in Figure 1. A fast pulse generator is required for accurate performance data. The Tektronix Model PG502 is a good example of a pulse generator for optimum performance, versatility and price considerations. The pulse generator has a rise time in the range of .8 ns and an output impedance of 50 ohms. A minimum-loss L-pad is used between the generator and the base of the driver transistor, Q_1. The impedance level at this point is designed to be 75 ohms. The voltage attenuation of the matching circuit is 0.64.

B. The Cascode Circuit

1. The Common-emitter stage uses an LT1001 transistor in a TO-39 package. The emitter current of 70 mA is supplied from a −5 V source via resistors R_4, and R_5. For ac, only R_4 at 15 ohms is operative. R_4 and the built-in emitter-ballast resistor of 1.6 ohms, determine the transconductance of Q_1, which is then 60 mA/V.

Both the emitter current and the collector current of this stage follow the base voltage almost instantaneously. Computer simulation has shown that the transition times are less than 1 ns. The transconductance may be increased during the transition times by adding the "peaking-network" R_6, C_2, C_3. Adding this network is very much like adjusting the rise time in the probes of fast oscilloscopes. In the cascade circuit under discussion the "peaking" network compensates rise time deterioration at the collector by speeding up the emitter current of Q_1. This procedure must be applied with moderation since it may affect the large-signal swing capability. The resistor, R_6, should be equal to or larger than R_4. The capacitor, C_2, determines the length of time during which "peaking" occurs. The product of R_6 and C_2 is typically a few nanoseconds. The trimmer, C_3, can be used for fine-tuning, but is usually not important and may be omitted. If there is lead inductance associated with the path from the emitter of Q_1 through C_3 to ground, use of C_3 may cause ringing at high frequencies.

2. The common-base stage uses an LT1817 transistor in a TO-117 package. Since the transistor must dissipate continuously some two Watts of DC power, good heatsinking is mandatory. The TO-117 package provides a high-conductance thermal path to a heatsink or chassis. At the same time, it adds only minimal capacitance to the circuit.

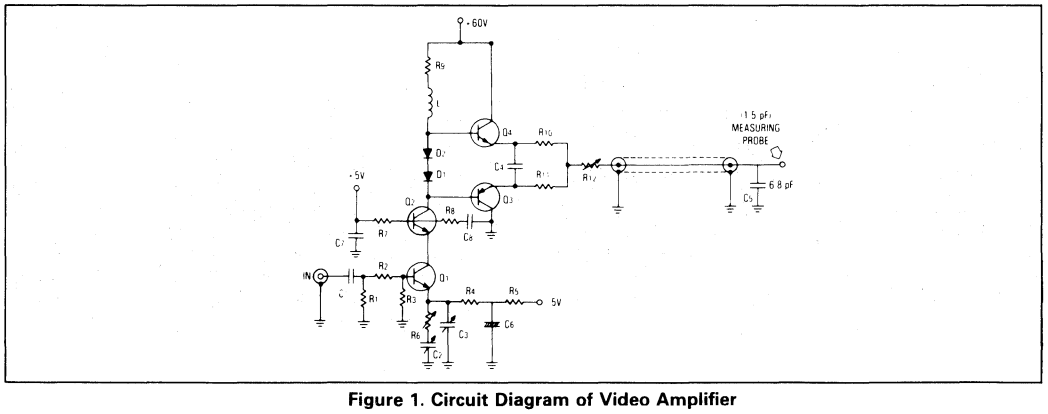


Figure 1. Circuit Diagram of Video Amplifier

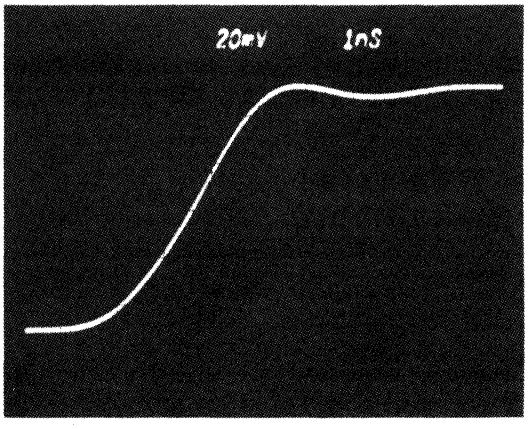


Figure 2A. Rise Time at 10 V p-p

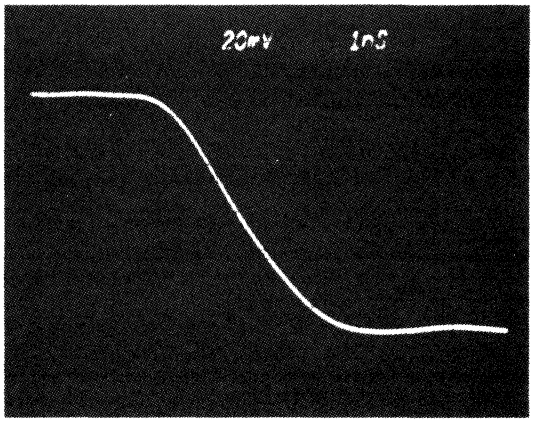


Figure 2B. Fall Time at 10 V p-p

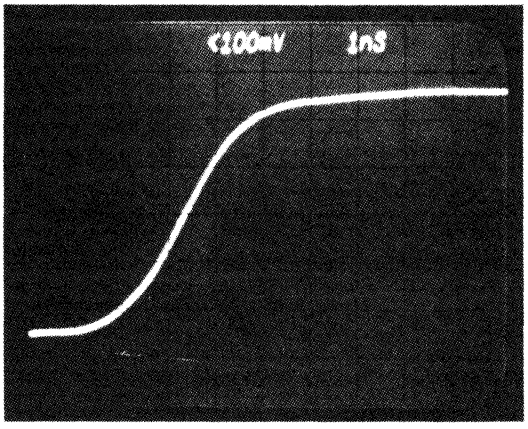


Figure 2C. Rise Time at 40 V p-p

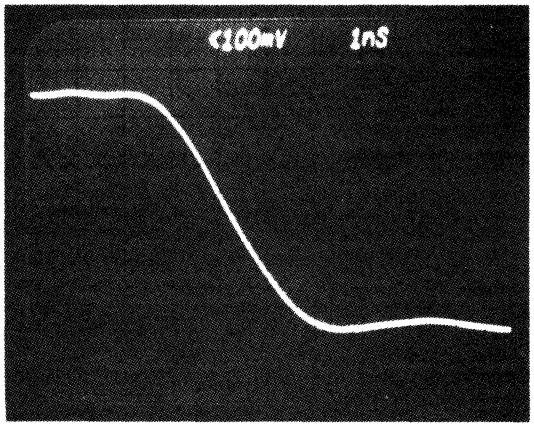


Figure 2D. Fall Time at 40 V p-p

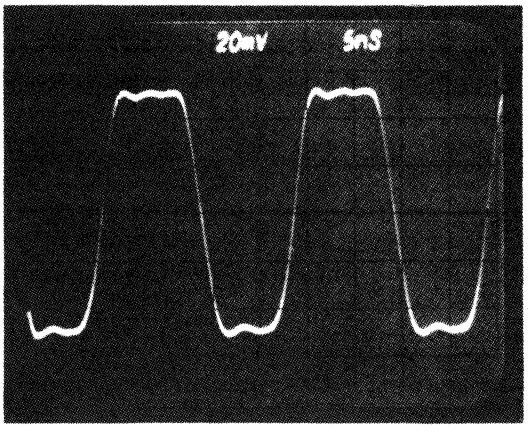


Figure 2E. 10 nsec Pixels 10 V p-p

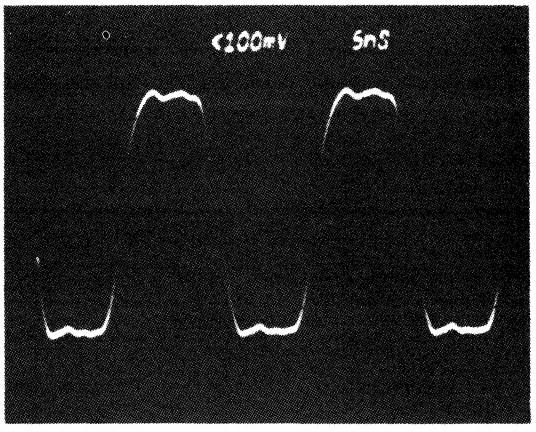


Figure 2F. 10 nsec Pixels 40 V p-p

The common-base stage has near unity current gain and acts as an impedance transformer, providing a current source at its collector. This current charges the combined collector capacitances of Q_2, and the emitter followers, Q_3 and Q_4, which add up to about 5 pF at the operating point. To this total one must add about one pF of stray capacitance. A load or "pull up" resistor of 430 ohms is used at the collector of the common-base transistor, Q_2. The rise time at this point may be calculated to be:

$$t_r = .35 \cdot 2 \cdot P_i \cdot 430 \cdot 6\ pF = 5.7\ nS$$

This value is improved by the addition of a peaking coil of .22μH. Theoretically, the rise time could be reduced by up to 40% (without overshoot) by optimizing the inductance. Due to the non-linear nature of the capacitances to be compensated for here, different effects result for rise and fall times. This situation requires a compromise resulting in a practical improvement of less than the theoretical transition time. Nevertheless, 3 ns transition times are obtained at the collector of Q_2 by means of the emitter peaking discussed earlier.

The LT1817 is packaged in a common-base configuration. This means that the transistor base is connected to two symmetrical low-inductance base leads. As is well known, base-lead inductance may cause instabilities in common-base configurations. To prevent this from happening, base damping resistors, R_7 and R_8, have been added. The value of these resistors depends on the device bias point and the circuit layout. If oscillations occur, they would be near a Gigahertz or higher, and therefore may not be seen on anything but a sampling oscilloscope. They will affect rise times and output swing capability. Instabilities may be easily detected with a spectrum analyzer connected to the input jack of the video amplifier. Enough signal will feed back through the collector capacitance of Q_1 to reach the analyzer.

3. The emitter-followers, Q_3 and Q_4, are a complementary pair of transistors, LT1829 and LT5839, in TO-39 packages. The transistors are biased to the threshhold of conduction by two diodes, D_1 and D_2. These diodes should be relatively large, slow rectifier types, each providing no more than 0.6V of bias with a forward diode current of 70mA. The diodes have low, largely capacitive impedances at high frequencies, and should be connected with short leads between the bases of Q_3 and Q_4.

The emitter followers provide temporary charging currents to the output circuit whenever the voltage across the load is changed. In case of a display with high contrast and many transitions, the current in Q_3 and Q_4 may become appreciable, causing the transistors to heat up. The elevated junction temperature shifts the bias point from Class "B" in the direction of "AB."

If the emitters of these transistors were connected directly, a DC component of current would flow from the 60 V supply through the devices to ground. This "pole current" would further heat up the junctions and might lead to thermal runaway. In the circuit described, this situation is prevented from occurring through the use of the emitter stabilizing resistors R_{10} and R_{11}. Using capacitor, C_4, prevents deterioration of the dynamic operation of the circuit.

A simpler, more primitive way to avoid thermal problems, is to use only one bias diode, or none at all. Doing this, however, has serious effects on the gray scale linearity at mid-range.

4. The output circuit. The LT1839 and LT5839 transistors have excellent peak current handling capabilities. Their emitter currents react virtually instantaneously to the base voltage. Even when supplying several hundred milliamperes of peak charging current, the base-to-emitter gain holds up well. It is therefore possible to drive more elaborate load configurations than a bare capacitance. This ability may ease interconnect problems. The circuit described in Figure 1 is powerful enough to accommodate a piece of shielded cable between the CRT and the video amplifier. A twin-lead line or a single wire connection may also be used instead of the shielded cable. The circuit is not only able to drive elaborate interconnect networks, but also to handle substantially larger CRT capacitances without significant penalties in rise and fall times. For instance, this circuit is capable of driving 15 pF with 3.8 ns transition times.

In all cases, the presence of additional reactive circuit elements causes the output circuit to have resonances which will cause ringing or overshoots, if the output circuit is not properly damped. To this end, a variable resistor, R_{12}, is included in the circuit. When adjusted for critical damping, the waveform will look smooth across the load capacitance.

In the demonstration circuit, (Fig. 1), a 6.5 pf chip capacitor simulates the CRT cathode capacitance. It is connected across a special jack, which has been designed for the Tektronix FET probe, Type 6201. Probe, jack and chip have a combined capacitance of 8pF. The FET probe may be used in conjunction with Tektronix sampling scopes or real-time scopes with bandwidths of 300 MHz or more.

One may be tempted to use slower instruments, such as a 200 MHz type, and correct mathematically for the additional transition time contributed by the scope. We do not recommend this approach since slower scopes appear to produce wave shape distortions which lead to misleading rise-time values.

IV. AMPLIFIER PERFORMANCE

Figure 2 contains photographs showing rise and fall times at 10 V and 40 V peak-to-peak swing. Also shown are some response curves generated by the well-known circuit analysis program SPICE. Careful modelling of the semiconductors used, according to the theory of Gummel and Poon, resulted in good agreement between computer and laboratory-generated performance data. In addition, computer analysis offers insights, which cannot be obtained by practical measurements.

Shown in Figure 3 are the superimposed plots of the input voltage at the base of Q_1 and the output voltage across the CRT capacitance. The second set of plots, Figure 4, displays the collector-current waveform of Q_1 and the combined emitter circuits of the complementary set of emitter followers. The collector current of Q_1 shows clearly the effect of "peaking," introduced by the emitter circuit components, R_6, C_2 and C_3. Note that under full swing conditions (40 V p-p output), the waveforms are not quite symmetrical. The effect on the transition times of the output voltage, however, is minimal.

The example shown in both Figures 3 and 4 corresponds to a pixel-time of 10 ns, which is the practical minimum for a system with 3 ns transitions. When operating continuously at this rate, approximately 25mA of average current flows in each one of the emitter-followers. This causes a significant rise in case temperature for these devices. It is therefore recommended that clip-on heat radiators be used. There is no electrical penalty for this measure, since the collectors are on ground potential.

Heatsinking becomes absolutely mandatory if one explores the limits of the amplifier by operating at 100 MHz and beyond.

V. CONCLUSION

An amplifier was developed which meets all needs of a high-resolution CRT monitor. While practical considerations played an important part in the circuit realization, the primary purpose was to demonstrate transistor capability. It is hoped that enough background information was given to allow the reader to tailor his circuit to his specific needs.

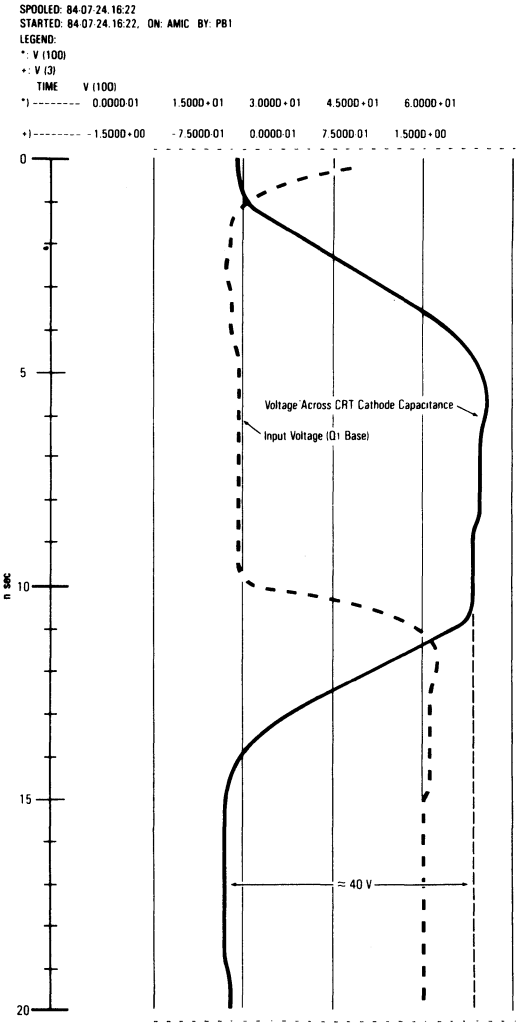


Figure 3. Computer Generated Voltage Plots

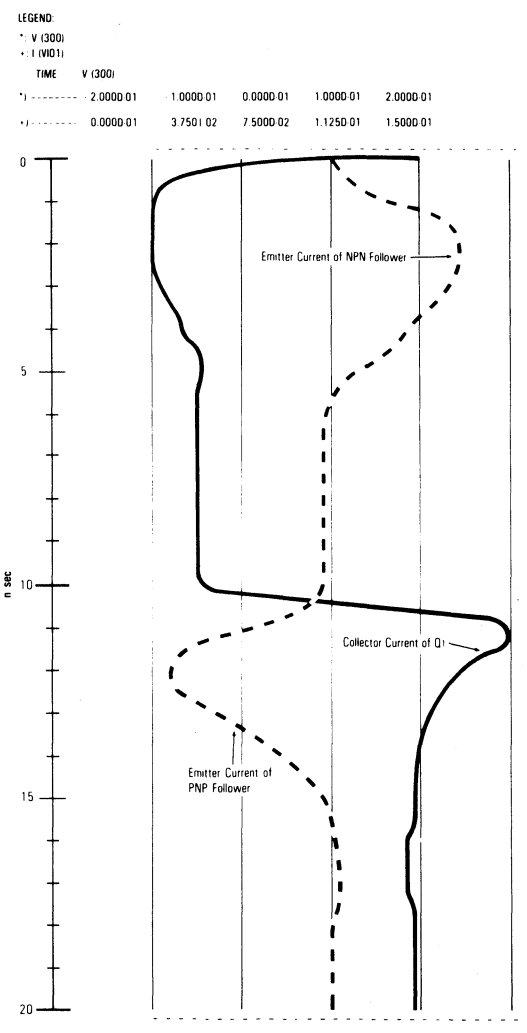


Figure 4. Computer Generated Current Waveforms

A Hybrid Video Amplifier For High Resolution CRT Applications

Motorola RF Devices has used their unique high frequency RF semiconductor capabilities and thin film hybrid expertise to produce a hybrid video amplifier with less than 2.9 ns rise and fall time for a 40 V output swing. This video amplifier provides a low power dissipation solution to a problem that has been limiting the performance of ultra high resolution CRT monitors: video amplifier speed. Many of the 1024 x 1024 and 1280 x 1024 pixel, 64 kHz horizontal sweep rate CRTs that are used in CAD/CAM and high resolution graphics applications have not realized their potential performance because of the speed of their video amplifiers. Video amplifiers with 3.5-4 ns rise and fall times often found in these high resolution CRTs do not provide optimum picture quality when the CRT has approximately 10 ns to energize each pixel. A slow video amp will produce dimmer vertical lines than horizontal lines or may force monitor designers to other compromises such as a slower sweep rate which may produce flicker, or lower cathode voltage which will produce a dimmer picture. The hybrid described here solves these problems.

SUMMARY

The Video Amplifiers, CR2424 and CR2425, are hybrid integrated circuits designed for high resolution CRT Video Amplifier applications. They are capable of delivering 40 volts peak-to-peak output with overshoot typically less than 5% into an 8.5pf load. Typical 10-90% transition times are 2.6 nsec with a bandwidth of better than 130MHz. They have excellent gray-scale linearity, are dc coupled and do not require an external load-resistor.

CONSTRUCTION

A. Mechanical

The amplifier is housed in a proven package, which consists of a plastic housing, attached to an aluminum heatsink. Dimensions and pin configurations are shown on the attached specification sheets. The circuit uses special silicon transistors mounted on heat spreaders on an alumina substrate with thin-film resistors and gold metalization. The substrate is soldered to the heatsink.

The heatsink is supplied in two versions, CA Low Profile which is designated CR2424, and a taller heatsink version, CR2425. These two package styles are shown in Figure 1. The electrical characteristics of these two amplifiers are identical. The heatsink style choice should be based on ease of mechanical/electrical interface. In both cases, the heatsink is at ground potential and should be attached directly to the chassis or external heatsink for mechanical stability and heat conduction to ambient.

This CR2424 hybrid driver can also be supplied in a hermetically sealed package. The hermetic version is designated CR2424H and can be screened to Mil Std 883 method 5008.

B. Electrical

The circuit uses bipolar silicon transistors in a two-stage feed-back amplifier configuration. The output is supplied by emitter-followers. Because of the complementary circuitry employed, there is no need for a load (or pull-up) resistor.

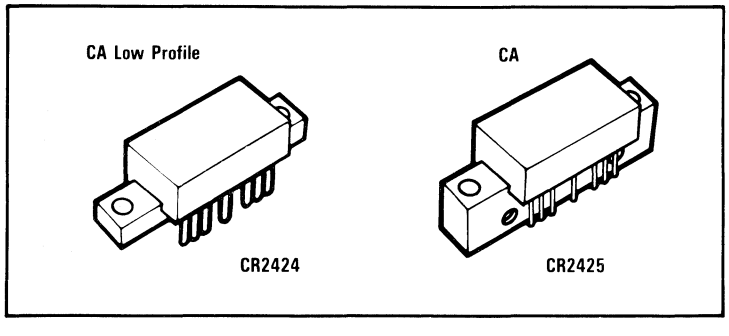


Figure 1. Package Types

The power consumption is typically 3.0 watts for average picture content and a maximum of 6.0W for 10ns continuous black to white transitions or worst case situations. The electrical pin connections are shown in Figure 2.

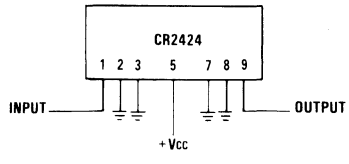
C. Thermal

Thermal analysis of an amplifier design is a very essential issue to ensure amplifier reliability. Heat is one of the most critical factors that determines how long the amplifier operates.

The ability to examine the CRT circuit thermally under operating conditions is absolutely necessary. The infrared microscanner was used for evaluation of the CRT hybrid amplifier from the standpoint of thermal resistance and operating temperature.

With the heatsink temperature stabilized at 60°C, the maximum transistor junction temperature was measured at 108°C. This is a very safe value, especially for devices with all gold metalization as used here. The maximum temperature occurs when the output voltage is either at its lower or upper extreme. Under this condition the maximum power dissipation on the die will be approximately 1.6W. Thus, the thermal resistance can be calculated to be 30°C/W.

Under normal operating conditions (normal operating conditions means an average picture content) the hottest transistor will dissipate approximately 1W. Again, with the heatsink temperature stabilized at 60°C, the transistor junction temperature will be 60°C + 30°C/W x 1W = 90°C. This is a very safe value for this kind of amplifier for a long life time.



(CASE 714G-01, STYLE 1)

Figure 2. Pin Configuration P/N CR2424

APPLICATIONS

A. Output Characteristics

The hybrid is intended to be used as the final stage of very fast video circuits. Properly driven, it can produce continuously alternating 10 nsec pixels with 40 volts swing and excellent brightness. The nominal load-capacitance is 8.5pf. Other values may be accommodated, since the output voltage is supplied by a pair of emitter followers, and is fairly insensitive to changes in load capacitance.

Often a wire connection of some length between the output of the module and the CRT cathode cannot be avoided. In this case a resonant circuit is formed, which may cause objectionable ringing or overshoot at its resonant frequency. To avoid this condition a damping resistor must be used in series with the lead inductance. For critical damping the value of this resistor becomes

$$R = 2 * \sqrt{\frac{L}{C}} \quad (1)$$

A resistor is often desired at this position also for protection against arcing. In practice, the optimum value of resistance may be determined experimentally during the bread-boarding stage. Typical values are 50 to 100 ohms. The lead-inductance may be artificially increased by a few tenths of a microhenry to obtain a desired peaking effect. Any change in inductance will require readjustment of the damping resistance, as stated by Equation (1).

A short piece of cable (75 or 93 ohm) or 300 ohm twin-lead, terminated by a capacitance, will act similar to an inductance in the frequency range involved. In this case a damping resistor must also be used.

The output terminal of the hybrid is not short-circuit proof. Any resistance from this point to either ground or B+ should not be less than 600 ohms.

B. Input and Transfer Characteristics

The dc transfer characteristics of the module are shown in Figures 3, 4 and 5.

It is seen from Figure 3 that, at dc, an input current swing of ±6.25mA causes the output voltage to change by ± 20 volts. The next plot (see Figure 4) relates the input voltage, as measured at RF input port to the output voltage. The amplifier is phase-inverting. The ratio between these voltages is approximately 13.5. From the above values, one may calculate a low frequency input impedance of ∼240 ohms at the RF input port.

Figure 5 is a plot that relates the input voltage, as measured immediately at module terminal 1, to the output voltage. The ratio between these voltages is approximately 230. From the above values, one may calculate a low-frequency input impedance of ∼15 ohms at Pin 1.

Pin 1 is an internal dc feedback node and thus, as we can see, has a low impedance looking in from the outside. Pin 1 must be fed from a series network made up of a resistor with a shunt capacitor for high frequency pre-emphasis. An appropriate input network is shown in Figure 7 and is included as part of the standard test fixturing.

With the input terminal open, a dc level of approximately 1.4 volt exists at this point. Under this condition the module output voltage is approximately one-half of the supply voltage applied.

GENERAL CONSIDERATIONS

A. Test Circuit

The test circuit used to evaluate the hybrid module is shown in Figure 7.

The input is driven from a fast pulse generator, such as the Tektronix model PG502. It is important that the internal generator impedance is 50 ohms. It is also advisable to keep the cable length between the generator and the test circuit at a minimum; preferably only a barrel connector is used.

Since the module is dc coupled, the input drive voltage must be adjusted such that the driving wave form is centered around 1.4 volts. If the pulse generator used should not allow the setting of the dc level, a biasing current, injected at module terminal 1, through a resistor of more than 1 kiloohm, may be applied in order to adjust the desired quiescent point of the output voltage.

The output is taken from terminal 9 with an active FET oscilloscope probe fitted with a 100:1 voltage divider. This probe adds 1.5pf to the load capacitance, bringing the total load capacitance to 8.5 pf.

The input circuit contains a series resistor and capacitor in parallel, which is tuned for good response when driving with a 50 ohm pulse-generator. These components perform a RC "peaking" circuit.

B. Practical Circuits

The module is best driven from a low-impedance source, such as an emitter follower. The reader is invited to experiment with a circuit as shown in Figure 8.

The driver transistor can be an LT2001, biased at about 30mA. The collector lead must be by-passed for RF as close to the transistor as possible. For all common-collector (or common-base) circuits, a base resistor of ∼20 ohms is recommended. It helps suppress spurious oscillations, which may occur in the GHz range and are difficult to detect. Resistors R_1, R_2 and R_3, and capacitor C_1 and coil L_1 are adjustable for desired circuit gain and response. Typical values may be:

$R_1 \approx 50\Omega$
$R_2 \approx 215\Omega$
$C_1 \approx 90pF$
$R_3 \approx 50\Omega$
$L_1 \approx 50nH$

The pulse generator used should allow changing the dc level in order to set a quiescent bias point of about 1.4V at the input of the module.

C. Frequency Response

In the literature and in many equipment specifications frequency response and rise-times are often treated as having a fixed relationship. The equation frequently quoted is

$$t_{r(10\text{-}90\%)} = .35 \quad f_{3dB} \quad (2)$$

It can be shown that (2) indeed applies for the simple case of a single-pole R-C network. In reality, video amplifiers have much more complicated transfer functions, and the above equation holds true only in a very general way.

In addition to the proper gain response, another amplifier characteristic is of great importance. Since a symmetrical square wave consists of a fundamental frequency and odd harmonics thereof, the preservation of the phase-relationship between all frequency components, while passing through the amplifier, must be guaranteed. This requirement is tantamount to specifying a "linear-phase" response or, in other terms, a uniform delay. Amplifiers having constant group delay exhibit smooth, monotonically decreasing frequency-response curves. One must be wary of responses which show ripple or peaking at high frequencies. Although sometimes impressive in terms of bandwidth, such amplifiers often have poor transient response. Shown in Figure 6 is the sine-wave frequency response of the CR2424 in its test fixture with the input variables previously adjusted for best rise and fall times. The output voltage is 20V peak-to-peak. The sine-wave signal generator has a 50 ohm internal impedance. The −3dB point occurs at about 200MHz. For 40V output swings the −3dB bandwidth is typically 145MHz. Actual photographs of CR2424 output waveforms driving a 8.5 pf load are shown in Figure 9.

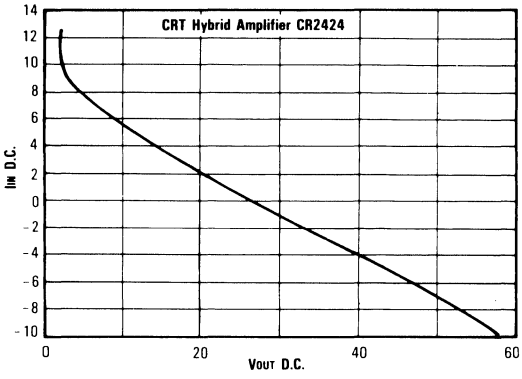


Figure 3. Output Voltage versus Input Current

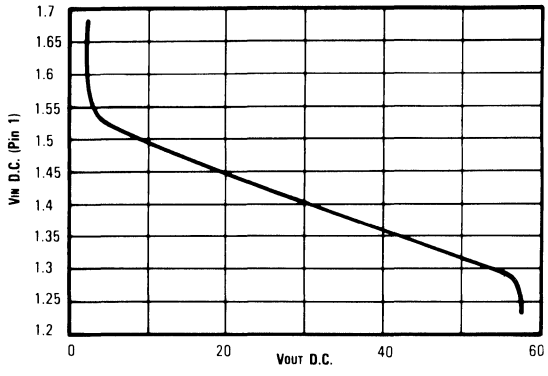


Figure 5. Voltage Ratio at Port 1

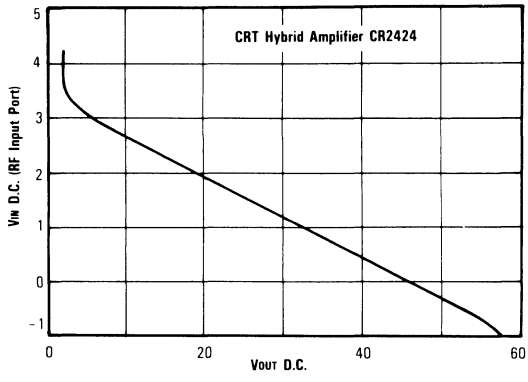


Figure 4. Voltage Ratio at RF Input Port

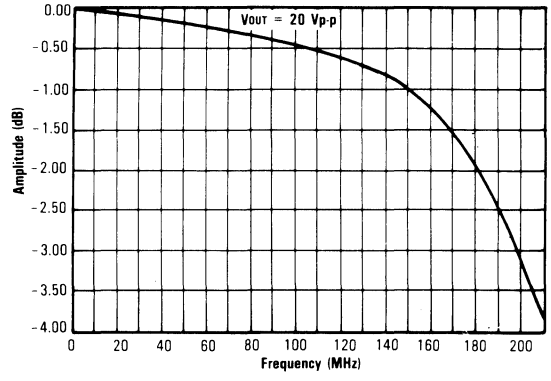


Figure 6. Frequency Response of CR2424

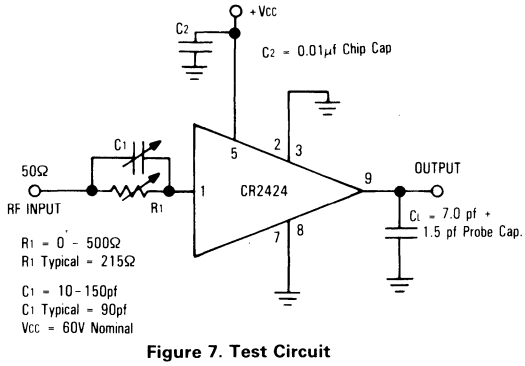


Figure 7. Test Circuit

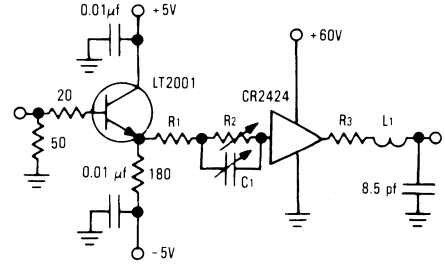
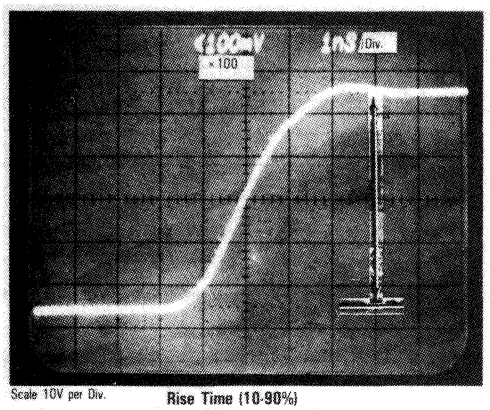
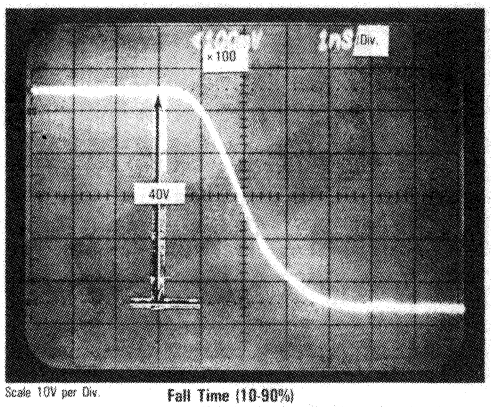


Figure 8. Experimental Circuit



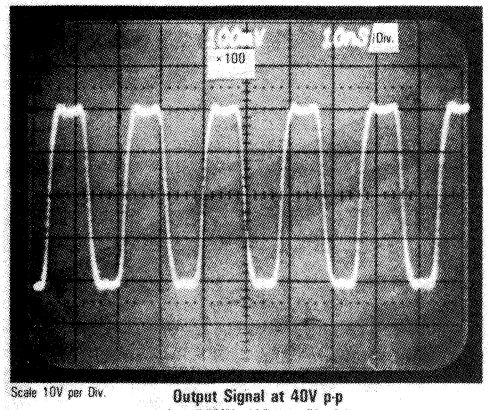
Scale 10V per Div.

Rise Time (10-90%)
t_r = 2.2nsec t_r typical = 2.5nsec



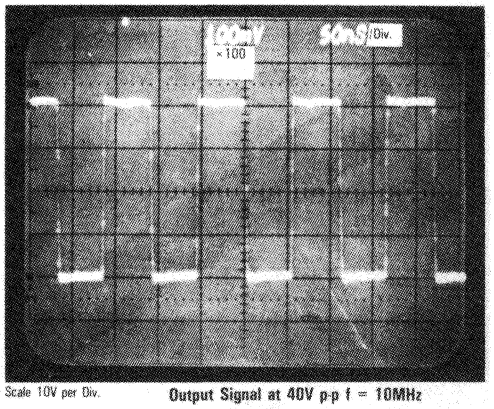
Scale 10V per Div.

Fall Time (10-90%)
t_f = 2.2nsec t_f typical = 2.5nsec



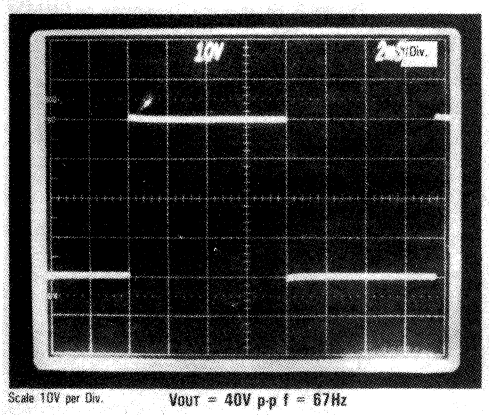
Scale 10V per Div.

Output Signal at 40V p-p
f = 50MHz (10nsec Pixels)



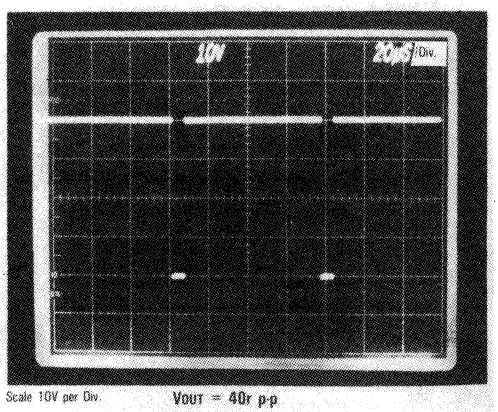
Scale 10V per Div.

Output Signal at 40V p-p f = 10MHz



Scale 10V per Div.

V_{OUT} = 40V p-p f = 67Hz



Scale 10V per Div.

V_{OUT} = 40r p-p

Figure 9. CR2424/2425 Output Waveforms Across 8.5 pF Load

AN1022

Mechanical and Thermal Considerations in Using RF Linear Hybrid Amplifiers

Prepared by
Don Feeney
Motorola RF Devices

ABSTRACT

Motorola's thin film hybrid amplifiers are medium power (0.2 W to 2.0 W power output) broadband devices (1 to 1000 MHz) that are biased in a class A mode for linear operation. To insure a proper electrical/mechanical interface with adequate RF/thermal characteristics, certain guidelines are presented for the design engineer to obtain maximum electrical performance and the longest operating life.

THERMAL CONSIDERATIONS

A question that often arises from engineers using our hybrid amplifiers is "What is the thermal impedance?" Thermal impedance (expressed as θ_{JC}) is a very real and important parameter for the RF design engineer using discrete solid state devices. However, this term loses its meaning in a multistage hybrid amplifier. Each stage may be biased at different quiescent conditions resulting in different junction temperatures under a given set of environmental conditions. Additionally, hybrid circuit design engineers may speak of θ_{JC} referring to the thermal impedance of a single transistor die mounted on a hybrid circuit using their particular assembly processes. However, this term has no meaning to the customer using their product who can only compute the power consumption of the total amplifier.

To avoid this confusion, Motorola RF Devices simply rates the maximum operating case temperature for their RF linear hybrid amplifiers. These amplifiers are designed so that under the worst case operating conditions, the maximum junction temperature of any of the transistor die will be below 150°C. This junction temperature correlates with our two years of accumulated reliability data which predicts an MTBF in excess of 142 years.

HEATSINK YOUR HYBRID

Like all RF power devices, hybrid amplifiers require heatsinking for proper operation. How much heatsinking is necessary? As much as is required to maintain the case operating temperature at the maximum value under worst case ambient temperature and maximum supply voltage. The presence or absence of the RF signal is insignificant due to the class A bias conditions. Reducing the supply voltage will decrease the power consumption, but it will also decrease the linearity. Attach the hybrid amplifier directly to the chassis, to a module card sidewall, to a small baseplate, or to a mounting bracket that is connected to one of the above. But before you complete your design, verify that the maximum case (flange) temperature for the hybrid amplifier is within the manufacturer's specified limits under your worst case operating conditions.

One additional note of caution. DO NOT attempt to lap or file the heatsink of the hybrid amplifier. Not only does this void the warranty (considered "mishandling" by the manufacturer), but you can induce substrate cracking during the machining operation. If you need a shorter heatsink, consider the hermetic package option or the low profile package available on some models. Motorola RF linear hybrid amplifiers are shipped with a mounting surface flatness of ±.002". To improve heatsinking, thermal grease can be used.

PRINTED CIRCUIT BOARD INTERFACE

All Motorola RF linear hybrid amplifiers are internally matched to a nominal characteristic impedance of 50 or 75 ohms, both at the input and the output. This not only reduces the external components normally required to match to these impedances in discrete designs, but it also simplifies the requirements for interfacing printed circuit board connections — for short path lengths, strip line width has little effect on RF performance.

Motorola RF linear hybrid amplifiers feature .020" diameter gold plated pins[1] spaced at .100" centers. Nominal pin length is .460" (.375" for hermetic package).[2] There is provision for a total of nine pins, but unused pins will be missing (refer to pin configuration diagram for the particular hybrid amplifier). Viewing the hybrid from the top, pin 1 is identified on the left. This is the RF input, usually transformer coupled.[3] The two adjacent pins are ground connections. The middle three pins are reserved for power supply connections. Positive polarity units have the power supply in pin located in the middle.[4] Units designed to operate from a negative supply have the power supply connection offset one pin to the left to guard against inadvertent installation in an improper test fixture. The extreme right hand pin is the RF output, and the two adjacent pins are ground connections. All ground connections are internally connected to the flange, except as noted on the functional schematic (refer to particular data sheets).

EXTERNAL COMPONENTS

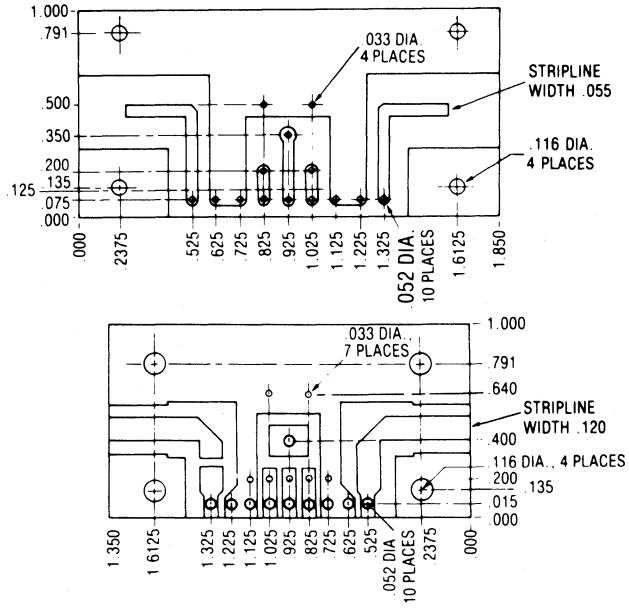
Although it is not specified as a requirement on the data sheets, it is usually good RF practice to add a low impedance RF bypass capacitor (e.g., 0.1 μF chip capacitor) located near the power supply pin. Additional decoupling is normally not required. However, some Motorola RF linear hybrids require external chokes and capacitors for proper operation.[5] Chip capacitors are recommended. A broadband 30 μH RF choke may be constructed by winding 30 turns of #36AWG magnet wire on a Ferroxcube 891 T050/4C4 core (alternate core is Indiana General P/N CF 12001). With an accompanying order of hybrid amplifiers, this choke may be procured through Motorola.

For Motorola hybrid amplifier model CA2820, the external chokes isolate the transistor from the power supply. Positioning of these chokes will have an effect on the high frequency end of the amplitude response.

TEST FIXTURES

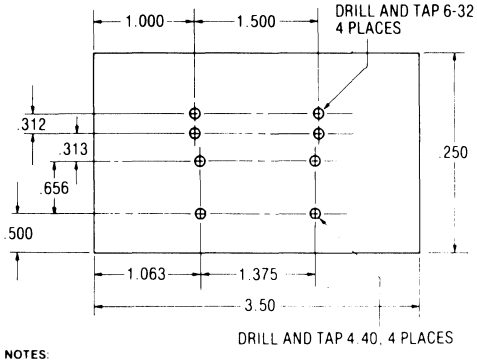
Figures 1 through 10 detail the assembly of standard test fixtures for Motorola's line of RF linear hybrid amplifiers. Much of this mechanical information will prove useful to the engineer who is designing one of these units into his equipment. The details of the test fixture assembly for the CA2820 presented in Figure 7 apply to most of the standard RF linear hybrid amplifiers (just substitute PC boards, adjust pin spacing, and remove external components as required). Special provisions for adapting this same test fixture for the low profile package, the bent pin option, and the hermetic package option are presented in Figures 8, 9, and 10.

[1] Pin diameter for hermetic package is .018".
[2] These pins will mate with sockets manufactured by Amphenol (P/N 502-20071-572) and Barnes (P/N 027-018-02).
[3] Except for CA2820, which has an internal DC blocking capacitor at the input.
[4] Except for CA2820 and CA2870. Refer to individual data sheets.
[5] e.g. CA2820, CA2870



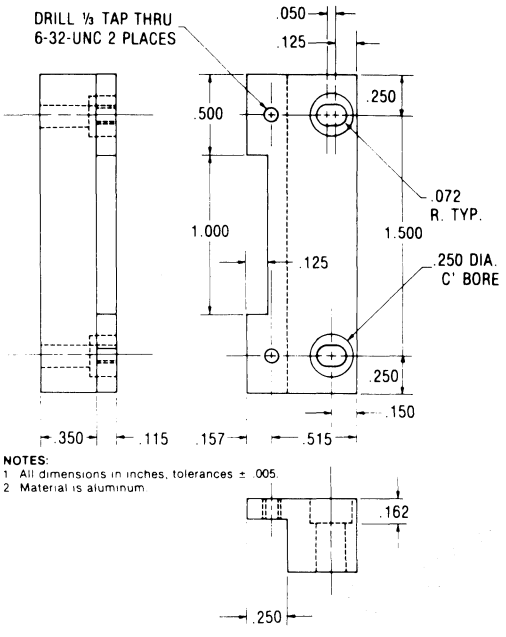
NOTES:
1. All dimensions in inches, tolerance ± .005.
2. Material is double sided glass epoxy (G10), 1/16" thickness, 1 oz. cooper, solder plated.
3. TF-06 used for CA2820 only. All other models use TF-03.

Figure 1. PC Board Construction for Hybrid Amplifier Test Fixtures



NOTES:
1. All dimensions in inches, tolerance ± .005.
2. Material is 3/8 aluminum.

Figure 2. Heatsink Base Plate Construction for Hybrid Amplifier Test Fixture



NOTES:
1. All dimensions in inches, tolerances ± .005.
2. Material is aluminum.

Figure 3. Adapter for Hermetic Package to Standard Hybrid Amplifier Test Fixtures

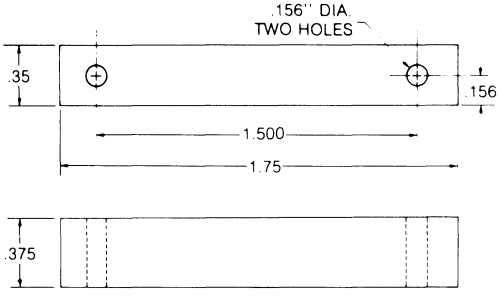


Figure 4. Adapter for Low Profile Package to Standard Hybrid Amplifier Test Fixtures

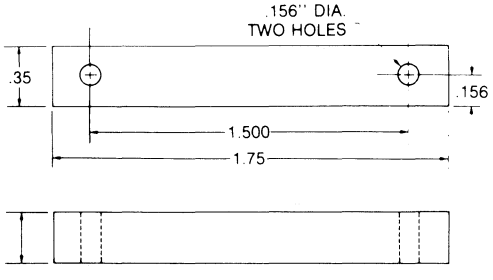
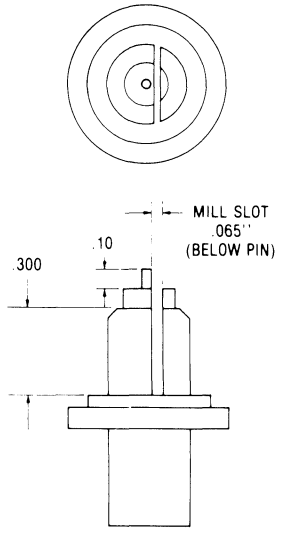


Figure 5. Spacer for Bent Pin Package Option to Standard Hybrid Amplifier Test Fixtures



AMPHENOL P/N US-625/U (50Ω)
TROPOMETER P/N UBJ-20 (75Ω)

Figure 6. Modifications to BNC Connector

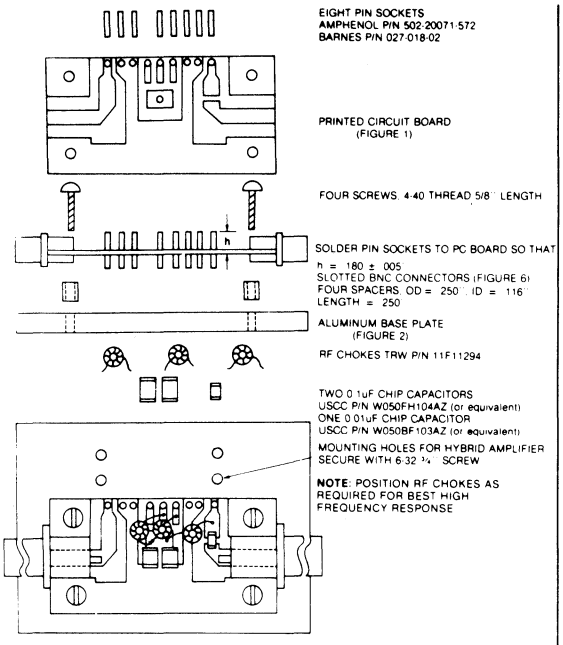


Figure 7. CA2820 Test Fixture Assembly (Case 714F-01)

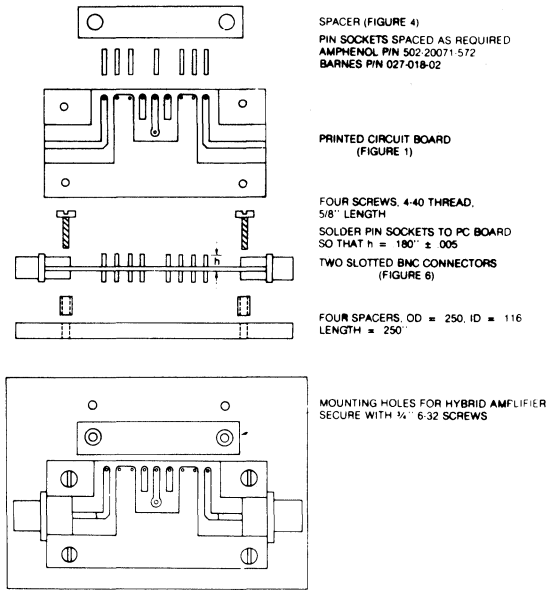


Figure 8. Text Fixture Assembly for Hybrid Amplifiers in Low Profile Package (Case 714G-01)

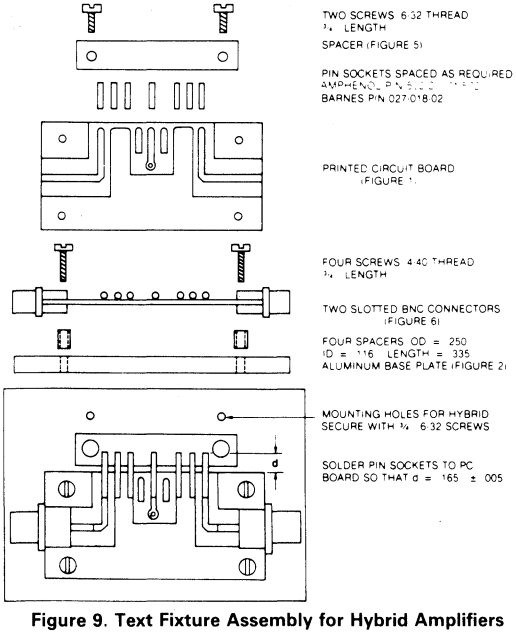


Figure 9. Text Fixture Assembly for Hybrid Amplifiers with Bent Pin Option (Case 714J-01)

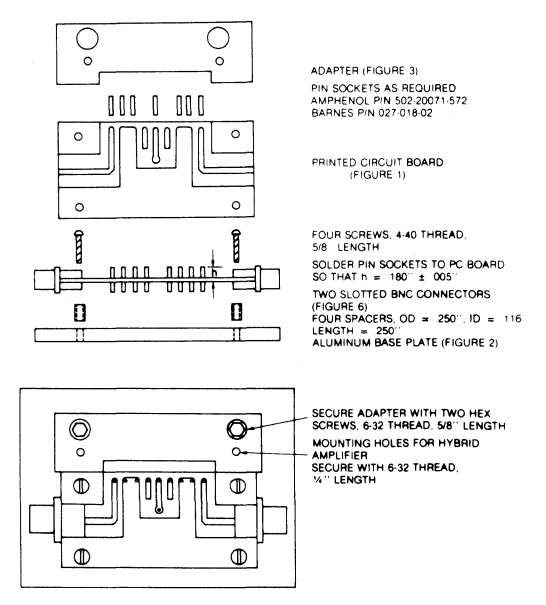


Figure 10. Test Fixture Assembly for Hybrid Amplifiers in Hermetic Package (Case 826-01)

AN1025

Reliability Considerations in Design and Use of RF Integrated Circuits

Prepared by
James Humphrey and George Luettgenau

ABSTRACT

Reliability is a major factor in the profitability of CATV Systems.

In spite of its proportionally low cost, the RF integrated circuit figures prominently in the overall reliability picture. This complex and important function is located at strategic points in the system.

Fortunately, modern design and manufacturing technology, which draws extensively from resources generated by military and space activities, assures a degree of reliability which is compatible with the most stringent requirements.

Transistor chips are the most vital elements of the RF integrated circuit. Low noise and distortion require state-of-the-art transistor structures. Gold metallization, thermal equilibrium by means of diffused balancing resistors, as well as automated process control have resulted in transistor lifetimes of over 100 years.

One of the inherent reliability advantages of IC's is the reduced number of interconnects. The full benefit of this characteristic is achieved through the use of gold conduction paths in conjunction with gold wire bonding. Perhaps the single most dangerous enemy of high reliability is excessive heat. Careful, computer-aided circuit design coupled with thermally sound, stress-free mechanical construction guarantee structural integrity and safe operating temperatures under all practical conditions. Infrared scanning helps verify the achievement of design goals.

Abuse or abnormal stresses may counteract the best of reliability. In order to avoid problems, the user must control the electrical, thermal, and mechanical environment surrounding the RF IC. Much progress in this respect has been made by the equipment industry.

INTRODUCTION

Reliability considerations are becoming increasingly important in the operation of CATV Systems, requiring an absorption of military and aerospace reliability technology into the CATV business. Market surveys show a large number of MSO's and consultants consider reliability as a major item in equipment selection.

A definition of major reliability terms is important along with an introduction to microcircuit reliability tools (both hardware and software).

An overview discussion of Physics of Construction involved with the die and interconnects must be presented.

DEFINITIONS

R = Reliability

Reliability is related to the probability that an item will perform a defined task satisfactorily for a specified length of time, when used for the purpose intended, and under conditions for which it was designed to operate.

Failure

Failure is a detected cessation of ability to perform a specified function within previously established limits in the area of interest.

(a) Dead on arrival
(b) Infant mortalities
(c) Lifetime failure rates (random)
(d) End of life (wearout)

MTBF (Mean Time Between Failures)

The total measured operating time of a population of equipment, divided by the total number of failures within the population during the measured period of time.

Average Life

The mean value for a normal distribution of lives, and generally, it applies to failures resulting from wearout.

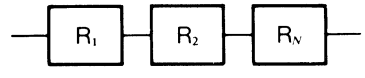
BASIC RELIABILITY EQUATION

$$R = e^{-t/m} = e^{-\lambda t}$$

Where: R = Reliability or probability of success
t = Mission time in hours
m = MTBF in hours = $\frac{\text{hours}}{\text{failures}}$
λ = Failure rate = $\frac{1}{\text{MTBF}} = \frac{\text{failures}}{\text{hours}}$

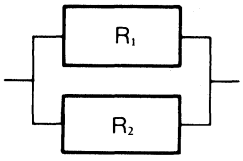
SYSTEM RELIABILITY

1. When components are in series, failure of any one of the components will result in failure of the system.



Then: $R_{SYSTEM} = R_1 \times R_2 \times R_3 \times \text{---} R_N$
$\lambda_{SYSTEM} = \lambda_1 + \lambda_2 + \lambda_3 + \text{---} \lambda_N$

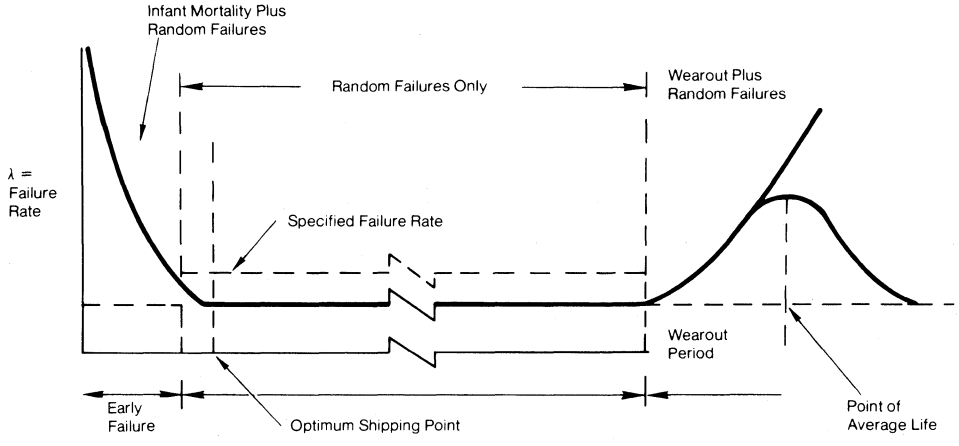
2. When the same components are in parallel (redundancy) neglecting, for simplicity, the decision-making device, the switchover function and the fail safe requirements:



$R_{SYSTEM} = R_1 + R_2 - (R_1 R_2)$

RELIABILITY CURVE

The following curve represents the typical condition of operational reliability.



RELIABILITY PREDICTION ALGORITHM

The military has put considerable money and time into the study of reliability. One very useful military document is Military Handbook 217B, *Reliability Prediction of Electronic Equipment*. This handbook shows how to develop failure rate predictions by the use of mathematical models based on years of data collection by military agencies. A discussion of the interaction of components in the model is very useful in gaining an understanding of the overall subject.

PART FAILURE RATE MODEL λ_p

$\lambda_p = \lambda_b (\pi_T \times \pi_E \times \pi_Q \times \pi_F \times \pi_M)$

Where:
- λ_p = Part failures in failures per 10^6 hrs.
- λ_b = Base failure rate
- π_T = Temperature adjustment factor
- π_E = Environmental adjustment factor
- π_Q = Adjustment factor based on quality
- π_F = Adjustment factor for circuit function
  - = 0.8 for digital hybrids
  - = 1.0 for linear hybrids
  - = 1.1 for combination hybrids
- π_M = Adjustment factor for maturity of product

BASE FAILURE RATE MODEL λ_b

$\lambda_b = \lambda_S + A_i\lambda_c + \Sigma\lambda_{RT}N_{RT}$ (Substrate contribution)
$+ \Sigma\lambda_{DC}N_{DC}$ (Attached components contributions)
$+ \lambda_{PF}\pi_{PF}$ (Package contributions)

Where:
- λ_b = Base failure rate in failures/10^6 hr.
- λ_S = Failure rate due to the substrate and film processing
- $A_i\lambda_c$ = Failure rate contributions due to network complexity and substrate area which includes:
  - (a) Number of lead terminations
  - (b) Number of film resistors
  - (c) Number of discrete chip devices
  - (d) Type of film (thin versus thick)
- $\Sigma\lambda_{RT}N_{RT}$ = The sum of the failure rates for each resistor as a function of the required resistance tolerance
- $\Sigma\lambda_{DC}N_{DC}$ = The sum of the attached device failure rates for semiconductors and capacitors
- $\lambda_{PF}\pi_{PF}$ = The hybrid package failure adjusted to include material and style

PHYSICS OF CONSTRUCTION

Following the enumeration and identification of symbols used in reliability algorithms, a discussion of the major microelectronic components with respect to their reliability contributions is in order:

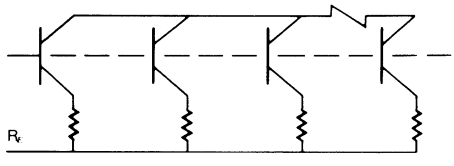
TRANSISTORS

The transistor die is the heart of the hybrid amplifier. With four to eight devices per circuit, the transistor determines performance and is most critical to proper circuit operation.

During the last few years users have witnessed major advances in the performance of linear broadband transistors. Often, efforts to improve one characteristic have adverse effects on other desirable features. For instance, distortion may be bettered by thinning the epitaxial collector region. This, however, leads to sensitivity to voltage transients and other abnormal operating conditions. Therefore, devices with outstanding performance in one area are prone to weakness in others. Computer-aided device design coupled with volume production and tight process controls have resulted in transistors in which all essential features are in proper balance.

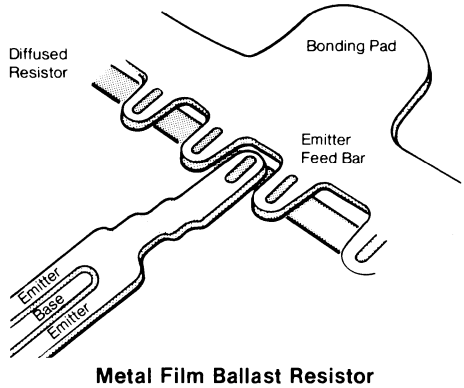
High f_T is generally recognized as an important factor in achieving wide bandwidth and uniform distortion characteristics. Gigahertz transistors, which are now being used, have very delicate patterns, involving micron and submicron tolerances. They also occupy sizable areas on the silicon wafer, since watt-sized powers have to be handled. It is only realistic to expect that all parts of the overall transistor structure are not perfectly alike, but rather resemble the parallel configuration of many, slightly differing, small devices, as shown in the figure.

Ballast Resistors

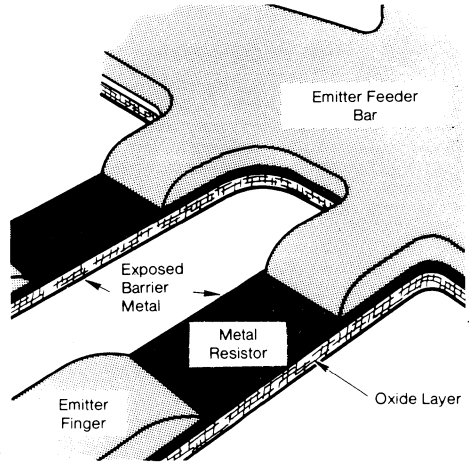


It is also apparent that the entire transistor geometry cannot be tightly thermally coupled within itself, therefore giving rise to the possibility of small sub-areas of the transistor assuming different values of temperature than others. This possible problem can be effectively combatted by adding emitter balancing resistors to the device. Ideally each emitter-site or finger should have its own resistor. This goal is easily realized in interdigitated structures. Film or diffused monolithic resistors may be used. From a process and reliability point of view, diffused resistors are preferred because they avoid the silicon-oxide barrier which has a very high thermal resistance.

Diffused Ballasting System
(Only one emitter contact shown)



Metal Film Ballast Resistor



METAL MIGRATION

Some time ago a serious failure mechanism, associated with GHz transistors, was discovered. The metallization stripes of such devices, as mentioned earlier, are only a few microns wide. The metal thickness is, because of fabrication limitations, of similar dimensions. Consequently, the current density in these stripes is quite high, often reading hundreds of thousands of amperes per cm^2 of cross-section. Under these circumstances, metal migration may occur. With such large numbers of electrons flowing in such crowded space, the probability of collisions with thermally activated metal ions is great. The ions are propelled in the direction of electron current flow causing, in the long run, the metal to move, forming hillocks, whiskers and voids. The lifetime of a transistor is a function of three things: the current density, the temperature, and the type and consistency of metallization.

Not much leeway exists in reducing the current density (unless f_T is sacrificed). Changing from aluminum to gold extends the life at least by an order of magnitude. At high temperatures the difference is even more pronounced. At 150°C, the time to metal failure for gold metallization microwave transistors is in excess of 10^6 hours = 114 years. While this number is quite comforting, one is not at liberty to treat the subject of transistor chip heat-sinking too lightly. A proven method for removing heat while at the same time obtaining a solid mechanical mount, has been to employ a heatspreader between the silicon chip and the IC substrate. Automatic mounting stations are used to eutectic collet mount the chip to indexed leadframes. Tight control of pressure and scrub sequence result in defect free attachment. Although one may employ other methods of heatsinking, e.g. beryllium oxide substrates for part of the circuit, the added mechanical complexity and the reduced freedom of optimal circuit layout presently outweight the minor advantages resulting from a reduction in transistor temperature.

INTERCONNECTS

One of the most important parts of hybrid circuits is the interconnect system. The ability to reduce the number, control the quality, and test them by screening complete functions, is one of the major advantages of hybrid circuits over more conventional approaches. Constant improvement in the mechanical and metallurgical systems have drastically improved reliability.

An analysis of the schematic on the standard 33dB Hybrid Amplifier will illustrate the point:

Comparing hybrid versus discrete techniques, one can show the following:

1. For each transistor used, a minimum of three interconnects corresponding to the solder joints at the PC board are eliminated.
2. For each capacitor used, a minimum of two interconnects are eliminated.
3. For each film resistor used, a minimum of four interconnects are eliminated corresponding to the connection to the resistor body and the connection to the PC board.
4. Transformer interconnects will be the same for hybrid or discrete.

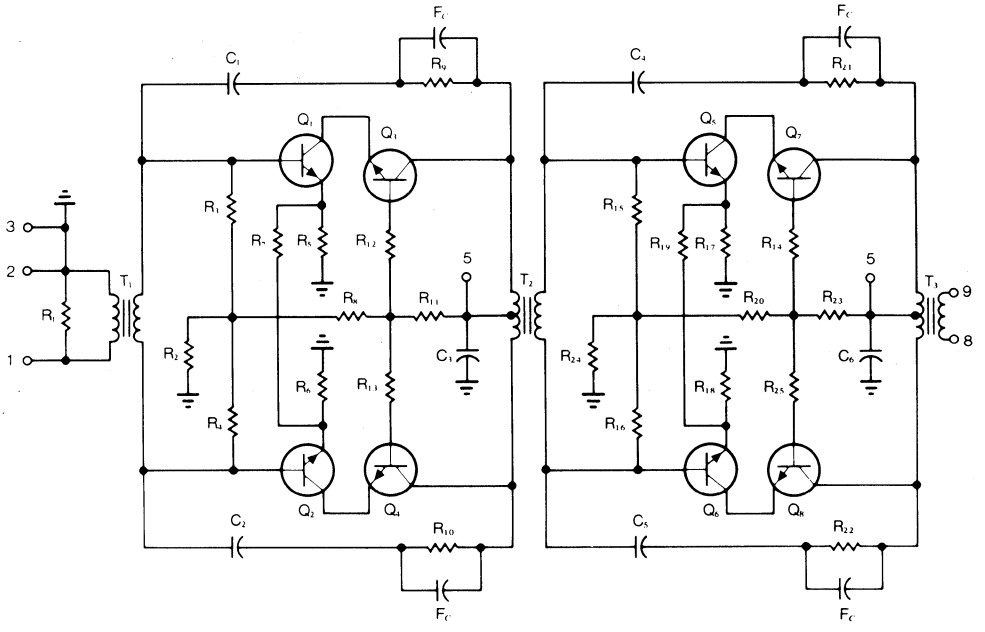
The increase in interconnects in building 33dB of gain in discrete form over the same circuit in hybrid form is:

Add due to transistors	=	24
Add due to chip capacitors	=	12
Add due to resistors	=	100
Add due to transformers	=	0
Less due to hybrid jumpers	=	-4
Less due to active pins	=	-5
		127 Additional interconnects per 33dB function

MIL Handbook 217B also discusses the reduction in reliability of printed circuit boards as a direct multiple of the holes required. Eighty-one additional holes are involved in making one discrete amplifier.

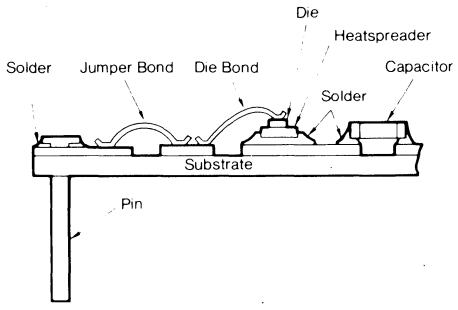
Having the interconnects made early in the manufacturing sequence, before the subsequent series of tests and inspections, has beneficial influence on end equipment reliability.

33dB Gain Block



The complete functional system including interconnects is tested, screened and Q.C. sampled many times before it even meets up with the PC board in the manufacturers subsystem.

Interconnects



COMPONENT MOUNT

The transistor heatspreaders, chip capacitors and pin connections are soldered to the metallization pattern on the substrate surface. This process is completed in a tightly controlled solder reflow furnace.

Due to the fact that the units are processed in an inert atmosphere and thoroughly cleaned and inspected early in the production process, workmanship problems are greatly reduced.

BONDS

Wire bonding was a major reliability issue for years.

Aluminum has been one of the most widely used bonding systems in the hybrid industry for many years. The main reason for this is that ultrasonic aluminum systems bond at room temperature and, hence, do not interfere with other hybrid assembly processes.

Gold thermal compression ball bonding has been a reliable standard process in the semiconductor industry for years. However, the requirement for 300°C bonding temperatures have kept this technique out of most hybrids. The recent changeover to all gold hybrids prompted the development of a compatible low temperature gold wire bonding system which by far out-performs aluminum.

Advantages of Aluminum Bonds

Low temperature process
Compatible with Al die metal
Low cost
High speed
Easy to loop (stiff)

Disadvantages of Aluminum Bonds

Degrades with time/temperature
Kirkendall voiding
Intermetallic formation with gold
Brittle and subject to cracks
Difficult to screen
Difficult to control

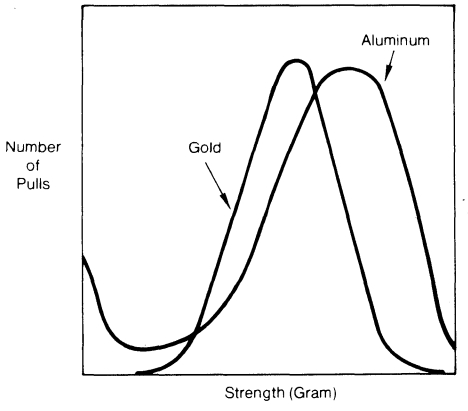
Advantages of Gold Bonding

Compatible with gold die and substrate
Strength stable with time/temperature
Malleable — not subject to cracking
Easier to control process

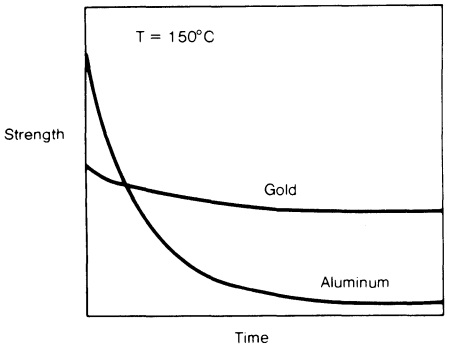
Disadvantages of Gold Bonding

More expensive
More deformation at bond foot
Hard to form loops

Histogram of Gold Versus Aluminum Bond Strengths



Strength Versus Time on Gold Versus Aluminum Wire



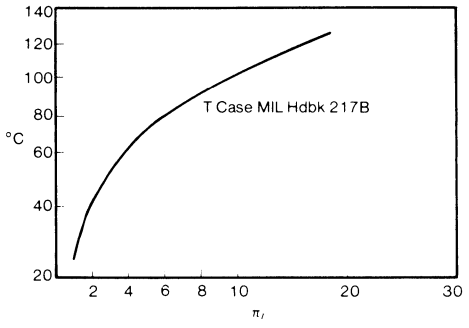
RELIABILITY ADJUSTMENT FACTORS

Following is a discussion of the "π adjustment factors" in MIL Handbook 217B. These relate to the external influences on hybrid circuit reliability.

TEMPERATURE ADJUSTMENT FACTOR π_T

Operating temperature is one of the most important factors in reliability. As can be seen by the curve shown, great reliability improvements can be obtained by lowering the case temperature.

Failure Rate Multiplier Due to Temperature



This curve shows that a hybrid circuit, operating at a case temperature of 100°C, has four times the failure rate as the same circuit run at 50°C.

ENVIRONMENTAL ADJUSTMENT FACTOR π_E

This adjustment factor is based on the service environmental conditions that the part will be exposed to during operation.

π_E, Environmental Factor Based on Environmental Service Conditions

Environment	Symbol	π_E
Ground, Benign	G_B	0.2
Space Flight	S_F	0.2
Ground Fixed	G_F	1.0
Airborne, Inhabited	A_I	4.0
Naval, Sheltered	N_S	4.0
Ground, Mobile	G_M	4.0
Naval, Unsheltered	N_U	5.0
Airborne, Uninhabited	A_U	6.0
Missile, Launch	M_L	10.0

MATURITY ADJUSTMENT FACTOR π_M

The failure rate predicted by this mechanical model can be expected to increase by a factor of (π_M = 10) under any one of the following conditions:

(a) New device in initial production.
(b) Where major changes in design or processes have occurred.
(c) Where there has been an extended interruption in production or a change in line personnel (radical expansion).

The factor of 10 can be expected to apply until conditions and controls have stabilized. This period can extend for as much as 6 months of continuous production.

This maturity factor is extremely important. The industry has used over 400,000 CATV modules since the first module was shipped in 1970. Since that time we have constantly improved and refined the IC. Optimum reliability is an evolutionary process depending on time, volume, defect analysis and feedback to fine tune the product and eliminate defects.

The question is where does CATV fit into this table. Mechanical and thermal casting designs are extremely important in protecting the RF IC from the external environment conditions. Still, wide variations in system placement introduce a swing factor for environmental effects, which will cause π_T for CATV to fall between 1.0 and 5.0.

The user must strive to keep the components as close to laboratory zero as possible.

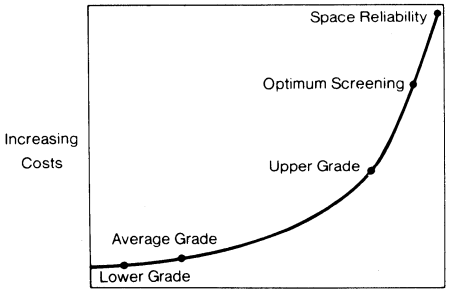
QUALITY ADJUSTMENT FACTOR π_Q

This is the adjustment factor based on the quality grade of the product. This factor modifies the reliability levels by the different quality levels specified in MIL STD 883, *Test Methods and Procedures for Microelectronics*. These levels take into account different screening levels, qualification levels and quality conformance inspection requirements for the specified class.

	π_Q
MIL STD 883 Class A	0.5
MIL STD 883 Class B	1.0
Vendor Equivalent Class B	5.0
MIL STD 883 Class C	30.0
Commercial with Screening	50.0
Commercial (No Screening)	75.0

A study of the MIL STD 883 Quality Requirements allow a very important discussion of cost versus reliability. As could be expected the test, manpower, equipment, time and paperwork go up rapidly as the MIL STD Grade is increased. A relative plot of this relationship is shown below:

Cost Versus Reliability



Many of the MIL Standard Military requirements seem unimportant in influencing CATV reliability. However, the cost versus reliability curve is real and the equipment supplier can make choices as to the type of reliability he is willing to pay for.

EQUIPMENT

It takes a massive capital investment in order to meet the manufacturing requirements for the CATV industry. The volume, quality and performance standards required have caused us to constantly reinvest for the future. Many of the invested dollars are for equipments for which the return on investment is subjective.

SCANNING ELECTRON MICROSCOPE

This instrument allows very high magnification of surface conditions not available with optical methods. Magnifications up to 100,000 times are possible with the SEM.

DISPERSIVE X-RAY ANALYSIS

This capability, which is a feature of the SEM, allows us to make a microprobe to determine the chemical composition of a sample. This is accomplished by detection of secondary emission x-rays which possess characteristic energies. The relative quantity and location of elements may then be displayed on the CRT.

VARIABLE FREQUENCY VIBRATION

This is a destructive test which is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range.

X-RAY

This is a very valuable tool for detecting voids in solder or eutectic bonds.

INFRARED MICROSCOPY

The ability to examine a circuit thermally under operating conditions is absolutely necessary when designing a new product or testing a new process. The infrared microscanner is used for evaluation of new products from the standpoint of thermal resistance and operating temperature. Resolution of 0.0005 inch can be achieved.

CONCLUSIONS

- Many reliability tools are available today both in equipments for evaluation of reliability and in analytical tools such as MIL Handbook 217B for predictions of reliability.
- Hybrid circuits offer massive reliability leverage due to:
  (a) Reduction of Interconnects
  (b) Ability to control quality by screening
  (c) Large volume of complex standard functions are easier to control
- Case temperature is very important for reliability
- A monometallic system, i.e., gold die metallization and gold wire bonding are optimum for reliability.
- Reliability can be improved by adding quality cost to the module process. This increased cost may easily be returned due to the lower failure rate.

ACKNOWLEDGEMENTS

The authors wish to thank Al Bird, TRW Systems Group, Redondo Beach, California, for his technical guidance.

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AN1027

Reliability/Performance Aspects of CATV Amplifier Design

Prepared by
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ABSTRACT

The reliability advantages to be offered by the RF hybrid amplifier as used in CATV applications are discussed. The active part of the hybrid amplifier is the transistor. Metallization, ballasting and ruggedness are reliability related factors that must be considered by the device engineer when designing a high performance CATV transistor. Vertical and horizontal geometry and device distortion mechanisms are performance related factors that must also be taken into account. The interrelation between these factors is examined. Life test data is then presented to illustrate the advantages to be gained by careful device design.

I. INTRODUCTION

The cable television system operator buys equipment which he knows has demonstrated a certain minimum level of performance, or in other words, equipment that meets his specifications. If he questions this performance he can run various electrical tests to check it.

Another question that we would like to be able to answer is, how long will his equipment operate before it fails, costing him downtime and repair. This is the question of reliability and to understand this it is necessary to understand the factors that go into designing for reliability.

The primary building block of a reliable CATV amplifier is the RF integrated circuit. This concept possesses many advantages over the PC board discrete design including a reduced number of interconnects and the ability of the manufacturer to effectively test the system before delivery to the equipment manufacturer.

Going one step further, the basic constituent of the integrated circuit is the transistor itself. It is in the design of this transistor that the ideals of high performance with reliability can be effectively realized.

The ultimate test is to see how long a part operates in the field without failing. The best way to simulate this is by means of a life test. Life test data is included as a means of demonstrating the results of a careful design.

II. WHAT IS RELIABILITY

One definition could be that reliability is something that can cost you money if you don't have it. The dictionary defines reliability as "the quality describing that which is dependable or honest." To build honest transistors and amplifiers is a noble concept but one which may be difficult to measure. So in the everyday sense, reliability is a somewhat abstract idea that is difficult to describe quantitatively. In engineering, however, reliability has an exact meaning.

> "Reliability is the probability of a device performing its purpose adequately for the period of time intended under the operating conditions encountered."[5]

When an amplifier is designed for a certain level of gain, it may happen in practice that the gain is less than that called out in the specification. In certain cases this may be acceptable if the amplifier turns out to be very reliable. However, another amplifier, which supplies the full gain with ease, may breakdown in operation because its components are being taxed to their limits. This is where reliability enters the picture. It is possible to achieve full performance and still have state-of-the-art reliability.[5] We said that reliability is the capability of equipment not to break down in operation. The measure of an equipment's reliability, then, is the frequency at which failures occur in time. A failure is a malfunction which causes the component to violate the requirement for adequate performance. The frequency of such failures is called the failure rate. The reciprocal of the failure rate is called the mean time between failures or MTBF.

λ = Failure Rate

$\frac{1}{\lambda}$ = MTBF

Referring to Figure 1, it is seen that there are three basic types of failures; early, chance and wearout failures.[2]

Early failures occur early in the life of a component and result usually from poor manufacturing. These can be eliminated by a 'burn-in' process.

Wearout failures are a symptom of component aging. These types of failures can be eliminated by either replacing at regular intervals or by designing for longer life than the intended life of the equipment if the components are inaccessible.

Chance failures occur at random intervals and are due to sudden stress accumulations beyond the design strength of the component. Since the other failure types are relatively easy to eliminate, performance reliability should be determined by the chance failures.

For chance failures only, reliability may be expressed by the exponential relationship

$$R(t) = e^{-\lambda t}$$

where λ is the failure rate and t is a given operating time; t must never exceed the 'useful life' of the device. The derivation of this reliability expression is found in the Appendix.

System failures are caused by component failures. When components can fail only because of chance, the system will fail only because of chance. The design engineer is responsible for the reliability which is characteristic of his equipment. If he desires to reduce the number of chance failures which occur during the useful life period of his equipment, he must keep several key points in mind.[5]

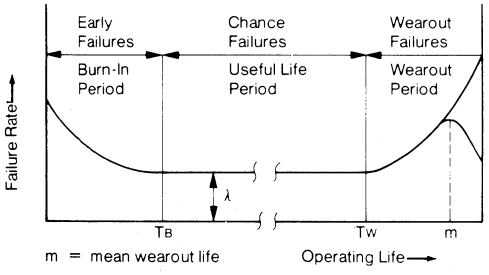


Figure 1. Component Failure Rate as a Function of Age

1. Design components to accept overstress; the normal operating point should be well below rated values, including temperature.
2. Provide good packaging with adequate heat sinking.
3. Design with as few components and interconnects as possible.

III. HYBRID CIRCUIT RELIABILITY ADVANTAGES

The hybrid circuit is the heart of the CATV amplifier. This assembly must perform its duty while experiencing a variety of electrical and environmental extremes. If the hybrid circuit should fail, then the cost to the system operator is high. For this reason the hybrid circuit should be an extremely reliable piece of equipment.

There are certain qualities of a hybrid circuit which make it an inherently reliable assembly.

One subtle advantage relates to the wear out life of components. Replacement of a hybrid circuit means replacing every amplifier component which resets the clock on the entire amplifier as far as mean life is concerned. Replacing a component in a discrete amplifier does not. All of the other discrete components continue to approach their wear out life.

The metallization system of the hybrid is another advantage. The gold metallization which is used for interconnects on the hybrid circuit allows the designer to have the high conductivity of gold for use in tying together the various components of the circuit, while having the additional reliability advantage of a monometallic gold system in wire bonding from the transistor to the hybrid. Even though the hybrid circuit utilizes heat sinking to reduce heat buildup, any bi-metallic interface will be susceptible to failure due to intermetallic formation. These gold-aluminum intermetallics are more brittle than the parent metals, and they also are susceptible to void formation due to the faster diffusion of aluminum into gold compared with gold into aluminum (Kirkendall Effect). If a hybrid circuit is manufactured using die with aluminum metallization, it is certainly preferable to use aluminum for bonding. This is because the gold-aluminum interface will then occur on the substrate, away from the heat of the transistor. This is important since the formation of intermetallics, $AuAl_2$ or Au_5Al_2, is accelerated by temperature. However, these interfaces, even though they occur on the substrate, are nonetheless sensitive to weakening. Which intermetallic compound is formed depends on the amount of gold available in the bonding area. If the gold is thin then Au_5Al_2 will be formed. If the gold is thicker then Au_5Al_2 will be formed. The end result is the same; voiding and a weak bond which eventually lifts. The entire process can be accelerated by thermal cycling whereby cracks are formed in the brittle intermetallics.[3] Data presented later illustrates the comparison between failure rates due to bond lifts in aluminum and gold systems.

Another advantage which hybrids enjoy over discrete designs is the reduction of the number of interconnects.

An interconnect is a potential failure point. Reduction of the number of these points will result in a more reliable system. A calculation of the additional interconnects required in a typical discrete amplifier over the hybrid equivalent shows an increase of 127 interconnects in the discrete version.[2] Figure 2 summarizes hybrid life test data.

So it is apparent that the hybrid structure is inherently more reliable than a discrete assembly. But the heart of the amplifier, be it hybrid or discrete, is the transistor.

Reliability Data at 95°C Case Temperature

Part Description	Unit Hours Accumulated	# Fail	MTBF With 90% Confidence	MTBF — Gain Product
Transistor Chip	7,398,000	3	141 Years	—
CA2200 Hybrid	984,000	4	13 Years	221dB — Yrs
CA2600 Hybrid	577,000	4	8 Years	264dB — Yrs

Figure 2. Hybrid Circuit Life Test Data

IV. RF TRANSISTOR DESIGN CONSIDERATIONS

The performance which can be obtained from the amplifier is determined, in the end, by the transistor. Not only must the transistor provide performance, however, it must provide this performance for a reasonable length of time. If the transistor fails, then the hybrid fails and cost to the system operator is the result.

When the transistor engineer begins to design a device for use in CATV amplifiers, then, he is faced with two main requirements. The device must offer a certain level of performance and it must do its job reliably. We will now investigate the RF transistor and the considerations that go into its design.

1. Starting Material

Modern transistors are built using what is called the planar technology. This name arises from the fact that all areas of the transistor are found on the planar surface of the silicon wafer. Figure 3 illustrates a cross-section

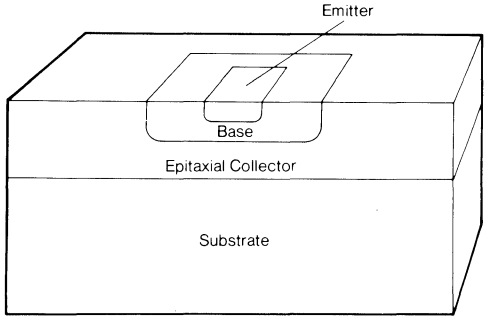


Figure 3. Planar-Epitaxial Technology

of a typical transistor structure as built using the planar technology. The first job of the designer is to decide what starting material he wishes to use for his transistor. The starting material consists of a wafer of silicon, approximately 10 mils thick and typically 2 inches in diameter. This silicon has been grown in crystal form while introducing a large concentration of impurities. This substrate silicon, then, is very heavily 'doped' so that the resistivity is very low. On the surface of this low resistivity silicon wafer is then grown a layer of silicon which is not so heavily doped so that the resistivity of this layer is higher than that of the substrate. It is the configuration of this 'epitaxial layer' that is very important to the performance of the device. It is this layer that will form the collector of the transistor. There are two parameters of the epi layer that can be specified by the engineer. One is the thickness and the other is the resistivity. The resistivity is chosen from operating voltage considerations. The transistor is intended for a specific purpose and presumably the voltage at which it will be operating is known. If the device will be biased at 20 volts in an amplifier, then the collector breakdown voltage of the transistor, BV_{CBO}, should be higher than 20 volts to provide a safety cushion. The phenomenon that occurs in a well-designed transistor at breakdown is called avalanche. This occurs when a sufficiently high reverse voltage is placed across a p-n junction. A field is formed across this junction and carriers are accelerated across the field. When the applied voltage equals the avalanche voltage a multiplication effect occurs in which atomic bonds are broken and the junction breaks down. This is the collector breakdown voltage and it is proportional inversely to the doping level of the collector or epi layer. By specifying epi material, then, the designer sets his voltage operating limit.

The other epi parameter of interest is the thickness of the layer. It has been found that epi thickness is closely tied in to both device reliability and performance. One parameter that is commonly used to describe high-frequency transistors is f_T. This is the gain-bandwidth product of the device or the frequency at which the common-emitter, short circuit current gain, h_{21}, equals unity. A high f_T means to the circuit designer better wide band gain performance. The f_T frequency can be related to the physical device in terms of the various delay times throughout the transistor. If the delay that a carrier sees in traveling through a device is less than in another device, then the f_t for the device with the least delay is higher. The thickness of the epitaxial region is related directly to one of these delay times; namely the $r_{sc}C_{Tc}$ time constant in the collector. The r_{sc} is the collector series resistance and to reduce this value for a given resistivity, we must reduce the epi thickness. There is another advantage to be gained from reducing the epi thickness which relates to distortion performance. Figure 4 shows a comparison of intermodulation distortion performance between two CATV transistors. The transistors are identical in all respects except that one

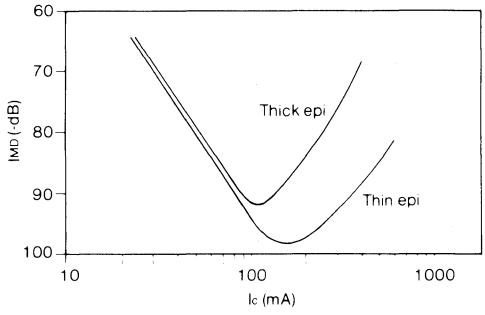


Figure 4. I_{MD} Distortion Performance as a Function of EPI Thickness

device was built on epi material which was 50% thicker than the other. It is seen that the device which was built on thin epi material offers better distortion performance at higher current levels. The reason for this performance gain with thin epi is the fact that the maximum current density available in a device increases as the epi thickness is decreased. This occurs because of debiasing of the collector-base depletion region by the resistive epi region. The thin epi device, then, acts like a larger device at higher currents, resulting in better distortion performance at these higher levels.

Thin epitaxial material appears to yield very good transistors for CATV applications. Unfortunately there is a negative side to the story. The fact is that as the epi material is made thinner and thinner to achieve good performance the transistor becomes more and more sensitive to voltage variations. With thin epi the ballasting effect of the collector resistor is lost and the transistor loses ruggedness. The designer, then, wants to choose an epitaxial material which is as thin as possible for performance yet which is thick enough to avoid complete depletion and provide some collector ballasting.

2. Vertical Geometry

Once the starting material is decided upon, then it must be insured that a process is available which will yield a high performance vertical geometry. The importance of high f_T in the CATV transistor has been discussed. Another time constant which can be reduced in order to increase f_T is the delay due to carrier movement through the base region. The relationship for this delay is

$$t_b = \frac{W_b^2}{2.43\, D_{eb}\, n\, (N_B{}' / N_{BC})}$$

This relationship describes the time required for carrier transit across the base region in terms of base width, W_b; diffusion co-efficient, D_{eb}; and doping gradient, $N_B{}'$ and N_{BC}. The point here is that this delay time varies directly as the square of the base width. A desirable goal then is to produce a transistor which has a narrow base width. The well understood diffusion process can be used to control this parameter to a point. However, as narrower base widths are sought, device yields go down due to non-uniformities which are inherent in the diffusion process. State-of-the-art base widths with good uniformity are possible, though, by taking advantage of ion implant technology for the formation of the device junctions. Another advantage of implantation is that it makes possible steeper gradients in the emitter and base regions resulting in higher fields and shorter transit times in those areas.

3. Horizontal Geometry

One more item must be considered before the CATV transistor is ready to be built. A mask set must be designed, or, in other words, it must be determined what the device will look like, physically.

First, the basic device configuration must be decided upon. There are three transistor contact geometries in use; these are interdigitated, overlay, and mesh. The overlay and mesh configurations are used primarily for modern power transistors. High frequency devices are sensitive to parasitic capacitances and this favors the interdigitated design.

Figure 5 is a representation of typical transistor configurations. The base area is dictated by the power

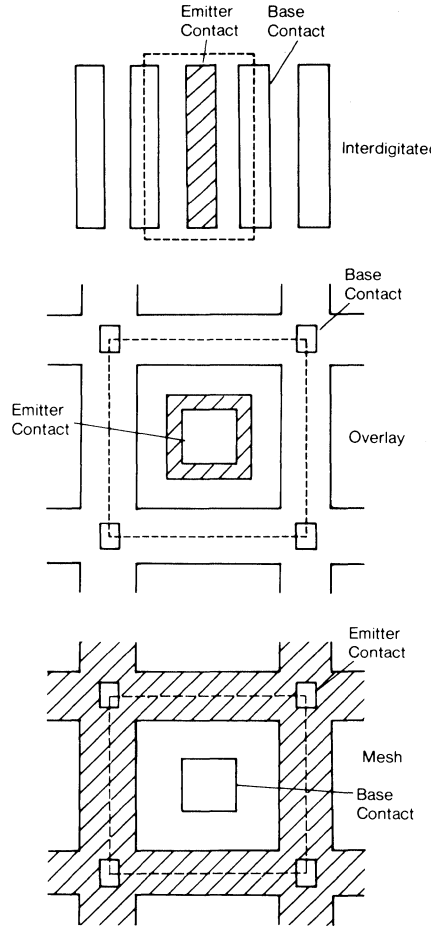
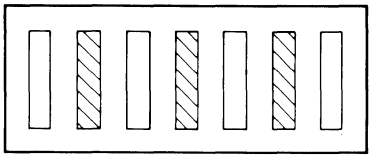


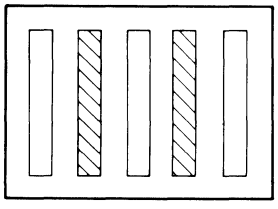
Figure 5. Typical Transistor Configurations

handling requirements of the transistor. There must be enough area available to dissipate the heat which is generated. The amount of current to be handled by the device will determine what the minimum emitter periphery is. This is because at higher bias levels and frequencies a large transverse voltage drop occurs in the active base region under the emitter. This will have a de-biasing effect on the central portion of the emitter-base junction causing most of the current to pass at the emitter edges. Since it is known how much current the

device will be required to handle, it is possible to calculate the amount of emitter periphery necessary to safely handle this current. The task now is to pack this amount of emitter periphery into the smallest base area possible, thereby reducing collector-base junction capacitance. Two examples of possible interdigitated designs having equal emitter peripheries are shown in Figure 6. It is seen



$E_P = 24$
$B_A = 90$
$E_P/B_A = .26$



$E_P = 24$
$B_A = 88$
$E_P/B_A = .27$

Figure 6. E_P/B_A Comparison for Square vs Rectangular Base Configuration

that slightly higher E_P/B_A ratios are possible with a design which is square compared to one with a higher aspect ratio. The problem with the square configuration is that the long emitter fingers required will result in considerable voltage drop along their length. The result is that part of the device is not being used and hot spots will develop. Not only will device performance be reduced, but it will soon fail because of overheating. The design with the higher aspect-ratio is desirable since the voltage drop problem is eliminated. Another advantage of this configuration is that it is inherently better able to dissipate heat since the cells are not so closely coupled as in the square configuration. This design also has a problem, however. Although the emitter fingers are now short enough, the active area of the device is now quite long. The middle portion of the device will tend to draw more current which is not efficient. The solution to this problem is to add ballast resistors between the emitter feeder arm and the emitter fingers. (See Figure 7.) The ballast resistors are thus in series with the emitter contact metallization. If an emitter-base junction site begins pulling more than its share of current the series resistance will cause a proportionate drop in the input voltage for that site, thus limiting the current and preventing failure. An important point is the type of ballast resistor used. Two types of resistor are popular, thin film or diffused. Thin film resistors are susceptible to microcracking and they also are faced with a high

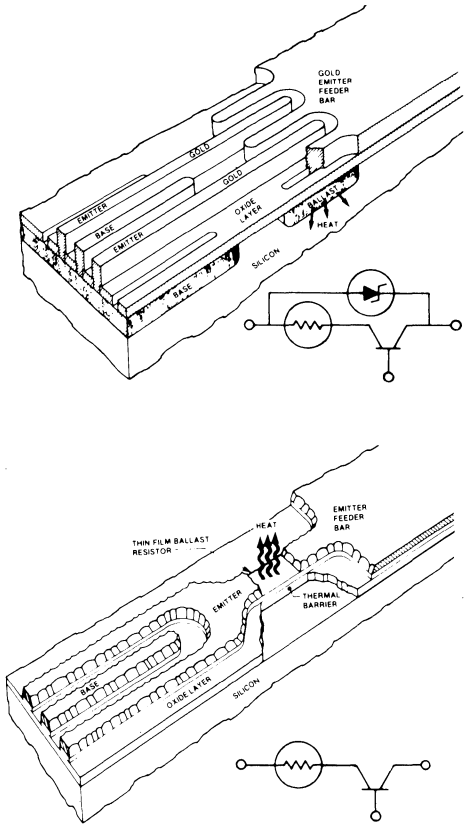


Figure 7. Ballast Resistor Configurations

thermal barrier since they sit on top of the silicon dioxide barrier. Diffused resistors are more reliable since they avoid the oxide barrier and are not susceptible to cracking.

It is also desirable to reduce the contact spacing and the emitter contact widths of the transistor for two important reasons.[1] A narrow contact spacing will allow more emitter periphery to be placed within a given base area. This is good since we have seen that gain performance depends directly on the amount of periphery available for current handling. A narrow emitter stripe is desirable since the resistance of the base region, r_b', varies directly as the emitter contact width and it is necessary to reduce the parasitic r_b' as much as possible for gain purposes. Incidentally, reduction of r_b' is good for noise figure too. Figure 8 illustrates the impact of emitter width on base resistance.

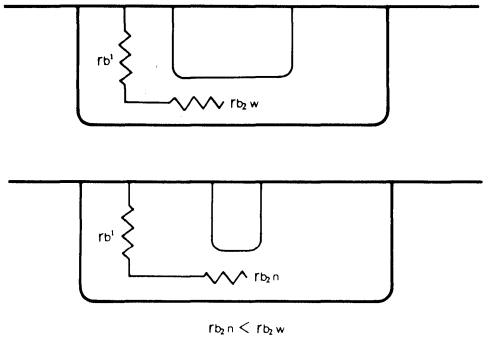


Figure 8. Effect of Emitter Stripe Width on Base Resistance

The last step in the construction of the transistor is the deposition of metallization so that contact can be made to the emitter and base regions. (See Figure 9.) The type

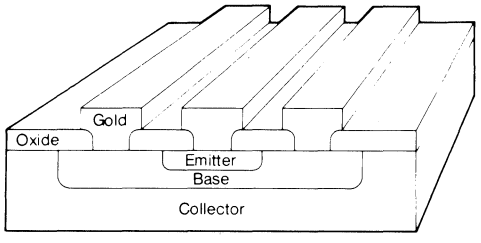


Figure 9. Transistor Metallization

of metal to be used is an important decision. The two metals that are low enough in conductivity that can be used for transistor metallization are gold and aluminum. Aluminum metallization has been used for years as a conductor for transistors. Its advantages are that it is a well-understood process, it offers a good silicon contact without any barrier metallization, and it is inexpensive. However, considering the micron contact geometry of the RF transistor and the fact that it will be mounted on a gold hybrid circuit, then the decision is considerably easier to make. For a CATV transistor, gold provides the following advantages over aluminum.[4]

1. Monometallic wire bonding system.
2. Electromigration resistance.
3. Low contact resistance with elimination of shorts due to silicon-metal alloying.
4. Corrosion resistance.
5. Oxide step coverage.

Allows use of tighter contact geometries.

Monometallic Wire Bonding System

As has been described, it is desirable to have an all-gold metal system for reasons of reliability. A monometallic system eliminates the formation of gold-aluminum intermetallics and the wire bond failures that result. Figure 10 illustrates life test data that shows an increased failure rate due to bond failures in the aluminum-gold system.

Life Test at 95°C Case Temperature

Part Description	Unit Hours Accumulated	Wire Bond Failure No's	Wire Bond Failure Rate %
601B, 200 Hybrids With Aluminum 3070 Die	1,162,000	24	4.1
2200, 2600 Hybrids With Gold 3040 Die	1,188,000	0	0

Figure 10. Wire Bond Failure Rates in Aluminum/Gold Life Test

Electromigration Resistance

It was shown earlier that it was desirable to achieve a high E_D/B_A ratio so as to obtain maximum performance from a device. This was achieved by placing the transistor contacts as close together as possible. The use of such tight contact geometry forces the use of very narrow metal fingers. The resulting high current densities can lead to reliability problems as a result of electromigration. Electromigration is a phenomenon which occurs in metal films as a function of time, temperature, and current density. For any given temperature, a certain equilibrium concentration of vacancies exists in all metal films. Self diffusion of metal ions throughout the film arise due to the metal ions being thermally activated into adjacent vacancies. In the absence of any external forces, the metal ion diffusion will be isotropic and will result in no net accumulation or depletion of mass in any given site. In the presence of an electric field, however, the metal ions experience a force due to their charge, inducing an ionic flux toward the cathode end of the film. In addition, the conduction flow of electrons in the metal due to the electric field will cause electron scattering off the activated ions and impart momentum to them inducing an ionic flux toward the anodic end of the film. In good conductors, the momentum exchange force dominates the electrostatic force and results in a net mass transport toward the anodic end of the film. The result is an open circuit in the metallization strip. This void formation is accelerated by high temperatures and current density.[6]

Aluminum has exhibited a high susceptibility to electromigration for current densities above 10^6 A/cm^2. Such a current density is easily realized in state-of-the-art RF devices. For a given device geometry there are only two alternatives to allow reduction of the current density in a device. Either the operating level can be reduced or a metal can be selected which has a higher mass and activation energy. The operating level cannot be reduced without a sacrifice in performance. We can still keep high performance and reduce the current density by using gold metallization. At 200°C, experiments conducted on identical transistors with gold vs. aluminum metallization showed an improvement in mean life time of two orders of magnitude using gold.

Contact Resistance

Gold cannot be used as a single layer metallization because of its relatively low silicon eutectic temperature and its poor adhesion to silicon and silicon dioxide. A barrier layer must be employed to prevent gold diffusion into the silicon and this barrier metal must offer good adhesion to silicon, silicon dioxide, and gold. Such a barrier is offered by a system utilizing platinum silicide, titanium and tungsten. The platinum silicide forms a good ohmic contact with the silicon; the Ti/W provides the necessary diffusion barrier and offers good adhesion to SiO_2 and silicon.

Aluminum has historically offered good ohmic contact without the need for barrier metals. In RF devices, however, at current densities well below electromigration densities, a problem of formation of silicon/aluminum alloy is ever present resulting in emitter-base shorts. Any hot spot formation will result in an increased alloying rate and early failure.

Corrosion Resistance

Under biased conditions, in a humid atmosphere, gold has demonstrated a lifetime more than 3 times that of aluminum. The failure mode in aluminum is electromechanical corrosion and gold is insensitive to this phenomenon.

Step Coverage

Gold offers tremendous improvements over aluminum in its ability to cover oxide steps without decrease in metal thickness or cracking. (See Figure 11.) Aluminum is deposited by means of evaporation in a vacuum where the mean free path of the aluminum particle is long. This means that equal coverage of all surfaces is impossible even if the target is rotated during evaporation. The plate-up gold system reduces step coverage problems to insignificance.

Narrow Contact Geometries

The RF transistor must have very fine horizontal geometry to achieve the performance required in a CATV system. With aluminum metallization these narrow finger widths are achieved by etching the aluminum to remove it. Such a process, if done very carefully, will at best result in fingers of uneven width which are susceptible to high current densities and the associated reliability problems. The gold system is capable of providing microwave geometries with insignificant variations in line widths. In fact, the geometry on present gold CATV devices is narrower than some low-noise microwave devices which are on the market today.

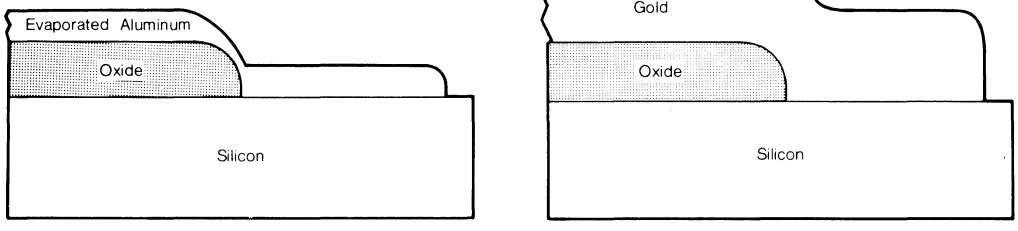


Figure 11. Oxide Step Coverage

V. SUMMARY

1. The CATV system operator is interested in performance with reliability in the amplifier equipment he uses.
2. The basic building block of the CATV amplifier is the hybrid circuit. The hybrid amplifier offers reliability advantages over discrete designs including gold circuit metallization and a reduced number of interconnects.
3. The heart of the hybrid circuit is the RF transistor.
4. The design of a reliable transistor for use in CATV amplifiers requires a knowledge of basic design values plus the availability of state-of-the-art processing. Points to be considered include:
   - starting material
   - vertical geometry
   - horizontal geometry
   - configuration
   - metallization.
5. Life tests show the improvements in reliability to be gained by careful transistor design.

APPENDIX

Derivation of reliability expression for chance failures:

$$R(t) = e^{-\lambda t}$$

If an original population of X_o items is continuously decaying so that there are X items at time t, the change of population in one interval dt is $dX \cdot dt$. Divided by the total population X at t, this gives the negative rate at which the population changes at time t.

$$-\lambda = \frac{dX \cdot dt}{X} = \frac{dX}{X} \cdot \frac{1}{dt}$$

then, $$-\lambda dt = dX \cdot X$$

Integrating over the time period being considered.

$$-\int_0^t \lambda dt = \ell n X \cdot C = \ell n X - \ell n C$$

for $t = O$, $X = X_o$

Then $C = X_o$

$$\text{And } X \cdot X_o = e^{-\int_0^t \lambda dt}$$

If the rate of decay, λ, is constant, then

$$X \cdot X_o = e^{-\lambda t}$$

Since $X \cdot X_o$ is probability of survival for a decaying population then

$$R(t) = X \cdot X_o = e^{-\lambda t}$$

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5. Igor Bazousky. *Reliability Theory and Practice*. Prentice-Hall, 1961.
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35/50 Watt Broadband (160–240 MHz) Push-Pull TV Amplifier Band III

This note describes the performance of a broadband ultra linear push pull amplifier designed for service in band III TV transposers and transmitters.

Devices used : two TPV 375.

Basic amplifier specifications :

IMD (1) = — 51 dB	at	P_o = 35 W	P_{gain} = 10 dB
IMD (1) = — 48 dB	at	P_o = 50 W	input VSWR : < 1.6
V_{ce} = 28 volts ;	Total = 4.4 A		output VSWR : < 1.5

(1) vision carrier — 8 dB, sound carrier — 7 dB, sideband signal — 16 dB.

General design Consideration

The principal aims were :

— employ a relatively simple solution permitting us to obtain the optimal performances from TWO TPV 375.

— simplify the design and reduce the cost.

The main consideration was to obtain the maximum output power with the best IMD over the band. To obtain this requirement the output match and losses must be the best possible in all the band.

The second consideration was to obtain the maximum gain by reducing the input matching circuit losses to a minimum.

These factors led us to choose matching circuits using quarter-wavelength transformers at the input and output which permit us to :

— reduce the load and source impedances to low values with low losses

— couple two transistors in a push pull configuration.

Because the output and input transistor impedances are in series, due to the push-pull configuration, the required transformation ratio is one half of that required for a single ended stage.

The first approach for the circuit calculation was made from the input and output impedances given in the TPV375 data sheet and matched to the proper impedance levels using a Smith Chart. The element values were then optimized with the aid of «COMPACT» program.

Amplifier Design

The basic block diagram for the amplifier is shown in Figure 1 and the circuit schematic is shown in Figure 2.

The input and output circuits are each composed of two networks : a quarter-wavelength transformer-balun and a matching network.

The quarter-wavelength transformer impedances have been chosen to be easily built using microstrip technology.

Input circuit

The input circuit is shown in Figure 3 and the input impedances are shown in Smith Chart 1.

The low transistor input impedances are transformed into higher impedances near the real axis by Capacitors FF.

The (EE, DD) series elements and (CC, BB) parallel elements collapse the amplifier input impedances around 8,5 Ω.

Since the devices can be considered in series at this point the impedance is doubled to 17 Ω. The quarter-wavelength transformer balun (AA) completes the match to 50 Ω.

The transformation ratio is 2.8 : 1.

The maximum theoritical input VSWR is 1.80 : 1 and the maximum experimental VSWR is 1.60 : 1.

Output circuit

The output circuit is shown in Figure 4 and the output impedances on Smith Chart. II. Since the output impedances are higher than the input impedances, the output matching network is simpler and the quarter-wavelength transformer ratio is lower.

The inductors aid the matching but primarily provide for good stability at the low frequencies, and are used for collector bias. The output quarter-wave-length transformer ratio is 1.6 : 1.

The maximum theoretical VSWR is 1.16:1 and the maximum experimental VSWR is 1.44:1.

Amplifier Performances

— IMD versus output power : Figure 5
— Input and output return loss and VSWR = Figure 6
— Gain versus frequency : see Figure 7
— 1 dB gain point compression : 70 W
— Bias conditions : V_{ce} = 28 V ; Total = 4.4 A.

Technology and layout considerations

The epoxy-Glass 1/16 inch (ε_r = 4.1) is used as board material except for the input and ouput transformers.

The glass - Teflon 1/50 inch (ε_r = 2.55) is used for the transformers (see the details Figure 8).

We have considered for a microstrip line that after W (Width) from the conductor strip edge the fields are negligible and we can size the ground conductor to be 3 W without perturbing the propagation. This kind of transformer has the following characteristics :

— We can have any impedance values within realizable min-max limits.
— The vertical dimensions are small and the mechanical realibility is good.
— Good repeatibility.

The bias circuits are included with RF circuits in order to give a compact amplifier : Figures 10 and 11 show the layouts and the Figure 12 the physical layout of the push-pull amplifier.

Combined pairs of push-pull Amplifiers

— In general several push-pull amplifiers are used for the final stage of the TV transmitter amplifiers.

They can be combined by pair with quadrature combiners (see block diagram Figure 9).

The advantage of using this kind of coupler is that the input and output VSWR become good (> 20 dB rtn. loss) in comparison with the relatively high original VSWR of the push-pull amplifier.

General Conclusions

— Pushpull techniques simplify the required circuitry and associated losses.
— The problems associated with 3 dB hybrids in cascade — insertion loss and imbalance — when four devices in parallel are required are minimized.
— With additional effort both the input and output VSWR could be improved to 1.2 : 1.
— Good repeatability in production without variable components being required.

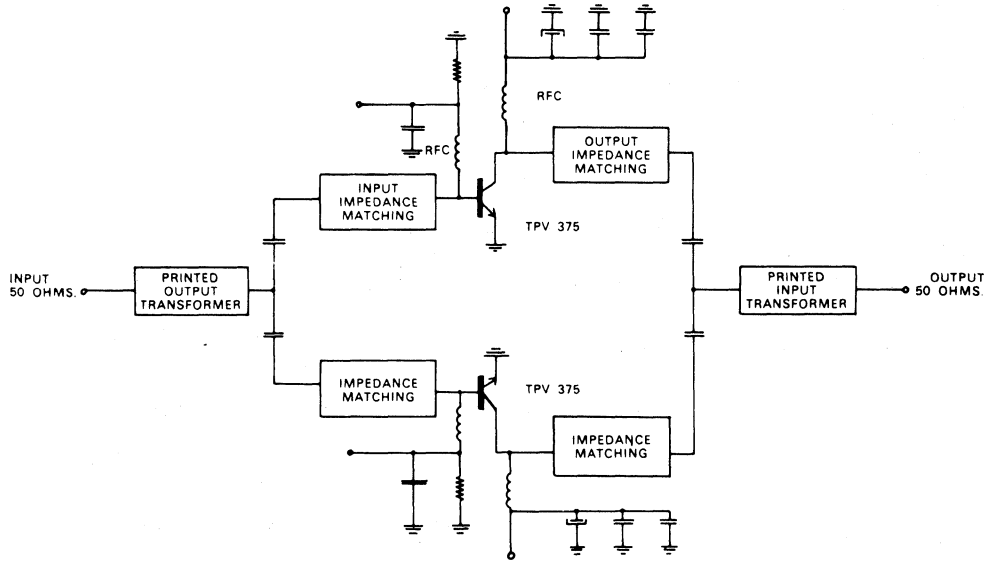


Figure 1. Push-Pull Circuit

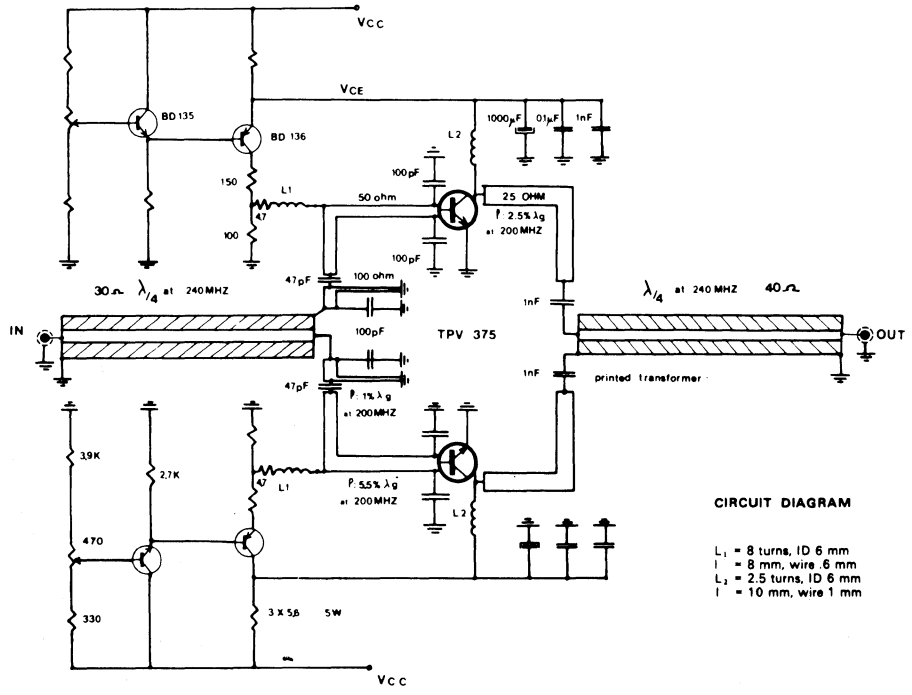
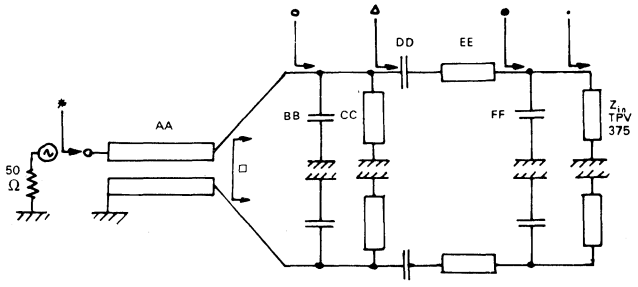


Figure 2. Circuit Diagram

On the smith chart the impedances are represented by :



	AA		BB	CC		DD	EE		FF
	Z_0 (Ω)	L* (mm)	(pF)	Z_0 (Ω)	L* (mm)	(pF)	Z_0 (Ω)	L* (mm)	(pF)
Calc. value	30	313	139	100	11.3	47	50	80.8	238
Empirical value	30	313	100	100	15.0	47	50	82.5	200

* L is given for $\varepsilon_r = 1$

Figure 3. Input Circuit

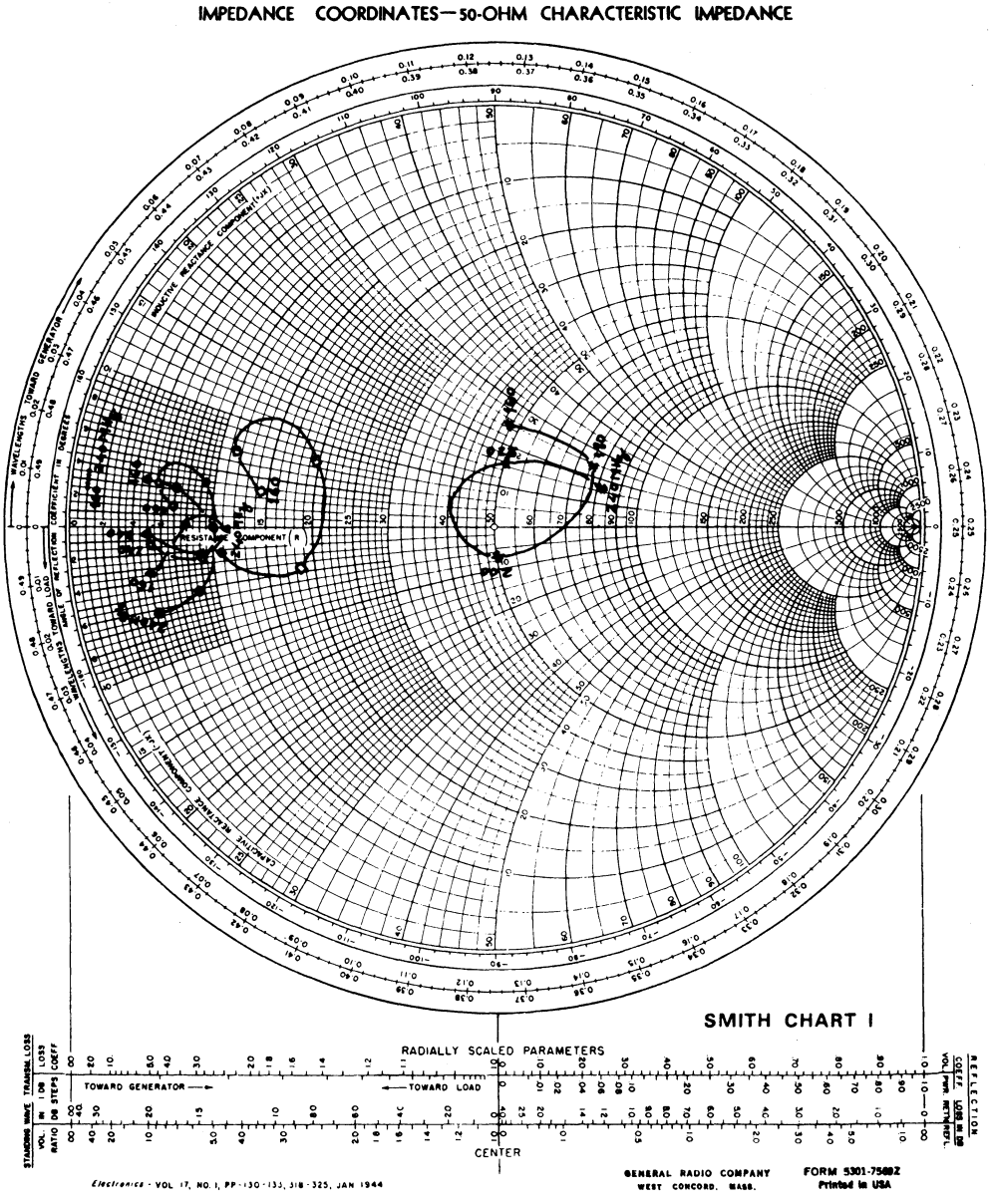


Figure 4A. Input Circuit

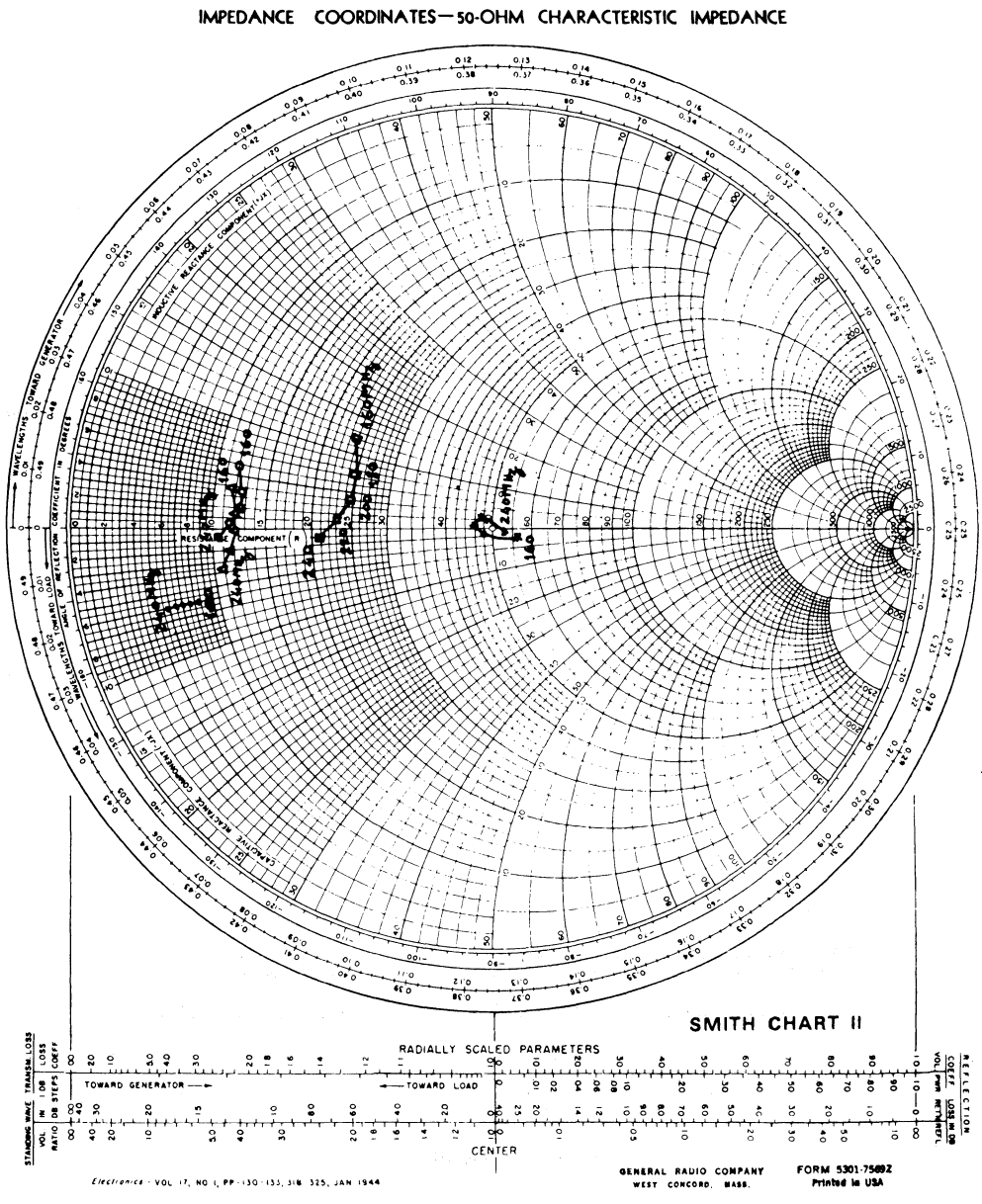


Figure 4B. Output Circuit

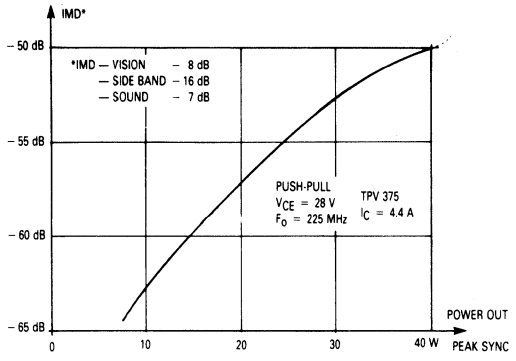


Figure 5. IMD versus Output Power

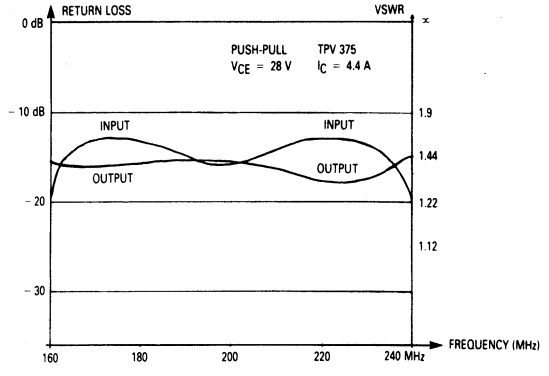


Figure 6. Input and Output Return Loss versus Frequency

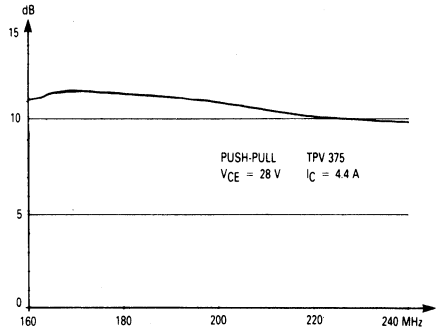
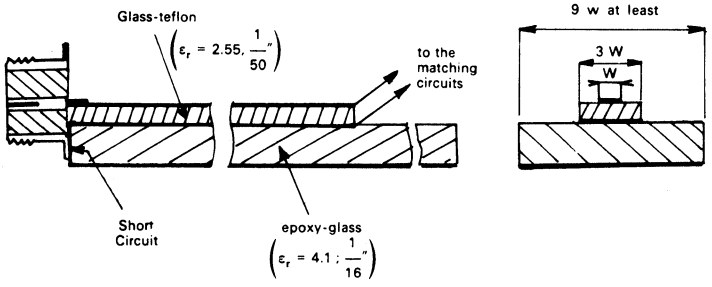
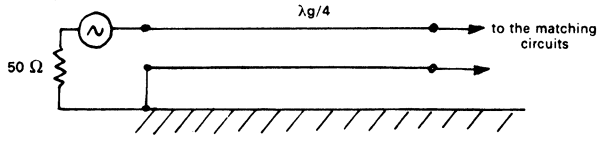


Figure 7. Low Level Gain versus Frequency



a.) Quater Wavelength Balun



b.) Equivalent Circuit

Figure 8.

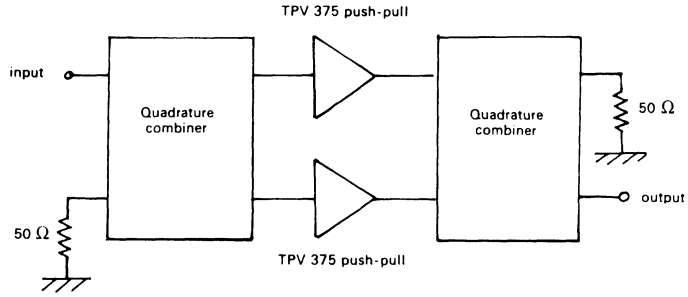
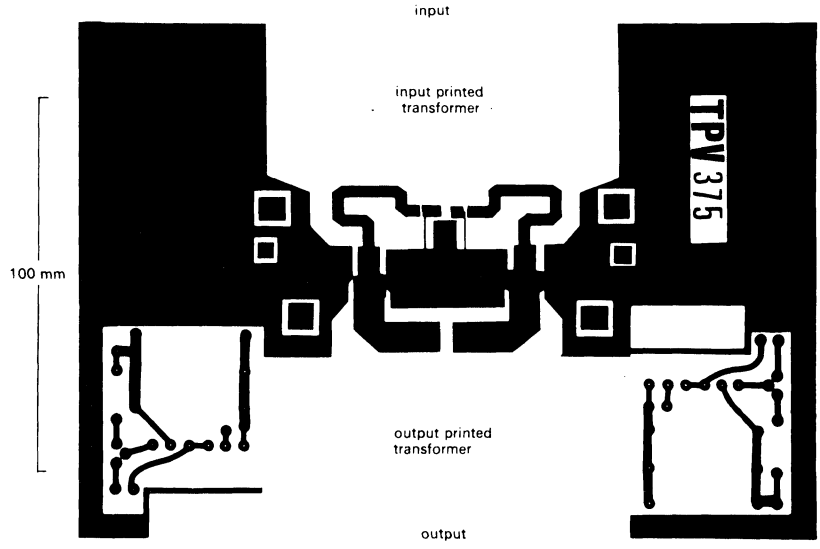
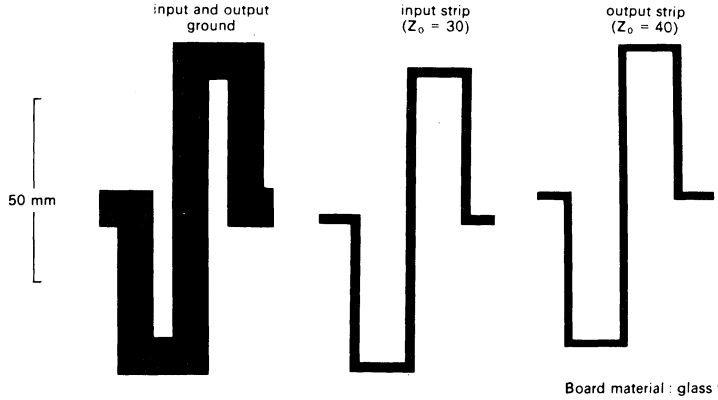


Figure 9. Combined Pair of Push-Pull Amplifiers



Board material : epoxy-glass ; 1/16 inch ; ε_r = 4.1

Figure 10. PC Board Layout (Not to Scale)



Board material : glass teflon ; 1/50 inch ; ε_r = 2.55

Figure 11. PC Board Layout for Input and Output Quater-Wavelength Transformer (Not to Scale)

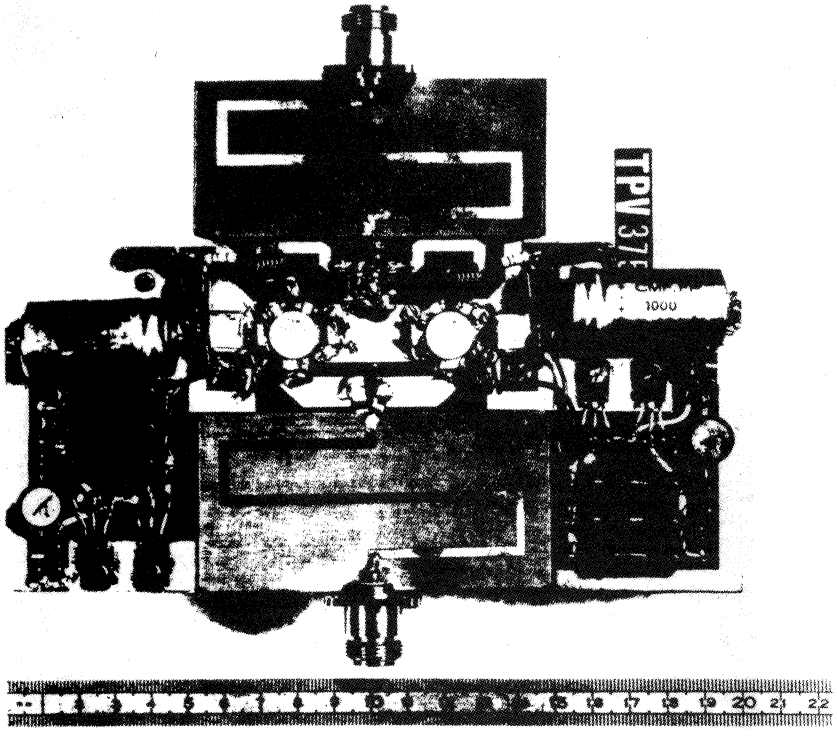
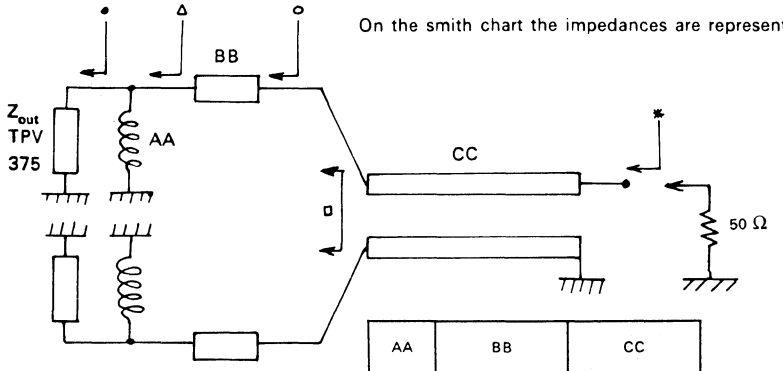


Figure 12. 160–240 MHz Amplifier



On the smith chart the impedances are represented by :

	AA	BB		CC	
	(nH)	Z_o (Ω)	L* (mm)	Z_o (Ω)	L* (mm)
Calc. value	11.7	21.6	37.5	33	312.5
Empirical value	53.1	25.0	37.5	40	312.5

* L is given for $\varepsilon_r = 1$

Figure 13. Output Circuit

AN1029

TV Transposers Band IV and V P_O = 0.5 W/1.0 W

This note describes the performance of a broadband (470-860 MHz) ultra linear amplifier designed for service in band IV and V T V transposers.
Device used :

TPV 596.

Basic specs :

I.M.D. — 60 dB max. at Po = 0.5 watts
Vce = 20 volts ; Ic = 200 mA
Pgain = 11.5 dB min.

The approach used is intended to be straight forward and inexpensive as follows.

1) The load line be defined to provide the correct match for peak power (P. sync).
2) The VSWR at the collector be less than 2 : 1.
3) The input match be designed to provide flat gain with decreasing frequency.
4) Use computer aided design.
5) Use a three tone norm

   Pvision = — 8 dB
   Psound = — 7 dB
   Psideband = — 16 dB

6) Circuit realization to be a distributed design built upon teflon glass copper clad circuit boards. However the design will be analized using Er = 1.0.

The input and output impedances were taken from the TPV596 data sheet and plotted on a smith chart. First consider the input. To have flat gain with an optimum collector load, the basic physics of a class «A» biased device defines a gain slope of −6 dB/octave which must be compensated for. The band of interest is 470–860 MHz which is .915 octaves which implies that 5.25 dB of gain must be compensated for if the device is perfectly matched at 860 MHz. This means that a transmission less of 5.25 dB or a VSWR for 11.0:1 must be employed at 470 MHz. The input Z is converted to Y on Smith Chart (I). The point at 860 MHz will intersect the constant conductance line equal to 1.0 (20 m℧) if it is rotated 0.14 λ using a 20 m℧ (50 Ω) transmission line. After this rotation a capacitive stub or chip capacitor is used to resonate the susceptance at 860 MHz; A capacitive stub or a chip capacitor equal to 16.7 pF can be used, and the result is shown on Smith chart (I). It is interesting to note that the VSWR vs frequency can be adjusted for gain flatness by selecting an optimum Z_O for the capacitive stub. It is also obvious that the locus of impedances at the circuit input can vary between the locus of points defined by using a chip capacitor, and the imaginary axis by using a stub with $Z_O = \infty$. Graph (II) is a plot of these results. Because infinite isolation doesn't exist between the output and input of any transistor, and because the required network is very simple, the input circuit will be optimized empirically. A computed aided circuit will be defined for the output only. It is also indicated that a combination chip capacitor and stub may provide the best results.

The output circuit considerations were first determined using a Smith Chart approach. It must be clearly understood that computer optimization is only as good as the circuit configuration and associated computer instructions.

The approach follows :

Smith Chart (II)

1) The device output impedances are first converted to admittances and plotted as the conjugate (Y load).
2) In order to allow easy collector lead soldering a Zo = 50 Ω, 3 mm long transmission line is used. Since the Smith chart is normalized to 20 m℧ (50 Ω) we can rotate toward the load directly as the chart is configured.
3) Since the balance of the circuit used Yo = 10 m℧ (100 Ω) we next normalize the chart to 10 m℧. 100 Ω transmission line was chosen as a good compromise between physical length requirements and ease of realization on Teflon Glass.

4) The next element, a shorted shunt transmission line less than $\lambda/4$ in length reduces the imaginary part by moving each point of admittance along a line of constant conductance. The length was chosen to locate the lowest frequency point (400 MHz) near the real axis so that the locus of points would be more equally distributed about a 2.0 : 1 VSWR circle.

5) The resultant locus of points are then rotated with a 10 m℧ (100 Ω) transmission line to a degree which locates the admittance point of 860 MHz near the line of constant conductance equal to 2.0 on Smith Chart (II). This conductance is exactly equal to 20 m℧ since the chart is normalized to 10 m℧.

6) The final step is to use a parallel resonant circuit which will reduce the imaginary pacts at both the upper and lower frequencies.

The following approach was used to calculate the element values for the antiresonant circuit.

By observation of the smith chart it was decided to place the 460 and 860 MHz points on or just inside the 2.0 : 1 VSWR circle.

It then follows that

$$\text{at } f_1 = 460 \text{ MHz} \qquad W_1 C - \frac{1}{W_1 L} = -0.4$$

$$\text{at } f_2 = 860 \text{ MHz} \qquad W_2 C - \frac{1}{W_2 L} = 1{,}7$$

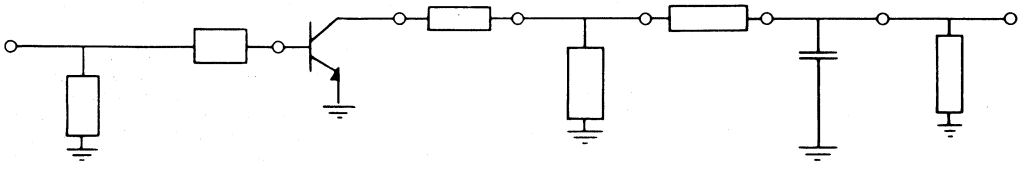
The 2 equations with 2 unknows are solved with the following result.

L = 0,189 nHy
C = 496.11 pFd

since we are normalized to 10 m℧

Lactual = 0.189/.01 nH = 18.9 nHy
Cactual = 496.11 × 0.1 pF = 4.96 pFd

7) The result is normalized to 20 m℧ with the final result shown.



Zo	10 Ω	50 Ω	TPV 596	50 Ω	100 Ω	100 Ω		100 Ω
Calc. Value	45.7 mm	3.78 mm		3 mm	76.1 mm	29,3 mm	4.9 pF	50.4 mm
Empirical Value	8.5 48.8 mm	1.5 mm	Opti-mized Value	3 mm	98.8 mm	39.62	5.5 pF	61.6 mm

Graph (III) shows the various VSWR calculated compared to the theoretical best curve and the actual VSWR measured.

Graph (IV) shows the collector load VSWR for the calculated, optimized, and actual result.

Graph (V) is a plot of the single ended amplifier results taken with a network analyzer. No component losses were considered for the theoretical and optimized analysis. The final circuit was also optimized empirically from 470–860 MHz using a network analyzer.

The following results are a summary of performance, bias conditions circuit configuration and recommended hybrid adaptation.

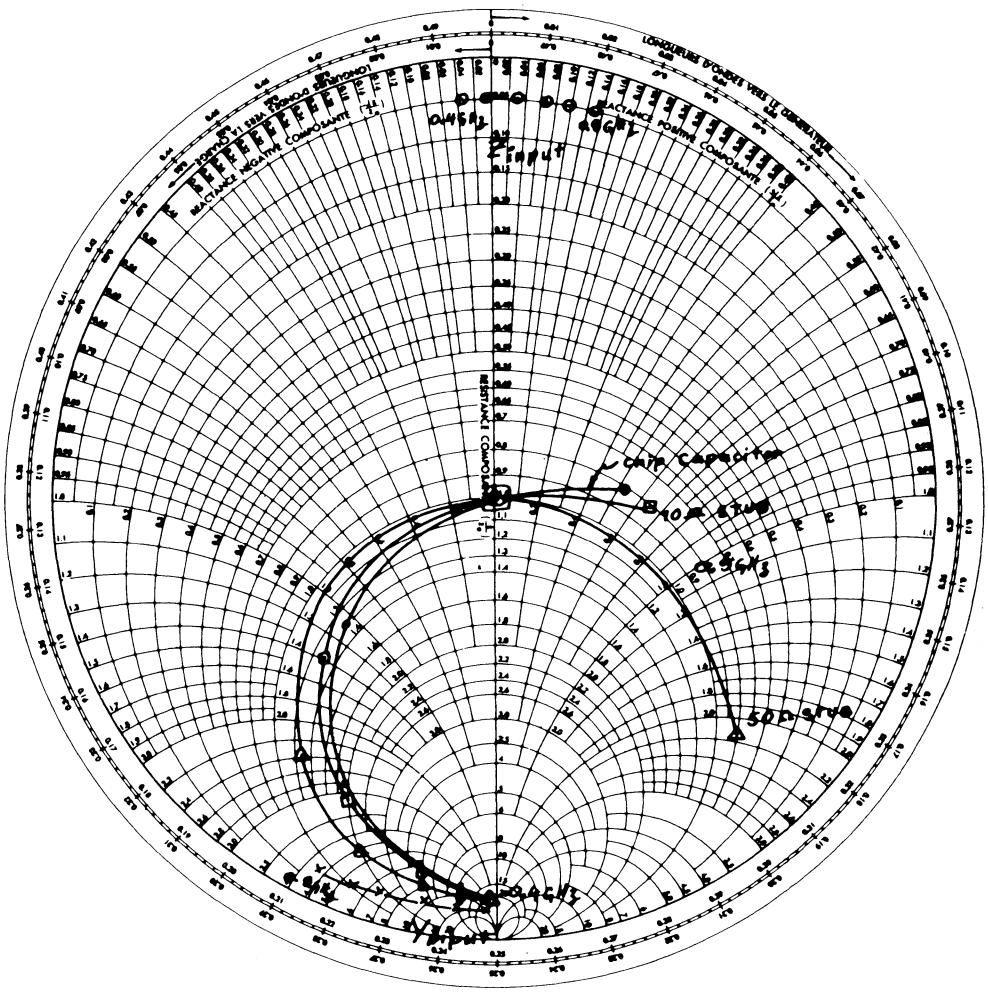


Figure 1. Smith Chart (I)

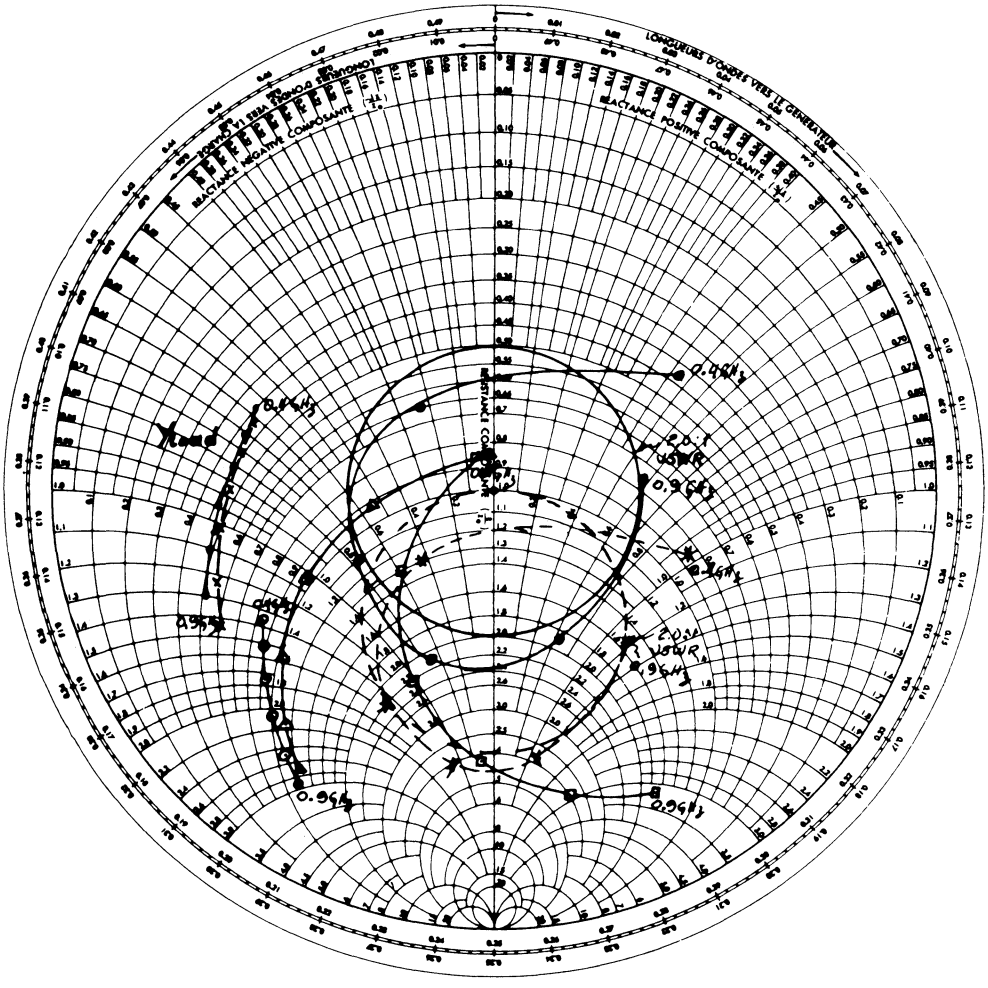


Figure 2. Smith Chart (II)

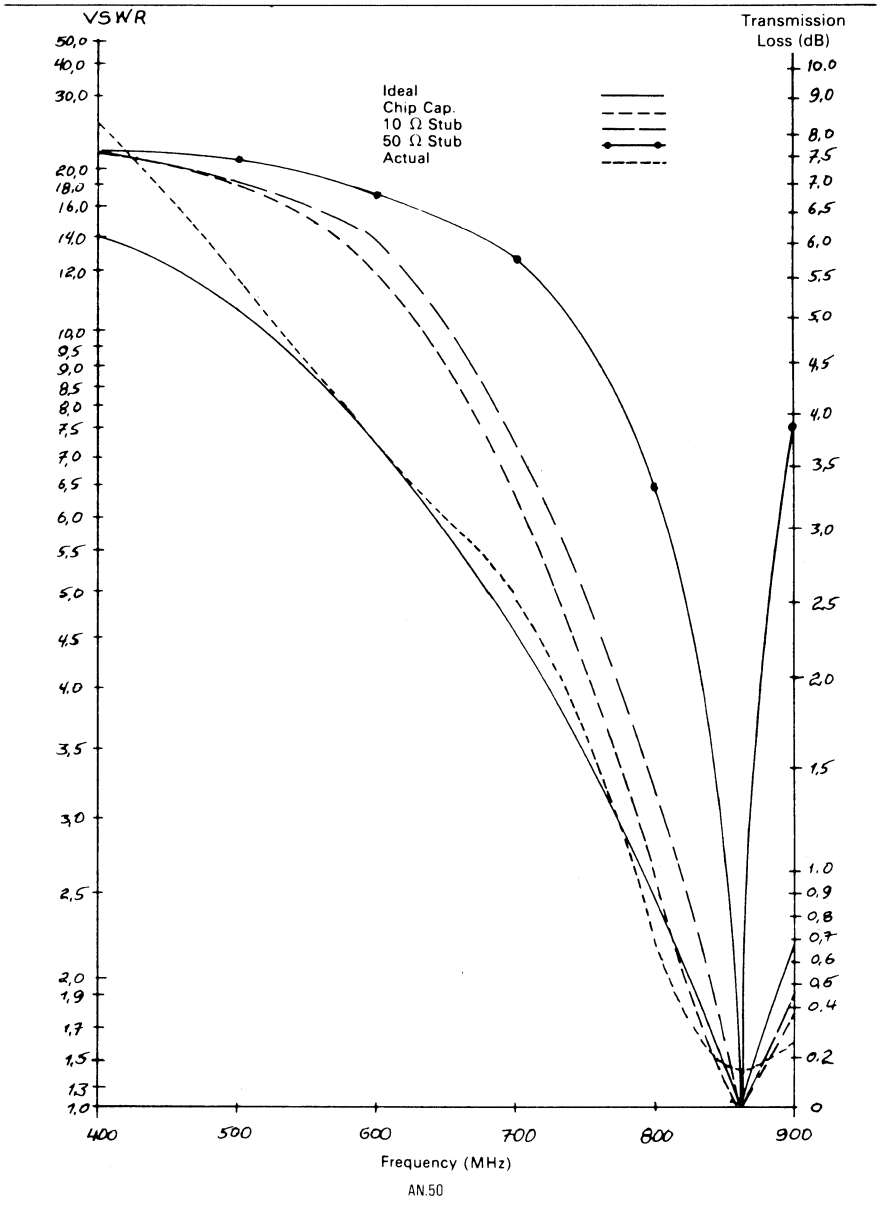


Figure 3. Graph III — VSWR versus Frequency

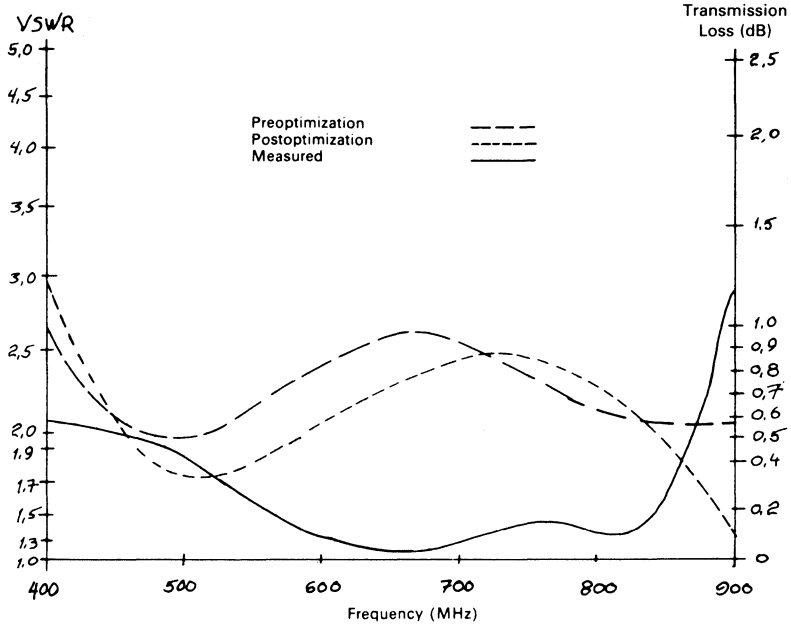


Figure 4. Graph IV — VSWR versus Frequency

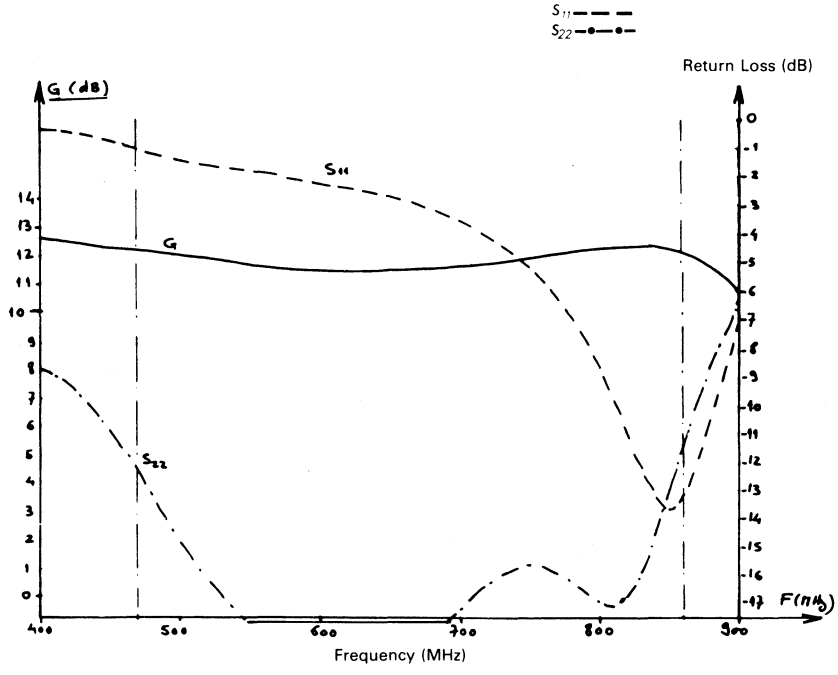
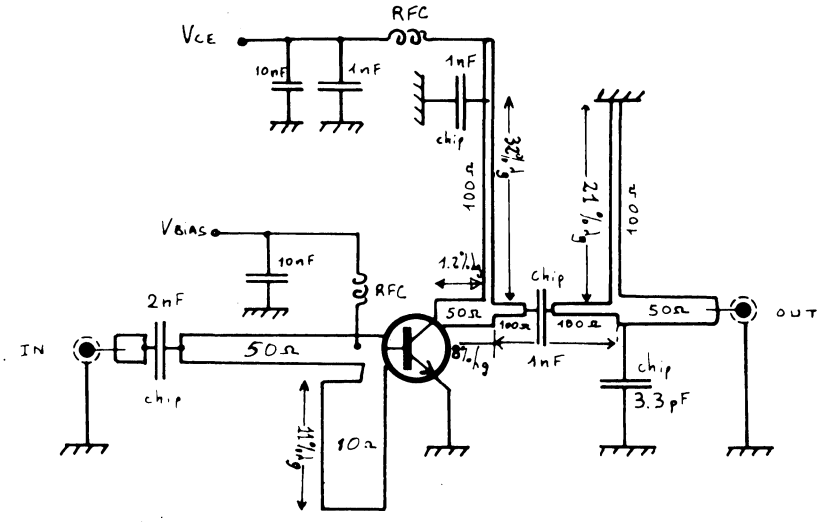


Figure 5. Graph V — TPV596 Amplifier Performance versus Frequency



Class A
V_{CE} = 20 V — I_C = 220 mA
f_o = 860 MHz — WAVELENGTH (λg) at 860 MHz
(material: Glass teflon ϵ_r = 2.55 — 1/16")
Transistor — TPV596

Figure 6. Circuit Diagram for 470–860 MHz Amplifier

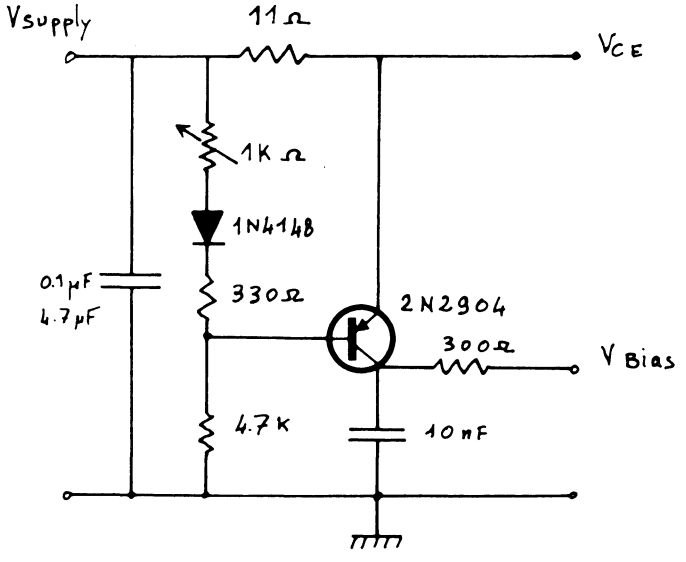


Figure 7. Class A Bias Circuit

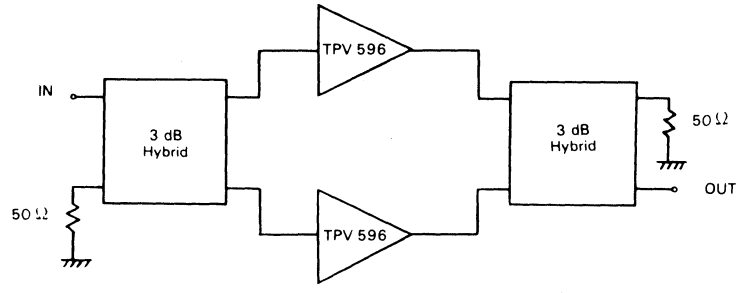
TPV 596 BROADBAND AMPLIFIER

FREQUENCY RANGE	: 470 MHz-860 MHz
POWER OUTPUT AT	: — 60 dB IMD* $\geqslant$ 0.5 W
POWER GAIN	: 11.5 $\leqslant$ G $\leqslant$ 12.7 dB
INPUT RETURN LOSS*	: < — 1 dB
OUTPUT RETURN LOSS	: < — 11 dB
VOLTAGE SUPPLY	: ~ 23 V (V_{CE} = 20 V)
TOTAL CURRENT	: 220 mA

*IMD : Vision : — 8 dB ; Sound carried : — 7 dB ; Side band : — 16 dB

RECOMMENDED CONFIGURATION

*INPUT RETURN LOSS : This amplifier must be used by two connected together with two 3 dB quadrature hybrids to have a balance amplifier with a good input VSWR.



*3 dB - 90° Hybrid coupler from

— ANAREN 10 264-3
— SAGE wireline 3 dB Hybrid 4450 900

IMD VS OUTPUT FOR A SINGLE STAGE
VCE = 20 V-220 mA

F = 860 MHz ; Vision = — 8 dB ; Sound Carrier = — 7 dB ; Sideband = — 16 dB

Pout (W)	0.25 W	0.5 W	1 W
IMD (dB)	— 67 dB	— 61 dB	— 55 dB

F = 860 MHz ; IMD DIN 45004/B
RL = 75 ohms

1.5 V/75 ohms IMD = — 66 dB
2 V/75 ohms IMD = — 60 dB

AN1030

1 W/2 W Broadband TV Amplifier Band IV and V

This note describes the performance of a broadband (470-860 MHz) ultra linear amplifier designed for service in band IV and V TV transposers.

Device used : TPV 597

Basic specifications

IMD (1) = — 60 dB at P_0 = 1 W
V_{ce} = 20 V ; I_e = 440 mA
P_{gain} = 11.5 dB.

(1) Vision carrier — 8 dB, sound carrier — 7 dB, sideband signal — 16 dB.

General design considerations

In general to obtain a flat gain for broadband amplifiers which use transistors with about — 6 dB power gain variation per octave we can use two techniques :

— feedback technique (eg emitter resistor and a negative feedback with a selective circuit between the collector and the base),

— or reflect the input or the output power selectivly to have an insertion loss of 6 dB per octave with 0 dB for the highest frequency.
(There is also another technique which uses a selective attenuator).

With the feedback technique we can have a good input and output match. With the second technique we need to reflect the input power and have a good output match in order to obtain a good IMD. It means the input VSWR is very high for the low frequencies.

The second solution is simpler than the first and if we use two amplifiers connected together with 3 dB quadrature hybrids to have a balanced amplifier this inconvenience disappears. We have chosen for this amplifier this second solution. For the larger broadband amplifier (eg 170-860 MHz) this solution must be rejected and the only acceptable solution is to use the feedback technique.

Amplifier design

The first approach for the circuit calculation was made by using the Smith Chart from the input and output impedances given in the TPV 597 data sheet to have, at the input, a reflected power so that the gain will be flat and at the output to obtain the best match possible.

INPUT VSWR VERSUS FREQUENCY TO OBTAIN A FLAT GAIN :

The power gain can be approximated by :

$$G \simeq \left(\frac{F_{max}}{F}\right)^2$$

F_{max} is the frequency for which power gain drops to unity.

The transmission loss due to the input reflection is :

$$\alpha = 1 - |\rho|^2$$

ρ is the reflection coefficient.

To have $G\alpha$ constant we must have :

$$G\alpha \simeq \left(\frac{F_{max}}{F}\right)^2 [1 - |\rho|^2] = G_H = \left(\frac{F_{max}}{F_H}\right)^2$$

G_H is the gain at the highest frequency used (F_H)

or

$$|\rho| \simeq \left[1 - \left(\frac{F}{F_H}\right)^2\right]^{1/2}$$

$$VSWR = \frac{1 + |\rho|}{1 - |\rho|} \simeq \frac{1 + \left[1 - \left(\frac{F}{F_H}\right)^2\right]^{1/2}}{1 - \left[1 - \left(\frac{F}{F_H}\right)^2\right]^{1/2}}$$

Figure 1 shows the theoretical VSWR versus frequency with an insertion loss of 0 dB (implies $\rho = 0$) for 860 MHz. We have defined the input circuit from the TPV597 input impedance to have an input VSWR as close as possible to this curve, and have assumed that output circuit losses versus frequency is negligible.

After we have calculated separately the input and the output circuits, we optimized some of the parameters by means of the global amplifier and the TPV597 S-parameters, with the COMPACT Program.

— RF equivalent circuit : Figure 2
— Program : Figure 3
— Calculated gain and empirical gain : Figure 4
— Calculated and empirical input VSWR : Figure 5
— Calculated and empirical output VSWR : Figure 6

Amplifier Performance

— IMD versus output power: Figure 7A
— IMD versus frequency: Figure 7B
— Input return loss and VSWR : Figure 5
— Output return loss and VSWR : Figure 6
— Gain versus frequency : Figure 4
— Bias conditions : $V_{ce} = 20$ V ; $I_e = 440$ mA

Technology and layout considerations

— The glass Teflon 1/16 inch ($\epsilon_r = 2.55$) is used as board material. This substrate is soldered to the heatsink to have a good contact and repeatable results.

Figure 8 shows the circuit diagram and the bias circuit; Figure 9 shows the PC board layout.

Combined - Transistor Stage

In many instance the power output requirements of transposers exceed the capability of a single transistor, which forces the designer to use combinations of transistors. They can be combined by pair with quadrature combiners (See figure 10). Since quadrature combiners have the ability to channel the reflected power from the amplifier into the fourth port of the combiner it means the input and output VSWR become very low (VSWR < 1.2). The power gain is reduced due to the couplers insertion loss by 0.6 dB. Coupler imbalance should also be taken into account as causing some IMD degradation.

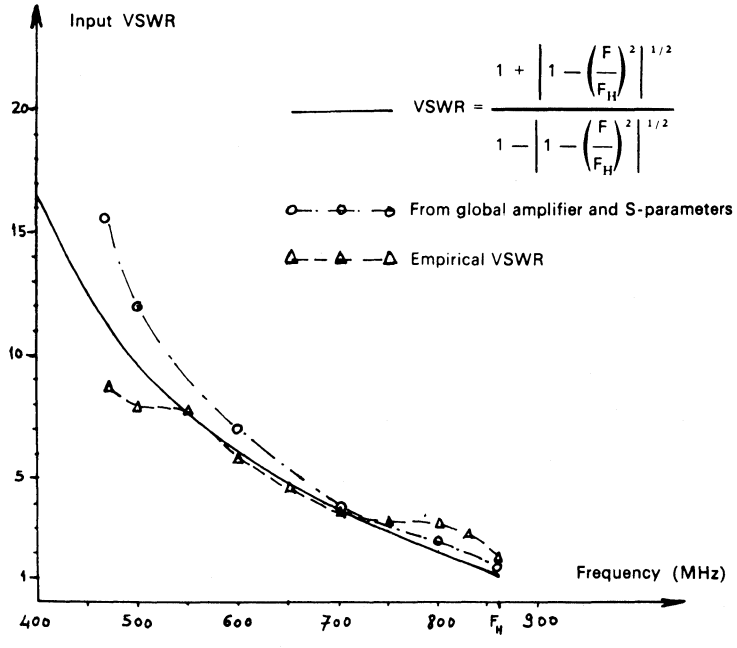
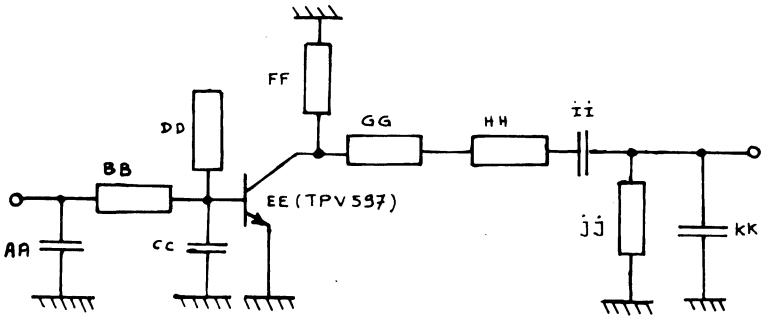


Figure 1. Input VSWR



	AA	BB		CC	DD		FF	
	pF	Z_0 (Ω)	L (mm)	pF	Z_0 (Ω)	L (mm)	Z_0 (Ω)	L (mm)
Calc. value	4.5	50	32.0	29.3	25	14	50	72.2
Empirical value	4.7	50	45.4	10.0	25	14	50	34.9

	GG		HH		II	JJ		KK
	Z_0 (Ω)	L (mm)	Z_0 (Ω)	L (mm)	pF	Z_0 (Ω)	L (mm)	pF
Calc. value	110	28.4	45	14	5.1	75	50	3.5
Empirical value	110	27.9	45	14	3.9	75	38.4	3.3

L are given for $\varepsilon_r = 1$.

Figure 2. RF Equivalent Circuit for Compact Program

```
MET  AA  ZZ
CAP  AA  PA   — 4.61
TRL  BB  SE   50   — 41.64   1
CAP  CC  PA   — 25.39
ØST  DD  PA   25   14   1
TWØ  EE  S1   50
SST  FF  PA   50   — 63.43   1
TRL  GG  SE   110  28.44   1
TRL  HH  SE   45   14   1
CAP  II  SE   — 5.134
SST  JJ  PA   75   49.98   1
CAP  KK  PA   — 4.129
CAX  AA  KK
PRI  AA  SI   50
END
```

CIRCUIT DEFINITION

```
470  500  600  700
800  860
END
```

FREQUENCY (MHz)

```
.92  176  2.38  72  .033  31  .55  — 166
.91  175  2.21  71  .034  33  .54  — 167
.93  171  1.80  63  .037  34  .56  — 170
.93  170  1.57  59  .039  36  .59  — 168
.92  169  1.40  54  .043  38  .58  — 165
.91  167  1.30  52  .045  40  .58  — 166
END
```

POLAR S PARAMETERS FOR TWØ EE (TPV 597)

```
.5
0  100  1  12
100  100  2  12
END
```

OPTIMIZATION DATA

Figure 3. Compact Program

VARIABLES (—)	GRADIENTS
(1) : 4.51899	(1) : — .894864
(2) : 32.0136	(2) : .704452E-01
(3) : 29.2938	(3) : 2.69282
(4) : 72.2399	(4) : .287748
(5) : 5.16145	(5) : 1.68585
(6) : 3.53445	(6) : — .267730

ERR. F. = 7.809

HOW MANY ITERATIONS BEFORE NEXT STOP? , 0 ' RESULTS IN FINAL ANALYSIS.
WANT INTERMEDIATE PRINTS (YES = 1' NO = 0)? TYPE TWO NUMBERS : (I, J) : 0
SEARCH INTERRUPTED, **FINAL ANALYSIS FOLLOWS** :

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN < ANGL)	S21 (MAGN < ANGL)	S12 (MAGN < ANGL)	S22 (MAGN < ANGL)	S21 DB	K FACT.
470.00	0.88 < 134	3.53 < 86.3	0.049 < 45.3	0.11 < 105	10.97	0.75
500.00	0.85 < 128	3.46 < 68.4	0.053 < 30.4	0.12 < 109	10.79	0.90
600.00	0.75 < 92	4.19 < 12.2	0.086 < — 16.8	0.05 < 5	12.45	0.78
700.00	0.59 < 55	4.48 < — 39.2	0.111 < — 62.2	0.19 < — 127	13.02	0.78
800.00	0.43 < 11	4.34 < — 93.2	0.133 < — 109.2	0.26 < 180	12.75	0.86
860.00	0.20 < — 44	4.08 < — 135.2	0.141 < — 147.2	0.26 < 114	12.22	1.01

COMPACT PROGRAM

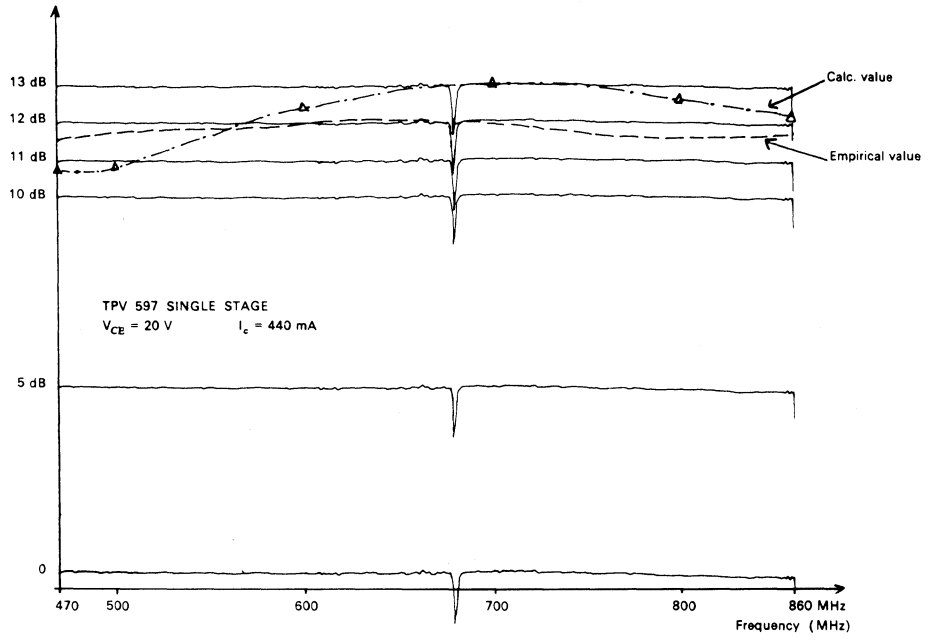


Figure 4. Gain versus Frequency

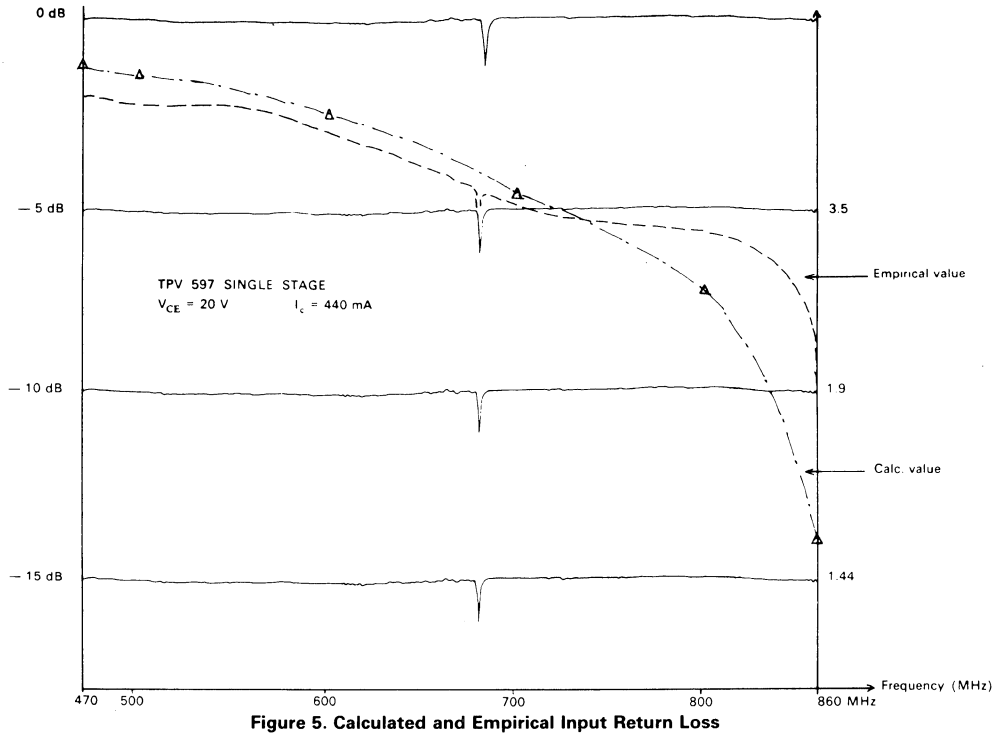


Figure 5. Calculated and Empirical Input Return Loss

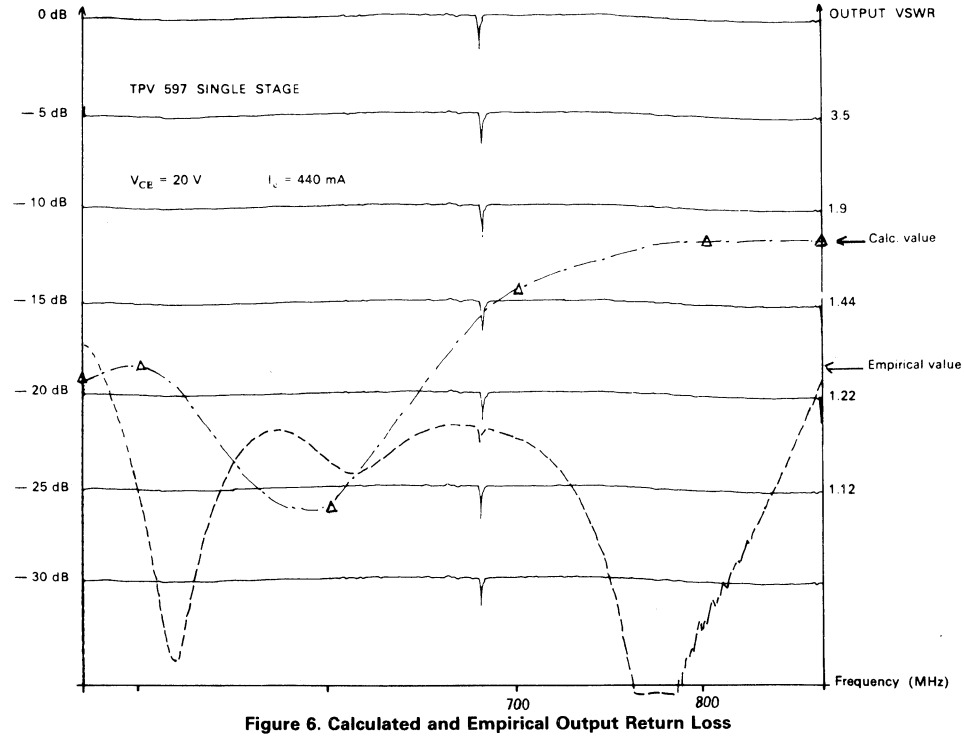


Figure 6. Calculated and Empirical Output Return Loss

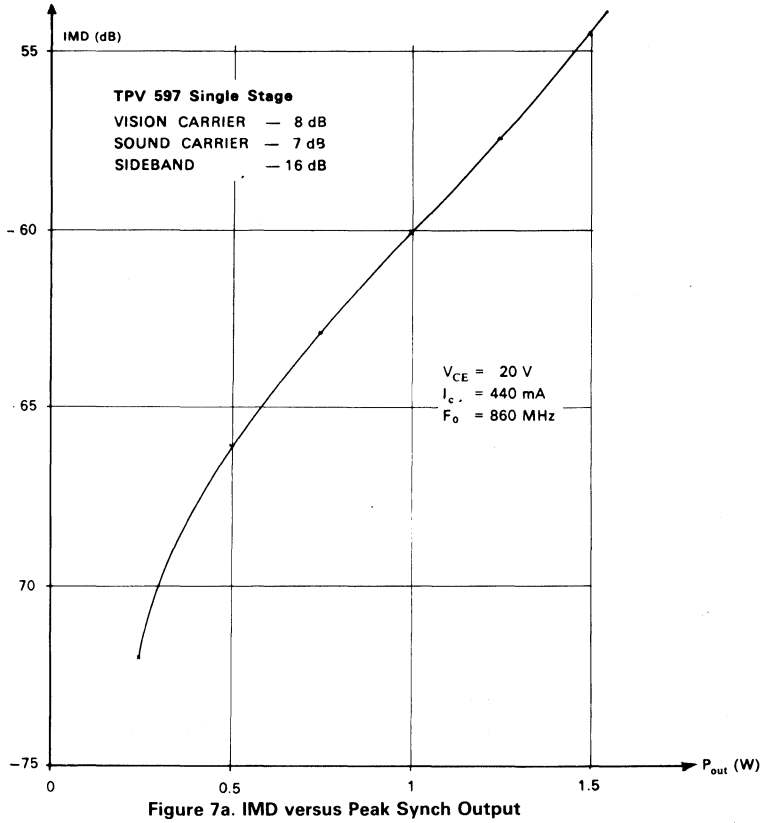


Figure 7a. IMD versus Peak Synch Output

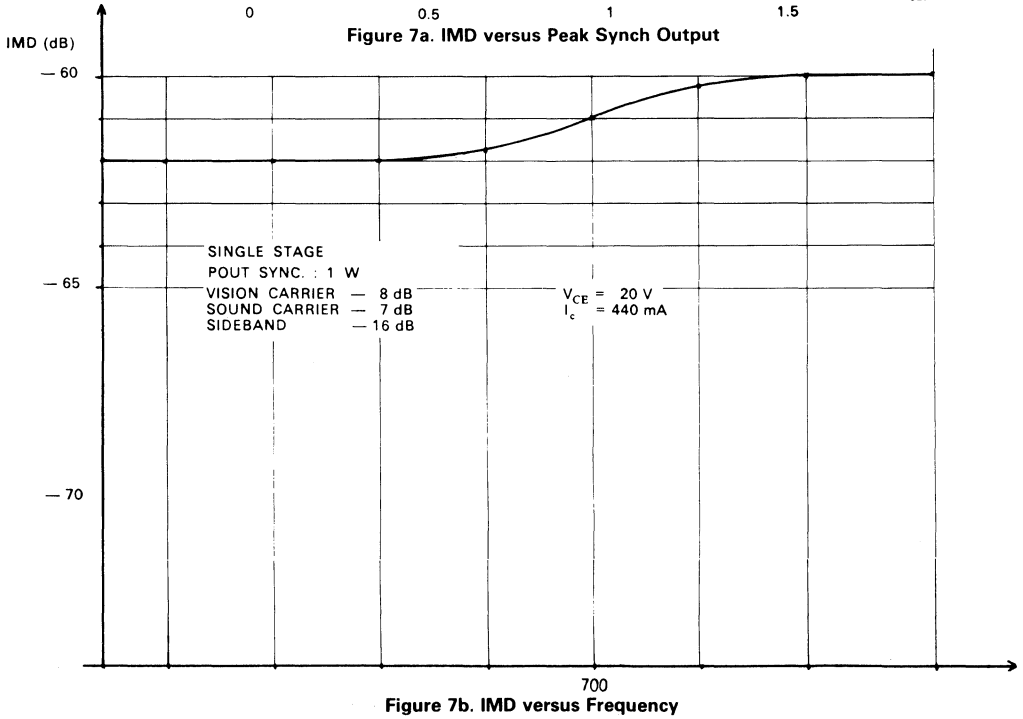
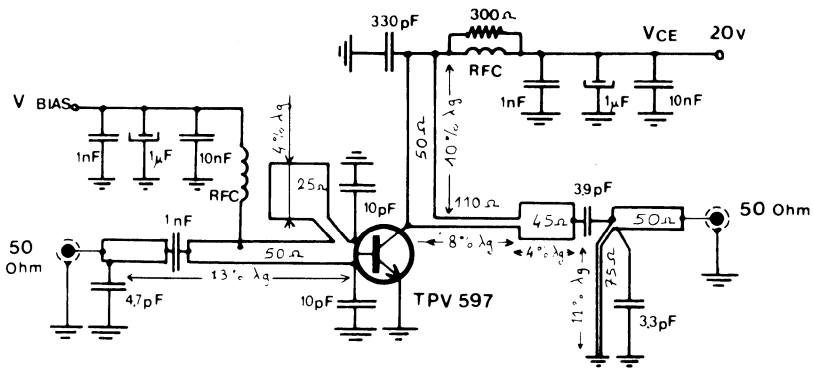


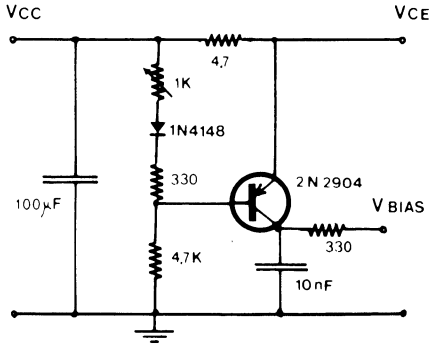
Figure 7b. IMD versus Frequency



Lengths are given at F_o = 860 MHz $\left(\lambda g = \frac{3.10^8}{F_o \sqrt{\varepsilon_{eff}}}\right)$

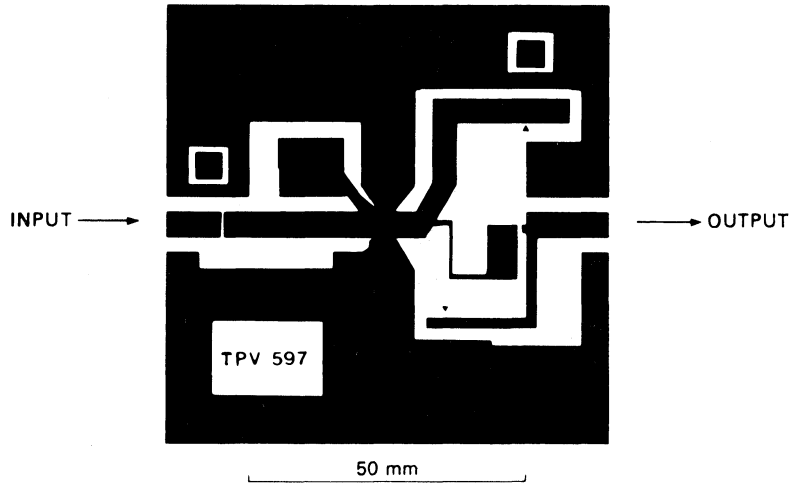
Glass teflon ϵ_r = 2.55, 1 16" board material.

a) Circuit Diagram



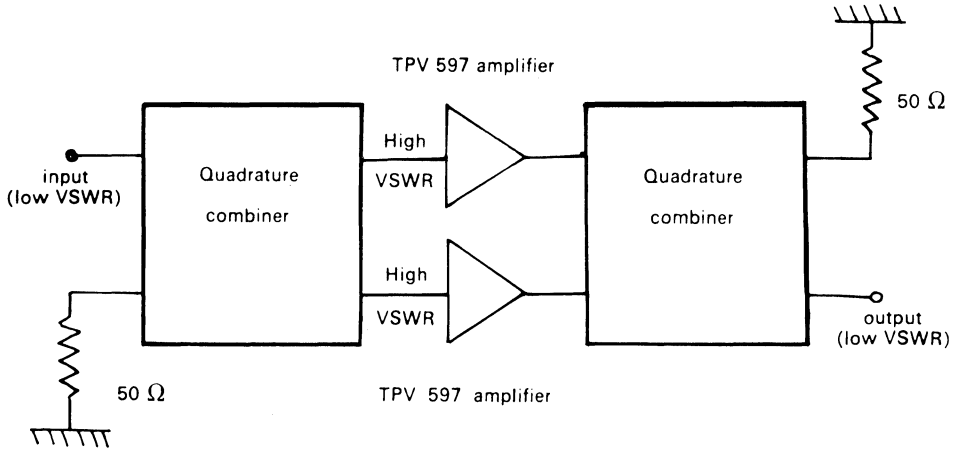
b) Class A Bias Circuit

Figure 8. Circuit Diagram and Bias Circuit



Board material : Glass Teflon ; 1/16 inch ; ϵ_r = 2.55

Figure 9. PC Board Layout (Not to Scale)



The 3 dB quadrature combiners can be supplied by :

— ANAREN (10 264-3)
— SAGE wireline (4450900)

Figure 10. Two Broadband Amplifiers Combined with Quadrature Combiners

How Load VSWR Affects Non-Linear Circuits

Prepared by
Don Murray
RF Devices Division
Lawndale, California

Reprinted from **RF Design** Magazine

If your amplifiers test out fine in the lab but fail QC testing, the testing environment – not the product – is likely at fault.

Consider the following scenario: You're designing and implementing into production a broadband Class C power amplifier. During your design phase, you follow all the rules of science and also dig into your bag of electronic tricks to meet the design specification. Your design is fabricated and tested successfully in the lab. Twenty-five more units are built in the lab and they, too, test out fine.

Confident that both design and production procedures are satisfactory, you begin series production. But when the first units reach RF test, not one meets specification. Yet when you retrieve the units, they test OK in the lab.

What's wrong with these amps? Probably nothing. This scenario, in one form or another, is all too common in the design and manufacture of non-linear RF circuitry. The culprit is correlation of test systems. A difference of .5 dB is enough to fail units that are perfectly good, resulting in unnecessary and expensive retesting or even reworking. Still worse, a half dB error will pass units that don't meet specs and never should be shipped.

Such correlation errors will disrupt an even more important function, that of maintaining product continuity. A device built in 1982 should perform the same as an identical model number device built in 1976. Another way of saying this is that a device tested in a 1982 test system should produce the same results when tested in a 1976 system. The key, of course, is RF correlation.

What is RF correlation? Simply put, RF correlation occurs when target error limits are established **and** adhered to on a continuous basis among two or more testing stations. Such correlation is essential to cost-effect production of non-linear RF and microwave power amplifiers, whose circuits are extremely sensitive to the impedance of their loads, either in test systems or equipment environments. It is easy to compensate for the insertion loss errors in an attenuator, but it is much more difficult to compensate for variations in the input impedance difference between attenuator pads, that is, the load VSWR.

Let's examine RF correlation on both an empirical and theoretical level.

EMPIRICAL APPROACH

The empirical approach is shown in Table I, where several test circuit loads (consisting of series attenuators, directional couplers and RF switches) were assembled. The insertion loss and input impedance of each load string was measured. Following this, the individual loads were connected to a given test circuit containing a common base microwave power transistor. The power meter used was also a constant.

Table I shows insertion loss, insertion loss corrections, indicated RF power, and actual power data of each load string. A maximum error of 0.52 dB was detected with a standard deviation of .19 dB. All these loads had a VSWR less than 1.1:1 at the frequency tested. A VSWR of 1.1:1 is better than the published specifications of commercially available attenuators, directional couplers, and RF switches from most leading manufacturers. A VSWR of 1.5:1 is a typical VSWR specification limit at 1.4 GHz. It must be noted that many users will gladly pay an additional nominal charge for components meeting a tighter VSWR spec.

THEORETICAL APPROACH

The vehicle for the theoretical discussion is the well known expression:

$$P_O = \frac{(V_{CC} - V_{CESAT})^2}{2R_L}$$

Where: P_O = Power output
V_{CC} = Collector supply voltage
V_{CESAT} = Collector-Emitter saturation voltage
R_L = Load resistance.

This expression is valid for a narrow range of R_L (10% range maximum). Over a wider range of R_L, significant changes in V_{CESAT} occur as a function of R_L. Output power varies with the square of V_{CESAT}. V_{CESAT} is a very strong function of collector current and transistor die temperature.

The theoretical approach will evaluate the changes in amplifier output power (P_O) for a given change in load resistance (R_L).

For simplicity, let us assume the following hypothetical conditions, which are typical of today's RF power transistors.

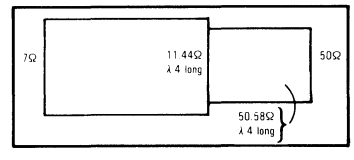
Hypothetical conditions:
V_{CC} = 28V
V_{CESAT} = 1.5V
P_{OUT} = 50W
Frequency = 1.0 GHz
Solving for load resistance:

$$R_L = \frac{(V_{CC} - V_{CESAT})^2}{2P_O} = \frac{702.25}{100} = 7.02\Omega$$

Additionally, assume that a simple two-section impedance matching network matches the 7Ω to 50Ω. Let this two-section match consist of two λ/4 wave transformers.

Given the conditions we have hypothesized, the R_L of 7.02Ω represents the collector load that will yield the best simultaneous satisfaction of device efficiency, device gain, gain transfer characteristics, and saturated power.

For minimum Q, with a 2 section match, the transformation ratio of each section is



$$\sqrt{\frac{50}{7}} = 2.67.$$

$$Z_O \text{ 1st section} = \sqrt{(7)(2.67)(7)} = 11.44\Omega$$

$$Z_O \text{ 2nd section} = \sqrt{(7)(2.67)(50)} = 30.58\Omega$$

λ/4 @ 1 GHz = 2.95" = .075m

Table II shows the transformed impedance at the input of the matching network as a function of

Table I. Microwave Load Substitution Study

The vehicle used for this test was a production test fixture and correlation sample #2 for the TRW MRA1417-6 broadband, high-gain transistor. Measurements were taken at 1400 MHz with input power of 1.1W.

Load #	Measured Power Level	Circuit Return Loss	Collector Current	Measured Insertion Loss	Calibration Error	Actual Power	Delta from Reference	Load Input Return Loss	Impedance Angle	Real	Imaginary
1	1.1W	35 dB	–	30.03 dB	+.03 dB	thru	calibration	-40.2	99.1	49.8	+1.0
1	7.7W	16 dB	.51 A	30.03 dB	+.03 dB	7.75W	reference	-40.2	99.1	49.8	+1.0
2	7.6W	15.5 dB	.5 A	39.66 dB	-.44 dB	6.87W	-30.5		-77.5	50.6	-3.0
3	7.65W	15.5 dB	.51 A	39.68 dB	-.32 dB	7.10W	+.38 dB	-34.1	-171.5	50.4	-2.0
4	8.0W	15.5 dB	.51 A	39.8 dB	-.20 dB	7.63W	-.07 dB	-34.1	68.1	50.7	-1.9
5	7.2W	16 dB	.505 A	30.16 dB	+.16 dB	7.47W	-.16 dB	-30.1	-128.0	51.1	-3.0
6	8.3W	15.2 dB	.51 A	39.78 dB	+.22 dB	7.89W	+.08 dB	-31.7	-144.6	47.9	-1.5
7	7.75W	16.2 dB	.505 A	39.73 dB	-.27 dB	7.28W	-.27 dB	-32.7	11.9	49.0	-2.4
8	7.78W	16.8 dB	.503 A	39.7 dB	-.30 dB	7.26W	-.28 dB	-35.4	-111.9	49.1	-1.5

Largest Delta after calibration correction is 0.52 dB.
Mean value of the measured power = 7.41W.
Standard Deviation = .34W = .19 dB.

Note: -30 dB RETURN LOSS = ϱ of 0.03 and VSWR of 1.06:1.

Table II. R_L Effects on Output Power

Load Resistance (Ω)	Transformed Load Resistance (Ω)	Output Power (W)	ΔdB	Cumulative ΔdB
45	6.30	55.73		
			.095	.095
46	6.44	54.52		
			.093	.189
47	6.58	53.36		
			.091	.280
48	6.72	52.25		
			.090	.370
49	6.86	51.18		
			.087	.457
50	7.00	50.16		
			.086	.543
51	7.14	49.18		
			.085	.628
52	7.28	48.23		
			.083	.710
53	7.42	47.32		
			.081	.791
54	7.56	46.45		
			.080	.871
55	7.70	45.60		

Maximum Delta dB Vs. VSWR

VSWR	Maximum ΔdB
1.02	.17 (±.085)
1.04	.34 (±.17)
1.06	.51 (±.255)
1.08	.68 (±.34)
1.10	.87 (±.435)

various load impedances. Our example utilizes a real-to-real impedance match for convenience. The analysis also is appropriate for an imaginary-to-real match in that center of the VSWR circle at the input to the matching network will be rotated but won't change in magnitude from the data presented.

CONCLUSION

The data presented in table represents the power variation into a load with a VSWR of 1.1:1 relative to 50Ω. The result is a power output of 50W ± 5.3W (±.435 dB). The total Delta is 10.3W (.87 dB). This is enough to:

A) Make a good circuit look bad, or . . .

B) Make a bad circuit look good.

This analysis was done for a single frequency. The problem is compounded in a broadband environment by requirements for a good broadband load impedance.

TEST EQUIPMENT ACCURACY

Test equipment manufacturers have produced some very impressive equipment in recent years; however, the accuracy of a well constructed system using the latest equipment available is generally considered to be no better than ±3%. Considering the number of variables in RF testing and the magnitude of the task faced by the test equipment manufacturers, ±3% is no small achievement. However, ±3% is ±.13 dB. This ±.13 dB added to the ±.435 dB indicated earlier yields a total possible error magnitude of ±.565 dB. This adds up to a total possible error of ±14% into a load with 1.1:1 VSWR. The output power range of our amplifier is now 50W ± 7.05W.

Now we see how bad things can be, a few comments on reality are in order.

The author believes that the correlation target for the test of RF power devices should be ±0.2 dB, which we believe is the optimum tolerance for combining strict quality standards and the need for easy repeatability under series production conditions. If more than an occasional device fails this test, do not assume that the devices are at fault. Instead, first analyze the test circuit and then the test system to determine the reason for the additional error. Some suggestions on how to maintain a ±0.2 dB correlation are shown in Table III.

Table III. Notes

Suggestions to the Maintenance of Correlation

1. Serialize and document all components (attenuators, directional couplers, power meters, detectors, etc.) of the test system. Do not disturb the system once calibration has been performed. Calibrate the system once a month.
2. Require that loads have a calibration return loss ≥ -35 dB (VSWR of 1.05:1) in frequency band of interest.
3. Dedicate test systems to specific circuits or products. This is necessary for both correlation and product continuity.
4. The placement of transistors in the test fixtures must be uniform. For instance, flanged transistors should be placed in the test fixtures with the device pushed towards collector load circuitry.
5. Be selective when using cables in test systems. For example, the MIL-C-17 specification for "RG" cable types says that RG-58 can have a characteristic impedance from 48 to 52Ω (maximu VSWR of 1.04:1) when terminated in a "perfect" 50Ω load.
6. Be very selective when choosing RF switches. The VSWR of a mechanical switch will vary with time.
7. If possible, terminate the system with a 50Ω load rather than an attenuator. Load manufacturers need only consider the VSWR of a load. However, for attenuator, tradeoffs must be made between VSWR and frequency response. Measure power and other performance parameters via calibrated directional couplers.

The 0.2 dB target is an achievable target in broadband test systems. However, a constant awareness of the test system capabilities and potential problem areas is mandatory. RF correlation problems will never go away, but they can be made easier to handle.

AN1033

Match Impedances in Microwave Amplifiers

and you're on the way to successful solid-state designs. Here's how to analyze input/output factors and to create a practical design.

Prepared by
Roger DeBloois

The key to successful solid-state microwave power-amplifier design is impedance matching.

In any high-frequency power-amplifier design, improper impedance matching will degrade stability and reduce circuit efficiency. At microwave frequencies, this consideration is even more critical, since the transistor's bond-wire inductance and base-to-collector capacitance become significant elements in input output impedance network design.

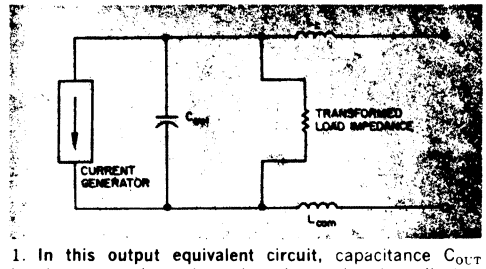
In selecting a suitable transistor, therefore, keep in mind that the input and output impedances are critical along with power output, gain and efficiency.

Unless the selected transistor is used at frequencies that are much lower than the maximum operating frequency, the input impedance is largely inductive with a small real part. The large inductance is due to bond wires that connect the transistor chip to the input lead of the package and to the common-element bond wires. The small real part of the input impedance is due to the large geometries required to generate high power at high frequencies; the base bulk resistance may be the predominant part of the real input impedance.

Use microstrip stubs at input network

The first and most important step in designing the input matching network for the selected device is to provide a shunt capacitance that will resonate the inductive component of the input impedance. This step forms the low-pass matching section of the network and should provide the smallest possible transformed impedance. To minimize the inductive component, the input and common-element lead lengths must be kept short.

The resonating capacitance is generally best provided by a microstrip stub. In some cases the stub producing the required capacitance is so large that a practical circuit size cannot be realized. It is best then to distribute as much of this capacitance as is physically practical and to provide the balance with high-quality chip capacitors.



1. **In this output equivalent circuit,** capacitance C_{OUT} is almost equal to the selected transistor's collector-to-base capacitance C_{ob}.

The first section of the impedance matching network is extremely important because it can degrade the stability of the amplifier if it is not well designed. Depending on the design frequency of the amplifier and the transistor selected, the resonated real impedance can range from less than 50 Ω to much higher. When it is below 50 Ω, an additional low-pass matching section can be conveniently added to achieve the required 50-Ω impedance at the input.

The higher-impedance case presents a special problem if microstrip techniques are used to build the matching network. The problem occurs because the resonated impedance may be as high as 300 Ω. Reducing this to 50 Ω by use of a low-pass network configuration requires a series-transmission line that will behave as an inductor. The rule of thumb is that the characteristic impedance of the transmission line must be at least twice the higher impedance before such behavior results. Examination of the accompanying table shows that characteristic impedance lines of greater than 100 Ω are very narrow. Narrow transmission lines (less than 0.01-inch wide) should be avoided wherever possible, because repeatability of width dimensions is poor. Also, the loss in a narrow line may become excessive. A better solution is to use a quarter-wave transmission-line transformer with a characteristic impedance

equal to the square root of the 50-Ω impedance product: $Z_o = \sqrt{50\,Z_R}$.

Make output bandwidth wider than input

The output impedance of a microwave power transistor is usually defined as the conjugate of the load impedance required to achieve the device performance. A typical output equivalent circuit is shown in Fig. 1. The capacitance C_{out} is nearly equal to the collector-base capacitance C_{ob} specified for the selected transistor. L_c is the inductance of the bond wires used to bridge from the collector metallization area to the package output lead, and L_{com} represents the inductive effects of the common element bond wires.

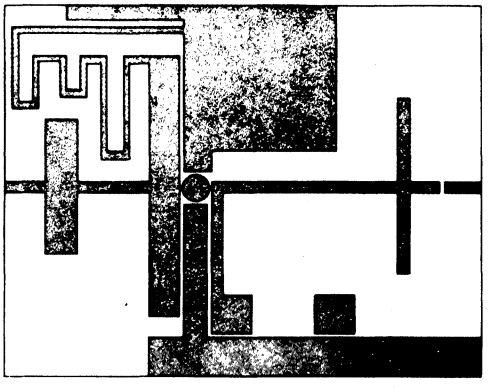
For correct operation of the transistor, the ultimate load impedance must be transformed to a real impedance across the current generator. This real impedance is determined by

$$R_L = \frac{[V_{cc} - V_{ce}(sat)]^2}{2P_{out}}.$$

The load impedance presented to the package terminals will contain the real impedance at the current generator, transformed to a lower value by the low-pass L section formed by C_{out} and the parasitic inductances L_c and L_{com}. Usually the reactive part of the load impedance is made inductive to tune out the residual capacitance of the device.

The output matching network should be designed so it has greater bandwidth than the input matching network. Providing a good collector match, both above and below the design frequency, ensures that the input power will be reflected before the collector VSWR rises to values that endanger the transistor. In this way the transistor is protected from off-frequency operation. The amount of additional bandwidth required for protection of the transistor depends on the ruggedness of the transistor used. The manufacturer's specifications for VSWR tolerance and input Q can be a guide for determining the bandwidth requirements of the input matching network.

One technique for obtaining the required bandwidth is to resonate a portion of the capacitive reactance of the transistor output impedance with a shunt inductor. The shunt inductor can also be used to feed the collector supply voltage to the transistor. Additional transformation may be obtained from a low-pass matching section.



2. **With this typical microwave amplifier breadboard layout,** the entire board can be soldered to a metal plate to provide a path for thermal cooling.

By adjusting the amount of shunt inductance and rematching with the low-pass section, the designer can create a truly broadband output match.

Don't overlook base and collector paths

In addition to matching the device impedances, direct-current paths must be provided to the base and collector of the transistor. The collector path is provided by the shorted stub in the impedance-matching network. The base path requires the addition of a choke from the base to ground. The choke can be a lumped element or a distributed shorted stub of sufficient impedance to be negligible in the circuit. A quarter-wavelength stub is ideal. The narrowest practical line should be selected. In addition a dc blocking capacitor is required in the collector circuit. Also needed is a bypass capacitor to provide the proper ac shorting point for the inductive stub in the collector-matching network.

Selection of a blocking capacitor is relatively straightforward. The capacitor should be chosen to provide low loss at the operating frequency while maintaining the capacitance at a value that inhibits low-frequency oscillation. The latter is caused by the series capacitor's tendency to display rising reactance with decreasing frequency.

Blocking capacitors must be large enough to preserve coupling characteristics down to a frequency where the shunt-feed chokes can effec-

Microstrip Z_0 and velocity factor vs width-to-height (W/H) ratio.

(Prepared by Don Schulz, Applications Engineer)

W/H	Air K = 1.0		Teflon K = 2.55		Epoxy K = 4.25		Alumina K = 9.6	
	Z_o	V_P	Z_o	V_P	Z_o	V_P	Z_o	V_P
0.630	168.425	1.000	110.683	0.657	87.986	0.522	60.977	0.362
0.695	161.878	1.000	106.258	0.656	84.414	0.521	58.441	0.361
0.766	155.370	1.000	101.865	0.656	80.870	0.521	55.927	0.360
0.844	148.909	1.000	97.509	0.655	77.360	0.520	53.440	0.359
0.931	142.506	1.000	93.199	0.654	73.888	0.518	50.985	0.358
1.026	136.171	1.000	88.941	0.653	70.463	0.517	48.566	0.357
1.131	129.916	1.000	84.745	0.652	67.090	0.516	46.187	0.356
1.247	123.753	1.000	80.616	0.651	63.775	0.515	43.853	0.354
1.375	117.692	1.000	76.565	0.651	60.524	0.514	41.568	0.353
1.516	111.746	1.000	72.597	0.650	57.345	0.513	39.337	0.352
1.672	105.926	1.000	68.721	0.649	54.243	0.512	37.164	0.351
1.843	100.242	1.000	64.944	0.648	51.223	0.511	35.053	0.350
2.032	94.706	1.000	61.273	0.647	48.291	0.510	33.007	0.349
2.240	89.327	1.000	57.714	0.646	45.451	0.509	31.030	0.347
2.470	84.115	1.000	54.271	0.645	42.709	0.508	29.123	0.346
2.723	79.076	1.000	50.951	0.644	40.066	0.507	27.289	0.345
3.002	74.218	1.000	47.757	0.643	37.527	0.506	25.531	0.344
3.310	69.546	1.000	44.692	0.643	35.094	0.505	23.849	0.343
3.649	65.065	1.000	41.759	0.642	32.768	0.504	22.244	0.342
4.023	60.779	1.000	38.959	0.641	30.550	0.503	20.716	0.341
4.435	56.689	1.000	36.292	0.640	28.440	0.502	19.266	0.340
4.890	52.796	1.000	33.760	0.639	26.439	0.501	17.892	0.339
5.391	49.100	1.000	31.360	0.639	24.544	0.500	16.594	0.338
5.944	45.600	1.000	29.091	0.638	22.755	0.499	15.370	0.337
6.553	42.291	1.000	26.952	0.637	21.069	0.498	14.218	0.336
7.224	39.173	1.000	24.938	0.637	19.485	0.497	13.138	0.335
7.965	36.233	1.000	23.047	0.636	17.998	0.497	12.125	0.335
8.781	33.484	1.000	21.275	0.635	16.606	0.496	11.179	0.334
9.681	30.904	1.000	19.618	0.635	15.305	0.495	10.295	0.333
10.674	28.491	1.000	18.071	0.634	14.091	0.495	9.472	0.332
11.768	26.240	1.000	16.629	0.634	12.961	0.494	8.707	0.332
12.974	24.143	1.000	15.288	0.633	11.911	0.493	7.996	0.331
14.304	22.192	1.000	14.043	0.633	10.937	0.493	7.338	0.331
15.770	20.381	1.000	12.888	0.632	10.033	0.492	6.728	0.330
17.387	18.702	1.000	11.818	0.632	9.198	0.492	6.164	0.330
19.169	17.148	1.000	10.830	0.632	8.425	0.491	5.644	0.329
21.133	15.172	1.000	9.917	0.631	7.713	0.491	5.164	0.329
23.300	14.385	1.000	9.074	0.631	7.056	0.490	4.722	0.328
25.688	13.162	1.000	8.299	0.630	6.451	0.490	4.315	0.328

Table continued

W/H	Air K = 1.0 Z_o	V_p	Teflon K = 2.55 Z_o	V_p	Epoxy K = 4.25 Z_o	V_p	Alumina K = 9.6 Z_o	V_p
28.321	12.036	1.000	7.585	0.630	5.894	0.490	3.942	0.327
31.224	10.999	1.000	6.929	0.630	5.383	0.489	3.598	0.327
34.424	10.047	1.000	6.326	0.630	4.914	0.489	3.284	0.327
37.953	9.172	1.000	5.773	0.629	4.483	0.489	2.995	0.327
41.843	8.370	1.000	5.266	0.629	4.089	0.489	2.731	0.326
*46.132	7.634	1.000	4.801	0.629	3.727	0.488	2.489	0.326
50.860	6.960	1.000	4.376	0.629	3.397	0.488	2.267	0.326
56.073	6.343	1.000	3.987	0.629	3.094	0.488	2.065	0.326
61.821	5.779	1.000	3.632	0.628	2.818	0.488	1.880	0.325
68.157	5.264	1.000	3.307	0.628	2.566	0.487	1.711	0.325
75.144	4.792	1.000	3.010	0.628	2.335	0.487	1.557	0.325
82.846	4.362	1.000	2.739	0.628	2.125	0.487	1.417	0.325
91.337	3.969	1.000	2.492	0.628	1.933	0.487	1.289	0.325
100.700	3.611	1.000	2.267	0.628	1.758	0.487	1.172	0.324

tively short the respective port to ground. Coupling capacitors should not be excessively large, or they may produce as much as 1-dB loss in gain with a corresponding decrease in efficiency in the case of collector coupling capacitors. The Q of the coupling capacitor determines the acceptable range of capacitance values and is generally inversely related to capacitance.

Bypass capacitors are selected by analysis of the same considerations as those for blocking capacitors. A large bypass capacitor (tantalum or electrolytic), placed from the dc feedpoint to ground, prevents tendencies toward low-frequency oscillation in the circuit. Also, it may be necessary to add smaller bypass capacitors to preserve stability over a wide range of frequencies.

Adjust for bandwidth and physical dimensions

The circuit design may be adjusted quickly for bandwidth requirements through use of a computer optimization program such as Magic, offered by University Computing of Dallas, Tex. When that step is finished, electrical dimensions must be converted to physical dimensions.

At this point in the design sequence, the dielectric material must be chosen. Three commonly used materials are Teflon fiberglass, epoxy fiberglass and alumina. Above 500 MHz, epoxy fiberglass exhibits too many losses to be a good choice. Teflon fiberglass can be used up to several gigahertz; it has reasonable dielectric losses and is easy to process. Alumina, a ceramic, offers a high dielectric constant, good dimensional consistency and small circuit geometry.

When plastic materials are used, it's a good practice to measure the material thickness and dielectric constant, because variations are common. In a recent test the dielectric constant of a sheet of epoxy fiberglass material was measured at 4.55 at 1 MHz and 4.25 at 500 MHz. If the manufacturer's value of 5.5 had been used for the design of matching networks, considerable error would have resulted.

The physical dimensions of the matching circuitry may be calculated from the data in the table. The line lengths are scaled by the velocity factor, which is equal to $Z_o Z_{o\ air}$ in air for a constant width-to-height ratio, W H.

The final design of a typical breadboard microwave amplifier is shown in Fig. 2. The ground areas on the top of the board are connected to the microstrip ground plane by 2-mil-thick foil wrapped around the edges of the board and the areas directly under the emitter leads of the transistor. The foil is secured to the top and bottom surfaces with solder. Plating may be used for production units. The entire board can be soldered to a metal plate to allow connector mounting and to provide a thermal path for the heat generated by the transistor.

The initial tune-up of the amplifier matching circuits can be expedited by use of a network analyzer and a precision load on the input or output connector. The circuit can be adjusted to match the nominal impedances supplied by the transistor manufacturer. Distributed stubs are purposely made longer than necessary and are adjusted to the correct length by trimming of the

foil on the capacitive stubs. The inductive stub in the output network is adjusted by positioning of the bypass capacitor along the stub and the adjacent ground plane.

This procedure results in a load line that is fairly close to optimum. A transistor can now be inserted in the circuit and the collector matching network readjusted for maximum collector efficiency. Stub tuners are used to match the amplifier input impedance, so that only one variable at a time need be considered. Initially it may be necessary to operate the transistor at reduced collector voltage and power output to avoid excessive stress. When maximum efficiency is obtained, the stub tuner is removed and the input network adjusted for minimum input VSWR.

Now let's design an impedance-matching circuit

Let's consider a practical example of a procedure for the design of impedance-matching circuitry. The sample circuit uses a TRW 2N5596 at 700 MHz as the active device.

Specifications for the completed amplifier are:

$Z_{in} = 50\ \Omega,$
$Z_{out} = 50\ \Omega,$
$P_{out} = 20\ W,$
$G_p = 7\ dB,$
$\eta = 55\%$ minimum.

Specifications for the TRW 2N5596 are:

$P_{out} = 20\ W$ at 1 GHz,
$\eta = 55\%$ minimum at 1 GHz,
$G_p = 5\ dB$ minimum at 1 GHz,
$Z_{in} = 2.5 + J4.0$ at 700 MHz,
$Z_{out} = 6.0 - J12.5$ at 700 MHz.

In practice, the gain of a common-emitter amplifier decreases at a rate of 4 to 5 dB per octave. The 2N5596 at 700 MHz produces about 7 dB of gain. Therefore approximately 4 W of drive will be required to produce 20 W of output power. The collector efficiency can be expected to increase at the lower frequency, but it is difficult to estimate because it is a complex phenomenon. Manufacturers' curves of typical behavior are useful. Output power will not increase significantly with the decreased frequency.

The efficiency-frequency relationship depends on device f_T and ballasting. Heavily ballasted transistors tend to give increased efficiency as frequency is decreased. However, they level out at a lower efficiency than a nonballasted part because of I^2R losses in ballast resistors. The average increase in efficiency as a result of decreasing frequency is about 20% per octave. Values from 10 to 40% per octave have been measured.

The initial phase of the design is best accomplished on an immittance chart. The chart with appropriate values indicated for the sample design is shown in Fig. 3. The input match is achieved when the input impedance is resonated with a capacitive susceptance of 0.18 mhos. This susceptance is realized by use of a pair of capacitive microstrip stubs. Each stub must exhibit a reactance of $2 \times 1/0.18$ mhos, or 11.1 Ω. The length of the stub may be calculated by

$$\tan \theta = \frac{Z_o}{X_c}.$$

For ease of adjustment, the length of the stubs should be less than 60 degrees. Because capacitive reactance is a tangential function, the reactive variations per unit length become increasingly severe past 60 degrees. It is better to decrease Z_o rather than to use longer stubs to achieve higher capacitance. Therefore $Z_o \leq 1.732\ X_c \leq 19.24\ \Omega$. Because it is easier to shorten a microstrip stub than to lengthen it, the Z_o of 15 Ω, for example, provides sufficient adjustment range to accommodate device variations.

The next step is to transform the resonated impedance to 50 Ω. This is accomplished by a series-transmission line with a characteristic impedance of 50 Ω. From Fig. 3, we see that the length of this line can be directly determined to be 0.062 wavelengths, or 22.3 degrees, long. A capacitive susceptance of 0.040 mhos completes the transformation. Again, a pair of capacitive stubs will provide the susceptance. For ease of converting the design to microstrip dimensions, it is convenient to choose a Z_o for the second stub that is equal to that selected for the first. Therefore:

$$\tan \theta = \frac{Z_o}{X_c} = \frac{15}{50} = 0.3,$$
$$\text{or } \theta = 16.7 \text{ degrees.}$$

In this case the length chosen is 20 degrees to allow for some adjustment.

The output match is achieved by partial resonating of the device's output impedance with an inductive susceptance. While the amount of susceptance chosen is arbitrary at this point, the output network bandwidth is affected by the value. From Fig. 3, we can determine that 0.05 mhos is required for the first matching element. This susceptance is achieved by use of a shorted microstrip stub. The length of the stub may be calculated from the equation

$$\tan \theta = \frac{X_L}{Z_o}.$$

If Z_o of the stub is arbitrarily chosen to be 50 Ω,

$$\tan \theta = \frac{20}{50} = 0.4,$$
$$\theta = 21.8 \text{ degrees.}$$

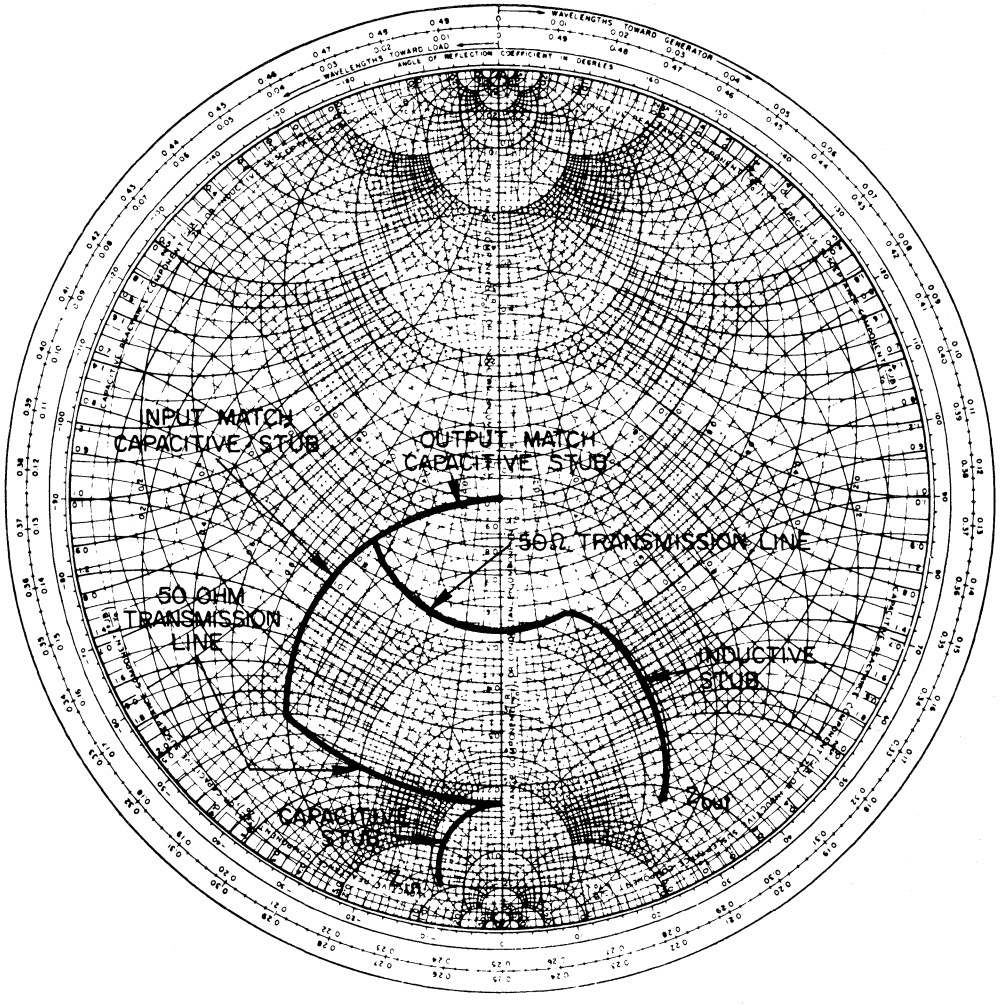
Again, the stub is made somewhat longer because it can be adjusted by sliding the chip

capacitor (ac short) up or down the line length. The remaining transformation is achieved by a 50-Ω series-transmission line of 0.15 wavelengths (54 degrees long) and a capacitive susceptance of 0.014 mhos. Selecting a pair of 50-ohm microstrip lines to provide the susceptance requires a stub length of

$$X_c = 2 \times \frac{1}{0.014} = 143\ \Omega.$$

$$\tan = \frac{Z_0}{X_c} = \frac{50}{143} = 0.350 = 19.3 \text{ degrees.}$$

A stub length of 25 degrees will provide an adequate allowance for adjustment of the circuit. ■■



3. **The immittance chart,** with values specified for the design example, indicates the necessary inductive and capacitive stubs. Impedance transformations are achieved by 50-Ω series-transmission lines.

AN1034

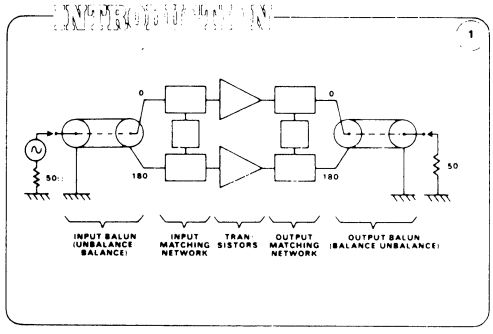
Three Balun Designs For Push-Pull Amplifiers

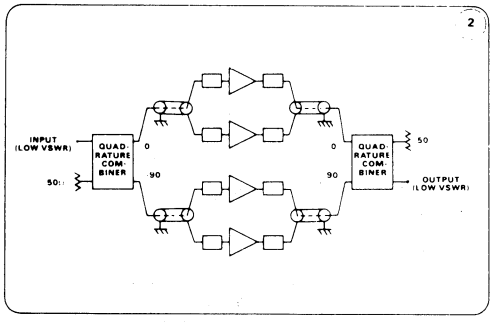
SINGLE RF power transistors seldom satisfy today's design criteria; several devices in separate packages, or in the same package (balanced, push-pull or dual transistors), must be coupled to obtain the required amplifier output power. Since high-power transistors have very low impedance, designers are challenged to match combined devices to a load. They often choose the push-pull technique because it allows the input and output impedances of transistors to be connected in series for RF operation.

Balun-transformers provide the key to push-pull design, but they have not been as conspicuous in microwave circuits as at lower frequencies. Ferrite baluns[2] have been applied up to 30 MHz; others incorporating coaxial transmission lines operate in the 30-to-400-MHz range.[3]

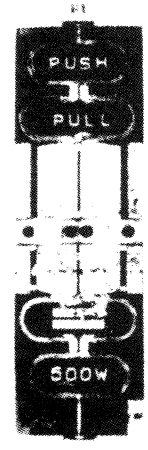
The success of these two balun types should prompt the microwave designer to ask if balun-transformers can be included in circuits for frequencies above 400 MHz. Theory and experimental results lead to the emphatic answer: yes! Not only will baluns function at microwave frequencies, but a special balun can be designed in microstrip form that avoids the inherent connection problems of coax.

On the next six pages, you will observe the development of three balun-transformers—culminating with the microstrip version. None of the baluns was tuned nor were the parasitic elements compensated. In this way, the deviation of the experimental baluns from their theoretical performance could be evaluated more easily. The frequency limitations imposed by the parasitic elements also were observed more clearly.





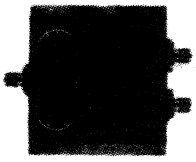
1. A balun transforms a balanced system that is symmetrical (with respect to ground) to an unbalanced system with one side grounded. Without balun-transformers, the minimum device impedance (real) that can be matched to 50 ohms with acceptable bandwidth and loss is approximately 0.5 ohms. The key to increasing the transistors' output power is reducing this impedance ratio. Although 3-dB hybrid combiners can double the maximum power output, they lower the matching ratio to only 50:1. Balun transformers can reduce the original 100:1 ratio to 6.25:1 or less. The design offers other advantages: the baluns and associated matching circuits have greater bandwidth, lower losses, and reduced even-harmonic levels.



A 500-W push-pull amplifier for DME band.

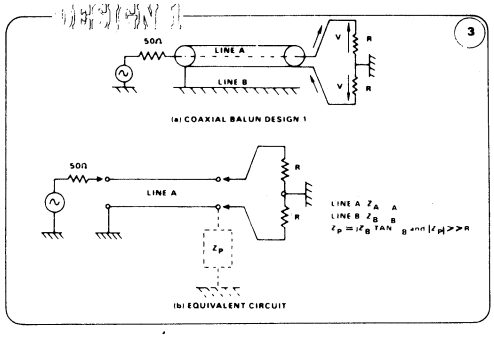
2. Baluns are not free of disadvantages. Coupling a pair of push-pull amplifiers with 3-dB hybrids avoids (for four-transistor circuits) one of these: the higher broadband VSWRs of balun-transformers. A second disadvantage, the lack of isolation between the two transistors in each push-pull configuration, is outweighed by the advantages of the balun design in reducing the critical impedance ratio.

3. In this simple balun that uses a coaxial transmission line, the grounded outer conductor makes an unbalanced termination, and the floating end makes a balanced termination. Charge conservation requires that the currents on the center and the outer conductors maintain equal magnitudes and a 180-degree phase relationship at any point along the line. By properly choosing the length and characteristic impedance, this balun can be designed to match devices to their loads. In the case shown, if $\emptyset_A$ = 90 degrees, the matching condition is:

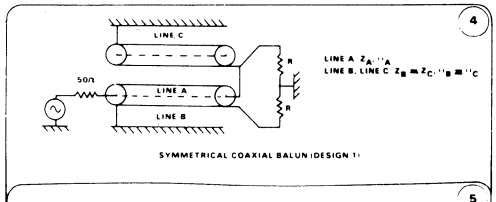


Experimental version of a simple balun using coaxial lines.

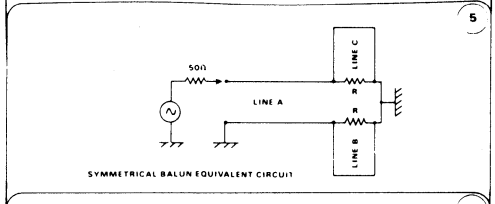
$$Z_A^2 = 2xRx50.$$



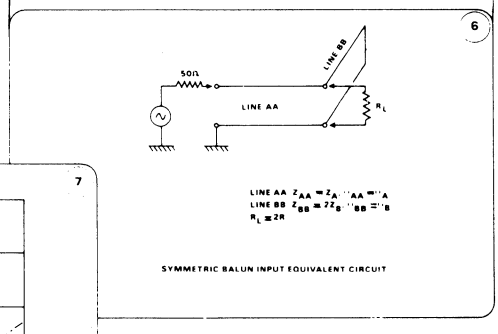
4. By adding a second coaxial line, the basic balun can be made perfectly symmetrical. In this symmetrical coaxial balun, the bandwidth (in terms of the input VSWR) is limited by the transformation ratio, 50/2R, and the leakages, which are represented by lines B and C. If Z_A = 50 ohms and R = 25 ohms, the bandwidth is constrained only by the leakages.



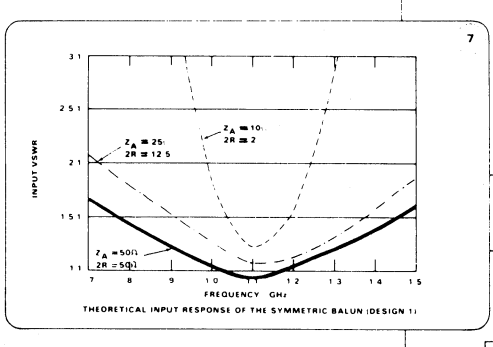
5. The equivalent circuit for the symmetrical balun shows the effect of the leakages (lines B and C) on its performance. A broadband balun can be obtained by using a relatively high characteristic impedance for these leakage lines. In theory, the construction of the baluns insures perfect balance.



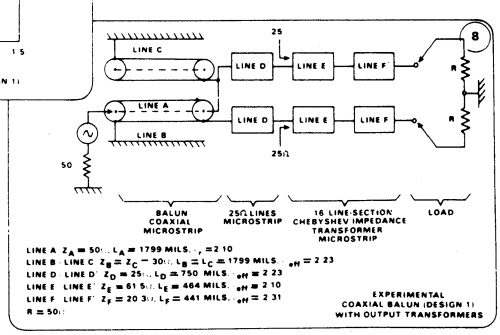
6. The symmetric balun's input equivalent circuit further simplifies its configuration and allows the input VSWR to be calculated.[4] In this design, line A has a characteristic impedance of Z_A = 50 ohms, a length of L_A = 1799 mils, and a dielectric constant (relative) of ϵ_r = 2.10. For lines B and C, Z_0 = 30 ohms, L = 1799 mils, and ϵ_{eff} = 2.23.



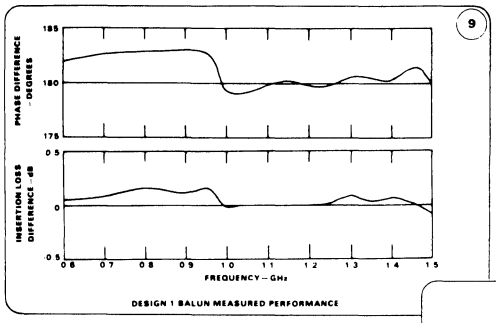
L = 1799



7. The theoretical input VSWR has been calculated for 50-ohm values of Z_A and 2R, and for two other sets of values for these parameters. The performance of an experimental balun will be compared with these theoretical results.

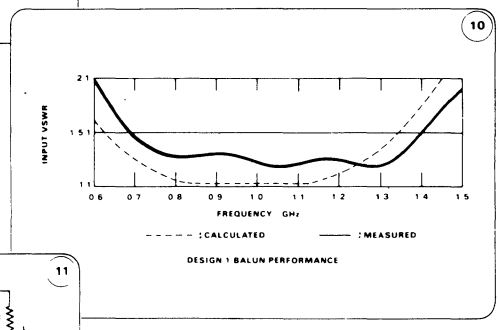


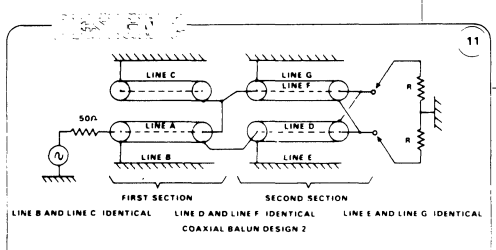
8. Two λ/16 line-section Chebyshev impedance transformers match the experimental balun to a 50-ohm measurement system. The balun was tested from 0.6 to 1.5 GHz.



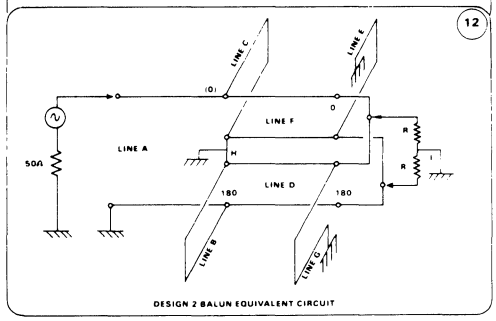
9. The measured phase difference and insertion loss difference, which indicate the maximum unbalance for the Design 1 experimental balun, are 3 degrees and 0.2 dB, respectively.

10. The maximum VSWR measured for the first design is 1.5:1. Note the comparison between the calculated and measured response. The performance shown can be considered valid for amplifier applications up to an octave range.

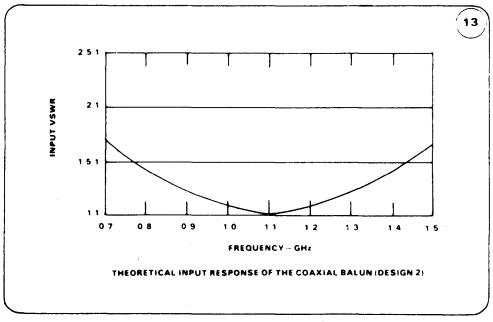




11. The second balun design adds two identical coax lines to the simple balun just described. The inputs of the identical lines are connected in series to the output of the first balun. By putting their outputs in parallel, the final output becomes symmetrical. The output impedance is halved.



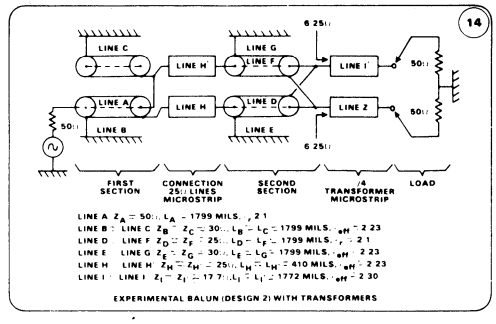
12. The equivalent circuit for the Design 2 balun indicates that its bandwidth, in terms of input VSWR, is limited by the transformation ratios of the first and second sections and the leakages represented by lines B, C, E, and G. If the balun is designed with Z_A = 50 ohms, and $Z_D = Z_F$ = 25 ohms, and if the load, 2R, is set at 2×6.25 ohms, all of the transmission lines will be connected to their characteristic impedances. In this case, the bandwidth will be limited by the leakage alone, and a broadband balun can be obtained by choosing lines B, C, E, and G with relatively high impedance and $\lambda/4$ length for the center frequency. The balun achieves a transformation from 50 ohms to twice 6.25 ohms without causing a standing wave in the coaxial cables.



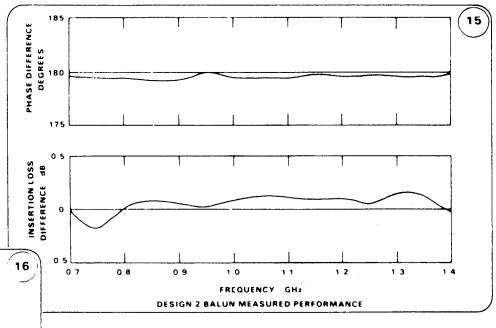
13. The performance of the Design 2 balun can be calculated using its equivalent circuit. The calculated VSWR shows a response very close to the simple coaxial balun (Fig. 10) because the new second section has four times the bandwidth of the first section. This design and its two companions are intended to have octave bandwidths centered at 1.1 GHz, the central frequency used in distance measuring equipment (DME, 1.025 to 1.150 GHz) and tactical air navigation (TACAN, 0.960 to 1.215 GHz). For line A: Z_A = 50 ohms, L_A = 1799 mils, ϵ_r = 2.10; lines B, C, E, and G: Z_o = 30 ohms, L = 1799 mils, ϵ_{eff} = 2.23; lines E and F: Z_o = 25 ohms, L = 1799 mils, ϵ_r = 2.10.

Two-section balun often used in the 100-to-400 MHz range.

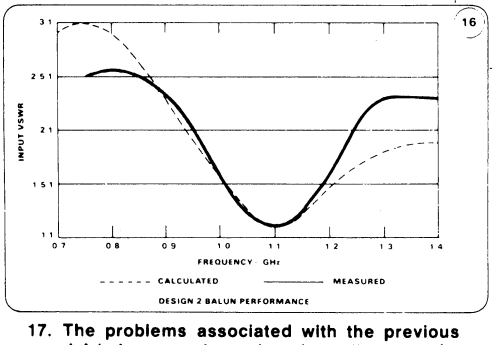
14. Two λ/4 transformers match the experimental two-section coaxial balun's 6.26-ohm impedance to the 50-ohm load. Although these transformers drastically reduce the bandwidth (in terms of the VSWR), they don't affect the balance.



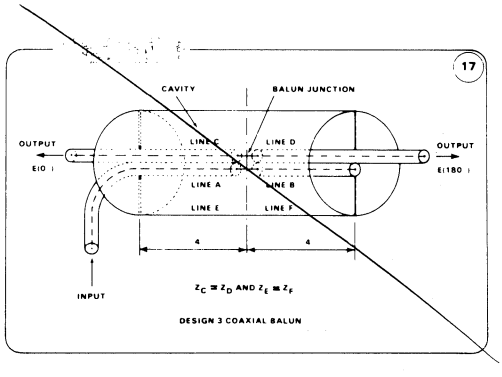
15. The measured phase difference and measured insertion loss difference are plotted for the two-section coaxial balun (Design 2). The maximum unbalances for these two measurements over the octave bandwidth are 1 degree and 0.2 dB.

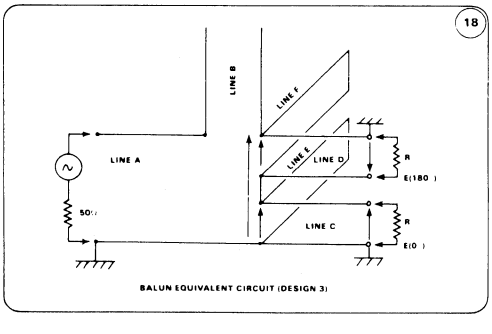


16. The calculated and measured values for the input VSWR for the Design 2 balun show close agreement between the experimental and predicted performances. This indicates that the parasitic inductors at the connections are negligible to at least 1.4 GHz. Moreover, the balun has excellent balance to 1.4 GHz and achieves the 4:1 transformation without causing a standing wave in the coaxial line. Despite the many excellent qualities of the Design 1 and Design 2 baluns, the necessary coaxial line connection limits them to approximately 2 GHz.



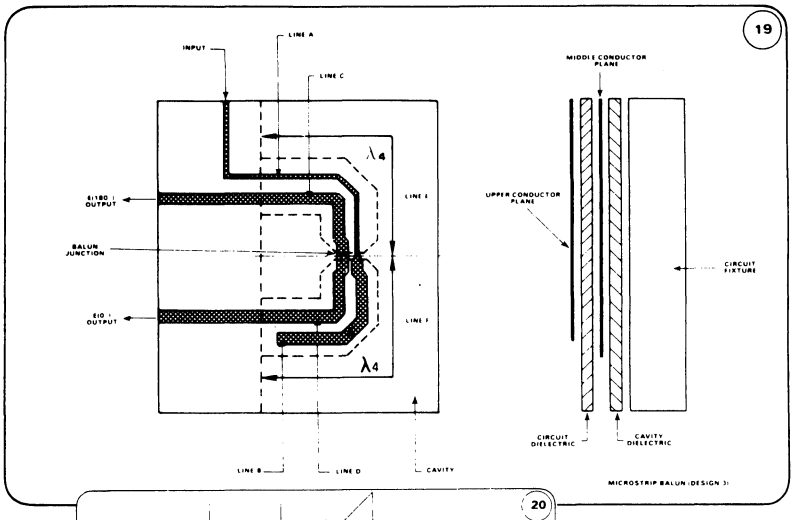
17. The problems associated with the previous coaxial baluns can be reduced or eliminated by using a balun that allows a microstrip coplanar arrangement of the input and output lines, which greatly simplifies the connections to the amplifier. This balun[5] consists of an input line, A, connected in series to three elements in the center of the half-wavelength cavity: a reactive open-circuit stub, B, and the λ/4 output lines, C and D.

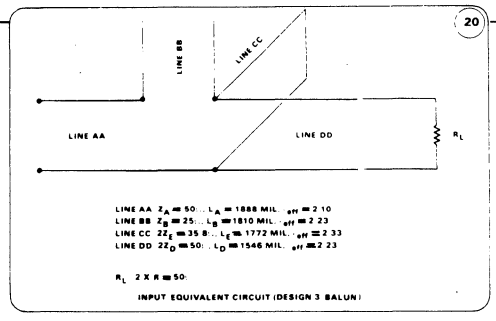




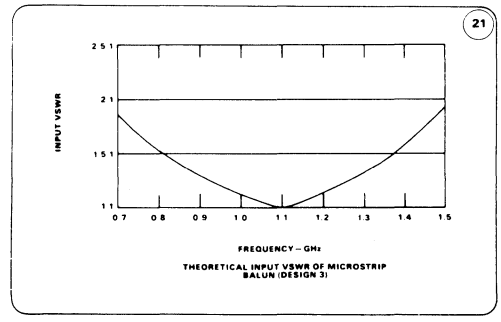
18. The equivalent circuit of the Design 3 coaxial version balun shows lines C and D connected to place their input signals in antiphase, thereby producing two antiphase signals at their outputs. Transmission line impedances and lengths are optimized to achieve the correct input/output transformation ratio and a good match across the desired bandwidth. If only one frequency or a narrow bandwidth is desired, and all lengths are λ/4, the matching condition $Z_A^2/50 = 2Z_c^2/R$, will occur. In this case, Z_E ($Z_E = Z_F$) and Z_B have no significance except for loss.

19. The coplanar arrangement of input and output lines can be accomplished with microstrip technology. The uppermost conductor plane contains input line A, output lines C and D, and the open stub B. Coupling between these lines is avoided by separating them by at least one line width. The middle conductor carries the ground plane for the lines. To avoid radiation loss, the center conductor must extend at least one line width to either side of the upper plane circuit line. The balun resonant cavity is formed by the region between the middle and the lower conductor planes. A hole for the cavity is cut in the circuit fixture, filled with dielectric, and covered with the middle conductor plane. The end-to-end length of the cavity is nominally a half-wavelength at midband. To avoid disturbance of the field distribution, the cavity width must be at least three times the width of the middle conductor plane. The arms of the balun cavity are folded to produce two parallel and proximate output transmission lines. This configuration is more suited to coupling two transistors than the original layout in which the two outputs were on opposite sides (Fig. 17).





20. The input equivalent circuit for the microstrip version of the Design 3 balun allows its theoretical performance to be calculated. The design parameters shown provide a microstrip circuit that can be compared with the coaxial baluns of Design 1 and Design 2. Transmission line A and lines C and D are loaded by their characteristic impedances—in this case, 50 and 25 ohms. The cavity and the stub impose the principal frequency limitation. The impedances of these elements are dictated by the properties of the available dielectric substrates (glass-Teflon 0.020 and 0.0625 inches thick).

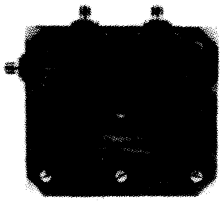


21. The input VSWR can be calculated based on the equivalent circuit for the microstrip balun. For a one-octave bandwidth, the input VSWR is lower than 1.75:1. This calculated performance is similar to that of the two previous balun designs. The design of the microstrip has theoretically perfect balance.

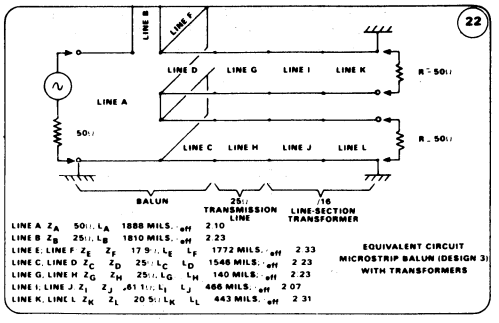
References

1. "35/50 Watt Broadband (160-240 MHz) Push-Pull TV Amplifier Band III," TRW Application Note, TRW RF Semiconductors Catalog No. 97, p. 84AN.
2. "150 W Linear Amplifier 2 to 28 MHz, 13.5 Volt DC," TRW Application Note, TRW RF Semiconductors Catalog No. 97, p. 108AN.
3. TRW Application Notes on the TPM-4100 (100 W, 100 - 400 MHz); the TPM-4040 (40 W, 100 - 400 MHz); the TPV-3100 (110 W, Band III); and the TPV-5050 (50 W, UHF), available from TRW RF Semiconductors.
4. The program used for the circuit calculation was COMPACT (Computerized Optimization of Microwave Passive and Active Circuits).
5. Gordon J. Laughlin, "New Impedance-Matched Wideband Balun and Magic Tee," *IEEE Transactions: Microwave Theory and Technology*, Vol. MTT-24, No. 3, (March 1976).

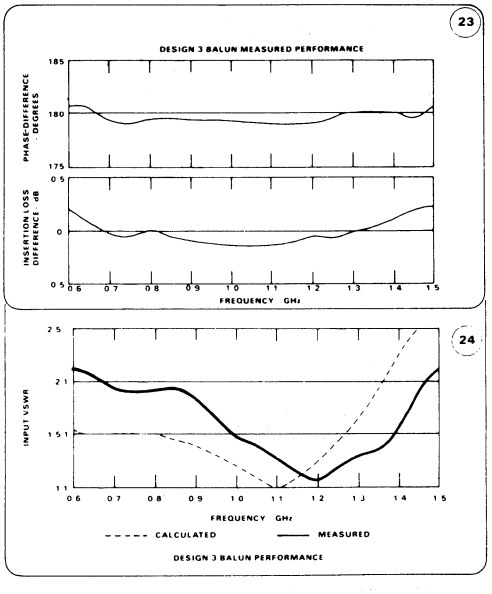
22. The equivalent circuit of the microstrip balun shows it during performance measurements with λ/16 matching lines. The experimental model uses 18-mil glass-Teflon (ϵ_r = 2.55) for the tap circuits and 62.5 mil glass-Teflon for the cavity. Balance properties were measured with a 50-ohm system, which was transformed to 25 ohms by the λ/16 line-section Chebyshev impedance transformers, which have a bandwidth from 0.960 to 1.215 GHz.



The experimental microstrip balun showing the uppermost conductor plane.



23. The unbalance between output ports for a one-octave bandwidth is shown in the measured 1.5-degree maximum phase difference and 0.15-dB maximum insertion loss difference.



24. The central frequency is 10 percent higher than expected, but response is close to the calculated values if relative frequency is considered. If the output transformers and their effect on input VSWR are disregarded, an octave bandwidth with a maximum input VSWR of around 2.0:1 can be obtained. The 100-MHz shift between the two curves may be caused by the improper determination of the folded cavity's electrical length. Similar calculation inaccuracies may arise from effects at the balun junction and from the electrical length of the stub. As in the calculated response, the experimental microstrip balun performs comparably to the two coaxial designs.

25. The similarity in the performance of the three balun designs within the considered frequency bands indicates that the parasitic elements do not significantly affect the theoretical properties. The frequency limit is higher than 1.5 GHz for all three. In the 0.960-to-1.215-GHz bandwidth (TACAN and DME applications), each performed with satisfactory balance. The table compares the main characteristics of the balun designs.

The phase differences (±1.5 degrees) for all three baluns are similar to those experienced with the miniature 3-dB hybrid couplers that are normally used to combine transistors for microwave balanced amplifiers. But the insertion loss differences of the baluns are better—0.2 dB for a one-octave bandwidth compared with 0.5 dB.

The physically simple microstrip balun eliminates the connection problem inherent in coaxial designs: physical variances that breed standing waves and unbalance. Microstripping the transmission lines allows a designer to choose any value of characteristic impedance of the lines. Consequently, the microstrip balun is both more manageable and more controllable.

Since the balun load impedance will vary with frequency, the best results will be obtained by simultaneously optimizing the balun parameters with those of the matching network. The transistor's internal prematching network must be considered.••

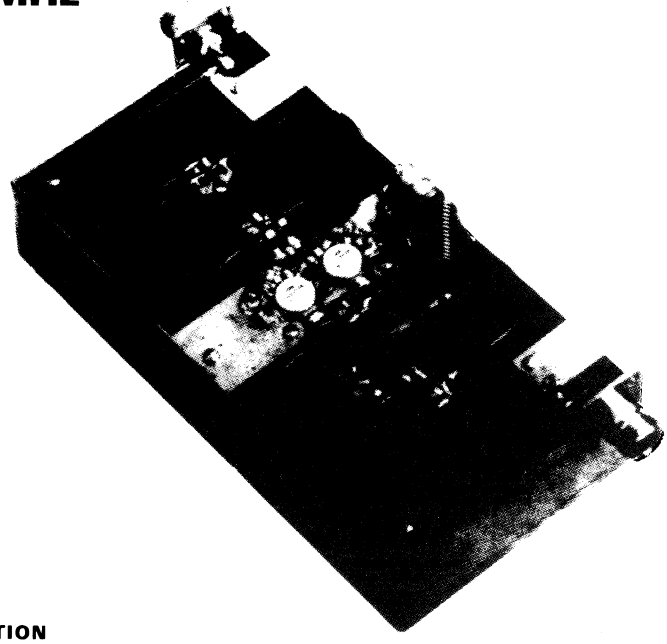
25

Performance of the Three Balun Designs

Type of balun	Balun loads, R (ohms)	Maximum experimental unbalance for one-octave bandwidth		Theoretical input VSWR for:	
		Δφ(°)	ΔMAG (dB)	960-1215 MHz	One-octave bandwidth
Coaxial I (Design 1)	25	3	0.2	1.15:1	1.6:1
Coaxial II (Design 2)	6.25	1	0.2	1.15:1	1.6:1
Microstrip (Design 3)	25	1.5	0.2	1.20:1	1.8:1

AN1037

Solid State Power Amplifier 300 W FM 88-108 MHz



INTRODUCTION

High efficiency multikilowat FM transmitters with full solid state amplifiers are possible today. The power amplifier of these transmitters should be made by multiparalleling of a basic building block amplifier. This building block should have a high output power and a high gain, a good collector efficiency, broad-band (88-108 MHz) frequency response and a simple, reproducible and reliable circuit design. This application note describes an FM building block amplifier that meets the requirements mentioned above and that can be successfully incorporated to a number of amplifier architectures.

The amplifier has been developed with a pair of TP 9383 transistors in push-pull configuration. TP 9383 is a double diffused silicon epitaxial transistor that makes use of gold metallization and diffused ballast resistors for long operationg life and ruggedness. Its basic specifications are :

V_{CC} = 28 V ; η = 75 % at 108 MHz and 150 W output power

G = 9 dB Po = 150 W

DESIGN CONSIDERATIONS

When designing an FM amplifier the total efficiency must be the first goal.

Overall efficiency is the combination of good collect efficiency and high gain. To get a good collector efficiency the transistors must be operated in class C and the load impedance should match the transistors output impedance at the operation power level. Class C amplifiers are non-linear units. The harmonic content of the output signal of this type of amplifiers can be very high and their power wasted with an important reduction in the efficiency.

This fact made **advantageous** the use of balanced amplifiers. In such circuit arrangement all the even harmonic are largely suppressed and the waste of power minimized. Push-pull amplifiers have also the additional advantages of connecting in series for RF operation the input and output impedance of the 2 transistors. That makes considerably easier to match the input and output impedances of the transistor pair. However, as the impedance transformation is lower, the RF power losses are smaller and the gain and efficiency higher.

Another important consideration in the design of an FM amplifier is the ruggedness of the amplifier. FM transmitters are often operated 24 hours per day and sometimes remotly controlled and in difficult access sites. The operating point of the transistors should be chosen in a conservative way and the heat properly evacuated. A thermo switch should be incorporated to the system. The amplifier must also be able to withstand output VSWR. Although all transmitters use to incorporate VSWR protection in their interlocky systems, the amplifier must be designed with the capability of supporting VSWR of 3.1 as a minimum. This point can be very determinent when considering that on a high efficiency circuit the collector voltage swing can be close to 3 times the collector supply voltage.

CIRCUIT DESCRIPTION

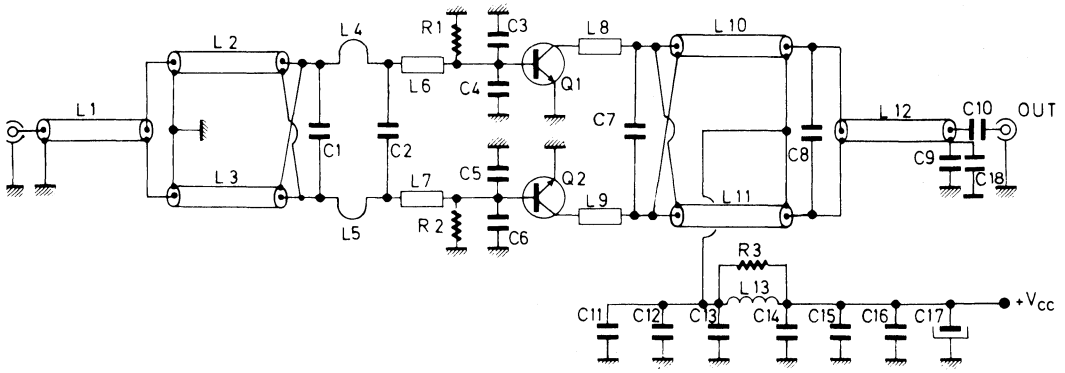
Circuit schematic is given in the Figure 1. At the amplifier input there is a two section balun. The first section, L_1, consists of a short lenght ($\simeq \lambda/20$) of 50 Ω coaxial semirigid cable. The outer conductor of the coaxial cable is grounded at the input side and floats at the output.

The second section of the balun consists of two identical coaxial cables, L_2 and L_3, of the same length that L_1 but with 25 Ω characteristic impedance. The ends of these two coaxials are interconnected in series at the input side (thus offering 50 Ω impedance to L_1) and in parallel at the output of the section.

The combined balanced impedance will be therefore 12.5 Ω at the output of the balun. The input impedance of the transistor pair Q_1 and Q_2 is transformed to 12.5 Ω (2 × 6.25) with the LC network represented in the schematic.

If this balun is well charged by 2 × 6.25 Ω it is well capable of multioctave operation. However in this case the LC network that transform the impedances of the transistor pair has been optimized only between 88 and 108 MHz.

A similar balun circuit is used at the output of the amplifier. The main difference with the input balun is that the coaxial cables are also used in the collect biasing circuit. Care has been taken with the decoupling of the collect bias in order to avoid low frequency oscillations. The collect impedance is higher than the base impedance and therefore the LC output transforming network is very simple, only L_8, L_9 and C_7.



88-108 MHz; 300 W 28 V

Figure 1. FM Broadband Power Amplifier

COMPONENTS LIST

C_1	= 120 + 80 pF Chip capacitor ATC 100 B
C_2	= 220 pF Chip capacitor ATC 100 B
C_3, C_4, C_5, C_6	= 470 pF Chip capacitor ATC 100 B
C_7	= 100 pF Chip capacitor ATC 100 B
C_8	= 27 pF Chip capacitor ATC 100 B
C_9, C_{10}, C_{11}, C_{14}	= 1 000 pF Disc capacitor
C_{12}, C_{15}	= 10 nF
C_{13}, C_{16}, C_{18}	= 0,1 µF
C_{17}	= 1 000 µF/63 V Electrolytic

L_1	= 50 Ω coaxial cable ⌀ 3,2 mm (Teflon) L = 110 mm
L_2, L_3	= 25 Ω coaxial cable ⌀ 3,2 mm (Teflon) L = 110 mm
L_4, L_5	= Hair pin : copper foil 18 × 3 mm 0,3 mm thickness
L_6, L_7	= Line on substrate : 15 × 5 mm
L_8, L_9	= Line on substrate : 10 × 5 mm
L_{10}, L_{11}	= 25 Ω coaxial cable ⌀ 5 mm (Teflon) L = 110 mm
L_{12}	= 50 Ω coaxial cable ⌀ 5 mm (Teflon) L = 110 mm
L_{13}	= 15 turns ⌀ 8 mm 1,4 mm wire

R_1, R_2	= 22 Ω 1/2 W
R_3	= 47 Ω 2 W

Q_1, Q_2	= TP 9383

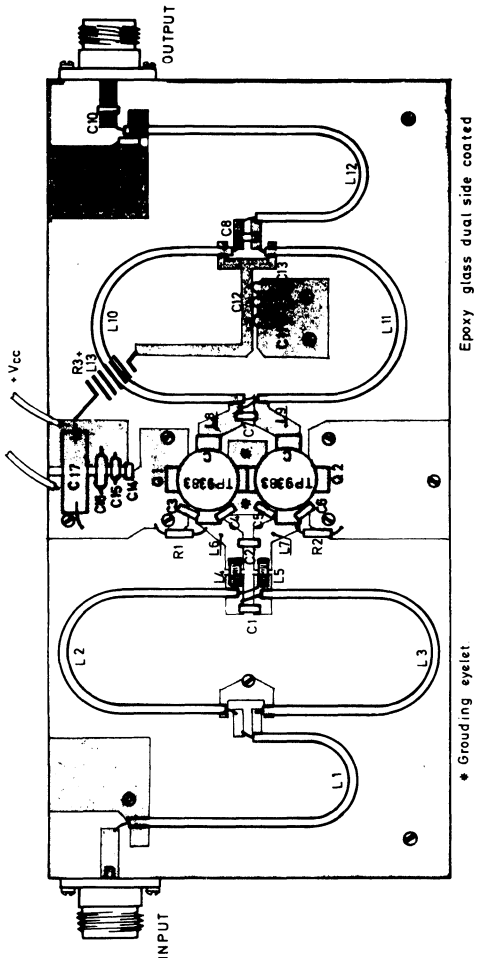


Figure 2. Component Layout

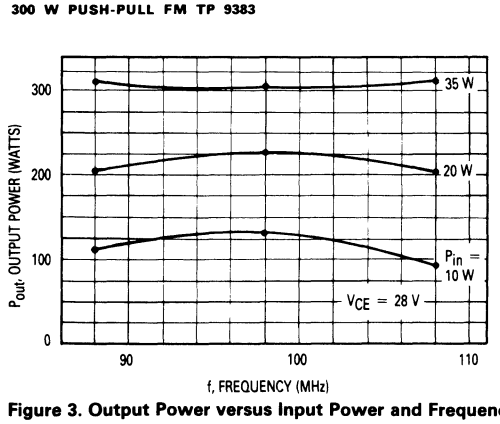


Figure 3. Output Power versus Input Power and Frequency

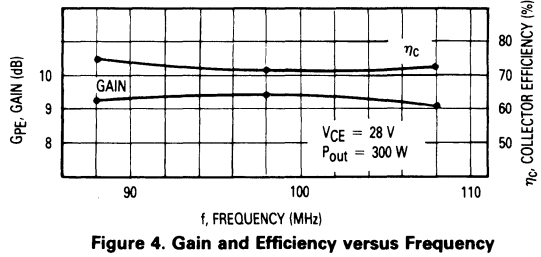
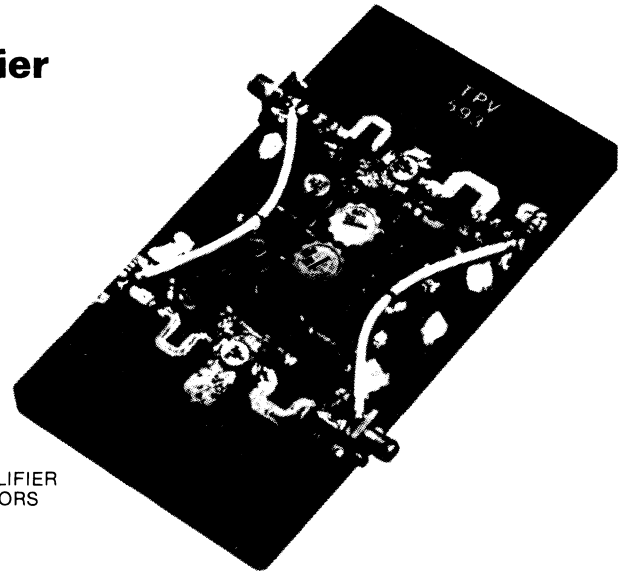


Figure 4. Gain and Efficiency versus Frequency

AN1039

470-860 MHz Broadband Amplifier 5 W



5 W UHF TV TRANSPOSER AMPLIFIER
WITH TWO TPV 593 TRANSISTORS

INTRODUCTION

This application note describes an ultralinear broadband (470-860 MHz) amplifier, developed for TV transposer applications. The amplifier incorporates two TPV 593 transistors.

Each transistor is used to build a separate broadband amplifier. The two identical amplifiers are later combined with 3 dB hybrids.

The TPV 593 transistor has been developed for TV class A application. It incorporates gold metallization and diffused ballast resistors for ruggedness and linearity. Its DC current consumption is very low and makes it a good candidate for solar cell powered systems. Its basic specifications are :

V_{CC} = 25 V I_C = 450 mA

G = 9 dB at 860 MHz

IMD = — 60 dB at 860 MHz and 2 W output

The S parameters of the TPV 593 are given in the table below.

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN	ANGL)	S21 (MAGN	ANGL)	S12 (MAGN	ANGL)	S22 (MAGN	ANGL)	S21 dB	K FACT
470.00	0.93	170	1.50	63.0	0.040	50.0	0.55	— 166	3.52	1.01
650.00	0.93	165	1.06	50.0	0.050	54.0	0.60	— 169	0.51	1.04
860.00	0.92	162	0.79	38.0	0.056	54.0	0.65	— 169	— 2.00	1.15

POLAR COORDINATES OF SIMULTANEOUS CONJUGATE MATCH

F MHz	SOURCE REFL. COEFF. MAGN.	ANGLE	LOAD REFL. COEFF. MAGN.	ANGLE	Gmax dB
470.0	0.99	— 173	0.91	124	15.23
650.0	0.97	— 168	0.83	134	12.01
860.0	0.95	— 165	0.79	146	9.16

DESIGN CONSIDERATIONS

Two identical single transistor class A amplifiers will be combined with 3 dB couplers. First the design of a single amplifier will be considered.

From the analysis of the variation of the TPV 593 S21 parameter with the frequency it may be seen that there is a difference of 5.52 dB between 470 and 860 MHz. If a flat gain is required this gain slope has to be compensated. The compensation can be implemented in two ways :

a) By placing a selective attenuator at the input of the transistor amplifier, with an insertion loss minimum at 860 MHz and which increases to 5.52 dB at 470 MHz. The insertion loss increase should compensate the transistor gain slope.

b) By selective mismatch at the input of the transistor. The input circuit will provide impedance matching at 860 MHz, in order to get a gain as close as possible to the GA max. Frequency dependent mismatch will compensate the gain slope. At 470 MHz a VSWR as high as 11:1 will be necessary. It has been proved that impedance mismatch at the base terminal of a transistor power amplifier does not modify the linearity behavior of the device.

As it was decided to combine two amplifiers with 3 dB couplers the method b) was selected. 50 ohms 3 dB hybrid couplers when used with two identical loads provide a good VSWR at the common terminal even if the loads differ from 50 ohms. The reflected energy is dissipated as the 50 ohms load connected to the fourth terminal of the coupler. The coupler behaves as a selective attenuator. Figure 1 shows the amplifier arrangement. The use of a 3 dB coupler to split the input signal makes almost compulsory the use of the same type of circuit at the output.

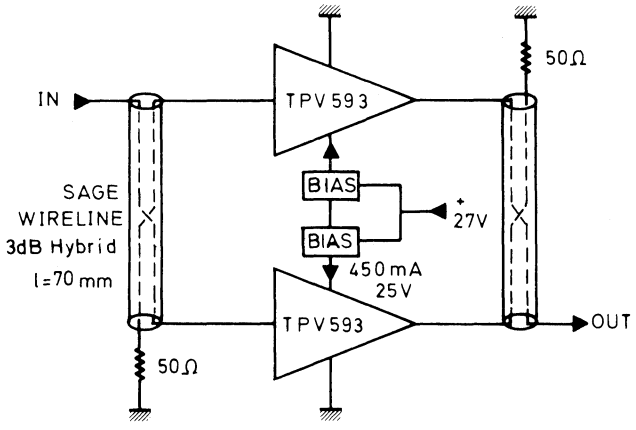


Figure 1. Block Diagram of Amplifier

The amplifier must be as linear as possible over the complete UHF band. A transistor power amplifier usually requires impedance matching at the collector side for optimum intermodulation. Therefore the output circuitry has been designed for impedance matching all over the bands IV and V.

COMPONENTS PART LIST

L_1 = 65 line 11 % g at 860 MHz
L_2 = 50 line 1.5 % g at 860 MHz
L_3 = 50 line 17 % g at 860 MHz
L_4 = 7 turns ID 2 mm - Closely Wound - wire 5 mm
L_5 = $\overleftarrow{10\ mm}$: 5 mm wire 1 mm

C_1-C_5 = Variable Airtronic AT 7275, .8-4.5 pF
C_2 = 6.8 pF ATC 100A
C_3-C_4 = 10 pF ATC 100A
C_6-C_7 = 1 nF + 10 nF + 1μ + 10 μF

Board Material: 1/16" Teflon Fiberglass

CIRCUIT DESCRIPTION

The circuit of a simple amplifier is given in Figure 2.

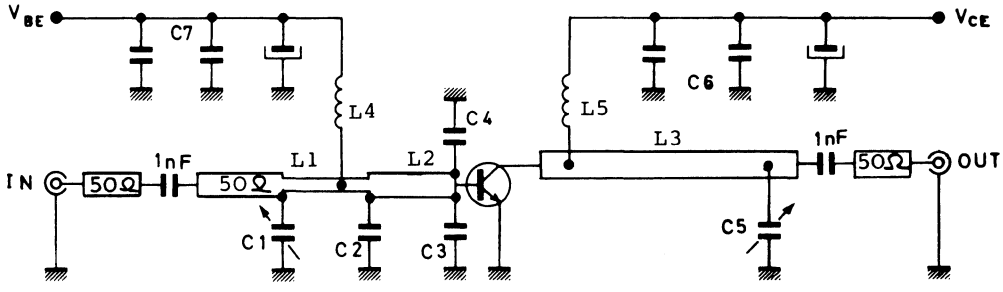


Figure 2. Circuit Schematic

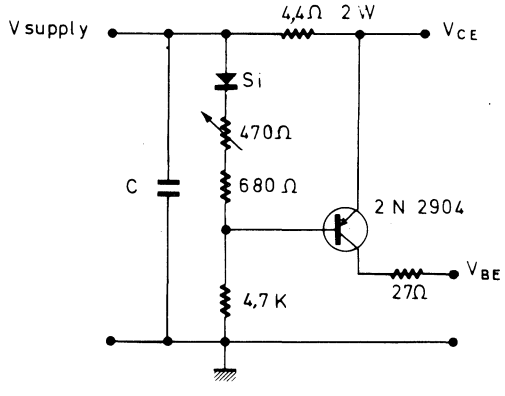


Figure 3. Class A Bias Circuit

The input circuit consist of a three section low pass type matching network. To minimize power losses all the impedance transformations are made at a low Q level. Variable capacitor C_1 is adjusted for optimum VSWR at 860 MHz. The tuning is straight forward and only a small retouch is necessary after the collector tuning.

The very constant S22 of the TPV 593 transistor makes extremely simple to match the collector to a 50 ohms load. L_8 tunes the output capacitance of the device and is determined for good matching at the low end of the band. Only one low pass section is necessary. Capacitor C_5, variable, allows a good shaping of the output VSWR. Collector tuning should be done after tuning the input.

The bias control circuitry is classical and is given in Figure 3.

CONSTRUCTIONAL DETAILS

The printed circuit board lay-out of the complete amplifier is given in Figure 4. Considerate attention should be paid to the ground returns. Plated through holes have been used to ensure low emitter inductance. Wrapped foils ensure proper grounding of parallel capacitors and connectors.

The couplers have been made with parallel wire cable.

This solution is as inexpensive as a straight forward.

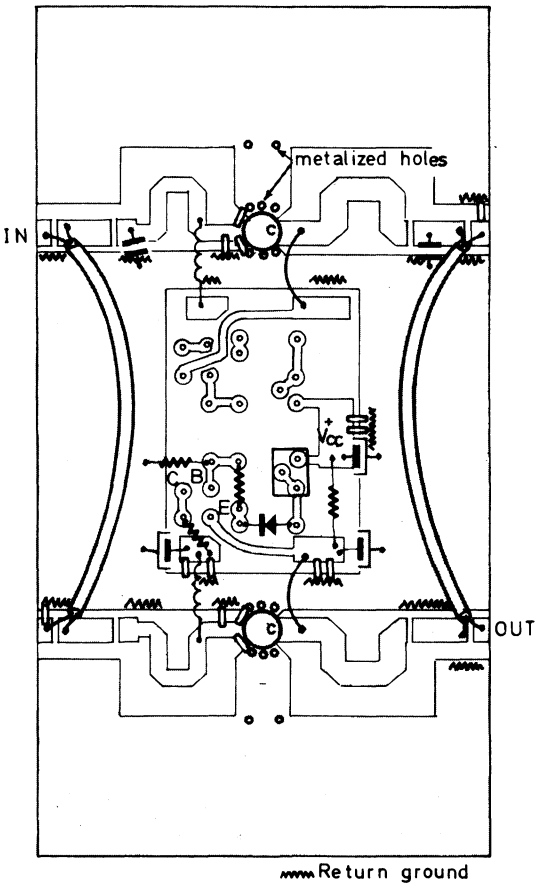


Figure 4. Printed Circuit Board Layout

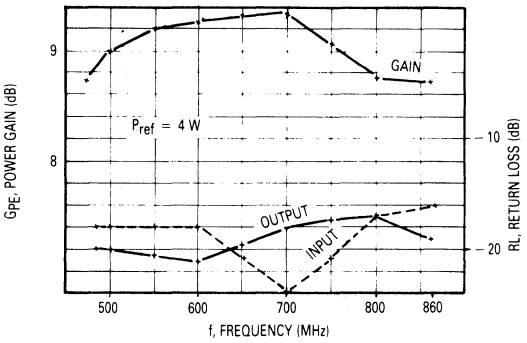


Figure 5. Gain and Return Loss versus Frequency

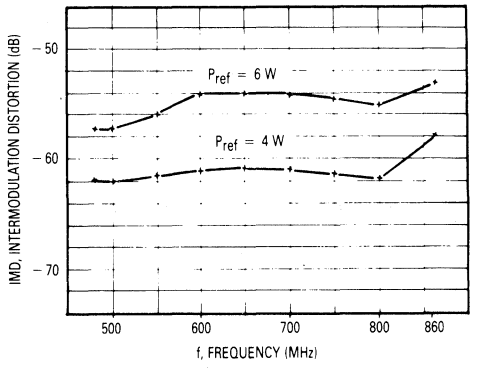
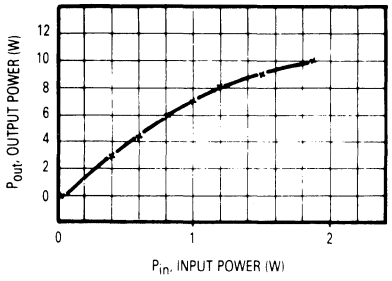
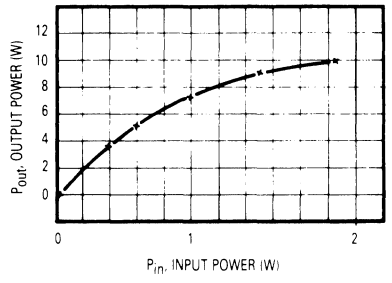


Figure 6. Intermodulation Distortion versus Frequency

Figure 7. Output Power versus Input Power





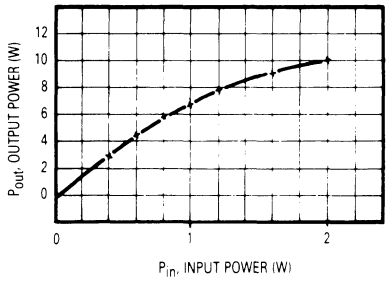
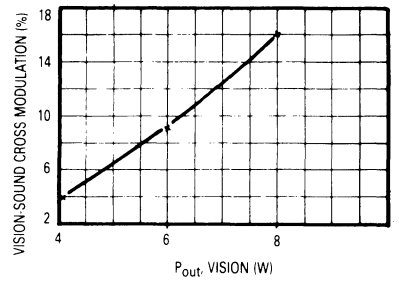
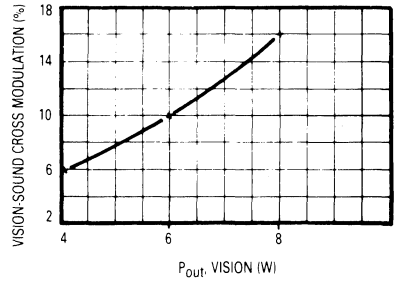


Figure 8. Vision to Sound Cross Modulation

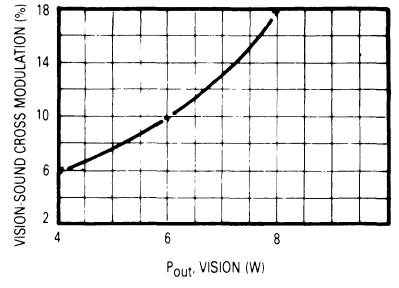
f = 470 MHz



f = 650 MHz



f = 860 MHz



NOTE: Δ% of sound carrier (−7 dB) when vision carrier is switch ON/OFF

MEASUREMENTS

The measurements results have been summarized in Table 2.

Figure 5 shows the frequency response of the amplifier as well as the input and output match. Figure 6 displays the linearity (IMD test; −8, −16, −7 dB) of the amplifier. Static transfer curves are given in the Figures 7 and 8 that show also the vision to sound cross modulation of the amplifier.

Table 2

TYPICAL RESULTS

BANDWIDTH	: 470 - 860 MHz	IMD : SOUND	= REF. - 7 dB
GAIN	: 8.7 dB min	VISION	REF. 8 dB
IMD* at - 4 W	: - 58 dB	SIDEBAND	REF. - 16 dB
- 5 W	: 56 dB		
INPUT RETURN LOSS	: 16 dB		
OUTPUT RETURN LOSS	: 17 dB		
BIAS CONDITIONS	: V_{cc} 25 V ; I_c 2 x 450 mA		

CONCLUSION

A high performance amplifier has been described as an example of the possibilities offered to the designer by the TPV 593. In particular the amplifier combines excellent frequency response and linearity with high efficient use of the DC power. This circuit may be of interest for output stages of low power TV transposers or drivers of higher power units.

AN1040

Mounting Considerations for Power Semiconductors

Prepared by Bill Roehr
Staff Consultant, Motorola Semiconductor Sector

TABLE OF CONTENTS

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic-packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 1 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4" hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

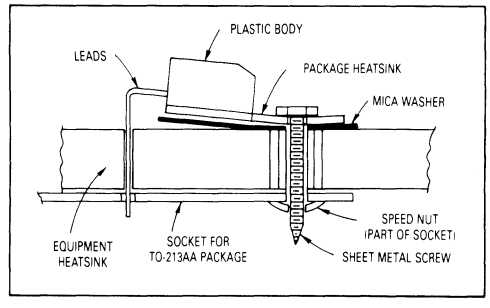


Figure 1. Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)

(1) MIL-HANDBOOK — 2178, SECTION 2.2.
(2) "Navy Power Supply Reliability — Design and Manufacturing Guidelines" NAVMAT P4855-1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Stud Mount
Flange Mount
Pressfit
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e, $\Delta h/TIR$, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO-204 (TO-3) package with a typical 32-microinch finish, showed that heatsink finishes between 16 and 64 μ-in caused less than $\pm 2.5\%$ difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.[3] Most commercially available cast or extruded heatsinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

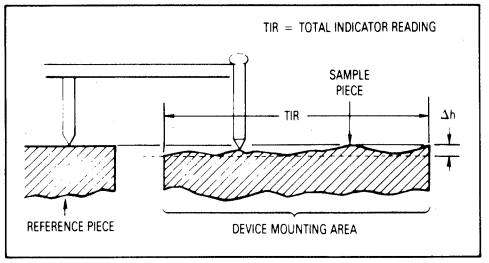


Figure 2. Surface Flatness Measurement

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

(3) Catalog #87-HS-9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock-marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 3. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON-DUX. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes

Table 1
Approximate Values for Interface Thermal Resistance Data from Measurements Performed in Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
JEDEC Outlines	Description	Test Torque In-Lb	Metal-to-Metal		With Insulator			See Note
			Dry	Lubed	Dry	Lubed	Type	
DO-203AA, TO-210AA TO-208AB	10-32 Stud 7/16" Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO-203AB, TO-210AC TO-208	1/4-28 Stud 11/16" Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-208AA	Pressfit, 1/2"	—	0.15	0.1	—	—	—	
TO-204AA (TO-3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-213AA (TO-66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO-126	Thermopad 1/4" x 3/8"	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO-220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 3 and 4 for additional data on TO-3 and TO-220 packages.
2. Screw not insulated. See Figure 12.

formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

INSULATION CONSIDERATIONS

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, are shown in Figure 3, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 3, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By

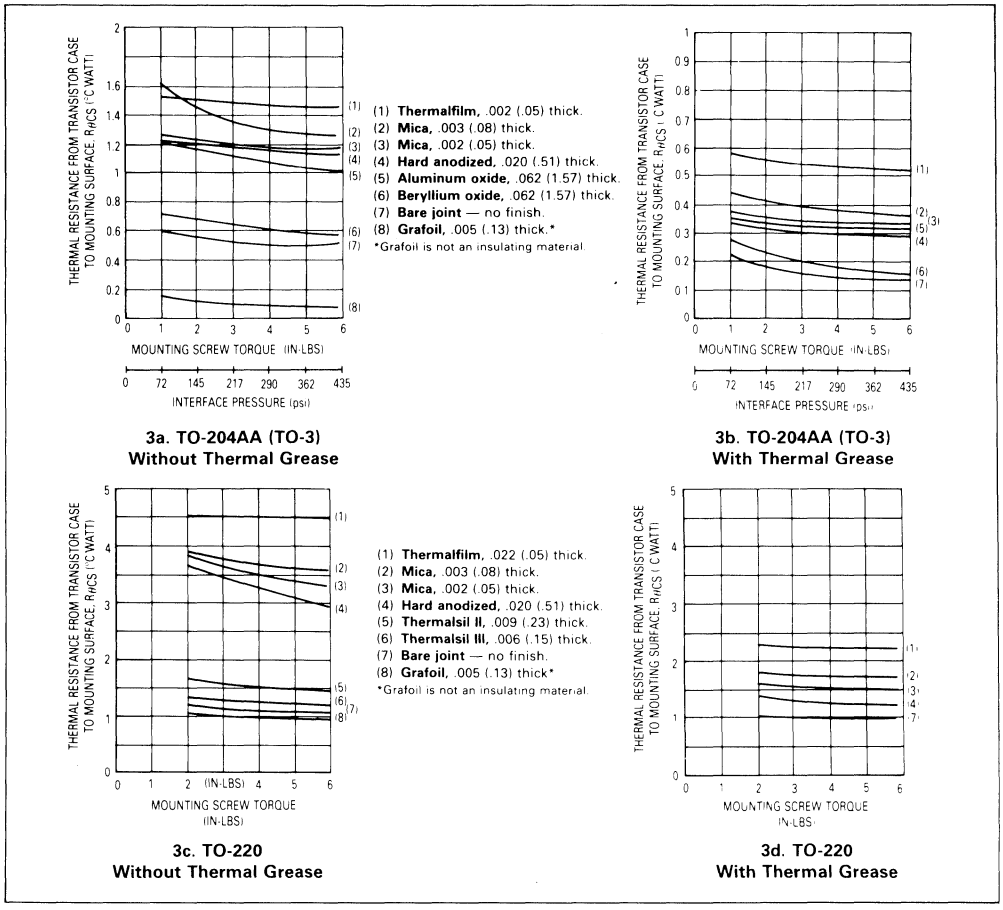


Figure 3. Interface Thermal Resistance for TO-204, TO-3 and TO-220 Packages using Different Insulating Materials as a Function of Mounting Screw Torque (Data Courtesy Thermalloy)

comparing Figures 3c and 3d, it can be noted that Thermasil, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO-220 package.

A number of manufacturers offer silicone rubber insulators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called

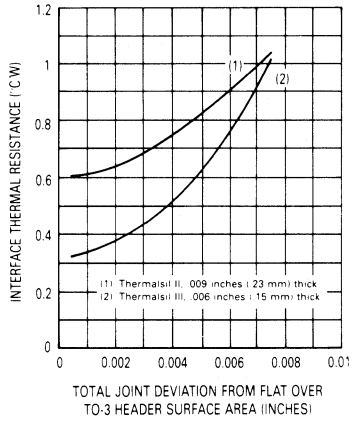
Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173-7	.790	1.175
Bergquist	Sil Pad K-4	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad 400-9	.735	1.205
Thermalloy	Thermalsil II	.680	1.045
Shin-Etsu	TC-30AG	.664	1.260
Bergquist	Sil Pad 400-7	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174-9	.574	.755
Bergquist	Sil Pad 1000	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermalsil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86-1010.

Rubber-Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown on Figure 4. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



Data courtesy of Thermalloy

Figure 4. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho-Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With non-conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The EMS (Energy Management Series) Modules, shown on Figure 8, Case 806 (ICePAK) and Case 388A (TO-258AA) (see Figure 11) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The Full Pak,

Table 3. Performance of Silicon Rubber Insulators Tested per MIL-I-49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Berquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho-Therm, 1617	0.233	—
Q Pad (non-insulated)	—	0.009
Sil-Pad, K-10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil-Pad 1000	0.400	0.300
Cho-therm 1674	0.433	—
Thermasil II	0.500	—
Sil-Pad 400	0.533	0.440
Sil-Pad K-4	0.583	0.440

(1) From Thermalloy EIR 87-1030
(2) From Berquist Data Sheet

Case 221C, illustrated in Figure 13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6-32 machine screw.(4)

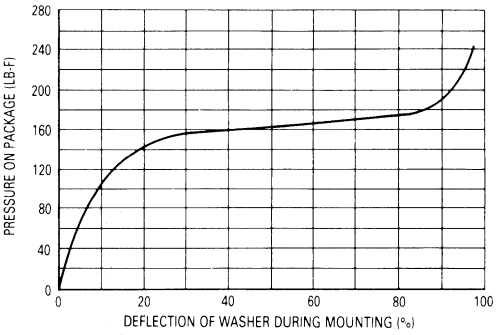


Figure 5. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board-mounted or free-standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync-nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self-Tapping Screws

Under carefully controlled conditions, sheet-metal screws are acceptable. However, during the tapping-process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed-nut. If a self tapping process is desired, the screw type must be used which roll-forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt-

furnace, irons, vapor-phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.(5) Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field-serviceable systems or low strength types for field-serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Stud Mount

Parts which fall into the stud-mount classification are shown in Figure 6. Mounting errors with non-insulated stud-mounted parts are generally confined to application

(5) Robert Batson, Elliot Fraunglass and James P. Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83. Conference, February 1–3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

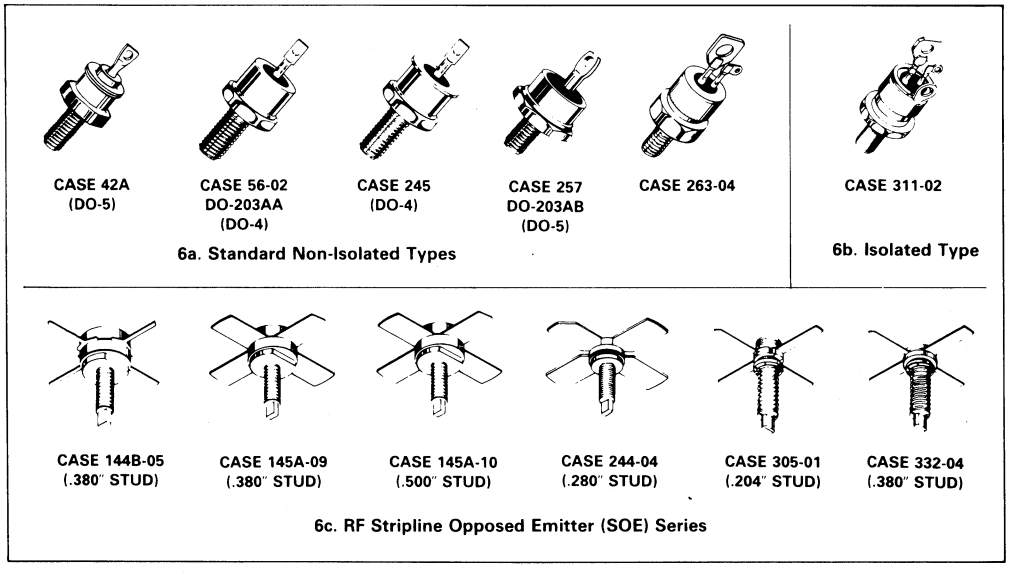


Figure 6. A Variety of Stud-Mount Parts

of excessive torque or tapping the stud into a threaded heatsink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer; the details are shown in Figure 7.

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non-insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a berrylium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

R.F. transistors in the stud-mount stripline opposed emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic — metal interface are discussed in the section entitled "Connecting and Handling Terminals."

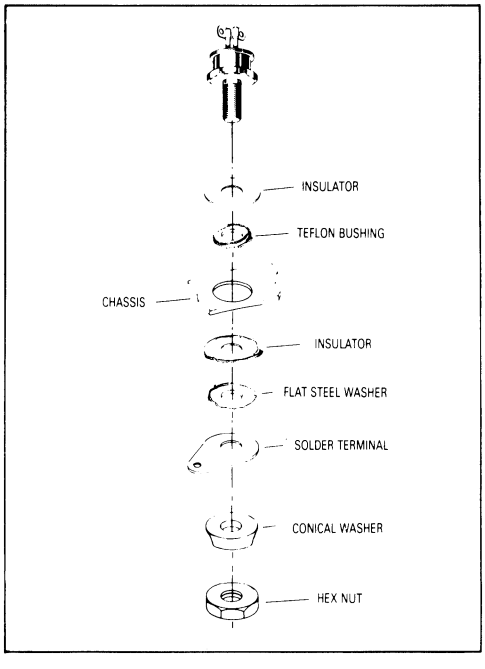
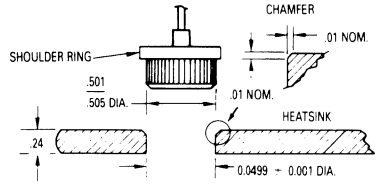


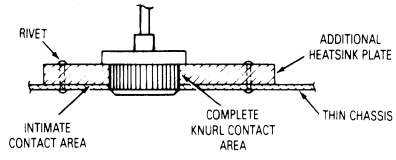
Figure 7. Isolating Hardware Used for a Non-Isolated Stud-Mount Package

Press Fit

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 8. A special fixture meeting the necessary requirements must be used.



Heat Sink Mounting



Thin-Chassis Mounting

The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper-less than 50 on the Rockwell F scale; aluminum-less than 65 on the Brinell scale. A heatsink as thin as 1 8" may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

Figure 8. Press-Fit Package

Flange Mount

A large variety of parts fit into the flange mount category as shown in Figure 9. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO-204 (TO-3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger-tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 10. Machine screws (preferred) self-tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section. "Fastener and Hardware Characteristics."

The copper flange of the Energy Management Series (EMS) Modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No

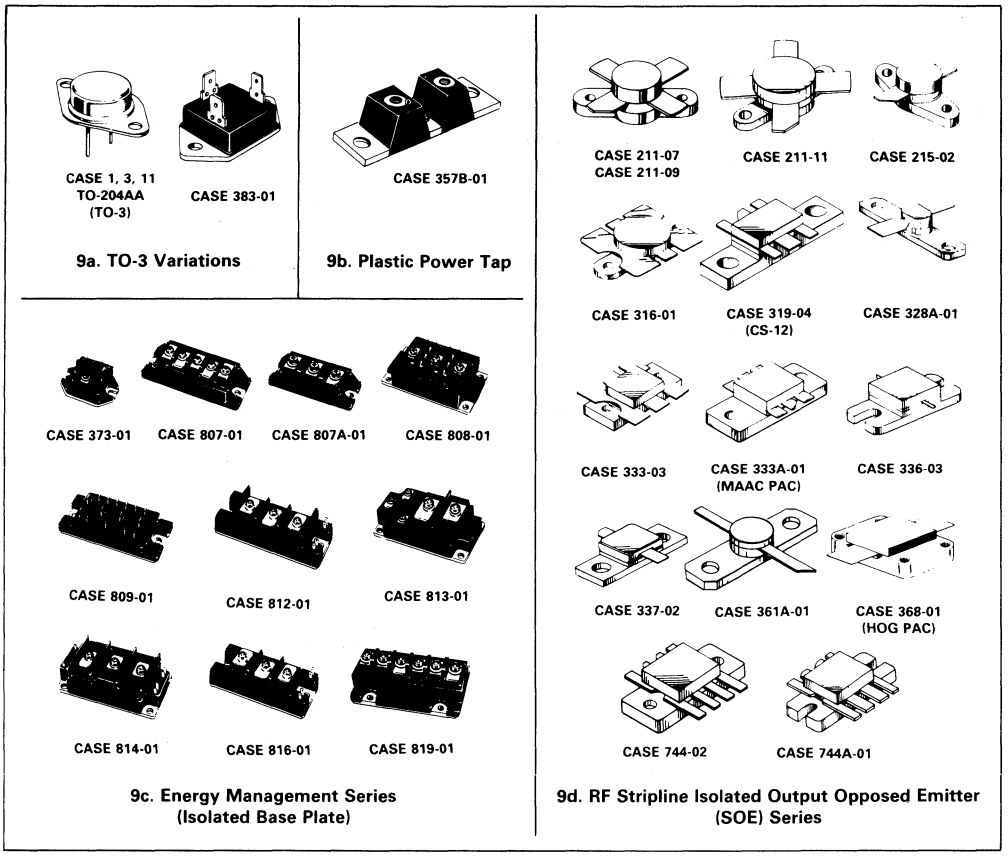


Figure 9. A Large Array of Parts Fit into the Flange-Mount Classification

special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, Figure 9b, final torque should be applied first to the center position.

The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in EB107 "Mounting Considerations for Motorola RF Power Modules." Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area Case 368-1 (HOG PAC) will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4–40 mounting screws is 5 in/lbs. Spring and flat washers are recommended. Over torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length, instead it bends upwards in the mid-section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center

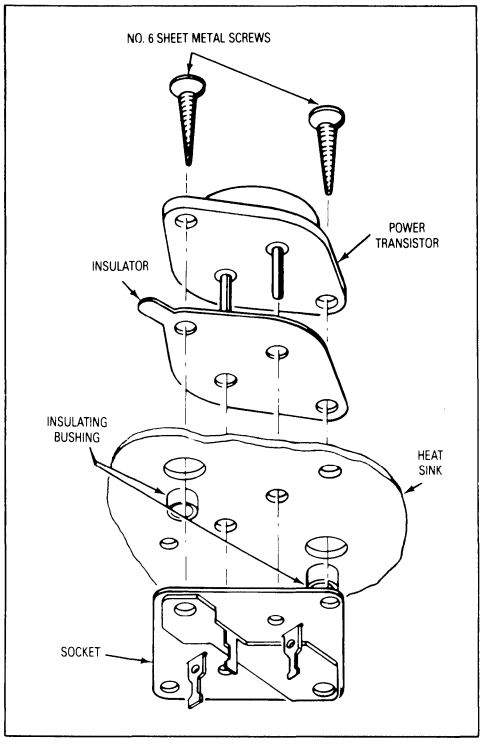


Figure 10. Hardware Used for a TO-204AA (TO-3) Flange Mount Part

of the flange, deforming it. Deformations of 2–3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 11. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 12. The rectangular washer shown in Figure 12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO-220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

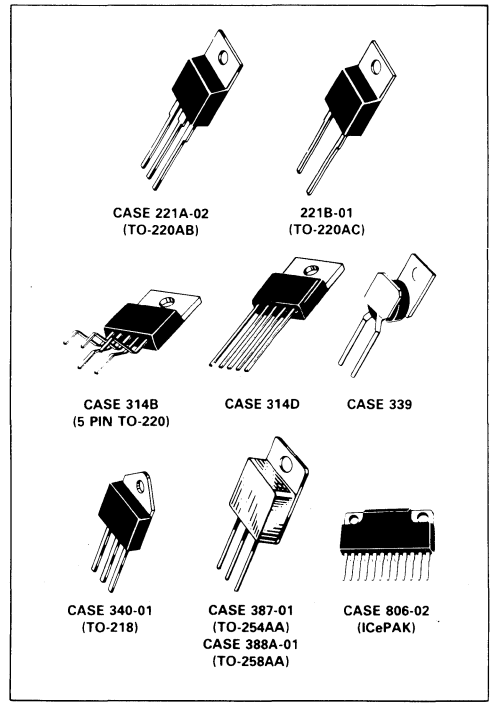


Figure 11. Several Types of Tab-Mount Parts

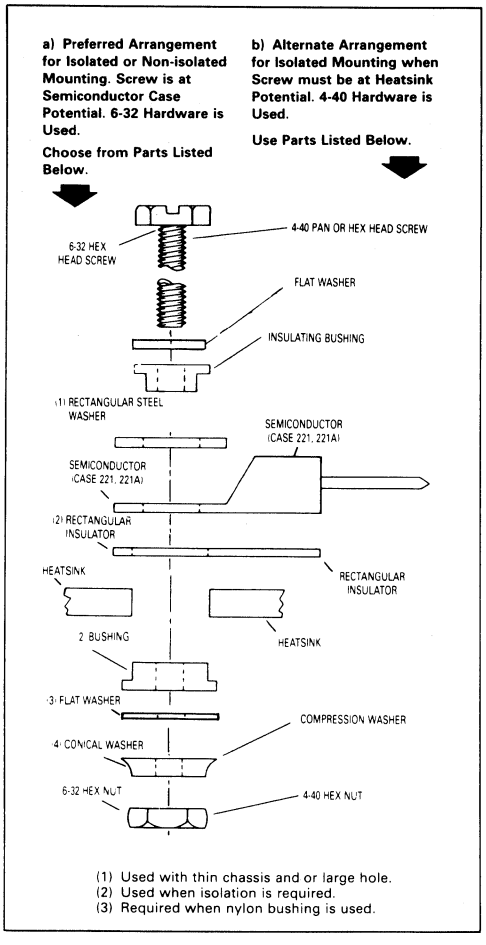


Figure 12. Mounting Arrangements for Tab Mount TO-220

the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 15c. To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806-02) is basically an elongated TO-220 package with isolated chips. The mounting precautions for the TO-220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

Plastic Body Mount

The Thermopad and Full Pak plastic power packages shown in Figure 13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The Full Pak (Case 221C-01) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5.

Figure 14 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The Full Pak, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 15c, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 15b may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 15a.

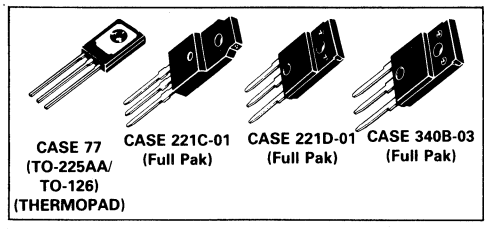
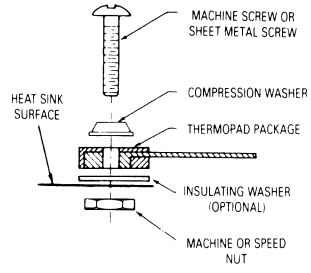
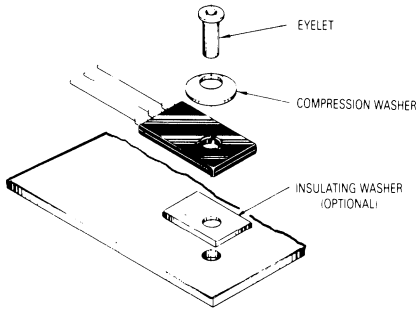


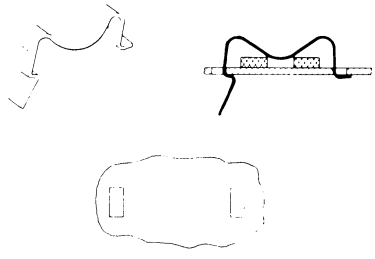
Figure 13. Plastic Body-Mount Packages



14a. Machine Screw Mounting

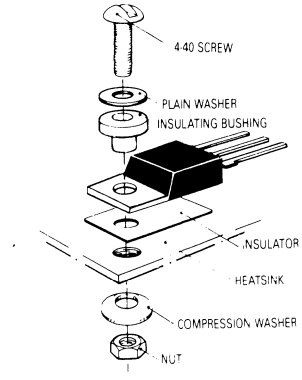


14b. Eyelet Mounting

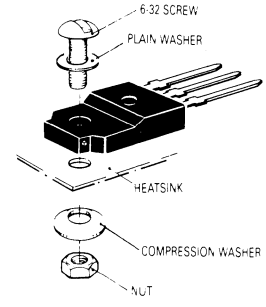


14c. Clips

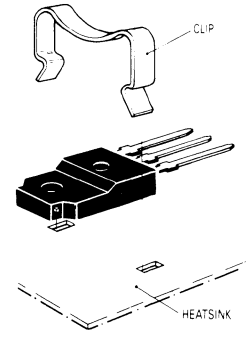
Figure 14. Recommended Mounting Arrangements for TO-225AA (TO-126) Thermopad Packages



15a. Screw-Mounted TO-220



15b. Screw-Mounted Full Pak



15c. Clip-Mounted Full Pak

Figure 15. Mounting Arrangements for the Full Pak as Compared to a Conventional TO-220

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 16, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resis-

tance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 17 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.(7) The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

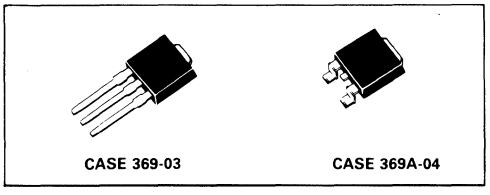


Figure 16. Surface Mount D-PAK Parts

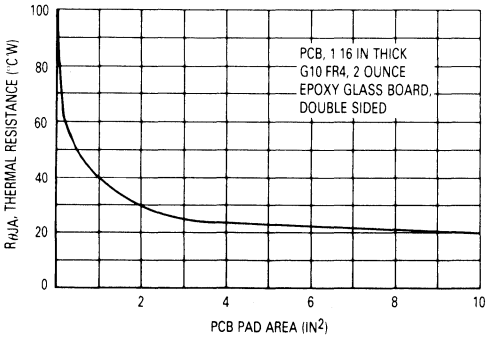
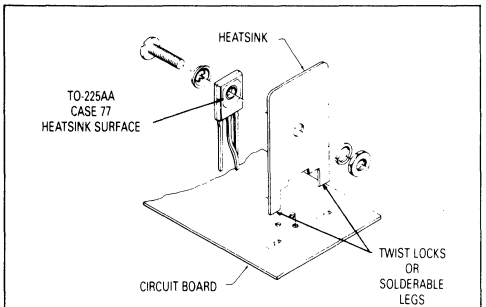


Figure 17. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass-Epoxy Board

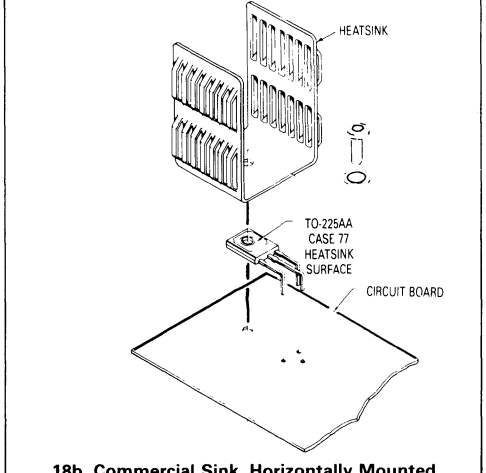
FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the CASE 77 (TO-225AA) (TO-127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 18. The arrangement of part (a) could be used with any plastic package, but the scheme of part (18b) is more practical



18a. Simple Plate, Vertically Mounted



18b. Commercial Sink, Horizontally Mounted

Figure 18. Methods of Using Small Heatsinks With Plastic Semiconductor Packages

(7) Herb Fick, "Thermal Management of Surface Mount Power Devices," Powerconversion and Intelligent Motion, August 1987.

with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

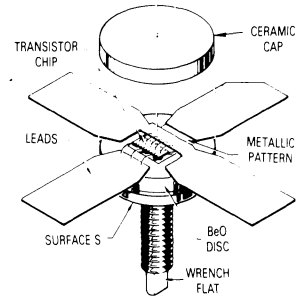
The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

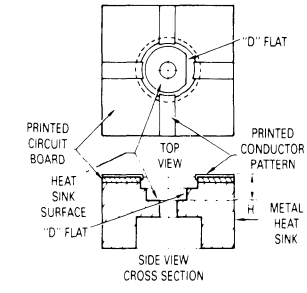
The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO-225AA (CASE 77) and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

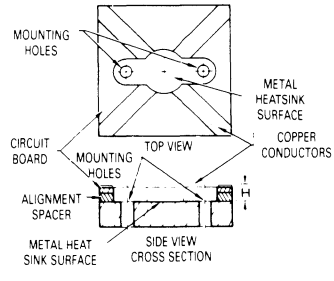
The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be



19a. Component Parts of a Stud Mount Stripline Package. Flange Mounted Packages are Similarly Constructed



19b. Typical Stud Type SOE Transistor Mounting Method



19c. Flange Type SOE Transistor Mounting Method

Figure 19. Mounting Details for SOE Transistors

exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 19. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic-to-metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 19b shows a cross-section of a printed circuit board and heatsink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D-flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud — BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead-soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger, this may result in device failure as power is applied.

Figure 19c shows a typical mounting technique for flange-type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where
T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instanta-

neous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
P_D = power dissipation
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heatsink),
$R_{\theta SA}$ = heatsink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal-resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

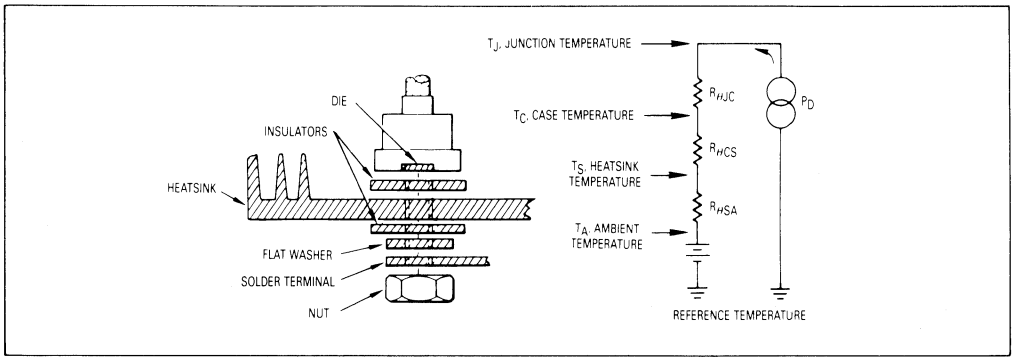


Figure A1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO-220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

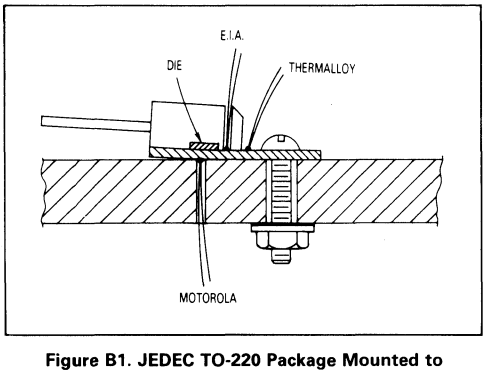


Figure B1. JEDEC TO-220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C
Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber	
Aavid Eng.	X	X	—	—	—	—	—	X	X
AHAM-TOR	—	—	—	—	—	—	—	—	X
Astrodynamis	X	—	—	—	—	—	—	—	X
Delbert Blinn	—	—	X	—	X	X	X	X	X
IERC	X	—	—	—	—	—	—	—	X
Staver	—	—	—	—	—	—	—	—	X
Thermalloy	X	X	X	X	X	X	X	X	X
Tran-tec	—	—	X	X	X	X	—	X	X
Wakefield Eng.	X	X	X	—	X	—	—	X	X

Other sources for silicone rubber pads: Chomerics, Berquist

Suppliers Addresses

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM-TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935-4944

Berquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835-2322

Chomerics, Inc., 16 Flagstone Drive, Hudson, New Hampshire 03051 1-800-633-8800

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 629-3900

International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481

The Staver Company, Inc., 41-51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

PACKAGE INDEX

PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non-related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package designations were re-registered to the new system as time permitted.

For example the venerable TO-3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO-204 family. The TO-204AA conforms to the original outline for the TO-3 having 40 mil pins while the TO-204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the DO-4, DO-5 and TO-3 still convey sufficient meaning for general verbal communication.

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
001	TO-3	TO-204AA		Flange	9
003	TO-3		2	Flange	9
009	TO-61	TO-210AC		Stud	8
011	TO-3	TO-204AA	—	Flange	9
011A	TO-3	—	2	Flange	9
012	TO-3	—	2	Flange	9
036	TO-60	TO-210AB	—	Stud	8
042A	DO-5	DO-203AB	—	Stud	8
044	DO-4	DO-203AA	—	Stud	8
054	TO-3	—	2	Flange	9
056	DO-4	—	—	Stud	8
058	DO-5	—	2	Stud	8
61-03				Flange	9
63-02	TO-64	TO-208AB		Stud	8
63-03	TO-64	TO-208AB		Stud	8
077	TO-126	TO-225AA	—	Plastic	12
080	TO-66	TO-213AA	—	Flange	9
086	—	TO-208	1	Stud	8
086L	—	TO-298	1	Stud	8
144B-05				Stud	8
145A-09				Stud	8
145A-10				Stud	8
145C	TO-232		1	Stud	8
157	—	DO-203	1	Stud	8
160-03	TO-59	TO-210AA	—	Stud	8
167	—	DO-203	1	Stud	8
174-04				Pressfit	9
175-03				Stud	8
197	—	TO-204AE	—	Flange	9
211-07				Flange	9
211-09				Flange	9

Notes: 1. Would fit within this family outline if registered with JEDEC.
2. Not within all JEDEC dimensions.

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
211-11				Flange	9
215-02				Flange	9
221	—	TO-220AB	—	Tab	11
221C-02				Plastic	12
221D-01	—	—	Isolated TO-220	Plastic	12
235	—	TO-208	1	Stud	8
235-03				Stud	8
238	—	TO-208	1	Stud	8
239	—	TO-208	—	Stud	8
244-04				Stud	8
245	DO-4	—	—	Stud	8
257-01	DO-5	—	—	Stud	8
263	—	TO-208	—	Stud	8
263-04				Stud	8
283	DO-4	—	—	Stud	8
289	—	TO-209	1	Stud	8
305-01				Stud	8
310-02				Pressfit	9
311-01			Isolated	Stud	8
311-02				Pressfit	9
311-02				Stud	8
314B-01				Tab	11
314D-01				Tab	11
316-01				Flange	9
319-04				Flange	9
328A-01				Flange	9
332-04				Stud	8
333-03				Flange	9
333A-01				Flange	9
336-03				Flange	9

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
337-02				Flange	9
340		TO-218AC		Tab	11
340A-02				Plastic	12
340B-03			Isolated TO-218	Plastic	12
342-01				Flange	9
357B-01				Flange	9
361-01				Flange	9
368-01				Flange	9
369-03		TO-251		Insertion	14
369A-04		TO-252		Surface	13
373-01			Isolated	Flange	9
383-01			Isolated	Flange	10
387-01		TO-254AA	Isolated 2	Tab	11
388A-01		TO-258AA	Isolated 2	Tab	11
744-02				Flange	9
744A-01				Flange	9
806-02			Isolated	Flange	9
807-01			Isolated	Flange	9
807-02			Isolated	Flange	9
807A-01			Isolated	Flange	9
808-01			Isolated	Flange	9
809-01			Isolated	Flange	9
812-01			Isolated	Flange	9
813-01			Isolated	Flange	9
814-01			Isolated	Flange	9
814A-01			Isolated	Flange	9
084B-01			Isolated	Flange	9
816-01			Isolated	Flange	9
819-01			Isolated	Flange	9
043-02	DO-21	DO-208AA		Pressfit	9

AN1041

Mounting Procedures for Very High Power RF Transistors

Prepared by
Helge O. Granberg
RF Engineering
Advanced Products Group

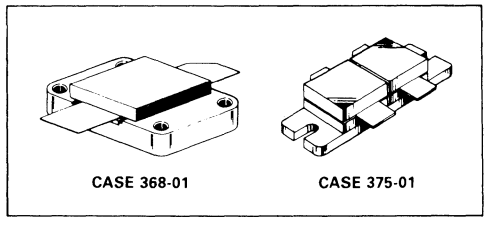
RF power semiconductors such as MRF153, MRF154, MRF155, MRF156 and MRF430 are housed in Case 368-01, whereas MRF141G, MRF151G, MRF175G and MRF176G use Case 375-01 (both shown below). All of these are high power devices (200–600 W), which results in an abnormally large amount of heat dissipated within a small physical area. For such high power transistors, special attention must be paid to the heat sink material as well as the finish and flatness of the mounting surface. The material should have at least a thermal conductivity equal to or better than copper and for the mounting surface flatness ±0.0005″ can be considered sufficient. The heat sink can be made of material with lower thermal conductivity such as aluminum, but in that case a copper heat spreader should be used. The heat spreader should have a minimum thickness of 0.25″ for case 375-01 and 0.375″ for 368-01 and should extend at least 0.5″ to 1.0″ beyond the flange edges, depending on the device type and the amount of dissipation involved. For die temperature calculations of devices in case 368-01, the Δ temperature between the mounting screw areas and the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions and dissipations of 150 W and 300 W respectively.

Although the data sheets contain information on the subject above as well as the mounting procedures of these devices, very few designers actually follow them. The maximum recommended torque on the #4 size mounting screws is 4–5 in.-lbs. along with split lock- and flat-washers, of which the latter should be in immediate contact with the flange's top surface. Experiments have shown that merely compressing the split lock washer to its full flatness produces enough torque for sufficient pressure against the heat sink. The split lock washers are available with various spring tensions. Bell type compression washers would be an even better choice if found with 5 in.-lbs. or lower torque specifications.

Calculations indicate that the length of the case 368-01 copper flange increases in excess of two thousands of an inch with a temperature change of 75°C. In such case, if the mounting screws are torqued too tight, the flange cannot expand in length but will bend upwards in the mid section, cracking the Beryllium Oxide insulators as well as the dice. It must also be noted that the thickness of the flange increases with temperature. For the excursion mentioned above, the amount is around 0.25 mils, which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. However the amount of increase is difficult to measure and depends on the exact type of mounting hardware used. The copper-tungsten flange of case 375-01 has a much lower expansion coefficient than copper, but if mounted on a copper or aluminum heat sink, it can be similarly bent during a cooling cycle as the heat sink material contracts.

Deformation can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied along with sufficient screw torque. The thermal compound will squeeze out of the mounting hole areas, but will remain under the center of the flange, deforming it in a similar manner. Depending on the amount of thermal compound and its type, deflections of 2–3 mils have been measured between the flange center and corners created by such conditions. The same can happen with all flange mounted RF devices, but with thicker Beryllium Oxide insulators and lower dissipation levels the problem is less severe.

The maximum operating junction temperature and the total dissipation are usually given in the data sheets. It should be able for the device to be operated within these limits if the case temperature can be kept at 25°C or the derating factor is taken into account. The 150°C storage temperature indicated implies that the device can be operated at that case temperature, which is true but at a much derated dissipation rating. However good engineering practices would limit the case temperature to 70–80°C and the die temperature to not higher than twice that.



CASE 368-01 CASE 375-01

The MC1378 — A Monolithic Composite Video Synchronizer

Prepared by Geoffrey Perkins

INTRODUCTION

The MC1378 was designed to enable an interface to be made between remote composite color video sources and a locally controlled RGB source of video. It contains the necessary synchronizing circuits, plus a complete color encoder.

The NTSC/PAL color encoding circuitry is very similar to the MC1377 and a detailed discussion of this subject can be found in AN932. The major differences between the MC1378 and MC1377 color encoding sections are that in the MC1378 the burst flag and color subcarrier quadrature accuracy are determined digitally and are not externally adjustable, and the MC1378 is designed to operate from a 5 V supply.

The MC1378 contains all the necessary circuitry to lock a computer to a remote color composite video source and to switch between the remote and the locally generated signals to create overlays in composite video. By using an additional device, the TDA3301/3, simultaneous overlays in RGB can be created. Because the MC1378, when operated in the remotely locked mode, passes the remote signal directly to its output without decoding and re-encoding, no loss in picture quality is experienced as can happen in less sophisticated systems.

SYSTEM DESCRIPTION: LOCAL MODE

(SEE FIGURE 1 AND BLOCK DIAGRAM)

Because the MC1378 operates in two basic modes, local and remote, it is logical to describe them separately. No external video is required in the local mode and the main function of the MC1378 is to encode the 1 V RGB signals into NTSC or PAL and to drive the graphics system's clock using the 4X subcarrier crystal oscillator as a reference.

A double balanced phase detector, PD5, is used to compare the now free running 4X subcarrier oscillator divided by four with the returning subcarrier signal at pin 8 and control the clock oscillator. The clock is divided down by the appropriate number within the graphics system to subcarrier frequency. This forms a PLL using the crystal oscillator at pins 10 and 11 as a reference. A separate clock could be used if it is not a multiple of subcarrier frequency — the disadvantage being that the encoded video signal's subcarrier will not be related to the horizontal frequency, and unpleasant dot crawl or beating on the display may result.

PD1 is a digital phase detector that compares the horizontal TTL sync fed into pin 40 with the MC1378's internal horizontal sync and controls the 4 MHz VCO to form a PLL. The 4 MHz VCO signal is internally divided by 256 to horizontal frequency. The eight stage divider is also used to develop the burst gate and burst flag signals by decoding the countdown. Burst gate is used extensively within the device for gating and clamping chroma and video signals. Burst gate is 4 μs wide and is centered about the 2.2 μs burst flag signal. Burst gate is also fed out of pin 5 to drive other devices that should be locked to horizontal frequency; e.g. TDA3301/3. Phase detectors PD2, 3 & 4 are not actively used in the LOCAL MODE but PD4 sets an arbitrary oscillator phase to the two electronic phase shifters.

In the PAL mode the R-Y modulator is phase inverted line by line and a burst flag is sent to both R-Y and B-Y modulators. The PAL flip-flop runs at an arbitrary phase in the local mode when the ident circuit is disabled by an external diode connected to pin 29. If a particular PAL phase is required, the PAL flip-flop can be reset at this pin.

The overlay enable (pin 25) should be set low in the LOCAL MODE to view the NTSC or PAL encoded RGB signals at pin 27.

REMOTE MODE

In the remote mode all phase detectors are active except PD5. An external valid video signal or remote signal must be fed into pin 24 to provide all the timing information to the host computer. Composite sync is separated from the remote signal and then fed to the vertical sync separator to detect vertical sync. The separated composite sync is used to lock the 4 MHz VCO using PD1, the vertical sync being fed out to the graphics system to lock its sync generator. The 4 MHz is divided by 256 to horizontal frequency and this is compared in PD2 with the TTL negative going H sync signal at pin 40. The output of PD2 is used to lock the system clock VCO, the frequency of which can range from 14 to 36 MHz depending upon the host computer's requirement. The system clock is divided down to Horizontal sync frequency within the host system and fed into pin 40.

The color burst from the remote signal is used to lock the 4X color subcarrier oscillator using PD3 which is

MC1378 Composite Video Overlay System
Block Diagram

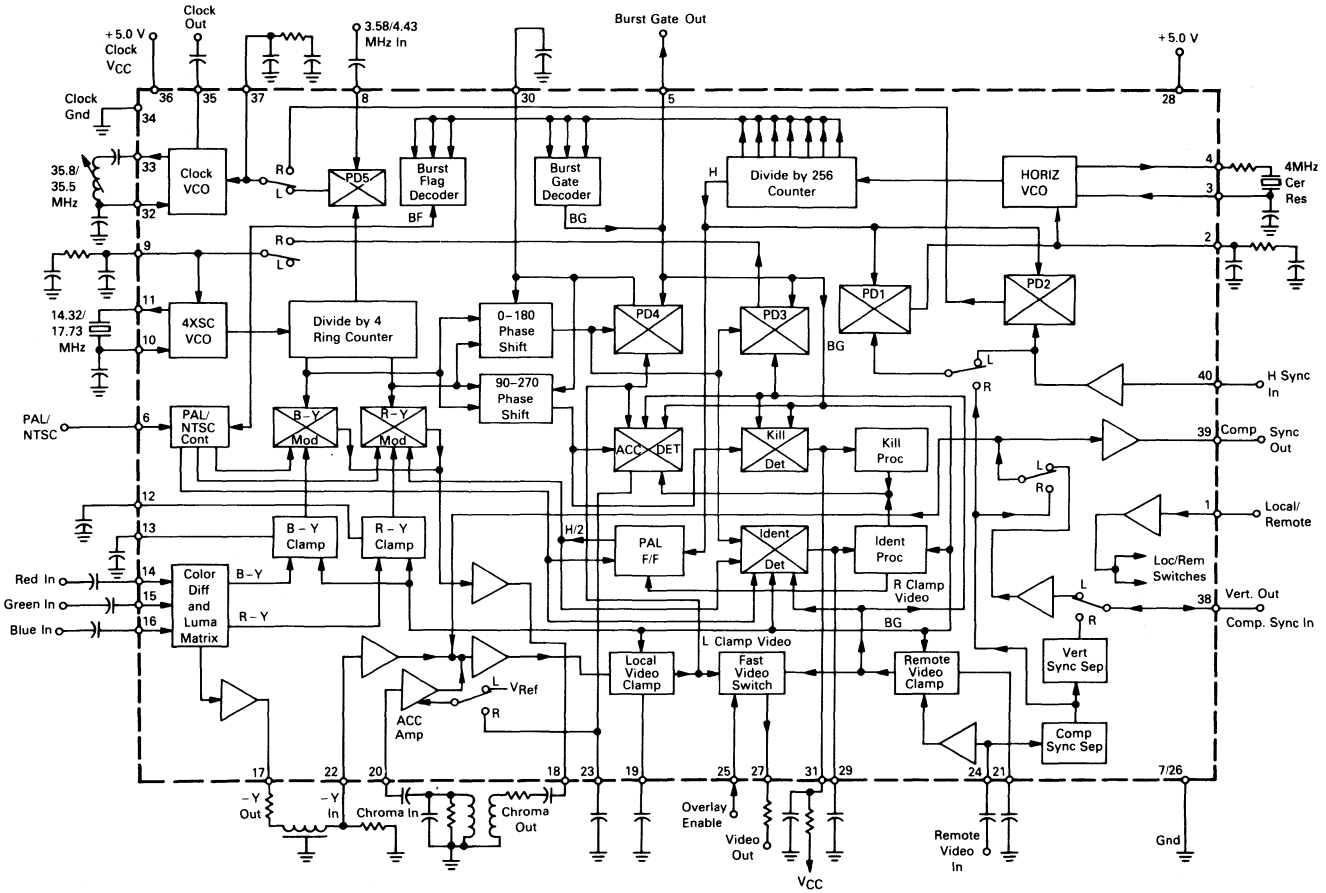
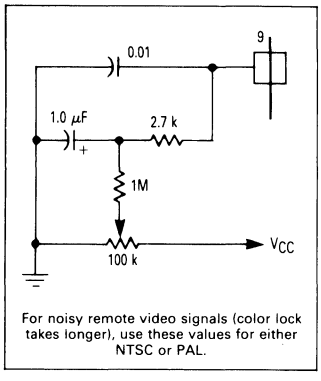
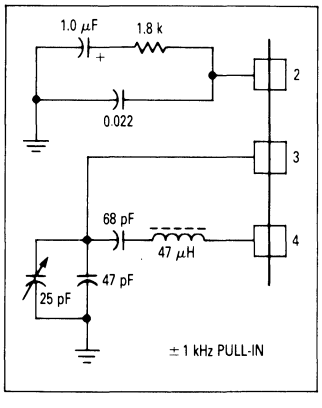


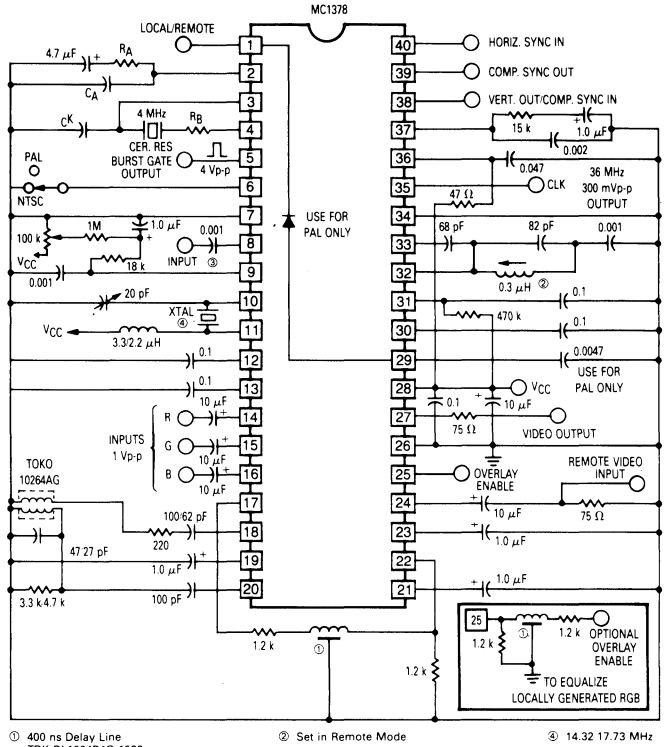
Figure 1. MC1378 Application Schematic

XTAL Specifications	
Frequency or	14.318180 MHz 17.734475 MHz
Mode:	Fundamental
Frequency Tolerance at 25°C	40 PPM Max
Frequency Temperature Tolerance $\Delta f/f_o$ 0–70°C	40 PPM Max
Load Capacitance	18 pF
Equivalent Series Resistance	50 Ω Max
C_1	15 mpF



For noisy remote video signals (color lock takes longer), use these values for either NTSC or PAL.





① 400 ns Delay Line
TDK DL1224D1D-1533 or
TDK401D-2249 (smaller) or
TOKO 321LNP1436PBAB

② Set in Remote Mode

③ 3.58/4.43 MHz
500 mVp-p

④ 14.32 17.73 MHz

Horizontal Pull-In (Typ)	Ceramic Resonators	CK	R_A	R_B	C_A
	For MURATA Resonator				
+400, −400	525 Line CSA4.03MTF102	47p	1.8 k	680	0.022
+400, −400	625 Line CSA4.00MTF102	47p	1.8 k	680	0.022

gated with burst gate. By using PD4 and comparing the burst of the locally generated composite video from the encoder section with the same subcarrier reference used to lock PD3, the subcarrier phases of both the local and the remote signals are made essentially equal. Similarly, the two burst amplitudes are compared in the ACC detector and made equal using a variable gain ACC amplifier in the locally generated chroma path.

The absolute burst amplitude of the remote signal only is detected by the kill detector, the chroma of the locally generated signal being turned off when the remote burst falls below a predetermined level. The kill level can be adjusted by changing the value of the resistor at pin 31. 470 kΩ kills at about 10–20 mVp-p remote burst (normal = 300 mVp-p).

In the PAL mode the phase of the ident of the remote burst is compared with the half line signal from the PAL flip-flop. If an error is detected, indicating that the local ident is not compatible with the remote ident, the flip-flop is reset using the ident processor. If a continuous ident error is detected, i.e. fixed or no burst on remote signal, the chroma in the local signal is killed.

Because the black levels, burst phases, burst amplitudes, and in the case of PAL, ident states are compatible between local and remote signals, the fast video switch operated by the overlay enable signal fed into pin 25 can be used to switch from one signal to the other to create overlays in composite video. Even portions of the timing waveforms (sync, burst, etc.) can be selected from either the local or remote sources for specific purposes, such as noise reduction due to weak signal remote, or VCR tape jitter reduction.

PHASE DETECTOR OPERATION SUMMARY

(SEE BLOCK DIAGRAM)

LOCAL MODE

PD1 — compares the internal horizontal frequency derived from the 4 MHz VCO with the Horizontal sync derived from the master clock from the host computer. The PLL formed locks the internal horizontal signal to the host computer's signal.

PD2 — not used in LOCAL MODE.

PD3 — not used in LOCAL MODE.

PD4 — active, but providing an arbitrary phase-shift setting between the subcarrier reference and the output chroma phase of the locally generated composite video.

PD5 — locks the master clock VCO (divided down to subcarrier frequency within the host computer) to the four times subcarrier crystal oscillator. The crystal oscillator becomes the system timing standard in the LOCAL MODE.

REMOTE MODE

PD1 — compares and locks the internally counted down 4 MHz VCO to the incoming remote horizontal sync. It is fast acting to follow VCR source fluctuations, etc.

PD2 — locks the master clock oscillator by comparing the internal horizontal signal with the H sync returning from the host computer.

PD3 — a gated phase detector, which locks the crystal oscillator frequency divided by four to the incoming remote signal burst.

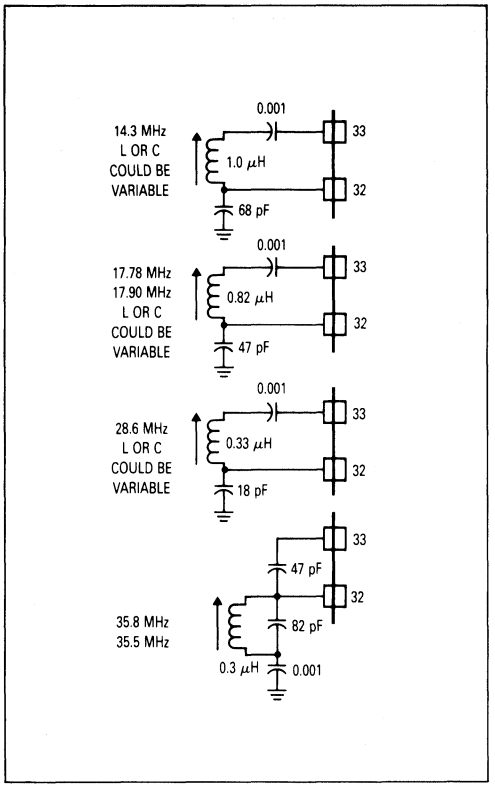
PD4 — controls an internal phase shifter to assure that the outgoing local color burst has the same phase as the incoming remote burst at PD3.

PD5 — not used in REMOTE MODE.

TYPICAL MASTER CLOCK FREQUENCY CONFIGURATIONS

Many applications require a Master Clock frequency different from the one shown in the standard schematic. The figure to the right shows the circuit and component values for typical clock frequencies. It is recommended that silver mica capacitors be used for accuracy and temperature stability except for the 0.001 μF coupling caps which can be standard ceramics.

Figure 2. Typical Master Clock Frequency Configurations



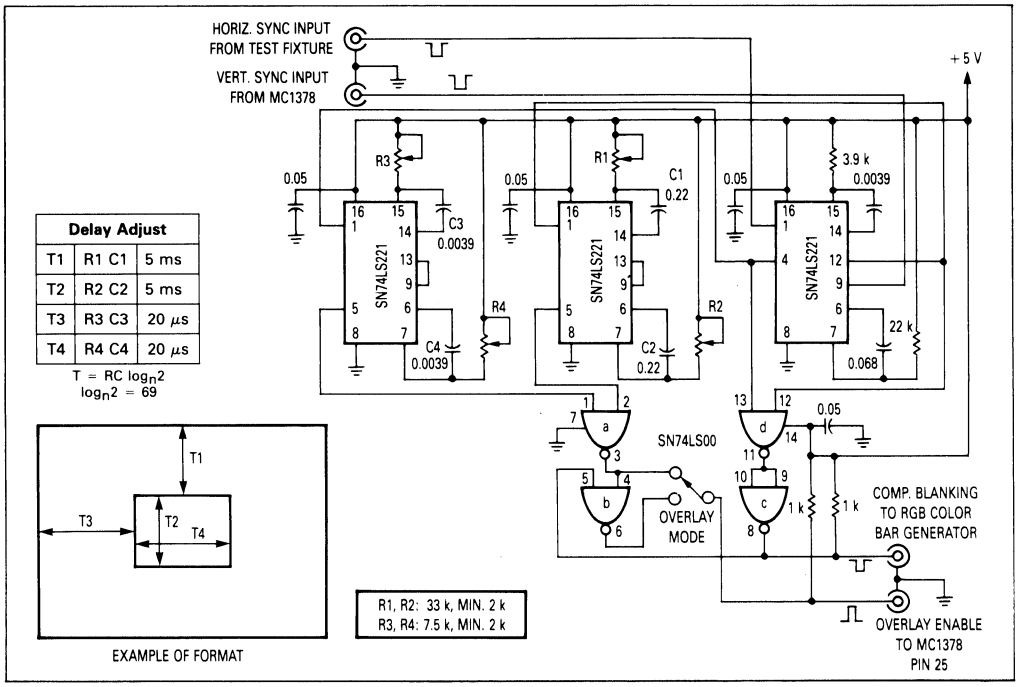
PICTURE IN PICTURE

Another test fixture that can be used with the RGB color bar generator (see schematic, Appendix D, in AN932) to insert video into color bars or vice-versa is the "picture in picture" circuit shown in Figure 3. Six one-shot monostables create variable delays and blanking pulses to drive the overlay input on the MC1378. T1, T2, T3, and T4 are variable delays such that the inserted picture window's size, position and aspect ratio may be adjusted.

TEST FIXTURES TO SIMULATE A COMPUTER

Sometimes major problems can be avoided if, before connecting the MC1378 to a computer system, the MC1378 application is tried using a test fixture. The major problems can be solved using the fixture leaving smaller details to be fixed in the total system. Two types of test fixture are shown in Figures 4 and 5. Both use a 36 MHz Master Clock, one for 525/60 Hz NTSC and the other for 625/50 Hz PAL. Other clock frequencies can be accommodated by changing the divide ratios.

Figure 3. Picture In Picture



Delay Adjust		
T1	R1 C1	5 ms
T2	R2 C2	5 ms
T3	R3 C3	20 μs
T4	R4 C4	20 μs

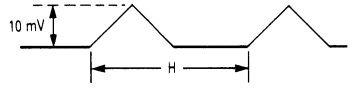
$T = RC \log_n 2$
$\log_n 2 = 69$

The Master Clock output from the MC1378 can be delivered using a short length (<12") of 50 Ω coax. The clock is amplified using one section of the MC74LS04 hex buffer-inverter connected with shunt feedback, followed by another stage to drive the first dividers. The first dividers bring the frequency down to 3.58 MHz or 4.43 MHz accordingly, to drive PD5 in the LOCAL MODE. This TTL output is reduced and rounded off using an RC network. Additional dividers are used to reach horizontal sync frequency. A one-shot MC74LS221 produces the 5 μs wide negative going horizontal sync signal to feed the MC1378 at pin 40. Other variations are possible and the two schematics are shown only as a guide.

MC1378 SET-UP PROCEDURE USING TEST FIXTURE

1. Switch to LOCAL MODE (pin 1 = 0 V). Ground pin 25.
2. Using a source of *accurate* subcarrier frequency, as an oscilloscope trigger, adjust the variable capacitor at pin 10 so that the burst appearing at pin 20 is the correct frequency to within 10 Hz.
   NTSC = 3.579545 MHz PAL = 4.4333619 MHz
3. Disconnect the signal feeding into pin 8 (3.58/4.43 MHz). Measure this frequency and adjust the Clock Oscillator until the meter reads 3.58 MHz (NTSC) or 4.43 MHz (PAL) ±10 kHz. Reconnect the signal to pin 8. This signal should now be phase-locked to the burst frequency at pin 20.
4. If a coil is used in the 4 MHz oscillator, adjust it to give the correct horizontal frequency at pin 5 (use pin 40 as a scope trigger). When the oscillator has phase locked, adjust the coil to give the correct waveform at pin 2.

   Pin 2 waveform



5. Switch to "REMOTE" MODE (pin 1 = +5 V).
6. Adjust the 100 k potentiometer at pin 9 to give the correct subcarrier frequency to within 50 Hz at pin 20 as in #2.
7. Feed 1 V p-p composite color video into pin 24. Color burst and composite sync should now appear at pin 27. The color burst will be absent if the 100 k pot was incorrectly adjusted.

MC1378 APPLICATION UPDATE: CLOCK OSCILLATOR ALIGNMENT

Two new circuits are shown in Figure 6 to improve the pull-in range and speed of the Clock Oscillator phase-locked loop. Figure 6b shows a circuit that has no compromise between the characteristics in both the local and remote modes. Both circuits allow a much wider tolerance on the alignment of the Clock Oscillator.

Figure 4. Test Fixture, NTSC 525/60 Hz

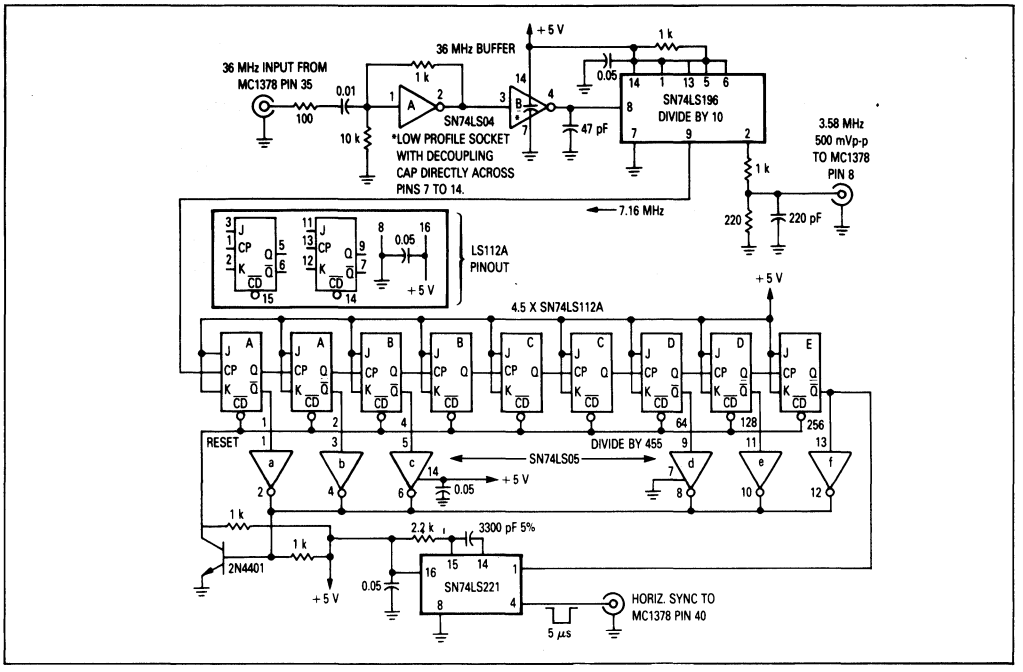


Figure 5. Test Fixture, PAL 625/50 Hz

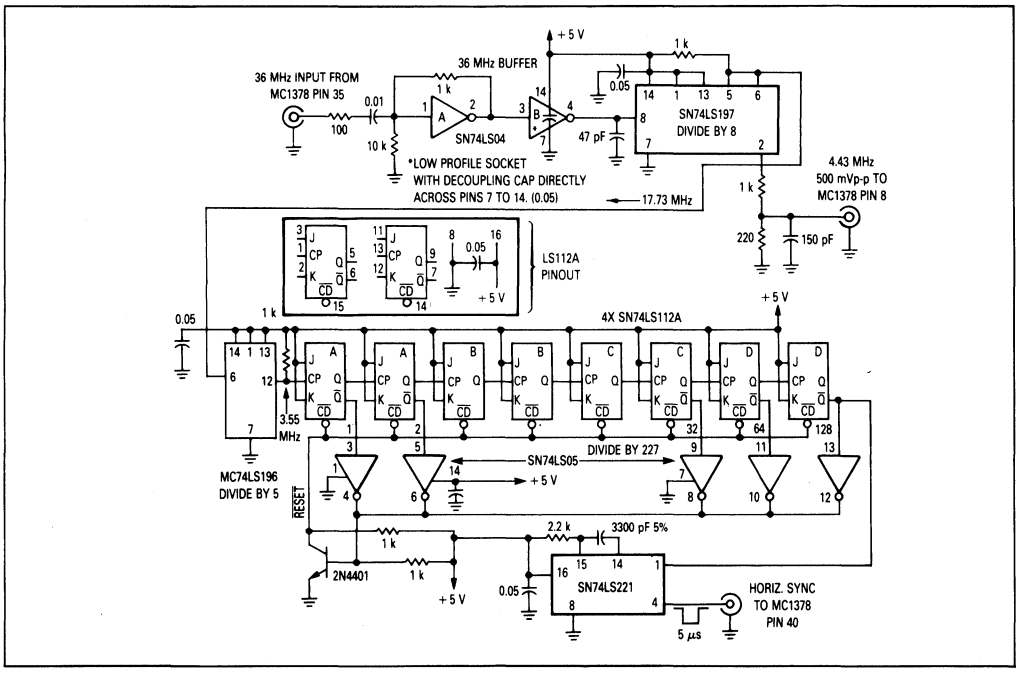
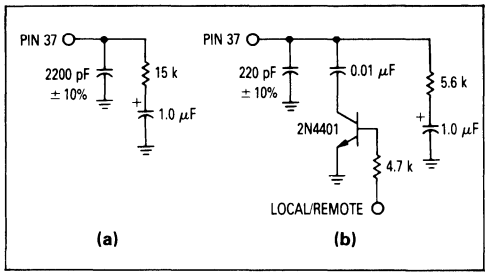


Figure 6. Clock Oscillator Alignment



RGBI TTL TO RGB, 1 V ANALOG CONVERSION

Figure 7 shows a circuit to interface a TTL RGBI output personal computer to the RGB analog inputs of the MC1378. If the circuit is used with the values shown, no coupling capacitors are required to the RGB inputs of the MC1378. The +5 volt supply to the 390 Ω resistors should be very clean to prevent interference on the encoded signal. IC4 is used to simulate 'brown' to be compatible with TTL display monitors.

USING THE MC1378 IN CONJUNCTION WITH THE TDA3301/3 FOR OVERLAYS IN BOTH RGB AND COMPOSITE VIDEO

In some video applications both RGB overlay and composite video overlay are required. In these situations the MC1378 can be used as a time base locked to the remote source, not only for the graphics computer, but also for the color decoder.

The burst gate output of the MC1378 appearing at pin 5 can be used to drive the sandcastle pulse input of the TDA3301/3 at pin 27. Because the output level of the MC1378 is too low to drive the TDA3301/3 directly, a small noninverting buffer is used, as shown in Figure 8, to enable the burst gate pulse to exceed the required slice level at the TDA3301/3. A vertical pulse for the TDA3301/3 clamping system can be obtained at pin 38 of the MC1378 operating in the REMOTE MODE only when a valid video signal is applied. The vertical output must be inverted as shown in Figure 9. If a continuous vertical pulse is required so that the output clamps of the TDA3301/3 are always operating, a locked 50/60 Hz oscillator will have to be used. This could consist of a MC1455 type timer circuit. If a vertical pulse is produced by the microcomputer graphics source, it should be used instead. When in LOCAL MODE, an alternative source of vertical sync must be found to drive the TDA3301/3.

The overlay fast video switches in the MC1378 and TDA3301/3 operate in the opposite sense to each other. Therefore an inverter must be used between pin 25 of the MC1378 and pin 23 of the TDA3301/3.

The delay produced by the use of a delay line in the luminance path of the MC1378 must be compensated by using a similar delay in the overlay enable line as shown in Figure 10. The RGB inputs are essentially compatible between the MC1378 and the TDA3301/3, and can be connected as shown in Figure 11.

Figure 7. RGBI to RGB Converter

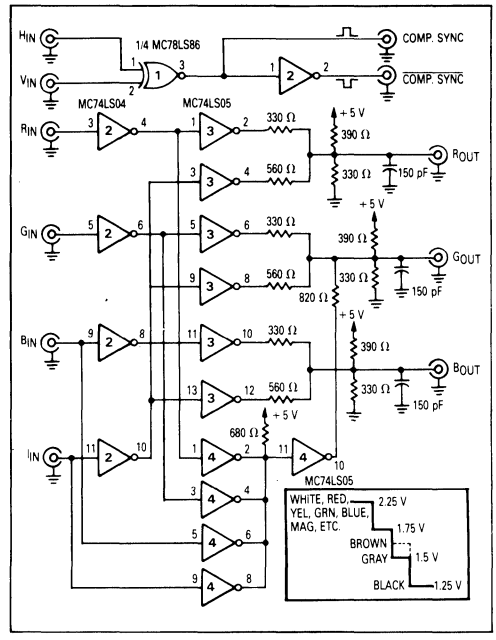


Figure 8. Noninverting Buffer, Level Changer

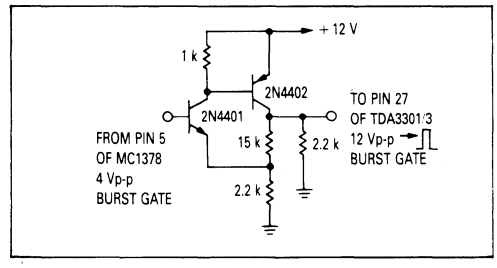


Figure 9. Vertical Output Inverter

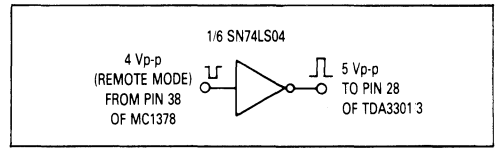


Figure 10. Overlay Input Inverter and Delay

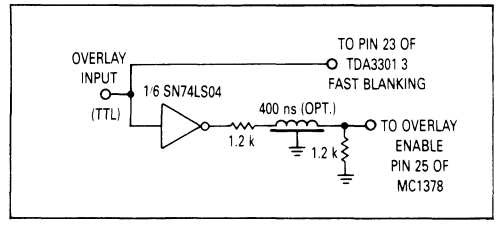


Figure 11. RGB Input Connection

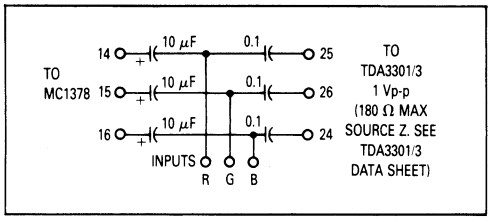


Figure 12. 3.58 MHz Chroma Trap

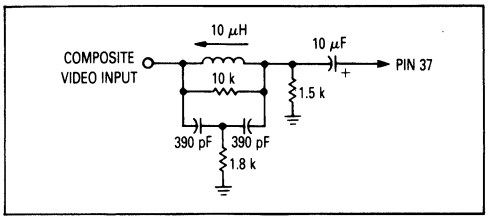


Figure 13. RGB Output Blanking Circuit (One of Three Required Shown)

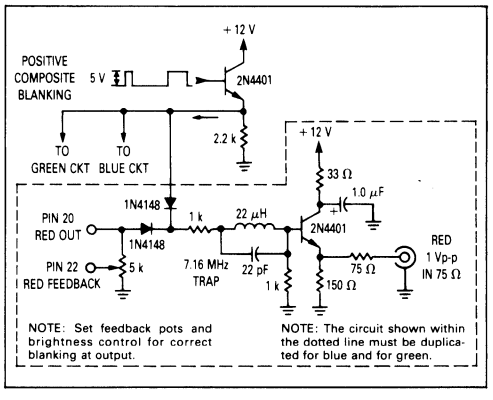
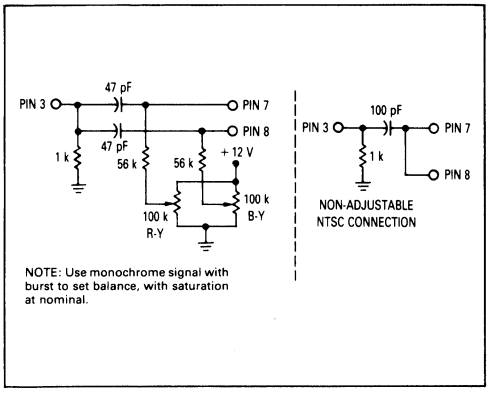


Figure 14. NTSC Components for TDA3301/3 for Coupling the Color I.F. to the Demodulators

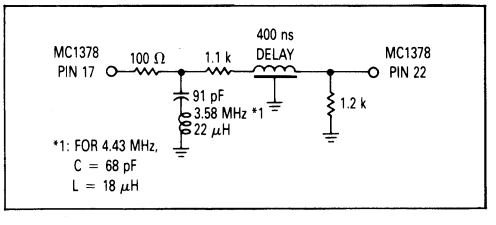


A 3.58 MHz chroma trap for the luminance input is shown in Figure 12. For more general information, see the TDA3301/3 data sheet.

A circuit for blanking, filtering and driving a 75 Ω load with 1 V p-p is shown in Figure 13. The 5 V composite blanking could be developed by using part of the circuit shown in Figure 4.

Figure 14 shows a method for balancing the 3.58 MHz or 4.43 MHz demodulator leakage appearing at the RGB outputs. Normally this is not necessary, but for more exacting applications it may be required.

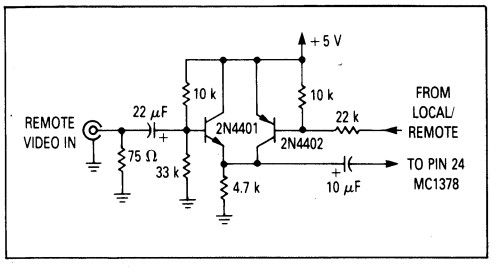
Figure 15. MC1378 Subcarrier Notch Filter



MC1378 SUBCARRIER NOTCH FILTER

Cross color can cause annoying rainbow effects on fast luminance edges especially in noninterlaced pictures. Figure 15 shows a simple subcarrier notch filter in the luminance delay path of the MC1378 to remove some of the offending cross color artifacts at the expense of luminance bandwidth. The cross color problem can be especially bad when attempting to record on consumer type VCRs because on playback the chroma-horizontal interleaving becomes random. The notch method is equally effective on PAL or NTSC.

Figure 16. Improved Remote Video Input Isolation Circuit



IMPROVED REMOTE VIDEO INPUT ISOLATION CIRCUIT

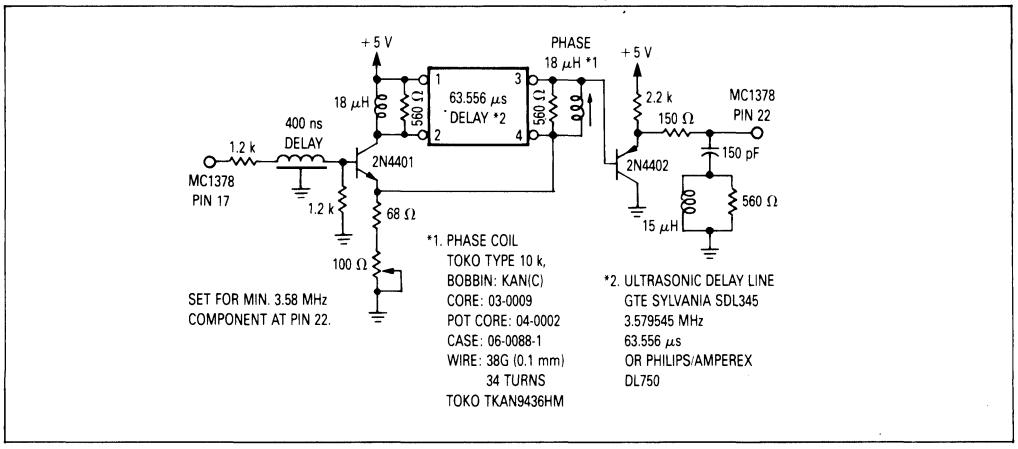
Because of certain limitations in the device and its packaging, the cross talk from remote composite video input to composite video output can be troublesome when operating in the LOCAL MODE with a video signal present at the composite video input. Typically, the cross talk is about −35 dB at 4.43 MHz and better at 3.58 MHz. Low frequencies are better than −60 dB. The circuit shown in Figure 16 will improve the isolation in the LOCAL MODE by an additional −20 dB.

MC1378 NTSC LUMINANCE COMB FILTER

To avoid loss of luminance bandwidth while removing color artifacts, a simple comb filter can be used in NTSC (see Figure 17). For 625 line PAL, a more complex arrangement has to be made which would be beyond the scope of this application note. The NTSC comb filter is only effective on interlaced color and horizontal signals. Noninterlaced signals could become worse with this arrangement. However, it may be possible to short the delay line input, pins 1 and 2, on noninterlaced signals.

The amplitude and phase adjustments are made when a small amount (550 mVp-p) of 3.58 MHz subcarrier is added at the output of the 400 ns delay line. The two adjustments are trimmed for minimum subcarrier at pin 22. By using this technique, virtually all the cross color artifacts are removed without loss of luminance bandwidth.

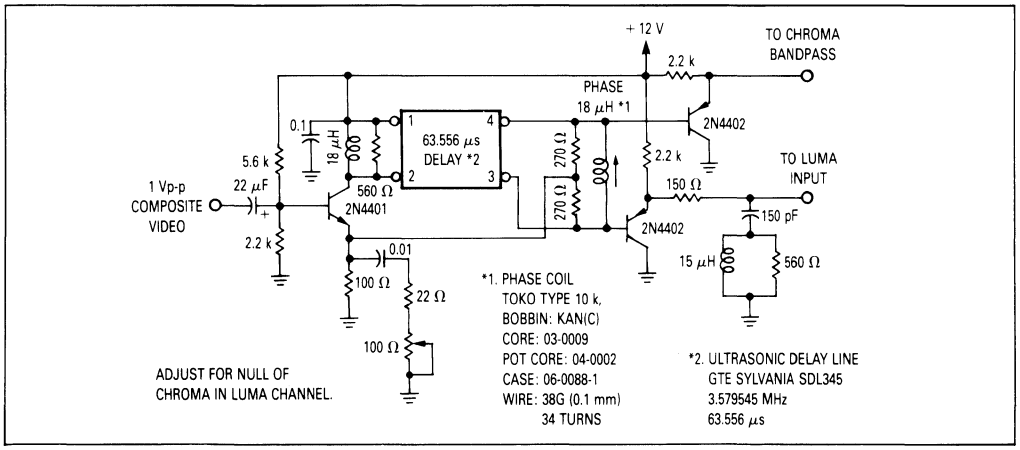
Figure 17. MC1378 NTSC Luminance Comb Filter (For Interlaced Video Only)



NTSC DECODER COMB FILTER FOR THE TDA3301/3

Figure 18 shows a circuit similar to Figure 17 to improve the luminance bandwidth by removing the 3.58 MHz notch in the luminance channel of the TDA3301/3. Again, this filter, as shown, is only applicable to NTSC. Both luminance and chrominance are combed of chroma and luma respectively to remove colored artifacts in interlaced video. The setup is accomplished by adjusting the amplitude and phase for minimum subcarrier at the luminance output.

Figure 18. NTSC Decoder Comb Filter for the TDA3301/3



CARRIER BALANCE OF COLOR MODULATORS

Certain applications require perfect carrier balance of the color modulators. This is simply realized in Figure 19. The two 100 k potentiometers should be adjusted with a black signal for minimum subcarrier at the video output.

Figure 19. Carrier Balance of Color Modulators

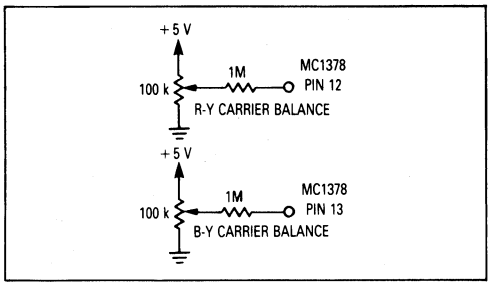
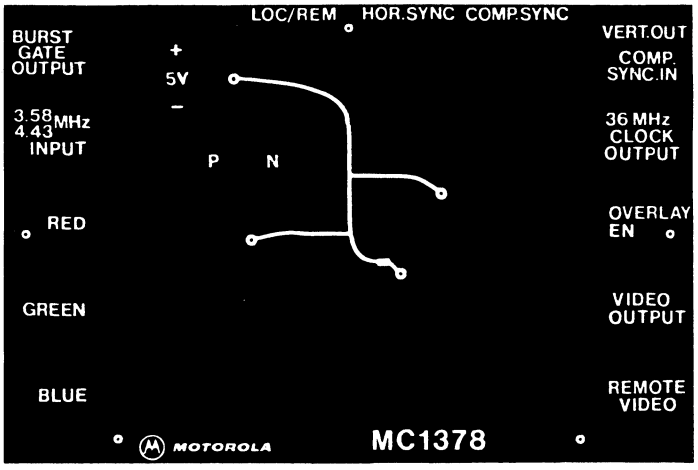
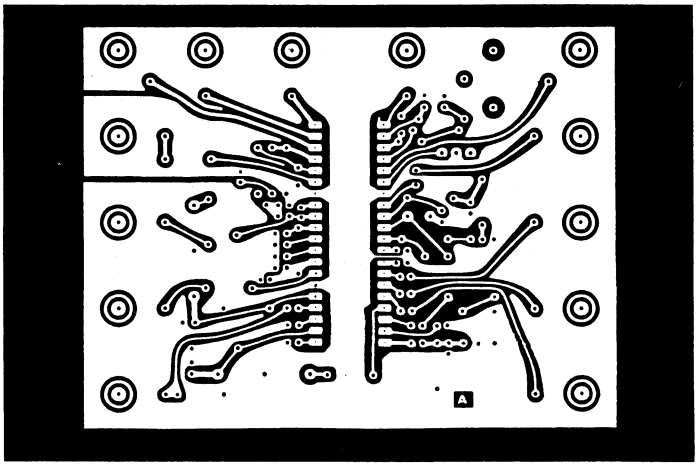


Figure 20. Printed Circuit Board Layout



Component Side Pattern (not full size)



Circuit Side Pattern (not full size)

Figure 21. Printed Circuit Board Components Layout

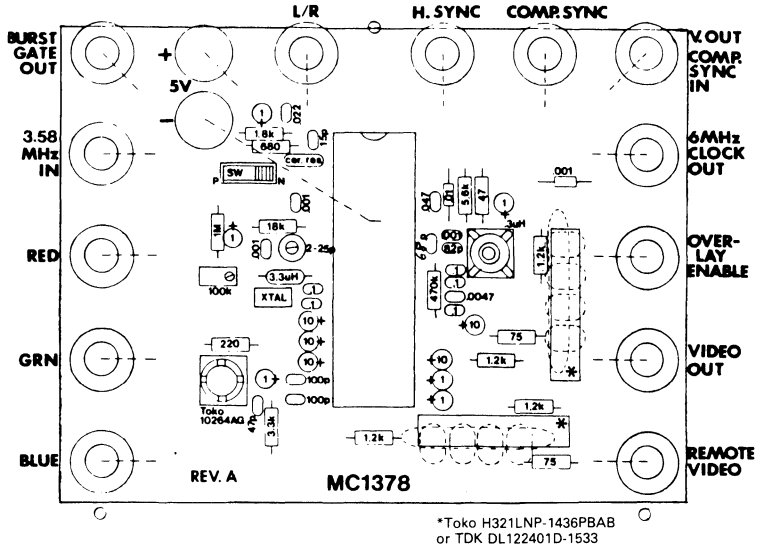
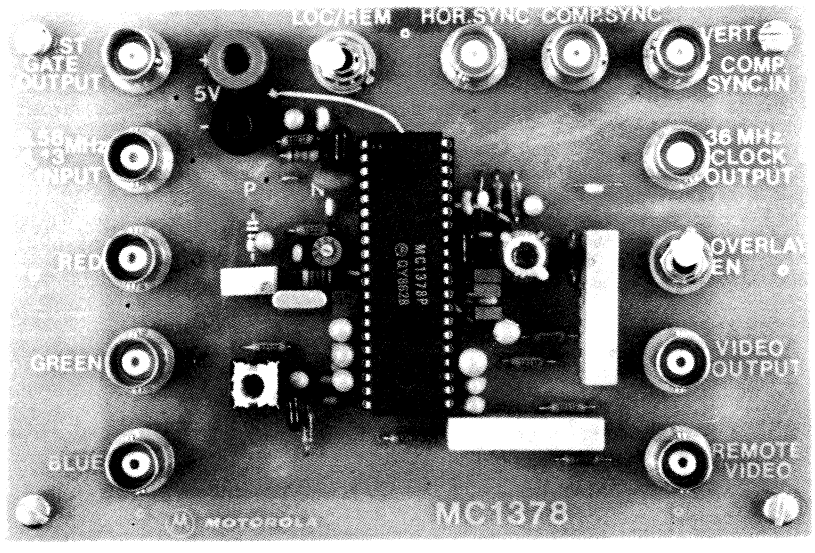


Figure 22. Photo



MC1378 EXPECTED WAVEFORMS

Pin 1 Local-0 Volts, Remote-5 Volts
2 3 Vdc Approximate (See Application Note)
3 4 MHz, 200–300 mVp-p Sine Wave (Oscilloscope Probe will disturb the Horizontal PLL)
4 Distorted 4 MHz Signal
5 4 V, 4 μs Wide Pulse Locked to Horizontal
6 NTSC-0 V/PAL-Open
7 Ground
8 3.58 MHz/4.43 MHz 300–800 mVp-p Sine or Square Wave from RMI in Local Mode — Shows Beat Between Remote Signal and Local Subcarrier, but otherwise unimportant
10 14.32/17.73 MHz, 150–300 mVp-p Sinewave (Scope Probe will disturb PLL)
11 Distorted 14.32/17.73 MHz Signal
12/13 3.5 Vdc Approximate
14/15/16 1 Vp-p RGB Color Signals, Low for Black, High for Color. All Blanking at Black Level both for Horizontal and Vertical. These are Analog Inputs, so any Noise on RGB will appear at the Output.
17 Inverted Luma Signal 1 Vp-p for 100% Color Bars (1.8 V White/2.8 V Black)
18 Chroma Output 3.58/4.43 MHz with Harmonics, Burst 100 mVp-p, Chroma 300 mVp-p, 100% Color Bars (Approximate Amplitudes)
19 3.4 Vdc Approximate
20 Chroma Input 3.58/4.43 MHz, Burst 100 mVp-p, Chroma 300 mVp-p, 100% Color Bars (Approximate Amplitudes)
21 3.3 Vdc Approximate
22 Inverted Luma 0.5 Vp-p, 100% Color Bars (0.9 White/1.4 V Black)
23 3.5 Vdc Approximate
24 Remote Video Input 1 Vp-p, Negative SYNC
25 Overlay Enable Input; Low — Encoded RGB, High — Remote Signal
Threshold = Approximately 1.4 V
26 Ground
27 Composite Video Output
28 V_{CC} +5 Vdc
29 PAL Identification Pin (Not Used in NTSC)
In PAL Stepped Waveform at Vertical Rate
In NTSC DC 0.5 V
30 2.7 Vdc Approximate
31 DC 0.6 V with 100 mV Vertical Ripple When Color Unkilled, 4.2 Vdc Approximate When Color Killed
32/33 36 MHz 200 mVp-p. Difficult to Observe with Conventional Oscilloscope Probe because of Grounding Problems
34 Ground
35 Clock Output 36 MHz, Sinewave 300 mVp-p, Open Circuit Approximate. When used at Lower Frequencies the Output may become Bigger and Clipped. Also same Scope Problem as with 32/33 at 36 MHz
36 V_{CC} +5 Vdc
37 2.2 Vdc Approximate (See Application Note)
38 Local Composite SYNC Input in LOCAL MODE TTL Negative
Remote Vertical SYNC Output in REMOTE MODE TTL Negative
39 Composite SYNC TTL Output Negative
40 Horizontal SYNC Input TTL Negative

APPENDIX
DIRECTORY OF COMPONENT MANUFACTURERS

California Crystal Laboratories	(800) 333-9825 crystals
Coilcraft 1102 Silver Lake Road Cary, IL 60013	(312) 639-6400 coils
Comtec	(602) 526-4123 crystals
Fox Electronics	(813) 693-0099 crystals
GTE Sylvania Electronic Components Division 2401 Reach Road Williamsport, PA 17701	(717) 326-6591 crystals, ultrasonic delay lines (for comb filter)
International Crystals	(405) 236-3741 crystals
muRata-Erie 2200 Lake Park Drive Smyrna, GA 30080 **Distributor — Time Electronics** **Distributor — Sterling Electronics**	(404) 436-1300 coils see local directory contact muRata for nearest location
Phillips/Amperex Optoelectronics Division	(401) 232-0500 ultrasonic delay lines (for comb filter)
Standard Crystal Corporation	(818) 443-2121 crystals
TDK Corporation of America 1600 Feehanville Drive Mount Prospect, IL 60056	(312) 803-6100 400 ns delay lines
Toko America Inc. 1250 Feehanville Drive Mount Prospect, IL 60056 **Distributor — Digikey** **Distributor — Inductor Supply**	(312) 297-0070 coils, transformers, 400 ns delay lines (800) 344-4539 (800) 854-1881 (800) 472-8421 (from within California)

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Electrical Characteristics of the CR2424 and CR2425 CRT Driver Hybrid Amplifiers

By Dan Brayton

CRICUIT AND THERMAL DESCRIPTION OF CR2424 AND CR2425 CRT DRIVER HYBRID AMPLIFIERS

CIRCUIT DESCRIPTION

The circuit of the CRT driver amplifiers consists of a pair of complementary common emitter Class A stages DC stacked across the 60 V supply. The "top" PNP device is connected as a current source at DC through mid frequencies; at high frequencies, the "current source" becomes active. This complementary Class A pair drives complementary Class B emitter followers.

THERMAL DESCRIPTION

All four transistors (silicon bipolar) have identical horizontal geometries (active areas), gold metallization and plasma nitride passivation. These transistors are each mounted on .055 x .055 inch gold plated copper heat spreaders which serve to maximize the heat flow from the transistor die through the alumina thin-film substrate to the aluminum flange (heatsink or case) that is soldered to the back side of the substrate. This structure results in a thermal resistance of 35°C/watt max (30°C/watt typical) for junction to case (flange) for each of the four active transistors.

Junction temperatures can, therefore, be computed if the power dissipation for each transistor is known. The power dissipated in each transistor is a function of the amplifier operating conditions as listed in Table 1.

Table 1. Transistor Power Dissipation

Designation	Q_1 PNP	Q_2 NPN	Q_3 PNP	Q_4 NPN
Type	A	A	B	B
Class of Operation	P_D(W)	P_D(W)	P_D(W)	P_D(W)
Case I	0.75	0.75	<0.1	<0.1
Case II	0.2	1.6	<0.1	<0.1
Case III	1.6	0.2	<0.1	<0.1
Case IV	0.8	0.8	0.2	0.2
Case V	1.0	1.0	1.6	1.6

Case I No connection to input pin 1; output ≈ 30 Vdc
Case II Black level; output ≈ 55 Vdc
Case III White level; output ≈ 5.0 Vdc
Case IV SQ wave input f = 60 Hz; output = 40 V_{P-P}
Case V SQ wave input 7.5 ns pixel; output = 40 V_{P-P}

General conditions: V_{CC} = 60 V; load = 8.5 pF

Therefore, worse case junction temperature rise over case (flange) is 1.6 watts x 35°C/W = 56°C. The type of transistor used in Motorola CRT hybrid driver amplifiers is rated for operation up to 200°C. At 150°C junction temperatures, MTTF for an individual transistor chip is greater than 140 years.

CRT HYBRID TUBE ARC SIMULATION

A tube arc was simulated by electrostatic discharge equipment. A variable voltage source charges up a capacitor.

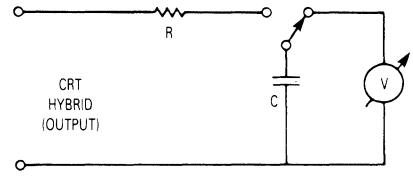


Figure 1. Electrostatic Discharge Simulator

Then the energy inside the capacitor is discharged through a resistor to the CRT hybrid. Test conditions of R = 10 ohms and C = 150 pF were used.

CASE 1, UNPROTECTED:

The CRT hybrid failed at 2500 volts. Because output of the Electrostatic Discharge Simulator is connected to ground during charge period, a 0.01 μF DC blocking capacitor is used to prevent output of the CRT hybrid to ground, which could damage the hybrid.

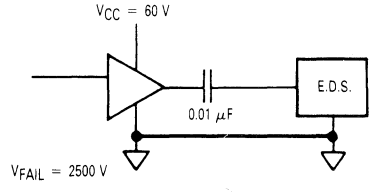


Figure 2. Circuit for Case 1

CASE 2, PROTECTION RESISTOR:

A protection resistor of 47 Ω is connected between the E.D.S. and hybrid. The hybrid failed at 4500 volts. Again a 0.01 μF blocking capacitor is used to prevent the hybrid discharging to ground.

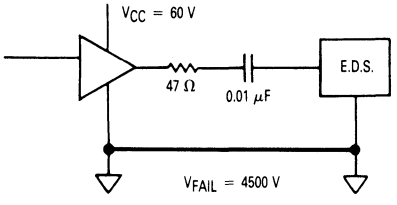


Figure 3. Circuit for Case 2

CASE 3, PROTECTION DIODE:

A protection diode (1S583 Hitachi) was added. Failure of the hybrid occurred at 9500 volts. Electrical characteristics for this diode are listed in Table 2 below.

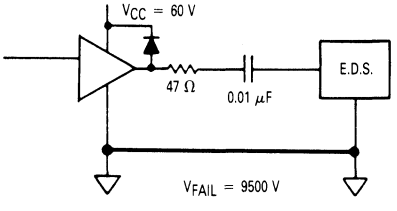


Figure 4. Circuit for Case 3

CASE 4, BYPASS CAPACITOR:

A 0.1 μF bypass capacitor was added along with diode and resistor. In this case, failure of the hybrid occurred at 15,000 volts.

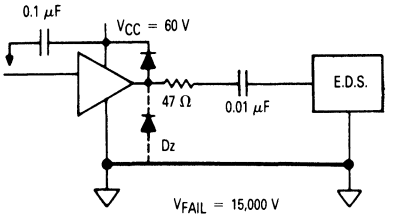


Figure 5. Circuit for Case 4

CONCLUSION:

Obviously the circuit in case 4 offered the best protection to the hybrid amplifier. The bypass capacitor and diode should be placed as close to hybrid V_{CC} node as possible, and ground leads on the bypass capacitor and hybrid should be able to carry surge current to insure the best protection.

NOTE: A diode, Dz, should be added if there is reason to believe that large negative surges may reach the video driver output port.

PERFORMANCE CHARACTERISTICS

Typical bandwidth and rise and fall times of the CRT driver are shown in Figures 6 through 10.

Table 2. Characteristics of Protection Diode 1S583

MAXIMUM RATINGS (T_A = 25°C)

Item	$V_{R(peak)}$	V_R	$I_{F(peak)}$	I_O	T_J
Unit	V	V	mA	mA	°C
Rating	250	220	625	200	175

NOTE: JEDEC DO-35 Sealing condition.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Item	Symbol	Test Condition	Limit		Unit
			Min	Max	
Forward Voltage	V_F	I_F = 100 mA		1.0	V
Reverse Current	I_R	V_R = 220 V		1.0	μA
Reverse Recovery Time	t_{rr}	$I_F = I_R$ = 30 mA R_L = 50 Ω, i_{rr} = 0.1 IR		80	ns

NOTE: Glass Sealing condition.

Figure 6. Bandwidth versus Output Load, C_L

C_L (pF)	V_O = 20 V_{p-p} BW (MHz)	V_O = 40 V_{p-p} BW (MHz)
6	175	145
8.5	172	145
10	166	140
12	160	130
15	150	120
18	140	100

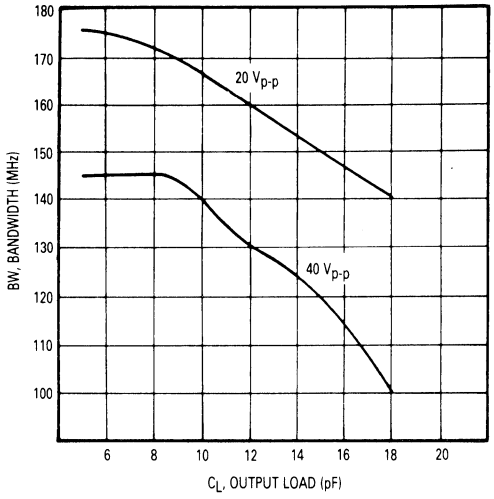


Figure 7. Rise and Fall Times and Overshoot versus Output Swing Voltage (Under Regular Operation Condition — V_{CC} = 60 V, Load = 8.5 pF)

Output Swing (V)	t_r (ns)	t_f (ns)	Overshoot (V) Leading	Trailing
50	2.6	2.4	2.5	1.2
40	2.2	2.0	4.0	2.4
30	1.9	1.9	4.6	3.0
20	1.8	1.7	4.2	2.8
10	1.8	1.8	2.4	1.2

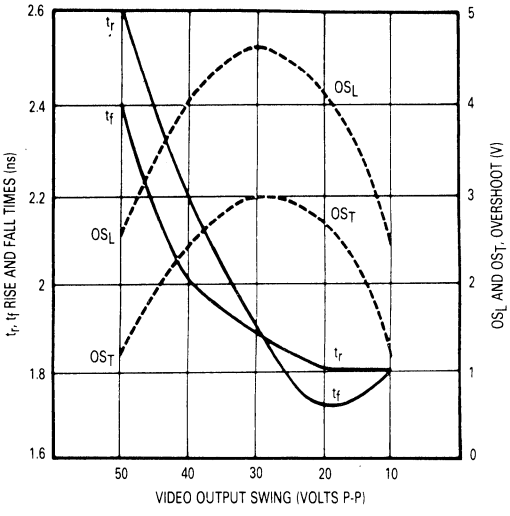


Figure 8. Rise (t_r) and Fall (t_f) Times versus Output Load, C_L

C_L (pF)	t_r (ns)	t_f (ns)
6.0 pF	1.8	1.6
8.5 pF	2.2	2.0
10 pF	2.4	2.1
12 pF	2.6	2.3
15 pF	2.8	2.5
18 pF	3.1	2.8

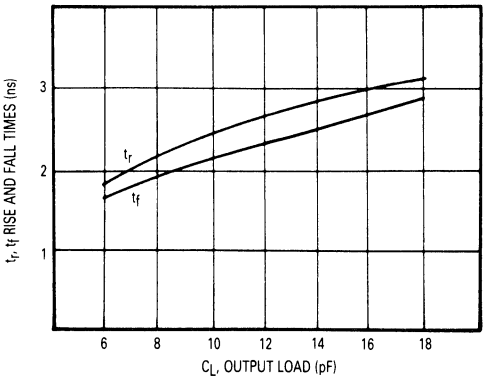


Figure 9. Rise and Fall Times and Bandwidth versus Loads

A. C_L = 8.5 pF V_{CC} = 70 V

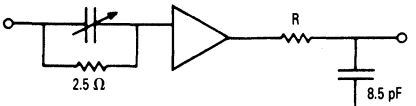
t_r (ns)	t_f (ns)	BW (MHz)	Condition
2.0	1.8	147	40 V Swing
2.6	2.2	133	50 V Swing
2.7	2.5	111	55 V Swing

B. C_L = 15 pF V_{CC} = 70 V

t_r (ns)	t_f (ns)	BW (MHz)	Condition
2.6	2.1	133	40 V Swing
3.5	2.5	105	50 V Swing
3.6	2.8	83	55 V Swing

C. C_L = 8.5 p V_{CC} = 60 V V_{OUT} = 40 V Swing (Standard Operating Conditions)

t_r (ns)	t_f (ns)	BW (MHz)
2.5	2.0	142



All standard test conditions, except add R.

Figure 10. Rise and Fall Times versus Serial Output Resistance

R (Ω)	t_r (ns)	t_f (ns)
0	2.1	1.8
10	2.1	1.9
20	2.2	2.2
30	2.4	2.3
40	2.5	2.5
50	2.6	2.6
60	2.7	2.8
70	2.8	3.0
80	3.0	3.2
90	3.2	3.4
100	3.4	3.6
110	3.4	3.8
120	3.6	4.0
130	3.8	4.2
140	4.0	4.4
150	4.2	4.6
160	4.4	4.7
170	4.5	4.8
180	4.8	5.0
190	4.8	5.4
200	5.0	5.6

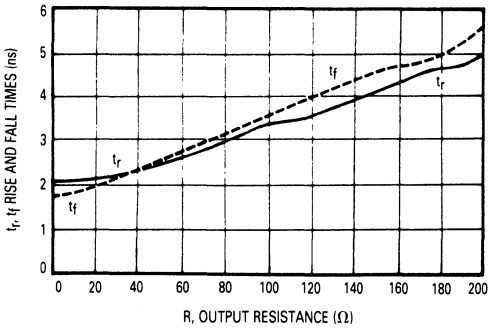


Figure 11.

Application Note

REFLECTING ON TRANSMISSION LINE EFFECTS

This application note describes introductory transmission line characterization, analysis, and application. Over the past couple of years, microprocessors and digital logic in general have seen substantial increases in line drive capability. This increase has fostered the current logic and microprocessor speeds readily available today. The relatively quick rise and fall time of today's digital devices makes an understanding of transmission lines and their effects on system reliability a necessity.

TRANSMISSION LINE CHARACTERIZATION

When discussing transmission lines one should reflect on the following definition. A transmission line is two or more conductors separated by some insulating medium, used to carry a signal. At first glance this seems rather trivial, but upon closer examination one finds a host of physical nuances which make the transmission line a sophistcated element to describe, among which are:

1. Line resistance present in any non-ideal conductor.
2. Line conductance ((1/R) = G) present in any non-ideal insulating medium resulting in leakage currents.
3. Line inductance present in any current carrying conductor undergoing a change in magnetic flux.
4. The line capacitance present between the two conductors separated by the insulating medium.

Figure 1 shows the line under discussion. The circuit consists of two series elements (Z + L) and two shunt elements (C + G).

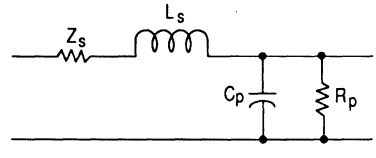


Figure 1. Transmission Line Circuit

Our discussion will be primarily concerned with C + L, because these elements are the frequency dependent components of the line (neglecting skin effect). For frequencies above approximately 100 kHz, Z_o, the characteristic impedance of the line, is equal to the square root of L/C and is independent of line length. The propagation constant (t_{pd}) or time delay constant is the square root of L*C, and is a function of line length. Z_o is of particular importance to our discussion because when you match this impedance to the load, you reduce the effects of transmission imparted to both the source and the load.

TRANSMISSION LINE REFLECTIONS

Reflections on a line are caused by a mismatch in impedance between the line and the load. If all the power delivered to the line is absorbed by the load then there will be no reflected power back at the source side of the line. This principle of power conservation is the cornerstone of this application note. Refer to Figure 2 as the equations are discussed. The equation describes the ratio of absorbed power to reflected power based on the ratio of line to load impedance.

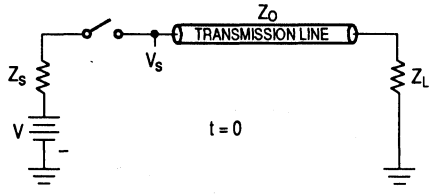


Figure 2. Transmission Line

The current delivered to the load is $I_L = I_{INC} - I_{RFL}$ (incident current minus reflected current), while the load voltage is, $V_L = V_{INC} + V_{RFL}$ (incident voltage plus reflected voltage). We need to find an equation that relates incident voltage to reflected voltage. Therefore noting that the load current $I_L = (V_F - V_{RFL})/Z_O$ (incident voltage minus reflected voltage divided by the characteristic impedance) we can see the following relationship.

$$\frac{V_{INC} + V_{RFL}}{Z_L} = \frac{V_{INC} - V_{RFL}}{Z_0} \quad (1)$$

Solving for V_{INC}/V_{RFL}

$$Z_O(V_{INC} + V_{RFL}) = Z_L(V_{INC} - V_{RFL}) \quad (2)$$

$$V_{RFL}(Z_O + Z_L) = V_{INC}(Z_L - Z_O) \quad (3)$$

$$\frac{V_{RFL}}{V_{INC}} = \frac{Z_L - Z_O}{Z_L + Z_O} = \rho_L \quad (4)$$

This expression is called the load reflection coefficient (ρ_L). Note a ρ_S also exists which relates the ratio of source impedance to line impedance. This expression is called the source reflection coefficient and is shown in Equation 5.

$$\rho_S = \frac{Z_S - Z_O}{Z_S + Z_O} \qquad (5)$$

One can see that there are three distinct possibilities which require inspection. First, the situation where the load impedance equals the line impedance ($Z_L = Z_O$) and $\rho_L = 0$ (no reflections – a properly terminated line); second, where the load impedance is greater than the line impedance ($Z_L > Z_O$) and ρ_L is positive, generating a reflection whose polarity matches that of the incident voltage, and, finally, where the load impedance is less than the line impedance and ρ_L is negative, generating a reflection whose polarity is opposite to that of the incident voltage. Let's take a closer look at the last two cases.

Assume that $Z_L = 4Z_O$, and that the source impedance = line impedance. V = source voltage, and V_L = load voltage (see Figure 3).

$$\rho_L = \frac{Z_L - Z_O}{Z_L + Z_O} = \frac{4Z_O - Z_O}{4Z_O + Z_O} = 0.6$$

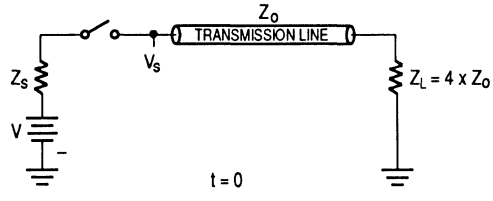


Figure 3. Transmission Line Circuit with $Z_L = 4 * Z_O$ and $Z_S = Z_O$

Thus at t = 0 a voltage wave of 1/2(V) (because Z_S and Z_O form a voltage divider on V) begins to travel down the line and arrives at Z_L one t_{pd} or propagation delay later. When the wave encounters the load impedance mismatch, a reflected wave equal in magnitude to (V/2)*0.6 is reflected back toward the source, and arrives at the source again one t_{pd} later. This causes the voltage at the source to rise therefore creating the classic overshoot condition.

Since the source and line impedance are matched no further reflections are generated and the line has reached its steady state condition. See Figure 4.

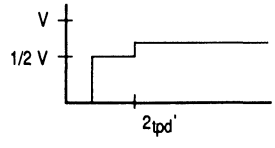


Figure 4. Voltage versus Time Plot of $Z_L = 4 * Z_O$ and $Z_S = Z_O$

The next scenario is when $Z_L < Z_O$. For this case assume the following conditions. $Z_L = Z_O/4$ and $Z_S = Z_O$. See Figure 5.

$$\rho_L = \frac{.25Z_O - Z_O}{.25Z_O + Z_O} = -0.6$$

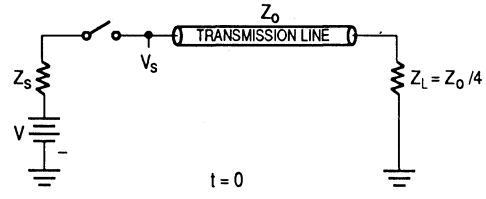


Figure 5. Transmission Line Circuit with $Z_L = Z_O / 4$ and $Z_S = Z_O$

At time t = 0 a voltage wave equal in magnitude to 1/2V begins to travel down the line arriving at the load one delay time later. The impedance mismatch generates a reflected wave equal in magnitude to the reflected wave discussed in the first example, but opposite in polarity. At time $2t_{pd}$ this wave reaches the source and sums with the existing voltage present from time t = 0 (V/2), reducing its value to $V_S/5$ or ((V/2)(–0.6) + V/2). This is the classic undershoot condition. See Figure 6.

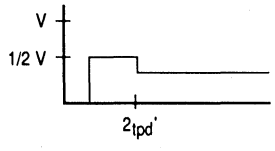


Figure 6. Voltage versus Time Plot of $Z_L = Z_O/4$ and $Z_S = Z_O$

At this point we need to reflect on one of the equations described earlier. The equation states that $V_L = V_{INC} + V_{RFL}$. We can see this holds true as noted In the preceding examples, where V_L and V_S either increased or decreased with corresponding mismatches in impedance.

THE LATTICE DIAGRAM

The lattice diagram permits a network to be checked quickly for balance (match). The diagram is essentially a two-line graph with corresponding source and load impedance, connected by a reflection diagonal with a period of $2t_{pd}$ (twice the line delay time). This diagonal is used to represent the reflected voltage's magnitude. See Figure 7.

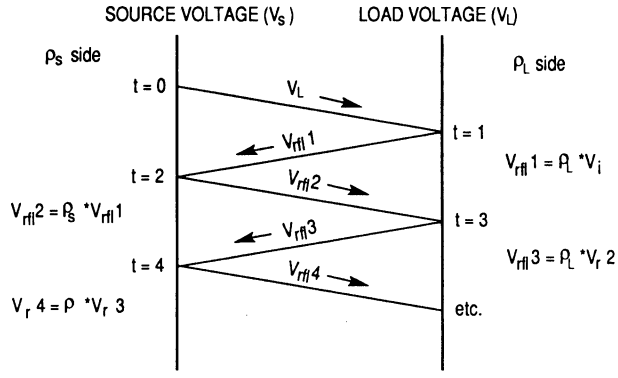


Figure 7. Lattice Diagram

The example below will illustrate the use of the lattice diagram. For the analysis assume the following circuit (see Figure 8 and 9).

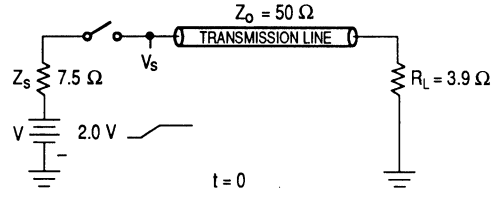


Figure 8. Transmission Line Circuit for Z_S = 7.5 Ω, Z_O = 50 Ω and Z_L = 3.9 Ω

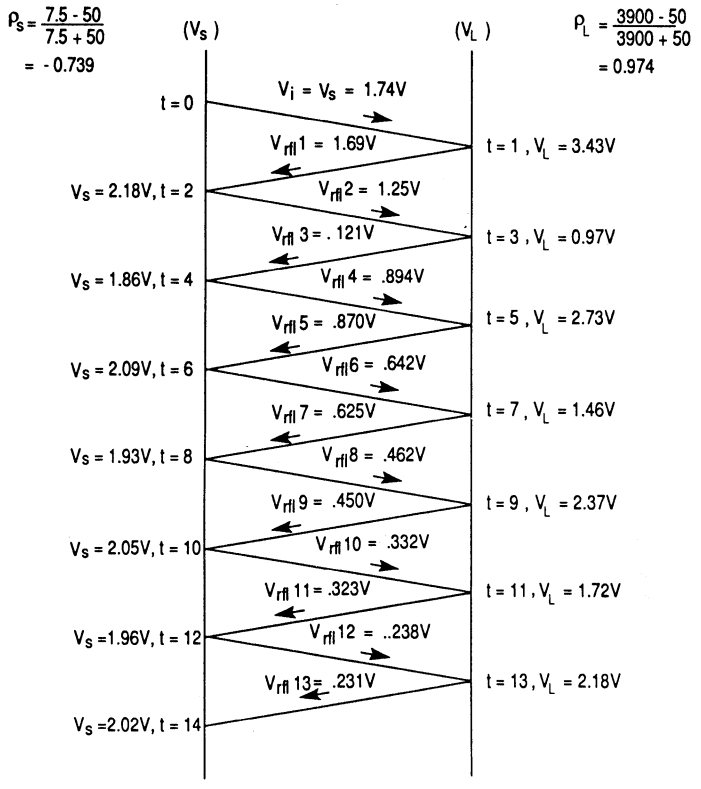


Figure 9. Lattice Diagram for ZS = 7.5 Ω, Zo = 50 Ω and ZL = 3.9 Ω

Transmission Line Types

There are essentially two types of transmission lines; the microstrip and the stripline. The microstrip is shown in Figure 10. It consists of a conductor separated from the ground plane on one side by a dielectric.

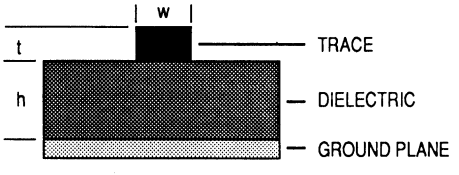


FIGURE 10. Microstrip Transmission Line

The characteristic impedance of a one ounce line configured as a microstrip on G–10 fiber glass is:

$$Z_O = \frac{87}{\sqrt{E_R + 1.41}} * \frac{Ln(5.98h)}{(0.8w + t)} \quad (6)$$

t = 0.0015 in. for 1 oz copper
= 0.0030 in. for 2 oz copper
h = 0.062 in. for G–10 glass epoxy
w = design dependent (based on current handling requirements.) = 0.015 in.

For our discussion,

$E_R = 4.7 - 5.3$

For this example, with $E_R = 4.7$, $Z_O = 116.6\ \Omega$

The unloaded propagation delay $t_{pd} = 1.017\sqrt{0.475E_R + 0.67}$ ns/ft = 173 ns/ft.

The stripline is a conductor separated from ground on two sides by a dielectric (see Figure 11).

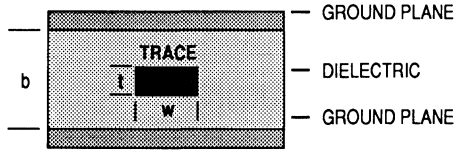


Figure 11. Stripline Transmission Line

The characteristic impedance of G–10 fiber glass board trace configured as a stripline is:

$$Z_O = \frac{60}{\sqrt{E_R}} * Ln\left[\frac{4b}{067\pi\ (0.8w + h)}\right] \quad (7)$$

Using the same parameters as above we find that $Z_O = 60\ \Omega$. The propagation delay = $1.017\sqrt{E_R}$ = 2.20 ns/ft

Loaded Transmission Line Propagation Delay and Impedance

As stated earlier the unloaded propagation of a microstrip line is:

$$t_{pd} = 1.107\sqrt{0.475E_R + 0.67} \text{ ns/ft}$$

This delay increases with capacitive loading. The increase is equal to $\sqrt{1 + C_D/C_O}$ where C_D is the distributed capacitance and C_O is the intrinsic capacitance of the line. C_O is obtained from Figure 3–8 of Reference 1, or alternatively it can be calculated as $C_O = t_{pd}/Z_O$. For the micro strip described above with thickness (h) of 0.062 in, and signal trace width of 0.015 in, C_O = 15 pf. Assuming this line is loaded with five 10 pf loads the loaded propagation delay becomes:

$$(1.73\text{ns})\sqrt{1 + 50/15} = 3/60 \text{ ns/ft}$$

The loaded line impedance $Z_O' = Z_O/\sqrt{1 + C_D/C_O} = 116.6/2.08 = 56\ \Omega$.

For the stripline discussed above there is a corresponding increase in t_{pd} and Z_O.

The loaded propagation delay $t_{pd}' = 2.2\sqrt{1 + 50/15} = 4.57$ ns/ft, while the loaded impedance $Z_{O'} = 60/\sqrt{1 + 50/15} = 28.8\ \Omega$.

It is apparent that capacitive loading increases the propagation delay of the line while decreasing its impedance.

TRANSMISSION LINE TERMINATION

No discussion about transmission lines would be complete without examining the techniques to properly terminate a line. Essentially there are three (3) methods which can be employed. They are:

1) Unterminated line (controlling board parameters to match line and load impedance).
2) Series termination.
3) Parallel termination.

Unterminated Line Method

This method involves controlling the length of the line such that any reflections caused by the load are absorbed by the rise and fall time, t_r and t_f of the driving gate. For this method to be effective the propagation delay (loaded delay) of the line must be short relative to t_r and t_f. This allows the reflected wave to sum with the rising or falling driving gate waveform. If four times the propagation delay of the line is less than or equal to t_r or t_f, then minimal ringing (overshoot, undershoot) will be observed. Specifications for t_r and t_f for various logic families are readily available. Knowing these times one can set the maximum

line length such that the lines $t_{pd}' <= t_r/4$. For distributed loads that are stubbed, the length of the stub should be set to minimize any reflections. A t_r/t_{pd}' ratio greater than 8:1 should suffice.

Series Termination

In series termination a resistance is inserted between the driving gate output and the line. The combined output impedance of the driving gate plus the added series resistance is selected to equal the loaded impedance of the line. Since the input impedance of the driven gate is much greater than Z_O, the line will ring. Basically this termination configuration will ring once and reach steady state within $2t_{pd}'$. End of line loading, (lumped loading) is the only method of loading that is recommended for this type of termination. This is because any distributed load on the line "sees" a voltage equal to v/2 until steady state. This condition could violate the valid V_{IH} or V_{IL} specification of these gates. Clearly distributed loads are to be avoided. Receivers at the end of the line will not experience this condition, as the incident voltage and the reflected voltage add together to equal the load voltage (V_L) one t_{pd}' after the signal is asserted.

Parallel Termination

In the parallel termination method two resistors are placed at the end of the line. One resistor from the line to ground, and the other from the line to VCC. The parallel combination of these resistors is set to be equal to the loaded impedance of the line. For example, if Z_O' of the line is equal to 50 Ω, then the parallel combination of both resistors should equal 50 Ω. Note this method of termination requires more drive current. The driver selected must be able to handle the additional load placed upon it by the added parallel load. Also it is apparent that this method of termination consumes power even in the steady state, as an additional current path has been set up between V_{CC} and ground.

A PRACTICAL EXAMPLE

Upon completing the paper design for our new project, we begin to peruse our schematics for possible transmission line problems. For the purposes of our discussion assume the following configuration:

V_{CC}	5 volts
PC trace	microstrip configuration, G–10 fiber glass, 1 oz copper, E_R = 4.7, w = 0.015, t = 0.0015, h = 0.062
Logic family:	Fast TTL (drive and receive side of line)
Driving gate:	F241 buffer
$t_f + t_r$ F241:	2 ns (for 50pf lumped load)
Number of loads (F08's):	5 (input capacitance = 5pf/load) (I_{IL} = 600 μa, I_{IH} = 100 μa)
Configuration:	Distributed loads approximately every 2 in. for a total trace length of 10 in.

Procedure

1. Calculate the lines characteristic impedance (Z_O).
   Z_O = same as example described earlier = 116 Ω.
2. Calculate unloaded propagation delay (t_{pd}).
   $t_{pd} = 1.017\sqrt{0.475E_R + 0.67} = 1.73$ ns/ft
3. Calculate the lines intrinsic capacitance (C_O).
   $C_O = t_{pd}/Z_O$ expressed as nf/ft
   C_O = (1.73 ns/ft)/116 = 15p f/ft = 1.25 pf/in. * 10 in. = 12.5 pf
4. Calculate the loaded line impedance (Z_O')
   $Z_O' = 116\sqrt{1.25/12.5} = 67\ \Omega$
5. Calculate the lines loaded propagation delay (tpd')
   $t_{pd}' = 1.73\sqrt{1 + 25/12.5}$
   $t_{pd}' = 3.0$ ns/ft = 0.25 ns/in. * 10in. = 2.5 ns >> $t_r/4$

As described earlier, since the loaded propagation delay of the line exceeds $t_r/4$, we will have to terminate the line. The loads are not lumped at the end of the line, they are distributed. As explained earlier, series termination cannot be used because of the possible threshold violations. For this example we will use parallel termination. The parallel resistor combination will be chosen to match the loaded impedance of the line. Noting the drive current of the F241, (I_{OL} = 64 ma, I_{OH} = 15 ma), we can set the source current resistor equal to:

V_{OH}(min)/((5*100 μa) + $I_{OH}/2$) = 2 V/8 ma = 250 Ω

Note: $I_{OH}/2$ arbitrarily chosen. Value could be reduced if required.

The sink current resistor part of this terminator is equal to 91 Ω. This results in a drive sink current equal to:

(Number of Loads * I_{IH}) + V – V_{OL}(F241)/91 = 5*600 μa + 5v – .55V/91 Ω = 52 ma

Note: Weight the source side terminator such that both sink and source current specification are not violated. As shown the parallel combination of the terminating resistors is set equal to the loaded line impedance. See Figure 12.

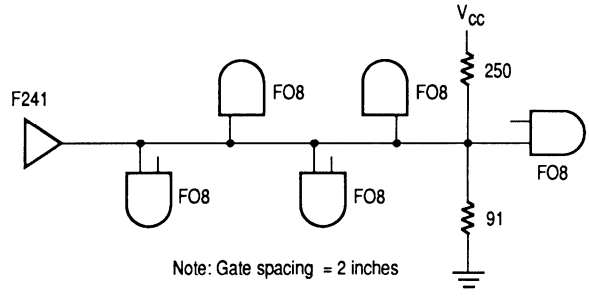


Figure 12. Transmission Line — Example

Since the line is now properly terminated, reflections will be minimized.

In this example, the loads were not stubbed. Had they been located on a stub, an extra calculation would have had to been performed to ascertain the maximum permissible stub length.

This calculation runs as follows:

1. Set $t_r/t_{pd}' = 8.5$ and solve for t_{pd}'
   $t_{pd}' = 2\text{ ns}/8.5 = 235\text{ ps}$
2. Solve for the maximum stub length (x)

   $$235\text{ ps} = 1.73\text{ ns/ft}\sqrt{1 + 5\text{ pf/(x)in.}/1.25\text{ pf/in.}}$$

   $$235\text{ ps} = 144\text{ ps/in.}\sqrt{1 + 4/x}$$

   $$X\,t_{pd} = 1.017\sqrt{0.475E_R + 0.67} = 1.73\text{ ns/ft} = 2.42\text{ in.}$$

REFERENCES

1. *MECL System Design Handbook*, Motorola Inc., 4th ed., 1988.
2. W. Sinnema; *Electronic Transmission Technology*, Prentice-Hall, Englewood Cliffs, New Jersey, 1979.
3. *The Interface Handbook Line Drivers and Receivers Interface*, Fairchild Semiconductor, 1st ed., 1975.

AN1080

External-Sync Power Supply with Universal Input Voltage Range for Monitors

By S.K. Tong and K.T. Cheng

ABSTRACT

This paper describes the design of a low-cost 90 W flyback switching power supply for a multi-sync color monitor. In order to minimize the screen interference from the switching noise, the power supply can be automatically synchronize at the fixed frequency of the horizontal scanning frequency (15 to 32 kHz) of the color monitor. The line and load regulations of the power supply are excellent. Also, a new universal input-voltage adaptor enables the power supply to operate at two input voltage ranges, 90–130 Vac or 180–260 Vac. It can minimize the ripple current requirement of the input bulk capacitors and the stresses on the power switch. The design demonstrates how to use recently introduced components in a low-cost power supply. The state-of-the-art perforated emitter epi-collector bipolar power transistor MJE18004 and opto-isolator MOC8102 are utilized.

1. INTRODUCTION

As the resolution of modern color display increases, the power supply for these high-definition monitors become critical in its features and performance. Nowadays, switching power supplies replace the linear regulators due to high efficiency and light weight. However, the EMI/RFI generated by switching power supplies has adverse effects on the resolution of high-definition color monitors (e.g. 800x600 or higher). Asynchronous switching noise beat with the horizontal scanning frequency of the color monitor, creating undesirable interferences and jitter on the screen. It affects the horizontal resolution of the high-definition color monitor because the random pulses generated by the asynchronous switching operation and also deflect the electron beams and blur their precisely controlled positions. Thus, the switching power supply for the high-definition monitors or TVs must be synchronous with the horizontal frequency.

Recently, multi-sync color monitors became popular because they can adapt to several modes of computer displays. For examples, CGA, EGA and VGA display modes are used in IBM PCs. The three display modes have different horizontal resolutions and scanning frequencies, ranging from 15.7 kHz to 31.5 kHz. Hence, the switching power supply developed in this note can be synchronize to the horizontal scanning frequencies of the multi-sync color monitor, as shown in Figure 1. It provides three d.c. outputs. The specifications are:

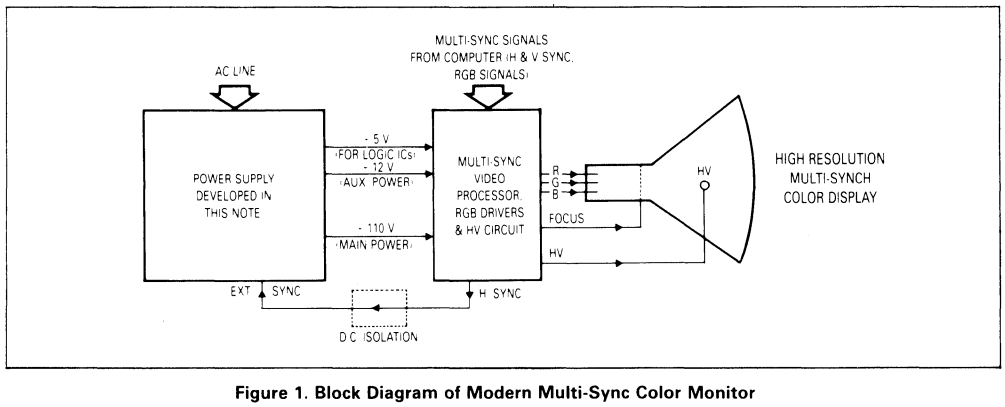


Figure 1. Block Diagram of Modern Multi-Sync Color Monitor

Outputs

+110 V	0.7 A	for HV, RGB drivers and deflection.
+12 V	0.3 A	for auxilary use.
+5 V	0.2 A	for logic ICs.

Inputs

90–130 Vac or 180–260 Vac 50/60 Hz

Power

90 W with overload protection

Conversion Efficiency

Minimum 70% at full load

Others

External synchronization with d.c. isolation (15 kHz to 32 kHz) which are regarded power supply standards for modern color monitors. The two low-voltage outputs are obtained by post-regulators of the +15 V and +8 V inputs.

In Figure 2, the block diagram of the switching power supply, according to the specifications, is shown. Besides the input filter, it mainly consists of three parts — the rectification circuit, the universal input-voltage adaptor and the 90 W flyback converter.

The universal input-voltage adaptor can automatically select the input-voltage range and controls the triac in order to provide the rectified d.c. voltage V_{CC} in between 200 to 370 V. In 90–130 V range, the triac is continuously fired and the whole rectification circuit forms a voltage doubler. In 180–260 V range, the triac turns off and the rectification circuit works as normal. This design can significantly reduce the current ripples of the two smoothing capacitors, C_{in}, and the switching stresses on the power transistor(s) due to wide range of V_{CC}. Some previous designs without the universal adaptor handle the full input-voltage range only by simple bridge rectification. The current ripple of the smoothing capacitors are usually several amperes for 90 W power converters. Furthermore, the output voltage ripple (at V_{CC}) is generally higher for the same value of smoothing capacitors at low line.

In section 2, the design of the flyback converter is reviewed, whereas the design of the universal input-voltage adaptor is given in section 3. Then, in section 4, the performance and further improvements of the power supply are discussed. In the last section, the conclusions include a summary of the design of the power supply and the future developments of switching power converters suitable for multi-sync monitors.

2. DESIGN OF THE FLYBACK POWER SUPPLY

2.1 TOPOLOGY SELECTION

The single-ended discontinuous-mode flyback topology is selected to perform the major power transfer from the rectified output (V_{CC}) to the load. Advantages and disadvantages of this topology are:

Advantages

1. It has smaller transformer size and output choke. The power density and cost of the power supply are lowered.
2. Current mode operation is excellent because the current waveform fed to the current mode controller is strictly triangular. It can improve the noise immunity of the current sensing circuit.
3. Single-pole roll-off characteristic of the power converter simplifies the design of feedback circuits. [1]
4. Simplified in design if single-ended configuration is used.
5. Good cross regulation. [1]
6. The working duty cycle can be greater than 50%. This is particularly important for multi-sync monitor power supply.
7. Lower cost than other topologies.

Disadvantages

1. High RMS and peak transformer currents result in high losses in power switch, windings and voltage clamp.
2. The large air gap in the flyback transformer causes higher EMI/RFI and flux fringe.
3. Higher ripple current appearing in output capacitors produces greater output ripple voltage which may cause screen interference. The switching frequency of the power supply is designed in synchronization with the horizontal frequency. The adverse effect due to this point becomes less significant.

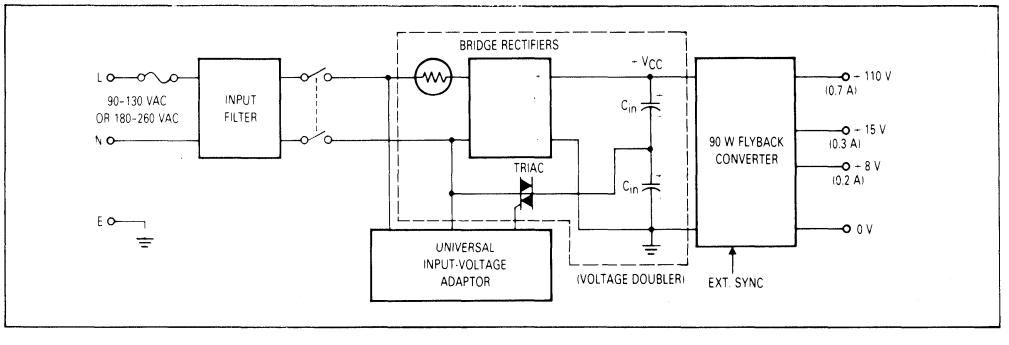


Figure 2. Block Diagram of Switched-Mode Power Supply for Multi-Sync Monitor

4. Transformer and snubber capacitor ring after the magnetic energy stored in the magnetic core is completely released. This phenomenon can be often found in the previous designs.

With the considerations of cost effectiveness, size, and cross regulations, flyback topology is selected. It is particularly suitable for 90 W switching power converter application. Disadvantages are minimized through careful design (see later).

Current-mode control is employed in this power supply because:

1. Inherent line ripple rejection ($\delta V_O/\delta V_{CC} = 0$)
2. Eliminate the possible double-pole characteristics in continuous mode. This would cause instability of the power supply under some critical conditions.
3. Discontinuous mode flyback topology has excellent current mode operation due to large current amplitude.
4. Synchronization is easier to implement without greatly affecting the converter performances and circuit configuration.
5. Simple and low cost as commercial current-mode controller IC is available.

UC3842A/3843A, Motorola current mode control IC, is used in the power supply to perform the current mode operation. The feedback from secondary side to primary is through MOC8102, a new Motorola opto-isolator.

2.2 DESIGN OF FLYBACK TRANSFORMER

The lowest value of V_{CC} is assumed to be 200 V, i.e. 50 V below the rectified low-line peak voltage (180 x 1.414 = 255 V), and the highest value is about 370 V. Therefore, the flyback converter shown in Figure 3 should operate within 200–370 Vdc. The total power is 90 W, slightly higher than the sum of all three outputs. The switching frequency is from 15 kHz to 32 kHz with external synchronization.

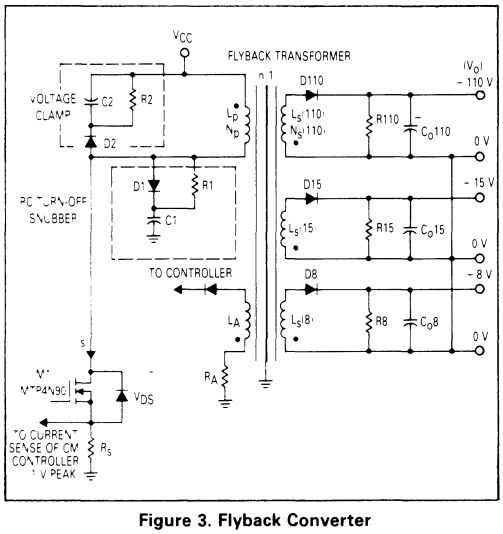


Figure 3. Flyback Converter (Discontinuous Inductor-Current Mode)

If the efficiency is taken into account and it is assumed that the typical conversion efficiency is about 70%, the total input power P_{in} is,

$$P_{in} = 90/0.7 = 128.6 \text{ W}$$

Then, the following problem is how to determine suitable primary inductance L_p and maximum working duty cycle D of the power transistor. Assuming that the primary inductance and input power are constant,

$$P_{in} = L_p I_{pk}^2 f_s/2 \text{ (Energy law)} \quad (1)$$

$$V_{CC} = L_p I_{pk}/t_c \text{ (Faraday's law)} \quad (2)$$

where t_c = conduction time of the switch = DT,
$T = 1/f_s$ = switching period.

Hence,

$$P_{in} = (V_{CC}\, t_c)\, I_{pk}\, f_s/2 = V_{CC}\, I_{pk}\, D/2 \quad (3)$$

If we set D = 0.4 at V_{CC} = 200 V, f_s = 15 kHz and P_{in} = 128.6 W, we have, from (3), I_{pk} = 3.215 A.

The current waveform is shown in Figure 4. Put I_{pk} into (1) or (2), then the primary inductance is calculated to be,

$$L_p = 1.66 \text{ mH}$$

The duty cycle at V_{CC} = 370 V is 0.216 under full-load condition. It becomes smaller as the load decreases. Also from (1), at same power level,

$$\frac{I_{pk} \text{ at } 32 \text{ kHz}}{I_{pk} \text{ at } 15 \text{ kHz}} = \sqrt{\frac{15}{32}} = 0.6847$$

I_{pk} at 32 kHz = (0.6847) (3.215) = 2.2 A

and D_{max} at 32 kHz = 0.4/0.6847 = 0.584

For the flyback converter operating in discontinuous mode at 32 kHz, the duty cycle with respect to secondary side of transformer $D' = t_d/T$ is set to 0.4, which is slightly less than (1–0.584) = 0.416, because the remaining switching time is used to compensate other non-idealities such as leakage inductances, stray capacitances, finite switching fall and rise times, etc. To calculate the secondary inductances, the power relation is used again. If the output power (90 W) was lumped to +110 V output, from (3), at f_s = 32 kHz and V_{CC} = 200 V,

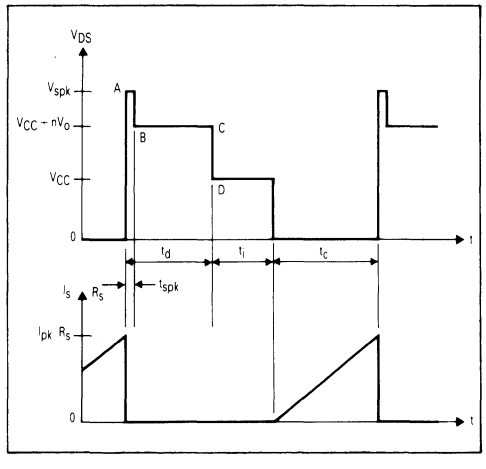


Figure 4. Switching Waveforms of Flyback Converter

P_o = 90 W = V_o I_{pk}' D'/2

where P_o = net output power
V_o = output voltage of +110 V
I_{pk}' = peak inductor current of +110 V windings
D' = t_d/T = 0.4 (referred to Figure 3).

Hence, I_{pk}' = 4.1 A and t_d = 12.5 μs.

Then, substitute I_{pk}' into (1) or (2), we have,

$L_{s(110)}$ = inductance of +110 V winding
= 0.334 mH

And, the inductances of other two windings are,

$L_{s(15)} = L_{s(110)} (16/111)^2$ = 6.9 μH
$L_{s(8)} = L_{s(110)} (9/111)^2$ = 2.2 μH.

The diode drops of the output rectifiers are taken into consideration for the two low-voltage outputs. The turn ratio n is equal to,

$$n = N_p/N_{s(110)} = [L_p/L_{s(110)}]^{1/2} = 2.22 \quad (4)$$

where N_p = number of turns of L_p (primary inductance)
$N_{s(110)}$ = number of turns of $L_{s(110)}$.

Two magnetic cores are found to be suitable for the implementation of the flyback transformer. They are EE40 core and ETD39 core. The spacing factors are just around 0.4 for both. The maximum working flux density B_{max} is set to 0.25T. For EE40 core, the effective cross-sectional area A_e is 130.65 mm^2.

$N_p = (V_{CC}\ t_c)/(B_{max}\ A_e)$ = (200 x 0.4 x 66.67)/(0.25 x 130.65) = 163
$N_{s(110)}$ = 163/2.22 = 73
$N_{s(15)}$ = 11
$N_{s(8)}$ = 6

where $N_{s(15)}$ = number of turns of $L_{s(15)}$, and
$N_{s(8)}$ = number of turns of $L_{s(8)}$.

For ETD39 core, A_e is 124.15 mm^2. The required wire gauges of each winding are also listed in the following. I_{rms} value is equal to $(D/3)^{1/2}\ I_{pk}$. At f_s = 15 kHz, I_{pk}' = 6 A and t_d = 18.2 μs, hence,

D' = 18.2/66.67 = 0.273
N_p = (200 x 0.4 x 66.67)/(0.25 x 124.15)
= 172 $I_{rms} = (0.4/3)^{1/2}$ x 3.215 = 1.17 A (AWG #23)
$N_{s(110)}$ = 77 $I_{rms} = (0.273/3)^{1/2}$ x 2 x 0.7/0.273 = 1.55 A (AWG #22)
$N_{s(15)}$ = 11 I_{rms} = 0.66 A (AMG #26)
$N_{s(8)}$ = 7 I_{rms} = 0.44 A (AWG #26)
N_A = 18 for MTP4N90 and N_A = 13 for MJE18004 (see later).

The ETD39 core will be used in the power supply due to its round bobbin shape and efficient AP product [1]. The temperature rise of the transformer core is about 30°C. To obtain an approximate length of air gap l_g, the calculation is based on:

1. the reluctances of the magnetic core are negligible.
2. the air gap are in the middles of the three limbs, all equal to l_g.
3. the relative permeability μ_r is constant and equals 2000 for TDK H7C4 material.

Hence, $L_p = \mu_o N_p^2 A_e/(2l_g)$ (5)
or l_g = 1.4 mm

But, a 4 mm air gap is used practically to obtain the required inductance due to flux fringe and other non-idealities. The transformer construction diagram is shown in Figure 10. To meet with the world safety regulations (e.g. VDE, UL, CSA, etc.) for the transformer, readers should refer to corresponding regulation books and (4).

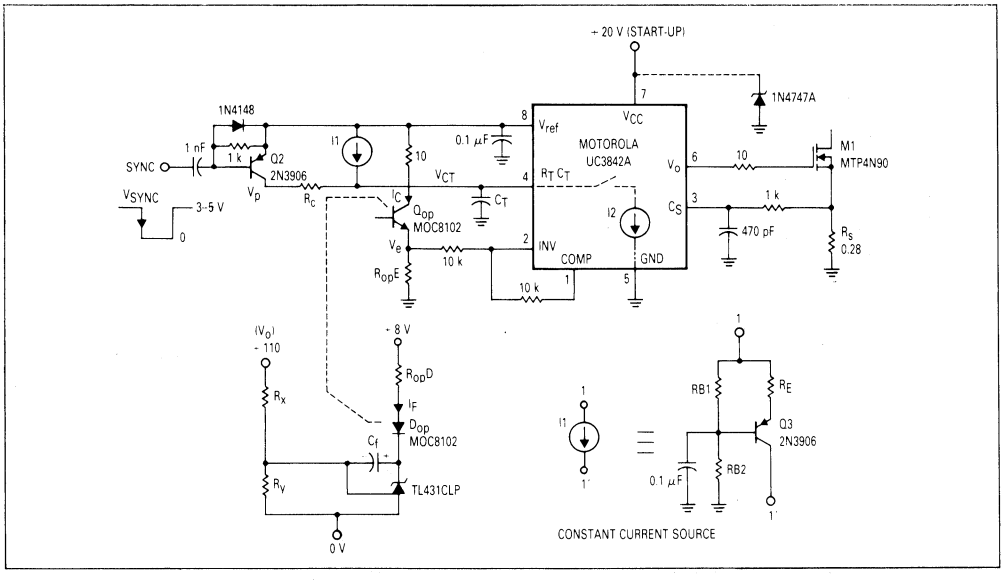


Figure 5a. Current-Mode Controller and Sync Circuit for MTP4N90 (MOSFET)

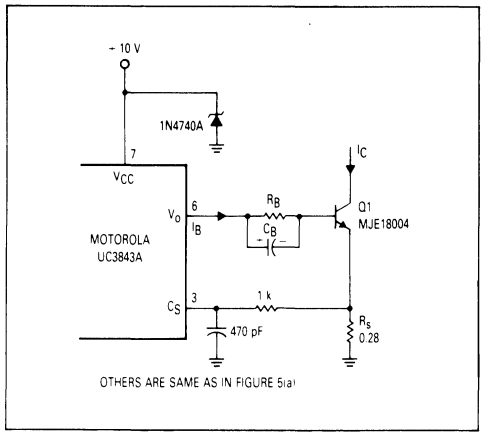


Figure 5b. Current-Mode Controller and Sync Circuit for MJE18004 (Bipolar Junction Transistor)

2.3 DESIGN OF OUTPUT CIRCUITS

The following paragraphs describe how to determine the values of output capacitors and to select output rectifiers as shown in Figure 3. The ultrafast recovery rectifier MUR140 is chosen for D_{110} due to its fast recovery time (75 ns), reliability and low cost. The maximum reverse voltage of this diode is 110 + 370/n = 277 V, so 400 V device is selected. The average current of D_{110} is 0.7 A maximum. D_{15} and D_8 are schottky diodes, MBR160 and 1N5819 respectively, because schottky rectifiers are more suitable for low voltage outputs.

During t_d, the output voltage rises from its minimum value to its peak.

$$V_o = \frac{1}{C_{o(110)}} \int_0^t \left[I_{pk(110)} - \frac{I_{pk(110)}}{t_d} t \right] dt + V_{o(min)}$$

$$= \frac{1}{C_{o(110)}} \left[I_{pk(110)}\, t - \frac{I_{pk(110)}}{2\, t_d} t^2 \right] + V_{o(min)}$$

It consists of a linearly increasing term and a convex parabolic curve. Thus,

$$V_{o(max)} = \frac{1}{C_{o(110)}} \left[I_{pk(110)}\, t - \frac{I_{pk(110)}}{2\, t_d} t^2 \right]_{t=t_d} + V_{o(min)}$$

$$= \frac{1}{2} \frac{I_{pk(110)}\, t_d}{C_{o(110)}} + V_{o(min)}$$

and output ripple voltage is,

$$\delta V_o = V_{o(max)} - V_{o(min)}$$

$$= \frac{1}{2} \frac{I_{pk(110)}\, t_d}{C_{o(110)}}$$

Since the maximum inductor current $I_{pk(110)}$ at 110 V rail is 5.13 A, and the output ripple voltage is maximum at f_s = 15 kHz,

t_d = 0.273 x 66.67 μs = 18.2 μs

t_i = idle time (as shown in Figure 4)

= T − t_c − t_d = 21.8 μs

If the output ripple voltage is set to 1% of V_o, i.e. 1 V,

δV_o = 1 = 0.5 x 5.13 x 18.2/$C_{o(110)}$

$C_{o(110)}$ = 46.68 μF

However, the output ripple current (1.55 A) is so large that two or more capacitors are needed to be connected in parallel in order to lower their individual ripple currents and the additional output ripple caused by ESR and ESL of the output capacitors. As a result, two of 22 μF to 33 μF capacitors each with maximum ripple current of 0.8 A are used in the power supply. Their maximum working voltage is 160 Vdc.

The dummy resistors R_{110}, R_{15} and R_8 are used to maintain minimum load currents of the three outputs. R_{110} is set to 5.6 kΩ and dissipates 2 W.

LC filter is cascaded with each output to lower the output ripple voltage. They are shown in Figure 8. The corner frequency for that at +110 V output is about 6.2 kHz and the approximate output ripple voltage is,

$1/[1 + (15/6.2)^4]^{1/2}$ = 0.1684 V (peak-to-peak).

2.4 SELECTION OF SWITCHING TRANSISTOR, SNUBBERS AND VOLTAGE CLAMP

Two types of power switches are considered for the flyback power supply. They are TMOS power FETs, and the state-of-the-art perforated emitter bipolar transistors introduced in 1988. The new series of Motorola TMOS FETs simplifies the design of driving circuits and provides extremely fast switching transitions. These MOSFETs can operate in the MHz range. In this power supply, although the switching frequency is relatively low, it still provides several advantages such as simple drive circuit, less supply current for the MOS driver, fast switching times which result in less energy loss at switching transitions, and hence a smaller value of snubber capacitor C_1 (1000 pF) is required. Since the maximum drain voltage of M_1 is near 850 V (see later), and the peak drain current is 3.2 A, MTP4N90 is selected for M_1, with 4 Ω $r_{DS(on)}$ [5]. Thus, the approximate conduction loss in M_1 is $[(0.4/3)^{1/2} \times 3.2]^2 \times 4$ = 5.5 W at f_s = 15 kHz, V_{CC} = 200 V and full load. The power dissipation is well below the maximum power that can be dissipated by the device.

To demonstrate the switching improvement of the newly introduced perforated-emitter BJT family, the design of the flyback power supply also provides an alternative for a new device. MJE18004 is chosen for M_1 because its breakdown voltage $V_{(BR)CES}$ is above 1000 V, the continuous collector current is 5 A and its switching times are excellent for switchers below 70 kHz (t_{fi} = 70 ns and t_{si} = 0.6 μs at I_C = 2 A, I_{b1} = 250 mA and $V_{BE(off)}$ = −5 V) [6]. Another two important features are its lower cost and power loss than the MOSFET. Its performance is quite different from the previous bipolar transistors. For the triple diffused power transistors, which are still widely used in Japan (e.g. BU508), these devices face three major problems: long switching times, dispersion of device characteristics, and h_{FE} degradations after several thousand operating hours. The epi-collector technologies which MJE18004 uses, improve the switching speed and control of device characteristics. Since the emitter of BJT affects the device performance very much, various emitter structures have evolved. With

Motorola SWITCHMODE III, with hollow emitter structure, the speed and RBSOA improvements are accompanied by the increased die size (about 125% of standard technology). For the perforated emitter structure, the emitter is interleaved by the base, thus, this increases the emitter perimeter to area ratio. That means higher speed switching transistor can be fabricated in a smaller die size. It improves the operating frequencies and lowers the cost.

In Figure 3, a dissipated RC turn-off snubber is shown. Its function is to reduce the power loss of the transistor M_1 at turn-off by limiting the rising slope of V_{DS}. It is also called the dV/dt limiter. When M_1 turns off, the inductor current begins to commutate from the power switch to the snubber capacitor C_1 through the diode D_1 within t_{fi}. The snubber capacitor slows down the increasing rate of V_{DS}, so the V_{DS} I_s product area (during cross-over time) can be limited to certain acceptable value. This snubber is particularly important for the old and slow bipolar transistors. With the advents of TMOS FETs and perforated emitter bipolar power transistors, the snubber capacitance can be chosen to be as low as 1000 pF. As the current fall-time of power transistor given in data sheets includes the effect of transistor output capacitance (C_{oss}), it is difficult to calculate an optimum value of C_1 which requires the fall-time information without the effect of C_{oss} [2],[3].

Theoretically, the charge stored in C_1 at turn-off should be completely dissipated in R_1 when the switch M_1 turns on. However, in the discontinuous-mode flyback power supply, it cannot always have that because severe stray oscillation which is caused by L_p and C_1 occurs when the energy stored in the magnetic core is completely discharged to the loads. This phenomenon is often seen in previous designs. Therefore, the resistor R_1 has another function that it acts as a damper for the L_p-C_1 resonant circuit. Then, a compromise between the two opposing operations should be considered. For a series LCR resonant circuit, the damping ratio can be used to control the envelope of the damped sinusoidal oscillation. From any standard text on linear control systems,

$$\text{Damping ratio} = \frac{R_1}{2}\sqrt{\frac{C_1}{L_p}} \qquad (7)$$

If the damping ratio is set to 1, no undershoot below V_{CC} will result.

Thus,

$$1 = 0.5 \times R_1 \times (1000p/1.66m)^{1/2} \text{ or } R_1 = 2.58\ k\Omega$$

In practice, a smaller value of R_1 will increase the discharge rate of C_1 at turn-on. So, a standard value of 2.4 kΩ is used. The maximum power dissipation of R_1 is equal to C_1 $V_{CC(max)}^2$ $f_{s(max)}/2$ = 2.2 W, for complete discharge of C_1 during the conduction time of M_1. But, due to the stray oscillation caused by C_1, L_p and R_1, the resistor R_1 should have a power dissipation of 3 W.

Another RC snubber of 180 Ω and 470 pF used in the power supply is to damp the stray oscillation caused by the junction capacitance of D_{110} and the leakage inductance [2].

In Figure 4, a high-voltage spike (point A) in V_{DS} is caused by the discharge of leakage magnetic energy in the transformer. The time between A and B represents this period. Since the discontinuous-mode flyback converter has greater peak inductor current, the effect of leakage inductance can be the dominant source of power loss. As shown in Figure 3, a voltage clamp for the leakage inductance limits the spike voltage to a designated value, V_{spk}. In [3], it points out that voltage clamp is more effective than shunt snubber in limiting the spike voltage. It is actually a boost converter with an input voltage of approximately nV_o and the leakage inductance as switching inductor. From power relation, neglecting the minor effect of the shunt RC snubber,

$$L_3 I_{pk}^2 f_s/2 + nV_o t_{spk} f_s I_{pk}/2 = (V_{spk} - V_{CC})^2/R_2$$

for $C_2R_2 \gg 1/f_s$

and from Faraday's law,

$$I_{pk} L_3/(V_{spk} - V_{CC} - nV_o) = t_{spk}$$

where L_3 = leakage inductance in primary side. On substitution,

$$\frac{1}{2} L_3 I_{pk}^2 f_s \left[1 + \frac{nV_o}{V_{spk} - V_{CC} - nV_o}\right] = \frac{(V_{spk} - V_{CC})^2}{R_2} \qquad (8)$$

Note that although the above result is similar to that shown in [3], the leakage inductance which stores energy to be dissipated is merely L_3, and the leakage inductances in the secondary side only come into effect between point A and B in Figure 4. The power loss due to L_3 is essentially same for all switching frequencies because $I_{pk}^2 f_s$ is constant for same power level and V_{CC}. At 15 kHz, the primary inductance was measured to be 0.15 mH with major secondary winding (110 V output) short-circuited at zero bias current. It is about one-tenth of L_p. So, L_3 is equal to 0.15 mH/2 = 75 μH. If the peak voltage of M_1 is limited to 850 V for MTP4N90, then,

$$0.5 \times 75\ \mu \times 3.2^2 \times 15\ k \times [1 + 244/(850\text{-}370\text{-}244)] = (850 - 370)^2/R_2$$

$$R_2 = 19.67\ k\Omega\ (11.7\ W)$$

For MJE18004, V_{spk} is limited to 950 V and R_2 = 33.8 kΩ (9.95 W). Practical values of 20 kΩ (10 W) and 33 kΩ (10 W) are used for MTP4N90 and MJE18004, respectively.

2.5 CONTROL, BASE DRIVE AND EXTERNAL SYNC CIRCUITS

The current-mode control IC selected is the UC3842A or UC3843A. For MOSFET, MTP4N90, UC3842A is used to provide sufficient gate voltage because it is operated at 20 V. The circuit configuration is shown in Figure 5(a). The maximum current-sense (CS) voltage on pin 3 of UC3842A is 0.9 V (minimum) [9]. Hence, the current sensing resistor R_S is 0.9/3.2 = 0.28 Ω with power dissipation less than 0.5 W. Three 1 Ω (1/4 W) and one 2.2 Ω (1/4 W) are connected in parallel to obtain the required resistance. A RC filter (1 kΩ and 470 pF) is added to "kill" the voltage spikes. The corner frequency of the filter is 339 kHz.

To be able to synchronize externally, the power supply must have a free-running frequency below 15 kHz. For the simplification of the design and operation of the oscillation in UC3842A, a constant current source I_1 is used instead of a resistor R_T. Since the internal current source I_2 in UC3842A provides a discharging current of 8.4 mA,

the dead time t_2 and switching frequency can be determined as follows.

$$I_1 = C_T \frac{1.6}{t_1} \text{ and } I_2 - I_1 = C_T \frac{1.6}{t_2} \qquad (I_2 > I_1)$$

$$\frac{I_2 - I_1}{I_1} = \frac{t_1}{t_2} \qquad (9)$$

$$T = t_1 + t_2 = 1/f_s$$

The hysteresis voltage of the oscillator is 1.6 V. The time periods t_1 and t_2 are the rise and fall times of the triangular waveforms (V_{CT}). Due to the effect of leakage inductance, other parasitics and snubber circuits at f_s = 32 kHz, the dead time t_2 is set to 6–8 μs. Then, if the free-running frequency is assumed to be 12.5 kHz, $t_1/T = 0.91$,

$$\frac{I_2 - I_1}{I_1} = \frac{0.91}{1 - 0.91}$$

or I_1 = 0.756 mA and C_T = 0.036 μF

The constant current source I_1 is implemented using a single PNP transistor Q_3. The current gain of 2N3906 is about 200. The current through R_{B1} and R_{B2} is assumed to be 20 x I_{B3}, and the emitter voltage is set to 4 V since the peak voltage of V_{CT} is 3 V. Then, we have,

$R_E = 1/I_1 = 1.32\ k\Omega$

and I_{B3} = 0.756 mA/200 ≈ 4 μA.

Since $V_{B3} = 5 - 1 - 0.7 = 3.3$ V,

$5 \times R_{B2}/(R_{B1} + R_{B2}) = 3.3$

$R_{B1}/R_{B2} = 0.515$

$R_{B1} \approx 20\ k\Omega$ and $R_{B2} \approx 39\ k\Omega$

The practical values for R_E and C_T are 1.2 kΩ and 39 nF, and the free-running switching frequency is around 13 kHz. The constant current source I_1 can be directly replaced by Motorola current regulating diode (1N5294), which is a JFET with gate-source short-circuited. The regulated output current is actually its saturation current I_{DSS} at pinch-off.

The external synchronization is achieved by the one-shot triggering circuit built around Q_2. It is active once when the falling edge of sync pulse appears. Then, a single high pulse of 2 to 3 μs charges the timing capacitor C_T through the charging resistor R_C at a very fast rate (about 50–100 times the normal rate). The value of R_C can be calculated by,

$(5 - 2.8 - 0.5) / (100 \times 0.756) \approx 47\ \Omega$

The minimum voltage drop on R_C is approximately 5 − 2.8 − 0.5 = 1.7 V because V_{CT} swings between 1.2 to 2.8 V, with respect to ground [9], and the saturation voltage of Q_2 is about 0.5 V. The choices of the input capacitance and BE resistance can vary the pulse period. The anti-parallel BE diode, 1N4148 is to prevent the BE junction from possible avalanche breakdown if the amplitude of V_{sync} is above 5 V.

It is also possible to combine the sync circuit into the constant current source by injecting the sync signal into the base of the current source transistor.

The feedback scheme is selected as follows. A voltage reference with comparator (linear error amplifier) TL431 detects and amplifies the error signal, and drives the LED of the opto-coupler MOC8102. The gain of the error amplifier (EA) in UC3842A is set to unity for better noise immunity and stability. Since the output voltage of the error amplifier is from 1.4 (two diode drops) to 4.1 V (1.4 + 0.3 x 3) typically [9], and V_e is equal to (5 — output voltage of EA), the voltage V_e across R_{opE} is from 0.9 to 3.6 V.

In the past opto-couplers have suffered from current transfer ratio (CTR) degradation. The main cause for CTR degradation is the reduction in efficiency of the LED within the opto-coupler due to the increase in space-charge recombination within the diode. Past industry LED burn-in data under accelerated conditions indicated that a 15% to 20% degradation after 1000 hours was not unusual. Of even more concern was the fact that the population also contained "fliers" units through infant mortality mechanisms eventually exhibited degradations approximately 50%. A typical percentage degradation is 40% after 10^5 hours normal operation at I_f = 25 mA. In 1987, Motorola's Optoelectronics Operation decided to resolve the industry-wide problem of LED light output degradation. They concentrated their efforts to improve and control certain critical LED wafer processing steps and eventually, 5000 hours of accelerated stress burn-in testing shows zero degradation. This means that low degradation characteristics are now achieveable not only on an average (mean) basis, but also that "fliers" can be eliminated. Therefore, the opto-isolator can be regarded as a low-cost, reliable, simple but high performance component to be used in future power supplies. Besides the zero degradation of CTR, the new MOC810X series opto-coupler that are specifically designed for switching power supplies provides two additional features. Their specifications include tightly controlled window values of CTR. Also, each device's internal base connection has been eliminated, effectively minimizing the noise susceptibility problem. Noise is further minimized by coplanar die placement, which puts the LED and phototransistor end-to-end, rather than one above the other. The result is a mere 0.2 pF coupled capacitance, which minimizes the amount of capacitively coupled noise that is injected by the optoisolator.

MOC8102 is selected due to its moderate CTR (from 0.73 to 1.17 at I_F = 10 mA) [11]. Then, two extreme cases are considered. For the lowest I_f delivered by TL431, it should provide sufficient coupled current to develop a minimum voltage of 0.9 V on R_{opE}. The operating current range of I_f is chosen to be 0.5 to 20 mA. For the highest limit of the selected I_f range, i.e. 20 mA, the value of R_{opE} is 3.6 V/0.5 x 20 mA) = 360 Ω, if CTR is at the lowest value, i.e. 0.5 approximately. Then, nearly whole ranges of CTR and I_f are covered by the design with R_{opE} equal to 360 Ω. The practical value for R_{opE} is selected to be 390 Ω. For the determination of R_{opD}, the maximum LED current is considered. Thus, the value of R_{opD} is (8 − 1) V/20 mA = 350 Ω. A 330 Ω resistor is used in practice.

The feedback point is directly taken from the positive terminal of the output capacitors $C_{O(110)}$. This point must be placed before the output LC filter because the filter forms an additional double-pole in the feedback loop. Since the internal reference voltage of TL431 is 2.5 V, the values of R_x and R_y (the voltage divider) are chosen to be R_x = 142 kΩ and R_y = 3.3 kΩ because, 110 $R_y/(R_x + R_y)$ = 2.5 or R_x/R_y = 43 .

The gate drive circuit consists of a series 10 Ω resistor to minimize the "gate ring" problem. But for MJE18004, the base drive circuit is not as simple as that for MOSFET. It is shown in Figure 5(b). The supply voltage of the current-mode controller is lowered to 10 V in order to minimize the power loss in base drive circuit, and meanwhile, UC3843A is used instead of UC3842A, which has a lower ON threshold of supply voltage. Other functions are identical to UC3842A. The typical h_{FE} value for MJE18004 is 14 [6], and thus, it is assumed that the minimum h_{FE} value is 10 partly because of the tight control in manufacture. Then, the minimum base current I_B is 3.2/10 = 0.32 A to maintain transistor saturation at full load. A slightly larger base current of 0.35 A is used practically. From [9], the voltage drop on the source output transistor of UC3843A is about 2 V at an output current of 0.35 A. And the value of $V_{BE(sat)}$ of MJE18004 is 0.95 V [6]. Therefore, the value of base resistor R_B is,

$$R_B = (10 - 0.95 - 2)/0.35 = 20\ \Omega \quad (1.2\ W)$$

The base drive capacitor C_B can be determined by $1/(2\pi C_B R_B) \leq f_{s(min)}/2$, i.e. $C_B \approx 1\ \mu F$. Note that the BE junction of MJE18004 will not have avalanche breakdown because the breakdown voltage of BE junction is about 9 V. Other optimum base drive circuits can be found in [7] (e.g., how to use base inductor to improve the turn-off operation of power transistor).

As shown in Figures 3 and 5, the primary control circuitry is self-supplied. The required power is delivered from the transformer winding N_A through D_A and R_A. A zener diode of appropriate voltage rating is used to regulate the supply voltage for IC_1. For UC3842A and MTP4N90, the supply voltage is 20 V and the total supply current is about 20 to 50 mA. Thus, N_A is chosen to be 18 turns to provide an extra 5 V for regulation. R_A is set to 47 Ω. Th smoothing capacitor C_A is for filtering, but an unobvious effect of its capacitance is on the start-up transients of the primary control circuitry. Since the current-mode controller UC3842A/3843A has a voltage hysteresis in under-volt lockout, the capacitance of C_A must be large enough to maintain the initial switching operations, i.e. the supply voltage must be kept above the lower threshold point, before the power can be fed from the transformer. The practical values of C_A are 3.3 μF for UC3842A and 2200 μF for UC3843A. The much larger capacitance used in the latter case is due to the small hysteresis of the supply voltage of UC3843A and the relatively large base current. N_A and R_A for MJE18004 are 13 turns and 10 Ω (1 W) respectively.

It is also possible to minimize the value of C_A to several μF and to avoid long start time using a "kick" starter described in previous Motorola Application Notes. The "kick" starter is actually a NPN high voltage, small-power transistor connected as a simple voltage regulator for the control circuit. The reference voltage is derived from a zener diode biased by a resistor connected across $+V_{CC}$ and the base of the "kick" transistor. Its emitter is regarded as output of the regulator and its collector can be tied to $+V_{CC}$. When the power supply is connected to a.c. mains, the "kick" starter charges C_A above the start-up threshold of UC3842A/3843A quickly. Then, the power for the control circuitry is fed from the auxiliary windings (N_A), which raises the d.c. voltage at the emitter of the "kick" transistor, and the transistor will be turned off. Thus, the "kick" transistor conducts for a very short time and dissipates very small power.

2.6 CLOSING THE FEEDBACK LOOP

After determination of almost all the component values and configurations for the flyback power supply, the last but not the least piece to design is the feedback loop. Figure 6(a) shows the gain-block diagram of the flyback power supply. The input of the system is the internal reference voltage in the TL431, which is 2.5 V ± 1%, and is compared to the feedback signal. The H-block is purely

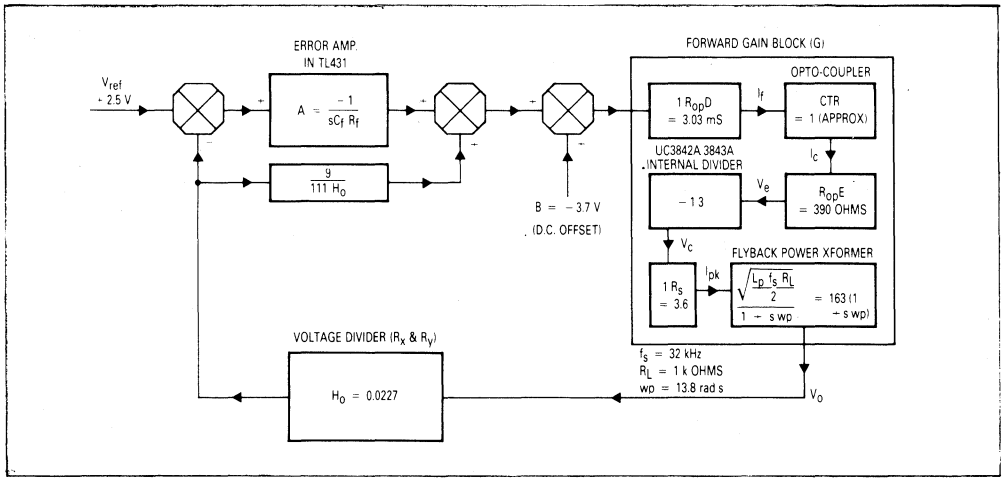


Figure 6a. Approximate d.c. and Low-Frequency a.c. Model of the Flyback Power Supply

a voltage divider formed by R_X and R_Y, thus the gain value in this block is $3.3/(142 + 3.3) = 0.0227 = H_O$. The difference or error signal is then amplified by the error amplifier in TL431, which is compensated externally. The compensation network is chosen to consist of an integrating capacitor C_f and a resistor R_f. Thus, we have,

$$A \approx \frac{-1}{sC_fR_f} \qquad (10)$$

where s = Laplace transform operator (jw for sinusoidal analysis),

$R_f = R_XR_Y/(R_X + R_Y) = 3.23\ k\Omega$.

The capacitance value of C_f can be determined for overall stability of the power supply once when the forward gain G is known under the worst condition.

The low-frequency a.c. model for the discontinuous-mode current-injected flyback converter consists of a d.c. gain block cascaded with a single-pole roll-off network which has a pole frequency at $1/(\pi C_OR_L)$, where C_O is the total output capacitance and R_L is the total load resistance at V_O [1]. The equivalent maximum load resistance $R_{L(max)}$ is approximated by experimental measurements at no load, f_s = 32 kHz and V_{CC} = 200 V (for MTP4N90). The input current was measured to be 0.06 A and thus,

$R_{L(max)} \approx 110^2/(200 \times 0.06) \approx 1\ k\Omega$

For the equivalent total output capacitance (for MTP4N90), the capacitances at three output circuits are lumped to +110 V output, and by charge relation,

$C_O = [(110\ V)\ (66\ \mu F) + (15\ V)\ (330\ \mu F) + (8\ V)\ (470\ \mu)]\ 110\ V \approx 145\ \mu F$

Hence, the lowest corner frequency f_P of the flyback power supply is approximately 2.2 Hz. If the ESR and ESL of the output capacitors are neglected, the G-block has a transfer function [1] as,

$$G = G_O\ (1 - s\ W_P) \qquad (11)$$

where $W_P = 2\pi f_P = 13.8$ rad s.

The forward gain block G is subdivided into its individual elemental blocks in Figure 6(a). They are the resistor R_{OPD} which converts the output voltage of TL431 into the diode current for the LED of MOC8102, the non-linear CTR (0.65 to 4.5 from data sheet), the resistor R_{OPE} which generates a voltage V_e from the coupled current I_C, the internal one-third divider of UC3842A/3843A (the minus sign is due to the inverting configuration of the op amp), the current sensing resistor R_S which relates V_C to I_{pk}, and finally, the gain of the power stage which includes the signal pole. The d.c. gain of the power stage can be directly derived from the power relation.

$$\frac{V_O^2}{R_L} = \frac{1}{2} L_P I_{pk}^2 f_s$$

$$\text{or } \frac{V_O}{I_{pk}} = \sqrt{\frac{L_P R_L f_s}{2}}$$

Thus,

$$G_O = \frac{-(R_{OPE}/R_{OPD})}{3 R_S} (CTR) \sqrt{\frac{R_L L_P f_s}{2}} \qquad (12)$$

The value of d.c. gain G_O can be determined analytically by substituting parameters under worst case, i.e. f_s = 32 kHz and R_L = 1 kΩ (including +8 V and +15 V rails), when the value of G_O is highest. On substituting the known parameters,

$R_{OPE} = 390\ \Omega$ $R_{OPD} = 330\ \Omega$ CTR = 1 (for MOC8102)
$R_S = 0.28\ \Omega$ $L_P = 1.66$ mH,

we have,

$|G_O|$ = 229 or 47.2 dB

It is observed that a local feedback occurs in the TL431 output circuit and the LED of the opto-coupler. Its end effects are:

1. loop-gain enhancement by the additional block connected in parallel with A-block, i.e. $9/(111\ H_O) = 3.57$;
2. a proportional-integral (PI) controller resulted, instead of a pure integrator.

The overall gain (transconductance) of the feedback error amplifier can be derived as follows.

$i_F = V_O\ (9/111) - V_O\ H_O\ A$
$= [9/(111\ H_O) - A]\ H_O\ V_O$

$$\text{or } i_F/(H_O\ V_O) = 9/(111\ H_O) - A \qquad (13)$$

where v_o = a.c. component of V_O

i_F = a.c. component of I_F (LED current).

To simulate the equation (13), an additional block consisting of $9/(111\ H_O)$ only is placed in Figure 6(a). The zero frequency of the error amplifier is,

$$w_f = 1/(3.57\ C_fR_f) \qquad (14)$$

when $|A| = 9/(111\ H_O)$.

After knowing all equivalent a.c. gains of the converter circuit, we can determine the value of C_f for optimum circuit dynamic performance. Since there is merely one

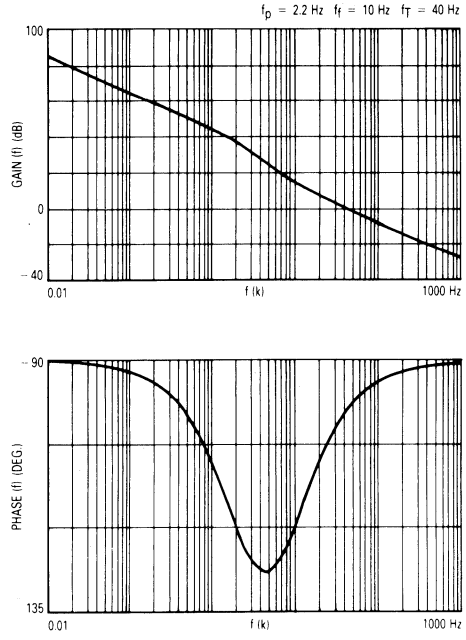


Figure 6b. Bode Plot of the Flyback Converter at f_s = 32 kHz and No Load

parameter that can be varied, i.e. C_f, and only one optimum condition (either gain or phase) can be satisfied, we set the minimum phase of the loop gain to $-120°$ to guarantee the relative stability. That means W_f should be placed 30/45 = 0.667 decade beyond W_p or,

$$W_f = 10^{0.667} W_P$$
$$= 4.64 W_P = 64 \text{ rad/s}$$

because the down slope of the phase of the flyback converter gain is $-45°$/decade and the PI controller has an initial phase shift of $-90°$. Then,

$$C_f = 1/[(3.23 \text{ k}) (3.57) (64)] = 1.355 \ \mu F$$

A practical value of 1.5 μF is used. Plots for the overall loop gain of the power supply at f_s = 32 kHz and minimum load is shown in Figure 6(b), with the following equations.

$$A(f) = \frac{1}{sC_fR_f} + \frac{9}{111 H_O} = \frac{206.4}{jw} + 3.57$$

$$G = \frac{G_O}{1 + s/W_P} \qquad \text{where } G_O = 229, \ W_P = 13.8$$

$$H_O = 0.0227$$

$$\text{Gain } (f) = 0.2 \log_{10} | A' (f) \times G \times H_O |$$

$$\text{Phase } (f) = \text{Arg}[A' (f) \times G \times H_O]$$

The unity gain bandwidth is about 40 Hz (at f_T) and the phase margin is about 82°. But, the dominant value in the phase plot is its lowest value of $-128°$ at w_f, where the gain is greater than 0 dB. It determines nearly all transient load responses.

2.7 OTHER OPTIONS

Under normal circumstances, the output voltage should not exceed 150 V. But, as protection for the monitor circuits (it would generate X-ray if extremely high anode voltage appears), an optional high-voltage zener diode 1N5953A (1 W) is connected across the 110 V output rail. If abnormally high voltage (>150 V) continuously appears on this rail, the zener diode will be zapped to form a permanent short-circuit. Other better OVP circuits such as SCR crowbar circuit and 0 V shutdown circuit can be used with higher unit cost.

Another option which may be required in the power supply is short-circuit (not just overload) protection. Since the flyback power converter is operated with current-mode control, it is inherently over-power protected. But, if the outputs are short-circuited, maximum power will be delivered to the low voltages with high output currents. Then, the output rectifiers and windings are likely to be damaged. Short circuit protection is generally best installed in secondary output(s). Shutdown or foldback signal(s) can be fed to the UC3842A/3843A by a Motorola optocoupler.

To improve and control the start-up transients, a soft-start circuit may be added to the current-mode controller. Typical example can be found in [9].

3. UNIVERSAL INPUT-VOLTAGE ADAPTOR

The universal input-voltage adaptor is used with bridge rectification circuit to provide a rather narrower range of rectified d.c. output voltage at either low or high range of input voltage, i.e. 90–130 Vac or 180–260 Vac. A simplified circuit block diagram has been shown in Figure 2, and the detailed circuits are shown in Figure 7(a) and (b). The voltage range selection is performed by an over-voltage detector and the adaptor is supplied from a charge pump circuit. At low range, the triac is fired continuously by the adaptor, and a voltage doubler is formed, while simple bridge rectification is retained at high range. The rectified output voltage (V_{CC}) range is from 200 to 370 Vdc.

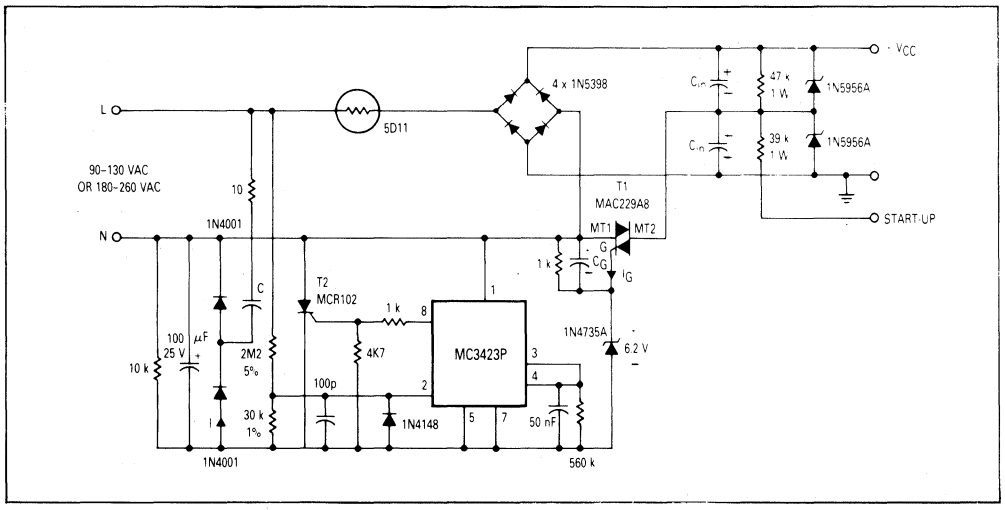


Figure 7a. Negative Gate (Triac) Current — Preferred

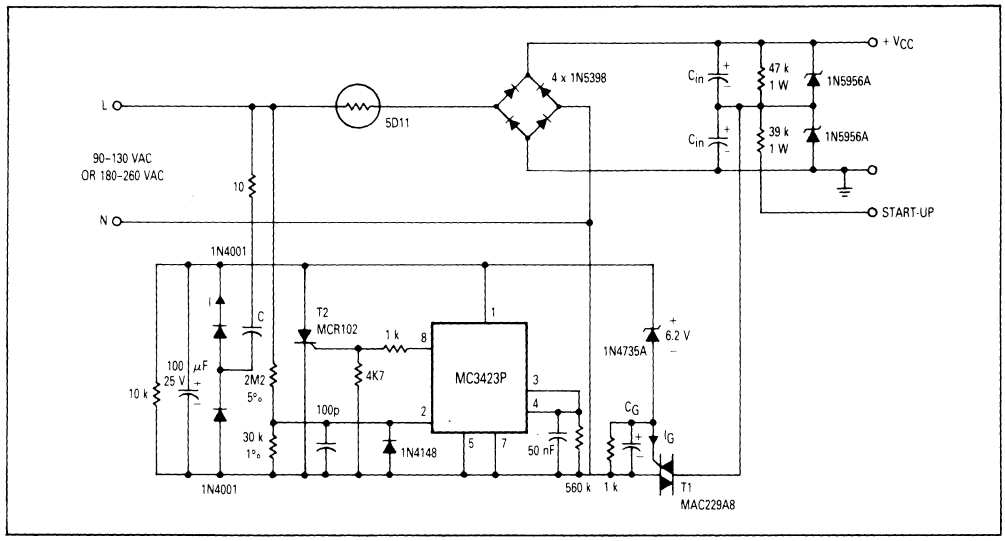


Figure 7b. Positive Gate (Triac) Current

3.1 ADVANTAGES OF USING UNIVERSAL INPUT-VOLTAGE ADAPTOR

Three advantages are gained by using the universal input-voltage adaptor. They are:

1. smaller ripple current in the smoothing bulk capacitors for fixed output power;
2. less output ripple voltage at the rectified d.c. output (V_{CC}) at constant output power;
3. greatly reducing the stresses (voltage and current) on the power switch of the flyback converter for constant output voltage (V_o).

3.2 DETAILS OF CIRCUIT DESIGN

To select a suitable capacitance for the input bulk capacitors C_{in}, the ripple voltage at V_{CC} is considered. Sketches of voltage and current ripples are shown in Figure 7(c) and (d) for the following analysis. Figure 7(c) is for normal bridge rectification, while Figure 7(d) is for voltage doubler.

For simple bridge rectification, the ripple voltage δV_{CC} is related to the capacitance of C_{in} as follows, from the power relation. It applies provided that t_a is much less T/2,

$$P_{in} \approx 1/2\ (C_{in}/2)\ [V_{CC(pk)}{}^2 - V_{CC(min)}{}^2]\ (2f_{in})$$

or

$$C_{in} = \frac{2\ P_{in}}{V_{CC(pk)}{}^2 - V_{CC(min)}{}^2} \frac{1}{f_{in}} \qquad (16)$$

and $\delta V_{CC} = V_{CC(pk)} - V_{CC(min)}$

where $V_{CC(pk)}$ = peak voltage at V_{CC} = 1.414 x input voltage (rms),

$V_{CC(min)}$ = lowest voltage at V_{CC},

f_{in} = frequency of input voltage.

For the worst case, $V_{CC(pk)}$ = 180 x 1.414 = 255 V, $V_{CC(min)}$ = 200 V, P_{in} = 128.6 W and f_{in} = 50 Hz since the lowest working voltage of the flyback power supply is 200 V, and the frequency of input voltage is from 50 Hz to 60 Hz. Therefore,

$$C_{in} = 205.6\ \mu F$$

The time period t_a, the conduction time of the bridge rectifiers, is given by,

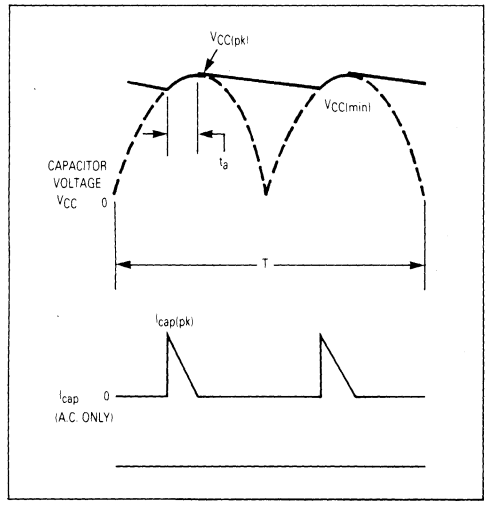


Figure 7c. Waveforms of Bridge Rectification

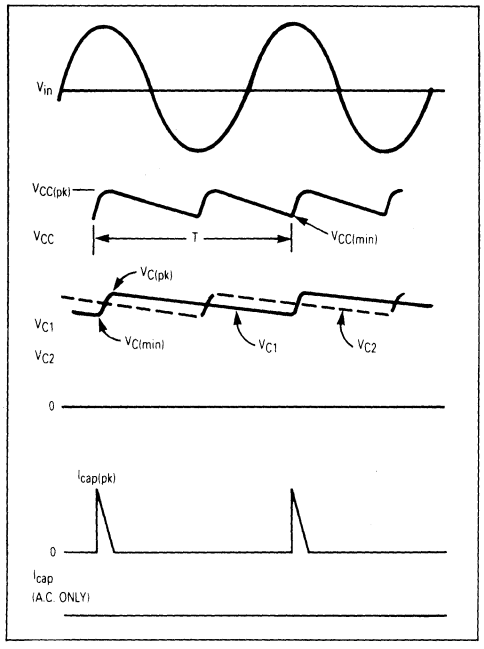


Figure 7d. Waveforms of Voltage Doubler

$$t_a \approx \frac{\cos^{-1}\left[\frac{V_{CC(min)}}{V_{CC(pk)}}\right]}{2\pi f_{in}} \qquad (17)$$

$$= 2.13 \text{ ms}$$

In order to evaluate the rms ripple current $I_{cap(rms)}$ of the smoothing capacitors C_{in}, a triangular approximation is used to simplify the derivation. The a.c. peak current $I_{cap(pk)}$ of C_{in} is,

$$I_{cap(pk)} = \frac{C_{in}}{2}\frac{dV_{CC}}{dt} \qquad (18)$$

$$= \pi f_{in} C_{in} \sqrt{V_{CC(pk)}^2 - V_{CC(min)}^2}$$

$$\approx 5.5 \text{ A for the practical value of } C_{in} \text{ equal to } 220\ \mu\text{F}.$$

Thus,

$$I_{cap(rms)} \approx I_{cap(pk)} \sqrt{\frac{D}{3}} = I_{cap(pk)} \sqrt{\frac{t_a}{3T/2}} \qquad (19)$$

$$= 1.47 \text{ A}$$

assuming that the a.c. component contributed by the switching operation of the flyback converter is negligible. This assumption holds because the high-frequency (switching frequency) ripple current is filtered by the additional small-valued capacitor (0.1 μF) connected across V_{CC}.

With reference to Figure 7(d), for the voltage doubler, the two capacitors are alternatively charged to peak line voltage. Note that whenever the rectified voltage V_{CC} is at instantaneous minimum $V_{CC(min)}$, the voltage of one capacitance is at its minimum, but the voltage on the other capacitor is at half way between peak and minimum voltages, $V_{C(pk)}$ and $V_{C(min)}$ respectively. The value of $V_{C(min)}$ can be determined as follows.

$$V_{CC(min)} = V_{C(min)} + [V_{C(min)} + V_{C(pk)}]/2$$

$$\text{or } V_{C(min)} = [2V_{CC(min)} - V_{C(pk)}]/3 \qquad (20)$$

$$= 91 \text{ V for } V_{C(pk)} = 90 \times 1.414 = 127 \text{ V and } V_{CC(min)} = 200 \text{ V}.$$

From energy law,

$$P_{in}/2 \approx 1/2\ C_{in}\ [V_{C(pk)}^2 - V_{C(min)}^2]\ f_{in}$$

or

$$C_{in} = \frac{P_{in}}{V_{C(pk)}^2 - V_{C(min)}^2}\frac{1}{f_{in}} \qquad (21)$$

$$= 327.5\ \mu\text{F at } f_{in} = 50 \text{ Hz and full load.}$$

The time t_a, ripple currents $I_{cap(pk)}$ and $I_{cap(rms)}$ are given by,

$$t_a \approx \frac{\cos^{-1}\left[\frac{V_{C(min)}}{V_{C(pk)}}\right]}{2\pi f_{in}} = 2.46 \text{ ms} \qquad (22)$$

$$I_{cap(pk)} = 2\pi f_{in} C_{in} \sqrt{V_{C(pk)}^2 - V_{C(min)}^2} \qquad (23)$$

$$\approx 9.18 \text{ A for } C_{in} = 330\ \mu\text{F (practical value)}.$$

$$I_{cap(rms)} \approx I_{cap(pk)} \sqrt{\frac{t_a}{3T}} \qquad (24)$$

$$= 1.86 \text{ A}$$

As the power supply is designed to operate at both input ranges, the latter case defines the relevant maximum ripple current. In order to demonstrate the effectiveness of the universal input-voltage adaptor, the ripple current and voltage assuming no doubler are calculated to be, with $C_{in} = 330\ \mu$F, $V_{in} = 90$ Vac and Pin = 128.6 W at 50 Hz,

$$V_{CC(min)} = [127^2 - 128.6/(60 \times 165\mu)]^{1/2} = 23.3 \text{ V}$$

$\delta V_{CC} = 127 - 23.3 = 103.7$ V (compared with 55 V for high range)

$t_a = 4.4$ ms

$I_{cap(pk)} \approx 6.5$ A

$I_{cap(rms)} \approx 3$ A (nearly double of the value with voltage doubler).

Such a large ripple voltage at V_{CC} will greatly stress the switching transistor and will degrade the overall performance, especially the conversion efficiency and regulation.

The bridge rectifiers are selected to be 1N5398, a 1.5 A device because the highest average line input current is $0.9 \times 128.6/90 \approx 1.3$ A. The two 1 W resistors, in parallel with C_{in}, are used to discharge the input capacitor after powered off. Note that one of them is connected to "start-up" at one end instead of the ground (the inverted triangular sign). It provides the starting current for the current-mode controller and drive circuit at initial power-on, when the control circuitry is still not self-supplied. The start-up current is limited to approximately 2 to 4.6 mA.

The inrush input current is limited to an acceptable level by the thermistor which has a resistance of 5 Ω at room temperature and 1 Ω after heated up.

MAC229A8 has been found suitable for the triac in the universal input-voltage adpator because of the following points:

1. It is a sensitive gate device with I_{GT} of 10 mA maximum for operation quadrants I, II and III [13]. The small gate current requirement will minimize the power dissipation in the adaptor and will lower the capacitance of the charge-pump capacitor C.
2. Its breakdown voltage is 600 V, which exceeds all input voltage limits.
3. Guaranteed 25 V/μs, rate of rise of off-state voltage ensures the accurate operation of MAC229A8 [13].
4. Low power loss in the device due to its low voltage drop across MT1 and MT2 at operation.

MC3423 is originally designed for overvolt "crowbar" sensing circuit, but it is also applicable in the universal input-voltage adaptor because of the similar working condition [14]. It has a temperature-compensated internal reference voltage of 2.6 V which is connected to one terminal of the input comparator. Thus, if the trip point at which the triac is turned off is set to 135 Vac or 191 Vdc, the divider ratio in Figure 7(a) is,

$$2.6 = 191 \times R_2/(R_1 + R_2)$$

or $R_1/R_2 = 72.5$

$R_1 = 2.2\ M\Omega$ and $R_2 = 30\ k\Omega$.

The internal constant current source (pin 4) can provide a time delay before tripping the "crowbar" SCR. It results in better noise immunity and controlled start-up transients of the adaptor. The practical values of the capacitor and resistor connected at pin 4 to ground are 50 nF and 560 kΩ, respectively, which has a time delay of approximate 650 μs. The output is connected, through a resistive divider, to a small-power SCR (MCR102 with $I_{K(max)}$ = 0.8 A). When the input voltage is detected to be above the trip point, the SCR is fired to shunt all the incoming current from the charge pump, and the triac will remain off.

The MC3423 can operate from 4.5 V to 40 V of supply voltage [15]. Hence, a 6.2 V zener diode is used to clamp the supply voltage of the crowbar senser to 6.2 + 0.7 ≈ 7 V for stable operation. A 100 pF filtering capacitor for the sensing divider and a small-signal diode 1N4148 for clamping the input of MC3423 are also added in the circuit.

To calculate a suitable value for the charge-pump capacitor C, the working principle of the charge pump is first considered. It consists of two diodes (1N4001), a coupling capacitor C, and a smoothing capacitor (100 μF). C is charged during the rise time of input voltage and is discharged during fall time. Assuming that the voltage drop on the charge pump circuit is much less than the peak of input voltage (V_P), from charge balance principle,

$$Q = (2V_P)\ C = IT$$

or $C = (IT)/(2V_P)$

where I = average d.c. current supplied to the line adaptor.

The boundary case is at low line, low range, where V_P = 127 V and I = 10 mA for gate current plus 6 mA for bias current. Thus,

$$C = [(10 + 6)\ (1/50)]/(2 \times 127) \approx 1.2\ \mu F$$

At high line, high range, $V_P \approx 370$ V and the maximum value of I is 53 mA at 60 Hz. The maximum power consumption of the line adaptor is 7 x 0.053 = 0.37 W. The 10 Ω resistor in series with C is used to limit the inrush current when starting.

So far in the design of the universal input-voltage adaptor, an important point which has not yet been considered is the hazard of severe overvoltage at V_{CC} during start-up. If the power supply is started at high line, high range, V_{in} = 260 Vac, during the falling edge of input voltage, and the supply voltage of MC3423 is charged to about 7 V, the triac will be turned on for the doubler operation in the remaining negative cycle of input voltage, without the gate capacitor C_G, since MC3423 had not yet and would not be tripped until the next positive cycle. Then, the lower bulk capacitor will be stressed to nearly double of its normal voltage rating. This harmful effect not only damages the bulk capacitor, but also produces abnormally high input voltage (V_{CC}) for the flyback converter, in a small instant. Therefore, C_G is connected to the gate and MT1 terminal of the triac to serve two purposes:

1. to delay the turn-on of triac for nearly a quarter of one cycle.
2. to increase the dV/dt blocking capability of the triac (> 200 V/μs) and hence, the overall system reliability [13].

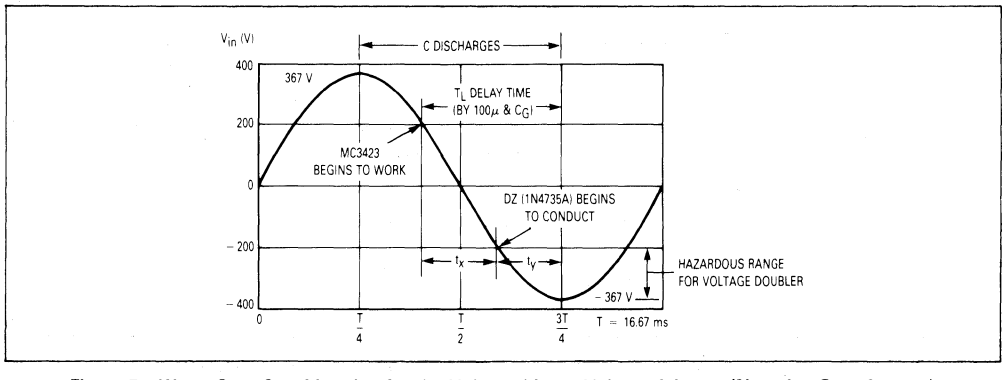
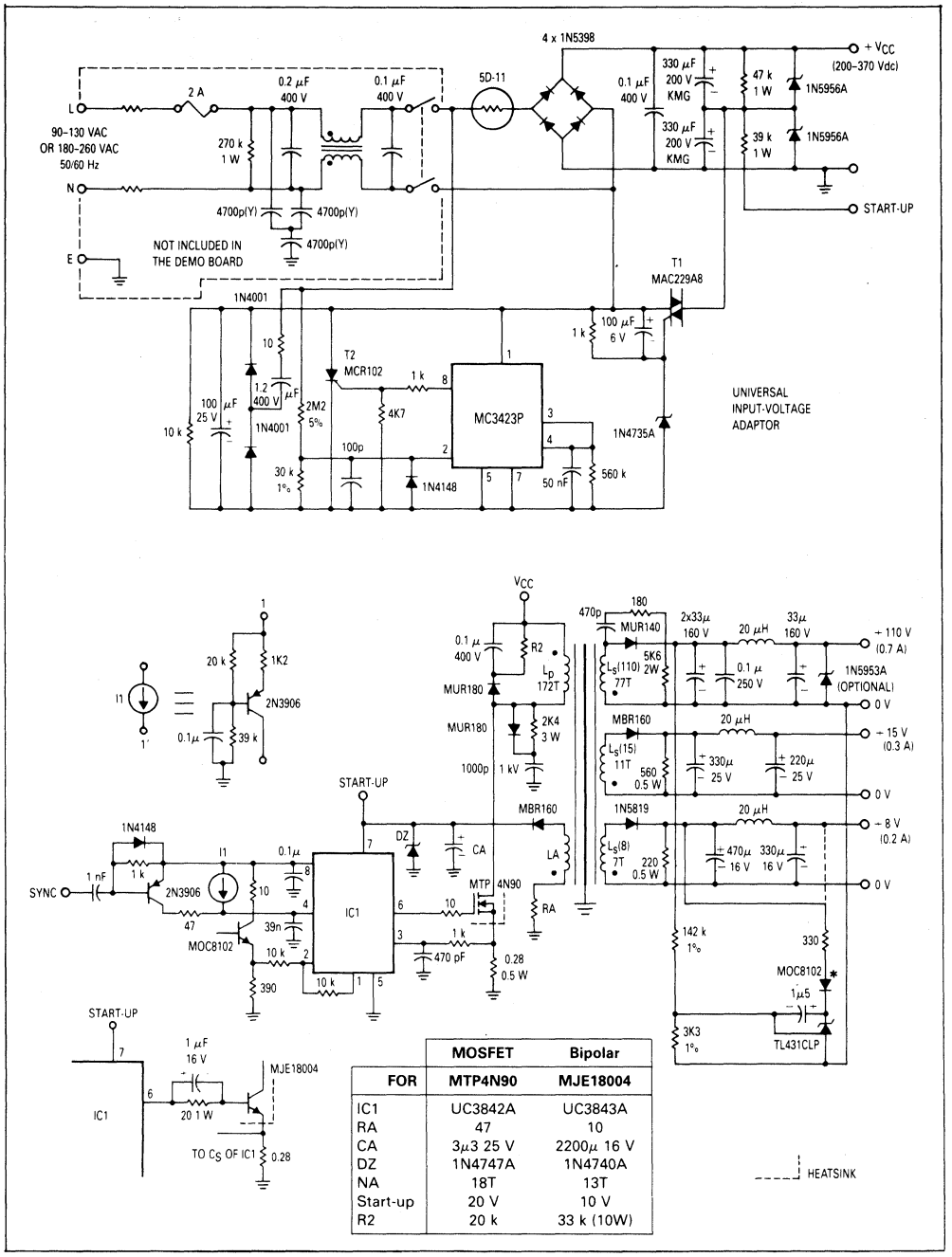


Figure 7e. Worst Case Consideration for the Universal Input-Voltage Adaptor (Negative Gate Current)



FOR	MOSFET MTP4N90	Bipolar MJE18004
IC1	UC3842A	UC3843A
RA	47	10
CA	3μ3 25 V	2200μ 16 V
DZ	1N4747A	1N4740A
NA	18T	13T
Start-up	20 V	10 V
R2	20 k	33 k (10W)

Figure 8. Complete Circuit Schematics of 90 W Off-the-Line Power Supply

The determination of the capacitance of C_G is determined as follows, with reference to Figure 7(e). At high line, high range, and 60 Hz, the average current I is maximum (53 mA). All discussions below are referred to a falling edge and the consecutive rising edge of less than 1/4 cycle of input voltage, because the charge-pump capacitor C is discharging to the adaptor circuit during fall time and the crowbar senser cannot be tripped if V_{in} falls beyond +200 V. If the supply voltage for MC3423 is just about 4.5 V, the crowbar sensing IC functions, and meanwhile, the instantaneous input voltage is at the trip point (200 V) and is going to the negative cycle, the gate capacitor C_G must be large enough to delay the conduction of the triac before the input voltage rises again, i.e. at the negative peak. Assume that, for simplicity, the supply voltage of MC3423 rises to about 6.2 V (zener voltage) when the input voltage falls to −200 V. Then,

t_x = charging time of the capacitor across the supply voltage of MC3423

$= 2 \times \sin^{-1} (200/367) / (2\pi \times 60) = 3$ ms

$\approx (6.2 - 4.5)$ V x (Capacitance value) / (53 − 6) mA

or capacitance value ≈ 100 μF (connected across supply voltage of MC3423)

But this capacitance is necessary to meet the ripple voltage requirement of the adaptor circuit. Afterwards, the zener diode (1N4735A) conducts, and the two capacitors connected in parallel are needed to delay the remaining time t_y before the input voltage rises from its negative peak again, within the same negative cycle. Therefore,

$t_Y = (16.67/4 - 3/2)$ ms ≈ 0.7 V x $(C_G + 100)$ μF/47 mA

since the threshold gate voltage of MAC229A8 is 0.7 V typically.

$C_G = 79$ μF

A practical value of 100 μF is used in Figure 8. Note that the discharging current of C at zero-crossing of input voltage is greater than the average value I. The time constant of the gate capacitance and gate resistor (1 kΩ) is 0.1s, which is sufficient for resetting the triac between consecutive power-off and on. The 10 kΩ resistor is for discharge of the 100 μF capacitor, and the corresponding time constant is 1 second. Time constants too long in the above design may result in failure of the universal input-voltage adaptor if the power supply which was previously socketed in 110 V line is quickly plugged in 220 V line.

It should be noted that two optional power zener diodes (1N5956A) are connected across each bulk capacitor C_{in} because:

1. they can absorb short transient voltages (>200 V) on C_{in},
2. they can prevent any failure of the universal input-voltage adaptor from damaging the flyback converter and the two bulk capacitors.

Although such failures are rare the consequences are to be avoided since failure of the line adaptor poses a safety hazard to the human beings (especially the eyes radiated by X-ray).

Common-mode and differential-mode EMI/RFI filters are generally required for all switching power supplies. They are included in Figure 8, but are excluded in the DEMO board.

4. PERFORMANCE OF THE FLYBACK POWER SUPPLY

4.1 COMPLETE CIRCUITRY

Figure 8 shows the complete circuit schematic of the 90 W flyback power supply. The triac in the universal adaptor is negatively driven by the charge pump, since

TOP VIEW

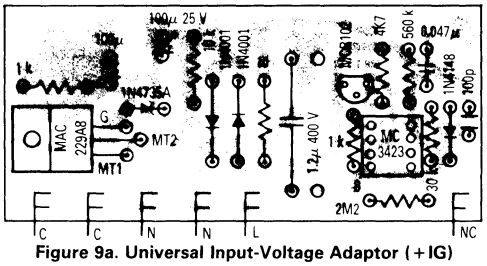


Figure 9a. Universal Input-Voltage Adaptor (+IG)

TOP VIEW

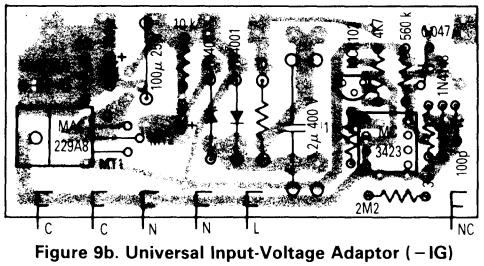


Figure 9b. Universal Input-Voltage Adaptor (−IG)

TOP VIEW

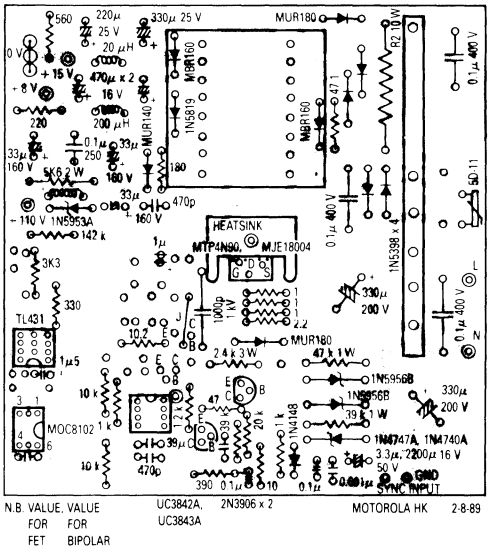


Figure 9c. Main Board (for MTP4N90 & MJE18004)

Figure 9. PCB and Component Layouts (not full size)

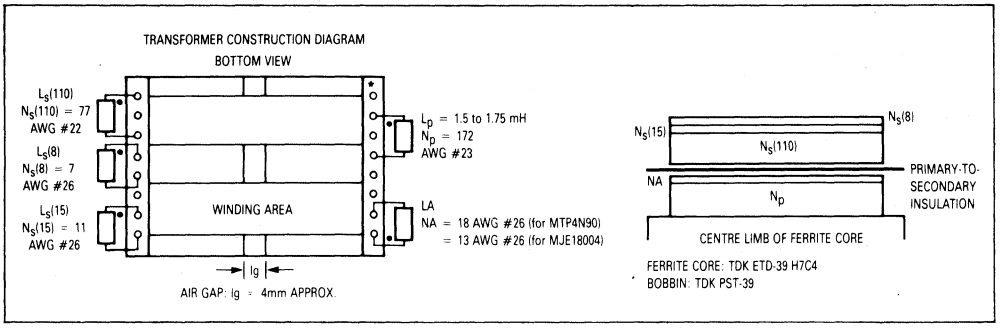


Figure 10. Flyback Transformer Construction

it is least sensitive to noise in this mode. Drive circuits for MTP4N90 and MJE18004 are also shown.

Sometimes, it is unnecessary to have the universal input-voltage adaptor because the power supply may be used only at one range. Then, a modular approach for the adaptor can lower the system cost and can increase the flexibility of manufacture. The universal input-voltage adaptor board can be simply removed or unplugged from the power supply board without affecting the normal operation of the power supply, if the adaptor is not needed. Therefore, using this approach, the adaptor becomes optional. The printed circuit board and component layouts of the universal input-voltage adaptor(s) and the main board of power supply are shown in Figure 9. The construction diagram of the power transformer is shown in Figure 10. Table 1 lists all Motorola semiconductor components used in this power supply.

Table 1. List of Motorola Semiconductor Components

	Part Numbers	Qty.
IC	UC3842A (for MTP4N90) UC3843A (for MJE18004) MC3423P TL431CLP	1 1 1 1
Opto	MOC8102	1
MOSFET	MTP4N90	1
SCR	MCR102	1
TRIAC	MAC229A8	1
BJT	MJE18004 2N3906	1 2
Rectifier	1N4001 1N5819 1N5398 MUR140 MUR180 MBR160	2 1 4 1 2 2
Zener	1N4735A 6.2 V 1N4740A 10 V (for MJE18004) 1N4747A 20 V (for MTP4N90) 1N5953A 150 V (optional) 1N5956A 200 V	1 1 1 1 2

4.2 EXPERIMENTAL MEASUREMENTS AND RESULTS

D.C. measurements are summarized in Table 2. Line and load regulation are excellent (better than 0.5%) for the +110 V output. Regulation for other two rails is within 10%, if the transformer is properly manufactured. Conversion efficiency, is close to the expected figure (70%), and the best one is 73.7% at $I_{O(110)}$ = 0.7 A, f_S = 15.7 kHz and V_{CC} = 360 V for MTP4N90; whereas for the bipolar power transistor MJE18004, the best efficiency is 74.2% at $I_{O(110)}$ = 0.7 A, f_S = 15.7 kHz and V_{CC} = 360 V. Although MJE18004 has lower conduction loss than MTP4N90, it has higher power losses in the base drive circuit and in the switching transitions. This is why MOSFETs can compete with advanced BJT even with higher conduction loss at relatively low switching frequency.

The maximum ripple voltage at 110 V output is approximately 150 mV (peak-to-peak) which is less than 0.2% of the output voltage, as predicted in section 2.3. The power supply is observed to be stable over the entire range of load currents. The dynamic response is also satisfactory, with an overshoot of less than 8 V at f_S = 15.7 kHz and V_{CC} = 200 V, from half-load to full-load (see Figure 1). Also in Figure 12, the transient responses of the power supply are introduced for very large-signal disturbances — from no load to full-load. The overshoot is about 20 V and the undershoot is over 30 V, which is quite satisfactory. The overshoot can be further reduced by increasing the integrating capacitance C_f in the feedback loop. But, this will result in slower transient responses.

Typical experimental switching waveforms are shown in Figure 11, at different load currents, input voltages and switching frequencies. Also, Figure 13 shows the photo of the 90 W off-the-line power supply.

5. CONCLUSION

A low-cost 90 W flyback power supply with external synchronization and universal input-voltage adaptor for multi-sync color monitor has been discussed in detail. The power supply has excellent line and load regulation and is found to be suitable in the application of low-cost multi-sync color monitors or TVs. Also, it can operate at both a.c. mains, i.e. 90–130 V or 180–260 V, without greatly affecting the system cost and performance.

Table 2. Performance of 90 W Off-the-Line Flyback Power Supply

MTP4N90 (MOSFET)

I_o (110 V)	V_o (110 V)	(15 V)	(8.0 V)	f_s	I_{in}	V_{CC}	Efficiency
0.2	110.1	16.01	8.88	15.7	0.12	300	61.2
0.5	110.0	16.23	9.05	15.7	0.26	300	70.5
0.7	109.9	16.31	9.10	15.7	0.35	300	73.3
0.7	109.9	16.32	9.10	15.7	0.55	200	69.9
0.7	109.9	16.30	9.10	15.7	0.29	360	73.7
0.2	110.1	15.99	8.88	25.0	0.13	300	56.5
0.5	110.0	16.19	9.03	25.0	0.26	300	70.5
0.7	110.0	16.25	9.08	25.0	0.35	300	73.3
0.7	110.0	16.26	9.07	25.0	0.53	200	72.6
0.7	109.9	16.25	9.08	25.0	0.29	360	73.7
0.2	110.1	15.98	8.88	32.0	0.13	300	56.5
0.5	110.0	16.17	9.03	32.0	0.26	300	70.5
0.7	110.0	16.23	9.07	32.0	0.35	300	73.3
0.7	110.0	16.24	9.07	32.0	0.53	200	72.6
0.7	110.0	16.23	9.07	32.0	0.30	360	71.3
A	V	V	V	kHz	A	V	%

MJE18004 (Bipolar)

I_o (110 V)	V_o (110 V)	(15 V)	(8.0 V)	f_s	I_{in}	V_{CC}	Efficiency
0.2	110.8	14.41	8.82	15.7	0.12	300	61.6
0.5	110.7	14.65	9.00	15.7	0.26	300	71.0
0.7	110.6	14.82	9.11	15.7	0.35	300	73.7
0.7	110.6	14.73	9.06	15.7	0.54	200	71.7
0.7	110.6	14.83	9.11	15.7	0.29	360	74.2
0.2	110.8	14.44	8.83	25.0	0.13	300	56.8
0.5	110.8	14.70	9.02	25.0	0.27	300	68.4
0.7	110.7	14.78	9.09	25.0	0.36	300	71.8
0.7	110.7	14.77	9.08	25.0	0.53	200	73.1
0.7	110.7	14.78	9.09	25.0	0.30	360	71.8
0.2	110.8	14.43	8.83	32.0	0.13	300	56.5
0.5	110.8	14.68	9.01	32.0	0.27	300	68.4
0.7	110.7	14.75	9.07	32.0	0.36	300	71.8
0.7	110.7	14.75	9.07	32.0	0.54	200	71.8
0.7	110.7	14.75	9.08	32.0	0.30	360	71.8
A	V	V	V	kHz	A	V	%

*Ripple voltage at 110 V output is about 150 mVpp at V_{CC} = 300 V, f_s = 15.7 kHz & I_o = 0.7 A.

Figure 11. Experimental Oscillograms

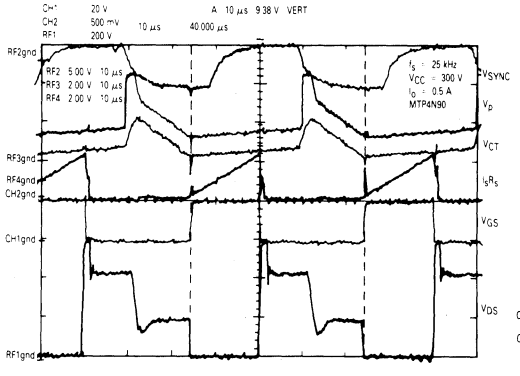


Figure 11a. Key Waveforms at f_s = 25 kHz and V_{CC} = 300 V (for MTP4N90)

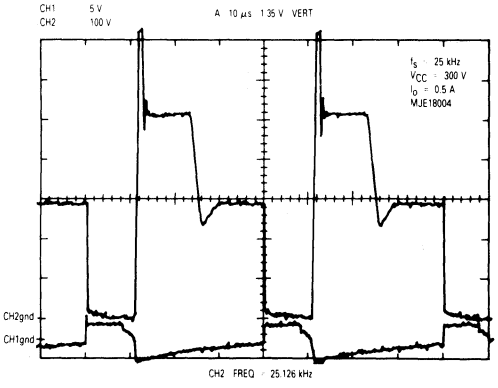


Figure 11b. V_{CE} and V_{BE} at f_s = 25 kHz and V_{CC} = 300 V (for MJE18004)

Figure 11. Experimental Oscillograms

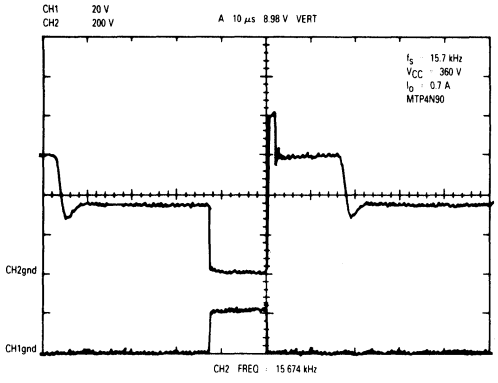


Figure 11c. V_{DS} and V_{GS} at f_S = 15.7 kHz and V_{CC} = 360 V (for MTP4N90)

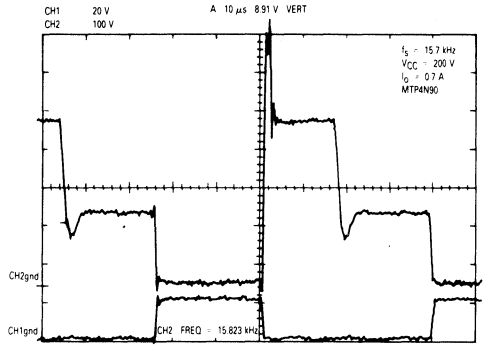


Figure 11d. V_{DS} and V_{GS} at f_S = 15.7 kHz and V_{CC} = 200 V (for MTP4N90)

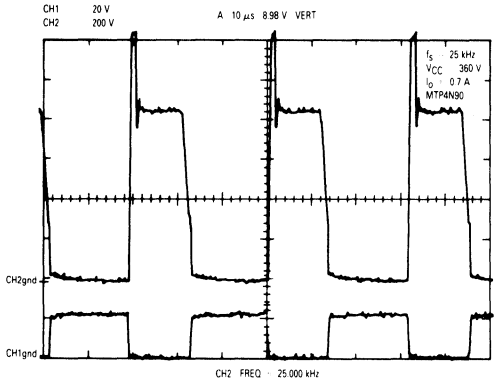


Figure 11e. V_{DS} and V_{GS} at f_S = 25 kHz and V_{CC} = 360 V (for MTP4N90)

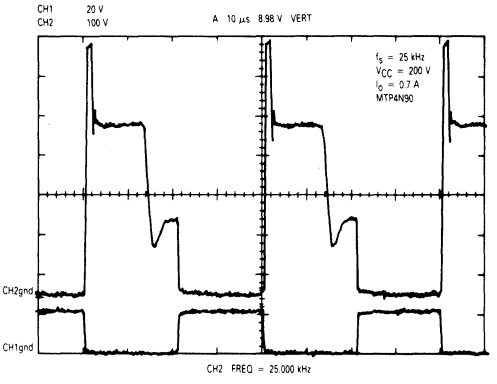


Figure 11f. V_{DS} and V_{GS} at f_S = 25 kHz and V_{CC} = 200 V (for MTP4N90)

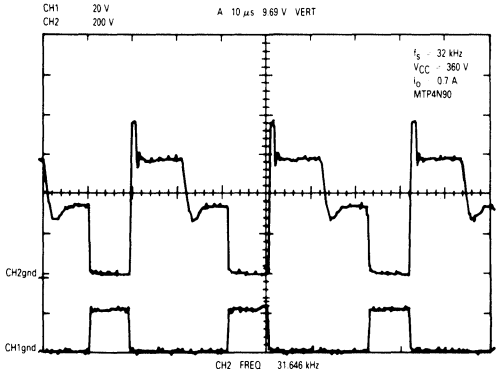


Figure 11g. V_{DS} and V_{GS} at f_S = 32 kHz and V_{CC} = 360 V (for MTP4N90)

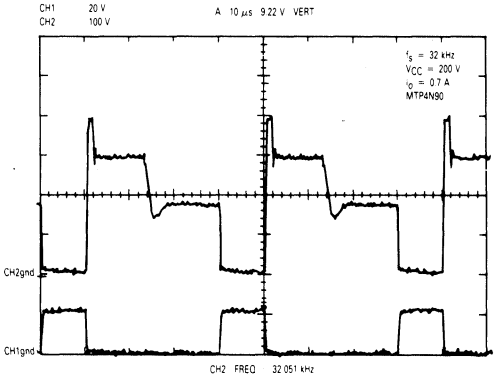


Figure 11h. V_{DS} and V_{GS} at f_S = 32 kHz and V_{CC} = 200 V (for MTP4N90)

Figure 12. Large-Signal Transient Load Responses

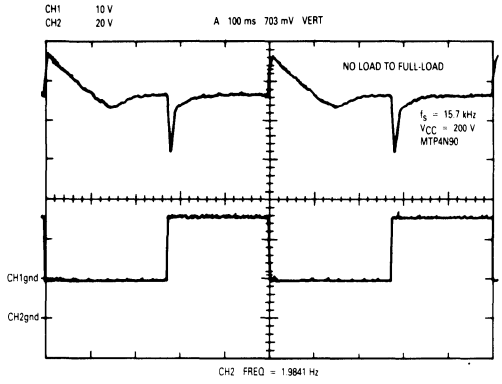


Figure 12a. For MTP4N90, From No Load to Full-Load at f_S = 15.7 kHz.

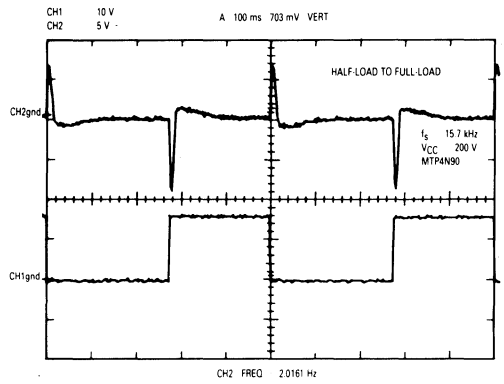


Figure 12b. For MTP4N90, From Half-Load to Full-Load at f_S = 15.7 kHz.

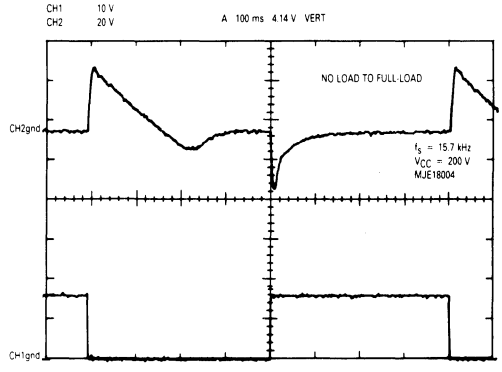


Figure 12c. For MJE18004, From No Load to Full-Load at f_S = 15.7 kHz.

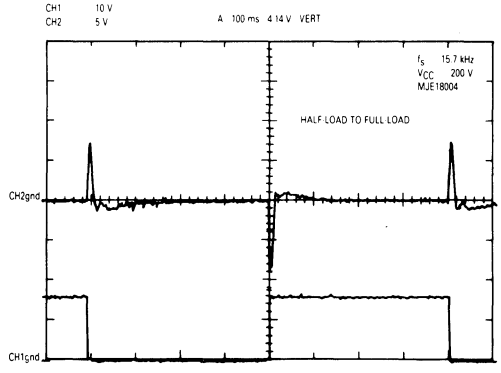


Figure 12d. For MJE18004, From Half-Load to Full-Load at f_S = 15.7 kHz.

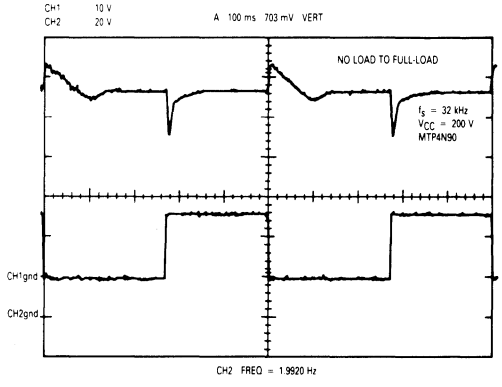


Figure 12e. For MTP4N90, From No Load to Full-Load at f_S = 32 kHz.

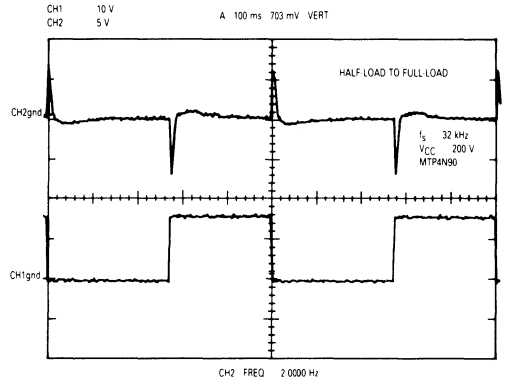


Figure 12f. For MTP4N90, From Half-Load to Full-Load at f_S = 32 kHz.

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In the course of preparing of the manuscript, several persons gave their contributions to aid the completion of this application note. Mr. T.S. Au, a summer student from H.K. Polytechnic helped to draft all P.C.B. and component layouts and to prepare demo boards. Mr. Cedric Lai, a cooperative student from H.K. University, reviewed the script with great care. Also, continual supports from Power Group of Discrete Business, Motorola Semiconductors H.K. Ltd. was proved to be essential to the success of our works. We, Cheng and Tong, must express our thanks to these helpful people at the end of our article.

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[11] Advanced data sheets for MOC810X (Motorola Semiconductors LTd.)

[12] "Guide to Thyristor Applications," Motorola Application Note AN849, p. 1–7, 1982.

[13] Data sheets for MAC229A8 (Motorola Thyristor Device Data — DL137 R1)

[14] Data sheets for MC3423P (Motorola Linear and Interface ICs — DI128 R2)

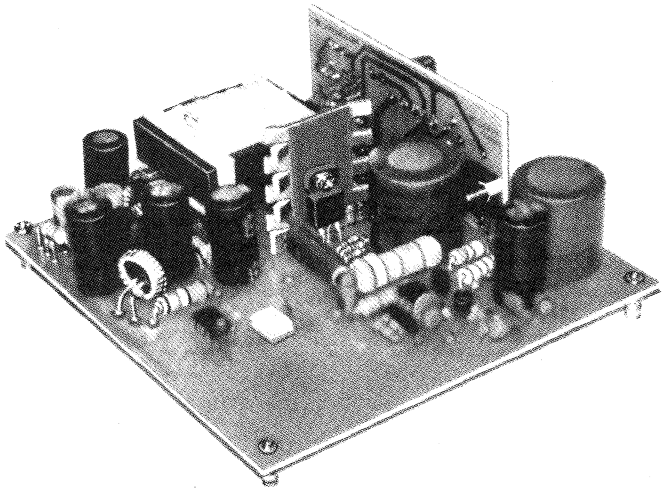


Figure 13. Photo of 90 W Off-the-Line Power Supply

Driving High Capacitance DRAMs In An ECL System

INTRODUCTION

In present day computer/controller systems where speed and efficiency are of the utmost importance, system designers are using mixed technology in their designs to achieve the necessary speed, power, cost and processing capability desired in high speed data processing systems.

The logic type most applicable to the high speed function of such a system is Emitter Coupled Logic (ECL). Motorola's 10K, 10H, and ECLinPS devices make it possible to operate with clock rates up to 1 GHz. However there are sections of a system where ECL speeds are not necessary. For example, in the area of bulk memory that is not accessed every clock cycle a large CMOS DRAM is less costly, uses less power and takes up less board space per bit than an ECL memory. Now, since ECL and CMOS are of different logic forms and their signal levels are not compatible there needs to be a level translation to enable the two logic families to be used together. The Motorola MC10H/100H660 4-BIT ECL-TTL LOAD REDUCING DRAM DRIVER was designed for this purpose. The H660 is shown in a simplified typical system application in Figure 1.

This paper will explain the features that were designed into the H660 and how to apply them in a mixed technology system to obtain the best performance versus power ratio.

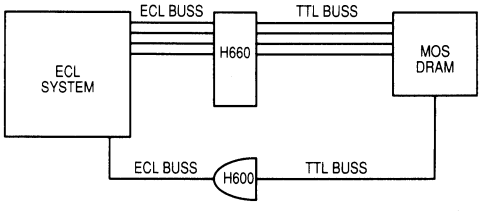
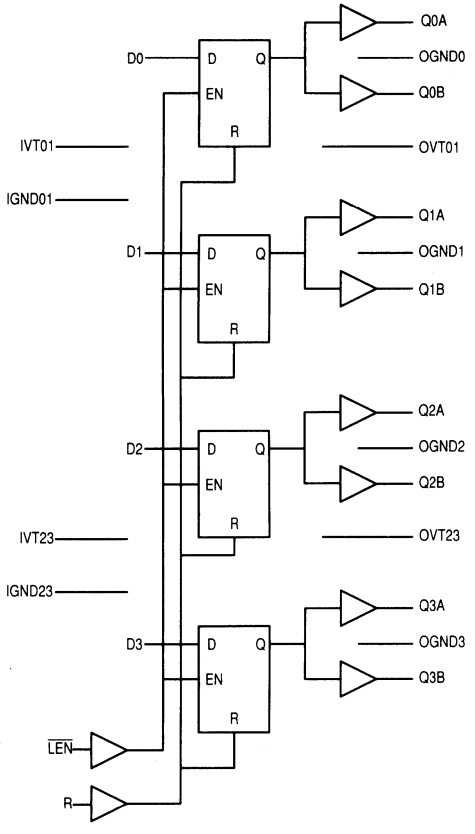


Figure 1.

SYSTEM DESIGN

To switch highly capacitive loads at speeds of a few nanoseconds, the device must supply a large amount of current to charge the lines then it must sink this current to discharge them. This fast switching on an unterminated line can result in a substantial amount of over shoot and ringing.

To eliminate the overshoot and ringing, a small value series resistor (Rs) can be placed at the driver. Figure 4 shows an application of the H660 with a series resistor.



MC10/100H660 Logic Diagram

FEATURES OF THE H660 DRAM DRIVER

The H660 translates the ECL signal to a TTL level suitable for driving DRAM memories with high input capacitance.

The input impedance of the 660 varies with frequency, at 10 MHz it is typically about 150 to 250 ohms and goes down to about 50 to 60 ohms at 200 MHz as shown in Figure 2.

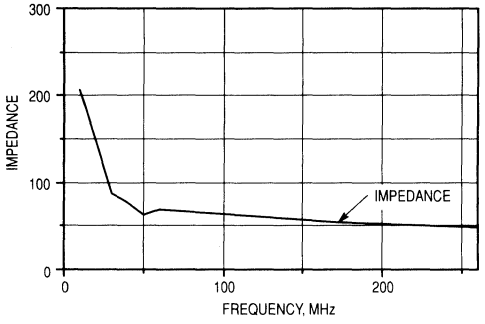


Figure 2. Input Impedance

For every ECL input there are two output lines, each capable of driving 300 pF. Assuming 5 to 15 pF capacitance per pin for 1 megabit of DRAM, each output pair could be connected to 40 megabits of DRAM.

The H660 has a totem type TTL output stage with no I_{OS} limiting resistor. The output Isink capability is 48 mA. The output transistors are driven differentially with a dual phase splitter from the translator, this assures that both the output totem transistors will never be turned on at the same time therefore, with no load, I_{CC} dynamic power remains constant over frequency. We recommend a minimum load of 100 pF the graph in Figure 3 was made using a special input signal just to show that the typical internal TTL current glitch is not present. The dual phase splitter is a unique method, patented by Motorola, of driving totem output transistors to avoid the current glitch that happens in all previous TTL drivers as one transistor turns on while the other turns off. The output can easily be put at a high impedance state by 'turning' off V_{EE} which will cut off both output transistors.

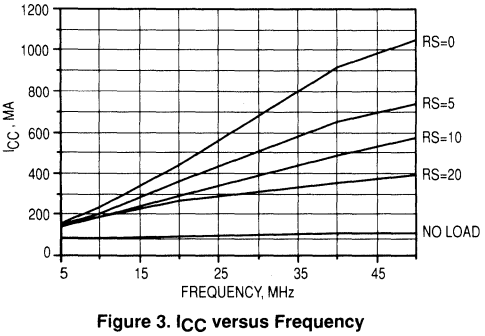


Figure 3. I_{CC} versus Frequency with 300 pF and No Load

The drivers are arranged to be used in pairs, each output pair is associated with a ground pin and every two pairs with one V_{CCT} pin. The internal logic V_{CC} and ground pins are separate from the output V_{CC} and ground pins, this keeps the noise from the high current output from feeding back to the internal logic. If there is ever a need to use only two data lines, power would be needed only on half of the device.

A latch is added to provide the capability for a memory controller to propagate new addresses to different banks without having to wait for the address timing constraints to be satisfied from a previous memory operation. For system implementations where this is acceptable, the user has the capability to keep the latch open, thus having the part act as an address translator/buffer, with minimal performance impact due to the additional propagation delay incurred from the internal latch. The latch is controlled with an already existing ECL level DRAM timing signal.

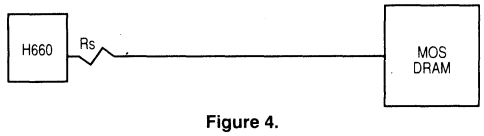


Figure 4.

The graphs in Figure 5 and 6 show that by adding the series resistor the device I_{CC} dynamic current is significantly reduced while the propagation delay is only slightly increased.

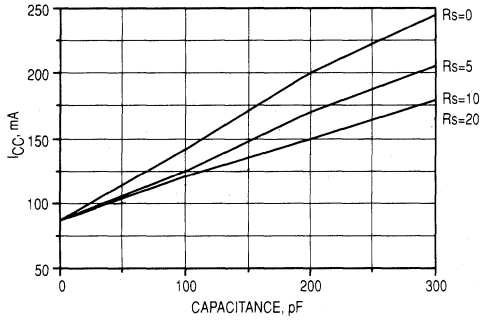


Figure 5. MC10/100H660 I_{CC} versus CL, RS

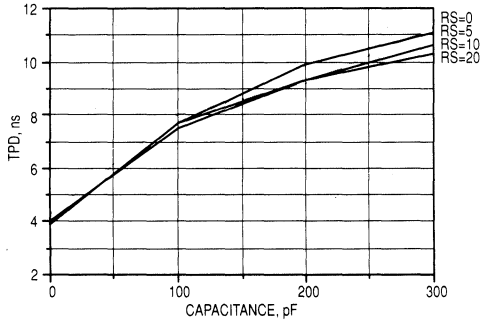
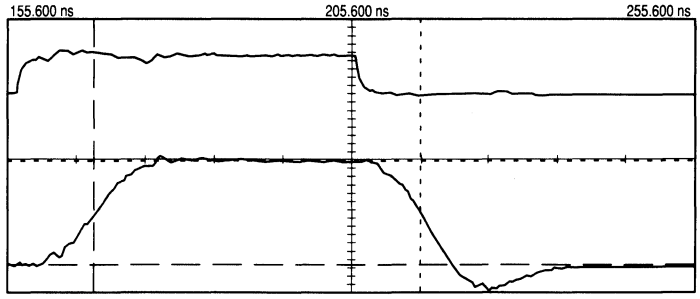
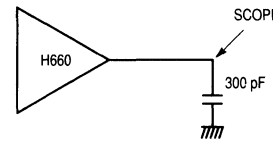


Figure 6. TPD versus CL, RS

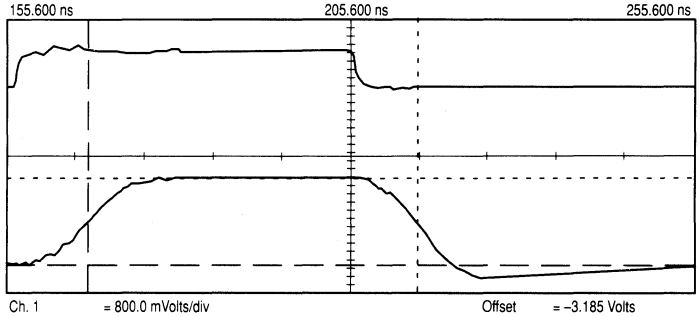
Another important benefit of the series resistor is that it reduces the device dynamic current by shaping the waveform, giving it slower rising and falling edges. The slower edge rate eliminates the overshoot and ringing that are associated with very fast signal edges on unterminated printed circuit card traces. Also, the slower edge allows for longer circuit traces to be used without the need to be terminated. As shown in the waveforms in Figure 7, the signal can be shaped to meet many system requirements.

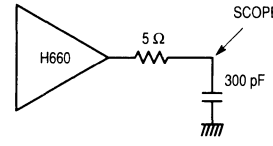




Ch. 1	= 800.0 mVolts/div	Offset	= –3.185 Volts
Ch. 2	= 2.000 Volts/div	Offset	= 6.375 Volts
Timebase	=10.0 ns/div	Delay	= 155.600 ns
Ch. 2 Parameters		+ Width	= 47.4560 ns
Fall Time	= 8.8850 ns	Overshoot	= 4.081%
P-P Volts	= 7.8750 Volts		
	Rise Time= 10.7652 ns		
	Preshoot = 24.48%		

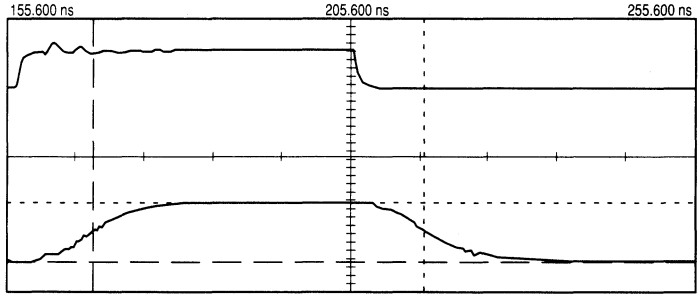
WAVEFORM 1

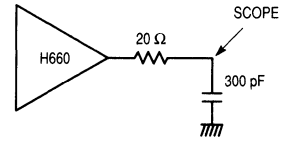




Ch. 1	= 800.0 mVolts/div	Offset	= –3.185 Volts
Ch. 2	= 2.000 Volts/div	Offset	= 6.375 Volts
Timebase	=10.0 ns/div	Delay	= 155.600 ns
Ch. 2 Parameters		+ Width	= 47.8818 ns
Fall Time	= 8.9770 ns	Overshoot	= 2.469%
P-P Volts	= 5.8750 Volts		
	Rise Time= 12.0178 ns		
	Preshoot = 13.58%		

WAVEFORM 2





Ch. 1	= 800.0 mVolts/div	Offset	= –3.185 Volts
Ch. 2	= 2.000 Volts/div	Offset	= 6.375 Volts
Timebase	=10.0 ns/div	Delay	= 155.600 ns
Ch. 2 Parameters		+ Width	= 48.2754 ns
Fall Time	= 14.9356 ns	Overshoot	= 3.636%
P-P Volts	= 3.6875 Volts		
	Rise Time= 13.9250 ns		
	Preshoot = 3.636%		

WAVEFORM 3

Figure 7.

There are times when the overshoot is desirable as when driving CMOS memories requiring a rail to rail input signal. When the load is capacitive with no pull up or pull down resistor, the output will go all the way to each rail and will not discharge in a cycle time period. An example of this phenomena is shown in Figure 8.

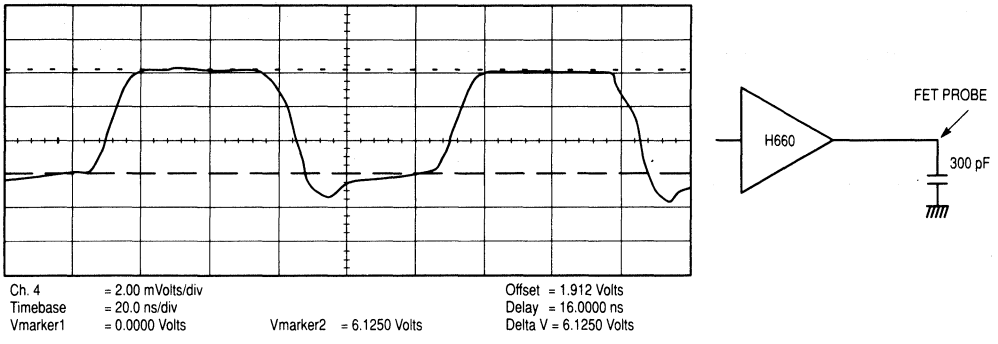


Figure 8.

When driving a resistive load it is seen on the chart in Figure 9 that the V_{OH} level remains somewhat constant over I_{OH} loads that are over the device rating.

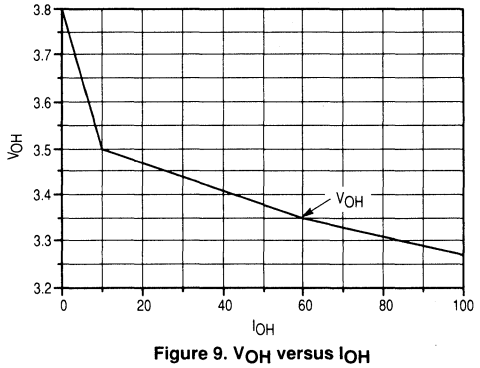


Figure 9. V_{OH} versus I_{OH}

As a precautionary note, if an output is being used without the series resistor and if it becomes shorted to ground while in a high state, it will source over 700 mA and in a short period of time the device will be destroyed.

After the proper memory addresses are selected and the TTL data is transferred from memory the data is then translated back to ECL by use of a TTL to ECL translator such as a Motorola MC10H/100H600, 602 nine bit TTL to ECL translator or a MC10124 or MC10H124, 4 bit translator.

CONCLUSION

Mixed technology systems are becoming very popular where system designers must optimize system performance while keeping overall system cost/power in line.

This application note described the MC10H/100H600 4-BIT ECL-TTL LOAD REDUCING DRAM DRIVER and some application techniques that can result in an improvement in system performance and reliability.

Considerations in Using The MHW801 and MHW851 Series RF Power Modules

by Norm Dye and Mike Shields
RF Products Division

INTRODUCTION

The MHW801/851 Series of power modules are designed primarily for applications in cellular portable radios. The -1 module is frequency compatible with the American system called AMPS; the -2 module is frequency compatible with the European TACS system; the -3 module is frequency compatible with the Scandanavian system called NMT; and the -4 module is frequency compatible with the NTACS system in Japan. Other than frequency of operation, all models of the MHW801 and MHW851 are identical and meet the general electrical specifications set forth on the data sheet. The only difference in the MHW801 and MHW851 Series of modules is the flange design. In the case of the MHW801, the flange does not extend any appreciable distance beyond the PCB substrate/cap and it is intended that mounting to a heatsink will be accomplished by attaching the flange to the heatsink with solder. The MHW801 modules are considered to be surface mount modules. The MHW851 modules were introduced to offer similar modules with the more conventional method of mounting. The flange extends beyond the substrate/cap and attachment to a heatsink is intended to be by means of mounting screws.

A significant amount of applications information is contained in the MHW801/MHW851 Series data sheet. Also included are a block diagram of the module and decoupling networks used in the test fixture; typical performance curves showing parameters such as V_{Cont}, efficiency, input VSWR and output power as functions of frequency; and output power and V_{Cont} as functions of temperature.

GENERAL ELECTRICAL CONSIDERATIONS

Modules are matched to an impedance of 50 ohms for both input and output. Thus their application in a sub-system such as the transmitter portion of a portable radio is relatively straightforward. However, there are certain precautions that should be observed. First, it is important that DC inputs to the module be de-coupled by means of by-pass capacitors and/or chokes to prevent bias and power supply circuitry contributing to circuit instabilities (spurious oscillations). It is recommended that the module user pay careful attention to the decoupling information presented in the data sheet. Second, grounding of the module should be adequate to prevent low-level Impedances that result in signal feedback with consequent module instabilities. Remember that the back of the circuit substrate is ground and this is soldered to the module flange which then becomes the ground connection to external circuitry. Third, the board layout should be such that isolation of input lines from output lines is at least 50 dB.

Normal use of the module is to amplify CW signals that are frequency modulated. The first two stages of the module are biased Class A; however, the last two stages are biased Class C. Significant distortion will result if the signal contains amplitude information, such as amplitude modulation. However, it is possible to operate the module in less than a CW condition. In a pulse mode of operation, any duty cycle up to 100% should create no problems provided the peak power does not exceed the rated CW output power of the module. Note, however, that case temperature can no longer be tied to die temperature by the same constant difference used for CW operation. The thermal time constant of the die is approximately 10 micro-seconds which says that for moderately long pulse trains with low duty cycles, die temperature could be much higher than that predicted from CW measurements.

The modules have not been characterized for pulse power operation. It is to be assumed that greater than rated CW output power can be obtained from the module in a pulse mode of operation; however, this is not recommended without first consulting the factory because of concern for maximum voltage swings as well as maximum die temperature.

NOISE CHARACTERISTICS

One parameter of power modules frequently not specified is noise. Most applications of power modules have been in radios where transmitting and receiving did not occur simultaneously. Today, cellular radios are duplexed, i.e, they are capable of transmitting and receiving at the same time. Thus radio manufacturers are concerned about the noise characteristics of the transmitter in the receive frequency band, which is normally 45 MHz above the transmit frequency. For this reason, Motorola has begun to characterize and guarantee noise performance of modules designed primarily for use in duplexed cellular radios.

Noise power for the MHW801/851 Series modules is guaranteed in a 30 kHz bandwidth, 45 MHz above f_o. This is shown visually in Figure 1. Note that the noise is specified for two widely different temperatures and for rated output power only. A characteristic of the MHW801/851 Series modules is that the small signal (noise) gain of the amplifier is approximately 35 dB at rated output power but increases by as much as 3 dB as the control voltage (V_{Cont}) is decreased.

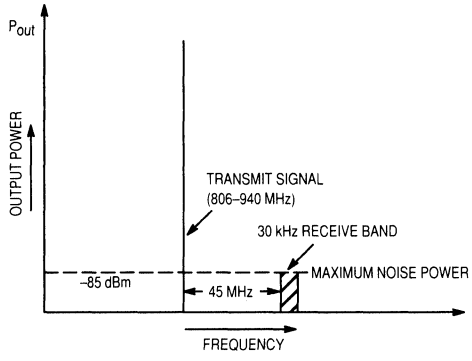
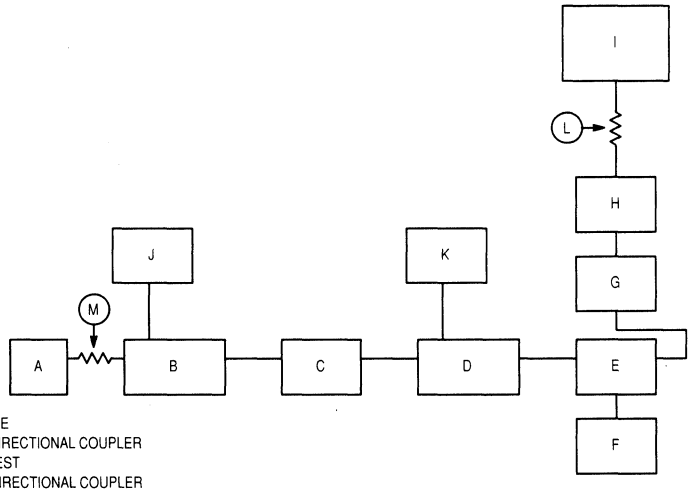


Figure 1. Noise Power In Receive Band

The block diagram for noise measurements is shown in Figure 2. Several comments about the block diagram are in order. First, the signal source must be extremely low noise, as close to kTB noise as possible. The HP8614A signal generator uses a cavity oscillator and satisfies the requirement of low noise. On the other hand, a frequency synthesized source such as the HP8656 (or Wavetek 2520A) signal generator does not. If this type of signal generator is used to make noise measurements, it is necessary to add a bandpass filter which will reject any signals 45 MHz above the output frequency.



A. SIGNAL SOURCE
B. 20 dB NARDA DIRECTIONAL COUPLER
C. UNIT UNDER TEST
D. 20 dB NARDA DIRECTIONAL COUPLER
E. CIRCULATOR IN FREQ BAND OF OPERATION
F. 50 OHM LOAD
G. TELONIC FILTER
H. TELONIC FILTER
I. HP 71000 SPECTRUM ANALYZER
J. HP POWER METER
K. HP POWER METER
L. 10 dB INTERNAL ATTEN.
M. 6 dB PAD

Figure 2. Block Diagram For Sideband Noise Measurement

Remember that any noise at the input of the MHW801/851 Series module is amplified by approximately 35 dB. This noise amplification should not be confused with internally generated noise which could be caused by a high stage noise figure or by regeneration in one of the module stages, neither of which is a factor in the MHW801/851 Series module design.

Second, it is essential that the module be terminated in a circulator which will prevent out-of-band impedances of the subsequent RF network from affecting the stability (and, thus noise) of the module. Third, care must be taken to prevent the carrier frequency from saturating the input stages of the spectrum analyzer used to measure the noise level. Again, it is critical in accurate noise measurements to be certain that the sensitivity of the spectrum analyzer be at least 10 dB better than the noise level being measured.

Normally to accomplish this it is necessary to reduce the resolution bandwidth (RBW) of the spectrum analyzer to 30 kHz and set the video filter to 100 Hz bandwidth. The manufacturer (Hewlett Packard) of the spectrum analyzer recommends a video bandwidth 100 times less than the RBW for best noise averaging.

The filters, "H" and "G" (in Figure 2) are stagger tuned to obtain adequate selectivity for rejecting the carrier frequency at the input to the spectrum analyzer. Obviously a single filter can be used if it has a rejection level of approximately 60 dB, 45 MHz away from the bandpass of the filter. The actual rejection needed depends on whatever is required to prevent saturation of the spectrum analyzer by the carrier signal.

GAIN CONTROL

The data sheet recommends gain control by keeping input power at 0 dBm and varying the control voltage. Output power versus control voltage is shown in the typical characteristics of the data sheet. Gain control in the MHW801/851 Series module is obtained by controlling the bias to the Class A input stage as opposed to other modules that controls the voltage to Class C driver stages. The benefit of this method of control is significantly less control current and a lower slope of the output power versus control voltage curve.

It is possible to control output power from the module by controlling input power with the control voltage maintained at a fixed level (generally maximum). This is somewhat intuitive; however, a major benefit of this method for power out control may not be obvious. This benefit is the best noise performance of the module because the small signal gain is approximately 3 dB less at high control voltage as compared to low control voltage. Other important factors such as stability, input VSWR, harmonics, efficiency and load mismatch are essentially unaffected by the method of output power control.

OTHER CIRCUIT CONSIDERATIONS

Performance of the module at less than rated output power is sometimes of significance in typical module applications. **Regardless of output power control, the noise characteristics, efficiency and harmonics will degrade at reduced output power.** As output power is reduced, the class C stages of the module operate further and further from their optimum load line resulting in significantly poorer efficiency. As their operation approaches the more non-linear region of the transistor transfer function, noise will likely increase and harmonics will increase with respect to carrier power. Generally these degradations in performance are not serious because they are relative to carrier power level. For example, efficiency becomes much less at output power levels of 100 mW; but current drain is much lower than for the case of 2 watts of output power, so this is generally not considered a problem in radio applications.

Other circuit considerations external to the module that are sometimes overlooked are source and load impedances. Note that the stability of the module is guaranteed only for source VSWR's of 3:1 and load VSWR's of 6:1. Frequently the load for the module is the transmit portion of a duplex filter. The out-of-band impedance presented by the filter can affect the stability of the module. The impedance reflected to the module depends on the length of transmission line between the module and the filter thereby causing line length to be an additional circuit consideration. It should be remembered that the MHW801/851 Series of modules are not unconditionally stable for all load and source impedances.

Out-of-band impedances of filters result in significantly high VSWR's at out-of-band frequencies. If these impedances are reflected to the module such that the module is terminated in impedances that lead to regions of instability, the module will oscillate.

Input power to the module can vary from a low value of 0 mW to a recommended maximum of 3 mW. Input powers greater than 3 mW are not recommended because of the potential damage that might result from overdriving the two final class C stages in the module. Overdrive results in excessive power dissipation particularly for the simultaneous condition of maximum supply voltage of 7.5 volts. Overdriving the final Class C stages can also lead to circuit instabilities because of changing impedances. Likewise, supply voltages greater than 7.5 volts should not be applied to the module for the same reasons of overdissipation and potential instabilities.

MOUNTING CONSIDERATIONS

GENERAL

In mounting power modules, consideration must be given to heat dissipation and grounding. Motorola specifies the range of case temperatures over which the module will perform safely. The upper temperature is determined by thermal resistances between each die and the case with the guideline that die temperature will be maintained below 200°C, which is considered a safe temperature for silicon transistors. All the user has to do is provide sufficient heat sinking for the module to be certain that the flange of the module does not exceed the maximum operating temperature rating. The maximum power dissipated by the module can be determined by determining the maximum DC power

input less the RF power output. Another way to determine the maximum power to be dissipated is to divide the rated output power by the minimum efficiency and then subtract the rated output power.

Maximum power dissipation for either the MHW801 or MHW851 Series modules is 2.44 watts (2 Watts divided by .45 minus 2 Watts). This relatively small amount of power can normally be dissipated by minimal thermal contact between the flange of the module and the heatsink provided in the application. Calculations using the MHW851 module attached to a heatsink only at the mounting screws indicate that the rise in flange temperature (at center of flange) above the temperature at the ends of the flange should not exceed 10°C.

Grounding the module to external circuitry through mounting screws only should be adequate to prevent spurious oscillations provided the ground contact does not become excessively resistive as a result of nickel oxide forming on the nickel plated flange. Nickel oxide (unlike copper and silver oxide) is resistive and its formation can lead to intermittent ground paths between the module and external circuits.

MHW801 Series

MHW801 modules are designed without "ears" on the flange. They should be attached to a heatsink with solder. When soldering, the primary consideration should be to prevent any part of the module flange from achieving a temperature greater than 165°C. A low temperature solder such as 52% In and 48% Sn (along with "R" type flux) is recommended because this solder liquifies below 150°C. Keep in mind that the internal construction of the module has been achieved using 36% Sn, 62% Pb and 2% Ag solder which liquifies at 179–180°C. If the module flange is allowed to achieve a temperature greater than 165°C, serious mechanical damage could occur with consequent failure to function electrically being the end result. Also, as stated on the data sheet, do not permit the module to be immersed in a flux removal system. The part is not hermetically sealed, and liquids could penetrate into the circuitry with potentially disasterous results.

MHW851 Series

MHW851 type modules have flanges with "ears" for attachment to a heatsink by means of screws. The cutouts at each end of the flange will accommodate 4–40 screws and these should be torqued to an amount no greater than 2 to 3 inch-pounds. The use of thermal grease is not recommended for the MHW851 Series module because the relatively low output power does not require intimate (thermal) contact of the flange surface to the heatsink. Use of thermal grease is permissible but care must be taken to prevent using an excessive amount. Since it is not needed, it is Motorola's recommendation that it not be used.

Flatness of the heatsink when using MHW851's is much less critical than that required for higher power modules. Motorola recommends that the heatsink surface be flat to within + or − 0.003 inches, a dimension that should be relatively easy to attain. The MHW801/851 Series module is constructed with a printed circuit board substrate which negates the stringent requirements for bending that are placed on ceramic substrate modules. Motorola believes that the MHW801/851 Series module can be distorted as much as 0.020 inches either concave or convex without damage to the module.

Because bending requirements are relaxed, it is also unnecessary to worry about tightening sequence as described in EB107 — "Mounting Considerations for Motorola RF Power Modules." This EB was written primarily for ceramic substrate modules and does not apply in total to printed circuit board substrate modules such as the MHW801/851 Series.

Understanding RF Data Sheet Parameters

by Norman E. Dye
RF Products Division

INTRODUCTION

Data sheets are often the sole source of information about the capability and characteristics of a product. This is particularly true of unique RF semiconductor devices that are used by equipment designers all over the world. Because the circuit designer often cannot talk directly with the factory, he relies on the data sheet for his device information. And for RF devices, many of the specifications are unique in themselves. Thus it is important that the user and the manufacturer of RF products speak a common language, i.e., what the semiconductor manufacturer says about his RF device is understood fully by the circuit designer.

This paper reviews RF transistor and amplifier module parameters from maximum ratings to functional characteristics. It is divided into 5 basic sections: 1) DC Specifications, 2) Power Transistors, 3) Low Power Transistors, 4) Power Modules and 5) Linear Modules. Comments are made about critical specifications, about how values are determined and what are their significance. A brief description of the procedures used to obtain impedance data and thermal data is set forth; the importance of test circuits is elaborated; and background information is given to help understand low noise considerations and linearity requirements.

DC SPECIFICATIONS

Basically RF transistors are characterized by two types of parameters: DC and functional. The "DC" specs consist (by definition) of breakdown voltages, leakage currents, h_{FE} (DC beta) and capacitances, while the functional specs cover gain, ruggedness, noise figure, Z_{in} and Z_{out}, S-parameters, distortion, etc. Thermal characteristics do not fall cleanly into either category since thermal resistance and power dissipation can be either DC or AC. Thus, we will treat the spec of thermal resistance as a special specification and give it its own heading called "thermal characteristics." Figure 1 is one page of a typical RF power data sheet showing DC and functional specs.

A critical part of selecting a transistor is choosing one that has breakdown voltages compatible with the supply voltage available in an intended application. It is important that the design engineer select a transistor on the one hand that has breakdown voltages which will NOT be exceeded by the DC and RF voltages that appear across the various junctions of the transistor and on the other hand has breakdown voltages that permit the "gain at frequency" objectives to be met by the transistor. Mobile radios normally operate from a 12 volt source; portable radios use a lower voltage, typically 6 to 9 volts; avionics applications are commonly 28 volt supplies while base station and other ground applications such as medical electronics generally take advantage of the superior performance characteristics of high voltage devices and operate with 24 to 50 volt supplies. In making a transistor, breakdown voltages are largely determined by material resistivity and junction depths (Figure 2). It is for these reasons that breakdown voltages are intimately entwined with functional performance characteristics. Most product portfolios in the RF power transistor industry have families of transistors designed for use at specified supply voltages such as 7.5 volts, 12.5 volts, 28 volts and 50 volts.

Leakage currents (defined as reverse biased junction currents that occur prior to avalanche breakdown) are likely to be more varied in their specification and also more informative. Many transistors do not have leakage currents specified because they can result in excessive (and frequently unnecessary) wafer/die yield losses. Leakage currents arise as a result of material defects, mask imperfections and/or undesired impurities that enter during wafer processing. Some sources of leakage currents are potential reliability problems; most are not. Leakage currents can be material related such as stacking faults and dislocations or they can be "pipes" created by mask defects and/or processing inadequacies. These sources result in leakage currents that are constant with time and if initially acceptable for a particular application will remain so. They do not pose long term reliability problems.

On the other hand, leakage currents created by channels induced by mobile ionic contaminants in the oxide (primarily sodium) tend to change with time and can lead to increases in leakage current that render the device useless for a specific application. Distinguishing between sources of leakage current can be difficult, which is one reason devices for application in military environments require HTRB (high temperature reverse bias) and burn-in testing. However, even for commercial applications particularly where battery drain is critical or where bias considerations dictate limitations, it is essential that a leakage current limit be included in any complete device specification.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)					
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	70	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	90	125	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 45 W, I_C(Max) = 5.8 Adc, f = 470 MHz)	G_{pe}	4.8	5.4	—	dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	P_{in}	—	13	15	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 45 W, I_C(Max) = 5.8 Adc, f = 470 MHz)	η	55	60	—	%
Load Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = Note 1, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ*	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	Z_{in}	—	1.4+j4.0	—	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	Z_{OL}*	—	1.2+j2.8	—	Ohms

Notes

1. P_{in} = 150% of Drive Requirement for 45 W output @ 12.5 V.

* ψ = Mismatch stress factor – the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 1) terminated in a 20:1 minimum load mismatch at all phase angles.

Figure 1. Typical DC and Functional Specifications

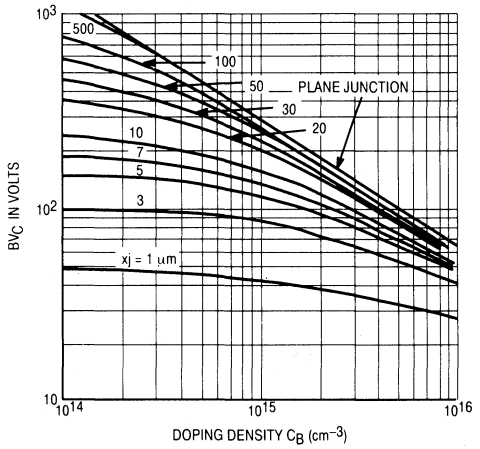


Figure 2. The Effect of Curvature and Resistivity on Breakdown Voltage

DC parameters such as h_{FE} and C_{ob} (output capacitance) need little comment. Typically, for RF devices, h_{FE} is relatively unimportant because the functional parameter of gain at the desired frequency of operation is specified. Note, though, that DC beta is related to AC beta (Figure 3). Functional gain will track DC beta particularly at lower RF frequencies. Generally RF device manufacturers do not like to have tight limits placed on h_{FE}. Primarily the reasons that justify this position are:

a) Lack of correlation with RF performance
b) Difficulty in control in wafer processing
c) Other device manufacturing constraints dictated by functional performance specs which preclude tight limits for h_{FE}.

A good rule of thumb for h_{FE} is to set a maximum-to-minimum ratio of not less than 3 and not more than 4 with the minimum h_{FE} value determined by an acceptable margin in functional gain.

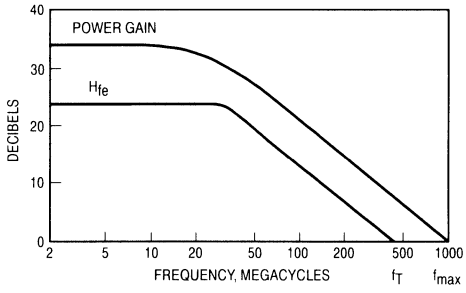


Figure 3. Beta versus Frequency

Output capacitance is an excellent measure of comparison of device size (base area) provided the majority of output capacitance is created by the base-collector junction and not parasitic capacitance arising from bond pads and other top metal of the die. Remember that junction capacitance will vary with voltage (Figure 4) while parasitic capacitance will not vary. Also, in comparing devices, one should note the voltage at which a given capacitance is specified. No industry standard exists. The preferred voltage at Motorola is the transistor V_{CC} rating, i.e., 12.5 volts for 12.5 volt transistors and 28 volts for 28 volt transistors, etc.

MAXIMUM RATINGS and THERMAL CHARACTERISTICS

Maximum ratings (shown for a typical RF power transistor in Figure 5) tend to be the most frequently misunderstood group of device specifications. Ratings for *maximum junction voltages* are straight forward and simply reflect the minimum values set forth in the DC specs for breakdown voltages. If the device in question meets the specified minimum breakdown voltages, then voltages less than the minimum will not cause junctions to reach reverse bias breakdown with the potentially destructive current levels that can result.

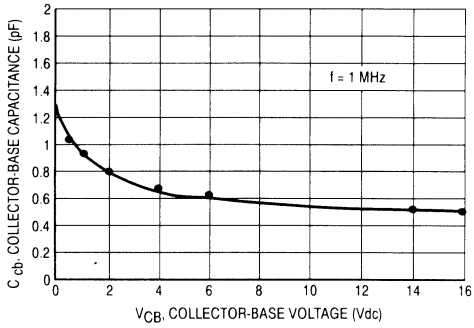


Figure 4. Junction Capacitance versus Voltage

The value of $V_{(BR)CEO}$ is sometimes misunderstood. Its value can approach or even equal the supply voltage rating of the transistor. The question naturally arises as to how such a low voltage can be used in practical applications. First, $V_{(BR)CEO}$ is the breakdown voltage of the collector-base junction plus the forward drop across the base-emitter junction with the base open, and it is never encountered in amplifiers where the base is at or near the potential of the emitter. That is to say, most amplifiers have the base shorted or they use a low value of resistance such that the breakdown value of interest approaches $V_{(BR)CES}$. Second, $V_{(BR)CEO}$ involves the current gain of the transistor and increases as frequency increases. Thus the value of $V_{(BR)CEO}$ at RF frequencies is always greater than the value at DC.

The maximum rating for *power dissipation* (P_D) is closely associated with thermal resistance (θ_{JC}). Actually maximum P_D is in reality a fictitious number — a kind of figure of merit — because it is based on the assumption that case temperature is maintained at 25°C. However, providing everyone arrives at the value in a similar manner, the rating of maximum P_D is a useful tool with which to compare devices.

The rating begins with a determination of thermal resistance — die to case. Knowing θ_{JC} and assuming a maximum die temperature, one can easily determine maximum P_D (based on the previously stated case temperature of 25°C). Measuring θ_{JC} is normally done by monitoring case temperature (T_C) of the device while it operates at or near rated output power (P_O) in an RF circuit. The die temperature (T_J) is measured simultaneously using an infra-red microscope (see Figure 6) which has a spot size resolution as small as 1 mil in diameter. Normally several readings are taken over the surface of the die and an average value is used to specify T_J.

It is true that temperatures over a die will vary typically 10–20°C. A poorly designed die (improper ballasting) could result in hot spot (worst case) temperatures that vary 40–50°C. Likewise, poor die bonds (see Figure 7) can result in hot spots but these are not normal characteristics of a properly designed and assembled transistor die.

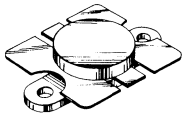
The RF Line
NPN Silicon RF Power Transistor

MRF650

50 WATTS, 512 MHz RF POWER TRANSISTOR NPN SILICON

. . . designed for 12.5 Volt Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 520 MHz.

- Guaranteed 440, 470, 512 MHz 12.5 Volt Characteristics
  Output Power = 50 Watts
  Minimum Gain = 5.2 dB @ 440, 470 MHz
  Efficiency = 55% @ 440, 470 MHz
  IRL = 10 dB
- Characterized with Series Equivalent Large-Signal Impedance Parameters from 400 to 520 MHz
- Built-In Matching Network for Broadband Operation
- Triple Ion Implanted for More Consistent Characteristics
- Implanted Emitter Ballast Resistors
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 15.5 Vdc, 2.0 dB Overdrive



CASE 316-01

MAXIMUM RATINGS			
Rating	**Symbol**	**Value**	**Unit**
Collector-Emitter Voltage	V_{CEO}	16.5	Vdc
Collector-Emitter Voltage	V_{CES}	38	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	12	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	135 0.77	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
THERMAL CHARACTERISTICS			
Characteristic	**Symbol**	**Max**	**Unit**
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	°C/W

Figure 5. Maximum Ratings of a Typical RF Power Transistor

By measuring T_C and T_J along with P_O and P_{in} — both DC and RF — one can calculate θ_{JC} from the formula $\theta_{JC} = (T_J - T_C)/(P_{in} - P_O)$. Typical values for an RF power transistor might be T_J = 130°C; T_C = 50°C; V_{CC} = 12.5 V; I_C = 12 A; Pin (RF) = 10 W; P_O (RF) = 50 W. Thus θ_{JC} = (130 − 50)/(10 + {12.5 x 12} − 30) = 80/80 = 1°C/W.

Several reasons dictate a conservative value be placed on θ_{JC}. First, thermal resistance increases with temperature (and we realize Tc = 25°C is NOT realistic). Second, T_J is not a worst case number. And, third, by using a conservative value of θ_{JC}, a realistic value is determined for maximum P_D. Generally, Motorola's practice is to publish θ_{JC} numbers approximately 25% higher than that determined by the measurements described in the preceding paragraphs, or for the case illustrated, a value of θ_{JC} = 1.25°C/W.

Now a few words are in order about die temperature. Reliability considerations dictate a safe value for an all Au (gold) system (die top metal and wire) to be 200°C. Once T_J max is determined, along with a value for θ_{JC}, maximum P_D is simply

$$P_D \text{ (max)} = (T_J \text{ (max)} - 25°C)/\theta_{JC}.$$

Specifying maximum P_D for T_C = 25°C leads to the necessity to derate maximum P_D for any value of T_C above 25°C. The derating factor is simply the reciprocal of θ_{JC}!

Maximum collector current (I_C) is probably the most subjective maximum rating on the transistor data sheets. It has

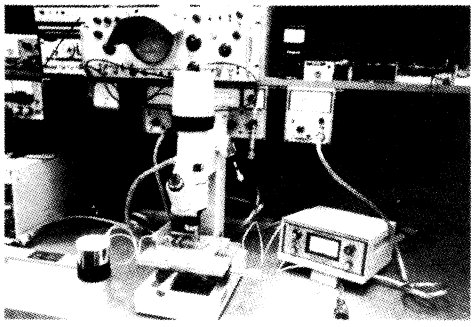


Figure 6. Equipment Used To Measure Die Temperature

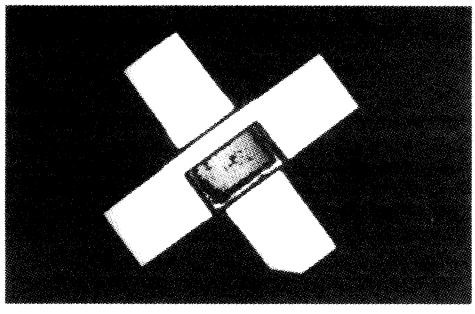


Figure 7. An Example of Incomplete Die Attach

been, and is, determined in a number of ways each leading to different maximum values. Actually, the only valid maximum current limitations in an RF transistor have to do with the current handling ability of the wires or the die. However, power dissipation ratings may restrict current to values far below what should be the maximum rating. Unfortunately, many older transistors had their maximum current rating determined by dividing maximum P_D by collector voltage (or be $V_{(BR)CEO}$ for added safety) but this is not a fundamental maximum current limitation of the part. Many lower frequency parts have relatively gross top metal on the transistor die, i.e., wide metal runners and the "weak current link" in the part is the current handling capability of the emitter wires (for common emitter parts). The current handling ability of wire (various sizes and material) is well known; thus the maximum current rating may be limited by the number, size and material used for emitter wires.

Most modern, high frequency transistors are die limited because of high current densities resulting from very small current carrying conductors and these densities can lead to metal migration and premature failure. The determination of I_C max for these types of transistors results from use of Black's equation for metal migration which determines a mean time between failures (MTBF) based on current density, temperature and type of metal. At Motorola, MTBF is generally set at >7 years and maximum die temperature at 200°C. For plastic packaged transistors, maximum T_J is set at 150°C. The resulting current density along with a knowledge of the die geometry and top metal thickness and material allows the determination of I_C max for the device.

It is up to the transistor manufacturer to specify an I_C max based on which of the two limitations (die, wire) is paramount. It is recommended that the circuit design engineer consult the semiconductor manufacturer for additional information if I_C max is of any concern in his specific use of the transistor.

Storage temperature is another maximum rating that is frequently not given the attention it deserves. A range of −55°C to 200°C has become more or less an industry standard. And for the single metal, hermetic packaged type of device, the upper limit of 200°C creates no reliability problems. However, a lower high temperture limitation exists for plastic encapsulated or epoxy sealed devices. These should not be subjected to temperatures above 150°C to prevent deterioration of the plastic material.

POWER TRANSISTORS — Functional Characteristics

The selection of a power transistor usually involves choosing one for a frequency of operation, a level of output power, a desired gain, a voltage of operation and preferred package configuration consistent with circuit construction techniques.

Functional characteristics of an RF power transistor are by necessity tied to a specific test circuit (an example is shown in Figure 8). Without specifying a circuit, the functional parameters of gain, reflected power, efficiency — even ruggedness — hold little meaning. Furthermore, most test circuits used by RF transistor manufacturers today (even those used to characterize devices) are designed mechanically to allow for easy insertion and removal of the device under test (D.U.T.). This mechanical restriction sometimes limits achievable device performance which explains why performance by users frequently exceeds that indicated in data sheet curves. On the other hand, a circuit used to characterize a device is usually narrow band and tunable. This results in higher gain than attainable in a broadband circuit. Unless otherwise stated, it can be assumed that characterization data such as P_O vs frequency is generated on a point-by-point basis by tuning a narrow band circuit across a band of frequencies and, thus, represents what can be achieved at a specific frequency of interest provided the circuit presents optimum source and load impedances to the D.U.T.

Broadband, fixed tuned test circuits are the most desirable for testing functional performance of an RF transistor. Fixed tuned is particularly important in assuring everyone — the manufacturer and the user — of product consistency, i.e., that devices manufactured tomorrow will be identical to devices manufactured today.

Tunable, narrow band circuits have led to the necessity for device users and device manufacturers to resort to the use of "correlation units" to assure product consistency over

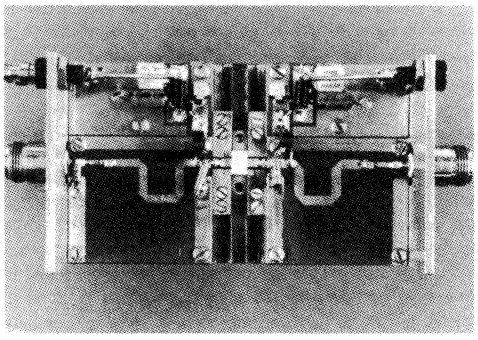


Figure 8. Typical RF Power Test Circuit

a period of time. Fixed tuned circuits minimize (if not eliminate) the requirements for correlation and in so doing tend to compensate for the increased constraints they place on the device manufacturer. On the other hand, manufacturers like tunable test circuits because their use allows adjustments that can compensate for variations in die fabrication and/or device assembly. Unfortunately gain is normally less in a broadband circuit that it is in a narrow band circuit, and this fact frequently forces transistor manufacturers to use narrow band circuits to make their product have sufficient attraction when compared with other similar devices made by competitors. This is called "specsmanship." One compromise for the transistor manufacturer is to use narrow band circuits with all tuning adjustments "locked" in place. For all of the above reasons, then, in comparing functional parameters of two or more devices, the data sheet reader should observe carefully the test circuit in which specific parameter limits are guaranteed.

For RF power transistors, the parameter of ruggedness takes on considerable importance. Ruggedness is the characteristic of a transistor to withstand extreme mismatch conditions in operation (which causes large amounts of output power to be "dumped back" into the transistor) without altering its performance capability or reliability. Many circuit environments particularly portable and mobile radios have limited control over the impedance presented to the power amplifier by an antenna, at least for some duration of time. In portables, the antenna may be placed against a metal surface; in mobiles, perhaps the antenna is broken off or inadvertently disconnected from the radio. Today's RF power transistor must be able to survive such load mismatches without any effect on subsequent operation. A truly realistic possibility for mobile radio transistors (although not a normal situation) is the condition whereby an RF power device "sees" a worst case load mismatch (an open circuit, any phase angle) along with maximum V_{CC} AND greater than normal input drive — all at the same time. Thus the ultimate test for ruggedness is to subject a transistor to a test wherein Pin (RF) is increased up to 50% above that value necessary to create rated P_O; V_{CC} is increased about 25% (12.5 V to 16 V for mobile transistors) AND then the load reflection coefficient is set at a magnitude of unity while its phase angle is varied through all possible values from 0 degrees to 360 degrees. Many 12 volt (land mobile) transistors are routinely given this test at Motorola Semiconductors by means of a test station similar to the one shown in Figure 9.

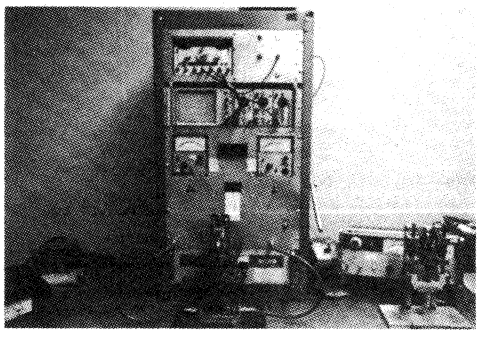


Figure 9. A Typical Functional Test Station

Ruggedness specifications come in many forms (or guises). Many older devices (and even some newer ones) simply have NO ruggedness spec. Others are said to be "capable of" withstanding load mismatches. Still others are guaranteed to withstand load mismatches of 2:1 VSWR to ∞:1 VSWR at rated output power. A few truly rugged transistors are guaranteed to withstand 30:1 VSWR at all phase angles (for all practical purposes 30:1 VSWR is the same as ∞:1 VSWR) with both over voltage and over drive. Once again it is up to the user to match his circuit requirements against device specifications.

Then as if the whole subject of ruggedness is not sufficiently confusing, the semiconductor manufacture slips in the ultimate "muddy the water" condition in stating what constitutes passing the ruggedness test. The words generally say that after the ruggedness test the D.U.T. "shall have no degradation in output power." A better phrase would be "no measurable change in output power." But even this is not the best. Unfortunately the D.U.T. can be "damaged" by the ruggedness test and still have "no degradation in output power." Today's RF power transistors consist of up to 1K or more low power transistors connected in parallel. Emitter resistors are placed in series with groups of these transistors in order to better control power sharing throughout the transistor die. It is well known by semiconductor manufacturers that a high percentage of an RF power transistor die (say up to 25–30%) can be destroyed with the transistor still able to deliver rated power at rated gain, at least for some period of time. If a ruggedness test destroys a high percentage of cells in a transistor, then it is likely that a 2nd ruggedness test (by the manufacturer or by the user while in his circuit) would result in additional damage leading to premature device failure.

A more scientific measurement of "passing" or "failing" a ruggedness test is called ΔV_{RE} — the change in emitter

resistance before and after the ruggedness test. V_{RE} is determined to a large extent by the net value of emitter resistance in the transistor die. Thus if cells are destroyed, emitter resistance will change with a resultant change in Vre. Changes as small as 1% are readily detectable, with 5% or less normally considered an acceptable limit. Today's more sophisticated device specifications for RF power transistors use this criteria to determine "success" or "failure" in ruggedness testing.

A circuit designer must know the input/output characteristics of the RF power transistor(s) he has selected in order to design a circuit that "matches" the transistor over the frequency band of operation. Data sheets provide this information in the form of large signal impedance parameters, Z_{in} and Z_{out} (commonly referred to as Z_{OL}*). Normally, these are stated as a function of frequency and are plotted on a Smith Chart and/or given in tabular form. It should be noted that Z_{in} and Z_{out} apply only for a specified set of operating conditions, i.e., P_O, V_{CC} and frequency. Both Z_{in} and Z_{out} of a device are determined in a similar way, i.e., place the D.U.T. in a tunable circuit and tune both input and output circuit elements to achieve maximum gain for the desired set of operating conditions. At maximum gain, D.U.T. impedances will be the conjugate of the input and output network impedances. Thus, terminate the input and output ports of the test circuit, remove the device and measure Z looking from the device — first, toward the input to obtain the conjugate of Z_{in} and, second, toward the output to obtain Z_{OL} which is the output load required to achieve maximum P_O.

A network analyzer is used in the actual measurement process to determine the complex reflection coefficient of the circuit using, typically, the edge of the package as a plane of reference. A typical measurement setup is shown in Figure 10. Figure 11 shows the special fixture used to obtain the short circuit reference while Figure 12 illustrates the adapter which allows the circuit impedance to be measured from the edge of the package.

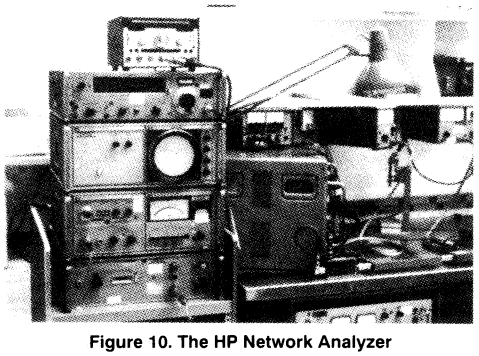


Figure 10. The HP Network Analyzer

Once the circuit designer knows Z_{IN} and Z_{OL}* of the transistor as a function of frequency, he can use computer

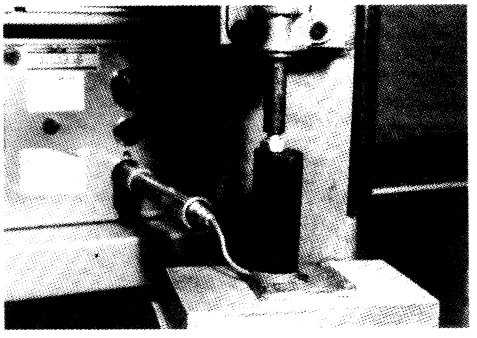


Figure 11. Short Circuit Reference Fixture

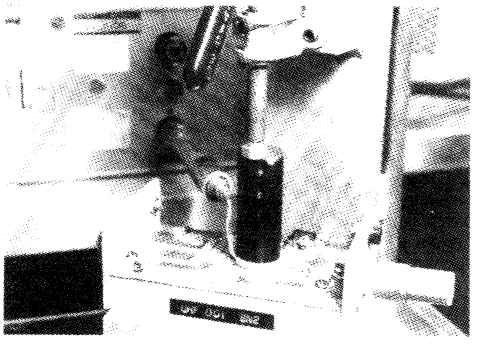


Figure 12. Adapter Used To Measure Circuit Impedance From Package

aided design programs to design L and C matching networks for his particular application.

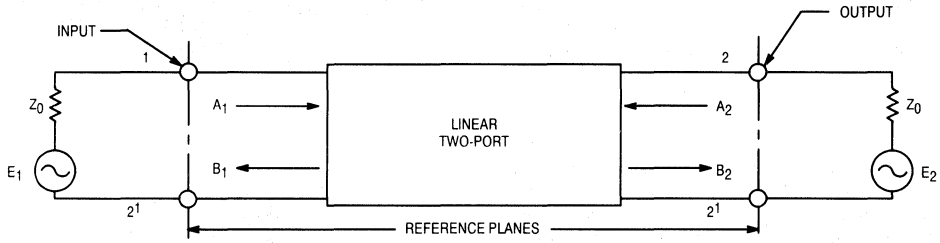
The entire impedance measuring process is somewhat laborious and time consuming since it must be repeated for each frequency of interest. Note that the frequency range permitted for characterization is that over which the circuit will tune. For other frequencies, additional test circuits must be designed and constructed, which explains why it is sometimes difficult to get a semiconductor manufacturer to supply impedance data for special conditions of operation such as different frequencies, different power levels or different operating voltages.

LOW POWER TRANSISTORS —
Functional Characteristics

Most semiconductor manufacturers characterize low power RF transistors for linear amplifier and/or low noise amplifier applications. Selecting a proper low power transistor involves choosing one having an adequate current rating, in the "right" package and with gain and noise figure capability that meets the requirements of the intended application.

One of the most useful means of specifying a linear device is by means of scattering parameters, commonly referred to as S-Parameters which are in reality voltage reflection and

transmission coefficients when the device is embedded into a 50 ohm system. See Figure 13. $|S_{11}|$, the magnitude of the input reflection coefficient is directly related to input VSWR by the equation VSWR = $(1 + |S_{11}|) / (1 - |S_{11}|)$. Likewise, $|S_{22}|$, the magnitude of the output reflection coefficient is directly related to output VSWR. $|S_{21}|^2$, which is the square of the magnitude of the input-to-output transfer function, is also the power gain of the device. It is referred to on data sheets as "Insertion Gain." Note, however, that $|S_{21}|^2$ is the power gain of the device when the source and load impedances are 50 ohms. An improvement in gain can always be acheived by matching the device's input and output impedances (which are almost always different from 50 ohms) to 50 ohms by means of matching networks. The larger the linear device, the lower the impedances and the greater is the need to use matching networks to achieve useful gain.



S_{11} ≡ INPUT REFLECTION COEFFICIENT = $\frac{b_1}{a_1}$

S_{22} ≡ OUTPUT REFLECTION COEFFICIENT = $\frac{b_2}{a_2}$

$|S_{21}|^2$ ≡ FORWARD TRANSDUCER GAIN = $\frac{b_2}{a_1}$

$|S_{12}|^2$ ≡ REVERSE TRANSDUCER GAIN = $\frac{b_1}{a_2}$

Figure 13. Two-Port S-Parameter Definitions

Another gain specification shown on low power data sheets is called "Associated Gain." The symbol used for Associated Gain is "G_{NF}." It is simply the gain of the device when matched for minimum noise figure. Yet another gain term is shown on some data sheets and it is called "Maximum Unilateral Gain." It's symbol is G_U max. As you might expect, G_U max is the gain achievable by the transistor when the input and output are conjugately matched for maximum power transfer (and $S_{12} = 0$.). One can derive a value for G_U max using scattering parameters:

$$G_U \text{ max} = |S_{21}|^2 / \{(1 - |S_{11}|^2 (1 - |S_{22}|^2)\}.$$

Simply stated, this is the 50 ohm gain increased by a factor which represents matching the input and increased again by a factor which represents matching the output.

Many RF low power transistors are used as low noise amplifiers which has led to several transistor data sheet parameters related to noise figure. NF_{min} is defined as the minimum noise figure that can be achieved with the transistor. To achieve this NF requires source impedance matching which is usually different from that required to achieve maximum gain. The design of a low noise amplifier, then, is always a compromise between gain and NF. A useful tool to aid in this compromise is a Smith Chart plot of constant gain and Noise Figure contours which can be drawn for specific operating conditions — typically bias and frequency. A typical Smith Chart plot showing constant gain and NF contours is shown in Figure 14. These contours are circles which are either totally or partially complete within the confines of the Smith Chart. If the gain circles are contained entirely within the Smith Chart, then the device is unconditionally stable. If portions of the gain circles are outside the Smith Chart, then the device is considered to be "conditionally stable" and the device designer must concern himself with instabilities, particularly outside the normal frequency range of operation.

If the data sheet includes Noise Parameters, a value will be given for the optimum input reflection coefficient to achieve minimum noise figure. Its symbol is Γ_o or sometimes Γ_{opt}. But remember if you match this value of input reflection coefficient you are likely to have far less gain than is achievable by the transistor. The input reflection coefficient for maximum gain is normally called Γ_{MS}, while the output reflection coefficient for maximum gain is normally called Γ_{ML}.

Another important noise parameter is noise resistance which is given the symbol R_n and is expressed in ohms. Sometimes in tabular form, you may see this value normalized to 50 ohms in which case it is designated r_n. The significance of r_n can be seen in the formula below which determines noise figure NF of a transistor for any source reflection coefficient Γ_S if the three noise parameters —

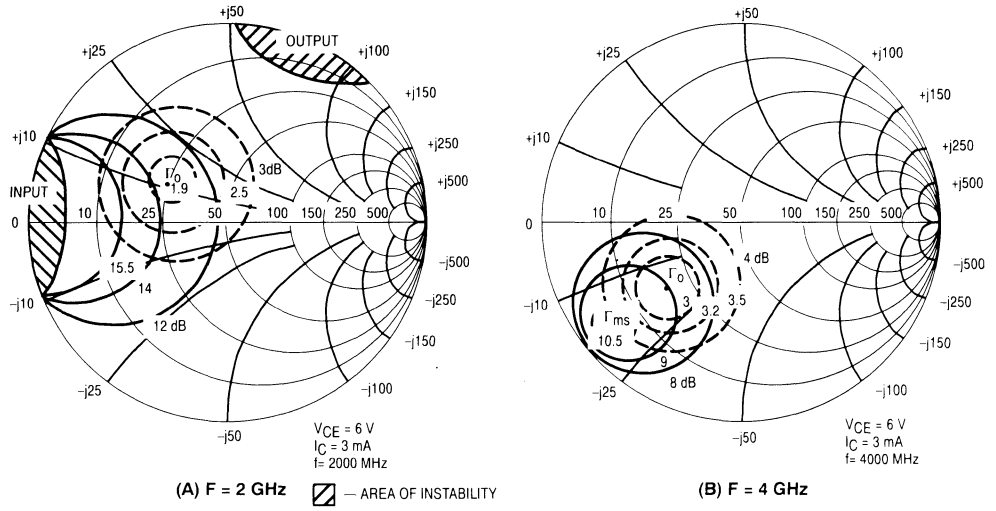


Figure 14. Gain & Noise Figure Contours

NF_{min}, r_n and Γ_o (the source resistance for minimum noise figure) — are known. Typical noise parameters taken from the MRF942 data sheet are shown in Figure 15.

$NF = NF_{min} + \{4r_n |\Gamma_s - \Gamma_o|^2\} / \{(1 - |\Gamma_s|^2) |1 + \Gamma_o|^2\}$.

The locus of points for a given NF turns out to be a circle (the NF_{min} circle being a point); thus, by choosing different values of NF one can plot a series of noise circles on the Smith Chart. Incidentally, r_n can be measured by measuring noise figure for $\Gamma_S = 0$ and applying the equation stated above.

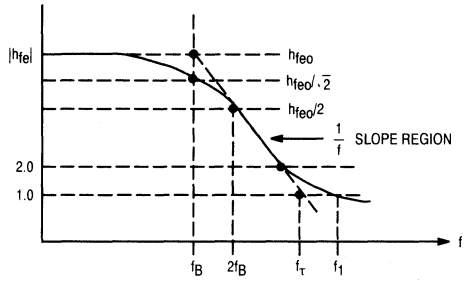
MRF942							
V_{CE} (Vdc)	I_C (mA)	f (MHz)	NF_{min} (dB)	G_{NF} (dB)	Γ_o (MAG, ANG)	R_N (ohms)	$NF_{50\ \Omega}$ (dB)
6	3	1000	1.3	16	.36 ∠ 94	17.5	1.7
		2000	2.0	11	.37 ∠ −145	15.5	2.6
		4000	2.9	8.0	.50 ∠ −134	21.5	4.3
	15	1000	2.1	19	.25 ∠ 150	13	2.6
		2000	2.7	14	.26 ∠ −173	16.5	3.1
		4000	4.3	9.0	.48 ∠ −96	47	5.4

Figure 15. Typical Noise Parameters

A parameter found on most RF low power data sheets is commonly called the current gain-bandwidth product. It's symbol is f_T. Sometimes it is referred to as the cutoff frequency because it is generally thought to be the product of low frequency current gain and the frequency at which the current gain becomes unity. While this is not precisely true (see Figure 16), it is close enough for practical purposes. And it is true that f_T is an excellent figure-of-merit which becomes useful in comparing devices for gain and noise figure capability. High values of ft are normally required to achieve higher gain at higher frequencies, other factors being equal. To the device designer, high f_T mean decreased spacings between emitter and base diffusions and it means shallower diffusions — things which are more difficult to achieve in making an RF transistor.

The complete RF low power transistor data sheet will include a plot of f_T versus collector current. Such a curve (as shown in Figure 17) will increase with current, flatten and then begin to decrease as I_C increases thereby revealing useful information about the optimum current with which to achieve maximum device gain.

Another group of characteristics associated with linear (or Class "A") transistors has to do with the degree to which the device is linear. Most common are terms such as "P_O, 1 dB Gain Compression Point" and "3rd Order Intercept Point (or ITO as it is sometimes called)." More will be said about



WHERE $|h_{fe}|$ = MAGNITUDE OF SMALL-SIGNAL COMMON-EMITTER (CE) SHORT-CIRCUIT (SC) CURRENT GAIN, h_{fe}

h_{feo} = LOW-FREQUENCY VALUE OF h_{fe}

f_B = 3 dB CUTOFF FREQUENCY FOR CE, SC CURRENT GAIN

f_T = TRANSITION FREQUENCY = $|h_{fe}| \bullet f_{MEAS}$

WHERE $f_{MEAS.}$ = FREQUENCY OF MEASUREMENT

(NOTE: $2 \leq |h_{fe}| \leq \frac{h_{feo}}{2}$)

f_1 = FREQUENCY AT WHICH $|h_{fe}| = 1$

Figure 16. Small Signal Current Gain versus Frequency

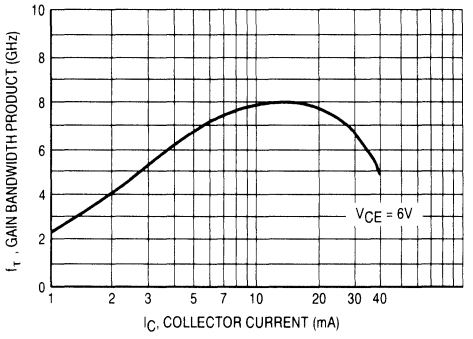


Figure 17. Gain-Bandwidth Product versus Collector Current

non-linearities and distortion measurements in the section about Linear Amplifiers; however, suffice it to be said now that "P_O, 1 dB Gain Compression Point" is simply the output power at which the input power has a gain associated with it that is 1 dB less than the low power gain. In other words, the device is beginning to go into "saturation" which is a condition where increases in input power fail to realize increases in output power. The concept of gain compression is illustrated in Figure 18.

The importance of the "1 dB Gain Compression Point" is that this is generally accepted as the limit of non-linearity that is tolerable in a "linear" amplifier and leads one to the dynamic range of the low power amplifier. On the low end of dynamic range is the limit imposed by noise, and on the high end of dynamic range is the limit imposed by "gain compression."

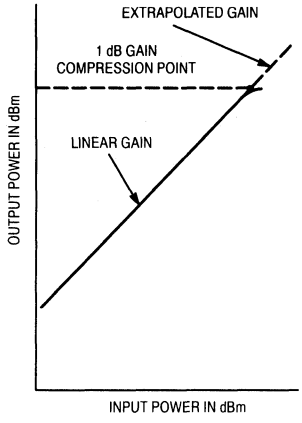


Figure 18. Linear Gain and 1 dB Compression Point

LINEAR MODULES — Functional Characteristics

Let's turn now to amplifiers and examine some specifications encountered that are unique to specific applications. Amplifiers intended for cable television applications are selected to have the desired gain and distortion characteristics compatible with the cable network requirements. They are linear amplifiers consisting of 2 or more stages of gain each using a push-pull cascode configuration. Remember that a cascode stage is one consisting of 2 transistors in which a common emitter stage drives a common base stage. A basic circuit configuration is shown in Figure 19. Most operate from a standard voltage of 24 volts and are packaged in an industry standard configuration shown in Figure 20. Because they are used to "boost" the RF signals that have been attenuated by the losses in long lengths of coaxial cable (the losses of which increase with frequency), their gain characteristics as a function of frequency are very important. These are defined by the specifications of "slope" and "flatness" over the frequency band of interest. Slope is defined simply as the difference in gain at the high and low end of the frequency band of the amplifier. Flatness, on the other hand, is defined as the deviation (at any frequency in the band) from an ideal gain which is determined theoretically by a universal cable loss function. Motorola normally measures the peak-to-valley (high-to-low) variations in gain across the frequency band, but specifies the flatness as a "plus, minus" quantity because it is assumed that cable television system designers have the capability of adjusting overall gain level.

The frequency band requirements of a CATV amplifier are determined by the number of channels used in the CATV system. Each channel requires 6 MHz bandwidth (to handle conventional color TV signals). Currently available models in the industry have bandwidths extending from 40 to 550 MHz and will accommodate up to 77 channels, the center

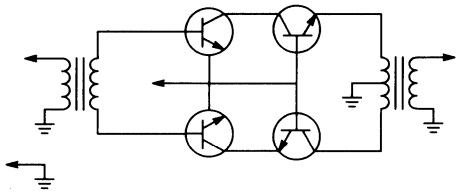


Figure 19. Basic CATV Amplifier

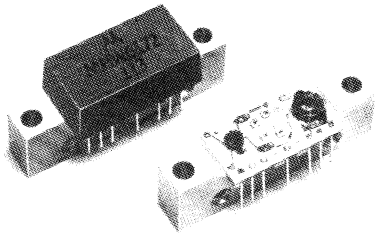


Figure 20. Standard CATV Package (Case 714-04)

frequencies of which are determined by industry standard frequency allocations.

Because CATV amplifiers must amplify TV signals and they must handle many channels simultaneously, these amplifiers must be extremely linear. The more linear, the less distortion that is added to the signal and, thus, the better is the quality of the TV picture being viewed. Distortion is generally specified in 3 conventional ways — 2nd Order Intermodulation Distortion (IMD), Cross Modulation Distortion (XMD) and Composite Triple Beat (CTB). In order to better understand what these terms mean, a few words need to be said about distortion in general

First, let's consider a perfectly linear amplifier. The output signal is exactly the same as the input except for a constant gain factor. Unfortunately, transistor amplifiers are, even under the best of circumstances, not perfectly linear. If one were to write a transfer function for a transistor amplifier, a typical input-output curve for which is shown in Figure 21, he would find the region near zero to be one best represented by "squared" terms, i.e., the output is proportional to the square of the input. And the region near saturation, i.e., where the amplifier produces less incremental output for incremental increases in input is best represented by "cubed" terms, i.e., the output is proportional to the cube of the input. A mathematically rigorous analysis of the transfer function of an amplifier would include an infinite number of higher order terms. However, an excellent approximation is obtained by considering the first three terms, i.e., make the assumption we can write

$F(x) = C_1x + C_2x^2 + C_3x^3$,

where F is the output signal and x is the input signal. C_1, C_2 and C_3 are constants that represent the transfer function (gain) for the first, second and third order terms.

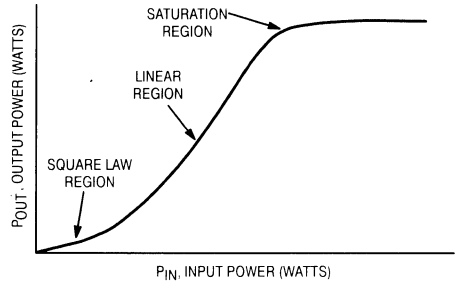


Figure 21. Transfer Function for Typical Transistor

Now consider a relatively simple input signal consisting of 3 frequencies each having a constant amplitude A. (In the case of CATV amplifiers, there could be 50–60 channels each having a carrier frequency and associated modulation frequencies spread over a bandwidth approaching 6 MHz.) The input signal x then equals $A\cos\omega_1 t + A\cos\omega_2 t + A\cos\omega_3 t$. If we apply this input signal to the transfer function and calculate F(x), we will find many terms involving x, x^2 and x^3. The "x" terms represent the "perfect", linear amplification of the input signal. Terms involving x^2 when analyzed on a frequency basis result in signal components at two times the frequencies of f_1, f_2 and f_3. Also created by x^2 terms are signal components at sums and difference frequencies of all combinations of f_1, f_2 and f_3. These are called 2nd order intermodulation components. Likewise, the terms involving x^3 result in frequency components at three times the frequencies of f_1, f_2 and f_3. And there are also frequency components at sum and difference frequencies (these are called 3rd order IMD). But in addition there are frequency components at $f_1 +,- f_2 +,- f_3$. These are called "triple beat" terms. And this is not all! A close examination reveals additional amplitude components at the original frequencies of f_1, f_2 and f_3. These terms can both "enhance" gain (expansion) or "reduce" gain (compression). The amplitude of these expansion and compression terms are such that we can divide the group of terms into two categories — "self-expansion/compression" and "cross-expansion/compression." Self-expansion/compression terms have amplitudes determined by the amplitude of a single frequency while cross-expansion/compression terms have amplitudes determined by the amplitudes of two frequencies. A summary of the terms that exist in this "simple" example is given in Table 1.

Table 1.
Terms in Output for Three Frequency Signal at Input

FIRST ORDER COMPONENTS	COMMENTS
$k1A \cos a + k1B \cos b + k1C \cos c$	Linear Amplification
SECOND ORDER DISTORTION COMPONENTS	
$k_2A^2/2 + k_2B^2/2 + k_2C^2/2$	3 DC components
$k_2AB \cos(a+,-b) + k_2AC \cos(a+,-c) + k_2BC \cos(b+,-c)$	6 Sum & Difference Beats
$k_2A^2/2 \cos 2a + k_2B^2/2 \cos 2b + k_2C^2/2 \cos 2c$	3-2nd Harmonic Component
THIRD ORDER DISTORTION COMPONENTS	
$k_3A^3/4 \cos 3(a) + k_3B^3/4 \cos 3(b) + k_3C^3/4 \cos 3(c)$	3-3rd Harmonic Components
$3k_3A^2B/4 \cos(2a+,-b) + 3k_3A^2C/4 \cos(2a+,-c) + 3k_3B^2A/4 \cos(2b+,-a) + 3k_3B^2C/4 \cos(2b+,-c) + 3k_3C^2A/4 \cos(2c+,-a) + 3k_3C^2B/4 \cos(2c+,-b)$	12 Intermodulation Beats
$3k_3ABC/2 \cos(a+,-b+,-c)$	4 Triple Beat Components
$3k_3A^3/4 \cos(a) + 3k_3B^3/4 \cos(b) + 3k_3C^3/4 \cos(c)$	3 Self Compression (k_3 is +) or Self Expansion (k_3 is –)
$3k_3AB^2/2 \cos(a) + 3k_3AC^2/2 \cos(a) + 3k_3BA^2/2 \cos(b) + 3k_3BC^2/2 \cos(b) + 3k_3CA^2/2 \cos(c) + 3k_3CB^2/2 \cos(c)$	6 Cross Compression (k_3 is + or Cross Expansion (k_3 is –)

Before going into an explanation of the tests performed on linear amplifiers such as CATV amplifiers, it is appropriate to review a concept called "intercept point." It can be shown mathematically that 2nd order distortion products have amplitudes that are directly proportional to the square of the input signal level, while 3rd order distortion products have amplitudes that are proportional to the cube of the input signal level. Hence, it can be concluded that a plot of each response on a log-log scale (or dB/dB scale) will be a straight line with a slope corresponding to the order of the response. Fundamental responses will have a slope of 1, the 2nd order responses will have a slope of 2 and the 3rd order responses a slope of 3. Note that the difference between fundamental and 2nd order is a slope of 1 and between fundamental and 3rd order is a slope of 2. That is to say, for 2nd order distortion, a 1 dB change in signal level results in a 1 dB change in 2nd order distortion; however, a 1 dB change in signal level results in a 2 dB change in 3rd order distortion. This is shown graphically in Figure 22. Using the curves of Figure 22, if the output level is 0 dBm, 2nd order distortion is at –30 dBc and 3rd order distortion is at –60 dBc. If we change the output level to –10 dBm, then 2nd order distortion should improve to –40 dBc (–50dBm) but 3rd order distortion will improve to –80 dBc (–90 dBm). Thus we see that a 10 dB decrease in signal has improved 2nd order distortion by 10 dB and 3rd order distortion has improved by 20 dB.

Now for "intercept point." We define the "intercept point" as the point on the plot of fundamental response and 2nd (or 3rd) order response where the two straight lines intercept each other. It is also that value of signal (hypothetical) at which the level of distortion would equal the initial signal level. For example, if at our point of measurement, the 2nd order

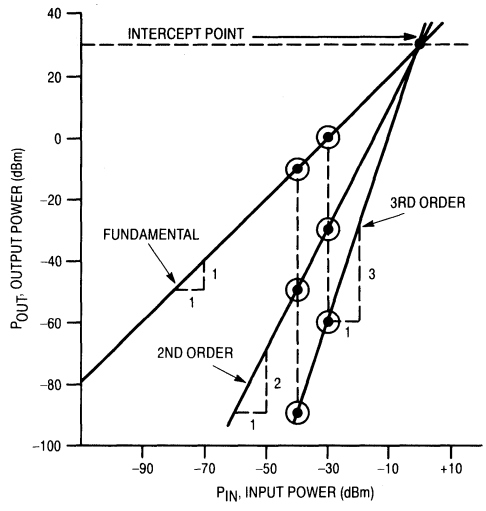


Figure 22. Amplifier Response Curves

distortion is –40 dBc and the signal level is –10 dBm; then the 2nd order intercept point is 40 dB above –10 dBm or +30 dBm. Note in Figure 22 that +30 dBm is the value of output signal at which the fundamental and 2nd order response lines cross. The beauty of the concept of "intercept point" is that once you know the intercept point, you can determine the value of distortion for any signal level — provided you are in a region of operation governed by the mathematical relationships stated, which typically means IMD's greater than 60 dB below the carrier.

Likewise to determine 3rd order intercept point, one must measure 3rd order distortion at a known signal level. Then take half the value of the distortion (expressed in dBc) and add to the signal level. For example, if the signal level is +10 dBm and the 3rd order distortion is –40 dBc, the 3rd order intercept point is the same as the 2nd order intercept point or 10 dBm + 20 dB = 30 dBm. Both 2nd order and 3rd order intercept points are illustrated in Figure 22 using the values assumed in the preceding examples. Note, also, that in general the intercept point for 2nd and 3rd order distortion will have the same value unless circuits are used that suppress even-order spurious responses, etc. However, even in this situation the concept of intercept point is still valid; the slopes of the responses are still 1, 2 and 3 respectively and all that needs to be done is to specify a 2nd order intercept point different from the 3rd order intercept point.

With this background information, let's turn to specific distortion specifications listed on many RF linear amplifier data sheets. If the amplifiers are for use in cable television distribution systems, as previously stated, it is common practice to specify Second Order Intermodulation Distortion, Cross Modulation Distortion and Composite Triple Beat. We will examine these one at a time. First, consider Second Order Intermodulation Distortion (IMD). Remember these are

unwanted signals created by the sums and differences of any two frequencies present in the amplifier. IMD is normally specified at a given signal output level and involves 3 channels — two for input frequencies and one to measure the resulting distortion frequency. The channel combinations are standardized in the industry but selected in a manner that typically gives a worst case condition for the 2nd order distortion results. An actual measurement consists of creating output signals (unmodulated) in the first two channels listed and looking for the distortion products that appear in the 3rd channel. If one wishes to predict the 2nd order IMD that would occur if the signals were stronger (or weaker), it is only necessary to remember the 1:1 relationship that led to a 2nd Order Intercept Point. In other words, if the specification guarantees an IMD of –68 dB Max. for a Vout = +46 dBmV per channel, then one would expect an IMD of –64 dB Max for a V_{out} = +50 dBmV per channel, etc.

Cross Modulation Distortion (XMD) is a result of the cross-compression and cross-expansion terms generated by the third order non-linearity in the amplifier's input-output transfer function. In general, the XMD test is a measurement of the presence of modulation on an unmodulated carrier caused by the distortion contribution of a large number of modulated carriers. The actual measurement consists of modulating each carrier with 100% square wave modulation at 15.75 kHz. Then the modulation is removed from one channel and the presence of residual modulation is measured with an amplitude modulation (AM) detector such as the commercially available Matrix RX12 distortion analyzer. Power levels and frequency relationships present in the XMD test are shown in Figure 23.

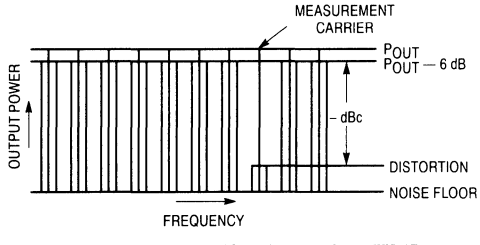


Figure 23. Frequency — Power Relationships for XMD

Composite Triple Beat (CTB) is quite similar to XMD except all channel frequencies are set to a specified output level without modulation. Then one channel frequency is removed and the presence of signal at that frequency is measured. The signals existing in the "off" channel are a result of triple beats (the mixing of 3 signals) among the host of carrier frequencies that are present in the amplifier. A graphical representation of the CTB test is shown in Figure 24.

European cable television systems usually invoke an additional specification for linear amplifiers which is called the DIN test. DIN is a German standard meaning Deutsche

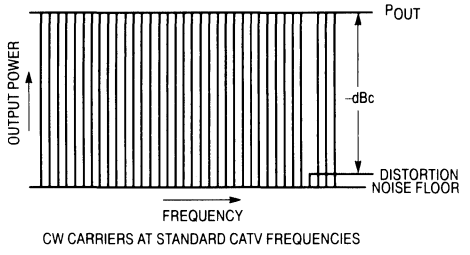


Figure 24. Frequency — Power Relationships for CTB

Industrie Norm (German Industrial Standard) and the standard that applies for CATV amplifiers is #45004B. DIN45004B is a special case of a three channel triple beat measurement in which the signal levels are adjusted to produce a –60 dBc distortion level. An additional difference from normal triple beat measurements is the fact that the levels are different for the three combining signals. If we call the four frequencies involved in the measurement F, F_1, F_2 and F_m, then F is set at the required output level that, along with F_1 and F_2 lead to a distortion level 60 dB below the level of F, and F1 and F_2 are adjusted to a level 6 dB below the level of F. Distortion is measured at the frequency F_m. Frequency relationships (used by Motorola) between F, F_1, F_2 and F_m are as follows: F_1 = F – 18 MHz; F_2 = F – 12 MHz and F_m = F + F_2 – F_1. Figure 25 illustrates the frequency and power level relationships that exist in the DIN test.

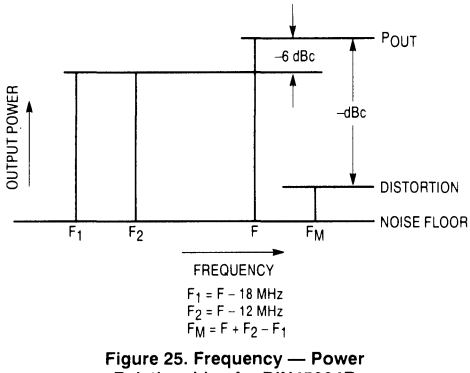


Figure 25. Frequency — Power Relationships for DIN45004B

Linear amplifiers aimed at television transmitter applications will generally have another distortion test involving 3 frequencies. Basically it is another 3rd order intermodulation test with power levels and frequencies that simulate a TV signal. Relative power levels and frequencies are shown in Figure 26.

Thermal resistance ratings of CATV modules (as well as Power modules described in the next section) are, perhaps,

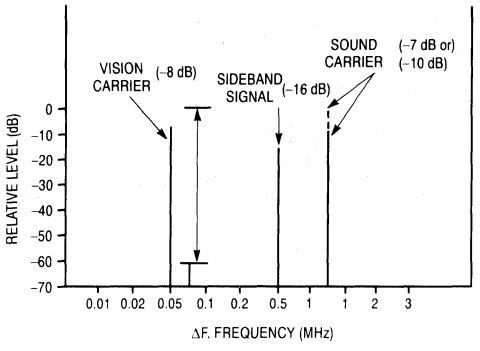


Figure 26. 3rd Order IMD Test for TV

conspicuous by their absence. Because the amplifiers have several heat sources that are contained within the amplifier, it is necessary for the user to provide sufficient heat sinking to the case of the amplifier such that the operating case temperature never exceeds its maximum rating. Actual power dissipation can be determined by considering the operating voltage and the maximum current rating of the device. Actual RF power output of most CATV modules is at most a few milliwatts which means that most of the power consumed by the module is dissipated in the form of heat. Typically this power dissipation runs in the range of 5 watts for conventional modules such as the MHW5122A but can increase to 10 watts for a power doubler such as the MHW5185.

Because linear (and power) modules have inputs and outputs that are matched to standard system impedances (75 ohms for CATV amplifiers and 50 ohms for power amplifiers), test circuits and fixtures are generally less important than for discrete devices. Basically test fixtures for modules are simply means of making RF and DC power connections to the module being tested. It is important if you build your own test fixture that you carefully decouple the DC power lines and that you provide adequate heat sinking for the device under test (D.U.T.). However, if the fixture is for linear modules involving low values of input and output VSWR, then it is extremely important, for accuracy, that the input and output networks (lines and connectors) be designed to exhibit return losses greater than 35 dB. Motorola modifies the RF connectors used in the fixture and, then, calibrates their fixtures to be sure that the fixture does not introduce errors in measuring module return loss.

POWER MODULES — Functional Characteristics

Power modules are generally used to amplify the transmit signals in a 2-way radio to the desired level for radiation by the antenna. They consist of several stages of amplification (usually common emitter, Class C except for some low level stages that are Class A) combined in a hybrid integrated assembly with nominally 50 ohm RF input and output impedances. Selection of a module involves choosing one having the proper operating voltage, frequency range, output power, overall gain and mechanical form factor suitable for a particular application.

Power modules for mobile and portable radios also have unique specifications related to their applications. One of the most significant is that of stability. The stability of a module is affected not only by its design but also by many external factors such as load and source impedances, by the value of supply voltage and by the amount of RF input signal. External factors influencing stability are highlighted in Figure 27. Combinations of these factors over a range of values for each factor must be considered to be certain the module will remain stable under typical conditions of operation. The greater the range of values for which stability is guaranteed, the more stable is the module. Of particular importance is the degree of load mismatch which can be tolerated as evidenced by the stated value of load VSWR (the larger the value, the better). Stability specifications are generally evaluated thoroughly during the pre-production phase and then guaranteed but not tested on a production basis.

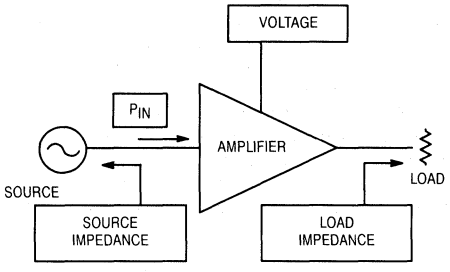


Figure 27. External Factors Affecting Stability

Efficiency is becoming an increasingly important specification particularly in modules for portable radio applications. The correct way to specify efficiency is to divide the net increase in RF power (output power minus input power) by the total DC power consumed by the module. It is generally specified at rated output power because efficiency will decrease when the module is operated at lower power levels. Be careful that the specification includes the current supplied for biasing and for stages other than the output stage. Overlooking these currents (and the DC power they use) results in an artifically high value for module efficiency.

Most power module data sheets include a curve of output power versus temperature. Some modules specify this "power slump" in terms of a minimum power output at a stated maximum temperature; others state the maximum permissible decrease in power (in dB) referenced to rated power output. It is important to note the temperature range and the other conditions applied to the specification before passing judgement on this specification.

Generally power modules, like linear modules, do not have thermal resistance specified from die to heatsink. For multiple stage modules, there would need to be a specific thermal

resistance from heatsink to each die. Thermal design of the module will take care of internal temperature rises provided the user adheres to the maximum rating attached to the operating case temperature range. This is an extremely important specification, particularly at the high temperature end because of two factors. First, exceeding the maximum case temperature can result in die temperatures that exceed 200°C. This, in turn, will lead as a minimum to decreased operating life and as a maximum to catastrophic failure as a result of thermal runaway destroying the die. Second, hybrid modules have components that are normally attached to a circuit board and the circuit board attached to the flange with a low temperature solder which may become liquid at temperatures as low as 125°C. Again, the power to be dissipated can be determined by considering the RF output power and the minimum efficiency of the module. For example, for the MHW607, output power is 7 watts and input power is 1 mW; efficiency is 40% minimum. Thus the DC power input must be 7/0.4 =17.5 watts. It follows that power dissipation would be 17.5–7 = 10.5 watts worst case.

Storage temperature maximum values are also important as a result of the melting temperatures of solder used in assembly of the modules. Another factor is the epoxy seal used to attach the cover to the flange. It is a material similar to that used in attaching caps for discrete transistors and, as stated earlier, is known to deteriorate at temperatures greater than 150°C.

Modules designed for use in cellular radios require wide dynamic range control of output power. Most modules provide for gain control by adjusting the gain of one (or two) stages by means of changing the voltage applied to that stage(s). Usually the control is to vary the collector voltage applied to an intermediate stage. A maximum voltage is stated on the data sheet to limit the control voltage to a safe value. This form of gain control is quite sensitive to small changes in control voltage as is evidenced by viewing the output power versus control voltage curves provided for the user (an example is shown in Figure 28). An alternative control procedure which uses much less current is to vary the base-to-emitter voltage of the input stages (which are generally class A) as illustrated in Figure 29. This is of particular significance in portables because of the power dissipated in the control network external to the module.

While not stated on most data sheets, it is always possible to control the output power of the module by controlling the RF input signal. Normally this is done by means of a PIN diode attenuator. Controlling the RF input signal allows the module to operate at optimum gain conditions regardless of output power. Under these conditions, the module will produce less sideband noise, particularly for small values of output power, when compared to the situation that arises from gain control by gain reduction within the module.

Noise produced by a power module becomes significant in a duplexed radio in the frequency band of the received signal (see Figure 30). A specification becoming more prominent, therefore, in power modules is one that controls the maximum noise power in a specified frequency band a given

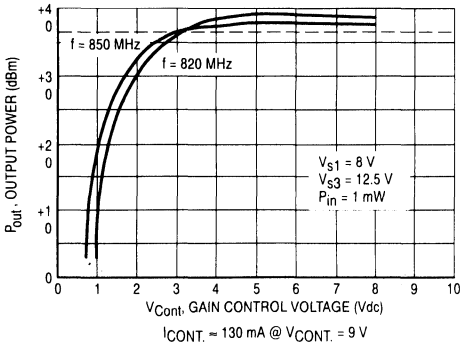


Figure 28. Output Power versus Gain Control Voltage

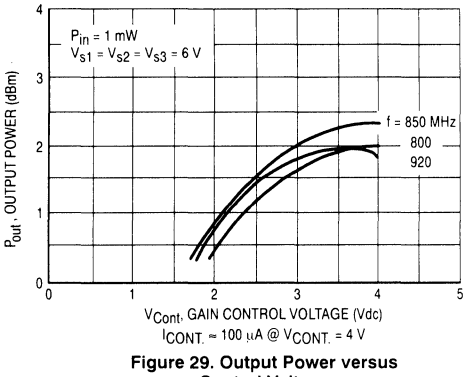


Figure 29. Output Power versus Control Voltage

distance from the transmit frequency. Caution must be taken in making measurements of noise power. Because the levels are generally very low (–85 dBm), one must be assured of a frequency source driving the module that has extremely low noise. Any noise on the input signal is amplified by the module and cannot be discerned from noise generated within the module. Another precaution is to be sure that the noise floor of the spectrum analyzer used to measure the noise power is at least 10 dB below the level to be measured.

DATA SHEETS OF THE FUTURE

World class data sheets in the next few years will tend to provide more and more information about characteristics of the RF device; information that will be directly applicable by the engineer in using the device. Semiconductor manufacturers such as Motorola will provide statistical data about parameters showing mean values and sigma deviations. For discrete devices, there will be additional data for computer aided circuit design such as SPICE constants. The use of typical values will become more widespread; and, the availability of statistical data and the major efforts to make more consistent products (six-sigma quality) will increase the usefulness of these values.

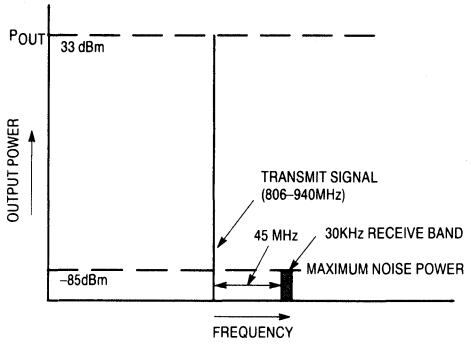


Figure 30. Noise Power in Receive Band

SUMMARY

Understanding data sheet specifications and what they mean can be a major asset to the circuit designer as he goes about selecting and using RF semiconductors for his specific application. This paper has emphasized some unique data sheet parameters of RF transistors and amplifiers and has explained what these mean from the semiconductor manufacturer's point-of-view. It is hoped this effort will help the circuit engineer make his selection and use of RF semiconductors more efficient and effective.

The RF transistor and the amplifiers made with RF transistors are unusually complex semiconductor products and difficult to fully characterize. Not all information about RF device characteristics has been explained in this paper. Nor can all be covered in a data sheet. The circuit design engineer should contact the device manufacturer for more detailed information whenever it is appropriate. Most if not all current manufacturers of RF transistors and amplifiers have extensive applications support for the express purpose of assisting the circuit designer whenever and wherever assistance is needed.

AN1122

Running the MC44802A PLL Circuit

Prepared by
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Bipolar Analog IC Division

INTRODUCTION

The MC44802A is the PLL portion of a tuning circuit intended for applications involving television, FM radio, and Set-Top converters up to 1.3 GHz. Coupled with a VCO and mixer, a complete tuning circuit can be formed. The tuning frequency is controlled through an MCU serial interface (I^2C).

As noted in the MC44802A data sheet, an MCU is recommended for sending the serial control bytes. This application note describes combining an MC68HC11E9 with an MC44802A in a tuner design. The information is sufficiently general however, that most any MCU could be used for this function. Those with a limited background in the use and programming of MCUs will find the information adequately detailed to permit a thorough understanding.

A Look at the MC44802A

The MC44802A is manufactured using Motorola's high density bipolar MOSAIC process. It features:

- I^2C interface for MCU control.
- Selectable ÷8 prescaler and a 15-bit divider accept frequencies up to 1.3 GHz.
- Programmable reference divider.
- Phase/frequency comparator output can be set to high impedance for disabling.
- Op amp provides direct tuning voltage output (0.3 V to 30 V).
- Seven programmable output buffers (10 mA, 12 V) for band switching, etc.
- Output options for 62.5 kHz, reference frequency and the programmable divider which are useful for system debugging.

Figure 1 shows a simplified block diagram of the MC44802A. The I^2C Bus receiver is a central block that controls the HF prescaler, 15-bit divider, the oscillator (typ. 4.0 MHz crystal) reference divider, and the output buffers.

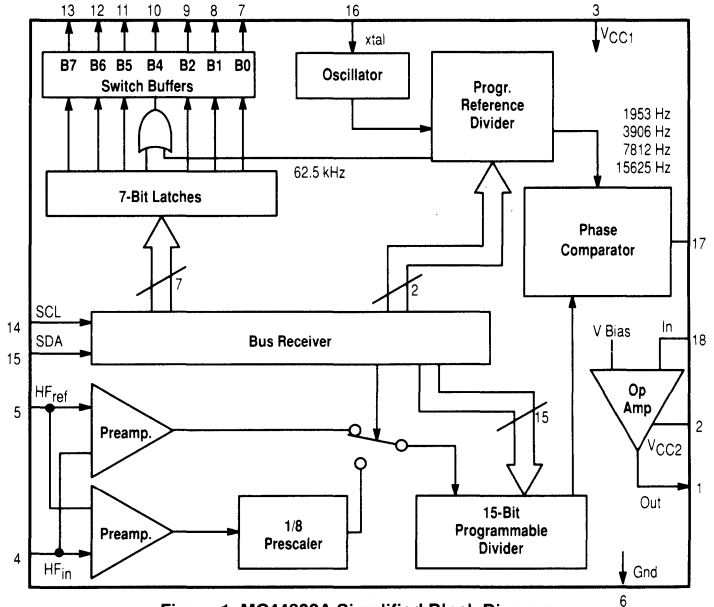

Figure 1. MC44802A Simplified Block Diagram

The I²C Bus

The I²C (Inter-Integrated Circuit) Bus required by the MC44802 is a serial transfer process using two wires for data and clock (SDA — serial data, SCL — serial clock). Each transfer is initiated by a master and acknowledged by a slave device. Each slave is assigned a unique address, allowing multiple I²C devices to be connected to a single bus. An example of a data transfer is shown in Figure 2.

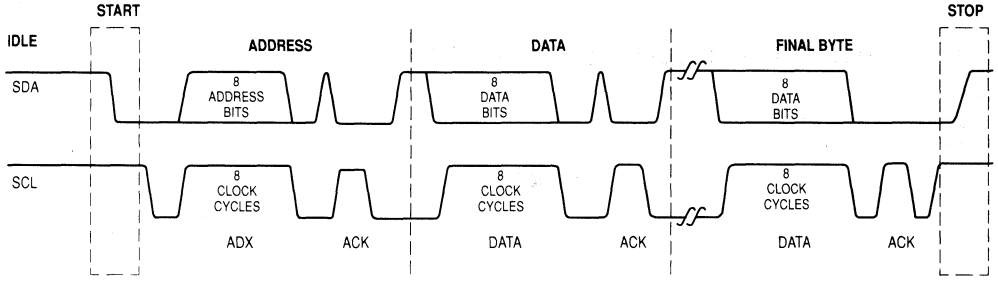

Figure 2. Complete Data Transfer Process

Referring to Figure 2:

Idle — When there are no transfers taking place on the bus, SDA and SCL idle high.

Start — A master initiates a data transfer by pulling SDA low while maintaining SCL in the high state. At this time all slave devices on the bus are listening for their address.

Address — The first byte is sent to select a slave device(s). Slaves that have read and write capabilities have a unique address for each. Upon completion of an address transmission, the master must leave the data line high and create the ACK clock pulse. The slave device is to acknowledge by pulling the data line to a stable low state before the end of the ACK pulse. From this point until a Stop Condition is generated, only the selected slave(s) device is active.

Data — The transfer continues with data bytes sent in the same manner as the address byte. An acknowledge is required at the end of each byte (except the last one). The master indicates the last data byte by sending the acknowledge (low) bit rather than leaving SDA high for slave acknowledge.

Stop — The master creates a Stop Condition by sending SCL high followed by a low-to-high SDA transition. This leaves the bus back in the idle state.

If a required acknowledge bit is not received for any reason, the master terminates the transfer and generates a Stop Condition.

The Microcontroller

The MCU chosen for an I²C data transfer must have a serial port with the following characteristics:

— Two-lines, clock and data, with open drain (collector) outputs
— 8-bit transfer buffer
— An I²C interface or I/O serial lines capable of emulating I²C protocol (Idle, Start/Stop conditions and ACK pulse).

Suitable microcontroller examples are the MC68HC11 or MC68HC05 families.

A SAMPLE SYSTEM

Overview

The remainder of this application note is devoted to describing a sample MC44802A system. From a high level view this system is simple (see Figure 3). Whenever the push button is pressed the circuit responds by changing the tuning frequency, and provides a display indicating the frequency. The following paragraphs describe this system which was built and tested to demonstrate the functionality of the MC44802A. Included are descriptions of each segment of this system — PLL tuning circuit, MCU control, user interface and LED displays.

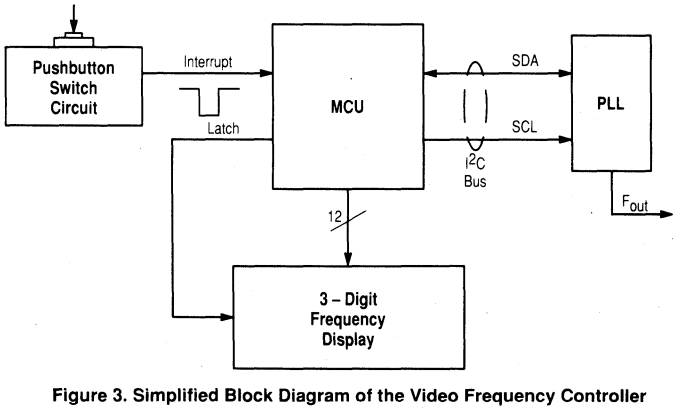

Figure 3. Simplified Block Diagram of the Video Frequency Controller

PLL Tuning Circuit Implementation

The MC44802A works with an MC1648 voltage controlled oscillator (VCO) to form a Phase-Locked Loop (see Figure 4). The MC1648 requires an external parallel tank circuit consisting of an inductor (L) and capacitors (Cv and Cx). Varactor diodes (Cv) are used in this case to provide a voltage variable capacitance for the VCO. The MC1648 may be operated from a +5.0 or –5.2 Vdc supply, depending upon system requirements (+5.0 V in this case). Its maximum frequency is typically 225 MHz.

The VCO output is connected through a capacitor to the phase detector input of the MC44802A. With the feedback network (G(s)) the MC44802A produces a stable voltage input to the tank circuit. A general purpose open collector output buffer (B2, Pin 9) is used in this application to switch a capacitor (Cx) in and out of the tank circuit. When that output buffer is switched low (by writing a "1" to it), the pin diode (D1) conducts making Cx part of the tank circuit (Cx//(Cv/2)). When the output buffer is open D1 does not conduct, thereby presenting a high impedance to Cx, making it ineffective. The tank circuit's capacitance is then Cv/2.

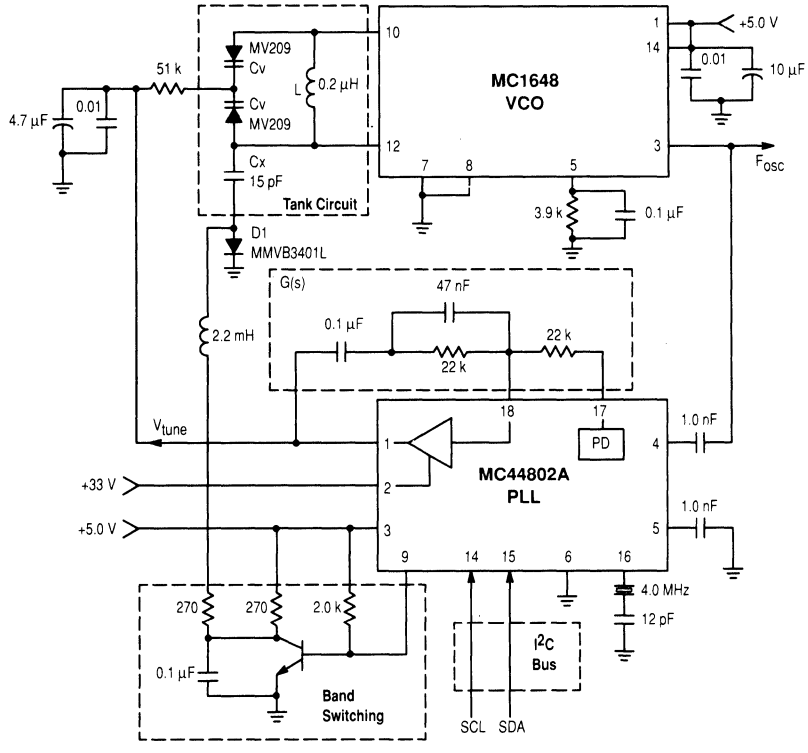

Figure 4. Sample PLL Tuning Circuit

I²C Data

Configuration data is sent by the MCU to the MC44802A I²C Bus Interface in five bytes as shown in Figure 5. Communication of the data is covered in the section describing MCU Implementation.

CA — Chip Address	1	1	0	0	0	0	1	0
CO — Control Info.	1	R6	T	P	R3	R2	R1	R0
BA — Band Info.	B7	B6	B5	B4	X	B2	B1	B0
FM — Frequency Info.	0	N14	N13	N12	N11	N10	N9	N8
FL — Frequency Info.	N7	N6	N5	N4	N3	N2	N1	N0

Figure 5. MC44802A I²C Byte Definitions

Referring to Figure 5:

CA — I^2C chip address for the MC44802A, $C2 (fixed internally).

CO — Sets up the 4.0 MHz oscillator divider ratio (R1, R0), prescaler (P), test outputs (R2, R3) and phase comparator output state (R2, R6, T) according to Figure 6.

BA — Each band buffer (Pins 7–13) can be set to active low by writing a 1 to it.

FM, FL — These two bytes set the tuning frequency. Their relationship with frequency (at Pin 4) depends on whether or not the prescaler is enabled, and the setting of the reference division ratio:

$$N = \frac{F_{out} \times \text{Divider ratio}}{F_{crystal}} \quad \text{(prescaler disabled)}$$

$$\text{or: } N = \frac{F_{out} \times \text{Divider ratio}}{F_{crystal} \times 8} \quad \text{(prescaler enabled)}$$

A hexadecimal representation of N at FM and FL sets the tuning frequency (F_{out}).

Per Figure 5, the address is sent and followed by CO, BA and/or FM, FL. Control and frequency byte pairs are distinguished in the first bit (1 for control, 0 for frequency). Therefore, it is not necessary to always send 5 bytes. A data transfer could consist of CA-CO-BA, or CA-FM-FL. The following example describes the five hex control bytes required to instruct the circuit to tune to VHF Channel 2 (101 MHz):

1) *$C2* (1100 0010) — This is the MC44802A address. The first byte of all MC44802A transmissions must be $C2.
2) *$88* (1000 1000) — R2, R6 and T are set to 000 to indicate normal operation. P=0 enables the internal prescaler. R1, R0=00 sets the divider ratio to 2048 which gives the greatest frequency resolution in the < 512 MHz region. R3 is optionally set high to output a 62.5 kHz test signal at Pin 10 (B4).
3) *$04* (0000 0100) — Sets band buffer B2 (Pin 9) high thereby disabling Cx.
4) and 5) *$19 40* (0001 1001, 0100 0000) — With the given prescaler and divider values, the frequency is defined by $N = F_{out}/15{,}625$ Hz. For 101 MHz:

$$N = \frac{101 \text{ MHz}}{15{,}625 \text{ Hz}} = 6464$$

which is represented in hex by $19 40.

Note that this is not a unique solution to getting 101 MHz out of the circuit since a different combination of prescaler setting, divider ratio and N could be used. Figure 7 shows a table of frequency control bytes (FM, FL) used in this application note. In all cases the internal prescaler is enabled, and the divider ratio is 2048.

MCU Implementation

The Motorola MC68HC11E9 has the required characteristics for generating I^2C transfers. It is equipped with parallel and serial I/O ports, timers, a pulse accumulator, an A/D converter system and expansion capability for multiple MPU systems. Each of these functions must be set-up and activated in user-programmed software to be part of the system. This allows the user to be concerned with only applicable functions. What follows are hardware and software descriptions for the sample MC44802A interface to this MCU. A full listing of the code is included in the Appendix. An HC11 program is written without line numbers. The code shown is the 'program.lst' version created by the assembler which inserts the line numbers and machine code.

R1	R0	Divider Ratio
0	0	2048
0	1	1024
1	0	512
1	1	256

P	Prescaler
0	Enabled
1	Bypassed

R2	R3	Pin 10	Pin 11
0	0	—	—
0	1	62.5 kHz	—
1	0	F (ref)	FBY2
1	1	—	—

R2	R6	T	Phase Comparator Output State
0	0	0	Normal Operation
0	0	1	Off (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	Off (High Impedance)
1	1	0	Normal Operation
1	1	1	Off (High Impedance)

Figure 6. CO Bit Specifications

FM	FL	F_{out} (MHz)	Display	FM	FL	F_{out} (MHz)	Display
$02	$80	10	None	$1A	$C0	107 (ch3)	C03
$06	$40	25	None	$1C	$40	113 (ch4)	C04
$08	$C0	35	None	$1E	$C0	123 (ch5)	C05
$0C	$80	50	None	$20	$40	129 (ch6)	C06
$12	$C0	75	075	$25	$80	150	150
$19	$00	100	090	$2A	$80	170	170
$19	$40	101 (ch2)	C02	$32	$00	200	None

P=0, R0=R1=0

Figure 7. Sample Frequency Control Bytes

Pin Descriptions

Note that only the HC11 pins used in this exercise are shown in Figure 8. Many of the I/O pins can be configured for different functions throughout the execution of a program. This is noted by pins labeled name1/name2. The names in bold indicate the functions used. They will be referred to by their functional name from here forward and are briefly explained below. Refer to the Appendix for code lines.

IC3 — (Input Capture 3) is an edge triggered interrupt pin that can be configured for rising, falling, or both edges. It is configured to respond to rising edges (code lines 70 and 71). All controller output changes are initiated at this pin.

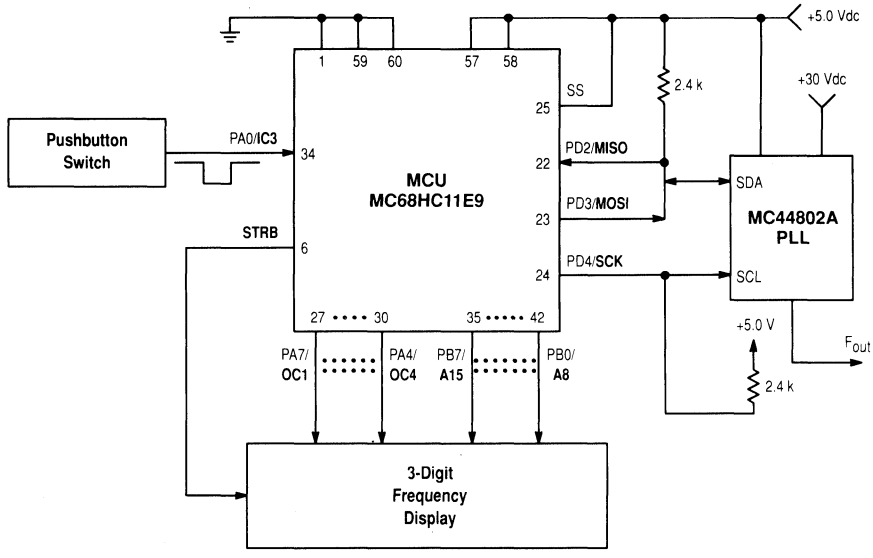

Figure 8. MCU Implementation

SPI (Serial Peripheral Interface) Pins:

MOSI — (Master Out Slave In) is the serial output line used for I^2C data communication with the PLL chip. The controller is configured as the master device in this exercise. This line is referred to as PORT D, bit 3 when the SPI is disabled (the SPI is enabled only during a serial transfer). It is essential that this be configured as an open drain output (an external pullup is used) when programming the SPI Control Register (SPCR, code lines 122–123). This allows the slave device (the PLL) to acknowledge by pulling the data line low.

MISO — (Master In Slave Out) is a serial input line to the controller. Tied to MOSI, it forms a bi-directional data port permitting the MCU to read the acknowledge pulse.

SCK — is the clock line in the I^2C protocol. It is referred to as PORT D, bit 4 when the SPI is disabled.

SS — is a slave select line that must be tied high (inactive) to set the MCU as the master.

Port A Pins:

PA7 — is a general I/O pin. It must be configured as input or output depending on the desired function. It is configured here as an output (code lines 46–48) to drive a bit in the seven segment display (in conjunction with PA6–PA4).

PA6 to PA4 — are fixed direction output pins also used for the seven segment displays.

Port B Pins:

PB7 to PB0 — are fixed direction output pins used for the seven segment displays.

STRB — is an enable line that provides an active low pulse each time new data is written to Port B. This is used to latch data into the display decoders.

Software Description

The software is written in two functional blocks — a main program and an interrupt service routine (ISR). The main program sets up the MCU ports and control registers. It then goes into a low power stopped state until an interrupt is initiated. The interrupt service routine creates the required serial and parallel output signals, and then returns control to the main program which waits for another interrupt.

The interrupt structure provides flexibility for expansion of this system. Other functions can be easily added to the main program without affecting performance of the serial interface. But for this exercise, the main program is kept simple. It sets up memory address references (lines 20–38), parallel Port A (lines 46–48), parallel Port B (line 51) and the interrupt control (lines 66–73). The main program then goes into its low power wait state. It does nothing until control is transferred to the ISR. An ISR flow diagram is included as Figure 10 for clarification.

The following program was written under the assumption that eventually the system will be run as a stand alone. Thus, the serial bytes pertaining to tuning requirements must be stored in the MCU EEPROM. To avoid program modification each time such requirements change, data space has been allocated for this function beginning at location B700. The program requires a specific data format while maintaining application flexibility.

The first requested transfer will output bytes starting at location B700. Transmission continues until a null data byte ($00) is encountered (which is not outputted). The two bytes following contain the display information. Transmissions of this format should follow consecutively as desired with another null after the last display value. The program will then reset the

data pointer to B700. Figure 9 shows the frequency data space for the sample system. It contains bytes for various frequencies from 75 MHz to 170 MHz. Band switching is done between the 90 MHz and 101 MHz (VHF Channel 2) frequency values.

B700> **c2 88 04 12 c0** 00 0f 75 **c2 16 10** 00 0f 90 **c2 88**
B710> **01 19 40** 00 cf 02 **c2 1a c0** 00 cf 03 **c2 1c 40** 00
B720> cf 04 **c2 1e c0** 00 cf 05 **c2 20 40** 00 cf 06 **c2 25**
B730> **80** 00 1f 50 **c2 2a 80** 00 1f 70 **00** ff ff ff ff ff

Figure 9. Sample System Control Data

Note that this example contains two five-byte transmissions and the remainder are three-byte transmissions. Three-byte transmissions are useful as unchanged control, and band information need not be repeated. The displays will cycle through '075', '090', 'C02', 'C03', 'C04', 'C05', 'C06', '150', and '170' which is a mix of frequency (in MHz) and VHF channel displays. The lower four-bits of the first display value (set to f) are ignored since they are unconnected.

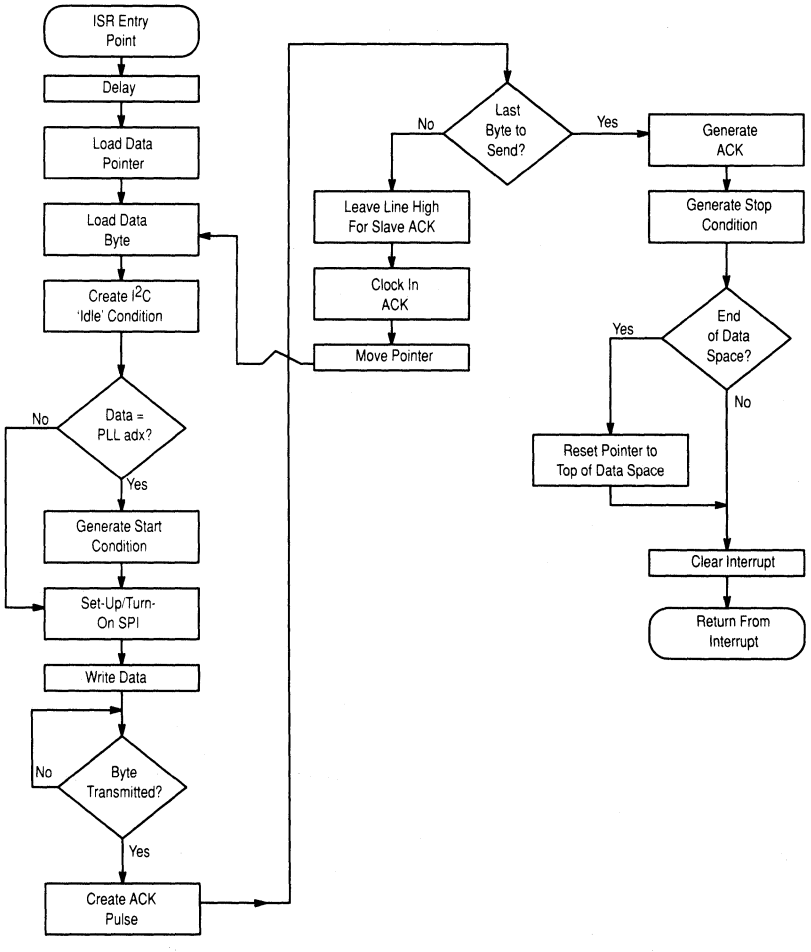

Figure 10. ISR Flow Diagram

Figure 11 is a picture of the first byte of a transmission (the PLL address). Note that the start condition is generated at the scope trigger point and the bit stream 11000010 ($C2) is clocked in on rising edges. After the eighth clock pulse, the data line is released by the MCU and quickly acknowledged (pulled low) by the PLL chip. Refer back to Figure 2.

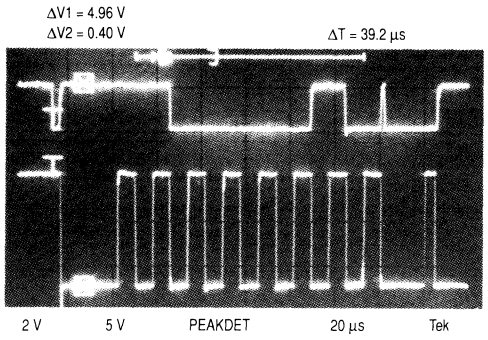

Figure 11. PLL Address Transmission

If the PLL were not responding, the data line would have remained high rather than looking like a spike. This acknowledge is clocked in and the next byte is ready for transmission. Figure 12 illustrates this by showing a full three-byte transmission that updates the PLL tuning frequency.

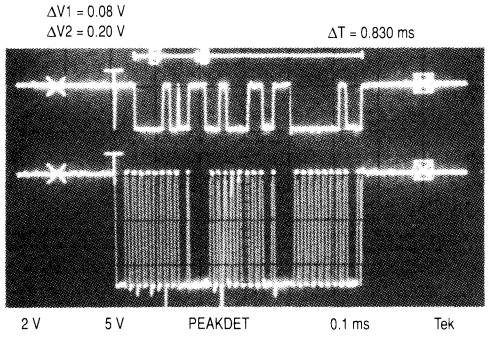

Figure 12. Three Byte Data Transmission

Interrupt Circuitry Implementation

The interrupt circuit (Figure 13) is designed as a simple debounced momentary pushbutton switch. The switch must have a normally open (N/O) and a normally closed (N/C) contact. The output of the circuit is normally at V_{CC} (+5.0 V). When the button is pushed the output goes low. It comes back high when the button is released. The cross-coupled NAND gates eliminate the effect of switch bounce.

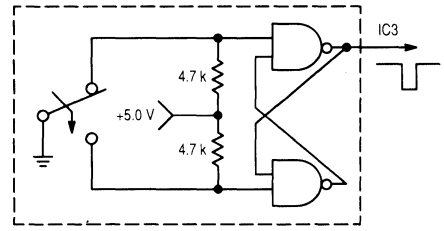

Figure 13. Pushbutton Interrupt Circuit

This will provide a clean low-going pulse to trigger one of the controller's edge-sensitive interrupts (IC3). IC3 is programmed to respond to the rising edge of the pulse to facilitate further debouncing in software.

Frequency/Channel Display Implementation

The display is implemented using three seven-segment (common cathode) LEDs. They are driven by parallel ports (A and B) of the controller in the ISR. These ports send the display information to the hexadecimal-to-seven segment decoders (MC14495-1). The STRB output from the controller is pulsed low each time data is written to Port B and is used to latch the decoders.

Display information is programmed in data space as shown in Figure 9. Outputs are done in the ISR to Port A (lines 147–148) and then to Port B (lines 150–151), and are done in this order because a write to Port B causes the STRB decoder enable pulse. Figure 14 shows the frequency display circuit.

The MC14495-1 is a hexadecimal-to-seven segment Latch/Decoder Driver. It is an improved version of the MC14495 with CMOS input levels and decreased propagation delays. This permits them to be operated directly from the limited duration pulse (STRB) generated by the MCU. The MC14495-1 has internal series output resistors (typically 290 Ω) allowing direct connection to a common cathode LED display.

SUMMARY

This application note should serve as a reference for using an MC44802A for various tuning applications. It is not intended as a replacement for the MC44802A Data Sheet nor the *MC68HC11 Reference Manual*. Its intention is to help bring these tools together to build a working system.

Bibliography

(1) MC44802A Data Sheet
(2) MC1648 Data Sheet
(3) M68HC11E9 Data Sheet
(4) M68HC11EVBU/AD1
(5) MC14495-1 Data Sheet

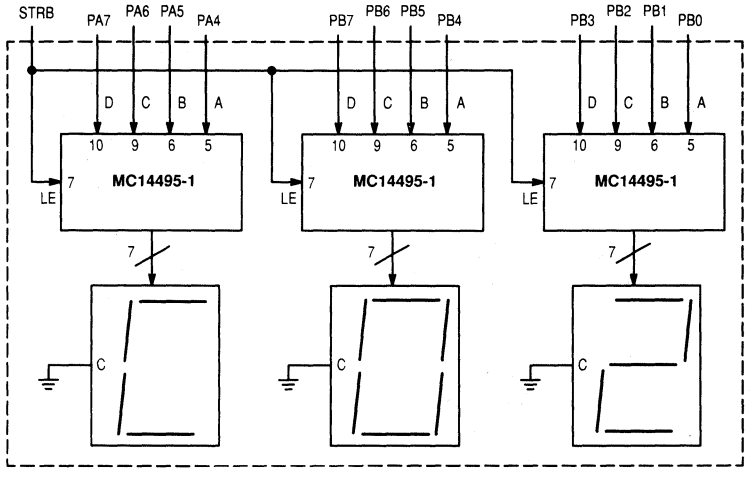

Figure 14. Three Digit Display Circuit

APPENDIX 1 — Microprogramming Basics/ Program Listing

The M68HC11 EVBU (Universal Evaluation Board) provides a friendly environment for developing an HC11 system. Programming is a three step process which includes writing software, assembling it, and downloading it to the MCU.

Writing/Modifying Software

Software should be created as a text file (e.g., program.asm) following the format of HC11 assembly commands. Full description of each command can be found in the *M68HC11 Reference Manual.*

Program Assembly

Once a program has been written, it is run through an assembler. This program will generate the necessary object code and, if desired, a listing file. The object file (xxxx.list) is then downloaded into the HC11:

program.list — listing file,
program.s19 — file to be downloaded.

Downloading/Debugging

Performance of the software and hardware should be evaluated with the help of a personal computer (Macintosh or a PC compatible) and a terminal emulation package such as Freeterm or Kermit. This program allows communication between the EVBU and computer.

APPENDIX 2 — Program Listing

```
0001                    * Motorola SPS — Bipolar Analog IC Division
0002                    * Written by Paul Brownlee
0003
0004                    * This M68HC11 code provides control bytes to operate
0005                    * an MC44802A (Motorola PLL Tuning Circuit) via I2C protocol
0006                    * The bytes are to be determined by the user and placed in
0007                    * memory starting with location B700 (see technical data sheet
0008                    * for control byte information).
0009
0010                    * Communication is achieved using the HC11's Synchronous Serial
0011                    * Peripheral Interface (SPI) to generate both the clock.and data
0012                    * signals. The main program is a short monitor loop. Output is
0013                    * implemented as an interrupt service routine for the edge
0014                    * triggered interrupt IC3. Thus, the location to the routine,
0015                    * B640, must be entered in user RAM as a jump destination for the IC3
0016                    * service routine. The interrupt can then be implemented as a
0017                    * simple debounced switch.
0018
0019                        * REFERENCED TO X-OFFSET ($1000)
0020 0000               PORTA   EQU     $00     PORT A DATA REGISTER
0021 0004               PORTB   EQU     $04     PORT B DATA REGISTER
0022 0002               PIOC    EQU     $02     PARALLEL I/O CONTROL
0023 0026               PACTL   EQU     $26     PULSE ACC CNTRL REG (PORT A)
0024 0008               PORTD   EQU     $08     PORT D DATA REGISTER
0025 0028               SPCR    EQU     $28     SPI CONTROL REGISTER
0026 002a               SPDR    EQU     $2A     SPI DATA REGISTER
0027 0029               SPSR    EQU     $29     SPI STATUS REGISTER
0028 0009               DDRD    EQU     $09     PORT D DATA DIRECTION REGISTER
0029 0022               TMSK1   EQU     $22     REGISTER FOR INPUT CAPTURE ENABLE
0030 0023               TFLG1   EQU     $23     REGISTER FOR INPUT CAPTURE STATUS
0031 0021               TCTL2   EQU     $21     REGISTER FOR INPUT CAPTURE CONTROL
0032                    * REFERENCED TO Y-OFFSET (STARTS AT $B700)
0033 0000               DATA    EQU     $00     DATA SPACE (REL DATA POINTER)
0034 0001               NEXTD   EQU     $01     NEXT DATA BYTE POINTER
0035                    * REFERENCED TO 0000
0036 0000               YSTOR   EQU     $0000   RAM LOC FOR CONTROL DATA
0037 00e2               IC3JMP  EQU     $E2     THE LOCATION FOR IC3 JUMP INST
0038 00e3               IC3JMP1 EQU     $E3     LOC. TO PLACE THE JMP ADX
0039
0040
0041                    ************************** MAIN PROGRAM **************************
0042 b600               ORG $B600
0043 b600 ce 10 00              LDX     #$1000          * BASE FOR CONTROL REGISTERS
0044
0045                    * PORT A SET-UP (FOR HIGH ORDER 7 SEG DISPLAY OUTPUT)
0046 b603 a6 26                 LDAA    PACTL,X         * SET PORTA, BIT 7 TO
0047 b605 8a 80                 ORAA    #$80            * AN OUTPUT PORT
0048 b607 a7 26                 STAA    PACTL,X
0049
0050                    * PORT B SET-UP (FOR 2 LOW ORDER 7 SEG DISPLAY OUTPUTS)
0051 b609 1d 02 ff              BCLR    PIOC,X $FF      * SIMPLE HANDSHAKE MODE
0052
0053                    * TEST OUTPUTS
0054 b60c 86 af                 LDAA    #$AF            * PUT AN 'A' IN THE HIGH
0055 b60e a7 00                 STAA    PORTA,X         * HEX DIGIT
0056 b610 86 bc                 LDAA    #$BC            * AND A 'BC' IN THE LOW
```

```
0057 b612 a7 04                     STAA    PORTB,X         * FOR LED DISPLAYS
0058
0059 b614 18 ce b7 00               LDY     #$B700          * SET MEMORY POINTER
0060 b618 18 df 00                  STY     YSTOR
0061
0062                * INITIALIZE USER STACK POINTER
0063 b61b 8e 00 ff                  LDS     #$FF            * STACK STARTS AT $FF WHICH
0064
0065                * INTERRUPT PREPARATIONS
0066 b61e 86 7e                     LDA     #$7E            * OPCODE FOR JMP INST
0067 b620 97 e2                     STAA    IC3JMP          * LOADED INTO RAM
0068 b622 cc b6 40                  LDD     #$B640          * SET THE JUMP LOCATION FOR
0069 b625 dd e3                     STD     IC3JMP1         * THE INT SERVICE ROUTINE
0070 b627 86 01                     LDAA    #$01            * INPUT CAPTURE (IC3) SET FOR
0071 b629 a7 21                     STAA    TCTL2,X         * RISING EDGE
0072 b62b 1c 22 01                  BSET    TMSK1,X $01     * ENABLE THE IC3
0073 b62e 0e                        CLI                     * ENABLE ALL NON-MASKED
                                                              INTERRUPTS
0074
0075                * MAIN PROGRAM DO NOTHING LOOP
0076 b62f           MONITOR         EQU     *
0077 b62f 01                        NOP                     SIT HERE AND DO NOTHING UNTIL
0078 b630 cf                        STOP                    * SAVE POWER IN STANDBY MODE
0079 b631 20 fc                     BRA     MONITOR         * INTERRUPT
0080
0081
0082
0083                ***************************** INTERRUPT SERVICE ROUTINE *****************************
0084 b640           ORG $B640
0085
0086 b640           START           EQU     *
0087 b640 86 64                     LDAA    #100
0088 b642 18 ce 03 e8 OUTERD        LDY     #1000           * DELAY FOR SOFTWARE
0089 b646 18 09     DELAY           DEY                     * DEBOUNCING OF
0090 b648 26 fc                     BNE     DELAY           * INTERRUPT CIRCUIT
0091 b64a 4a                        DECA
0092 b64b 26 f5                     BNE     OUTERD
0093
0094 b64d 18 de 00                  LDY     YSTOR           * LOAD POINTER
0095 b650 1c 08 10                  BSET    PORTD,X $10     * SET D BIT 4 HIGH (IDLE)
0096
0097                * THE REMAINING LOOP IS EXECUTED AS MANY TIMES AS THERE ARE
0098                * BYTES TO BE OUTPUTTED. IT STARTS AT B700 (OR WHEREVER IT LEFT
0099                * OFF ON PREVIOUS INTERRUPT HANDLED) AND OUTPUTS UNTIL A NULL
0100                * BYTE (00) IS FOUND (00 IS NOT OUTPUTTED). THE NEXT TWO BYTES
0101                * ARE DISPLAYED AND THE POINTER UPDATED.
0102
0103 b653           LOOP            EQU     *
0104 b653 18 e6 00                  LDAB    DATA,Y          * LOAD THE PRESENT BYTE
0105 b656 1d 28 40                  BCLR    SPCR,X $40      * DISABLE SPI
0106 b659 1c 08 08                  BSET    PORTD,X $08     * SET D BIT 3 HIGH (IDLE)
0107 b65c 86 38                     LDAA    #$38            * SS=1, SCK=MOSI=1
0108 b65e a7 09                     STAA    DDRD,X
0109 b660 c1 c2                     CMPB    #$C2            * CHECK DATA TO SEE IF A
0110 b662 26 03                     BNE     NOSTART         * START CONDITION IS REQ
0111                * (IF FIRST DATA BYTE)
0112
```

```
0113                        * This segment transfers a byte from the HC11's SPI
0114                        * to the I2C peripheral. Upon Entry, data is in Acc B.
0115                        * w_start is the entry point for sending a start bit.
0116                        * nostart is the entry point for transferring data
0117                        * without a start condition.
0118
0119 b664                   W_START             EQU         *
0120 b664 1d 08 08                      BCLR    PORTD,X $08 * START CONDITION
0121 b667                   NOSTART     EQU         *
0122 b667 86 73                         LDAA    #$73        * ENABLE SPI (SPE=1); MASTER
0123 b669 a7 28                         STAA    SPCR,X      * CPOL=CPHA=0; BITRATE=CLK/32
0124 b66b 1c 08 08                      BSET    PORTD,X $08 * RETURN PD3 TO IDLE STATE
0125 b66e e7 2a                         STAB    SPDR,X      * WRITE DATA
0126 b670 a6 29             WAIT        LDAA    SPSR,X      * WAIT FOR END OF XMISSION
0127 b672 2a fc                         BPL     WAIT        * IF NOT, WAIT
0128                                                        *
0129 b674 1d 08 10                      BCLR    PORTD,X $10 * LEAVE SCLK (PD4) LOW
0130 b677 a6 28                         LDAA    SPCR,X      * CREATE ACK PULSE
0131 b679 84 bf                         ANDA    #$BF        * CLEAR SPE, DISABLE SPI
0132 b67b a7 28                         STAA    SPCR,X      * CAUSES PD4 (SDA) TO GO HIGH
0133
0134 b67d 18 6d 01                      TST     NEXTD,Y     * TEST NEXT BYTE, IF <> 0
0135 b680 26 3a                         BNE     HI_ACK      * SLAVE GENRTS ACK (LOW)
0136
0137 b682 1d 08 08          LO_ACK      BCLR    PORTD,X $08 * ELSE, CLEAR ACK BIT
0138 b685 1c 08 10                      BSET    PORTD,X $10 * GEN ACK CLOCK
0139 b688 21 f8                         BRN     LO_ACK      * INSURE PULSE WIDTH
0140 b68a 1d 08 10                      BCLR    PORTD,X $10 * CLOCK LOW
0141 b68d 1c 08 10                      BSET    PORTD,X $10 * GEN STOP
0142 b690 1c 08 08                      BSET    PORTD,X $08 * CONDITION
0143
0144 b693 18 08                         INY
0145 b695 18 08                         INY                 * PNT TO FREQ VALU
0146 b697 1d 02 ff                      BCLR    PIOC,X $ff  * SIMPLE HANDSHAKE MODE
0147 b69a 18 a6 00                      LDAA    DATA,Y      * LOAD MSB OF FREQ VAL
0148 b69d a7 00                         STAA    PORTA,X     * AND OUTPUT IT
0149 b69f 18 08                         INY                 * MOVE POINTER
0150 b6a1 18 a6 00                      LDAA    DATA,Y      * LOAD 2 LS DIGITS
0151 b6a4 a7 04                         STAA    PORTB,X     * AND OUTPUT THOSE
0152
0153 b6a6 18 08                         INY                 * POINT TO NEXT GROUP
0154 b6a8 18 df 00                      STY     YSTOR       * SAVE NEW POINTER
0155 b6ab 18 6d 00                      TST     DATA,Y      * CHECK FOR LAST GROUP
0156 b6ae 26 07                         BNE     MODATA      * IF NOT, KEEP YSTOR
0157 b6b0 18 ce b7 00       SETPTR      LDY     #$B700      * ELSE RESET POINTER
0158 b6b4 18 df 00                      STY     YSTOR       * TO TOP OF DATA
0159
0160 b6b7 86 01             MODATA      LDAA    #$01
0161 b6b9 a7 23                         STAA    TFLG1,X     * CLEAR INTERRUPT
0162 b6bb 3b                            RTI                 * STOP SERVICE OF OUTPUT
0163
0164
0165
0166 b6bc 1c 08 10          HI_ACK      BSET    PORTD,X $10 * GENERATE ACK CLOCK
0167 b6bf a6 08                         LDAA    PORTD,X     * CHECK FOR SLAVE ACK
0168 b6c1 84 04                         ANDA    #$04        * BEING A LOW BIT 3
0169 b6c3 26 09                         BNE     ERROR       * IF NOT, BRANCH TO ERROR
0170 b6c5 21 f5                         BRN     HI_ACK      * ENSURE CLK PULSE WIDTH
```

APPENDIX 2 — Program Listing (continued)

```
0171 b6c7 1d 08 10                BCLR    PORTD,X $10     * BCLR 4, PORTD
0172 b6ca 18 08                   INY                     * POINT TO NEXT DATA BYTE
0173 b6cc 20 85                   BRA     LOOP
0174
0175 b6ce 86 ee          ERROR    LDAA    #$EE            * PRINT OUT AN 'EEE'
0176 b6d0 a7 00                   STAA    PORTA,X         * TO INDICATE THAT THE
0177 b6d2 a7 04                   STAA    PORTB,C         * SLAVE DIDN'T ACK
0178 b6d4 7e b6 b0                JMP     SETPTR          * END XMISSION ATTEMPT
0179
0180
```

The MC145170 in Basic HF and VHF Oscillators

Prepared by: David Babin and Mark Clark

Phase-locked loop (PLL) frequency synthesizers are commonly found in communication gear today. The carrier oscillator in a transmitter and local oscillator (LO) in a receiver are where PLL frequency synthesizers are utilized. In some cellular phones, a synthesizer can also be used to generate 90 MHz for an offset loop. In addition, synthesizers can be used in computers and other digital systems to create different clocks which are synchronized to a master clock.

The MC145170 is available to address some of these applications. The frequency capability of the MC145170 is very broad — from a few hertz to 160 MHz.

ADVANTAGES

Frequency synthesizers, such as the MC145170, use digital dividers which can be placed under MCU control. Usually, all that is required to change frequencies is to change the divide ratio of the N Counter. Tuning in less than a millisecond is achievable.

The MC145170 can generate many frequencies based on the accuracy of a single reference source. For example, the reference can be a low-cost basic crystal oscillator or a temperature-compensated crystal oscillator (TCXO). Therefore, high tuning accuracies can be achieved. Boosting of the reference frequency by 100x or more is achievable.

ELEMENTS IN THE LOOP

The components used in the PLL frequency synthesizer of Figure 1 are the MC145170 PLL chip, low-pass filter, and voltage-controlled oscillator (VCO). Sometimes a voltage-controlled multivibrator (VCM) is used in place of the VCO. The output of a VCM is a square wave and is usually integrated before being fed to other sections of the radio. The VCM output can be directly used in computers and other digital equipment. The output of a VCO or VCM is typically buffered, as shown.

As shown in Figure 2, the MC145170 contains a reference oscillator, reference counter (R Counter), VCO/VCM counter (N Counter), and phase detector. A more detailed block diagram is shown in the data sheet.

HF SYNTHESIZER

The basic information required for designing a stable high-frequency PLL frequency synthesizer is the frequencies required, tuning resolution, lock time, and overshoot. For the example design of Figure 3, the frequencies needed are 9.20 MHz to 12.19 MHz. The resolution (usually the same as the frequency steps or channel spacing) is 230 kHz. The lock time is 8 ms and a maximum overshoot of approximately 15% is targeted. For purposes of this example, lock is considered to be when the frequency is within about 1% of the final value.

HF SYNTHESIZER LOW-PASS FILTER

In this design, assume a square wave output is acceptable. To generate a square wave, a MC1658 VCM chip is chosen. Per the transfer characteristic given in the data sheet, the MC1658 transfer function, K_{VCM}, is approximately 1 x 10^8 radians/second/volt. The loading presented by the MC1658 control input is large; the maximum input current is 350 µA. Therefore, an active low-pass filter is used so that loading does not affect the filter's response. See Figure 3. In the filter, a 2N7002 FET is chosen because it has very high transconductance (80 mmhos) and low input leakage (100 nA).

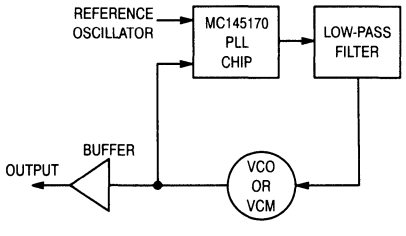

Figure 1. PLL Frequency Synthesizer

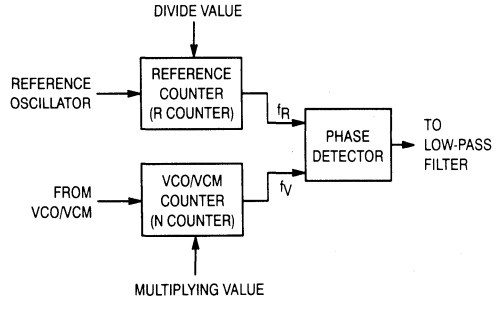

Figure 2. Detail of the MC145170

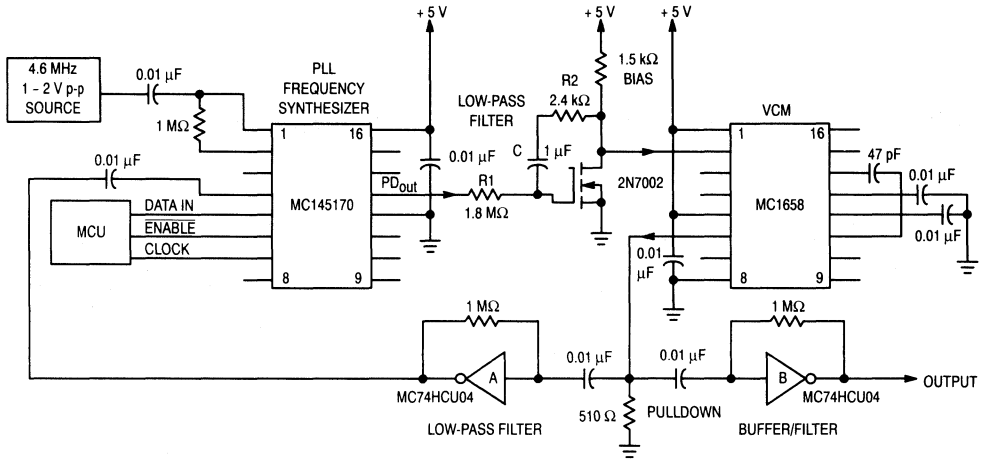

Figure 3. HF Synthesizer

In order to calculate the average divide value for the N Counter, follow this procedure. First, determine the average frequency; this is (12.19 + 9.2)/2 = 10.695 MHz or approximately 10.7 MHz. Next, divide this frequency by the resolution: 10.7 MHz/230 kHz = about 47.

Next, reference application note AN535 (see book DL130/D Rev 1). The active filter chosen takes the form shown in Figure 9 of the application note. This filter is used with the single-ended phase detector output of the MC145170, PD_{out}. The phase detector associated with PD_{out} has a gain $K_\phi = V_{DD}/4\pi$. For a supply of 5 V, this is $5/4\pi = 0.398$ V/rad. The system's step response is shown in Figure 4. To achieve about 15% overshoot, a damping factor of 0.8 is used. This causes frequency to settle to within 1% at $\omega_n t = 5.5$.

The information up to this point is as follows.

f_{ref} = 230 kHz

f_{VCM} = 9.2 to 12.19 MHz; the average is 10.7 MHz, average N = 47

power supply = 5 V for the phase detector

$K_{VCM} = 1 \times 10^8$ rad/s/V

overshoot = approximately 15%, yields a damping factor = 0.8

lock time t = 8 ms settling to within 1%, $\omega_n t = 5.5$

K_ϕ or K_p = 0.398 V/rad.

From the application note, equation 61, $\omega_n = 5.5/t = 5.5/0.008 = 687.5$ rad/s.

Equation 59 is $R1C = (K_p K_V)/\omega_n^2 N$

$= (0.398 \times 1 \times 10^8)/687.5^2 \times 47$

$= 1.79$

Equation 59 is used because of the high-gain FET.

Next, the capacitor C is picked to be 1 µF. Therefore, R1 = 1.79/C which is 1.79 MΩ. The standard value of 1.8 MΩ is used for R1.

Equation 63 is $R2 = (2\zeta)/C\,\omega_n$

$= (2 \times 0.8)/(1 \times 10^{-6} \times 687.5)$

$= 2.33$ kΩ.

A standard value for R2 of 2.4 kΩ is utilized.

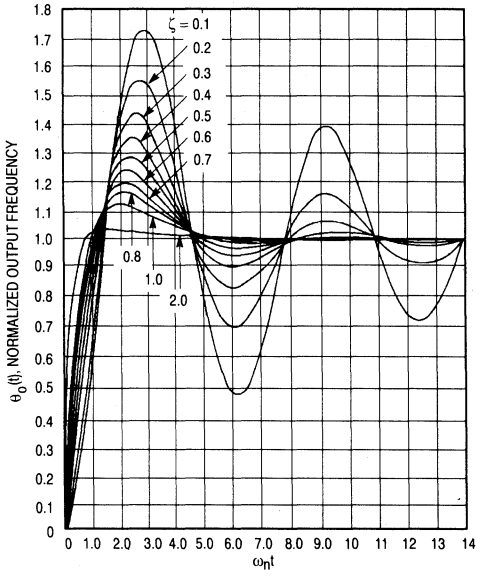

Figure 4. Type 2 Second Order Step Response

HF SYNTHESIZER PROGRAMMING

Programming the MC145170 is straightforward. The three registers may be programmed in a byte-oriented fashion. The registers retain their values as long as power is applied. Thus, usually both the C and R Registers are programmed just once, right after power up.

The C Register, which configures the device, is programmed with $C0 (1 byte). This sets the phase detector to the proper polarity and activates PD_{out}. This also turns off the unused outputs. The phase detector polarity is determined by the filter and the VCM. For this example, the MC1658 data sheet shows that a higher voltage level is needed if speed is to be increased. However, the low-pass filter inverts the signal from the phase detector (due to the active element configuration). Therefore, the programming of the polarity for the phase detector means that the POL bit must be a "1."

The R Register is programmed for a divide value that results in the proper frequency at the phase detector reference input. In this case, 230 kHz is needed. Therefore, with the 4.6 MHz source shown in Figure 3, the R Register needs a value of $000014 (3 bytes, 20 in decimal).

The N Register determines the frequency tuned. Tuning 9.2 MHz requires the proper value for N to multiply up the reference of 230 kHz to 9.2 MHz. This is 40 decimal. For 12.19 MHz, the value is 53 decimal. To tune over the range, change the value in the N Register within the range of 40 to 53 with a 2-byte transfer. Table 1 shows the possible frequencies.

Table 1. The HF Oscillator Frequencies

N Value	Frequency, MHz
40	9.20
41	9.43
42	9.66
43	9.89
44	10.12
45	10.35
46	10.58
47	10.81
48	11.04
49	11.27
50	11.50
51	11.73
52	11.96
53	12.19

EXTRA FILTERING FOR THE HF LOOP

When the HF oscillator was built, the proper frequencies could not be tuned. The output of the MC1658 was examined with an oscilloscope and the switching edges were discovered to be "ragged." That is, the output did not appear to be a square wave with clean transitions.

The f_{in} input of the MC145170 is sensitive to 500 mV p-p signals, and the ragged edges were being amplified and counted down by the N Counter. Therefore, the edges needed cleaning up. One method would have been to add a low-pass filter between the MC1658 and MC145170. However, because an additional buffer was needed elsewhere in the circuit, an MC74HCU04 inverter was used in place of the filter. This inverter's frequency response is low enough to clean up the ragged edges. That is, filtering of the ragged edges occurred, and the output had smoother transitions. As mentioned previously, one of the elements in the inverter package was used to buffer the output of the VCM before feeding it to the outside world. See Figure 3.

VHF SYNTHESIZER

The MC145170 may be used in VHF designs, also. The range for this next example is 140 to 160 MHz in 100 kHz increments.

VHF SYNTHESIZER LOW-PASS FILTER

To illustrate design with the doubled-ended phase detector, the ϕ_R and ϕ_V outputs are used. This requires an operational amplifier, as shown in Figure 5. From the design guidelines shown in the MC145170 data sheet, the following equations are used:

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{N\,C\,R_1}} \quad (1)$$

$$\text{damping factor} \quad \zeta = \frac{\omega_n R_2 C}{2} \quad (2)$$

where, from the data sheet, the equation for the ϕ_R and ϕ_V phase detector,

$$K_\phi = \frac{V_{DD}}{2\pi} = \frac{5}{2\pi} = 0.796 \text{ V/rad} \quad (3)$$

$$\zeta = 0.707,$$

$$\omega_n = \frac{2\pi f_R}{50} = \frac{2\pi \times 100 \text{ kHz}}{50} = 12{,}566 \text{ rad/s} \quad (4)$$

and

$$K_{VCO} = \frac{2\pi\,\Delta\, f_{VCO}}{\Delta\, V_{VCO}} = \frac{2\pi \times (160 - 140 \text{ MHz})}{10 - 2}$$

$$= 1.57 \times 10^7 \text{ rad/s/V} \quad (5)$$

The control voltage range on the input to the VCO is picked to be 2 to 10 V.

The average frequency = (140 + 160)/2 = 150 MHz. Therefore, the average N = 1500.

The above choices for ζ and ω_n are rules of thumb that are a good design starting point. A larger ω_n value results in faster loop lock times and higher reference frequency VCO sidebands for similar sideband filtering. (See Advanced Considerations.)

Choosing C_1 to be 4700 pF, R_1 is calculated from the rearranged expression for ω_n as:

$$R_1 = \frac{K_\phi K_{VCO}}{C_1 \omega_n^2 N} = \frac{(0.796 \text{ V/rad})(1.57 \times 10^7 \text{ rad/s/V})}{(4700 \text{ pF})(12{,}566 \text{ rad/s})^2\,(1500)}$$

$$= 11.23 \text{ k}\Omega \quad (6)$$

Therefore, chose an 11 kΩ standard value resistor.

R_2 is determined from:

$$R_2 = \frac{2\zeta}{\omega_n C_1} = \frac{(2)(0.707)}{(12{,}566)(4700 \text{ pF})}$$

$$= 23.94 \text{ k}\Omega \text{ or}$$
$$2.4 \text{ k}\Omega \text{ (standard value)} \quad (7)$$

VHF SYNTHESIZER EXTRA FILTERING

For more demanding applications, extra filtering is sometimes added. This reduces the VCO sidebands caused by a small amount of the reference frequency feeding through the filter. One form of this filtering consists of spitting R1 into two resistors; each resistor is one-half the value of R1, as indicated by R1/2 in Figure 5. Capacitors C_C are added from the

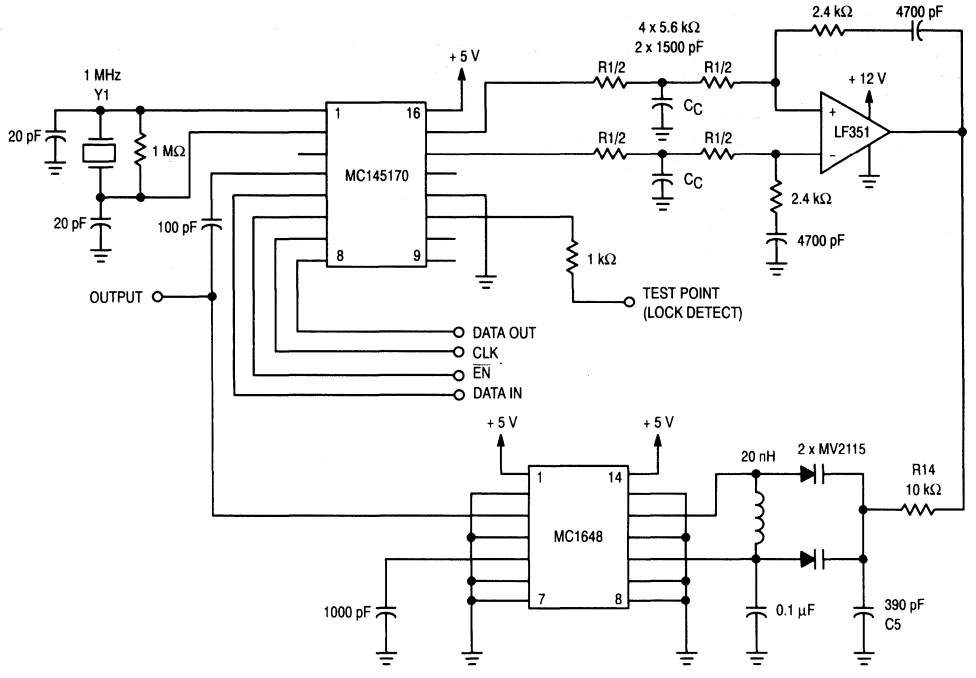

Figure 5. VHF Synthesizer

midpoints to ground to further filter the reference sidebands. The value of C_C is chosen so that the corner frequency of this added network does not significantly affect the original loop bandwidth ω_B.

The rule of thumb for an initial value is $C_C = 4 / (R1\ \omega_{RC})$, where ω_{RC} is the filter cutoff frequency. A good value is to choose ω_{RC} to be 10 x ω_B, so as to not significantly impact the original filter.

$$\omega_B = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}} \quad (8)$$

$$= 12{,}566\sqrt{1+(2)(0.707)^2+ \sqrt{2+(4)(0.707)^2+ (4)(0.707)^4}}$$

$$= 25{,}760 \text{ rad/s}$$

$$\omega_{RC} = 10\ \omega_B = (10)(25{,}760) = 257{,}600 \text{ rad/s} \quad (9)$$

$$C_C = \frac{4}{R1\omega_{RC}} = \frac{4}{(11.23\ k\Omega)(257{,}600 \text{ rad/s})} \quad (10)$$

$$= 1383 \text{ pF} \approx 1500 \text{ pF}$$

There is also a filter formed at the input to the VCO. Again, this should be selected to ensure that it does not significantly affect the loop bandwidth. For this example, the filter is dominated by R14 with C5. The capacitance of the varactors (in series with the rest of the circuit) is much smaller than C5 and can therefore be neglected for this calculation.

As above, let $\omega_{RC} = 257{,}600$ rad/s be the cutoff of this filter. R1 was previously chosen to be 10 kΩ. Therefore,

$$C_5 = \frac{1}{\omega_{RC} R_{14}} = \frac{1}{(257{,}600)(10\ k\Omega)} \quad (11)$$

$$= 388 \text{ pF} \approx 390 \text{ pF}$$

THE VARACTOR

The MV2115 was selected for its tuning ratio of 2.6 to 1. The capacitance can be changed from 49.1 pF to 127.7 pF over a reverse bias swing of 2 to 30 volts. Contact your Motorola representative for information regarding the MV2115 varactor diode.

For example, three parameters are considered.

C_T = Nominal capacitance
CR = Capacitance ratio
fR = Frequency ratio

$$CR = \frac{C_V min}{C_V max} = \left(\frac{V_{max}}{V_{min}}\right)^{\rho} \quad (12)$$

where ρ = the capacitance exponent

Therefore,

$$CR = 2.6\left(\frac{30}{2}\right)^{\rho} \quad (13)$$

$$\log(2.6) = \rho\log(15) \quad (14)$$

$$\rho = \log(2.6)/\log(15) = 0.3528 \quad (15)$$

Using the nominal capacitance of 100 pF at 4 volts:

$$\frac{100\text{ pF}}{C_V\text{max}} = \left(\frac{10}{4\text{ V}}\right)^{0.3528} \quad (16)$$

$$\frac{100\text{ pF}}{C_V\text{max}} = 1.382$$

Solving for $C_V$max:

$$\frac{100\text{ pF}}{1.382} = 72.4\text{ pF}$$

Solving for $C_V$min:

$$2.6 = \frac{C_V\text{min}}{49.1\text{ pF}} \quad (17)$$

$$C_V\text{min} = (2.6)(49.1\text{ pF})$$

$$C_V\text{min} = 127.7\text{ pF}$$

THE VCO

For convenience, the MC1648 VCO is selected. The tuning range of the VCO may be calculated as

$$\frac{f_{max}}{f_{min}} = \frac{(C_d\text{max} + C_S)^{0.5}}{(C_d\text{min} + C_S)^{0.5}} \quad (18)$$

where

$$f_{min} = \frac{1}{2\pi[L(C_d\text{max} + C_S)]^{0.5}} \quad (19)$$

As shown in Figure 8 of the data sheet, the VCO tank circuit is comprised of two varactors and an inductor. Typically, a single varactor might be used in either a series or parallel configuration. However, the second varactor has a two-fold purpose. First, if the 10 kΩ isolating impedance is left in place, the varactors add in series for a smaller capacitance. Second, the added varactor acts to eliminate distortion due to the tank voltage changing.

Therefore, with the two varactors in series, $C_d$max′ = $C_d$max/2. The shunt capacitance (input plus external capacitance) is symbolized by C_S.

Therefore, solving for the inductance:

$$L = \frac{1}{(2\pi f_{min})^2(C_d\text{max}' + C_S)} = 19.9\text{ nH} \approx 20\text{ nH} \quad (20)$$

The Q of the inductor should be more than 100 for best performance.

$$f_{min} = \frac{1}{2\pi[(19.9\text{ nH})(69.85\text{ pF})]^{0.5}} = 135\text{ MHz} \quad (21)$$

$$f_{max} = \frac{1}{2\pi[(19.9\text{ nH})(42.2\text{ pF})]^{0.5}} = 173\text{ MHz} \quad (22)$$

The frequency ratio is 1.5 to 1 and is impacted by the tuning range of the MV2115 varactor diode used in the tank circuit. Therefore, the required range of 140 to 160 MHz is not limited by this VCO design.

A pc board should be used to obtain favorable results with this VHF circuit. The lead lengths in the tank circuit should be kept short to minimize parasitic inductance. The length of the trace from the VCO output to the PLL input should be kept as short as possible. In addition, use of surface-mount components is recommended to help minimize strays.

VHF SYNTHESIZER PROGRAMMING

Again, programming the three registers of the MC145170 is straightforward. Also, usually both the C and the R Registers are programmed only once, after power up.

The C Register configures the device and is programmed with $00 (1 byte). This sets the phase detector to the correct polarity and activates the ϕ_R and ϕ_V outputs while turning off the other outputs. Like the HF oscillator, the phase detector polarity is determined by how the filter is hooked up and the VCO.

The R Register is programmed for a divide value that delivers the proper frequency at the phase detector reference input. In this case, 100 kHz is needed. Therefore, with the 1 MHz crystal shown, the R Register needs a value of $00000A (3 bytes, 10 in decimal).

The N Register determines the frequency tuned. To tune 140 MHz, the value required for N to multiply up the reference of 100 kHz to 140 MHz is 1400 decimal. For 160 MHz, the value is 1600 decimal. To tune over the range, simply change the value in the N Register with a 2-byte transfer.

ADVANCED CONSIDERATIONS

The circuit of Figure 5 may not function at very-high temperature. The reason is that the MC145170 is guaranteed to a maximum frequency of 160 MHz at 85°C. Therefore, there is no margin for overshoot (reference Figure 4) at high temperature. There are two possible solutions: (1) maintain the ambient temperature at less than 60°C, or (2) limit the tuning to less than 160 MHz.

Operational amplifiers are usually too noisy for critical applications. Therefore, if an active element is required in the integrator, one or more discrete transistors are utilized. These may be FETs or bipolar devices. However, active filter elements are not needed if the VCO loading is not severe, such as is encountered with most discrete VCO designs. Because active elements add noise, some performance parameters are improved if they are not used. On the other hand, an active filter can be used to scale up the VCO control voltage. For example, to tune a wide range, the control voltage may have to range up to 10 V. For a 5 V PLL output, this would be scaled by 2x via use of active elements.

Some applications have requirements that must be met in the areas of phase noise and reference suppression. These parameters are in conflict with fast lock times. That is, as lock times are reduced, reference suppression becomes more difficult. Both reference suppression and phase noise are advanced areas that are covered in several publications. As an example, consider that the VCO input voltage range for the above VHF loop was merely picked to be 8 V. Advanced

techniques demand a trade off between this voltage range and the spectral purity of the VCO output. This is because the lower the control voltage range, the more sensitive the VCO is to noise coming into its control input.

A VCO IC may not offer enough performance for some applications. Therefore, the VCO may have to be designed from discrete components.

Figure 6 shows the performance of the VHF Oscillator prototype on a spectrum analyzer. Note that the reference sidebands appear at 100 kHz as expected, and are 50 dB down.

REFERENCES

CMOS Application-Specific Standard ICs, book DL130/D, Motorola, 1990, MC145170 data sheet and AN535 application note.

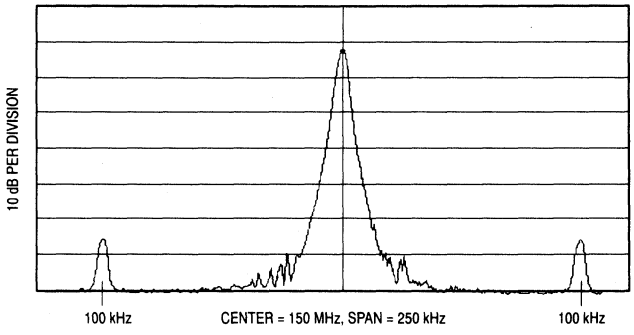

Figure 6. VHF Oscillator Performance

AN1306

Thermal Distortion In Video Amplifiers

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ABSTRACT

Thermal distortion is a problem in many high resolution video amplifiers. Thermal distortion occurs when there are instantaneous power changes in the transistor stages. If the problem goes uncompensated, it leads to a visual effect known as smearing. This Application Note will discuss what smearing is, what causes thermal distortion, how to measure it and how to compensate the problem.

WHAT IS SMEARING?

Smearing is best explained by using an example. Smearing, or ghosting, is most noticeable when a black block is displayed on an all white background. Referring to Figure 1, both Sections a. and b. should be the same brightness. When there is a smearing problem, Section b. will be brighter than Section a. This problem is related to the droop of the video signal, and can be explained using Figure 2. Notice after the transition from black to white (from high voltage to low voltage), the video signal is below the specified white level. This signal shows up on the display as a section "brighter" than white. The signal does eventually settle to the white level; but until it does, the display will appear brighter than it should be.

WHAT CAUSES THERMAL DISTORTION?

The transistors of a video amplifier are often subject to large instantaneous power changes because of the large voltage swings, particularly on transitions from black to white. These power changes cause changes in the transistor's junction temperature. Due to the transistor's thermal time constant, which is the amount of time it takes something to heat up or cool down, the transistor can't change temperature fast enough. It is this thermal time constant and the fact that V_{BE} of a transistor changes with temperature, – 2 mV/°C, that causes thermal distortion.

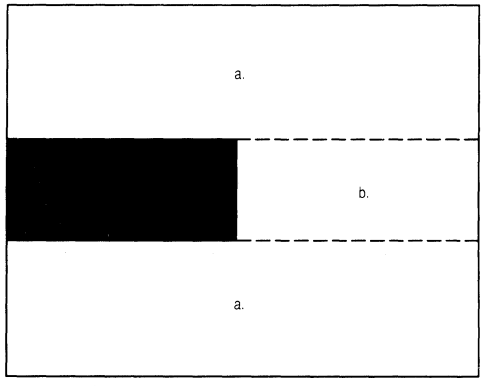

Figure 1.

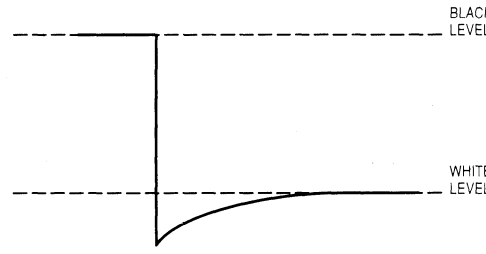

Figure 2.

Figure 3 shows a simple example that can be used to explain the thermal distortion concept. In the ideal case, where V_{BE} does not change with temperature, there is a power swing of 107 mW across the transistor. Using the 107 mW and a thermal resistance of 30°C/W, we can see how this power swing affects the output in the real case. (A change in power of 107 mW would create about the normal junction temperature T_E a change of ±1.6°C.) Notice on the plot of T_J, that the junction temperature does not change instantaneously. This is a result of the thermal time constant. Using −2 mV/°C, we can calculate V_{BE}; from there we can calculate V_E, I_E, and V_O. This example clearly shows the distortion of the square wave.

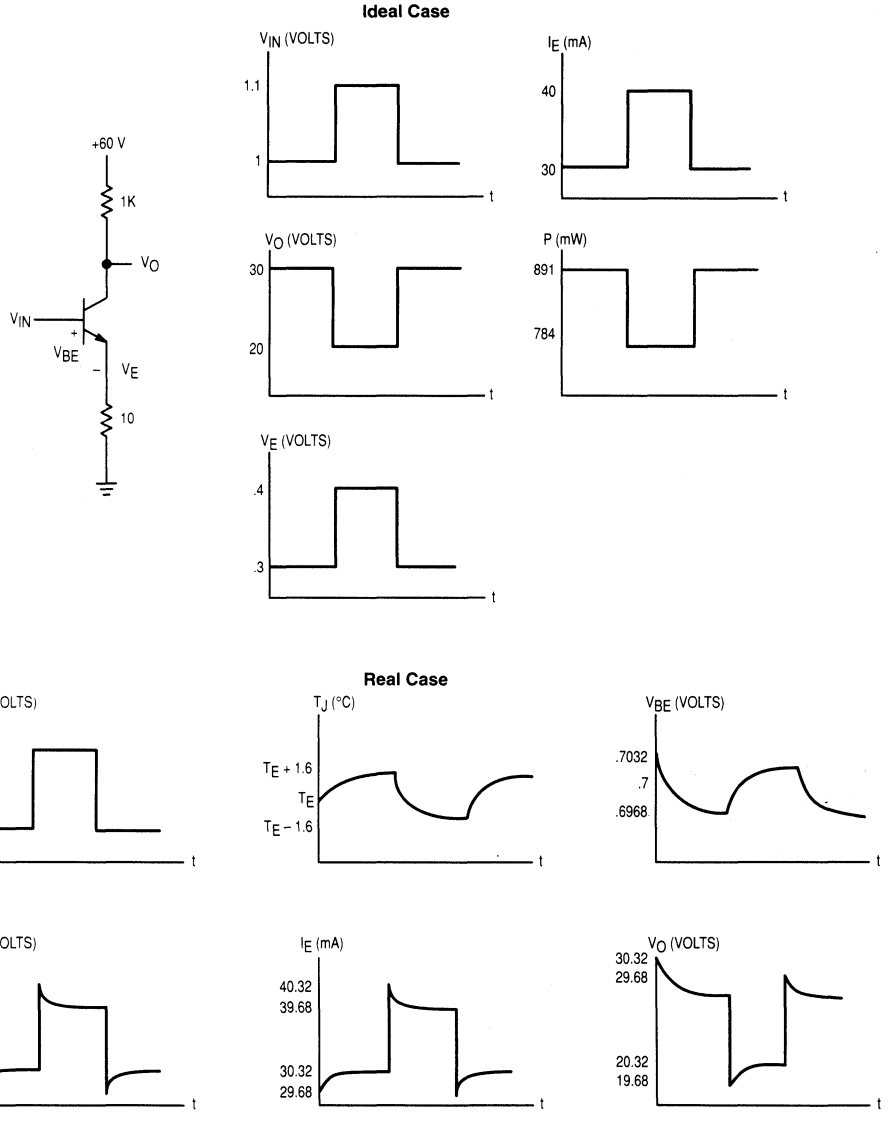

Figure 3.

MEASURING THE DISTORTION

Making an accurate measurement of the distortion can be difficult. The oscilloscope must have enough vertical offset to enable the edge to be viewed with a reasonable scale. Often, flatness measurements in the 100 mV to 200 mV range must be measured on a 1 Volt/div scale. In this case, the accuracy is not good. Another issue that must be considered is scope performance at maximum offsets. When a scope is operating at a maximum offset, it may introduce some of its own distortion. Check with the manufacturer.

HOW TO COMPENSATE THE PROBLEM

There is no real standard on how small the distortion must be. Several years ago a 1% flatness was acceptable (400 mV for a 40 V swing). On today's high resolution displays, this is clearly unacceptable. A flatness of 200 mV for a 40 V swing will cause noticeable smearing problems. Some designers believe a 50 mV flatness is required, but anything less than 100 mV is generally acceptable. Flatness of 50 mV – 100 mV for a 40 V swing is very difficult to measure.

The effect of thermal distortion can be compensated. The Motorola CR2424 is used as an example to show some of the compensation techniques that can be utilized. The output waveform, when there is a distortion problem, appears as a signal with excessive mid and high frequency gain. The signal would be flat if this excessive gain were eliminated. One way of doing this is to use a series RC network as feedback from the output to the input. The CR2424 has an internal compensation network which noticeably improves the flatness. Unfortunately, this is only a first order compensation network and doesn't eliminate all problems. The flatness can be further improved by adding an external compensation network consisting of a 150 pF capacitor and a 200 kΩ resistor. Figure 4 shows the flatness of the CR2424 without the internal compensation network while Figure 5 shows the flatness with the internal network. Note the considerable improvement in the flatness of the output waveform when the complete CR2424, including its internal compensation network, is used.

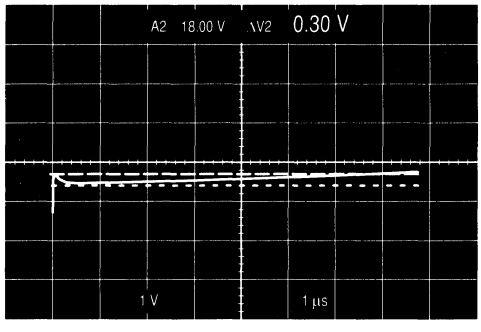

Figure 4. CR2424 Without Compensation

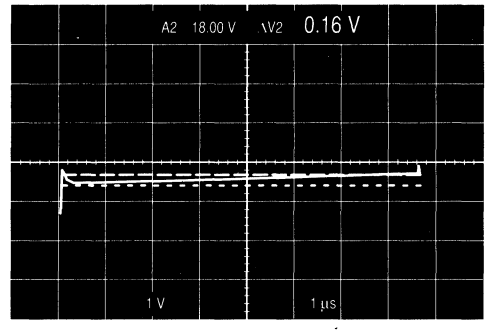

Figure 5. CR2424 With Internal Compensation

Figure 6 shows the effect of an external compensation network. The improvement may seem small, but it can be seen on the CRT. Additional external compensation networks may be added to further improve the flatness. In oscilloscopes, where flatness is very important, as many as ten networks are used.

There is another flatness issue. The first 0.5 µs of the pulse is not flat. This can be seen in Figures 5 and 6. On the display, this problem shows up as a gray area right after the transition from black to white. This is a frequency response issue and can be corrected by adding an additional input peaking network. Figure 7 shows the circuit and a photo of the actual waveform.

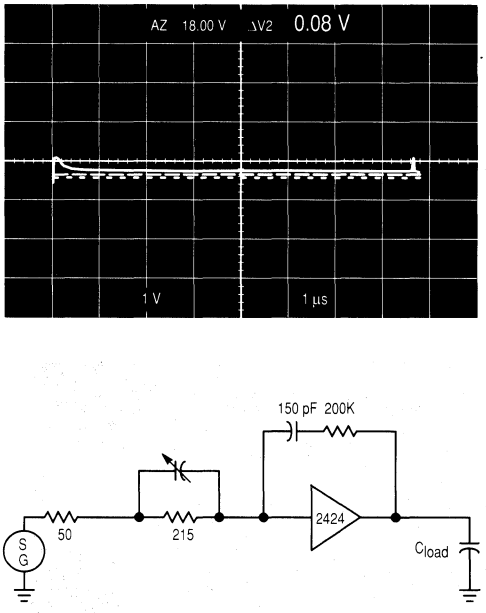

Figure 6. CR2424 With External Compensation

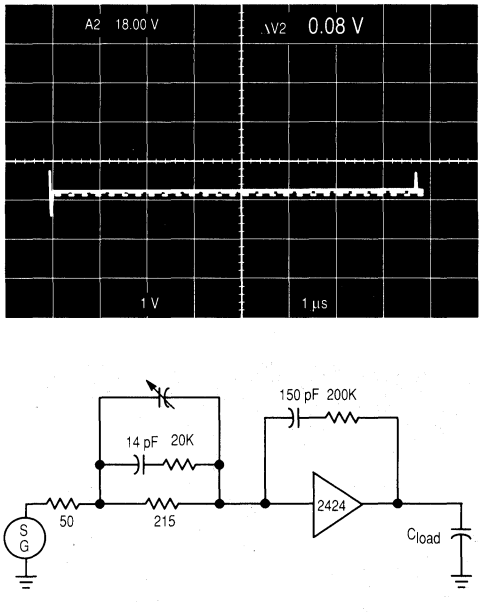

Figure 7. CR2424 With Modified Input Network

When using the external compensation network techniques as previously described, there are several precautions that must be taken. The first precaution is that thermal distortion is dependent on signal swing. The distortion improves with smaller signal swings because the power changes are less. The 200 kΩ and 150 pF RC compensation network was optimized for a 40 V signal swing. For smaller signal swings, the compensation network tends to overcompensate causing the flatness to slope in the opposite direction, i.e., the smearing would appear darker than white instead of brighter than white. In this case, the CRT designer may want to adjust the compensation network (by changing the capacitor) to optimize the flatness at a different contrast level (voltage swing) on the display.

Another area of precaution is the 215 Ω input peaking resistor. Since the CR2424 is a feedback amplifier, the gain is determined by the input peaking resistor and the feedback network. The previously mentioned compensation networks were optimized for a 215 Ω input resistor. If the resistor was changed, the CR2424 would have a different gain and the compensation networks would no longer be optimized.

AN1401

Using SPICE to Analyze the Effects of Board Layout on System Skew When Designing With the MC10/100H640 Family of Clock Drivers

Prepared by
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This application note illustrates the complexities of board layout influences on the total skew of a system when designing with the MC10H/100H64x family of clock drivers. Transmission line theory and the various termination techniques are discussed. The note also presents guidelines to assist designers in analyzing their board layouts and loading schemes using SPICE simulations to predict and minimize the total skew of a system.

Using SPICE to Analyze the Effects of Board Layout on System Skew When Designing With the H640 Family of Clock Drivers

Objective

The objective of this note is to illustrate the complexities of board layout influences on the total skew of a system when designing with the H64x series of clock distribution chips. The note will present some guidelines to assist designers in using SPICE to analyze their board layouts and loading schemes to predict and minimize the total skew of a system.

The MC10H/100H64x series of devices are ECL/TTL translating clock drivers designed for systems requiring very low skew clock distribution. Skew is most often specified in terms of "Output to Output" skew and "Part to Part" skew. "Output to Output" skew refers to the maximum variation in propagation delay between similar paths of a single device. "Part to Part" skew refers to the maximum propagation delay difference between similar paths on different devices being driven by the same inputs. The H64x series' skew specifications are specified based on equal capacitive loading of all outputs. Since skew is a measurement of propagation delay, and propagation delay is dependent on capacitive loading, optimum skew performance can only be achieved when all outputs are loaded equally.

In many designs the clock will need to be routed to a number of receiving gates at different locations in the system. For the system designer, skew measured at these destinations is a foremost concern. Skew between receiving gates is a measurement of the maximum variation in propagation delay between the driving gate and each receiving gate. This implies that the designer must not only be concerned with "Output to Output" and "Part to Part" skew, but also with the propagation delay along each path of the signal. Propagation delay is a function of supply voltage, ambient temperature, and capacitive loading (C_L). Since propagation delay is dependent on supply voltage, which can vary significantly from board to board, skew between ICs on a single board will be much tighter than skew between ICs on different boards. This illustrates the advantage of placing ICs with tight skew requirements on the same power plane. Assuming that a common power plane is used and that the temperature gradient over the board is minimal, the supply voltage and ambient temperature will affect the propagation delay of all outputs in relatively the same manner, and thus should have minimal effect on skew. Propagation delay due to capacitive loading, however, may vary from output to output; significantly affecting skew. This variation is due to the dependence of capacitive loading on board layout, termination technique, and fanout.

To realize minimal skew at the receiving gates, the designers goal is to design for equal propagation delays on all paths carrying the clock signal. The remainder of this note will concentrate on illustrating the relationship of capacitive loading versus propagation delay and the relationships dependence on board layout and termination technique. Capacitive loading refers to both "device output loading" and "transmission line loading." When the interconnect line is short (less than 4.5″) the capacitive loading is seen by the output of the driving device and the propagation delay can be predicted by assuming a lumped load at the output of the device. This is referred to as "device output loading." However, when the line length exceeds 4.5″, the capacitive loading is seen by the transmission line as opposed to the output device. This will be referred to as "transmission line loading." For the case of "transmission line loading," propagation delay predictions must be based on the T_{pd} versus C_L relationship derived for a desired line length and termination technique. The propagation delay versus C_L characteristics of an I_C and a transmission line are different, therefore it is not enough to simply ensure equal C_L's on all clock paths to minimize skew.

The results of this note are applicable to the entire H64x series of ECL/TTL translating devices, although only the output section of the H641 is modeled as the driving section of the analysis circuit. The ESD protection circuitry and "package" model circuitry were included on the output of the driving device and the input of the receiving device to more accurately model real in-line circuits. The "package" model circuitry simulates the effects of the device packaging. In all cases, the input clock to the analysis circuit is a 25 MHz ECL level input (+3.15 V to +4.15 V) with 1 ns rise and fall times. Propagation delay is measured from the 50% level of the input clock to the 1.5 V level of the TTL output at the receiving gate.

Transmission Line Concepts[1,2,3]

For high speed systems, the interactions between wiring and circuitry are most easily determined by treating the interconnections as transmission lines. A brief and simplified review of transmission line theory and termination techniques will be presented before discussing the effects of termination techniques on propagation delay. For a more detailed discussion of Transmission Line Theory, refer to The Motorola MECL™ System Design Handbook.[1]

Characteristic Impedance: The conductors (interconnect trace and the AC ground plane) that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. When these distributed parameters are constant over a length of line, the line is said to have a characteristic

impedance, Z_O. Z_O is the ratio of transient voltage to transient current passing by a point on the line when a signal change occurs. The relationship between the distributed parameters, characteristic impedance, and transient voltage and current is expressed as:

$$V/I = Z_O = \sqrt{(L_O/C_O)} \qquad \text{Eq 2.1}$$

where L_O = inductance per unit length and C_O = capacitance per unit length. Z_O is expressed in Ohms, L_O in Henries, and C_O in Farads.

Propagation Velocity: Propagation velocity can also be expressed in terms of C_O and L_O:

$$v = 1/\sqrt{(L_O/C_O)} \qquad \text{Eq 2.2}$$

Termination and Reflection: When a signal travels down a transmission line, if the terminating resistance (R_T) matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must prevail at R_T. From the viewpoint of the driving device, no adjustment of output current is required. If the line is not terminated in its characteristic impedance the signal propagating down the line is partially reflected back to the source. The magnitude of the reflected voltage signal is governed by the load reflection coefficient, ρ_L:

$$\rho_L = (R_T - Z_O)/(R_S - Z_O) \qquad \text{Eq 2.3}$$

where: R_S = Source Impedance
Z_O = Characteristic Impedance of the line

The reflected signal continues to be reflected between the source and load impedances and is attenuated with each passage over the transmission line. The output response appears as a damped oscillation asymptotically approaching the steady state value. This phenomena is referred to as ringing. Ringing has an adverse affect on noise margin. To minimize ringing, three basic termination techniques are available:

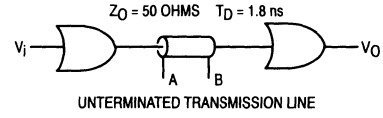
1. Minimizing Unterminated Line Length
2. Series Termination
3. Parallel AC Termination

Unterminated Lines

Figure 2.1a illustrates an unterminated transmission line. Since the reflection coefficient at the load is of opposite polarity to that at the source, the signal will be reflected back and forth over the transmission line with the polarity changing after each reflection from the source impedance. Thus, steps appear at the input to the receiving gate. When the driver gate delivers a full TTL swing, the signal propagates from point A arriving at point B a time T_D later. At point B, the signal is reflected as a function of ρ_L. The input impedance of the receiving gate is large relative to the line characteristic impedance, therefore: ρ_L is approximately equal to 1. A large positive reflection occurs resulting in overshoot. The reflected signal reaches point A at time $2T_D$, and a large negative reflection results because the output impedance of the driver gate is much less than the characteristic impedance of the line. In this case the reflection coefficient is negative. The signal is re-reflected back toward the load arriving at $3T_D$, resulting in undershoot at point B. The impetus in restricting interconnect lengths is to minimize the effects of overshoot and undershoot. A handy rule of thumb is: to limit the undershoot to 15% of the voltage swing, the two way line delay should be less than the rise time of the pulse. Thus the maximum length can be determined using the following equation:

$$L_{max} < t_R/(2*T_{pd}) \qquad \text{Eq 2.4}$$

where: L = Line Length, t_R = Rise Time
T_{pd} = Propagation delay/unit length



UNTERMINATED TRANSMISSION LINE

Figure 2.1a. Block Diagram of Unterminated Line

Maximum open line lengths for the ECL/TTL translator were derived from SPICE simulations for 10 and 20 pF loads, a maximum overshoot of 40%, and a maximum undershoot of 20%. Simulation results indicate for a 50 ohm line driving a 10 pF load, a stub length of less than 5 inches (assuming T_{pd} = 0.18 ns/inch) will limit the overshoot to less than 40%, and the undershoot to within 20% of the logic swing. When the load is increased to 20 pF the maximum line length is 4.5 inches. The results are shown in Figures 2.1b and 2.1c. To minimize undershoot the series termination or parallel AC termination technique should be used.

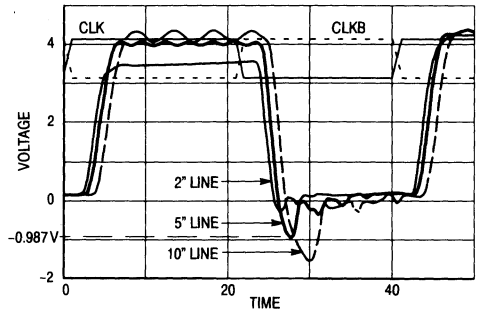


Figure 2.1b. H64x Driving a 10 pF Load over an Unterminated Line

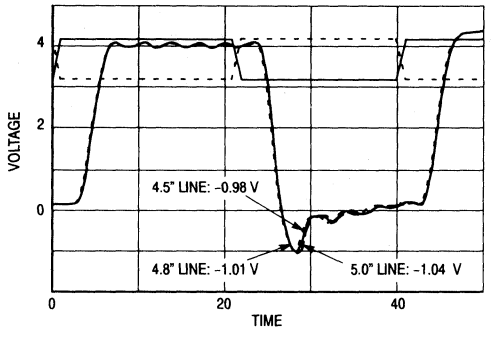


Figure 2.1c. H64x Driving a 20 pF Load over an Unterminated Line

Series Termination

Series damping is a technique in which a termination resistance is placed between the driver and the transmission line with no termination resistance placed at the receiving end of the line. Series termination, illustrated in Figure 2.2a,

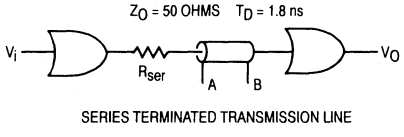


Figure 2.2a. Block Diagram of Series Terminated Line

is a special case of series damping in which the sum of the termination resistor (R_{ser}) and the output impedance of the gate (R_O) is equal to the line characteristic impedance, resulting in minimum undershoot and overshoot.

$$R_{ser} + R_O = Z_O \qquad \text{Eq 2.5}$$

With series termination, when the output of the driver gate switches, a change in voltage, delta V, occurs at the input to the transmission line:

$$\Delta V = V_{in}^* (Z_O)/(R_{ser} + R_O + Z_O) \qquad \text{Eq 2.6}$$

For a matched series termination: $R_{ser} + R_O = Z_O$, thus $\Delta V = V_{in}/2$. So an incident wave of half amplitude travels down the transmission line. Since the transmission line is unterminated at the receiving end, the reflection coefficient of the load is approximately unity; therefore causing the voltage to double at the receiving end. When the reflected wave arrives at the source it is completely absorbed by the series resistor since the impedance matches the characteristic impedance of the transmission line. The output impedance of the driving device was obtained by extracting the V_{OL} versus I_{OL} and the V_{OH} versus I_{OH} curves (refer to Figures 2.2b and 2.2c). The output impedance of the device is equal to the slope of the curves, which can be calculated to be approximately 8 Ω. This value was verified using SPICE simulations. R_{ser}, in Figure 2.2a was varied from 10 Ω to 50 Ω in 10 Ω increments and the signal was monitored at the input to the receiving gate (refer to Figure 2.2d). Minimal undershoot and overshoot occurred when the resistance of the output driving circuit was assumed to be 10 Ω. This value closely agrees with the 8 Ω value measured in the lab. So, the value of R_{ser} should be set to $(Z_O-10)\Omega$ for a matched series termination.

Series termination is useful when the interconnect lengths are long or impedance discontinuities exist on the line. Another advantage of using series termination is that the signal travels down the line at half amplitude, minimizing problems associated with crosstalk and EM Radiation. The drawbacks of this technique are twofold. First, is the possibility of a two step signal appearing when the driven inputs are far from the end of the transmission line. Second, series termination has limited use in TTL interconnect schemes due to the voltage drop across R_{ser} in the low state. Any voltage drop across R_{ser} will reduce noise margin (NM) at the receiver. This is illustrated below by calculating the NM_L of a TTL driver/receiver pair, using data book values of I_{IL}, V_{OL} and V_{IL}.

$$\begin{aligned} \text{TTL:}\quad NM_L &= V_{OL}\ \text{max} - [V_{IL}\ \text{max} + I_{IL}\ (R_{ser})] \\ &= 0.8\ \text{V} - [0.5\ \text{V} + 0.4\ \text{mA}\ (40\ \Omega)] \\ &= 0.284\ \text{V} \end{aligned}$$

However, when driving CMOS inputs, which pull very little input current, very little NM is lost due to the series termination resistor. Thus, series termination is a viable termination technique when driving CMOS gates.

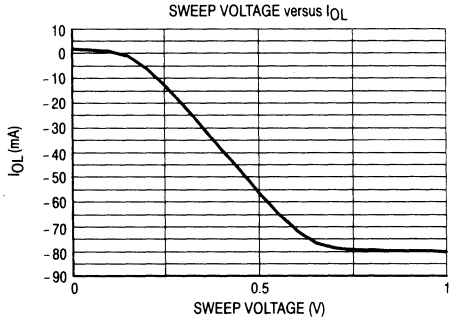


Figure 2.2b. V_{OL} versus I_{OL} for H64x Series

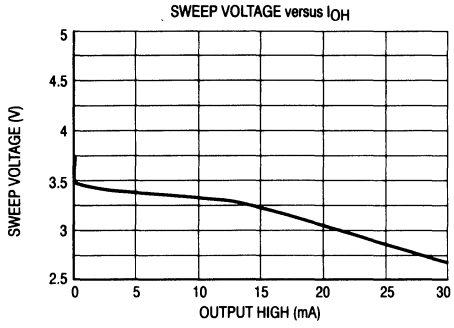


Figure 2.2c. V_{OH} versus I_{OH} for H64x Series

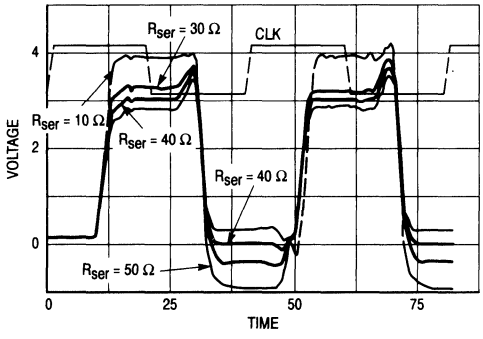
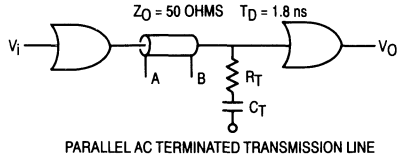


Figure 2.2d. Series Terminated Transmission Line Output for R_{ser} = 10, 30, 40, and 50 Ω

Parallel AC Termination

Parallel AC Termination, shown in Figure 2.3, should be used when the ability to drive distributed loads or when driving heavy DC TTL loads is required. Unlike series termination, the parallel AC termination scheme features an undistorted waveform along the full length of the line. In parallel AC termination, the receiving end is terminated to a voltage through a resistor (R_T) in series with a capacitance (C_T). The value of R_T is equal to the line characteristic impedance. As a rule of thumb $C_T = 10*T_D/Z_O$, where T_D is the delay of the transmission line. When the termination resistance matches the line impedance, no reflection occurs because all the energy is absorbed by the termination. The parallel AC termination scheme consumes no DC current with outputs in either state.



PARALLEL AC TERMINATED TRANSMISSION LINE

Figure 2.3. Block Diagram: Parallel AC Termination

DERIVATION OF T_{pd} versus C_L RELATIONSHIPS

Once the designer has chosen a termination technique, the relationship of T_{pd} versus C_L for the specific application should be derived. It is suggested that the derivation be performed through simulations using the H64x Clock Driver I/O Spice Model Kit. A guideline for deriving the relationships, T_{pd} versus C_L is presented through examples for each termination technique discussed.

In deriving the relationships necessary to predict propagation delay a reference for T_{pd} is established by finding the propagation delay of the H641's output driving circuit. To measure T_{pd} of the output driving gate using SPICE, the analysis circuit shown in Figure 3.1 is used.

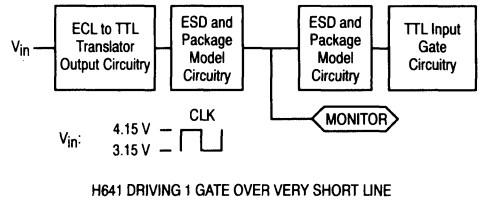


Figure 3.1. Simulation Block Diagram

In this circuit, the output driving gate is driving one gate over a very short line (<< 1"). When the interconnect line length is this short the SPICE "transmission line" model is not needed to simulate the interconnect line; and the propagation delay due to the interconnect line length can be assumed to be negligible. The propagation delay is measured from the 50% voltage level of the input signal to the 1.5 V level of the TTL output; and can be expressed as follows:

$$T_{pd(model)} = T_{pd(output\ gate)} + \Delta T_{pd(1\ gate\ load)} \quad \text{Eq 3.1}$$

Through a SPICE simulation $T_{pd(model)}$ was measured to be 2.76 ns. Rewriting the equation above to solve for $T_{pd(output\ gate)}$, the equation becomes:

$$T_{pd(output\ gate)} = 2.76\ ns - \Delta T_{pd(1\ gate\ load)}^{*} \quad \text{Eq 3.2}$$

To solve for $T_{pd(output\ gate)}$, the T_{pd} due to the capacitive loading of 1 gate is needed. This relationship will also be very useful in finding propagation delay contributed by fanout. By using the same circuit as above and incrementing the number of receiving gate inputs, measurements of T_{pd} are taken for each increment in the number of receiving gates in order to develop a relationship between Fanout versus Propagation Delay ($\Delta T_{pd}/\Delta$# of Gates).

The following measurements were taken:

Table 3.1

# of Gates	T_{pd} L-H (ns)	T_{pd} H-L (ns)
1	2.76	2.88
2	2.82	3.02
4	2.93	3.2
6	3.02	3.46
8	3.15	3.64
15	3.99	4.01

and plotted below:

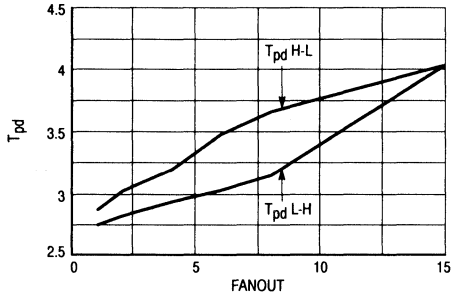


Figure 3.2. Fanout versus T_{pd} for a "Short Line"

The value of $\Delta(T_{pd})/\Delta(\#\text{ of gates})$ can be calculated by finding the slope of the Fanout versus T_{pd} curve. From Figure 3.2, $\Delta(T_{pd})/\Delta(\#\text{ of gates})$ can be measured to be, approximately:

$$\Delta(T_{pd})/\text{gate} = 0.057\text{ ns/gate.} \qquad \text{Eq 3.3}$$

$T_{pd\,(output)}$ can be calculated by substituting this data into Eq. 3.2.

$$T_{pd\,(\text{output gate})} = 2.76\text{ ns} - 0.057\text{ ns} = 2.7\text{ ns} \qquad \text{Eq 3.4}$$

Note, $T_{pd\,(output\ gate)}$ is not the propagation delay of the H64x, but, merely the propagation delay of the output circuitry common to all of the H64x series. This value and the values derived in the following T_{pd} versus C_L curves should not be used as actual values of propagation delay for the H64x series and are derived here only as a reference on which to base the effects of line length, fanout, and termination technique on the propagation delay of the H64x devices.

In real system designs, it will not always be realizable for the designer to have equal line lengths and fanout on each output. In attempting to achieve symmetrical loading on each output the designer will need to compensate for unsymmetrical loading by either adding line length or capacitive loads on appropriate lines. If the designer knows the skew between two paths, a relationship between capacitive loading and propagation delay is needed to determine the capacitive load needed for compensation. To determine this relationship, the circuit in Figure 3.1 was modified by adding a load capacitor in parallel with the receiving gate, the value of the load capacitor was varied and measurements of the propagation delay taken for each value of C_L. The data is summarized and shown in a plot in Table 3.2 and Figure 3.3a, respectively.

Table 3.2

C_L (pF)	T_{pd} L-H (ns)	T_{pd} H-L (ns)
0	2.76	2.88
10	2.98	3.34
20	3.19	3.76
30	3.39	3.99
40	3.52	4.18
50	3.75	4.35
70	4.07	4.66

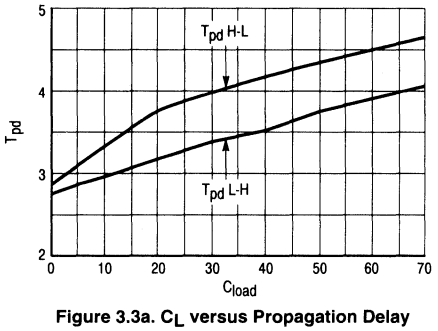


Figure 3.3a. C_L versus Propagation Delay for Short Line

From this data the change in propagation delay with respect to the change in C_L was calculated and the sensitivity of the output driver to capacitive loading for an unterminated "short" line was found to be 0.02 ns/pF. The capacitive load (C_L) per gate can be calculated by taking the ratio of delay/gate to delay/C_L.

$$C_L/\text{gate} = (0.057\text{ ns/gate})/(0.02\text{ ns/pF}) = 2.85\text{ pF/gate} \qquad \text{Eq 3.5}$$

When board layout constraints demand that line lengths exceed 4.5″, the effects of capacitive loading are no longer seen at the output of the gate (output loading) but instead are seen by the line (transmission line loading). SPICE simulations of Output gate Delay versus Line Length are shown in Figure 3.3b. Notice that for line lengths less than 4.5″ the Output gate Delay increases linearly as the line length (or capacitive load) increases. For line lengths greater than 4.5″ the Delay curve sharply rolls off and approaches a constant value. The rolloff occurs when the output gate no longer sees the capacitive load at the end of the transmission line. The output gate sees only the "load" of the transmission line and thus, T_{pd} approaches a constant value. So, for accurate simulations of T_{pd} versus C_L when lines are greater than 4.5″, the line should be modeled as

a transmission line and the effect of capacitive loading on propagation delay re-evaluated.

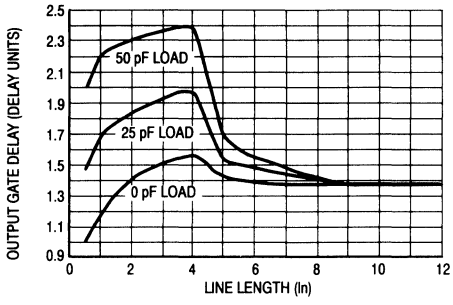


Figure 3.3b. T_{pd} versus Line Length

Using the SPICE model of a transmission line, three termination techniques will be examined. The transmission line model chosen for this exercise is available in the SPICE simulator and assumes a propagation delay of 0.18 ns/inch. Relationships between line length and termination technique will be developed along with relationships between propagation delay and capacitive loading for each termination type.

CASE 1: UNTERMINATED TRANSMISSION LINE

The analysis circuit, in Figure 3.1, was modified by inserting a transmission line between the output driving circuit and the receiving gate circuit. A capacitor, C_L, was hung in parallel with the receiving gate. (Refer to Figure 3.4).

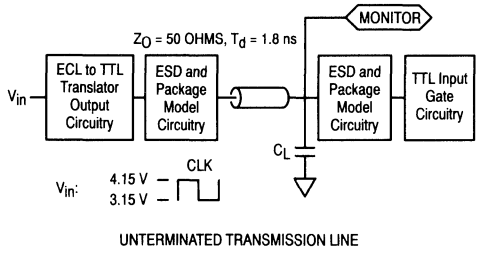


Figure 3.4. SPICE Model for Unterminated Line

To determine a relationship between T_{pd} versus C_L for the Unterminated transmission line, the capacitive load was varied and measurements of propagation delay at the load were taken for each value of C_L. The results are tabulated in Table 3.3 along with the measurements taken for a transmission line with Z_O = 75 ohms:

Table 3.3

C_L (pF)	T_{pd} (ns), Z_O = 50	T_{pd} (ns), Z_O = 75
0	4.3	4.27
10	4.71	4.79
20	5.03	5.2
30	5.31	5.55
40	5.56	5.86
50	5.8	6.16
60	6.02	6.44
70	6.22	6.71
100	6.82	7.45

*Note: T_{pd} includes the 1.8 ns delay of the transmission line.

Plotting C_L versus T_{pd}, the relationship is shown in Figure 3.5.

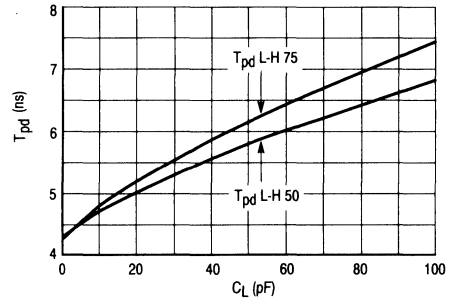


Figure 3.5. C_L versus T_{pd} for Unterminated Line

A comparison between Figure 3.3a and Figure 3.5 shows that output loading versus transmission line loading produces a nonlinear change in the T_{pd} versus C_L curves. This implies that, for line lengths > 4.5″ the designer should use the T_{pd} versus C_L curve which corresponds to transmission line loading, for predicting propagation delay. Figure 3.5 shows T_{pd} versus C_L curves for unterminated transmission lines with Z_O of 50 Ω and 75 Ω. Notice, the $\Delta T_{pd}/\Delta C_L$ increases as Z_O increases. This is due to the fact $C_{O50\Omega} > C_{O75\Omega}$. This demonstrates an advantage of using lines with lower Z_O.

CASE 2: SERIES TERMINATED TRANSMISSION LINE

The analysis circuit, in Figure 3.4, was modified by inserting a series resistor between the output driving circuit and the transmission line. A capacitor, C_L, was hung in parallel with the receiving gate. The resulting circuit is shown in Figure 3.6.

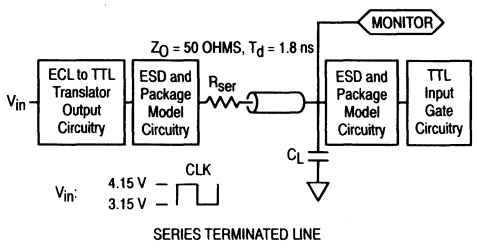


Figure 3.6. Simulation Circuit: Series Terminated Line

First, Z_O was set to a common value of 50 ohms and the line length was set to 10″, which translates to a line delay, T_D, of 1.8 ns. With C_L set to 0 pF and measuring the propagation delay at the output of the transmission line, the accuracy of the transmission line model's T_D can be confirmed by comparing this measurement to the measured vlaue of T_{pd} at the input of the transmission line. The equation for the measured T_D is:

$$T_D = T_{pdout} - T_{pdin}. \qquad \text{Eq 3.6}$$

Plugging measured values into this equation for the above circuit:

$$T_D = 4.69 \text{ ns} - 2.9 \text{ ns} = 1.79 \text{ ns} \qquad \text{Eq 3.7}$$

and we see it is very close to the predicted delay of (0.18 ns/inch)* 10 inches = 1.8 ns.

To determine a relationship between T_{pd} versus C_L for matched series termination, the capacitive load was varied and measurements of propagation delay at the load were taken for each value of C_L. The results are tabulated below along with the measurements taken for a transmission line with Z_O = 75 ohms:

Table 3.4

C_L (pF)	T_{pd} (ns), Z_O = 50	T_{pd} (ns), Z_O = 75
0	4.7	4.7
10	5.24	5.44
20	5.7	6.08
30	6.08	6.62
40	6.45	7.11
50	6.82	7.62
60	7.18	8.1
70	7.53	8.6
100	8.57	9.97

*Note: T_{pd} includes the 1.8 ns delay of the transmission line.

Plotting C_L versus T_{pd}, refer to Figure 3.7, the relationship between C_L and T_{pd} is found to be a linear equation, when the termination is matched, that can be expressed as follows:

$$T_{pd} = Z_O{}^* C_L + T_D + \text{delay of output circuit} \qquad \text{Eq 3.8}$$

slope: Z_O
y-intercept: T_D + delay of output circuit

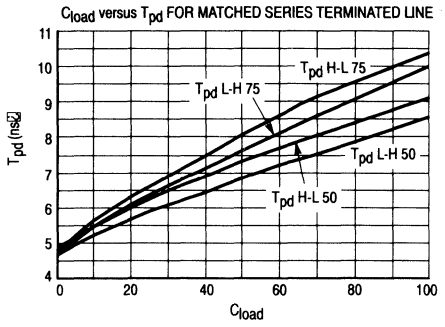


Figure 3.7. C_L versus T_{pd}: Series Terminated Line

Comparing these results to the results obtained for an unterminated line, it can be observed that the T_{pd} versus C_L relationship is not only affected by line length, but also, by the termination technique chosen by the designer. Using series termination produces a significant decrease in undershoot and overshoot. The tradeoff is an increase in $\Delta T_{pd}/\Delta C_L$. Notice, even when the gate is unloaded, the series terminated line is slower than the unterminated line.

CASE 3: PARALLEL AC TERMINATION WITH LUMPED LOAD

The original circuit was modified by inserting a transmission line between the output driving circuit and the receiving gate circuit. The circuit is shown in Figure 3.8. For Parallel AC Termination the matching network is a shunt resistor (R_T) in series with a capacitor (C_T) to ground, placed at the output of the transmission line. From transmission line theory, the Parallel AC Termination technique requires that the resistance of R_T match the characteristic impedance of the transmission line (Z_O) for optimum performance (minimum undershoot and overshoot and minimum propagation delay). Also as a rule of thumb the optimum C_T can be calculated as, $C_T = 10^*T_D/Z_O$, where T_D = the delay of the transmission line and Z_O is the characteristic impedance of the transmission line.

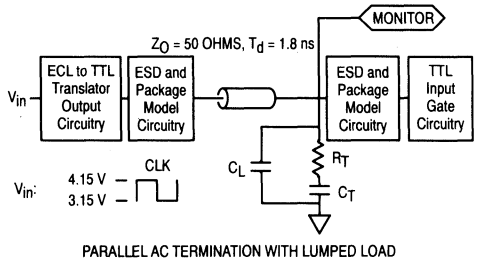


Figure 3.8. Simulation Circuit: Parallel AC Termination

With Z_O set to 50 ohms and T_D set to 1.8 ns, R_T and C_T were calculated as 50 ohms and 360 pF, respectively. C_L was varied and propagation delay measurements recorded at each value of C_L. Next, Z_O was set to 75 ohms and T_D to 1.8 ns. Values of R_T and C_T were recalculated for these conditions and set to 75 ohms and 240 pF, respectively. Again C_L was varied and propagation delay monitored. The results are tabulated in Table 3.5.

Table 3.5

C_L (pF)	T_{pd} (ns), Z_O = 50	T_{pd} (ns), Z_O = 75
0	5.01	4.86
5	5.17	
10	5.32	5.32
15	5.47	
20	5.63	5.73
25	5.75	
30	5.88	6.06
35	6.00	
40	6.14	6.4
45	6.26	
50	6.38	6.71
55	6.50	
60	6.61	6.95
70	6.85	7.28
100	7.54	8.03

*Note: T_{pd} includes the 1.8 ns delay of the transmission line.

Plotting C_L versus T_{pd} results in the relationship shown in Figure 3.9.

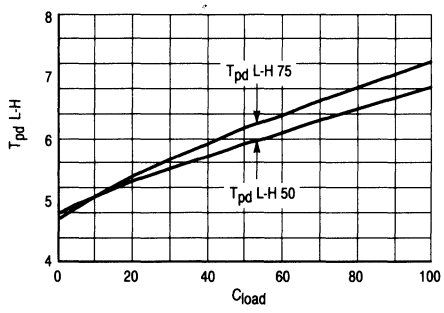
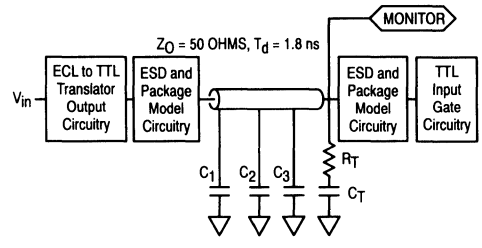


Figure 3.9. C_L versus T_{pd}: Parallel AC Termination

A comparison of the results of the Parallel AC termination scheme versus the unterminated scheme illustrates almost no increase in $\Delta T_{pd}/\Delta C_L$. However, the propagation delay for a Parallel AC terminated line driving a 0 pF load is greater than that for an unterminated line or a series terminated line driving 0 pF. So, choosing Parallel AC termination over an unterminated line significantly decreases undershoot and overshoot, however, it causes a positive linear shift in the T_{pd} versus C_L curve. Series termination caused an increase in $\Delta T_{pd}/\Delta C_L$ of approximately 0.01 ns/pF for a transmission line with a Z_O of 50 Ω. As a result, propagation delays for series terminated lines quickly pass those of Parallel AC terminated lines as capacitive load is increased. The tradeoff in choosing Parallel AC termination over series termination is that Parallel AC termination requires an extra capacitor, C_T, in each matching network. Comparing the T_{pd} versus C_L curves for Z_O = 50 Ω and 75 Ω in Figure 3.9 it is seen that, as was the case in the other examples, the $\Delta T_{pd}/\Delta C_L$ increases as Z_O increases.

CASE 4: PARALLEL AC TERMINATION WITH DISTRIBUTED LOAD

The original circuit was modified by inserting three separate transmission lines between the output driving circuit and the receiving gate circuit. The sum of the time delay of the three transmission lines being 1.8 ns, to be consistent with the data taken for the other termination techniques. Capacitive loads are placed at the end of each transmission line. The parallel AC matching network is placed at the end of the last transmission line. The circuit is shown in Figure 3.10.



PARALLEL AC TERMINATION WITH DISTRIBUTED LOAD

Figure 3.10. Simulation Circuit: Parallel AC Termination

Table 3.6

C_L (pF)	T_{pd} L-H (ns)
0	5.01
15	5.35
25	5.54
30	5.68
45	5.98
60	6.29
90	6.84

*Note: T_{pd} includes the 1.8 ns delay of the transmission line.

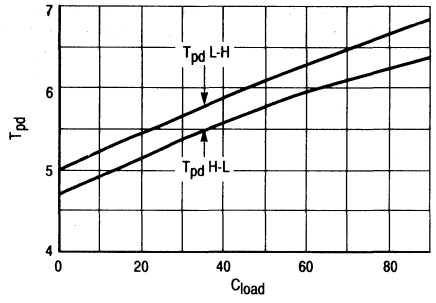


Figure 3.11. C_L versus T_{pd}: Distributed Load: Parallel AC Termination

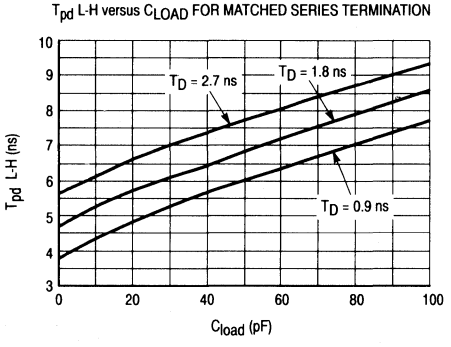


Figure 3.12. (T_{pd} versus C_L) versus T_D for Series Termination

With Z_O set to 50 ohms and T_D set to 1.8 ns. Using the equations above R_T and C_T were calculated as 50 Ω and 360 pF, respectively. Total C_L was varied and propagation delay measurements recorded at each value of C_L. The results are tabulated in Table 3.6. Plotting C_L versus T_{pd} gives the relationship shown in Figure 3.11.

Data has now been derived for the relationship between capacitive loading versus propagation delay for the following termination techniques: unterminated transmission lines, series termination, and parallel AC termination. To generalize these results for any interconnect line length, the relationship of (C_L versus T_{pd}) versus Line Length must be evaluated. Using the series termination circuit configuration, the delay (line length) of the transmission line is varied from T_D = 0.9 ns to T_D = 1.8 ns to T_D = 2.7 ns. At each line length setting a "C_L versus T_{pd}" curve was extracted. The results are summarized in the plot, Figure 3.12.

Notice, changing the length of the transmission line merely causes a vertical shift of the Series Terminations' "T_{pd} versus C_L" curve. This will be found true for the unterminated and the parallel AC termination schemes as well. So, by determining the relationship, T_{pd} versus T_D for each termination technique when C_L = 0, the designer could determine the y-intercept of that termination techniques' "T_{pd} versus C_L" curve for a desired line length.

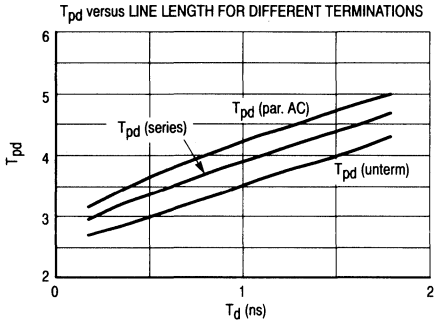


Figure 3.13. (C_{Id} versus T_{pd}) versus Termination Technique

By setting the capacitive load to 0 pF for each type of termination, and varying the line length only; this type of relationship is established. The results are shown in Figure 3.13. Once the designer knows the length of the transmission line and the termination technique, a "T_{pd} versus Line Length" chart can be used to determine the y-intercept of the appropriate termination schemes' "T_{pd} versus C_L" curve. Note, these values have been derived using only the output section of the H641 driving the input section of the H645. Therefore these propagation delay values are not representative of actual delays of the H64x and are derived here only to show the relationship of T_{pd} versus T_D. It is suggested that the designer derive the T_{pd} versus T_D curve with C_L = 0 pF for their specific application, using the "H64x Clock Driver I/O Spice Model Kit."

Summary

The MC10H/100H64x series ECL/TTL translating clock drivers are ideal devices for systems requiring very low skew clock distribution. Optimum skew performance from the H64x series requires equal capacitive loading on each output. To minimize skew in a system not only requires minimal "output to output" skew and "part to part" skew, but also requires equal propagation delay along all paths carrying the clock signal. Perhaps the most accurate technique of obtaining equal propagation delay along all paths is to add trace to the lines with shorter propagation delays. However, this is a trial and error method and does not always provide a feasible solution due to size constraints of the board. Another technique of obtaining equal propagation delays on each path is to add capacitive loading on paths with shorter propagation delays. This method requires an understanding

of T_{pd} versus C_L relationships. As shown in this note, T_{pd} versus C_L relationships are dependent on line length, termination technique, and the characteristic impedance of the transmission line. If line lengths are less than 4.5″, propagation delay can be predicted by assuming a lumped capacitive load at the output of the driving device. When lines exceed 4.5″ the capacitive load is no longer seen by the output driving device, but is instead seen by the transmission line. A different T_{pd} versus C_L relationship exists for the transmission line than the output device. The transmission line T_{pd} versus C_L relationship is dependent on termination technique and line characteristic impedance. The dependence on termination technique is important at line lengths greater than 4.5″ because at these lengths undershoot becomes significant enough (20% of logic swing for a 20 pF load) to necessitate some sort of termination scheme to minimize its adverse effects. Relationships of T_{pd} versus C_L were derived and compared for three termination schemes: the unterminated line, the series terminated line, and the parallel AC terminated line. All T_{pd} versus C_L curves were derived for transmission lines with T_D = 1.8 ns and Z_O = 50 Ω and 75 Ω. For all three termination schemes, increasing the characteristic impedance of the transmission line produces an increase in the $\Delta T_{pd}/\Delta C_L$ relationship. Of the three termination techniques the unterminated line had the smallest $\Delta T_{pd}/\Delta C_L$, followed by parallel AC termination, and finally series termination. The tradeoff in choosing terminated lines versus unterminated lines is, of course, minimized undershoot for an increase in $\Delta T_{pd}/\Delta C_L$. The tradeoff in choosing parallel AC termination versus series termination is an increase in the number of parts for a decrease in $\Delta T_{pd}/\Delta C_L$. Since the values in this note have been derived for the specific case of the output section of the H641 driving the input section of an H645, the values of propagation delay are not representative of actual delays of the H64x series of devices. Also, due to SPICE simulator limitations of accuracy, delays are not exact and should be used to predict relative differences only. For these reasons, the designer is encouraged to use the "H64x Clock Driver I/O Spice Model Kit" to derive the relationships necessary to predict and minimize skew for their particular system. To obtain the "H64x Clock Driver I/O Spice Model Kit" contact a Motorola representative.

References

[1]Motorola MECL System Design Handbook, second edition, Motorola Inc., 1983. Stock Code HB205R1/D.

[2]Motorola ECLinPS™ Data Book, Motorola Inc., 1991. Stock Code DL140R1/D.

[3]Fairchild FAST Applications Handbook. Fairchild Semiconductor Corporation, 1987.

AN1402

MC10/100H600 Translator Family I/O SPICE Modelling Kit

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This application note provides the SPICE information necessary to accurately model system interconnect situations for designs which utilize the translator circuits of the MC10H600 family. The note includes information on the H600, H601, H602, H603, H604, H605, H606 and H607 translators.

MC10/100H600 Translator Family I/O SPICE Modelling Kit

Objective

With the difficulty in designing highspeed controlled impedance PC boards and the expense of reworking those boards the ability to model circuit behavior prior to committing to a board layout is essential for high speed logic designers. The purpose of this document is to provide the user with enough information to perform basic SPICE model analysis on the interconnect traces being driven or driving the H600, H601, H602, H603, H604, H605, H606 or H607 translator chips. The packet includes schematics of the input and output structures as well as ESD protection structures and package models which may affect the waveshape of the input and output waveforms. Internal bias regulators and logic circuitry are not included as they have little impact on the I/O characteristics of the device and add a significant amount of time to the standard simulation analysis. In addition a SPICE parameter set for the devices referenced in the schematics is provided. The remainder of this document will introduce the various input and output stages for the H60x translators as well as the other structures which affect the I/O characteristics of these devices.

Schematic Overview

There are ten basic schematics which can be used to represent all of the I/O for the H60x family of translator chips. A single TTL input structure can be used to represent all of the TTL inputs, with the exception of the H606s "CLKT" input, which should be modeled using the "H606 TTL Input" structure. All of the ECL inputs can be represented by a single ECL input structure, with the exception of the H601s "data" inputs, the H601s ECL "TRI" and "TRIB" inputs and the H602s "ECLST" input, which should be modeled using the "H601 I/O Gate" structure, the "H601 ECL Input" structure and the "H602 ECL Input" structure, respectively. Six different output buffers represent all of the output buffers for the H60x series of translators. The rest of the schematics provided represent subcircuit schematics for the above mentioned I/O buffers, ESD protection circuitry and package models. The devices shown in shaded boxes on the I/O buffer schematics are modelled by the subcircuits illustrated on the appropriate subcircuit schematic sheet. This hieracrchical method of schematic representation is used to help simplify and clarify the buffer schematics.

The H600 and H602 utilize the same output buffer. This buffer is represented by the H600 Output schematic of Figure 6. These devices are dual supply devices which means they require +5V, –5.2V and ground supplies. The A and AN inputs should be driven differentially with the HIGH level at V_{CC} – 0.85V and the LOW level equal to V_{CC} – 1.25V and the B and BN inputs should be driven differentially with a voltage swing from –2.0V to –2.4V. Notice the ESD protection circuitry on the output, this circuitry is represented by the FPS009E schematic of Figure 15.

The H601 is also a dual supply device, however, both the input and output buffers are represented by one structure as shown in the H601 I/O Schematic of Figure 7. The H601 requires a single ended input, IN which should be driven from V_{CC} – 0.9 to V_{CC} – 1.75V. Notice the "ECL in Pad Cell" on the input, this circuitry is represented by the "ECL Input Pad Cell" schematic of Figure 15, and includes the 50KΩ input pull down resistor and the ESD protection circuity for the ECL input. The same ESD structure is used on the output buffer section of the H601 I/O Structure as is used on the H600 output buffer. The H601 I/O buffer also requires one bias supply, CBIAS, and differential tritstate buffer inputs, TRI and TRIB. The CBIAS input should be set at 1.1V, while the TRI and TRIB inputs should be driven by the "H601 ECL Input" structure of Figure 3.

The H603 Output gate is represented by the schematic of Figure 8. The IN and INB inputs should be driven differentially with voltage swings of VCC to VCC – 0.85V. The CBIAS input should be forced to 1.1V and the ENA input should be driven from VCC – 0.85 to VCC – 10.85V. The H603 again uses the same ESD protection scheme as the H600.

Table 1. Device Type Input Cross Reference

Part Type	ECL Inputs	TTL Inputs	H601 I/O	H606 TTL Inputs	H602 ECL Inputs	H601 ECL Inputs
H600	ECLST	TTLST, D0–D8	None	None	None	None
H601	None	TTLOE	D0–D8	None	None	ECLOE
H602	LEN, RESET	D0–D8	None	None	None	None
H603	All Inputs	None	None	None	None	None
H604	RESET, CLK, CLKN	CLKT, D0–D5	None	None	None	None
H605	All Inputs	None	None	None	None	None
H606	CLK, CLKN, RESET	None	None	CLKT, D0–D5	None	None
H607	All Inputs	None	None	None	None	None

The H604 and H606 utilize the same output buffer. This buffer is represented by the "H604 Output Schematic" of Figure 11. The IN and INB inputs should be driven differentially with voltage swings from V_{CC} – 0.85 to V_{CC} – 10.85V. Note, the ESD protection circuitry is the same as the H600.

Figure 12 represents the schematic for the output buffer utilized by the H605. The IN and INB inputs should be driven differentially from V_{CC} – 0.85 to V_{CC} – 10.85V, while CBIAS is forced to 1.1V. Again, the same ESD protection scheme is used as on the H600.

The H607 output buffer is represented by the schematic of Figure 13. The IN and INB inputs should be driven differentially from V_{CC} to V_{CC} – 1.8V. The ESD protection circuitry is the same.

Two input structures can represent most of the inputs for the H60x family of translators, one for TTL inputs and one for ECL inputs. The exceptions were discussed previously and the various inputs and appropriate input models are summarized in Table 1. For the dual supply devices with ECL inputs the V_{CC} and the V_{EE} on the typical ECL input gates should be tied to ground and –5.2V respectively. All input pins should have both a package model and ESD protection circuitry connected to them. For TTL inputs the ESD protection circuitry is represented by the FPS009E schematic of Figure 15. For ECL inputs the ESD protection circuitry is represented along with a 50KΩ input pull down resistor as part of the "ECL in Pad Cell" represented in Figure 15. The "Package Model" of Figure 15 is self explanatory, the parasitic values provided are worst case numbers. The package capacitance combines with the parasitic transistor capacitance of the input device and the ESD circuitry to comprise the load capacitance of the input. The various input buffer ESD circuits are outlined in Figure 15, notice that the ECL inputs utilize a different structure than the TTL inputs and outputs. The typical ECL input schematic represents a single ended ECL input, the VBB reference should be tied to V_{CC} – 1.3V and the VCS bias should be tied to V_{EE} + 1.3V. To simulate a differential ECL input one simply connects the complimentary input to the "V_{BB}" side of the input gate along with an associated ESD and package model. The differential input does not use the V_{BB} switching reference.

For all of the input and output buffer schematics the resistors should NOT be simulated as simple SPICE resistors. Because these resistors are realized by a diffusion step in wafer processing there are parasitic capacitances associated with each. The subcircuit schematic is shown for the resistors in the "Resistor Model" schematic of Figure 15. The value of each subcircuit resistor is one half the value given on the top level schematic and the parasitic capacitance is modelled by a diode back biased to V_{CC}. Also note that the resistor temperature coefficient (TC) values for both the resistor subcircuit and the resistors in the device subcircuits are provided. For modelling at nominal temperatures only, these TC's can be omitted. If however modelling will be performed at the temperature extremes the TC information should be included.

Table 2 is provided to summarize the various internal voltage swings and bias levels required to run the appropriate SPICE simulations.

Table 2. Input and Bias Levels

Schematic	Input	Level
ECL Input	V_{BB} V_{CS}	V_{CC} – 1.3V V_{EE} + 1.3V
H600, H602 Output	A/AN B/BN V_{CS}	V_{CC} – 0.85V to V_{CC} – 1.25V V_{CC} – 2.0V to V_{CC} – 2.4V V_{EE} + 1.3V
H601 I/O	IN CBIAS TRI/TRIB V_{CS} V_{BB}	V_{CC} – 0.85V to V_{CC} – 1.85V 1.1V –2.1V to –2.5V V_{EE} + 1.3V V_{CC} – 1.3V
H603 Output	IN/INB ENA V_{CS} V_{BBP} CBIAS	V_{CC} to V_{CC} – 0.85V V_{CC} – 0.85V to V_{CC} – 1.85V V_{EE} + 1.3V V_{CC} – 2.1V 1.1V
H605 Output	IN/INB CBIAS V_{CS}	V_{CC} – 0.85V to V_{CC} – 1.29V 1.1V V_{EE} + 1.3V
H604, H606 Output	V_{CS}	V_{EE} + 1.3V
H607 Output	IN/INB	V_{CC} to V_{CC} – 0.85V

Handling Power Supplies

It is important to properly apply the power supply voltages to accurately model these circuits. This section will explain the power supply terminology used on the I/O buffer schematics and how to properly apply these supplies with the appropriate package model.

Table 3. Power Pin Descriptions

Power	Description
EVCC	EVCC is the most positive supply for the ECL input gate (+5V for the H607 and ground for H600–H606)
VEE	V_{EE} is the most negative supply for an ECL gate. For the H607 it is equal to ground, for the H600–H606 it is equal to –5.2V
TVCCI	Internal V_{CC} for TTL circuitry
GNDI	Internal ground for TTL circuitry

Table 3 lists the voltage supplies referenced on the I/O schematics along with a description of each. The key to properly simulating these power supplies is in the application of the package model. Because the output buffers, to a varying degree, share VCC and ground pins, adjustments need to be made to get a more accurate model if all of the outputs are not simulated at the same time. If for example a single output is to be simulated the package model for the TVCCI and TGNDI supplies should be scaled based on the number of outputs which normally share the supplies. If the simulated output normally shares its supplies with two other outputs the package inductance would be tripled to simulate the same inductive glitch seen on the power pin in an actual application. The capacitive value for the package model is not as critical and thus can be left alone. This method will allow users to more accurately model an output behavior without resorting to

more accurately model an output behavior without resorting to more complicated and lengthy simulations. The internal power and ground pins are all powered through a single pin and are basically static, as a result no adjustments are needed for the package models on these supplies. Table 4 outlines the internal power distribution for the H60x translators, this information can be used to determine the scaling factors for the package inductance for the output buffers. To use the table simply identify the output in question and divide the number of outputs in the group by the number of power pins for that group, this will give the multiplication factor for the inductance.

Summary

The information included in this kit should provide the user with all of the information necessary to do SPICE level system interconnect modelling. The schematic information provided in this document is available in netlist form through EMAIL or an IBM or Macintosh disk. However with today's advanced design tools it will probably be a simpler task to enter the schematics in a good schematic capture package than it will be to manipulate the generic netlists. If, however the netlists are desired or questions arise about the contents of this document the user can contact an ECL applications engineer for assistance.

Table 4. Power Pin versus Outputs

Part Type	Number of Outputs	Number TVCC	Number TGND
H600	9	3	N/A
H601	9	2	3
H602	9	3	N/A
H603	9	2	3
H604	12	3	N/A
H605	6	2	2
H606	3	3	N/A
H607	6	2	2

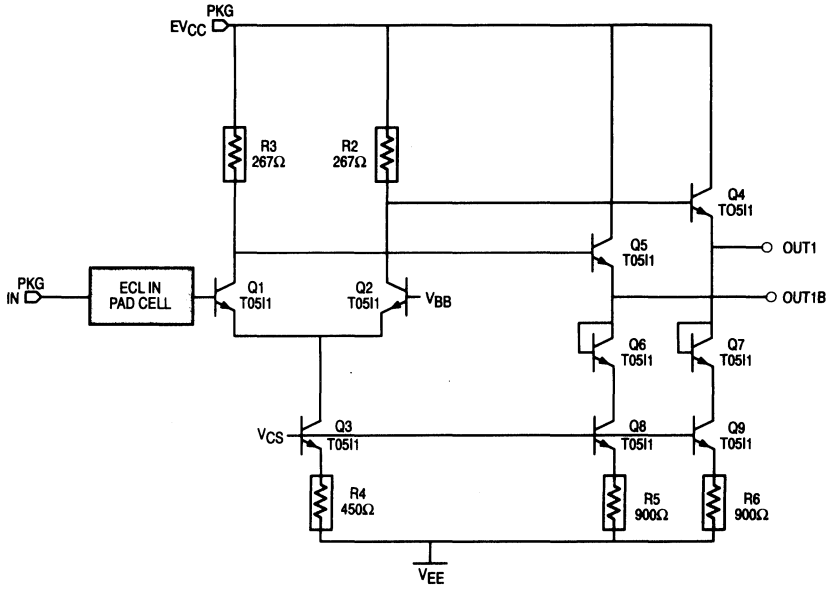


Figure 1. Typical ECL Input Gate

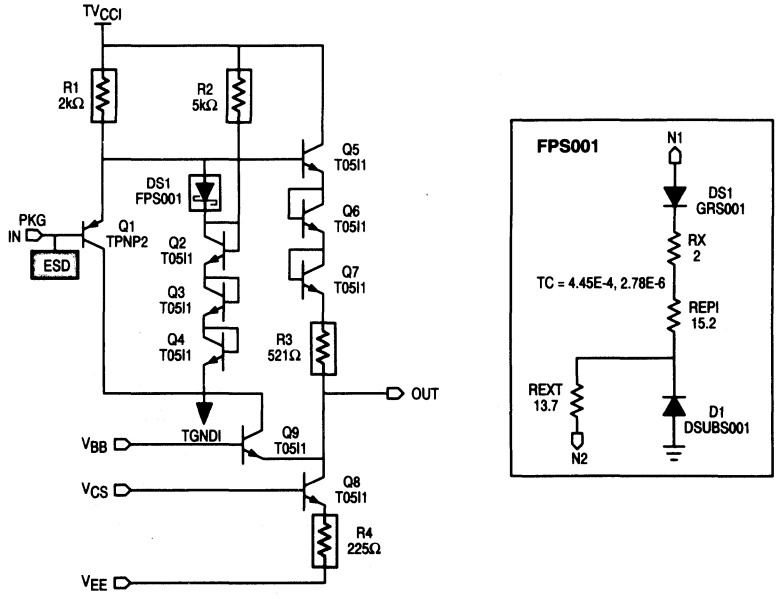


Figure 2. Typical TTL Input Gate

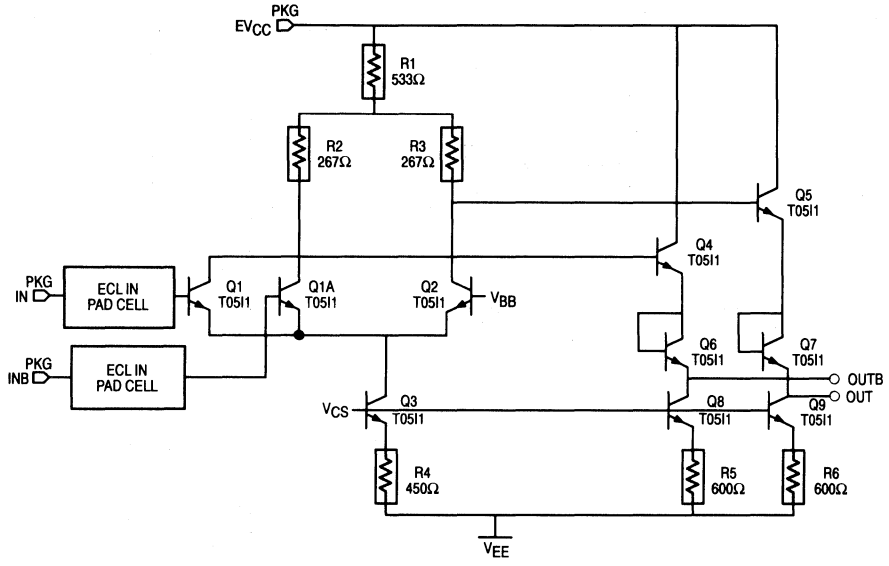


Figure 3. H601 ECL Input Gate

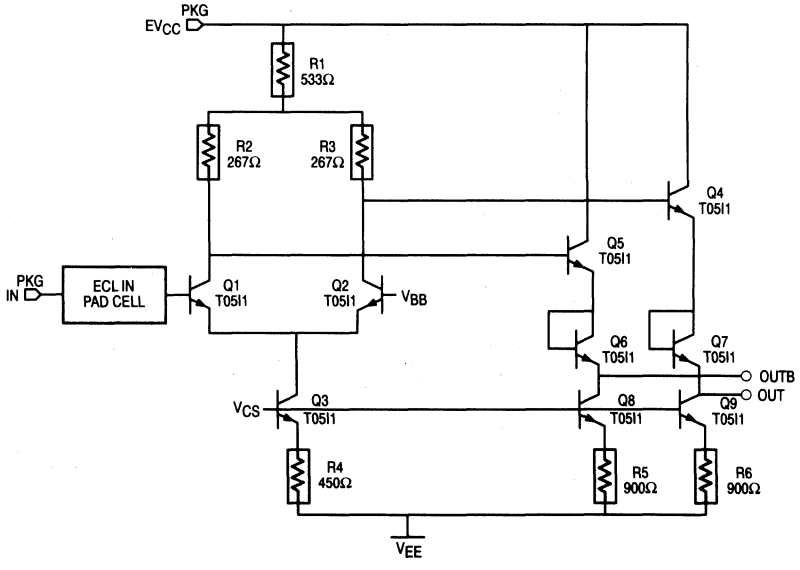


Figure 4. H602 ECL Input Gate

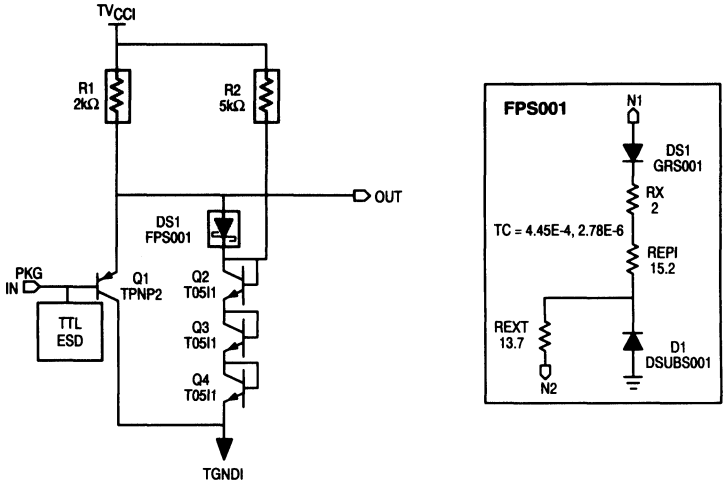


Figure 5. H606 TTL Input Gate

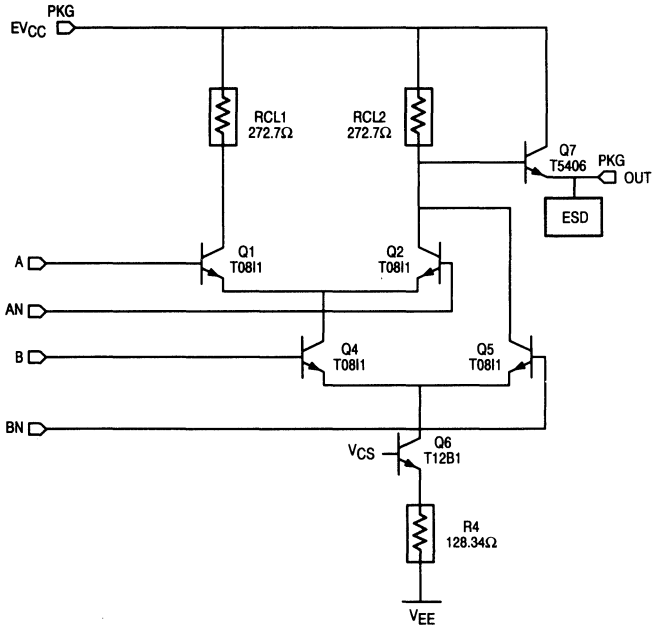


Figure 6. H600, H602 Output Gate

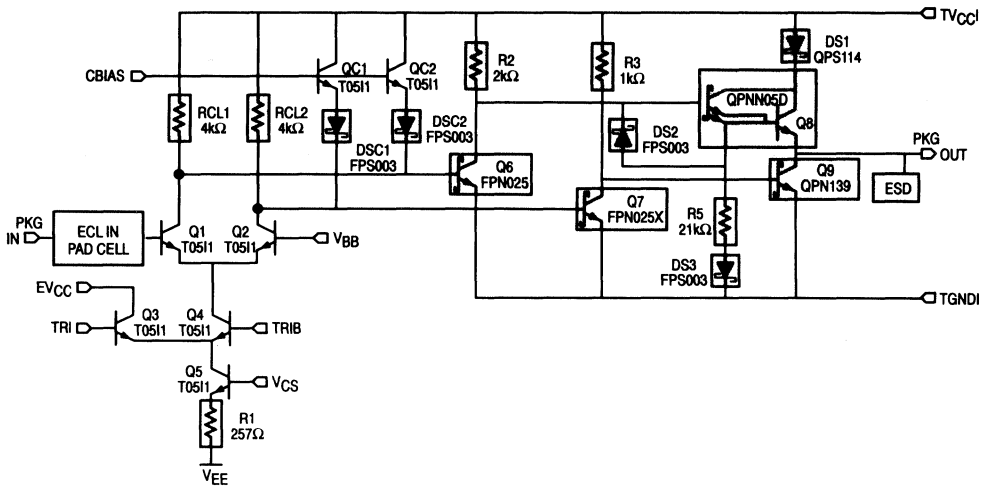


Figure 7. H601 I/O Gate

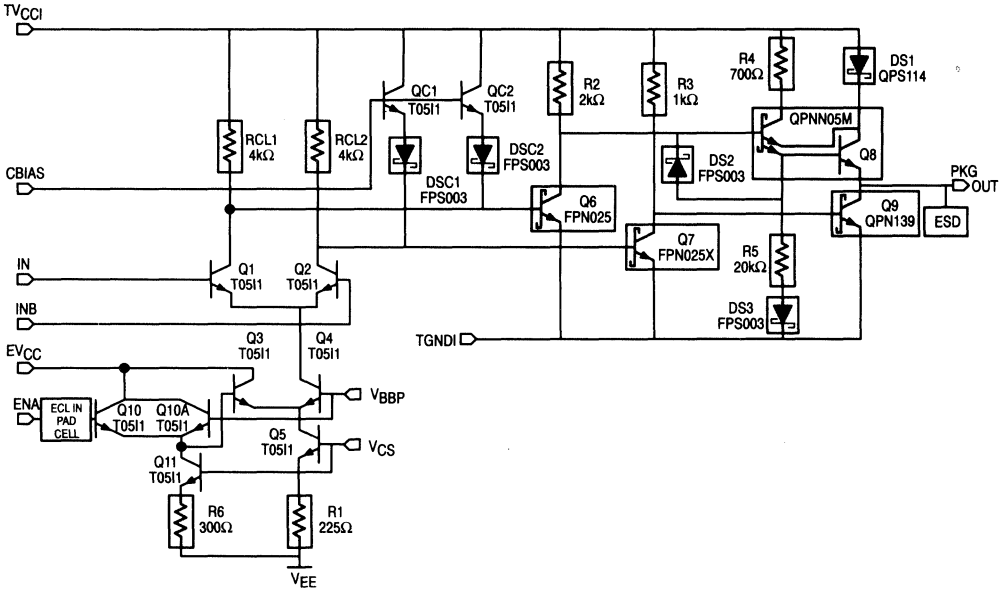
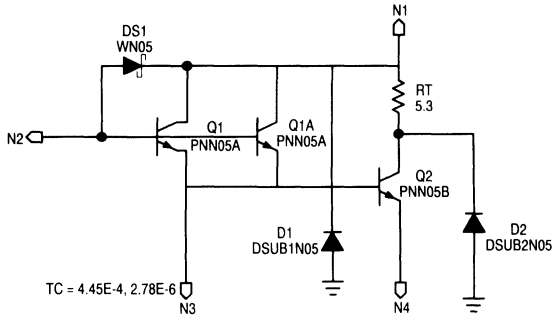


Figure 8. H603 Output Gate



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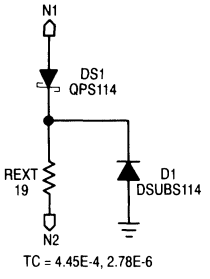
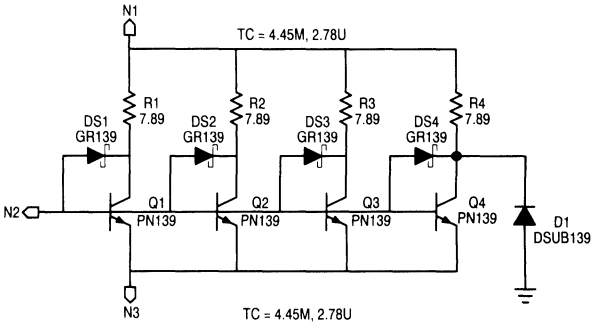
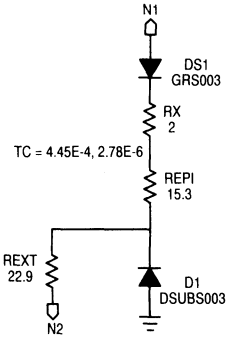


QPS114



QPN139



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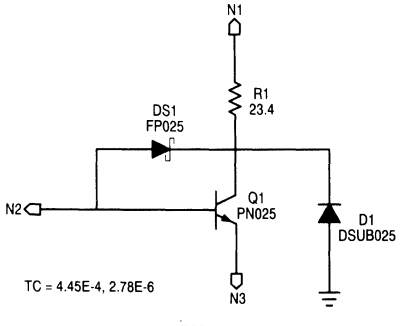

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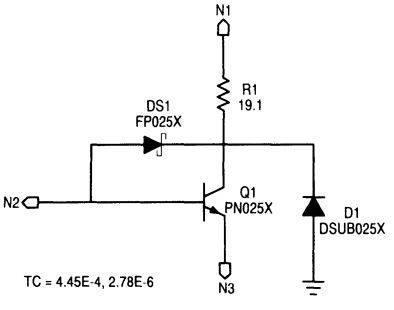
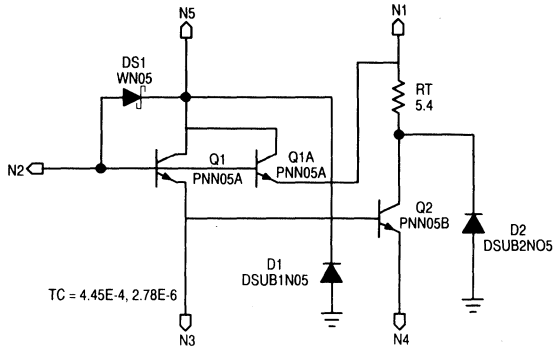
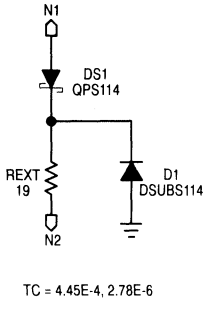


FPN025X

Figure 9. H601 Output Subcircuits



QPNN05M



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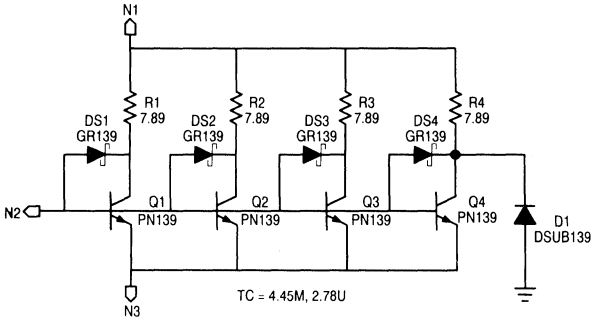

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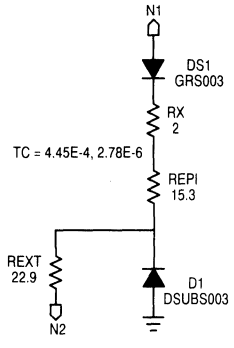

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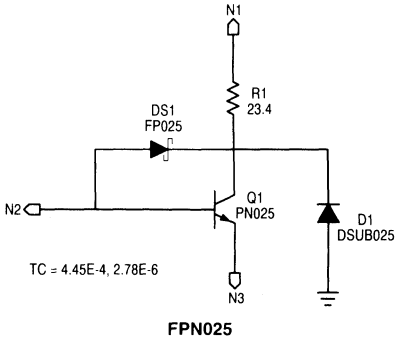

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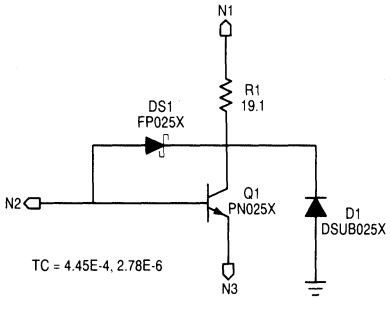


FPN025X

Figure 10. H603 Output Subcircuits

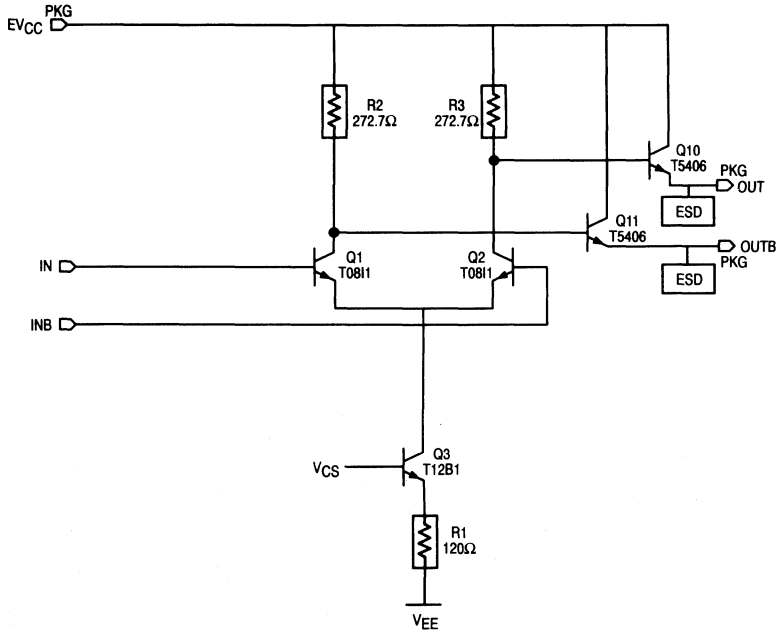


Figure 11. H604, H606 Output Gate

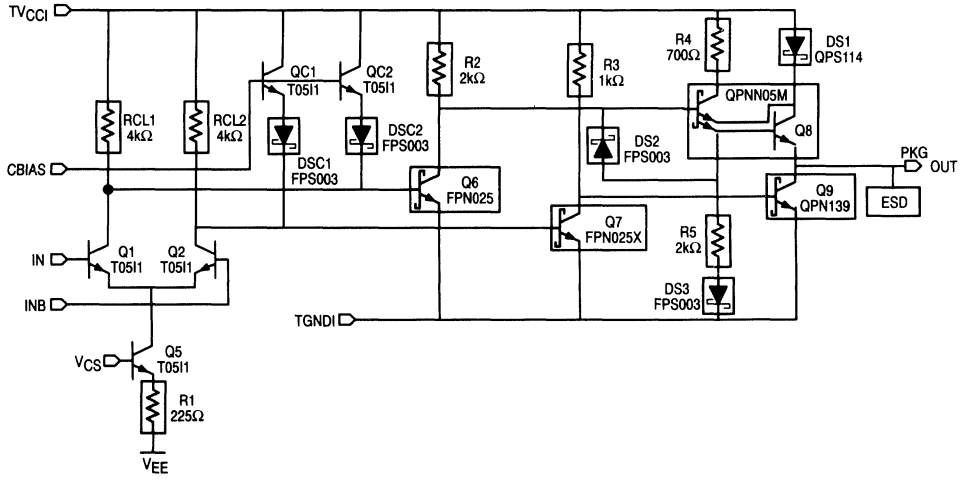


Figure 12. H605 Output Gate

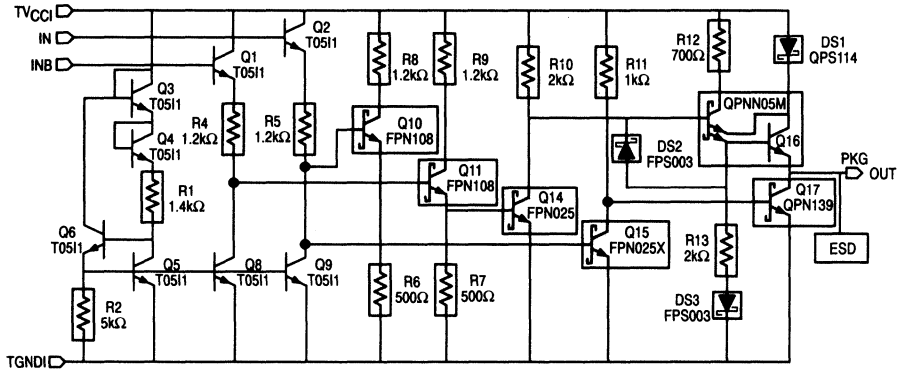


Figure 13. H607 Output Gate

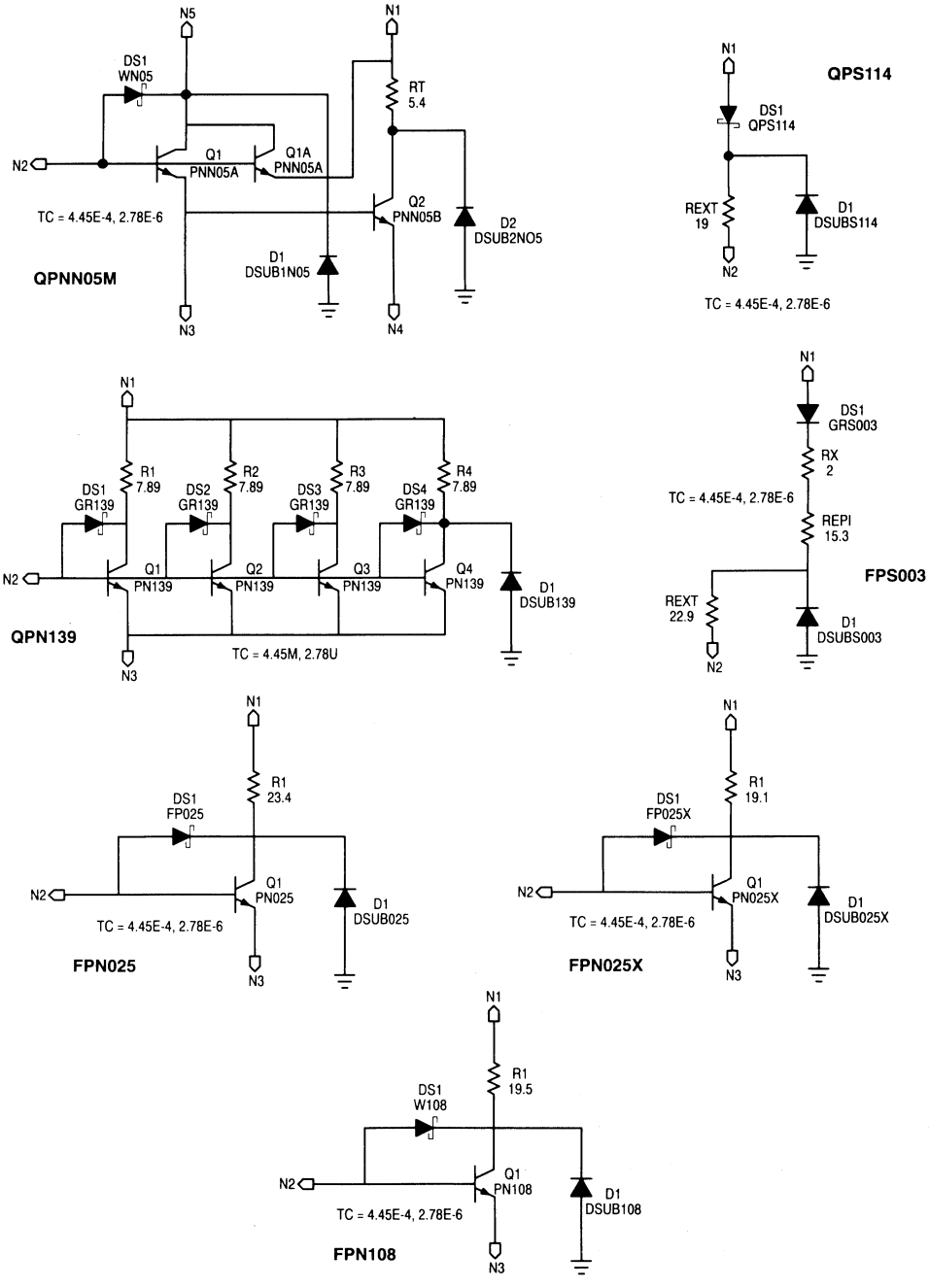
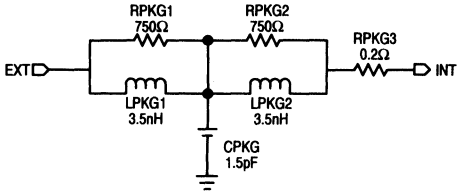
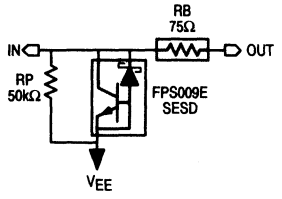


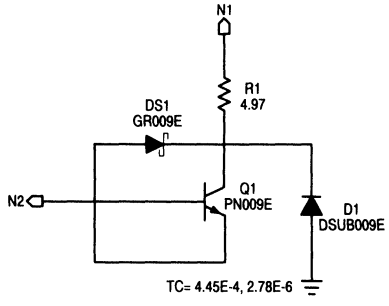
Figure 14. H607 Output Subcircuits



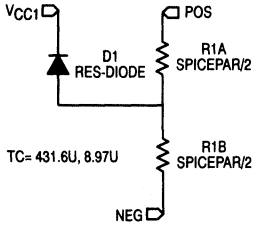
Package Model
(28-lead PLCC)



ECL Input Pad Cell



FPS009EX



Resistor Model

Figure 15. Miscellaneous Subcircuits

SPICE Parameter List

TTL Subcircuit Models

```
.MODEL GRS001 D          (IS=4.27E-14 RS=53 N=1.044 TT=10PS
+              CJO=54FF VJ=.4 M=.33
+              EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS001 D        (IS=1E-16 RS=0 N=1TTt=500PS
+              CJO=87FF VJ=.51 M=.24
+              EG=1.115 XTI=3 FC=.5 BV=35)
*
.MODEL DSUB1N05 D        (CJO=203FF VJ=.51 M=.24)
.MODEL DSUB2N05 D        (CJO=388FF VJ=.51 M=.24)
.MODEL PNN05A NPN        (IS=1.662E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+              ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+              IKR=.7125MA ISC=1.803E-16 NC=1 RB=656.7 RBM=218
+              RE=0 RC=91.62
+              CJE=86.47FF VJE=.9 MJE=.4
+              CJC=58.32FF VJC=.53 MJC=.37
+              TF=40P XTF=0 VTF=100 ITF=3.89MA PTF=0
+              TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL PNN05B NPN        (IS=1.583E-16 BF=70 NF=1.008 VAF=30 IKF=10A
+              ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+              IKR=6.78MA ISC=1.717E-15 NC=1 RB=77.29 RBM=31.25
+              RE=0 RC=9.61
+              CJE=751.6FF VJE=.9 MJE=.4
+              CJC=445.2FF VJC=.53 MJC=.37
+              TF=40P XTF=0 VTF=100 ITF=37.1MA PTF=0
+              TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
```

```
.MODEL WN05 D            (IS=1.0578E-12 RS=37.6 N=1.044 TT=10PS
+              CJO=141.75FF VJ=.4 M=.33
+              EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS114 D        (IS=1E-16 RS=0 N=1 TT=500PS
+              CJO=2.75PF VJ=.51 M=.24
+              EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL QPS114 D          (IS=2.52E-12 RS=1.35 N=1.044 TT=10PS
+              CJO=2.1PF VJ=.4 M=.33
+              EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB025X D        (CJO=284FF VJ=.51 M=.24)
.MODEL PN025X NPN        (IS=4.32E-17 BF=113 NF=1.008 VAF=30 IKF=10A
+              ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+              IKR=10.85MA ISC=4.68E-16 NC=1 RB=175 RBM=65
+              RE=0 RC=35.2
+              CJE=193FF VJE=.9 MJE=.4
+              CJC=158FF VJC=.53 MJC=.37
+              TF=40P XTF=0 VTF=100 ITF=5.7MA PTF=0
+              TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL FP025X D          (IS=1.08E-13 RS=48.3 N=1.044 TT=10PS
+              CJO=90FF VJ=.4 M=.33
+              EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB025 D         (CJO=284FF VJ=.51 M=.24)
.MODEL PN025 NPN         (IS=2.45E-17 BF=113 NF=1.008 VAF=30 IKF=10A
+              ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+              IKR=1MA ISC=2.66E-16 NC=1 RB=193 RBM=89
+              RE=0 RC=62
+              CJE=123FF VJE=.9 MJE=.4
+              CJC=108FF VJC=.53 MJC=.37
+              TF=40P XTF=0 VTF=100 ITF=5.7MA PTF=0
+              TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL FP025 D           (IS=1.4E-13 RS=52 N=1.044 TT=10PS
+              CJO=117FF VJ=.4 M=.33
+              EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB139 D         (CJO=2.12PF VJ=.51 M=.24)
.MODEL PN139 NPN         (IS=1.03E-16 BF=113 NF=1.008 VAF=30 IKF=10A
+              ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+              IKR=4.4MA ISC=1.22E-16 NC=1 RB=117 RBM=47
+              RE=0 RC=8.41
+              CJE=493FF VJE=.9 MJE=.4
+              CJC=244FF VJC=.53 MJC=.37
+              TF=40P XTF=0 VTF=100 ITF=96.7MA PTF=0
+              TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL GR139 D           (IS=7E-14 RS=10 N=1.044 TT=10PS
+              CJO=88FF VJ=.4 M=.33
+              EG=.69 XTI=3 FC=.5 BV=30)
.MODEL GRS003 D          (IS=4.27E-14 RS=53 N=1.044 TT=10PS
+              CJO=54FF VJ=.4 M=.33
+              EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS003 D        (IS=1E-16 RS=0 N=1 TT=500PS
+              CJO=127FF VJ=.51 M=.24
+              EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL DSUB009E D        (CJO=106FF VJ=.51 M=.24)
.MODEL PN009E NPN        (IS=3.92E-16 BF=113 NF=1.008 VAF=30 IKF=10A
+              ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+              IKR=.3MA ISC=4.25E-15 NC=1 RB=185 RBM=39
+              RE=0 RC=3.9
+              CJE=1.37PF VJE=.9 MJE=.4
+              CJC=609FF VJC=.53 MJC=.37
+              TF=40P XTF=0 VTF=100 ITF=1.64MA PTF=0
+              TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL GR009E D          (IS=5.4E-13 RS=9.57 N=1.044 TT=10PS
+              CJO=683FF VJ=.4 M=.33
+              EG=.69 XTI=3 FC=.5 BV=30)
```

```
.MODEL DSUB108 D        (CJO=163FF VJ=.51 M=.24)
.MODEL PN108 NPN        (IS=1.75E-17 BF=113 NF=1.008 VAF=30 IKF=10A
+               ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+               IKR=.75MA ISC=1.9E-16 NC=1 RB=638.8 RBM=222
+               RE=0 RC=87
+               CJE=90.6FF VJE=.9 MJE=.4
+               CJC=50.3FF VJC=.53 MJC=.37
+               TF=40P XTF=0 VTF=100 ITF=4.1MA PTF=0
+               TR=200p XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL W108 D            (IS=5.1E-13 RS=58.8 N=1.044 TT=10PS
+               CJO=68.3FF VJ=.4 M=.33
+               EG=.69 XTI=3 FC=.5 BV=30)
```

ECL Transistor Models

```
.MODEL T05I1 NPN
+    IS=21.18E-18  BF=112   BR=5.108  RE=1.533   IKF=.0213 VAF=41.8
+    ISE=250E-18   RB=52.7  RBM=0     IRB=0     IKR=53E-5 VAR=3.766
+    ISC=95.62E-18 EG=1.11  RC=26.33  NC=1.141  NR=.997
+    CJE=67.7E-15  VJE=1.037 MJE=.5718 NF=1.000  XTI=4.7
+    CJC=99.5E-15  VJC=.603  MJC=.266  NE=2.000  XTB=1.15
+    CJS=152E-15   VJS=.5052 MJS=.3465 TR=9.92E-9 PTF=20
+    TF=35E-12     XTF=2.25  VTF=1.67  ITF=.00808 XCJC=.069 FC=.8
.MODEL TPNP2 PNP
+    IS=7.69E-17 BF=5 BR=1 RB=164 RC=56 CJE=.086E-12
+    CJC=1.4E-12
.MODEL T08I1 NPN
+    IS=33.33E-18  BF=114.5  BR=2.029  RE=1.333   IKF=.0336 VAF=42.7
+    ISE=1.0E-15   RB=56.6   RBM=0     IRB=0     IKR=.115  VAR=3.665
+    ISC=184.7E-18 EG=1.11   RC=22.86  NC=1.085  NR=.995
+    CJE=99.3E-15  VJE=1.037 MJE=.5718 NF=1.000  XTI=4.7
+    CJC=124.4E-15 VJC=.603  MJC=.266  NE=2.000  XTB=1.15
+    CJS=170.4E-15 VJS=.5052 MJS=.3465 TR=9.92E-9 PTF=40
+    TF=35E-12     XTF=2.25  VTF=1.67  ITF=.00808 XCJC=.089 FC=.8
.MODEL T12B1 NPN
+    IS=5.7E-17   BF=113   BR=1.116  RE=1.25    IKF=.0828  VAF=4
+    ISE=2.4E-15  RB=170   RBM=170   IRB=1.7E-3 IKR=.27    VAR=3.6
+    ISC=1.01E-16 EG=1.11  RC=13.3   NC=1.028   NR=1.019   XTI=3
+    CJE=15E-15   VJE=.658 MJE=.273  NF=1.000
+    CJC=27e-15   VJC=.603 MJC=.369  NE=2.000
+    CJS=101E-15  VJS=.429 MJS=.259  TR=5E-9
+    TF=39E-12    XTFf=3   VTF=1.4   ITF=.008  XCJC=.620  FC=.005
.MODEL T5406  NPN
+    IS=3.3E-16 BF=113  RB=86.6 BR=5
+    RC=23.6 RE=.833 CJE=.495E-12 CJC=.722E-12 CJS=.576E-12
```

Resistor Diode Model

```
.MODEL RES-DIODE D (IS=1E-16 TT=1NS VJ=.759V M=.333 CJO=50FF )
```

AN1404

ECLinPS™ Circuit Performance at Non-Standard VIH Levels

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This application note explains the consequences of driving an ECLinPS device with an input voltage HIGH level (V_{IH}) which does not meet the maximum voltage specified in the ECLinPS Databook.

ECLinPS Circuit Performance at Non-Standard VIH Levels

Introduction

When interfacing ECLinPS devices to various other technologies times arise where the the input voltages do not meet the specification limits outlined in the ECLinPS data book. The purpose of this document is to explain the consequences of driving an ECLinPS device with an input voltage HIGH level (V_{IH}) which does not meet the maximum voltage specified in the ECLinPS Databook.

The results outlined in this document should not be viewed as guarantees by Motorola but rather as representative information from which the reader can base design decisions. It is up to the reader to assess the risks of implementing the non-standard interface and deciding if that level of risk is acceptable for the system design. Motorola's guarantee on V_{IH} will continue to be the specification standards established for the 10H™ and 100K ECL technologies.

Overview

The upper end of the V_{IH} spec of an ECLinPS, or any other ECL, input is limited by saturation affects of the input transistor. Figure 1 below illustrates a typical ECL input (excluding pulldown resistors and ESD structures); the structure is a basic differential amplifier configuration. With a logic HIGH level asserted at the input the collector of that transistor will be pulled down below the V_{CC} rail by the gate current passing through the collector load resistor. The voltage at the collector of the input transistor (V_C) will be dependent on the gate current and the size of the collector load resistor associated with the input gate.

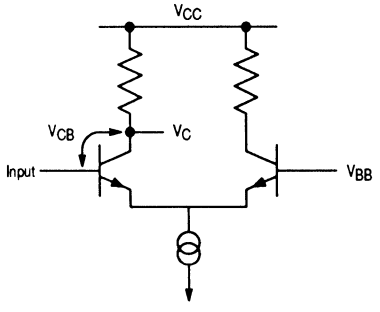


Figure 1. Typical ECLinPS Input Structure

As the input V_{IH} increases towards V_{CC} the collector base junction of the input transistor becomes forward biased; as this forward bias condition increases the transistor will move into the saturation region. The value of V_{CB} at which the transistor begins to saturate is process dependent and will vary from logic family to logic family. Fortunately the MOSAIC III process used to implement the ECLinPS family incorporates a deep n+ collector doping. This deep collector helps to mitigate the effects of saturation of transistors by requiring a larger collector-base forward bias to enter the saturation region.

V_{IH}max and the ECLinPS Family

As previously mentioned the MOSAIC III™ process allows for ECLinPS devices to operate at V_{IH}max levels somewhat higher than those specified in the databook, however the exact value of V_{IH} for which saturation problems will occur varies from device to device and even among different inputs for a given device. This variation is a result of the different input configurations used on the various inputs of ECLinPS devices.

The easiest way to define an acceptable V_{IH}max for each device in the family is to define at what point the input transistor will saturate and specify for each input what the worst case input transistor collector voltage will be. With this information designers will be able to determine on a part by part, input by input basis what input voltage levels will be acceptable for their application.

Simulation Results

The input saturation phenomenon was characterized through SPICE simulations and the results will be reported in the following text. For simplicity of simulation a buffer similar to the E122 was used. Since the outputs of this buffer drive off chip, the V_{IH}max performance of this structure will be worse than the typical input structure. Both a 100K and a 10H style buffer were analyzed to note any discrepancies between the two standards. As expected the simulation results showed no difference in the saturation susceptibility of a 100K versus a 10H style buffer. Therefore the simulation results of only the 100K style buffer will be presented to minimize redundancy of information.

The following text will refer to Figures 4–8 in the appendix of this document. Figures 4–8 are graphical plots of the input and output waveforms of an E122 style buffer (structure similar to that of Figure 1) for various V_{IH} levels. V(in) represents the input voltage while V(q) and V(qb) represent the output voltages. The V(vbb) line was included for measurement purposes only and will be ignored.

Figure 4 represents the "standard" operation of the device as a standard V_{IH} input was used. Note that in this condition the propagation delays measure in the 215–225ps range and the I_{INH} was 42.5μA. The I_{INH} of this device is simply a measure of the base current of the input transistor when that transistor is conducting current. We will be monitoring both of these conditions as well as any degradation in the output waveforms as a sign of the input transistor becoming saturated. As can be seen in Figures 5 and 6 none of the parameters change for V_{IH} levels of up to –0.4V. With a collector voltage, V_C, of ~1.0V these V_{IH}'s correspond to a collector base forward bias of 600mV. As the V_{IH} of the input moves closer to V_{CC}, Figures 7 and 8, three phenomena start to occur: the I_{INH} increases, the delays increase and significant changes occur to the output low level of the QB pin.

In Figure 7 the I_{INH} of the input transistor has more than doubled from the "standard" level. This increase in base current leads to an increase in the V_{OL} level as the collector

current must reduce to maintain the constant emitter current. As the collector current reduces, the IR drop across the collector load resistor reduces, thus raising the V_{OL} level on the QB output. Although the V_{OL} level has shifted the overall propagation delay has remained essentially unchanged.

Finally, when the input is switched all the way up to V_{CC} the V_{OL} level no longer remains in spec as the input base current has jumped to almost 1ma and there has been significant degradation in the high-low propagation delay. It is apparent that for this condition an E122 style buffer will not perform adequately for most systems.

From this information it can be concluded that for a collector-base forward bias of ≤600mV there will be no adverse conditions on the performance of the device. The performance starts to degrade with further forward bias until at a forward bias voltage of ≈1.0V the device will fail both its DC and AC specifications.

ECLinPS Input Structures

There are four basic input structures which will affect the V_{IH}max performance of ECLinPS devices. The four structures are as follows: an internal buffer, an external buffer, an emitter follower input buffer and a series gated emitter follower input.

The internal buffers are input structures whose outputs drive other gates internal to the device, the voltage swings of the input transistor collectors (V_C) on these devices will be ≈800mV. An external buffer is one in which the outputs are fed external to the chip. Because of the relatively large base drive of the output emitter follower for these structures the V_C voltage will typically be a couple hundred milivolts lower than for the internal buffer. Note that because of the larger output swings of a 10E device, a 10E style external buffer will require a V_{IH}max input level more near the specified value. Both of these structures are similar to that pictured in Figure 1.

The third and fourth structures are somewhat different in design than the first two. Figure 2 illustrates an emitter follower input structure. For the basic emitter follower input the input voltages are dropped by an additional V_{BE} (≈800mV) before they are fed into the differential amplifier input gate. The switching reference is also shifted down by one diode drop to remain centered in the input swing. Obviously this input structure will represent the "best case" in the area of extended V_{IH}max performance. In fact this type of input structure will allow for input voltages even several hundred millivolts above the V_{CC} rail. This characteristic makes these type devices ideal for interfacing with differential oscillators whose outputs lack any DC offset. In the emitter follower structure the limiting factor will be the saturation of the emitter follower device whose collector is at V_{CC}. From the previous simulation results this would suggest a maximum V_{IH} of +0.6V.

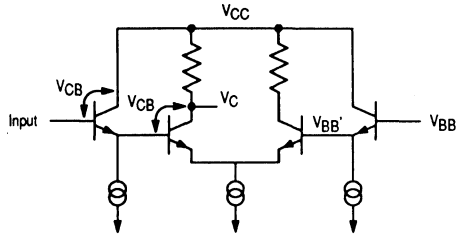


Figure 2. Emitter Follower Input Structure

The series gate emitter follower input will represent the absolute worst case situation for a 100E device. Figure 3 represents a series gate emitter follower input for a 10E and a 100E device. From this figure it is apparent that the lower switching level (B input level) is going to be much more susceptible to V_{IH}max for the 100E device than the 10E device. The two diode drops used for the 10E device is not possible for a 100E device due to the smaller V_{EE} voltage of a 100E device.

To summarize the external gate will represent the worst case V_{IH}max situation for a 10E device while the series gate emitter follower case will represent worst case for a 100E device. In either situation the standard emitter follower will allow the most leeway for non-standard V_{IH}max performance.

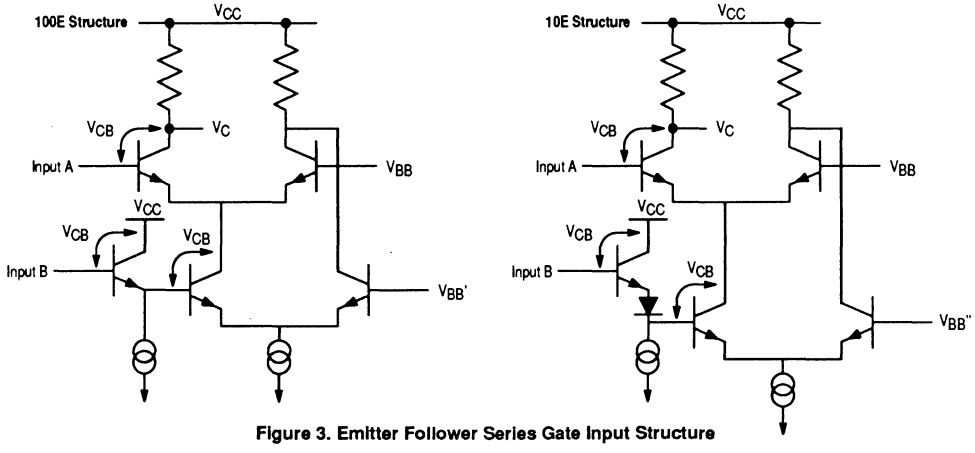


Figure 3. Emitter Follower Series Gate Input Structure

Other Considerations

When driving ECLinPS devices with other than standard input levels there is another phenomena that should be considered; namely effects of non-centered switching references on the AC performance of a device. For non-standard input voltages the midpoint of the voltage swing may not correspond to the internal V_{BB} switching reference. If this is the case the resulting AC variation should be included in the evaluation of a design.

An input voltage swing not centered about the switching reference will exhibit a delay skew between the two input edge transitions. The size of this skew will be dependent on both the voltage offset of the reference voltage and the midpoint of the input swing and the slew rate of the input as it passes through the threshold region. As an example for the case in which the V_{IH} = –0.5V and the V_{IL} remains at –1.7V the midpoint of the swing will be at –1.1V versus a –1.32V V_{BB} reference. With a typical slew rate of 1ps/mV for ECLinPS type edge rates the rising input edge delay will be 220ps longer than normal and the falling edge delay will be 220ps faster. This results in a 440ps skew between the two input transitions that would not be seen for an ideal switching reference.

The only means of correcting this skew is to lower the V_{IL} level to recenter the swing or provide a different switching reference for the device. The latter can be accomplished by buffering the signal with a differential input device with one input tied to an externally generated switching reference. Raising the V_{IL} level is not recommended due to the obvious loss of low end noise margin accompanied by any such shift.

Conclusions

Simulations show that forward bias levels of ≤600mV on the input transistor will keep the input transistor in the active region and the performance of the device will not be compromised. This forward bias voltage can be increased with varying degrees of performance degradation to levels somewhat higher than 600mV. Initial effects will be an increase in the I_{INH} current and a decrease in the output V_{OL} level on the QB output of the input gate. As the forward bias increases further the propagation delays through the device will be adversely affected.

The following example will outline the use of the table in the appendix to analyze the potential performance of a design using non-standard V_{IH} levels. If a design called for the 10E112 and the 10E416 to be driven by a –0.2V input signal a designer would want to know if these two devices would perform to specifications under these conditions. From the table the worst case collector voltage V_C would be –1.05V and 0.0V respectively. Subtracting these values from –0.2V yields forward bias voltages of 850mV and –200mV respectively. From this information the designer would conclude that the 10E416 will function with no problems however the 10E112 could suffer performance degradation under these same conditions.

The device information contained in the appendix of this document will provide designers with all of the information necessary to evaluate the input transistor forward bias conditions for all of the ECLinPS devices for different input voltages. With these numbers and the information provided in this document designers will be able to make informed decisions about their designs to meet the performance desired at an acceptable level of risk.

Appendix

Device	Input	Input Structure	V_C (10E Typical) (V)	V_C (10E Worst Case) (V)	V_C (100E Typical) (V)	V_C (100E Worst Case) (V)
E016	All	INT	–0.80	–0.90	–0.80	–0.90
E101	All	EF	–0.15	–0.25	–0.10	–0.20
E104/107	Dna	EXT	–0.95	–1.05	–0.90	–1.00
	Dnb	SG	–0.50	–0.60	–1.20	–1.30
E111	All	INT	–0.80	–0.90	–0.80	–0.90
E112	Dn	EXT	–0.95	–1.05	–0.90	–1.00
	EN/	INT	–0.80	–0.90	–0.80	–0.90
E116	All	EXT	–0.95	–1.05	–0.90	–1.00
E122	All	EXT	–0.95	–1.05	–0.90	–1.00
E131	D	INT	–0.90	–1.00	–0.90	–1.00
	Other	SG	–0.50	–0.60	–1.20	–1.30
E141	All	INT	–0.80	–0.90	–0.80	–0.90
E142	All	INT	–0.80	–0.90	–0.80	–0.90
E143	All	INT	–0.80	–0.90	–0.80	–0.90
E150	Dn	EXT	–0.95	–1.05	–0.90	–1.00
	Other	INT	–0.80	–0.90	–0.80	–0.90
E151	All	INT	–0.80	–0.90	–0.80	–0.90
E154	All	INT	–0.80	–0.90	–0.80	–0.90
E155	All	INT	–0.80	–0.90	–0.80	–0.90
E156	All	INT	–0.80	–0.90	–0.80	–0.90
E157	Dn	EXT	–0.95	–1.05	–0.90	–1.00
	SEL	INT	–0.80	–0.90	–0.80	–0.90
E158	Dn	EXT	–0.95	–1.05	–0.90	–1.00
	SEL	INT	–0.80	–0.90	–0.80	–0.90
E160	R, CLK	SG	–0.50	–0.60	–1.20	–1.30
	Other	INT	–0.80	–0.90	–0.80	–0.90
E163	All	INT	–0.80	–0.90	–0.80	–0.90
E164	All	INT	–0.80	–0.90	–0.80	–0.90
E166	All	INT	–0.80	–0.90	–0.80	–0.90
E167	All	INT	–0.80	–0.90	–0.80	–0.90
E171	All	INT	–0.80	–0.90	–0.80	–0.90
E175	All	INT	–0.80	–0.90	–0.80	–0.90
E195	All	INT	–0.80	–0.90	–0.80	–0.90
E196	All	INT	–0.80	–0.90	–0.80	–0.90
E212	All	INT	–0.80	–0.90	–0.80	–0.90
E241	All	INT	–0.80	–0.90	–0.80	–0.90
E256	All	INT	–0.80	–0.90	–0.80	–0.90
E336	All	INT	–0.80	–0.90	–0.80	–0.90
E337	All	INT	–0.80	–0.90	–0.80	–0.90
E404	All	EF	0.00	0.00	0.00	0.00
E416	All	EF	0.00	0.00	0.00	0.00
E431	All	INT	–0.80	–0.90	–0.80	–0.90
E451	All	INT	–0.80	–0.90	–0.80	–0.90
E452	All	INT	–0.80	–0.90	–0.80	–0.90
E457	Dn	EF	0.00	0.00	0.00	0.00
	SEL	INT	–0.80	–0.90	–0.80	–0.90

INT = Internal Gate; EXT = External Gate; EF = Emitter Follower Input; SG = Series Gated Input

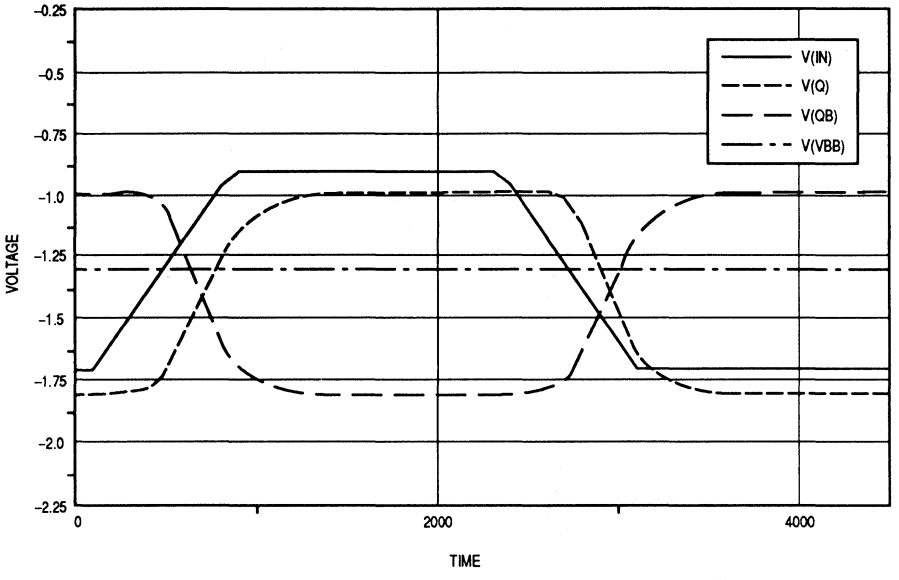


Figure 4. Input and Output Waveforms for V_{IH} = –0.9
(V_{OL} = –1.8; T_{PD++} = 215ps; T_{PD--} = 225ps; I_{INH} = 42.5µA)

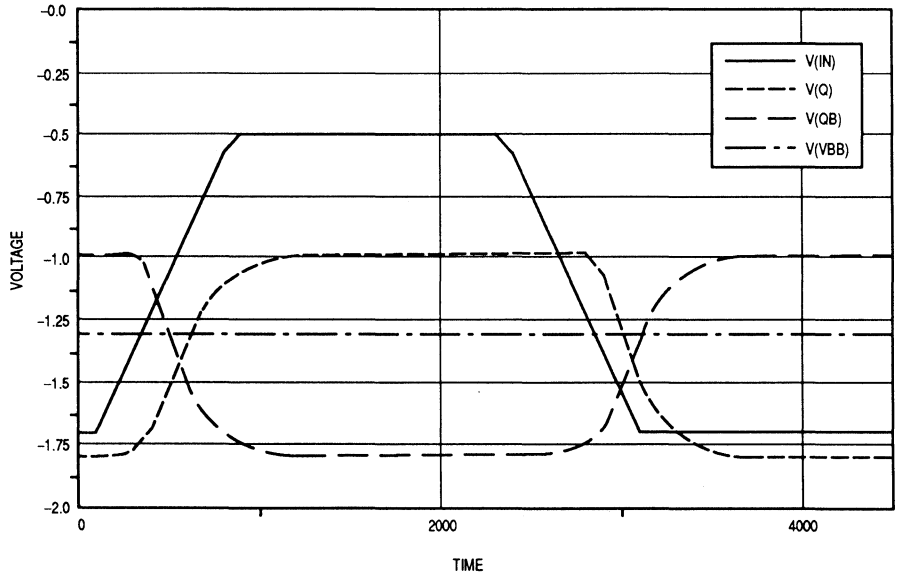


Figure 5. Input and Output Waveforms for V_{IH} = –0.5
(V_{OL} = –1.8; T_{PD++} = 204ps; T_{PD--} = 207ps; I_{INH} = 43.4µA)

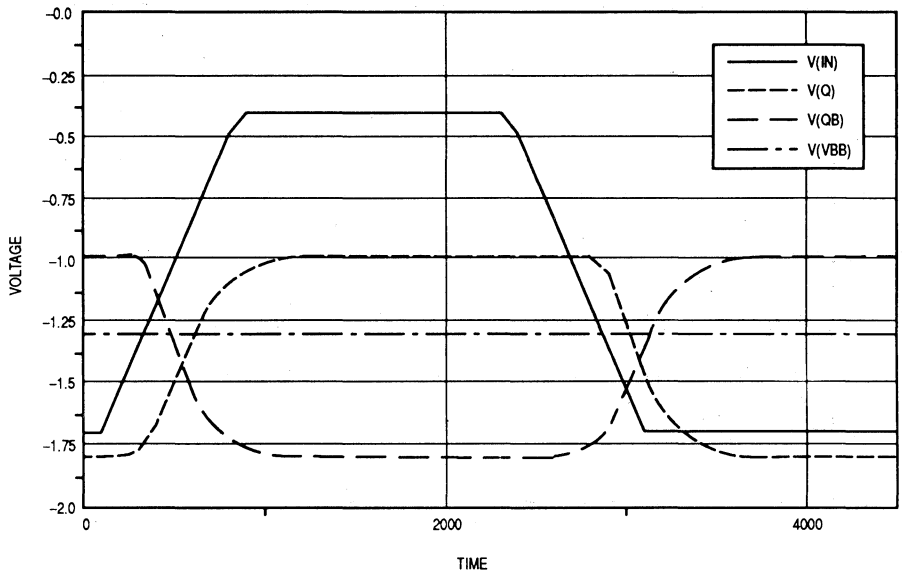


Figure 6. Input and Output Waveforms for V_{IH} = –0.4
(V_{OL} = –1.8; T_{PD++} = 201ps; T_{PD--} = 206ps; I_{INH} = 46.7µA)

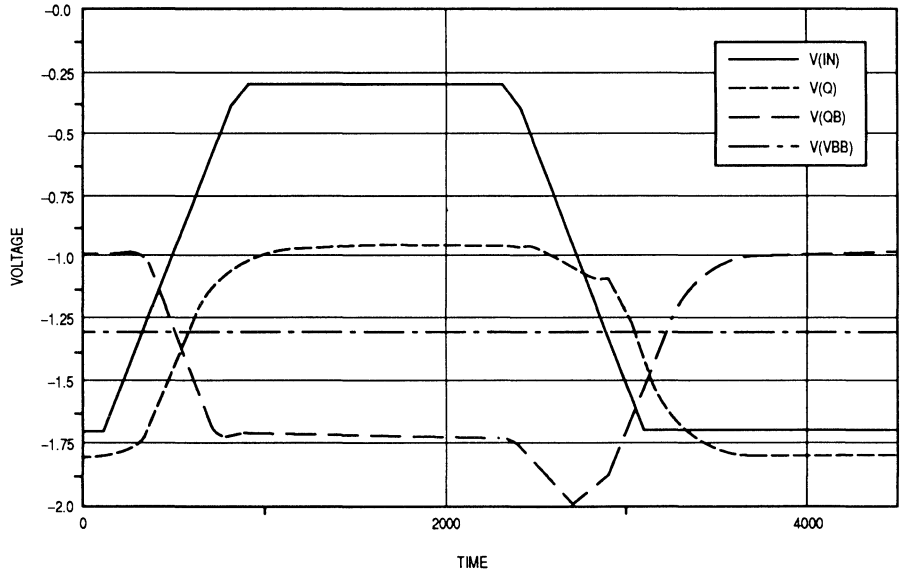


Figure 7. Input and Output Waveforms for V_{IH} = –0.3
(V_{OL} = –1.8; T_{PD++} = 196ps; T_{PD--} = 198ps; I_{INH} = 114.8µA)

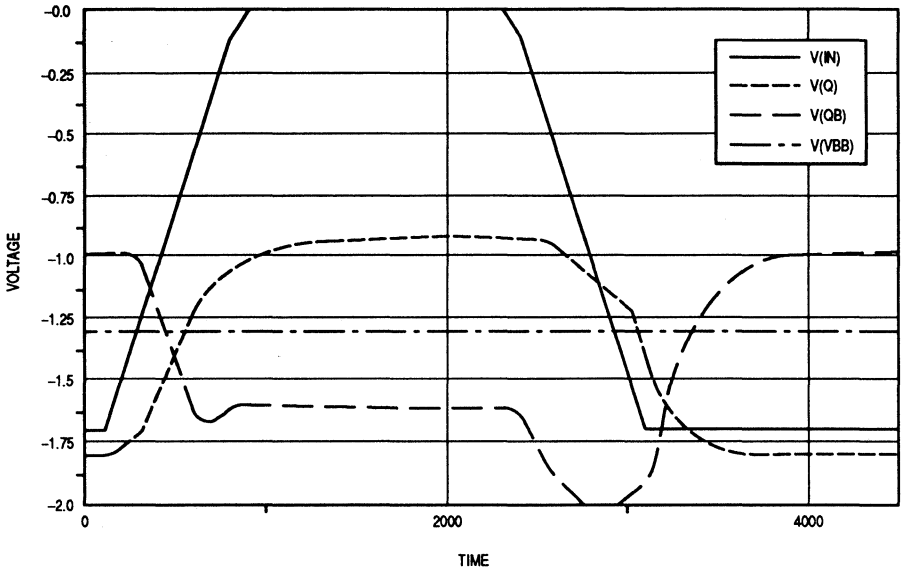


Figure 8. Input and Output Waveforms for V_{IH} = 0.0
(V_{OL} = −1.8; T_{PD++} = 196ps; T_{PD--} = 287ps; I_{INH} = 912μA)

AN1405

ECL Clock Distribution Techniques

Prepared by
Todd Pearson
ECL Applications Engineering

This application note provides information on system design using ECL logic technologies for reducing system clock skew over the alternative CMOS and TTL technologies.

ECL Clock Distribution Techniques

INTRODUCTION

The ever increasing performance requirements of today's systems has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions within a system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or more costly, faster logic. ECL logic technologies offer a number of advantages for reducing system clock skew over the alternative CMOS and TTL technologies.

SKEW DEFINITIONS

The skew introduced by logic devices can be divided into three parts: duty cycle skew, output-to-output skew and part-to-part skew. Depending on the specific application, each of the three components can be of equal or overriding importance.

Duty Cycle Skew

The duty cycle skew is a measure of the difference between the T_{PLH} and T_{PHL} propagation delays (Figure 1). Because differences in T_{PLH} and T_{PHL} will result in pulse width distortion the duty cycle skew is sometimes referred to as pulse skew. Duty cycle skew is important in applications where timing operations occur on both edges or when the duty cycle of the clock signal is critical. The later is a common requirement when driving the clock inputs of advanced microprocessors.

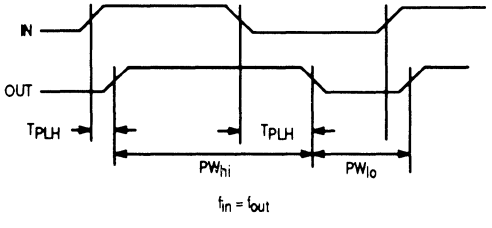


Figure 1. Duty Cycle Skew

Output-to-Output Skew

Output-to-output skew is defined as the difference between the propagation delays of all the outputs of a device. A key constraint on this measurement is the requirement that the output transitions are identical, therefore if the skew between all edges produced by a device is important the output-to-output skew would need to be added to the duty cycle skew to get the total system skew. Typically the output-to-output skew will be smaller than the duty cycle skew for TTL and CMOS devices. Because of the near zero duty cycle skew of a differential ECL device the output-to-output skew will generally be larger. The output-to-output skew is important in systems where either a single device can provide all of the necessary clocks or for the first level device of a nested clock distribution tree. In these two situations the only parameter of importance will be the relative position of each output with respect to the other outputs on that die. Since these outputs will all see the same environmental and process conditions the skew will be significantly less than the propagation delay windows specified in the standard device data sheet.

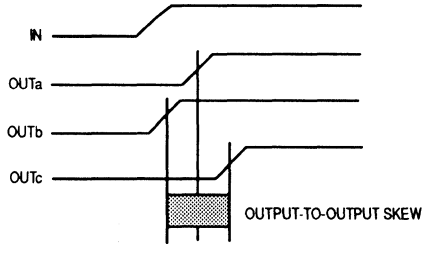


Figure 2. Output-to-Output Skew

Part-to-Part Skew

The part-to-part skew specification is by far the most difficult performance aspect of a device to minimize. Because the part-to-part skew is dependent on both process variations and variations in the environment the resultant specification is significantly larger than for the other two components of skew. Many times a vendor will provide subsets of part-to-part skew specifications based on non-varying environmental conditions. Care should be taken in reading data sheets to fully understand the conditions under which the specified limits are guaranteed. If the part-to-part skew is specified and is different than the specified propagation delay window for the device one can be assured there are constraints on the part-to-part skew specification.

Power supply and temperature variations are major contributors to variations in propagation delays of silicon devices. Constraints on these two parameters are commonly seen in part-to-part skew specifications. Although there are situations where the power supply variations could be ignored, it is difficult for this author to perceive of a realistic system whose devices are all under identical thermal conditions. Hot spots on boards or cabinets, interruption in air flow and variations in IC density of a board all lead to thermal gradients within a system. These thermal gradients will guarantee that devices in various parts of the system are under different junction temperature conditions. Although it is unlikely that a designer will need the entire commercial temperature range, a portion of this range will need to be considered. Therefore, a

part-to-part skew specified for a single temperature is of little use, especially if the temperature coefficient of the propagation delay is relatively large.

For designs whose clock distribution networks lie on a single board which utilizes power and ground planes an assumption of non-varying power supplies would be a valid assumption and a specification limit for a single power supply would be valuable. If, however, various pieces of the total distribution tree will be on different boards within a system there is a very real possibility that each device will see different power supply levels. In this case a specification limit for a fixed V_{CC} will be inadequate for the design of the system. Ideally the data sheets for clock distribution devices should include information which will allow designers to tailor the skew specifications of the device to their application environment.

SYSTEM ADVANTAGES OF ECL

Skew Reductions

ECL devices provide superior performance in all three areas of skew over their TTL or CMOS competitors. A skew reducing mechanism common to all skew parameters is the faster propagation delays of ECL devices. Since, to some extent, all skew represent a percentage of the typical delays faster delays will usually mean smaller skews. ECL devices, especially clock distribution devices, can be operated in either single-ended or differential modes. To minimize the skew of these devices the differential mode of operation should be used, however even in the single-ended mode the skew performance will be significantly better than for CMOS or TTL drivers.

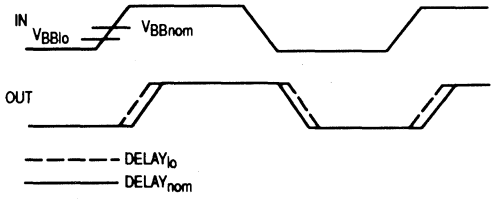


Figure 3. V_{BB} Induced Duty Cycle Skew

ECL output buffers inherently show very little difference between T_{PLH} and T_{PHL} delays. What differences one does see are due mainly to switching reference levels which are not ideally centered in the input swing (see Figure 3). For worst case switching reference levels the pulse skew of an ECL device will still be less than 300ps. If the ECL device is used differentially the variation in the switching reference will not impact the duty cycle skew as it is not used. In this case the pulse skew will be less than 50ps and can generally be ignored in all but the highest performance designs. The problem of generating clocks which are capable of meeting the duty cycle requirements of the most advanced microprocessors, would be a trivial task if differential ECL compatible clock inputs were used. TTL and CMOS clock drivers on the other hand have inherent differences between the T_{PLH} and T_{PHL} delays in addition to the problems with non-centered switching thresholds. In devices specifically designed to minimize this parameter it generally cannot be guaranteed to anything less than 1ns.

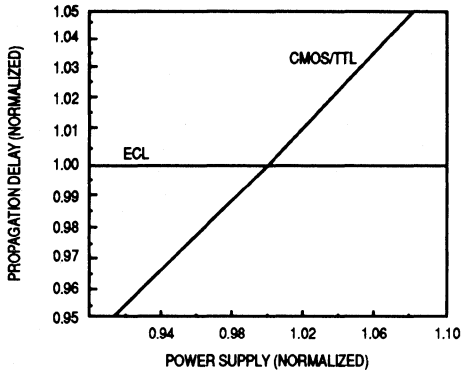
The major contributors to output-to-output skew is IC layout and package choice. Differences in internal paths and paths through the package generally can be minimized regardless of the silicon technology utilized at the die level, therefore ECL devices offer less of an advantage in this area than for other skew parameters. CMOS and TTL output performance is tied closely to the power supply levels and the stability of the power busses within the chip. Clock distribution trees by definition always switch simultaneously, thus creating significant disturbances on the internal power busses. To alleviate this problem multiple power and ground pins are utilized on TTL and CMOS clock distribution devices. However even with this strategy TTL and CMOS clock distribution devices are limited to 500ps – 700ps output-to-output skew guarantees. With differential ECL outputs very little if any noise is generated and coupled onto the internal power supplies. This coupled with the faster propagation delays of the output buffers produces output-to-output skews on ECL clock chips as low as 50ps.

Two aspects of ECL clock devices will lead to significantly smaller part-to-part skews than their CMOS and TTL competitors: faster propagation delays and delay insensitivity to environmental variations. Variations in propagation delays with process are typically going to be based on a percentage of the typical delay of the device. Assuming this percentage is going to be approximately equivalent between ECL, TTL and CMOS processes, the faster the device the smaller the delay variations. Because state-of-the-art ECL devices are at least 5 times faster than TTL and CMOS devices, the expected delay variation would be one fifth those of CMOS and TTL devices without even considering environmental dependencies.

The propagation delays of an ECL device are insensitive to variations in power supply while CMOS and TTL device propagation delays vary significantly with changes in this parameter. Across temperature the percentage variation for all technologies is comparable, however, again the faster propagation delays of ECL will reduce the magnitude of the variation. Figure 4 on the following page represents normalized propagation delay versus temperature and power supply for the three technologies.

Low Impedance Line Driving

The clock requirements of today's systems necessitate an almost exclusive use of controlled impedance interconnect. In the past this requirement was unique to the performance levels associated with ECL technologies, and in fact precluded its use in all but the highest performance systems. However the high performance CMOS and TTL clock distribution chips now require care in the design and layout of PC boards to optimize their performance, with this criteria established the migration from these technologies to ECL is simplified. In fact, the difficulties involved in designing with these "slower" technologies in a controlled impedance environment may even enhance the potential of using ECL devices as they are ideally suited to the task.



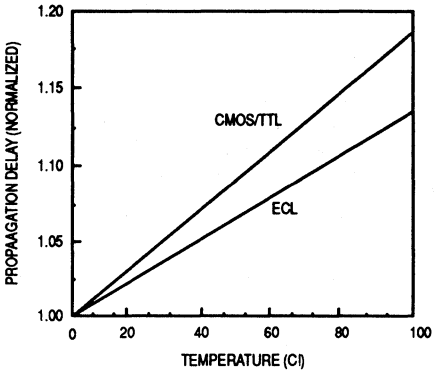


Figure 4. T_{PD} vs Environmental Condition Comparison

The low impedance outputs and high impedance inputs of an ECL device are ideal for driving 50Ω to 130Ω controlled impedance transmission lines. The specified driving impedance of ECL is 50Ω, however this value is used only for convenience sake due to the 50Ω impedance of most commonly used measurement equipment. Utilizing higher impedance lines will reduce the power dissipated by the termination resistors and thus should be considered in power sensitive designs. The major drawback of higher impedance lines (delays more dependent on capacitive loading) may not be an issue in the point to point interconnect scheme generally used in low skew clock distribution designs.

Differential Interconnect

The device skew minimization aspects of differential ECL have already been discussed however there are other system level advantages that should be mentioned. Whenever clock lines are distributed over long distances the losses in the line and the variations in power supply upset the ideal relationship between input voltages and switching thresholds. Because differential interconnect "carries" the switching threshold information from the source to the load the relationship between the two is less likely to be changed. In addition for long lines the smaller swings of an ECL device produce much lower levels of cross-talk between adjacent lines and minimizes EMI radiation from the PC board.

There is a cost associated with fully differential ECL, more pins for equivalent functions and more interconnect to be laid on a typically already crowded PC board. The first issue is really a non-issue for clock distribution devices. The output-to-output and duty cycle skew are very much dependent on quiet internal power supplies. Therefore the pins sacrificed for the complimentary outputs would otherwise have to be used as power supply pins, thus functionality is actually gained for an equivalent pin count as the inversion function is also available on a differential device. The presence of the inverted signal could be invaluable for a design which clocks both off the positive and negative edges. Figure 5 shows a method of obtaining very low skew (<50ps) 180° shifted two phase clocks.

It is true that differential interconnect requires more signals to be routed on the PC board. Fortunately with the wide data and address buses of today's designs the clock lines represent a small fraction of the total interconnect. The final choice as to whether or not to use differential interconnect lies in the level of skew performance necessary for the design. It should be noted that although single-ended ECL provides less attractive skew performance than differential ECL, it does provide significantly better performance than equivalent CMOS and TTL functions.

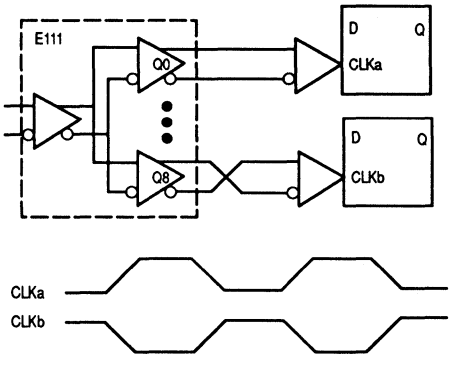


Figure 5. 180° Shifted Two Phase Clocks

USING ECL WITH POSITIVE SUPPLIES

It is hard to argue with the clock distribution advantages of ECL presented thus far, but it may be argued that except for all ECL designs it is too costly to include ECL devices in the distribution tree. This claim is based on the assumption that at least two extra power supplies are required; the negative V_{EE} supply and the negative V_{TT} termination voltage. Fortunately both these assumptions are false. PECL (Positive ECL) is an acronym which describes using ECL devices with a positive rather than negative power supply. It is important to understand that all ECL devices are also PECL devices. By

using ECL devices as PECL devices on a +5 volt supply and incorporating termination techniques which do not require a separate termination voltage (series termination, thevenin equivalent) ECL can be incorporated in a CMOS or TTL design with no added cost.

The reason for the choice of negative power supplies as standard for ECL is due to the fact that all of the output levels and internal switching bias levels are referenced to the V_{CC} rail. It is generally easier to keep the grounds quieter and equal potential throughout a system than it is with a power supply. Because the DC parameters are referenced to the V_{CC} rail any disturbances or voltage drops seen on V_{CC} will translate 1:1 to the output and internal reference levels. For this reason when communicating with PECL between two boards it is recommended that only differential interconnect be used. By using differential interconnect V_{CC} variations within the specified range will not in any way affect the performance of the device.

Finally mentioning ECL to a CMOS designer invariably conjures up visions of space heaters as their perception of ECL is high power. Although it is true that the static power of ECL is higher than for CMOS the dynamic power differences between the technologies narrows as the frequency increases. As can be seen in Figure 6 at frequencies as low as 20MHz the per gate power of ECL is actually less than for CMOS. Since clock distribution devices are never static it does not make sense to compare the power dissipation of the two technologies in a static environment.

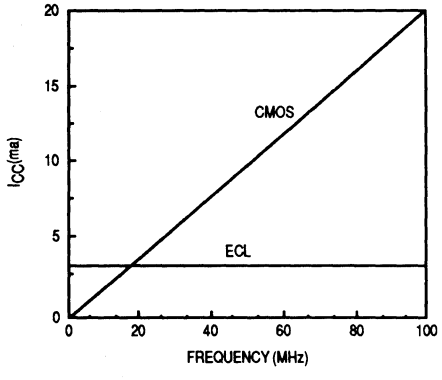


Figure 6. ICC/Gate vs Frequency Comparison

MIXED SIGNAL CLOCK DISTRIBUTION

ECL Clock Distribution Networks

Clock distribution in a ECL system is a relatively trivial matter. Figure 7 illustrates a two level clock distribution tree which produces nine differential ECL clocks on six different cards. The ECLinPS E211 device gives the flexibility of disabling each of the cards individually. In addition the synchronous registered enables will disable the device only when the clock is already in the LOW state, thus avoiding the problem of generating runt pulses when an asynchronous disable is used. The device also provides a muxed clock input for incorporating a high speed system clock and a lower speed test or scan clock within the same distribution tree. The ECLinPS E111 device is used to receive the signals from the backplane and distribute it on the card. The worst case skew between all 54 clocks in this situation would be 275ps assuming that all the loads and signal traces are equalized.

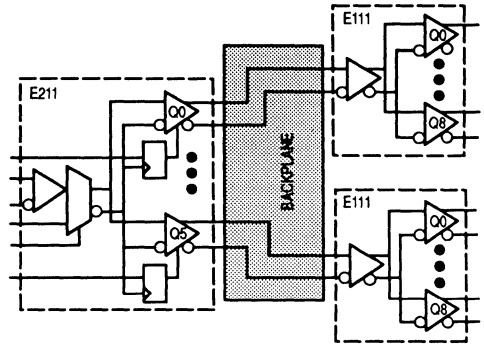


Figure 7. ECL Clock Distribution Tree

Mixed Technology Distribution Networks

Building clock networks in TTL and CMOS systems can be a little more complicated as there are more alternatives available. For simple one level distribution trees fanout devices like the MECL 10H645 1:9 TTL to TTL fanout tree can be used. However as the number of levels of fanout increases the addition of ECL devices in an other wise TTL or CMOS system becomes attractive. In Figure 8 on the next page an E111 device is combined with a MECL H641 device to produce 81 TTL level clocks. Analyzing the skew between the 81 clocks yields a worst case skew, allowing for the full temperature and V_{CC} range variation, of 1.25ns. Under ideal situations, no variation in temperature or V_{CC} supply, the skew would be only 750ps. When compared with distribution trees utilizing only TTL or CMOS technologies these numbers represent ≈50% improvement, more if the environmental conditions vary to any degree. For a 50MHz clock the total skew between the 81 TTL clocks is less than 6.5% of the clock period, thus providing the designer extra margin for layout induced skew to meet the overall skew budget of the design.

Many designers have already realized the benefits of ECL clock distribution trees and thus are implementing them in their designs. Furthermore where they have the capability, i.e. ASICs, they are building their VLSI circuits with ECL compatible clock inputs. Unfortunately other standard VLSI circuits such as microprocessors, microprocessor support chips and memory still cling to TTL or CMOS clock inputs. As a result many systems need both ECL and TTL clocks within the same system. Unlike the situation outlined in Figure 8 the ECL levels are not merely intermediate signals but rather are driving the clock inputs of the logic. As a result the ECL edges need to be matched with the TTL edges as pictured in Figure 9.

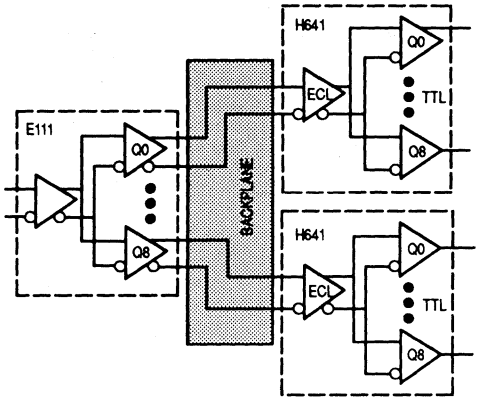


Figure 8. ECL to TTL Clock Distribution

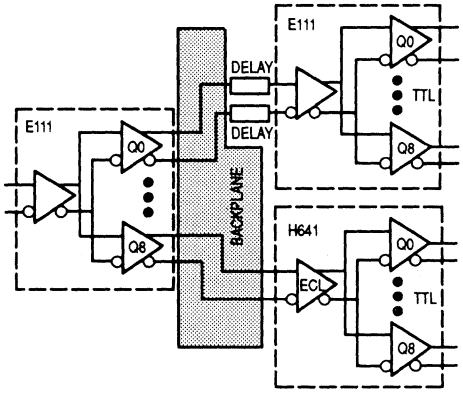


Figure 9. Mixed ECL and TTL Distribution

An ECL clock driver will be significantly faster than a TTL or CMOS equivalent function. Therefore to de-skew the ECL and TTL signals of Figure 9 a delay needs to be added to the input of the ECL device. Because a dynamic delay adjust would not lend itself to most production machines a static delay would be used. The value of the delay element would be a best guess estimate of the differences in the two propagation delays. It is highly unlikely that the temperature coefficients of the propagation delays of the ECL devices, TTL devices and delay devices would be equal. Although these problems will add skew to the system, the resultant total skew of the distribution network will be less than if no ECL chips were used.

PLL Based Clock Drivers

A potential solution for the problem outlined in Figure 9 is in the use of phase locked loop based clock distribution chips. Because these devices feedback an output and lock it to a reference clock input the delay differences between the various technology output buffers will be eliminated. One might believe that with all of the euphoria surrounding the performance of PLL based clock distribution devices that the need for any ECL in the distribution tree will be eliminated. However when analyzed further the opposite appears to be the case.

For a single board design with a one level distribution system there obviously is no need for ECL. When, however, a multiple board system is required where nested levels of devices are needed ECL once again becomes useful. One major aspect of part-to-part skew for PLL based clock chips often overlooked is the dependence on the skew of the various reference clocks being locked to. As can be seen in Figure 10 the specified part-to-part skew of the device would necessarily need to be added to the reference clock skew to get the overall skew of the clock tree. From the arguments presented earlier this skew will be minimized if the reference clock is distributed in ECL. It has not been shown as of yet where a PLL based ECL clock distribution chip can provide the skew performance of the simple fanout buffer. From a system standpoint the buffer type circuits are much easier to design with and thus given equivalent performance would represent the best alternative. The extra features provided by PLL based chips could all be realized if they were used in only the final stage of the distribution tree.

Unfortunately none of the PLL based devices available today feature differential ECL compatible reference clock inputs. Look for BiCMOS based PLL clock devices from Motorola in the near future. There will be a family of devices featuring various technology compatible inputs and outputs to allow for the building of precisely aligned clock trees based on either ECL, TTL or CMOS (or a mixture of all three) compatible levels.

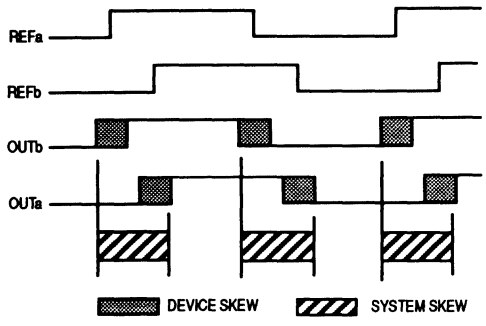


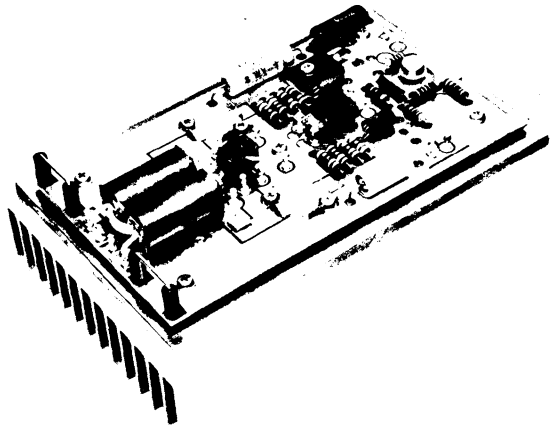
Figure 10. System Skew For PLL Clock Distribution

Conclusion

The best way to maximize the performance of any synchronous system is to spend the entire clock period performing value added operations. Obviously any portion of the clock period spent idle due to clock skew limits the potential performance of the system. Using ECL technology devices in clock distribution networks will minimize all aspects of skew and thus maximize the performance of a system. Unfortunately the VLSI world is not yet ECL clock based so that the benefits of a totally ECL based distribution tree cannot be realized for many systems. However there are methods of incorporating ECL into the intermediate levels of the tree to significantly reduce the overall skew. In addition the system designers can utilize their new found knowledge to incorporate ECL compatible clocks on those VLSI chips of which they have control while at the same time pressuring other VLSI vendors in doing the same so that future designs can enjoy fully the advantages of distributing clocks with ECL.

EB27A

Get 300 watts PEP Linear Across 2 to 30MHz from this Push-Pull Amplifier

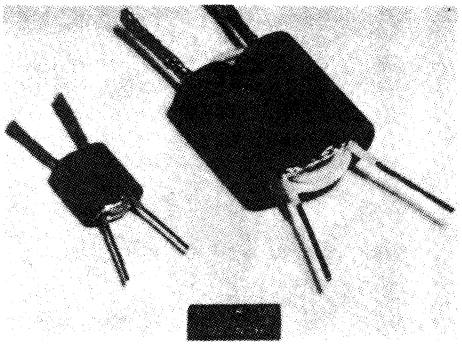


(The heat sink shown with amplifier is sufficient only for short test periods under forced air cooling.)

This bulletin supplies sufficient information to build a push-pull linear amplifier for 300 watts of PEP or CW output power across the 2- to 30-MHz band. One of Motorola's new high-power transistors developed for single-sideband, MRF422, is used in this application.

Like all transistors in its family of devices, MRF422 combines single-chip construction that is advancing the state-of-the-art, and improved packaging to accommodate the low collector efficiencies encountered in class B operation. Rated maximum output power is 150 watts CW or PEP with intermodulation distortion spec'd at −30 dB maximum, −33 dB typical. Although not recommended, a saturated power level of 240- to 250-W is achievable. Maximum allowable dissipation is 300 W at 25°C.

Because of its excellent load and line voltage regulating capabilities, an integrated circuit bias regulator is used in the amplifier. The MPC1000, originally described in this bulletin, consisted of a MC1723 chip and a built-in pass transistor. The manufacture of this device has been discontinued however, and the board lay-out was modified to incorporate the above two in separate packages. The load regulation typically measures less than 2% at current levels up to 0.5 A, which assumes an h_{FE} of 40 for the RF power devices. The board surface provides a sufficient heat sink for the 2N5990 pass transistor, but a separate heat dissipator, such as Thermalloy 6107 can be added if necessary. With the component values shown, the bias is adjustable from 0.4 to 0.8 volts.



Transformer Construction

Gain flatness over the band is achieved using base input networks R_1C_2 and R_2C_3 and negative feedback through R_3 and R_4. The networks represent a series reactance of 0.69 ohms at 30 MHz rising to 1.48 ohms at 2 MHz. A single-turn winding in the collector choke provides a low-impedance negative feedback source, thus R_3 and R_4 determine the amount. The reactance of C_4 reduces feedback at high frequencies with the result that feedback increases an average of 4 dB per octave at decreasing frequency.

For continuous operation at full power CW, it is recommended that heat sink compound, such as Dow Corning #340, be applied between the board surface and R_3 and R_4, and if possible have air circulating over the top of the circuit board as well.

The effective base-to-base impedance, increased by the RC networks is about 5 ohms at midband. As a result of this and the 9:1 impedance ratio in the input transformer T1, the input VSWR is limited to 1.9:1 or less across the band. Transformer T2, in addition to providing a source for the feedback and carrying the dc collector current, acts as the rf center tap of the output transformer. To construct T2, wind 5 turns of 2 twisted pairs of AWG No. 22 enameled wire on a Stackpole 57-9322 toroid (Indiana General F627-8Q1).

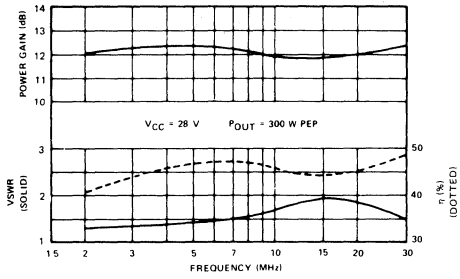
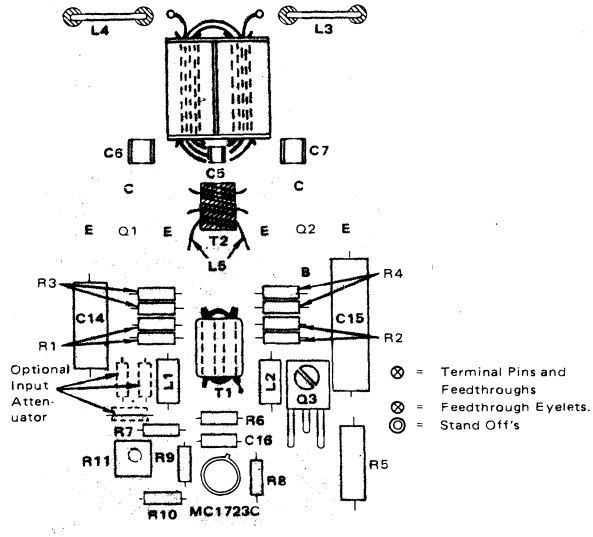
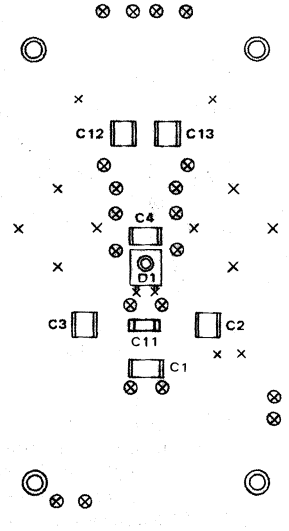


Figure 1 — Collector Efficiency, Power Gain and VSWR vs Frequency

A Stackpole dual balun ferrite core 57-1845-24B is used for T1. The secondary is made of ⅛" copper braid, through which three turns of the primary winding (No. 22 Teflon® insulated hook-up wire) are threaded. The construction of T3 is similar to that of T1. It employs two Stackpole 57-3238* ferrite sleeves which are cemented together for easier construction. The primary is made of ¼" copper braid, through which three turns of No. 16 Teflon® insulated wire are threaded for the secondary.

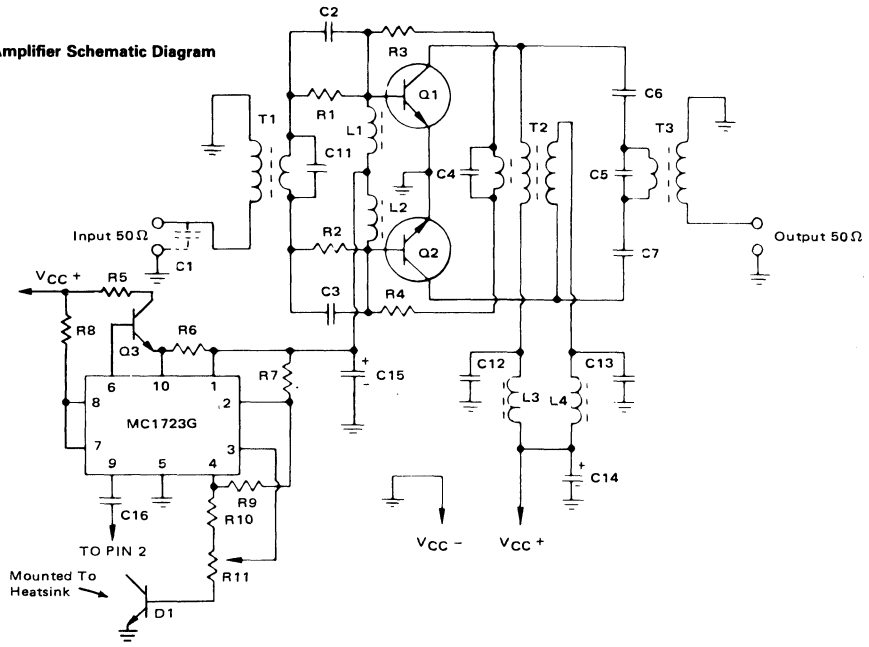


A.



B.

300-Watt Linear Amplifier Schematic Diagram



C1 – 100 pF
C2, C3 – 5600 pF
C4, C5 – 680 pF
C6, C7 – 0.10 μF
C11 – 470 pF
C12, C13 – 0.33 μF
C14 – 10 μF – 50 V electrolytic
C15 – 500 μF – 3 V electrolytic
C16 – 1000 pF

R1, R2 – 2 X 3.3 Ω, 1/2 W in parallel
R3, R4 – 2 X 3.9 Ω, 1/2 W in parallel
R5 – 47 Ω, 5 W
R6 – 1.0 Ω, 1/2 W
R7, R8 – 1.0 k, 1/2 W
R9 – 18 k, 1/2 W
R10 – 8.2 k, 1/2 W
R11 – 1.0 k Trimpot
D1 – 2N5190
L1, L2 – Ferroxcube VK200 20/4B
L3, L4 – 6 ferrite beads each, Ferroxcube 56590 65/3B

Q1, Q2 – MRF422, Q3 – 2N5990
T1, T2, T3 – See text

All capacitors except electrolytics and C16 are chips –

Union Carbide type 1813 and 1225, or Varadyne size 18 or 14, or equivalent

For production quantities, the braid in T_3 may be made of brass or copper tubes with their ends soldered to pieces of PC board laminate. See cover picture and Motorola AN-749 for details.

The bandwidth characteristics of these transformers do not equal those of the transmission line type, but they're much easier to duplicate.

The measured performance of the amplifier is shown in figures 1, 2, and 3 and harmonic rejection data in table I.

Table I. Output harmonic contents, measured at 300-W CW (all test data taken using a tuned output, narrow band signal source).

	2nd	3rd	4th	5th
f (Mhz)	(dB below the carrier)			
30.0	−38	−25	−34	−48
20.0	−33	−13	−43	−45
15.0	−50	−10	−51	−47
7.50	−40	−30	−55	−47
4.0	−37	−22	−55	−37
2.0	−36	−18	−45	−37

*A similar product is available from Fair-Rite Products Corp., Wallkill, N.Y., 12589

®Registered trademark of DuPont

PCB, chips capacitors, transformers T_1, T_2, T_3, and ferrite beads are available from: COMMUNICATIONS CONCEPTS, 2648 N. Aragon Ave., Kettering, Ohio 45420. Telephone: (513) 294-8425.

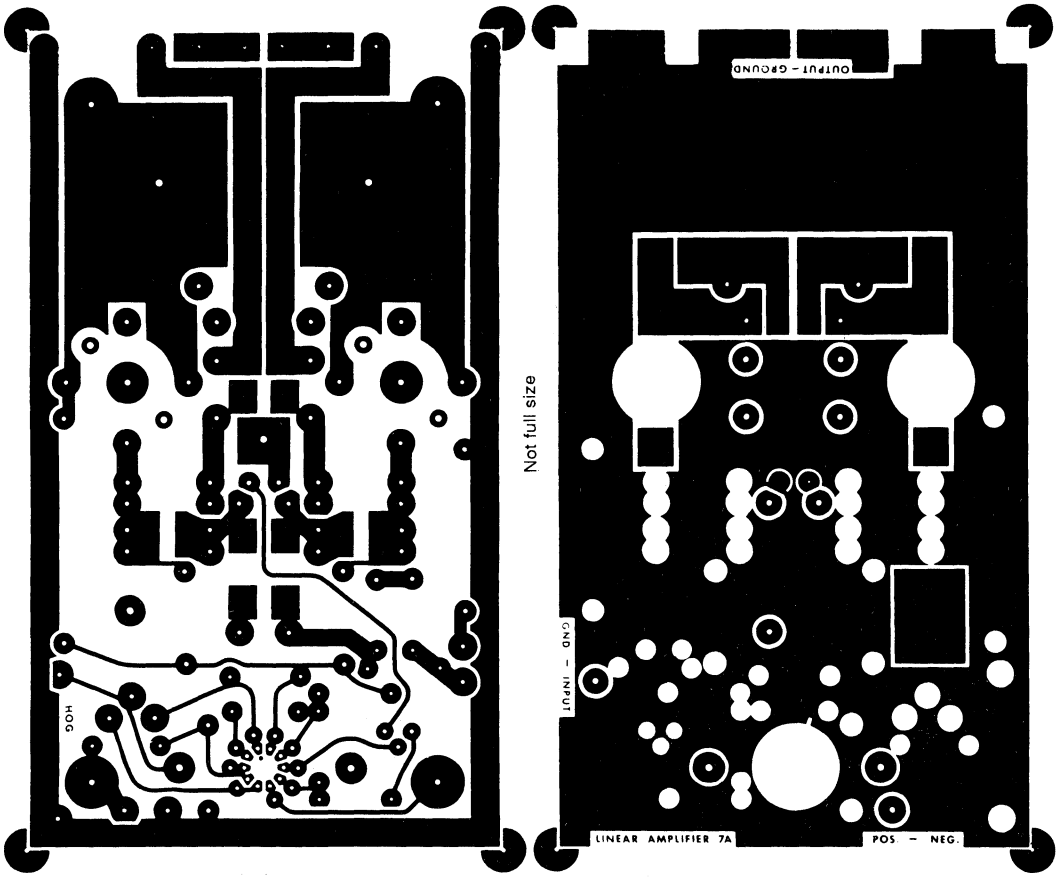


Figure 2 — IMD vs Frequency

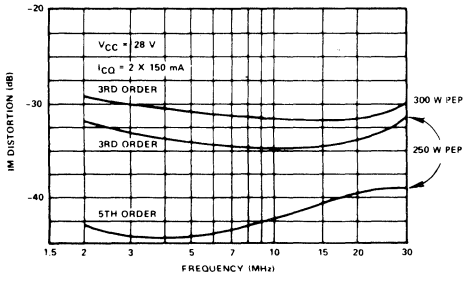
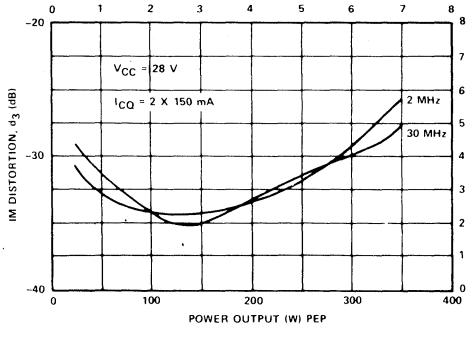
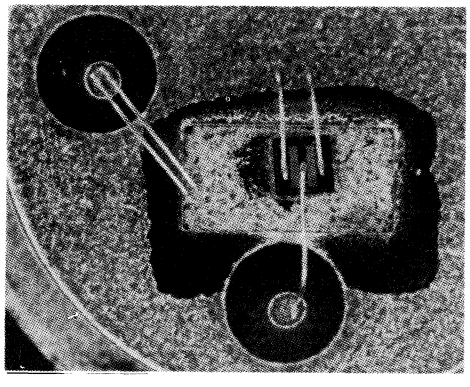


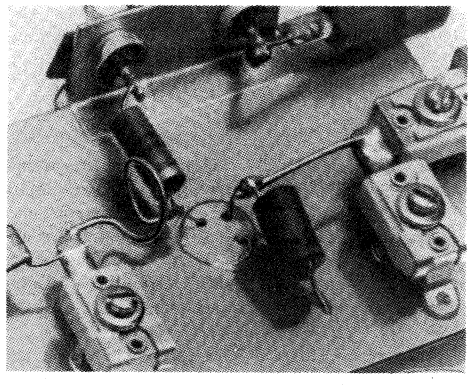
Figure 3 — IMD vs Power Output



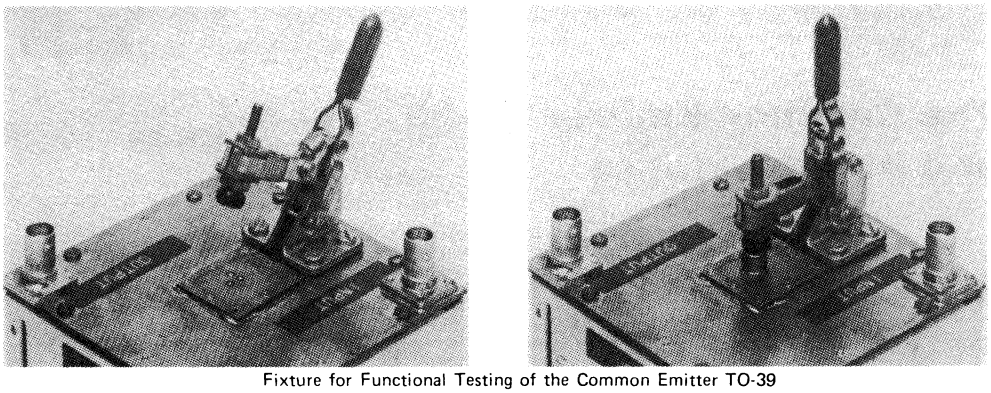
The Common Emitter TO-39 and its Advantages



The common emitter TO-39 package is one of Motorola's latest innovations in low-cost rf packages. It differs from conventional TO-39's or TO-5's in that the emitter, not the collector, is connected to the metal case. To achieve this, a BeO insulating block metallized on top and bottom is brazed to the can bottom and the transistor chip brazed to the BeO insulator. Wires are then bonded from the chip and insulator block to the terminals and the can bottom as shown in the photo. With NPN transistors, this configuration permits direct connection of the can to rf and negative dc ground for many class B and C circuits.



Two important advantages can be derived from the common emitter TO-39: By connecting the case to the rf circuit ground, emitter inductance is reduced and gain increased by 3 to 5 dB over that of comparable, conventionally wired transistors. And the case may be directly pressed, clipped, or soldered to the heat sink with no effect on rf performance. This feature may eliminate the need for the heat radiating "coolers" because soldering the transistor bottom to the circuit, typically a PC board, improves dissipation by removing heat through the thick metal base rather than the thin can.

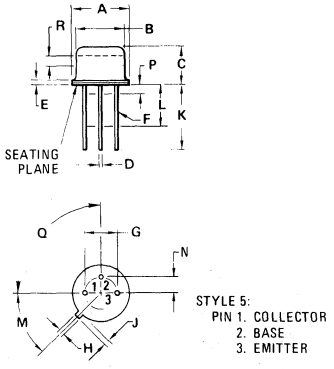


Fixture for Functional Testing of the Common Emitter TO-39

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39



For example, the MRF227 was mounted in this manner and a θ_{jc} of 15°C/W was measured using a Barnes RM-2A Infrared Microscope. Compared to an MRF607 in a conventional package operating under identical conditions, this is greater than a 2:1 reduction in thermal resistance. And as side benefits, the lower θ_{jc} also reduces power slump and improves reliability.

In many mobile radios CE-TO39 devices can replace stud or flange mounted stripline parts used for 1- to 4-watt drivers. This conversion should normally offer a significant savings in the cost of parts as well as the costs of mounting hardware and labor.

The designer of compact handheld radio equipment will find the CE-TO39 offers a real advantage from the elimination of interstage RFI or coupling because the can is at rf ground. Stability is usually improved and the higher available gain may reduce the number of transmitter stages. Simplified and improved cooling may also be obtained by connecting the can directly to the radio housing or chassis.

To sum it up: The emitter-to-can wired TO-39 known as the CE-TO39 offers the designer significant improvements in both gain and thermal performance. Because of its price, compared to SOE and TO-60 packages, the designer can use the CE-TO39 to reduce costs. And he can make his design easier to assemble with no loss in rf performance.

Predict Frequency Accuracy for MC12060 and MC12061 Crystal Oscillator Circuits

Crystal oscillators are used when it is necessary to generate a precise and highly stable signal. Such circuits typically provide this stable signal at a frequency close to the resonant frequency (either parallel or series) of their crystal. However, circuit components and other factors external to the crystal influence the crystal's natural resonance to some degree, an effect often referred to as "pulling" or "warping." A discussion of the variation in crystal frequency as a function of differing ICs*, temperature, and dc supply voltage is presented in this bulletin to aid the designer in predicting the amount of frequency pull in his particular design.

Crystal Characteristics

As shown by the equivalent circuit of Figure 1, crystals behave as open circuits to dc. For ac signals below a crystal's series resonant frequency, the crystal exhibits a capacitive reactance. As frequency increases, the series resonance of C_S and L_S is reached. The crystal then appears as a low value resistor, R_S, shunted by a small capacitance, C_O. At frequencies above series resonance, the C_S, L_S combination appears as an inductive reactance. As frequency increases even higher, the inductive reactance grows eventually equalling the capacitive reactance of C_O. This is the high impedance, parallel resonant frequency for the crystal. Although the separation in frequency between series and parallel resonance varies for different crystals, series resonance will typically occur several hundred Hertz to a few kilohertz below parallel resonance.

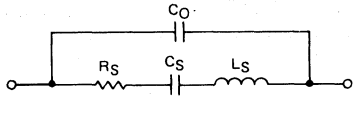


FIGURE 1 – Crystal Equivalent Circuit

Crystals used with MC12060/61 devices must meet the requirements specified in their data sheet. Since these devices oscillate at the frequency that provides the lowest impedance (series resonance) between pins 5 and 6, a crystal must not exhibit a spurious response resulting in impedance values near or less than the desired series resonance impedance. In the evaluations discussed here, standard commercial crystals with ±0.0025% calibration tolerance, fundamental mode, were used with the MC12060/61 devices. Measured series resonance frequencies for the crystals used, along with equivalent series inductance (L_S) and resistance (R_S) values are presented in Table I.

*Specifically, the Motorola MC12060/12560 and MC12061/12561 integrated circuits which are designed for use with an external fundamental series resonant crystal. Specified operating frequency range is 100 kHz to 2 MHz for the 12060/12560 and 2 MHz to 20 MHz for the 12061/12561. Complementary sine wave, com-

TABLE I
Crystal Parameters

Series Resonant Frequency (MHz)	Equiv. Series Resistance R_S (Ohms)	Equiv. Series Inductance L_S (mH)
2.500025	38.0	274.0
8.079977	8.4	17.6
13.411100	6.9	7.0
18.749563	12.5	2.9
19.999528	9.2	–
(kHz)		
100.002	497	–
200.012	509	–
500.031	995	9857
999.985	380	2629
2000.032	96	526

plementary ECL, and single ended TTL outputs are available. Complete technical specifications for these ICs can be found on the device data sheet. Additional applications information is available in Motorola application note AN-756 and engineering bulletin EB-60.

MC12060/61 Performance

The circuit elements in an oscillator environment have an effect on the fundamental resonant frequency of a crystal. To measure the influence of the MC12060/61 devices, tests were made using the circuit of Figure 2. Frequency measurements were taken at the sine wave output (pin 2 or pin 3), the 680 ohm resistor making it possible to drive a 50 ohm load. Laboratory quantities of the ICs were tested, consequently some variation in results could be expected if a production run cross section were evaluated.

MHz. Table III shows the variation in pull on the same crystal resulting from the use of different MC12060 and MC12061 devices.

Figure 3 gives the frequency shift caused by the MC12560/61 devices operating over their temperature range of -55°C to +125°C. Similar results can be expected for the MC12060/61 devices over their specified range of 0°C to +75°C. Data was taken with the crystals at a constant temperature of approximately +25°C to isolate the effect of temperature on the ICs. Since the curves are normalized, one must add the appropriate room temperature value (see Table II) to obtain the net frequency pull at a specific temperature. For example, the MC12561 device operating with the nominal 8.08 MHz crystal would exhibit a net pull of approximately

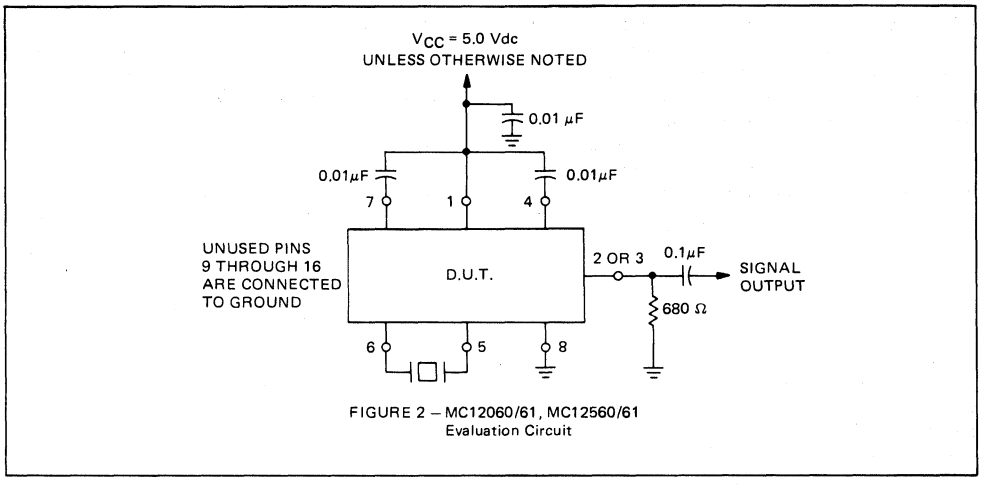


FIGURE 2 – MC12060/61, MC12560/61
Evaluation Circuit

The measured pull of the MC12060/61 devices on a crystal's series resonant frequency is shown in Table II for room temperature operation. Resonant frequency is always reduced, the effect becoming more pronounced with increasing operating frequency. Where minimum pull is required, the MC12061 rather than the MC12060 should be considered for use at or slightly below 2.0

-40 - 11 = -51 PPM at +125°C. The curves show a small temperature dependence at lower frequencies that increases significantly above midband. Although not plotted, over the -55°C to +85°C range MC12560 at 2 MHz and MC12561 at 18.75 MHz changed from +155 to -275 and from +7 to -45 PPM respectively, referenced to +25°C.

TABLE II
Crystal Frequency Pull In Percent For MC12060/61 IC's

DEVICE	MC12060					MC12061				
NOMINAL CRYSTAL FREQUENCY (MHz)	0.100	0.200	0.500	1.00	2.00	2.50	8.08	13.41	18.75	20.0
CRYSTAL PULL IN PERCENT	*	–0.0005	–0.0012	–0.0040	–0.03	–0.0002	–0.004	–0.01	–0.03	–0.05

*LESS THAN 1 Hz, MEASUREMENT LIMITED BY RESOLUTION OF TEST EQUIPMENT.

TABLE III
Measured Frequency Deviation From Device to Device

NOMINAL FREQUENCY (MHz)	FREQUENCY DEVIATION (Hz)	(PPM)
MC12060		
0.100	*	*
0.200	*	*
0.500	2	4.0
1.000	10	10.0
2.000	165	82.5
MC12061		
2.50	2	0.8
8.08	110	13.6
13.41	485	36.2
18.75	1755	93.6

*Less than 1 Hz, Measurement limited by resolution of test equipment.

pacitor and its effect on increasing frequency. Therefore, if only a small increase in frequency is required, the trim capacitor value may become unreasonably large. To assure a suitable value for the capacitor, it may be necessary to specify the crystal frequency lower than the actual desired operating frequency. The pulling effect of the ICs will normally be much less than that of the trim capacitor and therefore the crystal can simply be specified such that the series combination of crystal and trim capacitor is in series resonance at the desired operating frequency. If it is also desired to account for the effects of the ICs, this may be approximated by considering the MC12060 to add 266 μH and the MC12061 1.6 μH in series with the crystal.

As a typical example, assume that the MC12061 is to be

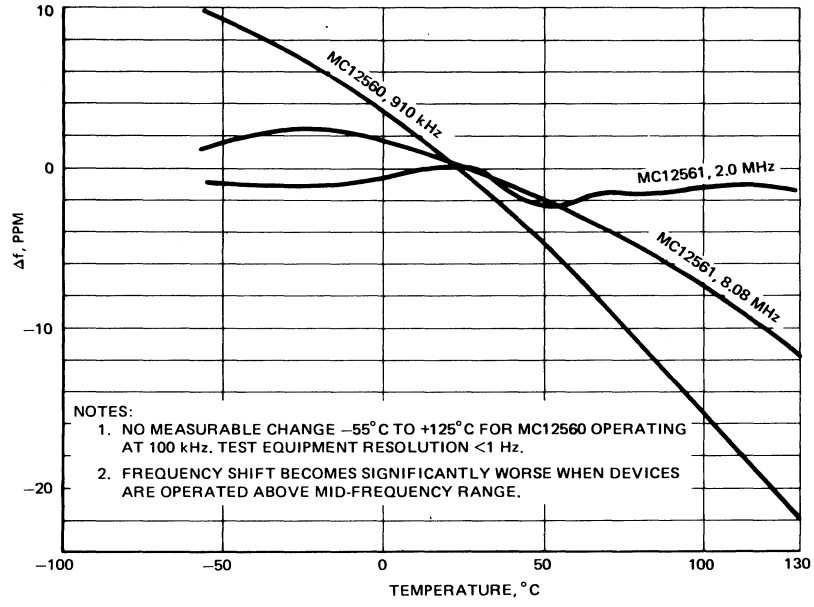


FIGURE 3 – Frequency Shift VS Temp. with Crystal Located Outside Temp. Chamber

Figure 4 provides plots of frequency pull as a function of change in dc supply for the MC12060/61 devices.

Design Example

The ICs are designed to pull the crystal's natural series resonant frequency lower. If desired, this permits a trim capacitor to be inserted in series with the crystal to set the oscillator "on frequency". Since this trim capacitor is approximately in series with C_S of the crystal, there is an inverse relationship between the value of the trim capacitor used with a nominal 8 MHz crystal having an equivalent series inductance L_S = 17.6 mH. Figure 5 shows the equivalent circuit. With no C_{TRIM} added, the IC will lower the crystal's resonant frequency by approximately $\sqrt{(17.6 + 0.0016)/17.6}$ or 0.0045%. Use of a 10 pF trim capacitor would place a net impedance in series with the crystal of $j\omega L_{IC} - j\ 1/\omega C_{TRIM} = -j\ 1.909 \times 10^3$. This corresponds to an equivalent capacitance in series with the crystal of $C_{EQUIV} = \frac{1}{2\pi \times 8 \times 10^6 \times 1.909 \times 10^3} =$

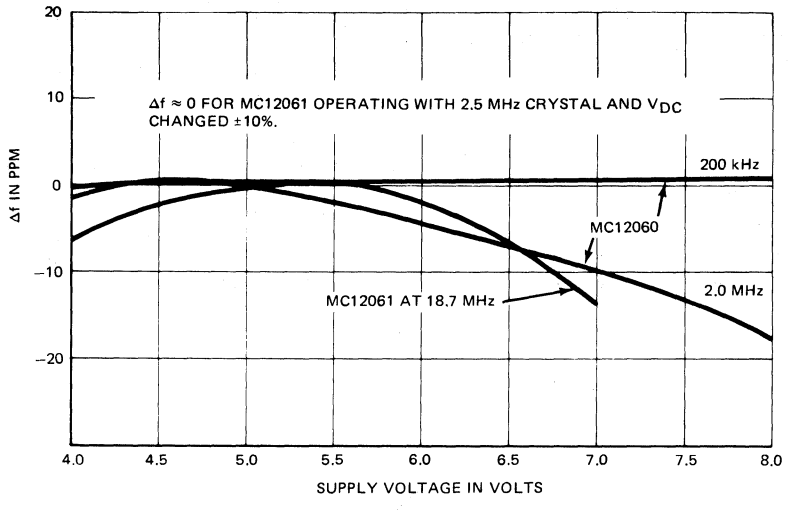
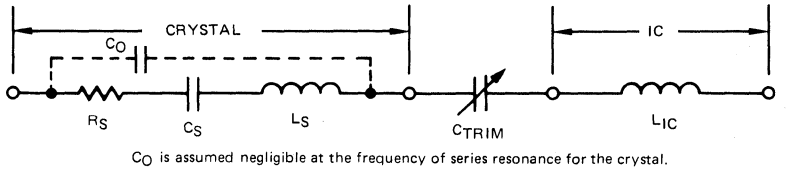


FIGURE 4 – MC12060/61 Frequency Shift Versus DC Supply Voltage Value



C_O is assumed negligible at the frequency of series resonance for the crystal.

FIGURE 5 – Crystal/IC Oscillator Equivalent Circuit

10.42 pF. The crystal should be specified so that the crystal reactance and that of C_{EQUIV} are in series resonance at the operating frequency (8.000 MHz). In effect, this requires a crystal with a series resonance slightly below 8.000 MHz so that at precisely 8.000 MHz it presents a +j impedance which equals the −j impedance supplied by C_{TRIM} in series with L_{IC}, i.e., C_{EQUIV}.

If the crystal is not resonant below 8 MHz as suggested, but rather at exactly 8 MHz, C_{TRIM} must then be chosen to resonate with an L_{IC} inductance of 1.6 μH requiring an undesirably large value of 247 pF. The C_{TRIM} value can approach infinity if the crystal calibration tolerance allows the crystal to be series resonant on the high side of 8 MHz.

A similar procedure can be followed for the MC12060 device. In this case the approximation L_{IC} = 266 μH is used. The calculated frequency pull for the nominal 500 kHz, 1 MHz and 2 MHz crystals described in Table I is then −0.0013, −0.0051 and −0.0253 percent respectively. This agrees closely with the measured values of −0.0012, −0.0040, and −0.03 percent given in Table II.

EB77

A 60 watt 225-400MHz Amplifier - 2N6439

This bulletin describes a 60 watt, 28 volt broadband amplifier covering the 225-400 MHz military communications band. The amplifier may be used singly as a 60 watt output stage in a 225-400 MHz transmitter, or by using two of these amplifiers combined with quadrature couplers, a 100 watt output amplifier stage may be constructed. Typical performance curves of gain, efficiency, and input SWR are shown in Figures 5, 6, and 7.

Circuit Description

This circuit is designed to be driven from a 50 ohm source and work into a nominal 50 ohm load. The input network consists of two microstrip L-sections composed of Z1, Z2 and C2 through C6. C1 serves as a dc blocking capacitor. A 4:1 impedance ratio coaxial transformer T1 completes the input matching network. L1 and ferrite bead serve as a base decoupling choke.

The output circuit consists of shunt inductor L2 at the collector, followed by two microstrip L-sections composed of Z3, Z4 and C8 through C11. C12 serves as a dc blocking capacitor, and is followed by another 4:1 impedance ratio coaxial transformer.

Collector decoupling is accomplished through the use of L3, L4, C14 through C16 and R1.

Construction

The circuit is constructed on a 3.375 X 2.5 inch (8.57 X 6.35 cm) double sided PC board. Board material is 3M Glass Teflon*, with a thickness of 0.031 inch (0.0787 cm). Glass Teflon was selected for its low loss and dielectric consistency. Figure 2 is a 1:1 photomaster print of the top side of the board. Eyelets are placed at the points marked by a plus sign to carry the top ground to the bottom side ground return. The edges of the transistor mounting hole beneath the emitter leads are also wrapped, using copper foil soldered in place to insure a solid emitter ground.[1,2] Construction details of the 4:1 transformers are shown in Figure 4.

*Registered Trademark of Dupont

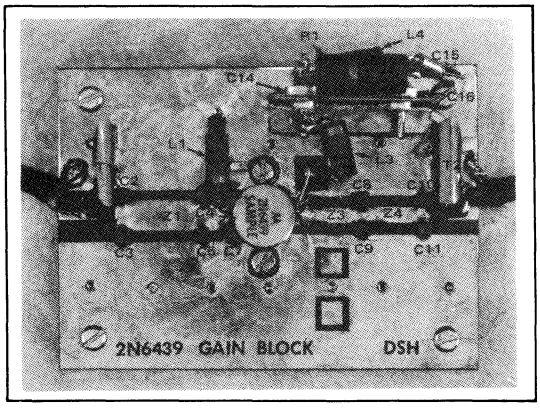


FIGURE 1 – Component Layout of the Amplifier

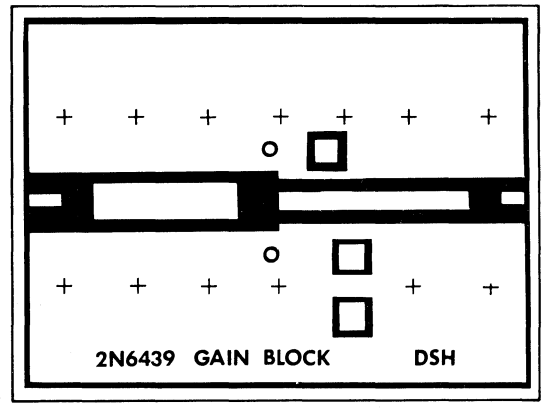
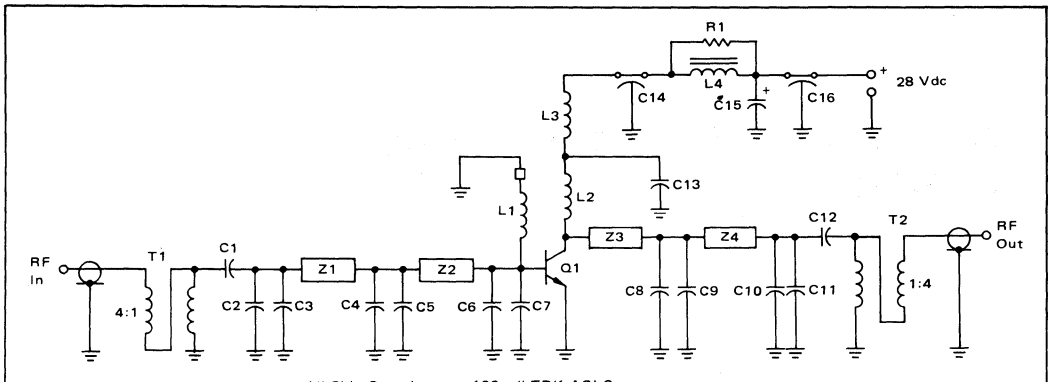


FIGURE 2 – Photomaster (not full size)



C1 – 63 pF Chip
C2, C8 – 27 pF Chip
C3 – 24 pF Chip
C4 – 15 pF Chip
C5, C9 – 30 pF Chip
C6, C7 – 50 pF Chip
C10 – 10 pF Chip
C11 – 5.1 pF Chip
C12 – 150 pF Chip
C13 – 270 pF Chip
C14, C16 – 680 pF Feedthru
C15 – 1.0 μF 50 V Tantalum

All Chip Capacitors are 100 mil TDK-ACI Co, Style FC282 BAG
L1 – 0.15 μH Molded Choke with Ferroxcube Bead #56-590-65/4B on ground end of coil
L2 – 1 Turn #22 AWG, 1/8" ID
L3 – 0.15 μH Molded Choke
L4 – Ferroxcube VK-200-19/4B

Q1 – 2N6439

R1 – 10 Ω 2 Watt

T1, T2 – 25 Ω Subminiature Coax (Type UT25) 2.25 inches (57.15 mm) long

Z1 – Microstrip Line
800 mils L X 225 mils W
20.32 mm L X 5.715 mm W
Z2 – Microstrip Line
200 mils L X 225 mils W
5.08 mm L X 5.715 mm W
Z3, Z4 – Microstrip Line
550 mils L X 125 mils W
13.97 mm L X 3.175 mm W

Board – 0.031" (0.787 mm) Glass Teflon
ϵ_r = 2.56

FIGURE 3 – 2N6439 60 Watt Building Block 225–400 MHz

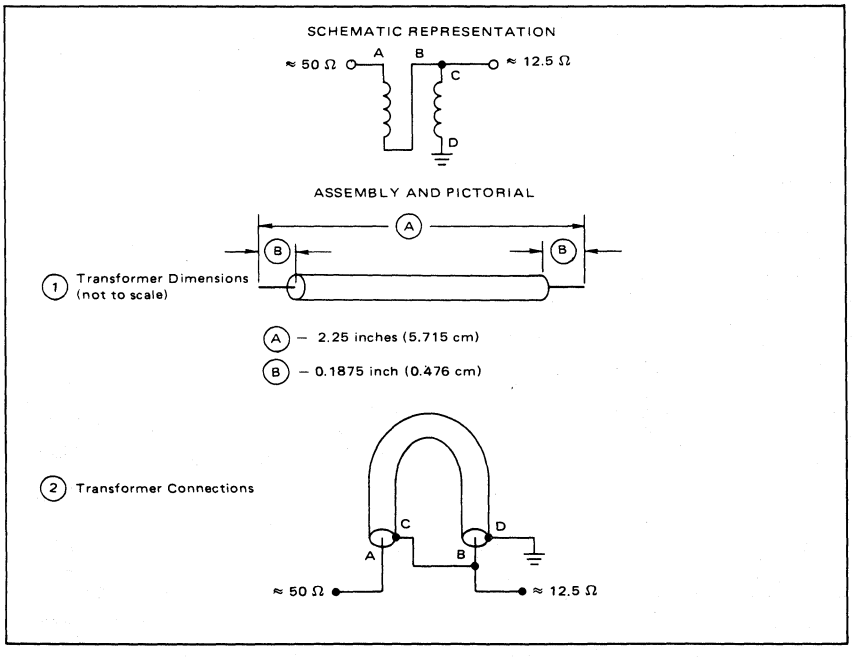


FIGURE 4 – Construction Details of the 4:1 Unbalanced to Unbalanced Transformers

AMPLIFIER PERFORMANCE

FIGURE 5 – Power Gain versus Frequency
Efficiency versus Frequency

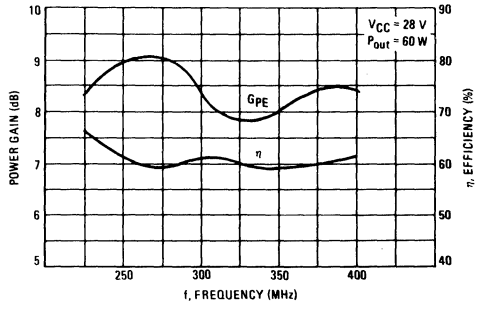


FIGURE 6 – Output Power versus Input Power

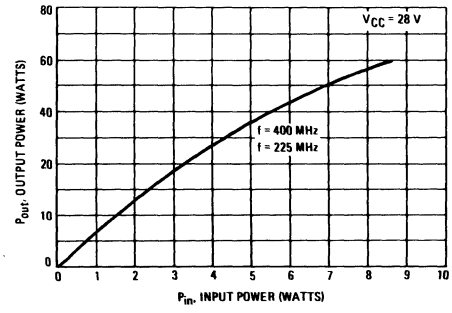
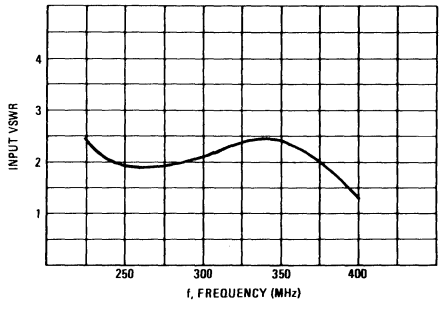


FIGURE 7 – Input VSWR versus Frequency



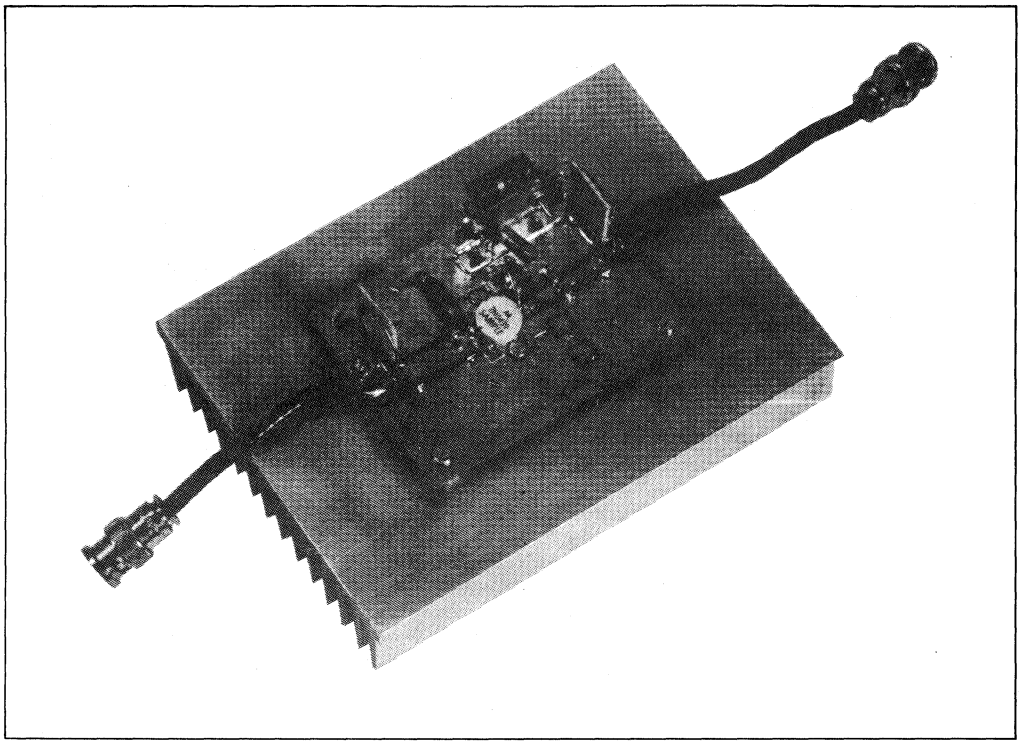


FIGURE 8 – Amplifier Assembly

Bibliography

1. "Mounting Stripline – Opposed Emitter (SOE) Transistors," Motorola Application Note AN-555, Motorola Semiconductor Products Inc., Phoenix, Arizona.

2. Glenn Young, "Microstrip Design Techniques for UHF Amplifiers," Motorola Application Note AN-548A, Motorola Semiconductor Products Inc., Phoenix, Arizona.

3. Roy Hejhall, "Systemizing RF Power Amplifier Design," Motorola Application Note AN-282A, Motorola Semiconductor Products Inc., Phoenix, Arizona.

NOTE: A 10 Watt 225–400 MHz Amplifier–MRF331 is described in Engineering Bulletin EB-74.

A 1 watt, 2.3GHz Amplifier

Introduction

Simplicity and repeatability are featured in this 1-watt S-band amplifier design. The design uses an MRF2001 transistor as a common base, Class C amplifier. The amplifier delivers 1-watt output with 8 dB minimum gain at 24 V, and is tunable from 2.25 to 2.35 GHz. Applications include microwave communications equipment and other systems requiring medium power, narrow band amplification. A photograph of the amplifier is shown in Figure 1.

Circuit Description

The amplifier circuitry consists almost entirely of distributed microstrip elements. A total of six additional components, including the MRF2001, are required to build a working amplifier. Refer to Figure 2 for the schematic diagram of the amplifier.

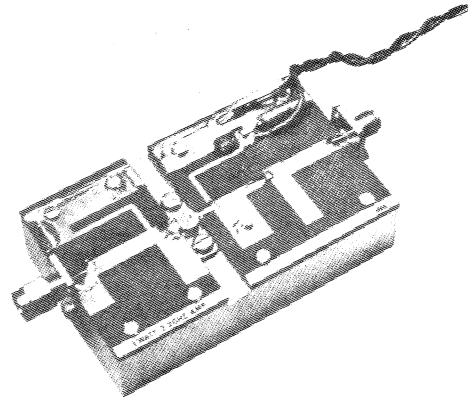
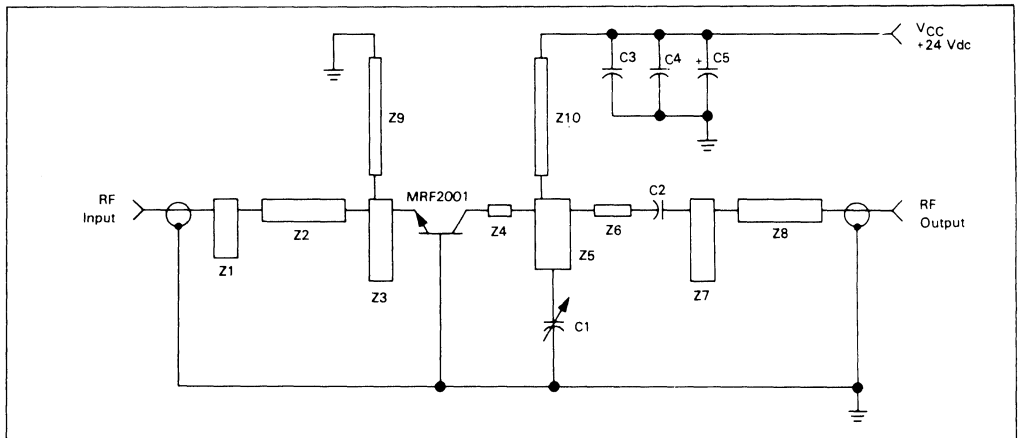


FIGURE 1 — 1-W, 2.3 GHz Amplifier



C1 — 0.4-2.5 pF Johanson 7285*
C2, C3 — 68 pF, 50 mil ATC**
C4 — 0.1 μF, 50 V
C5 — 4.7 μF, 50 V Tantalum

Z1-Z10 — Microstrip; see Photomaster, Figure 3

Board Material — 0.0625" 3M Glass Teflon,***
$\epsilon_r = 2.5 \pm 0.05$

*Johanson Manufacturing Corp., 400 Rockaway Valley Road, Boonton, NJ 07005
**American Technical Ceramics, One Norden Lane, Huntington Station, NY 11746
***Registered Trademark of Du Pont

FIGURE 2 — Schematic Diagram

The input and output impedances of the transistor are matched to 50 ohms by double section low pass networks. The networks are designed to provide about 3% 1 dB power bandwidth while maintaining a collector efficiency of approximately 30%. There is one tuning adjustment in the amplifier — C1 in the output network. Ceramic chip capacitors, C2 and C3, are used for DC blocking and power supply decoupling. Additional low frequency decoupling is provided by capacitors C4 and C5. Refer to Figure 3 for a 1:1 photomaster of the circuit boards.

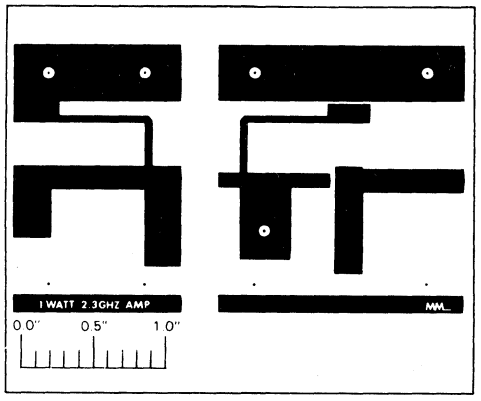


FIGURE 3 — Circuit Photomaster

Amplifier Assembly

The circuit boards are mounted on a 3.125" × 1.875" × 0.750" aluminum block. A 0.062" deep and 0.260" wide slot is milled in the heat sink as shown in Figure 4.

The transistor mounts in the slot with two 4-40 screws. An alternate approach that would eliminate the need for milling is the laminated structure shown in Figure 5.

Using the laminated assembly, the transistor is mounted on the surface of the block and 0.062" aluminum shim stock is sandwiched between the block and the circuit boards. Connector mounting plates are required if SMA type connectors are used for the RF input and output. The SMA connectors can be fastened directly to the block if the milled approach is used. Either method results in the same performance for this 1-watt design. The laminated structure, however, may not be suitable for higher power designs. With higher power levels the transistor impedances are lower. The RF ground impedance through the laminated metal may be sufficiently high to impair gain and stability. This point emphasizes the fact that the successful design of RF amplifiers is dependent not only on attention to electrical considerations, but to the physical construction as well. While construction related parasitics cannot be totally ignored at medium frequencies, they can pose serious problems at microwave frequencies. It is recommended that the following construction techniques be followed when building this amplifier. Refer to Figure 6 for the component placement diagram.

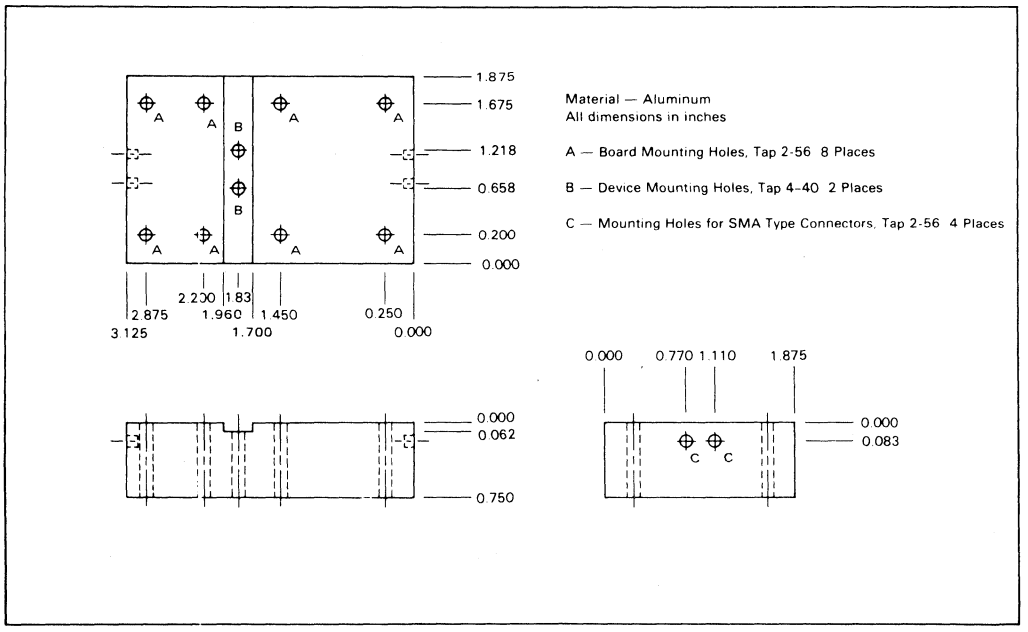


FIGURE 4 — Amplifier Heat Sink

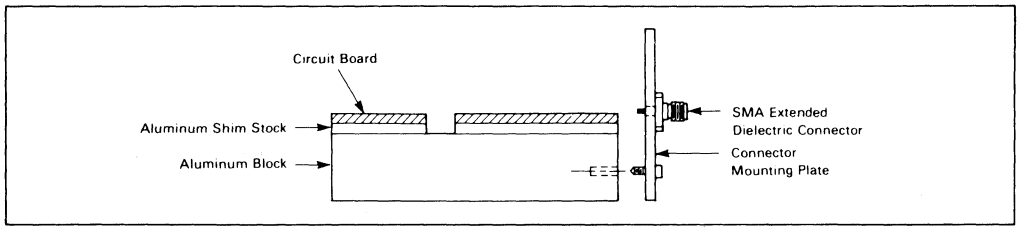
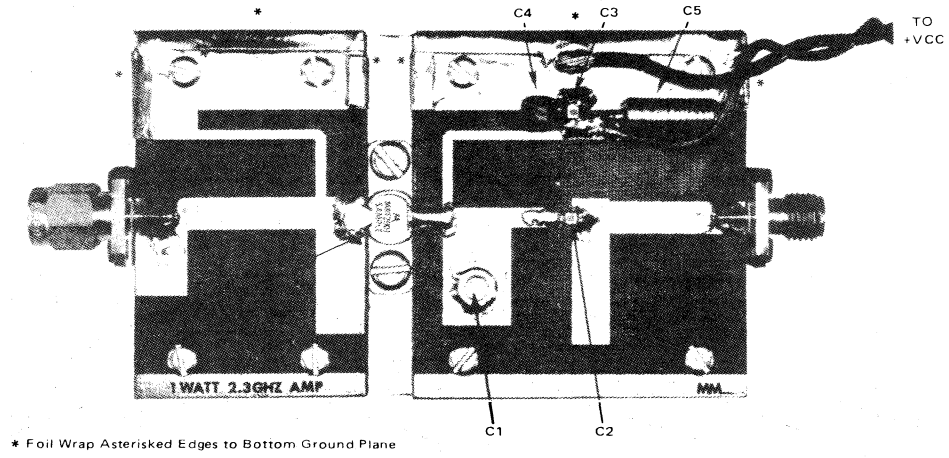


FIGURE 5 — Laminated Assembly



* Foil Wrap Asterisked Edges to Bottom Ground Plane

FIGURE 6 — Assembly Diagram

Construction Notes

1. The transistor is fastened to the heat sink with two 4-40 screws. The mounting surface should be flat and clean. Thermal compound should not be used on the underside of this device; the flange provides the transistor base connection and must make good electrical contact with the heat sink. The wide lead is the emitter and the narrow lead is the collector.

2. The edges of the boards marked with an asterisk (see Figure 6) must be foil wrapped to the bottom ground plane to provide a low impedance RF ground connection for C3, C4, C5 and the emitter choke, Z9. This is accomplished by soldering a 1/4"-wide strip of 1- to 5-mil thick copper foil to the top ground plane and then wrapping it around the edge of the board. The other edge of the foil is soldered to the bottom ground plane.

3. Use a #31 drill bit to drill the board mounting holes. With the transistor already mounted to the heat sink, slide the boards into position so they butt up against the transistor. This will insure that the excess lead inductance of the transistor is kept to a minimum. The boards can now be fastened to the heat sink and the remaining components mounted.

4. Use a minimum of heat when soldering C2 and C3. Excess heat could cause the end metal of the chip capacitor to separate from the ceramic.

5. C1 is a miniature variable capacitor whose high self-resonant frequency makes it ideal for use at microwave frequencies. The package design makes it very convenient to use wherever a shunt capacitive element is desired and is used here to vary the capacitance of microstrip stub, Z5. The capacitor is mounted by drilling a 0.120" diameter hole (#31 drill bit) at the point indicated in Figure 6. Using the circuit board as a template, mark the point on the heat sink directly below the mounting hole. Since the capacitor is slightly longer than the thickness of the board, a clearance hole is needed at this point. The bottom of the capacitor is soldered to the ground plane on the bottom of the board. The flange of the capacitor is soldered to Z5. Avoid getting solder into the area above the flange as this will prevent the movement of the tuning piston.

Performance Data

Amplifier tune-up is accomplished by adjusting C1 for maximum output power with minimum collector current. The amplifier will tune from 2.25 to 2.35 GHz while maintaining an input VSWR of less than 2:1. Typical performance curves appear in Figure 7. Figures 7a and 7b show performance with the amplifier re-tuned for each frequency. Figure 7c shows performance without re-tuning. Note from Figure 7c that the instantaneous 1 dB bandwidth is approximately 70 MHz with the amplifier tuned to a center frequency of 2.3 GHz.

FIGURE 7 — Performance Curves

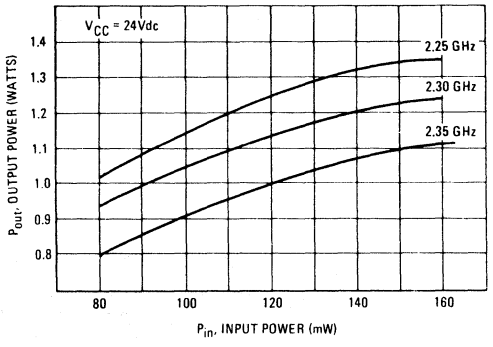


FIGURE 7a — Output Power versus Input Power

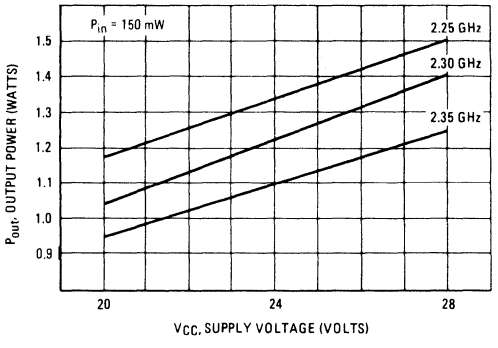


FIGURE 7b — Output Power versus Supply Voltage

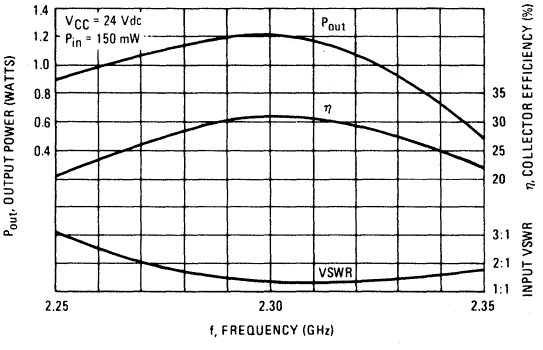


FIGURE 7c — Output Power, Efficiency and VSWR versus Frequency

NOTE: The MRF2001 is one of a family of 2 GHz power transistors with RF output powers as indicated below:

MRF2001 1 W	MRF2005 5 W
MRF2003 3 W	MRF2010 10 W

EB90

Low Cost VHF Amplifier Has Broadband Performance

Introduction

This bulletin presents two VHF amplifier designs intended for FM or CW service in the 136-174 MHz band. Both amplifiers feature the Motorola MRF260 and MRF262 plastic encased VHF transitors which are rated at 5.0 W and 15 W power output respectively. This new series is derived from a line of highly successful device types of similar capability, but packaged in a standard configuration, (i.e., stripline packages). The MRF260 and MRF262 are in a standard TO-220 silicone epoxy case with the emitter wired to the metal tab and center lead of the device. This common emitter configuration results in good RF performance, improved thermal conductivity, and ease of mounting in an RF amplifier, by connecting the transistor mounting flange to RF and DC ground.

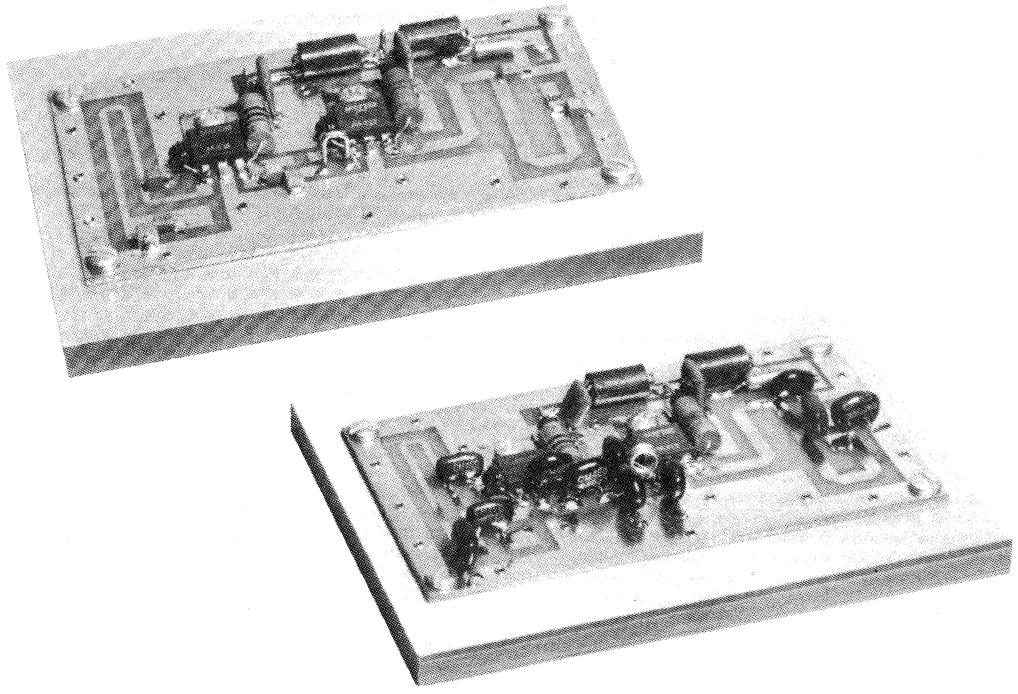


FIGURE 1 — Engineering Models. A Common Board Layout is Used for Both Versions

Design Considerations

The lower frequencies (136–160 MHz) are serviced by a design utilizing low-cost dipped silver mica capacitors. For a broadband response in the higher frequencies; (160–174 MHz), low inductance, ceramic chip capacitors are used.

Ease of assembly, repeatability and fast economical construction received the utmost consideration in the design of this amplifier. TO-220 devices result in a low profile circuit which minimizes the volume occupied by the amplifier. Additionally, the MRF262 transistor used in the output stage is a rugged device, able to tolerate high load SWR conditions. Maximum use of printed inductors assures good repeatability.

Both amplifiers utilize stagger tuned networks to enhance bandwidth. Additionally, each design retains excellent gain and stability characteristics when narrow banded. All of these merits are attributed to optimum device gain and the reasonably high inter-stage impedance levels incurred at these power levels.

Circuit Description

The amplifier has two stages and uses 5.0 W and 15 W rated transistors to accomplish the desired gain and power output. Two stage transmission line Chebyshev networks accomplish coupling and impedance transformation at the input and output. Nominal impedance levels are 50 ohms, while the interstage network transforms device impedances directly. Values for the reactive elements of these networks were almost entirely generated by computer aided design. Although the interstage network is straight forward in design, it required some modification and refinement of computer generated values to achieve the final results and accomodate available component values.

Construction

The amplifier is assembled on double-sided G-10 fiberglass board with 1 oz. copper cladding. The format is 2.0″ × 3.5″ and a photomask is provided (Figure 13). Some method of electrically connecting the upper and lower ground plane is required. Eyelets or plated through holes are recommended, but alternative measures such as short pieces of wire soldered to both planes can be used successfully. Failure to provide an adequate or consistent ground plane may result in poor RF performance, instability, and unpredictable tuning. The reverse side of the board retains all copper and forms the ground plane. Component placement and the recommended position of grounding eyelets is shown in Figures 13, 5, and 7. All component leads are positioned and soldered above the board. There are no through connections other than grounding points. This facilitates component positioning, replacement, and accessability. The transistors are fitted into a 0.4″ by 0.65″ opening in the board and are installed directly against the heat sink. A coating of heat sink compound such as Dow Corning 340 between each device and the heat sink improves thermal contact and helps prevent power slump.

At frequencies beyond 100 MHz, dipped silver mica capacitors generally become inductive, and do so with a high degree of unpredictability. This phenomenon is also dependent upon component value and becomes more pronounced with an increase in frequency. (Ref: 1, 2, 3). To maintain predictable performance beyond 160 MHz, a second layout featuring ceramic chip capacitors is offered (Figure 3, 6, 7). The design of these capacitors allows them to remain capacitive beyond the VHF frequencies. Maintaining the bandwidth of 160–174 MHz with this circuit board, the networks become lossy and power output suffers slightly. Variable capacitors may make this condition more tolerable and can be installed in the input and interstage networks. In some cases the ease of adjustment and added flexibility would justify the added cost of the variable capacitors.

Performance

Normally, this amplifier will not require tuning provided that components are as described and are positioned as shown on Figure 5 and 7. If an accurate method of measuring power is available, a quick check of amplifier performance can be accomplished by comparing its parameters with the performance data of Figures 8 through 11. Drive must be maintained at 220 mW (±20 mW) and V_{CC} held to 12.5 Vdc to accurately reproduce the overall response noted here. Allow some degree of tolerance (10%) in output power to account for differences inherent in component values and transistor performance. To assure broadband performance and tailored frequency response, the amplifier should be checked using a swept frequency generator capable of 200–300 mW output. Tuning for maximum power out and minimum reflected power at band centers will not necessarily provide a broadband response. Figures 8 through 11 graphically depict typical levels of performance achieved with this amplifier. Either version is stable into higher than 3:1 VSWR load mismatch at all phase angles. The output device is tolerant of short term operation into an open or short circuit load at full drive.

Harmonic content of a 150 MHz signal at the output of the dipped silver mica version is illustrated in Figure 12. The 2nd harmonic is approximately -50 dB with respect to the fundamental. This level of performance cannot be maintained across the entire band, therefore, some additional filtering of the output signal will be required to meet more stringent requirements.

With the amplifier mounted on aluminum stock, 2.0″ × 8.5″ and 0.090″ thick, a 25% duty cycle (1 min on, 4 min off) produced a temperature of 50°C (122°F) after two hours of operation. A 50% duty cycle (1 min on, 1 min off) raised this temperature to 60°C (140°F) and full key down operation caused a stabilized temperature of 80°C (176°F). All temperatures were measured on the heat sink at the final device with output power maintained at 15 watts. One can safely assume that a panel on the outside edge (i.e., backside) of a transceiver could be successfully used as a heat sink for this amplifier.

References

1. Hatchett, John: 25 Watt and 10 Watt VHF Marine Band Transmitters, AN-595, Motorola Semiconductor Products, Inc.
2. Granberg, H: A Simplified Approach to VHF Power Amplifier Design, AN-791, Motorola Semiconductor Products, Inc.
3. Hollander, D: A 15 Watt AM Aircraft Transmitter Power Amplifier Using Low Cost Plastic Transistors, AN-793, Motorola Semiconductor Products, Inc.

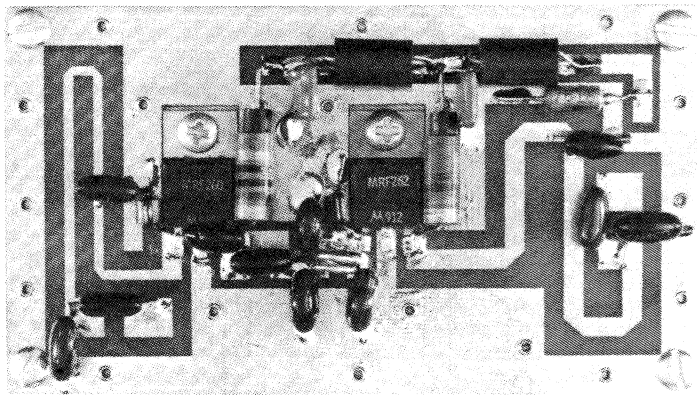


FIGURE 2 — 136-160 MHz Amplifier

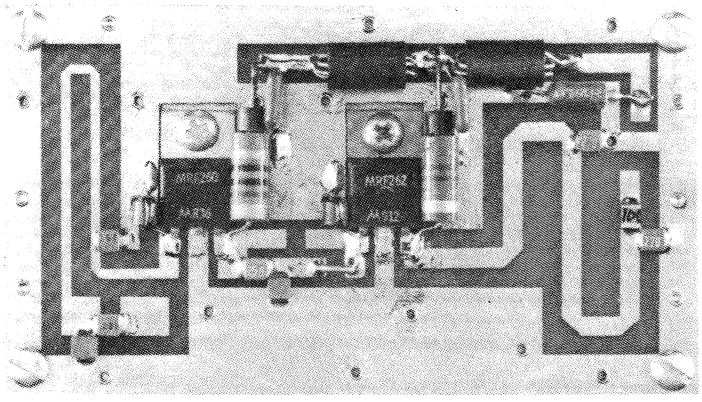


FIGURE 3 — 160-174 MHz Amplifier

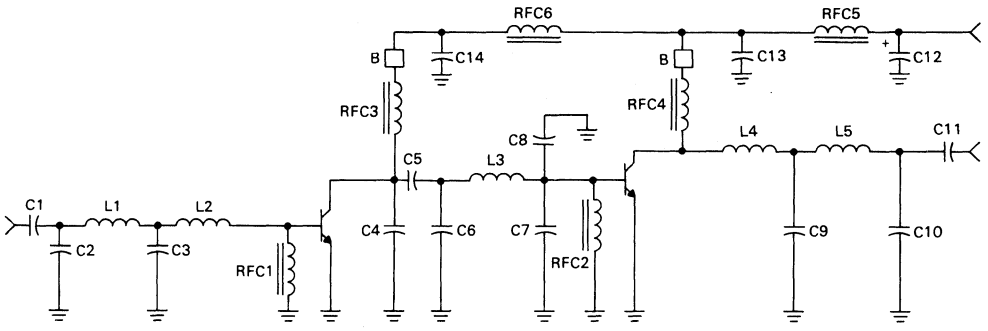
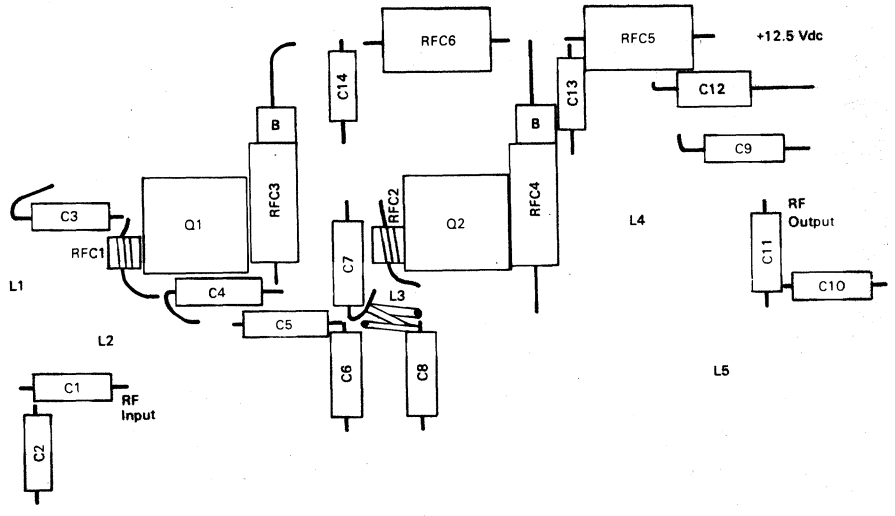


FIGURE 4 — Schematic Diagram of Dipped Silvered Mica Capacitor Version (136-160 MHz)



C1 — 200 pF
C2 — 33 pF
C3 — 47 pF
C4 — 18 pF
C5, C8 — 43 pF
C6 — 12 pF
C7, C9 — 50 pF
C10 — 22 pF
C11 — 100 pF
C12 — 1.0 μF Tantalum
C13, C14 — 0.05 μF Erie Redcap
L1-L5 — Printed Inductor
L3 — 1.25" #18 AWG, 1-1/2 Turns, 9/64 ID
Q1 — MRF260
Q2 — MRF262
RFC1, RFC2 — 2 Turns #26 Enameled on Ferrite Bead Ferroxcube 56-590-65/3B
RFC3 — 10 μH Molded Choke
RFC4 — 0.15 μH Molded Choke
RFC5, RFC6 — VK200-4B
B — Bead, Ferroxcube 56-590-65/3B

FIGURE 5 — Component Placement, 136-160 MHz Amplifier

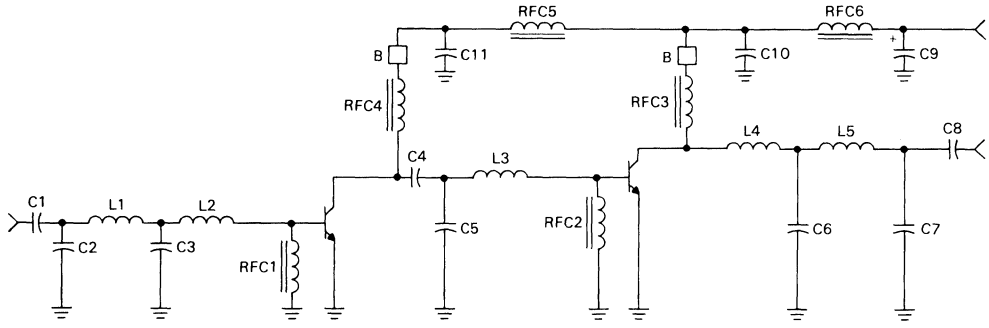
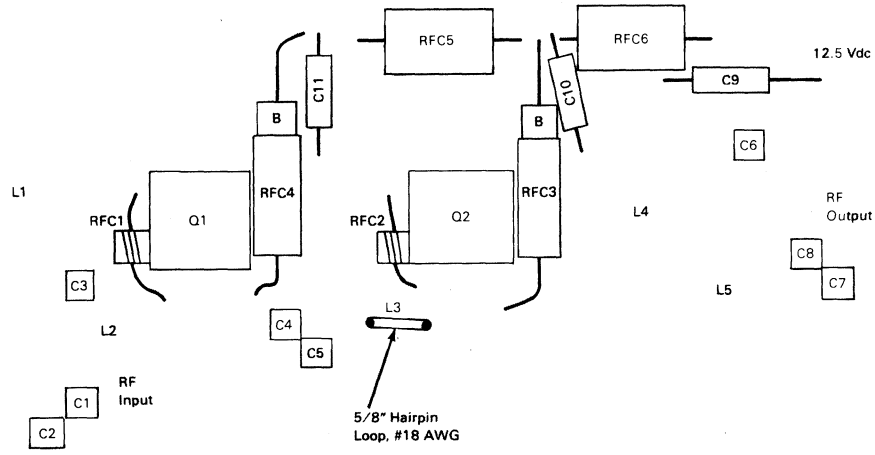


FIGURE 6 — Schematic Diagram of Chip Capacitor Version (160-174 MHz)



C1 — 220 pF, TDK 100 mil Chip Capacitor
C2 — 43 pF, TDK 100 mil Chip Capacitor
C3 — 150 pF, TDK 100 mil Chip Capacitor
C4 — 15 pF, TDK 100 mil Chip Capacitor
C5 — 63 pF, TDK 100 mil Chip Capacitor
C6 — 27 pF, TDK 100 mil Chip Capacitor
C7 — 22 pF, TDK 100 mil Chip Capacitor
C8 — 100 pF, TDK 100 mil Chip Capacitor
C9 — 1.0 μF Tantalum
C10 — 0.1 μF Erie Redcap, 100 V General Purpose
C11 — 0.05 μF Erie Redcap, 100 V General Purpose

L1-L5 — Printed Inductor
L3 — 5/8" #18 AWG Wire formed into hairpin loop
Q1 — MRF260
Q2 — MRF262
RFC1, RFC2 — 2 Turns #26 Enameled Wire through Ferrite Bead Ferroxcube 56-590-65/3B
RFC3 — 0.15 μH Molded Choke
RFC4 — 10 μH Molded Choke
RFC5, RFC6 — VK200-4B
B — Bead, Ferroxcube 56-590-65/3B

FIGURE 7 — Component Placement, 160-174 MHz Amplifier

FIGURE 8 — Power Output versus Frequency, 136-160 MHz Amplifier

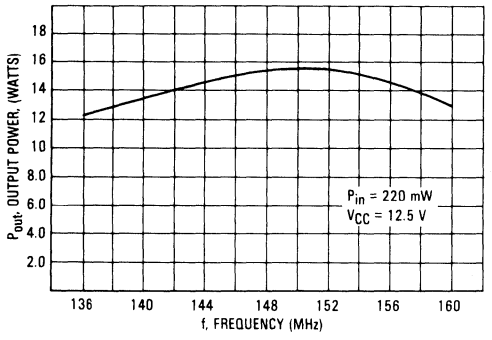


FIGURE 9 — Power Output versus Frequency, 160-174 MHz Amplifier

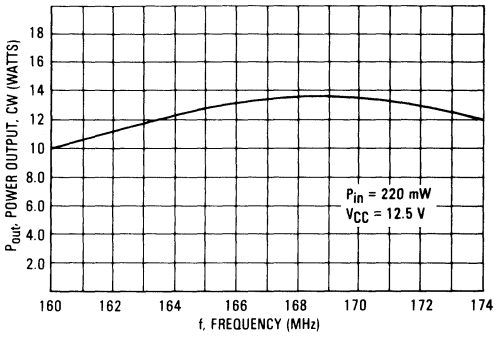


FIGURE 10 — Power Gain and Input VSWR versus Frequency, 136-160 MHz Amplifier

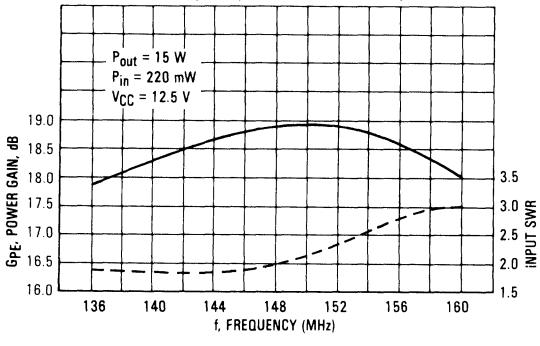


FIGURE 11 — Power Gain and Input VSWR, versus Frequency, 160-174 MHz Amplifier

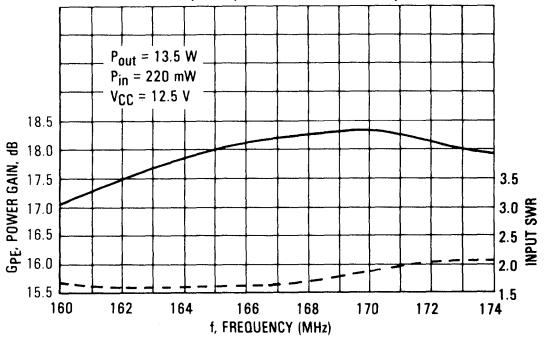


FIGURE 12 — Output Spectrum 136-160 MHz Model

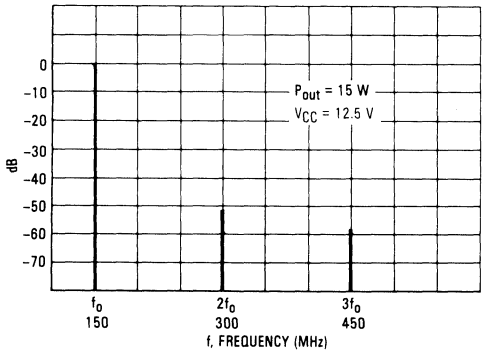
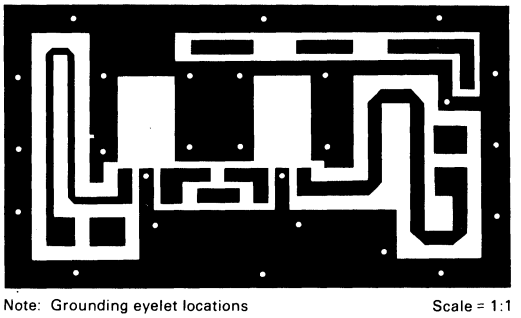


FIGURE 13 – PCB Photomaster (not full size)



Note: Grounding eyelet locations are indicated by dots.

Scale = 1:1

EB93

60 watt VHF Amplifier Uses Splitting/Combining Techniques

Using proven combining techniques to obtain higher output power or added reliability at VHF can be accomplished with excellent results. Simple matching networks and power transistors featuring moderate gain capability can produce a level of performance comparable to that of a single-stage amplifier using a larger, more expensive device. Though not the ultimate answer in VHF amplifier design, the splitter/combiner method does have distinct advantages over designs that brute force the transistors into a parallel configuration. Current hogging and reduced impedance level problems associated with that technique are minimized. The exotic materials or expensive board layout required to produce a true push-pull design operating at VHF again makes combining techniques more appealing.

This 60 W amplifier operates from 150 to 175 MHz and features two, low-cost Motorola MRF264 transistors. These devices are designed for operation at VHF and individually produce 30 watts of rated output power and 6.0 dB of gain with a 12.5 volt supply. The amplifier design makes use of a modified Wilkinson combiner technique to produce 60 watts output with a drive level of 15 watts.

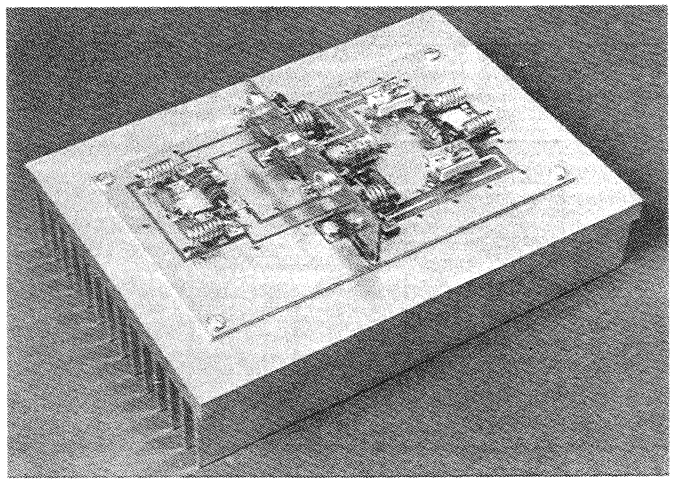


FIGURE 1 — Engineering Model

Design Considerations

Experimental work with 90° (quadrature) couplers proved unsuitable for this application. Generally, they are sensitive to mismatch and tend to create instability and loss of power when used in an amplifier. In-phase (Wilkinson) couplers provide an adequate solution to this problem. (Ref: 1) They are relatively insensitive to phase changes and offer good bandwidth characteristics.

Printed transmission lines for the frequency of interest can become somewhat cumbersome on standard circuit board material. Therefore, lumped reactances (L1, 2, 9, 10 and C1, 2, 3, 14, 15, 16, Figure 5) are used to simulate 70.7 ohm 1/4 wave transmission lines, the main element in the couplers. This approach not only conserves board space, but provides a means to compensate for small variations in associated component values.

Microstrip techniques are incorporated in the amplifier networks to balance RF performance and promote reproducibility. Because of the lower circulating currents and reduced component heating in the collector circuitry of low-powered stages, smaller capacitors can be used in the networks at that point than would be required for a single-ended 60 watt design. Separating the major heat producing devices to two areas on the heatsink produces a more even heat transfer to the ambient air. The combined amplifier presented here has good harmonic suppression (Figure 8). A low-pass filtering effect is noticeable with the Wilkinson combiners.

Construction and Alignment

A 1:1 photomask of the circuit is provided in Figure 9 and double-sided G-10 fiberglass board with two-ounce copper cladding is recommended for construction. The ground points are indicated on the PCB photomask.

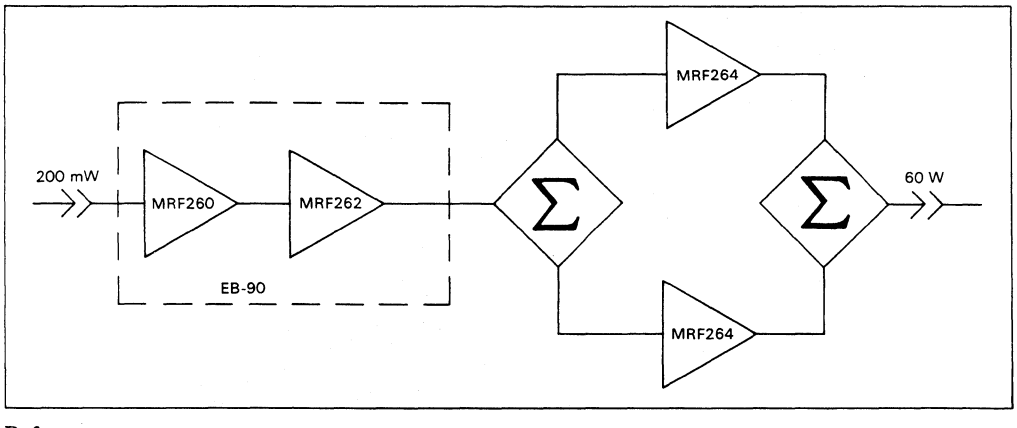
The inductors required for the splitter/combiner are constructed by winding the appropriate number of turns (closewound) on a temporary 1/8 inch form and then separating the individual turns by 0.020 inch. An Xacto number 11 knife blade was used for this purpose and provides the correct turns spacing. The 100-ohm isolation resistors, R1 and R2, must be noninductive and carbon composition resistors proved to be entirely adequate. In a properly tuned and balanced amplifier these resistors should remain fairly cool to the touch during normal operation. Each amplifier and coupler input and output port is designed to be terminated into 50-ohms to facilitate testing into a 50-ohm system.

A PCB bridge (Figures 3 and 9) is used to carry all of the dc feed circuitry. It acts as a continuation of the ground plane and enhances circuit stability. Solid copper (0.027 inch) and double-sided circuit board were used as a construction medium and no difference in performance was noted with either material.

Initial alignment is accomplished by driving the amplifier with a 5 watt CW source at approximately 160 MHz. The applied voltage is set at 12.5 volts and the variable capacitors, C4 and C5, are adjusted in an alternating manner to provide maximum output power. Full drive (15 watts) is then applied and the capacitor adjustments are repeated. At this point, the circuitry should be delivering 60 watts or more to the 50-ohm load with the 15 watts input. After the final adjustments are made, the isolation resistor temperature in either coupler should be relatively cool to the touch and the input VSWR should be at a minimum. Best results will be obtained if the transistors are beta matched (±10%) prior to installing them in the circuit.

Additional Comments

This amplifier has been extensively tested for ruggedness and reproducibility. The 15 watt input level makes it compatible with the EB-90 two-stage VHF amplifier as a driver. Together they form a chain requiring 200 mW of input power for a 60 watt or more output.



References

1. Lawrence R. Laveller; "Two Phased Transistors Shortchange Class C Amps," *Microwaves*, Pg. 48-54, February, 1978.

2. Ernest J. Wilkinson; "An N-Way Hybrid Power Divider," *PGM TT Transactions*, pg. 116-118, January, 1960.

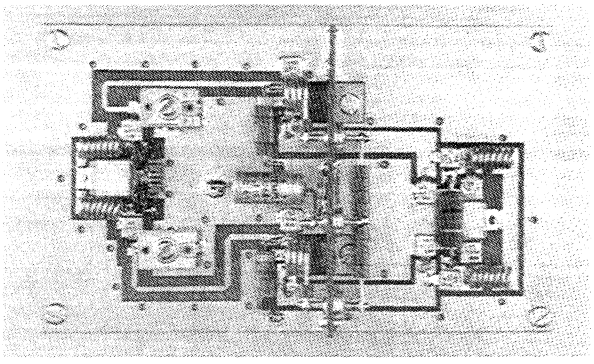


FIGURE 2 — Amplifier Layout - Top View

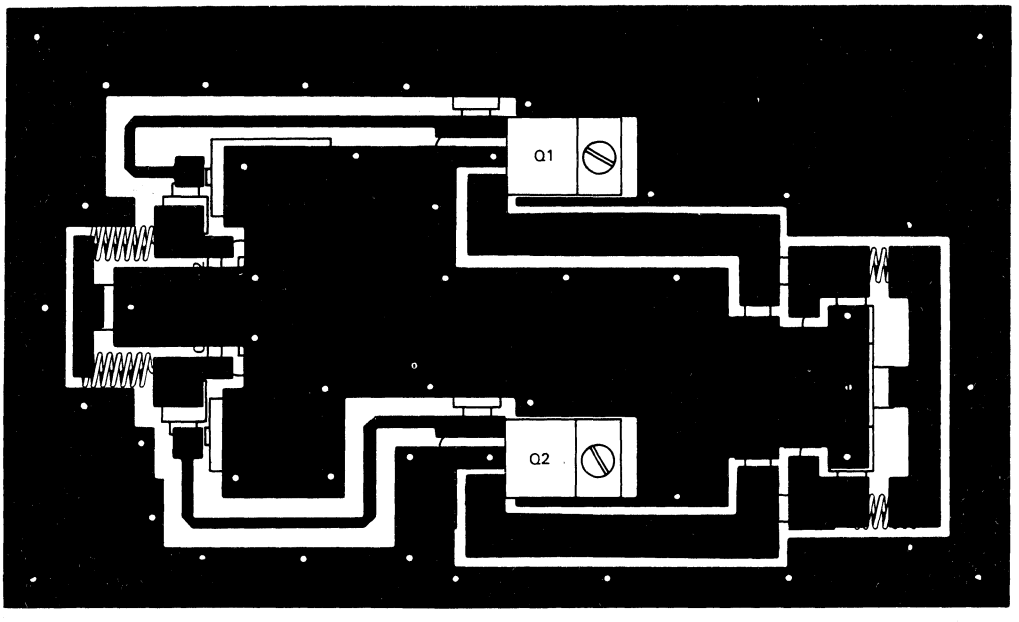
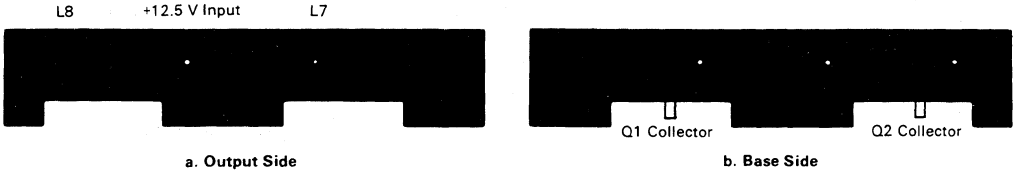


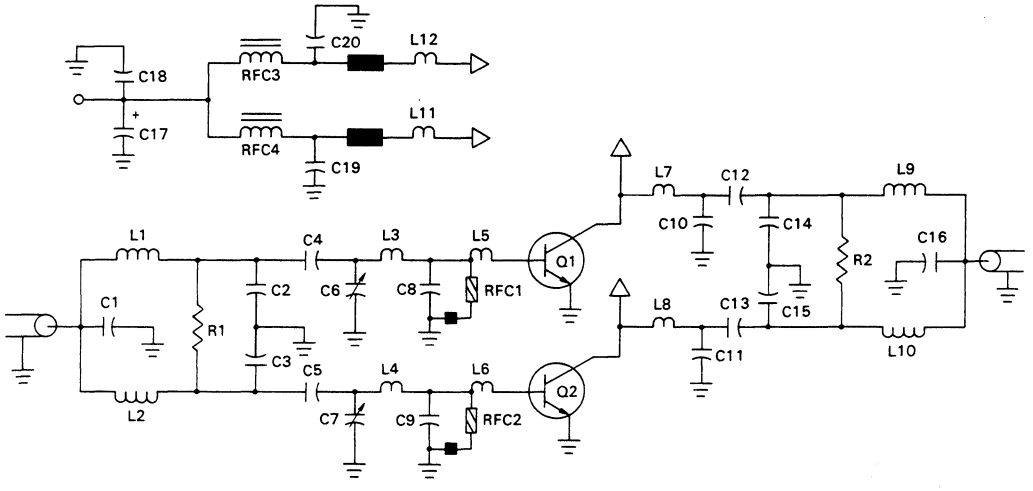
FIGURE 3 — Component Placement



a. Output Side

b. Base Side

FIGURE 4 — PCB Bridge Details



C1, C16 — 25 pF Unelco (J101)
C2, C3 — 15 pF CM04 Mica
C4, C5 — 68 pF Standex
C6, C7 — Arco 404 Variable
C8, C9 — 150 pF Standex
C10, C11 — 56 pF Standex
C12, C13 — 39 pF Standex
C14, C15 — 15 pF Standex
C17 — 100 μF @ 16 V Electrolytic
C18, C19, C20 — 680 pF Allen Bradley Feedthru

L1, L2 — 7 Turns #18, 0.125" ID
L3, L4, L5, L6 — Printed Inductors
L7, L8 — Printed Inductors
L9, L10 — 7 Turns #18 AWG, 0.125 ID
L11, L12 — 4 Turns #18 AWG, 0.250 ID w/Bead
Q1, Q2 — MRF264
RFC1, RFC2 — 0.15 μH Molded Choke w/Bead, Ferroxcube 56-590 65/3B
RFC3, RFC4 — 4 Ferrite Beads each on #18 AWG
R1 — 100 Ω 1/2 W Carbon
R2 — 100 Ω 2.0 W Carbon

FIGURE 5 — Schematic - 60 W Amplifier

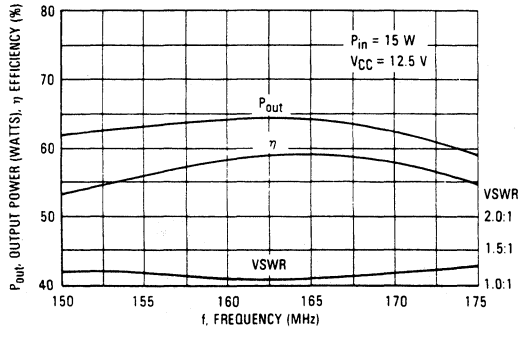


FIGURE 6 — Output Power, Efficiency, and Input VSWR versus Frequency

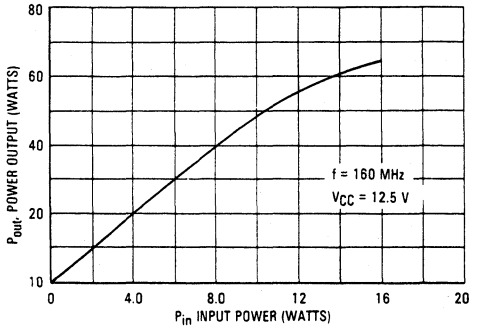


FIGURE 7 — Output Power versus Input Power

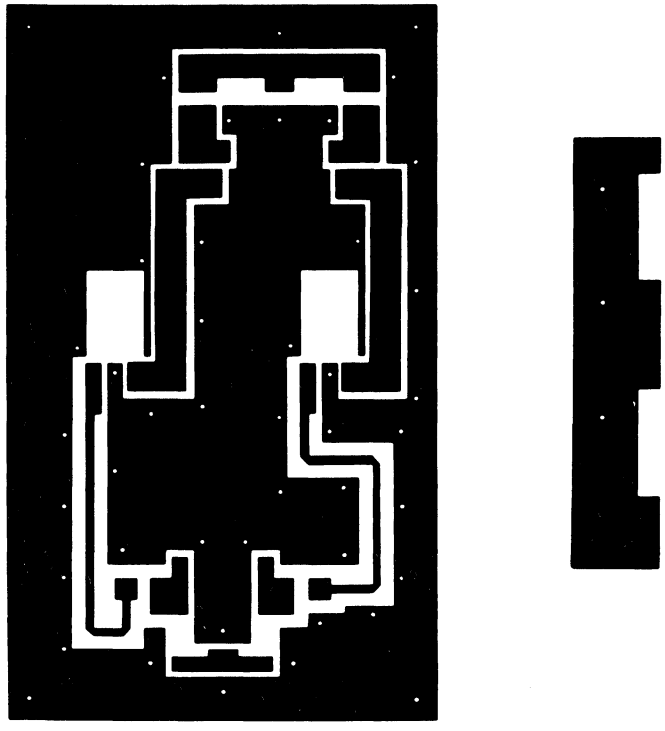


FIGURE 8 – PCB Photomaster (not full size)

Mounting Considerations for Motorola RF Power Modules

INTRODUCTION

The packaging used for standard Motorola RF Power modules consists of a copper flange on which the substrates are soldered and a non-conductive cover which is either of a "snap-on" or epoxy attached design. The ceramic substrates are either 96% alumina ($A1_20_3$), 99.5% alumina or 99% Beryllium oxide (BeO). These substrates are attached to the copper flange using either lead-tin or indium based soft solders. Typical liquidus temperatures of these solders are in the 149°C to 163°C range.

The purpose of this paper is to present the mechanical factors which should be considered in mounting these modules in equipment.

MAJOR MOUNTING FACTORS

There are three major considerations in mounting an RF power module. First, the flange is used for the RF electrical ground reference. Typical inductance of the connection pins used on these modules is about 18 nanohenries per inch or 1.8 nanohenries per 100 mils. Since at 800 MHz a nanohenry has about 5.0 ohms reactance, it is easy to see that it would be almost impossible to achieve a low reactance ground through the use of pins alone. Second, the copper flange provides the thermal path for the removal of the heat produced in the active devices present in the module. Thus, proper thermal handling must be considered in mounting the module. Finally, we must consider the mechanical stresses placed on the module by the mounting techniques used. Here we consider stresses placed on the leads and bending or twisting of the mounting flange which would cause ceramic fractures.

MODULE FLANGE FLATNESS

During the processing of the module, consideration has to be given to the various stresses produced. Through analysis of these stresses and the materials used we can arrive at the maximum allowable flange bending which can be tolerated from a mechanical standpoint. In determining the allowable flange flatness conditions, both analytical and empirical analyses were performed. Agreement between both of these analyses was very good. The theoretical analysis was performed by Motorola Government Electronics Group, Mechanical Engineering Laboratory. GEG was selected to do this work because they have done extensive work in the area of laminate stresses and have available several proven computer programs which apply directly to this problem. The assigned task was to provide an estimate of the maximum amount of initial bow (curvature) in the mounting flange which would not subsequently cause the ceramic substrate to fracture in the final assembled state. For the results of this analysis, see Table 1.

MOUNTING CONSIDERATIONS

The theoretical analysis shows that some of the responsibility for proper mounting rests on the user. Proper consideration should be given to the following items:

1. Flatness of the mounting area must be such that the final mounting of the module will not bend the flange beyond the limits given in Table 1.
2. Attention must be given to surface finish and cleanliness of the mounting surface. For instance, if one mounts the module with thermal compound and uses a dirty work area which allows 3 to 5 mil particles to be present in the compound, a failure mode can be produced.
3. Another consideration is the movement of material around tapped or punched holes. A tapped or punched hole which leaves a burr on the mounting surface can lead to failure modes.
4. In addition, rigidity of the mounting surface and its material should be considered. For instance, the copper flange on an aluminum heatsink will result in a bimetallic system which can create a bending problem. Consideration of the direction of ribs in a heatsink should be made to maximize stiffness in the direction of bending or adequate thickness of the heatsink must be provided to control bending.

It is not desirable to mechanically constrain the ends of the module so that no "slip" is possible between the module flange and its mounting surface. If the ends are constrained and the temperature differential between the module and the heatsink is significant, there can be enough bending of the module flange to break the ceramic. An example calculation is shown below to demonstrate this problem.

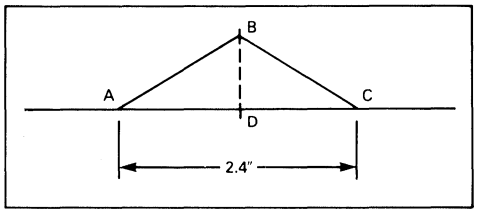
Assume that the ends of the flange are constrained at the centerline of the mounting holes. (2.4 inches for MHW612A/MHW710/MHW720 series modules). Assume

that the module is mounted on a machined aluminum heatsink.

Thermal expansion coefficients in μinch/inch/°C
Aluminum 25 x 10^{-6}
Copper 17 x 10^{-6}
L = 2.4 inches

For a reasonable approximation assume the thermally induced bending creates an isosceles triangle as shown in Figure 1.

FIGURE 1



Assume that the module flange changes temperature from 25°C to 50°C and the heatsink changes temperature from 25°C to 30°C in the same time (obviously the heat input to the system comes from the copper flange — more on this later).

Heatsink $\triangle$ L (aluminum) = 2.4" x 5°C x 25 x 10^{-6}
= 0.0003"
Flange $\triangle$ L (copper) = 2.4 x 25°C x 17 x 10^{-6}
= 0.00102"

So length ABC = 2.40102, AB = 1.20051"
length AC = 2.4003", AD = 1.20015
And $AB^2 = AD^2 + BD^2$
$BD = \sqrt{AB^2 - AD^2}$

So BD = 0.029397 inches which far exceeds the allowable flange bend.

This analysis also points out the advantage of keeping the heatsink and the flange at lowest possible temperature differential through the use of thermally conducting compounds between the surfaces.

For instance, in the example given above with an aluminum/copper system, the copper flange will remain in tension at any temperature *above* the temperature at which the system was constrained as long as the temperature ratio between the heatsink and flange is kept less than the ratio of the thermal expansion coefficients or 25/17. Incidentally, this assumes that the heat input source to the system originates in the copper flange. This situation points out the folly in some types of temperature cycling testing. For instance, if the aluminum/copper system is constrained at 25°C and is uniformly heated to say 125°C, the copper remains in tension — if the system is cooled below 25°C, the copper will go into compression. This is exactly the opposite situation obtained when the heat input to the system comes from the copper flange.

The above is a rather elementary analysis of the thermal effects on the module/heatsink system. Many other factors are involved such as relative strengths of the materials involved, bending of the mounting screws and so forth.

What should be derived from this discussion is that the design of the mounting for the module/heatsink system is not a simple one and should not be done in a casual manner.

Our recommendation is that a mock version of the system be constructed early in the equipment design and thermal cycling performed both with external heat input to the system and with heat input to the system from the module. This is a very effective "analog computer" and direct measurements of the flange/heatsink deflections can be made. In this manner the actual expected flange excursions can be compared to the recommended maximum flange bending to determine whether the design is adequate. Incidentally, the recommended maximum deflection values given in Table 1 have a safety factor of approximately 2. That is, the deflection required to crack the ceramic is approximately twice the value given. Table 1 includes data showing the empirical deflections required to fracture a ceramic board in the module.

5. We strongly recommend the use of a good thermal compound between the mounting surface. Sufficient material must be used to fill all gaps which may be present. We have not been able to create any mechanical problem with excess compound as long as there is a path for the excess material to escape as the module is tightened down with the mounting screws. At this point it should be pointed out that unless both the module flange and the heatsink were lapped to absolute gauge block flatness, there will always be a significant air gap between areas of the flange and the heatsink. Since it is obviously not practical to achieve a lapped surface of this quality, this portion of the mounting problem resolves to one of mechanical rather than thermal considerations. As an aside, some of the Motorola modules also have machined surfaces which may be oxidized to some degree. Infrared thermography of the active die was performed to see if there was any thermal degradation due to this oxide layer and no degradation could be found. This has also been found true on lapped discrete transistor flange mount parts.

Several manufacturers of thermally conductive heatsink compound exist. We have used products from Wakefield and Dow Corning with success.

MOUNTING HARDWARE

Obviously an ideal mounting hardware scheme would be one in which the clamping pressure remained constant with age. One way of achieving this is through the use of conical washers — one trade name is Belleville washers. Another possibility is "wavy" washers. Proper selection of mounting hardware and torque is also necessary. We recommend the following mounting hardware sizes and torques:

4–40	3 in/lb
6–32	5 in/lb
8–32	5 in/lb

TIGHTENING SEQUENCE

A very important factor to be considered in mounting the module is the proper torquing sequence. The personnel involved in mounting the modules should be given careful instruction and their procedures monitored at regular intervals. Since the flanges are punched from a

roll of material, there can sometimes be a small "roll-up" at the end of the mounting flange. If one considers what can happen if the mounting hardware were tightened completely at one end first, it is easy to see that the other end could be "lifted" off the mounting surface well in excess of the allowable flange bending tolerance.

This should be avoided by first lightly alternately snubbing down the mounting hardware "finger-tight." Next, the hardware can be torqued to its final specification again in at least two sequential steps.

THE IMPORTANCE OF THIS TORQUING SEQUENCE CANNOT BE STRESSED TOO HIGHLY

LEADS

The leads used on the standard Motorola RF Power Modules are of either tinned copper, gold or silver plated KOVAR, or pure silver strap, typically 5 to 10 mils thick and 15 to 20 mils wide. The leads are intended for making electrical connections to the modules *only* and are not intended to support the module at any time in the assembly process. Consideration should be given to the stresses which may occur during mounting or testing. Poorly designed test fixtures can create lead stresses far above those encountered in the end-use equipment. It is recommended that the fixture be designed so the leads are always clamped after the flange is clamped and the tolerances be such that an upward force is never placed on the leads, even as the fixture wears. Motorola's specification for lead pull in shear and peel are 908 gm shear and 454 gm peel for BeO boards and 1500 gm shear and 750 gm peel for alumina boards. Modules from PC86, 90, and 91 product lines use BeO boards. Modules from the PC87, PC103 line use one alumina and one BeO board. PC41, PC64, and PC104 use alumina boards.

DEFLUXING

These modules are designed to be manually soldered into an assembly. The modules have a silicone die coat over the active die, MOS capacitors, and nichrome resistors. The die coat used will not withstand the normal flux removal fluids and severe reliability problems could be incurred if the flux removal fluids or solder fluxes penetrate the inside of the module. We recommend a flux activity of no more than R or RMA be used.

CONCLUSION

In mounting RF power modules, the following major areas should be considered:

1. Heatsink flatness.
2. Use thermal compound — eliminate dirt or grit in the compound or on mounting surfaces, use an adequate amount to fill gaps.
3. Tighten modules down in an alternate manner "finger-tight" before final torquing.
4. Be careful with defluxing operations.
5. Consider lead stresses, both in mounting and testing.

TABLE 1 — Maximum Deflection

DEVICES	LINE	THEORETICAL DEFLECTION TO BREAK	***EMPIRICAL DEFLECTION TO BREAK		MAXIMUM RECOMMENDED DEFLECTION COMBINED HEATSINK & FLANGE		OUTGOING QA SPEC. (MAX)	
			MIN	AVG	CONVEX	CONCAVE	CONVEX	CONCAVE
MHW709, 710	PC41	0.015	0.0190	0.0218	0.008	0.010	0.005	0.005
MHW720 *	PC64	0.015	0.0190	0.0206	0.008	0.010	0.005	0.005
MHW720 **	PC64	0.011	0.0075	0.0079	0.007	0.0085	0.003	0.005
MHW720A	PC104	—	0.0190	0.0206	0.008	0.010	0.005	0.005
MHW612, 613†	PC86	0.0025	0.0019	0.0028	0.0015	0.002	0.001	0.002
MHW612A, 613A†	PC87	0.011	0.0103	0.0108	0.007	0.0085	0.003	0.005
MHW808	PC90	—	0.0025	0.0034	0.0015	0.002	0.001	0.002
MHW808A	PC103	—	0.0065	0.0070	0.0035	0.004	0.0015	0.0025
MHW820	PC91	0.005	0.0073	0.0084	0.004	0.005	0.002	0.003

ALL UNITS IN INCHES

* PC64 was changed to alumina board — BeO carrier transistor construction similar to PC41 in February, 1983. All product with date code .883 and after has this construction.

** Old construction of PC64 with total BeO output board.

*** Measured deflection to break a substrate within 3 to 5 seconds of application of force.

† These devices will be obsolete on September 30, 1983. Contact Motorola for the current availability and recommended discrete transistor replacement lineup.

A Digital Video Prototyping System

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1. INTRODUCTION

This Engineering Bulletin describes a Digital Video Prototyping System (DVPS) that has been developed using Motorola's latest multimedia devices, together with a PC-based Field Programmable Gate Array (FPGA) development system. It is designed to provide a fast and effective means of prototyping and demonstrating digital video processing functions. A function developed in this way may later be fully integrated as an ASIC device for use in a consumer end-product.

The focus here is on the functionality of the combination of the above components and development system. A Reference Section lists data-sheets and user manuals containing detailed descriptions and information on their use.

The DVPS has been successfully used to implement two T.V. sub-systems, namely, a Picture-In-Picture Processor and a 4:3-to-16:9 Picture Processor. Those sub-systems are described briefly below.

2. MOTOROLA DEVICES USED

The DVPS takes advantage of several versatile multimedia devices, that are listed below. They are used as a means of generating digital data from virtually any analogue video source, and providing a means of displaying the resulting analogue video signals on a consumer T.V. set, after the digital signal processing function being prototyped.

a) MC44011[1]. This is the multimedia derivative of the MC44001[2]. It performs the function of a Multistandard (PAL/SECAM/NTSC) Chroma Decoder, with a selection between RGB or YUV output signals. The MC44011 also generates a T.V. line-locked clock for digital sampling and subsequent processing of the output signals. The latter function is also available separately in the form of the MC44145[3]. The output stages of the MC44011 are designed to drive the inputs of the MC44250 directly.

b) MC44250[4]. This triple 8-bit Analogue-to-Digital Converter provides black-level clamping for either RGB or YUV signals. These are typically a.c. coupled into the device from the MC44011 which provides the appropriate clamping pulse, but may equally come from any other suitable video source.

c) MC44200[5]. This is the counterpart to the MC44250, a triple 8-bit Digital-to-Analogue Converter for RGB or YUV. It features differential current source outputs designed to drive 75Ω loads with 0.7Vpp.

Other devices used include the MC68HC05B6[6] (8-bit MCU with onboard EEPROM), the MC14576[7] (Dual Video OpAmp) and some standard CMOS logic.

3. FPGA DEVELOPMENT SYSTEM

The digital processing element of the DVPS consists of one or more FPGA devices. These comprise of user Configurable Logic Blocks (CLB's) and I/O Blocks (IOB's) that, together with programmable interconnect, allow most memory control and simple digital video processing circuits to be implemented successfully. The configuration data is stored in internal RAM. The reprogrammable nature of FPGA's makes debugging and development a relatively straightforward process.

The logic capacity of the FPGA devices ranges from 1,200 up to 20,000 equivalent gates, with between 58 and 240 user-programmable I/O's, which is ample for most applications. Their toggle frequency ranges between 50 and 125MHz, and the devices come in a range of package types.

The front-end to the development system is a Schematic Capture Package[8], together with the FPGA Library & Interface running on a Personal Computer. Schematic files are processed by the FPGA Development System[9] to produce a graphical file representing the configuration of the FPGA . This file may be manually edited for routing optimisation before the final binary file is generated. Programming of the FPGA devices may be carried out in one of two ways:

a) The binary file may be directly downloaded from the host computer serial port to a powered device in a matter of seconds. This is the most appropriate for the debugging and development stage, as it turns circuit design changes into a quick and easy process of device reconfiguration. It may be as simple as making an alteration to the schematic diagram and recompiling the design. As long as the device pin-out is unaltered, no rewiring is necessary.

b) When a design has matured and no further changes are expected, the binary file may be programmed into a serial or parallel PROM or EPROM. This is addressed by the FPGA device itself to perform automatic self-configuration of its RAM as part of the power-up sequence.

4. DVPS OVERVIEW

Figure 1 is a block diagram of the DVPS environment. The rack connects together the input card, the digital card(s) and the output card through a backplane. The external controller board also connects to the backplane to perform initialisation and control of the input and output cards. The PC download cable connection is made directly to the digital card(s) for configuration of the FPGA(s). A Video source is connected to the front of the input card; the outputs for connection to the final display are taken from the front of the output card.

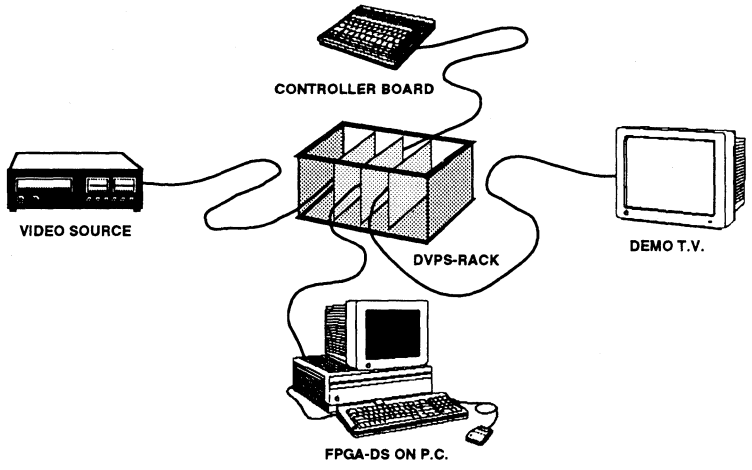

Figure 1. Digital Video Prototyping System

The following three sections describe each card and its functions in more detail. Reference should be made to the appropriate device data-sheet for more detail on application circuit diagrams.

5. INPUT CARD

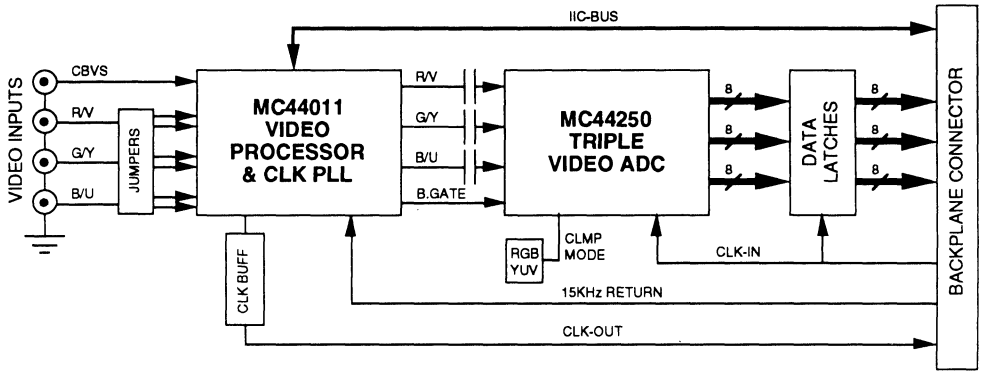

Figure 2. Input Card

The input card accepts various types of video signal sources from which it generates three byte-wide data streams. A T.V. line-locked clock of up to 42MHz is also generated on this card for use in digital processing of the data. Refer to figure 2 for a diagram of the card.

Four BNC connectors at the front of the card constitute the inputs. The first accepts composite video of any standard, or a composite sync signal accompanied by either RGB or YUV signals on the other three inputs. The desired input configuration is selectable through jumper settings on the card. These signals are processed by the MC44011 to perform chroma decoding and RGB matrixing where necessary.

The T.V. line-sync pulse from the signal source acts as a reference for the line-locked PLL that synthesises the clock on-board the MC44011. After suitable buffering, the clock is output from this card for division down to line frequency by a counter in the FPGA on the digital card. A T.V. line-rate signal is returned from that card to the phase/frequency comparator to complete the loop in the MC44011. The exact frequency of the synthesised clock is, therefore, determined by the division ratio set in the FPGA and is always an integral multiple of the T.V. line frequency. Normally this would be chosen to be 27MHz, so that the video signals are sampled at 13.5MHz, as recommended by CCIR Rec. 601[10].

The three signals from the MC44011 are a.c. coupled to the MC44250 inputs for black level clamping to the appropriate levels before conversion. YUV or RGB clamping modes are selectable through a jumper setting. The RGB-mode clamps the back-porch of the signals to the bottom of the ADC input ranges, while the YUV-mode clamps the U and V signals to the middle of the ranges, leaving the Y clamped to the bottom of its ADC range. A burst-gate pulse is generated by the MC44011 to activate the d.c. clamps in the MC44250 at the correct time.

The three 8-bit data streams resulting from the conversion are registered and buffered before being output to the digital card via the backplane.

Further details and circuit diagrams are given in an application note on video capture[11].

6. OUTPUT CARD

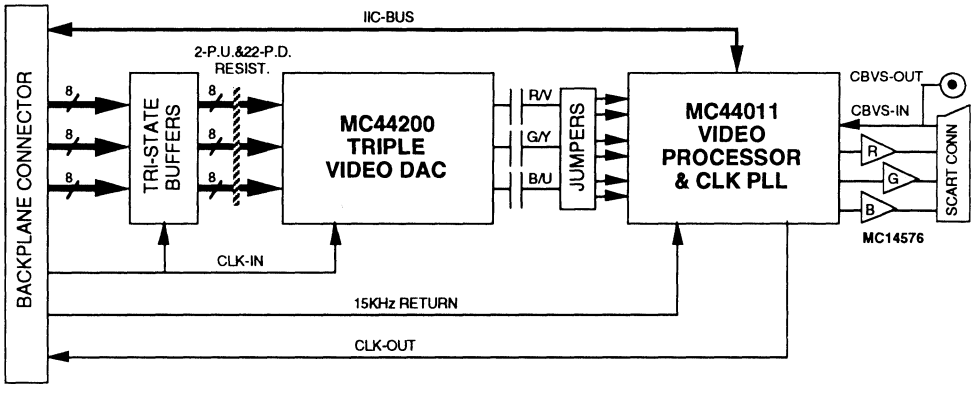

Figure 3. Output Card

The output card, illustrated in figure 3, receives three 8-bit data streams from the digital card. Its purpose is to convert these into the analogue domain for display on a consumer T.V. or RGB monitor. A line-locked clock is also available from this card for applications where the capture and display clock rates are potentially different and/or unrelated.

Access to the output signals is made via a PERITEL (SCART) Connection[12] providing RGB signals, together with a fast-commutate or switching signal. The MC44011 device on this card may also be used to perform the matrixing of YUV signals to RGB, if needed. Configuration of the card for the signal types being processed is set by jumpers, as on the input card. When connected to a T.V. set, the composite video signal coming from the receiver via the PERITEL connection may be used as a reference to which the display clock synthesised by the local MC44011 may be locked. This video signal is also output onto a BNC connector for use as a source for the input card, if the application requires it.

The clock synthesis PLL on this card uses the same principle as on the input card, using a separate counter in the FPGA on the digital card, if the division ratio or line frequency reference is different from that used by the former.

Data from the backplane is first registered by tri-state buffers before being input into the MC44200 for conversion. In the YUV-mode, the m.s.b.'s of the U and V data lines are pulled-up by resistors while all other bits are pulled-down at the inputs of the converter. This ensures that the video of any standard, or a composite sync signal accompanied by either RGB or YUV signals on the analogue outputs from the DAC's, are correctly set for black-level when the input buffers are set in tri-state mode. The MC44011 may then clamp these d.c. levels from the MC44200 and hence provide the right levels for the receiver to display true black.

The RGB signals from the MC44011 are buffered to drive the PERITEL socket with 0.7Vpp at 75Ω, using MC14576 Dual Video OpAmps.

7. DIGITAL CARD

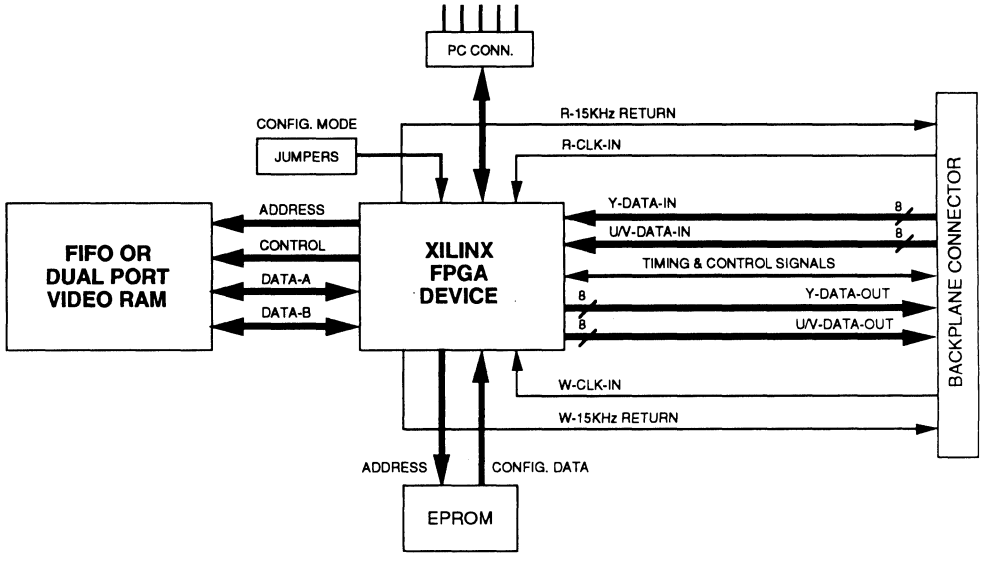

Figure 4. Digital Card

At the centre of the DVPS is the digital card. There may be one or several of these, between the input card and the output card, depending on the complexity of the digital processing required by the application being implemented. The FPGA currently employed in the DVPS is the Xilinx XC3042PC84-100 device. This is a 4,200 equivalent-gate FPGA with a toggle rate of 100MHz, in an 84-pin PLCC package.

In its simplest form the digital card consists of the FPGA device and the means to load its configuration RAM. This entails provision for a parallel or serial PROM and/or a connection for the PC serial download cable.

Invariably, the processing on the digital card involves video data storage that requires memory external to the FPGA. Therefore, FIFO or Dual Port RAM devices would normally also be included on this card, close to the FPGA device. Figure 4 depicts a typical configuration for this card.

As the function of the I/O pins is programmable and application dependent, connections to and from the FPGA pins are made using wire-wrap, once the pinout has been defined.

8. RACK AND BACKPLANE

A 3U-high rack houses the DVPS, providing the mechanical structure for, and the interconnections between, the input card, the digital card(s) and the output card. All the cards described earlier are constructed in the form of extended-eurocards (220mm x 100mm) and use 64-way edge connectors for plugging into the wire-wrapped DVPS backplane.

Here, two external 5V power supply units are used for the digital and analogue sections respectively. All power and ground lines are kept separate on the backplane and on the input and output cards. One star-point connection is made between the grounds at the power supplies to avoid loops between the cards in the rack.

9. CONTROLLER BOARD

The two MC44011 devices on the input and output cards must be initialised and controlled via software using the two wire I^2C-Bus Protocol[13]. For this purpose, an MCU Controller Board[14] built around the MC68HC05B6 8-bit microcontroller, is used with the DVPS.

This is a stand-alone board with a built-in keyboard and an 8-digit 7-segment display. It operates in a pseudo I^2C-Bus mode of communication with the two devices, using three wires to the DVPS backplane. This is necessary because the two identical MC44011 devices, by definition, have the same I^2C-Bus address, so that although they may share the same clock, two separate data lines are needed to maintain separate control using the I^2C-Bus protocol from a single controller board.

The controller board can also be used to manage the vertical picture timing control, as the processing requirements at T.V. line rate lie within the limits of the 4MHz MCU.

10. SYSTEM IMPLEMENTATION EXAMPLES

As mentioned in the introduction, the DVPS has proved to be useful as a flexible prototyping platform for digital video processing functions. This section will briefly describe two projects in which the DVPS was successfully employed to implement functions for demonstration to equipment manufacturers.

a) Picture-In-Picture Processor

Three digital cards were used together with the input card and the output card to emulate a multistandard PIP function. The YUV samples coming from the input card are standard independent by virtue of the MC44011.

The first digital card contains an FPGA to perform data reduction by multiplexing the U and V samples as a means of subsampling these channels and so reducing the data bandwidth by 33%. This takes advantage of the fact that the colour-difference signals each occupy only half the bandwidth of the luminance signal. The two resulting byte-wide data streams (Y, U/V) are then decimated by a factor of nine, using a two-dimensional median-filter. The output data represents the inserted picture but at one third the original height and width.

The second digital card contains dual port video-RAM which stores the data received from the first digital card. The FPGA on this card generates all the control signals necessary to access the memory, as well as performing the divider function for the PLL's on the input and output cards. Its function is to write the data into the memory at 4.5Msamples/s using a clock that is locked to the inserted (PIP) channel, and reading it out again at 13.5Msamples/s using a clock that is locked to the background (MAIN) channel. These two channels may, of course, be asynchronous to each other, hence the requirement of the two separate PLL clock sources.

Data read out of the memory is output to the third digital card. Here, the FPGA demultiplexes the colour-difference samples and interpolates them to reconstitute three byte-wide data streams together with the luminance samples. The YUV data is then converted to analogue signals and matrixed to RGB by the output card.

Here, the MCU controller board was successfully used to perform control of the two MC44011 devices, while also providing vertical timing control and row-addressing for the video memory accesses.

b) 4:3-to-16:9 Picture Processor

A single digital card between the input card and the output card was sufficient to implement a processor to correctly display a 4:3 aspect-ratio picture on a 16:9 aspect-ratio T.V. tube. Here too, the processor is multistandard by virtue of the MC44011 on the input card.

The geometric correction is achieved by writing video data into FIFO memories at 10.125MHz and reading out the data at 13.5MHz. As the read and write clocks are essentially related and both locked to the video derived from the T.V. receiver, only one PLL divider needs to be implemented in the FPGA. All the clocks used are therefore derived from the PLL's fundamental clock frequency of 40.5MHz.

Using the same principle as in the previous example, the two colour-difference data streams are multiplexed into one by the FPGA before being written into the memories along with the luminance samples. The MC44140[15] PAL and SECAM delay-line functions are also performed by this prototype using a further FIFO memory, hence replacing the former device in a system using the MC44001. To this end, the multiplexed colour-difference samples are processed across consecutive pairs of lines, before demultiplexing into separate data streams again and being output for conversion and matrixing by the output card.

11. REFERENCES

Copies of the Motorola data-sheets and application note listed below can be obtained from Motorola Product Marketing, 31023 Toulouse Cedex, France.

(1) MC44011 Chroma Processor & Pixel Clock Generator – MC44011 Advance Information
(2) MC44001 Chroma And Deflection Processor – MC44000 Product Preview
(3) MC44145 Pixel Clock Generator – MC44145 Product Preview
(4) MC44250 Triple Video ADC – MC44250/D Data Sheet
(5) MC44200 Triple Video DAC – MC44200 Product Preview
(6) MC68HC05B6 8-bit Microcontroller – MC68HC05B6/D Data Sheet
(7) MC14576 Dual Video Op-amp – MC14576 Advance Information
(8) OrCAD/SDT Schematic Capture – User Manual
(9) XILINX FPGA Development System – User Manual
(10) CCIR Recommendation 601 – Specification of Standard
(11) Video Capture Applications of the MC44010 & MC44250 – Application Note
(12) Peritel Connection – Specification of Standard
(13) Philips I2C-bus Protocol – Specification of Standard
(14) MCU Controller Board – MC44CTRBD010
(15) MC44140 Digital Delay-line – MC44140 Advance Information

Additional Information

Additional Information

Additional information relevant to Radio, RF and Video applications may be found in the following Motorola documents, available through your Franchised Distributor by quoting the appropriate reference.

AN1051/D	Transmission Line Effects in PCB Applications
BR347/D	Bipolar Logic Circuits — Quality & Reliability
BR470/D	Motorola Discretes – The Complete Solution *(Rev. 1)*
BR475/D	Advanced Logic Functions
BR904/D	MIL-Processed Devices: Technical Data
BR923/D	Communications, Power & Signal Technologies Group, Reliability Audit Report, September-December 1993
BR924/D	Military Analog Lineup
BR1130/D	Coming Through Loud and Clear
BR1305/D	Linear Integrated Circuits: New Product Calendar, January 1994
BR1330/D	ECLinPS Lite Single Gate ECL Devices
BR1332/D	Logic Integrated Circuits Division: New Product Calendar – Second Quarter, 1994
BR1333/D	Low Skew Clock Drivers & Programmable Delay Circuits *(Rev. 3)*
BR1334/D	High Performance Frequency Control Products *(Rev. 1)*
BR1409/D	ECL300 Logic Array
BR1415/D	Military Telecom Special Functions
BR1418/D	Military Analog, Telecom and Special Functions Fact Sheet, June 1992
BR1429/D	Wideband Linear Amplifiers – CATV, CRT Drivers, General Purpose
BRE378/D	UnitPAK Packaging
BRE504/D	Electronic Tuning Address Systems
DL110/D	RF Device Data *(Rev. 5, 1994)*
DL111/D	Bipolar Power Transistor Data *(Rev. 6, 1992)*
DL122/D	MECL Device Data *(Rev. 5, 1993)*
DL126/D	Small-Signal Transistors, FETs and Diodes Device Data *(Rev. 4)*
DL128/D	Linear and Interface Integrated Circuits *(2 volume set, Rev. 4, 1993)*
DL140/D	High Performance ECL Data – ECLinPS and ECLinPS Lite *(Rev. 2, 1993)*
DL145/D	Military MECL Family Data
DL148/D	Discrete Military Operations Data
DL151/D	Rectifier Device Data *(Rev. 1. Replaces DL125/D)*
DL410/D	Power Applications Manual *(Rev. 1)*
DL411/D	Communications Applications Manual *(Rev. 1)*
DL414/D	FET Applications Manual
HB205/D	MECL System Design Handbook *(Rev. 1)*
SG46/D	RF Products Selector Guide & Cross Reference – 1994 *(Rev. 11, 1994)*
SG138/D	Commercial Plus and Mil/Aero Application IC & Discrete Selector Guide *(Rev. 5, 1993)*
SG140/D	SCANSWITCH Selector Guide *(Rev. 1, 1990)*
SG169/D	Mixed Signal Solutions from MOS Digital-Analog Integrated Circuits Division – Quarter 1, 1994
SG270/D	Discrete Semiconductor Cross Reference Guide – 1992
SG365/D	Low Skew Clock Drivers and Programmable Delay Circuits *(Rev. 2)*
SG366/D	TTL, ECL, CMOS and Special Logic Circuits Selector Guide *(Rev. 3, 1993)*

Additional Information (continued)

SG370/D	Discrete Surface Mount Selector Guide *(Rev. 1, 1994)*
SGE112/D	Cross Reference for NEC-to-Motorola RF Transistors
TB326/D	Radio Frequency Transistors: Principles and Practical Applications *(Dye and Granberg, 1993)*

Literature Distribution Centres:

EUROPE:	Motorola Ltd., European Literature Centre, 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
ASIA PACIFIC:	Motorola Semiconductors (H.K.) Ltd., Silicon Harbour Center, No. 2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
JAPAN:	Nippon Motorola Ltd., 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
USA:	Motorola Literature Distribution, P.O. Box 20912, Phoenix, Arizona 85036.